

KD11-Z

11/44 MEM MGMT PRT A
CKKTA00

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IDENTIFICATION

PRODUCT CODE: AC-F609A-MC
PRODUCT NAME: CKKTAA0 11/44 MEM MGMT PRT A
DATE: OCTOBER, 1979
MAINTAINER: DIAGNOSTIC ENGINEERING
AUTHOR: J. PETER BRADY

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PROGRAM HISTORY

<u>DATE</u>	<u>REVISION</u>	<u>REASON FOR REVISION</u>
OCTOBER, 1979	A	FIRST RELEASE

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89
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91

TABLE OF CONTENTS

- 1.0 PROGRAM INFORMATION
 - 1.1 ABSTRACT
 - 1.2 REQUIREMENTS
 - 1.3 RELATED DOCUMENTS AND STANDARDS
 - 1.4 PRELIMINARY PROGRAMS

- 2.0 OPERATING INSTRUCTIONS
 - 2.1 LOADING PROCEDURES
 - 2.2 STARTING PROCEDURES
 - 2.3 OPERATIONAL SWITCH SETTINGS
 - 2.4 LOADING THE SWITCH REGISTER
 - 2.5 EXECUTION TIMES

- 3.0 ERROR INFORMATION
 - 3.1 ERROR REPORTING PROCEDURES
 - 3.2 INTERPRETING ERROR REPORTS
 - 3.3 SAMPLE ERROR REPORT

- 4.0 MISCELLANEOUS INFORMATION
 - 4.1 ACT/APT/XXDP COMPATABILITY
 - 4.2 END-OF-PASS MESSAGE
 - 4.3 T-BIT TRAPPING
 - 4.4 POWER FAILURE HANDLING
 - 4.5 PHYSICAL BUS ADDRESS CONSTRUCTION

- 5.0 PROGRAM DESCRIPTION
 - 5.1 SUBROUTINES USED BY THIS PROGRAM
 - 5.2 PROGRAM LISTING
 - 5.3 USING THE PROGRAM TO DIAGNOSE A FAULT

93
94
95
96
97
98
99
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101
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106
107
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1.0 PROGRAM INFORMATION

1.1 ABSTRACT

THIS PROGRAM WAS DESIGNED USING A 'BOTTOM UP' APPROACH STARTING WITH THE SMALLEST SEGMENT OF MEMORY MANAGEMENT LOGIC POSSIBLE AND BUILDING TO COVER ALL OF THE LOGIC. THE DIAGNOSTIC WILL PROVIDE ENOUGH INFORMATION SUCH THAT BY DEDUCTION, THE FAILURE CAN BE ISOLATED TO A SMALL SEGMENT OF THE MEMORY MANAGEMENT LOGIC.

PART A BEGINS BY TESTING SOME OF THE INTERNAL CPU DATA AND ADDRESS PATHS AND ADDRESS DETECTION LOGIC, THEN WORKS OUTWARD THROUGH THE MEMORY MANAGEMENT REGISTERS. AFTER THE REGISTERS ARE FOUND TO BE USEABLE, RELOCATION (CONSTRUCTION OF PHYSICAL ADDRESSES FROM A VIRTUAL ADDRESS AND THE ASSOCIATED PAR/PDR INFORMATION) IS TESTED. PART B BEGINS BY TESTING THE ABORT AND STATUS SEGMENTS OF LOGIC. PART B THEN CHECKS THE SPECIAL ABORT SEQUENCES, THE MFPI/MTPI INSTRUCTIONS AND THE CSM INSTRUCTION.

1.2 REQUIREMENTS

A PDP 11/44 PROCESSOR WITH A MINIMUM OF 16K OF MEMORY AND A CONSOLE TERMINAL ARE REQUIRED TO RUN THE PROGRAM UNLESS THE PROGRAM IS RUNNING UNDER APT OR ACT IN WHICH CASE THE CONSOLE TERMINAL IS NOT NECESSARY.

1.3 RELATED DOCUMENTS AND STANDARDS

1. ACT11/XXDP PROGRAMMING SPECIFICATION
2. STANDARD APT SYSTEM TO A PDP11 DIAGNOSTIC INTERFACE
3. DIAGNOSTIC ENGINEERING STANDARDS AND CONVENTIONS
4. PDP11 MAINDEC SYSMAC PACKAGE
5. XXDP USER'S MANUAL

1.4 PRELIMINARY PROGRAMS

BEFORE THIS MEMORY MANAGEMENT DIAGNOSTIC IS RUN, THE FOLLOWING DIAGNOSTICS SHOULD BE RUN:

CKKAAA0 1/44 CPU/EIS
CKKABA0 11/44 TRAPS

ALSO, THE MAIN MEMORY DIAGNOSTIC (CZMSD) SHOULD BE RUN TO SCAN AT LEAST THE FIRST 16K TO SEE THAT A PROGRAM CAN BE EXECUTED.

2.0 OPERATING INSTRUCTIONS

2.1 LOADING PROCEDURES

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THE PROGRAM IS SUPPLIED ON THE DIAGNOSTIC LOAD MEDIA. REFER TO THE XXDP USER'S MANUAL FOR FURTHER INFORMATION. FOR USE WITH ACT OR APT, REFER TO THEIR RESPECTIVE DOCUMENTS. THE PROGRAM CAN ALSO BE DIRECTLY LOADED USING THE ABSOLUTE LOADER AND THE BINARY PAPER TAPE.

2.2 STARTING PROCEDURES

THE PROGRAM IS STARTED BY LOADING ADDRESS 200 AND STARTING. THE SWITCH REGISTER SHOULD BE SET ACCORDING TO SECTION 2.3 BEFORE THE PROGRAM IS STARTED. HOWEVER, IF DESIRED, THE PROGRAM WILL USE THE SOFTWARE SWITCH REGISTER AT LOCATION 176 (LOCATION 174 WILL BE USED AS THE SOFTWARE DISPLAY REGISTER). IN THAT CASE, THE PROGRAM WILL ASK FOR THE INITIAL SWITCH REGISTER VALUE BY TYPING 'SWR= XXXXXX NEW= ' AFTER TYPING THE NAME OF THE PROGRAM (XXXXXX = THE OCTAL CONTENTS OF LOCATION 176). (SEE SECTION 2.4)

ALSO THE PROGRAM CAN BE MADE TO USE THE SOFTWARE SWITCH REG. EVEN IF THE CONSOLE SWITCH REG. IS PRESENT BY LOADING '177777' INTO THE CONSOLE SWITCH REG. BEFORE STARTING THE PROGRAM.

2.3 CONTROL SWITCH SETTINGS

SWITCH	OCTAL VALUE	USE
SW15	100000	HALT ON ERROR THIS SWITCH WHEN SET WILL HALT THE PROCESSOR WHEN AN ERROR IS DETECTED AFTER THE ERROR MESSAGE HAS BEEN TYPED. PRESSING CONTINUE WILL RESUME TESTING (SEE SECTION 3.1 ABOUT LOADING THE SWITCH REG BEFORE CONTINUING).
SW14	040000	LOOP ON TEST THIS SWITCH WHEN SET WILL CAUSE THE PROGRAM TO LOOP ON THE CURRENT SUBTEST.
SW13	020000	INHIBIT ERROR TYPEOUTS THIS SWITCH WHEN SET WILL INHIBIT THE TYPING OF ERROR MESSAGES.
SW12	010000	INHIBIT TRACE TRAP THIS SWITCH WHEN SET WILL INHIBIT T-BIT TRAPPING WHICH NORMALLY TAKES PLACE DURING EVERY OTHER PASS STARTING WITH THE THIRD PASS.
SW10	002000	BELL ON ERROR

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THIS SWITCH WHEN SET WILL RING
THE CONSOLE TERMINAL BELL WHEN
AN ERROR HAS BEEN DETECTED.

SW9 001000

LOOP ON ERROR

THIS SWITCH WHEN SET WILL
CAUSE THE PROGRAM TO LOOP ON THE
FIRST FAILURE WHICH IS ENCOUNTERED
EVEN IF THE FAILURE IS INTERMITTANT

SW8 000400

LOOP ON TEST IN SWR<7:0>

THIS SWITCH WHEN SET WILL
CAUSE THE PROGRAM TO LOOP ON THE
TEST WHOSE TEST NUMBER IS SET
IN BITS 7-0 OF THE SWITCH REG.

2.4 LOADING THE SWITCH REGISTER

THE CONSOLE SWITCH REGISTER PROVIDED IS LOADED DIRECTLY FROM
THE CONSOLE BY TYPING A CONTROL P (^P), THEN WHEN THE CONSOLE
PROMPT IS RECEIVED, TYPE 'D SW XXXXXX', WHERE 'XXXXXX' IS THE
INTENDED VALUE OF THE SWITCH REGISTER. THE VALUE OF THE
CONSOLE SWITCH REG. CAN BE CHANGED ANY TIME WHETHER THE PROGRAM
IS RUNNING OR NOT.

TO LOAD THE SOFTWARE SWITCH REG. WHILE THE PROGRAM IS
RUNNING, A CONTROL G (^G) SHOULD BE TYPED ON THE CONSOLE
TERMINAL. (THE 'SCOPE' AND 'ERROR' ROUTINES CHECK TO SEE
IF A ^G HAS BEEN TYPED.) THE ORIGINAL VALUE OF THE SOFTWARE
SWITCH REG. WILL BE REQUESTED AS MENTIONED IN SECTION 2.2.

IN RESPONSE TO A ^G OR AT THE BEGINNING OF THE PROGRAM, THE
PROGRAM WILL TYPE:

SWR = XXXXXX NEW =

WHERE 'XXXXXX' IS THE CURRENT OCTAL CONTENTS OF LOC. 176.
THE OPERATOR MAY THEN TYPE ANY ONE OF THE FOLLOWING:

XXXXXX<CR> ONE TO SIX OCTAL DIGITS FOLLOWED BY A
CARRIAGE RETURN WHICH WILL BE LOADED
AS THE NEW VALUE FOR THE SWITCH REG.
<CR> JUST A <CR>, LEAVES THE SWITCH REG.
AS IT IS.
XXX^U A CONTROL-U (^U) WILL CAUSE ALL OF THE
DIGITS TYPED SO FAR TO BE IGNORED.
^C WILL CAUSE THE PROGRAM TO TYPE THE PRESENT
TEST AND PASS NUMBERS, REQUEST A NEW VALUE
FOR THE SWITCH REG., AND JUMP TO THE END-
OF-PASS ROUTINE SO THE PROGRAM WILL GO DIRECTLY
TO THE NEXT PASS WITH A NEW SW. REG. VALUE
<ILL.CHAR> ANY CHARACTER TYPED WHICH IS NOT ANY OF THE
ABOVE OR AN OCTAL DIGIT WILL CAUSE THE PROGRAM
TO TYPE A '?<CRLF>' AND REACT AS THOUGH A
^U HAD BEEN TYPED.

NOTE: RECOGNITION OF A ^G MAY BE HAMPERED BY

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----- EXECUTION OF A COUPLE 'RESET' INSTRUCTIONS
WITHIN THE PROGRAM.

2.5 EXECUTION TIMES

THE RUN TIME FOR A SINGLE PASS WITH TRACE TRAPPING
ENABLED IS APPROXIMATELY 8 SECONDS WITH CACHE.

3.0 ERROR INFORMATION

3.1 ERROR REPORTING PROCEDURES

IF AN ERROR IS DETECTED, THE PROGRAM WILL TRAP TO THE
ERROR HANDLING ROUTINE (\$ERROR). THE VALUE OF BITS
15,13,10, AND 9 IN THE SWITCH REGISTER ARE CONSIDERED
IN REPORTING AN ERROR (SEE SECTION 2.3). THE
ERROR INFORMATION WILL BE TYPED UNLESS SW13 = 1.

IF SW15 = 1, THE PROCESSOR WILL HALT AFTER THE ERROR IS
REPORTED. IF THE CONTENTS OF THE SOFTWARE SWITCH REGISTER
ARE TO BE CHANGED, A ^G SHOULD BE TYPED BEFORE PRESSING
'CONTINUE' TO RESUME TESTING.

IF SW9 = 1 (LOOP ON ERROR), THE PROGRAM WILL GO TO THE
ADDRESS CONTAINED IN LOCATION '\$LPERR'. AFTER REPORTING
THE ERROR, '\$LPERR' IS SET BY EACH 'SCOPE' CALL AND IS
SET DIRECTLY DURING SOME SUBTESTS TO PROVIDE THE SMALLEST
LOOP FOR LOOPING ON ERROR. IF SW9 = 0, THE PROGRAM WILL
RETURN TO THE INSTRUCTION FOLLOWING THE ERROR CALL.
(SEE SECTION 5.3 FOR MORE ON 'LOOP ON ERROR').

3.2 INTERPRETING ERROR REPORTS

EVERY ERROR REPORT TYPES THE NUMBER OF THE TEST IN WHICH
THE ERROR TOOK PLACE (TESTNO) AND THE LOCATION OF THE
ERROR CALL (ERRORPC). THESE TWO VALUES PINPOINT THE
PLACE IN THE CODE THAT THE ERROR OCCURRED. BY REFERRING
TO THE PROGRAM LISTING, THE OPERATOR CAN THEN READ THE
COMMENTS ASSOCIATED WITH THAT PARTICULAR ERROR AND SUBTEST.
A DESCRIPTION OF THE TEST FOUND IN THE PROGRAM LISTING
WILL ALSO PROVIDE THE OPERATOR WITH INFORMATION ON THE LOGIC
AND FUNCTIONS BEING TESTED.

EVERY ERROR REPORT ALSO TYPES AN ERROR MESSAGE
GIVING A VERBAL DESCRIPTION OF THE ERROR THAT HAS
BEEN DETECTED.

BY USING THE COMMENTS AND TEST DESCRIPTION FOUND IN
THE PROGRAM LISTING TO DETERMINE WHAT FUNCTION OR
LOGIC WAS BEING TESTED, THE OPERATOR CAN THEN REFER
TO THE ENGINEERING DRAWINGS TO ISOLATE THE PROBABLE
CAUSE FOR THE FAILURE.

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3.3 SAMPLE ERROR REPORT

BELOW IS AN EXAMPLE OF AN ERROR WHICH COULD HAVE OCCURRED DURING EXECUTION OF THE PROGRAM:

MEM. MGMT. REG. BITS NOT SET CORRECTLY
REGISTR WROTE READ READ-(BINARY)
ADDRESS (OCTAL) (OCTAL) 5432109876543210 TESTNO ERRORPC
177572 040000 060000 0110000000000000 000012 022060

WE SEE THAT THE ERROR OCCURRED IN TEST 12 AT LOCATION 022060. THE 'REGISTER ADDRESS' TELLS US THAT WE WERE TESTING MEMORY MANAGEMENT'S STATUS REGISTER 0 (SRO). IN THE LISTING, THE TEST DESCRIPTION SAYS THAT THE ERROR BITS (BITS <15:13>) OF SRO WERE BEING SET AND CLEARED INDIVIDUALLY. THE ERROR REPORT SAYS WE TRIED TO SET BIT 14 BY WRITING '040000' TO SRO BUT WHEN WE READ IT BACK WE READ '060000'. IT APPEARS THAT BIT 13 IS STUCK AT '1' OR IT IS GETTING SET WHEN BIT 14 IS SET TO '1'. ERROR REPORTS BEFORE AND AFTER THIS ONE COULD TELL US WHICH IS THE CASE.

4.0 MISCELLANEOUS INFORMATION

4.1 ACT/APT/XXDP COMPATABILITY

THE PROGRAM IS FULLY ACT AND APT COMPATABLE AND IS SUPPORTED UNDER THE XXDP PACKAGE.

4.2 END-OF-PASS MESSAGE

AT THE END OF EACH PASS OF THE PROGRAM THE PASS NUMBER AND TOTAL NUMBER OF ERRORS SINCE THE LAST END-OF-PASS ARE REPORTED IN THE END-OF-PASS MESSAGE. FOR EXAMPLE:

END OF PASS #2 TOTAL ERRORS SINCE LAST REPORT 0

THAT WOULD INDICATE THAT PASS TWO WAS JUST COMPLETED AND NO ERRORS WERE DETECTED DURING THAT PASS. BOTH THE PASS NUMBER AND NUMBER OF ERRORS ARE DECIMAL NUMBERS.

4.3 T-BIT TRAPPING

THE 'T-BIT' (BIT 4) IN THE PROCESSOR STATUS WORD IS SET BY AN 'RTI' IN THE END-OF-PASS ROUTINE FOR EVERY OTHER PASS BEGINNING WITH THE THIRD PASS (PASSES 3,5,7,9...). T-BIT TRAPPING CAN BE INHIBITED BY SETTING BIT 12 = 1 IN THE SWITCH REGISTER (SEE SECTION 2.4).

4.4 POWER FAILURE HANDLING

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NOTE ALSO THAT THE MACRO LIBRARY USED TO ASSEMBLE THIS PROGRAM HAS OTHER SPECIAL ROUTINES APPENDED TO THE SYSMAC MACRO PACKAGE; THIS LIBRARY MUST BE USED TO ASSEMBLE EITHER PART A OR PART B CORRECTLY.

5.2 PROGRAM LISTING

A TABLE OF CONTENTS APPEARS AT THE BEGINNING OF THE LISTING WHICH CONTAINS THE NAMES OF EACH SECTION, SUBTEST, AND ROUTINE AND THE LINE NUMBERS CORRESPONDING TO THE START OF EACH.

FOLLOWING THIS SECTION OF DOCUMENTATION IS THE ACTUAL PROGRAM LISTING COMPLETE WITH SUBTEST DESCRIPTIONS AND 'CODING COMMENTS'.

5.3 USING THE PROGRAM TO DIAGNOSE A FAULT

WHEN AN ERROR OCCURS, ONE OF THE THINGS THAT'S IMPORTANT TO NOTE IS WHAT PASS THE ERROR OCCURRED ON. IF THE PASS NUMBER IS ODD AND IS THREE OR GREATER, THE ERROR MIGHT BE T-BIT SENSITIVE. TRY RUNNING THE PROGRAM AGAIN WITH BIT 12 OF THE SWITCH REG. EQUAL TO '1' TO INHIBIT T-BIT TRAPPING. THIS SHOULD HELP YOU DETERMINE WHAT MAKES THE MACHINE FAIL AND WHEN.

IF YOU HAVE BEEN RUNNING WITH BIT 15 OF THE SWITCH REG. EQUAL TO '0', THEN YOU ARE ABLE TO LOOK AT ALL THE ERRORS THAT MAY BE RELATED TO THE FAULT YOU ARE DIAGNOSING. A FAULT IN AN EARLIER TEST MAY RESULT IN ERRORS DURING LATER TESTS WHICH MAY GIVE YOU MORE CLUES ABOUT THE NATURE OF THE FAULT. NOW USE THE METHOD OUTLINED IN SECTION 3.2 FOR EACH ERROR TO GATHER AS MUCH INFORMATION AS POSSIBLE.

NOW TO TEST YOUR IDEAS ON THE CAUSE OF THE FAILURE, YOU MAY WANT TO SCOPE THIS ERROR CONDITION. SET BIT 09 OF THE SWITCH REG. EQUAL TO '1' TO LOOP ON THE ERROR. FOR AN EVEN TIGHTER SCOPE LOOP THE ERROR CALL CAN BE REPLACED WITH A BRANCH (REFER TO COMMENTS BY ERROR CALLS IN THE PROGRAM LISTING).

OR YOU COULD LOOP ON THE TEST BY EITHER SETTING BIT 14 OF THE SWITCH REG. EQUAL TO '1' OF BY SETTING BIT 08 OF THE SWITCH REG. EQUAL TO '1' AND THEN SETTING THE TEST NUMBER IN BITS 07-00 OF THE SWITCH REG. YOU WILL PROBABLY WANT TO INHIBIT ERROR TYPEOUTS BY SETTING BIT 13 OF THE SWITCH REG. EQUAL TO '1'.

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.TITLE CKKTAAO 11/44 MEM MGMT PRT A
.*COPYRIGHT (C) 1979
.*DIGITAL EQUIPMENT CORP.
.*MAYNARD, MASS. 01754
.*
.*
.*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
.*PACKAGE (MAINDEC-11-DZQAC-C3), JAN 19, 1977.
.*

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.SBTTL OPERATIONAL SWITCH SETTINGS
.*
.*      SWITCH      USE
.*      -----      -----
.*      15          HALT ON ERROR
.*      14          LOOP ON TEST
.*      13          INHIBIT ERROR TYPEOUTS
.*      12          INHIBIT TRACE TRAP
.*      10          BELL ON ERROR
.*      9           LOOP ON ERROR
.*      8           LOOP ON TEST IN SWR<7:0>

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001100
104000
000004

000011
000012
000015
000200
177776
177776
177774
177772
177570
177570

000000
000001
000002
000003
000004
000005
000006
000007
000006
000007

000000
000040
000100
000140
000200
000240
000300
000340

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.SBTTL BASIC DEFINITIONS
.*INITIAL ADDRESS OF THE STACK POINTER *** 1100 ***
STACK= 1100
      ERROR=EMT
      SCOPE=IOT

.*MISCELLANEOUS DEFINITIONS
HT= 11          ::CODE FOR HORIZONTAL TAB
LF= 12          ::CODE FOR LINE FEED
CR= 15          ::CODE FOR CARRIAGE RETURN
CRLF= 200       ::CODE FOR CARRIAGE RETURN-LINE FEED
PS= 177776     ::PROCESSOR STATUS WORD
      PSW=PS
STKLMT= 177774 ::STACK LIMIT REGISTER
PIRQ= 177772   ::PROGRAM INTERRUPT REQUEST REGISTER
DSWR= 177570   ::HARDWARE SWITCH REGISTER
DDISP= 177570  ::HARDWARE DISPLAY REGISTER

.*GENERAL PURPOSE REGISTER DEFINITIONS
R0= %0         ::GENERAL REGISTER
R1= %1         ::GENERAL REGISTER
R2= %2         ::GENERAL REGISTER
R3= %3         ::GENERAL REGISTER
R4= %4         ::GENERAL REGISTER
R5= %5         ::GENERAL REGISTER
R6= %6         ::GENERAL REGISTER
R7= %7         ::GENERAL REGISTER
SP= %6         ::STACK POINTER
PC= %7         ::PROGRAM COUNTER

.*PRIORITY LEVEL DEFINITIONS
PR0= 0         ::PRIORITY LEVEL 0
PR1= 40        ::PRIORITY LEVEL 1
PR2= 100       ::PRIORITY LEVEL 2
PR3= 140       ::PRIORITY LEVEL 3
PR4= 200       ::PRIORITY LEVEL 4
PR5= 240       ::PRIORITY LEVEL 5
PR6= 300       ::PRIORITY LEVEL 6
PR7= 340       ::PRIORITY LEVEL 7

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: * 'SWITCH REGISTER' SWITCH DEFINITIONS
100000 SW15= 100000
040000 SW14= 40000
020000 SW13= 20000
010000 SW12= 10000
004000 SW11= 4000
002000 SW10= 2000
001000 SW09= 1000
000400 SW08= 400
000200 SW07= 200
000100 SW06= 100
000040 SW05= 40
000020 SW04= 20
000010 SW03= 10
000004 SW02= 4
000002 SW01= 2
000001 SW00= 1
001000 SW9=SW09
000400 SW8=SW08
000200 SW7=SW07
000100 SW6=SW06
000040 SW5=SW05
000020 SW4=SW04
000010 SW3=SW03
000004 SW2=SW02
000002 SW1=SW01
000001 SW0=SW00

: * DATA BIT DEFINITIONS (BIT00 TO BIT15)
100000 BIT15= 100000
040000 BIT14= 40000
020000 BIT13= 20000
010000 BIT12= 10000
004000 BIT11= 4000
002000 BIT10= 2000
001000 BIT09= 1000
000400 BIT08= 400
000200 BIT07= 200
000100 BIT06= 100
000040 BIT05= 40
000020 BIT04= 20
000010 BIT03= 10
000004 BIT02= 4
000002 BIT01= 2
000001 BIT00= 1
001000 BIT9=BIT09
000400 BIT8=BIT08
000200 BIT7=BIT07
000100 BIT6=BIT06
000040 BIT5=BIT05
000020 BIT4=BIT04
000010 BIT3=BIT03
000004 BIT2=BIT02
000002 BIT1=BIT01
000001 BIT0=BIT00

: * BASIC 'CPU' TRAP VECTOR ADDRESSES
000004 ERRVEC= 4 ;; TIME OUT AND OTHER ERRORS
000010 RESVEC= 10 ;; RESERVED AND ILLEGAL INSTRUCTIONS
```

```
000014 TBITVEC=14 ::'T' BIT
000014 TRTVEC= 14 ::TRACE TRAP
000014 BPTVEC= 14 ::BREAKPOINT TRAP (BPT)
000020 IOTVEC= 20 ::INPUT/OUTPUT TRAP (IOT) **SCOPE**
000024 PWRVEC= 24 ::POWER FAIL
000030 EMTVEC= 30 ::EMULATOR TRAP (EMT) **ERROR**
000034 TRAPVEC=34 ::'TRAP' TRAP
000060 TKVEC= 60 ::TTY KEYBOARD VECTOR
000064 TPVEC= 64 ::TTY PRINTER VECTOR
000240 PIRQVEC=240 ::PROGRAM INTERRUPT REQUEST VECTOR
808 .SBTTL MEMORY MANAGEMENT DEFINITIONS
      ;*KT11 VECTOR ADDRESS
000250 MMVEC= 250
      ;*KT11 STATUS REGISTER ADDRESSES
177572 SR0= 177572
177574 SR1= 177574
177576 SR2= 177576
172516 SR3= 172516
      ;*USER 'I' PAGE DESCRIPTOR REGISTERS
177600 UIPDR0= 177600
177602 UIPDR1= 177602
177604 UIPDR2= 177604
177606 UIPDR3= 177606
177610 UIPDR4= 177610
177612 UIPDR5= 177612
177614 UIPDR6= 177614
177616 UIPDR7= 177616
      ;*USER 'D' PAGE DESCRIPTOR REGISTORS
177620 UDPDR0= 177620
177622 UDPDR1= 177622
177624 UDPDR2= 177624
177626 UDPDR3= 177626
177630 UDPDR4= 177630
177632 UDPDR5= 177632
177634 UDPDR6= 177634
177636 UDPDR7= 177636
      ;*USER 'I' PAGE ADDRESS REGISTERS
177640 UIPAR0= 177640
177642 UIPAR1= 177642
177644 UIPAR2= 177644
177646 UIPAR3= 177646
177650 UIPAR4= 177650
177652 UIPAR5= 177652
177654 UIPAR6= 177654
177656 UIPAR7= 177656
      ;*USER 'D' PAGE ADDRESS REGISTERS
177660 UDPAR0= 177660
177662 UDPAR1= 177662
177664 UDPAR2= 177664
177666 UDPAR3= 177666
177670 UDPAR4= 177670
177672 UDPAR5= 177672
177674 UDPAR6= 177674
177676 UDPAR7= 177676
      ;*SUPERVISOR 'I' PAGE DESCRIPTOR REGISTERS
172200 SIPDR0= 172200
172202 SIPDR1= 172202
```

172204	SIPDR2= 172204
172206	SIPDR3= 172206
172210	SIPDR4= 172210
172212	SIPDR5= 172212
172214	SIPDR6= 172214
172216	SIPDR7= 172216
	:*SUPERVISOR 'D' PAGE DESCRIPTOR REGISTERS
172220	SDPDR0= 172220
172222	SDPDR1= 172222
172224	SDPDR2= 172224
172226	SDPDR3= 172226
172230	SDPDR4= 172230
172232	SDPDR5= 172232
172234	SDPDR6= 172234
172236	SDPDR7= 172236
	:*SUPERVISOR 'I' PAGE ADDRESS REGISTERS
172240	SIPAR0= 172240
172242	SIPAR1= 172242
172244	SIPAR2= 172244
172246	SIPAR3= 172246
172250	SIPAR4= 172250
172252	SIPAR5= 172252
172254	SIPAR6= 172254
172256	SIPAR7= 172256
	:*SUPERVISOR 'D' PAGE ADDRESS REGISTERS
172260	SDPAR0= 172260
172262	SDPAR1= 172262
172264	SDPAR2= 172264
172266	SDPAR3= 172266
172270	SDPAR4= 172270
172272	SDPAR5= 172272
172274	SDPAR6= 172274
172276	SDPAR7= 172276
	:*KERNEL 'I' PAGE DESCRIPTOR REGISTERS
172300	KIPDR0= 172300
172302	KIPDR1= 172302
172304	KIPDR2= 172304
172306	KIPDR3= 172306
172310	KIPDR4= 172310
172312	KIPDR5= 172312
172314	KIPDR6= 172314
172316	KIPDR7= 172316
	:*KERNEL 'D' PAGE DESCRIPTOR REGISTERS
172320	KDPDR0= 172320
172322	KDPDR1= 172322
172324	KDPDR2= 172324
172326	KDPDR3= 172326
172330	KDPDR4= 172330
172332	KDPDR5= 172332
172334	KDPDR6= 172334
172336	KDPDR7= 172336
	:*KERNEL 'I' PAGE ADDRESS REGISTERS
172340	KIPAR0= 172340
172342	KIPAR1= 172342
172344	KIPAR2= 172344
172346	KIPAR3= 172346
172350	KIPAR4= 172350

```
172352 KIPAR5= 172352
172354 KIPAR6= 172354
172356 KIPAR7= 172356
;*KERNEL 'D' PAGE ADDRESS REGISTERS
172360 KDPAR0= 172360
172362 KDPAR1= 172362
172364 KDPAR2= 172364
172366 KDPAR3= 172366
172370 KDPAR4= 172370
172372 KDPAR5= 172372
172374 KDPAR6= 172374
172376 KDPAR7= 172376
;*ADDITIONAL DEFINITIONS
;*
MMR0=SR0
MMR1=SR1
MMR2=SR2
MMR3=SR3
KSP=SP
SSP=SP
USP=SP
TBIT=BIT4
WBIT=BIT6
KERSTK=STACK
SUPSTK=STACK-200
USESTK=STACK-300
CPUERR=177766
RMIREG=177770

.SBTTL TRAP CATCHER
.=0
;*ALL UNUSED LOCATIONS FROM 4 - 776 CONTAIN A ".+2,HALT"
;*SEQUENCE TO CATCH ILLEGAL TRAPS AND INTERRUPTS
;*LOCATION 0 CONTAINS 0 TO CATCH IMPROPERLY LOADED VECTORS
.=174
DISPREG: .WORD 0 ;;SOFTWARE DISPLAY REGISTER
SWREG: .WORD 0 ;;SOFTWARE SWITCH REGISTER
.SBTTL STARTING ADDRESS(ES)
JMP @#START ;;JUMP TO STARTING ADDRESS OF PROGRAM
.SBTTL ACT11 HOOKS
;*****
;HOOKS REQUIRED BY ACT11
$SVPC=. ;SAVE PC
.=46
$ENDAD ;;1)SET LOC.46 TO ADDRESS OF $ENDAD IN .$EOP
.=52
.WORD 0 ;;2)SET LOC.52 TO ZERO
.= $SVPC ;;RESTORE PC

.SBTTL APT PARAMETER BLOCK
;*****
;SET LOCATIONS 24 AND 44 AS REQUIRED FOR APT
;*****
.$X=. ;;SAVE CURRENT LOCATION
.=24 ;;SET POWER FAIL TO POINT TO START OF PROGRAM
200 ;;FOR APT START UP
.=44 ;;POINT TO APT INDIRECT ADDRESS PNTR.
$APTHDR ;;POINT TO APT HEADER BLOCK
```

000204

.=.\$X ;;RESET LOCATION COUNTER

:SETUP APT PARAMETER BLOCK AS DEFINED IN THE APT-PDP11 DIAGNOSTIC
:INTERFACE SPEC.

000204
000204 000000
000206 001224
000210 000010
000212 000020
000214 000005
000216 000014

\$APTHD:
\$HIBTS: .WORD 0 ;;TWO HIGH BITS OF 18 BIT MAILBOX ADDR.
\$MBADR: .WORD \$MAIL ;;ADDRESS OF APT MAILBOX (BITS 0-15)
\$STSM: .WORD 10 ;;RUN TIM OF LONGEST TEST
\$PASTM: .WORD 20 ;;RUN TIME IN SECS. OF 1ST PASS ON 1 UNIT (QUICK VERIFY)
\$UNITM: .WORD 5 ;;ADDITIONAL RUN TIME (SECS) OF A PASS FOR EACH ADDITIONAL UNIT
.WORD \$ETEND-\$MAIL/2 ;;LENGTH MAILBOX-ETABLE (WORDS)

884

```

.SBTTL COMMON TAGS
:*****
:*THIS TABLE CONTAINS VARIOUS COMMON STORAGE LOCATIONS
:*USED IN THE PROGRAM.
.=1100

001100 001100 $CMTAG: .WORD 0 ;;START OF COMMON TAGS
001100 000000 $STNM: .BYTE 0 ;;CONTAINS THE TEST NUMBER
001102 000 $ERFLG: .BYTE 0 ;;CONTAINS ERROR FLAG
001103 000 $ICNT: .WORD 0 ;;CONTAINS SUBTEST ITERATION COUNT
001104 000000 $LPADR: .WORD 0 ;;CONTAINS SCOPE LOOP ADDRESS
001106 000000 $LPERR: .WORD 0 ;;CONTAINS SCOPE RETURN FOR ERRORS
001110 000000 $ERTTL: .WORD 0 ;;CONTAINS TOTAL ERRORS DETECTED
001112 000000 $ITEMB: .BYTE 0 ;;CONTAINS ITEM CONTROL BYTE
001114 000 $ERMAX: .BYTE 1 ;;CONTAINS MAX. ERRORS PER TEST
001115 001 $ERRPC: .WORD 0 ;;CONTAINS PC OF LAST ERROR INSTRUCTION
001116 000000 $GDADR: .WORD 0 ;;CONTAINS ADDRESS OF 'GOOD' DATA
001120 000000 $BDADR: .WORD 0 ;;CONTAINS ADDRESS OF 'BAD' DATA
001122 000000 $GDDAT: .WORD 0 ;;CONTAINS 'GOOD' DATA
001124 000000 $BDDAT: .WORD 0 ;;CONTAINS 'BAD' DATA
001126 000000 .WORD 0 ;;RESERVED--NOT TO BE USED
001130 000000 .WORD 0
001132 000000 $AUTOB: .BYTE 0 ;;AUTOMATIC MODE INDICATOR
001134 000 $INTAG: .BYTE 0 ;;INTERRUPT MODE INDICATOR
001135 000 .WORD 0
001136 000000 SWR: .WORD DSWR ;;ADDRESS OF SWITCH REGISTER
001140 177570 DISPLAY: .WORD DDISP ;;ADDRESS OF DISPLAY REGISTER
001142 177570 $TKS: 177560 ;;TTY KBD STATUS
001144 177560 $TKB: 177562 ;;TTY KBD BUFFER
001146 177562 $TPS: 177564 ;;TTY PRINTER STATUS REG. ADDRESS
001150 177564 $TPB: 177566 ;;TTY PRINTER BUFFER REG. ADDRESS
001152 177566 $NULL: .BYTE 0 ;;CONTAINS NULL CHARACTER FOR FILLS
001154 000 $FILLS: .BYTE 2 ;;CONTAINS # OF FILLER CHARACTERS REQUIRED
001155 002 $FILLC: .BYTE 12 ;;INSERT FILL CHARS. AFTER A 'LINE FEED'
001156 012 $TPFLG: .BYTE 0 ;;'TERMINAL AVAILABLE' FLAG (BIT<07>=0=YES)
001157 000 $REGAD: .WORD 0 ;;CONTAINS THE ADDRESS FROM
001160 000000 .REPT $CM3 ;;WHICH ($REGO) WAS OBTAINED
001162 000000 $REG0: .WORD 0 ;;CONTAINS (($REGAD)+0)
001164 000000 $REG1: .WORD 0 ;;CONTAINS (($REGAD)+2)
001166 000000 $REG2: .WORD 0 ;;CONTAINS (($REGAD)+4)
001170 000000 $REG3: .WORD 0 ;;CONTAINS (($REGAD)+6)
001172 000000 $REG4: .WORD 0 ;;CONTAINS (($REGAD)+10)
001174 000000 $REG5: .WORD 0 ;;CONTAINS (($REGAD)+12)
001176 000000 .REPT 6
001200 000000 $TMP0: .WORD 0 ;;USER DEFINED
001202 000000 $TMP1: .WORD 0 ;;USER DEFINED
001204 000000 $TMP2: .WORD 0 ;;USER DEFINED
001206 000000 $TMP3: .WORD 0 ;;USER DEFINED
001210 000000 $TMP4: .WORD 0 ;;USER DEFINED
001212 000000 $TMP5: .WORD 0 ;;USER DEFINED
001214 207 377 377 $ESCAPE: 0 ;;ESCAPE ON ERROR ADDRESS
001217 000 $BELL: .ASCIZ <207><377><377> ;;CODE FOR BELL
001220 077 $QUES: .ASCII /?/ ;;QUESTION MARK
001221 015 $CRLF: .ASCII <15> ;;CARRIAGE RETURN
001222 012 000 $LF: .ASCIZ <12> ;;LINE FEED

```

```
*****  
:SBTTL APT MAILBOX-ETABLE  
*****  
:EVEN  
001224 $MAIL: ::APT MAILBOX  
001224 000000 $MSGTY: .WORD AMSTGY ::MESSAGE TYPE CODE  
001226 000000 $FATAL: .WORD AFATAL ::FATAL ERROR NUMBER  
001230 000000 $TESTN: .WORD ATESTN ::TEST NUMBER  
001232 000000 $PASS: .WORD APASS ::PASS COUNT  
001234 000000 $DEVCT: .WORD ADEVCT ::DEVICE COUNT  
001236 000000 $UNIT: .WORD AUNIT ::I/O UNIT NUMBER  
001240 000000 $MSGAD: .WORD AMSGAD ::MESSAGE ADDRESS  
001242 000000 $MSGLG: .WORD AMGLG ::MESSAGE LENGTH  
001244 $ETABLE: ::APT ENVIRONMENT TABLE  
001244 000 $ENV: .BYTE AENV ::ENVIRONMENT BYTE  
001245 000 $ENVM: .BYTE AENVM ::ENVIRONMENT MODE BITS  
001246 000000 $SWREG: .WORD ASWREG ::APT SWITCH REGISTER  
001250 000000 $USWR: .WORD AUSWR ::USER SWITCHES  
001252 000000 $CPUOP: .WORD ACPUOP ::CPU TYPE, OPTIONS  
: *  
: * BIT 15-11=CPU TYPE  
: * 11/04=01,11/05=02,11/20=03,11/40=04,11/45=05  
: * 11/70=06,PDQ=07,Q=10  
: * BIT 10=REAL TIME CLOCK  
: * BIT 9=FLOATING POINT PROCESSOR  
: * BIT 8=MEMORY MANAGEMENT  
001254 $ETEND:  
:MEXIT  
001254 000000 TESTNO: .WORD 0 :HOLDS TEST NUMBER FOR TIMEOUTS  
001256 000000 WASR6: .WORD 0 :USED TO STORE THE STACK POINTER AFTER A TRAP  
001260 000000 TRAPP: .WORD 0 :USED TO STORE THE PC OF A TRAP OR ABORT  
001262 000000 TRAPPS: .WORD 0 :USED TO STORE THE PS OF A TRAP OR ABORT  
001264 000000 WASSR0: .WORD 0 :USED TO STORE CONTENTS OF SR0  
001266 000000 WASSR1: .WORD 0 :USED TO STORE CONTENTS OF SR1  
001270 000000 WASSR2: .WORD 0 :USED TO STORE CONTENTS OF SR2  
001272 000000 TBITPS: .WORD 0 :SAVES THE PSW THAT MAY HAVE ITS T-BIT ON  
001274 000000 TONUM: .WORD 0 :HOLDS NUMBER OF TIME-OUTS  
001276 000000 VIRT1: .WORD 0 :HOLDS VIRTUAL ADDRESS TO BE CONVERTED  
001300 000000 VIRT2: .WORD 0 :  
001302 000000 PBALO: .WORD 0 :HOLDS BITS <15:00> OF PHYSICAL ADDRESS  
001304 000000 PBAHI: .WORD 0 :HOLDS BITS <21:16> OF PHYSICAL ADDRESS  
001306 000000 DATAOR: .WORD 0 :HOLDS LOGICAL OR OF BAD DATA  
001310 000000 DATAND: .WORD 0 :HOLDS LOGICAL AND OF BAD DATA  
001312 000000 PATTOR: .WORD 0 :HOLDS LOGICAL OR OF PATTERN LOADED  
001314 000000 PATAND: .WORD 0 :HOLDS LOGICAL AND OF PATTERN LOADED  
001316 000000 ADDROR: .WORD 0 :HOLDS LOGICAL OR OF ADDRESS  
001320 000000 ADRAND: .WORD 0 :HOLDS LOGICAL AND OF ADDRESS  
001322 000000 ERRCNT: .WORD 0 :HOLDS NUMBER OF ERRORS ON TEST  
001324 000000 BADPC: .WORD 0 :HOLDS PC FROM ABORT OR TRAP  
001326 000000 OLDPC: .WORD 0 :HOLDS RETURN ADDRESS IN CASE OF LOOP ON ERROR  
001330 000000 OLDPS: .WORD 0 :HOLDS OLD PSW IN CASE OF LOOP ON ERROR  
001332 000000 PCPUER: .WORD 0 :HOLDS VALUE OF CPU ERROR REGISTER  
001334 000000 CPUEXP: .WORD 0 :HOLDS EXPECTED CPU ERROR CONDITION  
001336 000000 HOLFLG: .WORD 0 :HOLDS NUMBER OF TIMEOUTS FOR CARRY PROPAGATION TEST  
001340 000000 HDWFLAG: .WORD 0 :FLAGS APT SPECIAL HARDWARE FOR T47 & T50  
001342 020000 READON: .WORD 20000 :READ ONLY BIT IN MMIO  
001344 000200 $MXCNT: .WORD 200 :HOLD MAX. NUMBER OF LOOP ITERATIONS
```

```
001346 000000
001350   136   103
001353   012   000

001356

001356 172200
001360 172240
001362 172300
001364 172340
001366 177600
001370 177640
```

\$TBIT: .WORD 0 ;'T' BIT STATE INDICATOR
\$CNTLC: .ASCIZ /[^]C/<15><12> ;CONTROL [^]C
.EVEN
PARTAB: ;THIS IS THE TABLE OF THE FIRST PAR OR PDR
 ;OF EACH GROUP. THEY ARE USED FOR THE DUAL
 ;ADDRESSING TEST.
.WORD 172200 ;SIPDRO
.WORD 172240 ;SIPARO
.WORD 172300 ;KIPDRO
.WORD 172340 ;KIPARO
.WORD 177600 ;UIPDRO
.WORD 177640 ;UIPARO

.SBTTL ERROR POINTER TABLE
 ;*THIS TABLE CONTAINS THE INFORMATION FOR EACH ERROR THAT CAN OCCUR.
 ;*THE INFORMATION IS OBTAINED BY USING THE INDEX NUMBER FOUND IN
 ;*LOCATION \$ITEMB. THIS NUMBER INDICATES WHICH ITEM IN THE TABLE IS PERTINENT.
 ;*NOTE1: IF \$ITEMB IS 0 THE ONLY PERTINENT DATA IS (\$ERRPC).
 ;*NOTE2: EACH ITEM IN THE TABLE CONTAINS 4 POINTERS EXPLAINED AS FOLLOWS:
 ;* EM ;:POINTS TO THE ERROR MESSAGE
 ;* DH ;:POINTS TO THE DATA HEADER
 ;* DT ;:POINTS TO THE DATA
 ;* DF ;:POINTS TO THE DATA FORMAT

001372	\$ERRTB:	
885		
886		
887 001372	041304	EM1 ;UNEXPECTED CPU TRAP TO LOC. 004
888 001374	044647	DH1 ;OLD PC OLD PSW R6 WAS CPUERR TESTNO ERRORPC
889 001376	047606	DT1 ;TRAPPC,TRAPPS,WASR6,CPUERR,TESTNO,\$ERPPC, 0
890 001400	050360	DF1 ;0,0,0,0,0
891		
892		
893 001402	041344	EM2 ;UNEXPECTED MEM. MGMT. TRAP TO LOC. 250
894 001404	044727	DH2 ;OLD PC OLD PSW R6 WAS SRO SR1 SR2 TESTNO ERR
895 001406	047624	DT2 ;TRAPPC,TRAPPS,WASR6,WASSRO,WASSR1,WASSR2,TESTNO,\$ERRPC,0
896 001410	050365	DF2 ;0,0,0,0,0,0,0,0
897		
898		
899 001412	041413	EM3 ;PRIORITY BITS SET WRONG IN PSW
900 001414	045026	DH3 ;WROTE READ TESTNO ERRORPC
901 001416	047646	DT3 ;\$REG0,\$REG1,TESTNO,\$ERRPC,0
902 001420	050375	DF3 ;0,0,0,0
903		
904		
905 001422	041452	EM4 ;MODE BITS SET WRONG IN PSW
906 001424	045026	DH3 ;WROTE READ TESTNO ERRORPC
907 001426	047646	DT3 ;\$REG0,\$REG1,TESTNO,\$ERRPC,0
908 001430	050375	DF3 ;0,0,0,0
909		
910		
911 001432	041505	EM5 ;DUAL ADDRESSING BETWEEN HI&LO BYTES OF PSW
912 001434	045026	DH3 ;WROTE READ TESTNO ERRORPC
913 001436	047646	DT3 ;\$REG0,\$REG1,TESTNO,\$ERRPC,0
914 001440	050375	DF3 ;0,0,0,0
915		
916		
917 001442	041560	EM6 ;KERNEL R6 CHANGED BY WRITING SUPERVISOR/USER R6
918 001444	045026	DH3 ;WROTE READ TESTNO ERRORPC
919 001446	047646	DT3 ;\$REG0,\$REG1,TESTNO,\$ERRPC,0
920 001450	050375	DF3 ;0,0,0,0
921		
922		
923 001452	041643	EM7 ;A MEMORY MGMT. REG. TIMED OUT
924 001454	045066	DH7 ;ADDRESS TESTNO ERRORPC
925 001456	047660	DT7 ;\$REG0,TESTNO,\$ERRPC,0
926 001460	050401	DF7 ;0,0,0
927		
928		
929 001462	041701	EM10 ;SUMMARY OF MEM. MGMT. REG. TIMEOUTS
930 001464	045116	DH10 ;REGISTER-ADDRS NUM. OF

Line No.	Address	Offset	Register	Description
931				:AND-ED OR-ED TIMOUTS TESTNO ERRORPC
932	001466	047670	DT10	:ADRAND,ADDROR,TONUM,TESTNO,\$ERRPC,0
933	001470	050404	DF10	:0,0,1,0,0
934				
935				;*ITEM 11
936	001472	041745	EM11	:MEM. MGMT. REG. WOULD NOT CLEAR
937	001474	045216	DH11	:REGISTR READ READ-(BINARY)
938				:ADDRESS (OCTAL) 5432109876543210 TESTNO ERRORPC
939	001476	047704	DT11	:\$REG0,\$REG1,\$REG1,TESTNO,\$ERRPC,0
940	001500	050411	DF11	:0,0,2,0,0
941				
942				;*ITEM 12
943	001502	042005	EM12	:MEM. MGMT. REG. BITS NOT SET CORRECTLY
944	001504	045336	DH12	:REGISTR WROTE READ READ
945				:ADDRESS (OCTAL) (OCTAL) (BINARY) TESTNO ERRORPC
946	001506	047720	DT12	:\$REG0,\$REG1,\$REG2,\$REG2,TESTNO,\$ERRPC,0
947	001510	050416	DF12	:0,0,0,2,0,0
948				
949				;*ITEM 13
950	001512	042054	EM13	:SRO EFFECTED BY WRITE TO PSW
951	001514	045476	DH13	:READ TESTNO ERRORPC
952	001516	047660	DT7	:\$REG0,TESTNO,\$ERRPC,0
953	001520	050401	DF7	:0,0,0
954				
955				;*ITEM 14
956	001522	042111	EM14	:MMR1 DID NOT TRACK PROPERLY
957	001524	045526	DH14	:EXPECTD (MMR1) TESTNO ERRORPC
958	001526	047736	DT14	:\$REG3,\$REG1,TESTNO,\$ERRPC,0
959	001530	050375	DF3	:0,0,0,0
960				
961				;*ITEM 15
962	001532	042145	EM15	:MMR3 IS HOLDING THE WRONG DATA
963	001534	045566	DH15	:LOADED (MMR3) TESTNO ERRORPC
964	001536	047750	DT15	:\$REG2,\$REG1,TESTNO,\$ERRPC,0
965	001540	050375	DF3	:0,0,0,0
966				
967				;*ITEM 16
968	001542	042204	EM16	:DUAL ADDRESSING BETWEEN PAR-PDR GROUPS
969	001544	045626	DH16	:INDEX INDEX PAR-PDR
970				:EXPECTD RECEIVD ADDRREAD TESTNO ERRORPC
971	001546	047762	DT16	:\$REG0,\$REG1,\$REG2,TESTNO,\$ERRPC,0
972	001550	050360	DF1	:0,0,0,0,0
973				
974				;*ITEM 17
975	001552	042253	EM17	:PHYS. ADDR. FORMED READ WRONG IN MAINT. MODE
976	001554	045727	DH17	:VIR ADDR KIPAR4 GDDATA BADDATA TESTNO ERRORPC
977	001556	047776	DT17	:\$REG0,KIPAR4,\$REG1,\$REG2,TESTNO,\$ERRPC,0
978	001560	050365	DF2	:0,0,0,0,0,0
979				
980				;*ITEM 20
981	001562	042331	EM20	:PHYS. ADDR. FORMED READ WRONG IN RELOCATE MODE
982	001564	046010	DH20	:PHYSICL PAR 4 PAR 5
983				:ADDRESS VBA VBA PAR 4 PAR 5 PSW TESTNO ERR
984	001566	050014	DT20	:PBAL0,VIRT1,VIRT2,\$REG4,\$REG5,\$TMP0,TESTNO,\$ERRPC,0
985	001570	050432	DF20	:3,0,0,0,0,0,0,0
986				
987				;*ITEM 21

988	001572	042403	EM21	:SR2 NOT TRACKING CORRECTLY
989	001574	046136	DH21	:SR2 WAS EXPECTD TESTNO ERRORPC
990	001576	050036	DT21	:WASSR2,\$REG1,TESTNO,\$ERRPC,0
991	001600	050375	DF3	:0,0,0,0
992				
993			;*ITEM 22	
994	001602	042436	EM22	:WRONG PDR'S REFERENCED WHILE IN RELOCATE MODE
995	001604	046176	DH22	:PHYSICL PAR 4
996				:ADDRESS V.B.A. PAR 4 SRO WAS SR2 WAS PSW TESTNO ERRO
997	001606	050050	DT22	:PBALO,VIRT1,\$REG4,WASSRO,WASSR2,\$TMPO,TESTNO,\$ERRPC,0
998	001610	050432	DF20	:3,0,0,0,0,0,0,0
999				
1000			;*ITEM 23	
1001	001612	042514	EM23	:PAR OR PDR WAS CHANGED BY A RESET
1002	001614	045216	DH11	:REGISTR READ READ-(BINARY)
1003				:ADDRESS (OCTAL) 5432109876543210 TESTNO ERRORPC
1004	001616	047704	DT11	:\$REG0,\$REG1,\$REG1,TESTNO,\$ERRPC,0
1005	001620	050411	DF11	:0,0,2,0,0
1006				
1007			;*ITEM 24	
1008	001622	042552	EM24	:MAINT MODE (SRO<8>) NOT DISABLED BY A RESET
1009	001624	046314	DH24	:TESTNO ERRORPC
1010	001626	050072	DT24	:TESTNO,\$ERRPC,0
1011	001630	050442	DF24	:0,0
1012				
1013			;*ITEM 25	
1014	001632	042630	EM25	:DATA INCORRECT AFTER A MAINT. MODE WRITE
1015	001634	045026	DH3	:WROTE READ TESTNO ERRORPC
1016	001636	050100	DT25	:\$REG1,\$REG2,TESTNO,\$ERRPC,0
1017	001640	050375	DF3	:0,0,0,0
1018				
1019			;*ITEM 26	
1020	001642	042701	EM26	:SOURCE RELOCATED IN MAINT. MODE
1021	001644	044727	DH2	:OLD PC OLD PSW R6 WAS SRO SR2 TESTNO ERRORPC
1022	001646	047624	DT2	:TRAPPC,TRAPPS,WASR6,WASSRO,WASSR2,TESTNO,\$ERRPC,0
1023	001650	050365	DF2	:0,0,0,0,0,0,0
1024				
1025			;*ITEM 27	
1026	001652	042741	EM27	:SR2 DIDNOT LOCKUP CORRECT VIRTUAL ADDR.
1027	001654	046136	DH21	:SR2 WAS EXPECTD TESTNO ERRORPC
1028	001656	050112	DT27	:WASSR2,\$REG4,TESTNO,\$ERRPC,0
1029	001660	050375	DF3	:0,0,0,0
1030				
1031			;*ITEM 30	
1032	001662	043015	EM30	:FOLLOWING PAR/PDR WILL NOT ZERO
1033	001664	046334	DH30	:ADDRESS DATA TESTNO ERRORPC
1034	001666	050124	DT30	:\$REG0,\$REG2,TESTNO,\$ERRPC,0
1035	001670	050375	DF3	:0,0,0,0
1036				
1037			;*ITEM 31	
1038	001672	043055	EM31	:SUMMARY OF DUAL ADDRESSING ERRORS
1039	001674	046374	DH31	:ADDROR ADDRAND ADDROR ADDRAND
1040				:LOADED LOADED ENABLED ENABLED TESTNO #ERRORS
1041	001676	050136	DT31	:ADDROR,ADRAND,DATAOR,DATAAND,TESTNO,ERRCNT,0
1042	001700	050375	DF3	:0,0,0,0,0,1
1043				
1044			;*ITEM 32	

Address	Offset	Value	Register	Description
1102	002012	043621	EM43	:18-BIT MAPPING POSSIBLE HOLE AT TOP OF MEMORY :STARTADR TESTNO ERRORPC :\$TMP1,TESTNO,\$ERRPC,0 :4,0,0
1103	002014	047153	DH43	
1104	002016	050264	DT43	
1105	002020	050462	DF43	
1106				
1107			:*ITEM 44	
1108	002022	043677	EM44	:NO TRAP THRU ERRVEC, AT 18-BIT ADDR. 760000 :TESTNO ERRORPC :TESTNO,\$ERRPC,0 :0,0
1109	002024	046314	DH24	
1110	002026	050072	DT24	
1111	002030	050442	DF24	
1112				
1113			:*ITEM 45	
1114	002032	043752	EM45	:DIDN'T GET WRAP AROUND TO ADDRESS ZERO :DATA TESTNO ERRORPC :\$REG1,TESTNO,\$ERRPC,0 :0,0,0
1115	002034	047203	DH45	
1116	002036	050274	DT45	
1117	002040	050401	DF7	
1118				
1119			:*ITEM 46	
1120	002042	044021	EM46	:NO TRAP THRU ERRVEC, ON NON-EXISTANT ADDR. :NEADDR TESTNO ERRORPC :\$REG0,TESTNO,\$ERRPC,0 :0,0,0
1121	002044	047233	DH46	
1122	002046	047660	DT7	
1123	002050	050401	DF7	
1124				
1125			:*ITEM 47	
1126	002052	044074	EM47	:PREMATURE END OF MEMORY FOUND :KIPAR4 LASTBK TESTNO ERRORPC :KIPAR4,\$LSTBK,TESTNO,\$ERRPC,0 :0,0,0,0
1127	002054	047262	DH47	
1128	002056	050304	DT47	
1129	002060	050365	DF2	
1130				
1131			:*ITEM 50	
1132	002062	044132	EM50	:22-BIT MAPPING POSSIBLE HOLE IN MAIN MEMORY FROM :STARTBK FINISHBK TESTNO ERRORPC :\$TMP1,\$TMP2,TESTNO,\$ERRPC,0 :0,0,0,0
1133	002064	047010	DH41	
1134	002066	050236	DT41	
1135	002070	050365	DF2	
1136				
1137			:*ITEM 51	
1138	002072	044213	EM51	:BAD RELOCATION, CARRY PROPAGATION 22-BIT MAPPING :PATTERN DATA ADDRESS :LOADED FETCHED INTENDED TESTNO ERRORPC :\$REG2,\$REG3,\$REG0,TESTNO,\$ERRPC,0 :0,0,0,0,0
1139	002074	047051	DH42	
1140				
1141	002076	050250	DT42	
1142	002100	050365	DF2	
1143				
1144			:*ITEM 52	
1145	002102	044273	EM52	:22-BIT MAPPING POSSIBLE HOLE AT TOP OF MEMORY :STARTADR TESTNO ERRORPC :\$TMP1,TESTNO,\$ERRPC,0 :0,0,0
1146	002104	047153	DH43	
1147	002106	050264	DT43	
1148	002110	050365	DF2	
1149				
1150			:*ITEM 53	
1151	002112	044351	EM53	:DID NOT GET UNIBUS ADDRESS :PATTERN DATA ADDRESS :LOADED FETCHED INTENDED TESTNO ERRORPC :\$REG2,\$REG3,\$REG0,TESTNO,\$ERRPC,0 :0,0,0,0,0
1152	002114	047051	DH42	
1153				
1154	002116	050250	DT42	
1155	002120	050365	DF2	
1156				
1157			:*ITEM 54	
1158	002122	044404	EM54	:W-BIT DID NOT GET SET IN PDR

Line	Address	Code	Register	Description
1159	002124	047326	DH54	:PDR VIRTUAL
1160				:TESTED ADDRESS TESTNO ERRORPC
1161	002126	050316	DT54	:\$REG5,\$REG3,TESTNO,\$ERRPC,0
1162	002130	050375	DF3	:0,0,0,0
1163				
1164				:*ITEM 55
1165	002132	044441	EM55	:W-BIT SET IN MORE THAN ONE PDR
1166	002134	047406	DH55	:PDR IN PDR VIRTUAL
1167				:ERROR TESTED ADDRESS TESTNO ERRORPC
1168	002136	050330	DT55	:\$REG0,\$REG5,\$REG3,TESTNO,\$ERRPC,0
1169	002140	050360	DF1	:0,0,0,0,0
1170				
1171				:*ITEM 56
1172	002142	044500	EM56	:W-BIT NOT CLEARED BY WRITING TO PDR
1173	002144	047506	DH56	:PDR TESTNO ERRORPC
1174	002146	050344	DT56	:\$REG5,TESTNO,\$ERRPC,0
1175	002150	050401	DF7	:0,0,0
1176				
1177				:*ITEM 57
1178	002152	044544	EM57	:W-BIT GOT SET DURING ODD ADDR. ABORT
1179	002154	047536	DH57	:PDR WAS EXPECTD TESTNO ERRORPC
1180	002156	047750	DT15	:\$REG2,\$REG1,TESTNO,\$ERRPC,0
1181	002160	050375	DF3	:0,0,0,0
1182				
1183				:*ITEM 60
1184	002162	044611	EM60	:NO APT SPECIAL HARDWARE FOUND
1185	002164	047576	DH60	:ERRORPC
1186	002166	050354	DT60	:\$ERRPC,0
1187	002170	050360	DF1	:0

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002172 036727 175600 000020
 002200 001411
 002202 016746 175570
 002206 011667 177060
 002212 042716 000020
 002216 012746 002224
 002222 000006
 002224 000207
 002226 036727 177040 000020
 002234 001410
 002236 016746 177030
 002242 012767 000340 177022
 002250 012746 002256
 002254 000006
 002256 000207
 002260 010046
 002262 012700 000020
 002266 005025
 002270 077002
 002272 012600
 002274 000207

```

.SBTTL ***** SUBROUTINES UNIQUE TO THIS PROGRAM *****
.SBTTL TURN OFF T-BIT AND SAVE CURRENT PSW
:*****
:*
:* THIS SUBROUTINE IS USED TO TURN OFF THE TRACE TRAP BIT IN
:* THE PSW IF IT IS ON. THE PROCESSOR STATUS IS SAVED IN
:* 'TBITPS' SO THAT THE PSW CAN BE RESTORED TO ITS PREVIOUS
:* CONDITION WHEN CONDITIONS WARRANT T-BIT TRAPPING.
:*
:*****
TOFF: BIT PSW,#TBIT ;IS THE T-BIT SET IN THE PSW?
      BEQ 1$ ;EXIT IF NO
      MOV PSW,-(SP) ;PUSH PRESENT PSW ON THE STACK
      MOV (SP),TBITPS ;ALSO SAVE IT IN 'TBITPS' FOR
                        ;RESTORING LATER
      BIC #TBIT,(SP) ;CLEAR THE T-BIT (BIT 4) IN THE PSW
      MOV #1$,-(SP) ;PUSH PC OF 'RTS' ON STACK
      RTT ;'RETURN' TO 1$ WITH T-BIT OFF
1$: RTS PC ;RETURN TO PROGRAM

.SBTTL TURN ON T-BIT AND RESTORE PREVIOUS PSW
:*****
:*
:* THIS SUBROUTINE IS USED TO RESTORE THE PROCESSOR STATUS
:* TO ITS PREVIOUS CONDITION BY RESTORING THE 'T-BIT PSW'
:* SAVED BY THE 'TOFF' SUBROUTINE IN THE 'TBITPS' LOCATION.
:*
:*****
TON: BIT TBITPS,#TBIT ;WAS T-BIT ON IN THE PREVIOUS PSW?
      BEQ 1$ ;EXIT IF NO
      MOV TBITPS,-(SP) ;PUSH PREVIOUS PSW ON THE STACK
      MOV #340,TBITPS ;RESET THE 'TBITPS' LOCATION
      MOV #1$,-(SP) ;PUSH PC OF 'RTS' ON STACK
      RTT ;'RETURN' TO 1$ WITH T-BIT RESTORED
1$: RTS PC ;RETURN TO PROGRAM

.SBTTL CLEAR 16 PAR'S OR PDR'S STARTING FROM ADDRESS IN R5
:*****
:*
:* THIS ROUTINE CLEARS 16 CONSECUTIVE MEMORY MANAGEMENT
:* REGISTERS STARTING WITH THE REGISTER POINTED TO BY R5.
:* IT SAVES R0 ON THE STACK, AND LOADS A COUNT IN R0,
:* CLEARS THE PAR'S OR PDR'S, AND THEN RESTORES R0
:* BEFORE RETURNING.
:*
:* CALL: MOV #KIPAR0,R5 ;PUT ADDRESS OF FIRST KERNAL PAR INTO R5
:* JSR PC,CLRREG ;CLEAR ALL THE KERNAL PAR'S
:*****
CLRREG: MOV R0,-(KSP) ;SAVE R0 ON THE STACK
        MOV #20,R0 ;PUT COUNT IN R0
1$: CLR (R5)+ ;CLEAR PAR OR PDR POINTED TO BY R5
      SOB R0,1$ ;BRANCH BACK 15 DECIMAL TIMES
      MOV (KSP)+,R0 ;POP R0 FROM STACK
      RTS PC ;RETURN TO TEST
  
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1253 002276
1254 002276 005067 177004
1255 002302 005067 177010
1256 002306 005067 177000
1257 002312 012700 177777
1258 002316 010067 176766
1259 002322 010067 176772
1260 002326 010067 176762
1261 002332 000207
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1272 002334
1273 002334 012667 176766
1274 002340 050067 176752
1275 002344 030067 176750
1276 002350 050167 176732
1277 002354 030167 176730
1278 002360 105767 176517
1279 002364 001002
1280 002366 104034
1281 002370 000401
1282 002372 104035
1283 002374 000177 176726
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1295 002400
1296 002400 012667 176722
1297 002404 050067 176706
1298 002410 030067 176704
1299 002414 050167 176672
1300 002420 030167 176670
1301 002424 050267 176656
1302 002430 030267 176654

```
.SBTTL CLEANUP LOCATIONS THAT HOLD LOGICAL 'AND' AND 'OR'
:*****
:* THIS SUBROUTINE IS USED TO INITIALIZE ALL LOCATIONS THAT
:* HOLD THE 'LOGICAL AND' AND 'LOGICAL OR' OF THE DATA AND
:* ADDRESSES THAT FAILED DURING THE EXECUTION OF A TEST.
:*****
CLEANUP:
CLR DATAOR ;LOCATION OF LOGICAL OR OF BAD DATA
CLR ADDROR ;LOCATION OF LOGICAL OR OF ADDRESS
CLR PATTOR ;LOCATION OF LOGICAL OR OF PATTERN LOADED
MOV #-1,R0 ;LOAD -1 INTO R0 TO INITIALIZE
MOV R0,DATAND ;LOCATION OF LOGICAL AND OF BAD DATA
MOV R0,ADRAND ;LOCATION OF LOGICAL AND OF ADDRESS
MOV R0,PATAND ;LOCATION OF LOGICAL AND OF PATTERN LOADED
RTS PC ;RETURN TO TEST
```

```
.SBTTL DUAL ADDRESSING WHEN LOADING A PAR OR PDR
:*****
:* THIS SUBROUTINE WILL LOG AND REPORT ALL DUAL ADDRESSING ERRORS
:* FOUND IN BOTH PAR'S AND PDR'S. A 'LOGICAL OR' AND A 'LOGICAL
:* AND' OF THE WRITTEN ADDRESSES WILL BE MAINTAINED IN 'ADDROR',
:* AND 'ADRAND'. THE LOG ON THE ADDITIONAL OR FAILING ADDRESSES
:* WILL BE MAINTAINED IN 'DATAOR' AND 'DATAND'.
:*****
```

```
DUALADR:
MOV (KSP)+,OLDPC ;SAVE RETURN ADDRESS IN CASE OF LOOP
BIS R0,ADDROR ;LOGICAL OR OF WRITTEN ADDRESS
BIT R0,ADRAND ;LOGICAL AND OF WRITTEN ADDRESS
BIS R1,DATAOR ;LOGICAL OR OF DUALED DATA
BIT R1,DATAND ;LOGICAL AND OF DUALED DATA
TSTB $ERFLG ;SEE IF THIS IS FIRST ERROR
BNE 1$ ;BRANCH IF NOT FIRST ERROR
ERROR +34
BR 2$ ;BRANCH TO EXIT
1$: ERROR +35
2$: JMP @OLDPC ;RETURN TO TEST
```

```
.SBTTL COUNT PATTERN ERRORS IN PAR'S OR PDR'S
:*****
:* THIS SUBROUTINE IS USED TO LOG AND REPORT THE COUNT PATTERN
:* ERRORS OCCURRING WHEN TESTING THE PAR'S AND PDR'S. THE
:* 'LOGICAL OR' AND 'LOGICAL AND' OF VARIOUS DATA WILL BE
:* MAINTAINED A FOLLOWS:
:* 1. ADDRESSES OF FAILED REGISTERS IN 'ADDROR' AND 'ADRAND'
:* 2. DATA FETCHED FROM REGISTERS IN 'DATAOR' AND 'DATAND'
:* 3. PATTERN LOADED INTO REGISTERS IN 'PATTOR' AND 'PATAND'.
:*****
```

```
PARCOUNT:
MOV (KSP)+,OLDPC ;SAVE RETURN ADDRESS IN CASE OF LOOP
BIS R0,ADDROR ;LOGICAL OR OF FAILING ADDRESS
BIT R0,ADRAND ;LOGICAL AND OF FAILING ADDRESS
BIS R1,PATTOR ;LOGICAL OR OF PATTERN LOADED
BIT R1,PATAND ;LOGICAL AND OF PATTERN LOADED
BIS R2,DATAOR ;LOGICAL OR OF DATA FETCHED
BIT R2,DATAND ;LOGICAL AND OF DATA FETCHED
```

1303 002434 105767 176443
 1304 002440 001002
 1305 002442 104036
 1306 002444 000401
 1307 002446 104037
 1308 002450 000177 176652
 1309
 1310

TSTB \$ERFLG ;SEE IF THIS IS THE FIRST ERROR
 BNE 1\$;BRANCH IF NOT FIRST ERROR
 ERROR +36
 BR 2\$;BRANCH TO EXIT
 ERROR +37
 1\$:
 2\$: JMP @OLDPC ;RETURN TO TEST

;*CALL:
 ;* JSR PC,\$SIZE
 ;* RETURN
 ;*\$LSTAD WILL CONTAIN:
 ;* WITH KT11 OPTION -- LAST VIRTUAL ADDRESS OF THE LAST BANK
 ;* WITHOUT KT11 OPTION -- LAST ABSOLUTE ADDRESS OF AVAILABLE MEMORY
 ;*\$LSTBK WILL CONTAIN THE LAST BANK AS A SAF
 ;*BIT07 = 0 DON'T USE MEMORY MANAGEMENT
 ;* MUST BE SETUP BEFORE TH CALL
 ;*BIT15 = 0 DON'T HAVE MEMORY MANAGEMENT OPTION
 ;* DETERMINED BY ROUTINE
 ;*\$LSTAD WILL CONTAIN THE LAST AVAILABLE MEMORY LOCATION

002454 010046
 002456 010146
 002460 010246
 002462 010346
 002464 013746 000004
 002470 013746 000006
 002474 010600

\$SIZE: MOV R0,-(SP) ;:SAVE R0 ON THE STACK
 MOV R1,-(SP) ;:SAVE R1 ON THE STACK
 MOV R2,-(SP) ;:SAVE R2 ON THE STACK
 MOV R3,-(SP) ;:SAVE R3 ON THE STACK
 MOV @ERRVEC,-(SP) ;:SAVE PRESENT ERROR VECTOR PS & PC
 MOV @ERRVEC+2,-(SP)
 MOV SP,R0 ;:SAVE THE STACK POINTER

;;SET THE ERRVEC PS TO THE PRESENT PS
 TRAP ;:PUSH OLD PSW AND PC ON STACK
 MOV (SP)+,@ERRVEC+2 ;:SAVE THE PSW IN @ERRVEC+2
 MOV #3776,R1 ;:SETUP ADDRESS
 TSTB (PC)+ ;:USE MEMORY MANAGEMENT?
 \$KT11: .WORD 200 ;:SET TO USE MEMORY MANAGEMENT
 BPL \$SCORE ;:BR IF NO
 MOV #\$KTNEX,@ERRVEC ;:SET FOR TIMEOUT
 TST @RSR0 ;:KT11 ARE YOU THERE?
 BIS #100000,\$KT11 ;:YES--SET KT11 KEY
 MOV @MGMERR,@MMVEC ;:SET IN CASE OF ERROR
 MOV #340,@MMVEC+2
 CLR -(SP) ;:INITIALIZE FOR 'PAR' LOADING
 MOV #KIPAR0,R2 ;:ADDRESS OF FIRST 'PAR'
 MOV #^D8,R3 ;:LOAD EIGHT 'PAR.'S' AND EIGHT 'PDR.'S'
 1\$: MOV #77406,-40(R2) ;:PDR = 4K, UP, READ/WRITE
 MOV (SP),(R2)+ ;:LOAD 'PAR'
 ADD #200,(SP) ;:UPDATE FOR NEXT 'PAR'
 SOB R3,1\$;:LOOP UNTIL ALL EIGHT ARE LOADED
 MOV #177600,-(R2) ;:SETUP KIPAR7 FOR I/O
 CLR -(R2) ;:SETUP KIPAR6 FOR TESTING.
 MOV #2\$,@ERRVEC ;:CATCH TIMEOUT IF NO SR3
 MOV #20,@RSR3 ;:ENABLE 22 BIT MODE
 BR 3\$;:THIS PDP-11 HAS A SR3 REGISTER
 2\$: CMP (SP)+,(SP)+ ;:CLEAN OFF TE STAC--NO SR3
 3\$: INC @RSR0 ;:TURN ON MEMORY MANAGEMENT
 MOV #\$KTOUR,@ERRVEC ;:SET FOR TIME OUT
 4\$: TST @143776 ;:TRAP ON NON-EX-MEM
 ADD #40,(R2) ;:MAKE A 1K STEP
 CMP @KIPAR7,(R2) ;:LAST ONE?
 BHI 4\$;:NO--TRY IT

002476 104400
 002500 012637 000006
 002504 012701 003776
 002510 105727
 002512 000200
 002514 100070
 002516 012737 002670 000004
 002524 005737 177572
 002530 052767 100000 177754
 002536 012737 003122 000250
 002544 012737 000340 000252
 002552 005046
 002554 012702 172340
 002560 012703 000010
 002564 012762 077406 177740
 002572 011622
 002574 062716 000200
 002600 077307
 002602 012742 177600
 002606 005042
 002610 012737 002626 000004
 002616 012737 000020 172516
 002624 000401
 002626 022626
 002630 005237 177572
 002634 012737 002660 000004
 002642 005737 143776
 002646 062712 000040
 002652 023712 172356
 002656 101371

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002660 011202          $KTOUT: MOV    (R2),R2          ;;GET LAST BANK+1
002662 005037 177572          CLR    @#SR0          ;;TURN OFF MEMORY MANAGEMENT
002666 000421          BR     $SIZEX
002670 042767 100000 177614 $KTNEX: BIC    #100000,$KT11      ;;KT11 NON-EXISTENT
002676 012737 002726 000004 $SCORE: MOV    #SCOREOUT,@#ERRVEC ;;SET FOR TIMEOUT
002704 005002          CLR    R2          ;;SET UP BANK
002706 062701 004000          1$:  ADD    #4000,R1      ;;INCREMENT BY 1K
002712 062702 000040          ADD    #40,R2        ;;1K STEP
002716 005711          TST    (R1)         ;;TRAP ON TIME OUT
002720 022701 177776          CMP    #177776,R1   ;;LAST ONE
002724 001370          BNE    1$          ;;NO--TRY AGAIN
002726 162701 004000          $CROUT: SUB   #4000,R1
002732 162702 000040          $SIZEX: SUB   #40,R2      ;;DROP BACK
002736 012737 002754 000004      MOV    #2$,@#ERRVEC    ;;SET FOR TIMEOUT
002744 012701 020000          MOV    #20000,R1     ;;FIRST ADDRESS
002750 005721          1$:  TST    (R1)+      ;;TEST AND STEP TO NEXT ADDRESS
002752 000776          BR     1$          ;;TRY ANOTHER
002754 162701 000002          2$:  SUB    #2,R1      ;;DROP BACK
002760 010006          MOV    R0,SP         ;;RESTORE THE STACK
002762 012637 000006          MOV    (SP)+,@#ERRVEC+2 ;;RESTORE ERROR VECTOR
002766 012637 000004          MOV    (SP)+,@#ERRVEC
002772 010167 000022          MOV    R1,$LSTAD     ;;LAST ADDRESS
002776 010267 000020          MOV    R2,$LSTBK     ;;LAST BANK
003002 012603          MOV    (SP)+,R3      ;;RESTORE R3
003004 012602          MOV    (SP)+,R2      ;;RESTORE R2
003006 012601          MOV    (SP)+,R1      ;;RESTORE R1
003010 012600          MOV    (SP)+,R0      ;;RESTORE R0
003012 005067 174750          CLR    CPUERR        ;;CLEAR THE ERROR REGISTER
003016 000207          RTS    PC
003020 000000          $LSTAD: .WORD 0      ;;CONTAINS THE LAST ADDRESS
003022 000000          $LSTBK: .WORD 0      ;;CONTAINS THE LAST BANK

1311
1312          .SBTTI ***** TRAP HANDLING ROUTINES *****
1313
1314          .SBTTL CPU TRAP HANDLER ROUTINE
1315          ;*****
1316          ;*
1317          ;* THIS SUBROUTINE WILL HANDLE ALL CPU TRAPS AND ABORTS THRU
1318          ;* 'ERRVEC' (LOC. 004). IF THIS SUBROUTINE IS ENTERED BY A
1319          ;* SECOND TRAP BEFORE THE FIRST HAS BEEN SERVICED, A HALT IS
1320          ;* EXECUTED.
1321          ;*
1322          ;*****
1323 003024 005227          TIMERR: INC    (PC)+      ;MAKE FLAG ZERO IF FIRST TIME THRU
1324 003026 177777          TIMFLG: .WORD -1      ;NEGATIVE ONE FOR 'HAVE ENTERED' FLAG
1325 003030 001401          BEQ    1$          ;BRANCH IF FIRST TIME IN
1326 003032 000000          HALT          ;STOP! - I'VE ENTERED THIS ROUTINE
1327          ;A SECOND TIME BEFORE I FINISHED
1328          ;REPORTING THE FIRST ERROR. THE
1329          ;SECOND ENTRY ADDRESS SHOULD BE ON
1330          ;THE KERNEL STACK.
1331 003034 012667 176220          1$:  MOV    (KSP)+,TRAPPC  ;SAVE PC+2 AT TIME OF ABORT
1332 003040 012667 176216          MOV    (KSP)+,TRAPPS  ;SAVE PS AT TIME OF ABORT
1333 003044 016767 174716 176260          MOV    CPUERR,PCPUER ;SAVE CPU ERROR REGISTER
1334 003052 010667 176200          MOV    KSP,WASR6     ;SAVE STACK POINTER VALUE
1335 003056 005767 176252          TST    CPUEXP        ;SEE IF ANY ERROR CONDITION WAS EXPECTED
1336 003062 001404          BEQ    2$          ;BRANCH IF NO TRAP EXPECTED
    
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1337 003064 026767 176242 176242      CMP      PCPUER, CPUEXP      ;SEE IF EXPECTED CONDITION OCCURED
1338 003072 001401                    BEQ      3$                  ;BRANCH IF ERROR CODES MATCH
1339 003074 104001                    2$:     ERROR      +1        ;UNEXPECTED TRAP OR ABORT TO LOC. 4
1340 003076 005067 174664            3$:     CLR      CPUERR      ;CLEAR CPU ERROR REGISTER
1341 003102 012767 177777 177716      MOV      #-1, TIMFLG       ;MAKE FLAG NEGATIVE ONE FOR NEXT TIME
1342 003110 016746 176146            MOV      TRAPPS, -(KSP)    ;PUT PC & PS OF TRAP ON STACK
1343 003114 016746 176140            MOV      TRAPPC, -(KSP)
1344 003120 000006                    RTT                          ;RETURN FROM INTERRUPT OR ABORT
1345
1346
1347      .SBTTL MEMORY MANAGEMENT TRAP HANDLER ROUTINE
1348      :*****
1349      :*
1350      :* THIS SUBROUTINE WILL HANDLE ALL UNEXPECTED MEMORY MANAGEMENT
1351      :* TRAPS AND ABORTS THRU 'MMVEC' (LOC. 250). IF THIS SUBROUTINE IS
1352      :* ENTERED BY A SECOND TRAP BEFORE THE FIRST HAS BEEN SERVICED, A
1353      :* HALT IS EXECUTED.
1354      :*
1355      :*****
1356 003122 005227      MGMERR: INC      (PC)+      ;MAKE FLAG ZERO IF FIRST TIME THRU
1357 003124 177777      MGMFLG: .WORD   -1        ;NEGATIVE ONE FOR 'HAVE ENTERED' FLAG
1358 003126 001401                    BEQ      1$                  ;BRANCH IF FIRST TIME IN
1359 003130 000000                    HALT                          ;STOP! - I'VE ENTERED THIS ROUTINE
1360      :* A SECOND TIME BEFORE I FINISHED
1361      :* REPORTING THE FIRST ERROR. THE
1362      :* SECOND ENTRY ADDRESS SHOULD BE ON
1363      :* THE KERNEL STACK.
1364 003132 012667 176122            1$:     MOV      (KSP)+, TRAPPC ;SAVE PC+2 AT TIME OF ABORT
1365 003136 012667 176120            MOV      (KSP)+, TRAPPS    ;SAVE PS AT TIME OF ABORT
1366 003142 010667 176110            MOV      KSP, WASR6        ;SAVE STACK POINTER VALUE
1367 003146 016767 174420 176110      MOV      SR0, WASSR0       ;SAVE CONTENTS OF KT STATUS REG. 0
1368 003154 016767 174414 176104      MOV      SR1, WASSR1       ;SAVE CONTENTS OF KT STATUS REG. 1
1369 003162 016767 174410 176100      MOV      SR2, WASSR2       ;SAVE CONTENTS OF KT STATUS REG. 2
1370 003170 042767 160000 174374      BIC      #160000, SR0      ;CLEAR ERROR BITS IN STATUS REG 0
1371 003176 104002                    ERROR      +2                ;UNEXPECTED TRAP OR ABORT TO LOC. 250
1372 003200 012767 177777 177716      MOV      #-1, MGMFLG      ;MAKE FLAG NEGATIVE ONE FOR NEXT TIME
1373 003206 016746 176050            MOV      TRAPPS, -(KSP)    ;PUT PC & PS OF TRAP ON STACK
1374 003212 016746 176042            MOV      TRAPPC, -(KSP)
1375 003216 000006                    RTT                          ;RETURN FROM INTERRUPT OR ABORT.
1376
1377      .SBTTL CONVERT VIRTUAL ADDRESS TO PHYSICAL ADDRESS
1378      :*****
1379      :*
1380      :* THIS SUBROUTINE IS USED TO FORM AN 22-BIT PHYSICAL ADDRESS
1381      :* (PBA) FROM THE 16-BIT VIRTUAL ADDRESS (VBA) AND THE APPROPRIATE
1382      :* PAGE ADDRESS REGISTER (PAR). THE SAME METHOD USED BY THE MEMORY
1383      :* MANAGEMENT LOGIC IS USED. VBA <15:13> SELECTS WHICH PAR/PDR
1384      :* IS TO BE USED, VBA <5:0>+PBA <5:0>, AND VBA <12:6> IS ADDED
1385      :* TO PAR <15:00> TO GIVE PBA <21:6>. BITS <21:16> OF THE
1386      :* PHYSICAL ADDRESS ARE LEFT IN LOC. 'PBAHI' AND BITS <15:00>
1387      :* ARE LEFT IN LOC. 'PBALO'. THE PSW'S 'CURRENT MODE' BITS
1388      :* ARE USED TO SELECT THE KERNEL, SUPERVISOR OR USER PAR/PDR'S.
1389      :* THE ROUTINE IS ENTERED WITH LOC. 'VIRT1' CONTAINING THE 16-BIT
1390      :* VIRTUAL ADDRESS.
1391      :*
1392      :*****
1393

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1394 003220 012702 172340 FORMPA: MOV #KIPAR0,R2 ;LOAD ADDRESS OF FIRST KERNEL PAR IN R2
1395 003224 032767 140000 174544 BIT #140000,PSW ;IN USER MODE?
1396 003232 001403 BEQ 1$ ;BRANCH IF NO
1397 003234 012702 177640 MOV #UIPAR0,R2 ;LOAD ADDRESS OF FIRST USER PAR IN R2
1398 003240 000406 BR 2$ ;BRANCH WHEN DONE
1399 003242 032767 040000 174526 1$: BIT #40000,PSW ;IN SUPERVISOR MODE?
1400 003250 001402 BEQ 2$ ;BRANCH IF NO
1401 003252 012702 172240 MOV #SIPAR0,R2 ;LOAD ADDRESS OF FIRST SUPERVISOR PAR IN R2
1402 003256 016700 176014 2$: MOV VIRT1,R0 ;LOAD VIRTUAL ADDR. (VBA) INTO R0
1403 003262 072027 177764 ASH #-14,R0 ;GET BITS <15:13> DOWN TO BITS <3:1>
1404 003266 042700 177761 BIC #177761,R0 ;MASK OF ALL BITS BUT BITS <3:1>
1405 003272 060002 ADD R0,R2 ;ADD OFFSET TO BASE PAR ADDRESS
1406 003274 011200 MOV (R2),R0 ;GET BITS <15:00> FROM APPROPRIATE PAR
1407 003276 010002 MOV R0,R2 ;COPY PAR BITS <15:00> INTO R2
1408 003300 016767 175772 175774 MOV VIRT1,PBALO ;PUT VIRTUAL ADDR. IN LOC. 'PBALO'
1409 003306 042767 160000 175766 BIC #160000,PBALO ;CLEAR OFF BITS <15:13> OF ORIGINAL VBA
1410 003314 072227 177766 ASH #-12,R2 ;GET PAR <15:00> DOWN TO BITS <1:0> OF R2
1411 003320 042702 177774 BIC #177774,R2 ;CLEAR OFF ALL BITS BUT BITS <1:0>
1412 003324 072027 000006 ASH #6,R0 ;SHIFT PAR<9:0> TO <15:6> OF R0
1413 003330 042700 000077 BIC #77,R0 ;CLEAR BITS <5:0> OF R0
1414 003334 060067 175742 ADD R0,PBALO ;IN EFFECT, ADD VBA<12:0> TO PAR<9:0>
1415 ;(PAR<9:0> IN BITS <15:6> OF R0)
1416 003340 005502 ADC R2 ;ADD ANY CARRY TO R2
1417 003342 010267 175736 MOV R2,PBAHI ;PUT BITS <21:16> OF PHYSICAL ADDR. IN PBAHI
1418 003346 000207 RTS PC ;RETURN TO PROGRAM
    
```



```

020322 001403          BEQ    70$      ::YES,USE NON-APT SWITCH
020324 012767 001246 160606  MOV    $$SWREG,SWR  ::NO,USE APT SWITCH REGISTER
020332
1425 70$:
.SBTTL TYPE PROGRAM NAME
::TYPE THE NAME OF THE PROGRAM IF FIRST PASS
020332 005227 177777      INC    #-1          ::FIRST TIME?
020336 001047          BNE    71$          ::BRANCH IF NO
020340 022737 035116 000042  CMP    $SENDAD,@#42  ::ACT-11?
020346 001443          BEQ    71$          ::BRANCH IF YES
020350 104401 020416      TYPE    ,72$        ::TYPE ASCIZ STRING
.SBTTL GET VALUE FOR SOFTWARE SWITCH REGISTER
020354 005737 000042      TST    @#42         ::ARE WE RUNNING UNDER XXDP/ACT?
020360 001012          BNE    73$          ::BRANCH IF YES
020362 126727 160656 000001  CMPB   $ENV,#1      ::ARE WE RUNNING UNDER APT?
020370 001406          BEQ    73$          ::BRANCH IF YES
020372 026727 160542 000176  CMP    SWR,$SWREG   ::SOFTWARE SWITCH REG SELECTED?
020400 001005          BNE    74$          ::BRANCH IF NO
020402 104407          GTSWR                ::GET SOFT-SWR SETTINGS
020404 000403          BR     74$
020406 112767 000001 160520 73$:  MOVB   #1,$AUTOB   ::SET AUTO-MODE INDICATOR
020414          74$:
020414 000420          BR     71$          ::GET OVER THE ASCIZ
020456          ::72$: .ASCIZ <CRLF>#CKKTA0 11/44 MEM MGMT PRT A#<CRLF>
          71$:
1426
1427 020456          LOOP:
1428 020456 012706 001100      MOV    #STACK,KSP   ::INITIALIZE THE STACK POINTER
1429 020462 012767 003024 157314  MOV    #TIMERR,ERRVEC  ::LOAD CPU SERVICE ROUTINE INTO TRAP VECTOR
1430 020470 012767 000340 157310  MOV    #340,ERRVEC+2  ::SET NEW PS TO PRIORITY LEVEL 7-KERNEL
1431 020476 012767 003122 157544  MOV    #MGMERR,MMVEC  ::LOAD MEMORY MANAGENT ROUTINE INTO VECTOR
1432 020504 012767 000340 157540  MOV    #340,MMVEC+2   ::SET NEW PS TO PRIORITY LEVEL 7-KERNEL
1433 020512 012700 177777      MOV    #-1,R0        ::PUT -1 INTO R0 TO INITIALIZE FLAGS
1434 020516 010067 162304      MOV    R0,TIMFLG     ::INITIALIZE CPU ERROR FLAG
1435 020522 010067 162376      MOV    R0,MGMFLG     ::INITIALIZE MEMORY MANAGEMENT ERROR FLAG
1436 020526 012767 000340 160536  MOV    #340,TBITPS   ::INITIALIZE LOG THAT HOLDS T-BIT PSW

```

1438 020534 005067 157032
1439 020540 005067 151752

CLR MMRO
CLR MMR3

;BE SURE MEM. MGMT IS OFF TO START WITH
;MAKE SURE ALL MAPPING IS OFF

1441	020544	005067	157216	CLR	CPUERR	:MAKE SURE CPU ERROR REG. IS CLEAR
1442	020550	052767	000200 161734	BIS	#BIT7,\$KT11	:SET M.M. FLAG FOR SIZING ROUTINE
1443	020556	004767	161672	JSR	PC,\$SIZE	:RUN SIZING ROUTINE
1444	020562	005067	157200	CLR	CPUERR	:CLEAR CPU ERROR REG. AFTER SIZING
1445						

1509

```

*****
*TEST 3          BYTE ADDRESSING TEST FOR PSW
*
*          THIS TEST WRITES THE HIGH AND LOW BYTES OF THE PROCESSOR STATUS WORD
*          AND READS THEM BACK TO BE SURE THEY CAN BE WRITTEN INDEPENDENTLY.
*          THIS CHECKS THE PSW PORTION OF THE ADDRESS DETECTION LOGIC.
*
*****

```

```

1510 020730 000004
1510 020732 012767 020740 160150 1$:  SCOPE
1511 020740 005067 157032 2$:  MOV #2$, $LPERR ;SET LOOP ON ERROR POINTER TO 2$
1512 020744 012700 000360      CLR PSW ;CLEAR THE PSW
1513 020750 110067 157023      MOV #360, R0 ;PUT THE HIGH BYTE DATA INTO R0
1514 020754 016701 157016      MOVB R0, PSW+1 ;WRITE THE HIGH BYTE OF THE PSW
1515 020760 042701 007437      MOV PSW, R1 ;READ BACK THE ENTIRE PSW
1516 020764 000300      BIC #007437, R1 ;MASK OFF THE T & CC BITS
1517 020766 020001      SWAB R0 ;GET DATA WRITTEN IN HIGH BYTE OF R0
1518 020770 001403      CMP R0, R1 ;WAS THE PSW WRITTEN TO CORRECTLY
1519 020772 005067 157000      BEQ 3$ ;BRANCH IF YES
1520 020776 104005      CLR PSW ;CLEAR PSW FOR ERROR REPORT
1521      ERROR +5 ;LOW BYTE EFFECTED BY WRITE TO HIGH BYTE OF PSW
1522      ;FOR TIGHTER SCOPE LOOP
1523      ;REPLACE ERROR CALL WITH
1524 021000 012767 021006 160102 3$:  MOV #4$, $LPERR ;SET LOOP ON ERROR POINTER TO 4$
1525 021006 005067 156764 4$:  CLR PSW ;CLEAR THE PSW
1526 021012 012700 000340      MOV #340, R0 ;PUT THE LOW BYTE DATA INTO R0
1527 021016 110067 156754      MOVB R0, PSW ;WRITE THE LOW BYTE OF THE PSW
1528 021022 016701 156750      MOV PSW, R1 ;READ BACK THE ENTIRE PSW
1529 021026 042701 007437      BIC #007437, R1 ;MASK OFF THE T&CC BITS
1530 021032 020001      CMP R0, R1 ;WAS PSW WRITTEN TO CORRECTLY
1531 021034 001403      BEQ 5$ ;BRANCH IF YES
1532 021036 005067 156734      CLR PSW ;CLEAR PSW FOR ERROR REPORT
1533 021042 104005      ERROR +5 ;HIGH BYTE EFFECTED BY WRITE TO LOW BYTE OF PSW
1534      ;FOR TIGHTER SCOPE LOOP
1535      ;REPLACE ERROR CALL WITH
1536      ;'BR 2$' = 000760
1537 021044 012767 020732 160036 5$:  MOV #1$, $LPERR ;RESET LOOP ON ERROR POINTER TO 1$

```

1550

```

*****
*TEST 4          TEST AND SETUP OF STACK POINTERS
*
*   THIS TEST SETS THE USER AND KERNEL STACK POINTERS FOR THE
*   REST OF THE PROGRAM AND MAKES SURE THEY ARE INDEPENDENT OF
*   EACH OTHER.  KERNEL R6 IS SET TO 1100, SUPERVISOR R6 IS SET TO 700,
*   USER R6 IS SET TO 600, THEN KERNEL R6 IS READ TO BE SURE
*   IT'S STILL 1100.  THE SECOND PART OF THE TEST CHECKS TO SEE
*   THAT THE ILLEGAL MODE('10') STACK POINTER IS MAPPED TO THE
*   USER STACK POINTER, WITH MEMORY MANAGEMENT OFF.
*
*****

```

```

1551 021052 000004
1551 021054 005037 177572
1552 021060 005067 156712
1553 021064 012706 001100
1554 021070 012767 040000 156700
1555 021076 012706 000700
1556 021102 012767 140000 156666
1557 021110 012706 000600
1558 021114 005067 156656
1559 021120 022706 001100
1560 021124 000404
1561 021126 012700 001100
1562 021132 010601
1563 021134 104006
1564
1565
1566
1567 021136 012767 021136 157744 1$:
1568 021144 005067 156626
1569 021150 012746 177777
1570 021154 012767 040000 156614
1571 021162 012746 000001
1572 021166 012767 140000 156602
1573 021174 005046
1574 021176 012767 100000 156572
1575 021204 011600
1576 021206 001401
1577 021210 104040

```

```

TST4:  SCOPE
      CLR  @MMRO           ;MAKE SURE M.M. IS OFF
      CLR  PSW             ;GO TO KERNEL MODE
      MOV  #KERSTK,KSP     ;SET KERNEL STACK POINTER TO 1100
      MOV  #40000,PSW      ;GO TO SUPERVISOR MODE
      MOV  #SUPSTK,SSP     ;SET SUPERVISOR STACK POINTER TO 700
      MOV  #140000,PSW     ;GO TO USER MODE
      MOV  #USESTK,USP     ;SET USER STACK POINTER TO 600
      CLR  PSW             ;BACK TO KERNEL MODE
      CMP  #KERSTK,KSP     ;IS KERNEL R6 STILL 1100?
      BR   1$             ;BRANCH TO NEXT PART OF TEST
      MOV  #KERSTK,R0      ;SAVE DATA WRITTEN FOR ERROR REPORT
      MOV  KSP,R1          ;SAVE DATA READ AFTER USER R6 WAS WRITTEN
      ERROR +6            ;KERNEL R6 CHANGED BY WRITING USER R6
                          ;FOR TIGHTER SCOPE LOOP
                          ;REPLACE ERROR CALL WITH
                          ;000756
                          ;SET LOOP ON ERROR POINTER TO 1$
      MOV  #1$,$LPERR      ;SET LOOP ON ERROR POINTER TO 1$
      CLR  PSW             ;GO TO KERNAL MODE
      MOV  #-1,-(KSP)      ;PUSH A -1 ONTO STACK
      MOV  #40000,PSW      ;GO TO SUPERVISOR MODE
      MOV  #1,-(SSP)       ;PUSH A 1 ONTO THE STACK
      MOV  #140000,PSW     ;GO TO USER MODE
      CLR  -(USP)          ;PUSH A ZERO ONTO THE STACK
      MOV  #100000,PSW     ;PUT ILLEGAL MODE IN PSW
      MOV  (SP),R0         ;PUT TOP OF STACK INTO R0
      BEQ  TST5            ;WE'RE OK-GO TO NEXT TEST
      ERROR +40           ;ILLEGAL MODE NOT MAPPED TO USER MODE

```


1744	022570	005067	154776		CLR	SRO	:CLEAR STATUS REGISTER 0
1745	022574	012737	000340	177776	MOV	#340,@PSW	:SET PRIORITY 7 IN LOW BYTE OF PSW
1746	022602	016700	154764		MOV	SRO,R0	:READ STATUS REGISTER 0
1747	022606	001401			BEQ	2\$:BRANCH IF IT WAS STILL 0
1748	022610	104013			ERROR	+13	:SRO EFFECTED BY A WRITE TO THE PSW
1749							:FOR TIGHTER SCOPE LOOP
1750							:REPLACE ERROR CALL WITH
1751							: 'BR 1\$' = 000767
1752	022612	005067	154754	2\$:	CLR	SRO	:BE SURE SRO IS 0 BEFORE LEAVING
1753	022616	005067	155154		CLR	PSW	:BE SURE PSW IS 0 BEFORE LEAVING


```

025336 062700 000002      3$:  ADD    #2,R0      ;POINT TO NEXT REGISTER
025342 022700 172336      CMP    #KDPDR7,R0   ;SEE IF YOU PASSED THE KDPDR7 PDR
025346 103362                BHIS   2$           ;BRANCH IF MORE TEST
025350 022701 177777      CMP    #177777,R1   ;SEE IF COUNT HAS REACHED 177777
025354 001403                BEQ    4$           ;BRANCH IF SO
025356 062701 000401      ADD    #401,R1      ;INCREASE COUNT PATTERN
025362 000752                BR     1$           ;BRANCH TO CONTINUE TEST
025364 012767 025274 153516 4$:  MOV    #20$,$LPERR  ;SET LOOP POINTER TO START OF TEST
025372 005767 153724      TST   ERRCNT        ;SEE IF THERE WERE ANY ERRORS
025376 000404                BR     TST32        ;BRANCH TO NEXT TEST IF NO ERRORS
025400 016767 153716 153602  MOV    ERRCNT,$TMP5 ;SAVE # OF ERRORS FOR TYPEOUT
025406 104032                ERROR  +32          ;SUMMARY OF COUNT PATTERN FAILURES
  
```

1979

026444	012702	052014			MOV	#52014,R2	:LOAD EXPECTED DATA INTO R2
026450	112710	000124	12\$:		MOVB	#124,(R0)	:WRITE UPPER BYTE OF REGISTER
026454	016701	151120			MOV	UIPDR0,R1	:READ REGISTER INTO R1
026460	020102				CMP	R1,R2	:SEE IF ONLY UPPER BYTE WAS WRITTEN
026462	001401				BEQ	2\$:BRANCH TO EXIT IF CORRECT
026464	104033				ERROR	+33	:DIDN'T LOAD CORRECT BYTE
026466	012767	026372	152414	2\$:	MOV	#20\$,\$LPERR	:SET LOOP POINTER TO START OF TEST


```

2087 026644 077305                                SOB      R3,22$                ;LOOP UNTIL ALL SUPERVISOR PAR/PDR'S LOADED
2088 026646 012703 000020                        MOV      #20,R3              ;LOAD LOOP COUNTER WITH A 16
2089 026652 012701 177600                        MOV      #UIPDRO,R1         ;LOAD FIRST ADDRESS OF PDR INTO R1
2090 026656 012702 177640                        MOV      #UIPARO,R2         ;LOAD FIRST ADDRESS OF PAR INTO R2
2091 026662 012721 177777                        23$:   MOV      #-1,(R1)+     ;SET BITS IN PDR TO 1'S
2092 026666 012722 177777                        MOV      #-1,(R2)+         ;SET BITS IN PAR'S TO 1'S
2093 026672 077305                                SOB      R3,23$                ;LOOP UNTIL ALL USER PAR/PDR'S LOADED
2094 026674 000005                                RESET                                ;ISSUE AN "INIT" BY EXECUTING A RESET
2095 026676 012700 172300                        MOV      #KIPDRO,R0         ;LOAD ADDRESS OF FIRST KERNEL PDR IN R0

```

```
2097 026702 012704 000020          MOV      #20,R4           ;LOAD LOOP COUNTER WITH A 16
2098 026706 011001                 2$:      MOV      (R0),R1      ;READ A KERNEL PDR INTO R1
2099 026710 022701 177416          CMP      #177416,R1      ;ARE ALL THE BITS STILL SET?
2100 026714 001401                 BEQ      3$               ;BRANCH IF YES
2101 026716 104023                 ERROR   +23              ;KERNEL PDR AFFECTED BY A RESET
2102                                     ;FOR TIGHTER SCOPE LOOP
2103                                     ;REPLACE ERROR CALL WITH
2104                                     ;'BR 2$' = 000773
2105 026720 062700 000002          3$:      ADD      #2,R0           ;FORM ADDRESS OF NEXT KERNEL PDR
2106 026724 077410                 SOB      R4,2$           ;LOOP TO 2$ UNTIL ALL KERNEL PDR'S CHECKED
2107 026726 012700 172340          MOV      #KIPAR0,R0      ;LOAD ADDRESS OF FIRST KERNEL PAR IN R0
2108 026732 012704 000020          MOV      #20,R4           ;LOAD LOOP COUNTER WITH A 16
2109 026736 011001                 4$:      MOV      (R0),R1      ;READ A KERNEL PAR INTO R1
2110 026740 022701 177777          CMP      #177777,R1      ;ARE ALL THE BITS STILL SET?
2111 026744 001401                 BEQ      5$               ;BRANCH IF YES
2112 026746 104023                 ERROR   +23              ;KERNEL PAR AFFECTED BY A RESET
2113                                     ;FOR TIGHTER SCOPE LOOP
2114                                     ;REPLACE ERROR CALL WITH
2115                                     ;'BR 4$' = 000773
2116 026750 062700 000002          5$:      ADD      #2,R0           ;FORM ADDRESS OF NEXT KERNEL PAR
2117 026754 077410                 SOB      R4,4$           ;LOOP TO 4$ UNTIL ALL KERNEL PAR'S CHECKED
2118
2119 026756 012700 172200          MOV      #SIPDR0,R0      ;LOAD ADDRESS OF FIRST SUPERVISOR PDR IN R0
2120 026762 012704 000020          MOV      #20,R4           ;LOAD LOOP COUNTER WITH A 16
2121 026766 011001                 6$:      MOV      (R0),R1      ;READ A SUPERVISOR PDR INTO R1
2122 026770 022701 177416          CMP      #177416,R1      ;ARE ALL THE BITS STILL SET?
2123 026774 001401                 BEQ      7$               ;BRANCH IF YES
2124 026776 104023                 ERROR   +23              ;SUPERVISOR PDR AFFECTED BY A RESET
2125                                     ;FOR TIGHTER SCOPE LOOP
2126                                     ;REPLACE ERROR CALL WITH
2127                                     ;'BR 6$' = 000773
2128 027000 062700 000002          7$:      ADD      #2,R0           ;FORM ADDRESS OF NEXT SUPERVISOR PDR
2129 027004 077410                 SOB      R4,6$           ;LOOP TO 6$ UNTIL ALL SUPERVISOR PDR'S CHECKED
2130
2131 027006 012700 172240          MOV      #SIPAR0,R0      ;LOAD ADDRESS OF FIRST SUPERVISOR PAR IN R0
2132 027012 012704 000020          MOV      #20,R4           ;LOAD LOOP COUNTER WITH A 16
2133 027016 011001                 8$:      MOV      (R0),R1      ;READ A SUPERVISOR PAR INTO R1
2134 027020 022701 177777          CMP      #177777,R1      ;ARE ALL THE BITS STILL SET?
2135 027024 001401                 BEQ      9$               ;BRANCH IF YES
2136 027026 104023                 ERROR   +23              ;SUPERVISOR PAR AFFECTED BY A RESET
2137                                     ;FOR TIGHTER SCOPE LOOP
2138                                     ;REPLACE ERROR CALL WITH
2139                                     ;'BR 8$' = 000773
2140 027030 062700 000002          9$:      ADD      #2,R0           ;FORM ADDRESS OF NEXT SUPERVISOR PAR
2141 027034 077410                 SOB      R4,8$           ;LOOP TO 8$ UNTIL ALL SUPERVISOR PAR'S CHECKED
2142
2143 027036 012700 177600          MOV      #UIPDR0,R0      ;LOAD ADDRESS OF FIRST USER PDR WITH R0
2144 027042 012704 000020          MOV      #20,R4           ;LOAD LOOP COUNTER WITH A 16
2145 027046 011001                 10$:     MOV      (R0),R1      ;READ A USER PDR INTO R1
2146 027050 022701 177416          CMP      #177416,R1      ;ARE ALL THE BITS STILL SET?
2147 027054 001401                 BEQ     11$               ;BRANCH IF YES
2148 027056 104023                 ERROR   +23              ;USER PDR AFFECTED BY A RESET
2149                                     ;FOR TIGHTER SCOPE LOOP
2150                                     ;REPLACE ERROR CALL WITH
2151                                     ;'BR 10$' = 000773
2152 027060 062700 000002          11$:     ADD      #2,R0           ;FORM ADDRESS OF NEXT USER PDR
2153 027064 077410                 SOB     R4,10$           ;LOOP TO 10$ UNTIL ALL USER PDR'S CHECKED
```

```
2154  
2155 027066 012700 177640       MOV    #UIPAR0,R0    ;LOAD ADDRESS OF FIRST USER PAR IN R0  
2156 027072 012704 000020       MOV    #20,R4        ;LOAD LOOP COUNTER WITH A 16  
2157 027076 011001           12$:  MOV    (R0),R1      ;READ A USER PAR INTO R1  
2158 027100 022701 177777       CMP    #177777,R1    ;ARE ALL THE BITS STILL SET?  
2159 027104 001401           BEQ    13$           ;BRANCH IF YES  
2160 027106 104023           ERROR  +23          ;USER PAR AFFECTED BY A RESET  
2161                                   ;FOR TIGHTER SCOPE LOOP  
2162                                   ;REPLACE ERROR CALL WITH  
2163                                   ;'BR 12$' = 000773  
2164 027110 062700 000002       13$:  ADD    #2,R0        ;FORM ADDRESS OF NEXT USER PAR  
2165 027114 077410           SOB    R4,12$       ;LOOP TO 12$ UNTIL ALL USER PAR'S CHECKED  
2166  
2167
```

2181

```
*****
*TEST 44      INST. FETCH NOT RELOCATED IN MAINT. MODE
*
*   THIS TEST CHECKS TO SEE THAT WHEN MEMORY MANAGEMENT IS IN
*   MAINTENANCE MODE (DESTINATION-ONLY-RELOCATION), AN INSTRUCTION
*   FETCH IS NOT RELOCATED AND A RESET CLEARS THE MAINTENANCE BIT
*   (BIT 08) IN SRO.  IF THE 'FETCH' IS RELOCATED, A PG.LENGTH ABORT
*   SHOULD OCCUR, CAUSING A HALT SINCE TRAP CATCHER IS PLACED IN VECTOR 250
*
*   NOTE:  A HALT MAY OCCUR IF MAINT. MODE NOT DISABLED BY RESET
*
*****
```

```

027116 000004
2182 027120 004767 153046
2183 027124 012700 172300
2184 027130 012704 000010
2185 027134 005020
2186 027136 077402
2187 027140 012767 000252 151102
2188 027146 005067 151100
2189
2190
2191 027152 012767 001006 143120
2192 027160 012767 027166 151722
2193 027166 012767 000400 150376
2194 027174 000005
2195 027176 032767 000400 150366
2196 027204 001403
2197 027206 005067 150360
2198 027212 104024
2199
2200
2201
2202 027214 012706 001100
2203 027220 005067 150346
2204 027224 012767 003122 151016
2205 027232 012767 000340 151012
2206 027240 012767 027120 151642
2207 027246 004767 152754
2208
2222
```

```
TST44: SCOPE
1$: JSR PC,TOFF ;TURN T-BIT TRAPPING OFF FOR THIS TEST
   MOV #KIPDR0,R0 ;LOAD ADDRESS OF FIRST KERNEL PDR INTO R0
   MOV #10,R4 ;LOAD LOOP COUNTER WITH AN 8
2$: CLR (R0)+ ;CLEAR PDR - MAPPING PAGE NON-RES, 0 BLKS.
   SOB R4,2$ ;LOOP TO 2$ UNTIL ALL KERNEL PDR'S CLEARED
   MOV #MMVEC+2,MMVEC ;LOAD TRAP CATCHER INTO MEM MGMT. VECTOR
   CLR MMVEC+2 ;
   ;A HALT WILL OCCUR IF RESET FAILS
   ;TO DISABLE DEST.-ONLY RELOCATION
   MOV #1006,KIPDR0 ;MAP KERNEL PG 0 R/W, 3 BLOCKS LONG.
   MOV #3$,SLPERR ;SET LOOP ON ERROR POINTER TO 3$
3$: MOV #BIT8,SRO ;TURN ON DEST-ONLY-RELOCATION
   RESET ;SHOULD CLEAR MAINT. BIT - WILL ABORT IF RELOCATED
   BIT #BIT8,SRO ;WAS MAINT. BIT (BIT 8) OF SRO CLEARED?
   BEQ 4$ ;BRANCH IF YES
   CLR SRO ;CLEAR SRO SO ERROR CAN BE REPORTED
   ERROR +24 ;MAINT. MODE NOT DISABLED BY A RESET
   ;FOR A TIGHTER SCOPE LOOP
   ;REPLACE ERROR CALL WITH
   ;'BR 3$' = 000765
4$: MOV #KERSTK,KSP ;RESTORE STACK POINTER
   CLR SRO ;BE SURE SRO IS CLEAR
   MOV #MGMERR,MMVEC ;RESTORE MEM. MGMT. TRAP VECTOR
   MOV #340,MMVEC+2 ;RESTORE MEM. MGMT VECTOR+2
   MOV #1$,SLPERR ;RESET LOOP ON ERROR POINTER TO 1$
   JSR PC,TON ;TURN T-BIT TRAPPING BACK ON
```

```

027252 000004
2223 027254 004767 152712
```

```
*****
*TEST 45      TEST THAT SOURCE NOT RELOCATED IN MAINT. MODE
*
*   THIS TEST CHECKS TO SEE THAT WHEN MEMORY MANAGEMENT IS IN
*   MAINTENANCE MODE, THE SOURCE IS NOT RELOCATED; ONLY THE
*   DESTINATION IS RELOCATED.  KERNEL PAR'S 3 & 4 ARE MAPPED TO
*   PHYSICAL ADDRESS 60000-77776.  PDR4 IS SET TO ALLOW FULL
*   READ/WRITE BUT PDR3 IS CLEAR ALLOWING NO ACCESS.  VIRTUAL
*   ADDRESSES REFERENCING PAR/PDR'S 4 & 3 ARE USED AS
*   DESTINATION AND SOURCE RESPECTIVELY.  IF THE SOURCE IS
*   RELOCATED IN MAINTENANCE MODE A MEM. MGMT. TRAP WILL OCCUR
*   AND THE ERROR WILL BE REPORTED.  KERNEL PG. 7 IS MAPPED R/W.
*
*****
TST45: SCOPE
1$: JSR PC,TOFF ;TURN OFF T-BIT TRAPPING FOR THIS TEST
```



```

031204 104017      ERROR      +17      ;RELOCATION FAILED
2327 031206 016737 147764 142000 30$:  MOV      $TMP0,@#142000 ;RESTORE ORIGINAL DATA TO TEST LOCATION
031214 012767 031246 147666      MOV      #31$, $LPERR   ;SET LOOP ON ERROR POINTER TO 31$
031222 013767 140000 147746      MOV      @#140000,$TMP0 ;SAVE DATA AT TEST LOCATION
031230 012737 001377 172350      MOV      #1377,@#KIPAR4 ;LOAD PAR4 WITH 1377
031236 012700 100100      MOV      #100100,R0     ;PUT VIRTUAL ADDRESS IN R0
031242 012701 125216      MOV      #125216,R1     ;PUT DATA PATTERN INTO R1
031246 052737 000400 177572 31$:  BIS      #BIT8,@#MMRO   ;TURN ON DESTINATION ONLY RELOCATION
031254 010110      MOV      R1,(R0)       ;TRY TO LOAD DATA PATTERN INTO 100100
031256 013702 140000      MOV      @#140000,R2   ;READ (140000) INTO R2
031262 000005      RESET                      ;CLEAR MMRO
031264 020102      CMP      R1,R2        ;SEE IF DATA MATCHES PATTERN
031266 001401      BEQ     32$           ;BRANCH IF DATA MATCHES
031270 104017      ERROR      +17      ;RELOCATION FAILED
2328 031272 016737 147700 140000 32$:  MOV      $TMP0,@#140000 ;RESTORE ORIGINAL DATA TO TEST LOCATION
031300 012767 031332 147602      MOV      #33$, $LPERR   ;SET LOOP ON ERROR POINTER TO 33$
031306 013767 140000 147662      MOV      @#140000,$TMP0 ;SAVE DATA AT TEST LOCATION
031314 012737 001370 172350      MOV      #1370,@#KIPAR4 ;LOAD PAR4 WITH 1370
031322 012700 101000      MOV      #101000,R0     ;PUT VIRTUAL ADDRESS IN R0
031326 012701 125217      MOV      #125217,R1     ;PUT DATA PATTERN INTO R1
031332 052737 000400 177572 33$:  BIS      #BIT8,@#MMRO   ;TURN ON DESTINATION ONLY RELOCATION
031340 010110      MOV      R1,(R0)       ;TRY TO LOAD DATA PATTERN INTO 101000
031342 013702 140000      MOV      @#140000,R2   ;READ (140000) INTO R2
031346 000005      RESET                      ;CLEAR MMRO
031350 020102      CMP      R1,R2        ;SEE IF DATA MATCHES PATTERN
031352 001401      BEQ     34$           ;BRANCH IF DATA MATCHES
031354 104017      ERROR      +17      ;RELOCATION FAILED
2329 031356 016737 147614 140000 34$:  MOV      $TMP0,@#140000 ;RESTORE ORIGINAL DATA TO TEST LOCATION
031364 012767 027572 147516      MOV      #40$, $LPERR   ;SET LOOP ON ERROR POINTER TO 40$

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:*****
;* THIS PIECE OF CODE CHECKS TO SEE IF THE PROGRAM IS RUNNING UNDER
;* APT, AND THEN LOOKS FOR THE APT SPECIAL ADDRESSING HARDWARE. IF
;* THE HARDWARE IS FOUND, THE NEXT TWO TESTS OPERATE AS IF THERE
;* WERE A FULL COMPLEMENT OF MEMORY ON THE SYSTEM.
:*****

```

```

APTTST: CLR      HDWFLAG      ;RESET THE HARDWARE PRESENT FLAG
        TSTB     $ENV        ;ARE WE UNDER APT?
2339   BNE      1$          ;BRANCH IF WE ARE
2340   JMP      TST47       ;ELSE GO TO TEST 47
2341   BIT      #BIT7,$USWR  ;IS THE HARDWARE SUPPOSED TO BE THERE?
2342   BNE      2$          ;BRANCH IF TRUE
2343   JMP      TST47       ;ELSE GO TO TEST 47
2344   MOV      #3$,ERRVEC   ;TRAPS TO 4 GO TO 3$
2345   TST      RMIREG       ;SPECIAL HARDWARE PRESENT?
2346   BR       4$          ;IF WE GOT HERE, THE HARDWARE IS THERE
2347   ERROR    +60         ;APT SPECIAL HARDWARE NOT FOUND
2348   JMP      TST47       ;GO TO TEST 47
2349   INC      HDWFLAG      ;SET SPECIAL HARDWARE PRESENT FLAG

```

```

:*****
;*TEST 47      18-BIT MAPPING CARRY PROPAGATION
:
;*      THIS TEST USES FULL 18-BIT RELOCATION TO CHECK THE CARRY
;*      PROPAGATION OF THE RELOCATION ADDER. SINCE THIS TEST SCANS
;*      MEMORY FROM 00100000 TO 00740000 ON 8K BOUNDARIES, IT WILL
;*      REPORT ANY HOLES THAT IT FINDS IN MEMORY UP TO THE LAST

```

```
:* BLOCK. THE INFORMATION GIVEN WILL BE THE ADDRESS WHERE
:* THE HOLE WAS DISCOVERED AND THE FIRST GOOD ADDRESS AFTER
:* THE HOLE.
```

```
:* NOTE - PART OF THIS TEST WILL NOT BE RUN IF THE SYSTEM
:* MEMORY SIZE IS LESS THAN 16K WORDS.
```

TST47: SCOPE

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031452 000004
2366
2367 031454 012700 100100          MOV    #100100,R0          ;LOAD VIRTUAL ADDR FOR PAR4 INTO R0
2368 031460 012737 000001 177572  MOV    #1,@#MMR0         ;TURN ON 18-BIT MAPPING
2369 031466 005767 147646          TST    HDWFLAG           ;SPECIAL HARDWARE?
2370 031472 001004          BNE    20$               ;BRANCH IF TRUE
2371 031474 026727 151322 001000  CMP    $LSTBK,#1000      ;IS THERE AT LEAST 16K ON THE SYSTEM?
2372 031502 002510          BLT    4$                ;BRANCH IF LESS THAN 16K TO 4$
2373 031504 005067 147626          CLR    HOLFLG           ;MAKE SURE HOLE FLAG STARTS AT ZERO
2374 031510 012767 032146 146266 20$:  MOV    #10$,ERRVEC       ;SET ERROR VECTOR POINTER TO 10$
2375 031516 012767 000777 140624  MOV    #777,KIPAR4       ;LOAD PAR4 WITH STARTING BASE
2376 031524 012767 001000 140620  MOV    #1000,KIPAR5      ;START ADDRESSING WITH 16K
2377 031532 012701 120000          MOV    #120000,R1        ;LOAD VIRTUAL ADDR FOR PAR5 INTO R1
2378 031536 012702 000375          MOV    #375,R2           ;LOAD DATA PATTERN INTO R2
2379 031542 012767 031550 147340  MOV    #1$, $LPERR        ;SET LOOP ON ERROR POINTER TO 1$
2380 031550 005067 147556          CLR    PCPUER           ;CLEAR CPU ERROR FLAG
2381 031554 005767 147560          TST    HDWFLAG           ;SPECIAL HARDWARE?
2382 031560 001404          BEQ    2$                ;BRANCH IF FALSE
2383 031562 026767 140564 151232  CMP    KIPAR5,$LSTBK     ;ARE WE OUT OF EXISTING MEMORY?
2384 031570 003023          BGT    21$               ;BRANCH IF TRUE
2385 031572 011167 147400          2$:  MOV    (R1), $TMP0       ;SAVE DATA AT TEST LOCATION
2386 031576 005767 147530          TST    PCPUER           ;SEE IF THERE WAS A CPU TRAP
2387 031602 001014          BNE    3$                ;BRANCH IF TRAP OCCURRED
2388 031604 005767 147526          TST    HOLFLG           ;SEE IF HOLE WAS FOUND IN MEMORY
2389 031610 001411          BEQ    3$                ;BRANCH IF NO HOLE WAS FOUND
2390 031612 016767 140534 147362  MOV    KIPAR5,$TMP2      ;SAVE PAR THAT POINTS TO END OF HOLE
2391 031620 012767 031504 147262  MOV    #20$, $LPERR      ;SET LOOP ON ERROR POINTER TO 20$
2392 031626 104041          ERROR +41                ;HOLE IN MEMORY FROM $TMP1 TO $TMP2
2393 031630 005067 147502          CLR    HOLFLG           ;CLEAR HOLE FLAG IN CASE THERE ARE MORE
2394 031634 010210          3$:  MOV    R2,(R0)           ;LOAD TEST PATTERN INTO TEST LOCATION
2395 031636 000405          BR     23$               ;BRANCH OVER NEXT INSTRUCTIONS
2396 031640 010204          21$: MOV    R2,R4             ;GET COPY OF DATA
2397 031642 052704 000400          BIS    #BIT8,R4         ;ADD SPECIAL HARDWARE ENABLE BIT
2398 031646 010467 146116          MOV    R4, RMIREG       ;PUT DATA IN SPECIAL HARDWARE
2399 031652 011103          23$: MOV    (R1),R3         ;READ TEST LOCATION VIA DIFFERENT VIRT. ADDR.
2400 031654 020203          CMP    R2,R3            ;SEE IF THE CORRECT LOCATION WAS REFERENCED
2401 031656 001401          BEQ    22$               ;BRANCH IF CORRECT DATA WAS OBTAINED
2402 031660 104042          ERROR +42                ;BAD RELOCATION
2403 031662 016711 147310          22$: MOV    $TMP0,(R1)      ;RESTORE ORIGINAL DATA TO TEST LOCATION
2404 031666 062767 000400 140454  ADD    #400,KIPAR4       ;CHANGE BASE ADDRESS
2405 031674 062767 000400 140450  ADD    #400,KIPAR5       ;CHANGE BASE ADDRESS
2406 031702 005302          DEC    R2               ;CHANGE DATA PATTERN
2407 031704 022767 007400 140440  CMP    #7400,KIPAR5     ;SEE IF PAST LAST ADDRESS
2408 031712 103316          BHIS  1$                ;BRANCH IF NOT PAST LAST ADDRESS
2409 031714 005767 147416          TST    HOLFLG           ;SEE IF YOU ARE IN MIDDLE OF HOLE
2410 031720 001401          BEQ    4$                ;BRANCH IF NOT IN MIDDLE OF HOLE
2411 031722 104043          ERROR +43                ;IN MIDDLE OF HOLE IN MEMORY
2412          HOLFLG HAS NUMBER OF TIMEOUTS
2413          $TMP1 HAS PAR OF FIRST TIMEOUT

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2753
2754 033732 012667 145322      8$:  MOV      (KSP)+,TRAPPC  ;SAVE PC & PS OF TRAP
2755 033736 012667 145320      MOV      (KSP)+,TRAPPS
2756                                     ;PROGRAM WILL TRAP TO HERE IF TRY
2757                                     ;TO USE USER/SUPERVISOR PDR'S WHEN IN KERNEL MODE
2758                                     ;OR KERNEL PDR'S WHEN IN USER/SUPERVISOR MODE
2759 033742 010067 145330      MOV      R0,VIRT1      ;SAVE VIRTUAL ADDRESS FOR ERROR REPORT
2760 033746 004767 147246      JSR      PC,FORMPA     ;GO FORM THE PHYSICAL ADDRESS BEING USED
2761 033752 016767 143614 145304  MOV      SR0,WASSR0    ;SAVE SR0 & SR2 FOR ERROR REPORT
2762 033760 016767 143612 145302  MOV      SR2,WASSR2
2763 033766 042767 160000 143576  BIC      #160000,SR0   ;CLEAR ERROR BITS IN SR0
2764 033774 104022      ERROR +22             ;M.M. TRAP WHILE IN RELOCATE MODE -
2765                                     ;REFERENCED WRONG SET OF PDR'S
2766                                     ;FOR TIGHTER SCOPE LOOP
2767                                     ;REPLACE ERROR CALL WITH
2768                                     ;A 'NOP' = 000240
2769 033776 016746 145260      MOV      TRAPPS,-(KSP) ;PUT PC & PS OF TRAP ON STACK
2770 034002 016746 145252      MOV      TRAPPC,-(KSP)
2771 034006 000002      RTI                    ;RETURN TO TEST
  
```


034522	000422			BR	8\$:	SKIP CHECKING OTHER PDR'S-ERROR WILL SET W-BITS
034524	012702	000010		5\$:	MOV	#8,R2		:	SET LOOP COUNTER TO 8
034530	012700	177600			MOV	#UIPDRO,R0		:	LOAD ADDR. OF FIRST PDR TO BE CHECKED IN R0
034534	031027	000100		6\$:	BIT	(R0),#WBIT		:	DID W-BIT IN OTHER PDRS REMAIN CLEAR?
034540	001403				BEQ	7\$:	BRANCH IF YES
034542	020500				CMP	R5,R0		:	IF W-BIT SET, THEN WAS IT PDR UNDER TEST?
034544	001401				BEQ	7\$:	BRANCH IF YES
034546	104055				ERROR	+55		:	W-BIT GOT SET IN MORE THAN ONE PDR
								:	FOR TIGHTER SCOPE LOOP, REPLACE ERROR
								:	CALL WITH 'BR 3\$' = 000750
								:	POINT R0 TO NEXT PDR TO BE CHECKED
034550	062700	000002		7\$:	ADD	#2,R0		:	LOOP UNTIL ALL 8 CHECKED FOR CLEAR W-BIT
034554	077211				SOB	R2,6\$:	WRITE TO THE PDR TESTED TO CLEAR W-BIT
034556	010115				MOV	R1,(R5)		:	DID WRITING PDR CLEAR THE W-BIT?
034560	031527	000100			BIT	(R5),#WBIT		:	BRANCH IF YES
034564	001401				BEQ	8\$:	W-BIT DID NOT CLEAR BY WRITING THE PDR
034566	104056				ERROR	+56		:	FOR TIGHTER SCOPE LOOP, REPLACE ERROR CALL
								:	WITH 'BR 3\$' = 000740
								:	POINT R5 TO THE NEXT PDR TO BE TESTED
034570	062705	000002		8\$:	ADD	#2,R5		:	CHANGE VIRT. ADDR TO REF. NEXT PDR
034574	062703	020000			ADD	#20000,R3		:	LOOP BACK TO 3\$ UNTIL ALL 8 PDR'S TESTED
034600	077445				SOB	R4,3\$:	RESET LOOP ON ERROR POINTER TO 1\$
034602	012767	034414	144300		MOV	#1\$, \$LPERR		:	TURN T-BIT BACK ON FOR NEXT TEST
034610	004767	145412			JSR	PC,TON		:	BACK TO KERNEL MODE BEFORE LEAVING
2798	034614	005067	143156		CLR	PSW			

2810

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*****
*TEST 55      TEST 'W-BIT NOT SET' CASES
*
*      THIS TEST CHECKS TWO SPECIAL CASES WHERE THE W-BIT DOES
*      NOT GET SET ON A WRITE.  FIRST CASE IS THAT THE W-BIT
*      SHOULD NOT SET IN PAGE DESCRIPTOR REG. 7 WHEN WRITING TO
*      STATUS REG SRO (KERNEL PDR 7 IS USED).  SECOND CASE IS THAT
*      THE W-BIT IS NOT SET IF THE 'DATO' IS ABORTED DUE TO AN
*      ODD ADDRESS ERROR (KERNEL PDR3 & VIRTUAL ADDR 60001 ARE USED).
*
*****
  
```

```

034620 000004
2811
2812 034622 004767 145344      1$:  JSR      PC,TOFF      ;TURN OFF T-BIT TRAPPING FOR THIS TEST
2813 034626 012701 077406      MOV      #77406,R1      ;PUT 'W-BIT OFF' VALUE FOR PDR IN R1
2814 034632 012767 034632 144250 2$:  MOV      #2$,SLPERR     ;SET LOOP ON ERROR POINTER TO 2$
2815 034640 010167 135442      MOV      R1,KIPDR3      ;LOAD KERNEL PDR3 WITH 77406 TO CLEAR W-BIT
2816 034644 012767 034656 143132  MOV      #3$,ERRVEC     ;SET UP LOC. 4 TO 3$ FOR ODD ADDR. ABORT
2817 034652 005267 023123      INC      60001          ;CAUSE ODD ADDRESS ABORT THRU LOC. 4
2818 034656 012706 001100      3$:  MOV      #KERSTK,KSP  ;RESTORE THE STACK POINTER
2819 034662 016702 135420      MOV      KIPDR3,R2      ;READ KIPDR3 INTO R2
2820 034666 020102              CMP      R1,R2          ;WAS W-BIT LEFT CLEARED?
2821 034670 001401              BEQ      4$             ;BRANCH IF YES
2822 034672 104057              ERROR   +57            ;W-BIT GOT SET DURING AN ODD ADDR. ABORT
2823
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2826 034674 012767 003024 143102 4$:  MOV      #TIMERR,ERRVEC ;RESTORE NORMAL CPU TRAP ROUTINE TO LOC.4
2827 034702 012767 034622 144200  MOV      #1$,SLPERR     ;RESET LOOP ON ERROR POINTER TO 1$
2828 034710 004767 145312      JSR      PC,TON        ;TURN T-BIT TRAPPING BACK ON
  
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```
.SBTTL *****
.SBTTL END OF PASS ROUTINE
:*****
;*INCREMENT THE PASS NUMBER ($PASS)
;*TYPE 'END PASS #XXXXX TOTAL NUMBER OF ERRORS SINCE LAST REPORT YYYY'
;*WHERE XXXXX AND YYYY ARE DECIMAL NUMBERS
;*IF SW12=1 INHIBIT TRACE TRAP
;*IF THERES A MONITOR GO TO IT
;*IF THERE ISN'T JUMP TO LOOP
$EOP:
034714          SCOPE
034714 000004   CLR      $STNM      ;;ZERO THE TEST NUMBER
034716 005067 144160  CLR      $PASS      ;;INCREMENT THE PASS NUMBER
034722 005267 144304  INC      #100000,$PASS ;;DON'T ALLOW A NEG. NUMBER
034726 042767 100000 144276 BIC     (PC)+      ;;LOOP?
034734 005327        DEC      1
034736 000001  $EOPCT: .WORD  1
034740 003072  BGT     $DOAGN     ;;YES
034742 012737  MOV     (PC)+,@(PC)+ ;;RESTORE COUNTER
034744 000001  $ENDCT: .WORD  1
034746 034736  $EOPCT
034750 104401 034756  TYPE   ,65$       ;;TYPE ASCIZ STRING
034754 000407  BR     64$       ;;GET OVER THE ASCIZ
;65$: .ASCIZ <12><15>/END PASS #/
64$:
034774          MOV     $PASS,-(SP)   ;;SAVE $PASS FOR TYPEOUT
034774 016746 144232  ;;TYPE PASS NUMBER
035000 104405  TYPDS   ;;GO TYPE--DECIMAL ASCII WITH SIGN
035002 104401 035010  TYPE   ,67$       ;;TYPE ASCIZ STRING
035006 000421  BR     66$       ;;GET OVER THE ASCIZ
;67$: .ASCIZ / TOTAL ERRORS SINCE LAST REPORT /
66$:
035052          MOV     $ERTTL,-(SP) ;;SAVE $ERTTL FOR TYPEOUT
035052 016746 144034  ;;TOTAL NUMBER OF ERRORS
035056 104405  TYPDS   ;;GO TYPE--DECIMAL ASCII WITH SIGN
035060 104401 001221  TYPE   ,$CRLF     ;;TYPE CARRIAGE RETURN, LINE FEED
035064 005067 144022  CLR     $ERTTL     ;;CLEAR ERROR TOTAL
035070 013700 000042  $GET42: MOV    @#42,R0  ;;GET MONITOR ADDRESS
035074 001414  BEQ    $DOAGN     ;;BRANCH IF NO MONITOR
035076 005046  CLR    -(SP)      ;;INSURE THE 'T' BIT IS CLEAR
035100 012746 035106  MOV    # $CLR.T,-(SP) ;;SETUP FOR AN RTI OR RTT
035104 000426  BR     $RTRN      ;;GO DO AN RTI OR RTT TO LOAD THE PSW
;;WITH A CLEARED 'T' BIT
$CLR.T:
035106          MOV    @#42,R0  ;;INSURE R0 CONTAINS THE MONITORS
035106 013700 000042  BEQ    $DOAGN     ;;RETURN ADDRESS
035112 001405  BEQ    $DOAGN     ;;RETURN ADDRESS
035114 000005  RESET  ;;CLEAR THE WORLD
035116 004710  $ENDAD: JSR   PC,(R0) ;;GO TO MONITOR
035120 000240  NOP    ;;SAVE ROOM
035122 000240  NOP    ;;FOR
035124 000240  NOP    ;;ACT11
035126          $DOAGN: TRAP  ;;PUSH OLD PSW AND PC ON STACK
035126 104400  TRAP  ;;PUSH OLD PSW AND PC ON STACK
035130 042716 000020  BIC    #20,(SP)  ;;CLEAR THE 'T' BIT
035134 032777 010000 143776 BIT    #BIT12,@SWR ;;RUN WITH TRACE TRAP?
035142 001005  BNE    1$        ;;BR IF NO
035144 005167 144176  COM    $TBIT     ;;IS IT TIME FOR TRACE TRAP
```

2833

```

035150 100402           BMI 1$           ;;BR IF NO
035152 052716 000020   BIS #20,(SP)      ;;SET TRACE TRAP
035156 012746 035164   1$:  MOV #$LOOP,-(SP) ;;JUMP TO START OF TEST
035162 000002          SRTRN: RTI          ;;RETURN--THIS IS CHANGED TO
                              ;;AN 'RTT' IF 'RTT' IS A LEGAL
                              ;;INSTRUCTION

035164           $LOOP:           JMP @ (PC)+          ;;RETURN
035164 000137          $RTNAD: .WORD  LOOP
035166 020456          $ENULL: .BYTE  -1,-1,0      ;;NULL CHARACTER STRING
035170 377           .EVEN

```

SBTTL SCOPE HANDLER ROUTINE

*THIS ROUTINE CONTROLS THE LOOPING OF SUBTESTS. IT WILL INCREMENT
 *AND LOAD THE TEST NUMBER(\$STNM) INTO THE DISPLAY REG.(DISPLAY<7:0>)
 *AND LOAD THE ERROR FLAG (\$ERFLG) INTO DISPLAY<15:08>
 *THE SWITCH OPTIONS PROVIDED BY THIS ROUTINE ARE:
 *SW14=1 LOOP ON TEST
 *SW09=1 LOOP ON ERROR
 *SW08=1 LOOP ON TEST IN SWR<7:0>

*CALL SCOPE ;;SCOPE=IOT

```

035174           $SCOPE:           CKSWR           ;;TEST FOR CHANGE IN SOFT-SWR
035174 104410           1$:  BIT #BIT14,@SWR      ;;LOOP ON PRESENT TEST?
035176 032777 040000 143734 BNE $OVER         ;;YES IF SW14=1
035204 001062          ;;#####START OF CODE FOR THE XOR TESTER#####
035206 000416          $XTSTR: BR 6$           ;;IF RUNNING ON THE 'XOR' TESTER CHANGE
                              ;;THIS INSTRUCTION TO A 'NOP' (NOP=240)
035210 013746 000004          MOV @#ERRVEC,-(SP)   ;;SAVE THE CONTENTS OF THE ERROR VECTOR
035214 012737 035234 000004 MOV #5,@#ERRVEC      ;;SET FOR TIMEOUT
035222 005737 177060          TST @#177060       ;;TIME OUT ON XOR?
035226 012637 000004          MOV (SP)+,@#ERRVEC  ;;RESTORE THE ERROR VECTOR
035232 000431          BR $SVLAD        ;;GO TO THE NEXT TEST
035234 022626          5$:  CMP (SP)+,(SP)+   ;;CLEAR THE STACK AFTER A TIME OUT
035236 012637 000004          MOV (SP)+,@#ERRVEC  ;;RESTORE THE ERROR VECTOR
035242 000417          BR 7$           ;;LOOP ON THE PRESENT TEST
035244          6$:;#####END OF CODE FOR THE XOR TESTER#####
035244 032777 000400 143666 BIT #BIT08,@SWR      ;;LOOP ON SPEC. TEST?
035252 001404          BEQ 2$           ;;BR IF NO
035254 127767 143660 143620 CMPB @SWR,$STNM     ;;ON THE RIGHT TEST? SWR<7:0>
035262 001433          BEQ $OVER         ;;BR IF YES
035264 105767 143613          2$:  TSTB $ERFLG      ;;HAS AN ERROR OCCURRED?
035270 001412          BEQ $SVLAD        ;;BR IF NO
035272 032777 001000 143640 BIT #BIT09,@SWR      ;;LOOP ON ERROR?
035300 001404          BEQ 4$           ;;BR IF NO
035302 016767 143602 143576 7$:  MOV $LPERR,$LPADR     ;;SET LOOP ADDRESS TO LAST SCOPE
035310 000420          BR $OVER
035312 105067 143565          4$:  CLRB $ERFLG       ;;ZERO THE ERROR FLAG
035316 105267 143560          $SVLAD: INCB $STNM      ;;COUNT TEST NUMBERS
035322 116767 143554 143700 MOVB $STNM,$TESTN   ;;SET TEST NUMBER IN APT MAILBOX
035330 011667 143552          MOV (SP), $LPADR    ;;SAVE SCOPE LOOP ADDRESS
035334 011667 143550          MOV (SP), $LPERR    ;;SAVE ERROR LOOP ADDRESS
035340 005067 143646          CLR $ESCAPE        ;;CLEAR THE ESCAPE FROM ERROR ADDRESS
035344 112767 000001 143543 MOVB #1,$ERMAX      ;;ONLY ALLOW ONE(1) ERROR ON NEXT TEST
035352 016777 143524 143562 $OVER:  MOV $STNM,@DISPLAY ;;DISPLAY TEST NUMBER
035360 016716 143522          MOV $LPADR,(SP)    ;;FUDGE RETURN ADDRESS

```



```
040466 000764 BR 6$ ;;GO CHANGE TO ASCII
040470 105726 8$: TSTB (SP)+ ;;WAS THE LSD THE FIRST NON-ZERO?
040472 100003 BPL 9$ ;;BR IF NO
040474 116663 177777 177776 MOV -1(SP),-2(R3) ;;YES--SET THE SIGN FOR TYPING
040502 105013 9$: CLRB (R3) ;;SET THE TERMINATOR
040504 012605 MOV (SP)+,R5 ;;POP STACK INTO R5
040506 012603 MOV (SP)+,R3 ;;POP STACK INTO R3
040510 012602 MOV (SP)+,R2 ;;POP STACK INTO R2
040512 012601 MOV (SP)+,R1 ;;POP STACK INTO R1
040514 012600 MOV (SP)+,R0 ;;POP STACK INTO R0
040516 104401 040544 TYPE $DBLK ;;NOW TYPE THE NUMBER
040522 016666 000002 000004 MOV 2(SP),4(SP) ;;ADJUST THE STACK
040530 012616 MOV (SP)+,(SP)
040532 000002 RTI ;;RETURN TO USER
040534 023420 $DTBL: 10000.
040536 001750 1000.
040540 000144 100.
040542 000012 10.
040544 $DBLK: .BLKW 4
```

2944

```
.SBTTL SAVE AND RESTORE R0-R5 ROUTINES
*****
*SAVE R0-R5
*CALL:
* SAVREG
*UPON RETURN FROM $SAVREG THE STACK WILL LOOK LIKE:
*
*TOP---(+16)
* +2---(+18)
* +4---R5
* +6---R4
* +8---R3
*+10---R2
*+12---R1
*+14---R0
```

```
040554 010046 $SAVREG: MOV R0,-(SP) ;;PUSH R0 ON STACK
040556 010146 MOV R1,-(SP) ;;PUSH R1 ON STACK
040560 010246 MOV R2,-(SP) ;;PUSH R2 ON STACK
040562 010346 MOV R3,-(SP) ;;PUSH R3 ON STACK
040564 010446 MOV R4,-(SP) ;;PUSH R4 ON STACK
040566 010546 MOV R5,-(SP) ;;PUSH R5 ON STACK
040570 016646 000022 MOV 22(SP),-(SP) ;;SAVE PS OF MAIN FLOW
040574 016646 000022 MOV 22(SP),-(SP) ;;SAVE PC OF MAIN FLOW
040600 016646 000022 MOV 22(SP),-(SP) ;;SAVE PS OF CALL
040604 016646 000022 MOV 22(SP),-(SP) ;;SAVE PC OF CALL
040610 000002 RTI
```

```
*RESTORE R0-R5
*CALL:
* RESREG
```

```
$RESREG:
040612 012666 000022 MOV (SP)+,22(SP) ;;RESTORE PC OF CALL
040616 012666 000022 MOV (SP)+,22(SP) ;;RESTORE PS OF CALL
040622 012666 000022 MOV (SP)+,22(SP) ;;RESTORE PC OF MAIN FLOW
040626 012666 000022 MOV (SP)+,22(SP) ;;RESTORE PS OF MAIN FLOW
040632 012605 MOV (SP)+,R5 ;;POP STACK INTO R5
040634 012604 MOV (SP)+,R4 ;;POP STACK INTO R4
040636 012603 MOV (SP)+,R3 ;;POP STACK INTO R3
```

040640 012602
 040642 012601
 040644 012600
 040646 000002
 2945

 040650 104413
 040652 016601 000002
 040656 012705 040767
 040662 012704 000014
 040666 012703 177770
 040672 012100
 040674 012101
 040676 005002
 040700 110245
 040702 010002
 040704 005304
 040706 003007
 040710 001405
 040712 005205
 040714 010566 000002
 040720 104414
 040722 000207
 040724 006203
 040726 006001
 040730 006000
 040732 006001
 040734 006000
 040736 006001
 040740 006000
 040742 040302
 040744 062702 000060
 040750 000753
 040752

```

MOV      (SP)+,R2      ;;POP STACK INTO R2
MOV      (SP)+,R1      ;;POP STACK INTO R1
MOV      (SP)+,R0      ;;POP STACK INTO R0
RTI

.SBTTL  DOUBLE LENGTH BINARY TO OCTAL ASCII CONVERT ROUTINE
*****
*THIS ROUTINE WILL CONVERT A 32-BIT UNSIGNED BINARY NUMBER TO AN
*UNSIGNED OCTAL ASCII NUMBER.
*CALL
*
*   MOV      #PNTR,-(SP)      ;;POINTER TO LOW WORD OF BINARY NUMBER
*   JSR      PC,@#$DB20      ;;CALL THE ROUTINE
*   RETURN   ;;THE ADDRESS OF THE FIRST ASCII CHAR. IS ON THE STACK
$DB20:  SAVREG      ;;SAVE ALL REGISTERS
        MOV      2(SP),R1     ;;PICKUP THE POINTER TO LOW WORD
        MOV--   #$OCTVL+13.,R5 ;;POINTER TO DATA TABLE
        MOV      #12.,R4      ;;DO ELEVEN CHARACTERS
        MOV      #^C7,R3      ;;MASK
        MOV      (R1)+,R0     ;;LOWER WORD
        MOV      (R1)+,R1     ;;HIGH WORD
        CLR      R2           ;;TERMINATOR
1$:     MOVVB   R2,-(R5)      ;;PUT CHARACTER IN DATA TABLE
        MOV      R0,R2        ;;GET THIS DIGIT
        DEC      R4           ;;COUNT THIS CHARACTER
        BGT      3$          ;;BR IF NOT THE LAST DIGIT
        BEQ      2$          ;;BR IF IT IS THE LAST DIGIT
        INC      R5           ;;ALL DIGITS DONE-ADJUST POINTER FOR FIRST
        MOV      R5,2(SP)     ;;ASCII CHAR. & PUT IT ON THE STACK
        RESREG     ;;RESTORE ALL REGISTERS
        RTS      PC          ;;RETURN TO USER
2$:     ASR      R3           ;;POSITION THE MASK FOR THE LAST DIGIT
3$:     ROR      R1           ;;POSITION THE BINARY NUMBER FOR
        ROR      R0           ;;
        ROR      R1           ;;
        ROR      R0           ;;
        ROR      R1           ;;
        ROR      R0           ;;
        BIC      R3,R2        ;;MASK OUT ALL JUNK
        ADD     #'0,R2        ;;MAKE THIS CHAR. ASCII
        BR      1$           ;;GO PUT IT IN THE DATA TABLE
$OCTVL: .BLKB  14.          ;;RESERVE DATA TABLE
    
```

2947

040770 010046
040772 016600 000002
040776 005740
041000 111000
041002 006300
041004 016000 041024
041010 000200

041012 011646
041014 016666 000004 000002
041022 000002

```
.SBTTL TRAP DECODER
:*****
:THIS ROUTINE WILL PICKUP THE LOWER BYTE OF THE 'TRAP' INSTRUCTION
:AND USE IT TO INDEX THROUGH THE TRAP TABLE FOR THE STARTING ADDRESS
:OF THE DESIRED ROUTINE. THEN USING THE ADDRESS OBTAINED IT WILL
:GO TO THAT ROUTINE.
$TRAP:  MOV     R0,-(SP)           ;;SAVE R0
        MOV     2(SP),R0         ;;GET TRAP ADDRESS
        TST     -(R0)           ;;BACKUP BY 2
        MOVB    (R0),R0         ;;GET RIGHT BYTE OF TRAP
        ASL     R0              ;;POSITION FOR INDEXING
        MOV     $TRPAD(R0),R0   ;;INDEX TO TABLE
        RTS     R0              ;;GO TO ROUTINE
:THIS IS USE TO HANDLE THE 'GETPRI' MACRO
$TRAP2: MOV     (SP),-(SP)       ;;MOVE THE PC DOWN
        MOV     4(SP),2(SP)     ;;MOVE THE PSW DOWN
        RTI                      ;;RESTORE THE PSW
```

041024 041012
041026 037226
041030 040126
041032 040102
041034 040142
041036 040330
041040 040026
041042 036202
041044 036132
041046 036454
041050 036574
041052 040554
041054 040612

```
.SBTTL TRAP TABLE
:THIS TABLE CONTAINS THE STARTING ADDRESSES OF THE ROUTINES CALLED
:BY THE 'TRAP' INSTRUCTION.
:ROUTINE
:-----
$TRPAD: .WORD    $TRAP2
        $TYPE   ;;CALL=TYPE       TRAP+1(104401)  TTY TYPEOUT ROUTINE
        $TYPOC  ;;CALL=TYPOC     TRAP+2(104402)  TYPE OCTAL NUMBER (WITH LEADING ZEROS)
        $TYPOS  ;;CALL=TYPOS     TRAP+3(104403)  TYPE OCTAL NUMBER (NO LEADING ZEROS)
        $TYPON  ;;CALL=TYPON     TRAP+4(104404)  TYPE OCTAL NUMBER (AS PER LAST CALL)
        $TYPDS  ;;CALL=TYPDS     TRAP+5(104405)  TYPE DECIMAL NUMBER (WITH SIGN)
        $TYPBN  ;;CALL=TYPBN     TRAP+6(104406)  TYPE BINARY (ASCII) NUMBER
        $GTSWR  ;;CALL=GTSWR     TRAP+7(104407)  GET SOFT-SWR SETTING
        $CKSWR  ;;CALL=CKSWR     TRAP+10(104410) TEST FOR CHANGE IN SOFT-SWR
        $RDCHR  ;;CALL=RDCHR     TRAP+11(104411) TTY TYPEIN CHARACTER ROUTINE
        $RDLIN  ;;CALL=RDLIN     TRAP+12(104412) TTY TYPEIN STRING ROUTINE
        $$SAVREG ;;CALL=SAVREG   TRAP+13(104413) SAVE R0-R5 ROUTINE
        $RESREG ;;CALL=RESREG   TRAP+14(104414) RESTORE R0-R5 ROUTINE
```

2948

041056 012737 041234 000024
041064 012737 000340 000026
041072 010046
041074 010146
041076 010246
041100 010346
041102 010446
041104 010546
041106 017746 140026
041112 010667 000122
041116 012737 041130 000024
041124 000000
041126 000776

```
.SBTTL POWER DOWN AND UP ROUTINES
:*****
:POWER DOWN ROUTINE
$PWRDN: MOV     #$ILLUP,@#PWRVEC ;;SET FOR FAST UP
        MOV     #340,@#PWRVEC+2 ;;PRIO:7
        MOV     R0,-(SP)        ;;PUSH R0 ON STACK
        MOV     R1,-(SP)        ;;PUSH R1 ON STACK
        MOV     R2,-(SP)        ;;PUSH R2 ON STACK
        MOV     R3,-(SP)        ;;PUSH R3 ON STACK
        MOV     R4,-(SP)        ;;PUSH R4 ON STACK
        MOV     R5,-(SP)        ;;PUSH R5 ON STACK
        MOV     @SWR,-(SP)      ;;PUSH @SWR ON STACK
        MOV     SP,$SAVR6      ;;SAVE SP
        MOV     #$PWRUP,@#PWRVEC ;;SET UP VECTOR
        HALT
        BR      -2             ;;HANG UP
:*****
```

041130 012737 041234 000024
041136 016706 000076
041142 005067 000072
041146 005267 000066

```
:POWER UP ROUTINE
$PWRUP: MOV     #$ILLUP,@#PWRVEC ;;SET FOR FAST DOWN
        MOV     $$SAVR6,SP      ;;GET SP
        CLR     $$SAVR6        ;;WAIT LOOP FOR THE TTY
1$:      INC     $$SAVR6        ;;WAIT FOR THE INC
```


