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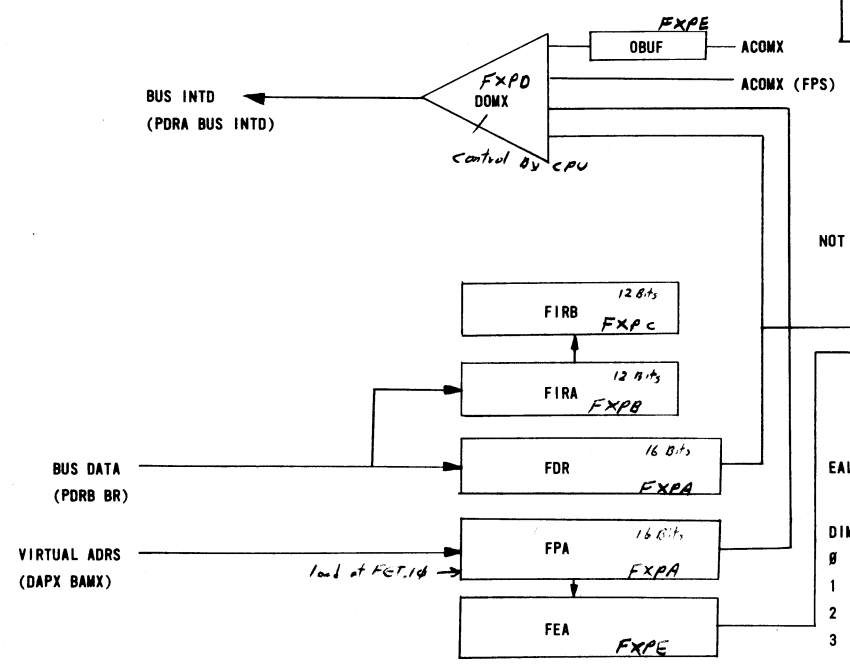
- SHIFT CONTROL [8:51]
- 0 - EALU
 - 1 - DIV
 - 2 - MUL
 - 3 - NORM
 - 4 - ALIGN
 - 5 - NOT USED
 - 6 - NOT USED
 - 7 - 0 SHIFT
 - IX - CLR CONTROL AT T2 LOAD CONTROL WITH SPECIFIED FUNCTION AT T3
- MISCELLANEOUS CONTROL [25:27]
- 0 - NOP
 - 1 - FPS CLK
 - 2 - UBRK CLK
 - 3 - DOMX MOD
 - 4 - OBUF CLK
 - 5 - CLR QR
 - 6 - LD FP REQ
 - 7 - FP CLASS

- EALUC [3:55]
- 0 - A PLUS B
 - 1 - A PLUS B PLUS 1
 - 2 - A MINUS B MINUS 1
 - 3 - A MINUS B
 - 4 - A
 - 5 - B
 - 6 - NOT USED
 - 7 - NOT USED

- FALUC [56:59]
- 0 - A * B
 - 1 - ~A
 - 2 - B
 - 3 - A ~ B
 - 4 - A PLUS B
 - 5 - A PLUS B PLUS 1
 - 6 - A MINUS 1
 - 7 - A MINUS B
- 10 - ZERO
 - 11 - NOT USED
 - 12 - NOT USED
 - 13 - NOT USED
 - 14 - A PLUS B CONDITIONAL (SWR)
 - 15 - NOT USED
 - 16 - MUL/DIV CONDITIONAL (SWR)
 - 17 - A

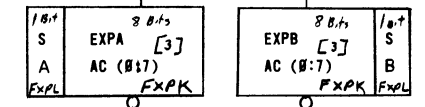
- QMX [32:33]
- 0 - SCR OUT
 - 1 - Q SHIFTER
 - 2 - CONDITIONAL SCR OUT (FD)
 - 3 - QUOTIENT
- FMX [34:35]
- 0 - SCR OUT
 - 1 - Q SHIFTER
 - 2 - CONDITIONAL SCR OUT (FD)
 - 3 - ROUND, INT INC

To load exec. LOUB
Micro Break Reg
FxpC
50B2



- SC CLK [3]
- 0 - NOP
 - 1 - CLK SC

- ER CLK [12]
- 0 - NOP
 - 1 - CLK ER



- AMX [18:19]
- 0 - EXPA
 - 1 - ABS SC
 - 2 - SC
 - 3 - ER
- BMX [18:17]
- 0 - EXPB
 - 1 - CONSTANTS
 - 2 - DIMX 6:0
 - 3 - SHIFT CONTROL

- NEXT ADR [68:75]
- SEE FLOWS

- UBR [65:67]
- 0 - NO BRANCH
 - 1 - 7 - BRANCH ENABLE (SEE FLOWS)

- UAF [60:61]
- 0 - BRANCH ENABLE
 - 1 - BRANCH ENABLE 3:2
 - 2 - BRANCH ENABLE 1:0
 - 3 - BRANCH ENABLE 3:0

- UJMP [64]
- 0 - NOP
 - 1 - TRAP TO 3 IF NA (1:0)=3

- LONG CYCLE [44]
- 0 - 180 NS STATE
 - 1 - 240 NS STATE

- ATTN WAIT [62]
- 0 - NOP
 - 1 - WAIT FOR FPATTN

- ACKN WAIT [63]
- 0 - NOP
 - 1 - WAIT FOR FPACKN

- CNST [6:7]
- 0 - 377 CONSTANTS

- SIGN CONTROL [28:29:42]
- 0 - SD ← SD
 - 1 - SD ← SC09
 - 2 - SD ← SS
 - 3 - SD ← ~SS
 - 4 - SD ← SD XOR SS
 - 5 - SD ← SD XOR SUBTRACT
 - 6 - SD ← 0
 - 7 - SD ← SCR OUT

- FIR CLK [24]
- 0 - NOP
 - 1 - LOAD FIRB
- FPC1 [21]
- 0 - DAT1
 - 1 - DAT0

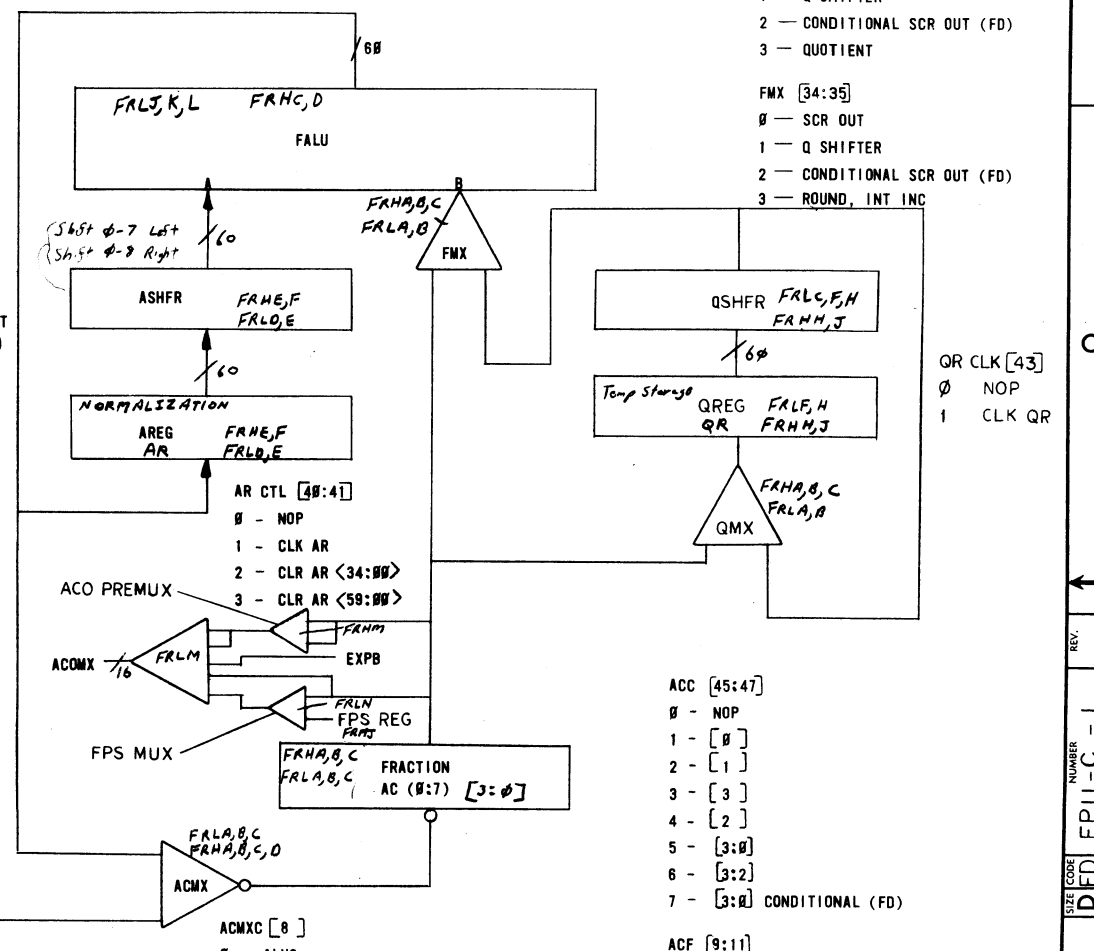
- FP REG WR [20]
- 0 - NOP
 - 1 - WRITE CPU RX

- ACOMX [38:39]
- 0 - ACX [0] / FPS
 - 1 - ACX [1]
 - 2 - ACX [2]
 - 3 - ACX [3]
- EN FM0 [22]
- 0 - DISABLE FM0 TRAP
 - 1 - ENABLE FM0 TRAP

- FP SYNC [29]
- 0 - NOP
 - 1 - FP SYNC
- DISABLE INTR [52]
- 0 - ALLOW INTR CLR
 - 1 - DISABLE INTR CLR

- FLOATING CONDITION CODES [30:31]
- 0 - FN, FZ ← CONDITIONS, FC, FV ← 0
 - 1 - FN, FZ, FV ← CONDITIONS FC ← 0
 - 2 - FC ← 1
 - 3 - NOP

- FEC IS AC7 [1]
- FEA IS AC7 [2]



- ACO PREMUX
- 1 - CLK AR
 - 2 - CLR AR <34:00>
 - 3 - CLR AR <59:00>
- FPS MUX
- FRACTION AC (6:7) [3:0]
- ACMX [8]
- 0 - ALUS
 - 1 - DIMX

- ACC [45:47]
- 0 - NOP
 - 1 - [0]
 - 2 - [1]
 - 3 - [3]
 - 4 - [2]
 - 5 - [3:0]
 - 6 - [3:2]
 - 7 - [3:0] CONDITIONAL (FD)

- ACF [9:11]
- 0 - NOT USED
 - 1 - ACDV1/ACDV1
 - 2 - ACS/ACD
 - 3 - ACD/ACD
 - 4 - ACS/ACS
 - 5 - ACD/ACS
 - 6 - ACS/AC6
 - 7 - AC7/AC7 EXPA/EXPB AND FRACTION

REV.	CHANGE NO.

FIRST USED ON OPTION/MODEL		QTY.	DESCRIPTION	PART NO.	ITEM NO.
FPII-C					
PARTS LIST					
DIMENSIONAL TOLERANCE					
DIMENSIONS ARE MILLIMETERS UNLESS OTHERWISE SPECIFIED					
MILLIMETERS	INCHES	ANGLES			
.XX ±0.10	.XX ±.006	±0°30'			
.X ±0.05	.X ±.02				
X ±.2	X ±.1				
THIRD ANGLE PROJECTION					
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY					
MATERIAL					
FINISH					
SCALE					
SHEET 1 OF 15					

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READY
 RDY.# (3)
 CLEAR AC6 AND SIGNS
 DECODE IRA
 LONG CYCLE ← 1
 BMX ← CNST 0
 EALU ← B
 FALU ← 0
 ACMX ← ALUS
 SS, SD ← 0
 WAIT FOR FP START
 FEA ← FPA
 FIRB ← FIRA
 AC6[3;0] ← ACMX
 FP REQ ← IR DECODE
 IF3 (000)

Prevent False Start

NOM.# (30)
 WAIT FOR CPU TO ALLOW EXECUTE
 FP SYNC ← 1
 WAIT FOR FP START
 SCR OUT ← ACD/ACS
 AMX ← SCR OUT
 BMX ← SCR OUT
 EALU ← A MINUS B
 SC ← EALU
 SD ← SCR OUT
 IF3 (000)



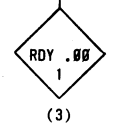
SXP.# (50)
 SUBTRACT BIAS
 SCR OUT ← ACD/ACD
 AMX ← SCR OUT
 BMX ← CNST 200
 EALU ← A MINUS B
 SC ← EALU
 (64)
 SXP.1# (64)
 STORE IN AC6 [2]
 AMX ← SC
 EALU ← A
 DIMX ← EALU
 ACMX ← DIMX
 AC6 [2] ← DIMX
 (147)

SXP.2# (147)
 LOAD OUTPUT BUFFER
 EALU ← A
 ACMX ← ALUS
 AMX ← SC
 ACOMX ← AC6 [2]
 OBUF ← ACOMX
 SET FCC (0)
 SD ← SC09
 (63)
 SXP.3# (63)
 WAIT FOR CP TO SAY IT HAS THE DATA
 FP SYNC ← 1
 FC ← DATO
 FP REG WR ← 1
 WAIT FOR FPATTN
 (152)



STR SP = STFPS + STEXP + STCI + STCF + STST

STF.# (62)
 FORCE DOMX TO FPS
 FP SYNC ← 1
 FC ← DATO
 FP REG WR ← 1
 DOMX ← FPS
 WAIT FOR FPATTN
 (23)
 STF.1# (23)
 HOLD DATA TIL CP HAS IT FOR MODE 0
 FP REG WR ← 1
 DOMX ← FPS
 (3)



LDE.# (15)
 GET 2's COMP # FROM MEMORY
 FP ← SYNC
 ACMX ← DIMX
 BMX ← DIMX
 EALU ← B
 WAIT FOR FPATTN
 AC6 [3] ← ACMX
 SC ← EALU
 (10)
 LDEXP.1 (10)

LDE.1# (10)
 PUT 14:7 IN ER TO SET BZ, BN
 SCR OUT ← AC6/AC6
 BMX ← SCR OUT
 EALU ← B
 ER ← EALU
 ACMX ← DIMX
 SS ← SCR OUT
 (207)
 LDE.2# (207)
 SET BZ FOR 6;0
 SAVE AC6 [3]
 SCR OUT ← ACD/ACD
 FMX ← SCR OUT[3;0] COND
 FALU ← B
 AR ← FALU
 SD ← SCR OUT
 AMX ← SC
 EALU ← A
 SC ← EALU
 (205)

NAO Field UAF = 2
D 3 input of y Branch max enable (UBA) select control FRMA

LDE.3# (362)
 DO ADD AND GO TO READY
 AMX ← SC
 BMX ← CNST 200
 EALU ← A PLUS B
 FALU ← A
 ACMX ← ALUS
 ACD [3] ← ACMX
 SET FCC (0)
 (3)
 RDY.# 1 (3)

LDE.4# (360)
 GO TO UNDERFLOW
 AMX ← SC
 EALU ← A
 FALU ← A
 ACMX ← ALUS
 ACD [3] ← ACMX
 SET FCC (0)
 (360)
 UNF.2# 14 (207)
 UNF.1# 14 (205)

LDE.5# (363)
 GO TO OVERFLOW
 AMX ← SC
 BMX ← CNST 377
 EALU ← A PLUS B PLUS 1
 FALU ← A
 ACMX ← ALUS
 ACD [3] ← ACMX
 SET FCC (1)
 (70)
 OVF.# 14 (70)
 ~BZ (70)

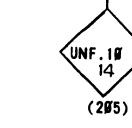
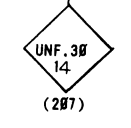
LDE.6# (361)
 COULD BE GOOD NUMBER CHECK FOR -1
 AMX ← ER
 BMX ← CNST 1
 EALU ← A PLUS B
 ER ← EALU
 (226)
 3F# (226)

LDE.7# (227)
 6;0 WAS NOT 0 STORE ANYWAY
 AMX ← SC
 EALU ← A
 FALU ← A
 ACMX ← ALUS
 ACD [3] ← ACMX
 SET FCC (0)
 (227)
 3F# (236)

LDE.8# (226)
 6;0 WAS 0 RESULT WILL BE UFLOW
 AMX ← SC
 EALU ← A
 FALU ← A
 ACMX ← ALUS
 ACD [3] ← ACMX
 SET FCC (0)
 (226)
 ~FIU (207)
 7F2 (205) FIU (205)

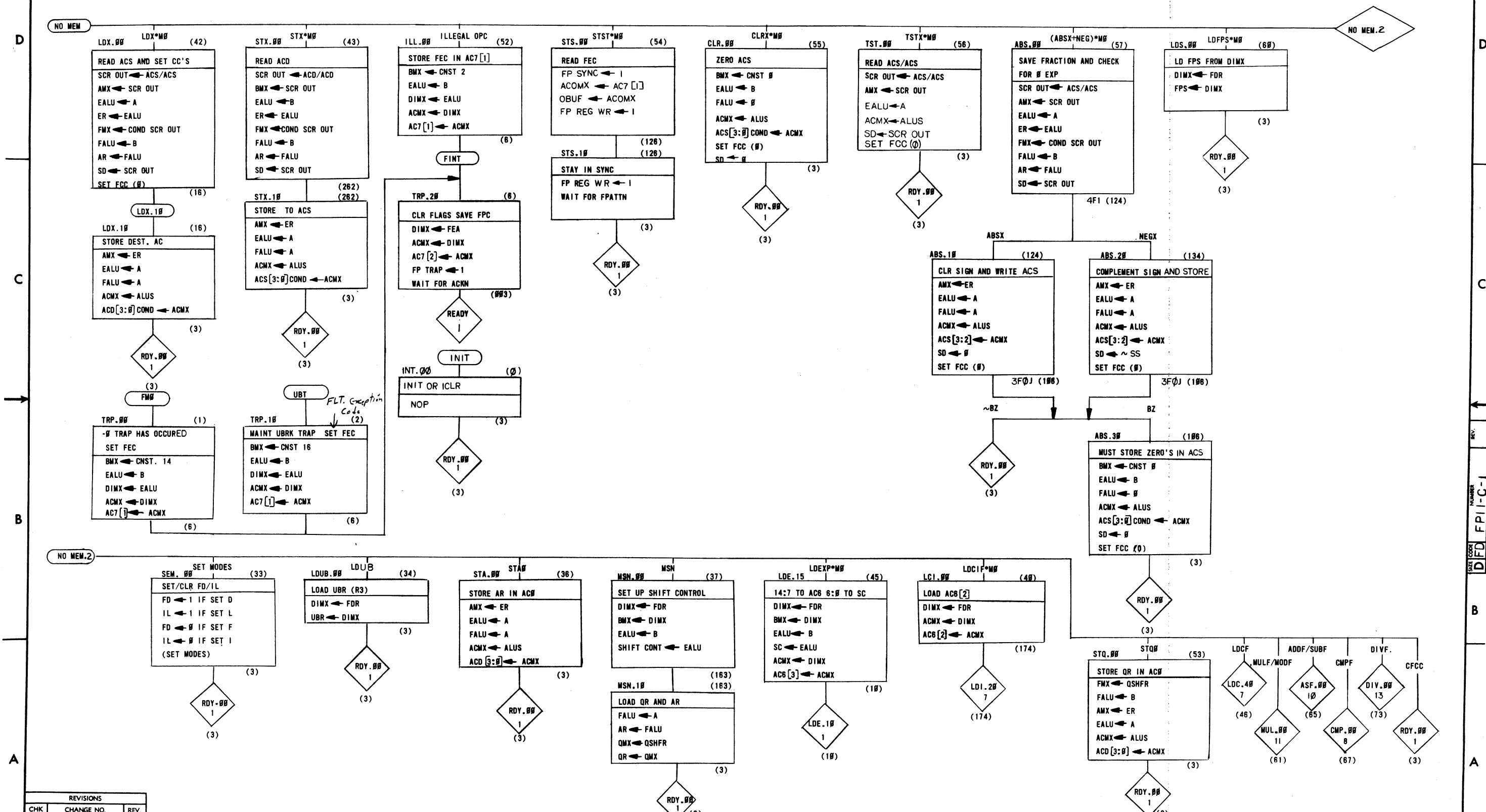
LDE.9# (236)
 14:7 WAS ALL 1's
 NOP
 (236)
 RDY.# 1 (3)

LDE.95 (237)
 UNDERFLOW
 NOP
 (237)
 ~FIU (207)
 7 F2 (205) FIU (205)



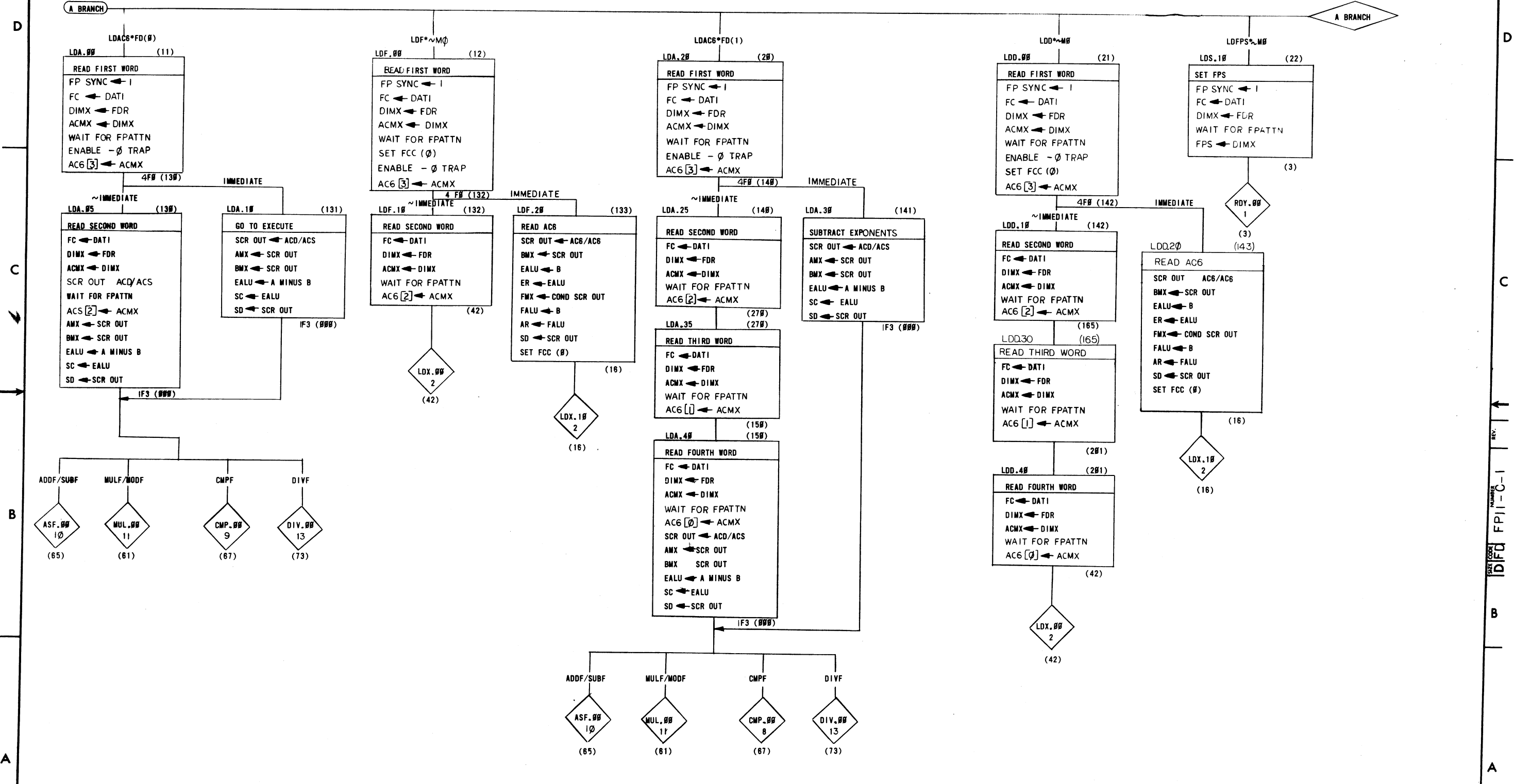
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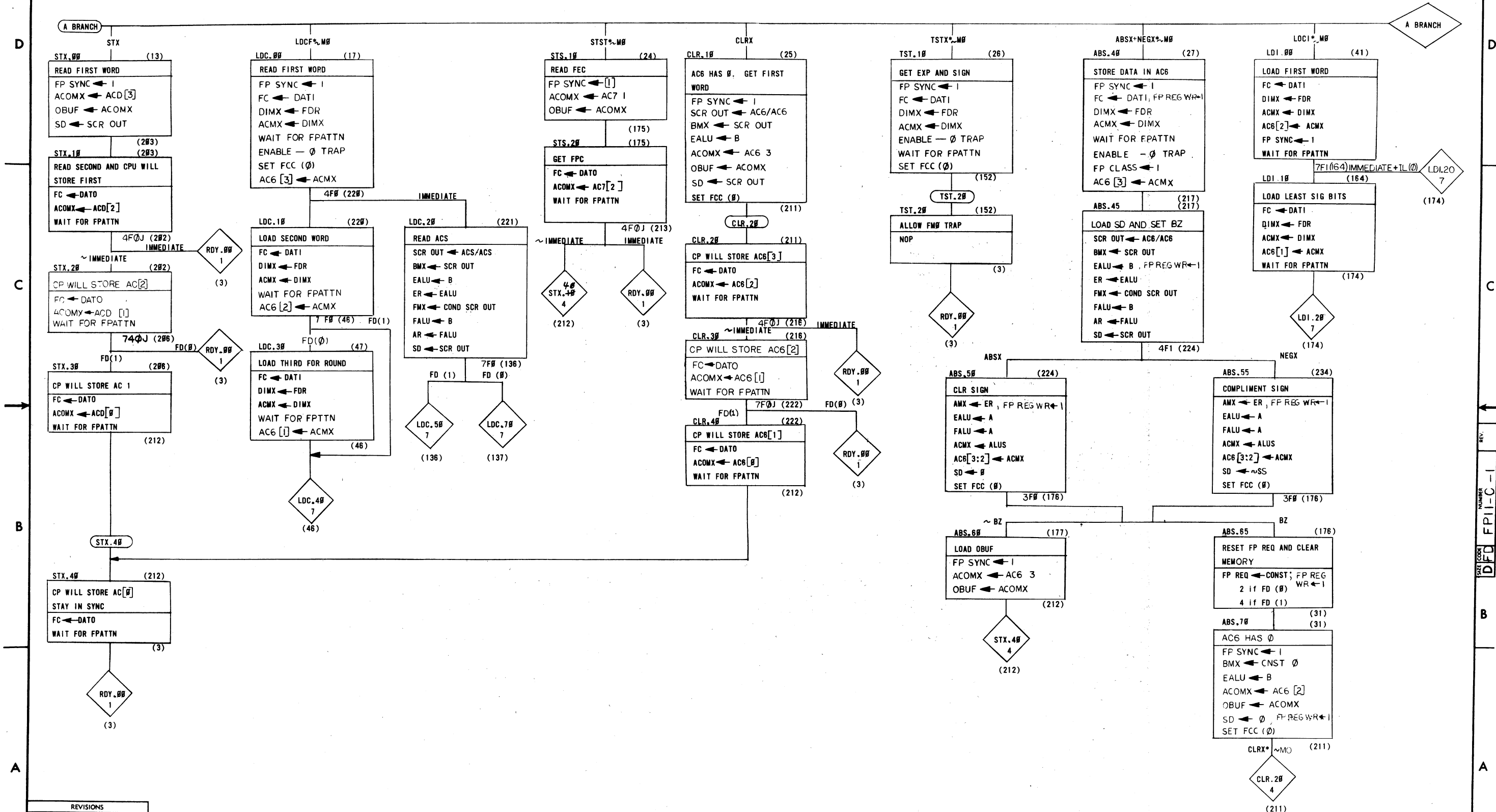


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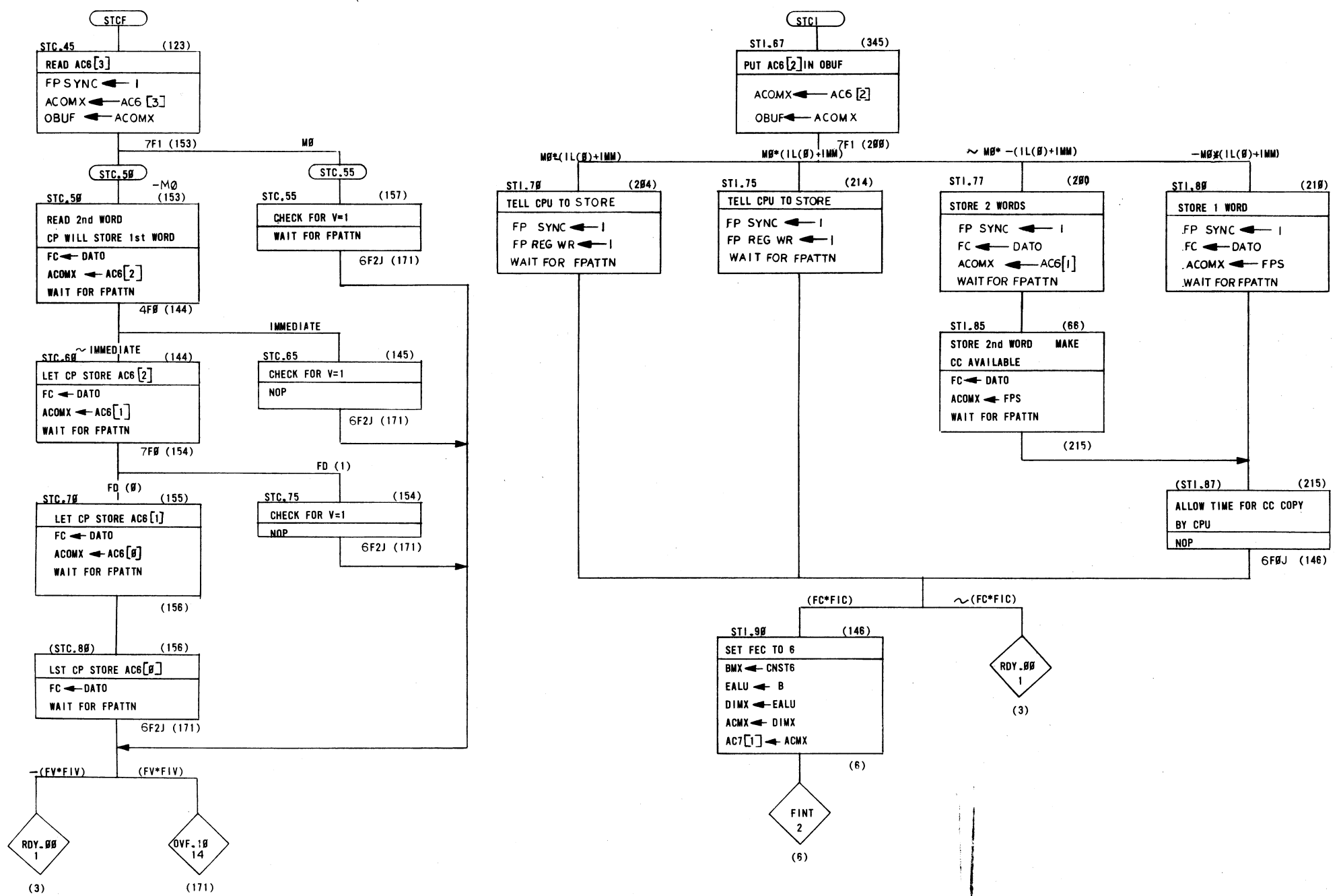


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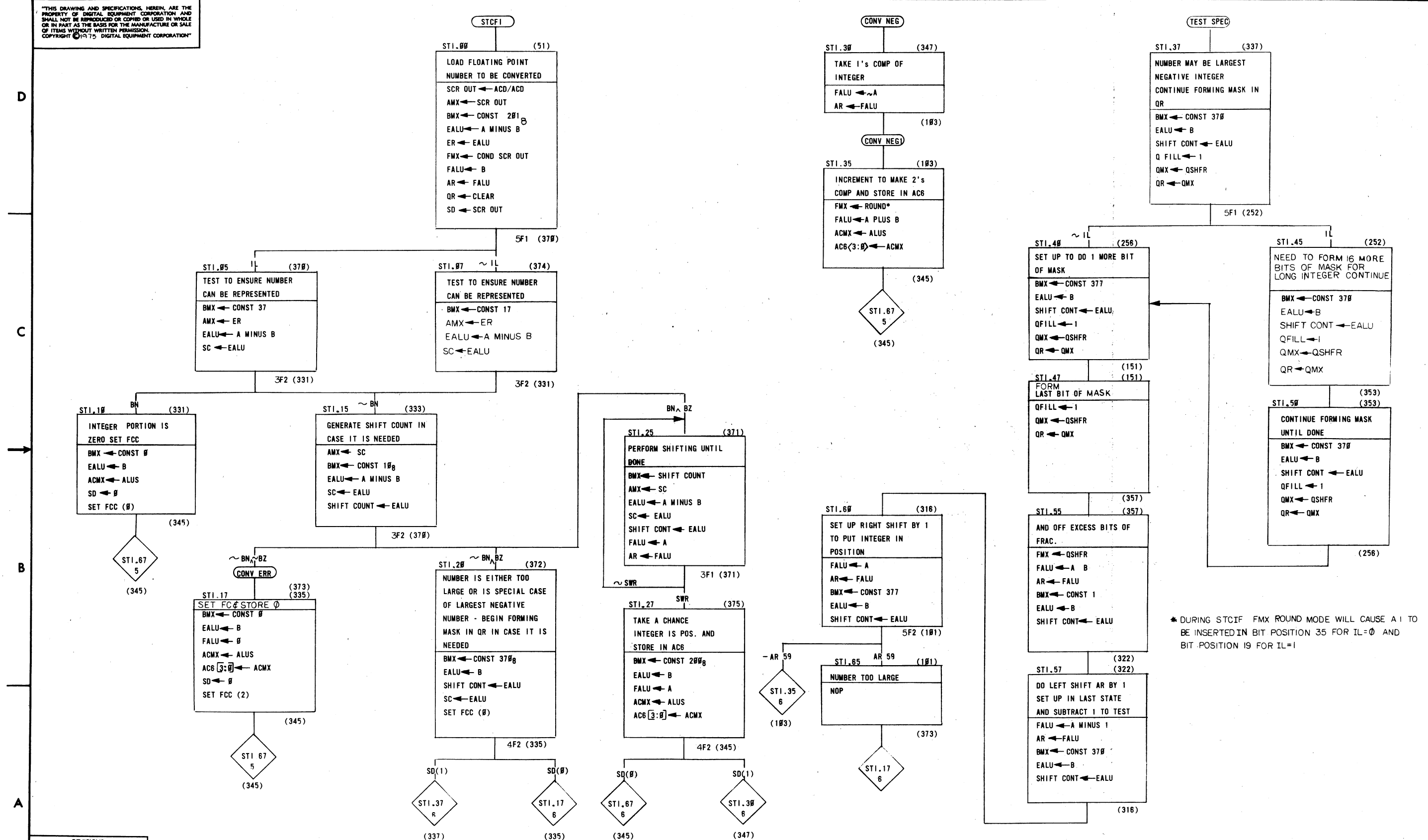
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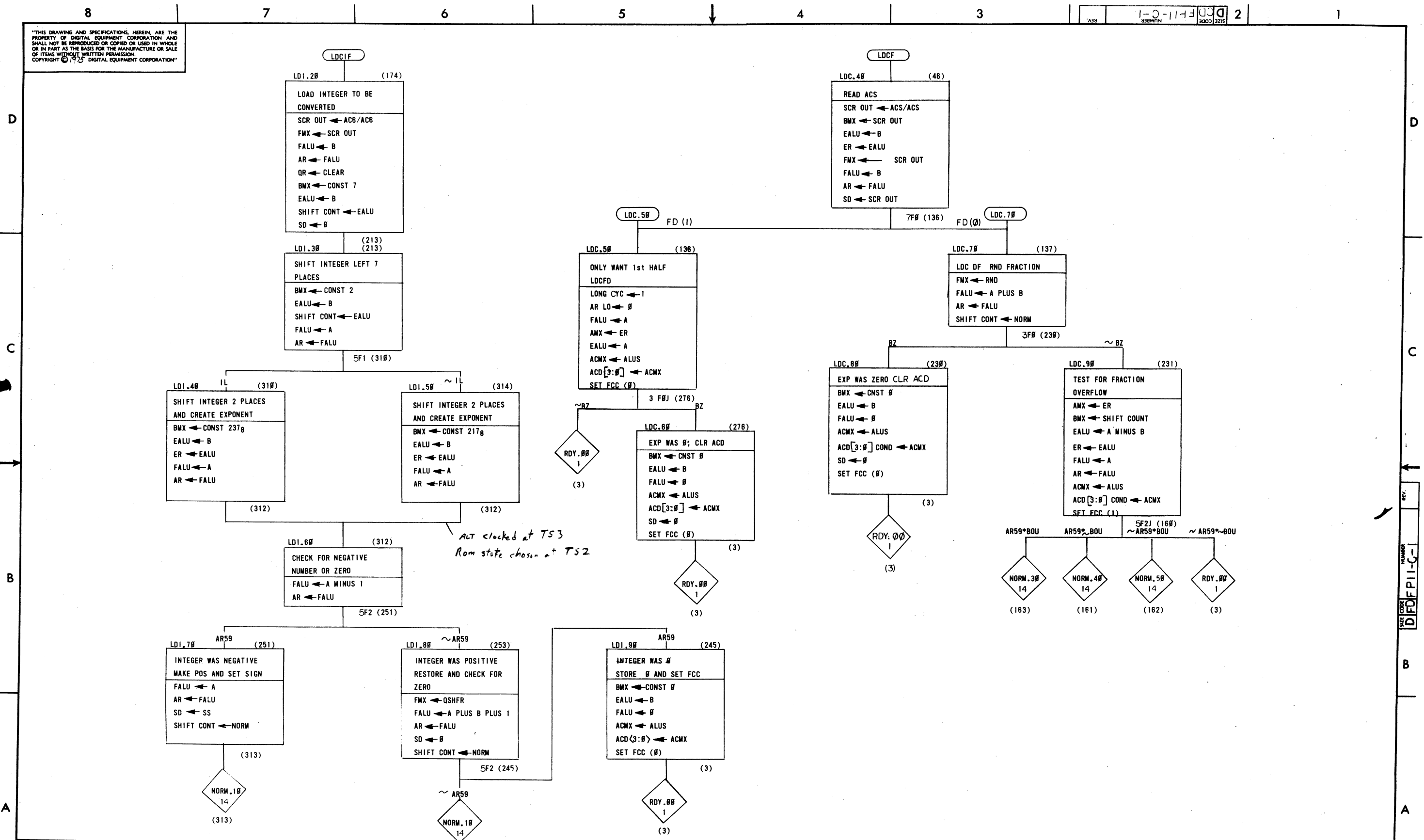


* DURING STCFI FMX ROUND MODE WILL CAUSE A 1 TO BE INSERTED IN BIT POSITION 35 FOR IL=0 AND BIT POSITION 19 FOR IL=1

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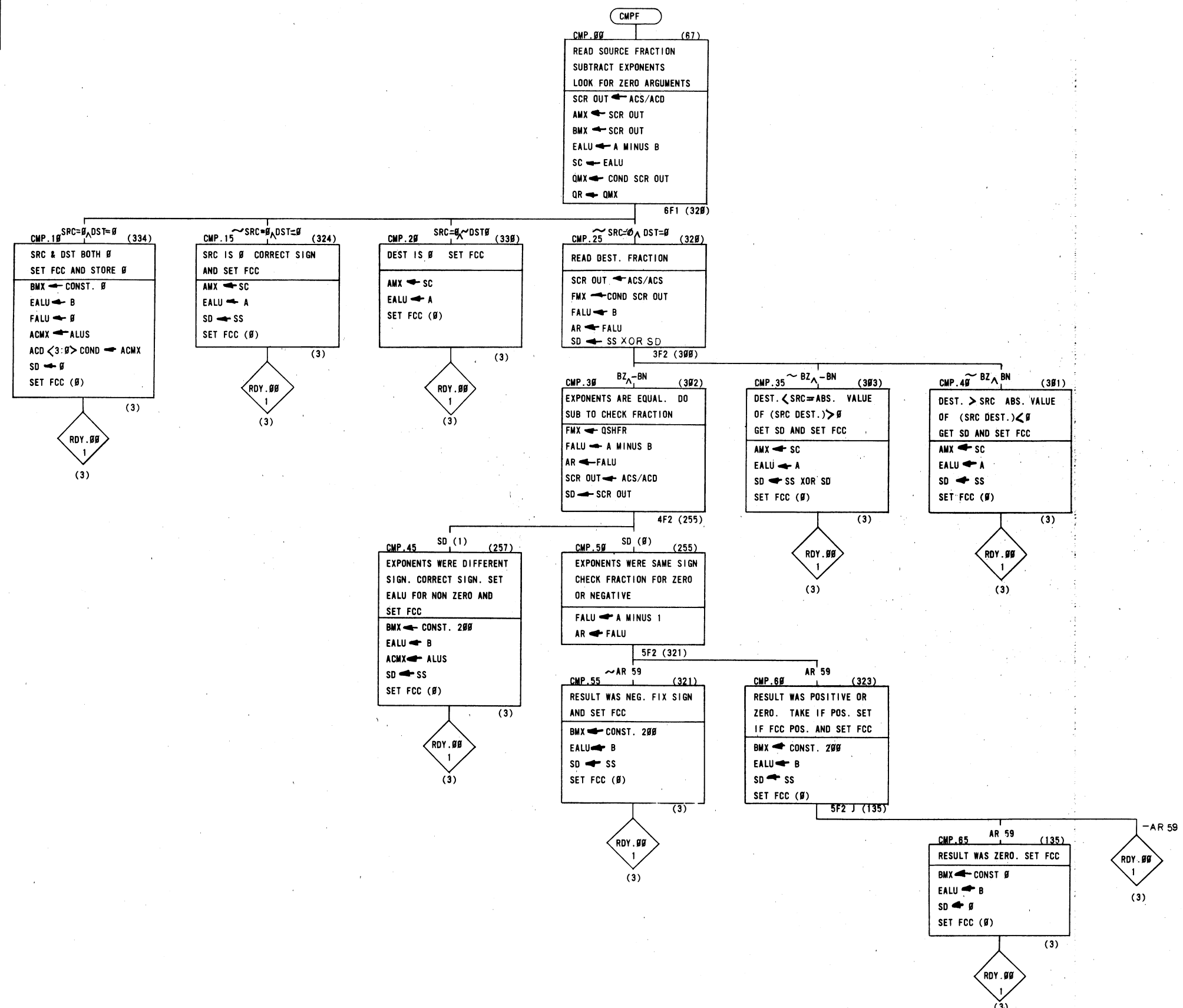
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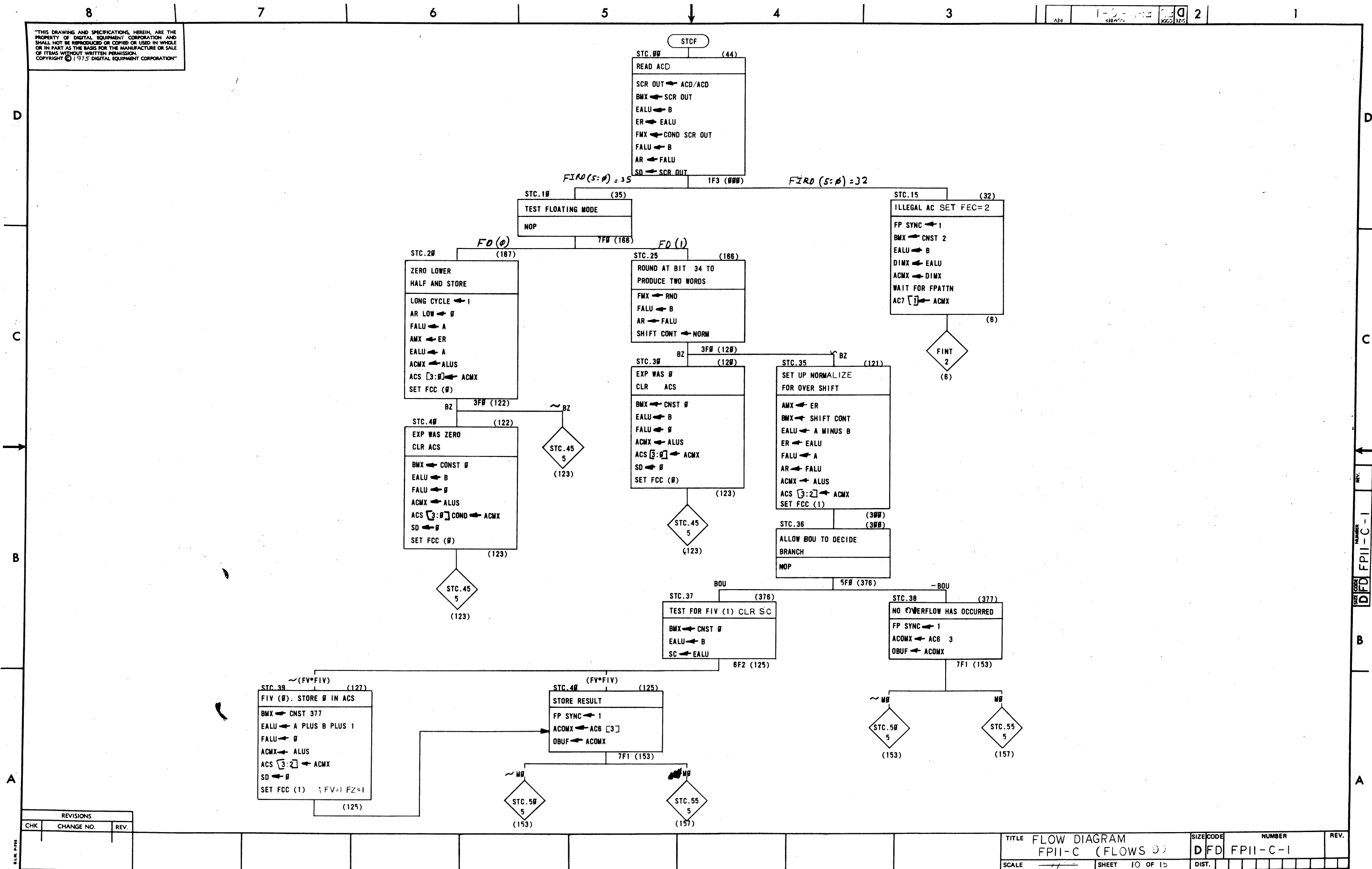
TITLE	FLOW DIAGRAM FPII-C (FLOWS 7)	SIZE/CODE	D F D	NUMBER	FFII-C-1	REV.	
SCALE		SHEET	B	OF	15	DIST.	

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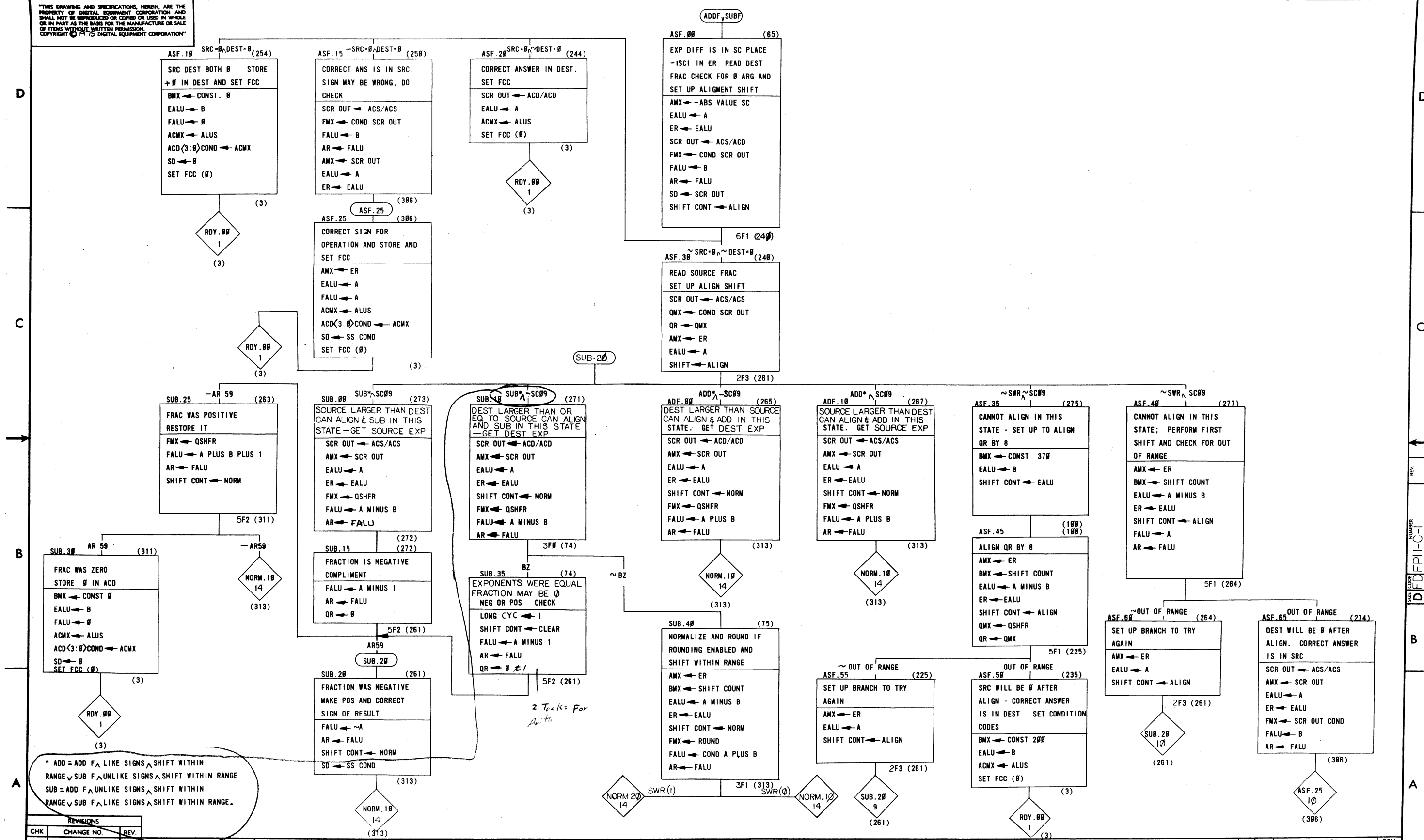
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TITLE	FLOW DIAGRAM FPII-C (FLOWS)	SIZE CODE	NUMBER	REV.
SCALE	SHEET 10 OF 15	D F D	FPII-C-1	

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* ADD = ADD F_A LIKE SIGNS, SHIFT WITHIN RANGE
 SUB = SUB F_A UNLIKE SIGNS, SHIFT WITHIN RANGE
 SUB = ADD F_A UNLIKE SIGNS, SHIFT WITHIN RANGE
 SUB = SUB F_A LIKE SIGNS, SHIFT WITHIN RANGE.

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DEC FORM NO. DND 138

REV. NUMBER DFD FPII-C-1

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MUL MOD (61)

READ SOURCE FRAC.; ADD EXPONENTS AND LOOK FOR ZERO ARGUMENTS

SCR OUT ← ACD/ACS
 BMX ← SCR OUT
 EALU ← A PLUS B
 ER ← EALU
 QMX ← COND SCR OUT
 QR ← QMX
 AR ← B
 SD ← SCR OUT

MUL 7B (72)

NORMALIZE AND ROUND IF ENABLED — CALCULATE SIGN

FMX ← ROUND
 FALU ← COND A PLUS B
 AR ← FALU
 AMX ← ER
 BMX ← SHIFT COUNT
 EALU ← A MINUS B
 ER ← EALU
 SHIFT CONT ← NORM
 SD ← SS XOR SD

MUL 25 SRC=B, DEST=B (354)

MULTIPLICATION BY ZERO
 STORE B IN DEST AND SET FCC

FCC ← CONST B
 EALU ← B
 FALU ← B
 ACMX ← ALUS
 ACD<3:B> COND ← ACMX
 SD ← B
 SET FCC (B)

MUL 2B SRC=B, DEST=B (344)

MULTIPLICATION BY ZERO
 STORE B IN DEST AND SET FCC

FCC ← CONST B
 EALU ← B
 FALU ← B
 ACMX ← ALUS
 ACD<3:B> COND ← ACMX
 SD ← B
 SET FCC (B)

MUL 15 SRC=B, DEST=0 (350)

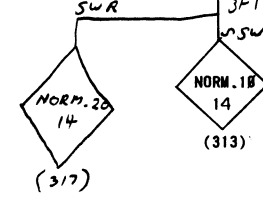
MULTIPLICATION BY ZERO
 STORE B IN DEST AND SET FCC

FCC ← CONST B
 EALU ← B
 FALU ← B
 ACMX ← ALUS
 ACD<3:B> COND ← ACMX
 SD ← B
 SET FCC (B)

MUL 1B SRC=B, DEST=B (340)

READ DEST FRAC.; LOAD STEP COUNT WITH 2's COMP. OF NUMBER OF BITS TO MULTIPLY

SCR OUT ← ACD/ACD
 FMX ← COND SCR OUT
 BMX ← CONST. 30B
 EALU ← B
 SC ← EALU
 SD ← SS



MOD B MOD (355)

STORE ZERO IN ACDv1

BMX ← CONST B
 EALU ← B
 FALU ← B
 ACMX ← ALUS
 ACDv1 [3:B] COND ← ACMX
 SD ← B

MUL 3B ~MOD (351)

GO BACK TO READY MUL BY 0
 NOP

MUL 35 (233)

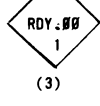
SET UP SHIFT CONTROL FOR MUL LOOP

SCR OUT ← ACD/ACD
 FMX ← COND SCR OUT
 AMX ← ISCI
 BMX ← SHIFT COUNT
 EALU ← A MINUS B
 SC ← EALU
 SHIFT CONT ← MUL SHF

MUL 4B (232)

STEP COUNT OFF BY 32; CORRECT IT

AMX ← SC
 BMX ← CONST 40B
 EALU ← A PLUS B
 SC ← EALU



MUL 5B SWR, SCB9, A, SCB0 (113)

DO MULTIPLY UNTIL COMPLETE (COPY)

SCR OUT ← ACD/ACD
 FMX ← SCR OUT COND
 FALU ← MUL/DIV COND
 AR ← FALU
 QMX ← QSHFR
 QR ← QMX
 AFILL ← SIGN EXTEND
 AMX ← SC
 BMX ← SHIFT COUNT
 EALU ← A MINUS B
 SC ← EALU
 SHIFT CONT ← MUL SHF

MUL 45 (112)

DO MULTIPLY UNTIL COMPLETE

SCR OUT ← ACD/ACD
 FMX ← SCR OUT COND
 FALU ← MUL/DIV COND
 AR ← FALU
 QMX ← QSHFR
 QR ← QMX
 AFILL ← SIGN EXTEND
 AMX ← SC
 BMX ← SHIFT COUNT
 EALU ← A MINUS B
 SC ← EALU
 SHIFT CONT ← MUL SHF

MUL 55 SWR, SCB9, A, SCB0 (111)

MULTIPLY IS DONE
 SUBT EXCESS 200B FROM EXPONENT & GET NORM SHIFT AND GET SIGNS

AMX ← ER
 BMX ← CONST 200B
 EALU ← A MINUS B
 ER ← EALU
 SHIFT CONT ← CLEAR
 SCR OUT ← ACS/ACD
 FALU ← A
 SHIFT CONT ← NORM
 SD ← SCR OUT

MUL 5B SWR, SCB9, A, SCB0 (110)

MULTIPLY IS DONE
 MULTIPLY RESULTED IN CORRECT ANS BUT LEFT SHIFTED; SUBTRACT 201B FROM EXPONENT AND SET UP FOR ROUNDING AND GET SIGNS

AMX ← ER
 BMX ← CONST 201B
 EALU ← A MINUS B
 ER ← EALU
 SHIFT CONT ← CLEAR
 SCR OUT ← ACS/ACD
 FALU ← A
 SHIFT CONT ← NORM
 SD ← SCR OUT

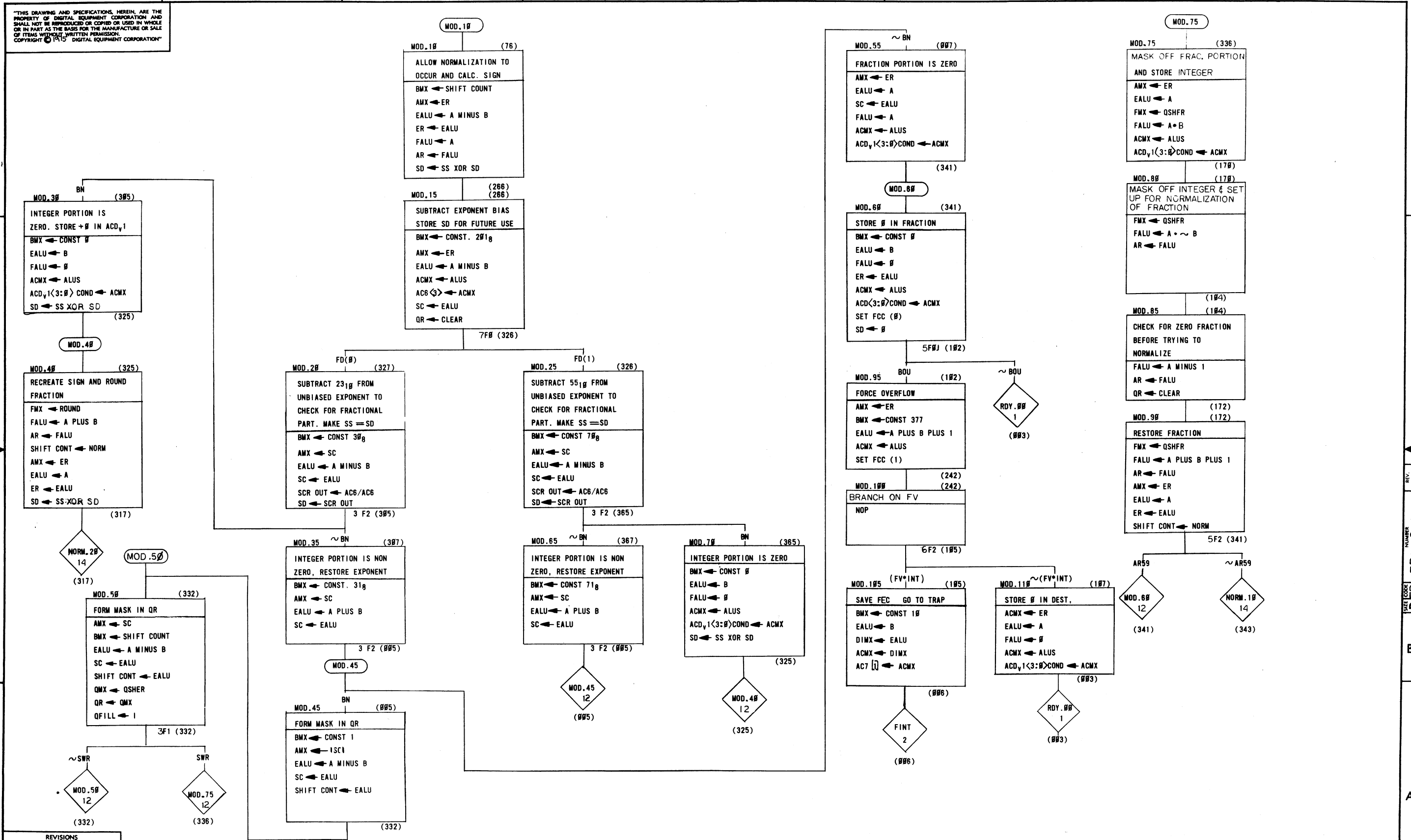
MUL 65 ~SWR (114)

DO MULTIPLY UNTIL COMPLETE (COPY)

SCR OUT ← ACD/ACD
 FMX ← COND SCR OUT
 FALU ← MUL/DIV COND
 AR ← FALU
 AFILL ← SIGN EXTEND
 QMX ← QSHFR
 QR ← QMX
 AMX ← SC
 BMX ← SHIFT COUNT
 EALU ← A MINUS B
 SC ← EALU
 SHIFT CONT ← MUL SHF



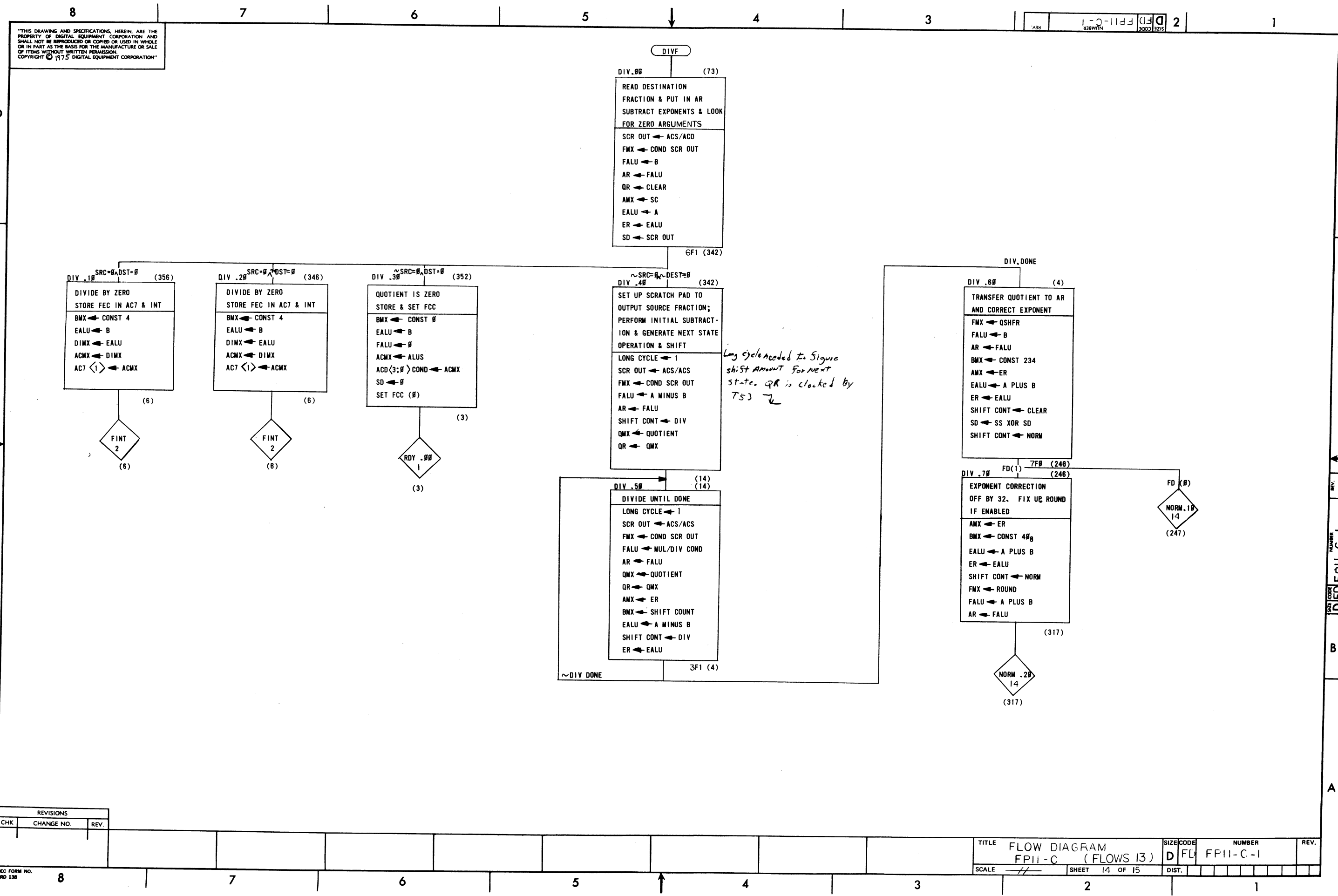
REVISIONS		
CHK	CHANGE NO.	REV.



REVISIONS		
CHK	CHANGE NO.	REV.

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REV. 2
 SIZE CODE D
 NUMBER FPII-C-1



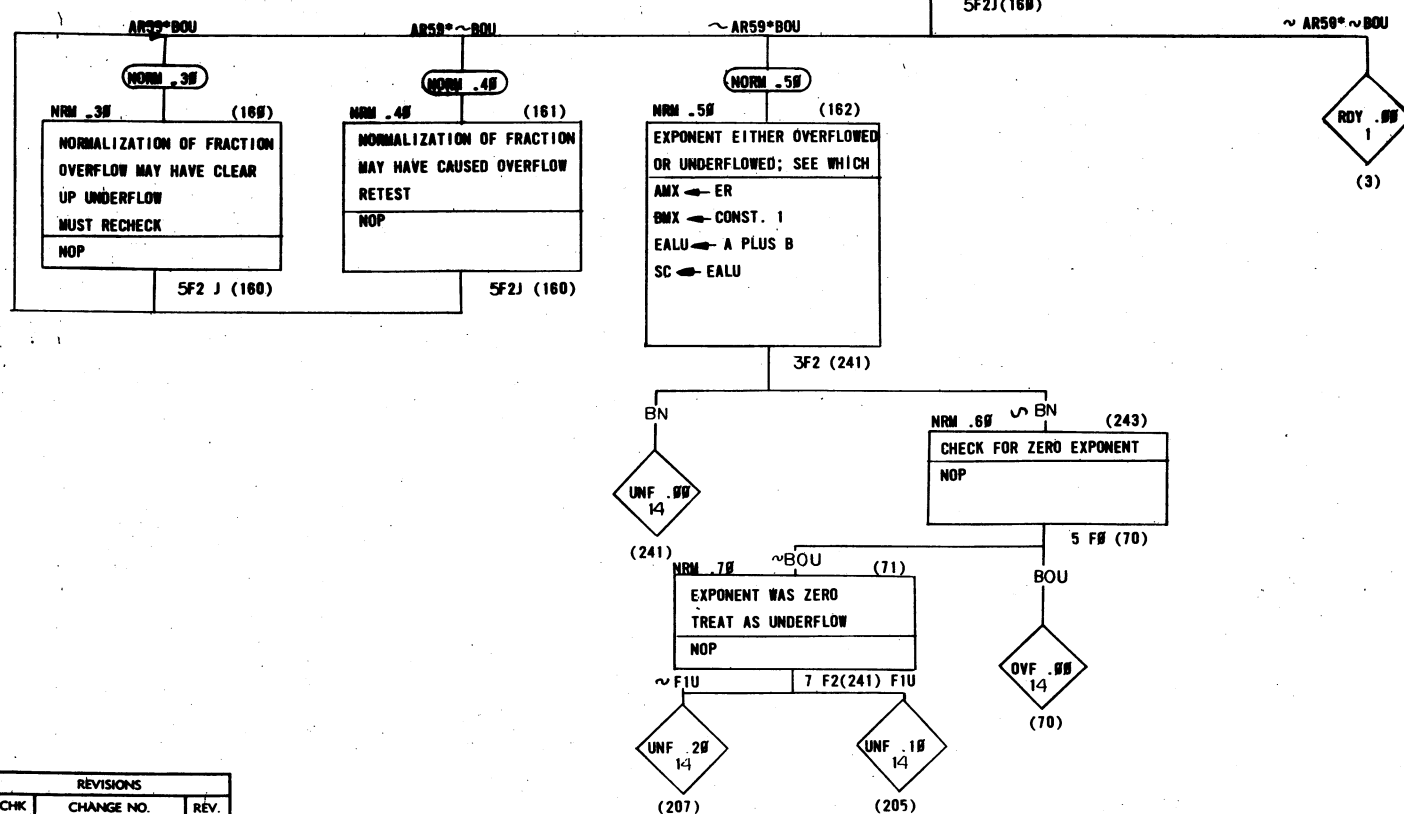
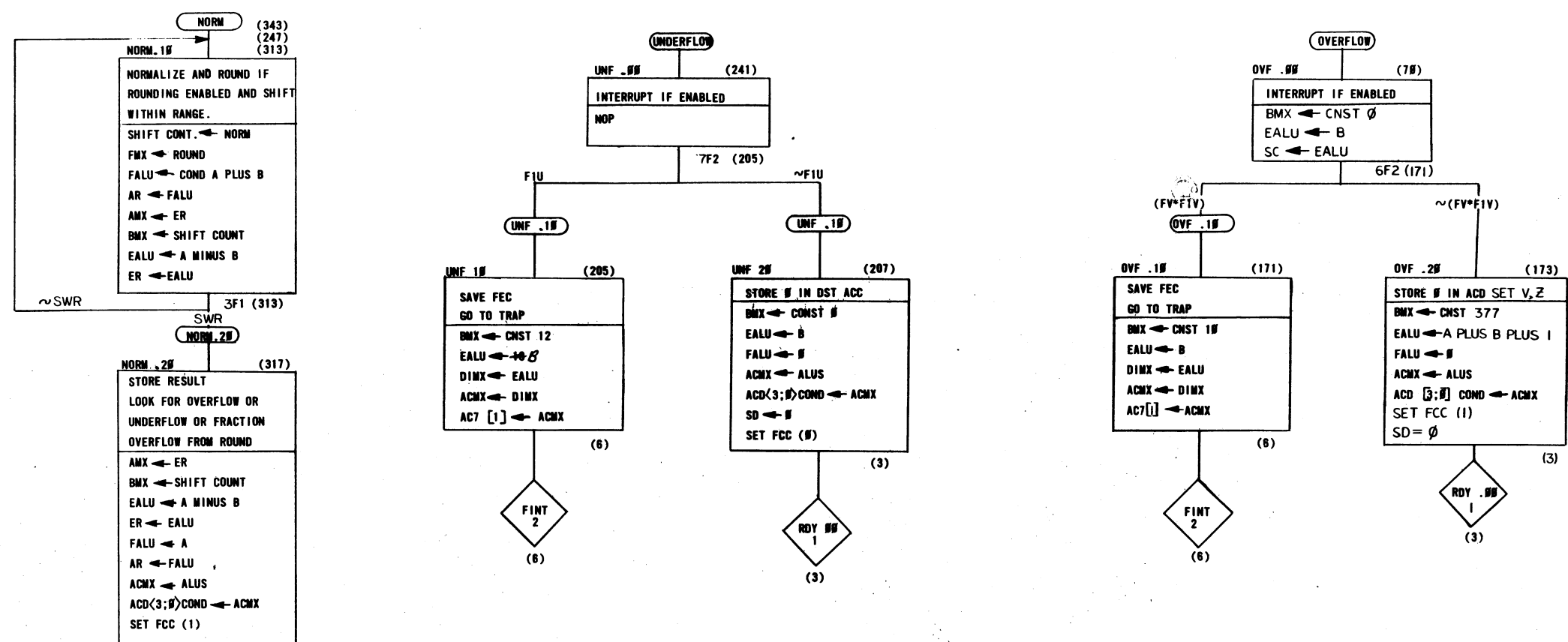
Long cycle needed to figure shift amount for next state. QR is clocked by T53

REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. DRD 138

TITLE FLOW DIAGRAM
 FPII-C (FLOWS 13)
 SCALE // SHEET 14 OF 15
 SIZE CODE D FD NUMBER FPII-C-1
 DIST. REV.

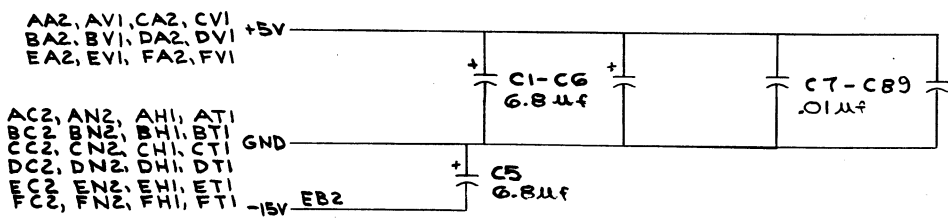
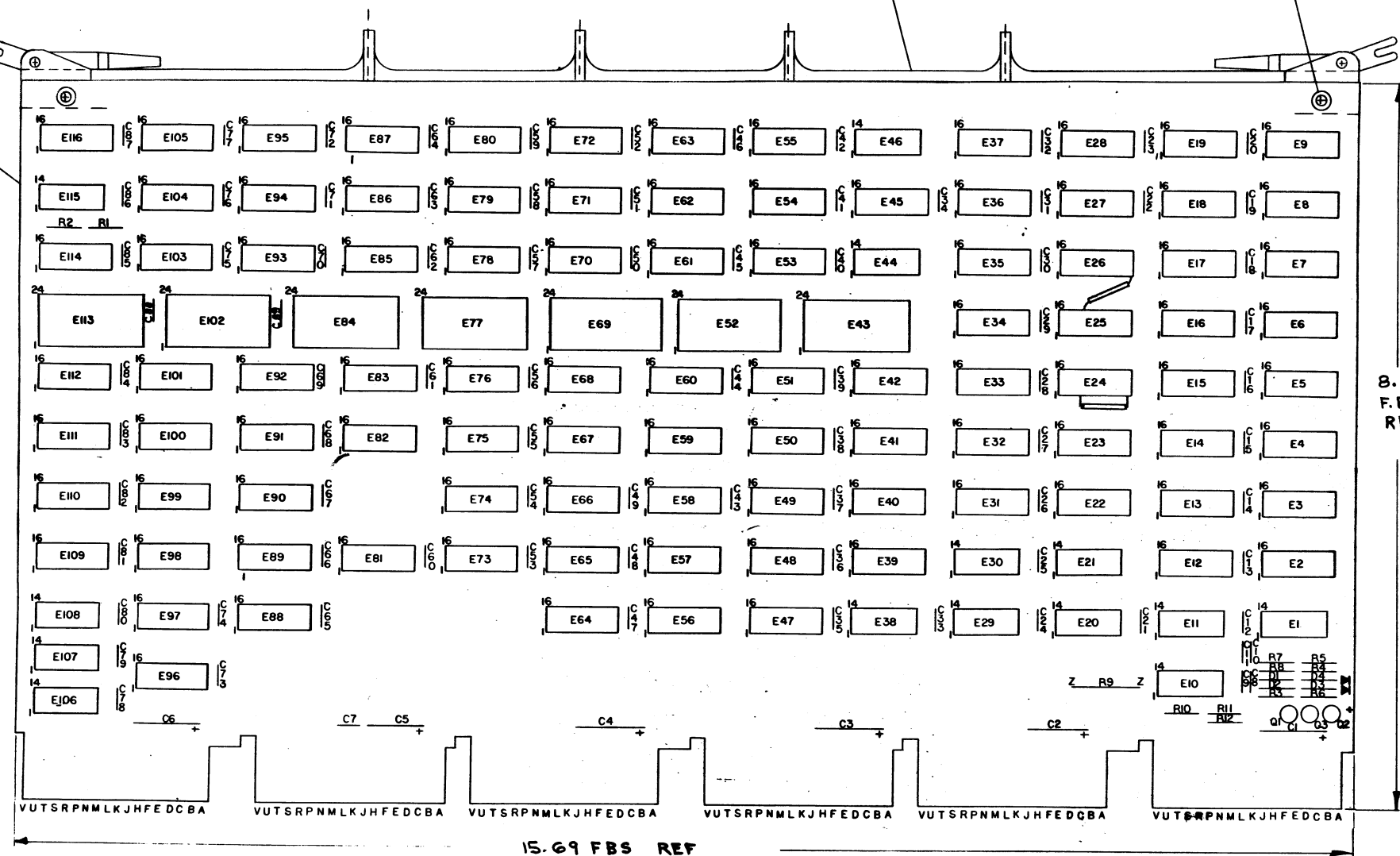
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REVISIONS		
CHK	CHANGE NO.	REV.

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NOTES:



IC TYPE	GND	+5V
IC 74S182	8	16
IC 74S85	8	16
IC 74S175	8	16
IC 74157	8	16
IC 74174	8	16
IC 74S174	8	16
IC 74S158	8	16
IC 74S157	8	16
IC 74S153	8	16
IC 74S181	12	24
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY. EXCEPTIONS ARE STATED ABOVE.

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL
FPII-C

CHK	CHG	REV	DATE

DEC. NO.	EIA NO.	DEC. NO.	EIA NO.

REVISIONS

NO.	DESCRIPTION	DATE
1	INITIAL DESIGN	1/25/75
2	REVISED FOR MANUFACTURE	11/25/75
3	REVISED FOR MANUFACTURE	11/25/75
4	REVISED FOR MANUFACTURE	12/12/75

digital

TITLE: FRACTION PROC HIGH ORDER

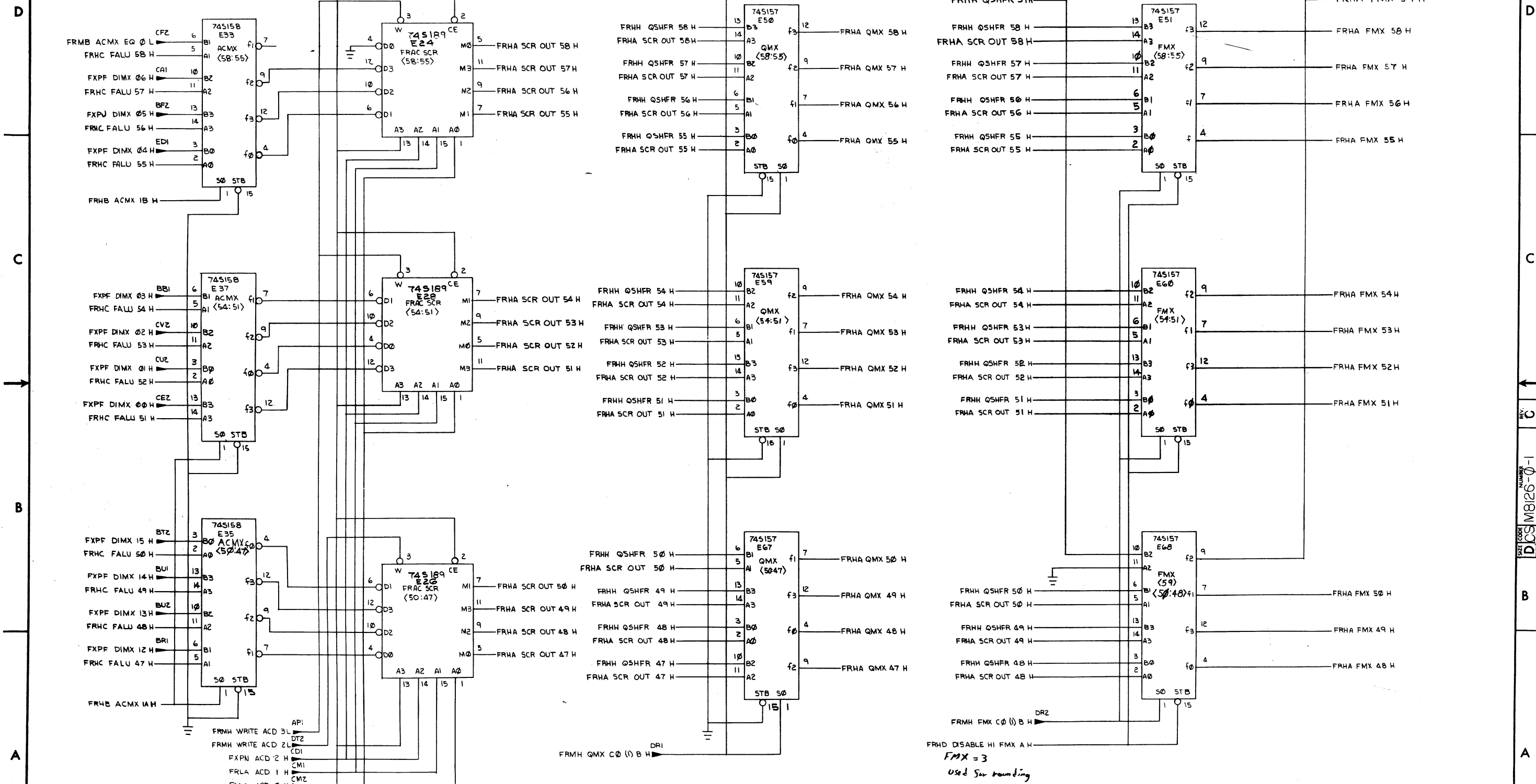
SIZE CODE: DCS M8126-0-1

REV. C

SCALE: 1 OF 13

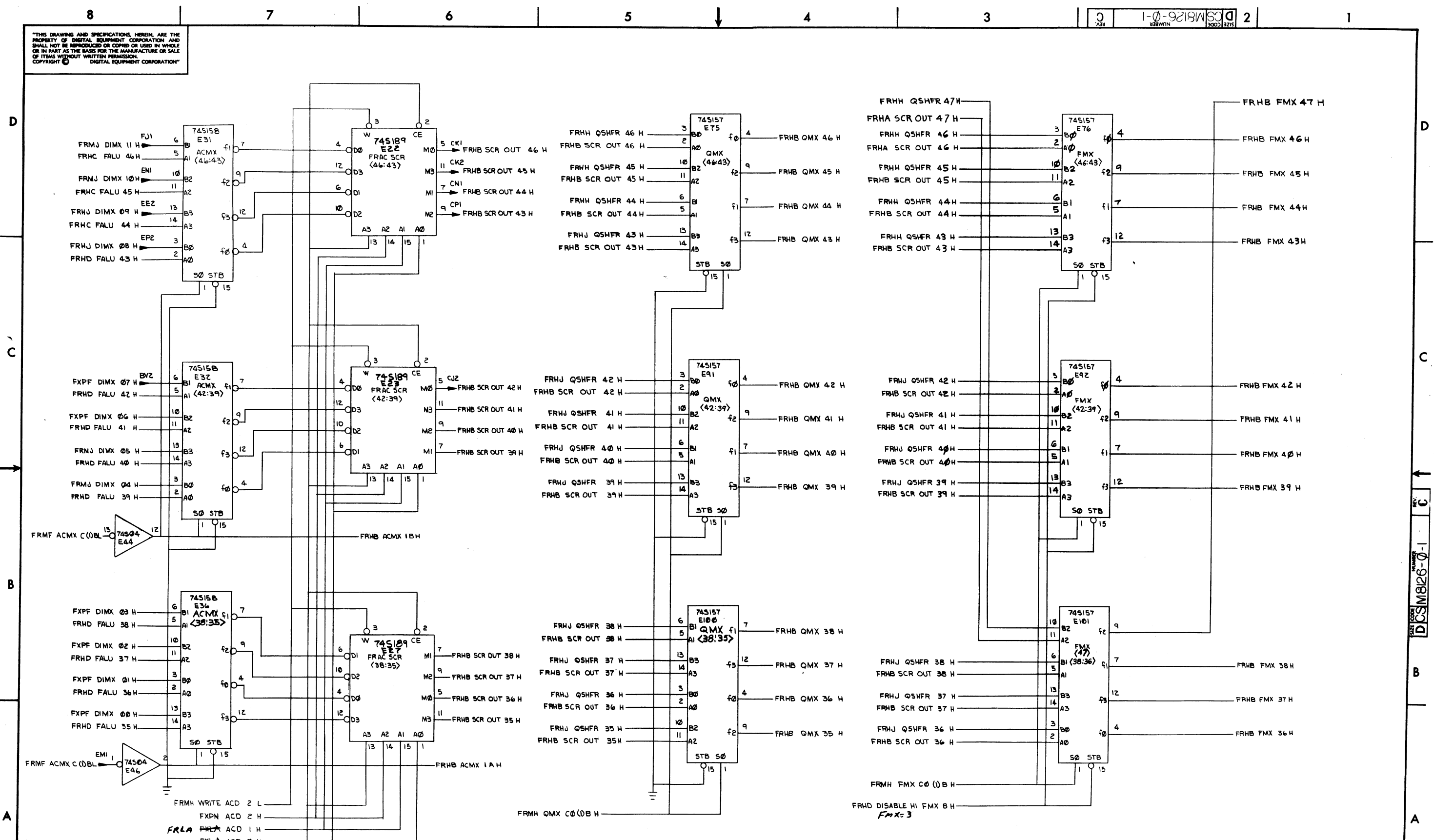
REF	X-Y COORDINATE HOLE LOCATION	K-CO-M8126-B-4	1
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M8126-B-5	2
REF	MODULE ECO HISTORY	B-MH-M8126-B-6	3
1	ETCHED CIRCUIT BOARD	5011870	4
3	C7 THRU C89	1001610-00	5
6	C1 THRU C6	1005306	6
4	D1 THRU D4	1100113	7
1	HANDLE HEX MODULE	1210711-2	8
3	R1, R7, R11	1300295	9
1	R3	1300316	10
3	R2, R8, R12	1301424	11
1	R6	1301477	12
2	R4, R5	1301969	13
1	R9	1300292	14
1	R10	1300294	15
2	Q1, Q2	1503100	16
1	Q3	1505321	17
1	E115	1909712	18
7	E43, E52, E69, E77, E84, E102, E113	1910531	19
3	E1, E11, E30	1910532	20
4	E29, E38, E44, E46	1910534	21
2	E20, E18	1910536	22
3	E21, E106, E107	1910537	23
1	E10	1910544	24
5	E13, E16, E112, E14, E15	1910547	25
17	E2, E7, E17, E50, E51, E59, E60, E67, E68, E75, E76, E82, E83, E91, E92, E100, E101	1910548	26
7	E31 THRU E37	1910549	27
12	E3, E4, E47, E56, E61, E64, E78, E85, E88, E97, E103, E114	1910550	28
1 1/2	#30 AWG. JUMPERS	9105740-55	29
3	E40, E41, E111	1910655	30
3	E5, E6, E53	1910957	31
1	E108	1911712-BB-S	32
1	E12	1912089-BB-S	33
7	E22 THRU E28	1912661	34
2	E42, E45	1912796	35
2	E70, E93	1912097	36
30	E48, E49, E54, E55, E57, E58, E62, E63, E65, E66, E71 THRU E74, E79 THRU E81, E86, E87, E89, E90, E94, E95, E98, E99, E104, E105, E109, E110, E116	1912693	37
1	E39	23009A2	38
1	E96	23006A2	39
12	EYELET	9006732	40

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REVISIONS		
CHK	CHANGE NO.	REV.

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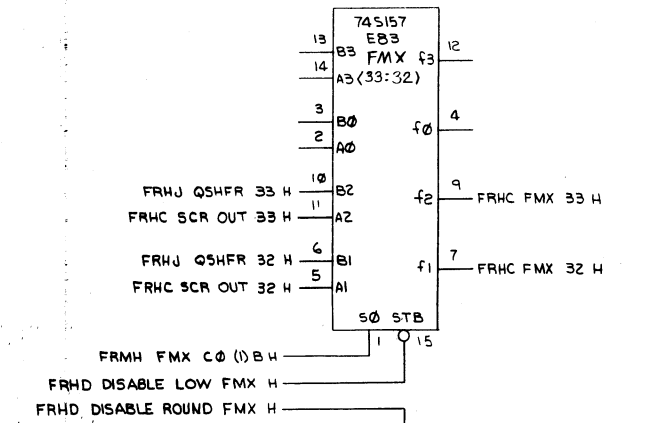
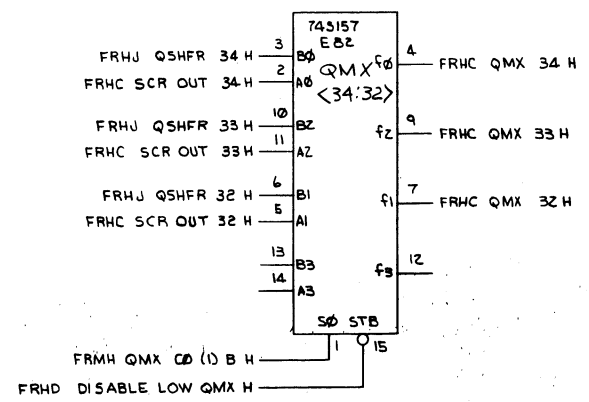
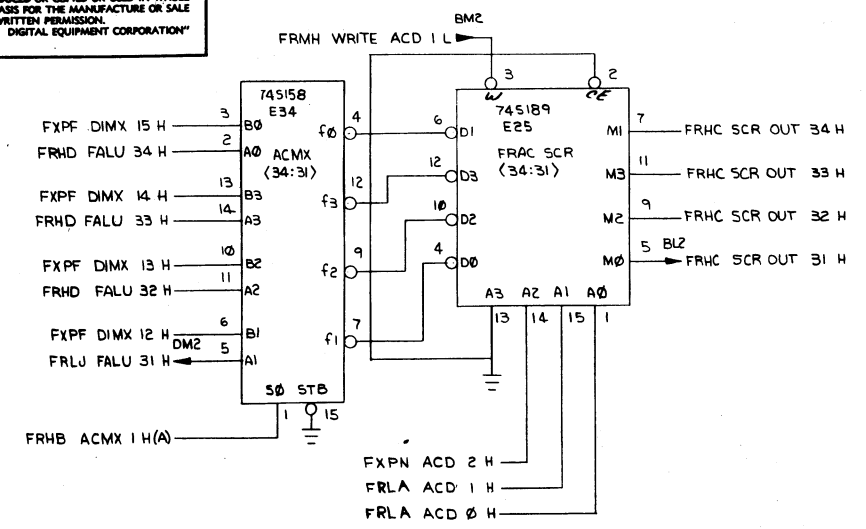


REVISIONS		
CHK	CHANGE NO.	REV.

(SLOT 02)

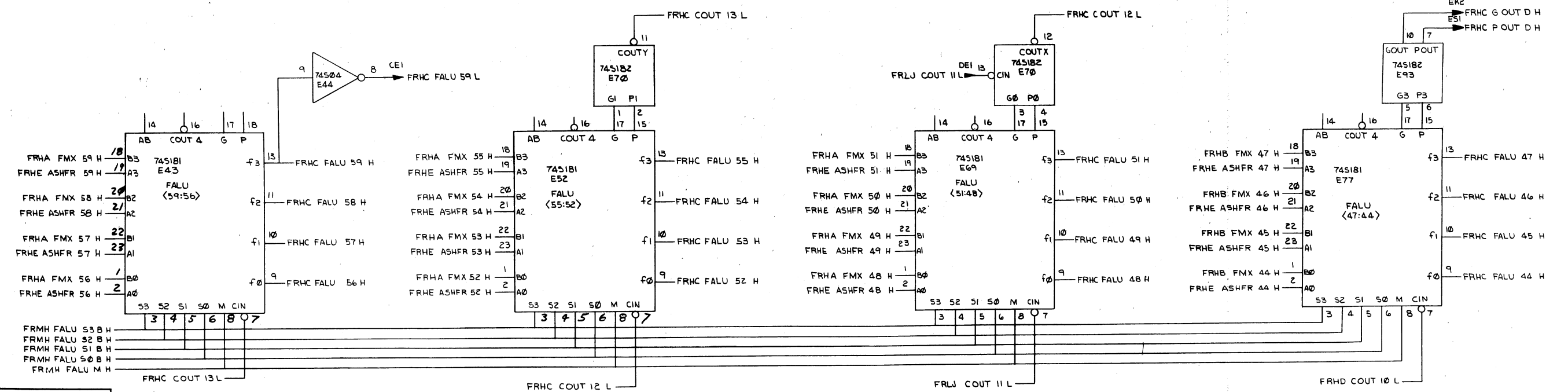
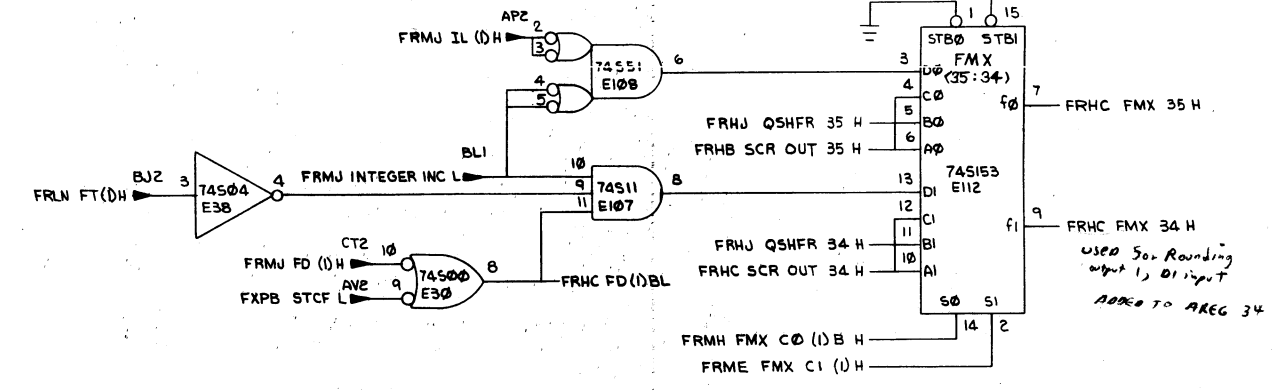
TITLE	FRACTION (FRHB) PROC. HIGH ORDER	SIZE CODE	D	NUMBER	CS M8126-0-1	REV.	C
SCALE	1:1	SHEET	3	OF 13	DIST.		

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FMXC1	FMXC0	FMX FUNCTION
0	0	FMX (59:00) ← SCR OUT (59:00)
0	1	FMX (59:00) ← QSHFR (59:00)
1	0	FMX (59:35) ← SCR OUT (59:35) IF FD(1) FMX(34:00) ← SCR OUT (34:00) ELSE FMX (34:00) ← 0
1	1	FMX (59:30) ← 0; FMX (33:20) (18:0) ← 0; FMX (1:0) ← 0; FMX (34) ← FT(0); FD(0) ← INTEGER INCAL (0); FMX (35) ← INTEGER INCAL (0); FMX (19) ← INTEGER INCAL (1)

QMXC1	QMXC0	QMX FUNCTION
0	0	QMX (59:00) ← SCR OUT (59:00)
0	1	QMX (59:00) ← QSHFR (59:00)
1	0	QMX (59:35) ← SCR OUT (59:35) IF FD(1) QMX (34:00) ← SCR OUT (34:00) ELSE QMX (34:00) ← 0
1	1	QMX (59:00) ← QSHFR (59:00) IF FD(0) QSHFR (31:24) ← QUOT

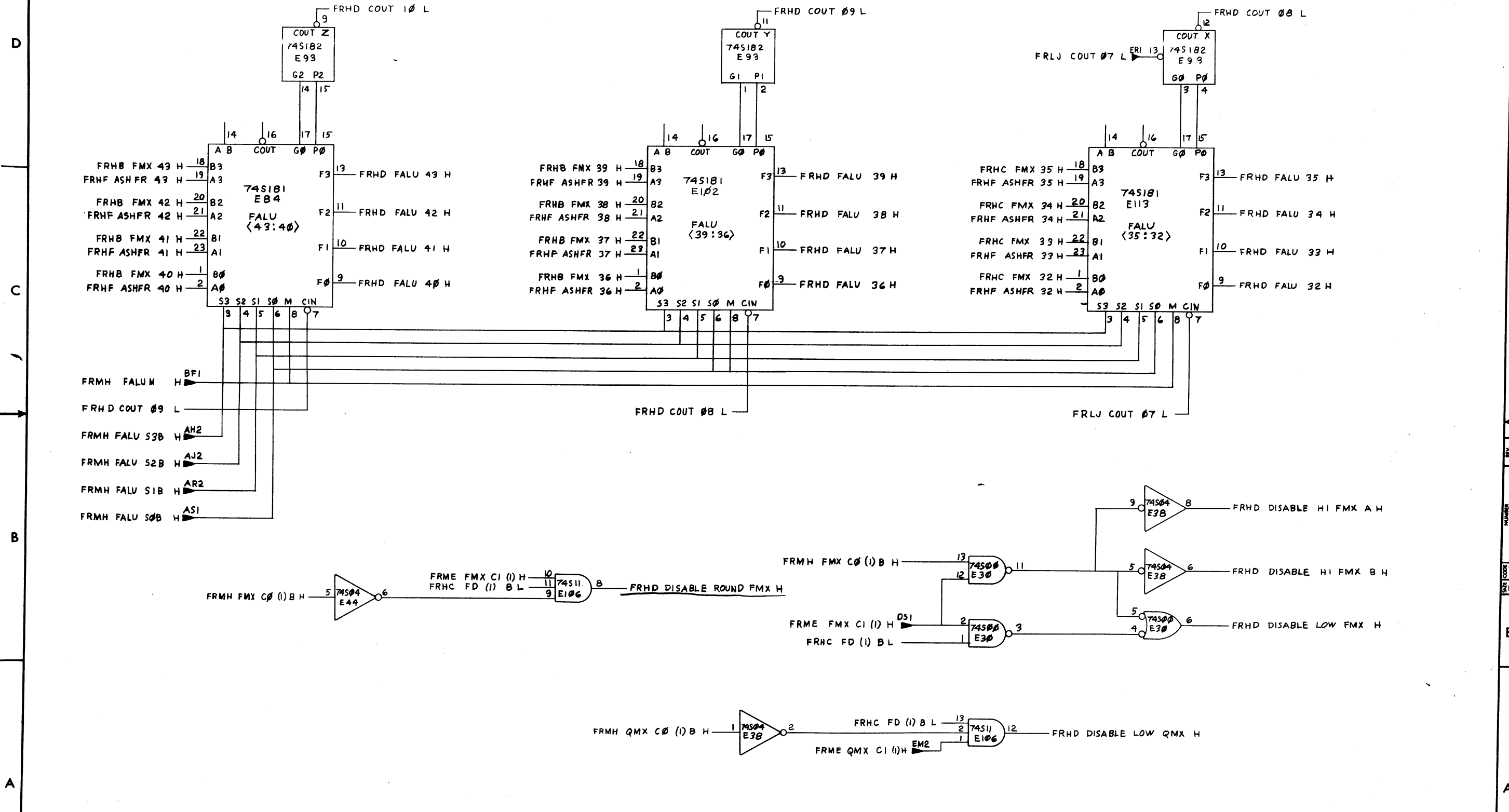


REVISIONS		
CHK	CHANGE NO.	REV.

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D
C
B
A

D
C
B
A



REVISIONS		
CHK	CHANGE NO.	REV.

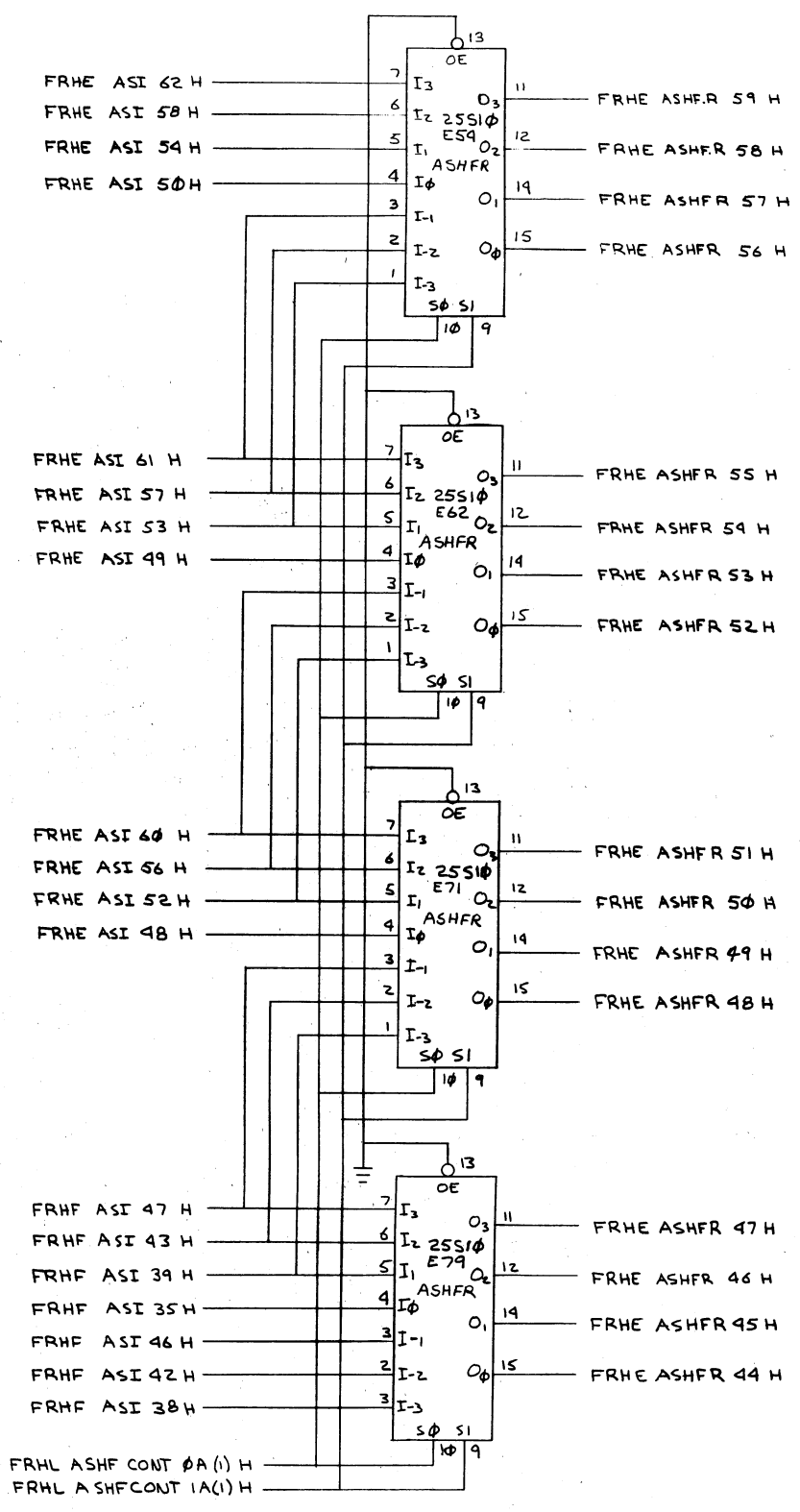
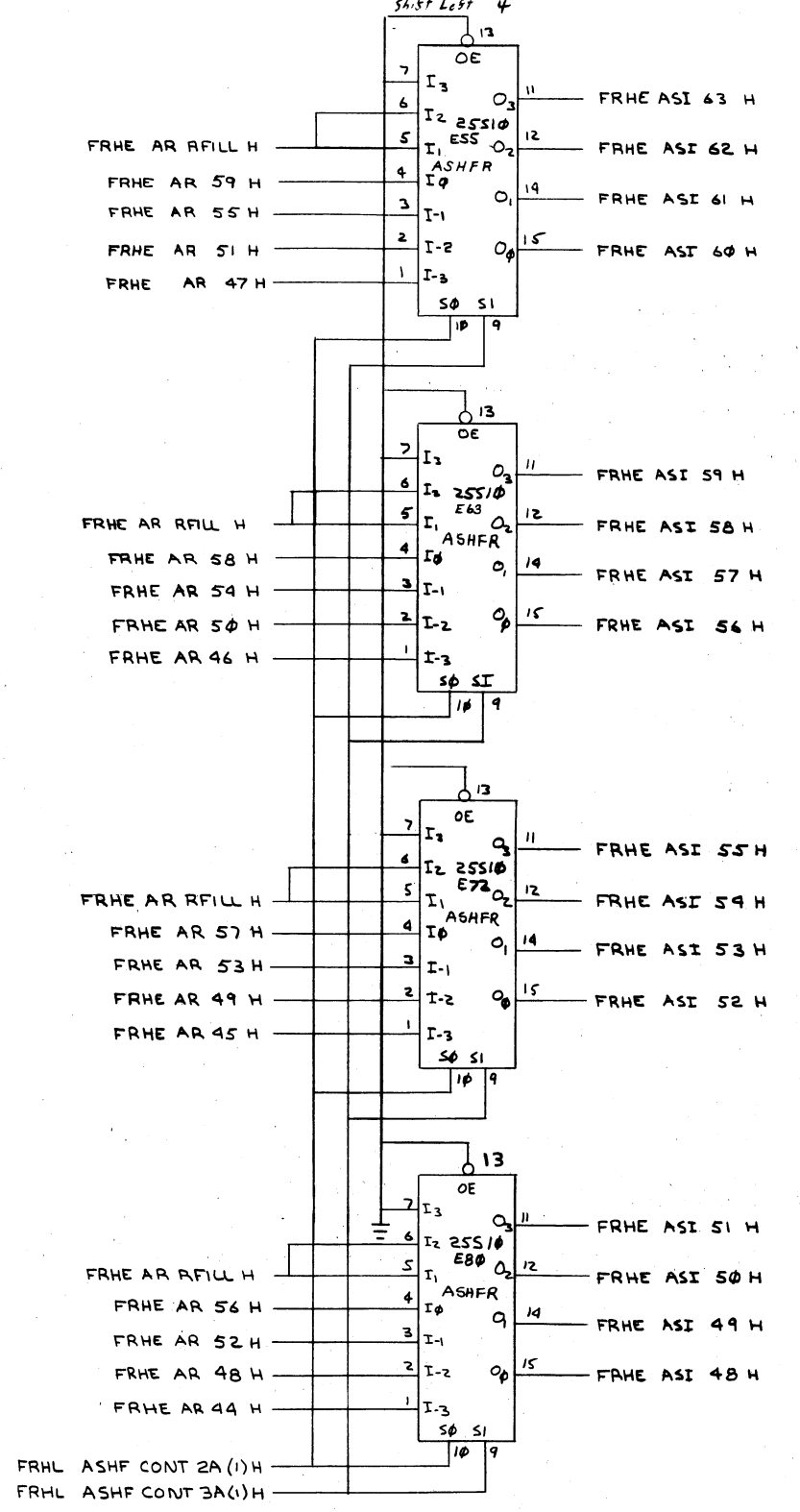
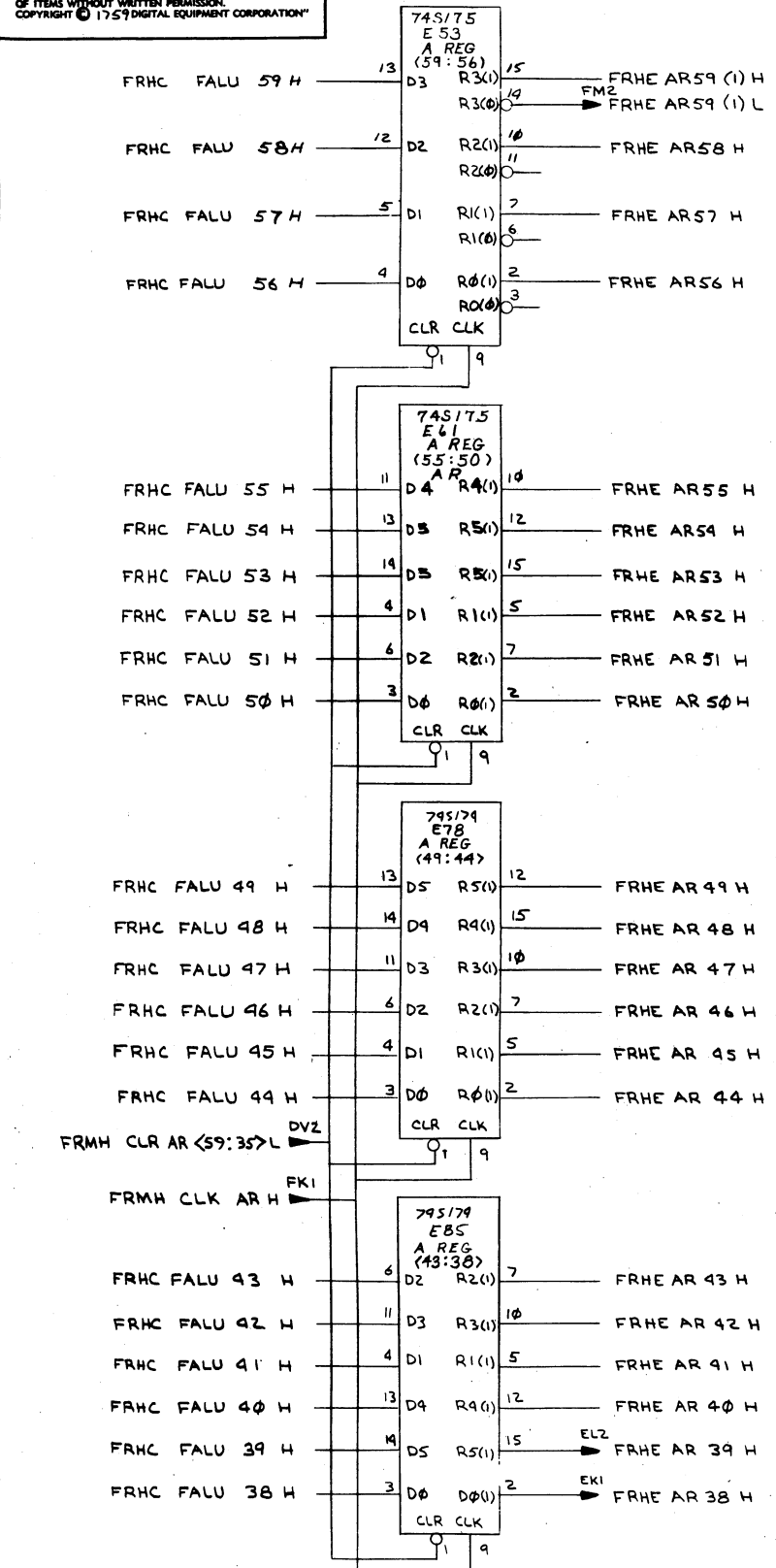
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First level shifting
Shift Right 0,4,8
Shift Left 4

Second level of shifting
Shift Left 0,1,2,3

D
C
B
A

D
C
B
A



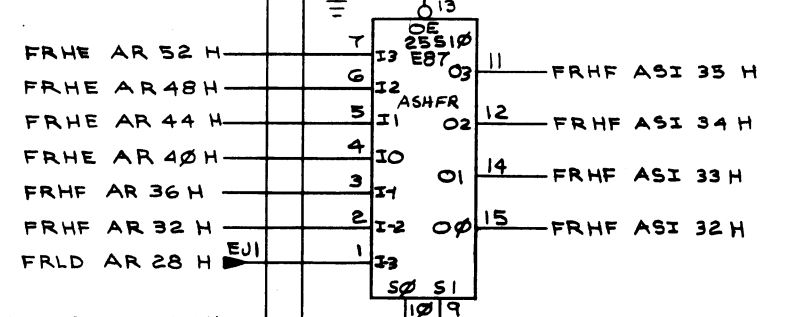
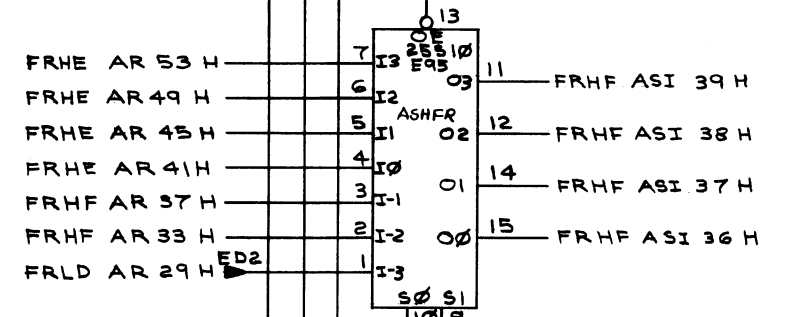
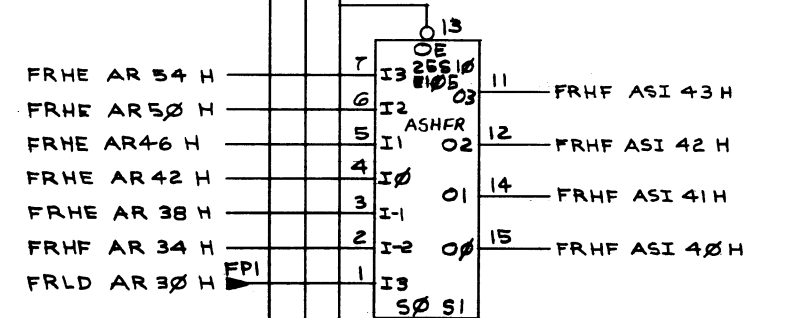
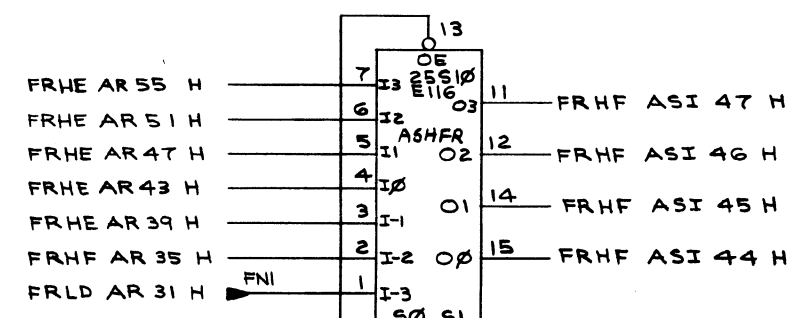
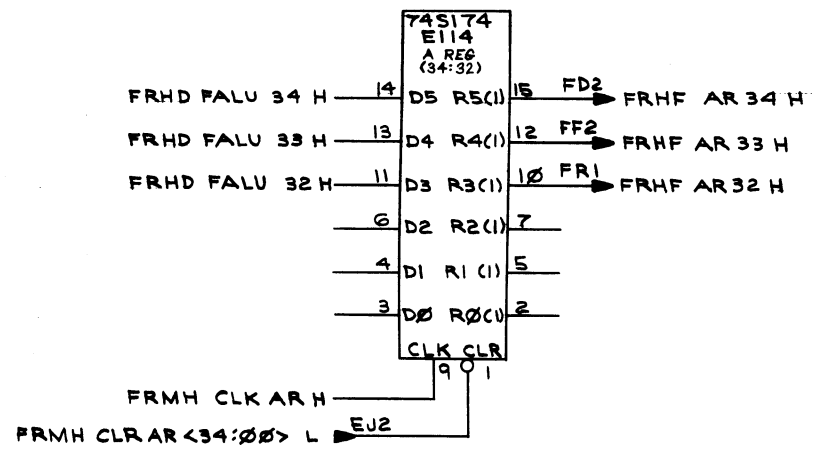
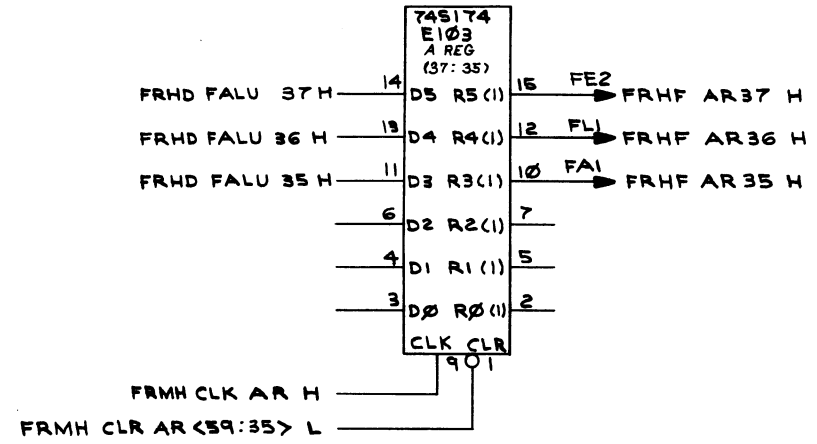
REVISIONS		
CHK	CHANGE NO.	REV.

(SLOT 02) (A REGISTER <59 38> A SHIFTER)
TITLE FRACTION PROC HIGH ORDER (FRHE)
SCALE 1:1 SHEET 6 OF 13
SIZE CODE D NUMBER DC5M8126-0-1 REV. C

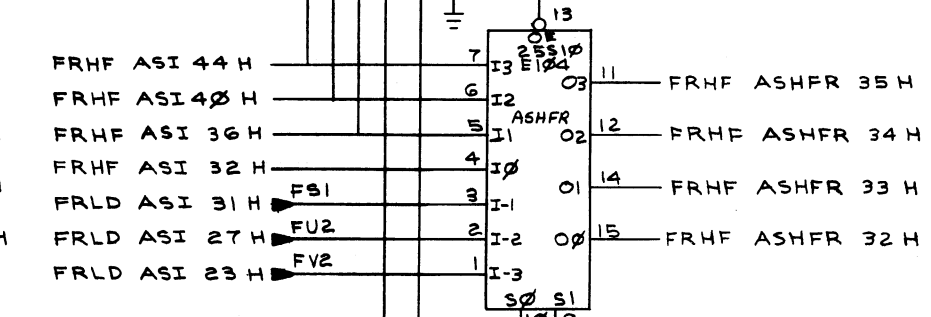
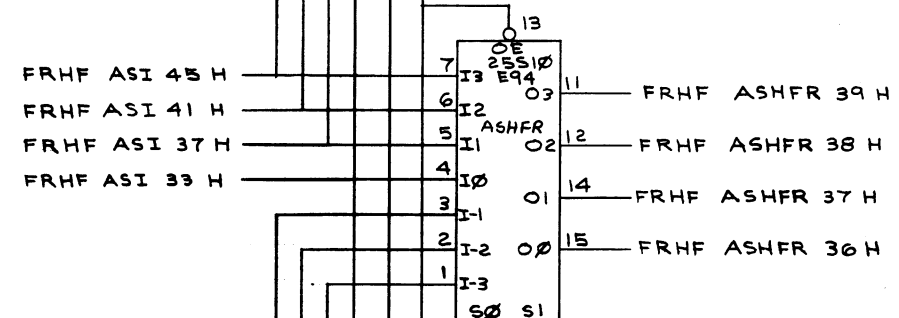
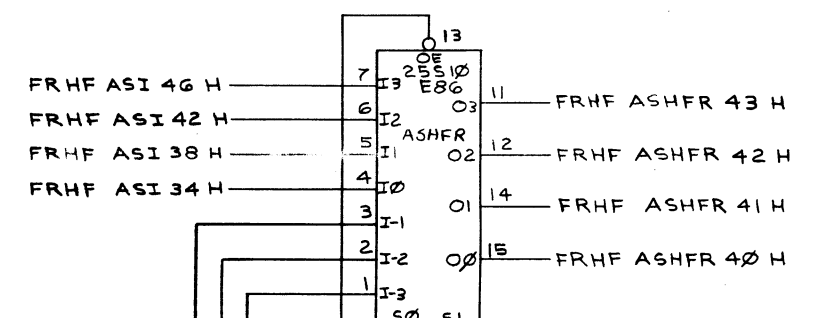
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D
C
B
A

D
C
B
A



FRHL ASHF CONT 2A(1) H
FRHL ASHF CONT 3A(1) H



FRHL ASHF CONT 0A(1) H
FRHL ASHF CONT 1A(1) H

TRUTH TABLE FOR DEC 25510

OE	S1	S0	00	O1	O2	O3
0	0	0	I0	I1	I2	I3
0	0	1	I-1	I0	I1	I2
0	1	0	I-2	I-1	I0	I1
0	1	1	I-3	I-2	I-1	I0
1	X	X	Z	Z	Z	Z

NOTES: X = DON'T CARE
Z = OUTPUT "OFF" I.E. IN HIGH IMPEDANCE STATE

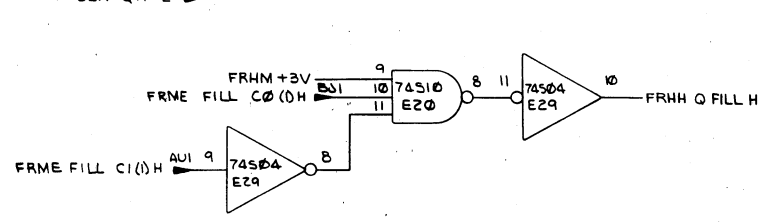
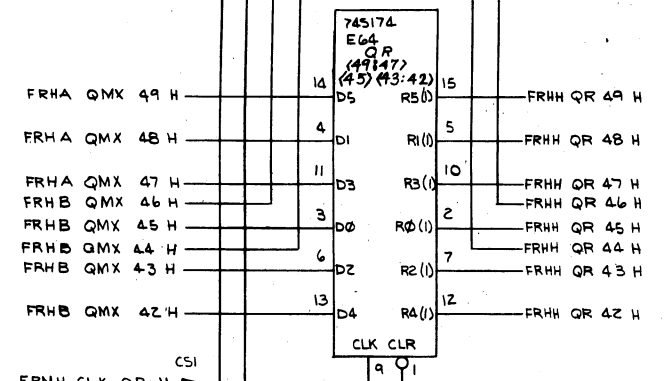
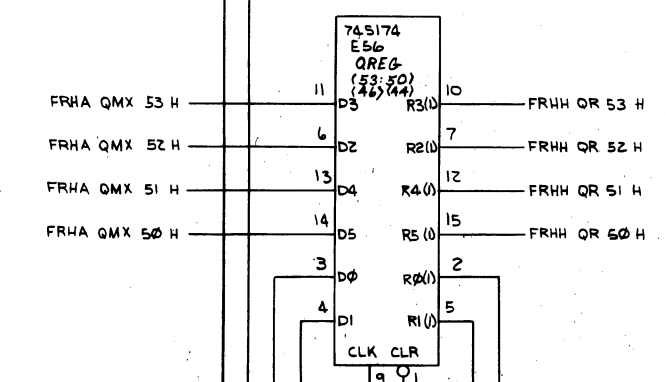
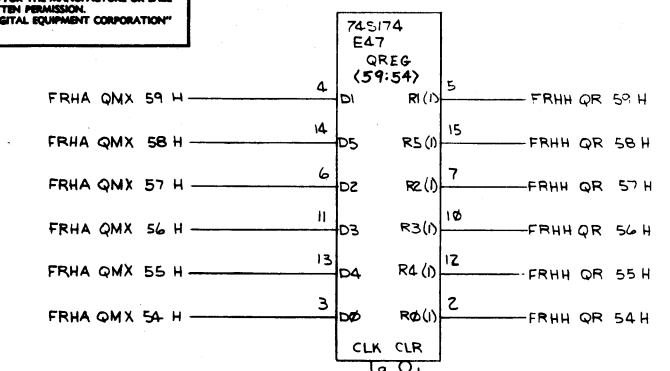
REVISIONS

CHK	CHANGE NO.	REV.

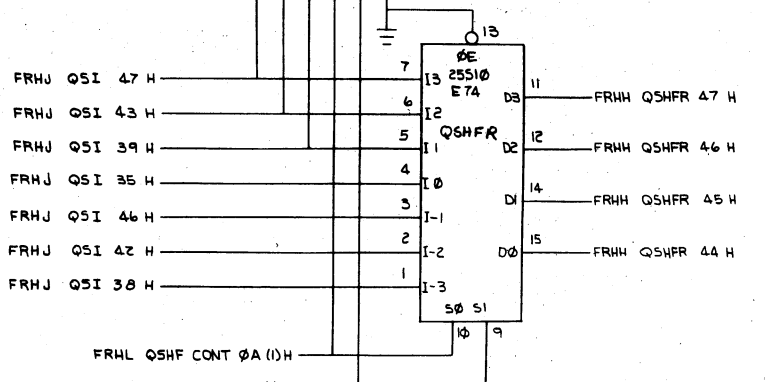
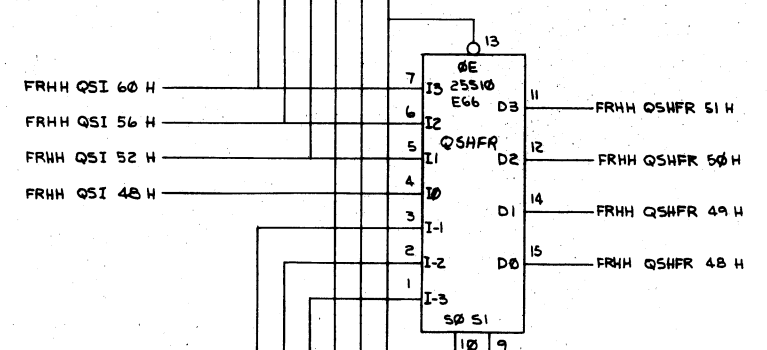
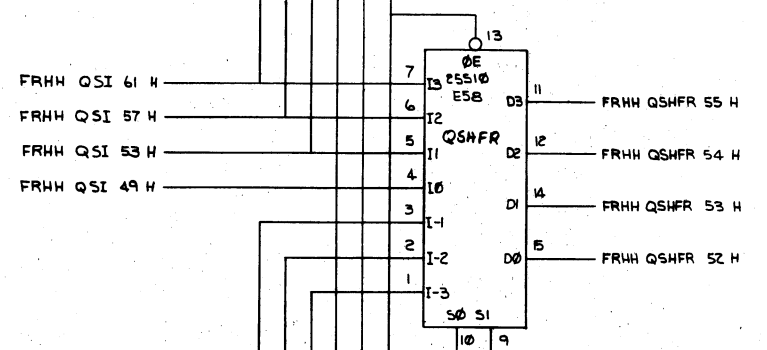
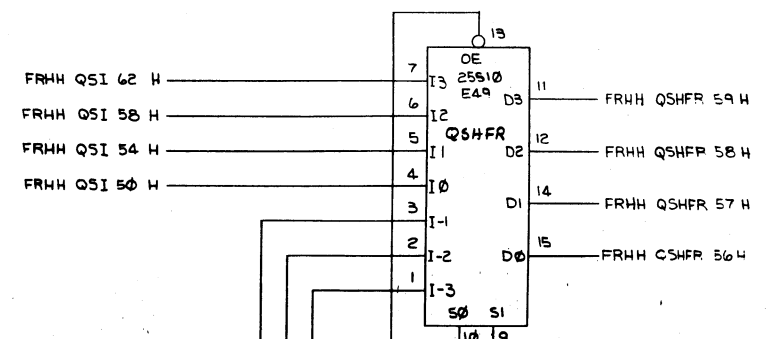
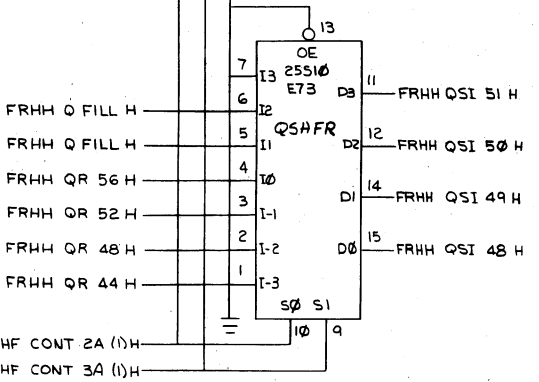
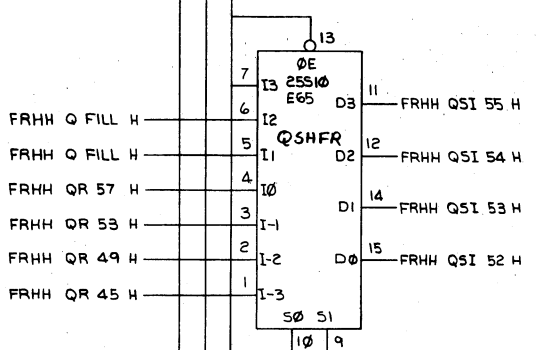
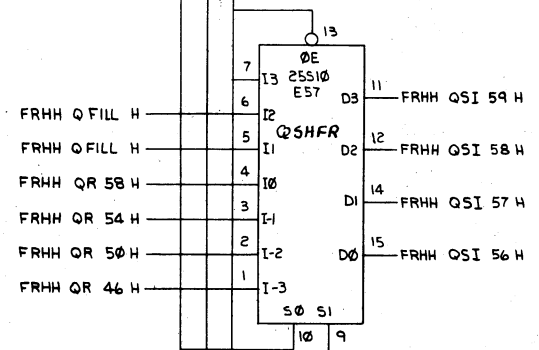
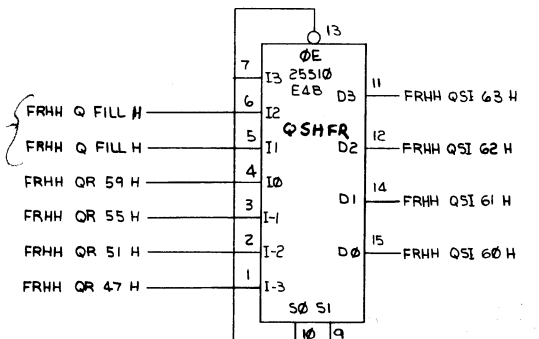
(SLOT 02)

TITLE	(FRHF)	SIZE CODE	NUMBER	REV.
FRACTION PROC. HIGH ORDER	D CS	M8126-0-1	C	
SCALE	SHEET 7 OF 13	DIST.		

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US60 BY
M00 Inst.
STCPE Inst.



FRHL QSHF CONT 2A (1)H
 FRHL QSHF CONT 3A (1)H

FRHL QSHF CONT 0A (1)H
 FRHL QSHF CONT 1A (1)H

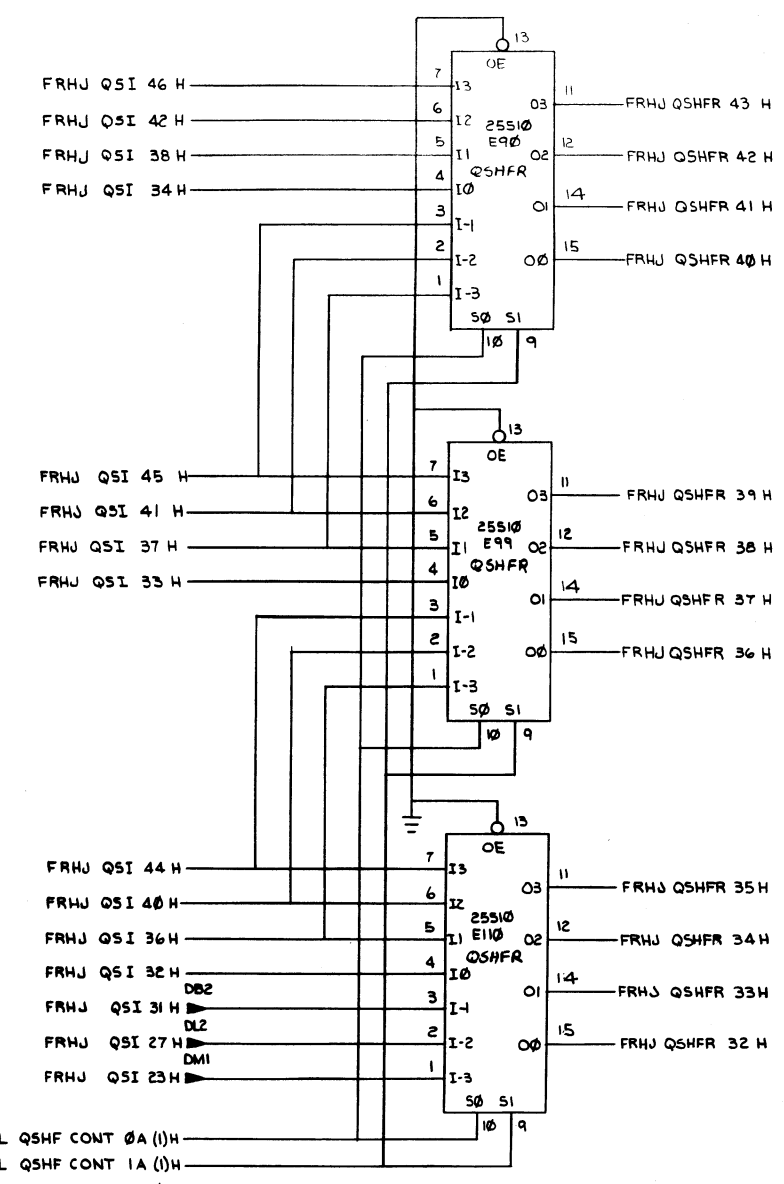
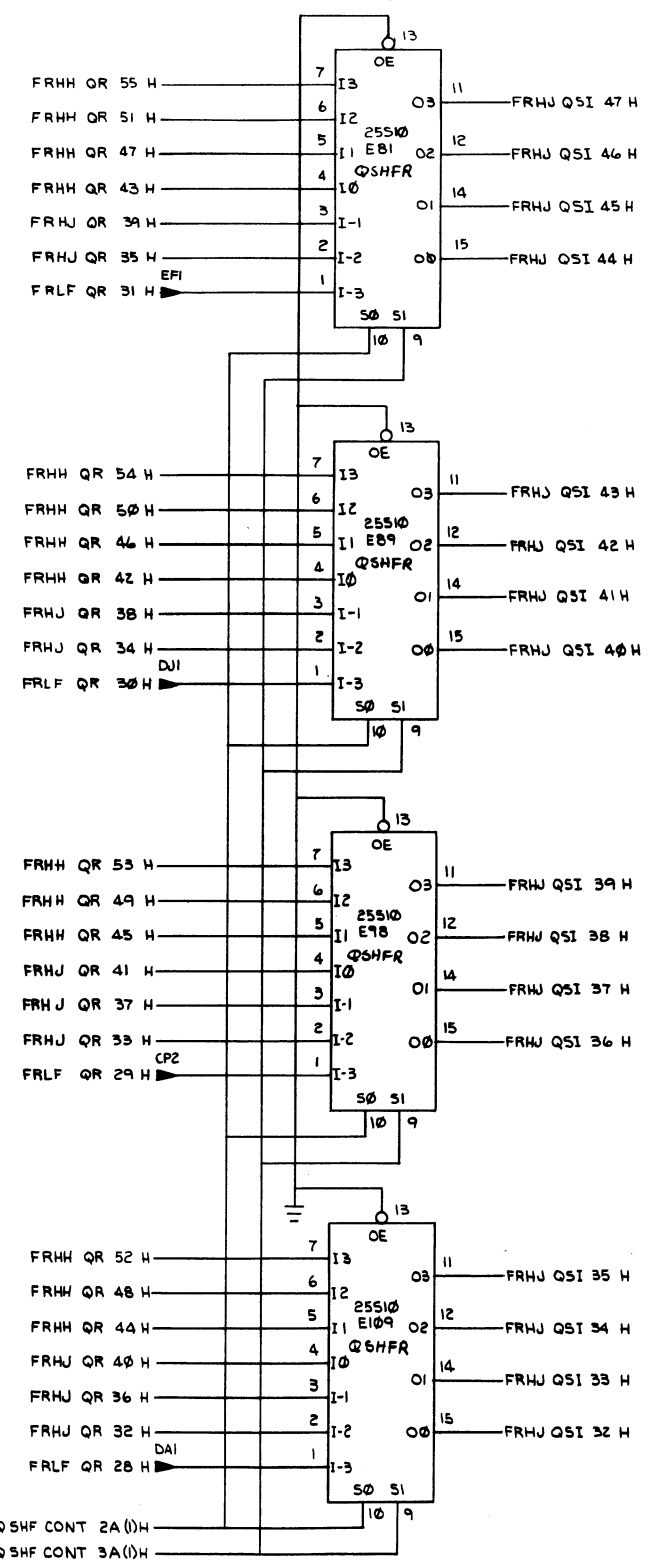
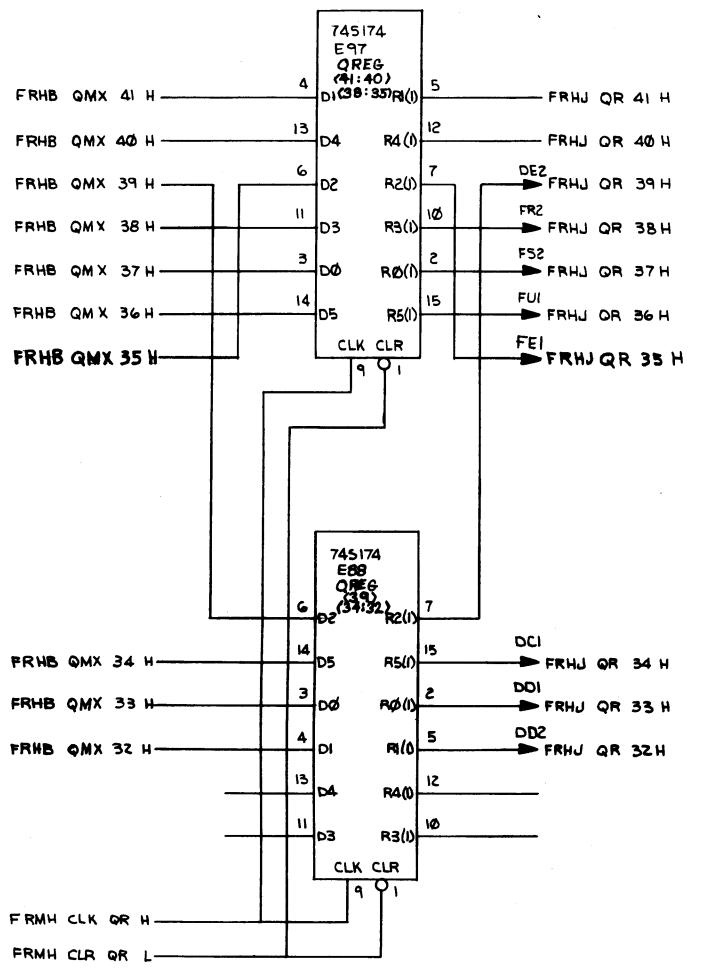
REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. DFD 138

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D
C
B
A

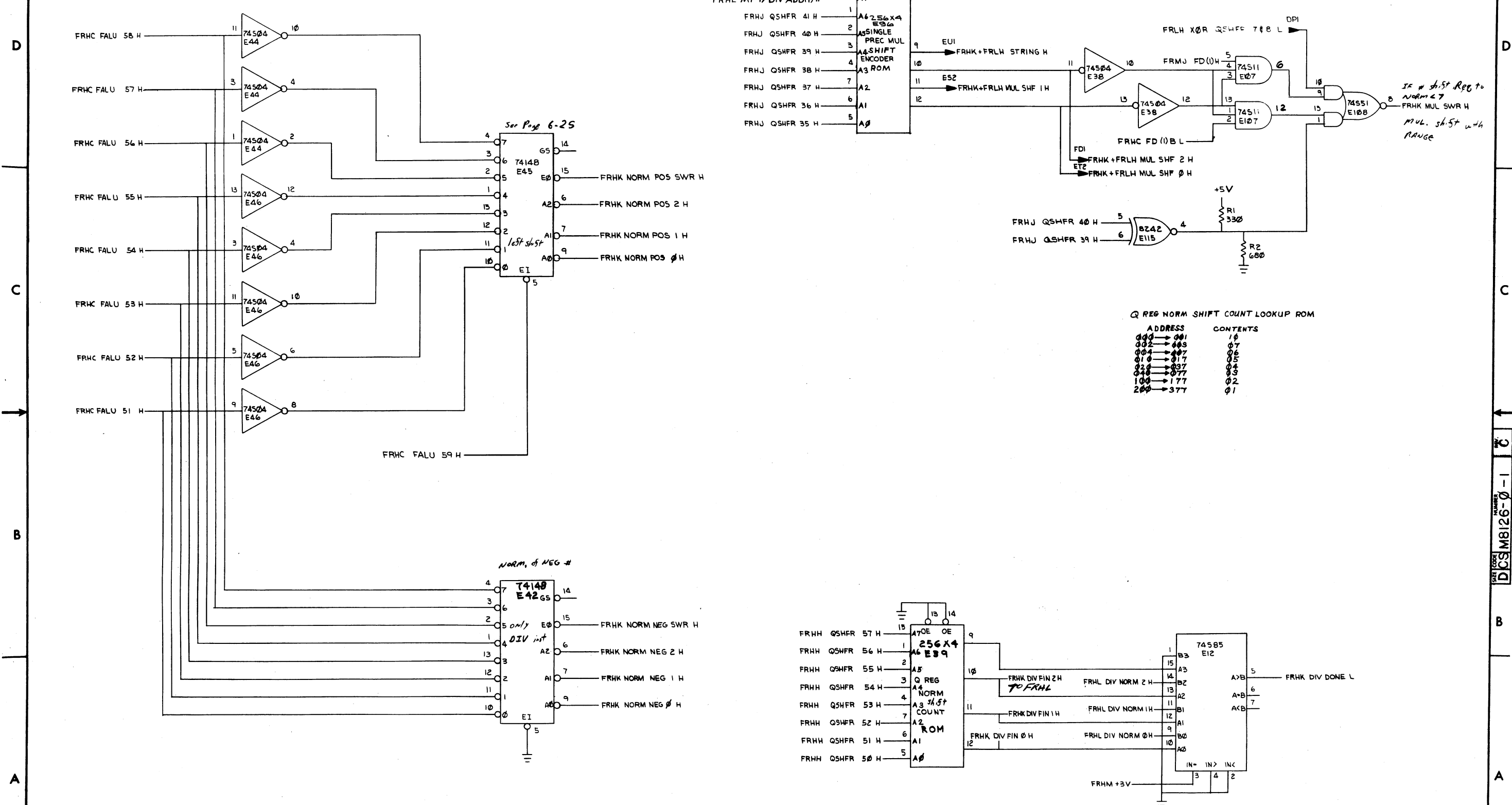
D
C
B
A



A/Q SHF CONT	ASHFR/QSHFR FUNCTION
3 2 1 0	SHIFT RIGHT 8 PLACES
0 0 0 0	" " 7 "
0 0 0 1	" " 6 "
0 0 1 0	" " 5 "
0 0 1 1	" " 4 "
0 1 0 0	" " 3 "
0 1 0 1	" " 2 "
0 1 1 0	" " 1 "
0 1 1 1	NO SHIFT
1 0 0 0	SHIFT LEFT 1 PLACE
1 0 0 1	" " 2 "
1 0 1 0	" " 3 "
1 0 1 1	" " 4 "
1 1 0 0	" " 5 "
1 1 0 1	" " 6 "
1 1 1 0	" " 7 "
1 1 1 1	" " 7 "

REVISIONS		
CHK	CHANGE NO.	REV.

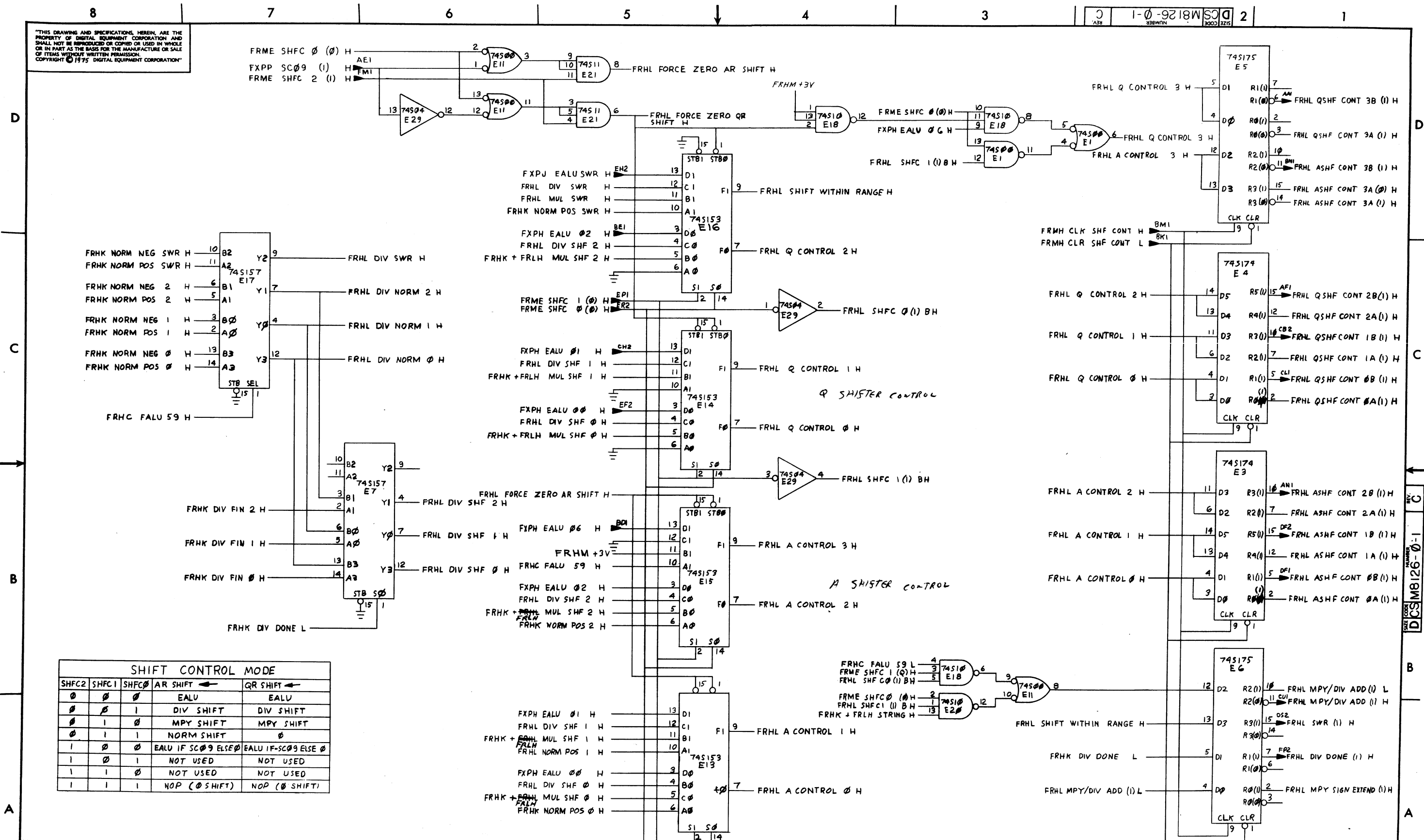
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE		SIZE CODE	NUMBER	REV.
FRACTION PROC HIGH ORDER		DCS M8126-0	10 OF 19	C
SCALE		SHEET	DIST.	

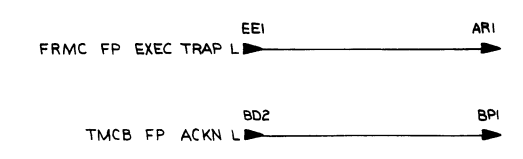
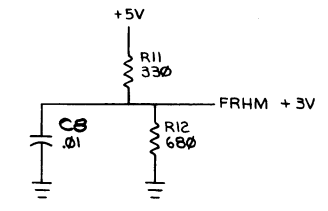
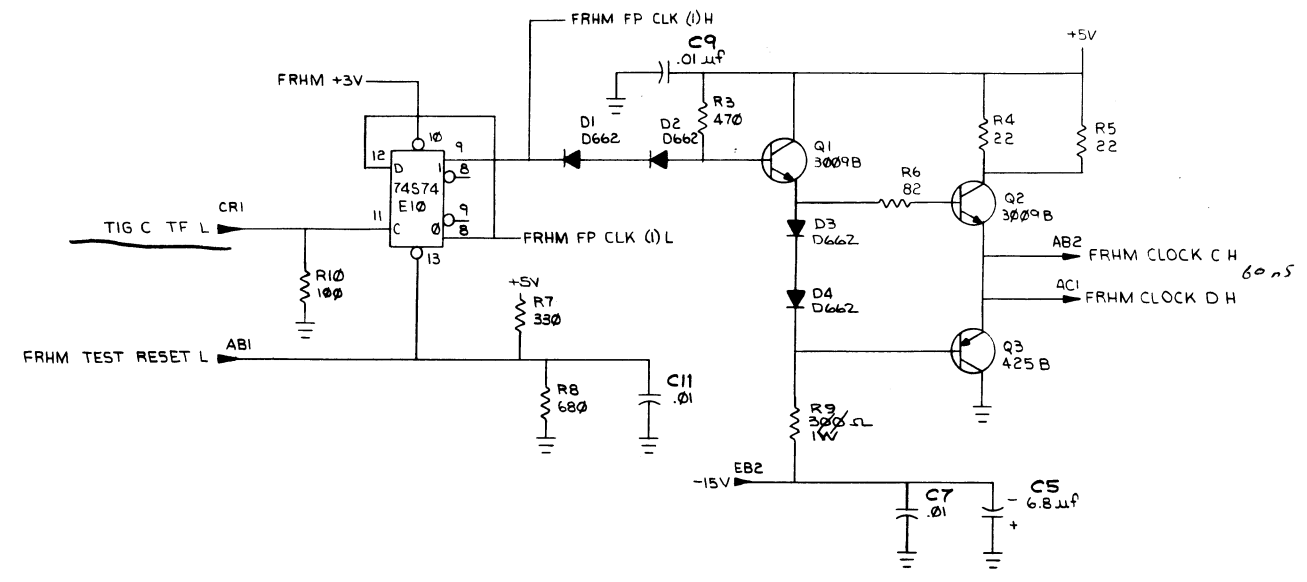
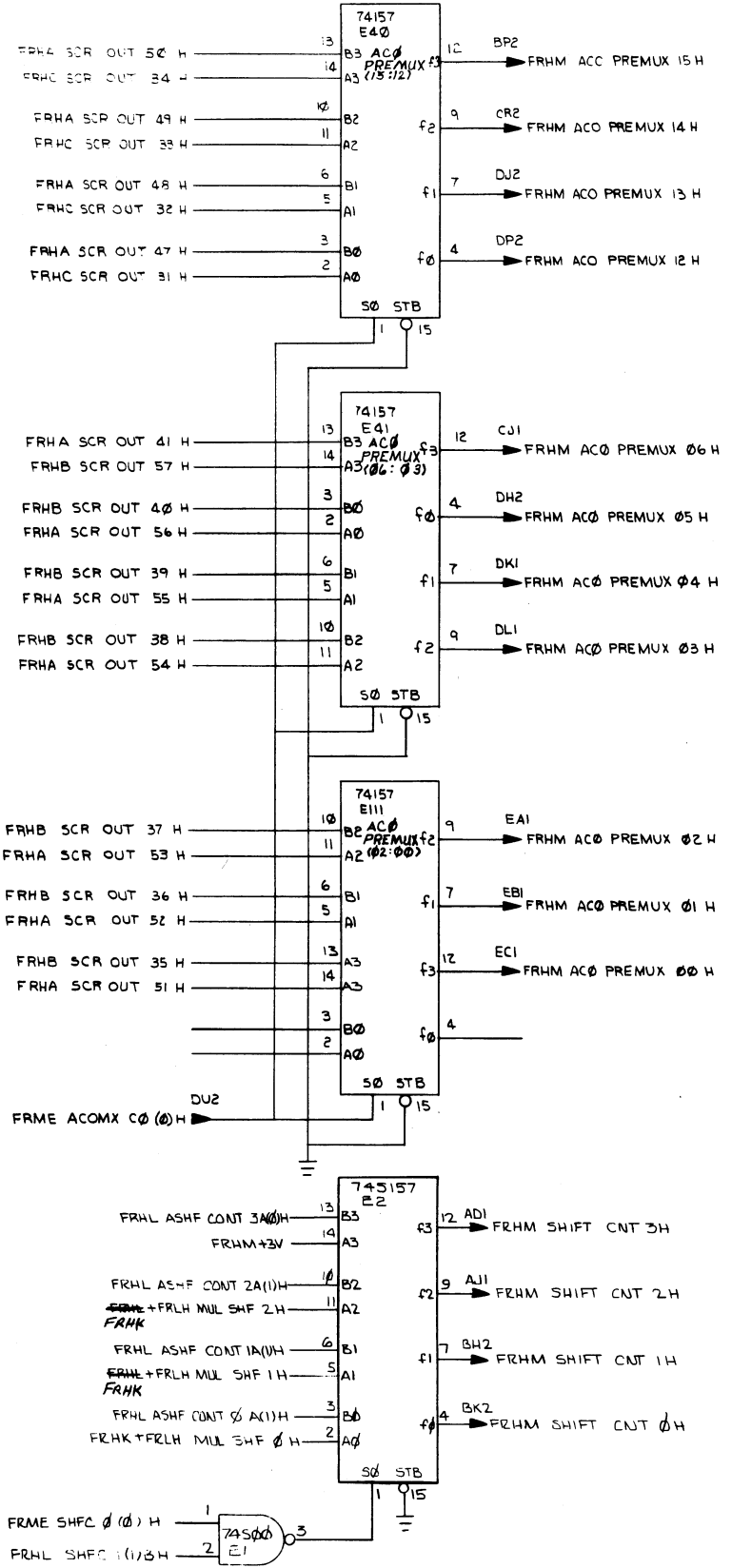
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SHFC2	SHFC1	SHFC0	AR SHIFT	QR SHIFT
0	0	0	EALU	EALU
0	0	1	DIV SHIFT	DIV SHIFT
0	1	0	MPY SHIFT	MPY SHIFT
0	1	1	NORM SHIFT	0
1	0	0	EALU IF SC09 ELSE 0	EALU IF-SC09 ELSE 0
1	0	1	NOT USED	NOT USED
1	1	0	NOT USED	NOT USED
1	1	1	NOP (0 SHIFT)	NOP (0 SHIFT)

CHK	CHANGE NO.	REV.

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SHIFT COUNT MUX FUNCTION

SHFC1	SHFC0	Function
0	0	FRHM SHIFT CNT (3:0) ← FRHL ASHF CONT (3:0)
0	1	FRHM SHIFT CNT (3:0) ← FRHK + FRLH MUL SHF (3:0)
1	1	FRHM SHIFT CNT (3:0) ← FRHL ASHF CONT (3:0)

REVISIONS		
CHK	CHANGE NO.	REV.

(SLOT 02)

TITLE	(FRHM)	SIZE CODE	NUMBER	REV.
FRACTION PROC. HIGH ORDER	DCS	M8126-0-1	C	
SCALE	+	SHEET 12 OF 13	DIST.	

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MULTIPLY CONTROL LOOKUP ROM

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
000	07	1	ADD
001	06	2	ADD
002	17	1	SUB
003	05	3	ADD
004	07	1	ADD
005	16	2	SUB
006	17	1	SUB
007	04	4	ADD
010	07	1	ADD
011	06	2	ADD
012	17	1	SUB
013	15	3	SUB
014	07	1	ADD
015	16	2	SUB
016	17	1	SUB
017	03	5	ADD
020	07	1	ADD
021	06	2	ADD
022	17	1	SUB
023	15	3	SUB
024	07	1	ADD
025	16	2	SUB
026	17	1	SUB
027	14	4	SUB
030	07	1	ADD
031	06	2	ADD
032	17	1	SUB
033	15	3	SUB
034	07	1	ADD
035	16	2	SUB
036	17	1	SUB
037	02	6	ADD
040	07	1	ADD
041	06	2	ADD
042	17	1	SUB
043	05	3	ADD
044	07	1	ADD
045	16	2	SUB
046	17	1	SUB
047	04	4	ADD
050	07	1	ADD
052	17	1	SUB
053	15	3	SUB
054	07	1	ADD
055	16	2	SUB
056	17	1	SUB
057	13	5	SUB
060	07	1	ADD
061	06	2	ADD
062	17	1	SUB
063	05	3	ADD
064	07	1	ADD
065	16	2	SUB
066	17	1	SUB
067	14	4	SUB
070	07	1	ADD
071	06	2	ADD
072	17	1	SUB
073	15	3	SUB
074	07	1	ADD
075	16	2	SUB
076	17	1	SUB
077	12	6	SUB

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
100	07	1	ADD
101	06	2	ADD
102	17	1	SUB
103	05	3	ADD
104	07	1	ADD
105	16	2	SUB
106	17	1	SUB
107	04	4	ADD
110	07	1	ADD
111	06	2	ADD
112	17	1	SUB
113	15	3	SUB
114	07	1	ADD
115	16	2	SUB
116	17	1	SUB
117	03	5	ADD
120	07	1	ADD
121	06	2	ADD
122	17	1	SUB
123	05	3	ADD
124	07	1	ADD
125	16	2	SUB
126	17	1	SUB
127	14	4	SUB
130	07	1	ADD
131	06	2	ADD
132	17	1	SUB
133	15	3	SUB
134	07	1	ADD
135	16	2	SUB
136	17	1	SUB
137	12	6	ADD
140	07	1	ADD
141	06	2	ADD
142	17	1	SUB
143	05	3	ADD
144	07	1	ADD
145	16	2	SUB
146	17	1	SUB
147	04	4	ADD
150	07	1	ADD
151	06	2	ADD
152	17	1	SUB
153	15	3	SUB
154	07	1	ADD
155	16	2	SUB
156	17	1	SUB
157	13	5	SUB
160	07	1	ADD
161	06	2	ADD
162	17	1	SUB
163	05	3	ADD
164	07	1	ADD
165	16	2	SUB
166	17	1	SUB
167	14	4	SUB
170	07	1	ADD
171	06	2	ADD
172	17	1	SUB
173	15	3	SUB
174	07	1	ADD
175	16	2	SUB
176	17	1	SUB
177	12	6	SUB

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
200	02	6	ADD
201	07	1	ADD
202	06	2	ADD
203	17	1	SUB
204	05	3	ADD
205	07	1	ADD
206	16	2	SUB
207	17	1	SUB
210	04	4	ADD
211	07	1	ADD
212	06	2	ADD
213	17	1	SUB
214	15	3	SUB
215	07	1	ADD
216	16	2	SUB
217	17	1	SUB
220	03	5	ADD
221	07	1	ADD
222	06	2	ADD
223	17	1	SUB
224	05	3	ADD
225	07	1	ADD
226	16	2	SUB
227	17	1	SUB
230	14	4	SUB
231	07	1	ADD
232	06	2	ADD
233	17	1	SUB
234	15	3	SUB
235	07	1	ADD
236	16	2	SUB
237	17	1	SUB
240	02	6	ADD
241	07	1	ADD
242	06	2	ADD
243	17	1	SUB
244	05	3	ADD
245	07	1	ADD
246	16	2	SUB
247	17	1	SUB
250	04	4	ADD
251	07	1	ADD
252	06	2	ADD
253	17	1	SUB
254	15	3	SUB
255	07	1	ADD
256	16	2	SUB
257	17	1	SUB
260	13	5	SUB
261	07	1	ADD
262	06	2	ADD
263	17	1	SUB
264	05	3	ADD
265	07	1	ADD
266	16	2	SUB
267	17	1	SUB
270	14	4	SUB
271	07	1	ADD
272	06	2	ADD
273	17	1	SUB
274	15	3	SUB
275	07	1	ADD
276	16	2	SUB
277	17	1	SUB

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
300	02	6	ADD
301	07	1	ADD
302	06	2	ADD
303	17	1	SUB
304	05	3	ADD
305	07	1	ADD
306	16	2	SUB
307	17	1	SUB
310	04	4	ADD
311	07	1	ADD
312	06	2	ADD
313	17	1	SUB
314	15	3	SUB
315	07	1	ADD
316	16	2	SUB
317	17	1	SUB
320	03	5	ADD
321	07	1	ADD
322	06	2	ADD
323	17	1	SUB
324	05	3	ADD
325	07	1	ADD
326	16	2	SUB
327	17	1	SUB
330	14	4	SUB
331	07	1	ADD
332	06	2	ADD
333	17	1	SUB
334	15	3	SUB
335	07	1	ADD
336	16	2	SUB
337	17	1	SUB
340	02	6	ADD
341	07	1	ADD
342	06	2	ADD
343	17	1	SUB
344	05	3	ADD
345	07	1	ADD
346	16	2	SUB
347	17	1	SUB
350	04	4	ADD
351	07	1	ADD
352	06	2	ADD
353	17	1	SUB
354	15	3	SUB
355	07	1	ADD
356	16	2	SUB
357	17	1	SUB
360	13	5	SUB
361	07	1	ADD
362	06	2	ADD
363	17	1	SUB
364	05	3	ADD
365	07	1	ADD
366	16	2	SUB
367	17	1	SUB
370	14	4	SUB
371	07	1	ADD
372	06	2	ADD
373	17	1	SUB
374	15	3	SUB
375	07	1	ADD
376	16	2	SUB
377	17	1	SUB

REVISIONS		
CHK	CHANGE NO.	REV.

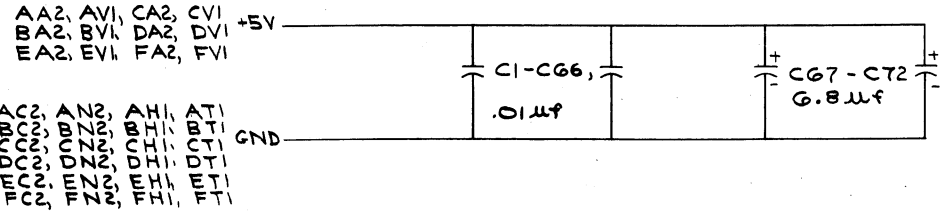
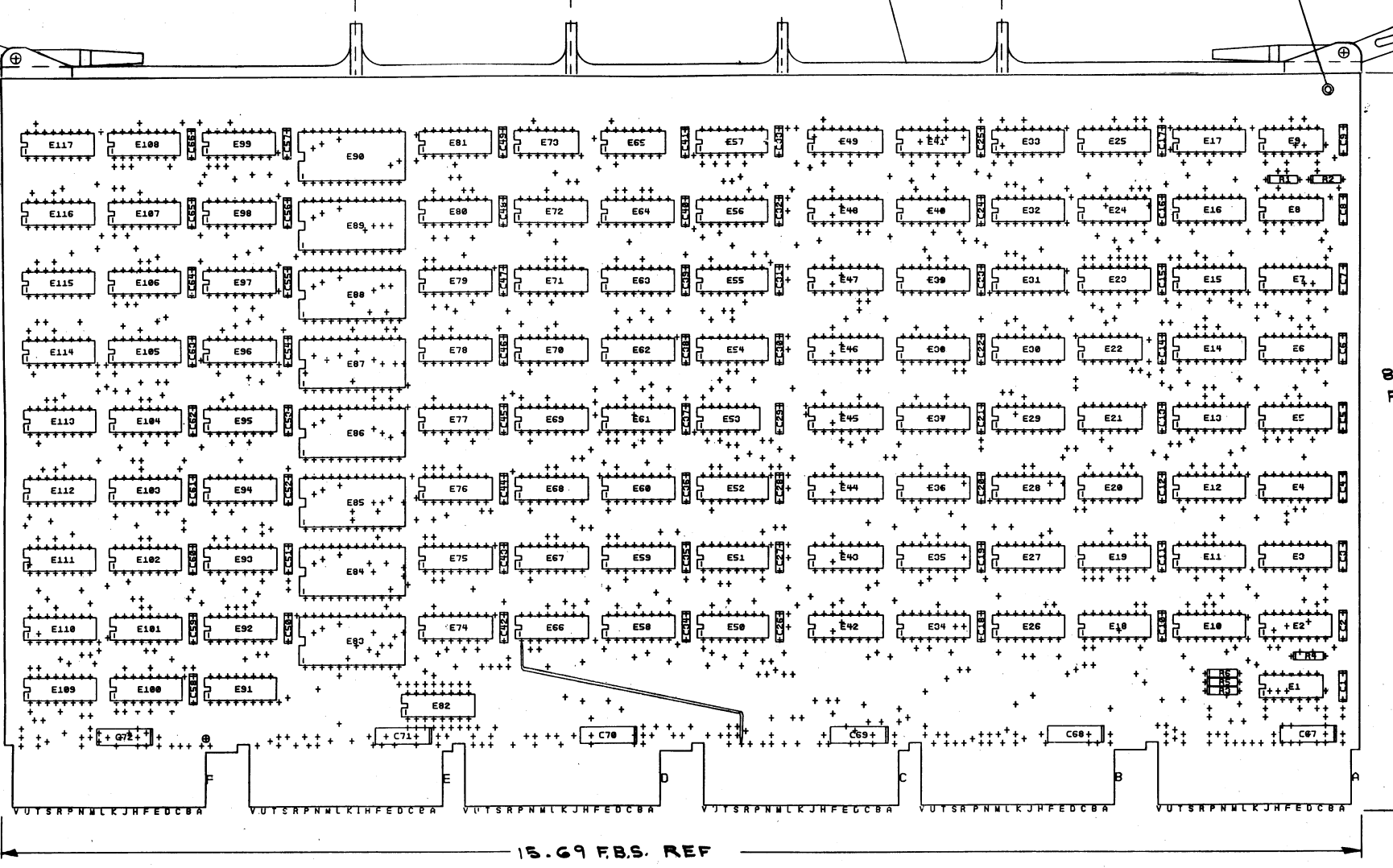
(SLOT 02)

TITLE	FRACTION PROC. HIGH ORDER	SIZE CODE	D CS M8126-0-1	NUMBER	13 OF 13	REV.	C
SCALE		SHEET	13 OF 13	DIST.			

REV. C
NUMBER D CS M8126-0-1

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NOTES:



IC 74S182	8	16
IC 74S175	8	16
IC 74157	8	16
IC 74174	8	16
IC 74175	8	16
IC 74S174	8	16
IC 74S158	8	16
IC 74S157	8	16
IC 74S153	8	16
IC 74S181	12	24
IC 74153	8	16
IC TYPE	GND	+5V

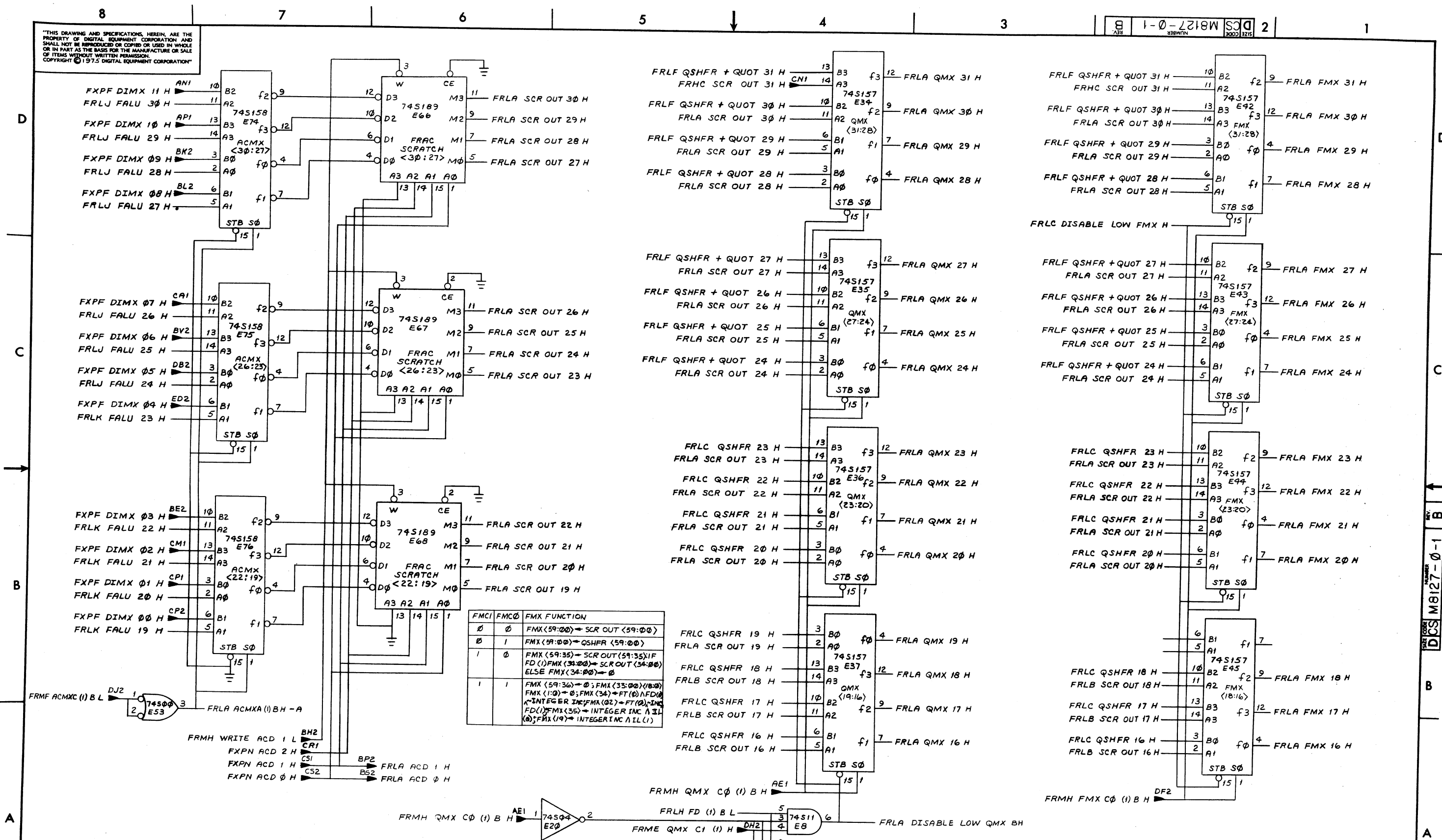
GND AND 5V ARE USUALLY PIN 7 AND 14
 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REF	X-Y COORDINATE HOLE LOCATION	K-CO-M8127-0-4	1	
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M8127-0-5	2	
REF	MODULE ECO HISTORY	B-MH-M8127-0-6	3	
1	ETCHED CIRCUIT BOARD	5011871	4	
66	C1 THRU C66	CAPACITOR, .01µf	10J1610-00	5
6	C67 THRU C72	CAPACITOR, 6.8µf	1005306	6
1	HANDLE HEX MODULE	1210711-2	7	
3	R1, R3, R5	RESISTOR, 330 OHM, 1/4W, 5%	1300295	8
3	R2, R4, R6	RESISTOR, 680 OHM, 1/4W, 5%	1301424	9
1	E1	I.C. DEC 8242	1909712	10
8	E50, E51, E52, E58, E60, E100, E109, E59	I.C. DEC 74153	1909937	11
8	E83 THRU E90	I.C. DEC 74S181	1910531	12
2	E9, E53	I.C. DEC 74S00	1910532	13
2	E20, E73	I.C. DEC 74S04	1910534	14
1	E21	I.C. DEC 74S10	1910536	15
3	E8, E22, E65	I.C. DEC 74S11	1910537	16
3	E23, E25, E57	I.C. DEC 74S153	1910547	17
5	E61 THRU E64, E55	I.C. DEC 74157	1910655	18
7	E74 THRU E80	I.C. DEC 74S158	1910549	19
10	E2-E6, E92, E94, E95, E97, E98	I.C. DEC 74S174	1910550	20
1	E56	I.C. DEC 74175	1910651	21
1	E54	I.C. DEC 74174	1910652	22
17	E34 THRU E49, E93	I.C. DEC 74S157	1910548	23
2	E7, E81	I.C. DEC 74S175	1910957	24
3	E91, E93, E86	I.C. DEC 74S182	1912097	25
7	E66 THRU E72	I.C. DEC 74S189	1912661	26
34	E10 THRU E19, E26 THRU E33, E101 THRU E108, E110-E117	I.C. DEC 25S10	1912693	27
1	E24	ROM	23006A2	28
12	EYELET	9006732	29	
A/B	#30 AWG WIRE	9105740-55	30	

QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
	FPII-C	ETCH BOARD REV. C		
PARTS LIST				
DRN.	DATE	TITLE		
CHKD.	DATE	FRACTION PROC.		
ENG.	DATE	LOW ORDER		
PROJ. ENG.	DATE	B-LD-FPII-C		
PROD.	DATE	SCALE		
NEXT HIGHER ASSY				
SEMICONDUCTOR CONVERSION CHART				
DEC. NO.	EIA. NO.	DEC. NO.	EIA. NO.	SHEET 1 OF 14

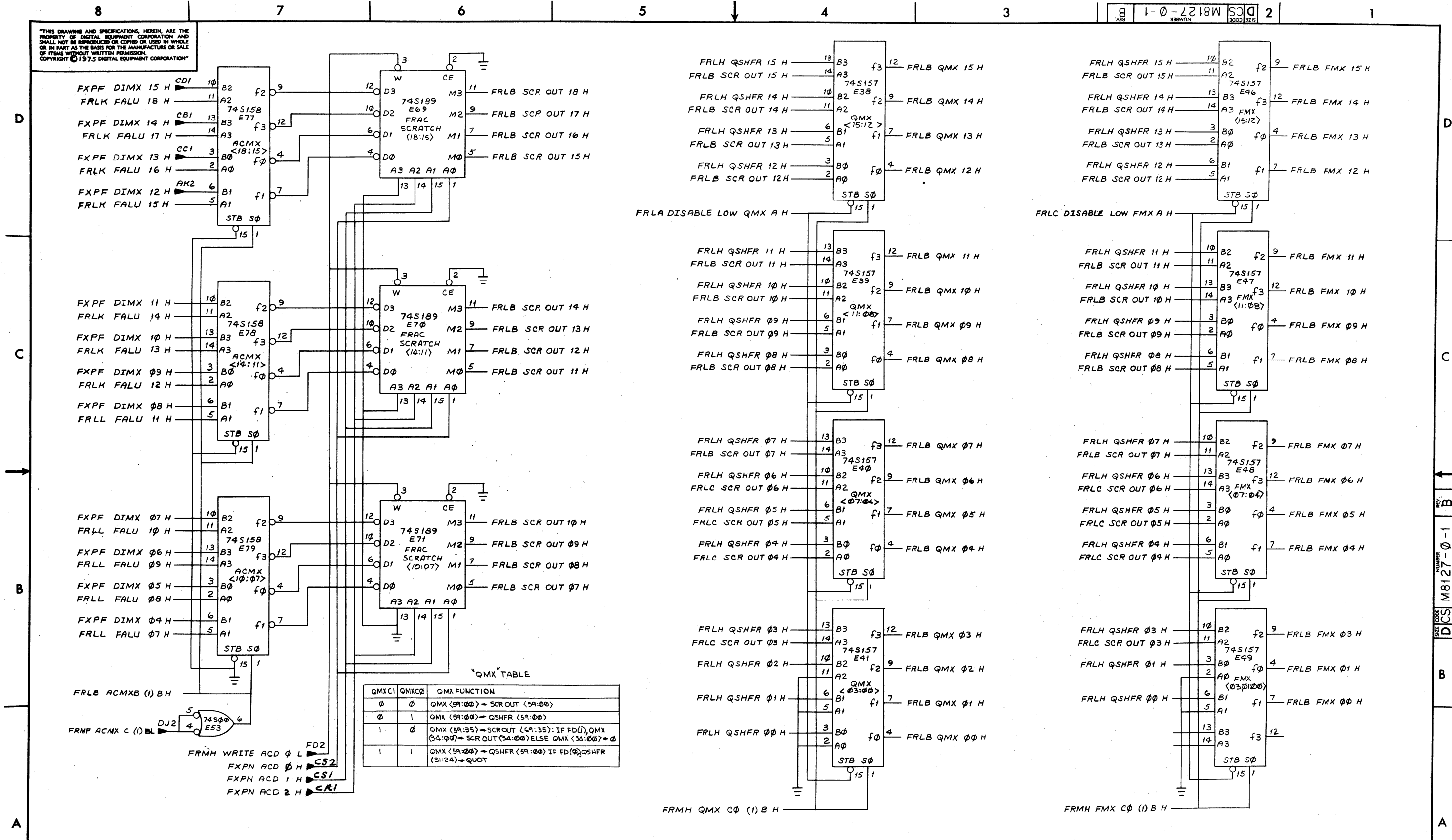
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FMC1	FMC0	FMX FUNCTION
0	0	FMX(59:00) → SCR OUT (59:00)
0	1	FMX(59:00) → QSHFR (59:00)
1	0	FMX(59:35) → SCR OUT (59:35) IF FD(1) FMX(34:00) → SCR OUT (34:00) ELSE FMX(34:00) → 0
1	1	FMX(59:36) → 0; FMX(33:00) → (B:0) FMX(1:0) → 0; FMX(34) → FT(0) NFD(0) → INTEGER INC; FMX(02) → FT(0) → INC; FD(1) FMX(35) → INTEGER INC A IL(1) (0); FMX(19) → INTEGER INC A IL(1)

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CHK	CHANGE NO.	REV.

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'QMX' TABLE

QMXC1	QMXC0	QMX FUNCTION
0	0	QMX (5A:00) → SCR OUT (5A:00)
0	1	QMX (5A:00) → QSHFR (5A:00)
1	0	QMX (5A:35) → SCR OUT (5A:35); IF FD(1), QMX (3A:00) → SCR OUT (3A:00) ELSE QMX (3A:00) → 0
1	1	QMX (5A:00) → QSHFR (5A:00) IF FD(0); QSHFR (31:24) → QUOT

REVISIONS

CHK	CHANGE NO.	REV.

(SLOT 3)

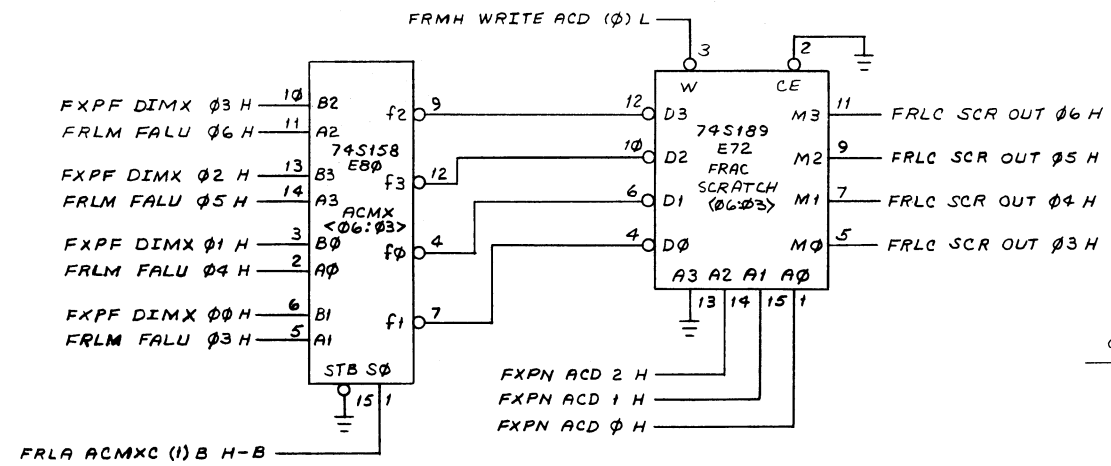
TITLE	SIZE CODE	NUMBER	REV.
FRACTION PROC. LOW ORDER (FRLB)	DCS	M8127-0-1	B

SCALE: 1/4 SHEET: 3 OF 14 DIST.:

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D
C
B
A

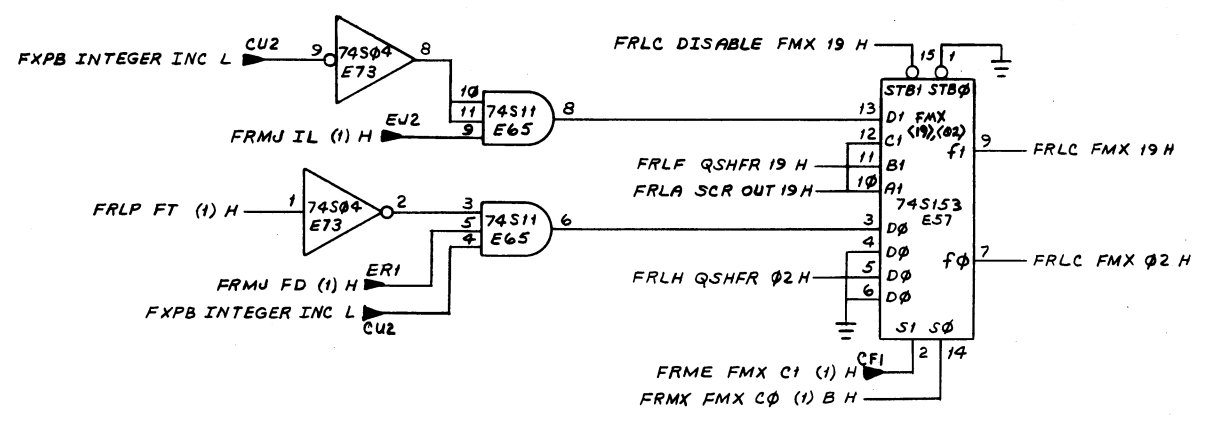
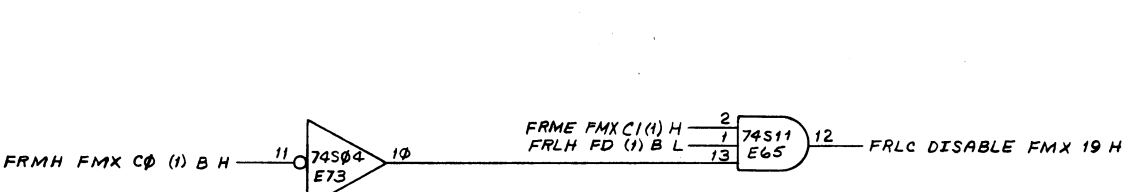
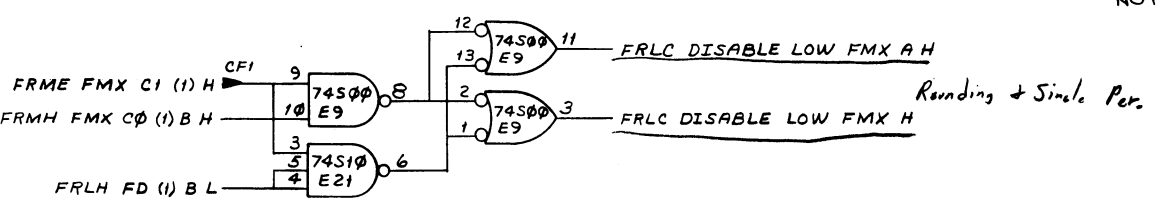
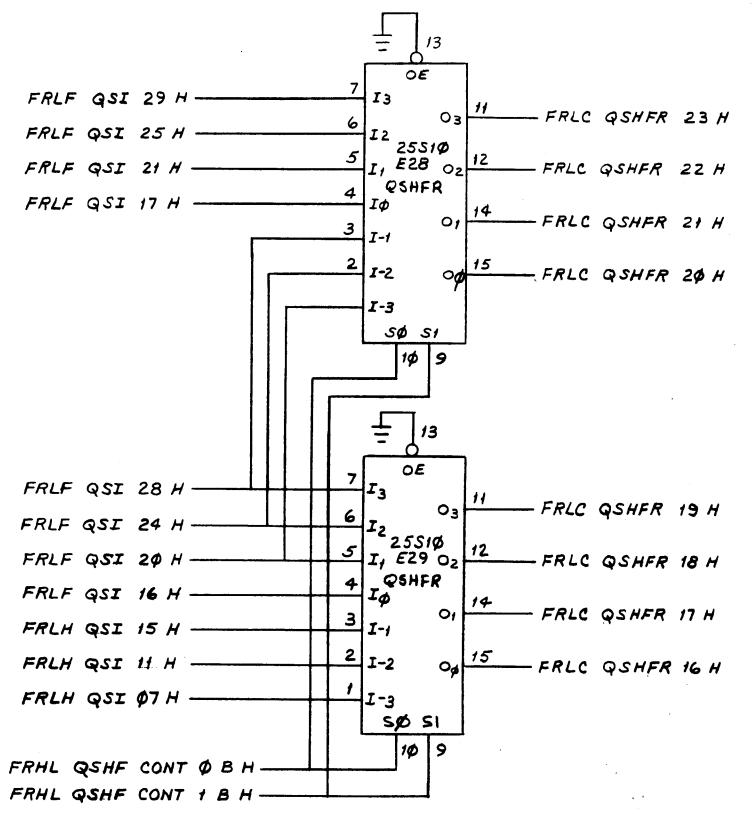
D
C
B
A



TRUTH TABLE FOR DEC 25510

O _E	S ₁	S ₀	O ₀	O ₁	O ₂	O ₃
0	0	0	I ₀	I ₁	I ₂	I ₃
0	0	1	I-1	I ₀	I ₁	I ₂
0	1	0	I-2	I-1	I ₀	I ₁
0	1	1	I-3	I-2	I-1	I ₀
1	X	X	Z	Z	Z	Z

NOTES: X=DONT CARE
Z=OUTPUT 'OFF' I.E. IN HIGH IMPEDANCE STATE

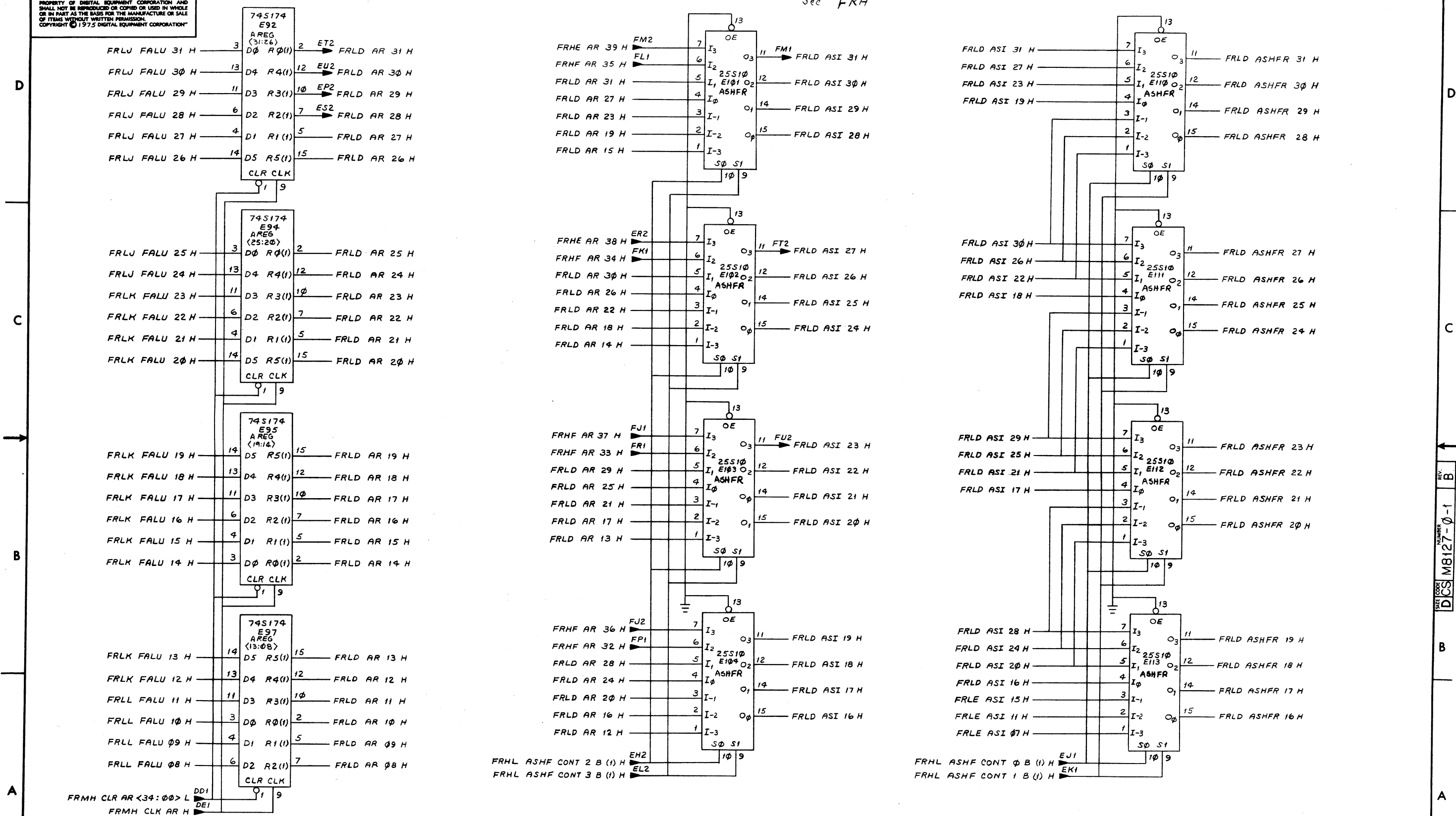


(SLOT 3)

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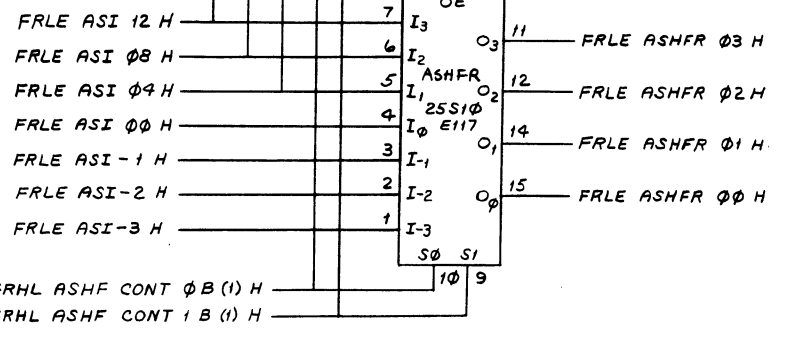
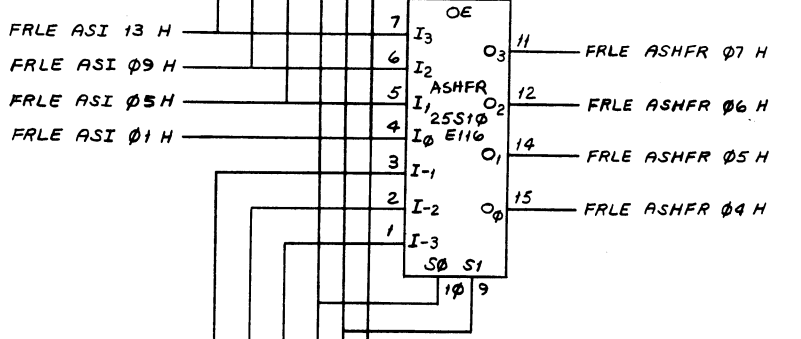
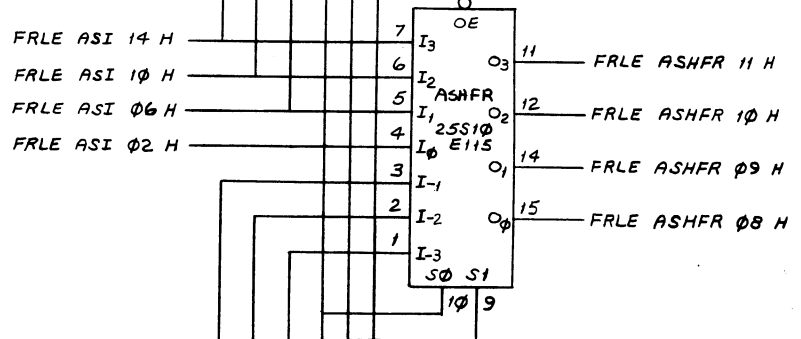
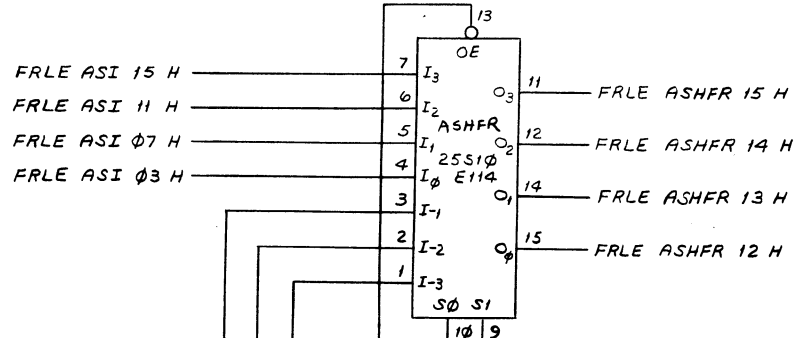
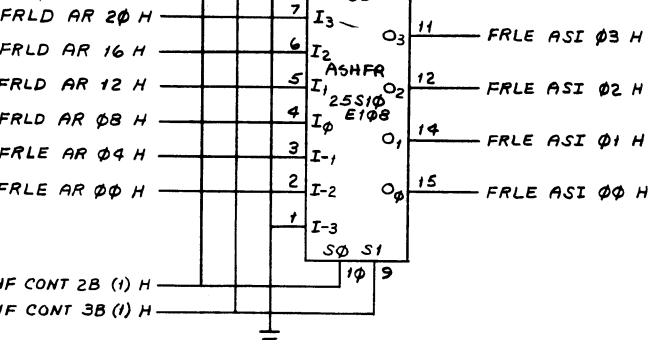
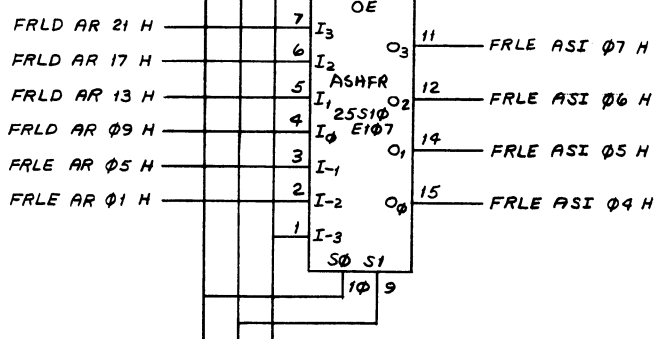
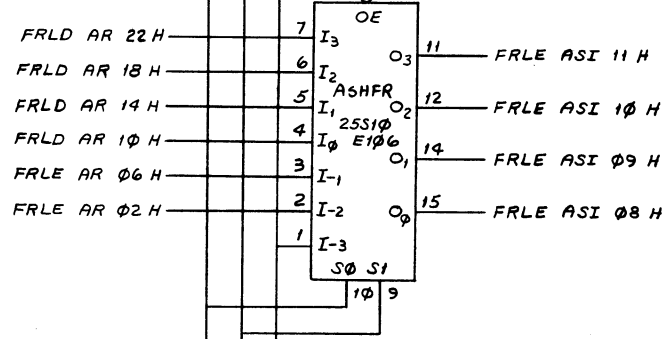
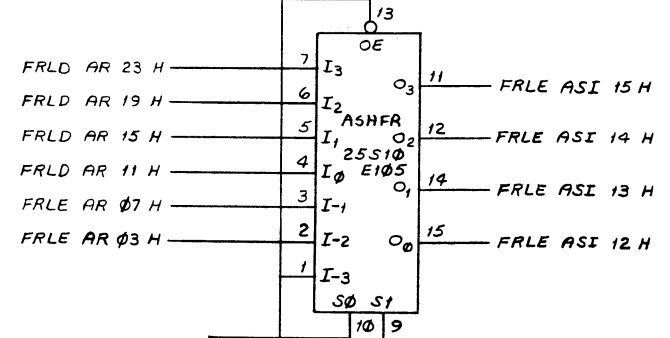
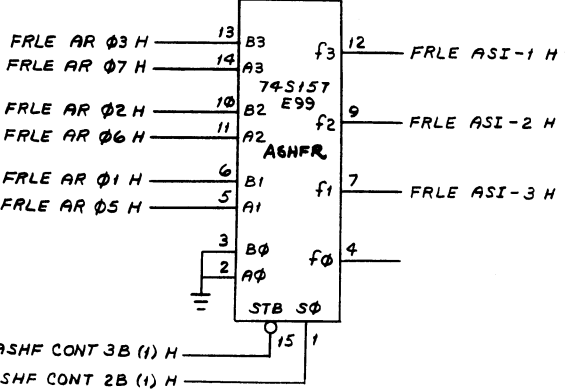
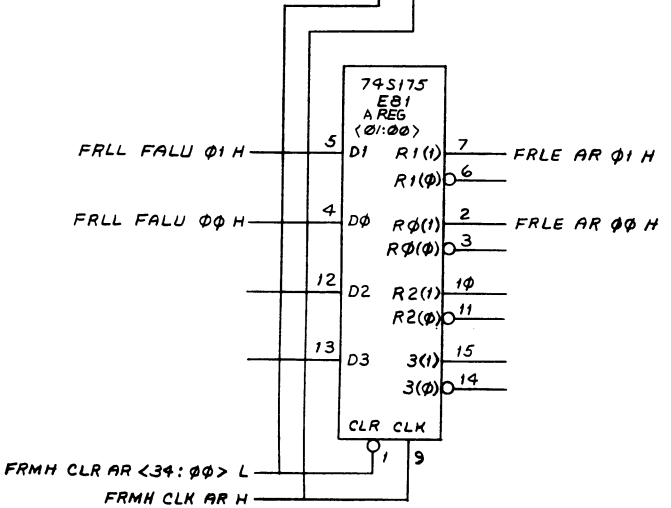
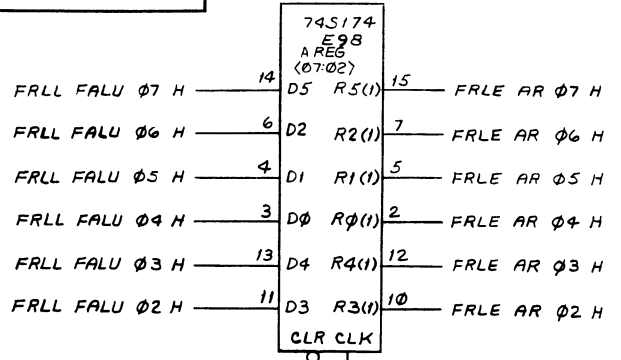
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		FRACTION PROC.	DCS	M8127-0-1	B
		LOW ORDER (FRLD)			
SCALE	SHEET	DIST.			
1/1	5 OF 14				

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REV. B
 NUMBER 1-0-2218W
 SIZE DCS
 3000 3215

D
 C
 B
 A

D
 C
 B
 A

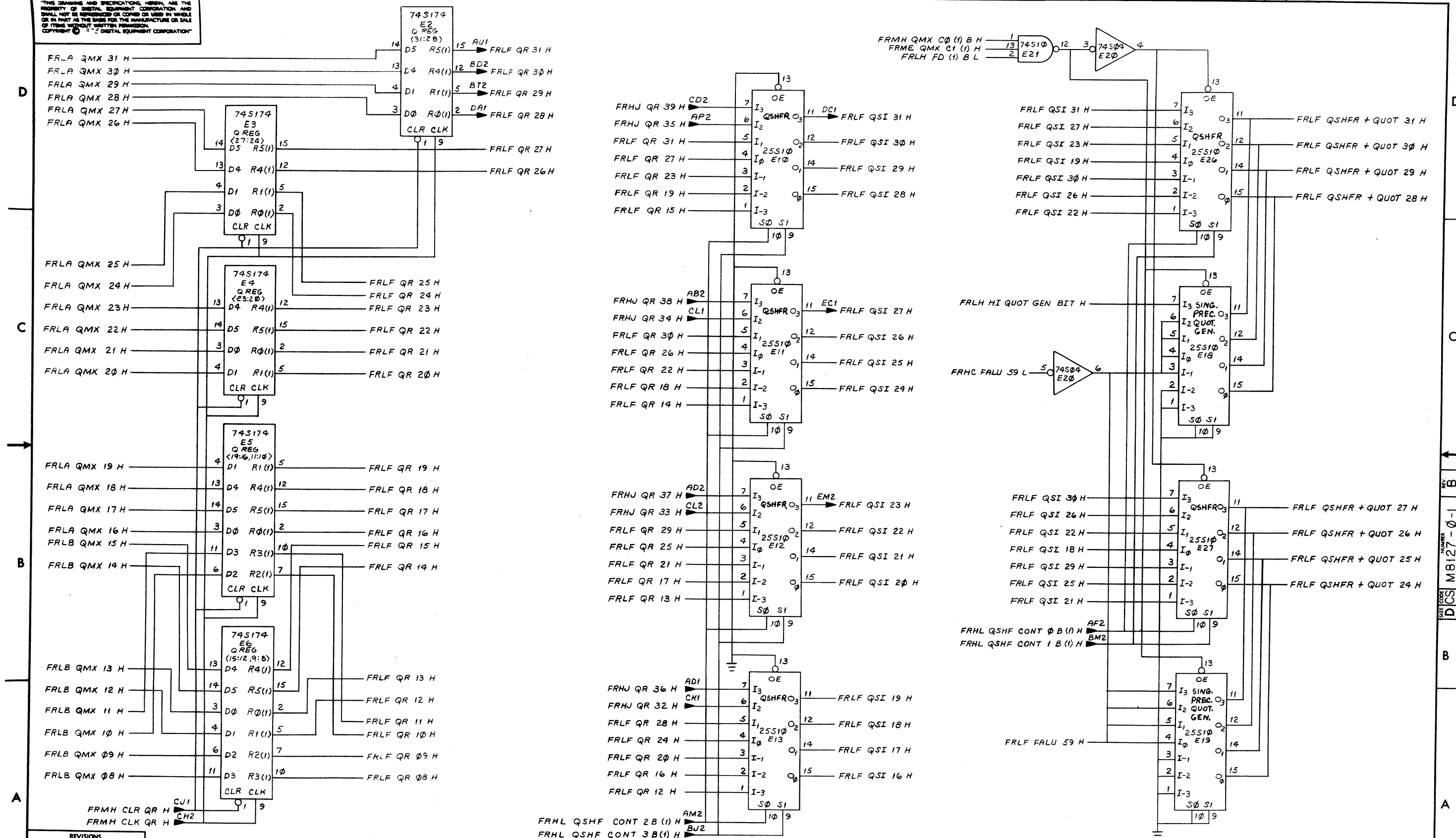


(SLOT 3)

REVISIONS		
CHK	CHANGE NO.	REV.

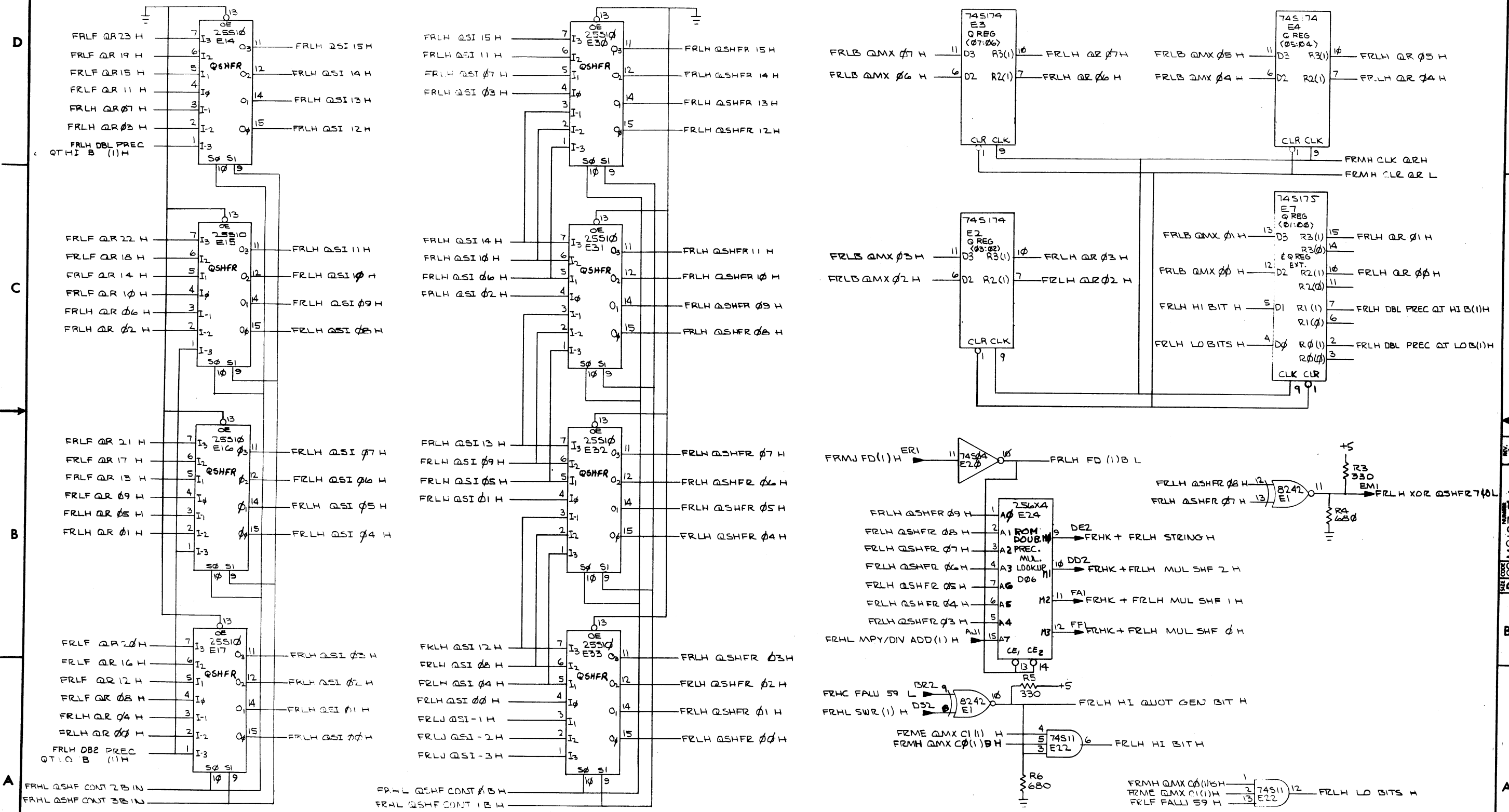
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SCALE	1/1	DCS	M8127-0-1	B.
SHEET	6 OF 14	DIST.		

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REVISIONS		
CHK	CHANGE NO.	REV.

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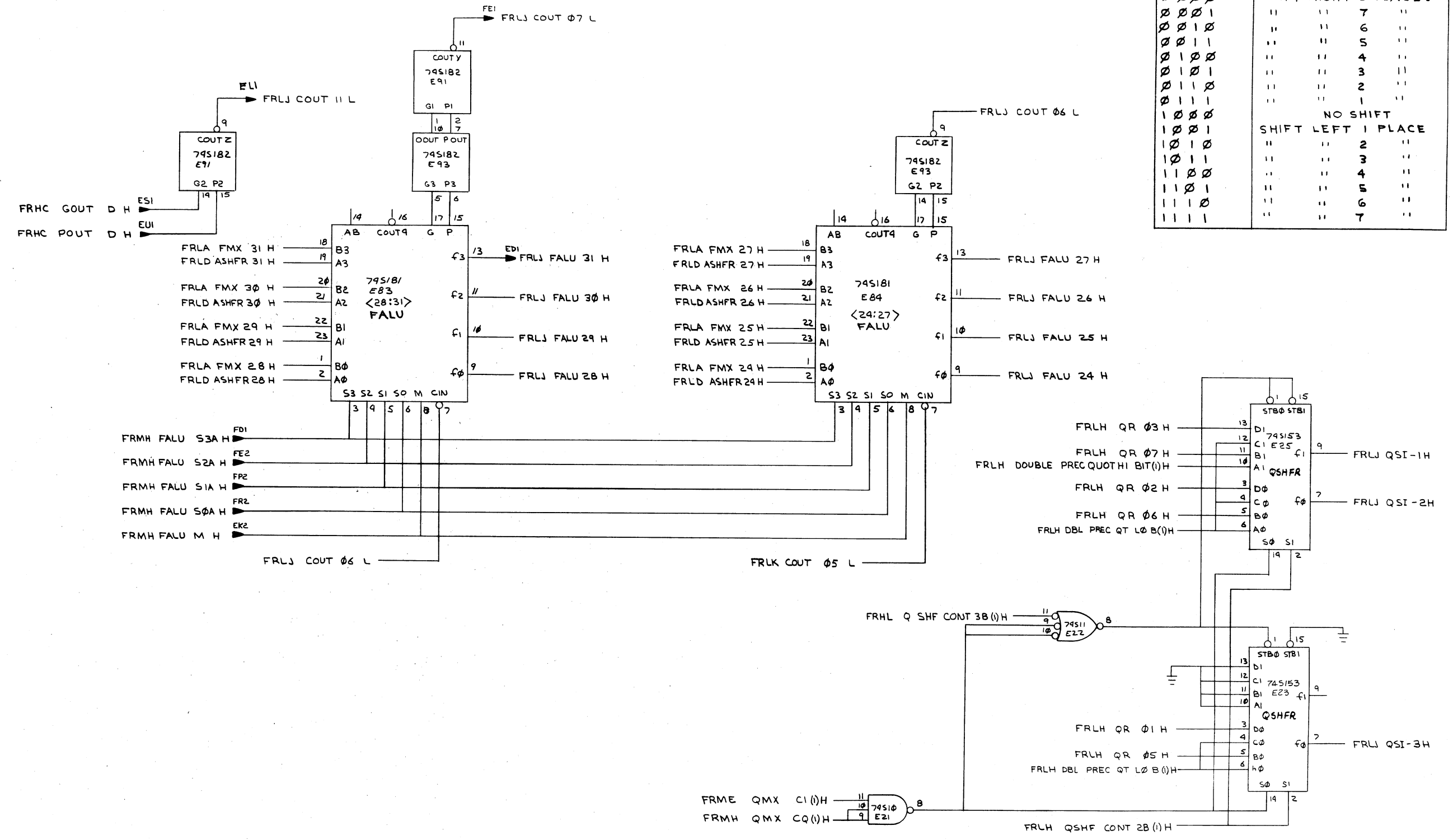


REVISIONS		
CHK	CHANGE NO.	REV.

(SLOT 3)

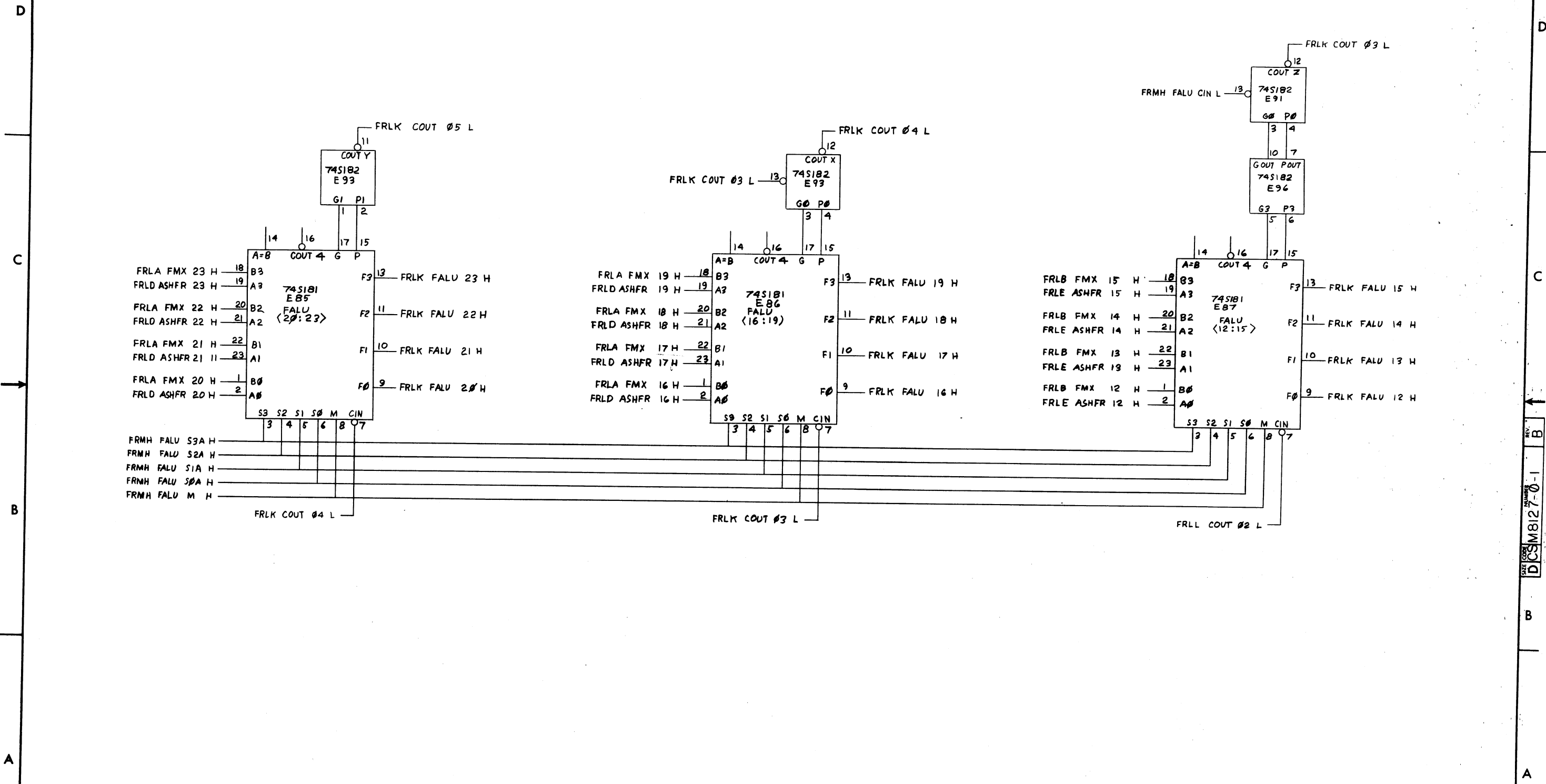
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A/Q SHF CONT	ASHFR/QSHFR FUNCTION	
3 2 1 0		
0 0 0 0	SHIFT RIGHT 8 PLACES	
0 0 0 1	" " 7	"
0 0 1 0	" " 6	"
0 0 1 1	" " 5	"
0 1 0 0	" " 4	"
0 1 0 1	" " 3	"
0 1 1 0	" " 2	"
0 1 1 1	" " 1	"
1 0 0 0	NO SHIFT	
1 0 0 1	SHIFT LEFT 1 PLACE	
1 0 1 0	" " 2	"
1 0 1 1	" " 3	"
1 1 0 0	" " 4	"
1 1 0 1	" " 5	"
1 1 1 0	" " 6	"
1 1 1 1	" " 7	"



REVISIONS		
CHK	CHANGE NO.	REV.

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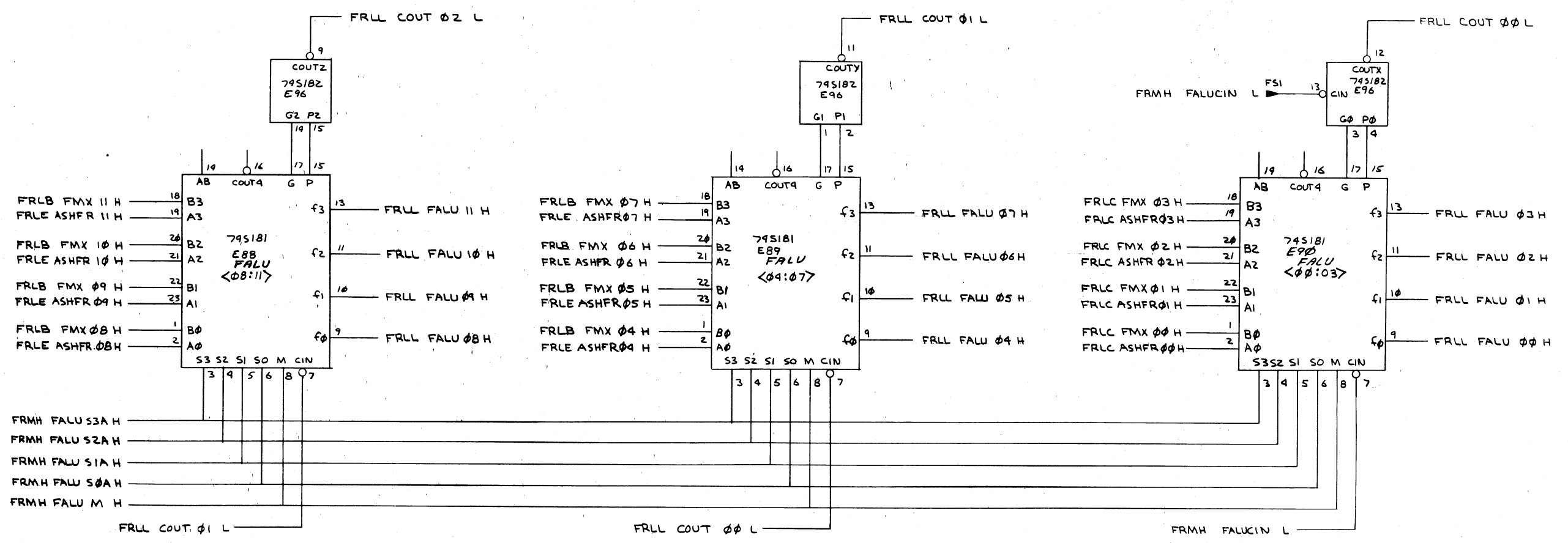


REVISIONS		
CHK	CHANGE NO.	REV.

(SLOT 3)

TITLE	FRACTION (FRLK) PROC LOW ORDER	SIZE CODE	D	NUMBER	CSM8127-0-1	REV.	B
SCALE	1:1	SHEET	10	OF	14	DIST.	

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REVISIONS		
CHK	CHANGE NO.	REV.

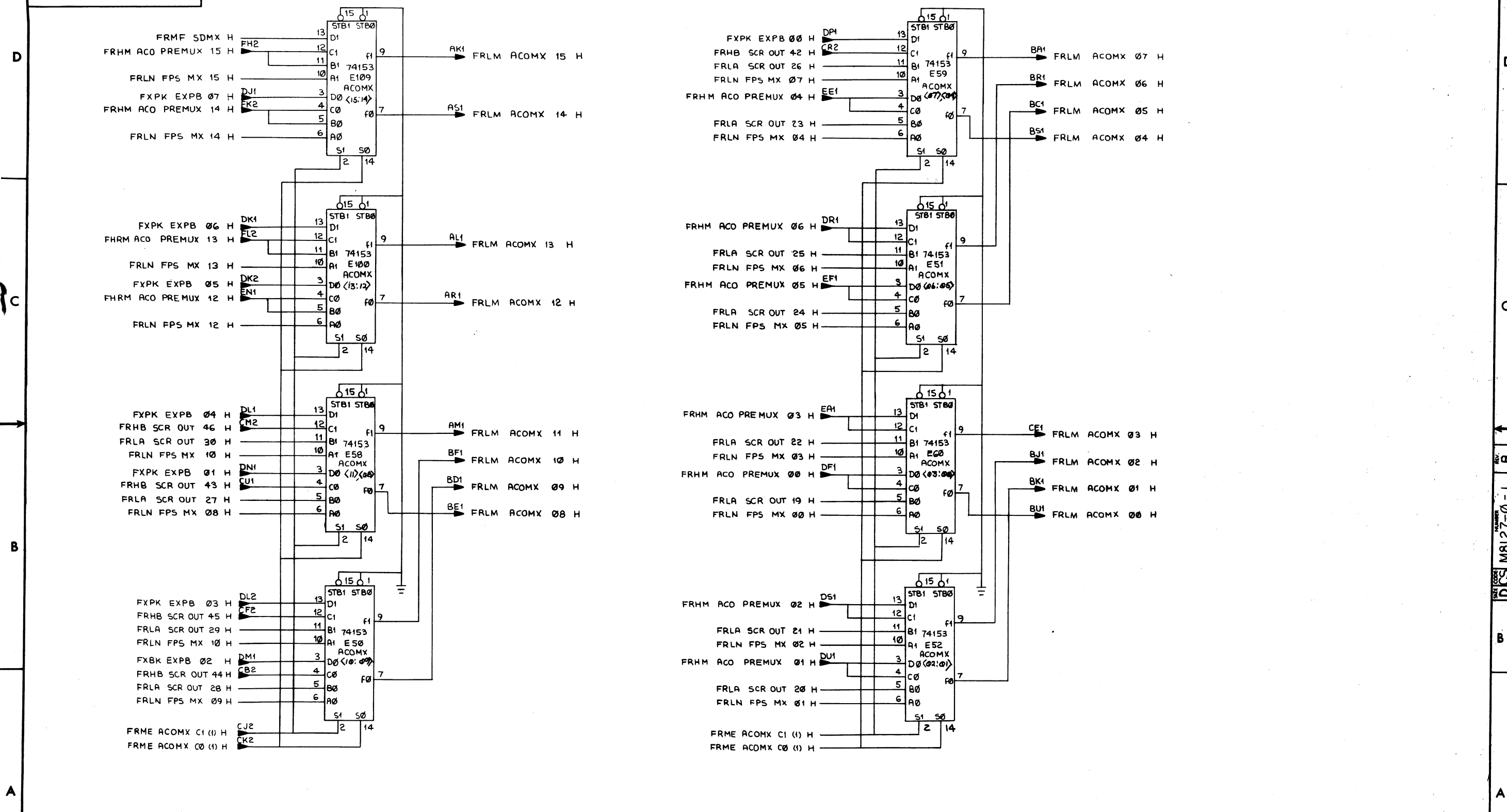
TITLE	FRACTION PROC LOW ORDER (FALL)	SIZE CODE	D	NUMBER	DCSM8127-0-1	REV.	B
SCALE		SHEET	11	OF	14	DIST.	

REV. B DCSM8127-0-1

(SLOT 3)

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REV. 1-0-2-0-1 DCS M8127-0-1

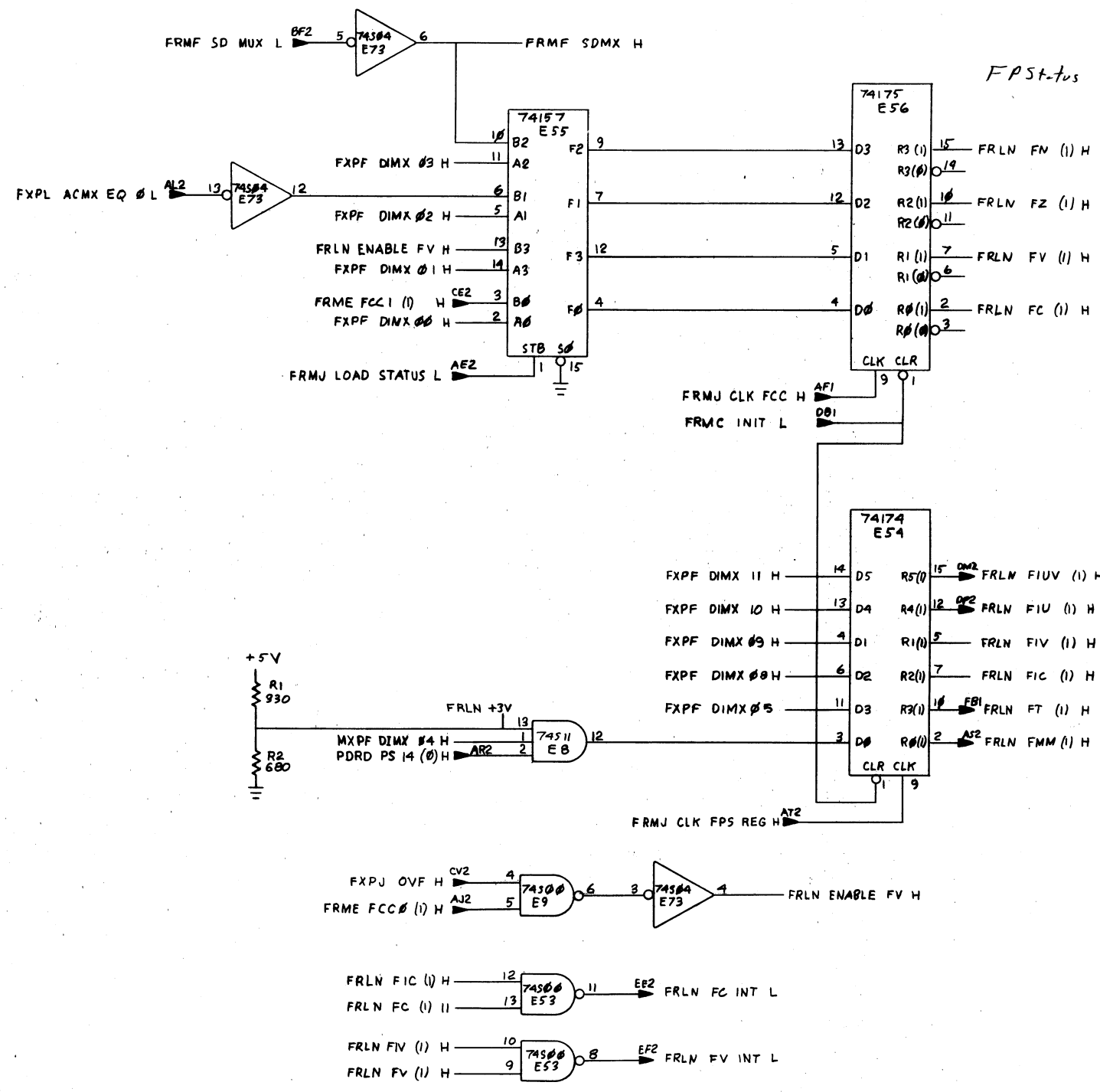
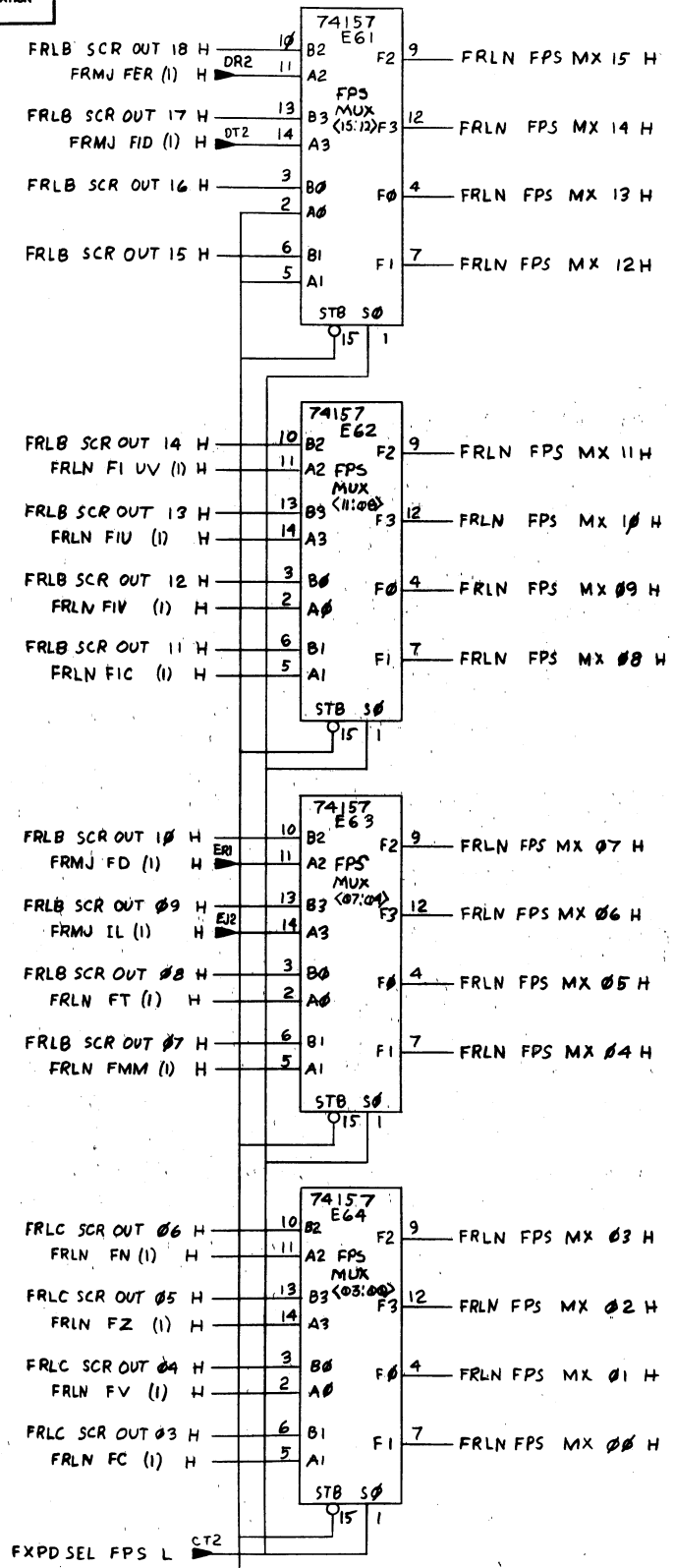


REVISIONS		
CHK	CHANGE NO.	REV.

(SLOT 3)

TITLE	FRACTION (FRLM) PROC. LOW ORDER	SIZE CODE	DCS	NUMBER	M8127-0-1	REV.	B
SCALE	—	SHEET	12	OF	14	DIST.	

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(SLOT 3)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	FRACTION (FRLN) PROC LOW ORDER	SIZE CODE	D	NUMBER	DCS M8127-0-1	REV.	B
SCALE		SHEET	13	OF	14	DIST.	

DATE FORK NUMBER DCS M8127-0-1 REV. B

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MULTIPLY CONTROL LOOKUP ROM

REV. 8 DCS M8127-0-1 2

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
000	07	1	ADD
001	06	2	ADD
002	17	1	SUB
003	05	3	ADD
004	07	1	ADD
005	16	2	SUB
006	17	1	SUB
007	04	4	ADD
010	07	1	ADD
011	06	2	ADD
012	17	1	SUB
013	15	3	SUB
014	07	1	ADD
015	16	2	SUB
016	17	1	SUB
017	03	5	ADD
020	07	1	ADD
021	06	2	ADD
022	17	1	SUB
023	15	3	SUB
024	07	1	ADD
025	16	2	SUB
026	17	1	SUB
027	14	4	SUB
030	07	1	ADD
031	06	2	ADD
032	17	1	SUB
033	15	3	SUB
034	07	1	ADD
035	16	2	SUB
036	17	1	SUB
037	02	6	ADD
040	07	1	ADD
041	06	2	ADD
042	17	1	SUB
043	05	3	ADD
044	07	1	ADD
045	16	2	SUB
046	17	1	SUB
047	04	4	ADD
050	07	1	ADD
051	06	2	ADD
052	17	1	SUB
053	15	3	SUB
054	07	1	ADD
055	16	2	SUB
056	17	1	SUB
057	13	5	SUB
060	07	1	ADD
061	06	2	ADD
062	17	1	SUB
063	05	3	ADD
064	07	1	ADD
065	16	2	SUB
066	17	1	SUB
067	14	4	SUB
070	07	1	ADD
071	06	2	ADD
072	17	1	SUB
073	15	3	SUB
074	07	1	ADD
075	16	2	SUB
076	17	1	SUB
077	12	6	SUB

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
100	07	1	ADD
101	06	2	ADD
102	17	1	SUB
103	05	3	ADD
104	07	1	ADD
105	16	2	SUB
106	17	1	SUB
107	04	4	ADD
110	07	1	ADD
111	06	2	ADD
112	17	1	SUB
113	15	3	SUB
114	07	1	ADD
115	16	2	SUB
116	17	1	SUB
117	03	5	ADD
120	07	1	ADD
121	06	2	ADD
122	17	1	SUB
123	05	3	ADD
124	07	1	ADD
125	16	2	SUB
126	17	1	SUB
127	14	4	SUB
130	07	1	ADD
131	06	2	ADD
132	17	1	SUB
133	15	3	SUB
134	07	1	ADD
135	16	2	SUB
136	17	1	SUB
137	12	6	SUB
140	07	1	ADD
141	06	2	ADD
142	17	1	SUB
143	05	3	ADD
144	07	1	ADD
145	16	2	SUB
146	17	1	SUB
147	04	4	ADD
150	07	1	ADD
151	06	2	ADD
152	17	1	SUB
153	15	3	SUB
154	07	1	ADD
155	16	2	SUB
156	17	1	SUB
157	13	5	SUB
160	07	1	ADD
161	06	2	ADD
162	17	1	SUB
163	05	3	ADD
164	07	1	ADD
165	16	2	SUB
166	17	1	SUB
167	14	4	SUB
170	07	1	ADD
171	06	2	ADD
172	17	1	SUB
173	15	3	SUB
174	07	1	ADD
175	16	2	SUB
176	17	1	SUB
177	12	6	SUB

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
200	02	6	ADD
201	07	1	ADD
202	06	2	ADD
203	17	1	SUB
204	05	3	ADD
205	07	1	ADD
206	16	2	SUB
207	17	1	SUB
210	04	4	ADD
211	07	1	ADD
212	06	2	ADD
213	17	1	SUB
214	15	3	SUB
215	07	1	ADD
216	16	2	SUB
217	17	1	SUB
220	03	5	ADD
221	06	2	ADD
222	17	1	SUB
223	05	3	ADD
224	07	1	ADD
225	16	2	SUB
226	17	1	SUB
227	14	4	SUB
230	07	1	ADD
231	06	2	ADD
232	17	1	SUB
233	15	3	SUB
234	07	1	ADD
235	16	2	SUB
236	17	1	SUB
237	17	1	SUB
240	02	6	ADD
241	07	1	ADD
242	06	2	ADD
243	17	1	SUB
244	05	3	ADD
245	07	1	ADD
246	16	2	SUB
247	17	1	SUB
250	04	4	ADD
251	07	1	ADD
252	06	2	ADD
253	17	1	SUB
254	15	3	SUB
255	07	1	ADD
256	16	2	SUB
257	17	1	SUB
260	13	5	SUB
261	07	1	ADD
262	06	2	ADD
263	17	1	SUB
264	05	3	ADD
265	07	1	ADD
266	16	2	SUB
267	17	1	SUB
270	14	4	SUB
271	07	1	ADD
272	06	2	ADD
273	17	1	SUB
274	15	3	SUB
275	07	1	ADD
276	16	2	SUB
277	17	1	SUB

ADDRESS (OCTAL)	CONTENTS (OCTAL)	FUNCTION	
		SHIFT BY	OPERATION
300	02	6	ADD
301	07	1	ADD
302	06	2	ADD
303	17	1	SUB
304	05	3	ADD
305	07	1	ADD
306	16	2	SUB
307	17	1	SUB
310	04	4	ADD
311	07	1	ADD
312	06	2	ADD
313	17	1	SUB
314	15	3	SUB
315	07	1	ADD
316	16	2	SUB
317	17	1	SUB
320	03	5	ADD
321	06	2	ADD
322	17	1	SUB
323	05	3	ADD
324	07	1	ADD
325	16	2	SUB
326	17	1	SUB
327	14	4	SUB
330	07	1	ADD
331	06	2	ADD
332	17	1	SUB
333	15	3	SUB
334	07	1	ADD
335	16	2	SUB
336	17	1	SUB
337	17	1	SUB
340	02	6	ADD
341	07	1	ADD
342	06	2	ADD
343	17	1	SUB
344	05	3	ADD
345	07	1	ADD
346	16	2	SUB
347	17	1	SUB
350	04	4	ADD
351	07	1	ADD
352	06	2	ADD
353	17	1	SUB
354	15	3	SUB
355	07	1	ADD
356	16	2	SUB
357	17	1	SUB
360	13	5	SUB
361	07	1	ADD
362	06	2	ADD
363	17	1	SUB
364	05	3	ADD
365	07	1	ADD
366	16	2	SUB
367	17	1	SUB
370	14	4	SUB
371	07	1	ADD
372	06	2	ADD
373	17	1	SUB
374	15	3	SUB
375	07	1	ADD
376	16	2	SUB
377	17	1	SUB

REVISIONS		
CHK	CHANGE NO.	REV.

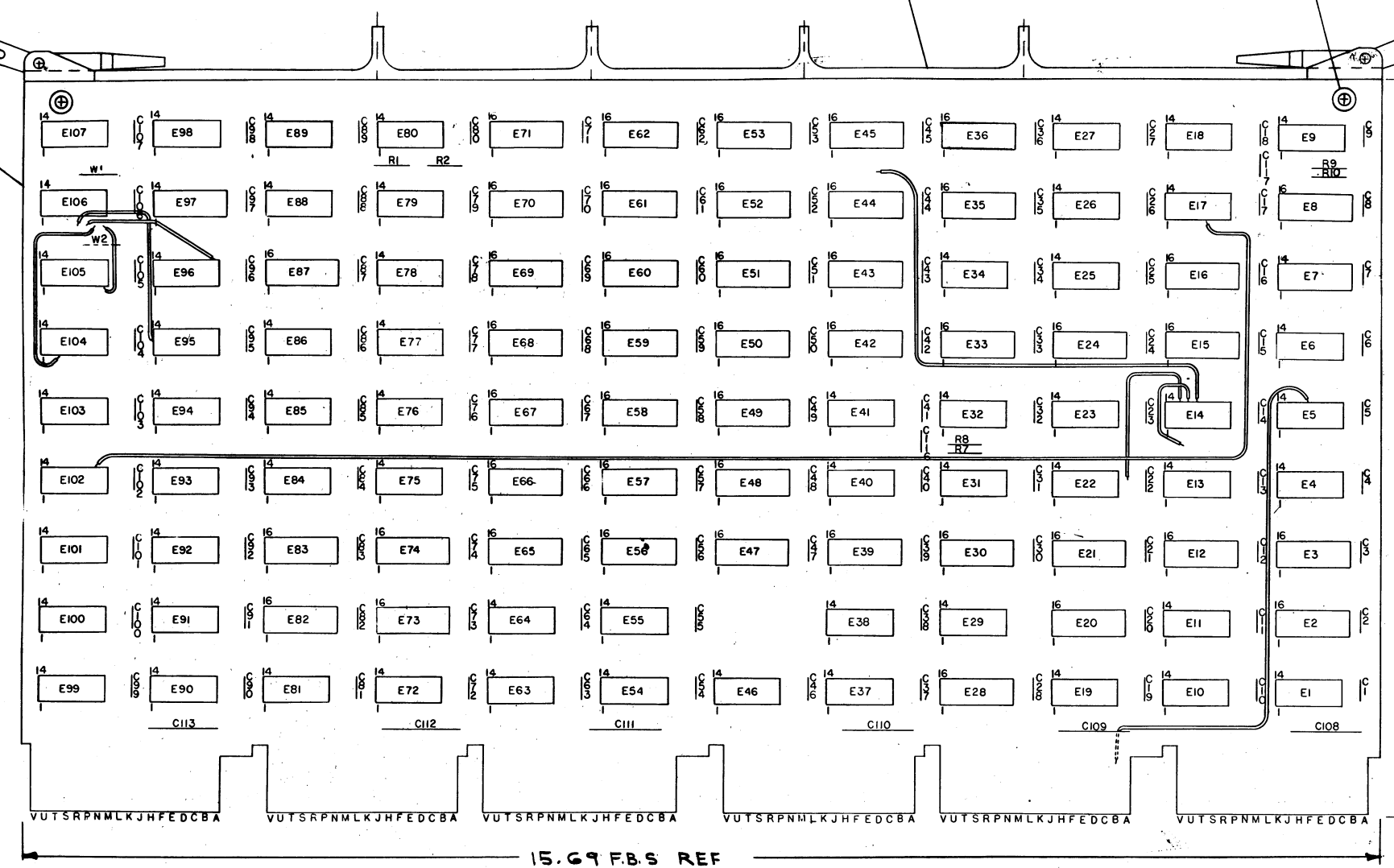
TITLE		FRACTION PROC. LOW ORDER (FRLP)		SIZE CODE	NUMBER		REV.
SCALE		SHEET 14 OF 14		DIST.	DCS M8127-0-1		B

(SLOT 3)

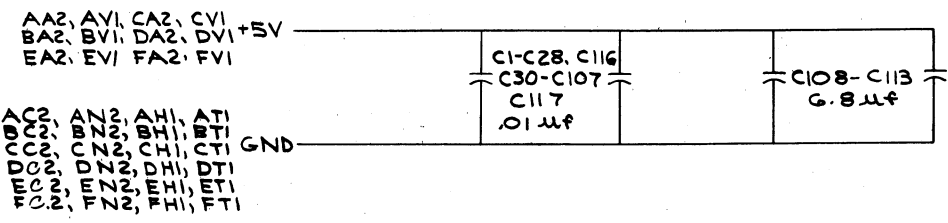
REV. 8 DCS M8127-0-1

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NOTES: 1) E8, AND E73 ARE SPARE IC LOCATIONS
2) REF. DES. C29 IS NOT USED



REF	X-Y COORDINATE HOLE LOCATION	K-CO-M8128-0-4	1
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M8128-0-5	2
REF	MODULE ECO HISTORY	B-MH-M8128-0-6	3
1	ETCHED CIRCUIT BOARD	5011872	4
108	C1 THRU C28, C30 THRU C107, C116, C117	CAPACITOR, .01uf	1001610-00
6	C108 THRU C113	CAPACITOR, 6.8uf	1005306
1	HANDLE HEX MODULE	1210711-2	7
1	R1	SPARE	8
2	R8, R10	RESISTOR, 560 OHM, 1/4W, 5%	1301890
1	R2	RESISTOR, 100 OHM, 1/4W, 5%	1300229
2	R7, R9	RESISTOR, 270 OHM, 1/4W, 5%	1301972
3	E35, E36, E87	I.C. DEC 74151	1909936
1	E27	I.C. DEC 7486	1910011
1	E16	I.C. DEC 74193	1910018
9	E14, E17, E55, E75, E78, E84, E98, E100, E106	I.C. DEC 74S00	1910532
6	E26, E40, E41, E64, E96, E101	I.C. DEC 74S04	1910534
7	E18, E19, E72, E80, E89, E94, E102	I.C. DEC 74S10	1910536
4	E11, E34, E95, E7	I.C. DEC 74S11	1910537
2	E4, E93	I.C. DEC 74S20	1910539
9	E29, E37, E88, E46, E90, E99, E103, E20, E79	I.C. DEC 74S40	1910541
3	E13, E22, E54	I.C. DEC 74S64	1910542
9	E1, E5, E9, E10, E19, E63, E81, E105, E107	I.C. DEC 74S74	1910544
3	E82, E83, E104	I.C. DEC 74S112	1910545
7	E76, E77, E85, E86, E91, E92, E38	I.C. DEC 74S140	1910546
3	E15, E24, E33	I.C. DEC 74S174	1910550
1	E28	I.C. DEC 74157	1910655
4	E3, E12, E21, E30	I.C. DEC 74S151	1910956
5	E2, E39, E42, E65, E66	I.C. DEC 74S175	1910957
5	E23, E25, E31, E32, E97	I.C. DEC 74S51	1911712-00-S
1	E74	IC DEC 8251-1	1909014
1	E47	ROM	23030A2
1	E48	ROM	23030A2
1	E49	ROM	23027A2
1	E50	ROM	23031A2
1	E51	ROM	23013A2
1	E52	ROM	23019A2
1	E53	ROM	23021A2
1	E56	ROM	23022A2
1	E57	ROM	23014A2
1	E58	ROM	23015A2
1	E59	ROM	23016A2
1	E60	ROM	23017A2
1	E61	ROM	23020A2
1	E62	ROM	23018A2
12	EYELET	9006732	45
8	E42, E45, E67, E69, E70, E71	IC DEC 74175	1910651
1	VVI	JUMPER	9009185
A/R	WIRE, 30 AWG	9105740-55	48
			49



IC TYPE	GND	+5V
IC 74175	8	16
256x4 ROM	8	16
IC 74S175	8	16
IC 74S151	8	16
IC 74157	8	16
IC 74S174	8	16
IC 74S112	8	16
IC 74193	8	16
IC 74151	8	16
IC TYPE	GND	+5V

AA2, AV1, CA2, CV1
BA2, BV1, DA2, DV1 +5V
EA2, EV1, FA2, FV1

AA1, AV2, CA1, CV2
BA1, BV2, DA1, DV2
EA1, EV2, FA1, FV2

AA3, AV3, CA3, CV3
BA3, BV3, DA3, DV3
EA3, EV3, FA3, FV3

AA4, AV4, CA4, CV4
BA4, BV4, DA4, DV4
EA4, EV4, FA4, FV4

AA5, AV5, CA5, CV5
BA5, BV5, DA5, DV5
EA5, EV5, FA5, FV5

AA6, AV6, CA6, CV6
BA6, BV6, DA6, DV6
EA6, EV6, FA6, FV6

AA7, AV7, CA7, CV7
BA7, BV7, DA7, DV7
EA7, EV7, FA7, FV7

AA8, AV8, CA8, CV8
BA8, BV8, DA8, DV8
EA8, EV8, FA8, FV8

AA9, AV9, CA9, CV9
BA9, BV9, DA9, DV9
EA9, EV9, FA9, FV9

AA0, AV0, CA0, CV0
BA0, BV0, DA0, DV0
EA0, EV0, FA0, FV0

FIRST USED ON OPTION MODEL
FPII-C

ETCH BOARD REV. C

digital

TITLE: FP ROM CONTROL

SEMICONDUCTOR CONVERSION CHART

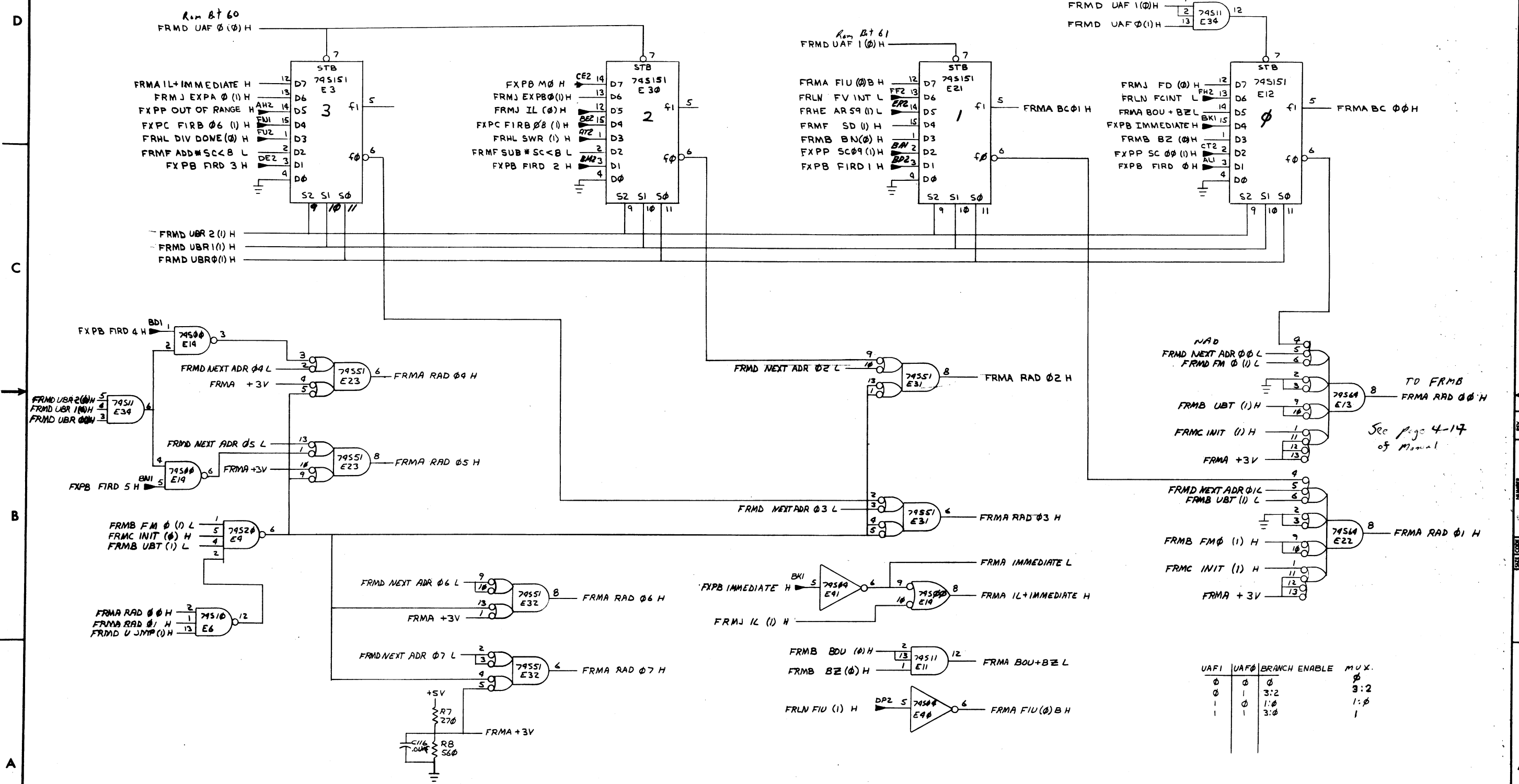
DEC NO. EIA NO. DEC NO. EIA NO.

SHEET 1 OF 11

DIST. CODE: M8128-0-1

REV. B

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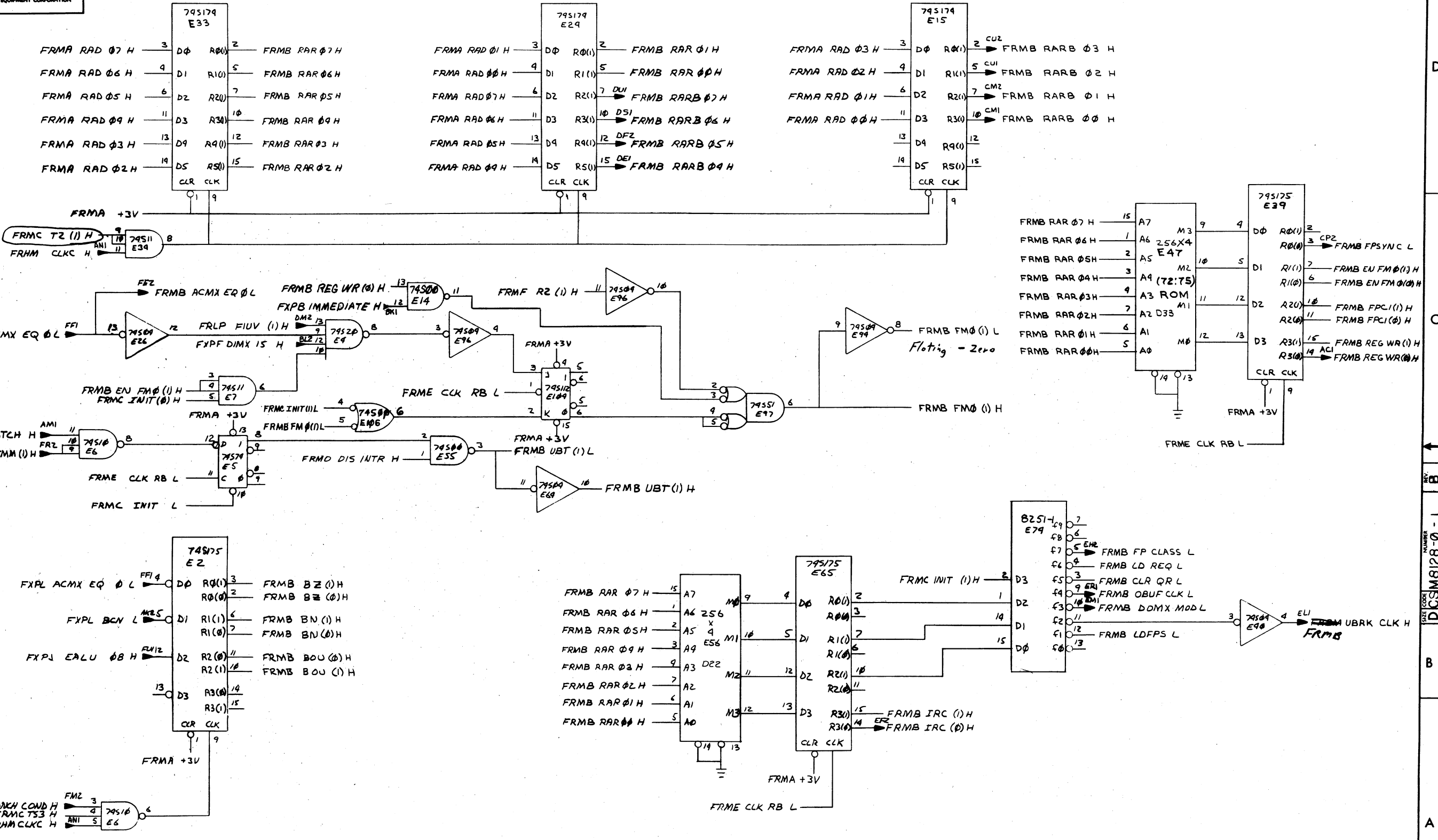
UAF1	UAF0	BRANCH ENABLE	MUX.
0	0	0	0
0	1	3:2	3:2
1	0	1:0	1:0
1	1	3:0	1

REVISIONS		
CHK	CHANGE NO.	REV.

(BRANCH CONTROL (SLOT 4))		TITLE	SIZE CODE	NUMBER	REV.
		FP ROM CONTROL (FRMA)	DCS	M8128-0-1	B
SCALE	SHEET	DIST.			
	2 OF 11				

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Rom Address Registers



REVISIONS			(UTRAP+ROM ADDRESS (SLOT 4))		TITLE	SIZE CODE	NUMBER	REV.
CHK	CHANGE NO.	REV.			FP ROM CONTROL (FRMB)	D CS	M8128-0-1	B
					SCALE	SHEET	3 OF 11	

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D

C

B

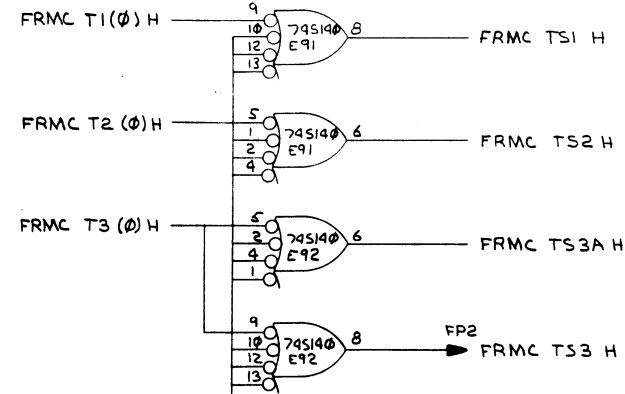
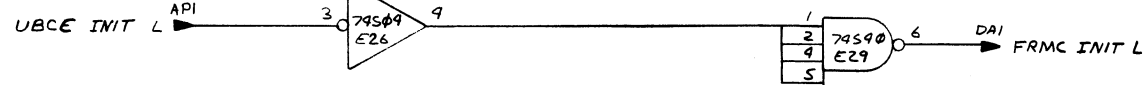
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D

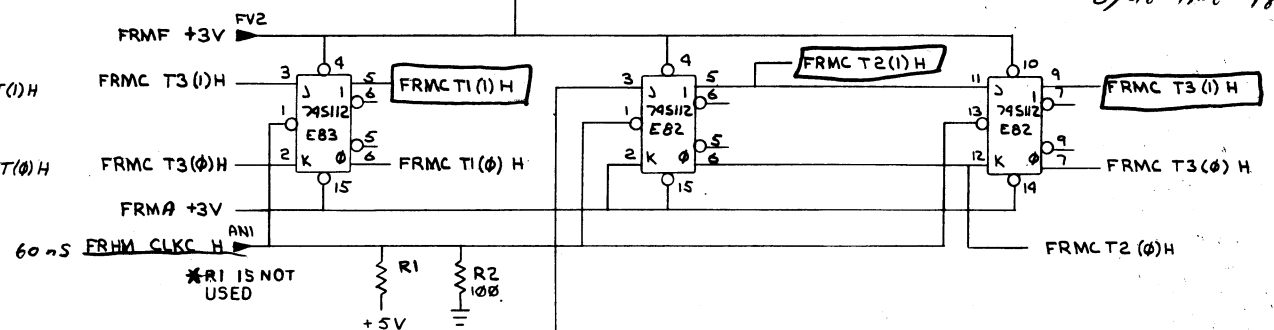
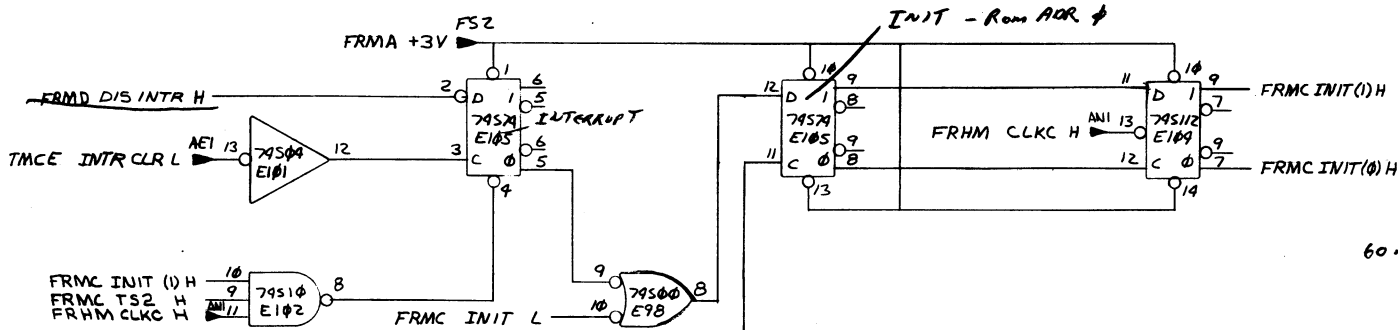
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B

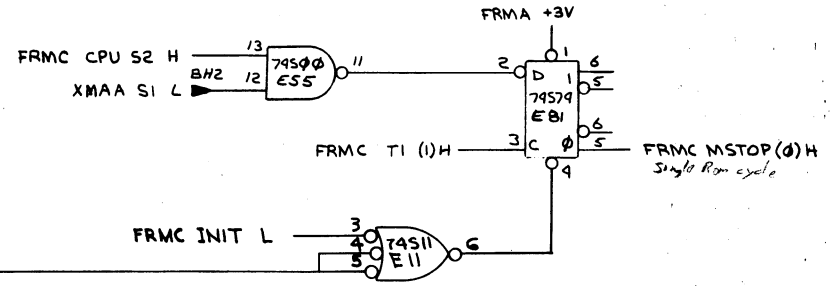
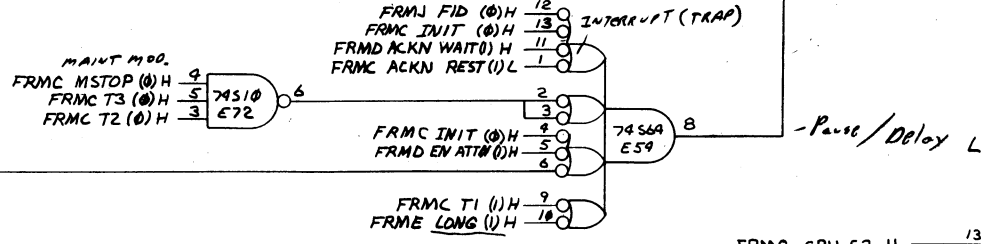
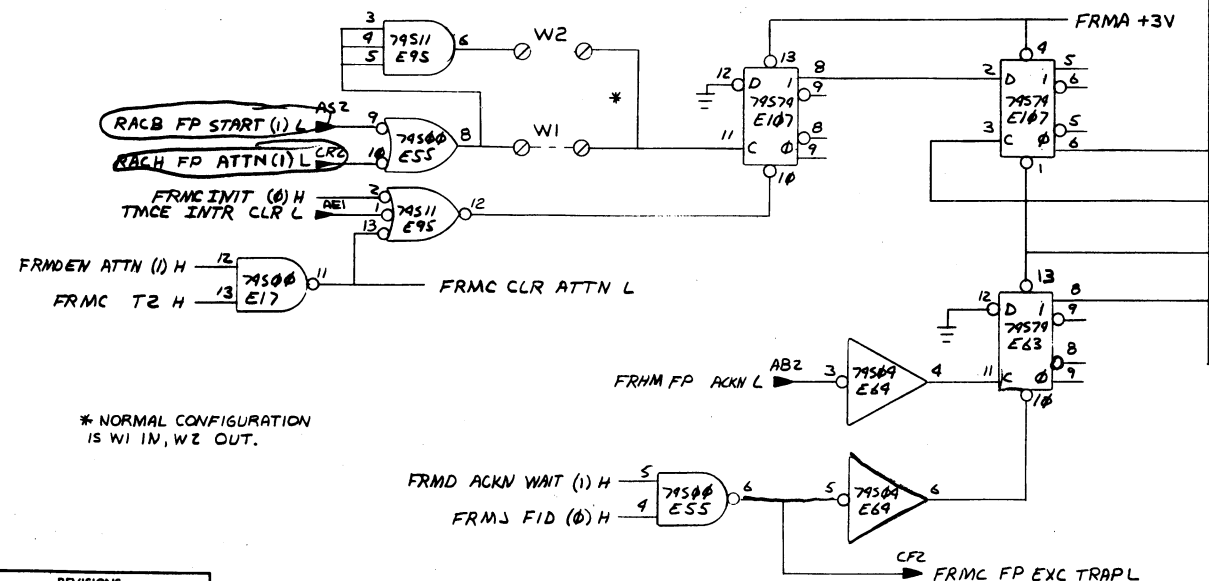
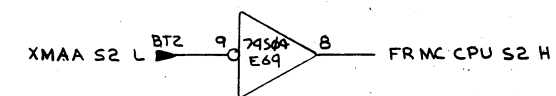
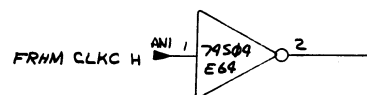
A



long cycle Time 240ns
cycle Time 180ns



*R1 IS NOT USED
+5V
R1
R2
100Ω



* NORMAL CONFIGURATION IS W1 IN, W2 OUT.

(TIMING AND SYNCHRONIZER) (SLOT 4)

CHK	CHANGE NO.	REV.

TITLE	SIZE CODE	NUMBER	REV.
FP ROM CONTROL (FRMC)	D	CSM8128-0-1	B
SCALE	SHEET	OF	
—H—	4	OF 11	

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D

C

B

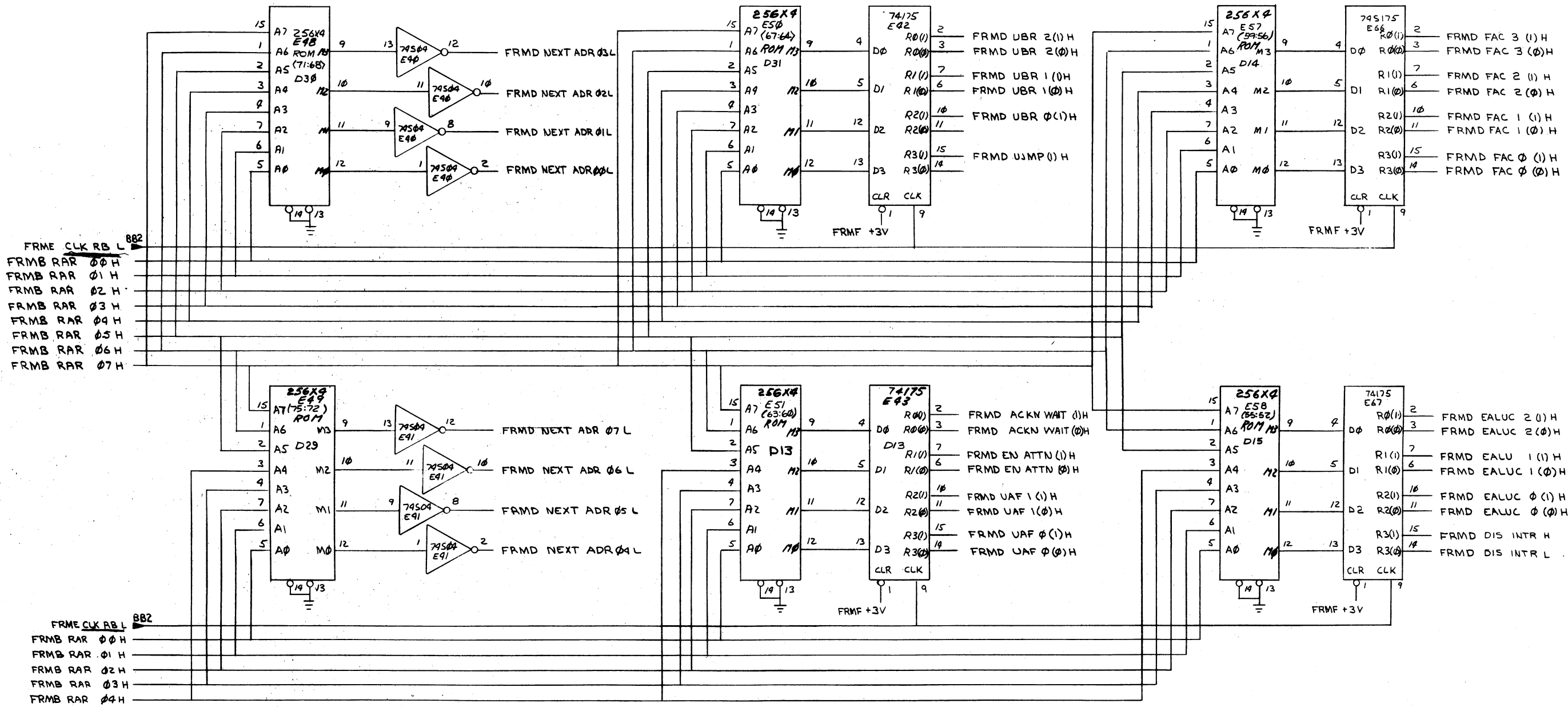
A

D

C

B

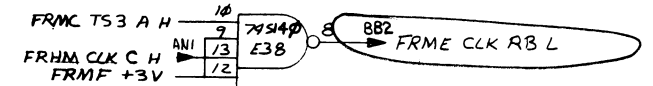
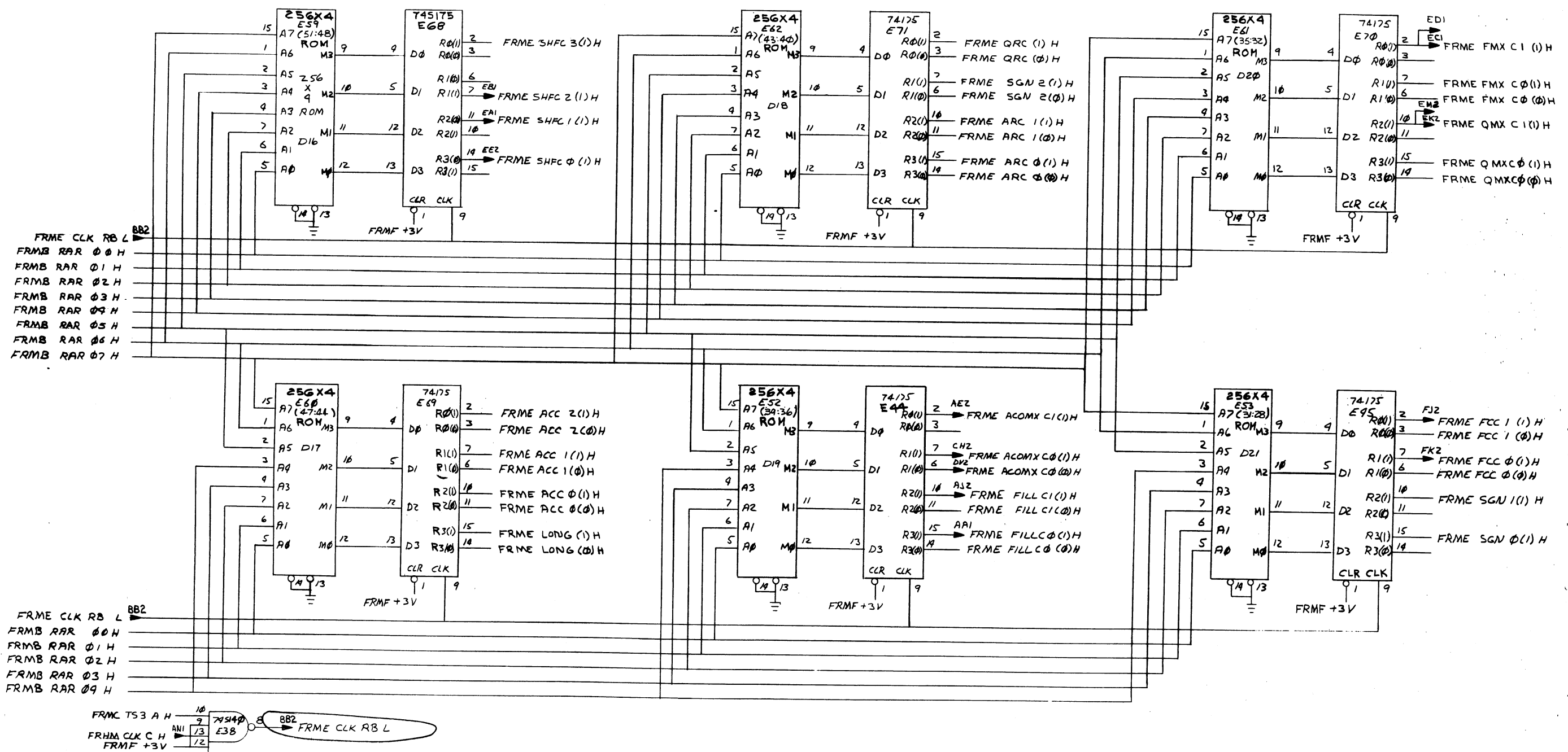
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REVISIONS		
CHK	CHANGE NO.	REV.

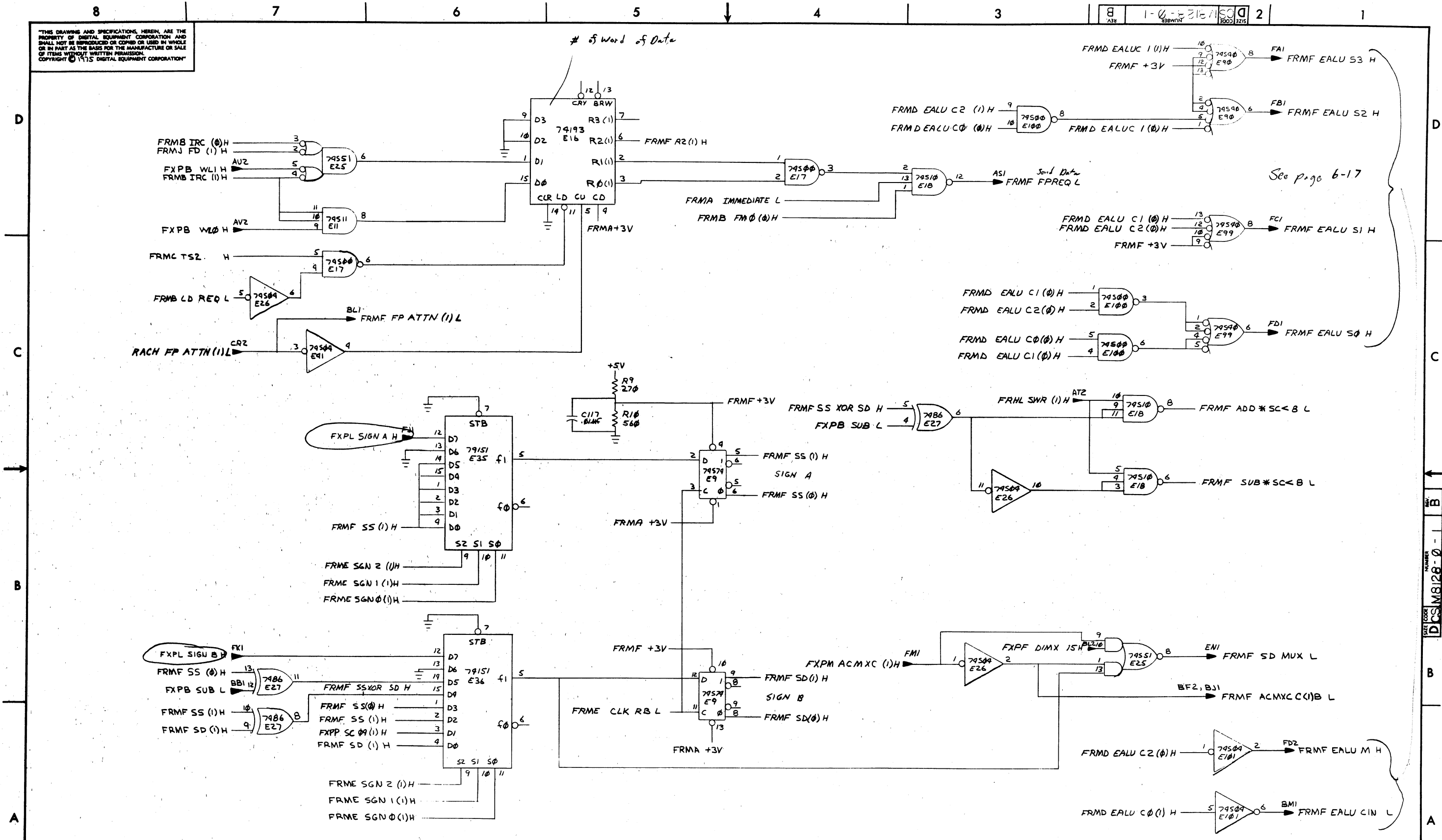
(CONTROL ROM)(SLOT 4)		TITLE	SIZE CODE	NUMBER	REV.
FP ROM CONTROL (FRMD)		DCS	M8128-0-1	B	
SCALE	SHEET 5 OF 11	DIST.			

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REVISIONS		
CHK	CHANGE NO.	REV.

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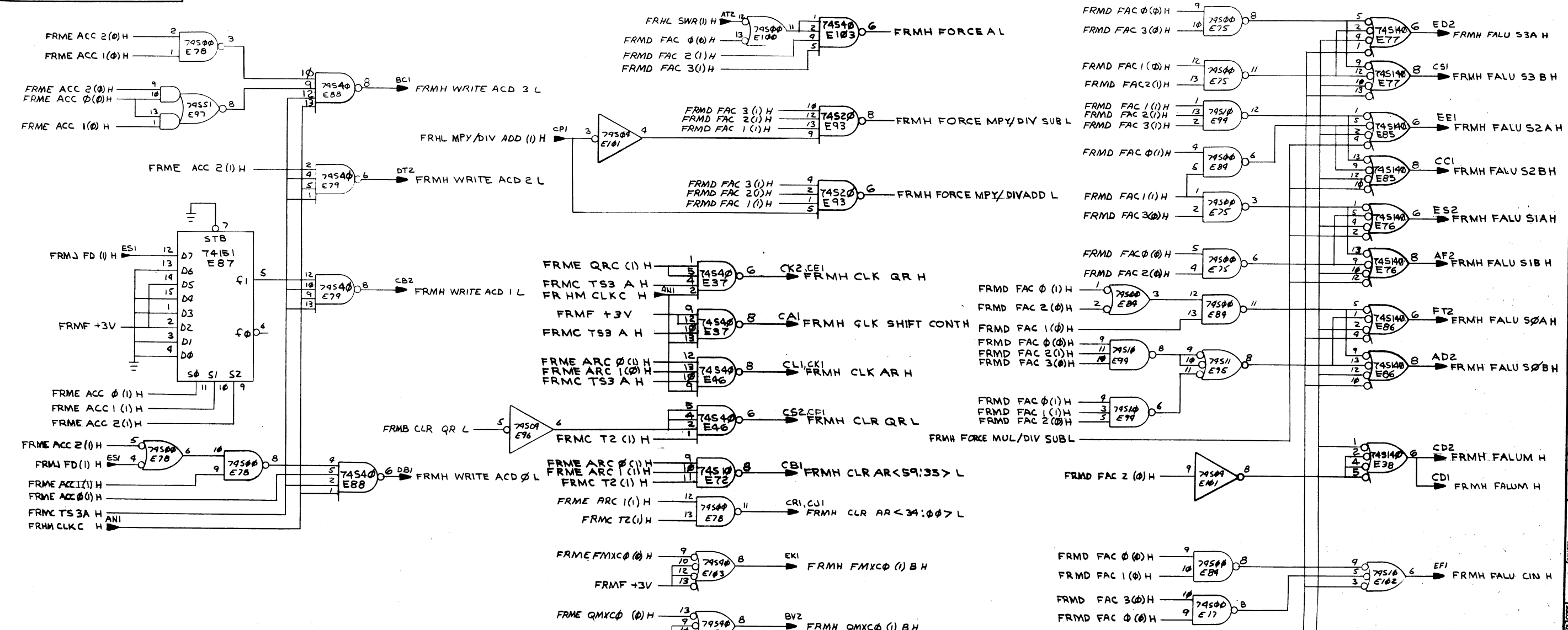


See page 6-17

REVISIONS													TITLE			SIZE CODE		NUMBER		REV.
CHK	CHANGE NO.	REV.											FP ROM CONTROL (FRMF)			D	CS	M8128-0-1	B	
													SCALE	//	SHEET	7	OF	11	DIST.	
8	7	6	5	4	3	2	1													

SIZE CODE NUMBER DCS M8128-0-1 B

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SCRATCH PAD WRITE PULSE CONTROL

FDX	ACC2	ACC1	ACC0	FUNCTION	WRITE ACD0	WRITE ACD1	WRITE ACD2	WRITE ACD3
X	0	0	0	NOP	NO	NO	NO	NO
X	0	0	1	WRITE ACD 0	YES	NO	NO	NO
X	0	1	0	WRITE ACD 1	NO	YES	NO	NO
X	0	1	1	WRITE ACD 3	NO	NO	YES	NO
X	1	0	0	WRITE ACD 2	NO	NO	YES	NO
X	1	0	1	WRITE ACD 3-0	YES	YES	YES	YES
X	1	1	0	WRITE ACD 3-2	NO	NO	YES	YES
0	1	1	1	WRITE ACD 3-0 IF FD(1) ELSE ACD 3-2	YES	YES	YES	YES

FALU CONTROL

MPY/DIV ADD	SWR	FAC3	FAC2	FAC1	FAC0	FUNCTION	S3	S2	S1	S0	M	CIN
X	X	0	0	0	0	A AND B	1	0	1	1	1	1
X	X	0	0	0	1	NOT A	0	0	0	1	1	0
X	X	0	0	1	0	A OR B	1	0	1	0	1	0
X	X	0	1	0	0	A PLUS B	0	1	1	1	1	0
X	X	0	1	1	0	A PLUS PLUS 1	1	0	0	1	0	0
X	X	0	1	1	1	A MINUS 1	1	1	1	1	0	0
X	X	0	1	1	1	A MINUS B	0	1	1	1	0	0
X	X	1	0	0	0	NOT (A AND B)	0	1	0	0	1	0
X	X	1	0	0	1	NOT (A OR B)	0	1	0	0	1	0
X	X	1	0	1	0	NOT B	0	1	0	1	1	0
X	0	1	1	0	0	COND A	1	1	1	1	1	1
X	0	1	1	0	1	ADD A PLUS B	1	0	0	1	0	1
X	X	1	1	0	1	NOT USED	1	1	1	1	1	1
0	0	1	1	1	0	MPY/DIV A	1	1	1	1	1	1
0	0	1	1	1	1	MPY/DIV A MINUS B	0	1	1	1	0	0
0	0	1	1	1	1	MPY/DIV A	1	1	1	1	1	1
0	0	1	1	1	1	MPY/DIV A PLUS B	1	1	1	1	1	1
X	X	1	1	1	1	A	1	1	1	1	1	1

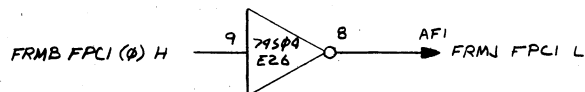
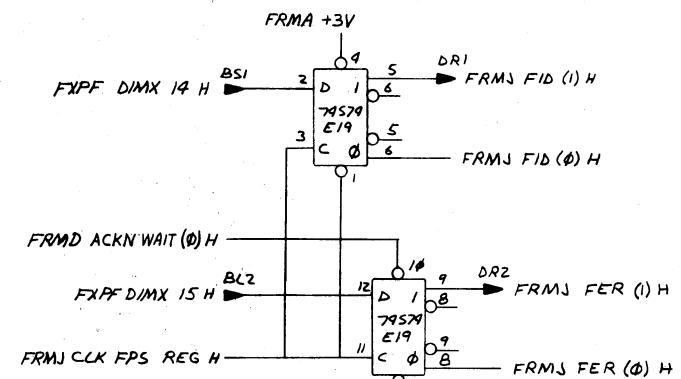
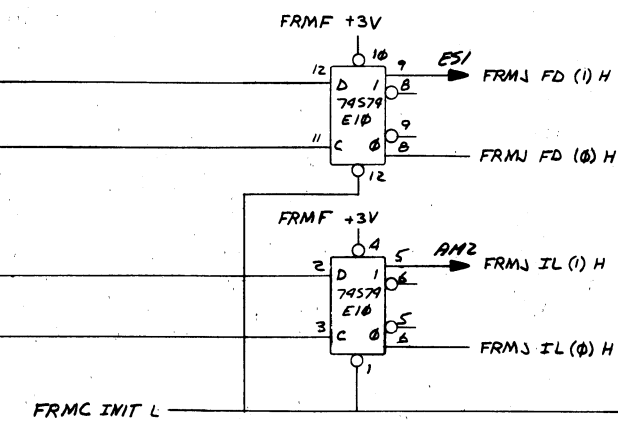
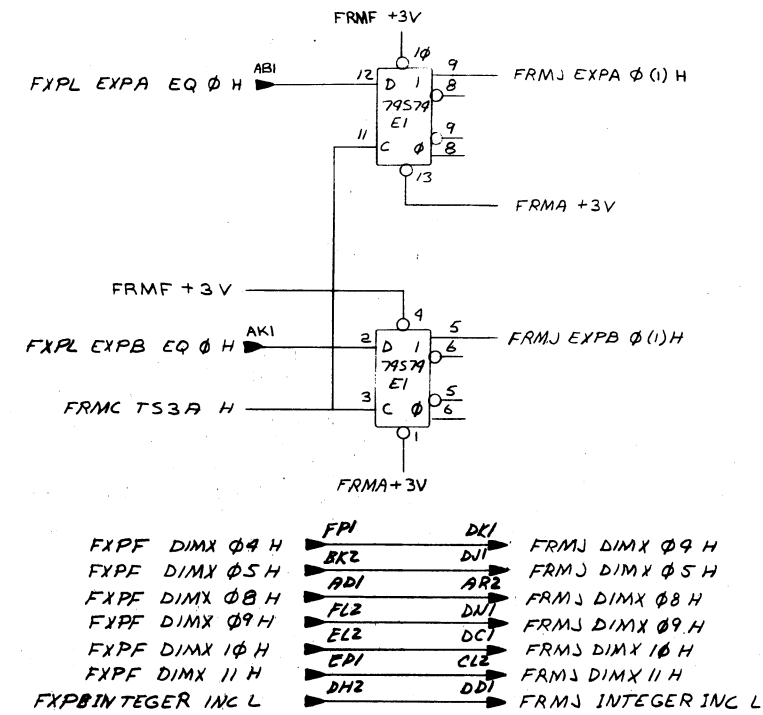
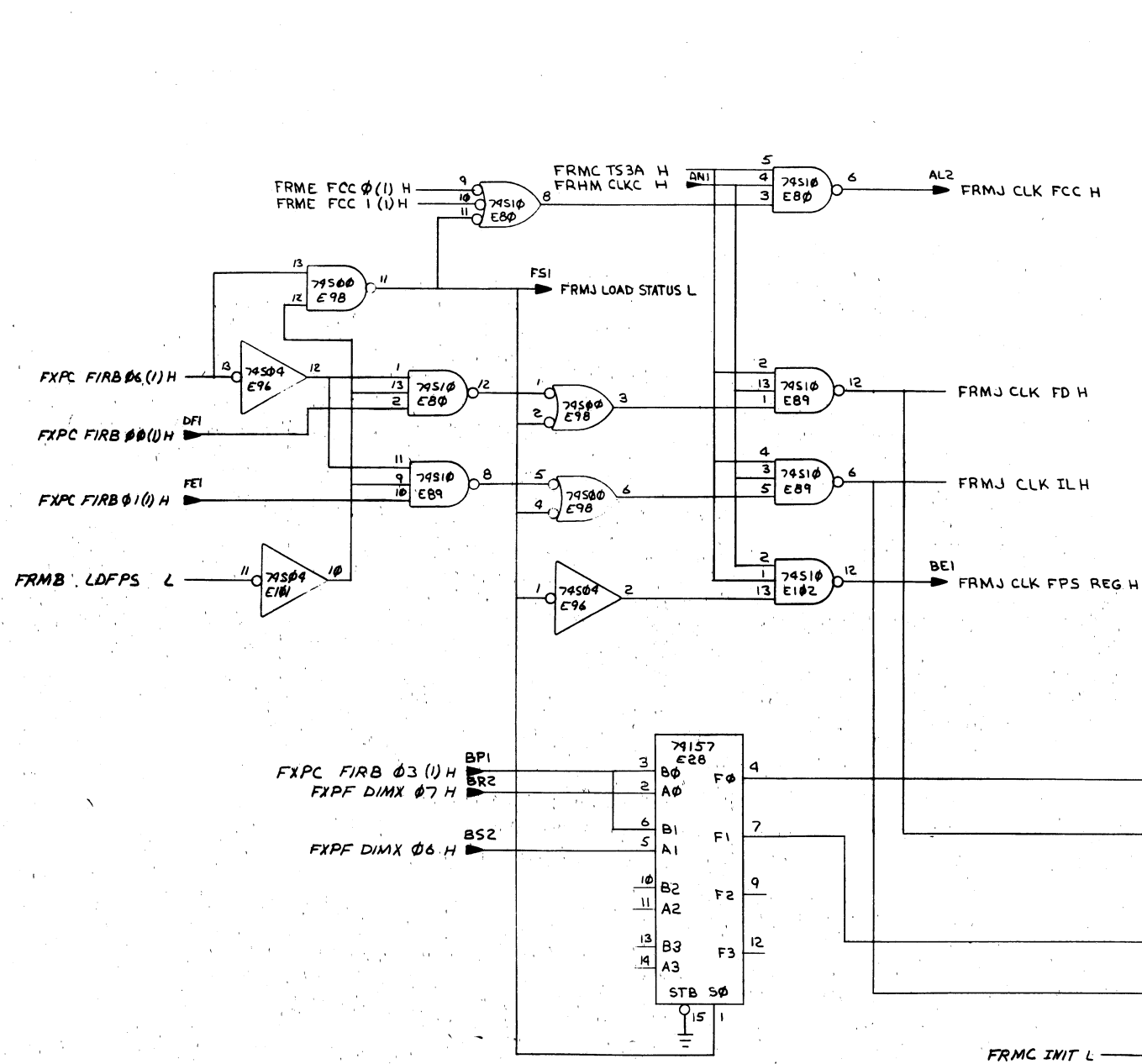
REGISTER CLOCKS, FALU CONTROL (SLOT 4)

REVISIONS

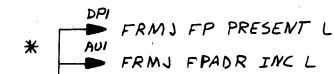
CHK	CHANGE NO.	REV.

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NOTE:
SIGNAL NEW ORIGIN
FRMJ FP SYNC L FRMB FP SYNC L



* THESE GNDS ARE GENERATED ON THE ETCH BOARD



REVISIONS		
CHK	CHANGE NO.	REV.

(FPS CONTROL (SLOT 4))

TITLE	SIZE CODE	NUMBER	REV.
FP ROM CONTROL (FRMJ)	D CS M8128 0 1		B
SCALE	SHEET	OF	DIST.
	9	11	

REV. B
NUMBER DCS M8128-0-1

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D

C

B

A

D

C

B

A

NAD UBR UJP AKW ATM UAF FAC EAC DSI SMC ACC LNG ORC SNM ARC ACO FIL FMX QMX FCC SNL MSC IRC SYN FMB FCI RGM ANX BNH DIM SCC ERC ACF ACX CNT PGE

Table of data points for ROM control, including item numbers (e.g., 054 126, 055 003) and their corresponding values across various parameters.

NAD UBR UJP AKW ATM UAF FAC EAC DSI SMC ACC LNG ORC SNM ARC ACO FIL FMX QMX FCC SNL MSC IRC SYN FMB FCI RGM ANX BNH DIM SCC ERC ACF ACX CNT PGE

Table of data points for ROM control, continuing from the previous section with item numbers (e.g., 130 000, 131 000) and their corresponding values.

REVISIONS table with columns for CHK, CHANGE NO., and REV.

Form containing TITLE (FP ROM CONTROL), SIZE CODE (DCS M8128-0-1), NUMBER, and REV. (B) information.

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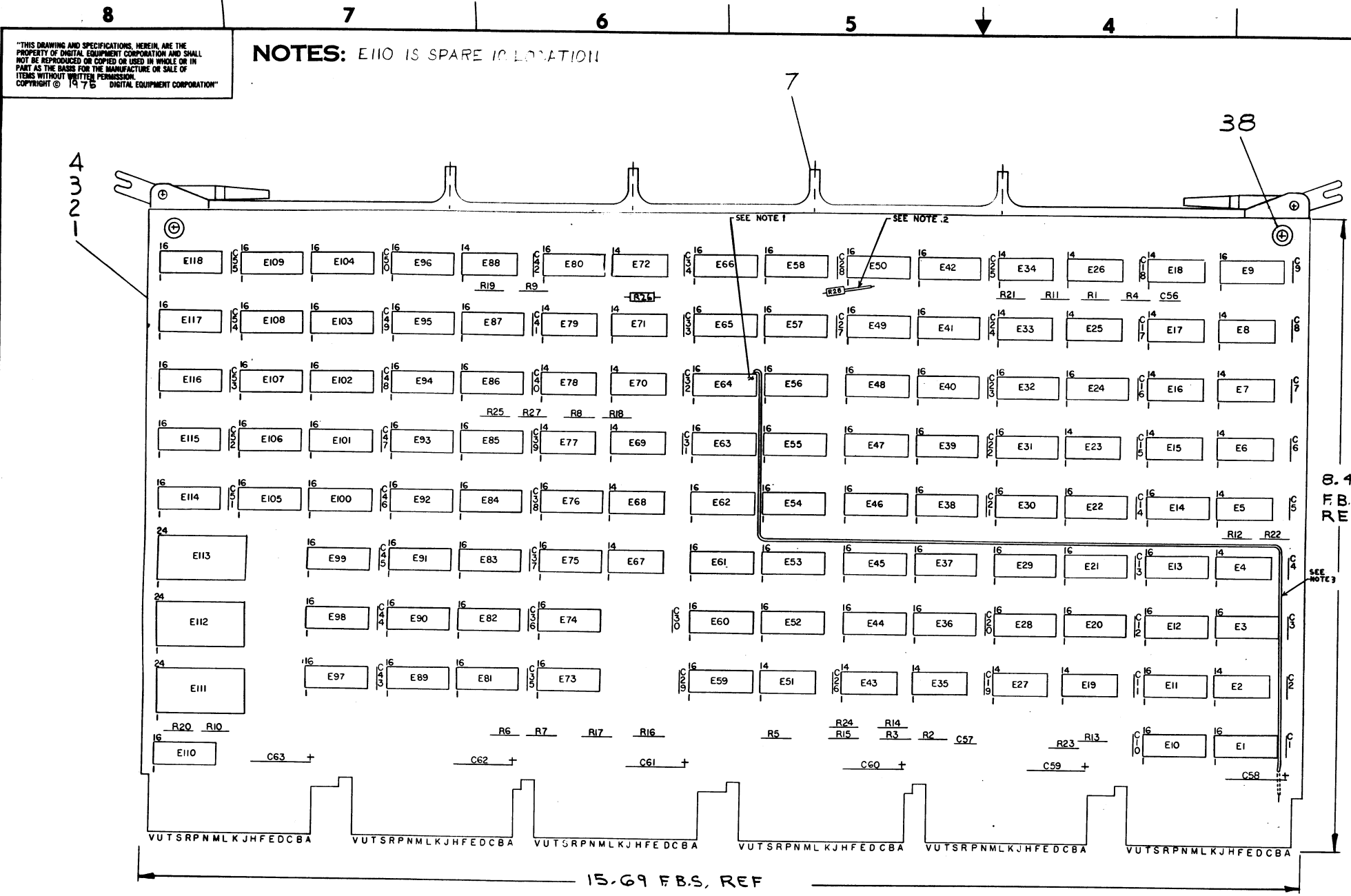
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Table with columns: NAD, UBR, UJP, AKH, ATH, UAF, FAC, EAC, DSI, SMC, ACC, LNG, QRC, SNH, ARC, ACO, FIL, FMX, DMX, FCC, SNL, MSC, IRC, SYN, FMB, FC1, RGH, AMX, BMX, DIM, SCC, ERC, ACF, ACX, CNT, PGE. Rows 204-233, 236-239, 240-243, 244-247, 250-253, 254-257, 258-261, 262-265, 266-269, 270-273, 274-277, 278-281, 282-285, 286-289, 290-293, 294-297, 298-301, 302-305, 306-309, 310-313, 314-317, 318-321, 322-325, 326-329, 330-333.

Table with columns: NAD, UBR, UJP, AKH, ATH, UAF, FAC, EAC, DSI, SMC, ACC, LNG, QRC, SNH, ARC, ACO, FIL, FMX, DMX, FCC, SNL, MSC, IRC, SYN, FMB, FC1, RGH, AMX, BMX, DIM, SCC, ERC, ACF, ACX, CNT, PGE. Rows 334-337, 340-343, 344-347, 350-353, 354-357, 360-363, 364-367, 370-373, 374-377.

REVISIONS table with columns: CHK, CHANGE NO., REV.

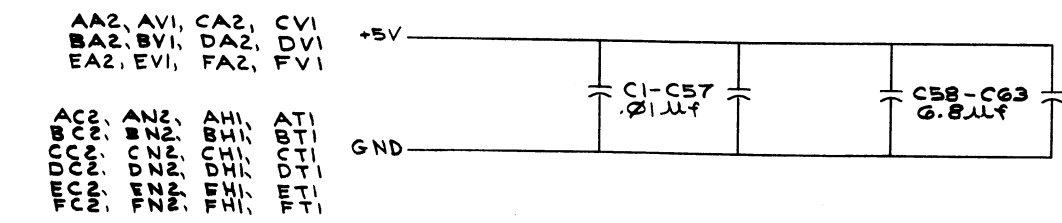
Table with columns: TITLE (FP ROM CONTROL), SIZE CODE (DCS), NUMBER (M8128-0-1), REV. (B), SHEET (11 OF 11), DIST.



IC 74S182	8	16
IC 74S133	8	16
IC 74S175	8	16
IC 74157	8	16
IC 74174	8	16
IC 74175	8	16
IC 74S174	8	16
IC 74S158	8	16
IC 74S153	8	16
IC 74S181	12	24
IC 7485	8	16
IC 74153	8	16
IC 74151	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14
RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS



REF	DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.
REF	X-Y COORDINATE HOLE LOCATION	K-CO-M8129-B-4		1
REF	ASSY/DRILLING HOLE LAYOUT	D-AH-M8129-B-5		2
REF	MODULE ECO HISTORY	B-MH-M8129-B-6		3
1	ETCHED CIRCUIT BOARD	5011873		4
57	C1 THRU C57	CAPACITOR, .01µf	1001610-00	5
6	C58 THRU C63	CAPACITOR, 6.8µf	1005306	6
1	HANDLE HEX MODULE	1210711-2		7
12	R5 THRU R14, R25, R27	RESISTOR, 330 OHM, 1/4W, 5%	1300295	8
2	R3, R4	RESISTOR, 560 OHM, 1/4W, 5%	1300890	9
10	R15 THRU R24	RESISTOR, 680 OHM, 1/4W, 5%	1301424	10
2	R1, R2	RESISTOR, 270 OHM, 1/4W, 5%	1301972	11
1	R26	RES, 100Ω, 1/4W, 5%	1300229	12
2	E33, E69	I.C. DEC 8242	1909712	13
1	E84	I.C. DEC 74151	1909936	14
8	E45 THRU E48, E53 THRU E56	I.C. DEC 74153	1909937	15
2	E42, E50	I.C. DEC 7485	1910224	16
3	E111 THRU E113	I.C. DEC 74S181	1910531	17
5	E7, E9, E15, E43, E80	I.C. DEC 74S88	1910532	18
2	E23, E99	I.C. DEC 74S84	1910534	19
6	E2, E4, E5, E19, E27, E35	I.C. DEC 74S85	1910535	20
5	E16, E67, E70, E71, E78	I.C. DEC 74S18	1910536	21
3	E25, E72, E79	I.C. DEC 74S11	1910537	22
3	E51, E68, E88	I.C. DEC 74S28	1910539	23
3	E6, E8, E18	I.C. DEC 74S148	1910546	24
17	E21, E22, E29 THRU E31, E37, E38, E39, E104 THRU E107, E114 THRU E118	I.C. DEC 74S153	1910547	25
1	E26	I.C. DEC 74S74	1910544	26
1	E17	I.C. DEC 74SG4	1910542	27
5	E20, E28, E36, E100, E102	I.C. DEC 74S174	1910550	28
11	E14, E17, E18, E20, E21, E22, E23, E24, E25, E26, E27, E28, E29, E30, E31, E32, E33, E34, E35, E36, E37, E38, E39, E40, E41, E42, E43, E44, E45, E46, E47, E48, E49, E50, E51, E52, E53, E54, E55, E56, E57, E58, E59, E60, E61, E62, E63, E64, E65, E66, E67, E68, E69, E70, E71, E72, E73, E74, E75, E76, E77, E78, E79, E80, E81, E82, E83, E84, E85, E86, E87, E88, E89, E90, E91, E92, E93, E94, E95, E96, E97, E98, E99, E100, E101, E102, E103, E104, E105, E106, E107, E108, E109, E110, E111, E112, E113, E114, E115, E116, E117, E118	I.C. DEC 74175	1910651	29
9	E14, E17, E18, E20, E21, E22, E23, E24, E25, E26, E27, E28, E29, E30, E31, E32, E33, E34, E35, E36, E37, E38, E39, E40, E41, E42, E43, E44, E45, E46, E47, E48, E49, E50, E51, E52, E53, E54, E55, E56, E57, E58, E59, E60, E61, E62, E63, E64, E65, E66, E67, E68, E69, E70, E71, E72, E73, E74, E75, E76, E77, E78, E79, E80, E81, E82, E83, E84, E85, E86, E87, E88, E89, E90, E91, E92, E93, E94, E95, E96, E97, E98, E99, E100, E101, E102, E103, E104, E105, E106, E107, E108, E109, E110, E111, E112, E113, E114, E115, E116, E117, E118	I.C. DEC 74174	1910652	30
1	E94	I.C. DEC 74157	1910655	31
4	E64, E75, E89, E91	I.C. DEC 74S175	1910957	32
2	E34, E77	I.C. DEC 74S51	1911712-88-S	33
1	E12	I.C. DEC 74S133	1911983-88-S	34
3	E44, E52, E86	I.C. DEC 74S158	1910549	35
6	E1, E3, E10, E11, E13, E14	I.C. DEC 74S189	1912661	36
1	E98	I.C. DEC 74S182	1912097	37
12	EYELET			38
1	E63	ROM	9006732	38
1	E65	ROM	23D28A2	39
1	E66	ROM	23D28A2	40
1	E87	ROM	23D27A2	41
1	E93	ROM	23D81A2	42
1	E93	ROM	23D82A2	43
1	E96	ROM	23D83A2	44
1	E95	ROM	23D84A2	45
1	E85	ROM	23D85A2	46
1	E108	ROM	23D87A2	47
1	E109	ROM	23D88A2	48
1	E59	ROM	23D24A2	49
1	E61	ROM	23D25A2	50
1	R28	RES 150Ω 1/4W 5%	1300250	51
A/R		WIRE, 30AWG.	9105740-B5	52
A/R		TUBING	9107278-01	53

DEC FORM NO. DRD 135-B

FIRST USED ON OPTION MODEL
FP11-C

ETCH BOARD REV.	C
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DRN.	DATE
CHK'D.	DATE
PROJ. ENG.	DATE
PROD.	DATE

digital

TITLE
FRACTION PROC
EXPON PATH

SCALE
1 OF 15

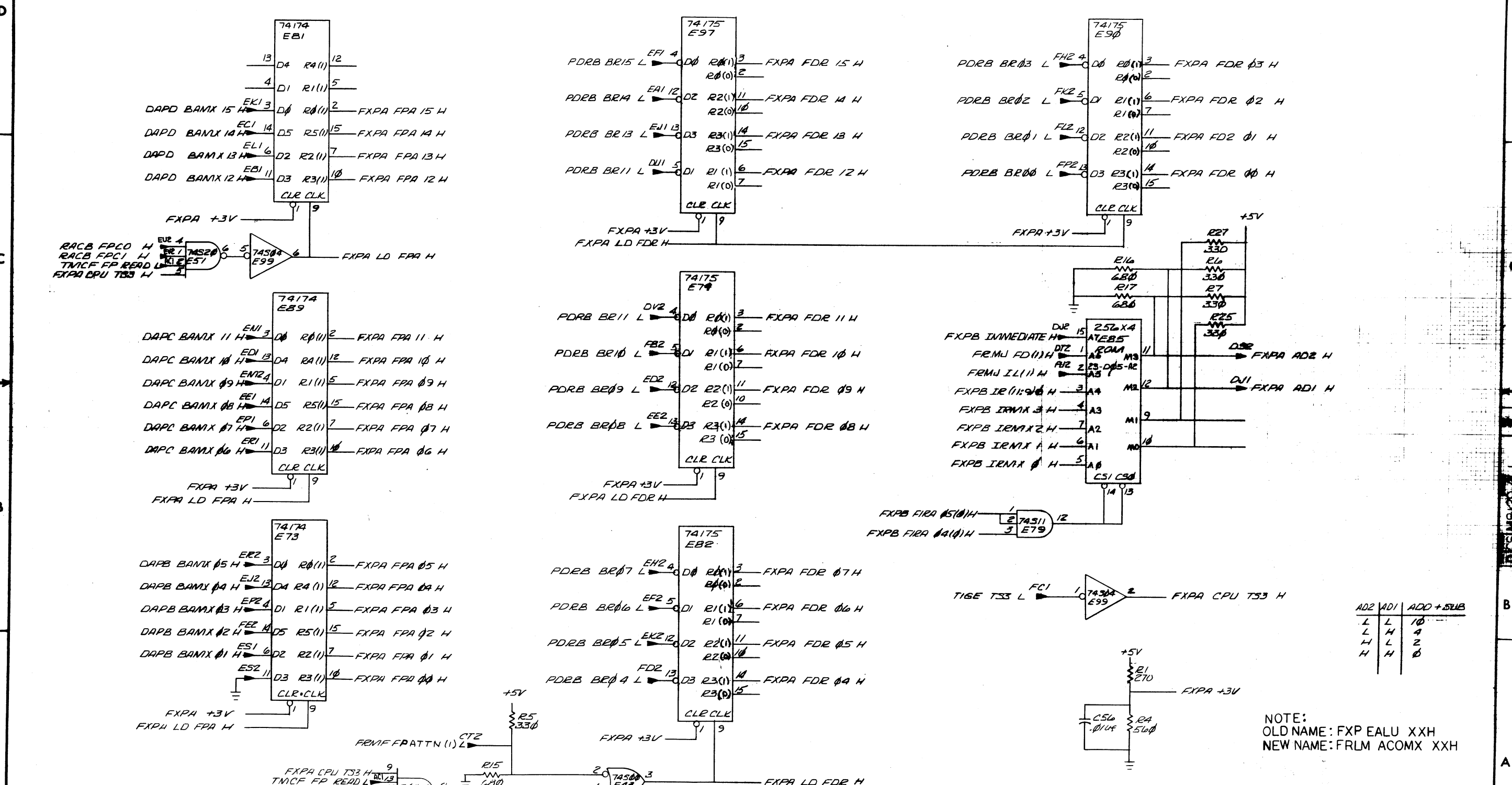
SEMICONDUCTOR CONVERSION CHART

DEC NO. EIA NO. DEC NO. EIA NO.

SIZE CODE NUMBER
D|CS M8129-0-1

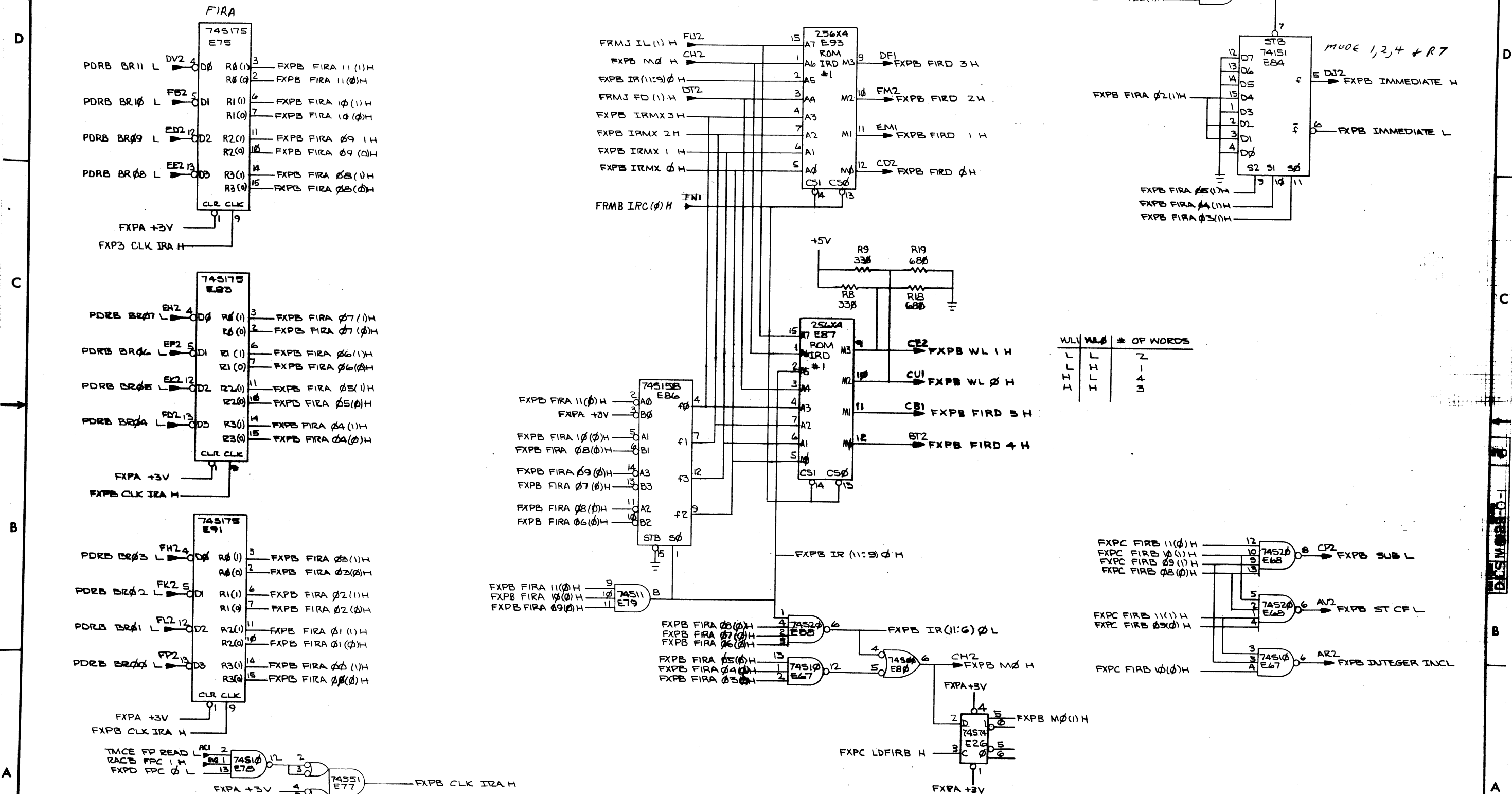
REV. B

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REVISIONS		
CHK	CHANGE NO.	REV.

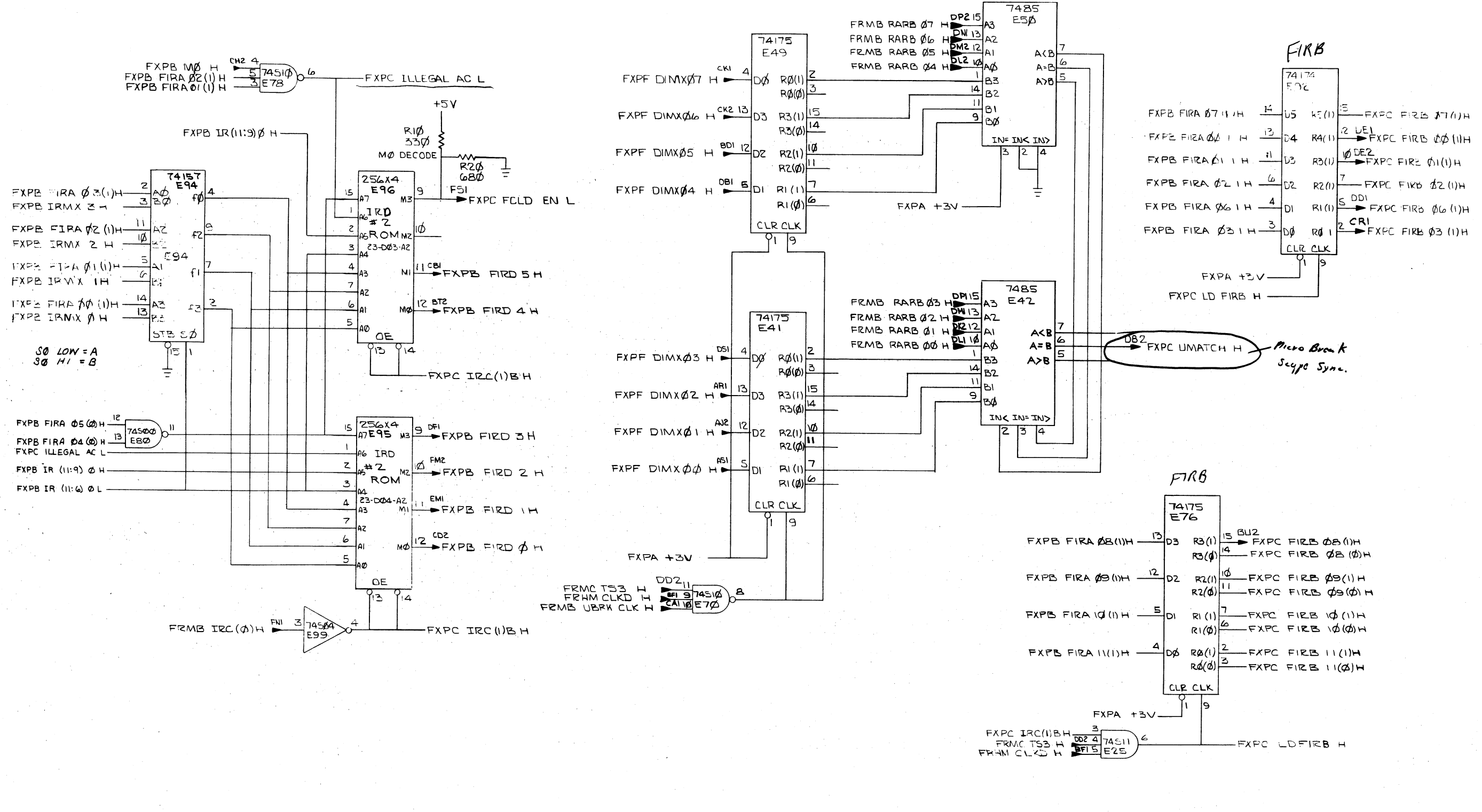
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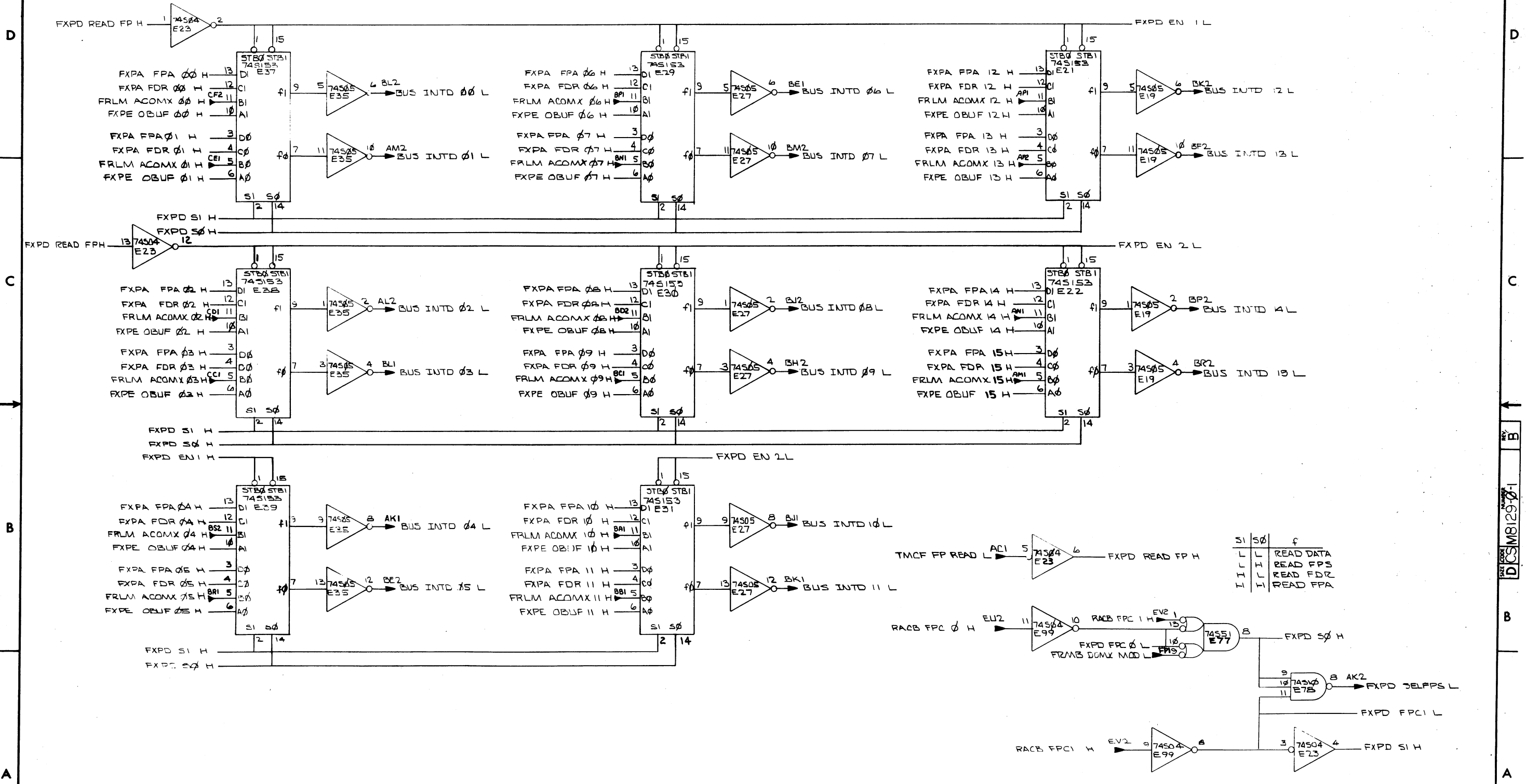
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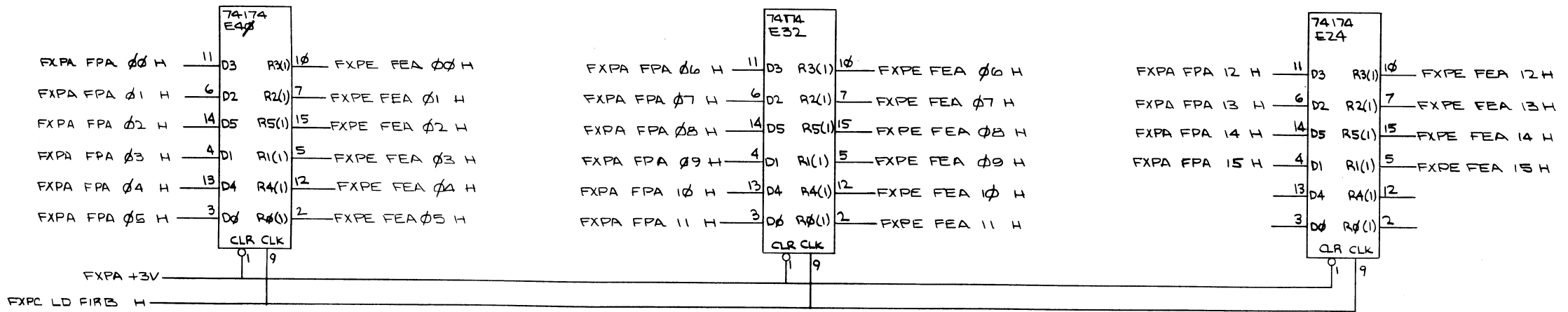
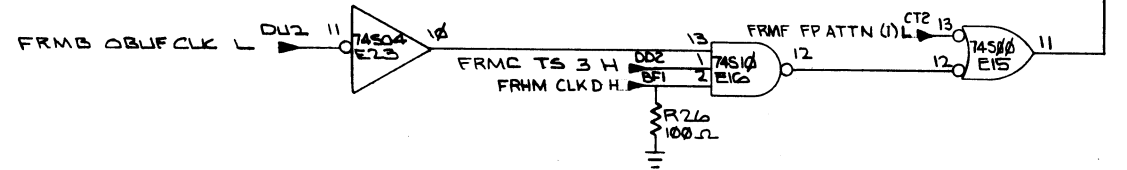
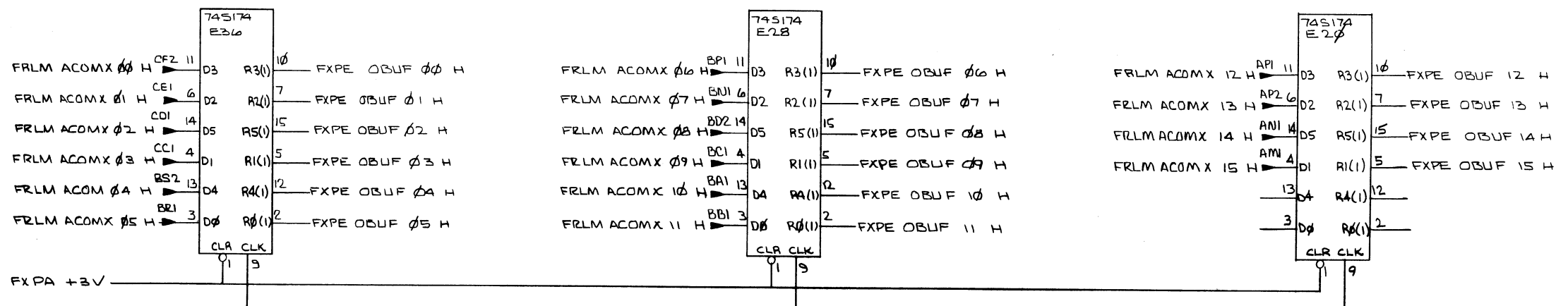
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CHK	CHANGE NO.	REV.

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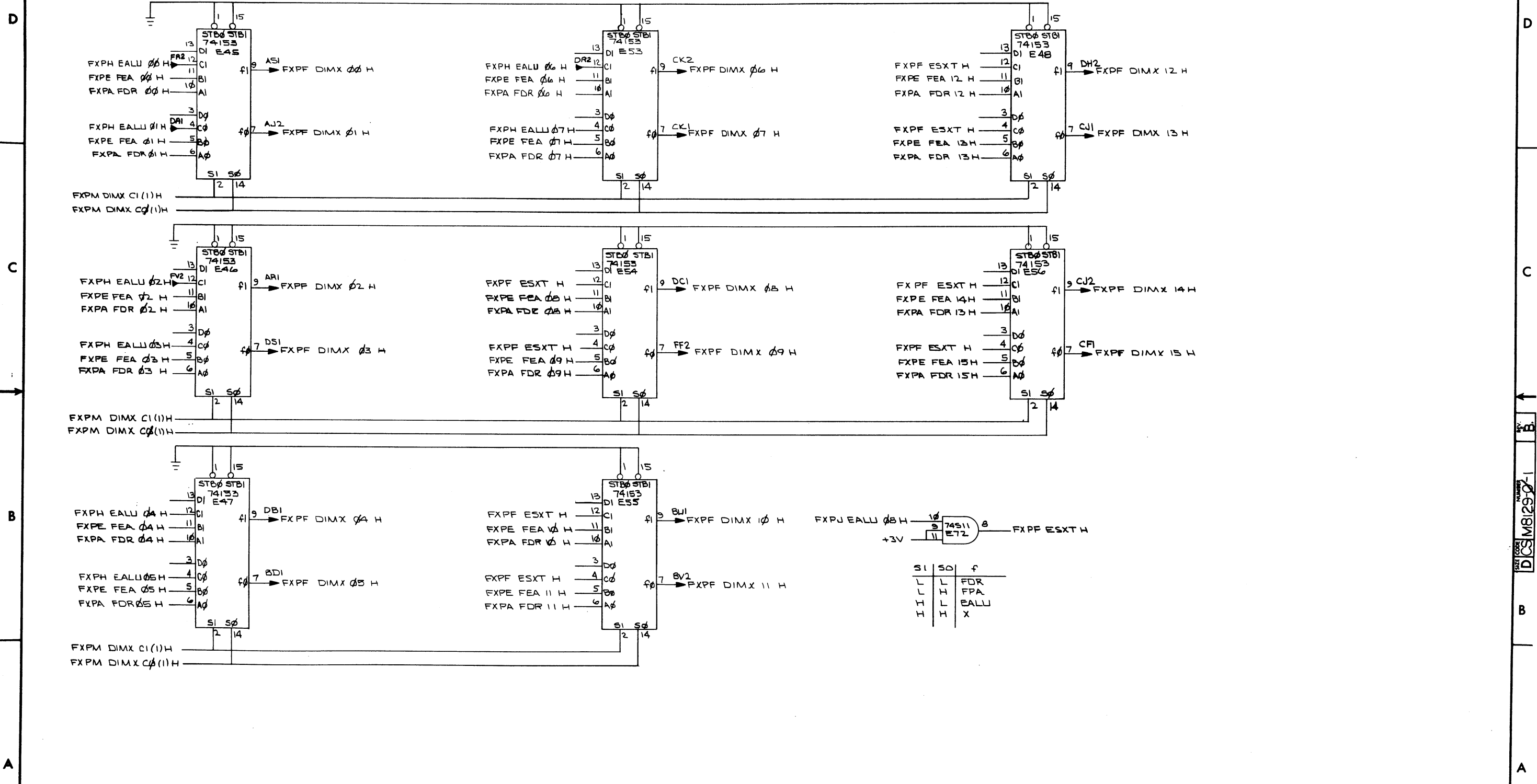
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REVISIONS		
CHK	CHANGE NO.	REV.

DEC FORM NO. 500 128

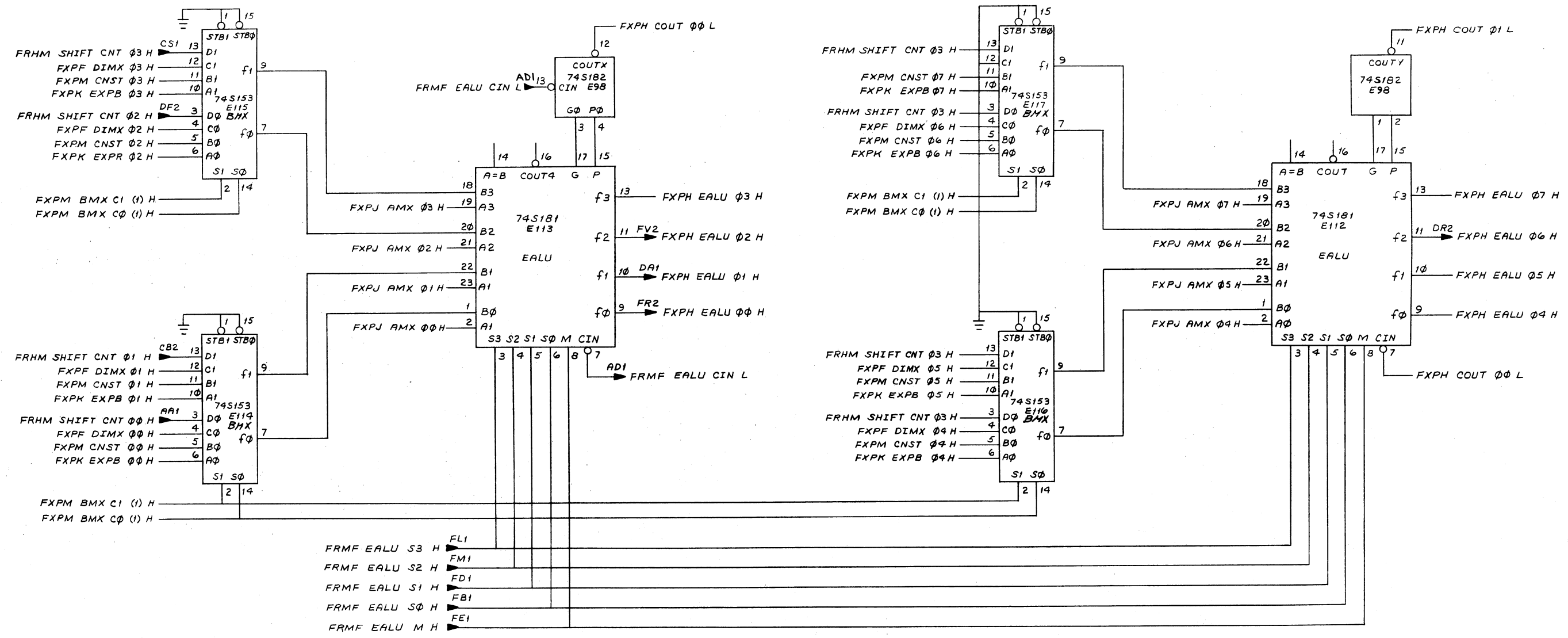
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REVISIONS		
CHK	CHANGE NO.	REV.

TITLE FRACTION PROC. EXPON. PATH. (FXPF)		SIZE CODE D	NUMBER CS M8129-0-1	REV. B
SCALE 1/1	SHEET 7	OF 15	DIST.	

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BMX	SI	S0	f
L	L		EXP
L	H		CNST
H	L		DIMX
H	H		SHIFT CONT.

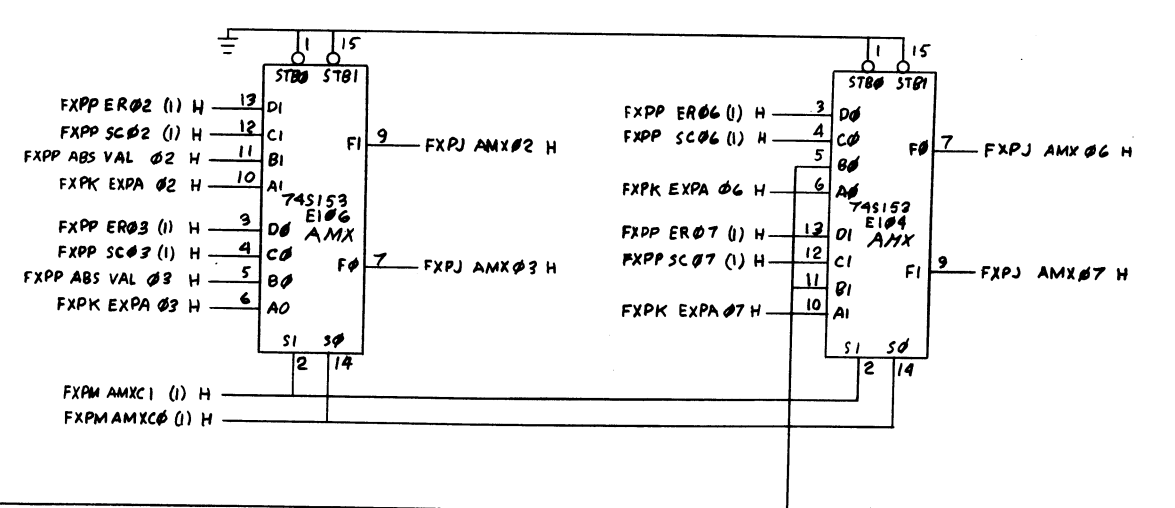
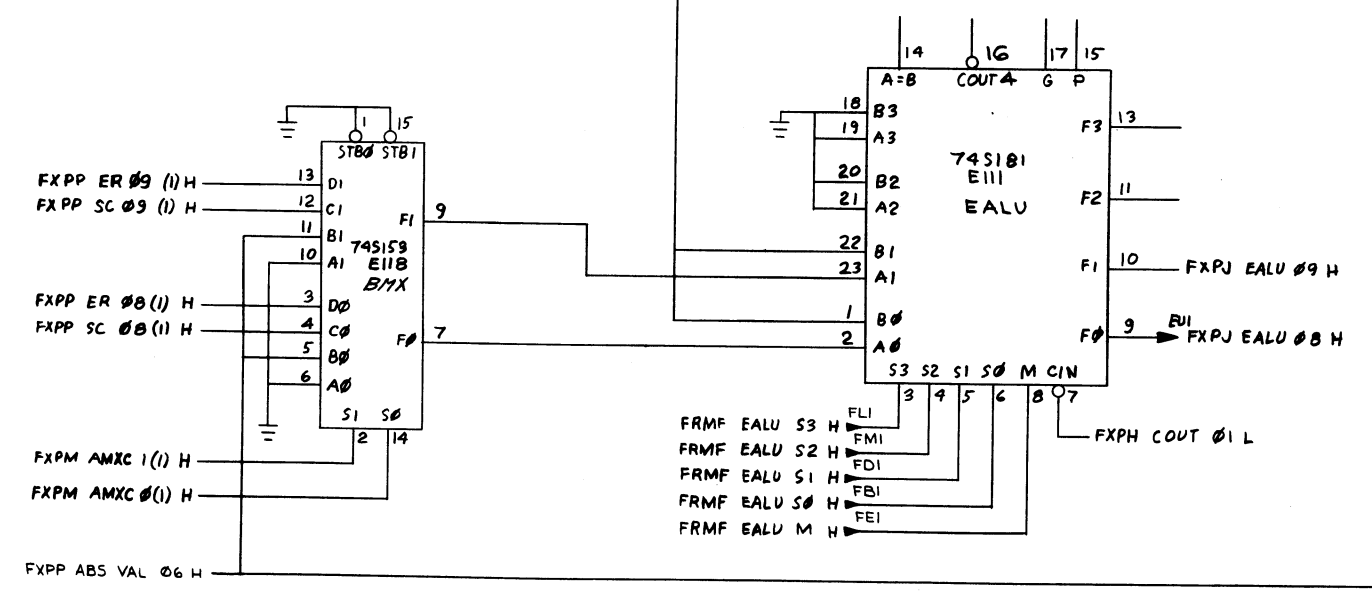
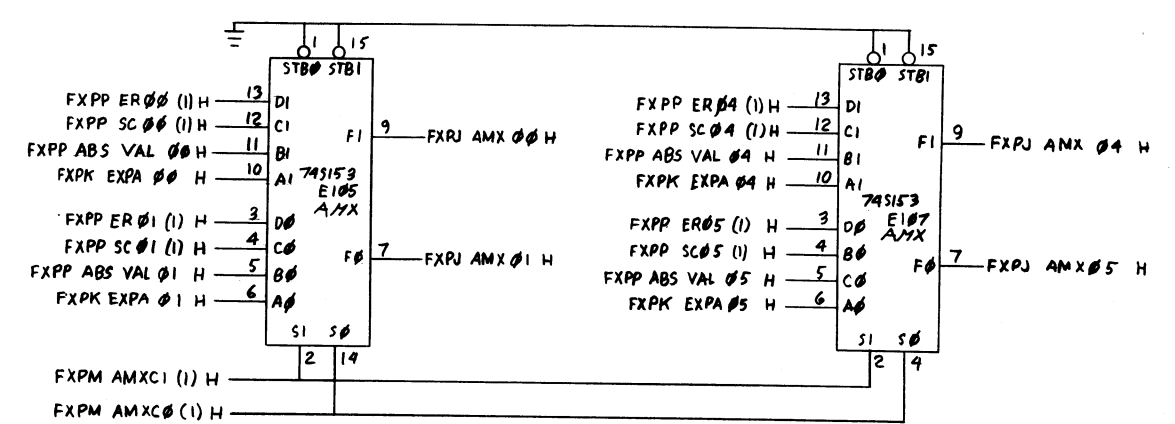
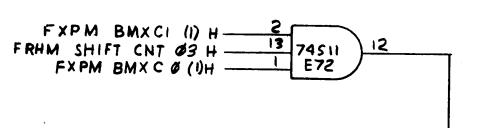
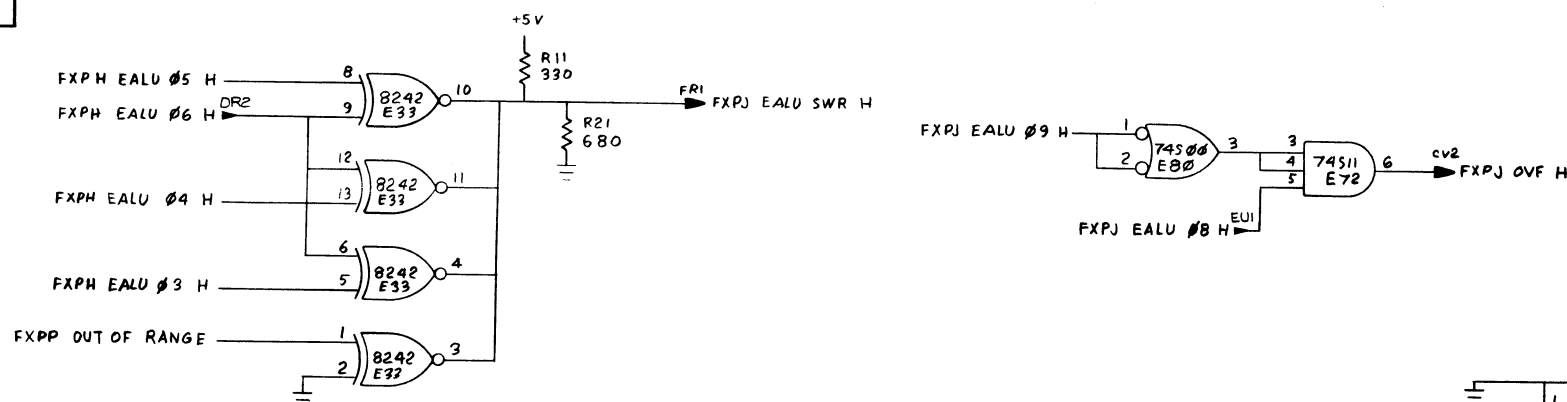
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- FRMF EALU S2 H FM1
- FRMF EALU S1 H FD1
- FRMF EALU S0 H FB1
- FRMF EALU M H FE1

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE FRACTION PROC. EXPON. PATH (FXPH)		SIZE CODE DCS	NUMBER M8129-0-1	REV. B
SCALE	SHEET 8 OF 15	DIST.		

(EALU LOW (SLOT 5))

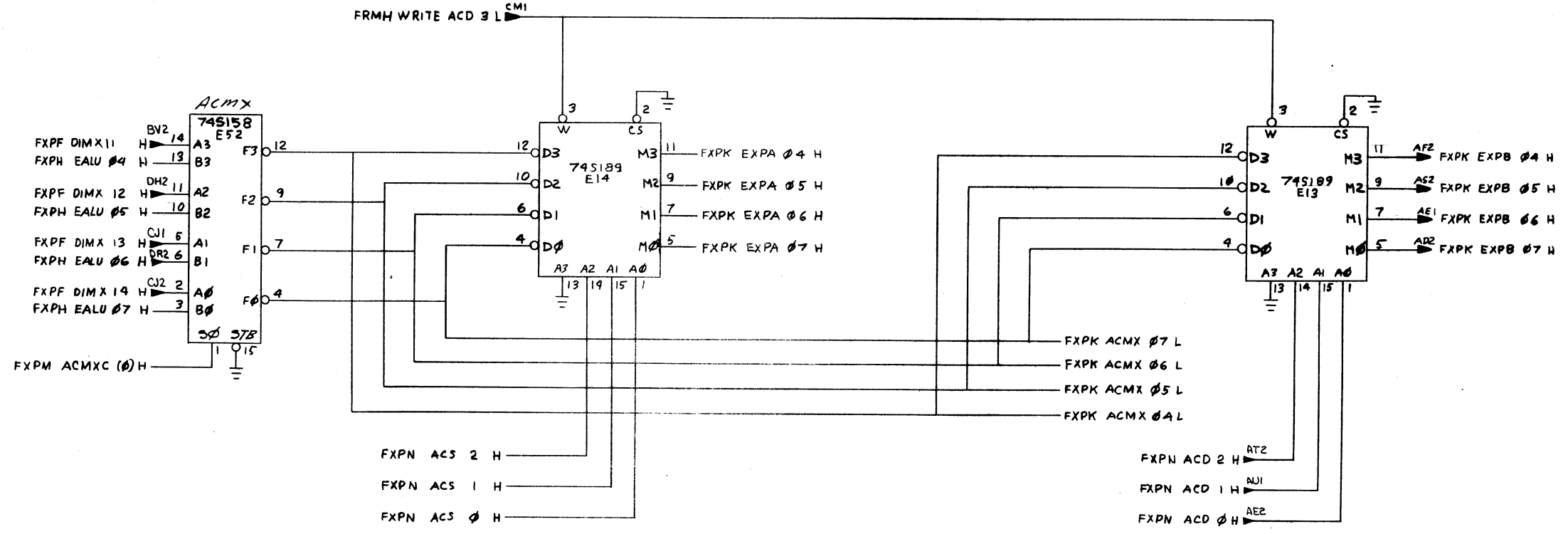
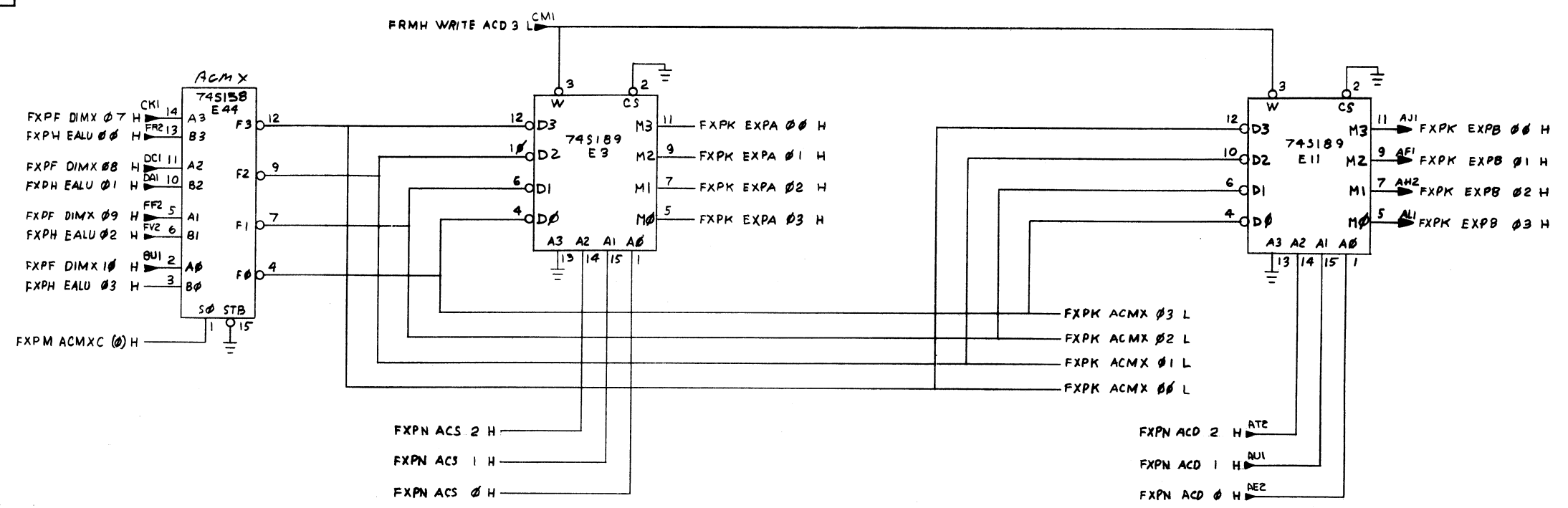
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AMX	S1	S0	F
L	L	L	EXP
L	H	L	ABS SC
H	L	L	SC
H	H	L	ER

REVISIONS		
CHK	CHANGE NO.	REV.

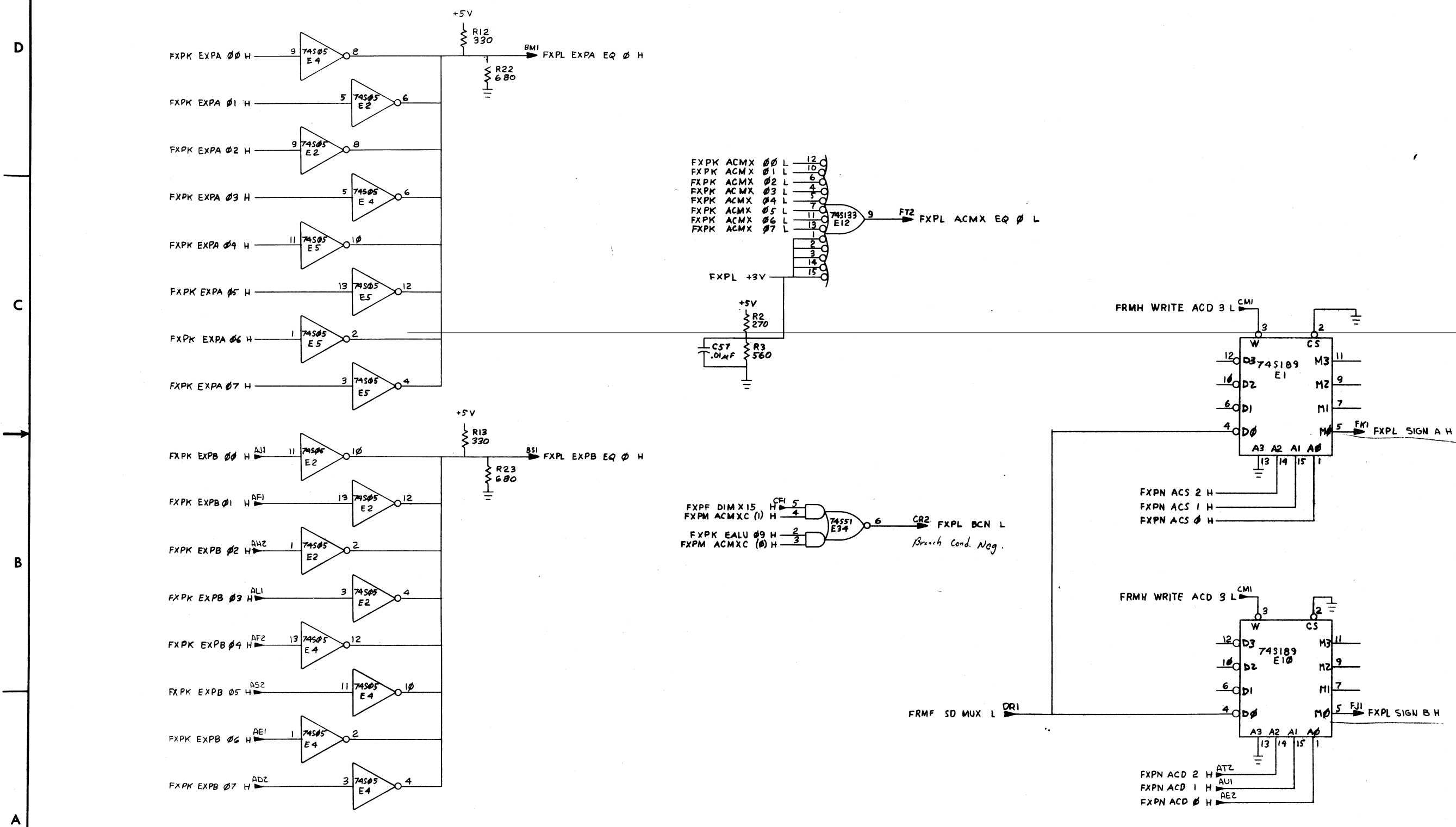
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REVISIONS		
CHK	CHANGE NO.	REV.

(EXP SCRATCH PADS (SL0T5))

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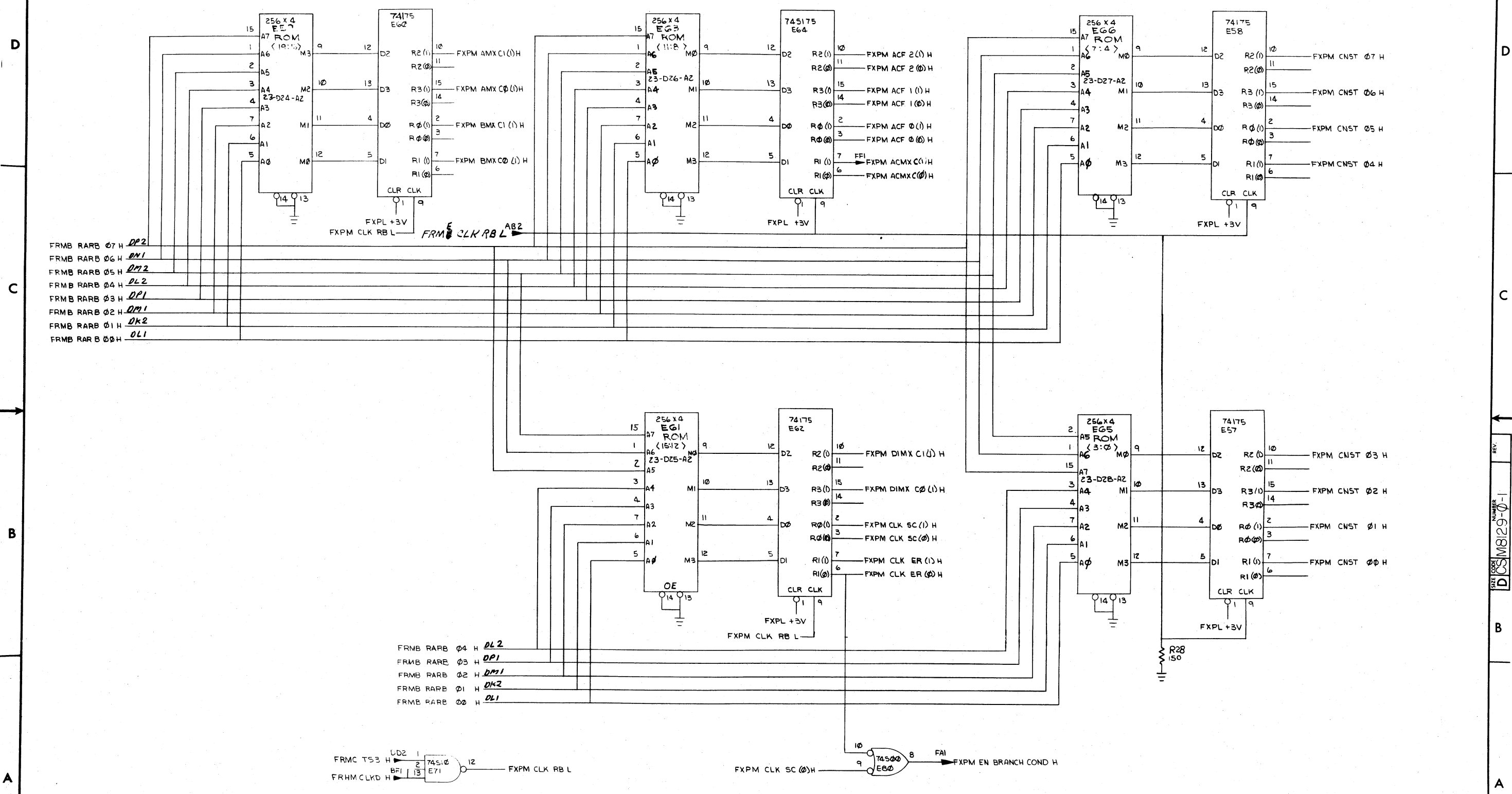


REVISIONS		
CHK	CHANGE NO.	REV.

(ZERO CHECKERS, SIGNS) (SL0T 5)

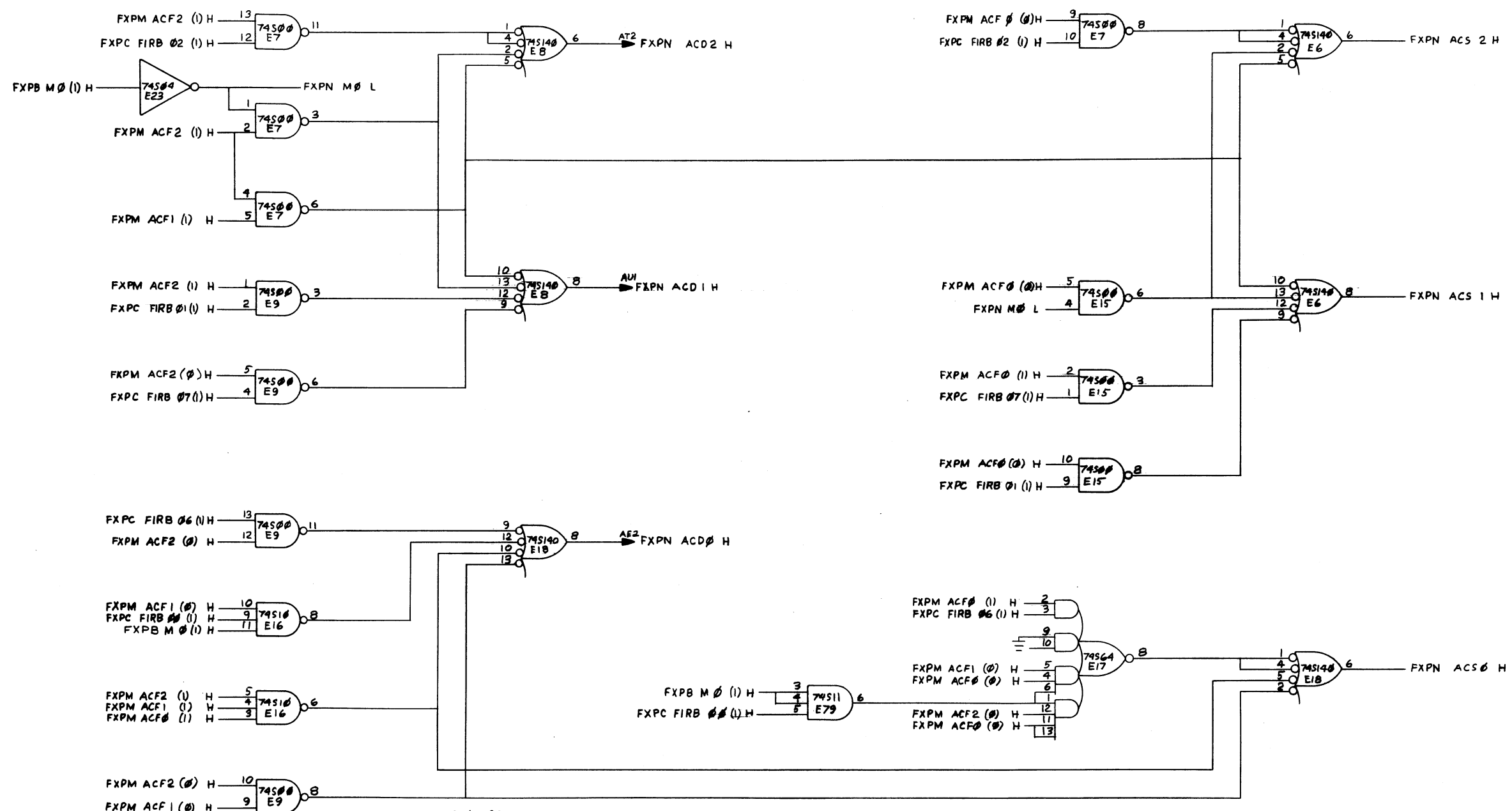
TITLE	FRACTION (FXPL) PROC. EXPON PATH	SIZE CODE	DCSM8129-0-1	NUMBER		REV.	B
SCALE		SHEET	11	OF	15	DIST.	

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CHK	CHANGE NO.	REV.

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ACF	ACS / ACD	EXPA / EXPB
0	X	
1	ACDV1 / ACDV1	
2	ACS / ACD	
3	ACD / ACD	
4	ACS / ACS	
5	ACD / ACS	
6	AC6 / AC6	
7	AC7 / AC7	

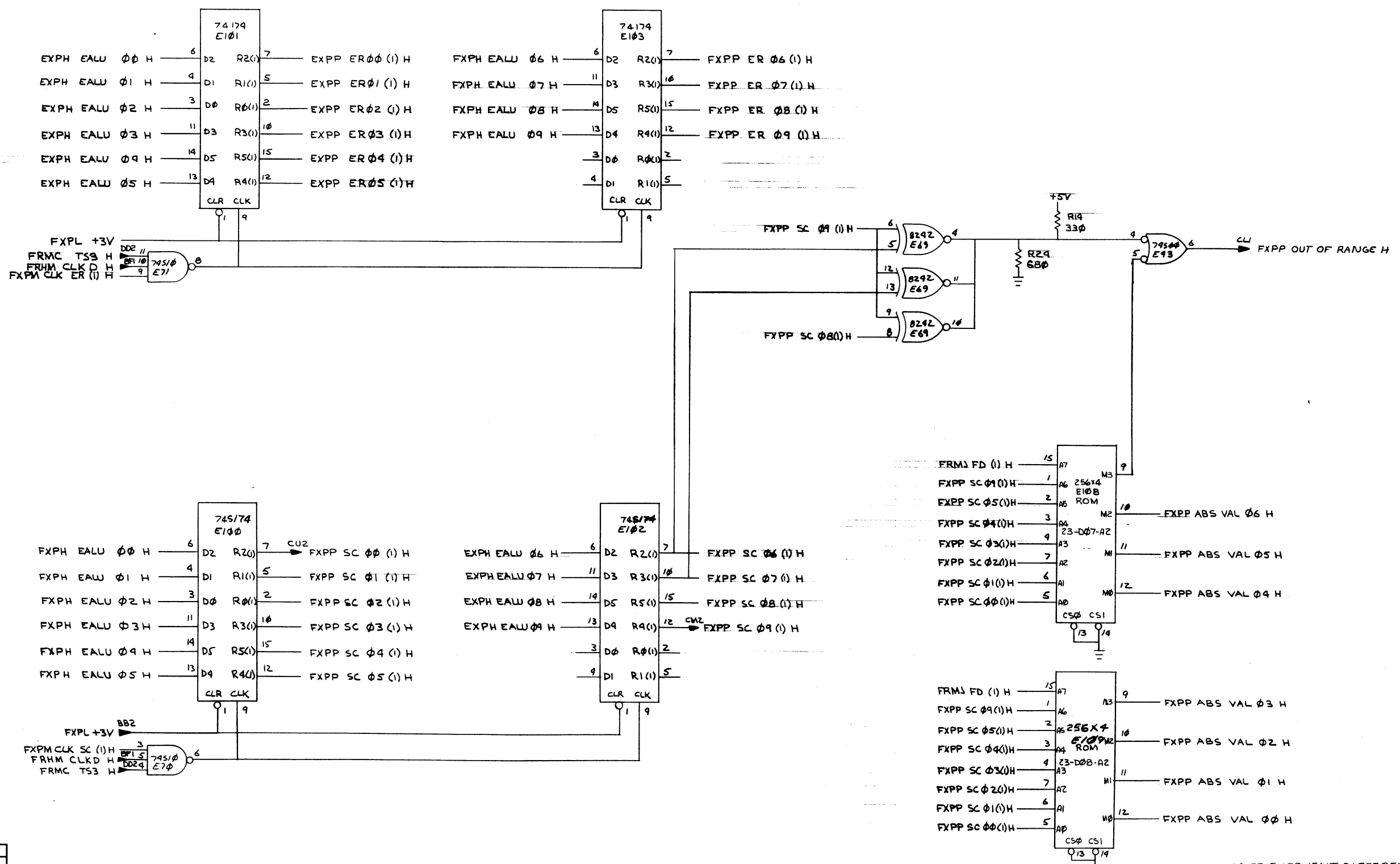
ACD = FIR07, FIR06
 ACS = FIR0(2:0) IF M0
 AC6 IF ~M0

REVISIONS		
CHK	CHANGE NO.	REV.

(ACCUMULATOR ADDRESS (SLOT 5))

TITLE	FRACTION (FXPN) PROC EXPON PATH	SIZE CODE	D CS	NUMBER	M8129-0-1	REV.	B
SCALE		SHEET	13	OF	15	DIST.	

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REVISIONS		
CHK	CHANGE NO.	REV.

DCS M8129-0-1

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

MADE BY D. HEALY	CHECKED D. HEALY	SECTION
DATE 12/15/75	DATE 12/15/75	1
ENG <i>Donna A. Ho</i>	PROD <i>Don W. Auer</i>	ISSUED SECT.
DATE 12/22/75	DATE 12-22-75	1

QUANTITY/VARIATION

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QTY	UNIT	REV	ECO NO.	REV	ECO NO.
	ZR112-RZ	PDP/11-45-55-70 FP11-C DIAGNOSTIC (DOCUMENT ONLY KIT)	1					

TITLE SOFTWARE LIST FP11-C	ASSY NO. NONE	SIZE	CODE	NUMBER	REV.	ECO NO.
	SHEET 1 OF 1	A	PL	FP11-C-3		
DIST.						

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

MADE BY	D. HEALY	CHECKED	D. HEALY	SECTION
DATE	12/16/75	DATE	12/16/75	1
ENG	<i>Ronald A. [Signature]</i>	PROD	<i>Don Weaver</i>	ISSUED SECT.
DATE	12/22/75	DATE	12-22-75	1

QUANTITY / VARIATION

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	FP11-C																		
	EK-FP11C-MM	FLOATING POINT PROC MAINT. MANUAL	1																		

TITLE	ASSY NO.	SIZE CODE	NUMBER	REV.	ECO NO.
SHIPPING LIST FP11-C	NONE	A PL	FP11-C-4		
	SHEET 1 OF 1	DIST.			

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**DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS**

ENGINEERING SPECIFICATION

DATE 15 DEC 75

TITLE FP11-C INSTALLATION AND ACCEPTANCE PROCEDURE

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG <i>Thomas A. [Signature]</i>	APPD	SIZE A	CODE SP	NUMBER FP11-C-5	REV
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DEC 16-(392)-1079A-R873
DRA 107A

SHEET 1 OF 3

ENGINEERING SPECIFICATION

digital

CONTINUATION SHEET

TITLE FP11-C INSTALLATION AND ACCEPTANCE PROCEDURE

EQUIPMENT REQUIRED

- 11/70 MA (115V), 11/70 MB (230V), 11/45, 11/50, or 11/55
- FP11-C Floating Point Processor

TEST EQUIPMENT REQUIRED

- Oscilloscope, Tektronix 453 or equivalent
- Digital Voltmeter (DVM)

INSTALLATION PROCEDURE

- Run Processor diagnostic:

11/70	11/45
DEKQC	T-17
DEKBA	
DEKBB	
- Verify that Processor into which FP11-C is to be installed is KB11-C (11/70) or KB11-D (11/45, 11/50, or 11/55).

 Quick verification is as follows:
 - RAC module (slot 9) is M8123.
 - There is continuity between backplane pins.

11/70: E13R2 and CØ2R1, or
11/45, 11/50, 11/55: E15R2 to CØ2R1

NOTE: If the Processor is found not to be one of the above, it must be upgraded to accept the FP11-C. Upgrade kits (which include an FP11-C) are FP-45-CU (11/45) and FP-70-CU (11/70).
- With system power off, install the floating point +5V regulator (H744), (included with the FP11-C), in the upper system bulk power supply regulator A position. (See Figure 1.) Connect the regulator by inserting the provided male mate-n-lock connector from the system power harness (P9 for 11/70, P17 for 11/45, 11/50, 11/55) into the female mate-n-lock receptacle on the regulator.
- Apply power to the system and measure the voltage present at pin AØ2A2 of the Processor backplane. It should be between 5.0 and 5.3 volts. Adjust the regulator (position A) output, if necessary, to obtain the required voltage.

SIZE A	CODE SP	NUMBER FP11-C-5	REV
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DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 2 OF 3

TITLE FP11-C INSTALLATION AND ACCEPTANCE PROCEDURE

5. Remove power from the system.
6. Plug in the four FP11-C modules as follows:
 - Slot 2 M8126
 - Slot 3 M8127
 - Slot 4 M8128
 - Slot 5 M8129
7. Remove IRC module (M8132 for 11/70, 11/45, 11/50, 11/55) from the system. Verify board is rev. B or higher, and that jumper W1 has been removed from the board. If it has not been, remove it. Replace the module.
8. Turn on system power and, using the DVM, measure the voltage present at backplane pin A02A2. Adjust the regulator (position A) output until the voltage measured is $+5.0V \pm .05V$.
9. Load and run each of the following diagnostics for the prescribed times:
 - a. MAINDEC-11-DEFFA - 5 passes
 - b. MAINDEC-11-DEFPB - 5 passes

No error printouts should be experienced.
10. Run Processor diagnostics:

<u>11/70</u>	<u>11/45</u>
DEKQC	T17
DEKBA	
DEKBB	

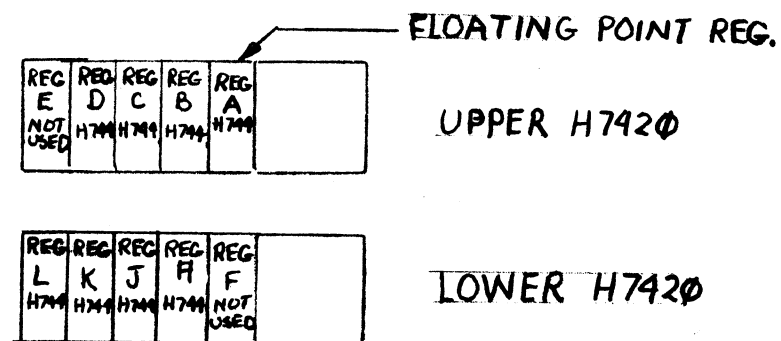


FIGURE 1 INSTALLATION OF FP11-C REGULATOR

SIZE A	CODE SP	NUMBER FP11-C-5	REV
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