Digital Equipment Corporation
Maynard, Massachusetts

digital

PDP-10
Maintenance Manual

VP10
DISPLAY CONTROL

DEC-10-H6AB-D

PDP-10
VP10 DISPLAY CONTROL MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION ▫ MAYNARD, MASSACHUSETTS

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Instruction times, operating speeds and the like are included in this manual for reference only; they are not to be taken as specifications.

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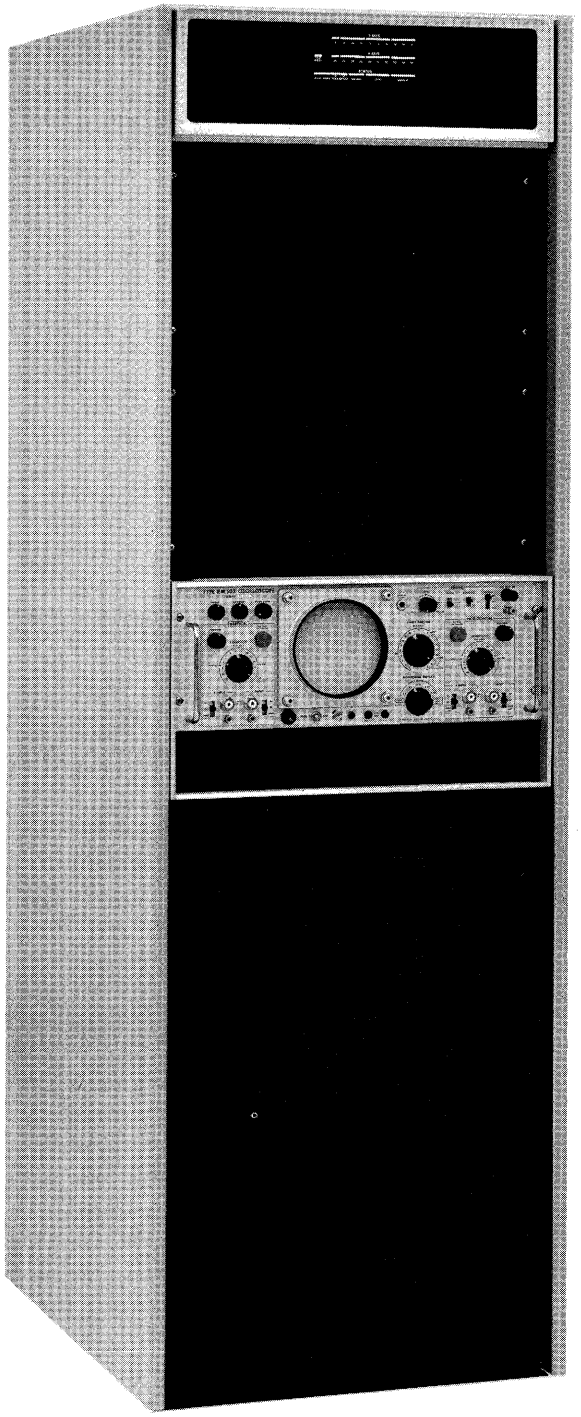
VP10 Point Plot Display Control



VP10 Point Plot Display Control

CHAPTER 1
GENERAL INFORMATION

1.1 SCOPE

This manual provides the necessary information for installation, operation, and maintenance of the VP10 Point Plot Display Control. The VP10 is intended for use with the PDP-10 Computer System.

Reference documents which supplement the material presented in this manual are listed in Section 1.6.6.

1.2 GENERAL DESCRIPTION

The VP10 is housed in a DEC cabinet, Type CAB 9-B, which can accommodate up to 12 horizontal 5-3/16 in. x 19 in. panels. Two locations are utilized for the logic, which is contained in DEC Type 1943B mounting panels. The indicator panel occupies one location as illustrated in Figure 1-1. A half-height single door, mounted on the lower front of the cabinet, provides access to the wiring side of the logic panels. A DEC Type 728 Power Supply and Type 844 Power Control are mounted in the bottom two locations on the hinged full-width plenum door at the rear of the cabinet. Ventilation is provided by a single fan, mounted on the floor of the cabinet, which draws in filtered air. Three blower fans, below the logic panels, circulate the filtered air around the modules.

The VP10 accepts coordinate address words from the PDP-10 Central Processor. These words are converted to appropriate analog levels and applied to the horizontal and vertical deflection inputs of an oscilloscope (Tektronix Type RM503, or equivalent) or an appropriate CRT Display (DEC Type VR12) to provide a point plot of the coordinate address words. The program can designate a variable duration pulse to the Z axis input of the display, to produce an intensity modulated plot. The VP10 is program-compatible with the DEC Type 30E Display Control.

The following information can be displayed on the cathode-ray tube (CRT) display:

a. mathematical curves
b. line drawings

c. in general, any graphic which can be written in binary form and stored in the PDP-10 Memory.

Most stored data is in a form that requires mathematical operations within the computer, specified by the program, before transmission to the VP10 for display.

The VP10 contains logic which allows a light pen to control or communicate with the program by use of a priority interrupt channel selection system. The DEC Type 370 Light Pen is described in Appendix A.

NOTE

The light pen and light pen power supply, as well as the Tektronix Type RM503, with mounting hardware for adaptation to the DEC CAB 9B cabinet, are offered as options to the VP10.

1.3 SPECIFICATIONS

Size:	69-1/2 in. h, 21-1/4 in. w, 27-1/16 in. d (1763 mm h, 540 mm w, 690 mm d)
Weight:	(260 lb, 118 kg)
Voltage Requirements:	115V ± 10%, 60 Hz ± 2% 230V ± 10%, 50 Hz ± 2%
Current Consumption:	2.0A
Power Dissipation:	230W
Temperature:	16°C to 32°C Ambient (operating) 61°F to 90°F 4°C to 43°C Ambient (storage) 39°F to 110°F
Humidity:	20% to 80% (relative)
Output Levels:	X 0V to -10V Y 0V to -10V Z -15V to +10V
Logic Levels	0V, -3V

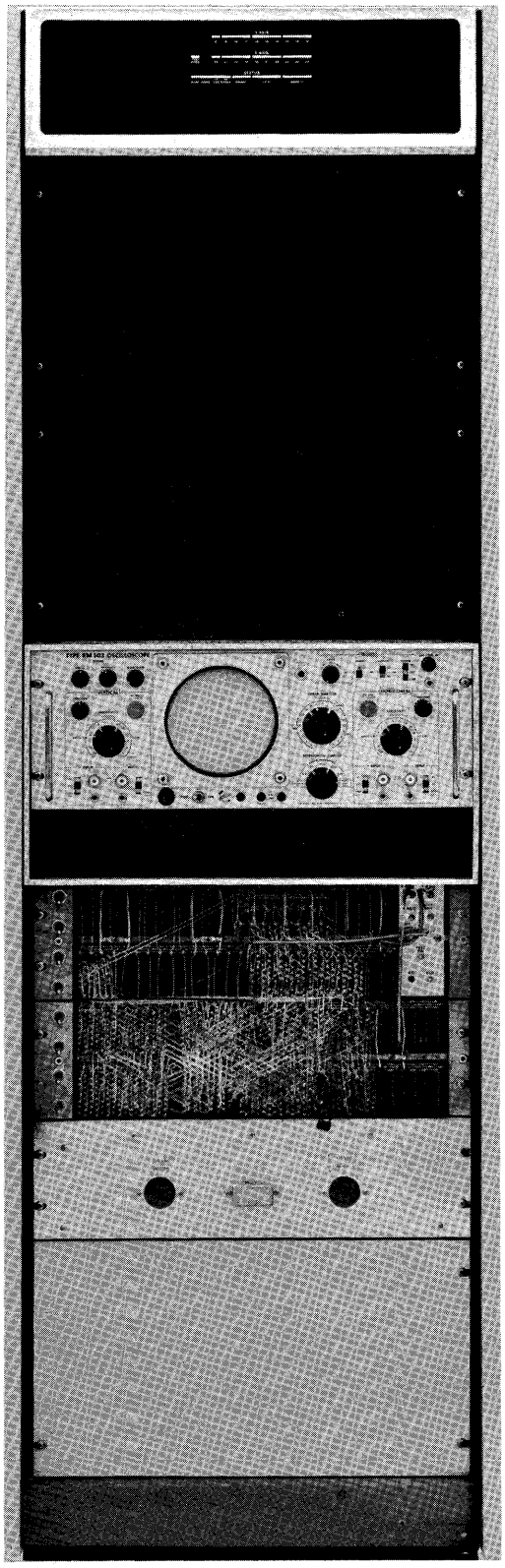


Figure 1-1 VP10 Front View

1.3.1 Module Utilization

Table 1-1 is a list of the DEC FLIP CHIP Modules used in the VP10. Refer to drawing D-MU-VP10-0-2 in Chapter 7 of this manual for the location within the display and the logical function of each module.

Table 1-1
DEC FLIP CHIP Modules for VP10

DEC Number	Description	DEC Number	Description
A601	Digital-to-Analog Converter	S203	Triple Flip-Flop
A704	Reference Supply	S205	Dual Flip-Flop
B152	Binary-to-Octal Decoder	W005	Clamped Load
B163	Diode Gate	W012	Indicator Cable Connector
R002	Diode Network	W023	Cable Connector
R201	Flip-Flop	W107	I/O Bus Receiver
R302	Dual Delay Multivibrator	W250	Indicator Cable Connector
R613	Pulse Amplifier	W681	Oscilloscope Intensifier
S107	Inverter	W851	PDP-10 Bus Connector Board
S111	Diode Gate	W990	Blank Module/18 pins

1.4 MNEMONICS

Table 1-2 is a list of the mnemonics used in this manual.

Table 1-2
Mnemonics

Mnemonic	Meaning	Mnemonic	Meaning
BR	Brightness	DEL	Delay
CLR	Clear	DPY	Display
CONI	Conditions in Instruction	INT	Intensity
CONO	Conditions Out Instruction	IOB	I/O Bus Interface
DAC	Digital-to-Analog Converter	IOBC	Input/Output Bus Control
DATAI	Data In Instruction	LP	Light Pen
DATAO	Data Out Instruction	PI	Priority Interrupt
DC	Display Control	ST	Status
DCDR	Decoder		

1.5 LEVELS AND PULSES

Table 1-3 is a listing of the levels and pulses utilized or developed in the VP10, including a brief description of the function of each.

Table 1-3
VP10 Levels and Pulses

Level/Pulse	Function
CROBAR	This level is generated in the 844 Power Control for 4 seconds during power up and down conditions, precluding data transfers or interrupt requests during the period of assertion.
DC ANALOG SETTLE DOWN	The delayed level, generated by DC ST INT and applied to the inputs of the three display brightness delays in the DC logic.
DC BR LOW	The delayed level generated by DC ANALOG SETTLE DOWN when ST BR00 (1) and ST BR 01 (1) are asserted. This level establishes the low brightness CRT display.
DC BR MED	The delayed level generated by DC ANALOG SETTLE DOWN when ST BR 00 (0) and ST BR 01 (0) are asserted. This level established the medium brightness CRT display.
DC BR HI	The delayed level generated by DC ANALOG SETTLE DOWN when ST BR 00 (0) and ST BR 01 (1) are asserted. This level establishes the high brightness CRT display.
DC ST INT	This pulse initiates the logic in the display control which will determine the CRT display intensity.
IOB CONI	From the PDP-10 Central Processor, this level causes generation of IOBC CONI(A) and (B) in the VP10 if ~CROBAR and IOB DPY SEL are asserted.
IOB CONO CLR	From the PDP-10 Central Processor. When IOBC DPY SEL is asserted, this pulse generates IOBC DPY CONO CLR in the VP10.
IOB CONO SET	From the PDP-10 Central Processor. When IOBC DPY SEL is asserted, this pulse causes generation of IOBC DPY CONO SET in the VP10.
IOB DATAI	From the PDP-10 Central Processor. When ~CROBAR and IOB DPY SEL are asserted, this level causes generation of IOBC DPY DATAI (A), (B), and (C) in the VP10.
IOB DATAO CLR	From the PDP-10 Central Processor. When IOBC DPY SEL is asserted, this pulse generates IOB DPY DATAO CLR X and Y in the VP10.

Table 1-3 (Cont)
VP10 Levels and Pulses

Level/Pulse	Function
IOB DPY DATAI (A)	This level causes the contents of Y00-09 to be read into IOB 08-17 and IOB 08(B)-17(B).
IOB DPY DATAI (B)	This level causes the contents of X00-09 to be read into IOB 26-35 and IOB 26(B)-35(B).
IOBC DATAO SET	From the PDP-10 Central Processor. When IOBC DPY SEL DATAO X and Y is asserted, this pulse causes generation of IOBC DPY DATAO SET (X) and (Y) in the VP10.
IOBC DPY CONI (A)	This level causes the status of the Status Register flip-flops to be placed on IOB 20, 22-25 and 27, 28.
IOBC DPY CONI (B)	This level causes the status of the Status Register flip-flops to be placed on IOB 21, 26, and 30-35.
IOBC DPY CONO CLR	This pulse clears all VP10 Status Register flip-flops.
IOBC DPY CONO SET	This pulse causes 1s from IOB 20-28 and 30-35 to be read into the Status Register flip-flops.
IOBC DPY DATAO CLR X	Clears X register, sets ST BUSY, and clears ST DONE flag.
IOBC DPY DATAO CLR Y	Clears Y register simultaneously with IOBC DPY DATAO CLR X; therefore ST BUSY is set and ST DONE cleared on the IOBC DPY DATAO CLR Y pulse (except in X or Y ONLY mode).
IOB DPY DATAO SET (X)	This pulse causes the contents of IOB 26(B)-35(B) to be read into X00-09 and causes generation of DC ST INT.
IOBC DPY DATAO SET (Y)	This pulse causes the contents of IOB 08(B)-17(B) to be read into Y00-09.
IOBC DPY SEL	Developed as a result of decoding the VP10 Device Select Code (134_8); also dependent on the ~CROBAR condition, this level must be present to set the VP10 in operation.

1.6 MAJOR LOGIC SECTIONS, SIMPLIFIED DESCRIPTION

The VP10 contains five major logic sections. Figure 1-2 is a simplified block diagram illustrating the relative logical position of each section. Detailed descriptions of the logic functions are contained in Chapter 4, Principles of Operation.

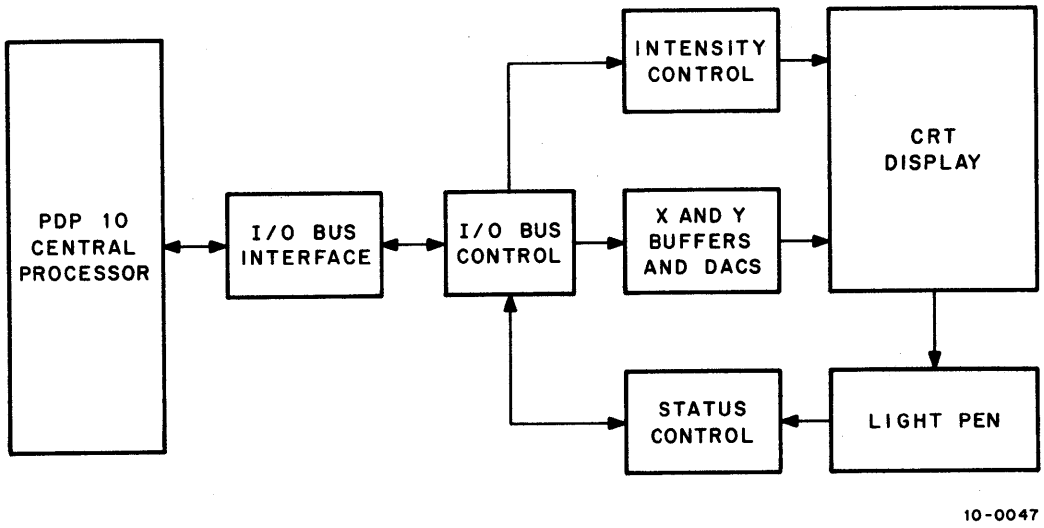


Figure 1-2 Simplified Block Diagram

1.6.1 I/O Bus Interface

The I/O Bus (IOB) Interface contains circuitry for information transfers to and from the PDP-10 over the I/O Bus.

1.6.2 I/O Bus Control

The I/O Bus Control contains the logic for decoding device commands, thereby providing the basic activating signal for display functions. The Display Control internal instruction pulses and levels are triggered by pulses generated in the PDP-10 Central Processor by the four basic instructions; CONI, DATAI, CONO, and DATAO.

1.6.3 Display Control

The Display Control (DC) contains the circuitry which determines the brightness of the CRT display. Delayed pulses for initiating the Test Mode are also developed in this section of the logic.

1.6.4 XY Buffers and Digital-to-Analog Converters

This section of the logic contains the X and Y registers where the data word is applied to the Digital-to-Analog conversion (DAC) circuitry. The DACs provide analog output levels to the CRT horizontal and vertical deflection inputs.

1.6.5 Status Control

This section contains the logic for: all flags; the registers for selecting the Priority Interrupt channels through binary-to-octal decoders; the register for the brightness control; and the buffers for reading the display conditions into the IOB Bus.

1.6.6 Reference Material

The following documents contain information pertinent to the operation and maintenance of PDP-10/VP10 system:

KA10 Maintenance Manual (two volumes)
PDP-10 System Reference Manual
Digital Logic Handbook, C-105
PDP-10 Interface Manual
PDP-10 Site Preparation Guide

Documents published by DEC are available from Digital Equipment Corporation, 146 Main Street, Maynard, Mass. 01754, or from the nearest DEC District Office. The technical documents applicable to the particular oscilloscope or CRT display in use should be obtained from the manufacturer.

CHAPTER 2
INSTALLATION

2.1 SCOPE

This chapter contains the basic requirements for installation of the VP10 Display Control.

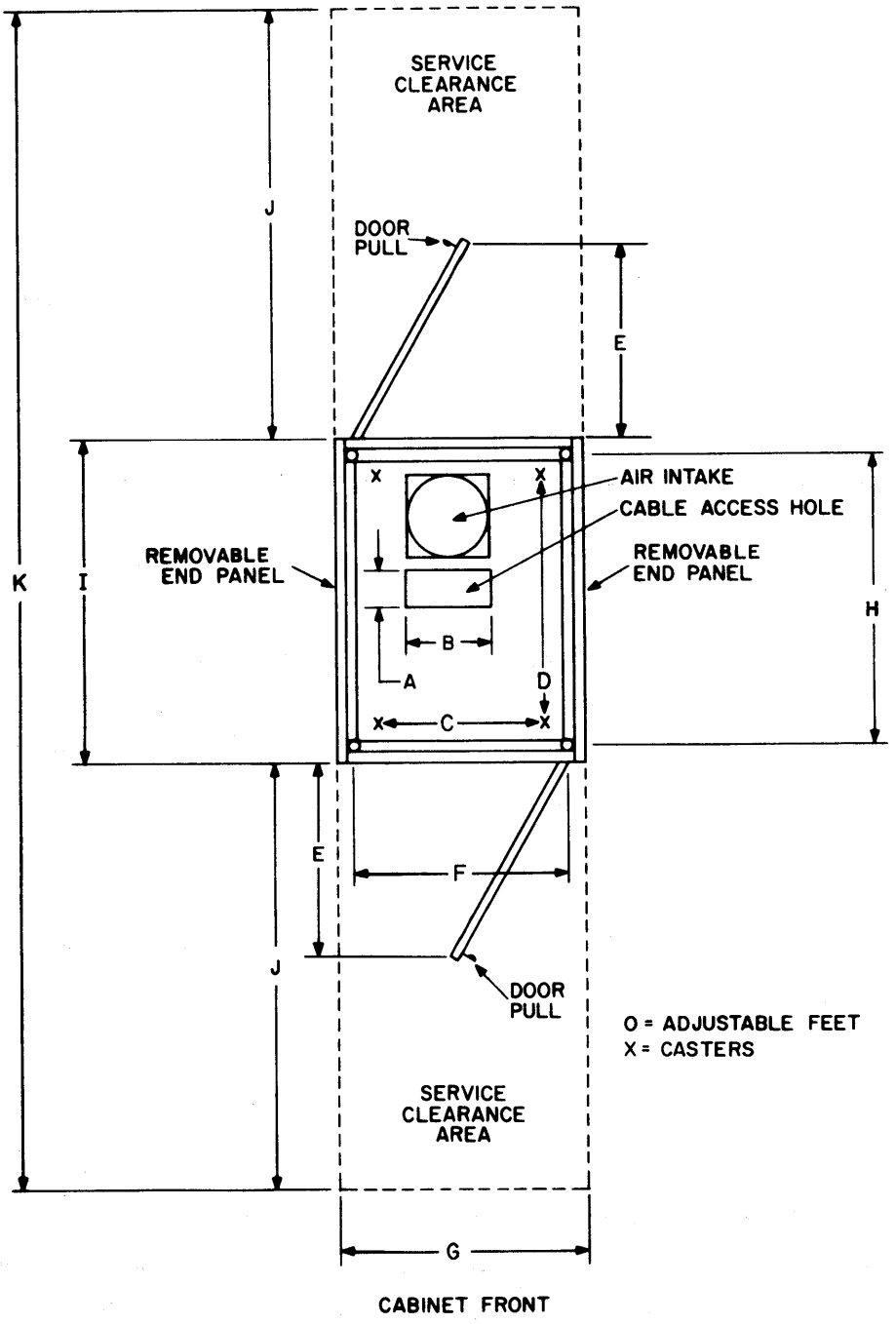
2.2 UNPACKING

The VP10 is crated for shipment and mounted on a skid. Remove all crating and strapping material, and all protective padding. Ensure that the equipment is not scratched or otherwise damaged during unpacking. The plenum door at the rear of the equipment has spring catches. To reinforce the door during shipment, two screws are used to hold the door shut. Remove these screws and store them in the plastic loops provided. Remove any packing material, shipping blocks, etc., from the interior of the equipment. The plug-in modules are taped-in during shipment; carefully remove the tape. Determine that all modules are properly seated and make a careful inspection of the cabinet interior. If relocation or reshipment of the equipment is anticipated, save the special packing materials for reuse.

2.3 SITE SELECTION

There are no special site requirements other than the floor space dimensions and service clearances shown in Figure 2-1. Both cabinet end-panels are removable. If possible, allow sufficient area for their removal to facilitate cleaning and maintenance. No sub-flooring is required. Casters on the bottom of the cabinets permit easy positioning and provide clearance for cable entry. The installation site should be as free as possible from excess dirt and dust; corrosive fumes and vapors; and strong magnetic fields.

The cabinet is equipped with cooling fans, therefore, no additional cooling is required in a normal installation.



DIMENSIONS	A	B	C	D	E	F	G	H	I	J	K
INCHES	3.50	7.25	12.50	17.25	19.25	20.00	21.25	25.50	27.00	36.00	99.00
METERS	0.08	0.18	0.32	0.44	0.49	0.51	0.54	0.65	0.68	0.91	2.51

10-0147

Figure 2-1 VP10 Area Requirements

2.4 INSTALLATION SPECIFICATIONS

Table 2-1 lists the general specifications of the VP10 which pertain to the installation of the equipment.

2.4.1 Interconnection

The maximum length for all interconnecting cables is 150 ft. Table 2-2 contains the information necessary for interconnecting the system. The cables supplied with the VP10 are terminated on both ends with the proper connectors. All cables enter through access cutouts in the bottom of the cabinet.

Table 2-1
General Specifications

Voltage (AC)	Current (Nominal)	Power Dissipation	Ambient Temperature	Relative Humidity	Dimensions	Service Clearance	Cable Lengths (Max.)
115V ±10% 60 Hz ±2 Hz or 230V ±10% 50 Hz ±2 Hz	2.0A 1.0A	230W	Operating: 16-32°C 61-90°F Storage: 4-43°C 37-110°F	20% to 80%	69-1/2 in. h 1753 mm h 21-1/4 in. w 540 mm w 27-1/16 in. d 687 mm d	36 in 910 mm	150 ft 45 m

Table 2-2
Cable Interconnections

VP10 Location	Oscilloscope Location (RM503)	Cable Type	Function
844 Power Control		#14 (3 Cond.)	Power
844 Power Control		#16 (3Cond.)	Remote Power Control
Power Distribution Strip		BC10B	Margin Voltage
CD01-CD08 (See Dwg. No. D-MU-VP10-02)		BC10A	I/O Bus
BNC Female Connectors on Switch Panel	+Horizontal = X +Vertical = Y -Horizontal } XY -Vertical } Return	RG-59/U, terminated at both ends with male BNC connectors	X, Y and X+Y Return Scope inputs
BNC Female Connector on Switch Panel	Z Input	RG-59/U BNC → Banana Plug	Z Scope Input
B28		7006212-0-0	Light Pen

CHAPTER 3

OPERATION AND PROGRAMMING

3.1 SCOPE

This chapter describes the VP10 controls and indicators and discusses the operation and programming of the VP10 Point Plot Display Control. VP10 operation on receipt of an I/O instruction and step by step operation of a sample program are described.

3.2 VP10 CONTROLS AND INDICATORS

3.2.1 Indicator Panel

The indicator panel is shown in Figure 3-1. Lamps are provided to monitor the data and status registers, as shown in Table 3-1.

Table 3-1
Data/Status Register Monitoring

Lamp	Flip-Flop
Y AXIS	Y00 through 09
X AXIS	X00 through 09
TEST MODE	ST TEST MODE
BUSY	ST BUSY
DONE	ST DONE
LP FLAG	ST LP FLAG
HI SPEED	ST HI SPEED
BRIGHTNESS	ST BR00 and 01
LP PRIORITY INTERRUPT	ST LP PI00 through 02
DONE PRIORITY INTERRUPT	ST DONE PI00 through 02

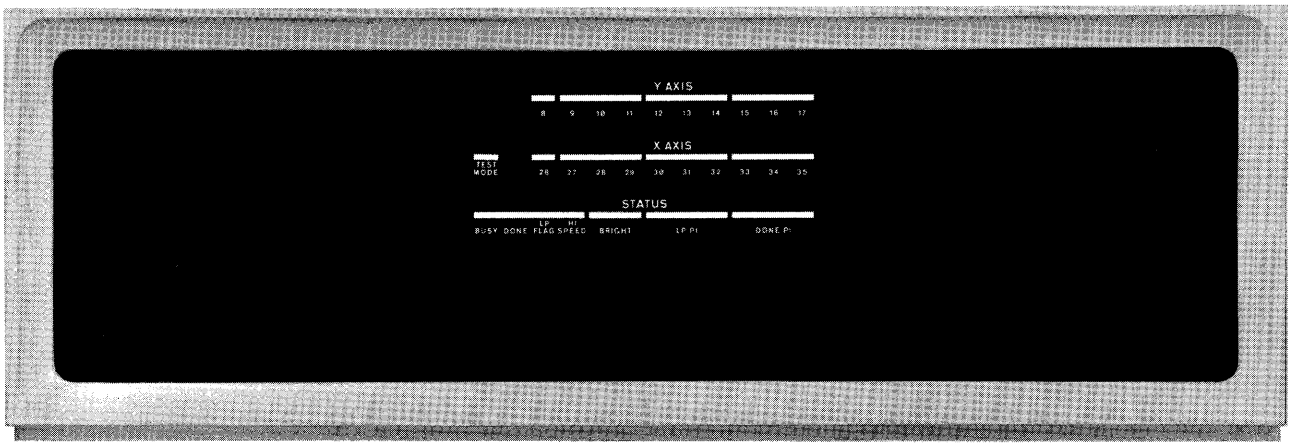


Figure 3-1 Indicator Panel

3.2.2 Switch Panel

The Switch Panel is shown in Figure 3-2. Switches and connectors are described in Table 3-2.

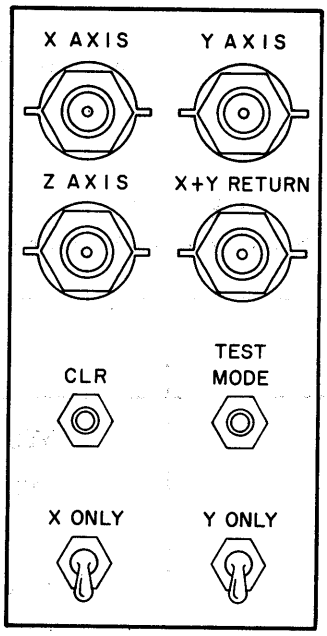


Figure 3-2 Switch Panel

Table 3-2
Switches/Connectors

Switch	Function
CLR	The CLR switch, when depressed, momentarily asserts IOBC RESET, which generates IOBC DPY DATAO CLR X and Y. IOBC DPY DATAO CLR X and Y clears the X and Y Registers; and resets the ST DONE flag. IOB RESET also generates IOBC DPY CONO CLP which clears the ST BUSY Flag.
X ONLY	When in the up position prohibits changes in the Y register.
Y ONLY	When in the up position prohibits changes in the X register.
TEST MODE	The TEST MODE switch, when depressed, collector sets DC GO, BR01, ST TEST MODE, and ST HI SPEED. Releasing the TEST MODE switch generates DC ST INT, which sets the DC ANALOG SETTLEDOWN delay. The recovery of DC ANALOG SETTLEDOWN triggers the DC BR HI delay which enters the display into the Test Mode.
CONNECTOR	
X AXIS	BNC connector for the X level output to the CRT display.
Y AXIS	BNC connector for the Y level output to the CRT display.
Z AXIS	BNC connector for the Z level (intensity) output to the CRT display.
X+Y RETURN	BNC connector for the X and Y returns to the CRT display.

3.2.3 Type 844 Power Control

Remote turn-on and local power to the VP10 is controlled from the Type 844 Power Control Panel. The panel is illustrated in Figure 3-3. Table 3-3 lists the functions of the controls and indicators.

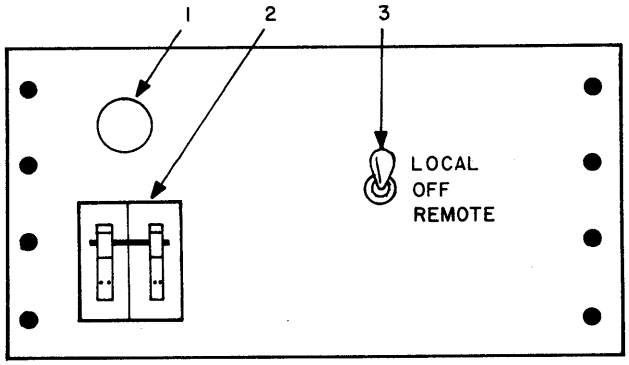


Figure 3-3 Power Control Panel

Table 3-3
Power Control Functions

Number	Nomenclature	Item	Function
1		Indicator - White	Illuminated when line power is applied.
2	30 AMP	Circuit Breaker	Controls the line power to, and protects, the VP10.
3	REMOTE/OFF/ LOCAL	Toggle Switch	Selects the Local, Off, or Remote Turn-On mode.

3.2.4 Margin Switches

Margin switches are provided for performance of margin checks in each section of the logic. As shown in Figure 1-1, the switches are located on the left, front side of the logic panels and are accessible when the cabinet front door is open.

3.3 I/O INFORMATION

Input/output instructions govern all transfers of data to and from the VP10 and also perform many operations within the processor. Section 2.12 of the PDP-10 System Reference Manual illustrates the I/O instruction format and contains descriptions of each instruction.

3.3.1 VP10 I/O Conditions

Bits 20 to 35 of the instruction word designate the following conditions when they contain a 1:

Bit	CONO Display	Function
20	Hi Speed	When 0, the DONE flag is set 100 μs after each DATAO operation. When 1, the DONE Flag is set approximately 20 μs after each DATAO.
21	TEST MODE	Enables the VP10 to plot a diagonal line on the CRT screen. One point is plotted every 19.4 μs.
22	BUSY Flag	Display in operation

Bit	CONO Display	Function
23	LP Flag	The light pen has sensed light and caused an interrupt on the channel selected by bits 30-32.
24	DONE Flag	A set of coordinate points has been displayed on the oscilloscope. An interrupt is requested on the channel selected by bits 33-35.
25	Y ONLY	Prevents X Register from changing.
26	X ONLY	Prevents Y Register from changing.
27,28	Brightness	Selects brightness level by allowing the time of the intensity output level to be selectable. 10 - No Intensity 11 - Low 00 - Medium 01 - High
29	Not used	
30-32	LP PI	Selects interrupt channel for LP Flag.
33-35	DONE PI	Selects interrupt channel for DONE Flag.

3.4 VP10 OPERATIONS

The VP10 contains a 7-bit device selection network and three flags; BUSY, DONE, and LP. The device selection code, 134_8, contained in bits 3 through 9 of the instruction word, is decoded so that the VP10 responds only to signals sent to it by the processor over the in-out bus. For priority interrupt operation, the program must assign an interrupt channel. Channels are designated by bits 30 through 32 for Light Pen Priority Interrupt and bits 33 through 35 for Done Priority Interrupt.

The BUSY and DONE flags together denote the basic state of the VP10. When both are clear, the VP10 is idle. To place the display in operation, a CONO instruction conditions the logic which determines:

a. selection of PI Channels
b. brightness of the CRT plot
c. mode (HI or ~HI SPEED)

The program must give a DATAO to send the first unit of data. This unit consists of 10X and 10Y bits. When this data has been converted to appropriate analog levels and a point has been displayed, BUSY is cleared and DONE is set to indicate that the VP10 is again ready to receive new data. The program

responds with a DATAO to send more data for conversion and display. If a point displayed is in the field of vision of the Light Pen, the VP10 sets the LP Flag. The setting of DONE or LP signals the program by requesting an interrupt.

Interrupt requests are handled through seven channels arranged in a priority chain within the Central Processor. The selection of channels is left entirely at the discretion of the programmer. To assign the Light Pen Interrupt or Done Interrupt to a channel, the program sends the number of the channel to the VP10 Control Register as part of the conditions by a CONO (bits 30 through 32 for LP PI and bits 33 through 35 for DONE PI). Channels are designated 1 through 7 with 1 having the highest priority. A zero assignment disconnects the VP10 from the interrupt channels altogether. In this situation, the program must continue testing DONE to determine when the display is ready.

3.5 SAMPLE PROGRAM

The following is a discussion of VP10 operations during a sample program (refer to Table 3-4) which results in the plotting of a square on the CRT screen, as shown in Figure 3-4. The program steps, designated 1 through 28, do not refer to memory locations.

The program first gives CONO 134, 104200 where 134_8 is the Device Code which selects the VP10. The value 104200_8 sets HI SPEED, DONE, and ST BR01, specifying the high brightness level (refer to Section 3.3.1). The second step (SETZ 1, 0) sets AC 1 = 0. Step 3 (MOVEI 2, 400) puts the size of the square (400), selected for convenience, into AC 2. Step 4, CONSO 134, 4000, tests the VP10 and will skip the next instruction if the DONE flag is up. CONSO can test only the right 18 bits and since the specified bit is 24, the program is testing for the DONE flag. The instruction in Step 5 (JRST. -1) will only be executed if the DONE flag is not up. The program will continue to test for DONE and jump back until the flag goes up and Step 5 will be skipped. Step 6 (DATAO 134, 1) loads the VP10 X and Y Registers with the contents of AC 1, which was set to 0 in Step 2. The VP10 will now plot one point corresponding to the X and Y coordinates 0, 0.

Step 7, MOVSS 1, swaps the left and right halves of the word in AC 1. This is actually an X and Y swap because the Y data was originally in the left half of the word and the X data in the right half. Steps 8 and 9 are identical to Steps 4 and 5 (the DONE flag is tested), in this case following the DATAO to determine if the VP10 is ready to accept more data. The program could specify a DONE Priority Interrupt Channel, thereby eliminating the requirement for the program to test for the DONE condition. Central Processor time would be more economically utilized, if a PI were designated.

Step 10 (DATAO 134, 1) causes the point 0, 0 to be plotted again, as the contents of the AC 1, although swapped, were not changed and remain all 0s.

Step 11 (SOJE 2, SQ) subtracts one from the contents of AC 2 (400) and jumps to SQ if the subtraction leaves AC 2 containing all 0s. When AC 2 goes to all 0s, the square is half plotted (the base and left side), and the program goes to SQ where the AC's are loaded in preparation for plotting the right half of the square.

In Step 12, MOVSS 1 swaps the two halves of the word in AC 1 as before. Step 13 (ADDI 1, 4) increments AC 1 by 4, thereby adding 4 to the value of the X half of the word in AC 1. Step 14 (JRST SQUARE) jumps the program back to Step 4 where the sequence is repeated. In step 6, the VP10 X and Y registers are loaded with X = 4 and Y = 0, and the point 4, 0 is plotted, followed by the plotting of 0, 4 after the swapping in Step 7. This sequence, Step 4 through Step 7, will continue until AC 2 goes to 0 and the program skips to SQ because of the SOJE 2, SQ instruction, Step 11. At this time, 1000_8 points have been plotted and the square is half complete.

In Step 15 (MOVEI 2, 400), the size of the square, 400, is loaded into AC 2 as before. Step 16 (MOVSI 1, 1777_8) loads 1777_8 into the left half of AC 1. Steps 17, 18, and 19 ready the VP10 and test for the DONE flag.

In Step 20, the point 0, 1777_8, is plotted. The MOVSS 1 instruction in Step 21 swaps 1777_8 into the X (right) half of the word in AC 1. Steps 22 and 23 test for the DONE flag. In Step 24 the point 1777_8, 0, is plotted. The SOJE 2, instruction in Step 25 will cause a jump back to SQUARE when the contents of AC 2 go to zero (after 400_8 subtractions).

Step 26 (MOVSS 1) swaps the X and Y halves of the word in AC 1 resulting in 1777_8 being contained in the left (Y) half, and 0s in the right (X) half. Step 27 (ADDI 1, 4) adds 4 to the X half of the word. The program now jumps back to SQ + 3, and after testing for DONE, the point 4, 1777_8, is plotted. The sequence continues until the final point 1777_8, 1774_8 is plotted; at which time (Step 25) the program jumps back to SQUARE, and the plotting of another square begins.

Table 3-4
Sample Program

Step	Instruction		Description
1	SQUARE/	CONO 134,104200	Select VP10 and set DONE, HI SPEED, BR01
2		SETZ 1,0	Set AC1 = 0
3		MOVEI 2,400	Load size of square into AC 2
4	SQUARE+3/	CONSO 134,4000	Is VP10 DONE flag up? If so, skip next instruction.
5		JRST .-1	No. Jump back 1
6		DATAO 134,1	Yes, select VP10 and send X and Y
7		MOVSS 1	Swap X and Y
8		CONSO 134,4000	Is VP10 DONE flag up? If so, skip next instruction.
9		JRST .-1	No. Jump back 1.
10		DATAO 134,1	Yes, select VP10 and send X and Y.
11		SOJE 2, SQ	Subtract 1 from AC 2. Does AC 2 contain all 0s, indicating that the square is half plotted? If so, jump to SQ.
12		MOVSS 1	No. Swap X and Y.
13		ADDI 1,4	Add 4 to X in AC 1.
14		JRST SQUARE+3	Jump back to SQUARE + 3.
15	SQ/	MOVEI 2,400	Load size of square into AC 2.
16		MOVSI 1,1777	Load 1777 into AC 1 and swap into Y half.
17		CONO 134,104200	Select VP10 and set DONE, HI SPEED and BR01
18	SQ+3/	CONSO 134,4000	Is VP10 DONE flag up? If so, skip next instruction.
19		JRST .-1	No. Jump back 1.
20		DATAO 134,1	Yes, select VP10 and send X and Y.
21		MOVSS 1	Swap X and Y.
22		CONSO 134,4000	Is VP10 DONE flag up? If so, skip next instruction.

Table 3-4 (Cont)
Sample Program

Step	Instruction	Description
23	JRST .-1	No. Jump back 1.
24	DATAO 134,1	Yes. Select VP10 and send X and Y.
25	SOJE 2, SQUARE	Does AC 2 contain all 0s? If so, the square is completed and jump back to SQUARE.
26	MOVSS 1	No. Swap X and Y.
27	ADDI 1,4	Add 4 to X in AC 1.
28	JRST SQ+3	Jump back to SQ + 3.

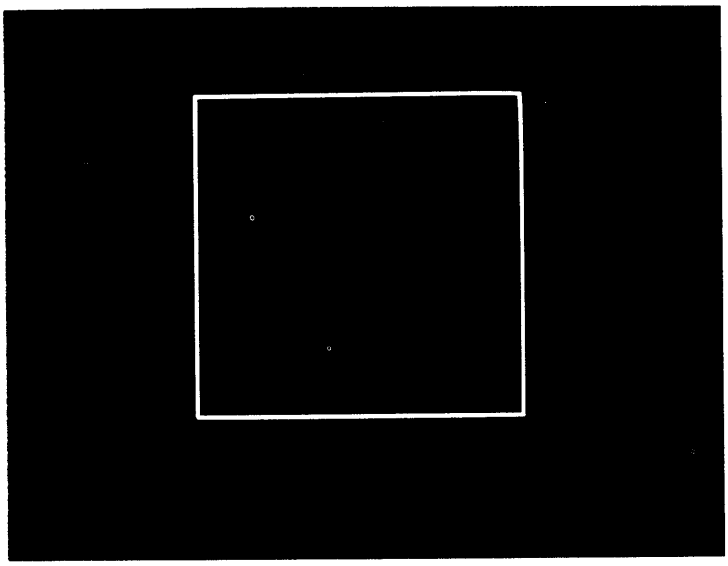


Figure 3-4 Sample Program Display

CHAPTER 4

PRINCIPLES OF OPERATION

4.1 SCOPE

This chapter presents a discussion of the logical events which take place in the VP10 on receipt of each basic I/O instruction. A discussion of the CROBAR, HI SPEED, TEST MODE, IOBC RESET, and LP STROBE option is also included.

Figure 4-1 is a Timing Diagram showing the various VP10 pulses and levels in the Test Mode. All Display Control functions are asynchronous.

Standard DEC logic (a high is represented by ground and a low by -3V) is used throughout the Display Control, except for the analog outputs to the CRT display, which may vary between between +10V and -15V for the Z input and between 0V and -10V for the X and Y inputs. The oscilloscope X+Y return is -5V.

4.2 CONDITIONS OUT INSTRUCTION - CONO

IOS 03 through 09 of the I/O Bus are ANDed with ~CROBAR in the I/O Bus Control Logic. If selection bits 03 through 09 contain the VP10 device selection code (134_8) and ~CROBAR is asserted, the gate is enabled and the IOBC DPY SEL level is produced. This is the basic activating level for all Display Control functions. The performance of all basic instructions are dependent upon the presence of this level. In the following discussions, it will be assumed that the VP10 has been selected by device code 134_8 and that, in all instances, IOBC DPY SEL has been asserted.

When IOB CONO CLR is asserted by the processor, IOBC DPY CONO CLR is produced in the I/O Bus Control Logic and clears the following flip-flops:

ST BUSY	ST DONE PI00-02
ST DONE	ST LP FLAG
ST BR00-01	ST TEST MODE
ST LP PI00-02	ST HI SPEED
	DC GO

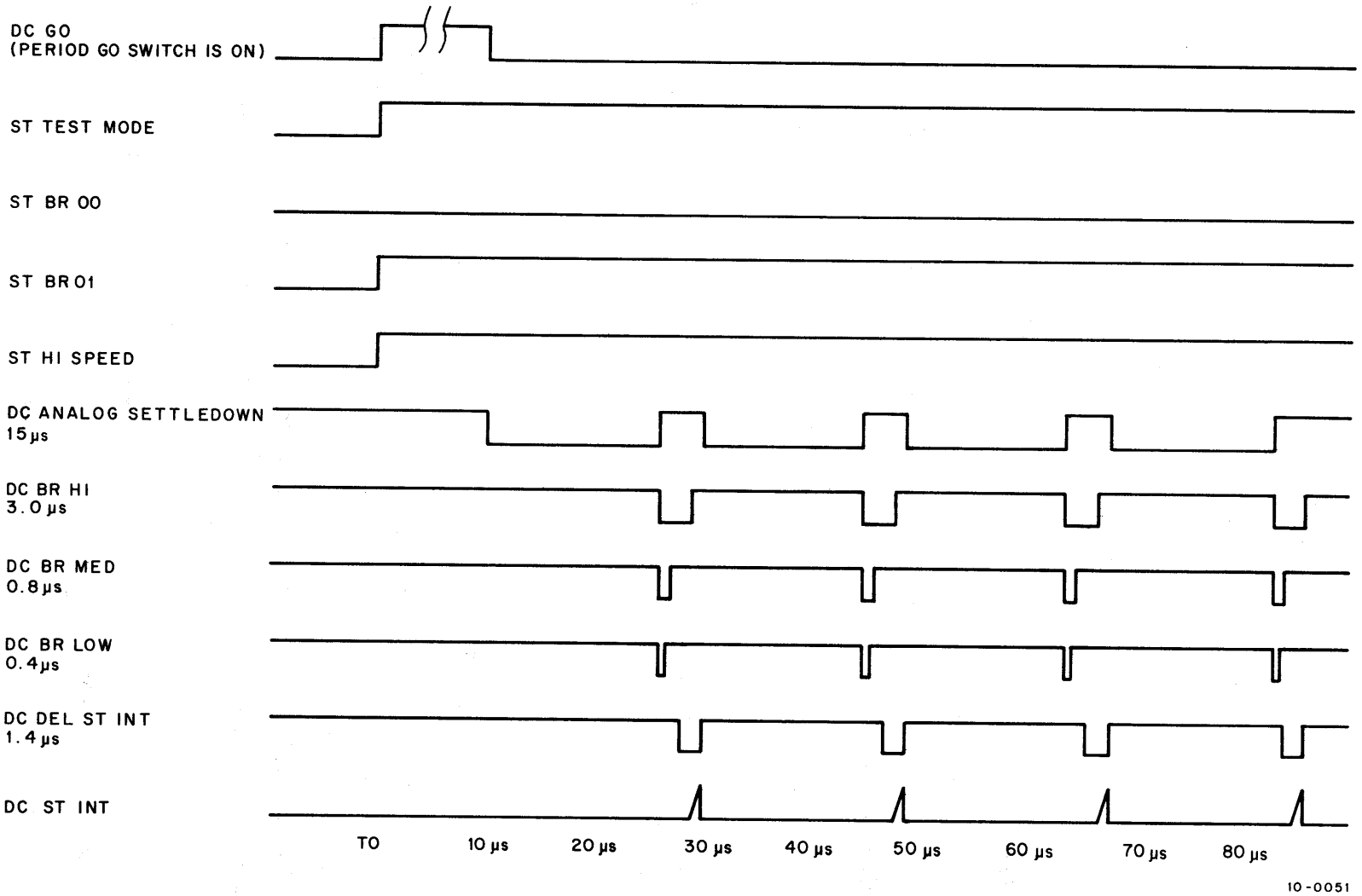


Figure 4-1 TEST MODE Timing Diagram

The next pulse from the processor, IOB CONO SET, generates IOB DPY CONO SET in the I/O Bus Control Logic. This pulse will cause the contents of IOB bits 20 through 28 and 30 through 35 to be read into the condition flip-flops as follows:

IOB Bit	Reads Into
20	HI SPEED
21	ST TEST MODE
22	ST BUSY
23	ST LP FLAG
24	ST DONE
25	ST Y ONLY
26	ST X ONLY
27	ST BR00
28	ST BR01
30	ST LP PI00
31	ST LP PI01
32	ST LP PI02
33	ST DONE PI00
34	ST DONE PI01
35	ST DONE PI02

The program conditions the VP10 during this operation. For example: if IOB bits 20 and 24 are 1s, HI SPEED and ST DONE are set to allow the VP10 to accept data and perform conversions in the HI SPEED mode during the ensuing DATAO instruction. The configuration of IOB bits 27 and 28 and 33 through 35 will determine the display brightness and priority interrupt channel, respectively.

4.3 DATA OUT INSTRUCTION - DATAO

IOB DATAO CLR from the processor produces IOBC DPY DATAO CLR X and Y in the I/O Bus Control Logic. These pulses clear the X and Y Registers, respectively, in preparation for the reading-in of a data word from the I/O Bus. IOBC DPY DATAO CLR X also sets ST BUSY, indicating that the VP10 is in operation, and clears ST DONE. The 0 state of ST DONE specifies that the VP10 cannot request another data word until it is again set to its 1 state.

Upon assertion of IOB DATAO SET by the processor, two pulses; IOBC DPY DATAO SET (Y) and (X) are produced by the I/O Bus Control Logic. IOBC DPY DATAO SET (Y) causes the contents of IOB08(B) through 17(B) to be read into Y00 through 09 in the XY Buffers. In the same manner,

X00 through 09 are loaded from IOB26(B) through 35(B) by the assertion of IOBC DPY DATAO SET (X). The information now contained in the X and Y buffers is in the form of 10-bit non-negative integer binary words which correspond to an X and a Y coordinate. The binary output from each buffer is connected to the binary input of a 10-bit, high-resolution digital-to-analog converter (DAC) composed of DEC Type A601 Modules. Reference potential (-10V) is provided to the DACs by a DEC Type A704 Reference Voltage Supply. Each analog output may vary between 0V and -10V, where the 0V output corresponds to the maximum value binary input to the DAC and the -10V analog output corresponds to the minimum value binary input. The X and Y outputs, which are applied to the horizontal and vertical inputs of the CRT display, are the analog equivalents of the digital inputs to the DACs, and together, determine the relative location of the single spot plotted on the oscilloscope screen.

Bits 27 and 28 of the CONO instruction determine the brightness of this spot by conditioning ST BR00 and ST BR01 in the status logic. IOBC DPY DATAO SET (X), which causes the loading of the X Register, also produces DC ST INT in the Display Control Logic. This pulse, delayed, (DC ANALOG SETTLEDOWN) is the trigger for the DCD gates which enable the three brightness determining delays. The delay associated with DC ANALOG SETTLEDOWN allows the DAC outputs to stabilize, thereby preventing the displayed point from smearing. The outputs of the three brightness delays, DC BR LOW, DC BR MED and DC BR HI, are applied to input pins K, J, and L, respectively of the W681 Scope Intensifier where the duration of assertion of these negative levels determines the duration of the output of the Intensifier. The Intensifier output (+10V or -15V depending on the OR of the inputs) is taken from pin N and applied to the cathode circuit of the CRT via the Z axis input, where longer duration pulses cause brighter displays. Depending on the status of ST BR00 and ST BR01, one of the following four display intensity levels may be obtained:

ST BR00	ST BR01	Level
1	0	No Brightness
1	1	Low
0	0	Medium
0	1	High

The delay associated with DC BR LOW is the shortest of the three and corresponds to the low brightness level. DC BR MED is asserted negatively for a longer period than DC BR LOW but for a shorter time

than DC BR HI. When both ST BR00 and ST BR01 are set, all three levels are asserted; however, only DC BR HI is considered because its delay exceeds the delay of DC BR LOW and DC BR MED and all are triggered simultaneously by DC ANALOG SETTLEDOWN.

4.4 CONDITIONS IN INSTRUCTION CONI

The assertion of IOB CONI by the processor produces IOBC DPY CONI (A) and (B) in the I/O Bus Control Logic. IOBC DPY CONI (A) causes the states of the following flip-flops to be tested and read onto the indicated IOB lines:

Flip-Flop	IOB Bit
ST HI SPEED	20
ST TEST MODE	21
ST BUSY	22
ST LP FLAG	23
ST DONE	24
ST BR00	27
ST BR01	28

Similarly, IOBC DPY CONI (B) tests the status of the following flip-flops, reading their states onto the indicated IOB lines:

Flip-Flop	IOB Bit
ST LP PI00	30
ST LP PI01	31
ST LP PI02	32
ST DONE PI00	33
ST DONE PI01	34
ST DONE PI02	35

4.5 DATA IN INSTRUCTION - DATAI

The assertion of IOB DATAI by the processor produces IOBC DPY DATAI (A) and (B) in the I/O Bus Control Logic. IOBC DPY DATAI(A) causes the contents of Y00 through 09 to be read into IOB08 through 17, while IOBC DPY DATAI(B) causes the contents of X00 through 09 to be read into IOB26 through 35.

These operations result in the contents of the X and Y registers being read into IOB bits 08 through 17 and 26 through 35 and stored in the computer memory in the location specified by the program.

4.6 OTHER LOGIC

To preserve the continuity of the previous logic discussion, the logic contained in this section was intentionally omitted. In some instances, the sequence of operations, as previously discussed, were qualified by conditions described in the following.

4.6.1 CROBAR

The CROBAR level is positively asserted for four seconds after power comes up and for four seconds prior to power down. One condition necessary for the generation of IOBC DPY SEL is ~CROBAR; therefore, the VP10 cannot be placed in operation during the period of CROBAR assertion. CROBAR also generates IOBC DPY DATAO CLR X & Y and IOBC DPY CONO CLR in the I/O Bus Control Logic which clears the X and Y registers and all STATUS flip-flops respectively.

4.6.2 HI SPEED

In the following discussion all timing is referenced to the RM503 oscilloscope display. Normal settings of the oscilloscope X and Y input sensitivities are 2V/cm. The VP10 has provisions for operating at two speeds designated HI SPEED and ~HI SPEED. IOB bit 20 in a CONO determines the mode. In the HI SPEED mode, the DONE flag is set 19.4 μs following a DATAO (when the high brightness level has been selected), while in the ~HI SPEED mode, DONE is set 100 μs following the DATAO. Assuming that the Central Processor is granting Priority Interrupt requests when they are made, it is therefore possible to plot over 50,000 points per second in HI SPEED and 10,000 points per second in ~HI SPEED.

HI SPEED is set through a DCD gate qualified by IOB 20 (B) (1) and triggered by IOBC DPY CONO SET. The ST DONE Flag is set through a DCD gate qualified by HI SPEED and triggered by ST DPY DONE. The assertion of ST DPY DONE is dependent upon the enabling of a DCD gate qualified by TEST MODE (0)

and triggered by ~DP LP STROBE. The DONE flag is set by the positive going transition of DC LP STROBE 18 μs after the DATAO. The 19.4 μs delay is derived from DC ANALOG SETTLEDOWN (15 μs) and DC BR HI (2 μs) in the Display Control logic.

In the ~HI SPEED mode, HI SPEED is not set due to the IOB 20 (B) (0) condition. The ST DONE flag is set through a DCD gate qualified by ST HI SPEED (0) and triggered by the trailing edge of DC CYCLE SLOW. DC CYCLE SLOW is the combined (100 μs) delay of two 50 μs delays conditioned by ST HI SPEED (0) and triggered by IOBC DPY DATAO SET(X). This sequence results in setting the ST DONE flag 100 μs after each DATAO.

4.6.3 TEST MODE

The Test Mode may be entered by: program instruction CONO 134_8 with IOB21(1), or by pushing the TEST MODE switch on the VP10. DC GO is collector-set by depressing the TEST MODE switch. The trailing edge of the DC GO (1) transition causes generation of DC ST INT, initiating the sequence of events described in Section 4.3. Release of the TEST MODE switch, or assertion of IOBC DPY CONO CLR, resets the DC GO flip-flop.

A DCD gate, qualified by ST TEST MODE (1) and triggered by DC DEL START INT, generates DC ST INT and activates the display brightness circuitry. The DC GO (1) level collector-sets ST BR01 to provide the high brightness level, if the TEST MODE switch has been depressed. If under program control, the display brightness is determined by IOB bits 27 and 28 as before.

TEST MODE (1) with DC BR HI asserted, sets Y09 and X09 and causes the sequential setting of X08 through 00 and Y08 through 00, resulting in a diagonal line display on the oscilloscope. Both the X and Y registers are connected as ripple delay counters. The positive-going transition of ~DC BR HI sets X09 and Y09 through DCD gates as shown on the X-Y Buffer Drawing. The next assertion of ~DC BR HI clears X09 and Y09. Connections between the flip-flops are such that when X09 and Y09 change state from 1 to 0, X08 and Y08 are set. Similarly, X07 and Y07 are set and cleared by the positive transitions of X08 and Y08 as they change state from 1 to 0. The operation of the remainder of the counter is identical. X09 and Y09 change states on every assertion of ~DC BR HI; X08 and Y08 on every second assertion; X07 and Y07 on every fourth assertion; etc.

DC DEL ST INT provides a delay between the display of successive points to allow sufficient time for the carries to cease and for the DACS to settle in the new state.

4.6.4 IOBC RESET

IOBC RESET is generated by depressing the CLR switch, by IOB RESET from the processor, or by CROBAR. The assertion of IOBC RESET produces IOBC DPY DATAO CLR X & Y in the I/O Bus Control Logic and causes the X and Y registers to be cleared. IOBC RESET also generates IOBC DPY CONO CLR which clears all status flip-flops.

4.6.5 LP STROBE

An LP OUTPUT level from the light pen amplifier ANDed with DC LP STROBE collector sets ST LP FLAG. DC LP STROBE causes the light pen to be inactive except while a point is being intensified. ST LP FLAG (1) selects a priority interrupt channel through a binary-to-octal decoder in the status logic. The specific channel (01 through 07) selected depends upon the condition of ST LP PI00 through 02. The decoder output is applied to IOB PI01 through 07.

CHAPTER 5
MAINTENANCE

5.1 SCOPE

This Chapter contains maintenance information for the VP10 Point Plot Display Control. Maintenance procedures relevant to the particular oscilloscope or display in use and other system equipment are contained in the equipment maintenance manual. The following test equipment is required for performance of preventive and corrective maintenance procedures in the VP10:

a. A multimeter with a 20,000 ohms/Vdc Sensitivity.
b. An oscilloscope with properly calibrated sweep and deflection circuits.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to initial operation of the VP10 and periodically thereafter to ensure that the equipment is operating at optimum efficiency and to detect conditions which might lead to subsequent failure of the equipment. Preventive maintenance schedules are primarily based on average usage of the VP10 and down-time limitations.

5.2.1 Mechanical Inspection and Cleaning

Mechanical inspection and cleaning consists of periodically cleaning the interior and exterior of the equipment, checking for signs of deterioration, and cleaning the air filters. The exterior of the equipment should be wiped occasionally with a soft cloth to maintain an attractive appearance. The equipment interior should be vacuumed on a regular schedule depending upon environmental conditions. The mechanical inspection of the equipment can be easily conducted while the cleaning tasks are being accomplished. The blower air filters should be checked as often as required to maintain efficient operation of the cooling system. Remove the mesh filters from the blower assemblies. Shake and vacuum thoroughly before reinstalling. If the filters are excessively dirty or clogged, they should be washed in a detergent solution, dried, and sprayed with Filtercoat®, before reinstallation.

5.2.2 Electrical Inspection

Electrical inspection consists of making measurements of power supply voltages, observing ripple contents to ensure that operation is within the limits specified for the supply in use, and conducting margin checks to aggravate border line conditions within the logic, thereby revealing definite observable faults.

5.2.2.1 DEC Type 728 Power Supply Test Procedures - The +10V and -15V potentials required for operation of the VP10 logic are provided by a single Type 728 Power Supply, mounted on the rear plenum door as shown in Figure 5-1. Both voltages should be read from the terminals at the logic panel end and are not adjustable; therefore, if the voltage and ripple contents are not within the specified limits, the power supply must be either repaired or replaced.

Check the +10V output between the red (+) and black (-) leads. This reading should be between 9.5V and 11V, with less than 700 mV rms ripple. Check the -15V output between the blue (-) and black (+) leads. This reading should be between -14.5V and -16V, with less than 700 mV rms ripple.

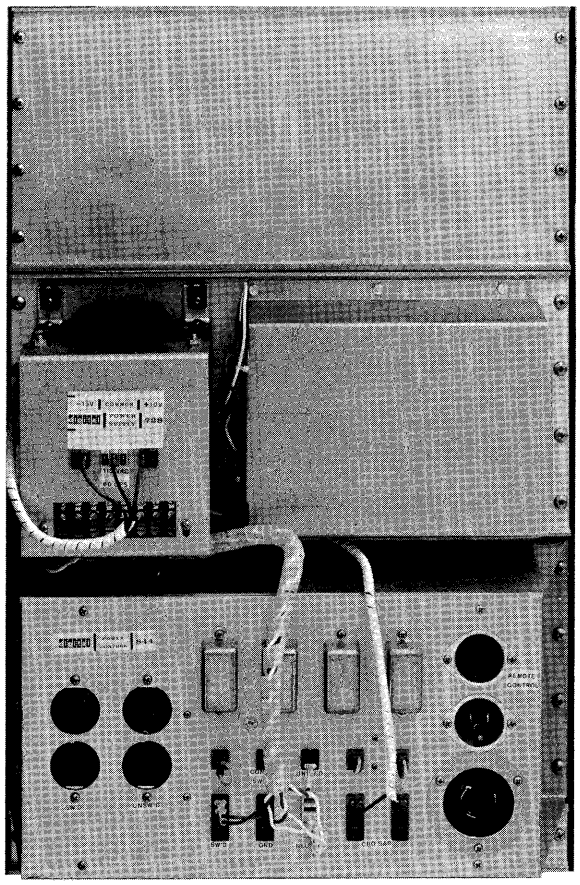


Figure 5-1 Plenum Door Layout

5.2.2.2 DEC Type A704 Reference Supply - The DEC Type A704 Reference Supply provides the -10V reference potential to the digital-to-analog converters. This is a double-height module installed in location AB14 of the logic. The output, measured between pins T (-10V) and C (ground) of location A14, should be within ± 0.1 mV of -10V (from no load to full load) with a ripple content of less than 0.1 mV rms.

5.2.2.3 Margin Checks - VP10 margin checks are accomplished while running the Diagnostic Program, MAINDEC-10-D6Bn* T0, T1, T2, and Test Mode. The toggle switches located on the left front of the logic panels provide selection of VP10 internal power or power supplied through the margin panel. The checks are performed by manually varying the +10V and -15V logic potentials at the Central Processor Margin Control Panel and observing the effects on VP10 operation. Thus, marginal conditions can be corrected prior to an actual failure. These checks are also useful in locating a faulty component causing intermittent failures. Each rack should be tested separately to allow for more precise fault isolation.

The VP10 margin ranges are:

+10V	+2.5V to 17.5V
-15V	-12V to -18V

5.3 CORRECTIVE MAINTENANCE

The VP10 is constructed of highly reliable transistorized modules and standard circuits. The reliability of the equipment, combined with proper performance of the preventive maintenance tasks, ensures minimum down-time due to failure. If a malfunction occurs, analyze the fault and correct the condition as outlined in the following paragraphs. Schematic Diagrams of all modules used in the VP10 logic are contained in Chapter 7 of this Manual.

5.3.1 Preliminary Investigation

The primary purpose of the preliminary investigation is to simplify and, if possible, isolate the fault. If the fault occurred while in a user program, determine from the user what is expected of the program and the particular error. Two valuable maintenance aids, the diagnostic program and the VP10 Test Mode, are described in the following paragraphs.

*Use latest available program version

5.3.2 Diagnostic Program

The diagnostic program which is applicable to VP10 troubleshooting is MAINDEC-10-D6Bn. This program is arranged in three sections designated T0, T1, and T2. In Section T0, all flags are tested. Section T1 allows one of four patterns to be displayed in a dynamic test. Section T2 tests the light pen. A complete description is contained in the write-up which accompanies the program.

If the fault cannot be isolated using the diagnostic program, run the user program that failed, simplifying it with the user's help, if possible.

5.3.3 Test Mode

The Test Mode is initiated by first depressing the CLR and then the TEST MODE switch on the VP10 Switch and Connector Panel. When in the Test Mode, self-contained logic places the VP10 in a loop independent of Central Processor control. The Test Mode display is a high intensity diagonal line as shown in Figure 5-2. Most of the logic contained in the VP10 is used during Test Mode operation. The following logic sections are exercised:

a. ST BR 01
b. X and Y Buffers
c. All DACs
d. HI SPEED
e. All the Display Intensity Control logic

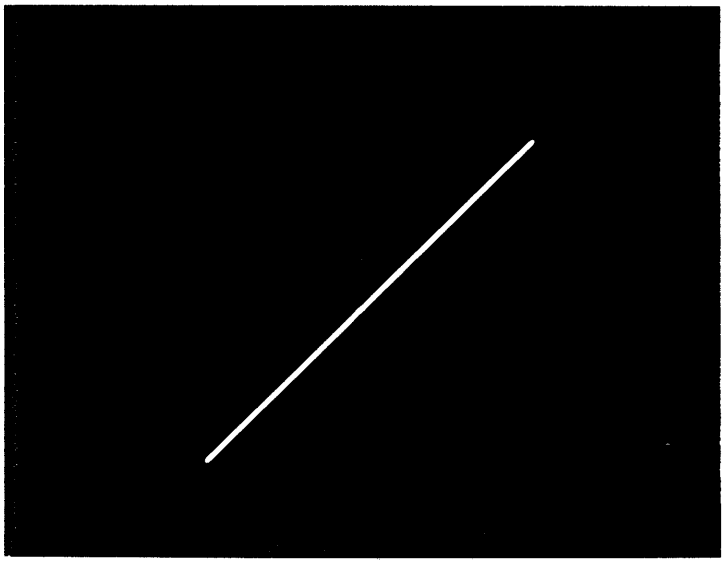


Figure 5-2 Test Mode Display

5.3.4 Signal Tracing

When a malfunction has been detected and the VP10 is in a loop, either in the Diagnostic Program or while in the Test Mode, use an oscilloscope to trace signal flow through suspected elements. In this manner, the quality of pulse amplitude, duration, rise time, and timing may be observed. If the malfunction occurs intermittently, combine signal tracing with a margin check or other form of aggravation test.

5.3.5 Validation Test

After replacement of any electrical component, perform a test to ensure that the malfunction has been corrected and to determine if adjustments are necessary. This test normally consists of the corrective maintenance tasks (i.e., Diagnostic Program and Test Mode, as well as margin checks), or if the problem was not exhibited by these procedures, the user program in which the failure was originally detected. When time permits, it is suggested that the entire preventive maintenance procedure be performed as a validation test.

5.3.6 Log Entry

Corrective maintenance procedures are not completed until the action taken has been recorded in the maintenance log. Record all data concerning the symptoms of the malfunction, method of isolation, and any other pertinent information.

CHAPTER 6
PARTS LIST

6.1 SCOPE

This chapter contains a listing of the VP10 logic modules, power supplies and semiconductors. The indicated spare stock quantities are based on percentages of the total quantity of each component installed in the VP10. The actual quantity of spare parts to be stocked depends on down-time tolerance and system reliability requirements.

6.2 MODULES

Table 6-1 is a listing of VP10 modules with the total of each type installed and suggested spare quantities.

Table 6-1
VP10 Module Requirements

DEC Type Number	Quantity in Use	Suggested Spares
A601	8	1
A704	1	1
B152	2	1
B163	6	1
R002	3	1
R201	2	1
R302	5	1
R613	2	1
S107	1	1
S111	1	1
S203	2	1

Table 6-1 (Cont)
VP10 Module Requirements

DEC Type Number	Quantity in Use	Suggested Spares
S205	10	1
W005	1	1
W012	3	1
W023	1	1
W107	4	1
W250	3	1
W681	1	1
W851	6	1
W990	4	1

6.2.1 Semiconductors

Table 6-2 is a listing of VP10 semiconductor types with the total number installed and suggested spare quantities.

Table 6-2
VP10 Semiconductor Requirements

DEC Designation	EIA Designation	Number in Use	Suggested Spares
1N3499	1N3499	1	1
2N1305	2N1305	48	5
2N3605	2N3605	10	1
2N4258	2N4258	18	2
D662	1N645	700	10
D664	1N3606	1792	20
D670	1N3653	5	1
DEC2894-2	None	6	1
DEC2894-3	None	26	3
DEC2219A	None	2	1

Table 6-2 (Cont)
VP10 Semiconductor Requirements

DEC Designation	EIA Designation	Number in Use	Suggested Spares
DEC3009	2N3009	26	3
DEC3638B	2N3638	12	1
DEC3639	2N3639	42	4
DEC3639B	2N3639	98	10
DEC3639C	2N3639	65	7
DEC3639-0	2N3639	12	1
DEC6534	None	10	1
DEC6534B	MPS6534	40	4
SDA-6	2N2060	2	1

6.2.2 Power Supplies

DEC Type Number	Number in Use	Suggested Spares
728	1	0
844 (Power Control)	1	0

6.2.3 Indicator Lamps

DEC Type Number	Number in Use	Suggested Spares
12-00555	34	4

CHAPTER 7
ENGINEERING DRAWINGS

7.1 SCOPE

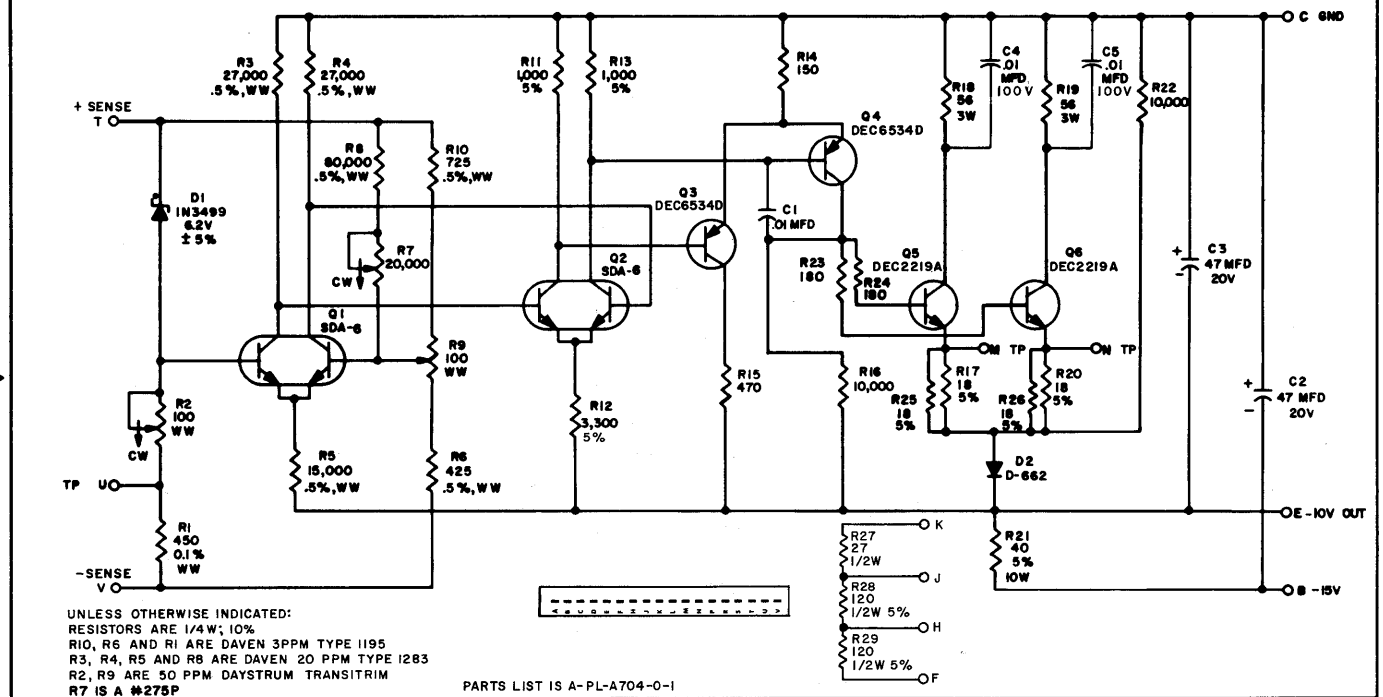
This chapter contains block schematics, circuit schematics, and other engineering drawings necessary to understand and maintain the VP10. Only those drawings which are essential, and not available in the referenced pertinent documents, are included. If any discrepancy exists between the drawings in this chapter and those supplied with the equipment, assume that the equipment drawings are correct. Appendix A of Volume 1 of the KA10 Central Processor Maintenance Manual contains a discussion of flow diagram and schematic drawing interpretation; chapter 1 of Volume 2 describes the DEC engineering drawing numbering system.

Table 7-1
Engineering Drawing List

Table 7-1 (Cont)
Engineering Drawing List

Drawing Number	Title	Page
B-CS-W023-0-1	Connector	7-10
B-CS-W107-0-1	I/O Bus Receiver Ckt.	7-11
B-CS-W250-0-1	Indicator Cable Connector	7-11
B-CS-W681-0-1	Scope Intensifier	7-12
C-CS-W851-0-1	PDP-10 Bus Connector Board	7-13
D-BS-VP10-0-DC	Display Control DC	7-15
D-BS-VP10-0-IOBC	I/O Bus Control Logic	7-17
D-IC-VP10-0-IOBI	I/O Bus Interface IOBI	7-19
D-BS-VP10-0-IOB	I/O Bus Interface IOB	7-21
D-BS-VP10-0-ST	Status ST	7-23
D-BS-VP10-0-XYB	X-Y Buffers XYB	7-25
A-PL-VP10-0-0	Point Plot Display Interface (3 sheets)	7-27,28
D-MU-VP10-0-2	Module Utilization	7-29
D-IC-VP10-0-4	Wiring, Power VP10 (2 sheets)	7-31, 33
A-PL-7006041-0-0	Wired Assembly	7-35
C-CS-844-0-1	Power Control 844	7-36
B-CS-728-0-1	Power Supply 728	7-37

SIZE B | CODE CS | NUMBER A704-0-1 | REV K



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
R10, R6 AND R1 ARE DAVEN 3PPM TYPE 1195
R3, R4, R5 AND R8 ARE DAVEN 20 PPM TYPE 1283
R2, R9 ARE 50 PPM DAYSTRUM TRANSITRIM
R7 IS A #275P

PARTS LIST IS A-PL-A704-0-1

REVISIONS	CHK	CHG NO	REV
	DAW	4535	4
	REV	5751	E
		5849	F
		5900	H
		6762	J
		00001	K

DRN.	A.OUELLETTE	DATE 9-3-64
CHK'D	N. PERRYMAN	DATE 9-4-64
ENG.	R.A.GAGNE	DATE 9-4-64
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
SDA-6	2N2060		
DEC6534D	SAME		
DEC2219A	SAME		
D662	IN645		
IN3499	SAME		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

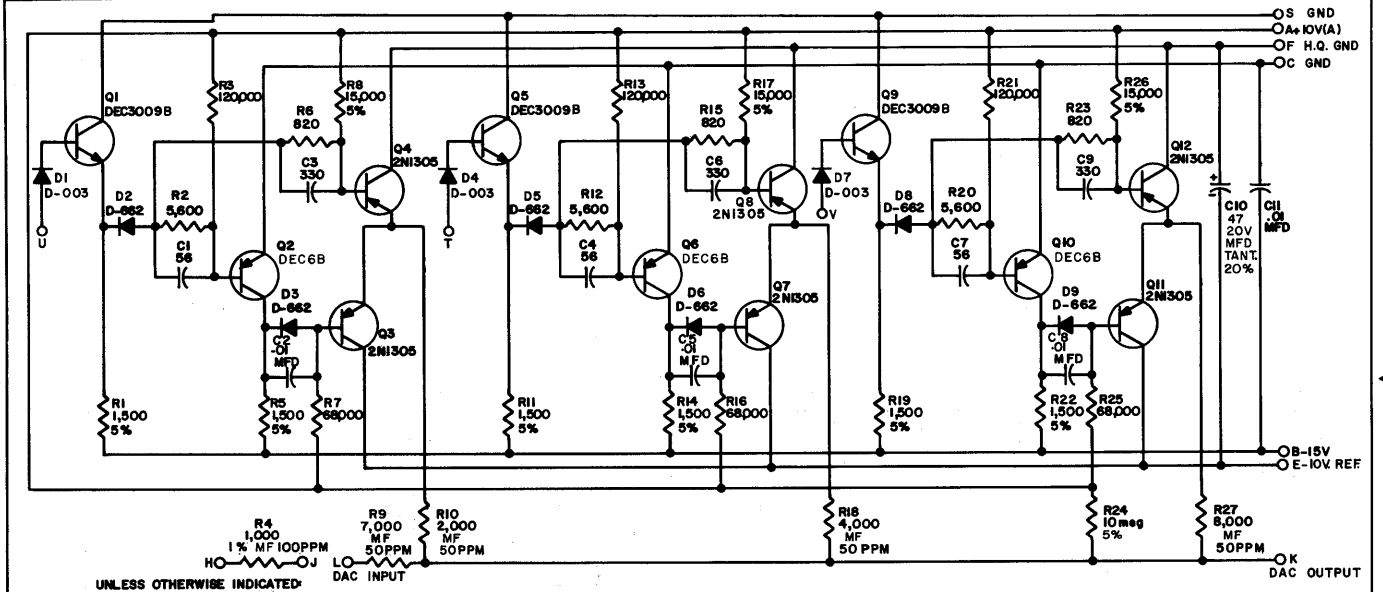
TITLE -10V PRECISION POWER SUPPLY A704

SIZE	CODE	NUMBER	REV.
B	CS	A704-0-1	K

PRINTED CIRCUIT REV. F

DEC FORM NO. DRB 102

SIZE B | CODE CS | NUMBER A601-0-1 | REV J



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
MF RESISTORS ARE 0.1%; 1/8W
CAPACITORS ARE MMFD

NOTE:
WHEN USED AS THE LEAST SIGNIFICANT BIT, CONNECT J TO L AND CONNECT H TO H.Q. GND.

PARTS LIST A-PL-A601-0-0

REVISIONS	CHK	CHG NO	REV
	DAW	4459	2
	REV	5606	D
		5618	
		5728	E
		5836	F
		6756	H
		7004	J

DRN.	H. PORTER	DATE 9-15-64
CHK'D	N. PERRYMAN	DATE 9-30-64
ENG.	R. SORENSEN	DATE 9-30-64
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
2N1305	SAME		
DEC6B	NONE		
DEC3009B	2N3009		
D003	IN994		
D662	IN645		

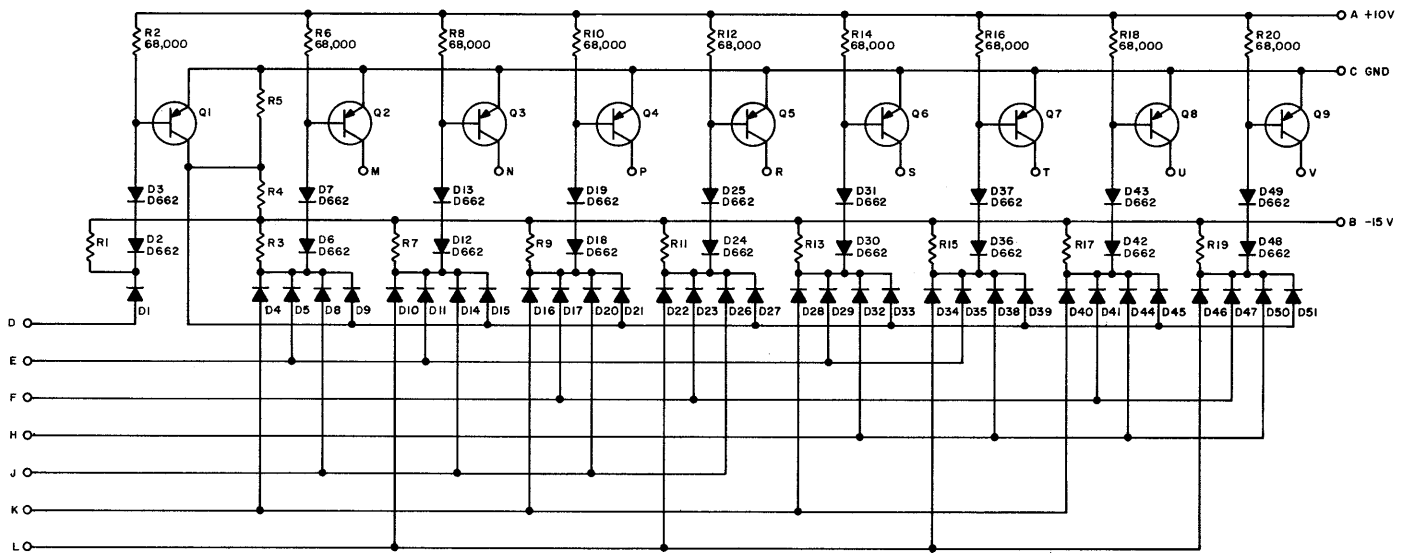
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE 3 BIT DAC A601

SIZE	CODE	NUMBER	REV.
B	CS	A601-0-1	J

PRINTED CIRCUIT REV. D

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 7,500
RESISTORS ARE 1/4W, 5%
DIODES ARE D664
TRANSISTORS ARE 2N4258

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N4258	SAME		
D662	IN645		
D664	IN3606		

REVISIONS | CHK | CHG NO. | REV.

DRN. Jo. Walker	DATE	5-17-67
CHK'D P. Solomon	DATE	5/17/67
ENG. A. Kotok	DATE	5-23-67
PROD.	DATE	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

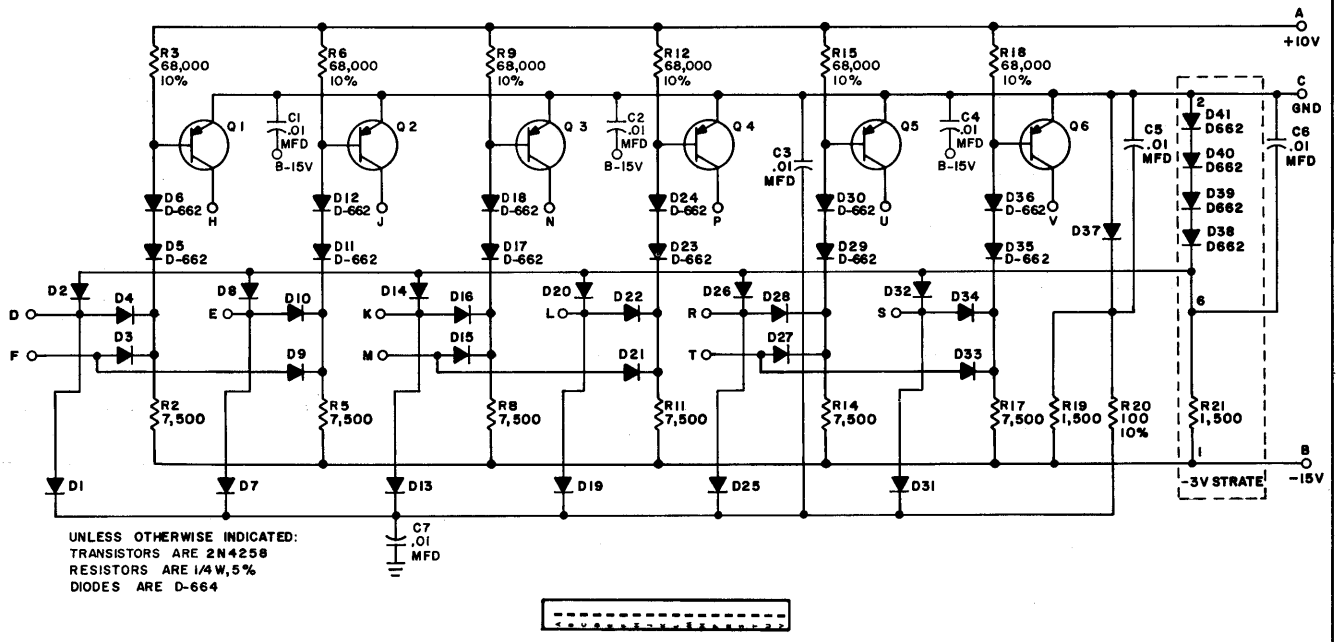
TITLE BINARY TO OCTAL DECODER B152

SIZE	CODE	NUMBER	REV.
C	CS	B152-0-1	

PRINTED CIRCUIT REV. A

DEC FORM NO. DRC 102

SIZE C | CODE CS | NUMBER B152-0-1 | REV.



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE 2N4258
RESISTORS ARE 1/4W, 5%
DIODES ARE D-664

REVISIONS			
REV.	A	B	C	D
CHG NO.	5913	5991	6212	
CHK				

DRN.		DATE 9-30-66
CHK'D	A. Silverman	DATE 10/3/66
ENG.	Allan Kent	DATE 10 Oct 66
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
2N4258	2N4258		
D662	IN645		
D664	IN3606		

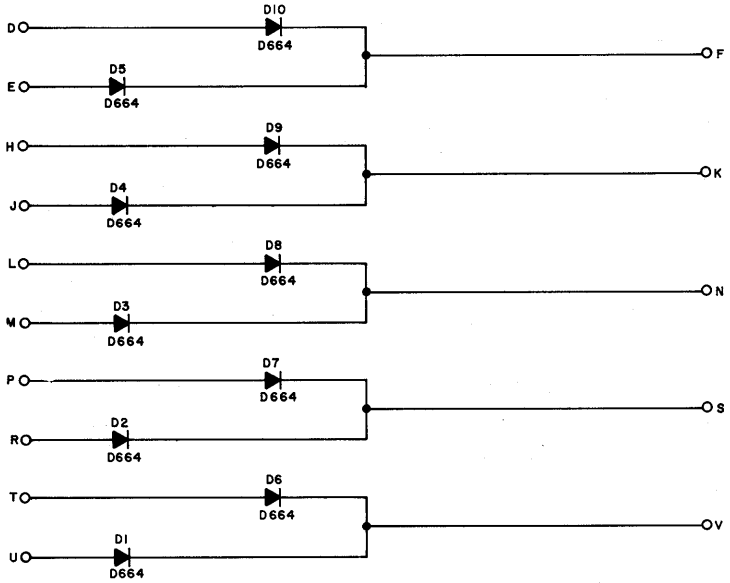
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DIODE GATE B163

SIZE	CODE	NUMBER	REV.
B	CS	B163-0-1	D

PRINTED CIRCUIT REV. D

DEC FORM NO. DRB 102



REVISIONS		
REV.	A	
CHG NO.	REDR.	
CHK	5537	

DRN.	H. PORTER	DATE 5-21-64
CHK'D	N. PERRYMAN	DATE 5-25-64
ENG.	R. BANK	DATE 5-25-64
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D664	IN3606		

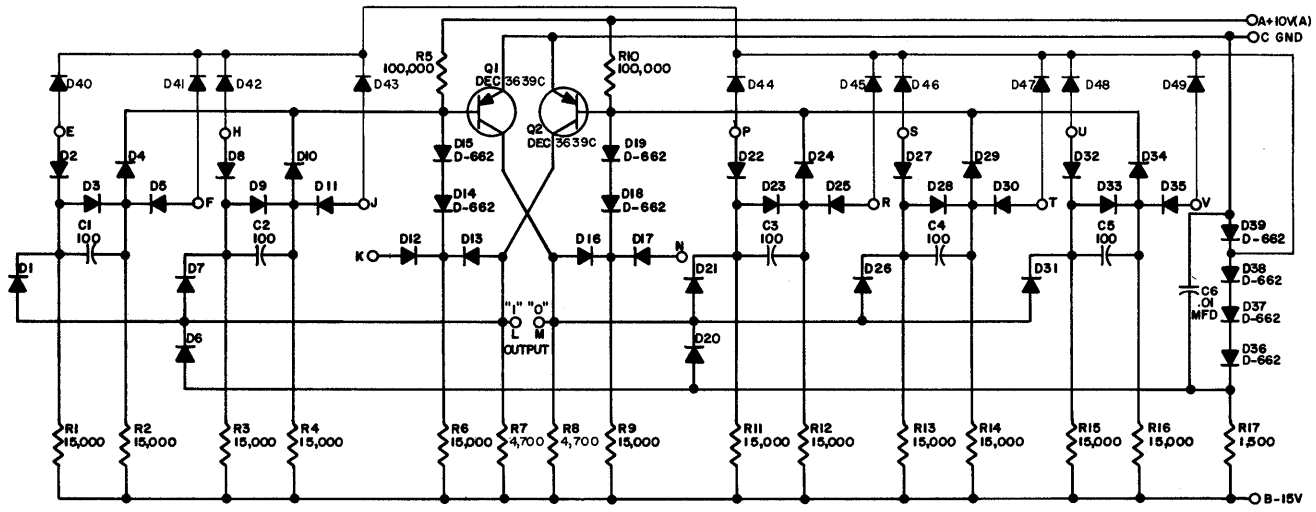
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DIODE CLUSTER R002

SIZE	CODE	NUMBER	REV.
B	CS	R002-0-1	A

PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664

REVISIONS	CHK	CHG NO.	REV.
	RMS	6329	3
	REV'D	REDR. 6548	D

DRN. H.W.PORTER	DATE 5-19-64	
CHK'D N.PERRYMAN	DATE 5-25-64	
ENG. R.BANK	DATE 5-25-64	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3639C	2N3639		

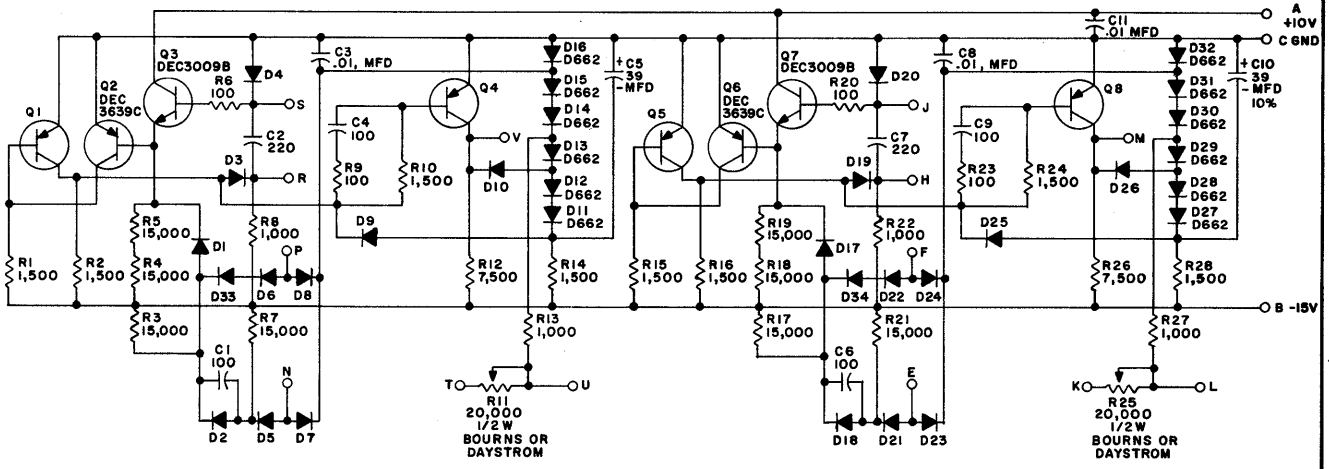
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: FLIP-FLOP R201

SIZE	CODE	NUMBER	REV.
B	CS	R201-0-1	D

PRINTED CIRCUIT REV. C D

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC3639

PARTS LIST A-PL-R302-0-0

REVISIONS	CHK	CHG NO.	REV.
	DAW	4856	7
	REV'D	REDR. 5538	J
	Fink	5978	K
	Fink	6499	P
	Fink	6696	R
	Fink	6749	S

DRN. A.OUELLETTE	DATE 6-12-64	
CHK'D N.PERRYMAN	DATE 6-17-64	
ENG. R. BANK	DATE 6-17-64	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3639	2N3639		
DEC3009B	2N3009		
D662	IN645		
D664	IN3606		
DEC3639C	2N3639		

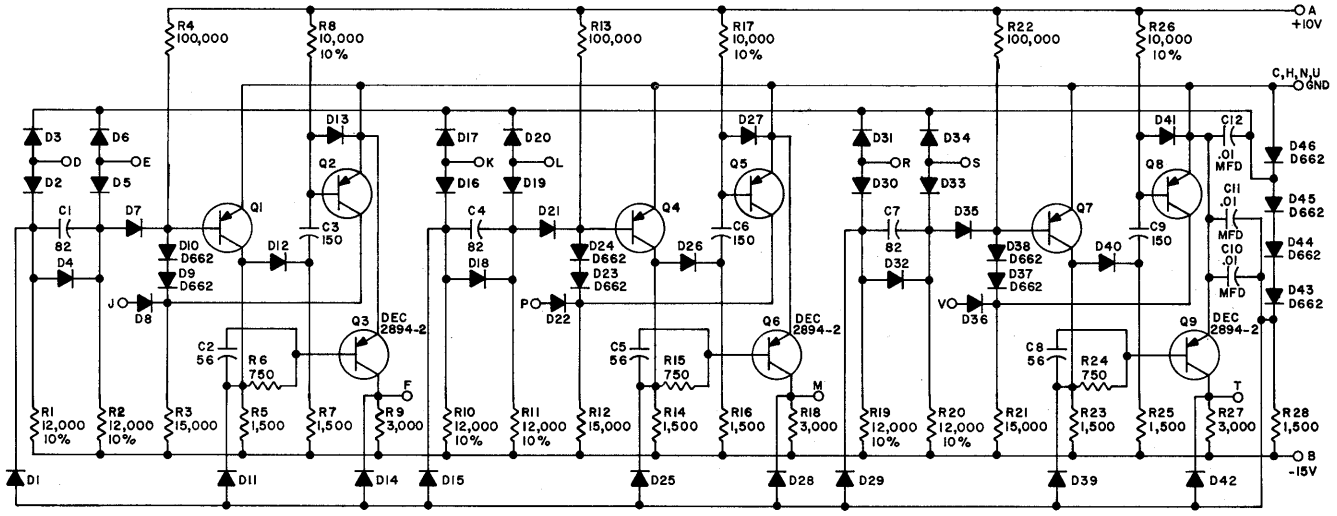
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DELAY R302

SIZE	CODE	NUMBER	REV.
B	CS	R302-0-1	S

PRINTED CIRCUIT REV. K

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D664
TRANSISTORS ARE DEC 3639-0

REVISIONS	CHK	CHG NO	REV
		5681	A
		6559	B

DRN.		DATE 4/29/66
CHK'D		DATE 6/3/66
ENG.		DATE 5/31/66
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC 3639-0	2N3639		
DEC 2894-2	NONE		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PULSE AMPLIFIER R613

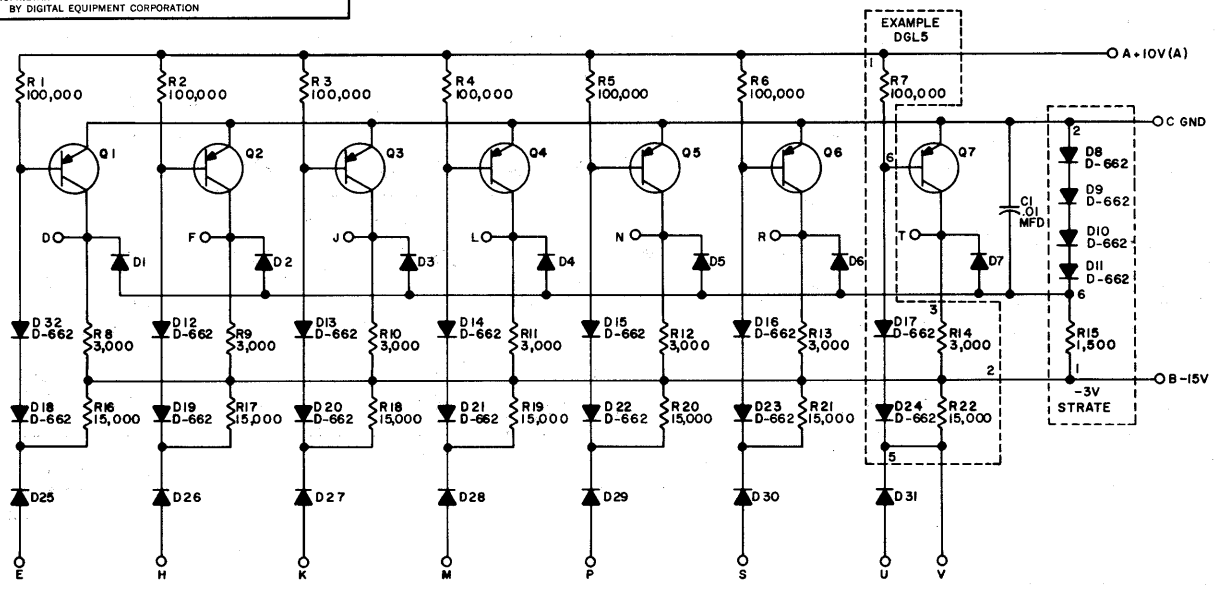
SIZE	CODE	NUMBER	REV.
B	CS	R613-0-1	B

PRINTED CIRCUIT REV. A B

DEC FORM NO. DRB 102

SIZE B | CODE CS | NUMBER R613-0-1 | REV. B

SIZE B | CODE CS | NUMBER S107-0-1 | REV. D



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664
TRANSISTORS ARE DEC 3639B
PRINTED CIRCUIT REV. FOR
DGL BOARD IS SIA

USE THE ETCH BOARD OF THE R107

PARTS LIST A-PL-S107-0-0

REVISIONS	CHK	CHG NO	REV
REV B REDR.		5384	B
		5458	C
		6857	D

DRN.	I HAHN	DATE 6-11-65
CHK'D	R SILVERMAN	DATE 6-18-65
ENG.	R SOGGE	DATE 6-18-65
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC 3639B	2N3639		
D662	IN645		
D664	IN3606		

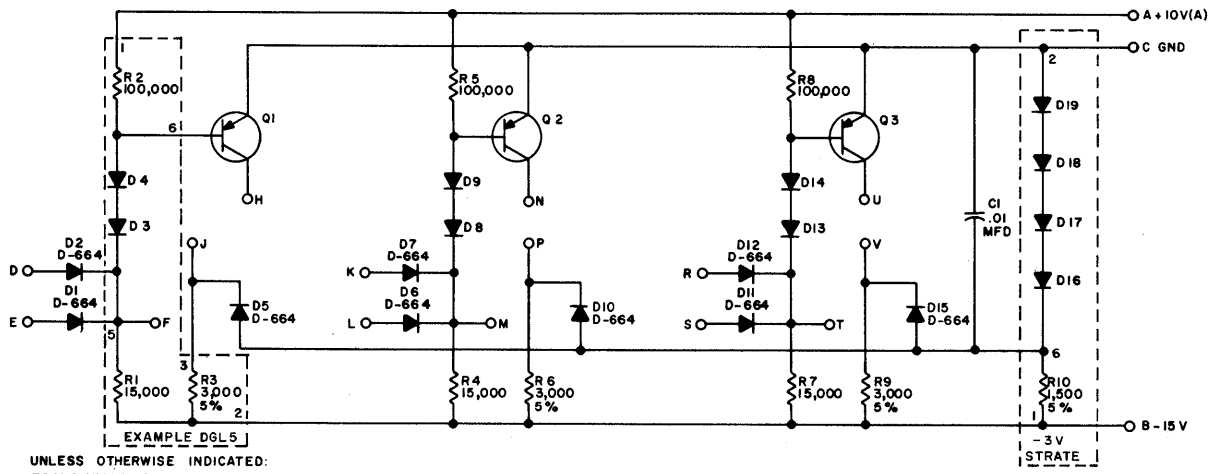
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: INVERTER S107

SIZE	CODE	NUMBER	REV.
B	CS	S107-0-1	D

PRINTED CIRCUIT REV. D

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC 3639
RESISTORS ARE 1/4W; 10%
DIODES ARE D-662
PRINTED CIRCUIT REV. FOR DGL BOARD IS SIA

USE THE ETCH BOARD OF THE R111

REVISIONS			
CHK	CHG NO.	REV.	
	REV. & REDR.	B	
	5365		
	5460	C	
	6750	D	

DRN. I HAHN	DATE 6-10-65	
CHK'D R SILVERMAN	DATE 6-18-65	
ENG. R SOGGE	DATE 6-18-65	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3639	2N3639		
D662	IN645		
D664	IN3606		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DIODE GATE S111

SIZE	CODE	NUMBER	REV.
B	CS	S111-0-1	D

PRINTED CIRCUIT REV. D F

DEC FORM NO. DRB 102

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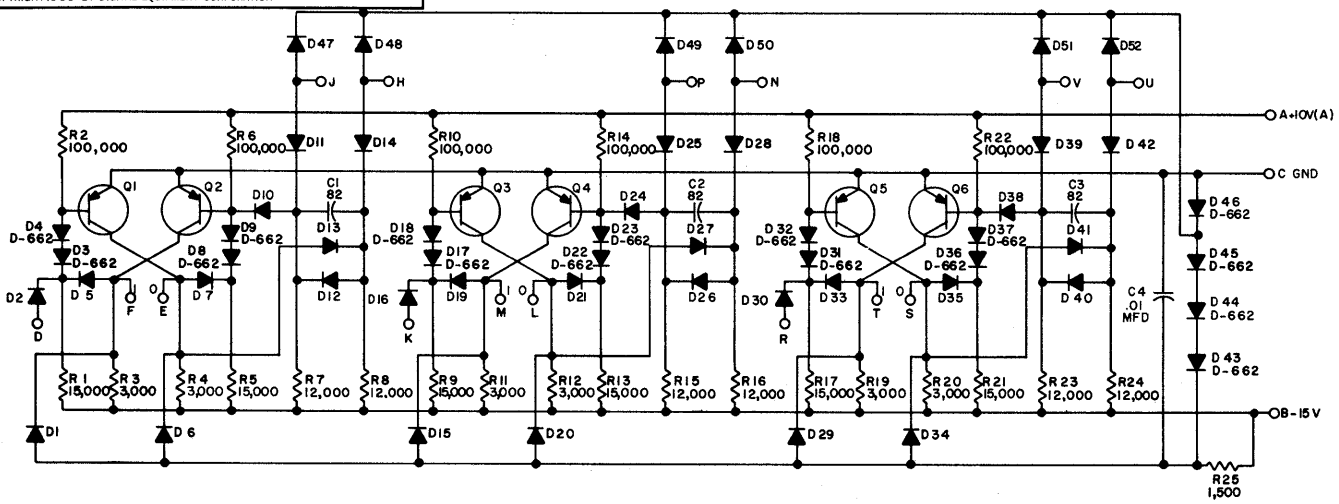


UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639C

USE THE ETCH BOARD OF THE R203

REVISIONS			
CHK	CHG NO.	REV.	
DAW	4990	I	
	REV. & REDR.	B	
	5468		
	6494	C	

DRN. I. HAHN	DATE 6-11-65	
CHK'D R. SILVERMAN	DATE 6-18-65	
ENG. R. SOGGE	DATE 6-18-65	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3639C	2N3639		
D662	IN645		
D664	IN3606		

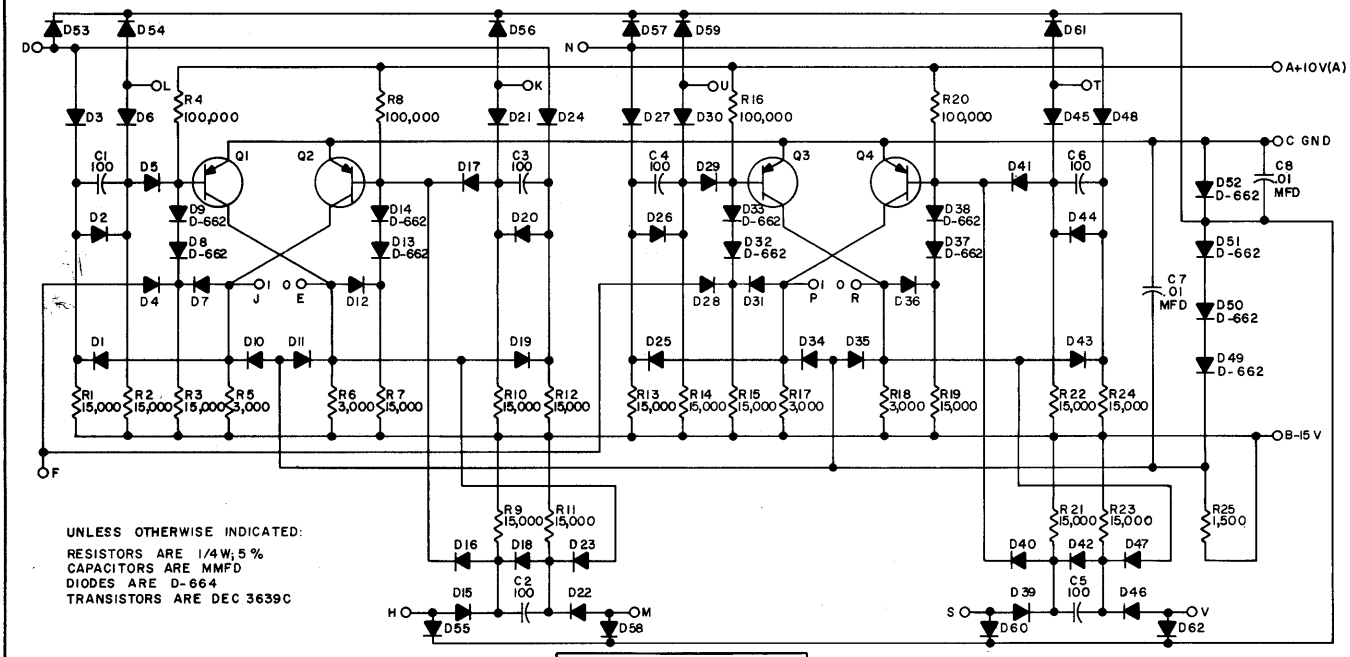
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: TRIPLE FLIP-FLOP S203

SIZE	CODE	NUMBER	REV.
B	CS	S203-0-1	C

PRINTED CIRCUIT REV. D

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5 %
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 3639C

PARTS LIST A-PL-S205-0-0

USE THE ETCH BOARD OF THE R205

REVISIONS	CHK	CHG NO.	REV
	DAW	4999	2
	REV	B REDR	C
	Chk	6492	
	Chk	6853	D

DRN. I. HAHN	DATE	6-14-65
CHK'D R. SILVERMAN	DATE	6-18-65
ENG. R. SOGGE	DATE	6-18-65
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC3639C	2N3639		
D662	IN645		
D664	IN3606		

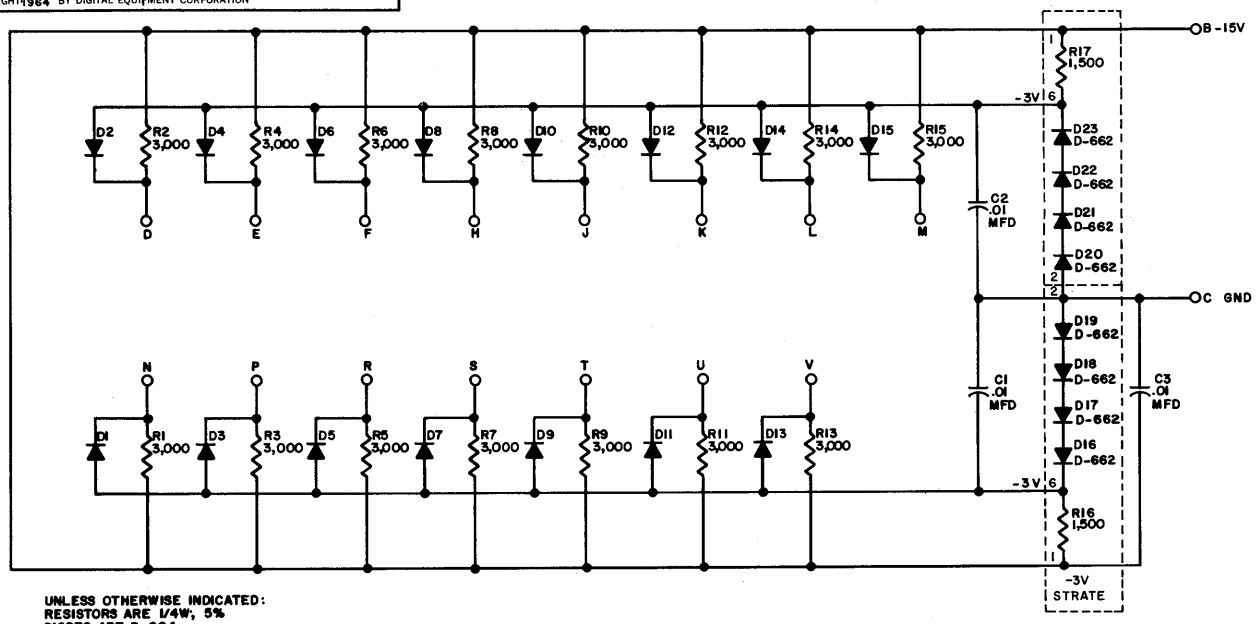
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: DUAL FLIP FLOP S205

SIZE	CODE	NUMBER	REV.
B	CS	S205-0-1	D

PRINTED CIRCUIT REV. D

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D-664

REVISIONS	CHK	CHG NO.	REV
	DAW	5037	1
	REV	B REDR.	B
	Chk	5397	

DRN. H. PORTER	DATE	4-27-64
CHK'D N. PERRYMAN	DATE	5-4-64
ENG. B. SCUDNEY	DATE	5-4-64
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	IN645		
D664	IN3606		

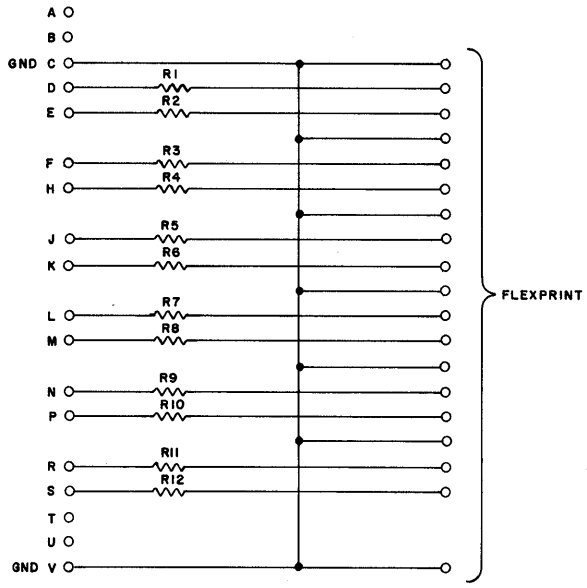
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CLAMPED LOADS W005

SIZE	CODE	NUMBER	REV.
B	CS	W005-0-1	B

PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-W012-0-0
R1 - R12	RES. 1.5K 1/4W 5% CC	1300391

PARTS LIST

REVISIONS	CHK	CHG NO.	REV.
	REV B RED	5832	A
		7146	B

DRN.	M. HALLER	DATE 11-1-66
CHK'D	R. SILVERMAN	DATE 11-1-66
ENG.	J. SIMEONE	DATE 11-11-66
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

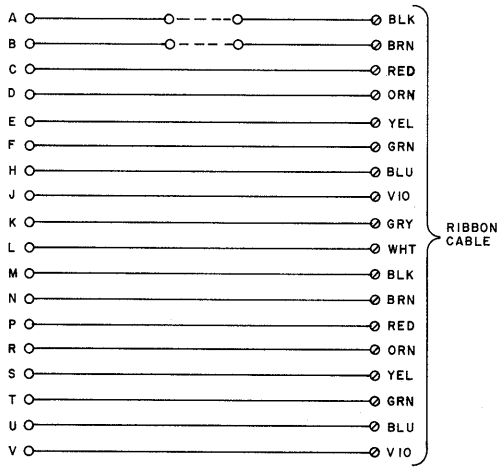
TITLE: INDICATOR CABLE CONNECTOR W012

SIZE	CODE	NUMBER	REV.
B	CS	W012-0-1	B

PRINTED CIRCUIT REV. B C

DEC FORM NO. DRB 102

SIZE B | CODE CS | NUMBER W012-0-1 | REV. B



NOTE:
Ø ARE SPLIT LUGS

PARTS LIST IS A-PL-W023-0-0

REVISIONS	CHK	CHG NO.	REV.

DRN.	M. Haller	DATE 10-16-68
CHK'D	M. Haller	DATE 10-18-68
ENG.	R. Goldberg	DATE 11-12-68
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

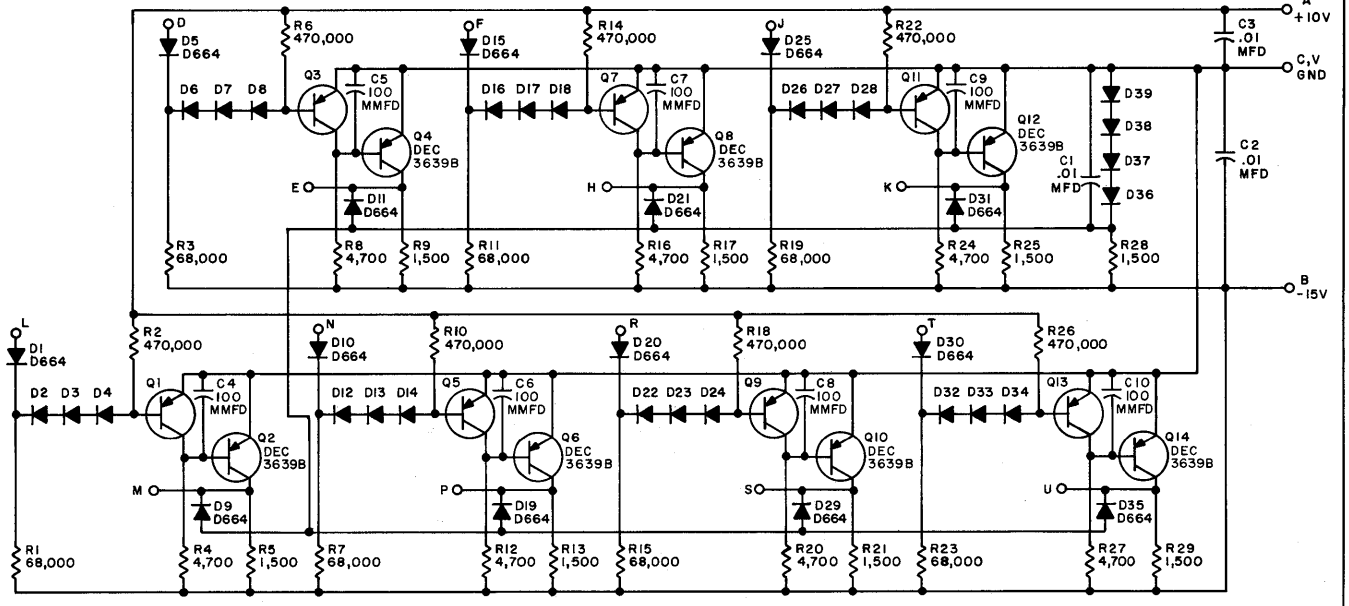
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CONNECTOR W023

SIZE	CODE	NUMBER	REV.
B	CS	W023-0-1	

PRINTED CIRCUIT REV. A

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 5%
DIODES ARE D662
TRANSISTORS ARE DEC3639C

REVISIONS					
CHK	CHG NO.	REV.			
Rad	6827	A			

DRN.	M. Waller	3-13-67
CHK'D.	R. Schumann	3/15/67
ENG.	K. Bodley	3/21/67
PROD.		

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	IN645		
D664	IN3606		
DEC3639B	2N3639		
DEC3639C	2N3639		

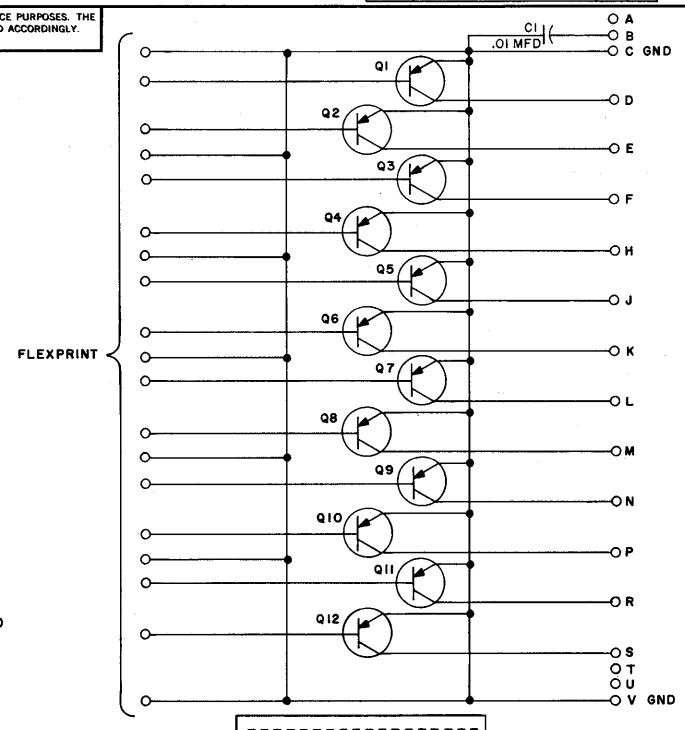
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: I/O BUS RECEIVER CKT. W107

SIZE	CODE	NUMBER	REV.
B	CS	W107-0-1	A

PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102



UNLESS OTHERWISE INDICATED:
TRANSISTORS ARE DEC6534D

PARTS LIST A-PL-W250-0-0

REVISIONS					
CHK	CHG NO.	REV.			
Rad	6835	B			
Rad	6989				
Rad	7036				

DRN.	M. Waller	11-29-66
CHK'D	R. Schumann	11/30/66
ENG.	Allan Kent	12/1/66
PROD.		

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC6534D	MPS6534		

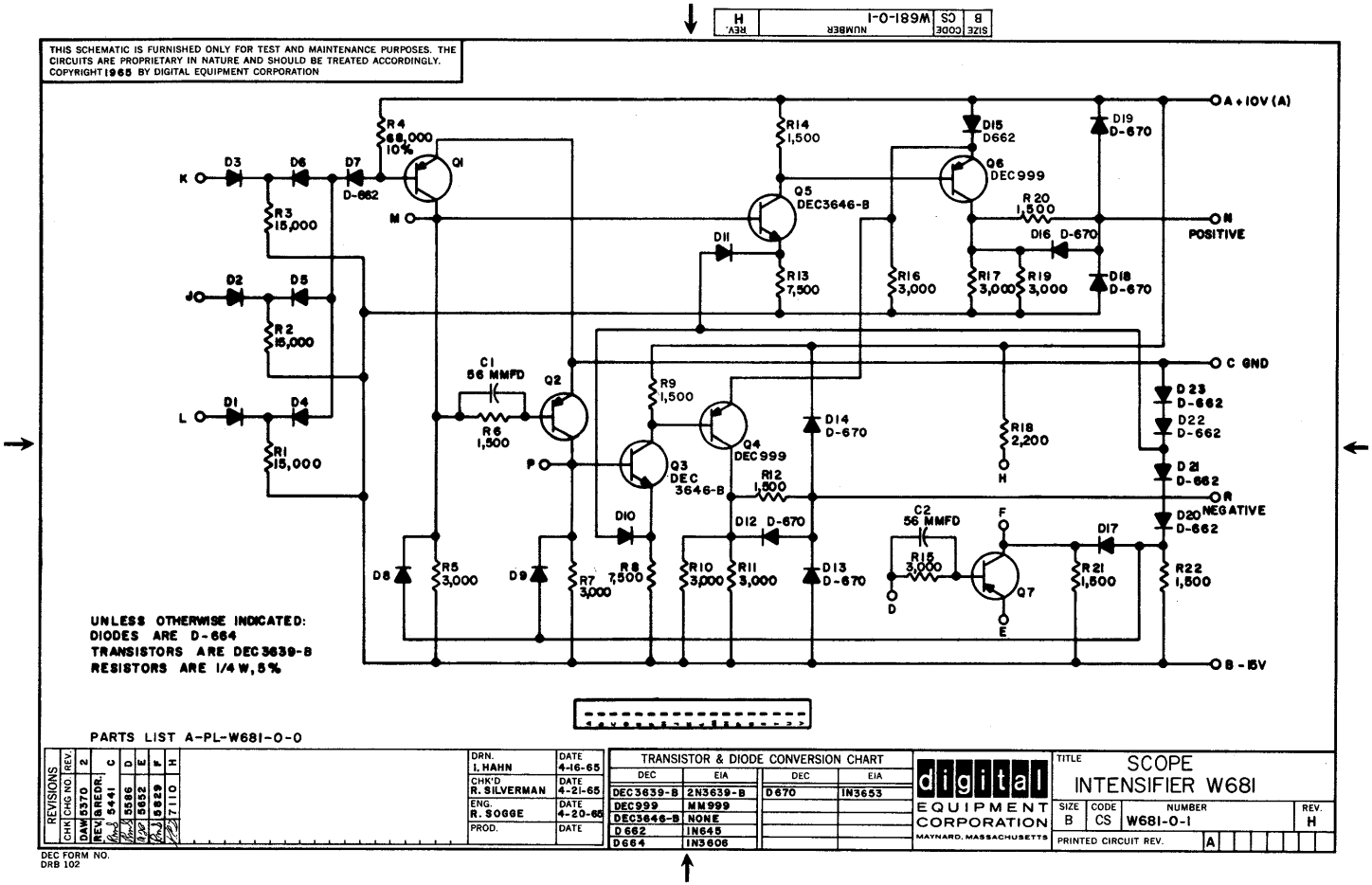
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: INDICATOR CABLE CONNECTOR W250

SIZE	CODE	NUMBER	REV.
B	CS	W250-0-1	B

PRINTED CIRCUIT REV. A B

DEC FORM NO. DRB 102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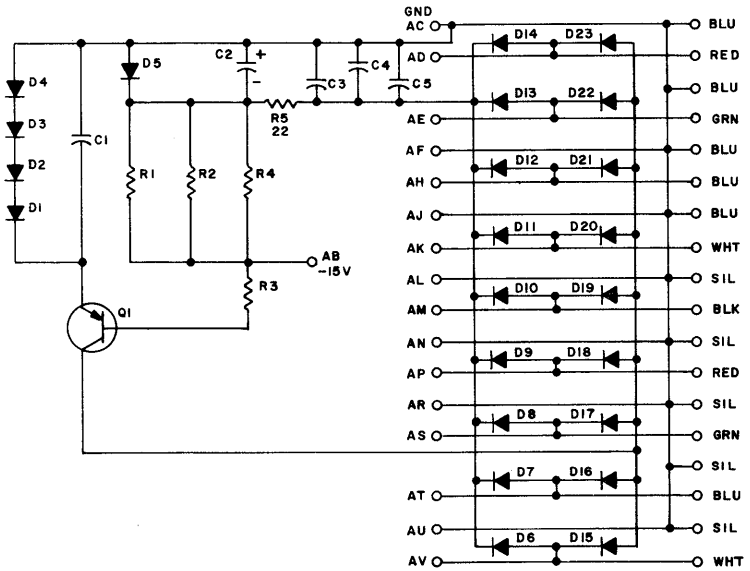
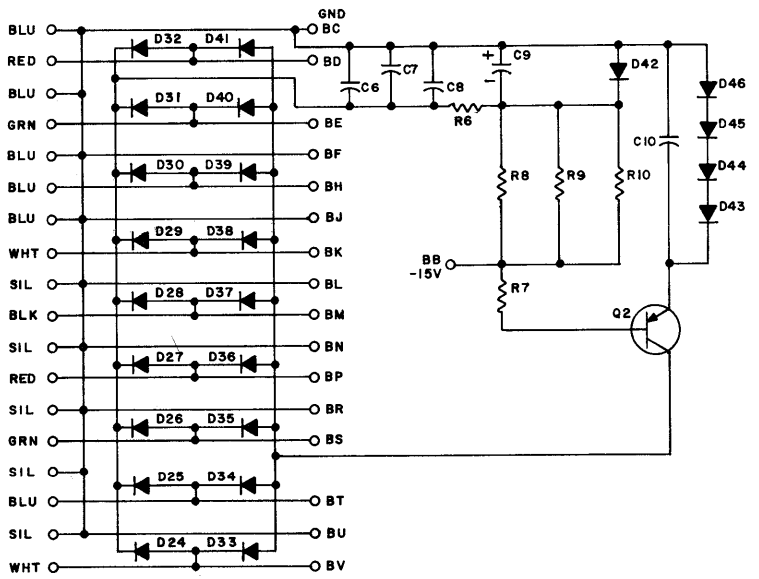
SIZE B CODE CS NUMBER W681-0-1 REV. H
A +10V (A)
N POSITIVE
C GND
R NEGATIVE
B -15V
K
J
L
M
P
F
D
E
H
R1 15,000
R2 15,000
R3 15,000
R4 68,000 10%
R5 3,000
R6 1,500
R7 7,500
R8 3,000
R9 1,500
R10 3,000
R11 3,000
R12 1,500
R13 7,500
R14 1,500
R15 3,000
R16 3,000
R17 3,000
R18 2,200
R19 3,000
R20 1,500
R21 1,500
R22 1,500
C1 56 MMFD
C2 56 MMFD
D1 D2 D3 D4 D5 D6 D7 D-662
D8 D9 D10 D11 D12 D-670 D13 D-670 D14 D-670
D15 D662
D16 D-670
D17
D18 D-670
D19 D-670
D20 D-662
D21 D-662
D22 D-662
D23 D-662
Q1
Q2
Q3 DEC 3646-B
Q4 DEC999
Q5 DEC3646-B
Q6 DEC999
Q7
UNLESS OTHERWISE INDICATED:
DIODES ARE D-664
TRANSISTORS ARE DEC3639-B
RESISTORS ARE 1/4 W, 5%
PARTS LIST A-PL-W681-0-0
REVISIONS
CHK CHG NO REV
DAM 5370 2
REV. & REDR. 5441 C
5566 D
5652 E
5829 F
7110 H
DRN. I. HAHN DATE 4-16-65
CHK'D R. SILVERMAN DATE 4-21-65
ENG. R. SOGGE DATE 4-20-65
PROD. DATE
TRANSISTOR & DIODE CONVERSION CHART
DEC EIA
DEC3639-B 2N3639-B
DEC999 MM999
DEC3646-B NONE
D662 IN645
D664 IN3606
DEC EIA
D670 IN3653
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
TITLE SCOPE INTENSIFIER W681
SIZE B CODE CS NUMBER W681-0-1 REV. H
PRINTED CIRCUIT REV. A
DEC FORM NO. DRB 102





REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-W851-0-0
Q1,Q2	TRANSISTOR DEC3638B OR DEC6534D	1502979 1503409-00
R1-R4,R7-R10	RES. 1.5K 1/4W 5% CC	1300391
R5,R6	RES. 22 1/4W 5% CC	1301969
D6-D41	DIODE D664	1100114
D1-D5,D42-D46	DIODE D662	1100113
C2,C9	CAP. 3.9MFD 10V 20% S.TANT	1000064
C1,C3-C8,C10	CAP. .01MFD 100V 20% DISC	1001610

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC6534D	MPS6534		
DEC3638B	2N3638		
D662	IN645		
D664	IN3606		

REVISIONS			
CHK	CHG NO.	REV	
	6914	B	C
	00001		

DRN. M. Waller DATE 7-25-67
CHK'D DATE 7/27/67
ENG. DATE 8-7-67
PROD. 1 DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

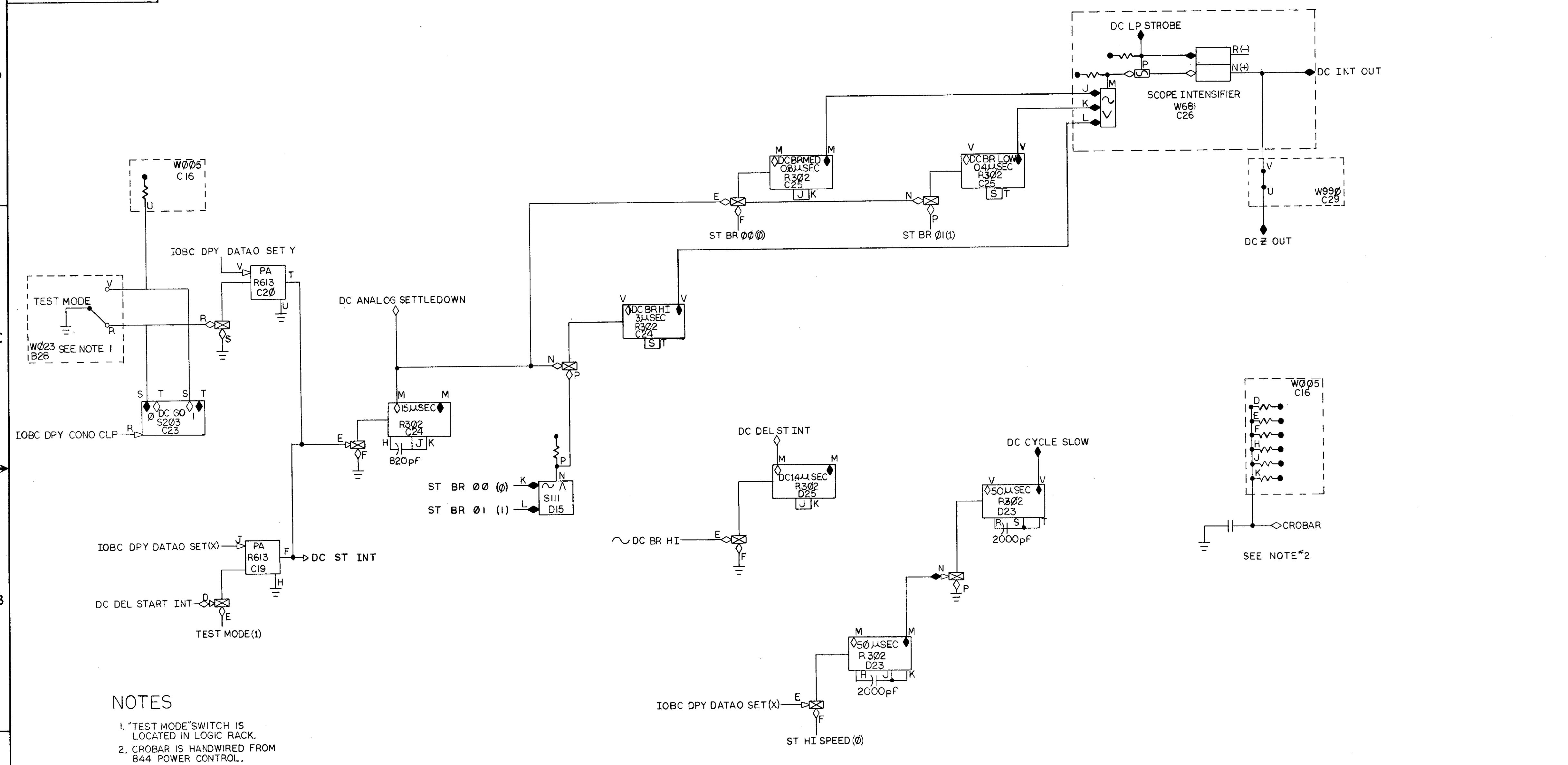
TITLE PDP-10 BUS CONNECTOR BOARD W851

SIZE	CODE	NUMBER	REV.
C	CS	W851-0-1	C

PRINTED CIRCUIT REV. D

SIZE C CODE CS NUMBER W851-0-1 REV. C

DEC FORM NO. DRC 102



NOTES

1. "TEST MODE" SWITCH IS LOCATED IN LOGIC RACK.
2. CROBAR IS HANDWIRED FROM 844 POWER CONTROL.

FIRST USED ON OPTION/MODEL: VP1Ø-Ø

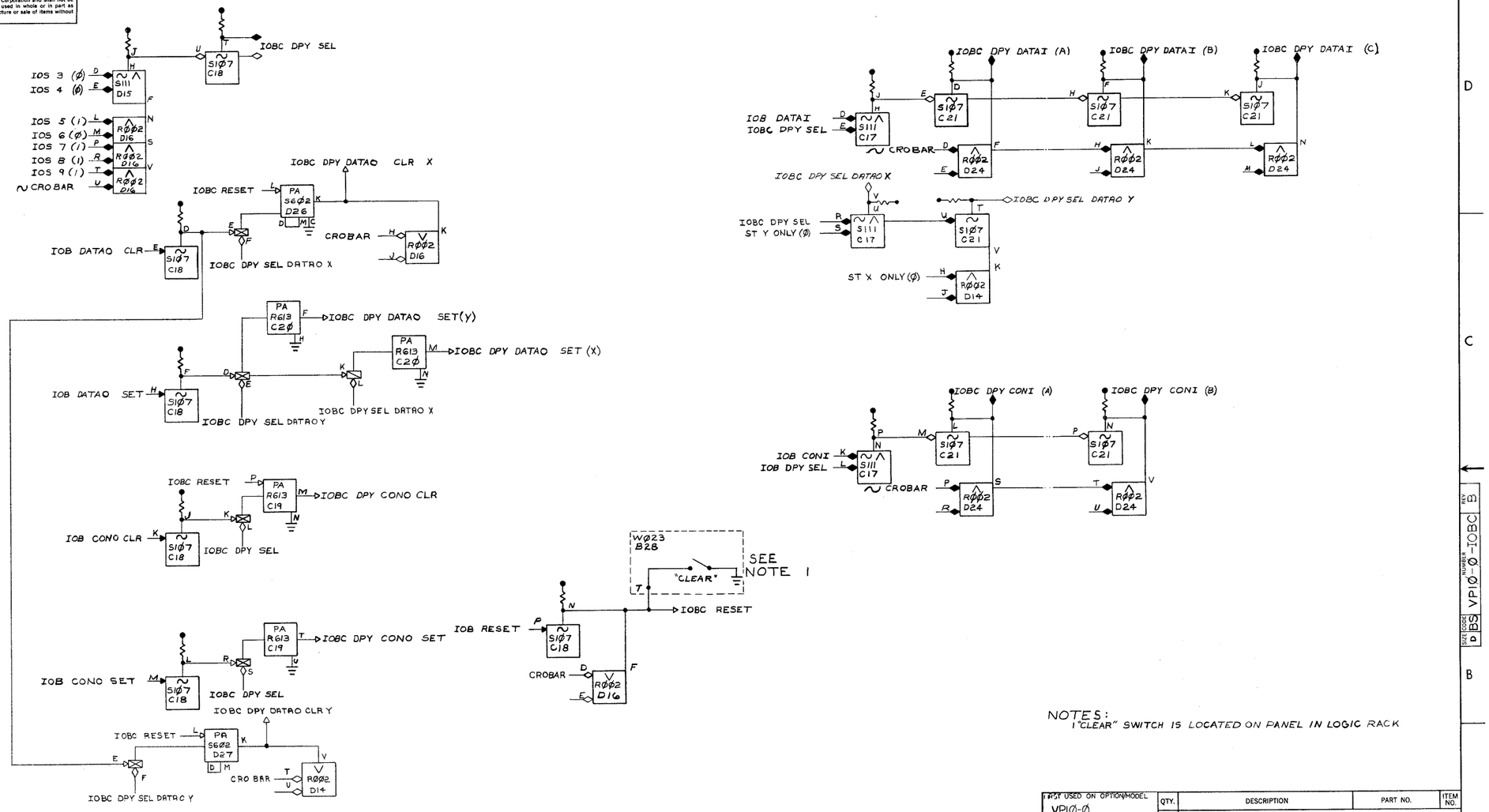
DIGITAL EQUIPMENT CORPORATION, MAYNARD, MASSACHUSETTS

TITLE: DISPLAY CONTROL DC

NEXT HIGHER ASSY: A-ML-VP1Ø-Ø

SIZE D CODE BS NUMBER VP1Ø-Ø-DC REV. A

SCALE — SHEET 1 OF 1



NOTES:
1 "CLEAR" SWITCH IS LOCATED ON PANEL IN LOGIC RACK

REVISIONS			
CHK	CHANGE NO.	REV.	
[illegible]	[illegible]	A	
[illegible]	[illegible]	B	

DEC FORM NO. DRD 102A

NEXT USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
VPIØ-Ø		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS .005 ± 1/64 FRACTIONS ± 0°30' ANGLES
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN	[illegible]	DATE 11/7/68
CHK'D	[illegible]	DATE 3/5/69
ENG	[illegible]	DATE 3/14/69
PROJ ENG		DATE
PROD	[illegible]	DATE 3/14/69

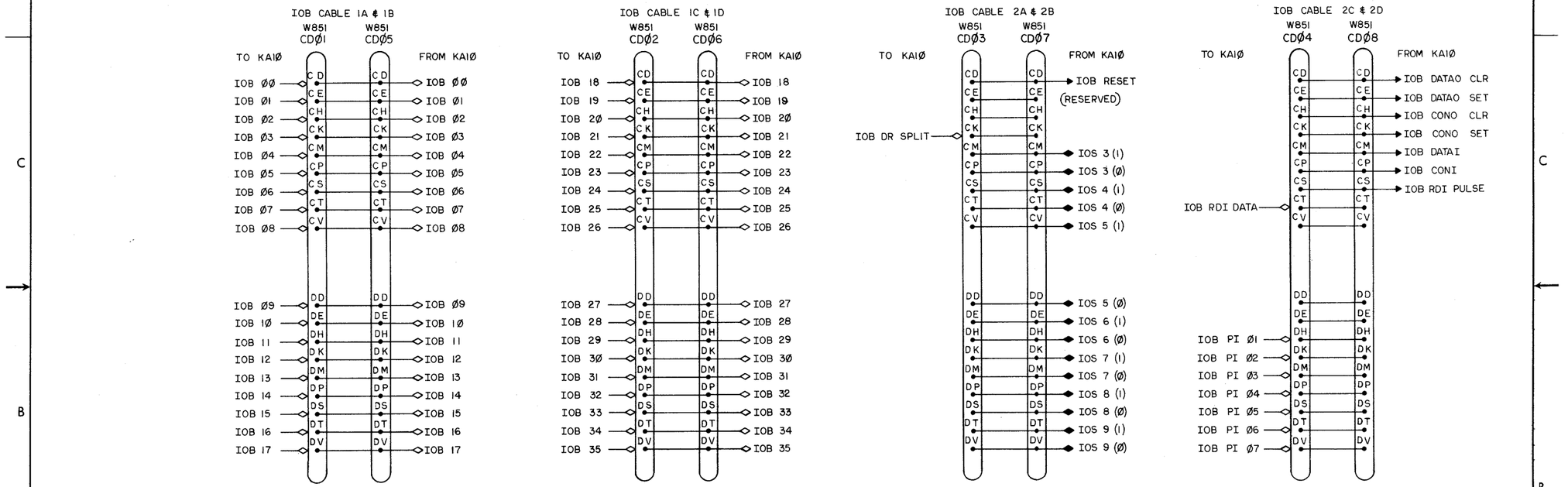
NEXT HIGHER ASSY A-ML-VPIØ-Ø
SCALE
SHEET OF

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE I/O BUS CONTROL LOGIC

SIZE D CODE BS NUMBER VPIØ-Ø-IOBC REV E
DIST.

SIZE D CODE BS NUMBER VPIØ-Ø-IOBC REV B



NOTES:

1. PINS C,F,J,L,N,R,U ARE GROUNDED.
2. CABLE SETS (1A-D, 2A-D) MUST BE LOCATED ON SINGLE FLIP CHIP BLOCKS.

FIRST USED ON OPTION/MODEL: VPIØ-Ø	QTY.	DESCRIPTION	PART NO. / ITEM NO.
		PARTS LIST	

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN		DATE 9/12/68
CHK'D		DATE 2/5/69
ENGR		DATE 2/11/69
PROJ ENGR		DATE 2/11/69
PROD ENGR		DATE 2/27/69

NEXT HIGHER ASSY: A-ML-VPIØ-Ø

SCALE —

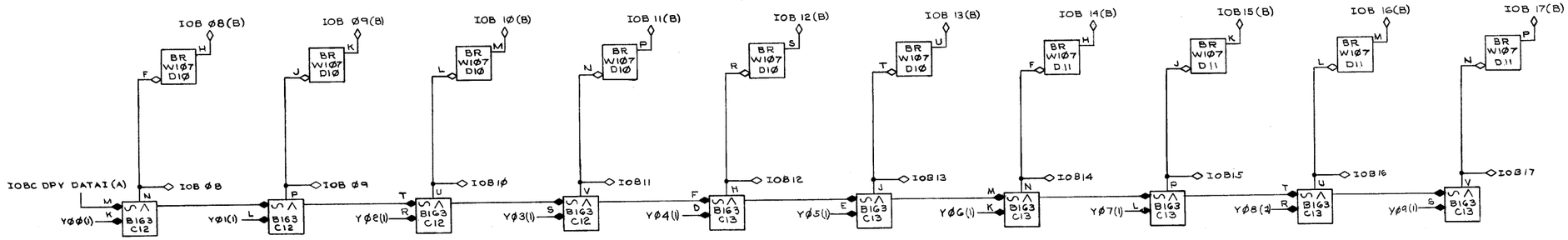
SHEET 1 OF 1

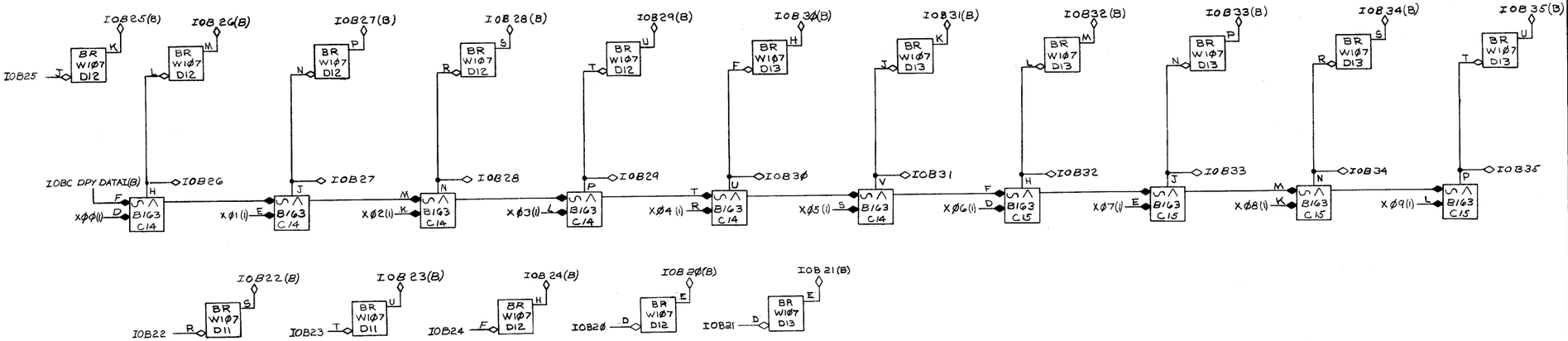
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: I/O BUS INTERFACE IOBI

SIZE	CODE	NUMBER	REV.
D	IC	VPIØ-Ø-IOBI	

DIST.





REVISIONS			
CHK	CHANGE NO.	REV.	
	VPIØ 00006	A	
	D.SPOSS		

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
VPIØ-Ø		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 | FRACTIONS ± 1/64 | ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. Paul LaBlanc	DATE	11/16/68
CHK'D.	DATE	3/14/69
ENG.	DATE	3/19/69
PROJ. ENG.	DATE	3/19/69
PROD.	DATE	3/19/69
NEXT HIGHER ASSY		
A-ML-VPIØ-Ø		
SCALE NONE		
SHEET 1 OF 1		

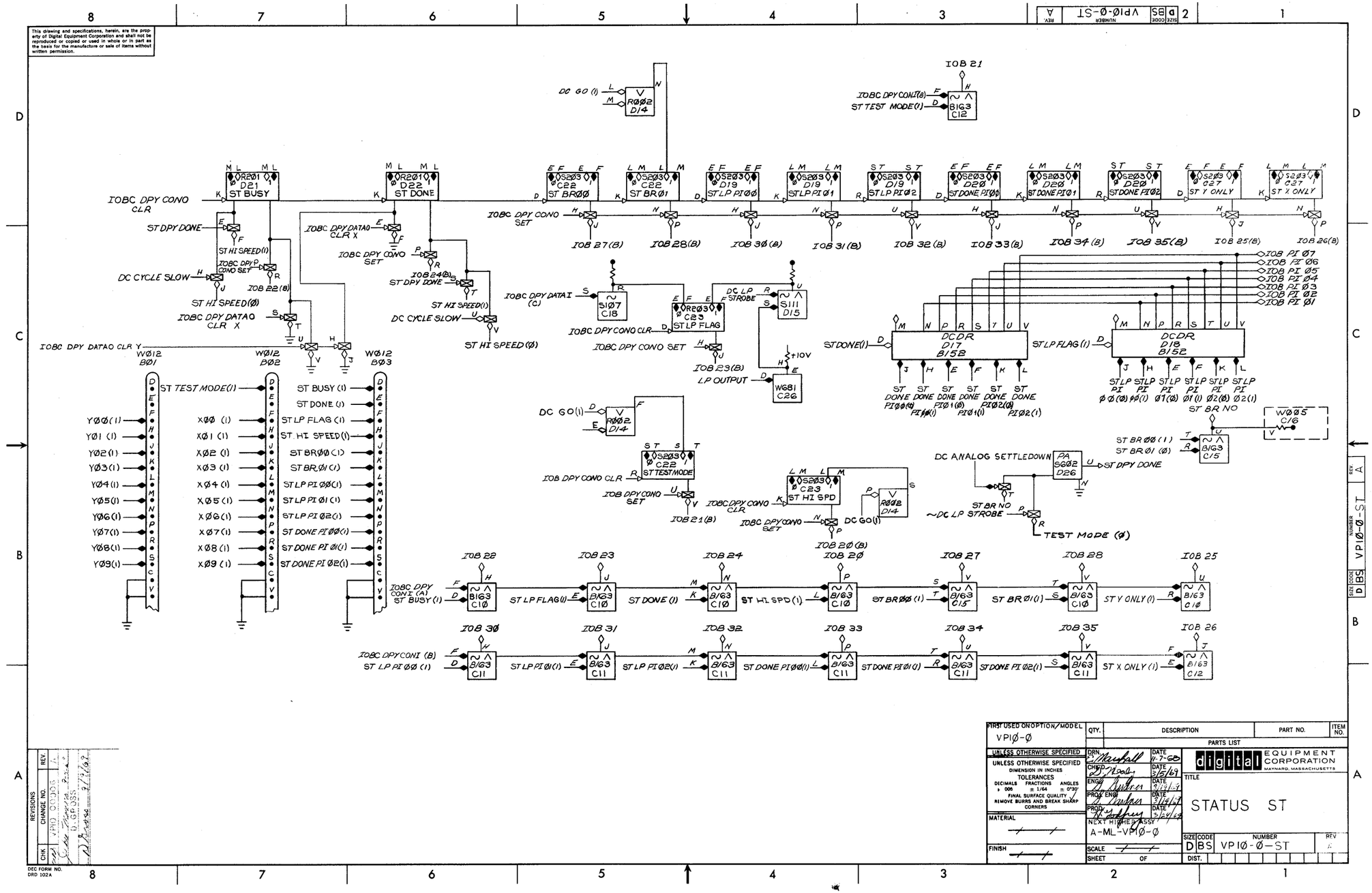
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE
I/O BUS INTERFACE
IOB

SIZE	CODE	NUMBER	REV.
D	BS	VPIØ-Ø-IO B	A

DIST.

DEC FORM NO. DRD 102A



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
VPIØ-Ø		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN	D. Marshall	DATE 11-7-68
CHKD	D. Neale	DATE 3/5/69
ENGR	[illegible]	DATE 9/11/-1
PROJ ENGR	[illegible]	DATE 3/26/-1
PROJ	[illegible]	DATE 3/26/68

NEXT HIGHER ASSY
A-ML-VPIØ-Ø

SCALE —

SHEET OF

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

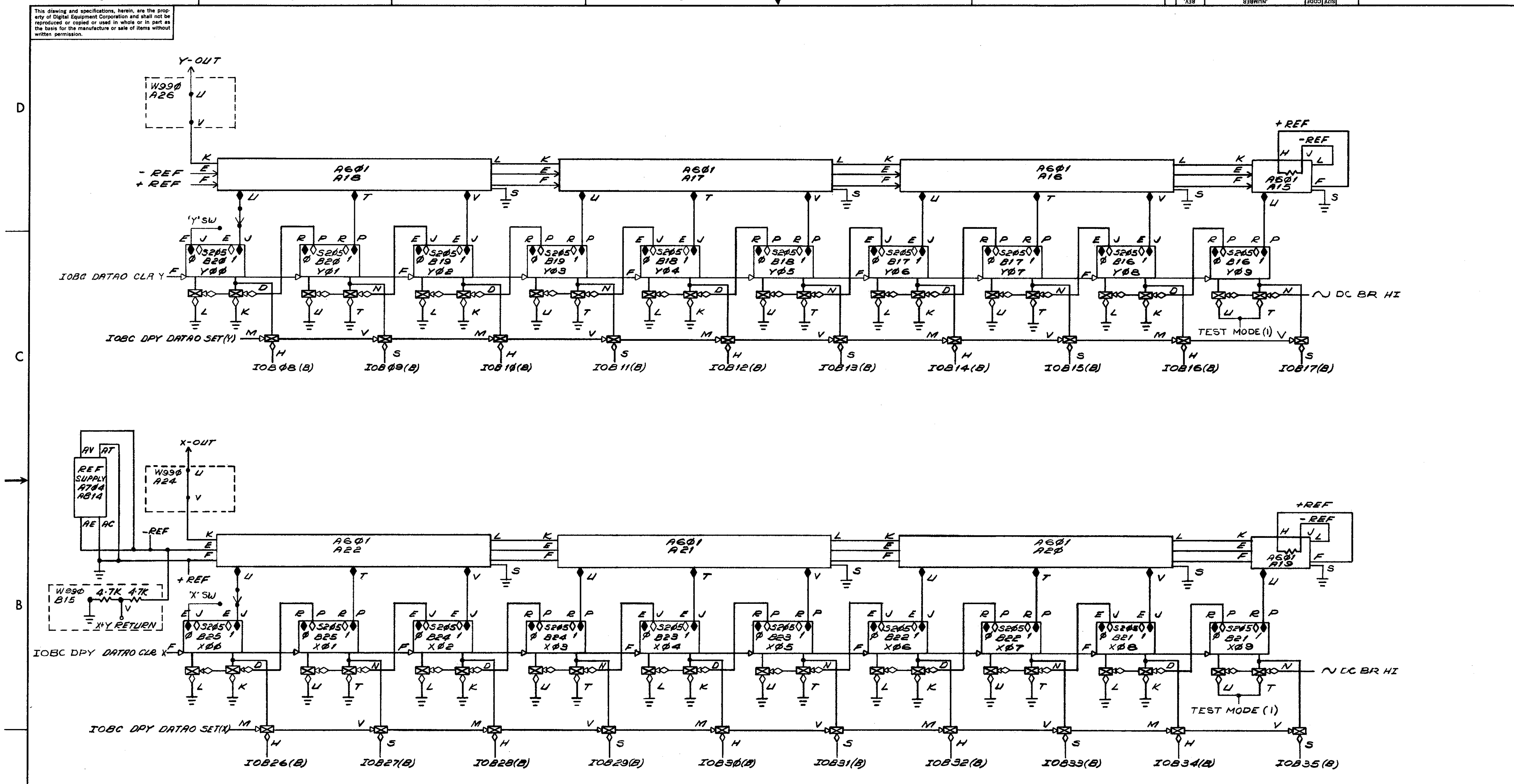
TITLE
STATUS ST

SIZE	CODE	NUMBER	REV
D	BS	VPIØ-Ø-ST	A

DIST.

REVISIONS	REV.	CHK	CHANGE NO.
	A	[illegible]	VPID 01005

DEC FORM NO. DRD 102A



CHK	REVISIONS CHANGE NO.	REV.
	VP1Ø-ØØØ4 G. GARDNER 8/12/69	A
	VP1Ø ØØØØ6 D. GROSS 9/9/69	B

FIRST USED ON OPTION/MOD: VP1Ø-Ø

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —
FINISH —

		DATE
DRN		11-6-68
CHK'D		3/5/69
ENG		3/4/69
PROJ. ENG		3/4/69
PROD.		3/4/69

NEXT HIGHER ASSY. A-ML-VP1Ø-Ø
SCALE — SHEET 1 OF 1

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE X-Y BUFFERS XYB

SIZE D CODE BS NUMBER VP1Ø-Ø-XYB REV E

DEC FORM NO. DRD 102A

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY G. FLANDERS	CHECKED D. HEALY	SECTION
DATE 11/11/68	DATE 2/21/69	1
ENG D. Flanders	PROD H. Hudgins	ISSUED SECT.
DATE 3/3/69	DATE 3/24/69	1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION VP1Ø 60HZ	VP1Ø 50HZ
23	D-MA-728-0-1	728 POWER SUPPLY	1	
24	D-MA-728A-Ø-1	728A POWER SUPPLY		1
25	D-AD-7005358-2-0	DOOR FULL ASSY	1	1
26	9007620	BOLT SQ HD 3/8 - 16 x 9-½ SST	2	2
27	9007858	WASHER 11/16 O.D. x 3/8 I.D. x 1/16 THK SST	2	2
28	9006593	NUT HEX 3/8-16 SST	2	2
29	9007074	CLAMP CAB-L-TITE #261-100 DAKOTA	7	7
30	9006075-1	SCR PH PAN HD 10-32 c 3/4 LG SST	7	7
31	B-MD-7406047-0-0	BLOCK RETAINER	2	2
32	9007799	SCR PH HD FIL #8-32 x 1½ LG SST	4	4
33	D-AD-BC1ØA-Ø-Ø	BC1ØA CABLE ASSY (LGTH PER ENG.)	2	2
34	B-IA-BC1ØB-Ø-Ø	MARGINAL CHK CABLE (LGTH PER ENG.)	1	1
35	D-IA-7005459-12-0	WØ12 TO W25Ø CABLE	3	3
36	A-DC-7406255-0-0	DECAL	1	1
37	B-5111	CHASSIS "C" SIZE #7402035	2	2
38	9007238	TAB, SOLDER #7-202-5 HEYMAN MFG.	2	2
39	9007633	BUSHING, TERM (BRN) #DC-202-2 HEXMAN MFG	1	1
40	9006346	SCR SOC HD CAP 10-32 x ½ SST	2	2
41	9006083-1	SCR, PH HD PAN 10-32 x 2-½ LG SST	2	2
42	9006074-3	SCR PHL HD TRUSS #10-32 x 5/8 SST	72	72
43	A-DC-7407035-0-0	DECAL VP10	1	1
44	D-AD-7005501-0-0	TRANSFORMER PANEL ASSY		1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
POINT PLOT DISPLAY INTERFACE VP1Ø	D-UA-VP1Ø-Ø-Ø	A	PL	VP1Ø-Ø-Ø		
	SHEET 2 OF 3	DIST.				

DEC FORM NO.
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY G. FLANDERS	CHECKED D. HELAY	SECTION
DATE 11/11/68	DATE 2/20/69	1
ENG D. Flanders	PROD H. Hudgins	ISSUED SECT.
DATE 3/3/69	DATE 3/24/69	1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION VP1Ø-Ø 60HZ	VP1Ø-A 50HZ
1	E-IA-7406052-0-0	CABINET FRAME REWORK	1	1
2	D-AD-7006078-0-0	BEZEL ASSY	1	1
3	E-AD-7005474-0-0	FAN HOUSING ASSY	1	1
4	B-MD-5100	PANEL BLANK #7402016	8	8
5	D-SC-3405331-0-0	COVER	6	6
6	C-IA-7405570-2-0	COVER RETAINER	12	12
7	D-AD-7005492-2-0	DOOR, FRONT ASSY	1	1
8	B-MD-7405861-0-0	BRACKET, DOOR PIVOT	1	1
9	A-MD-7405860-0-0	BAR, SPACER	1	1
10	9006350	SCR, SOC HD CAP #10-32 x 1" LG SST	6	6
11	9006635	WASHER LOCK EXT TOOTH #10	74	74
12	B-MD-7406049-2-0	PLATE, STRIKER	1	1
13	B-MD-5111	CHASSIS "D" SIZE #7402036	2	2
14	B-MD-5111	CHASSIS "E" SIZE #7402037	1	1
15	B-MD-5111	CHASSIS "A" SIZE #7402033	1	1
16	D-MD-7405862-0-0	TRIM STRIP BOTTOM	1	1
17	9006074-3	SCR PH HD TRUSS #10-32 x ½ LG SST	2	2
18	D-AD-7005467-0-0	BRACKET, POWER CONN ASSY	1	1
19	C-AD-7006210-0-0	LOGIC ASSY VP1Ø	1	1
20	1201265	117V TURN ON 9'	2	2
21	7005427	MALE TO FEMALE TW. LOCK 25'	1	1
22	D-UA-844-0-0	844 POWER CONTROL	1	1

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
POINT PLOT DISPLAY INTERFACE (VP1Ø)	D-UA-VP1Ø-Ø-Ø	A	PL	VP1Ø-Ø-Ø		
	SHEET 1 OF 3	DIST.				

DEC FORM NO.
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY G. FLANDERS	CHECKED D. HEALY	SECTION 1
DATE 11/11/68	DATE 2/21/69	
ENG D. Healy	PROD H. Sundgren	ISSUED SECT. 1
DATE 3/13/69	DATE 3/24/69	

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION VP1Ø-Ø 60HZ	VP1Ø-A 50HZ
45	B-AD-7006214-0-0	SCOPE CABLE (OPTION)	4	4
46	E-IA-7405092-0-0	END PANEL	2	2

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
POINT PLOT DISPLAY INTERFACE VP1Ø	D-UA-VP1Ø-Ø-Ø	A	PL	VP1Ø-Ø-Ø		
	SHEET 3 OF 3	DIST.	G			

DEC FORM NO.
DRA 110

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
USAGE														A7Ø4	A6Ø1	A6Ø1	A6Ø1	A6Ø1	A6Ø1	A6Ø1	A6Ø1	A6Ø1	A6Ø1		W99Ø		W99Ø																		
A														REF SUP	Y Ø9	Y Ø6 TO Y Ø8	Y Ø3 TO Y Ø5	Y Ø0 TO Y Ø2	X Ø9	X Ø6 TO X Ø8	X Ø3 TO X Ø5	X Ø0 TO X Ø2		X- OUT		Y- OUT																		
	W Ø12	W Ø12	W Ø12												W99Ø	S2Ø5	S2Ø5	S2Ø5	S2Ø5	S2Ø5	S2Ø5	S2Ø5	S2Ø5	S2Ø5	S2Ø5			W22Ø																		
USAGE	CABLE	CABLE	CABLE																																								
B	Y Ø0 (I) TO Y Ø9 (I)	ST TEST MODE (I) X Ø0 TO X Ø9 (I)	ST BUSY (I) TO ST DONE P1 Ø2 (I)												X-Y RETURN	Y Ø9	Y Ø6	Y Ø4	Y Ø2	Y Ø0	X Ø9	X Ø6	X Ø4	X Ø2	X Ø0		R T V																		
																Y Ø9	Y Ø7	Y Ø5	Y Ø3	Y Ø1	X Ø9	X Ø7	X Ø5	X Ø3	X Ø1																				

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44
USAGE	W851 CABLE	W851 CABLE	W851 CABLE	W851 CABLE	W851 CABLE	W851 CABLE	W851 CABLE	W851 CABLE		B163	B163	B163	B163	B163	B163	W Ø5	S111	S1Ø7	R613	R613	S1Ø7	S2Ø3	S2Ø3	R3Ø2	R3Ø2	W631	S6Ø3		W99Ø																
C	IOB Ø0 TO IOB Ø6	IOB 18 TO IOB 26	IOB RESET DR SPLIT IOS 3(I) IOS3(Ø) IOS4(I) IOS4(Ø) IOS5(I)	DATO CLR DATAO SET CONO CLR CONO SET DATAI CONTI RDI PULSE RDI DATA	IOB Ø0 TO IOB Ø6	IOB 18 TO IOB 26	IOB RESET	DATO CLR DATO SET CONO CLR CONO SET DATI CONTI RDI PULSE RDI DATA		IOB 22	IOB 3Ø	IOB 21	IOB 12	IOB 26	IOB 32		IOBC DPY DATAI(A)			IOBC DPY DATAO SET (A)	IOBC DPY DATAI(A) IOBC DPY DATAI(B) IOBC DPY DATAI(C) IOBC DPY CONI(A) IOBC DPY CONI(B) IOBC DPY SEL DATAO Y	ST BR Ø0 ST BR Ø1 ST TEST MODE	ST LP FLAG ST HI SPD DC GO	DC ANALOG SETTLE-DOWN INT OUT DC LIGHT PEN STROBS	INT OUT INT OUT	INT OUT INT OUT	ST Y ONLY ST X ONLY		DC Z OUT																
										IOB 23	IOB 31	IOB 26	IOB 13	IOB 27	IOB 33			IOB DATO CLR IOB DATO SET IOB CONO CLR IOB CONO SET IOBC RESET IOBC DPY DATAI(C) IOBC DPY SEL																														
										IOB 24	IOB 32	IOB Ø8	IOB 14	IOB 28	IOB 34				IOBC DPY CONO CLR	IOBC DPY DATAO SET (B)																												
										IOB 2Ø	IOB 33	IOB Ø9	IOB 15	IOB 29	IOB 35		IOBC DPY SEL																														
										IOB 25	IOB 34	IOB 1Ø	IOB 16	IOB 3Ø	ST BR LOW				IOBC DPY CONO SET	DC ST INT																										
										IOB 28	IOB 35	IOB 11	IOB 17	IOB 31	IOB 27		DATAO X																														
	W1Ø7	W1Ø7	W1Ø7	W1Ø7										R Ø02	S111	R Ø02	B152	B152	S2Ø3	S2Ø3	R2Ø1	R2Ø1	R3Ø2	R Ø02	R3Ø2	S6Ø2	S6Ø2																		
D				IOB 20 (B)	IOB 21 (B)	DC GO (I) ST X ONLY (Ø) DC GO (I) TEST SW CRO BAR									IOBC DPY SEL INT OUT DC LP STROBE	IOBC RESET IOBC DPY DATAO CLR IOBC DPY SEL	IOB PI Ø1 TO IOB PI Ø7	IOB PI Ø1 TO IOB PI Ø7	ST LP PI Ø0 ST LP PI Ø1 ST LP PI Ø2	ST DONE PI Ø0 ST DONE PI Ø1 ST DONE PI Ø2	ST BUSY	ST DONE	DC CYCLE SLOW DC CYCLE SLOW	IOBC DPY DATAI(A) IOBC DPY DATAI(B) IOBC DPY DATAI(C) IOBC DPY CONI(A) IOBC DPY CONI(B)	DC DELAY ST INT ST DPY DONE	IOBC DPY DATAO CLR X	IOBC DPY DATAO CLR Y																		
	IOB Ø8(B)	IOB 14(B)	IOB 24(B)	IOB 3Ø(B)																																								
	IOB Ø9(B)	IOB 15(B)	IOB 25(B)	IOB 31(B)																																								
	IOB 1Ø(B)	IOB 16(B)	IOB 26(B)	IOB 32(B)																																								
	IOB 11(B)	IOB 17(B)	IOB 27(B)	IOB 33(B)																																								
	IOB 12(B)	IOB 22(B)	IOB 28(B)	IOB 34(B)																																								
	IOB 13(B)	IOB 23(B)	IOB 29(B)	IOB 35(B)																																								

NOTE
1. CABLES IN RACK BØ1, BØ2 & BØ3 ARE WØ12 TO W25Ø #D-IA-7005459-12-D
2. CABLES IN RACK CDØ1 THRU CDØ4 CDØ5 THRU CDØ8 ARE BC1ØA #D-AD-BC1ØA-Ø-Ø

REVISIONS	REV	CHANGE NO.	CHK
	A	VP10 0000	

UNLESS OTHERWISE SPECIFIED	DRN.	DATE
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS FRACTIONS ANGLES .XXX ± 1/64 ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	CHK'D.	DATE 3/5/69
	ENG.	DATE 3/14/69
	PROJ. ENG.	DATE 3/14/69
	PROD.	DATE 3/24/69
MATERIAL	NEXT HIGHER ASSY. A-ML-VP10-Ø	
FINISH	SCALE	
FIRST USED ON OPTION/MODEL VP10-Ø	SHEET 1 OF 1	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MODULE UTILIZATION

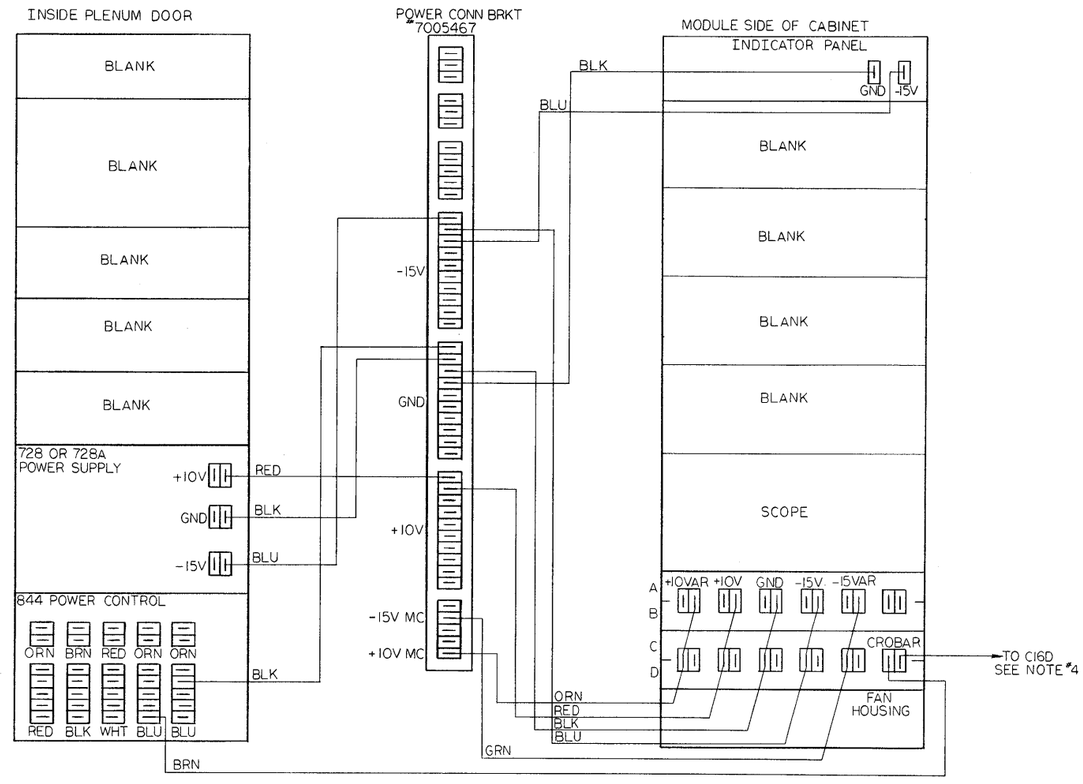
SIZE	CODE	NUMBER	REV.
D	MU	VP10-Ø-2	A

DIST.

DEC FORM NO. DRD 105

NOTES:

1. ALL WIRING TO BE #14 AWG STRANDED TEFLON UNLESS OTHERWISE SPECIFIED.
2. ALL AC WIRING TO BE #14 AWG RED/WHT TWISTED PAIRS.
3. HERTZ (HZ)=CYCLES PER SECOND.
4. CROBAR WIRE (TO C16D) IS HAND WIRED.



50 & 60 Hz DC WIRING

FIRST USED ON OPTION / MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
VPIØ-Ø		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN.	DATE	11/11/68
CHKD.	DATE	3/6/69
ENG.	DATE	3/7/69
PROJ. ENG.	DATE	3/10/69
PROD.	DATE	3/14/69

NEXT HIGHER ASSY
D-UA-VPIØ-Ø-Ø

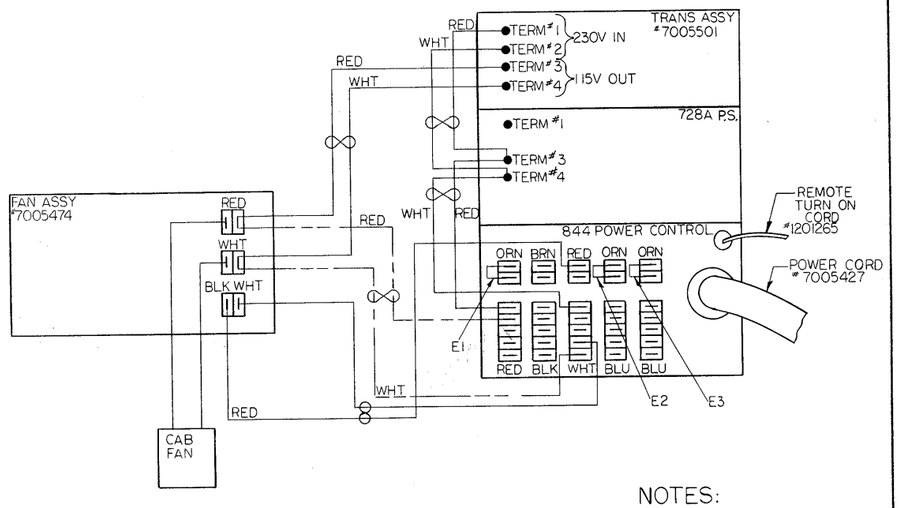
digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
WIRING, POWER
VPIØ

SIZE	CODE	NUMBER	REV.
D	IC	VPIØ-Ø-4	

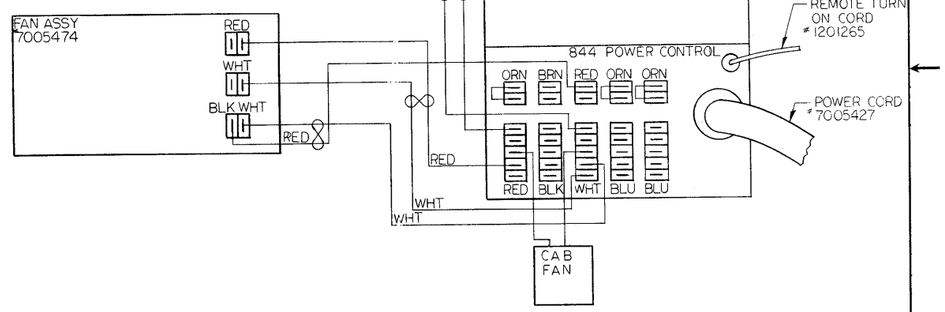
SCALE
SHEET 1 OF 2
DIST.

728A JUMPING			
INPUT VOLTAGE	JUMPER	LINE	
195V	1-5	3,4	
220V	1-6	3,4	
235V	2-8	3,4	
112.5V	2-4,3-7	3,4	
123.5	1-4,3-8	3,4	



NOTES:
1. JUMPERS E1,E2,E3 REMOVED FOR 230V OPERATION.
2. WIRING SHOWN IN PHANTON FOR 115V OPERATION ONLY.

115V OR 230V 50 Hz AC WIRING



115V 60 Hz AC WIRING

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN. [illegible] DATE 11/14/68
CHK'D [illegible] DATE 3/5/69
ENG [illegible] DATE 3/13/69
PROJ ENG [illegible] DATE 3/19/69
PROD [illegible] DATE 3/24/69
FIRST USED ON

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: WIRING, POWER

SIZE D | CODE IC | NUMBER VP10-0-4 | REV.
DIST.
SCALE
SHEET 2 OF 2

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

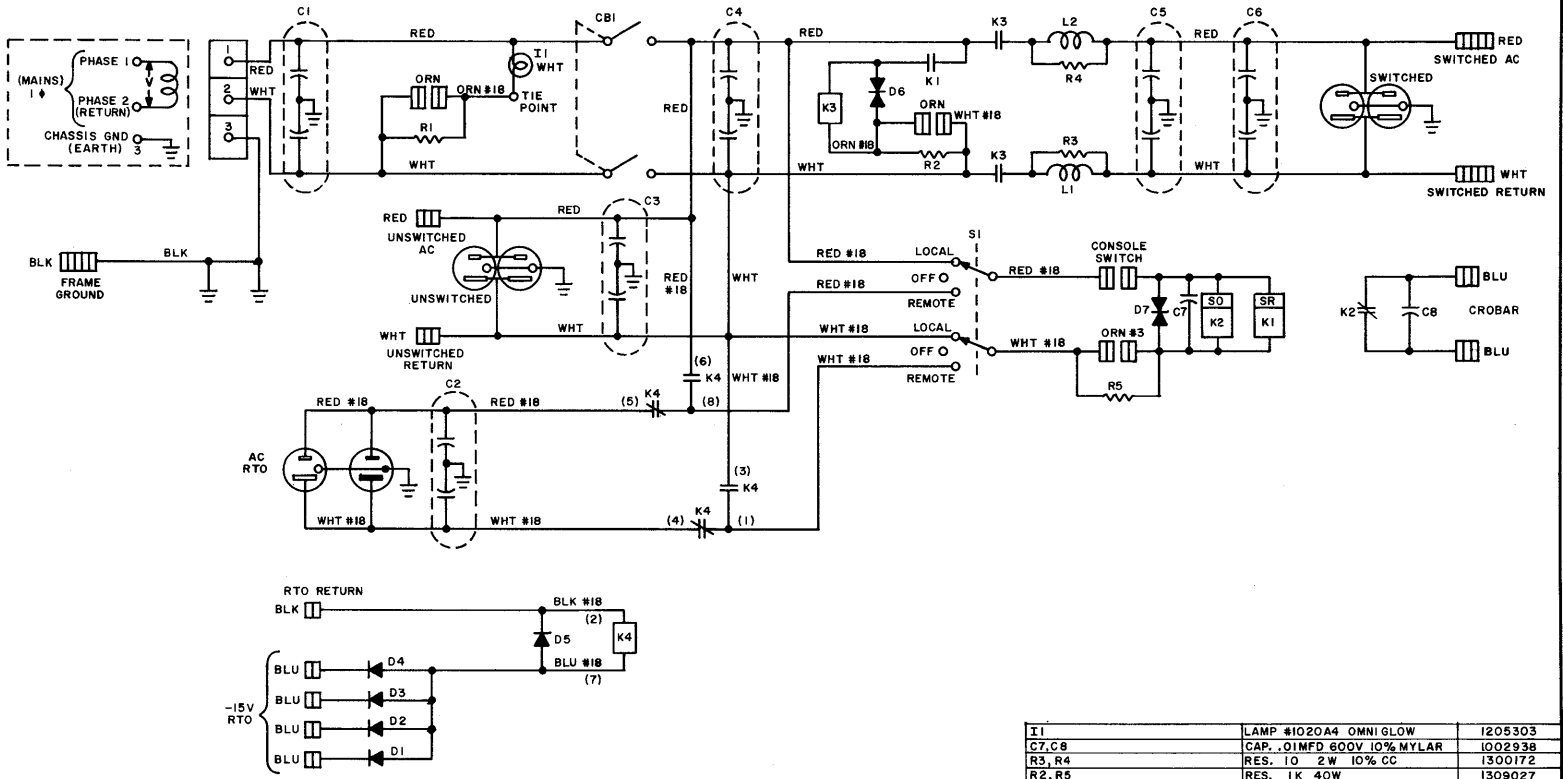
PARTS LIST

MADE BY G. FLANDERS	CHECKED D. HEALY	SECTION
DATE 11/18/68	DATE 2/19/69	1
ENG D. Flanders DATE 3/13/69	PROD H. Godfrey DATE 3/24/69	ISSUED SECT. 1

ITEM NO.	DWG NO. / PART NO.	DESCRIPTION	QUANTITY / VARIATION 7006041-0
	SEE ML	WIRE LIST	REF
1	1202188	VOLTAGE CHAIN	A/R
2	9107560-1	#22 AWG SOLID BUSSING	A/R
3	9107265	#22 INSULATION TEF WHT	A/R
4	9107470-5	#24 AWG SOLID KY NAR YEL	A/R
5	9107470-10	#24 AWG SOLID KY NAR BLU	A/R
6	D-AD-1943-D-Ø	1943D MTG PANEL ASSY	2
7	A-DC-7406371-0-0	PANEL SCOTCH CALS	A/R
8	1000027	CAPACITOR 820 MMF 100V 5%	1
9	1000004	CAPACITOR .02 MFD 50V 5%	2

TITLE	ASSY NO.	SIZE	CODE	NUMBER	REV.	ECO NO.
WIRED ASSY VP1Ø	C-AD-7006041-0-0	A	PL	7006041-0-0		
	SHEET 1 OF 1	DIST.				

DEC FORM NO.
DRA 110



NOTES:
WIRE NOT MARKED IS #14 GAUGE
WIRE IS TEFLON STRANDED
K1 IS 4 SEC QOSR 115VAC
K2 IS 4 SEC SOQR 115VAC
(2) INDICATES PIN NUMBER ON K4 SOCKET

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-844-0-0
I1	LAMP #1020A4 OMNI GLOW	1205303
C7,C8	CAP. .01MFD 600V 10% MYLAR	1002938
R3, R4	RES. 10 2W 10% CC	1300172
R2, R5	RES. 1K 40W	1309027
R1	RES. 130K 1W 5% CC	1305604
L1, L2	FERROXCUBE #56-261-30-3B	1605147
K4	RELAY KRPIIDG 12VDC	1203410
K3	RELAY EM-4 115VAC 35AMPS	1205768
K2	RELAY ADLAKE #1040-34-43	1205809
K1	RELAY ADLAKE #1040-8-687	1202184
D6, D7	THYRECTOR GE6RS20SP4B4	1100106
D1-D5	DIODE IN4001	1102942
CB1	CKT. BKR. #190-230-104 30A 250V	1201219
C1-C6	CAP. 2X.1MFD BATHTUB #CAF0001	1002153

PARTS LIST

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN4001	SAME		

REVISIONS			
CHK	CHG NO.	REV.	
RMS	6628	B	
REV.	& REDR.	C	
	6722		
	6999	D	

DRN.	M.HALLER	DATE 7-20-67
CHK'D	R.SILVERMAN	DATE 8-24-68
ENG.	R.WYMAN	DATE 8-24-68
PROD.		DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: POWER CONTROL 844

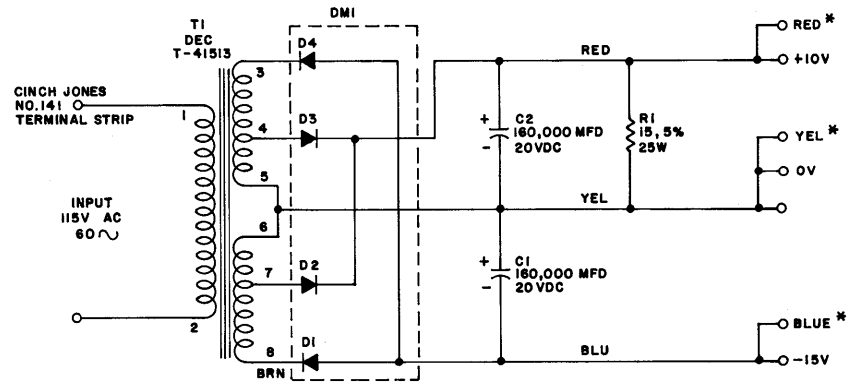
SIZE	CODE	NUMBER	REV.
C	CS	844-0-1	D

PRINTED CIRCUIT REV.

DEC FORM NO. DRC 102

SIZE	CODE	NUMBER	REV.
C	CS	844-0-1	D

SIZE	CODE	NUMBER	REV.
B	CS	728-0-1	H



NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS:

BOTH SIDES LOADED	+10V 0 TO 7.0 AMPS -15V 1.0 TO 6.0 AMPS
ONE SIDE LOADED	+10V 0 TO 7.5 AMPS -15V 1.0 TO 6.5 AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE EQUATION: $51_{10} + 61_{15} \leq 53$

* HEYMAN MFG. CO. TAB TERMINALS

REVISIONS			
CHK	CHG NO.	REV.	
DAM	4609	G	
REVISED	8051	H	

DRN.	SPAULDING	DATE 11-7-61
CHK'D	N.PERRYMAN	DATE 11-8-61
ENG.	D.WARDIMAN	DATE 11-9-61
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE: POWER SUPPLY 728

SIZE	CODE	NUMBER	REV.
B	CS	728-0-1	H

PRINTED CIRCUIT REV.

DEC FORM NO.
DRB 102

APPENDIX A
370 LIGHT PEN

A.1 INTRODUCTION

The function of the light pen (see Figure A-1) is to detect light pulses appearing on the face of a display oscilloscope. The light pulses are converted into electrical pulses by the light pen circuitry and interpreted by the computer program into coordinate locations on the face of a scope. These locations are then treated in accordance with the computer program.

The shutter for the light pen is located on the pen itself. There are six fixed apertures available, ranging from 0.300 inch to 0.050 inch. The amplitude of the output signal is adjustable; rise and fall times of the output signal are primarily dependent on the rise and decay times of the CRT phosphor.

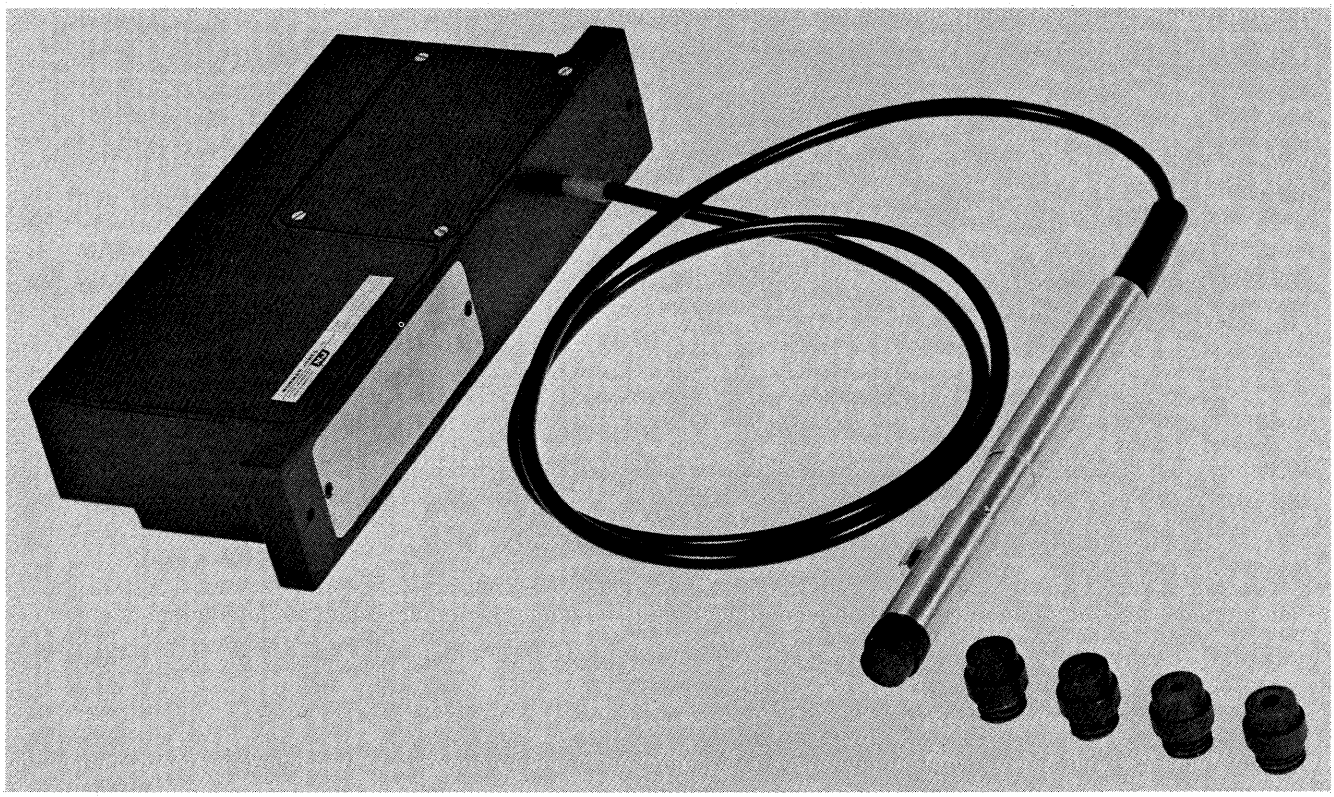


Figure A-1 Light Pen, Pipe, Power Supply, and Apertures

A.2 PHYSICAL AND ELECTRICAL SPECIFICATIONS

Light Pen

Length: 8-1/2 inches

Diameter: 5/8 inch

Light Pipe

Length: 4 feet

Power Supply

Depth: 1-3/4 inches
Height: 4-1/4 inches
Width: 8-1/4 inches

Operating Temperature

50°F to 100°F

Input Power

-15 volts at 700 milliamperes

Input Light (Minimum)

300 foot-lamberts

Spectral Response

4300 to 5600 angstroms

Output

Approximately 0 to -6 volts

(This output may be used to drive the base input of an inverter such as the one utilized in the DEC Type 4105 Module. If the phosphor is fast enough, the output may be differentiated. Use of a pulse amplifier with a differentiating input, such as the DEC Type 4604, produces a standard output pulse with other DEC Modules.

A.3 THEORY OF OPERATION

A flexible fiber optic light pipe is combined with a photomultiplier tube to detect points displayed on a cathode ray tube screen. A mechanical shutter in the form of a pen is attached to one end of the light pipe. This shutter prevents unwanted light information from entering the light pipe during pen positioning. To detect displayed points, the pen is positioned and then the shutter is depressed. Light is transmitted through the light pipe to the photo-cathode of the photomultiplier. The amplified signal from the photomultiplier is connected to an emitter follower which acts as an output buffer.

A.3.1 Light Guide

The flexible light guide is constructed of unoriented glass fibers 0.003 inch in diameter. The approximate number of fibers is 1470. The minimum radius of bend is 3/4 inch. For sharper bends, the fibers may be broken. Figure A-2 shows the relative transmission for light of different wave lengths.

A.3.2 Photomultiplier

The photomultiplier operates as follows. Light falling on the light-sensitive photocathode provides sufficient energy to liberate some of the electrons. The freed electrons are attracted towards an electrode with a potential more positive than the photocathode. Each electron striking this secondary electrode (dynode) frees more electrons which are attracted to the next more positive dynode. This

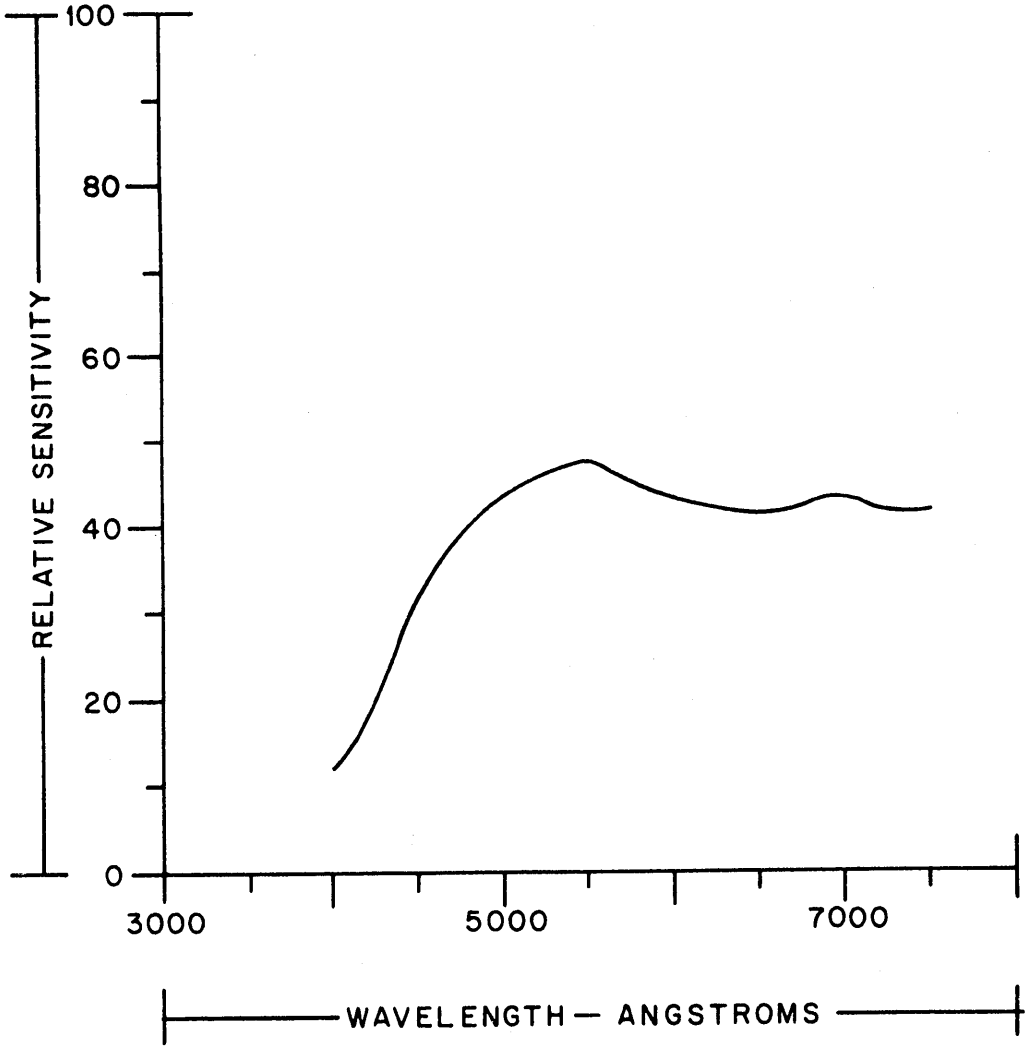


Figure A-2 Transmission Curve for Four Foot Length of Standard Light Guide

process is repeated for a number of stages. The electrons from the final stage are collected at the anode. Drawing D-370-0-2, page A-7 , illustrates the circuitry of the photomultiplier (a 931A tube with an S-4 spectral response). Figure A-3 shows the spectral sensitivity characteristics of a phototube exhibiting an S-4 response.

The 100,000-ohm 1-watt resistor in series with the photocathode partially limits the current through the photomultiplier and dynode resistor string.

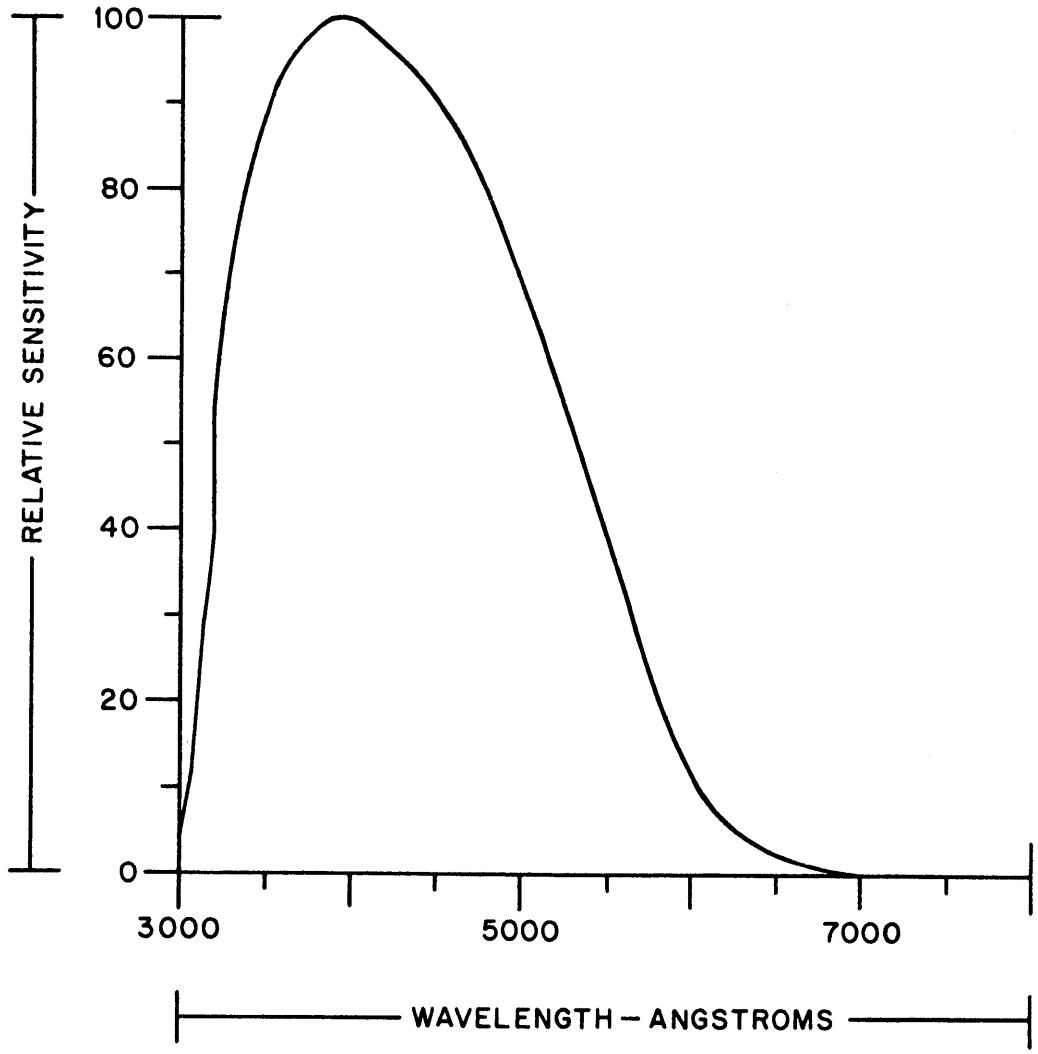


Figure A-3 Composite Spectral Sensitivity Characteristics for Phototube Having S-4 Response and a Standard Four Foot Length of Light Guide

A.3.3 Overall Spectral Response

The combination of the spectral responses of the photomultiplier and the light pipe is shown in the composite spectral response of Figure A-4. This is the response of the 370 Light Pen.

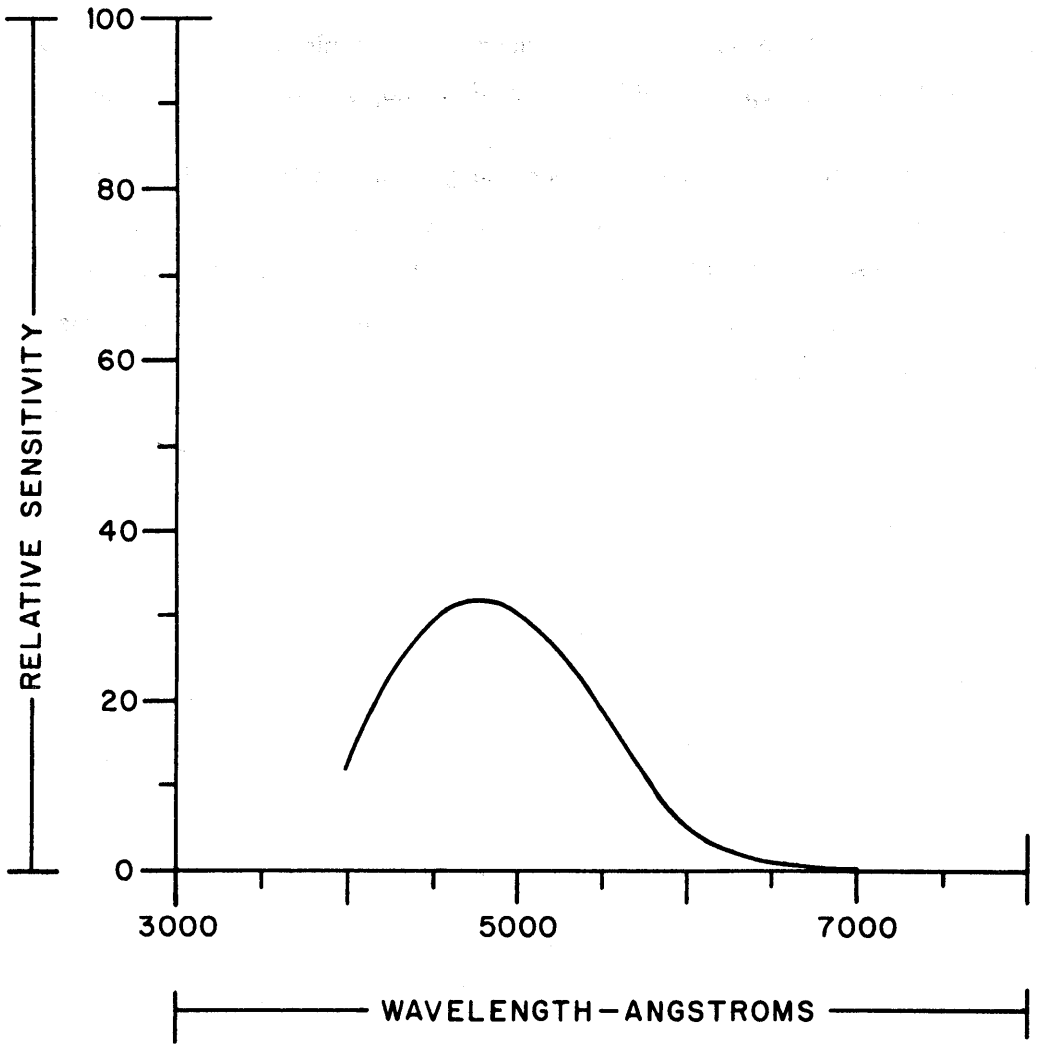


Figure A-4 Spectral Sensitivity Characteristics from Phototube Having S-4 Response

A.3.4 Output Circuitry

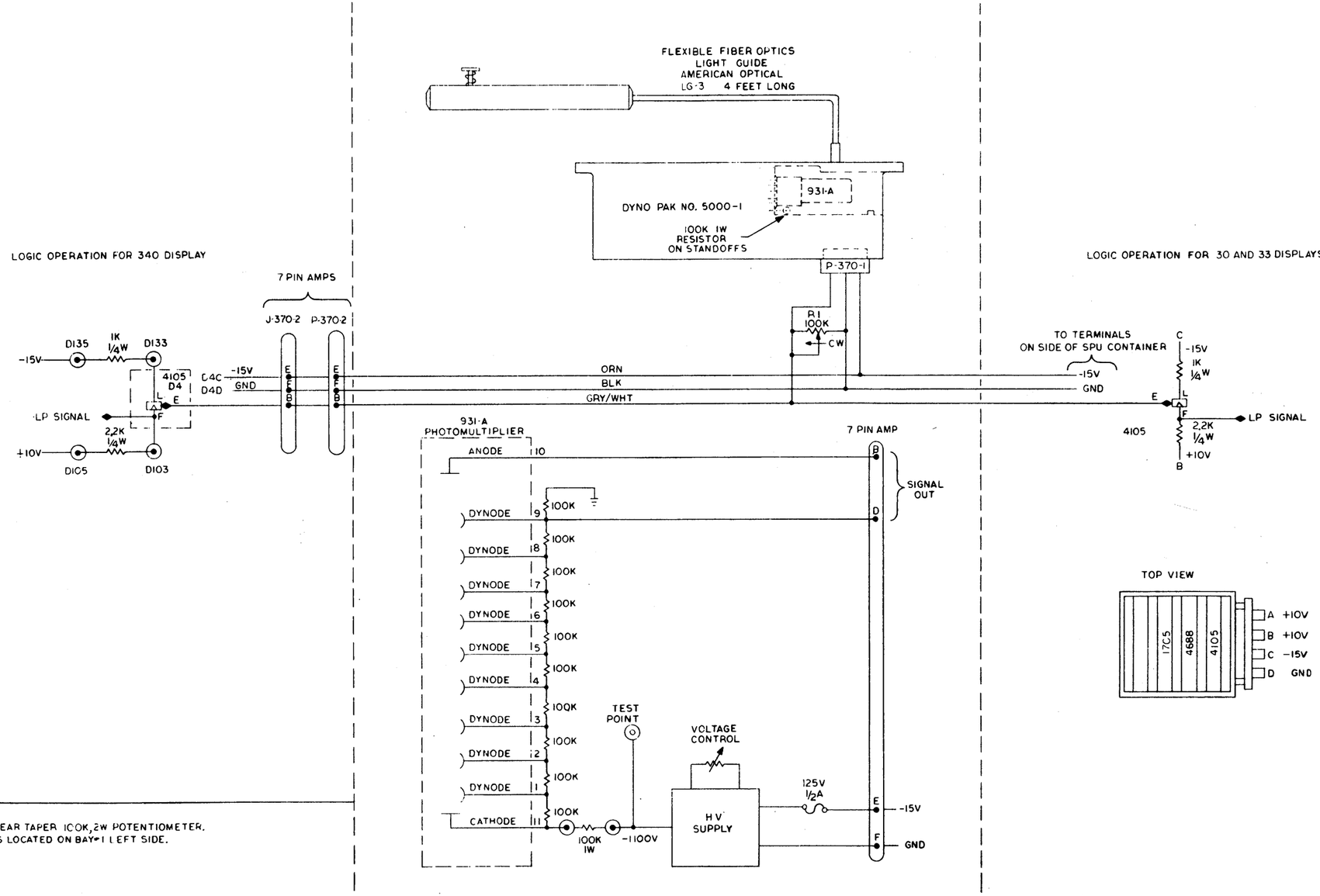
The anode of the photomultiplier is connected to one end of a potentiometer, the other end of which is grounded. The amplified current collected at the anode passes through the potentiometer to generate a voltage signal which varies in accordance with changes in load resistance. This signal is applied

to the input of an emitter follower to provide driving power and a low output impedance. Drawing D-370-0-2 shows some of the logic connections of the 370 Light Pen for operation with some of the DEC displays.

A.4 MAINTENANCE

Because of the simplicity of the light pen, maintenance is at a minimum. In addition to visual inspection, the high voltage power supply should be checked and adjusted as described below:

To measure the high voltage supply, unscrew the red slug located at the top of the supply. This provides access to the voltage test point. The voltage may be varied by means of the screwdriver slot adjustment. The voltage should not be increased beyond -1250 volts, which is the maximum rating of the photomultiplier. If it is necessary to remove the cover of the supply, disconnect the 7-inch amphenol socket before removing the cover.



NOTES:

1. R1 IS A LINEAR TAPER 100K, 2W POTENTIOMETER.
2. P-370-2 IS LOCATED ON BAY-1 LEFT SIDE.

Figure A-5 Interconnection Wiring and Logic D-370-0-2

Digital Equipment Corporation
Maynard, Massachusetts

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