DOLPHIN CONSOLE FUNCTIONAL SPECIFICATION

COMPANY CONFIDENTIAL

REVISION HISTORY

REV	DATE	REASON
*	14 JULY 1978	ORIGINATE - S.R. HOLMES
0	5 SEPT 1978	UPDATE
1	29 SEPT 1978	DISTRIBUTION

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1.0 INTRODUCTION

1.1 GENERAL

THE DOLPHIN CONSOLE CONSISTS OF AN F-11 MICROCOMPUTER WITH 96K BYTES OF RAM MEMORY, 16K BYTES OF ROM (USED TO STORE THE F-11 BOOTSTRAP, MONITOR BOOTSTRAP, DIAGNOSTICS, AND FUNDAMENTAL CONSOLE ROUTINES), 5 SERIAL LINE INTERFACES A DECTAPE II (FOR STORAGE OF BASIC DIAGNOSTIC PROGRAMS AND SOFTWARE UPDATES), A UNIBUS, AND 2 EXTENDED HEX MODULES (CONSOLE SYSTEM INTERFACE,CSI). REMOTE ACCESS BY THE DIGITAL DIAGNOSTIC CENTER IS AVAILABLE.

THE CONSOLE SUBSYSTEM SERVES AS A TOPS20 OPERATING SYSTEM TERMINAL, AS A SYSTEM CONSOLE, AND A DIAGNOSTIC CONSOLE. WHEN THE CONSOLE IS USED AS AN OPERATING SYSTEM TERMINAL, IT IS USED BY PRIVILEGED SYSTEM USERS FOR SYSTEM OPERATIONS. AS THE SYSTEM CONSOLE IT IS USED FOR OPERATION CONTROL OF THE SYSTEM (E.G., BOOTSTRAPPING, POWER FAIL RESTART, SYSTEM INITIALIZATION, SOFTWARE UPDATES). AS A DIAGNOSTIC CONSOLE IT CAN ACCESS THE SYSTEM REGISTERS AND BUSSES, THRU A SPECIAL SYSTEM DIAGNOSTIC BUS. SYSTEM OPERATIONS ARE PERFORMED THROUGH SIMPLY KEYBOARD COMMANDS.

1.2 CONSOLE STRATEGY

A PRIMARY AND SECONDARY DOLPHIN CONSOLE STRATEGY IS NEEDED TO INSURE THE CONSOLE POWER ON SCHEDULE CAN BE MET.

THE PRIMARY STRATEGY USES THE PDT/TOBY/UNIBUS, TO PROVIDE THE KERNAL MICRO SYSTEM (ROM, RAM, SLUS, LOAD DEVICE, INTERFACE BUS, ETC.). THE INTERFACE BUS WOULD BE THE UNIBUS WHICH PROVIDES A PROVEN, WELL DEFINED BUS STRUCTURE. CONSOLE HEX MODULES WOULD BE DESIGNED AS UNIBUS OPTIONS. THIS METHOD IS FLEXIBLE AND COST EFFECTIVE.

THE SECONDARY STRATEGY STILL USES THE UNIBUS AND THE CONSOLE HEX MODULES. THE KERNAL SYSTEM WOULD CHANGE TO AN 1134A, CORE OR MOS MEMORY, ROM, SLUS, LOAD DEVICE, INTERFACE BUS, ETC., AND RETAINS UNIBUS COMPATIBILITY. THE USE OF THE SECONDARY STRATEGY WOULD BACK UP THE PRIMARY STRATEGY, IF IT WERE TO FAIL, IT WOULD ALLOW THE DOLPHIN CONSOLE POWER ON AND SUCCESIVE POWER ON'S TO BE MET ON SCHEDULE IF THE PDT/TOBY/UNIBUS WERE CANCELLED OR LATE.

TO SUMMARIZE THE CONSOLE STRATEGY:

1. THE PDT/TOBY/UNIBUS IS THE FIRST CHOICE FOR THE CONSOLE MICRO SYSTEM. IT PROVIDES A FLEXIBILE, COST EFFECTIVE CONSOLE. IF THE PDT/TOBY/UNIBUS WERE LATE OR CANCELLED, THIS STRATEGY PROVIDES A COMMON BUS INTERFACE, WHICH MANY EXISTING PDP11 PROCESSORS CAN INTERFACE TO.

2. THE 1134A WILL PROVIDE A BACKUP CONSOLE DEVELOPMENT AND CUSTOMER SHIP STRATEGY, BUT IS NOT AS COST EFFECTIVE AS THE PDT/TOBY/UNIBUS.

3. ANY NEW UNIBUS CPU PRODUCT, WHICH IS MORE COST EFFECTIVE THAN THE 1134A, CAN BE IMPLEMENTED PRE OR POST FCS.

2.0 CONSOLE DESCRIPTION

2.1 DOLPHIN CONSOLE MICRO SYSTEM ARCHITECTURAL REQUIREMENTS

THIS SECTION IS WILL ADDRESS THE ARCHITECTURAL REQUIREMENTS OF THE DOLPHIN CONSOLE MICRO SYSTEM .

THIS SECTION WILL NOT ATTEMPT TO DEFINE THE WAY IN WHICH THESE REQUIREMENTS HANG TOGETHER, BUT DEFINE THE FUNDAMENTAL REQUIREMENTS AND FUNCTIONALITY OF WHAT I PERCEIVE TO BE THE "INTELLIGENT" NUCLEUS OF THE DOLPHIN CONSOLE DESIGN.

THIS SECTION FREQUENTLY USES THE TERMS MICROPROCESSOR, MICROSYSTEM OR ALLUDES TO THE USE OF MICRO PRODUCTS. THERE ARE 2 BASIC REASONS FOR IMPLEMENTING A MICRO PRODUCT, 1) NOT UTILIZING A MICRO PRODUCT WILL JEOPARDIZE THE COST GOAL ESTABLISHED IN ITEM 23, 2) ANY AVAILABLE CORPORATE TECHNOLOGY WHICH COULD ACCOMODATE THE FEATURES DESIRED (SECTION ONE), WILL REQUIRE A CABINET AND DRAWER. LARGE MICROSYSTEMS CAN BE PROVIDED IN A TERMINAL ENCLOSURE, OR ON A SINGLE HEX MODULE.

1. 8K EPROM MEMORY FOR DOLPHIN BOOTSTRAP, DIAGNOSTICS, CONSOLE FUNDAMENTAL ROUTINES.

2. 48K (18 BIT WORD) MAIN RAM (DYNAMIC) MEMORY.

3. SYSTEM MUST SUPPLY REFRESH FOR THE DYNAMIC RAM.

4. INTENTIONALLY LEFT BLANK.

5. MEMORY MUST BE DIRECTLY ADDRESSABLE AND EXPANDABLE UP TO 128K WORDS MINIMUM.

6. MEMORY MANAGEMENT, WITH ASSIGNABLE KERNAL AND USER INSTRUCTION SPACE, ACTIVE PAGE REGISTER, ACCESS ERROR DETECTION (PAGE) E.G., LIKE 11/40, 1134A, ETC., IS DESIRABLE BUT NOT REQUIRED.

7. THE MICROSYSTEM MTBF GOAL (PURE ELECTRONICS) IS 10K HOURS. THE MICROSYSTEM WITH ELECTRO MECHANICAL DEVICES MTBF IS T.B.D.

8. THE CPU, BUS, CSR'S (CONTROL AND STATUS REGISTERS) MUST HAVE PARITY.

8A. RAM CHOICES SHOULD CONSIDER SOFT FAILURE RATES AND THEIR EFFECT ON THE MICROSYSTEM MTBF. IF THE RAMS EXHIBIT SOFT FAILURES GREATER THAN 1 IN 10 HOURS, AN ECC SCHEME OR A DIFFERENT RAM CHOICE S.B. IMPLEMENTED.

9. THE EXTERNAL BUS OF THE SYSTEM IS A UNIBUS.

10. DISTANCE FACTORS ARE IMPORTANT IF THE MICRO SYSTEM DOES NOT RESIDE IN THE DOLPHIN ENCLOSURE. A MINIMUM DISTANCE REQUIREMENT IF NOT CO-LOCATED IS 25 FEET, MAXIMUM OF 50 FEET.

11. THE MICRO BUS STRUCTURE MUST ACCOMADATE AT LEAST A FOUR LEVEL PRIORITY INTERRUPT SCHEME. VECTORED INTERRUPTS ARE ALSO A MUST. THIS INCLUDES THE EXTERNAL BUS STRUCTURE.

12. THE MICROPROCESSOR INSTRUCTION SET MUST BE EQUIVALENT TO AT LEAST THAT OF AN 1134A, INCLUDING MUL, DIV, AND IT IS DESIRABLE THAT THE ISP(INSTRUCTION SET PROCESSOR) BE ABLE TO MANIPULATE 8 BIT DATA WITH OUT NEED TO ROTATE, SWAP BYTE,OR MASK. INTRODUCTION OF AN ISP THAT REQUIRES NEW DEVELOPMENT SYSTEMS, OR TOOLS FOR DIAGNOSTIC OR SOFTWARE DEVELOPMENT IS HIGHLY UNDESIRABLE AND SHOULD NOT BE CONSIDERED.

13. THE MICROPROCESSOR WILL EXECUTE AT MINIMUM .2 MEGA (5 USEC AVERAGE, INCLUDES DOUBLE OPERAND INSTRUCTIONS, MULTIPLY, DIVIDE, ETC.) INSTRUCTIONS PER SECOND (EXAMPLE, TIGHT LOOP: MOV @XXX, @R, INC (R), BNE, 7.9 USEC LOOP. THIS SPEED RANGE IS THAT OF AN 1134A CPU WITH CORE MEMORY.

14. A PROGRAMMABLE REAL TIME CLOCK IS DESIRABLE, BUT A FIXED FREQUENCY RTC IS REQUIRED.

15. REQUIRED MICRO SYSTEM/OPTIONS SHOULD BE OFF THE SHELF SUPPORTED PRODUCTS.

16. RS 232-C TYPE D (20K BPS) SERIAL INTERFACES (FIVE) ARE REQUIRED.

17. MASS STORAGE LOAD DEVICE IS REQUIRED FOR STORAGE OF BASIC DIAGNOSTIC SOFTWARE AND SOFTWARE PATCHES (SIMPLE FUNCTION DEVICE, APPROXIMATELY 256 KB STORAGE, 10-20% DUTY CYCLE, MTBF 2000 HOURS, 90% CONF).

18. THE PACKAGING WOULD BE DESIRABLE IN A TERMINAL ENCLOSURE. IT SHOULD BE OF COMPACT SIZE, AND THE TERMINAL INTERFACE PROVIDES A FLEXIBLE HUMAN INTERFACE. THE ENCLOSURE FOR THE MICRO SYSTEM SHALL BE HIGHLY MAINTAINABLE, SERVICABLE, RELIABLE, AND EASILY DISCONNECTED FROM THE REST OF THE COMPONENTS IT INTERFACES TO. THE MICRO SYSTEM MUST ALSO BE CAPABLE OF DISCONNECT DURING DOLPHIN SYSTEM OPERATION WITH OUT

INTERRUPTION TO THE OPERATING SYSTEM.

19. POWER CONSUMPTION SHALL BE WITHIN 200-400 WATTS.

20. INTENTIONALLY LEFT BLANK

21. DMT, PMT, UL, CSA, IEC SPECIFICATIONS AND REGULATIONS MUST BE MET.

22. THE POWER ON DATE OF THE DOLPHIN CONSOLE IS JULY 1979. IT IS DESIRABLE THAT THE MICROSYSTEM BE AVAILABLE ON THIS DATE. IT IS REQUIRED THAT THE MICROSYSTEM BE AVAILABLE BY NO LATER THAN OCTOBER 1979.

23. THE TRANSFER COST GOAL OF THE MICRO SYSTEM WITH 48K WORDS RAM, 8K ROM, INTERFACE BUS, 5-RS 232-C INTERFACES, RIC, REFERENCE SECTION ONE, WILL BE $1,5K OR LESS.

2.1.1 PRIMARY STRATEGY:F-11 MICROSYSTEM

THE F-11 MICROSYSTEM WILL PROVIDE THE NUCLEUS FOR THE CONSOLE SYSTEM. THE FONZ-11 IS A FAMILY OF CUSTOM CHIPS THAT CONTINUES PDP-11 INSTRUCTION SET COMPATIBILITY. THE CHIP SET IS COMPATIBLE WITH INDUSTRY AVAILABLE CHIPS, E.G., INTEL, MOTOROLA, ETC.,,THE MAJOR DISADVANTAGE IS THAT THE AVAILABLE PDP11 SOFTWARE IS NOT I/O DRIVER COMPATIBLE AND THUS ALL EXISTING SOFTWARE (PDP11) MUST BE REWRITTEN. THE SOLUTION TO THIS IS TO EMULATE THE NECESSARY I/O DEVICES THRU HARDWARE OR SOFTWARE. THE NOW CALLED "TOBY" MACHINE WHICH IS GEARED TO REPLACE THE ALREADY EXISTING SMART TERMINAL PROCESSER BOARD (P.O. HTE PDT11 SERIES OF SMART TERMINALS) CALLED "TIM".

TOBY IS A SINGLE BOARD COMPUTER SYSTEM DESIGNED TO PROVIDE HIGH PERFORMACE PDP-11 ISP (INSTRUCTION SET PROCESSING) IN INTELLIGENT TERMINALS. THERE ARE THREE MAJOR SECTIONS TO THE TOBY ARCHITECTURE. THE FIRST IS THE INSTRUCTION SET PROCESSOR AND ITS MAIN MEMORY. THE SECOND IS AN I/O PROCESSOR WHICH IS OPERATING IN PARALLEL WITH THE ISP PROCESSOR AND HANDLES ALL OF THE I/O. THE THIRD SECTION IS A DMA CHANNEL WHICH IS SWITCHABLE BETWEEN THE I/O PROCESSOR AND THE ISP PROCESSOR. THE DMA SYSTEM IS FOR HANDLING HIGH SPEED DATA. THE SYSTEM IS DESIGNED TO ACOMADATE I/O PROCESSOR FIRMWARE THAT REGISTER EMULATE SPECIFIC PDP-11 OPTIONS. THE FIRMWARE CAN ALSO BE CHANGED TO ADD SPECIAL CODE TO THE SYSTEM IN THE I/O PROCESSOR.

THE BASIC TOBY BOARD WILL CONTAIN THE FONZ-11 CONTROL AND DATA CHIPS 16K WORDS OF MEMORY, 3 SERIAL LINE UNITS, A CLOCK, AN 8-BIT BIDIRECTIONAL PARALLEL PORT AND A GENERALIZED DMA PORT WHICH CAN BE BIT SERIAL OR 16 BIT PARALLEL. THE RX02 CAN PLUG DIRECTLY INTO THIS BOARD. THERE WILL BE MEMORY EXPANSION FACILITIES CONTAINED ON

DAUGHTER BOARDS UP TO 64K WORDS OF RAM MEMORY. THERE WILL ALSO BE 2K WORDS OF ROM SPACE ON THE MAIN BOARD. ROM EXPANSION CAN BE PROVIDED VIA DAUGHTER BOARD ARRANGEMENTS.

THE BASIC CPU ADDRESSING CAPABILITY IS 28 K WORDS WITHOUT MEMORY MANAGEMENT, WITH 4K I/O PAGE. THE MEMORY MANAGEMENT UNIT (MMU) WILL BE INCLUDED ON A DAUGHTER BOARD ALONG WITH THE MICROM (ISP) AND CIS, FPP CHIPS. THIS BOARD WILL ALSO PROVIDE ADDITIONAL MEMORY EXPANSION.

2.1.2 SIZE

THE SIZE OF THE TOBY BOARD IS 10.437 INCHES BY 10.437 INCHES

2.1.3 POWER

THE POWER REQUIRED FOR THE BASIC BOARD IS (ESTIMATE):

AMPS +12 VDC

AMPS +5VDC

AMPS -12VDC

2.1.4 PDP-11 DIFFERENCES

THE FIRST 2K WORDS OF THE I/O PAGE IS USED FOR DIAGNOSTICS AND BOOTSTRAPS. ALL I/O IS RESTRICTED TO THE TOP 2K WORDS OF THE I/O PAGE.

2.2 TOBY AND THE VT100

TEH TOBY WHEN INTEGRATED WITH THE VT100 PRODUCES A YET UNNAMED VERSION OF THE PDT SERIES OF INTELLIGENT TERMINALS. BECAUSE OF THE ARCHITECTURAL CHARACTERISTICS (MMU, FFP, CIS, CRT, SLU'S, TU58, ETC.) THE TOBY VERSION OF THE NEW INTELLIGENT TERMINAL SERIES PROVIDES AN "ENGINE"TO BASE THE DOLPHIN CONSOLE DESIGN ON. FOR FURTHER INFORMATION REFERENCE TOBY SPECIFICATION.

2.3 DOLPHIN CLOCK AND DISTRIBUTION

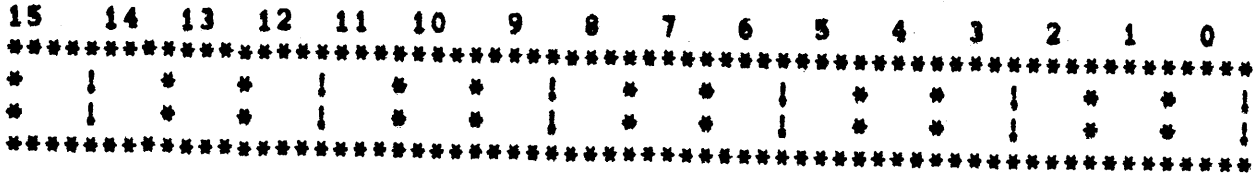
THE CLOCK AND DISTRIBUTION WILL BE BUILT IN MCA'S AND RESIDE ON THE CONSOLE HEX MODULES IN THE DOLPHIN ENCLOSURE.THE CLOCK WIL BE SIMILAR TO THE KL10 BUT WITH THE FOLLOWING ENHANCHMENTS. THE CLOCK WILL SUPPORT BURST,SINGLE STEP,START,STOP,AND CONTINUATION FROM CLOCK STOP.THE CLOCK STEP WILL BE IN HALF CYCLE INCREMENTS.THE CLOCK WILL ALSO PROVIDE 1/2 MEGAHERTZ INCREMENTS BETWEEN 50-70 MEGAHERTZ FOR SPEED MARGINS. THE CLOCK SYSTEM WILL ALSO BE CAPABLE OF ARBITRARILY STOPPING CLOCK SOURCES TO VARIOUS PORTIONS OF THE SYSTEM.THIS MEANS THAT THE MEMORY CLOCKS WILL BE RUNNING WHEN THE CPU CLOCKS ARE STOPPED.THE CLOCK PARTIONING WILL AT LEAST PROVIDE SEPERATE CLOCK DISABLES TO THE

CPU,MEMORY,I/O,AND THE DOLPHIN BUS. THE CLOCK TO THE MEMORY WILL BE BATTERY BACKED UP TO PROVIDE DATA INTEGRITY IN CASE OF POWER OUTAGES,A SELECTABLE CLOCK STOP ENABLE WILL BE PROVIDED. THIS WILL ENABLE THE FIELD PERSONEL TO SELECT THE ERROR STOP CONDITION DESIRED.

THE SMP CLOCK SCHEME WILL INCLUDE AN EXTERNAL OSCILLATOR WHICH PROVIDES CLOCK SOURCE AND PHASE INFORMATION TO THE CONSOLE BOARDS WHICH WILL THEN DISTRIBUTE THE INFORMATION TO THE REST OF THE SYSTEM.

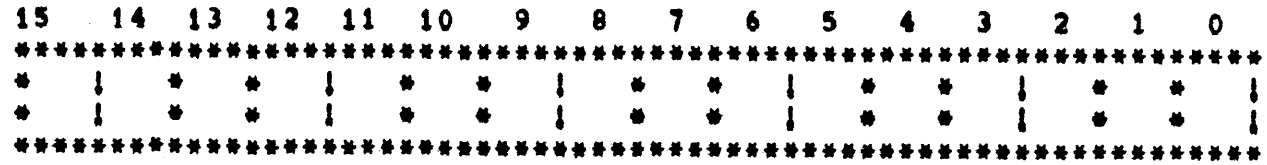
CLOCK PROGRAMMING

REGISTER 1



BITS	DEFINITION
<15>	• BURST THE CLOCK,THE LOADING OF THE BURST COUNT REGISTER MUST HAVE BEEN BY AN PREVIOUS OPERATION.
<14>	• READY TO INTERRUPT.
<13>	• ENABLE INTERRUPTS
<12>	• CONTINUE SYSTEM CLOCKS FOR AS MANY CYCLES AS INDICATED IN THE BURST COUNT BITS
<11>	• EXTERNAL CLOCK CLEAR.
<10>	• EXTERNAL CLOCK ENABLE,ALLOWS THE EXTERNAL OSCILLATOR BE SELECTED.
<9>	• STOP THE SYSTEM CLOCKS
<8>	• START THE SYSTEM CLOCKS
<7:0>	• CLOCK BURST COUNT,TO BE LOADED BEFORE BURST CLK IS ENAB

REGISTER 2



BITS DEFINITION

<15:13> CONDITION CHECK BITS(STOPS SYSTEM CLOCKS, AND LOCKS THE RECORDER) SEE BUS RECORDER PROGRAMMING

TABLE
000 =SINGLE BIT ERROR
001 =DOUBLE BIT ERROR
010 =PARITY BIT ERROR
011 =CONTROL ERROR
100 =FIELD SERVICE PROBE
101 =TBD
110 =TBD
111 =TBD

<12> = PHASE LOCK LOOP IN LOCK ,THE CLOCK OSCILLATOR IS IN LOCK, IF THIS BIT IS FALSE THE CLOCK SYSTEM IS NOT OPERATING PROPERLY.

<11> = BATTERY BACKUP IS CONNECTED AND AVAILABLE.

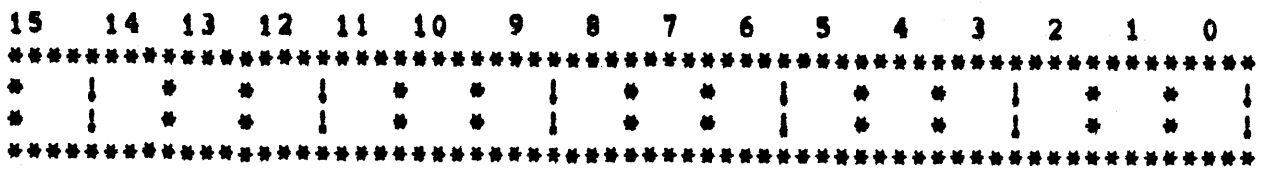
<10> = LOAD CONDITION CHECK BITS

<9> = CLEAR CONDITION CHECK

<8> = SELECT MARGINS

<7:0> = MARGINS SPEED SELECT BITS (TBD)

REGISTER 3



BITS DEFINITION

<15:4> = UNUSED

<3> = LOAD CLOCK CONDITIONS

<2:0> - CLOCK CONDITIONS,ENABLES TO CLOCK PARTIONS

TABLE
<00> - MEMORY CLOCKS
<01> - I/O CLOCKS
<10> - BUS CLOCKS
<11> - CPU CLOCKS

2.4 DOLPHIN BUS RECORDER

THE DOLPHIN BUS RECORDER IS DESIGNED TO SERVE TWO PURPOSES, ONE IS TO ACT AS A BUS RECORDER FOR ALL DOLPHIN BUS ACTIVITY, THE SECOND IS AS DOLPHIN RANDOM ACCESS MEMORY.

WHEN THE BUS RECORDER IS IN THE "RECORD" STATE IT LATCHES ALL INFORMATION (62 WIRES, SEE DOLPHIN BUS SPECIFICATION FOR DESCRIPTION OF THE 62 WIRES) WHICH IS PRESENT DURING THE IMMEDIATE BUS CLOCK CYCLE, ALL INFOMRATION IS STORED IN THE MANNER IT IS LATCHED OFF THE BUS AND ECC ERRORS ARE LOGGED INTO THE RECORDER "AS SEEN" BY THE BUS CHIP SET WITH NO ECC CORRECTION APPLIED, THE CLOCK MAY BE STOPPED WHEN "SPECIAL" ERRORS ARE DETECTED BY THE RECORDER (SEE CLOCK PROGRAMMING), THE INFORMATION MAY THEN BE DUMPED TO THE CONSOLE MEMORY, THE STORAGE OF THE RECORDER WILL BE 256 WORDS BY 64 BITS WIDE, THE RECORDER WILL OPERATE AT BUS SPEED (30 MEGA HZ).

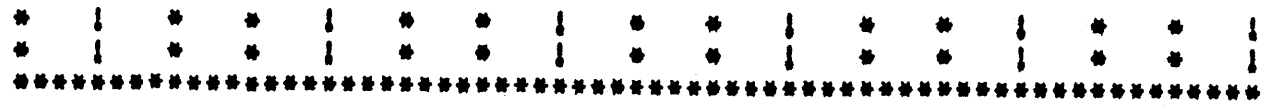
IN RECORDER MODE, THE MEMORY ACTS AS A PUSH DOWN STACK AND AS THE 255TH CYCLE IS LOGGED THE NEXT CYCLE LOGGED WILL CAUSE THE STACK TO "OVERFLOW" AND THE BOTTOM OF THE STACK DATA TO BE LOST.

THE RECORDER ALSO SERVES AS RANDOM ACCESS MEMORY, WHEN IN THIS MODE, THE RECORDER IS USED AND SEEN BY THE DOLPHIN CPU AS "DOLPHIN MEMORY", TO SIMPLIFY THE DESIGN THE RECORDER IN MEMORY MODE WILL NOT SUPPORT 2 OR 4 WORDS TRANSFERS.THE PSUEDO DOLPHIN MEMORY CAN BE USED TO EXECUTE BASIC DOLPHIN DIAGNOSTICS, IT CAN ALSO BE USED FOR EXECUTING INITIATIZATION/CONFIGURATION ROUTINES WHEN STARTING A COLD SYSTEM, ONCE THE SYSTEM IS INITIALIZED AND CONFIGURED, THE MEMORY CAN BE USED TO BOOTSTRAP THE MONITOR INTO MAIN MEMORY, BEFORE THE MONITOR BEGINS OPERATING THE CONSOLE MUST BE TOLD TO TURN THE RECORDER BACK TO "RECORDER MODE" FOR SYSTEM OPERATION.

THE RECORDER WHEN IN "BOOT MEMORY MODE", RESPONDS TO ADDRESS BIT 27 ON A 1 FOR A TOTAL OF 256 WORDS, IN AN SMP SCHEME THE TOAL WORDS OCCUPIED IS 1K WORDS.

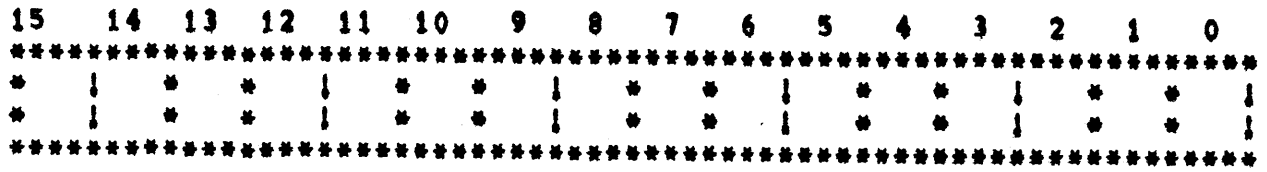
REGISTER 1

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
****



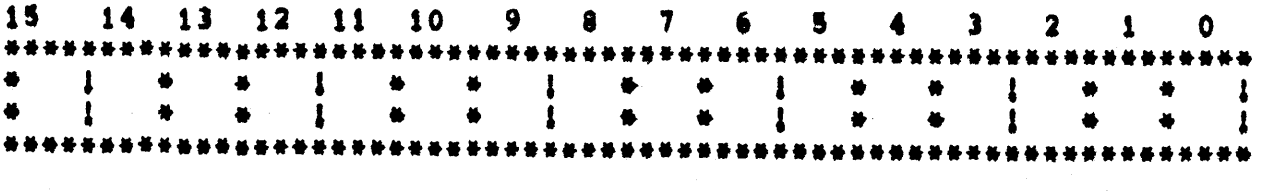
BITS	DEFINITION
<15:0>	- RECORDER DATA (1 OF 4 WORDS READ, WHICH WORD IS INDICATED BY THE BYTE COUNT, THE MEMORY ADDRESS POINTS AT THE 10 WORD LOCATION IN THE RECORDER.

REGISTER 2



BITS	DEFINITION
<15:8>	-RECORDER MEMORY ADDRESS
<9>	-UNUSED
<7>	- READY TO INTERRUPT
<6>	- ENABLE INTERRUPT
<5>	- FAULT LINE TRUE IN MESSAGE
<4>	- BUS CHIP SET ECC ERROR
<3:2>	- BYTE COUNT
<1>	- ADDRESS MODE SELECT, SEQUENTIAL OR RANDOM
<0>	- RUN, RECORDER IS LOGGING THE DOLPHIN BUS

REGISTER 3



BITS	DEFINITION
<15:9>	- UNUSED
<8>	- CLEAR RECORDER RUN STATE

<7> - UNLOAD RECORDER WORD

<6> - CLR RECORD NULL CYCLE

<5> - SET RECORD NULL CYCLE

<4> -UNUSED

<3> -UNUSED

<2> - PARITY ERROR IN RECORDER RAMS

<1> - CLR STOP ON CLOCK CHECKS

<0> - ENABLE STOP RECORDER ON CLOCK CHECKS

2.5 DOLPHIN BUS INTERFACE

THE BUS ACCESS REGISTER WILL BE PROVIDED VIA A BUS CHIP SET,IT WILL PROVIDE THE FOLLOWING FUNCTIONS FOR THE DOLPHIN CONSOLE:

A. DEPOSIT EXAMINES FROM THE PDP11 CPU

B. CHECK BUS BIT STATES FROM THE PDP11

C. TRANSMIT A PACKET TO ANY DEVICE ON THE DOLPHIN BUS

D. PDP11 TO ACT AS PSEUDO DOLPHIN CPU (NOT FULL SPEED)

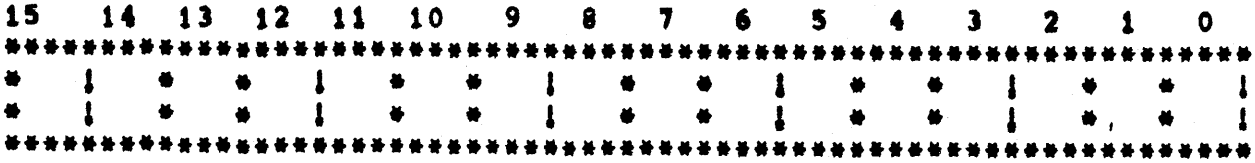
E. I/O PORT FOR DOLPHIN ACCESS TO THE PDP11

F. THE ACCESS REGISTER WILL SUPPORT "TO 10","TO 11" INTERUPTS

G. PDP11 ACCESS TO THE BUS CHIP SET WILL BE VIA 1-16 BIT 11 I/O REGISTER, THE COMPLETE BUS WORD WILL BE MAPPED INTO FOUR PDP11 WORDS.

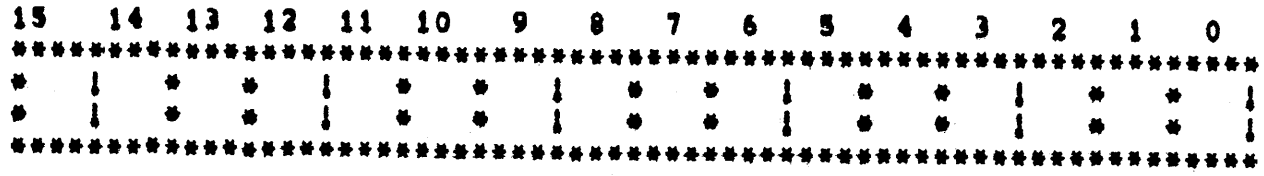
BUS INTERFACE PROGRAMING

REGISTER 1



BITS	DEFINITION
<15:0>	- BUS CHIP DATA(ONE OF FOUR WORDS,MSB FIRST)

REGISTER 2



BITS	DEFINITION
<15>	• SET TO TEN INTERUPT
<14>	• MEM EXAMINE DONE
<13>	• EXAMINE DOLPHIN MEMORY (EX GO)
<12>	• DEPOSIT DONE
<11>	• DEPOSIT DOLPHIN MEMORY
<10>	• TBD
<9>	• CHIP SET CONTAINS A WORD TO BE XFERRED TO 11 MEM (INT)
<8>	• ENABLE INTERUPTS
<7:6>	• WORD COUNT (WHEN READING OR WRITING CHIP SET)
<5>	• LOAD WORD INTO BUS CHIP SET (FROM DATA REGISTER, POSITION BY WORD COUNT)
<4>	• UNLOAD WORD FROM CHIP SET (TO DATA REGISTER,POSTION BY WORD COUNT)
<3>	• TBD
<2>	• TBD
<1>	• TBD
<0>	• TRANSMIT PACKET (CHIP SET GO,SELF CLR BIT)

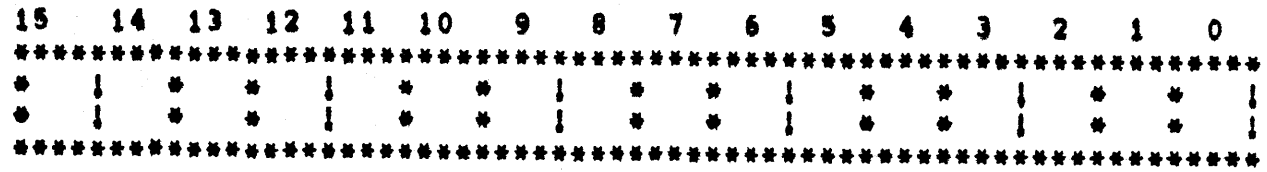
2.6 DOLPHIN TIME OF DAY CLOCK

THE TIME OF DAY CLOCK IS BATTERY POWERED AND WILL BE USED AS A SOURCE OF 24 HOUR DAY TIME ,WHICH SHOULD ALWAYS BE ACCURATE (ONCE IT IS SET) REGARDLESS OF POWER FLUCTUATIONS.THE CLOCK CONTAINS TWO SIXTEEN BIT WORDS FOR A TOTAL WORD LENGTH OF 32 BITS.THE CLOCK WILL RUN FOR AT LEAST 100 HOURS WITHOUT AC INPUT POWER.THE ACCURACY OF THE CLOCK IS T.B.D..

THE TOD CLOCK MAY BE PROVIDED IN INDUSTRY COMPATIBLE 24 HOUR MOS CHIP SET.BATTERY BACKUP WILL ALSO BE PROVIDED IF THIS SCHEME IS USED.THE ACCURACY OF THIS CHIP SET WILL BE AT LEAST THAT OF THE REGISTER SCHEME.

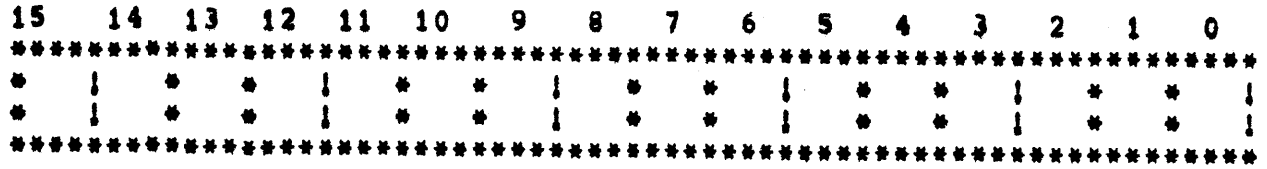
TOD PROGRAMMING

REGISTER 1



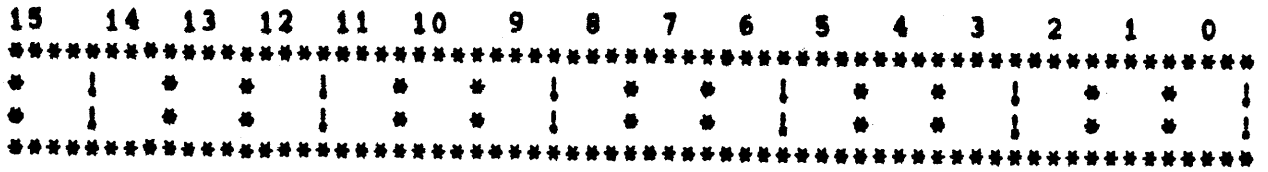
BITS	DEFINITION
<15:0>	- HIGH ORDER 16 BIT OF TIME DATA (BITS ARE R/W)

REGISTER 2



BITS	DEFINITION
<15:0>	- LOW ORDER 16 BITS OF TIME DATA (BITS ARE R/W)

REGISTER 3

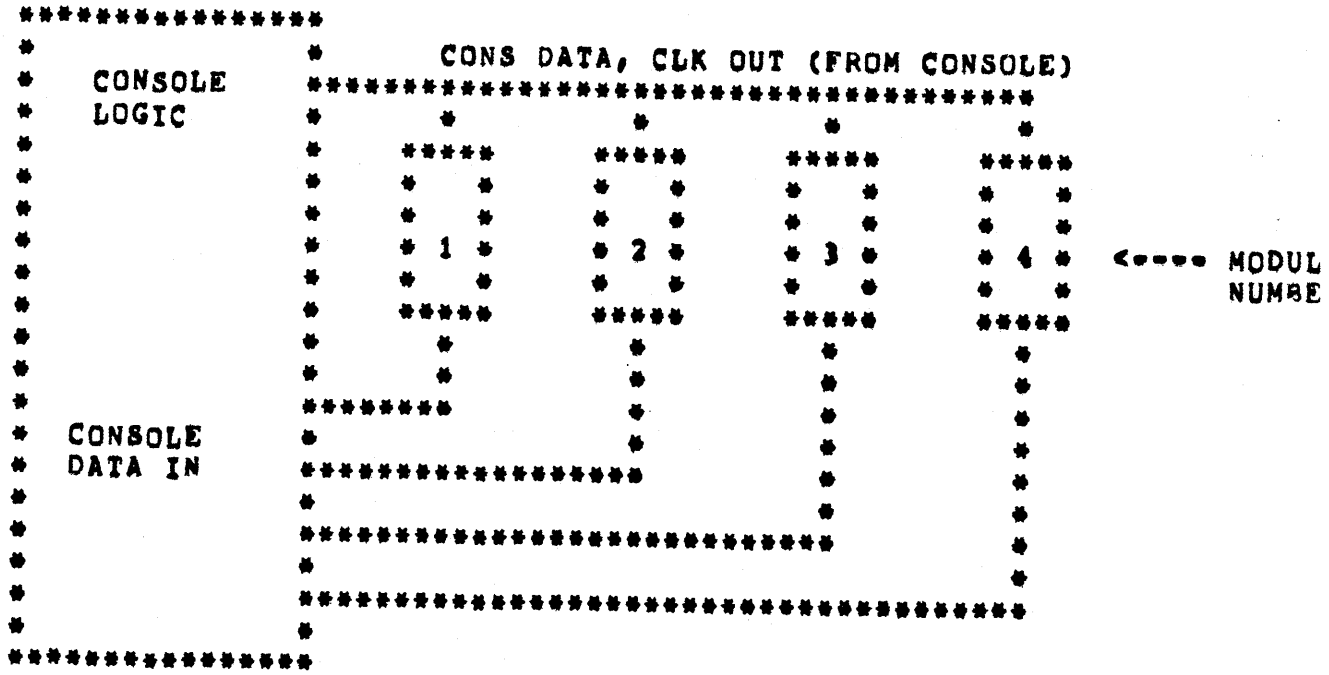


BITS	DEFINITION
<15:6>	- TBD
<5>	-DISABLE WRITE OF TIME OF DAY REGISTER
<4>	-ENABLE WRITE OF TIME OF DAY REGISTER
<3>	- BATTERY BACKUP OK
<2>	- DISABLE TOD CLOCK
<1>	- ENABLE TOD CLOCK

<0> = RESET TOD CLOCK

2.7 DIAGNOSTIC LOGIC

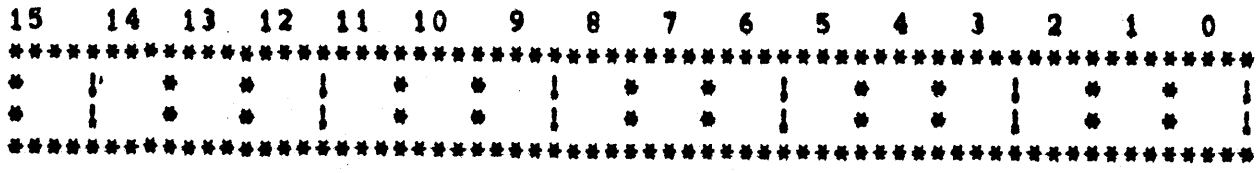
THE DIAGNOSTIC LOGIC IN THE MCA IS AN IMPORTANT PART OF THE DIAGNOSTIC AND MACHINE CONFIGURATION CAPABILITY. THE DIAGNOSTIC LOGIC ON THE MCA'S IS DESIGNED TO BE CONNECTED TOGETHER IN SERIAL. ALL THE MCA'S ON A SINGLE MODULE ARE CONNECTED TOGETHER IN ONE SERIAL STRING. EACH MODULE IS CONNECTED TO THE CONSOLE SEPARATELY. THE DATA OUT FROM THE CONSOLE IS A SINGLE WIRE DISTRIBUTED TO ALL MODULES. THE DATA IN FORM EACH MODULE COMES IN ON A SEPARATE WIRE. THE DIAGNOSTIC CLOCKS ARE ISSUED BY THE CONSOLE. THE CLOCK IS DISTRIBUTED TO ALL THE MCA'S VIA ONE WIRE. THE DIAGNOSTIC LOGIC ALSO REQUIRES THAT ALL MCA MODULES TOUCH THE DIAGNOSTIC LOGIC ADDRESS BUS.THE ADDRESS BUS CONSISTS OF SEVEN BIT WIDE ADDRESS BUS,FOUR OF THE WIRES ARE FOR MODULE ID. TWO OF THE WIRES PROVIDE SYSTEM/BOARD PARTIONING,THE LAST WIRE (BIT) IS FOR SELECTING ALL MODULES TO ENABLE CLOCK TO THE MODULE (REGARDLESS OF THE ADDRESS) TO ALLOW THE FUNCTION CODE COMMANDS TO BE SHIFTED INTO THE MCA .THERE ARE FIVE REGISTERS ASSOCIATED WITH USING THE DIAGNOSTIC LOGIC.



2.7.1 MODULE SELECT/CONTROL AND STATUS

THE MODULE SELECT FIELD IS USED TO SELECT WHICH MODULE IS BEING ASSESSED BY THE DIAGNOSTIC LOGIC. TRANSMITTING THE DIAGNOSTIC FUNCTION CODE REQUIRES ALL MODULES TO BE ACCESSED SIMULTANEOUSLY WHEN A SNAPSHOT IS BEING TAKEN. IF BIT 0 IS

SET ALL MODULES ARE ACCESSED REGARDLESS OF THE MODULE SELECT CODE.

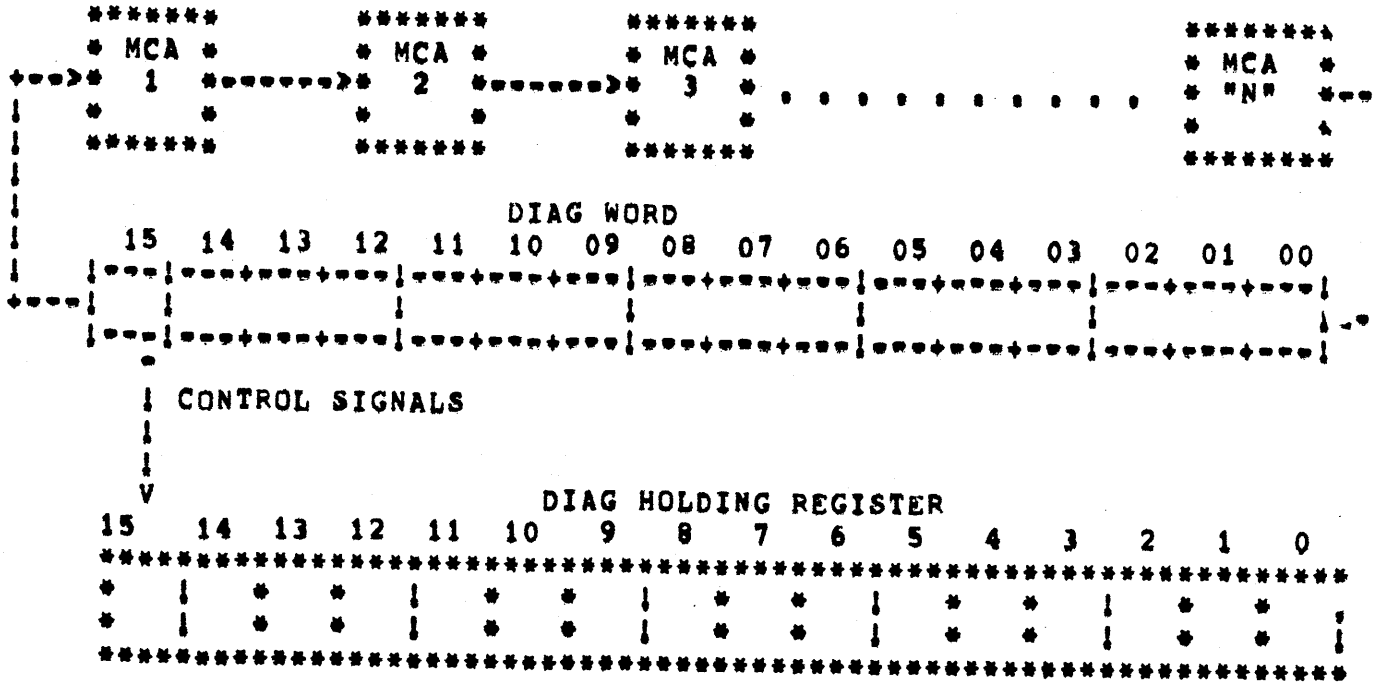


BITS	DEFINITION
<15>	= CLR DATA VALID
<14>	= DATA VALID (HOLDING REGISTER IS LOADED,INT.)
<13>	= AUTO REPEAT (REPEAT 16 SHIFTS AND UNLOAD THE DIAG WORD TO THE HOLDING REGISTER).
<12>	= ENABLE INTERUPTS
<11>	= CLOCK SHIFT COUNT DONE (INT)
<10>	= 1=PRELOAD THE SHIFT COUNT WITH 16, 0=PRELOAD COUNT WITH 4 (USED IN CONJUNCTION WITH AUTO REPEAT)
<9>	= ENABLE DIAG CLOCK (SHIFT COUNT MUST BE LOADED)
<8>	= DISABLE DIAG CLOCK
<7>	= UNUSED
<6:3>	= DIAGNOSTIC BUS, MODULE ADDRESS SELECT
<2:1>	= SYSTEM PARTITION 00=CPU SELECTED 01=MEM SELECTED 10=I/O SELECTED 11=HALF BOARD SELECT
<0>	= WHEN SET THE DIAGNOSTIC CLOCK IS SELECTED FOR ALL MODULES

2.7.2 DIAG DATA WORD

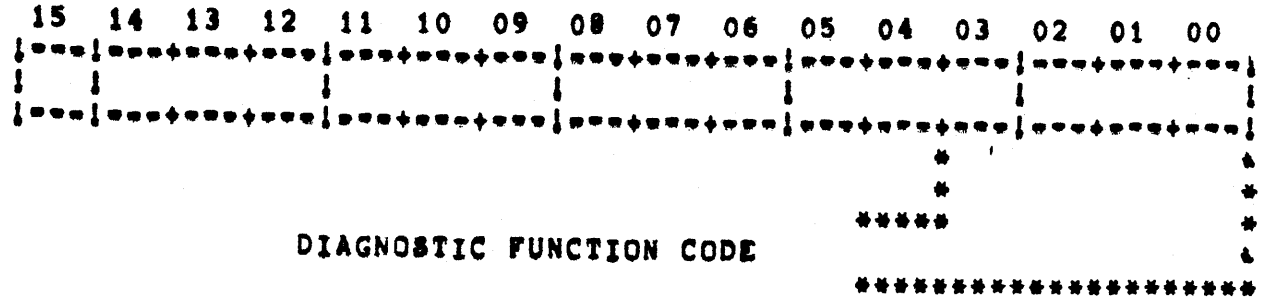
THE DIAG DATA WORD IS USED BY THE SOFTWARE TO EXTRACT OR INSERT DATA INTO THE DIAGNOSTIC SHIFT PATH. THE REGISTER IS INITALLY EMPTY. THE DIAGNOSTICS DATA WORD HAS A HOLDING REGISTER ASSOCIATED WITH IT. THE HOLDING REGISTER READS OR WRITES THE DIAGNOSTIC DATA WORD. WHEN A CHARACTER IS SHIFTED INTO THE DIAGNOSTIC DATA WORD IT IS LOADED INTO THE HOLDING REGISTER AT THE END OF THE 16TH CLOCK CYCLE. THE CLOCK MAY STOP AT THIS TIME TO ALLOW DIRECT WRITING OF A NEW DIAGNOSTIC DATA WORD. THE HOLDING REGISTER CAN BE READ AT THIS TIME AND THE PROCESS MAY PROCEED. IF A SNAP SHOT IS BEING TAKEN AT THIS TIME THE DATA VALID MUST BE USED TO

IDENTIFY WHEN THE CONSOLE MUST READ THE HOLDING REGISTER. SNAP SHOT MODE IS AN AUTOMATED MODE AND THE DATA VALID BIT WILL CAUSE AN INTERRUPT TO THE PDP11 IF ENABLED. WHEN THE INTERRUPT OCCURS THE PROGRAM WILL HAVE 16 CLOCK CYCLES TO REMOVE THE DATA WORD AND CLEAR THE DATA VALID BIT. IF IN AUTO REPEAT MODE THE PDP11 FAILS TO REMOVE A WORD IN TIME (SIGNALED BY CLEAR OF DATA VALID) THE DIAGNOSTIC LOGIC WILL STOP UNTIL THE BIT IS CLEARED. ANOTHER REGISTER USED IN CONJUNCTION WITH THESE REGISTERS IS THE SHIFT COUNT. A SHIFT OF ONE RESULTS IN THE FIRST BIT OF THE DATA FROM THE MCA'S BEING SHIFTED INTO BIT POSITION 00. A COUNT OF 256 WOULD RESULT IN THE 256 BIT IN THE SHIFT PATH BEING IN BIT POSITION 00. THE DATA OR BITS IN POSITION 15 ARE SHIFT BACK INTO THE MCA SHIFT PATH.



2.7.3 FUNCTION TRANSMIT

THIS WORD CONTAINS THE FUNCTION TO BE TRANSMITTED TO THE MCA DIAGNOSTIC LOGIC.

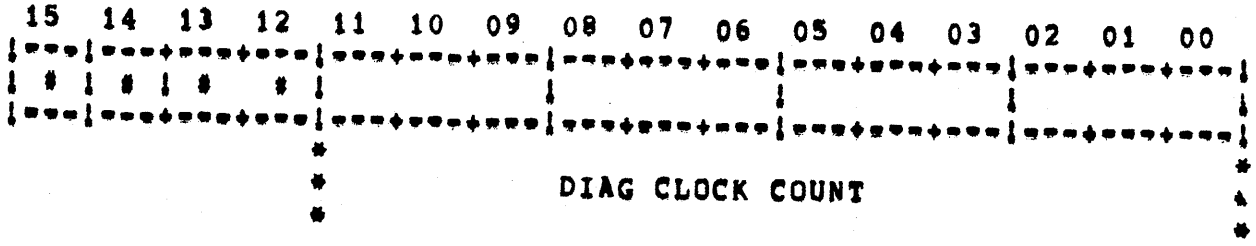


1. FUNCTION CODE 0 =SHIFT THE SELECTED REGISTER IN THE MCA
2. FUNCTION CODE 1 =SELECT DATA INPUT 1.
3. FUNCTION CODE 2 =SELECT DATA INPUT 2.
4. FUNCTION CODE 3 =SELECT DATA INPUT 3.
5. FUNCTION CODE 4 =STATUS LOAD
6. FUNCTION CODE 5 =CHIP RESET
7. FUNCTION CODE 6 =LOAD BUS CHIP SET MASK
8. FUNCTION CODE 7 =F7 UNUSED

2.7.4 DIAGNOSTIC SHIFT COUNT

THE DIAGNOSTIC SHIFT COUNT IS USED TO ISSUE MCA DIAGNOSTIC CLOCKS. THE MCA DIAGNOSTIC CLOCK PERFORMS DIFFERENT FUNCTIONS ON THE RISING AND FALLING EDGES. THEREFORE THE COUNT IS ONE FOR EACH EDGE (I.E. A COUNT OF 4 MEANS TWO COMPLETE CLOCK CYCLES).

DIAG CLOCK WORD



2.8 DOLPHIN POWER AND ENVIORMENTAL LOGIC

2.8.1 GENERAL

THE POWER AND ENVIOROMENTAL CONTROL LOGIC WILL PROVIDE THE FOLLOWIMG FUNCTIONS:

-MONITOR ALL MOVING AIR DEVICES AND ATTEMPT TO PINPOINT FAILING COMPONENTS BEFORE THEY FAIL (FANS WILL INCLUDE "HALL" EFFECT DEVICE TO MONITOR SPEED).

-MONITOR (SENSE) ALL SUPPLY VOLTAGES IN THE SYSTEM AND REPORT ALL VARIATIONS TO CONSOLE (PDP11).

-PROVIDE INTERNAL "SYSTEM POWER" RAMPING. E.G. SYSTEMATIC

SEGUENTIAL POWER UP OF THE CPU.

-MONITOR AMBIENT AND ENCLOSURE TEMPERATURES WITHIN THE CPU (NOT PASS/FAIL MONITORING,BUT ANALOG REAL TIME WITH SOFT/HARD LIMITS).

-PROVIDE 863 COMPATIBLE POWER AND ENVIORMENTAL FUNCTIONS, E.G. DOOR OPEN,OVERTEMP,OVERRIDE,INTELLIGENT MESSAGES SHALL BE PROVIDED TO CTY TO WARN OF FAILURE SUCH THAT LIMITS OF SENSED CONDITION CAN BE DETERMINED TO MAKE SOFT/HARD DECISION ABOUT WHETHER THE SYSTEM SHOULD BE TAKEN DOWN,THIS INTELLIGENT DECISION PROCESS WILL BE MADE VIA THE CONSOLE SOFTWARE.

THE PC AND ENVIOROMENTAL LOGIC AND SENSE LOGIC WILL BE CONNECTED TO A CONSOLE SLU. THE CONTROL LOGIC WILL BE CONTROLLED BY AN 8085 MICRO. THE LOCATION OF THIS LOGIC IS TBD,THE FOUR WIRE INTERFACE WILL BE THE ONLY MEANS OF COMMUNICATION BETWEEN THE PC/ENV LOGIC AND THE CONSOLE PDP11,A SIMPLE COMMAND PROTOCOL WILL BE DEFINED FOR THE COMMUNICATION LINK,IT IS IMPORTANT THAT DATA INTEGRITY BE GUARANTEED IN THIS LINK.

THE 8085 WILL PROVIDE EAROM SPACE FOR THE CONSOLE SYSTEM,ANY VOLITALE SYSTEM CONSTANTS WILL BE SENT TO THE 8085 WHEN A POWER FAIL IS SENSED,THIS INFORMATION WILL BE RECOVERED BY THE CONSOLE WHEN POWER RETURNS.

THE POWER CONTROL LOGIC (AND ENV. LOGIC) WILL BE POWERED AT ALL TIMES WHEN THERE IS AC TO THE COMPUTER ROOM,THIS LOGIC MUST BE POWERED TO PROVIDE BASIC LIFE TO THE SYSTEM TO BOOTSTRAP THE POWER UP PROCESS.

IT IS ENVISIONED THAT THE 8085 PROVIDE PROGRAMMED INTELLIGENCE WHEN DEALINGWITH REPORTED (SENSED) CONDITIONS, SOFT AND HARD LIMITS REGISTERS WILL BE PROVIDED (SOFTWARE) TO DEAL WITH REPORTED CONDITIONS,THEY WILL DETERMINE IF THE IMPENDING FAILURE IS CRITICAL ENOUGH TO WARRANT POWERING DOWN THE SYSTEM OR JUST PROVIDING A MESSAGE TO THE PDP11 TO WARN OF THE SPECIFIC FAILURE,THIS SOFT/HARD LIMIT OF THE PC/ENV LOGIC WILL BE FURTHER DEFINED.

2.8.2 ENVIRONMENTAL SENSING

1.0 PURPOSE

THE PURPOSE OF THE ENVIRONMENTAL MONITOR AND CONTROL SYSTEM IS TWOFOLD. PRIMARILY THIS SYSTEM WILL PROVIDE PROTECTION TO THE DOLPHIN BY PREVENTING OVER TEMPERATURE SITUATIONS WHICH CAN SERIOUSLY DAMAGE THE MACHINE. SECONDLY, BY

PROVIDING TIMELY, INTELLIGENT INFORMATION TO FIELD SERVICE, IT WILL INCREASE MTBF AND REDUCE DOWNTIME.

A. ROOM AIR TEMPERATURE

SYSTEM WILL MONITOR TEMPERATURE OF AIR IN ROOM OR ENTERING MACHINE. PROGRAM WILL CONTAIN SOFT AND HARD LIMITS ON MAXIMUM ROOM AMBIENT TEMPERATURE. WHEN ROOM TEMPERATURE INCREASES TO SOFT LIMIT, SYSTEM WILL WRITE HARD COPY MESSAGE TO OPERATOR. THIS ACTION SHOULD PROMPT OPEARATOR TO CHANGE ROOM TEMPERATURE OR ALERT BUILDING MAINTENANCE STAFF. WHEN R.A.T. INCREASES TO HARD LIMIT, SYSTEM SHOULD NOTIFY OPERATOR OF IMPENDING SHUTDOWN, AND THAN PROCEED WITH THE POWER SHUTDOWN SEQUENCE. THIS SECOND STEP IS DIRECTED TOWARD PROTECTING THE PERIPHERALS SINCE THE CPU CABINET WILL HAVE ITS OWN SYSTEM FOR MONITORING INTERAL AIR TEMPERATURE.

B. INTERNAL AIR TEMPERATURE

THERE ARE THREE (3) CARD CAGES WITHIN THE ENCOLSURE. AS A MINIMUM, AIR TEMPERATURE EXITING EACH CARD CAGE AREA WILL BE MEASURED. THIS CAN BE ACHIEVED BY PLACING A TEMPERATURE SENSOR AT THE UPPER END OF AT LEAST TWO, OR POSSIBLY EACH MODULE IN THE ENCLOSURE. WHEN AN OVER TEMPERATURE CONDITION IS REACHED THE SYSTEM WILL RECORD THE LOCATION OF THE PROBLEM, NOTIFY OPERATOR OF IMPENDING SHUTDOWN, AND BEGIN POWER DOWN SEQUENCE. SEE SECTION F REGARDING OVERIDE.

2.8.3 AIR MOVING DEVICES

EACH AIR MOVING DEVICE IN THE SYSTEM SHALL BE EQUIPED WITH A MOTION DETECTOR, PROBABLY A HALL EFFECT DEVICE. THESE DETECTORS CAN BE USED IN TWO WAYS:

CASE 1: CASTASTROPHIC FAILURE, WHEN FAN SPEED DROPS BELOW SOME FIXED HARD LIMIT DUE TO BEARING OR WINDING FAILURE THE MACHINE WILL SHUTDOWN.

CASE 2: PENDING FAILURE, EACH TIME THE MACHINE IS POWERED UP SYSTEM WILL MEASURE AND STORE FAN SPEED. DURING THE ENSUING TIME THE SYSTEM SHOULD BE LOOKING FOR ANY ONE FAN TO EXHIBIT A DECREASE IN SPEED. THERE WOULD BE A FIXED SOFT LIMIT FOR THIS CRITERIA, SOME VALUE LESS THAN FAN SPEED ASSOCIATED WITH MINIMUM AC VOLTAGE. WHEN FAN SPEED GOES BELOW THE SOFT LIMIT, SYSTEM SHOULD TYPE OUT HARD COPY WARNING OF IMPENDING FAILURE FOR FIELD SERVICE INFORMATION.

D. AIR FLOW

DESPITE PROPER OPERATION OF AIR MOVERS, DIRTY AIR FILTERS, OR OTHER MECHANICAL OBSTRUCTIONS, INTERNAL OR EXTERNAL, CAN REDUCE THE FLOW OF AIR AND CREATE EXCESSIVE INTERNAL TEMPERATURES. SYSTEM WILL MONITOR AIR FLOW, WHEN FLOW IS INADEQUATE SYSTEM WILL ALERT OPERATOR TO CHECK FOR EXTERNAL OBSTRUCTIONS, IT WILL ALSO PROVIDE INFORMATION TO FIELD

SERVICE, SO THAT TECHNICIAN WILL KNOW THAT PREVENTIVE MAINTENANCE IS REQUIRED.

E. INTERLOCKS

DEPENDANT ON MECHANCAL CONFIGURATION, TO BE DEFINED.

F. OVERRIDE

THERE WILL BE A HIERARCHY OF SYSTEM FAULTS. FIELD SERVICE WILL HAVE THE ABILITY TO OVERRIDE SOME FAULT SITUATIONS BUT OTHER SITUATIONS, SUCH AS INTERNAL TEMPERATURE SHOULD NEVER BE OVERRIDDEN.

B. POWER CONTROL SENSING

1.0 MONITOR FUNCTIONS

1.1 BUS VOLTAGES

EACH BUS VOLTAGE SHALL BE MONITORED ON THE BACKPLANE OF THE SYSTEM. IF BACKPLANES ARE PARTIONED THEN EACH SECTION SHALL BE MONITORED.

CPU AND I/O PANELS
-5.2
-2.0
 5.0
 2.5 (OPTION)
12.0 (OPTION)

MEMORY PANEL
12.0
-2.0
-5.2

THE NAUTRE OF THESE SIGNALS IS ANALOG. SUITABLE INTERFACES SHALL EXIST TO CONVERT TO LEVELS FOR THE CONSOLE.

2.0 POWER SUPPLY OUTPUT REGULATOR VOLTAGE SENSE

THESE SIGNALS PROVIDE INFORMATION ON THE ISNTERNAL VOLTAGES IN THE MODULES AHEAD OF THE OUTPUT BUS. THERE IS ONE SIGNAL AND A RETURN FOR EACH OUTPUT MODULE. (THERE ARE PRESENTLY 8 MODULES).

SIGNAL IS A DC LEVEL AND RETURN. AMPLITUDE IS PROPORTIONAL TO THE DC OUTPUT VOLTAGE WHICH THE REGULATOR CAN PROVIDE.

AMPLITUDE: 0 TO +20 VOLTS
LOAD Z : TBD

3.0 POWER SUPPLY MODULE OVER TEMPERATURE

THIS SIGNAL INDICATES THAT AN OVER TEMPERATURE CONDITION EXISTS IN A SUPPLY MODULE AND THIS MODULE WHOULD BE DISABLED. THIS SIGNAL IS A SUMMATION OF ALL TEMPERATURE FAULTS INSIDE A PARTICULAR MODULE. SIGNAL SHALL BE A SET OF CLOSED CONTACTS. NORMALLY CLOSED CONTACTS INDICATE NO FAULT.

4.0 SEQUENCE SIGNALS

THESE SIGNALS CONTROL THE TURN ON AND TURN OFF OF OUTPUT REGULATOR MODULES. THESE SIGNALS SHALL REQUIRE A VOLTAGE FOR OPERATION TO TURN ON A REGULATOR VOLTAGE. (THERE ARE AS MANY SIGNALS AS REGULATOR MODULES).

AMPLITUDE: 5 VOLT DC (OR 12V DC POSSIBLE)
LOAD Z : GREATER THAN 1K OHM

OPEN INPUT IS TO BE CONSIDER THE LACK OF A SIGNAL.

5.0 PROGRAMMING SIGNALS

THESE SIGNALS COMMAND THE OUTPUT REGULATORS TO MARGIN THE POWER VOLTAGES EITHER 5 PERCENT HIGH OR LOW FROM THEIR NOMINAL VALUES. DURING LOW MARGINS DC LOW SIGNALS SHALL BE OVERRIDDEN. THERE IS A SIGNAL PAIR FOR EACH MODULE. METHOD OF MARGIN FOR PARALLEL MODULES IS TO BE DETERMINED.

EACH PROGRAMMING CONTROL CONSISTS OF 3 WIRES. THERE IS A COMMON LEAD AND A PLUS MARGIN AND A MINUS PERCENT MARGIN LINE. MARGIN IS PERFORMED BY CONNECTING THE COMMON TO THE DESIRED MARGINLEAD. THIS MAY BE ACCOMPLISHED BY SWITCHES OR ON TRANSISTORS.

AMPLITUDE: EACH LINE 12V
CURRENT SINK: EACH LINE IS 15 MA MAXIMUM.

6.0 POWER CONTROLLER SIGNALS

THESE SIGNAL INTERFACE THE POWER CONTROLLER (869!S) TO THE LOGIC. SIGNAL AMPLITUDE AND SENSE SHALL BE COMPATIBLE WITH THE DEC POWER CONTROL BUS IN DEC STD #123.

SIGNALS

POWER ON/OFF
DC POWER ON/OFF LEAVES FANS ON, BUT NO DC

7.0 EMERGENCY OFF

THIS SIGNAL MUST REMOVE ALL POWER FROM THE CABINET. THIS FEATURE MAY ALSO POWER OFF THE POWER TO THE EXTERNAL TERMINAL OF THE CONSOLE. (THIS AREA NEEDS CLARIFICATION).

8.0 AC SENSE SIGNAL

THIS SIGNAL IS AC LOW. THIS INDICATES THAT THE INPUT LINE VOLTAGE HAS FALLEN BELOW 87 VAC (LINE TO NEUTRAL) AND OPERATION CANNOT BE SUSTAINED. THIS SIGNAL SHALL BE ASSERTED IN TIME TO PROVIDE ABOUT 20 MS. OF SUPPLY HOLDUP TIME.

AMPLITUDE: 15 V MAXIMUM, NO PULL UP.
IMPEDANCE: 100K OHM MINIMUM.

2.9 POWER CONTROL LOGIC

TO BE DEFINED.

2.10 DOLPHIN BUS ARBITRATOR

THE DOLPHIN BUS ARBITRATOR WILL CONSIST OF ONE MCA LOCATED ON ONE OF THE CONSOLE BOARDS,THE ARBITRATOR WILL OPERATE TO DOLPHIN BUS SPECIFICATION.

ACCESS TO THE BUS ARBITRATOR WILL BE PROVIDED VIA THE IIL LOGIC. THE ARBITRATOR CANNOT BE ACCESSED BY ANY OTHER REGISTER .ENABLE OF THE BUS ARBITRATOR WILL BE THROUGH A STATUS CODE PROVIDED ACROSS THE IIL BUS.

DUAL BUS ARBITRATORS WILL RESIDE IN THE CONSOLE FOR HIGH AVAILABILITY PURPOSES,THE PRIMARY OR SECONDARY ARBITRATORS CAN BE DISABLED WHEN NOT IN USE,THIS CONTROL WILL BE PROVIDED THROUGH THE IIL LOGIC.

2.11 TERMINALS

THE PDT11/TOBY TERMINAL WILL BE THE NUCLEUS OF THE CONSOLE SYSTEM. IT ALLOWS EIGHT SLU'S (SERIAL LINE UNITS) TO BE CONNECTED,THE DEFINITION OF THESE PORTS ARE AS FOLLOWS :AN LA120 WILL BE USED ON SLU 2 FOR CTY HARD COPY .THE LA120 IS THE CTY TERMINAL FOR THE DOLPHIN SYSTEM,SLU 1 HAS THE VT100 CONNECTED TO IT .THIS PORT PROVIDES SYSDPY INFORMATION ALONG WITH REAL TIME DISPLAY OF THE INTERNAL REGISTERS OF THE MACHINE VIA THE SPLIT SCREEN ANSI FEATURE OF THE VT100. SLU 3 CONNECTS TO A MODEM (UP TO 1200 BAUD ASYNCHRONOUS,1200 BPS SYNCHRONOUS (212A MODEM))FOR KLINIK USE. SLU 4 WILL PROVIDE A MULTIDROP COMMUNICATIONS LINK FOR DUAL /SMP INTERPROCESSOR COMMUNICATIONS,SLU 5 WILL BE USED TO

COMMUNICATE TO THE POWER CONTROL LOGIC.

2.12 REAL TIME DISPLAY INFORMATION

THE FOLLOWING IS A LIST OF THE REAL TIME DISPLAY FEATURES OF THE DOLPHIN CONSOLE CRT DISPLAY.

AS THE MACHINE OPERATES IT IS NECESSARY TO PROVIDE SOME INFORMATION ABOUT THE MACHINE INTERNAL MODES, STATES TO TEH OPERATOR.THE INFORMATION SHOULD UPDATED ON INTERVALS OF TIME WHICH IS PROGRAMMABLY SETTABLE VIA A CONSOLE COMAND.THE CONSOLE SHOULD UPDATE THE REAL TIME DISPLAY AND HOLD THE DATA WHEN THE MACHINE HALTS.

PI SYSTEM INFORMATION

ACTIVE (PION, 7 BITS)

REQUEST (PIR, 7 BITS)

IN PROGRESS (PIH, 7 BITS)

PI ON (1 BIT)

MODE (EXEC/USER OR KERNAL/SUPER/CONCEAL/PUBLIC)

STATE (RUN/PROG-STOP/MANUAL-STOP)

PROGRAM COUNTER

VMA AND REFERENCE MODE (EXEC/USER)

MEMORY DATA

MICROCODE INFORMATION (TBD)

CACHE (ON/OFF)

OTHER INFORMATION SHOULD BE AVAILABLE BUT NOT CONTINUOSLY DISPLAYED.IT SHOULD BE EASILY FETCHED AND DISPLAYED UPON SIMPLE CONSOLE COMMAND.

EXAMPLE:

UBR,EBR,CURRENT AC BLOCK,PREVIOUS AC BLOCK

FLAGS:OV,CR0,CR1,FOV,FPD,UIOT,ETC,(MONITOR FLAGS):PCU,PCS,PAGE FAIL WORD,

2.13 KLINIK

SEE DOLPHIN FIELD SERVICE MAINTENANCE PLAN, AUTHOR: MIKE ROBEY.

2.14 MONITOR/CONSOLE PROTOCOL

REFERENCE MONITIOR/CONSOLE PROTOCOL ,AUTHOR:JIM JONES

3.0 PERFORMANCE AND GOALS

3.1 PERFORMANCE

3.2 CONSOLE GOALS

1. MEET SYSTEM RAMP GOALS
2. PROVIDE COST EFFECTIVE CONSOLE WITHOUT SACRIFICING RAMP
3. UNUSED
4. MEET VAX COMPATIBILITY GOALS
5. PROVIDE PACKAGEING ,POWER ,FUNCTIONALITY IMPROVEMENTS OVER PREVIOUS CONSOLES
6. UTILIZE NEW CORPORATE INTELLIGENT TERMINAL SERIES (PDT11).
7. PROVIDE PRIMARY SYSTEM BOOT VIA CONSOLE ROM
8. PROVIDE MULTIPLE SECONDARY LOAD PATH IN CASE OF PRIMARY BOOT FAILURE
9. PROVIDE A METHOD TO RECORD DOLPHIN BUS COMMUNICATIONS
10. PROVIDE SYSTEM TIME OF DAY CLOCK WITH BATTERY BACK UP
11. PROVIDE SYSTEM CLOCK CONTROL AND DISTRIBUTION
12. PROVIDE CONSOLE WITH ABILITY TO COMMUNICATE WITH ANY DEVICE ON THE BUS

13. PROVIDE SOUND MECHANICAL DESIGN

14. PROVIDE SOFTWARE POWER FAIL RELOAD/RESTART OF THE OPERATING SYSTEM

15. PROVIDE PHYSICAL BOOT BUTTON(S) FOR SYSTEM LOAD

16. KLINIK INTERFACE TO BE COMPATABLE TO U.S. AND EUROPEAN MARKETS, IF POSSIBLE.

3.3 PACKAGING

THE PDT100 WILL BE PACKAGED IN THE STANDARD VT100 ENCLOSURE. TRANSITION CONNECTORS AND A RUGGEDIZED CABLE WILL BE REQUIRED TO INTERFACE TO THE DOLPHIN ENCLOSURE.THE TWO EXTENDED HEX MODULES WILL RESIDE IN THE DOLPHIN ENCLOSURE.THE BUS WILL BE ROUTED FROM THE TRANSITION PANELS TO THE MODULES EITHER THRU BACKPLANE INTERCONNECTIONS OR A CONNECTOR ON THE BOARDS.THE BACKPANEL WILL PROVIDE MEANS FOR THE SYSTEM CLOCK,DIAGNOSTIC CLOCK/DATA, DOLPHIN BUS INTERCONNECTIONS.THE TOTAL FINGER PINS AVAILABLE MAY PRECLUDE UNIBUS INTERCONNECT THRU THE BACKPLANE.

THE AMOUNT OF CONSOLE HEX MODULES (GOAL) IS TWO (2).THIS STRATEGY MAY CHANGE TO 3 HEX MODULES IF THE INTERCONNETIONS VIA THE BACKPLANE BECOME GREATER THAN WHAT TWO BOARDS CAN PROVIDE.THE BOARD STRATEGY IS TO LOCATE ALL MCA'S ON ONE EXTENDED HEX MODULE AND THE BALANCE OF THE LOGIC (TTL,10K ECL) ON TWO EXTENDED MODULES.THE SPACING OF THE MCA BOARDS WILL ALLOW SPACING OF TWO NON-MCA BOARDS IN THE SAME AMOUNT OF SPACE THAT A SECOND MCA BOARD WOULD OCCUPY.THIS WOULD PROVIDE AN ADDITIONAL BOARDS WORTH OF BACKPLANE PINS TO CONNECT TO. ACTUAL CONNECTION TO THE BACKPLANE FOR THE EXTRA BOARD MAY NOT BE NECESSARY IF THE BOARD SPACING WERE USED FOR A MOTHER/DAUGHTER EXTENDED HEX MODULE COMBINATION. IT MAY BE POSSIBLE TO HAVE FINGER PIN CONNECTION TO ONLY ONE OPTION SLOT AND USE STACKING CONNECTOR TECHNIQUES TO PROVIDE 1 MOTHER BOARD AND TWO DAUGHTER BOARDS COMBINATION.

3.4 COSTS

THE COST ESTIMATE OF THE CONSOLE IS DERIVED IN THE FOLLING MANNER:

VT100 + (1) TOBY INTELLIGENCE MODULE COST= $1.2K
(THE ESTIMATED TRANSFER COST OF THE VT100 IS .8K AND
THE ESTIMATED TRANSFER COST OF THE TOBY BOARD IS .4K)

EXTENDED HEX MODULES (2) $1.0K EACH = $2.0K
(BOARD COST ESTIMATE YET TO BE DONE)

INCIDENTAL HARDWARE (RUGGEDIZED BUS,TRANSITION

PANELS ETC) = $.1K

TOTAL ESTIMATED COST FOR THE DOLPHIN CONSOLE = $3.3K

3.5 TECHNOLOGY

THE CONSOLE IS BUILT OUT OF MANY TECHNOLOGIES,MACRO CELL ARRAY, ECL,TTL,OP-AMPS AND DISCRETE COMPONENTS ARE USED,NO SPECIAL LSI COMPONENTS ARE USED,THE HIGH SPEED FUJITSU 256 X 4 BIT 10 NS RAM ARE USED FOR THE BUS RECORDER OR EQUIVALENT.

MULTILAYER EXTENDED 4 OR 6 LAYER HEX MODULES WILL BE USED FOR CONSOLE P.C. LAYOUT,THE PROTOTYPE CONSOLE SYSTEM INTERFACE (CSI) WILL BE MULTIWIRE EXTENDED HEX MODULE.

THE CONSOLE LOGIC WHICH RESIDES IN THE DOLPHIN ENCLOSURE WILL FIT ON TWO OR THREE EXTENDED HEX MODULES.

THE CONSOLE PROCESSOR WILL UTILIZE THE PDT/TOBY MICROSYSTEM. IT FEATURES 1134A MINICOMPUTER SPEED AND FUNCTIONS AT MICROCOMPUTER COSTS.

3.6 CONFIGURATIONS

SEE APPENDIX A

3.7 RAMP

3.7.1 RELIABILITY

3.7.1.1 MTBF

THE MTBF GOAL FOR THE CONSOLE WILL BE BROKEN INTO TWO SECTIONS, THE PDT11 MTBF GOAL AND THE CONSOLE HEX MODULE GOAL.THE MTBF GOAL FOR THE PDT11 WILL BE ESTABLISHED BY THE SMALL SYSTEMS GROUP IN MAYNARD,THE MTBF GOAL FOR THE HEX MODULES SHALL BE AT LEAST 20000 HOURS. THE MTBF OF THE PDT11 AND THE HEX MODULES WILL BE NOT LESS THAN 5000 HOURS.THESE GOALS WILL BE CONTINUALLY BE UPDATED AS MTBF DATA BECOMES AVAILABLE FOR THE COMPONENTS USED (E.G. THE MCA'S,10NS RAMS ETC).

BECAUSE THE PDT11 INCLUDES AN ELECTROMECHNICAL DEVICE THE PDT11 MTBF MAY BE FURTHER BROKEN DOWN TO PROVIDE PURE ELECTRONICS MTBF AND ELECTROMECHANICAL MTBF. THE STATED

GOALS (ABOVE) DO NOT INCLUDE ELECTROMECHANICAL DEVICES.

3.7.1.2 MTTR

THE MTTR GOAL FOR THE CONSOLE WILL BE 2 HOURS.THE ASSUMPTIONS MADE ARE THE PDT100 WILL BE REPLACABLE WITHOUT DISRUPTION TO THE DOLPHIN MONITOR OPERATION.REPLACEMENT OF THE HEX MODULES ASSUMES THAT THE DOLPHIN SYSTEM MUST BE TAKEN STAND ALONE.THE REPAIR METHOD FOR THE CONSOLE ASSUMES THE PDT100 AND THE HEX MODULES ARE FIELD REPLACABLE UNITS(FRU). WITH SPARES AVAILABLE AT THE SITE THE MTTR GOAL CAN BE MET. THE ASSUMPTION MADE IS THAT THE SPARES ARE AVAILABLE AT THE SITE.

3.7.1.3 MTTD

THE MTTD GOALS FOR THE CONSOLE WILL BE 45 MINUTES OR LESS. THIS FIGURE WILL INCLUDE DIAGNOSIS OF THE PDT100 AND THE LOGIC RESIDING IN THE DOLPHIN ENCLOSURE. QUICK VERIFY DIAGNOSTICS WILL IDENTIFY TO THE BOARD OR TERMINAL, WHAT FIELD REPLACABLE UNIT IS BAD.THE MAIN DIAGNOSTICS FOR THE CONSOLE WILL RESIDE ON CASSETTES AND LOADING OF THESE DIAGNOSTICS AND RUN TIME FOR A COMPLETE CONSOLE DIAGNOSTIC PASS SHALL MEET THE SPECIFIED LIMIT (45 MINUTES).TO MEET THESE GOALS IT IS NOT ENVISIONED THAT THE DIAGNOSTICS MAKE COMPLETE AND EXHAUSTIVE CHECKS ON THE CONSOLE BUT IT ONLY EMPLOY A CHECKING TECHNIQUE THAT VERIFYS THE MIMIMAL LOGIC TO DIAGNOSE THE REST OF THE DOLPHIN SYSTEM. IF THE CONSOLE APPEARS TO BE FUNCTIONAL THE EXHAUSTIVE TESTING OF THE CONSOLE WILL BE DONE AFTER THE SYSTEM HAS COME BACK UP FROM ITS FAILURE.IF THE CONSOLE ITSELF IS THE FAILING DEVICE THEN THE MTTD OF THE CONSOLE WILL BE 45 MINUTES WHICH INCLUDES AT LEAST ONE PASS OF ALL CONSOLE DIAGNOSTICS, INCLUDING THE MEMORY TESTS.

3.7.2 AVAILABILITY

TO BE DEFINED

3.7.3 MAINTAINABILITY

TO BE DEFINED

3.7.4 PRODUCIBILITY

TO BE DEFINED

4.0 DEVELOPMENT

4.1 DEVELOPERS

THE CONSOLE DEVELOPMENT PERSONNEL ARE:

DOLPHIN CONSOLE PROJECT ENGINEER: STEVE HOLMES

DOLPHIN CONSOLE CSI DESIGNER: STEVE HOLMES

DOLPHIN CONSOLE PWR CONTROL LOGIC: DENNIS LITWINETZ

DOLPHIN CONSOLE ENV ANALOG DESIGNER: JOHN KELLY

DOLPHIN CONSOLE PWR CONTROL ANALOG DESIGNER: CHUCK BUTALA

DOLPHIN CONSOLE DIAG ENG SUPERVISOR: JIM JONES

DOLPHIN CONSOLE PDT11/TOBY DESIGN LIASON: PAUL KELLY

DOLPHIN CONSOLE CLOCK CONTROL & DIST DESIGNER: B. BRUCKERT/D. LITWINETZ

DOLPHIN CONSOLE BACKPLANE DESIGNER: J. HACKENBERG/J. TOURTELLOTT

4.2 SCHEDULE

SEE APPENDIX B

5.0 RISKS

THE RISKS ASSOCIATED WITH THE CONSOLE PROJECT ARE:

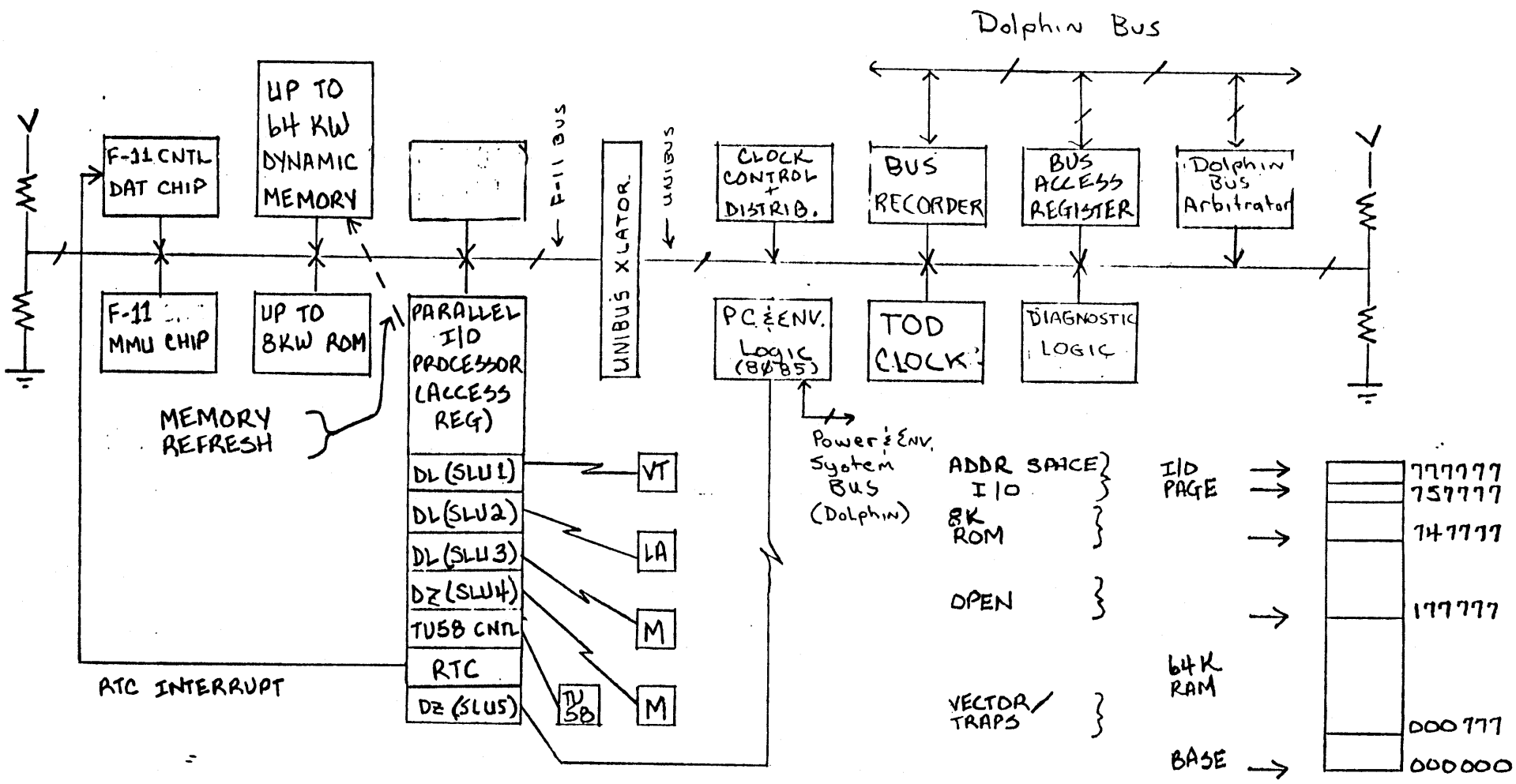
- THE SMALL SYSTEMS GROUP EMPLOYS ALL DESIGN ENHANCEMENTS ON PDT11/TOBY FOR DOLPHIN CONSOLE DESIGN GOALS.
- TOBY PROJECT IS FUNDED PROPERLY
- TOBY SCHEDULES ARE MET
- IIL DESIGN MEETS DIAGNOSTIC GOALS
- MULTIPLE CONSOLE DEVELOPER SCHEDULES ARE MET

6.0 APLICABLE DOCUMENTS

TOBY SPECIFICATION REV.2
MICROCOMPUTER HANDBOOK
F-11 CHIP SPECIFICATIONS(DAT,CNTL,MMU)

6120 SPECIFICATION
DOLPHIN BUS SPECIFICATION
" MCA "
" RAMP "
" POWER SUPPLY SPECIFICATION
MONITOR/CONSOLE PROTOCOL
UNIBUS SPECIFICATION
DOLPHIN FIELD SERVICE MAINTENANCE PLAN

CONSOLE MICRO SYSTEM
BLOCK DIAGRAM



F-11 MEMORY MAP

Appendix A

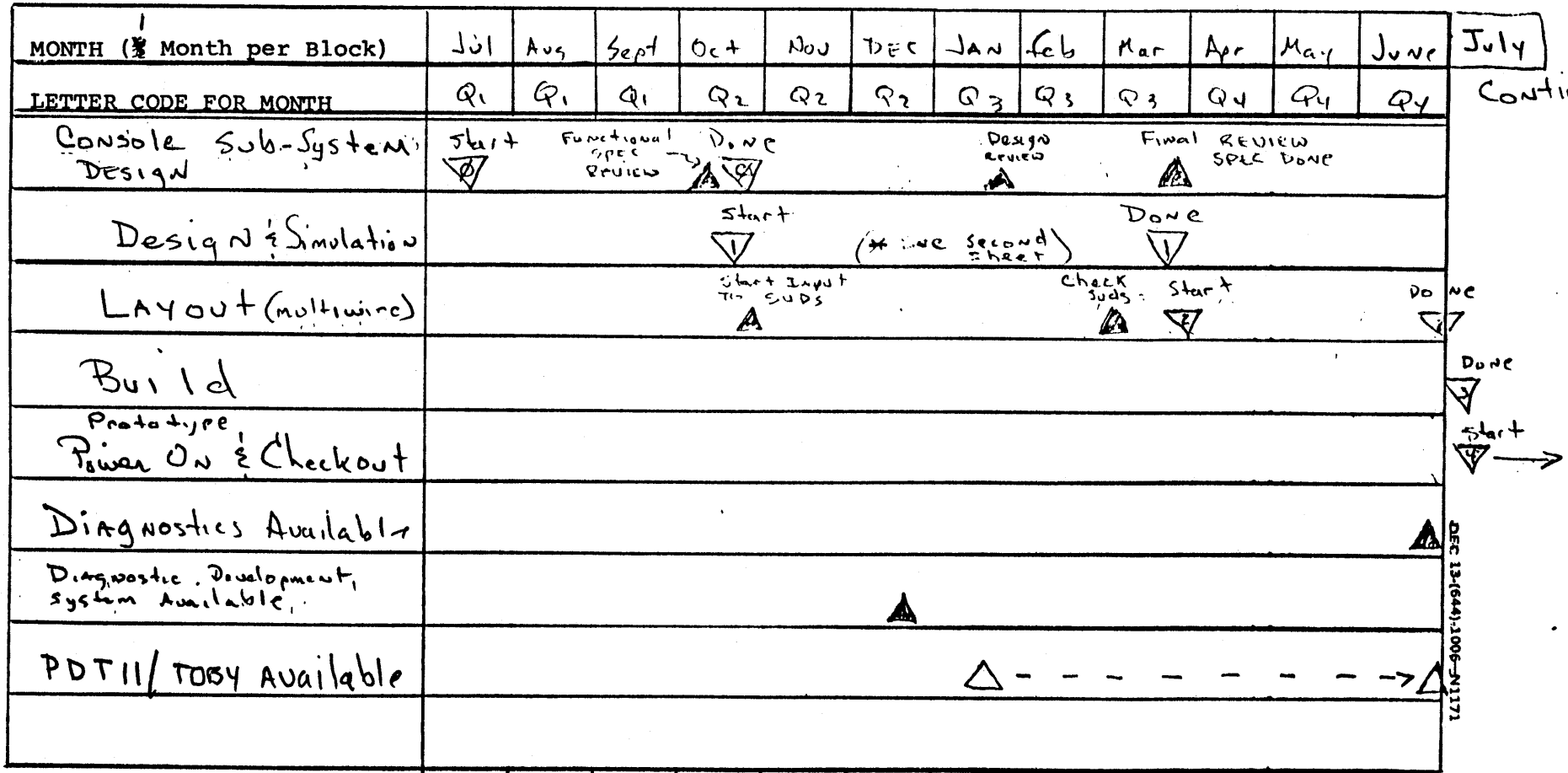
S. HOLMES

26-JUL-78 REV.Ø
28-Sept-78 REV.1

PROJECT SCHEDULE

PROJECT(S) Dolphin Console (1 of 2 sheets) BY Steve Holmes

SHORT DESCRIPTION Provide Dolphin Console Subsystem DATE 9-12-78



*If "Test" ends with Accumulated Errors that require rework, appropriate design steps such as re-design, relayout, etc. should be inserted until it is expected that "test" will terminate with Limited Release.