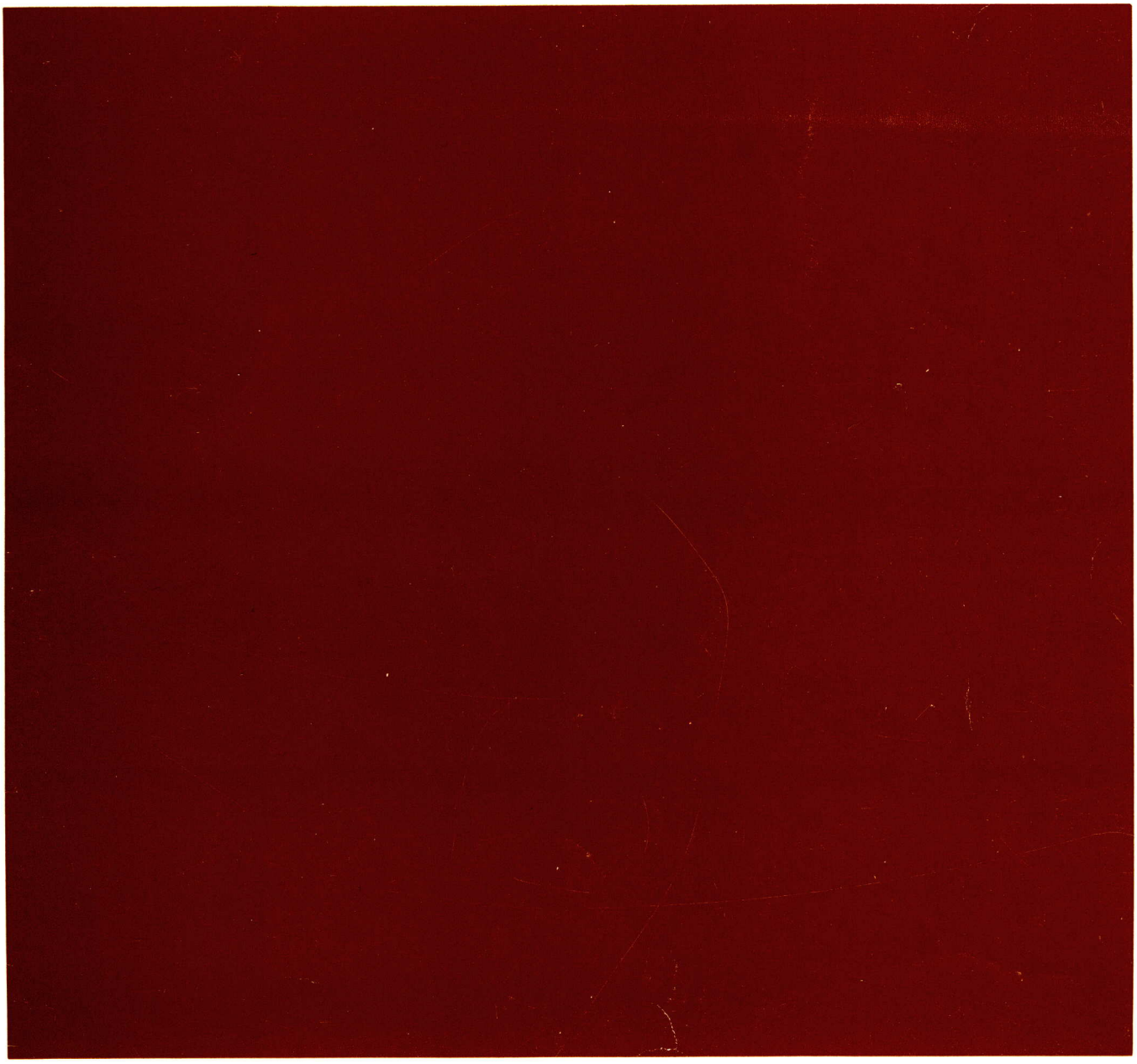
Digital Equipment Corporation
Marlboro, Massachusetts

digital

PCL20
Parallel Communications Link
User's Guide



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PCL20
Parallel Communications Link
User's Guide

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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

This chapter provides an overview of the PCL20 communications system. Included are a block diagram description, specifications, physical description, and references to related documents.

The PCL20 is a time-division, multiplexed, parallel communications link that allows up to 16 DECSYSTEM-2020s and/or PDP-11s to be connected together on one TDM bus. Up to four TDM busses may be attached to a DECSYSTEM-2020 through a separate interface, allowing a maximum of 64 DECSYSTEM-2020s and/or PDP-11s to communicate with each other. (See Figure 1-1.)

The PCL20 provides mounting space for a PCL11-B parallel communications link interface, a BA11-K mounting box, and a Unibus adapter. The PCL11-B is housed in a BA11-K box mounted in the DNHXX-A expansion cabinet (a prerequisite for implementing the PCL20). The Unibus adapter interfaces the PCL11-B to the DECSYSTEM-2020, and is installed in the fourth UBA slot. Individual systems may be connected or disconnected from the bus for maintenance purposes without affecting the other systems.

1.2 BLOCK DIAGRAM DESCRIPTION

The PCL11-B is composed of three functional areas: transmitter, receiver, and master section. (See Figure 1-2.) Since the PCL11-B is a Unibus peripheral, all data and controls are derived from the Unibus through the Unibus adapter. At the TDM bus side of the PCL11-B, each communications system is independent.

Data to be sent from one DECSYSTEM-2020 to another is loaded into the data silo by the load silo control. The data silo may be loaded in either of two ways. A DMA transfer may occur by an NPR request for the Unibus to transfer a block of data directly from memory whenever there is space in the silo for the next word of the block. Also, the load silo control can respond as a Unibus slave, moving data directly to the silo, which appears as a register on the Unibus.

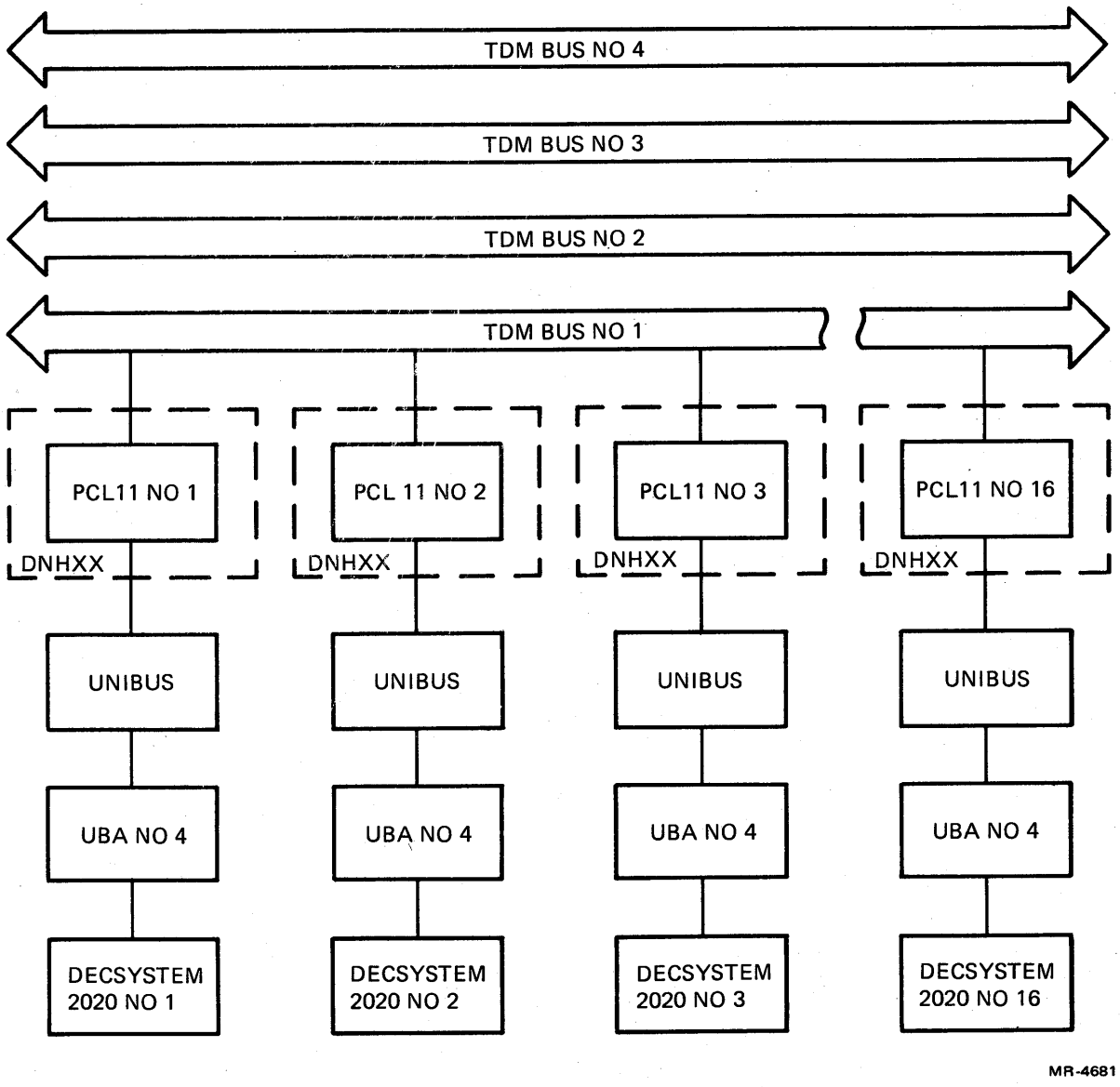

Figure 1-1 System Block Diagram

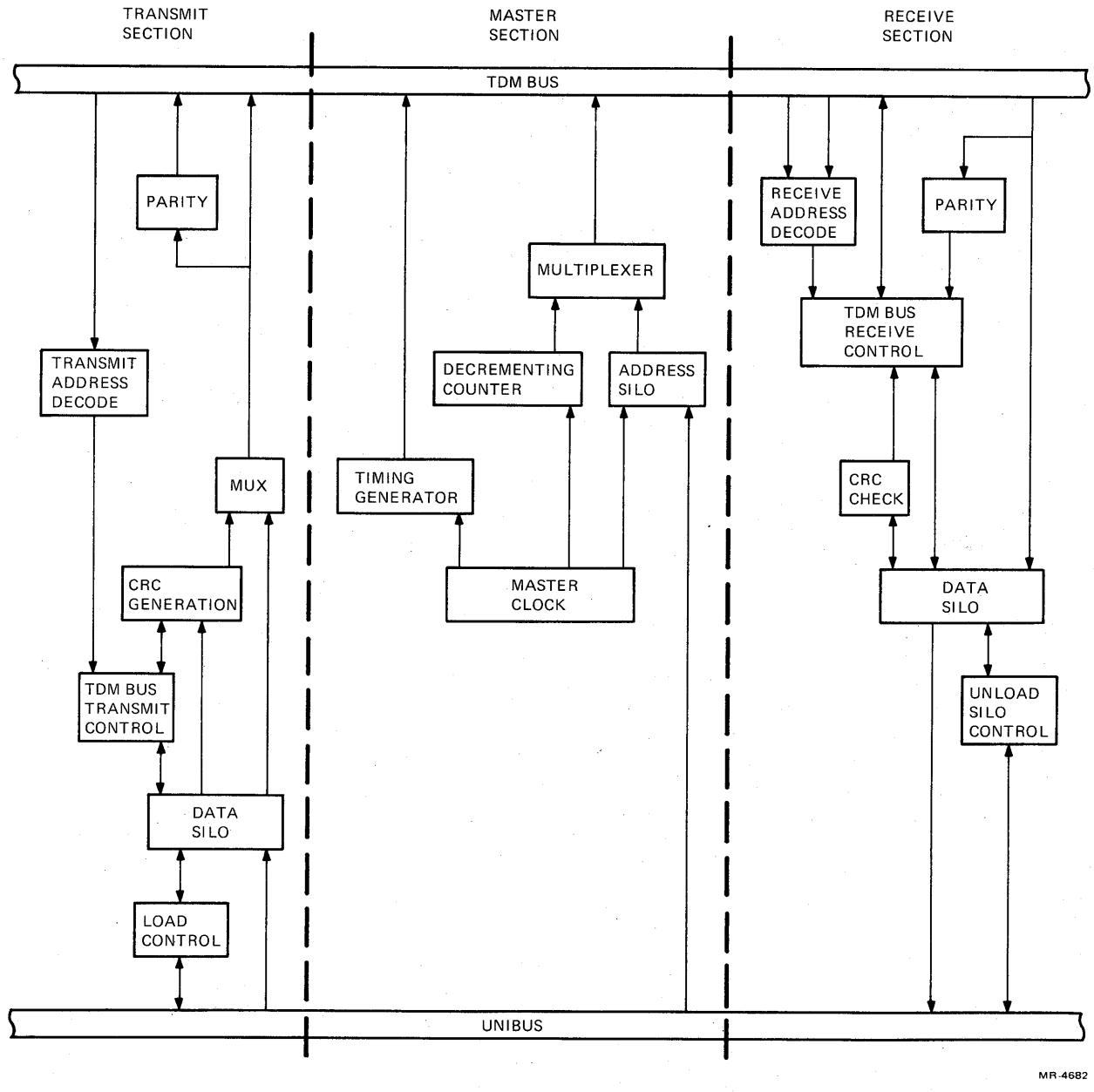

Figure 1-2 PCL11-B Block Diagram

The TDM bus transmit control logic controls the transfer of data from the silo to the remote receiver over the TDM bus. When the transmitter address decode logic signals the transmit control logic that its timeslice has occurred, the control logic determines the correct time to drive the TDM bus with the signals required for the transfer. The transmit control logic generates the address of the remote receiver, and two response signals. The response signals tell the receiver what will occur during the timeslice. The transmit control logic also multiplexes the data lines with the silo or CRC character.

The CRC generation logic calculates a CRC-16 character for transmitted data. This logic includes a counter that keeps track of the number of words transmitted. After each 200_8 (128_{10}) words, the CRC character is sent during the next timeslice.

The parity generation logic generates a parity bit for each 16-bit word transmitted, including the CRC character.

The receive logic functions in the same way as the transmitter, except in the reverse direction. The data silo is loaded with data received from a remote transmitter over the TDM bus. Data is transferred from the silo to the Unibus either by NPR requests when the data is ready, or by READ I/O instructions received from the computer.

The TDM bus receive control logic controls the reception of data and the loading of data into the receive data silo.

The receiver address decode logic determines when the receiver is being addressed, and whether a channel is open to a particular transmitter. The time phase signals determine when data is removed from the TDM bus and loaded into the receive data silo. The receiver address decode logic asserts four lines on the TDM bus. These lines indicate to the transmitter what was done by the receiver during the timeslice.

The CRC and parity logic check data when it arrives at the receiver. If an error is detected, one of the response lines indicates an error condition to the transmitter.

The master section controls all TDM bus transactions by time phase signals and transmitter address signals. The time phase signals are square waves 90° out of phase. The transmitter address signals are generated in either of two ways. The first method involves a decrementing counter, which puts out all addresses sequentially on the TDM bus, from the highest to the lowest. The alternate method employs an address silo, which is loaded by software. The silo circulates addresses on the TDM bus, allowing a particular transmitter to be assigned more or less of the available bus bandwidth. The master clock generates the timing to run all sections of the master.

1.3 SPECIFICATIONS

System Characteristics:

TDM bus protocol	Time-division multiplexing.
Message type	Parallel 16-bit words are transferred.
Error detection	Odd parity accompanies every word. A CRC-16 check character is sent after each block or at the end of the message.
Maximum bus length	90 meters (300 feet).
Bus levels	Differential tri-state bus (0-5 volts).
Common mode	No common mode voltage is acceptable between any two units.
Data transfer rate	The bus bandwidth depends on the TDM bus length. The portion of bandwidth assignable to any unit depends on the total number of units in the system. The chart below shows the allocation of bandwidth for networks of various sizes. These allocations may be changed dynamically by the master using the address silo.

Total TDM Bus Lengths (less than)	50 ft	100 ft	240 ft	300 ft
TDM Bus Bandwidth (in K bytes)	1000	800	500	400
1 unit	500	400	250	200
2 units	500	400	250	200
8 units	125	100	62	50
16 units	62	50	31	25

PCL20 Interface Characteristics:

Prerequisites

DNHXX to contain the PCL20

NOTE

The PCL11-B requires space for a double-system unit backplane in a PCL20 mounting box.

Mechanical

Modules		The PCL11-B contains seven hex modules and one quad module.
Cables		Each PCL11-B is shipped with one BC20K cable. BC20P-xx cables may be required to connect the PCL11-B units to each other. Unibus cables are provided with the PCL20.
Configurations:	PCL20 AA/AB:	BA11-K, M8619 UBA module, and Unibus cable.
	PCL20 AC/AD:	BA11-K and Unibus cable.

Electrical

Power requirements

PCL20-AA	115 Vac	60 Hz	5 A
PCL20-AB	230 Vac	50 Hz	2.5 A
PCL20-AC	115 Vac	60 Hz	5 A
PCL20-AD	230 Vac	50 Hz	2.5 A

Logic levels — All levels in the PCL11-B are TTL.

1.4 PHYSICAL DESCRIPTION

The PCL20 consists of a Unibus adapter (UBA), which is plugged into the fourth UBA slot of the 2020, and a BA11-K box to mount PCL11-B logic.

The PCL11-B consists of a backplane (a double-system unit), seven hex modules (M7991 through M7997) and one quad module (M8003). The backplane must be mounted in a PCL20 mounting box and supplied with the correct power. Unibus connections must be made with the proper cables or M920 modules. The PCL11-B is shipped with one M920. Also included is one terminator (H3370) for the TDM bus, as well as a short section of TDM bus cable (BC20K) to connect the PCL11-B to the TDM bus.

1.5 RELATED DOCUMENTS

Title	Document No.
PCL11-B Parallel Communication Link Differential TDM Bus	YC-A20TC-00
PCL11 Communications Systems General Introduction and Configuration Guide	YC-A20TC-01
PCL11-B Communications System Installation and Maintenance Guide	YC-A20TC-02
Parallel Communication Link Field Maintenance Print Set	PCL11-00
PDP-11 Peripherals Handbook	EB-07667-20

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The following provides all the information required to install the PCL20. The two variations of the procedure are determined by whether the installation is an add-on to an existing system, or a new installation.

2.2 SITE CONSIDERATIONS AND PREPARATION

A physical layout and schematic diagram of the power distribution and grounding is a prerequisite for installation. Each PCL20 must be included in the original DECSYSTEM-2020 configuration, or the system must be reconfigured to include add-on PCL20s.

After the system has been configured, a chart should be drawn showing the location of each cabinet in the system. Each cabinet that contains a PCL20 should be identified, and its source of ac power determined. If possible, each PCL20 in the system should be powered from the same phase of the power distribution panel. If any PCL20s are to be located in different cabinets, a cable tray or alternate route must be employed. The cables should not be routed near structural building metal such as beams or pipes, or electrically noisy devices such as arc welders or electromechanical machinery. If the TDM bus is to be routed inside a cabinet, ensure that there is a suitable path for the cable so that it will not be damaged when the PCL20 is slid in or out of the mounting box.

Figure 2-1 is a model configuration chart users can reproduce in planning their particular installations. Using the site diagram, determine the distance the TDM bus cables must travel between all mounting boxes that contain a PCL20. Ensure that enough length is included to allow for the height of the box in the cabinet, plus four feet to allow the box to be pulled out of the cabinet without disconnecting the TDM bus. If the PCL20s are within ten feet of each other, the cable is not required. Complete the configuration chart as follows: Starting at one end of the bus, assign unique TDM bus addresses to each PCL20 in the system; connect each unit on the chart with a line and above the line write the cable length required to join the units. The cable required is BC20P-xx, which is available in lengths of 10, 25, 50, and 100 feet. The total bus length cannot exceed 300 feet.

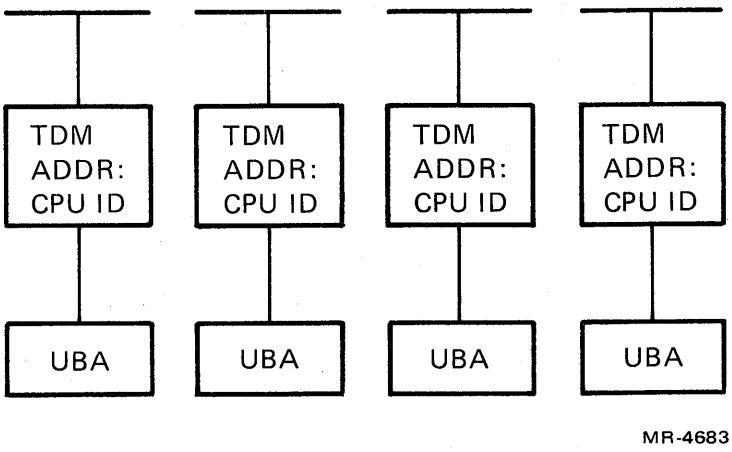

Figure 2-1 Configuration Chart

2.3 NEW INSTALLATIONS

The following procedure must be followed when installing new PCL20 systems.

1. Place the PCL20/DNHXX cabinet next to the DECSYSTEM-2020 CPU cabinet and bolt the cabinets together.

2. Install the UBA module in CPU backplane slot 15 (fourth UBA slot). Cable the UBA to the first PCL20/PCL11-B logic using the cable supplied. (Refer to the PCL20 Field Maintenance Print Set for details.)

3. Ensure that all PCL11-B units have successfully passed the checkout procedure outlined in Paragraph 2.7. Refer to the PCL11-B Option Description (YC-A20TC-00) if nonstandard addressing is to be used for switch setting information.

4. Begin with the PCL11-B next to the terminator. Ensure that the address switches on M7991 and M7997 have been configured correctly for the TDM bus address of the unit. The configuration chart should show the TDM bus address. The address switches have their most significant bit on the left; turn the switch off for a one. Write the TDM bus address of the unit on all six labels of the BC20K and plug one end of the cable into the TDM bus terminator (H3370). One control cable (orange label), and one data cable (blue label) should be plugged into the H3370.

5. Temporarily plug another H3370 into the free end of the BC20X.

6. Load the PCL20 exerciser (Maindec-10-DSPCB under DSMON) into the DECSYSTEM-2020 this PCL11-B is attached to. Refer to the listing for complete instructions on the use of this program. Check that the switch on M7994 is set up to the highest address on the TDM bus. (The most significant bit is on the left; turn the switch off for a one.) If future expansion is envisioned for the system, set this switch to the highest address that could ever occur on this TDM bus.

7. Start the exerciser via the DSMON diagnostic monitor. When the prompt is given, type the following.

   ```
   PCL>MASTER SET<CR>
   PCL>
   ```

   This will set this unit as master. Using an oscilloscope, monitor the waveform on F05T2 of the PCL11-B backplane; it should appear as a square wave. Adjust this square wave so that its period is that indicated in Table 2-1 according to the total TDM bus

length. It is recommended that this adjustment be made for possible expansion of the system to greater bus lengths.

Table 2-1 Timeslice Adjustments

TDM Bus Length	50' or less	50'-100'	100'-240'	240'-300'
Set Timing on M7994 to:	2 μs	2.5 μs	4 μs	5 μs

8. Run the exerciser in this unit as follows.

```
PCL>ADD ID1,ID2,...IDn <CR> ; where ID1,ID2,...IDn are
                              receiving node numbers.

PCL>RIB SET <CR>
PCL>GO <CR>

EXERCISER STARTED
```

Go to all other units already installed and type:

```
PCL>GO <CR>
EXERCISER STARTED
```

9. Let the exerciser run a few minutes in all units. Obtain a status and summary of errors by typing the following sequence at all units already installed on the bus.

```
ALT MODE or Control C
PCL>STATUS <CR>
.....Program will respond with status.
PCL>SUMMARY <CR>
.....Program will respond with summary of errors.
PCL>
```

If any errors occur they must be rectified before proceeding.

10. Disconnect the terminator from this unit and clear this unit from being master by typing:

```
PCL>MASTER CLEAR <CR>
PCL>
```

Connect this unit to the next PCL11-B, using BC20P-xx if required. When connecting a BC20P, connect the blue data cables and the orange control cables to each other. On each cable's label, write the TDM bus address to which

the cable connects as well as the TDM bus address to which the other end is connected. If this is the last unit on the bus, connect the BC20K to the end terminator. If the units are within 10 feet of each other, connect the BC20K directly to each unit.

The BC20P-xx cable must be routed with great care between the two units. It should be put in cable trays if the units are in separate cabinets. If the cable must travel within a cabinet, it must be properly tie-wrapped so that it is not pinched or damaged by mounting boxes being opened for maintenance. There must be enough slack left behind the mounting box where the PCL11-B is mounted to allow the box to be opened and closed without breaking the TDM bus connection.

If the units are in separate cabinets, the ground strap provided with the BC20P-xx cable must be connected to the base of both cabinets. This strap must be routed in the same tray as the BC20P-xx but should not be connected too closely to it.

11. Move on to the next unit and repeat steps 4 through 10 for all units in the system.

2.4 ADD-ONS TO EXISTING SYSTEMS

1. Mount an add-on of PCL11-B logic into the space available in the existing PCL20 box in the DNHXX-A cabinet. For an add-on of the mounting box and PCL11-B logic, mount the PCL20 box in the space provided in the DNHXX-A cabinet. (Refer to the PCL20 Field Maintenance Print Set for details.)

2. Ensure that this new unit has successfully passed the checkout procedure. (See Paragraph 2.7.)

3. Run the PCL20 exerciser successfully on both the new and existing units on the DECSYSTEM-2020. Debug any errors before proceeding.

4. Complete a new configuration chart for the revised system.

5. If the new system has no TDM bus addresses higher than the old system, and the bus length has not increased so that the new bus length is in a larger range in Table 2-1, proceed to step 7.

6. Halt the exerciser and turn off power in all units. Complete the following at each PCL11-B unit in the system. Change the switch on the M7994 to reflect the highest address on the bus. (The most significant bit is on the left; turn the switch off for a one.) Turn the unit on and start the exerciser. When given the dollar sign prompt, type:

```
PCL>MASTER SET <CR>
PCL>
```

Adjust the square wave on module M7994 to the correct value indicated in Table 2-1 using the potentiometer on the rear of the M7994. When finished, type:

```
PCL>MASTER CLEAR <CR>
PCL>
```

Move on to the next unit. Repeat this step until all master sections have been upgraded.

7. On the unit to be added, check that the TDM bus address is configured correctly in the switches on M7991 and M7997. (The most significant bit is on the left; turn the switch off for a one.) Ensure that the address on M7994 is set to the highest TDM bus address on the bus. (The most significant bit is on the left; turn the switch off for a one.) Write the TDM address of the unit on the six labels on the BC20K cable. Disconnect the TDM bus where this unit is to be inserted. Change the labels on any BC20P-xx to indicate the new units to which they will be connected. Connect the unit to be added per the revised configuration chart. If a new BC20P is required, write the addresses required on the labels.

The BC20P-xx cable must be routed with great care between the two units. It should be put in cable trays if the units are in separate cabinets. If the cable must travel within a cabinet, it must be properly tie-wrapped so that it is not pinched or damaged by mounting boxes being opened for maintenance. There must be enough slack left behind the mounting box where the PCL11-B is mounted to allow the box to be opened and closed without breaking the TDM bus connection.

If the units are in separate cabinets, the ground strap provided with the BC20P-xx cable must be connected to the base of both cabinets. This strap must be routed in the same tray as the BC20P-xx but should not be connected too closely to it.

8. Load the exerciser into the unit added to the system. Start the exerciser via DSMON and set master by typing the following.

```
PCL>MASTER SET <CR>
PCL>
```

Connect an oscilloscope to F05T2 of the PCL11-B backplane and observe the period of the square wave. Adjust this to the proper value indicated in Table 2-1, using the potentiometer on M7994.

9. Set up this unit to talk to all other units in the system by typing the following on all units on the bus.

```
PCL>ADD ID1,ID2,...IDn <CR> ; where ID1,ID2,...IDn are
                              receiving node numbers.
PCL>RIB SET <CR>
PCL>GO <CR.

EXERCISER STARTED
```

10. Obtain status and summary reports as follows.

```
CNTRL C
PCL>STATUS <CR>
.....Program will respond with status.
PCL>SUMMARY <CR>
.....Program will respond with summary of errors
          and statistics.
PCL>
```

2.5 CABLING

The TDM bus is implemented by two cable kits. These are the BC20K, which connects to the PCL11-B, and the BC20P, which is used to extend the bus to interconnect additional PCL11-Bs. Each BC20-K cable kit includes two cables, one labeled in blue for data and the other labeled in orange for control. The BC20K is a dual "Y" cable. The center of the cable connects to the M8003 cable in the PCL11-B. The other ends of the BC20Ks are connected to the BC20Ps to extend the TDM bus. This allows the PCL11-B to be connected to the TDM bus in a "T" so that it may be disconnected without breaking the connection between other PCL11-Bs on the TDM bus. The BC20-P cable kits include a ground strap to interconnect separate cabinets.

2.6 GROUNDING

A good grounding system is essential for reliable operation of the PCL11-B. The allowable common mode voltage between the various cabinets in the system is zero. The ground strap supplied with the BC20-P cable ensures that the separate cabinets remain at the

same potential. If two PCL11-Bs are mounted in the same cabinet, the ground strap is not required. If the units are in separate cabinets, it is essential that the cabinets be grounded together at the base. Scrape away any paint at the point of contact to ensure a low resistance connection.

In addition to providing a signal ground reference, this strap is part of the safety grounding system of the computer. The ground bus should be connected to an earth ground at one point. To minimize danger during electrical storms, do not connect the ground bus to building beams, pipes, or other conductors to earth. Before connecting cables together, check that there is not a large potential difference between the two cabinets. This condition creates a potential shock hazard and should be corrected before the cabinets are strapped together.

2.7 CHECKOUT PROCEDURE

1. Standalone Test

   The following procedure should be followed to determine if a PCL20/PCL11-B meets its operating requirements.

   a. Ensure that the switch on M8003 is turned off (i.e., it must point away from the cable connectors).

   b. Load the PCL20 standalone test (Maindec-10-DSPCA under DSMON). Verify that the timeslice adjustment on pin F05T2 concurs with that in Table 2-1. (Use an oscilloscope and the TP0 select test in the basic diagnostic program.) Enter all required information and when asked to select test, run "ALL".

   c. Let the test run for a minimum of 100 passes without error.

   d. Load and start the PCL20 exerciser (Maindec-10-DSPCB via DSMON). Set master (type MASTER SET <CR>), set RIB (type RIB SET <CR>), and add the receiver address. Let run for five minutes and check to ensure that there are no errors.

   e. After this has been accomplished, the PCL20 is operating successfully as a DECSYSTEM-20 peripheral. The PCL20 must still be checked out as part of a communications system.

2. System Test

   a. Ensure that all PCL11-B units have passed the checkout procedure as outlined in the standalone test above.

b. Load the PCL20 exerciser into all units in the system.

c. Start the exerciser in all units. Enter the following sequence of commands in all units.

```
PCL>ADD ID1,ID2,...IDn <CR> ; where ID1,ID2,...IDn
                              are receiving node
                              numbers.
PCL>RIB SET <CR>
PCL>
```

This will ready all units in the system to talk to each other.

d. Go to the first unit on the bus. Type the following sequence to set this unit as master.

```
PCL>MASTER SET <CR>
PCL>
```

e. Go to all the remaining units and type the following to start them up.

```
PCL>GO <CR>
EXERCISER STARTED
```

Wait five minutes and then type on all units:

```
ALT MODE
PCL>STATUS <CR>
.............Computer will respond with status.
PCL>SUMMARY <CR>
.............Computer will respond with summary of
  all errors.
PCL>
```

Ensure that all units have been talked to successfully by every PCL11-B in the system. Ensure that there are no errors.

f. Return to the unit that is master. Type the following on its console.

```
PCL>SILO n..... m <CR> ;n is the lowest address
                       ;m is the highest address
PCL>
```

Repeat step e.

g. Repeat steps d through f using the unit most likely to become master. However, run the system for one hour before obtaining status and summary reports. When the status is obtained, the system meets its operating requirements if:

(1) at least 80 successful completions have occurred for every 100 attempts.

(2) no more than one error has occurred for every 100 successful completions with any unit.

(3) no hard errors occur. (Allow the occasional soft errors that may occur.)

2.8 CUSTOMER ACCEPTANCE TEST

The purpose of this test is to demonstrate proper operation and functioning of a DECSYSTEM-2020 participating in a locally linked network with other DECSYSTEM-2020s and/or PDP-11 systems using the PCL11-B parallel communications link. This acceptance test is designed to demonstrate the following.

- Standalone diagnostic capability to support the PCL11-B on the DECSYSTEM-2020
- Network exerciser diagnostics to run on the DECSYSTEM-2020 compatible with the other PCL11-B network exerciser diagnostic
- Integration and testing of network functions as a system

2.8.1 Test Environment

1. A minimum of two computer systems is needed for the test:

   a. One DECSYSTEM-2020 (with 256K words of memory) to be tested with a PCL20 installed on a third UBA.

   b. Another DECSYSTEM-2020 with a PCL20 option or a PDP-11 system (with PCL11-B interfaces) running the PCL11-B exerciser.

2. The PCL20's timeslicing must be adjusted to a setting approximating the total system bus length for the field installation.

3. Sequential round-robin addressing must be used with the PCL11, with the scan limit set to approximate the field installation.

2.8.2 Test Procedure

2.8.2.1 Standalone Diagnostic Test - The following diagnostics must be run for the time periods specified.

Diagnostic	Run time
UBA Diagnostic on the DECSYSTEM-2020	1/2 hour
PCL20 Standalone Test (DSPCA) on the DECSYSTEM-2020	1/2 hour

Both tests must be completed without error.

2.8.2.2 Exerciser Test (EXEC Mode) - The exerciser diagnostic is configured to run the network with the DECSYSTEM-2020 in EXEC mode. (This test uses the DECSYSTEM-2020 exerciser diagnostic without the operating system.) The following diagnostics must be run for the time limit specified.

Diagnostic	Run time
PCL20 Exerciser (DSPCB) on at least two DECSYSTEM-2020s	1 hour
or	
PCL11-B Exerciser (CZPLAA0) (if a PDP-11 is to be used for the other system in the test)	1 hour

The exercisers should run on both CPUs simultaneously with no hard errors. Allow the occasional soft errors that may occur.

CHAPTER 3
OPERATION AND PROGRAMMING

3.1 INTRODUCTION

This chapter contains operation and programming information for the PCL20 subsystem (PCL11-B and the Unibus adapter (UBA)) on the DECSYSTEM-2020. Included are bit assignments for all registers and a description of the KS10 instructions used for I/O transfers.

3.2 PCL11-B PARALLEL COMMUNICATIONS LINK

3.2.1 Input/Output Coding

The following details the bit assignments for and describes all of the registers in the PCL11-B. There are seven registers associated with the transmitter and six with the receiver. These are described in Figures 3-1 through 3-7 and Tables 3-1 through 3-3. One of these, the TMMR, contains bits that control the master section. This means the master section, conceptually, is part of the transmitter logic; although, in fact, it is an independent section of logic. Default addresses and mnemonics are enclosed in parentheses.

Transmitter Command Register (TCR-764200)

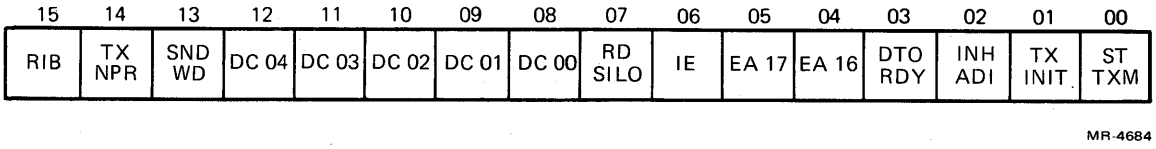

Figure 3-1 TCR Register Format

Table 3-1 TCR Register Bit Descriptions

Bit	Name	Description
0	ST TXM	START TRANSMISSION (R/W) - When set, will cause data and a CRC character to be transmitted to the receiver selected by destination bits (8-12), until the end of message. Cleared by an interrupt request (see bit 6) or TX INIT.
1	TX INIT	TRANSMITTER INITIALIZE (WO) - When set, will initialize all bits in the transmitter. (Their initialized state is indicated for only one instruction time.) Also generated by a BUS INIT or a reset instruction.
2	INH ADI	INHIBIT ADDRESS INCREMENT (R/W) - When set, will inhibit incrementing of the transmitter source bus address (TSBA) register on NPR cycles. Cleared by TX INIT.
3	DT O RDY	DATA OUTPUT READY (RO) - Will be set whenever a word is available to be moved out of the data silo. Used primarily for maintenance. Cleared by TX INIT.
4	EA 16	EXTENDED BUS ADDRESS 16 (R/W) - Together with EA 17 and the TSBA, forms an 18-bit address for NPR cycles. EA 16 and EA 17 will be automatically incremented when the TSBA overflows. Cleared by TX INIT.
5	EA 17	EXTENDED BUS ADDRESS 17 (R/W) - (See bit 4.) Cleared by TX INIT.
6	IE	INTERRUPT ENABLE (R/W) - An interrupt request is made if any of the following bits are set in the TSR: ERR, SUC TXF, SORE, or if RCV BSY is set and RIB is clear. When set, this bit will enable an interrupt request to cause an interrupt if the processor is running on a lower priority than the PCL11-B. Cleared by TX INIT.

Table 3-1 TCR Register Bit Descriptions (Cont)

Bit	Name	Description
7	RD SILO	READ SILO (R/W) - When set, a read of the TSDB or a low byte of the TMMR will remove a word from the data or address silo, respectively. When set, no words may be loaded into either silo. Used primarily for maintenance. Cleared by TX INIT.
8	DC 00	DESTINATION CODE 00 (R/W) - TCR bits 8-12 are loaded with the TDM bus address of the receiver with which communication will take place. (This address must not be zero.) Cleared by TX INIT.
9	DC 01	DESTINATION CODE 01 (R/W) Cleared by TX INIT.
10	DC 02	DESTINATION CODE 02 (R/W) Cleared by TX INIT.
11	DC 03	DESTINATION CODE 03 (R/W) Cleared by TX INIT.
12	DC 04	DESTINATION CODE 04 (R/W) Cleared by TX INIT.
13	SND WD	SEND WORD (R/W) - Must be set to open a channel. When set, will cause one word to be sent to the receiver, if ST TXM is clear. Cleared by an interrupt request (see bit 6) and TX INIT.
14	TX NPR	TRANSMITTER NPR (R/W) - When set, if the TSBC has been loaded with data, will cause hardware to initiate a NPR transfer of one word to the TSDB when the TSDB is ready to accept a word. NPR cycles will continue until the TSBC overflows or an error occurs. No words may be moved into the silo when this bit is set. Cleared by an TSBC overflow and TX INIT.
15	RIB	RETRY IF BUSY (R/W) - When set, will cause hardware to continue trying to open a channel with a receiver, even after receiving a busy response, until a timeout error occurs. Cleared by TX INIT.

Transmitter Status Register (TSR-764202)

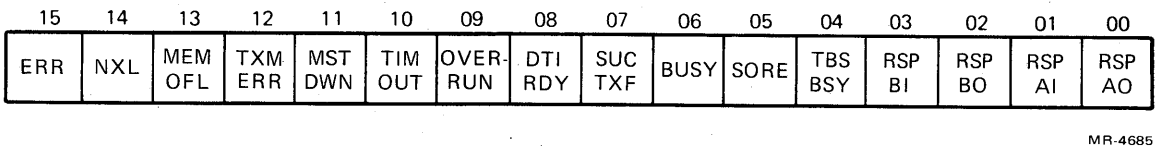

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Figure 3-2 TSR Register Format

Table 3-2 TSR Register Bit Descriptions

Bit	Name	Description
0	RSP A 0	RESPONSE A 0 (RO) - TSR bits 0 and 1 contain the response A generated during the most recent transmitter timeslice. In the event of an error these bits will be frozen in the state at which the error occurred, while in some cases, a 00 response is returned to the receiver. Cleared by TX INIT or SUC TXF.
1	RSP A 1	RESPONSE A 1 (RO) Cleared by TX INIT or SUC TXF. The response A bits accompany every data word sent to the receiver. They indicate to the receiver what the transmitter is sending during the timeslice.

RSP A 1	RSP A 0	
0	0	Transmitter has an error or is off-line
0	1	Null cycle
1	0	Valid word or CRC on data lines
1	1	Last CRC on data lines

2	RSP B 0	RESPONSE B 0 (RO) - TSR bits 2 and 3 contain the response B codes received during the most recent timeslice. These codes will be frozen in the same manner as TSR bits 0 and 1 in the event of an error. Cleared by TX INIT or SUC TXF.
3	RSP B 1	RESPONSE B 1 (RO) Cleared by TX INIT or SUC TXF. The response B bits are returned to the transmitter to indicate what the receiver will be doing with the data during the timeslice.

Table 3-2 TSR Register Bit Descriptions (Cont)

Bit	Name	Description
		RSP B 1 | RSP B 0 | 0 | 0 | Receiver has an error or is off-line 0 | 1 | Null cycle 1 | 0 | Check failure (CRC or parity error has been detected on previous data) 1 | 1 | Acknowledge CRC or data
4	TBS BSY	TDM BUS BUSY (R/W) - This bit will be set if a busy response is received from a receiver while trying to open a channel. Will make an interrupt request only if RIB (TCR bit 15) is clear. Cleared by CHN OPN or TX INIT.
5	SORE	SOFTWARE REJECT (R/W) - This bit will be set if the receiver rejects or truncates a message. If SUC TXF and SORE are set, a truncation has taken place. If SUC TXF is clear and SORE is set, a rejection has taken place. Will cause an interrupt request. Cleared by TX INIT.
6	BUSY	BUSY (RO) - Indicates the transmitter is engaged in a transmission. Will be set if either SND WD or CHN OPN is set. Cleared by TX INIT.
7	SUC TXF	SUCCESSFUL TRANSFER (R/W) - When set, indicates: 1. if SND WD was set and ST TXM was clear, one word has been moved into the receiver data silo. (SUC TXF and BUSY set, SORE clear.) 2. an entire message has been sent, parity and CRC checked, and data moved onto the receiver's Unibus. (SUC TXF set, SORE and BUSY clear.) 3. the message has been truncated, but data transferred has successfully passed CRC and parity checks. (SUC TXF and SORE set, BUSY clear.)
8	DTIRDY	DATA INPUT READY (RO) - When set, indicates a word may be loaded into the TSDB. Set by TX INIT.

Table 3-2 TSR Register Bit Descriptions (Cont)

Bit	Name	Description
9	OVERUN	DATA OVERRUN (R/W) - When set, indicates a data word has been lost in movement into the TSDB before DTIRDY was set. Cleared by TX INIT.
10	TIM OUT	TIME OUT (R/W) - This bit will set if, after SEND WORD is set, more than one timeout period (approximately 2 seconds) passes without a successful transfer of a word. Cleared by TX INIT.
11	MST DWN	MASTER DOWN (R/W) - This bit will set if the transmitter has a word ready to send while the TDM bus master active line is unasserted. Cleared by TX INIT.
12	TXM ERR	TRANSMISSION ERROR (R/W) - When set, indicates an error condition was detected in communicating with a receiver. The type of error can be determined by looking at the RSP B and A bits. 1. CHECK FAIL (parity or CRC error) TSR bit 15 = 1 ERR 12 = TXM ERR 3 = 1 RSP B = 10 2 = 0 RSP A = don't care 2. OFF-LINE (Receiver has gone off-line during a message either due to error or unexpected shutdown). TSR BIT 15 = 1 ERR 12 = 1 TXM ERR 3 = 0 2 = 0 RSP B = 00 RSP A = don't care (This will not cause an error on the first word [only a RCV BUSY] or while closing the channel for a SUC TXF.)

Table 3-2 TSR Register Bit Descriptions (Cont)

Bit	Name	Description
		3. RCV ACCEPTS A NULL TSR BIT 15 = 1 ERR 12 = 1 TSM ERR 3 = 1 RSP B = 11 2 = 1 (acknowledge) 1 = 0 RSP A = 01 0 = 1 (null) 4. RCV DOES NOT ACCEPT FIRST WORD TSR BIT 15 = 1 ERR 12 = 1 TXM ERR 3 = 0 RSP B = 01 2 = 1 (null) 1 = 1 RSP A = 10 0 = 0 Valid Word If RCV is not ready to accept the word, it should return a busy. Cleared by TX INIT.
13	MEMO OFL	MEMORY OVERFLOW (R/W) - When set, indicates TSBA has overflowed and both EA 17 and EA 16 were set. Cleared by TX INIT.
14	NXL	NONEXISTENT LOCATION (RO) - When set, indicates an aborted NPR transfer was made to the address that was contained in the TSBA which does not exist on the Unibus. Cleared by writing a zero into this bit or by TX INIT.
15	ERR	ERROR (RO) - This bit will set whenever any TSR bit 9 through 14 is set. Will make an interrupt request. Cleared by TX INIT.

Transmitter Source Data Buffer (TSDB-764204)
Writing into this register will load a word into the transmitter's data silo. This may be done by NPR transfer or direct moves. If a WRIO is used, the DTIRDY (TSR bit 8) should first be checked before loading this location. Only words may be loaded into this location.

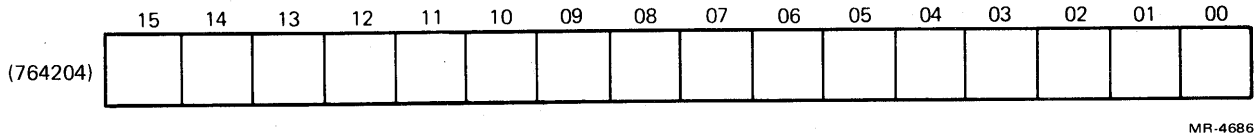


Figure 3-3 TSDB Register Format

For maintenance purposes, the silo may also be read. The data read from this location will be the next word to be removed from the silo. Further, if RD SILO (TCR bit 7) is set, after reading this location the word will be removed from the silo. No writes into this location will be executed while the RD SILO bit is set. Because the TSDB is the output of a 64-word FIFO during reading and the input of the FIFO during writing, instructions that involve a read-restore cycle may not be executed accurately.

Transmitter Source Byte Count (TSBC-764206)
This register is loaded with the 2's complement of the number of bytes in the length of the buffer from which the data is received. This register is incremented after each NPR cycle, or on a WRIO to the TSDB if the NPR bit is not set in the command register.

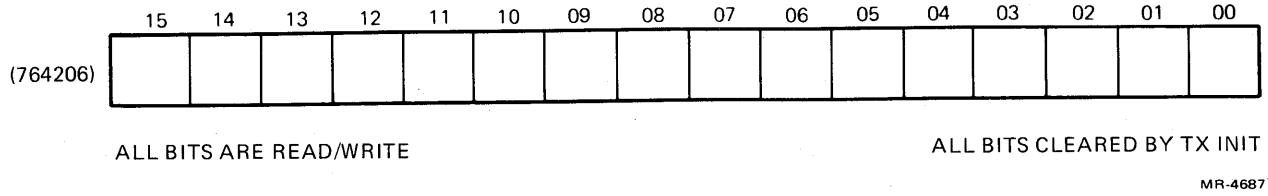


Figure 3-4 TSBC Register Format

Transmitter Source Bus Address (TSBA-764210)
This register is loaded with the address of the first word of the buffer to be transferred to the TSBA. The TSDB will be incremented after each NPR cycle executed, unless INH ADI (TCR bit 2) is set.

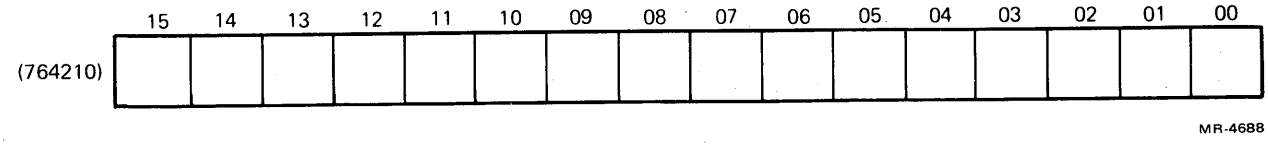


Figure 3-5 TSBA Register Format

Transmitter Master/Maintenance Register (TMMR-764212)
The low byte of the TMMR contains the address silo. Data words are loaded into the silo by the execution of a byte I/O instruction to the low byte. (AIP RDY should be checked before the instruction is actually executed.) The silo is loaded with AUT ADR set and RD SILO clear. This silo must be loaded with at least 20 addresses but not more than 50 addresses.

The silo is used to generate transmitter addresses on the TDM bus that are not necessarily sequential. To implement this, the silo is first loaded with the desired sequence of addresses. Before loading address silo bit 13 of the TMMR, CLR ADR must be asserted. Ensure that the same address does not appear on successive timeslices. When the unit becomes master, AUT ADR is cleared, thus enabling the silo to cycle.

Like the TSDB, the low byte of the TMMR may also be read in a maintenance mode. The word read will be the one appearing on the output of the silo; if RD SILO is set, this word will be removed from the silo after reading. No loads of the silo will be executed with RD SILO set. AUT ADR must also be set to obtain valid data when reading. Because the low byte of the TMMR appears as the output of a 64-word silo during reading and the input of the silo during writing, nonbyte instructions involving a read-restore-write cycle will not be executed accurately. Use byte I/O instructions to set the eight high-order bits of the TMMR.

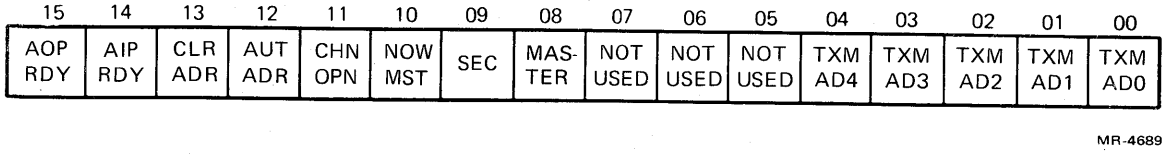


Figure 3-6 TMMR Register Format

Table 3-3 TMMR Register Bit Descriptions

Bit	Name	Description
0	TXM AD0	TRANSMITTER ADDRESS 0
1	TXM AD1	TRANSMITTER ADDRESS 1
2	TXM AD2	TRANSMITTER ADDRESS 2
3	TXM AD3	TRANSMITTER ADDRESS 3
4	TXM AD4	TRANSMITTER ADDRESS 4

Table 3-3 TMMR Register Bit Descriptions (Cont)

Bit	Name	Description
8	MASTER	MASTER (R/W) - When set, indicates this unit is TDM bus master; cannot be set if another master exists on the TDM bus. Cleared by BUS INIT. Set if SEC is set and there is no other TDM bus master.
9	SEC	SECONDARY MASTER (R/W) - When set, indicates this unit is a backup to the TDM bus master. Cleared by MASTER or BUS INIT.
10	NOW MST	NOW MASTER (R/W) - When set, indicates the unit was secondary (SEC was set) and master on the TDM bus was unasserted. (Unit has become master.) (N.B. When checking this bit, use byte manipulation.) Cleared by BUS INIT.
11	CHN OPN	CHANNEL OPEN (RO) - When set, indicates there is a channel open with a receiver. Cleared by TX INIT.
12	AUT ADR	AUTO ADDRESS (R/W) - When set, the counter will generate transmitter addresses and the transmitter address silo will be frozen. When clear, the address silo will cycle, putting out transmitter addresses in the desired sequence. Set by an empty address silo or BUS INIT.
13	CLR ADR	CLEAR ADDRESS SILO (WO) - When set, will clear out the address silo. This bit is only asserted for one instruction time; also generated by a BUS INIT.
14	AIP RDY	ADDRESS INPUT READY (RO) - When set, indicates the address silo may be loaded with a word. Set by asserting CLR ADR or a BUS INIT.
15	AOP RDY	ADDRESS OUTPUT READY (RO) - When set, indicates a word is ready to be moved out of the address silo. Cleared by asserting CLR ADR or a BUS INIT.

Transmitter Source CRC (TSCRC-764214)
Each time a word is ready at the output of the data silo it is strobed through the CRC logic. The resulting character may be read in this location. This register is used for maintenance only.

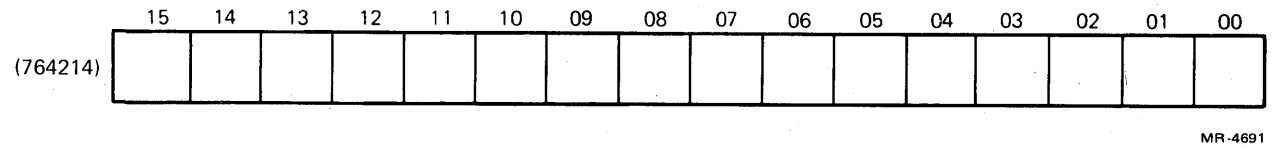


Figure 3-7 TSCRC Register Format

3.2.2 Receiver Bit Definitions

There are six registers associated with the receiver. These are described in Figures 3-8 through 3-13 and Tables 3-4 and 3-5.

Receiver Command Register (RCR-764220)

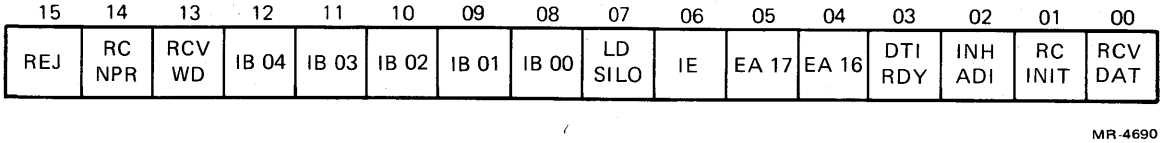


Figure 3-8 RCR Register Format

Table 3-4 RCR Register Bit Descriptions

Bit	Name	Description
0	RCV DAT	RECEIVE DATA (R/W) - When set, will accept all words and CRC characters until the end of a message from a transmitter that has a channel open. Cleared by an interrupt request (see bit 6), except for that of a DTO RDY or RC INIT.
1	RC INIT	RECEIVER INITIALIZE (WO) - When set, will initialize all bits in the receiver. Their initialized state is indicated in their description. This bit is asserted for only one instruction time. It is also generated by a BUS INIT or reset instruction.
2	INH ADI	INHIBIT ADDRESS INCREMENT (R/W) - When set, will inhibit incrementing of the receiver destination bus address (RDBA) register on NPR cycles. Cleared by RC INIT.
3	DTIRDY	DATA INPUT READY (RO) - This bit will set whenever the data silo is ready to accept the loading of a word. Primarily used for maintenance purposes. Set by RC INIT.

Table 3-4 RCR Register Bit Descriptions (Cont)

Bit	Name	Description
4	EA 16	EXTENDED BUS ADDRESS 16 (R/W) - Together with E 17 and the RDBA, forms an 18-bit address for NPR cycles. EA 16 and EA 17 will be automatically incremented when the RDBA overflows. Cleared by RC INIT.
5	EA 17	EXTENDED BUS ADDRESS 17 (R/W) - (See bit 4.) Cleared by RC INIT.
6	IE	INTERRUPT ENABLE (R/W) - An interrupt request is made if any of the following bits are set: ERR, SUC TXF, REJ COM, or if DTORDY is set and RC NPR is clear. When set, IE will enable an interrupt request to actually interrupt the processor, if it is running on a lower priority than the PCL11-B. Cleared by RC INIT.
7	LD SILO	LOAD SILO (R/W) - When set, the data silo may be loaded by moving a word into the RDDB. Reading the RDDB will not remove a data word if LD SILO is set. Cleared by RC INIT.
8	IB 00	IDENTIFICATION BIT 00 (RO) - RCR bits 8-12 contain the address of the transmitter which is communicating, or was last in communication with the receiver. Cleared by INIT.
9	IB 01	IDENTIFICATION BIT 01 (RO) Cleared by RC INIT.
10	IB 02	IDENTIFICATION BIT 02 (RO) Cleared by RC INIT.
11	IB 03	IDENTIFICATION BIT 03 (RO) Cleared by RC INIT.
12	IB 04	IDENTIFICATION BIT 04 (RO) Cleared by RC INIT.
13	RCV WD	RECEIVE WORD (R/W) - Must be set to open a channel. When set, will cause one word to be accepted (if RCV DAT is clear) from the first transmitter to address the receiver. Cleared by the interrupt request, receipt of a word or RC INIT.

Table 3-4 RCR Register Bit Descriptions (Cont)

Bit	Name	Description
14	RC NPR	RECEIVER NPR (R/W) - When set, if the RDBC is loaded, will cause hardware to initiate a NPR transfer of one word from the data silo, when such a word is ready. NPR cycles will continue until either the silo is empty, an error occurs or the RDBC overflows. No words may be moved from the silo when RC NPR is set. Cleared by RC INIT.
15	REJ	REJECT (R/W) - The receiver will reject a message after a channel is opened if REJ is set before RCV DAT. If REJ is set after RCV DAT, the receiver will truncate the message. Cleared by RC INIT.

Receiver Status Register (RSR-764222)

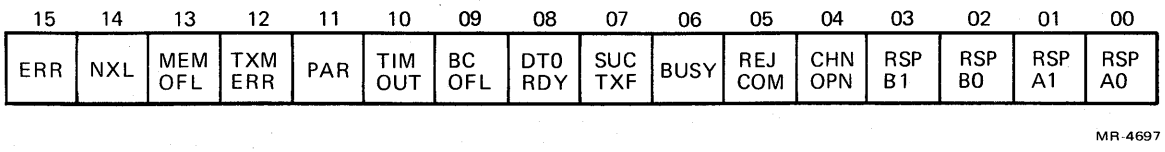


Figure 3-9 RSR Register Format

Table 3-5 RSR Register Bit Descriptions

<table>
<tr><th>Bit</th><th>Name</th><th>Description</th></tr>
<tr><td>0</td><td>RSP A 0</td><td>RESPONSE A 0 (RO) - RSR bits 0 and 1 contain the response codes received from the transmitter during the most recent timeslice. In the event of an error, these will be frozen while an RSP B = 0 0 is returned to the transmitter.
Cleared by RC INIT or SUC TXF.</td></tr>
<tr><td>1</td><td>RSP A 1</td><td>RESPONSE A 1 (RO)
Cleared by RC INIT or SUC TXF.

The response A bits accompany every data word sent to the receiver. They indicate to the receiver what the transmitter is sending during the timeslice.
<table>
<tr><th>RSP A 1</th><th>RSP A 0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>Transmitter has an error or is off-line</td></tr>
<tr><td>0</td><td>1</td><td>Null cycle</td></tr>
<tr><td>1</td><td>0</td><td>Valid word or CRC on data lines</td></tr>
<tr><td>1</td><td>1</td><td>Last CRC on data lines</td></tr>
</table></td></tr>
<tr><td>2</td><td>RSP B 0</td><td>RESPONSE B 0 (RO) - RSR bits 2 and 3 contain the response bits last sent out to the transmitter. In the event of an error, these bits will be frozen while a RSP B = 0 0 is returned to the transmitter.
Cleared by RC INIT or SUC TXF.</td></tr>
<tr><td>3</td><td>RSP B 1</td><td>RESPONSE B 1 (RO)
Cleared by RC INIT or SUC TXF.

The response B bits are returned to the transmitter to indicate what the receiver will be doing with the data during the timeslice.
<table>
<tr><th>RSP B 1</th><th>RSP B 0</th><th></th></tr>
<tr><td>0</td><td>0</td><td>Receiver has an error or is off-line</td></tr>
<tr><td>0</td><td>1</td><td>Null cycle</td></tr>
<tr><td>1</td><td>0</td><td>Check failure (CRC or parity error has been detected on previous data)</td></tr>
<tr><td>1</td><td>1</td><td>Acknowledge CRC or data</td></tr>
</table></td></tr>
</table>

Table 3-5 RSR Register Bit Descriptions (Cont)

Bit	Name	Description
4	CHN OPN	CHANNEL OPEN (RO) - When set, indicates there is a channel open with a transmitter. Cleared by RC INIT.
5	REJ COM	REJECT COMPLETE (R/W) - When set, indicates a rejection or truncation has been completed. If SUC TXF is clear, this was a rejection; if SUC TXF is set, it was a truncation. Will cause an interrupt request. Cleared by RC INIT.
6	BUSY	BUSY (RO) - Indicates the receiver is engaged in a reception. Will be set if CHN OPN or SND WD is set. Cleared by INIT.
7	SUC TXF	SUC TXF (R/W) - When set, indicates: 1. an entire message has been received, with parity and CRC checks. (SUC TXF set; REJ COM clear.) 2. a message has been truncated, but CRC and parity have been checked. (SUC TXF set; REJ COM clear.) Will cause an interrupt request. Cleared by RC INIT.
8	DTORDY	DATA OUTPUT READY (RO) - When set, indicates a word is ready on the output of the data silo. Will cause an interrupt request if RC NPR is clear. Cleared by RC INIT.
9	BC OFL	BYTE COUNT OVERFLOW (R/W) - When set, indicates the RDBC has overflowed. Cleared by RC INIT.
10	TIM OUT	TIME OUT (R/W) - This bit will set if, after a channel is open, more than one timeout period (approximately 1.5 seconds) passes without the successful transfer of a word. Cleared by RC INIT.
11	PAR	PARITY (R/W) - When set, indicates a parity error has been detected on an incoming word or CRC character. Cleared by RC INIT.

Table 3-5 RSR Register Bit Descriptions (Cont)

Bit	Name	Description
12	TXM ERR	TRANSMISSION ERROR (R/W) - When set, indicates an error condition has been detected in communicating with a transmitter. The type of error can be defined by looking at the RSP B and A bits. 1. CHECK FAIL (Parity or CRC error) RSR bit 15 = 1 ERR 12 = 1 TXM ERR 3 = 1 RSP B = 10 2 = 0 RSP B = 10 RSP A = don't care 2. OFF-LINE (Transmitter has error) RSR bit 15 = 1 ERR 12 = 1 TXM ERR 3 = d 2 = d RSP B = don't care 1 = 0 RSP A = 00 (off-line) 0 = 0 3. FAILED TO OPEN CHANNEL RSR bit 15 = 1 ERR 12 = 1 TXM ERR 3 = 0 RSP B = null 2 = 1 1 = 0 1 RSP A indicates or first word was 0 = 1 1 not valid. (Occurs only on first word.) Cleared by RC INIT.
13	MEM OFL	MEMORY OVERFLOW (R/W) - When set, indicates RDBA has overflowed and both EA 17 and EA 16 were set. Cleared by RC INIT.
14	NXL	NONEXISTENT LOCATION (RO) - When set, indicates the address that was contained in RDBA does not exist on the Unibus and an NPR to the location was aborted. Cleared by writing a zero into this bit or by RC INIT.
15	ERR	ERROR (RO) - This bit will set whenever any RSR bit 9 through 14 is set. Will make an interrupt request. Cleared by RC INIT.

Receiver Destination Data Buffer (RDDB-764224)
All data received from the transmitter will appear on the output of the data silo at this location. This data must be read, then removed before the transfer is considered complete. This may be done by NPR transfers or direct moves. If an RDIO instruction is used, the DTORDY (RSR bit 8) should first be checked. (This bit may cause an interrupt if RC NPR is clear.)

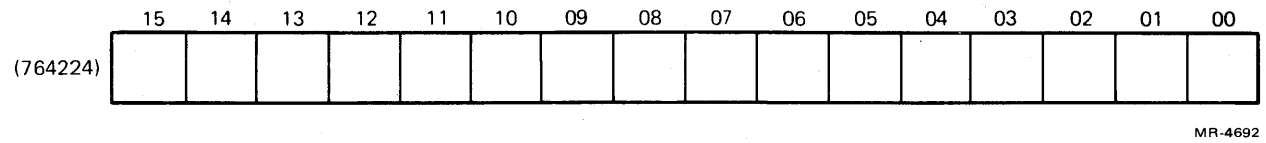


Figure 3-10 RDDB Register Format

For maintenance purposes the silo may also be loaded. If LD SILO is set, moving a word into this location will load it into the data silo. With LD SILO set, reading the TSDB will not remove the word read from the silo.

Because the RDDB is the input of a 64-word silo when writing, and the output of the silo when reading, instructions that involve a read-restore-write cycle may not be executed accurately on this location.

Receiver Destination Byte Count (RDBC-764226)
This register is loaded with the 2's complement of the number of bytes in the length of the buffer area that will receive the data via NPR transfers. During NPRs this register will increment twice every time a word is transferred from the silo to its destination. If more data is sent than indicated in the RDBC, BC OFL will set. The host computer may then decide to allocate more room, or truncate the message.

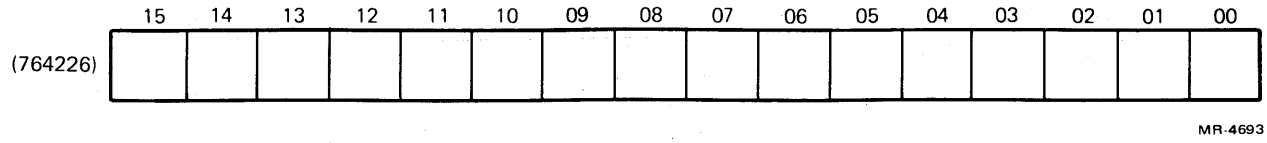


Figure 3-11 RDBC Register Format

Receiver Destination Bus Address (RDBA-764230)
This register is loaded with the address of the first word of the buffer area to which the received data is transferred. The RDBA will be incremented after each NPR cycle is executed, unless INH ADI (RCR bit 2) is set.

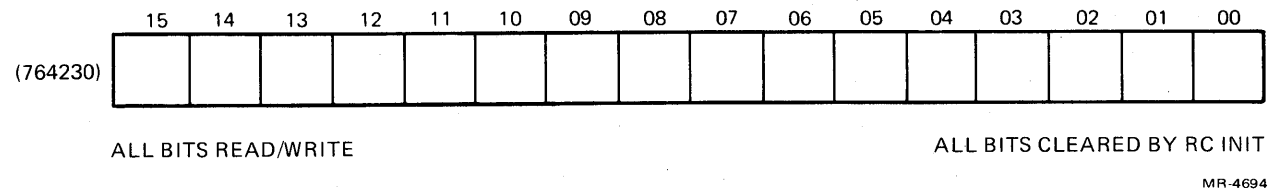


Figure 3-12 RDBA Register Format

Receiver Destination CRC (RDCRC-764234)
Each time a word is loaded into the silo it is also strobed through the CRC logic. The resulting character may be read in this location. This register is used for maintenance purposes only.

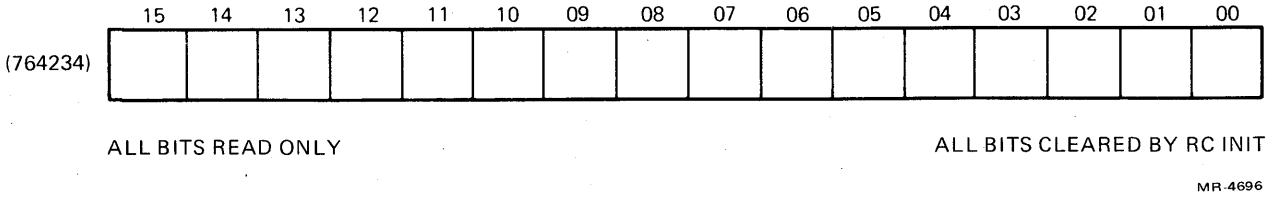


Figure 3-13 RDCRC Register Format

Summary of Registers and Mnemonics

Transmitter
The following is a list of registers and their standard Unibus addresses.

Transmitter Command Register	764200	TCR
Transmitter Status Register	764202	TSR
Transmitter Source Data Buffer	764204	TSDB
Transmitter Source Byte Counts	764206	TSBC
Transmitter Source Bus Address	764210	TSBA
Transmitter Master/Maintenance Register	764212	TMMR
Transmitter Source Cyclic Redundancy Character	764214	TSCRC
Interrupt Vector	170	

Receiver
The following is a list of registers and their standard Unibus addresses.

Receiver Command Register	764220	RCR
Receiver Status Register	764222	RSR
Receiver Destination Data Buffer	764224	RDDB
Receiver Destination Byte Count	764226	RDBC
Receiver Destination Bus Address	764230	RDBA
Receiver Destination Cyclic Redundancy Character	764234	RDCRC
Interrupt Vector	174	

NOTE

PCL11-B will respond to addresses 764216, 764232, 764236. However, since these registers are not part of the device, writing into them will have no effect and reads will be returned all zeros.

3.2.3 PCL11-B Operation

This section is a general discussion of the manner in which one PCL11-B may transfer data to another over the TDM bus. Timing, detailed description of TDM bus signals, the protocol for proper transfer and descriptions of software/hardware interactions are discussed.

3.2.3.1 General Operation - One 16-bit word may be transferred from a transmitter to a receiver every two microseconds. The timing signals for the transfer are generated from an enabled master section (only one section may be enabled on a TDM at any time) and the control signals are generated from the transmitter (e.g., receiver address and type of transfer). Before a successful transfer can take place, both the transmitter and receiver involved must be properly set up by programs residing in their respective computers.

3.2.3.2 Master Section - The master section has two functions. It divides the bus into timeslices by generating two timing signals, TP0 and TP1. These timing signals are used by both the transmitter and receiver to complete data transfers. The master section also provides a new 5-bit transmitter address every timeslice. This address will be decoded by one transmitter on the bus, enabling it to effect a word transfer.

Time Phase Signals

Each master section has a clock that produces the two time-phase signals TP0 and TP1. These are both square waves, 90° out of phase. They may be corrected to have a period corresponding to bus length, and they are seen by all transmitters and receivers on the bus. (See Figure 3-14.)

These two signals further divide each timeslice into four phases. During each phase, one part of the data transfer will take place.

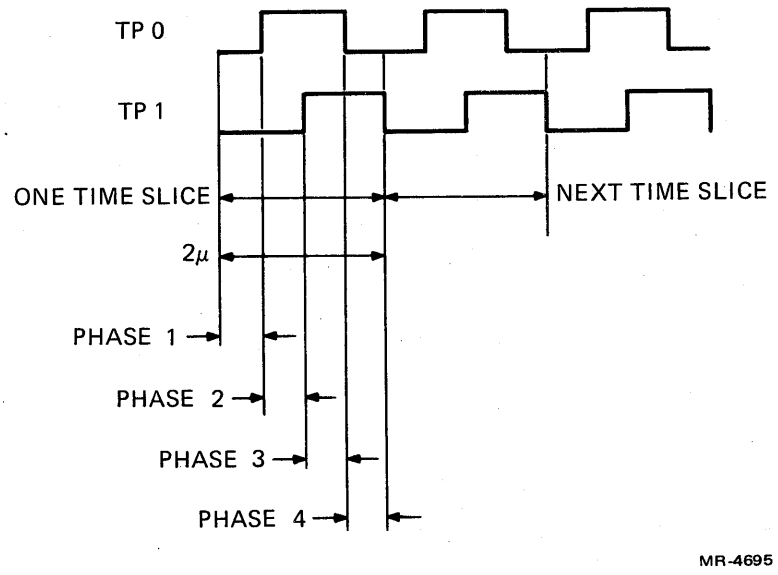


Figure 3-14 Master Timing

Address Generation

The master section also provides a transmitter address every timeslice. Every transmitter section contains a 5-bit address switch set up to the transmitter's TDM bus address. During Phase 1 of each timeslice, every transmitter on the TDM bus will compare this switch to the address generated by the master section. If the two are identical, the transmitter may use the rest of the timeslice to send one 16-bit word of a message to a receiver of its choice. Since a new transmitter may be selected every timeslice, a number of transmitters may be in the process of transmitting a message at the same time. Each will wait its turn to send one word of its message to the receiver.

The master section may generate these transmitter addresses in one of two ways. The first, and simplest, method involves the use of a 5-bit decrementing counter. The counter is loaded with the number contained in a 5-bit switch residing in the master section. The counter is decremented, by one, every timeslice, until address number one is being put out onto the bus. The counter will then be reloaded with the number in the switch in time for the next timeslice, whereupon the entire process will repeat itself.

The second means of address generation involves use of a 5-bit X 50-word address silo (which consists of a FIFO: First In, First Out memory). This silo may be loaded, by software, with 5-bit transmitter addresses in any sequence (though no address may be repeated in succession). When this silo is enabled, the addresses contained in it are put out onto the bus for one timeslice, and then returned to the top of the silo. They will continue circulating this way until disabled. Generating transmitter addresses in this manner allows great flexibility in assigning the speed of transfer of messages. If one transmitter's address is loaded into the silo, for example, so as to appear every second timeslice, while all other addresses appear only once, this transmitter will then be able to send an entire message more quickly than any other.

Which of the above two methods is used by an enabled master section is determined by the state of the auto-address (AUT ADR) bit in the TMMR register. When this bit is set, the counter method of address generation is operational; when cleared, the address silo is used. This bit will be set whenever the address silo is empty or when set via the Unibus. Also, it must be set during the time in which the address silo is being loaded. Once the silo is loaded this bit may be cleared, thus enabling the silo to circulate. Note that at least 20 addresses must be loaded into the silo before it will operate reliably.

Enabling the Master Section

Although each PCL11-B unit contains its own master section, only one of these may be enabled at any one time, when a number of units are connected together on a TDM bus. A master section is enabled when the MASTER bit is set in the TMMR register. There are two ways this bit may be set. First, it may be set from its host computer, via the Unibus.

The second way involves another bit in the TMMR, the secondary (SEC) bit. This bit is used to transfer mastership of the TDM bus from the enabled master section to a backup master, automatically, in the event the first master is removed from the bus for any reason. An enabled master section will assert a TDM bus line called MASTER ACTIVE. Assertion of this line will prevent the setting of a different master bit by the above method. If a master section has its SEC bit set, and sees MASTER ACTIVE become unasserted, it will set its own MASTER bit and take over mastership of the bus, then clear SEC. At the same time, NOW MST sets in the TMMR, indicating this PCL11-B has assumed the role of TDM bus master.

The SEC bit is set via the Unibus. Take care to ensure that no more than one SEC bit is set at any one time - this guarantees that if any master goes down, only one new master will take its place.

3.2.3.3 **Data Transfer** - The transmitter uses the address and time phase signals generated by the master section to synchronize communication. During each phase one part of the transfer of one word of the message takes place.

Phase 1
During this period of time the transmitter is comparing the 5-bit transmitter address on the TDM bus with its own address switch. When the two are identical, the transmitter's timeslice is identified. Before the transmitter will use the timeslice, however, one of two conditions must occur. The transmitter must either be in communication with a receiver (have a channel open) or be in the process of opening one. If one of these conditions exists, and the TDM bus transmitter address compares with its own, active communication will commence during Phase 2.

Phase 2
During this period the transmitter will assert the TDM bus data lines, putting out the word it wishes to transfer. This word comes from the output of a 64-word X 16-bit data silo (which is a FIFO, First In, First Out memory). At the same time, the receiver address is asserted on the TDM bus, as well as on two response A lines. These two lines indicate to the receiver what type of transfer is coming during the next two phases. The two lines allow four possibilities:

RSP A 1	RSP A 0	
0	0	OFF-LINE If neither line is asserted, one of two possibilities exists: 1. The transmitter either does not exist on the bus or it did not satisfy either condition for commencing communication as per Phase 1. If either of these cases exists, all receiver address lines will also be 0s. 2. During communication, the transmitter has come up with an error and will consider the channel closed after this timeslice.
0	1	NULL CYCLE The transmitter will assert only the RSP A 0 line if either the data is not ready to be sent or no command bit to send a word is set. A null cycle should occur only with a channel already open.

1	0	VALID WORD OR CRC Only the RSP A 1 line is asserted if the data lines on the bus are being driven by a word to be transferred or a cyclic redundancy check (CRC) character.
1	1	LAST CRC Both lines are asserted for these timeslices. The last character to be sent is always a CRC check character. This response is an indication to the receiver to begin the channel closing procedure.

Both the receiver and transmitter separately remember whether a channel is open. A channel is opened on the successful transfer of the first word of a message, and will be closed after the sending of either the first or last of the response A codes above.

During this phase the receiver decodes the five receiver address lines being driven by the transmitter. Decoding is accomplished by comparison of these five lines with the 5-bit address switch residing in the receiver section. At the end of Phase 2 the receiver will decide if it has been addressed, and then take the appropriate action.

Phase 3

Once the receiver has decided that it has been addressed, it will set up its own response codes to be sent back to the transmitter. These codes will indicate to the transmitter exactly the receiver's response to what the transmitter has done during the timeslice.

Before setting up these codes, the receiver looks at a number of different things in the interface. First, the address of the transmitter is checked. If the word being sent is the first of a message, this address will not matter. However, if a channel is already opened, the receiver will compare the address of the transmitter presently talking to it with that of the transmitter with which it has an open channel. If the address does not compare, the receiver will return a busy response. The receiver also looks at the response codes that the transmitter has sent. From these the receiver can discover the type of transfer occurring in the timeslice, and thereby deduce what its response should be.

Finally, the receiver checks the command bits in the interface. They will indicate whether a word (or message) should be accepted.

The receiver has two response lines (called RSP B 0 and 1) allowing four possible responses:

RSP B 1	RSP B 0	
0	0	**BUSY OR OFF-LINE** Neither line will be asserted if: 1. the receiver does not exist on the bus or is not set up to receive a message. 2. the receiver has an open channel with a different transmitter. 3. the receiver, during communication, has come up with an error and will consider the channel closed after this timeslice.
0	1	**NULL CYCLE** The receiver will assert only the RSP B 0 line if it is not prepared to receive a word during this timeslice (e.g., if the silo is full), if it does not have the proper command bit set, or if the transmitter is executing a null cycle. A null cycle may occur only when the channel is open.
1	0	**CHECK FAIL** Only RSP B 1 will be asserted if the receiver has detected a CRC or parity error.
1	1	**ACKNOWLEDGE** Both lines will be asserted if: 1. the transmitter has sent a valid word and the receiver will take and put it into its silo. 2. the transmitter has sent a CRC on a previous timeslice and it has been checked by the receiver and found to have no errors.

Phase 4
At the beginning of this phase the receiver actually removes the data from the bus by strobing it into a 64-word X 16-bit data silo. During this phase the receiver is driving the TDM bus with its response to the transmitter. At the end of the phase the transmitter will strobe these responses into its interface. Depending on what these response bits actually are, the transmitter will begin setting up for the next transfer. If the receiver has accepted a data word, the transmitter will remove the sent word from its silo.

3.2.3.4 Checking of Data - There are two checks made on the data sent from the transmitter to the receiver. First, every 16-bit word transferred is accompanied by a parity bit (odd parity is used). In the event that the receiver detects a parity error in any word received, the receiver will return a CHECK FAIL response, and consider the channel closed on the succeeding timeslice.

Cyclic redundancy check (CRC) characters are also used to guard further against data errors during transmission. This method of error detection involves modulo 2 division of the message by a selected polynomial, in this case $1+X+X^8+X^{15}$. Both receiver and transmitter contain logic to perform division by the polynomial. This logic keeps track of only the remainder of the division. Before each word is removed from the transmitter's data silo, it is divided by the polynomial. The remainder after the entire block of the message has been sent will be the CRC character. The receiver performs an identical division as the words are loaded into its silo. The remainders after all data words have been processed will be equal, if no errors have occurred. The check character will be sent as part of the message, and when divided by the receiver (modulo 2) will result in a remainder of zero, if transmission was error-free.

If $Q(x)$ was the message polynomial,
$P(x)$ the selected polynomial,
$S(x)$ the quotient of $\frac{Q(x)}{P(x)}$, and

$R(x)$ the remainder of $\frac{Q(x)}{P(x)}$,

we then perform in the transmitter:

$$\frac{Q(x)\ X^{16}}{P(x)} = S(x) + \frac{R(x)}{P(x)}$$

$Q(x)$ is shifted by 16 bits (as the remainder $R(x)$ will be appended to the message) by multiplying by X^{16}. In the receiver we perform:

$$\frac{Q(x)\ X^{16} + R(x)}{P(x)} = \frac{\text{Received message}}{P(x)}$$

$$= S(x) + \frac{R(x)}{P(x)} + \frac{R(x)}{P(x)}$$

$$= S(x)$$
(modulo 2 addition)

Any error not divisible by P(x) will be detected by a nonzero remainder after the division. If the error is represented by E(x), when the check is performed:

$$\frac{Q(x)\ X^{16} + R(x) + E(x)}{P(x)} = S(x) + \frac{R(x)}{P(x)} + \frac{R(x)}{P(x)} + \frac{E(x)}{P(x)}$$

$$= S(x) + \frac{E(x)}{P(x)}$$

a nonzero remainder results.

The selected polynomial will detect the following errors.

1. any odd-number errors
2. all double errors
3. all burst errors of length 15 or less
4. 99.994% of bursts of length 16
5. 99.997% of bursts longer than 16

Because the above error detection capabilities will only be valid with messages of up to 2635_{10} bits (164_{10} words), a block length of 128_{10} (200_8) words was selected. The transmitter will insert a CRC character after every block and then begin calculation of a new CRC character. The last block transmitted may be less than or equal to 200_8 words, but only one CRC will be sent after this block, no matter what size it is.

Both receiver and transmitter are counting the number of words being transferred and thus both are able to tell when a CRC is to be transferred. The CRC is actually sent in exactly the same manner as a data word. It is accompanied by a RSP A of 10, unless it is the last CRC in the message, in which case RSP A = 11.

3.2.3.5 Channel Opening and Closing - As previously described, a channel is opened between a receiver and transmitter upon the successful transfer of one word between them. Both units have a channel open bit set in one of their registers upon such a transfer and cleared only at the end of a message or in the event of an error.

If the transmitter receives a check-fail, an off-line response from the receiver, or a master down or timeout error, it will immediately clear CHN OPN and interrupt its processor with an error. Other transmission errors, overrun, and nonexistent location errors will wait until the next transmitter timeslice, and the transmitter will then send out a RSP A = 0 0 to the receiver before clearing CHN OPN and interrupting. The RSP A and B bits, which may be read by the transmitter's processor, will remain frozen in the state they were in at the time the error occurred.

Memory overflow errors will result in a suspension of NPR cycles until the error condition is removed. TDM bus transfer may continue as usual, but the silo is liable to empty out, causing only null cycles to occur on the TDM bus.

If the receiver gets an off-line response from the transmitter, or a check-fail, it will immediately clear CHN OPN and interrupt its processor with the error. In the event of other transmission errors or a nonexistent location error, the receiver will wait until the next time the transmitter with which the channel is opened addresses its receiver, and then send out a RSP B = 0 0. After the timeslice, CHN OPN will be cleared and the processor interrupted. As in the transmitter, the response codes that may be read by the computer are frozen at the time the error occurred. Memory overflow and byte count errors will only result in the suspension of NPR activity until the error is handled. However, the receiver silo may become full, resulting in a number of null cycles occurring on the TDM bus. If a timeout error occurs, the receiver will immediately clear CHN OPN and cause an interrupt.

At the end of a message, there is a set sequence for the closing of the channel between the transmitter and receiver. First, the transmitter decides that all of the data has been sent. This is considered done when the data silo is empty and the byte count register has overflowed. (The byte count register is originally loaded with the 2's complement of the number of words to be sent, and is incremented twice every time a word is loaded into the silo from the Unibus). When this occurs, the transmitter prepares and sends the last CRC character, accompanied by RSP A = 1 1. This response is an indication to the receiver that the message has been entirely transmitted. The receiver will check the CRC character and then wait until its silo has been emptied into its Unibus. After this, the receiver will respond with a RSP B = 1 1. When the transmitter sees this response, it will wait, and then expect to see RSP B = 0 0; this will ensure the response lines have not become permanently stuck in the asserted state. After this has happened, the receiver and transmitter will clear CHN OPN.

CHN OPN will also be cleared after a reject or truncate operation.

3.2.3.6 Command Procedure - The preceding paragraphs discussed how data is transferred one word per timeslice until the entire message is sent and checked. The following paragraphs describe the host computer's function in the transfer.

Transmitter

The transmitter logic will remove data from its silo and send it to the desired receiver. The transmitter's host computer has three functions to fulfill in order to complete the transfer.

First, it must load the silo with the data to be transferred. This can be done in two ways: (1) The silo input appears on the Unibus as a register (the transmitter source data buffer, TSDB). Moving a word to this location will cause it to be loaded into the silo, whereupon it will migrate toward the output. Thus, the transmitter may load up the silo with as many words as desired, simply by moving them into the TSDB. (2) In addition to simple moves, the host processor may set up an NPR transfer of a section of memory to the TSDB. This can be effected by loading the transmitter source byte count (TSBC) with the 2's complement of the number of bytes to be loaded, and loading the transmitter source bus address (TSBA) with the first address of the section of memory to be loaded. When these registers have been loaded, the NPR cycles are initiated by setting the TX NPR (bit 14) in the transmitter command register (TCR). Once this bit has been set, moves to the TSBD will be inhibited.

Both direct move and NPR transfer methods of loading the silo may be used in the sending of a message. It is important to realize, however, that the TSBC is incremented twice every time a word is loaded into the silo by moving or by NPR transfer. Therefore, the TSBC should be loaded with the total number of NPRs transferred to the silo. The TSBC is used by the transmitter logic to determine if there are any more words to be transferred, and hence, should be loaded even if no NPRs are to take place. The TSBC need not be loaded if the user can ensure the data silo will not be empty until the last word of the message has been sent to the receiver.

Second, the transmitter's host computer must specify the receiver to which the message is destined. This is achieved by loading the 5-bit TDM BUS address of the receiver into the destination code bits in the TCR. (DC 00-DC 04 are bits 8 through 12.)

Third, the host computer must enable the transmission by setting the proper command bits in the TCR. Send word (SND WD bit 13) must be set to open a channel with a receiver; this will cause one word to be sent out before interrupting the processor after opening the channel. If so desired, SND WD may be set again a number of times, each time sending out only one word before interrupting. After the channel is opened, the hardware will execute a number of null cycles while waiting for SND WD to be set. The start of transmission (ST TXM bit 0) will cause all words to be sent on successive timeslices, if possible, until the entire message has been transmitted. After the CRC has been checked and the channel properly closed, the processor will be interrupted. The ST TXM bit may be set at the beginning of the message as well as when SND WD is set. In such case, no interrupts will occur until the entire message has been transferred. ST TXM may be set at any time and, even if SND WD is also set, no interrupts will occur until the end of the message. However, SND WD must be set at the beginning of the message to open the channel.

Receiver

The receiver's host computer must perform functions similar to that of the transmitter's, but these are involved rather in unloading the silo onto the Unibus. The receiver contains command bits (similar in function to the transmitter's) that must be manipulated.

The receiver's host computer is responsible for unloading the data silo in either of two ways: (1) The silo output appears as a register on the Unibus (the receiver destination data buffer, RDDB). Moving a word from this location will cause it to be removed from the silo. Thus, the receiver may unload the silo simply by moving data words out of the TSDB. (2) On the other hand, the host processor may set up an NPR transfer of the data in the silo to a buffer area in memory. This buffer area is defined by a receiver destination byte count (RDBC) and a receiver destination bus address (RDBA) register. The RDBA is loaded by the host computer with the first address of the buffer, and the RDBC with the 2's complement of the number of bytes. Once these registers are loaded and RC NPR (RCR bit 14) is set, a word ready at the output of the silo will begin an NPR cycle to remove the data to the buffer. Setting the RC NPR bit will inhibit program moves out of the silo.

The RDBC will be incremented every time an NPR cycle is executed. After a message is successfully received, this register may be used to determine the number of words actually transferred into the buffer. If the incoming message has more words than set up in the RDBC, a byte count overflow error will occur. The host computer may then set up a new buffer or merely truncate the message at that point.

The receiver also has two command bits, similar in use to the transmitter's: receive data (RCV DAT) and receive word (RCV WD). RCV WD must be set to open the channel; every time it is set, one word will be accepted, causing an interrupt. If RCV DAT is set, the entire message will be received before interruption. As in the transmitter, both bits may be set to allow interrupt-free reception of the entire message.

End of Message

Both the receiver's and transmitter's host computers are informed of the successful completion of a message's transfer by an interrupt from the successful transfer (SUC TXF) bit in their respective status registers, receive status register (RSR) and transmitter status register (TSR). The setting of this bit indicates that data has moved from the transmitter's Unibus to the receiver's Unibus without error.

3.2.3.7 Rejection and Truncation - The receiver has the capability of terminating a message before its last word is received from the transmitter. A receiver may reject an entire message after only a few words have been received, or truncate the remainder of the message if it decides it does not want any more data.

Rejection

By rejection, the receiver indicates to the transmitter that it does not wish to receive any of the message being sent. Rejection can only take place before RCV DAT is set. The receiver, after having received one or more data words, may decide from information contained in these words, or from the identification bits indicating the transmitter's address, that it does not wish to receive the message at all. It can then reject it, if need be.

Rejection is accomplished by setting the reject (REJ) bit in the RCR. This will cause the receiver hardware to assert the reject line on the TDM bus during the next addressed timeslice, as well as return a response B = 0 1, a null cycle. After this timeslice, the channel open bit in the receiver will be closed and the reject complete (REJ COM) bit in the RSR will be set, causing an interrupt. The channel open bit in the transmitter will also be cleared, and software reject (SORE) set in the TSR. This will interrupt the transmitter's computer to indicate the message was not accepted at all.

Truncation

Truncation occurs when the receiver decides that it cannot, or does not wish to, accept any more data from the transmitter. This would occur, for example, if the receiver's memory buffer had been filled and no other space was available for the rest of the message. The receiver could, at that point, truncate the message. Truncation can only take place after RCV DAT has been set.

Truncation is initiated by setting the REJ bit in the RCR. Truncation is differentiated from rejection by RCV DAT having been set during reception of the message. During the next addressed timeslice, the receiver will respond with a null cycle, as well as assert the truncate line on the TDM bus. Both receiver and transmitter data silos will be cleared, along with the TSBC. A CRC check character will then be prepared and the channel will be closed in exactly the same manner as in a successful transfer. This means the SUC TXF will be set in both the receiver and transmitter. To differentiate between a regular successful transfer and a truncation, the SORE bit will also be asserted in the transmitter, with the REJ COM asserted in the receiver.

3.3 UNIBUS ADAPTER

The Unibus adapter (UBA) is a KS10 I/O controller that allows Unibus peripheral devices to be connected to the KS10 system. The UBA connects between the internal KS10 (backplane) bus and a

Unibus as shown in Figure 3-15. More than one UBA may connect to the backplane bus, thus allowing more than one Unibus to be interfaced to the KS10 system. Each UBA consists of a single extended hex module (M8619) mounted in the KS10 cabinet.

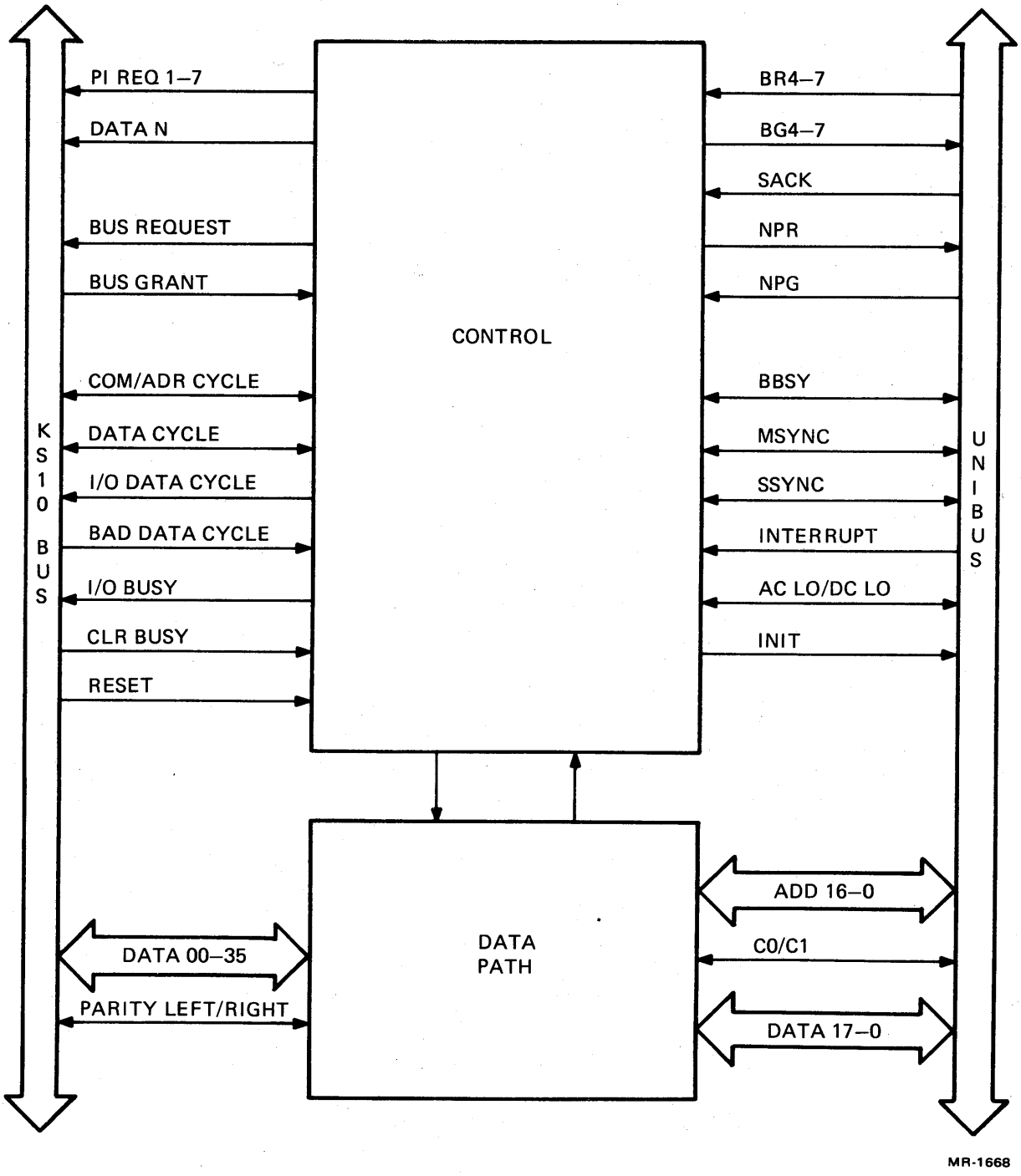


Figure 3-15 UBA, Simplified Block Diagram

3.3.1 Basic Operation

A UBA controls and synchronizes the following major operations that take place between the connecting Unibus devices and the rest of the system.

1. NPR data transfers from Unibus devices to KS10 memory, and transfers from KS10 memory to Unibus devices
2. I/O register data transfers (initiated by the CPU or console) to/from Unibus devices
3. Vector address transfers from Unibus devices to the CPU, following device interrupts

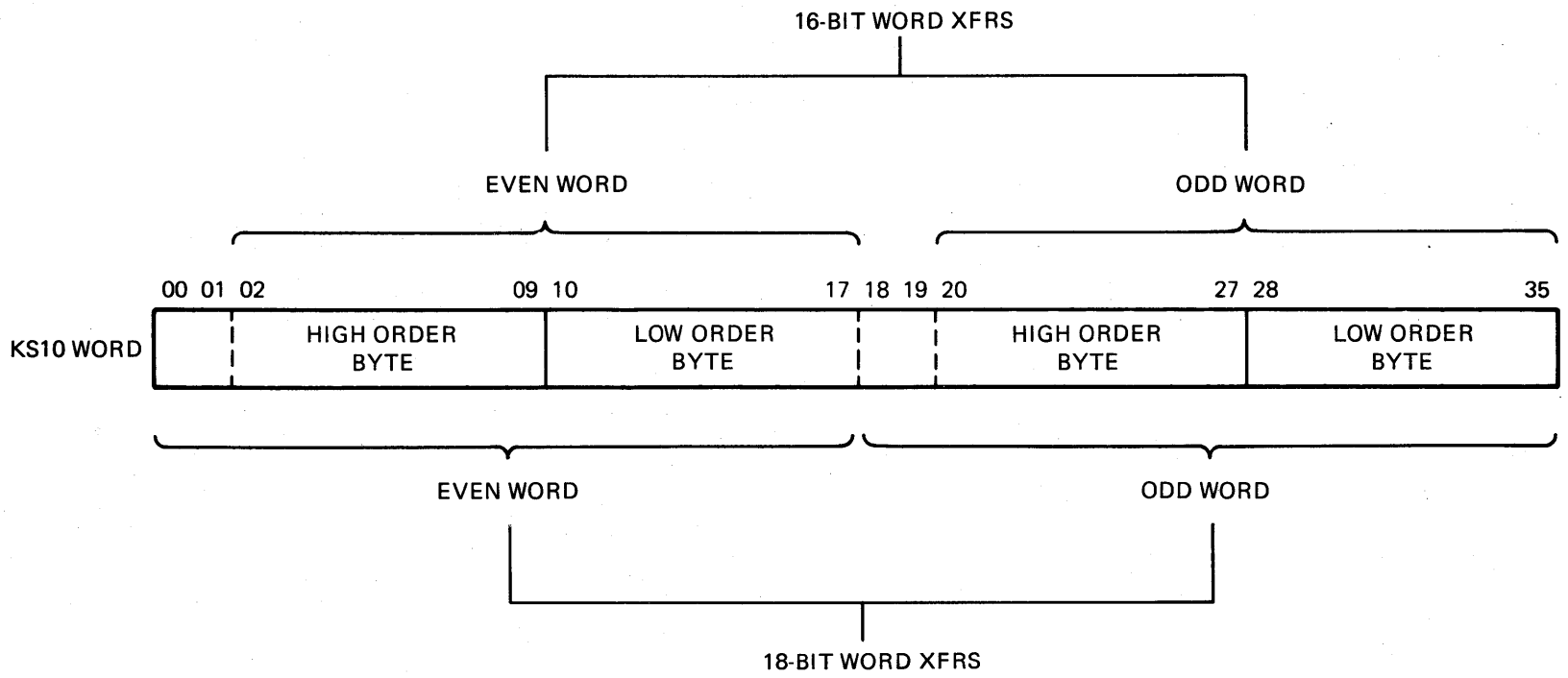
3.3.1.1 NPR Data Transfers - The UBA allows the following NPR data transfers by a Unibus device to/from KS10 memory.

1. DATO to memory (16- or 18-bit word)
2. DATOB to memory (8-bit byte)
3. DATI from memory (16- or 18-bit word or 8-bit byte)

The transfers to/from memory are direct, with no intervention or control by the CPU. Unibus data positioning within the KS10 memory word is shown in Figure 3-16. Correspondence to the Unibus address is indicated.

Data flow for the NPR write-to-memory operation (DATO or DATOB by device) and the NPR read-from-memory operation (i.e., DATI by device) are shown in Figures 3-17 and 3-18. Note that word transfers may be 18 bits as well as 16 bits. (Some devices such as the RH11 use the 2 Unibus parity lines, in addition to the 16 data lines, to transfer NPR data.) Also note that in addition to normal byte and word transfers, a fast-transfer mode of operation is implemented for word transfers only. This mode, which is program-selectable, is used for transfers to/from high-speed I/O devices such as disk drives. It provides an extra 18 bits of data buffering, thus reducing the number of KS10 bus memory operations by a factor of 2. Fast-transfer mode is set by loading a bit in the paging RAM as specified in Paragraph 3.3.2.

> NOTE
>
> **Fast mode should not be set for more than one device on a Unibus. Simultaneous NPR data transfers on a single Unibus give unspecified results when two or more of the active devices are transferring data in fast mode.**



UNIBUS DATA	UNIBUS ADDRESS BITS A1	A0
LOW ORDER BYTE – EVEN WORD	0	0
HIGH ORDER BYTE – EVEN WORD	0	1
LOW ORDER BYTE – ODD WORD	1	0
HIGH ORDER BYTE – ODD WORD	1	1
EVEN WORD	0	0
ODD WORD	1	0

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Figure 3-16 Unibus Data Positioning within a KS10 Word

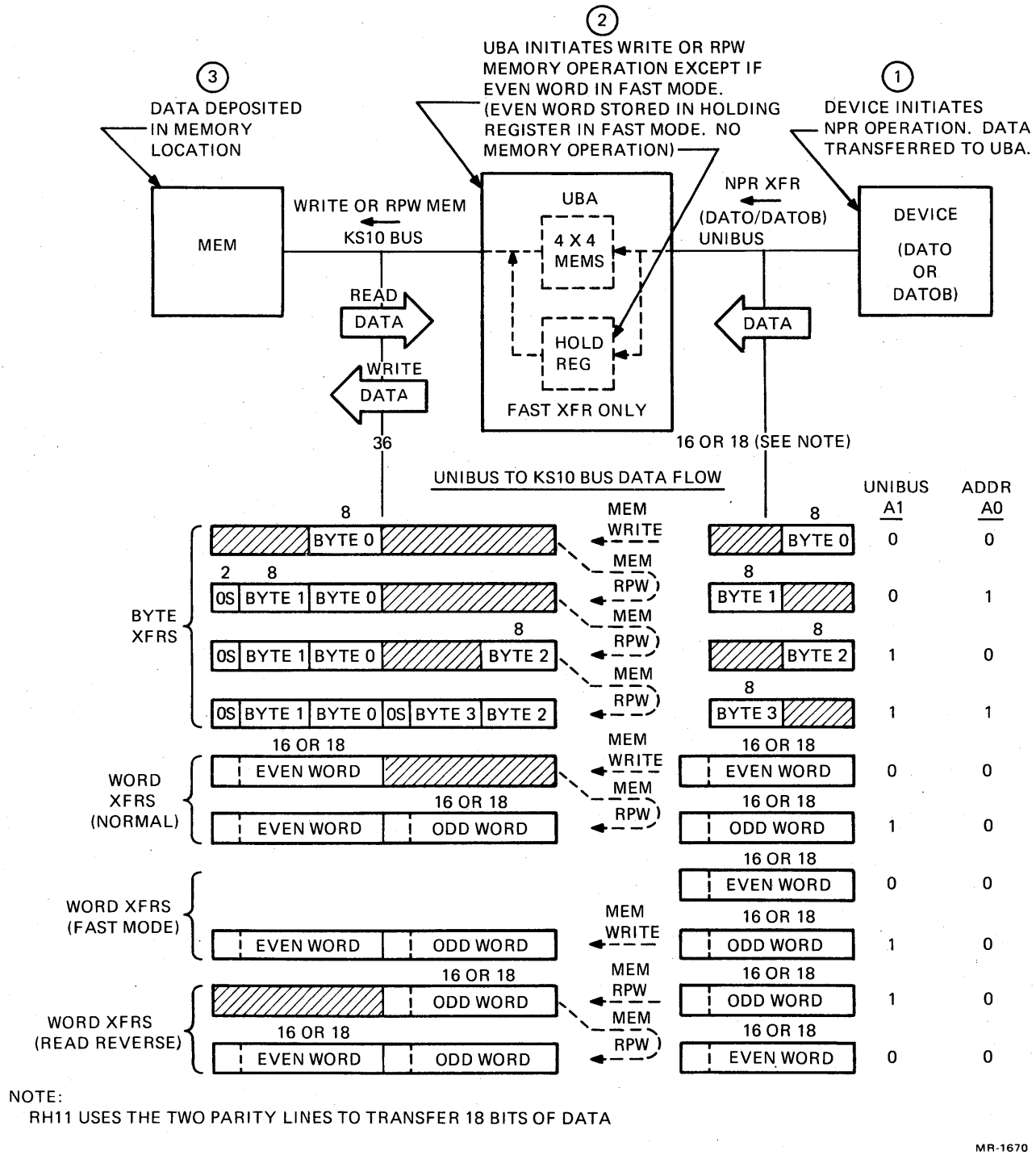


Figure 3-17 NPR Write-to-Memory, Data Flow

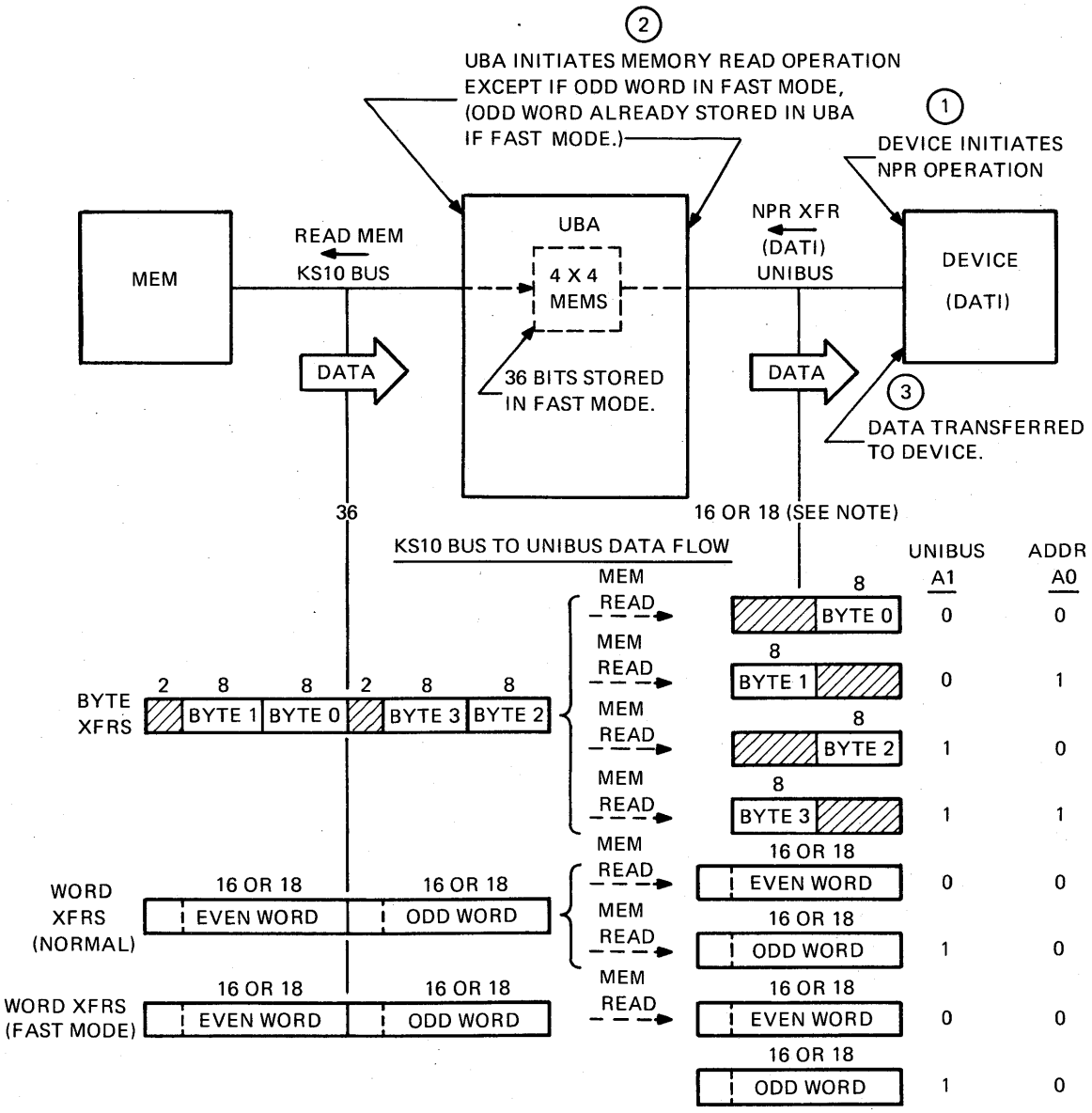


Figure 3-18 NPR Read-from-Memory, Data Flow

In addition to the fast mode of operation for both NPR write-to-memory operations and read-from-memory operations, a special mode for NPR write-to-memory operations is implemented in the UBA to accommodate device read-reverse operations from slower devices such as tape drives. The read-reverse mode is provided mainly for diagnostic program use; the system monitor does not use it. As for fast mode, read-reverse mode is set by loading a bit in the paging RAM as specified in Paragraph 3.3.2.

NOTE
Results are unspecified if read-reverse mode and fast-transfer mode are both set for the same NPR data transfer.

Basic operation during NPR data transfers is as follows.

1. The Unibus device, in response to a previously issued read/write command, initiates a Unibus NPR operation when it has read data to transfer to KS10 memory, or when it requires write data from KS10 memory.

2. For NPR write-to-memory operations, the UBA stores the read data transferred over the Unibus and then does one of the following operations, depending on the Unibus address and the transfer type.

   a. Byte Transfers - For the low-order byte in an even word (byte 0 in Figure 3-17), which is the first byte loaded into a KS10 memory location during execution of a device-read command, the UBA does a memory-write operation on the KS10 bus to load the byte directly into memory. For all other bytes (bytes 1, 2, and 3 in Figure 3-11), the UBA does a memory read-pause-write operation. The read-pause-write operation is necessary so that the data loaded in memory during the device's previous NPR data transfer may be first read and recirculated by the UBA. The previously loaded data is then written back into memory along with the current byte.

   b. Word Transfers (Normal) - For normal even-word transfers (as for byte 0 transfers), the UBA does a memory-write operation over the KS10 bus to load the data directly into memory. For normal odd-word transfers (as for bytes 1, 2, and 3), the UBA does a read-pause-write memory operation. This reads the previously loaded even word and then writes both the odd and even word into memory.

c. Word Transfers (Fast Mode) - For fast mode even-word transfers, the UBA initiates no memory operation. The word is loaded from the Unibus into a holding register until the next NPR data transfer (an odd word). The UBA then initiates a memory-write operation to write both even and odd words into memory.

d. Word Transfer (Read-Reverse) - For transfers in read-reverse mode, the UBA receives data words from the Unibus in reverse order; that is, the odd word is received and written by the UBA into a memory location first. This, and the fact that a read-pause-write memory operation is initiated for odd and even words, is the only difference in data flow between read-reverse and normal operation.

3. For all NPR read-from-memory operations, except for odd words in fast mode, the UBA does a memory-read operation over the KS10 bus, temporarily stores the memory data, and then transfers the byte or word specified by the Unibus address over the Unibus to the device. In fast mode, both odd and even words are stored in the UBA during the even-word transfer. Thus, for the next (odd-word) transfer, the data is transferred directly to the device with no memory operation being required.

3.3.1.2 I/O Register Data Transfers - The UBA allows the CPU or console to write and read the addressable I/O registers in the Unibus devices connected to the KS10 system. Transfers initiated on the Unibus by the UBA in response to KS10 bus commands are as follows.

1. DATO to device (16-bit word)
2. DATOB to device (8-bit byte)
3. DATI from device (16-bit word or 8-bit byte)

In addition to writing and reading Unibus device (external) registers, the CPU or console may also write/read registers in the UBA itself. These UBA (internal) registers are discussed in Paragraph 3.3.2.

Data flow for both I/O register write and read operations is shown in Figures 3-19 and 3-20. I/O register data transfers are initiated by the CPU as a result of the external instruction set. (See Paragraph 3.4.) Both word and byte instructions can be executed. I/O register data transfers are also initiated by the console in response to deposit and examine I/O commands entered via the CTY (DI and EI commands). The console does only word transfers; byte transfers are not implemented.

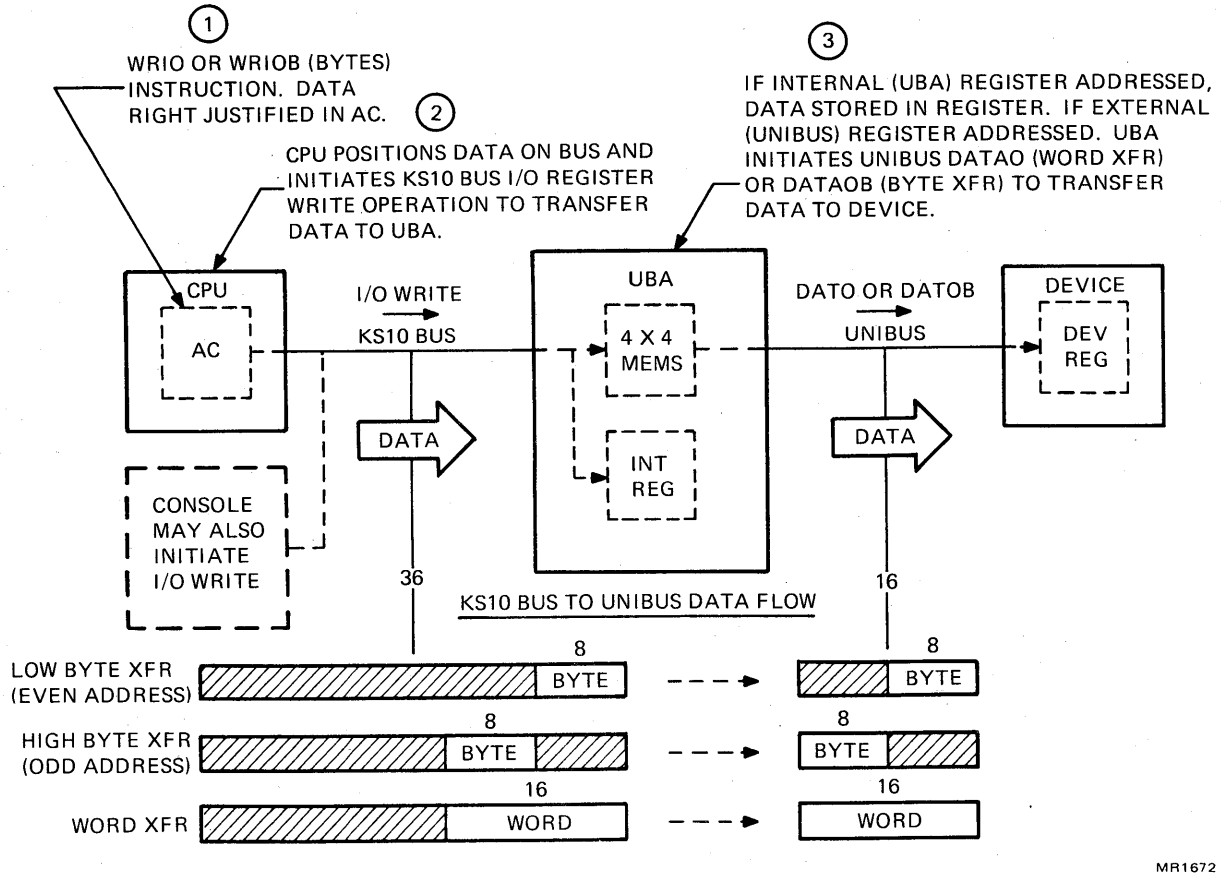


Figure 3-19 I/O Write, Data Flow

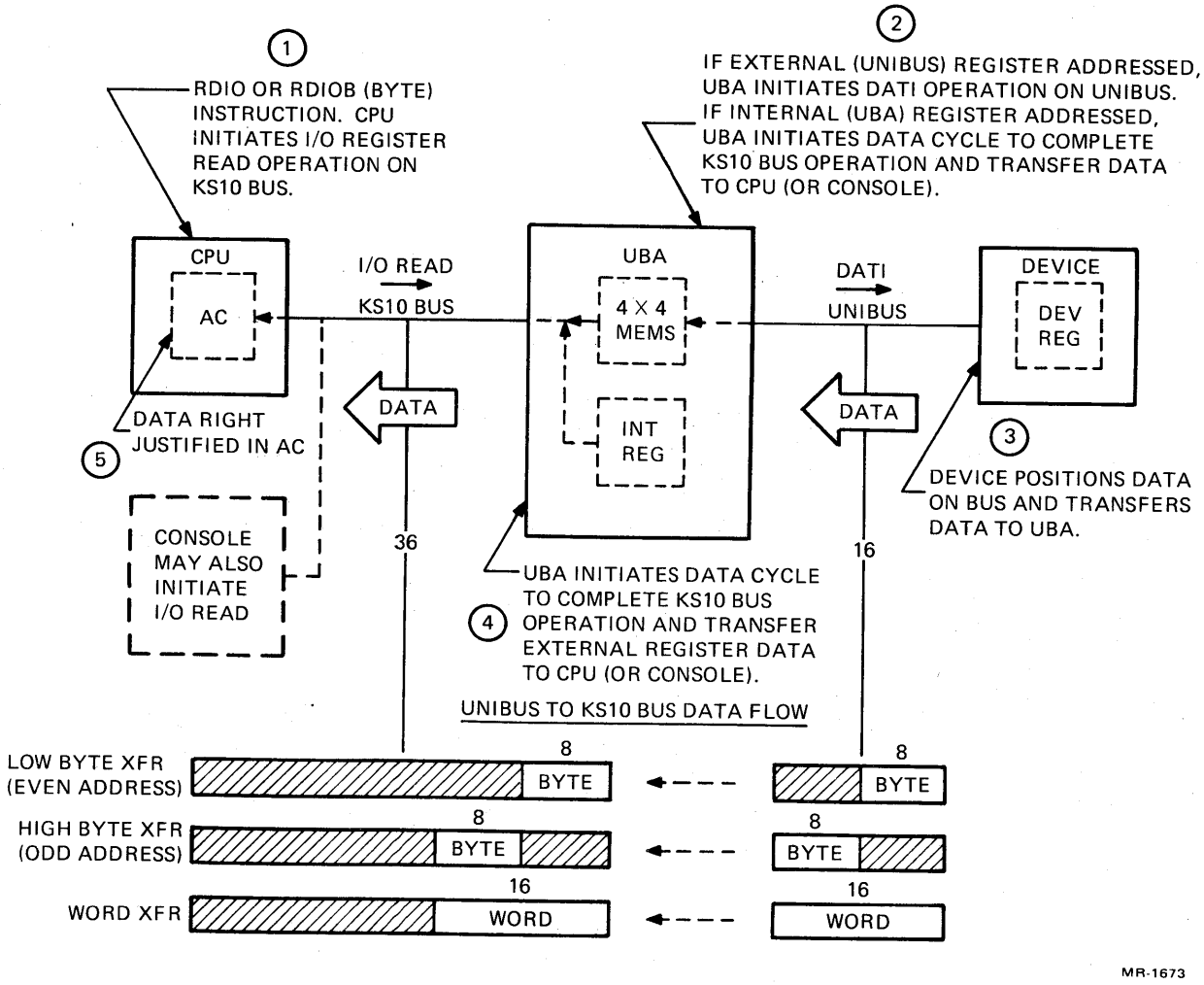


Figure 3-20 I/O Read, Data Flow

NOTE

All UBA internal and external I/O register addresses have the most significant register address bit (the 64K bit) equal to 1. If an I/O register data transfer is directed to a UBA and this address bit is equal to 0, it forces a UBA NPR data transfer cycle. This causes I/O register data to be read from, or written into, KS10 memory.

The basic sequence of operations for I/O register data transfers is as follows.

1. The CPU (when an I/O instruction is executed) or the console (when the appropriate command is given) initiates an I/O register write or read operation on the KS10 bus.

2. For an I/O register write operation, and when an external (Unibus) register is addressed, the UBA responds by loading the register data from the KS10 bus and then initiating a Unibus DATO or DATOB operation to write the word or byte into the addressed device register. When an internal (UBA) register is addressed, no Unibus action is required and the data is loaded directly into the UBA register address.

3. For an I/O register read operation and an external address, the UBA responds by performing a Unibus DATI operation (for both word and byte operations) to read the addressed register. Because the time required to retrieve the register data from the device is greater than the time allotted the CPU or console for the KS10 bus operation (three bus cycles), the UBA is disconnected from the KS10 bus during the Unibus DATI operation. As a result, when the register data is finally received from the device, the KS10 bus must be requested again, this time by the UBA. (The CPU or console requested the bus originally to initiate the operation.) The UBA then does a KS10 bus data cycle to transfer the data to the CPU or console. The UBA also performs a KS10 bus data cycle when an internal (UBA) register is addressed. In such case, however, the UBA is disconnected from the KS10 bus for only a short interval if it is granted the bus immediately. This is so because there is no delaying Unibus action, the data being readily available from the UBA register address.

3.3.1.3 PI Operation - The UBA monitors all interrupt requests (BR levels) on the Unibus and asserts PI requests (1-7) on the KS10 bus, depending on the PI channel number (PIA) loaded in the UBA's status register. (See Paragraph 3.3.2.) Both a low-level

PIA (for BR4 and BR5) and a high-level PIA (for BR6 and BR7) may be loaded, allowing one group of Unibus devices to interrupt at one PI request level, and a second group to interrupt at another PI request level. Following a device interrupt request, the UBA performs a second major PI function by allowing the Unibus device interrupt vector to be transferred to the CPU. Data flow is shown in Figure 3-21. The basic operation develops as follows.

1. When the CPU detects a PI request on the KS10 bus, it first resolves PI channel number priority; that is, more than one PI request may be asserted on the bus by the various I/O controllers, such as UBAs, and the CPU selects the highest priority (lowest numbered) channel to service.

2. The CPU then performs a KS10 bus operation to read the controller numbers interrupting on the selected channel. (More than one controller may assert the same PI request line.) In response, each interrupting controller asserts a data line corresponding to its controller number. UBA1 (controller 1) asserts data line 19 and UBA3 (controller 3) asserts data line 21.

3. After reading the interrupting controller numbers for the selected PI channel, the CPU resolves controller number priority (lowest number has highest priority) and initiates another KS10 bus operation to read the interrupt vector from or (in the case of a UBA) via the selected controller. In response, an addressed UBA initiates a Unibus interrupt operation to read the vector from the highest priority Unibus device interrupting on the PI channel being serviced. (Devices may be asserting both of the BR levels associated with the PIA, and more than one device can assert the same BR level.)

4. To initiate a Unibus interrupt operation, the UBA asserts the BG level corresponding to the highest priority BR level asserted (highest numbered BR level has highest priority). For example, if the low-level PIA is being served and both BR4 and BR5 are asserted, the UBA asserts BG5. Once the BG level is asserted, the first device on the Unibus asserting the associated BR level transfers the vector to the UBA. (The device electrically nearest the UBA has highest priority.) The UBA, in turn, transfers the vector to the CPU. As for an I/O register read operation, the UBA is disconnected from the KS10 bus during the Unibus interrupt operation. Thus, when it collects the vector from the device, the UBA must first request the KS10 bus before transferring the vector to the CPU via a data cycle.

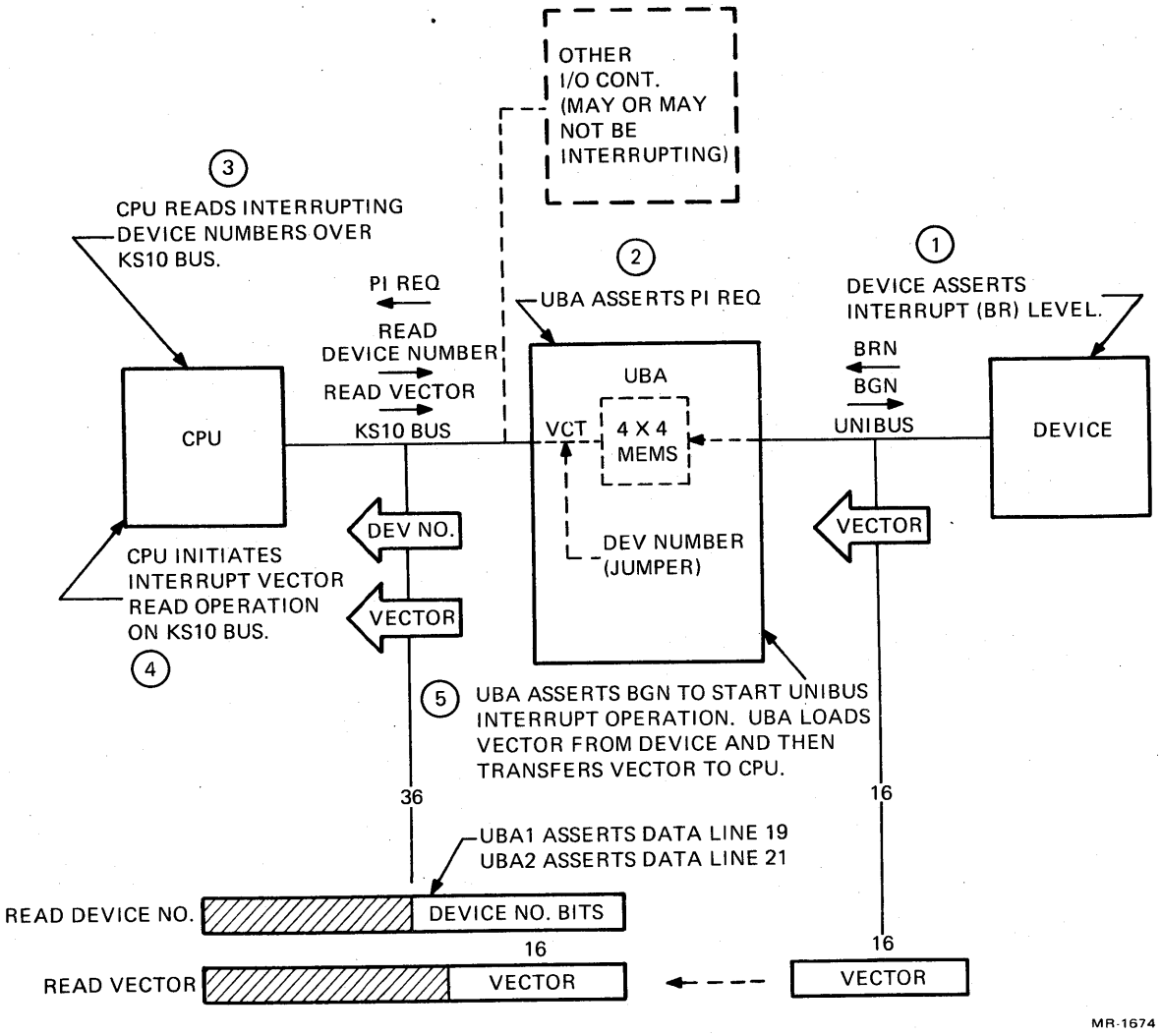


Figure 3-21 PI Operation, Data Flow

3.3.2 UBA Status and Control Registers

The UBA has the following internal registers.

Address (octal)	Register	Read/Write
763000-77	Paging RAM	R/W
763100	Status Register	R/W
763101	Maintenance Register	W

The registers may be accessed with the external I/O instruction set (WRIO, RDIO, etc.) or by the appropriate console commands (DI and EI). Note that the maintenance register (763101_8) is a write-only register.

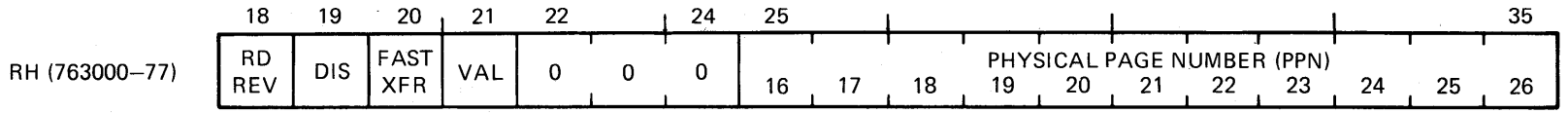
3.3.2.1 Paging RAM - The 64-location paging RAM allows a virtual address on the 18 Unibus address lines to be translated to a 20-bit physical KS10 memory address during NPR data transfers. Each RAM location contains 16 bits, 11 of which are used to specify a KS10 memory page address. The other five RAM bits are used for control purposes. Bit format and definitions for the I/O instructions accessing the RAM are given in Figure 3-22. As shown, the bit format is not the same when loading the RAM as when reading the RAM locations.

Unibus-to-memory address translation is shown in Figure 3-23. The two least significant bits of a Unibus address specify the position of the Unibus data within a memory location and are not used as part of the memory address; bit 1 specifies an odd or even word; bit 0 specifies a high- or low-order byte. (Refer to Figure 3-16.) The next nine least significant bits of a Unibus address (bits 10-2) are used directly as the nine least significant bits of the memory address (bits 27-35). This is similar to virtual-to-physical address translation in the CPU. The nine bits specify one of 512 words (that is, a word within a 512-word page). To furnish the page address, six of the remaining seven Unibus address bits (bits 16-11) select a paging RAM location. The contents (the 11-bit address) then supply the KS10 memory page address (memory address bits 16-26). The most significant bit of the Unibus address (bit 17) is not used.

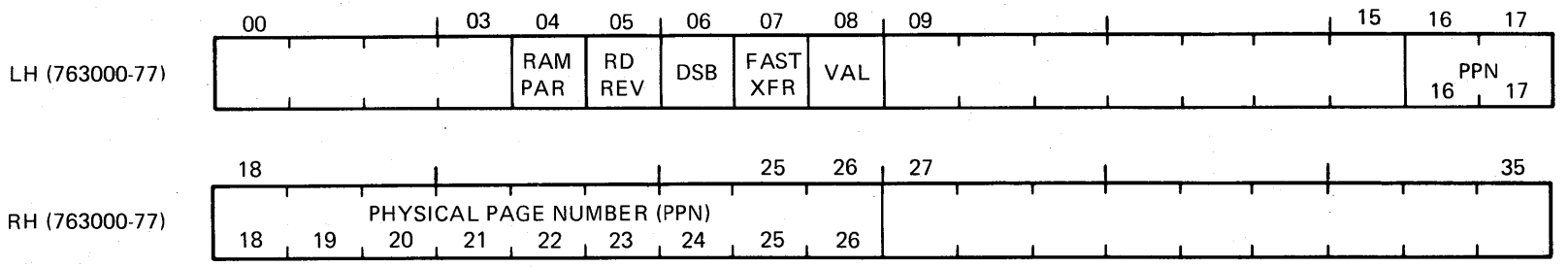
NOTE

The most significant bit of a Unibus address (the 64K bit) must be made equal to 0 for NPR data transfers. If equal to 1, a memory reference is not made, causing the Unibus device to time out, set an error flag, and terminate the device read or write operation.

UBA PAGING RAM (WRITE)



UBA PAGING RAM (READ)



BIT(S) WRT	BIT(S) RD	FUNCTION
–	04	PAGING RAM PARITY BIT
18	05	READ REVERSE
19	06	DISABLE PARITY BIT XFR TO UNIBUS
20	07	FAST TRANSFER MODE
21	08	ADDRESS IS VALID
22–24	–	MBZ (MUST BE ZERO)
25–35	16–26	PHYSICAL PAGE NUMBER

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Figure 3-22 Paging RAM

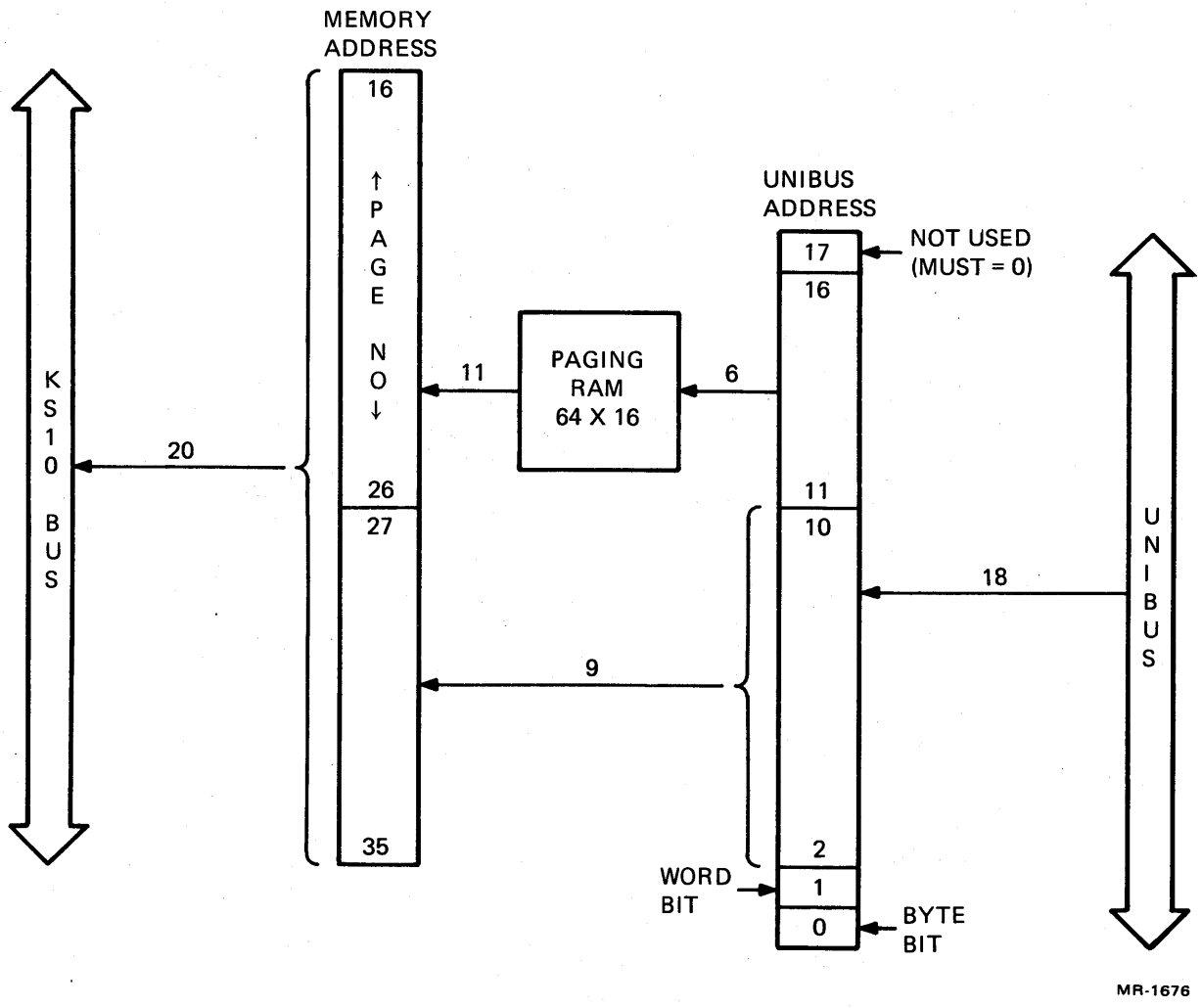


Figure 3-23 Unibus-to-Memory Address Translation

The five paging RAM control bits are as follows.

1. VALID - Indicates the physical page number is a valid address; set by the program when the paging RAM is loaded.

2. READ REVERSE (READ-PAUSE-WRITE) - Forces read-pause-write memory cycles for all NPR write (-to-memory) transfers. Allows read-reverse operations by a Unibus device by causing odd words previously loaded in memory to be read and recirculated by the UBA during even-word transfers. (Normally, even words are the first data loaded in a memory location and they are loaded directly via a memory write cycle.)

3. DISABLE - Prevents the two most significant bits of Unibus data in KS10 memory (bits 0 and 1, or bits 18 and 19) from being transferred to the Unibus data lines (17 and 16) during NPR read (-from-memory) operations. The two Unibus data lines, which are device parity error lines during non-18-bit transfers, are forced to 0 to prevent nonzero data in memory from causing false parity error indications in the Unibus device. The DISABLE bit must not be set for 18-bit word transfers.

4. FAST TRANSFER (36-BIT ENABLE) - Sets fast-transfer mode for NPR word transfers. In this mode, both odd and even words of Unibus data (a total of 36 bits) are transferred during a single KS10 memory reference.

5. RAM PARITY - Paging RAM odd parity bit; generated by hardware when the paging RAM is loaded.

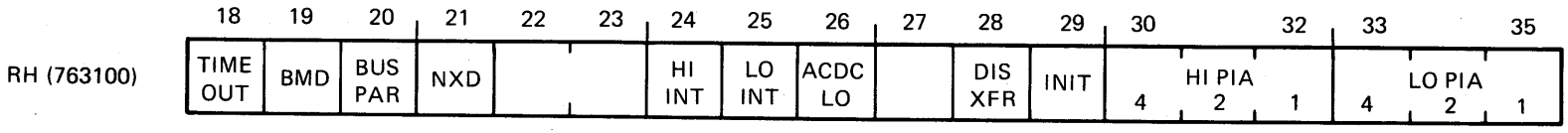
NOTE

A RAM parity error, or the absence of a RAM valid bit, detected during an NPR transfer will cause the associated Unibus device to time out, set an error flag, and terminate the device read/write operation.

3.3.2.2 **Status Register** - The UBA status register bit format and definitions are given in Figure 3-24. As shown, provision is made for indication of both high- and low-level interrupt requests (bits 24 and 25, respectively), and for the loading and indication of high- and low-level PIAs (bits 30-32 and 33-35, respectively). Provision is also made for initialization of both the UBA and the Unibus devices (bit 29 = 1). In addition, there are five error flags and a DISABLE TRANSFER control bit, as described below.

1. TIMEOUT (bit 18) - Indicates a Unibus arbitrator timeout (10 μs) or a nonexistent memory timeout (1.2 μs). The Unibus arbitrator timeout may be caused by any of the following conditions.

UBA STATUS REGISTER



BIT(S)	READ/WRITE	FUNCTION
* 18	R/W	UNIBUS ARBITRATOR TIME-OUT OR NON-EXISTENT MEMORY ADDRESS.
* 19	R/W	BAD MEMORY DATA
* 20	R/W	KS10 (BACKPLANE) BUS PARITY ERROR
* 21	R/W	NON-EXISTENT DEVICE
24	R	HIGH LEVEL INTERRUPT PENDING (BR7 AND BR6).
25	R	LOW LEVEL INTERRUPT PENDING (BR5 AND BR4).
26	R	AC OR DC LOW
28	R/W	DISABLE TRANSFER IF BMD (BIT 19 = 1).
29	W	INITIALIZE UBA AND UNIBUS DEVICES
30–32	R/W	HIGH LEVEL PIA.
33–35	R/W	LOW LEVEL PIA.

NOTE:
*WRITING A 1 BIT CLEARS THE FLAG.

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Figure 3-24 UBA Status

a. No SACK signal was received from a Unibus device after the UBA granted the Unibus to a device for an NPR or interrupt vector data transfer. This usually indicates a system malfunction.

b. No SSYNC signal was received from a Unibus device after the UBA initiated a DATO, DATOB, or DATI operation. This usually indicates a nonexistent device.

The nonexistent memory timeout is caused by the condition that no MEM BUSY signal was received after the UBA was granted the KS10 bus for a memory operation during an NPR data transfer. It usually indicates a nonexistent memory address.

The TIMEOUT error flag is cleared by writing the status register with bit 18 = 1.

2. BAD MEMORY DATA (bit 19) - Indicates uncorrectable data was read from memory during an NPR data transfer. The error may be set not only during an NPR read-from-memory data transfer (memory-read operation), but also during an NPR write-to-memory data transfer (memory read-pause-write operation). Except for an NPR read-from-memory operation when DISABLE TRANSFER (bit 28) is not set, this error prevents the UBA from generating SSYNC, causing the device controller (for example, RH11) to time out and terminate the device read or write operation. The BAD MEMORY DATA error flag is cleared by writing the status register with bit 19 = 1.

3. BUS PARITY ERROR (bit 20) - Indicates that the UBA detected a KS10 (backplane) bus parity error when it either received or transmitted bus information. Unless disabled by a console command, a BUS PARITY error causes the console module to stop the CPU clock. The BUS PARITY ERROR flag is cleared by writing the status register with bit 20 = 1.

4. NONEXISTENT DEVICE (bit 21) - Indicates that no SSYNC signal was received from a Unibus device 10 μs after the UBA initiated a DATO, DATOB, or DATI operation, and usually signifies a nonexistent device. This error condition also sets a TIMEOUT error (bit 18). The NONEXISTENT DEVICE error flag is cleared by writing the status register with bit 21 = 1.

5. AC/DC LOW (bit 26) - Indicates the assertion of a Unibus AC LOW or DC LOW (a condition sensed by the H765 power supply), or the assertion of a KS10 bus AC LOW (a condition sensed by the H7130 power supply).

3.3.2.3 Maintenance Register - The maintenance register contains a single write-only control bit as shown in Figure 3-25. CHANGE REGISTER (bit 35), when set during an I/O register read/write or interrupt vector read operation, modifies the addressing logic for the 4 X 4 memories interfacing to the Unibus so that the data received or transmitted on the bus is stored in the 4 X 4 memory locations normally used for NPR data transfers. This facilitates operation in wraparound mode, but it also allows a quick check of 4 X 4 memory operation when Unibus data is in error during normal operation. For example, if it is found that after writing and reading a Unibus device register that the register data does not match, the maintenance bit may be set and the operation repeated. If the register data then agrees, it indicates a bad 4 X 4 memory location.

3.3.3 Logical Organization

The UBA consists of the following major logic elements.

1. Data path
2. NPR control
3. I/O read/write control
4. Unibus arbitrator
5. Unibus control
6. KS10 bus control

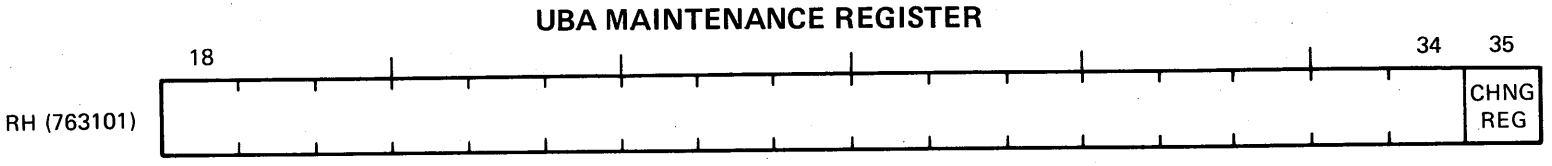
The data path (UBA circuit schematics UBA8, 9, A-C) consists of data mixers, KS10 bus tranceiver/latches, 4 X 4 IC memory elements, and Unibus drivers and receivers that are arranged to allow NPR and I/O register data to pass between the KS10 bus and the Unibus. The data path also transfers addressing information, and contains an address register to store I/O register addresses and the 64 X 16-bit paging RAM for NPR address translations.

The NPR control (UBA5 and part of UBA7) contains the control flip-flops and assorted logic to sequence NPR data transfers. It also contains the paging RAM read/write control logic and parity circuits.

The I/O read/write control (UBA4 and part of UBA7) contains the I/O command/address decoding logic, as well as the control logic necessary to sequence I/O register read/write operations for both external and internal register addresses. It also controls interrupt vector read operations.

The Unibus arbitrator (UBA1) consists of a priority encoder, latches, a counter, several one-shots, and the associated logic to detect, store, initiate, and synchronize Unibus I/O, NPR, and interrupt requests. Requests for the Unibus are honored on a priority basis (highest to lowest) in the following order.

1. NPR requests
2. I/O requests
3. Interrupt requests



BIT	FUNCTION
35	CHANGE REGISTER. MODIFIES 4 X 4 MEMORY ADDRESS.

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Figure 3-25 Maintenance Register

The arbitrator logic also detects either the successful completion of a Unibus operation or the associated error conditions (TIMEOUT and/or NXD).

The Unibus control (UBA2) contains the control logic associated with Unibus signals MSYNC, SSYNC, BBSY and INIT. It also controls the transmission of Unibus data and addressing information.

The KS10 bus control (UBA6) contains the circuitry to request the KS10 bus, initiate bus data cycles, and initiate bus command/address cycles to read/write memory. It also contains the mixer selection logic that controls the data path mixers.

3.4 EXTERNAL I/O INSTRUCTIONS

The external I/O instructions read, write, modify, and test registers in KS10 devices external to the CPU. The effective address (E) for these instructions specifies an I/O address (see Figure 3-26); the specified AC holds either register read/write data or mask data (for test or modification), depending on the instruction type. Both full-word (normal) instructions and byte instructions are implemented. The full-word instructions transfer 36 bits of data and use the full contents of an AC. The byte instructions, which are employed only when addressing Unibus device registers, transfer only eight bits of data and use only the eight rightmost bits in an AC. The various external I/O instructions are described below.

- **TIOE and TIOEB** (710_8 and 720_8) - The TIOE (or TIOEB) instruction fetches one word (or byte) from the I/O address specified by E, and ANDs the word (or byte) with the contents of the specified AC. The instruction skips if the result of the AND is zero. The contents of the AC are not modified.

- **TION and TIONB** (711_8 and 721_8) - The TION (or TIONB) instruction performs the same function as the TIOE (or TIOEB) instruction except that this instruction skips if the result of the AND is not zero.

- **RDIO and RDIOB** (712_8 and 722_8) - The RDIO (or RDIOB) instruction fetches the word (or byte) from the I/O address specified by E and stores the word (or byte) right-justified in the specified AC.

- **WRIO and WRIOB** (713_8 and 723_8) - The WRIO (or WRIOB) instruction takes the word (or byte) contained in the specified AC and transfers the word (or byte) to the I/O address specified by E.

- **BSIO and BSIOB (714_8 and 724_8)** - The BSIO (or BSIOB) instruction fetches the word (or byte) from the I/O address specified by E, ORs the word (or byte) with the contents of the specified AC, and then transfers the result back to the I/O address. The instruction(s) may be used to set selected bits in Unibus device registers. The contents of the AC are not modified.

- **BCIO and BCIOB (715_8 and 725_8)** - The BCIO (or BCIOB) instruction is similar to the BSIO (or BSIOB) instruction except that the word (or byte) read from the I/O address is ANDed with the complement of the AC contents. The instruction(s) may be used to clear selected bits in Unibus device registers. The contents of the AC are not modified.

Effective Address Calculation

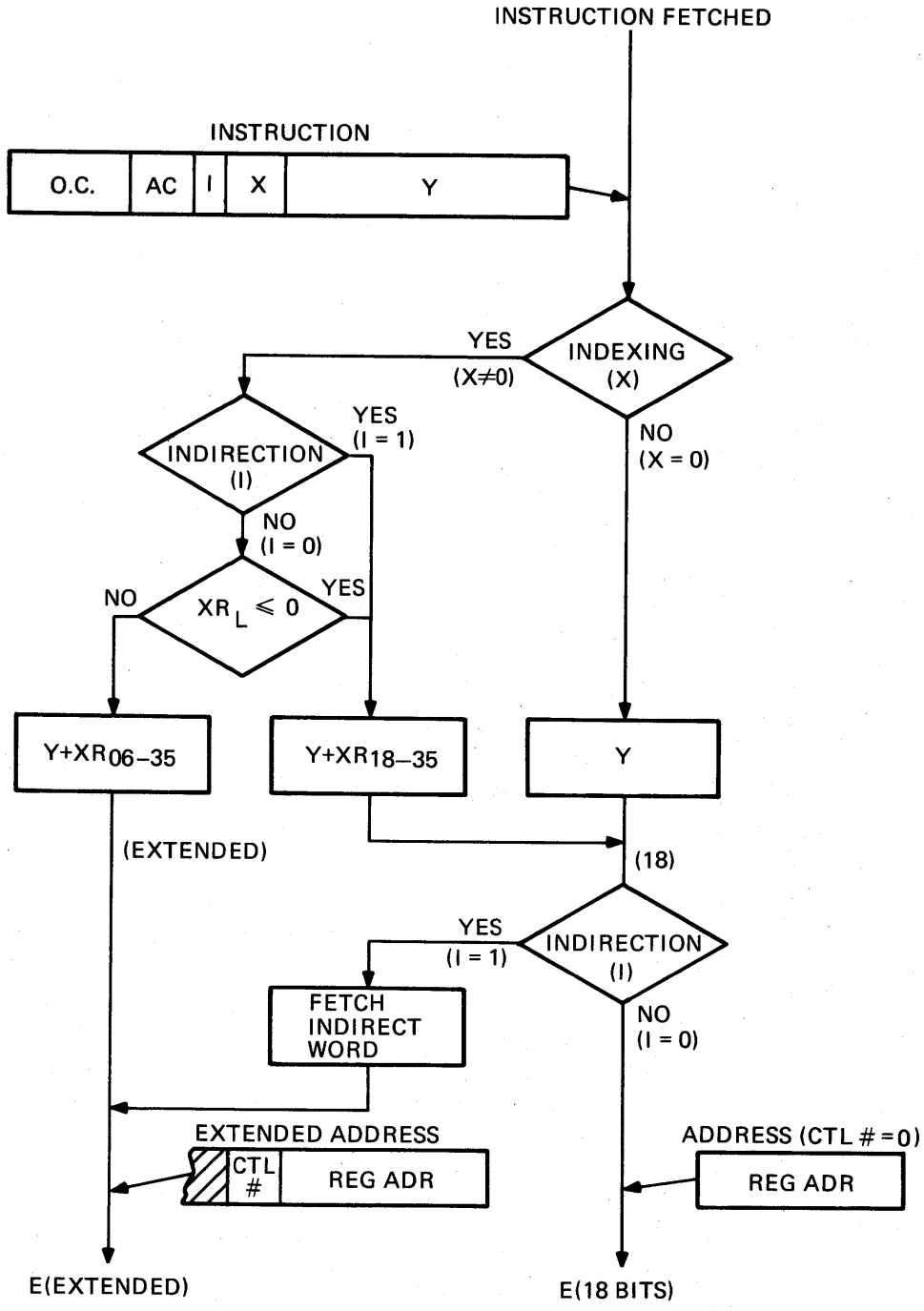
The effective address calculation for the external I/O instructions (instruction codes 710_8-727_8) is diagrammed in Figure 3-26. The calculation differs from other KS10 instructions in that the result, an I/O address, can be either an 18-bit or an extended (greater than 18-bit) address. An extended address is necessary because an I/O address consists of a 4-bit controller number plus an 18-bit register address as shown in Figure 3-27. Controller numbers 1 and 3 select a Unibus adapter (UBA), in which cases the register address selects a register in a Unibus device connecting to the addressed UBA, or it selects a register in the UBA itself. Controller number 0 is used to address KS10 registers not associated with a Unibus (for example, the memory status register).

NOTE

If the controller number is to be 0, the I/O address need not be extended. That is, an 18-bit effective address calculation results in the hardware forcing the controller number to 0.

The effective address calculation for the external I/O instructions is as follows.

1. As for the other KS10 instructions, Y is not modified if there is no indexing (X = 0). Also, if there is indexing (X ≠ 0), Y is added to the right half (bits 18-35) of the index register, but only if the left half of the index register is negative (bit 00 = 1) or if the indirect bit is set (I = 1). If the indirect bit is not set (I = 0), and if the left half of the index register is positive (bit 00 = 0), Y is added to bits 06-35 of the index register to generate an extended effective address.



NOTES:
- AC = ACCUMULATOR ADDRESS
- O.C. = OP CODE
- E = EFFECTIVE ADDRESS
- I = INDIRECT BIT
- X = INDEX REGISTER ADDRESS
- XR = INDEX REGISTER CONTENTS
- Y = ADDRESS FIELD

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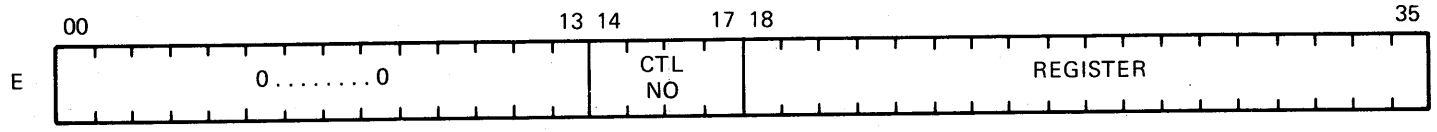
Figure 3-26 KS10 Effective Address Calculation for External I/O Instructions



CONTROLLER NUMBER	REGISTER ADDRESS (OCTAL)	REGISTER(S)
0	0-077777	NOT USED
0	100000	MEMORY STATUS REGISTER
0	100000-1-177777	NOT USED
0	200000	CONSOLE INSTRUCTION REGISTER
0	20000001-777777	NOT USED
1	0-377777	NOT USED
1	400000-777777	UNIBUS 1 (UBA AND DEVICE) REGISTERS
3	0-377777	NOT USED
3	400000-777777	UNIBUS 3 (UBA AND DEVICE) REGISTERS
2, 4-17		NOT USED

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Figure 3-27 I/O Address Format

2. Next, if an extended effective address has not been generated in the first step, the resulting 18-bit address (Y, or Y + XR 18-35) is used as the effective address, provided there is no indirection (I = 0). If there is indirection (I = 1), the 18-bit address is used to fetch an indirect word from memory.

3. When an indirect word is fetched from memory, bits 14-35 of the contents are unconditionally used to generate an extended address. Unlike the address calculation for the rest of the KS10 instruction set, the indirect word is not treated as another instruction word. There is only one level of indirection employed for external I/O instructions.

Instructions using indexed or indirect addressing must be used to address controllers other than 0 (which require an extended address). Examples of indexed and indirect addressing follow. In both examples, the status register (register address = 763100_8) in UBA 1 (controller no. = 1) is read into an AC with the RDIO external I/O instruction.

Example 1 - Indexed Addressing

RDIO AC, 763100 (5) where the contents of index register = 1000000.

The index register contents (the controller number) are added to Y (the register address) to give the extended I/O address 1736100.

Example 2 - Indirect Addressing

RDIO AC, @ 100 where the contents of 100 = 1763100.

An indirect word fetch of location 100 is made and the contents are used to generate the extended I/O address 1763100.

CHAPTER 4
MAINTENANCE

4.1 INTRODUCTION

Maintenance of the PCL20 is limited to circuit board replacement. Fault isolation is done by running and interpreting the diagnostics.

4.2 SPECIAL TEST EQUIPMENT

The only special test equipment required is a Tektronix Model 465 or an equivalent oscilloscope.

4.3 DIAGNOSTIC SOFTWARE

The following diagnostics are used for checkout, acceptance and debugging of PCL20 systems.

MAINDEC-10-DSPCA PCL20 STANDALONE TEST

This test is used to diagnose problems within a PCL11-B unit. It is composed of three parts: a transmitter test, receiver test, and loop test. The loop test uses the TTL TDM bus driver chips to send messages from the transmitter to the receiver. This test does not send any data through the differential transceivers on the M8003 module. This test is EXEC mode only.

The PCL11-B should be disconnected from the TDM bus to ensure correct operation of the test. This may be accomplished by using the switch on the M8003 to turn the unit off-line, or else the cables may be disconnected from the connectors on the M8003.

MAINDEC-10-DSPCB PCL20 EXERCISER

This program runs in all DECSYSTEM-2020s that form part of the PCL20 network. It is an EXEC/USER mode program to test each unit and may be run with or without operating systems. This exerciser is intended to be run concurrently with the exerciser running in the other computers in the network.

NOTE

A properly configured TOPS-10 operating system must run in user mode.

4.4 PREVENTIVE MAINTENANCE

When nodes are removed from the PCL20 system for preventive or corrective maintenance, off-line diagnostics may be run on the PCL11-B to ensure it is still performing correctly. For this purpose, use the standalone test. Use the exerciser to isolate system and/or network problems.

4.5 CORRECTIVE MAINTENANCE

If an error occurs in a system, isolate the problem to one unit and remove it from the system for off-line debugging. Once a unit has been removed from the system, the standalone test may be used to complete the problem solution. Refer to the PCL11-B option description (YC-A20TC-00 Section 5) for information on maintenance techniques.

The PCL20 communication system is designed to allow removal of any unit from the TDM bus without fatal errors occurring in units that remain. This is accomplished by a T-junction connector on the BC20K cable. Also, any unit in the system may be powered down without causing problems in the system. A detailed troubleshooting flow chart appears in Paragraph 4.5 of the PCL11-B Communications Systems Installation and Maintenance Guide, YC-A20TC-02.

PCL20 Parallel Communications Link
User's Guide
EK-PCL20-UG-001

Reader's Comments

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