KL10 Maintenance Guide

Company Confidential

Volume I

digital

EK-OKL10-MG-003

KL10
Maintenance Guide
Volume I

Prepared by Educational Services
of
Digital Equipment Corporation
Marlborough, MA

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Printed in U.S.A.

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To the Reader:

IMPORTANT - This guide contains information for internal use only and is intended for use by DIGITAL Field Service engineers only. Refer to the Field Service Methods and Procedures Manual for company policy pertaining to internal information.

OBJECTIVE - The objective of this guide is to organize and present the maintenance information necessary to resolve 80% of all KL10 hardware malfunctions.

To properly maintain and improve this guide in subsequent revisions, we need feedback concerning accuracy and clarity. This communication is very helpful to your fellow engineers. Please forward any corrections, suggestions, and comments that would improve this guide to:

Customer Services, Systems Engineering (CSSE)
RE: KL10 Maintenance Guide
MR01-1/S35

ORGANIZATION - Volume I contains general maintenance information pertaining to the KL10. The volume is divided into tabbed sections with separate tables of contents as follows.

1. GENERAL INFORMATION consists of miscellaneous maintenance information that cannot be classifed and filed in any of the other hardware sections.

2. SWITCHES AND JUMPERS contains information pertaining to hardware switch positions and jumper connections.

3. TABLES AND MAPS describes the process tables and bit maps associated with the KL10 mainframe and peripheral equipment.

4. CHECKS AND ADJUSTMENTS consists of check and adjustment procedures performed during preventive and corrective maintenance.

5. DIAGRAMS AND MULS contains block diagrams, power supply layouts, and module utilization lists associated with KL10-based systems.

6. MULTI-CPU contains maintenance and diagnostic information specific to multiprocessor systems.

7. DECnet-10/20 contains system hardware and software information.

The information in each hardware section is arranged according to unit and subsystem (i.e., CPU, memory, disk, tape, and I/O).

Volume II contains additional hardware and software information related to the KL10. The volume is divided into tabbed sections with separate tables of contents as follows.

1. COMPUTER INTERCONNECT contains descriptions of the card cage, module locations, switch settings, bit/error formats, diagnostics, and label information.

2. NETWORK INTERCONNECT provides descriptions of the card cage, module locations, switch setting, bit/error formats, diagnostics, and label information.

3. HSC SUBSYSTEM consists of RA81, RA60, and HSC50 Error Codes.

4. CLUSTER TROUBLESHOOTING includes procedures for fault isolation on the cluster level.

5. RP07/RP20 presents RP07 registers and RP20 FSC, jumper, routines, error stops, and other information.

6. S/X BUS contains a general description, installation, and operation information.

7. ARM-10LS provides installation, operation, and memory fault isolation information.

8. MAINTENANCE SOFTWARE consists of information related to the DIACON, KLDCP, KLDCPU, MEMCON, TRACON, DIAMON, DDT, D20MON programs.

9. SYSTEM SOFTWARE includes information on typical operating systems and command formats.

10. RSX-20F presents information on programs SYSLIB-20F and PARSER, in addition to stop/error codes.

11. TOPS-10 supplies information on TOPS-10, DECnet-10, GALAXY-10, and PIP programs.

12. TOPS-20 contains system program, command summary/format, and error message information.

13. NOTES provides blank pages for note taking.

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IMPORTANT TELEPHONE NUMBERS

Digital Diagnostic Center (10/20/ 11/70, and VAX)

NORAM Colorado Springs, Colorado

303-599-4000 This number should be used by:

1. Canadian customers to log a request for service.

2. All field engineers to request either a KLINIK link or technical assist.

8-522 + ext. This is the DIGITAL Telephone Network (DTN) code for NORAM DDC. This number plus the appropriate extension should be used to contact DDC personnel.

303-599-4111 This number should be used to contact the DDC switchboard operator.

LCG Resources

Digital Diagnostic Center
U.S. Area Field Support Systems Support Center
Customer Support Center
Digital Equipment Corporation
4405 North Chestnut Street
Colorado Springs, Colorado 80907-3812
Telephone: 1-800-525-6570

DIGITAL DIAGNOSES CENTER (DDC)

The DDC is staffed 24 x 7 and provides the following support:

- Initial System Diagnoses
- Technical Support for Field Engineer
- Remote Support Referral/Screening
- Limited Dump, Analysis/Screening
- Acceptance Testing
- Klinik Verification
- Inclusion in Action Plans
- System Monitoring and Repair Certification
- Preventive Maintenance (PM) - Diagnostics
- Pro-Active Remote Diagnoses (PARD)
- Special Requests

LCG Remote SUPPORT

The LCG Remote Support Group is currently staffed with T7S level Support Engineers M - F (0600 to 1800 MT), with standby coverage for all other hours. Future call loads may dictate a 24 x 7 coverage.

LCG Remote Support provides First Level Telephone Support on the KL and KL specific options, and limited support on KS, KA, and KI options.

Options that are across product lines (Disk, Tapes, etc.) may be supported by the LCG Remote Support Group, or by the Cross Product Line Remote Support Group, depending on the option and the expertise of the engineer available.

- Technical Support - KL and KL specific options, and limited support on KS, KA, and KI options.

LCG CRASH ANALYSIS

The Crash Analysis Group is staffed M - F (0800 to 1800 MT)

- Crash Analysis - RSX20F, TOPS20, and TOPS10

US AREA THIRD LEVEL SUPPORT

Provides third level support on KL systems.

TELEPHONE SUPPORT CENTER (TSC)

The TSC is staffed M - F (0800 to 1800 MT) with standby coverage all other hours.

Software Support is provided to customers having software contracts with the TSC.

- The TSC does software analysis of Operating Systems and Layered Products.

US AREA LIBRARY

The Library is staffed M- F (0600 to 1800 MT). They provide Field Service with Technical Documentation.

HOW TO YOU ACCESS THE ABOVE RESOURCES?

To invoke any resource at the Colorado Springs Customer Support Center you dial 1-800-525-6570 and ask for the specific group you desire.

DIGITAL DIAGNOSES CENTER (DDC)

If the DDC is contacted by the customer, the Branch is immediately contacted by the DDC to inform them of the call. The customer will be contacted within approximately fifteen minutes and the engineer will begin working the call. The Branch will be notified within approximately one hour with the results or status of the call.

If the Branch Engineer needs assistance in working the call he will inform the DDC. The DDC will then change the call type to a Technical Support type call.

Once the call is four hours old, and the DDC has not been able to affect a fix, it will then be turned over to Remote Support by the DDC Engineer.

LCG REMOTE SUPPORT

If the Remote Support Group is contacted by either the Field Service Engineer, Product Support Engineer, or the DDC Engineer to help in the resolution of a problem, they will work with the Field Service or Product Support Engineer (on-site) to resolve the problem.

When Remote Support is requested, it is assumed that an engineer has worked the call and been unable to affect a fix.

After Remote Support has worked on a call for three hours, the

District Product Support Manager/Engineer will be notified of the problem and the call turned over to them. If they request, the Remote Support Group may assist the District in the established Action Plan (set up by the Branch and District) with telephone support (depending on the groups call load and available staff).

LCG CRASH ANALYSIS

All initial requests for crash analysis will be screened through the DDC. Once the engineer performing the crash analysis has made contact with the Branch Engineer, then all dumps relating to that specific problem may be referred directly to the LCG Crash Analysis Group.

Requests for crash analysis are handled on a first-in first-out basis, and also on the availability of an engineer to perform the analysis. However, support level requests have priority over those of a routine nature.

When calling for Crash Analysis it is assumed that an engineer has a system with a recurring problem that he/she has been unable to diagnose using other methods of troubleshooting. It is also assumed that correct telephone numbers, account and passwords are provided, and that sufficient privileges are available to access the required files.

US AREA THIRD LEVEL SUPPORT

This level of support is invoked by the Regional Product Support Unit Manager.

TELEPHONE SUPPORT CENTER (TSC)

Software support is provided to customers having a valid access number and to a specific contact person.

Support is also provided to Field Software Specialist, Field Service, DDC, and Remote Support Engineers.

US AREA LIBRARY

Documentation support is provided to all Field Service Engineers.

EUROPEAN LCG SUPPORT

Telephone Numbers

Hotline	(33)	(93)	74 72 50
Cupid	(33)	(93)	74 45 05
LCG Area Manager	(33)	(93)	74 24 24
Backup Support Manager	(33)	(93)	74 24 24

SITE	SITE CONTACT	OPERATOR NUMBER
		KLINIK NUMBER

MR-2329

BOOTSTRAP ROMS

BM873YH

First Used On - DECsystem-10XX console front end.

Current Usability - DECsystem-10XX console front end, DECSYSTEM-20XX console front end.

Summary of Features

1 Switch register
2 RP04/05/06 disk bootstrap
3 RX11 floppy disk bootstrap
4 TC11 DECtape bootstrap
5 Error retry
6 Bootstrap parameters
7 Parameter entry

Button Addresses

1 773000 Switch register
2 773030 Disk
3 773020 Floppy/DECtape
4 773554 DTE20

Other Entry Locations

773300 TC11 DECtape bootstrap. Used if DECtape bootstrap (unit 0) desired and RX11 floppy exists in configuration.

BM873YJ

First Used On - DECSYSTEM-20XX communications front end.

Current Usability - DECsystem-10XX console front end, DECSYSTEM-20XX console front end, DECsystem-10XX communications front end, DECSYSTEM-20XX communications front end.

Summary of Features

1 Switch register
2 RP04/05/06 disk bootstrap
3 RX11 floppy disk bootstrap
4 TC11 DECtape bootstrap
5 DTE20 bootstrap and dump
6 DL11 asynchronous line bootstrap
7 Error retry
8 Bootstrap parameters
9 Parameter entry
10 PDP11/34 support

Button Addresses

1 773220 Switch register (halts)
1 773000 Switch register (does not halt)
2 773030 Disk
3 773020 Floppy/DECtape/DL11
4 773230 DTE20

Other Entry Locations

773214 TC11 DECtape bootstrap. Used if DECtape bootstrap (unit 0) desired and RX11 floppy disk exists in configuration.

773530 DL11 asynchronous line bootstrap. Used if DL11 bootstrap desired and either RX11 floppy disk on TC11 DECtape exists in configuration.

To make any terminal on the first DH11 act as the console terminal, select the line number using the switches on the 11/40. Bits 14-11 are the line numbers. The line numbers start at line 0.

	Bits 14-11
300 baud	XXX277 (address in the switches)
1200	XXX317
2400	XXX337
4800	XXX347
9600	XXX357

VECTOR AND ADDRESS ASSIGNMENTS FOR FRONT END OPTIONS

Unit No.	DN11	DQ11	DM11BB	DH11	DTE20	LP20	CD20	CTY DL11-C	DL11-E
01	775200 660	760230 520	770500 320	760020 330	774400 774	775400 754	777160 230	777560 60	775610 300
02	775210 664	760240 530	770510 340	760040 350	774440 770	775420 750			
03	775220 670	760250 540	770520 360	760060 370	774500 764				
04	775230 674	760260 550	770530 400	760100 410	774540 760				
05	775240 700	760270 560	770540 420	760120 430					
06	775250 704	760300 570	770550 440	760140 450					
07	775260 710	760310 600	770560 460	760160 470					
08	775270 714	760320 610	770570 500	760200 510					
09	775300 720	760330 620							
10	775310 724	760340 630							
11	775320 730	760350 640							
12	775330 734	760360 650							
13	775340 740								
14	775350 744								
15	775360 750								
16	775370 754								

DL11-E		RH11	
fe1	175630 740	RH11	176700 254
fe2	175640 730	RX11	177170 264
fe3	175650 720		

UNIBUS PIN ASSIGNMENTS
(BY PIN NUMBERS)

AA1	INIT L
AA2	POWER (+5 V)
AB1	INTR L
AB2	GROUND
AC1	DOO L
AC2	GROUND
AD1	DO2 L
AD2	DO1 L
AE1	DO4 L
AE2	DO3 L
AF1	DO6 L
AF2	DO5 L
AH1	DO8 L
AH2	DO7 L
AJ1	D10 L
AJ2	DO9 L
AK1	D12 L
AK2	D11 L
AL1	D14 L
AL2	D13 L
AM1	PA L (D16 L)
AM2	D15 L
AN1	GROUND
AN2	PB L (D17 L)
AP1	GROUND
AP2	BBSY L
AR1	GROUND
AR2	SACK L
AS1	GROUND
AS2	NPR L
AT1	GROUND
AT2	BR 7 L
AU1	NPG H
AU2	BR 6 L
AV1	BG 7 H
AV2	GROUND
BA1	BG6 H
BA2	POWER (+5 V)
BB1	BG 5 H
BB2	GROUND
BC1	BR 5 L
BC2	GROUND
BD1	GROUND
BD2	BR 4 L
BE1	GROUND
BE2	BG 4 H
BF1	ACLO L
BF2	DCLO L
BH1	AO1 L
BH2	AOO L
BJ1	AO3 L
BJ2	AO2 L
BK1	AO5 L
BK2	AO4 L
BL1	AO7 L
BL2	AO6 L
BM1	AO9 L
BM2	AO8 L
BN1	A11 L
BN2	A10 L
BP1	A13 L
BP2	A12 L
BR1	A15 L
BR2	A14 L
BS1	A17 L
BS2	A16 L
BT1	GROUND
BT2	C1 L
BU1	SSYN L
BU2	CO L
BV1	MSYN L
BV2	GROUND

UNIBUS PIN ASSIGNMENTS
(BY SIGNAL NAME)

AOO L	BH2
AO1 L	BH1
AO2 L	BJ2
AO3 L	BJ1
AO4 L	BK2
AO5 L	BK1
AO6 L	BL2
AO7 L	BL1
AO8 L	BM2
AO9 L	BM1
A10 L	BN2
A11 L	BN1
A12 L	BP2
A13 L	BP1
A14 L	BR2
A15 L	BR1
A16 L	BS2
A17 L	BS1
ACLO L	BF1
BBSY L	AP2
BG4 H	BE2
BG5 H	BB1
BG6 H	BA1
BG7 H	AV1
BR4 L	BD2
BR5 L	BC1
BR6 L	AU2
BR7 L	AT2
CO L	BU2
C1 L	BT2
DOO L	AC1
DO1 L	AD2
DO2 L	AD1
DO3 L	AE2
DO4 L	AE1
DO5 L	AF2
DO6 L	AF1
DO7 L	AH2
DO8 L	AH1
DO9 L	AJ2
D10 L	AJ1
D11 L	AK2
D12 L	AK1
D13 L	AL2
D14 L	AL1
D15 L	AM2
GROUND	AB2
GROUND	AC2
GROUND	AN1
GROUND	AP1
GROUND	AR1
GROUND	AS1
GROUND	AT1
GROUND	AV2
GROUND	BB2
GROUND	BC2
GROUND	BD1
GROUND	BE1
GROUND	BT1
GROUND	BV2
INIT L	AA1
INTR L	AB1
MSYN L	BV1
NPG H	AU1
NPR L	AS2
PA L (D16 L)	AM1
PB L (D17 L)	AN2
+5 V*	AA2
+5 V*	BA2
SACK L	AR2
DCLO L	BF2
SSYN L	BU1

NOTES

1. +5 V is wired to these pins to supply power to the bus terminator only.

2. +5 V should never be connected via the Unibus between system units.

GENERAL POWER SUPPLY SPECIFICATIONS

The following voltage measurements are to be made from the backplane of the option.

POWER SUPPLY TYPE	OUTPUT	TOLERANCE MAXIMUM	TOLERANCE MINIMUM	MAXIMUM RIPPLE IN MILLIVOLTS
702		VARIABLE		600
703	+10	+11.0	+9.4	300
	+1.8	+1.9	+1.7	N/A
	-3.0	-3.15	-2.85	N/A
705	+10	+11.0	+9.4	300
	-15	-16.5	-14.5	700
706	+50	+54.0	+49.0	1500
723	+8	+9.5	+7.8	600
725	-15	-18.0	-14.7	900
728	+10	+11.0	+9.5	700
	-15	-16.0	-14.5	700
732		VARIABLE		600
739	+53	+55	+52	250
	+65	+65	+63	250
742/7420	+25 V	+30	+20	N/A
	-15	-16.5	-13.5	N/A
	+3	+3.5	+2.5	N/A
744/7440	+5	+5.05	+4.95	150
745	-15	-15.05	-14.95	450
754	+20	+20.2	+19.8	450
	-5	-5.05	-4.95	150
761	-2	NONE		
	-5.2	NONE		
770	+15	+15.05	+14.95	450
778	-15	-16.5	-14.5	700
7131/7131A	+5	+5.07	+4.93	50
	+12	+12.18	+11.82	100
	-2	-2.03	-1.97	50
	-5.2	-5.28	-5.12	50

KL10-BASED SYSTEM AND PROCESSOR DESIGNATIONS

The following tables summarize the differences between the various KL10-based DECsystem-10, DECSYSTEM-20, and KL10 processors. Consult the Option/Module List for a complete list of the differences.

KL10 System Designations

Designation	Description
1080	KL10-A(PA) running TOPS-10
1088	Dual processor (1080) system
1090	KL10-B(PA) or KL10-D(PV) running TOPS-10
1090T	KL10-BC(PA) running TOPS-20 (ARPANET system only)
1091	KL10-E/R(PV) with cache running TOPS-10
1095	KL10-E/R(PW) with MCA25 and MG20
1099	SMP multiprocessor (1090) system
2040	KL10-C(PA) or KL10-E(PV) running TOPS-20
2050	KL10-C(PA) or KL10-E/R(PV) with cache running TOPS-20
2060	KL10-E/R(PV) with MOS memory
2065	KL10-E/R(PW) with MCA25 and MG20

KL10 Processor Designations

Designation	PV/ PW	FE TYPE	CACHE	INT CHAN	MAX NO. OF DTEs	MAX NO. OF RH20s	DIA	DMA
KL10-A	NO	10	YES	NO	1	0	YES	YES
KL10-B	NO	10	YES	YES	4	8	YES	YES
KL10-BC	NO	20	YES	YES	4	8	YES	YES
KL10-C	NO	20	OPTIONAL	YES	4	8	NO	NO
KL10-D	YES	10	YES	YES	4	8*	YES	YES
KL10-E	YES	20	OPTIONAL	YES	4	8*	OPT	OPT
KL10-R	YES	20	OPTIONAL	YES	4	8*	OPT	OPT

NOTES

1. KL10-PA (Model A) — A basic ECL processor with slots for cache and internal channels. Unofficially, this processor is referred to as the Model A machine.

2. KL10-PV (Model B) — A KL10-PA which has been modified to include extended addressing, more extensive microcode, and a faster clock. Unofficially, this processor variation is referred to as the Model B machine.

3. KL10-PW (Model B) — A KL10-PV which has been modified to enable support of MCA25.

*Maximum number of RH20s will decrease to 4 with installation of either a CI20 or an NIA20.

KL10A, B, or C MODEL A(PA) SYSTEM REVISION
VRS MODULE REVISION COMPATIBILITY

MODULE TYPE	CPU-PA MODULE REVISION COMPATIBILITY 10	10A	10B	11	12-12D
M8510	A	A	A	A	A
M8511	B,C	B,C	B,C	B,C	B,C
M8512	A,B,C	A,B,C	A,B,C	A,B,C	A,B,C,
M8513	D1,F	D1,F	D1,F	D1,F	D1,F
M8516	D,E	D,E	D,E	D,E	D,E
M8517	B	B	B	B	B
M8518	B	B	B	B	B
M8519	A,B,C	A,B,C	A,B,C	A,B,C	A,B,C
M8520	D	D	D	D	D
M8522	A	A	A	A	A
M8523	B,C	B,C	B,C	B,C	B,C
M8524	D,E	D,E	D,E	D,E	D,E
M8525	E,F,H	E,F,H	E,F,H	E,F,H	E,F,H
M8526	F<H	F<H	F<H	F<H	F<H
M8527	E	E	E	E	E
M8528	B	B	B	B	B
M8529	C,C1,D	C,C1,D	C,C1,D	C,C1,D	C,C1,D
M8530	D	D	D	D	D
M8531	B,C	B,C	B,C	B,C	B,C
M8532	D,E	D,E	D,E	D,E	D1,F
M8537	C,D	C,D	C,D	C,D	C,D
M8538	C,D	C,D	C,D	C,D	C,D
M8539	B	B	B	B	B

MODULE TYPE	CACHE MODULE REVISION COMPATIBILITY 10	10A	10B	11	12-12D
M8514	A	A	A	A	A
M8515	B	B	B	B	B
M8521	A	A	A	A	A

MODULE TYPE	CACHE SUBSTITUTE MODULE REVISION 10	10A	10B	11	12-12D
M8549YE	A	A	A	A	A
M8549YF	A	A	A	A	A
M8549YH	B	B	B	B	B

MODULE TYPE	CHANNEL MODULE REVISION COMPATIBILITY 10	10A	10B	11	12-12D
M8533	C	C	C	C	C
M8534	C,D	C,D	C,D	C,D	C,D
M8535	C,D	C,D	C,D	C,D	C,D
M8536	D,E	D,E	D,E	D,E	D,E

MODULE TYPE	CHANNEL SUBSTITUTE MODULE REVISION 10	10A	10B	11	12-12D
M8549YA	A	A	A	A	A
M8549YC	A	A	A	A	A
M8549YD	B	B	B	B	B

MODULE TYPE	RH20/DTE MODULE REVISION COMPATIBILITY 10	10A	10B	11	12-12B
M8552	E,F	E,F	E,F	E,F	E,F
M8553	H,J,K,L	H,J,K,L	H,J,K,L	H,J,K,L	H,J,K,L
M8554	D,F	D,F	D,F	F	F
M8555	C,D,E	C,D,E	C,D,E	D,E	D,E
M8556	C,D<E<F	C,D<E<F	C,D<E<F	D<E<F	E
M8557	C	C	C	D	D1,E
M8559	A	A	A	A	A

MODULE TYPE	DMADIA MODULE REVISION COMPATIBILITY 10	10A	10B	10B	12-12A
M8550	B,C	B,C	B,C	B,C	B,C
M8551	C	C	C	C	C
M8558	B,C,D	B,C,D	B,C,D	B,C,D	B,C,D
M8560	B,C	B,C	B,C	B,C	B,C
M8563	D,D1	D,D1	D,D1	D,D1	D1
	E,F	E,F	E,F	E,F	F

KD10D, E, or R MODEL B(PV) SYSTEM REVISION VRS
MODULE REVISION COMPATIBILITY

MODULE TYPE	CPU-PV MODULE REVISION COMPATIBILITY 2	2A	3	4-4	5
M8512	B,C	B,C	B,C	B,C	B,C
M8513YA	B	B	B	B	B
M8514	A	A	A		
M8515	B	B	B		
M8516	D,E	D,E	D,E	D,E	D,E
M8517	B	B	B	B	B
M8518YA	A	A	A	A	A
M8519	C	C	C	C	C
M8520YA	A	A	A	A	A
M8521	A	A	A		
M8522	A	A	A	A	A
M8524	D,E	D,E	D,E	D,E	D,E
M8525	H	H	H	H	H
M8526YA	B	B	B	B	B
M8529YA	A	A	A	A	A
M8531YA	A	A	A	A	A
M8532	D,E	D,E	D,E	D1,F	
M8532YA					A
M8533	C	C	C	C	C
M8534	C,D	C,D	C,D	C,D	C,D
M8535	D	D	D	D	D
M8536	E	E	E	E	E
M8537	D	D	D	D	D
M8538	C,D	C,D	C,D	C,D	C,D
M8540	A	A	A	A	A
M8541	A	A	A	A	A
M8542	A	A	A	A	A
M8543	A	A	A	A	A
M8544	A	A	A	A	A
M8545	A	A	A	A	A
M8548	A	A	A	A	A

MODULE TYPE	CACHE SUBSTITUTION MODULE REVISION 10A	10B	11	4-4D	
M8549YA	A	A	A	A	A
M8549YC	A	A	A	A	A
M8549YD	B	B	B	B	B
M8549YE	A	A	A		
M8549YF	A	A	A		
M8549YH	B	B	B		

MODULE TYPE	MCA25 LARGER CACHE/PAGER			4	5
M852				A1	A1
M853				A1	A1
M854				A1	A1
M855				A1,A2	A1,A2
M856				A1	A1
M857				A1	A1

MODULE TYPE	RH20/DTE MODULE REVISION COMPATIBILITY 10A	10B	11	12A-12B	
M8552	E,F	E,F	E,F	E,F	E,F
M8553	J,K,L	J,K,L	J,K,L	J,K,L	J1,M
M8554	F	F	F	F	H
M8555	C,D,E	C,D,E	D,E	D,E	D,E
M8556	C<D<E<F	C,D<E<F	D<E<F	E,H	E,H
M8557	C	C	D	D1,E	D1,E
M8559	A	A	A	A	A

MODULE TYPE	DMADIA MODULE REVISION COMPATIBILITY 10A	10B	11	12-A	
M8550	B,C	B,C	B,C	B,C	B,C
M8551	C	C	C	C	C
M8558	C,D	C,D	C,D	C,D	C,D
M8560	C	C	C	C	C
M8563	D1,F	D1,F	D1,F	D1,F	D1,F

NOTE

Refer to KL REV (purple microfiche) for future revision level changes. For KL10-R, see KL10-R RM.

KL10-PA DRAWING INDEX

Module Type	Index Name	Module Description
M8563	AI1	ADAPTER INTERFACE DM20 BOARD 2
	AI2	ADDRESS BUFFERS DM20 BOARD 2
	AI3	BUSS SELECTION DM20
	AI4	REQUEST LOGIC DM20 BOARD 3
	AI5	TIMING LOGIC DM20 BOARD 2
M8539	APR1-6	APR BOARD
	APR7	APR POWER, GND, CAPS
M8559	CDS3	I/O BOX CLOCK DISTRIBUTION
M8514	CHA1	CACHE DIRECTORY 0, 1 BITS 14-25
	CHA2	CACHE DIRECTORY 2, 3 BITS 14-25
	CHA3	CACHE DIRECTORY BIT 26 AND WRITTEN 1
	CHA4	CACHE DIRECTORY PARITY BITS
	CHA5	CACHE DIRECTORY POWER, GND, CAPS
	CHA6	CACHE DIRECTORY TERMINATORS
M8521	CHD1	CACHE DATA BITS [N] - [N+02]
	CHD2	CACHE DATA BITS [N+03] - [N+05]
	CHD3	CACHE DATA BITS [N+06] - [N+08]
	CHD4	CACHE DATA ADDRESSING LOGIC
	CHD5	CACHE DATA PARITY BITS
	CHD6	CACHE DATA POWER, GND, CAP
	CHD7	CACHE DATA TERMINATORS
M8515	CHX1	CSH ADR COMPARITORS AND VAL BIT MIXERS
	CHX2	CHS VAL BITS AND ADR MIXERS
	CHX3	CACHE USE BITS
	CHX4	CSH DIR PAR CHECKERS AND DIAG MIXERS
	CHX5	CACHE DIRECTORY POWER AND GND
	CHX6	CACHE EXTENSION TERMINATORS
M8551	CL1-3	IBUS ADAPTER INTERFACE
	CL4	I/O BUS ADAPTER INTERFACE
M8526	CLK1	CLK CONTROL CLOCK CONTROL
	CLK2, 4	CLK CONTROL DIAGNOSTIC CONTROL
	CLK3	CLK CONTROL EBOX CLK CONTROL
	CLK5	CLOCK CONTROL DIAGNOSTICS
	CLK6	EMBOX CLOCK TERMINATORS
M8553	CNT0-7	DTE20 CONTROL LOGIC
M8525	CON1-5	EBOX CONTROL #2
	CON6	CON POWER, GND, CAPS
M8511	CRA2	CONTROL RAM ADR CRADR 07-10
	CRA3, 4	CONTROL RAM ADR EBUS, SBR
	CRA5	CONTROL RAM ADR RAM
	CRA6	CONTROL RAM ADR POWER, GND, CAPS
M8528	CRM1	CONTROL RAM INPUT SIGNALS
	CRM2	CONTROL RAM CRAM 00-19
	CRM3	CONTROL RAM CRAM 20-39
	CRM4	CONTROL RAM CRAM 40-59
	CRM5	CONTROL RAM OUTPUT SIGNALS
	CRM6	CONTROL RAM POWER, GND, CAPS
M8513	CSH1-7	CACHE CONTROL
	CSH8	MBOX CONTROL - CSH POWER, GND, CAP
M8527	CTL1-3	EBOX CONTROL #1
	CTL4	CTL POWER, GND, CAPS
M8550	DLH1-4	IBUS ADAPTER DATA PATH
	DLH5	IBUS ADAPTER DATA PATH LEFT
M8552	DPS1-7	DTE20 DATA PATH AND STATUS
M8512	EPD1	DATA PATH AR REGISTERS
	EDP2	DATA PATH ARX, MQ REGISTERS
	EDP3	DATA PATH AD, ADX, ADDER
	EDP4	DATA PATH EBUS, FM, BR, BRX REGISTERS
	EDP5	EBOX DATA PATH POWER, GND, CAPS
M8554	INT1, 2	DTE20 UNIBUS INTERRUPT CONTROL
M8522	IR1	IR, DRAM & CARRY IR REG, DRAM BUFF
	IR2	IR, DRAM & CARRY DRAM
	IR3	IR, DRAM & CARRY DIAG REG & MISC
	IR4	IR, DRAM & CARRY ADD CARRY NETOWKR
	IR5	IR, DRAM & CARRY POWER, GND, CAPS
M8558	KIB1-5	KI MEMORY BUS ADAPTER

KL10-PA DRAWING INDEX (Cont)

Module Type	Index Name	Module Description
M8561 M8562 M8517	MAC1-6 MAT1-2 MB1-5 MB6	MA20 CONTROL BOARD MA20 TIMING BOARD MB BOARD MEMORY BUFFER POWER, GND, CAPS
M8531 M8529 M8537	MBC1-5 MBC6 MBX1-6 MBX7 MBZ1-6	MBOX CONTROL #5 MBC POWER, GND, CAPS MBOX CONTROL LOGIC MBX TERMINATORS MBOX CONTROL #4
M8530 M8519	MBZ7 MCL1-6 MCL7 MEM1-6 MTR1	MBOX CONTROL - MBZ POWER, GND, CAPS MEMORY CONTROL MCL POWER, GND, CAPS INTERNAL MEMORY BUS TRANSLATOR METER COUNTERS
M8538	MTR2 MTR3 MTR4 MTR5 MTR6	ACCOUNTING ENABLES AND 1 MHZ CLOCKS INTERVAL TIMER PERFORMANCE ANALYSIS EBUS MIXERS AND BUFFERS METERS POWER, GND, CAPS
M8520	PAG1 PAG2 PAG3 PAG4 PAG5	PAGE TABLE DATA PT ACCESS-PT-17 PAGE TABLE DATA PT 16-PT-26 PAGE TABLE DIRECTORY PAGE TABLE CONTROL LOGIC PAGE TABLE PARITY LOGIC
M8532	PAG6 PI1 PI2 PI3 PI4	PAGING BOARD POWER, GND, CAPS PRIORITY INTERRUPT REGISTERS PRIORITY INTERRUPT DEVICE SELECTION PRIORITY INTERRUPT CHANNELS PRIORITY INTERRUPT EBUS INTERFACE
M8518	PI5 PI6 PMA1 PMA2 PMA3	PRIORITY INTERRUPT CONTROL PI POWER, GND, CAPS PHYSICAL MEM ADR EBR, UBP, UEBR & VMA PHYSICAL MEM ADR CACHE CLR ADR PHYSICAL MEM ADR PA 14-31
M8524	PMA4 PMA5 PMA6 SCD1 SCD2	PHYSICAL MEM ADR ERA, PA 32-35 & PMA PHYSICAL MEM ADR SELECTION LOGIC PHYSICAL MEM ADR POWER, GND, CAPS SCAD, PC FLAGS SCADD, SCADA, SCADB SCAD, PC FLAGS SC, SCM, FE
M8510	SCD3 SCD4, 5 SH1 SH2 SH3	SCAD, PC FLAGS ARM DIAG MIXER SCAD, PC FLAGS PC FLAGS SHIFT MATRIX CONTROL SHIFT MATRIX SHIFT 16, 32 SHIFT MATRIX SHIFT 4, 8
M8560	SH4 SH5 SH6 SIC1 SIC2	SHIFT MATRIX SHIFT 1, 2 SHIFT MATRIX POWER, GND, CAPS SHIFT REGISTER TERMINATORS SBUS INTERFACE CONTROL BOARD ERROR AND DIAGNOSTIC DMA 20 BOARD
M8516	SIC3 SIC4 TRM2-5 VMA1 VMA2	CLOCK LOGIC DMA20 BOARD 1 (2 OF 3) TIMING LOGIC DMA20 BOARD 2 E AND C BUS TRANSLATOR VIRTUAL MEM ADR ADDER & CONTROL VIRTUAL MEM ADR VMA REGISTER
M8523	VMA3 VMA4 VMA5 VMA6	VIRTUAL MEM ADR PC & ADR BRK REG VIRTUAL MEM ADR VMA - HELD REGISTER VIRTUAL MEM ADR DIAGNOSTICS VIRTUAL MEM ADR POWER, GND, CAPS

CRAM BIT LOCATIONS

CRAM BITS SORTED BY LOCATION

LOCATION	FUNCTION	PHYSICAL BIT
A40R2	FM ADR SEL 1	58
A40V2	COND 05	59
B40F1	# 08	39
B40P2	COND 02	19
C40F2	TIME 01	78
C40J2	# 07	38
C40K2	COND 01	18
D40R2	TIME 00	76
D40V2	COND 00	17
E40D2	MQ SEL	16
E40P2	# 06	37
E40S2	ARMX SEL 4	36
E40K2	FM ADR SEL 2	57
E40P2	FM ADR SEL 4	56
A42P1	BRX LOAD	54
A42V2	COND 04	55
B42F1	# 05	35
B42P2	J 10	15
C42F2	AD CRY	74
C42J2	# 04	34
C42K2	J 09	14
D42R2	VMA SEL 1	72
D42V2	J 08	13
E42D2	J 07	12
E42P2	# 03	33
E42S2	ADB SEL 1	32
F42K2	COND 03	53
F42P1	BR LOAD	52
A44R2	MEM 02	50
A44V2	MEM 03	51
B44F1	# 02	31
B44P2	J 06	11
C44F2	ARMX SEL 1	70
C44J2	# 01	30
C44K2	J 05	10

LOCATION	FUNCTION	PHYSICAL BIT
D44R2	ARXM SEL 2	68
D44V2	J 04	09
E44D2	J 03	08
E44P2	# 00	29
E44S2	ADB SEL 2	28
F44K2	MEM 01	49
F44P2	MEM 00	48
D45M2	DISP00	81
D45T2	DISP01	82
E45F1	DISP02	83
E45M2	DISP03	84
E45S2	DISP04	85
A50R2	SH-ARMM SEL 2	46
A50V2	SH-ARMM SEL 1	47
B50A1	ADA SEL 1	27
B50P2	J 02	07
C50F2	ARM SEL 1	66
C50J2	ADA SEL 2	26
C50K2	J 01	06
D50R2	ARM SEL 2	64
D50V2	J 00	05
E50D2	FE LOAD	04
E50L1	ADA DISABLE	25
E50S1	AD BOOLE	24
E50K2	ARM SEL 4	45
E50P2	VMA SEL 2	44
A52R2	SCADB SEL 2	42
A52V2	MARK BIT	43
B52F1	AD SEL 1	23
B52P2	SCAD 1	03
C52F2	SCM SEL 2	62
C52J2	AD SEL 2	22
C52K2	SCAD 2	02
D52R2	SCADB SEL 1	60
D52V2	SCAD 4	01
E52D2	SCADA EN L	00
E52P2	AD SEL 4	21
E52S1	AD SEL 8	20
F52K2	SCADA SEL 1	41
F52P2	SCADA SEL 2	40

CRAM BITS SORTED BY FUNCTION

FUNCTION	PHYSICAL BIT	LOCATION
AD SEL 1	23	B52F1
AD SEL 4	21	E52P2
AD BOOLE	24	E50S1
ADA SEL 1	27	B50A1
ADA DISABLE	25	E50L1
ADB SEL 2	28	E44S2
ARM SEL 2	64	D50R2
ARXM SEL 1	70	C44F2
ARXM SEL 4	36	E40S2
BRX LOAD	54	A42P1
CALL	80	*
COND 01	18	C40K2
COND 03	53	F42K2
COND 05	59	A40V2
DISP00	81	D45M2
DISP01	82	D45T2
DISP02	83	E45F1
DISP03	84	E45M2
DISP04	85	E45S2
FM ADR SEL 1	58	A40R2
FM ADR SEL 4	56	F40P2
J 01	06	C50K2
J 03	08	E44D2
J 05	10	C44K2
J 07	12	E42D2
J 09	14	C42K2
MEM 00	48	F44P2
MEM 02	50	A44R2
MQ SEL	16	E40D2
# 01	30	C44J2
# 03	33	E42P2
# 05	35	B42F1
# 07	38	C40J2
SCAD 1	03	B52P2
SCAD 4	01	D52V2
SCADA SEL 1	41	F52K2
SCADB SEL 1	60	D52R2
SH-ARMM SEL 1	47	A50V2
SCM SEL 2	62	C52F2
TIME 01	78	C40F2
VMA SEL 2	44	F50P2

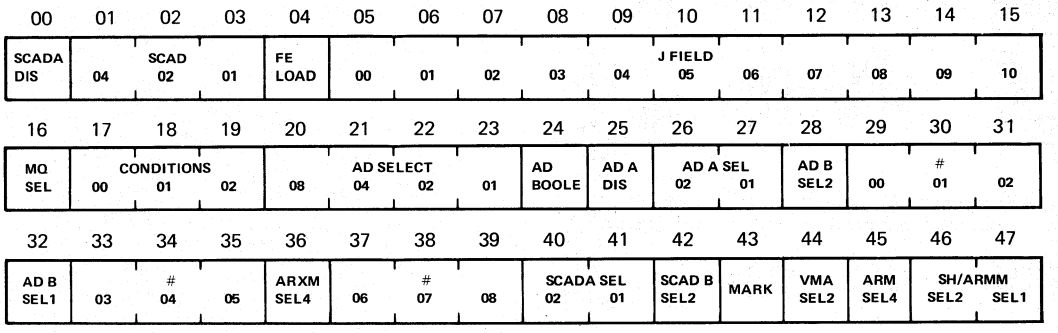
FUNCTION	PHYSICAL BIT	LOCATION
AD SEL 2	22	C52J2
AD SEL 8	20	E52S1
AD CRY	74	C42F2
ADA SEL 2	26	C50J2
ADB SEL 1	32	E42S2
ARM SEL 1	66	C50F2
ARM SEL 4	45	F50K2
ARXM SEL 2	68	D44R2
BR LOAD	52	F42P1
COND 00	17	D40V2
COND 02	19	B40P2
COND 04	55	A42V2
FE LOAD	04	E50D2
FM ADR SEL 2	57	F40K2
J 00	05	D50V2
J 02	07	B50P2
J 04	09	D44V2
J 06	11	B44P2
J 08	13	D42V2
J 10	15	B42P2
MEM 01	49	F44K2
MEM 03	51	A44V2
# 00	29	E44P2
# 02	31	B44F1
# 04	34	C42J2
# 05	37	E40P2
# 08	39	B40F1
SCAD 2	02	C52K2
SCADA EN L	00	E52D2
SCADA SEL 2	40	F52P2
SCADB SEL 2	42	A52R2
SH-ARMM SEL 2	46	A50R2
TIME 00	76	D40R2
VMA SEL 1	72	D42R2
MARK BIT	43	A52V2

CRAM SORTED BY BITS

PHYSICAL BIT	FUNCTION	LOCATION	PHYSICAL BIT	FUNCTION	LOCATION
00	SCADA EN L	E52D2	35	# 05	B42F1
01	SCAD 4	D52V2	36	ARMX SEL 4	E40S2
02	SCAD 2	C52K2	37	# 06	E40P2
03	SCAD 1	B52P2	38	# 07	C40J2
04	FE LOAD	E50D2	39	# 08	B40F1
05	J 00	D50V2	40	SCADA SEL 2	F52P2
06	J 01	C50K2	41	SCADA SEL 1	F52K2
07	J 02	B50P2	42	SCADB SEL 2	A52R2
08	J 03	E44D2	43	MARK BIT	A52V2
09	J 04	D44V2	44	VMA SEL 2	F50P2
10	J 05	C44K2	45	ARM SEL 4	F50K2
11	J 06	B44P2	46	SH ARMM SEL 2	A50R2
12	J 07	E42D2	47	SH ARMM SEL 1	A50V2
13	J 08	D42V2	48	MEM 00	F44P2
14	J 09	C42K2	49	MEM 01	F44K2
15	J 10	B42P2	50	MEM 02	A44R2
16	MQ SEL	E40D2	51	MEM 03	A44V2
17	COND 00	D40V2	52	BR LOAD	F42P1
18	COND 01	C40K2	53	COND 03	F42K2
19	COND 02	B40P2	54	BRX LOAD	A42P1
20	AD SEL 8	E52S1	55	COND 04	A42V2
21	AD SEL 4	E52P2	56	FM ADR SEL 4	F40P2
22	AD SEL 2	C52J2	57	FM ADR SEL 2	F40K2
23	AD SEL 1	B52F1	58	FM ADR SEL 1	A40R2
24	AD BOOLE	E50S1	59	COND 05	A40V2
25	ADA DISABLE	E50L1	60	SCADB SEL 1	D52R2
26	ADA SEL 2	C50J2	62	SCM SEL 2	C52F2
27	ADA SEL 1	B50A1	64	ARM SEL 2	D50R2
28	ADB SEL 2	E44S2	66	ARM SEL 1	C50F2
29	# 00	E44D2	68	ARXM SEL 2	D44R2
30	# 01	C44J2	70	ARXM SEL 1	C44F2
31	# 02	D44F1	72	VMA SEL 1	D42R2
32	ADB SEL 1	E42S2	74	AD CRY	C42F2
33	# 03	E42P2	76	TIME 00	D40R2
34	# 04	C42J2	78	TIME 01	C40F2
			80	CALL	*
			81	DISP00	D45M2
			82	DISP01	D45T2
			83	DISP02	E45F1
			84	DISP03	E45M2
			85	DISP04	E45S2

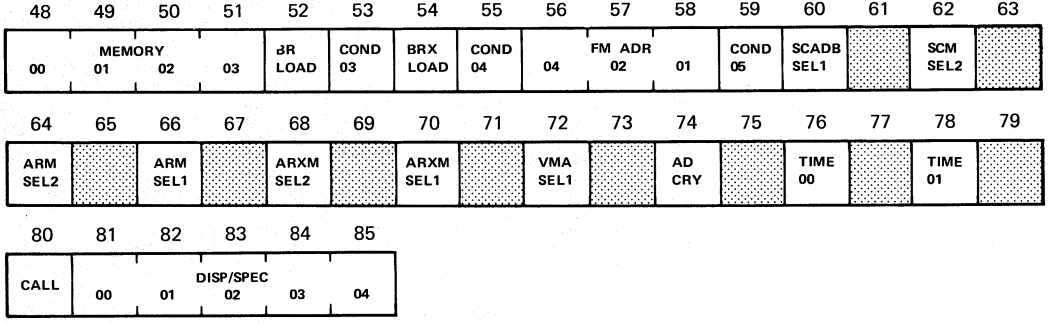
*CALL BIT IS USED IN KL10(PV) ONLY, THERE IS NO LOGIC FOR IT IN THE MODEL PA. THE CALL BIT IS NOT ACCESSIBLE ON THE BACKPLANE, IT MUST BE READ VIA A DIAGNOSTIC READ FUNCTION 141 BIT 00.

C RAM BIT MAP



BITS	SLOT
<00:03>	52
<04:07>	50
<08:11>	44
<12:15>	42
<16:19>	40
<20:23>	52
<24:27>	50
<28:31>	44
<32:35>	42
<36:39>	40
<40:43>	52
<44:47>	50
<48:51>	44
<52:55>	42
<56:59>	40
<60,62>	52
<64,66>	50
<68,70>	44
<72,74>	42
<76,78>	40
<80:85>	45

MR-2212


48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
MEMORY
00 01 02 03
dR LOAD
COND 03
BRX LOAD
COND 04
04 FM ADR 02 01
COND 05
SCADB SEL1
SCM SEL2
64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
ARM SEL2
ARM SEL1
ARXM SEL2
ARXM SEL1
VMA SEL1
AD CRY
TIME 00
TIME 01
80 81 82 83 84 85
CALL
DISP/SPEC
00 01 02 03 04

MR-2213

KLDCP EC AND DC COMMAND DATA FORMAT

ADR/	J	T	AR	AD	BR	MQ	FM	SCAD	SC	FE	SH	#	VMA	MEM	COND	SPEC	M
3777/3777		3	77	3777	3	1	7	377	1	1	3	777	3	17	77	77	1

SEE NOTE

	ARITH 00–07	ARITH 10–17	AR/ARX 00–07	BOOLE 00–07	BOOLE 10–17	COND 00–07	COND 10–17	COND 20–27	COND 30–37	COND 40–47	COND 50–57
00	A+C	ORCB+C	AR/ARX	SETCA	ANDCA		FM WRITE	DIAG FUNC	VMA–#		SC,LT,36
01		A-B-1+C	CACHE	ORC	XOR	LD AR0–8	PCF–#	EBOX STATE	VMA–#+TRP	EVEN PAR	SCAD0
02			AD	ORCA	B	LD AR9–17	FE SHRT	EBUS CTL	VMA–#+MODE	BR0	SCAD#0
03	A#2+C		EBUS/MQ	1S	OR	LD ARR	AD FLAGS	MBOX CTL	VMA–#+AR	ARX0	ADX0
04		-1+C	SH	ANDC	0S	AR CLR	LOAD IR		VMA–#+PI*2	AR18	AD CRY0
05			AD*2	SETCB	ANDCB	ARX CLR	SPEC INSTR		VMA DEC	AR0	AD0
06	A+B+C	AND-1+C	ADX	EQV	AND	ARL IND	SR–#		VMA INC	AC#0	AD#0
07		A-1+C	AD*,25	ORCB	A	REG CTL	SEL VMA		LD VMA HLD	SC0	AD#0

NOTE: AR FIELD INCLUDES AR AND ARX
AD FIELD INCLUDES ADA AND ADB
SCAN FIELD INCLUDES SCADA AND SCADB.

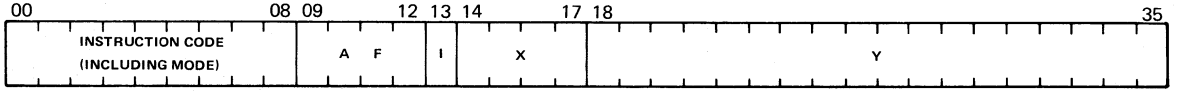
MR-2210

	COND 60–67	COND 70–77	FMADR 00–07	MEM 00–07	MEM 10–17	SCAD 00–07	SPEC 00–07	SPEC 10–17	SPEC 20–27	SPEC 30–37
00	FETCH	INTRPT	AC0		A INDRCT	A	DIAG		SEC HOLD	MUL
01	KERNEL	-START	AC1	ARL IND	BYTE INDRCT	A-B-1	DRAM J	INH CRY18	CALL	DIV
02	USER	RUN	XR	MB WAIT	LOAD AR	A+B	A READ	MQ SHIFT	ARL IND	SIGNS
03	PUBLIC	IO LEGAL	VMA	SEC 0	LOAD ARX	A-1	RETURN	SCM ALT	MTR CTL	DRAM B
04	RPW CYCLE	PIS XCT	AC2	A READ	AD FUNC	A+1	PF DISP	CLR FPD	FLG CTL	BYTE
05	PI CYCLE		AC3	B WRITE	BYTE READ	A-B	SR	LOAD PC	SV FLGS	NORM
06	-EBUS GRNT	AC REF	AC+#	FETCH	WRITE	OR	NICOND	XCRY AR0	SP MEM	EA MOD
07	-EBUS XFER	-MTR REQ	#B#	REG FUNC	RPW	AND	SH 0–3	GEN CRY18	AD LONG	EA TYPE

	ADA	ADB	SCADA	SCADB	SH	ARMM	VMA
0	AR	FM	FE	SC	SHIFT	#	VMA
1	ARX	BR*2	AR0–5	AR6–11	AR	AR SIGN	PC
2	MQ	BR	AR EXP	AR0–8	ARX	EXP	PC+1
3	PC	AR*4	#	#	AR SWAP	POS	AD

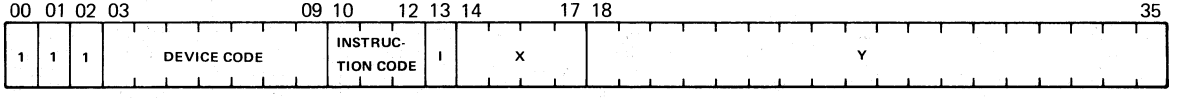
MR-2211

BASIC INSTRUCTION (KA10, KI10 AND KL10)



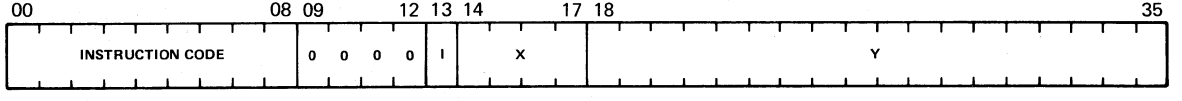
MR-3953

IN-OUT INSTRUCTION (KA10, KI10 and KL10)



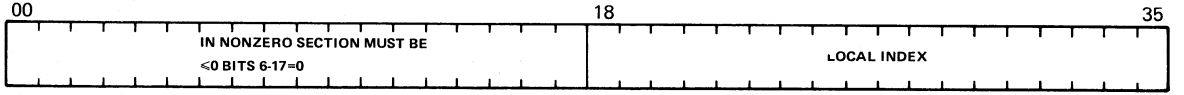
MR-3954

INSTRUCTIONS EXECUTED UNDER EXTEND (KL10 ONLY)



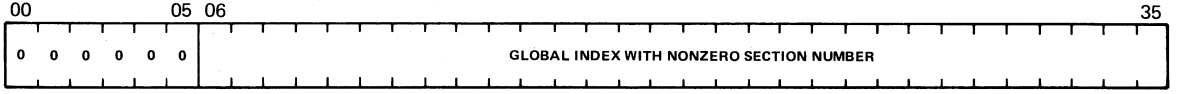
MR-3955

LOCAL INDEX REGISTER (KL10 ONLY)



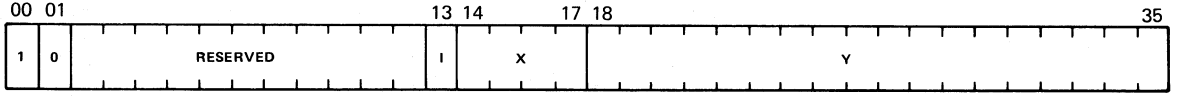
MR-3956

GLOBAL INDEX REGISTER (KL10 ONLY)



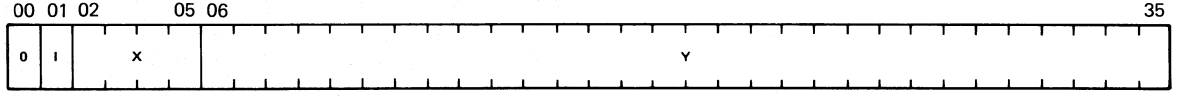
MR-3957

LOCAL INDIRECT WORD (KL10 ONLY)



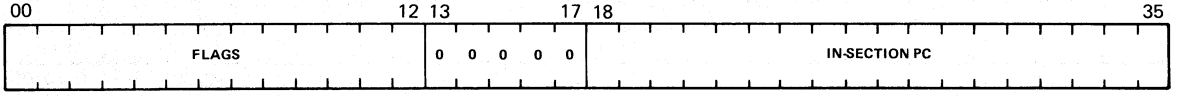
MR-3958

GLOBAL INDIRECT WORD (KL10 ONLY)



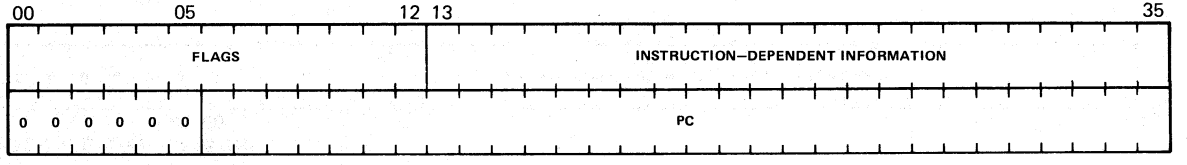
MR-3959

PC WORD (KA10, KI10 AND KL10)



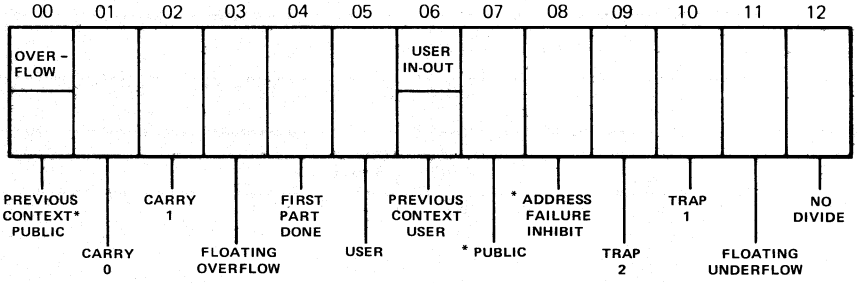
MR-3960

PC DOUBLEWORD (KL10 ONLY)



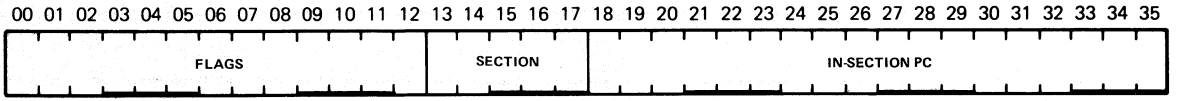
MR-3961

SAVED FLAGS

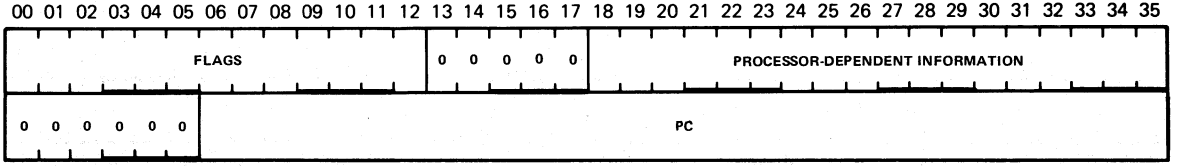


*KL10 ONLY

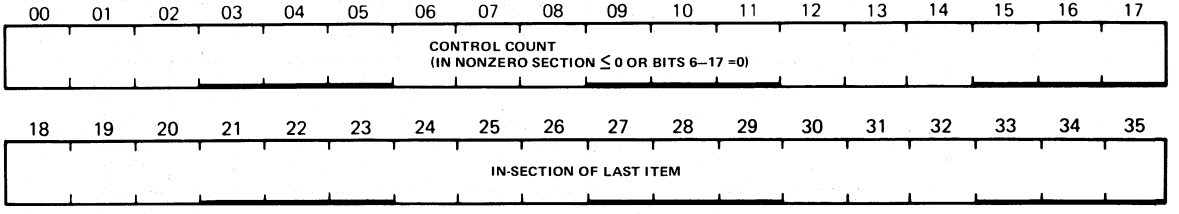
PC WORD



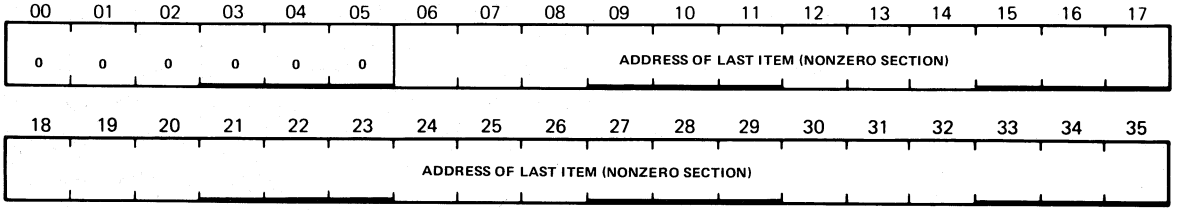
FLAG-PC DOUBLE WORD



LOCAL STACK POINTER

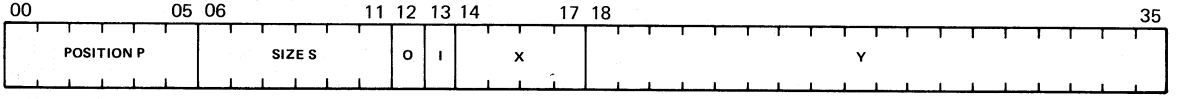


GLOBAL STACK POINTER

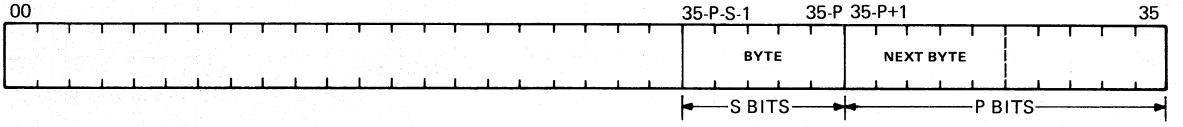


MR-6482

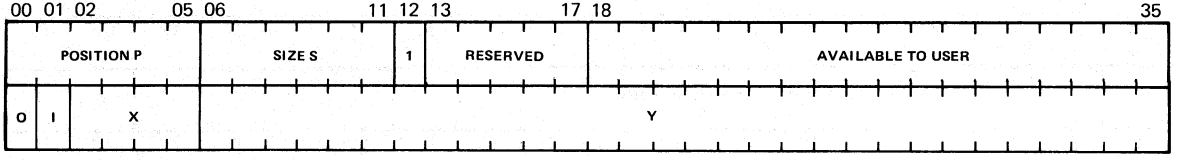
LOCAL BYTE POINTER (KA10, KI10 AND KL10)



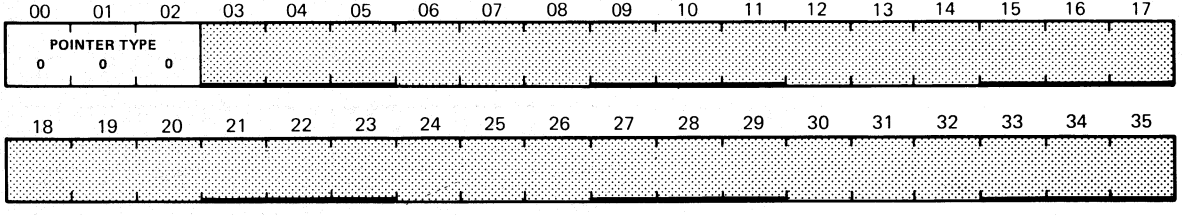
BYTE STORAGE



GLOBAL BYTE POINTER (KL10 ONLY)

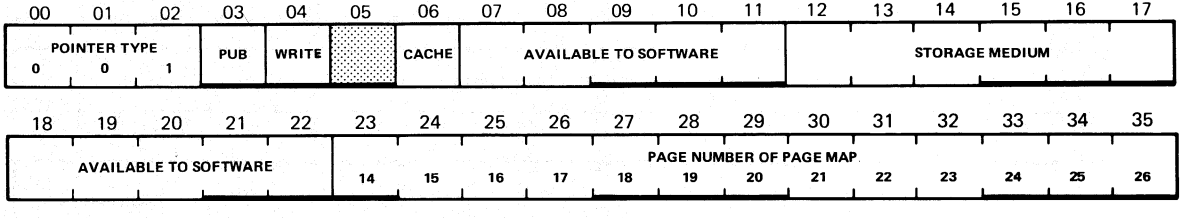


SECTION POINTER — No Access (TOPS-20 Only)



MR-3832

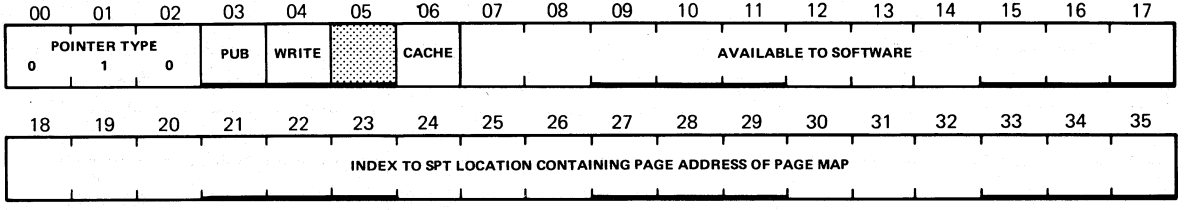
SECTION POINTER — Immediate (TOPS-20 Only)



03	0 = PRIVATE 1 = PUBLIC	06	0 = CACHE-LOOK BUT DO NOT LOAD 1 = CACHEABLE
04	0 = WRITE-PROTECTED 1 = WRITABLE	<12:17>	NON-ZERO INDICATES PAGE MAP IS NOT IN MEMORY

MR-3833

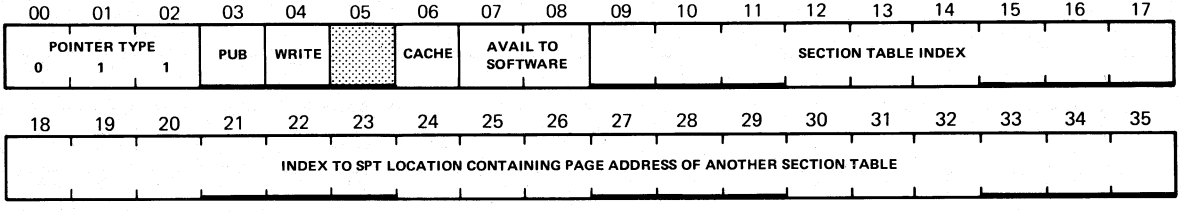
SECTION POINTER – Shared (TOPS-20 Only)



NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

MR-3835

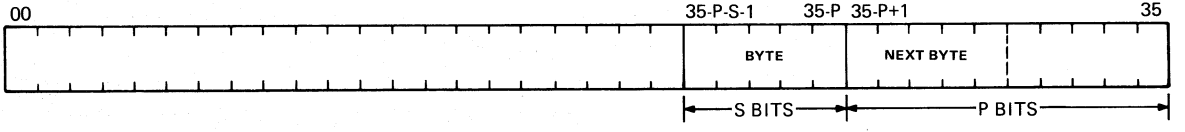
SECTION POINTER – Indirect (TOPS-20 Only)



NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

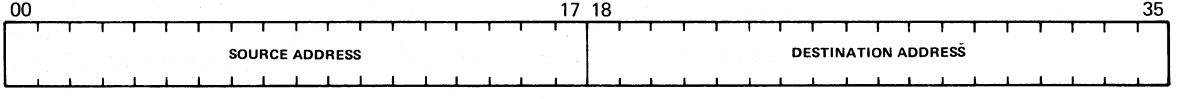
MR-3834

BYTE STORAGE



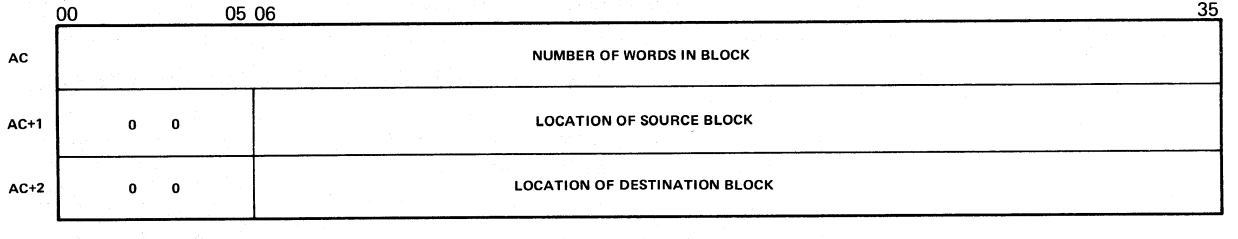
MR-3967

BLT POINTER (XWD) (KA10, KI10 AND KL10)



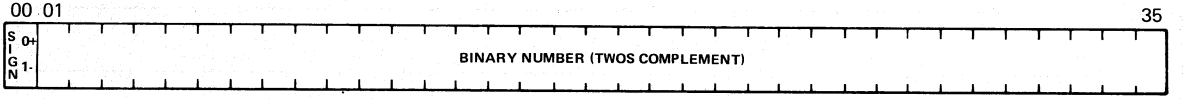
MR-3968

XBLT POINTER (KL10 ONLY)

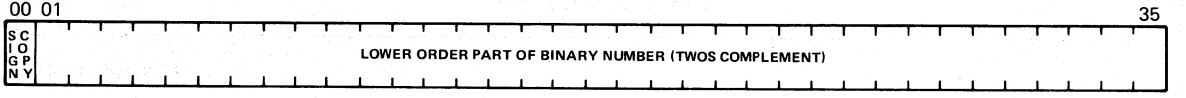


MR-3969

FIXED POINT OPERANDS (SINGLE PRECISION OR HIGH ORDER WORD (KA10, KI10 AND KL10)

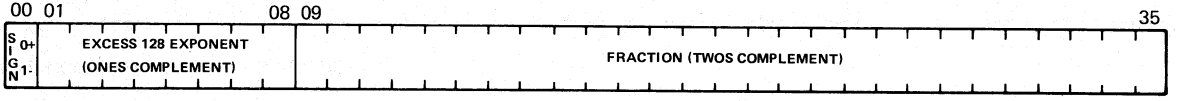


LOWER ORDER WORDS IN DOUBLE LENGTH FIXED POINT OPERANDS

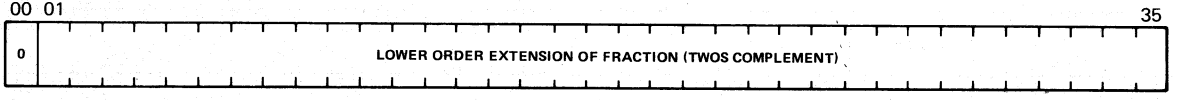


MR-3970

FLOATING POINT OPERANDS (SINGLE PRECISION OR HIGH ORDER WORD) (KI10 AND KL10 ONLY)



LOWER ORDER WORDS IN DOUBLE LENGTH FLOATING POINT OPERANDS



MR-3971

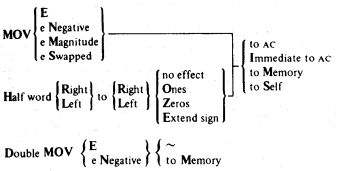
DEVICE CODE AND MNEMONICS

FIRST OCTAL DIGIT \ SECOND AND THIRD OCTAL DIGITS	00	04	10	14	20	24	30	34	40	44	50	54	60	64	70	74
0	APR CPA CENTRAL PROCESSOR	PI PRIORITY INTERRUPT	PAG KI10 PAGING	MCA20 CCA CACHE	TIM KL10 ACCOUNTING LOGIC	MTR	AD10 ADC2 ANALOG-DIGITAL CONVERTER	DX10 PDC3 MAGNETIC TAPE					DLB PDP-11 DATA LINK	DL10 DLC	DK10 CLK REAL TIME CLOCK	DK10 CLK2 REAL TIME CLOCK
1	PTP PAPER TAPE PUNCH	PTR PAPER TAPE READER	CP10 CDP CARD PUNCH		626 TTY CONSOLE TELETYPE	LP10 LPT LINE PRINTER	VP10 DIS DISPLAY	VP10 DIS2 DISPLAY	XY10 PLT PLOTTER	XY10 PLT2 PLOTTER	CR10 CR CARD READER	CR10 CR2 CARD READER	DLB2 PDP-11 DATA LINK	DL10 DLC2	RC10 DSK DISK/DRUM	RC10 DSK2 DISK/DRUM
2	DTE20 DTE0 10/11 INTERFACE	DTE20 DTE1 10/11 INTERFACE	DTE20 DTE2 10/11 INTERFACE	DTE20 DTE3 10/11 INTERFACE	DX10 PDC MAGNETIC TAPE	DX10 PDC2 MAGNETIC TAPE		LP10 LPT2 LINE PRINTER	DC10 DLS DATA LINE SCANNER	DC10 DLS2 DATA LINE SCANNER	RP10 DPC DISK PACK SYSTEM	RP10 DPC2 DISK PACK SYSTEM	RP10 DPC3 DISK PACK SYSTEM	RP10 DPC4 DISK PACK SYSTEM	RH10 RMC DATA CONTROL	RH10 RMC2 DATA CONTROL
3		DX10 PDC4 MAGNETIC TAPE			TD10 DTC DECTAPE	TD10 DTS DECTAPE	DTC2 DECTAPE	TD10 DTS2 DECTAPE	TMC MAGNETIC TAPE	TM10 TMS MAGNETIC TAPE	TMC2 MAGNETIC TAPE	TM10 TMS2 MAGNETIC TAPE	RH10 RMC3 DATA CONTROL	RH10 RMC4 DATA CONTROL	RH10 RMC5 DATA CONTROL	RH10 RMC6 DATA CONTROL
4													DSS SINGLE SYNCHRONOUS LINE UNIT	DS10 DSI	DSS2 SINGLE SYNCHRONOUS LINE UNIT	DS10 DSI2
5	CODES IN THIS SECTION RESERVED FOR USER SPECIAL DEVICES								RH20 MBC0 MASSBUS CONTROL	RH20 MBC1 MASSBUS CONTROL	RH20 MBC2 MASSBUS CONTROL	RH20 MBC3 MASSBUS CONTROL	RH20 MBC4 MASSBUS CONTROL	RH20 MBC5 MASSBUS CONTROL	RH20 MBC6 MASSBUS CONTROL	MBC7 MASSBUS CONTROL
6																
7									KI10 UNRESTRICTED CODES RESERVED FOR USERS				KI10 UNRESTRICTED CODES RESERVED FOR DEC			

MR-2300

MACHINE LANGUAGE INSTRUCTION SET

Full and Half Word Transmission



eXtended MOVE Immediate
eXtended Half word Left to Left Immediate
BLock Transfer
e**X**tended **BL**ock Transfer
EXCHange AC and memory

Full Word Data Transmission

EXCH	250	(AC) ↔ (E)			
MOVE	200	(E) → (AC)	MOVS	204	$(E)_S \rightarrow (AC)$
MOVEI	201	0,E → (AC)	MOVSI	205	E,0 → (AC)
MOVEM	202	(AC) → (E)	MOVSM	206	$(AC)_S \rightarrow (E)$
MOVES	203	*If* AC ≠ 0: (E) → (AC)	MOVSS	207	$(E)_S \rightarrow (E)$ *If* AC ≠ 0: (E) → (AC)
MOVN	210	− (E) → (AC)	MOVM	214	|(E)| → (AC)
MOVNI	211	− [0,E] → (AC)	MOVMI	215	0,E → (AC)
MOVNM	212	− (AC) → (E)	MOVMM	216	|(AC)| → (E)
MOVNS	213	− (E) → (E) *If* AC ≠ 0: (E) → (AC)	MOVMS	217	|(E)| → (E) *If* AC ≠ 0: (E) → (AC)
XMOVEI	415	*If not local AC reference:* E → (AC) *If local AC reference:* 1,E → (AC)			
DMOVE	120	(E,E+1) → (AC,AC+1)	DMOVEM	124	(AC,AC+1) → (E,E+1)
DMOVN	121	− (E,E+1) → (AC,AC+1)	DMOVNM	125	− (AC,AC+1) → (E,E+1)
BLT	251	*Move* $E_R - (AC)_R + 1$ *words starting with* $((AC)_L) \rightarrow ((AC)_R)$			
XBLT	020	*Move* |(AC)| *words* *If* (AC) > 0: *start with* ((AC+1)) → ((AC+2)) *and go up* *If* (AC) < 0: *start with* ((AC+1) − 1) → ((AC+2) − 1) *and go down*			

Half Word Data Transmission

HLL	500	$(E)_L \rightarrow (AC)_L$	HLLZ	510	$(E)_L$,0 → (AC)
HLLI	501	0 → $(AC)_L$	HLLZI	511	0 → (AC)
HLLM	502	$(AC)_L \rightarrow (E)_L$	HLLZM	512	$(AC)_L$,0 → (E)
HLLS	503	*If* AC ≠ 0: (E) → (AC)	HLLZS	513	0 → $(E)_R$ *If* AC ≠ 0: (E) → (AC)
HLLO	520	$(E)_L$,777777 → (AC)	HLLE	530	$(E)_L$,[$(E)_0$ × 777777] → (AC)
HLLOI	521	0,777777 → (AC)	HLLEI	531	0 → (AC)
HLLOM	522	$(AC)_L$,777777 → (E)	HLLEM	532	$(AC)_L$,[$(AC)_0$ × 777777] → (E)
HLLOS	523	777777 → $(E)_R$ *If* AC ≠ 0: (E) → (AC)	HLLES	533	$(E)_0$ × 777777 → $(E)_R$ *If* AC ≠ 0: (E) → (AC)
HLR	544	$(E)_L \rightarrow (AC)_R$	HLRZ	554	0,$(E)_L$ → (AC)
HLRI	545	0 → $(AC)_R$	HLRZI	555	0 → (AC)
HLRM	546	$(AC)_L \rightarrow (E)_R$	HLRZM	556	0,$(AC)_L$ → (E)
HLRS	547	$(E)_L \rightarrow (E)_R$ *If* AC ≠ 0: (E) → (AC)	HLRZS	557	0,$(E)_L$ → (E) *If* AC ≠ 0: (E) → (AC)

HLRO	564	777777,$(E)_L \rightarrow (AC)$	HLRE	574	$[(E)_0 \times 777777],(E)_L \rightarrow (AC)$
HLROI	565	777777,0 → (AC)	HLREI	575	0 → (AC)
HLROM	566	777777,$(AC)_L \rightarrow (E)$	HLREM	576	$[(AC)_0 \times 777777],(AC)_L \rightarrow (E)$
HLROS	567	777777,$(E)_L \rightarrow (E)$ *If* AC ≠ 0: (E) → (AC)	HLRES	577	$[(E)_0 \times 777777],(E)_L \rightarrow (E)$ *If* AC ≠ 0: (E) → (AC)
HRR	540	$(E)_R \rightarrow (AC)_R$	HRRZ	550	$0,(E)_R \rightarrow (AC)$
HRRI	541	$E \rightarrow (AC)_R$	HRRZI	551	0,E → (AC)
HRRM	542	$(AC)_R \rightarrow (E)_R$	HRRZM	552	$0,(AC)_R \rightarrow (E)$
HRRS	543	*If* AC ≠ 0: (E) → (AC)	HRRZS	553	$0 \rightarrow (E)_L$ *If* AC ≠ 0: (E) → (AC)
HRRO	560	777777,$(E)_R \rightarrow (AC)$	HRRE	570	$[(E)_{18} \times 777777],(E)_R \rightarrow (AC)$
HRROI	561	777777,E → (AC)	HRREI	571	$[E_{18} \times 777777],E \rightarrow (AC)$
HRROM	562	777777,$(AC)_R \rightarrow (E)$	HRREM	572	$[(AC)_{18} \times 777777],(AC)_R \rightarrow (E)$
HRROS	563	777777 → $(E)_L$ *If* AC ≠ 0: (E) → (AC)	HRRES	573	$(E)_{18} \times 777777 \rightarrow (E)_L$ *If* AC ≠ 0: (E) → (AC)
HRL	504	$(E)_R \rightarrow (AC)_L$	HRLZ	514	$(E)_R,0 \rightarrow (AC)$
HRLI	505	$E \rightarrow (AC)_L$	HRLZI	515	E,0 → (AC)
HRLM	506	$(AC)_R \rightarrow (E)_L$	HRLZM	516	$(AC)_R,0 \rightarrow (E)$
HRLS	507	$(E)_R \rightarrow (E)_L$ *If* AC ≠ 0: (E) → (AC)	HRLZS	517	$(E)_R,0 \rightarrow (E)$ *If* AC ≠ 0: (E) → (AC)
HRLO	524	$(E)_R$,777777 → (AC)	HRLE	534	$(E)_R,[(E)_{18} \times 777777] \rightarrow (AC)$
HRLOI	525	E,777777 → (AC)	HRLEI	535	$E,[E_{18} \times 777777] \rightarrow (AC)$
HRLOM	526	$(AC)_R$,777777 → (E)	HRLEM	536	$(AC)_R,[(AC)_{18} \times 777777] \rightarrow (E)$
HRLOS	527	$(E)_R$,777777 → (E) *If* AC ≠ 0: (E) → (AC)	HRLES	537	$(E)_R,[(E)_{18} \times 777777] \rightarrow (E)$ *If* AC ≠ 0: (E) → (AC)
XHLLI	501	$E_L \rightarrow (AC)_L$			

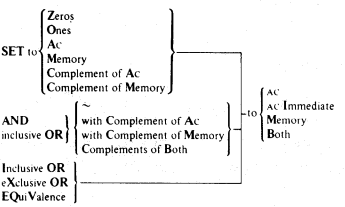
Byte Manipulation

use present pointer / Increment pointer } and { **LoaD** Byte into AC / **DePosit** Byte in memory

Increment / **ADJust** } **Byte Pointer**

IBP	133	*Linear operations on pointer in* E *or* E,E+1
	AC = 0	*If* P - S ≥ 0: P - S → P *If* P - S < 0: Y + 1 → Y 36 - S → P
ADJBP	133	*Array operations on pointer in* E *or* E,E+1
	AC ≠ 0	*Let A* = REMAINDER $\frac{36 - P}{S}$ *If* S > 36 - *A*: 1 → NO DIVIDE *If* S = 0: (E) → (AC) *or* (E,E+1) → (AC,AC+1) *If* 0 < S < 36 - *A*: *make copy* C *of* (E) *or* (E,E+1) *Compute* (AC) + $\left[\frac{36 - P}{S}\right]$ = Q × BYTES/WORD + R $1 \leqslant R \leqslant$ BYTES/WORD = $\left[\frac{36 - P}{S}\right] + \left[\frac{P}{S}\right]$ $Y\{C\} + Q \rightarrow Y\{C\}$ $36 - R \times S - A \rightarrow P\{C\}$ C → (AC) *or* (AC,AC+1)
LDB	135	BYTE IN ((E)) → (AC)
DPB	137	BYTE IN (AC) → BYTE IN ((E))
ILDB	134	IBP *and* LDB
IDPB	136	IBP *and* DPB

Boolean



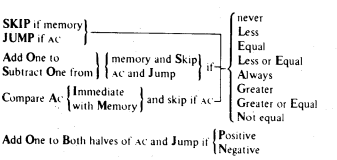
SETZ	400	0 → (AC)	SETO	474	777777777777 → (AC)
SETZI	401	0 → (AC)	SETOI	475	777777777777 → (AC)
SETZM	402	0 → (E)	SETOM	476	777777777777 → (E)
SETZB	403	0 → (AC) (E)	SETOB	477	777777777777 → (AC) (E)
SETA	424	(AC) → (AC) [*no-op*]	SETCA	450	~ (AC) → (AC)
SETAI	425	(AC) → (AC) [*no-op*]	SETCAI	451	~ (AC) → (AC)
SETAM	426	(AC) → (E)	SETCAM	452	~ (AC) → (E)
SETAB	427	(AC) → (E)	SETCAB	453	~ (AC) → (AC) (E)
SETM	414	(E) → (AC)	SETCM	460	~ (E) → (AC)
SETMI	415	0,E → (AC)	SETCMI	461	~ [0,E] → (AC)
SETMM	416	(E) → (E) [*no-op*]	SETCMM	462	~ (E) → (E)
SETMB	417	(E) → (AC) (E)	SETCMB	463	~ (E) → (AC) (E)
AND	404	(AC) ∧ (E) → (AC)	ANDCA	410	~ (AC) ∧ (E) → (AC)
ANDI	405	(AC) ∧ 0,E → (AC)	ANDCAI	411	~ (AC) ∧ 0,E → (AC)
ANDM	406	(AC) ∧ (E) → (E)	ANDCAM	412	~ (AC) ∧ (E) → (E)
ANDB	407	(AC) ∧ (E) → (AC) (E)	ANDCAB	413	~ (AC) ∧ (E) → (AC) (E)
ANDCM	420	(AC) ∧ ~ (E) → (AC)	ANDCB	440	~ (AC) ∧ ~ (E) → (AC)
ANDCMI	421	(AC) ∧ ~ [0,E] → (AC)	ANDCBI	441	~ (AC) ∧ ~ [0,E] → (AC)
ANDCMM	422	(AC) ∧ ~ (E) → (E)	ANDCBM	442	~ (AC) ∧ ~ (E) → (E)
ANDCMB	423	(AC) ∧ ~ (E) → (AC) (E)	ANDCBB	443	~ (AC) ∧ ~ (E) → (AC) (E)
IOR	434	(AC) ∨ (E) → (AC)	ORCA	454	~ (AC) ∨ (E) → (AC)
IORI	435	(AC) ∨ 0,E → (AC)	ORCAI	455	~ (AC) ∨ 0,E → (AC)
IORM	436	(AC) ∨ (E) → (E)	ORCAM	456	~ (AC) ∨ (E) → (E)
IORB	437	(AC) ∨ (E) → (AC) (E)	ORCAB	457	~ (AC) ∨ (E) → (AC) (E)
ORCM	464	(AC) ∨ ~ (E) → (AC)	ORCB	470	~ (AC) ∨ ~ (E) → (AC)
ORCMI	465	(AC) ∨ ~ [0,E] → (AC)	ORCBI	471	~ (AC) ∨ ~ [0,E] → (AC)
ORCMM	466	(AC) ∨ ~ (E) → (E)	ORCBM	472	~ (AC) ∨ ~ (E) → (E)
ORCMB	467	(AC) ∨ ~ (E) → (AC) (E)	ORCBB	473	~ (AC) ∨ ~ (E) → (AC) (E)
XOR	430	(AC) ∀ (E) → (AC)	EQV	444	~ [(AC) ∀ (E)] → (AC)
XORI	431	(AC) ∀ 0,E → (AC)	EQVI	445	~ [(AC) ∀ 0,E] → (AC)
XORM	432	(AC) ∀ (E) → (E)	EQVM	446	~ [(AC) ∀ (E)] → (E)
XORB	433	(AC) ∀ (E) → (AC) (E)	EQVB	447	~ [(AC) ∀ (E)] → (AC) (E)

Logical Testing and Modification

Test AC { with **D**irect mask / with **S**wapped mask / **R**ight with ε / **L**eft with ε } { **N**o modification / set masked bits to **Z**eros / set masked bits to **O**nes / **C**omplement masked bits } and skip { never / if all masked bits **E**qual 0 / if **N**ot all masked bits equal 0 / **A**lways }

TLN	601	*No-op*	TRN	600	*No-op*
TLNE	603	*If* $(AC)_L \wedge E = 0$: *skip*	TRNE	602	*If* $(AC)_R \wedge E = 0$: *skip*
TLNA	605	*Skip*	TRNA	604	*Skip*
TLNN	607	*If* $(AC)_L \wedge E \neq 0$: *skip*	TRNN	606	*If* $(AC)_R \wedge E \neq 0$: *skip*
TLZ	621	$(AC)_L \wedge \sim E \rightarrow (AC)_L$	TRZ	620	$(AC)_R \wedge \sim E \rightarrow (AC)_R$
TLZE	623	*If* $(AC)_L \wedge E = 0$: *skip* $(AC)_L \wedge \sim E \rightarrow (AC)_L$	TRZE	622	*If* $(AC)_R \wedge E = 0$: *skip* $(AC)_R \wedge \sim E \rightarrow (AC)_R$
TLZA	625	$(AC)_L \wedge \sim E \rightarrow (AC)_L$ *skip*	TRZA	624	$(AC)_R \wedge \sim E \rightarrow (AC)_R$ *skip*
TLZN	627	*If* $(AC)_L \wedge E \neq 0$: *skip* $(AC)_L \wedge \sim E \rightarrow (AC)_L$	TRZN	626	*If* $(AC)_R \wedge E \neq 0$: *skip* $(AC)_R \wedge \sim E \rightarrow (AC)_R$
TLC	641	$(AC)_L \forall E \rightarrow (AC)_L$	TRC	640	$(AC)_R \forall E \rightarrow (AC)_R$
TLCE	643	*If* $(AC)_L \wedge E = 0$: *skip* $(AC)_L \forall E \rightarrow (AC)_L$	TRCE	642	*If* $(AC)_R \wedge E = 0$: *skip* $(AC)_R \forall E \rightarrow (AC)_R$
TLCA	645	$(AC)_L \forall E \rightarrow (AC)_L$ *skip*	TRCA	644	$(AC)_R \forall E \rightarrow (AC)_R$ *skip*
TLCN	647	*If* $(AC)_L \wedge E \neq 0$: *skip* $(AC)_L \forall E \rightarrow (AC)_L$	TRCN	646	*If* $(AC)_R \wedge E \neq 0$: *skip* $(AC)_R \forall E \rightarrow (AC)_R$
TLO	661	$(AC)_L \vee E \rightarrow (AC)_L$	TRO	660	$(AC)_R \vee E \rightarrow (AC)_R$
TLOE	663	*If* $(AC)_L \wedge E = 0$: *skip* $(AC)_L \vee E \rightarrow (AC)_L$	TROE	662	*If* $(AC)_R \wedge E = 0$: *skip* $(AC)_R \vee E \rightarrow (AC)_R$
TLOA	665	$(AC)_L \vee E \rightarrow (AC)_L$ *skip*	TROA	664	$(AC)_R \vee E \rightarrow (AC)_R$ *skip*
TLON	667	*If* $(AC)_L \wedge E \neq 0$: *skip* $(AC)_L \vee E \rightarrow (AC)_L$	TRON	666	*If* $(AC)_R \wedge E \neq 0$: *skip* $(AC)_R \vee E \rightarrow (AC)_R$
TDN	610	*No-op*	TSN	611	*No-op*
TDNE	612	*If* $(AC) \wedge (E) = 0$: *skip*	TSNE	613	*If* $(AC) \wedge (E)_S = 0$: *skip*
TDNA	614	*Skip*	TSNA	615	*Skip*
TDNN	616	*If* $(AC) \wedge (E) \neq 0$: *skip*	TSNN	617	*If* $(AC) \wedge (E)_S \neq 0$: *skip*
TDZ	630	$(AC) \wedge \sim (E) \rightarrow (AC)$	TSZ	631	$(AC) \wedge \sim (E)_S \rightarrow (AC)$
TDZE	632	*If* $(AC) \wedge (E) = 0$: *skip* $(AC) \wedge \sim (E) \rightarrow (AC)$	TSZE	633	*If* $(AC) \wedge (E)_S = 0$: *skip* $(AC) \wedge \sim (E)_S \rightarrow (AC)$
TDZA	634	$(AC) \wedge \sim (E) \rightarrow (AC)$ *skip*	TSZA	635	$(AC) \wedge \sim (E)_S \rightarrow (AC)$ *skip*
TDZN	636	*If* $(AC) \wedge (E) \neq 0$: *skip* $(AC) \wedge \sim (E) \rightarrow (AC)$	TSZN	637	*If* $(AC) \wedge (E)_S \neq 0$: *skip* $(AC) \wedge \sim (E)_S \rightarrow (AC)$
TDC	650	$(AC) \forall (E) \rightarrow (AC)$	TSC	651	$(AC) \forall (E)_S \rightarrow (AC)$
TDCE	652	*If* $(AC) \wedge (E) = 0$: *skip* $(AC) \forall (E) \rightarrow (AC)$	TSCE	653	*If* $(AC) \wedge (E)_S = 0$: *skip* $(AC) \forall (E)_S \rightarrow (AC)$
TDCA	654	$(AC) \forall (E) \rightarrow (AC)$ *skip*	TSCA	655	$(AC) \forall (E)_S \rightarrow (AC)$ *skip*
TDCN	656	*If* $(AC) \wedge (E) \neq 0$: *skip* $(AC) \forall (E) \rightarrow (AC)$	TSCN	657	*If* $(AC) \wedge (E)_S \neq 0$: *skip* $(AC) \forall (E)_S \rightarrow (AC)$
TDO	670	$(AC) \vee (E) \rightarrow (AC)$	TSO	671	$(AC) \vee (E)_S \rightarrow (AC)$
TDOE	672	*If* $(AC) \wedge (E) = 0$: *skip* $(AC) \vee (E) \rightarrow (AC)$	TSOE	673	*If* $(AC) \wedge (E)_S = 0$: *skip* $(AC) \vee (E)_S \rightarrow (AC)$
TDOA	674	$(AC) \vee (E) \rightarrow (AC)$ *skip*	TSOA	675	$(AC) \vee (E)_S \rightarrow (AC)$ *skip*
TDON	676	*If* $(AC) \wedge (E) \neq 0$: *skip* $(AC) \vee (E) \rightarrow (AC)$	TSON	677	*If* $(AC) \wedge (E)_S \neq 0$: *skip* $(AC) \vee (E)_S \rightarrow (AC)$

Arithmetic Testing



AOBJP	252	(AC) + 1,1 → (AC) *If* (AC) ⩾ 0: E → (PC)			
AOBJN	253	(AC) + 1,1 → (AC) *If* (AC) < 0: E → (PC)			
CAI	300	*No-op*	CAM	310	*No-op*
CAIL	301	*If* (AC) < E: *skip*	CAML	311	*If* (AC) < (E): *skip*
CAIE	302	*If* (AC) = E: *skip*	CAME	312	*If* (AC) = (E): *skip*
CAILE	303	*If* (AC) ⩽ E: *skip*	CAMLE	313	*If* (AC) ⩽ (E): *skip*
CAIA	304	*Skip*	CAMA	314	*Skip*
CAIGE	305	*If* (AC) ⩾ E: *skip*	CAMGE	315	*If* (AC) ⩾ (E): *skip*
CAIN	306	*If* (AC) ≠ E: *skip*	CAMN	316	*If* (AC) ≠ (E): *skip*
CAIG	307	*If* (AC) > E: *skip*	CAMG	317	*If* (AC) > (E): *skip*
JUMP	320	*No-op*	SKIP	330	*If* AC ≠ 0: (E) → (AC)
JUMPL	321	*If* (AC) < 0: E → (PC)	SKIPL	331	*If* AC ≠ 0: (E) → (AC) *If* (E) < 0: *skip*
JUMPE	322	*If* (AC) = 0: E → (PC)	SKIPE	332	*If* AC ≠ 0: (E) → (AC) *If* (E) = 0: *skip*
JUMPLE	323	*If* (AC) ⩽ 0: E → (PC)	SKIPLE	333	*If* AC ≠ 0: (E) → (AC) *If* (E) ⩽ 0: *skip*
JUMPA	324	E → (PC)	SKIPA	334	*If* AC ≠ 0: (E) → (AC) *Skip*
JUMPGE	325	*If* (AC) ⩾ 0: E → (PC)	SKIPGE	335	*If* AC ≠ 0: (E) → (AC) *If* (E) ⩾ 0: *skip*
JUMPN	326	*If* (AC) ≠ 0: E → (PC)	SKIPN	336	*If* AC ≠ 0: (E) → (AC) *If* (E) ≠ 0: *skip*
JUMPG	327	*If* (AC) > 0: E → (PC)	SKIPG	337	*If* AC ≠ 0: (E) → (AC) *If* (E) > 0: *skip*
AOJ	340	(AC) + 1 → (AC)	SOJ	360	(AC) − 1 → (AC)
AOJL	341	(AC) + 1 → (AC) *If* (AC) < 0: E → (PC)	SOJL	361	(AC) − 1 → (AC) *If* (AC) < 0: E → (PC)
AOJE	342	(AC) + 1 → (AC) *If* (AC) = 0: E → (PC)	SOJE	362	(AC) − 1 → (AC) *If* (AC) = 0: E → (PC)
AOJLE	343	(AC) + 1 → (AC) *If* (AC) ⩽ 0: E → (PC)	SOJLE	363	(AC) − 1 → (AC) *If* (AC) ⩽ 0: E → (PC)
AOJA	344	(AC) + 1 → (AC) E → (PC)	SOJA	364	(AC) − 1 → (AC) E → (PC)
AOJGE	345	(AC) + 1 → (AC) *If* (AC) ⩾ 0: E → (PC)	SOJGE	365	(AC) − 1 → (AC) *If* (AC) ⩾ 0: E → (PC)
AOJN	346	(AC) + 1 → (AC) *If* (AC) ≠ 0: E → (PC)	SOJN	366	(AC) − 1 → (AC) *If* (AC) ≠ 0: E → (PC)
AOJG	347	(AC) + 1 → (AC) *If* (AC) > 0: E → (PC)	SOJG	367	(AC) − 1 → (AC) *If* (AC) > 0: E → (PC)
AOS	350	(E) + 1 → (E) *If* (AC) ≠ 0: (E) → (AC)	SOS	370	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC)
AOSL	351	(E) + 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) < 0: *skip*	SOSL	371	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) < 0: *skip*
AOSE	352	(E) + 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) = 0: *skip*	SOSE	372	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) = 0: *skip*
AOSLE	353	(E) + 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) ⩽ 0: *skip*	SOSLE	373	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) ⩽ 0: *skip*

AOSA	354	(E) + 1 → (E) *If* AC ≠ 0: (E) → (AC) *Skip*	SOSA	374	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC) *Skip*
AOSGE	355	(E) + 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) ⩾ 0: *skip*	SOSGE	375	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) ⩾ 0: *skip*
AOSN	356	(E) + 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) ≠ 0: *skip*	SOSN	376	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) ≠ 0: *skip*
AOSG	357	(E) + 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) > 0: *skip*	SOSG	377	(E) − 1 → (E) *If* AC ≠ 0: (E) → (AC) *If* (E) > 0: *skip*

Shift and Rotate

Arithmetic **SH**ift
Logical **SH**ift
ROTate
} { ~ Combined

ASH	240	(AC) X 2^E → (AC)	ASHC	244	(AC,AC+1) X 2^E → (AC,AC+1)
ROT	241	*Rotate* (AC) E *places*	ROTC	245	*Rotate* (AC,AC+1) E *places*
LSH	242	*Shift* (AC) E *places*	LSHC	246	*Shift* (AC,AC+1) E *places*

FIXED AND FLOATING POINT ARITHMETIC

ADD
SUBtract
MULtiply
Integer **MUL**tiply
DIVide
Integer **DIV**ide
} { ~ Immediate to Memory to Both

and Round

Floating **A**d**D**
Floating **Su**B**t**ract
Floating **Mult**i**P**ly
Floating **D**i**V**ide
} { ~ Long to Memory to Both

Floating **SC**ale

Double **F**loating **N**egate
Unnormalized **F**loating **A**dd

FIX
FIX and Round
FLOAT and Round
Double **ADD**
Double **SUB**tract
Double **MUL**tiply
Double **DIV**ide
Double Floating **A**d**D**
Double Floating **Su**B**t**ract
Double Floating **Mult**i**P**ly
Double Floating **D**i**V**ide

Fixed Point Arithmetic

ADD	270	(AC) + (E) → (AC)	SUB	274	(AC) − (E) → (AC)
ADDI	271	(AC) + 0,E → (AC)	SUBI	275	(AC) − 0,E → (AC)
ADDM	272	(AC) + (E) → (E)	SUBM	276	(AC) − (E) → (E)
ADDB	273	(AC) + (E) → (AC) (E)	SUBB	277	(AC) − (E) → (AC) (E)
IMUL	220	(AC) X (E) → (AC)*	MUL	224	(AC) X (E) → (AC,AC+1)
IMULI	221	(AC) X 0,E → (AC)*	MULI	225	(AC) X 0,E → (AC,AC+1)
IMULM	222	(AC) X (E) → (E)*	MULM	226	(AC) X (E) → (E)†
IMULB	223	(AC) X (E) → (AC) (E)*	MULB	227	(AC) X (E) → (AC,AC+1) (E)
IDIV	230	(AC) ÷ (E) → (AC) REMAINDER → (AC+1)	DIV	234	(AC,AC+1) ÷ (E) → (AC) REMAINDER → (AC+1)
IDIVI	231	(AC) ÷ 0,E → (AC) REMAINDER → (AC+1)	DIVI	235	(AC,AC+1) ÷ 0,E → (AC) REMAINDER → (AC+1)
IDIVM	232	(AC) ÷ (E) → (E)	DIVM	236	(AC,AC+1) ÷ (E) → (E)
IDIVB	233	(AC) ÷ (E) → (AC) (E) REMAINDER → (AC+1)	DIVB	237	(AC,AC+1) ÷ (E) → (AC) (E) REMAINDER → (AC+1)

DADD	114	(AC,AC+1) + (E,E+1) → (AC,AC+1)
DSUB	115	(AC,AC+1) - (E,E+1) → (AC,AC+1)
DMUL	116	(AC,AC+1) × (E,E+1) → (AC-AC+3)
DDIV	117	(AC-AC+3) ÷ (E,E+1) → (AC,AC+1) REMAINDER → (AC+2,AC+3)

*The high order word of the product is discarded.
†The low order word of the product is discarded.

Floating Point Arithmetic

FAD	140	(AC) + (E) → (AC)	FADR	144	(AC) + (E) → (AC)
FADL	141	(AC) + (E) → (AC,AC+1)	FADRI	145	(AC) + E,0 → (AC)
FADM	142	(AC) + (E) → (E)	FADRM	146	(AC) + (E) → (E)
FADB	143	(AC) + (E) → (AC) (E)	FADRB	147	(AC) + (E) → (AC) (E)
FSB	150	(AC) − (E) → (AC)	FSBR	154	(AC) − (E) → (AC)
FSBL	151	(AC) − (E) → (AC,AC+1)	FSBRI	155	(AC) − E,0 → (AC)
FSBM	152	(AC) − (E) → (E)	FSBRM	156	(AC) − (E) → (E)
FSBB	153	(AC) − (E) → (AC) (E)	FSBRB	157	(AC) − (E) → (AC) (E)
FMP	160	(AC) × (E) → (AC)	FMPR	164	(AC) × (E) → (AC)
FMPL	161	(AC) × (E) → (AC,AC+1)	FMPRI	165	(AC) × E,0 → (AC)
FMPM	162	(AC) × (E) → (E)	FMPRM	166	(AC) × (E) → (E)
FMPB	163	(AC) × (E) → (AC) (E)	FMPRB	167	(AC) × (E) → (AC) (E)
FDV	170	(AC) ÷ (E) → (AC)	FDVR	174	(AC) ÷ (E) → (AC)
FDVL	171	(AC) ÷ (E) → (AC) REMAINDER → (AC+1)	FDVRI	175	(AC) ÷ E,0 → (AC)
FDVM	172	(AC) ÷ (E) → (E)	FDVRM	176	(AC) ÷ (E) → (E)
FDVB	173	(AC) ÷ (E) → (AC) (E)	FDVRB	177	(AC) ÷ (E) → (AC) (E)

UFA	130	(AC) + (E) → (AC+1) *without normalization*
DFN	131	− (AC,E) → (AC,E)
FSC	132	(AC) × 2^E → (AC)
FLTR	127	(E) *floated, rounded* → (AC)

FIX 122 (E) *fixed* → (AC) FIXR 126 (E) *fixed, rounded* → (AC)

DFAD	110	(AC,AC+1) + (E,E+1) → (AC,AC+1)
DFSB	111	(AC,AC+1) − (E,E+1) → (AC,AC+1)
DFMP	112	(AC,AC+1) × (E,E+1) → (AC,AC+1)
DFDV	113	(AC,AC+1) ÷ (E,E+1) → (AC,AC+1)

STACK

PUSH } { ~
POP } { and **J**ump
ADJust **S**tack **P**ointer

PUSH	261	*If* PC_L = 0 *or* $(AC)_{0,6\text{-}17} \leq 0$: (AC) + 1,1 → (AC) (E) → $((AC)_R)$ *If* $PC_L \neq 0$ *and* $(AC)_{0,6\text{-}17} < 0$: (AC) + 1 → (AC) (E) → ((AC))
POP	262	*If* PC_L = 0 *or* $(AC)_{0,6\text{-}17} \leq 0$: $((AC)_R)$ → (E) (AC) - 1,1 → (AC) *If* $PC_L \neq 0$ *and* $(AC)_{0,6\text{-}17} > 0$: ((AC)) → (E) (AC) - 1 → (AC)
PUSHJ	260	*If* PC_L = 0: (AC) + 1,1 → (AC) FLAGS, PC+1 → $((AC)_R)$ *If* $PC_L \neq 0$ *and* $(AC)_{0,6\text{-}17} \leq 0$: (AC) + 1,1 → (AC) PC+1 → $((AC)_R)$ *If* $PC_L \neq 0$ *and* $(AC)_{0,6\text{-}17} > 0$: (AC) + 1 → (AC) PC+1 → ((AC)) E → (PC)
POPJ	263	*If* PC_L = 0: $((AC)_R)_R$ → (PC) (AC) - 1,1 → (AC) *If* $PC_L \neq 0$ *and* $(AC)_{0,6\text{-}17} \leq 0$: $((AC)_R)$ → (PC) (AC) - 1,1 → (AC) *If* $PC_L \neq 0$ *and* $(AC)_{0,6\text{-}17} > 0$: ((AC)) → (PC) (AC) - 1 → (AC)
ADJSP	105	*If* PC_L = 0 *or* $(AC)_{0,6\text{-}17} \leq 0$: (AC) + [±] E_R, E_R → (AC) *If* $PC_L \neq 0$ *and* $(AC)_{0,6\text{-}17} > 0$: (AC) + [±] E_R → (AC)

Program Control

Jump
- to SubRoutine
- and Save PC
- and Save AC
- and Restore AC
- if Find First One
- on Flag and CLear it
- on OVerflow (JFCL 10,)
- on CaRrY 0 (JFCL 4,)
- on CaRrY 1 (JFCL 2,)
- on CaRrY (JFCL 6,)
- on Floating OVerflow (JFCL 1,)
- and ReSTore
- and ReSTore Flags (JRST 2,)
- and ENable PI level (JRST 12,)

HALT (JRST 4,)

PORTAL (JRST 1,)

eXtended Jump and ReSTore Flags (JRST 5,)
eXtended Jump and ENable PI level (JRST 6,)
eXtended PC Word (JRST 7,)
Save Flags in Memory (JRST 14,)
eXeCuTe
MAP

XCT	256	*Execute* (E)
JFFO	243	*If* (AC) = 0: 0 → (AC + 1)
		If (AC) ≠ 0: E → (PC) *(see page 2-63)*
JFCL	255	*If* AC ∧ FLAGS ≠ 0: E → (PC) ~ AC ∧ FLAGS → FLAGS
JRST	25400	E → (PC)
PORTAL	25404	0 → PUBLIC E → (PC)
JRSTF	25410	$(X)_L$ *or* $(Y)_L$ → FLAGS E → (PC)
HALT	25420	E → (PC) *stop*
XJRSTF	25424	$(E)_L$ → FLAGS (E+1) → (PC)
XJEN	25430	*Dismiss* PI $(E)_L$ → FLAGS (E+1) → (PC)
XPCW	25434	FLAGS, 0 → (E) PC+1 → (E+1) $(E+2)_L$ → FLAGS (E+3) → (PC)
JEN	25450	*Dismiss* PI $(X)_L$ *or* $(Y)_L$ → FLAGS E → (PC)
SFM	25460	FLAGS, 0 → (E)
JSR	264	*If* PC_L = 0: FLAGS, PC_R +1 → (E) E+1 → (PC)
		If PC_L ≠ 0: PC+1 → (E) E+1 → (PC)
JSP	265	*If* PC_L = 0: FLAGS, PC_R +1 → (AC) E → (PC)
		If PC_L ≠ 0: PC+1 → (AC) E → (PC)
JSA	266	(AC) → (E) E_R, PC_R +1 → (AC) E+1 → (PC)
JRA	267	$((AC)_L)$ → (AC) E → (PC)
MAP	257	PHYSICAL MAP DATA → (AC)

Extended Instructions

MOVe String
- Left Justified
- Right Justified
- Offset
- Translated

CoMPare Strings and skip if
- Less
- Equal
- Less or Equal
- Greater
- Greater or Equal
- Not equal

ConVert { Decimal to Binary / Binary to Decimal } { Offset / Translated }

EDIT string

CMPSL	001	CVTDBO	010
CMPSE	002	CVTDBT	011
CMPSLE	003	CVTDBO	012
EDIT	004	CVTDBT	013
CMPSGE	005	MOVSO	014
CMPSN	006	MOVST	015
CMPSG	007	MOVSLJ	016
		MOVSRJ	017

NOTE

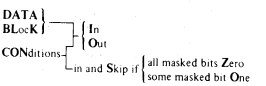
Refer to the DECsystem-10/DECSYSTEM-20 Hardware Reference Manual, Volume I, for a description of the Extended Instructions.

Cache *CCA 014*

All sweeps initially set Sweep Busy, and at termination they clear Sweep Busy and set Sweep Done.

SWPIA	70144	*Invalidate all pages*	* SWPIO	70164	*Invalidate page E*
SWPVA	70150	*Validate all pages*	* SWPVO	70170	*Validate page E*
SWPUA	70154	*Unload all pages*	* SWPUO	70174	*Unload page E*

In-out



CONO	70020	E → COMMAND	CONSZ	70030	*If* $\text{STATUS}_R \wedge E = 0$: *skip*
CONI	70024	STATUS → (E)	CONSO	70034	*If* $\text{STATUS}_R \wedge E \neq 0$: *skip*
DATAO	70014	(E) → DATA	DATAI	70004	DATA → (E)

BLKO	70010	(E) + 1,1 → (E)	$((E)_R)$ → DATA	*If* $(E)_L \neq 0$: *skip*
BLKI	70000	(E) + 1,1 → (E)	DATA → $((E)_R)$	*If* $(E)_L \neq 0$: *skip*

ALGEBRAIC REPRESENTATION

AC — The accumulator address in bits 9–12 of the instruction word

AC+*N* — The address *N* greater than AC, except that accumulator addresses wrap around from 17, e.g., AC+3 is 1 if AC is 16.

E — The result of the effective address calculation. When E is an address it has the number of bits appropriate to such use – depending on the type of processor, whether local or global, etc. E is eighteen bits unsigned when used as a half word operand, mask or output conditions; nine bits signed when used as a scale factor or shift number; and eighteen bits signed when used as an offset. For any signed quantity, the sign is always bit 18.

E_R — The in-section part of E (the right eighteen bits).

E_L — The section-number part of E (those bits, if any, at the left of bit 18).

E+*N* — The address *N* greater than E, with a wraparound, where appropriate, from an in-section value of 777777 without changing the section number.

PC — The 30-bit or 18-bit program counter; the symbol also represents the contents of PC when used as the source of an address.

PC+1 — The address produced by adding 1 to the in-section part of PC with a wraparound from 777777 (the section number does not change).

(X) — The word contained in register *X*.

$(X)_L$ — The left half of (X).

$(X)_R$ — The right half of (X).

$(X)_S$ — The word contained in *X* with its left and right halves swapped.

A_n — The value of bit *n* of the quantity *A*.

A,*B* — A 36-bit word with the 18-bit quantity *A* in its left half and the 18-bit quantity *B* in its right half (either *A* or *B* may be 0).

(X,Y) — The contents of registers *X* and *Y* concatenated into a double word operand.

$(X\text{-}Y)$ — The contents of registers *X* to *Y* concatenated into a multiword operand.

$((X))$ — The word contained in the register addressed by (X), i.e., addressed by the word in register *X*.

*With MCA25 installed cache data sweep for one page instruction, SWPTO, SWPVO, and SWPUO will sweep two pages (both even and odd pages will be swept when these instructions are executed).

$A \rightarrow B$ The quantity A replaces the quantity B (A and B may be half words, full words or double words). For example,

$$(AC) + (E) \rightarrow (AC)$$

means the word in accumulator AC plus the word in memory location E replaces the word in AC.

(AC) (E) The word in AC and the word in E.

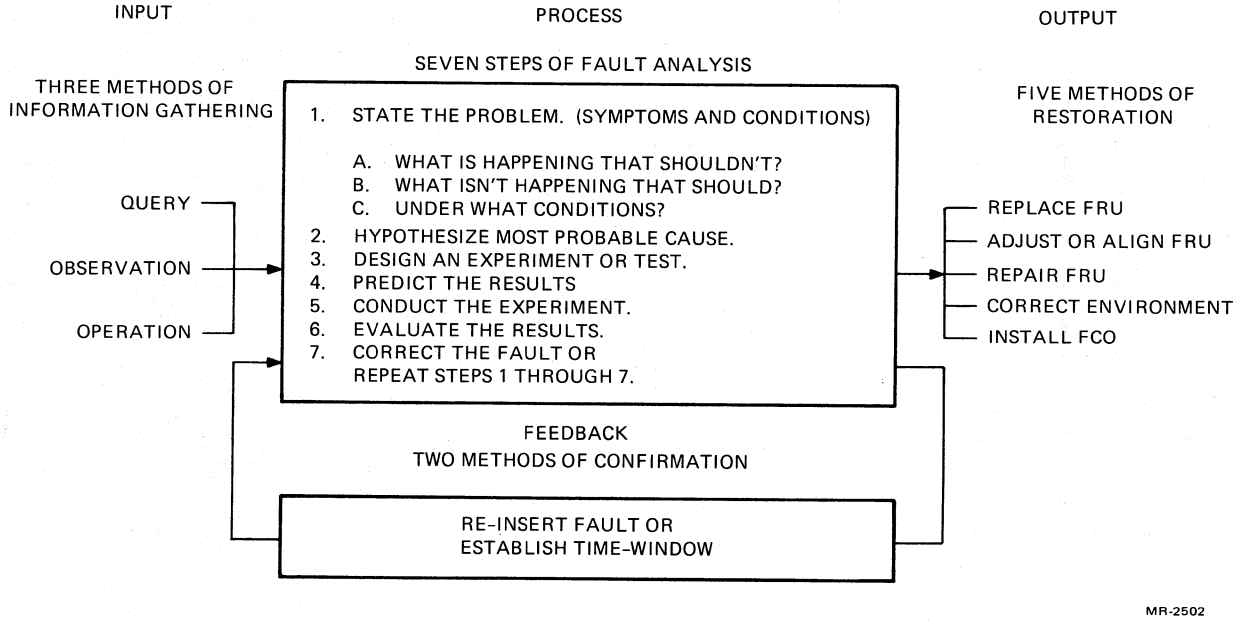
$\wedge \vee \forall \sim$ The Boolean operators AND, inclusive OR, exclusive OR, and complement (logical negation).

$+ - \times \div \|$ The arithmetic operators for addition, negation or subtraction, multiplication, division, and absolute value (magnitude).

Square brackets are used occasionally for grouping, but when they enclose an arithmetic computation they represent the "largest integer contained in" the enclosed quantity. With respect to the values of their terms, the equations for a given instruction are in chronological order; e.g., in the pair of equations

$$(AC) + 1 \rightarrow (AC)$$
$$If\ (AC) = 0: E \rightarrow (PC)$$

the quantity tested in the second equation is the word in AC after it has been incremented by one.


INPUT
PROCESS
OUTPUT
SEVEN STEPS OF FAULT ANALYSIS
THREE METHODS OF INFORMATION GATHERING
1. STATE THE PROBLEM. (SYMPTOMS AND CONDITIONS)
A. WHAT IS HAPPENING THAT SHOULDN'T?
B. WHAT ISN'T HAPPENING THAT SHOULD?
C. UNDER WHAT CONDITIONS?
2. HYPOTHESIZE MOST PROBABLE CAUSE.
3. DESIGN AN EXPERIMENT OR TEST.
4. PREDICT THE RESULTS
5. CONDUCT THE EXPERIMENT.
6. EVALUATE THE RESULTS.
7. CORRECT THE FAULT OR REPEAT STEPS 1 THROUGH 7.
FIVE METHODS OF RESTORATION
QUERY
OBSERVATION
OPERATION
REPLACE FRU
ADJUST OR ALIGN FRU
REPAIR FRU
CORRECT ENVIRONMENT
INSTALL FCO
FEEDBACK
TWO METHODS OF CONFIRMATION
RE-INSERT FAULT OR
ESTABLISH TIME-WINDOW
MR-2502

NOTES

GATHERING KL10 SYSTEM ERROR INFORMATION

Prior to gathering KL10 system error information, the auto-reload feature must be disabled.

Procedure 1 lists the steps necessary to disable auto-reload for TOPS-20 and TOPS-10 (release 603 or later).

Procedure 2 lists additional steps necessary to disable auto-reload for all TOPS-10 operating systems.

Procedure 3 lists the steps necessary to gather essential KL10 system error information.

Procedure 1 Disabling Auto-Reload (TOPS-20 and TOPS-10/603 and Later)

Step	Command Response	Comments
1	↑\	Enter PARSER command mode
2	PAR>SET CONSOLE PROGRAMER<CR>	Request PROGRAMMER mode privileges
	CONSOLE MODE: PROGRAMMER	PARSER response
3	PAR>SET NO RELOAD<CR>	Disable auto-reload
	RELOAD ENABLE: OFF	PARSER response
4	PAR>QUIT<CR>	Exit PARSER. Return to command mode.

Procedure 2 Disabling Auto-Reload (TOPS-10 Only)

Step	Command Response	Comments
1	↑C	Control C - Enter TOPS-20 command mode.
2	.R WHEEL<CR> Setting Wheel Capability if the CTY is used.	Request 1,2 privileges. This step is not necessary
3	.R FILDDT<CR>	Run FILDDT
4	FILE: SYSTEM/S<CR>	Load the operating system's symbol table.
5	FILE:/M/P<CR>	Enable, examining and patching the operating system.
6	*$H<CR>	Set DDT printout mode to half-word.
7	*DEBUGF/XYXXXX,,XXXXXX	Bit 03 of this word must be set to disable auto-reload. That is, the second octal digit (Y) must be either a 4, 5, 6, or 7. If it is, type a carriage return. If it is not, retype the line changing the second octal digit. From To 0 4 1 5 2 6 3 7 For example, 127413,,371520 would become; 167413,,371520<CR>
8	↑Z	Control-Z Exit FILDDT and return to TOPS-10 command mode.

Procedure 3 Gathering System Error Status

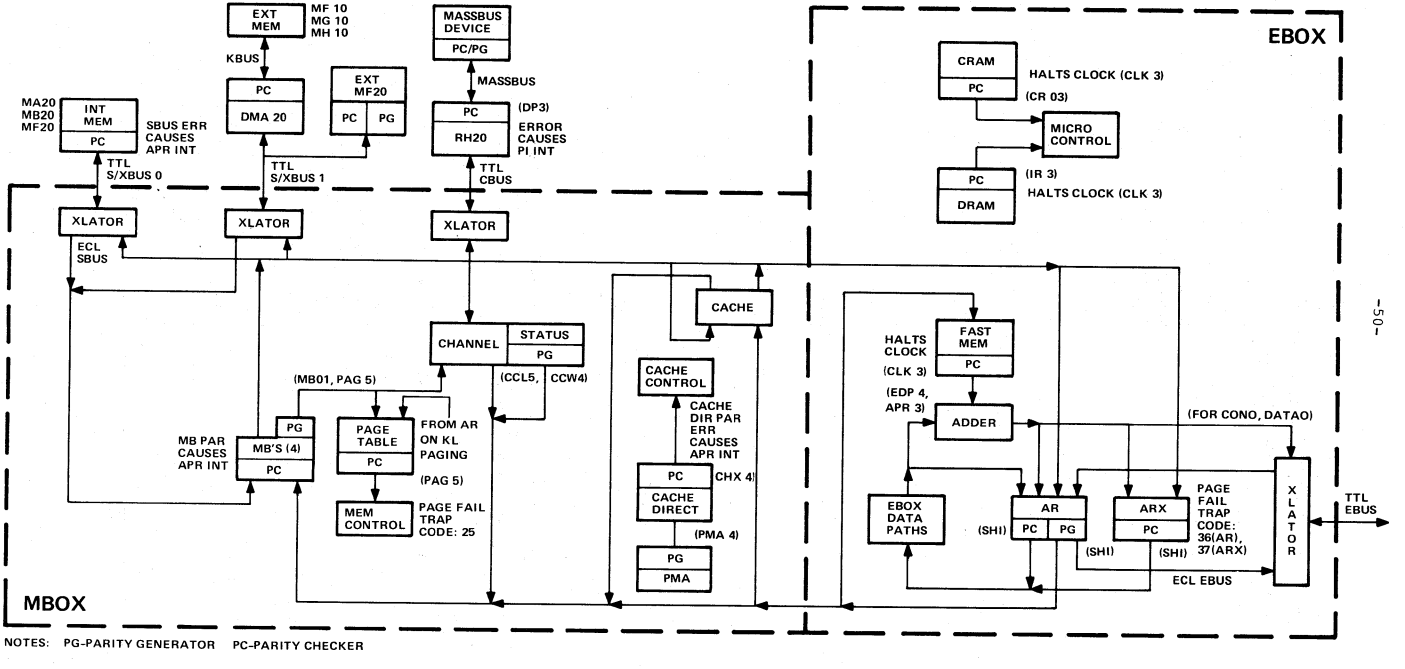
Step	PARSER Command	Comments
1	↑\	Enter PARSER.
2	SET CON MAINT<CR>	Request Maintenance Mode privileges.
3	EXAMINE DTE-20<CR>	Get current DTE20 status.
4	MCR BOO<CR>	Load BOO.TSK file.
5	DBOOT<CR>	Direct BOO to load and start KLDCP.
Step	**KLDCP Command**	**Comments**
6	EE 174434<CR>	Examine DTE STATUS register.
7	EE 174430<CR>	Examine DTE DIAG 1 register.
8	DE 174432:100<CR>	Reset the DTE.
9	FX 0<CR>	Turn off the clock.
10	ALL<CR>	Print all CRAM and registers
11	FR 110<CR>	Read APR.
12	FR 100,177<CR>	Read all diagnostic functions.
13	FX 1,FX 10,PC<CR>	Start the clock, stop the clock, get the PC.
14	FX 12,PC,FX 12,PC<CR>	Continue (momentarily) and get PC, continue (momentarily) and get the PC again. Perform this step several times.
15	EC<CR>	Examine the current CRAM location. Determine if the location is the halt loop location for the version of microcode in use by the system. If it is, proceed to step 19. If it is not, stop. The KL10 is hung in an unknown state and the remainder of the procedure cannot be executed.
16	FX 1<CR>	Turn on the clock.
17	EM 16,17<CR>	Examine ACs 16 and 17. If the examine works, proceed to step 21. If the examine fails, the KL10 is hung in an unknown state. Then do the following steps. a. Jumper 4F20E1 to ground. b. SM to KLDCP - reset machine and hold ERA valid. c. EX 700400 17, EM 17<CR> d. Remove the jumper. e. Do steps 21 and 24, then continue with procedure.
18	EX 700000 17,EM 17<CR>	BLKI APR(APRID) and print.
19	EX 700240 17,EM 17<CR>	CONI APR and print.
20	EX 701240 17,EM 17<CR>	CONI PAG and print.
21	EX 701040 17,EM 17<CR>	DATAI PAG and print.
22	EX 700400 17,EM 17<CR>	BLKI PI (RDERA) and print.
23	EX 720240 17,EM 17<CR>	CONI DTE (STATUS) and print.

Procedure 3 Gathering System Error Status (Cont)

Step	KLDCP Command (Cont)	Comments (Cont)
24	EM xxxxx500,xxxxx502<CR>	Examine PAGE FAIL location. Where xxxxx equals bits <23:35> of the DATAI PAG (UBR) refer to step 13. xxxxx500 = PAGE FAIL WORD xxxxx501 = PAGE FAIL PC and FLAGS xxxxx502 = PAGE FAIL PC
25	AC BLK 7<CR>	Select microcode AC block 7.
26	EM 0,2<CR>	Examine the AC block. AC0 = AR data for PAGE FAIL AC1 = ARX data for PAGE FAIL AC2 = I/O PAGE FAIL word
27	AC BLK 0<CR>	Select AC block 0.
INTERNAL MEMORY STATUS		
28	DM 16:0<CR>	Set up for BLKO PI (SBDIAG 0, controller 0)
29	EX 700500 16,EM 17<CR>	Execute SBDIAG0 and print E+1.
30	DM 16:1<CR>	Set up for BLKO PI (SBDIAG1, controller 0)
31	EX 700500 16,EM 17<CR>	Execute SBDIAG1 and print E+1.
32		Repeat steps 21 through 24 for each controller on the system by incrementing bits <00:04> of the BLKO PI word deposited in AC 16.
EXTERNAL MEMORY (DMA) STATUS		
33	DM 16:100000 0<CR>	Set up BLKO PI (SBDIAG 0, controller 4).
34	EX 700500 16,EM 17<CR>	Execute SBDIAG 0 and print E+1.
MASSBUS CONTROLLER (RH20) STATUS		
35	EX 754240 17,EM 17<CR>	CONI RH and print
36		Repeat step 28 for each RH20 on the system by changing the I/O device select code. RH20 CONI 1 754640 2 755240 3 755640 4 756240 5 756640 6 757240 7 757640
INTERNAL CHANNEL STATUS IF EBR IS EQUAL TO 0		
37	DM 600:540001 540000<CR>	Set up page table
38	EX 701200 20000<CR>	Turn paging on
39	EX 200740 1000,EM 17<CR>	Move CHAN 0 (INIT CMD) to AC17 and print.
40	EX 200740 1001,EM 17<CR>	Move CHAN 0 (ERROR STATUS) to AC17 and print.
41	EX 200740 1002,EM 17<CR>	Move CHAN 0 (STATUS) to AC17 and print.
42		Repeat steps 32 through 34 for each channel on the system. CHAN 1 (1004-1006) CHAN 2 (1010-1012) CHAN 3 (1014-1016) CHAN 4 (1020-1022) CHAN 5 (1024-1026) CHAN 6 (1030-1032) CHAN 7 (1034-1036)

Procedure 3 Gathering System Error Status (Cont)

Step	KLDCP Command (Cont)	Comments (Cont)
INTERNAL CHANNEL STATUS IF EBR IS GREATER THAN 0		
43	EM xxxxx000,xxxxx037	Examine channel locations. Where xxxxx equals bits <23:35> of the CONI PAG (EBR) refer to step 20. xxxxx000 = CHAN 0 INIT CMD xxxxx001 = CHAN 0 ERROR STATUS xxxxx002 = CHAN 0 STATUS xxxxx004 through xxxxx006 CHAN 1 xxxxx010 through xxxxx012 CHAN 2 xxxxx014 through xxxxx016 CHAN 3 xxxxx020 through xxxxx022 CHAN 4 xxxxx024 through xxxxx026 CHAN 5 xxxxx030 through xxxxx032 CHAN 6 xxxxx034 through xxxxx036 CHAN 7
RH20 DEVICE STATUS		
44	DM 16:000400 0<CR>	Set up DATAO RH to select reg 0 (DRCR).
45	EX 754140 16<CR>	DATAO RH select reg 0.
46	EX 754040 17,EM 17<CR>	DATAI RH print reg 0.
47	DM 16:010400 0<CR>	Set up DATAO RH to select reg 1 (DRSR).
48	EX 754140 16<CR>	DATAO RH select reg 1.
49	EX 754040 17,EM 17<CR>	DATAI RH print reg 1.
50	DM 16:020400 0<CR>	Set up DATAO RH to select reg 2 (DRER1).
51	EX 754140 16<CR>	DATAO RH select reg 2.
52	EX 754040 17,EM 17<CR>	DATAI RH print reg 2.
53	DM 16:140400 0<CR>	Set up DATAO RH to select reg 14 (DRER2).
54	EX 754140 16<CR>	DATAO RH select reg 14.
55	EX 754040 17,EM 17<CR>	DATAI RH print reg 14.
56	DM 16:150400 0<CR>	Set up DATAO RH to select reg 15 (DRER3)
57	EX 754140 16<CR>	DATAO RH select reg 15.
58	EX 754040 17,EM 17<CR>	DATAI RH print reg 15.
59		Repeat steps 37 through 51 for each device on the controller by incrementing bits <15:17> of the DATAO RH word deposited in AC 16. Repeat steps 37 through 52 for each controller on the system by changing the I/O device select code. RH20 DATAO DATAI 1 754540 754440 2 755140 755040 3 755540 755440 4 756140 756040 5 756540 756440 6 757140 757040 7 757540 757440


EBOX
MBOX
EXT MEM
MF 10
MG 10
MH 10
KBUS
PC
DMA 20
EXT MF20
PC
PG
MASSBUS DEVICE
PC/PG
MASSBUS
PC
RH20
(DP3)
ERROR CAUSES PI INT
TTL CBUS
MA20
MB20
MF20
INT MEM
PC
SBUS ERR CAUSES APR INT
TTL S/XBUS 0
TTL S/XBUS 1
XLATOR
XLATOR
XLATOR
ECL SBUS
CRAM
PC
HALTS CLOCK (CLK 3)
(CR 03)
MICRO CONTROL
PC
DRAM
(IR 3)
HALTS CLOCK (CLK 3)
CACHE
CHANNEL
STATUS
PG
(CCL5,
CCW4)
(MB01, PAG 5)
CACHE CONTROL
CACHE DIR PAR ERR CAUSES APR INT
PC
CACHE DIRECT
CHX 4)
(PMA 4)
PG
PMA
HALTS CLOCK
(CLK 3)
FAST MEM
PC
(EDP 4, APR 3)
ADDER
(FOR CONO, DATAO)
PG
MB'S (4)
PC
MB PAR CAUSES APR INT
PAGE TABLE
PC
FROM AR ON KL PAGING
(PAG 5)
MEM CONTROL
PAGE FAIL TRAP CODE: 25
EBOX DATA PATHS
AR
PC
PG
(SHI)
ARX
PC
(SHI)
(SHI)
PAGE FAIL TRAP CODE: 36(AR), 37(ARX)
ECL EBUS
XLATOR
TTL EBUS
NOTES: PG-PARITY GENERATOR PC-PARITY CHECKER

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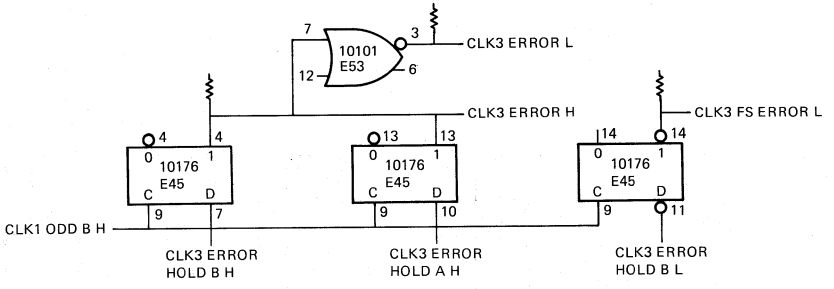
F/S PROBE



NOTE

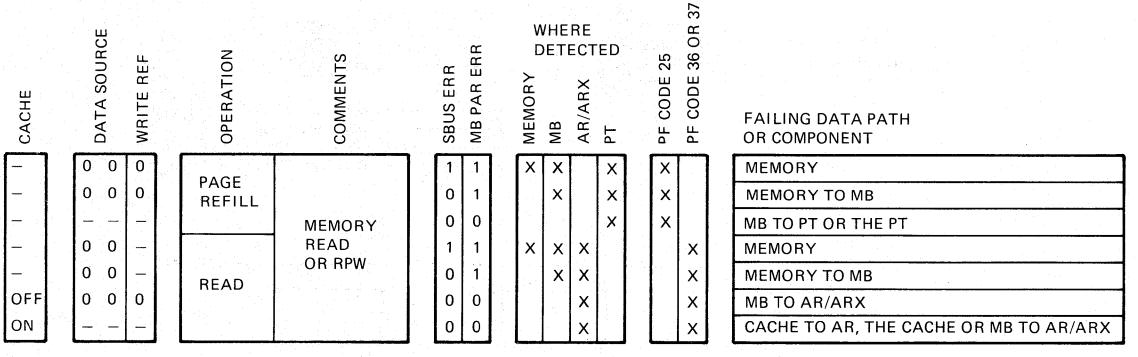
1 THIS LOGIC IS CHECKED ON EVERY MBOX CLOCK. IF THE ERROR STEP LOGIC IS USED ON EBOX SIGNALS THEN CLK EBOX SYNC SHOULD BE JUMPERED IN.

2 USE EBOX SYNC AS AN FS INPUT WHEN LOOKING AT EBOX SIGNALS.

MR-2301

3 WHEN USING NAND GATE FOR QUALIFIERS GROUND PIN EM1.

KL10 PAGE FAIL TRAPS (INT. MEM.)



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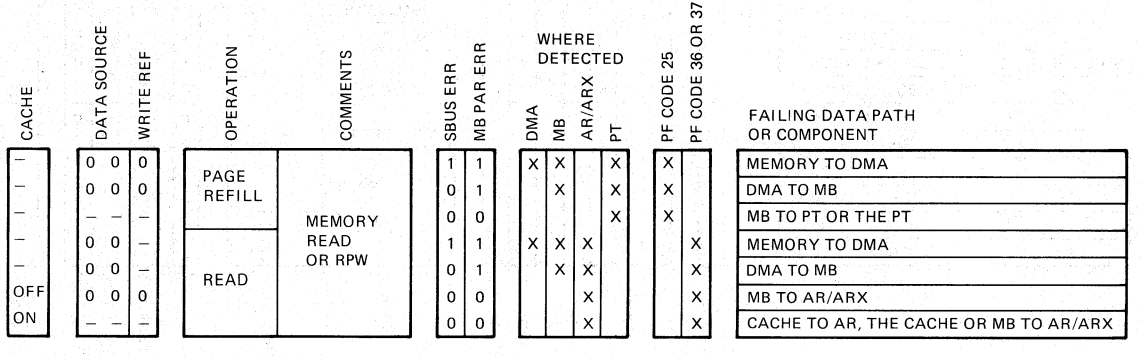
KL10 HARDWARE FAULTS (INT. MEM.)

CACHE	SWEEP REF	CHAN REF	DATA SOURCE		WRITE REF		OPERATION	COMMENTS	SBUS ERR	MB PAR ERR	WHERE DETECTED: MEMORY	MB	AR/ARX	PT	PF CODE 25	PF CODE 36 OR 37	FAILING DATA PATH OR COMPONENT
–	–	–	0	0	0		PAGE REFILL	MEMORY READ OR RPW	0	1		X		X	X		MEMORY TO MB
–	–	–	0	0	0				1	1	X	X		X	X		MEMORY
–	–	–	0	0	0		READ		0	1		X					MEMORY TO MB
–	–	–	0	0	0				1	1	X	X	X			X	MEMORY
–	–	–	0	0	0				0	1		X	X			X	MEMORY TO MB
–	0	1	0	0	0			CHAN DATA	0	1		X					MEMORY TO MB
ON	0	1	1	1	0				0	1		X					MB OR AR TO CACHE TO MB
–	0	1	0	1	1		WRITE		0	1		X					MASSBUS DEVICE TO RH TO CACHE TO MB
–	0	1	0	0	1			CHAN STATUS	0	1		X					CHAN TO MB
–	–	–	1	0	1			EBOX STORE	0	1		X					AR TO MB
–	–	–	–	–	–			RPW	1	0	X						MB TO MEMORY
ON	–	–	1	1	1			WRITEBACK	0	1		X					CACHE TO MB OR THE CACHE
ON	1	0	1	1	1		SWEEP		0	1		X					CACHE TO MB OR THE CACHE

MR-2422

KL10 PAGE FAIL TRAPS (EXT. MEM.)



KL10 HARDWARE FAULTS (EXT. MEM.)

CACHE	SWEEP REF	CHAN REF	DATA SOURCE	WRITE REF	OPERATION	COMMENTS	SBUS ERR	MB PAR ERR	WHERE DETECTED: DMA	WHERE DETECTED: MB	WHERE DETECTED: AR/ARX	WHERE DETECTED: PT	PF CODE 25	PF CODE 36 OR 37	FAILING DATA PATH OR COMPONENT
–	–	–	0 0	0	PAGE REFILL	MEMORY READ OR RPW	0	1		X		X	X		DMA TO MB
–	–	–	0 0	0			1	1	X	X		X	X		MEMORY TO DMA
–	–	–	0 0	0	READ		0	1		X					DMA TO MB
–	–	–	0 0	0			1	1	X	X	X			X	MEMORY TO DMA
–	–	–	0 0	0			0	1		X	X			X	DMA TO MB
–	0	1	0 0	0		CHAN DATA	1	1	X	X					MEMORY TO DMA
–	0	1	0 0	0			0	1		X					DMA TO MB
ON	0	1	1 1	0			0	1		X					AR OR MB TO CACHE TO MB
–	0	1	0 1	1	WRITE	CHAN STATUS	0	1		X					MASSBUS DEVICE TO RH TO CHAN TO MB
–	0	1	0 0	1		EBOX STORE	0	1		X					CHAN TO MB
–	–	–	1 0	1		RPW	0	1		X					AR TO MB
–	–	–	– –	–		WRITEBACK	1	0	X						MB TO DMA
ON	–	–	1 1	1			0	1		X					CACHE TO MB OR THE CACHE
ON	1	0	1 1	1	SWEEP		0	1		X					CACHE TO MB OR THE CACHE

MR-2420

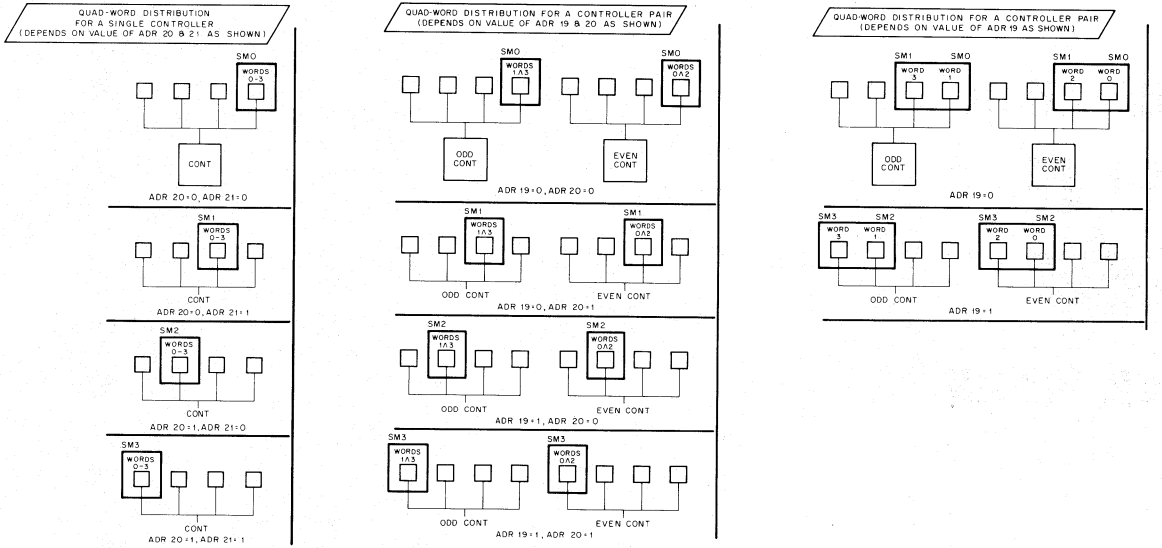
MEMORY ADDRESS MAP

Double spaced at 16K
Triple spaced at 64K

FROM	START	STOP	TO
0K	00	07777	4K
4K	10000	17777	8K
8K	20000	27777	12K
12K	30000	37777	16K
16K	40000	47777	20K
20K	50000	57777	24K
24K	60000	67777	28K
28K	70000	77777	32K
32K	100000	107777	36K
36K	110000	117777	40K
40K	120000	127777	44K
44K	130000	137777	48K
48K	140000	147777	52K
52K	150000	157777	56K
56K	160000	167777	60K
60K	170000	177777	64K
64K	200000	207777	68K
68K	210000	217777	72K
72K	220000	227777	76K
76K	230000	237777	80K
80K	240000	247777	84K
84K	250000	257777	88K
88K	260000	267777	92K
92K	270000	277777	96K
96K	300000	307777	100K
100K	310000	317777	104K
104K	320000	327777	108K
108K	330000	337777	112K
112K	340000	347777	116K
116K	350000	357777	120K
120K	360000	367777	124K
124K	370000	377777	128K
128K	400000	407777	132K
132K	410000	417777	136K
136K	420000	427777	140K
140K	430000	437777	144K
144K	440000	447777	148K
148K	450000	457777	152K
152K	460000	467777	156K
156K	470000	477777	160K
160K	500000	507777	164K
164K	510000	517777	168K
168K	520000	527777	172K
172K	530000	537777	176K
176K	540000	547777	180K
180K	550000	557777	184K
184K	560000	567777	188K
188K	570000	577777	192K

192K	600000	607777	196K
196K	610000	617777	200K
200K	620000	627777	204K
204K	630000	637777	208K
208K	640000	647777	212K
212K	650000	657777	216K
216K	660000	667777	220K
220K	670000	677777	224K
224K	700000	707777	228K
228K	710000	717777	232K
232K	720000	727777	236K
236K	730000	737777	240K
240K	740000	747777	244K
244K	750000	757777	248K
248K	760000	767777	252K
252K	770000	777777	256K

MA20 1, 2 AND 4-WAY INTERLEAVING



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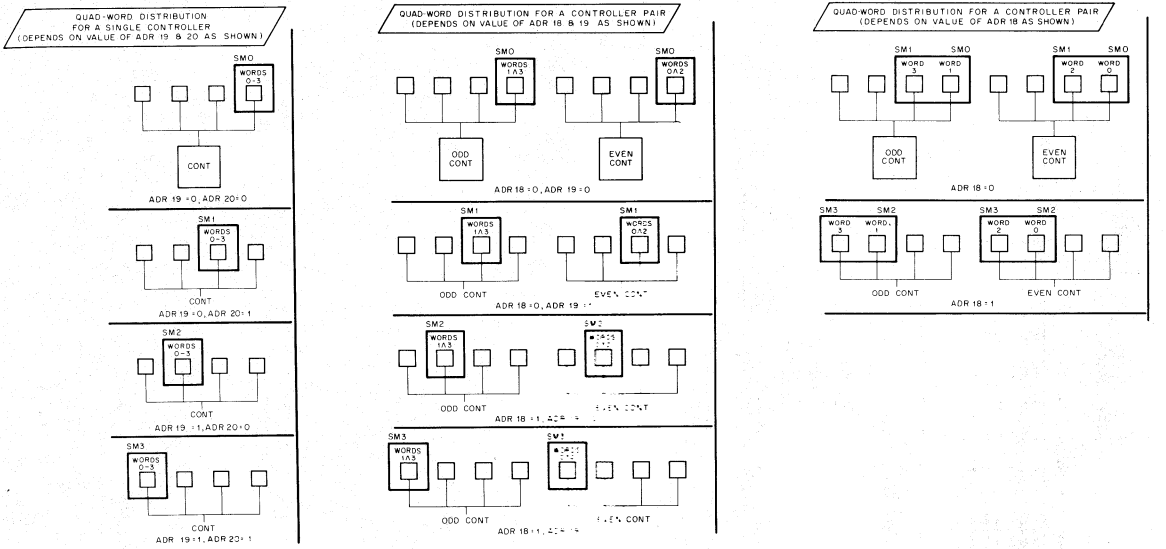
MB20 1, 2 AND 4-WAY INTERLEAVING



MR-2070

MAGTAPE FORMATS

7 TRACK

TRACK 7	P	P	P	P	P	P	/	C
TRACK 6	0	6	12	18	24	30	/	B
TRACK 5	1	7	13	19	25	31	L	A
TRACK 4	2	8	14	20	26	32	P	8
TRACK 3	3	9	15	21	27	33	C	4
TRACK 2	4	10	16	22	28	34	C	2
TRACK 1	5	11	17	23	29	35	/	1

REFERENCE EDGE

9 TRACK (INDUSTRY COMPATIBILITY MODE)

TRACK 9	4	12	20	28	/	/	4	
TRACK 8	6	14	22	30	/	/	6	
TRACK 7	0	8	16	24	/	/	0	
TRACK 6	1	9	17	25	C	L	1	
TRACK 5	2	10	18	26	R	P	2	
TRACK 4	P	P	P	P	C	C	C	
TRACK 3	3	11	19	27	/	/	3	
TRACK 2	7	15	23	31	/	/	7	
TRACK 1	5	13	21	29	/	/	5	

REFERENCE EDGE

9 TRACK (CORE DUMP MODE)

TRACK 9	4	12	20	28	32	/	/	4
TRACK 8	6	14	22	30	34	/	/	6
TRACK 7	0	8	16	24		/	/	0
TRACK 6	1	9	17	25		C	L	1
TRACK 5	2	10	18	26	30	R	P	2
TRACK 4	P	P	P	P	P	C	C	C
TRACK 3	3	11	19	27	31	/	C	3
TRACK 2	7	15	23	31	35	/	/	7
TRACK 1	5	13	21	29	33	/	/	5

REFERENCE EDGE

RELATIONSHIP BETWEEN TRACK NO. AND CRC REGISTER BIT POSITIONS:

TRACK NO	1	2	3	4	5	6	7	8	9
CRC REG, BIT	7	9	5	1	4	3	2	8	6

NOTES

TX0x/TU7x SENSE BYTES

BYTE I T	0 (8)	1 (4)	2 (2)	3 (1)	4 (8)	5 (4)	6 (2)	7 (1)	BYTE I T
0	COMMAND REJECT	INTERVENTION REQUIRED	BUS OUT CHECK	EQUIPMENT CHECK	DATA CHECK	OVERRUN	WORD COUNT ZERO	DATA CONVERT CHECK	0
1	NOISE	TU STATUS A	TU STATUS B	7-TRK	LOAD POINT	SELECTED & WR STAT	FILE PROTECTED	NOT CAPABLE	1
2	TRACK IN ERROR								2
3	R/W VRC	MTE/LRC	SKEW ERROR	END DATA CK /CRC	ENV CK/ SKEW VRC	1600 BPI SET IN TU	BACKWARD	C/P COMP.	3
4		REJECT TU	TI	WRITE TRG VRC		LWR	TU CHECK	RPQ	4
5		NEW SUBSYSTEM	WTM ** CHECK	ID BURST ** CK	START * READ CHECK	PARTIAL ** RECORD	POSTAMBLE ** ERROR	RPQ	5
6	7-TRK ** TU	WRITE ** CURRENT FAIL	DUAL *** DENSITY TU	NOT ** 1600	TAPE UNIT MODEL IDENTIFICATION				6
7	COLUMN *** TOP OR BTM	LEFT. COL. FAIL ***	RIGHT COL. FAIL ***	RESET *** KEY	DSE FAILURE	ERASE HD *** FAILURE		LOAD *** FAILURE	7
8	IBG ** DETECTED								8
9	6250 *** CORRECTION	VELOCITY CHANGE	CHANNEL ** BUFFER CK	CRC III **	6250 **			TCU RESERVED	9
10	CMND STAT REJECT **			RECORD NOT DETECTED		TACH START FAIL **		VELOCITY ** CHECK	10
11									11

* TX01 ONLY ** TX02 ONLY *** TU72 ONLY

MR-2309

12									12
13	CU FEATURES			CONTROL UNIT UNIQUE IDENTIFICATION (HI-ORDER PART S/N) 4096	2048	1024	512	256	13
14	128	64	32	CONTROL UNIT UNIQUE IDENTIFICATION (LO–ORDER PART S/N) 16	8	4	2	1	14
15			8192	TAPE UNIT UNIQUE IDENTIFICATION (HI–ORDER PART S/N) 4096	2048	1024	512	256	15
16	128	64	32	TAPE UNIT UNIQUE IDENTIFICATION (LO–ORDER PART S/N) 16	8	4	2	1	16
17	2 CH SW FEATURE	SWITCH FEATURES			REFLECTS TCU DIAGNOSTIC RELEASE LEVEL				17
18		SAME	TU	I.D.	TU		E.C. LEVEL		18
19	TU 7	TU 6	TU 5	BUSY STATUS, LO–ORDER TAPE UNITS TU 4	TU 3	TU 2	TU1	TU 0	19
20	TU F	TU E	TU D	BUSY STATUS, HI–ORDER TAPE UNITS TU C	TU B	TU A	TU9	TU 8	20
21									21
22	"REFER TO MICROPROGRAM PAGE QA025" **								22
23	MOD IV TCU **	"REFER TO MICROPROGRAM PAGE AQ025" **							23
BYTE I T	0 (8)	1 (4)	2 (2)	3 (1)	4 (8)	5 (4)	6 (2)	7 (1)	BYTE I T

* TX01 ONLY ** TX02 ONLY *** TU72 ONLY

MR-2310

DIAGNOSTIC FUNCTIONS

KL10(PA and PV) Diagnostic Execute (Control) Functions

Function	Mnemonic	Operation
CLOCK CONTROL		
00	STPCLK	STOP THE KL10 CLOCK
01	STRCLK	START THE KL10 CLOCK
02	SSCLK	SINGLE STEP THE MBOX CLOCK
03	SECLK	SINGLE STEP THE EBOX CLOCK. LEAVES THE EBOX CLOCK FALSE AND EBOX SYNC TRUE. CAUSES (2,3) MBOX CLOCKS DEPENDING ON EBOX CLOCK INITIALLY (FALSE,TRUE). DOES NOT DEPEND ON 'T' FIELD OR MB WAIT.
04	CECLK	CONDITIONALLY ISSUE AN MBOX CLOCK IF THE EBOX CLOCK IS TRUE. MAKES EBOX CLOCK FALSE. IF ISSUED IN THE MASTER RESET STATE,LEAVES EBOX SYNC TRUE.
05	BRCLK	ISSUE A BURST OF CLOCKS. THE NUMBER OF MBOX CLOCKS DESIRED (1-255) HAS BEEN LOADED PREVIOUSLY BY FUNCTIONS 42,43.
06	CLRMR	CLEAR MASTER RESET STATE.
07	SETMR	SET MASTER RESET STATE. RUNNING THE CLOCK WHILE IN THIS STATE 'CLEARS' THE KL10.
EBOX CONTROL		
10	CLRRUN	CLEAR THE RUN FLOP. MAKE THE MICRO-CODE GO TO THE "HALT LOOP".
11	SETRUN	SET THE RUN FLOP. ALLOW REPEATED INSTRUCTION EXECUTION.
12	CONBUT	SET THE CONTINUE FLOP (MOMENTARY). ALLOW THE MICROCODE TO LEAVE THE HALT LOOP.
14	IRLTCH	UNLATCH THE IR AND LOAD IT FROM THE AD.
15	DRLTCH	UNLATCH THE DRAM REGISTER AND ALLOW IT TO LOAD FROM THE RAMS.

KL10(PA and PV) Diagnostic Write Functions

CLOCK 'LOAD' FUNCTIONS.

42	LDBRR	LOAD THE RIGHTHAND 4 BITS OF THE 8-BIT BURST COUNTER FROM EBUS BITS 32-35
43	LDBRL	LOAD THE LEFTHAND 4 BITS OF THE BURST CTR.
44	LDSEL	LOAD THE CLOCK SOURCE AND RATE SELECT REGISTER:

32	33	SOURCE	34	35	RATE
0	0	NORM XTAL	0	0	NORMAL
0	1	FAST XTAL	0	1	DIVIDE BY 2
1	0	EXTERN	1	0	DIVIDE BY 4
1	1	FAST XTAL	1	1	DIVIDE BY 8

45	LDDIS	LOAD THE REGISTER WHICH CONTROLS THE EBOX CLOCK DISTRIBUTION.

BIT	ACTION
33	DISABLE CONTROL RAM CLOCK
34	DISABLE DATA PATHS CLOCK
35	DISABLE CONTROL LOGIC CLOCK

46	LDCHK1	LOAD THE CONDITION-CHECKING ENABLE REGISTER: THESE ALL ENABLE THE CLOCK TO STOP AND SHOULD BE USED IN CONJUNCTION WITH BIT 35 OF FUNCTION 47.

BIT	FUNCTION
32	CHECK FM PARITY
33	CHECK CRAM PARITY
34	CHECK DRAM PARITY
35	CHECK FIELD SERVICE 'PROBE'

47	LDCHK2	LOAD THE ENABLE/DISABLE FUNCTION REGISTER:

BIT	FUNCTION
32	DISABLE EBOX REQUESTS TO MBOX
33	SIMULATE AN MB RESP FOR EACH MB WAIT.
34	CHECK AR AND ARX PARITY AND CAUSE A 'PAGE FAIL' UCODE TRAP IF ERROR.
35	MUST BE SET TO PERFORM DESIRED ACTION OF FUNCTION 46 (ABOVE). STOPS ALL CLOCKS IF AN ERROR IS DETECTED.

CONTROL RAM LOAD FUNCTIONS

51	LCRDAR	00-05	CRAM DIAG ADR 05-10
52	LCRDAL	01-05	CRAM DIAG ADR 00-04
53	LCRAM5	00-05	EA CALL & DISP 00-04

		BITS	
		EBUS	CRAM
54	LCRAM4	08	60
		10	62
		14	64
		16	66
		20	68
		22	70
		26	72
		28	74
		32	76
		34	78
55	LCRAM3	08-11	40-43
		14-7	44-47
		20-23	48-51
		26-29	52-55
		32-35	56-59
56	LCRAM2	08-11	20-23
		14-17	24-27
		20-23	28-31
		26-29	32-35
		32-35	36-39
57	LCRAM1	08-11	00-03
		14-17	04-07
		20-23	08-11
		26-29	12-15
		32-35	16-19

NOTE
ODD NUMBERED BITS ABOVE 60 ARE NONEXISTENT.

LOAD DRAM FUNCTIONS

		BITS	
60	LDRAM1	12-14	DRAM A00-02, EVEN ADDRESSES
		15-17	DRAM B00-02, EVEN ADDRESSES
61	LDRAM2	12-14	DRAM A00-02, ODD ADDRESSES
		15-17	DRAM B00-02, ODD ADDRESSES
62	LDRAM3	14-17	COMMON J01-04
63	LDRJEV	15-17	J08-10, EVEN ADDRESSES
		12	PARITY BIT, EVEN ADDRESSES
64	LDRJOD	14	COMMON J07 (NOTE: J05 AND J06 DO NOT EXIST.)
		15-17	J08-10, ODD ADDRESSES
		12	PARITY BIT, ODD ADDRESSES

IR, DRAM CONTROL FUNCTIONS

65	DISIOJ	DISABLE SPECIAL DECODE OF OP CODES 254,7XX.
66	DISACF	DISABLE IR AC OUTPUTS.
67	ENIOJA	ENABLE KL10 STYLE DECODING OF OP CODES AND AC'S.

CHANNEL CONTROL FUNCTIONS

70 THIS FUNCTION IS USED TO ESTABLISH CERTAIN CONDITIONS WITHIN THE CHANNEL NEEDED FOR DEVICELESS TESTING. THIS FUNCTION SHOULD NOT BE USED WITHOUT PROPER TIMING SYNCHRONIZATION.

EBUS BIT	OPERATION
06	SIMULATE CBUS RESET
07	SIMULATE CBUS START
09	SIMULATE CBUS DONE
10	SIMULATE CBUS CTOM
11	SIMULATE CBUS STORE
12	SET DIAG SLOW REQ
13	SET DIAG FAST REQ

MBOX CONTROL FUNCTIONS

71 LDMBXA — CONTROL OF THE MEMORY TO CACHE SELECTOR (MEM TO C SEL 1,2) IS GIVEN THROUGH THE FUNCTION LDMBXA (071) USING SIX EBUS BITS TO LOAD A CONTROL REGISTER. THIS REGISTER IS NOT INITIALIZED BY MR RESET AND THEREFORE MUST BE LOADED BEFORE NORMAL USE OF THE KL10.

BITS	FUNCTION
34 35	CONTROL MEM TO CACHE MIXER ENABLE
0 0	UNDEFINED
0 1	FORCE MIXER ENABLE
1 0	ALLOW NORMAL OPERATION. MR RESET STATE
1 1	UNDEFINED

32 33	SELECT THE SOURCE OF SEL 2 AND SEL 1
0 0	INCLUSIVE OR BITS 30 AND 31 WITH THE NORMAL SOURCE OF SEL 2 AND SEL 1, RESPECTIVELY.
0 1	REPLACE NORMAL SOURCE WITH BITS 30, 31.
1 0	ALLOW ONLY THE NORMAL INPUTS. THIS IS WHAT THE CONSOLE SHOULD SUPPLY FOR NORMAL OPERATION.
1 1	FORCE SEL 2 AND SEL 1 FALSE. SELECT AR

30 31	(INVERTED) INPUTS TO SEL 2, SEL 1
1 1	SELECT AR
1 0	SELECT MB
0 1	SELECT MEM

72 — TO CHANGE THE KW20 CLOCK FREQUENCY, EXECUTE FUNCTION WRITE 72.

BITS	FUNCTION
34 35	MOS CLOCK CONTROL
0 0	EXT CLK
0 1	31 MHZ
1 0	25 MHZ
1 1	30 MHZ

NOTE THE FOLLOWING FUNCTION (76) MUST BE INITIALIZED BY THE CONSOLE MASTER RESET SOFTWARE.

76

SBUS CONTROLLER RESET
24=1 WILL SET THE MEM RESET FLIP-FLOP
24=0 WILL CLEAR THE MEM RESET FLIP-FLOP

TO CLEAR ALL MEMORY CONTROLLERS, SET THE MEM RESET FLIP-FLOP, RUN THE CLOK, THEN CLEAR THE MEM REST FLIP-FLOP.

CHANNEL CLOCK CONTROL

25=1 INHIBIT MBOX CLOCK DISTRIBUTION TO THE CHANNEL LOGIC.
25=0 ENABLE MBOX CLOCK DISTRIBUTION TO THE CHANNEL LOGIC

EBUS REGISTER LOAD ENABLE

26=1 ENABLE EBUS REGISTER LOADING ON EVERY CLOCK TICK
26=0 DISABLE EBUS REGISTER LOADING ON EVERY CLOCK TICK

FORCE EXTENDED ADDRESSING (KL10(PV) ONLY)

27=1 CAUSES THE EFFECTIVE ADDRESS CALCULATIONS TO OCCUR AD IF THE VMA, PC & PCS SECTIONS WERE NONZERO IN ANY SECTION. TRUE UNTIL A FUNCTION WRITE 76 WITH BIT 27=0 IS EXPECTED.

AR LOAD FUNCTION

77 LDAR — 0-35 LOAD THE AR FROM EBUS 0-35.

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	100	03	PIC1	M8532	PIC1 PIH1 H
**	100	04	PIC1	M8532	PIC1 PIH2 H
**	100	05	PIC1	M8532	PIC1 PIH3 H
**	100	06	PIC1	M8532	PIC1 PIH4 H
**	100	07	PIC1	M8532	PIC1 PIH5 H
**	100	08	PIC1	M8532	PIC1 PIH6 H
**	100	09	PIC1	M8532	PIC1 PIH7 H
	100	10	PIC1	M8532	PIC1 ACTIVE H
**	100	11	PIC1	M8532	PIC1 ON 1 H
**	100	12	PIC1	M8532	PIC1 ON 2 H
**	100	13	PIC1	M8532	PIC1 ON 3 H
**	100	14	PIC1	M8532	PIC1 ON 4 H
**	100	15	PIC1	M8532	PIC1 ON 5 H
**	100	16	PIC1	M8532	PIC1 ON 6 H
**	100	17	PIC1	M8532	PIC1 ON 7 H
**	100	18	MCL3	M8530	VMA HELD OR PC 01 H
**	100	19	MCL3	M8530	VMA HELD OR PC 02 H
**	100	20	MCL3	M8530	VMA HELD OR PC 03 H
**	100	21	MCL3	M8530	VMA HELD OR PC 04 H
**	100	22	MCL3	M8530	VMA HELD OR PC 05 H
**	100	23	MCL3	M8530	VMA HELD OR PC 06 H
	100	24	CTL1	M8527	CTL SPEC/SCM ALT H
	100	25	CTL1	M8527	CTL SPEC/SAVE FLAGS L
	100	26	CTL2	M8527	CTL ARL SEL 2 H
	100	27	CTL2	M8527	CTL ARR LOAD A L
	100	28	CTL2	M8527	CTL AR 00-08 LOAD L
	100	30	CLK1	M8526	CLK EBUS CLK H
	100	31	CLK1	M8526	CLK SBUS CLK H
	100	33	CLK5	M8526	CLK BURST CNT=0 H
**	100	34	CLK5	M8526	CLK BURST 128 H
**	100	35	CLK5	M8526	CLK BURST 64 H
**	101	11	PIC1	M8532	PIC1 GEN 1 H
**	101	12	PIC1	M8532	PIC1 GEN 2 H
**	101	13	PIC1	M8532	PIC1 GEN 3 H
**	101	14	PIC1	M8532	PIC1 GEN 4 H
**	101	15	PIC1	M8532	PIC1 GEN 5 H
**	101	16	PIC1	M8532	PIC1 GEN 6 H
**	101	17	PIC1	M8532	PIC1 GEN 7 H
**	101	18	MCL3	M8530	VMA HELD OR PC 07 H
**	101	19	MCL3	M8530	VMA HELD OR PC 08 H
**	101	20	MCL3	M8530	VMA HELD OR PC 09 H
**	101	21	MCL3	M8530	VMA HELD OR PC 10 H
**	101	22	MCL3	M8530	VMA HELD OR PC 11 H
**	101	23	MCL3	M8530	VMA HELD OR PC 12 H
	101	24	CTL1	M8527	CTL SPEC/CLR FPD H
	101	25	CTL1	M8527	CTL SPEC MTR CTL L
	101	26	CTL2	M8527	CTL ARL SEL 1 H
	101	27	CTL2	M8527	CTL ARR LOAD B L
	101	28	CTL2	M8527	CTL AR 09-17 LOAD L
**	101	30	CLK5	M8526	CLK BURST 32 H
**	101	31	CLK5	M8526	CLK BURST 16 H
**	101	32	CLK5	M8526	CLK BURST 08 H
**	101	33	CLK5	M8526	CLK BURST 04 H
**	101	34	CLK5	M8526	CLK BURST 02 H
**	101	35	CLK5	M8526	CLK BURST 01 H
**	102	11	PIC4	M8532	EBUS CS05 E H
**	102	12	PIC4	M8532	EBUS CS06 E H
	102	13	PIC2	M8532	EBUS DEMAND E H
**	102	14	PIC4	M8532	EBUS CS00 E H
**	102	15	PIC4	M8532	EBUS CS01 E H
**	102	16	PIC4	M8532	EBUS CS02 E H
**	102	17	PIC4	M8532	EBUS CS03 E H
	102	18	MCL2	M8530	MCL VMA READ H
	102	19	MCL1	M8530	MCL MEM/ARL IND H
	102	20	MCL2	M8530	MCL PAGE TEST PRIVATE H
	102	21	MCL4	M8530	MCL XR PREVIOUS H
	102	22	MCL4	M8530	MCL VMA GETS AD H
	102	23	MCL5	M8530	ARMM 12 H
	102	24	CTL1	M8527	CTL SPEC/GEN CRY 18 H
	102	25	CTL1	M8527	CTL COND/AR GETS EXP H
	102	26	CTL2	M8527	CTL ARR SEL 2 H
	102	27	CTL2	M8527	CTL MQM SEL 2 H
	102	28	CTL2	M8527	CTL ARX LOAD H
	102	30	CLK1	M8526	CLK ERROR STOP H
	102	31	CLK2	M8526	CLK GO L
	102	32	CLK4	M8526	CLK EBOX REQ H
	102	33	CLK3	M8526	CLK SYNC H
	102	34	CLK4	M8526	CLK PAGE FAIL EN L
	102	35	CLK4	M8526	CLK FORCE 1777 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING BOARD	NAME AND TRUTH
	103	11	PIC2 M8532	PIC2 TIMER DONE H
	103	12	PIC5 M8532	PIC5 EBUS PI GRANT H
	103	13	PIC2 M8532	PIC2 STATE HOLD H
**	103	14	PIC4 M8532	EBUS CS04 E H
	103	15	PIC2 M8532	PIC2 HONOR INTERNAL H
	103	16	PIC2 M8532	PIC2 READY H
	103	17	PIC5 M8532	PIC5 EBUS REQ H
	103	18	MCL2 M8530	MCL VMA PAUSE H
	103	19	MCL1 M8530	MCL REQ EN L
	103	20	MCL3 M8530	MCL VMA UPT H
	103	21	MCL4 M8530	MCL PREV COND L
	103	22	MCL4 M8530	MCL VMA INC H
	103	23	MCL5 M8530	MCL PREV SEC TO ARMM H
	103	24	CTL1 M8527	CTL SPEC/SECTION HOLD H
	103	25	CTL1 M8527	CTL DISP RET L
	103	26	CTL2 M8527	CTL ARR SEL 1 H
	103	27	CTL2 M8527	CTL MQM SEL 1 H
	103	28	CTL2 M8527	CTL ARL SEL 4 H
	103	30	CLK3 M8526	CLK DRAM PAR ERR H
	103	31	CLK2 M8526	CLK BURST L
	103	32	CLK4 M8526	CLK MB XFER H
	103	33	CLK4 M8526	CLK EBOX CLK L
	103	34	CLK4 M8526	CLK INSTR 1777 H
	103	35	CLK4 M8526	CLK 1777 EN H
	104	18	MCL2 M8530	MCL VMA WRITE H
	104	19	MCL2 M8530	MCL VMA USER H
	104	20	MCL3 M8530	MCL PAGE UEBR REF H
	104	21	MCL4 M8530	MCL VMAX EN L
	104	22	MCL4 M8530	MCL LOAD VMA CONTEXT L
	104	23	MCL6 M8530	MCL EBOX CACHE L
	104	24	CTL1 M8527	CTL SPEC/FLAG CTL H
	104	25	CTL1 M8527	CTL LOAD PC L
	104	26	CTL2 M8527	CTL ARXL SEL 2 H
	104	27	CTL2 M8527	CTL MQ SEL 2 H
	104	28	CTL2 M8527	CTL AR 00-11 CLR H
	104	30	CLK3 M8526	CLK CRAM PAR ERR H
	104	31	CLK2 M8526	CLK EBOX SS L
	104	32	CLK5 M8526	CLK SOURCE SEL 2 H
	104	33	CLK3 M8526	CLK EBOX SOURCE H
	104	34	CLK5 M8526	CLK FM PAR CHECK L
	104	35	CLK5 M8526	CLK MBOX CYCLE DIS H
	105	18	MCL2 M8530	MCL LOAD AR H
	105	19	MCL2 M8530	MCL VMA PUBLIC H
	105	20	MCL3 M8530	MCL PAGE ADDRESS COND H
	105	21	MCL4 M8530	MCL VMAX SEL 2 H
	105	22	MCL4 M8530	MCL 23 BIT EA H
	105	23	MCL6 M8530	MCL EBOX MAY BE PAGED L
	105	24	CTL1 M8527	CTL SPEC/SP MEM CYCLE H
	105	25	CTL1 M8527	CTL ADX CRY 36 H
	105	26	CTL2 M8527	CTL ARXL SEL 1 H
	105	27	CTL2 M8527	CTL MQ SEL 1 H
	105	28	CTL2 M8527	CTL AR 12-17 CLR H
	105	30	CLK3 M8526	CLK FM PAR ERR H
	105	31	SHD1 M8526	SH AR PAR ODD H
	105	32	CLK5 M8526	CLK SOURCE SEL 1 H
	105	33	CLK5 M8526	CLK EBOX CRM DIS H
	105	34	CLK5 M8526	CLK CRAM PAR CHECK L
	105	35	CLK5 M8526	CLK MBOX RESP SIM L
	106	18	MCL2 M8530	MCL LOAD ARX H
	106	19	MCL2 M8530	MCL VMA PREVIOUS L
	106	20	MCL3 M8530	MCL PAGE ILL ENTRY H
	106	21	MCL4 M8530	MCL VMAX SEL 1 H
	106	22	MCL4 M8530	MCL 18 BIT EA H
	106	23	MCL6 M8530	MCL REG FUNC H
	106	24	CTL1 M8527	CTL AD LONG H
	106	25	CTL1 M8527	CTL ADX CRY 36 A H
	106	26	CTL2 M8527	CTL ARXR SEL 2 H
	106	27	CTL2 M8527	CTL MQM EN H
	106	28	CTL2 M8527	CTL ARR CLR H
	106	30	CLK3 M8526	CLK FS ERROR H
	106	31	SHD1 M8526	SH ARX PAR ODD H
	106	32	CLK5 M8526	CLK RATE SEL 2 H
	106	33	CLK5 M8526	CLK EBOX EDP DIS H
	106	34	CLK5 M8526	CLK DRAM PAR CHECK L
	106	35	CLK5 M8526	CLK AR/ARX PAR CHECK L
	107	18	MCL2 M8530	MCL STORE AR L
	107	19	MCL2 M8530	MCL VMA EXTENDED L
	107	20	MCL4 M8530	MCL EA TYPE 10 H
	107	21	MCL4 M8530	MCL EA TYPE 09 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	107	22	MCL5	M8530	MCL MBOX CYC REQ H
	107	23	MCL6	M8530	MCL EBOX MAP L
	107	24	CTL1	M8527	CTL INH CRY 18 L
	107	25	CTL3	M8527	DIAG MEM RESET H
	107	26	CTL2	M8527	CTL ARXR SEL 1 H
	107	27	CTL3	M8527	DIAG LOAD EBUS REG L
	107	28	CTL2	M8527	CTL SPEC CALL L
	107	30	CLK3	M8526	CLK ERROR L
	107	31	CLK4	M8526	CLK PAGE FAIL H
	107	32	CLK5	M8526	CLK RATE SEL 1 H
	107	33	CLK5	M8526	CLK EBOX CTL DIS H
	107	34	CLK5	M8526	CLK FS CHECK L
	107	35	CLK5	M8526	CLK ERR STOP EN L
	110	01	APR2	M8539	APR SWEEP BUSY EN H
	110	06	APR1	M8539	APR SBUS ERR IN H
	110	07	APR1	M8539	APR NXM ERR IN H
	110	08	APR1	M8539	APR I/O PF ERR IN H
	110	09	APR1	M8539	APR MB PAR ERR IN H
	110	10	APR2	M8539	APR C DIR P ERR IN H
	110	11	APR2	M8539	APR S ADR P ERR IN H
	110	12	APR2	M8539	APR PWR FAIL IN H
	110	13	APR2	M8539	APR SWEEP DONE IN H
	110	14	APR2	M8539	APR APR INTERRUPT H
	110	15	PIC3	M8539	PI3 APR PIA 04 H
	110	16	PIC3	M8539	PI3 APR PIA 02 H
	110	17	PIC3	M8539	PI3 APR PIA 01 H
*	110	20-35	MTR1	M8538	MTR TIME 02-17 H
	111	06	APR5	M8539	APR CURRENT BLOCK 4 H
	111	07	APR5	M8539	APR CURRENT BLOCK 2 H
	111	08	APR5	M8539	APR CURRENT BLOCK 1 H
	111	09	APR5	M8539	APR PREV BLOCK 4 H
	111	10	APR5	M8539	APR PREV BLOCK 2 H
	111	11	APR5	M8539	APR PREV BLOCK 1 H
	111	12	APR3	M8539	APR CWSX H
	111	13	APR3	M8539	APR PREV SEC 13 H
	111	14	APR3	M8539	APR PREV SEC 14 H
	111	15	APR3	M8539	APR PREV SEC 15 H
	111	16	APR3	M8539	APR PREV SEC 16 H
	111	17	APR3	M8539	APR PREV SEC 17 H
*	111	20-35	MTR1	M8538	MTR PERF COUNT 02-17 H
	112	06	APR1	M8539	APR SBUS ERR EN IN H
	112	07	APR1	M8539	APR NXM ERR EN IN H
	112	08	APR1	M8539	APR I/O PF ERR EN IN H
	112	09	APR1	M8539	APR MB PAR ERR EN IN H
	112	10	APR2	M8539	APR C DIR P ERR EN IN H
	112	11	APR2	M8539	APR S ADR P ERR EN IN H
	112	12	APR2	M8539	APR PWR FAIL EN IN H
	112	13	APR2	M8539	APR SWEEP DONE EN IN H
*	112	20-35	MTR1	M8538	MTR EBOX COUNT 02-17 H
	113	09	APR3	M8539	APR FETCH COMP H
	113	10	APR3	M8539	APR READ COMP H
	113	11	APR3	M8539	APR WRITE COMP H
	113	12	APR3	M8539	APR USER COMP H
*	113	20-35	MTR1	M8538	MTR CACHE COUNT 02-17 H
	114	07	APR5	M8539	APR MBOX CTL 03 H
**	114	08	APR5	M8539	APR FM BLOCK 4 H
**	114	09	APR5	M8539	APR FM BLOCK 2 H
**	114	10	APR5	M8539	APR FM BLOCK 1 H
**	114	11	APR4	M8539	APR FM ADR 10 H
**	114	12	APR4	M8539	APR FM ADR 4 H
**	114	13	APR4	M8539	APR FM ADR 2 H
**	114	14	APR4	M8539	APR FM ADR 1 H
	114	15	APR4	M8539	APR F02 EN H
	114	16	APR3	M8539	APR FM 36 H
	114	17	APR3	M8539	APR FM ODD PARITY H
*	114	24-35	MTR1	M8538	MTR INTERVAL 06-17 H
	115	07	APR5	M8539	APR MBOX CTL 06 H
	115	08	APR5	M8539	APR SET PAGE FAIL L
	115	09	APR3	M8539	APR EBUS RETURN H
	115	10	APR3	M8539	APR EBOX DISABLE CS H
	115	11	APR2	M8539	APR WR BAD ADR PAR L
	115	12	APR6	M8539	APR EBOX CCA H
	115	13	APR6	M8539	APR EBOX ERA H
	115	14	APR6	M8539	APR EBOX SBUS DIAG H
	115	15	APR6	M8539	MCL MEM/REG FUNC L
	115	16	APR6	M8539	APR EBOX LOAD REG L
	115	17	APR6	M8539	APR EBOX READ REG L
	115	21	MTR3	M8538	MTR3 INTERVAL ON H
	115	22	MTR3	M8538	MTR3 INTERVAL DONE H
	115	23	MTR3	M8538	MTR3 INTERVAL OVRFLO H
*	115	24-35	MTR3	M8538	MTR PERIOD 06-17 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	116	07	APR5	M8539	APR WR PT SEL 0 H
	116	08	APR5	M8539	APR PT DIR WR L
	116	09	APR3	M8539	APR EBUS REQ L
	116	10	APR3	M8539	APR EBUS F01 E H
	116	11	APR2	M8539	APR ANY EBOX ERR FLG H
	116	12	APR6	M8539	APR EBOX UBR H
	116	13	APR6	M8539	APR EN REFILL RAM WR H
	116	21	MTR2	M8538	MTR2 PI ACCT EN H
	116	22	MTR2	M8538	MTR2 EXEC ACCT EN H
	116	23	MTR2	M8538	MTR2 ACCT ON H
	116	25	MTR2	M8538	MTR2 TIME ON H
**	116	33	PIC3	M8538	PI3 MTR PIA 04 H
**	116	34	PIC3	M8538	PI3 MTR PIA 02 H
**	116	35	PIC3	M8538	PI3 MTR PIA 01 H
	117	07	APR5	M8539	APR WR PT SEL 1 H
	117	08	APR5	M8539	APR PT WR L
	117	09	APR3	M8539	APR EBUS DEMAND H
	117	10	APR3	M8539	APR EBOX SEND F02 H
	117	11	CON5	M8539	CON FM WRITE PAR L
	117	12	APR6	M8539	APR EBOX EBR H
	117	13	APR6	M8539	APR EBOX SPARE H
	117	20	MTR5	M8538	MTR5 VECTOR REQ H
	117	21	MTR5	M8538	MTR5 INCR SEL 2 H
	117	22	MTR5	M8538	MTR5 INCR SEL 1 H
	117	25	MTR3	M8538	MTR CONO MTR, L
**	120	00	EDP1	M8512	EDP AR 00 H
**	120	01	EDP1	M8512	EDP AR 01 H
**	120	02	EDP1	M8512	EDP AR 02 H
**	120	03	EDP1	M8512	EDP AR 03 H
**	120	04	EDP1	M8512	EDP AR 04 H
**	120	05	EDP1	M8512	EDP AR 05 H
**	120	06	EDP1	M8512	EDP AR 06 H
**	120	07	EDP1	M8512	EDP AR 07 H
**	120	08	EDP1	M8512	EDP AR 08 H
**	120	09	EDP1	M8512	EDP AR 09 H
**	120	10	EDP1	M8512	EDP AR 10 H
**	120	11	EDP1	M8512	EDP AR 11 H
*	120	12-35	EDP1	M8512	AR 12 TO 35 H
*	121	0-35	EDP4	M8512	BR 0 TO 35 H
*	122	0-35	EDP2	M8512	MQ 0 TO 35 H
*	123	0-35	EDP4	M8512	FM 0 TO 35 H
*	124	0-35	EDP4	M8512	BRX 0 TO 35 H
*	125	0-35	EDP2	M8512	ARX 0 TO 35 H
*	126	0-35	EDP3	M8512	ADX 0 TO 35 H
*	127	0-35	EDP3	M8512	AD 0 TO 35 H
	130	02	SCD4	M8524	SCD TRAP REQ 2 H
	130	03	SCD4	M8524	SCD TRAP CYC 2 H
	130	04	SCD4	M8524	SCD TRAP CYC 1 H
	130	05	SCD4	M8524	SCD TRAP REQ 1 H
	130	06	SCD4	M8524	SCD FPD H
**	130	07	SCD2	M8524	SC 05 H
**	130	08	SCD2	M8524	SC 06 H
**	130	09	SCD2	M8524	SC 07 H
**	130	10	SCD2	M8524	SC 08 H
**	130	11	SCD2	M8524	SC 09 H
	130	12	IRD3	M8522	IR NORM 08 H
	130	13	IRD3	M8522	IR NORM 09 H
	130	14	IRD3	M8522	IR NORM 10 H
**	130	15	IRD1	M8522	DR ADR 00 A H
**	130	16	IRD1	M8522	DR ADR 01 A H
**	130	17	IRD1	M8522	DR ADR 02 A H
	130	18	CON3	M8525	CON WR EVEN PAR ADR H
	130	19	CON3	M8525	CON3 WR EVEN PAR DATA H
	130	20	CON3	M8525	CON3 WR EVEN PAR DIR H
	131	02	SCD4	M8524	SCD OV H
	131	03	SCD4	M8524	SCD CRY0 H
	131	04	SCD4	M8524	SCD CRY1 H
	131	05	EDP3	M8524	AD CRY 01 L
	131	06	SCD4	M8524	SCD DIV CHK H
**	131	07	SCD2	M8524	SC 00 H
**	131	08	SCD2	M8524	SC 01 H
**	131	09	SCD2	M8524	SC 02 H
**	131	10	SCD2	M8524	SC 03 H
**	131	11	SCD2	M8524	SC 04 H
**	131	12	IRD1	M8522	DR ADR 03 A H
**	131	13	IRD1	M8522	DR ADR 04 A H
**	131	14	IRD1	M8522	DR ADR 05 A H
**	131	15	IRD1	M8522	DR ADR 06 A H
**	131	16	IRD1	M8522	DR ADR 07 A H
**	131	17	IRD1	M8522	DR ADR 08 A H
	131	18	CON3	M8525	CON3 CACHE LOOK EN H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	131	19	CON3	M8525	CON CACHE LOAD EN H
	131	21	CON3	M8525	CON KI10 PAGING MODE L
	131	22	CON3	M8525	CON TRAP EN H
	132	02	SCD4	M8524	VMA HELD OR PC 00 H
	132	03	SCD4	M8524	SCD FOV H
	132	04	SCD4	M8524	SCD FXU H
	132	05	EDP3	M8524	AD OVERFLOW 00 L
	132	06	IRD4	M8524	AD CRY -02 A L
**	132	07	SCD2	M8524	FE 05 H
**	132	08	SCD2	M8524	FE 06 H
**	132	09	SCD2	M8524	FE 07 H
**	132	10	SCD2	M8524	FE 08 H
**	132	11	SCD2	M8524	FE 09 H
	132	12	IRD3	M8522	IR EN I/O, JRST H
	132	13	IRD3	M8522	IR EN AC H
**	132	14	IRD1	M8522	IR AC 09 H
**	132	15	IRD1	M8522	IR AC 10 H
**	132	16	IRD1	M8522	IR AC 11 H
**	132	17	IRD1	M8522	IR AC 12 H
	132	18	CON1	M8525	CON COND EN 00-07 L
	132	19	CON1	M8525	CON COND/SEL VMA L
	132	20	CON1	M8525	CON COND/MBOX CTL L
	132	22	CON2	M8525	CON LOAD IR L
	132	23	CON4	M8525	CON4 AR LOADED H
	132	24	CON5	M8525	CON5 PI CYCLE H
	133	02	SCD4	M8524	SCD PCP H
	133	03	SCD5	M8524	SCD LOAD FLAGS A H
	133	04	SCD1	M8524	SCAD=0 L
	133	05	CON2	M8524	CON CLR PRIVATE INSTR H
	133	06	SCD4	M8524	SCD NICOND 10 H
**	133	07	SCD2	M8524	FE 00 H
**	133	08	SCD2	M8524	FE 01 H
**	133	09	SCD2	M8524	FE 02 H
**	133	10	SCD2	M8524	FE 03 H
**	133	11	SCD2	M8524	FE 04 H
**	133	12	IRD1	M8522	DRAM A 00 H
**	133	13	IRD1	M8522	DRAM A 01 H
**	133	14	IRD1	M8522	DRAM A 02 H
**	133	15	IRD1	M8522	DRAM B 00 H
**	133	16	IRD1	M8522	DRAM B 01 H
**	133	17	IRD1	M8522	DRAM B 02 H
	133	18	CON1	M8525	CON SKIP EN 40-47 L
	133	19	CON1	M8525	CON COND/VMA GETS # H
	133	20	CON3	M8525	CON EBUS REL H
	133	21	CON4	M8525	CON PC+1 INH L
	133	22	CON2	M8525	CON COND INSTR ABORT H
	133	23	CON4	M8525	CON ARX LOADED L
	133	24	CON5	M8525	CON5 MEM CYCLE L
	134	02	SCD5	M8524	SCD USER A L
	134	03	SCD5	M8524	SCD LEAVE USER H
	134	04	CON5	M8524	CON PI CYCLE A L
	134	05	SCD5	M8524	SCD USER EN L
	134	06	SCD5	M8524	SCD PUBLIC PAGE H
	134	07	SCD2	M8524	SC SIGN H
	134	12	IRD3	M8522	TEST SATISFIED H
	134	13	IRD3	M8522	IR JRST 0, L
**	134	14	IRD1	M8522	DRAM J 01 H
**	134	15	IRD1	M8522	DRAM J 02 H
**	134	16	IRD1	M8522	DRAM J 03 H
**	134	17	IRD1	M8522	DRAM J 04 H
	134	18	CON1	M8525	CON SKIP EN 50-57 L
	134	19	CON1	M8525	CON COND/LOAD VMA HELD H
	134	20	CON3	M8525	CON SR 00 H
	134	21	CON2	M8525	CON NICOND TRAP EN H
	134	22	CON2	M8525	CON LOAD ACCESS COND H
	134	23	CON4	M8525	CON UCODE STATE 01 H
	134	24	CON5	M8525	CON FM WRITE PAR L
	135	02	SCD5	M8524	SCD PUBLIC EN L
	135	03	SCD5	M8524	SCD PUBLIC A H
	135	04	SCD5	M8524	SCD KERNEL MODE H
	135	05	SCD5	M8524	SCD PRIVATE INSTR L
	135	06	SCD5	M8524	SCD PRIVATE INSTR EN L
	135	07	SCD2	M8524	FE SIGN H
**	135	12	IRD1	M8522	DRAM PAR H
	135	13	IRD3	M8522	DRAM ODD PARITY H
**	135	14	IRD1	M8522	DRAM J 07 H
**	135	15	IRD1	M8522	DRAM J 08 H
**	135	16	IRD1	M8522	DRAM J 09 H
**	135	17	IRD1	M8522	DRAM J 10 H
	135	18	CON3	M8525	CON DELAY REQ H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	135	19	CON1	M8525	CON LOAD SPEC INSTR L
	135	20	CON3	M8525	CON SR 01 H
	135	21	CON2	M8525	CON NICOND 07 H
	135	22	CON2	M8525	CON2 INSTR GO L
	135	23	CON4	M8525	CON UCODE STATE 03 H
	135	24	CON5	M8525	CON MBOX WAIT L
	136	02	SCD5	M8524	SCD KERNEL OR USER IOT H
**	136	03	SCD3	M8524	SCD TRAP MIX 32 H
**	136	04	SCD3	M8524	SCD TRAP MIX 33 H
	136	05	SCD5	M8524	SCD USER IOT A H
	136	06	SCD5	M8524	SCD USER IOT EN L
	136	07	SCD2	M8524	SC .GE. 36 H
	136	12	IRD3	M8522	AD=0 L
	136	13	IRD1	M8522	IR I/O LEGAL H
	136	14	CTL1	M8522	CTL INH CRY 18 L
	136	15	CTL1	M8522	CTL SPEC/GEN CRY 18 H
	136	16	IRD4	M8522	GEN CRY 36 H
	136	17	IRD4	M8522	AD CRY -02 A H
	136	18	CON4	M8525	CON AR 36 H
	136	19	CON1	M8525	CON VMA SEL 2 L
	136	20	CON3	M8525	CON SR 02 H
	136	21	CON2	M8525	CON NICOND 08 H
	136	22	CON2	M8525	CON LOAD DRAM H
	136	23	CON4	M8525	CON UCODE STATE 05 H
	136	24	CON5	M8525	CON FM XFER L
	137	02	SCD5	M8524	SCD ADR BRK INH H
**	137	03	SCD3	M8524	SCD TRAP MIX 34 H
**	137	04	SCD3	M8524	SCD TRAP MIX 35 H
	137	05	SCD5	M8524	SCD ADR BRK CYC H
	137	06	SCD5	M8524	SCD ADR BREAK PREVENT H
	137	07	SCD4	M8524	SCD TRAP CLEAR L
	137	12	IRD4	M8522	AD CRY 12 H
	137	13	IRD4	M8522	AD CRY 18 H
	137	14	IRD4	M8522	AD CRY 24 H
	137	15	IRD4	M8522	AD CRY 36 H
	137	16	IRD4	M8522	ADX CRY 12 H
	137	17	IRD4	M8522	ADX CRY 24 H
	137	18	CON4	M8525	CON ARX 36 H
	137	19	CON1	M8525	CON VMA SEL 1 L
	137	20	CON3	M8525	CON SR 03 H
	137	21	CON2	M8525	CON NICOND 09 H
	137	22	CON2	M8525	CON COND ADR 10 H
	137	23	CON4	M8525	CON UCODE STATE 07 H
	137	24	CON5	M8525	CON PI DISMISS L
	140	00	CRA3	M8511	DISP EN 00-07 L
	140	01	CRA3	M8511	DISP EN 00-03 L
	140	02	CRA3	M8511	DISP EN 30-37 L
	140	03	CRA3	M8511	DISP 02 A H
	140	04	CRA3	M8511	DISP 03 A H
	140	05	CRA3	M8511	DISP 04 A H
**	141	00	CRA3	M8511	CRA DISP PARITY H
**	141	01	CRA3	M8511	CRA DISP 00 H
**	141	02	CRA3	M8511	CRA DISP 01 H
**	141	03	CRA3	M8511	CRA DISP 02 H
**	141	04	CRA3	M8511	CRA DISP 03 H
**	141	05	CRA3	M8511	CRA DISP 04 H
**	142	00	CRA4	M8511	SBR RET 05 H
**	142	01	CRA4	M8511	SBR RET 06 H
**	142	02	CRA4	M8511	SBR RET 07 H
**	142	03	CRA4	M8511	SBR RET 08 H
**	142	04	CRA4	M8511	SBR RET 09 H
**	142	05	CRA4	M8511	SBR RET 10 H
**	143	01	CRA4	M8511	SBR RET 00 H
**	143	02	CRA4	M8511	SBR RET 01 H
**	143	03	CRA4	M8511	SBR RET 02 H
**	143	04	CRA4	M8511	SBR RET 03 H
**	143	05	CRA4	M8511	SBR RET 04 H
**	144	00	CRA2	M8511	CR ADR 05 F H
**	144	01	CRA2	M8511	CR ADR 06 F H
**	144	02	CRA2	M8511	CR ADR 07 F H
**	144	03	CRA2	M8511	CR ADR 08 F H
**	144	04	CRA2	M8511	CR ADR 09 F H
**	144	05	CRA2	M8511	CR ADR 10 F H
**	144	08	CRM5	M8528	CRAM 60 H
**	144	09	CRM5	M8528	CRAM PAR 1ST 00 H
**	144	10	CRM5	M8528	CRAM 62 H
**	144	11	CRM5	M8528	CRAM PAR 00 H
**	144	14	CRM5	M8528	CRAM 64 H
**	144	15	CRM5	M8528	CRAM PAR 1ST 04 H
**	144	16	CRM5	M8528	CRAM 66 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	144	17	CRM5	M8528	CRAM PAR 04 H
**	144	20	CRM5	M8528	CRAM 68 H
**	144	21	CRM5	M8528	CRAM PAR 1ST 08 H
**	144	22	CRM5	M8528	CRAM 70 H
**	144	23	CRM5	M8528	CRAM PAR 08 H
**	144	26	CRM5	M8528	CRAM 72 H
**	144	27	CRM5	M8528	CRAM PAR 1ST 12 H
**	144	28	CRM5	M8528	CRAM 74 H
**	144	29	CRM5	M8528	CRAM PAR 12 H
**	144	32	CRM5	M8528	CRAM 76 H
**	144	33	CRM5	M8528	CRAM PAR 1ST 16 H
**	144	34	CRM5	M8528	CRAM 78 H
**	144	35	CRM5	M8528	CRAM PAR 16 H
**	145	01	CRA1	M8511	CR ADR 00 F H
**	145	02	CRA1	M8511	CR ADR 01 F H
**	145	03	CRA1	M8511	CR ADR 02 F H
**	145	04	CRA1	M8511	CR ADR 03 F H
**	145	05	CRA1	M8511	CR ADR 04 F H
*	145	08-11	CRM5	M8528	CRAM 40-43 H
*	145	14-17	CRM5	M8528	CRAM 44-47 H
*	145	20-23	CRM5	M8528	CRAM 48-51 H
*	145	26-29	CRM5	M8528	CRAM 52-55 H
*	145	32-35	CRM5	M8528	CRAM 56-59 H
**	146	00	CRA3	M8511	CRA LOC 05 H
**	146	01	CRA3	M8511	CRA LOC 06 H
**	146	02	CRA3	M8511	CRA LOC 07 H
**	146	03	CRA3	M8511	CRA LOC 08 H
**	146	04	CRA3	M8511	CRA LOC 09 H
**	146	05	CRA3	M8511	CRA LOC 10 H
*	146	08-11	CRM5	M8528	CRAM 20-23 H
*	146	14-17	CRM5	M8528	CRAM 24-27 H
*	146	20-23	CRM5	M8528	CRAM 28-31 H
*	146	26-29	CRM5	M8528	CRAM 32-35 H
*	146	32-35	CRM5	M8528	CRAM 36-39 H
**	147	01	CRA3	M8511	CRA LOC 00 H
**	147	02	CRA3	M8511	CRA LOC 01 H
**	147	03	CRA3	M8511	CRA LOC 02 H
**	147	04	CRA3	M8511	CRA LOC 03 H
**	147	05	CRA3	M8511	CRA LOC 04 H
*	147	08-11	CRM5	M8528	CRAM 00-03 H
*	147	14-17	CRM5	M8528	CRAM 04-07 H
*	147	20-23	CRM5	M8528	CRAM 08-11 H
*	147	26-29	CRM5	M8528	CRAM 12-15 H
*	147	32-35	CRM5	M8528	CRAM 16-19 H

NOTE ABOUT READING VMA BOARD REGISTERS
THESE FORMULAS TERSELY DESCRIBE THE DIAGNOSTIC FUNCTION (150-157) AND EBUS BIT NUMBER (13-35, ODD) CORRESPONDING TO A REGISTER BIT 'B'.
[] MEANS "THE INTEGER PART OF THE QUOTIENT"
REM() MEANS "THE REMAINDER OF"

	FORMULA FOR:	
REGISTER	DIAG FUNC	EBUS BIT
ADR BRK	153-REM(B/4)	4*[B/4]+3
PC	DITTO	4*[B/4]+1
VMA	157-REM(B/4)	4*[B/4]+3
VMA HELD	DITTO	4*[B/4]+1

BETTER YET--SEE THE PRINTS!

	153	13	VMA1	M8523	VMA 18-31=0 H
	157	13	VMA1	M8523	VMA AC REF H
	157	15	VMA3	M8523	VMA MATCH 13-35 H
*	15X	13-35	VMA3	M8523	ADR BRK 13-35 H **NOTE
*	15X	13-35	VMA4	M8523	VMA HELD 13-35 H **NOTE
*	15X	13-35	VMA2	M8523	VMA 13-35 H **NOTE
*	15X	13-35	VMA3	M8523	PC 13-35 H **NOTE
	160	15	MBZ1	M8537	CORE BUSY H
	160	16	MBZ4	M8537	CHAN PAR ERR L
	160	17	SHD1	M8537	SH AR PAR ODD A H
	160	18	MBZ5	M8537	MB PAR BIT IN H
	160	19	MBZ1	M8537	CSH EN CSH DATA L
	160	20	MBZ1	M8537	MB IN SEL 1 H
	160	21	MBZ3	M8537	NXM ACKN H
	160	22	MBZ1	M8537	MBZ1 CHAN CORE BUSY H
	160	23	MBZ3	M8537	NXM ANY L
	160	24	MBZ4	M8537	MBZ4 NXM T6,7 L
	160	25	MBZ3	M8537	CHAN NXM ERR L
	160	26	PAG5	M8537	PAG MB 18-35 PAR H
	160	27	MBC5	M8531	FORCE VALID MATCH 0 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	160	28	MBC5	M8531	FORCE VALID MATCH 1 H
	160	29	MBC5	M8531	FORCE VALID MATCH 2 H
	160	30	MBC5	M8531	FORCE VALID MATCH 3 H
	160	31	MBC1	M8531	WRITE OK H
	160	32	MBC2	M8531	MBC2 CSH ADR WR PULSE H
	160	33	MBC2	M8531	CSH DATA CLR DONE IN L
	161	15	MBZ4	M8537	MBOX ADR PAR ERR L
	161	16	MBZ5	M8537	CBUS PAR LEFT TE H
	161	17	MEM5	M8537	MEM PAR IN H
	161	18	MBZ6	M8537	MBZ6 CSH PAR BIT H
	161	19	MBZ1	M8537	MEM TO C DIAG EN L
	161	20	MBZ1	M8537	MB IN SEL 2 H
	161	21	MBZ1	M8537	MBZ1 RD-PSE-WR REF L
	161	22	MBZ3	M8537	MBOX NXM ERR L
	161	23	MBZ3	M8537	MBZ3 CHAN MEM REF L
	161	24	MBZ4	M8537	MBOX SBUS ERR L
	161	25	MBZ3	M8537	NXM DATA VAL L
	161	26	MBZ6	M8537	CSH PAR BIT A H
	161	27	MBC2	M8531	CSH DATA CLR T1 L
	161	28	MBC2	M8531	CSH DATA CLR T2 L
	161	29	MBC2	M8531	CSH DATA CLR T3 L
	161	30	MBC2	M8531	CSH SEL LRU H
	161	31	MBC2	M8531	MBC2 CSH VAL WR PULSE H
	161	32	MBC2	M8531	MBC2 CSH WR WR PULSE H
	161	33	MBC2	M8531	RQ HOLD FF H
	162	15	MBZ4	M8537	CHAN ADR PAR ERR L
	162	16	MBZ5	M8537	CBUS PAR RIGHT TE H
	162	17	MBZ5	M8537	CSH PAR BIT IN H
	162	18	MBZ3	M8537	MBZ3 SEQUENTIAL RQ H
	162	19	MBZ1	M8537	CHAN READ L
	162	20	MBZ1	M8537	MB IN SEL 4 H
	162	21	MBZ1	M8537	MEM BUSY H
	162	22	MBZ3	M8537	MBZ3 HOLD ERA L
	162	23	MBZ4	M8537	MBZ4 NXM T2 H
	162	24	MBZ4	M8537	MBOX MB PAR ERR L
	162	25	PAG5	M8537	PAG MB 00-17 PAR H
	162	26	MBZ6	M8537	CSH PAR BIT B H
	162	27	MBC2	M8531	MBC2 CACHE WR 00 A H
	162	28	MBC2	M8531	MBC2 CACHE WR 09 A H
	162	29	MBC2	M8531	MBC2 CACHE WR 18 A H
	162	30	MBC2	M8531	MBC2 CACHE WR 27 A H
	162	31	MBC2	M8531	SBUS ADR HOLD H
	162	32	MBC3	M8531	A CHANGE COMING A L
	162	33	MBC3	M8531	MBC3 ANY SBUS RQ IN L
	163	27	MBC3	M8531	MBC3 B CHANGE COMING L
	163	28	MBC5	M8531	CORE BUSY B H
	163	29	MBC3	M8531	CSH VAL SEL ALL H
	163	30	MBC3	M8531	CSH VAL WR DATA H
	163	31	MBC3	M8531	CSH WR SEL ALL H
	163	32	MBC3	M8531	CSH WR WR DATA H
	163	33	MBC3	M8531	DATA VALID A OUT H
	164	27	MBC3	M8531	DATA VALID B OUT H
	164	28	MBC3	M8531	MBC INH 1ST MB REQ H
	164	29	MBC3	M8531	MEM TO C EN L
	164	30	MBC3	M8531	PHASE CHANGE COMING L
	164	31	MBC4	M8531	ACKN PULSE L
	164	32	MBC4	M8531	CORE ADR 34 H
	164	33	MBC4	M8531	CORE ADR 35 H
	165	27	MBC1	M8531	CAM SEL 1 H
	165	28	MBC1	M8531	CAM SEL 2 H
	165	29	MBC4	M8531	CORE DATA VALID -1 L
	165	30	MBC4	M8531	MBC4 CORE DATA VALID -2 L
	165	31	MBC4	M8531	CORE DATA VALID L
	165	32	MBC4	M8531	MBC4 CORE RD IN PROG H
	165	33	MBC4	M8531	MEM ADR PAR H
	166	27	MBC4	M8531	MEM RD RQ B H
	166	28	MBC4	M8531	MEM RQ 0 H
	166	29	MBC4	M8531	MEM RQ 1 H
	166	30	MBC4	M8531	MEM RQ 2 H
	166	31	MBC4	M8531	MEM RQ 3 H
	166	32	MBC4	M8531	MEM START L
	166	33	MBC4	M8531	MEM WR RQ L
*	167	00-08	MBZ2	M8537	EBUS REG 00-08 H
*	167	14-26	MBZ2	M8537	EBUS REG 14-26 H
*	167	27-33	MBC1	M8531	EBUS REG 27-33 H
*	167	34,35	MBZ2	M8537	EBUS REG 34,35 H
**	170	00	CRC6	M8535	CRC CH BUF ADR 0 H
	170	01	CRC4	M8535	CRC4 RESET IN L
	170	02	CRC4	M8535	CRC MEM STORE ENA L
	170	03	CRC4	M8535	CRC4 DONE IN H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	170	04	CRC4	M8535	CRC4 STORE IN H
	170	05	CCW4	M8534	CCW WD READY H
	170	06	CCW6	M8534	CCW CCWF REQ ENA H
	170	07	CCW6	M8534	CCW MEM STORE ENA H
	170	08	CCW5	M8534	CCW ACT FLAG REQ ENA H
	170	09	CCW3	M8534	CCW ALU C8 OUT H
	170	10	CCW3	M8534	CCW ALU C2 OUT H
	170	11	CHC1	M8533	CH T0 H
	170	12	CHC5	M8533	CBUS SEL 0 E H
	170	13	CHC1	M8533	CHX RESET H
	170	14	CHC2	M8533	CH RESET INTR H
	170	16	CCL5	M8536	CCL ODD WC PAR H
	170	18	CCL5	M8536	CCL5 WC GE4 H
	170	19	CCL5	M8536	CCL WC=0 L
	170	20	CHX2	M8515	CSH 0 ANY VAL L
	170	21	CHX3	M8515	CSH USE IN 0 H
	170	22	CSH5	M8513	CSH5 PAGE REFILL COMP L
	170	23	CSH6	M8513	CACHE WR IN H
	170	24	CSH6	M8513	MBOX PT DIR WR L
	170	25	CSH2	M8513	CSH2 WR TEST L
	170	26	CSH3	M8513	ANY VAL HOLD H
	170	27	CSH4	M8513	CSH DATA CLR DONE L
	170	28	CSH4	M8513	CSH REFILL RAM WR L
	170	29	CSH4	M8513	CSH EBOX T3 L
	170	30	MBX1	M8529	CACHE BIT H
	170	31	MBX1	M8529	CCA REQ L
	170	32	MBX4	M8529	CSH WR WD 2 EN H
	170	33	MBX5	M8529	MB REQ IN H
	170	34	MBX5	M8529	MBX MEM TO C EN L
	170	35	MBX5	M8529	RQ 1 IN H
**	171	00	CRC6	M8535	CRC CH BUF ADR 1 H
	171	01	CRC4	M8535	CRC RH20 ERR IN H
	171	02	CRC4	M8535	CRC OVN ERR IN H
	171	03	CRC4	M8535	CRC SHORT WC ERR H
	171	04	CRC4	M8535	CRC LONG WC ERR H
	171	05	CCW4	M8534	CCW WD0 REQ H
	171	06	CCW4	M8534	CCW WD1 REQ H
	171	07	CCW4	M8534	CCW WD2 REQ H
	171	08	CCW4	M8534	CCW WD3 REQ H
	171	09	CCW1	M8534	CCW MEM ADR=0 H
	171	10	CCW6	M8534	CCW CCWF WAITING H
	171	11	CHC1	M8533	CH T1 H
	171	12	CHC5	M8533	CBUS SEL 1 E H
	171	13	CHC1	M8533	CHX START H
	171	14	CHC2	M8533	CH START INTR H
	171	16	CCL3	M8536	CCL3 MB RIP A H
	171	18	CCL3	M8536	CCL ALU MINUS L
	171	19	CCL4	M8536	CCL CH TEST MB PAR L
	171	20	CHX2	M8515	CSH 1 ANY VAL L
	171	21	CHX3	M8515	CSH USE IN 1 H
	171	22	CSH5	M8513	CHAN RD T5 L
	171	23	CSH6	M8513	CSH6 WR DATA RDY L
	171	24	CSH4	M8513	PAGE FAIL T2 L
	171	25	CSH6	M8513	CSH EBOX LOAD REG H
	171	26	CSH7	M8513	CSH FILL CACHE RD L
	171	27	CSH5	M8513	CSH5 CHAN WR T5 L
	171	28	CSH3	M8513	MB WR RQ CLR NXT L
	171	29	CSH4	M8513	CSH4 EBOX T1 L
	171	30	MBX2	M8529	CACHE TO MB 34 H
	171	31	MBX1	M8529	CCA SEL 1 H
	171	32	MBX4	M8529	CSH WR WD 3 EN H
	171	33	MBX2	M8529	MB SEL 1 H
	171	34	MBX3	M8529	MEM DIAG L
	171	35	MBX5	M8529	RQ 2 IN H
**	172	00	CRC6	M8535	CRC CH BUF ADR 2 H
	172	01	CRC3	M8535	CRC READY IN H
	172	02	CRC3	M8535	CRC LAST WORD IN H
	172	03	CRC3	M8535	CRC ERR IN H
	172	04	CRC3	M8535	CRC REVERSE IN H
	172	05	CCW3	M8534	CCW ACT CTR 0 EN H
	172	06	CCW3	M8534	CCW ACT CTR 1 EN H
	172	07	CCW3	M8534	CCW ACT CTR 2 EN H
	172	08	CCW1	M8534	CCW BUF ADR 0 L
	172	09	CCW1	M8534	CCW BUF ADR 1 L
	172	10	CCW1	M8534	CCW BUF ADR 2 L
	172	11	CHC1	M8533	CH T2 H
	172	12	CHC5	M8533	CBUS SEL 2 E H
	172	13	CHC1	M8533	CHX DONE H
	172	14	CHC2	M8533	CH DONE INTR H
	172	16	CCL3	M8536	CCL3 CCWF T2 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	172	18	CCL3	M8536	CCL3 MB REQ T2 H
	172	19	CCL4	M8536	CCL4 REVERSE H
	172	20	CHX2	M8515	CSH 2 ANY VAL L
	172	21	CHX3	M8515	CSH USE IN 2 H
	172	22	CSH6	M8513	CHAN WR CACHE L
	172	23	CSH6	M8513	CCA CYC DONE L
	172	24	CSH5	M8513	CHAN T4 L
	172	25	CHX3	M8513	CSH LRU 2 H
	172	26	CSH1	M8513	CSH1 READY TO GO A H
	172	27	CSH6	M8513	CSH USE HOLD H
	172	28	CSH1	M8513	CSH CCA CYC L
	172	29	CSH2	M8513	CSH2 EBOX REQ EN L
	172	30	MBX2	M8529	CACHE TO MB 35 H
	172	31	MBX1	M8529	CCA SEL 2 H
	172	32	MBX1	M8529	FORCE NO MATCH H
	172	33	MBX2	M8529	MB SEL 2 H
	172	34	MBX5	M8529	MEM RD RQ IN H
	172	35	MBX5	M8529	RQ 3 IN H
**	173	00	CRC6	M8535	CRC CH BUF ADR 3 H
	173	01	CRC2	M8535	CRC2 ACT CTR 0R H
	173	02	CRC2	M8535	CRC2 ACT CTR 1R H
	173	03	CRC2	M8535	CRC2 ACT CTR 2R H
	173	04	CRC2	M8535	CRC2 RAM CYC H
**	173	05	CCW2	M8534	CCW CHA 30 H
**	173	06	CCW2	M8534	CCW CHA 31 H
**	173	07	CCW2	M8534	CCW CHA 32 H
**	173	08	CCW2	M8534	CCW CHA 33 H
**	173	09	CCW2	M8534	CCW CHA 34 H
**	173	10	CCW2	M8534	CCW CHA 35 H
	173	11	CHC1	M8533	CH T3 H
	173	12	CHC5	M8533	CBUS SEL 3 E H
	173	13	CHC1	M8533	CHX STORE H
	173	14	CHC2	M8533	CH STORE H
	173	16	CCL4	M8536	CCL CH MB SEL 2 H
	173	18	CCL4	M8536	CCL CH MB SEL 1 H
	173	19	CCL3	M8536	CCL AF T2 L
	173	20	CHX2	M8515	CSH 3 ANY VAL L
	173	21	CHX3	M8515	CSH USE IN 3 H
	173	22	CSH2	M8513	CSH2 ONE WORD RD A L
	173	23	CSH2	M8513	CSH2 MBOX RESP L
	173	24	CSH2	M8513	CSH2 RD PSE 2ND REQ EN L
	173	25	CHX3	M8513	CSH LRU 1 H
	173	26	CSH5	M8513	CSH5 T1 L
	173	27	CSH4	M8513	CSH4 WRITEBACK T1 A H
	173	28	CSH7	M8513	CSH CCA WRITEBACK L
	173	29	CSH4	M8513	CSH4 EBOX T2 L
	173	30	MBX4	M8529	MBX4 CACHE TO MB DONE H
	173	31	MBX2	M8529	CHAN WR CYC L
	173	32	MBX3	M8529	MEM DATA TO MEM H
	173	33	MBX2	M8529	MB SEL HOLD H
	173	34	MBX3	M8529	MEM TO C SEL 1 H
	173	35	MBX2	M8529	SBUS ADR 34 H
**	174	00	CRC6	M8535	CRC CH BUF ADR 4 H
	174	01	CRC1	M8535	CRC1 ACT FLAG ENA H
	174	02	CRC5	M8535	CRC WR RAM L
	174	03	CRC3	M8535	CRC3 OP CODE 00 H
	174	04	CRC3	M8535	CRC3 OP CODE 01 H
*	174	05-10	CCW2	M8534	CCW CHA 24-29 H
	174	11	CHC1	M8533	CBUS READY E H
	174	12	CHC5	M8533	CBUS SEL 4 E H
	174	13	CHC1	M8533	CHX CTOM H
	174	14	CHC3	M8533	CH CTOM H
	174	16	CCL3	M8536	CCL CHAN REQ H
	174	18	CCL3	M8536	CCL CHAN EPT H
	174	19	CCL4	M8536	CCL CHAN TO MEM H
	174	20	CHX4	M8515	CSH DIR 0 PAR ODD H
	174	21	CHX3	M8515	CSH USE IN 4 H
	174	22	CSH2	M8513	CSH2 E CORE RD RQ A L
	174	23	CSH6	M8513	PAGE FAIL HOLD L
	174	24	CSH5	M8513	CSH5 PAGE REFILL T9,12 L
	174	25	CHA3	M8513	CSH 3 ANY WR L
	174	26	CSH5	M8513	CSH T0 L
	174	27	CSH3	M8513	CSH ADR PMA EN H
	174	28	CSH1	M8513	CSH1 EBOX CYC B L
	174	29	CSH1	M8513	CSH1 CACHE IDLE L
	174	30	MBX4	M8529	CACHE TO MB T2 L
	174	31	MBX1	M8529	CSH CCA INVAL CSH H
	174	32	MBX3	M8529	MB DATA CODE 1 H
	174	33	MBX6	M8529	MB0 HOLD IN H
	174	34	MBX3	M8529	MEM TO C SEL 2 H
	174	35	MBX2	M8529	SBUS ADR 35 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	175	00	CRC6	M8535	CRC CH BUF ADR 5 H
	175	01	CRC6	M8535	CRC SEL 1D L
	175	02	CRC6	M8535	CRC SEL 2D L
	175	03	CRC6	M8535	CRC SEL 4D L
	175	04	CRC1	M8535	CRC1 AF REQ ENA L
*	175	05-10	CCW2	M8534	CCW CHA 18-23 H
	175	11	CHC1	M8533	CBUS LAST WORD E H
	175	12	CHC5	M8533	CBUS SEL 5 E H
	175	13	CHC5	M8533	CH SEL 8A H
	175	14	CHC2	M8533	CH CONTR REQ H
	175	16	CCL2	M8536	CCL CCWF REQ H
	175	18	CCL2	M8536	CCL2 ACT FLAG REQ H
	175	19	CCL2	M8536	CCL MEM STORE REQ H
	175	20	CHX4	M8515	CSH DIR 1 PAR ODD H
	175	21	CHX3	M8515	CSH USE ADR 2 H
	175	22	CSH2	M8513	CSH EBOX RETRY REQ L
	175	23	CSH6	M8513	CSH USE WR EN H
	175	24	CSH3	M8513	MB TEST PAR A IN L
	175	25	CHA3	M8513	CSH 1 ANY WR L
	175	26	CSH5	M8513	CSH5 T3 L
	175	27	CSH3	M8513	MBOX GATE VMA 27-33 H
	175	28	CSH1	M8513	CSH MB CYC L
	175	29	CSH4	M8513	ONE WORD WR T0 L
	175	30	MBX4	M8529	MBX4 CACHE TO MB T3 L
	175	31	MBX1	M8529	CSH CCA VAL CORE H
	175	32	MBX3	M8529	MB DATA CODE 2 H
	175	33	MBX6	M8529	MB1 HOLD IN H
	175	34	MBX5	M8529	MEM WR RQ IN H
	175	35	MBX3	M8529	SBUS DIAG 3 L
**	176	00	CRC6	M8535	CRC CH BUF ADR 6 H
	176	01	CRC1	M8535	CRC1 MEM PTR0 H
	176	02	CRC1	M8535	CRC1 MEM PTR1 H
	176	03	CRC1	M8535	CRC1 MEM PTR2 H
	176	04	CRC1	M8535	CRC1 MEM PTR3 H
	176	05	CCW3	M8534	CCL WC=3 H
	176	06	CCW4	M8534	CCL CCW REG LOAD H
*	176	07-10	CCW2	M8534	CCW CHA 14-17 H
	176	11	CHC1	M8533	CBUS ERROR E H
	176	12	CHC5	M8533	CBUS SEL 6 E H
	176	13	CHC1	M8533	CH MB REQ INH H
	176	14	CHC1	M8533	CH REVERSE H
	176	16	CCL4	M8536	CCL4 STORE CCW H
	176	18	CCL2	M8536	CCL BUF ADR 3 H
	176	19	CCL4	M8536	CCL START MEM L
	176	20	CHX4	M8515	CSH DIR 2 PAR ODD H
	176	21	CHX3	M8515	CSH USE ADR 3 H
	176	22	CSH6	M8513	CCA INVAL T4 L
	176	23	CSH5	M8513	PAGE REFILL T8 L
	176	24	CSH4	M8513	CSH4 EBOX T0 L
	176	25	CHA3	M8513	CSH 2 ANY WR L
	176	26	CSH5	M8513	CSH T2 L
	176	27	CSH2	M8513	E CACHE WR CYC H
	176	28	CSH7	M8513	CSH E WRITEBACK L
	176	29	CSH5	M8513	PAGE REFILL T4 L
	176	30	MBX4	M8529	CACHE TO MB T4 A L
	176	31	MBX4	M8529	CSH WR WD 0 EN H
	176	32	MBX3	M8529	MB PAR H
	176	33	MBX6	M8529	MB2 HOLD IN H
	176	34	MBX3	M8529	REFILL HOLD H
	176	35	MBX3	M8529	MBX3 SBUS DIAG CYC L
	177	00	CRC1	M8535	CRC1 PTR DIF=0 H
	177	01	CRC6	M8535	CRC6 CH ADR 0C L
	177	02	CRC6	M8535	CRC6 CH ADR 1C L
	177	03	CRC6	M8535	CRC6 CH ADR 2C L
	177	04	CRC6	M8535	CRC6 CH ADR 3C L
	177	05	CCW6	M8534	CCW RAM ADR 1 H
	177	06	CCW6	M8534	CCW RAM ADR 2 H
	177	07	CCW6	M8534	CCW RAM ADR 4 H
	177	08	CCW3	M8534	CCL WC=1 H
	177	09	CCW3	M8534	CCL WC=2 H
	177	10	CCW4	M8534	CCW ODD ADR PAR H
	177	11	CHC1	M8533	CH CBUS REQ H
	177	12	CHC5	M8533	CBUS SEL 7 E H
	177	13	CHC2	M8533	CH CONTR CYC H
	177	14	CHC2	M8533	CH START H
	177	16	CCL1	M8536	CCL1 ERR REQ H
	177	18	CCL6	M8536	CCL6 CSH CHAN CYC L
	177	19	CCL3	M8536	CCL3 MEM PTR EN H
	177	20	CHX4	M8515	CSH DIR 3 PAR ODD H
	177	21	CHX3	M8515	CSH USE ADR 4 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

DF	BIT	DRAWING BOARD		NAME AND TRUTH
177	22	CSH6	M8513	PAGE REFILL ERROR L
177	23	CSH6	M8513	CSH6 DATA DLY 1 L
177	24	CSH4	M8513	CSH4 PAGE FAIL DLY H
177	25	CHA3	M8513	CSH 0 ANY WR L
177	26	CSH5	M8513	CSH5 PAGE REFILL T10 L
177	28	CSH2	M8513	RD PAUSE 2ND HALF L
177	29	CSH4	M8513	CSH4 EBOX WR T4 L
177	30	MBX1	M8529	CCA ALL PAGES CYC H
177	31	MBX4	M8529	CSH WR WD 1 EN H
177	32	MBX2	M8529	MB REQ HOLD H
177	33	MBX6	M8529	MB3 HOLD IN H
177	34	MBX5	M8529	RQ 0 IN H
177	35	MBX4	M8529	WRITEBACK T2 L

NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(*) or (**)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (**) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.

KL10(PA) DIAGNOSTIC READ FUNCTION CODES SORTED ALPHABETICALLY

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	162	32	MBC3	M8531	A CHANGE COMING A L
	164	31	MBC4	M8531	ACKN PULSE L
*	127	0-35	EDP3	M8512	AD 0 TO 35 H
	136	17	IRD4	M8522	AD CRY -02 A H
	132	06	IRD4	M8524	AD CRY -02 A L
	131	05	EDP3	M8524	AD CRY 01 L
	137	12	IRD4	M8522	AD CRY 12 H
	137	13	IRD4	M8522	AD CRY 18 H
	137	14	IRD4	M8522	AD CRY 24 H
	137	15	IRD4	M8522	AD CRY 36 H
	132	05	EDP3	M8524	AD OVERFLOW 00 L
	136	12	IRD3	M8522	AD=0 L
*	15X	13-35	VMA3	M8523	ADR BRK 13-35 H **NOTE
*	126	0-35	EDP3	M8512	ADX 0 TO 35 H
	137	16	IRD4	M8522	ADX CRY 12 H
	137	17	IRD4	M8522	ADX CRY 24 H
	170	26	CSH3	M8513	ANY VAL HOLD H
	116	11	APR2	M8539	APR ANY EBOX ERR FLG H
	110	14	APR2	M8539	APR APR INTERRUPT H
	112	10	APR2	M8539	APR C DIR P ERR EN IN H
	110	10	APR2	M8539	APR C DIR P ERR IN H
	111	08	APR5	M8539	APR CURRENT BLOCK 1 H
	111	07	APR5	M8539	APR CURRENT BLOCK 2 H
	111	06	APR5	M8539	APR CURRENT BLOCK 4 H
	111	12	APR3	M8539	APR CWSX H
	115	12	APR6	M8539	APR EBOX CCA H
	115	10	APR3	M8539	APR EBOX DISABLE CS H
	117	12	APR6	M8539	APR EBOX EBR H
	115	13	APR6	M8539	APR EBOX ERA H
	115	16	APR6	M8539	APR EBOX LOAD REG L
	115	17	APR6	M8539	APR EBOX READ REG L
	115	14	APR6	M8539	APR EBOX SBUS DIAG H
	117	10	APR3	M8539	APR EBOX SEND F02 H
	117	13	APR6	M8539	APR EBOX SPARE H
	116	12	APR6	M8539	APR EBOX UBR H
	117	09	APR3	M8539	APR EBUS DEMAND H
	116	10	APR3	M8539	APR EBUS F01 E H
	116	09	APR3	M8539	APR EBUS REQ L
	115	09	APR3	M8539	APR EBUS RETURN H
	116	13	APR6	M8539	APR EN REFILL RAM WR H
	114	15	APR4	M8539	APR F02 EN H
	113	09	APR3	M8539	APR FETCH COMP H
	114	16	APR3	M8539	APR FM 36 H
**	114	14	APR4	M8539	APR FM ADR 1 H
**	114	11	APR4	M8539	APR FM ADR 10 H
**	114	13	APR4	M8539	APR FM ADR 2 H
**	114	12	APR4	M8539	APR FM ADR 4 H
**	114	10	APR5	M8539	APR FM BLOCK 1 H
**	114	09	APR5	M8539	APR FM BLOCK 2 H
**	114	08	APR5	M8539	APR FM BLOCK 4 H
	114	17	APR3	M8539	APR FM ODD PARITY H
	112	08	APR1	M8539	APR I/O PF ERR EN IN H
	110	08	APR1	M8539	APR I/O PF ERR IN H
	112	09	APR1	M8539	APR MB PAR ERR EN IN H
	110	09	APR1	M8539	APR MB PAR ERR IN H
	114	07	APR5	M8539	APR MBOX CTL 03 H
	115	07	APR5	M8539	APR MBOX CTL 06 H
	112	07	APR1	M8539	APR NXM ERR EN IN H
	110	07	APR1	M8539	APR NXM ERR IN H
	111	11	APR5	M8539	APR PREV BLOCK 1 H
	111	10	APR5	M8539	APR PREV BLOCK 2 H
	111	09	APR5	M8539	APR PREV BLOCK 4 H
	111	13	APR3	M8539	APR PREV SEC 13 H
	111	14	APR3	M8539	APR PREV SEC 14 H
	111	15	APR3	M8539	APR PREV SEC 15 H
	111	16	APR3	M8539	APR PREV SEC 16 H
	111	17	APR3	M8539	APR PREV SEC 17 H
	116	08	APR5	M8539	APR PT DIR WR L
	117	08	APR5	M8539	APR PT WR L
	112	12	APR2	M8539	APR PWR FAIL EN IN H
	110	12	APR2	M8539	APR PWR FAIL IN H
	113	10	APR3	M8539	APR READ COMP H
	112	11	APR2	M8539	APR S ADR P ERR EN IN H
	110	11	APR2	M8539	APR S ADR P ERR IN H
	112	06	APR1	M8539	APR SBUS ERR EN IN H
	110	06	APR1	M8539	APR SBUS ERR IN H
	115	08	APR5	M8539	APR SET PAGE FAIL L
	110	01	APR2	M8539	APR SWEEP BUSY EN H
	112	13	APR2	M8539	APR SWEEP DONE EN IN H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	110	13	APR2	M8539	APR SWEEP DONE IN H
	113	12	APR3	M8539	APR USER COMP H
	115	11	APR2	M8539	APR WR BAD ADR PAR L
	116	07	APR5	M8539	APR WR PT SEL 0 H
	117	07	APR5	M8539	APR WR PT SEL 1 H
	113	11	APR3	M8539	APR WRITE COMP H
*	120	12-35	EDP1	M8512	AR 12 TO 35 H
	102	23	MCL5	M8530	ARMM 12 H
*	125	0-35	EDP2	M8512	ARX 0 TO 35 H
*	121	0-35	EDP4	M8512	BR 0 TO 35 H
*	124	0-35	EDP4	M8512	BRX 0 TO 35 H
	170	30	MBX1	M8529	CACHE BIT H
	171	30	MBX2	M8529	CACHE TO MB 34 H
	172	30	MBX2	M8529	CACHE TO MB 35 H
	174	30	MBX4	M8529	CACHE TO MB T2 L
	176	30	MBX4	M8529	CACHE TO MB T4 A L
	170	23	CSH6	M8513	CACHE WR IN H
	165	27	MBC1	M8531	CAM SEL 1 H
	165	28	MBC1	M8531	CAM SEL 2 H
	176	11	CHC1	M8533	CBUS ERROR E H
	175	11	CHC1	M8533	CBUS LAST WORD E H
	161	16	MBZ5	M8537	CBUS PAR LEFT TE H
	162	16	MBZ5	M8537	CBUS PAR RIGHT TE H
	174	11	CHC1	M8533	CBUS READY E H
	170	12	CHC5	M8533	CBUS SEL 0 E H
	171	12	CHC5	M8533	CBUS SEL 1 E H
	172	12	CHC5	M8533	CBUS SEL 2 E H
	173	12	CHC5	M8533	CBUS SEL 3 E H
	174	12	CHC5	M8533	CBUS SEL 4 E H
	175	12	CHC5	M8533	CBUS SEL 5 E H
	176	12	CHC5	M8533	CBUS SEL 6 E H
	177	12	CHC5	M8533	CBUS SEL 7 E H
	177	30	MBX1	M8529	CCA ALL PAGES CYC H
	172	23	CSH6	M8513	CCA CYC DONE L
	176	22	CSH6	M8513	CCA INVAL T4 L
	170	31	MBX1	M8529	CCA REQ L
	171	31	MBX1	M8529	CCA SEL 1 H
	172	31	MBX1	M8529	CCA SEL 2 H
	173	19	CCL3	M8536	CCL AF T2 L
	171	18	CCL3	M8536	CCL ALU MINUS L
	176	18	CCL2	M8536	CCL BUF ADR 3 H
	176	06	CCW4	M8534	CCL CCW REG LOAD H
	175	16	CCL2	M8536	CCL CCWF REQ H
	173	18	CCL4	M8536	CCL CH MB SEL 1 H
	173	16	CCL4	M8536	CCL CH MB SEL 2 H
	171	19	CCL4	M8536	CCL CH TEST MB PAR L
	174	18	CCL3	M8536	CCL CHAN EPT H
	174	16	CCL3	M8536	CCL CHAN REQ H
	174	19	CCL4	M8536	CCL CHAN TO MEM H
	175	19	CCL2	M8536	CCL MEM STORE REQ H
	170	16	CCL5	M8536	CCL ODD WC PAR H
	176	19	CCL4	M8536	CCL START MEM L
	170	19	CCL5	M8536	CCL WC=0 L
	177	08	CCW3	M8534	CCL WC=1 H
	177	09	CCW3	M8534	CCL WC=2 H
	176	05	CCW3	M8534	CCL WC=3 H
	177	16	CCL1	M8536	CCL1 ERR REQ H
	175	18	CCL2	M8536	CCL2 ACT FLAG REQ H
	172	16	CCL3	M8536	CCL3 CCWF T2 H
	172	18	CCL3	M8536	CCL3 MB REQ T2 H
	171	16	CCL3	M8536	CCL3 MB RIP A H
	177	19	CCL3	M8536	CCL3 MEM PTR EN H
	172	19	CCL4	M8536	CCL4 REVERSE H
	176	16	CCL4	M8536	CCL4 STORE CCW H
	170	18	CCL5	M8536	CCL5 WC GE4 H
	177	18	CCL6	M8536	CCL6 CSH CHAN CYC L
	172	05	CCW3	M8534	CCW ACT CTR 0 EN H
	172	06	CCW3	M8534	CCW ACT CTR 1 EN H
	172	07	CCW3	M8534	CCW ACT CTR 2 EN H
	170	08	CCW5	M8534	CCW ACT FLAG REQ ENA H
	170	10	CCW3	M8534	CCW ALU C2 OUT H
	170	09	CCW3	M8534	CCW ALU C8 OUT H
	172	08	CCW1	M8534	CCW BUF ADR 0 L
	172	09	CCW1	M8534	CCW BUF ADR 1 L
	172	10	CCW1	M8534	CCW BUF ADR 2 L
	170	06	CCW6	M8534	CCW CCWF REQ ENA H
	171	10	CCW6	M8534	CCW CCWF WAITING H
*	176	07-10	CCW2	M8534	CCW CHA 14-17 H
*	175	05-10	CCW2	M8534	CCW CHA 18-23 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
*	174	05-10	CCW2	M8534	CCW CHA 24-29 H
**	173	05	CCW2	M8534	CCW CHA 30 H
**	173	06	CCW2	M8534	CCW CHA 31 H
**	173	07	CCW2	M8534	CCW CHA 32 H
**	173	08	CCW2	M8534	CCW CHA 33 H
**	173	09	CCW2	M8534	CCW CHA 34 H
**	173	10	CCW2	M8534	CCW CHA 35 H
	171	09	CCW1	M8534	CCW MEM ADR=0 H
	170	07	CCW6	M8534	CCW MEM STORE ENA H
	177	10	CCW4	M8534	CCW ODD ADR PAR H
	177	05	CCW6	M8534	CCW RAM ADR 1 H
	177	06	CCW6	M8534	CCW RAM ADR 2 H
	177	07	CCW6	M8534	CCW RAM ADR 4 H
	170	05	CCW4	M8534	CCW WD READY H
	171	05	CCW4	M8534	CCW WD0 REQ H
	171	06	CCW4	M8534	CCW WD1 REQ H
	171	07	CCW4	M8534	CCW WD2 REQ H
	171	08	CCW4	M8534	CCW WD3 REQ H
	177	11	CHC1	M8533	CH CBUS REQ H
	177	13	CHC2	M8533	CH CONTR CYC H
	175	14	CHC2	M8533	CH CONTR REQ H
	174	14	CHC3	M8533	CH CTOM H
	172	14	CHC2	M8533	CH DONE INTR H
	176	13	CHC1	M8533	CH MB REQ INH H
	170	14	CHC2	M8533	CH RESET INTR H
	176	14	CHC1	M8533	CH REVERSE H
	175	13	CHC5	M8533	CH SEL 8A H
	177	14	CHC2	M8533	CH START H
	171	14	CHC2	M8533	CH START INTR H
	173	14	CHC2	M8533	CH STORE H
	170	11	CHC1	M8533	CH T0 H
	171	11	CHC1	M8533	CH T1 H
	172	11	CHC1	M8533	CH T2 H
	173	11	CHC1	M8533	CH T3 H
	162	15	MBZ4	M8537	CHAN ADR PAR ERR L
	160	25	MBZ3	M8537	CHAN NXM ERR L
	160	16	MBZ4	M8537	CHAN PAR ERR L
	171	22	CSH5	M8513	CHAN RD T5 L
	162	19	MBZ1	M8537	CHAN READ L
	172	24	CSH5	M8513	CHAN T4 L
	172	22	CSH6	M8513	CHAN WR CACHE L
	173	31	MBX2	M8529	CHAN WR CYC L
	174	13	CHC1	M8533	CHX CTOM H
	172	13	CHC1	M8533	CHX DONE H
	170	13	CHC1	M8533	CHX RESET H
	171	13	CHC1	M8533	CHX START H
	173	13	CHC1	M8533	CHX STORE H
	103	35	CLK4	M8526	CLK 1777 EN H
	106	35	CLK5	M8526	CLK AR/ARX PAR CHECK L
**	101	35	CLK5	M8526	CLK BURST 01 H
**	101	34	CLK5	M8526	CLK BURST 02 H
**	101	33	CLK5	M8526	CLK BURST 04 H
**	101	32	CLK5	M8526	CLK BURST 08 H
**	100	34	CLK5	M8526	CLK BURST 128 H
**	101	31	CLK5	M8526	CLK BURST 16 H
**	101	30	CLK5	M8526	CLK BURST 32 H
**	100	35	CLK5	M8526	CLK BURST 64 H
	100	33	CLK5	M8526	CLK BURST CNT=0 H
	103	31	CLK2	M8526	CLK BURST L
	105	34	CLK5	M8526	CLK CRAM PAR CHECK L
	104	30	CLK3	M8526	CLK CRAM PAR ERR H
	106	34	CLK5	M8526	CLK DRAM PAR CHECK L
	103	30	CLK3	M8526	CLK DRAM PAR ERR H
	103	33	CLK4	M8526	CLK EBOX CLK L
	105	33	CLK5	M8526	CLK EBOX CRM DIS H
	107	33	CLK5	M8526	CLK EBOX CTL DIS H
	106	33	CLK5	M8526	CLK EBOX EDP DIS H
	102	32	CLK4	M8526	CLK EBOX REQ H
	104	33	CLK3	M8526	CLK EBOX SOURCE H
	104	31	CLK2	M8526	CLK EBOX SS L
	100	30	CLK1	M8526	CLK EBUS CLK H
	107	35	CLK5	M8526	CLK ERR STOP EN L
	107	30	CLK3	M8526	CLK ERROR L
	102	30	CLK1	M8526	CLK ERROR STOP H
	104	34	CLK5	M8526	CLK FM PAR CHECK L
	105	30	CLK3	M8526	CLK FM PAR ERR H
	102	35	CLK4	M8526	CLK FORCE 1777 H
	107	34	CLK5	M8526	CLK FS CHECK L
	106	30	CLK3	M8526	CLK FS ERROR H

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SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING BOARD	NAME AND TRUTH
	102	31	CLK2 M8526	CLK GO L
	103	34	CLK4 M8526	CLK INSTR 1777 H
	103	32	CLK4 M8526	CLK MB XFER H
	104	35	CLK5 M8526	CLK MBOX CYCLE DIS H
	105	35	CLK5 M8526	CLK MBOX RESP SIM L
	102	34	CLK4 M8526	CLK PAGE FAIL EN L
	107	31	CLK4 M8526	CLK PAGE FAIL H
	107	32	CLK5 M8526	CLK RATE SEL 1 H
	106	32	CLK5 M8526	CLK RATE SEL 2 H
	100	31	CLK1 M8526	CLK SBUS CLK H
	105	32	CLK5 M8526	CLK SOURCE SEL 1 H
	104	32	CLK5 M8526	CLK SOURCE SEL 2 H
	102	33	CLK3 M8526	CLK SYNC H
	136	18	CON4 M8525	CON AR 36 H
	137	18	CON4 M8525	CON ARX 36 H
	133	23	CON4 M8525	CON ARX LOADED L
	131	19	CON3 M8525	CON CACHE LOAD EN H
	133	05	CON2 M8524	CON CLR PRIVATE INSTR H
	137	22	CON2 M8525	CON COND ADR 10 H
	132	18	CON1 M8525	CON COND EN 00-07 L
	133	22	CON2 M8525	CON COND INSTR ABORT H
	134	19	CON1 M8525	CON COND/LOAD VMA HELD H
	132	20	CON1 M8525	CON COND/MBOX CTL L
	132	19	CON1 M8525	CON COND/SEL VMA L
	133	19	CON1 M8525	CON COND/VMA GETS # H
	135	18	CON3 M8525	CON DELAY REQ H
	133	20	CON3 M8525	CON EBUS REL H
	117	11	CON5 M8539	CON FM WRITE PAR L
	134	24	CON5 M8525	CON FM WRITE PAR L
	136	24	CON5 M8525	CON FM XFER L
	131	21	CON3 M8525	CON KI10 PAGING MODE L
	134	22	CON2 M8525	CON LOAD ACCESS COND H
	136	22	CON2 M8525	CON LOAD DRAM H
	132	22	CON2 M8525	CON LOAD IR L
	135	19	CON1 M8525	CON LOAD SPEC INSTR L
	135	24	CON5 M8525	CON MBOX WAIT L
	135	21	CON2 M8525	CON NICOND 07 H
	136	21	CON2 M8525	CON NICOND 08 H
	137	21	CON2 M8525	CON NICOND 09 H
	134	21	CON2 M8525	CON NICOND TRAP EN H
	133	21	CON4 M8525	CON PC+1 INH L
	134	04	CON5 M8524	CON PI CYCLE A L
	137	24	CON5 M8525	CON PI DISMISS L
	133	18	CON1 M8525	CON SKIP EN 40-47 L
	134	18	CON1 M8525	CON SKIP EN 50-57 L
	134	20	CON3 M8525	CON SR 00 H
	135	20	CON3 M8525	CON SR 01 H
	136	20	CON3 M8525	CON SR 02 H
	137	20	CON3 M8525	CON SR 03 H
	131	22	CON3 M8525	CON TRAP EN H
	134	23	CON4 M8525	CON UCODE STATE 01 H
	135	23	CON4 M8525	CON UCODE STATE 03 H
	136	23	CON4 M8525	CON UCODE STATE 05 H
	137	23	CON4 M8525	CON UCODE STATE 07 H
	137	19	CON1 M8525	CON VMA SEL 1 L
	136	19	CON1 M8525	CON VMA SEL 2 L
	130	18	CON3 M8525	CON WR EVEN PAR ADR H
	135	22	CON2 M8525	CON2 INSTR GO L
	131	18	CON3 M8525	CON3 CACHE LOOK EN H
	130	19	CON3 M8525	CON3 WR EVEN PAR DATA H
	130	20	CON3 M8525	CON3 WR EVEN PAR DIR H
	132	23	CON4 M8525	CON4 AR LOADED H
	133	24	CON5 M8525	CON5 MEM CYCLE L
	132	24	CON5 M8525	CON5 PI CYCLE H
	164	32	MBC4 M8531	CORE ADR 34 H
	164	33	MBC4 M8531	CORE ADR 35 H
	163	28	MBC5 M8531	CORE BUSY B H
	160	15	MBZ1 M8537	CORE BUSY H
	165	29	MBC4 M8531	CORE DATA VALID -1 L
	165	31	MBC4 M8531	CORE DATA VALID L
**	145	01	CRA1 M8511	CR ADR 00 F H
**	145	02	CRA1 M8511	CR ADR 01 F H
**	145	03	CRA1 M8511	CR ADR 02 F H
**	145	04	CRA1 M8511	CR ADR 03 F H
**	145	05	CRA1 M8511	CR ADR 04 F H
**	144	00	CRA2 M8511	CR ADR 05 F H
**	144	01	CRA2 M8511	CR ADR 06 F H
**	144	02	CRA2 M8511	CR ADR 07 F H
**	144	03	CRA2 M8511	CR ADR 08 F H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	144	04	CRA2	M8511	CR ADR 09 F H
**	144	05	CRA2	M8511	CR ADR 10 F H
**	141	01	CRA3	M8511	CRA DISP 00 H
**	141	02	CRA3	M8511	CRA DISP 01 H
**	141	03	CRA3	M8511	CRA DISP 02 H
**	141	04	CRA3	M8511	CRA DISP 03 H
**	141	05	CRA3	M8511	CRA DISP 04 H
**	141	00	CRA3	M8511	CRA DISP PARITY H
**	147	01	CRA3	M8511	CRA LOC 00 H
**	147	02	CRA3	M8511	CRA LOC 01 H
**	147	03	CRA3	M8511	CRA LOC 02 H
**	147	04	CRA3	M8511	CRA LOC 03 H
**	147	05	CRA3	M8511	CRA LOC 04 H
**	146	00	CRA3	M8511	CRA LOC 05 H
**	146	01	CRA3	M8511	CRA LOC 06 H
**	146	02	CRA3	M8511	CRA LOC 07 H
**	146	03	CRA3	M8511	CRA LOC 08 H
**	146	04	CRA3	M8511	CRA LOC 09 H
**	146	05	CRA3	M8511	CRA LOC 10 H
*	147	08-11	CRM5	M8528	CRAM 00-03 H
*	147	14-17	CRM5	M8528	CRAM 04-07 H
*	147	20-23	CRM5	M8528	CRAM 08-11 H
*	147	26-29	CRM5	M8528	CRAM 12-15 H
*	147	32-35	CRM5	M8528	CRAM 16-19 H
*	146	08-11	CRM5	M8528	CRAM 20-23 H
*	146	14-17	CRM5	M8528	CRAM 24-27 H
*	146	20-23	CRM5	M8528	CRAM 28-31 H
*	146	26-29	CRM5	M8528	CRAM 32-35 H
*	146	32-35	CRM5	M8528	CRAM 36-39 H
*	145	08-11	CRM5	M8528	CRAM 40-43 H
*	145	14-17	CRM5	M8528	CRAM 44-47 H
*	145	20-23	CRM5	M8528	CRAM 48-51 H
*	145	26-29	CRM5	M8528	CRAM 52-55 H
*	145	32-35	CRM5	M8528	CRAM 56-59 H
**	144	08	CRM5	M8528	CRAM 60 H
**	144	10	CRM5	M8528	CRAM 62 H
**	144	14	CRM5	M8528	CRAM 64 H
**	144	16	CRM5	M8528	CRAM 66 H
**	144	20	CRM5	M8528	CRAM 68 H
**	144	22	CRM5	M8528	CRAM 70 H
**	144	26	CRM5	M8528	CRAM 72 H
**	144	28	CRM5	M8528	CRAM 74 H
**	144	32	CRM5	M8528	CRAM 76 H
**	144	34	CRM5	M8528	CRAM 78 H
**	144	11	CRM5	M8528	CRAM PAR 00 H
**	144	17	CRM5	M8528	CRAM PAR 04 H
**	144	23	CRM5	M8528	CRAM PAR 08 H
**	144	29	CRM5	M8528	CRAM PAR 12 H
**	144	35	CRM5	M8528	CRAM PAR 16 H
**	144	09	CRM5	M8528	CRAM PAR 1ST 00 H
**	144	15	CRM5	M8528	CRAM PAR 1ST 04 H
**	144	21	CRM5	M8528	CRAM PAR 1ST 08 H
**	144	27	CRM5	M8528	CRAM PAR 1ST 12 H
**	144	33	CRM5	M8528	CRAM PAR 1ST 16 H
**	170	00	CRC6	M8535	CRC CH BUF ADR 0 H
**	171	00	CRC6	M8535	CRC CH BUF ADR 1 H
**	172	00	CRC6	M8535	CRC CH BUF ADR 2 H
**	173	00	CRC6	M8535	CRC CH BUF ADR 3 H
**	174	00	CRC6	M8535	CRC CH BUF ADR 4 H
**	175	00	CRC6	M8535	CRC CH BUF ADR 5 H
**	176	00	CRC6	M8535	CRC CH BUF ADR 6 H
	172	03	CRC3	M8535	CRC ERR IN H
	172	02	CRC3	M8535	CRC LAST WORD IN H
	171	04	CRC4	M8535	CRC LONG WC ERR H
	170	02	CRC4	M8535	CRC MEM STORE ENA L
	171	02	CRC4	M8535	CRC OVN ERR IN H
	172	01	CRC3	M8535	CRC READY IN H
	172	04	CRC3	M8535	CRC REVERSE IN H
	171	01	CRC4	M8535	CRC RH20 ERR IN H
	175	01	CRC6	M8535	CRC SEL 1D L
	175	02	CRC6	M8535	CRC SEL 2D L
	175	03	CRC6	M8535	CRC SEL 4D L
	171	03	CRC4	M8535	CRC SHORT WC ERR H
	174	02	CRC5	M8535	CRC WR RAM L
	174	01	CRC1	M8535	CRC1 ACT FLAG ENA H
	175	04	CRC1	M8535	CRC1 AF REQ ENA L
	176	01	CRC1	M8535	CRC1 MEM PTR0 H
	176	02	CRC1	M8535	CRC1 MEM PTR1 H
	176	03	CRC1	M8535	CRC1 MEM PTR2 H

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DF	BIT	DRAWING	BOARD	NAME AND TRUTH
176	04	CRC1	M8535	CRC1 MEM PTR3 H
177	00	CRC1	M8535	CRC1 PTR DIF=0 H
173	01	CRC2	M8535	CRC2 ACT CTR 0R H
173	02	CRC2	M8535	CRC2 ACT CTR 1R H
173	03	CRC2	M8535	CRC2 ACT CTR 2R H
173	04	CRC2	M8535	CRC2 RAM CYC H
174	03	CRC3	M8535	CRC3 OP CODE 00 H
174	04	CRC3	M8535	CRC3 OP CODE 01 H
170	03	CRC4	M8535	CRC4 DONE IN H
170	01	CRC4	M8535	CRC4 RESET IN L
170	04	CRC4	M8535	CRC4 STORE IN H
177	01	CRC6	M8535	CRC6 CH ADR 0C L
177	02	CRC6	M8535	CRC6 CH ADR 1C L
177	03	CRC6	M8535	CRC6 CH ADR 2C L
177	04	CRC6	M8535	CRC6 CH ADR 3C L
170	20	CHX2	M8515	CSH 0 ANY VAL L
177	25	CHA3	M8513	CSH 0 ANY WR L
171	20	CHX2	M8515	CSH 1 ANY VAL L
175	25	CHA3	M8513	CSH 1 ANY WR L
172	20	CHX2	M8515	CSH 2 ANY VAL L
176	25	CHA3	M8513	CSH 2 ANY WR L
173	20	CHX2	M8515	CSH 3 ANY VAL L
174	25	CHA3	M8513	CSH 3 ANY WR L
174	27	CSH3	M8513	CSH ADR PMA EN H
172	28	CSH1	M8513	CSH CCA CYC L
174	31	MBX1	M8529	CSH CCA INVAL CSH H
175	31	MBX1	M8529	CSH CCA VAL CORE H
173	28	CSH7	M8513	CSH CCA WRITEBACK L
160	33	MBC2	M8531	CSH DATA CLR DONE IN L
170	27	CSH4	M8513	CSH DATA CLR DONE L
161	27	MBC2	M8531	CSH DATA CLR T1 L
161	28	MBC2	M8531	CSH DATA CLR T2 L
161	29	MBC2	M8531	CSH DATA CLR T3 L
174	20	CHX4	M8515	CSH DIR 0 PAR ODD H
175	20	CHX4	M8515	CSH DIR 1 PAR ODD H
176	20	CHX4	M8515	CSH DIR 2 PAR ODD H
177	20	CHX4	M8515	CSH DIR 3 PAR ODD H
176	28	CSH7	M8513	CSH E WRITEBACK L
171	25	CSH6	M8513	CSH EBOX LOAD REG H
175	22	CSH2	M8513	CSH EBOX RETRY REQ L
170	29	CSH4	M8513	CSH EBOX T3 L
160	19	MBZ1	M8537	CSH EN CSH DATA L
171	26	CSH7	M8513	CSH FILL CACHE RD L
173	25	CHX3	M8513	CSH LRU 1 H
172	25	CHX3	M8513	CSH LRU 2 H
175	28	CSH1	M8513	CSH MB CYC L
161	26	MBZ6	M8537	CSH PAR BIT A H
162	26	MBZ6	M8537	CSH PAR BIT B H
162	17	MBZ5	M8537	CSH PAR BIT IN H
170	28	CSH4	M8513	CSH REFILL RAM WR L
161	30	MBC2	M8531	CSH SEL LRU H
174	26	CSH5	M8513	CSH T0 L
176	26	CSH5	M8513	CSH T2 L
175	21	CHX3	M8515	CSH USE ADR 2 H
176	21	CHX3	M8515	CSH USE ADR 3 H
177	21	CHX3	M8515	CSH USE ADR 4 H
172	27	CSH6	M8513	CSH USE HOLD H
170	21	CHX3	M8515	CSH USE IN 0 H
171	21	CHX3	M8515	CSH USE IN 1 H
172	21	CHX3	M8515	CSH USE IN 2 H
173	21	CHX3	M8515	CSH USE IN 3 H
174	21	CHX3	M8515	CSH USE IN 4 H
175	23	CSH6	M8513	CSH USE WR EN H
163	29	MBC3	M8531	CSH VAL SEL ALL H
163	30	MBC3	M8531	CSH VAL WR DATA H
163	31	MBC3	M8531	CSH WR SEL ALL H
176	31	MBX4	M8529	CSH WR WD 0 EN H
177	31	MBX4	M8529	CSH WR WD 1 EN H
170	32	MBX4	M8529	CSH WR WD 2 EN H
171	32	MBX4	M8529	CSH WR WD 3 EN H
163	32	MBC3	M8531	CSH WR WR DATA H
174	29	CSH1	M8513	CSH1 CACHE IDLE L
174	28	CSH1	M8513	CSH1 EBOX CYC B L
172	26	CSH1	M8513	CSH1 READY TO GO A H
174	22	CSH2	M8513	CSH2 E CORE RD RQ A L
172	29	CSH2	M8513	CSH2 EBOX REQ EN L
173	23	CSH2	M8513	CSH2 MBOX RESP L
173	22	CSH2	M8513	CSH2 ONE WORD RD A L
173	24	CSH2	M8513	CSH2 RD PSE 2ND REQ EN L

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	170	25	CSH2	M8513	CSH2 WR TEST L
	176	24	CSH4	M8513	CSH4 EBOX T0 L
	171	29	CSH4	M8513	CSH4 EBOX T1 L
	173	29	CSH4	M8513	CSH4 EBOX T2 L
	177	29	CSH4	M8513	CSH4 EBOX WR T4 L
	177	24	CSH4	M8513	CSH4 PAGE FAIL DLY H
	173	27	CSH4	M8513	CSH4 WRITEBACK T1 A H
	171	27	CSH5	M8513	CSH5 CHAN WR T5 L
	170	22	CSH5	M8513	CSH5 PAGE REFILL COMP L
	177	26	CSH5	M8513	CSH5 PAGE REFILL T10 L
	174	24	CSH5	M8513	CSH5 PAGE REFILL T9,12 L
	173	26	CSH5	M8513	CSH5 T1 L
	175	26	CSH5	M8513	CSH5 T3 L
	177	23	CSH6	M8513	CSH6 DATA DLY 1 L
	171	23	CSH6	M8513	CSH6 WR DATA RDY L
	106	24	CTL1	M8527	CTL AD LONG H
	106	25	CTL1	M8527	CTL ADX CRY 36 A H
	105	25	CTL1	M8527	CTL ADX CRY 36 H
	100	28	CTL2	M8527	CTL AR 00-08 LOAD L
	104	28	CTL2	M8527	CTL AR 00-11 CLR H
	101	28	CTL2	M8527	CTL AR 09-17 LOAD L
	105	28	CTL2	M8527	CTL AR 12-17 CLR H
	101	26	CTL2	M8527	CTL ARL SEL 1 H
	100	26	CTL2	M8527	CTL ARL SEL 2 H
	103	28	CTL2	M8527	CTL ARL SEL 4 H
	106	28	CTL2	M8527	CTL ARR CLR H
	100	27	CTL2	M8527	CTL ARR LOAD A L
	101	27	CTL2	M8527	CTL ARR LOAD B L
	103	26	CTL2	M8527	CTL ARR SEL 1 H
	102	26	CTL2	M8527	CTL ARR SEL 2 H
	102	28	CTL2	M8527	CTL ARX LOAD H
	105	26	CTL2	M8527	CTL ARXL SEL 1 H
	104	26	CTL2	M8527	CTL ARXL SEL 2 H
	107	26	CTL2	M8527	CTL ARXR SEL 1 H
	106	26	CTL2	M8527	CTL ARXR SEL 2 H
	102	25	CTL1	M8527	CTL COND/AR GETS EXP H
	103	25	CTL1	M8527	CTL DISP RET L
	107	24	CTL1	M8527	CTL INH CRY 18 L
	136	14	CTL1	M8522	CTL INH CRY 18 L
	104	25	CTL1	M8527	CTL LOAD PC L
	105	27	CTL2	M8527	CTL MQ SEL 1 H
	104	27	CTL2	M8527	CTL MQ SEL 2 H
	106	27	CTL2	M8527	CTL MQM EN H
	103	27	CTL2	M8527	CTL MQM SEL 1 H
	102	27	CTL2	M8527	CTL MQM SEL 2 H
	107	28	CTL2	M8527	CTL SPEC CALL L
	101	25	CTL1	M8527	CTL SPEC MTR CTL L
	101	24	CTL1	M8527	CTL SPEC/CLR FPD H
	104	24	CTL1	M8527	CTL SPEC/FLAG CTL H
	102	24	CTL1	M8527	CTL SPEC/GEN CRY 18 H
	136	15	CTL1	M8522	CTL SPEC/GEN CRY 18 H
	100	25	CTL1	M8527	CTL SPEC/SAVE FLAGS L
	100	24	CTL1	M8527	CTL SPEC/SCM ALT H
	103	24	CTL1	M8527	CTL SPEC/SECTION HOLD H
	105	24	CTL1	M8527	CTL SPEC/SP MEM CYCLE H
	163	33	MBC3	M8531	DATA VALID A OUT H
	164	27	MBC3	M8531	DATA VALID B OUT H
	107	27	CTL3	M8527	DIAG LOAD EBUS REG L
	107	25	CTL3	M8527	DIAG MEM RESET H
	140	03	CRA3	M8511	DISP 02 A H
	140	04	CRA3	M8511	DISP 03 A H
	140	05	CRA3	M8511	DISP 04 A H
	140	01	CRA3	M8511	DISP EN 00-03 L
	140	00	CRA3	M8511	DISP EN 00-07 L
	140	02	CRA3	M8511	DISP EN 30-37 L
**	130	15	IRD1	M8522	DR ADR 00 A H
**	130	16	IRD1	M8522	DR ADR 01 A H
**	130	17	IRD1	M8522	DR ADR 02 A H
**	131	12	IRD1	M8522	DR ADR 03 A H
**	131	13	IRD1	M8522	DR ADR 04 A H
**	131	14	IRD1	M8522	DR ADR 05 A H
**	131	15	IRD1	M8522	DR ADR 06 A H
**	131	16	IRD1	M8522	DR ADR 07 A H
**	131	17	IRD1	M8522	DR ADR 08 A H
**	133	12	IRD1	M8522	DRAM A 00 H
**	133	13	IRD1	M8522	DRAM A 01 H
**	133	14	IRD1	M8522	DRAM A 02 H
**	133	15	IRD1	M8522	DRAM B 00 H
**	133	16	IRD1	M8522	DRAM B 01 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	133	17	IRD1	M8522	DRAM B 02 H
**	134	14	IRD1	M8522	DRAM J 01 H
**	134	15	IRD1	M8522	DRAM J 02 H
**	134	16	IRD1	M8522	DRAM J 03 H
**	134	17	IRD1	M8522	DRAM J 04 H
**	135	14	IRD1	M8522	DRAM J 07 H
**	135	15	IRD1	M8522	DRAM J 08 H
**	135	16	IRD1	M8522	DRAM J 09 H
**	135	17	IRD1	M8522	DRAM J 10 H
	135	13	IRD3	M8522	DRAM ODD PARITY H
**	135	12	IRD1	M8522	DRAM PAR H
	176	27	CSH2	M8513	E CACHE WR CYC H
**	102	14	PIC4	M8532	EBUS CS00 E H
**	102	15	PIC4	M8532	EBUS CS01 E H
**	102	16	PIC4	M8532	EBUS CS02 E H
**	102	17	PIC4	M8532	EBUS CS03 E H
**	103	14	PIC4	M8532	EBUS CS04 E H
**	102	11	PIC4	M8532	EBUS CS05 E H
**	102	12	PIC4	M8532	EBUS CS06 E H
	102	13	PIC2	M8532	EBUS DEMAND E H
*	167	00-08	MBZ2	M8537	EBUS REG 00-08 H
*	167	14-26	MBZ2	M8537	EBUS REG 14-26 H
*	167	27-33	MBC1	M8531	EBUS REG 27-33 H
*	167	34,35	MBZ2	M8537	EBUS REG 34,35 H
**	120	00	EDP1	M8512	EDP AR 00 H
**	120	01	EDP1	M8512	EDP AR 01 H
**	120	02	EDP1	M8512	EDP AR 02 H
**	120	03	EDP1	M8512	EDP AR 03 H
**	120	04	EDP1	M8512	EDP AR 04 H
**	120	05	EDP1	M8512	EDP AR 05 H
**	120	06	EDP1	M8512	EDP AR 06 H
**	120	07	EDP1	M8512	EDP AR 07 H
**	120	08	EDP1	M8512	EDP AR 08 H
**	120	09	EDP1	M8512	EDP AR 09 H
**	120	10	EDP1	M8512	EDP AR 10 H
**	120	11	EDP1	M8512	EDP AR 11 H
**	133	07	SCD2	M8524	FE 00 H
**	133	08	SCD2	M8524	FE 01 H
**	133	09	SCD2	M8524	FE 02 H
**	133	10	SCD2	M8524	FE 03 H
**	133	11	SCD2	M8524	FE 04 H
**	132	07	SCD2	M8524	FE 05 H
**	132	08	SCD2	M8524	FE 06 H
**	132	09	SCD2	M8524	FE 07 H
**	132	10	SCD2	M8524	FE 08 H
**	132	11	SCD2	M8524	FE 09 H
	135	07	SCD2	M8524	FE SIGN H
*	123	0-35	EDP4	M8512	FM 0 TO 35 H
	172	32	MBX1	M8529	FORCE NO MATCH H
	160	27	MBC5	M8531	FORCE VALID MATCH 0 H
	160	28	MBC5	M8531	FORCE VALID MATCH 1 H
	160	29	MBC5	M8531	FORCE VALID MATCH 2 H
	160	30	MBC5	M8531	FORCE VALID MATCH 3 H
	136	16	IRD4	M8522	GEN CRY 36 H
**	132	14	IRD1	M8522	IR AC 09 H
**	132	15	IRD1	M8522	IR AC 10 H
**	132	16	IRD1	M8522	IR AC 11 H
**	132	17	IRD1	M8522	IR AC 12 H
	132	13	IRD3	M8522	IR EN AC H
	132	12	IRD3	M8522	IR EN I/O, JRST H
	136	13	IRD1	M8522	IR I/O LEGAL H
	134	13	IRD3	M8522	IR JRST 0, L
	130	12	IRD3	M8522	IR NORM 08 H
	130	13	IRD3	M8522	IR NORM 09 H
	130	14	IRD3	M8522	IR NORM 10 H
	174	32	MBX3	M8529	MB DATA CODE 1 H
	175	32	MBX3	M8529	MB DATA CODE 2 H
	160	20	MBZ1	M8537	MB IN SEL 1 H
	161	20	MBZ1	M8537	MB IN SEL 2 H
	162	20	MBZ1	M8537	MB IN SEL 4 H
	160	18	MBZ5	M8537	MB PAR BIT IN H
	176	32	MBX3	M8529	MB PAR H
	177	32	MBX2	M8529	MB REQ HOLD H
	170	33	MBX5	M8529	MB REQ IN H
	171	33	MBX2	M8529	MB SEL 1 H
	172	33	MBX2	M8529	MB SEL 2 H
	173	33	MBX2	M8529	MB SEL HOLD H
	175	24	CSH3	M8513	MB TEST PAR A IN L
	171	28	CSH3	M8513	MB WR RQ CLR NXT L

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

DF	BIT	DRAWING	BOARD	NAME AND TRUTH
174	33	MBX6	M8529	MB0 HOLD IN H
175	33	MBX6	M8529	MB1 HOLD IN H
176	33	MBX6	M8529	MB2 HOLD IN H
177	33	MBX6	M8529	MB3 HOLD IN H
164	28	MBC3	M8531	MBC INH 1ST MB REQ H
162	27	MBC2	M8531	MBC2 CACHE WR 00 A H
162	28	MBC2	M8531	MBC2 CACHE WR 09 A H
162	29	MBC2	M8531	MBC2 CACHE WR 18 A H
162	30	MBC2	M8531	MBC2 CACHE WR 27 A H
160	32	MBC2	M8531	MBC2 CSH ADR WR PULSE H
161	31	MBC2	M8531	MBC2 CSH VAL WR PULSE H
161	32	MBC2	M8531	MBC2 CSH WR WR PULSE H
162	33	MBC3	M8531	MBC3 ANY SBUS RQ IN L
163	27	MBC3	M8531	MBC3 B CHANGE COMING L
165	30	MBC4	M8531	MBC4 CORE DATA VALID -2 L
165	32	MBC4	M8531	MBC4 CORE RD IN PROG H
161	15	MBZ4	M8537	MBOX ADR PAR ERR L
175	27	CSH3	M8513	MBOX GATE VMA 27-33 H
162	24	MBZ4	M8537	MBOX MB PAR ERR L
161	22	MBZ3	M8537	MBOX NXM ERR L
170	24	CSH6	M8513	MBOX PT DIR WR L
161	24	MBZ4	M8537	MBOX SBUS ERR L
170	34	MBX5	M8529	MBX MEM TO C EN L
176	35	MBX3	M8529	MBX3 SBUS DIAG CYC L
173	30	MBX4	M8529	MBX4 CACHE TO MB DONE H
175	30	MBX4	M8529	MBX4 CACHE TO MB T3 L
160	22	MBZ1	M8537	MBZ1 CHAN CORE BUSY H
161	21	MBZ1	M8537	MBZ1 RD-PSE-WR REF L
161	23	MBZ3	M8537	MBZ3 CHAN MEM REF L
162	22	MBZ3	M8537	MBZ3 HOLD ERA L
162	18	MBZ3	M8537	MBZ3 SEQUENTIAL RQ H
162	23	MBZ4	M8537	MBZ4 NXM T2 H
160	24	MBZ4	M8537	MBZ4 NXM T6,7 L
161	18	MBZ6	M8537	MBZ6 CSH PAR BIT H
106	22	MCL4	M8530	MCL 18 BIT EA H
105	22	MCL4	M8530	MCL 23 BIT EA H
107	21	MCL4	M8530	MCL EA TYPE 09 H
107	20	MCL4	M8530	MCL EA TYPE 10 H
104	23	MCL6	M8530	MCL EBOX CACHE L
107	23	MCL6	M8530	MCL EBOX MAP L
105	23	MCL6	M8530	MCL EBOX MAY BE PAGED L
105	18	MCL2	M8530	MCL LOAD AR H
106	18	MCL2	M8530	MCL LOAD ARX H
104	22	MCL4	M8530	MCL LOAD VMA CONTEXT L
107	22	MCL5	M8530	MCL MBOX CYC REQ H
102	19	MCL1	M8530	MCL MEM/ARL IND H
115	15	APR6	M8539	MCL MEM/REG FUNC L
105	20	MCL3	M8530	MCL PAGE ADDRESS COND H
106	20	MCL3	M8530	MCL PAGE ILL ENTRY H
102	20	MCL2	M8530	MCL PAGE TEST PRIVATE H
104	20	MCL3	M8530	MCL PAGE UEBR REF H
103	21	MCL4	M8530	MCL PREV COND L
103	23	MCL5	M8530	MCL PREV SEC TO ARMM H
106	23	MCL6	M8530	MCL REG FUNC H
103	19	MCL1	M8530	MCL REQ EN L
107	18	MCL2	M8530	MCL STORE AR L
107	19	MCL2	M8530	MCL VMA EXTENDED L
102	22	MCL4	M8530	MCL VMA GETS AD H
103	22	MCL4	M8530	MCL VMA INC H
103	18	MCL2	M8530	MCL VMA PAUSE H
106	19	MCL2	M8530	MCL VMA PREVIOUS L
105	19	MCL2	M8530	MCL VMA PUBLIC H
102	18	MCL2	M8530	MCL VMA READ H
103	20	MCL3	M8530	MCL VMA UPT H
104	19	MCL2	M8530	MCL VMA USER H
104	18	MCL2	M8530	MCL VMA WRITE H
104	21	MCL4	M8530	MCL VMAX EN L
106	21	MCL4	M8530	MCL VMAX SEL 1 H
105	21	MCL4	M8530	MCL VMAX SEL 2 H
102	21	MCL4	M8530	MCL XR PREVIOUS H
165	33	MBC4	M8531	MEM ADR PAR H
162	21	MBZ1	M8537	MEM BUSY H
173	32	MBX3	M8529	MEM DATA TO MEM H
171	34	MBX3	M8529	MEM DIAG L
161	17	MEM5	M8537	MEM PAR IN H
166	27	MBC4	M8531	MEM RD RQ B H
172	34	MBX5	M8529	MEM RD RQ IN H
166	28	MBC4	M8531	MEM RQ 0 H
166	29	MBC4	M8531	MEM RQ 1 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	166	30	MBC4	M8531	MEM RQ 2 H
	166	31	MBC4	M8531	MEM RQ 3 H
	166	32	MBC4	M8531	MEM START L
	161	19	MBZ1	M8537	MEM TO C DIAG EN L
	164	29	MBC3	M8531	MEM TO C EN L
	173	34	MBX3	M8529	MEM TO C SEL 1 H
	174	34	MBX3	M8529	MEM TO C SEL 2 H
	175	34	MBX5	M8529	MEM WR RQ IN H
	166	33	MBC4	M8531	MEM WR RQ L
*	122	0-35	EDP2	M8512	MQ 0 TO 35 H
*	113	20-35	MTR1	M8538	MTR CACHE COUNT 02-17 H
	117	25	MTR3	M8538	MTR CONO MTR, L
*	112	20-35	MTR1	M8538	MTR EBOX COUNT 02-17 H
*	114	24-35	MTR1	M8538	MTR INTERVAL 06-17 H
*	111	20-35	MTR1	M8538	MTR PERF COUNT 02-17 H
*	115	24-35	MTR3	M8538	MTR PERIOD 06-17 H
*	110	20-35	MTR1	M8538	MTR TIME 02-17 H
	116	23	MTR2	M8538	MTR2 ACCT ON H
	116	22	MTR2	M8538	MTR2 EXEC ACCT EN H
	116	21	MTR2	M8538	MTR2 PI ACCT EN H
	116	25	MTR2	M8538	MTR2 TIME ON H
	115	22	MTR3	M8538	MTR3 INTERVAL DONE H
	115	21	MTR3	M8538	MTR3 INTERVAL ON H
	115	23	MTR3	M8538	MTR3 INTERVAL OVRFLO H
	117	22	MTR5	M8538	MTR5 INCR SEL 1 H
	117	21	MTR5	M8538	MTR5 INCR SEL 2 H
	117	20	MTR5	M8538	MTR5 VECTOR REQ H
	160	21	MBZ3	M8537	NXM ACKN H
	160	23	MBZ3	M8537	NXM ANY L
	161	25	MBZ3	M8537	NXM DATA VAL L
	175	29	CSH4	M8513	ONE WORD WR T0 L
	162	25	PAG5	M8537	PAG MB 00-17 PAR H
	160	26	PAG5	M8537	PAG MB 18-35 PAR H
	174	23	CSH6	M8513	PAGE FAIL HOLD L
	171	24	CSH4	M8513	PAGE FAIL T2 L
	177	22	CSH6	M8513	PAGE REFILL ERROR L
	176	29	CSH5	M8513	PAGE REFILL T4 L
	176	23	CSH5	M8513	PAGE REFILL T8 L
*	15X	13-35	VMA3	M8523	PC 13-35 H **NOTE
	164	30	MBC3	M8531	PHASE CHANGE COMING L
	110	17	PIC3	M8539	PI3 APR PIA 01 H
	110	16	PIC3	M8539	PI3 APR PIA 02 H
	110	15	PIC3	M8539	PI3 APR PIA 04 H
**	116	35	PIC3	M8538	PI3 MTR PIA 01 H
**	116	34	PIC3	M8538	PI3 MTR PIA 02 H
**	116	33	PIC3	M8538	PI3 MTR PIA 04 H
	100	10	PIC1	M8532	PIC1 ACTIVE H
**	101	11	PIC1	M8532	PIC1 GEN 1 H
**	101	12	PIC1	M8532	PIC1 GEN 2 H
**	101	13	PIC1	M8532	PIC1 GEN 3 H
**	101	14	PIC1	M8532	PIC1 GEN 4 H
**	101	15	PIC1	M8532	PIC1 GEN 5 H
**	101	16	PIC1	M8532	PIC1 GEN 6 H
**	101	17	PIC1	M8532	PIC1 GEN 7 H
**	100	11	PIC1	M8532	PIC1 ON 1 H
**	100	12	PIC1	M8532	PIC1 ON 2 H
**	100	13	PIC1	M8532	PIC1 ON 3 H
**	100	14	PIC1	M8532	PIC1 ON 4 H
**	100	15	PIC1	M8532	PIC1 ON 5 H
**	100	16	PIC1	M8532	PIC1 ON 6 H
**	100	17	PIC1	M8532	PIC1 ON 7 H
**	100	03	PIC1	M8532	PIC1 PIH1 H
**	100	04	PIC1	M8532	PIC1 PIH2 H
**	100	05	PIC1	M8532	PIC1 PIH3 H
**	100	06	PIC1	M8532	PIC1 PIH4 H
**	100	07	PIC1	M8532	PIC1 PIH5 H
**	100	08	PIC1	M8532	PIC1 PIH6 H
**	100	09	PIC1	M8532	PIC1 PIH7 H
	103	15	PIC2	M8532	PIC2 HONOR INTERNAL H
	103	16	PIC2	M8532	PIC2 READY H
	103	13	PIC2	M8532	PIC2 STATE HOLD H
	103	11	PIC2	M8532	PIC2 TIMER DONE H
	103	12	PIC5	M8532	PIC5 EBUS PI GRANT H
	103	17	PIC5	M8532	PIC5 EBUS REQ H
	177	28	CSH2	M8513	RD PAUSE 2ND HALF L
	176	34	MBX3	M8529	REFILL HOLD H
	177	34	MBX5	M8529	RQ 0 IN H
	170	35	MBX5	M8529	RQ 1 IN H
	171	35	MBX5	M8529	RQ 2 IN H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	172	35	MBX5	M8529	RQ 3 IN H
	161	33	MBC2	M8531	RQ HOLD FF H
**	143	01	CRA4	M8511	SBR RET 00 H
**	143	02	CRA4	M8511	SBR RET 01 H
**	143	03	CRA4	M8511	SBR RET 02 H
**	143	04	CRA4	M8511	SBR RET 03 H
**	143	05	CRA4	M8511	SBR RET 04 H
**	142	00	CRA4	M8511	SBR RET 05 H
**	142	01	CRA4	M8511	SBR RET 06 H
**	142	02	CRA4	M8511	SBR RET 07 H
**	142	03	CRA4	M8511	SBR RET 08 H
**	142	04	CRA4	M8511	SBR RET 09 H
**	142	05	CRA4	M8511	SBR RET 10 H
	173	35	MBX2	M8529	SBUS ADR 34 H
	174	35	MBX2	M8529	SBUS ADR 35 H
	162	31	MBC2	M8531	SBUS ADR HOLD H
	175	35	MBX3	M8529	SBUS DIAG 3 L
	136	07	SCD2	M8524	SC .GE. 36 H
**	131	07	SCD2	M8524	SC 00 H
**	131	08	SCD2	M8524	SC 01 H
**	131	09	SCD2	M8524	SC 02 H
**	131	10	SCD2	M8524	SC 03 H
**	131	11	SCD2	M8524	SC 04 H
**	130	07	SCD2	M8524	SC 05 H
**	130	08	SCD2	M8524	SC 06 H
**	130	09	SCD2	M8524	SC 07 H
**	130	10	SCD2	M8524	SC 08 H
**	130	11	SCD2	M8524	SC 09 H
	134	07	SCD2	M8524	SC SIGN H
	133	04	SCD1	M8524	SCAD=0 L
	137	06	SCD5	M8524	SCD ADR BREAK PREVENT H
	137	05	SCD5	M8524	SCD ADR BRK CYC H
	137	02	SCD5	M8524	SCD ADR BRK INH H
	131	03	SCD4	M8524	SCD CRY0 H
	131	04	SCD4	M8524	SCD CRY1 H
	131	06	SCD4	M8524	SCD DIV CHK H
	132	03	SCD4	M8524	SCD FOV H
	130	06	SCD4	M8524	SCD FPD H
	132	04	SCD4	M8524	SCD FXU H
	135	04	SCD5	M8524	SCD KERNEL MODE H
	136	02	SCD5	M8524	SCD KERNEL OR USER IOT H
	134	03	SCD5	M8524	SCD LEAVE USER H
	133	03	SCD5	M8524	SCD LOAD FLAGS A H
	133	06	SCD4	M8524	SCD NICOND 10 H
	131	02	SCD4	M8524	SCD OV H
	133	02	SCD4	M8524	SCD PCP H
	135	06	SCD5	M8524	SCD PRIVATE INSTR EN L
	135	05	SCD5	M8524	SCD PRIVATE INSTR L
	135	03	SCD5	M8524	SCD PUBLIC A H
	135	02	SCD5	M8524	SCD PUBLIC EN L
	134	06	SCD5	M8524	SCD PUBLIC PAGE H
	137	07	SCD4	M8524	SCD TRAP CLEAR L
	130	04	SCD4	M8524	SCD TRAP CYC 1 H
	130	03	SCD4	M8524	SCD TRAP CYC 2 H
**	136	03	SCD3	M8524	SCD TRAP MIX 32 H
**	136	04	SCD3	M8524	SCD TRAP MIX 33 H
**	137	03	SCD3	M8524	SCD TRAP MIX 34 H
**	137	04	SCD3	M8524	SCD TRAP MIX 35 H
	130	05	SCD4	M8524	SCD TRAP REQ 1 H
	130	02	SCD4	M8524	SCD TRAP REQ 2 H
	134	02	SCD5	M8524	SCD USER A L
	134	05	SCD5	M8524	SCD USER EN L
	136	05	SCD5	M8524	SCD USER IOT A H
	136	06	SCD5	M8524	SCD USER IOT EN L
	160	17	SHD1	M8537	SH AR PAR ODD A H
	105	31	SHD1	M8526	SH AR PAR ODD H
	106	31	SHD1	M8526	SH ARX PAR ODD H
	134	12	IRD3	M8522	TEST SATISFIED H
*	15X	13-35	VMA2	M8523	VMA 13-35 H **NOTE
	153	13	VMA1	M8523	VMA 18-31=0 H
	157	13	VMA1	M8523	VMA AC REF H
*	15X	13-35	VMA4	M8523	VMA HELD 13-35 H **NOTE
	132	02	SCD4	M8524	VMA HELD OR PC 00 H
**	100	18	MCL3	M8530	VMA HELD OR PC 01 H
**	100	19	MCL3	M8530	VMA HELD OR PC 02 H
**	100	20	MCL3	M8530	VMA HELD OR PC 03 H
**	100	21	MCL3	M8530	VMA HELD OR PC 04 H
**	100	22	MCL3	M8530	VMA HELD OR PC 05 H
**	100	23	MCL3	M8530	VMA HELD OR PC 06 H

KL10(PA) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	101	18	MCL3	M8530	VMA HELD OR PC 07 H
**	101	19	MCL3	M8530	VMA HELD OR PC 08 H
**	101	20	MCL3	M8530	VMA HELD OR PC 09 H
**	101	21	MCL3	M8530	VMA HELD OR PC 10 H
**	101	22	MCL3	M8530	VMA HELD OR PC 11 H
**	101	23	MCL3	M8530	VMA HELD OR PC 12 H
	157	15	VMA3	M8523	VMA MATCH 13-35 H
	160	31	MBC1	M8531	WRITE OK H
	177	35	MBX4	M8529	WRITEBACK T2 L

NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(*) or (**)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (**) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	100	03	PIC1	M8532	PIC1 PIH1 H
**	100	04	PIC1	M8532	PIC1 PIH2 H
**	100	05	PIC1	M8532	PIC1 PIH3 H
**	100	06	PIC1	M8532	PIC1 PIH4 H
**	100	07	PIC1	M8532	PIC1 PIH5 H
**	100	08	PIC1	M8532	PIC1 PIH6 H
**	100	09	PIC1	M8532	PIC1 PIH7 H
	100	10	PIC1	M8532	PIC1 ACTIVE H
**	100	11	PIC1	M8532	PIC1 ON 1 H
**	100	12	PIC1	M8532	PIC1 ON 2 H
**	100	13	PIC1	M8532	PIC1 ON 3 H
**	100	14	PIC1	M8532	PIC1 ON 4 H
**	100	15	PIC1	M8532	PIC1 ON 5 H
**	100	16	PIC1	M8532	PIC1 ON 6 H
**	100	17	PIC1	M8532	PIC1 ON 7 H
**	100	18	MCL3	M8544	VMA HELD OR PC 01 H
**	100	19	MCL3	M8544	VMA HELD OR PC 02 H
**	100	20	MCL3	M8544	VMA HELD OR PC 03 H
**	100	21	MCL3	M8544	VMA HELD OR PC 04 H
**	100	22	MCL3	M8544	VMA HELD OR PC 05 H
**	100	23	MCL3	M8544	VMA HELD OR PC 06 H
	100	24	CTL1	M8543	CTL SPEC/SCM ALT H
	100	25	CTL1	M8543	CTL SPEC/SAVE FLAGS L
	100	26	CTL2	M8543	CTL ARL SEL 2 H
	100	27	CTL2	M8543	CTL ARR LOAD A L
	100	28	CTL2	M8543	CTL AR 00-08 LOAD L
	100	30	CLK1	M8526YA	CLK EBUS CLK H
	100	31	CLK1	M8526YA	CLK SBUS CLK H
	100	32	CLK4	M8526YA	CLK INSTR 1777 H
	100	33	CLK5	M8526YA	CLK5 BURST CNT=0 H
**	100	34	CLK5	M8526YA	CLK5 BURST 128 H
**	100	35	CLK5	M8526YA	CLK5 BURST 64 H
**	101	11	PIC1	M8532	PIC1 GEN 1 H
**	101	12	PIC1	M8532	PIC1 GEN 2 H
**	101	13	PIC1	M8532	PIC1 GEN 3 H
**	101	14	PIC1	M8532	PIC1 GEN 4 H
**	101	15	PIC1	M8532	PIC1 GEN 5 H
**	101	16	PIC1	M8532	PIC1 GEN 6 H
**	101	17	PIC1	M8532	PIC1 GEN 7 H
**	101	18	MCL3	M8544	VMA HELD OR PC 07 H
**	101	19	MCL3	M8544	VMA HELD OR PC 08 H
**	101	20	MCL3	M8544	VMA HELD OR PC 09 H
**	101	21	MCL3	M8544	VMA HELD OR PC 10 H
**	101	22	MCL3	M8544	VMA HELD OR PC 11 H
**	101	23	MCL3	M8544	VMA HELD OR PC 12 H
	101	24	CTL1	M8543	CTL SPEC/CLR FPD H
	101	25	CTL1	M8543	CTL SPEC MTR CTL L
	101	26	CTL2	M8543	CTL ARL SEL 1 H
	101	27	CTL2	M8543	CTL ARR LOAD B L
	101	28	CTL2	M8543	CTL AR 09-17 LOAD L
**	101	30	CLK5	M8526YA	CLK5 BURST 32 H
**	101	31	CLK5	M8526YA	CLK5 BURST 16 H
**	101	32	CLK5	M8526YA	CLK5 BURST 08 H
**	101	33	CLK5	M8526YA	CLK5 BURST 04 H
**	101	34	CLK5	M8526YA	CLK5 BURST 02 H
**	101	35	CLK5	M8526YA	CLK5 BURST 01 H
**	102	11	PIC4	M8532	EBUS CS05 E H
**	102	12	PIC4	M8532	EBUS CS06 E H
	102	13	PIC2	M8532	EBUS DEMAND E H
**	102	14	PIC4	M8532	EBUS CS00 E H
**	102	15	PIC4	M8532	EBUS CS01 E H
**	102	16	PIC4	M8532	EBUS CS02 E H
**	102	17	PIC4	M8532	EBUS CS03 E H
	102	18	MCL2	M8544	MCL2 VMA READ H
	102	19	MCL1	M8544	MCL1 MEM/ARL IND H
	102	20	MCL3	M8544	MCL3 PAGE TEST PRIVATE H
	102	21	MCL4	M8544	MCL4 XR PREVIOUS H
	102	22	MCL4	M8544	MCL4 VMA GETS AD H
	102	23	MCL4	M8544	MCL4 XR SHORT H
	102	24	CTL1	M8543	CTL SPEC/GEN CRY 18 H
	102	25	CTL1	M8543	CTL COND/AR GETS EXP H
	102	26	CTL2	M8543	CTL ARR SEL 2 H
	102	27	CTL2	M8543	CTL MQM SEL 2 H
	102	28	CTL2	M8543	CTL ARX LOAD H
	102	30	CLK1	M8526YA	CLK ERROR STOP H
	102	31	CLK2	M8526YA	CLK2 GO L
	102	32	CLK4	M8526YA	CLK EBOX REQ H
	102	33	CLK3	M8526YA	CLK3 SYNC H
	102	34	CLK4	M8526YA	CLK4 PAGE FAIL EN L

KL10 (PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	102	35	CLK4	M8526YA	CLK FORCE 1777 H
	103	11	PIC2	M8532	PIC2 TIMER DONE H
	103	12	PIC5	M8532	PIC5 EBUS PI GRANT H
	103	13	PIC2	M8532	PIC2 STATE HOLD H
**	103	14	PIC4	M8532	EBUS CS04 E H
	103	15	PIC2	M8532	PIC2 HONOR INTERNAL H
	103	16	PIC2	M8532	PIC2 READY H
	103	17	PIC5	M8532	PIC5 EBUS REQ H
	103	18	MCL2	M8544	MCL2 VMA PAUSE H
	103	19	MCL1	M8544	MCL1 REQ EN L
	103	20	MCL6	M8544	MCL6 VMA UPT H
	103	21	MCL5	M8544	MCL5 VMA ADR ERR H
	103	22	MCL4	M8544	MCL4 VMA INC H
	103	23	MCL4	M8544	MCL4 SHORT STACK H
	103	24	CTL1	M8543	CTL SPEC/STACK UPDATE H
	103	25	CTL1	M8543	CTL DISP RET L
	103	26	CTL2	M8543	CTL ARR SEL 1 H
	103	27	CTL2	M8543	CTL MQM SEL 1 H
	103	28	CTL2	M8543	CTL ARL SEL 4 H
	103	30	CLK3	M8526YA	CLK3 DRAM PAR ERR H
	103	31	CLK2	M8526YA	CLK2 BURST L
	103	32	CLK4	M8526YA	CLK MB XFER H
	103	33	CLK4	M8526YA	CLK4 EBOX CLK L
	103	34	CLK4	M8526YA	CLK PAGE ERROR H
	103	35	CLK4	M8526YA	CLK4 1777 EN H
	104	18	MCL2	M8544	MCL2 VMA WRITE H
	104	19	MCL2	M8544	MCL VMA USER H
	104	20	MCL6	M8544	MCL6 PAGE UEBR REF H
	104	21	MCL5	M8544	MCL5 VMAX EN L
	104	22	MCL4	M8544	MCL4 LOAD VMA CONTEXT L
	104	23	MCL6	M8544	MCL6 EBOX CACHE L
	104	24	CTL1	M8543	CTL SPEC/FLAG CTL H
	104	25	CTL1	M8543	CTL LOAD PC L
	104	26	CTL2	M8543	CTL ARXL SEL 2 H
	104	27	CTL2	M8543	CTL MQ SEL 2 H
	104	28	CTL2	M8543	CTL AR 00-11 CLR H
	104	30	CLK3	M8526YA	CLK3 CRAM PAR ERR H
	104	31	CLK2	M8526YA	CLK2 EBOX SS L
	104	32	CLK5	M8526YA	CLK5 SOURCE SEL 2 H
	104	33	CLK3	M8526YA	CLK3 EBOX SOURCE H
	104	34	CLK5	M8526YA	CLK5 FM PAR CHECK L
	104	35	CLK5	M8526YA	CLK5 MBOX CYCLE DIS H
	105	18	MCL2	M8544	MCL LOAD AR H
	105	19	MCL2	M8544	MCL2 VMA PUBLIC H
	105	20	MCL3	M8544	MCL3 PAGE ADDRESS COND H
	105	21	MCL4	M8544	MCL4 VMAX SEL 2 H
	105	22	MCL5	M8544	MCL5 23 BIT EA H
	105	23	MCL6	M8544	MCL6 EBOX MAY BE PAGED L
	105	24	CTL1	M8543	CTL SPEC/SP MEM CYCLE H
	105	25	CTL1	M8543	CTL ADX CRY 36 H
	105	26	CTL2	M8543	CTL ARXL SEL 1 L
	105	27	CTL2	M8543	CTL MQ SEL 1 H
	105	28	CTL2	M8543	CTL AR 12-17 CLR H
	105	30	CLK3	M8526YA	CLK3 FM PAR ERR H
	105	31	SHD1	M8526YA	SH AR PAR ODD H
	105	32	CLK5	M8526YA	CLK5 SOURCE SEL 1 H
	105	33	CLK5	M8526YA	CLK5 EBOX CRM DIS H
	105	34	CLK5	M8526YA	CLK5 CRAM PAR CHECK L
	105	35	CLK5	M8526YA	CLK5 MBOX RESP SIM L
	106	18	MCL2	M8544	MCL LOAD ARX H
	106	19	MCL2	M8544	MCL2 VMA PREVIOUS L
	106	20	MCL3	M8544	MCL3 PAGE ILL ENTRY H
	106	21	MCL4	M8544	MCL4 VMAX SEL 1 H
	106	22	MCL5	M8544	MCL5 18 BIT EA H
	106	23	MCL6	M8544	MCL6 REG FUNC H
	106	24	CTL1	M8543	CTL AD LONG H
	106	25	CTL1	M8543	CTL ADX CRY 36 A H
	106	26	CTL2	M8543	CTL ARXR SEL 2 H
	106	27	CTL2	M8543	CTL MQM EN H
	106	28	CTL2	M8543	CTL ARR CLR H
	106	30	CLK3	M8526YA	CLK3 FS ERROR H
	106	31	SHD1	M8526YA	SH ARX PAR ODD H
	106	32	CLK5	M8526YA	CLK5 RATE SEL 2 H
	106	33	CLK5	M8526YA	CLK5 EBOX EDP DIS H
	106	34	CLK5	M8526YA	CLK5 DRAM PAR CHECK L
	106	35	CLK5	M8526YA	CLK5 AR/ARX PAR CHECK L
	107	18	MCL2	M8544	MCL STORE AR L
	107	19	MCL2	M8544	MCL2 VMA EXTENDED L
	107	20	MCL6	M8544	MCL6 VMA FETCH H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	107	21	MCL6	M8544	MCL6 PAGED FETCH L
	107	22	MCL5	M8544	MCL MBOX CYC REQ H
	107	23	MCL6	M8544	MCL6 EBOX MAP L
	107	24	CTL1	M8543	CTL INH CRY 18 L
	107	25	CTL3	M8543	DIAG MEM RESET H
	107	26	CTL2	M8543	CTL ARXR SEL 1 H
	107	27	CTL3	M8543	DIAG LOAD EBUS REG L
	107	28	CTL2	M8543	CTL SPEC CALL L
	107	30	CLK3	M8526YA	CLK3 ERROR L
	107	31	CLK4	M8526YA	CLK4 PAGE FAIL H
	107	32	CLK5	M8526YA	CLK5 RATE SEL 1 H
	107	33	CLK5	M8526YA	CLK5 EBOX CTL DIS H
	107	34	CLK5	M8526YA	CLK5 FS CHECK L
	107	35	CLK5	M8526YA	CLK5 ERR STOP EN L
	110	01	APR1	M8545	APR1 SWEEP BUSY EN H
	110	06	APR1	M8545	APR1 SBUS ERR IN H
	110	07	APR1	M8545	APR1 NXM ERR IN H
	110	08	APR1	M8545	APR1 I/O PF ERR IN H
	110	09	APR1	M8545	APR1 MB PAR ERR IN H
	110	10	APR2	M8545	APR2 C DIR P ERR IN H
	110	11	APR2	M8545	APR2 S ADR P ERR IN H
	110	12	APR2	M8545	APR2 PWR FAIL IN H
	110	13	APR2	M8545	APR2 SWEEP DONE IN H
	110	14	APR2	M8545	APR2 APR INTERRUPT H
	110	15	PIC3	M8545	PI3 APR PIA 04 H
	110	16	PIC3	M8545	PI3 APR PIA 02 H
	110	17	PIC3	M8545	PI3 APR PIA 01 H
*	110	20-35	MTR1	M8538	MTR TIME 02-17 H
	111	06	APR5	M8545	APR5 CURRENT BLOCK 4 H
	111	07	APR5	M8545	APR5 CURRENT BLOCK 2 H
	111	08	APR5	M8545	APR5 CURRENT BLOCK 1 H
	111	09	APR5	M8545	APR5 PREV BLOCK 4 H
	111	10	APR5	M8545	APR5 PREV BLOCK 2 H
	111	11	APR5	M8545	APR5 PREV BLOCK 1 H
	111	12	SHM1	M8540	SHM1 AR EXTENDED H
	111	13	APR3	M8545	APR3 FM EXTENDED H
	111	14	APR4	M8545	APR4 AC+# 09 H
	111	15	APR4	M8545	APR4 AC+# 10 H
	111	16	APR4	M8545	APR4 AC+# 11 H
	111	17	APR4	M8545	APR4 AC+# 12 H
*	111	20-35	MTR1	M8538	MTR PERF COUNT 02-17 H
	112	06	APR1	M8545	APR1 SBUS ERR EN IN H
	112	07	APR1	M8545	APR1 NXM ERR EN IN H
	112	08	APR1	M8545	APR1 I/O PF ERR EN IN H
	112	09	APR1	M8545	APR1 MB PAR ERR EN IN H
	112	10	APR2	M8545	APR2 C DIR P ERR EN IN H
	112	11	APR2	M8545	APR2 S ADR P ERR EN IN H
	112	12	APR2	M8545	APR2 PWR FAIL EN IN H
	112	13	APR2	M8545	APR2 SWEEP DONE EN IN H
*	112	20-35	MTR1	M8538	MTR EBOX COUNT 02-17 H
	113	09	APR3	M8545	APR3 FETCH COMP H
	113	10	APR3	M8545	APR3 READ COMP H
	113	11	APR3	M8545	APR3 WRITE COMP H
	113	12	APR3	M8545	APR3 USER COMP H
*	113	20-35	MTR1	M8538	MTR CACHE COUNT 02-17 H
	114	07	APR5	M8545	APR MBOX CTL 03 H
**	114	08	APR5	M8545	APR FM BLOCK 4 H
**	114	09	APR5	M8545	APR FM BLOCK 2 H
**	114	10	APR5	M8545	APR FM BLOCK 1 H
**	114	11	APR4	M8545	APR FM ADR 10 H
**	114	12	APR4	M8545	APR FM ADR 4 H
**	114	13	APR4	M8545	APR FM ADR 2 H
**	114	14	APR4	M8545	APR FM ADR 1 H
	114	15	APR4	M8545	APR4 F02 EN H
	114	16	APR3	M8545	APR FM 36 H
	114	17	APR3	M8545	APR3 FM ODD PARITY H
*	114	24-35	MTR1	M8538	MTR INTERVAL 06-17 H
	115	07	APR5	M8545	APR MBOX CTL 06 H
	115	08	APR5	M8545	APR5 SET PAGE FAIL L
	115	09	APR3	M8545	APR EBUS RETURN H
	115	10	APR3	M8545	APR EBOX DISABLE CS H
	115	11	APR2	M8545	APR2 WR BAD ADR PAR L
	115	12	APR6	M8545	APR6 EBOX CCA H
	115	13	APR6	M8545	APR EBOX ERA H
	115	14	APR6	M8545	APR6 EBOX SBUS DIAG H
	115	15	MCL1	M8545	MCL1 MEM/REG FUNC L
	115	16	APR6	M8545	APR6 EBOX LOAD REG L
	115	17	APR6	M8545	APR6 EBOX READ REG L
	115	21	MTR3	M8538	MTR3 INTERVAL ON H
	115	22	MTR3	M8538	MTR3 INTERVAL DONE H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	115	23	MTR3	M8538	MTR3 INTERVAL OVRFLO H
*	115	24-35	MTR3	M8538	MTR PERIOD 06-17 H
	116	07	APR5	M8545	APR5 WR PT SEL 0 H
	116	08	APR5	M8545	APR5 PT DIR WR L
	116	09	APR3	M8545	APR EBUS REQ L
	116	10	APR3	M8545	APR EBUS F01 E H
	116	11	APR2	M8545	APR ANY EBOX ERR FLG H
	116	12	APR6	M8545	APR6 EBOX UBR H
	116	13	APR6	M8545	APR EN REFILL RAM WR H
	116	21	MTR2	M8538	MTR2 PI ACCT EN H
	116	22	MTR2	M8538	MTR2 EXEC ACCT EN H
	116	23	MTR2	M8538	MTR2 ACCT ON H
	116	25	MTR2	M8538	MTR2 TIME ON H
**	116	33	PIC3	M8538	PI3 MTR PIA 04 H
**	116	34	PIC3	M8538	PI3 MTR PIA 02 H
**	116	35	PIC3	M8538	PI3 MTR PIA 01 H
	117	07	APR5	M8545	APR5 WR PT SEL 1 H
	117	08	APR5	M8545	APR5 PT WR L
	117	09	APR3	M8545	APR3 EBUS DEMAND H
	117	10	APR3	M8545	APR3 EBOX SEND F02 H
	117	11	CON5	M8545	CON FM WRITE PAR L
	117	12	APR6	M8545	APR6 EBOX EBR H
	117	13	APR6	M8545	APR6 EBOX SPARE H
	117	20	MTR5	M8538	MTR5 VECTOR REQ H
	117	21	MTR5	M8538	MTR5 INCR SEL 2 H
	117	22	MTR5	M8538	MTR5 INCR SEL 1 H
	117	25	MTR3	M8538	MTR CONO MTR, L
**	120	00	EDP1	M8512	EDP AR 00 H
**	120	01	EDP1	M8512	EDP AR 01 H
**	120	02	EDP1	M8512	EDP AR 02 H
**	120	03	EDP1	M8512	EDP AR 03 H
**	120	04	EDP1	M8512	EDP AR 04 H
**	120	05	EDP1	M8512	EDP AR 05 H
**	120	06	EDP1	M8512	EDP AR 06 H
**	120	07	EDP1	M8512	EDP AR 07 H
**	120	08	EDP1	M8512	EDP AR 08 H
**	120	09	EDP1	M8512	EDP AR 09 H
**	120	10	EDP1	M8512	EDP AR 10 H
**	120	11	EDP1	M8512	EDP AR 11 H
*	120	12-35	EDP1	M8512	AR 12 TO 35 H
*	121	0-35	EDP4	M8512	BR 0 TO 35 H
*	122	0-35	EDP2	M8512	MQ 0 TO 35 H
*	123	0-35	EDP4	M8512	FM 0 TO 35 H
*	124	0-35	EDP4	M8512	BRX 0 TO 35 H
*	125	0-35	EDP2	M8512	ARX 0 TO 35 H
*	126	0-35	EDP3	M8512	ADX 0 TO 35 H
*	127	0-35	EDP3	M8512	AD 0 TO 35 H
	130	02	SCD4	M8524	SCD TRAP REQ 2 H
	130	03	SCD4	M8524	SCD TRAP CYC 2 H
	130	04	SCD4	M8524	SCD TRAP CYC 1 H
	130	05	SCD4	M8524	SCD TRAP REQ 1 H
	130	06	SCD4	M8524	SCD FPD H
**	130	07	SCD2	M8524	SC 05 H
**	130	08	SCD2	M8524	SC 06 H
**	130	09	SCD2	M8524	SC 07 H
**	130	10	SCD2	M8524	SC 08 H
**	130	11	SCD2	M8524	SC 09 H
	130	12	IRD3	M8522	IR NORM 08 H
	130	13	IRD3	M8522	IR NORM 09 H
	130	14	IRD3	M8522	IR NORM 10 H
**	130	15	IRD1	M8522	DR ADR 00 A H
**	130	16	IRD1	M8522	DR ADR 01 A H
**	130	17	IRD1	M8522	DR ADR 02 A H
	130	18	CON3	M8525	CON WR EVEN PAR ADR H
	130	19	CON3	M8525	CON3 WR EVEN PAR DATA H
	130	20	CON3	M8525	CON3 WR EVEN PAR DIR H
	131	02	SCD4	M8524	SCD OV H
	131	03	SCD4	M8524	SCD CRY0 H
	131	04	SCD4	M8524	SCD CRY1 H
	131	05	EDP3	M8524	AD CRY 01 L
	131	06	SCD4	M8524	SCD DIV CHK H
**	131	07	SCD2	M8524	SC 00 H
**	131	08	SCD2	M8524	SC 01 H
**	131	09	SCD2	M8524	SC 02 H
**	131	10	SCD2	M8524	SC 03 H
**	131	11	SCD2	M8524	SC 04 H
**	131	12	IRD1	M8522	DR ADR 03 A H
**	131	13	IRD1	M8522	DR ADR 04 A H
**	131	14	IRD1	M8522	DR ADR 05 A H
**	131	15	IRD1	M8522	DR ADR 06 A H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION (Cont) CODES SORTED NUMERICALLY

	DF	BIT	DRAWING BOARD		NAME AND TRUTH
**	131	16	IRD1	M8522	DR ADR 07 A H
**	131	17	IRD1	M8522	DR ADR 08 A H
	131	18	CON3	M8525	CON3 CACHE LOOK EN H
	131	19	CON3	M8525	CON CACHE LOAD EN H
	131	21	CON3	M8525	CON KI10 PAGING MODE L
	131	22	CON3	M8525	CON TRAP EN H
	132	02	SCD4	M8524	VMA HELD OR PC 00 H
	132	03	SCD4	M8524	SCD FOV H
	132	04	SCD4	M8524	SCD FXU H
	132	05	EDP3	M8524	AD OVERFLOW 00 L
	132	06	IRD4	M8524	AD CRY -02 A L
**	132	07	SCD2	M8524	FE 05 H
**	132	08	SCD2	M8524	FE 06 H
**	132	09	SCD2	M8524	FE 07 H
**	132	10	SCD2	M8524	FE 08 H
**	132	11	SCD2	M8524	FE 09 H
	132	12	IRD3	M8522	IR EN I/O, JRST H
	132	13	IRD3	M8522	IR EN AC H
**	132	14	IRD1	M8522	IR AC 09 H
**	132	15	IRD1	M8522	IR AC 10 H
**	132	16	IRD1	M8522	IR AC 11 H
**	132	17	IRD1	M8522	IR AC 12 H
	132	18	CON1	M8525	CON COND EN 00-07 L
	132	19	CON1	M8525	CON COND/SEL VMA L
	132	20	CON1	M8525	CON COND/MBOX CTL L
	132	21	CON2	M8525	CON LONG EN L
	132	22	CON2	M8525	CON LOAD IR L
	132	23	CON4	M8525	CON4 AR LOADED H
	132	24	CON5	M8525	CON5 PI CYCLE H
	133	02	SCD4	M8524	SCD PCP H
	133	03	SCD5	M8524	SCD LOAD FLAGS A H
	133	04	SCD1	M8524	SCAD=0 L
	133	05	CON2	M8524	CON CLR PRIVATE INSTR H
	133	06	SCD4	M8524	SCD NICOND 10 H
**	133	07	SCD2	M8524	FE 00 H
**	133	08	SCD2	M8524	FE 01 H
**	133	09	SCD2	M8524	FE 02 H
**	133	10	SCD2	M8524	FE 03 H
**	133	11	SCD2	M8524	FE 04 H
**	133	12	IRD1	M8522	DRAM A 00 H
**	133	13	IRD1	M8522	DRAM A 01 H
**	133	14	IRD1	M8522	DRAM A 02 H
**	133	15	IRD1	M8522	DRAM B 00 H
**	133	16	IRD1	M8522	DRAM B 01 H
**	133	17	IRD1	M8522	DRAM B 02 H
	133	18	CON1	M8525	CON SKIP EN 40-47 L
	133	19	CON1	M8525	CON COND/VMA GETS # H
	133	20	CON3	M8525	CON EBUS REL H
	133	21	CON4	M8525	CON PC+1 INH L
	133	22	CON2	M8525	CON COND INSTR ABORT H
	133	23	CON4	M8525	CON ARX LOADED L
	133	24	CON5	M8525	CON5 MEM CYCLE L
	134	02	SCD5	M8524	SCD USER A L
	134	03	SCD5	M8524	SCD LEAVE USER H
	134	04	CON5	M8524	CON PI CYCLE A L
	134	05	SCD5	M8524	SCD USER EN L
	134	06	SCD5	M8524	SCD PUBLIC PAGE H
	134	07	SCD2	M8524	SC SIGN H
	134	12	IRD3	M8522	TEST SATISFIED H
	134	13	IRD3	M8522	IR JRST 0, L
**	134	14	IRD1	M8522	DRAM J 01 H
**	134	15	IRD1	M8522	DRAM J 02 H
**	134	16	IRD1	M8522	DRAM J 03 H
**	134	17	IRD1	M8522	DRAM J 04 H
	134	18	CON1	M8525	CON SKIP EN 50-57 L
	134	19	CON1	M8525	CON COND/LOAD VMA HELD H
	134	20	CON3	M8525	CON SR 00 H
	134	21	CON2	M8525	CON NICOND TRAP EN H
	134	22	CON2	M8525	CON LOAD ACCESS COND H
	134	23	CON4	M8525	CON UCODE STATE 01 H
	134	24	CON5	M8525	CON FM WRITE PAR L
	134	34	XCD1	M8572	CP CLK SEL 2 L
	134	35	XCD1	M8572	CP CLK SEL 1 L
	135	02	SCD5	M8524	SCD PUBLIC EN L
	135	03	SCD5	M8524	SCD PUBLIC A H
	135	04	SCD5	M8524	SCD KERNEL MODE H
	135	05	SCD5	M8524	SCD PRIVATE INSTR L
	135	06	SCD5	M8524	SCD PRIVATE INSTR EN L
	135	07	SCD2	M8524	FE SIGN H
**	135	12	IRD1	M8522	DRAM PAR H
	135	13	IRD3	M8522	DRAM ODD PARITY H
**	135	14	IRD1	M8522	DRAM J 07 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION (Cont) CODES SORTED NUMERICALLY

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	135	15	IRD1	M8522	DRAM J 08 H
**	135	16	IRD1	M8522	DRAM J 09 H
**	135	17	IRD1	M8522	DRAM J 10 H
	135	18	CON3	M8525	CON DELAY REQ H
	135	19	CON1	M8525	CON LOAD SPEC INSTR L
	135	20	CON3	M8525	CON SR 01 H
	135	21	CON2	M8525	CON NICOND 07 H
	135	22	CON2	M8525	CON2 INSTR GO L
	135	23	CON4	M8525	CON UCODE STATE 03 H
	135	24	CON5	M8525	CON MBOX WAIT L
	136	02	SCD5	M8524	SCD KERNEL OR USER IOT H
**	136	03	SCD3	M8524	SCD TRAP MIX 32 H
**	136	04	SCD3	M8524	SCD TRAP MIX 33 H
	136	05	SCD5	M8524	SCD USER IOT A H
	136	06	SCD5	M8524	SCD USER IOT EN L
	136	07	SCD2	M8524	SC .GE. 36 H
	136	12	IRD3	M8522	AD=0 L
	136	13	IRD1	M8522	IR I/O LEGAL H
	136	14	CTL1	M8522	CTL INH CRY 18 L
	136	15	CTL1	M8522	CTL SPEC/GEN CRY 18 H
	136	16	IRD4	M8522	GEN CRY 36 H
	136	17	IRD4	M8522	AD CRY -02 A H
	136	18	CON4	M8525	CON AR 36 H
	136	19	CON1	M8525	CON VMA SEL 2 L
	136	20	CON3	M8525	CON SR 02 H
	136	21	CON2	M8525	CON NICOND 08 H
	136	22	CON2	M8525	CON LOAD DRAM H
	136	23	CON4	M8525	CON UCODE STATE 05 H
	136	24	CON5	M8525	CON FM XFER L
	137	02	SCD5	M8524	SCD ADR BRK INH H
**	137	03	SCD3	M8524	SCD TRAP MIX 34 H
**	137	04	SCD3	M8524	SCD TRAP MIX 35 H
	137	05	SCD5	M8524	SCD ADR BRK CYC H
	137	06	SCD5	M8524	SCD ADR BREAK PREVENT H
	137	07	SCD4	M8524	SCD TRAP CLEAR L
	137	12	IRD4	M8522	AD CRY 12 H
	137	13	IRD4	M8522	AD CRY 18 H
	137	14	IRD4	M8522	AD CRY 24 H
	137	15	IRD4	M8522	AD CRY 36 H
	137	16	IRD4	M8522	ADX CRY 12 H
	137	17	IRD4	M8522	ADX CRY 24 H
	137	18	CON4	M8525	CON ARX 36 H
	137	19	CON1	M8525	CON VMA SEL 1 L
	137	20	CON3	M8525	CON SR 03 H
	137	21	CON2	M8525	CON NICOND 09 H
	137	22	CON2	M8525	CON COND ADR 10 H
	137	23	CON4	M8525	CON UCODE STATE 07 H
	137	24	CON5	M8525	CON PI DISMISS L
	140	00	CRA3	M8541	CRA DISP EN 00-07 L
	140	01	CRA3	M8541	CRA DISP EN 00-03 L
**	140	02	CRA4	M8541	CRA STACK ADR 10 H
**	140	03	CRA4	M8541	CRA STACK ADR 04 H
**	140	04	CRA4	M8541	CRA STACK ADR 02 H
**	140	05	CRA4	M8541	CRA STACK ADR 01 H
**	141	00	CRA4	M8541	CRA CALL, RESET H
**	141	01	CRA3	M8541	CRA DISP 00 H
**	141	02	CRA3	M8541	CRA DISP 01 H
**	141	03	CRA3	M8541	CRA DISP 02 H
**	141	04	CRA3	M8541	CRA DISP 03 H
**	141	05	CRA3	M8541	CRA DISP 04 H
**	142	00	CRA4	M8541	CRA SBR RET 05 H
**	142	01	CRA4	M8541	CRA SBR RET 06 H
**	142	02	CRA4	M8541	CRA SBR RET 07 H
**	142	03	CRA4	M8541	CRA SBR RET 08 H
**	142	04	CRA4	M8541	CRA SBR RET 09 H
**	142	05	CRA4	M8541	CRA SBR RET 10 H
	143	00	CRA3	M8541	CRA DISP EN 30-37 L
**	143	01	CRA4	M8541	CRA SBR RET 00 H
**	143	02	CRA4	M8541	CRA SBR RET 01 H
**	143	03	CRA4	M8541	CRA SBR RET 02 H
**	143	04	CRA4	M8541	CRA SBR RET 03 H
**	143	05	CRA4	M8541	CRA SBR RET 04 H
**	144	00	CRA1	M8541	CR ADR 05 F H
**	144	01	CRA1	M8541	CR ADR 06 F H
**	144	02	CRA2	M8541	CR ADR 07 F H
**	144	03	CRA2	M8541	CR ADR 08 F H
**	144	04	CRA2	M8541	CR ADR 09 F H
**	144	05	CRA2	M8541	CR ADR 10 F H
**	144	08	CRM5	M8548	CRAM 60 H
**	144	09	CRM5	M8548	CRAM PAR 1ST 00 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	144	10	CRM5	M8548	CRAM 62 H
**	144	11	CRM5	M8548	CRAM PAR 00 H
**	144	14	CRM5	M8548	CRAM 64 H
**	144	15	CRM5	M8548	CRAM PAR 1ST 04 H
**	144	16	CRM5	M8548	CRAM 66 H
**	144	17	CRM5	M8548	CRAM PAR 04 H
**	144	20	CRM5	M8548	CRAM 68 H
**	144	21	CRM5	M8548	CRAM PAR 1ST 08 H
**	144	22	CRM5	M8548	CRAM 70 H
**	144	23	CRM5	M8548	CRAM PAR 08 H
**	144	26	CRM5	M8548	CRAM 72 H
**	144	27	CRM5	M8548	CRAM PAR 1ST 12 H
**	144	28	CRM5	M8548	CRAM 74 H
**	144	29	CRM5	M8548	CRAM PAR 12 H
**	144	32	CRM5	M8548	CRAM 76 H
**	144	33	CRM5	M8548	CRAM PAR 1ST 16 H
**	144	34	CRM5	M8548	CRAM 78 H
**	144	35	CRM5	M8548	CRAM PAR 16 H
**	145	00	CRA3	M8541	CRA DISP PARITY H
**	145	01	CRA1	M8541	CR ADR 00 F H
**	145	02	CRA1	M8541	CR ADR 01 F H
**	145	03	CRA1	M8541	CR ADR 02 F H
**	145	04	CRA1	M8541	CR ADR 03 F H
**	145	05	CRA1	M8541	CR ADR 04 F H
*	145	08-11	CRM5	M8548	CRAM 40-43 H
*	145	14-17	CRM5	M8548	CRAM 44-47 H
*	145	20-23	CRM5	M8548	CRAM 48-51 H
*	145	26-29	CRM5	M8548	CRAM 52-55 H
*	145	32-35	CRM5	M8548	CRAM 56-59 H
**	146	00	CRA3	M8541	CRA LOC 05 H
**	146	01	CRA3	M8541	CRA LOC 06 H
**	146	02	CRA3	M8541	CRA LOC 07 H
**	146	03	CRA3	M8541	CRA LOC 08 H
**	146	04	CRA3	M8541	CRA LOC 09 H
**	146	05	CRA3	M8541	CRA LOC 10 H
*	146	08-11	CRM5	M8548	CRAM 20-23 H
*	146	14-17	CRM5	M8548	CRAM 24-27 H
*	146	20-23	CRM5	M8548	CRAM 28-31 H
*	146	26-29	CRM5	M8548	CRAM 32-35 H
*	146	32-35	CRM5	M8548	CRAM 36-39 H
**	147	01	CRA3	M8541	CRA LOC 00 H
**	147	02	CRA3	M8541	CRA LOC 01 H
**	147	03	CRA3	M8541	CRA LOC 02 H
**	147	04	CRA3	M8541	CRA LOC 03 H
**	147	05	CRA3	M8541	CRA LOC 04 H
*	147	08-11	CRM5	M8548	CRAM 00-03 H
*	147	14-17	CRM5	M8548	CRAM 04-07 H
*	147	20-23	CRM5	M8548	CRAM 08-11 H
*	147	26-29	CRM5	M8548	CRAM 12-15 H
*	147	32-35	CRM5	M8548	CRAM 16-19 H

NOTE ABOUT READING VMA BOARD REGISTERS

THESE FORMULAS TERSELY DESCRIBE THE DIAGNOSTIC FUNCTION (150-157) AND EBUS BIT NUMBER (13-35, ODD) CORRESPONDING TO A REGISTER BIT 'B'.
[] MEANS "THE INTEGER PART OF THE QUOTIENT"
REM() MEANS "THE REMAINDER OF"

	FORMULA FOR:	
REGISTER	DIAG FUNC	EBUS BIT
ADR BRK	153-REM(B/4)	4*[B/4]+3
PC	DITTO	4*[B/4]+1
VMA	157-REM(B/4)	4*[B/4]+3
VMA HELD	DITTO	4*[B/4]+1

BETTER YET--SEE THE PRINTS!

	150	11	VMA1	M8542	VMA1 VMA SECTION 0 L
	151	11	VMA3	M8542	VMA3 PC SECTION 0 L
	152	11	VMA4	M8542	VMA4 PCS SECTION 0 L
**	153	11	VMA4	M8542	VMA PREV SEC 17 H
	153	13	VMA1	M8542	VMA1 MISC=0 L
	153	15	VMA1	M8542	VMA1 LOCAL AC ADDRESS L
**	154	11	VMA4	M8542	VMA PREV SEC 16 H
**	155	11	VMA4	M8542	VMA PREV SEC 15 H
**	156	11	VMA4	M8542	VMA PREV SEC 14 H
**	157	11	VMA4	M8542	VMA PREV SEC 13 H
	157	13	VMA1	M8542	VMA1 AC REF A L
	157	15	VMA3	M8542	VMA3 MATCH 13-35 H

KL10 (PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
*	15X	13-35	VMA3	M8542	ADR BRK 13-35 H **NOTE
*	15X	13-35	VMA4	M8542	VMA HELD 13-35 H **NOTE
*	15X	13-35	VMA2	M8542	VMA 13-35 H **NOTE
*	15X	13-35	VMA3	M8542	PC 13-35 H **NOTE
	160	15	MBZ1	M8537	CORE BUSY H
	160	16	MBZ4	M8537	CHAN PAR ERR L
	160	17	SHD1	M8537	SH AR PAR ODD A H
	160	18	MBZ5	M8537	MB PAR BIT IN H
	160	19	MBZ1	M8537	CSH EN CSH DATA L
	160	20	MBZ1	M8537	MB IN SEL 1 H
	160	21	MBZ3	M8537	NXM ACKN H
	160	22	MBZ1	M8537	MBZ1 CHAN CORE BUSY H
	160	23	MBZ3	M8537	NXM ANY L
	160	24	MBZ4	M8537	MBZ4 NXM T6,7 L
	160	25	MBZ3	M8537	CHAN NXM ERR L
	160	26	PAG5	M8537	PAG MB 18-35 PAR H
NOTE	160	27	MBC5	M8531YA	FORCE VALID MATCH 0 H
NOTE	160	28	MBC5	M8531YA	FORCE VALID MATCH 1 H
NOTE	160	29	MBC5	M8531YA	FORCE VALID MATCH 2 H
NOTE	160	30	MBC5	M8531YA	FORCE VALID MATCH 3 H
NOTE	160	31	MBC1	M8531YA	MBC1 WRITE OK H
NOTE	160	32	MBC2	M8531YA	MBC2 CSH ADR WR PULSE H
NOTE	160	33	MBC2	M8531YA	MBC2 CSH DATA CLR DONE IN L
	161	15	MBZ4	M8537	MBOX ADR PAR ERR L
	161	16	MBZ5	M8537	CBUS PAR LEFT TE H
	161	17	MEM5	M8537	MEM PAR IN H
	161	18	MBZ6	M8537	MBZ6 CSH PAR BIT H
	161	19	MBZ1	M8537	MEM TO C DIAG EN L
	161	20	MBZ1	M8537	MB IN SEL 2 H
	161	21	MBZ1	M8537	MBZ1 RD-PSE-WR REF L
	161	22	MBZ3	M8537	MBOX NXM ERR L
	161	23	MBZ3	M8537	MBZ3 CHAN MEM REF L
	161	24	MBZ4	M8537	MBOX SBUS ERR L
	161	25	MBZ3	M8537	NXM DATA VAL L
	161	26	MBZ6	M8537	CSH PAR BIT A H
NOTE	161	27	MBC2	M8531YA	MBC2 CSH DATA CLR T1 L
NOTE	161	28	MBC2	M8531YA	MBC2 CSH DATA CLR T2 L
NOTE	161	29	MBC2	M8531YA	MBC2 CSH DATA CLR T3 L
NOTE	161	30	MBC2	M8531YA	CSH SEL LRU H
NOTE	161	31	MBC2	M8531YA	MBC2 CSH VAL WR PULSE H
NOTE	161	32	MBC2	M8531YA	MBC2 CSH WR WR PULSE H
NOTE	161	33	MBC2	M8531YA	RQ HOLD FF H
	162	15	MBZ4	M8537	CHAN ADR PAR ERR L
	162	16	MBZ5	M8537	CBUS PAR RIGHT TE H
	162	17	MBZ5	M8537	CSH PAR BIT IN H
	162	18	MBZ3	M8537	MBZ3 SEQUENTIAL RQ H
	162	19	MBZ1	M8537	CHAN READ L
	162	20	MBZ1	M8537	MB IN SEL 4 H
	162	21	MBZ1	M8537	MEM BUSY H
	162	22	MBZ3	M8537	MBZ3 HOLD ERA L
	162	23	MBZ4	M8537	MBZ4 NXM T2 H
	162	24	MBZ4	M8537	MBOX MB PAR ERR L
	162	25	PAG5	M8537	PAG MB 00-17 PAR H
	162	26	MBZ6	M8537	CSH PAR BIT B H
NOTE	162	27	MBC2	M8531YA	MBC2 CACHE WR 00 A H
NOTE	162	28	MBC2	M8531YA	MBC2 CACHE WR 09 A H
NOTE	162	29	MBC2	M8531YA	MBC2 CACHE WR 18 A H
NOTE	162	30	MBC2	M8531YA	MBC2 CACHE WR 27 A H
NOTE	162	31	MBC2	M8531YA	SBUS ADR HOLD H
NOTE	162	32	MBC3	M8531YA	MBC3 A CHANGE COMING A L
NOTE	162	33	MBC3	M8531YA	MBC3 ANY SBUS RQ IN L
NOTE	163	27	MBC3	M8531YA	MBC3 B CHANGE COMING L
NOTE	163	28	MBC5	M8531YA	MBC5 CORE BUSY B H
NOTE	163	29	MBC3	M8531YA	CSH VAL SEL ALL H
NOTE	163	30	MBC3	M8531YA	CSH VAL WR DATA H
NOTE	163	31	MBC3	M8531YA	CSH WR SEL ALL H
NOTE	163	32	MBC3	M8531YA	CSH WR WR DATA H
NOTE	163	33	MBC3	M8531YA	DATA VALID A OUT H
NOTE	164	27	MBC3	M8531YA	DATA VALID B OUT H
NOTE	164	28	MBC3	M8531YA	MBC3 INH 1ST MB REQ H
NOTE	164	29	MBC3	M8531YA	MEM TO C EN L
NOTE	164	30	MBC3	M8531YA	PHASE CHANGE COMING L
NOTE	164	31	MBC4	M8531YA	ACKN PULSE L
NOTE	164	32	MBC4	M8531YA	MBC4 CORE ADR 34 H
NOTE	164	33	MBC4	M8531YA	MBC4 CORE ADR 35 H
NOTE	165	27	MBC1	M8531YA	CAM SEL 1 H
NOTE	165	28	MBC1	M8531YA	CAM SEL 2 H
NOTE	165	29	MBC4	M8531YA	MBC4 CORE DATA VAL -1 L
NOTE	165	30	MBC4	M8531YA	MBC4 CORE DATA VALID -2 L

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
NOTE	165	31	MBC4	M8531YA	MBC4 CORE DATA VALID L
NOTE	165	32	MBC4	M8531YA	MBC4 CORE RD IN PROG A H
NOTE	165	33	MBC4	M8531YA	MEM ADR PAR H
NOTE	166	27	MBC4	M8531YA	MEM RD RQ B H
NOTE	166	28	MBC4	M8531YA	MEM RQ 0 H
NOTE	166	29	MBC4	M8531YA	MEM RQ 1 H
NOTE	166	30	MBC4	M8531YA	MEM RQ 2 H
NOTE	166	31	MBC4	M8531YA	MEM RQ 3 H
NOTE	166	32	MBC4	M8531YA	MBC4 MEM START L
NOTE	166	33	MBC4	M8531YA	MEM WR RQ L
*	167	00-08	MBZ2	M8537	EBUS REG 00-08 H
*	167	14-26	MBZ2	M8537	EBUS REG 14-26 H
NOTE	167	27-33	MBC1	M8531YA	EBUS REG 27-33 H
*	167	34,35	MBZ2	M8537	EBUS REG 34,35 H
**	170	00	CRC6	M8535	CRC CH BUF ADR 0 H
	170	01	CRC4	M8535	CRC4 RESET IN L
	170	02	CRC4	M8535	CRC MEM STORE ENA L
	170	03	CRC4	M8535	CRC4 DONE IN H
	170	04	CRC4	M8535	CRC4 STORE IN H
	170	05	CCW4	M8534	CCW WD READY H
	170	06	CCW6	M8534	CCW CCWF REQ ENA H
	170	07	CCW6	M8534	CCW MEM STORE ENA H
	170	08	CCW5	M8534	CCW ACT FLAG REQ ENA H
	170	09	CCW3	M8534	CCW ALU C8 OUT H
	170	10	CCW3	M8534	CCW ALU C2 OUT H
	170	11	CHC1	M8533	CH T0 H
	170	12	CHC5	M8533	CBUS SEL 0 E H
	170	13	CHC1	M8533	CHX RESET H
	170	14	CHC2	M8533	CH RESET INTR H
	170	16	CCL5	M8536	CCL ODD WC PAR H
	170	18	CCL5	M8536	CCL5 WC GE4 H
	170	19	CCL5	M8536	CCL WC=0 L
NOTE	170	20	CHX2	M8515	CSH 0 ANY VAL L
NOTE	170	21	CHX3	M8515	CSH USE IN 0 H
	170	22	CSH5	M8513YA	CSH5 PAGE REFILL COMP L
	170	23	CSH6	M8513YA	CSH6 CACHE WR IN H
	170	24	CSH6	M8513YA	CSH6 MBOX PT DIR WR L
	170	25	CSH2	M8513YA	CSH2 WR TEST L
	170	26	CSH3	M8513YA	CSH3 ANY VAL HOLD H
	170	27	CSH4	M8513YA	CSH4 DATA CLR DONE L
	170	28	CSH4	M8513YA	CSH REFILL RAM WR L
	170	29	CSH4	M8513YA	CSH4 EBOX T3 L
	170	30	MBX1	M8529YA	MBX1 CACHE BIT H
	170	31	MBX1	M8529YA	MBX1 CCA REQ L
	170	32	MBX4	M8529YA	CSH WR WD 2 EN H
	170	33	MBX5	M8529YA	MBX5 MB REQ IN H
	170	34	MBX5	M8529YA	MBX5 MEM TO C EN L
	170	35	MBX5	M8529YA	MBX5 RQ 1 IN H
**	171	00	CRC6	M8535	CRC CH BUF ADR 1 H
	171	01	CRC4	M8535	CRC RH20 ERR IN H
	171	02	CRC4	M8535	CRC OVN ERR IN H
	171	03	CRC4	M8535	CRC SHORT WC ERR H
	171	04	CRC4	M8535	CRC LONG WC ERR H
	171	05	CCW4	M8534	CCW WD0 REQ H
	171	06	CCW4	M8534	CCW WD1 REQ H
	171	07	CCW4	M8534	CCW WD2 REQ H
	171	08	CCW4	M8534	CCW WD3 REQ H
	171	09	CCW1	M8534	CCW MEM ADR=0 H
	171	10	CCW6	M8534	CCW CCWF WAITING H
	171	11	CHC1	M8533	CH T1 H
	171	12	CHC5	M8533	CBUS SEL 1 E H
	171	13	CHC1	M8533	CHX START H
	171	14	CHC2	M8533	CH START INTR H
	171	16	CCL3	M8536	CCL3 MB RIP A H
	171	18	CCL3	M8536	CCL ALU MINUS L
	171	19	CCL4	M8536	CCL CH TEST MB PAR L
NOTE	171	20	CHX2	M8515	CSH 1 ANY VAL L
NOTE	171	21	CHX3	M8515	CSH USE IN 1 H
	171	22	CSH5	M8513YA	CSH5 CHAN RD T5 L
	171	23	CSH6	M8513YA	CSH6 WR DATA RDY L
	171	24	CSH4	M8513YA	CSH4 PAGE FAIL T2 L
	171	25	CSH6	M8513YA	CSH6 EBOX LOAD REG H
	171	26	CSH7	M8513YA	CSH7 FILL CACHE RD L
	171	27	CSH5	M8513YA	CSH5 CHAN WR T5 L
	171	28	CSH3	M8513YA	CSH3 MB WR RQ CLR NXT L
	171	29	CSH4	M8513YA	CSH4 EBOX T1 L
	171	30	MBX2	M8529YA	MBX2 CACHE TO MB 34 H
	171	31	MBX1	M8529YA	MBX1 CCA SEL 1 H
	171	32	MBX4	M8529YA	CSH WR WD 3 EN H
	171	33	MBX2	M8529YA	MB SEL 1 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	171	34	MBX3	M8529YA	MEM DIAG L
	171	35	MBX5	M8529YA	MBX5 RQ 2 IN H
**	172	00	CRC6	M8535	CRC CH BUF ADR 2 H
	172	01	CRC3	M8535	CRC READY IN H
	172	02	CRC3	M8535	CRC LAST WORD IN H
	172	03	CRC3	M8535	CRC ERR IN H
	172	04	CRC3	M8535	CRC REVERSE IN H
	172	05	CCW3	M8534	CCW ACT CTR 0 EN H
	172	06	CCW3	M8534	CCW ACT CTR 1 EN H
	172	07	CCW3	M8534	CCW ACT CTR 2 EN H
	172	08	CCW1	M8534	CCW BUF ADR 0 L
	172	09	CCW1	M8534	CCW BUF ADR 1 L
	172	10	CCW1	M8534	CCW BUF ADR 2 L
	172	11	CHC1	M8533	CH T2 H
	172	12	CHC5	M8533	CBUS SEL 2 E H
	172	13	CHC1	M8533	CHX DONE H
	172	14	CHC2	M8533	CH DONE INTR H
	172	16	CCL3	M8536	CCL3 CCWF T2 H
	172	18	CCL3	M8536	CCL3 MB REQ T2 H
	172	19	CCL4	M8536	CCL4 REVERSE H
NOTE	172	20	CHX2	M8515	CSH 2 ANY VAL L
NOTE	172	21	CHX3	M8515	CSH USE IN 2 H
	172	22	CSH6	M8513YA	CSH6 CHAN WR CACHE L
	172	23	CSH6	M8513YA	CSH6 CCA CYC DONE L
	172	24	CSH5	M8513YA	CSH5 CHAN T4 L
	172	25	CHX3	M8513YA	CSH LRU 2 H
	172	26	CSH1	M8513YA	CSH1 READY TO GO A H
	172	27	CSH6	M8513YA	CSH USE HOLD H
	172	28	CSH1	M8513YA	CSH1 CCA CYC L
	172	29	CSH2	M8513YA	CSH2 EBOX REQ EN L
	172	30	MBX2	M8529YA	MBX2 CACHE TO MB 35 H
	172	31	MBX1	M8529YA	MBX1 CCA SEL 2 H
	172	32	MBX1	M8529YA	FORCE NO MATCH H
	172	33	MBX2	M8529YA	MB SEL 2 H
	172	34	MBX5	M8529YA	MBX5 MEM RD RQ IN H
	172	35	MBX5	M8529YA	MBX5 RQ 3 IN H
**	173	00	CRC6	M8535	CRC CH BUF ADR 3 H
	173	01	CRC2	M8535	CRC2 ACT CTR 0R H
	173	02	CRC2	M8535	CRC2 ACT CTR 1R H
	173	03	CRC2	M8535	CRC2 ACT CTR 2R H
	173	04	CRC2	M8535	CRC2 RAM CYC H
**	173	05	CCW2	M8534	CCW CHA 30 H
**	173	06	CCW2	M8534	CCW CHA 31 H
**	173	07	CCW2	M8534	CCW CHA 32 H
**	173	08	CCW2	M8534	CCW CHA 33 H
**	173	09	CCW2	M8534	CCW CHA 34 H
**	173	10	CCW2	M8534	CCW CHA 35 H
	173	11	CHC1	M8533	CH T3 H
	173	12	CHC5	M8533	CBUS SEL 3 E H
	173	13	CHC1	M8533	CHX STORE H
	173	14	CHC2	M8533	CH STORE H
	173	16	CCL4	M8536	CCL CH MB SEL 2 H
	173	18	CCL4	M8536	CCL CH MB SEL 1 H
	173	19	CCL3	M8536	CCL AF T2 L
NOTE	173	20	CHX2	M8515	CSH 3 ANY VAL L
NOTE	173	21	CHX3	M8515	CSH USE IN 3 H
	173	22	CSH2	M8513YA	CSH2 ONE WORD RD A L
	173	23	CSH2	M8513YA	CSH2 MBOX RESP L
	173	24	CSH2	M8513YA	CSH2 RD PSE 2ND REQ EN L
	173	25	CHX3	M8513YA	CSH LRU 1 H
	173	26	CSH5	M8513YA	CSH5 T1 L
	173	27	CSH4	M8513YA	CSH4 WRITEBACK T1 A H
	173	28	CSH7	M8513YA	CSH7 CCA WRITEBACK L
	173	29	CSH4	M8513YA	CSH4 EBOX T2 L
	173	30	MBX4	M8529YA	MBX4 CACHE TO MB DONE H
	173	31	MBX2	M8529YA	MBX2 CHAN WR CYC L
	173	32	MBX3	M8529YA	MEM DATA TO MEM H
	173	33	MBX2	M8529YA	MB SEL HOLD H
	173	34	MBX3	M8529YA	MEM TO C SEL 1 H
	173	35	MBX2	M8529YA	SBUS ADR 34 H
**	174	00	CRC6	M8535	CRC CH BUF ADR 4 H
	174	01	CRC1	M8535	CRC1 ACT FLAG ENA H
	174	02	CRC5	M8535	CRC WR RAM L
	174	03	CRC3	M8535	CRC3 OP CODE 00 H
	174	04	CRC3	M8535	CRC3 OP CODE 01 H
*	174	05-10	CCW2	M8534	CCW CHA 24-29 H
	174	11	CHC1	M8533	CBUS READY E H
	174	12	CHC5	M8533	CBUS SEL 4 E H
	174	13	CHC1	M8533	CHX CTOM H
	174	14	CHC3	M8533	CH CTOM H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION (Cont) CODES SORTED NUMERICALLY

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	174	16	CCL3	M8536	CCL CHAN REQ H
	174	18	CCL3	M8536	CCL CHAN EPT H
	174	19	CCL4	M8536	CCL CHAN TO MEM H
NOTE	174	20	CHX4	M8515	CSH DIR 0 PAR ODD H
NOTE	174	21	CHX3	M8515	CSH USE IN 4 H
	174	22	CSH2	M8513YA	CSH2 E CORE RD RQ A L
	174	23	CSH6	M8513YA	CSH6 PAGE FAIL HOLD L
	174	24	CSH5	M8513YA	CSH5 PAGE REFILL T9,12 L
	174	25	CHA3	M8513YA	CSH 3 ANY WR L
	174	26	CSH5	M8513YA	CSH5 CSH T0 L
	174	27	CSH3	M8513YA	CSH3 ADR PMA EN H
	174	28	CSH1	M8513YA	CSH1 EBOX CYC B L
	174	29	CSH1	M8513YA	CSH1 CACHE IDLE L
	174	30	MBX4	M8529YA	MBX4 CACHE TO MB T2 L
	174	31	MBX1	M8529YA	MBX1 CSH CCA INVAL CSH H
	174	32	MBX3	M8529YA	MB DATA CODE 1 H
	174	33	MBX6	M8529YA	MB0 HOLD IN H
	174	34	MBX3	M8529YA	MEM TO C SEL 2 H
	174	35	MBX2	M8529YA	SBUS ADR 35 H
**	175	00	CRC6	M8535	CRC CH BUF ADR 5 H
	175	01	CRC6	M8535	CRC SEL 1D L
	175	02	CRC6	M8535	CRC SEL 2D L
	175	03	CRC6	M8535	CRC SEL 4D L
	175	04	CRC1	M8535	CRC1 AF REQ ENA L
*	175	05-10	CCW2	M8534	CCW CHA 18-23 H
	175	11	CHC1	M8533	CBUS LAST WORD E H
	175	12	CHC5	M8533	CBUS SEL 5 E H
	175	13	CHC5	M8533	CH SEL 8A H
	175	14	CHC2	M8533	CH CONTR REQ H
	175	16	CCL2	M8536	CCL CCWF REQ H
	175	18	CCL2	M8536	CCL2 ACT FLAG REQ H
	175	19	CCL2	M8536	CCL MEM STORE REQ H
NOTE	175	20	CHX4	M8515	CSH DIR 1 PAR ODD H
NOTE	175	21	CHX3	M8515	CSH USE ADR 2 H
	175	22	CSH2	M8513YA	CSH2 EBOX RETRY REQ L
	175	23	CSH6	M8513YA	CSH USE WR EN H
	175	24	CSH3	M8513YA	MB TEST PAR A IN L
	175	25	CHA3	M8513YA	CSH 1 ANY WR L
	175	26	CSH5	M8513YA	CSH5 T3 L
	175	27	CSH3	M8513YA	CSH3 GATE VMA 27-33 H
	175	28	CSH1	M8513YA	CSH1 MB CYC L
	175	29	CSH4	M8513YA	CSH4 ONE WORD WR T0 L
	175	30	MBX4	M8529YA	MBX4 CACHE TO MB T3 L
	175	31	MBX1	M8529YA	MBX1 CSH CCA VAL CORE H
	175	32	MBX3	M8529YA	MB DATA CODE 2 H
	175	33	MBX6	M8529YA	MB1 HOLD IN H
	175	34	MBX5	M8529YA	MBX5 MEM WR RQ IN H
	175	35	MBX3	M8529YA	MBX3 SBUS DIAG 3 L
**	176	00	CRC6	M8535	CRC CH BUF ADR 6 H
	176	01	CRC1	M8535	CRC1 MEM PTR0 H
	176	02	CRC1	M8535	CRC1 MEM PTR1 H
	176	03	CRC1	M8535	CRC1 MEM PTR2 H
	176	04	CRC1	M8535	CRC1 MEM PTR3 H
	176	05	CCW3	M8534	CCL WC=3 H
	176	06	CCW4	M8534	CCL CCW REG LOAD H
*	176	07-10	CCW2	M8534	CCW CHA 14-17 H
	176	11	CHC1	M8533	CBUS ERROR E H
	176	12	CHC5	M8533	CBUS SEL 6 E H
	176	13	CHC1	M8533	CH MB REQ INH H
	176	14	CHC1	M8533	CH REVERSE H
	176	16	CCL4	M8536	CCL4 STORE CCW H
	176	18	CCL2	M8536	CCL BUF ADR 3 H
	176	19	CCL4	M8536	CCL START MEM L
NOTE	176	20	CHX4	M8515	CSH DIR 2 PAR ODD H
NOTE	176	21	CHX3	M8515	CSH USE ADR 3 H
	176	22	CSH6	M8513YA	CSH6 CCA INVAL T4 L
	176	23	CSH5	M8513YA	CSH5 PAGE REFILL T8 L
	176	24	CSH4	M8513YA	CSH4 EBOX T0 L
	176	25	CHA3	M8513YA	CSH 2 ANY WR L
	176	26	CSH5	M8513YA	CSH5 T2 L
	176	27	CSH2	M8513YA	CSH2 E CACHE WR CYC H
	176	28	CSH7	M8513YA	CSH7 E WRITEBACK L
	176	29	CSH5	M8513YA	CSH5 PAGE REFILL T4 L
	176	30	MBX4	M8529YA	MBX4 CACHE TO MB T4 A L
	176	31	MBX4	M8529YA	CSH WR WD 0 EN H
	176	32	MBX3	M8529YA	MB PAR H
	176	33	MBX6	M8529YA	MB2 HOLD IN H
	176	34	MBX3	M8529YA	MBX3 REFILL HOLD H
	176	35	MBX3	M8529YA	MBX3 SBUS DIAG CYC L
	177	00	CRC1	M8535	CRC1 PTR DIF=0 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED NUMERICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	177	01	CRC6	M8535	CRC6 CH ADR 0C L
	177	02	CRC6	M8535	CRC6 CH ADR 1C L
	177	03	CRC6	M8535	CRC6 CH ADR 2C L
	177	04	CRC6	M8535	CRC6 CH ADR 3C L
	177	05	CCW6	M8534	CCW RAM ADR 1 H
	177	06	CCW6	M8534	CCW RAM ADR 2 H
	177	07	CCW6	M8534	CCW RAM ADR 4 H
	177	08	CCW3	M8534	CCL WC=1 H
	177	09	CCW3	M8534	CCL WC=2 H
	177	10	CCW4	M8534	CCW ODD ADR PAR H
	177	11	CHC1	M8533	CH CBUS REQ H
	177	12	CHC5	M8533	CBUS SEL 7 E H
	177	13	CHC2	M8533	CH CONTR CYC H
	177	14	CHC2	M8533	CH START H
	177	16	CCL1	M8536	CCL1 ERR REQ H
	177	18	CCL6	M8536	CCL6 CSH CHAN CYC L
	177	19	CCL3	M8536	CCL3 MEM PTR EN H
NOTE	177	20	CHX4	M8515	CSH DIR 3 PAR ODD H
NOTE	177	21	CHX3	M8515	CSH USE ADR 4 H
	177	22	CSH6	M8513YA	CSH6 PAGE REFILL ERROR L
	177	23	CSH6	M8513YA	CSH6 DATA DLY 1 L
	177	24	CSH4	M8513YA	CSH4 PAGE FAIL DLY H
	177	25	CHA3	M8513YA	CSH 0 ANY WR L
	177	26	CSH5	M8513YA	CSH5 PAGE REFILL T10 L
	177	27	CSH1	M8513YA	CSH1 CYC TYPE HOLD H
	177	28	CSH2	M8513YA	CSH2 RD PAUSE 2ND HALF L
	177	29	CSH4	M8513YA	CSH4 EBOX WR T4 L
	177	30	MBX1	M8529YA	MBX1 CCA ALL PAGES CYC H
	177	31	MBX4	M8529YA	CSH WR WD 1 EN H
	177	32	MBX2	M8529YA	MB REQ HOLD H
	177	33	MBX6	M8529YA	MB3 HOLD IN H
	177	34	MBX5	M8529YA	MBX5 RQ 0 IN H
	177	35	MBX4	M8529YA	MBX4 WRITEBACK T2 L

NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(*) or (**)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (**) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES SORTED ALPHABETICALLY

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
NOTE	164	31	MBC4	M8531YA	ACKN PULSE L
*	127	0-35	EDP3	M8512	AD 0 TO 35 H
	136	17	IRD4	M8522	AD CRY -02 A H
	132	06	IRD4	M8524	AD CRY -02 A L
	131	05	EDP3	M8524	AD CRY 01 L
	137	12	IRD4	M8522	AD CRY 12 H
	137	13	IRD4	M8522	AD CRY 18 H
	137	14	IRD4	M8522	AD CRY 24 H
	137	15	IRD4	M8522	AD CRY 36 H
	132	05	EDP3	M8524	AD OVERFLOW 00 L
	136	12	IRD3	M8522	AD=0 L
*	15X	13-35	VMA3	M8542	ADR BRK 13-35 H **NOTE
;	126	0-35	EDP3	M8512	ADX 0 TO 35 H
	137	16	IRD4	M8522	ADX CRY 12 H
	137	17	IRD4	M8522	ADX CRY 24 H
	116	11	APR2	M8545	APR ANY EBOX ERR FLG H
	115	10	APR3	M8545	APR EBOX DISABLE CS H
	115	13	APR6	M8545	APR EBOX ERA H
	116	10	APR3	M8545	APR EBUS F01 E H
	116	09	APR3	M8545	APR EBUS REQ L
	115	09	APR3	M8545	APR EBUS RETURN H
	116	13	APR6	M8545	APR EN REFILL RAM WR H
	114	16	APR3	M8545	APR FM 36 H
**	114	14	APR4	M8545	APR FM ADR 1 H
**	114	11	APR4	M8545	APR FM ADR 10 H
**	114	13	APR4	M8545	APR FM ADR 2 H
**	114	12	APR4	M8545	APR FM ADR 4 H
**	114	10	APR5	M8545	APR FM BLOCK 1 H
**	114	09	APR5	M8545	APR FM BLOCK 2 H
**	114	08	APR5	M8545	APR FM BLOCK 4 H
	114	07	APR5	M8545	APR MBOX CTL 03 H
	115	07	APR5	M8545	APR MBOX CTL 06 H
	112	08	APR1	M8545	APR1 I/O PF ERR EN IN H
	110	08	APR1	M8545	APR1 I/O PF ERR IN H
	112	09	APR1	M8545	APR1 MB PAR ERR EN IN H
	110	09	APR1	M8545	APR1 MB PAR ERR IN H
	112	07	APR1	M8545	APR1 NXM ERR EN IN H
	110	07	APR1	M8545	APR1 NXM ERR IN H
	112	06	APR1	M8545	APR1 SBUS ERR EN IN H
	110	06	APR1	M8545	APR1 SBUS ERR IN H
	110	01	APR1	M8545	APR1 SWEEP BUSY EN H
	110	14	APR2	M8545	APR2 APR INTERRUPT H
	112	10	APR2	M8545	APR2 C DIR P ERR EN IN H
	110	10	APR2	M8545	APR2 C DIR P ERR IN H
	112	12	APR2	M8545	APR2 PWR FAIL EN IN H
	110	12	APR2	M8545	APR2 PWR FAIL IN H
	112	11	APR2	M8545	APR2 S ADR P ERR EN IN H
	110	11	APR2	M8545	APR2 S ADR P ERR IN H
	112	13	APR2	M8545	APR2 SWEEP DONE EN IN H
	110	13	APR2	M8545	APR2 SWEEP DONE IN H
	115	11	APR2	M8545	APR2 WR BAD ADR PAR L
	117	10	APR3	M8545	APR3 EBOX SEND F02 H
	117	09	APR3	M8545	APR3 EBUS DEMAND H
	113	09	APR3	M8545	APR3 FETCH COMP H
	111	13	APR3	M8545	APR3 FM EXTENDED H
	114	17	APR3	M8545	APR3 FM ODD PARITY H
	113	10	APR3	M8545	APR3 READ COMP H
	113	12	APR3	M8545	APR3 USER COMP H
	113	11	APR3	M8545	APR3 WRITE COMP H
	111	14	APR4	M8545	APR4 AC+# 09 H
	111	15	APR4	M8545	APR4 AC+# 10 H
	111	16	APR4	M8545	APR4 AC+# 11 H
	111	17	APR4	M8545	APR4 AC+# 12 H
	114	15	APR4	M8545	APR4 F02 EN H
	111	08	APR5	M8545	APR5 CURRENT BLOCK 1 H
	111	07	APR5	M8545	APR5 CURRENT BLOCK 2 H
	111	06	APR5	M8545	APR5 CURRENT BLOCK 4 H
	111	11	APR5	M8545	APR5 PREV BLOCK 1 H
	111	10	APR5	M8545	APR5 PREV BLOCK 2 H
	111	09	APR5	M8545	APR5 PREV BLOCK 4 H
	116	08	APR5	M8545	APR5 PT DIR WR L
	117	08	APR5	M8545	APR5 PT WR L
	115	08	APR5	M8545	APR5 SET PAGE FAIL L
	116	07	APR5	M8545	APR5 WR PT SEL 0 H
	117	07	APR5	M8545	APR5 WR PT SEL 1 H
	115	12	APR6	M8545	APR6 EBOX CCA H
	117	12	APR6	M8545	APR6 EBOX EBR H
	115	16	APR6	M8545	APR6 EBOX LOAD REG L
	115	17	APR6	M8545	APR6 EBOX READ REG L

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	115	14	APR6	M8545	APR6 EBOX SBUS DIAG H
	117	13	APR6	M8545	APR6 EBOX SPARE H
	116	12	APR6	M8545	APR6 EBOX UBR H
*	120	12-35	EDP1	M8512	AR 12 TO 35 H
*	125	0-35	EDP2	M8512	ARX 0 TO 35 H
*	121	0-35	EDP4	M8512	BR 0 TO 35 H
*	124	0-35	EDP4	M8512	BRX 0 TO 35 H
NOTE	165	27	MBC1	M8531YA	CAM SEL 1 H
NOTE	165	28	MBC1	M8531YA	CAM SEL 2 H
	176	11	CHC1	M8533	CBUS ERROR E H
	175	11	CHC1	M8533	CBUS LAST WORD E H
	161	16	MBZ5	M8537	CBUS PAR LEFT TE H
	162	16	MBZ5	M8537	CBUS PAR RIGHT TE H
	174	11	CHC1	M8533	CBUS READY E H
	170	12	CHC5	M8533	CBUS SEL 0 E H
	171	12	CHC5	M8533	CBUS SEL 1 E H
	172	12	CHC5	M8533	CBUS SEL 2 E H
	173	12	CHC5	M8533	CBUS SEL 3 E H
	174	12	CHC5	M8533	CBUS SEL 4 E H
	175	12	CHC5	M8533	CBUS SEL 5 E H
	176	12	CHC5	M8533	CBUS SEL 6 E H
	177	12	CHC5	M8533	CBUS SEL 7 E H
	173	19	CCL3	M8536	CCL AF T2 L
	171	18	CCL3	M8536	CCL ALU MINUS L
	176	18	CCL2	M8536	CCL BUF ADR 3 H
	176	06	CCW4	M8534	CCL CCW REG LOAD H
	175	16	CCL2	M8536	CCL CCWF REQ H
	173	18	CCL4	M8536	CCL CH MB SEL 1 H
	173	16	CCL4	M8536	CCL CH MB SEL 2 H
	171	19	CCL4	M8536	CCL CH TEST MB PAR L
	174	18	CCL3	M8536	CCL CHAN EPT H
	174	16	CCL3	M8536	CCL CHAN REQ H
	174	19	CCL4	M8536	CCL CHAN TO MEM H
	175	19	CCL2	M8536	CCL MEM STORE REQ H
	170	16	CCL5	M8536	CCL ODD WC PAR H
	176	19	CCL4	M8536	CCL START MEM L
	170	19	CCL5	M8536	CCL WC=0 L
	177	08	CCW3	M8534	CCL WC=1 H
	177	09	CCW3	M8534	CCL WC=2 H
	176	05	CCW3	M8534	CCL WC=3 H
	177	16	CCL1	M8536	CCL1 ERR REQ H
	175	18	CCL2	M8536	CCL2 ACT FLAG REQ H
	172	16	CCL3	M8536	CCL3 CCWF T2 H
	172	18	CCL3	M8536	CCL3 MB REQ T2 H
	171	16	CCL3	M8536	CCL3 MB RIP A H
	177	19	CCL3	M8536	CCL3 MEM PTR EN H
	172	19	CCL4	M8536	CCL4 REVERSE H
	176	16	CCL4	M8536	CCL4 STORE CCW H
	170	18	CCL5	M8536	CCL5 WC GE4 H
	177	18	CCL6	M8536	CCL6 CSH CHAN CYC L
	172	05	CCW3	M8534	CCW ACT CTR 0 EN H
	172	06	CCW3	M8534	CCW ACT CTR 1 EN H
	172	07	CCW3	M8534	CCW ACT CTR 2 EN H
	170	08	CCW5	M8534	CCW ACT FLAG REQ ENA H
	170	10	CCW3	M8534	CCW ALU C2 OUT H
	170	09	CCW3	M8534	CCW ALU C8 OUT H
	172	08	CCW1	M8534	CCW BUF ADR 0 L
	172	09	CCW1	M8534	CCW BUF ADR 1 L
	172	10	CCW1	M8534	CCW BUF ADR 2 L
	170	06	CCW6	M8534	CCW CCWF REQ ENA H
	171	10	CCW6	M8534	CCW CCWF WAITING H
*	176	07-10	CCW2	M8534	CCW CHA 14-17 H
*	175	05-10	CCW2	M8534	CCW CHA 18-23 H
*	174	05-10	CCW2	M8534	CCW CHA 24-29 H
**	173	05	CCW2	M8534	CCW CHA 30 H
**	173	06	CCW2	M8534	CCW CHA 31 H
**	173	07	CCW2	M8534	CCW CHA 32 H
**	173	08	CCW2	M8534	CCW CHA 33 H
**	173	09	CCW2	M8534	CCW CHA 34 H
**	173	10	CCW2	M8534	CCW CHA 35 H
	171	09	CCW1	M8534	CCW MEM ADR=0 H
	170	07	CCW6	M8534	CCW MEM STORE ENA H
	177	10	CCW4	M8534	CCW ODD ADR PAR H
	177	05	CCW6	M8534	CCW RAM ADR 1 H
	177	06	CCW6	M8534	CCW RAM ADR 2 H
	177	07	CCW6	M8534	CCW RAM ADR 4 H
	170	05	CCW4	M8534	CCW WD READY H
	171	05	CCW4	M8534	CCW WD0 REQ H
	171	06	CCW4	M8534	CCW WD1 REQ H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	171	07	CCW4	M8534	CCW WD2 REQ H
	171	08	CCW4	M8534	CCW WD3 REQ H
	177	11	CHC1	M8533	CH CBUS REQ H
	177	13	CHC2	M8533	CH CONTR CYC H
	175	14	CHC2	M8533	CH CONTR REQ H
	174	14	CHC3	M8533	CH CTOM H
	172	14	CHC2	M8533	CH DONE INTR H
	176	13	CHC1	M8533	CH MB REQ INH H
	170	14	CHC2	M8533	CH RESET INTR H
	176	14	CHC1	M8533	CH REVERSE H
	175	13	CHC5	M8533	CH SEL 8A H
	177	14	CHC2	M8533	CH START H
	171	14	CHC2	M8533	CH START INTR H
	173	14	CHC2	M8533	CH STORE H
	170	11	CHC1	M8533	CH T0 H
	171	11	CHC1	M8533	CH T1 H
	172	11	CHC1	M8533	CH T2 H
	173	11	CHC1	M8533	CH T3 H
	162	15	MBZ4	M8537	CHAN ADR PAR ERR L
	160	25	MBZ3	M8537	CHAN NXM ERR L
	160	16	MBZ4	M8537	CHAN PAR ERR L
	162	19	MBZ1	M8537	CHAN READ L
	174	13	CHC1	M8533	CHX CTOM H
	172	13	CHC1	M8533	CHX DONE H
	170	13	CHC1	M8533	CHX RESET H
	171	13	CHC1	M8533	CHX START H
	173	13	CHC1	M8533	CHX STORE H
	102	32	CLK4	M8526YA	CLK EBOX REQ H
	100	30	CLK1	M8526YA	CLK EBUS CLK H
	102	30	CLK1	M8526YA	CLK ERROR STOP H
	102	35	CLK4	M8526YA	CLK FORCE 1777 H
	100	32	CLK4	M8526YA	CLK INSTR 1777 H
	103	32	CLK4	M8526YA	CLK MB XFER H
	103	34	CLK4	M8526YA	CLK PAGE ERROR H
	100	31	CLK1	M8526YA	CLK SBUS CLK H
	103	31	CLK2	M8526YA	CLK2 BURST L
	104	31	CLK2	M8526YA	CLK2 EBOX SS L
	102	31	CLK2	M8526YA	CLK2 GO L
	104	30	CLK3	M8526YA	CLK3 CRAM PAR ERR H
	103	30	CLK3	M8526YA	CLK3 DRAM PAR ERR H
	104	33	CLK3	M8526YA	CLK3 EBOX SOURCE H
	107	30	CLK3	M8526YA	CLK3 ERROR L
	105	30	CLK3	M8526YA	CLK3 FM PAR ERR H
	106	30	CLK3	M8526YA	CLK3 FS ERROR H
	102	33	CLK3	M8526YA	CLK3 SYNC H
	103	35	CLK4	M8526YA	CLK4 1777 EN H
	103	33	CLK4	M8526YA	CLK4 EBOX CLK L
	102	34	CLK4	M8526YA	CLK4 PAGE FAIL EN L
	107	31	CLK4	M8526YA	CLK4 PAGE FAIL H
	106	35	CLK5	M8526YA	CLK5 AR/ARX PAR CHECK L
**	101	35	CLK5	M8526YA	CLK5 BURST 01 H
**	101	34	CLK5	M8526YA	CLK5 BURST 02 H
**	101	33	CLK5	M8526YA	CLK5 BURST 04 H
**	101	32	CLK5	M8526YA	CLK5 BURST 08 H
**	100	34	CLK5	M8526YA	CLK5 BURST 128 H
**	101	31	CLK5	M8526YA	CLK5 BURST 16 H
**	101	30	CLK5	M8526YA	CLK5 BURST 32 H
**	100	35	CLK5	M8526YA	CLK5 BURST 64 H
	100	33	CLK5	M8526YA	CLK5 BURST CNT=0 H
	105	34	CLK5	M8526YA	CLK5 CRAM PAR CHECK L
	106	34	CLK5	M8526YA	CLK5 DRAM PAR CHECK L
	105	33	CLK5	M8526YA	CLK5 EBOX CRM DIS H
	107	33	CLK5	M8526YA	CLK5 EBOX CTL DIS H
	106	33	CLK5	M8526YA	CLK5 EBOX EDP DIS H
	107	35	CLK5	M8526YA	CLK5 ERR STOP EN L
	104	34	CLK5	M8526YA	CLK5 FM PAR CHECK L
	107	34	CLK5	M8526YA	CLK5 FS CHECK L
	104	35	CLK5	M8526YA	CLK5 MBOX CYCLE DIS H
	105	35	CLK5	M8526YA	CLK5 MBOX RESP SIM L
	107	32	CLK5	M8526YA	CLK5 RATE SEL 1 H
	106	32	CLK5	M8526YA	CLK5 RATE SEL 2 H
	105	32	CLK5	M8526YA	CLK5 SOURCE SEL 1 H
	104	32	CLK5	M8526YA	CLK5 SOURCE SEL 2 H
	136	18	CON4	M8525	CON AR 36 H
	137	18	CON4	M8525	CON ARX 36 H
	133	23	CON4	M8525	CON ARX LOADED L
	131	19	CON3	M8525	CON CACHE LOAD EN H
	133	05	CON2	M8524	CON CLR PRIVATE INSTR H
	137	22	CON2	M8525	CON COND ADR 10 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	132	18	CON1	M8525	CON COND EN 00-07 L
	133	22	CON2	M8525	CON COND INSTR ABORT H
	134	19	CON1	M8525	CON COND/LOAD VMA HELD H
	132	20	CON1	M8525	CON COND/MBOX CTL L
	132	19	CON1	M8525	CON COND/SEL VMA L
	133	19	CON1	M8525	CON COND/VMA GETS # H
	135	18	CON3	M8525	CON DELAY REQ H
	133	20	CON3	M8525	CON EBUS REL H
	117	11	CON5	M8545	CON FM WRITE PAR L
	134	24	CON5	M8525	CON FM WRITE PAR L
	136	24	CON5	M8525	CON FM XFER L
	131	21	CON3	M8525	CON KI10 PAGING MODE L
	134	22	CON2	M8525	CON LOAD ACCESS COND H
	136	22	CON2	M8525	CON LOAD DRAM H
	132	22	CON2	M8525	CON LOAD IR L
	135	19	CON1	M8525	CON LOAD SPEC INSTR L
	132	21	CON2	M8525	CON LONG EN L
	135	24	CON5	M8525	CON MBOX WAIT L
	135	21	CON2	M8525	CON NICOND 07 H
	136	21	CON2	M8525	CON NICOND 08 H
	137	21	CON2	M8525	CON NICOND 09 H
	134	21	CON2	M8525	CON NICOND TRAP EN H
	133	21	CON4	M8525	CON PC+1 INH L
	134	04	CON5	M8524	CON PI CYCLE A L
	137	24	CON5	M8525	CON PI DISMISS L
	133	18	CON1	M8525	CON SKIP EN 40-47 L
	134	18	CON1	M8525	CON SKIP EN 50-57 L
	134	20	CON3	M8525	CON SR 00 H
	135	20	CON3	M8525	CON SR 01 H
	136	20	CON3	M8525	CON SR 02 H
	137	20	CON3	M8525	CON SR 03 H
	131	22	CON3	M8525	CON TRAP EN H
	134	23	CON4	M8525	CON UCODE STATE 01 H
	135	23	CON4	M8525	CON UCODE STATE 03 H
	136	23	CON4	M8525	CON UCODE STATE 05 H
	137	23	CON4	M8525	CON UCODE STATE 07 H
	137	19	CON1	M8525	CON VMA SEL 1 L
	136	19	CON1	M8525	CON VMA SEL 2 L
	130	18	CON3	M8525	CON WR EVEN PAR ADR H
	135	22	CON2	M8525	CON2 INSTR GO L
	131	18	CON3	M8525	CON3 CACHE LOOK EN H
	130	19	CON3	M8525	CON3 WR EVEN PAR DATA H
	130	20	CON3	M8525	CON3 WR EVEN PAR DIR H
	132	23	CON4	M8525	CON4 AR LOADED H
	133	24	CON5	M8525	CON5 MEM CYCLE L
	132	24	CON5	M8525	CON5 PI CYCLE H
	160	15	MBZ1	M8537	CORE BUSY H
**	145	01	CRA1	M8541	CR ADR 00 F H
**	145	02	CRA1	M8541	CR ADR 01 F H
**	145	03	CRA1	M8541	CR ADR 02 F H
**	145	04	CRA1	M8541	CR ADR 03 F H
**	145	05	CRA1	M8541	CR ADR 04 F H
**	144	00	CRA1	M8541	CR ADR 05 F H
**	144	01	CRA1	M8541	CR ADR 06 F H
**	144	02	CRA2	M8541	CR ADR 07 F H
**	144	03	CRA2	M8541	CR ADR 08 F H
**	144	04	CRA2	M8541	CR ADR 09 F H
**	144	05	CRA2	M8541	CR ADR 10 F H
**	141	00	CRA4	M8541	CRA CALL, RESET H
**	141	01	CRA3	M8541	CRA DISP 00 H
**	141	02	CRA3	M8541	CRA DISP 01 H
**	141	03	CRA3	M8541	CRA DISP 02 H
**	141	04	CRA3	M8541	CRA DISP 03 H
**	141	05	CRA3	M8541	CRA DISP 04 H
	140	01	CRA3	M8541	CRA DISP EN 00-03 L
	140	00	CRA3	M8541	CRA DISP EN 00-07 L
	143	00	CRA3	M8541	CRA DISP EN 30-37 L
**	145	00	CRA3	M8541	CRA DISP PARITY H
**	147	01	CRA3	M8541	CRA LOC 00 H
**	147	02	CRA3	M8541	CRA LOC 01 H
**	147	03	CRA3	M8541	CRA LOC 02 H
**	147	04	CRA3	M8541	CRA LOC 03 H
**	147	05	CRA3	M8541	CRA LOC 04 H
**	146	00	CRA3	M8541	CRA LOC 05 H
**	146	01	CRA3	M8541	CRA LOC 06 H
**	146	02	CRA3	M8541	CRA LOC 07 H
**	146	03	CRA3	M8541	CRA LOC 08 H
**	146	04	CRA3	M8541	CRA LOC 09 H
**	146	05	CRA3	M8541	CRA LOC 10 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	143	01	CRA4	M8541	CRA SBR RET 00 H
**	143	02	CRA4	M8541	CRA SBR RET 01 H
**	143	03	CRA4	M8541	CRA SBR RET 02 H
**	143	04	CRA4	M8541	CRA SBR RET 03 H
**	143	05	CRA4	M8541	CRA SBR RET 04 H
**	142	00	CRA4	M8541	CRA SBR RET 05 H
**	142	01	CRA4	M8541	CRA SBR RET 06 H
**	142	02	CRA4	M8541	CRA SBR RET 07 H
**	142	03	CRA4	M8541	CRA SBR RET 08 H
**	142	04	CRA4	M8541	CRA SBR RET 09 H
**	142	05	CRA4	M8541	CRA SBR RET 10 H
**	140	05	CRA4	M8541	CRA STACK ADR 01 H
**	140	04	CRA4	M8541	CRA STACK ADR 02 H
**	140	03	CRA4	M8541	CRA STACK ADR 04 H
**	140	02	CRA4	M8541	CRA STACK ADR 10 H
*	147	08-11	CRM5	M8548	CRAM 00-03 H
*	147	14-17	CRM5	M8548	CRAM 04-07 H
*	147	20-23	CRM5	M8548	CRAM 08-11 H
*	147	26-29	CRM5	M8548	CRAM 12-15 H
*	147	32-35	CRM5	M8548	CRAM 16-19 H
*	146	08-11	CRM5	M8548	CRAM 20-23 H
*	146	14-17	CRM5	M8548	CRAM 24-27 H
*	146	20-23	CRM5	M8548	CRAM 28-31 H
*	146	26-29	CRM5	M8548	CRAM 32-35 H
*	146	32-35	CRM5	M8548	CRAM 36-39 H
*	145	08-11	CRM5	M8548	CRAM 40-43 H
*	145	14-17	CRM5	M8548	CRAM 44-47 H
*	145	20-23	CRM5	M8548	CRAM 48-51 H
*	145	26-29	CRM5	M8548	CRAM 52-55 H
*	145	32-35	CRM5	M8548	CRAM 56-59 H
**	144	08	CRM5	M8548	CRAM 60 H
**	144	10	CRM5	M8548	CRAM 62 H
**	144	14	CRM5	M8548	CRAM 64 H
**	144	16	CRM5	M8548	CRAM 66 H
**	144	20	CRM5	M8548	CRAM 68 H
**	144	22	CRM5	M8548	CRAM 70 H
**	144	26	CRM5	M8548	CRAM 72 H
**	144	28	CRM5	M8548	CRAM 74 H
**	144	32	CRM5	M8548	CRAM 76 H
**	144	34	CRM5	M8548	CRAM 78 H
**	144	11	CRM5	M8548	CRAM PAR 00 H
**	144	17	CRM5	M8548	CRAM PAR 04 H
**	144	23	CRM5	M8548	CRAM PAR 08 H
**	144	29	CRM5	M8548	CRAM PAR 12 H
**	144	35	CRM5	M8548	CRAM PAR 16 H
**	144	09	CRM5	M8548	CRAM PAR 1ST 00 H
**	144	15	CRM5	M8548	CRAM PAR 1ST 04 H
**	144	21	CRM5	M8548	CRAM PAR 1ST 08 H
**	144	27	CRM5	M8548	CRAM PAR 1ST 12 H
**	144	33	CRM5	M8548	CRAM PAR 1ST 16 H
**	170	00	CRC6	M8535	CRC CH BUF ADR 0 H
**	171	00	CRC6	M8535	CRC CH BUF ADR 1 H
**	172	00	CRC6	M8535	CRC CH BUF ADR 2 H
**	173	00	CRC6	M8535	CRC CH BUF ADR 3 H
**	174	00	CRC6	M8535	CRC CH BUF ADR 4 H
**	175	00	CRC6	M8535	CRC CH BUF ADR 5 H
**	176	00	CRC6	M8535	CRC CH BUF ADR 6 H
	172	03	CRC3	M8535	CRC ERR IN H
	172	02	CRC3	M8535	CRC LAST WORD IN H
	171	04	CRC4	M8535	CRC LONG WC ERR H
	170	02	CRC4	M8535	CRC MEM STORE ENA L
	171	02	CRC4	M8535	CRC OVN ERR IN H
	172	01	CRC3	M8535	CRC READY IN H
	172	04	CRC3	M8535	CRC REVERSE IN H
	171	01	CRC4	M8535	CRC RH20 ERR IN H
	175	01	CRC6	M8535	CRC SEL 1D L
	175	02	CRC6	M8535	CRC SEL 2D L
	175	03	CRC6	M8535	CRC SEL 4D L
	171	03	CRC4	M8535	CRC SHORT WC ERR H
	174	02	CRC5	M8535	CRC WR RAM L
	174	01	CRC1	M8535	CRC1 ACT FLAG ENA H
	175	04	CRC1	M8535	CRC1 AF REQ ENA L
	176	01	CRC1	M8535	CRC1 MEM PTR0 H
	176	02	CRC1	M8535	CRC1 MEM PTR1 H
	176	03	CRC1	M8535	CRC1 MEM PTR2 H
	176	04	CRC1	M8535	CRC1 MEM PTR3 H
	177	00	CRC1	M8535	CRC1 PTR DIF=0 H
	173	01	CRC2	M8535	CRC2 ACT CTR 0R H
	173	02	CRC2	M8535	CRC2 ACT CTR 1R H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES
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	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	173	03	CRC2	M8535	CRC2 ACT CTR 2R H
	173	04	CRC2	M8535	CRC2 RAM CYC H
	174	03	CRC3	M8535	CRC3 OP CODE 00 H
	174	04	CRC3	M8535	CRC3 OP CODE 01 H
	170	03	CRC4	M8535	CRC4 DONE IN H
	170	01	CRC4	M8535	CRC4 RESET IN L
	170	04	CRC4	M8535	CRC4 STORE IN H
	177	01	CRC6	M8535	CRC6 CH ADR 0C L
	177	02	CRC6	M8535	CRC6 CH ADR 1C L
	177	03	CRC6	M8535	CRC6 CH ADR 2C L
	177	04	CRC6	M8535	CRC6 CH ADR 3C L
NOTE	170	20	CHX2	M8515	CSH 0 ANY VAL L
	177	25	CHA3	M8513YA	CSH 0 ANY WR L
NOTE	171	20	CHX2	M8515	CSH 1 ANY VAL L
	175	25	CHA3	M8513YA	CSH 1 ANY WR L
NOTE	172	20	CHX2	M8515	CSH 2 ANY VAL L
	176	25	CHA3	M8513YA	CSH 2 ANY WR L
NOTE	173	20	CHX2	M8515	CSH 3 ANY VAL L
	174	25	CHA3	M8513YA	CSH 3 ANY WR L
NOTE	174	20	CHX4	M8515	CSH DIR 0 PAR ODD H
NOTE	175	20	CHX4	M8515	CSH DIR 1 PAR ODD H
NOTE	176	20	CHX4	M8515	CSH DIR 2 PAR ODD H
NOTE	177	20	CHX4	M8515	CSH DIR 3 PAR ODD H
	160	19	MBZ1	M8537	CSH EN CSH DATA L
	173	25	CHX3	M8513YA	CSH LRU 1 H
	172	25	CHX3	M8513YA	CSH LRU 2 H
	161	26	MBZ6	M8537	CSH PAR BIT A H
	162	26	MBZ6	M8537	CSH PAR BIT B H
	162	17	MBZ5	M8537	CSH PAR BIT IN H
	170	28	CSH4	M8513YA	CSH REFILL RAM WR L
NOTE	161	30	MBC2	M8531YA	CSH SEL LRU H
NOTE	175	21	CHX3	M8515	CSH USE ADR 2 H
NOTE	176	21	CHX3	M8515	CSH USE ADR 3 H
NOTE	177	21	CHX3	M8515	CSH USE ADR 4 H
	172	27	CSH6	M8513YA	CSH USE HOLD H
NOTE	170	21	CHX3	M8515	CSH USE IN 0 H
NOTE	171	21	CHX3	M8515	CSH USE IN 1 H
NOTE	172	21	CHX3	M8515	CSH USE IN 2 H
NOTE	173	21	CHX3	M8515	CSH USE IN 3 H
NOTE	174	21	CHX3	M8515	CSH USE IN 4 H
	175	23	CSH6	M8513YA	CSH USE WR EN H
NOTE	163	29	MBC3	M8531YA	CSH VAL SEL ALL H
NOTE	163	30	MBC3	M8531YA	CSH VAL WR DATA H
NOTE	163	31	MBC3	M8531YA	CSH WR SEL ALL H
	176	31	MBX4	M8529YA	CSH WR WD 0 EN H
	177	31	MBX4	M8529YA	CSH WR WD 1 EN H
	170	32	MBX4	M8529YA	CSH WR WD 2 EN H
	171	32	MBX4	M8529YA	CSH WR WD 3 EN H
NOTE	163	32	MBC3	M8531YA	CSH WR WR DATA H
	174	29	CSH1	M8513YA	CSH1 CACHE IDLE L
	172	28	CSH1	M8513YA	CSH1 CCA CYC L
	177	27	CSH1	M8513YA	CSH1 CYC TYPE HOLD H
	174	28	CSH1	M8513YA	CSH1 EBOX CYC B L
	175	28	CSH1	M8513YA	CSH1 MB CYC L
	172	26	CSH1	M8513YA	CSH1 READY TO GO A H
	176	27	CSH2	M8513YA	CSH2 E CACHE WR CYC H
	174	22	CSH2	M8513YA	CSH2 E CORE RD RQ A L
	172	29	CSH2	M8513YA	CSH2 EBOX REQ EN L
	175	22	CSH2	M8513YA	CSH2 EBOX RETRY REQ L
	173	23	CSH2	M8513YA	CSH2 MBOX RESP L
	173	22	CSH2	M8513YA	CSH2 ONE WORD RD A L
	177	28	CSH2	M8513YA	CSH2 RD PAUSE 2ND HALF L
	173	24	CSH2	M8513YA	CSH2 RD PSE 2ND REQ EN L
	170	25	CSH2	M8513YA	CSH2 WR TEST L
	174	27	CSH3	M8513YA	CSH3 ADR PMA EN H
	170	26	CSH3	M8513YA	CSH3 ANY VAL HOLD H
	175	27	CSH3	M8513YA	CSH3 GATE VMA 27-33 H
	171	28	CSH3	M8513YA	CSH3 MB WR RQ CLR NXT L
	170	27	CSH4	M8513YA	CSH4 DATA CLR DONE L
	176	24	CSH4	M8513YA	CSH4 EBOX T0 L
	171	29	CSH4	M8513YA	CSH4 EBOX T1 L
	173	29	CSH4	M8513YA	CSH4 EBOX T2 L
	170	29	CSH4	M8513YA	CSH4 EBOX T3 L
	177	29	CSH4	M8513YA	CSH4 EBOX WR T4 L
	175	29	CSH4	M8513YA	CSH4 ONE WORD WR T0 L
	177	24	CSH4	M8513YA	CSH4 PAGE FAIL DLY H
	171	24	CSH4	M8513YA	CSH4 PAGE FAIL T2 L
	173	27	CSH4	M8513YA	CSH4 WRITEBACK T1 A H
	171	22	CSH5	M8513YA	CSH5 CHAN RD T5 L

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	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	172	24	CSH5	M8513YA	CSH5 CHAN T4 L
	171	27	CSH5	M8513YA	CSH5 CHAN WR T5 L
	174	26	CSH5	M8513YA	CSH5 CSH T0 L
	170	22	CSH5	M8513YA	CSH5 PAGE REFILL COMP L
	177	26	CSH5	M8513YA	CSH5 PAGE REFILL T10 L
	176	29	CSH5	M8513YA	CSH5 PAGE REFILL T4 L
	176	23	CSH5	M8513YA	CSH5 PAGE REFILL T8 L
	174	24	CSH5	M8513YA	CSH5 PAGE REFILL T9,12 L
	173	26	CSH5	M8513YA	CSH5 T1 L
	176	26	CSH5	M8513YA	CSH5 T2 L
	175	26	CSH5	M8513YA	CSH5 T3 L
	170	23	CSH6	M8513YA	CSH6 CACHE WR IN H
	172	23	CSH6	M8513YA	CSH6 CCA CYC DONE L
	176	22	CSH6	M8513YA	CSH6 CCA INVAL T4 L
	172	22	CSH6	M8513YA	CSH6 CHAN WR CACHE L
	177	23	CSH6	M8513YA	CSH6 DATA DLY 1 L
	171	25	CSH6	M8513YA	CSH6 EBOX LOAD REG H
	170	24	CSH6	M8513YA	CSH6 MBOX PT DIR WR L
	174	23	CSH6	M8513YA	CSH6 PAGE FAIL HOLD L
	177	22	CSH6	M8513YA	CSH6 PAGE REFILL ERROR L
	171	23	CSH6	M8513YA	CSH6 WR DATA RDY L
	173	28	CSH7	M8513YA	CSH7 CCA WRITEBACK L
	176	28	CSH7	M8513YA	CSH7 E WRITEBACK L
	171	26	CSH7	M8513YA	CSH7 FILL CACHE RD L
	106	24	CTL1	M8543	CTL AD LONG H
	106	25	CTL1	M8543	CTL ADX CRY 36 A H
	105	25	CTL1	M8543	CTL ADX CRY 36 H
	100	28	CTL2	M8543	CTL AR 00-08 LOAD L
	104	28	CTL2	M8543	CTL AR 00-11 CLR H
	101	28	CTL2	M8543	CTL AR 09-17 LOAD L
	105	28	CTL2	M8543	CTL AR 12-17 CLR H
	101	26	CTL2	M8543	CTL ARL SEL 1 H
	100	26	CTL2	M8543	CTL ARL SEL 2 H
	103	28	CTL2	M8543	CTL ARL SEL 4 H
	106	28	CTL2	M8543	CTL ARR CLR H
	100	27	CTL2	M8543	CTL ARR LOAD A L
	101	27	CTL2	M8543	CTL ARR LOAD B L
	103	26	CTL2	M8543	CTL ARR SEL 1 H
	102	26	CTL2	M8543	CTL ARR SEL 2 H
	102	28	CTL2	M8543	CTL ARX LOAD H
	105	26	CTL2	M8543	CTL ARXL SEL 1 L
	104	26	CTL2	M8543	CTL ARXL SEL 2 H
	107	26	CTL2	M8543	CTL ARXR SEL 1 H
	106	26	CTL2	M8543	CTL ARXR SEL 2 H
	102	25	CTL1	M8543	CTL COND/AR GETS EXP H
	103	25	CTL1	M8543	CTL DISP RET L
	107	24	CTL1	M8543	CTL INH CRY 18 L
	136	14	CTL1	M8522	CTL INH CRY 18 L
	104	25	CTL1	M8543	CTL LOAD PC L
	105	27	CTL2	M8543	CTL MQ SEL 1 H
	104	27	CTL2	M8543	CTL MQ SEL 2 H
	106	27	CTL2	M8543	CTL MQM EN H
	103	27	CTL2	M8543	CTL MQM SEL 1 H
	102	27	CTL2	M8543	CTL MQM SEL 2 H
	107	28	CTL2	M8543	CTL SPEC CALL L
	101	25	CTL1	M8543	CTL SPEC MTR CTL L
	101	24	CTL1	M8543	CTL SPEC/CLR FPD H
	104	24	CTL1	M8543	CTL SPEC/FLAG CTL H
	102	24	CTL1	M8543	CTL SPEC/GEN CRY 18 H
	136	15	CTL1	M8522	CTL SPEC/GEN CRY 18 H
	100	25	CTL1	M8543	CTL SPEC/SAVE FLAGS L
	100	24	CTL1	M8543	CTL SPEC/SCM ALT H
	105	24	CTL1	M8543	CTL SPEC/SP MEM CYCLE H
	103	24	CTL1	M8543	CTL SPEC/STACK UPDATE H
NOTE	163	33	MBC3	M8531YA	DATA VALID A OUT H
NOTE	164	27	MBC3	M8531YA	DATA VALID B OUT H
	107	27	CTL3	M8543	DIAG LOAD EBUS REG L
	107	25	CTL3	M8543	DIAG MEM RESET H
**	130	15	IRD1	M8522	DR ADR 00 A H
**	130	16	IRD1	M8522	DR ADR 01 A H
**	130	17	IRD1	M8522	DR ADR 02 A H
**	131	12	IRD1	M8522	DR ADR 03 A H
**	131	13	IRD1	M8522	DR ADR 04 A H
**	131	14	IRD1	M8522	DR ADR 05 A H
**	131	15	IRD1	M8522	DR ADR 06 A H
**	131	16	IRD1	M8522	DR ADR 07 A H
**	131	17	IRD1	M8522	DR ADR 08 A H
**	133	12	IRD1	M8522	DRAM A 00 H
**	133	13	IRD1	M8522	DRAM A 01 H

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**	133	14	IRD1	M8522	DRAM A 02 H
**	133	15	IRD1	M8522	DRAM B 00 H
**	133	16	IRD1	M8522	DRAM B 01 H
**	133	17	IRD1	M8522	DRAM B 02 H
**	134	14	IRD1	M8522	DRAM J 01 H
**	134	15	IRD1	M8522	DRAM J 02 H
**	134	16	IRD1	M8522	DRAM J 03 H
**	134	17	IRD1	M8522	DRAM J 04 H
**	135	14	IRD1	M8522	DRAM J 07 H
**	135	15	IRD1	M8522	DRAM J 08 H
**	135	16	IRD1	M8522	DRAM J 09 H
**	135	17	IRD1	M8522	DRAM J 10 H
	135	13	IRD3	M8522	DRAM ODD PARITY H
**	135	12	IRD1	M8522	DRAM PAR H
**	102	14	PIC4	M8532	EBUS CS00 E H
**	102	15	PIC4	M8532	EBUS CS01 E H
**	102	16	PIC4	M8532	EBUS CS02 E H
**	102	17	PIC4	M8532	EBUS CS03 E H
**	103	14	PIC4	M8532	EBUS CS04 E H
**	102	11	PIC4	M8532	EBUS CS05 E H
**	102	12	PIC4	M8532	EBUS CS06 E H
	102	13	PIC2	M8532	EBUS DEMAND E H
*	167	00-08	MBZ2	M8537	EBUS REG 00-08 H
*	167	14-26	MBZ2	M8537	EBUS REG 14-26 H
*NOTE	167	27-33	MBC1	M8531YA	EBUS REG 27-33 H
**	167	34,35	MBZ2	M8537	EBUS REG 34,35 H
**	120	00	EDP1	M8512	EDP AR 00 H
**	120	01	EDP1	M8512	EDP AR 01 H
**	120	02	EDP1	M8512	EDP AR 02 H
**	120	03	EDP1	M8512	EDP AR 03 H
**	120	04	EDP1	M8512	EDP AR 04 H
**	120	05	EDP1	M8512	EDP AR 05 H
**	120	06	EDP1	M8512	EDP AR 06 H
**	120	07	EDP1	M8512	EDP AR 07 H
**	120	08	EDP1	M8512	EDP AR 08 H
**	120	09	EDP1	M8512	EDP AR 09 H
**	120	10	EDP1	M8512	EDP AR 10 H
**	120	11	EDP1	M8512	EDP AR 11 H
**	133	07	SCD2	M8524	FE 00 H
**	133	08	SCD2	M8524	FE 01 H
**	133	09	SCD2	M8524	FE 02 H
**	133	10	SCD2	M8524	FE 03 H
**	133	11	SCD2	M8524	FE 04 H
**	132	07	SCD2	M8524	FE 05 H
**	132	08	SCD2	M8524	FE 06 H
**	132	09	SCD2	M8524	FE 07 H
**	132	10	SCD2	M8524	FE 08 H
**	132	11	SCD2	M8524	FE 09 H
	135	07	SCD2	M8524	FE SIGN H
*	123	0-35	EDP4	M8512	FM 0 TO 35 H
	172	32	MBX1	M8529YA	FORCE NO MATCH H
NOTE	160	27	MBC5	M8531YA	FORCE VALID MATCH 0 H
NOTE	160	28	MBC5	M8531YA	FORCE VALID MATCH 1 H
NOTE	160	29	MBC5	M8531YA	FORCE VALID MATCH 2 H
NOTE	160	30	MBC5	M8531YA	FORCE VALID MATCH 3 H
	136	16	IRD4	M8522	GEN CRY 36 H
**	132	14	IRD1	M8522	IR AC 09 H
**	132	15	IRD1	M8522	IR AC 10 H
**	132	16	IRD1	M8522	IR AC 11 H
**	132	17	IRD1	M8522	IR AC 12 H
	132	13	IRD3	M8522	IR EN AC H
	132	12	IRD3	M8522	IR EN I/O, JRST H
	136	13	IRD1	M8522	IR I/O LEGAL H
	134	13	IRD3	M8522	IR JRST 0, L
	130	12	IRD3	M8522	IR NORM 08 H
	130	13	IRD3	M8522	IR NORM 09 H
	130	14	IRD3	M8522	IR NORM 10 H
	174	32	MBX3	M8529YA	MB DATA CODE 1 H
	175	32	MBX3	M8529YA	MB DATA CODE 2 H
	160	20	MBZ1	M8537	MB IN SEL 1 H
	161	20	MBZ1	M8537	MB IN SEL 2 H
	162	20	MBZ1	M8537	MB IN SEL 4 H
	160	18	MBZ5	M8537	MB PAR BIT IN H
	176	32	MBX3	M8529YA	MB PAR H
	177	32	MBX2	M8529YA	MB REQ HOLD H
	171	33	MBX2	M8529YA	MB SEL 1 H
	172	33	MBX2	M8529YA	MB SEL 2 H
	173	33	MBX2	M8529YA	MB SEL HOLD H
	175	24	CSH3	M8513YA	MB TEST PAR A IN L

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	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	174	33	MBX6	M8529YA	MB0 HOLD IN H
	175	33	MBX6	M8529YA	MB1 HOLD IN H
	176	33	MBX6	M8529YA	MB2 HOLD IN H
	177	33	MBX6	M8529YA	MB3 HOLD IN H
NOTE	160	31	MBC1	M8531YA	MBC1 WRITE OK H
NOTE	162	27	MBC2	M8531YA	MBC2 CACHE WR 00 A H
NOTE	162	28	MBC2	M8531YA	MBC2 CACHE WR 09 A H
NOTE	162	29	MBC2	M8531YA	MBC2 CACHE WR 18 A H
NOTE	162	30	MBC2	M8531YA	MBC2 CACHE WR 27 A H
NOTE	160	32	MBC2	M8531YA	MBC2 CSH ADR WR PULSE H
NOTE	160	33	MBC2	M8531YA	MBC2 CSH DATA CLR DONE IN L
NOTE	161	27	MBC2	M8531YA	MBC2 CSH DATA CLR T1 L
NOTE	161	28	MBC2	M8531YA	MBC2 CSH DATA CLR T2 L
NOTE	161	29	MBC2	M8531YA	MBC2 CSH DATA CLR T3 L
NOTE	161	31	MBC2	M8531YA	MBC2 CSH VAL WR PULSE H
NOTE	161	32	MBC2	M8531YA	MBC2 CSH WR WR PULSE H
NOTE	162	32	MBC3	M8531YA	MBC3 A CHANGE COMING A L
NOTE	162	33	MBC3	M8531YA	MBC3 ANY SBUS RQ IN L
NOTE	163	27	MBC3	M8531YA	MBC3 B CHANGE COMING L
NOTE	164	28	MBC3	M8531YA	MBC3 INH 1ST MB REQ H
NOTE	164	32	MBC4	M8531YA	MBC4 CORE ADR 34 H
NOTE	164	33	MBC4	M8531YA	MBC4 CORE ADR 35 H
NOTE	165	29	MBC4	M8531YA	MBC4 CORE DATA VAL -1 L
NOTE	165	30	MBC4	M8531YA	MBC4 CORE DATA VALID -2 L
NOTE	165	31	MBC4	M8531YA	MBC4 CORE DATA VALID L
NOTE	165	32	MBC4	M8531YA	MBC4 CORE RD IN PROG A H
NOTE	166	32	MBC4	M8531YA	MBC4 MEM START L
NOTE	163	28	MBC5	M8531YA	MBC5 CORE BUSY B H
	161	15	MBZ4	M8537	MBOX ADR PAR ERR L
	162	24	MBZ4	M8537	MBOX MB PAR ERR L
	161	22	MBZ3	M8537	MBOX NXM ERR L
	161	24	MBZ4	M8537	MBOX SBUS ERR L
	170	30	MBX1	M8529YA	MBX1 CACHE BIT H
	177	30	MBX1	M8529YA	MBX1 CCA ALL PAGES CYC H
	170	31	MBX1	M8529YA	MBX1 CCA REQ L
	171	31	MBX1	M8529YA	MBX1 CCA SEL 1 H
	172	31	MBX1	M8529YA	MBX1 CCA SEL 2 H
	174	31	MBX1	M8529YA	MBX1 CSH CCA INVAL CSH H
	175	31	MBX1	M8529YA	MBX1 CSH CCA VAL CORE H
	171	30	MBX2	M8529YA	MBX2 CACHE TO MB 34 H
	172	30	MBX2	M8529YA	MBX2 CACHE TO MB 35 H
	173	31	MBX2	M8529YA	MBX2 CHAN WR CYC L
	176	34	MBX3	M8529YA	MBX3 REFILL HOLD H
	175	35	MBX3	M8529YA	MBX3 SBUS DIAG 3 L
	176	35	MBX3	M8529YA	MBX3 SBUS DIAG CYC L
	173	30	MBX4	M8529YA	MBX4 CACHE TO MB DONE H
	174	30	MBX4	M8529YA	MBX4 CACHE TO MB T2 L
	175	30	MBX4	M8529YA	MBX4 CACHE TO MB T3 L
	176	30	MBX4	M8529YA	MBX4 CACHE TO MB T4 A L
	177	35	MBX4	M8529YA	MBX4 WRITEBACK T2 L
	170	33	MBX5	M8529YA	MBX5 MB REQ IN H
	172	34	MBX5	M8529YA	MBX5 MEM RD RQ IN H
	170	34	MBX5	M8529YA	MBX5 MEM TO C EN L
	175	34	MBX5	M8529YA	MBX5 MEM WR RQ IN H
	177	34	MBX5	M8529YA	MBX5 RQ 0 IN H
	170	35	MBX5	M8529YA	MBX5 RQ 1 IN H
	171	35	MBX5	M8529YA	MBX5 RQ 2 IN H
	172	35	MBX5	M8529YA	MBX5 RQ 3 IN H
	160	22	MBZ1	M8537	MBZ1 CHAN CORE BUSY H
	161	21	MBZ1	M8537	MBZ1 RD-PSE-WR REF L
	161	23	MBZ3	M8537	MBZ3 CHAN MEM REF L
	162	22	MBZ3	M8537	MBZ3 HOLD ERA L
	162	18	MBZ3	M8537	MBZ3 SEQUENTIAL RQ H
	162	23	MBZ4	M8537	MBZ4 NXM T2 H
	160	24	MBZ4	M8537	MBZ4 NXM T6,7 L
	161	18	MBZ6	M8537	MBZ6 CSH PAR BIT H
	105	18	MCL2	M8544	MCL LOAD AR H
	106	18	MCL2	M8544	MCL LOAD ARX H
	107	22	MCL5	M8544	MCL MBOX CYC REQ H
	107	18	MCL2	M8544	MCL STORE AR L
	104	19	MCL2	M8544	MCL VMA USER H
	102	19	MCL1	M8544	MCL1 MEM/ARL IND H
	115	15	MCL1	M8545	MCL1 MEM/REG FUNC L
	103	19	MCL1	M8544	MCL1 REQ EN L
	107	19	MCL2	M8544	MCL2 VMA EXTENDED L
	103	18	MCL2	M8544	MCL2 VMA PAUSE H
	106	19	MCL2	M8544	MCL2 VMA PREVIOUS L
	105	19	MCL2	M8544	MCL2 VMA PUBLIC H

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	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
	102	18	MCL2	M8544	MCL2 VMA READ H
	104	18	MCL2	M8544	MCL2 VMA WRITE H
	105	20	MCL3	M8544	MCL3 PAGE ADDRESS COND H
	106	20	MCL3	M8544	MCL3 PAGE ILL ENTRY H
	102	20	MCL3	M8544	MCL3 PAGE TEST PRIVATE H
	104	22	MCL4	M8544	MCL4 LOAD VMA CONTEXT L
	103	23	MCL4	M8544	MCL4 SHORT STACK H
	102	22	MCL4	M8544	MCL4 VMA GETS AD H
	103	22	MCL4	M8544	MCL4 VMA INC H
	106	21	MCL4	M8544	MCL4 VMAX SEL 1 H
	105	21	MCL4	M8544	MCL4 VMAX SEL 2 H
	102	21	MCL4	M8544	MCL4 XR PREVIOUS H
	102	23	MCL4	M8544	MCL4 XR SHORT H
	106	22	MCL5	M8544	MCL5 18 BIT EA H
	105	22	MCL5	M8544	MCL5 23 BIT EA H
	103	21	MCL5	M8544	MCL5 VMA ADR ERR H
	104	21	MCL5	M8544	MCL5 VMAX EN L
	104	23	MCL6	M8544	MCL6 EBOX CACHE L
	107	23	MCL6	M8544	MCL6 EBOX MAP L
	105	23	MCL6	M8544	MCL6 EBOX MAY BE PAGED L
	104	20	MCL6	M8544	MCL6 PAGE UEBR REF H
	107	21	MCL6	M8544	MCL6 PAGED FETCH L
	106	23	MCL6	M8544	MCL6 REG FUNC H
	107	20	MCL6	M8544	MCL6 VMA FETCH H
	103	20	MCL6	M8544	MCL6 VMA UPT H
NOTE	165	33	MBC4	M8531YA	MEM ADR PAR H
	162	21	MBZ1	M8537	MEM BUSY H
	173	32	MBX3	M8529YA	MEM DATA TO MEM H
	171	34	MBX3	M8529YA	MEM DIAG L
	161	17	MEM5	M8537	MEM PAR IN H
NOTE	166	27	MBC4	M8531YA	MEM RD RQ B H
NOTE	166	28	MBC4	M8531YA	MEM RQ 0 H
NOTE	166	29	MBC4	M8531YA	MEM RQ 1 H
NOTE	166	30	MBC4	M8531YA	MEM RQ 2 H
NOTE	166	31	MBC4	M8531YA	MEM RQ 3 H
	161	19	MBZ1	M8537	MEM TO C DIAG EN L
NOTE	164	29	MBC3	M8531YA	MEM TO C EN L
	173	34	MBX3	M8529YA	MEM TO C SEL 1 H
	174	34	MBX3	M8529YA	MEM TO C SEL 2 H
NOTE	166	33	MBC4	M8531YA	MEM WR RQ L
*	122	0-35	EDP2	M8512	MQ 0 TO 35 H
*	113	20-35	MTR1	M8538	MTR CACHE COUNT 02-17 H
	117	25	MTR3	M8538	MTR CONO MTR, L
*	112	20-35	MTR1	M8538	MTR EBOX COUNT 02-17 H
*	114	24-35	MTR1	M8538	MTR INTERVAL 06-17 H
*	111	20-35	MTR1	M8538	MTR PERF COUNT 02-17 H
*	115	24-35	MTR3	M8538	MTR PERIOD 06-17 H
*	110	20-35	MTR1	M8538	MTR TIME 02-17 H
	116	23	MTR2	M8538	MTR2 ACCT ON H
	116	22	MTR2	M8538	MTR2 EXEC ACCT EN H
	116	21	MTR2	M8538	MTR2 PI ACCT EN H
	116	25	MTR2	M8538	MTR2 TIME ON H
	115	22	MTR3	M8538	MTR3 INTERVAL DONE H
	115	21	MTR3	M8538	MTR3 INTERVAL ON H
	115	23	MTR3	M8538	MTR3 INTERVAL OVRFLO H
	117	22	MTR5	M8538	MTR5 INCR SEL 1 H
	117	21	MTR5	M8538	MTR5 INCR SEL 2 H
	117	20	MTR5	M8538	MTR5 VECTOR REQ H
	160	21	MBZ3	M8537	NXM ACKN H
	160	23	MBZ3	M8537	NXM ANY L
	161	25	MBZ3	M8537	NXM DATA VAL L
	162	25	PAG5	M8537	PAG MB 00-17 PAR H
	160	26	PAG5	M8537	PAG MB 18-35 PAR H
*	15X	13-35	VMA3	M8542	PC 13-35 H **NOTE
NOTE	164	30	MBC3	M8531YA	PHASE CHANGE COMING L
	110	17	PIC3	M8545	PI3 APR PIA 01 H
	110	16	PIC3	M8545	PI3 APR PIA 02 H
	110	15	PIC3	M8545	PI3 APR PIA 04 H
**	116	35	PIC3	M8538	PI3 MTR PIA 01 H
**	116	34	PIC3	M8538	PI3 MTR PIA 02 H
**	116	33	PIC3	M8538	PI3 MTR PIA 04 H
	100	10	PIC1	M8532	PIC1 ACTIVE H
**	101	11	PIC1	M8532	PIC1 GEN 1 H
**	101	12	PIC1	M8532	PIC1 GEN 2 H
**	101	13	PIC1	M8532	PIC1 GEN 3 H
**	101	14	PIC1	M8532	PIC1 GEN 4 H
**	101	15	PIC1	M8532	PIC1 GEN 5 H
**	101	16	PIC1	M8532	PIC1 GEN 6 H
**	101	17	PIC1	M8532	PIC1 GEN 7 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING	BOARD	NAME AND TRUTH
**	100	11	PIC1	M8532	PIC1 ON 1 H
**	100	12	PIC1	M8532	PIC1 ON 2 H
**	100	13	PIC1	M8532	PIC1 ON 3 H
**	100	14	PIC1	M8532	PIC1 ON 4 H
**	100	15	PIC1	M8532	PIC1 ON 5 H
**	100	16	PIC1	M8532	PIC1 ON 6 H
**	100	17	PIC1	M8532	PIC1 ON 7 H
**	100	03	PIC1	M8532	PIC1 PIH1 H
**	100	04	PIC1	M8532	PIC1 PIH2 H
**	100	05	PIC1	M8532	PIC1 PIH3 H
**	100	06	PIC1	M8532	PIC1 PIH4 H
**	100	07	PIC1	M8532	PIC1 PIH5 H
**	100	08	PIC1	M8532	PIC1 PIH6 H
**	100	09	PIC1	M8532	PIC1 PIH7 H
	103	15	PIC2	M8532	PIC2 HONOR INTERNAL H
	103	16	PIC2	M8532	PIC2 READY H
	103	13	PIC2	M8532	PIC2 STATE HOLD H
	103	11	PIC2	M8532	PIC2 TIMER DONE H
	103	12	PIC5	M8532	PIC5 EBUS PI GRANT H
	103	17	PIC5	M8532	PIC5 EBUS REQ H
NOTE	161	33	MBC2	M8531YA	RQ HOLD FF H
	173	35	MBX2	M8529YA	SBUS ADR 34 H
	174	35	MBX2	M8529YA	SBUS ADR 35 H
NOTE	162	31	MBC2	M8531YA	SBUS ADR HOLD H
	136	07	SCD2	M8524	SC .GE. 36 H
**	131	07	SCD2	M8524	SC 00 H
**	131	08	SCD2	M8524	SC 01 H
**	131	09	SCD2	M8524	SC 02 H
**	131	10	SCD2	M8524	SC 03 H
**	131	11	SCD2	M8524	SC 04 H
**	130	07	SCD2	M8524	SC 05 H
**	130	08	SCD2	M8524	SC 06 H
**	130	09	SCD2	M8524	SC 07 H
**	130	10	SCD2	M8524	SC 08 H
**	130	11	SCD2	M8524	SC 09 H
	134	07	SCD2	M8524	SC SIGN H
	133	04	SCD1	M8524	SCAD=0 L
	137	06	SCD5	M8524	SCD ADR BREAK PREVENT H
	137	05	SCD5	M8524	SCD ADR BRK CYC H
	137	02	SCD5	M8524	SCD ADR BRK INH H
	131	03	SCD4	M8524	SCD CRY0 H
	131	04	SCD4	M8524	SCD CRY1 H
	131	06	SCD4	M8524	SCD DIV CHK H
	132	03	SCD4	M8524	SCD FOV H
	130	06	SCD4	M8524	SCD FPD H
	132	04	SCD4	M8524	SCD FXU H
	135	04	SCD5	M8524	SCD KERNEL MODE H
	136	02	SCD5	M8524	SCD KERNEL OR USER IOT H
	134	03	SCD5	M8524	SCD LEAVE USER H
	133	03	SCD5	M8524	SCD LOAD FLAGS A H
	133	06	SCD4	M8524	SCD NICOND 10 H
	131	02	SCD4	M8524	SCD OV H
	133	02	SCD4	M8524	SCD PCP H
	135	06	SCD5	M8524	SCD PRIVATE INSTR EN L
	135	05	SCD5	M8524	SCD PRIVATE INSTR L
	135	03	SCD5	M8524	SCD PUBLIC A H
	135	02	SCD5	M8524	SCD PUBLIC EN L
	134	06	SCD5	M8524	SCD PUBLIC PAGE H
	137	07	SCD4	M8524	SCD TRAP CLEAR L
	130	04	SCD4	M8524	SCD TRAP CYC 1 H
	130	03	SCD4	M8524	SCD TRAP CYC 2 H
**	136	03	SCD3	M8524	SCD TRAP MIX 32 H
**	136	04	SCD3	M8524	SCD TRAP MIX 33 H
**	137	03	SCD3	M8524	SCD TRAP MIX 34 H
**	137	04	SCD3	M8524	SCD TRAP MIX 35 H
	130	05	SCD4	M8524	SCD TRAP REQ 1 H
	130	02	SCD4	M8524	SCD TRAP REQ 2 H
	134	02	SCD5	M8524	SCD USER A L
	134	05	SCD5	M8524	SCD USER EN L
	136	05	SCD5	M8524	SCD USER IOT A H
	136	06	SCD5	M8524	SCD USER IOT EN L
	160	17	SHD1	M8537	SH AR PAR ODD A H
	105	31	SHD1	M8526YA	SH AR PAR ODD H
	106	31	SHD1	M8526YA	SH ARX PAR ODD H
	111	12	SHM1	M8540	SHM1 AR EXTENDED H
	134	12	IRD3	M8522	TEST SATISFIED H
*	15X	13-35	VMA2	M8542	VMA 13-35 H **NOTE
*	15X	13-35	VMA4	M8542	VMA HELD 13-35 H **NOTE
	132	02	SCD4	M8524	VMA HELD OR PC 00 H
**	100	18	MCL3	M8544	VMA HELD OR PC 01 H

KL10(PV/PW) DIAGNOSTIC READ FUNCTION CODES
SORTED ALPHABETICALLY (Cont)

	DF	BIT	DRAWING BOARD		NAME AND TRUTH
**	100	19	MCL3	M8544	VMA HELD OR PC 02 H
**	100	20	MCL3	M8544	VMA HELD OR PC 03 H
**	100	21	MCL3	M8544	VMA HELD OR PC 04 H
**	100	22	MCL3	M8544	VMA HELD OR PC 05 H
**	100	23	MCL3	M8544	VMA HELD OR PC 06 H
**	101	18	MCL3	M8544	VMA HELD OR PC 07 H
**	101	19	MCL3	M8544	VMA HELD OR PC 08 H
**	101	20	MCL3	M8544	VMA HELD OR PC 09 H
**	101	21	MCL3	M8544	VMA HELD OR PC 10 H
**	101	22	MCL3	M8544	VMA HELD OR PC 11 H
**	101	23	MCL3	M8544	VMA HELD OR PC 12 H
**	157	11	VMA4	M8542	VMA PREV SEC 13 H
**	156	11	VMA4	M8542	VMA PREV SEC 14 H
**	155	11	VMA4	M8542	VMA PREV SEC 15 H
**	154	11	VMA4	M8542	VMA PREV SEC 16 H
**	153	11	VMA4	M8542	VMA PREV SEC 17 H
	157	13	VMA1	M8542	VMA1 AC REF A L
	153	15	VMA1	M8542	VMA1 LOCAL AC ADDRESS L
	153	13	VMA1	M8542	VMA1 MISC=0 L
	150	11	VMA1	M8542	VMA1 VMA SECTION 0 L
	157	15	VMA3	M8542	VMA3 MATCH 13-35 H
	151	11	VMA3	M8542	VMA3 PC SECTION 0 L
	152	11	VMA4	M8542	VMA4 PCS SECTION 0 L

KL10 PV/PW CROSS REFERENCE CHART
DIAGNOSTIC READ FUNCTION CODES

PV	PW	
M8514	M852	CHA
M8515	M853	CHX
M8518YA	M854	PMA
M8520YA	M855	PAG
M8521	M856	CHD
M8531YA	M857	MBC

NOTE

TRACON and the 11-based 10 diagnostic programs interpret all diagnostic read functions which are not preceded with either a single or double asterisk [(*) or (**)] as single bits; as such, they are printed out by bit position and/or name. Diagnostic read functions preceded by a single asterisk (*) are interpreted as registers and are printed out as such. Diagnostic read functions which are preceded by a double asterisk (**) may be interpreted and printed as either single bits or as a register depending on the program doing the interpretation.

KL10 DATA PATH PARITY NETWORKS

There are very few places in the KL10 system that generate parity. Generally, once parity is generated, it is passed from component to component and checked for errors in the process. This reduces the chance of having undetected errors. The KL10 system has two parity generation (PG) networks: one is at the output of the arithmetic register (AR); the other is at the output of the channel status words. Proper parity is generated when data leaves the AR to go to cache, to fast memory, to the EBus, or to the memory buffer. This parity remains with the data in cache, fast memory, the EBus, and the memory buffer.

There are instances where the data paths must decrease from 36 bits to 18 bits, or increase from 18 bits to 36 bits. In these cases, parity folding generation occurs. As an example, when data passes from the memory buffer to the input side of the page table, there is a conversion from 36 bits to 18 bits (and proper parity is generated to check each 18 bits). Conversely, as data passes from the RH20 to the channel, there is a conversion from 18 bits to 36 bits (because the RH20 deals with 18-bit entities and the channel deals with 36-bit entities).

In addition to the two parity generation networks, there are six parity checking networks in the major data path of the system. These parity checking networks are as follows.

- On the memory side of the DMA20 - Parity is checked on data as it is received from memory and enters the DMA20, and as it leaves the DMA20 and goes through the KBus to memory.
- At the output of the memory buffer (MB) registers - Parity is checked when data leaves a memory buffer for any of the following: memory, the hardware page table, channel, cache, AR, or the arithmetic register extender (ARX).
- At the output side of the page table - Parity is checked as data comes out of the hardware page table.
- On the device side of the RH20 - Parity is checked as data travels the Massbus from the mass storage device to the RH20. Parity is also checked as data leaves the RH20 and is put on the Massbus to go to the mass storage device.
- On the AR - It checks the data arriving at the AR from memory.
- On the ARX - It checks data arriving at the ARX from

There are three other parity checking networks in the system. One is on the output of fast memory. It checks stored parity and data coming from fast memory. The other two are on the output of the CRAM and the output of the DRAM. For both of these, parity is checked on each word before the microword controls use it.

APR ERROR STATUS REGISTER

Internal devices (CONO APR and CONI operations) allow enabling, disabling, setting, and clearing of eight error conditions. These eight error conditions (bits 24-31) are SBus, nonexistent memory, I/O page fail, MB parity, cache directory, address parity, power failure, and cache sweep done. Four bits (20-23) in the CONO word indicate whether to enable, disable, clear, or set the selected flags. (Bits 24-31, the eight error conditions, are used for the selected flags). Bit 32 is set to 1 to indicate that one of the selected flags is true. Bits 33-35 are the priority interrupt level bits for the APR device. Bits 6-13 of the CONI word indicate which of the selected flags are enabled. When CONI bit 19 is set to 1, the cache sweeper is busy. When CONO bit 19 is set to 1, all the I/O in the system is reset.

ERROR ADDRESS REGISTER - ERA

The error address register, or ERA, is an internal register in the MBox. This register contains the last address requested of the memory system. It also contains the flags that indicate what type of operation (read, write, etc.) has been requested. Until an error occurs, the ERA register is changing with every address that is being sent by the MBox to the memory system for reading or writing. When an error occurs, the ERA register latches at the

last address sent by the MBox to the memory system. The ERA remains latched until the software is able to correct the error address and until the error address is recorded in the system error log for field service.

As mentioned previously, there are eight error bits in the APR error status register. Three of these error bits indicate to the software (upon an interrupt to the APR) that the ERA register contains error information. These three error bits are: bit 25 (Nonexistent Memory Error), bit 27 (MB Parity Error), and bit 29 (SBus Address Parity Error). The software reads the contents of the ERA register, using the appropriate internal device code (BLKI PI), and clears the three error bits in the APR register. When the error bits are cleared, the ERA register is again ready for a subsequent error.

Layout of the ERA Register

When the MBox makes a reference to memory, it requests four words at a time: the word that the EBox needs is requested first and the other three follow in quick succession. Bits 0-1 indicate in which of the four words the error occurred (note that word numbers are in physical, not chronological order). Bits 2-6 identify the reference to memory. Bit 2 is the Clear Cache Reference bit. It equals 1 when the memory error occurred while the cache was sweeping. Bit 3 is the Channel Reference bit. It equals 1 if the error occurred when the channel was making a refernce to memory. Bits 4 and 5 comprise a data source code that indicates where, in the MB, the data originated. Data may come from: memory on a read or a read-pause-write, the channel on a storing status (writing into memory), the AR on an EBox write, cache on a page refill or channel read operation, cache on a write operation to memory. The data source field is not valid on an address parity error. Bit 6 is the write reference bit. It equals 1 if a memory write operation was in progress when the error occurred.

Bits 14-35 contain the physical address that the EBox requests from the MBox. If the reference requires only a single transfer, that address is the error address. If the reference triggers a group transfer, then bits 14-35 are the address of the first reference chronologically in the group.

SBUS DIAGNOSTIC CYCLE

The SBus diagnostic cycle is used to communicate between the MBox and the internal memory controllers. Because there are no switches associated with the internal memory controllers, functions such as address boundaries, interleave mode, margining, etc., are controlled using the diagnostic cycle. The processor initiates the diagnostic cycle when it gives the instruction to send a function word to a particular controller and to receive an error word and diagnostic information back from it. The MBox executes the diagnostic cycle and uses 36 SBus data lines to transfer information. A macroinstruction, BLKO PI, (700500) takes a 36-bit input argument and returns a 36-bit output argument. The microcode for this instruction puts the 36-bit input argument in the AR and tells the MBox to execute an SBus diagnostic cycle. When the MBox turns on its response signal, the microcode clocks the contents of the cache data lines into the AR and returns the information as the output argument.

Layout of the SBus Diagnostic Cycle

There are two halves to the SBus diagnostic cycle: the first is "to memory" (700500) and the second is "from memory" (E+1). Also, for each controller (DMA20, MA20, MB20), there are two function codes: 00 and 01.

SBus Diagnostic Cycle, "To Memory", Function 00

Bit(s)	Name	Description
0-4	Controller Address	Bits 0-4 specify with which controller the MBox is communicating. Bits 0-3 specify the internal controllers: MA20 or MB20. Bit 4 specifies the external controller: DMA20. This is true for both function 00 and function 01.
5	Clear Error	If bit 5 is set to 1, then the error-reporting flags (bits 0-4, "from memory" function 00) are cleared.
6-7	Bus Mode (DMA20) Interleave Mode (MA20/MB20)	
8-11	SBus Request Enables (MA20/MB20)	The SBus Request Enables bits assign odd or even status to the controller for interleave modes.
12	Load 6-7 (DMA20) Load 6-11 (MA20/MB20)	
31-35	Function Code	

SBus Diagnostic Cycle, "To Memory", Function 01

Bit(s)	Name	Description
0-4	Controller Address	
12	Loopback	
14-17	SBus Address (MA20/MB20)	
18-21	Low Address Boundary (MA20/MB20)	Bits 18-25 act in conjunction with the memory address (bits 14-17) to specify lower and upper address limits
22-25	High Address Boundary (MA20/MB20)	
26	Load 14-25 (MA20/MB20)	Bit 26 enables the loading of bits 14-25. If bit 26 is set to 0, it reads bits 14-25. If it is set to 1, it loads and reads back.
27-30	Select Margins (MA20/MB20)	Bits 27-30 control the amount of current, strobe, and threshold. When all bits are not set, the margin control is nonoperational. If bit 30 is set, all margins are cleared. If bit 29 is set, the current margin is operational. If bit 28 is set, the strobe margin is operational. If bit 27 is set, the threshold margin is operational. If bit 30 is set for either current, strobe or threshold, the margin is high. If bit 30 is not set, the margin is low.
31-35	Function Code	With bit 35 set, the function code equals 01.

SBus Diagnostic Cycle, "From Memory", Function 00

Bit(s)	Name	Description
0-1	(for expansion)	
2	Incomplete Cycle (NXM on DMA20)	Bits 2-5 are error-reporting flags in the memory controllers. If bit 1 is set in the "to memory" half of the cycle, then these error reporting flags are cleared.
3	Read Parity Error (DMA20)	
4	Write Parity Error (DMA20)	
5	Address Parity Error	
6-7	Bus Mode (Interleave Mode on MA20/MB20)	Setting bits 6-7 to 00, in either controller, indicates off-line mode.
8-11	Last Request (DMA20)	Bits 8-11 ask: In what quad word did the failure occur?
12-13	Last Type (DMA20)	Bit 12 is the read request and bit 13 is the write request.
14-35	Address or First Address of Error (DMA20)	

SBus Diagnostic Cycle, "From Memory", Function 01

Bit(s)	Name	Description
0-7	Storage Modules Installed (DMA20)	These bits indicate the number of storage modules connected to a controller. Setting a particular bit indicates the presence of a storage module.
4-7	Storage Modules Installed (MA20/MB20)	
8-11	Controller Type	Bits 8-11 identify the memory type.
12	Loopback	
14-17	SBus Address (MA20/MB20)	
18-21	Low Address Boundary (MA20/MB20)	Bits 18-25 indicate the address boundaries located in the "to memory" half of function 1.
22-25	High Address Boundary (MA20/MB20	
30	Margin On (MA20/MB20)	Bit 30 indicates that the current, strobe, or threshold margin control is on.
32-35	Requests Enabled (MA20/MB20)	

DESCRIPTION OF SBUS ERRORS

MA20/MB20

Incomplete Cycle - Occurs on a read-pause-write (RPW) cycle when the processor fails to send valid data to the memory to initiate the write portion of the RPW cycle. It also occurs on any cycle that the memory fails to complete before the 8.0 us timeout. The MA20/MB20 signals the occurrence of this error by sending an SBus error to the processor.

Address Parity Error - Can occur at the start of any memory cycle. The MA20/MB20 signals the occurrence of this error by sending the SBus address parity error to the processor. Thus, the processor is notified of the occurrence of the error within 125 us. The address that the processor was attempting to reference when the error occurred becomes latched in the ERA register. An address parity error flag is set in the MA20/MB20 to indicate the occurrence of this error.

DMA20

Data Parity Error - Both read and write are checked in the DMA20 during the three types of memory cycles. Each type of parity error sets appropriate flags in the status register. The error detection logic stores the address of the first error in the error address register until the associated error bit is cleared. A cumulative error signal (SBus error) is sent to the MBox. On a write cycle, the error signal may not arrive at the processor until 500 us after the last word arrives. On a read cycle, the error signal may not arrive at the processor until 250 us after the last word arrives. The DMA20 signals the occurrence of this error by sending an SBus error to the processor.

Address Parity Error - Can occur at the start of any memory cycle. The DMA20 signals the occurrence of this error by sending the SBus address parity error to the processor. Thus, the processor is notified of the occurrence of the error within 125 us. The address that the processor was attempting to reference when the error occurred becomes latched in the ERA register. An address parity error flag is set in the DMA20 to indicate the occurrence of this error. The address that the DMA20 receives at the time of the error is latched in the DMA20 error address registers.

NOTE

The address parity is only checked for SBus addresses and does not include KBus addresses.

NXM Error - If an acknowledge (ACK) is received from the first storage module, and any subsequent reference in the cycle does not receive an ACK (i.e., a storage module did not respond), then a nonexistent memory (NXM) flag is set in the DMA status register. The DMA20 error address register becomes frozen in the same way as an address or data parity error. The timeout for this error is 28 us. The processor is notified immediately after the timeout when the DMA20 sends SBus error.

MBOX

SBus Error - When the MBox sees the SBus error from the MA20/MB20 or DMA20, it sets the SBus error APR flag in the EBox. No valid information is held in the ERA on occurrence of this error.

SBus Address Parity Error - When the MBox sees the SBus address parity error from the MA20/MB20 or DMA20, the MBox sets the SBus address parity error flag in the APR status register. The ERA register in the MBox is latched when the error is detected. It does not unlatch until the software clears the APR flag after having copied the data out of the ERA.

Data Parity Error - The parity of all data leaving the MBs is checked. If the parity is incorrect, the address of the location is referenced: an 8-bit code indicating the source of the data, and two bits indicating the MB that held the bad word are held in the ERA. This information is held until the MB parity error flag in the EBox (APR status word) is cleared.

Page Table Parity Error - Forces a page fail trap (code is 25). The error is the result of either memory, cache data parity error on a page refill, or a fatal error on the hardware page table. If there is a fatal error on the hardware page table and it is a solid failure, then the hardware page table is unusable.

Cache Directory Parity Error - When a parity error is detected in the cache directory, a flag is set in the APR register. The cache is effectively turned off at the end of the current memory reference and remains "off" until the cache directory parity error flag in the APR status register is cleared. This error is nonrecoverable by the KL10 software, but the PDP-11 is able to scan the cache in a diagnostic mode and turn off the affected cache before monitor reload (if the error is reproducable).

NXM Error - An error flag is set in the APR register when a nonexistent memory location is addressed. During a read from memory, the MBox supplies four words of zeros to the EBox that has bad parity. The EBox gets a data parity trap. During a write to memory, the data in the MBs is discarded. The ERA register in the MBox is latched when this type of error occurs.

EBOX

AR/ARX Parity Error - Parity is checked on all data that enters the AR/ARX for use by the EBox. If a failure is detected, a page fail trap which has a code of 36/37 occurs.

EBus Parity Error - All words that enter the AR/ARX from the EBus are checked for parity if the parity was generated by the transmitting device. If an error is detected, an I/O page fail interrupt occurs, and the monitor is able to determine that the bad data was received from the EBus.

Fast Memory Parity Error - Each word stored in fast memory generates odd parity as it leaves the AR. If the fast memory word is read out through the Adder B (ADB) mixer, parity is checked. If an error is detected, and if fast memory parity checking is enabled by the console processor, then the EBox clock is halted.

CRAM and DRAM Parity Errors - Odd parity is generated by the microcode assembly program for each word stored into the CRAM and DRAM. This is done each time these RAMs are loaded. When a word in either RAM is referenced, odd parity is checked. If an error occurs and the halt on the error diagnostic function is enabled, the EBox clock is halted.

RH20

Data Parity Error - Occurs when the RH20 detects bad parity on a data transfer from the device. If disable transfer error stop is set, the transfer will continue after a status flag is set. If the disable transfer error stop is not set, the EXC is set and an interrupt is sent to the EBox.

SUMMARY OF PARITY ERRORS

There are two ways in which the software recognizes parity errors.

1. The Trap Method - A trap is an interruption of the instruction sequence of the CPU caused by an attempt to execute that instruction. Control passes to a trap routine that attempts to solve the problem. When a trap occurs, the software retries and if the error does not repeat, then there is a successful recovery. There are two types of page fail traps: page table parity error (code 25), and AR/ARX data parity error (code 36/37).

2. An Interrupt on the APR - Interrupts differ from traps in that they are usually caused by an external activity. In many cases, the software is unable to recover by retrying. In other cases, such as channel errors, the software is able to recover by retrying the I/O operation. In all cases, core memory is reviewed by the sweep instruction in the search for and the recording of more errors.

Address Parity Errors
Address parity errors are detected by the MA20/MB20 or the DMA20 on a read, write, or read-pause-write. Address parity is a way of checking the bus and drivers that exist between the MBox and the MA20/MB20 or the DMA20.

MA20/MB20 Response
When, during a read, the MA20/MB20 detects an address parity error on the address lines coming from the MBox, the MA20/MB20 returns four words of zeros with bad parity to the MBox. The bad parity is detected throughout the system by the parity network. Thus, parity is never regenerated, but is simply checked along the way, at each level. During a write from the MBox to the MA20/MB20, the controller throws away the data. The MA20/MB20 does not write the data into memory because it is not clear into which address it should be written, since there is a parity error in the address.

DMA20 Response
The DMA20 does not respond to the MBox if an address parity error occurs during a read and a write. Instead, the MBox does a timeout and gives a normal nonexistent memory interrupt to the CPU on the APR. The DMA20 does not attempt to read or write memory, but it always checks all addresses on the memory bus, whether the addresses are intended for the MA20/MB20 or the DMA20. Therefore, the DMA20 may send an address parity error condition to the CPU via SBus address parity error, even if the address is intended for the MA20/MB20.

Nonexistent Memory (NXM)
The ERA register is valid when a nonexistent memory error occurs and an APR interrupt is caused. A NXM error is detected by the MBox because there is no response from the MA20/MB20 or the DMA20 after 64 us. The software determines which word received the NXM and the source of the request. If address parity error is also set, the error is an address parity error, not a NXM error. That is, the DMA20 does not respond to an address if there is a parity error in the address. Because of the lack of response, after the 64 us period, the MBox concludes that there is a NXM. Consequently, the software should be aware of what the real failure is when both NXM and address parity errors are indicated in the APR error status word. If the MBox reads from the memory when the NXM occurs, the MBox will supply four words of zeros, with bad parity, to the EBox so that the EBox gets a data parity trap when it uses the data. The software checks to see if the address being referenced is in bounds, i.e., does the address exist where the software expects it to exist. If it does, the software retries as if a data parity error occurred. This retry procedure is programmed in the parity trap routine and occurs because the EBox detects a parity error on the NXM condition. Note that an APR interrupt also occurs with the ERA latched to the error word. Thus, software logs the error in the APR interrupt routine.

On a write to memory, and on a NXM, the data in the MBs is lost. However, everything in the ERA register is valid.

Another form of NXM error occurs in the DMA20. It occurs if the first word requested by the MBox is acknowledged. However, if one of the subsequent three words does not send back an acknowledgement within 28 us, a NXM condition is indicated to the software via an SBus error interrupt on the APR, instead of via an NXM error interrupt on the APR. The DMA20 remembers the address of the specific word that received a NXM condition. The software reads this address from the DMA20 by using the SBus diagnostic function. In this case, the ERA is not valid.

CRAM and DRAM Parity Errors
Odd parity is generated by the microcode assembly program for each word stored into the CRAM and DRAM. This is done each time the RAMs are loaded. When a word in either RAM is referenced, odd parity is checked. If an error occurs and the halt on error diagnostic function is enabled, the EBox clock is halted. The PDP-11 must detect this and save the entire internal hardware state of the machine by using diagnostic functions. This information is included in the system error file, and presented, in a condensed form, on the operator's console.

The error-recording overlay in the front-end processor validates the associated RAM. A copy of the "good" contents (from a disk file) is compared with the contents of the RAM.

Fast Memory Parity Error
Odd parity is generated as each word stored in fast memory leaves the AR. Parity is checked if the fast memory word is read out through the ADB mixer. The EBox clock halts if an error is detected and if the halt function is enabled by the console processor.

EBus Parity Error
The AR parity tree generates odd parity for all DATAO and CONO words that are destined to be output on the EBus. All devices may check this parity. The DTE20 checks parity on DATAO operations, but not on CONO. All devices may not generate odd parity for all words that are transmitted to the EBox over the EBus. The appropriate EBus signal is generated by the device to indicate that parity has been generated.

If parity is generated by the transmitting device, then all words entering the AR/ARX from the EBus are checked for correct parity. If an error is detected, an I/O page fail interrupt occurs and the monitor determines that the bad data was received from the EBus. The information collected for error reporting should be the same as for other occurrences of the same APR interrupt.

Note that a PDP-11 deposit to KL10 memory causes parity interrupt. This has nothing to do with the KL10 instruction being executed. This interrupt should be treated like an interrupt by the KL10 monitor. Continue all parity traps. The KL10 monitor tells the PDP-11 that the deposit failed, and the KL10 logs the failure in the log file.

NOTES

RP20 INLINE ROUTINES
Refer to STC 8350/8650 Disk Inlines Reference Manual (ER-91392-RM).

The various types of RP20 inline routines are listed below.

Linked Series

C1 Control Module Tests
C2 Drive Interface Tests
C3 Basic Servo Tests
C4 Index and Sector Tests
C5 Gap Counter Tests
C6 Basic Read/Write Tests
C7 Padding Tests
C8 ECC Logic Tests
C9 Reorient Counter, TR Counter Tests
CA Complex Servo Tests
CB Read/Write Reliability
CC* Read/Write Margin
CD AM Detection Tests
CE Overwrite Test
CF Reformat FE Tracks

Servo Utilities

D8 Servo Adjustment
D9 Incremental Seek Test
DA Cylinder Seek Test
DB Random Seek Test
DC Pumped Resonance
DD Crash Stop Test
DE On Track Servo Test

General Utilities

E0 Sync Utility
E1 Read Test
E2 Display HA Utility
E6 Display Memory
E7 Memory Scan
E8 FE Panel Test
E9 HDA State Analysis
EA Display Sense Data
EB TAG Utility
EC String Switch/Dual Path
EE Manual Intervention Test

Skip Handling Routines

F2* Track Analysis Utility

RP20 Inline Operating Instructions
Refer to STC 8350/8650 Disk Inlines Reference Manual - Chapter 1

Enter Parameters
Refer to STC 8350/8650 Disk Inlines Reference Manual - Chapter 1

Select Run Options
Refer to STC 8350/8650 Disk Inlines Reference Manual - Chapter 1

Displaying Errors/Messages
Refer to STC 8350/8650 Disk Inlines Reference Manual - Chapter 1

Display Message Bytes
Refer to STC 8350/8650 Disk Inlines Reference Manual - Chapter 1

RP20 Microdiagnostic Loading Procedures (Control Unit Microdiagnostics) - Hardcore Routines
Refer to STC 8000-2 Maintenance Reference Manual (MRM) (ER-80002-RM), Entry S000

*Not supported on Digital-formatted packs.

Table 1 Inline Display Summary*

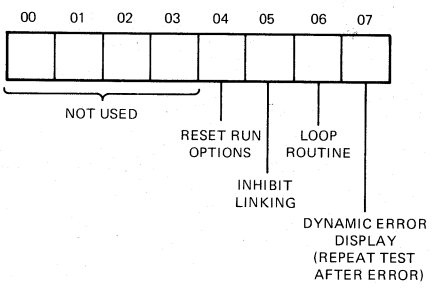
PROGRAM CONTROL DISPLAY (Hex)	Description	DATA DISPLAY
82	The routine specified in the DATA ENTRY switches is now loading.	Routine Number
8C	The Inline (routine series, routine, or test) is running.	Routine Number
8D	Dynamic Error Display. Errors are displayed as they occur, but execution is not stopped because of the dynamic error display run option.	Error Number
C0	An invalid routine number was set in the DATA ENTRY switches, or an incorrect Inline floppy is installed.	Routine Number
	The routine execution was interrupted by a system or elective reset. Restart the Inline.	00
	The Inline monitor has accepted a 5X or 4X entry from the data entry switches	5X or 4X
CA	Inline is ready for execution.	Routine Number
CE	Routine stopped because manual intervention is required or the error or message display is complete.	Routine Number
CF	Normal end of routine or end of series of linked routines.	Routine Number
	Normal end of control option 30, and fault symptom code generator overlay complete.	30
DX	Parameter entry required. Bits 4 through 7 of the PROGRAM CONTROL DISPLAY indicate a parameter byte is needed.	Routine Number
E1 or EX	Error or Message Stop. If bits 0 through 7 of the PROGRAM CONTROL DISPLAY show E1, it indicates that the first error message byte is shown in the DATA DISPLAY indicators. If control option 20 is used to display additional bytes, bits 4 through 7 of the PROGRAM CONTROL DISPLAY indicate the byte numbers displayed in the DATA DISPLAY indicators.	Error Number or Message Byte
FX	An error was detected by the DCU. Verify: 1. The proper Inline floppy disk is installed. If the disk is not correct or not properly installed, reinstall the correct disk and reissue the previous command. 2. Floppy disk reader door is securely closed. Refer to the 8000-2 MRM if the correct disk is installed and an FXXX error occurs. NOTES 1. Routine D8 has an FX display. Refer to instructions for running D8 in the Routine Listings in Chapter 4 of the 8000-2 MRM. 2. Routines D8 and E0 generate displays to both sets of FE indicators. Refer to instructions for running these routines in the Routine Listings in Chapter 4 of the 8000-2 MRM.	N/A

Table 2 Control Options*

Option	Description
00	Start/Stop Starts (or resumes) execution if the routine stopped. Stops execution if the routine is running or if error message display is in progress.
10	Parameter entry control
20	Start of advance error or message display
30	Reset diagnostic control Control option 30 must be selected with the functional microprogram disk installed before returning the subsystem to the customer. The purpose is to reload the fault symptom code generator into the diagnostic overlay area. If control option 30 is selected: 1. PROGRAM CONTROL/DATA DISPLAY should then display CF30 to indicate reload completion. 2. With no disk installed, an FXXX error occurs. To recover, insert the disk in the reader and reissue the 30 command. 3. If the correct disk is installed and an FXXX error occurs, refer to the 8000-2 MRM.

Table 3 Run Options*

DATA ENTRY Switches (Hex)	Description
01	Dynamic error display. Repeat test after error. Can be used when looping test.
02	Loop routine. All routines linked to looped routine also run.
03	Dynamic error display and loop routine.
04	Inhibit routine linking. Runs only the routine selected.
05	Inhibit routine linking, dynamic error display. Repeats routine after error.
06	Loop single routine (inhibit linking).
07	Loop single routine (inhibit linking) and dynamic error display.
08	Reset run options (allows linking, no looping, and error stops as if no run options were selected).



RP20 Fault Symptom Codes‡

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
1000	False Device Interface Check	A07* J03 J04 J09 J10	C08 C08	IV-3
1001	Device Interface Check - TAG BUS PAR CHK	A07* J03 J10	C07	IV-7
1002	Device Interface Check - BO PAR CHK	A07* J03 J10	C03 C06 C07 C08	IV-20
1003	Device Interface Check - TAG BUS and BO PAR CHK	A08 J03 J04 J09 J10	C07 C08 C09/10	IV-2
11FF	HDA Mode Parity Check This indicates that either multiple or no format mode was detected.	A02** A08† A01** A07* A06 A04 A05	J04 J09	IV-10
11XX	HDA Sequence Check - This indicates an initial status problem was detected during the sequence from state 0 to state 6 (READY), or a run status problem was detected while in state 6.	A02** A08† A01** A07* A06 A04 A05		IV-1
1200	Timeout Check During Recalibrate State 0 - Move Out	A06 A01** A02** A04 A05 A08†		Par. 6.84
1201	Timeout Check During Recalibrate State 1 - Reset	A02** A08† A06 A04 A05 A01**		Par. 6.84
1206	Timeout Check During Rezero State 6 - Rezero Linear Mode	A01** A02** A06 A04 A05 A08† PA Card**		Par. 6.84
1208	Timeout Check During Seek State 8 - Decelerate	A02** A01** A04 A05 A06 PA Card**		Par. 6.84

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
†Before replacing, check K631 (K641) for shorted coils.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
120A	Timeout Check During Seek State A - Accelerate	A02** A01** A04 A05 A06 PA Card**		Par. 6.84
120C	Timeout Check During Seek State C - Seek Linear Mode	A02** PA Card** A01** A04 A05 A06 A06		Par. 6.84
120E	Invalid Timeout Check During Seek State E - On Track	A06 A01** A02** A04 A05 A08†		Par. 6.84
1210	Timeout Check During Rezero State 10 - Move Out	A01** A14 A05 A06 A02** A08† A07* PA Card**		Par. 6.84
1212	Timeout Check During Rezero State 12 - Turn Around	A06 A02** A01** A04 A05 A08† PA Card**		Par. 6.84
1216	Timeout Check During Rezero State 16 - Move In	A01** A08† A06 A02** A05 A07* PA Card**		Par. 6.84
12XX	Timeout Check During an Invalid Control State	A06 A07* A08† A05		Par. 6.84
1301	Sector Non Comp (Sector Compare) - This indicates that a sector compare was not received within two index marks (one complete revolution of the disk).	A01** A06 A07 A08†	J04 J09	IX-14
1310	False Drive Check - This indicates that drive check occurred without a sector compare or access check.	A01** A04 A05 A06 A10* A08†	C07 C08 C09/10 C11 (C12) J07 J03	IX-14
1400	False Read/Write Check Sense Bytes 12 and 19 (EA Message Bytes 8 and 15)	A04 A05 A07*		VIII-1/2

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
†Before replacing, check K631 (K641) for shorted coils.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
1401	Write I Check	A04 A05 A07*		VIII-1/2
1402	Transitions Check	A04 A05 A07*	C01 C06 C05 C03 C04	VIII-1/2
1404	Control Check	A04 A05 A07*	C08 C06 C11 (C12)	VIII-1/2
1408	Delta I/W Check	A04 A05 A07*	C06	VIII-1/2
1410	Index Check Select	A04 A05 A07*		VIII-1/2
1420	Write Overrun Latch	A04 A05 A07*	C05 C05 C08 C11 (C12)	
1440	Capable Enable Check	A04 A05 A07*		VIII-1/2
1480	Multichip Check	A04 A05 A07*		VIII-1/2
14F4	Pad Gate Error 5	A04 A05 A07*		VIII-1/2
14F8	Head Short Latch	A04 A05 A07*		VIII-1/2
14XX	Multiple Read/Write Checks	A04 A05 A07*		VIII-1/2
1500	Overshoot Check During Rezero	A06 A02** A01** A04	G3‡ G5‡ G6‡	Par. 6.84
1506	Recalibrate - Track 0 Overshoot Check	A05 A08† PA Card**	G3‡ G5‡ G6‡	Par. 6.84
1508	Overshoot Check During Seek State 8 - Decelerate	A01** A04 A05 A06 A02** A07* PA Card**	G3‡ G5‡ G6‡	Par. 6.84
150A	Overshoot Check During Seek State A - Accelerate	A02** A06 A05 A01** PA Card**	G3‡ G5‡ G6‡	Par. 6.84

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
†Before replacing, check K631 (K641) for shorted coils.
‡Cable Groups. See Table 6.3A in STC 8650 MRM.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
150C	Overshoot Check During Seek State C - Linear Mode	A06 A04 A05 A02** A01** A07* PA Card**	G3‡ G5‡ G6‡	Par. 6.84
150E	Overshoot Check - Lost Servo Track Following	A06 A02** A01 A04 A05 PA Card**	G3‡ G5‡ G6‡	Par. 6.84
1510	Overshoot Check During Rezero	A06 A02** A01** A04 A05 PA Card**	G3‡ G5‡ G6‡	Par. 6.84
1512	Overshoot Check During Rezero	A06 A02** A01** A04 A05 PA Card**	G3‡ G5‡ G6‡	Par. 6.84
1516	Overshoot Check During Rezero	A06 A02** A01** A04 A05 PA Card**	G3‡ G5‡ G6‡	Par. 6.84
15XX	Overshoot Check During an Invalid State	A06 A02** A01** A04 A05 PA Card**	G3‡ G5‡ G6‡	Par. 6.84
160E	Servo Off Track Error During Track State	A06 A02** A01** PA Card**		
16XX	Servo Off Track Error - during an invalid control state or set read/write active during access motion	A06 A07* A04 A05 A08+ A02**	C07 C08 C11 (C12) C09/10 G0 G1 G3 G5 G6	Par. 6.84
1910	Error Alert	CJ06,CJ08 CJ05,CJ07 J110,J111 J112,J113 J114,J115 J116,J117	C11 (C12) C07 C08 C09/10	III-8
1911	Transmit Target Error	A01** A06 A07* A08+ A04 A05		IX-17

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
+Before replacing, check K631 (K641) for shorted coils.
‡Cable Groups. See Table 6.3A in STC 8650 MRM.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
1912	Microprogram Detected Error (detailed information is in sense byte 18)			Par. 5.22
1913	Difference Counter or HAR (head address register) Failed to Reset on a Rezero Operation	A05 A06 A07* A08† G0,G1‡	C07 C08 C09/10 C11 (C12)	IV-14/16
1914	Sync Out Timing Check	G9‡	C03 C04 C06 C07 C08 C09/10 C11 (C12)	V-36
1915	Unexpected File Status at Initial Selection	A07(B07)* A06 A01** A04 A05 A08† A02**	C07 C08 C11 (C12) C09/10	Par. 6.14
1916	Transmit CAR (cylinder address register) Error	A05 A07*	G0‡ G1‡ G7‡ G8‡ G9‡	IV-10
1917	Transmit HAR Error	A05 A07*	G0‡ G1‡ G7‡ G8‡ G9‡	V-14
1918	Transmit Difference Counter Error	A05 A06 A07*	G0‡ G1‡ G7‡ G8‡ G9‡	IV-16
1919	Unexpected File Status During Read IPL		G3‡ G5‡ G6‡	Par. 6.5
191A	Seek Verification Check	A02** A01** A06 A04 A05 A07* PA Card**	C07 C08 C06 C11 (C12) G3‡ G5‡ G6‡	Par. 6.136
191B	Sector Compare Check if byte 9, bit 1 is on (EA message byte 5, bit 1) Timeout Check if byte 16, bit 0 is on (EA message byte 9, bit 1) Overshoot Check if byte 16 bit 1 is on (EA message byte 9, bit 0)			Par. 6.91

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
†Before replacing, check K631 (K641) for shorted coils.
‡Cable Groups. See Table 6.3A in STC 8650 MRM.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
191C	No Interrupt From Drive (Missing Device Attention)	A02** A06		IV-19
191D	Defective Skipping Reorientation Error			V-47
191E	Unable to Determine Device Format Mode	A07* A05 A08†	C08 C04 C11 (C12) C09/10	IV-23
191F	Retry Orientation Check	G0‡ G1‡ G8‡	C01 C07 C04	V-54
4940	ECC Data Check - HA Field	A03(B03) A04 A05 A07* A06	C05 C03 C07 C01	Par. 6.149
4941	ECC Data Check - Count Field	A03(B03) A04 A05 A07* A06	C01 C03 C04 C05 C06	Par. 6.149
4942	ECC Data Check - Key Field	See FSC 4941		Par. 6.149
4943	ECC Data Check - Data Field	See FSC 4941		Par. 6.149
4944	No Sync Byte Found - HA Field	A03 A04 A05 A06 A07* A08	C03 C04 C01 C07 C05	Par. 6.148
4945	No Sync Byte Found - Count Field	See FSC 4944		Par. 6.148
4946	No Sync Byte Found - Key Field	A03 A05 A06 A07* A08†	C03 C04 C01 C06 C05	Par. 6.148
4947	No Sync Byte Found - Data Field	See FSC 4946		Par. 6.148
4949	No AM Found During Retry - When reorienting on the failing record during a retry operation, an address mark was not detected.	A03 A04 A05 A06 A07*	C03 C04 C01 C05 C06	Par. 6.150
9001	Missing Tag Valid on Read/Write Operation	A07* A06 G7‡ G8‡ GA‡ G1‡	C06 C01 C03 C04	III-12

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
†Before replacing, check K631 (K641) for shorted coils.
‡Cable Groups. See Table 6.3A in STC 8650 MRM.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
9002	Normal or Check End Missing Following Read/Write or ECC Operation	G7,G8‡, GA,G1‡	C06 C05 C03 C04 C01 C07 C08 C09/10 C11 (C12)	III-25
9003	No Response from Control Module on a Control Operation	A07* G7,GB‡ GA,G1‡	C06 C03 C07 C08 C09/10 C11 (C12)	IV-20
9004	Timeout Waiting For Index	A04(B04) A05 A07* A01** G0,G7‡ G8,G1‡ GC,G9‡	C06 C08 C11(C12) C05 C02 C03 C04 C07	IX-12
9005	ECC Hardware Check	A05 A06 A07* A08‡ G0,G7‡ G8,G1‡ GC,G9‡	C06 C04 C07 C08 C05	V-22
9006	Multiple Controllers Selected	G0,G7‡ G8,G9‡	C08 C11 (C12) C07 C09/10 C04	III-2
9007	Preselected Check	G0,G7‡ G8‡	C04 C07 C08 C09/10 C11 (C12) C05 C06 C02 C03	III-2
9008	Repetitive Command Overruns on G1 Operations	G0,G7‡ G8‡	C06 C04 C05 C07 C08 C11 (C12)	V-32
9009	Repetitive Command Overruns on G2 or G3 Operations	A07*	C08 C11 (C12)	V-38
900A	Physical Address Check - incorrect physical address returned after a drive selection	A07*	C07 C08 C09/10	IV-2

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
‡Cable Groups. See Table 6.3A in STC 8650 MRM.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
900B	Busy Missing After Seek Start Is Issued	A06 A07* A04 A05 A02** A01**	C08 C11 (C12) G0‡ G3‡ G5‡ G6‡	VII-18
900E	Device Interface Failure	A05 A06 A07* G0,G1‡ G8‡	C03 C04 C08	IV-9
900F	Attention Check - device attention failed to reset	A06 A05 A07* A08‡ G0,G1‡ G8‡	C07 C08 C09/10 C11 (C12)	IV-22
9101	Reorient Counter Check	G1,G8‡ G0‡	C07 C05 C08 C11 (C12) C04	V-49
9102	Track Counter Check	G1,G8‡ G0‡	C02,C07 C05,C08 C06,C03 C04,C11 (C12)	V-56
9104	Write Fail	A04 A05 A07* G1,G8‡ G0‡	C06 C05 C08 C11 (C12) C04	V-20
9018	Controller BI P Check	A07* G1,G8‡ G0‡	C04 C08 C11 (C12) C03 C07 C09/10 C02	III-13
9110	Device BI P Check	A07* G1,G8‡ G0‡	C03 C08	IV-15
9118	Device BI P Check and Controller BI P Check	A07* G1,G8‡ G0‡	C03 C08 C07 C09/10 C11 (C12)	IV-15
9120	Check 1 of 8 - The number of drives selected is less than or greater than one.	A07* G1,G8‡ G0‡	C09/10	IV-2
9140	BO Parity Check	GA,GC‡	C11 (C12) C07 C08 C09/10 C04	III-11

*When replacing, check address module.
**After replacing, adjust servo velocity gain.
‡Cable Groups. See Table 6.3A in STC 8650 MRM.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
9180	Tag Bus Parity Check	GA,GC‡	C11 (C12) C07 C08 C09/10 C04	III-11
91FF	Control Interface Bus in Assembly Failure	GA,GC‡	C05 C06 C04 C08 C11 (C12) C07	III-15
91XX	Some Failures Cause Multiple Fault Symptom Codes	GA,GC‡	Refer to RP20 Inline Section	
9200	False Controller Check		C04 C07 C08 C11 (C12) C02 C05 C06	III-17
9201	ECC 0 Compare - This indicates the normal completion of a read or write operation.	This is not an error		
9202	ECC Hardware Check		C03 C04 C05 C06 C02 C01	V-15
9204	Status Monitor Check		C05 C07 C08 C03 C06 C04 C02	V-46
9208	Write Data Parity Error		C02 C03 C04 C07 C08 C09/10 C11 (C12) C05	V-17

‡Cable Groups. See Table 6.3A in STC 8650 MRM.

RP20 Fault Symptom Codes (Cont)

Fault Symptom Code (Hex)	Error Description	Drive FRUs (Cards)	Control Modules	8650 MRM Map Entry or Par.
9210	GAP Counter Check		C05 C03 C04 C07 C08 C09/10 C11 (C12)	V-7
9220	Shift Register Error		C03 C04 C01 C05 C08 C11 (C12)	V-31
9240	Missing Servo Data		C01 C06 C02 C03 C05 C07	V-45
9280	VFO Phase Error		C06 C01 C03 C04 C11 (C12)	V-10
92XX	Some Failures Cause Multiple Fault Symptom Codes		Refer to RP20 Inline Section	
93XX	Invalid Fault Symptom Code		C07 C08 C11 (C12)	

INFORMATION COMMON TO ALL FORMATS

BYTE \ BIT	0	1	2	3	4	5	6	7
0	COMMAND REJECT	INTERVENTION REQUIRED	BUS OUT PARITY	EQUIPMENT CHECK	DATA CHECK	OVERRUN	NOT USED	NOT USED
1	PERMANENT ERROR	INVALID TRACK FORMAT	END OF CYCLE	NOT USED	NO RECORD FOUND	FILE PROTECT	WRITE INHIBIT	OPERATION INCOMPLETE
2	NOT USED	CORRECTABLE	NOT USED	ENVIRONMENTAL DATA BYTE 8-23	EMULATION	NOT USED	NOT USED	NOT USED
3	RESTART COMMAND BYTE 1 BIT 7 = 0 - LAST CHANNEL COMMAND IN THE CCW BYTE 1 BIT 7 = 1 - OPERATION IN PROGRESS WHEN OBR WAS GENERATED							
4	PHYSICAL DRIVE IDENTIFICATION DRIVE 8 OR 0	DRIVE 9 OR 1	DRIVE A OR 2	DRIVE B OR 3	DRIVE C OR 4	DRIVE D OR 5	DRIVE E OR 6	DRIVE F OR 7
5	LOGICAL CYLINDER ADDRESS LOW 128	64	32	16	8	4	2	1
6	FE CYLINDER	CYL ADD HIGH NAT/-11 512	CYL ADD HIGH NAT/-11 256	LOGICAL TRACK 16	8	4	2	1

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FORMAT 0 MESSAGE ONLY SENSE BYTE 7 FORMAT/MESSAGE SENSE BYTES 8-23 NOT USED

	0	1	2	3	4	5	6	7
MESSAGE	NO MESSAGE	INVALID COMMAND	INVALID SEQUENCE	CCW COUNT LOW	DATA ARGUMENT INVALID	DIAG/W INHIBITED BY FILE MASK	CHANNEL ABORTED RETRY	CHANNEL CCW 1 INCORRECT ON RETRY
	8	9	A	B	C	D	E	F
MESSAGE	MPL FILE NOT READY	MPL FILE PERMANENT SEEK CHECK	MPL FILE PERMANENT READ CHECK	COMMAND OVERRUN	DATA OVERRUN	DEFECTIVE TRACK	ALTERNATE TRACK	NOT USED

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FORMAT 1 DRIVE EQUIPMENT CHECK SENSE BYTE 7 FORMAT/MESSAGE

	0	1	2	3	4	5	6	7
MESSAGE	NOT USED	TRANSMIT TARGET ERROR	MICRO-PROGRAM DETECTED ERROR	TRANSMIT DIFFERENCE HIGH ERR	SYNC OUT TIMING ERROR	UNEXPECTED DRIVE STATUS AT INITIAL SELECTION	TRANSMIT CYL ADDR REGISTER ERR	TRANSMIT HEAD ERROR
	8	9	A	B	C	D	E	F
MESSAGE	TRANSMIT DIFFERENCE ERR	DRIVE STAT NOT AS EXPECTED DURING RD IPL	SEEK VER CHECK ON PHYSICAL ADDRESS	SEEK INCOMPLETE OR SECTOR COMPARE CHECK	NO INTR FROM DRIVE	DEFECT SKIPPING OR REORIENTATION CHECK	NOT USED	RETRY REORIENTATION CHECK

MR-6085

FORMAT 2 DCU ERROR SENSE BYTE 7 FORMAT/MESSAGE

	0	1	2	3	4	
MESSAGE	NO MESSAGE	NOT USED	NOT USED	S REG LOAD CHECK	CTL INTF REG VALID SENSE BYTES 13-15	MESSAGE 5-F NOT USED

MR-6086

FORMAT 3 SENSE BYTE 7 FORMAT/MESSAGE

MESSAGE	FORMAT 3 SENSE BYTE 7/MESSAGE NOT USED SELECTIVE RESET

MR-6087

FORMAT 4 DATA CHECKS UNCORRECTABLE SENSE BYTE 7 FORMAT/MESSAGE

	0	1	2	3	4	5	6	7
MESSAGE	HA ECC DATA CHECK	COUNT FIELD DATA CHECK	KEY FIELD DATA CHECK	DATA FIELD DATA CHECK	HA FIELD NO SYNC BYTE FOUND	COUNT FIELD NO SYNC BYTE FOUND	KEY FIELD NO SYNC BYTE FOUND	DATA FIELD NO SYNC BYTE FOUND
	8	9						
MESSAGE	NOT USED	AM DETECTION FAILURE ON RETRY	A-F NOT USED					

MR-6088

FORMAT 5 DATA CHECKS CORRECTABLE FORMAT/MESSAGE

	0	1	2	3	
MESSAGE	NOT USED	NOT USED	NOT USED	DATA FIELD CORRECTABLE DATA CHECK	MESSAGES 4 - F NOT USED

MR-6089

FORMAT 6 USAGE AND OVERRUN ERROR STATISTICS

MESSAGE	FORMAT 6 - MESSAGE 0-F ARE NOT USED

MR-6090

FORMAT 1 SENSE BYTES 8-13

BYTE \ BIT	0	1	2	3	4	5	6	7
8 — DRIVE STATUS BYTE 19 BIT 0 = 0	CONTROLLER CHECK (REF. BYTE 17&20) CC170	TAG BUS OR BUS OUT PAR DG050	ACCESS CHECK SECTOR NONCOMPARE DP050	RD/WR CHECK (REF BYTE 12&19) DE005	ONLINE DF030	ACCESS HDA ATTN DF030	BUSY DF040	SK CMPT SK SCTR PAD CMPT DF070
8 — BYTE 19 BIT 0 = 1		WRITE 1 DD010				PAD IN PROGRESS DE030	INDEX MARK DE015	3330 MODES DH005
9 CHECK STATUS	PAD STATUS DE030	SECTOR NON COMPARE DH060	MOTOR AT SPEED LTH DH010	AIR SWITCH ON LTH DH010	WRITE ENABLE DH010	FIXED HEADS DH005	3330-1 .... 10 8350 .... 01* 3330-11 .... 11* DH005	
10 HDA/SEQ CONTROL	FMT ERR/ FMT LTH ERROR	HDA SEQUENCE STATE LATCH 4	2	1	HDA SEQUENCE CHECK LTH	INHIBIT HDA RECYCLE	GEMINI* HDA	ODD TRACK STAT 7
11 LOAD SW STATUS	DRIVE START LTH DH010	GUARD BAND LTH DA005	TARGET VELOCITY DB030	TRACK CROSSING DA025	NOT USED	AIR SWITCH ON DH085	GEMINI* HDA DOUBLE DENSITY	MOTOR AT SPEED DH010
12	MULTICHIP CHECK DE010	CAPABLE ENABLE CHECK DE010	WRITE OVERRUN LTCH DE015	INDEX CHECK SEL DA005	DELTA I/W CHECK ** DE025	CONTROL CHECK DE010	TRANSITIONS CHECK DE035	WRITE 1 CHECK DE035
13 MESSAGE CODE 2 AND C	BUS OUT AT TIME OF ERROR WHEN SENSE BYTE 18 = 01,03,05, OR 06							
13 MESSAGE CODE A OR B	LOGICAL CYL ADDRESS LOW PRIOR TO SENSE BYTE 5							
	128	64	32	16	8	4	2	1

*8650 ONLY **8350 ONLY

MR-6091

FORMAT 1 SENSE BYTES 13-18

BYTE \ BIT	0	1	2	3	4	5	6	7
13 MESSAGE CODE 1,3,5,6, 7,8,&9	EXPECTED DRIVE STATUS/DATA							
14 MESSAGE OTHER THAN A&B	CONTROL INTERFACE BUS IN AT TIME OF FAILURE							
14 MESSAGE CODE A&B	IF BIT 0&1 = 11 FIXED HEAD LOGICAL CYL ADDR HIGH PRIOR TO BYTE 6 512	256	LOGICAL TRACK PRIOR TO SENSE BYTE 6 TRACK = HEAD 32	16	8	4	2	1
15	CONTROL INTERFACE TAG BUS AT THE TIME OF THE DETECTED ERROR							
16	TIME OUT CHECK DF040	OVER SHOOT CHECK DF030	SERVO OFF-TRACK DF010	REZERO MODE LATCH DF050	SERVO LATCH DF010	LINEAR MODE LATCH DF010	CONTROL LATCH DF010	WAIT LATCH DF040
17	VFO PHASE CK 01 = MISSING SERVO DATA 10 = VFO PHASE ERR 11 = MISSING READ DATA CC140		SHIFT REG ERR CC140	GAP CNTR CHECK CF120	WRT DATA PARITY ERROR CC140	STATUS MONITOR CHECK CJ160	ECC HARDWARE CHECK CD100	ECC O COMPARE CD100
18	NOT USED				CODED ERROR CONDITION (BITS 4-7 HEX) LISTED BELOW			

BYTE 18, BITS 4-7

0	1 !	2	3 !	4	5 !	6 !	7
NOT USED	NO TAG VALID ON R/W OPERATION	NO NORMAL OR CHECK END ON R/W OR ECC OPERATION	NO RESPONSE FROM CNT MOD ON CNT OPERATION	TIME OUT WAITING FOR INDEX	ECC HARDWARE CHECK	MULTIPLE OR NO CNT MOD SELECTED	PRESELECTION CHECKS
8	9	A	B	C !	D	E	F
REPETITIVE CMND OVERRUNS ON G1 OPERATIONS	REPETITIVE CMND OVERRUNS ON G2 OR G3 OPERATIONS	POLL OR 1 OF 8 DECODE ERROR	BUSY MISSING AFTER SEEK START IS ISSUED	DEVICE TYPE ERROR	CHANNEL SELECT ERROR	PRESELECTION DISK CONTROL INTERFACE BUS	UNRESETABLE INTERRUPT

NOTE
! SENSE BYTES 13,14,15 ARE VALID FOR THESE MESSAGES

MR-6092

FORMAT 1 SENSE BYTES 19-23

BYTE \ BIT	0	1	2	3	4	5	6	7
19	SET R/W OPERATION 85 CH100	NOT USED	NOT USED	NOT USED	HEAD SHORT LATCH DE015	PAD GATE ERROR 5 DE110	1,2 MB FILE * / SELECTED **	ALWAYS ON
20	TAG BUS PARITY CHECK CH120	BUS OUT PARITY CHECK LATCHED CH120	CHECK 1 OF 8 CJ150	DEVICE BUS IN PARITY CHECK LATCHED CJ150	CONTROLLER BUS IN PARITY CHK LATCHED CD180	CURRENT (I) WRITE CHECK CC170	TRACK COUNTER CHECK GTD CC170	REORIENT COUNTER CH150
20 MESSAGE A AND BYTE 0 BIT 3 = 1	LOGICAL CYLINDER ADDRESS LOW							
	128	64	32	16	8	4	2	1
21 MESSAGE A AND BYTE 0 BIT 3 = 1	BITS 0 & 1 = 11 FIXED HEAD / LOGICAL CYLINDER ADDRESS HIGH		LOGICAL TRACK (HEAD)					
	512	256	32	16	8	4	2	1
21	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	BUS OUT PARITY (BO PAR)	TAG BUS PARITY
22-23	FAULT SYMPTOM CODE							

*8650 ONLY **8350 ONLY

MR-6093

FORMAT 2 DCU CHECK SENSE BYTES 8-23

BYTE \ BIT	0	1	2	3	4	5	6	7
8-10	NOT USED							
11 CONTROL CHECK	CHANNEL BUFFER PARITY CHECK	INTERFACE CHECK CHANNEL A OR C	INTERFACE CHECK CHANNEL B OR D	DATA TRANSFER CHECK	CONTROL INTERFACE LOGIC CHECK	LOAD 5 REGISTERS CHECK	COMPARE ASSIST CHECK	CHANNEL C/D OR MULTI-CONNECT
12	SET TO 0							
13	CONTROL INTERFACE (CONTENTS OF TA REGISTERS, VALID ONLY IF SENSE BYTE 7 IS 24)							
14	CONTROL INTERFACE BUS-IN (CONTENTS OF MA REGISTER, VALID ONLY IF SENSE BYTE 7 IS 24)							
15	CONTROL INTERFACE BUS-IN (CONTENTS OF MD REGISTER, VALID ONLY IF SENSE BYTE 7 IS 24)							
16-19	NOT USED, SET TO 0							
20	CONTROL MODULE CHECK	CONTROL MODULE ACTIVE CHECK	CONTROL MODULE BUFFER PARITY CHECK	CONTROL MODULE UNEXPECTED END CHECK	CONTROL MODULE TAG BUS CHECK	CONTROL MODULE BUS-OUT CHECK	CONTROL MODULE TRANSFER CHECK	NOT USED
21	NOT USED, SET TO 0							
22-23	FAULT SYMPTOM CODE							

MR-6094

FORMAT 3 SENSE BYTES 8-23

BYTE \ BIT	0	1	2	3	4	5	6	7
8	FAILING ADDRESS (BACK-UP ADDRESS REGISTER BUS 0-7)							
9	FAILING ADDRESS (BACK-UP ADDRESS REGISTER BUS 8-13)							
10	BIT 0 = 1 EARLY ERROR	CLOCK ERROR	0	0	0	0	0	SPECIAL OP ERROR
	BIT 0 = 0 LATE ERROR				A REG CHECK	B REG CHECK	ALU CHECK	MPL READ CHECK
11 SENSE BYTE 10 BIT 0 = 1	0	STORE MULTIPLE READ ERROR	STORE ECC LOGIC ERROR	0	0	CD DECODE ERROR	0	0
11 SENSE BYTE 10 BIT 0 = 0	STORE ADDRESS BUS 0-7 CHECK	STORE ADDRESS BUS 8-13 CHECK	STORE WRITE BUS 2/3 CHECK	STORE WRITE BUS 0/1 CHECK	0	0	MPL NOT READY	0
12	SYNDROME REGISTER							
13	TC REGISTER (THIS REGISTER IS RESET IF SELECTIVE RESET OCCURRED IN RESPONSE TO DISCONNECT IN)							
14	TG REGISTER (THIS REGISTER IS RESET IF SELECTIVE RESET OCCURRED IN RESPONSE TO DISCONNECT IN)							
15-23	NOT USED. SET TO 0							

MR-6095

FORMAT 4 DATA CHECKS NOT PROVIDING DISPLACEMENT INFORMATION SENSE BYTES 8-23

BYTE \ BIT	0	1	2	3	4	5	6	7
8	CYLINDER ADDRESS OF THE RECORD IN ERROR							
	0	0	0	0	0	0	512	256
9	CYLINDER ADDRESS OF THE RECORD IN ERROR							
	128	64	32	16	8	4	2	1
10	HEAD ADDRESS OF THE RECORD IN ERROR							
	0	0	0	0	0	0	0	0
11	HEAD ADDRESS OF THE RECORD IN ERROR							
	0	0	0	16	8	4	2	1
12	RECORD NUMBER (UNRELIABLE MESSAGE 0 OR 4, ERROR HA) (UNRELIABLE MESSAGE 1 OR 5, ERROR COUNT FIELD)							
13	SECTOR NUMBER OF THE RECORD IN ERROR							
		64	32	16	8	4	2	1
14-21	NOTE BYTE 15 = RETRY COUNT			NOT USED				
22-23	FAULT SYMPTOM CODE							

MR-6096

FORMAT 5 DATA CHECKS PROVIDING DISPLACEMENT INFORMATION SENSE BYTES 8-23

BYTE \ BIT	0	1	2	3	4	5	6	7
8	CYLINDER ADDRESS OF THE RECORD IN ERROR							
							512	256
9	CYLINDER ADDRESS OF THE RECORD IN ERROR							
	128	64	32	16	8	4	2	1
10	HEAD ADDRESS OF THE RECORD IN ERROR							
11	HEAD ADDRESS OF THE RECORD IN ERROR							
	0	0	0	0	0	0	0	0
12	RECORD NUMBER SET TO 0 IF ERROR OCCURRED IN HA							
				16	8	4	2	1

13	SECTOR NUMBER OF THE RECORD IN ERROR
14	NOT USED
15,16,17	IDENTIFIES THE NUMBER OF BYTES PROCESSED BY THE DCU FROM THE INITIATION OF DATA TRANSFER AND THE END OF THE DATA FIELD
18-19	ERROR DISPLACEMENT. SPECIFIES THE FIRST BYTE IN ERROR WITHIN THE DATA FIELD WITH RELATIONSHIP TO THE END OF THAT DATA FIELD
20-21	ERROR CORRECTION PATTERN (EACH BIT IN ERROR WILL BE INDICATED BY A 1)
22	ALWAYS 0
23	NOT USED

MR-6097

FORMAT 6 USAGE AND OVERRUN ERROR STATISTICS SENSE BYTES 8-23

BYTE \ BIT	0	1	2	3	4	5	6	7
8-11	NUMBER OF BYTES READ OR SEARCHED (KEY AND DATA FIELD ONLY)							
12-13	NOT USED SET TO ZERO							
14-15	NUMBER OF DATA CHECKS SUCCESSFULLY RETRIED							
16-17	NUMBER OF ACCESS MOTIONS							
18	CHANNEL SELECT FOR SENSE BYTES 20-23. BIT 0=0 INFORMATION APPLIES TO INTERFACES A AND B. IF BIT 0=1 INFORMATION APPLIES TO INTERFACES C & D. BITS 1-7 NOT USED							
19	TOTAL SEEK ERRORS RETRIED							
20	COMMAND OVERRUNS A (C)							
21	DATA OVERRUNS A (C)							
22	COMMAND OVERRUNS B (D)							
23	DATA OVERRUNS B (D)							

MR-6098

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LP20 SWITCHES AND JUMPERS

Switches
M8586 (Rev. E) uses a switch pack in place of jumpers.

775400 (address unit 0) set switches 5, 6, 8, 9, and 10 OFF.

754 (vector unit 0) set switch 3 OFF

775420 (address unit 1) set switches 1, 5, 6, 8, 9, and 10 OFF.

750 (vector, unit 1) set switches 1 and 3 OFF.

Jumpers
I indicates that the jumper should be installed.

R indicates that the jumper should be removed.

M8586 Control Loc: ABCDEF02

W1-W9 corresponds to base address 775400 (for unit 0) or 775420 (for unit 1).

Jumper	Adr List	775400	775420
W1	4	I	R
W2	5	I	I
W3	6	I	I
W4	7	I	I
W5	8	R	R
W6	9	R	R
W7	10	I	I
W8	11	R	R
W9	12	R	R

W10-W16 corresponds to vector 754 (for unit 0) or 750 (for unit 1)

Jumper	Vec bit	754	750
W10	2	I	R
W11	3	I	I
W12	4	R	R
W13	5	I	I
W14	6	I	I
W15	7	I	I
W16	8	I	I

M8587 Data Paths

Jumper	Function
W1	Install to enable parity
W2	Install for DAVFU

KL10 MODEL(PA and PV) OPTION JUMPERS

OPTION BITS--SOURCE------4D44E1=CRM 08 H

CACHE AVAILABLE--------4E43A1
CHANNELS AVAILABLE-----4E43E1
50 HRZ-----------------4E43M2
MCA25 AVAILABLE________4E43F2
KL10-PV/PW-CPU_________4D43D2

SERIAL NUMBER BITS--SOURCE--4D42E1

2048--4E41M2
1024--4E41A1
512---4E41E1
256---4D41D2
128---4D41E1
64----4E41F2
SERIAL NUMBER BITS--SOURCE--4D40E1

32----4E39M2
16----4E39A1
08----4E39E1
04----4D39D2
02----4D39E1
01----4E39F2

MA20 JUMPERS

CONT #	JUMPER PINS(S) TO GROUND
0	EE1 AND EF2
1	EF2
2	EE1
3	NONE

NOTE: Jumpers are external on the backplane.

MG10/MH10 JUMPERS

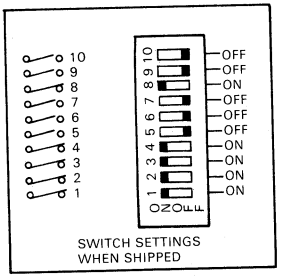
DEV	REQCYC (M ROW)		ADRACK (N ROW)	
	From	To	From	To
DAS33	T7	A5*	T7	C7
DF10	T7	A4	T7	A1
DF10C	T7	A5*	T7	C7
DL10	T7	A5*	T7	C7
DT05	T7	A4	T7	A1
DX10	T7	A5**	T7	C7
KA10	T7	A4	T7	A1
KI10	T7	A5*	T7	C7
KL10	T7	A5*	T7	A1
MX10	T7	A4	T7	A1
MX10C	T7	A5*	T7	C7

* Use pin A5 if MG10 is the fastest memory on that bus; otherwise, use pin B5.
**Never use pin B5 (RQ Cyc Slow).

SW./JUMPS.

DC20F

H3007 DISTRIBUTION PANEL



SWITCH SETTINGS
WHEN SHIPPED

MODEM TYPE	DESCRIPTON
183A	300 BAUD FULL DUP
183E, G, H	300 BAUD FULL DUP
183F	300 BAUD FULL DUP
113A	300 BAUD ORIGINATE ONLY
282C,D	1000 BAUD ½ DUP
011B	LOW SPEED TWX
EIA	RS232-C (SEE BELOW)

DON'T CARE
CASES

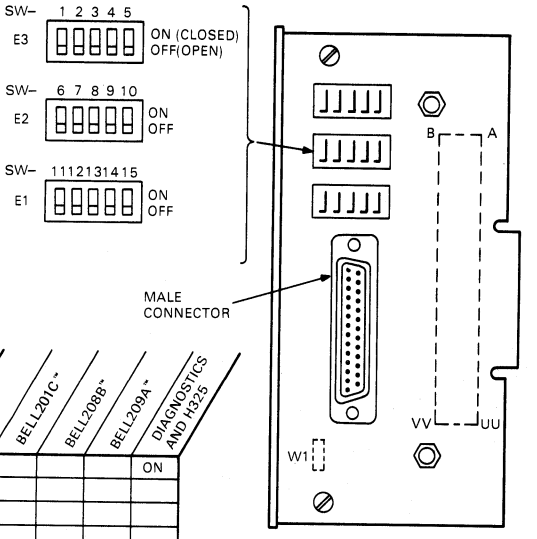
SWITCH LOCATION	PIN NO	SIGNAL	MODEM
8	4	REQ TO SEND	—
2	11	SEC TRANS DATA	BEL 202
3	12	SEC REC'D DATA	
2	14	SEC TRANS DATA	EIA
3	16	SEC REC'D DATA	
4	17	RESTRAINT	011B
8	25	BUSY	103E,G,H

SWITCH SETTINGS H3007 DISTRIBUTION PANEL

1. IN SPECIAL CASES, ANY GIVEN SIGNAL FROM THE MODEM SHOULD BE PUT ON WHATEVER PIN REPRESENTS THAT SIGNAL ON THE H3007 DIST. PANEL WITH SWITCHES 1-7. CHECK MODEM SCHEMATIC AND COMPARE IT WITH THIS FIGURE.
2. BUS INITIALIZATION OF THE MODEM CONTROL MODULES, H7807, AND H7147 (OR M7808) CAN BE INHIBITED BY REMOVING DH11 BACKPANEL WIRE F02B2 TO GROUND.
3. INTERRUPTS FOR ALL LINES MAY BE INHIBITED FOR CARRIER RING, SEC RX, OR CLEAR TO SEND BY REMOVING THE WIRES LISTED BELOW.

STATUS	DH11 WIRE REMOVED
CARRIER	E02A1 TO D02B1
RING	E02C1 TO D02F2
SEC RX	E02B1 TO D02A1
CLEAR TO SEND	E02D1 TO D02C1

H3001 DISTRIBUTION PANEL



	DF03	BELL201C*	BELL208B*	BELL209A*	DIAGNOSTICS AND H325
S1					ON
S2					
S3					
S4					
S5					ON
S6					
S7					
S8					
S9					
S10		*			
S11					
S12					
S13					
S14					
S15					

NOTE:
SWITCHES ARE OFF UNLESS OTHERWISE INDICATED.
*ON IF NEW SYNC CONFIGURED ON M7867
201™, 208™, 209™ ARE TRADEMARKS OF WESTERN ELECTRIC.

MR-14266

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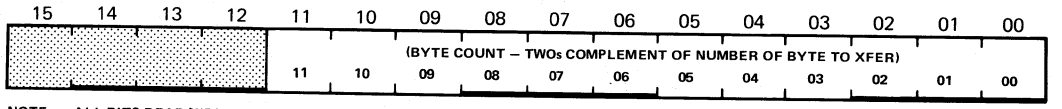
NOTES

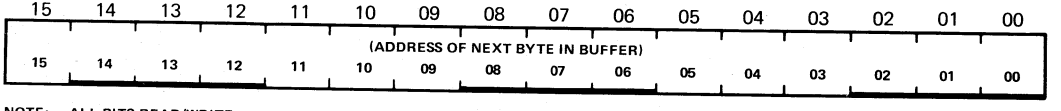
LPBCTR – DMA Byte Count Register



NOTE: ALL BITS READ/WRITE.

MR-2015

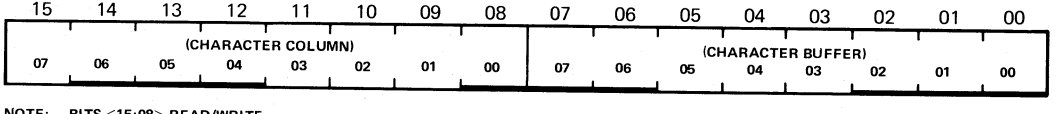
LPBSAD – DMA Bus Address Register



NOTE: ALL BITS READ/WRITE

MR-2014

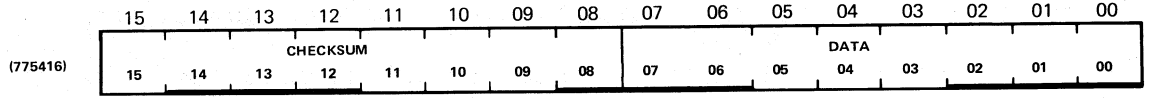
LPCCTR – Column Count Register (High Byte)
LPCBUF – Character Buffer Register (Low Byte)



NOTE: BITS <15:08> READ/WRITE

MR-2018

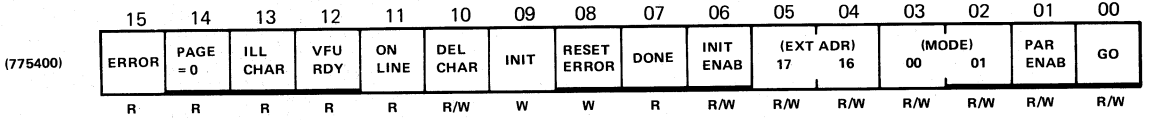
LPCKSM – Checksum Register
LPTDAT – Printer Data Register



NOTE: ALL BITS READ ONLY

MR-2013

LPCSRA – Control and Status Register "A"



15	LOGICAL "OR" OF ALL ERRORS
14	PAGE COUNTER INCREMENTED TO ZERO
13	ILLEGAL CHARACTER
12	DAVFU READY (SET IF OPTICAL VFU)
11	PRINTER READY AND ON LINE
10	DELIMITER CHAR HELD
09	INITIALIZE - RESET FLAGS SET DONE
08	RESET ERROR, SET DONE, RESET GO
06	INTERRUPT ENABLE
<05:04>	EXTENDED UNIBUS ADDRESS BITS 17 AND 16
<03:02>	MODE BITS 00 = NORMAL 01 = TEST MODE (INHIBIT PRINTING) 10 = VFU LOAD (DMA TO VFU) 11 = RAM LOAD (DMA MODE ONLY)
01	PARITY ENABLE (RAM AND MEMORY)

MR-2012

LPCSRB — Control and Status Register "B"

(775402)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
VALID DATA	LA180	NOT RDY	PAR BIT	OP VFU	02	(TEST) 01	00	OFF LINE	VFU ERROR	PAR ERROR	MEM ERROR	RAM ERROR	SYNC T O	DEM T O	GO ERROR
R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

14 SET IF LA180 TYPE PRINTER
13 NOT READY (OTHER THAN TAPE FAULT)
12 DATA PARITY BIT (AS SENT TO PRINTER)
11 OPTICAL VFU (ZERO IF DAVFU)
05 PARITY ERROR AT PRINTER
04 MEMORY PARITY ERROR
03 RAM PARITY ERROR DURING DMA XFER
02 MASTER SYNC TIME OUT (NO SSYNC)
01 DEMAND TIME OUT
00 GO SET AND "ERROR" OR "DEMAND

<10:08> FORCE ERROR CONDITIONS

02	01	00	
0	0	0	NORMAL
0	0	1	DEMAND TIME OUT
0	1	0	M SYNC TIME OUT
0	1	1	RAM PARITY ERROR
1	0	0	MEM PARITY ERROR
1	0	1	LPT DATA PAR ERROR
1	1	0	DECREMENT PAGE COUNT
1	1	1	NOT USED

MR-2016

LPPCTR — Page Count Register

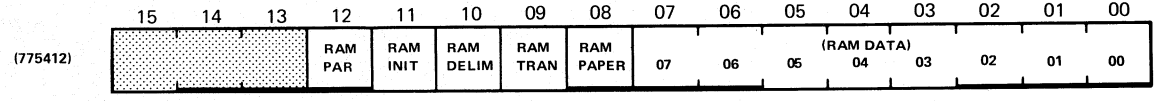
(775410)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
				(PAGE COUNT)											
				11	10	09	08	07	06	05	04	03	02	01	00

NOTE: ALL USED BITS READ/WRITE

MR-2017

LPRAMD – RAM Data Register



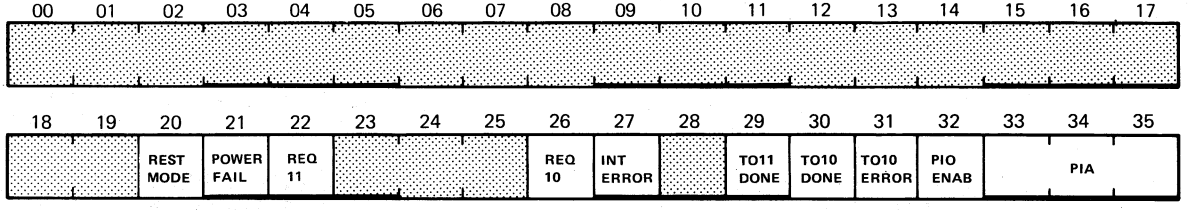
NOTE: ALL USED BITS EXCEPT 12 READ/WRITE

12	RAM PARITY BIT
11	INTERRUPT BIT – GEN A BR
10	DELIMITER – TAKE DATA FROM RAM
09	TRANSLATION BIT – RDAT TO PRINTER
08	PAPER INSTRUCTION RDAT TO DAVFU
<07:00>	RAM DATA – ADDRESS IS IN LPCBUF

MR-2019

CONI DTE

(7xx240)

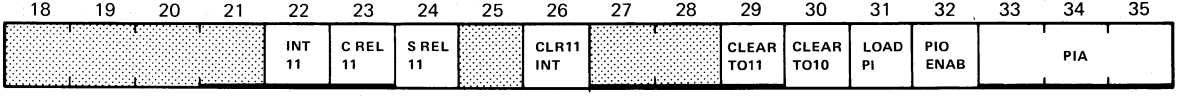


20 RESTRICTED MODE
22 10 REQUESTING 11
26 11 REQUESTING 10
27 INTERRUPT TO11 ERROR
32 PIO ENABLE

MR-2100

CONO DTE

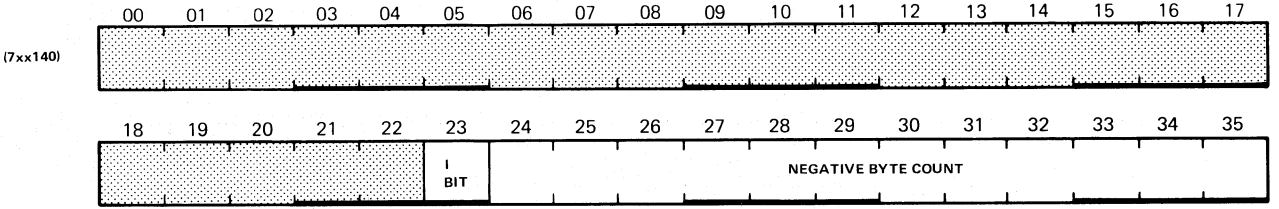
(7xx200)



22 10 REQUESTING 11 INTERRUPT
23 CLEAR RELOAD 11
24 SET RELOAD 11
26 CLEAR 11 REQUESTING 10 INTERRUPT
29 CLEAR TO 11 DONE AND TO 11 ERROR
30 CLEAR TO 10 DONE AND TO 11 ERROR
31 LOAD PI CHAN NUMBER INTO BITS <33:35>
32 PIO ENABLE

MR-2099

DATAO DTE



23 0 = INTERRUPT KL10 (ONLY) AT END OF TRANSFER
1 = INTERRUPT BOTH 10 AND 11 AT END OF TRANSFER

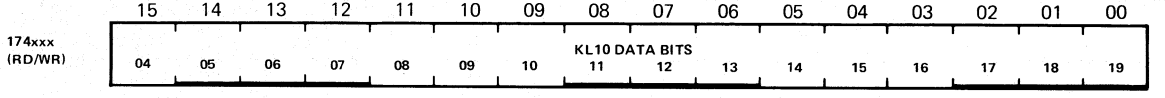
MR-2106

DEXWD1 — Deposit or Examine Word 1

NOTE: xxx = (406 — DTE NO. 0) (446 — DTE NO. 1) (506 — DTE NO. 2) (546 — DTE NO. 3)

MR-2107

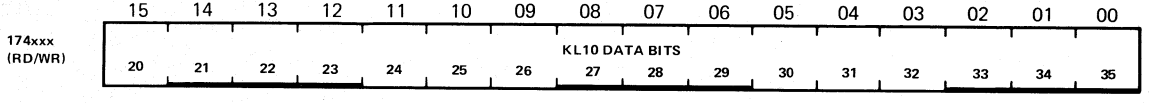
DEXWD2 — Deposit or Examine Word 2



NOTE: xxx = (404 — DTE NO. 0) (444 — DTE NO. 1) (504 — DTE NO. 2) (544 — DTE NO. 3)

MR-2108

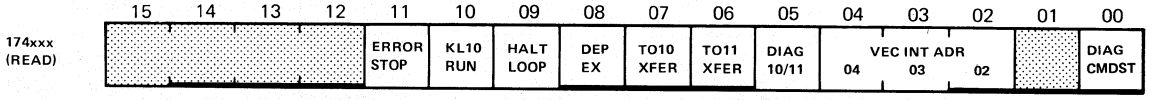
DEXWD3 — Deposit or Examine Word 3



NOTE: xxx = (402 — DTE NO. 0) (442 — DTE NO. 1) (502 — DTE NO. 2) (542 — DTE NO. 3)

MR-2109

DIAG1 – Diagnostic Word 1

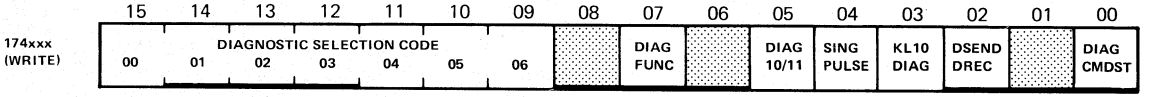


NOTE: xxx = (430 – DTE NO. 0) (470 – DTE NO. 1) (530 – DTE NO. 2) (570 – DTE NO. 3)

11	CRAM, DRAM, FM PARERR OR FS PROBE COND
10	RUN FLOP SET, CONTROLLED BY 11
09	MICROCODE IN HALT LOOP
08	DEPOSIT OR EXAMINE
07	TO10 TRANSFER
06	TO11 TRANSFER
05	DIAGNOSE 10/11 INTERFACE
<04:02>	VECTOR INTERRUPT ADDRESS
00	DIAGNOSTIC COMMAND START

MR-2118

DIAG1 – Diagnostic Word 1



NOTE: xxx = (430 – DTE NO. 0) (470 – DTE NO. 1) (530 – DTE NO. 2) (570 – DTE NO. 3)

07	REMOVE STATUS FROM DS LINES
05	DIAGNOSE 10/11 INTERFACE
04	SINGLE CLOCK CYCLE
03	KL10 DIAGNOSTIC TRANSFER MODE
02	SEND/RECEIVE DURING DIAGNOSTIC BUS TRANSFER
00	DIAG COMMAND START (DCOMST)

MR-2102

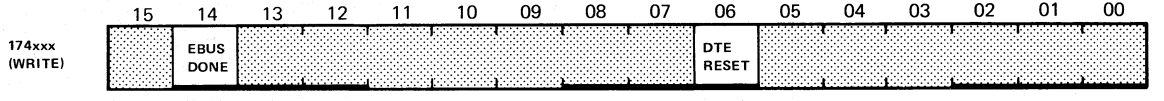
DIAG2 – Diagnostic Word 2

NOTE: xxx = (432 – DTE NO. 0) (472 – DTE NO. 1) (532 – DTE NO. 2) (572 DTE NO. 3)

<15:12> RAM FILE MIXER ADDRESS

MR-2119

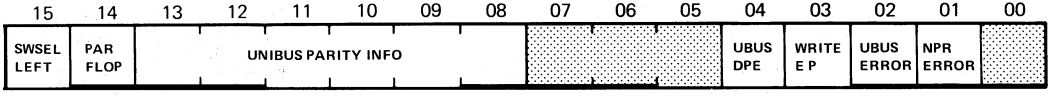
DIAG2 – Diagnostic Word 2



NOTE: xxx = (432 – DTE NO. 0) (472 – DTE NO. 1) (532 – DTE NO. 2) (572 – DTE NO. 3)

MR-2103

DIAG3 – Diagnostic Word 3

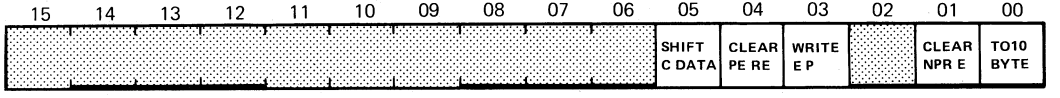


NOTE: xxx = (436 – DTE NO. 0) (476 – DTE NO. 1) (536 – DTE NO. 2) (576 – DTE NO. 3)

15	SWAP SELECT LEFT	03	EVEN PARITY WRITE SET
14	DPS4 (N) PARITY FLOP	02	UNIBUS RECEIVER ERROR
<13:09>	UNIBUS PARITY ERROR CAPTURED DATA	01	UNIBUS (NPR – BYTE) PARITY ERROR
04	DATO UNIBUS PARITY ERROR		

MR-2120

DIAG3 – Diagnostic Word 3

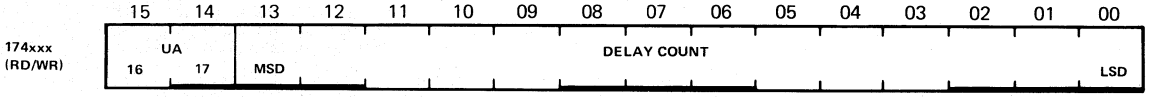


NOTE: xxx = (436 – DTE NO. 0) (476 – DTE NO. 1) (536 – DTE NO. 2) (576 – DTE NO. 3)

05	SHIFT CAPTURED DATA	01	CLEAR NPR PARITY ERROR
04	CLEAR UNIBUS PARITY AND RECEIVE ERROR	00	TO10 BYTE MODE
03	WRITE EVEN PARITY		

MR-2104

DLYCNT DELAY COUNT

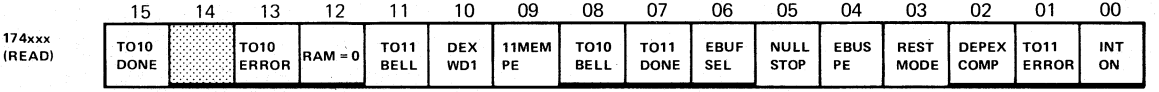


NOTE: xxx = (400 – DTE NO. 0) (440 – DTE NO. 1) (500 – DTE NO. 2) (540 – DTE NO. 3)
DELAY COUNT 37777 = NO DELAY

<15:14> UNIBUS ADDRESS BITS 16 AND 17

MR-2101

STATUS



NOTE: xxx = (434 – DTE NO. 0) (474 – DTE NO. 1) (534 – DTE NO. 2) (574 – DTE NO. 3)

15	TO10 BYTE COUNT = 0 OR PDP-11 SET TO10 DONE
13	NPR UNIBUS OR – 11 MEM PE OR UNIBUS TIMEOUT DURING TO10 BYTE XFER
12	RAM DATA = 0
11	11 DOORBELL INT REQ BY 10
10	DIAGNOSTIC USE ONLY
09	PDP-11 MEM PARITY ERROR
08	10 DOORBELL INT REQ BY 11
07	TO11 BYTE COUNT = 0, XFER STOP ON MU11 CHAR OR PDP-11 SET TO11 DONE
06	E BUFFER SELECT
04	EBUS PARITY ERROR DURING TO11 BYTE OR EXAM XFER
03	1 = RESTRICTED MODE, 0 = PRIVILEGED MODE
02	LAST DEP/EXAM COMPLETED
01	TO11 BYTE XFER ERROR
00	INTERRUPT ON

MR-2105

STATUS

174xxx (WRITE)

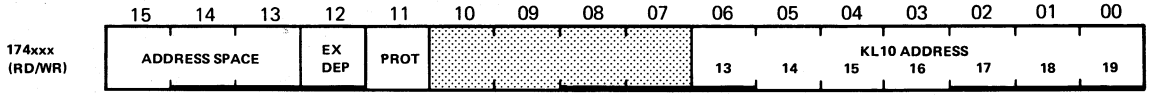
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
TO10 TERM	CLEAR TERM	TO10 ERROR	CLEAR TO10E	SET11 BELL	CLR11 BELL	CLR11 PE	SET10 BELL	SET11 DONE	CLR11 DONE	11INT REQ	CEBUS PE	INT OFF	SET EB PE	SET TO11E	CLEAR TO11E

NOTE: xxx = (434 – DTE NO. 0) (474 – DTE NO. 1) (534 – DTE NO. 2) (574 – DTE NO. 3)

15	TO10 NORMAL TERMINATION	07	SET TO11 DONE
14	CLEAR TO10 NORMAL TERMINATION	06	CLEAR TO11 DONE
13	SET TO10 ERROR	05	GEN PDP-11 BR REQ
12	CLEAR TO10 ERROR	04	CLEAR EBUS PARITY ERROR
11	SET TO11 DOORBELL	03	DISABLE DTE FROM GENERATING BR REQ
10	CLEAR TO11 DOOR BELL	02	SET EBUS PARITY ERROR
09	CLEAR PDP-11 MEMORY PARITY ERROR	01	SET TO11 ERROR
08	SET T10DB	00	CLEAR TO11 ERROR

MR-2121

TENAD1 – Ten Address 1



NOTE: xxx = (410 – DTE NO. 0) (450 – DTE NO. 1) (510 – DTE NO. 2) (550 – DTE NO. 3)

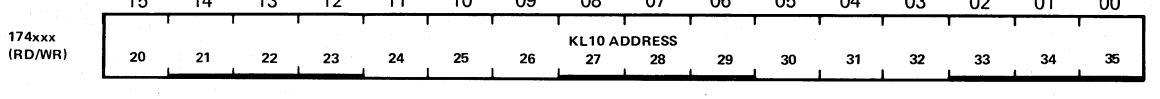
<15:13> 0 = EPT, 1 = EXEC VIRTUAL,
2–3 = RES, 4 = PHYS, 5–7 = RES

12 0 = EXAMINE 1 = DEPOSIT

11 1 = PROTECTION AND RELOCATION IS OFF FOR PRIVILEGED FRONT END.
0 = PROTECTION AND RELOCATION IS ON FOR PRIVILEGED FRONT END.

MR-2110

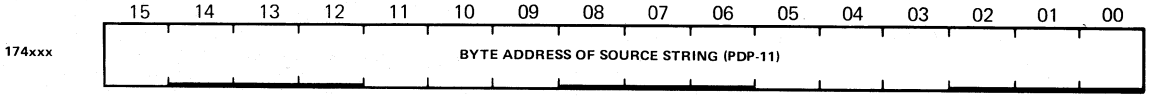
TENAD2 – Ten Address 2



NOTE: xxx = (412 – DTE NO. 0) (452 – DTE NO. 1) (512 – DTE NO. 2) (552 – DTE NO. 3)

MR-2111

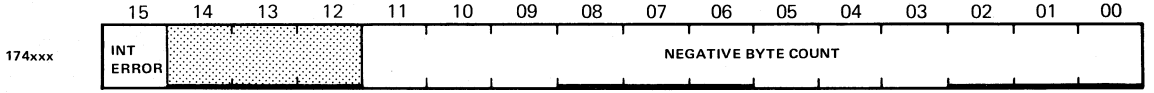
TO10AD – TO10 Address



NOTE: xxx = (420 – DTE NO. 0) (460 – DTE NO. 1) (520 – DTE NO. 2) (560 – DTE NO. 3)

MR-2115

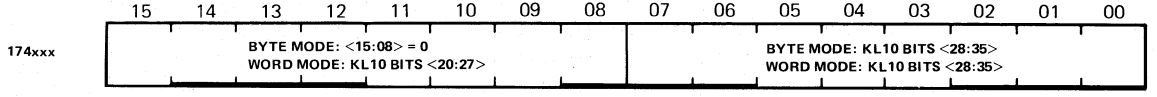
TO10BC – TO10 Byte Count



NOTE: xxx = (414 – DTE NO. 0) (454 – DTE NO. 1) (514 – DTE NO. 2) (554 – DTE NO. 3)

MR-2117

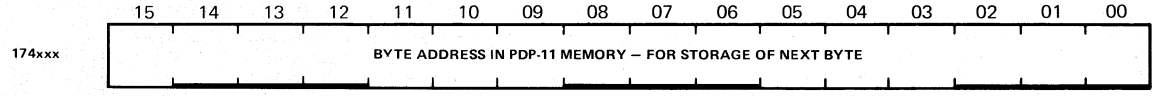
TO10DT – TO10 Data



NOTE: xxx = (424 – DTE NO. 0) (464 – DTE NO. 1) (524 – DTE NO. 2) (564 – DTE NO. 3)

MR-2113

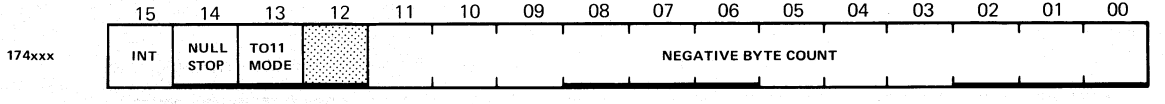
TO11AD – TO11 Address



NOTE: xxx = (422 – DTE NO. 0) (462 – DTE NO. 1) (522 – DTE NO. 2) (562 – DTE NO. 3)

MR-2114

TO11BC – TO11 Byte Count



NOTE: xxx = (416 – DTE NO. 0) (456 – DTE NO. 2) (516 – DTE NO. 2) (556 – DTE NO. 3)

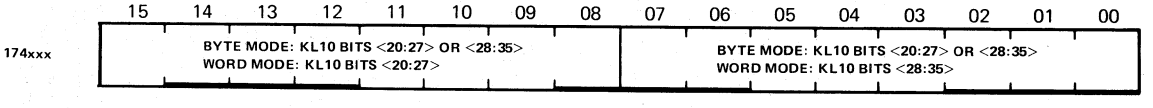
15 INT BIT: 0 = INT 11 NORM TERM,
: 1 = INT 10 AND 11

14 STOP ON NULL CHAR FROM EBOX

13 0 = WORD MODE IN DTE
1 = BYTE MODE IN DTE

MR-2116

TO11DT – TO11 Data

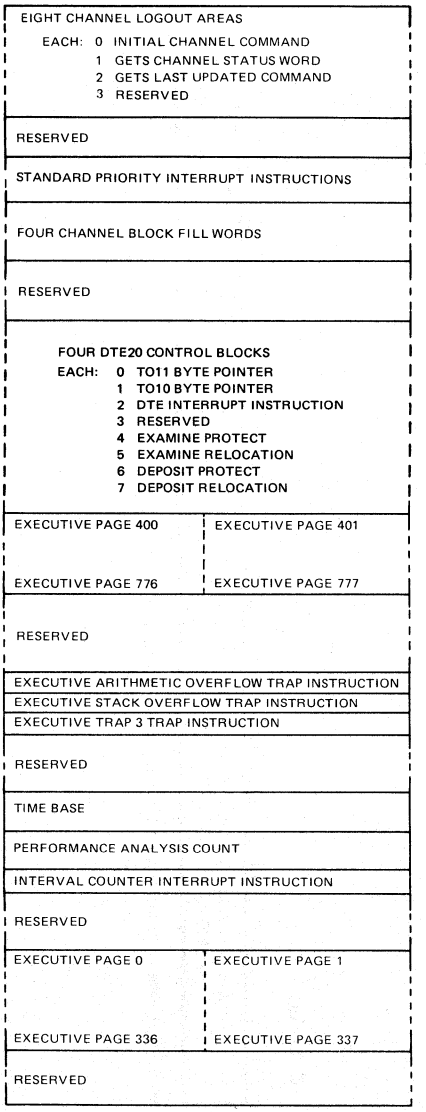


NOTE: xxx = (426 – DTE NO. 0) (466 – DTE NO. 1) (526 – DTE NO. 2) (566 – DTE NO. 3)

MR-2112

EXECUTIVE PROCESS TABLE

(ADDRESSED FROM EBR)



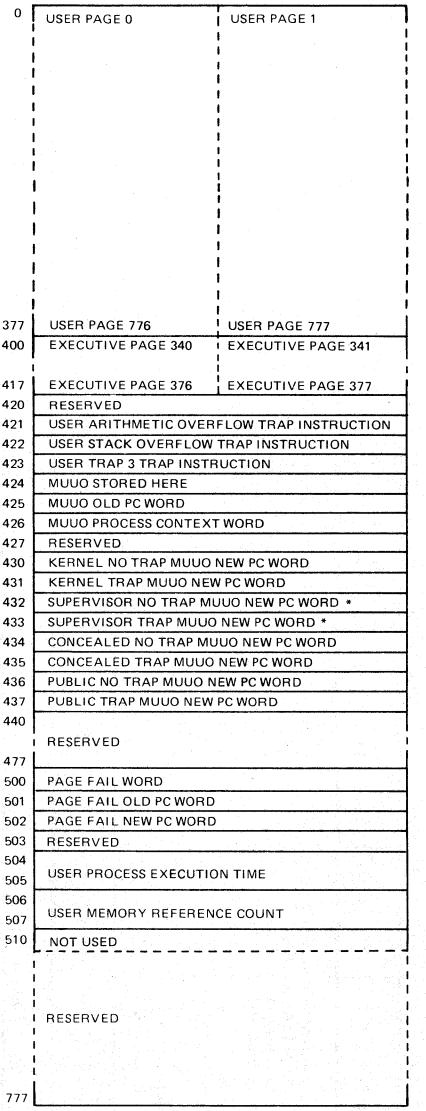
NOTE: APPLICABLE ONLY FOR MONITORS UP TO 7.01A

TOPS - 10 PROCESS TABLE
CONFIGURATION

MR-3699

USER PROCESS TABLE

(ADDRESSED FROM UBR)



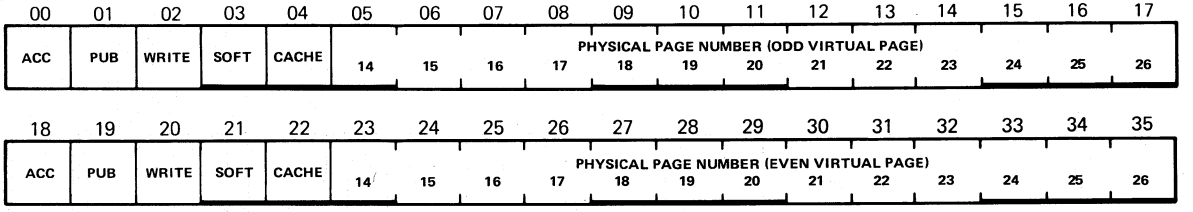
*NOT USED.

NOTE: APPLICABLE ONLY FOR MONITORS UP TO 7.01A

TOPS - 10 PROCESS TABLE
CONFIGURATION

MR-3698

Page Map Entry (TOPS-10 Only)



00 & 18 0 = NO ACCESS ALLOWED
1 = ACCESS ALLOWED

01 & 19 0 = PRIVATE
1 = PUBLIC

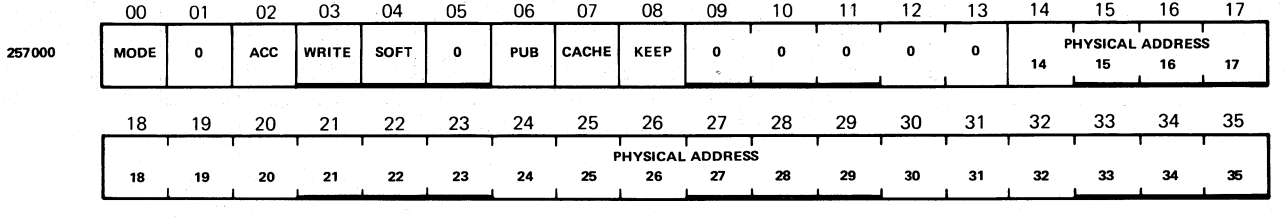
02 & 20 0 = WRITE-PROTECTED
1 = WRITABLE

03 & 21 SOFTWARE (NOT INTERPERTED BY HARDWARE)

04 & 22 0 = CACHE-LOOK BUT DO NOT LOAD
1 = CACHEABLE

MR-2194

Map (TOPS-10 Only)



NOTE: THIS REPRESENTS THE CONTENTS OF AC IF NO ERRORS OCCURRED.

00 0 = EXEC MODE
1 = USER MODE

02 0 = NO ACCESS ALLOWED

04 SOFTWARE (NOT INTERPERTED BY HARDWARE)

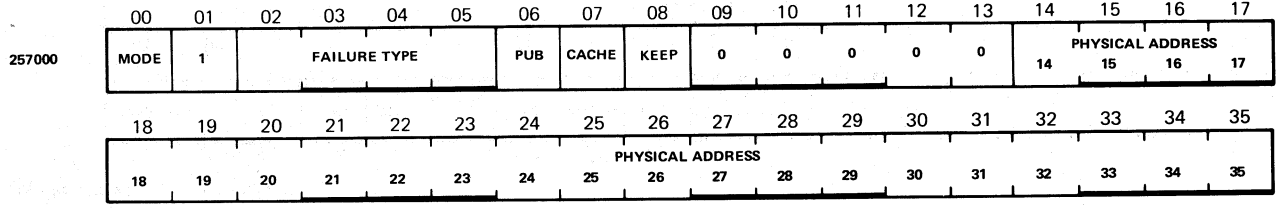
06 0 = PRIVATE
1 = PUBLIC

NOTE: THIS REPRESENTS THE CONTENTS OF AC IF NO ERRORS OCCURRED.

00 0 = EXEC MODE
1 = USER MODE
02 0 = NO ACCESS ALLOWED
1 = ACCESS ALLOWED
03 0 = WRITE-PROTECTED
1 = WRITABLE
04 SOFTWARE (NOT INTERPERTED BY HARDWARE)
06 0 = PRIVATE
1 = PUBLIC
07 0 = CACHE LOOK BUT DO NOT LOAD
1 = CACHEABLE

MR-3824

Map (TOPS-10 Only)

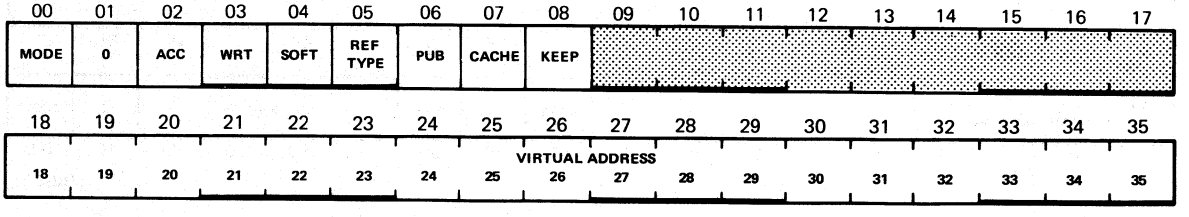


NOTE: THIS REPRESENTS THE CONTENTS OF AC IF A MAP ERROR IS DETECTED.
REFER TO OTHER MAP WORD FOR BIT DEFINITIONS.

<01:05> FAILURE TYPE
21 = PROPRIETARY ERROR
25 = PAGE TABLE PARITY ERROR

MR-3825

Page Fail Word (TOPS-10 Only)



00 0 = EXEC MODE
1 = USER MODE

02 0 = NO ACCESS ALLOWED
1 = ACCESS ALLOWED

03 0 = WRITE PROTECTED
1 = WRITABLE

04 SOFTWARE (NOT INTERPERTED BY HARDWARE)

05 0 = READ-ONLY REFERENCE
1 = REFERENCE INVOLVED A WRITE

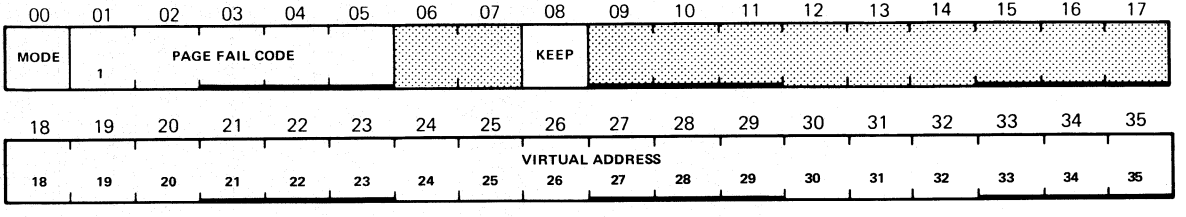
06 0 = PRIVATE
1 = PUBLIC

07 0 = CACHE LOOK BUT DO NOT LOAD
1 = CACHEABLE

08 A 1 INDICATES A VIRTUAL ADDRESS WAS GIVEN FOR THE REFERENCE

MR-2193

Page Fail Word (TOPS-10 Only)



NOTE: REFER TO OTHER PAGE FAIL WORD FOR BIT DEFINITIONS.

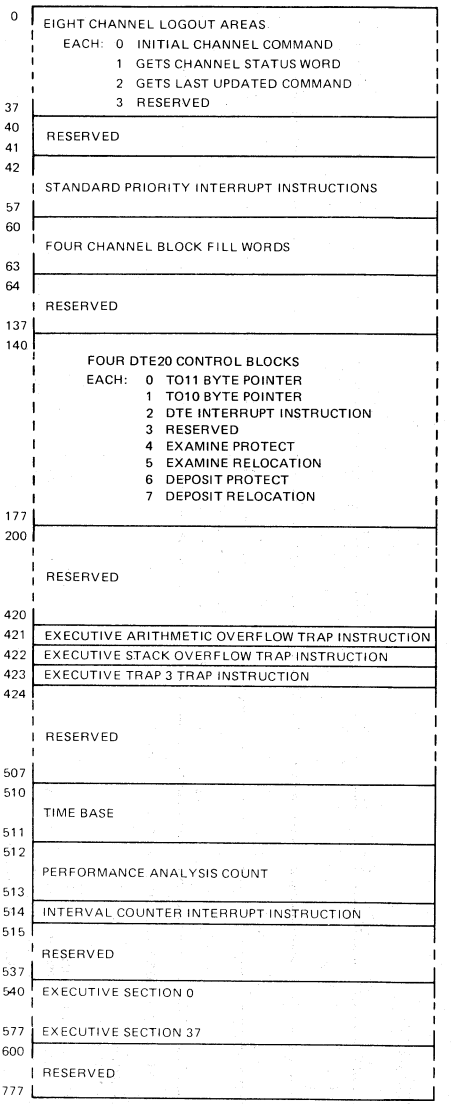
0 = EXEC MODE
1 = USER MODE

<01:05>	PAGE FAIL CODES	
	21	PROPRIETARY VIOLATION
	22	REFILL ERROR
	23	ADDRESS FAILURE
<01:05>	25	PAGE TABLE PARITY ERROR
CONT	36	AR DATA PARITY ERROR
	37	ARX DATA PARITY ERROR

MR-3823

EXECUTIVE PROCESS TABLE

(ADDRESSED FROM EBR)

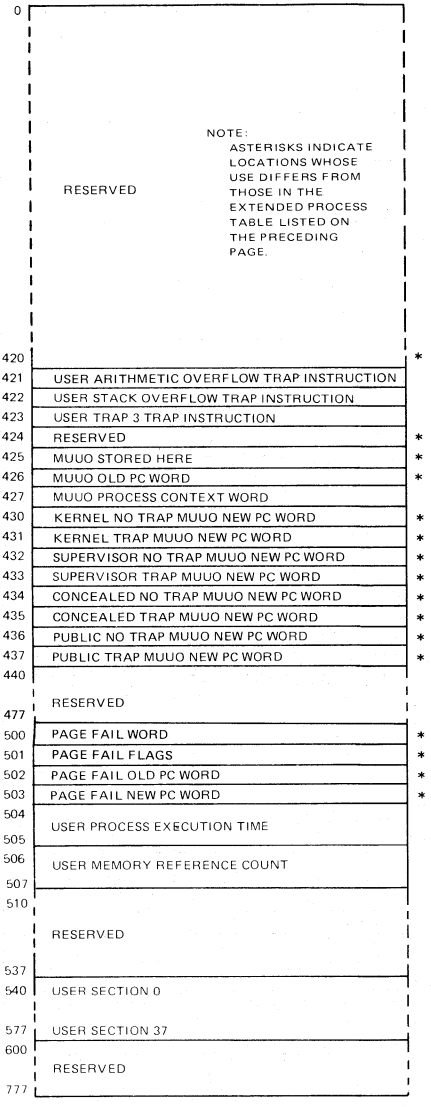


SINGLE–SECTION TOPS-20 PROCESS
TABLE CONFIGURATION

MR-3702

USER PROCESS TABLE

(ADDRESSED FROM UBR)

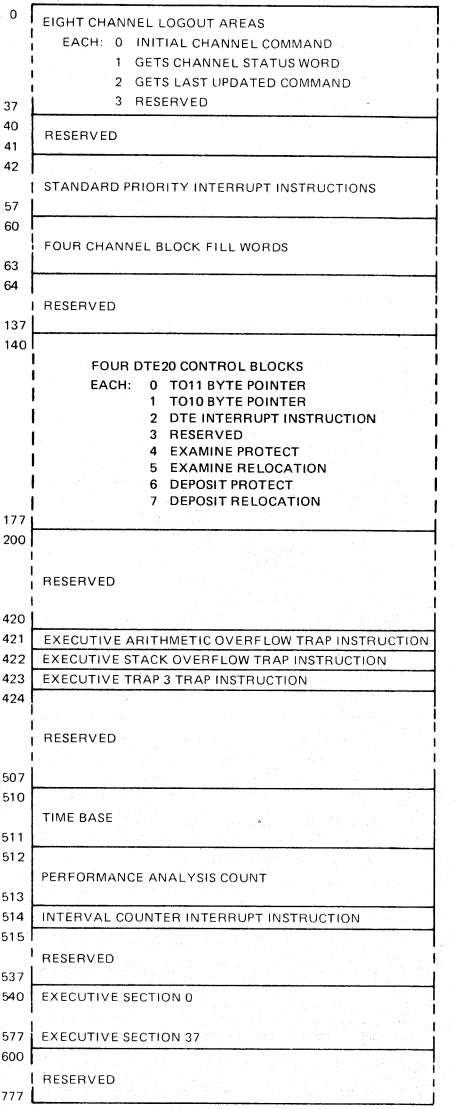


SINGLE-SECTION TOPS-20 PROCESS TABLE CONFIGURATION

MR-3703

EXECUTIVE PROCESS TABLE

(ADDRESSED FROM EBR)

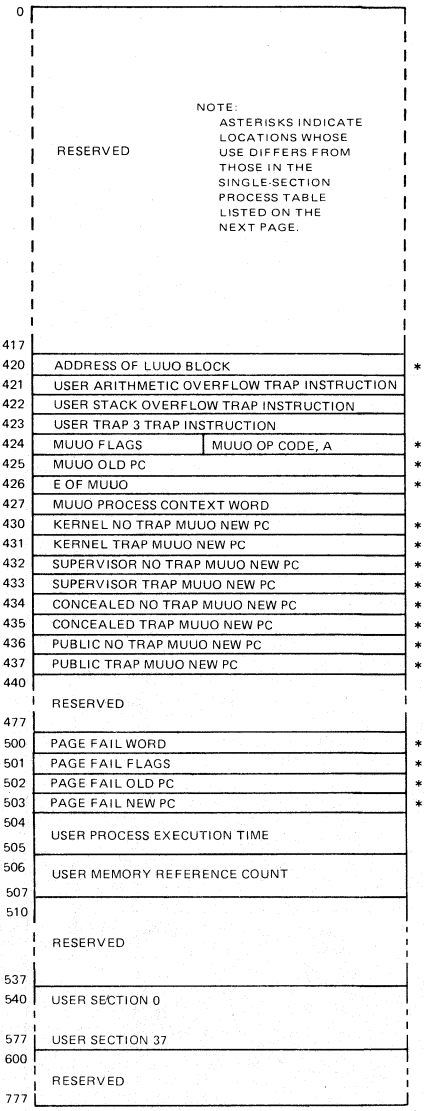


EXTENDED TOPS - 20 PROCESS TABLE
CONFIGURATION

MR-3700

USER PROCESS TABLE

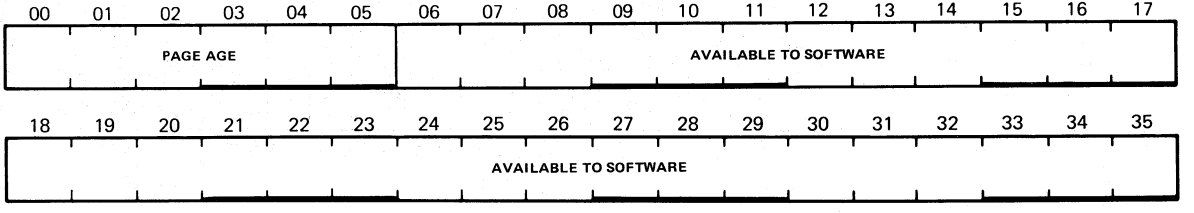
(ADDRESSED FROM UBR)



EXTENDED TOPS - 20 PROCESS TABLE
CONFIGURATION (CONT)

MR-3701

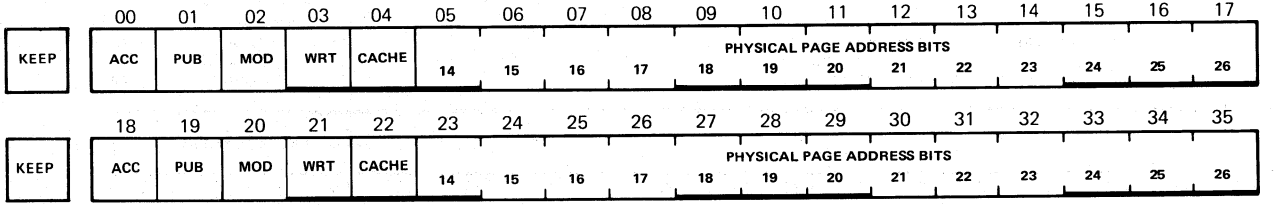
CST ENTRY



NOTE: AGE TRAP OCCURS IF BITS <00:05> EQUAL ZERO.

MR-2152

Page Map Entry (TOPS-20 Only)



00:18 0 = REFILL REQUIRED TO DETERMINE PAGE ACCESSIBILITY
1 = ACCESSIBLE

01 & 19 0 = PRIVATE
1 = PUBLIC

02 & 20 0 = PAGE NOT MODIFIED
1 = PAGE MODIFIED

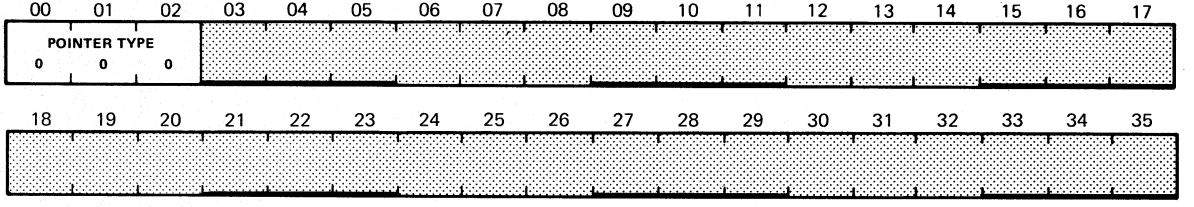
03 & 21 0 = WRITE-PROTECTED
1 = WRITABLE

04 & 22 0 = CACHE-LOOK BUT DO NOT LOAD
1 = CACHEABLE

NOTE: KEEP BIT 0 = PAGE WILL BE INVALIDATED ON DATAO PAGE
1 = PAGE WILL NOT BE INVALIDATED ON DATAO PAGE

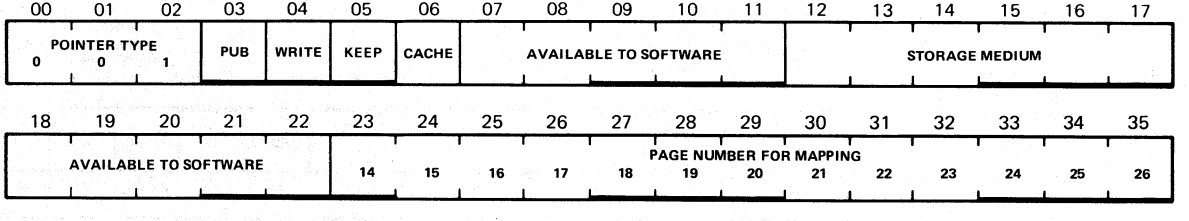
MR-3828

MAP POINTER — No Access (TOPS-20 Only)



MR-3831

MAP POINTER — Immediate (TOPS-20 Only)



03 0 = PRIVATE
1 = PUBLIC

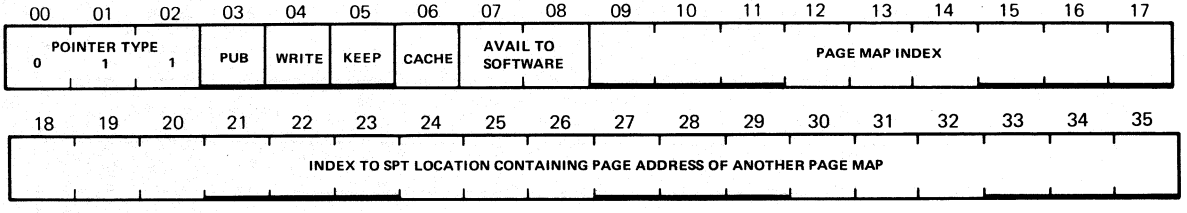
04 0 = WRITE PROTECTED
1 = WRITABLE

06 0 = CACHE-LOOK BUT DO NOT LOAD
1 = CACHEABLE

<12:17> NONZERO INDICATES PAGE NOT IN MEMORY

MR-2149

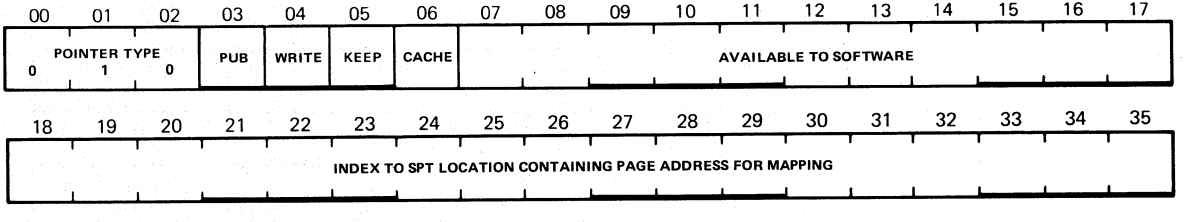
MAP POINTER – Indirect (TOPS-20 Only)



NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

MR-2151

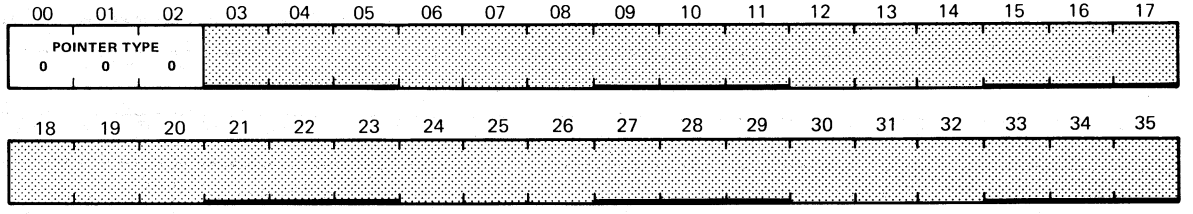
MAP POINTER – Shared (TOPS-20 Only)



NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

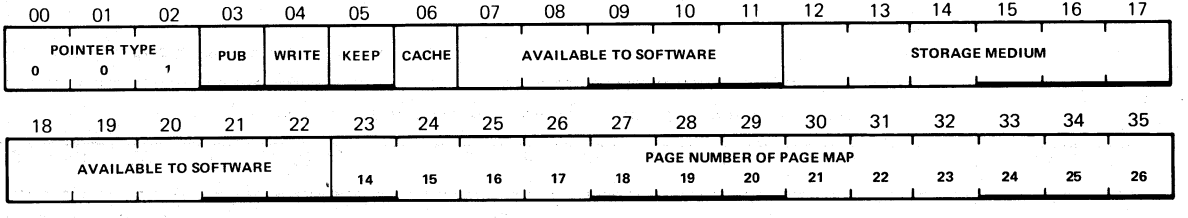
MR-2150

SECTION POINTER – No Access (TOPS-20 Only)



MR-3832

SECTION POINTER – Immediate (TOPS-20 Only)



03 0 = PRIVATE
1 = PUBLIC

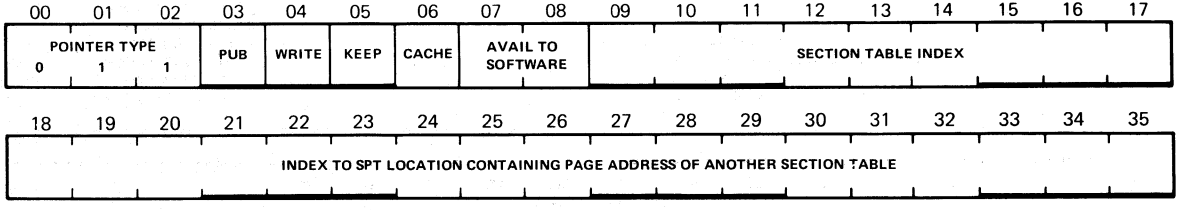
04 0 = WRITE-PROTECTED
1 = WRITABLE

06 0 = CACHE-LOOK BUT DO NOT LOAD
1 = CACHEABLE

<12:17> NONZERO INDICATES PAGE MAP IS NOT IN MEMORY

MR-15041

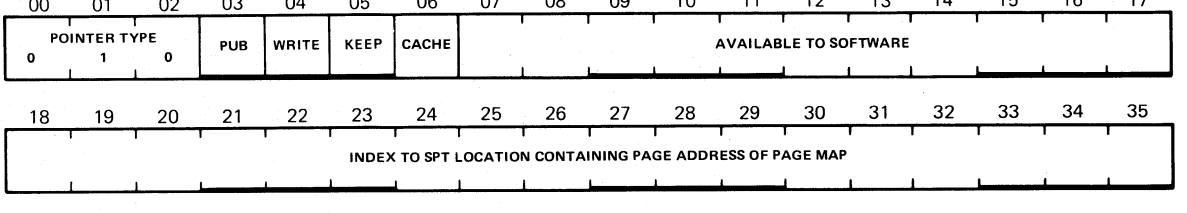
SECTION POINTER — Indirect (TOPS-20 Only)



NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

MR-15042

SECTION POINTER — Shared (TOPS-20 Only)

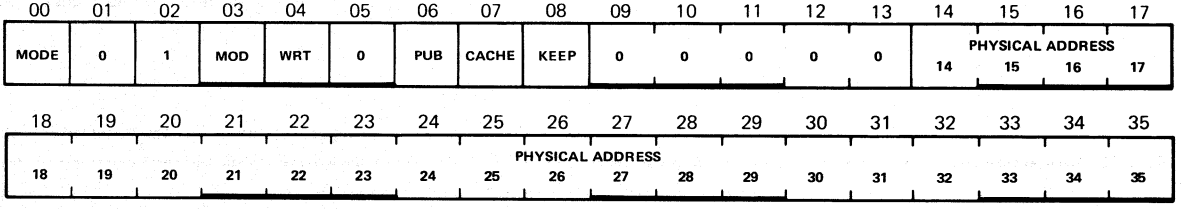


NOTE: REFER TO IMMEDIATE POINTER FOR BIT DEFINITIONS.

MR-15043

Map (TOPS-20 Only)

257000



NOTE: THIS REPRESENTS THE CONTENTS OF AC IF NO ERRORS OCCURRED.

00 0 = EXEC MODE
1 = USER MODE

03 0 = PAGE NOT MODIFIED
1 = PAGE MODIFIED

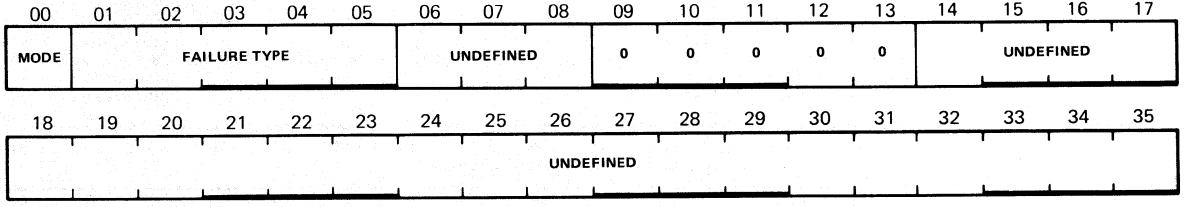
04 0 = WRITE-PROTECTED
1 = WRITABLE

06 0 = PRIVATE
1 = PUBLIC

07 0 = CACHE-LOOK BUT DO NOT LOAD
1 = CACHEABLE

MR-3829

Map (TOPS-20 Only)



NOTE: THIS REPRESENTS THE CONTENTS OF AC IF A MAP ERROR IS DETECTED.

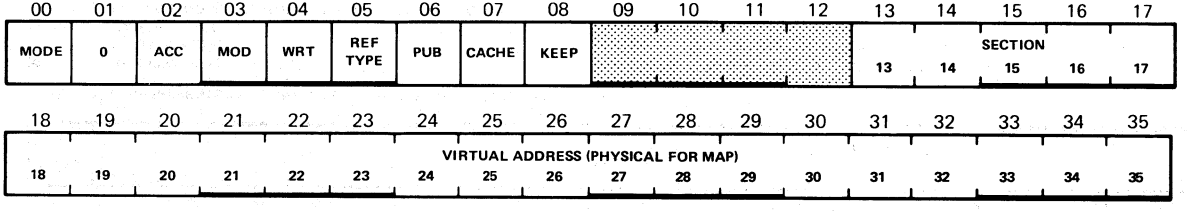
00 0 = EXEC MODE
1 = USER MODE

<01:05> FAILURE TYPE
00 = AGE, NO ACCESS OR NOT-IN-MEMORY IN A REFILL
21 = PROPRIETARY VIOLATION
25 = PAGE TABLE PARITY ERROR

<01:05> 27 = ILLEGAL ADDRESS - SECTION > 37
CONT 36 = AR DATA PARITY ERROR

MR-3830

Page Fail Word (TOPS-20 Only)



00 0 = EXEC MODE
1 = USER MODE

02 0 = REFILL REQUIRED TO DETERMINE PAGE ACCESSIBILITY
1 = ACCESSIBLE

03 0 = PAGE NOT MODIFIED
1 = PAGE MODIFIED

04 0 = WRITE-PROTECTED
1 = WRITABLE

05 0 = READ-ONLY REFERENCE
1 = REFERENCE INVOLVED A WRITE

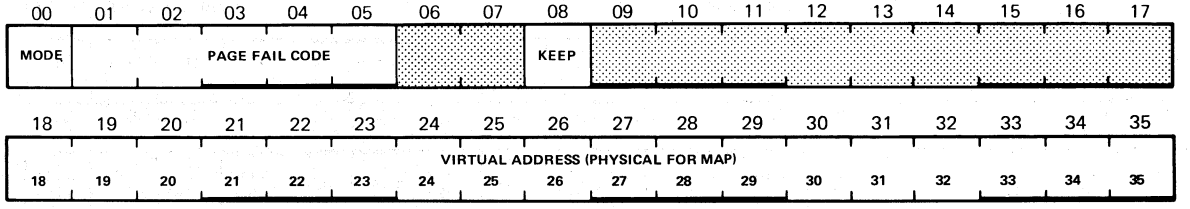
06 0 = PRIVATE
1 = PUBLIC

07 0 = CACHE-LOOK BUT DO NOT LOAD
1 = CACHEABLE

08 A 1 INDICATES A VIRTUAL ADDRESS WAS GIVEN FOR THE REFERENCE

MR-3826

Page Fail Word (TOPS-20 Only)



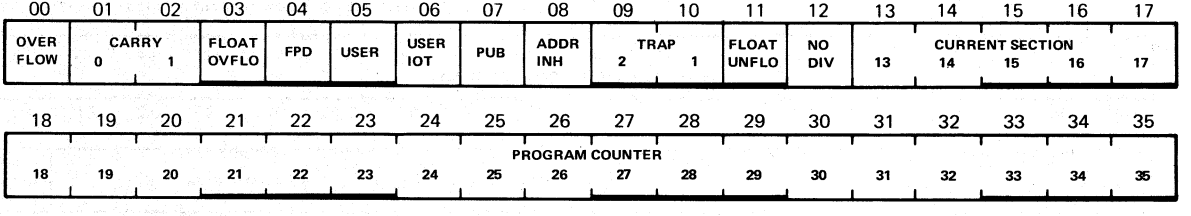
NOTE: REFER TO OTHER PAGE FAIL WORD FOR BIT DEFINITIONS.

0 = EXEC MODE
1 = USER MODE

<01:05>	PAGE FAIL CODES	
	21	PROPRIETARY VIOLATION
	23	ADDRESS FAILURE
	24	ILLEGAL INDIRECT
<01:05>	25	PAGE TABLE PARITY ERROR
CONT	27	ILLEGAL ADDRESS - SECTION > 37
	36	AR DATA PARITY ERROR
	37	ARX DATA PARITY ERROR

MR-3827

PC — Program Counter

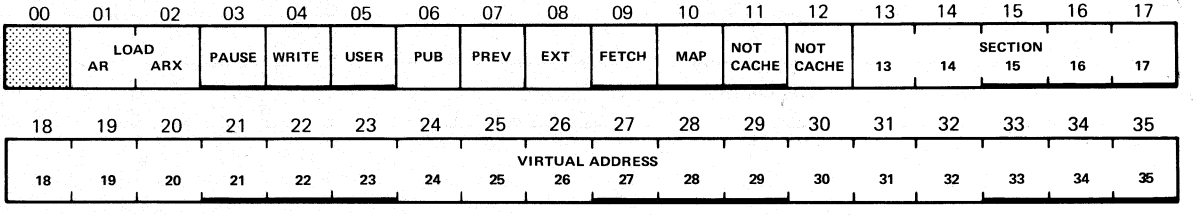


04 FIRST PART DONE

08 ADDRESS FAILURE INHIBIT

MR-2192

VMA – FORMAT

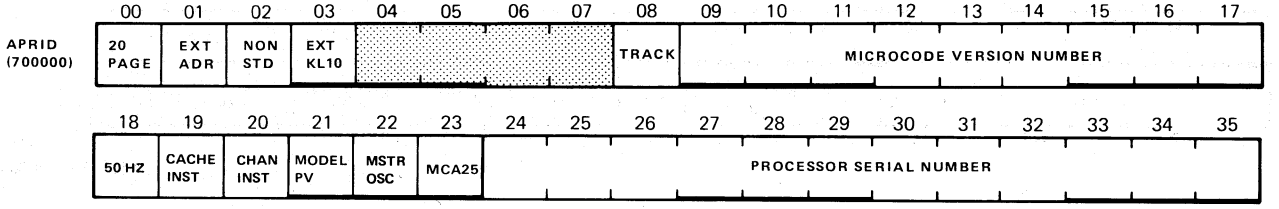


NOTE: THIS IS THE INTERMEDIATE WORD STORED BY THE MICROCODE AT LOCATION SV. VMA DURING A PAGE TABLE REFILL. THE STATUS BITS MAY BE READ VIA DIAGNOSTIC FUNCTIONS.

01	FR 105 BIT 18(1)
02	FR 106 BIT 18(1)
03	FR 103 BIT 18(1)
04	FR 104 BIT 18(1)
05	FR 104 BIT 19(1)
06	FR 105 BIT 19(1)
07	FR 106 BIT 19(0)
08	FR 107 BIT 19(0)
09	FR 107 BIT 20(1) KL10 PV ONLY
10	FR 107 BIT 23(0)
11	FR 104 BIT 23(1)
12	FR 105 BIT 23(1)

MR-2196

BLKI APR,

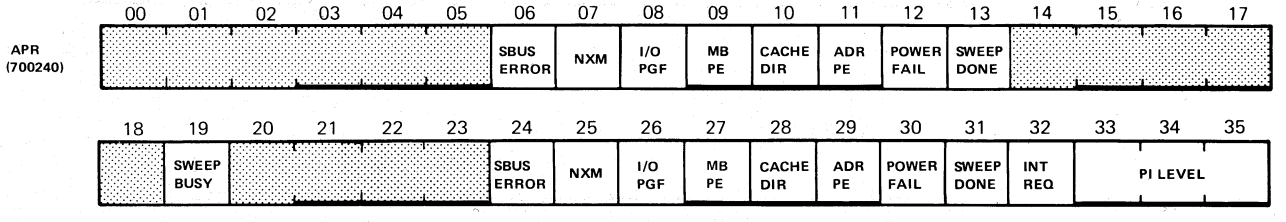


NOTE: BITS <00:08> ARE MICROCODE OPTIONS
BITS <18:23> ARE HARDWARE OPTIONS

00	MICROCODE IS FOR TOPS-20 PAGING
01	MICROCODE HANDLES EXTENDED ADDRESSES
02	NON-STANDARD MICROCODE
03	CPU IS AN EXTENDED KL10
08	MICROCODE VERSION SUPPORTS TRACKING
19	CACHE INSTALLED
20	CHANNELS INSTALLED
21	MODEL PV TYPE PROCESSOR
22	MASTER OSCILLATOR (KW20 OPTION)
23	OPTION BIT FOR MCA25

MR-2067

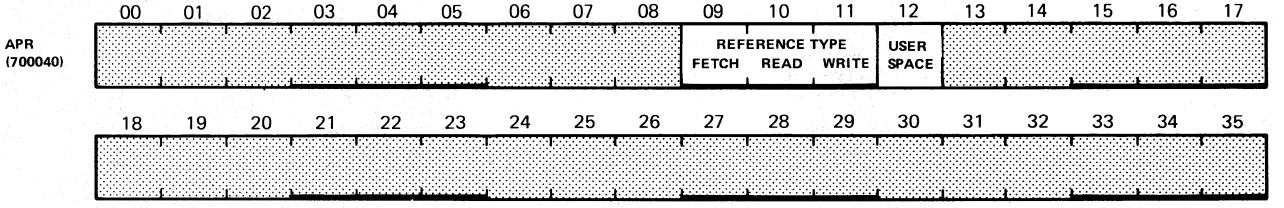
CONI APR,



06	INTERRUPT ON: SBUS ERROR	24	SBUS ERROR
07	: NONEXISTENT MEMORY	25	NONEXISTENT MEMORY
08	: I/O PAGE FAIL	26	I/O PAGE FAILURE
09	: MB PARITY ERROR	27	MB PARITY ERROR
10	: CACHE DIR PARITY ERROR	28	CACHE DIRECTORY PARITY ERROR
11	: ADDRESS PARITY ERROR	29	ADDRESS PARITY ERROR
12	: POWER FAILURE	30	POWER FAILURE
13	: CACHE SWEEP DONE	31	CACHE SWEEP DONE
19	CACHE SWEEP IN PROGRESS	32	INTERRUPT REQUEST

MR-2064

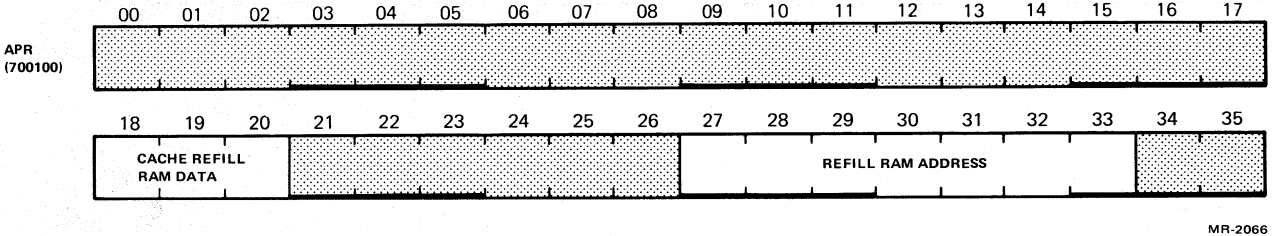
DATAI APR,



NOTE: REFER TO DATAO APR FOR BIT DEFINITIONS

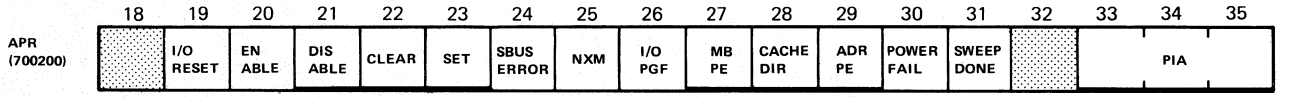
MR-2068

BLKO APR, (WRFIL)



MR-2066

CONO APR,

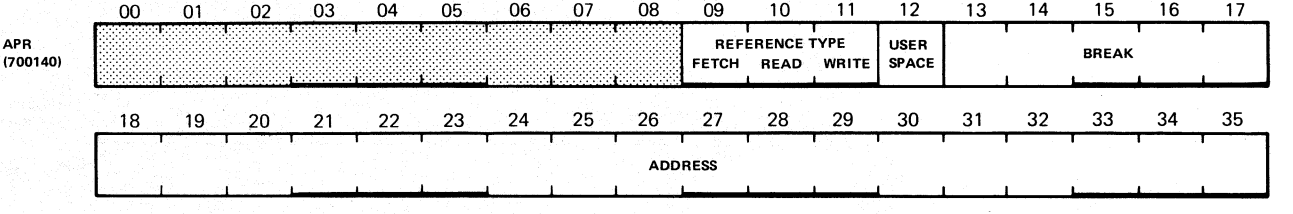


20	ENABLE	SELECTED FLAGS <24:31>
21	DISABLE	SELECTED FLAGS <24:31>
22	CLEAR	SELECTED FLAGS <24:31>
23	SET	SELECTED FLAGS <24:31>

24	SELECT FLAG:	SBUS ERROR
25	:	NON-EX-MEMORY
26	:	I/O PAGE FAIL
27	:	MB PARITY ERROR
28	:	CACHE DIR PARITY ERROR
29	:	ADDRESS PARITY ERROR
30	:	POWER FAIL
31	:	CACHE SWEEP DONE

MR-2063

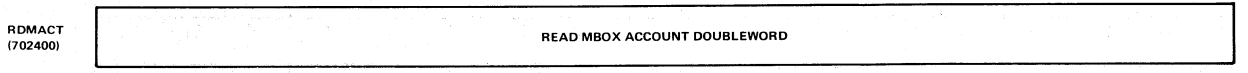
DATAO APR,



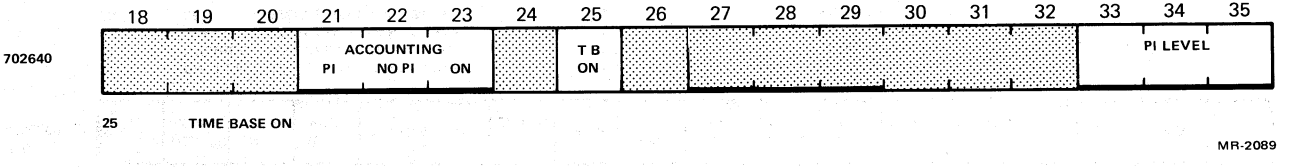
<09:12> ADDRESS BREAK ENABLES

MR-2065

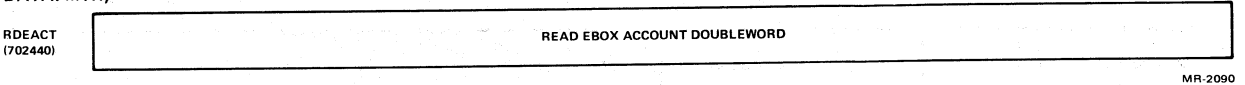
BLKI MTR,



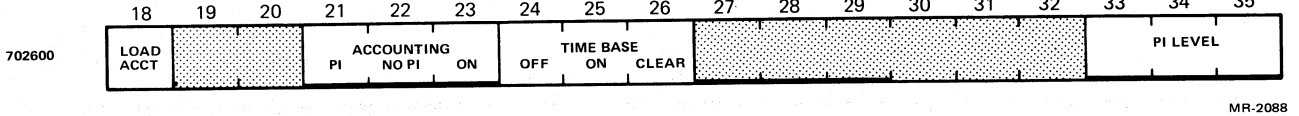
CONI MTR,



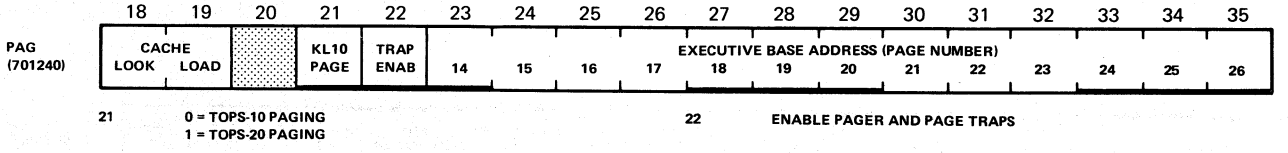
DATAI MTR;



CONO MTR,

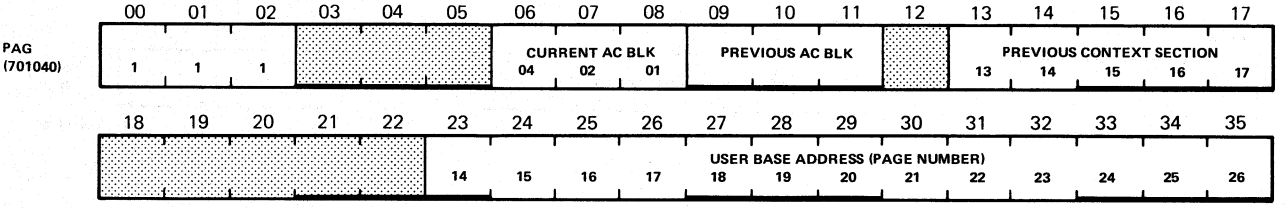


CONI PAG,



MR-2145

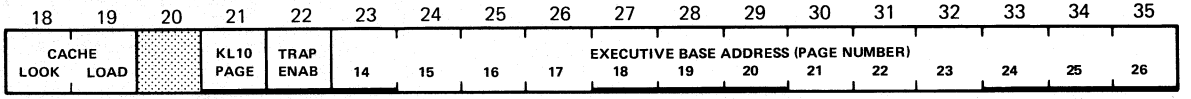
DATAI PAG,



MR-2147

CONO PAG,

(701200)

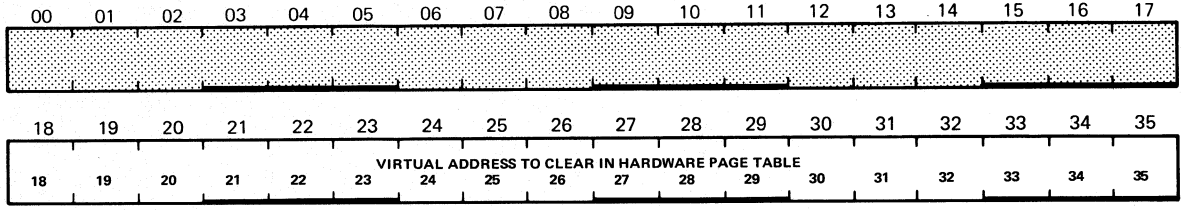


NOTE: REFER TO CONI PAG FOR BIT DEFINITIONS.

MR-2144

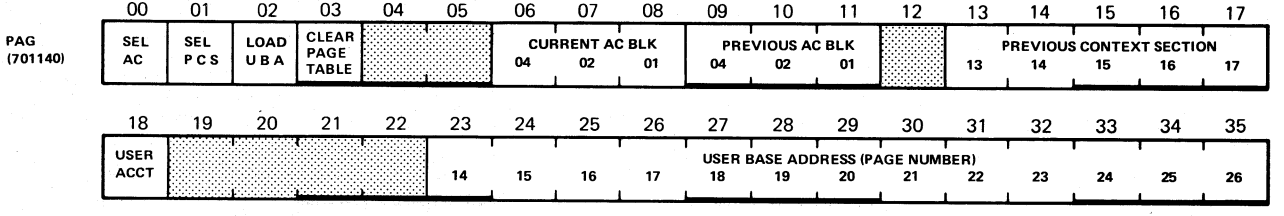
BLKO PAG, (CLRPT)

PAG
(701100)



MR-2148

DATAO PAG



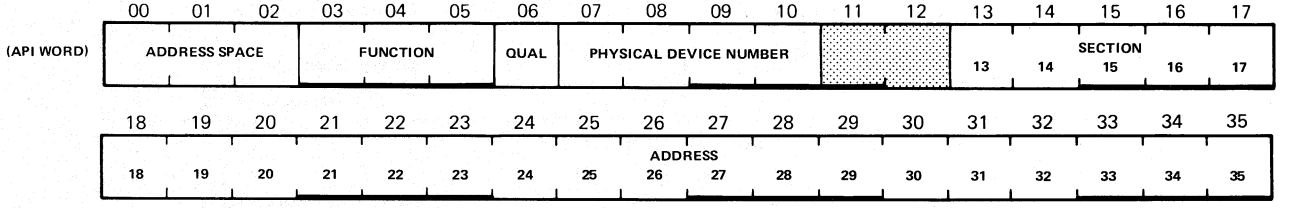
NOTE:

BIT3 = 0 INVALIDATE ALL PAGE TABLE ENTRIES
BIT3 = 1 INVALIDATE NONKEEP ENTRIES ONLY

MR-2146

00	SELECT AC BLOCKS <06:08>	02	LOAD USER BASE ADDRESS
01	SELECT PREVIOUS CONTEXT SECTION <09:11>	18	1 = DO NOT UPDATE USER ACCOUNTS
03	CLEAR PAGE TABLE		

IOP FUNCTION WORD



<00:02> 0 = EPT 1 = EXECUTE VIRTUAL
4 = PHYSICAL

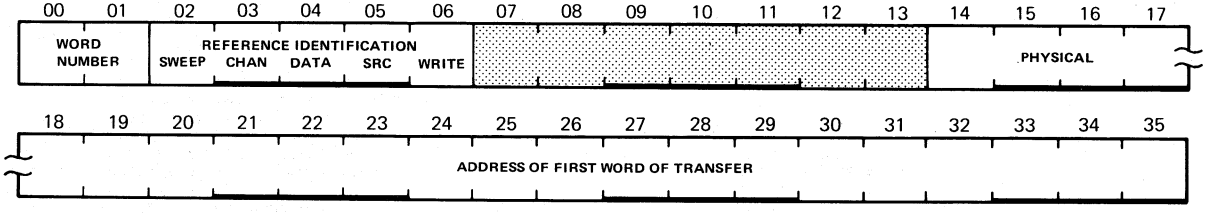
<03:05> 0 = STANDARD (40 + 2N) INTERRUPT
1 = STANDARD INTERRUPT (40 + 2N)
2 = VECTOR INTERRUPT [XCT (13-35)]
3 = INCREMENT [QUAL = > DECREMENT]
4 = DATAO (EXAMINE) [QUAL = > PROTECTED]
5 = DATAI (DEPOSIT) [QUAL = > PROTECTED]
6 = BYTE [QUAL = > TO -10]
7 = STANDARD (40 + 2n) INTERRUPT
n = DTE NUMBER

<07:10> 0–7 = RH20
10–13 = DTE20
17 = DIA 20

MR-2195

BLKI PI,

PI
(700400)
(RDERA)



02 REF MADE FOR CACHE SWEEP
03 REF MADE FOR CHANNEL XFER
04 DATA
05 SOURCE
06 WRITE

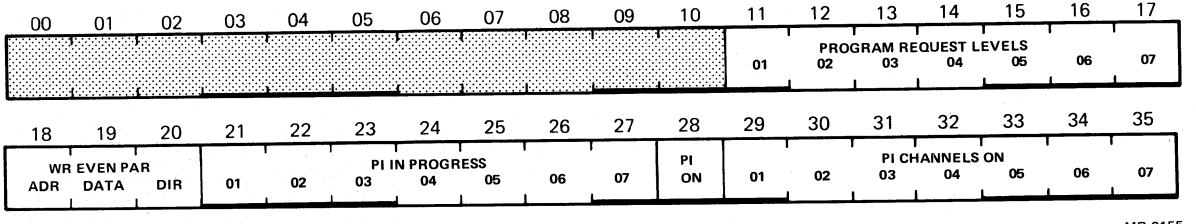
BIT <04:06> COMBINATIONS

04	05	06 (WRITE = 0)	06 (WRITE = 1)
0	0	MEMORY (RD OR RPW)	CHAN STORE STATUS
0	1		CHAN STORE DATA
1	0		EBOX STORE FROM AR
1	1	READ FROM CACHE (PAGE REFILL OR CHAN READ)	CACHE WRITEBACK

MR-2162

CONI PI,

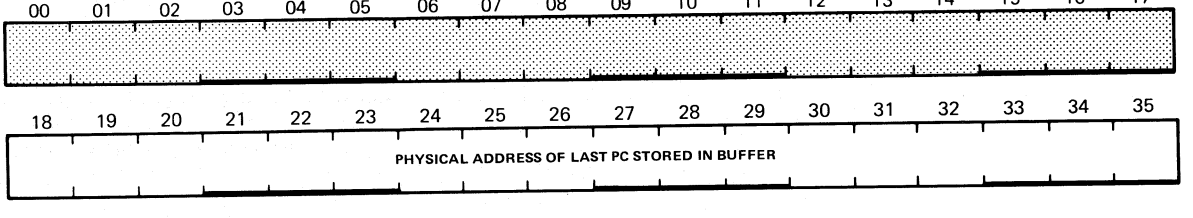
PI
(700640)



MR-2155

DATAI PI,

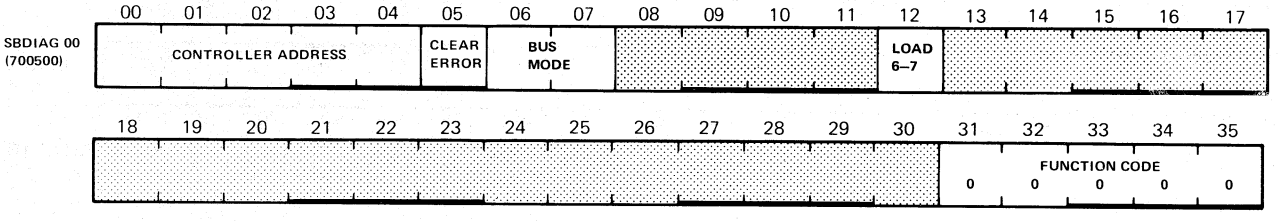
PI
(700440)



NOTE: TRACKS ONLY

MR-2157

BLKO PI, (SBus Diagnostic Function Code 00) DMA



NOTE: THIS BIT MAP APPLIES TO DMA20S ONLY.

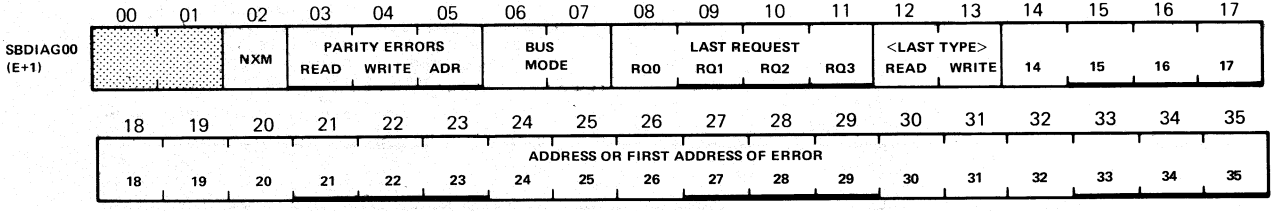
<00:04> CONTROLLER ADDRESS
04 = DMA20

05 CLEAR ERROR - CLEARS CONTROLLER'S ERROR FLAGS NXM, RD PE, WR PE AND ADR PE

<06:07> BUS MODE
0 = OFF LINE
1 = 1 BUS MODE
2 = 2 BUS MODE
3 = 4 BUS MODE

12 LOAD ENABLE - ENABLES LOADING OF BITS 6–7.
0 = READ ONLY
1 = LOAD AND READ BACK

MR-3814

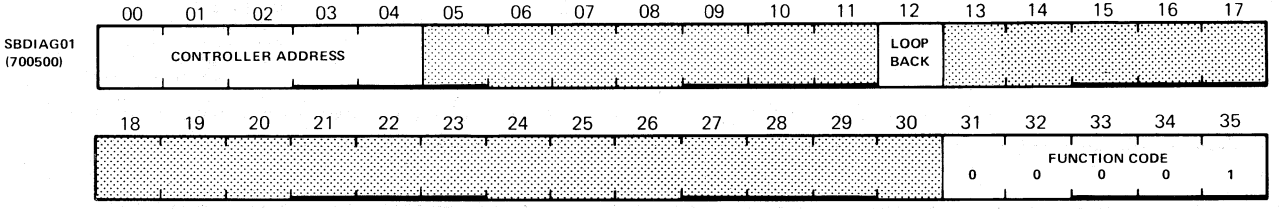


NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 00). THIS BIT MAP APPLIES TO DMA20S ONLY.

<06:07> BUS MODE
0 = OFF LINE
1 = 1 BUS MODE
2 = 2 BUS MODE
3 = 4 BUS MODE

MR-3815

BLKO PI, (SBus Diagnostic Function Code 01) DMA

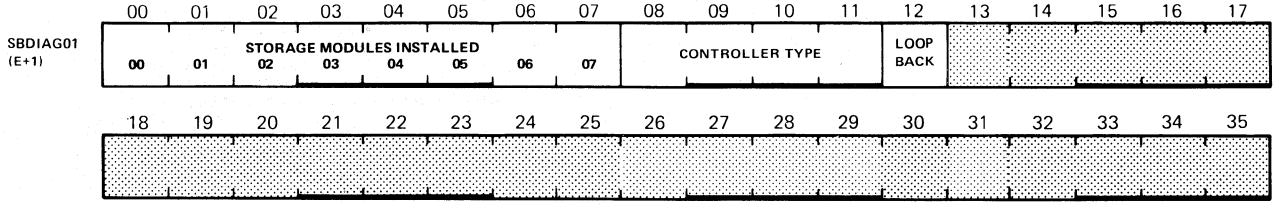


NOTE: THIS BIT MAP APPLIES TO DMA20S ONLY.

<00:04> REFER TO SBDIAG FUNCTION 00

12 SET LOOP-AROUND MODE-INHIBITS READ/WRITE CURRENTS IN STORAGE MODULES. A DIAGNOSTIC FEATURE FOR CHECKING DATA PATH INDEPENDENT OF CORE ACTIVITY

MR-3816



NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI (FUNCT 01). THIS BIT MAP APPLIES TO DMA20S ONLY.

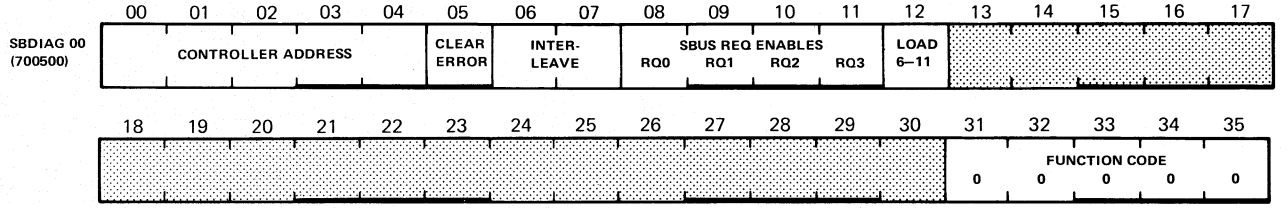
<00:07> DMA ALWAYS RETURNS 0.

<08:11> MEMORY ID-THESE HARDWIRED BITS IDENTIFY MEMORY TYPE.
00 = CUSTOMER UNIT
01 = MA20
02 = DMA20
03 = MB20
05 = MF20 MOS

12 LOOP-AROUND MODE – INDICATES CONTROLLER IN LOOP-AROUND MODE.

MR-3817

BLKO PI, (SBus Diagnostic Function Code 00) MA/MB



NOTE: THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

<00:04> CONTROLLER ADDRESS-EACH MA20 CONTROLLER HAS A HARDWIRED ADDRESS 0-3. MC0 AND MC1 CONNECT TO SBUS 0; MC2 AND MC3 TO SBUS 1
00 = MC0 FIRST 128K (MA20) OR
01 = MC1 FIRST 256K (MB20)
02 = MC2 SECOND 128K (MA20) OR
03 = MC3 SECOND 256K (MB20)
04 = DMA20 (NOT AN MA20 OR MB20 ADDRESS)

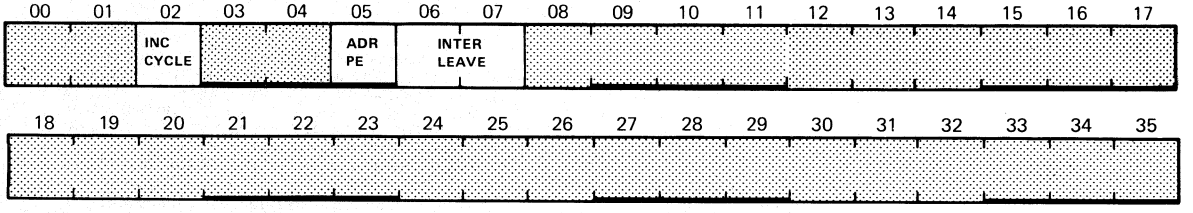
05 CLEAR ERROR-CLEARS CONTROLLER'S INTERNAL ERROR FLAGS INCOMPLETE REQUEST AND ADR PAR ERR.

<06:07> INTERLEAVE
0 = OFF-LINE FOR DMA20 (NOT AN MA20 OR MB20 OPERATING MODE)
1 = NO INTERLEAVE
2 = TWO WAY INTERLEAVING
3 = FOUR WAY INTERLEAVING

<08:11> SET REQUEST ENABLES-ASSIGNS CONTROLLER ODD-EVEN STATUS
00 = CONTROLLER OFF-LINE
05 = CONTROLLER ODD (2 WAY AND 4 WAY INTERLEAVE MODES)
12 = CONTROLLER EVEN (2 AND 4 WAY INTERLEAVE MODES)
17 = CONTROLLER ODD AND EVEN (NO INTERLEAVE MODES)

12 LOAD ENABLE-ENABLES LOADING OF BITS 6–11.
0 = READ ONLY
1 = LOAD AND READ BACK

MR-2158



NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 00). THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

02 INCOMPLETE REQUEST-INDICATES CONTROLLER ACTIVE FOR 10.2 MICROSECONDS: HUNG CONTROLLER.

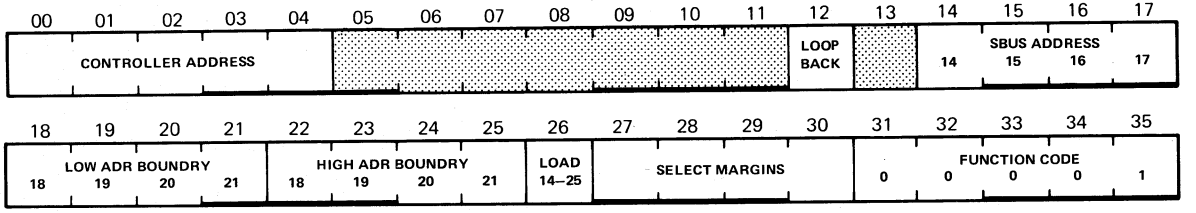
05 ADDRESS PARITY ERROR-INDICATES BAD PARITY DETECTED FOR INFORMATION ON SBUS ADR, RQn, RD RQ, AND WR RQ LINES.

<06:07> INTERLEAVE MODE-INDICATES INTERLEAVE MODE LOADED IN FIRST HALF OF FUNCTION 0.

MR-2159

BLKO PI, (SBus Diagnostic Function Code 01) MA/MB

SBDIAG01
(700500)



NOTE: THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

<00:04> REFER TO SBDIAG FUNCTION 00

12 SET LOOP-AROUND MODE-INHIBITS READ/WRITE CURRENTS IN STORAGE MODULES. A DIAGNOSTIC FEATURE FOR CHECKING DATA PATH INDEPENDENT OF CORE ACTIVITY

<14:17> SET MEMORY ADDRESS-CORRESPOND TO SBUS ADR 14–17. MUST MATCH THE SBUS ADDRESS LINES IF A CONTROLLER IS TO RESPOND TO A MEMORY REFERENCE

<18:21> SET LOWER ADDRESS BOUNDARY-CORRESPOND TO SBUS ADR 18–21. ACT IN CONJUNCTION WITH MEMORY ADDRESS (BITS 14–17) TO SPECIFY LOWER ADDRESS LIMIT

<22:25> SET UPPER ADDRESS BOUNDARY-CORRESPOND TO SBUS ADR 18–21. ACT IN CONJUNCTION WITH MEMORY ADDRESS (BITS 14–17) TO SPECIFY UPPER ADDRESS LIMIT

26 LOAD ENABLE – ENABLE LOADING BITS <14:25>
0 = READ ONLY
1 = LOAD AND READ BACK

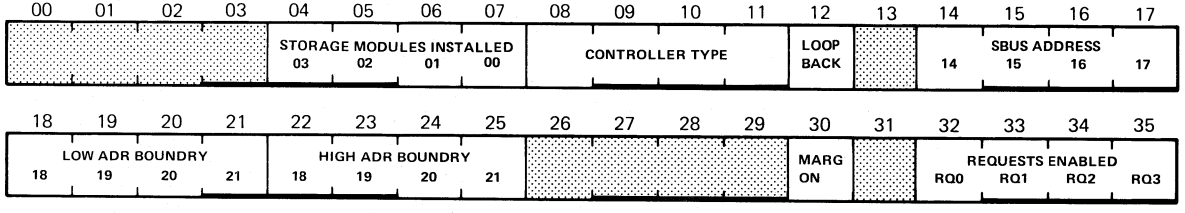
<27:35> SET MARGIN CONTROL-TURN ON MARGIN CONTROL AS SPECIFIED BELOW. ONLY ONE MARGIN SHOULD BE TURNED ON AT ANY ONE TIME

27	28	29	30	
0	0	0	0	NO OP
0	0	0	1	CLEAR ALL MARGINS
0	0	1	X	CURRENT MARGIN
0	1	0	X	STROBE MARGIN
1	0	0	X	THRESHOLD MARGIN

X = 0 – LOW MARGIN
X = 1 – HIGH MARGIN

MR-2160

SBDIAG01
(E+1)



NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI (FUNCT 01). THIS BIT MAP APPLIES TO MA20 AND MB20 MEMORIES ONLY.

<04:07> STORAGE MODULES CONNECTED – THESE HARDWIRED BITS INDICATE THE NUMBER OF STORAGE MODULES CONNECTED TO A CONTROLLER.
1 = SM CONNECTED
0 = SM NOT CONNECTED

<08:11> MEMORY ID – THESE HARDWIRED BITS IDENTIFY MEMORY TYPE.
00 = CUSTOMER UNIT
01 = MA20
02 = DMA20
03 = MB20

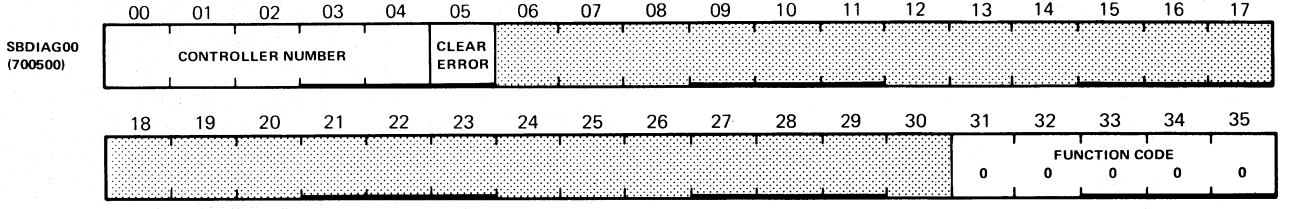
12 LOOP-AROUND MODE – INDICATES CONTROLLER IN LOOP-AROUND MODE.

<14:25> ADDRESS BOUNDARIES – INDICATES ADDRESS BOUNDARIES LOCATED IN FIRST HALF OF FUNCTION 1.

30 MARGINS SELECTED – INDICATES THAT CURRENT, STROBE, OR THRESHOLD MARGIN CONTROL IS ON.

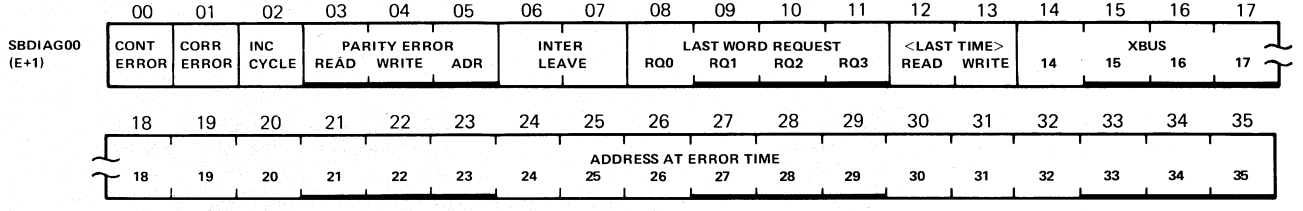
MR-2161

BLKO PI (SBus Diagnostic Function Code 00) MF/MG20



05 CLEAR ERRORS – REFER TO FUNCT 0
(E+1) BITS <00:05>

MR-2163



NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 00). THIS BIT MAP APPLIES TO MF20/MG20 MEMORIES ONLY

00 CONTROLLER ERROR – REFER TO FUNCT 2 (E+1) BITS <28:30>

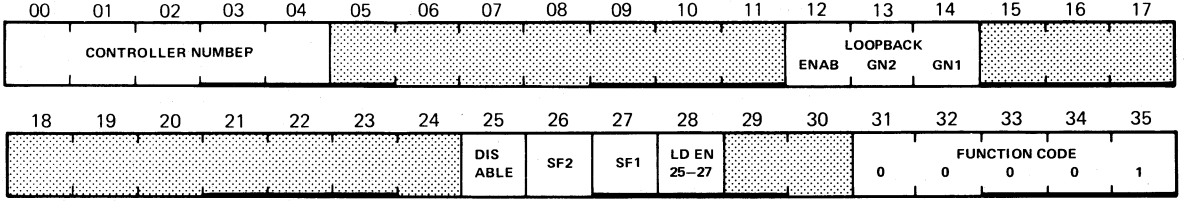
01 CORRECTABLE READ PARITY ERROR

02 INCOMPLETE MEMORY CYCLE

MR-2164

BLKO PI (SBus Diagnostic Function Code 01) MF/MG20

SBDIAG01
(700500)



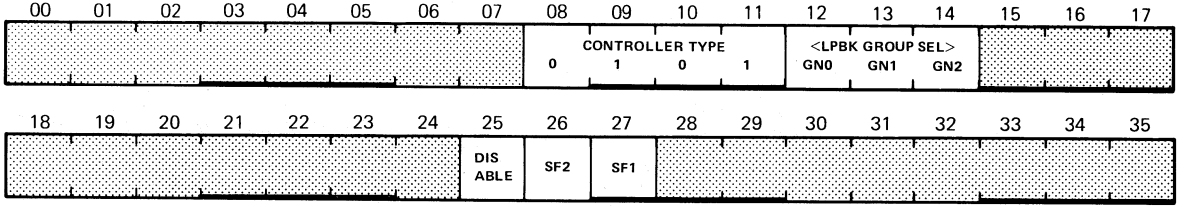
NOTE: THIS BIT MAP APPLIES TO MF20/MG20 MEMORIES ONLY. BITS <26:27> ARE SOFTWARE FLAGS. THEY DO NOT AFFECT THE HARDWARE, NOR DOES THE HARDWARE AFFECT THEM.

12	ENABLE LOOPBACK
<13:14>	GROUP NUMBER TO LOOPBACK
25	DISABLE MF20/MG20 (PLACE OFF-LINE)

<26:27>	00 = MF20/MG20 JUST POWER UP
	01 = ALL RAMS EXCEPT ADDRESS RESPONSE RAM LOADED
	10 = ALL RAMS LOADED
	11 = ALL RAMS LOADED AND TGHA HAS BEEN RUN

MR-2165

SBDIAG01
(E+1)



NOTE: THIS BIT MAP APPLIES TO MF20/MG20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 01).

<08:11> CONTROLLER TYPE (5 = MF/MG20)

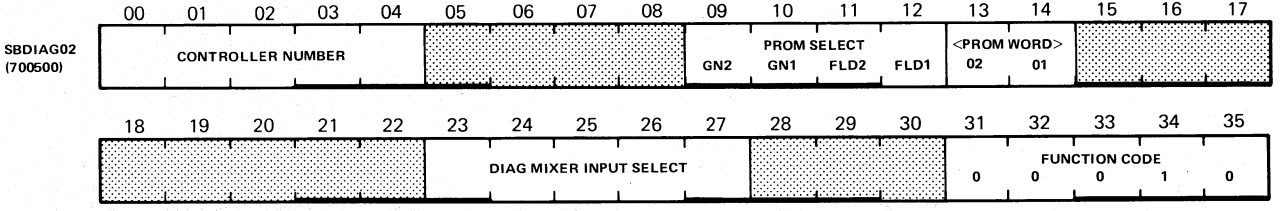
<12:14> LOOPBACK GROUP SELECTED

<25:27> REFER TO FUNCT 01 (E) BITS <25:27>

MR-2166

PI

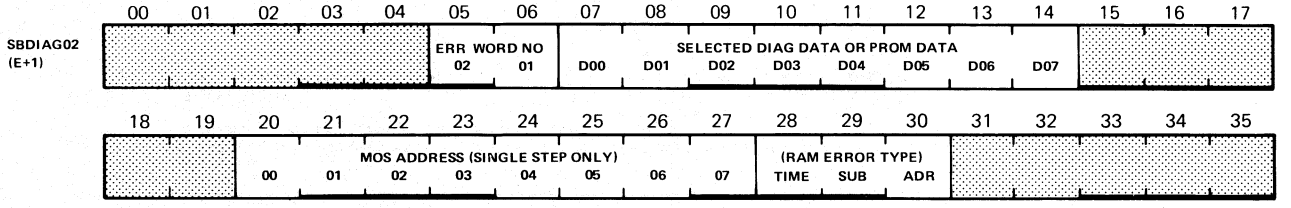
BLKO PI (SBus Diagnostic Function Code 02) MF/MG20



<23:27> WHEN ALL ZEROS, THIS FIELD INDICATES THAT THE CONTENTS OF BITS <07:14> DURING THE SECOND HALF OF THE DIAGNOSTIC CYCLE WILL BE PROM DATA.

<23:27> WHEN NOT ALL ZEROS, THE BITS ARE USED TO SELECT WHICH MF20 CONTROL SIGNALS WILL APPEAR IN <07:14> DURING THE SECOND HALF OF THE DIAGNOSTIC CYCLE (DIAGNOSTIC DATA).

MR-2167



NOTE: THIS BIT MAP APPLIES TO MF20/MG20 MEMORIES ONLY. E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 02).

<05:06> SPECIFY WHICH WORD IN QUAD WORD GROUP CAUSED ERROR

<07:14> REFER TO FUNCT 02 (E) BITS <23:27>

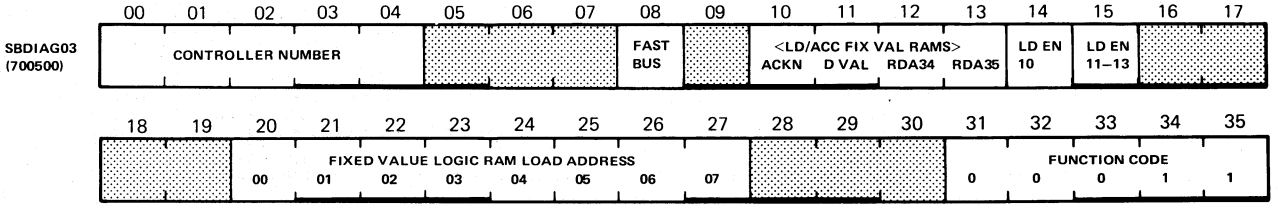
28 RAM TIMING ERROR

29 RAM SUBSTITUTION BIT ERROR

30 RAM ADDRESS RESPONSE ERROR

MR-2168

BLKO PI (SBus Diagnostic Function Code 03) MF/MG20

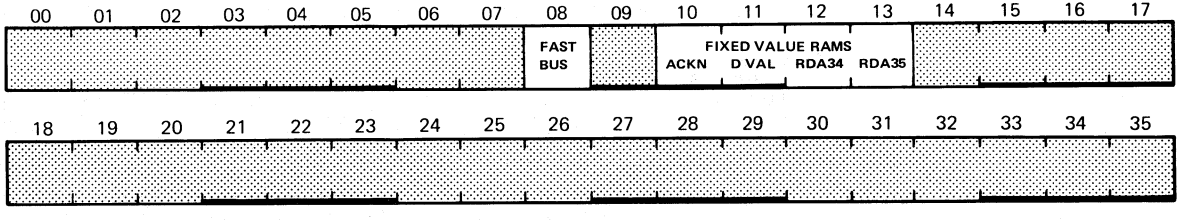


NOTE: THE FAST-BUS (BIT 08) IS DISCONNECTED INTERNALLY. IT IS LEFT IN ONLY FOR DIAGNOSTIC COMPATABILITY. THE ACKN RAM (BIT 10) USES ADDRESS BITS <21:27> ONLY.

10	P ACKN EN BIT	11	SET DATA VALID BIT
<10:13>	LOAD OR ACCESS FIXED VALUE RAMS	<12:13>	P RD ADR 34–35 BITS

MR-2169

SBDIAG03
(E+1)

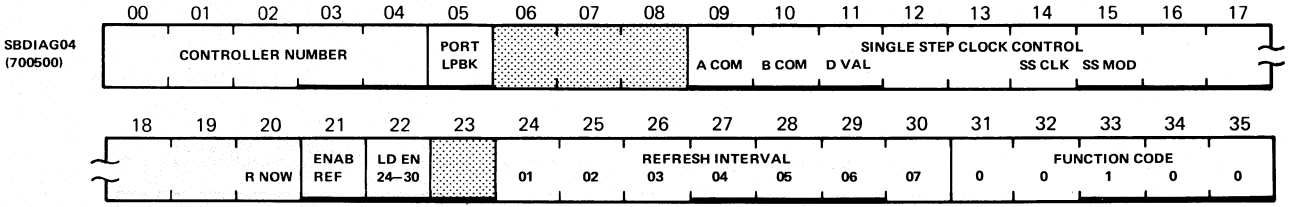


NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI. (FUNCT 03). REFER TO FUNCT 03 (E) FOR BIT DEFINITIONS.

MR-2170

PI

BLKO PI, (SBus Diagnostic Function Code 04) MF/MG20

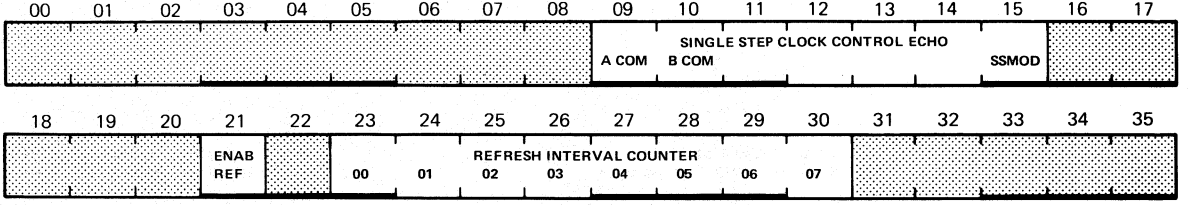


NOTE: IF 5 = 1 THE CONTROLLER WILL ONLY ECHO INFORMATION SENT OUT BY AN SBUS DIAG AS LONG AS THE PROPER CONTROLLER NUMBER IS GIVEN. ONLY A SBUS RESET CAN CLEAR THIS CONDITION.

05	PORT LOOPBACK	11	P DATA VALID IN
09	SIM A PHASE COMING	20	REFRESH NOW
10	SIM B PHASE COMING	21	ENABLE REFRESH

MR-2171

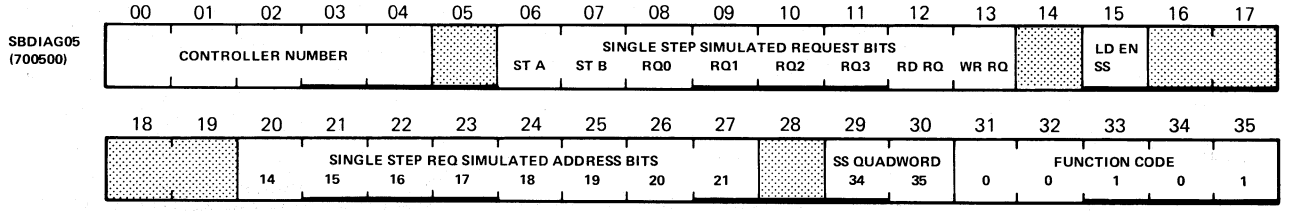
SBDIAG04
(E+1)



NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF A BLKO PI, (FUNCT 04), REFER TO FUNCT 4 (E) FOR BIT DEFINITIONS.

MR-2172

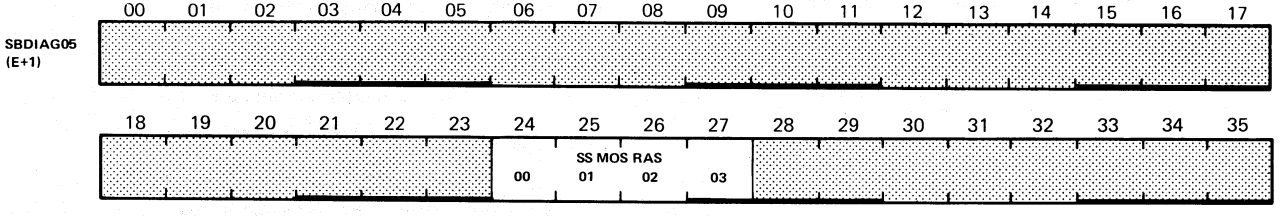
BLKO PI, (SBus Diagnostic Function Code 05) MF/MG20



06 DIAGNOSTIC START A
07 DIAGNOSTIC START B

<29:30> SELECTS QUADWORD FOR DIAGNOSTIC SINGLE STEP OPERATION

MR-2173



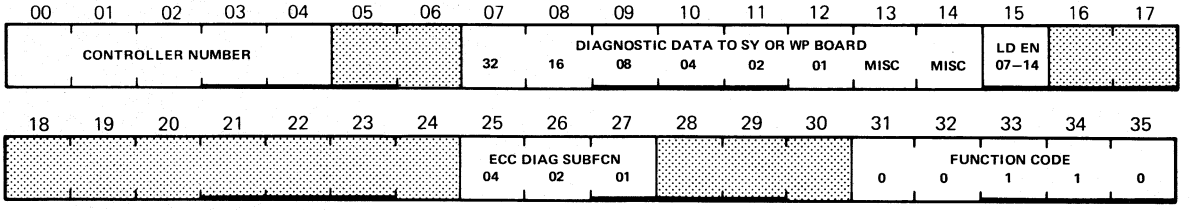
NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 05).

<24:27> ROW ADDRESS STROBE (RAS) BITS

MR-2174

BLKO PI, (SBus Diagnostic Function Code 06) MF/MG20

SBDIAG06
(700500)



<07:14> AN 8-BIT FIELD USED TO SET UP THE DIAGNOSTIC DATA USED TO CONTROL SYN2 M TO CHK ECC 32, 16, 8, 4, 2, 1, PAR TO BE USED AS SPECIFIED BY THE DIAGNOSTIC SUBFUNCTION SPECIFIED IN <25:27>

<25:27> SPECIFIES ONE OF EIGHT SUBFUNCTIONS PERFORMED BY A DIAGNOSTIC FUNCTION CODE 6.

= 0 READ THE ECC REGISTER ON WRP7.

= 1 READ THE SYNDROME BUFFER REGISTER ON THE SYN BOARD.

= 2 SELECT DIAGNOSTIC BITS <07:13> IN PLACE OF MOS BITS <36:42>, FORCE 0S ON <00:35>, RUN A CORRECTION PASS, AND RETURN <00:35>.

<25:27> CONT

= 3 NOT USED

= 4 WRITE THE ECC COMPLEMENT REGISTER IF 15 = 1, THEN READ IT BACK.

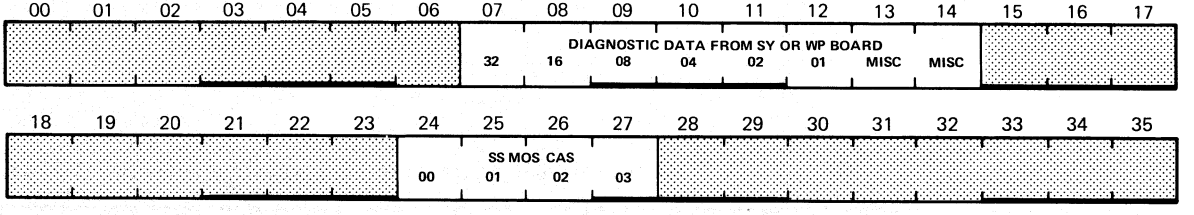
= 5 WRITE THE ECC COMPLEMENT REGISTER, THEN ENABLE IT TO BE SENT TO MEMORY IN PLACE OF <36:42> ON THE NEXT WRITE CYCLE.

= 6 READ THE OUTPUT OF THE <36:42> MIXER.

= 7 ENABLE LATCHING OF <36:42> MIXER AFTER NEXT WRITE.

MR-2175

SBDIAG06
(E+1)



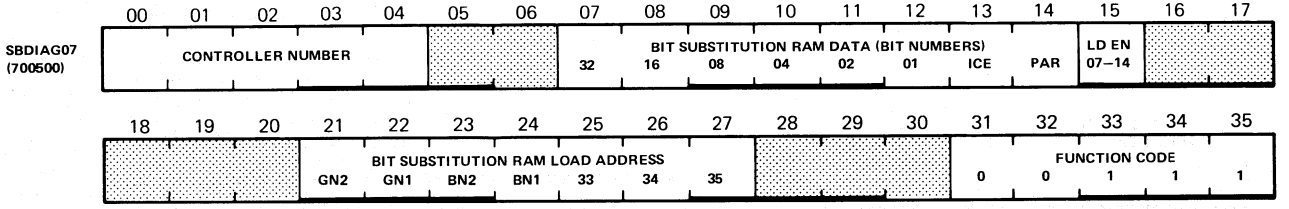
NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 08).

<07:14> REFER TO FUNCT 06 E <07:14>

<24:27> A 4-BIT FIELD THAT DISPLAYS THE STATE OF THE COLUMN ADDRESS STROBE (CAS) SIGNALS ADT5 MOS CAS 0–3.

MR-2176

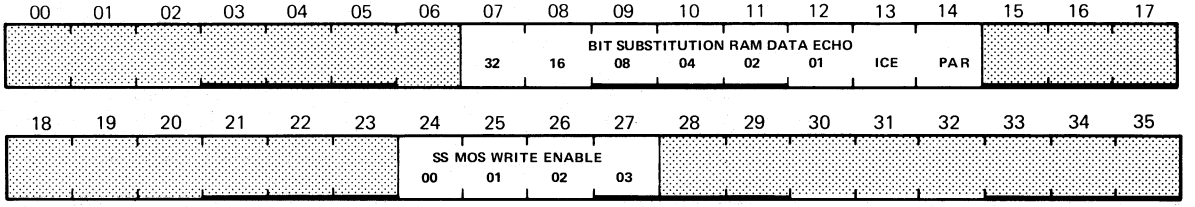
BLKO PI (SBus Diagnostic Function Code 07) MF/MG20



NOTE: "ICE" MEANS IGNORE CORRECTABLE ERROR (I.E., DON'T SET CORR ERR FLAG).

MR-2177

SBDIAG07
(E+1)



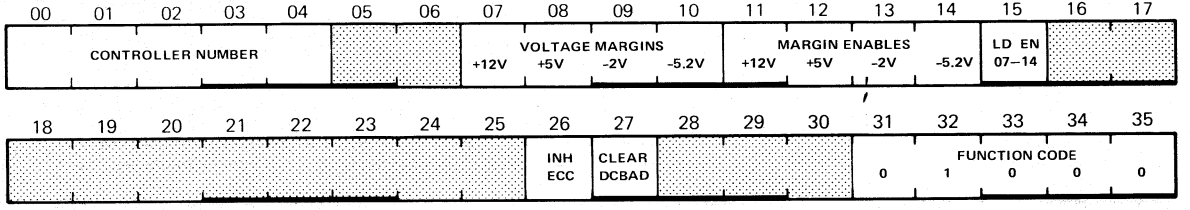
NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 07).
"ICE" MEANS IGNORE CORRECTABLE ERROR (I.E., DON'T SET CORR ERR FLAG).

MR-2178

PI

BLKO PI, (SBus Diagnostic Function Code 10) MF/MG20

SBDIAG10 (700500)

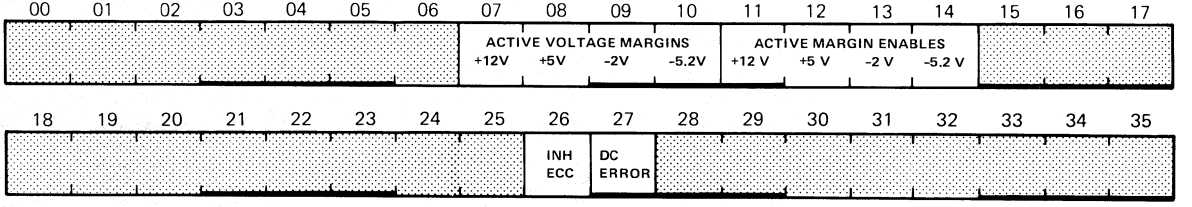


NOTE: MORE THAN ONE VOLTAGE MARGIN MAY BE SET CONCURRENTLY.

07	0 = 11.40, 1 = 12.60	09	0 = -1.90, 1 = 2.10
08	0 = 4.75, 1 = 5.25	10	0 = -4.94, 1 -5.46

MR-2179

SBDIAG10
(E+1)

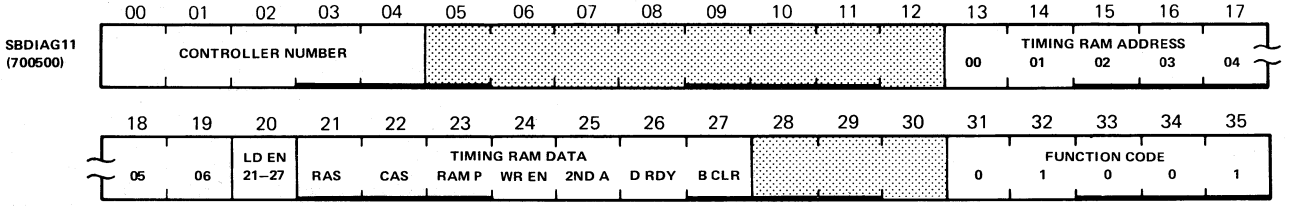


NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 10).

<07:10> REFER TO FUNCT 10 (E) FOR MARGINS

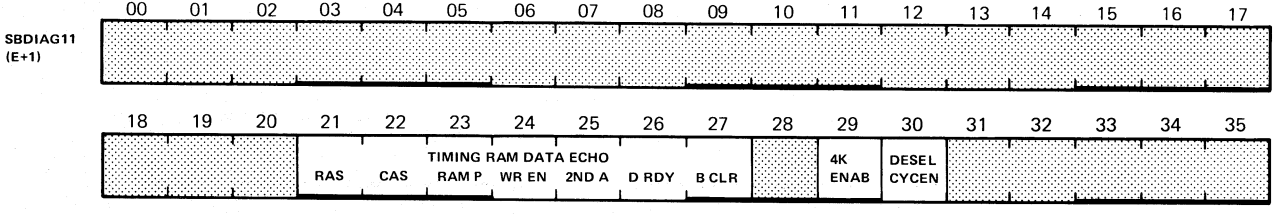
MR-2180

BLKO PI (SBus Diagnostic Function Code 11) MF/MG20



21	ROW ADDRESS STROBE
22	COLUMN ADDRESS STROBE
23	RAM PARITY
24	WRITE ENABLE
25	ADDRESS 2ND HALF
26	DATA READY
27	RAM BUSY CLEAR

MR-2181

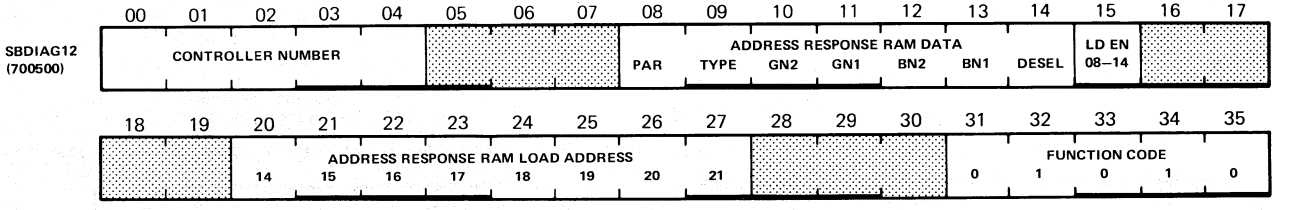


NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 11).

<21:27>	REFER TO FUNCT 11 (E) BITS <21:27>	30	DESELECT CYCLE ENABLE
29	SPECIFY MOS CHIP SIZE		

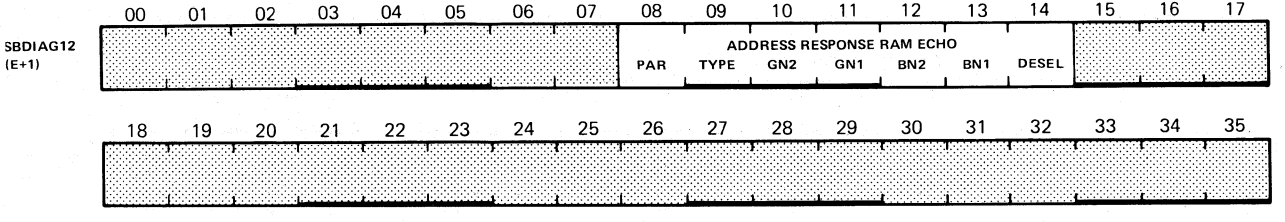
MR-2182

BLKO PI, (SBus Diagnostic Function Code 12)



14 1 = BOX DESELECTED ON A 1

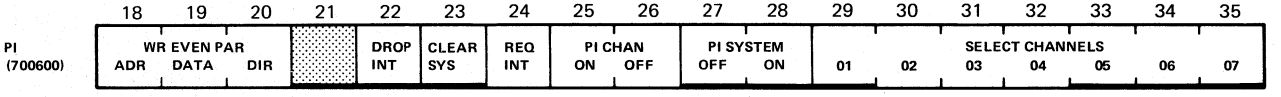
MR-2183



NOTE: E+1 IS THE WORD RETURNED FROM MEMORY AS A RESULT OF BLKO PI, (FUNCT 12).

MR-2184

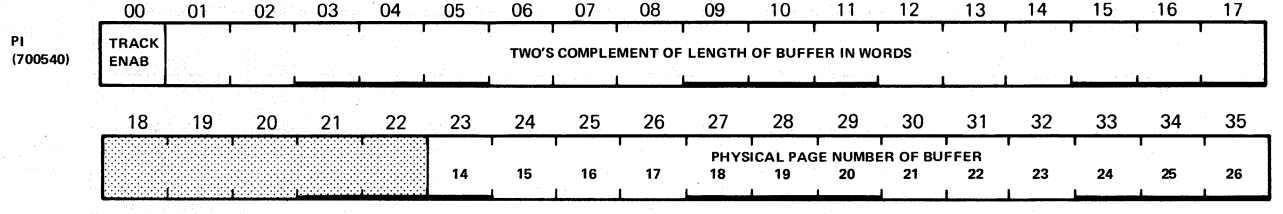
CONO PI,



22 DROP INTERRUPT
23 CLEAR PI SYSTEM
24 REQUEST INTERRUPT

MR-2154

DATAO PI,

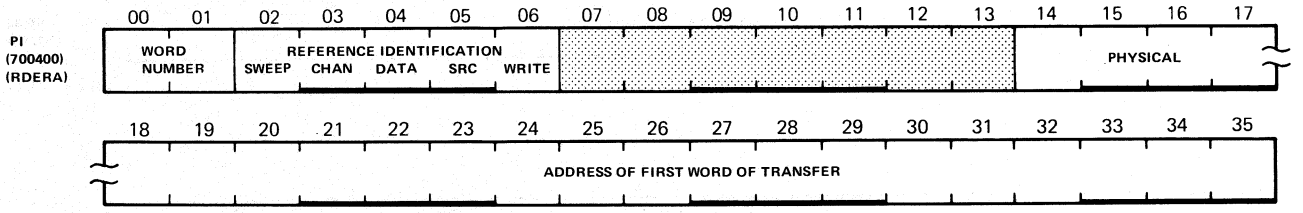


NOTE: TRACKS ONLY

00 ENABLE MICROCODE TRACKING

MR-2156

BLKI PI,



02 REF MADE FOR CACHE SWEEP
03 REF MADE FOR CHANNEL XFER
04 DATA
05 SOURCE
06 WRITE

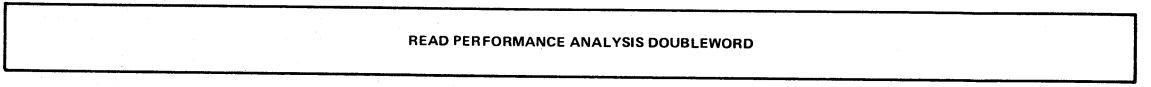
BIT <04:06> COMBINATIONS

04	05	06 (WRITE = 0)	06 (WRITE = 1)
0	0	MEMORY (RD OR RPW)	CHAN STORE STATUS
0	1		CHAN STORE DATA
1	0		EBOX STORE FROM AR
1	1	READ FROM CACHE (PAGE REFILL OR CHAN READ)	CACHE WRITEBACK

MR-2162

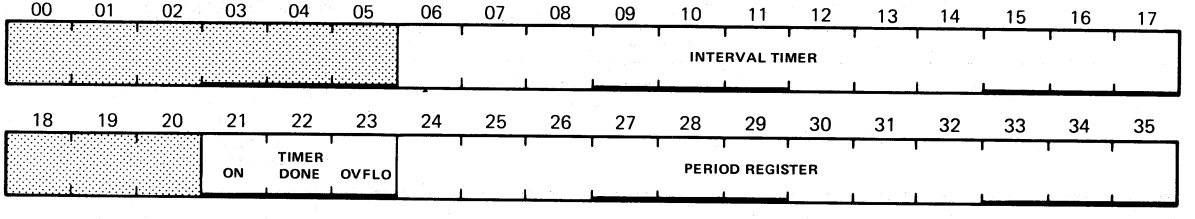
BLKI TIM,

RDPERF
(702000)



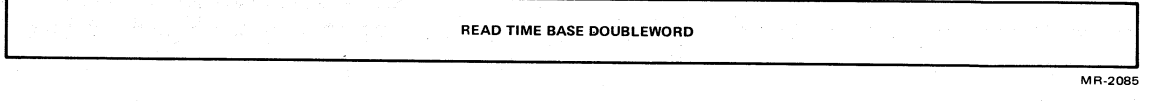
CONI TIM (TOPS-10 TAG: TIMSTS)

702240



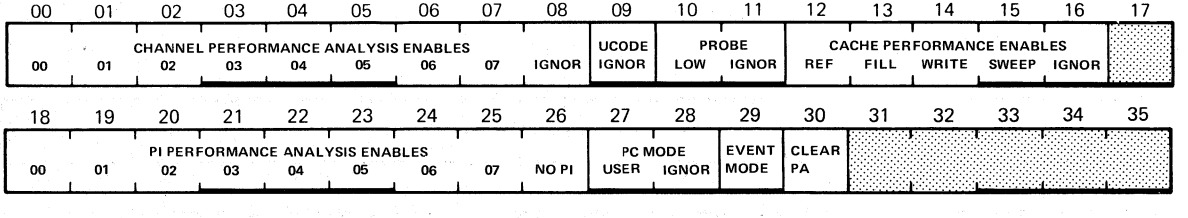
DATAI TIM,

RDTIM
(702040)



BLKO TIM,

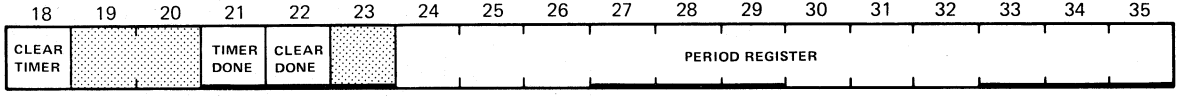
WRPAE
(702100)



MR-2087

CONO TIM

702200

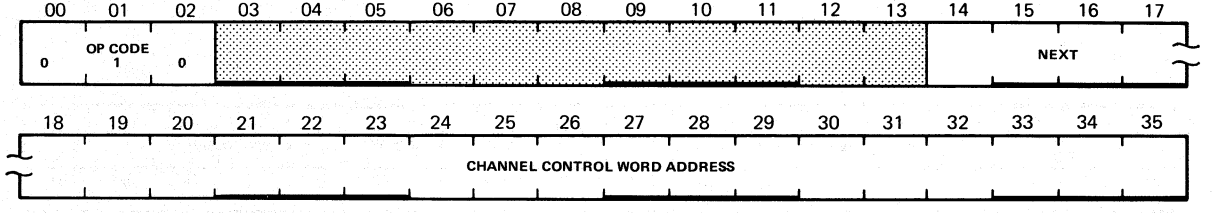


MR-2083

CHANNEL COMMAND CODES

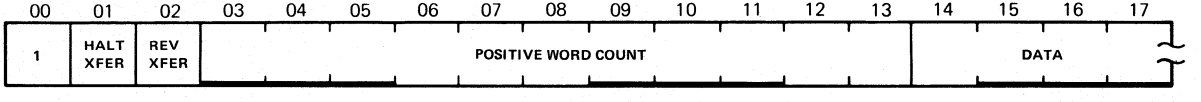
Code	Operation	Code	Operation
000	HALT	100	FORWARD DATA TRANSFER (DO NOT HALT)
001	NOT USED	101	REVERSE DATA TRANSFER (DO NOT HALT)
010	JUMP	110	FORWARD DATA TRANSFER (HALT)
011	NOT USED	111	REVERSE DATA TRANSFER (HALT)

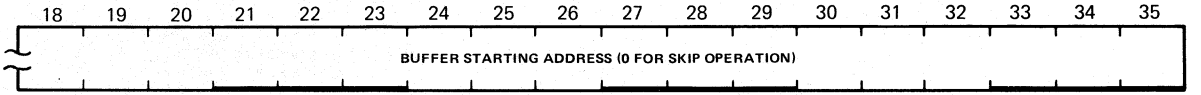
CCW JUMP



MR-2186

CCW DATA TRANSFER





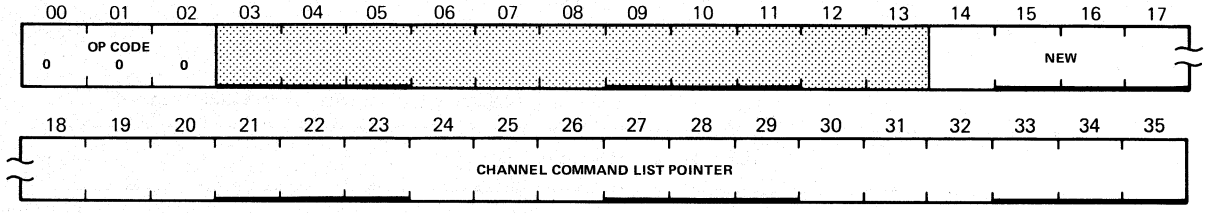
NOTE: WORD COUNT FIELD = POSITIVE WORD COUNT STORED IN CHAN AND DECREMENTED, IF BIT 1 = 1 HALT WHEN WC = 0.
ADDRESS = 22 BIT PHYSICAL ADDRESS:

IF = 0; SKIP
IF DEVICE READ; DON'T MOVE DATA TO MEMORY
IF DEVICE WRITE; CHANNEL SUPPLIES FILL DATA FROM EXEC PROCESS TABLE LOCATIONS 60–63 TO WRITE REMAINDER OF DRIVES DATA BLOCK.

01 HALT AFTER LAST TRANSFER 02 REVERSE DATA TRANSFER

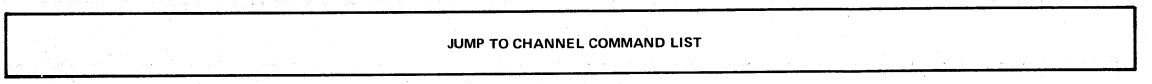
MR-2187

CCW HALT



MR-2185

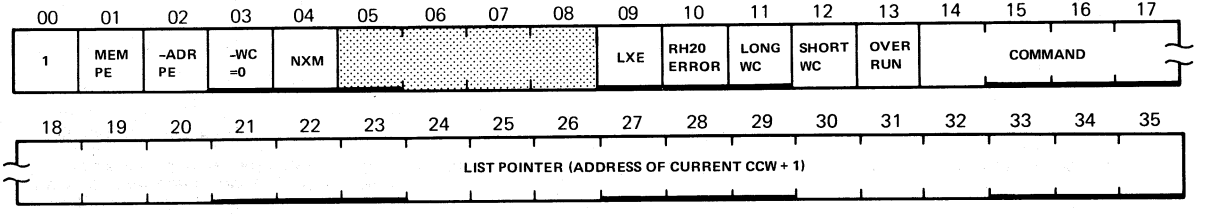
WORD 0 JUMP



NOTE: EXECUTED AS A RESULT OF RH20 ASSERTING CBUS RESET.

MR-2188

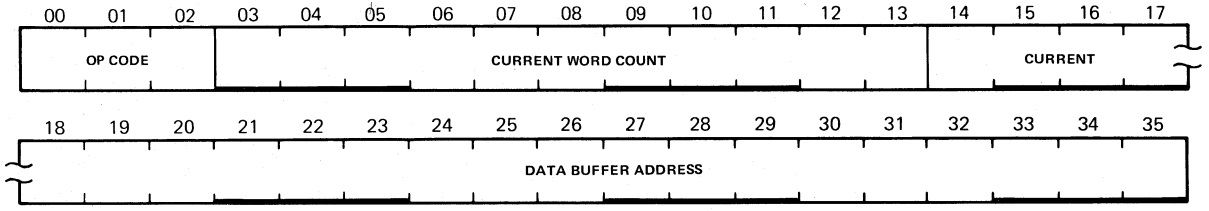
WORD 1 STATUS



01	MEMORY PARITY ERROR
02	NOT ADDRESS PARITY ERROR
03	CHAN WORD COUNT DID NOT = 0 WHEN CHAN DID STORE TO EPT
04	CHAN REF NON EXIST MEM
09	ERROR DETECTED AFTER RH20 TERM XFER, CHAN ABORTS NEXT XFER
10	RH20 TRIED TO START CHAN WHEN CHAN WAS NOT READY
11	RH20 COMP XFER, BUT WORD COUNT IN CCW NOT REACHED
12	CHAN XFERRED DATA SPEC BY CCW, BUT RH20 STILL HAS DATA
13	IF DEV READ, RH20 SENT DATA BUT CHAN BUFF WERE FULL IF DEV WRITE, RH20 REQ DATA BUT CHAN BUFF WERE EMPTY

MR-2189

WORD 2 STATUS



<00:01> CURRENT FUNCTION CODE IN CCW
00 = HALT
01 = NOT IMPLEMENTED
02 = JUMP
03 = NOT IMPLEMENTED
04 = FWD DATA XFER
05 = REV DATA XFER
06 = FWD DATA XFER (HALT LAST XFER)
07 = REV DATA XFER (HALT LAST XFER)

<03:13> NORMALLY 0 AT END OF TRANSFER

<14:35> ADDRESS OF LAST DATA TRANSFERRED TO/FROM MEMORY

MR-2190

WORD 3 STATUS

NOTE: WORD 3 OF THE CHANNEL LOGOUT AREA IS NOT CURRENTLY USED BUT THE PROGRAM MAY USE IT AS THE VECTOR INTERRUPT ADDRESS FOR THE ASSOCIATED CHANNEL.

MR-2191

RH/DISK Function Codes

Nondata Transfer Codes			Data Transfer Codes		
Code	Fixed Head	Moving Head	Code	Fixed Head	Moving Head
01	NO-OP	NO-OP	51*	WR CK DATA	WR CK DATA
03		UNLOAD	53*		WR CK HDR/DATA
05		SEEK	61	WR DATA	WR DATA
07		RECAL	63		WR HRD/DATA
11	DRIVE CLEAR	DRIVE CLEAR	71	RD DATA	RD DATA
13		RELEASE	73		RD HDR/DATA
15		OFFSET			
17		RET TO C.L.			
21	RD-IN PRESET	RD-IN PRESET			
23		PACK ACK			
31	SEARCH	SEARCH			

*Implemented in RH11 controllers only.

RH/TAPE Function Codes

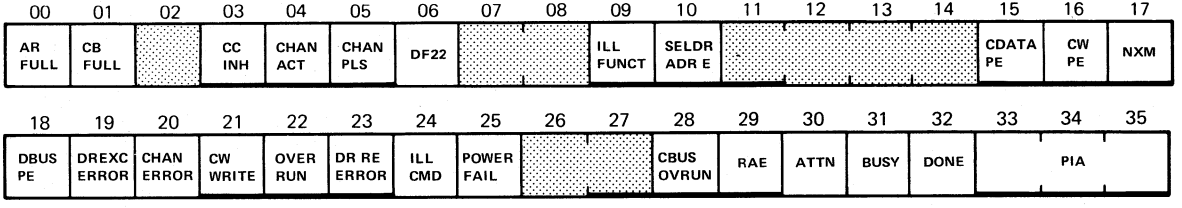
Nondata Transfer Codes		Data Transfer Codes	
Code	Magnetic Tape	Code	Magnetic Tape
01	NO-OP	51*	WR CHECK FORWARD
03	REWIND - OFF LINE	57*	WR CHECK REVERSE
07	REWIND	61	WR FORWARD
11	DRIVE CLEAR	71	RD FORWARD
21	RD-IN PRESET	77	RD REVERSE
25	ERASE		
27	WR FILE MARK		
31	SPACE FORWARD		
33	BACKSPACE		

*Implemented in RH11 controllers only.

NOTES

CONI RHn

(7XX240)



00	ASSEMBLY REGISTER FULL
01	CHANNEL BUFFER FULL
03	CHANNEL CONTROL INHIBIT
04	CHANNEL CONTROL CHANNEL ACTIVE
05	CHANNEL CONTROL CHANNEL PULSE
06	CHANNEL IS IN 22 BIT ADDRESS MODE
09	ILLEGAL FUNCTION CODE
10	SELECTED DRIVE REGISTER ADDRESS ERROR
15	CHANNEL DATA PARITY ERROR
16	CONTROL WORD PARITY ERROR
17	NONEXISTENT MEMORY
18	DATA BUS PARITY ERROR
19	EXCEPTION ERROR
20	CHANNEL ERROR
21	CONTROL WORD WRITTEN
22	DATA CHANNEL OVERRUN
23	DRIVE RESPONSE ERROR
24	ILLEGAL COMMAND
28	CONTROL BUS OVERRUN
29	REGISTER ACCESS ERROR
30	ATTENTION

MR-2198

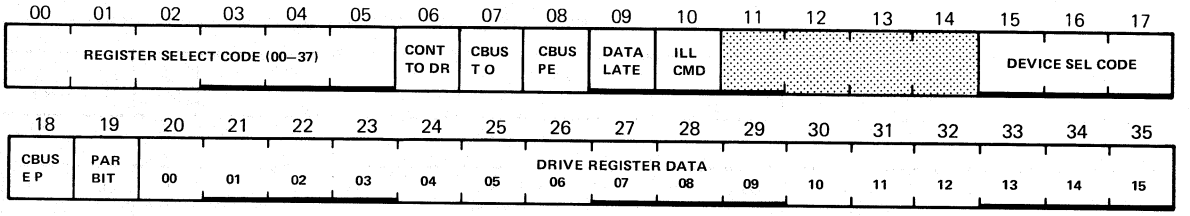
RH10 Register Addresses

Reg Adr	R/W	Name
40	R W	CR - Control Register
44	R W	IA - Interrupt Address
50	R W	DB - Data Buffer
54	R W	AE = Access Error

Reg Adr	R/W	Name

DIB — Drive Interface Buffer

DATAI RHn (7XX040)

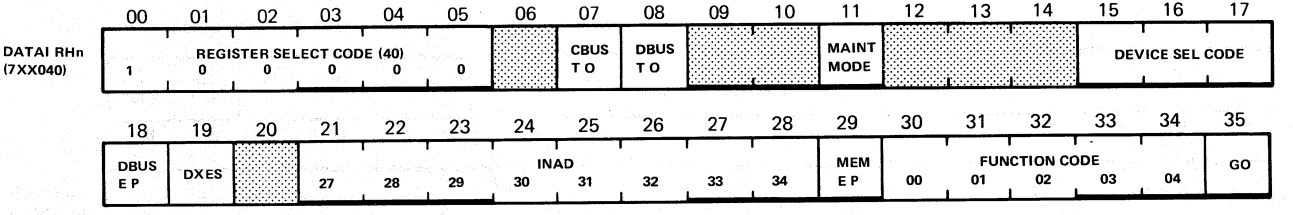


NOTE: REFER TO DATAO DIB FOR A DEFINITION OF BITS <00:05>, 06, <15:17> AND 18.

07 CONTROL BUS TIME OUT
08 CONTROL BUS PARITY ERROR
10 ILLEGAL COMMAND

MR-2200

CR — Control Register



NOTE: REFER TO DATAO CR FOR A DEFINITION OF BITS <00:05>, 15, 18, 19, AND 29.

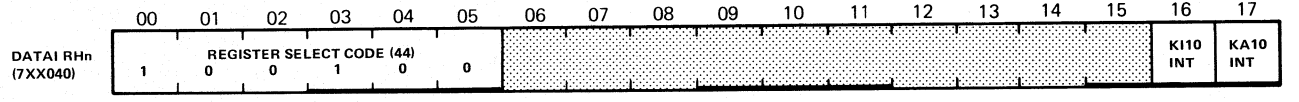
Refer to the function code tables which precede the RH10 I/O bit maps.

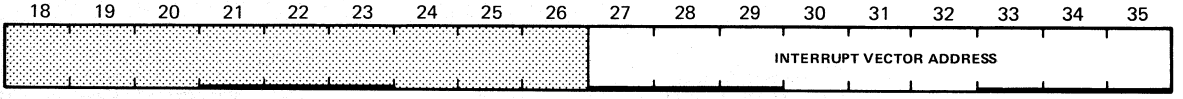
07 CONTROL BUS TIME OUT

08 DATA BUS TIME OUT

MR-2202

IA — Interrupt Address





NOTE: REFER TO DATAO CR FOR A DEFINITION OF BITS <00:05>.

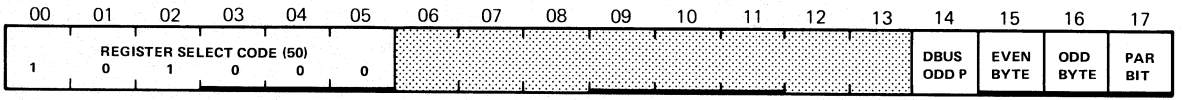
16 KI10 INTERRUPT BIT

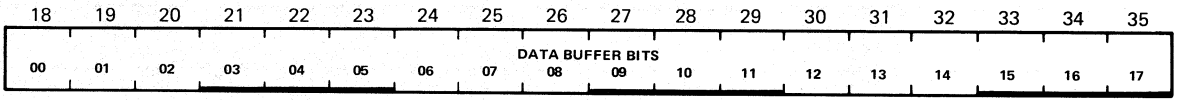
17 KA10 INTERRUPT BIT

MR-2204

DB – Data Buffer

DATAI RHn (7XX040)





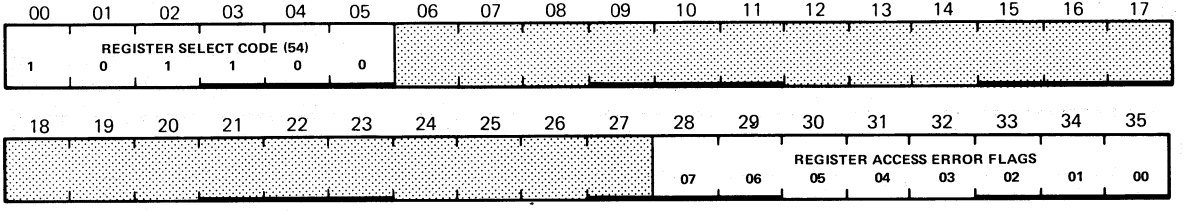
NOTE: REFER TO DATAO CR FOR A DEFINITION OF BITS <00:05>.

14 DATA BUS ODD PARITY

MR-2206

AE — Access Error

DATAI RHn (7XX040)

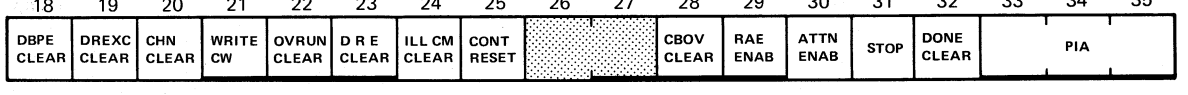


NOTE: REFER TO DATAO CR FOR A DEFINITION OF BITS <00:05>.

MR-2208

CONO RHn

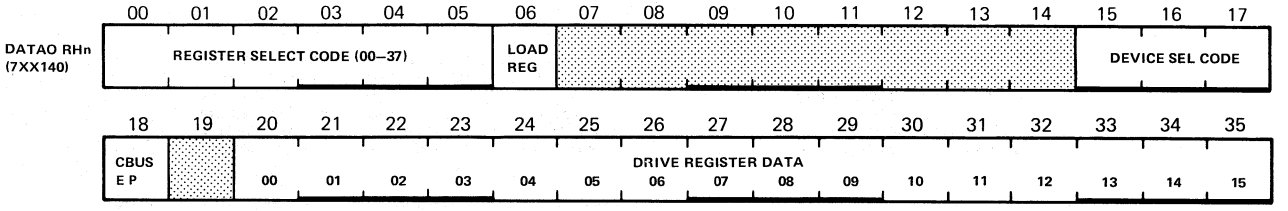
(7XX200)



18	DATA BUS PARITY ERROR CLEAR
19	CLEAR DRIVE EXCEPTION ERROR
20	CHANNEL ERROR CLEAR
21	WRITE CONTROL WORD
22	OVERRUN CLEAR
23	DRIVE RESPONSE ERROR CLEAR
24	ILLEGAL COMMAND CLEAR
25	CONTROLLER RESET
28	CONTROL BUS OVERRUN CLEAR
29	REGISTER ACCESS ERROR ENABLE
30	ATTENTION ENABLE

MR-2197

DIB – Drive Interface Buffer



<00:05> SELECTS ONE OF 32 DRIVE REGISTERS FOR INPUT OR OUTPUT DEPENDING ON BIT 6.

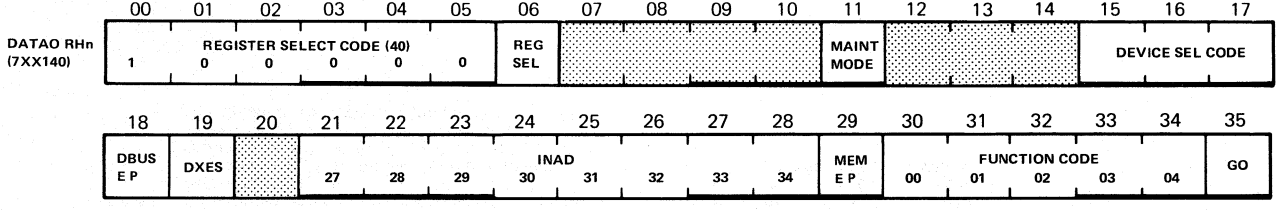
06 IF = 0 DATA (FROM THE DRIVE REGISTER AND DRIVE SPECIFIED BY BITS <00:05> AND <15:17>) WILL BE TRANSFERRED TO THE RH. IF = 1 DATA WILL BE TRANSFERRED TO THE DRIVE AND REGISTER SPECIFIED

<15:17> DEVICE SELECT CODE SPECIFIES WHICH DEVICE (0–7) IS TO BE USED IN THE OPERATION.

18 CONTROL BUS EVEN PARITY

MR-2199

CR – Control Register



NOTE: Refer to the function code tables which precede the RH10 I/O bit maps.

<00:05> REGISTER SELECT CODE – SPECIFIES WHICH REGISTER IS TO BE LOADED IF BIT 06 IS SET. THIS APPLIES TO REGISTER ADDRESS 40–77 ONLY. REFER TO DIB REGISTER FOR ADDRESS 00–37

06 LOAD REGISTER – IF = 0 LOAD CONTROL REGISTER. IF = 1 LOAD THE REGISTER SPECIFIED BY BIT <00:05>

<15:17> DEVICE SELECT CODE – SPECIFIES WHICH DEVICE (0–7) IS TO BE USED IN THE OPERATION

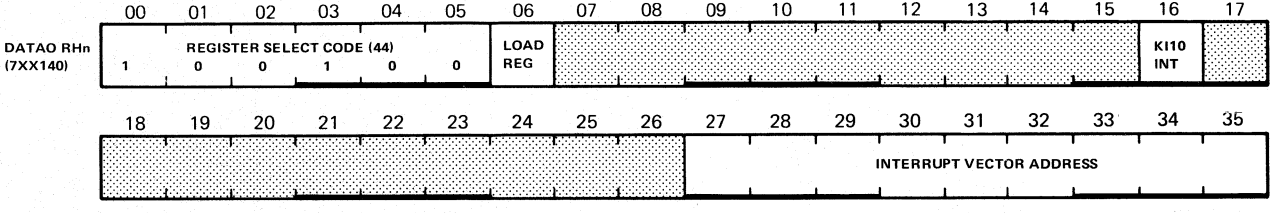
18 DATA BUS EVEN PARITY

19 DISABLE TRANSFER ERROR STOP

29 WRITE EVEN MEMORY PARITY

MR-2201

IA – Interrupt Address

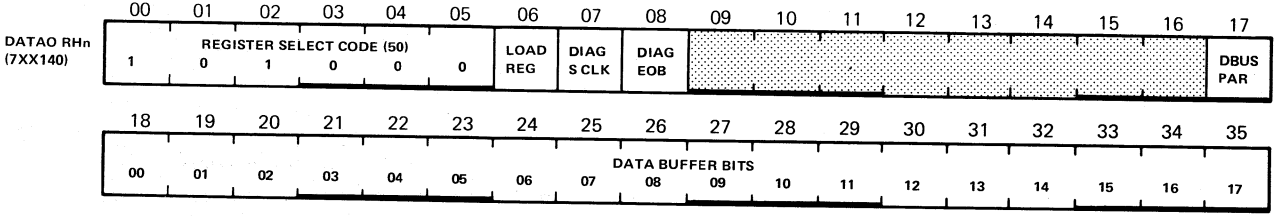


NOTE: REFER TO DATAO CR FOR A DEFINITION OF BITS <00:05> AND 06.

16 KI10 INTERRUPT ENABLE

MR-2203

DB – Data Buffer

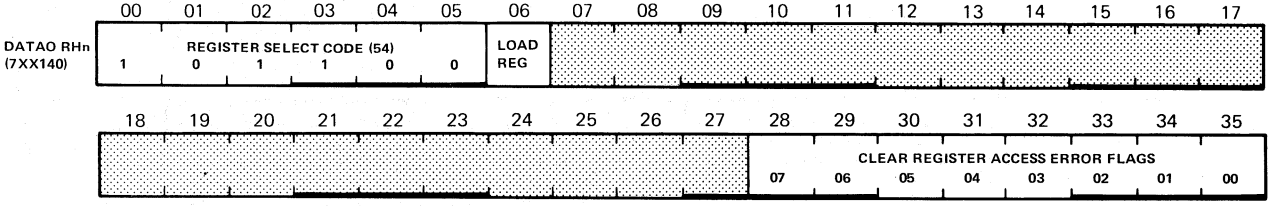


NOTE: REFER TO DATAO CR FOR A DEFINITION OF BITS <00:05> AND 06.

07 DIAGNOSTIC SYNC CLOCK
08 DIAGNOSTIC END OF BLOCK
17 DATA BUS PARITY

MR-2205

AE – Access Error



NOTE: REFER TO DATAO CR FOR A DEFINITION OF BITS <00:05> AND 06.

MR-2207

RH11 — RPBA — Bus Address Register

(776704)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BUS ADDRESS															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

NOTE: ALL BITS READ/WRITE

MR-2215

RH11 — RPCS2 — Control and Status Register 2

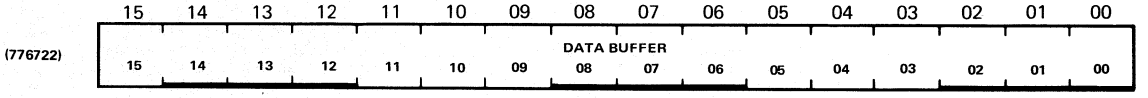
(776710)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA LATE	WR CK ERROR	UBUS PE	NON-X DRIVE	NXM	PROG ERROR	MISS XFER	MBUS D PE	OUT READY	IN READY	CONT CLEAR	PAR TEST	BAI INH	UNIT SEL 02	UNIT SEL 01	UNIT SEL 00
R	R	R/W	R	R	R	R/W	R	R	R	W	R/W	R/W	R/W	R/W	R/W

15	DATA LATE
14	WRITE CHECK
13	UNIBUS PARITY ERROR
12	NON-EXISTENT DRIVE
11	NON-EXISTENT MEMORY
10	PROGRAM ERROR — RH BUSY
09	MISSED TRANSFER
08	MASSBUS DATA PARITY ERROR
07	OUTPUT READY
06	INPUT READY
05	CONTROLLER CLEAR
04	PARITY TEST
03	BUS ADDRESS INCREMENT INHIBIT
<02:00>	UNIT SELECT

MR-2216

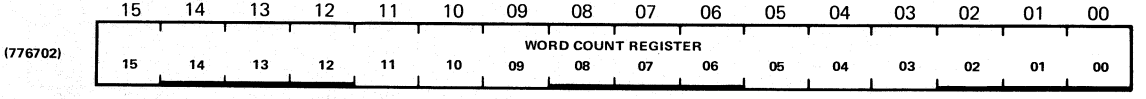
RH11 — RPDB — Data Buffer Register



NOTE: ALL BITS READ/WRITE

MR-2217

RH11 — RPWC — Word Count Register

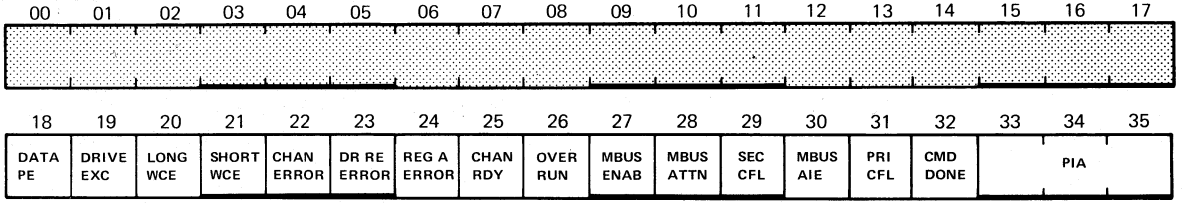


NOTE: ALL BITS READ/WRITE

MR-2218

CONI RHn

(7XX 240)



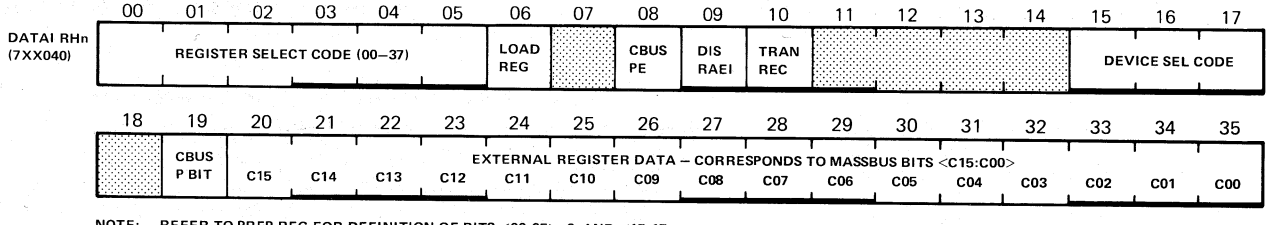
NOTE: BITS 24, 28 AND 32 WILL CAUSE AN INTERRUPT.

18	DATA BUS PARITY ERROR
19	DRIVE EXCEPTION ERROR
20	LONG WORD COUNT ERROR
21	SHORT WORD COUNT ERROR
22	CHANNEL ERROR
23	DRIVE RESPONSE ERROR
24	REGISTER ACCESS ERROR (CBTO OR CBPE)
25	CHANNEL READY TO BEGIN TRANSFER
26	DATA OVERRUN ERROR
27	MASSBUS ENABLE
28	MASSBUS ATTENTION
29	SECONDARY COMMAND FILE LOADED
30	MASSBUS ATTENTION INTERRUPT ENABLED
31	PRIMARY COMMAND FILE LOADED
32	COMMAND DONE
<33:35>	PRIORITY INTERRUPT CHANNEL

MR-2046

Reg	Adr	R/W	Name
--		R W	PREP - Preparation Register (not addressed directly)
7	0	R W	SBAR - Secondary Block Address Register
7	1	R W	STCR - Secondary Transfer Control Register
7	2	R -	PBAR - Primary Block Address Register
7	3	R -	PTCR - Primary Transfer Control Register
7	4	R W	IVIR - Interrupt Vector Index Register
7	5	R -	RR - Read Register (Diagnostic Use)
7	6	- W	WR - Write Register (Diagnostic Use)
7	7	- W	DCR - Diagnostic Control Register (Diagnostic Use)

EXT — External Registers (00–37)

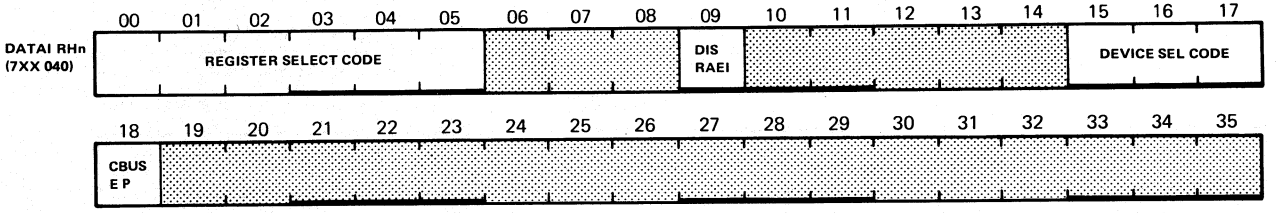


NOTE: REFER TO PREP REG FOR DEFINITION OF BITS <00:05>, 6, AND <15:17>.

08 CONTROL BUS PARITY ERROR
09 DISABLE REG ACCESS ERROR, INTERRUPTS AND SUBSEQUENT REG WRITES
10 TRANSFER RECEIVED (DEVICE RESPONDED)
19 CONTROL BUS PARITY BIT

MR-2050

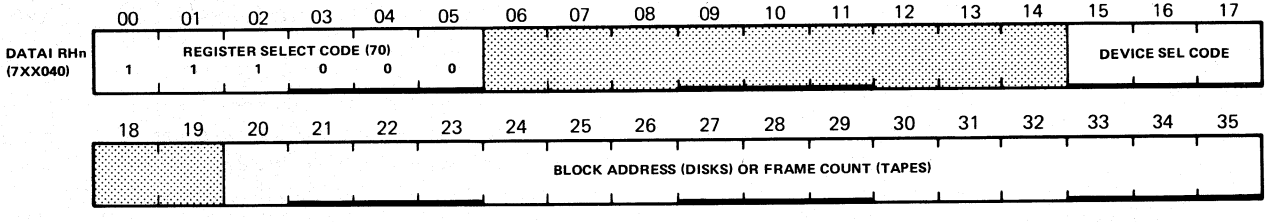
PREP – Preparation Register (Not Addressed Directly)



NOTE: REFER TO DATAO PREP REG FOR DEFINITIONS OF BITS.

MR-2048

SBAR – Secondary Block Address Register (70)

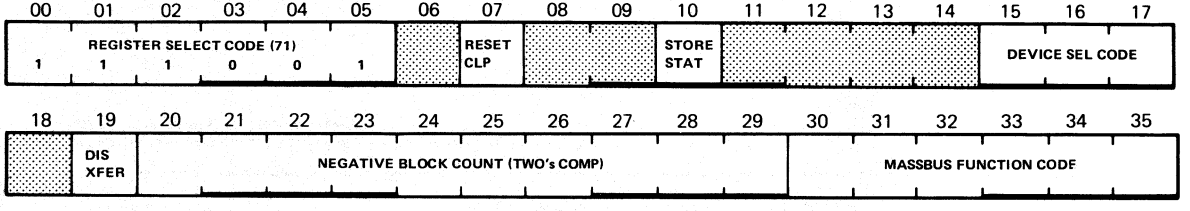


NOTE: REFER TO PREP REG FOR DEFINITIONS OF <00:05>, 06 AND <15:17>.

MR-2052

STCR — Secondary Transfer Control Register (71)

DATAI RHn (7XX040)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.

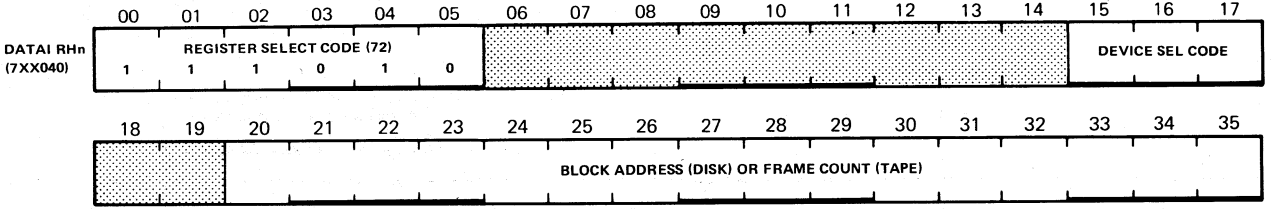
07 RESET COMMAND LIST POINTER

10 STORE CHANNEL STATUS CONTROL BIT

19 DISABLE TRANSFER ERROR STOP BIT

MR-2054

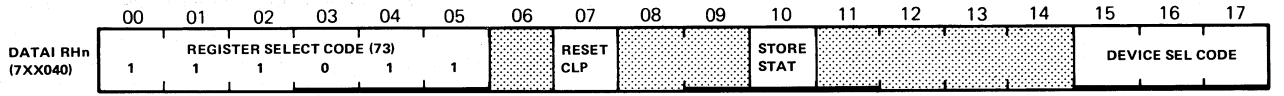
PBAR – Primary Block Address Register (72)

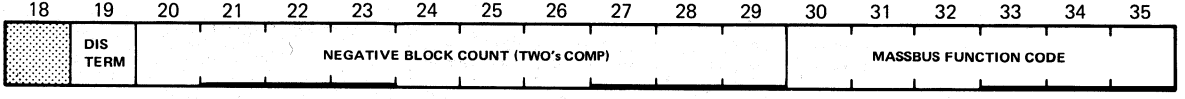


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.
REFER TO SBAR REG FOR DEFINITIONS OF BITS <20:35>.

MR-2055

PTCR – Primary Transfer Control Register (73)

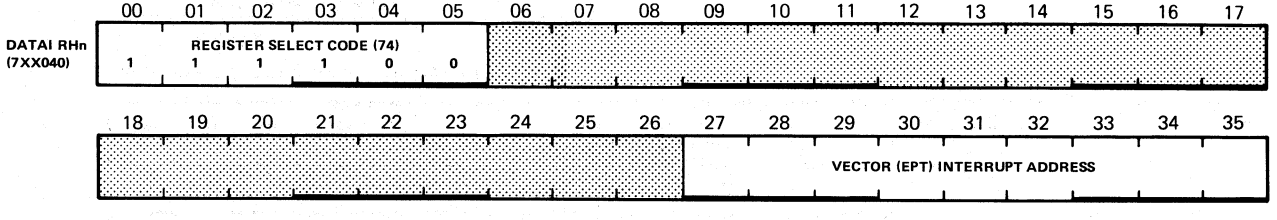




NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.
REFER TO STCR REG FOR DEFINITION OF BITS 07, 10, AND 19.

MR-2056

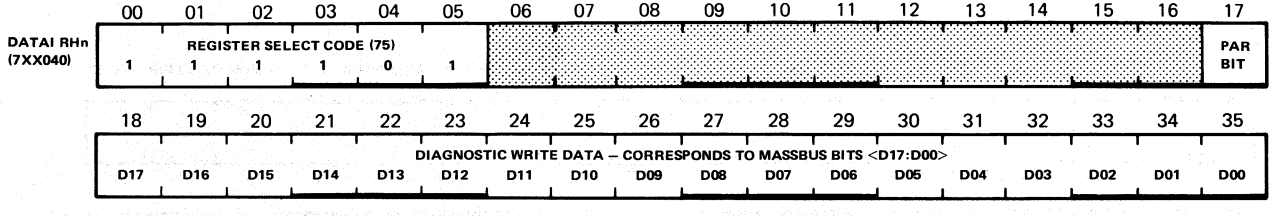
IVIR – Interrupt Vector Index Register (74)



NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

MR-2058

RR – Read Register (75) Diagnostic Use

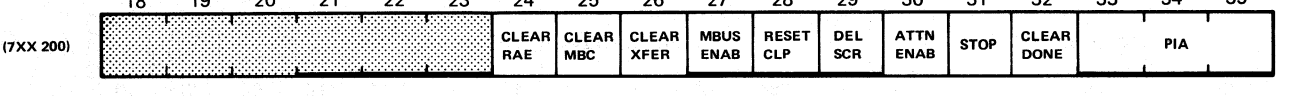


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

17 PARITY BIT
<18:35> WRITE DATA AND PARITY (17) LOOPED BACK VIA MASSBUS XCVRS DURING DIAG WRITE

MR-2059

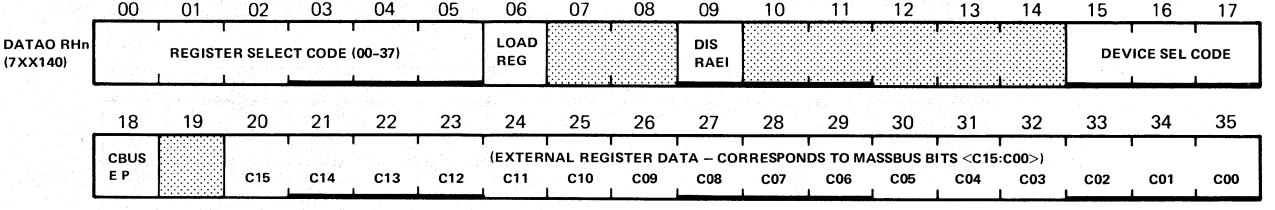
CONO RHn



24	CLEAR REGISTER ACCESS ERROR	29	DELETE SECONDARY CONTROL REGISTER
25	CLEAR MASSBUS CONTROLLER, ZERO IVIR REGISTER	30	ATTENTION INTERRUPT ENABLE
26	CLEAR TRANSFER ERRORS	31	STOP TRANSFER (STATUS BITS NOT CLEARED)
27	MASSBUS ENABLE	<33:35>	PRIORITY INTERRUPT CHANNEL
28	RESET COMMAND LIST POINTER		

MR-2045

EXT – External Registers (00–37)

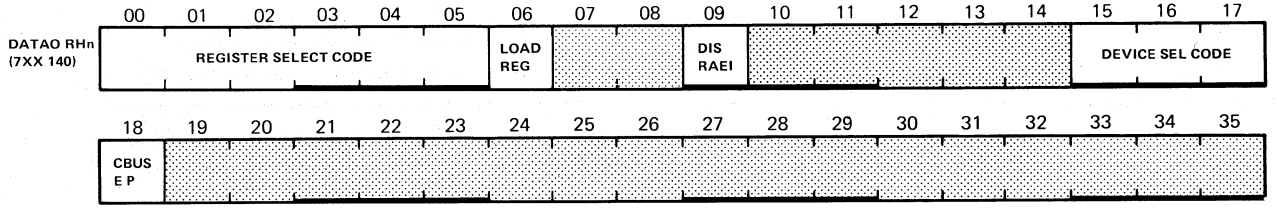


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:18>.

09 DISABLE REG ACCESS ERROR, INTERRUPTS AND SUBSEQUENT REG WRITES.

MR-2049

PREP – Preparation Register (Not Addressed Directly)



NOTE: BITS <00:05>, 06 AND <15:17> HAVE A COMMON DEFINITION FOR MANY RH REGISTERS, TO ELIMINATE REDUNDENCY THEY ARE DESCRIBED ONCE HERE.

<00:05> REGISTER SELECT CODE. SPECIFIES WHICH REGISTER IS TO BE LOADED IF BIT 06 IS SET.

06 LOAD REGISTER. IF 0 LOAD PREP REG. IF 1 LOAD REG SPECIFIED BY BITS <00:05>

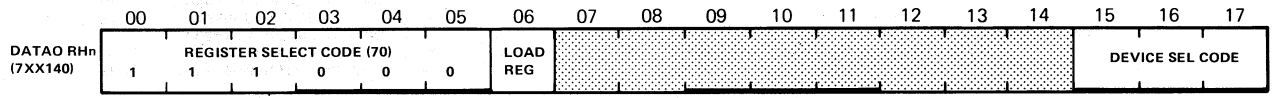
09 DISABLE REG ACCESS ERROR INTERRUPTS AND SUBSEQUENT REG WRITES

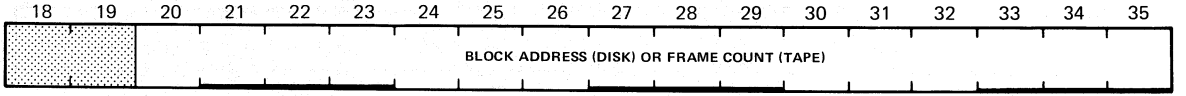
<15:17> DEVICE SELECT CODE. SPECIFIES WHICH DEVICE (0–7) IS TO BE USED IN THE OPERATION.

18 CONTROL BUS EVEN PARITY

MR-2047

SBAR – Secondary Block Address Register (70)



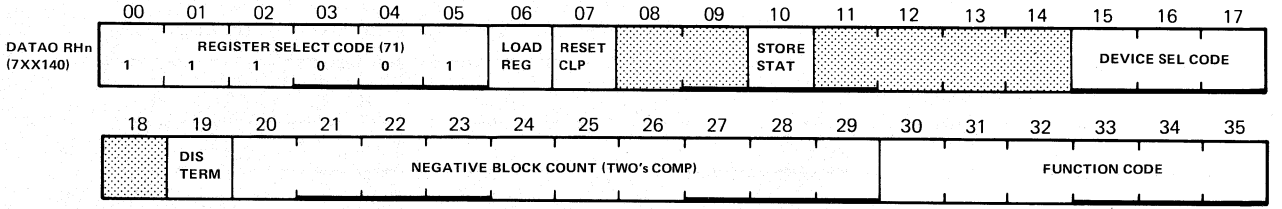


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, <15:17>.

<20:35> TAPE – FRAME COUNT 20 = MSD 35 = LSD
<23:27> DISK – TRACK ADDRESS
<31:35> DISK – SECTOR ADDRESS

MR-2051

STCR – Secondary Transfer Control Register (71)



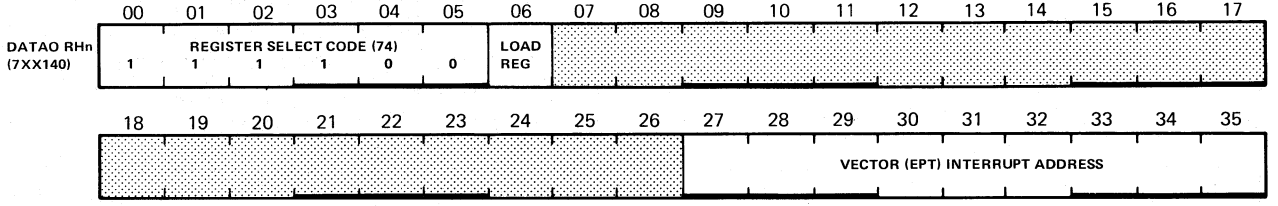
NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05>, 06, AND <15:17>.

Refer to the function code tables which precede the RH10 I/O bit maps.

07 RESET COMMAND LIST POINTER
10 STORE CHANNEL STATUS CONTROL BIT
19 DISABLE TERMINATION OF TRANSFERS DUE TO DATA BUS PARITY ERRORS OR DRIVE EXCEPTION ERRORS.

MR-2053

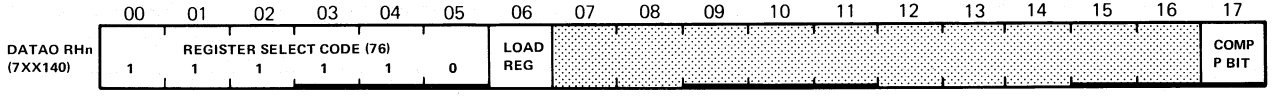
IVIR – Interrupt Vector Index Register (74)

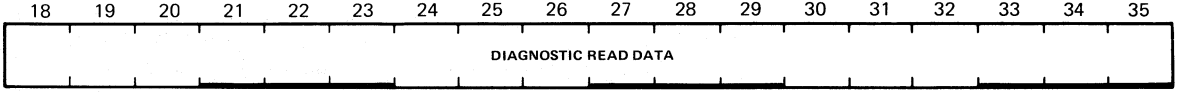


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

MR-2057

WR – Write Register (76) Diagnostic Use



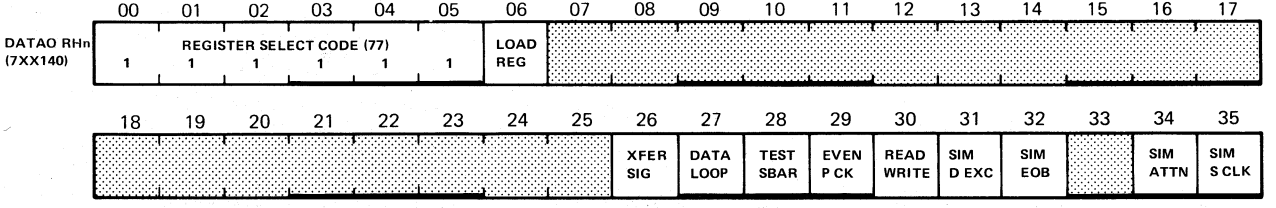


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

17 COMPUTED PARITY BIT (BY PROG) FOR DIAG READ DATA

MR-2060

DCR – Diagnostic Control Register (77) Diagnostic Use

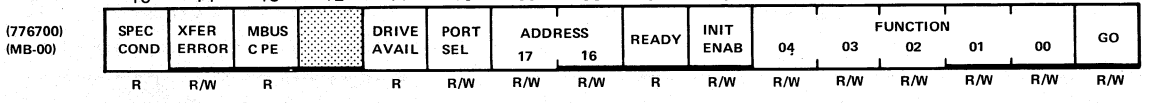


NOTE: REFER TO PREP REG FOR DEFINITIONS OF BITS <00:05> AND 06.

26 TRANSFER SIGNAL (SIMULATED)
27 DATA LOOPBACK (VIA MASSBUS XCVRS)
28 TEST SBAR
29 EVEN PARITY CHECK
30 READ/WRITE-SET ON DIAG READ (LOOPS RD DATA VIA MASSBUS XCVRS)
31 SIMULATES DRIVE EXCEPTION
32 SIMULATES END OF BLOCK
34 SIMULATES ATTENTION
35 SIMULATES SYNC CLOCK SIGNAL

MR-2061

RH11 – RPCS1 – Control and Status Register 1
RH20 – DRCR – Control Register



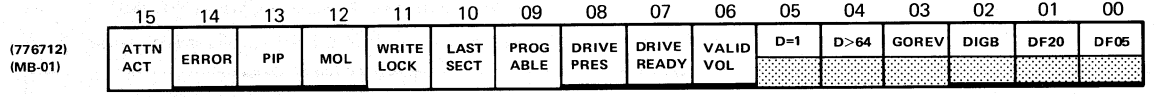
NOTE: SHARED REGISTER BITS <15:13> AND <10:06> ARE IN RH.
REFER TO DCL PRINT RG3 AND RG6.

Refer to the function code tables which precede the RH10 I/O bit maps.

15	SPECIAL CONDITION	10	PORT SELECT
14	TRANSFER ERROR	<09:08>	UNIBUS ADDRESS EXTENSION BITS 17 AND 16
13	MASSBUS CONTROL PARITY ERROR	06	INTERRUPT ENABLE
11	DRIVE AVAILABLE		

MR-2219

RH11 – RPDS – Drive Status
RH20 – DRSR – Status Register



NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT RG6.

15	ATTENTION ACTIVE
13	POSITIONING IN PROGRESS
12	MEDIUM ON LINE
10	LAST SECTOR TRANSFERRED
09	PROGRAMMABLE
08	DRIVE PRESENT
06	VALID VOLUME
05	RP04 – DIFFERENCE EQUALS ONE
04	RP04 – DIFFERENCE LESS THAN 64
03	RP04 – GO REVERSE
02	RP04 – DRIVE TO INNER GUARD BAND
01	RP04 – DRIVE FORWARD 20 INCH/SEC
00	RP04 – DRIVE FORWARD 5 INCH/SEC
<05:00>	RP06 UNUSED

MR-2220

RH11 – RPER1 – Error Register 1
RH20 – DRER1 – Error Register 1

(776714)
(MB-02)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA CHECK	UN SAFE	OPER INC	DR T ERROR	WR LK ERROR	I ADR ERROR	A OV ERROR	H CRC ERROR	H COM ERROR	ECC ERROR	WR CK FAIL	FMT ERROR	PAR ERROR	RMR	ILL REG	ILL FUNC

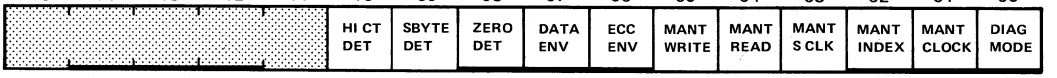
NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT RG0.

13	OPERATION INCOMPLETE
12	DRIVE TIMING ERROR
11	WRITE LOCK ERROR
10	INVALID ADDRESS ERROR
09	ADDRESS OVERFLOW ERROR
08	HEADER CRC ERROR
07	HEADER COMPARE ERROR
06	ECC HARD ERROR
05	WRITE CLOCK FAIL
04	FORMAT ERROR
03	PARITY ERROR
02	REGISTER MODIFICATION REFUSED
01	ILLEGAL REGISTER
00	ILLEGAL FUNCTION

MR-2221

RH11 – RPMR – Maintenance Register
RH20 – DRMR – Maintenance Register

(776724)
(MB-03)



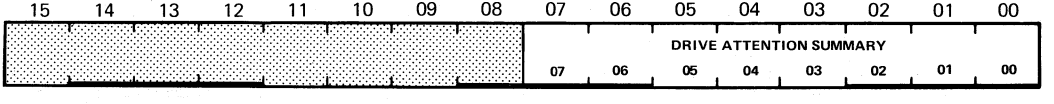
NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT EC1 AND RG3.

10	HIGH COUNT DETECT	06	ECC ENVELOPE
09	SYNC BYTE DETECTED	03	MAINTENANCE SECTOR CLOCK
08	ZERO DETECT	00	DIAGNOSTIC MODE
07	DATA ENVELOPE		

MR-2222

RH11 – RPAS – Attention Summary
RH20 – DRAS – Attention Summary

(776716)
(MB-04)

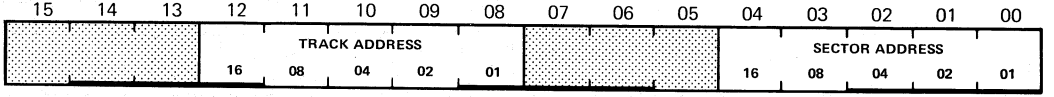


NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT DP.

MR-2223

RH11 – RPDA – Desired Track/Sector Address
RH20 – DRDA – Desired Track/Sector Address

(776706)
(MB-05)

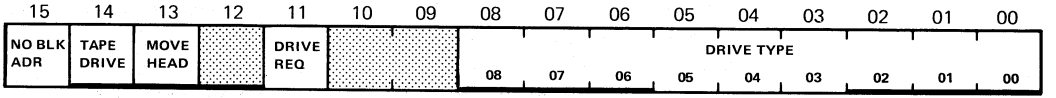


NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT SS3 AND SS6.

MR-2224

RH11 – RPDT – Drive Type
RH20 – DRTR – Type Register

(776726)
(MB-06)

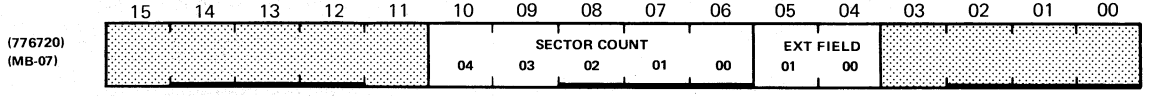


NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC8.

15 NOT BLOCK ADDRESSED
14 TAPE DRIVE
13 MOVING HEAD
11 DRIVE REQUEST REQUIRED

MR-2225

RH11 – RPLA – Look Ahead
RH20 – DRLP

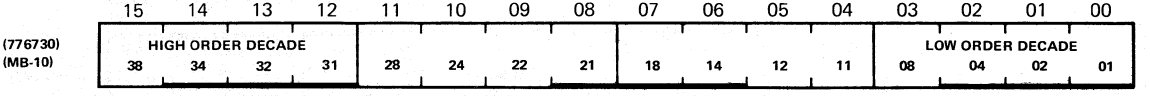


NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT DP6.

<05:04> EXTENSION FIELD
05 04 HEAD LOCATION
0 0 = <20% (IN FIRST 20% OF SECTOR)
0 1 = 20 – 40%
1 0 = 40 – 80%
1 1 = >80% (IN LAST 20% OF SECTOR)

MR-2226

RH11 – RPSN – Serial Number
RH20 – DRSN – Serial Number

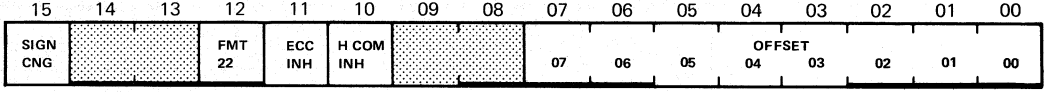


NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC8.

MR-2227

RH11 – DPOF – Offset
RH20 – DROF – Offset

(776732)
(MB-11)



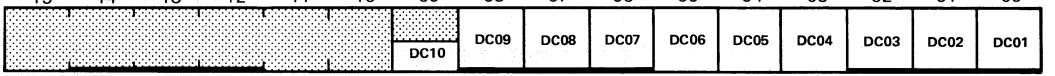
NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT RG1.

15 SIGN CHANGE
12 FORMAT 22 SECTORS
11 ECC INHIBIT
10 HEADER COMPARE INHIBIT

MR-2228

RH11 – RPDC – Desired Cylinder
RH20 – DRDC – Desired Cylinder

(776734)
(MB-12)

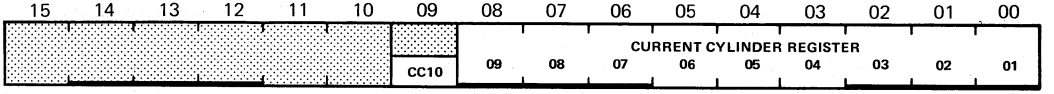


NOTE: ALL BITS READ WRITE.
REFER TO DCL PRINT SS1.

MR-2229

RH11 – RPCC – Current Cylinder Address
RH20 – DRCC – Current Cylinder Address

(776736)
(MB-13)



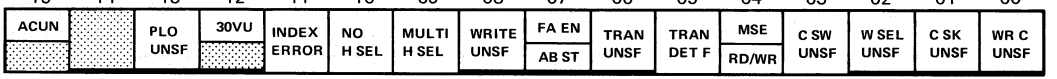
NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT SS1.

09 RP04 – UNUSED
RP06 – CURRENT CYLINDER BIT 10

MR-2230

RH11 – RPER2 – Error Register 2
RH20 – DRER2 – Error Register 2

(776740)
(MB-14)



NOTE: ALL BITS READ/WRITE
REFER TO DCL PRINT EC6.

15	RP04 – AC UNSAFE RP06 – UNUSED	07	RP04 – FAILSAFE ENABLED RP06 – ABNORMAL STOP
13	PHASE LOCKED OSCILLATOR UNSAFE	06	TRANSITION UNSAFE
12	RP04 – 30 VOLTS UNSAFE RP06 – UNUSED	05	TRANSITION DETECTOR FAILURE
11	INDEX ERROR	04	RP04 – MOTOR SEQUENCE ERROR RP06 – READ AND WRITE
10	NO HEAD SELECT	03	CURRENT SWITCH UNSAFE
09	MULTIPLE HEAD SELECT	02	WRITE SELECT UNSAFE
08	WRITE READY UNSAFE	01	CURRENT SINK FAILURE
		00	WRITE CURRENT UNSAFE

MR-2231

RH11 – RPER3 – Error Register 3
RH20 – DRER3 – Error Register 3

(776742)
(MB-15)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OFF CYL	SEEK INC	OPER							AC LOW	DC LOW	35 VF	UNSF		VE US WR OS	PS UN DC UN

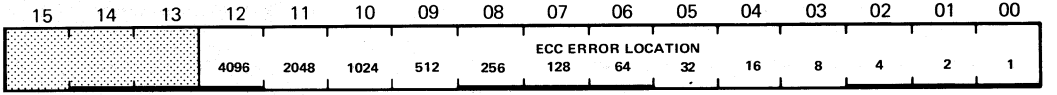
NOTE: ALL BITS READ/WRITE.
REFER TO DCL PRINT EC7.

15	OFF CYLINDER	03	RP04 – ANY UNSAFE EXCEPT READ/WRITE RP06 – UNUSED
14	SEEK INCOMPLETE	01	RP04 – VELOCITY UNSAFE RP06 – WRITE AND OFFSET
13	RP04 – UNUSED RP06 – OPERATOR PLUG ERROR	00	RP04 – PACK SPEED UNSAFE RP06 – DC VOLTAGE UNSAFE
06	AC VOLTAGE UNSAFE		
05	DC VOLTAGE UNSAFE		
04	RP04 – UNUSED RP06 – 35 VOLTS UNSAFE		

MR-2232

RH11 – RPEC1 – ECC Position Register
RH20 – DREC1 – ECC Position Register

(776744)
(MB-16)



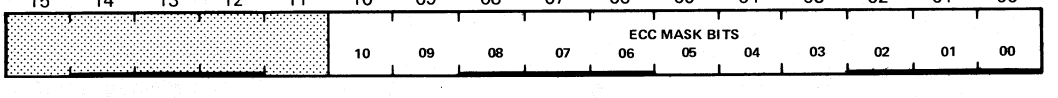
NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC2.

<12:00> BURST LOCATION CODE FOR ECC

MR-2233

RH11 – RPEC2 – ECC Pattern
RH20 – DREC2 – ECC Pattern

(776746)
(MB-17)



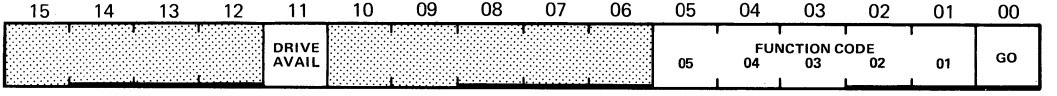
NOTE: ALL BITS READ ONLY.
REFER TO DCL PRINT EC1.

<10:00> ERROR BURST AT COMPLETION OF ECC

MR-2234

NOTES

CS1 — Control Register 1

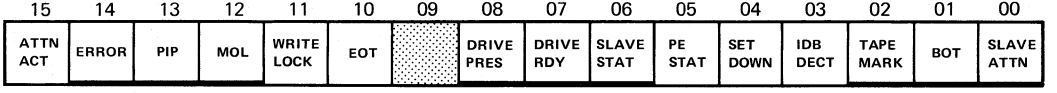


NOTE: Refer to the function code tables which precede the RH10 I/O bit maps.

11 DRIVE AVAILABLE (HARDWIRED)

MR-2072

DS — Status Register



NOTE: ALL BITS READ ONLY.

15	ATTENTION ACTIVE	06	SLAVE STATUS CHANGE
14	COMPOSITE ERROR	05	PHASE ENCODED STATUS
13	POSITIONING IN PROGRESS	04	SETTLE DOWN
12	MEDIUM ON LINE	03	IDENTIFICATION BURST DETECTED
10	END OF TAPE	02	TAPE MARK DETECTED
08	DRIVE PRESENT	01	BEGINNING OF TAPE
07	DRIVE READY	00	SLAVE ATTENTION

MR-2073

ER – Error Register

(MB-02)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CORR / CRC	UN SAFE	OPER INC	DR T ERROR	NXF	CS / ITM	F C ERR	N STD GAP	PFE / LRC	NDE / VPE	DBUS PE	FMT ERROR	CBUS PE	REG MOD	ILL REG	ILL FUNC

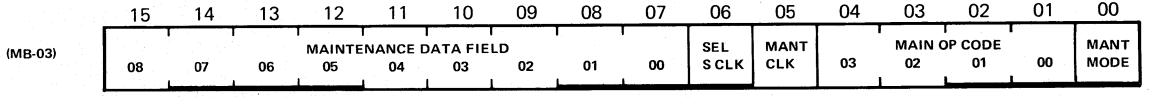
NOTE: ALL BITS READ ONLY

SPLIT BITS PE / NRZI

15 PE – CORRECTABLE DATA ERROR NRZI – CRC DOES NOT MATCH COMPUTED CRCC
14 UNSAFE
13 OPERATION INCOMPLETE
12 DRIVE TIMING ERROR
11 NONEXECUTABLE FUNCTION
10 PE CORRECTABLE SKEW
NRZI – ILLEGAL TAPE MARK
09 FRAME COUNT ERROR
08 NONSTANDARD GAP TAPE CHAR
07 PE – FORMAT ERROR
NRZI – CHECK CHAR ERROR
06 PE – NONCORRECTABLE DATA ERROR
NRZI – VERTICAL PARITY ERROR
05 DATA BUS PARITY ERROR
04 FORMAT ERROR
03 CONTROL BUS PARITY
02 REGISTER MODIFICATION REFUSED
01 ILLEGAL REGISTER
00 ILLEGAL FUNCTION

MR-2074

MR – Maintenance Register

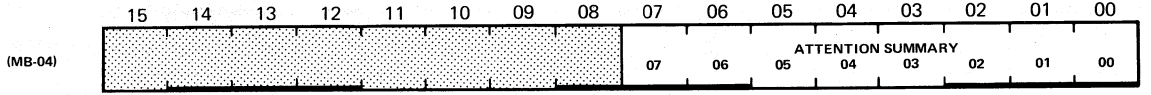


NOTE: ALL BITS READ/WRITE

<15:7>	MAINT DATA FIELD: BUFFER DATA ON WRAP OP, LRC AT END OF NRZI TRANSFERS	05	MAINTENANCE CLOCK
06	SELECTED SLAVE CLOCK: WRT CLOCK SIG GEN BY SEL SLAVE	<4:1>	MAINT OPERATION CODE
		00	MAINT MODE

MR-2075

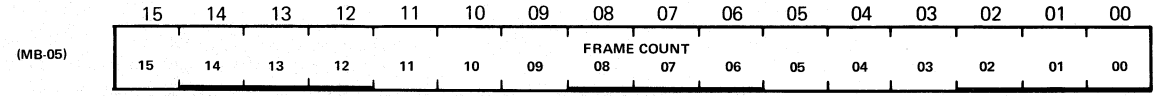
AS – Attention Summary



NOTE: ALL BITS READ/WRITE

MR-2076

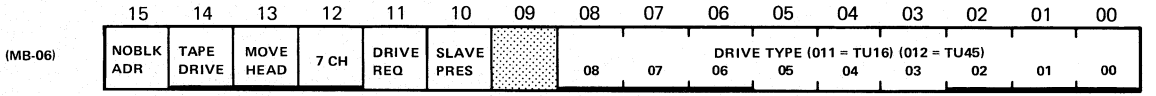
FC — Frame Count



NOTE: ALL BITS: READ/WRITE

MR-2082

DT — Drive Type



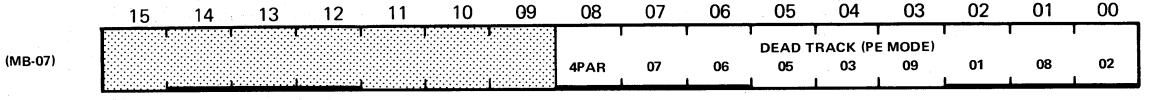
NOTE: ALL BITS READ ONLY
BITS <08:00> HARDWIRED

15 NOT BLOCK ADDRESSED
14 TAPE DRIVE
13 MOVING HEAD UNIT
12 7 CHANNEL UNIT-NEGATED ON 9 CH DRIVE OR POWER LOSS
11 DRIVE REQUEST REQUIRED
10 SLAVE PRESENT

<08:00> DRIVE TYPE
X5X = TM03
X1X = TM02
XX1 = 45 IPS SLAVE
XX2 = 75 IPS
XX4 = 125 IPS

MR-2077

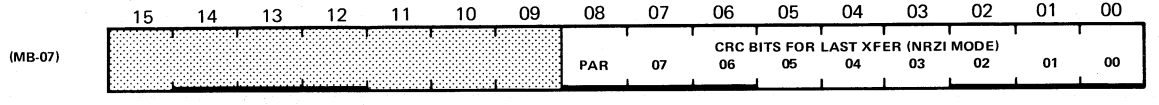
CK – Check Character



NOTE: ALL BITS READ ONLY
USE THIS BIT MAP FOR PHASE ENCODED DRIVES

MR-2078

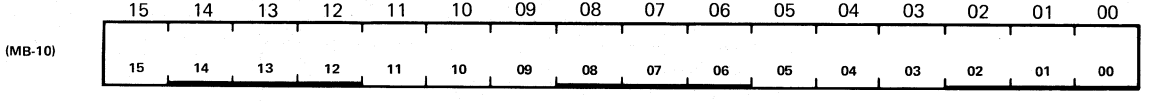
CK – Check Character



NOTE: ALL BITS READ ONLY
USE THIS BIT MAP FOR NRZI DRIVES

MR-2079

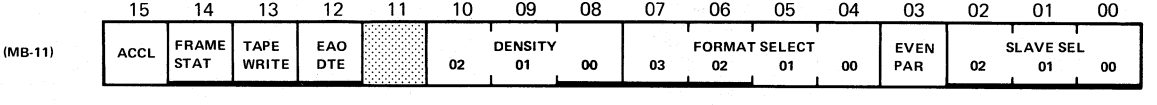
SN — Serial Number



NOTE: ALL BITS READ ONLY

MR-2080

TC — Tape Control

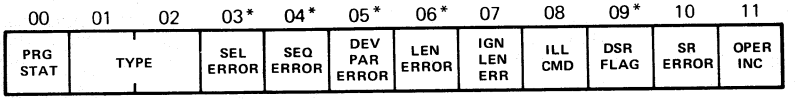


NOTE: ALL BITS READ/WRITE

15	ACCELERATION
14	FRAME COUNT STATUS
13	TAPE CONTROL WRITE
12	ENABLE ABORT ON DATA TRANS ERROR
3	EVEN PARITY
<02:00>	SLAVE SELECT BITS

MR-2081

CHANNEL STATUS REGISTER

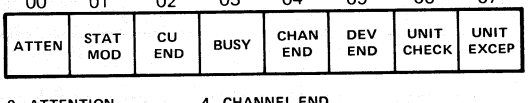


0 PROGRAM STATUS
1,2 TYPE 00 = INITIAL SELECTOR STATUS
01 = ENDING STATUS
10 = TX0X INITIATED STATUS
11 = IDLE STATUS
3 SELECTION ERROR
4 SEQUENCE ERROR
5 DEVICE PAR ERROR
6 LENGTH ERROR
7 IGNORE LENGTH ERROR
8 ILLEGAL COMMAND
9 DEVICE STATUS REGISTER FLAG
10 SENSE BYTE READ ERROR
11 OPERATION INCOMPLETE

*THIS REGISTER CONTAINS USEFUL ERROR INFORMATION WHEN CSR FLAG IN DX10 CONI IS SET.

MR-11411

DEVICE STATUS REGISTER



0 ATTENTION
1 STATUS MODIFIER
2 CONTROL UNIT END
3 BUSY
4 CHANNEL END
5 DEVICE END
6 UNIT CHECK
7 UNIT EXCEPTION

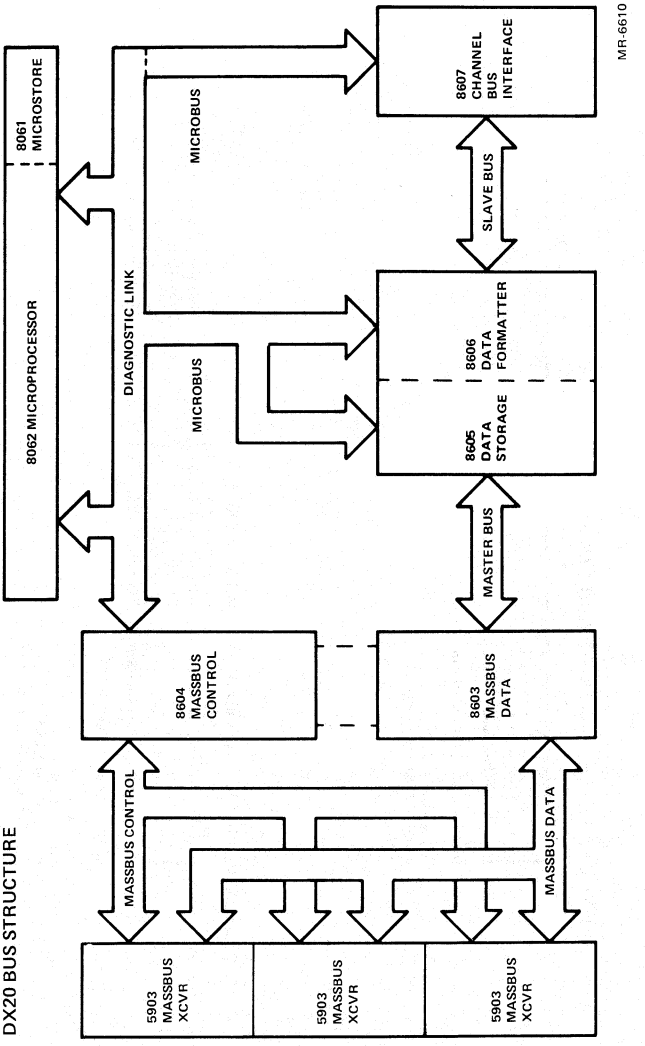
*SET DSR FLAG IN CHANNEL STATUS REGISTER.
THIS REGISTER CONTAINS USEFUL ERROR INFORMATION WHEN SET.

MR-11412

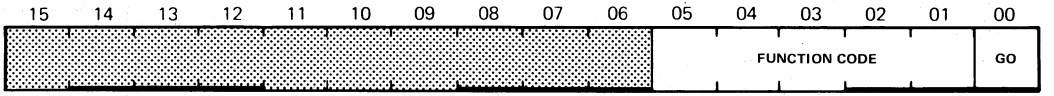
DX20 MASSBUS INTERFACE REGISTER DEFINITIONS

Refer to Microfiche Library Diagnostics DXMCA.SEQ for tape, DXMCD.SEQ for TOPS-10 disks, and DXMCE.SEQ for TOPS-20 disks.

The designators in parentheses after the register or bit names refer to the print set. This includes the printed circuit board, the page the printed circuit is located on in the print set, and its physical reference on that page.



CONTROL REGISTER – Address 00 (M8604-MC02 E91, 110)

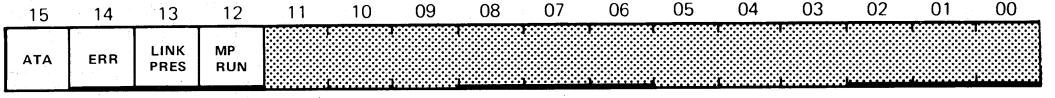


NOTE: ALL BITS ARE READ/WRITE.

15–06 NOT USED
05–01 FUNCTION CODE
00 GO

MR-6611

STATUS REGISTER – Address 01 (M8604-MC10 E8)



NOTE: ALL BITS ARE READ ONLY.

15 ATTENTION
14 ERROR
13 LINK PRESENT
12 MICROPROCESSOR RUN

MR-6612

CONTROL REGISTER - Address 00 (M8604-MC02 E91, 110)

Bits 15-06 - Not used.

Bits 05-01 - Function Code - The function code is the function to be performed. Valid operations to be put into bits 05-01 are as follows.

Code	Disk Functions	Tape Functions
01	No Operation	No Operation
03	-	Rewind Unload
05	Seek	-
07	Recalibrate	Rewind
11	Drive Clear	Drive Clear
13	-	Sense Release
25	-	Erase Gap
27	-	Write Tape Mark
31	Search	Forward Space Record
33	-	Backward Space Record
35	-	Forward Space File
37	-	Backward Space File
41	-	Test I/O
43	-	Data Security Erase
45	-	Sense
47	Sense	Sense Reverse
61	Write Data	Write Data
63	Write Format	Write Diagnostic
65	Write Special	Loop Write to Read
71	Read Data	Read Data
73	Read Format	-
75	Read Special	Read Extended Status
77	-	Read Reverse

Bit 00 - GO Bit - The GO bit causes the DX20 to study the data available to it and start the operation. The bit is cleared by the DX20 when the function is complete and the DX20 is then ready to accept another command.

NOTE
The GO bit cannot be set if error is set in the Status Register (address 01).

STATUS REGISTER - Address 01 (M8604-MC10 E8)

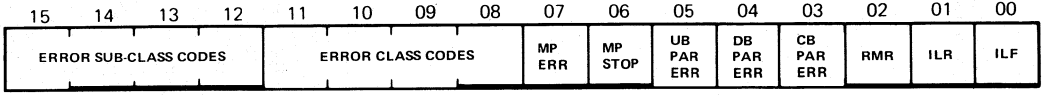
Bit 15 - Attention (M8604-MC02 E97) - The attention bit being set indicates that the DX20 has status ready for the host. To clear this bit, the attention bit corresponding to the Massbus device in the attention summary register (address 04) must be cleared.

Bit 14 - Error (M8604-MC03 E78) - This bit is set if an error condition is detected by the DX20, but has not been cleared by the host. When the error bit is set, the attention bit (bit 15) is also set. The error bit is cleared by clearing any bits in bit field 07-00 in the error register (address 02).

Bit 13 - Link Present (M8604-MC03 E76) - This bit is always set when the DX20 is in operation.

Bit 12 - Microprocessor Run (M8604-MC10 E8) - This bit is set if the microprocessor is running.

ERROR REGISTER – Address 02



NOTE: ALL BITS ARE READ/WRITE.

15–12	MICROPROCESSOR DETECTED ERROR SUB-CLASS CODE	04	DATA BUS PARITY ERROR
11–08	MICROPROCESSOR DETECTED ERROR CLASS CODE	03	CONTROL BUS PARITY ERROR
07	MICROPROCESSOR ERROR	02	REGISTER MODIFICATION REFUSED
06	MICROPROCESSOR STOPPED	01	ILLEGAL REGISTER
05	MICROBUS PARITY ERROR	00	ILLEGAL FUNCTION

MR-6613

ERROR REGISTER - Address 02

Bits 15-12 - Microprocessor Detected Error Class Code - Indicates which class error the microprocessor has detected. Each class has a type of error logging and recovery.

Bits 11-08 - Microprocessor Detected Error Subclass Code - Indicates a specific error within an error class. This error subclass is designed to be used for SYSERR in providing a detailed report of the failures.

The Error Class and Error Subclass Codes are as follows.

Class	Subclass	Description
1		Unusual Device or Status Condition - This code is not necessarily an error. It is set if the device returns a status byte with either a unit check (error) or unit exception (unusual condition) set. Refer to RP20 sense bytes (disk) or TX02 sense bytes (tape) for detailed information.
	0	Status is from the final sequence.
	1	Status is from the initial selection sequence.
2		Disk Only: Record Length - Indicates the last data transfer was not the correct length. This is always an error with disks.
2		Tape Only: Short record on a read, not necessarily an error.
3		Disk Only: Device Selection Error - Indicates that the addressed drive is not present (i.e., received SELECT IN).
3		Tape Only: Long record on a read.
4		Disk Only: Recoverable Error - Indicates the CPU may retry the operation.
	0	Data path parity error.
	1	Ending status byte parity error.
	2	Address Mismatch - Address returned by the drive does not match the correct address.
	3	Address Parity Error - Address returned by the drive has bad parity.
	4	Initial status byte parity error.
	5	Data path detected microbus parity error.
	6	Channel bus interface detected a microbus parity error.
	7	Channel handshake timeout.
	8	Device asserted disconnect in.
	9	Run was not received from RH20.
4		Tape Only: Device Select Error - Received Select In - Addressed a TX02 address that is not present.
5		Disk Only: Command Retry Request - The DX20 is in a command retry sequence with the drive and needs help from the host.

Class	Subclass	Description
5		Tape Only: Recoverable error during tape motion.
	0	Data path parity error on IBM channel bus.
	1	Parity error in final status byte from TX02.
6		Disk Only: Nonrecoverable Error - Issued if a parity error is detected on the channel bus which cannot be recovered after a known number of retries (microcode).
	0	Parity error receiving the drive address during the sequence initiated by the control unit. The microcode previously retried the operation five times.
	1	Parity error receiving the drive status during the sequence initiated by the control unit. The microcode previously retried the operation five times.
6		Tape Only: Recoverable error before tape motion.
	0	Address returned by TX02 because it did not match the correct address.
	1	Bus in parity error on IBM channel bus while receiving address from TX02.
	2	Bus in parity error on IBM channel bus in initial status byte.
	3	Run not received from RH20.
7		Disk Only: Retry log information available.
7		Tape Only: Nonrecoverable error because the tape position was not known.
	0	Data path (M8605, M8606) detected microbus parity error.
	1	Channel bus interface (M8607) detected microbus parity error.
	2	IBM channel bus handshake timeout with TX02.
	3	TX02 asserted disconnect in.
8		Disk Only: Fatal - Error cannot be corrected without repairing hardware or reloading the microcode. Error occurs along with the microprocessor halting.
	0	Drive type expected by the microcode does not match hardware drive type.
	1	Unknown Control Unit - Microcode detects a control unit other than the RP20 disk control unit (DCU).
	2	Massbus controller (RH20) power failed (power fail line).
	3	Microprocessor interrupted from interface 0 (nothing on interrupt 0).

Class	Subclass	Description
8		Tape Only: Fatal - Reload microcode or repair hardware; microprocessor is halted.
	0	Microcode drive type does not match hardware drive type.
	1	Parity error in the drive address during the sequence initiated by the control unit. Microcode has retried the operation five times.
	2	Parity error in the drive status byte during the sequence initiated by the control unit. Microcode has retried the operation five times.
	3	Massbus controller (RH20) power failed (power fail line).
	4	Microprocessor interrupted from Interface 0 (nothing on interrupt 0).
9		Diagnostic Error - Microprocessor loops on error if started at locations 3 or 4. Otherwise the microprocessor halts by a stack pointer underflow error. Either way, the error code and error flag are set. Extended status register 0 [E0(26) in SYSERR] includes the error number.
10		Disk Only: Interrupt on Full Initial Start-Up - Confirms that the host knows that the microcode has been started. Before entering the idle loop, the code is placed in the error register (address 02) and the attention bit in the status register (address 01) is set.

Bit 07 - Microprocessor Error (M8604-MC02 E80) - Set by the microprocessor to indicate that bits 08-15 include new error information.

Bit 06 - Microprocessor Stopped (M8604-MC02 E80) - Set when the DX20 halts, which is caused by a detected hardware failure.

Bit 05 - Microbus Parity Error (M8604-MC02 E86) - Set if the DX20 detects an error on its internal microbus. When set, the microprocessor halts, which sets the microprocessor stopped bit (bit 06).

Bit 04 - Data Bus Parity Error (M8604-MC02 E86) - Set if the DX20 receives data from the host with bad parity or if the data path from the DX20 includes bad parity transmitted to the host.

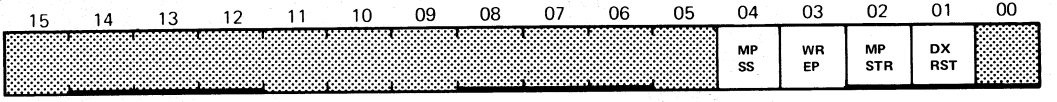
Bit 03 - Control Bus Parity Error (M8604-MC02 E95) - Set if the DX20 receives control information from the host with bad parity.

Bit 02 - Register Modification Refused (M8604-MC02 E95) - Set when the host tries to write into a register that is prevented from being written into because the GO bit (control register address 00) is set. The maintenance register (address 03) and the diagnostic register (address 31) are the only registers that can be written into when the GO bit is set.

Bit 01 - Illegal Register (M8604-MC02 E101) - Set if the host tries to access an undefined register.

Bit 00 - Illegal Function (M8604-MC02 E101) - Set if the host has asked for an illegal function to be performed.

MAINTENANCE REGISTER – Address 03

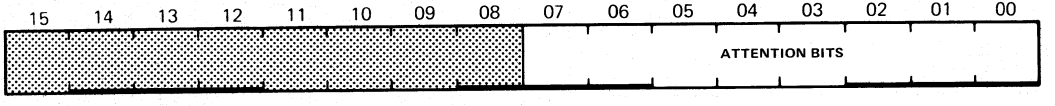


NOTE: ALL BITS ARE READ/WRITE.

15–05 NOT USED
04 MICROPROCESSOR SINGLE CYCLE
03 WRITE EVEN PARITY
02 MICROPROCESSOR START
01 DX20 RESET
00 NOT USED

MR-6614

ATTENTION SUMMARY REGISTER – Address 04



NOTE: ALL BITS ARE READ/WRITE.

15–08 NOT USED
07–00 ATTENTION BITS

MR-6615

MAINTENANCE REGISTER - Address 03

Bits 15-05 - Not used.

Bit 04 - Microprocessor Single Cycle - If set, the DX20 microprocessor will cycle its clock once per microprocessor start. Only the diagnostics use this bit.

Bit 03 - Write Even Parity - If set, the DX20 microprocessor generates even parity on the results of any ALU operation. Only the diagnostics use this bit.

Bit 02 - Microprocessor Start - When set by the host, the DX20 starts execution at its current PC location. If the host clears the bit, the DX20 halts at the end of the current instruction.

Bit 01 - DX20 Reset - When set by the host, the DX20 halts and resets all registers.

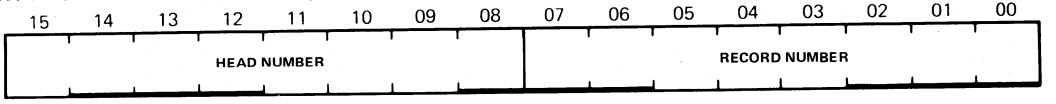
Bit 00 - Not used.

ATTENTION SUMMARY REGISTER - Address 04

Bits 15-08 - Not used.

Bits 07-00 Attention Bits - This register has one attention bit for each Massbus device. If the attention bit for device 3 is set, bit 3 of this register is set. To clear the attention bit in the status register (address 01), clear the bit that identifies the Massbus device.

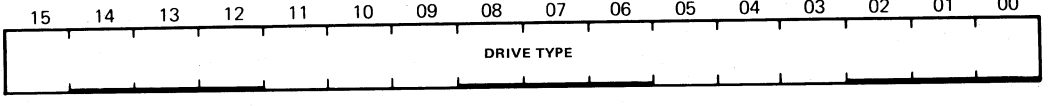
HEAD/RECORD REGISTER – Address 05 [Disks Only]
BYTE COUNT REGISTER – Address 05 [Tapes Only]



NOTE: ALL BITS ARE READ/WRITE.

MR-6616

DRIVE TYPE REGISTER – Address 06

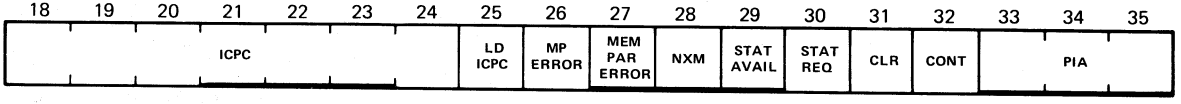


NOTE: ALL BITS ARE READ/WRITE.

15–00 DRIVE TYPE REGISTER

MR-6617

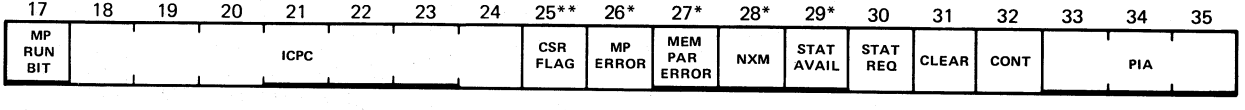
CONO BIT ASSIGNMENTS



18–24	INITIAL CHANNEL PROGRAM COUNTER	29	STATUS AVAILABLE
25	1 = INHIBIT ICPC LOAD	30	STATUS REQUEST
	0 = LOAD ICPC	31	CLEAR
26	MICROPROCESSOR ERROR	32	CONTINUE
27	MEMORY PARITY ERROR	33–35	PRIORITY INTERRUPT ASSIGNMENT
28	NONEXISTENT MEMORY		

MR-11409

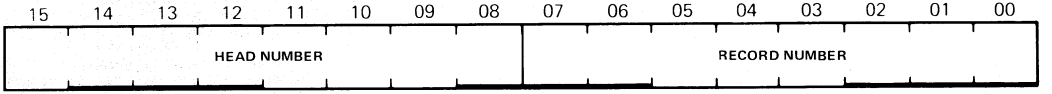
CONI BIT ASSIGNMENTS



BITS 18–24 AND 26–35 SEE CONO BIT ASSIGNMENTS.
17 MICROPROCESSOR RUN BIT
25 CSR FLAG
* CAUSES AN INTERRUPT TO THE CPO.
** AFTER SETTING THE CSR FLAG, THE PDP-BA SETS STATUS AVAILABLE.

MR-11410

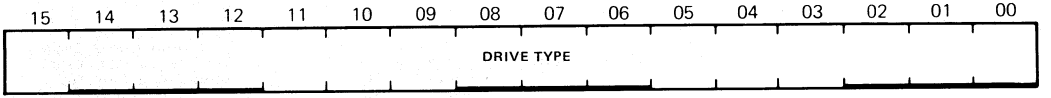
HEAD/RECORD REGISTER – Address 05 [Disks Only]
BYTE COUNT REGISTER – Address 05 [Tapes Only]



NOTE: ALL BITS ARE READ/WRITE.

MR-6616

DRIVE TYPE REGISTER – Address 06



NOTE: ALL BITS ARE READ/WRITE.

15–00 DRIVE TYPE REGISTER

MR-6617

HEAD/RECORD REGISTER - Address 05 [Disks Only]
BYTE COUNT REGISTER - Address 05 [Tapes Only]

This register is used interchangeably with address 25. Both addresses access the same register. Refer to address 25 for a description of the contents of this register.

DRIVE TYPE REGISTER - Address 06

Bits 15-00 - Drive Type Register - This register includes the hardware drive type code that differentiates the DX20 from other devices on the Massbus. The microcode checks the contents of the register. If the drive type is not correct, an error code is written into the error register (address 02). Microprocessor error and halt bits are also set in the error register.

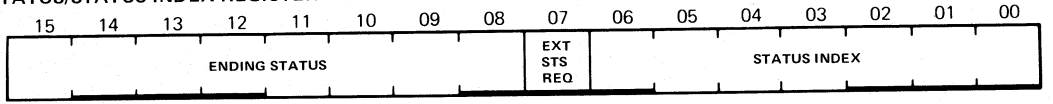
The legal drive types are as follows.

050060 DX20-V100 interfaces with TX02 tape subsystem.

010061 DX20-V200 interfaces with RP20 disk subsystem.

010052 DX20-V400 interfaces directly to an IBM 360/370 by acting as a peripheral on the IBM selector channel bus.

ENDING STATUS/STATUS INDEX REGISTER – Address 20

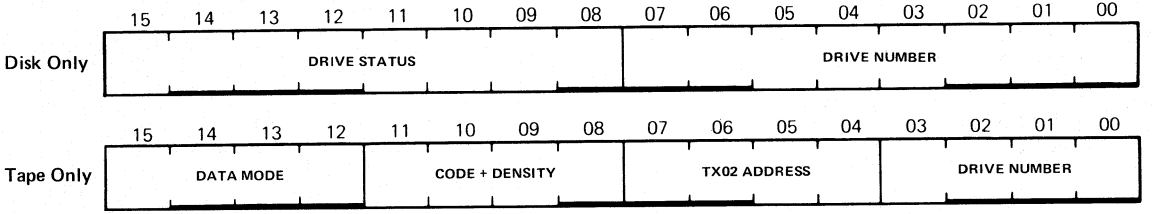


NOTE: ALL BITS ARE READ/WRITE.

15–08 ENDING STATUS
07 EXTENDED STATUS REQUEST
06–00 STATUS INDEX

MR-6618

ASYNCHRONOUS ADDRESS REGISTER – Address 21 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 01 – Address 21 (M8604-MC06) [Tape Only]



NOTE: ALL BITS ARE READ/WRITE.

DISK ONLY: 15–08 DRIVE STATUS
07–00 DRIVE NUMBER

TAPE ONLY: 15–12 DATA MODE
11–08 CODE + DENSITY
07–04 TX02 ADDRESS
03–00 DRIVE NUMBER

MR-6619

ENDING STATUS/STATUS INDEX REGISTER - Address 20

Bits 15-08 - Ending Status - These bits include the device status bytes.

Bit 07 - Extended Status Request - The host sets this bit to request the DX20 microcode to change the extended status registers (addresses 26 and 27) according to the status index. This bit is set by the DX20 if a sense operation is performed at command completion, indicating an update to the extended status registers is in progress. Either way, the DX20 microcode clears this bit after the extended status register updates are completed.

Bits 06-00 - Status Index - These bits are used to index into the extended status table. The setting of bits 00-07 by the host allows the DX20 to select status information specified by the status index and load it into the extended status registers (addresses 26 and 27). When the updates to the extended status registers are completed, the DX20 microcode clears the extended status request bit (bit 07).

Status information (bytes) in this register may not agree with the operation because of the unit check bit being set in the ending status byte of the DX20 read sense bytes. Status information also may not correspond due to the setting of the force sense bit or a sense operation being performed. Sense operations, performed by the DX20 microcode at command completion, reset the status index and set the extended status request bit while updating the extended status registers. If the status index is larger than the size of the extended status table, the DX20 microcode will clear the index field and update the extended status registers using index 0. After completing the extended status register updates, the DX20 sets the extended status request bit, which indicates completion of the updates.

NOTE
The host should not write into this register while the extended status request bit (bit 07) is set.

ASYNCHRONOUS STATUS REGISTER - Address 21 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 01 - Address 21 (M8604-MC06) [Tape Only]

Disk Only:

Bits 15-08 - Drive Status - Drive status, which is usually the device end.

Bits 07-00 - Drive Number - The number of drives showing asynchronous status.

Tape Only:

Bits 15-12 - Data Mode - Indicates the mode of data being used.

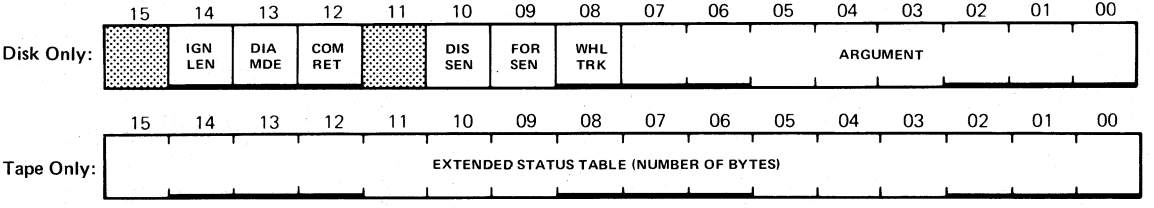
Bits 11-08 - Code and Density - Codes and Density for the drives are as follows.

Code	Density	Mode
00	No Mode Set	
01	7-Track 508 bits/cm (200 bits/in)	Odd Parity
02	7-Track 1412 bits/cm (556 bits/in)	Odd Parity
03	7-Track 2032 bits/cm (800 bits/in)	Odd Parity
05	7-Track 508 bits/cm (200 bits/in)	Even Parity
06	7-Track 1412 bits/cm (556 bits/in)	Even Parity
07	7-Track 2032 bits/cm (800 bits/in)	Even Parity
13	9-Track 2032 bits/cm (800 bits/in)	NRZI
14	9-Track 4064 bits/cm (1600 bits/in)	PE
15	9-Track 15875 bits/cm (6025 bits/in)	GCR

Bits 07-04 - TX02 Address - This address is usually zero.

Bits 03-00 - Drive Number - The number of the drive showing asynchronous status.

FLAGS/ARGUMENT REGISTER — Address 22 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 02 — Address 22 (M8604-MC06) [Tape Only]



NOTE: ALL BITS ARE READ/WRITE.

DISK ONLY:

15	SPARE BIT	10	DISABLE SENSE
14	IGNORE LENGTH	09	FORCE SENSE
13	DIAGNOSTIC MODE	08	WHOLE TRACK
12	COMMAND RETRY	07–00	ARGUMENT
11	NOT USED		

MR-6620

FLAGS/ARGUMENT REGISTER - Address 22 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 02 - Address 22 (M8604-MC06) [Tape Only]

Disk Only:

Bit 15 - Spare bit.

Bit 14 - Ignore Length - When set, record Lengths other than 576 bytes for TOPS-10 (2304 bytes for TOPS-20) may be read or written into with the DX20 ignoring length records. Records other than 584 bytes long (total) for TOPS-10 (2312 for TOPS-20) can be formatted and verified with this bit set. This block count in the RH20 and the word count in the channel must be met when this bit is set.

Bit 13 - Diagnostic Mode - Set when read and write special operate in diagnostic mode.

Bit 12 - Command Retry - Set by the DX20 when command retry assistance is asked for from the host. The host clears this bit if it is determined that command retry asistance is not needed. The host never sets this bit. The DX20 microcode continues command retry when the Command Register is reloaded with the GO bit set.

Bit 11 - Not used.

Bit 10 - Disable Sense - Set to suppress the sense operation when a unit check condition is detected. The force sense bit (bit 09) overrides this bit. This bit is present for diagnostic purposes.

Bit 09 - Force Sense - A sense operation is performed on completion of this command, which is not dependent on the setting of unit check in the final status.

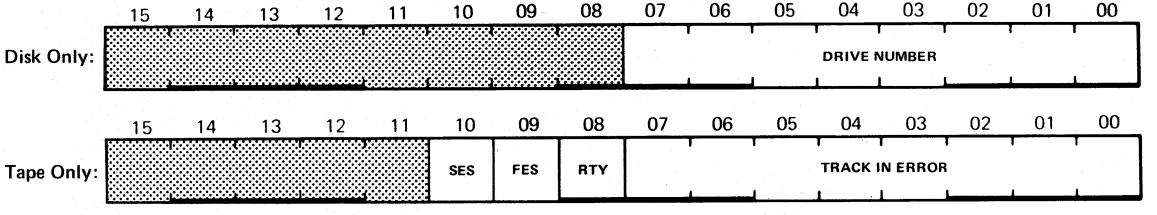
Bit 08 - Whole Track - If set when a read format is issued, the complete track is read beginning at the home address. If the bit is cleared, only part of the track that starts with the record in the head/record register (addresses 05 and 25) is read. If set during a write format, the entire track, including the home address, is formatted. This bit is used for diagnostic purposes only.

Bits 07-00 - Argument - For sense and no operation commands, these bits include operations to be performed. For read special macro in diagnostic mode, these bits contain the control byte identifying the 512-byte block of microcode to be transferred.

Tape Only:

Bit 15 - Includes the number of bytes in the extended status table.

DRIVE NUMBER REGISTER — Address 23 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 03 — Address 23 (M8604-MC06) [Tape Only]



NOTE: ALL BITS ARE READ/WRITE.

DISK ONLY:
15–08	FUTURE USE
07–00	DRIVE NUMBER

TAPE ONLY:
15–11	NOT USED
10	SUPPRESS EXTENDED STATUS
09	FORCE EXTENDED STATUS
08	RETRY
07–00	TRACK IN ERROR

MR-6621

DRIVE NUMBER REGISTER - Address 23 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 03 - Address 23 (M8604-MC06) [Tape Only]

Disk Only:

Bits 15-08 - Future use.

Bits 07-00 - Drive Number - Includes the drive number (device address) for the operation defined in the function code field of the control register.

Tape Only:

Bits 15-11 - Not used.

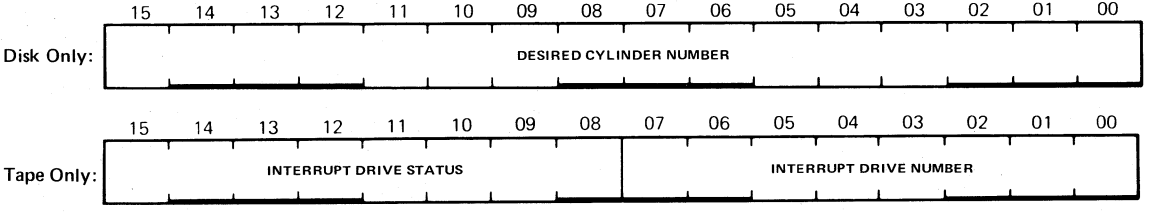
Bit 10 - Supress extended status - When set, causes the DX20 not to get extended status from the TX02 even with the unit check bit set in the TX02 status byte.

Bit 09 - Force Extended Status - When set, the DX20 gets extended status from the TX02 on completion of the operation. The DX20 normally gets Extended Status only if the TX02 returns the unit check bit in the status byte.

Bit 08 - Retry - When set, causes the DX20 to automatically retry the operation if there is an error.

Bits 07-00 - Track In Error - The DX20 writes the track in error from the TX02.

CYLINDER REGISTER — Address 24 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 04 — Address 24 (M8604-MC06) [Tape Only]



NOTE: ALL BITS ARE READ/WRITE.

DISK ONLY: BITS 15–00 CONTAIN THE DESIRED CYLINDER NUMBER FOR THE CURRENT OPERATION.

TAPE ONLY: 15–08 INTERRUPT DRIVE STATUS
07–00 INTERRUPT DRIVE NUMBER

MR-6622

CYLINDER REGISTER - Address 24 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 04 - Address 24 (M8604-MC06) [Tape Only]

Disk Only:

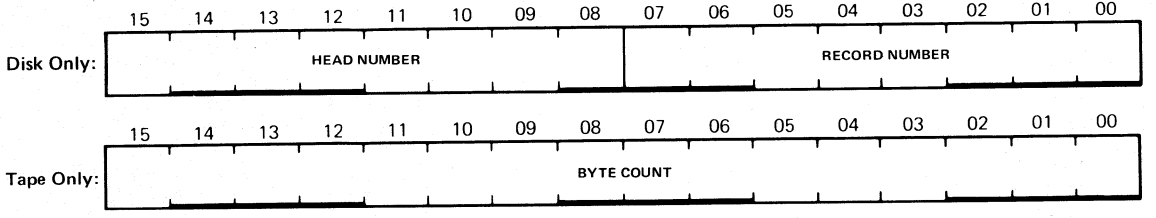
Bits 15-00 have the needed cylinder number for the current operation.

Tape Only:

Bits 15-08 - Interrupt Drive Status - These bits include the number of the drive that interrupted. The interrupt is caused by rewind completed or drive coming on-line.

Bits 07-00 - Interrupt Drive Number - These bits include the TX02 status byte that goes with the interrupt.

HEAD/RECORD REGISTER — Address 25 (M8604-MC06) [Disk Only] *
GENERAL PURPOSE REGISTER 05 — Address 25 (M8604-MC06) [Tape Only] *



*THIS REGISTER IS THE SAME AS THE HEAD/RECORD REGISTER (ADDRESS 05).

NOTE: ALL BITS READ/WRITE.

DISK ONLY: 15–08 HEAD NUMBER
07–00 RECORD NUMBER

TAPE ONLY: 15–00 BYTE COUNT REGISTER

MR-6623

HEAD/RECORD REGISTER - Address 25 (M8604-MC06) [Disk Only]
GENERAL PURPOSE REGISTER 05 - Address 25 (M8604-MC06) [Tape Only]

Disk Only:

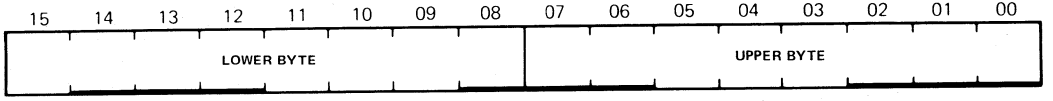
Bits 15-08 - Head Number - These bits include the correct head number for the current operation.

Bits 07-00 - Record Number - These bits include the correct start head for the current operation.

Tape Only:

15-00 - Byte Count Register - This register must be set to 2's complement of the expected record length at the start of the operation. At the completion of a read operation, the positive length of the record is returned in this register. On a nondata transfer operation, set this register to 2's complement of the number of times the operation is to be repeated. At termination this register includes 2's complement of the number of repeats not performed. (This register is the same as the head/record register - address 05.)

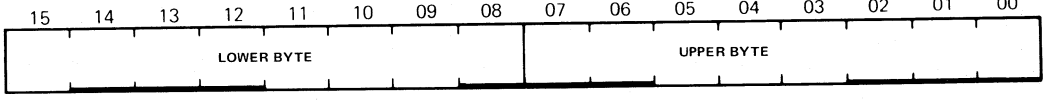
EXTENDED STATUS REGISTER – Address 26



NOTE: ALL BITS ARE READ/WRITE.

MR-6624

EXTENDED STATUS REGISTER 01 – Address 27



NOTE: ALL BITS ARE READ/WRITE.

MR-6625

EXTENDED STATUS REGISTER 0 - Address 26

This register returns spare status information to the host from the extended status table. The information from the extended status table in this register depends on the index placed in the ending status/status index register (address 20). Two bytes of information are returned to this register, with the lower numbered byte being bits 15-08.

Index	Contents
00	Sense Bytes 00 and 01
01	Sense Bytes 04 and 05
02	Sense Bytes 08 and 09
03	Sense Bytes 12 and 13
04	Sense Bytes 16 and 17
05	Sense Bytes 20 and 21
06	Microcode Version Number
07	MBI Registers 00 and 01
10	MBI Registers 04 and 05
11	MBI Registers 10 and 11
12	MBI Registers 14 and 15
13	MBI Registers 20 and 21
14	MBI Registers 24 and 25
15	CBI Registers 00 and 01
16	CBI Registers 04 and 05
17	Data Path Registers 00 and 01
20	Data Path Registers 04 and 05
21	Data Path Registers 10 and 11
22	Data Path Registers 14 and 15
23	Last Command Sent; Last Device Address
24	Diagnostic Bytes 00 and 01
25	Diagnostic Bytes 04 and 05
26	Diagnostic Bytes 08 and 09
27	Diagnostic Bytes 12 and 13

EXTENDED STATUS REGISTER 01 - Address 27

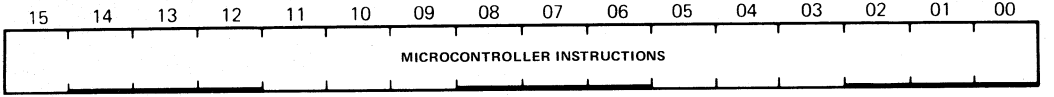
This register is used to return spare status information to the host from the extended status table. The information from the extended status table placed in this register depends on the index placed in the ending status/status index register (address 20).

Index	Contents
00	Sense Bytes 02 and 03
01	Sense Bytes 06 and 07
02	Sense Bytes 10 and 11
03	Sense Bytes 14 and 15
04	Sense Bytes 18 and 19
05	Sense Bytes 22 and 23
06	Microprocessor Status Register; I/O Bank Select
07	MBI Registers 02 and 03
10	MBI Registers 06 and 07
11	MBI Registers 12 and 13
12	MBI Registers 16 and 17
13	MBI Registers 22 and 23
14	MBI Registers 26 and 27
15	CBI Registers 02 and 03
16	CBI Registers 06 and 07
17	Data Path Registers 02 and 03
20	Data Path Registers 06 and 07
21	Data Path Registers 12 and 13
22	Data Path Registers 16 and 17
23	Last Asynchronous Status; Last Asynchronous Device
24	Diagnostic Bytes 02 and 03
25	Diagnostic Bytes 06 and 07
26	Diagnostic Bytes 10 and 11
27	Diagnostic Bytes 14 and 15

DIAGNOSTIC REGISTER 0 - Address 30

Bits 15-00 - Instruction Register - This is a 16-bit read/write microcontroller register accessible from the Massbus control bus. It includes instructions to be performed by the microcontroller. Reading or writing operations depend on the contents of diagnostic register 01 (bits 15, 14 and 12). The register is cleared by DX reset.

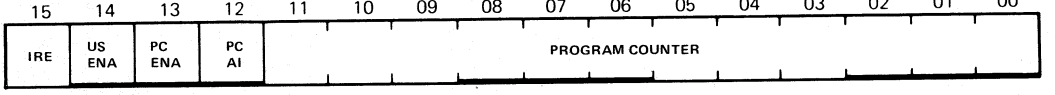
DIAGNOSTIC REGISTER 0 — Address 30



NOTE: ALL BITS ARE READ/WRITE.

MR-6626

DIAGNOSTIC REGISTER 01 — Address 31

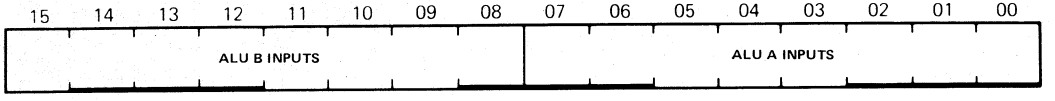


NOTE: ALL BITS ARE READ/WRITE.

15 INSTRUCTION REGISTER ENABLE
14 MICROSTORE ENABLE
13 PROGRAM COUNTER ENABLE
12 PROGRAM COUNTER AUTOINCREMENT
11–00 PROGRAM COUNTER

MR-6627

DIAGNOSTIC REGISTER 02 — Address 32



NOTE: ALL BITS ARE READ ONLY.

15–08 ALU B INPUTS
07–00 ALU A INPUTS

MR-6628

DIAGNOSTIC REGISTER 01 - Address 31

Bit 15 - Instruction Register Enable - This bit is set by the host to allow the microcontroller to execute or run a program stored in microstore. With this bit set, reading or writing into the instruction register (address 30) from the Massbus control bus, results in the instruction register being loaded from the microstore location being pointed to by the program counter (bits 11-00). With this bit cleared, reading the instruction register from the control bus does not change the current contents of the instruction register. Writing into the instruction register loads data into the instruction register from the control bus data lines. This bit is cleared by DX reset.

Bit 14 - Microstore Enable - This bit is cleared during typical operation and prevents writing into the microstore. When this bit is set and instruction register enable bit (bit 15) is cleared, the microstore location pointed to by the current PC is loaded from the Massbus control data bus lines via the Instruction Register multiplexer (address 30) during a control bus write to the instruction register. When the instruction register enable is set (and this bit is set), a control bus write into the instruction register loads ones into the microstore location pointed to by the PC and into the instruction register. This bit is cleared by DX reset.

Bit 13 - Program Counter Enable - When this bit is set, the program counter lines (bits 11-00) are loaded from the Massbus control data lines during a control bus write to the program counter (PC). This bit is set during typical microprogram execution, because the host loads the PC before starting the microprocessor and does not clear it. Once the microprocessor is loaded, a write to the PC has no effect. This bit must be cleared before the host can modify the instruction register enable bit, the microstore enable bit, or the program counter auto-increment bit. It is possible to set this bit and load PC in the same control bus write operation. This bit is cleared by DX reset and when cleared will not change the PC.

Bit 12 - Program Counter Auto-Increment - This bit is set to allow automatic incrementing of the PC. With this bit and the microstore enable bit both set, and the instruction register enable bit reset, control bus write operations of the instruction register, will load consecutive locations of the microstore via the Instruction Register without having to load the PC each time. The PC is incremented following a read or write of the current microstore location. When bit is cleared, the microcontroller is allowed to repeat the execution of an instruction. This bit is cleared by DX reset.

Bits 11-00 - Program Counter - This 12-bit register includes the microcontroller program counter used to address the microstore (CRAM). It can be written into from the Massbus when program counter enable (bit 13) is set and microprocessor start is cleared. This register is cleared by DX reset.

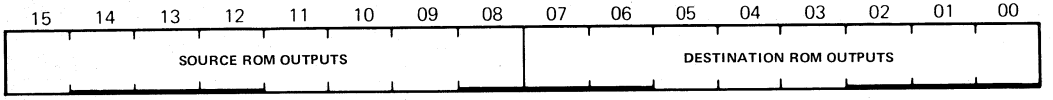
DIAGNOSTIC REGISTER 02 - Address 32

Bits 15-08 - ALU B Inputs - These bits include the inputs to the "A" side of the ALU which are received from one of the eight accumulator registers. To determine which accumulator register is being read, instruction register bits 06-04 (address 30) must be decoded in a direct octal code.

Bits 07-00 - ALU A Inputs - These bits include the inputs to the "B" side of the ALU which are received from the output of the source multiplexer. These outputs, selected by the source ROM, are available from instruction register bits 15-00 (address 30), input multiplexer bits 15-08 (address 36), memory register bits 07-00 (address 35) and buffer register bits 07-00 (address 36). To determine which outputs are being read, source ROM bits 05 and 06 (SROM bits 05 and 06, address 33) must be decoded. The source decoding of these bits is as follows.

SROM 06	SROM 05	Source
0	0	Instruction Register
0	1	Input Multiplexer
1	0	Memory Register
1	1	Buffer Register

DIAGNOSTIC REGISTER 03 – Address 33

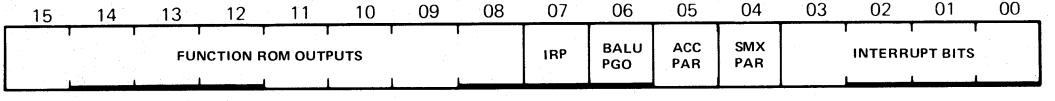


NOTE: ALL BITS ARE READ ONLY.

15–08 SOURCE ROM OUTPUTS
07–00 DESTINATION ROM OUTPUTS

MR-6629

DIAGNOSTIC REGISTER 04 – Address 34



NOTE: ALL BITS ARE READ ONLY.

15–08 FUNCTION ROM OUTPUTS
07 INSTRUCTION REGISTER PARITY
06 BALU PARITY GENERATOR OUTPUT
05 ACCUMULATOR PARITY
04 SOURCE MUX PARITY
03–00 INTERRUPT BITS 03–00

MR-6630

DIAGNOSTIC REGISTER 03 - Address 33

Bits 15-08 - Source ROM Outputs - The location of the source ROM (SROM) outputs being read is determined by the following instruction register bits: IR15, IR14, IR13, IR09, and IR08. The eight outputs are determined as follows for a logical 01.

SROM7 = -MA EXT BITS EN
SROM6 = SMUX S1
SROM5 = SMUX S0
SROM4 = -MOV INST
SROM3 = MOV INST
SROM2 = SEC SEL EN
SROM1 = ALU PAR CHK EN
SROM0 = IBUS

Bits 07-00 - Destination ROM Outputs - The location of the destination ROM (DROM) outputs being read is determined by the following instruction register bits: IR09, IR08, IR12, IR11, and IR10. The eight outputs are determined as follows for a logical 01.

DROM7 = WRITE MEM
DROM6 = WRITE AC
DROM5 = MAR INC EN
DROM4 = -MAR LD EN
DROM3 = WRITE OUT
DROM2 = PUSH/POP
DROM1 = BR S1
DROM0 = BR S0

DIAGNOSTIC REGISTER 04 - Address 34

Bits 15-08 - Function ROM Outputs - These bits indicate which of the 32 locations of the function ROM (FROM) are being read, as determined by the following instruction register bits: IR14, IR03, IR02, IR01, and IR00. The eight outputs use the following logical names for a logical 1.

FROM7 = CLK C
FROM6 = EN C
FROM5 = FORCE C
FROM4 = -ALU S0
FROM3 = -ALU S1
FROM2 = -ALU S2
FROM1 = -ALU S3
FROM0 = ALU M

Bit 07 - Instruction Register Parity - This bit indicates that the instruction register parity was read from the microstore or received from the Massbus, depending on when it was read. This bit is cleared by DX reset.

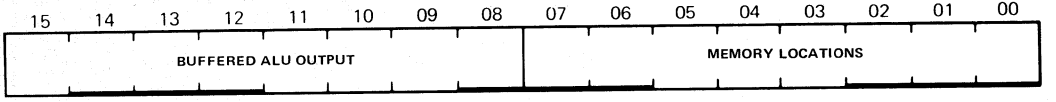
Bit 06 - BALU Parity Generator Output - This bit feeds the BALU parity logic and indicates the parity being generated by the outputs of the ALU.

Bit 05 - Accumulator Parity - This is the parity bit for one of the eight ALU A input bits (address 32, bits 07-00). If instruction register (address 30, bits 06-04) is the same as when diagnostic register 02 was read, this bit echos the correct parity for ALU A input bits (address 32, bits 07-00).

Bit 04 - Source MUX Parity - This is the parity bit for the source multiplexer. If the instruction register (address 30) bits are the same as when diagnostic register 02 was read, this bit shows the correct parity for the ALU A input bits (address 32, bits 07-00).

Bits 03-00 - Interrupt - These bits include the status of the microbus interrupt lines (UBUS INT 03-00). This register is clocked at the microprocessor time state T60 and is cleared by DX reset.

DIAGNOSTIC REGISTER 05 – Address 35



NOTE: ALL BITS ARE READ ONLY.

15–08 BUFFERED ALU OUTPUT 07–00
07–00 MEMORY LOCATIONS 07–00

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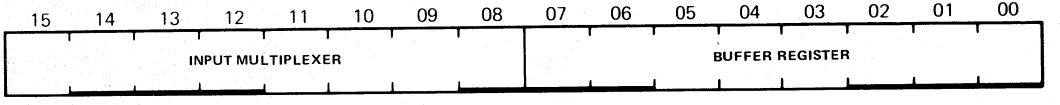
DIAGNOSTIC REGISTER 06 – Address 36



NOTE: ALL BITS ARE READ ONLY.

15–08 INPUT MULTIPLEXER (07–00)
07–00 BUFFER REGISTER (07–00)

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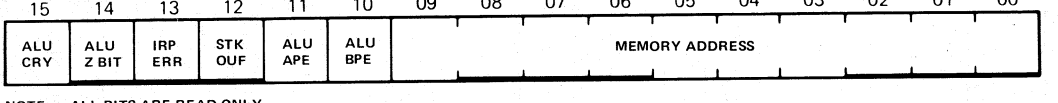
DIAGNOSTIC REGISTER 07 – Address 37



NOTE: ALL BITS ARE READ ONLY.

15 ALU CARRY BIT
14 ALU Z BIT
13 INSTRUCTION REGISTER PARITY ERROR
12 STACK OVER/UNDER FLOW
11 ALU A PARITY ERROR
10 ALU B PARITY ERROR
09–00 MEMORY ADDRESS 09–00

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DIAGNOSTIC REGISTER 05 - ADDRESS 35

Bits 15-08 - Buffered ALU Output (07-00) - This register includes the output of the ALU, as of the last microprocessor T180 time state. This register is cleared by DX reset.

Bits 07-00 - Memory Locations (07-00) - This register includes the output of one of the 1024 working memory locations pointed to by the memory address register (address 37). The data stored in working memory comes from the BALU.

DIAGNOSTIC REGISTER 06 - Address 36

Bits 15-08 - Input Multiplexer (07-00) - The outputs of this register are fed into the source multiplexer (SMUX). The outputs available from the input multiplexer are the Ubus data register, the I/O bank register, and the status register. The Ubus data register includes the data strobed from the microbus data lines on the last DATI instruction. The I/O bank register is used for selecting different microbus interfaces for I/O operations. The status register inputs are available from bits 15 and 14 in diagnostic register 7 - address 37, and from bits 03-00 in diagnostic register 4 - address 34. These bits are cleared by DX reset.

Bits 07-00 - Buffer Register (07-00) - The outputs of this register is fed into the source multiplexer (SMUX). The buffer register is loaded from the BALU at microprocessor time state T30. This register can be used for a "rotate right" operation under the control of DROM (diagnostic register 03 - address 33) bits 00 and 01. This register is cleared by DX reset.

DIAGNOSTIC REGISTER 07 - Address 37

Bit 15 - ALU Carry Bit - When set this bit indicates a carry takes place from the most significant bit of the ALU as a result of the last move instruction with an arithmetic ALU function. This bit is cleared by DX reset.

Bit 14 - ALU Z Bit - This bit is set when the output of the ALU from a move instruction is equal to all 1s. The Z bit is used in the comparison of the A and B inputs of the ALU. By placing the ALU in the 1's complement subtract mode, a magnitude comparison of the A and B inputs is made. This bit is cleared by DX reset.

Bit 13 - Instruction Register Parity Error - Set when the input to the instruction register (address 30) has even parity. This bit is cleared by DX reset.

Bit 12 - Stack Over/Under Flow - Set when the hardware detects a stack overflow (too many pushes) or a stack underflow (too many pops). This bit is reset by DX reset or SP reset. SP reset is a bit within the I/O bank register (diagnostic register 06 - address 36 [bits 15-08]) which the microprocessor sets.

Bit 11 - ALU A Parity Error - This bit is set when the inputs to the A side of the ALU have even parity. This bit is cleared by DX reset.

Bit 10 - ALU B Parity Error - This bit is set when the inputs to the B side of the ALU have even parity. This bit is cleared by DX reset.

Bits 09-00 - Memory Address - This 10-bit register includes the address for selecting one of 1K (1024 decimal) working memory locations. This register is loaded in two bytes from the BALU and is cleared by DX reset.

BYTE I T	0 (8)	1 (4)	2 (2)	3 (1)	4 (8)	5 (4)	6 (2)	7 (1)	BYTE I T
0	COMMAND REJECT	INTERVENTION REQUIRED	BUS OUT CHECK	EQUIPMENT CHECK	DATA CHECK	OVERRUN	WORD COUNT ZERO	DATA CONVERT CHECK	0
1	NOISE	TU STATUS A	TU STATUS B	7-TRK	LOAD POINT	SELECTED & WR STAT	FILE PROTECTED	NOT CAPABLE	1
2	TRACK IN ERROR								2
3	R/W VRC	MTE/LRC	SKEW ERROR	END DATA CK /CRC	ENV CK/ SKEW VRC	1600 BPI SET IN TU	BACKWARD	C/P COMP.	3
4		REJECT TU	TI	WRITE TRG VRC		LWR	TU CHECK	RPQ	4
5		NEW SUBSYSTEM	WTM CHECK **	ID BURST CK **	START READ CHECK *	PARTIAL RECORD **	POSTAMBLE ERROR **	RPQ	5
6	7-TRK TU **	WRITE CURRENT FAIL **	DUAL DENSITY TU ***	NOT 1600 **	TAPE UNIT MODEL IDENTIFICATION				6
7	COLUMN TOP OR BTM ***	LEFT. COL. FAIL ***	RIGHT COL. FAIL ***	RESET KEY ***	DSE FAILURE	ERASE HD FAILURE ***		LOAD FAILURE ***	7
8	IBG DETECTED **								8
9	6250 CORRECTION ***	VELOCITY CHANGE	CHANNEL BUFFER CK **	CRC III **	6250 **			TCU RESERVED	9
10	CMND STAT REJECT **			RECORD NOT DETECTED		TACH START FAIL **		VELOCITY CHECK **	10
11									11

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12									12
13	CU FEATURES			CONTROL UNIT UNIQUE IDENTIFICATION (HI-ORDER PART S/N) 4096	2048	1024	512	256	13
14	128	64	32	16	8	4	2	1	14
15			8192	TAPE UNIT UNIQUE IDENTIFICATION (HI–ORDER PART S/N) 4096	2048	1024	512	256	15
16	128	64	32	16	8	4	2	1	16
17	2 CH SW FEATURE	SWITCH FEATURES			REFLECTS TCU DIAGNOSTIC RELEASE LEVEL				17
18		SAME	TU	I.D.	TU		E.C. LEVEL		18
19	TU 7	TU 6	TU 5	BUSY STATUS, LO–ORDER TAPE UNITS TU 4	TU 3	TU 2	TU1	TU 0	19
20	TU F	TU E	TU D	BUSY STATUS, HI–ORDER TAPE UNITS TU C	TU B	TU A	TU9	TU 8	20
21									21
22	"REFER TO MICROPROGRAM PAGE QA025" **								22
23	MOD IV TCU **	"REFER TO MICROPROGRAM PAGE AQ025" **							23
BYTE I T	0 (8)	1 (4)	2 (2)	3 (1)	4 (8)	5 (4)	6 (2)	7 (1)	BYTE I T

* TX01 ONLY ** TX02 ONLY *** TU72 ONLY

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Table of Contents

CHECKS/ADJ

RH20 MASS FAIL ADJ

1 Attach channel 1 probe to appropriate pin for RH20 being adjusted.

RH20 #	PIN #
0	2F34T2
1	2F31T2
2	2F28T2
3	2F25T2
4	2F22T2
5	2F19T2
6	2F16T2
7	2F13T2

2 Adjust MASS FAIL potentiometer on appropriate M8555 one turn beyond the point at which it goes low.

WHEN TO DESKEW

When doing adjustments of fault correction of power supplies related to the following modules, check the appropriate deskews.

LOGIC ASSY.	MODULE REPLACED	DESKEW
CPU Bay	M8526 - CLK CPU Clock Module	DMA20, All MA20s, All MB20s, All RH20s
	M8519 - MEM (Slot 07) SBus Translator	DMA20, All MA20s, All MB20s
	M8516 - TRN (Slot 06) E & C Bus Translator	All RH20s
MA20	M8562 - MA20 Timing Module	MA20
	M8561 - MA20 Control Module	MA20
	SBus Cable	MA20
DMA20	M8563 - DMC Adapter Interface DMA20 Board Two	DMA20
	M8560 - DTR DMA Timing and S Bus Transceivers	DMA20
	SBus Cable	MB20
MB20	M8565 MB20 Timing Module	MB20
	M8568 MB20 Control Module	MB20
	SBus Cable	MB20
I/O BAY	M8559 - CDS I/O Bay Clock Distribution Module	All RH20s
	M8556-DP RH20 Data Path	RH20

RH20 DESKEW PROCEDURE

EQUIPMENT REQUIRED

Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

OBJECTIVE

ALL RH20s are deskewed to the MBox clock that produces channel time zero, CHT0.

NOTES

Recheck skew whenever the CBus cable or the M8556 module is replaced.

The adjustments are made on the M8559 module. The top potentiometer is for RH20 #0, the second potentiometer is for RH20 #1, etc.

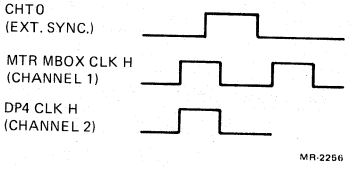
ADJUSTMENT PROCEDURE

Attach a probe (either ext, sync or channel 3) to CHT0 H, 4B09K1.

Sync positve external.

Attach channel 1 probe to MTR MBOX CLK H, 4D33P1.

Push TRIGGER VIEW and verify that the MBOX CLK that occurs just prior to CHT0 can be seen on the scope. See diagram below.



Attach channel 2 probe to appropriate clock pin for RH20 being deskewed. See chart below.

RH20	PIN
0	2A36D2
1	2A33D2
2	2A30D2
3	2A27D2
4	2A24D2
5	2A21D2
6	2A18D2
7	2A15D2

Align clock pulse on channel 2 with the MBox clock that occurs approximately 10 nanoseconds before CHT0. Do this for all RH20s that are installed.

MA20/MB20 DESKEW PROCEDURE

EQUIPMENT REQUIRED
Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

OBJECTIVE
To assure proper clock alignment between KL10 and MA20/MB20 controller.

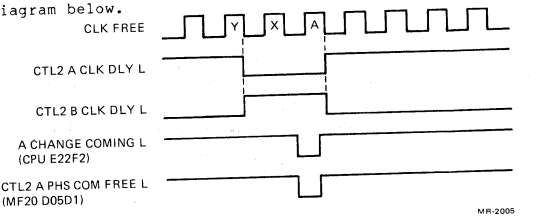
NOTES
Select CR0 on the KL10. Type a MR and then a FX1 to turn on the clock.

The M8562 delay lines are arranged so that A clock is the top potentiometer and B clock is the bottom potentiometer.

ADJUSTMENT PROCEDURE
Attach a probe (either external sync or channel 3) to A CHANGE COMING L, 4E22F2. Set scope for external trigger and negative edge.

Attach channel 1 probe to MTR MBOX CLK C, 4D33P1. Use 0.5 V/CM and set scope such that the ground reference is 1.3 V above the centerline.

Press TRIGGER VIEW and observe that the relationship of MTR MBOX CLK C to A CHANGE COMING L corresponds to diagram below.



Set the leading edge of the first A phase clock on the first division on the scope screen.

Attach channel 2 probe to pin 5D26A1 in memory to be aligned.

Adjust the top potentiometer on the M8562 or M8565 in slot 1 of the memory so that the leading edge 50% point crosses the leading edge 50% point of MBox A phase clock.

Connect channel 2 probe to pin 5D26K1 in the memory to be aligned.

Adjust the bottom potentiometer on the M8562 or M8565 in slot 1 of the memory so that the leading edge 50% point crosses the leading edge 50% point of MBox B phase clock.

Connect channel 2 probe to pin 5D29A1 in the memory to be aligned.

Perform the A phase alignment described above. Adjust the top potentiometer of the M8562 or M8565 in slot 54.

Connect channel 2 probe to pin 5D29K1 in the memory to be aligned.

Perform the B phase alignment described above. Adjust the bottom potentiometer of the M8562 or M8565 in slot 54. This completes the adjustments for one MA20 or MB20 unit.

For additional memory boxes the procedure is identical.

DMA20 CLOCK DESKEW PROCEDURE

EQUIPMENT REQUIRED

Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

OBJECTIVE

To assure performing clock deskew procedure type MR and then type FX1 to turn on the clock. Do not check deskew under a running program.

NOTES

Before performing clock deskew procedure type MR and then type FX1 to turn on the clock. Do not check deskew under a running program

ADJUSTMENT PROCEDURE

Attach a probe (either external sync or channel 3) to A CHANGE COMING L, 4E22F2. Set sync for negative edge.

Attach channel 1 probe to MTR MBOX CLOCK, 4D33P1. Use 0.5 V/CM and set scope such that the ground reference is 1.3 V above the centerline.

Attach channel 2 probe to DMC2 CLK DESKEW POINT, 1A02R2. Use 0.5 V/CM and adjust scope such that the ground reference is 1.5 V below the centerline.

The positive MBox clock pulse which occurs after A CHANGE COMING L goes low is the A phase clock. The second clock tick after the A phase clock tick is the B phase clock tick. The second clock tick after the B phase clock tick is another A phase clock tick, etc.

Adjust DL2 on the M8560 in slot 1AF03 (it is the 4th delay from the top) until the leading edge of the clock on channel 2 which is affected by this adjustment crosses the centerline at the same time as the leading edge of A phase MBox clock on channel 1.

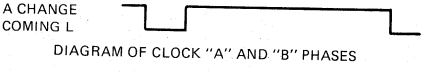


DIAGRAM OF CLOCK "A" AND "B" PHASES

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Adjust DL3 on the M8560 in slot 1AF03 (it is the top delay) until the leading edge of the clock which is affected by this adjustment crosses the centerline at the same time as the leading edge of B phase MBox clock on channel 1.

Connect channel 2 to DTR3 CLK 125 NS A H, 1D03F1.

Adjust DL1 on the M8560 in slot 1AF03 (it is the bottom delay) until the leading edge of the clock on channel 2 which is affected by this adjustment crosses the centerline at the same time as the leading edge of A phase MBox clock on channel 1.

Connect channel 2 to DTR3 CLK 62 NS A H, 1D03L2.

Adjust DL4 on the M8560 in slot 1AF03 (it is the 2nd delay from the top) until the leading edge of the clock which is affected by this delay crosses the centerline at the same time as the leading edge of A phase MBox clock on channel 1.

Adjust DL5 on the M8560 in slot 1AF03 (it is the 3rd delay from the top) until the leading edge of the clock which is affected by this delay crosses the centerline at the same time as the leading edge of B phase MBox clock on channel 1.

This completes the adjustment of the DMA20 clock.

DMA20 DATA WARNING ADJ

EQUIPMENT REQUIRED

Tektronics 475 or equivalent (100 MHz) scope with identical probes and short ground clips.

OBJECTIVE

The KL10 use DATA WARN as well as READ RESTART for memory reads. This procedure assures correct alignment of these pulses.

NOTES

This procedure should be done in 4-Bus Mode, assuming the system has multiples of 4 memories. This general procedure will, however, work in any bus mode.

The memory must be set up to return DATA WARNING SLOW and ADDRESS ACK (NT) only. No other combination is legal!

ADJUSTMENT PROCEDURE

Set up the DMA20 in 4-Bus Mode doing a small loop which reads from only one memory on a given bus, such as:

```
10/ MOVE 0, 100 (200000 100)
11/ MOVE 0, 101 (200000 101)
12/ MOVE 0, 102 (200000 102)
13/ MOVE 0, 103 (200000 103)
14/ JRST  10    (254000 10)
```

Put channel 1 probe on KBus n DATA WARNING.

KBus 0	1C05D1
KBus 1	1C07D1
KBus 2	1C09D1
KBus 3	1C11D1

Put channel 2 probe on KBus n RD RS.

KBus 0	1C05J1
KBus 1	1C07J1
KBus 2	1C09J1
KBus 3	1C11J1

Sync on channel 1 going negative.

Adjust each memory such that DATA WARNING (on channel 1) occurs (MG10s 260 $\pm$5) MH10s 295 $\pm$5) nanoseconds prior to RD RS (on channel 2). This adjustment is done in the memory. Refer to the memory print set for delay locations for the specific type of memory being adjusted.

If more than four memory controllers are to be adjusted, deselect the memories just adjusted and select the next boxes as low core. Rerun the program and adjust the next memories.

Adjust the appropriate M8591 for the port - top delay potentiometer.

MG10/MH10

Port	Loc
0	KL39
1	KL32
2	KL38
3	KL31
4	KL37
5	KL30
6	KL36
7	KL29

PNEUMATIC ADJUSTMENTS

THREAD MODE
ALL MODELS

ITEM	V/P	TUBE COLOR	EASY LOAD
LOWER RESTRAINT	P	10 RED	10" - 12"
UPPER RESTRAINT	P	10 BLUE	16" - 20"
RT THD CHAN	P	10 YELLOW	30"
RT THD CHAN	V	10 PURPLE	5" - 6"
LT THD CHAN	P	6 YELLOW	30"
AIR JET	P	6 BLUE	15" - 17"
VACUUM REEL	V	6 RED	19" - 21"

RUN MODE TU70

ITEM	V/P	TUBE COLOR	TU70
COLUMNS	V	6 PURPLE	34" - 35"
RT UPPER AIR BEARING	P	10 PINK	48" - 53"
RT GUIDE	P	10 GREEN	44" - 48"
LT GUIDE	P	10 BROWN	40" - 60"
RT LOWER AIR BEARING	P	10 CLEAR	48" - 53"
LT LOWER AIR BEARING	P	6 GREEN	40" - 42"
TAPE CLEANER BLOCK	V	10 BLACK	5" - 8" — ADJUST SO THAT TAPE SEALS TO CLEANER BLOCK WITH MINIMUM VACUUM.

RUN MODE TU72

ITEM	V/P	TUBE COLOR	TU72
COLUMNS	V	6 PURPLE	33" - 35"
RT UPPER AIR BRNG	P	10 PINK	48" - 53"
RT LOWER AIR BRNG	P	10 CLEAR	48" - 53"
RT GUIDE	P	10 GREEN	60" - 70"
LT GUIDE	P	10 BROWN	0
LT LOWER AIR BRNG	P	6 GREEN	40" - 42"
CAPSTAN	V	6 PINK	15" - 19"
TAPE CLEANER BLOCK	V	10 BLACK	5" - 6" — ADJUST FOR TAPE SEAL AT MINIMUM VACUUM

MF20/MG20 CLOCK DESKEW PROCEDURE

The following equipment is required.

1. Oscilloscope - Tektronix 475 or equivalent
2. W9025, 12-inch extender module
3. Alignment tool

Clock Check Procedure

NOTE

This is not a deskew procedure. If the requirements of this check are not satisfied, the deskew must be performed as described in the Clock Deskew Procedure below.

1. Set oscilloscope to 1V/div for both channel 1 and channel 2. Set sweep rate to 20 ns/div. Load the KL10 microcode. Select full clock rate and source the clock from the master oscillator at 30 MHz. Start the microcode (CR0, FW72/3, CS2, SM).

2. Place probe 1 on pin E22F2 in the CPU bay (signal A CHANGE COMING L) and place the clip on a ground pin. Place probe 2 on pin D5D1 in MF20/MG20 (signal CTL2 A PHS COM FREE L) and place the clip on a ground pin. Sync internal on channel 1. These signals must be identical.

3. Move probe 1 from CPU bay to MF20/MG20 at pin C5M2 (signal CTL2 B PHS COM FREE L) and place the clip on a ground pin. Set the oscilloscope to add channel 1 with channel 2. The waveform observed must be perfectly symmetrical with respect to ON/OFF time.

Clock Deskew Procedure

1. Power down the MF20/MG20 and place the M8576 on the extender. Rotate the two switches all the way clockwise. Restore power and load the KL10 microcode, master reset the machine (MR), select full clock rate (CR0), and source the clock from the master oscillator at 30 MHz. Now start the microcode (SM).

2. Place the probe for the viewable external sync on pin E22F2 in CPU bay (signal A CHANGE COMING L) and place the ground clip on a ground pin.

3. Select negative external sync as a trigger on oscilloscope.

4. Put the dip clip on E86 of the M8576 and place probe 2 on E86 pin 5 (CT A CLK DLY L). Place the ground clip on pin 1.

5. Place probe 1 on E86 pin 9 of the M8576 (CLK FREE) and ground clip on pin 16.

6. View external sync and locate A phase tick of CLK FREE (probe 1). It is the first positive-going pulse after the CPU signal A CHANGE COMING L goes low.

7. Having located the A tick of CLK FREE, define the positive pulse before A tick to be X tick. Define the positive pulse before X tick to be Y tick.

8. Rotate the bottom switch to align the negative-going edge of CT A CLK DLY L (probe 2) with the negative-going edge of Y tick (probe 1). If this optimal setting is not possible, the negative-going edge of CT A CLK DLY L must be aligned within the following range: after the positive-going edge of Y tick and before the positive-going edge of X tick.

9. Move probe 2 from E86 pin 5 to E86 pin 6. Rotate the upper switch to align the negative-going edge of CT B CLK DLY L (probe 2) with the negative-going edge of A tick (probe 1). If this optimal setting is not possible, the negative-going edge of CT B CLK DLY L must be aligned within the following range: after the positive-going edge of A tick and before the positive-going edge of the pulse following A tick.

10. Semi-Final check - Remove probe 1 from pin 9 of E86 and place it on pin 5. The waveforms observed on channels 1 and 2 should be logically opposite to each other.

11. Final Check - At the scope, move the probe monitoring A CHANGE COMING L from the EXT SYNC to CHANNEL 1. Sync internal on channel 1. Now remove the probes attached to the dip clip and place the dip clip on E61. Put channel 2 probe on E61 pin 2 (signal A PHS COM FREE 1 L in MF20/MG20) and place the ground clip on E61 pin 16. These signals should be identical.

MF20/MG20 JUMPERS

	Pin to Ground Connections		
No.	A4L1	A4M1	A4N1
10	NC	NC	NC
11	NC	NC	GND
12	NC	GND	NC
13	NC	GND	GND

KL10 TROUBLESHOOTING FLOWCHARTS

INTRODUCTION

These flowcharts were produced to help guide the Field Service engineer. It shows the steps that should be performed to debug a KL10-based system that is experiencing intermittent crashes.

In order to isolate the failing Field Replaceable Unit (FRU) which is causing an intermittent error, two basic steps must be taken. They are data collection, and decoding of this data. These flowcharts describe a logical sequence of steps that can be followed to collect and decode data.

Data Collection

Data collection portions of the flowcharts deal with how to go about gathering as much information as possible about the error. Due to the nature of intermittent errors, it is best to collect data from a number of related crashes. It is important to collect the information in a logical sequence.

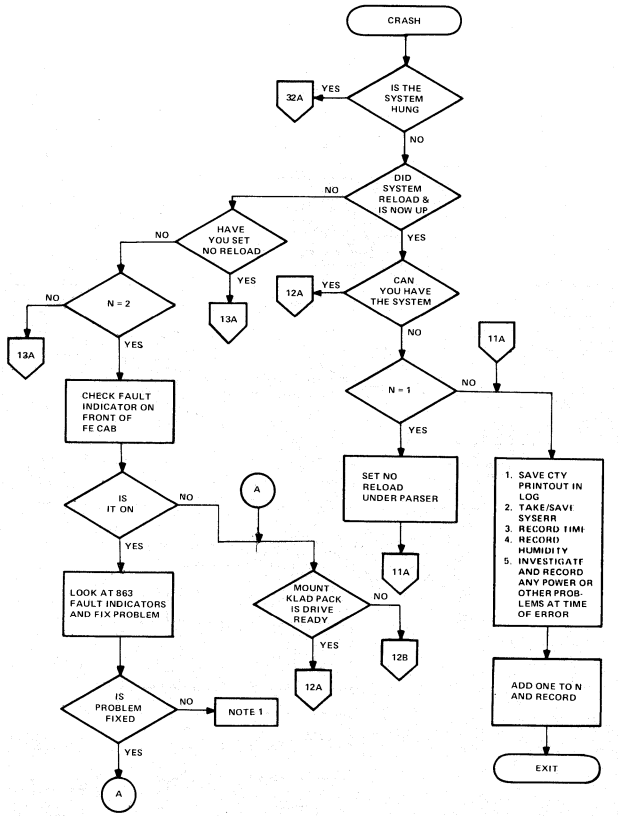
In this portion of the flow you will find many references to (N). This symbol is equal to the number of crashes the system has experienced. Whenever a call has been closed, (N) is reset to zero. (A closed call means everyone involved - DEC Service, management, and the customer - perceive that the particular problem which initiated the call has been solved.) This ensures that data collected for a new problem is not confused with data previously collected for old unrelated errors.

All data collected should be logged into the Site Management Guide. This ensures that the data is readily available to anyone who needs to use it. It is assumed that the engineer will solve any hard-down situation that may occur during data collection, using his or her expertise and available tools such as diagnostics and this manual (the KL10 Maintenance Guide).

Decoding of Data

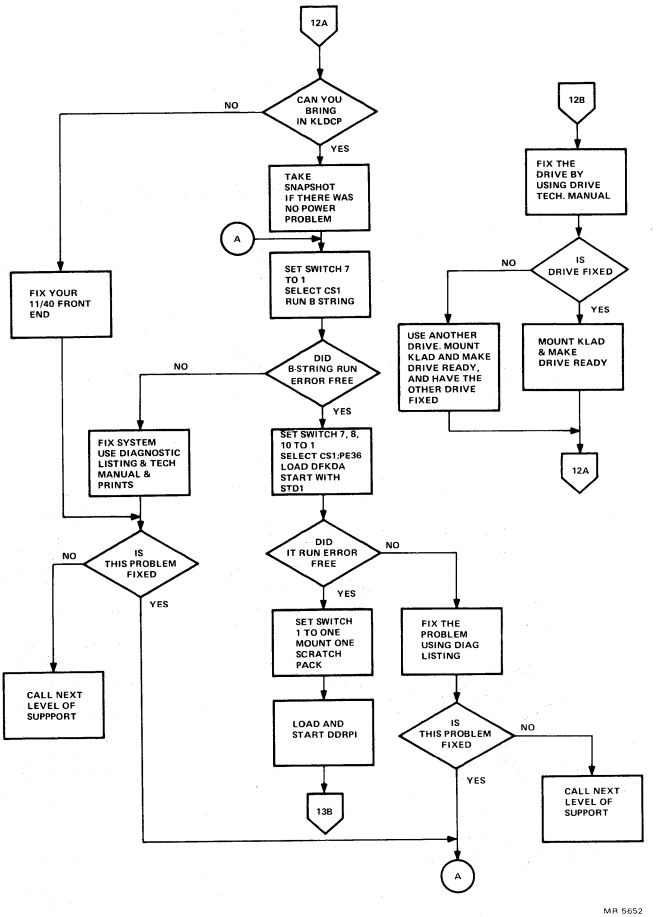
This portion of the flow uses the "tables", "maps", and "general information" sections of this manual. Data that has been collected from crashes is interpreted and acted upon. FRU selection is done where possible.

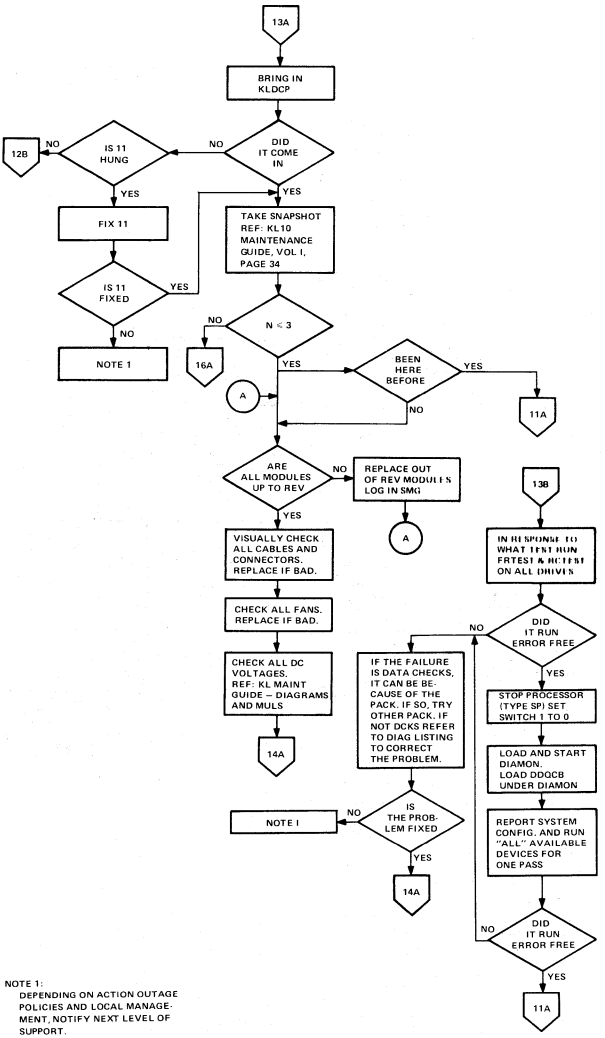
There will be times when escalation of a problem is needed. This is reflected in NOTE 1 of the flow. This note pertains to support escalation as it is now defined in the Action Outage policy.



NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

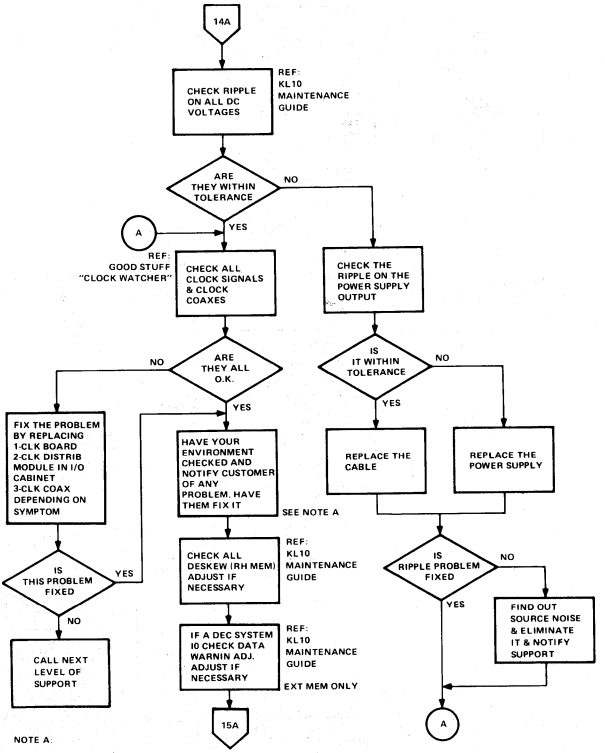
MR 5651

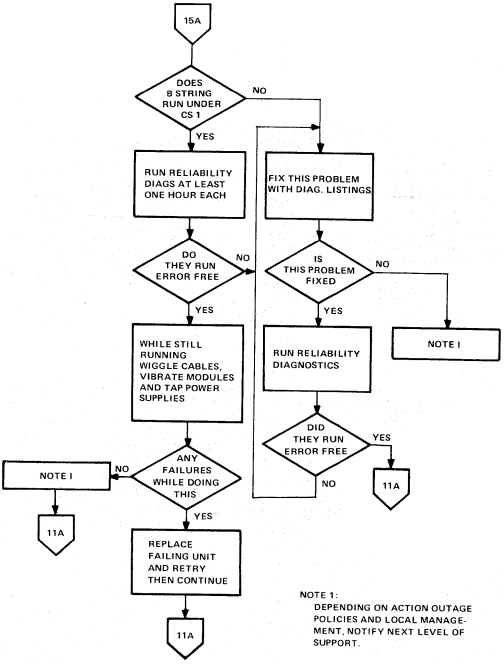

12A
CAN YOU BRING IN KLDCP
NO
YES
TAKE SNAPSHOT IF THERE WAS NO POWER PROBLEM
A
SET SWITCH 7 TO 1 SELECT CS1 RUN B STRING
FIX YOUR 11/40 FRONT END
DID B-STRING RUN ERROR FREE
NO
YES
FIX SYSTEM USE DIAGNOSTIC LISTING & TECH MANUAL & PRINTS
SET SWITCH 7, 8, 10 TO 1 SELECT CS1;PE36 LOAD DFKDA START WITH STD1
IS THIS PROBLEM FIXED
NO
YES
CALL NEXT LEVEL OF SUPPPORT
DID IT RUN ERROR FREE
NO
YES
SET SWITCH 1 TO ONE MOUNT ONE SCRATCH PACK
LOAD AND START DDRPI
13B
FIX THE PROBLEM USING DIAG LISTING
IS THIS PROBLEM FIXED
NO
YES
CALL NEXT LEVEL OF SUPPORT
A
12B
FIX THE DRIVE BY USING DRIVE TECH. MANUAL
IS DRIVE FIXED
NO
YES
USE ANOTHER DRIVE. MOUNT KLAD AND MAKE DRIVE READY, AND HAVE THE OTHER DRIVE FIXED
MOUNT KLAD & MAKE DRIVE READY
12A
MR 5652

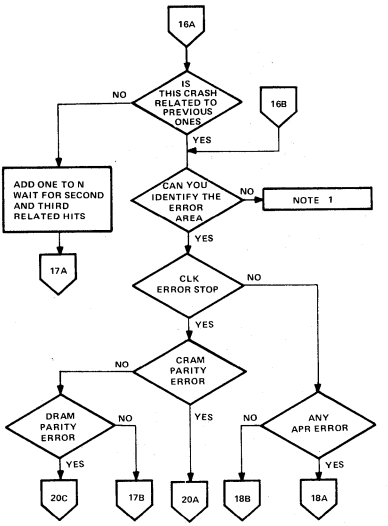


NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGE-MENT, NOTIFY NEXT LEVEL OF SUPPORT.

MR-5653

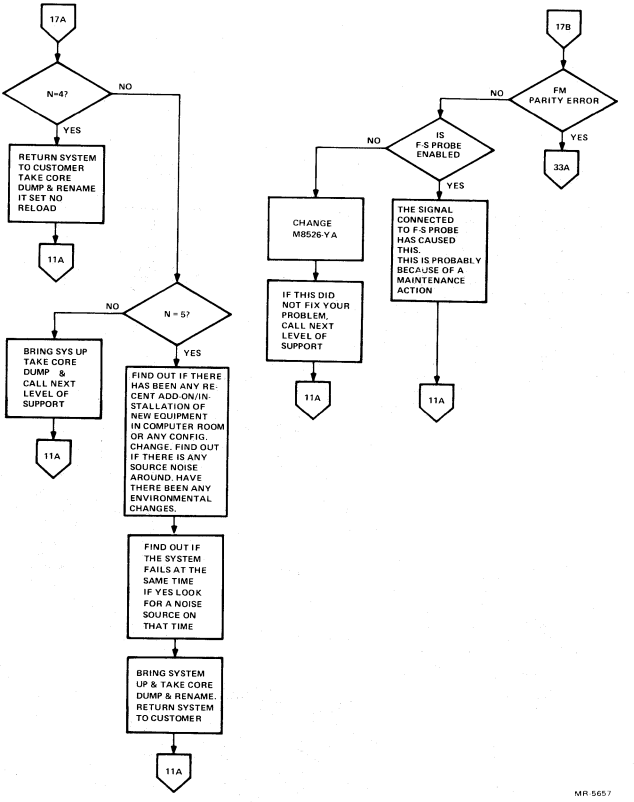

14A
CHECK RIPPLE ON ALL DC VOLTAGES
REF: KL10 MAINTENANCE GUIDE
ARE THEY WITHIN TOLERANCE
NO
YES
A
REF: GOOD STUFF "CLOCK WATCHER"
CHECK ALL CLOCK SIGNALS & CLOCK COAXES
CHECK THE RIPPLE ON THE POWER SUPPLY OUTPUT
ARE THEY ALL O.K.
NO
YES
IS IT WITHIN TOLERANCE
NO
YES
FIX THE PROBLEM BY REPLACING 1-CLK BOARD 2-CLK DISTRIB MODULE IN I/O CABINET 3-CLK COAX DEPENDING ON SYMPTOM
HAVE YOUR ENVIRONMENT CHECKED AND NOTIFY CUSTOMER OF ANY PROBLEM. HAVE THEM FIX IT
SEE NOTE A
REPLACE THE CABLE
REPLACE THE POWER SUPPLY
IS THIS PROBLEM FIXED
YES
NO
CHECK ALL DESKEW (RH MEM) ADJUST IF NECESSARY
REF: KL10 MAINTENANCE GUIDE
IS RIPPLE PROBLEM FIXED
NO
YES
FIND OUT SOURCE NOISE & ELIMINATE IT & NOTIFY SUPPORT
CALL NEXT LEVEL OF SUPPORT
IF A DEC SYSTEM 10 CHECK DATA WARNIN ADJ. ADJUST IF NECESSARY
REF: KL10 MAINTENANCE GUIDE
EXT MEM ONLY
15A
A
NOTE A:
1. HAVE ENVIRONMENT CHECKED (SOURCE PWR, TEMP, HUMIDITY)
2. NOTIFY THE CUSTOMER AND PROBLEM MANAGER OF THE RESULTS
3. CONTINUE
MR 5654

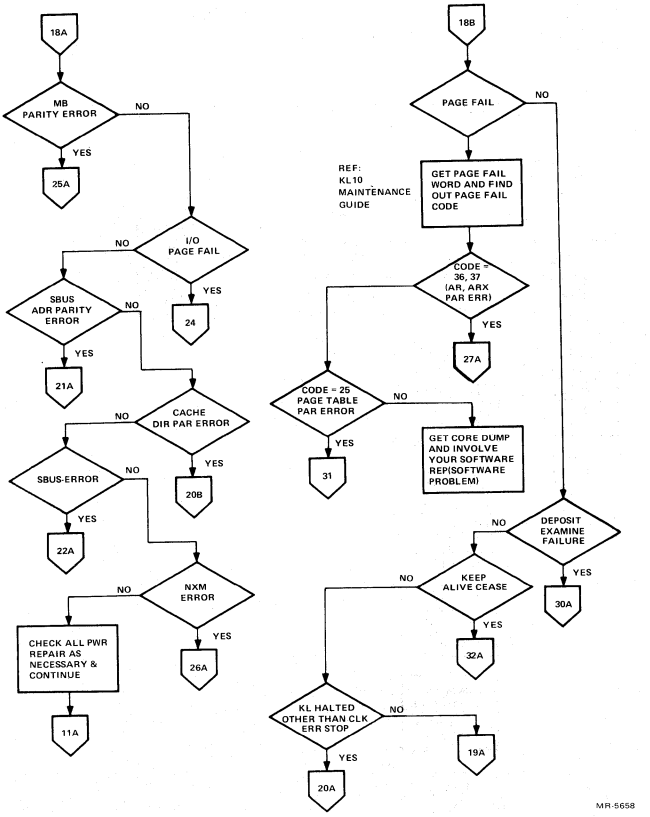

15A
DOES B STRING RUN UNDER CS 1
NO
YES
RUN RELIABILITY DIAGS AT LEAST ONE HOUR EACH
FIX THIS PROBLEM WITH DIAG. LISTINGS
DO THEY RUN ERROR FREE
NO
IS THIS PROBLEM FIXED
NO
YES
YES
WHILE STILL RUNNING WIGGLE CABLES, VIBRATE MODULES AND TAP POWER SUPPLIES
RUN RELIABILITY DIAGNOSTICS
NOTE 1
DID THEY RUN ERROR FREE
YES
NO
11A
ANY FAILURES WHILE DOING THIS
NO
NOTE 1
YES
11A
REPLACE FAILING UNIT AND RETRY THEN CONTINUE
11A
NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.
MR-5655

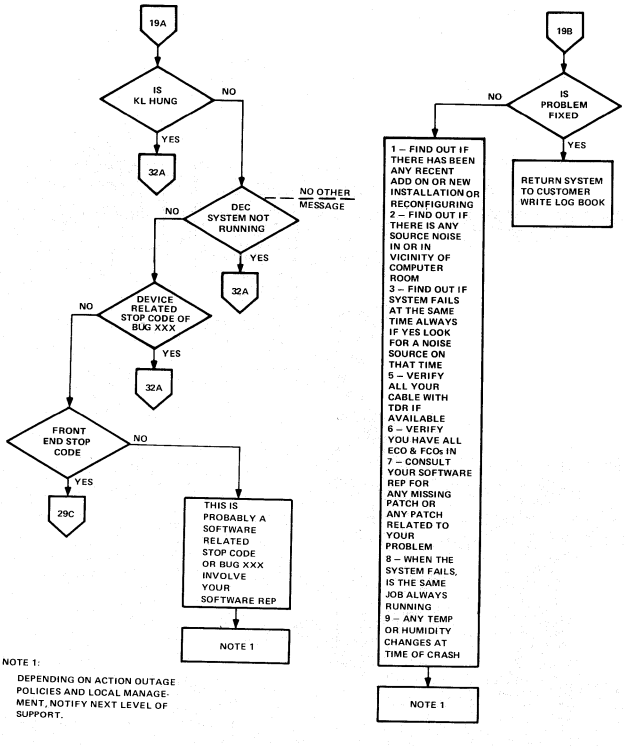


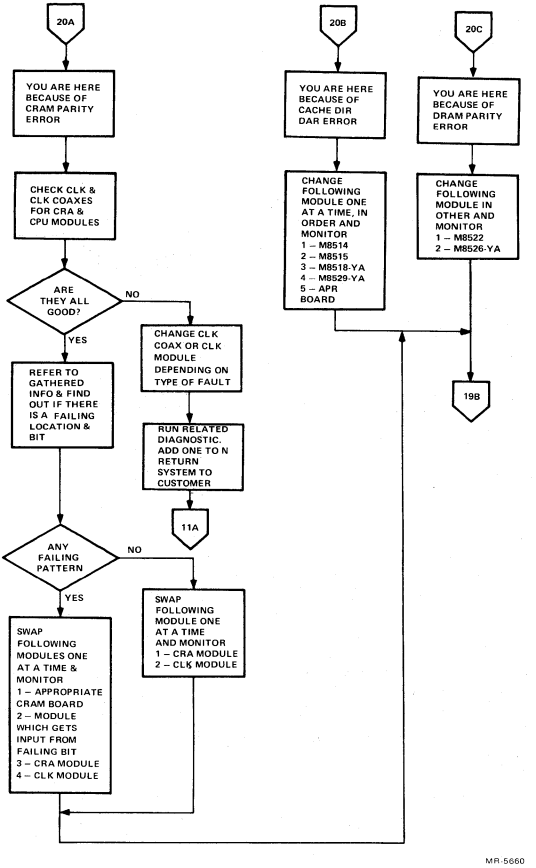
NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

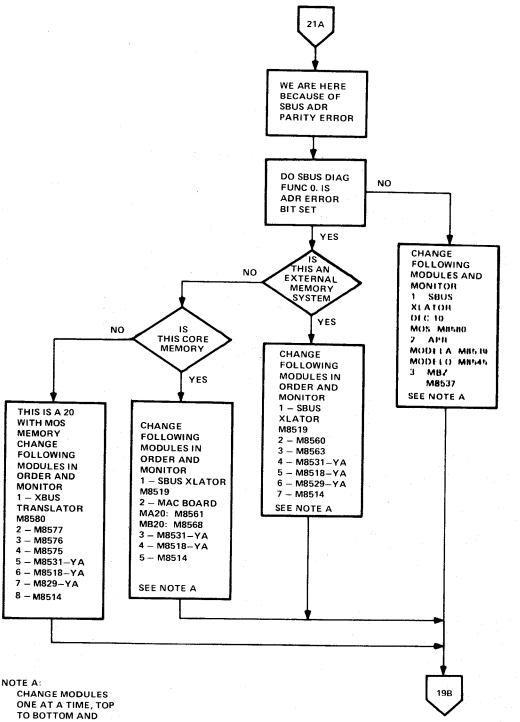
MR-5656

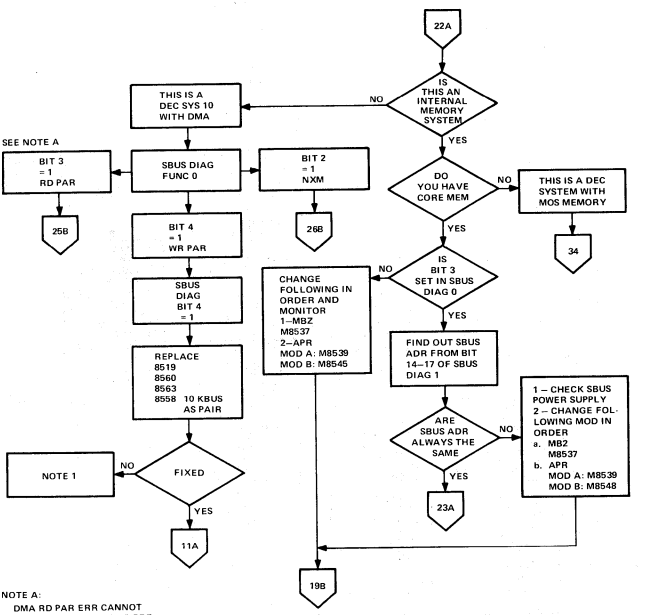

17A
N=4?
NO
YES
RETURN SYSTEM TO CUSTOMER TAKE CORE DUMP & RENAME IT SET NO RELOAD
11A
N = 5?
NO
YES
BRING SYS UP TAKE CORE DUMP & CALL NEXT LEVEL OF SUPPORT
11A
FIND OUT IF THERE HAS BEEN ANY RECENT ADD-ON/INSTALLATION OF NEW EQUIPMENT IN COMPUTER ROOM OR ANY CONFIG. CHANGE. FIND OUT IF THERE IS ANY SOURCE NOISE AROUND. HAVE THERE BEEN ANY ENVIRONMENTAL CHANGES.
FIND OUT IF THE SYSTEM FAILS AT THE SAME TIME IF YES LOOK FOR A NOISE SOURCE ON THAT TIME
BRING SYSTEM UP & TAKE CORE DUMP & RENAME. RETURN SYSTEM TO CUSTOMER
11A
17B
FM PARITY ERROR
NO
YES
33A
IS F-S PROBE ENABLED
NO
YES
CHANGE M8526-YA
IF THIS DID NOT FIX YOUR PROBLEM, CALL NEXT LEVEL OF SUPPORT
11A
THE SIGNAL CONNECTED TO F-S PROBE HAS CAUSED THIS. THIS IS PROBABLY BECAUSE OF A MAINTENANCE ACTION
11A
MR-5657


18A
MB PARITY ERROR
NO
YES
25A
I/O PAGE FAIL
NO
YES
24
SBUS ADR PARITY ERROR
NO
YES
21A
CACHE DIR PAR ERROR
NO
YES
20B
SBUS-ERROR
NO
YES
22A
NXM ERROR
NO
YES
26A
CHECK ALL PWR REPAIR AS NECESSARY & CONTINUE
11A
18B
PAGE FAIL
NO
REF: KL10 MAINTENANCE GUIDE
GET PAGE FAIL WORD AND FIND OUT PAGE FAIL CODE
CODE = 36, 37 (AR, ARX PAR ERR)
YES
27A
CODE = 25 PAGE TABLE PAR ERROR
NO
YES
31
GET CORE DUMP AND INVOLVE YOUR SOFTWARE REP(SOFTWARE PROBLEM)
DEPOSIT EXAMINE FAILURE
NO
YES
30A
KEEP ALIVE CEASE
NO
YES
32A
KL HALTED OTHER THAN CLK ERR STOP
NO
YES
19A
20A
MR-5658


19A
IS KL HUNG
NO
YES
32A
NO OTHER MESSAGE
DEC SYSTEM NOT RUNNING
NO
YES
32A
DEVICE RELATED STOP CODE OF BUG XXX
NO
YES
32A
FRONT END STOP CODE
NO
YES
29C
THIS IS PROBABLY A SOFTWARE RELATED STOP CODE OR BUG XXX INVOLVE YOUR SOFTWARE REP
NOTE 1
NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.
19B
IS PROBLEM FIXED
NO
YES
RETURN SYSTEM TO CUSTOMER WRITE LOG BOOK
1 – FIND OUT IF THERE HAS BEEN ANY RECENT ADD ON OR NEW INSTALLATION OR RECONFIGURING
2 – FIND OUT IF THERE IS ANY SOURCE NOISE IN OR IN VICINITY OF COMPUTER ROOM
3 – FIND OUT IF SYSTEM FAILS AT THE SAME TIME ALWAYS IF YES LOOK FOR A NOISE SOURCE ON THAT TIME
5 – VERIFY ALL YOUR CABLE WITH TDR IF AVAILABLE
6 – VERIFY YOU HAVE ALL ECO & FCOs IN
7 – CONSULT YOUR SOFTWARE REP FOR ANY MISSING PATCH OR ANY PATCH RELATED TO YOUR PROBLEM
8 – WHEN THE SYSTEM FAILS, IS THE SAME JOB ALWAYS RUNNING
9 – ANY TEMP OR HUMIDITY CHANGES AT TIME OF CRASH
NOTE 1
MR-5659


20A
YOU ARE HERE BECAUSE OF CRAM PARITY ERROR
CHECK CLK & CLK COAXES FOR CRA & CPU MODULES
ARE THEY ALL GOOD?
NO
YES
CHANGE CLK COAX OR CLK MODULE DEPENDING ON TYPE OF FAULT
REFER TO GATHERED INFO & FIND OUT IF THERE IS A FAILING LOCATION & BIT
RUN RELATED DIAGNOSTIC. ADD ONE TO N RETURN SYSTEM TO CUSTOMER
11A
ANY FAILING PATTERN
NO
YES
SWAP FOLLOWING MODULES ONE AT A TIME & MONITOR
1 – APPROPRIATE CRAM BOARD
2 – MODULE WHICH GETS INPUT FROM FAILING BIT
3 – CRA MODULE
4 – CLK MODULE
SWAP FOLLOWING MODULE ONE AT A TIME AND MONITOR
1 – CRA MODULE
2 – CLK MODULE
20B
YOU ARE HERE BECAUSE OF CACHE DIR DAR ERROR
CHANGE FOLLOWING MODULE ONE AT A TIME, IN ORDER AND MONITOR
1 – M8514
2 – M8515
3 – M8518-YA
4 – M8529-YA
5 – APR BOARD
20C
YOU ARE HERE BECAUSE OF DRAM PARITY ERROR
CHANGE FOLLOWING MODULE IN OTHER AND MONITOR
1 – M8522
2 – M8526-YA
19B
MR-5660

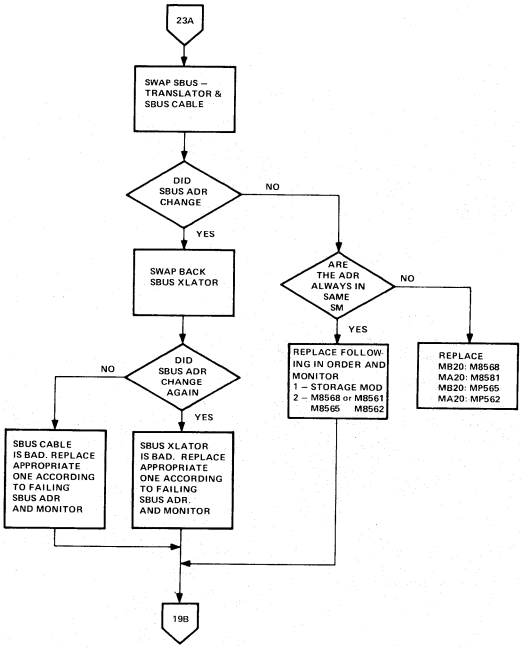

21A
WE ARE HERE BECAUSE OF SBUS ADR PARITY ERROR
DO SBUS DIAG FUNC 0. IS ADR ERROR BIT SET
NO
YES
CHANGE FOLLOWING MODULES AND MONITOR
1 SBUS XLATOR
DEC 10
MOS M8580
2 APR
MODEL A M8510
MODEL C M8545
3 MBX
M8537
SEE NOTE A
IS THIS AN EXTERNAL MEMORY SYSTEM
NO
YES
IS THIS CORE MEMORY
NO
YES
THIS IS A 20 WITH MOS MEMORY CHANGE FOLLOWING MODULES IN ORDER AND MONITOR
1 – XBUS TRANSLATOR M8580
2 – M8577
3 – M8576
4 – M8575
5 – M8531–YA
6 – M8518–YA
7 – M829–YA
8 – M8514
CHANGE FOLLOWING MODULES IN ORDER AND MONITOR
1 – SBUS XLATOR M8519
2 – MAC BOARD MA20: M8561 M820: M8568
3 – M8531–YA
4 – M8518–YA
5 – M8514
SEE NOTE A
CHANGE FOLLOWING MODULES IN ORDER AND MONITOR
1 – SBUS XLATOR M8519
2 – M8560
3 – M8563
4 – M8531–YA
5 – M8518–YA
6 – M8529–YA
7 – M8514
SEE NOTE A
19B
NOTE A:
CHANGE MODULES ONE AT A TIME, TOP TO BOTTOM AND MONITOR.
MR 5661

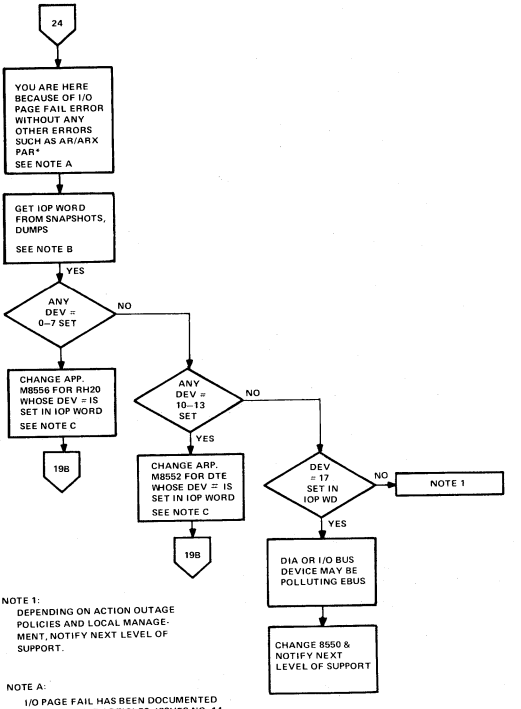


NOTE A:
DMA RD PAR ERR CANNOT EXIST WITHOUT MB PAR ERR IN APR UNLESS ERR DET IN DMA IS BROKE

NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

MR-5662


23A
SWAP SBUS – TRANSLATOR & SBUS CABLE
DID SBUS ADR CHANGE
NO
YES
SWAP BACK SBUS XLATOR
ARE THE ADR ALWAYS IN SAME SM
NO
YES
REPLACE FOLLOWING IN ORDER AND MONITOR
1 – STORAGE MOD
2 – M8568 or M8561
M8565 M8562
REPLACE
M820: M8568
MA20: M8581
M820: MP565
MA20: MP562
DID SBUS ADR CHANGE AGAIN
NO
YES
SBUS CABLE IS BAD. REPLACE APPROPRIATE ONE ACCORDING TO FAILING SBUS ADR AND MONITOR
SBUS XLATOR IS BAD. REPLACE APPROPRIATE ONE ACCORDING TO FAILING SBUS ADR AND MONITOR
19B
MR-5663



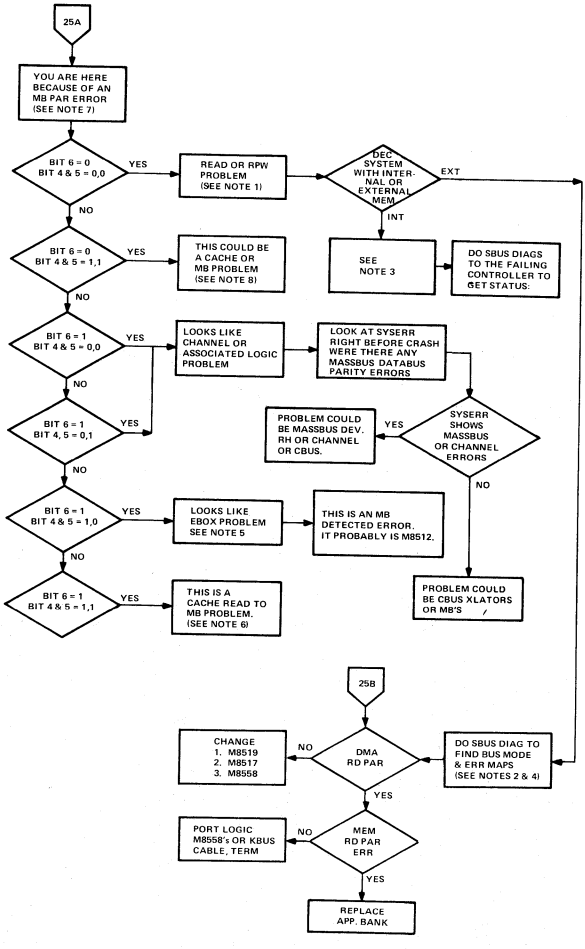
NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

NOTE A:
I/O PAGE FAIL HAS BEEN DOCUMENTED IN GOODSTUFF ARTICLES; ISSUES NO. 14, PAGE 9, AND ISSUE NO. 17, PAGE 7.

NOTE B:
THE DEV NUMBERS ARE DECODING FROM BITS 7–10 IN THE IOP WORD WHICH IS CONTAINED IN AC BLK 7, LOC 2. THE IOP WORD SHOULD BE VALID PROVIDING THAT BIT 10 IN FR 100 (PI ACTIVE) IS TRUE.

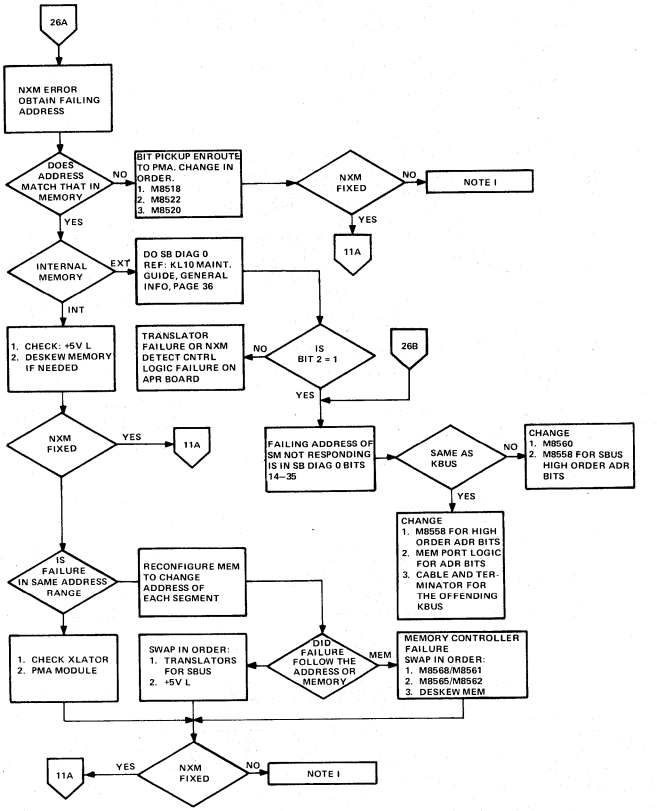
NOTE C:
THE CHANGING OF THESE CONTROL MODULES SHOULD ONLY BE DONE IF THE PREVIOUS SNAPSHOTS AND DUMPS AGREE WITH EACH OTHER ON THE DEV = PRESENT IN THE IOP WORD.

MR-5664



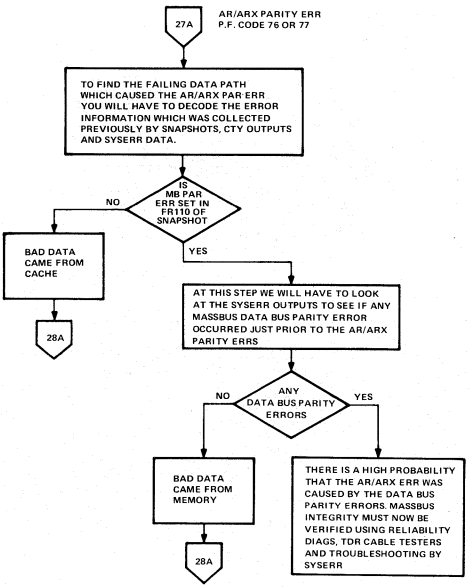
NOTES:

1. WITH THIS ERROR TAKE THE ERA WORD BITS 14:35 AND WORD NO. (BITS 0,1) AND FIGURE OUT THE FAILING REQUEST. THIS WILL HELP YOU FIGURE OUT WHICH REQUEST ON THE SBUS.
2. WITH THE REQUEST NO. AND BUS MODE YOU CAN FIGURE OUT WHICH KBUS HAS THE ERROR. ALSO CHECK ERROR LIGHTS IN THE EXTERNAL MEMORY FOR FURTHER HELP.
3. SINCE YOU HAVE THE FAILING REQUEST, GO TO THE INTERNAL MEMORY PRINTS TO POINT YOU TO THE APPROPRIATE STACK OR CONTROLLER WHICH CAUSED THE FAILURE. IF RANDOM MEM, REPLACE TRANSLATORS.
4. THE SBUS DIAG WILL TELL IF IT IS A READ OR WRITE PROBLEM. IF READ BIT IS NOT SET CHANCES ARE IT IS THE SBUS OR SBUS XLATOR BOARDS OR IF SET IT IS THE DMA, KBUS, OR MEMORY.
5. THIS IS AN EBOX STORE FROM AR.
6. THIS IS PROBABLY A CACHE OR MB BOARD PROBLEM (8521 OR 8517).
7. IN THIS FLOW ALL BITS TALKED ABOUT ARE FROM THE ERA WORD.
8. THIS IS A PAGE REFILL CYCLE OR CHANNEL READING FROM CACHE. CHANNEL READING FROM CACHE USES MB'S AS DATA PATH. THE MOST PROBABLE BOARDS ARE (8517s).



NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

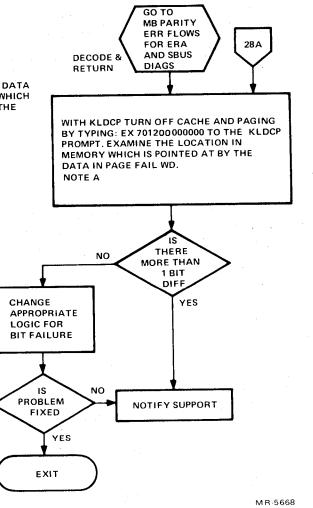
MR-5666


27A
AR/ARX PARITY ERR
P.F. CODE 76 OR 77
TO FIND THE FAILING DATA PATH WHICH CAUSED THE AR/ARX PAR ERR YOU WILL HAVE TO DECODE THE ERROR INFORMATION WHICH WAS COLLECTED PREVIOUSLY BY SNAPSHOTS, CTY OUTPUTS AND SYSERR DATA.
IS MB PAR ERR SET IN FR110 OF SNAPSHOT
NO
YES
BAD DATA CAME FROM CACHE
28A
AT THIS STEP WE WILL HAVE TO LOOK AT THE SYSERR OUTPUTS TO SEE IF ANY MASSBUS DATA BUS PARITY ERROR OCCURRED JUST PRIOR TO THE AR/ARX PARITY ERRS
ANY DATA BUS PARITY ERRORS
NO
YES
BAD DATA CAME FROM MEMORY
28A
THERE IS A HIGH PROBABILITY THAT THE AR/ARX ERR WAS CAUSED BY THE DATA BUS PARITY ERRORS. MASSBUS INTEGRITY MUST NOW BE VERIFIED USING RELIABILITY DIAGS, TDR CABLE TESTERS AND TROUBLESHOOTING BY SYSERR
MR 5667

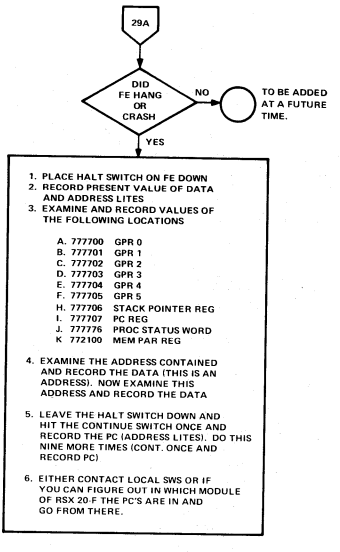
NOTE A
TOPS10 & TOPS20 UCODE. STORE DIFFERENT VALUES INTO THE AC's.

TOPS10
AC BLK 7
LOC 0 = BAD ARR DATA
LOC 1 = BAD ARX DATA

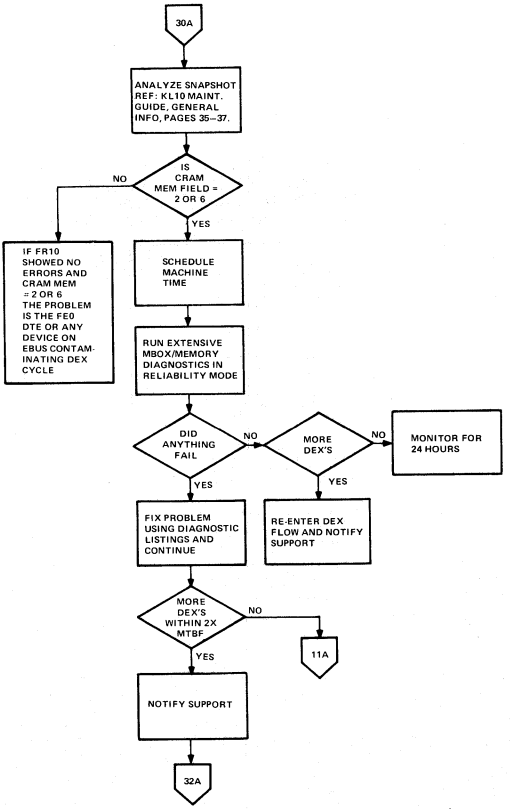
TOPS20
AC BLK 7
LOC 0 = BAD AR OR ARX DATA DEPENDING ON WHICH REGISTER HAD THE PARITY ERR

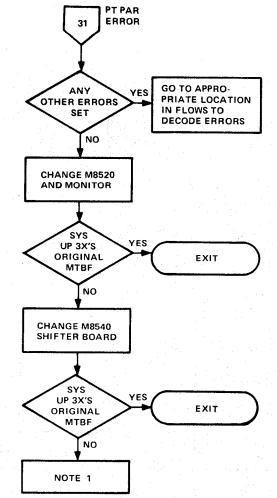


MR-5668


29A
DID FE HANG OR CRASH
NO
TO BE ADDED AT A FUTURE TIME.
YES
1. PLACE HALT SWITCH ON FE DOWN
2. RECORD PRESENT VALUE OF DATA AND ADDRESS LITES
3. EXAMINE AND RECORD VALUES OF THE FOLLOWING LOCATIONS
A. 777700 GPR 0
B. 777701 GPR 1
C. 777702 GPR 2
D. 777703 GPR 3
E. 777704 GPR 4
F. 777705 GPR 5
H. 777706 STACK POINTER REG
I. 777707 PC REG
J. 777776 PROC STATUS WORD
K 772100 MEM PAR REG
4. EXAMINE THE ADDRESS CONTAINED AND RECORD THE DATA (THIS IS AN ADDRESS). NOW EXAMINE THIS ADDRESS AND RECORD THE DATA
5. LEAVE THE HALT SWITCH DOWN AND HIT THE CONTINUE SWITCH ONCE AND RECORD THE PC (ADDRESS LITES). DO THIS NINE MORE TIMES (CONT. ONCE AND RECORD PC)
6. EITHER CONTACT LOCAL SWS OR IF YOU CAN FIGURE OUT IN WHICH MODULE OF RSX 20-F THE PC'S ARE IN AND GO FROM THERE.

MR-5669

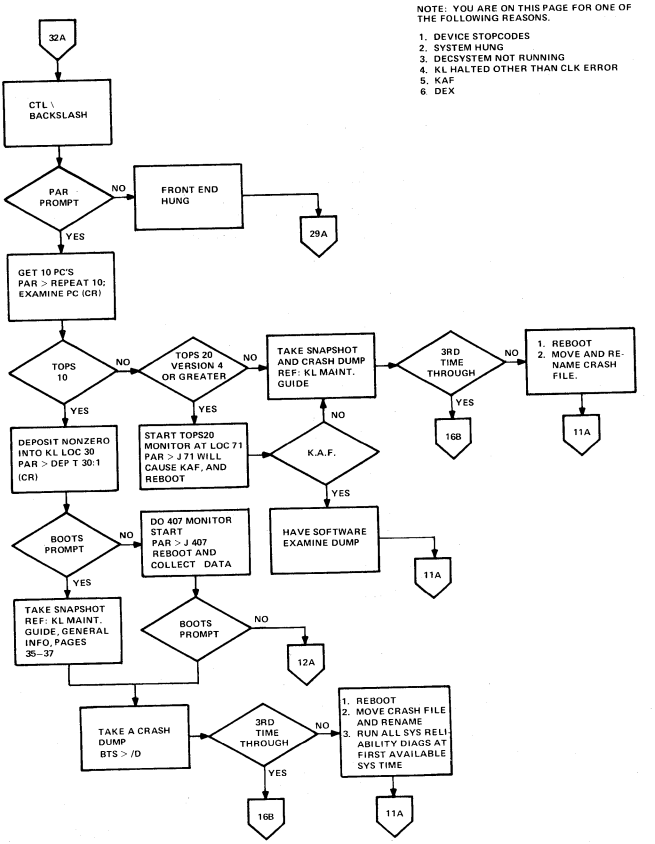

30A
ANALYZE SNAPSHOT REF: KL10 MAINT. GUIDE, GENERAL INFO, PAGES 35–37.
IS CRAM MEM FIELD = 2 OR 6
NO
YES
IF FR10 SHOWED NO ERRORS AND CRAM MEM = 2 OR 6 THE PROBLEM IS THE FE0 DTE OR ANY DEVICE ON EBUS CONTAMINATING DEX CYCLE
SCHEDULE MACHINE TIME
RUN EXTENSIVE MBOX/MEMORY DIAGNOSTICS IN RELIABILITY MODE
DID ANYTHING FAIL
NO
YES
MORE DEX'S
NO
YES
MONITOR FOR 24 HOURS
FIX PROBLEM USING DIAGNOSTIC LISTINGS AND CONTINUE
RE-ENTER DEX FLOW AND NOTIFY SUPPORT
MORE DEX'S WITHIN 2X MTBF
NO
YES
11A
NOTIFY SUPPORT
32A
MR-5670



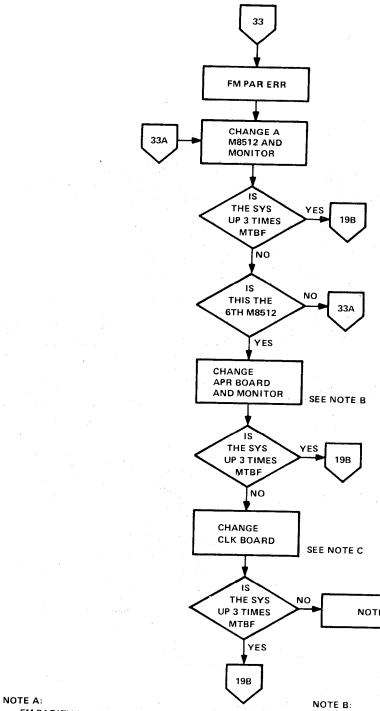
NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

MR 5671

TROUBLESHOOTING



MR 5672



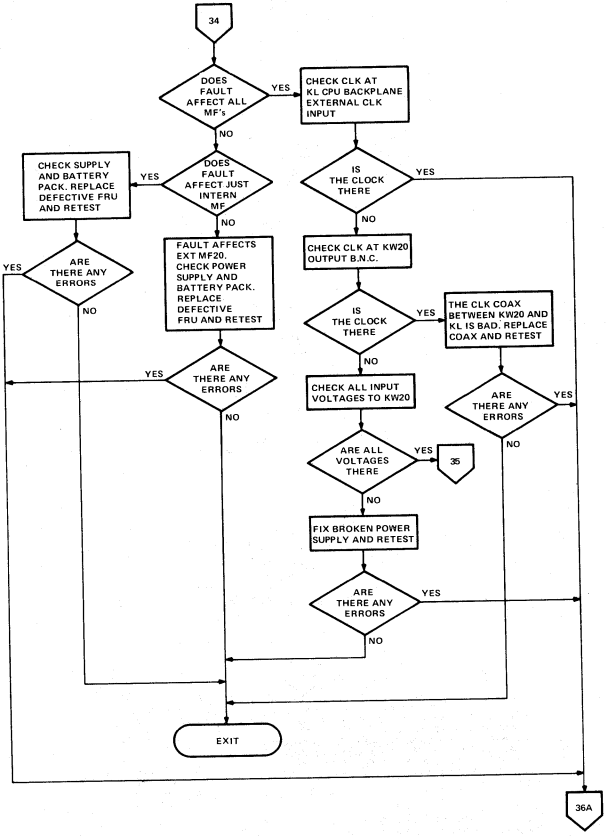
NOTE A:
FM PARITY ERRORS ARE SOME OF THE HARDEST ERRORS TO TROUBLESHOOT. WITH THE HELP OF LOGIC ANALYZERS AN ENGINEER WILL BE BETTER EQUIPPED TO DETERMINE THE CAUSE OF THE ERRORS. IT IS THEREFOR RECOMMENDED THAT A SUPPORT ENGINEER EXPERIENCED WITH LA'S ATTACK THIS TYPE OF ERROR IF YOU REACH THE NOTE 1 BOX IN THIS FLOW.

NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

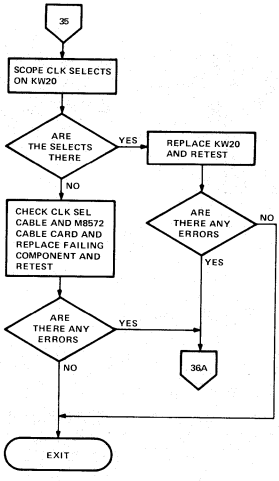
NOTE B:
REFERENCE MUL FOR PROPER CPU I.E. MODEL A, MODEL B

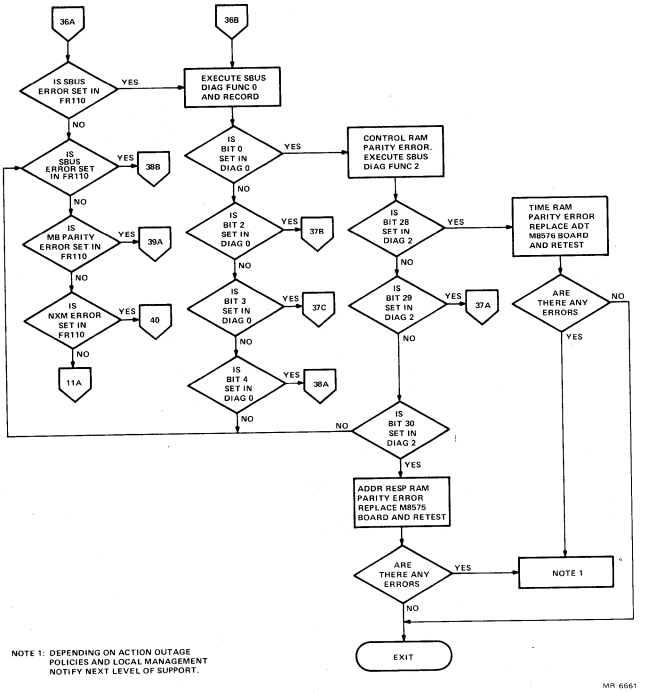
NOTE C:
SYS MUST BE DESKEWED AFTER THIS MODULE CHANGE

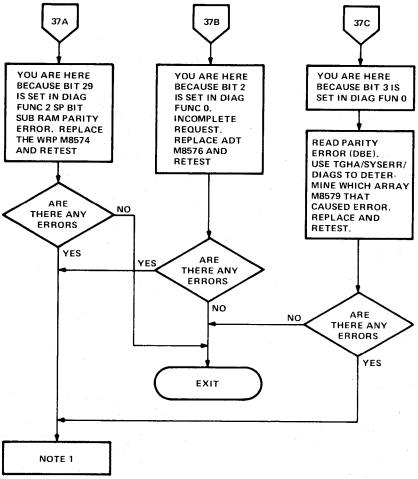
MR-5673


34
DOES FAULT AFFECT ALL MF's
YES
CHECK CLK AT KL CPU BACKPLANE EXTERNAL CLK INPUT
NO
CHECK SUPPLY AND BATTERY PACK. REPLACE DEFECTIVE FRU AND RETEST
YES
DOES FAULT AFFECT JUST INTERN MF
IS THE CLOCK THERE
YES
NO
FAULT AFFECTS EXT MF20. CHECK POWER SUPPLY AND BATTERY PACK. REPLACE DEFECTIVE FRU AND RETEST
CHECK CLK AT KW20 OUTPUT B.N.C.
YES
ARE THERE ANY ERRORS
NO
IS THE CLOCK THERE
YES
THE CLK COAX BETWEEN KW20 AND KL IS BAD. REPLACE COAX AND RETEST
NO
YES
ARE THERE ANY ERRORS
CHECK ALL INPUT VOLTAGES TO KW20
YES
ARE THERE ANY ERRORS
NO
ARE ALL VOLTAGES THERE
YES
35
NO
FIX BROKEN POWER SUPPLY AND RETEST
ARE THERE ANY ERRORS
YES
NO
EXIT
36A

MR-6659

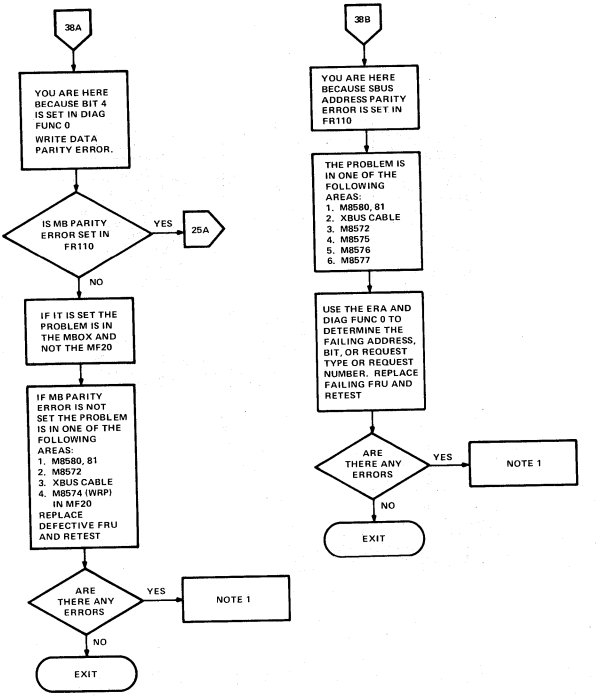

35
SCOPE CLK SELECTS ON KW20
ARE THE SELECTS THERE
YES
REPLACE KW20 AND RETEST
NO
CHECK CLK SEL CABLE AND M8572 CABLE CARD AND REPLACE FAILING COMPONENT AND RETEST
ARE THERE ANY ERRORS
NO
YES
ARE THERE ANY ERRORS
YES
NO
36A
EXIT
MR-6660


36A
36B
IS SBUS ERROR SET IN FR110
YES
EXECUTE SBUS DIAG FUNC 0 AND RECORD
NO
IS SBUS ERROR SET IN FR110
YES
38B
IS BIT 0 SET IN DIAG 0
YES
CONTROL RAM PARITY ERROR, EXECUTE SBUS DIAG FUNC 2
NO
IS MB PARITY ERROR SET IN FR110
YES
39A
IS BIT 2 SET IN DIAG 0
YES
37B
IS BIT 28 SET IN DIAG 2
YES
TIME RAM PARITY ERROR REPLACE ADT M8576 BOARD AND RETEST
NO
IS NXM ERROR SET IN FR110
YES
40
IS BIT 3 SET IN DIAG 0
YES
37C
IS BIT 29 SET IN DIAG 2
YES
37A
ARE THERE ANY ERRORS
NO
YES
NO
11A
IS BIT 4 SET IN DIAG 0
YES
38A
NO
IS BIT 30 SET IN DIAG 2
NO
YES
ADDR RESP RAM PARITY ERROR REPLACE M8575 BOARD AND RETEST
ARE THERE ANY ERRORS
YES
NOTE 1
NO
EXIT
NOTE 1: DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT NOTIFY NEXT LEVEL OF SUPPORT.
MR 6661



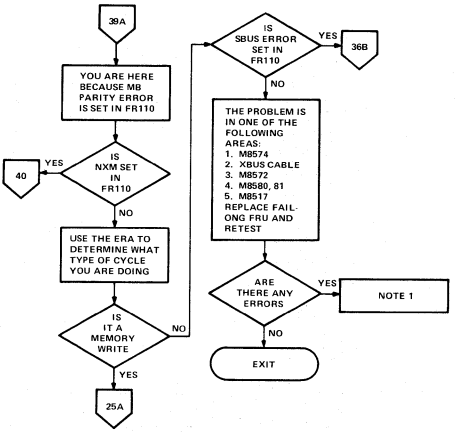
NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

MR-6662



NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

MR-6663



NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.

MR-6664

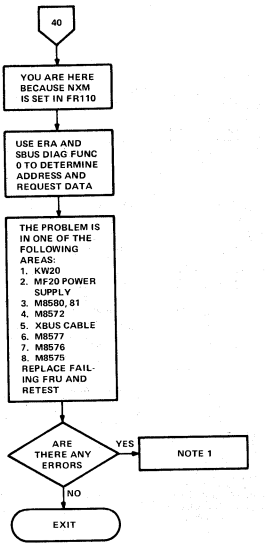

40
YOU ARE HERE BECAUSE NXM IS SET IN FR110
USE ERA AND SBUS DIAG FUNC 0 TO DETERMINE ADDRESS AND REQUEST DATA
THE PROBLEM IS IN ONE OF THE FOLLOWING AREAS:
1. KW20
2. MF20 POWER SUPPLY
3. M8580, 81
4. M8572
5. XBUS CABLE
6. M8577
7. M8576
8. M8575
REPLACE FAILING FRU AND RETEST
ARE THERE ANY ERRORS
YES
NOTE 1
NO
EXIT
NOTE 1:
DEPENDING ON ACTION OUTAGE POLICIES AND LOCAL MANAGEMENT, NOTIFY NEXT LEVEL OF SUPPORT.
MR-6665

Table of Contents

Notes for KL10 CPU Power Layout

1. PTn - U represents upper power tabs on CPU backplane.

2. PTn - L represents lower power tabs on CPU backplane.

3. PT tabs 5-U, 5-L, 6-U and 6-L are connected to the H7420 No. 2 in the I/O cabinet for +5 volt power.

4. The following power tabs are jumpered together.

   PT9U to PT11U PT9L to PT11L PT10U to PT12U PT10L to PT12L
   PT19U to PT21U PT19L to PT21L PT20U to PT22U PT20L to PT22L

5. STn represents sense tabs for remote sensing. Connections are from J2 and J3 of the H761 to the sense tabs, and from the sense tabs (via an etch) to the remote sensing pins on the backplane as indicated below.

   TWISTED PAIR FROM H761 (J2 AND J3) TO SENSE TABS

-5.2A	-SENSE - J2-2 TO ST17
	+SENSE - J2-1 TO ST16
-5.2B	-SENSE - J2-4 TO ST19
	+SENSE - J2-3 TO ST18
-5.2C	-SENSE - J2-6 TO ST1
	+SENSE - J2-5 TO PT15-U
-5.2D	-SENSE - J2-8 TO ST2
	+SENSE - J2-7 TO PT17-U
-5.2E	-SENSE - J2-10 TO ST13
	+SENSE - J2-9 TO PT17-L
-5.2F	-SENSE - J2-12 TO ST7
	+SENSE - J2-11 TO ST6
-5.2H	-SENSE - J2-14 TO ST5
	+SENSE - J2-13 TO ST4
-5.2J	-SENSE - J3-2 TO ST3
	+SENSE - J3-1 TO ST4
-5.2K	-SENSE - J3-4 TO ST10
	+SENSE - J3-3 TO ST11
-2A	-SENSE - J3-8 TO ST15
	+SENSE - J3-7 TO ST16
-2B	-SENSE - J3-10 TO ST14
	+SENSE - J3-9 TO PT15-L
-2C	-SENSE - J3-12 TO ST12
	+SENSE - J3-11 TO ST11
-2D	-SENSE - J3-14 TO ST8
	+SENSE - J3-13 TO ST9

   ETCH FROM SENSE TABS TO REMOTE SENSE PIN

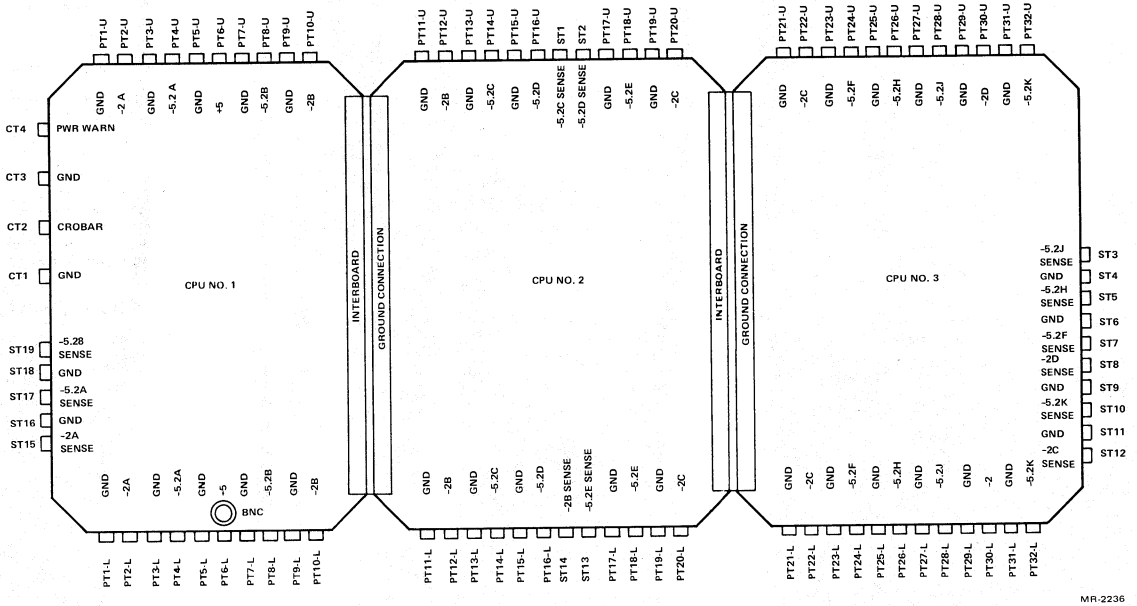
-5.2A	ST17 TO F8B2
-5.2B	ST19 TO F14B2
-5.2C	ST1 TO A21U1
-5.2D	ST2 TO A27U1
-5.2E	ST13 TO F33B2
-5.2F	ST7 TO A48U1
-5.2H	ST5 TO A45U1
-5.2J	ST3 TO A49U1
-5.2K	ST10 TO F53B2
-2A	ST15 TO F9B1
-2B	ST14 TO F21B1
-2C	ST12 TO F38B1
-2D	ST8 TO F48B1

6. The sense lines use the following color code.

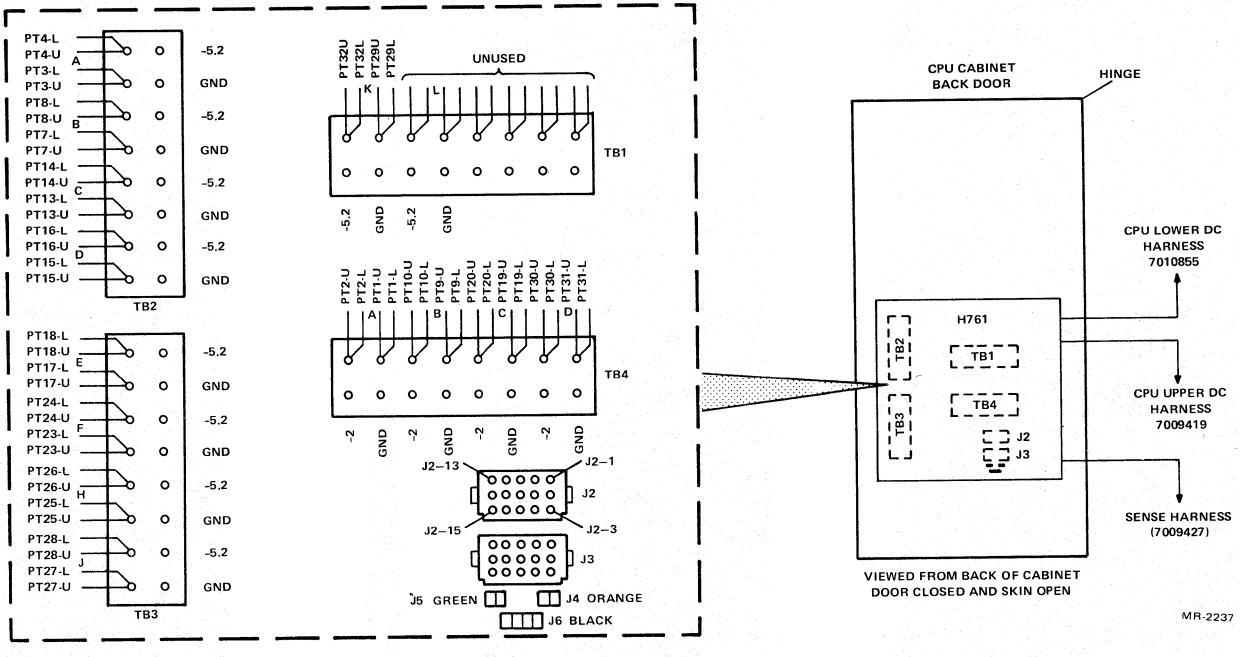
   BLACK = GND RED - +5 GREEN = -2.0 BLUE = -5.2

7. CTn represents control tabs. Connections are from the 863 power control to the control tabs, and from the control tabs (via an etch) to the following pins.

   POWER WARN CT4 to A04J1
   CROWAR CT2 to A06U2, B06S1, C02S1, C03S1, and F01U2.



KL10 CPU DC POWER (BACKPLANE)



Notes for KL10 I/O DC Power Layout

1. PTn - U represents upper power tabs on I/O backplane.

2. PTn - L represents lower power tabs on I/O backplane.

3. The following power tabs are jumpered together.

   PT7U to PT9U PT8U to PT10U PT7L to PT9L PT8L to PT10L
   PT5U to PT25U PT5L to PT25L PT6U to PT26U PT6L to PT26L

4. Pin block bus bars are used in the RH20 and DTE20 to distribute -5.0 V and in the DIA/DMA20 to distribute -15 V.

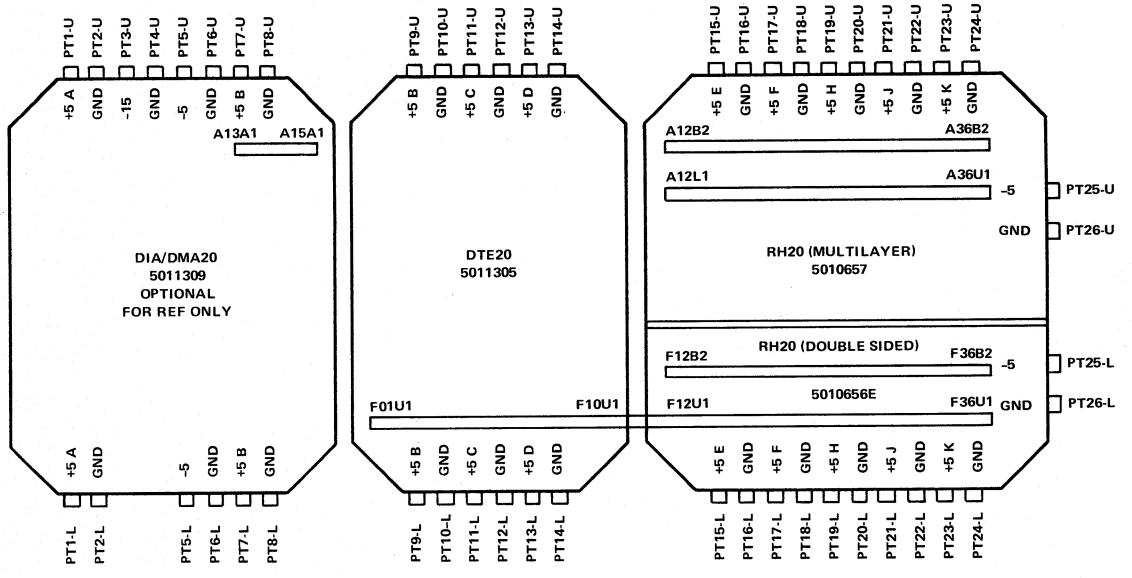
6. H7420 No. 2 (+5.0 L) supplies power tabs 5-U, 5L, 6U and 6L of the CPU backplane.

7. The +15 V regulator (H770) supplies the air flow sensors and voltage monitors in the KL10 system and the master oscillator (KW20).

8. The following color code is applicable.

   BLACK = GND GREEN = -5 ORANGE = +15
   RED = +5 BLUE = -15

NOTES



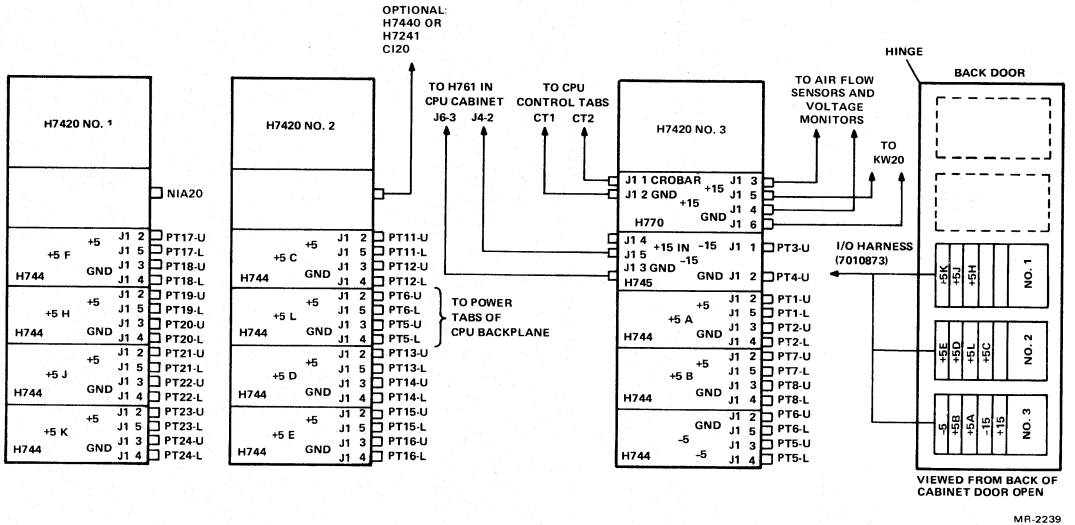
NOTES:
1. PTn-U = UPPER POWER TABS ON I/O BACKPLANE.
2. PTn-L = LOWER POWER TABS ON I/O BACKPLANE.
3. THE FOLLOWING POWER TABS ARE JUMPERED TOGETHER.

   PT7U TO PT9U
   PT5U TO PT25U
   PT8U TO PT10U
   PT5L TO PT25L
   PT7L TO PT9L
   PT6U TO PT26U
   PT8L TO PT10L
   PT6L TO PT26L
4. PIN BLOCK BUS BARS ARE USED IN THE RH20 AND DTE20 TO DISTRIBUTE -5.0 V AND IN THE DIA/DMA20 TO DISTRIBUTE -15 V.
5. H7420 NO. 2 (+5.0 L) SUPPLIES POWER TABS 5-U, 5L, 6U, AND 6L OF THE CPU BACKPLANE.
6. THE +15 V REGULATOR (H770) SUPPLIES THE AIR FLOW SENSORS IN THE KL10 SYSTEM.
7. COLOR CODES ARE AS FOLLOWS.

   BLACK = GND
   RED = +5
   GREEN = -5
   BLUE = -15
   ORANGE = +15

MR-2238

KL10 I/O DC POWER (BACKPLANE)



KL10 I/O DC POWER (DISTRIBUTION)

ECL PWR

KL10 ECL POWER ZONES

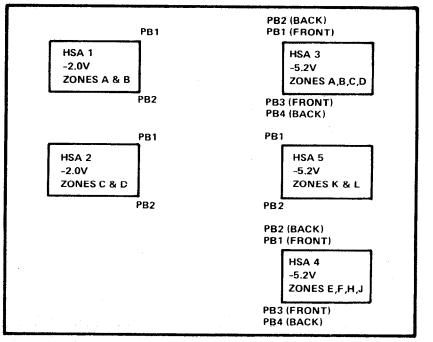
-5.2 VOLTS

ZONE	POWER REG	PB#	CIRCUIT BRKR	SENSE MODULE	BACKPLANE MOD
A	HSA-3	1	CBI	SLOT 1 G8010	SLOTS 4--12
B	HSA-3	2	CB2	SLOT 1 G8010	SLOTS 13--17
C	HSA-3	3	CB3	SLOT 1 G8010	SLOTS 19--24
D	HSA-3	4	CB4	SLOT 2 G8010	SLOTS 25--29
E	HSA-4	1	CB5	SLOT 2 G8010	SLOTS 30--36
F	HSA-4	2	CB6	SLOT 2 G8010	SLOTS 38--41
H	HSA-4	3	CB7	SLOT 3 G8010	SLOTS 42--45
J	HSA-4	4	CB8	SLOT 3 G8010	SLOTS 46--50
K	HSA-5	1	CB9	SLOT 3 G8010	SLOTS 51--54
L	HSA-5	2	CB10		

-2.0 VOLTS

ZONE	POWER REG	PB#	CIRCUIT BRKR	SENSE MODULE	BACKPLANE MOD
A	HSA-1	1	CB11	SLOT 5 G8011	SLOTS 4--14
B	HSA-1	2	CB12	SLOT 5 G8011	SLOTS 15--28
C	HSA-2	1	CB13	SLOT 5 G8011	SLOTS 29--41
D	HSA-2	2	CB14	SLOT 6 G8011	SLOTS 42--54

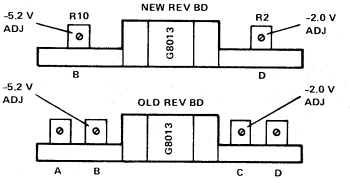
KL10 ECL POWER



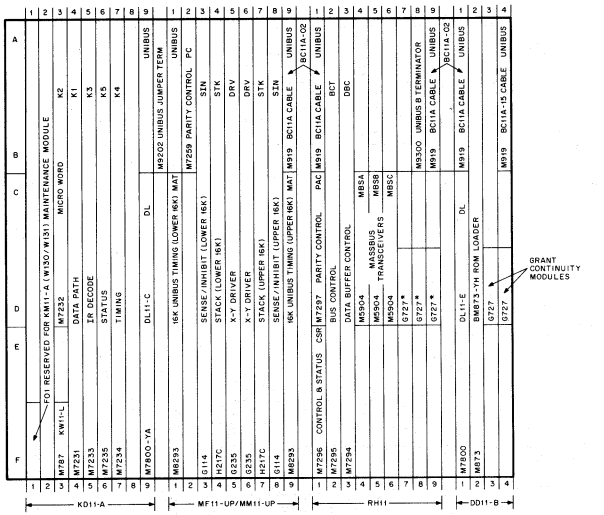
SLOTS

1	2	3	4	5	6	7	8
G8010 -5.2V ZONES A,B,C	G8010 -5.2V ZONES D,E,F	G8010 -5.2V ZONES H,J,K	SPARE	G8011 -2.0V ZONES A,B,C	G8011 -2.0V ZONE D	G8013 +10V REF.	G8014 DC LOW DETECT.

G8013 +10 VOLT REF
SLOT A07

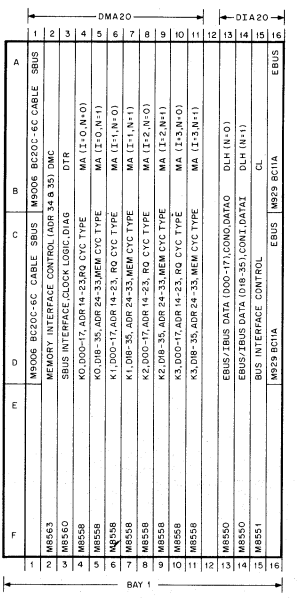


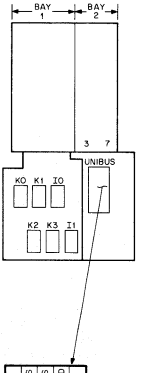
MR-2235



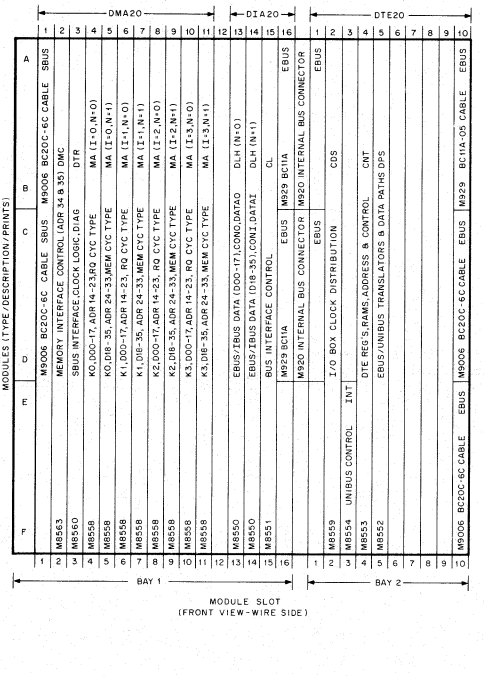
*G727 GRANT CONTINUITY MODULES IN D7,8,&9 (RH11) ARE NOT REQUIRED FOR BACKPLANES WIRED PER WIRELIST K-WL-RH11-0-12 OR HIGHER

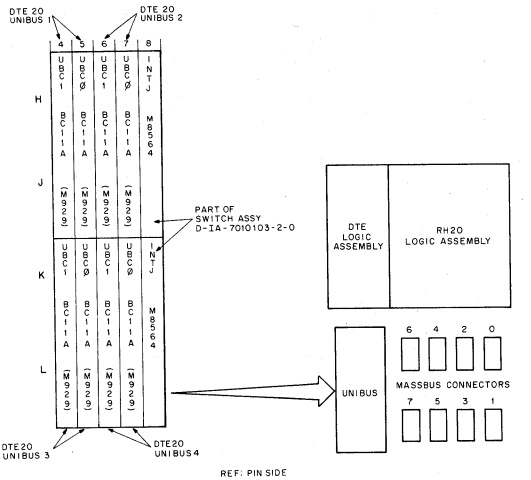
10-2073


MODULES (TYPE/DESCRIPTION/PRINTS)
DMA20
DIA20
BAY 1
MODULE SLOT
(FRONT VIEW-WIRE SIDE)

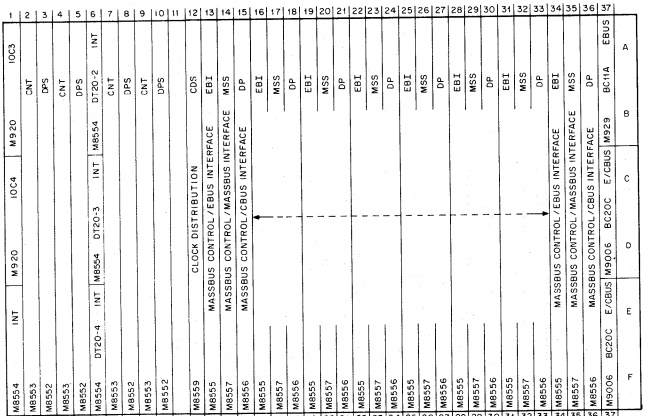

BAY 1
BAY 2
UNIBUS
K0 K1 I0
K2 K3 I1
NOT USED
BC11A-15 CABLE UNIBUS
BC11A-15 CABLE UNIBUS
M8564 DTE SWITCH/JUMPER BOARD
NOT USED

KL1080


MODULES (TYPE/DESCRIPTION/PRINTS)
DMA20
DIA20
DTE20
BAY 1
BAY 2
MODULE SLOT
(FRONT VIEW-WIRE SIDE)

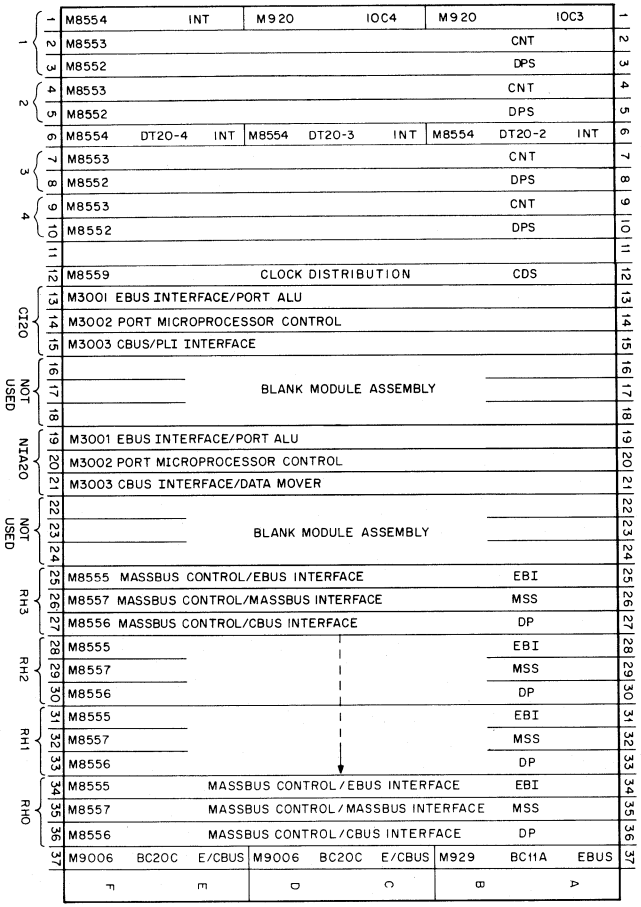


ALL SYSTEMS EXCEPT KL1080

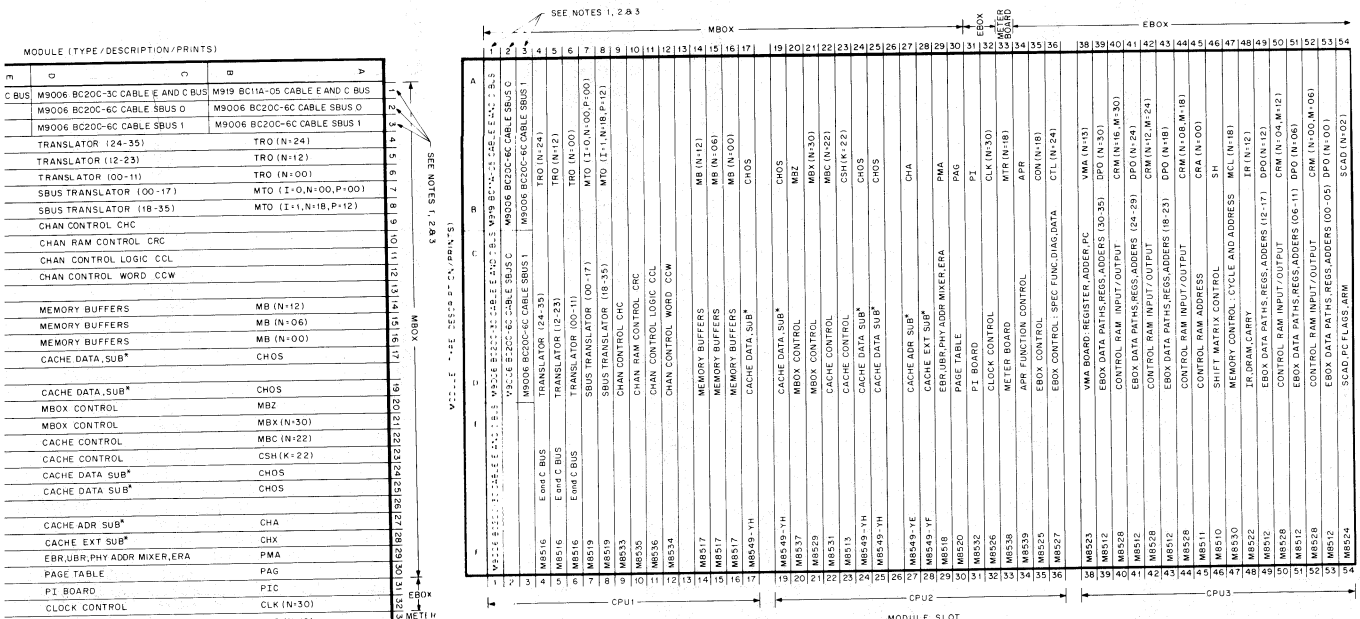


10-2472

MODULE LOCATIONS



MR 14265



MODULE (TYPE/DESCRIPTION/PRINTS)

E	D	C	B	A
C BUS	M9006 BC20C-3C CABLE E AND C BUS		M919 BC11A-05 CABLE E AND C BUS	
	M9006 BC20C-6C CABLE SBUS 0		M9006 BC20C-6C CABLE SBUS 0	
	M9006 BC20C-6C CABLE SBUS 1		M9006 BC20C-6C CABLE SBUS 1	
	TRANSLATOR (24-35)		TRO (N+24)	
	TRANSLATOR (12-23)		TRO (N+12)	
	TRANSLATOR (00-11)		TRO (N+00)	
	SBUS TRANSLATOR (00-17)		MTO (I+0,N+00,P+00)	
	SBUS TRANSLATOR (18-35)		MTO (I+1,N+18,P+12)	
	CHAN CONTROL CHC			
	CHAN RAM CONTROL CRC			
	CHAN CONTROL LOGIC CCL			
	CHAN CONTROL WORD CCW			
	MEMORY BUFFERS		MB (N+12)	
	MEMORY BUFFERS		MB (N+06)	
	MEMORY BUFFERS		MB (N+00)	
	CACHE DATA,SUB*		CHOS	
	CACHE DATA,SUB*		CHOS	
	MBOX CONTROL		MBZ	
	MBOX CONTROL		MBX (N+30)	
	CACHE CONTROL		MBC (N+22)	
	CACHE CONTROL		CSH (K+22)	
	CACHE DATA SUB*		CHOS	
	CACHE DATA SUB*		CHOS	
	CACHE ADR SUB*		CHA	
	CACHE EXT SUB*		CHX	
	EBR,UBR,PHY ADDR MIXER,ERA		PMA	
	PAGE TABLE		PAG	
	PI BOARD		PIC	
	CLOCK CONTROL		CLK (N+30)	
	METER BOARD		MTR (N+18)	
	APR FUNCTION CONTROL		APR	
	EBOX CONTROL		CON (N+18)	
	EBOX CONTROL : SPEC FUNC,DIAG,DATA		CTL (N+24)	
	VMA BOARD: REGISTER,ADDER,PC		VMA (N+13)	
	EBOX DATA PATHS,REGS,ADDERS (30-35)		EDP (N+30)	
	CONTROL RAM INPUT/OUTPUT		CRM (N+16,M+30)	
	EBOX DATA PATHS,REGS,ADDERS (24-29)		EDP (N+24)	
	CONTROL RAM INPUT/OUTPUT		CRM (N+12,M+24)	
	EBOX DATA PATHS,REGS,ADDERS (18-23)		EDP (N+18)	
	CONTROL RAM INPUT/OUTPUT		CRM (N+08,M+18)	
	CONTROL RAM ADDRESS		CRA (N+00)	
	SHIFT MATRIX CONTROL		SHM	
	MEMORY CONTROL : CYCLE AND ADDRESS		MCL (N+18)	
	IR,DRAM,CARRY		IRD (N+12)	
	EBOX DATA PATHS,REGS,ADDERS (12-17)		EDP (N+12)	
	CONTROL RAM INPUT/OUTPUT		CRM (N+04,M+12)	
	EBOX DATA PATHS,REGS,ADDERS (06-11)		EDP (N+06)	
	CONTROL RAM INPUT/OUTPUT		CRM (N+00,M+06)	
	EBOX DATA PATHS,REGS,ADDERS (00-05)		EDP (N+00)	
	SCAD,PC FLAGS,ARM		SCD (N+02)	

NOTES:
1. Slots 2 & 3 (SBUS) BC20C cables from internal memory or empty
2. Slots 1 (E/C BUS) BC11A and BC20C cables from DTE20
3. DMA20 SBUS connection to slot 3 only

*See module/variation chart.

** M8532-YA REQUIRED FOR CI20, NIA20

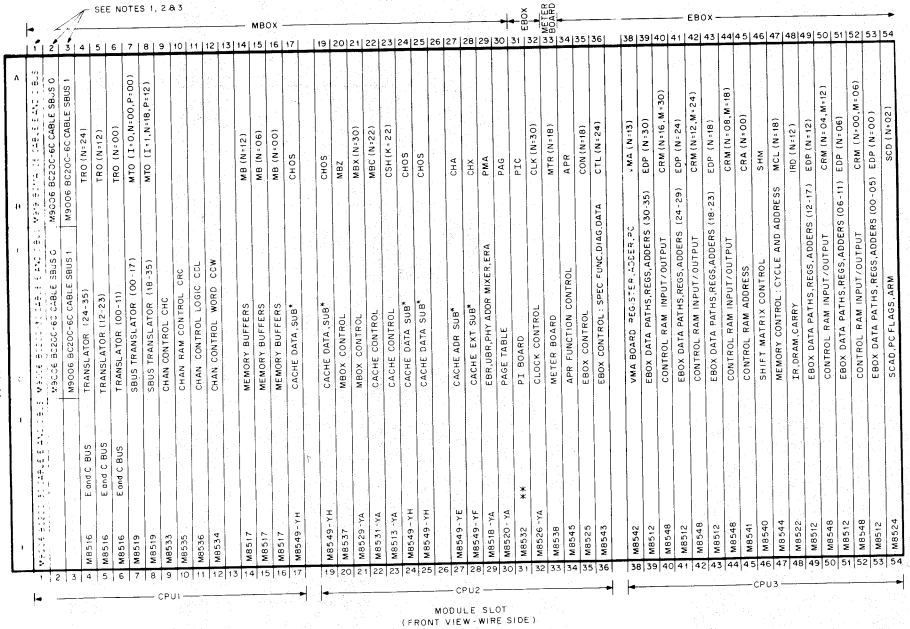
SLOT	MODULE/VARIATION CHART NO CACHE	CACHE
17	M8549-YH	M8521
19	M8549-YH	M8521
24	M8549-YH	M8521
25	M8549-YH	M8521
27	M8549-YE	M8514
28	M8549-YF	M8515

MR-2342

NOTES:
1. Slots 2 & 3 (SBUS) BC20C cables from internal memory or empty
2. Slots 1 (E/C BUS) BC11A and BC20C cables from DTE20
3. DMA20 SBUS connection to slot 3 only
   8519s can be 8580s for CORE/MOS mix
   8581s for MOS only
   8572 will be in slot 2 for machines with MOS

*See module/variation chart.

KL10 PA MUL



NOTES:
1. Slots 2 & 3 (SBUS) BC20C cables from internal memory or empty
2. Slots 1 (E/C BUS) BC11A and BC20C cables from DTE20
3. DMA20 SBUS connection to slot 3 only

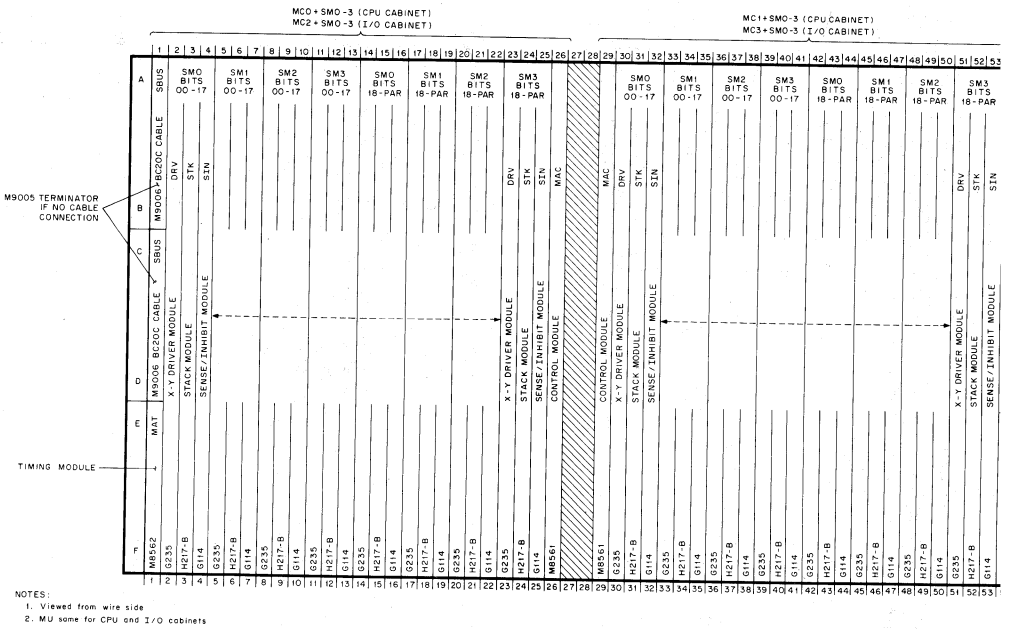
*See module/variation chart.

** M8532-YA REQUIRED FOR CI20, NIA20

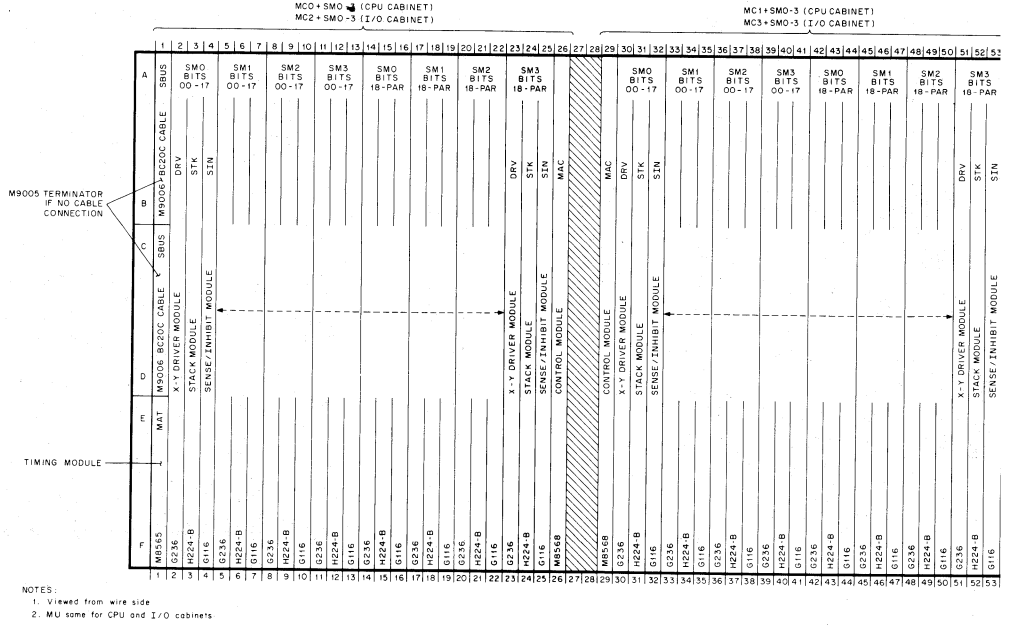
SLOT	MODULE/VARIATION CHART NO CACHE	CACHE
17	M8549-YH	M8521
19	M8549-YH	M8521
24	M8549-YH	M8521
25	M8549-YH	M8521
27	M8549-YE	M8514
28	M8549-YF	M8515

MR-3813

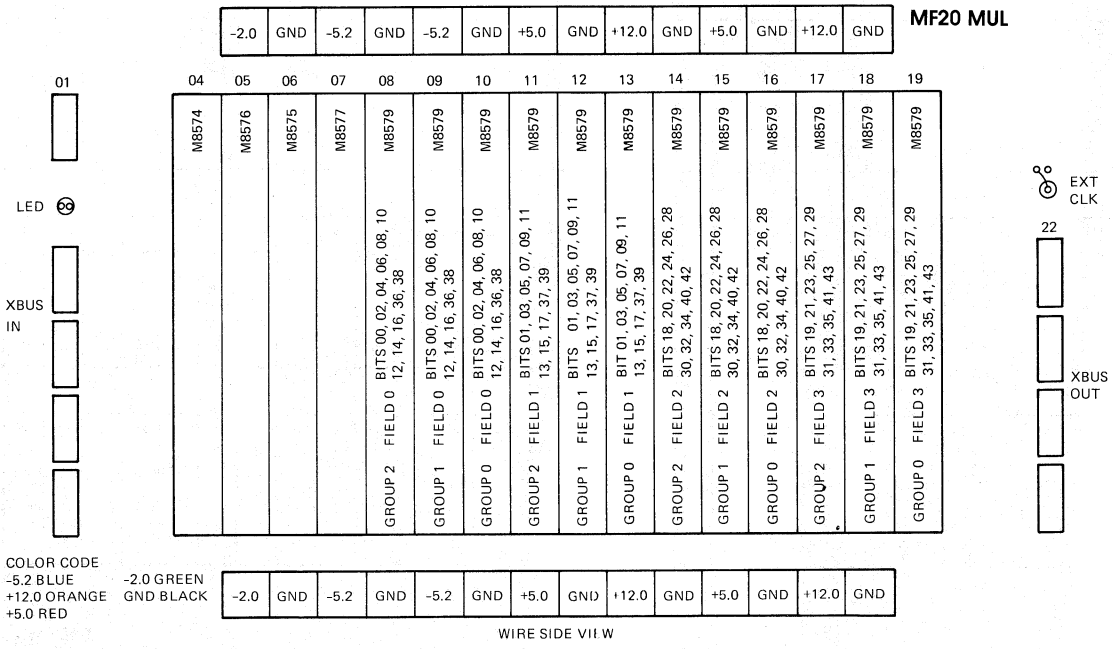
KL10 PV MUL



NOTES:
1. Viewed from wire side
2. MU same for CPU and I/O cabinets

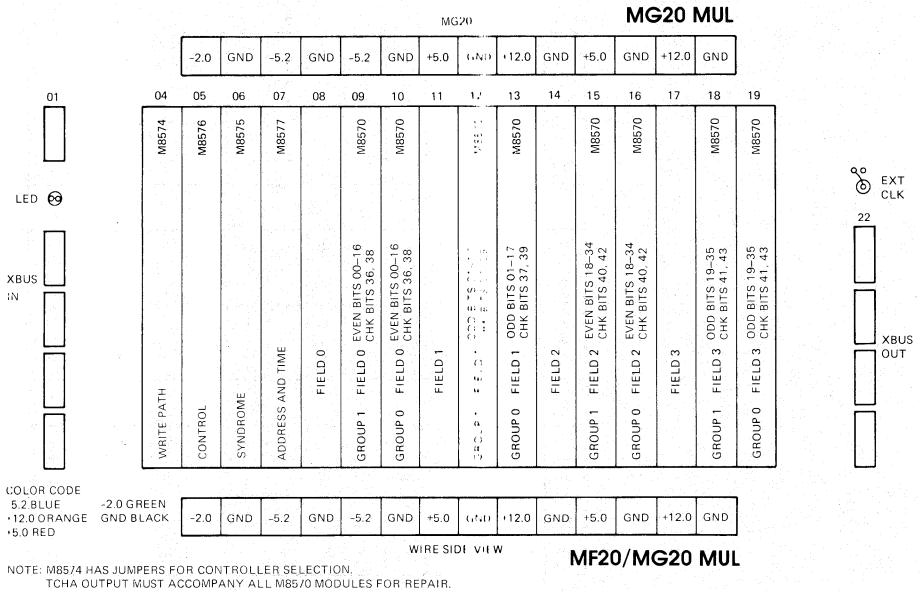


NOTES:
1. Viewed from wire side
2. MU same for CPU and I/O cabinets



MR-2302

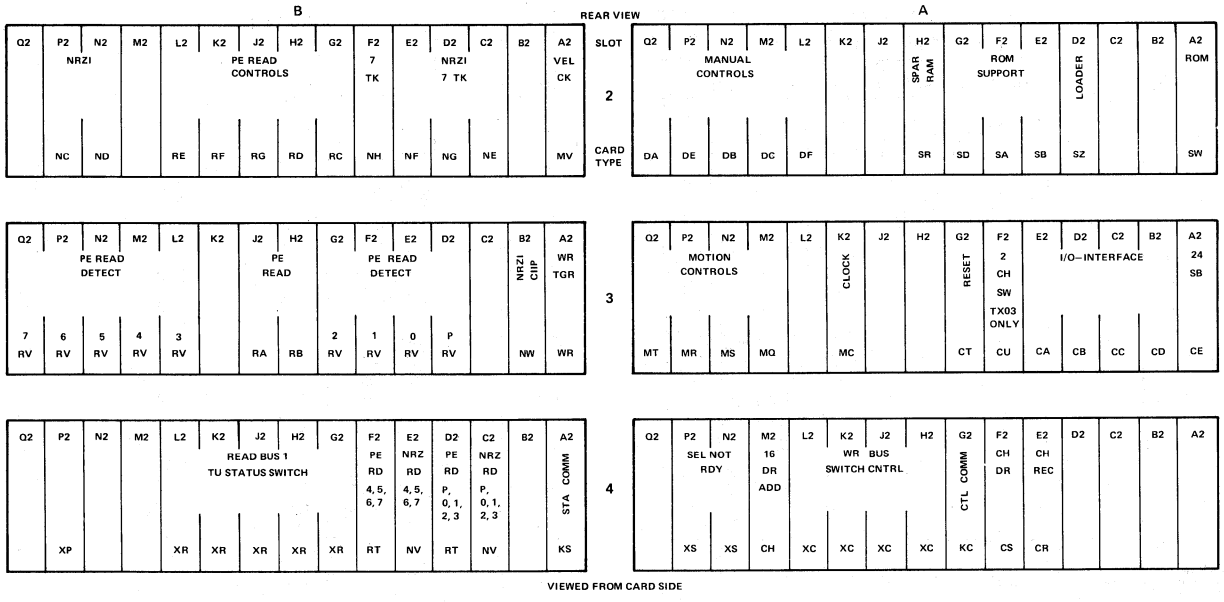
NOTE: M8574 HAS JUMPERS FOR CONTROLLER SELECTION.



MF20/MG20 MUL

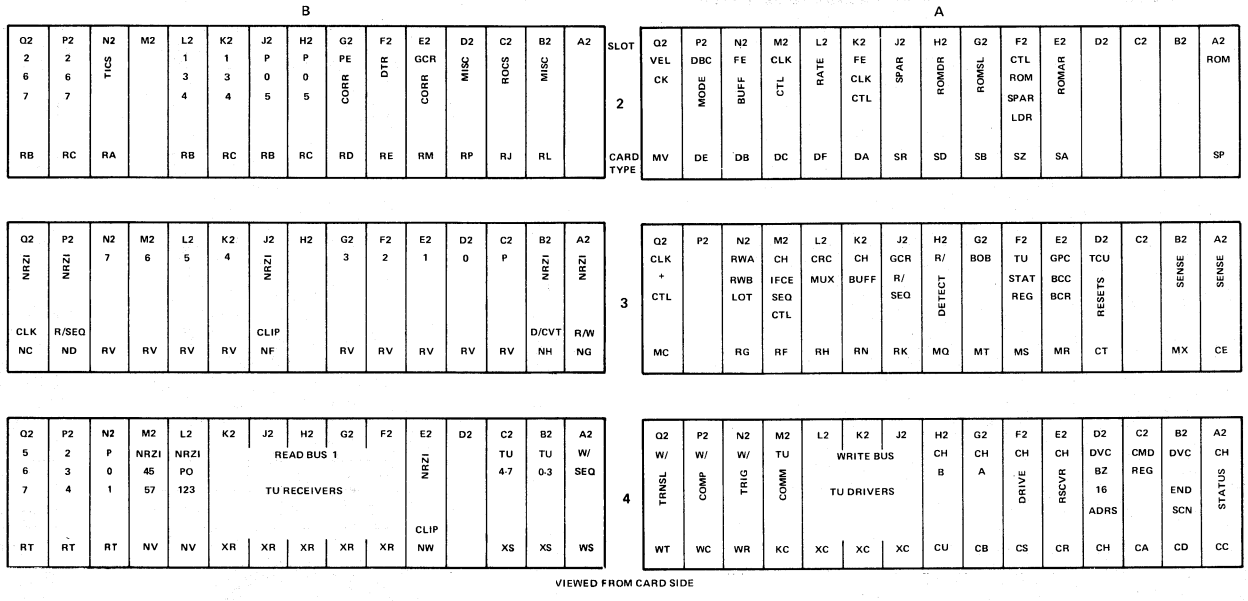
NOTE: M8574 HAS JUMPERS FOR CONTROLLER SELECTION.
TCHA OUTPUT MUST ACCOMPANY ALL M850 MODULES FOR REPAIR.
CHECK X-BUS DESKEW WHENEVER THE FOLLOWING MODULES ARE REPLACED
M8526, M8576, M8581, M8572, M8580.
CHECK X-BUS VREF WHENEVER M8580/81 IN SLOT 7 OF KL1C-PV IS REQUIRED REPLACED.
MG20 MAXIMUM MEMORY IS 2MG

MR-14262



MR-2311

TX01 MUL



MR-2312

TX02 MUL

	1	2	3	4	5	6	7
1A	R/W TERM	PADDLE TO LOGIC GATE (2C2)	WRITE STATUS	WRITE DRIVER 5 P O	WRITE DRIVER 7 2 6	WRITE DRIVER 3 1 4	LOAD CARD
1B	DAC	PE READ PRE AM 5, 7, 3, P, 2	PE READ PRE AM 1, 0, 6, 4	PADDLE TO HEAD AMP	NRZI READ PRE AM 0, 6, 4	NRZI READ PRE AM P, 2, 1	NRZI READ PRE AM 5, 7, 3

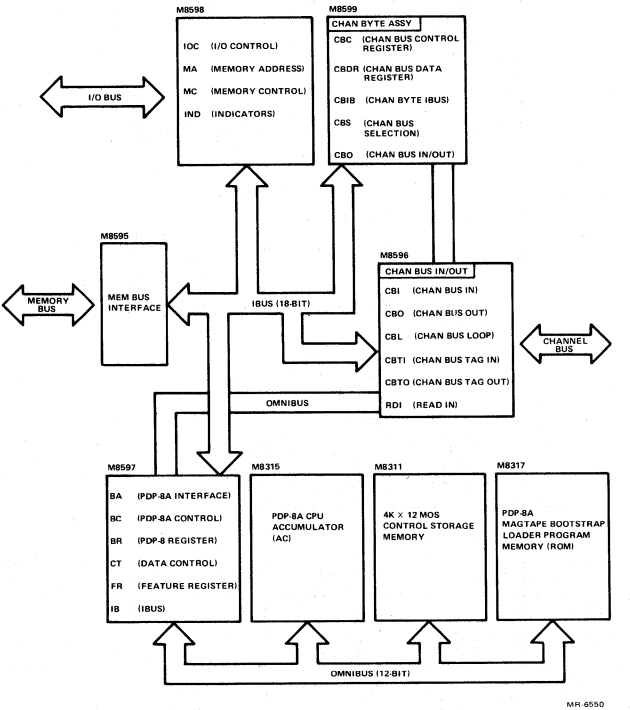
	1	2	3	4	5	6
2A		THREAD LOAD LOGIC		COUNTER LOGIC		TESTER CONN
2B		GO/ REW/ UNLOAD LOGIC		REEL CONTROL LOGIC		AC CONTROL LOGIC
2C	EOT/BOT LOGIC	PADDLE TO R/W GATE (1A2)		I/O LOGIC		CONFIG LOGIC

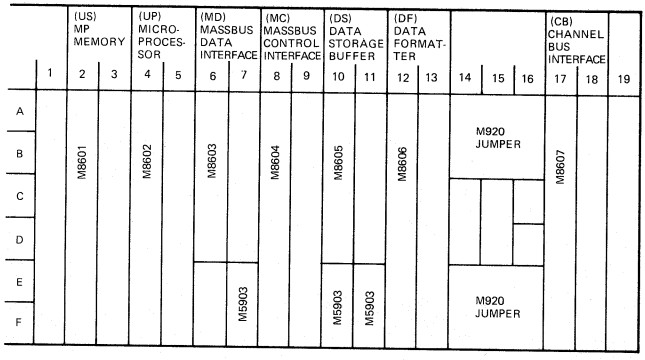
FRONT VIEW

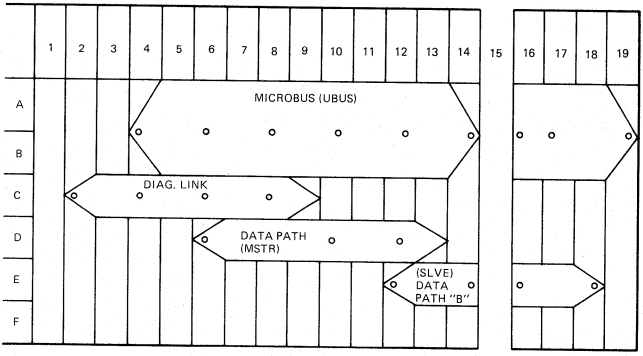
MR-2313

TU70 MUL

DX10 BOARD FUNCTIONS







NOTES:
1. SLOTS 3,5,7,9,11,13,AND 18 ARE RESERVED.
2. SLOT NUMBER 6, E/F IS A BLANK SPARE LOCATION, SLOT NUMBER 1 A-F IS BLANK SLOT,SLOT NUMBER 14, C/D IS BLANK SPARE LOCATION, SLOT NUMBER 15 IS SHOWN FOR REFERENCE ONLY AND DOES NOT PHYSICALLY EXIST.
3. SLOT NUMBER 19 IS RESERVED FOR CHANNEL BUS EXTENSION EXPANSION.

MR 0908

Table of Contents

MULTI-CPU

INTRODUCTION
The information in this module is meant for DIGITAL field service engineers and applies to the maintenance of the multi-CPU configuration. The multi-CPU configuration is a system made of multiple KL10-D (DECsystem-1090) CPUs.

Hardware Documentation
Table 1 lists the hardware manuals that have information pertaining to the multi-CPU configuration.

Table 1 Hardware Documents

Title	Document No.
BA10 Hard Copy Control Maintenance Manual, Volume 1	EK-0BA10-MM
CI20 Reference Manual	EK-OCT20-TM
CR04 M200 Technical Manual	ER-00200-TM
CR04-A/B/C/D Card Reader Manual	EK-CR04A-IP
CR04-H/J Documentation M-1200	EK-CR04H-IP
DF10 Data Channel Maintenance Manual	63H028
DF10-C Data Channel Maintenance Manual	63H030
DL10 Data Line Maintenance Manual	EK-0DL10-MM
DN2X/DNHXX Communications Subsystem Technical Manual	EK-0DN2X-TM
DN87S Communications Subsystem Technical Manual	EK-DN875-TM
DX10 Data Channel Maintenance Manual	EK-0DX10-TM
DX10 Data Channel Maintenance Manual Addendum	EK-0DX10-AD
DX20 Programmed Device Adapter Technical Manual	EK-0DX20-TM
KL10 Based DECsystem-10 Installation Manual	EK-1080U-IN
KL10 Based Power Description	EK-1080U-PD
KL10 Based System Service Manual	EK-0KL10-SV
LP04 Maintenance Manual, Volume 1	ER-90671-00
LP04 Line Printer, Volume 2	ER-2LP04-TM
LP04 Maintenance Manual, Volume 3	ER-90670-00
LP05 Maintenance Manual, Volume 1	ER-00009-MM
LP05 Maintenance Manual, Volume 2	ER-5V157-MM
LP14 Maintenance Manual, Volume 1	ER-12290-TM
LP14 Maintenance Manual, Volume 2	ER-22290-TM
LP100 Line Printer System Maintenance Manual	EK-LP100-MM
MF10 Core Memory Maintenance Manual	63H095
MH10 Maintenance Manual	EK-0MH10-MM
MX10/MX10C Multiplexor Manual	EK-MX10C-MM
Multi-CPU User's Guide	EK-MULCP-UG
NIA20 Reference Manual	EK-NIA20-RM
PC04 Paper Tape Reader Punch	EK-0PC04-IP
PC04/05 Reader Punch Manual	EK-PC045-MM
PC04/05 User's Manual	EK-PC045-OP
PC10/PC20 High Speed Paper Tape Reader/Punch Technical Manual	EK-0PC20-TM
Power System (1080/1090) Interface Description	EK-0PWR-ID
RH10 Maintenance Manual	EK-0RH10-MM
RP04 Device Control Logic User's Manual	EK-0RP04-OP

Table 1 Hardware Documents (Cont)

Title	Document No.
RP04 Device Control Logic Maintenance Manual	EK-0RP04-MM
RP04 Disk Drive Installation Manual	EK-0RP04-IN
RP05/06 677-01/51 Logic Manual	EK-00012-TM
RP05/06 677-01/51 Logic Manual	EK-00014-TM
RP05/06 Disk Drive Installation Manual	EK-RP056-IN
RP05/06 Disk Drive Maintenance Manual	EK-RP056-MM
RP05/06 User's Manual	EK-RP056-OP
RP07 Service Manual	EK-0RP07-SV
RP07 Technical Description	ER-0RP07-TD
RP07 Pocket Service Guide	EK-0RP07-PS
RP07 Pathfinder	
RP07 User's Guide	ER-0RP07-UG
RP10 Maintenance Manual	63H8120
RP20 Disk Subsystem User's Guide	EK-0RP20-UG
TD10 DECtape Control, Volume 1	DEC10-I3AB-D
TM03 Magnetic Tape Formatter Technical Manual	EK-OTM03-TM
TM03 User's Manual	EK-OTM03-OP
TU16/TM02 Maintenance Manual	EK-OTU16-MM
TU16/TM02 Tape Drive System User's Manual	EK-OTU16-OP
TU45 Magtape System Manual	EK-TU45A-MM
TU56 DECtape Transport User's Manual	EK-OTU56-OP
TU56 DECtape Transport Maintenance Manual	99H429
TU72 Field Engineering Maintenance Manual (STC Vendor Manual)	P/N 9094
TU72 SPAR User's Guides, Volumes 1 and 2 (STC Vendor Manual)	P/N 9245
TU77 Magtape Technical Manual, Volume 2	EK-2TU77-TM
TU77 Magtape Transport	EK-0TU77-UG
TX01/02 3800-III Tape Control Unit (STC Manual)	EK-TX01-VEN)
TX02 Theory of Operation Manual (STC Manual)	P/N 9194
TX02 Field Engineering Maintenance Manual (STC Manual)	P/N 9204
TX02 Installation Manual (STC Manual)	P/N 9057

Software Documentation
Table 2 lists the software guides that have information pertaining to the multi-CPU configuration.

Table 2 Software Documents

Title	Document No.
TOPS-10 Monitor Installation Guide	AD-5056B-T2
TOPS-10 Networks Software Installation Guide	AD-5156E-T1
TOPS-10 Operator's Guide	AD-H283A-T2

Print Sets
Table 3 lists the print sets that have information pertaining to the multi-CPU configuration.

Table 3 Print Sets

Device	Order Number	Device	Order Number
BA10	MP-BA10-00	PC04	MP00316
CI20	MP01906-01		
CR04-W	MP00359	RH10	MP-RH10-00
DF10	MP-DF10-00	RP04-H	MP00257
DF10-C	MP-DF10-C	RP04-TC	MP00614
DL10	MP-DL10-00	RP06	MP00081 and MP01011
DN20	MP00389	RP07	ER-ORP07-MP
DN21	MP00390	RP10-A	MP-RP10-A
DN25	MP00391	RP10-C	MP-RP10-C
DN87S	MP00109	RP20	
DX10	MP-0DX10-00	TD10	MP-TD10-00
DX20	MP00432	TM02	MP-TM02-00
KL10-D	MP00448	TM03	MP00349
LP04	MP-LP04-00	TU16	MP-TU16-00
LP05	MP-0LP05-00	TU45	MP00441 and MP01113
LP07		TU56	MP-TU56-00
LP14	MP00861	TU70	
LP100	MP00201	TU71	
MF10	MP-MF10-00	TU72	
MG10	MP-MG10-00	TU77	MP00644
MH10	MP00178	TX01/02/ 03/05	
MX10	MP-MX10-00		
NIA20-B	MP-01907-01		

Acceptance, corrective maintenance, installation, and preventive maintenance procedures can be found in maintenance or technical manuals pertaining to the specific device. Detailed installation information and procedures for the KL10-D CPU can be found in the KL10 Based DECsystem-10 Installation Manual (EK-1080U-IN). Diagrams and information specific to the multi-CPU configuration can be found in the Multi-CPU User's Guide (EK-MULCP-UG).

MAINTENANCE PHILOSOPHY
The maintenance philosophy for the multi-CPU configuration is simple: isolate the failing devices while the rest of the system is in operation, repair or replace these devices, and reconfigure the system. Isolating failing devices for repair involves separating from the system a minimum system that includes those devices; this allows the bulk of the system to continue operating normally. A minimum system is made up of one KL10-D CPU, one disk drive, the failing device(s), and the minimum memory needed. Thus, corrective and preventive maintenance may be performed without loss to the customer.

The maintenance philosophy is based on the following facts.

1. The operating system software completely supports user mode diagnostics for the KL10-D CPU and its peripheral devices.

2. Remote diagnostics and software support are available through the use of the KL Integrated Network for Investigation and Korrection (KLINIK) at local field service branch offices and at the DIGITAL Diagnosis Center (DDC).

service branch offices and at the DIGITAL Diagnosis Center (DDC).

3. The diagnostics can isolate failures.

4. The system error reporting package (SPEAR) is available on the system.

SYSTEM SEPARATION

In order to separate the Multi-CPU configuration into two separate systems, (one for Field Service maintenance and one for the customers normal operations), the following procedure is used. This procedure allows the system operator to separate KL10-D CPUs, disk drives, and system memories. The procedure also allows Field Service engineers to reconfigure the KL10-D CPU, disk drives, and system memory after the operator has completed his/her task.

For the operator to split the Multi-CPU configuration, the necessary devices are removed from the timesharing system. The following steps set aside a portion of the system, while maintaining the timesharing portion, and then rejoin the sections after the Field Service engineer is done.

NOTE

In this procedure, the system used by the customer for normal timesharing operation is called SYSTEM A and its components CPU A, RP A, and MEM A. The system used by the Field Service engineer for Field Service maintenance is called SYSTEM B and its components CPU B, RP B, and MEM B.

In sections of the procedure where a system and operator dialog is used, the characters typed by the operator are underlined and the characters shown by the system are not underlined.

Refer to the TOPS-10 Software Notebooks for details of the commands used in this procedure.

1. Make sure that all disk packs are removed from the disk drives that the Field Service engineer needs.

NOTE

The dismounting of structures on the disk drives to be used by Field Service must be done by the system operator.

2. To prepare the system for the removal of CPU B and its memory (MEM B) reserved for it, run CONFIG at CPU A's operator terminal. The following dialog is an example of typical structures and the exchange that follows.

```
.R CONFIG

CONFIG> REMOVE CPU B

% Following drive(s) are dual ported with CPU being removed:

     RPC3
     RPD2
     RPD4
     RNC0
     RNC1
     RNC2
     RNC3
     RND0
     RND1
     RND2
     RND3
CPU B Detached
CONFIG> REMOVE MEMORY mmmK to nnnK words

CONFIG> ^C

.XCHNGE RPC3 RPC3

.XCHNGE RPD2 RPD2
```

.XCHNGE RPD4 RPD4

.XCHNGE RNC0 RNC0

.XCHNGE RNC1 RNC1

.XCHNGE RNC2 RNC2

.XCHNGE RNC3 RNC3

.XCHNGE RND0 RND0

.XCHNGE RND1 RND1

.XCHNGE RND2 RND2

.XCHNGE RND3 RND3

NOTE

The terms mmmK to nnnK compose the part of memory that will be used for stand-alone purposes.

3. On the CTY connected to CPU B, enter PARSER, then HALT and RESET the CPU.

Table 4 indicates the memory address switch settings (MADR) for MH10 core memories with 256K boxes of memory.

Table 4 Memory Address Switch Settings

Memory Address	Memory No.	MADR Switches 14	15	16	17	18	19	20
0000000-0777777	0	0	0	0	0	0	0	0
1000000-1777777	1	0	0	0	1	0	0	0
2000000-2777777	2	0	0	1	0	0	0	0
3000000-3777777	3	0	0	1	1	0	0	0
4000000-4777777	4	0	1	0	0	0	0	0
5000000-5777777	5	0	1	0	1	0	0	0
6000000-6777777	6	0	1	1	0	0	0	0
7000000-7777777	7	0	1	1	1	0	0	0

In order to reconfigure the MH10 memory, perform the following steps.

1. Record all switches in MH10 memories.
2. Deselect the memories affected using the SELECT/DESELECT switch in each MH10.
3. Deselect all memory ports that are connected to CPU A.
4. Deselect all memory ports that are connected to CPU B in the memories remaining on CPU A.
5. Set the address switches on the deselected memories to 0 and 1 (refer to Table 4).

NOTE

The desired memories are now physically connected to the stand-alone CPU (CPU B). CPU B cannot access the memories remaining on CPU A.

The disk drives between SYSTEM A and SYSTEM B are dual ported, so there are different procedures for placing these disk drives on SYSTEM A or SYSTEM B. Those drives that were previously exchanged must have their DUAL PORT switch locked on to the correct port.

After exchanging the drives (as done in step 2 by the XCHNGE command), do the following.

For RP04-type disk drives, set the A/B switch to the correct position and press the DISABLE switch.

For RP06-type disk drives, set the A/B switch to the correct port and remove the lap plug.

For RP07-type disk drives, set the access A/B switch to the correct port. Toggle the OFF LINE/ON LINE switch once to switch to the locked-on port and once again to put the drive on-line.

For RP20-type disk drives, set the X or Y interface switches to ENABLE or DISABLE.

SYSTEM REJOINING

To return the system to maximum performance, HALT and RESET the stand-alone CPU (CPU B). Then do the following.

1. Return all dual-ported disk drives to the A/B position. (Refer to the separation procedure for disk drives in the System Separation section).

2. To reconfigure memory, follow the inverse of the memory deselect procedure:

   a. Set the address switches on the deselected memory to their original positions as recorded.

   b. Enable all memory ports.

   c. Enable the memories affected using the SELECT/DESELECT switches in each MH10.

SYSTEM A and SYSTEM B can now access all memory. In order to boot SYSTEM B, do the following.

1. Using the CTY of SYSTEM B, type RESET to the PARSER.

2. Carry out the KLINIT dialog, as shown below, to reload the correct microcode on the system and ensure that all field service data is cleared from memory.

```
CTRL/\
PAR# RESET
PAR# MCR KLI
```

   The system will type the following.

```
KLI -- VERSION YA12-27 RUNNING
KLI -- ENTER DIALOG [NO,YES<EXIT,BOOT]?
KLI>NO
KLI -- KL10 S/N 1026 ., MODEL B, 60 HERTZ
KLI -- KL10 HARDWARE ENVIRONMENT
       Extended Addressing
       Internal Channels
       Cache

KLI -- MICROCODE VERSION 247 LOADED
KLI -- ALL CACHES ENABLED
```

3. After exiting from KLINIT, reset the clock again (as a safety precaution), type J 400, and press RETURN to start CPU B.

4. To complete the return of CPU B and MEM B to the system, run CONFIG on the operator's terminal on SYSTEM A by typing the following.

```
.R CONFIG

CONFIG> ADD CPU B

CONFIG> ADD MEMORY mmmK to nnnK words

CONFIG> ^C

.
```

5. Now go to the CTY of SYSTEM B and the following message should appear there.

```
[CPU B]
```

This indicates that the system is now rejoined and capable of full operation.

NOTE

To verify that the disks are dual-ported again, run SYS/P.

DIAGNOSTIC INFORMATION
Different types of diagnostics are available on the multi-CPU system. (All these diagnostics are used on other system configurations as well.) Each diagnostic has a code that tells the user how the diagnostic is used. The codes are as follows.

```
0 = Not specified
1 = EXEC mode type
2 = USER mode type
4 = Special
```

These codes can be combined (added together), so that one code may be used for multiple diagnostics. For example:

```
3 = EXEC (1) + USER (2)
```

SLEEP MODE
Sleep mode allows the field service engineer to put the multi-CPU system in a "time freeze" condition. This allows the field service engineer to replace, reconfigure, or repair parts of the system without affecting it seriously. This mode differs from system division in that physical reconfiguration and/or repair can be done without damage to the TOPS-10 monitor or system operations in progress.

The procedure for putting the system to sleep appears below. Information placed in parentheses ( ) is not part of the procedure, but rather a comment meant to help the field service engineer in understanding this mode.

```
.R CONFIG (run the CONFIG program)
CONFIG>REMOVE MEMORY 512K to 1024K (logically remove 512K)
CONFIG>REMOVE CPU1 (logically remove CPU1)
CPU1 Detached
CONFIG>SUSPEND (places the system in sleep mode)

;;SYSTEM: - Expect an interruption of service
            (first warning to system users)

;;SYSTEM: - Suspending system operation
            (second warning to system users)

[Suspending system on DSKN:CRASH.EXE[1,4]]
[SYSTEM suspended] (messages on CTY)

PAR>RESET   (reset parser)
PAR#MCR KLI (the field service engineer can physically
              reconfigure and work on system)
      .      (time to boot again should be short; major repairs
      .       in which the entire system is needed
      .       should be scheduled for stand-alone time by
      .       field service)
      .
      .
      .

KLI -- VERSION YA12-27 RUNNING (get system running)
KLI -- ENTER DIALOG [NO,YES,EXIT,BOOT]?
KLI>NO
KLI -- KL10 S/N: 1026., MODEL B, 60 HZ
KLI -- KL10 HARDWARE ENVIRONMENT (system information)
        EXTENDED ADDRESSING
        INTERNAL CHANNELS
        CACHE

KLI -- MICROCODE VERSION 247 LOADED (load microcode)
KLI -- ALL CACHES ENABLED

LOGICAL MEMORY CONFIGURATION. (512K of memory physically removed)
  ADDRESS  SIZE  INT  TYPE CONTROLLER
 00000000  512K  4  DMA20  4

KLI -- CONFIGURATION FILE WRITTEN (loading bootstrap)
KLI -- BOOTSTRAP LOADED AND STARTED
BOOT V1(6)

BOOT>dskn:/r (boot again)
[Reloading from DSKN:CRASH.EXE[1,4]]
```

```
[CPU0]
CONFIG>
;;SYSTEM: - System resumed
            (system up and running with CPU0 and 512K of memory)
^C

(make repairs and put the system back together after repairs are
completed)

.R CONFIG (run CONFIG)

CONFIG>SUSPEND

;;SYSTEM: - Expect an interruption of service
            (in order to put the system back together)

;;SYSTEM: - Suspending system operation
[Suspending system on DSKN:CRASH.EXE[1,41]]
[SYSTEM suspended]

PAR>RESET (put memory back on system)
PAR#MCR KLI
KLI -- VERSION YA12-27 RUNNING
KLI -- ENTER DIALOG [NO,YES,EXIT,BOOT]?
KLI>NO
KLI -- KL10 S/N: 1026., MODEL B, 60 HZ
KLI -- KL10 HARDWARE ENVIRONMENT:
        EXTENDED ADDRESSING
        INTERNAL CHANNELS
        CACHE

KLI -- MICROCODE VERSION 247 LOADED
KLI -- ALL CACHES ENABLED

LOGICAL MEMORY CONFIGURATION.
  ADDRESS  SIZE  INT  TYPE CONTROLLER
 00000000 1024K  4  DMA20  4
(back to 1024K of memory)

KLI -- CONFIGURATION FILE WRITTEN
KLI -- BOOTSTRAP LOADED AND STARTED
BOOT V1(6)

BOOT>dskn:/r
[Reloading from DSKN:CRASH.EXE[1,4]]

[CPU]
CONFIG>
;;SYSTEM: - System resumed

CONFIG>ADD MEMORY 512K TO 1024K (logically put back 512K
                                 of memory)
CONFIG>ADD CPU1 (logically put back CPU1)
CONFIG>
```

SYSTEM CHECKOUT PROCEDURE

The following procedure is used when a new multi-CPU system or additional KL10-D processors are being installed. The procedure provides the field service engineer with a diagnostic sequence that must be successfully completed before the operating system can be loaded and run. Problems or errors that occur should be corrected and related diagnostics run again before continuing with the sequential checkout.

The following test equipment and media are needed for the standard diagnostic checkout procedure.

- Oscilloscope, Tektronix™ 475
- Digital voltmeter
- Microfiche library and reader
- RP04 DDU or RP06 PERCH tester
- RPCE pack for RP04 or RP06
- Front-end DECtapes (one set)
- KLAD-10 pack
- Master skew tape
- Scratch magnetic tapes (quantity depends on number of drives on the system)
- Scratch disk (quantity depends on number of drives on the system)
- Scratch DECtape

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Index MD-10-DDXXA can be found on microfiche in the microfiche diagnostic library. The index lists all available diagnostics and their latest revisions.

In order to check out any single KL10-D processor on a multi-CPU system, proceed as follows.

1. Run the utility programs needed to run the KL10-D front-end diagnostics.

2. Load KLDCP from DECtape or disk. At KLDCP command level, set the clock rate to normal, set the clock source to fast, and execute the B command. This will direct KLDCP to run the 11-based 11 and 11-based 10 diagnostics.

3. Reset the clock source to normal. Then run the Instruction Timing Test (DFKFB) and compare the results with those provided by the manufacturing specifications.

4. Boot the KL10-D using the KLDCP BT command, which initializes the KL10-D to run 10-based 10 diagnostics.

5. Run DEMMG.A10, a memory dependability test, for 8 hours. When the test is completed, run DDMME.A10, the memory BLT test.

6. Run DFRHB.A10, the RH20 Fault Isolator Test, for 20 minutes.

7. Verify the correct head alignment for each drive in the system. Refer to the RP06 Installation Manual or the RP20 User's Guide for the correct procedures.

8. Format the scratch packs in PDP-10 (20 sector) mode. Refer to the specific disk drive diagnostic for the formatting procedure.

9. After the scratch packs are formatted, run the appropriate Basic Device Test.

10. Under DDRPI, run PTIME (Test 14), ACCEPT (Test 12), and RONLY (Test 01). For compatibility, run RONLY on all drives and rotate the packs until all packs have cycled through all drives.

11. Run the system exerciser, DFSXA.A10, to check all channels, system memory, all I/O devices, and the front end. Try to run this test overnight before booting the KLAD pack monitor.

Table of Contents

DECnet-10/20

HARDWARE

The DECnet-10 and -20 are supported by the DN2X Communications Subsystem which features an 1134A processor with 32K of parity core memory (expandable to 48K) or 128K MOS directory, memory management, a programmer's maintenance panel, a ROM bootstrap loader, and a down-line load link for maintenance purposes. The DN2X communicates with the DECsystem-10/DECsystem-20 via the DTE20. DECNET-10/20 requires 128K of memory.

The two basic product families of the subsystem are:

1. Low Speed Synchronous - The DN20 provides a low-speed (2.4K to 19.2K bits/second) synchronous communications capability from a minimum of 1 line to a maximum of 12 lines.

2. High Speed Synchronous - The DN21 and DMR11 provide a high-speed (19.2K bits/second to 1M bits/second synchronous communications capability from a minimum of 1 line to a maximum of 4 lines (DN20-CX) or 6 lines (DN20-MX).

Product Definitions
The following model numbers are defined for use with the DN2X front end processor.

DN20 2.4K--19.2K bits/s synchronous communication family.

DN20-BA — 2.4K--19.2K bits/s synchronous single line expander (maximum of one per DN20-C and DN20-D -- includes one DUP11-DA and one KMC11-A).

DN20-BB — Basic 2.4K--19.2K bits/s synchronous line expander (maximum of three per DN20-C and six per DN20-D -- includes one DUP11-DA).

DN20-C — 2.4K--19.2K bits/s basic synchronous communications cabinet (required for all synchronous and asynchronous capability -- expandable to four -- 2.4K--19.2K bits/s lines with DN20-BA and DN20-BB -- includes one 1134A CPU in a 26.6 cm (10.5 in) mounting drawer and one cabinet).

DN20-CA/CC 120 V/60 Hz
DN20-CB/CD 240 V/50 Hz

DN20-D — 2.4K--19.2K bits/s synchronous communications expansion drawer. Required for up to 19.2K bits/s expansion beyond four lines when there is no other synchronous expansion drawer already installed in the available mounting space in the basic cabinet -- expandable to eight lines with DN20-BA and DN20-BB -- includes one DUP11-DA, one KMC11-A, and one 26.6 cm (10.5 in) mounting drawer.

DN20-DA 120 V/60 Hz
DN20-DB 240 V/50 Hz

DN20-M — Basic synchronous communications cabinet required for all synchronous and asynchronous capability -- includes one 1134A CPU with 128K MOS memory in mounting drawer and one cabinet.

DN20 MA/MC 120 V/60 Hz
DN20 MB/MD 240 V/50 Hz

DN21 56K/1M bits/s synchronous communication family.

DN21-BA — 19.2--56K bits/s synchronous single line expander (maximum of three per DN21-D -- includes one DMC11-FA and one DMC11-AR).

DN21-BB — 56K baud integral line unit -- includes one DMC11-AL IPL microprocessor, one DMC11-MD line unit with integral modem and one BC03N-A0 coaxial cable.

DN21-D — 19.2--56K bits/s synchronous communications expansion drawer (required for basic 56K bits/s expansion when there is no other synchronous expansion drawer already installed in the available mounting space in the basic cabinet -- expandable to four lines with DN21-BA -- includes one DMC11-FA, one DMC11-AR, and one 26.6 cm (10.5 in) mounting drawer).

DN21-DA 120 V/60 Hz
DN21-DB 240 V/50 Hz

DN21-HA — 1 megabaud integral line unit -- includes one DMC11-AL IPL microprocessor, one DMC11-MA line unit with integral modem and one BC03N-A0 coaxial cable. Placed in DN20-M drawer.

DN21-JA — 19.2K-1M bits/s synchronous communications expansion drawer (required for basic 56K bits/s expansion when there is no other synchronous expansion drawer already installed in the available mounting space in the basic cabinet - expandable to four lines.

DN21-JA 120 V/60 Hz
DN21-JB 240 V/50 Hz

DMR11-A — High speed synchronous line unit capable of supporting several interface specifications according to switch settings and cables used. It consists of two boards: an M8207-RA microprocessor, and an M8203 line unit. The variations are as follows.

DMR11-AA -- 19.2K bits/s maximum (RS-232-C) or 56K bits/s maximum (RS-423-A) interface configuration.

DMR11-AB -- 1M bits/s maximum CCITT V.35 interface configuration

DMR11-AC -- 1M bits/s maximum integral modem interface configuration

DMR11-AE -- 1M bits/s maximum RS-422-A interface configuration

DN20F OPTIONS
The following options are available on the DN20F Communications Subsystem.

DN20F-MA/MC — This base starter unit is used for configuring any capability. The PDP-11/34 drawer in this unit has dedicated space for low-speed synchronous lines or high-speed lines. The first low-speed line is obtained with the DN20F-BA. The second, third, and fourth lines are obtained with three DN20F-BBs. The high-speed line is obtained with DMR11-*P.

DN20F-BA — This 2.4K to 19.2K bits/s low-speed synchronous single line expander has a maximum of three lines per DN20F-MA and DN20F-MC, which iincludes one DUP11-M, one KMC11-M, and one CK-DUP11-A*. The DN20F-BA provides the first low-speed synchronous line expansion in the basic drawer of a DN20F-MA/MC and the fifth and ninth lines expansion when used in the second backplane of the expansion drawer.

DN20F-BB — This 2.4 to 19.2K bits/s low-speed synchronous single line expander provides a maximum of nine lines per DN20F-MA/MC, which includes one DUP11-M and one CK-DUP11-A*. The DN20F-BB provides the second, third, fourth, sixth, seventh, eighth, tenth, eleventh, and twelfth low-speed synchronous line expansions. The second, third, and fourth lines are always configured in the basic drawer of the DN20F-MA/MC. The sixth, seventh, and eighth lines are configured in the first backplane of the expansion drawer. The tenth, eleventh, and twelfth lines can be only configured in the second backplane of the expansion drawer. No more than twelve low-speed synchronous lines can be configured in any one DN20F front end configuration.

DMR11-*P

This is the high-speed synchronous line. The DMR11-** includes one high-speed DMR11-M module and one CK-DMR11-*D kit. Each drawer can have up to two DRM11-**s.

DMR11-AP — This includes the DMR11-M and the CK-DMR11-AD cabinet kit. 19.2 Kbps maximum (RS-232-C).

DMR11-BP — This includes the DMR11-M and the CK-DMR11-BD cabinet kit. 1 Mbps maximum CITT V.35 interface configuration.

DMR11-CP — This includes the DMR11-M and the CK-DMR11-CD cabinet kit. 1 Mbps maximum integral modem interface configuration.

DMR11-EP — This includes the DMR11-M and the CK-DMR11-ED cabinet kit. 1 Mbps maximum RS-422-A interface configuration.

DMR11-FP — This includes the DMR11-M and the CK-DMR11-FD cabinet kit. 19.2 Kbps maximum (RS-423-A).

(16) M7867 (DUP11-DA) (LOWEST ACCEPTABLE CS REV. F)
A FULLY CONFIGURED DN20 SUBSYSTEM WILL HAVE UP TO 12 M7867 (DUP11-DA) MODULES. THEIR ADDRESS AND VECTOR ASSIGNMENTS WILL BE ACCORDING TO THE FOLLOWING CHART.

DN20 CONFIGURATIONS (ADDRESS & VECTORS)

	#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12
DUP11 # 1 ADDRESS	760300	760300	760300	760300	760300	760300	760300	760300	760300	760300	760300	760300
VECTOR	570	570	570	570	570	570	570	570	570	570	570	570
# 2 ADDRESS	760310	760310	760310	760310	760310	760310	760310	760310	760310	760310	760310	760310
VECTOR	600	600	600	600	600	600	600	600	600	600	600	600
# 3 ADDRESS			760320	760320	760320	760320	760320	760320	760320	760320	760320	760320
VECTOR			610	610	610	610	610	610	610	610	610	610
# 4 ADDRESS				760330	760330	760330	760330	760330	760330	760330	760330	760330
VECTOR				620	620	620	620	620	620	620	620	620
# 5 ADDRESS					760340	760340	760340	760340	760340	760340	760340	760340
VECTOR					630	630	630	630	630	630	630	630
# 6 ADDRESS						760350	760350	760350	760350	760350	760350	760350
VECTOR						640	640	640	640	640	640	640
# 7 ADDRESS							760360	760360	760360	760360	760360	760360
VECTOR							650	650	650	650	650	650
# 8 ADDRESS								760370	760370	760370	760370	760370
VECTOR								660	660	660	660	660
# 9 ADDRESS									760400	760400	760400	760400
VECTOR									670	670	670	670
#10 ADDRESS										760410	760410	760410
VECTOR										700	700	700
#11 ADDRESS											760420	760420
VECTOR											710	710
#12 ADDRESS												760430
VECTOR												720

MR-0263

Address and Vector Assignments DUP11-FA Synchronous Line Unit
(Sheet 1 of 2)

Address and Vector Assignments DUP11-FA Synchronous Line Unit
(Sheet 2 of 2)

THERE ARE 2 SWITCH PACKS ON EACH M7867 (DUP11-DA) MODULE. THEIR SWITCH SETTINGS ARE AS FOLLOWS IN ORDER TO PROPERLY CONFIGURE THE ABOVE ADDRESS AND VECTOR ASSIGNMENTS.

DUP11 # 1		
PACK	SWITCH	STATE
E65	1	ON
E65	2	OFF
E65	3	ON
E65	4	ON
E65	5	ON
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	ON
E116	3	ON
E116	4	OFF
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 2		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	OFF
E65	5	OFF
E65	6	OFF
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	OFF
E116	3	ON
E116	4	ON
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 3		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	OFF
E65	5	OFF
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	OFF
E116	3	ON
E116	4	OFF
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 4		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	OFF
E65	5	ON
E65	6	OFF
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	OFF
E116	3	ON
E116	4	OFF
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 5		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	OFF
E65	5	ON
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	ON
E116	3	OFF
E116	4	OFF
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 6		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	ON
E65	5	OFF
E65	6	OFF
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	ON
E116	3	OFF
E116	4	OFF
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 7		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	ON
E65	5	OFF
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	OFF
E116	3	OFF
E116	4	OFF
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 8		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	ON
E65	5	ON
E65	6	OFF
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	OFF
E116	3	OFF
E116	4	OFF
E116	5	OFF
E116	6	ON
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 9		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	OFF
E65	4	ON
E65	5	ON
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	ON
E116	3	ON
E116	4	ON
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 10		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	ON
E65	4	OFF
E65	5	OFF
E65	6	OFF
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	ON
E116	3	ON
E116	4	ON
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 11		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	ON
E65	4	OFF
E65	5	OFF
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	OFF
E116	3	ON
E116	4	ON
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

DUP11 # 12		
PACK	SWITCH	STATE
E65	1	ON
E65	2	ON
E65	3	ON
E65	4	OFF
E65	5	ON
E65	6	OFF
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	OFF
E116	3	ON
E116	4	ON
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

THERE ARE 7 JUMPERS ON EACH M7867 (DUP11-DA) MODULE. THEY ARE ALL FACTORY SETTABLE FOR COMPATIBILITY WITH BELL 201, BELL 208 AND 209 SERIES MODEMS AND SHOULD NOT HAVE TO BE CHANGED UNLESS ANOTHER TYPE MODEM IS USED.

SHOULD ANOTHER TYPE MODEM BE USED THE JUMPERS MUST BE RE CONFIGURED SO THAT THEY ARE COMPATIBLE WITH THE TYPE MODEM USED. REFER TO THE DUP11-DA BIT SYNCHRONOUS INTERFACE MAINTENANCE MANUAL (EK-DUP11-M).

AS A QUICK VERIFY THE STANDARD FACTORY SETTABLE JUMPER SETTINGS ARE AS FOLLOWS:

W1	IN	W5	OUT
W2	OUT	W6	IN
W3	IN	W7	IN
W4	IN		

BR PRIORITY LEVEL 5 (PRIORITY JUMPER P/N 5408778)

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17) M8204 (KMC11) (LOWEST ACCEPTABLE CS REV. D)
A FULLY CONFIGURED DN20 SUB-SYSTEM WILL HAVE UP TO 3 M8204 (KMC11) MODULES. THEIR ADDRESS AND VECTOR ASSIGNMENTS WILL BE ACCORDING TO THE V
THE FOLLOWING CHART.

	KMC	#1	#2	#3	
KMC11 #1	ADDRESS VECTOR	760540 540	760540 540	760540 540	CONTROLS DUP11 #1 THRU 4
#2	ADDRESS VECTOR		760550 550	760550 550	CONTROLS DUP11 #5 THRU 8
#3	ADDRESS VECTOR			760560 560	CONTROLS DUP11 #9 THRU 12

THERE ARE TWO SWITCH PACKS ON EACH M8204 MODULE. THEIR SWITCH SETTINGS ARE AS FOLLOWS IN ORDER TO PROPERLY CONFIGURE THE ABOVE ADDRESS AND VECTOR ASSIGNMENTS.

KWC11 #1		
PACK	SWITCH	STATE
E65	1	OFF
E65	2	OFF
E65	3	ON
E65	4	ON
E65	5	OFF
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	ON
E116	3	OFF
E116	4	OFF
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

KWC11 #2		
PACK	SWITCH	STATE
E65	1	ON
E65	2	OFF
E65	3	ON
E65	4	ON
E65	5	OFF
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	OFF
E116	2	ON
E116	3	OFF
E116	4	OFF
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

KWC11 #3		
PACK	SWITCH	STATE
E65	1	OFF
E65	2	ON
E65	3	ON
E65	4	ON
E65	5	OFF
E65	6	ON
E65	7	N/A
E65	8	N/A
E116	1	ON
E116	2	OFF
E116	3	OFF
E116	4	OFF
E116	5	ON
E116	6	OFF
E116	7	ON
E116	8	ON
E116	9	ON
E116	10	ON

NOTE:
EACH BACKPLANE SLOT WHICH HAS AN M8204 (KMC11) MODULE INSTALLED MUST HAVE THE BACKPLANE WIRE FROM PIN CA1 TO PIN CB1 OF THAT SLOT REMOVED. SHOULD THE KMC11 EVER BE REMOVED FROM THAT SLOT THE WIRE MUST BE RE-INSERTED IN O ORDER TO GUARANTEE THAT THE NPG SIGNAL WILL BE PASSED ALONG THE UNIBUS.

THE ONLY SLOTS AFFECTED BY THIS IN THE DN20 ARE AS FOLLOWS:

DRAWER	BACKPLANE	SLOT =
BASIC (1134A)	DD11-PK	4
EXPANSION	BOTH DD11-DK BACKPLANES	2

BR PRIORITY LEVEL = 5 (PRIORITY JUMPER PN 5408778)

II) BACKPLANE CONFIGURATION INFORMATION

1) DD11-PK (LOWEST ACCEPTABLE REV. C)
ALL SLOTS WHICH HAVE NO QUAD OR HEX MODULE INSTALLED MUST HAVE A GRANT CONTINUITY CARD (G727) INSTALLED IN ROW "D" OF THAT SLOT.

2) DD11-DK (LOWEST ACCEPTABLE REV. B)
ALL SLOTS WHICH HAVE NO QUAD OR HEX MODULE INSTALLED MUST HAVE A GRANT CONTINUITY CARD (G727) INSTALLED IN ROW "D" OF THAT SLOT.

3) DD11-CK (LOWEST ACCEPTABLE REV. B)
ALL SLOTS WHICH HAVE NO QUAD OR HEX MODULES INSTALLED MUST HAVE A GRANT CONTINUITY CARD (G727) INSTALLED IN ROW "D" OF THAT SLOT.

4) DB11-A BACKPLANE (LOWEST ACCEPTABLE REV. E)
THERE ARE NO MODIFICATIONS NECESSARY TO THIS BACKPLANE.

MR-0126

Address and Vector Assignments KMC11-A as used in DN20/DN20F

THERE ARE 2 SWITCH PACKS ON EACH M8200-YA MODULE.
THEIR SWITCH SETTINGS ARE AS FOLLOWS IN ORDER
TO PROPERLY CONFIGURE THE ABOVE ADDRESS AND VECTOR ASSIGNMENT.

HIGH SPEED SYNCHRONOUS LINE NUMBER ONE		
E76	SWITCH	STATE
E76	1	ON
E76	2	ON
E76	3	ON
E76	4	OFF
E76	5	ON
E76	6	ON
E76	7	OFF
E76	8	N/A
E76	9	OFF
E76	10	N/A
E113	1	ON
E113	2	ON
E113	3	OFF
E113	4	OFF
E113	5	OFF
E113	6	OFF
E113	7	ON
E113	8	ON
E113	9	ON
E113	10	ON

HIGH SPEED SYNCHRONOUS LINE NUMBER TWO		
E76	SWITCH	STATE
E76	1	OFF
E76	1	OFF
E76	3	OFF
E76	4	ON
E76	5	ON
E76	6	ON
E76	7	OFF
E76	8	N/A
E76	9	OFF
E76	10	N/A
E113	1	OFF
E113	2 O	ON
E113	3	OFF
E113	4	OFF
E113	5	OFF
E113	6	OFF
E113	7	ON
E113	8	ON
E113	9	ON
E113	10	ON

HIGH SPEED SYNCHRONOUS LINE NUMBER THREE		
E76	SWITCH	STATE
E76	1	ON
E76	2	OFF
E76	3	OFF
E76	4	ON
E76	5	ON
E76	6	ON
E76	7	OFF
E76	8	N/A
E76	9	OFF
E76	10	N/A
E113	1	ON
E113	2	OFF
E113	3	OFF
E113	4	OFF
E113	5	OFF
E113	6	OFF
E113	7	ON
E113	8	ON
E113	9	ON
E113	10	ON

HIGH SPEED SYNCHRONOUS LINE NUMBER FOUR		
E76	SWITCH	STATE
E76	1	OFF
E76	2	ON
E76	3	OFF
E76	4	ON
E76	5	ON
E76	6	ON
E76	7	OFF
E76	8	N/A
E76	9	OFF
E76	10	N/A
E113	1	OFF
E113	2	OFF
E113	3	OFF
E113	4	OFF
E113	5	OFF
E113	6	OFF
E113	7	ON
E113	8	ON
E113	9	ON
E113	10	ON

MR-0127

SOFTWARE
The material for this section will be supplied at a later date.