EK-UDA50-UG-002

UDA50
USER GUIDE

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UDA50
USER GUIDE

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	MASSBUS	

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CHAPTER 1
INTRODUCTION

1.1 UDA50 DISK CONTROLLER

The UDA50 is a two-module disk controller that operates on the UNIBUS. It controls up to four Standard Disk Interconnect (SDI) disk drives. Each SDI disk drive is connected to the UDA50 by a separate shielded SDI cable. The basic configuration for the UDA50 Disk Subsystem is illustrated in Figure 1-1.

The operation of the UDA50 is controlled by two resident processors known as the U and the D processors. The U processor controls the interface between the UNIBUS and the UDA50 controller. The D processor controls the interface between the SDI disk drives and the UDA50 Disk Controller.

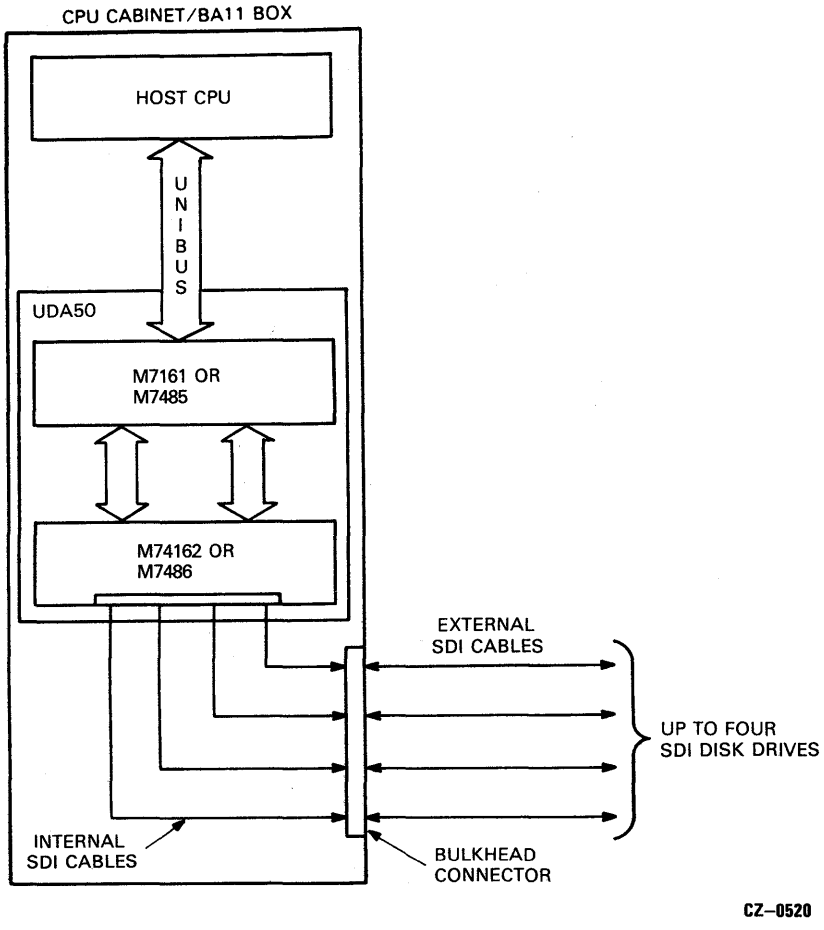

Figure 1-1 UDA50 Disk Subsystem Configuration

1.2 UDA50 UPGRADE

The UDA50 has been upgraded to increase its performance. The difference between the old UDA50 and the upgraded UDA50 will be called out in this manual where applicable.

1.3 UDA50 DIFFERENCES

The upgraded UDA50 consists of two new modules. Refer to Table 1-1. Some of the features which increase the performance of the new UDA50 are:

- Increased RAM size on the M7486 module from 4K to 16K.
- Minor hardware modification to make buffering easier.
- Etched-in capability to use larger PROMS.
- Selectable jumpers for UNIBUS delays, for various systems.

Table 1-1 UDA50 Modules

OLD UDA50 MODULES	NEW UDA50 MODULES
M7161	M7485
M7162	M7486

CAUTION

The new UDA50 M7485 and M7486 modules are not upward or downward compatible with the old UDA50 M7161 and M7162 modules. Under no circumstances should a new UDA50 module be used to replace a failing old UDA50 module unless both modules are replaced as a set.

1.4 MASS STORAGE CONTROL PROTOCOL

The UDA50 Disk Controller is a Mass Storage Control Protocol (MSCP) device. MSCP is a communication protocol used with intelligent mass storage controllers. MSCP hides device-dependent requirements, such as disk geometry and error recovery strategies, from the host. It thus enables several different device drivers to be replaced by one class driver.

A detailed description of the Mass Storage Control Protocol is provided in the *MSCP Basic Disk Functions Manual* (AA-L619A-TK).

1.5 UDA50 SPECIFICATIONS

The UDA50 Disk Controller Specifications are described in Table 1-2 and 1-3.

Table 1-2 Old UDA50 Specifications

Characteristics	Specification
Physical components	UDA module #1 (M7161-YA) UDA module #2 (M7162) 50-pin flat cable assembly 40-pin flat cable assembly SDI cable assembly I/O bulkhead assembly
Power consumption	80 watts nominal
Heat dissipation	Approximately 256 Btu/hour
Electrical voltage and current requirements	11 amps at +5 volts 60 millamps at +15 volts 2 amps at —15 volts
Operating temperature range	10° C to 40° C (5° F to 109° F) with a temperature gradient of 20° C/hour (36° F/hour)
Operating relative humidity range	10% to 90% with a wet bulb temperature of 28° C (82° F) and a minimum dew point of 2° C (36° F)
Operating altitude range	Sea level to 2400 meters (8000 ft). Derate the maximum allowable operating temperature by 1.8° C/1000 meters (1° F/1000 feet) for operation above sea level
Mounting restrictions	Mounts in two hex-height UNIBUS SPC slots in the following UNIBUS and VAX mounting boxes: BA11-A BA11-K BA11-L

Table 1-3 New UDA50 Specifications

Characteristics	Specifications
Physical components	UDA module 1 (M7485) UDA module 2 (M7486) 50-pin flat cable assembly 40-pin flat cable assembly SDI cable assembly I/O bulkhead assembly
Power consumption	83 watts nominal
Heat dissipation	Approximately 256 Btu/hour
Electrical voltage and current requirements	12 amps at +5 volts 60 millamps at +15 volts 1.4 amps at —15 volts
Operating temperature range	10° C to 40° C (50° F to 109° F) with a temperature gradient of 20° C/hour (36° F/hour)
Operating relative humidity range	10% to 90% with a wet bulb temperature of 28° C (82° F) and a minimum dew point of 2° C (36° F)
Operating altitude range	Sea level to 2400 meters (8000 ft). Derate the maximum allowable operating temperature by 1.8° C/1000 meters (1° F/1000 feet) for operation above sea level
Mounting restrictions	Mounts in two hex-height UNIBUS SPC slots in the following UNIBUS and VAX mounting boxes: BA11-A BA11-K BA11-L

1.6 RELATED DOCUMENTATION

The UDA50 Disk Controller related documentation is listed below.

Documentation is available from the Printing and Circulation Services, 444 Whitney St., Northboro, Massachusetts 01532.

- *UDA50 Disk Controller User Guide* (EK-UDA50-UG)
- *UDA50 Disk Controller Service Manual* (EK-UDA50-SV)

Documentation is available from the Software Distribution Center Order Administration/Processing, 20 Forbes Rd., Northboro, Massachusetts 01532.

- *UDA50 Field Maintenance Print Set* (MP-01331)
- *UDA50 Programmer's Documentation Kit* (QP905-GZ) - This kit consists of the following three software manuals.
  - *MSCP Basic Disk Function Manual* (AA-L619A-TK)
  - *Storage System Diagnostic and Utilities Protocol* (AA-L620A-TK)
  - *Storage System UNIBUS Port Description* (AA-L621A-TK)
- *UDA50 Maintenance Documentation Kit* (QP904-GZ) - This kit consists of a small looseleaf binder, the *UDA50 Maintenance Guide* , and the current drive maintenance guides that operate on the UDA50.
  - *UDA50 Maintenance Guide* (AA-M185B-TC) - The above maintenance guide is a 6¾ × 4 inch looseleaf.
  - *RA80 Maintenance Guide* (AA-M186A-TC) - The above maintenance guide is a 6¾ × 4 inch looseleaf.
  - *RA8l Maintenance Guide* (AA-M879A-TC) - The above maintenance guide is a 6¾ × 4 inch looseleaf.
  - *Maintenance Guide Looseleaf Binder* (AV-L980A-TK)

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

The installation procedure for the UDA50 Disk Controller requires the insertion of two hex-height modules into a UNIBUS backplane. If the UDA50 Disk Controller is to control disk drives located outside the same cabinet that the controller is in, then an I/O bulkhead assembly must be mounted on the rear of the CPU cabinet. SDI cables must be connected between the UDA50 Disk Controller and the I/O bulkhead assembly and from the I/O bulkhead to each disk drive. Figure 2-1 gives an illustrated parts breakdown of the UDA50 assembly.

Use the following checklist to perform the UDA50 installation. The list indicates the paragraph number where each procedure is described.

- Join the CPU cabinet to the drive cabinet (2.2) _____
- Check the I/O page address switches and jumpers (2.3.1) _____
- Check the UDA50 priority plug (2.3.4) _____
- Insert and clamp the SDI cable to J4 (2.3.5) _____
- Select the backplane slot (2.3.6) _____
- Prepare the backplane slot (2.3.70 _____
- Insert the UDA50 modules (2.3.8) _____
- Install two flat ribbon cables (2.3.9) _____
- Install the I/O bulkhead connector (2.3.9.1) _____
- Install the internal SDI cable to the I/O bulkhead (2.3.9.3) _____
- Install the external SDI cable to the I/O bulkhead (2.3.9.4) _____
- Install the bootstrap ROM (2.4) _____
- Perform the field acceptance test (2.5) _____

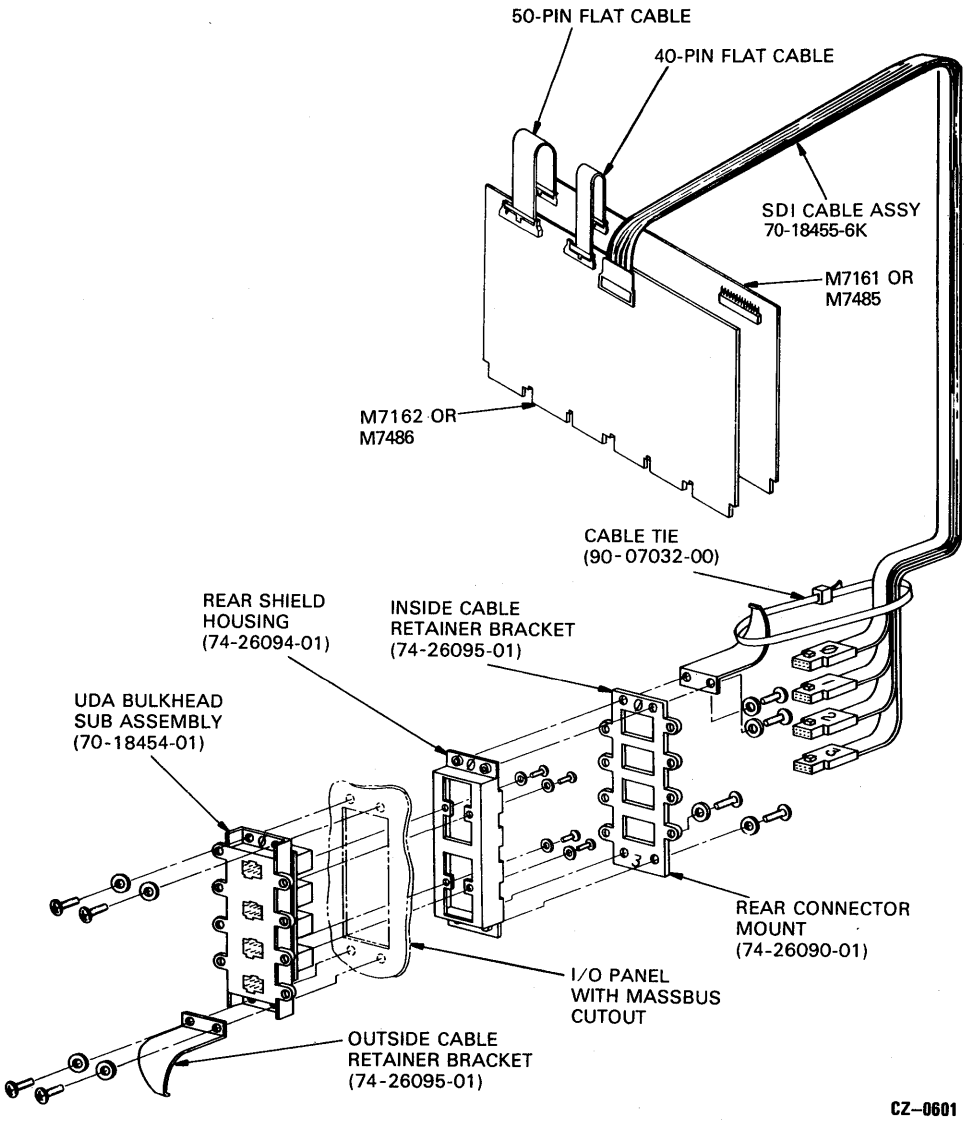

Figure 2-1 UDA50 Illustrated Parts

2.2 CABINET JOINING PROCEDURE

The disk drives that operate with the UDA50 Disk Controller come in an H9642 cabinet with a joiner panel. The joiner panel allows the disk drive cabinet to be joined to the cross-product CPU cabinet in which the UDA50 is located. Figure 2-2 shows how two cross-product cabinets are joined. Use the following procedure to join cross-product cabinets.

1. Open the front door of the CPU cabinet. If the CPU cabinet does not have a front door, remove the lowest front filler panel to expose the end panel lock shown in Figure 2-3.

2. Remove the front left-end panel lock from the CPU cabinet.

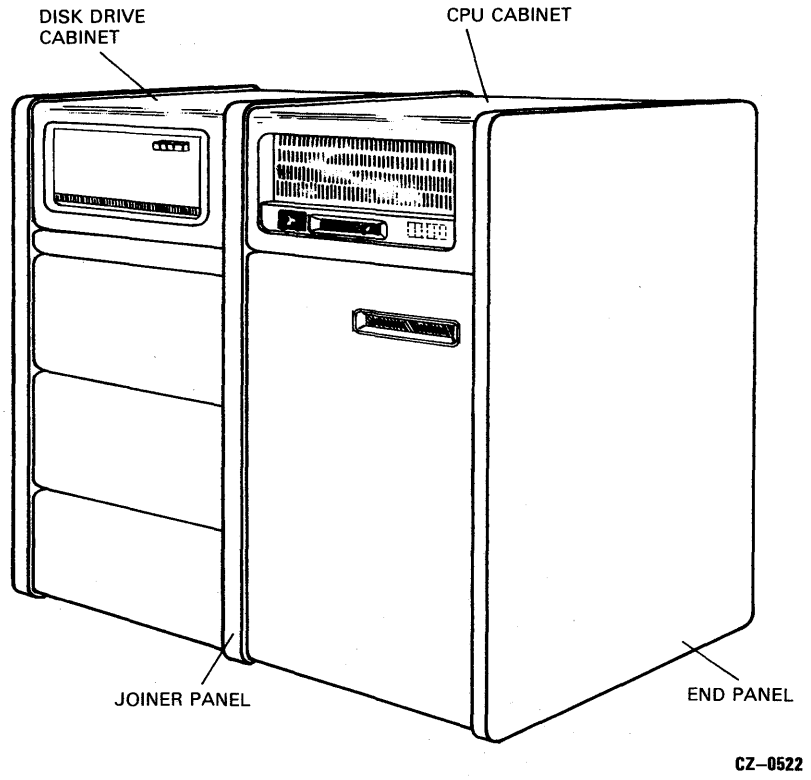

Figure 2-2 Joining Cross Product Cabinets

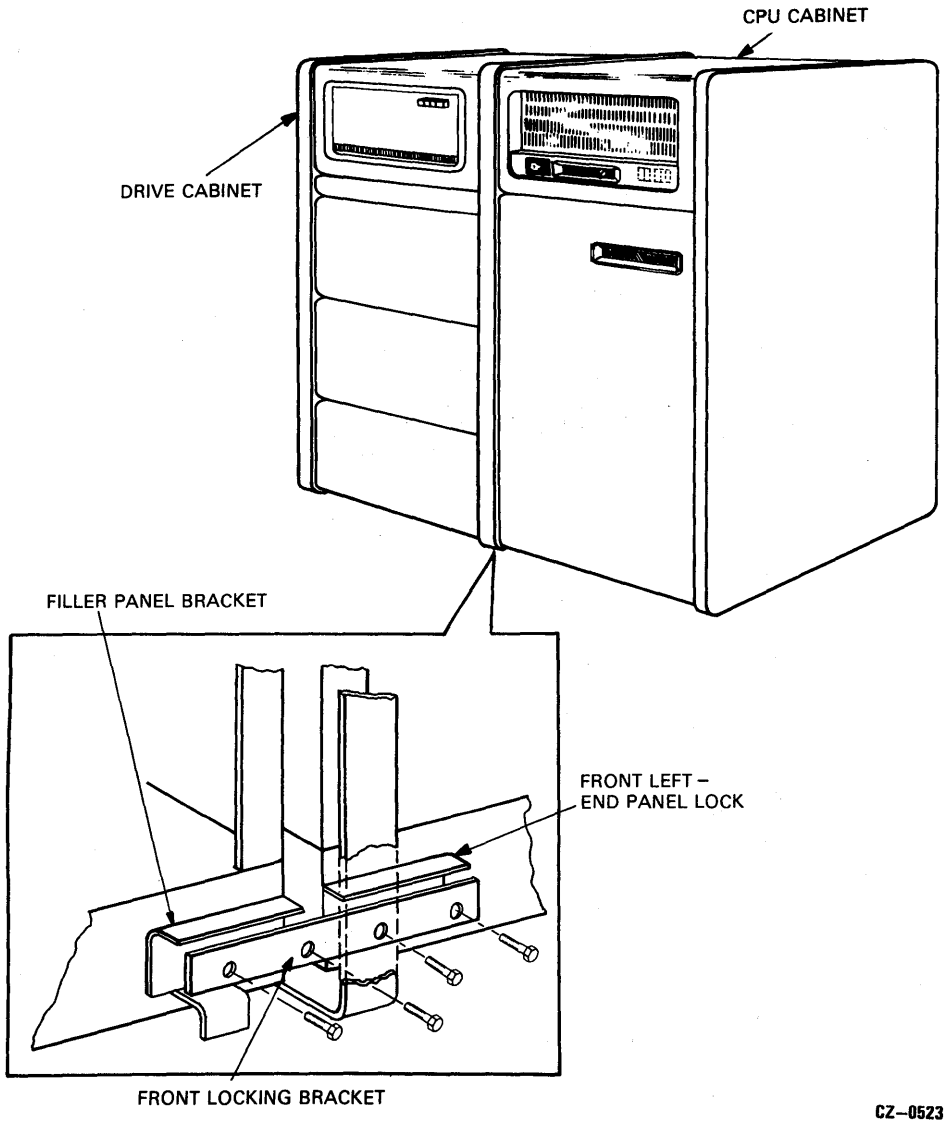

Figure 2-3 Removing Front End Panel Lock

3. Open the rear door of the CPU cabinet.

4. Loosen the screws that secure the right rear-end panel lock. Refer to Figure 2-4.

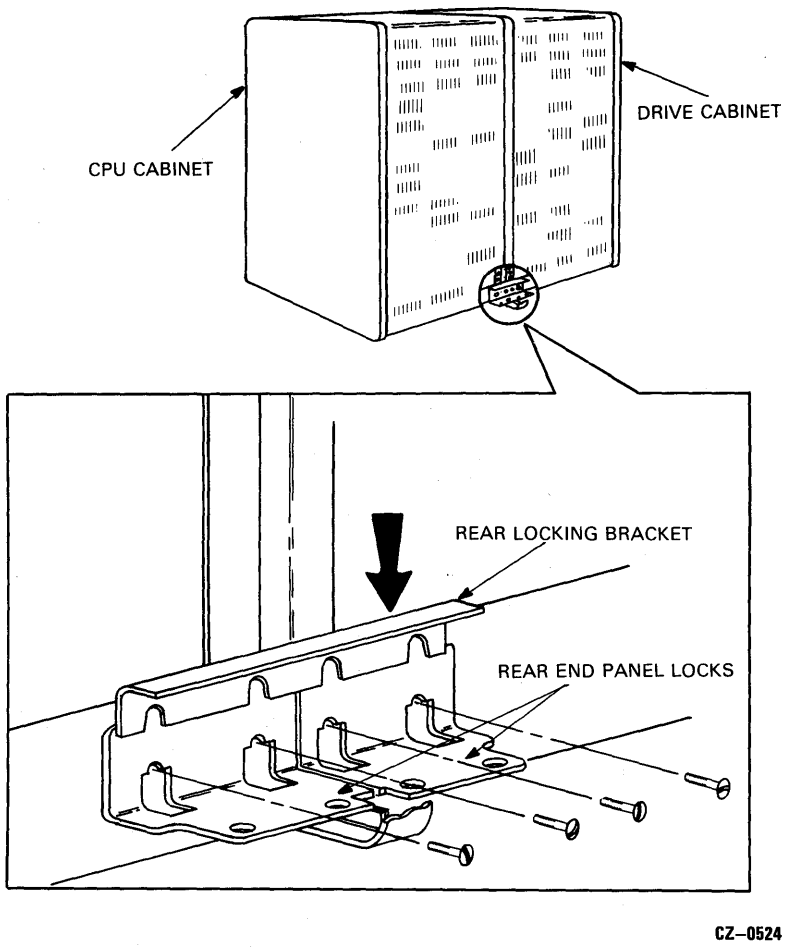

Figure 2-4 Removing Rear End Panel Lock

5. Remove the CPU cabinet end panel and its ground strap, if there is one.

6. Remove the two lower key buttons from the left side of the CPU cabinet uprights. These are removed by unscrewing the Phillips head screws in their center. Refer to Figure 2-5.

7. Slide the two cabinets together and engage the top two key buttons on the CPU cabinet in the keyhole slots on the drive cabinet joiner panel. Adjust the cabinets until their fronts are flush. Refer to Figures 2-5 and 2-6.

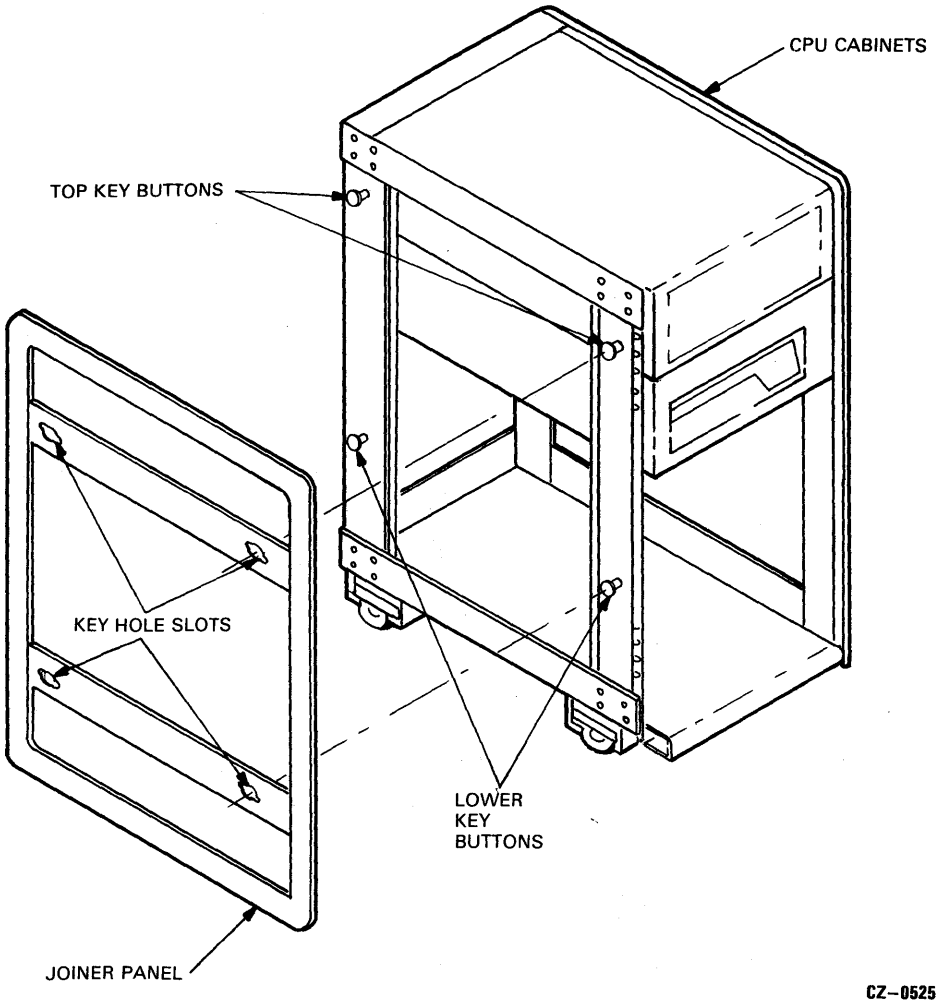

Figure 2-5 Removing Lower Key Buttons

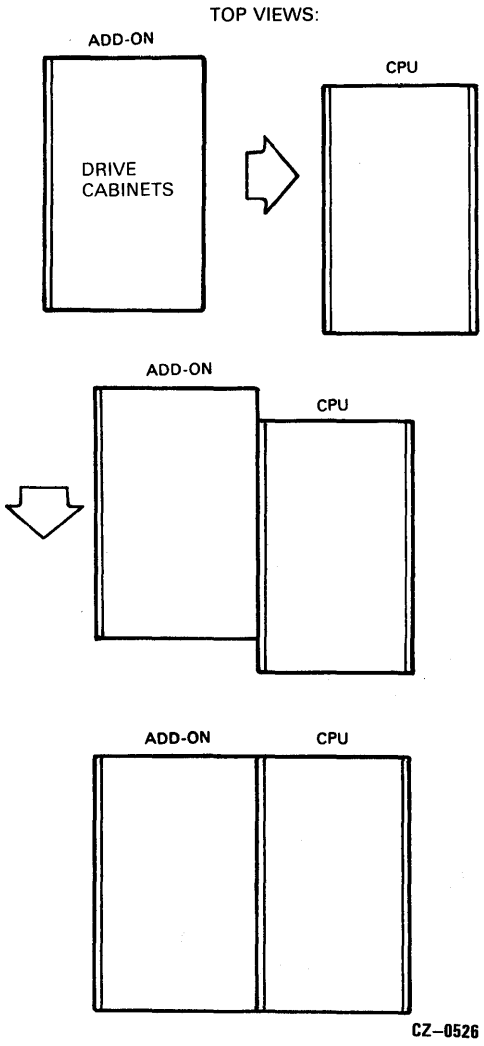

Figure 2-6 Joining the Cabinets

8. Remove the bottom front filler panel from the disk drive cabinet by removing the two screws at its base. Refer to Figure 2-7.

9. Remove the front right filler panel bracket from the disk drive cabinet.

10. Place the front locking bracket over the filler panel bracket and end panel lock as shown in Figure 2-3. Then bolt the two cabinets together with the existing hardware.

11. Open the rear door of the disk drive cabinet and loosen the screws that secure the rear left-end panel lock. Refer to Figure 2-4.

12. Slide the rear locking bracket over the end panel locks as shown in Figure 2-4. Then tighten the four screws.

13. Install the end panel that was removed from the left side of the CPU cabinet onto the left side of the drive cabinet. If an end panel is needed for drives in cross product cabinets, order part number H9544-AA. Be sure to reattach any ground straps to the end panel that might have been removed.

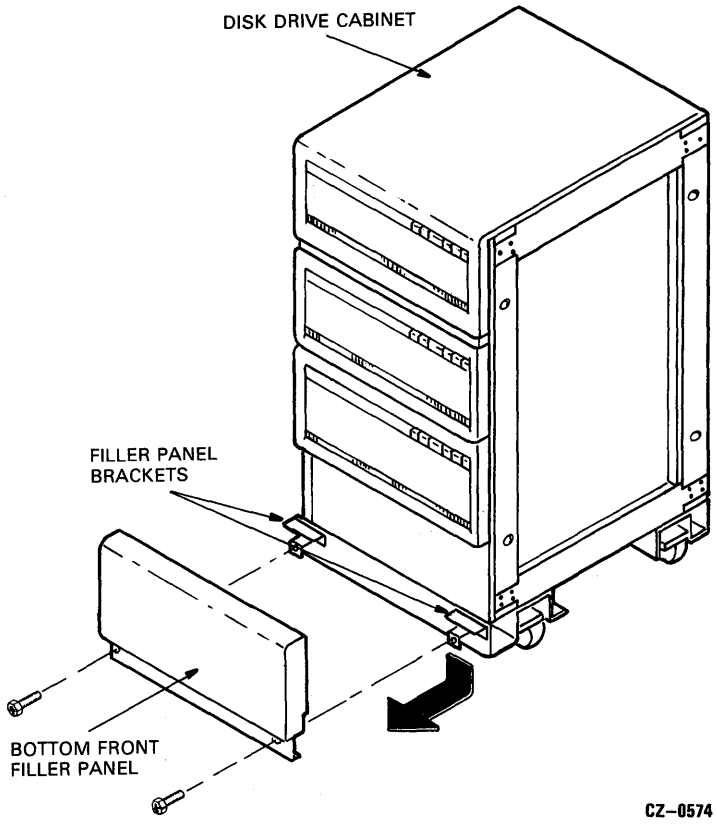

Figure 2-7 Removing the Filler Panel Brackets

2.3 MODULE PREPARATION AND INSTALLATION

The following paragraphs describe how to install the UDA50 modules, I/O bulkhead, and cables once the CPU and disk drive cabinets have been joined.

2.3.1 I/O Page Address Switches and Jumpers

The UDA50 Disk Controller contains two registers that are visible to the I/O page. They are the initializing and polling (IP) register and the status and address (SA) register. The IP and SA registers are assigned an octal UNIBUS address of 772150 and 772152, respectively.

The UNIBUS address selector switches and jumper plugs W4 and W5 are used to set the UNIBUS address for the IP register. The location of these switches and jumpers on UDA50 module (M7161) is shown in Figures 2-8A and 2-8B. The location of these switches and jumpers on UDA50 module (M7485) is shown in Figure 2-8A. Set the UNIBUS address switches and jumpers for both modules to the positions shown in Figure 2-9 to select UNIBUS address 772150.

In past disk products, a vector address was also physically selectable. This is not true with the UDA50 Disk Controller. A vector address of 154 (octal) will be supplied by the software.

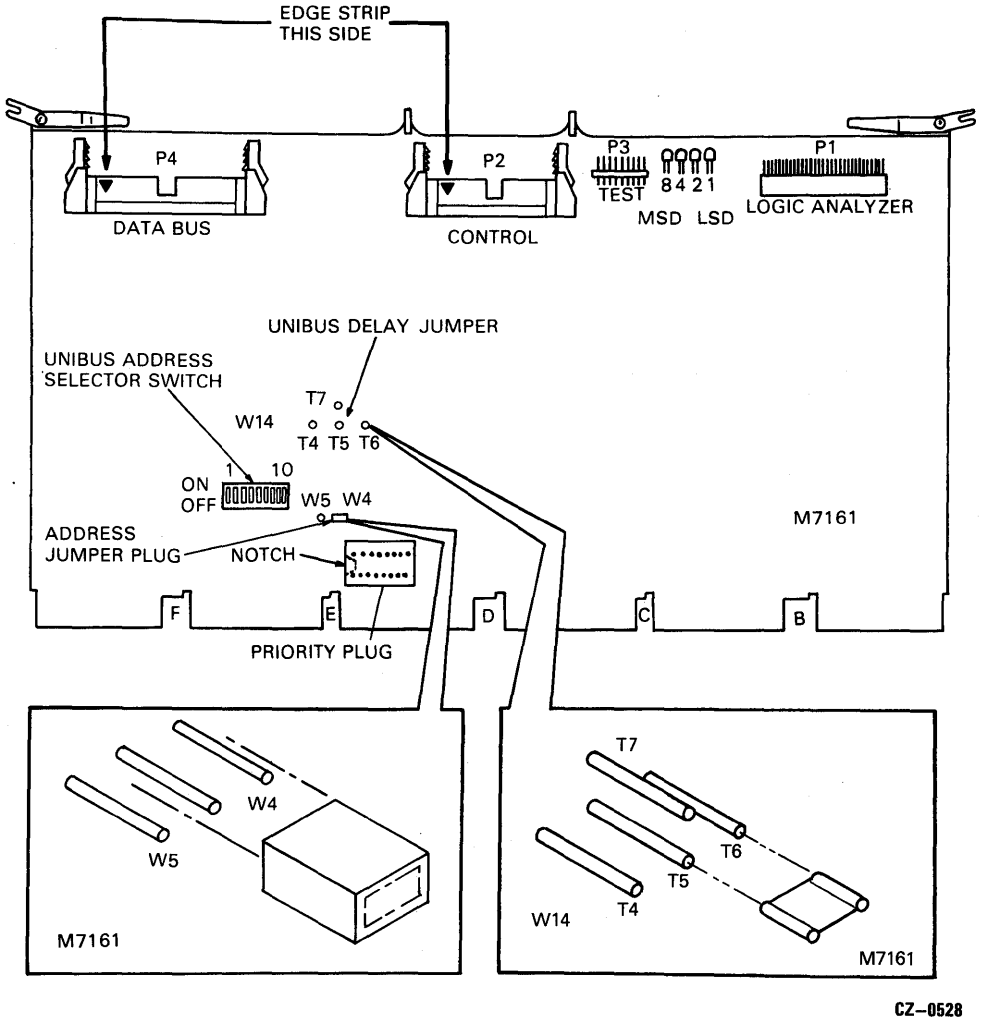

Figure 2-8A M7161 UNIBUS Address Switch and Jumper Locations

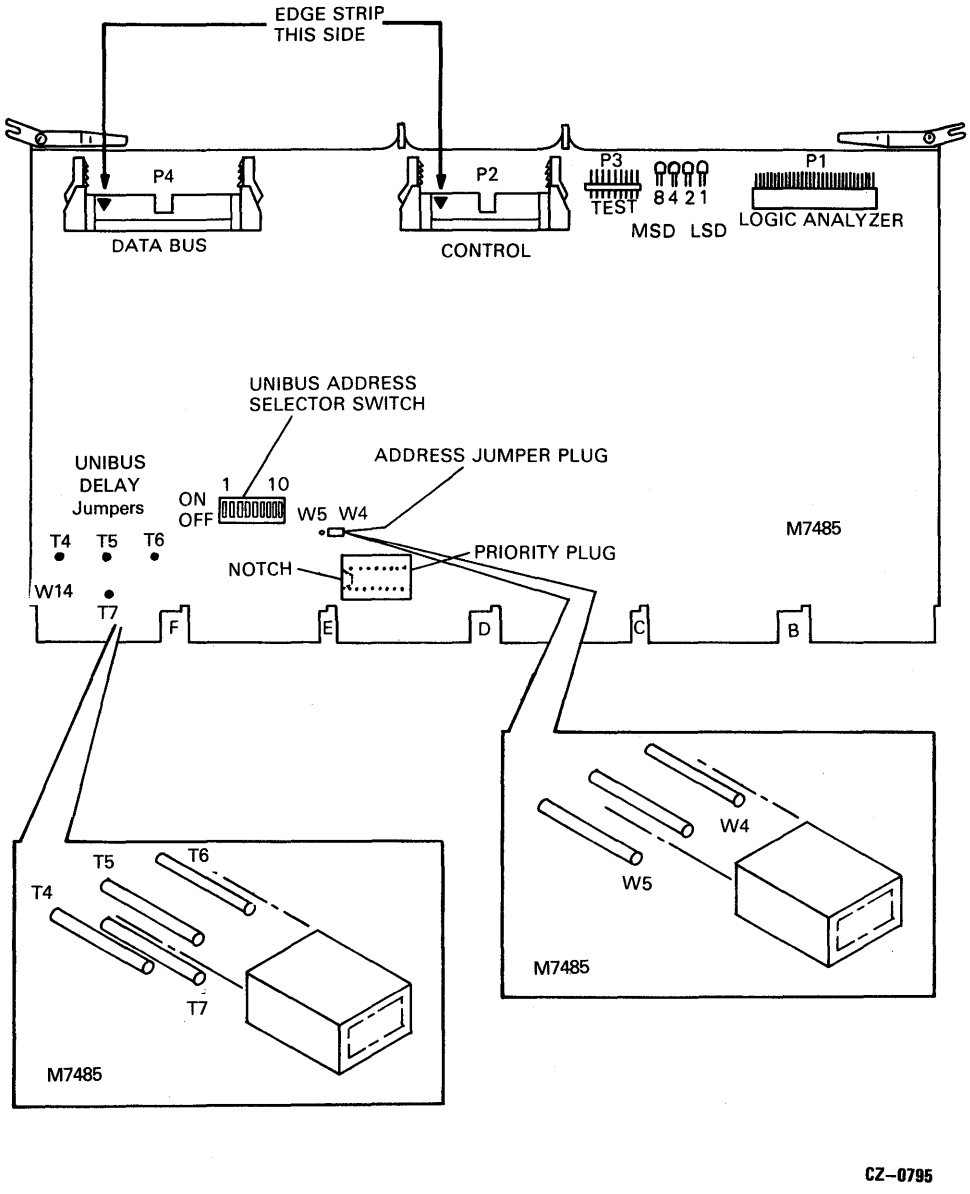

Figure 2-8B M7485 UNIBUS Address Switch and Jumper Locations

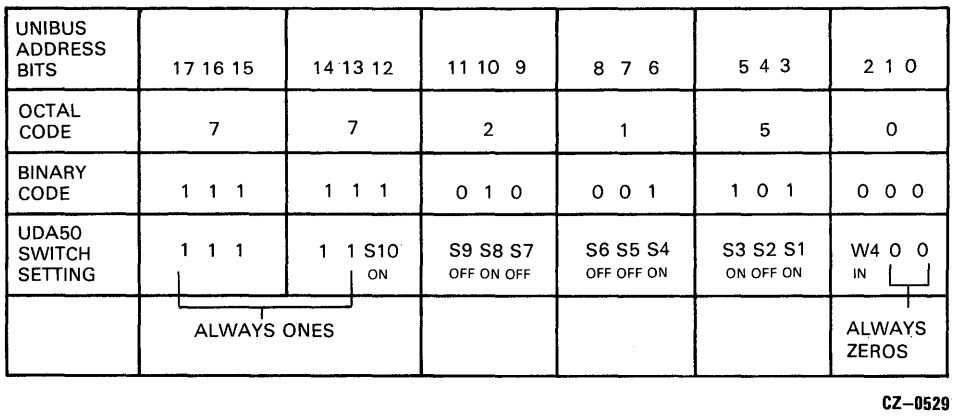

Figure 2-9 UDA50 Switch Setting for Address 772150

NOTE

UNIBUS address bit 2 is selected by jumper plugs W4 and W5. Only one jumper plug can be in place at a time. When jumper W4 is IN, bit 2 equals 0. When jumper W5 is IN, bit 2 equals 1.

NOTE

The UNIBUS address switches and jumpers should be set for a floating address when a second UDA50 is installed on a system. Check the system configuration and UNIBUS addresses of all devices already installed.

2.3.2 UNIBUS Overloading

A set of jumpers has been inserted on both the M7161 and M7485 modules to prevent UNIBUS overloading. The location of these jumpers on UDA50 module (M7161) is shown in Figure 2-8A. The location of these jumpers on UDA50 module (M7485) is shown in Figure 2-8B. Table 2-1 shows the amount of delay, jumper configuration, and system configuration.

Table 2-1 UNIBUS Delay

Amount of Delay	Jumper Config.	Type of System
0 usec	T4-T5	UDA installed and the only other disk drive is a RL02 or a RK07 (11/70 system with a RK07 and 1mb DMR will not work *)
6.2 usec	T5-T6	UDA installed with multiple DMR11s or DMC11s or DZ11s
		11/44 system (or any other PDP-11 with ECC memory) using RM02 or RP04/05/06 disk drives
		11/44 with RL02 or RK07 disk drives

Table 2-1 UNIBUS Delay (Cont)

Amount of Delay	Jumper Config.	Type of System
		11/24 system (or any other PDP-11 with non-ECC memory) with 1 or 2 UDAs installed with other disk controllers and a DZ11 VAX systems should be treated as an 11/24 for UNIBUS configuration UDA installed on the UNIBUS with one or more real time data acquistion devices, and real time data overrun or underflow is observed †
10 usec	T5-T7	11/44 system with RL02 and RK07 disk drives 11/70 system with a UDA/RL02/DMR11 (1mb) mix

* The UDA/RK07/DMR11 configuration gives data late errors from the RK07 regardless of the UDAs jumper setting. Because of this, either an RK07 or a UDA, but not both can be configured on the 11/70 when a 1mb DMR11 is present.

† If underflow or overrun conditions are observed after setting the UDAs jumper to the 6.2 usec. position, the UDA's jumper must be set to the 10 usec. position (T5-T7).

2.3.3 UNIBUS Overload Exceptions

There are exceptions to using the UNIBUS delay in preventing overload and the number of UDAs that can be installed on a system. They are:

1. The UDA should not be installed on a UNIBUS system which has a bus repeater because the repeater slows the UNIBUS. Other devices such as RK07, RM02, and RP04/05/06 may also experience data late conditions.

2. The UDA must be installed after all non-buffered devices on the UNIBUS.

3. On PDP-11 systems, there may be no more than two UDAs installed on a UNIBUS. However on VAX systems, no more than one UDA should be installed on a UNIBUS with non-buffered UNIBUS peripheral devices.

NOTE

The old UDA50 M7161 module has the UNIBUS delay jumpers installed starting with M7161 module revision E. Check this module and its delay jumpers if you are having UNIBUS overload problems.

2.3.4 UDA50 Priority Plug

All UDA50 M7161 or M7485 modules are shipped with a level 5 priority plug. This is the recommended priority level for UDA50 Disk Subsystems and thus, the priority plug need not be changed for the majority of installations. If another priority level is required in some special circumstance, then the current priority plug must be removed and the new one inserted. The location of the priority plug is shown in Figures 2-8A and 2-8B. It should be inserted so that the notch on the priority plug aligns with the hole on the module socket.

2.3.5 SDI Cable Installation

Insert plug P4 of the internal SDI cable assembly into connector J4 on UDA50 module M7162 or M7486 as shown in Figure 2-10. Slide the cable retainer over connector J4 until the connector protrudes through the plastic cutout. The cable retainer should lock the SDI cable in place.

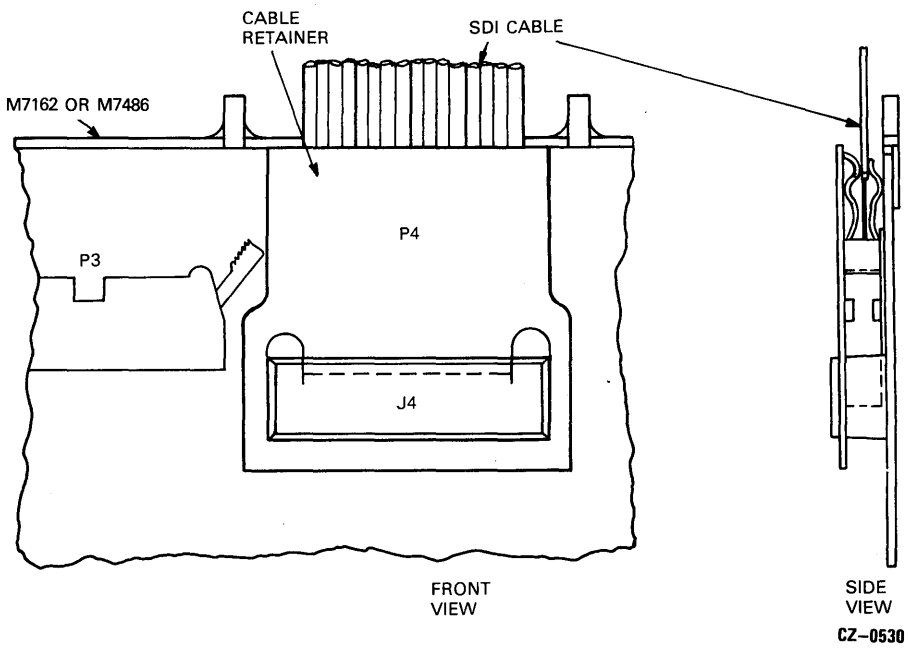

Figure 2-10 M7162 or M7486 SDI Cable Assembly Installation

2.3.6 UNIBUS Backplane SPC Slots

The UDA50 Disk Controller will operate in either the standard UNIBUS or modified UNIBUS hex-height small peripheral connector (SPC) slots. Locate two adjacent empty SPC slots for the two UDA50 modules. Illustrations of the UNIBUS backplanes and pin assignments are shown in Figures 2-11 and 2-12, respectively.

The early SPCs did not utilize direct memory access (DMA) data transfers to and from memory; therefore, the signals now used for this purpose are not part of the original SPC pin assignments. Newer options, such as the UDA50 Disk Controller, do utilize DMA transfers. There is a new pin assignment called SPC PRIME that includes these signals. Refer to Figure 2-13. If the UDA50 Disk Controller is used in an older (non-SPC PRIME) slot, it is then necessary to make sure that the signals shown in Table 2-2 are wired on the backplane.

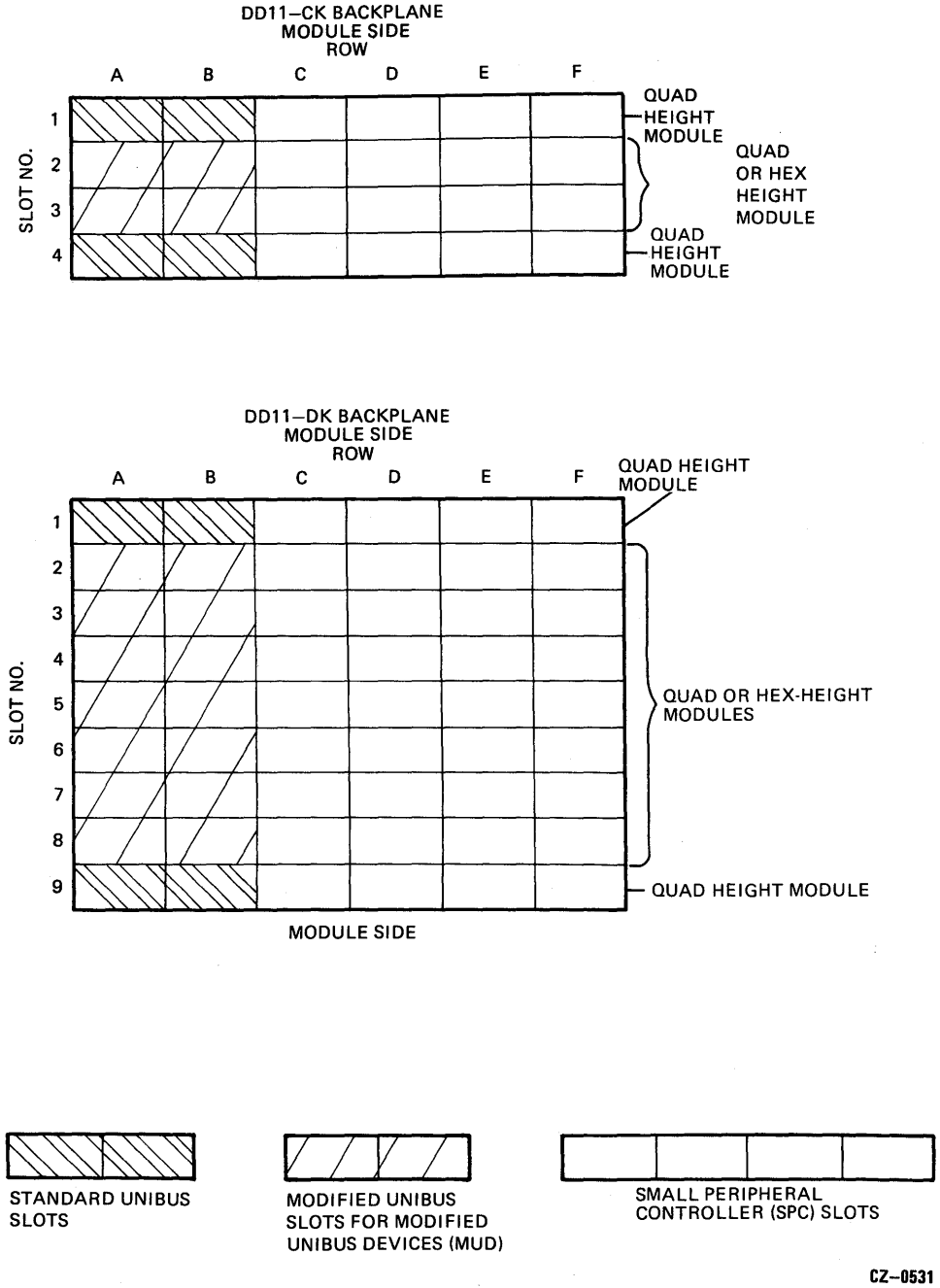

Figure 2-11 Optional Backplane Slot Assignments

STANDARD UNIBUS PIN DESIGNATIONS

Side / Pin	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	BG6 H	+5V
B	INTR L	GND	BG5 H	GND
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	GND	BR4 L
E	D04 L	D03 L	GND	BG4 H
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	GND	PB L	A11 L	A10 L
P	GND	BBSY L	A13 L	A12 L
R	GND	SACK L	A15 L	A14 L
S	GND	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	NPG H	BR6 L	SSYN L	C0 L
V	BG7 SO	GND	MSYN L	GND

MODIFIED UNIBUS PIN DESIGNATIONS

SIDE / PIN	ROW A 1	ROW A 2	ROW B 1	ROW B 2
A	INIT L	+5V	RESV PIN	+5V
B	INTR L	TP	RESV PIN	TP
C	D00 L	GND	BR5 L	GND
D	D02 L	D01 L	+5 BAT	BR4 L
E	D04 L	D03 L	INT SSYN	PAR DET
F	D06 L	D05 L	AC LO L	DC LO L
H	D08 L	D07 L	A01 L	A00 L
J	D10 L	D09 L	A03 L	A02 L
K	D12 L	D11 L	A05 L	A04 L
L	D14 L	D13 L	A07 L	A06 L
M	PA L	D15 L	A09 L	A08 L
N	PAR P1	PB L	A11 L	A10 L
P	PAR P0	BBSY L	A13 L	A12 L
R	+15 BAT	SACK L	A15 L	A14 L
S	-15 BAT	NPR L	A17 L	A16 L
T	GND	BR7 L	GND	C1 L
U	+20 (CORE)	BR6 L	SSYN L	C0 L
V	+20 (CORE)	+20 (CORE)	MSYN L	-5 (CORE)

NOTE: INDICATES A REDESIGNATED PIN.

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Figure 2-12 Standard and Modified Backplane Pin Assignments

	ROW C		ROW D		ROW E		ROW F	
SIDE / PIN	1	2	1	2	1	2	1	2
A	NPG (IN)	+5V	TP	+5V	GND A	+5V	ABG OUT	+5V
B	NPG (OUT)	-15V	TP	-15V	ASSYN IN H	-15V	ABG IN	-15V
C	PA L	GND	A SEL 6	GND	A12 L	GND	SSYN L	GND
D	LTC	D15 L	A OUT LOW	BR7 L	A17 L	A15 L	BBSY L	FO1 N1
E	TP	D14 L	A SEL 4	BR6 L	MSYN L	A16 L	FO1 V2	D02 L
F	TP	D13 L	A SEL 0	BR5 L	A02 L	C1 L	D05 L	D06 L
H	D11 L	D12 L	A IN	BR4 L	A01 L	A00 L	D07 L	A INT ENB B
J	A INT B	D10 L	A SEL 2	A BR OUT	SSYN L	C0 L	NPR L	GND A
K	TP	D09 L	A OUT	BG7 SO	A14 L	A13 L	D08 L	A INT B
L	A INT ENBB	D08 L	INIT L	BG7 OUT	A11 L	TP	D03 L	FO1 L2
M	TP	D07 L	AINT ENBA	BG6 SO	AIN	AOUT HIGH	INTR L	FO1 M2
N	DC LO	D04 L	A INT A	BG6 OUT	A OUT LOW	A08 L	FO1 N1	D04 L
P	HALT REQ	D05 L	TP	BG5 S0	A10 L	A07 L	ABR OUT	FO1 P2
R	HALT GRT	D01 L	TP	BG5 OUT	A09 L	ASEL 4	FO1 L2	FO1 N1
S	PB L	D00 L	TP	BG4 S0	ASEL 6	ASEL 0	FO1 M2	FO1 P2
T	GND	D03 L	GND	BG4 OUT	GND	ASEL 2	GND	SACK L
U	+15	D02 L	TP	ABG IN	A06 L	A04 L	A INT A	ABR OUT
V	AC LO	D06 L	ASSYN IN H	ABG OUT	A05 L	A03 L	A INT ENB A	FO1 FO1

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Figure 2-13 SPC PRIME Backplane Pin Assignments

Table 2-2 Backplane Signal Checks

Backplane Pins	Signal Names	Used On
Pin CA1	NPG IN	M7161 or M7485
Pin CB1	NPG OUT	M7161 or M7485
Pin FJ1	NPR	M7161 or M7485
Pin CV1	AC LO1	M7161 or M7485
Pin CU1	+15V	M7162 or M7486

2.3.7 UNIBUS Backplane Slot Preparation

If the slot has SPC PRIME pinning, the NPG jumper will have to be removed. The NPG line is the UNIBUS grant line for devices that perform data transfers without processor intervention. Continuity of the NPG line is provided by wirewrap jumpers on the backplane. When an NPR device is placed in a slot, the corresponding jumper wire from pin CA1 to pin CB1 of that slot must be removed. The routing of the NPG signal through the backplane is shown in Figure 2-14. Grant priority decreases from slot 1 to slot 9 (slot 1 has the highest priority).

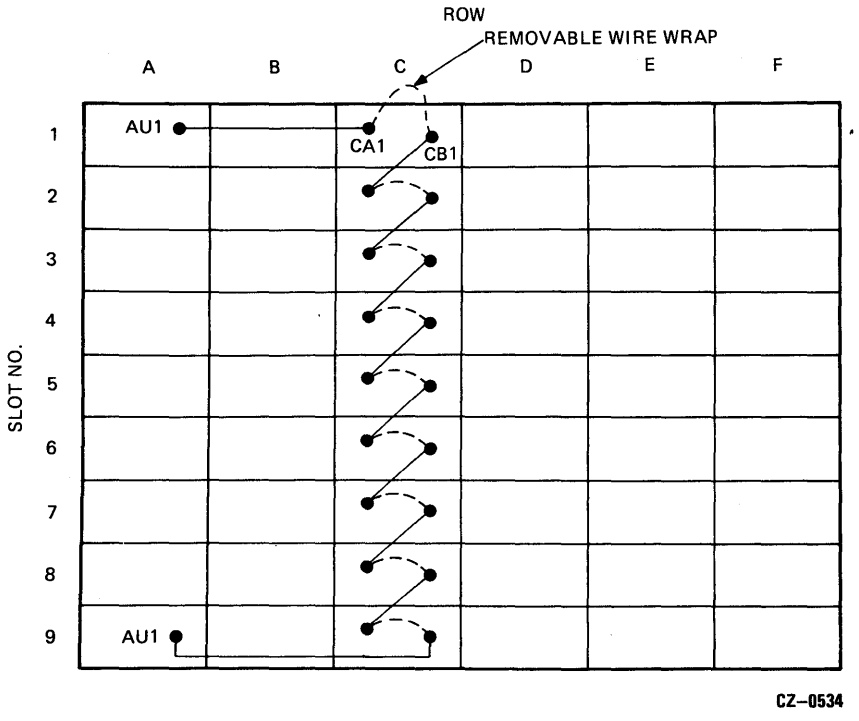


Figure 2-14 NPG Jumper Lead Routing

The NPG jumper must be removed from the slot that will be occupied by UDA50 module M7161 or M7485. Module M7161 or M7485 will not operate with the NPG jumper in place. The NPG jumper may also be removed from the slot occupied by the second UDA50 Module, M7162 or M7486, since the module will provide continuity on the NPG line. Module M7162 or M7486 will operate whether or not the NPG jumper is in place. If both NPG jumpers are removed from these two module slots, the module location can be interchanged and the UDA50 will still operate. However, remember that the NPG continuity line will be interrupted whenever Module M7162 or M7486 is removed.

NOTE
If an NPR device is removed from a slot, the jumper wire from pin CA1 to pin CB1 must be reconnected.

The bus grant lines (BG4 through BG7) for devices requiring processor intervention during data transfers are routed through each small peripheral control section in slot D. Each of the four grant signals is routed on a separate line. Grant priority for each level decreases from slot 1 to slot 9.

A bus grant jumper card (G727, G7270, or G7271) must be placed in connector D of any unoccupied SPC section. If an SPC section is left open, bus grant continuity will be lost.

2.3.8 UDA50 Module Insertion

Insert the two UDA50 modules into the two adjacent SPC slots prepared for them. The two modules may be inserted in any order if the NPG jumpers have been removed from both SPC slots. Otherwise, make sure that module M7161 or M7485 is in the SPC slot without the NPG jumper.

2.3.9 Flat Ribbon Cable Installation

The two UDA50 hex-height modules must be interconnected by two 4 inch long flat ribbon cables as shown in Figure 2-15. The outer cable is a 50-conductor flat ribbon cable which connects M7162 or M7486 (P1) to M7161 or M7485 (P4). The inner cable is a 40-conductor flat ribbon cable which connects M7162 or M7486 (P3) to M7161 or M7485 (P2).

The order in which the two UDA50 modules are inserted into the backplane does not matter to these cables. Install the cables so that the arrows on the plugs align with the sockets. The edge stripe on the cables is on the same edge as the arrow.

2.3.9.1 I/O Bulkhead Connector Installation – An I/O bulkhead connector must be installed on the I/O panel at the rear of the CPU cabinet. The I/O bulkhead provides a feedthrough connection for all SDI cables leaving the CPU cabinet. Figure 2-16 shows the location of the I/O panel on a PDP-11/44 cabinet. Other CPU cabinets use this same I/O panel. If no I/O panel is available, refer to Paragraph 2.3.9.5 (Alternate SDI Cable Installation). On the I/O panel are three wide cutouts intended for MASSBUS cable use. The location of these three MASSBUS cable cutouts is also shown in Figure 2-16. Select any empty MASSBUS cable cutout to mount the I/O bulkhead connector. Once an empty MASSBUS cable cutout is found, use the following procedure to install the I/O bulkhead.

1. Install the UDA bulkhead sub-assembly and its outside cable retainer bracket as shown in Figure 2-17. Connector number 0 on the bulkhead should be on the top. Four screws and lock washers are used for mounting.

2. Install the rear shield housing next. Connector number 0 should be on the top. Four screws and lock washers are used for mounting.

3. Install the rear connector mount and the inside cable retainer bracket next. Again, connector number 0 should be on the top.

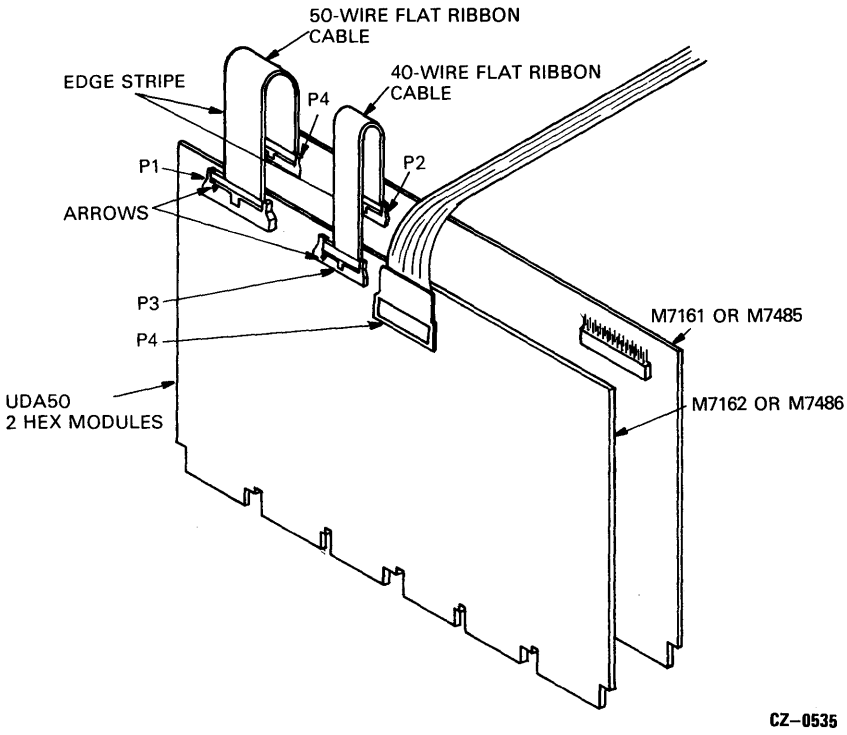


Figure 2-15 UDA50 Intermodule Flat Ribbon Cables

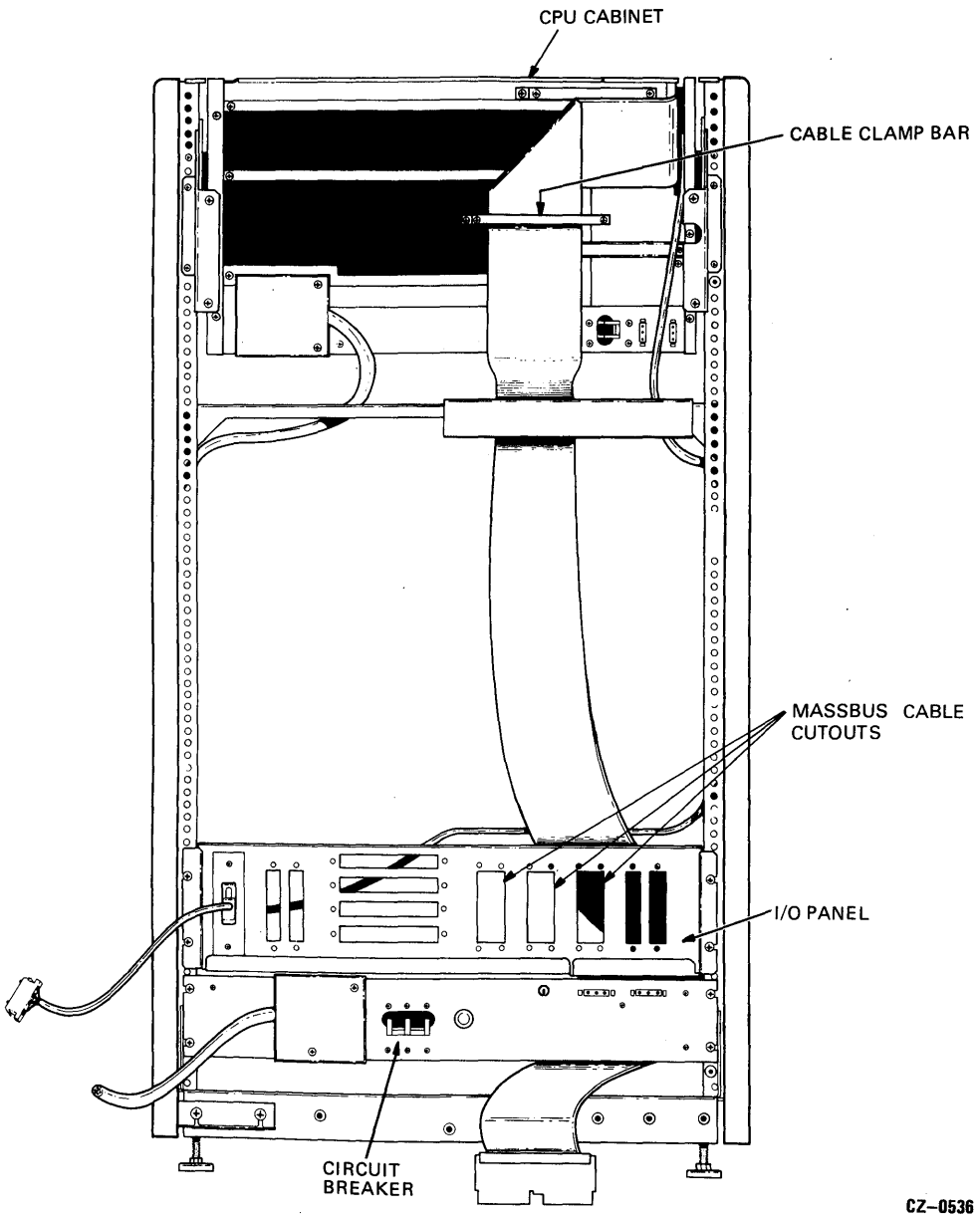


Figure 2-16 I/O Panel and MASSBUS Cable Slot Locations

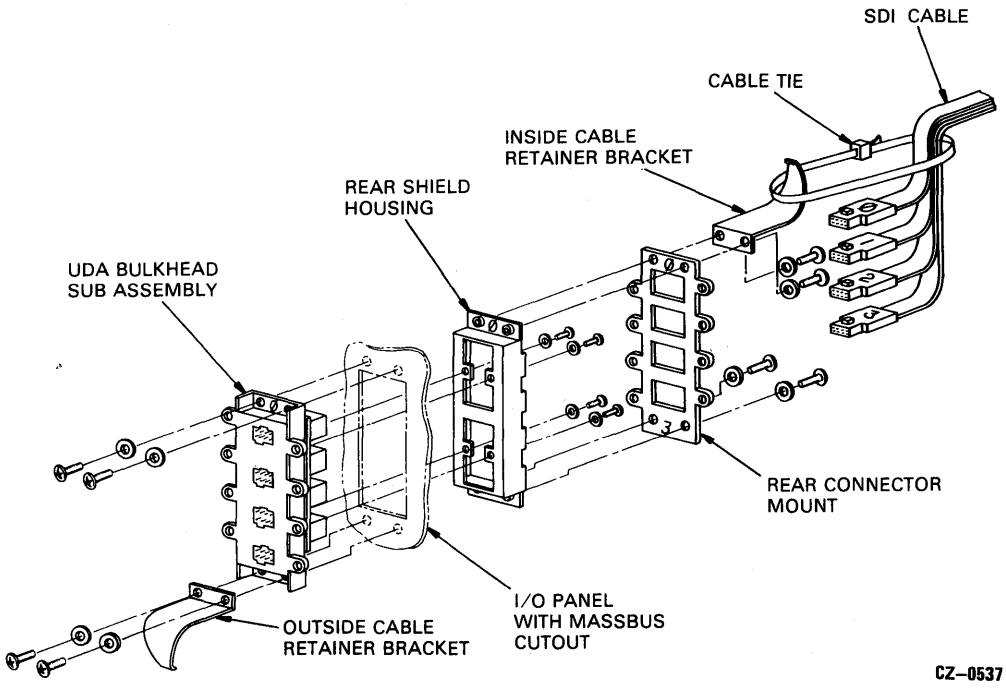


Figure 2-17 I/O Bulkhead Installation

2.3.9.2 SDI Cabling Procedures – Standard Disk Interconnect (SDI) cables must be installed both inside and outside the CPU cabinet. The internal SDI cabling procedure will be described first.

2.3.9.3 Internal SDI Cables – One end of the internal SDI cable is already connected to UDA50 Module M7162 and M7486. This is described in paragraph 2.3.5. Now the other end of the SDI cable assembly must be plugged into the I/O bulkhead on the I/O panel at the rear of the CPU cabinet. Use the following procedure to install this cable.

1. Bring the SDI cable assembly out of the CPU UNIBUS BA-11 box through the cable trough shown in Figure 2-18.

2. Install a tie wrap on the SDI cable assembly approximately where it passes through the cable trough. Refer to Figures 2-18 and 2-19.

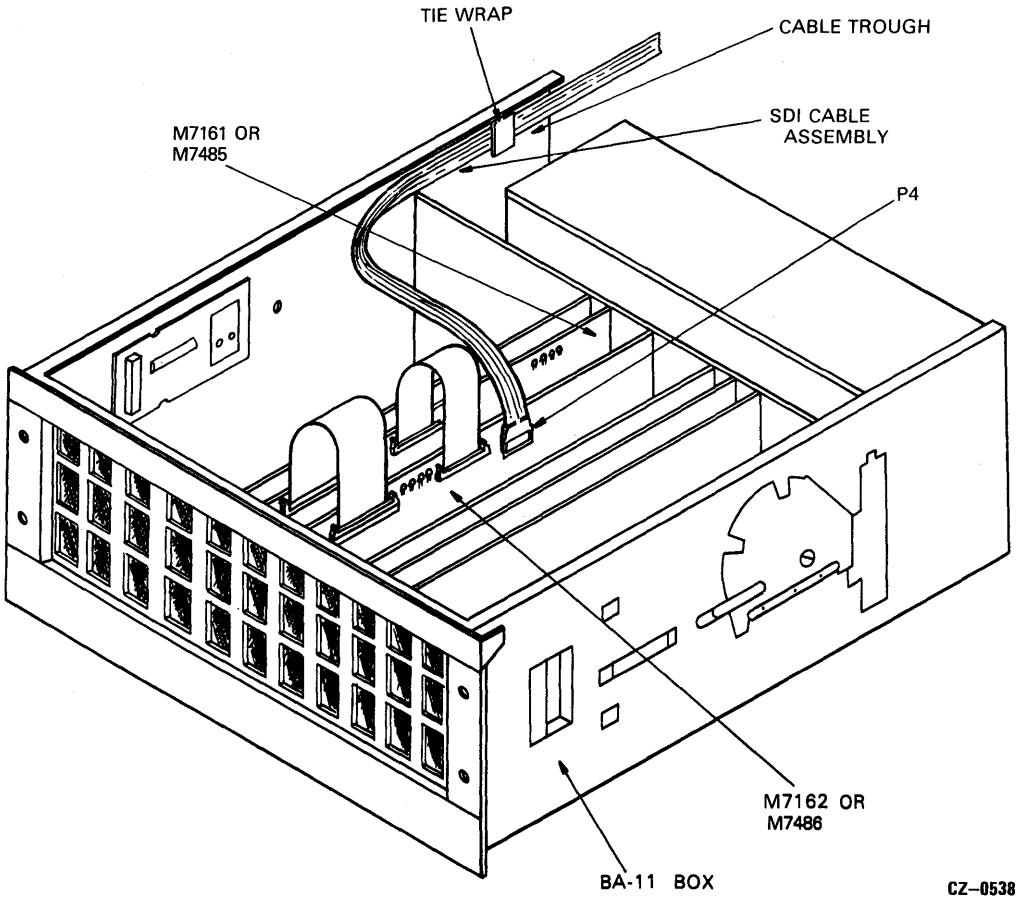
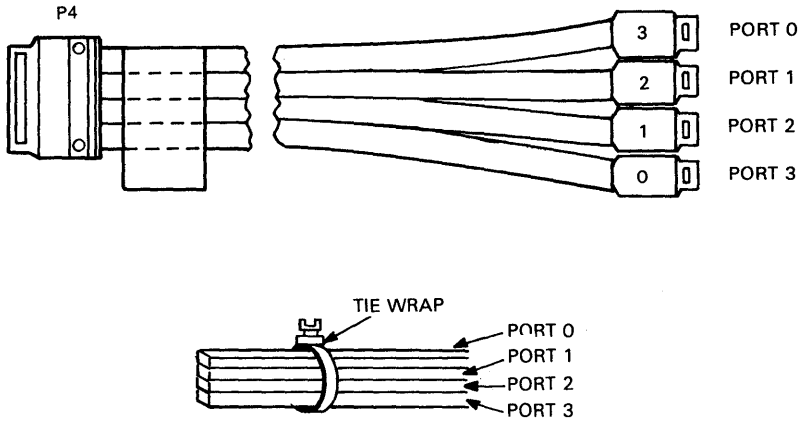


Figure 2-18 SDI Cable Routing Inside BA-11 Box



NOTE
1. TIE WRAP THE SDI CABLE ASSEMBLY SO THAT CABLES ARE STACKED ONE ABOVE THE OTHER WITH PORT 0 AT TOP

CZ-0539

Figure 2-19 SDI Cable Assembly with Tie Wrap

3. Tie wrap the SDI cable at point A where it exits the rear of the BA-11 box. Refer to Figure 2-20.

4. Install the two Dakota clamps as shown in Figure 2-20 and insert the SDI cable assembly in them.

5. Install the remaining seven cable ties on the SDI cable assembly as shown in Figure 2-20. The seventh cable tie is hidden behind the bottom I/O panel.

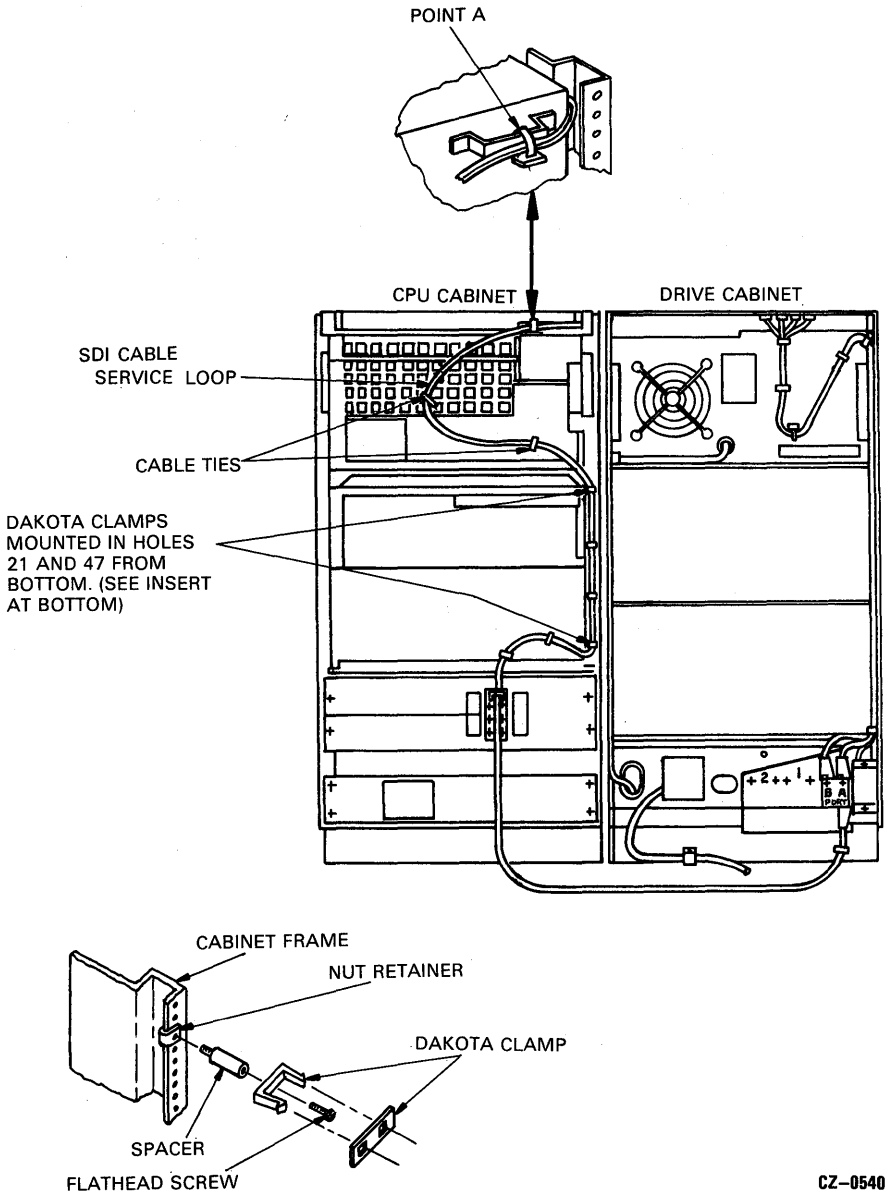


Figure 2-20 SDI Cable Assembly Installation

6. Insert the SDI cable plugs into the I/O bulkhead with the port 0 cable in the top connector. The I/O bulkhead connectors are numbered 0, 1, 2, and 3 from the top. Clamp the SDI cables to the retainer bracket. Refer to Figure 2-21.

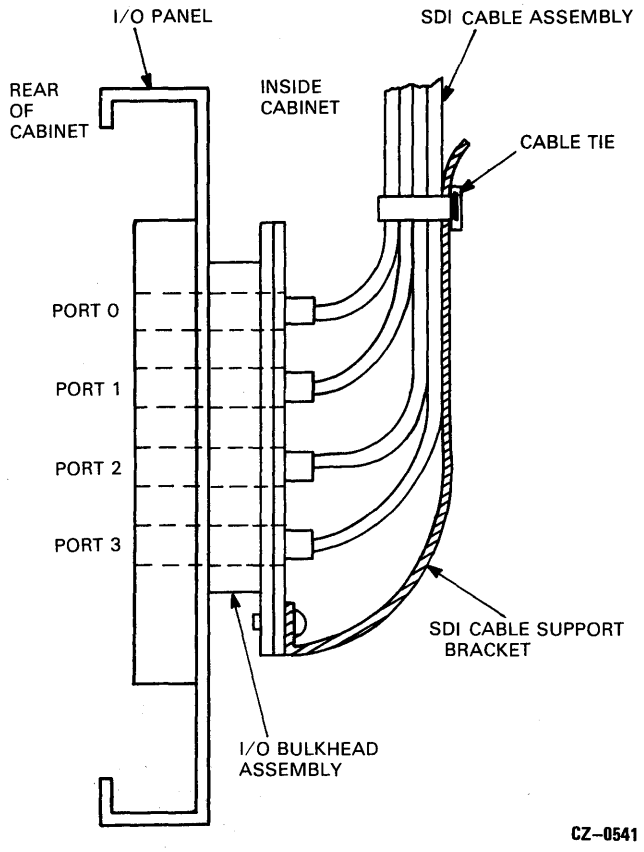


Figure 2-21 SDI Cable Retainer Bracket

2.3.9.4 External SDI Cables – The external SDI cables are shielded cables that must be grounded to the I/O bulkhead by mounting the shield terminators with screws. Use the following procedure to install these cables.

1. Plug the first SDI cable into the top I/O bulkhead connector (Port 0).

2. Screw the SDI cable shield terminator to the I/O bulkhead as shown in Figure 2-22.

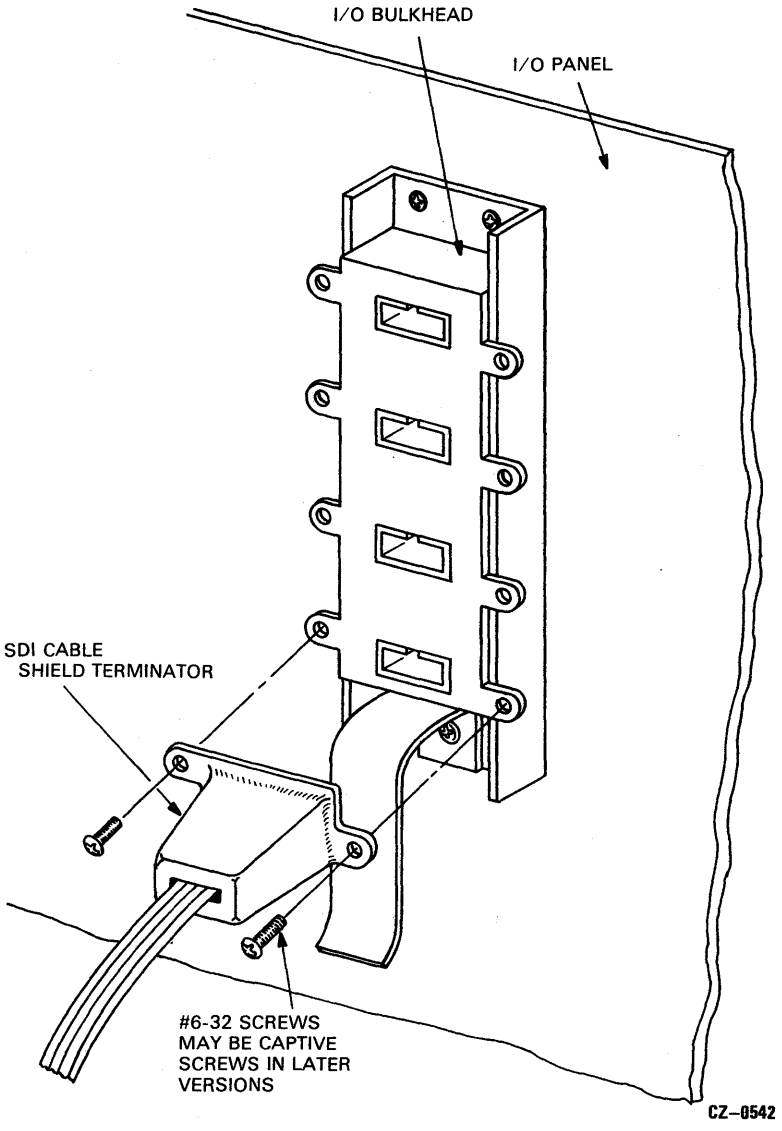


Figure 2-22 SDI Cable Shield Terminator Installation

3. Install an SDI cable for each disk drive, starting at I/O bulkhead connector 0 and going down sequentially.

4. Secure the SDI cables to the SDI cable retainer bracket shown in Figure 2-23.

5. Install the drive end of the SDI cables into the drive I/O bulkhead connectors as described in the disk drive user guide. The UDA50 port 0 SDI cable should attach to drive 0, UDA50 port 1 to drive 1, etc.

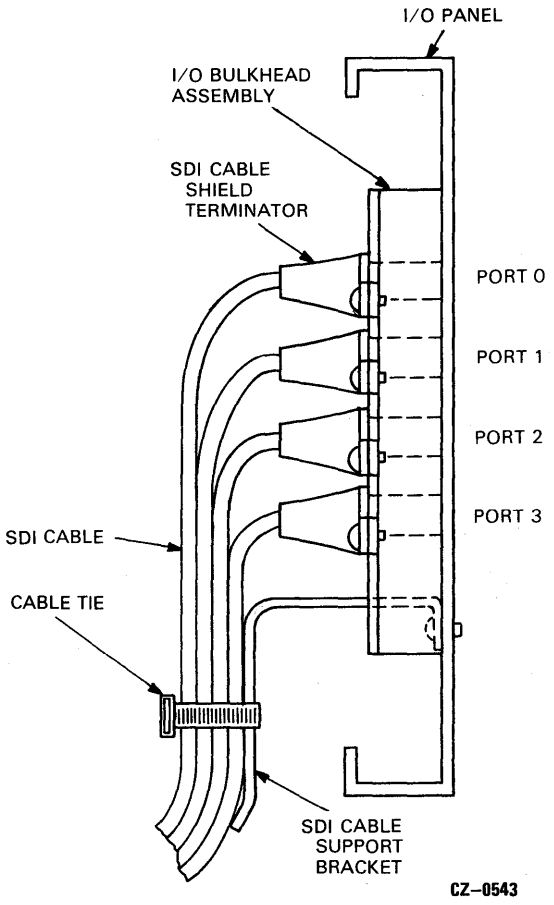


Figure 2-23 Clamping the SDI Cables to the Support Bracket

2.3.9.5 Alternate SDI Cable Installation – The SDI cable installation procedures described in paragraph 2.3.9.3 and 2.3.9.4 should be used whenever an I/O panel is available and room permits. When no I/O panel is present, an alternate means of SDI cable installation is provided. This alternate procedure requires the parts shown in Figure 2-24. Use Figure 2-24 as a reference and perform the following steps.

1. Select a suitable location on either rear vertical cabinet rail where this alternate I/O bulkhead can be mounted without interfering with existing equipment. Choose the lowest available location in the cabinet.

2. Push on the four u-nuts to align with the holes in the vertical rail bracket.

3. Select the best angle and mount the bulkhead shield terminator onto the vertical rail bracket with two' Phillips head sems (10-32 × 1/2 inch).

4. Mount the vertical rail bracket onto the vertical cabinet rail with the four Phillips head sems (10-32 × 1/2 inch).

5. Install the I/O bulkhead connector onto the bulkhead shield terminator using the same procedure described in paragraph 2.3.8. Mount the I/O bulkhead so that connector number 0 is towards the right.

2.4 INSTALLATION OF BOOTSTRAP ROM

The proper bootstrap ROMs will be shipped with the UDA50. Bootstrap ROM # 23-767A9-00 must be installed on the PDP-11 bootstrap ROM module M9312.

Bootstrap ROM # 23-990A9-00 must be installed on the VAX 11/750.

2.5 FIELD ACCEPTANCE TEST PROCEDURE

The field acceptance and test procedure for the UDA50 Disk Subsystem has three parts. The first part is to run the UDA50 Disk Controller resident diagnostic test. The second part involves running the disk drive field acceptance test found in the disk drive user guide. After each subsystem device has been tested separately, the UDA50 host-resident diagnostics are run to complete the third part of this procedure.

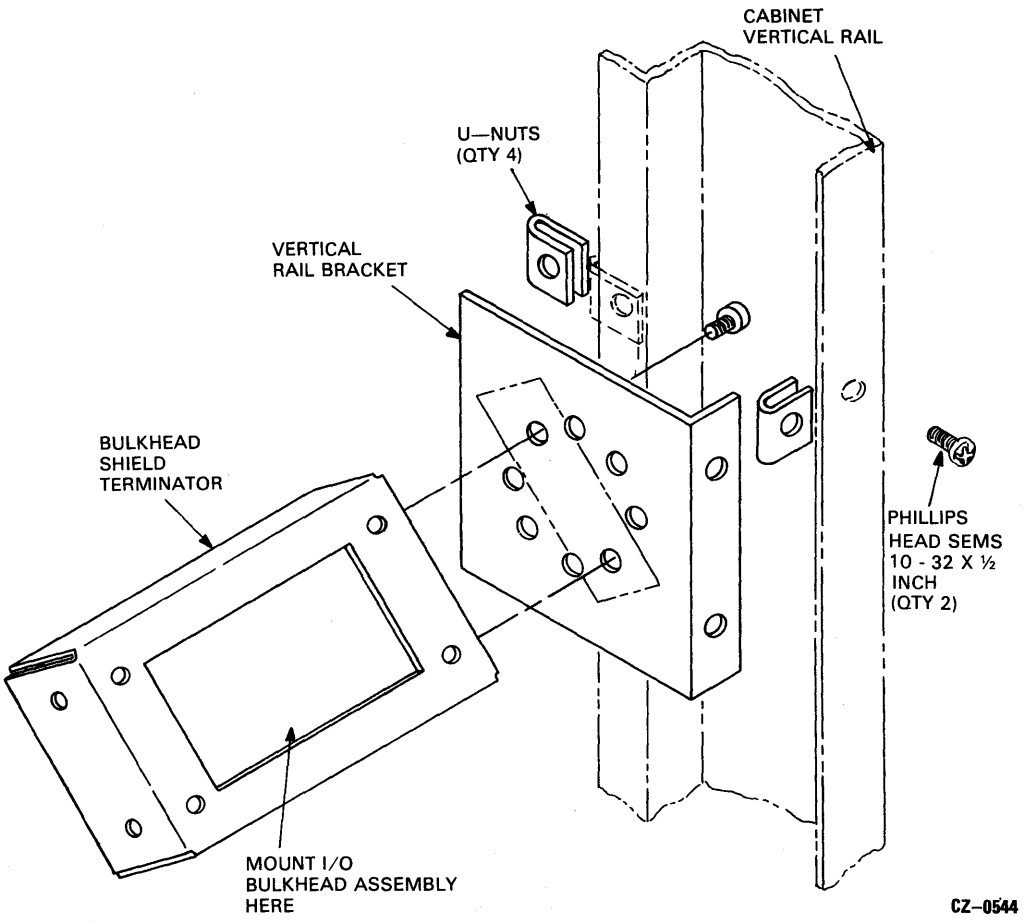


Figure 2-24 Alternate SDI Cable Installation

2.5.1 UDA50-Resident Diagnostics

The UDA50-resident diagnostics is initiated when power is applied to the UDA50 Disk Controller. The CPU should be halted during this test. The four LED indicators on each UDA50 module should display a cycling pattern in the LEDs. The cycling pattern in the LEDs signifies the completion of a successful UDA50 diagnostic test. Figure 2-25 shows the location of the four LEDs on each UDA50 module.

If the UDA50 LEDs do not display the cycling pattern after power is applied, look up the LED code in Table 2-3 to locate the problem.

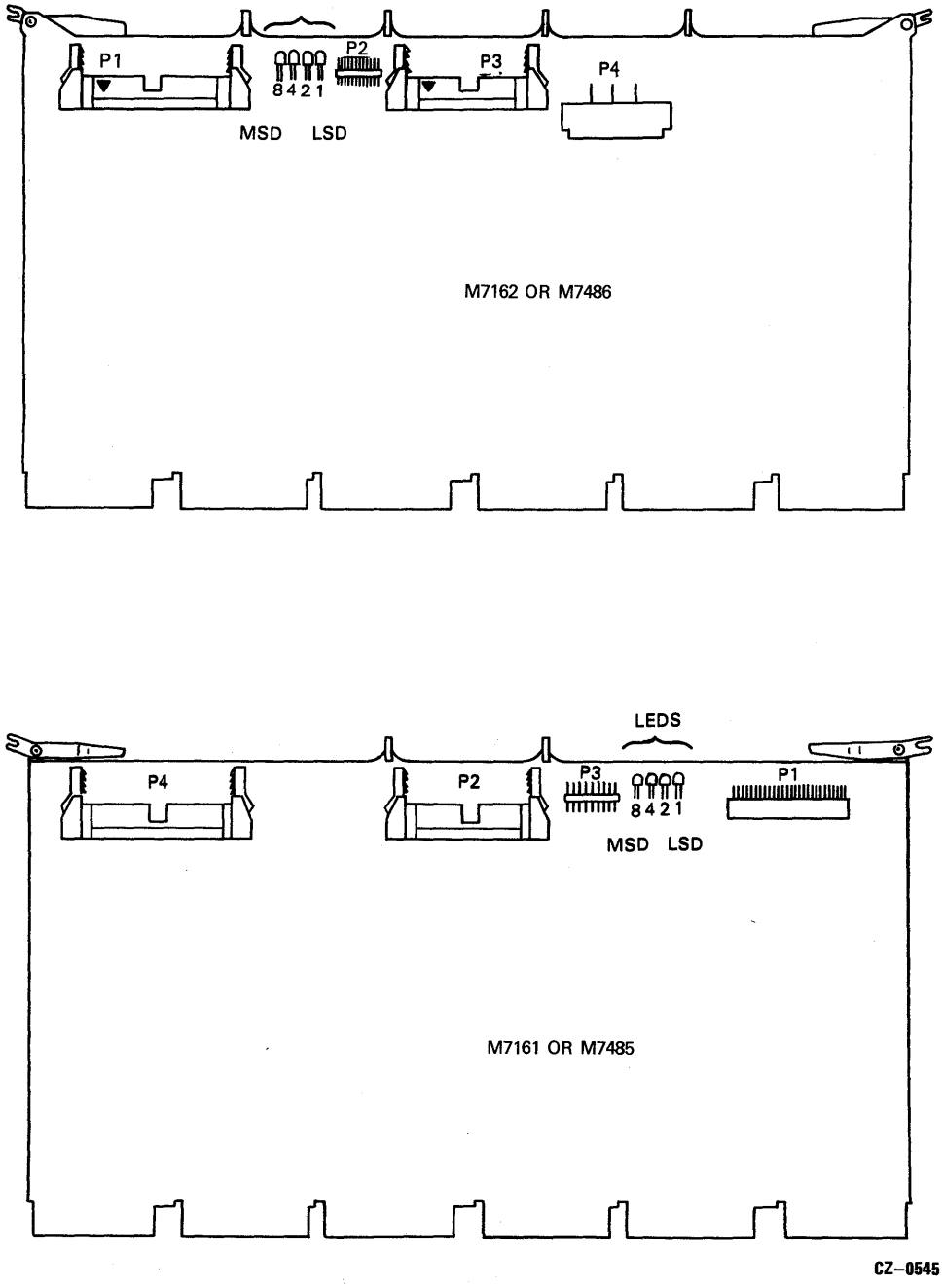


Figure 2-25 Diagnostic LED Locations on UDA50 Modules

Table 2-3 LED Error and Symptom Codes

M7161 or M7485 LEDs 8 4 2 1	M7162 or M7485 LEDs 8 4 2 1	Error Symptoms	Most Likely Failure
○ ○ ○ ●	x x x x	Hex 1; undefined	Undefined
○ ○ ● ○	○ ○ ○ ○	Hex 2; microcode stuck in init step 2	M7161 or M7485 or software
○ ○ ● ●	○ ○ ○ ○	Hex 3; microcode stuck in init step 3	M7161 or M7485 or software
○ ● ○ ○	○ ○ ○ ○	Hex 4; microcode stuck in init step 4 or UNIBUS timeout error	M7161 or M7485 or host inactive
○ ● ○ BLINK	○ ○ ○ ○	Hex 4/5; test complete	No problem
○ ● ● ○ x x x x	x x x x ○ ● ● ○	Hex 6; undefined	Undefined
○ ● ● ● x x x x	x x x x ○ ● ● ●	Hex 7; undefined	Undefined
● ○ ○ ○	○ ○ ○ ○	Hex 8; wrap bit 14 set in SA register	M7161 or M7485 or software
● ○ ○ ● ○ ○ ○ ○	○ ○ ○ ○ ● ○ ○ ●	Hex 9; board one error	M7161 or M7485
● ○ ● ○ ● ○ ● ○	○ ○ ○ ○ ● ○ ● ○	Hex A; board two error	M7162 or M7486
● ○ ● ● x x x x	x x x x ● ○ ● ●	Hex B; undefined	Undefined
x x x x ● ● ○ ○	● ● ○ ○ x x x x	Hex C; ROM parity error	M7161 or M7485
● ● ○ ● x x x x	x x x x ● ● ○ ●	Hex D; RAM parity error	M7162 or M7486
● ● ● ○ x x x x ● ● ● ●	x x x x ● ● ● ○ ● ● ● ●	Hex E; ROM or RAM parity error Hex F; sequencer error	M7161 or M7485 M7162 or M7486 M7161 or M7485

Table 2-3 LED Error and Symptom Codes (Cont)

M7161 or M7485 LEDs 8 4 2 1	M7162 or M7485 LEDs 8 4 2 1	Error Symptoms	Most Likely Failure
Cycling pattern	Cycling pattern	UDA responds to host if cycling pattern lasts less than 2 seconds after host sends step 1 data.	No problem
		UDA does not respond to host if cycling pattern lasts more than 2 seconds after host sends step 1 data.	M7161 or M7485

Note: • = LED ON ○ = LED OFF x = Does not care condition

When two codes are given for the same error, both indicate the same failure.

2.5.2 Drive-Resident Diagnostics

Each disk drive should be tested separately by running the drive-resident diagnostics. The procedure for running the resident diagnostics is found in the installation chapter of the disk drive user guide. Perform the drive field acceptance tests found in the installation chapter and then go to Paragraph 2.4.3 for the subsystem diagnostic procedures.

2.5.3 Subsystem Diagnostics

The subsystem diagnostic procedures for the UDA50 controller are different, depending on whether they are used on a PDP-11 CPU or a VAX CPU. The following paragraphs first cover the PDP-11 diagnostics and then secondly, the VAX diagnostics.

NOTE

If the diagnostic program reports errors, refer to the *UDA50 Service Manual* or *Maintenance Guide*.

2.5.3.1 PDP-11 Subsystem Diagnostics –

- CZUDEC0 (UDA disk formatter)

  Most disk drives will be shipped with formatted disk packs. On these disk drives, it will not be necessary to run the formatter program. Refer to the disk drive user guide to determine if you must run the formatter before the diagnostic program.

- CZUDCC0 (UDA and disk drive diagnostic)

  This diagnostic consists of the following four tests:

  - Test 1 - UNIBUS Addressing Test
  - Test 2 - Disk-Resident Diagnostic Test
  - Test 3 - Disk Functional Test
  - Test 4 - Disk Exerciser Test

  The hardware and software questions asked by this diagnostic are shown in the following two samples along with their default conditions < X>.

  NOTE
  Refer to the software documentation for detailed description, error messages, etc.

  Sample hardware questions:

```
CHANGE HW (L)      ? N

# UNITS (D)   ? 1

UNIT 0
UNIBUS ADDRESS OF UDA (0) 172150
VECTOR (0) 154?
BR LEVEL (D) 5 ?
UNIBUS BURST RATE (D)   0?
DRIVE NUMBER (D) 0?

EXERCISE ON CUSTOMER DATA AREA IN TEST 4 (L) N ? N
```

  Sample software questions:

```
CHANGE SW (L)      ? N

ENTER MANUAL INTERVENTION MODE FOR SPECIAL DIAGNOSDIS (L) Y ? N

REMAINING SOFTWARE QUESTIONS APPLY TO TEST 4 ONLY

ERROR LIMIT (D) 32 ?
READ TRANSFER LIMIT IN MEGABYTES - 0 FOR NO LIMIT (D) 0 ?
SUPRESS PRINTING SOFT ERRORS (L) Y ?
DO INITIAL WRITE ON START (L) Y ?
ENABLE ERROR LOG (L) N ?
```

2.5.3.2 VAX Subsystem Diagnostics –

- ZZ-EVRLB (UDA50 disk formatter)

  Most disk drives will be shipped with formatted disk packs. It will not be necessary nor desirable to run the formatter program on these disk drives. Refer to the disk drive user guide to determine if you must run the formatter before the diagnostic program.

- ZZ-EVRLA (UDA50 disk subsystem diagnostic)

  The VAX UDA host-resident diagnostic contains the following four tests.

  - Test 1 - UNIBUS addressing test
  - Test 2 - Disk-resident diagnostic test
  - Test 3 - Disk functional test
  - Test 4 - Disk exerciser test

    Use the verify section of this diagnostic for system installation.

- ZZ-EVRLC (Generic disk drive exerciser)

  This program tests the read and write ability of any SDI type disk drive, and will display differences in the read and write data to the operator.

NOTE
Refer to the software documentation for detailed descriptions, error messages, etc.

CHAPTER 3
UDA50 PROGRAMMER INFORMATION

3.1 GENERAL PROGRAMMING INFORMATION

The UDA50 operates according to the rules defined in three separate documents. The following is a list of these documents.

- *MSCP Basic Disk Functions Manual* (AA-L619A-TK)
- *Storage System Diagnostic and Utilities Protocol* (AA-L620A-TK)
- *Storage System UNIBUS Port Description* (AA-L621A-TK)

All three documents may be purchased separately or as a kit called the *UDA50 Programmer's Documentation Kit* (QP905-GZ) from the Software Distribution Center, Order Administration/Processing, 20 Forbes Road (NR4), Northboro, Massachusetts 01532.

3.2 UDA50-SPECIFIC PROGRAMMING INFORMATION

The following information is UDA50-specific and is necessary for anyone needing to write his own software for the UDA50.

- The address of the UDA50 IP register is 772150 (octal).
- The address of the UDA50 SA register is 772152 (octal).
- The UDA50 supports a host-settable interrupt vector address. A vector address of 154 (octal) is assigned to the UDA50.
- The UDA50 has a command limit value of 13. This includes 12 MSCP commands plus 1 immediate-only command.
- The UDA50 supports an NPR burst value of 1 to 32 long words. One long-word is the default condition.
- The UDA50 supports only 512 byte disk formats.
- The UDA50 supports both the MSCP and the diagnostic and utilities protocols (DUP).
- The diagnostic option capabilities available on the UDA50 are the purge and poll and the diagnostics wrap.
- The UDA50 supports maintenance read and maintenance write to and from the UDA RAM.
- The UDA50 supports last fail log packets.

UDA50 USER GUIDE
EK-UDA50-UG-002

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