Digital Equipment Corporation
Maynard, Massachusetts

digital

Maintenance Manual

RS64 DISK FILE

DEC-00-RS64-DB

RS64
DISK FILE
MAINTENANCE MANUAL

DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

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CONTENTS

CONTENTS (cont)

ILLUSTRATIONS

TABLES

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This manual contains instructions for interfacing, installing, operating, and maintaining the RS64 Disk File manufactured by Digital Equipment Corporation (DEC), Maynard, Massachusetts. The instructions are intended for maintenance personnel with a basic understanding of disk files but who may not necessarily be familiar with the RS64 Disk File.

The instructions are arranged in six primary divisions: General Description, Installation and Operation, Theory of Operation, Interfacing, Maintenance, and Drawings. Two appendices are also provided; (a) track writer format and relationships, and (b) the power supply.

In addition to this manual, the following documents contain information relevant to the RS64 Disk File:

a. DEC Logic Handbook, 1970, C105

b. Special Maintenance Procedures for Disks, DEC-SP-DISK-DA.

1.2 PURPOSE AND APPLICATION INFORMATION

The RS64 Disk File, Figure 1-1, is a fast, random-access file that provides up to 1,280,000 bits of storage. With the disk select logic provided in each disk file, up to four RS64 Disk Files can be operated from one controller, thus providing a storage capability of up to 5,120,000 bits.

The RS64 is designed for standard 19-in. rack mounting. It is furnished complete with disk assembly, modularized read/write electronics, and power supply contained in a slide-mounted chassis that requires 10-1/2 in. of front panel height. Two basic models are available; the RS64A operates with 115V, 47 to 63 Hz primary power and the RS64B operates with 230V, 47 to 63 Hz primary power.

The disk assembly contains a 10-in. nickel-cobalt plated disk that is driven by an induction motor at approximately 1400 (50 Hz) or 1800 (60 Hz) rpm. Data is recorded on a single disk surface using 32 fixed read/write heads. Other features include a highly reliable, self-synchronizing clock recovery system and write protection (write lockout) for the data tracks. Three spare timing tracks are also provided.

Pertinent interfacing and design criteria, plus recommended controller interface circuits, are provided in this manual. In addition, the RS64 Power Supply is capable of providing a controller with up to 4.5 A at +5V.

1.3 PHYSICAL DESCRIPTION

1.3.1 General

The RS64 Disk File consists of two major assemblies, disk assembly RS64M and power control and logic assembly RS64P. These assemblies and the elements comprising them are described in subsequent paragraphs.

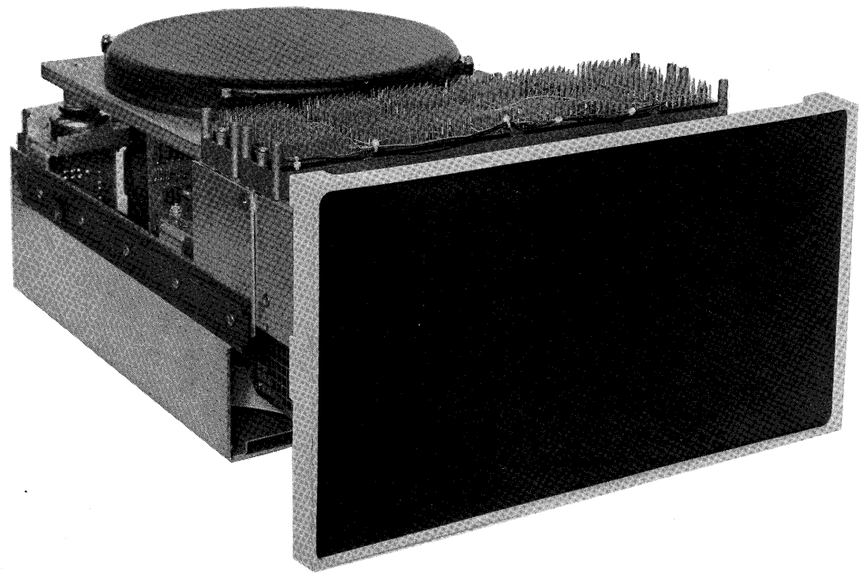


Figure 1-1 RS64 Disk File

1.3.2 RS64M Disk Assembly

The disk assembly, Figure 1-2, consists of a 10-in. diameter nickel-cobalt plated aluminum disk, a drive motor, and five head assemblies mounted on a deck plate. The deck plate is supported by four shock mounts. A cover protects the disk and heads from dust and foreign particles. Data connections are made via connectors on the underside of the deck plate. A 4-wire power cord connects the drive motor to the RS64P power control and logic assembly.

1.3.3 RS64P Power Control and Logic Assembly

The power control and logic assembly, Figure 1-3, consists of a wired assembly for housing logic modules, a power control panel, a disk select and write lockout panel, and a power supply. It also includes two data cable assemblies and one timing cable assembly that convey signals between the disk assembly and the read/write electronics.

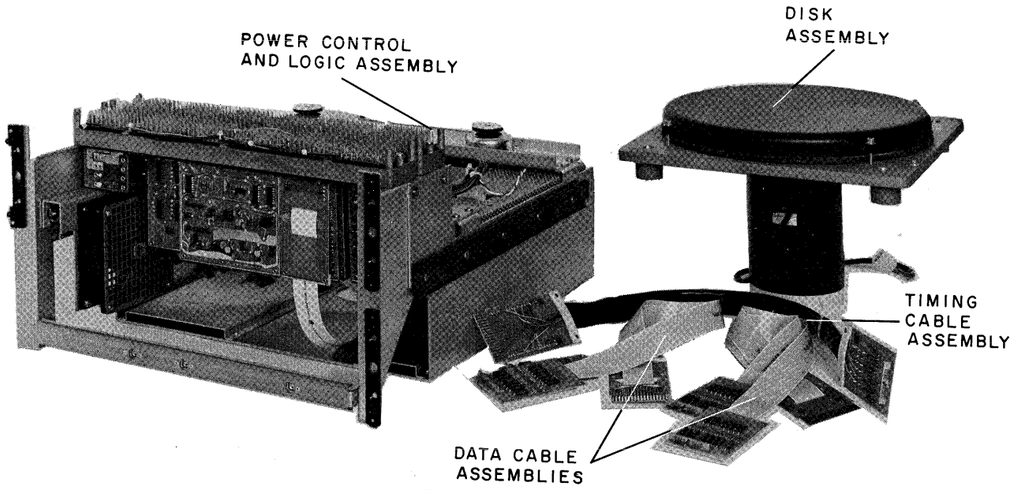


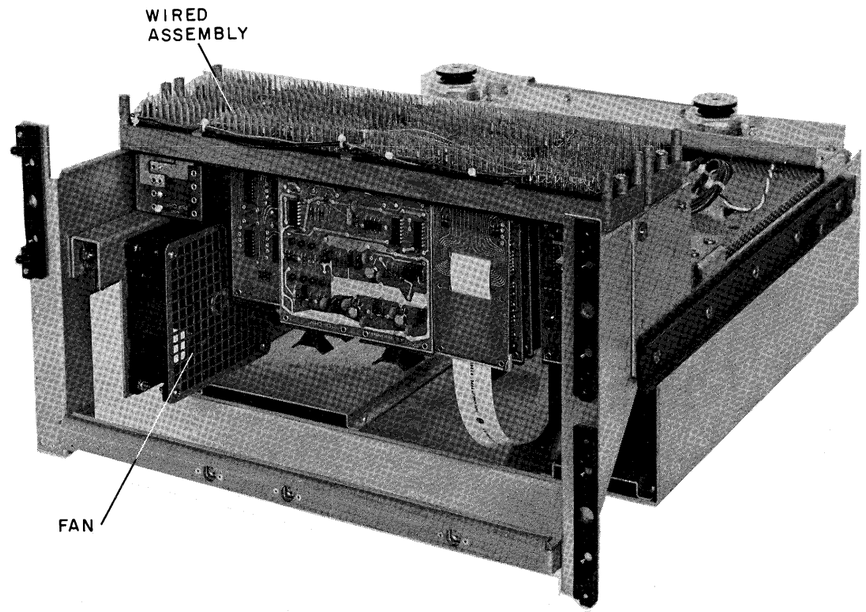
Figure 1-2 RS64 Disk File Major Assemblies

1.3.3.1 Wired Assembly – The wired assembly contains the read/write modules and provides the connectors for the data and timing cables, the power supply cable, and the controller cables. The assembly consists of a logic frame that houses six connector blocks each capable of accepting eight single-height modules or four double-height modules. Wire-wrap connections are used between connector blocks. A fan, located on the module side, provides forced-air cooling for the modules. The wired assembly is hinged at each end and can be rotated on its horizontal axis for convenient servicing.

1.3.3.2 Power Control Panel Assembly – The power control panel assembly contains the receptacles for primary power connections, an RFI filter, and circuits for local/remote control of primary power. The assembly is attached to the chassis by four screws and can be removed readily for internal access. All electrical connections between the panel and other assemblies are made using connectors on the external portion of the assembly. The internal wiring of this assembly determines if the unit is used with 115V or 230V.

1.3.3.3 Disk Select and WLO Panel Assembly – This assembly contains the controls for selecting disk unit assignment and track write protection (write lockout). A 5-position rotary switch is used for disk file assignment (0 through 3) and for placing the unit off-line (OFF). Five rocker switches are used for the write lockout function. The upper rocker switch enables or disables the write lockout function. With this switch in the enable position, all tracks from 00 through the track number selected by the other four rocker switches are write protected. The rotary switch and the five rocker switches are mounted on a PC module located behind the panel. A flat Mylar cable connects this assembly to the wired assembly.

1.3.3.4 Power Supply – The power supply provides -15V, +5V, and +20V potentials for the read/write electronics. Primary power connections are made using a 12-inch cord with a 4-pin connector. This connector mates with a receptacle on the power control panel assembly. The ac operating potentials (and other power supply signals) are provided by a 12-pin female connector located on the top of the power supply. A 12-wire cable with a PC connector module on the connector block end connects the potentials to the wired assembly. For additional power supply coverage, refer to Appendix B.



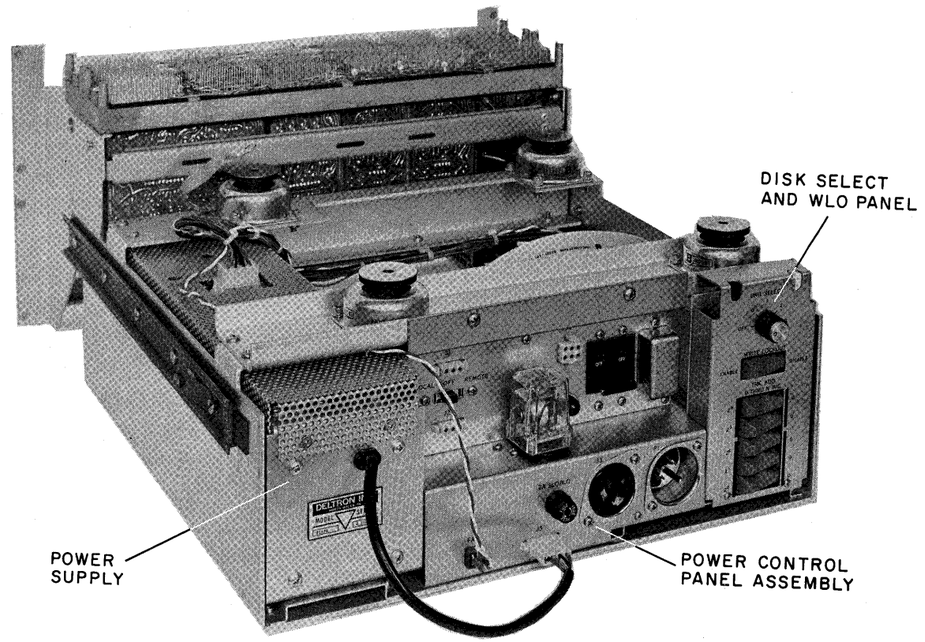


Figure 1-3 Power and Control Logic Assembly

1.3.3.5 Data and Timing Cable Assemblies – Two flat Mylar data cable assemblies (Figure 1-2) interconnect the data track heads with the read/write logic. Each data cable assembly handles the signals for two head shoe assemblies; it has two 8-track matrix-connector modules at the head end. One timing matrix cable assembly (Figure 1-2) interconnects the timing heads with the read/write logic. This cable has a 6-track matrix module at the disk end and a connector module at the logic end.

1.4 SPECIFICATIONS

Storage Medium	10-in. diameter nickel-cobalt plated disk with proprietary protective coating	
Storage Capacity	Up to 1,280,000 bits	
Access Time	**60 Hz Power**	**50 Hz Power**
Minimum	260 μs	260 μs
Average	16.9 ms	20.3 ms
Maximum	33.6 ms	40.3 ms
Data Tracks	32	
Bits Per Track	Up to 40,000	
Recording Method	Self-clocking one-of-N, NRZI code	
Bit Density	1700 bpi (maximum)	
Timing Tracks	3 plus 3 spare	
Write Protection Features	5 switches provide write protection on all binary track addresses up to and including binary track address indicated by switch selections.	
Motor Bearing Life	Expected operating life of at least 20,000 hours under a standard computer operating environment.	
Power Requirements	115/230 Vac ±15%, single-phase, 47 to 63 Hz.	
	Starting current of 6A; nominal operating current of 2.2A.	
Operating Environment	40°F to 125°F, ambient. Relative humidity of 20% to 80% (non-condensing).	
Storage and Shipping Environment	-40°F to 135°F (non-condensing)	
Physical Characteristics		
Height	10-1/2 in.	
Width	19 in.	
Depth	18-3/4 in.	
Weight	64 lb	
Vibration	5–20 Hz 0.010 in. D.A. 20–500 Hz ±1.5g, any plane.	
Shock	5g's Halfsine, 10 ms duration, any plane. Suitable for office, industrial, and large vessel operation.	

CHAPTER 2
INSTALLATION AND OPERATION

2.1 UNPACKING AND INSPECTION

The RS64 Disk File can be shipped in a cabinet as an integral part of a system or separately in its own container for mounting in an existing cabinet. If a unit is shipped in a separate container, Figure 2-1, remove it from the container, remove packing materials, and inspect for shipping damage. Report any damage to the carrier. Retain packing materials for possible reshipment.

The RS64 is shipped with a motor lock installed to prevent rotation of the disk during shipment. In addition, four corosote shock mount yokes, Figure 2-1, prevent bottoming of the shocks during impact. These items *must not* be removed until the disk is correctly installed in a cabinet.

CAUTION

Exercise care in unpacking the unit. Do not drop unit or subject it to unreasonable impact.

If the RS64 Disk File is shipped in a cabinet, the unit is retained in place by shipping brackets located at the rear of the chassis. These brackets must be removed to extend the unit from the cabinet. Remove the shipping brackets and any packing materials and inspect the unit for shipping damage. Report any damage to the carrier.

CAUTION

Do not remove motor lock or shock mount shipping yokes until cabinet is in final installation location. Disk heads can be damaged if unit is moved without these items in place.

2.2 MECHANICAL INSTALLATION

The RS64 Disk File is designed for 19-in. equipment rack mounting and requires 10-1/2 in. of front panel height Up to four disk files can be installed in an H950 cabinet as shown in D-SD-RS64-0-11 (see Chapter 6).

If the RS64 is to be installed in an existing cabinet, it may be necessary to install the cabinet portion of the track slide assembly. Cabinet hardware (10-32 x 3/4 screws and 10-32 clip nuts) shipped with the file should be used to attach the track slide assembly to the cabinet.

Once the RS64 is correctly mounted on track slides, extend the assembly and remove the four shock mount yokes used for shipping. Next, remove the motor lock on the bottom of the motor shaft. Retain these items and the shipping brackets (and the shipping container) for possible reshipment of disk.

2.3 POWER REQUIREMENTS

Model RS64A operates from a 95-135V, 47-63 Hz single-phase source and model RS64B operates from a 190-260V, 47-63 Hz single-phase source. The power control panel of each model provides the facilities for connecting primary power. Each panel contains a male receptacle for input power and a female outlet for extending primary power to other units. Drawing C-BD-RS64-0-10 illustrates a typical arrangement for primary power. A mating connector rated at 15 Amperes is recommended for power input-output connections.

The power control panel also provides the receptacle for remote control for primary power and extending remote control to other units. Drawing C-BD-RS64-0-10 also illustrates a typical arrangement for remote control of power; Figure 2-2 illustrates the circuits used for remote control.

2.4 SIGNAL CONNECTIONS

Drawing C-DB-RS64-0-9 shows a typical arrangement for connecting up to four RS64 Disk Files on a controller bus. This drawing also defines the cable types. Bus length should be 35 ft or less and a G739 terminator card should be used in the last RS64 unit on the bus.

2.5 INSTALLATION CHECKOUT

The RS64 Disk File is thoroughly checked at the factory. However, complete diagnostics should be run after the unit is installed. Information for running the diagnostics is included with the controller.

2.6 PREPARATION FOR MOVING AND SHIPPING DISK FILE

If the unit is to be moved or shipped in a cabinet, install motor lock and shock mount yokes. Lock the assembly in place using shipping brackets.

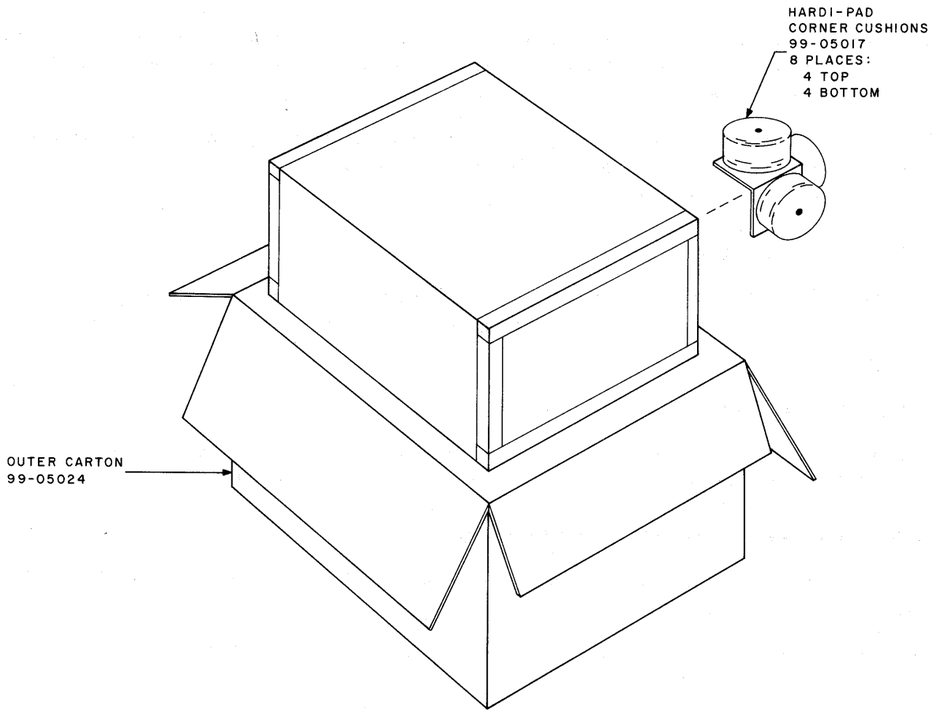
If the unit is to be shipped in a separage container, use the original shipping container where possible. Items used for shipping are depicted in Figure 2-1.

2.7 OPERATION

2.7.1 Power Control Panel Controls and Indicators

The power control panel, Figure 2-3, contains an input power indicator, a 15A circuit breaker, and a LOCAL/OFF/REMOTE switch. The input power indicator is lit whenever primary power is applied to input receptacle P1. Circuit breaker CB1 controls the application of primary power to the disk drive motor, the fan, the power supply relay, and the local/remote control circuits.

The LOCAL/OFF/REMOTE switch controls the application of primary power to the power supply. In the LOCAL position, it energizes the power supply relay to complete the primary power path. In the OFF position, this switch interrupts the control path for the power supply relay to remove primary power.



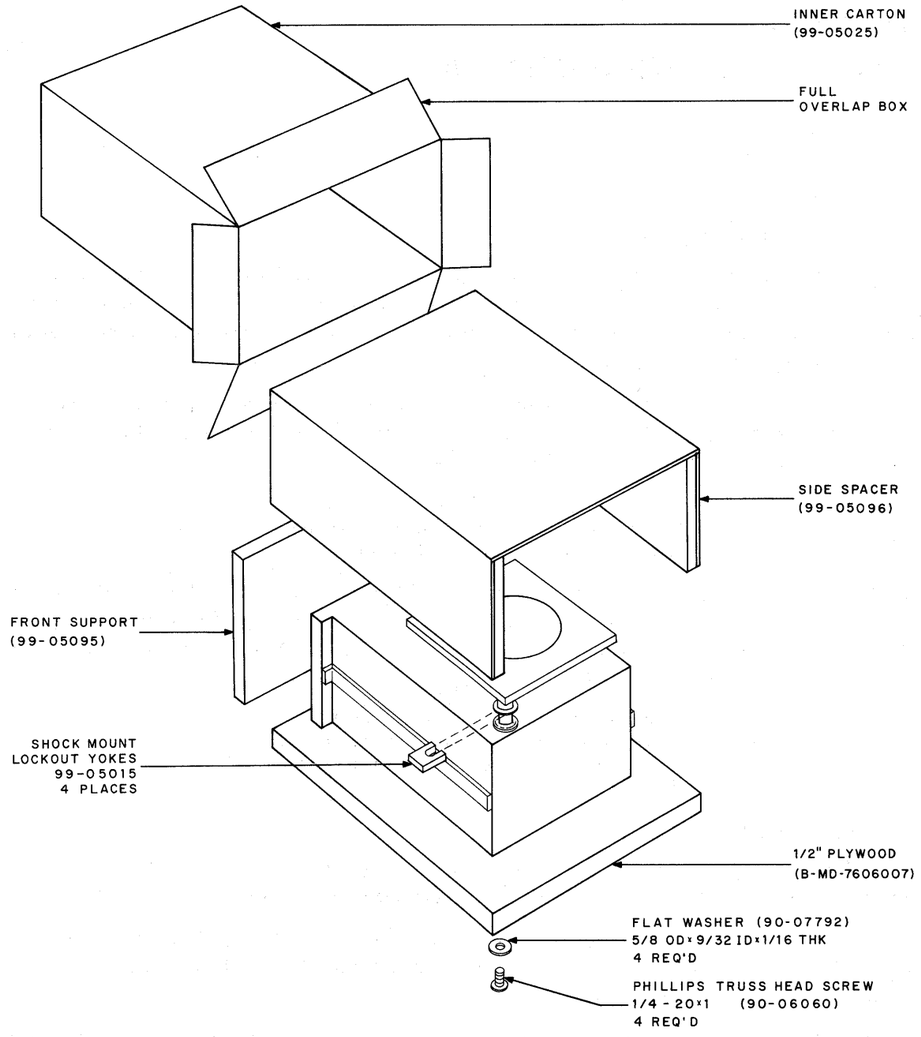


Figure 2-1 RS64 Disk File Packaging

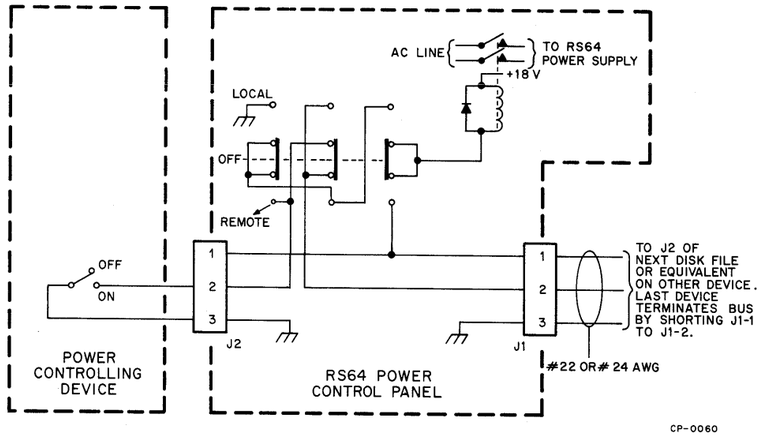


Figure 2-2 Remote Control and Interlock Connections

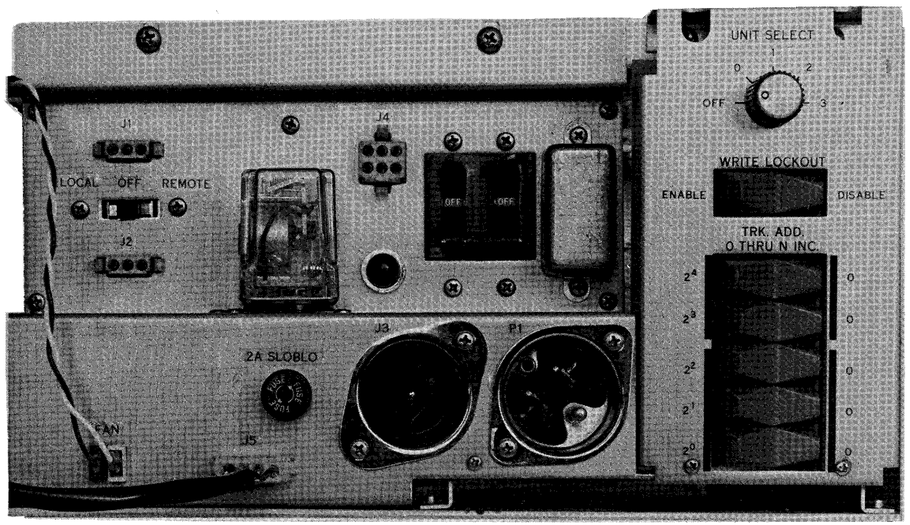


Figure 2-3 Power Control and WLO Panel

The REMOTE position permits power supply turn-on by a remote switch closure. When used in a remote turn-on chain with other units, the LOCAL and OFF positions complete the remote turn-on chain for other units. This feature permits any device to be controlled locally yet still maintain the remote turn-on control for other units.

2.7.2 Disk Select and WLO Panel Controls

This panel, Figure 2-3, provides the controls for establishing a disk drive unit number and for selecting tracks that are to be write protected (write lockout).

a. UNIT SELECT – This 5-position rotary switch establishes a unit number (0 through 3) for a drive or places it logically off-line (OFF position) with respect to a controller or program. With this switch in other than OFF, the drive is selected by a corresponding unit number from a controller. This feature permits up to four disk units to be operated from one controller.

b. WRITE LOCKOUT – This rocker switch, when placed to the ENABLE position, permits the tracks designated by the TRK ADD switches to be write protected. When placed to the DISABLE position, this switch negates any write lockout function.

c. TRK ADD 2^0 – 2^4 – These binary-weighted rocker switches select the tracks that are to have write lockout or write protection. The write lockout function is provided for tracks selected by the binary combination of the switches plus any lower-number tracks. For example, with the 2^0 switch in the logical 1 position and all others in the logical 0 position, tracks 1 and 0 have write lockout. Similarly, with the 2^0 and 2^1 switches in the logical 1 position, tracks 0 through 3 inclusive are write locked.

2.7.3 Operating Instructions

In general, the RS64 disk is an automatic device that does not require operator intervention. To operate the device, simply select a unit number (0 through 3) corresponding to program assignment and apply primary power.

To set up write lockout for tracks:

Step	Procedure
1	Press WRITE LOCKOUT switch to ENABLE.
2	Set up TRK ADD switches to binary equivalent of the highest track number that is to have write lockout. For example, to provide write lockout for tracks 0 through 16, press the 2^4 switch and leave 2^0 through 2^3 in 0 position. To provide write lockout for track 0 only, set all switches to 0.

To discontinue write lockout for previously selected tracks, simply return WRITE LOCKOUT switch to DISABLE position.

CHAPTER 3
THEORY OF OPERATION

3.1 SYSTEM RELATIONSHIPS

Figure 3-1 shows the general relationships of an RS64 Disk File with a controller. Up to four disk files can be operated with one controller. Each disk file is assigned a unit number and is selected by one of four lines from the controller. Only that disk file having the unit number designated by the controller responds to a selection. When a disk is selected, it acknowledges the selection and provides the controller with timing and address information recovered from the disk. Five binary-weighted lines from the controller select one of 32 data tracks. If the data track specified in the selection is write locked, the disk file also notifies the controller.

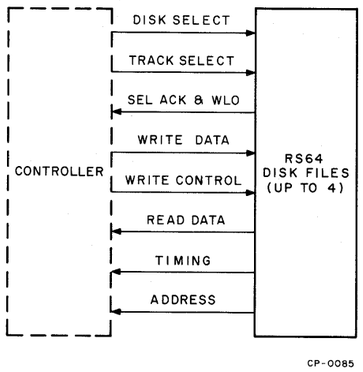


Figure 3-1 RS64 System Relationships

When the controller synchronizes with disk timing information and recognizes the address specified by the program, it begins writing or reading information at that address. For a write operation, the controller enables the disk write electronics and provides the disk with serial data. A read operation is implemented whenever a write operation is not specified. A synchronizing preamble is included with the address and data so that recovery synchronization can be independent of inherent skew between timing, address and data tracks.

3.2 DISK SURFACE AND TRACK ARRANGEMENT

Information is recorded on the lower side of the disk plate, Figure 3-2, at a perimeter beginning approximately 3/4 in. from the outer edge of the disk. Four head shoe assemblies, each containing eight read/write heads, store and retrieve data. One head shoe assembly, containing six read/write heads, is used for writing and recovery of timing and address information, i.e., timing tracks A, B, and C and three spares. These head shoe assemblies are located in the disk base plate as shown in Figure 3-3. Figure 3-4 depicts the arrangement of tracks.

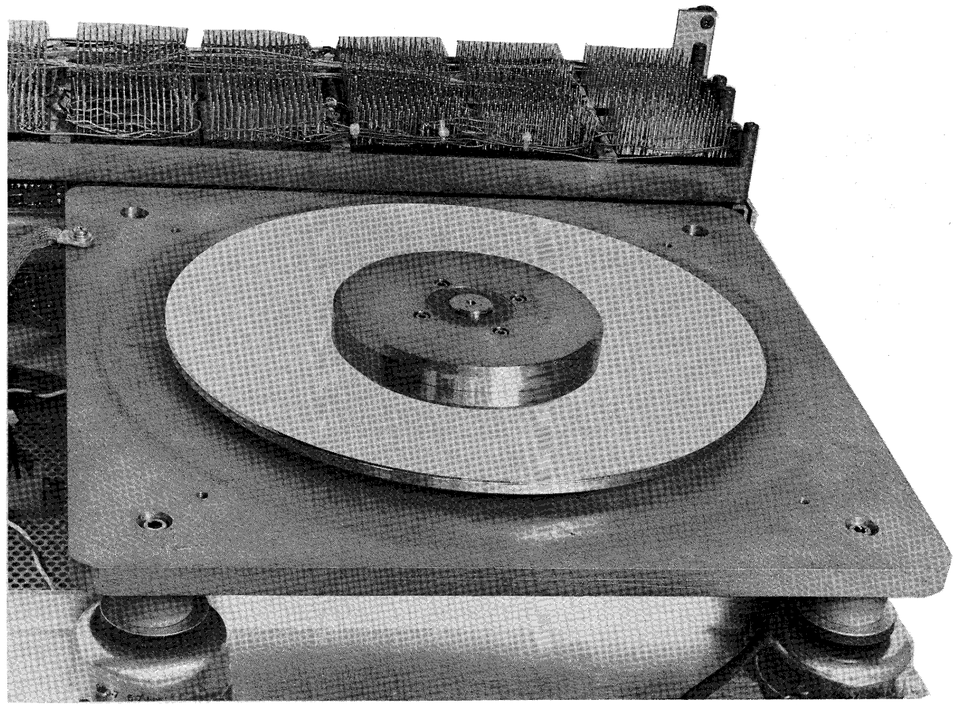


Figure 3-2 Disk Assembly with Cover Removed

3.3 FUNCTIONAL DESCRIPTION

3.3.1 Functional Block Description

Figure 3-5 illustrates the functional circuits that comprise the RS64 Disk File. The upper part of this diagram depicts the disk and track selection circuits and the read and write data paths. The lower part of the diagram depicts the circuits associated with the timing and address tracks.

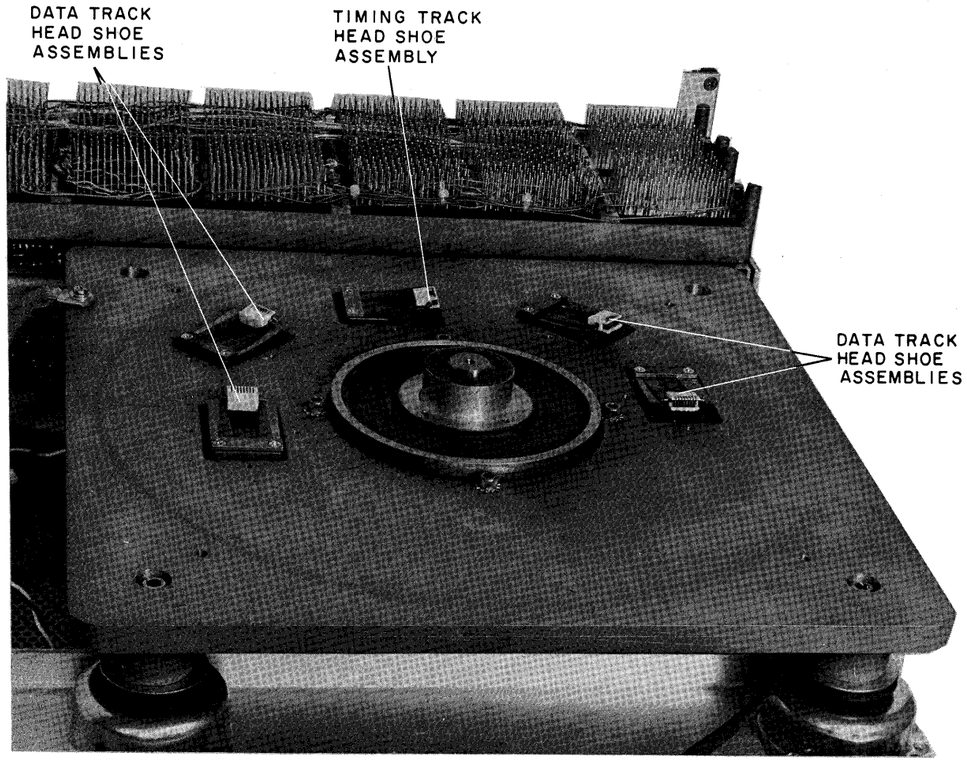


Figure 3-3 Disk Assembly with Head Shoes Exposed

The disk utilizes three pre-recorded timing tracks (plus three spares) and 32 data tracks for recording and recovery of data. Bit timing (and bit cell width) is established by timing track A (TTA). With the exception of an origin gap, this track contains a continuous stream of logical 1's. Timing from this track is supplied to a self-synchronizing phase-locked clock. The phase-locked clock is used as a three times frequency multiplier; it synchronizes its output (F/3) to the phase of the TTA timing stream to enable separation of sync pulses, data ones, and data zeros recovered from the other tracks.

Timing track B conveys address and data markers. The address marker denotes the beginning of an address sector on timing track C; it occurs at least six bit times before the address preamble. Similarly, the data marker signifies the beginning of a data sector of a track.

Timing track C conveys the information for addressing portions of a data track, i.e., block addresses. A synchronizing preamble and an odd parity bit are included with each block address. The number of primary divisions or blocks assigned to the data tracks determines the number of address bits. For RC11 usage, for example, data is stored in 64 blocks; thus, a 6-bit address is required. The synchronizing preamble provided with the address permits a controller to correctly synchronize with TTC information without having to compensate for skew between the clock timing track and the address track.

Information is continuously read from timing tracks A, B and C; however, this information is not gated to the controller until the disk file is selected. For selection of a disk file, the controller enables one of four input lines

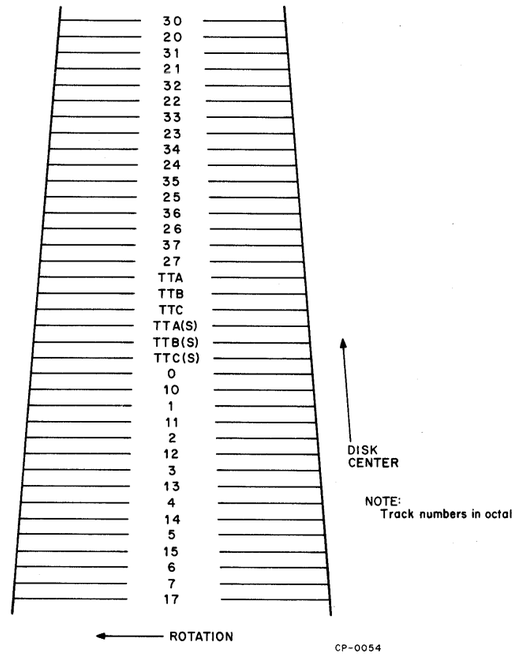


Figure 3-4 Track Arrangement

(DISK SEL 0–3) to the Disk Select/WLO panel. If the disk file is assigned a unit number corresponding to the controller selection, the Disk Select/WLO panel provides an SEL output. This output enables the gating of timing, address, and read data to the controller. Selection of a disk file also causes the selected unit to return a SEL ACK signal to the controller. This signal informs the controller the disk file is operable and has recognized the selection.

Concurrent with selection of the disk file, the controller specifies which track is to be used. This information is provided as a 5-bit track address (TRK $2^0 - 2^4$) to the track decoder circuits and a write lockout (WLO) comparator. If the track designated by the controller is one of a group selected to be write-protected (no rewriting of the track), the WLO comparator disables the disk write circuits. Thus, only a read operation can be performed for the track. Since the write lockout disables the write driver, no combination of control signals can enter information on the write locked tracks.

The track address is decoded in two parts. One decoder circuit decodes the three LSB's ($2^0 - 2^2$) and enables one of eight center tap selector circuits to select one of eight matrix lines (0–7). Similarly, a second decoder circuit decodes the two MSB's of the track address and enables the corresponding series switch circuits to select one of four pairs of matrix lines (octal group 0–7, 10–17, 20–27, or 30–37). The combination provided by the center tap selector and the series switch selects the track for an ensuing read or write operation.

A read operation is specified by the negation of a write enable (WREN) input. This input disables the disk writer circuits to allow a read operation. When the controller recognizes the address for the desired block of the selected track, it begins accepting the serial read data.

For a write operation, the controller compares the address from timing track C with the address specified by the program. Upon recognizing the correct address, the controller asserts the WREN input and provides serial NRZ data to the disk write flip-flop. This flip-flop, clocked at mid-bit time with respect to the input serial NRZ data,

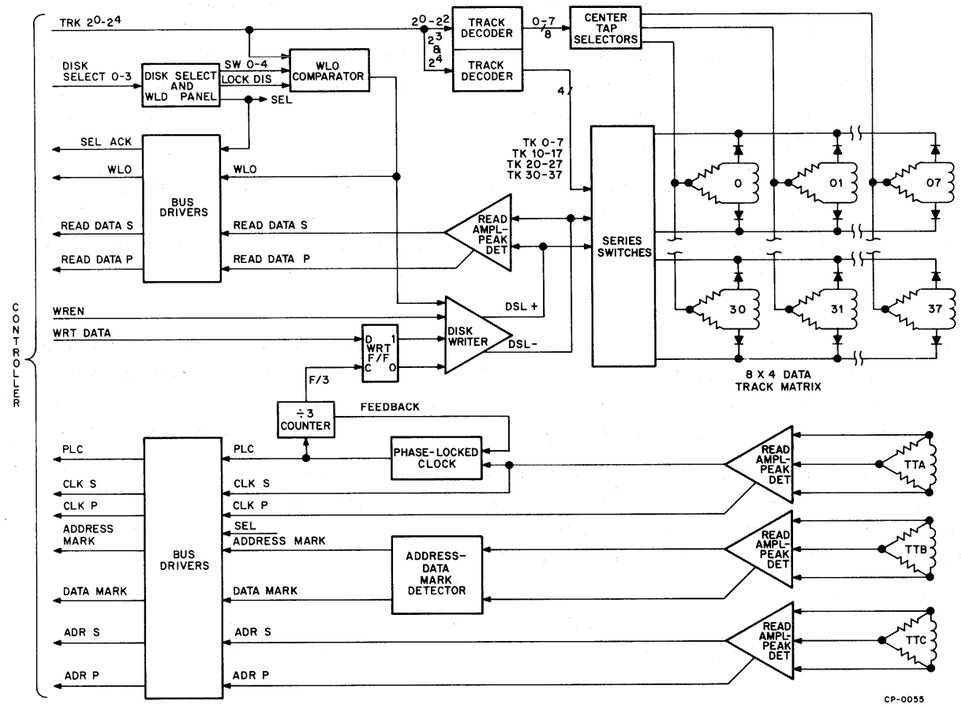


Figure 3-5 RS64 Functional Block Diagram

toggles on each binary 1 in the input. This action reverses the record head current each time a binary 1 is present and results in the recording of a binary 1 by reversing the flux saturation.

3.3.2 Timing Path Logic

Drawing D-BS-RS64-0-2 shows the circuits associated with disk timing. In general, these circuits reconstruct the digital form of disk timing tracks, synchronize an internal clock with the disk bit timing track (TTA), and provide timing information to a controller when the disk is selected by the controller. Bit timing is also provided to the write data path.

Differential inputs from timing track heads TTA, TTB, and TTC are applied to read amplifier-peak detector modules E-F08, E-F07, and E-F06, respectively. These modules convert the differential bipolar input pulses (representing logical 1's) into negative-true (0V) 300-ns strobe pulses at output pin E2. The leading edge of a strobe pulse occurs at approximately the peak of the input pulse. The read amplifier-peak detector modules also produce an output at pin H2 that signifies the polarity of the input pulse. This signal is negative-true (0V) for a positive-input pulse and has a pulse width corresponding to the duration of the input pulse. The strobe and polarity outputs of TTA and TTC are gated to the controller whenever the disk is selected. The strobe output (CLK S or ADR S) is used as a timing reference while the polarity output (CLK P or ADR P) is used for error checking functions.

The TTA read amplifier-peak detector also provides strobe pulses to a self-synchronizing phase-locked loop consisting of an M4201 phase-locked clock and two M205 D-type flip-flops connected as a divide-by-3 counter.

This loop synchronizes the output phase with the strobe pulses recovered from TTA. For this function, the M4201 phase-locked clock compares the time occurrence of the counter output (feedback) with the TTA strobe pulses and uses the result of these comparisons to correct the frequency of a VCO. Since this VCO drives the divide-by-3 counter, the self-correcting loop phase-locks the output phase to the TTA strobes. Counter timing relationships are provided in Figure 3-6. Additional information on the phase-locked clock is provided in the module descriptions (Paragraph 3.4.16).

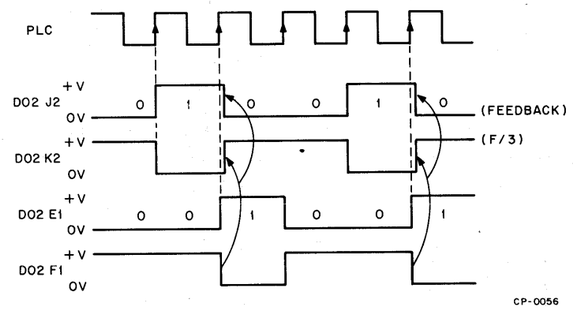


Figure 3-6 Counter Timing Relationships

As mentioned previously, TTB conveys the address and data markers signifying the beginning of address or data. The address marker is identified by a negative polarity pulse recovered from TTB and a data marker is identified by a positive polarity pulse recovered from TTB. For the detection of the markers, the strobe output of the TTB read amplifier-peak detector is ANDed with its polarity output. If the polarity output at F07–H2 is positive and a strobe pulse is present, the timing logic provides a 300-ns, negative-true address marker pulse to the controller. Similarly, if the polarity output at F07–H2 is at 0V and a strobe pulse is present, the timing logic provides a 300-ns, negative-true (0V) data marker pulse to the controller.

3.3.3 Data Path Logic

Drawing D-BS-RS64-0-3 shows the circuits for disk selection, write lockout, and the write and read data paths. For selection of a disk file, the controller ground-asserts one of four select lines (DSK 0–3). If the UNIT SELECT switch on the Disk Select/WLO panel is in a corresponding position, the ground-asserted input generates a SEL L gating level; a SEL ACK output is also returned to the controller. The SEL L signal gates disk timing, read data, and other signals to the controller bus. The SEL ACK output informs the controller the disk file is not in a power-down or off-line state so that the ensuing operation can proceed.

A write lockout function is implemented with an M167 comparator module. This module compares the controller track address (TK 2^0 – TK 2^4) with inputs from the binary-weighted TRK ADD switches. If the track address specified by the controller is equal to or less than the address selected by the TRK ADD switches, the M167 comparator output is a ground level. This output prevents turn-on of the G291 disk writer; thus, information on the track cannot be erased or changed. The ground level from the M167 comparator also generates a WLO L signal to the controller. In contrast, if the track address specified by the controller is greater than the switch selection, the M167 comparator provides an enable level to the G291 disk writer.

The upper part of D-BS-RS64-0-3 shows the circuit elements comprising the write and read data paths up to the data sense lines (+DSL and -DSL). From a logic viewpoint, these paths are straight-forward and, therefore, are not discussed in detail. However, the read/write electronics are described in subsequent paragraphs.

3.3.4 Read/Write Electronics

As mentioned previously, data is stored serially around the disk surface by 32 fixed data heads. The controller selects the active data read/write head with five binary-weighted lines. Drawing D-BS-RS64-0-4 shows the circuit elements for track selection. Note that the track address is decoded in two parts. One octal group (0–7, 10–17, 20–27, or 30–37) enables a related G295 series switch while decoding the lower order track address bits enables one G296 center tap selector. Once selected, the head reads or writes according to inputs from the controller.

The RS64 disk uses the Non-Return-To-Zero Inverted (NRZI) recording technique. In this technique, a change in the direction of the magnetic flux along the disk track represents a binary 1 and no change in the magnetic flux represents a binary 0. A binary 1 is written by reversing the direction of the write current in the recording head.

Figure 3-7 illustrates in simplified form the circuits used for writing and reading of data. A head winding is represented by coil L1. This coil forms the center leg of a bridge circuit consisting of resistors R1 and R2, isolation diodes D1 and D2, and switching transistors Q1 and Q2 in the G295 series switch module.

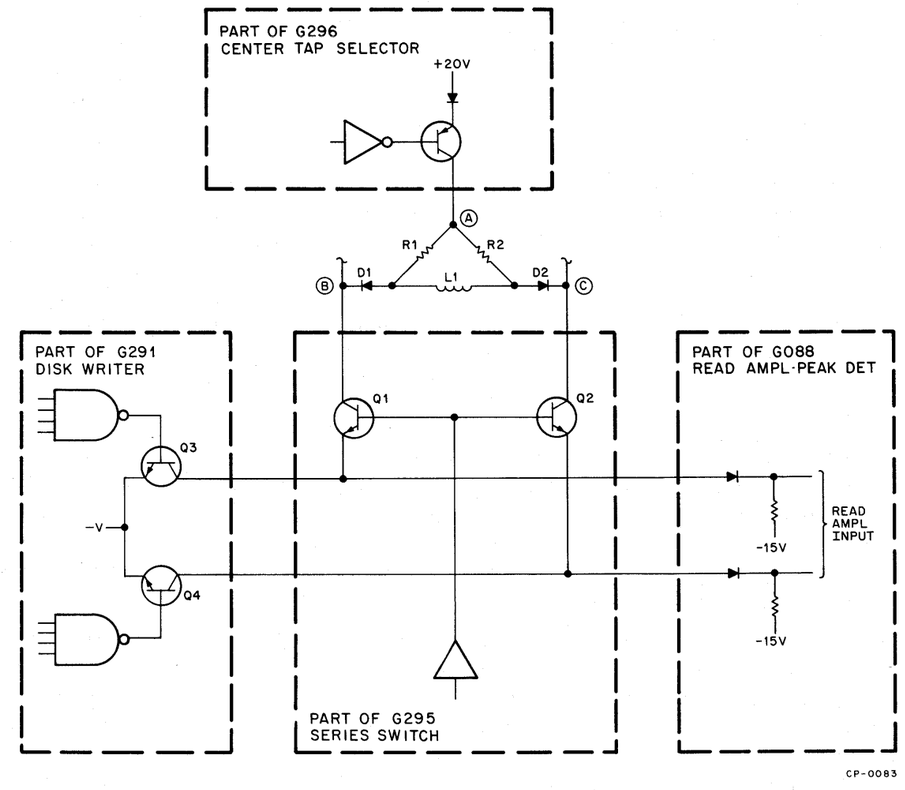


Figure 3-7 Read/Write Electronics

When the controller reads using this head, it does so by activating the appropriate G296 center tap selector module (to select one of eight matrix lines) and the appropriate G295 series switch module (to select one of four groups). This combination connects node A to +20V, switches transistors Q1 and Q2 on, forward biases diodes D1 and D2, and completes a 5 mA (approximate) current path through each leg of the bridge and the differential input of the read amplifier. With equal current in the legs, no current flows in the read/write head. When data is read, the changing magnetic field from the disk surface induces a voltage in the head that appears across the differential input of the G088 read amplifier-peak detector. This voltage is subsequently amplified and converted to a digital strobe. The polarity of the voltage across the coil is a function of the direction of flux change; thus, bipolar analog pulses are provided to the read amplifier.

For a write operation, the recording head is selected the same as for a read operation, but the bridge is unbalanced by switching the emitter of Q1 or Q2 to -15V via one of the transistors in the G291 disk writer module. This action forces approximately 45 mA through the head coil. The direction of current flow through the head is determined by which G291 transistor is active; this transistor switching, in turn, is controlled by the state of the write flip-flop.

Figure 3-8 shows the relationships of the read and write waveforms. For a write operation, the serial NRZ write (WRT) data is clocked by the positive transition in the bit rate (F/3) timing. Each binary 1 in the NRZ input complements the flip-flop which, in turn, switches one of the transistors in the G291 disk writer module on and its counterpart off. As a result, head current is reversed and the magnetic field is reversed on the disk surface.

Figure 3-8 also shows the corresponding analog and digital waveforms for a read operation. Note that the read voltage consists of bell-shaped pulses that peak at the maximum change in the flux pattern. Note also that the NRZI format results in bipolar pulses having alternate polarities, i.e., no two successive pulses have the same polarity. This characteristic, through the use of the DATA P output, can be used to detect errors.

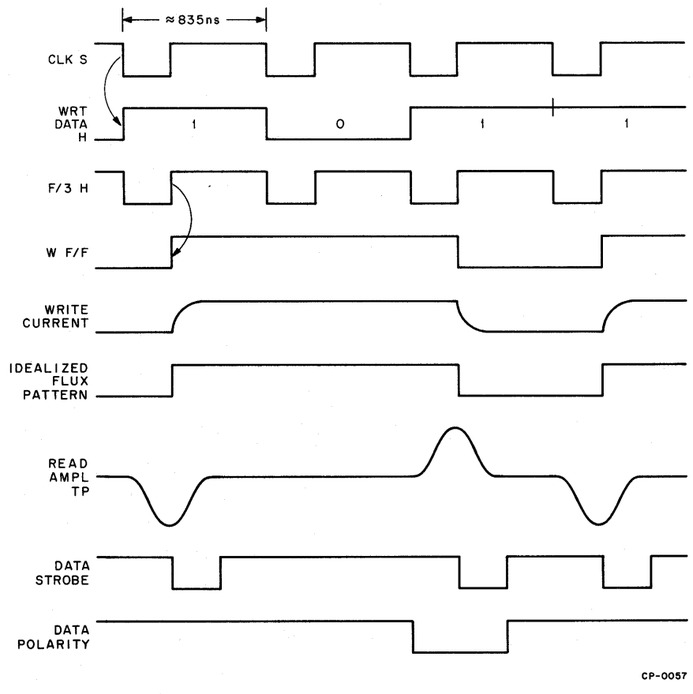


Figure 3-8 Write and Read Waveforms

3.3.5 Power Control Panel

Drawing D-AD-7006868-0-0 is a schematic of the 115V and 230V power control panels. These panels are functionally identical; they differ primarily in the wiring for the primary of the local/remote power transformer (parallel connections for 115V and series for 230V) drive motor connections and rating of various components. Each control panel contains:

a. a male receptacle for primary power,

b. a female utility receptacle,

c. an RFI filter (L1, L2, and C1),

d. a power input indicator,

e. 15-A circuit breaker CB1,

f. step-down transformer T1,

g. local/remote switch assembly S1 and

h. power supply relay K1.

Transformer T1 provides an 18 Vrms potential that is rectified by diodes on local/remote switch assembly S1. The resulting potential is used as a supply voltage to energize K1. The LOCAL/OFF/REMOTE switch completes the energizing path for K1 by providing a ground input to K1. This input can be supplied as a result of positioning the switch to LOCAL or by a remote switch closure when the switch is in the REMOTE position.

3.3.6 Power Supply

Refer to Appendix B for power supply coverage.

3.4 MODULE DESCRIPTIONS

3.4.1 G088 Read Amplifier-Peak Detector

The read amplifier-peak detector reconstructs the digital form of bipolar analog pulses read from disk timing and data tracks. Disk head inputs are provided in differential form and all outputs are TTL compatible.

Functionally, the G088 module consists of a differential amplifier and a peak detector as shown in Figure 3-9, Drawing DS-C-G088-0-1 is a schematic of the G088 module.

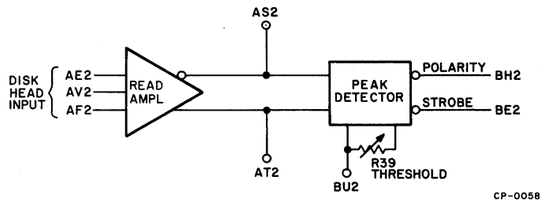


Figure 3-9 G088 Read Amplifier-Peak Detector Simplified Diagram

The read amplifier portion is a 3-stage, discrete-component differential amplifier (Q1 through Q6) with a 3 dB bandwidth from 60 kHz to 700 kHz. The amplifier has linear gain characteristics (up to a maximum gain of 1000) for low-level inputs (up to 10 mV) and nonlinear gain characteristics (gain compression) to prevent peak distortion at higher level inputs. Diodes D5, D6, D10, and D11 provide the gain compression features.

The differential output of the amplifier is ac-coupled to the peak detector. Figure 3-10 depicts the amplifier output and the waveforms for the peak detector. The peak detector portion detects the peaks of the bipolar pulses provided by the read amplifier and generates a 300-ns, negative-true strobe pulse for each peak. It also generates a polarity output denoting the polarity of the peak; a negative pulse denotes a positive polarity input pulse. Two test points (AS2 and AT2) permit monitoring of the amplified output.

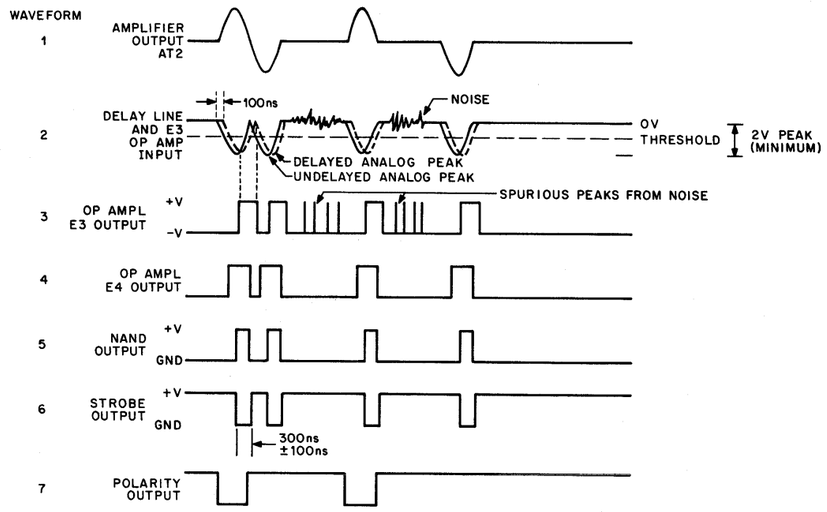


Figure 3-10 G088 Read Amplifier-Peak Detector Waveforms

Transistor stages Q8 and Q9 (with diodes D12 and D13) rectify the bipolar pulse input and provide a single-ended signal to the 100-ns delay line and amplifier E3. Peak detection is accomplished by delaying the analog input by 100 ns then comparing the magnitude of the delayed signal with the undelayed signal. Stage E3 functions as an analog voltage comparator that is operated open-loop. Its output saturates positive whenever the delayed analog signal is more negative than the undelayed analog signal (Figure 3-10). Conversely, its output is negative whenever the difference in the analog inputs is zero or the undelayed input is more negative than the delayed input. Thus, its output approximates a digital form and is positive for each analog peak.

When both the delayed and undelayed analog inputs are at zero (no peaks), any noise that exceeds the input threshold of E3 causes spurious peaks in its output. To eliminate this aspect, the delayed analog signal is compared with a voltage reference (provided by R39 and R42) at operational amplifier E4 and the output of E4 remains negative unless the analog input exceeds the threshold reference. This threshold is set such that noise peaks cannot drive the output of E4 positive yet data peaks can. Since the output of E4 is ANDed with the output of E3, the net effect cancels noise peaks in the output of NAND gate E1 (Waveform 5, Figure 3-10). Test point BU2 is provided for adjusting the threshold. This reference is set to the midpoint between maximum noise peaks and minimum data peaks. Nominally, this reference is -1.2V.

The pulsewidth of the strobe output is standardized by one-shot E2. This circuit, triggered by a negative transition, produces a nominal 300-ns strobe pulse. The leading edge of this pulse denotes the data peak position. This pulse is inverted for a negative-true strobe output (Waveform 6, Figure 3-10).

Transistor stage Q7 produces a polarity pulse for each positive pulse in the disk head input. The output of Q7 is inverted for a negative-true pulse. This pulse has a duration corresponding to the width of the input pulse.

INPUTS:

Pin	Use	Drive or Load
AE2, AF2	Head Differential Input	5 to 10 mV
AV2	Head Center Tap	----

OUTPUTS:

Pin	Use	Drive or Load
BE2	Strobe (300 ±100 ns)	10 TTL loads*
BH2	Polarity	10 TTL loads
AS2, AT2	Read Amplifier Output Test Points	----
BU2	Peak Detector Threshold Test Point	----

POWER:

Pin	Use
BA2	25 mA at +5V
AB2, BB2	60 mA at -15V
AC2, BC2	GND
AA2, BD2	60 mA at +20V

*One TTL unit load is 1.6 mA (maximum).

3.4.2 G291 Disk Writer

The disk writer records information on a disk. Functionally, it consists of an 80-mA differential-current amplifier with two 4-input AND gates for accepting complementary TTL data inputs (and gating signals) as shown in Figure 3-11. The module also contains a power-fail sensor that holds the writer off during power-up or power-down sequencing.

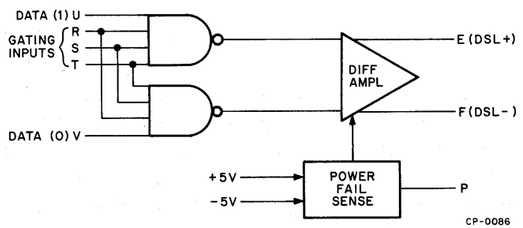


Figure 3-11 G291 Disk Writer Simplified Diagram

Transistor stages Q1 through Q4 (Drawing CS-G291-0-1) comprise the differential-current amplifier. Stages Q1 and Q4 are the differential input pair. Stages Q2 and Q3 function as the current sinks for writing. These stages complete the write current path between -15V and the data sense lines (DSL). With the data input to pin U a logical 1 (and gating inputs at +3V), Q3 completes the current path for the DSL (-) line. Similarly, with the data complement at pin V a logical 1, Q2 connects -15V to the DSL (-) line.

Transistors Q5 and Q6 (with breakdown diodes D3 and D17) monitor the +5V and -15V for a power fail condition. When the sum of these potentials drops below 16.4V, Q2 and Q3 are clamped off. This feature prevents the disk writer from recording extraneous information on the disk during power-up or power-down sequencing. A power fail output is also made available at pin P. This output is low (0V) whenever power is below the power-fail threshold.

INPUTS:

Pin	Use	Drive or Load
U2	Data Input	1 TTL load
V2	Complementary Data Input	1 TTL load
R2, S2, T2	Write Enable	2 TTL loads each

OUTPUTS:

Pin	Use	Drive or Load
F2	Write Output	80 mA (nominal)
E2	Complementary Write Output	80 mA (nominal)
P2	Power Fail	10 TTL loads

POWER:

Pin	Use
A2	30 mA at +5V
B2	85 mA at -15V
C2	GND
D2	1 mA at +20V

3.4.3 G295 Series Switch

The G295 module is a single-height module containing two series switch circuits. It is used with the G296 center tap selector module to select disk track read/write heads. Functionally, each series switch circuit consists of an input level converter and a driver and two NPN current switches as shown in Figure 3-12.

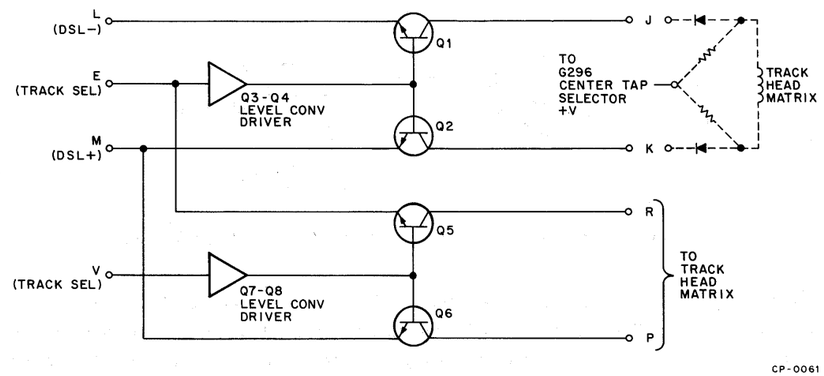


Figure 3-12 G295 Series Switch Simplified Diagram

Pin E (or V) accepts a TTL track select input. When this input is a logical 1 (+3V), the level converter-driver provides base drive for current switch pair Q1 and Q2. One of these switches, in turn, provides a current path between a Data Sense Line (DSL- or DSL+) and a track head selection matrix and passes either the 80-mA write current or the 5 to 10-mV read signal. This current path is completed by a G296 center tape selector module.

INPUTS: TTL levels (0V and +3V) to pins E and V; -15V and 0V to pins L and M.

Pin	Use	Drive or Load
E and V	Track Select Enabling	1 TTL load
L and M	Complementary Data Sense Line outputs of Disk Write Module	Capable of sinking 80 mA

OUTPUTS: Voltage levels of 0V or -15V. Each series switch pole can drive up to 150 mA. At a load current of 100 mA, the internal voltage drop is approximately 1V.

INPUT/OUTPUT DELAY: 1 μs

POWER:

Pin	Use
B2	81 mA at -15V
D2	2 mA at +20V
A2	20 mA at +5V
C2	GND

3.4.4 G296 Center Tap Selector

The G296 is a single-height module that is used with a G295 series switch module to select a disk read/write head. The G296 module selects the center tap axis of this matrix, while the G295 module selects the other axis of the matrix. The module consists of four identical circuits. Each circuit uses a TTL input stage and driver and a PNP transistor switch as shown in Figure 3-13.

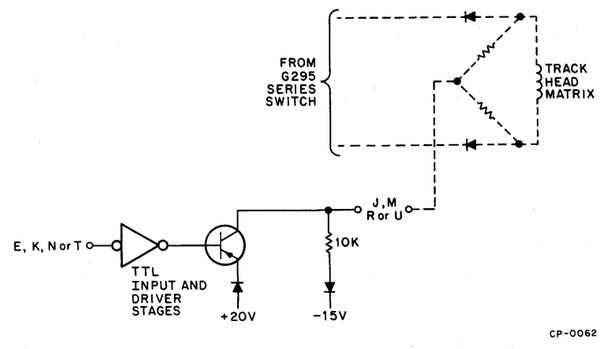


Figure 3-13 G296 Center Tap Selector Simplified Diagram

With the TTL input at pin E, K, N, or T at 0V, the circuit connects the respective output (pin J, M, R, or U) to the +20V source. This action, with that of the G295 series switch, provides a current path for reading or writing.

Conversely, when the TTL input is at +3V, this circuit provides a -15V potential to the head selection matrix.

INPUTS: TTL levels (0V and +3V) to pins E and V; -15V and 0V to pins L and M

Pin	Use	Drive or Load
E, K, N and T	Digital Input (Track Select)	1 TTL load each

OUTPUTS: Each output provides 150 mA (maximum) at +10V when respective input is 0V.

POWER:

Pin	Use
A2	11 mA at +5V
B2	22 mA at -15V
D2	81 mA at +20V
C2	GND

3.4.5 G738 Terminator

The G738 is a single-height module used as a cable bus terminator at the controller end of an RS64 Disk File interface. Ten pins terminate the "fast" signal bus lines, i.e., lines that convey information by signal transition or signals having a duration less than 100 ns. These pins provide an 82-ohm termination to ground. Fifteen pins provide termination for the "slow" signal bus lines (signals strobed by fast signals). These pins provide a termination of 180-ohms to +5V and 330 ohms to ground, yielding a Thevinin termination of 117 ohms and 3.25V.

INPUTS:

Pin	Use
D2, E2, H2 K2, M2, P2 S2, T2 and V2	82 ohms pulldown to ground
D1, E1, F1, H1, J1 K1, L1, M1, N1 P1, R1, S1, A1, B1 and V1	180 ohms to +5V and 330 ohms to ground
F2, J2, L2, N2 R2 and U2	GND

POWER:

Pin	Use
A2	20 mA at +5V
C2	GND

3.4.6 G739 Peripheral Terminator

The G739 is a single-height module used as a cable terminator for the last drive on the bus. Ten pins terminate the "fast" signal bus lines. These pins provide an 82-ohm pullup to +5V. Fifteen pins provide termination for the "slow"

signal bus lines. These pins provide a termination of 180 ohms to +5V and 330 ohms to ground, yielding Thevinin termination of 117 ohms and 3.25 volts.

INPUTS:

Pin	Use
D2, E2, H2 K2, M2, P2 S2, T2 and V2	82 ohms pullup to +5V
D1, E1, F1, H1, J1 K1, L1, M1, N1 P1, R1, S1, A1, B1 and V1	180 ohms to +5V and 330 ohms to ground
F2, J2, L2, N2 R2 and U2	GND

POWER:

Pin	Use
A2	20 mA at +5V
C2	GND

3.4.7 G8001 Low-Voltage Detector

This module monitors the unregulated +5V from the power supply to inform a processor of an impending loss of dc power for the disk file and its controller. The AC LO signal is generated approximately 3 ms before the +5V reaches a nonusable value, thus a processor can use this feature to enter a power-fail routine for saving pertinent data. Detection of a low-voltage condition occurs when the unregulated +5V drops to approximately 65 percent of its nominal value. When this action occurs, the low-voltage detector generates a negative-true (0V) AC LO output. During a power-up sequence, the AC LO signal remains at 0V for a minimum of 3 ms of usable power. This feature can be used to initiate a processor power-restore routine.

INPUT:

Pin	Use	Load
E2	Unregulated +5V	1 mA

OUTPUT:

Pin	Use	Drive
H2	AC LO	Low; 0.8V (max) at 50 mA High; 25 μA (max) at 3.5V

POWER:

Pin	Use
A2	20 mA at +5V
C2	GND

3.4.8 M111 Inverter

The M111 contains sixteen independent inverters.

INPUTS: Voltage levels of 0V and +3V (typical). Each input presents one TTL unit load.

OUTPUTS: Voltage levels of 0V and +3V (typical). Each output can drive 10 TTL unit loads.

POWER: 87 mA (max) at +5V.

3.4.9 M113 2-Input NAND Gate

The M113 contains ten 2-input NAND gates used for general-purpose gating functions. The module also contains a divider network so that any unused inputs of a gate can be connected to +3V for maximum noise immunity. Pins U1 and V1 are provided for this function; each can supply up to 40 TTL unit loads.

INPUTS: Voltage levels of 0V and +3V (typical). Each input presents 1 TTL unit load.

OUTPUTS: Voltage levels of 0V and +3V (typical). Each output can drive 10 TTL unit loads.

Propagation Delay: 15 ns (typical)

POWER: 71 mA (max) at +5V

3.4.10 M163 Dual Binary-To-Decimal Decoder

The M163 consists of two independent binary-to-decimal decoding structures on a single-height module (see Figure 3-14). Each decoder produces a negative-true (0V) output for the decimal equivalent of the binary input.

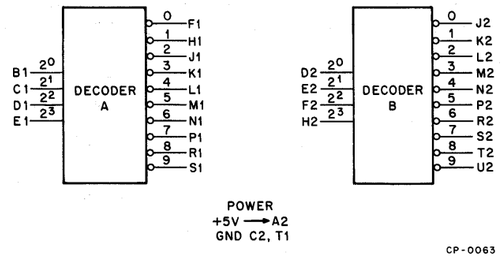


Figure 3-14 M163 Decoder Simplified Diagram

Each decoder can also be used for octal or quad decoding by grounding the most significant bit (MSB) line or MSB and next MSB input lines. Each decoder has a propagation delay of 40 μs (maximum) for input-to-output turn-on or turn-off.

INPUTS: Voltage levels of 0V and +3V (typical). All inputs present 1 TTL unit load each.

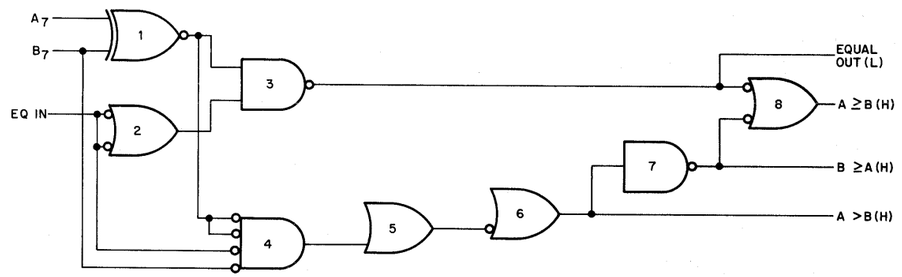
OUTPUTS: Voltage levels of 0V and +3V (typical). All outputs are capable of driving 10 TTL unit loads.

POWER: 58 mA (typical) at +5V.

3.4.11 M167 Magnitude Comparator

The M167 module compares the magnitude of two 8-bit binary numbers and provides four outputs defining the relationships of these numbers. For example, for two numbers designated A and B, the comparator defines whether A = B, A > B, A ≥ B, or B ≥ A. In addition, an EQUAL IN input enables cascading of modules so that comparison can be performed for greater than 8-bit numbers. For the comparison of less than 8-bit numbers, unused comparison inputs are connected to +3V and the EQUAL IN input is connected to ground.

The basic logic structure for a binary stage consists of an EXCLUSIVE OR, two 2-input NAND/NOR gates (one used as an inverter) and one 4-input NAND/NOR as shown in Figure 3-15. The remaining logic elements in Figure 3-15 are common to all stages. A truth table is provided for the stage; it assumes all higher order inputs are equal (EQUAL IN in 0V).



EQUAL IN	A_7	B_7	EQUAL OUT	A≥B	B≥A	A>B
T (0V)	0 (0V)	0 (0V)	T (0V)	T (+3V)	T (+3V)	F (0V)
T	0	1	F	F	T	F
T	1	0	F	T	F	F
T	1	1	T	T	T	T

CP-0064

Figure 3-15 M167 Comparator Simplified Diagram

A principle use of this module is to compare track addresses for a write lockout function. For this application, a track address is connected to the "A" input, write lockout switch levels are connected to the "B" inputs, and the A > B output controls the write operation. With this arrangement, a write operation is disabled whenever the track address is equal to or less than the write lockout switch setting. In addition, the write lockout function can be disabled entirely by simulating a track address-greater-than-switch input to the MSB stage. For this function, the MSB "B" input is connected to ground and the MSB "A" input is switched to +3V. Conversely, to enable the write lockout function, the MSB "A" input need only be switched to 0V.

INPUTS: Voltage levels of 0V and +3V (typical) for all TTL inputs.

Pin	Use	Drive or Load
F2	A_0 (MSB)	1 TTL load
H1	A_1	
E2	A_2	
F1	A_3	
C1	A_4	
J1	A_5	
K1	A_6	
B1	A_7 (LSB)	

INPUTS: (cont)

Pin	Use	Drive or Load
H2	B_0 (MSB)	2 TTL loads
S1	B_1	
D2	B_2	
E1	B_3	
D1	B_4	
M1	B_5	
M2	B_6	
A1	B_7 (LSB)	
U2	EQUAL IN	3 TTL loads

OUTPUTS: Voltage levels of 0V and +3V (typical) for all outputs.

Pin	Use	Drive or Load
P1	EQUAL OUT (L)	7 TTL loads
R1	EQUAL OUT (H)	10 TTL loads
V1	A > B (H)	8 TTL loads
U1	B ≥ A (H)	9 TTL loads
L1	A ≥ B (H)	10 TTL loads

POWER:

Pin	Use
A2	20 mA at +5V
C2, T1	GND

3.4.12 M205 D-Type Flip-Flop

The M205 module contains five D-type flip-flops. Each flip-flop has independent DATA, CLOCK, SET, and CLEAR inputs. Information must be present on the DATA input 20 ns (maximum) before the CLOCK pulse and the information should remain at the input at least 5 ns (maximum) after the CLOCK pulse has passed the threshold voltage. Data transferred into the flip-flop by the previous CLOCK pulse will be present on the 1 output of the flip-flop. Typical time duration of the CLOCK pulse preset and reset pulses is 30 ns each. Maximum delay through the flip-flop is 50 ns.

INPUTS: D inputs present 1 TTL unit load each.
C inputs present 2 TTL unit loads each.
SET inputs present 2 TTL unit loads each.
CLEAR inputs present 3 TTL unit loads each.

OUTPUTS: Each output (0 and 1) is capable of driving 10 TTL unit loads. Two +3V supplies (U1 and V1), capable of 25 unit loads, are available.

POWER: 100 mA (maximum) at +5V.

3.4.13 M623 Bus Driver

The M623 module contains twelve 2-input bus drivers capable of driving the positive input bus of a computer. Drivers are arranged in six pairs, with each pair having a common gating line and two data bit inputs. For simultaneous gating of data bits, the common gating lines of each pair are connected to a single gating source. For direct output (without gating), the common gating lines are connected to signal ground. The driver output is then at ground when both inputs are at ground. Output rise and fall times are 30 ns (maximum) for a 100-mA resistive load.

INPUTS: Pins C1, J1, P1, F2, M2, and T2 present two unit loads, when used for pair gating. Pin C1 presents 12 unit loads when connected to all other common gating lines. Pins A1, B1, F1, H1, M1, N1, D2, E2, K2, L2, R2 and S2 each present one unit load.

OUTPUTS: All outputs can sink 100 mA to ground. An open-collector NPN transistor is used as an output stage, and all output lines are protected from negative voltage of -0.3V or greater. A maximum collector voltage of +20V can be used.

POWER: 71 mA at +5V (max) plus external load.

3.4.14 M901 Flat Mylar Cable Connector

This connector module allows 36 lines to be used for signals and grounds. The 100-ohm resistors connected in series with pins A2, B2, U1, and V1 provide some measure of protection if these pins are inadvertently connected to a source voltage.

INPUTS: Recommended current per line is 100 mA maximum.

3.4.15 M908 Ribbon Connector

The M908 cable connector consists of a single-height, double-sided board that contains 36 split pins for the connection of 36 separate wires. All connections are made on the component side of the module.

3.4.16 M4201 Phase-Locked Clock

The M4201 clock synchronizes disk read/write operations with the bit timing strobes recovered from a disk timing track. Basically, it consists of a phase error detector and a VCO operated in a self-synchronizing phase-lock loop as shown in Figure 3-16.

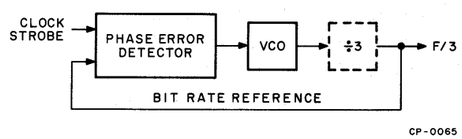


Figure 3-16 M4201 Phase-Locked Clock Simplified Diagram

The VCO has a natural (or center) frequency of approximately 3.6 MHz; it drives an external divide-by-3 counter that provides a bit rate reference for the phase-lock loop. A phase error detector compares the time occurrence of the clock strobes from a disk with the bit rate reference. Errors resulting from the comparison are then integrated and converted to an analog voltage that adjusts the VCO frequency accordingly. This loop synchronizes the VCO with the clock strobes within a nominal 300 μs.

The phase error detector consists of a digital comparator stage, fast-integrator E4, long-term integrator E5, and linear amplifier E6, as shown in Drawing D-CS-M4201-0-1. The digital comparator stage consists of two D-type flip-flops in IC E2 and a NAND latch in IC E3. These logic elements accept the clock strobe input (pin BE) and bit rate reference input (pin BH) and generate pulse outputs that drive the differential inputs of E4. Figure 3-17 shows the waveforms produced by these logic elements for both a phase lead and a phase lag. The shaded areas depict the error inputs applied to the differential inputs of E4. The output of E4 is proportional to the difference between the two inputs and thus represents the bit-by-bit phase error. Integrator E5, in turn, averages the bit-by-bit phase error for long-term stability. The outputs of E4 and E5 are added. The output at AV2 thus contains a component from E4 that corrects phase errors and a component from E5 that provides frequency lock. Amplifier E6 functions as a unity-gain inverting amplifier to provide the correct drive to VCO. Its output at pin AV2 is negative for a phase lead and positive for phase lag.

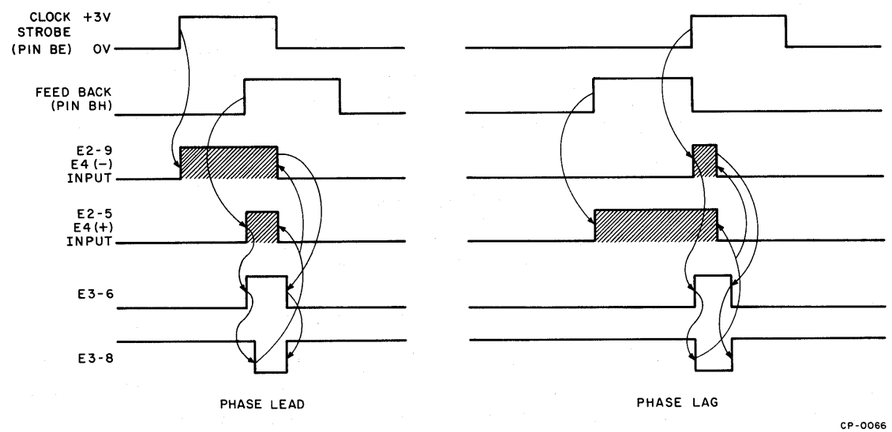


Figure 3-17 M4201 Phase-Locked Clock Waveforms

The VCO is a discrete-component RC oscillator consisting of transistor stages Q1 through Q7. It has a natural frequency of approximately 3.6 MHz (determined primarily by the network comprised of C18, R9, R26, and R11). Integrated circuit E1 buffers the VCO output and provides the necessary output drive. The clock output at pin BK is a square wave with a near 50 percent duty cycle.

INPUTS: Voltage levels of 0V and +3V (typical)

Pin	Use	Drive or Load
BE2	Clock Strobe	1 TTL load
BH2	Feedback (Bit Rate Reference)	1 TTL load

OUTPUTS: Voltage levels of 0V and +3V (typical) for all digital outputs.

Pin	Use
BK2	Phase Lock Clock
BD2	Digital Comparator Test Point

OUTPUTS: (cont)

Pin	Use
BN2	Digital Comparator Test Point
AV2	Phase Detector Analog Output
AU2	VCO Control Input

CLOCK STABILITY: Phase jitter between clock strobe and phase-lock clock is less than 100 ns.

SYNCHRONIZING TIME: 300 μs or less

POWER:

Pin	Use
AK2	15 mA at +20V
BA	100 mA at +5V
AH	10 mA at -15V
AC, BC	GND

3.4.17 8-Track Matrix 5408996

This module is part of a data cable assembly that connects the track selection logic to the data track read/write heads. It contains current-limiting resistors and isolation diodes for an 8-track data matrix.

3.4.18 Timing Head Matrix 5408937

This connector module is part of a timing cable assembly that connects the timing head shoe to the read amplifier-peak detector modules. It contains current-limiting resistors and connections for six timing heads.

CHAPTER 4
INTERFACING

4.1 BUS VOLTAGE SPECTRUM

The recommended voltage spectrum for an RS64 controller interface is shown in Figure 4-1.

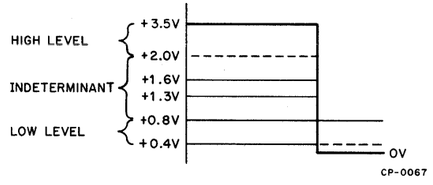


Figure 4-1 Voltage Spectrum for Controller Bus

4.2 BUS PHILOSOPHY

A cable assembly consisting of two 19-conductor flat Mylar cables is used for the RS64 controller bus. One cable should be used to convey 10 "fast" bus signals, i.e., signals that convey information via a signal transition or that can be 100 ns or less in duration. This cable should have alternate signal and ground conductors and be terminated with 82 ohms to +5V at the RS64 and 82 ohms to ground at the controller as shown in Figure 4-2.

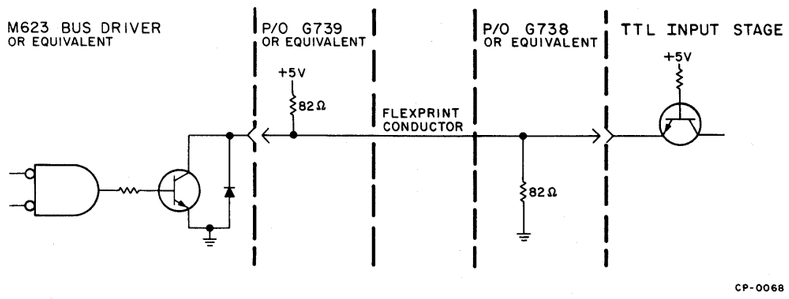


Figure 4-2 "Fast" Bus Configuration

The second 19-conductor cable should be used to convey 16 "slow" bus signals, i.e., signals that are strobed by the "fast" signals or used only as a level. These signals should be terminated by 180 ohms to +5V and 330 ohms to ground at each end of the cable as shown in Figure 4-3.

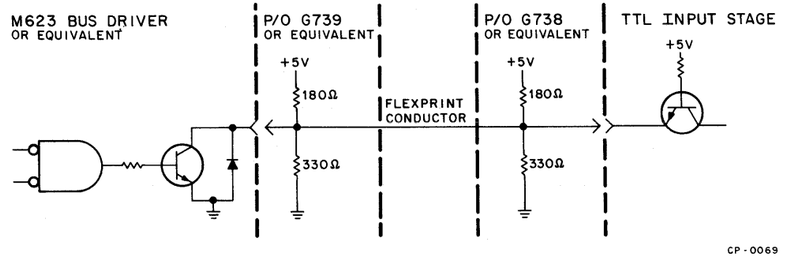


Figure 4-3 "Slow" Bus Configuration

The two cables should be separated by a solid Mylar shield and attached to one M901 connector at one end to form an assembly capable of handling at least 24 signals. Signal polarity is chosen to minimize logic and to make the bus fail-safe for a power failure or unplugging of the bus cable.

4.3 INTERFACE SIGNALS

Figure 4-4 defines: *(a)* the signals for an RS64-controller interface, *(b)* the signal assertion level, *(c)* the source of the signal and *(d)* the pin usage at the RS64 Disk File end. Each interface signal is described in subsequent paragraphs.

4.3.1 Disk Select (DSK SEL) 0–3

Up to four disk files can be used with one controller, thus each file must be assigned a unit number. Each RS64 has a 5-position rotary switch (0–3 and OFF) for assigning a unit number or placing the unit off-line. The four DSK SEL lines are wired to corresponding positions on this switch. To select a disk for a read or write operation, the controller ground-asserts the select line corresponding to the disk unit number. No interlocks are provided to prevent multiple disk files from being assigned the same unit number.

4.3.2 Select Acknowledge (SEL ACK)

This signal indicates that a disk file (or files) has been selected and that the selected unit does not have a power-fail condition. This line is negative-true (0V) for a select acknowledge condition.

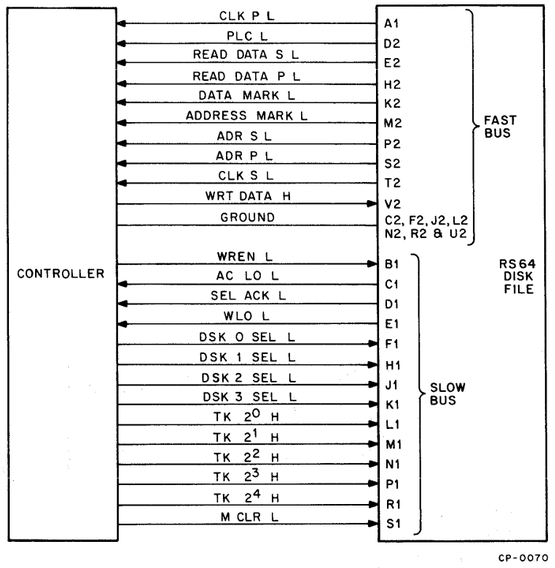


Figure 4-4 RS64 Controller Interface

4.3.3 Track Select (TK SEL) $2^0 - 2^4$

These five binary-weighted lines select one of 32 ($00_8 - 37_8$) data tracks for a read or write operation. Each disk file decodes these lines regardless of the file selected. Positive-true inputs are used.

4.3.4 Write Lockout (WLO)

This signal denotes that the write lockout feature is enabled for the selected track. This signal is negative-true (0V) for a write lockout condition.

4.3.5 Clock Strobe (CLK S)

This signal line conveys the bit timing information recovered from the disk. The negative-going leading edge of each 300-ns pulse occurs at the peak of the recovered data (at each transition).

4.3.6 Clock Polarity (CLK P)

This signal indicates the polarity of the peak for each clock strobe. A negative-true (0V) pulse denotes a positive peak and the absence of a pulse denotes a negative peak. The clock polarity pulse can be strobed by the leading edge of the clock strobe for error detection since two or more successive pulses of the same polarity indicate an error.

4.3.7 Address Mark

This signal line conveys 300-ns pulses denoting the start of the address portion of a sector. The leading edge of each negative-true pulse corresponds to the peak of the address mark recovered from the disk.

4.3.8 Data Mark

This signal line conveys 300-ns pulses denoting the start of a data sector. The leading edge of each negative-true pulse corresponds to the peak of the data mark recovered from the disk.

4.3.9 Address Strobe (ADR S)

This signal line conveys the address information (sync, address, and parity bits) recovered from the disk. Each 300-ns negative-true strobe signifies a logical one and the absence of a pulse signifies a logical zero. The leading edge of each strobe corresponds to the peak of a detected bit.

4.3.10 Address Polarity (ADR P)

This signal indicates the polarity of the peak for each address strobe. A negative-true (0V) pulse indicates a positive peak; the absence of a pulse denotes a negative peak. The address polarity pulse can be strobed by the address strobe for error detection.

4.3.11 Read Data Strobe

This signal line conveys 300-ns negative-true (0V) pulses denoting logical ones in data read from the disk; a logical zero is denoted by the absence of a strobe pulse. As with the timing strobes, the leading edge of each pulse corresponds to the peak of the detected pulse.

4.3.12 Read Data Polarity

This signal indicates the polarity of the data peak for the read data strobe. A negative-true (0V) pulse denotes a positive peak; the absence of a pulse denotes a negative peak. This signal can be strobed by the read data strobe for error detection.

4.3.13 Write Enable (WREN)

This signal controls the writing of data on the disk. A low-level signal (0V) enables a write operation if the write lockout feature is not enabled for the selected track. Write current is turned on as soon as WREN is asserted. Write current 10-percent turn-off and 90-percent turn-on levels are established 200 ±100 ns after a change in WREN. Therefore, WREN should be switched on and off with the Address Parity bit (at least 300 ns before the DATA MARK) to ensure adequate write current transition time.

4.3.14 Write (WRT) Data

This signal line conveys the serial NRZ data to be written on the disk. A positive-true (+3V) signal denotes a logical one in the data stream. Write data should be clocked with the leading edge of CLK S.

4.3.15 Phase-Locked Clock (PLC)

This signal line conveys clock timing having a frequency of three times that of the CLK S frequency or 3X bit rate (approximately 3.6 MHz) and is in phase with CLK S. Phase jitter between CLK S and PLC is less than ±100 ns over the full operating speed.

4.3.16 Master Clear (M CLR)

This signal clears the disk write flip-flop and disables the disk writer circuits. This negative-true (0V) signal overrides any other disk signals and can be used for power-up control.

4.3.17 AC Low (AC LO)

This signal, when ground-asserted, signifies an impending loss of dc power for the disk file and the controller. Approximately 3 ms of usable power remains after this signal is switched to 0V, thus a processor can use this signal to enter a power-fail routine for saving pertinent data.

4.4 FORMAT REQUIREMENTS

The overall requirements for disk formatting are as follows:

a. Recording Technique – NRZI recording will be used and data will be recovered using a self-synchronizing phase-locked clock. The peak of a logical one flux transition, when read, is defined as the nominal data bit location.

b. Disk Speed – The disk maintains a speed from approximately 1400 to 1800 rpm for worst-case input voltage and frequency extremes.

c. Origin Gap – An origin gap of sufficient length (50 μs or greater) will be used to facilitate writing of timing tracks.

d. Phase-Locked Clock – The phase-locked clock synchronizes with the bit timing track of the disk. This clock re-synchronizes with the bit timing within 300 μs after the origin gap.

e. Sector Gaps – Sector gaps should be long enough to tolerate worse-case speed variations and to overlap the writer turn-off functions.

f. Synchronizing Preamble – Each address and data sector will begin with a logical one – zero synchronizing pattern to provide intersymbol interference – free synchronization.

g. Clock Skew – Total dynamic and static skew (any clock to any other clock) is less than ±2 μs from the nominal bit position.

h. Data-Clock Skew – Total dynamic and static skew (any clock to any data) less than ±4 μs from nominal bit position.

i. Amplifier Recovery – An interval of at least 300 μs should be allotted for write-to-read switchover or for switching of tracks.

j. Synchronization – Data on a track should be segmented in no fewer than 32 equal-sized blocks and should be synchronized for each block.

4.5 SYNCHRONIZING LOGIC

4.5.1 Write Synchronization

The primary requirements for synchronizing a write operation are as follows:

a. WRT DATA must be clocked by the leading edge of CLK S.

b. WREN must be asserted at least 300 ns before DATA MARK. WREN can be negated at the end of the last word to be written or at the next ADDRESS MARK denoting the start of another sector.

Figure 4-5 shows the timing for synchronization.

4.5.2 Read Synchronization

The read synchronizing logic generates read clock pulses for reading of data addresses. These clock pulses are synchronized with the phase-locked clock of the RS64 Disk File.

Figures 4-6 and 4-7 show the logic circuits and timing recommended for read synchronization. Although the circuits and timing are labeled for data usage, the same circuits and timing can be used for reading address information. If the disk format does not require simultaneous usage of the circuit for both data and address, then the same circuit can be used with input gating of ADDRESS STROBE or DATA STROBE. If, however, simultaneous usage is required, duplicate circuits can be used.

The read synchronizing logic generates READ CLK pulses only during the reading of the data or address portions of a block. The READ signal provides the primary control for this function. This signal is clocked by the DATA MARK or ADDRESS MARK as shown in Figure 4-7. With this signal at a ground level, the DATA, START SYNC, SYNC DATA, and START BIT flip-flops are held reset and READ CLK pulses are negated. With the READ signal asserted, these circuits provide a READ DATA output and generate the READ CLK pulses for strobing data.

The DATA flip-flop, Figure 4-6, accepts the data input from the read amplifier-peak detector. Each DATA STROBE (denoting a logical one in the data stream) triggers a 50-ns one-shot; this stage, in turn, direct sets the DATA flip-flop. The START SYNC and SYNC DATA flip-flops select the correct phase of the phase-locked clock to be used for READ CLK pulses. The PA and PB flip-flops form a 3-state counter. A count of one is decoded to control the output gating of the selected phase. The START BIT flip-flop bypasses or prevents generation of READ CLK pulses for the sync pattern so that the first READ CLK pulse occurs with the first data bit.

The trailing edge of each READ CLK pulse is used to sample or clock the READ DATA output. With this usage, the system results in data being sampled midway between the nominal DATA STROBE position as defined by the sync bits.

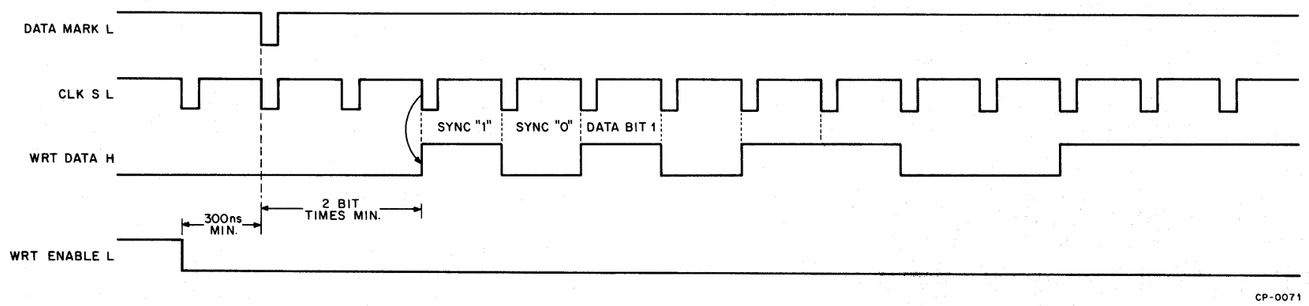
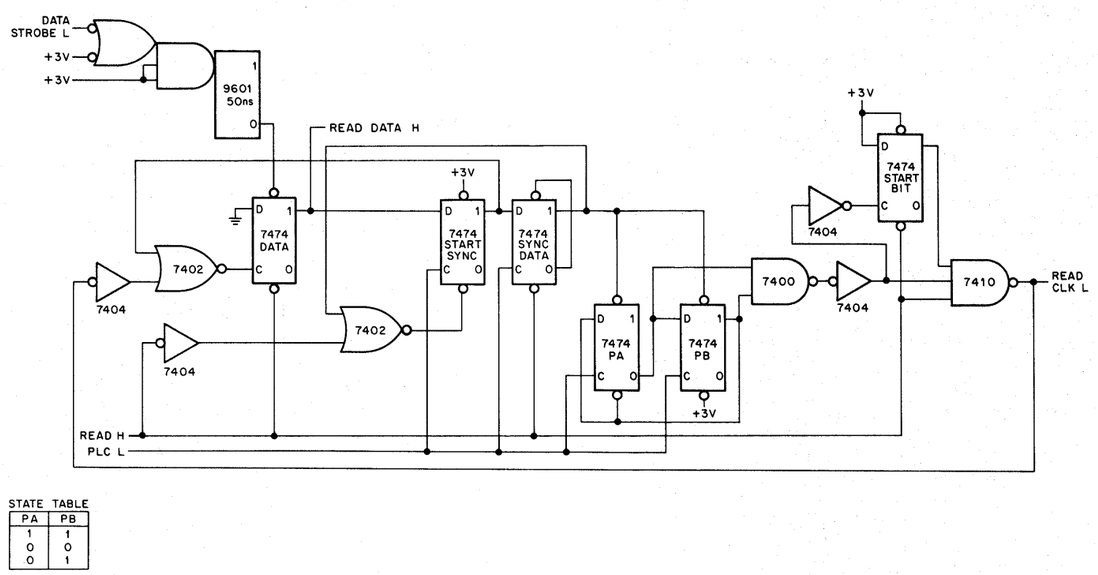


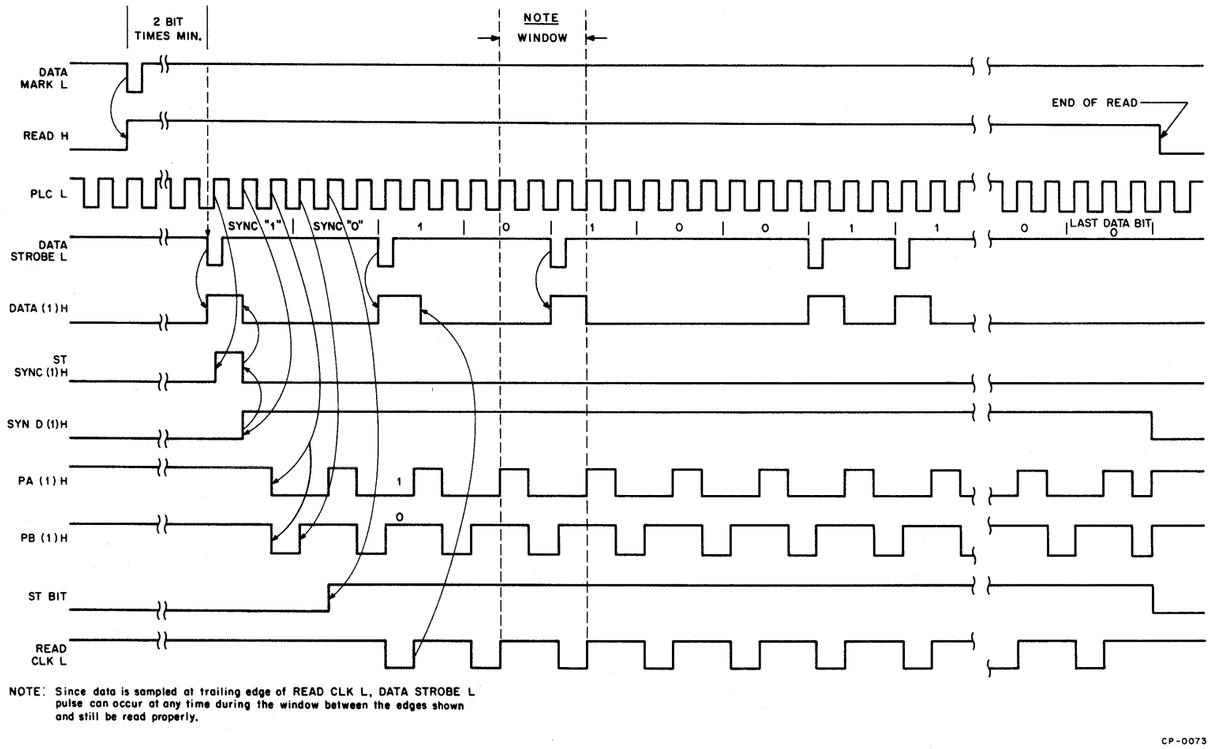
Figure 4-5 Write Synchronization



STATE TABLE

PA	PB
1	1
0	0
0	1

Figure 4-6 Read Synchronizing Interface Logic



NOTE: Since data is sampled at trailing edge of READ CLK L, DATA STROBE L pulse can occur at any time during the window between the edges shown and still be read properly.

Figure 4-7 Read Synchronizing Interface Timing

CHAPTER 5
MAINTENANCE

5.1 GENERAL

This chapter contains instructions for maintaining the RS64 Disk File. The instructions are intended for field level servicing by the user, but exclude any cleaning, repairs, or replacements internal to the disk assembly.

5.2 RECOMMENDED TEST EQUIPMENT

Table 5-1 lists the test equipment recommended for field servicing of the RS64 Disk File

Table 5-1
Recommended Test Equipment

Equipment	Manufacturer and Model/Part No.
Multimeter	Triplett 310 or Simpson 360
Oscilloscope	Tektronix 453
Oscilloscope Probes	
Voltage	Tektronix P6010
Current	Tektronic P6019 clip-on with passive terminator
Wire Wrap Tool (24-gauge)	DEC H811
Unwrapping Tool (24-gauge)	DEC H812
Wire Wrap Tool (30-gauge)	DEC H811A
Unwrapping Tool (30-gauge)	DEC H812A
Module Extender Board	DEC H982

5.3 PREVENTIVE MAINTENANCE

The following preventive maintenance procedures should be performed every six months or more often if deemed necessary.

CAUTION
Do not *attempt* to clean or replace disk or disk heads. Disk warranty is void if cover is removed by other than authorized personnel. For special equipment and procedures needed for repair of the disk assembly, authorized personnel should refer to Document DEC-SP-DISK-DA. .

Step	Procedure
1	Clean exterior surfaces with a soft cloth.
2	Clean the interior of equipment. Use a small brush to loosen dirt or, if necessary, the brush can be moistened with a commercial solvent. The solvent must be non-flammable, nonconducting, and not injurious to paint, plastic, and electronic components. Fumes from some solvents can be harmful to personnel and therefore should be used only in adequately ventilated areas and according to manufacturer's instructions.
3	Vacuum all loose dirt and other foreign particles from equipment interior.
4	Inspect all wiring and cables for cuts, breaks, kinks, fraying, mechanical security, or other signs of damage or deterioration. Re-wrap or re-solder any loose connections. When replacing wire runs, duplicate wire length and route.
5	Inspect the power supply, modules, and panel assemblies for evidence of damaged components. Replace components that show signs of deterioration.
6	Ensure that all modules and connectors are properly seated.

5.4 CORRECTIVE MAINTENANCE

5.4.1 Module and Pin Designation

Figure 5-1 illustrates the matrix scheme used to locate a module from the wire-wrap pin side of the wired assembly This figure also shows the pin arrangement for a connector block.

5.4.2 Power Control Panel Connector-Pin Identification

Figure 5-2 identifies the connectors and pins for the power control panel.

5.4.3 Power Supply Adjustments

The power supply should be checked when it is repaired or replaced. To adjust the supply outputs for optimum operation, proceed as follows:

Step	Procedure
1	Turn off primary power to power supply by positioning LOCAL/OFF/REMOTE switch to OFF.
2	Fully extend the disk file to gain access to four Phillip screws that attach power supply to the chassis. Remove these screws so that power supply can be positioned for access to adjustment slots. (continued on page 5-3)

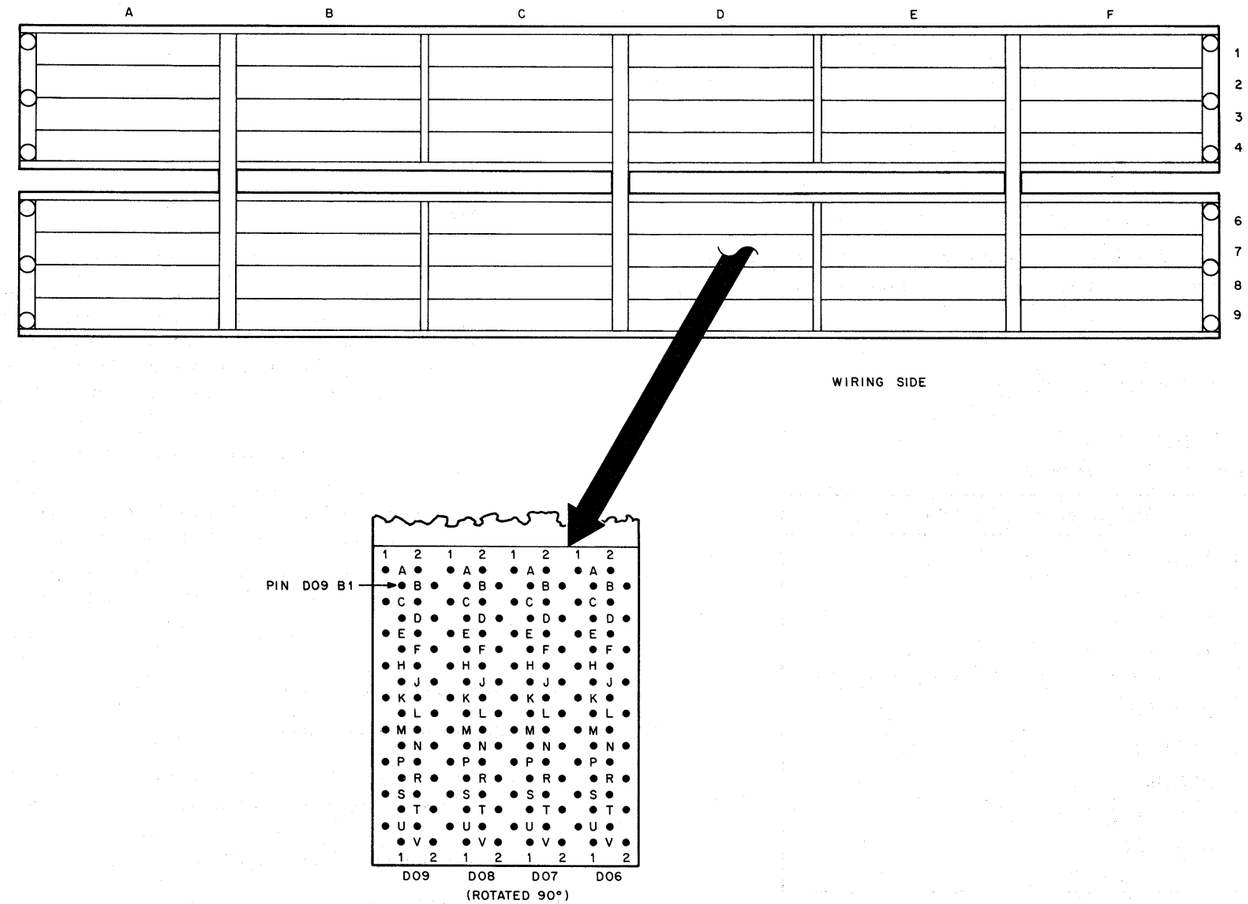


Figure 5-1 Module and Pin Designations

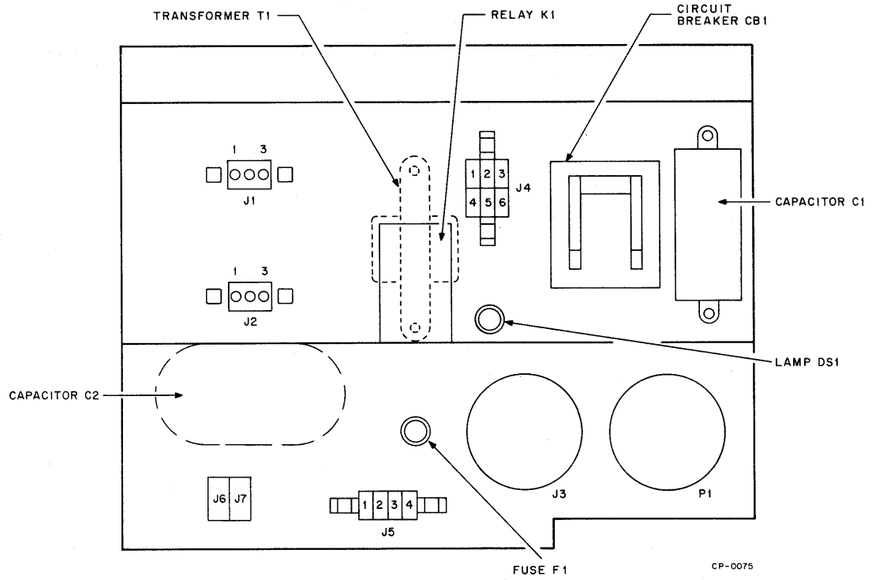


Figure 5-2 Power Control Panel Connector-Pin Identification

Step	Procedure
3	Remove power supply loads by disconnecting output connector, Figure 5-3, on top of supply.
4	Turn on primary power to the supply.
5	With no loads, adjust power supply outputs to values shown below. (Refer to Figure 5-3 for the location of adjustments and access points.)

Output	Connector Pin	Value
+20V	7 or 8	+22V
+5V	1, 2 or 3	+5.15V
-15V	11 or 12	-16V

6	Turn off primary power to the supply and reconnect loads.	
7	Turn on primary power to the supply and recheck power supply outputs under load. Readjust outputs if necessary, as indicated below. If output is below normal value, do not change the adjustment.	

Output	Access Point	Readjustment
+5V	A08-A2	If $+5 \leqslant V \leqslant +5.15$, set to +5V
+20V	A08-S2	If $+20 \leqslant V \leqslant +22$, set to +20V
-15V	A08-R2	If $-15 \geqslant V \geqslant = 16$, set to -15V

8	Turn off primary power. Reposition power supply and install four attaching Phillips screws.

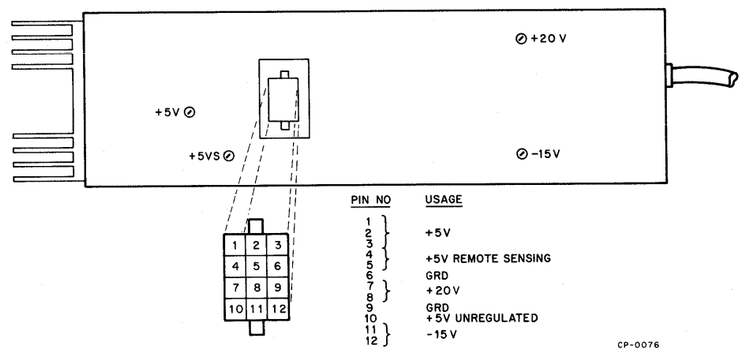


Figure 5-3 Power Supply Adjustment Location and Connector Pin Usage

5.4.4 Read Amplifier-Peak Detector Adjustments

The following adjustments should be performed when:

a. A read amplifier-peak detector is replaced.

b. The disk writer, any track selector modules, or timing or data cables are replaced.

c. The disk is replaced or heads are realigned.

Initially, the read amplifier-peak detectors are statically adjusted for a nominal operating point. Next, each is dynamically adjusted using a controller for bit patterns and for error detection. The dynamic adjustment entails locating a mean point between data peaks and noise peaks. To perform these adjustments:

Step	Procedure
1	Using an oscilloscope or VOM, adjust all four read amplifier-peak detectors for static threshold operating value of -1.2V. Access points for the read amplifier-peak detectors are as follows:

Read Amplifier-Peak Detector	Access Point
Clock	F08-U2
Sector Mark	F07-U2
Address	F06-U2
Data	D07-U2

2	Write a pattern (all 1's, for example) on one complete data track then begin a repetitive read and comparison operation for that track.
3	Connect an oscilloscope or VOM at the clock read amplifier-peak detector test point (F08-U2).
4	While monitoring for errors, slowly adjust clock threshold potentiometer for a more positive indication. When an error occurs, record the threshold indication as V_{High}.
5	Adjust potentiometer for a more negative threshold value and observe where error occurs. Record this value as V_{Low}.

(continued on next page)

Step	Procedure
6	Calculate mean threshold as follows and set potentiometer for that value. $$V_{mpt} = \frac{V_{High} + V_{Low}}{2}$$
7	Using steps 2 through 6, set up threshold for sector mark and address read amplifier-peak detectors. Test points are as follows: Sector Mark – F07-U2 Address – F06-U2
8	For the data read amplifier-peak detector adjustment, write an all-zero pattern in every track. Next, initiate a repetitive read and comparison for track 17_8 (the outermost data track is chosen because it most likely has the greatest amount of noise).
9	Connect the oscilloscope to data read amplifier-peak detector test point (D07-U2). While observing data comparison result, adjust data threshold potentiometer (for a more positive scope indication) until an error occurs. Decrease threshold setting slightly until no errors occur.
10	Read and compare data for all other tracks. If no errors are detected for the other tracks, proceed with Step 11. If errors are detected (signifying tracks with greater amounts of noise than track 17_8), record track numbers containing errors. Readjust data threshold while reading and comparing data from these tracks and locate the noisiest track on disk.
11	Record the threshold voltage (V_{High}) for track 17_8 or the noisiest track on the disk.
12	To define the lowest threshold (V_{Low}), write all ones for every track. Initiate a repetitive read and comparison operation for track 30_8 (the innermost track will probably have lowest amplitude data peaks). Adjust data threshold potentiometer (for a more negative threshold) until error occurs. Decrease threshold setting slightly until no errors occur.
13	Read and compare data from all tracks. If no errors are detected for the other tracks, proceed with Step 14. If errors are detected (signifying tracks having data peaks less than the threshold) record track numbers. Readjust data threshold while reading and comparing data from these tracks. Locate the lowest data peak track and set up threshold for this track.
14	Record the threshold voltage (V_{Low}) for track 30_8 or the track having the lowest data peaks.
15	Calculate the mean threshold as follows and set the potentiometer for that value. $$V_{mpt} = \frac{V_{High} + V_{Low}}{2}$$

5.4.5 Timing Track Changeover

To use the spare timing tracks:

Step	Procedure
1	Turn off dc power to logic by placing LOCAL/OFF/REMOTE switch to OFF.
2	Disconnect timing cable assembly at head shoe 1, rotate head matrix connector 180°, then reconnect cable.
3	Turn on dc power to logic.

NOTE
Readjust read amplifier-peak detector threshold for all timing tracks before attempting further operation.

5.4.6 Rewriting Timing Tracks

Timing tracks should be rewritten whenever the disk surface is replaced or the timing tracks are partially or completely destroyed. To rewrite RS64 timing tracks:

Step	Procedure
1	Remove dc power from RS64 logic by placing the LOCAL/OFF/REMOTE switch on RS64 power control panel to OFF. The ac power to the drive motor should remain on.
2	Disconnect timing cable assembly from module slot E09 and connect it to the timing track writer I/O connector.
3	Disconnect the dc power connector on top of RS64 power supply and connect track writer power cable to power supply.
4	On track writer, select 50 Hz or 60 Hz timing, as applicable, then place all other switches to OFF position.
5	Apply dc power to the track writer by placing the LOCAL/OFF/REMOTE switch to LOCAL.
6	On the track writer, place the WRT ENABLE switch to ON and observe that WRITE VLT indicator lights.
7	Place MAINT switch to ON and observe gap width indicators. If the INCREASE indicator is flashing, turn gap ADJ clockwise until GAP OK indicator flashes. Similarly, turn gap ADJ counterclockwise until GAP OK indicator flashes.
8	Place MAINT switch OFF. To write timing track, depress PUSH-TO-WRITE switch.
9	Turn off WRT ENABLE switch. Remove dc power by placing the LOCAL/OFF/REMOTE switch to OFF.
10	Disconnect track writer power cable at RS64 power supply. Disconnect timing cable assembly at track writer I/O connector and connect it in module slot E09.
11	Connect RS64 logic dc power cable at top power supply, then apply dc power by returning the LOCAL/OFF/REMOTE to the normal operating position.
12	Adjust all timing track read amplifiers (refer to Paragraph 5.4.4 for procedures). Following these adjustments, thoroughly test the operation of the disk.

5.4.7 Troubleshooting Recommendations

5.4.7.1 General – The following remedial action is recommended when a malfunction is detected.

Step	Procedure
1	Investigate all available information concerning the malfunction.
2	Where possible, substitute a known operable disk file to isolate malfunction between the controller and the suspected malfunctioning unit.
3	If an error occurs for a group of addresses, always check the write lockout switches to ensure that the group is not included in write lockout function.
4	In general, diagnostic error printouts classify errors in four primary categories. These error categories and the recommended isolation approach are described in subsequent paragraphs.

5.4.7.2 Track Address Errors – Track address errors can be of two primary types, i.e., those involving a group of tracks or individual tracks.

Step	Procedure
1	For errors associated with octal groups 0–7, 10–17, 20–27, and 30–37, initiate a repetitive write operation for the malfunctioning group. Check the series switch output associated with that group for a write transition. Refer to D-BS-RS64-0-4 for access points and track group circuits.
2	For errors associated with octal groups 0, 10, 20, and 30 or 1, 11, 21, or 31, etc., initiate a repetitive write operation for the malfunctioning group. Check the center top module associated with the grouping. Refer to D-BS-RS64-0-4 for access points.
3	For individual track errors, initiate a repetitive write operation and check the M163 decoder output for the selected track for a negative-true (0V) pulse. Also check cable connections and wiring for the track. Refer to D-BS-RS64-0-4 for access points, levels, and wiring connections.

5.4.7.3 Sector Address Errors – To check and further isolate sector address errors:

Step	Procedure
1	Check address marks and address strobes at digital interface. Refer to Figure 5-4 for oscilloscope set up and waveforms. This figure depicts the last address (77_8) of track. Beginning at address 0 or 77_8, verify the remaining addresses are present by changing the delay interval.
2	If address marks or strobes are not present, check for at least a 6V p-p analog signal at TTB or TTC read amplifier peak-detector. Figure 5-5 shows the address strobes and analog waveform for address 75_8. If analog signal is good, readjust related read amplifier-peak detector (Paragraph 5.4.4).
3	If the analog signal is abnormal, substitute the read amplifier-peak detector. If the analog signal is still abnormal, reverse the timing cable to use spare tracks (Paragraph 5.4.5) or rewrite timing tracks (Paragraph 5.4.6).
4	If malfunction is isolated to the disk or disk heads, only authorized personnel should attempt repair.

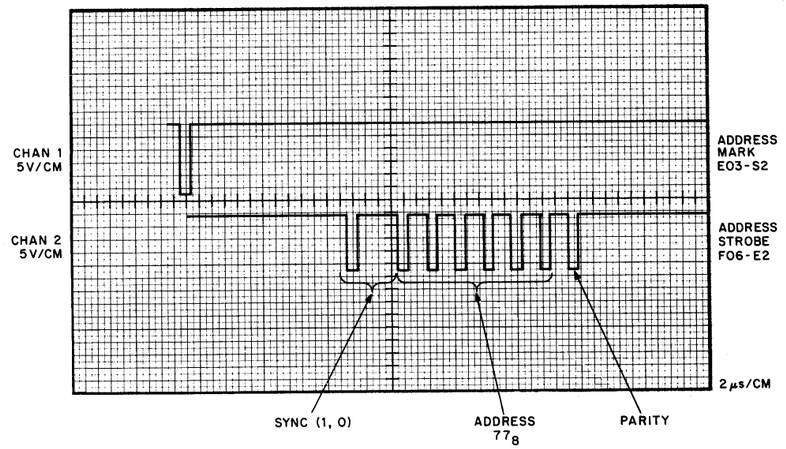


Figure 5-4 Address Mark and Address Strobe

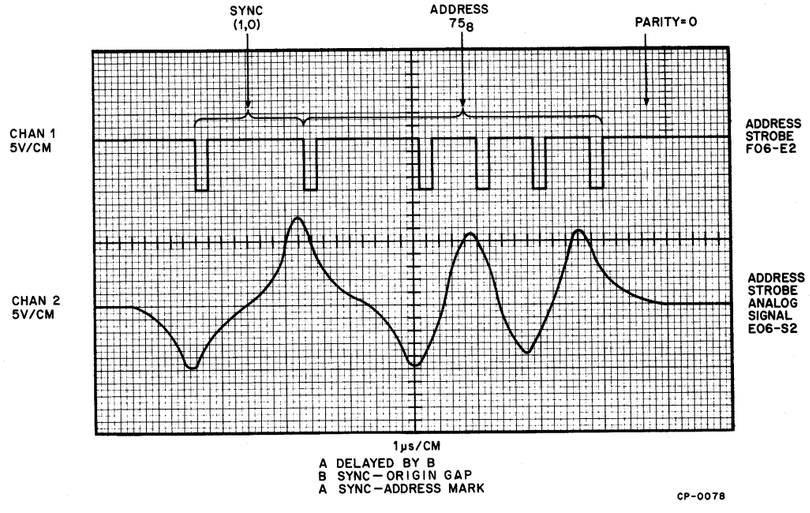


Figure 5-5 Address Strobe and Analog Signal

5.4.7.4 Timing Errors – To check and isolate clock timing errors:

Step	Procedure
1	Check the relationship of CLK S and PLC. Figure 5-6 shows the relationship of these signals plus access points and oscilloscope setup. The negative transitions of each clock strobe should occur within 100 ns of a negative transition in the phase-locked clock. (continued on next page)

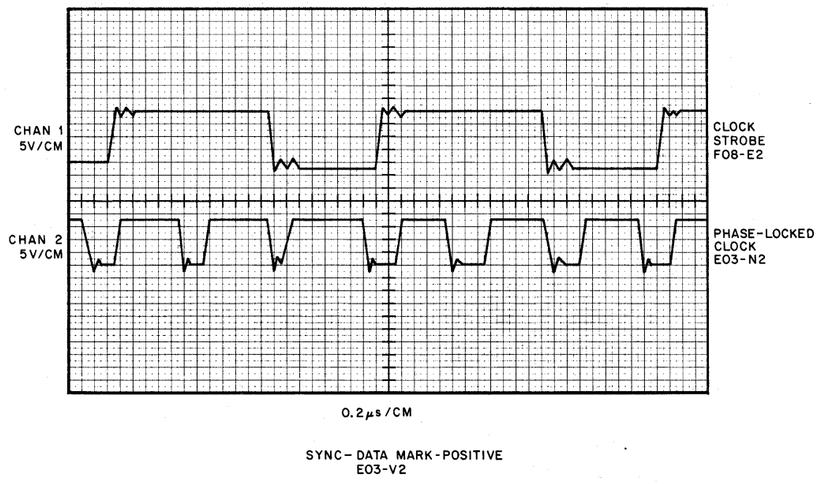


Figure 5-6 Clock Timing Signals

Step	Procedure
2	If the phase-locked output is abnormal, check the M4201 Clock (module slot CD1) and the divide-by-3 counter (module slot D02).
3	If the CLK S is abnormal, check its associated read-amplifier-peak detector. This check can be made in the same general manner as described for sector address (Paragraph 5.4.4).
4	If the malfunction is isolated to the disk, reverse timing cable to use spare tracks (Paragraph 5.4.5). If this action does not correct the problem, rewrite the timing tracks (Paragraph 5.4.6).
5	If malfunction is isolated to disk or disk heads and cannot be corrected by rewriting timing tracks, only authorized personnel should attempt repair.

5.4.7.5 Data Errors – Data errors are generally classified as hard (equipment failure) or random (occurring without any recognizable pattern). Random errors are generally caused by marginal supply voltages, marginal timing, marginal disk writer current, or misadjustment of the data read amplifier-peak detector. A general approach to isolating data errors is as follows:

Step	Procedure
1	Check the write lockout switches to ensure that data error is not caused by write lockout function.
2	Check +5V, -15V, and +20V potentials. Refer to Paragraph 5.4.3 for operating limits and adjustment procedures.
3	Check clock timing. Refer to Paragraph 5.4.7.4 for timing error checks.
4	Continuously write an alternating one-zero pattern or another readily recognizable pattern and check the disk write circuits. Figure 5-7 depicts the relationship of write (WRT) Data and the disk writer output.

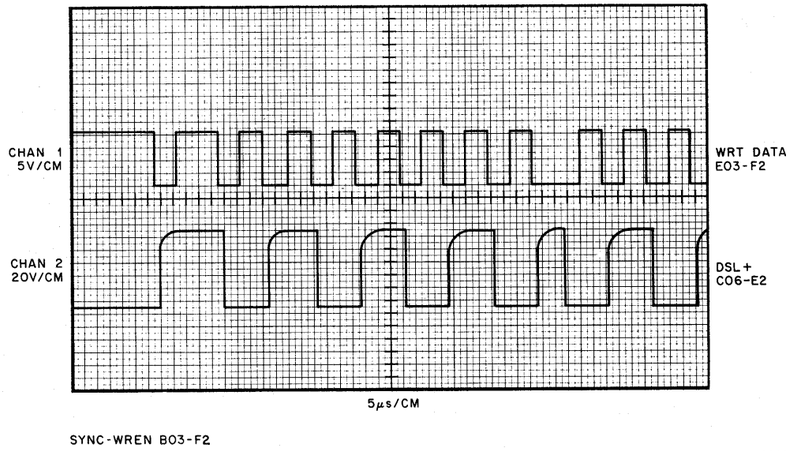


Figure 5-7 WRT Data and DSL Relationships

Step	Procedure
5	If the disk writer output is normal, check the data read amplifier-peak detector strobe and analog signals and adjust peak detector threshold if necessary. (Refer to Paragraph 5.4.7.3 for typical read amplifier-peak detector checks.)
6	If malfunction is isolated to the disk assembly, only authorized personnel should attempt repair.

5.5 REMOVAL AND REPLACEMENT

5.5.1 Removal of Disk Assembly

CAUTION

Do not attempt removal of disk assembly without motor lock installed.

Step	Procedure
1	Remove primary power and disconnect drive motor cable at power control panel.
2	Disconnect four data head matrix connectors and timing head connector at disk base.
3	Install motor lock on base of motor shaft.
4	Disconnect ground strap. Retain hardware.
5	Using a 5/32 Hexagon wrench, remove four bolts that attach deck plate to shock absorber mounts. Retain bolts and nuts for reassembly.
6	Disk assembly is now ready for removal.

CAUTION

Exercise care in handling disk assembly. Do not drop or subject disk assembly to heavy impact because heads can be damaged or misaligned.

5.5.2 Reinstallation of Disk Assembly

Step	Procedure
1	If power supply, power control panel, and disk select/WLO panel have not been removed, remove these items to gain working access.
2	Position disk assembly over shock mounts and attach shock mounts to base plate.
3	Connect head matrix connector for head shoe 2 first, then continue in a counter clockwise direction with balance of head matrix connectors. The shorter cable from module slot B09 mates with the head shoe 2 connector. Similarly, the shorter cable from module slot C09 mates with the head shoe 3 connector. Refer to Drawing D-BS-RS64-0-6 for the location of head shoes.
4	Reconnect ground strap.
5	Remove motor lock on base of motor shaft.
6	Install power supply, power control panel, and disk select/WLO panel.
7	Reconnect disk drive motor, power supply and disk select/WLO panel. Connect fan and any remote control lines.

5.6 RECOMMENDED SPARE PARTS

Table 5-2 lists the spare parts recommended for the RS64 Disk File.

Table 5-2
Recommended Spare Parts

DEC Type/Part No.	Figure	Description	Quantity
1210167-0	5-2	Breaker, Circuit (APL-11-1-6-0-502 Air Pax)	1
7007049-0-0	1-2	Cable Assembly, Data	1
7006111-01	–	Cable, I/O	1
7007238-0-0	–	Cable Assembly, Power	1
7007050-0-0	1-2	Cable Assembly, Timing	1
1002153	5-2	Capacitor; 2X 0.1 mfd, 600 Vdc	1
1005767	5-2	Capacitor, GE #72F6211, 10 mfd, 330V, 60 Hz	1
1209378	–	Contact, Male, Mate-N-Lock	6
7408624-0-0	–	Cover, Module	1
1205033-01	1-3	Fan	1
9009039	5-2	Fuse, 2/10 Amp, Slo-Blow	5
9007242	–	Holder, Fuse, HKP	1
1209351-12	–	Housing, Pin, 1-480278-0	1
1201280	5-2	Lamp, Pilot 1020C55, 125V	1
M623	D-MU-RS64-0-8	Module, Bus Driver	1
G296	↓	Module, Center Tap Selector	1
M205	↓	Module D-Type Flip-Flop	1
G291	D-MU-RS64-0-8	Module, Disk Writer	1
M163	↓	Module, Dual Binary-to-Decimal Decoder	1
M111	↓	Module, Inverter	1
G8001	↓	Module, Low-Voltage Detector	1
M167	↓	Module, Magnitude Comparator	1
M4201	↓	Module, Phase-Locked Clock	1
G739	↓	Module, Peripheral Terminator	1
G088	↓	Module, Read Amplifier-Peak Detector	1
G295	↓	Module, Series Switch	1
G738	↓	Module, Terminator	1
M113	↓	Module, 2-Input NAND Gate	1
H737 or H736	1-3	Power Supply	1
None	5-2	Relay, (#KRP-11DE Potter and Brumfield)	1
1302407	–	Resistor, 47K, 1/2W	1*
5409182	5-2	Switch Assembly, Remote/Local	1
1102915	–	Thyrector, 115V	1*
1100106	–	Thyrector, 230V	1*
161050-0	5-2	Transformer	1
1605147	–	Tube, Ferrite	1

*As Applicable.

CHAPTER 6
DRAWINGS

Table 6-1 lists the mechanical and electrical drawings supplied with this manual. A set of engineering drawings is also supplied with each disk file. If drawing differences are observed, the drawings supplied with the equipment take precedence. Table 6-2 defines the signal mnemonics used on the block schematics.

Table 6-1
Drawings

Drawing Number	Title	Page
D-SD-RS64-0-11	Maximum Configuration	6-3
C-DB-RS64-0-9	Signal Bus Configuration	6-4
C-BD-RS64-0-10	Power Cable Configuration	6-5
D-MU-RS64-0-8	Module Utilization	6-6
D-BS-RS64-0-2	Timing Path	6-7
D-BS-RS64-0-3	Data Path	6-8
D-BS-RS64-0-4	Track Selection	6-9
D-BS-RS64-0-5	I/O Connectors	6-10
D-BS-RS64-0-6	Head Matrices	6-11
D-AD-7006858-0-0	Control Panel	6-12
D-CS-G088-0-1	G088 Read Amplifier-Peak Detector Schematic	6-16
CP-0048	G088 Read Amplifier-Peak Detector Component Location	6-17
C-CS-G291-0-1	G291 Disk Writer Schematic	6-18
CP-0052	G291 Disk Writer Component Location	6-18
B-CS-G295-0-1	G295 Series Switch Schematic	6-19
CP-0047	G295 Series Switch Component Location	6-19
B-CS-G296-0-1	G296 Center Tap Selector Schematic	6-20
CP-0046	G296 Center Tap Selector Component Location	6-20
B-CS-G738-0-1	G738 Terminator Schematic	6-21
CP-0109	G738 Terminator Component Location	6-21
B-CS-G739-0-1	G739 Peripheral Terminator Schematic	6-22
CP-0045	G739 Peripheral Terminator Component Location	6-22

Table 6-1 (Cont)
Drawings

Drawing Number	Title	Page
B-CS-G8001-0-1	G8001 Low Voltage Detector Schematic	6-23
CP-0041	G8001 Low Voltage Detector Component Location	6-23
B-CS-M111-0-1	M111 Inverter Schematic	6-24
CP-0039	M111 Inverter Component Location	6-24
B-CS-M113-0-1	M113 2-Input NAND Gate Schematic	6-25
CP-0042	M113 2-Input NAND Gate Component Location	6-25
B-CS-M163-0-1	M163 Dual Binary-to-Decimal Decoder Schematic	6-26
CP-0044	M163 Dual Binary-to-Decimal Decoder Component Location	6-26
D-CS-M167-0-1	M167 Magnitude Comparator Schematic	6-28
CP-0037	M167 Magnitude Comparator Component Location	6-29
B-CS-M205-0-1	M205 D-Type Flip-Flop Schematic	6-30
CP-0053	M205 D-Type Flip-Flop Component Location	6-30
C-CS-623-0-1	M623 Bus Driver Schematic	6-31
CP-0059	M623 Bus Driver Component Location	6-31
B-CS-M901-0-1	M901 Flexprint Cable Connector Schematic	6-32
CP-0040	M901 Flexprint Cable Connector Component Location	6-32
B-CS-M908-0-1	M908 Ribbon Connector Schematic	6-33
CP-0043	M908 Ribbon Connector Component Location	6-33
D-CS-M4201-0-1	M4201 Phase-Locked Clock Schematic	6-34
CP-0038	M4201 Phase-Locked Clock Component Location	6-35
B-CS-5408998-0-1	RS64 Disk Select	6-36
CP-0051	Write Lockout Panel Component Location	6-37
B-CS-5408996-0-1	8-Track Matrix 5408996 Schematic	6-38
CP-0049	8-Track Matrix 5408996 Component Location	6-38
B-CS-5408937-0-1	Timing Head Matrix 5408937 Schematic	6-39
CP-0050	Timing Head Matrix 5408937 Component Location	6-39
CP-0110*	Power Supply Circuit Schematic (sheet 1 of 2)	6-40
CP-0111*	Power Supply Circuit Schematic (sheet 2 of 2)	6-41

This power supply schematic is the property of Deltron Inc. The layout of the schematic has been modified by DEC for use in the RS64 Maintenance Manual.

Table 6-2
Signal Glossary

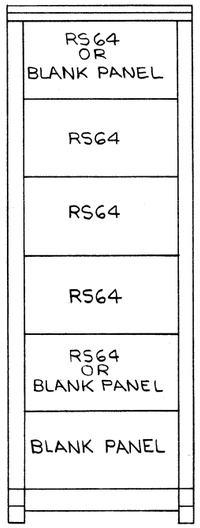
Mnemonic	RS64 Source Drawing	Meaning
AC LO	-0-3	*AC Low*; level change denoting an imminent loss of dc power for disk and controller.
ADR P	-0-2	*ADdRess Polarity*; polarity pulse from the address track read amplifier-peak detector.
ADR S	-0-2	*ADdRess Strobe*; strobe pulse from the address track read amplifier-peak detector.
CLK P	-0-2	*CLocK Polarity*; polarity pulse from the clock track read amplifier-peak detector.
CLK S	-0-2	*CLocK Strobe*; strobe pulse from the clock track read amplifier-peak detector.
DSK 0 – DSK 3 SEL	-0-5	*DiSK SELect*; discrete selection levels for selecting disk files 0 through 3.
DSL (+)	-0-3, -0-4	*Data Sense Line* (positive); positive data line for selected read/write head.
DSL (-)	-0-3, -0-4	*Data Sense Line* (negative); positive data line for selected read/write head.
F/3	-0-2	Phase-Lock Clock *Frequency* divided by three.
LOCK DIS	-0-3	Write *LOCK DISable*; disable line for write lockout function.
M CLR	-0-5	*Master CLeaR*; initializing signal for write electronics.
PLC	-0-2	*Phase Lock Clock*; output of phase-locked clock (3 times bit rate).

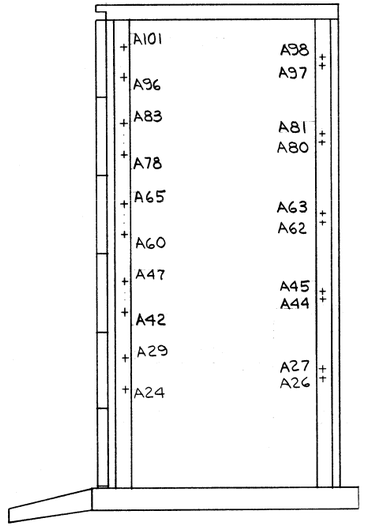
Table 6-2 (Cont)
Signal Glossary

Mnemonic	RS64 Source Drawing	Meaning
READ DATA P	-0-3	*READ DATA Polarity*; polarity pulse from data read amplifier-peak detector.
READ DATA S	-0-3	*READ DATA Strobe*; strobe pulse from data read amplifier-peak detector.
SEL	-0-3	*SELect*; output level of drive select switch denoting selection this drive.
SEL ACK	-0-3	*SELect ACKnowledge*; acknowledge signal for selected drive.
SW 0 – SW 4	-0-3	Write Lockout *SWitch*; SW 0 corresponds to LSB (2^0) of track address selected for write lockout; SW 4 corresponds MSB (2^4).
TK 2^0 – TK 2^4	-0-5	*TracK* Address Bits defining one of 32 tracks.
TK 0 – TK 7	-0-4	*TracK* 0–7; center tap lines for octal groups X0 through X7 of data head matrix.
TRK 0–7, 10–17, 20–27, 30–37	-0-4	*TRacK*; series switch selection lines for data head matrix groups 0_8 through 7_8, 10_8 through 17_8, 20_8 through 27_8, and 30_8 through 37_8.
WLO	-0-3	*Write LockOut*; control level that denotes a write lockout condition is established for the selected track.
WREN	-0-5	*WRite ENable*; control level that enables the writing of data.
WRT DATA	-0-5	*WRiTe DATA*; serial NRZ data input to be written on selected track.

NOTES:

1. CABINET - H95Ø-A (DWG E-UA-H95Ø-A-Ø)
   END PANEL - H952-A (DWG D-UA-H952-A-Ø)
   REAR DOOR - H95Ø-D (DWG D-UA-H95Ø-D-Ø)
   FRONT DOOR - H95Ø-H (DWG D-UA-H95Ø-H-Ø)
   BLANK PANEL - H95Ø-Q (DWG D-UA-H95Ø-Q-Ø)
   STABILIZER FOOT - H952-B (DWG D-UA-H952-B-Ø)
   PANEL FASTENERS - H952-D (DWG D-UA-H952-D-Ø)
   CASTER SET - H952-E-Ø (DWG D-UA-H952-E-Ø)
   LEVELER SET - H952-F-Ø (DWG D-UA-H952-F-Ø)





QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION / MODEL: RS64

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. B. Milan	DATE 3-10-71	
CHK'D. B. Milan	DATE 3-11-71	
ENG. D. Brenden	DATE 11 MAR 71	
PROJ. ENG.	DATE 3-17-71	
PROD.	DATE 3-17-71	

NEXT HIGHER ASSY: A-ML-RS64-Ø-Ø

SCALE

SHEET 1 OF 1

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MAXIMUM CONFIGURATION

SIZE	CODE	NUMBER	REV.
D	SD	RS64-0-11	

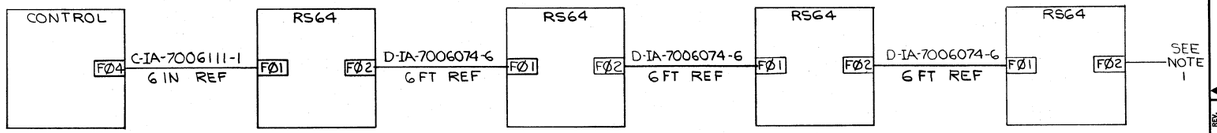
DIST.

REVISIONS	REV.	CHANGE NO.	CHK.

DEC FORM NO. DRD 100

SIZE D CODE SD NUMBER RS64-0-11 REV.

NOTES
1. PERIPHERAL TERMINATOR G739 IS PLACED IN LOCATION FØ2 OF THE LAST RS64 ON THE BUS.
2. MAX BUS LENGTH = 35 FEET
3. REF CABLE LENGTHS ENABLE FULL SLIDE EXTENSION FOR SERVICING



FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RS64		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINISH SURFACE QUALITY ✓
REMOVE BURRS AND BREAK SHARP CORNERS

DRN. P. Miles	DATE 1-13-71	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P. Miles	DATE 1-19-71	
ENG.	DATE 2-5-71	
PROJ. ENG.	DATE 2-5-71	
PROD.	DATE 2-8-71	

MATERIAL —
FINISH —
NEXT HIGHER ASSY A-ML-RS64-Ø-Ø
SCALE —
SHEET 1 OF 1

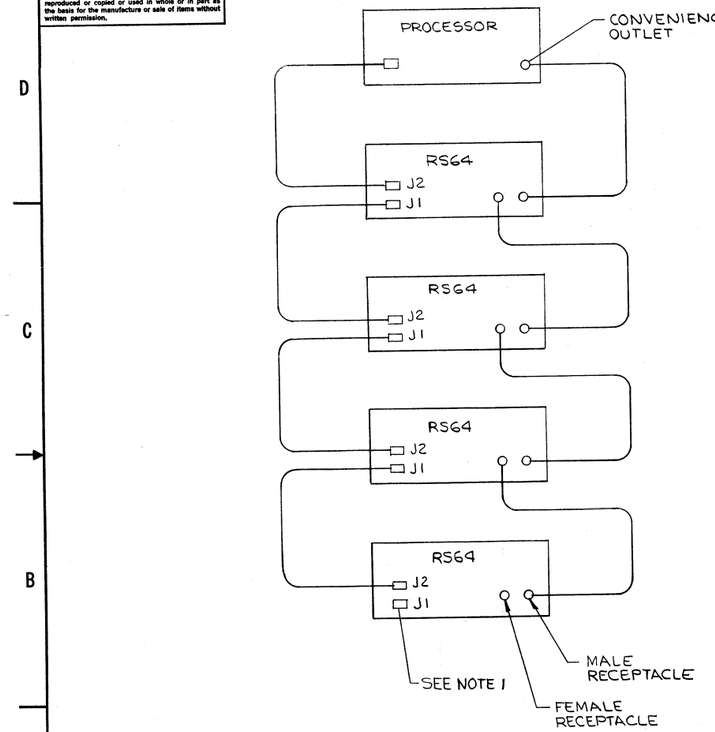
TITLE: SIGNAL BUS CONFIGURATION

SIZE	CODE	NUMBER	REV.
C	BD	RS64-Ø-9	

DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO. DRC 100



NOTES:

1. LAST UNIT ON REMOTE POWER CONTROL BUS HAS TERMINATOR ON J1 WHICH JUMPER PIN 1 TO PIN 2

REVISIONS	REV.
CHANGE NO.	
CHK.	

DEC FORM NO. DRC 100

FIRST USED ON OPTION/MODEL: RS64

UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DRN. P. Milan	DATE 1-9-70	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P. Milan	DATE 1-19-70	
ENG.	DATE 2-7-71	
PROJ. ENG.	DATE 2-7-71	TITLE: POWER CABLE CONFIGURATION
PROD.	DATE 2-7-71	

NEXT HIGHER ASSY: A-ML-RS64-Ø-Ø

SCALE

SHEET 1 OF 1

SIZE	CODE	NUMBER	REV.
C	BD	RS64-Ø-1Ø	

DIST.

NOTES
1. IF MULTIPLE DRIVES ARE INTERCONNECTED ON THE CONTROL BUS, THE BUS CONNECTOR TO FURTHER DRIVES IS IN THIS LOCATION. THE TERMINATOR IS PLACED IN THIS LOCATION IN THE LAST DRIVE OF THE CHAIN.

	1	2	3	4	5	6	7	8	9
A			M111		CASTING SPACE		G296 CENTER TAP SELECT	G772 POWER CONNECTOR G295 SERIES SWITCH	M901 DATA CONNECTOR
B									
C	M4201 PHASE LOCK CLOCK	G8001 LOW VOLTAGE DETECTOR	M163 TRACK DECODER			G291 WRITE AMP	G888 DATA READ AMP	G295 SERIES SWITCH	M901 DATA CONNECTOR
D		M205							G296 CENTER TAP SELECT
E	M901 WLO CONNECTOR	M167 MAGNITUDE COMPACATOR	M113			G888 SECTOR ADDRESS READ AMP	G888 SECTOR MARK READ AMP	G888 CLOCK READ AMP	M908 TIMING CONNECTOR
F	M901 CONTROL BUS CONNECTOR	G739 BUS TERMINATOR OR CONTROL BUS CONNECTOR (SEE NOTE 1)	M623 BUS DRIVERS						

QTY.	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			

REVISIONS	REV.	CHANGE NO.	CHK.

FIRST USED ON OPTION/MODEL: RS64

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

DRN. P. Miller	DATE 12-17-70	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P. Miller	DATE 12-22-70	
ENG.	DATE 2-3-71	
PROJ. ENG.	DATE 2-3-71	
PROD.	DATE 12-21-71	
NEXT HIGHER ASSY A-ML-RS64-Ø		
SCALE NONE		
SHEET 1 OF 1		

TITLE: MODULE UTILIZATION

SIZE D | CODE MU | NUMBER RS64-Ø-8 | REV.

DIST.

DEC FORM NO. DRD 100

SIZE D | CODE MU | NUMBER RS64-0-8 | REV.

M908 E09

D2 E2 F2 H2 J2 K2 L2 M2 N2

G088 E08 — G088 F08 — TEST PT. U2
G088 E07 — G088 F07 — TEST PT. U2
G088 E06 — G088 F06 — TEST PT. U2

+3V — M113 F03 (E1, D1) — F1
M113 B03 (J1, K1)
M113 B03 (H2, J2)
M113 E03 (R2, P2) — S2
M113 E03 (T2, U2) — V2
M113 F03 (M2, L2) — N2

M4201 CD01 (DE2, D H2, CY2, DK2, CU2)

M205 D02 (F2, H2, J2, K2, E2, D2)
M205 D02 (C1, D1, E1, F1, B1, A1)
+3V
F/3 H

M623 F03 (R2, T2) — U2 — CLKS L
M623 F03 (S2) — V2 — CLKP L
M623 F03 (M1, P1) — R1 — PLC
M623 F03 (C1, B1) — E1 — ADDRESS MARK L
M623 F03 (A1) — D1 — DATA MARK L
M623 F03 (F1, J1) — K1 — ADRS L
M623 F03 (H1) — L1 — ADRP L

SEL L

REVISIONS			
CHK	CHANGE NO.	REV.	
[illegible]	RS64-0000X	A	
[illegible]	McLEAN	5-14-71	

FIRST USED ON OPTION/MODEL: RS64	QTY.	DESCRIPTION	PART NO. / ITEM NO.
		PARTS LIST	
UNLESS OTHERWISE SPECIFIED	DRN. S. HILL	DATE 12-21-70	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	CHK'D. R. McLean	DATE 12-22-70	TITLE: TIMING PATH
	ENG. [illegible]	DATE 2-8-71	
	PROJ. ENG. [illegible]	DATE 2-3-71	
MATERIAL	PROD. W. Allen	DATE 2/3/71	
	NEXT HIGHER ASSY A-ML-RS64-0-0		SIZE D | CODE BS | NUMBER RS64-0-2 | REV. A
FINISH	SCALE		
	SHEET OF		DIST.

DEC FORM NO. DRD 102A

WREN L — M111 B03 S1 — M113 E03 A1 B1 C1 — M111 B03 E2 F2

WFF(0)H — M113 E03 L1 M1 N1 — M111 B03 L1 M1

WFF(1)H — M113 E03 J1 H1 K1

WRT DATA H — M113 E03 D2 E2 F2

M113 E03 J2 H2 K2

+3V — WFF M2Ø5 DØ2 L1 M1 N1 K1 J1 H1 C Ø D I

MCLR L

U2 V2 S2 T2 R2 P2

G291 CØ6 E2 F2

DSL + / DSL - — G088 CØ7 E2 F2 T2 S2

G8ØØ1 CØ2 E2 H2 — UNREG 5V — ACLO L

G088 DØ7 U2 E2 H2

MG23 FØ3 K2 M2 N2 — READ DATA S L

MG23 FØ3 L2 P2 — READ DATA P L

MG23 FØ3 P1 N1 S1 — WLO L

M2Ø5 DØ2 U1 +3V

M113 EØ3 U1 +3V

M113 EØ3 V1 +3V

M301 EØ1 C2 A2 D2 E2 F2 H2 J2 K2

S1 S2 S3 S4 S5 S6 S7 OFF Ø 1 2 3

WLO-DSK SEL 5408998

LOCK DIS H

SW Ø L SW 1 L SW 2 L SW 3 L SW 4 L

M167 EØ2 H1 S1 E2 D2 B1 K1 J1 C1 F1 F2 A1 M2 M1 D1 E1 H2 U2 P1 R1 V1 U1 L1

TK 2^0 H TK 2^1 H TK 2^2 H TK 2^3 H TK 2^4 H

DSK Ø SEL L L2 — DSK 1 SEL L M2 — DSK 2 SEL L N2 — DSK 3 SEL L P2 — S2

MG23 FØ3 D2 F2 H2 — SEL ACK L

M113 EØ3 P1 R1 S1

M111 BØ3 N1 P1 — SEL L

REVISIONS			
	CHANGE NO.		REV.
CHK	RS64-00002		A
Mclean	5-4-71		
Engineering	5-6-71		

FIRST USED ON OPTION/MODEL	RS64		
UNLESS OTHERWISE SPECIFIED	DRN. P Milan	DATE 12-18-70	
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS .005 ± 1/64 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	CHK'D. P. Milan	DATE 12-22-70	
	ENG.	DATE 2-2-71	
	PROJ. ENG.	DATE 2-2-71	
MATERIAL	PROD.	DATE 2-3-71	
FINISH	NEXT HIGHER ASSY A-ML-RS64-Ø-Ø		
	SCALE		
	SHEET 1 OF 1		

PARTS LIST

QTY.	DESCRIPTION	PART NO.	ITEM NO.

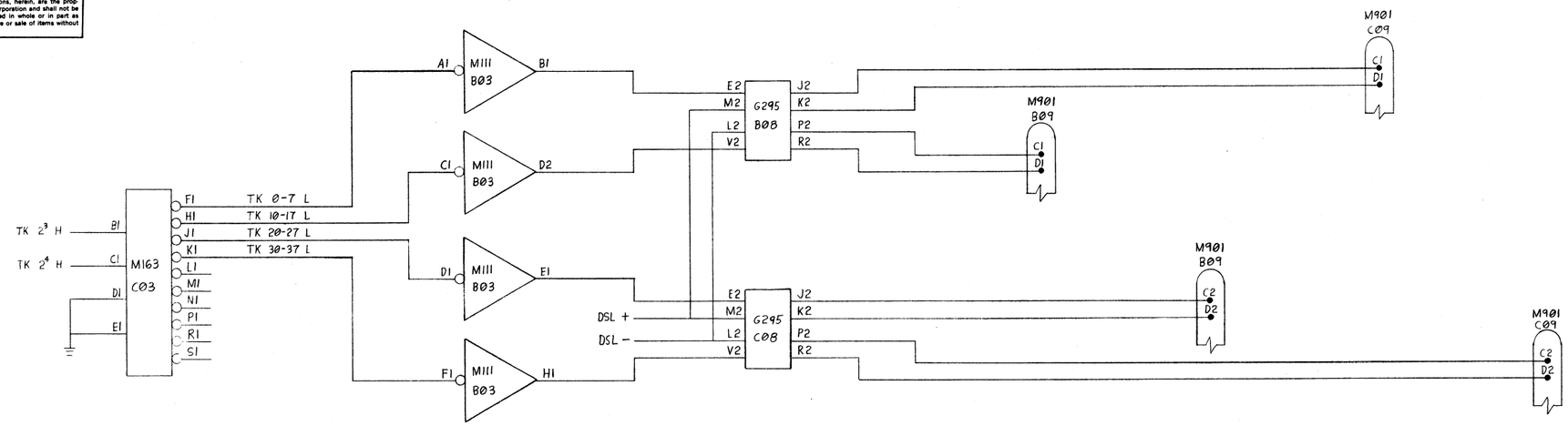
digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

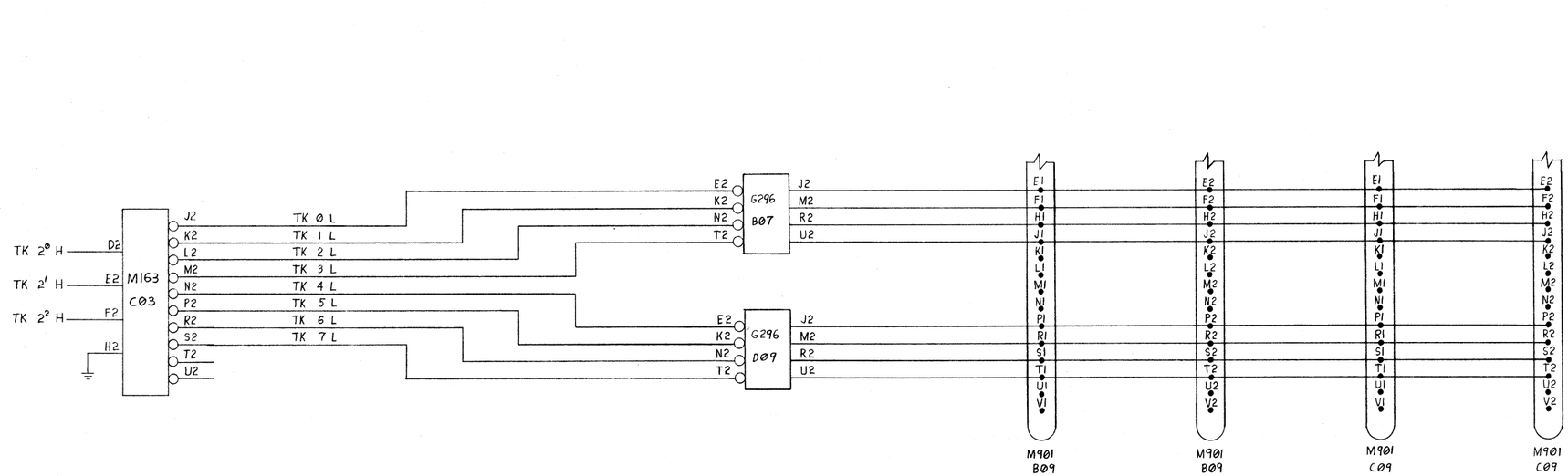
TITLE: DATA PATH

SIZE	CODE	NUMBER	REV.
D	BS	RS64-Ø-3	A

DIST.

DEC FORM NO. DRD 102A





FIRST USED ON OPTION/MODEL: RS64	QTY.	DESCRIPTION (PARTS LIST)	PART NO. / ITEM NO.
UNLESS OTHERWISE SPECIFIED: DIMENSION IN INCHES; TOLERANCES: DECIMALS ± .005, FRACTIONS ± 1/64, ANGLES ± 0°30'; FINAL SURFACE QUALITY √; REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL: —			
FINISH: —			
DRN. S. HILL — DATE 12-21-70			
CHK'D. P. Mulvey — DATE 12-22-70			
ENG. — DATE 2-2-71			
PROJ. ENG. — DATE 2-3-71			
PROD. — DATE 2/3/71			
NEXT HIGHER ASSY: A-ML-RS64-0-0			
SCALE: —			
SHEET: OF			

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: TRACK SELECTORS

SIZE D | CODE BS | NUMBER RS64-0-4 | REV.

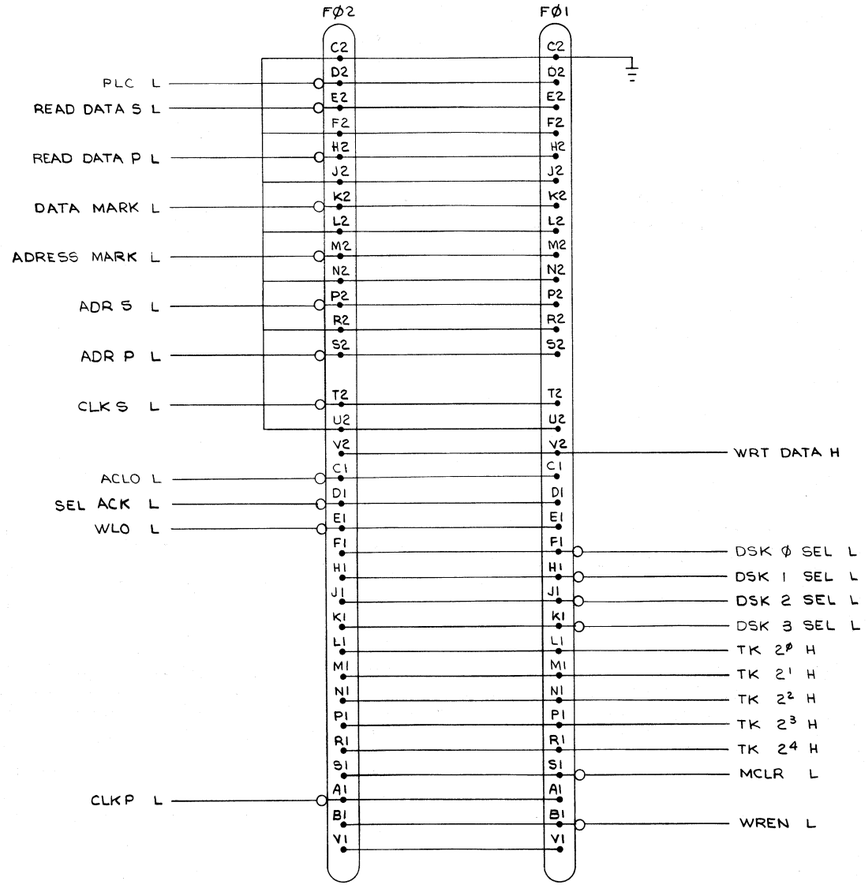
DIST.

REVISIONS: REV. | CHANGE NO. | CHK

DEC FORM NO. DRD 102A

SIGNALS DRIVEN

SIGNALS RECEIVED



REVISIONS	CHK	CHANGE NO	REV
	MCLEAN	RS64-00001	A

FIRST USED ON OPTION/MOD	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RS64		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30'
FINAL SURFACE QUALITY √
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN. P Mclean	DATE 12-18-70	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P Mclean	DATE 12-22-70	
ENG.	DATE 2-3-71	
PROJ. ENG.	DATE 2-3-71	
PROD.	DATE 3/8/71	

NEXT HIGHER ASSY A-ML-RS64-Ø-Ø

SCALE —

SHEET 1 OF 1

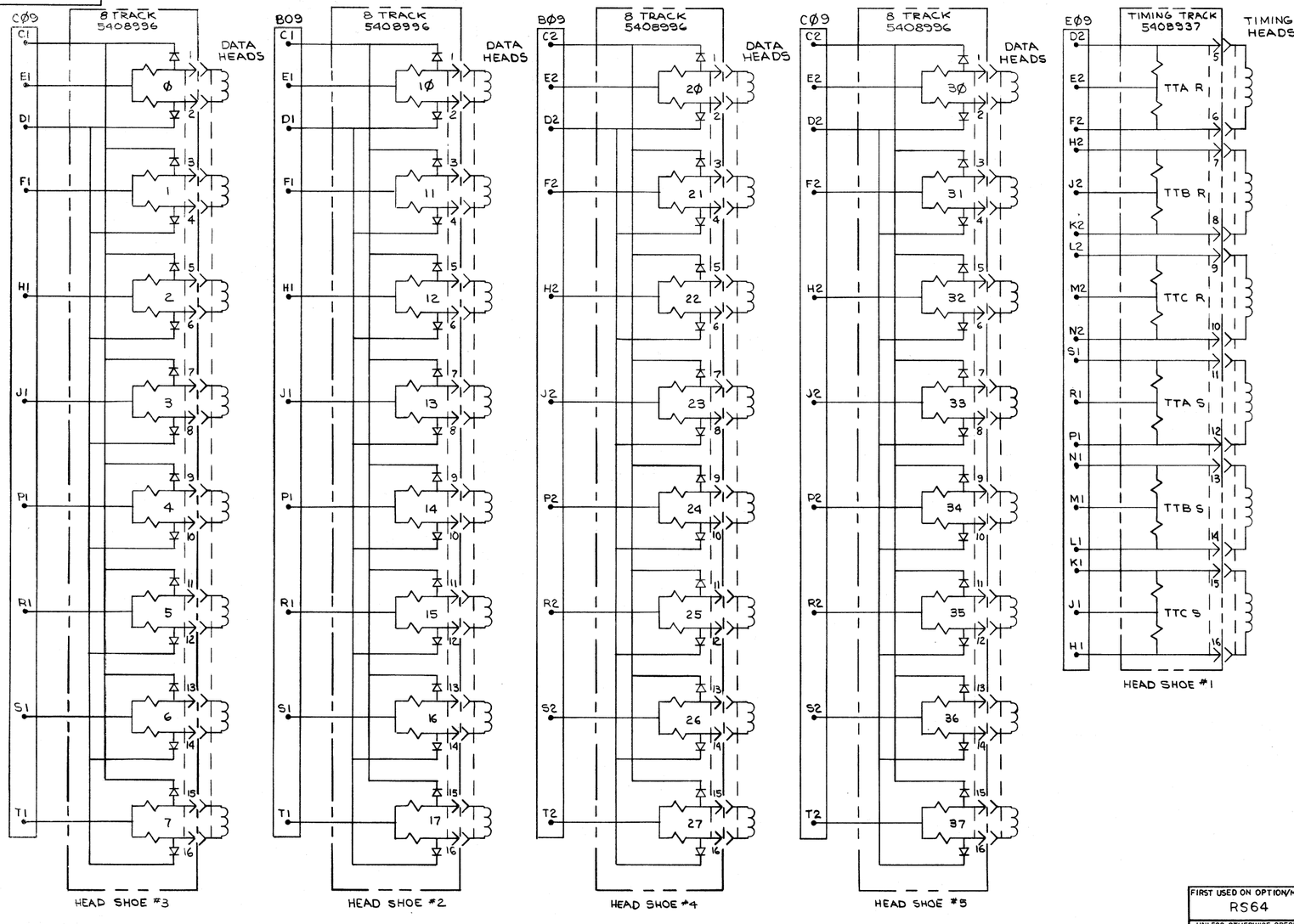
TITLE I/O CONNECTORS

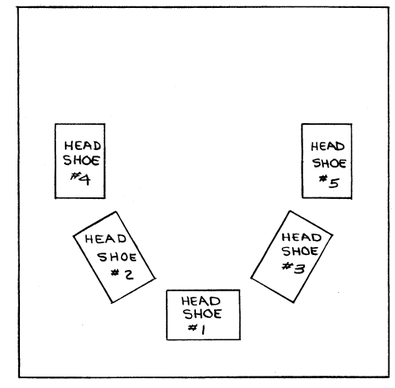
SIZE	CODE	NUMBER	REV
D	BS	RS64-0-5	A

DIST.

DEC FORM NO. DRD 102A

NOTES:
1. ALL RESISTOR 750 Ω, ±1%
   ALL DIODES D672





TOP VIEW

REVISIONS	REV	CHANGE NO.	CHK

FIRST USED ON OPTION/MODEL	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RS64		PARTS LIST		

UNLESS OTHERWISE SPECIFIED
UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINISH SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL —

FINISH —

DRN. P. Milan	DATE	12-16-70
CHK'D. P. Milan	DATE	12-22-70
ENG.	DATE	2-3-71
PROJ. ENG.	DATE	2-3-71
PROD.	DATE	2/24/71

digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

TITLE: HEAD MATRICES

NEXT HIGHER ASSY: A-ML-RS64-0-0

SIZE D | CODE BS | NUMBER RS64-0-6 | REV.

SCALE NONE

SHEET OF

DIST.

DEC FORM NO. DRD 102A

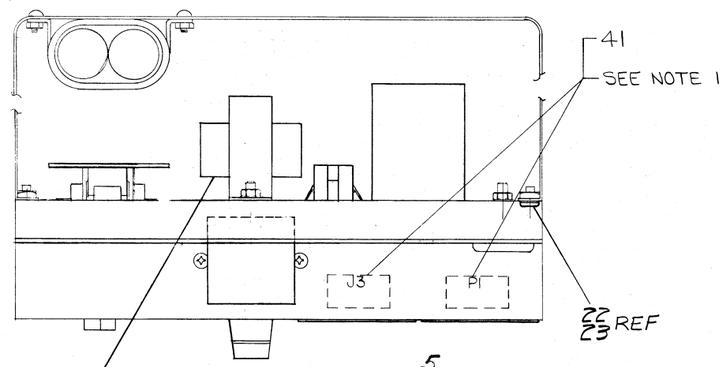
LEGEND	
NUMBER	VARIATION
7006858-1	115 VAC.
7006858-2	230 VAC.

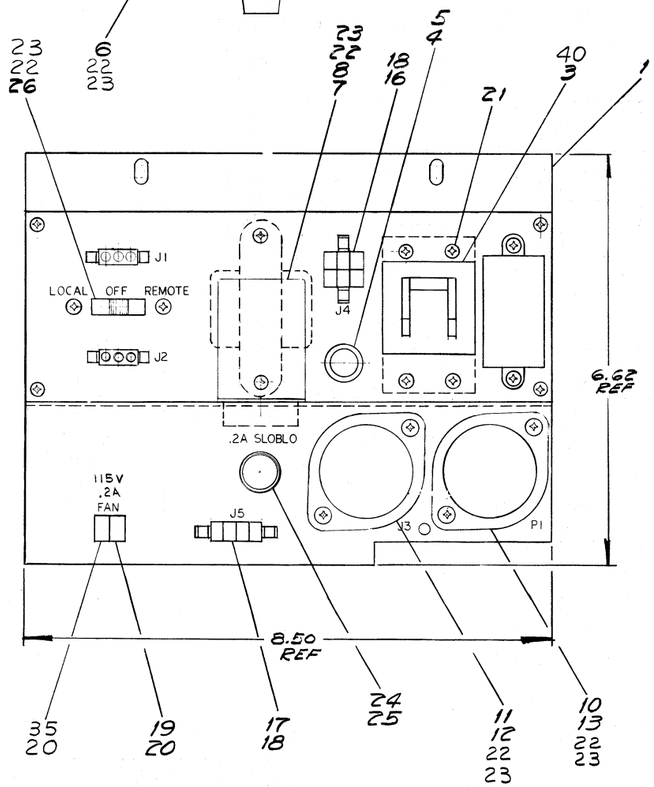
NOTES:
1. APPLY APPROPRIATE DECAL AS FOLLOWS.
   A.) ASSY NO. 7006858-1

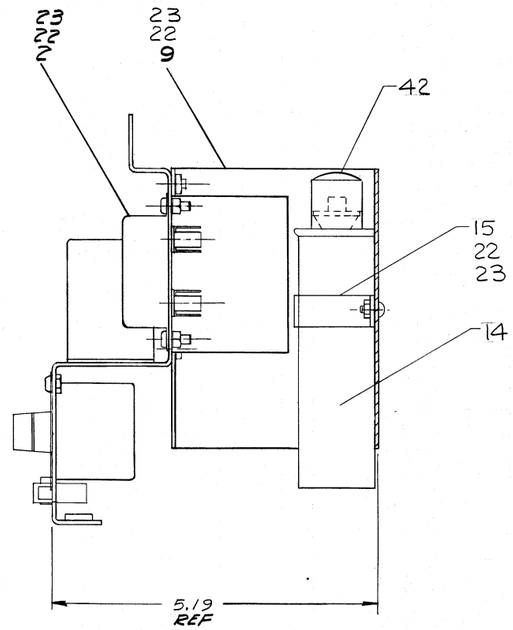
J3	P1
115 VAC	115 VAC
2.5 AMP	5 AMP

   B) ASSY NO. 7006858-2

J3	P1
230 VAC	230 VAC
1.25 AMP	2.5 AMP







REVISIONS	REV.	CHANGE NO.	CHK

FIRST USED ON OPTION/MODEL	DO NOT SCALE DRAWING	QTY.	DESCRIPTION	PART NO.	ITEM NO.
RS64	UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES TOLERANCES DECIMALS ± .005 FRACTIONS ± 1/64 ANGLES ± 0°30' FINAL SURFACE QUALITY ✓ REMOVE BURRS AND BREAK SHARP CORNERS	PARTS LIST			

MATERIAL	DRN. M. White	DATE 5-12-71
— H —	CHK'D. P. Miller	DATE 5-12-71
FINISH	ENG. [illegible]	DATE [illegible]
— H —	PROJ. ENG. —	DATE 5-12-71
NEXT HIGHER ASSY E-UA-RS64-P-0	PROD. [illegible]	DATE [illegible]
SCALE	SHEET 1 OF 3	

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

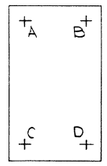
TITLE: CONTROL PANEL

SIZE	CODE	NUMBER	REV.
D	AD	7006858-G-0	

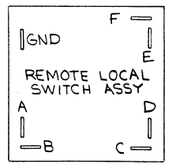
DIST. G

DEC FORM NO. DRD 100

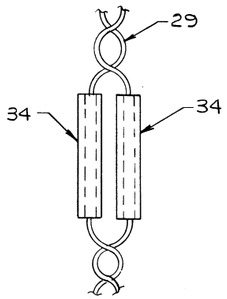
SIZE D | CODE AD | NUMBER 7006858-0-0 | REV.



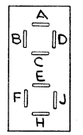
CB1
ITEM 3,40



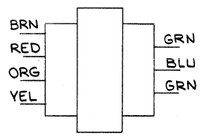
S1
ITEM 26



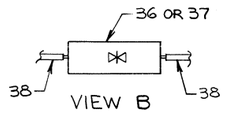
VIEW A



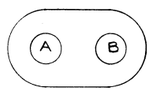
C1
ITEM 2



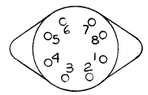
T1
ITEM 6



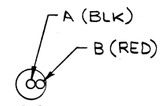
VIEW B



C2
ITEM 14

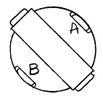


K1
ITEMS 7,8

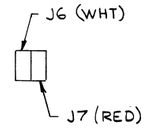


DS1
ITEM 4,5

P1
ITEM 10 (115V)
ITEM 13 (230V)

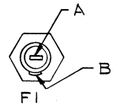


J3
ITEM 11 (115V)
ITEM 12 (230V)



J4
ITEM 16

J5
ITEM 17



F1
ITEM 24

WIRE LIST 115 VAC

ITEM NO	DESCRIPTION AWG	COLOR	FROM CONNECTION	WITH	TO CONNECTION	WITH	REMARKS
29,34	18	RED	P1-B	27	C1-B	28	SEE VIEW A
		WHT	P1-A	27	C1-F	28	
29		RED	J3-A	27	C1-D	28	
		WHT	J3-B	27	C1-H	28	
32		RED	CB1-A	27	C1-A	28	
33	18	WHT	CB1-B	27	C1-J	28	
4		BLK	DS1-A		CB1-B	27	
		RED	DS1-B		CB1-A	27	
29	18	RED	J7-RED	20	CB1-C	27	
		WHT	J6-WHT	20	CB1-D	27	
32		RED	CB1-C	27	J4-3	18	
32		RED	J4-2	18			
32		RED			J4-1	18	
33		WHT	CB1-D	27	J4-4	18	
33		WHT	J4-5	18			
29		WHT			C2-A	28	
	18	RED	J4-6	18	C2-B	28	
6		GRN	T1-GRN		S1-A	28	
		BLU	T1-BLU		F1-A	SOLDER	
		GRN	T1-GRN		S1-B	28	
		BRN	T1-BRN		CB1-D	27	
		ORG	T1-ORG				
		RED	T1-RED		CB1-C	27	
		YEL	T1-YEL				
29	18	WHT	CB1-D	27	K1-3	SOLDER	
		RED	CB1-C	27	K1-6	SOLDER	
30		BLK	K1-2	SOLDER	S1-F	28	
		ORG	K1-7	SOLDER	S1-E	28	
33		WHT	K1-1	SOLDER	J5-1	18	
33		WHT	J5-3	18			
32		RED	K1-8	SOLDER	J5-4	18	
32		RED	J5-2	18			
32		RED	S1-C	28	S1-D	28	
31		GRN	S1-GRD	28	CHASSIS	27	
31	18	GRN	F1-B	SOLDER	CHASSIS	27	

WIRE LIST 230 VAC

ITEM NO	DESCRIPTION AWG	COLOR	FROM CONNECTION	WITH	TO CONNECTION	WITH	REMARKS
29,34	18	RED	P1-B	27	C1-B	28	SEE VIEW A
		WHT	P1-A	27	C1-F	28	
29		RED	J3-A	27	C1-D	28	
		WHT	J3-B	27	C1-H	28	
32		RED	CB1-A	27	C1-A	28	
33	18	WHT	CB1-B	27	C1-J	28	
5		BLK	DS1-A		CB1-B	27	
		RED	DS1-B		CB1-A	27	
29	18	RED	J4-2	18	C2-B	28	
		WHT	J4-1	18	C2-A	28	
33		WHT			J4-4	18	
29		WHT	J6-WHT	20			
		RED	J7-RED	20	J4-3	18	
32		RED	CB1-C	27			
33		WHT	CB1-D	27	J4-6	18	
33	18	WHT	J4-5	18			
6		GRN	T1-GRN		S1-A	28	
		BLU	T1-BLU		F1-A	SOLDER	
		GRN	T1-GRN		S1-B	28	
		BRN	T1-BRN		CB1-D	27	
		RED	T1-RED	39	T1-ORG	39	
		YEL	T1-YEL		CB1-C	27	
29	18	RED	CB1-C	27	K1-6	SOLDER	
		WHT	CB1-D	27	K1-3	SOLDER	
30		BLK	K1-2	SOLDER	S1-F	28	
		ORG	K1-7	SOLDER	S1-E	28	
33		WHT	K1-1	SOLDER	J5-1	18	
33		WHT	J5-2	18	J5-3	18	
32		RED	K1-8	SOLDER	J5-4	18	
32		RED	S1-C	28	S1-D	28	
31		GRN	F1-B	SOLDER	CHASSIS	27	
31	18	GRN	S1-GRD	28	CHASSIS	27	

EXTERNAL COMPONENT LIST 115 VAC

ITEM NO	DESCRIPTION	FROM CONNECTION	WITH	POL	TO CONNECTION	WITH	POL	REMARKS
37,38	THYRECTOR	K1-3	SLDR		K1-1	SLDR		SEE VIEW B
37,38	THYRECTOR	K1-6	SLDR		K1-8	SLDR		SEE VIEW B

EXTERNAL COMPONENT LIST 230 VAC

ITEM NO	DESCRIPTION	FROM CONNECTION	WITH	POL	TO CONNECTION	WITH	POL	REMARKS
36,38	THYRECTOR	K1-3	SLDR		K1-1	SLDR		SEE VIEW B
36,38	THYRECTOR	K1-6	SLDR		K1-8	SLDR		SEE VIEW B

REVISIONS | REV. | CHANGE NO. | CHK

FIRST USED ON OPTION/MODEL: RS64

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
~~DECIMALS FRACTIONS~~ ANGLES
~~.005 1/64~~ ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

QTY. | DESCRIPTION | PART NO. | ITEM NO.
PARTS LIST

DRN. R. Milan DATE 12-30-70
CHK'D. DATE 1-1-71
ENG. DATE
PROJ. ENG. DATE
PROD. DATE
NEXT HIGHER ASSY E-UA-RS64-A-0

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: CONTROL PANEL

SIZE D | CODE AD | NUMBER 7006858-0-0 | REV.
SCALE
SHEET 2 OF 3
DIST.

DEC FORM NO. DRD 100

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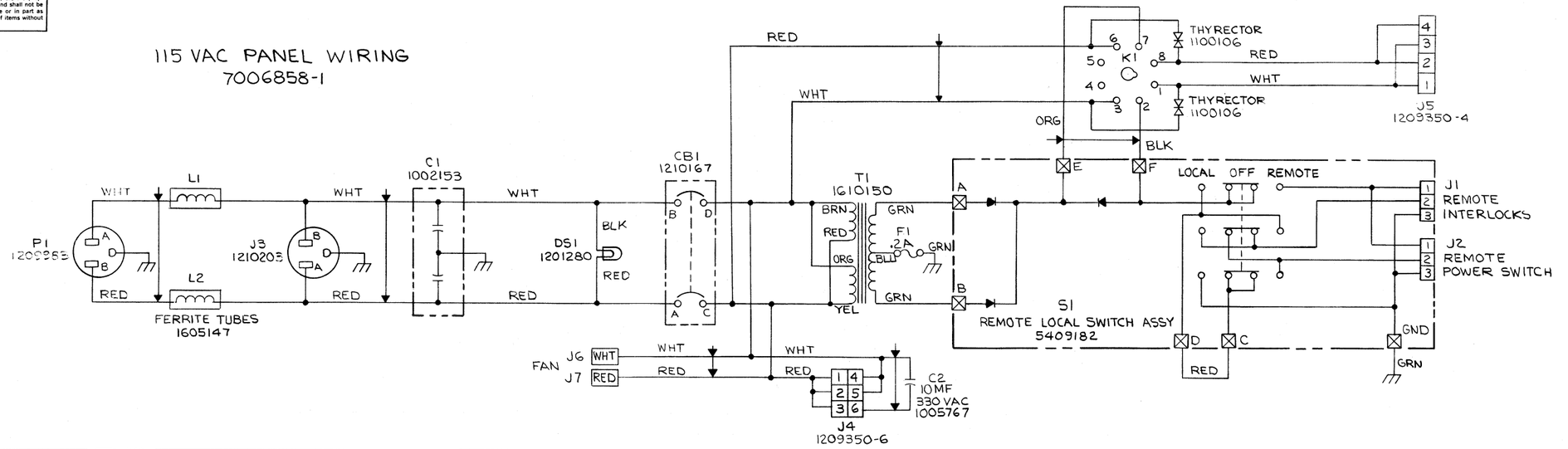
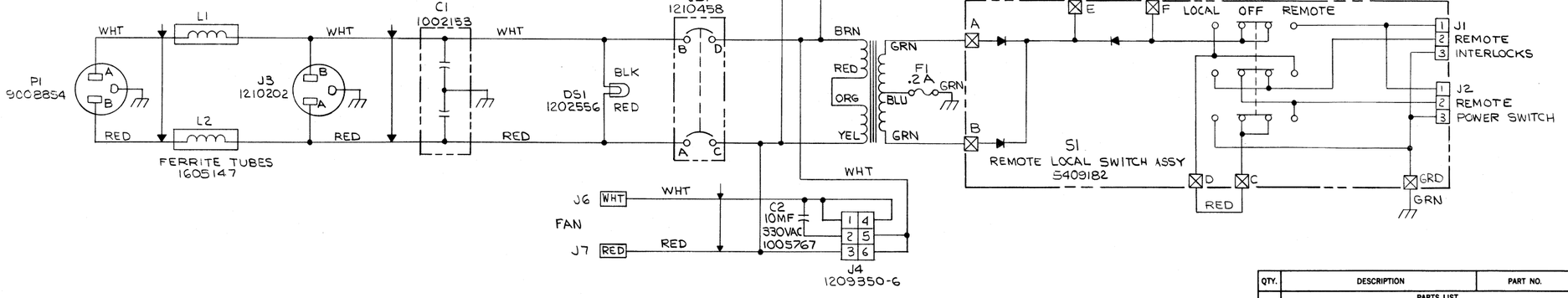
115 VAC PANEL WIRING
7006858-1



230 VAC PANEL WIRING
7006858-2



QTY.	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

FIRST USED ON OPTION/MODEL: RS64

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
.005 ± 1/64 ± 0°30'
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS

MATERIAL

FINISH

DRN. P. Milan	DATE 1-3-71	digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS
CHK'D. P. Milan	DATE 2-1-71	
ENG.	DATE 2-25-71	
PROJ. ENG.	DATE 3-1-71	
PROD.	DATE 3-1-71	

TITLE: CONTROL PANEL

NEXT HIGHER ASSY: E-UA-RS64- -Ø

SCALE

SHEET 3 OF 3

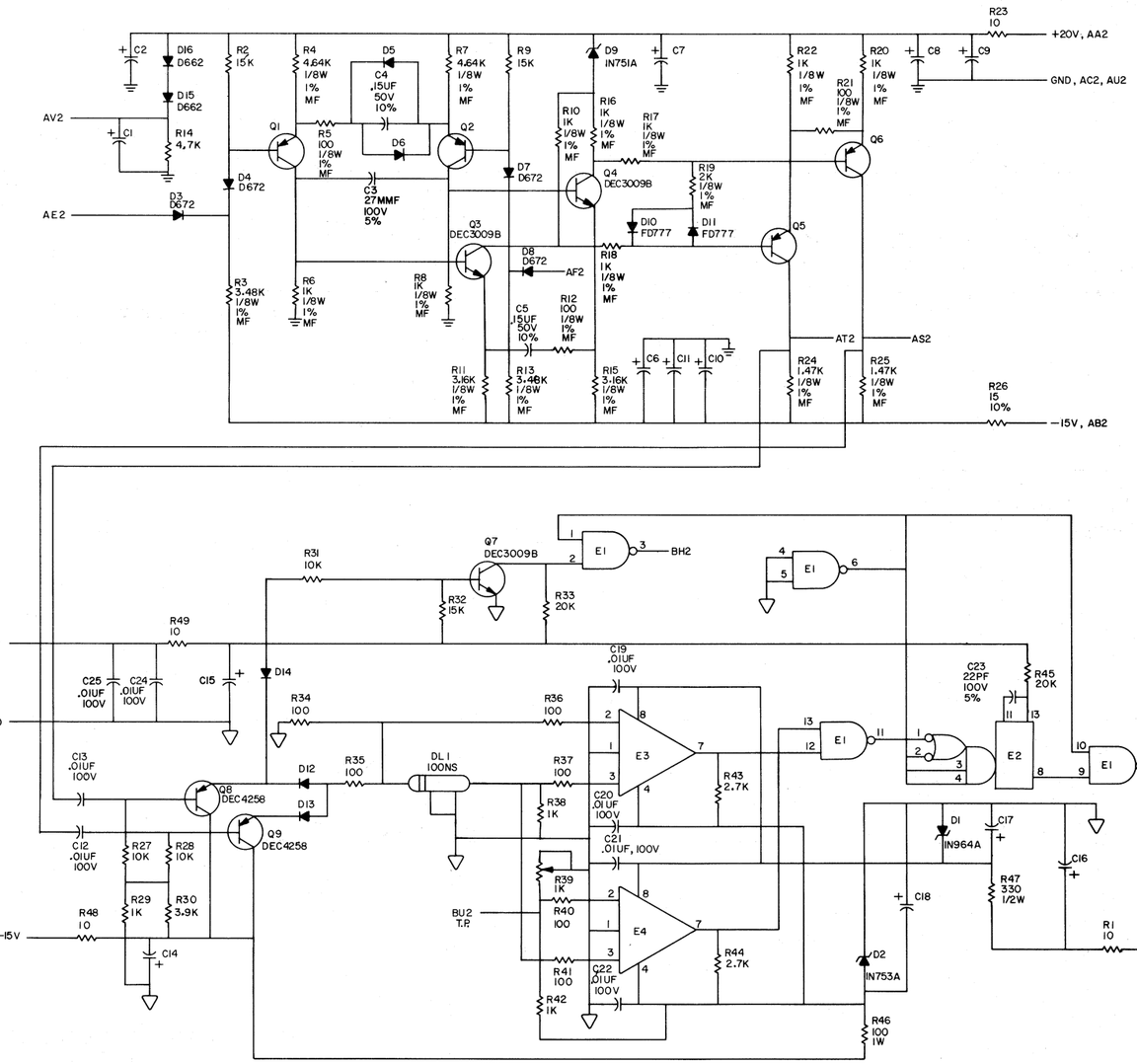
SIZE D | CODE AD | NUMBER 7006853-Ø-Ø | REV.

DIST.

REVISIONS: REV. | CHANGE NO. | CHK.

DEC FORM NO. DRD 100

REV. 0 | SIZE/CODE D AD | NUMBER 7006858-0-0



UNLESS OTHERWISE INDICATED:

RESISTORS ARE 1/4W, 5%
CAPACITORS ARE 6.8UF, 35V, 20%
DIODES ARE D664
TRANSISTORS ARE DEC6534C
POTENTIOMETER IS A 1K, 3/4W, 76PR
DEC7400 = E1
DEC9601 = E2
UA710 = E3, E4

PIN 7 = GND ON E1 AND E2
PIN 14 = +5V

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D664	IN3606	D672	IN3655
D662	IN645	IN751A	SAME
IN964A	SAME	DEC3009B	2N3646
IN753A	SAME	DEC6534C	NONE
FD777	SAME	DEC4258	2N4258

REVISIONS: CHG REQ 10000 | REV F

DRN. George Wyatt DATE 1-6-71
CHKD. DATE 1-15-71
ENG. Ray Key DATE 1/15/71
PROG. DATE

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: READ AMP PEAK DETECTOR G088
SIZE D | CODE CS | NUMBER G088-0-1 | REV. F
PRINTED CIRCUIT REV. E

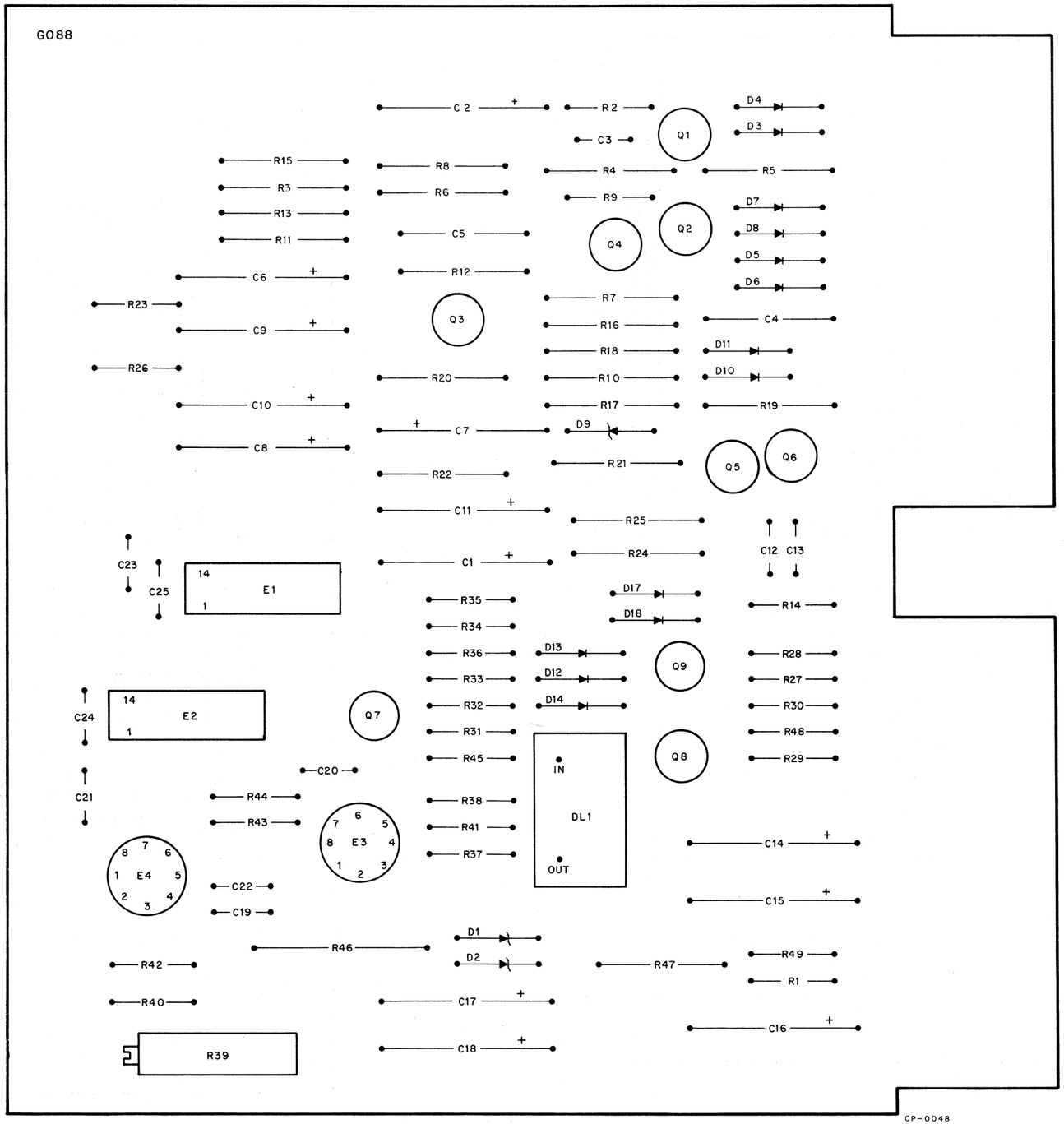
DEC FORM RQ. DBD 118

DIST: 32U, U2:, 435 2
4 PINK

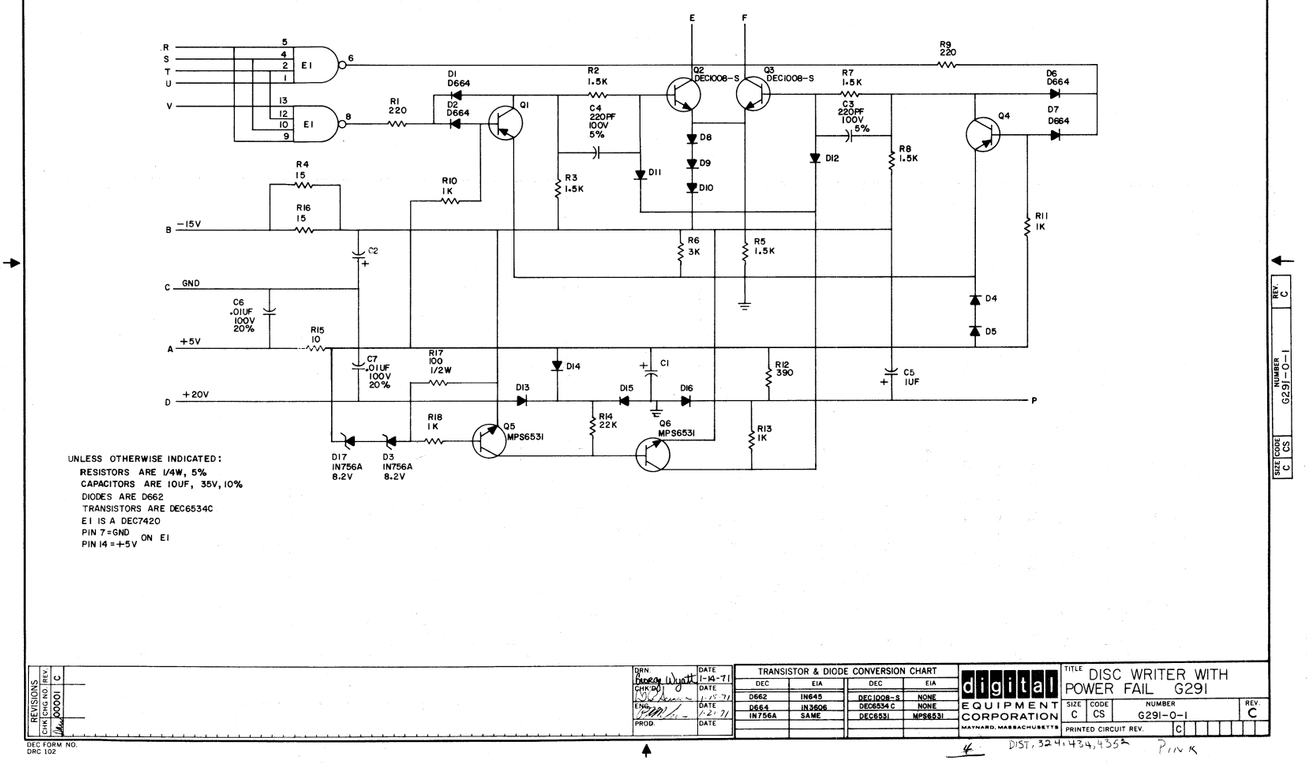
SIZE CODE D CS | NUMBER G088-0-1 | REV F

D-AH-G088-0-5, Rev D

G088



CP-0048



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W, 5%
CAPACITORS ARE 10UF, 35V, 10%
DIODES ARE D662
TRANSISTORS ARE DEC6534C
E1 IS A DEC7420
PIN 7=GND
PIN 14=+5V ON E1

REVISIONS
CHR | CHG NO | REV
A | 00001 | C

DRN: [illegible] DATE 1-14-71
CHK (QC) [illegible] DATE 1-2-71
ENG [illegible] DATE 1-2-71
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D662	IN645	DEC1008-S	NONE
D664	IN3606	DEC6534C	NONE
IN756A	SAME	DEC6531	MPS6531

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

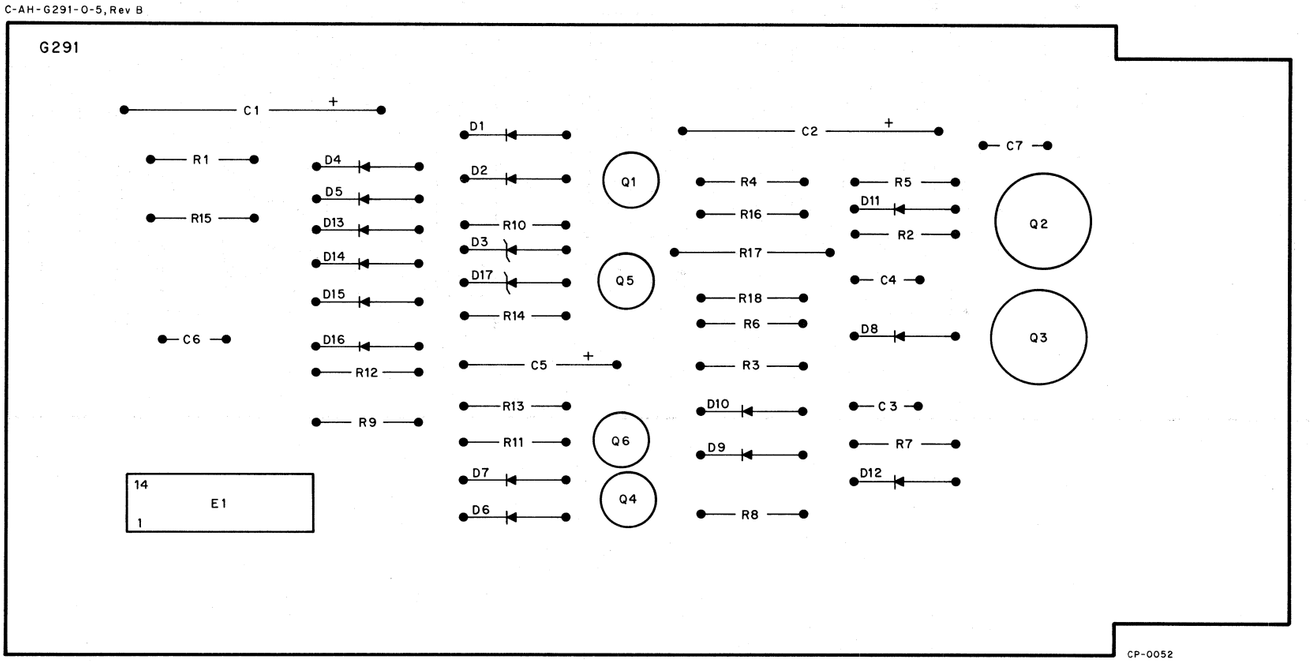
TITLE DISC WRITER WITH POWER FAIL G291
SIZE C | CODE CS | NUMBER G291-0-1 | REV. C
PRINTED CIRCUIT REV. C

DEC FORM NO. DRC 102

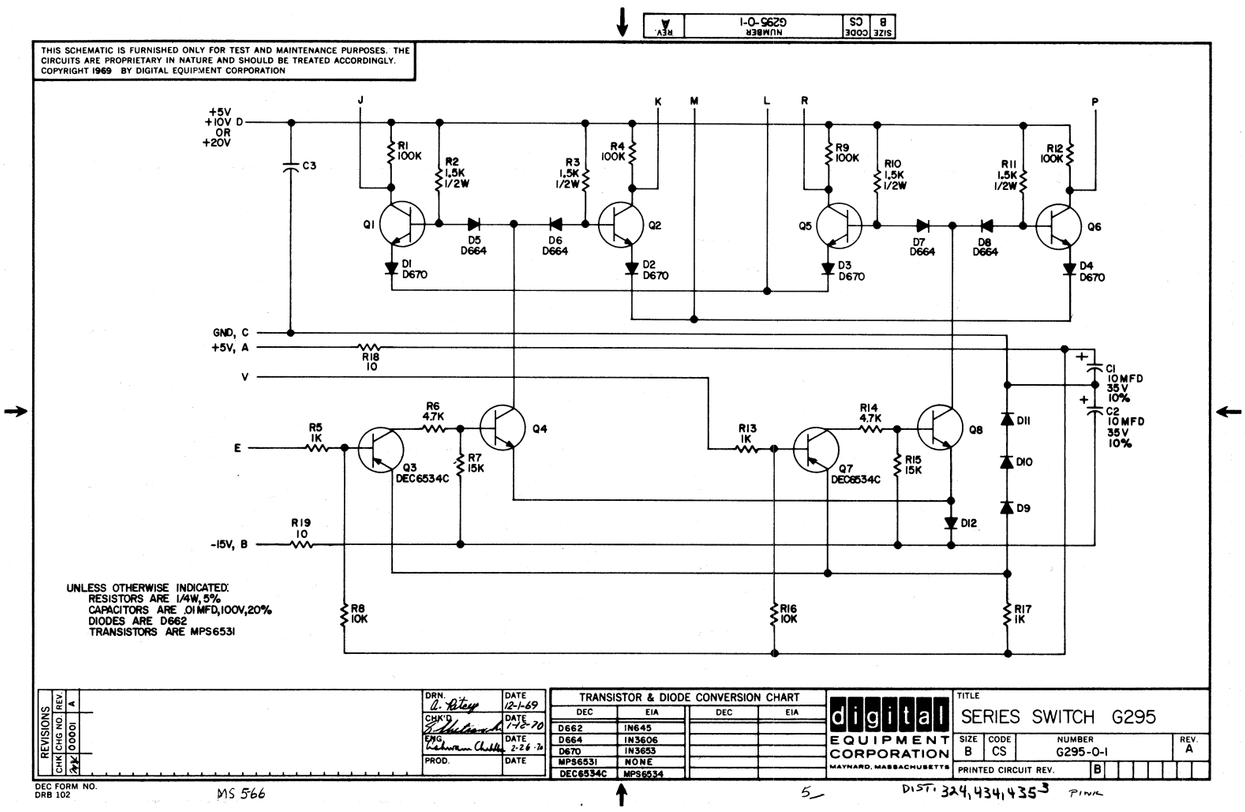
DIST. 32,4,4,3,4,4,5,3 PINK

REV. C | CODE CS | SIZE C | NUMBER G291-0-1

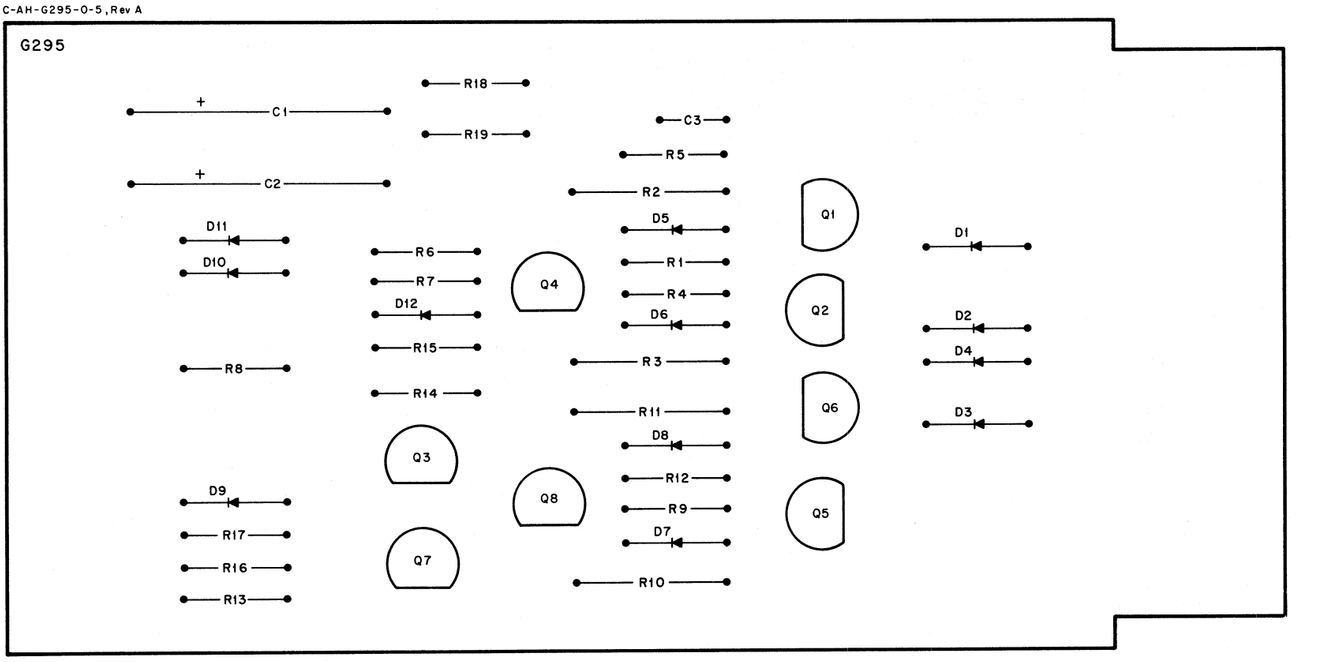
C-AH-G291-0-5, Rev B



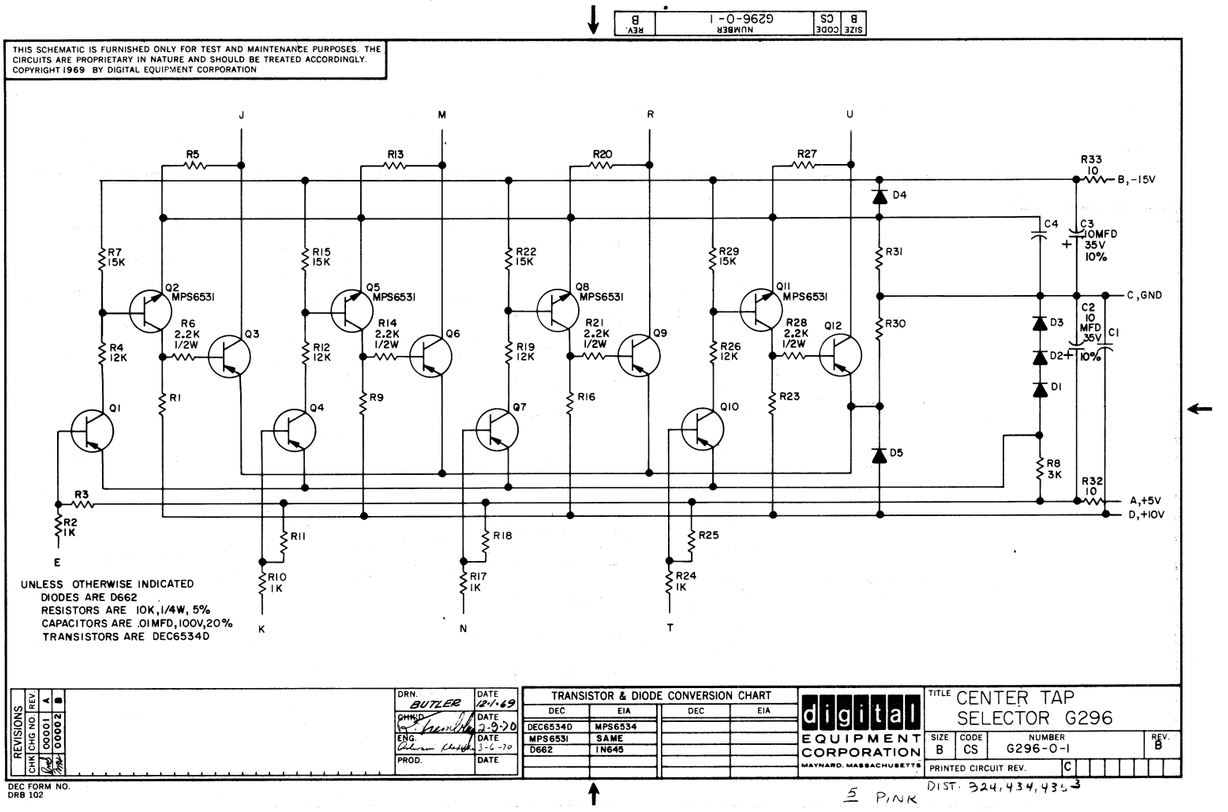
CP-0052



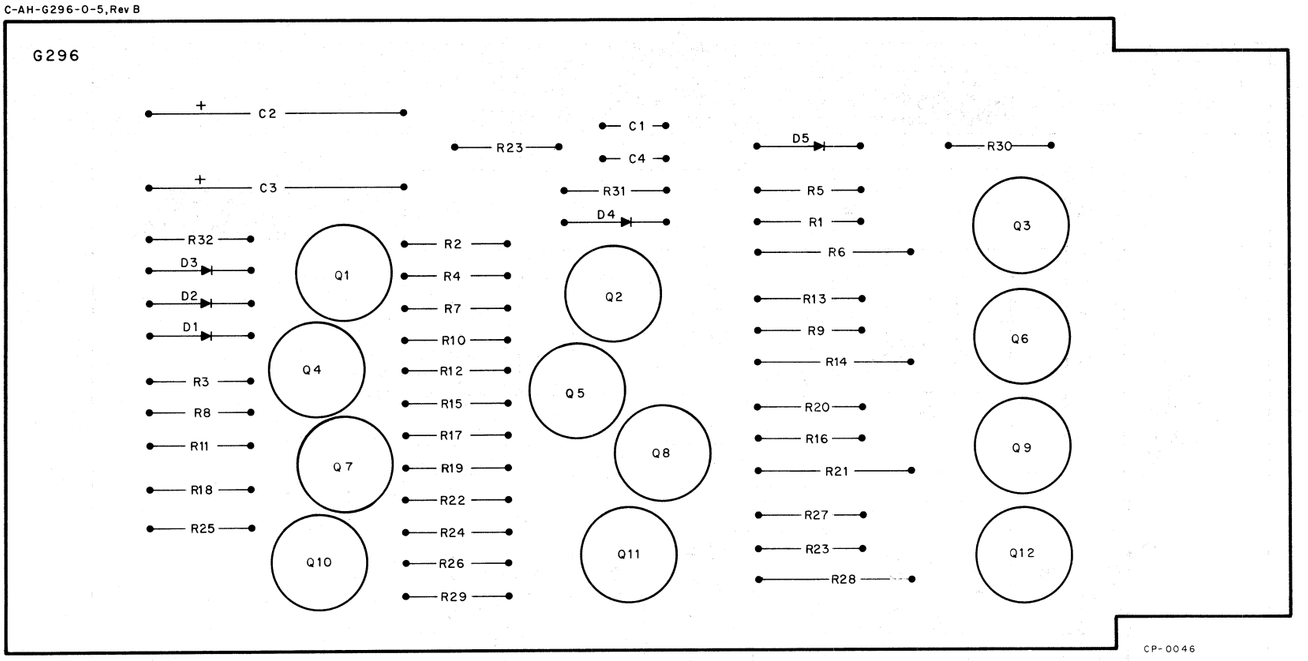
C-AH-G295-0-5, Rev A

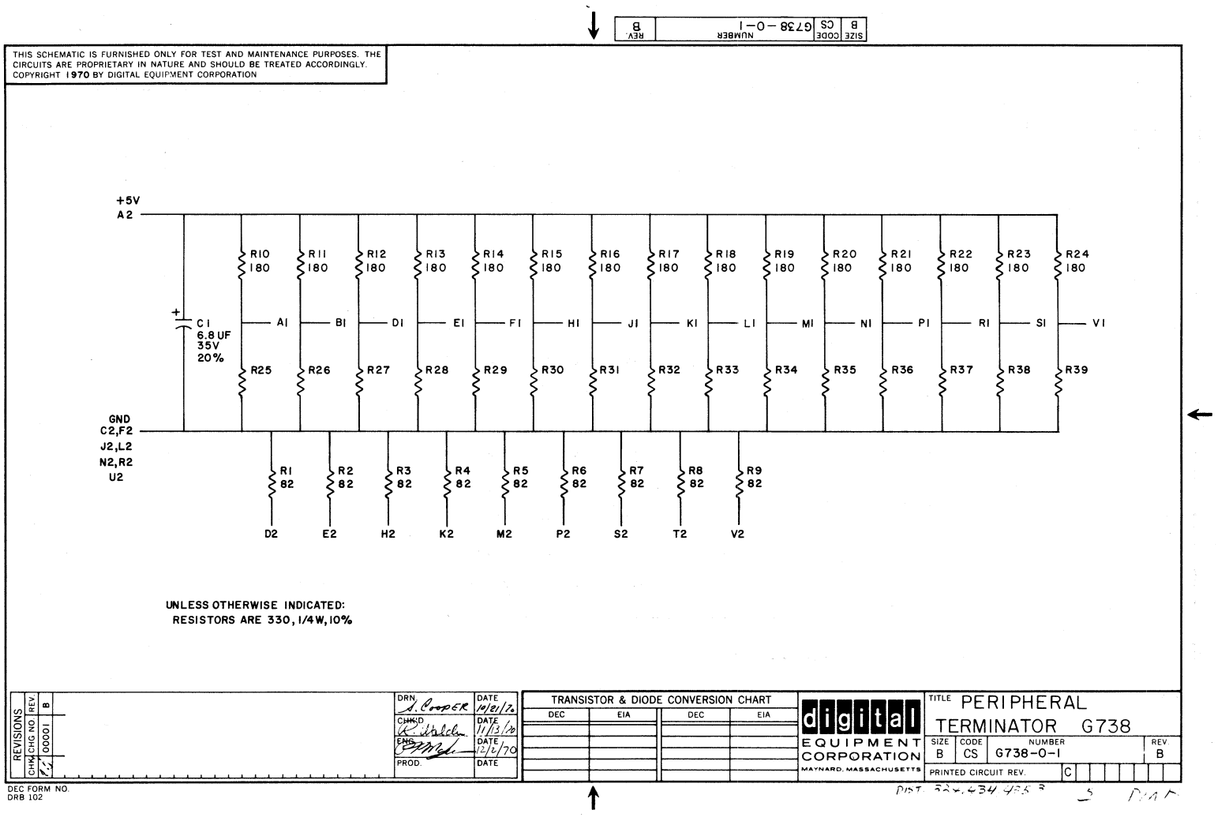


CP-0047

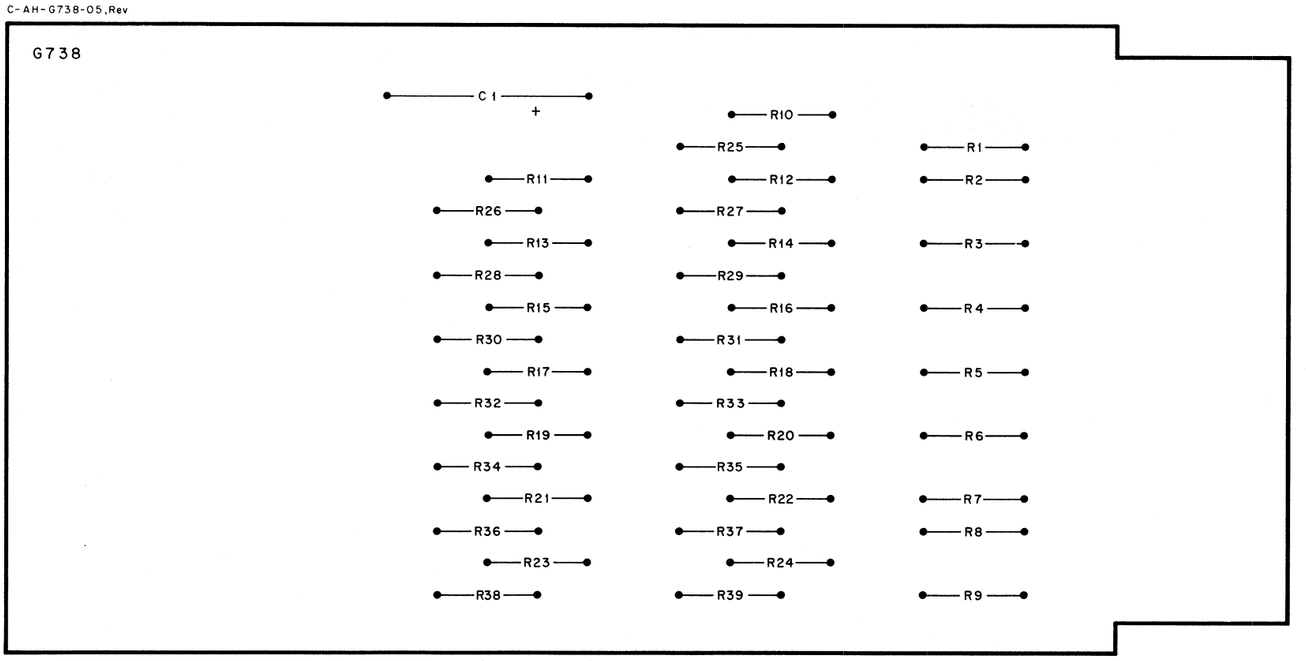


C-AH-G296-0-5,Rev B



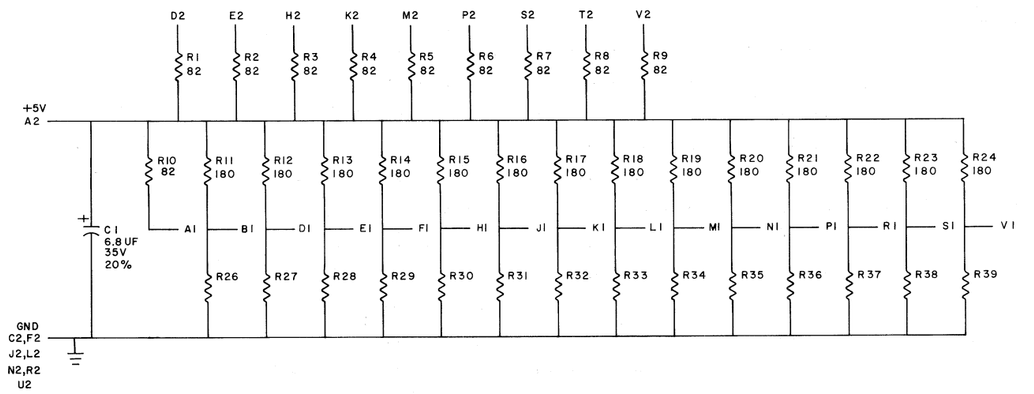


C-AH-G738-05,Rev



CP-0109

SIZE B | CODE CS | NUMBER G739-0-1 | REV B



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 330, 1/4W, 10%

REVISIONS

CHK	CHG NO	REV
DGO	01	A
DGO	02	B

DRN A. Cooper DATE 10/28/70
CHK'D DATE 11/2/70
ENG DATE 12/1/70
PROD. DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

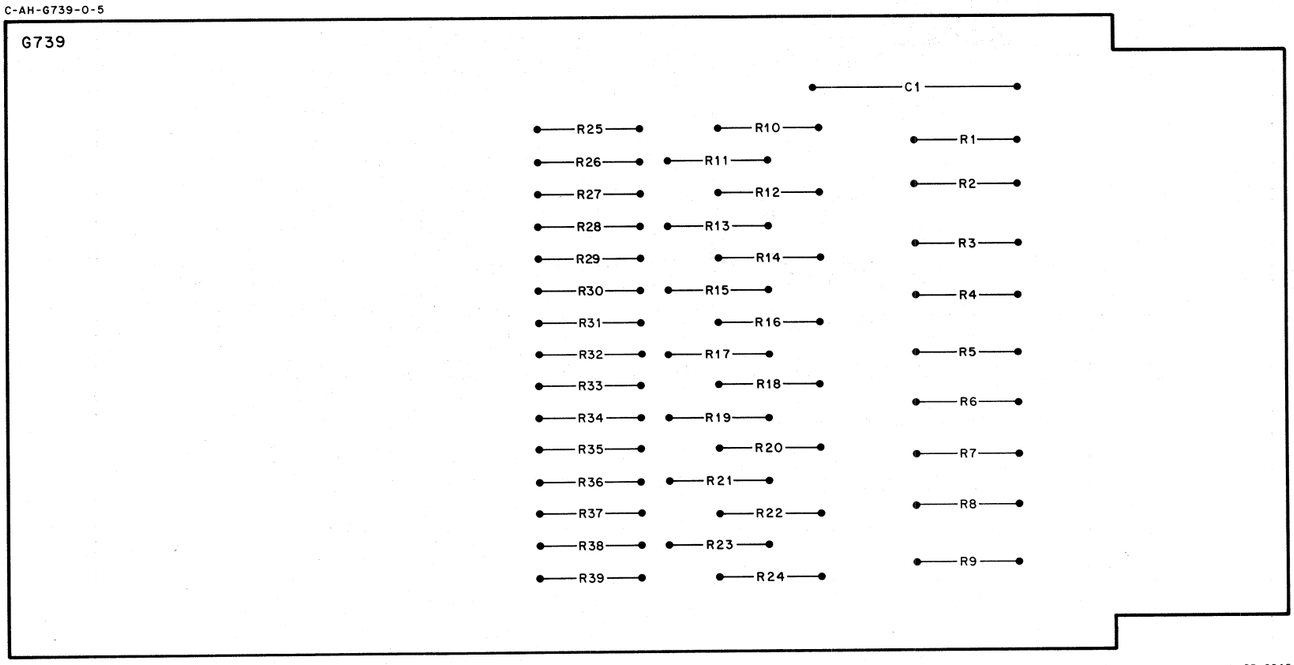
TITLE PERIPHERAL TERMINATOR G739

SIZE	CODE	NUMBER	REV.
B	CS	G739-0-1	B

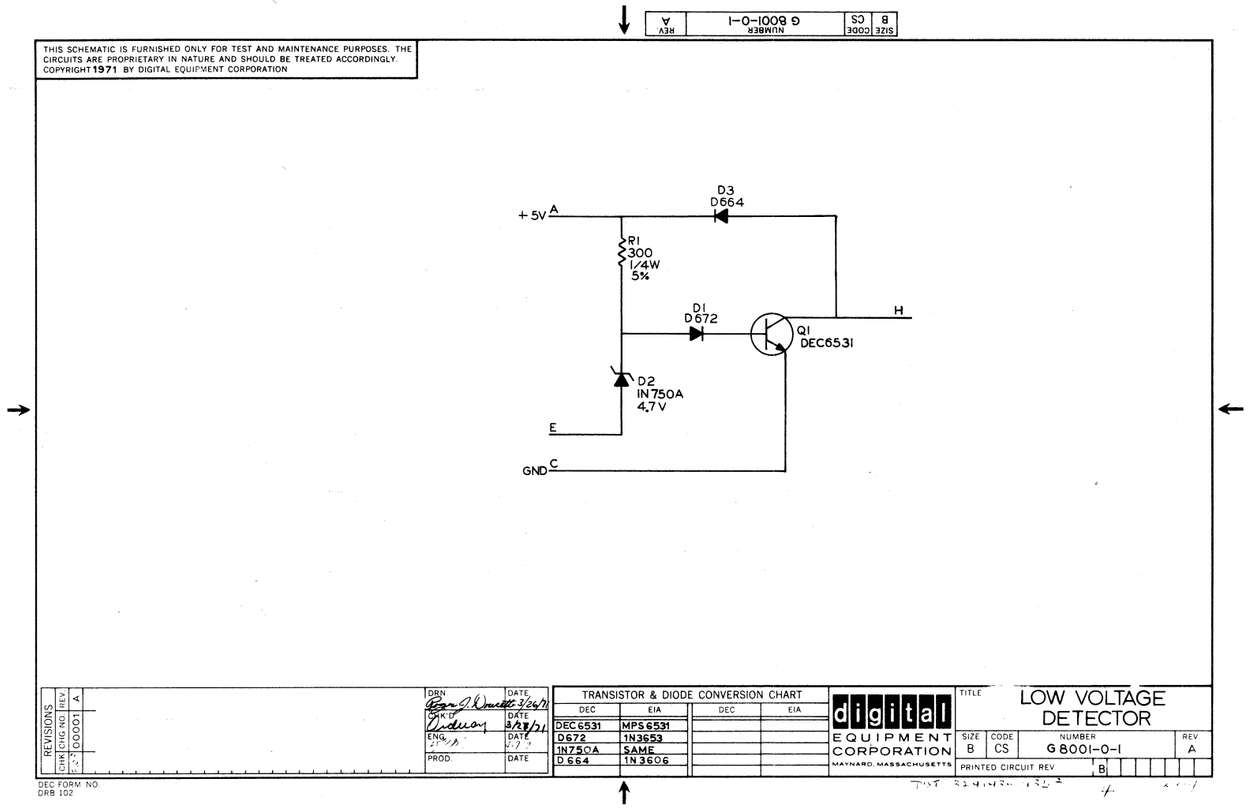
PRINTED CIRCUIT REV. B

DEC FORM NO. DRB 102

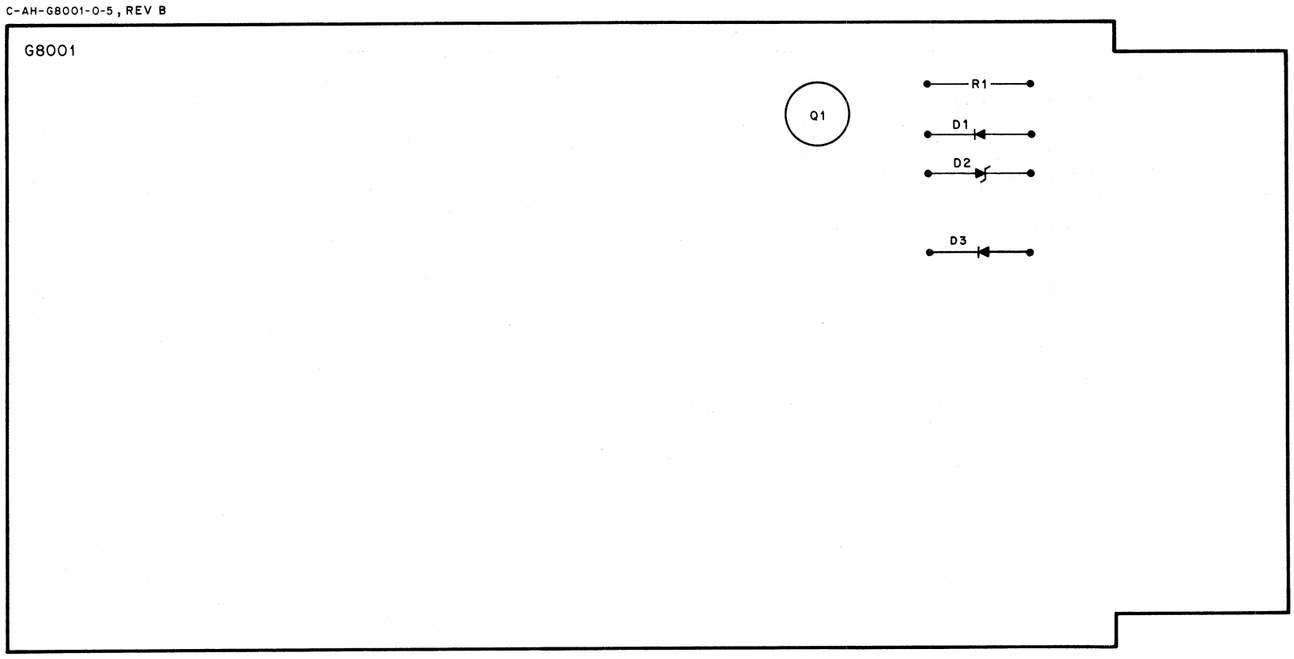
C-AH-G739-0-5



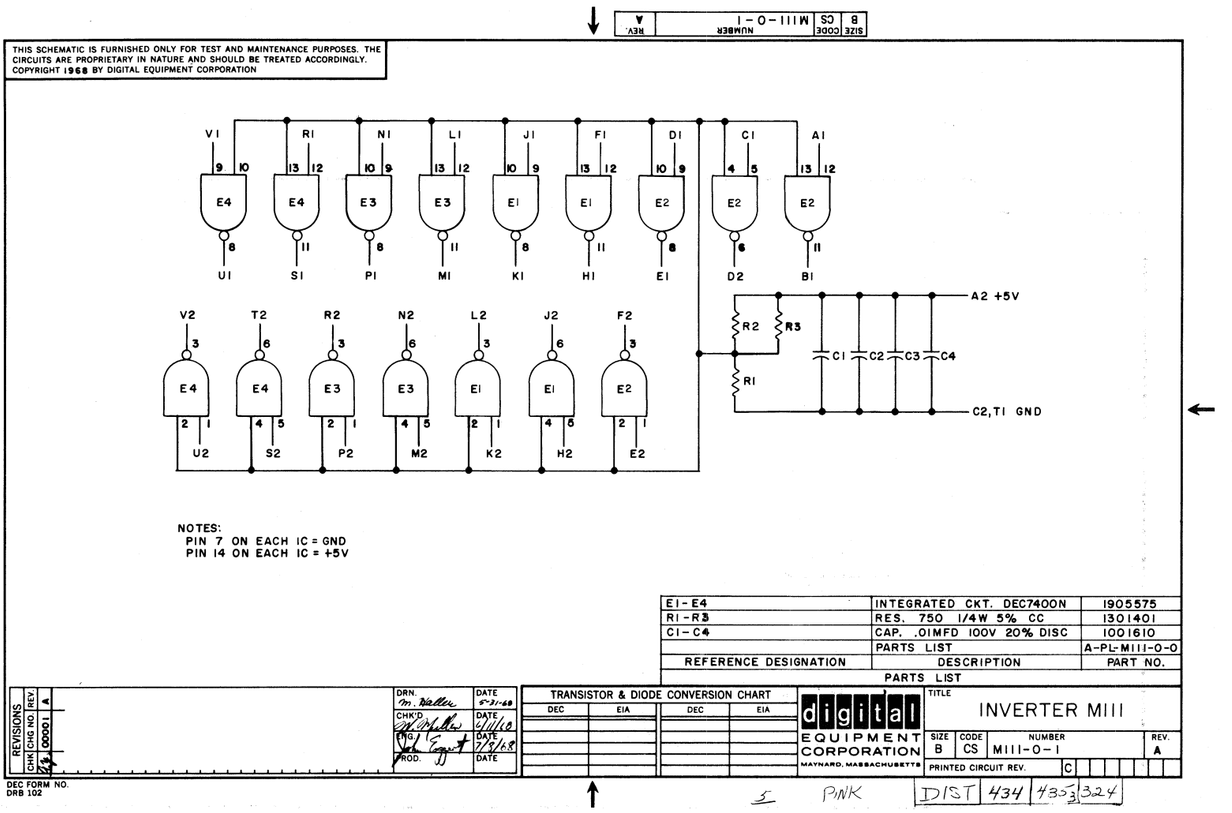
CP-0045



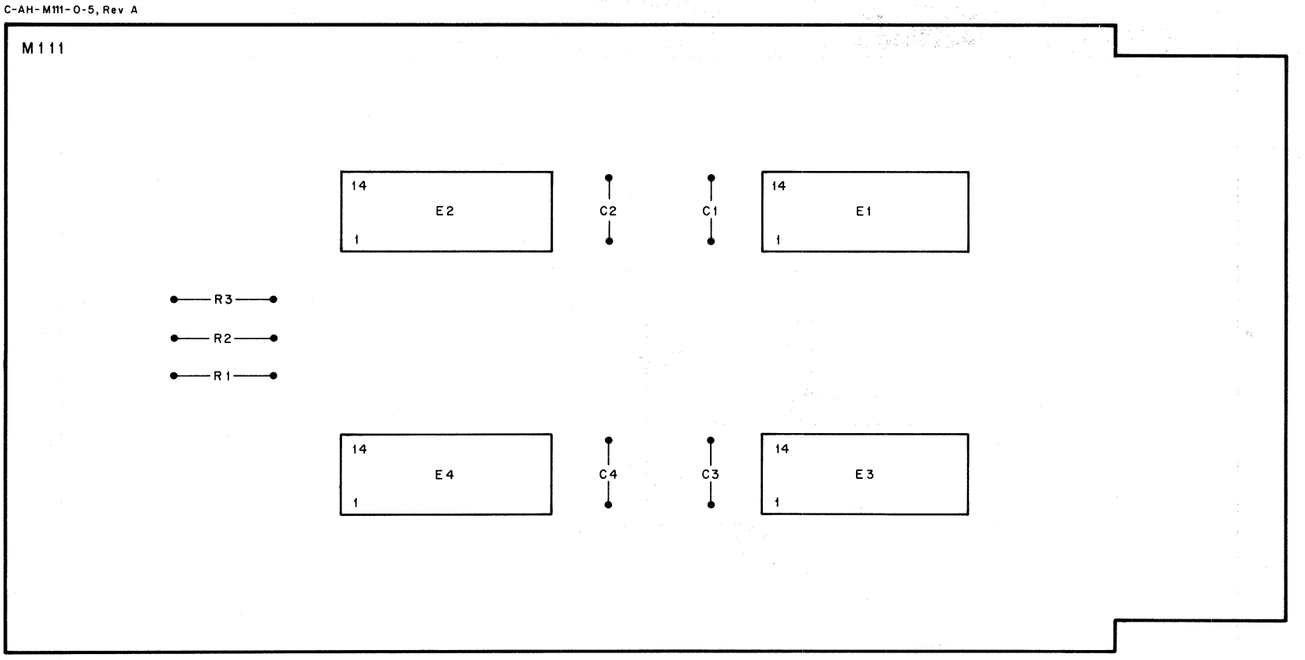
C-AH-G8001-0-5, REV B



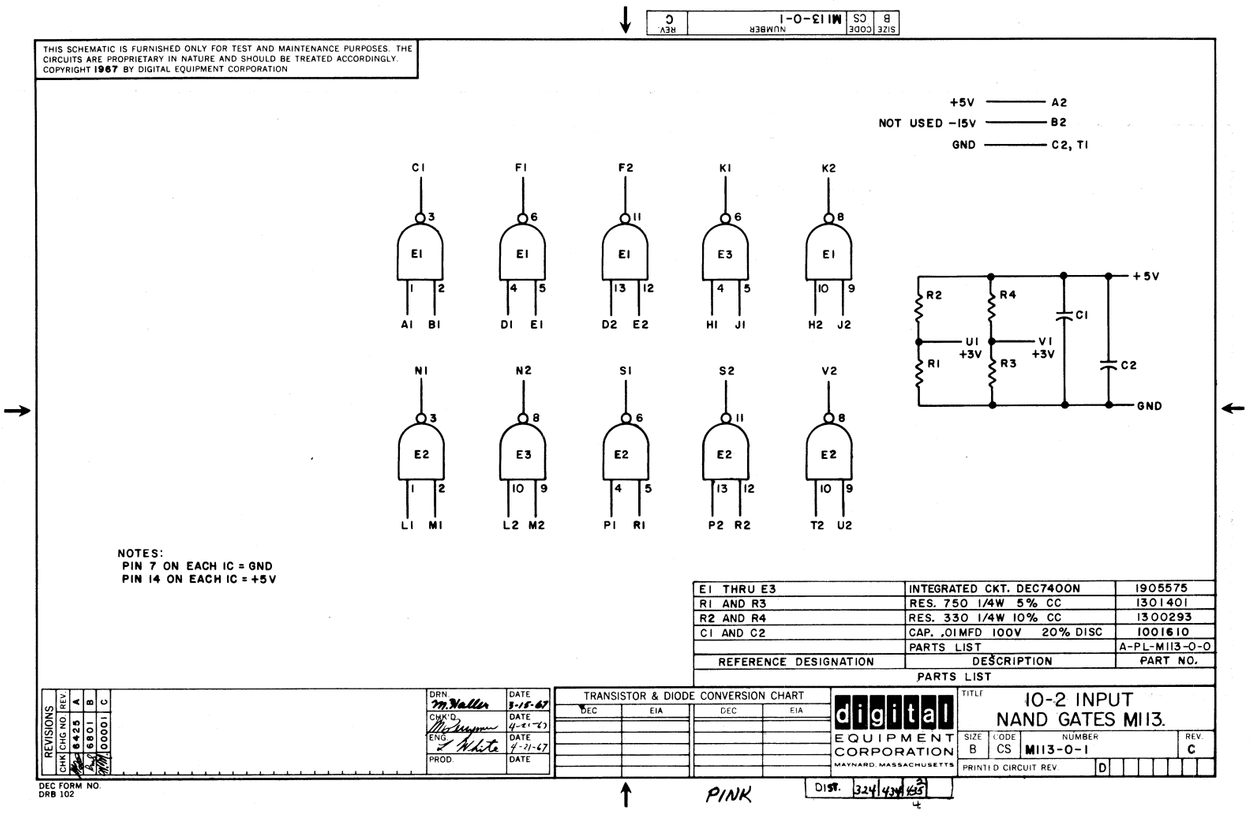
CP-0041



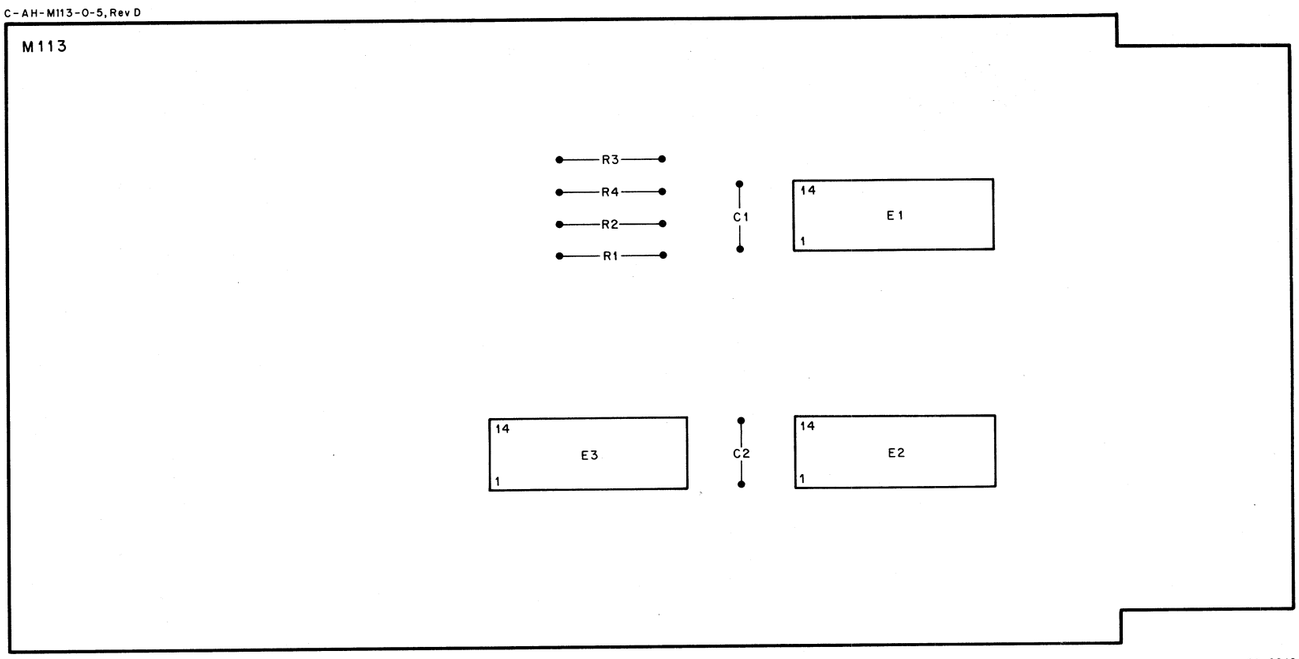
C-AH-M111-0-5, Rev A



CP-0039

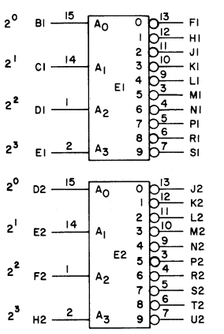


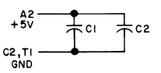
C-AH-M113-0-5, Rev D



CP-0042

SIZE	CODE	NUMBER	REV
B	CS	M163-0-1	A





UNLESS OTHERWISE INDICATED:
PIN 8 ON EACH IC = GND
PIN 16 ON EACH IC = +5V
E1 AND E2 ARE FAIRCHILD 9301
CAPACITORS ARE .01 MFD

REVISIONS	CHK	CHG NO.	REV
	RK	10001	A

DRN.	BUTLER	DATE 12/3/68
CHK'D	[illegible]	DATE 12/3/68
ENG.	[illegible]	DATE 12/3/68
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE DUAL BINARY TO DECIMAL DECODER M163

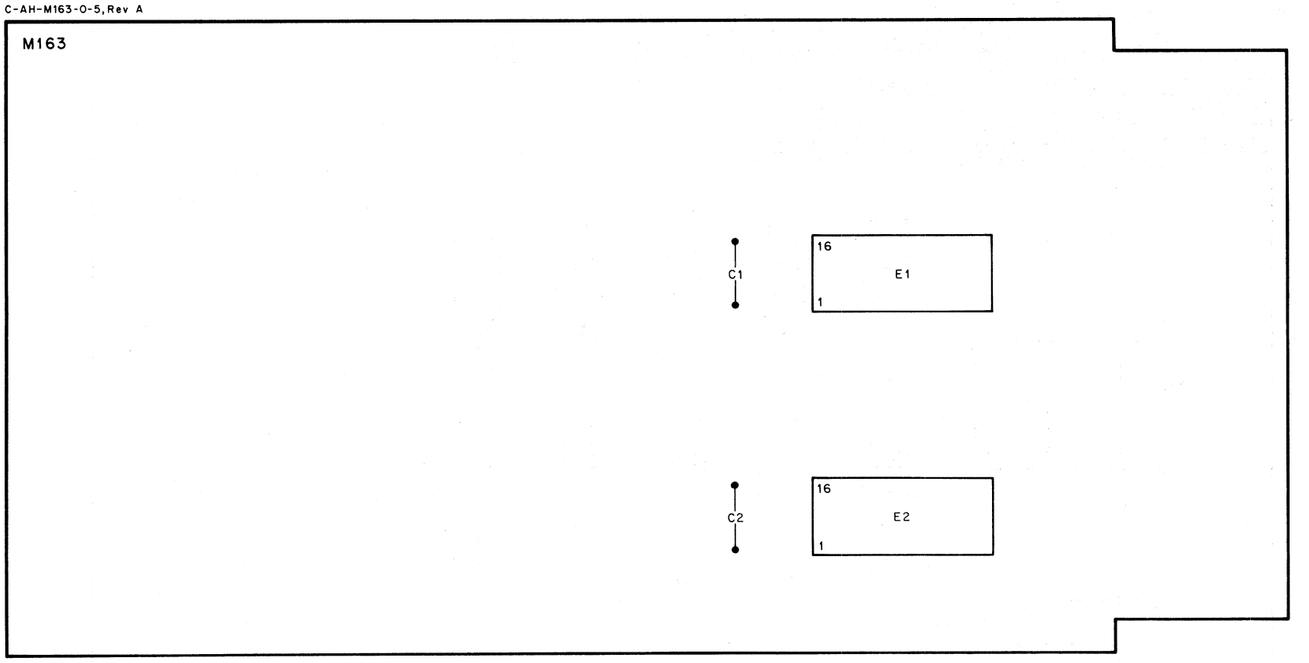
SIZE	CODE	NUMBER	REV.
B	CS	M163-0-1	A

PRINTED CIRCUIT REV. A

DEC FORM NO. DRB 102

5 DIST. 324,434,435 PINK

C-AH-M163-0-5, Rev A



CP-2044

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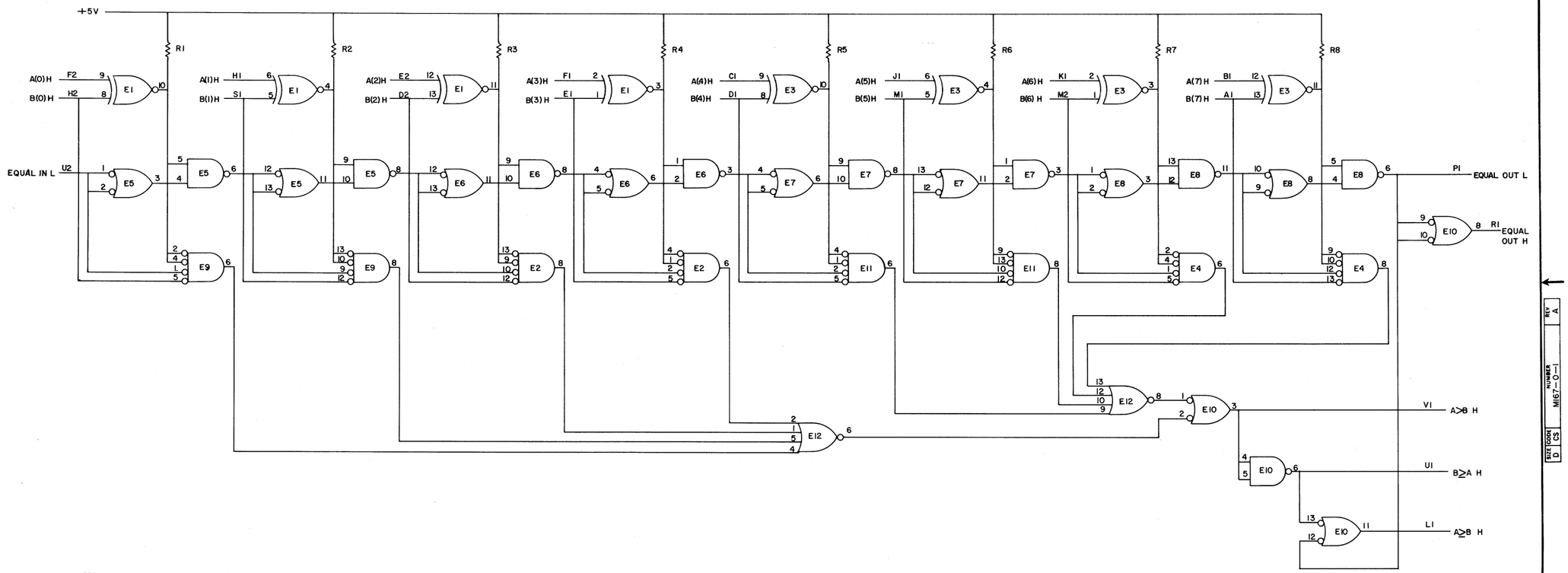
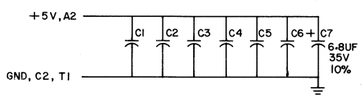




UNLESS OTHERWISE INDICATED;
RESISTORS ARE 470, 1/4W, 5%
CAPACITORS ARE .01UF, 100V, 20%
DEC74H00 = E5, E6, E7, E8, E10
DEC8815 = E2, E4, E9, E11, E12
DEC8242 = E1, E3
PIN 7 = GND
PIN 14 = +5V ON ALL IC'S

REVISIONS			
CHK CHG NO.	REV.		

DRN		DATE 1-14-71
CHK'D		DATE 1-22-71
ENG		DATE 2-1-71
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: MAGNITUDE COMPARATOR M167

SIZE	CODE	NUMBER	REV.
D	CS	M167-0-1	A

PRINTED CIRCUIT REV. B

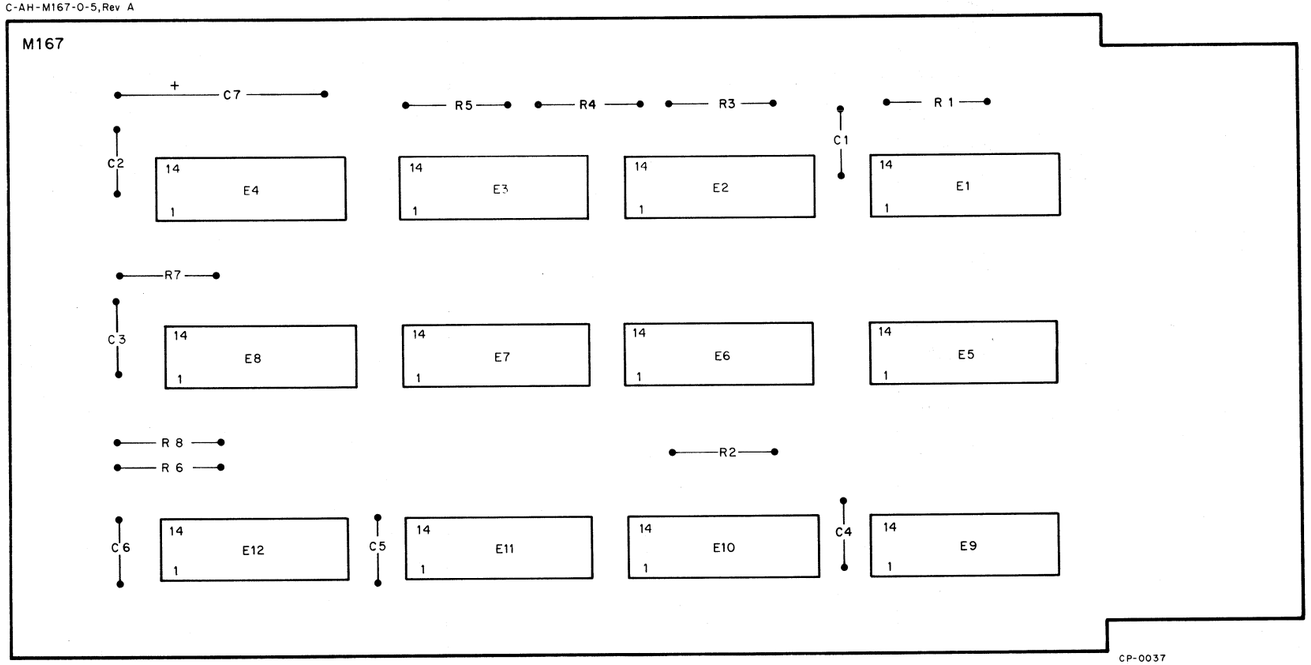
DEC FORM NO. DBD 118

DIST. 324,434,435 2

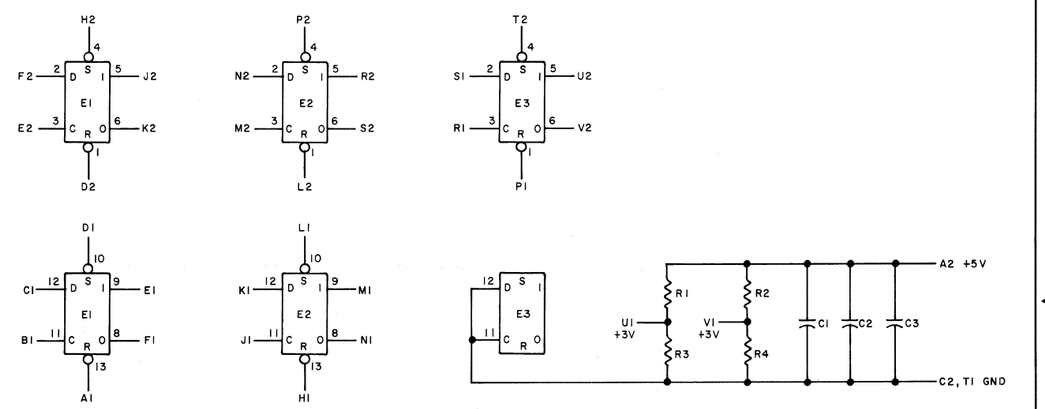
4 PNK

SIZE D | CODE CS | NUMBER M167-0-1 | REV A

C-AH-M167-0-5,Rev A



SIZE B | CODE CS | NUMBER M205-0-1 | REV B



NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V

REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	A-PL-M205-0-0
E1, E2, E3	INTEGRATED CKT. DEC7474N	1905547
R3, R4	RES. 750 1/4W 5% CC	1301401
R1, R2	RES. 330 1/4W 5% CC	1300295
C1, C2, C3	CAP. .01MFD 100V 20% DISC	1001610

PARTS LIST

REVISIONS | REV. B | CHG NO. 00001 | CHK

DRN. M. Waller	DATE 2-17-69	
CHK'D L. Schreiner	DATE 3/13/69	
ENGR. R. Cannon	DATE 4/7/69	
PROD.	DATE	

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: 5 "D" FLIP FLOPS M205

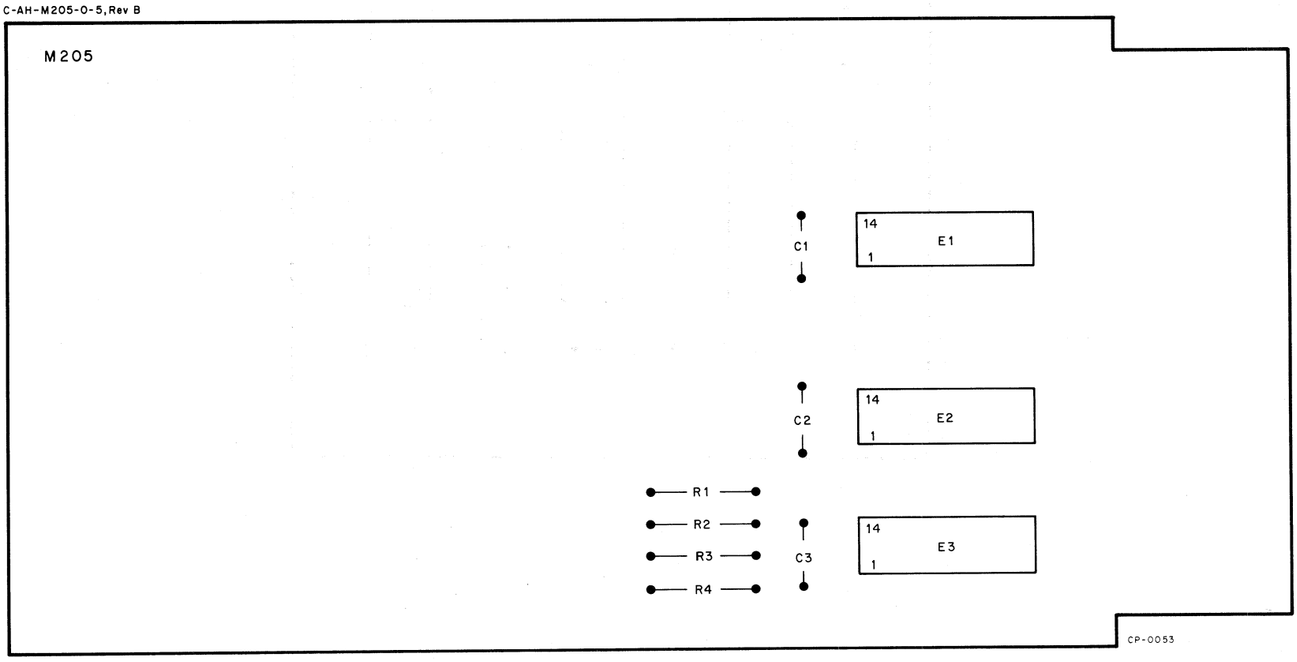
SIZE	CODE	NUMBER	REV.
B	CS	M205-0-1	B

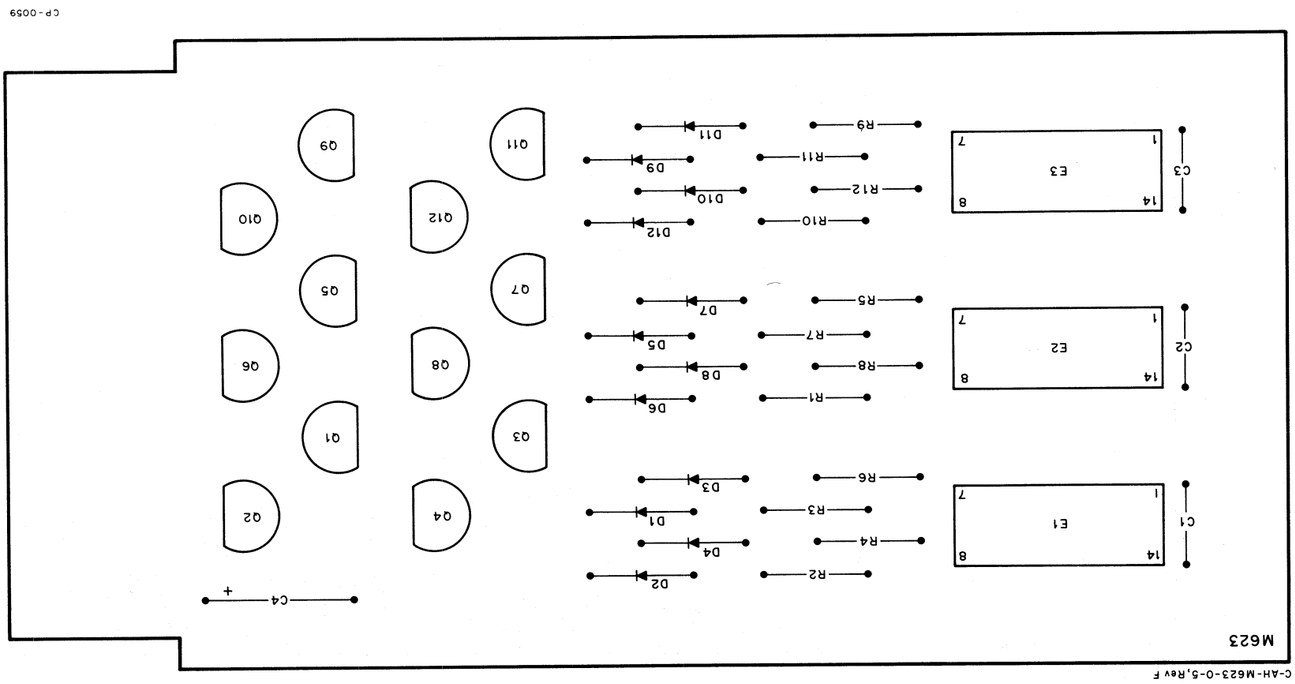
PRINTED CIRCUIT REV. A

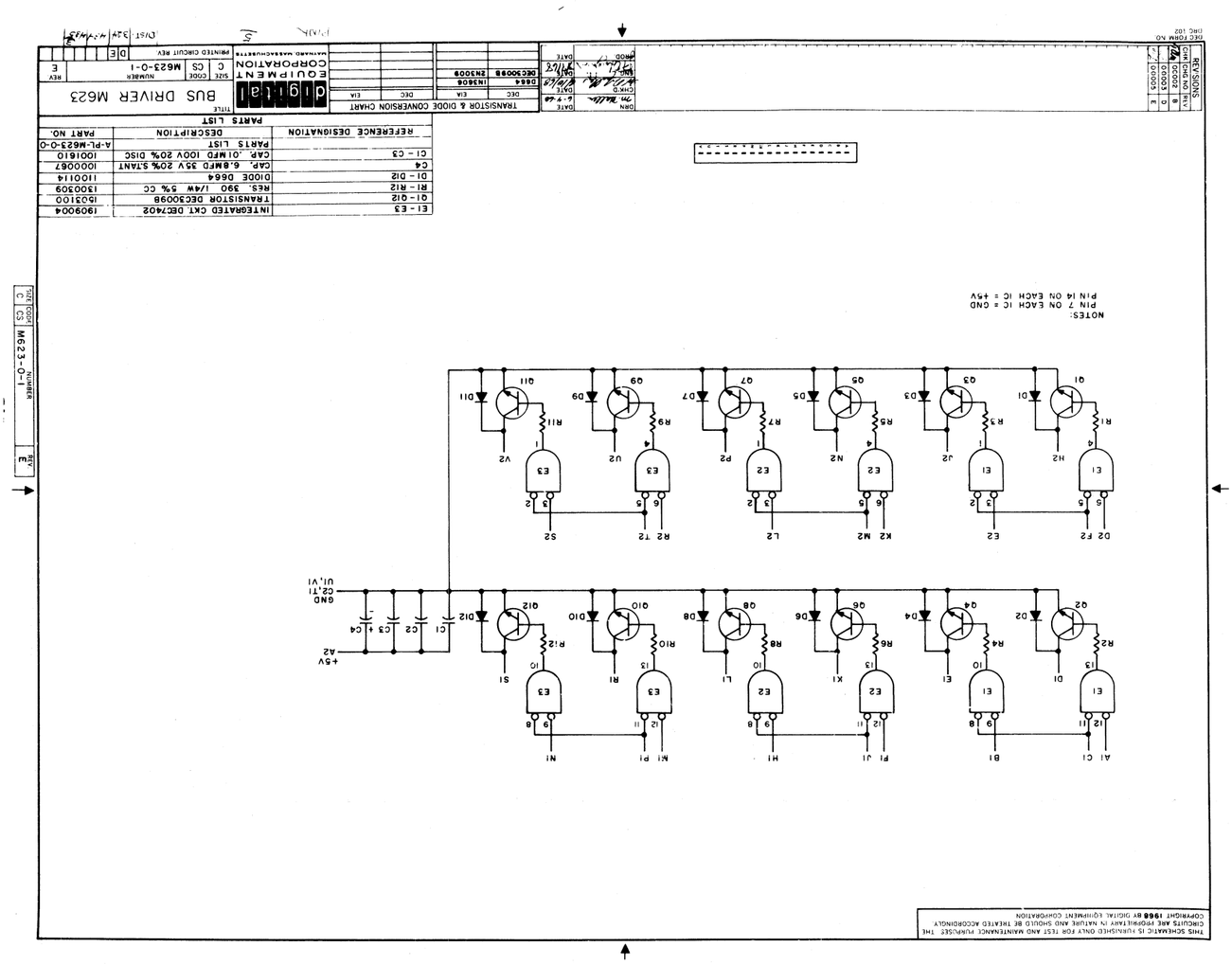
DEC FORM NO. DRB 102

5 DIST. 324,434,435 PINK

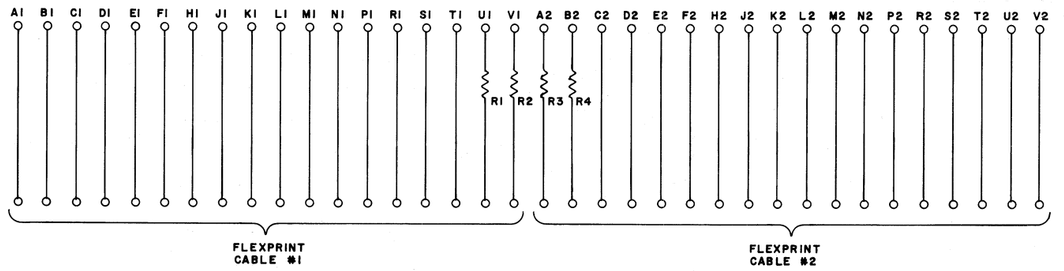
C-AH-M205-0-5, Rev B




CP-0059
M623
C-AH-M623-0-5,Rev F
C1
C2
C3
C4
E1
E2
E3
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12


BUS DRIVER M623
digital
EQUIPMENT CORPORATION
M623-0-1
TRANSISTOR & DIODE CONVERSION CHART
PARTS LIST
REFERENCE DESIGNATION
DESCRIPTION
PART NO.
E1 - E3
INTEGRATED CKT DEC7402
1909004
Q1 - Q12
TRANSISTOR DEC2009B
1502100
R1 - R12
RES. 390 1/4W 2% CC
1500309
D1 - D12
DIODE D664
1100114
C4
CAP. 6.8MFD 35V 20% STANT
1000087
C1 - C3
CAP .01MFD 100V 20% DISC
1001610
A-PL-M623-0-0
PARTS LIST
NOTES:
PIN 7 ON EACH IC = GND
PIN 14 ON EACH IC = +5V
+5V
GND
C1
C2
C3
C4
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
E1
E2
E3

SIZE B | CODE CS | NUMBER M901-0-1 | REV. C



REFERENCE DESIGNATION	DESCRIPTION	PART NO.
R1-R4	RES. 10 1/4W 10% CC	1300170
	PARTS LIST	A-PL-M901-0-0

PARTS LIST

REVISIONS	CHG NO	REV
	0001	C

		DATE
DRN.	M. Waller	8-14-68
CHKD.	[illegible]	8/19/68
ENG.	[illegible]	11/5/68
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: FLEXPRINT CABLE CONNECTOR M901

SIZE	CODE	NUMBER	REV.
B	CS	M901-0-1	C

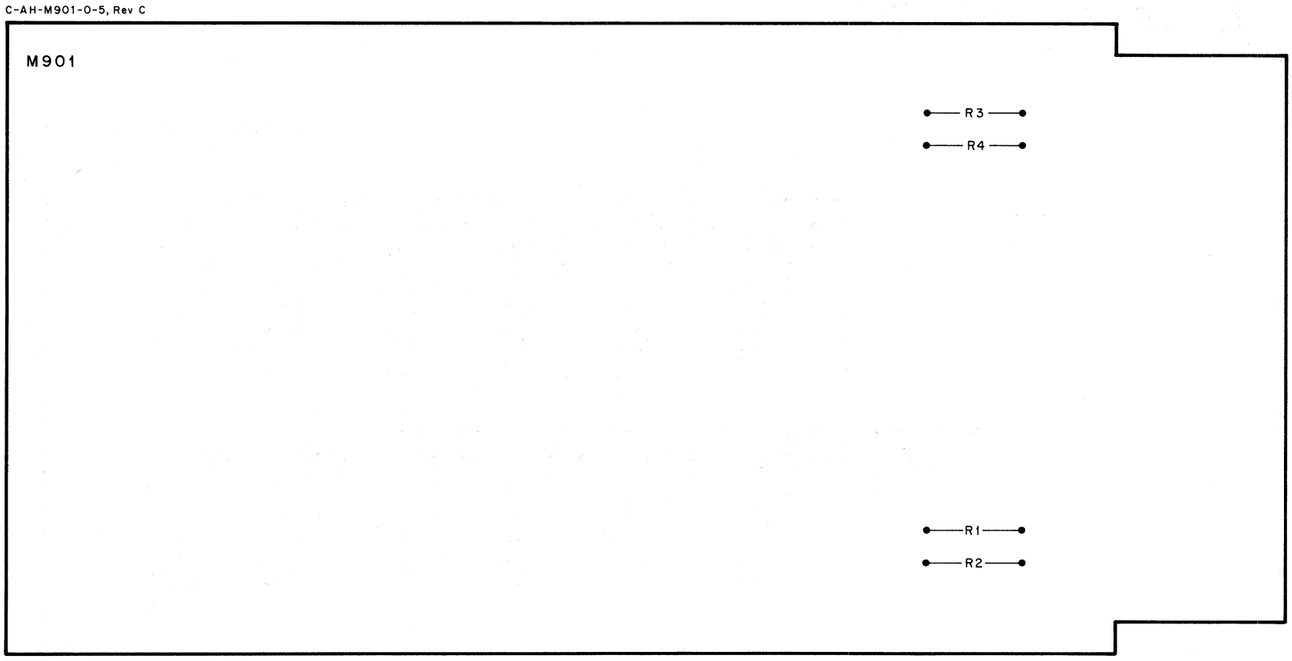
PRINTED CIRCUIT REV. B C

DIST. 324 434 433

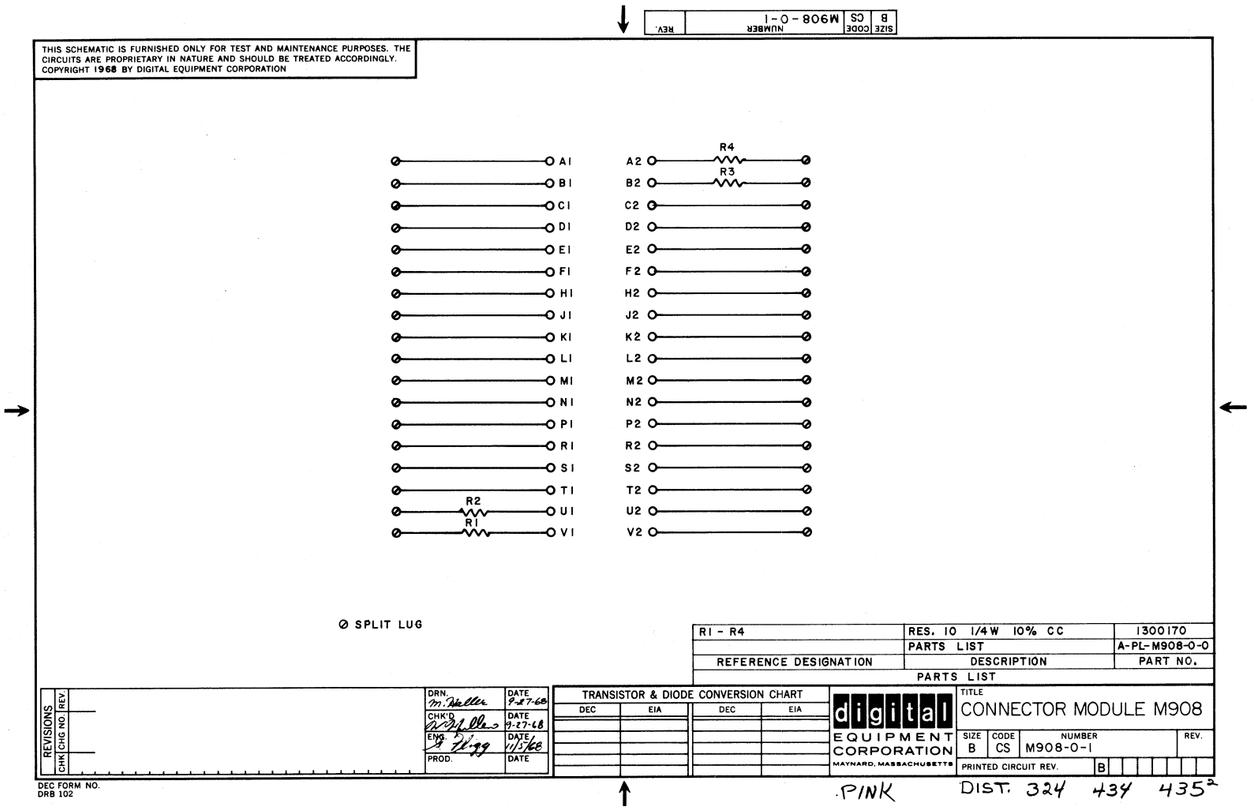
PINK

DEC FORM NO. DRB 102

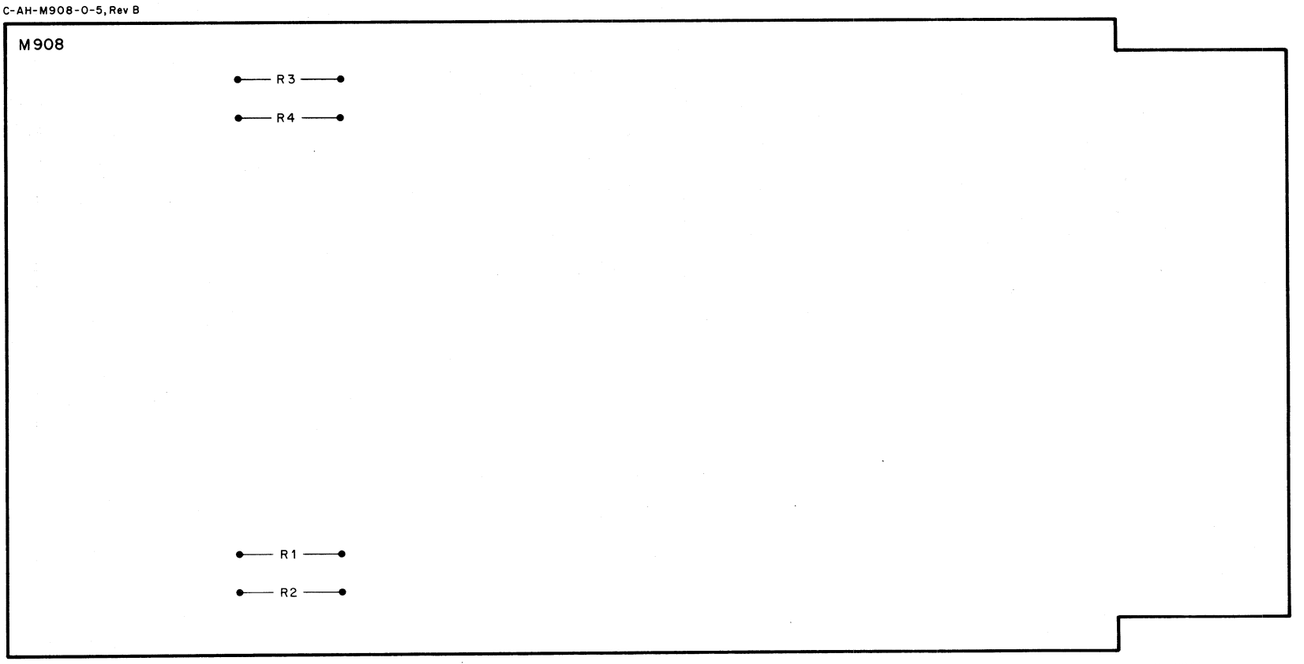
C-AH-M901-0-5, Rev C



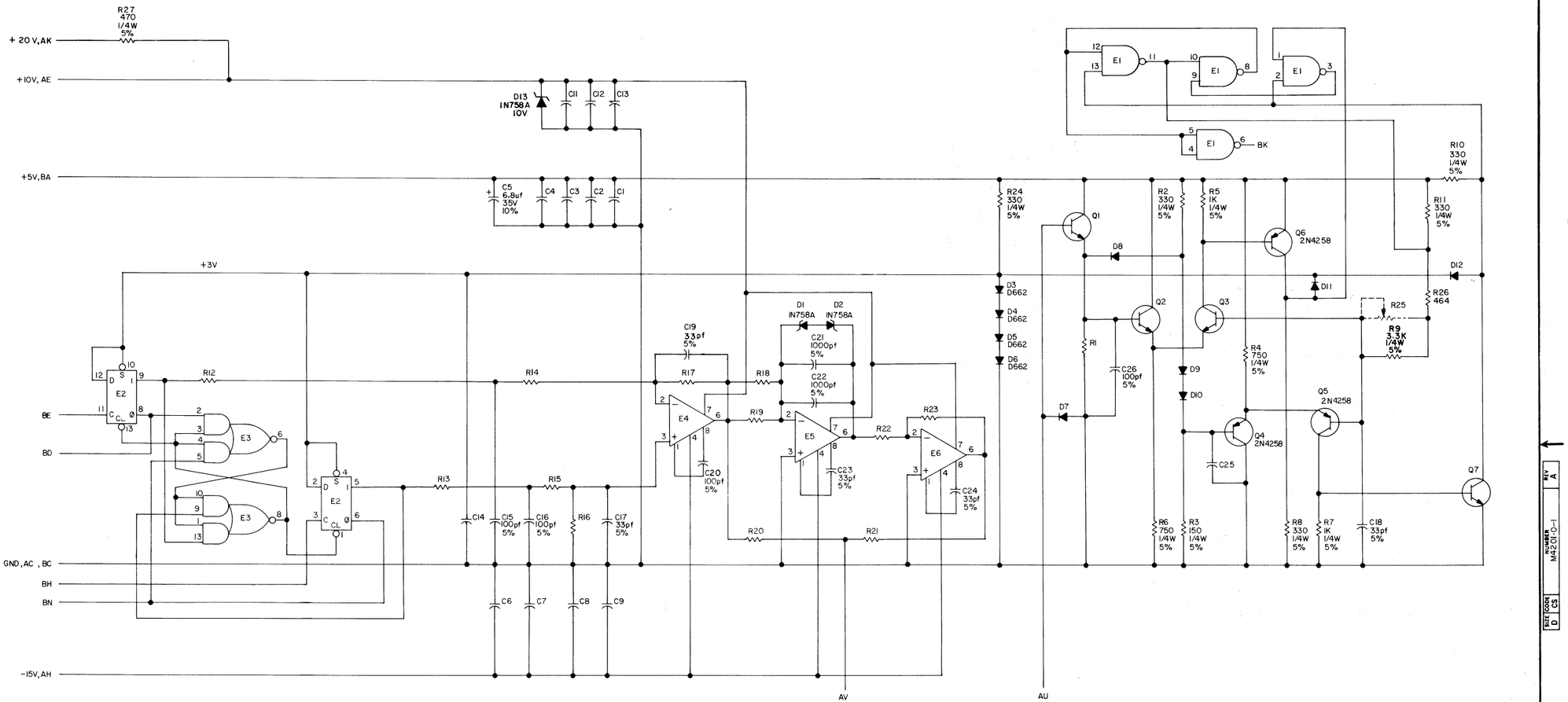
CP-0040



C-AH-M908-0-5, Rev B



CP-0043



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 10K, 1/8W, 1%, MF
CAPACITORS ARE .01uf, 100V, 20%
DIODES ARE D664
TRANSISTORS ARE 2N4274
R25 IS A CUSTOMER OPTION
E1 IS DEC74H00
E2 IS DEC74H74
E4–E6 ARE DEC301
PIN 7 = GND ON E1, E2, E3
PIN 14 = +5V
E3 IS DEC74H50

REVISIONS	CHG NO	REV
	00001	A

DRN: S. Cooper 1/12/71
CHK'D: Graham 1/14/71
ENG: [illegible] 1.21.71
PROD: DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
DEC4274	2N4274	D662	IN645
D664	N13606	IN758A	SAME
DEC4258	2N4258		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

TITLE: PHASE LOCK CLOCK M4201

SIZE	CODE	NUMBER	REV
D	CS	M4201-0-1	A

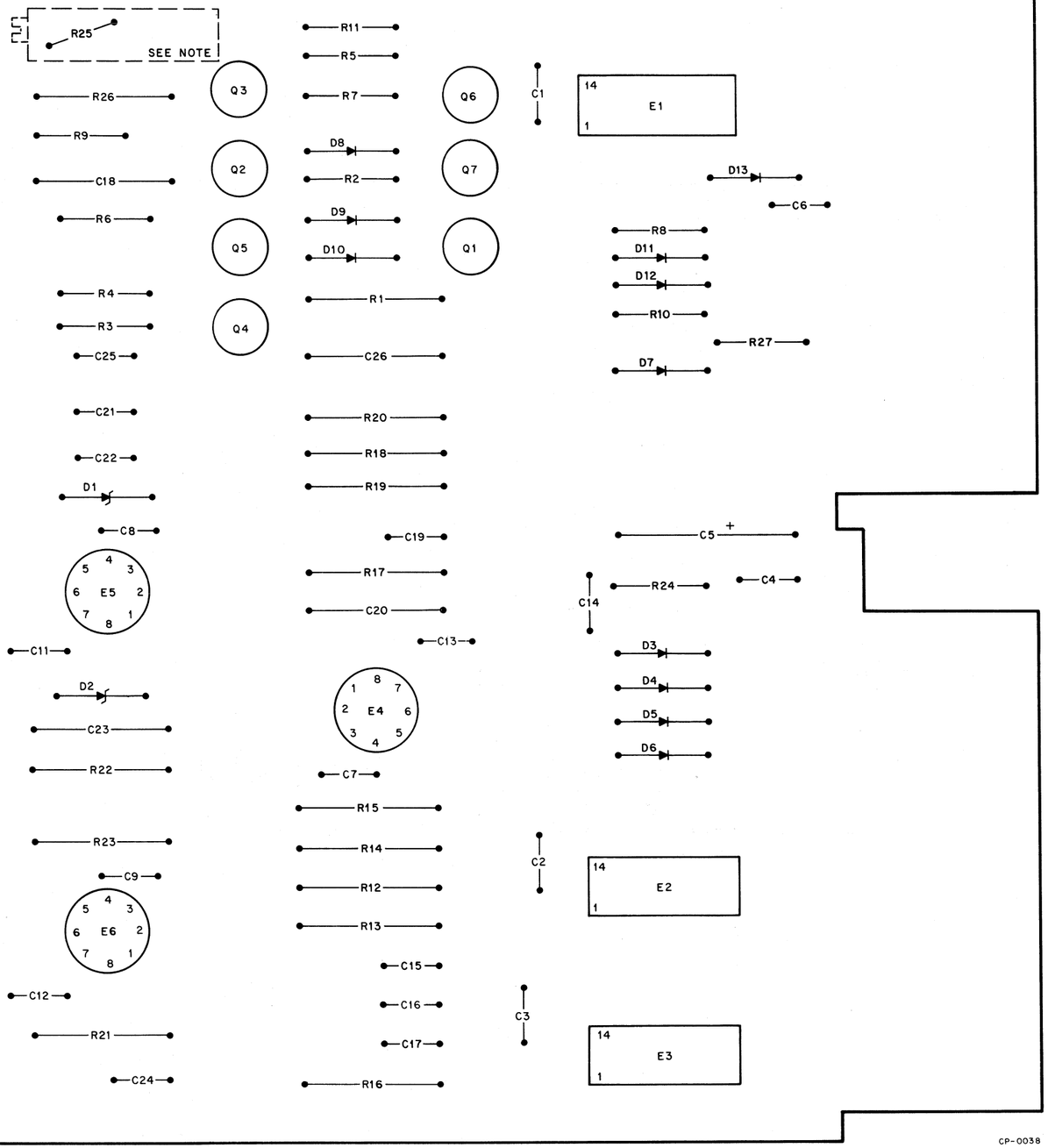
PRINTED CIRCUIT REV. B

DEC FORM NO. BBD 116

MS 1219

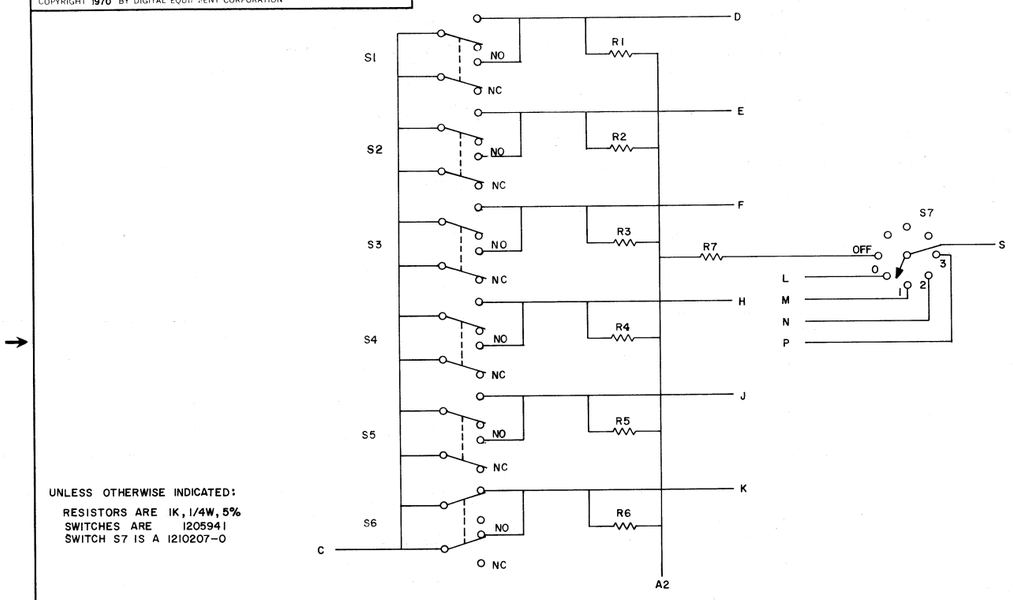
DIST: 324,434,455 2
4 Pink

M4201



NOTE:
R25 IS ENG'S OPTION

SIZE	CODE	NUMBER	REV
B	CS	5408998-0-1	A



UNLESS OTHERWISE INDICATED:

RESISTORS ARE 1K, 1/4W, 5%
SWITCHES ARE 1205941
SWITCH S7 IS A 1210207-0

REVISIONS	REV.	CHK CHG NO

DRN	George Wyatt	DATE 1-11-71
CHK'D	Driscoll	DATE 1/19/71
ENG	Anderson	DATE 1/19/71
PROD		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

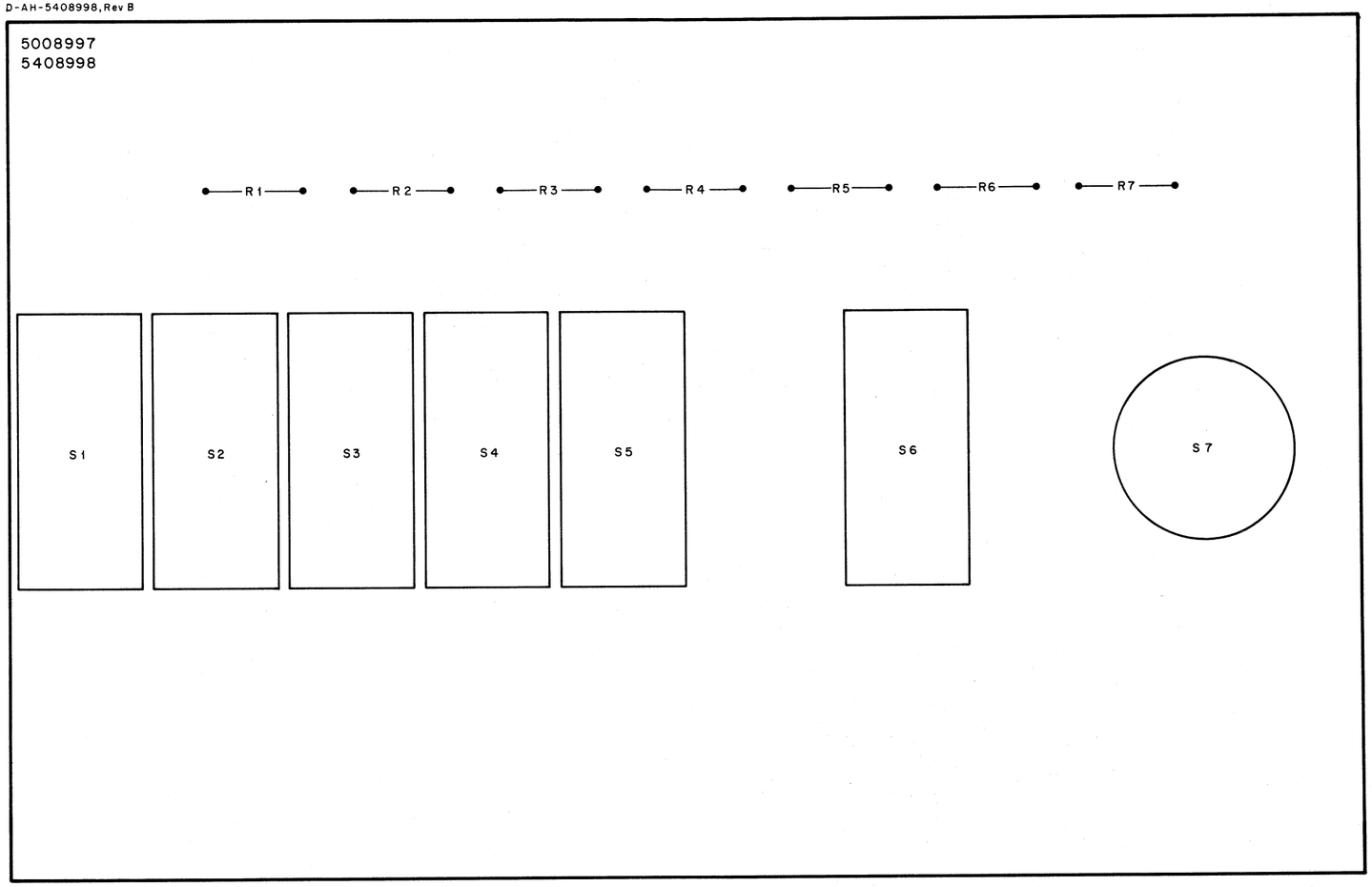
TITLE RS64 DISC SELECT

SIZE	CODE	NUMBER	REV.
B	CS	5408998-0-1	A

PRINTED CIRCUIT REV. B

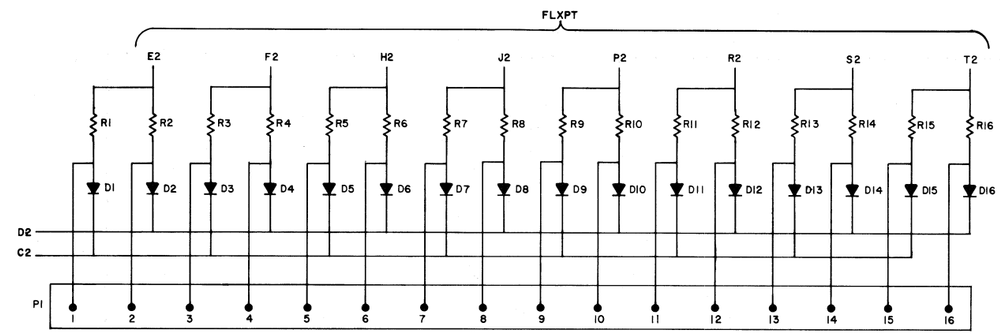
DEC FORM NO. DRB 102

D-AH-5408998, Rev B



CP-0051

SIZE	CODE	NUMBER	REV.
B	CS	5408996-0-1	



UNLESS OTHERWISE INDICATED:

RESISTORS ARE 750, 1W, 1%, MF
DIODES ARE D672
P1 IS A CONNECTOR PLATE 16 PINS MALE

REVISIONS | CHN | CHG NO. | REV.

		DATE
DRN.	E. Silvestro	10/20/70
CHK'D	M. Weller	10/28/70
ENG.		11/10/70
PROD.		DATE

DEC FORM NO. DRB 102

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA
D672	1N3653		

digital EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

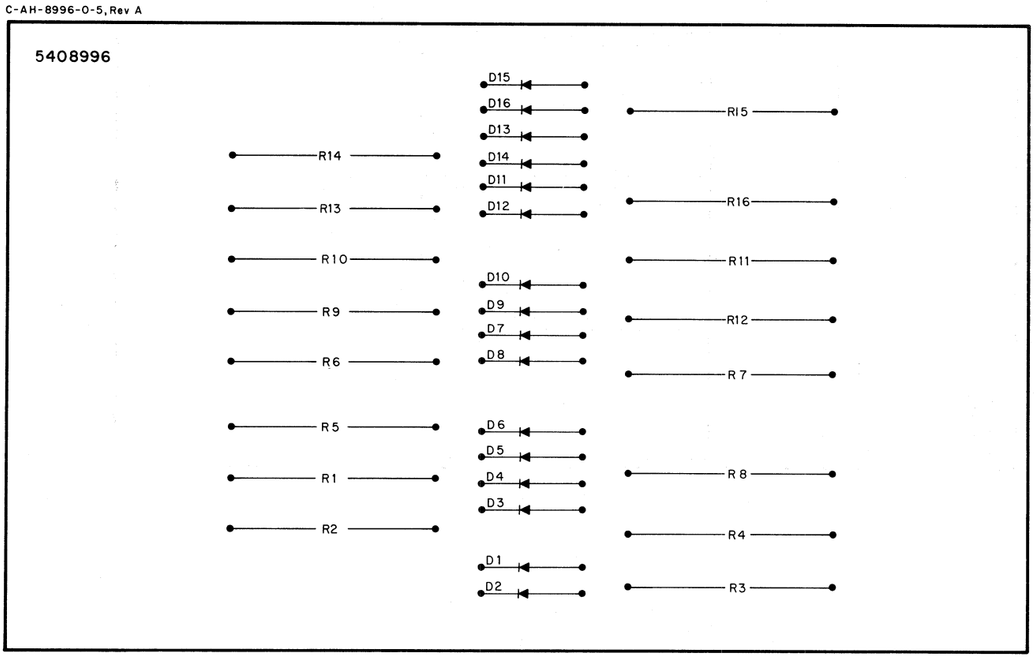
TITLE: 8 TRACK MATRIX 5408996

SIZE	CODE	NUMBER	REV.
B	CS	5408996-0-1	

PRINTED CIRCUIT REV. A

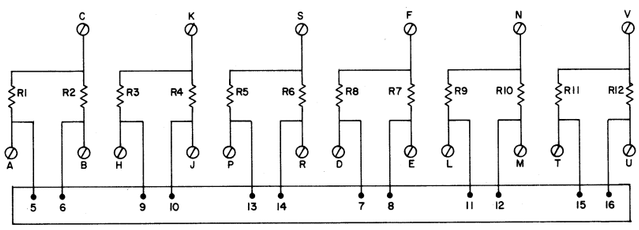
4 Print DIST. 324,434,435 2

C-AH-8996-0-5, Rev A



CP-0049

SIZE	CODE	NUMBER	REV
B	CS	5408937-0-1	C



UNLESS OTHERWISE INDICATED:
RESISTORS = 750, 1W, 1% MF
Ⓘ = SPLIT LUGS
CONNECTOR IS 1210159-0-0

REVISIONS	CHK	CHG NO.	REV.

DRN.	NANCY MOORE	DATE 11/9/70
CHK'D.	M. Miller	DATE 11/24/70
ENG.		DATE 3/8/71
PROD.		DATE

TRANSISTOR & DIODE CONVERSION CHART

DEC	EIA	DEC	EIA

digital
EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE RS64 TIMING TRACK HEAD MATRIX 5408937

SIZE	CODE	NUMBER	REV.
B	CS	5408937-0-1	C

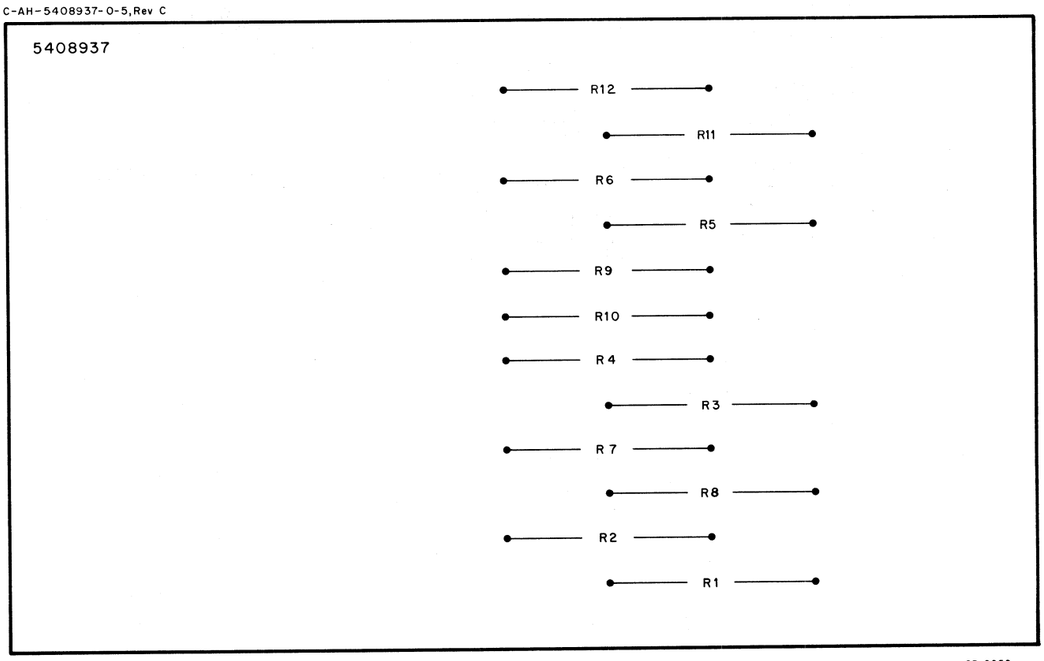
PRINTED CIRCUIT REV. C

DEC FORM NO. DRB 102

DIST. 324,434,455 2

4 PINK

C-AH-5408937-0-5, Rev C

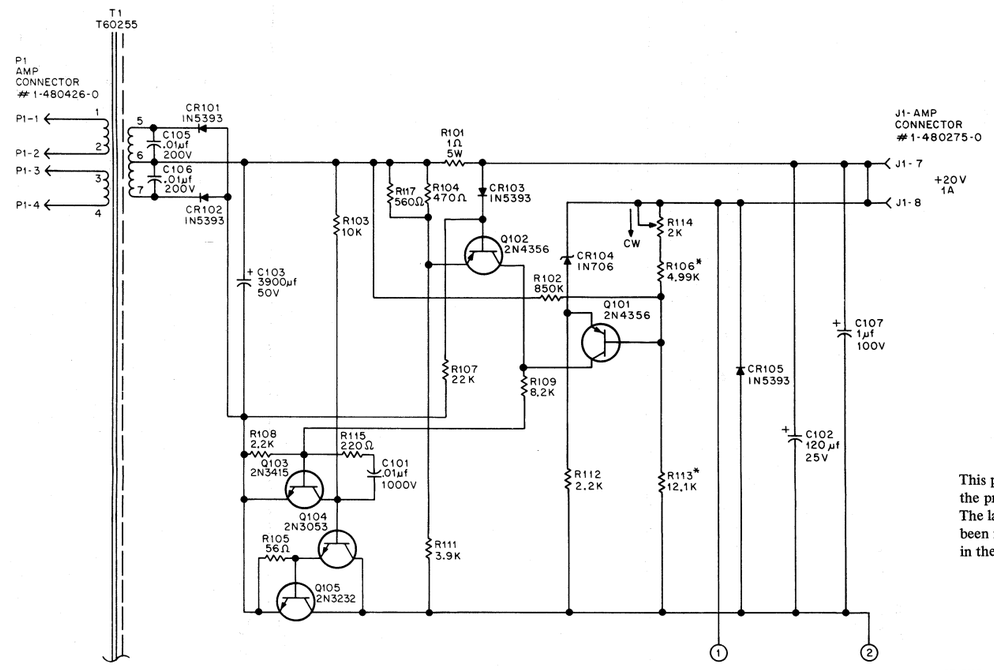


CP-0050

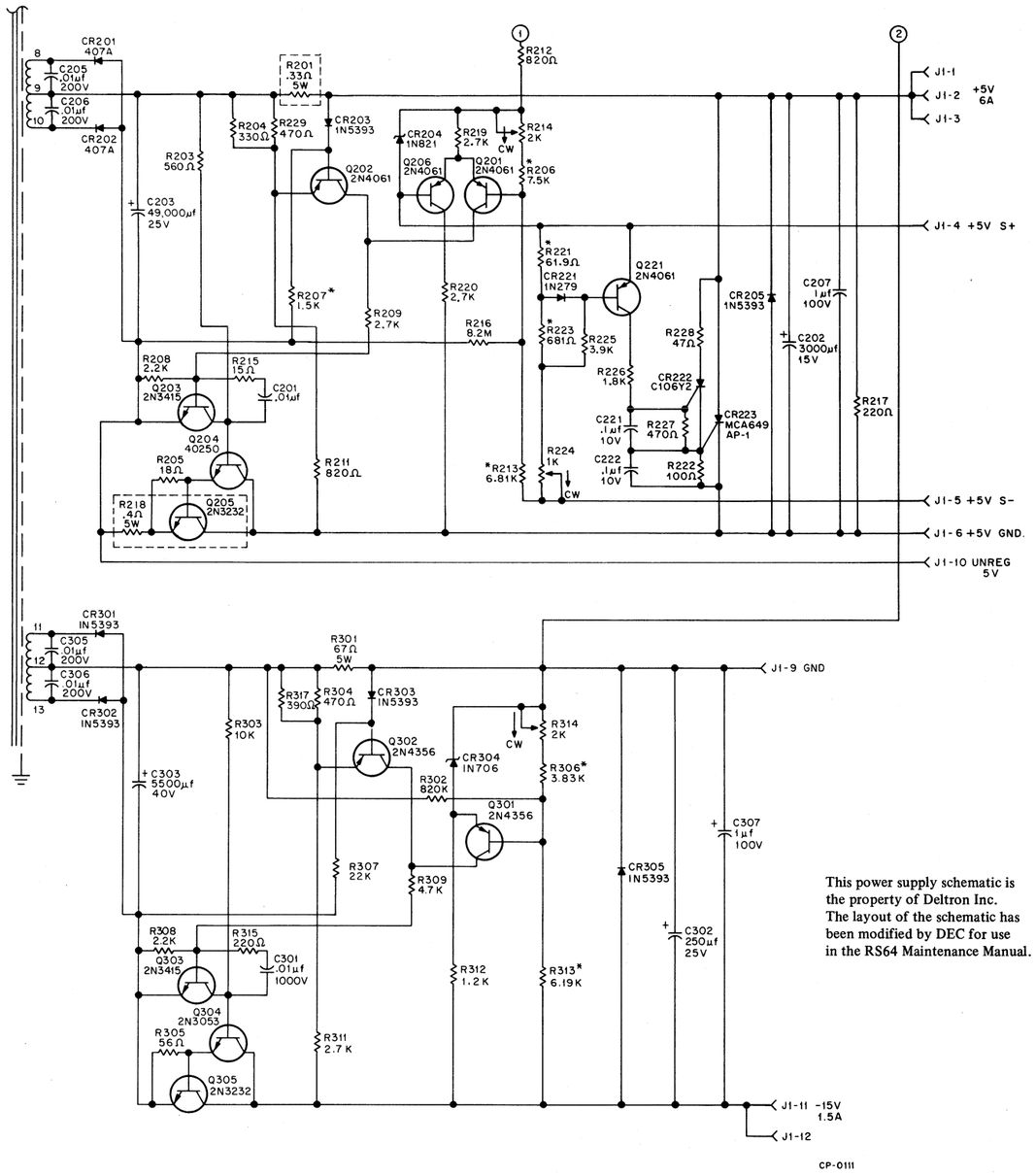
NOTES:

1. Resistor wattage .5 watt unless otherwise indicated.
2. All potentiometers are wirewound.
3. Resistors above 2 watts are wirewound.
4. Resistor tolerance ±10% unless otherwise indicated.
5. Items within dotted areas are wired in parallel.

*6. Denotes 1% film resistors.



This power supply schematic is the property of Deltron Inc. The layout of the schematic has been modified by DEC for use in the RS64 Maintenance Manual.



This power supply schematic is the property of Deltron Inc. The layout of the schematic has been modified by DEC for use in the RS64 Maintenance Manual.

APPENDIX A
RC11 FORMAT AND RS64 TIMING TRACK WRITER

A.1 RC11 FORMAT

A.1.1 Data Organization

Data is organized in block format on the disk as follows:

a. 32 data tracks per disk

b. 64 data blocks per track

c. 32 data words per block

With this arrangement, the storage capacity of the disk is 65,536 16-bit words.

A.1.2 Disk Timing Tracks

There are six prerecorded timing tracks (3 timing tracks are spares) on the disk. The timing tracks (designated A, B, and C) are used as follows:

a. TTA – Clock timing track

b. TTB – Address and data sector marker track

c. TTC – Sector address code track

A.1.3 Addressing Data on Disk

The following parameters are used for addressing disk content:

a. A 2-bit code selects any one of four disk files assigned a corresponding unit number.

b. A 5-bit track select code addresses any one of the 32 data tracks.

c. A 6-bit address code on the prerecorded address track (TTC) defines 64 data blocks.

d. An address code on TTC and the data block for this address is designated a sector.

A.1.4 Address and Data Demarkation

The address and data marker track (TTB) is prerecorded with address and data markers that identify the beginning of an address on TTC or data on one of the data tracks. These markers are logical ones recorded at appropriate places on TTB as shown in Figure A-1. Address and data markers are distinguishable by the polarity of the induced signal.

A.1.5 Controller Clocking

With the exception of the origin gap, the A timing track contains a continuous stream of clock pulses as shown in Figure A-1. All controller major events are derived from the master clock signals recovered from this track.

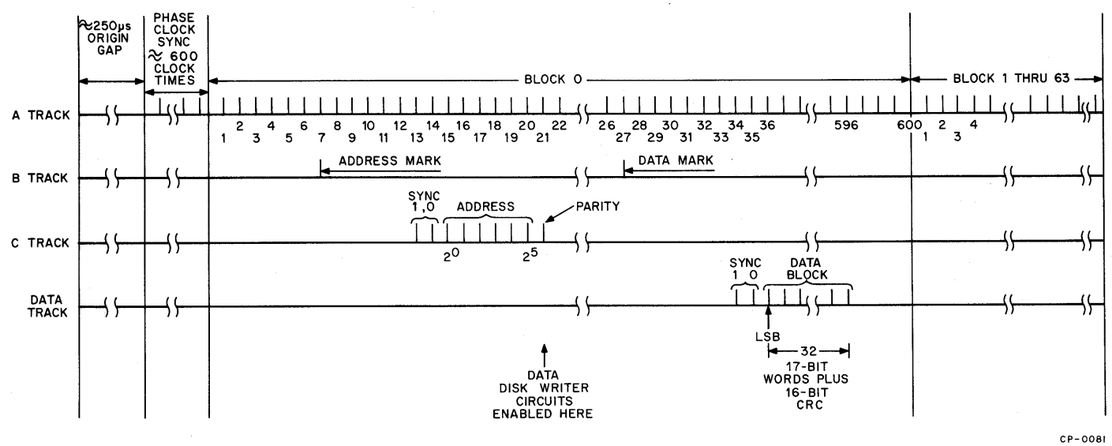


Figure A-1 RC11 Format

All address codes and data blocks are written with a 2-bit synchronizing preamble consisting of a logical one followed by a logical zero. The synchronizing preamble enables self-clocking of address and data to eliminate inherent skew between tracks.

A.1.6 Disk Track Format

For control purposes, the disk surface is divided into 65 equal blocks plus an origin gap (Figure A-1). Each block consists of a segment of 600 TTA pulses. Data can be recorded in all blocks except the block immediately following the origin gap. This block is used for synchronizing the RS64 phase-locked clock with TTA pulses.

An address marker is recorded on TTB the seventh clock time of each data block. The sector address on TTC begins at the 13th clock time of each block. The first two bits are the synchronizing preamble. The 6-bit address begins at the 15th clock time and is recorded with the LSB first. A parity bit follows the MSB.

A data marker is recorded on TTB the 27th clock time of each data block and data begins on the 34th clock pulse. The first two clock times are allotted for the synchronizing preamble. The last word in a block is a block parity word and ends on the 596th clock pulse.

As denoted in Figure A-1, the disk write circuits are enabled at the 21st clock time. This action ensures that logical zeros are written on the data track shortly before and after sensing the data mark. This action prevents any spurious transitions appearing in that area of the data track from creating a false sync pattern.

A.2 RS64 TIMING TRACK WRITER

The RS64 timing track writer records timing tracks A (clock), B (address and data marks), and C (address) on an RS64 Disk. Three spare timing tracks are written at the same time.

To write the timing tracks, the RS64 timing cable assembly is disconnected at the logic assembly and is connected to the timing track writer outputs shown in Figure A-2. A track writer cycle begins when the PUSH-TO-WRITE switch is depressed. As a result of this action, the track writer erases the timing tracks by writing zeros for at least 50 ms. Following this action, the track writer starts writing timing track A (TTA) and TTA Spare. These tracks establish the bit cell or basic clock timing for the disk as shown in Figure A-1.

After writing one block of 600 clock pulses for TTA (this block is allotted for disk clock resynchronization), the track writer begins recording address and data sector marks on TTB, consecutive addresses on TTC, and continues the recording of clock pulses on TTA. Figure A-1 shows the location of address and data marks within a block and the arrangement of address bits on TTC.

The track writer continues writing of TTA, TTB, and TTC until 64 600-bit blocks (and one 600-bit block for clock synchronization) have been written. Upon sensing that 65 equal length blocks have been recorded, the track writer concurrently disables the TTA, TTB, and TTC disk writers and triggers its gap detection circuits to signify the start of an origin gap. The track writer determines gap length by using the first TTA clock pulse after the gap to reset the detection circuits. An incorrect gap is corrected by adjusting the frequency of the clock and rewriting the timing tracks.

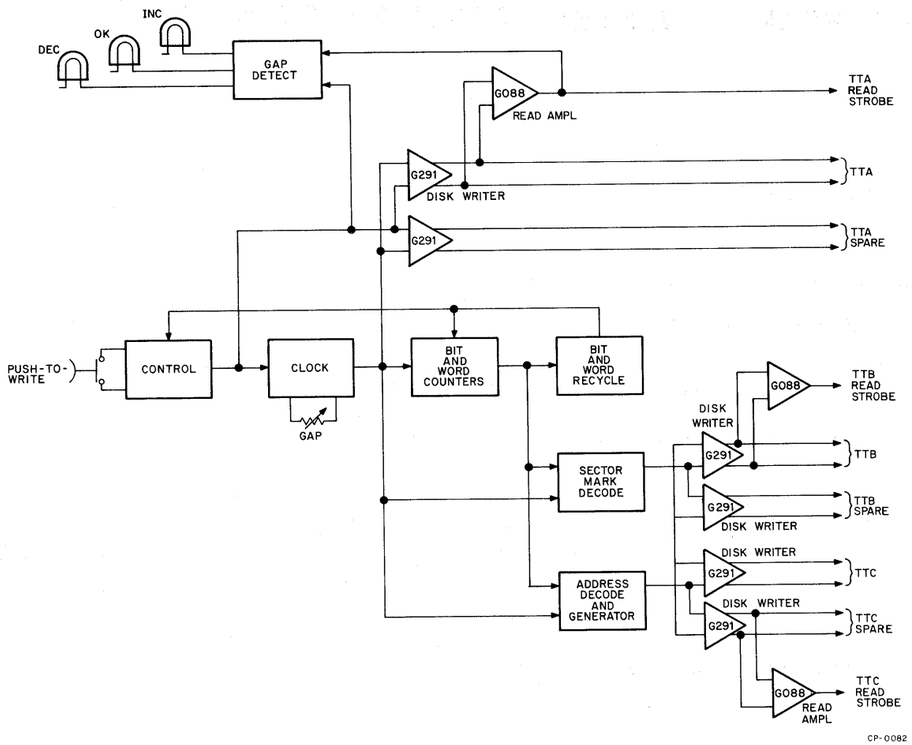


Figure A-2 Timing Track Writer Block Diagram

APPENDIX B
POWER SUPPLY

The power supply produces regulated +5V, -15V, and +20V operating potentials for the RS64 Disk File. The +5V supply can also provide the operating potentials for an external logic load (for example, a controller) of up to 4.5 A.

The power supply, Figure B-1, can be operated from a 115V or 230V source by changing the connections of the power transformer windings. Input power ranges are:

100 to 135 Vac, 47 to 63 Hz
200 to 250 Vac, 47 to 63 Hz

Load current rating for the three supplies is as follows:

+5 Vdc at 6A
+20 Vdc at 1A
-15 Vdc at 1.5A

The outputs are regulated to within the voltage bands specified below with full input voltage and frequency variations and from zero to full load current:

Output	Regulation
+5V	+5 ±0.15 Vdc
+20V	+20 ±2 Vdc
-15V	-15 ±1 Vdc

Other features are:

a. All supplies are adjustable.

b. All supplies are short-circuit proof.

c. The +5 Vdc supply provides overvoltage protection for logic. Maximum overvoltage trip point is +6 Vdc.

d. Remote sensing lead provided for +5 Vdc supply.

READER'S COMMENTS

RS64 DISK FILE
MAINTENANCE MANUAL
DEC-00-RS64-DA

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications.

What is your general reaction to this manual? In your judgement is it complete, accurate, well organized, well written, etc.? Is it easy to use? _____

_____

_____

_____

What features are most useful? _____

_____

_____

What faults do you find with the manual? _____

_____

_____

Does this manual satisfy the need you think it was intended to satisfy? _____
Does it satisfy *your* needs? _____ Why? _____

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Would you please indicate any factual errors you have found. _____

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