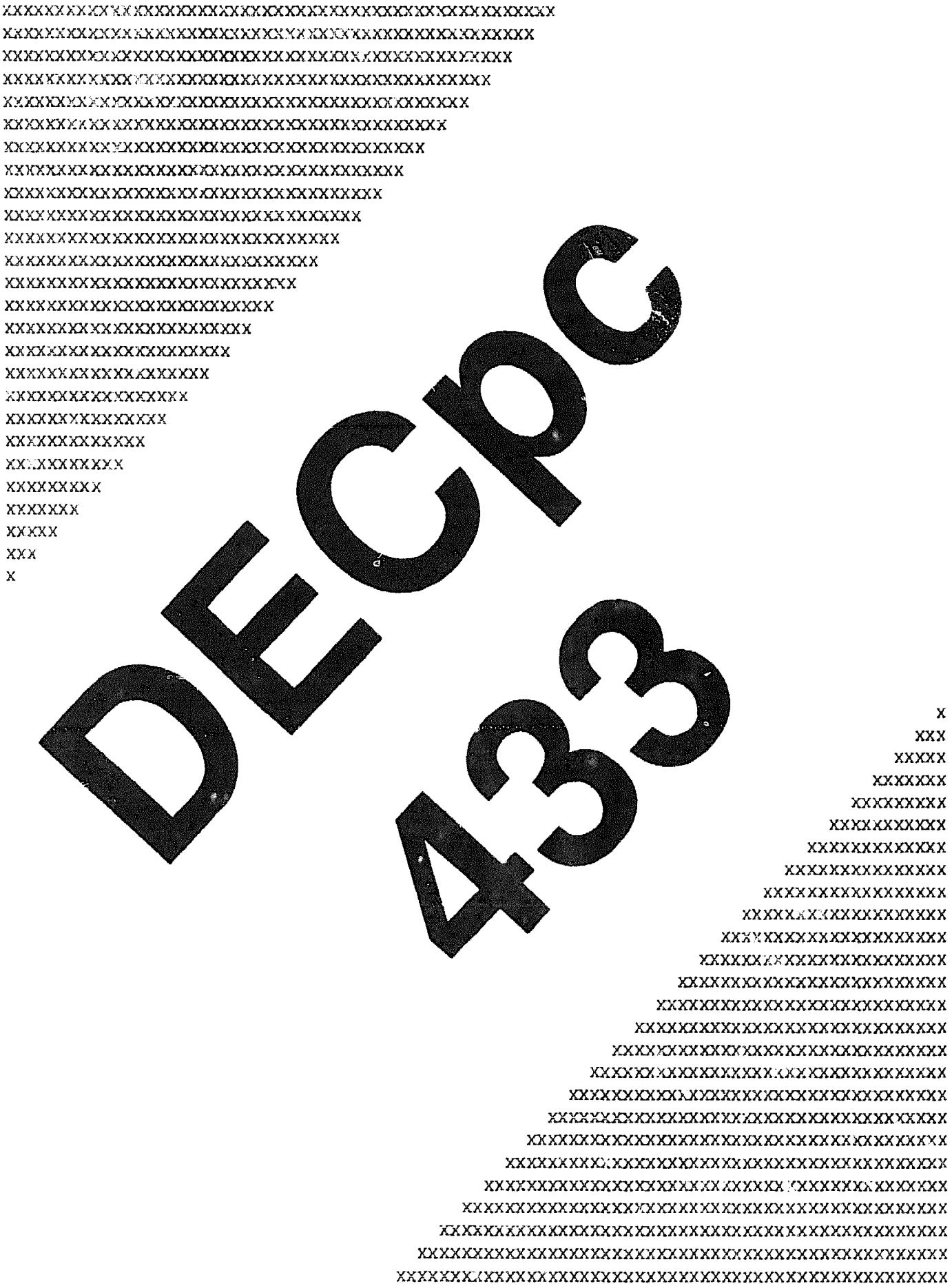
DECpc
433

DECpc™ 433 Workstation

Technical Reference Manual

Order Number ER-PCW1A-TR

Digital Equipment Corporation

December 1991

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About This Manual

Purpose

The purpose of this manual is to provide a comprehensive hardware description of the major components in the DECpc Workstations. Descriptions include:

- System architecture
- Buses
- Interfaces
- System specifications
- Basic input/output system (BIOS) specifications
- Configuration options.

Audience

This manual is written specifically for a system engineer or hardware designer familiar with the fundamental concepts of microprocessor-based systems. It also assumes a familiarity with the general terminology used in the field of microprocessor design. In addition, this manual contains information for engineers who design system accessories and for programmers who require hardware and firmware specifications.

Organization of This Document

This manual contains 11 chapters and three appendices, as follows:

Chapter 1	System Board Overview — describes the major features of the DECpc Workstation system board.
Chapter 2	Central Processing Core — describes the Intel486 microprocessor, the optional 64 KB or 128 KB external cache, and the Corona Application Specific Integrated Circuit (ASIC).
Chapter 3	Memory — describes system board dynamic random access memory (DRAM) and the operation of the memory controller section of the 82346 system controller.
Chapter 4	82340DX ISA Chip Set — describes operation of the 82344 ISA bus controller, the 82345 data buffer, and the 82346 system controller (less memory controller section).
Chapter 5	82341 Peripheral Combo Controller — describes operation of the 82341 peripheral combo controller. Information includes serial and parallel port descriptions, keyboard and mouse interface descriptions, and an integrated drive electronics (IDE) interface description.
Chapter 6	AIC-6260 SCSI Controller — describes operation of the AIC-6260 SCSI controller and provides information about its internal registers.
Chapter 7	Floppy Disk Drive Subsystem — describes operation of the 82077 onboard floppy disk controller and provides information about its internal registers.
Chapter 8	Ethernet LAN Subsystem — describes operation of the Ethernet LAN interface and provides information about internal Ethernet LAN interface registers.
Chapter 9	Token Ring LAN Subsystem — describes operation of the Token Ring LAN interface and provides information about internal Token Ring LAN interface registers.

Chapter 10	Power Supply — describes the system power supply and expansion box power supply input requirements and output specifications.
Chapter 11	Intelligent Graphics Controller — describes operation of the intelligent graphics controller.
Appendix A	Specifications — lists general specifications for the system board and environmental and dimensional specifications for the system module and SCSI expansion box.
Appendix B	BIOS Interrupt Routines — describes the interrupt service routines available in the system's BIOS.
Appendix C	Device Mapping — provides tables that list the system memory map, I/O address map, interrupt map, and LAN memory map. It also includes information about the system DMA users.
Index	Index — includes important terms arranged in alphabetical order for quick reference.

Notational Conventions

Notational conventions used throughout this manual include:

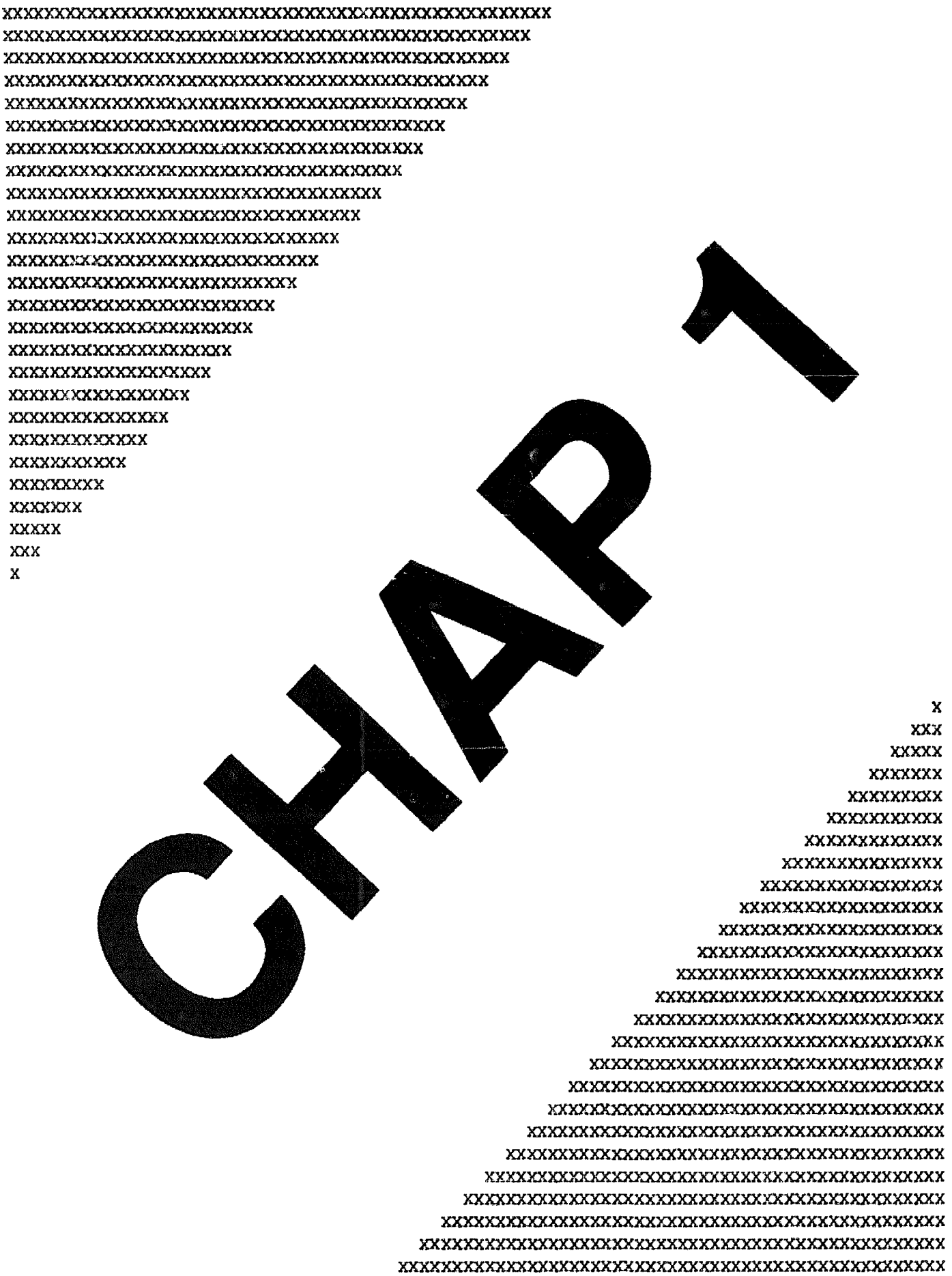
*	In connector pinout listings, the asterisk (*) indicates an active low signal. For example, IOCHCK*
H	An H suffix to a numerical value denotes hexadecimal numbers. For example, 0F8H equals 0F8 (hexadecimal).
Kb	A Kb suffix to a numerical value indicates size in kilobits. For example, 512 Kb. A kilobit equals 1024 bits.
KB	A KB suffix to a numerical value indicates size in kilobytes. For example, 640 KB, 7168 KB, etc. A kilobyte equals 1024 bytes.
Mb	An Mb suffix to a numerical value indicates size in megabits. For example, 4 Mb. A megabit equals 1,048,576 bits.
MB	An MB suffix to a numerical value indicates size in megabytes. For example, 1 MB, 256 MB, etc. A megabyte equals 1,048,576 bytes.
GB	A GB suffix to a numerical value indicates size in gigabytes. For example, 1 GB, 256 GB, etc. A gigabyte equals 1,073,741,824 bytes.

An italicized word or phrase is used to represent a variable or to lend emphasis in textual descriptions. File names, path names, and directories are also italicized.

Related Documentation

The following related documents are available as supplements to the information provided in this manual.

Document	Part Number
DECpc 433 Ethernet Workstation User's Guide	ER-PCW10-UG
DECpc 433 Token Ring Workstation User's Guide	ER-PCW11-UG
DECpc 433 Workstation Service Manual	ER-PCW10-SV-002
DECpc SCSI Expansion Box Installation Guide	ER-PCWXE-IG
MS-DOS Supplemental Kit Installation Guide	PCWXQ-XA
OS/2 Supplemental Kit Installation Guide	PCWXQ-XB


CHAP 1

1

System Board Overview

Introduction

This chapter provides an overview of the two available DECpc 433 Workstation system boards: Ethernet system board PCP10-A2 and Token Ring system board PCP11-A2 (see Figures 1-1 and 1-2). Each board supports:

- A high performance Intel486™ microprocessor
- An optional external cache (Intel TurboCache486™)
- An Intel 82340DX™ Industry Standard Architecture (ISA) chip set
- Corona and SCSI Application Specific Integrated Circuits (ASICs)
- Local Area Network (LAN) support circuitry for either Ethernet™ or Token Ring™
- A peripheral combo controller
- An onboard floppy disk controller
- Integrated Disk Electronics (IDE) support
- 80 ns (or faster) fast-paged Dynamic Random Access Memory (DRAM)
- 128 KB of Read-only Memory (ROM)

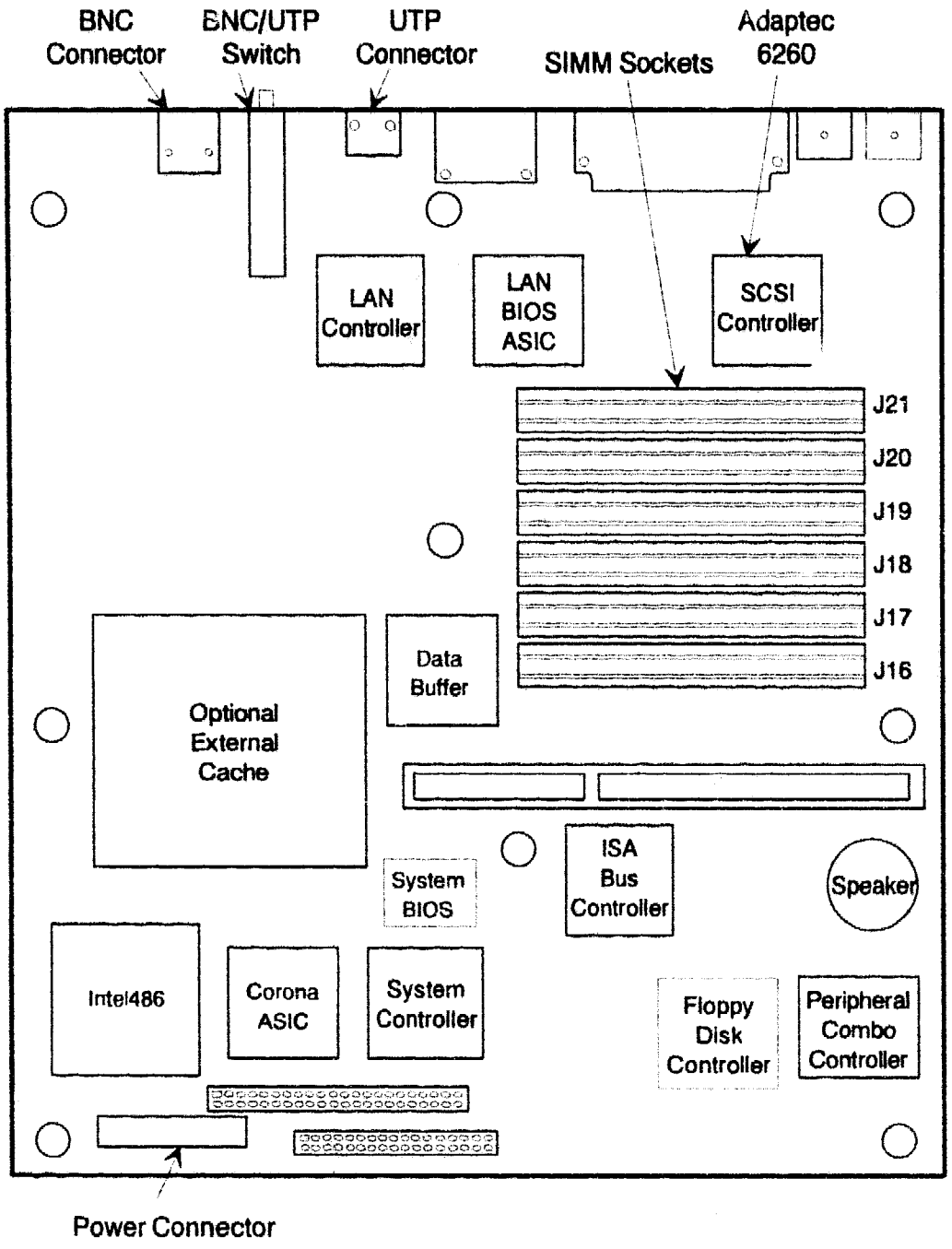


Figure 1-1. DECpc 433 Ethernet Workstation System Board Layout

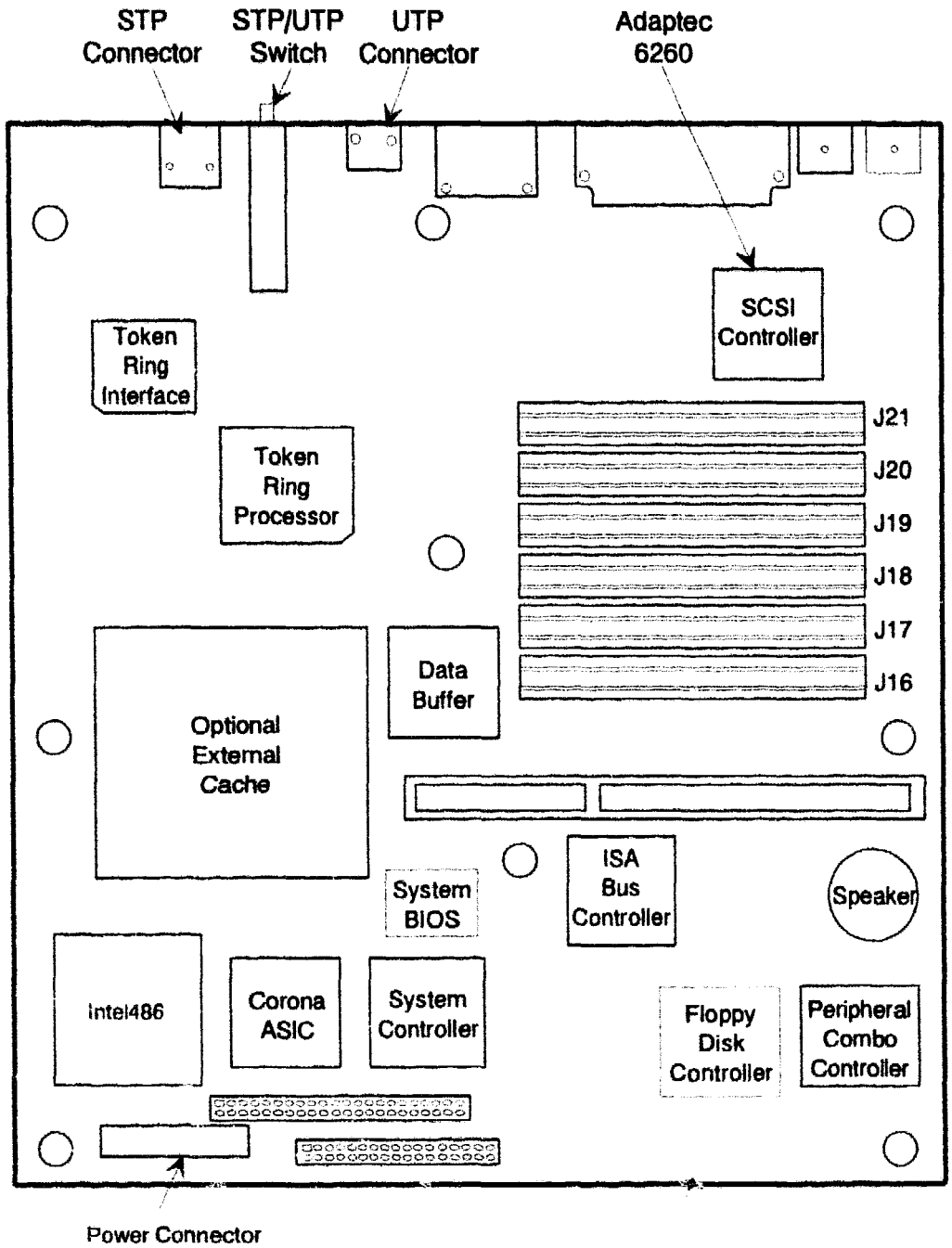


Figure 1-2. DECpc 433 Token Ring Workstation System Board Layout

In addition, the system boards support:

- One 16-bit ISA expansion slot (dedicated to the intelligent graphics controller)
- Two 9-pin serial ports
- One 25-pin parallel port
- One 50-pin SCSI connector
- One 34-pin floppy disk controller header
- One IDE header
- ThinWire™ and Twisted Pair Ethernet LAN connectors or Shielded Twisted Pair and Unshielded Twisted Pair Token Ring LAN connectors
- 6-pin (mini-DIN) keyboard and mouse connectors
- Four system status LED indicators
- One 105 watt power supply

The remainder of this chapter provides a brief description of the hardware components and major features for each system board.

DECpc 433 Workstation System Board Features

This section provides detailed descriptions relating to the hardware components and major features of each DECpc 433 Workstation system board (see Figure 1-3).

Intel486 Microprocessor

The Intel486 microprocessor provides multi-tasking support, on-chip memory management, on-chip floating point unit, on-chip cache memory with a 106 MB/sec burst bus, and a high-speed 32-bit bus interface. The Intel486 microprocessor runs at a clock speed of 33 MHz, which results in a system speed of 30 ns per clock cycle. For applications requiring slower operation (such as installing copy-protected software), a slow mode is provided. The slow mode reduces the effective Intel486 microprocessor operating speed to that of an Intel286 running at 8 MHz.

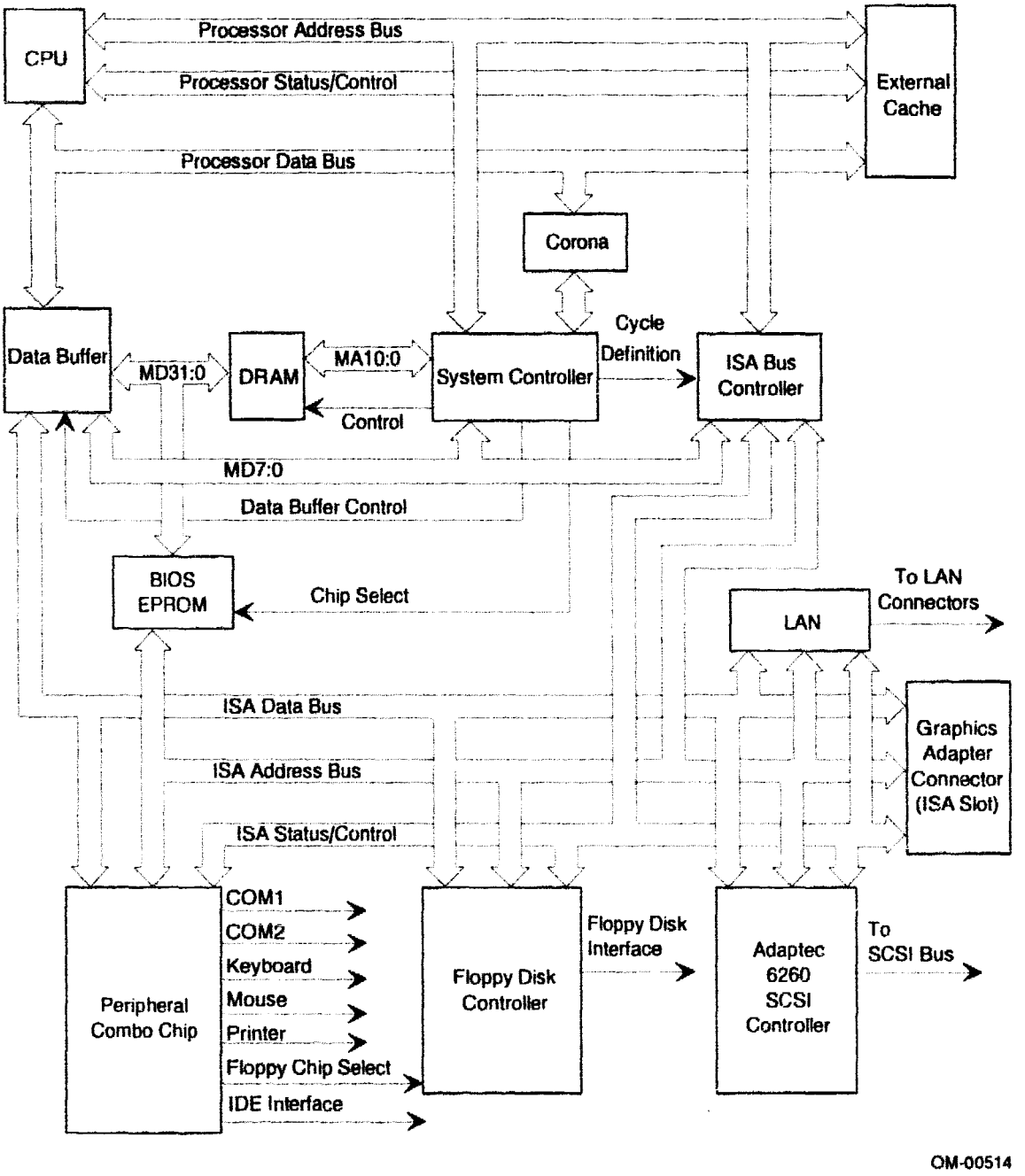


Figure 1-3. DECpc 433 Workstation Block Diagram

External Cache

The system board provides a 113-pin socket for an optional 64 KB or 128 KB external cache. The external cache is a high-performance cache subsystem designed for the Intel486 microprocessor. The external cache increases system performance by reducing the average number of wait states seen by the Intel486 microprocessor.

Corona

The Corona ASIC generates clocks for the Intel486 microprocessor, the 82346 system controller, external cache, LAN controller, and AIC-6260 SCSI controller. Corona also arbitrates and controls bus functions for accesses initiated by the Intel486 microprocessor, converts Intel486 microprocessor bus control signals to Intel386™ bus control signals (required by the system controller), and provides address decoding for the LAN and SCSI controllers.

82340DX ISA Bus Chip Set

The 82340DX chip set consists of an 82344 ISA bus controller, an 82345 data buffer, and an 82346 system controller. Together, these components are responsible for controlling all addressing and data transmissions to and from the ISA bus.

DRAM

The system board contains three Single In-line Memory Module (SIMM) banks. Each bank holds four SIMMs. The SIMM size can be either 1 MB or 4 MB. The base system DRAM configuration is 8 MB. The maximum system DRAM configuration is 48 MB.

ROM

The system board ROM is one 128 KB EPROM. The EPROM contains the system BIOS, a Power-On Self Test (POST), and the Setup Utility. The BIOS initializes the DRAM and loads the operating system. The system BIOS also contains a shadow option. This option, when enabled, increases system performance by placing ROM instructions into high-speed DRAM. POST tests system hardware and the Setup utility allows you to set system configuration parameters.

82077 Floppy Disk Drive Controller

An 82077 floppy disk drive controller provides the data interface between the floppy disk drive and the Intel486 microprocessor. The data interface consists of an 8-bit bidirectional data bus and eight general purpose registers.

82341 Peripheral Combo Controller

The 82341 peripheral combo controller provides the interface between the ISA bus and the serial ports, keyboard and mouse, parallel port, and IDE controller.

AIC-6260 SCSI Controller

The Adaptec AIC-6260 is a single-chip ISA bus-to-SCSI bus controller that supports second path DMA transfers and I/O.

LAN Support Circuitry

The LAN support circuitry provides external network interface. The system is provided either with an Ethernet LAN (DECpc 433 Ethernet Workstation) or with a Token Ring LAN (DECpc 433 Token Ring Workstation). A pushbutton switch selects the cable type in use: ThinWire or Twisted Pair for Ethernet; Shielded Twisted Pair or Unshielded Twisted Pair for Token Ring.

I/O Ports

There are three I/O ports: one 25-pin parallel printer port and two 9-pin serial communication ports.

System Status LED Indicators

The DECpc 433 Workstation system provides four system status LED indicators. When on, they indicate LAN activity, disk drive access, SCSI activity, and applied system power.


CHAP 2

2

Central Processing Core

Introduction

This chapter describes the processing core of the DECpc 433 Workstation. The processing core provides the major system processing resources and includes the following major functional blocks:

- Intel486 microprocessor
- Optional external cache
- Corona ASIC

Intel486 Microprocessor

The Intel486 microprocessor is a high-performance 32-bit microprocessor with an on-chip memory management unit, numeric coprocessor unit, and cache memory unit. The Intel486 microprocessor supports multiuser and multi-tasking operating systems, memory management, virtual memory, and task or memory isolation. The following text describes the Intel486 microprocessor's basic architecture and the two modes of operation. This section concludes with brief descriptions relating to the signals generated by the Intel486 microprocessor.

Basic Architecture

The Intel486 microprocessor is divided into four major sections:

- Central processing unit
- Memory management unit
- Numeric coprocessor unit
- Cache memory unit

Central Processing Unit

The central processing unit (CPU) consists of the execution unit and instruction unit. The execution unit contains the eight 32-bit general purpose registers used for both address calculation and data operations. The execution unit also contains a 64-bit barrel shifter that speeds up shift, rotate, multiply, and divide operations. The instruction unit decodes the instruction opcodes and stores them in the decoded instruction queue for immediate use by the execution unit.

Memory Management Unit

The memory management unit (MMU) consists of a segmentation unit and a paging unit. Segmentation manages the logical address space by providing an extra addressing component that allows the relocation and sharing of code and data. The paging unit operates beneath, and is transparent to, the segmentation process to allow physical address space management. Paging is optional and is under system software control.

Numeric Coprocessor Unit

The on-chip numeric coprocessor unit conforms to the ANSI/IEEE standard 754-1985 specification, operates in parallel with the arithmetic and logic unit, and provides arithmetic instructions for a variety of numeric data types. The numeric coprocessor unit executes built-in tangent, sine, cosine, and log functions and is compatible with software written for 287 and 387DX numeric coprocessors.

Cache Memory Unit

The 8 KB on-chip cache memory unit is 4-way set-associative and follows a write-through policy. It can designate individual pages as cacheable or non-cacheable by hardware or software.

Modes of Operation

The Intel486 microprocessor has two modes of operation: real address mode (real mode) and protected mode. In real mode, the Intel486 microprocessor operates as a fast 8086™ and sets up the CPU for protected mode operation. Protected mode provides access to the sophisticated memory management paging and privilege capabilities of the microprocessor.

In protected mode, software can execute a task switch and enter into a virtual 8086 mode. In this virtual mode 8086 semantics are used and the application program or operating system executes as if running on an 8086 microprocessor.

Signal Definitions

Table 2-1 lists a signal name cross reference for the Intel486 microprocessor and system board. Following Table 2-1 are brief descriptions of each Intel486 microprocessor signal.

Table 2-1. Signal Name Cross Reference

Pin Number	Intel486 Signal Name	System Board Signal Name
P1	D0	PD0
N2	D1	PD1
N1	D2	PD2
H2	D3	PD3
M3	D4	PD4
J2	D5	PD5
L2	D6	PD6
L3	D7	PD7
F2	D8	PD8
D1	D9	PD9
E3	D10	PD10
C1	D11	PD11
G3	D12	PD12
D2	D13	PD13
K3	D14	PD14
F3	D15	PD15
J3	D16	PD16
D3	D17	PD17
C2	D18	PD18
B1	D19	PD19
A1	D20	PD20

Table 2-1. Signal Name Cross Reference *(continued)*

Pin Number	Intel486 Signal Name	System Board Signal Name
B2	D21	PD21
A2	D22	PD22
A4	D23	PD23
A6	D24	PD24
B6	D25	PD25
C7	D26	PD26
C6	D27	PD27
C8	D28	PD28
A8	D29	PD29
C9	D30	PD30
B8	D31	PD31
N3	DP0	PDP0
F1	DP1	PDP1
H3	DP2	PDP2
A5	DP3	PDP3
C3	CLK	PCLK
E15	HOLD	PHOLD
D17	BOFF*	Not used
C17	BS16*	Not used
D16	BS8*	Not used
D15	A20M*	PA20M*
A16	INTR	PINTR

Table 2-1. Signal Name Cross Reference *(continued)*

Pin Number	Intel486 Signal Name	System Board Signal Name
B15	NMI	PNMI
A15	IGNNE*	IGNNE*
F15	KEN*	PKEN*
C15	FLUSH*	FLUSH*
A17	AHOLD	AHOLD
B17	EADS*	EADS*
F16	RDY*	PRDY*
C16	RESET	RST486
Q14	A2	PA2
R15	A3	PA3
S16	A4	PA4
H15	BRDY*	PBRDY*
Q12	A5	PA5
S15	A6	PA6
Q13	A7	PA7
R13	A8	PA8
Q11	A9	PA9
S13	A10	PA10
R12	A11	PA11
S7	A12	PA12
Q10	A13	PA13

Table 2-1. Signal Name Cross Reference *(continued)*

Pin Number	Intel486 Signal Name	System Board Signal Name
R7	A15	PA15
Q9	A16	PA16
Q3	A17	PA17
R5	A18	PA18
Q4	A19	PA19
Q8	A20	PA20
Q5	A21	PA21
Q7	A22	PA22
S3	A23	PA23
S5	A14	PA14
Q6	A24	PA24
R2	A25	PA25
S2	A26	PA26
S1	A27	PA27
R1	A28	PA28
P2	A29	PA29
P3	A30	PA30
Q1	A31	PA31
K15	BE0*	PBE0*
J16	BE1*	PBE1*
J15	BE2*	PBE2*
F17	BE3*	PBE3*

Table 2-1. Signal Name Cross Reference *(continued)*

Pin Number	Intel486 Signal Name	System Board Signal Name
Q15	BREQ	Not Used
P15	HLDA	PHLDA
Q16	PLOCK*	Not used
N15	LOCK*	Not used
N17	W/R*	PW/R*
M15	D/C*	PD/C*
N16	M/IO*	PM/IO*
Q17	PCHK*	Not used
C14	FERR*	FERR*
R16	BLAST*	BLAST*
J17	PCD	PCD
L15	PWT	Not Used
S17	ADS*	PADS*

PD31:0 (Input/Output)

PD31:0 are bidirectional signals that form the data bus for the Intel486 microprocessor. PD7:0 define the least significant byte and PD31:24 the most significant byte.

PDP3:0 (Input/Output)

PDP3:0 are data parity signals. Even parity is generated or checked by the parity generators/checkers. Data parity is generated on all write data cycles with the same timing as the data driven by the Intel486 microprocessor. There is one parity pin for each byte of the data bus.

PCLK (Input)

PCLK provides the fundamental timing and the internal operating frequency for the Intel486 microprocessor. All external timing parameters are specified with respect to the rising edge of PCLK.

PHOLD (Input)

PHOLD allows another bus master complete control of the Intel486 microprocessor bus. The Intel486 microprocessor responds to an active PHOLD signal by asserting PHLDA and placing most of its output and input/output pins in a floated state after completing a bus cycle, burst cycle, or locked sequence of cycles.

PA20M* (Input)

PA20M* causes the Intel486 microprocessor to mask physical address bit 20 before performing a lookup in the internal cache and before driving a memory cycle to the external logic.

PINTR (Input)

PINTR indicates that an external interrupt request has been generated.

PNMI (Input)

PNMI indicates a request for interrupt service has been generated and cannot be masked by software. PNMI has priority over all other interrupts, is rising-edge-sensitive, and is asynchronous to PCLK.

IGNNE* (Input)

When IGNNE* is activated, the Intel486 microprocessor ignores a numeric error and continues running non-control numeric coprocessor instructions. When deactivated, the Intel486 microprocessor freezes on a non-control numeric coprocessor instruction if a previous instruction caused an error.

PKEN* (Input)

PKEN* determines whether the data being returned by the current cycle is cacheable.

FLUSH* (Input)

FLUSH* forces the Intel486 microprocessor to flush its entire internal cache.

AHOLD (Input)

AHOLD allows another bus master access to the Intel486 microprocessor's address bus for a cache invalidation cycle. During this access, the Intel486 microprocessor stops driving its address bus in the clock cycle following an active AHOLD. Only the address bus floats during an address hold. The remainder of the Intel486 microprocessor bus signals remain active.

EADS* (Input)

EADS* indicates that a valid external address has been driven onto the Intel486 microprocessor address bus. This address will then do an internal cache invalidation cycle.

PRDY* (Input)

PRDY* indicates that a current bus cycle is complete. During a read request, PRDY* indicates that an external device has presented valid data on the bus. During a write request, PRDY* indicates that an external device has accepted Intel486 microprocessor data.

RST486 (Input)

RST486 suspends any system operation in progress and places the Intel486 microprocessor in a known (reset) state.

PA3:2 (Output)

PA3:2 form the remainder of the address bus and provide physical memory and I/O port addresses.

PBRDY* (Input)

PBRDY* does the same function during a burst cycle that PRDY* does during a non-burst cycle. PBRDY* indicates that a bus master has presented valid data in response to a read or that the bus master has accepted data in response to a write. PBRDY* is ignored when the Intel486 microprocessor bus is idle and at the end of the first clock during an Intel486 microprocessor bus cycle.

PA31:4 (Input/Output)

PA31:4 form part of the address bus and provide physical memory and I/O port addresses. These lines can be driven as inputs to perform internal cache line invalidations.

PBE3:0* (Output)

PBE3:0* determine which bytes of the address bus must be valid for read and write cycles to external memory. PBE3* applies to PD31:24, PBE2* applies to PD23:PD16, PBE1* applies to PD15:8, and PBE0* applies to PD7:0.

PHLDA (Output)

PHLDA indicates that the Intel486 microprocessor has given up control of its local bus in response to PHOLD being asserted, and is in the bus-hold-acknowledge state. In the bus-hold-acknowledge state, PHLDA is the only bus control signal being driven by the Intel486 microprocessor. The remaining output or bidirectional signals are floated to allow a bus master to control them.

PW/R* (Output)

PW/R* distinguishes between write and read cycles.

PD/C* (Output)

PD/C* distinguishes between data and control cycles.

PM/IO* (Output)

PM/IO* distinguishes between memory and I/O cycles.

FERR* (Output)

The Intel486 microprocessor activates FERR* each time an unmasked numeric coprocessor error occurs.

BLAST* (Output)

BLAST* indicates that the next time PBRDY* is returned, it will be treated as a normal PRDY* signal and will end line fill or other multiple data-cycle transfer.

PCD (Output)

PCD corresponds to two user attribute bits in the page table entry. When paging is enabled, PCD corresponds to bits three and four of the page table entry respectively. When paging is disabled, or for cycles that are not paged when paging is enabled, PCD corresponds to bits three and four in control register three.

PADS* (Output)

PADS* indicates that the address and bus cycle definition signals are valid. PADS* is used by external bus circuitry as an indication that the Intel486 microprocessor has started a bus cycle.

Optional External Cache

The DECpc 433 Workstation system board provides a 113-pin socket for an optional Intel 485Turbocache Module, available in either 64 KB or 128 KB. The external cache is a single-ported device that enhances the capabilities of the Intel486 microprocessor internal cache by providing zero wait states for DRAM read cycles each time an external cache hit occurs. Cache access time is five CPU clock cycles. It is physically connected to the Intel486 microprocessor address bus and acts as a bus watcher.

Base Architecture

The external cache module is a 16-byte line size. Its two-way set-associative external cache contains an 82485 cache controller and eight SRAMs (see Figure 2-1). The following paragraphs contain a detailed description of the 82485 cache controller and SRAMs and brief signal descriptions of signals unique to the external cache.

82485 Cache Controller

The 82485 controller contains two sections. Each section has 2 KB tags with 17 bits per tag so it can store the full 4 GB real address space of the Intel486 microprocessor. These tags also reference two valid bits and a write-protect bit and are forced to reference two consecutive 16-byte lines (two sectors per tag). An LS input (address PA4) determines which sector of each tag is being selected (see Figure 2-2).

The control units of the 82485 are responsible for controlling the data SRAMs, controlling the tag RAM structure, and interfacing to the Intel486 microprocessor. Because the units are independent, the 82485 is capable of updating its tag RAM while data is being bursted into SRAM or it can become invalid during a line fill to a different address.

The 82485 uses the Least Recently Used (LRU) algorithm to determine which tag should be invalidated on cache misses. A single LRU bit per tag points to the tag that will be replaced.

SRAMs

The external cache SRAMs operate at a speed of 24 ns and are capable of zero wait state reads and writes, single clock bursting, and have minimized capacitive loading on the Intel486 microprocessor clock and data lines.

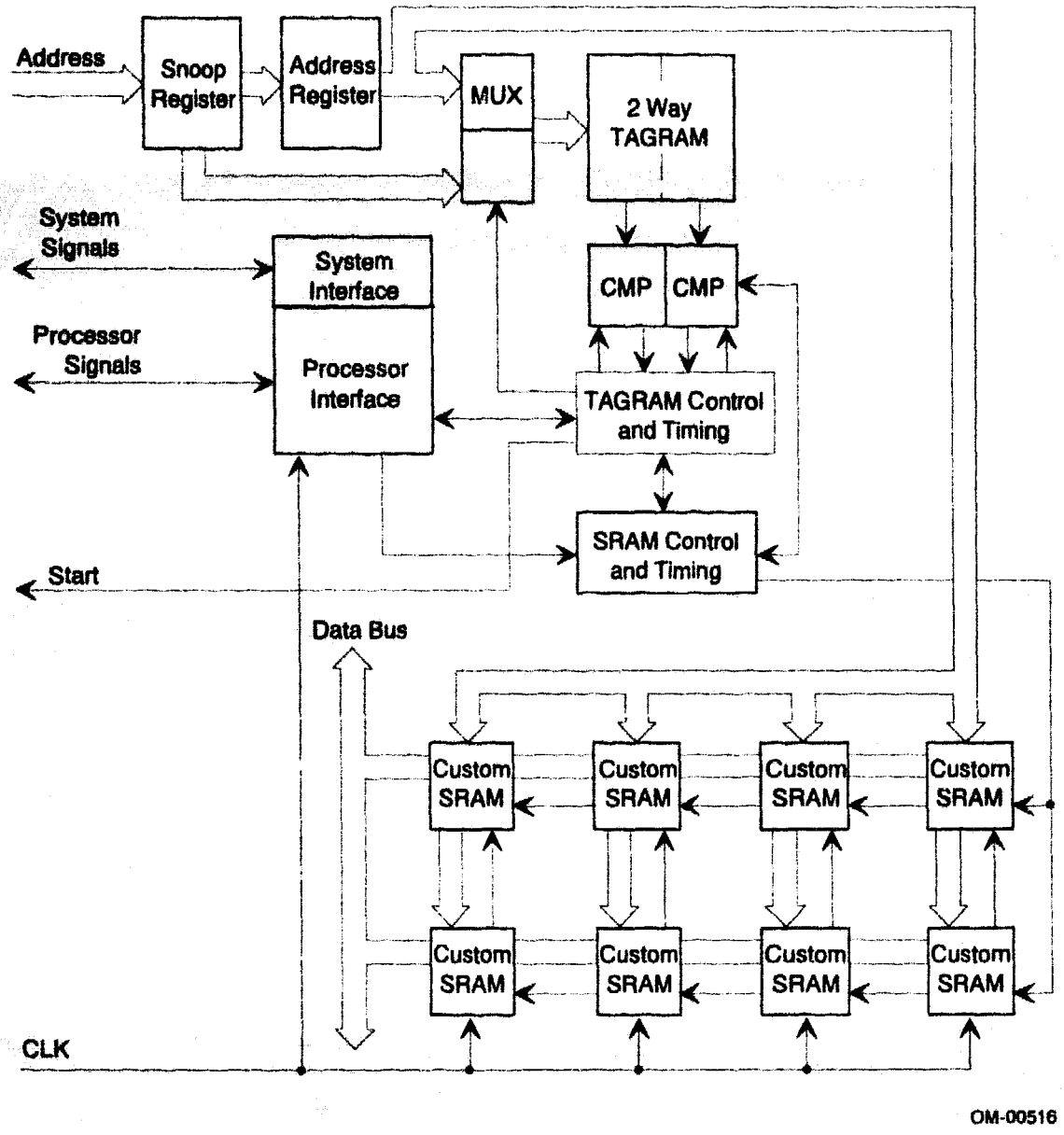


Figure 2-1. External Cache Functional Block Diagram

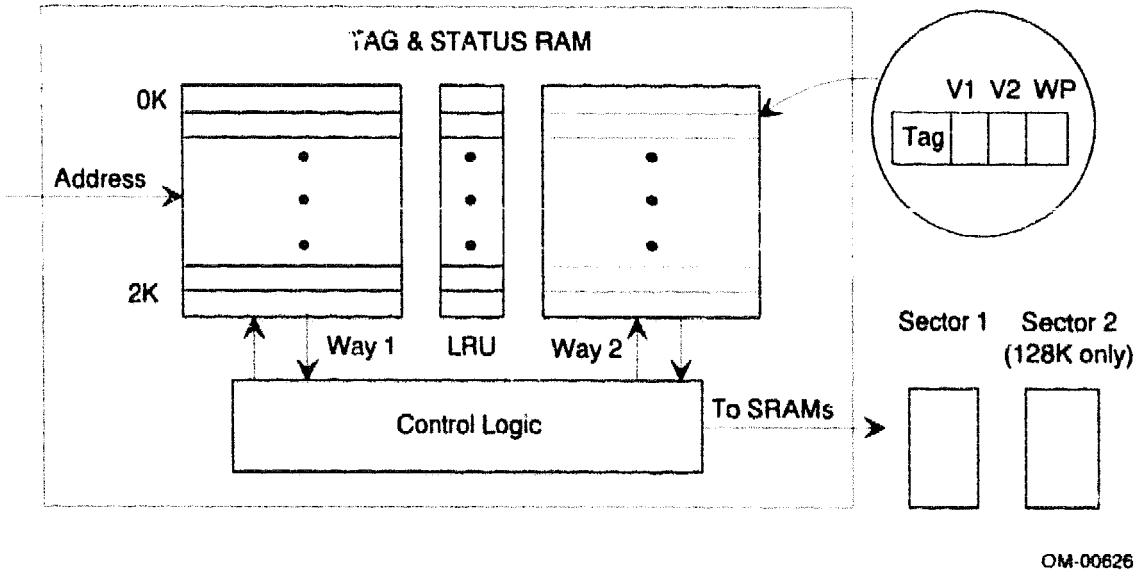


Figure 2-2. 82485 Cache Controller

External Cache Signal Definitions

Table 2-2 is a signal name cross reference for the external cache and system board. Following Table 2-2 are brief descriptions of external cache signals not common to the Intel486 microprocessor.

Table 2-2. External Cache Signal Cross Reference

Pin Number	External Cache Signal Name	System Board Signal Name
J1	A2	PA2
K2	A3	PA3
L1	A4	PA4
L2	A5	PA5
M1	A6	PA6
M2	A7	PA7
N2	A8	PA8
N1	A9	PA9
O1	A10	PA10
P2	A11	PA11
Q2	A12	PA12
R2	A13	PA13
R1	A14	PA14
S1	A15	PA15
T2	A16	PA16
T1	A17	PA17
U2	A18	PA18
U1	A19	PA19
V2	A20	PA20
W2	A21	PA21

Table 2-2. External Cache Signal Cross Reference *(continued)*

Pin Number	External Cache Signal Name	System Board Signal Name
W1	A22	PA22
X1	A23	PA23
Y2	A24	PA24
Y1	A25	PA25
Z2	A26	PA26
Z1	A27	PA27
AA2	A28	PA28
AA1	A29	PA29
BB2	A30	PA30
Q1	A31	PA31
H1	BE0*	PBE0*
H2	BE1*	PBE1*
I1	BE2*	PBE2*
I2	BE3*	PBE3*
B4	CRDY*	PRDY*
C4	CBRDY*	PBRDY*
B2	MIO*	PM/IO*
F1	ADS*	PADS*
F2	WR*	PW/R*

Table 2-2. External Cache Signal Cross Reference *(continued)*

Pin Number	External Cache Signal Name	System Board Signal Name
D1	BLAST*	BLAST*
D5	SKEN*	SKEN*
D2	EADS*	EADS*
C1	RESVD	Not used
E1	BOFF*	BOFF*
E4	WP	C6 WP
B1	CLK	CLKB
A4	CS*	C6 CS*
C2	FLUSH*	FLUSH*
A2	RST	RST486
F4	D0	PD0
G5	D1	PD1
G4	D2	PD2
H5	D3	PD3
I5	D4	PD4
I4	D5	PD5
J5	D6	PD6
J4	D7	PD7
K4	D8	PD8
L5	D9	PD9
L4	D10	PD10

Table 2-2. External Cache Signal Cross Reference *(continued)*

Pin Number	External Cache Signal Name	System Board Signal Name
M5	D11	PD11
N5	D12	PD12
N4	D13	PD13
O5	D14	PD14
O4	D15	PD15
Q4	D16	PD16
R5	D17	PD17
S5	D18	PD18
S4	D19	PD19
T5	D20	PD20
T4	D21	PD21
U4	D22	PD22
V5	D23	PD23
V4	D24	PD24
W5	D25	PD25
X5	D26	PD26
X4	D27	PD27
Y5	D28	PD28
Y4	D29	PD29
Z4	D30	PD30
Z5	D31	PD31
P4	DP0	PDP0

Table 2-2. External Cache Signal Cross Reference *(continued)*

Pin Number	External Cache Signal Name	System Board Signal Name
Q5	DP1	PDP1
AA4	DP2	PDP2
AA5	DP3	PDP3
E5	START*	START*
C5	BRDYO*	CBRDY
B5	CKEN*	CKEN*
BB3	PRSN*	C6PRES*
G2	WPSTP*	WPSTP*

SKEN* (Input)

If the external cache misses a read, the external memory provides the line fill to both the Intel486 microprocessor and to the external cache. System memory reissues the line fill request by activating SKEN*. Multiple line fill requests can be issued as long as a request arrives at its final value in the clock before the first PRDY* or PBRDY* is returned to the Intel486 microprocessor.

C6 WP (Input)

Write protect defines a line as write-protected. Any writes to this line will not update the cache data SRAM. WP is a synchronous signal and requires that the setup and hold times be met at each clock edge regardless of the C6 WP state being acted upon. C6 WP is derived from the write-protect bit of the decode SRAM.

C6 CS* (Input)

Cache select enables a cache cycle. C6 CS* is driven inactive for Intel486 microprocessor locked cycles.

FLUSH* (Input)

Activating this pin causes the external cache to invalidate the contents of its cache. If predictable external cache flushing is required, the pin's setup and hold time requirements must be met. FLUSH* can also accept asynchronous input.

START* (Output)

The external cache generates START* to indicate the current bus cycle must be serviced by the system. The external cache also activates START* for read miss cycles and all writes. START* is not activated for I/O cycles.

CBRDY* (Output)

The external cache activates CBRDYO* when a read hit occurs.

CKEN* (Output)

The external cache activates CKEN* for non-write-protected read hit cycles.

WPSTP* (Output)

The write-protect strap option changes CKEN* behavior each time a read hit occurs on a C6 WP line. If strapped high, CKEN* validates a C6 WP line fill. If strapped low, C6 WP line fills are validated. WPSTP* is always driven low by the system board.

Corona ASIC

The Corona ASIC generates clocks for the Intel486 microprocessor, the 82346 system controller, and the external cache. It also does bus arbitration and bus control functions for accesses initiated by the Intel486 microprocessor and the 82346 system controller. Four configuration ports allow Corona ASIC tailoring for different caching options.

Corona ASIC Functional Units

The Corona ASIC consists of the following functional blocks (see Figure 2-3).

- Clock, reset, and test
- Bus arbitration
- Local bus control
- Cache control
- Bus conversion
- Miscellaneous logic and NPX support
- Address decode
- Configuration ports

The remainder of this section provides a brief description of the Corona ASIC's functional blocks.

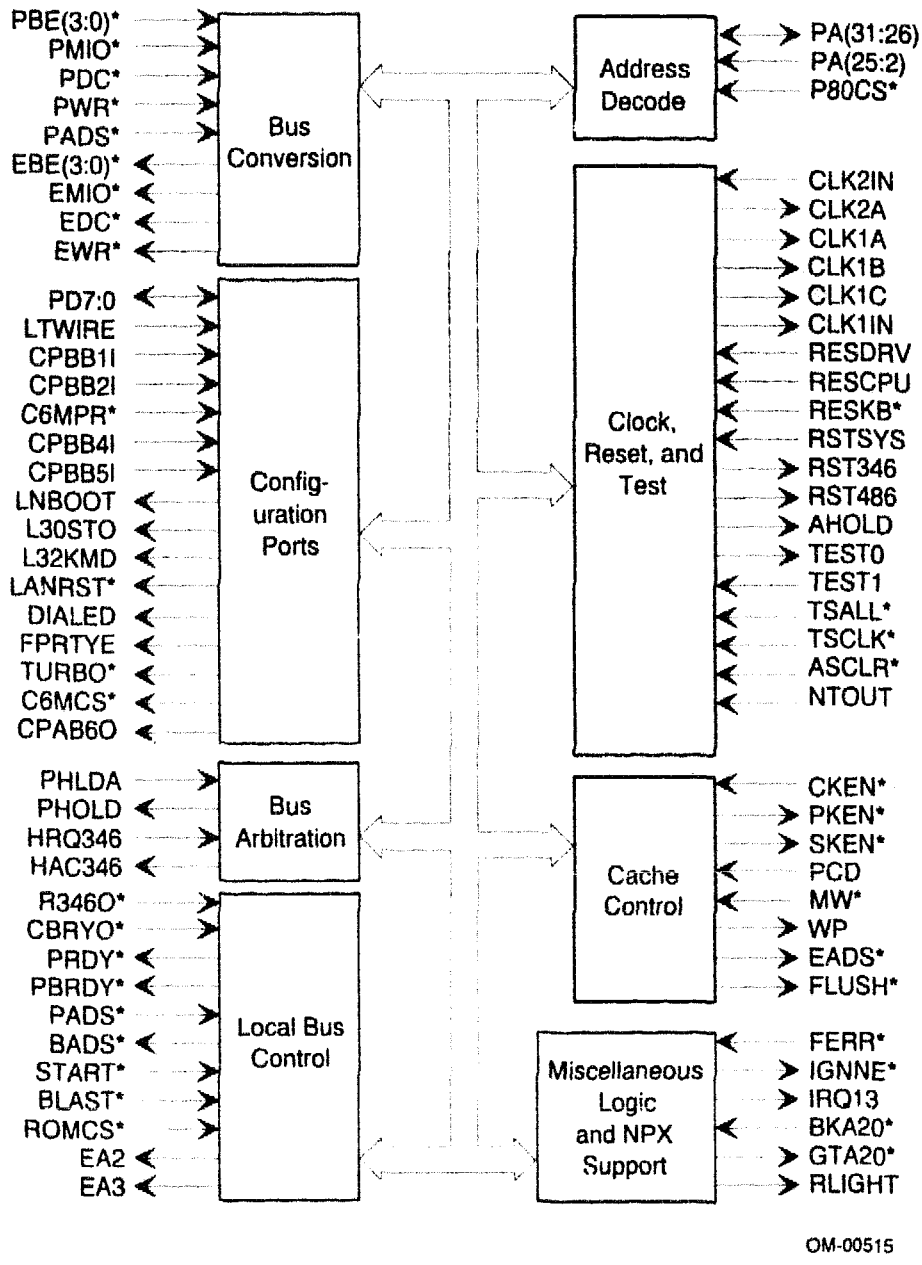


Figure 2-3. Corona ASIC Functional Block Diagram

Clock, Reset, and Test

The clock portion generates 66 MHz and 33 MHz clock signals for the system board and internal Corona ASIC operations. Corona divides the 66 MHz input clock (CLK2IN) by two to produce 33 MHZ clocks for the external cache (CLK1B) and the Intel486 microprocessor (CLK1A). Clock CLK1A is returned from the system board to the Corona ASIC as CLK1IN. Corona also outputs 66 MHz clocks (CLK2A) to the 82346 system controller.

The reset portion forces the Corona ASIC to a known state when either a hard or soft reset is received. Reset also generates synchronous reset to the Intel486 microprocessor and the 82346 system controller.

The test portion provides functionality for component and board level testing.

Bus Arbitration

The bus arbitration block provides bus arbitration control signals in response to DMA or refresh requests from the 82346 system controller. It also monitors memory bus activity and generates an invalidation signal for the Intel486 microprocessor and the external cache. Bus arbitration also provides deturbo functions.

Local Bus Control Block

The local bus control block generates address strobes for the 82346 system controller for all memory accesses except: memory read cycles satisfied by the external cache (secondary cache hit), Corona ASIC configuration register I/O accesses, a flush cycle, or an invalidate external write-back cache cycle. This block also generates ready for both burst and non-burst requests.

Cache Control Block

The cache control block generates cache enable signals for the Intel486 microprocessor and the external cache. It also generates the external cache write protect signal.

Bus Conversion Block

The bus conversion block converts Intel486 microprocessor bus cycle definitions to definitions compatible with the 82346 system controller, (Intel386™ microprocessor compatible).

Miscellaneous Logic and NPX Support Block

The miscellaneous logic provides gate A20 support. The numeric coprocessor extension (NPX) provides hardware support for floating-point errors. This includes floating-point error (FERR*), ignore floating-point error (IGNNE*), and interrupt request 13 (IRQ13).

Address Decode Block

The address decode block decodes various system memory address spaces and then passes this information internally to the cache control block. The address decode block also generates internal select signals for configuration ports. Accesses to these ports are by the Intel486 microprocessor local bus and are not translated into 82346 system controller cycles.

Configuration Ports Block

The Corona ASIC contains four configuration ports (A through D) that enable or disable various system and test options. Configuration ports A, C, and D are output ports with readback. Configuration port B is read only. Refer to Tables 2-3 through 2-8 for specific bit definitions. Configuration ports are initialized with a hard reset and are not affected by a soft reset.

Table 2-3. Configuration Port A Bit Definitions for Ethernet

Bit	Definition
7	When active high and a soft reset occurs, causes the Intel486 microprocessor to perform its Built-in Self Test (BIST).
6	Reserved.
5	When active high, generates false parity.
4	When active high, turns on the diagnostic LED.
3	When active high, resets onboard LAN logic without resetting the system board. Stays reset until set back to zero.
2	When active high, selects LAN data buffer size of 32 KB. When active low, selects a LAN data buffer size of 64 KB.
1	When active high, sets LAN operation timeout to 30 seconds. When active low, sets the LAN operation timeout to 2.5 minutes.
0	When active high, configures system board LAN logic for remote boot.

Table 2-4. Configuration Port B Bit Definitions for Ethernet

Bit	Definition
7:4	Reserved.
3	When sampled high, an external cache is installed on the system board.
2:1	Reserved.
0	When active high, the Shielded Twisted Pair/Unshielded Twisted Pair switch is in the Shielded Twisted Pair position.

Table 2-5. Configuration Port A Bit Definitions for Token Ring

Bit	Definition
7	When active high and a soft reset occurs, causes the Intel486 microprocessor to perform its BIST.
6	When active high, selects 16 Mbps Token Ring network. When active low, selects 4 Mbps Token Ring network.
5	When active high, generates false parity.
4	When active high, turns on the diagnostic LED.
3	When active high, resets onboard LAN logic without resetting the system board. Stays reset until set back to zero.
2	When active high, selects upper 1 MB of 2 MB LANBOOT PROM (if 2 MB PROM installed), otherwise, no effect.
1	Reserved.
0	When active high, configures system board LAN logic for remote boot.

Table 2-6. Configuration Port B Bit Definitions for Token Ring

Bit	Definition
7:4	Reserved.
3	When sampled high, an external cache is installed on the system board.
2:1	Reserved.
0	When active high, the Shielded Twisted Pair/Unshielded Twisted Pair switch is in the Shielded Twisted Pair position.

Table 2-7. Configuration Port C Bit Definitions

Bit	Definition
7	When active high, pulses the FLUSH* signal to flush both the primary and secondary cache. Returns zero when read.
6	When active high, the external cache is not selected.
5	When active high, sets the write protection attribute of the cache lines filled from video BIOS address space 0C0000H to 0C7FFFH.
4	When active high, enables the cache for system BIOS address space 0E0000H to 0FFFFFH.
3	When active high, enables the cache for video BIOS address space 0C0000H to 0C7FFFH.
2	When active high, enables the cache for memory address space 80000H to 9FFFFH.
1	When active high, enables the external cache.
0	When active high, enables the Intel486 microprocessor's internal cache.

Table 2-8. Configuration Port D Bit Definitions

Bit	Definition
7	When active high, controls the deturbo emulation speed of the Intel486 microprocessor as set by bits 5:0. When active low, the Intel486 microprocessor runs at full speed.
6	Reserved.
5:0	This 6-bit unsigned integer loads a counter to adjust the effective speed of the Intel486 microprocessor in the deturbo mode.


СНАРЗ

3

Memory

Introduction

System memory is primarily controlled by the memory controller section of the 82346 system controller. The memory controller generates access timing signals for fast-paged mode memory and, if more than one memory bank is installed, generates bank-interleaved fast-paged mode accesses (see Figure 3-1). For a complete description of the 82346 system controller, refer to Chapter 5.

During memory accesses, the memory controller converts its local bus signals to the proper memory control signals. It also generates the necessary data conversion signals and then passes them to the correct byte lanes. During memory accesses by DMA or bus masters, the memory controller does the necessary signal conversions to properly read data from and write data to memory.

Memory refresh is also controlled by the memory controller. A typical refresh cycle takes approximately 1 µs every 16 µs. In addition, all refresh cycles are staggered to minimize power supply loading and attendant noise on ground pins.

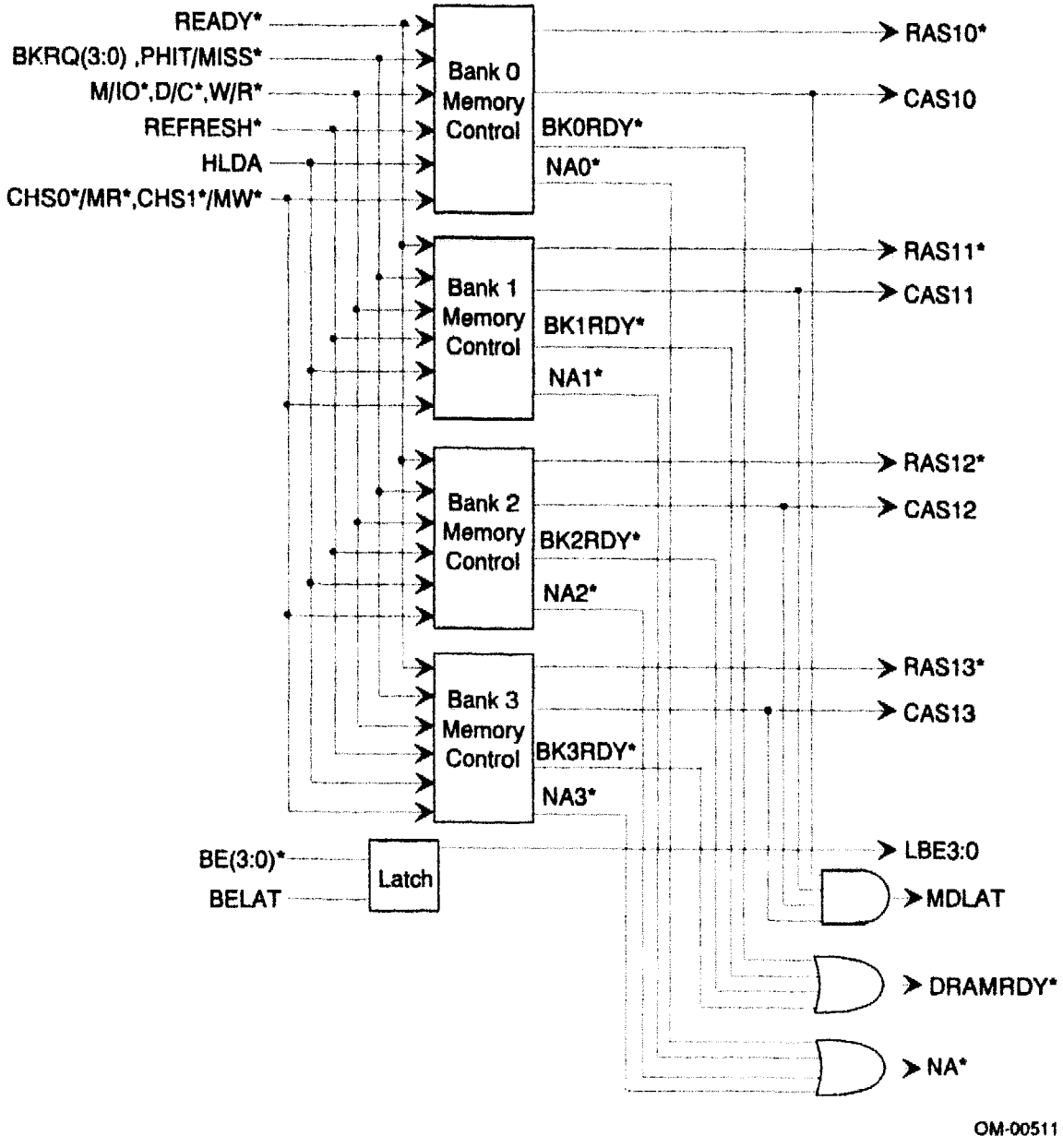


Figure 3-1. 82346 Memory Controller Section Block Diagram

DRAM

The DECpc 433 Workstation system board provides three 32-bit memory banks that support up to 48 MB of DRAM. DRAM consists of either 1 MB or 4 MB Single In-line Memory Modules (SIMMs). DRAM access time is 80 nanoseconds or faster. Both types of SIMMs can be mixed between the three memory banks; however, they cannot be mixed within the same memory bank.

Memory Mapping

The memory controller supports the nine DRAM memory maps listed in Table 3-1. Each combination listed is addressable in each of the three 32-bit memory banks. Note that memory banks zero through two are referred to as logical banks when internally addressed by the 82346. The actual system board memory banks, when accessed internally, might differ depending on the value stored in the indexed configuration register RAMMOV. The memory column lists the total amount of DRAM available in each memory map. The RAMMAP (4:0) column indicates the hex value written in bits four through zero from the RAMMAP indexed configuration register (refer to Table 3-2).

Table 3-1. DRAM Mapping

Config No.	Bank 0 SIMMs	Bank 1 SIMMs	Bank 2 SIMMs	Total Mem	RAMMAP (4:0)
1	(4) 1 MB			4 MB	4
2	(4) 1 MB	(4) 1 MB		8 MB	7
3	(4) 1 MB	(4) 1 MB	(4) 1 MB	12 MB	A
4	(4) 4 MB			16 MB	C
5	(4) 1 MB	(4) 4 MB		20 MB	F
6	(4) 1 MB	(4) 1 MB	(4) 4 MB	24 MB	10
7	(4) 4 MB	(4) 4 MB		32 MB	11
8	(4) 4 MB	(4) 4 MB	(4) 1 MB	36 MB	14
9	(4) 4 MB	(4) 4 MB	(4) 4 MB	48 MB	16

Table 3-2. RAMMAP Indexed Configuration Register

Bit	Function
7:5	Always one
4:0	DRAM memory map code

Fast-Paged Mode and Interleaving

DRAM operates in fast-paged mode or two-way interleaving. Both options are selected by programming the RAMMAP and RAMSET indexed configuration registers (refer to Tables 3-2 and 3-3, respectively). Fast-paged mode is enabled or disabled for each pair of memory banks independently. Interleaving requires two memory banks. Banks zero and one are the memory banks available for interleaving. Refer to Table 3-4 for a listing of fast-paged and interleave options versus selected memory map options.

Table 3-3. RAMSET Indexed Configuration Register

Bit	Function
7:6	DRAM drive
5	STDLY
4	PIPE
3	Page mode A
2	Page mode B
1	Bank A interleave
0	Bank B interleave

Table 3-4. Fast Paged/Interleave Versus Memory Map Options

32-Bit DRAM Memory Banks			Page/ Interleave		Total Mem
Bank 0	Bank 1	Bank 2	A	B	
(4) 1 MB			A	2/P	4 MB
(4) 1 MB	(4) 1 MB		2/P		8 MB
(4) 1 MB	(4) 1 MB	(4) 1 MB	2/P	Page	12 MB
(4) 4 MB			2/P	Page	24 MB
(4) 1 MB	(4) 4 MB		Page		16 MB
(4) 1 MB	(4) 1 MB	(4) 4 MB	2/P	Page	32 MB
(4) 4 MB	(4) 4 MB		2/P	Page	36 MB
(4) 4 MB	(4) 4 MB	(4) 1 MB	2/P	Page	48 MB
(4) 4 MB	(4) 4 MB	(4) 4 MB	Page		20 MB

DRAM Timing Parameters

Two configuration registers are used to program the DRAM timing parameters: RASTMA and CASTMA. Refer to Table 3-5 for specific bit allocations.

Table 3-5. RASTMA and CASTMA Configuration Registers

RASTMA		CASTMA	
Bit	Function	Bit	Function
7	RAS address select	7:6	CASW
6	RCD	5	CST
5:3	RP	4:3	CP
2:0	RAS	2:0	CASR

DRAM Refresh

The memory controller generates onboard DRAM refresh cycles and controls both onboard and offboard refresh timing in all modes. Refresh timing occurs in two modes: coupled mode or decoupled mode. In coupled mode, refresh timing for the system board and intelligent graphics controller executes synchronously. In decoupled mode, the memory controller has complete control over the timing of onboard refresh and offboard refresh; however, the timing of each is independent. Configuration register REFCTL is used to program the specific modes (refer to Table 3-6).

Table 3-6. REFCTL Configuration Register

Bit	Function
7	Decouple
6:4	Slow refresh (system board)
3	10/16 I/O
2:0	Slow refresh (intelligent graphics controller)


CHAP 4

4

82340DX ISA Chip Set

Introduction

The 82340DX ISA Chip Set contains an 82344 ISA bus controller, an 82345 data buffer, and an 82346 system controller (see Figure 4-1). This chapter describes each of these in detail.

82344 ISA Bus Controller

The 82344 ISA Bus Controller provides the functions of DMA, interrupt control, counter/timer, and real-time clock (see Figure 4-2). The following paragraphs describe each of these subsections in detail.

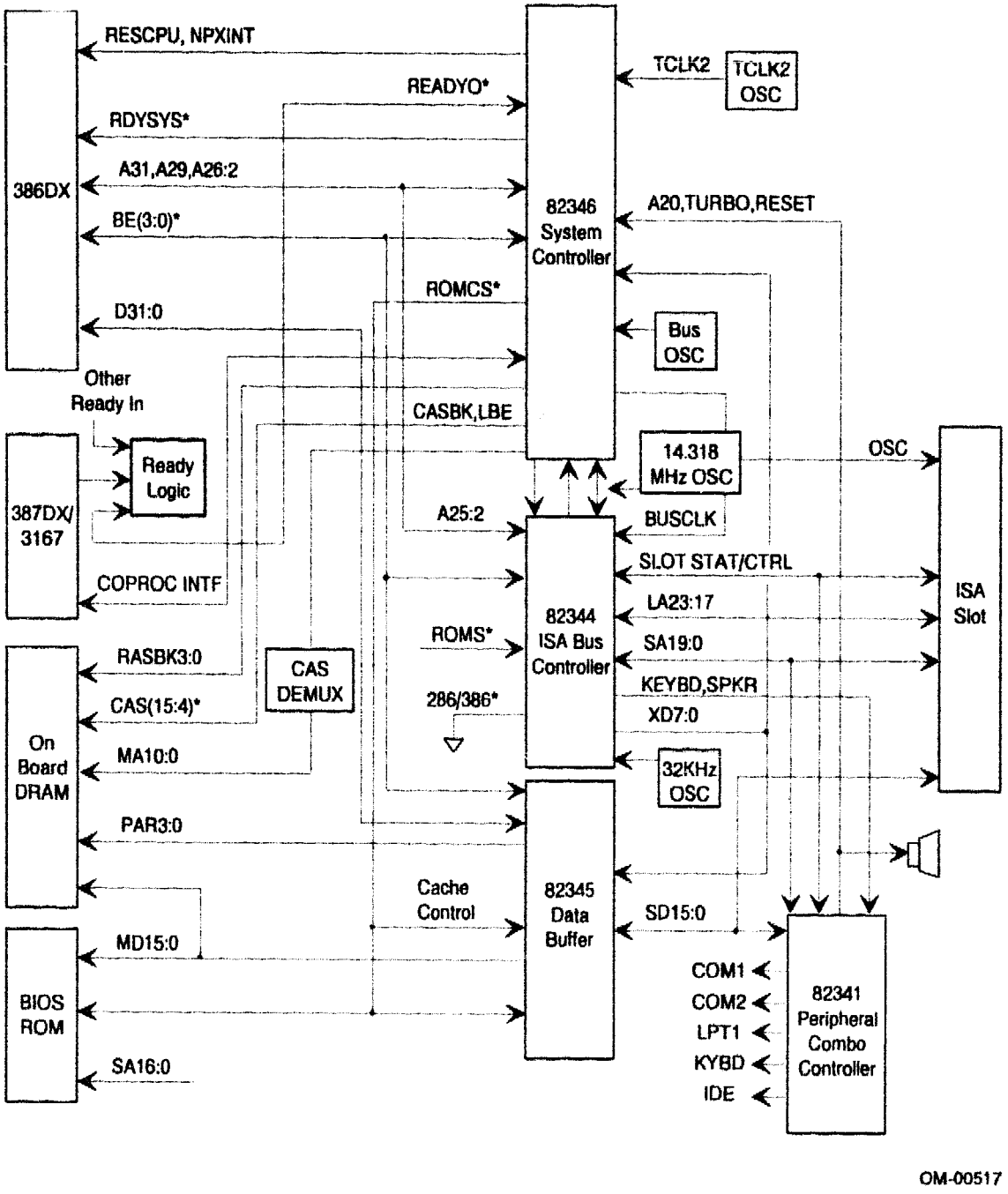


Figure 4-1. 82340DX Functional Block Diagram

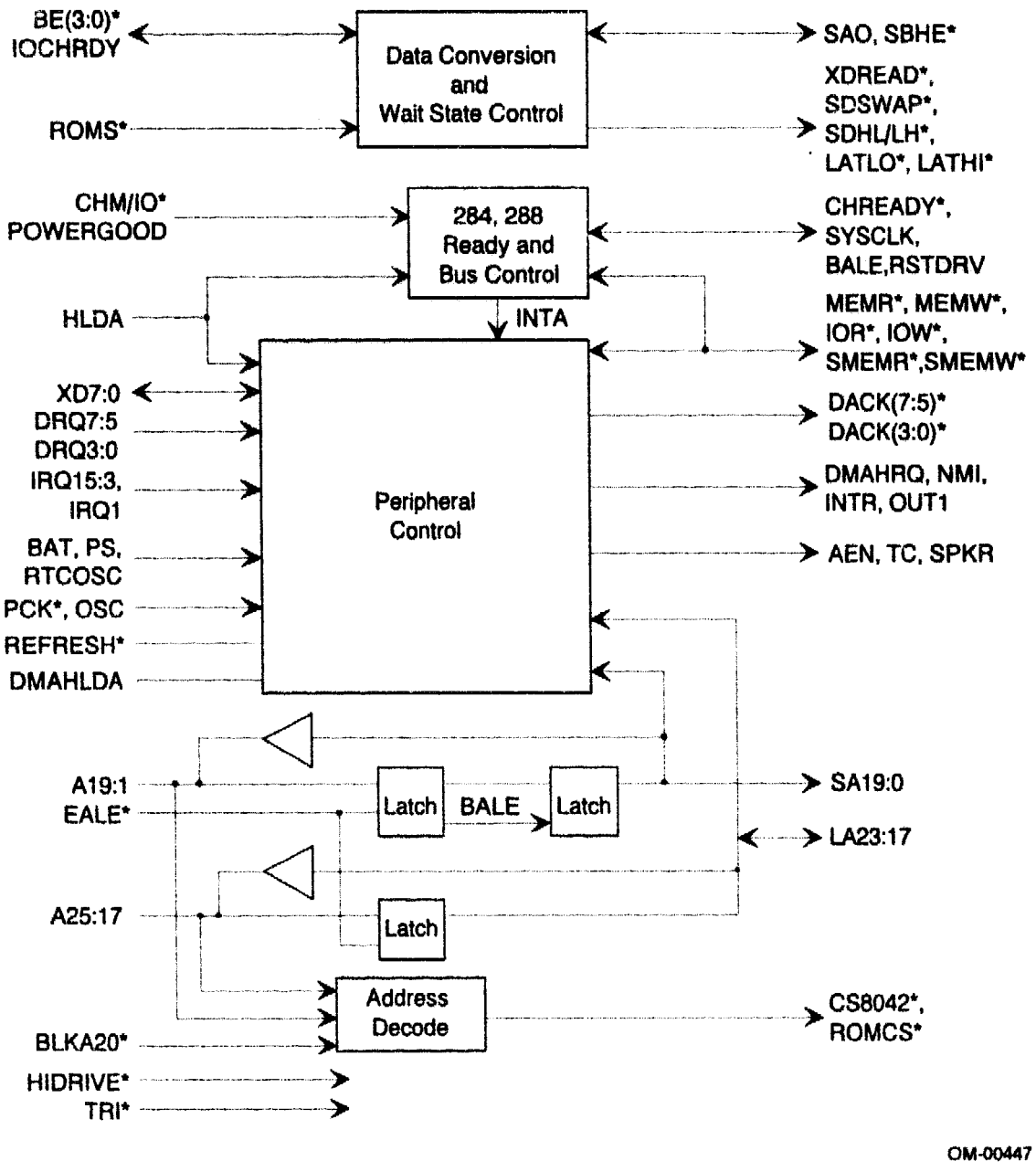


Figure 4-2. 82344 Functional Block Diagram Subsection

DMA

The DMA subsection controls DMA transfers between I/O channels, onboard memory, and ISA slot accessing. It allows data transfers throughout the entire 48 MB range of system board DRAM and drives the appropriate bus command signals, depending on whether an access is a memory read or write (see Figure 4-3).

The DMA subsection contains the following:

- Two DMA controllers
- Middle address bit latches
- DMA controller registers
- Page registers
- Address generation

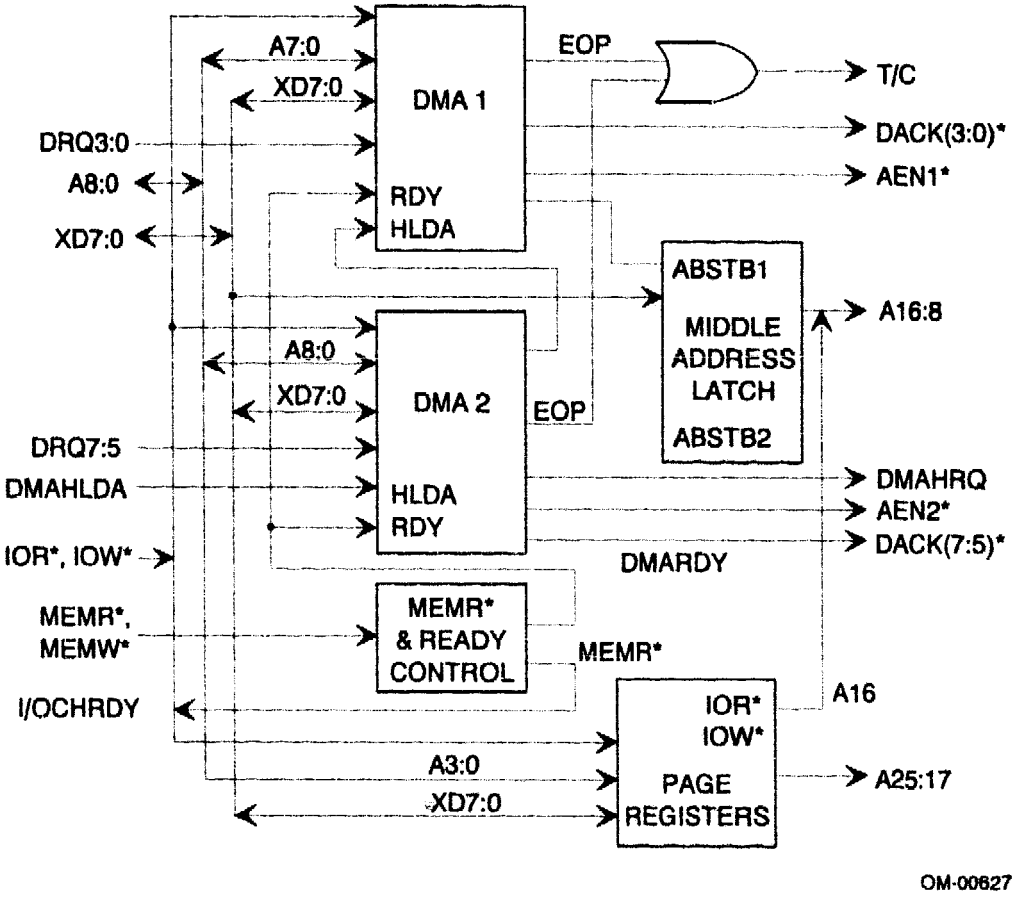


Figure 4-3. DMA Subsection Functional Block Diagram

DMA Controllers

The ISA bus controller supports seven DMA channels using two 8237 DMA controller equivalent megacells. The megacells are programmable via two indexed configuration registers: DMA and ROMDMA (refer to Tables 4-1 and 4-2). DMA controller one contains channels zero through three. These channels are used to transfer data between 8-bit peripherals and 8- or 16-bit memory in pages of 64 KB. DMA controller two contains channels four through seven. These channels (except channel four) are used to transfer data between 16-bit I/O adapters and 16-bit memory in pages of 128 KB. Also, a full 26-bit address is output for each of the seven channels, so data can be transferred throughout the entire 48 MB system address space.

Table 4-1. DMA Indexed Configuration Register

Bit	Function
7	Enable FF
6	4xx enable
5:1	Always one
0	FF PTR

Table 4-2. ROMDMA Indexed Configuration Register

Bit	Function
7:6	ROM wait states
5:4	8-bit wait states
3:2	16-bit wait states
1	DMA clock
0	MEMR* timing

Middle Address Bit Latches

The middle address bits are latched to an internal 8-bit register when the DMA controller writes a specified value onto an internal bus and by issuing an address strobe. The DMA controller issues the address strobe at the beginning of a DMA cycle and each time the lower 8-bit address increments across an 8-bit subpage boundary during block transfers. The middle DMA address bits register cannot be written to or read from externally and can only be loaded from the address strobe signals.

DMA Controller Registers

Table 4-3 lists the addresses of all registers that can be read or written to DMA controller one and two.

Table 4-3. DMA Controller Read/Write Addressing

DMA2	DMA1	Function
0C0H	000H	Channel zero base and current address register
0C2H	001H	Channel zero base and current word count register
0C4H	002H	Channel one base and current address register
0C6H	003H	Channel one base and current word count register
0C8H	004H	Channel two base and current address register
0CAH	005H	Channel two base and current word count register
0CCH	006H	Channel three base and current address register
0CEH	007H	Channel three base and current word count register
0D0H	008H	Read status register/write command register
0D2H	009H	Write request register
0D4H	00AH	Write single mask register bit
OD6H	00BH	Write mode register
0D8H	00CH	Clear byte pointer flip-flop
0DAH	00DH	Read temporary register/write master clear
0DCH	00EH	Clear mask register
0DEH	00FH	Write all mask register bits

Page Registers

An extended megacell is used in the ISA bus controller to generate the page registers for each DMA channel. These page registers provide the upper address bits during DMA cycles and are programmed by the ROMDMA indexed configuration register. Tables 4-4 and 4-5 list the available page register options.

Table 4-4. DMA Page Register Option One

Addresses A25:24 (B6 = 1)	Addresses A23:16 (B6 = x)	DMA Channel
487H	87H	0
483H	83H	1
481H	81H	2
482H	82H	3
48BH	8BH	5
489H	89H	6
48AH	8AH	7
48FH	8FH	REFRESH*

Table 4-5. DMA Page Register Option Two

Addresses A25:24 (B0 = 1, B7 = 1)	Addresses A23:16 (B0 = 0, B7 = 1)	DMA Channel
87H	87H	0
83H	83H	1
81H	81H	2
82H	82H	3
8BH	8BH	5
89H	89H	6
8AH	8AH	7
8FH	8FH	REFRESH*

Address Generation

DMA addressing for the ISA slot and system DRAM is made up of upper, middle, and lower address portions. The page registers for each DMA controller generate the upper address portion and must be set up by the Intel486 microprocessor prior to any DMA operation. The DMA controllers generate the middle address portion at the beginning of a DMA operation and each time a DMA address increments or decrements through a block boundary. The DMA controllers also generate the lower address portion during DMA operations. Tables 4-6 and 4-7 list the DMA addressing for the ISA slot and system DRAM.

Table 4-6. DMA Addressing for ISA Slot Access

Page Registers	Middle Address Latches	8237 Megacell	8-Bit DMA	16-Bit DMA
M9				
M8				
M7			LA23	LA23
M6			LA22	LA22
M5			LA21	LA21
M4			S/LA20	S/LA20
M3			S/LA19	S/LA19
M2			S/LA18	S/LA18
M1			S/LA17	S/LA17
M0			SA16	
	D7		SA15	SA16
	D6		SA14	SA15
	D5		SA13	SA14
	D4		SA12	SA13
	D3		SA11	SA12
	D2		SA10	SA11
	D1		SA9	SA10
	D0		SA8	SA9
		A7	SA7	SA8

Table 4-6. DMA Addressing for ISA Slot Access *(continued)*

Page Registers	Middle Address Latches	8237 Megacell	8-Bit DMA	16-Bit DMA
		A6	SA6	SA7
		A5	SA5	SA6
		A4	SA4	SA5
		A3	SA3	SA4
		A2	SA2	SA3
		A1	SA1	SA2
		A0	SA0	SA1
		VSS		SA0
		A0*	SBHE*	
		VSS		SBHE*

Table 4-7. DMA Addressing for System DRAM Accesses

Page Registers	Middle Address Latches	8237 Megacell	8-Bit DMA	16-Bit DMA
M9			A25	A24
M8			A24	A24
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18

Table 4-7. DMA Addressing for System DRAM Accesses *(continued)*

Page Registers	Middle Address Latches	8237 Megacell	8-Bit DMA	16-Bit DMA
M1			A17	A17
M0			A16	
	D7		A15	A16
	D6		A14	A15
	D5		A13	A14
	D4		A12	A13
	D3		A11	A12
	D2		A10	A11
	D1		A9	A10
	D0		A8	A9
		A7	A7	A8
		A6	A6	A7
		A5	A5	A6
		A4	S4	A5
		A3	A3	A4
		A2	A2	A3
		A1		A2
		A0		

Interrupt Controller

The interrupt controller consists of two 8259 programmable interrupt controller equivalent megacells with eight interrupt request lines each. The two 8259s are cascaded inside the ISA bus controller with two of the interrupt request inputs connected to internal circuitry. This allows a total of 13 external interrupt requests (see Figure 4-4).

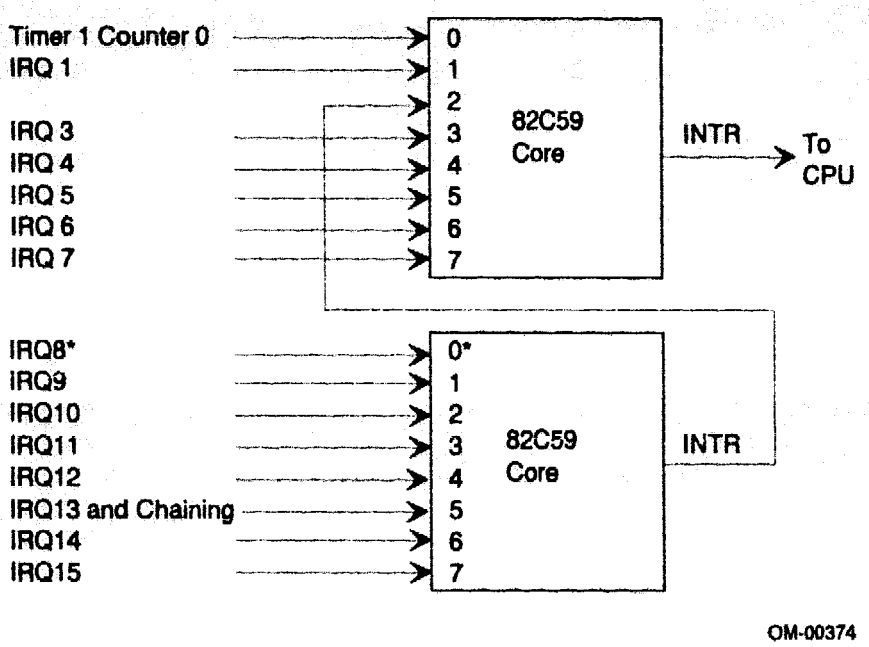


Figure 4-4. Interrupt Controller Functional Block Diagram

Interrupt Controller Registers

The internal registers of the 8259 megacells are written to in the same manner as the standard 8259 chip. However, before normal operation begins, each megacell must follow an initialization sequence. The sequence starts by writing Initialization Command Word one (ICW1). Once written, the megacells expect the following sequence: ICW2, ICW3, and ICW4 (if required). Operation Control Words (OCWs) are written any time after initialization (refer to Tables 4-8 and 4-9).

Table 4-8. Interrupt Controller Write Operations

Int1	Int2	XD4	XD3	Register Function
020H	0A0H	1	x	Write ICW1
021H	0A1H	x	x	Write ICW2
021H	0A1H	x	x	Write ICW3
021H	0A1H	x	x	Write ICW4
021H	0A1H	x	x	Write OCW1
020H	0A0H	0	0	Write OCW2
020H	0A0H	0	1	Write OCW3

Table 4-9. Interrupt Controller Read Operations

Int1	Int2	Register Function
020H	0A0H	Interrupt Request Register (IRR), In-Service Register (ISR), or Poll Command (PC)
021H	0A1H	Interrupt Mask Register (IMR)

Interrupt Levels

Table 4-10 lists the interrupt levels for the DECpc 433 Workstation.

Table 4-10. DECpc 433 Workstation System Interrupt Levels

Priority	Interrupt Controller	Interrupt Number	Interrupt Source
1	1	IRQ0	Timer tick
2	1	IRQ1	Keyboard controller
	1	IRQ2	Cascade interrupt
3	2	IRQ8	Real-time clock (RTC)
4	2	IRQ9	Reserved
5	2	IRQ10	TIGA video
6	2	IRQ11	SCSI interrupt
7	2	IRQ12	Mouse interrupt
8	2	IRQ13	Numeric coprocessor
9	2	IRQ14	Hard disk drive
10	2	IRQ15	Reserved
11	1	IRQ3	COM2
12	1	IRQ4	COM1
13	1	IRQ5	LAN interrupt
14	1	IRQ6	Floppy disk drive
15	1	IRQ7	LPT1

Counter/Timer

The counter/timer consists of one 8254 programmable interval timer equivalent megacell with three independent counters. The clocks for each of the internal counters are tied to a 14.318 MHz oscillator through a divide-by-twelve counter. The gate inputs of counters zero and one are tied high to enable them at all times. The gate input of counter two is tied to bit zero of the port B register inside the ISA bus controller (see Figure 4-5).

Counter/Timer Outputs

Three counter/timer outputs are available from the 8254 megacell. One of the three outputs is directly available at an external pin. The output of counter zero is connected to input IRQ0 at interrupt controller one. The output of counter one is directly connected to pin OUT1. The output of one counter is tied to one of the inputs of an AND gate; the other AND gate input is connected to bit one of the port B register inside the ISA bus controller (see Figure 4-5). Table 4-11 lists the addressing for each of the counter/timer's internal registers.

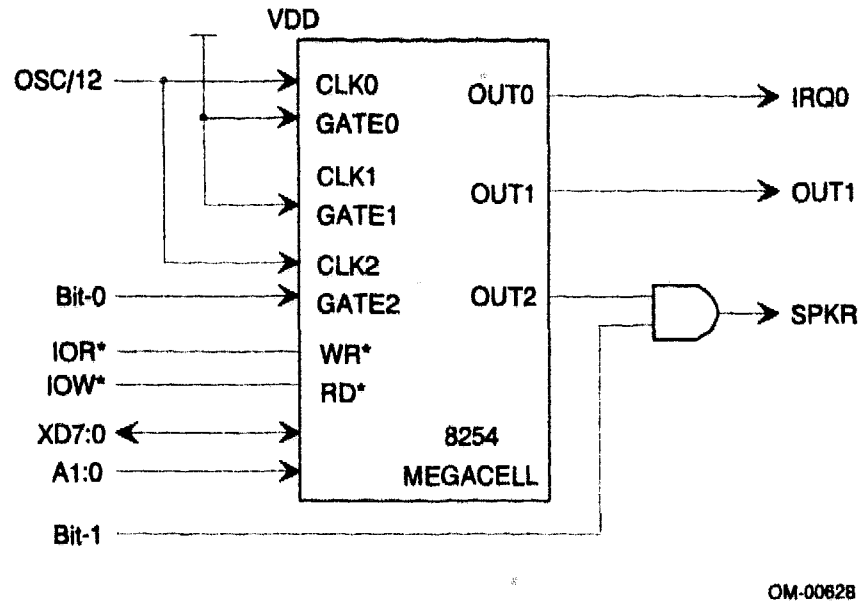


Figure 4-5. Counter/Timer Functional Block Diagram

Table 4-11. Counter/Timer Register Addressing

Address	IOR*	IOW*	Register Function
040H	1	0	Write initial count to counter
040H	0	1	Read count/status from counter zero
041H	1	0	Write initial count to counter one
041H	0	1	Read count/status from counter one
042H	1	0	Write initial count to counter two
042H	0	1	Read count/status from counter two
043H	1	0	Write control word
043H	0	1	No operation

Real-Time Clock

The Real Time Clock (RTC) contains a 146818 RTC equivalent megacell. This megacell consists of 10 RAM bytes (for the time, calendar, and alarm data), four control and status bytes, and 114 general purpose RAM bytes (refer to Table 4-12).

Note

If the system information contained in the RTC becomes corrupted or if the RTC needs to be replaced, you must clear CMOS RAM and, if set, the password using the clear CMOS RAM and clear password jumpers before resetting system parameters. Table 4-13 describes the jumper settings.

Table 4-12. RTC Clock Address Map

Address	Function	Range
127:14	User RAM	
13	RTC register D	Read only
12	RTC register C	Read only
11	RTC register B	Read/write
10	RTC register A	Read/write
9	Year	99:0
8	Month	12:1
7	Date of month	31:1
6	Day of week	7:1
5	Hours (alarm)	23:0
4	Hours (time)	12:1 (12 hour mode)
2	Minutes (time)	59:0
1	Seconds (alarm)	59:0
0	Seconds (time)	59:0

Table 4-13. System Board Jumper Settings

Feature	Description	Jumper Settings
Password	Normal operation (default)	E1-1 and E1-2
	Clear password	E1-2 and E1-3
CMOS RAM	Normal operation (default)	E1-4 and E1-5
	Clear CMOS RAM	E1-5 and E1-6

Time-Of-Day Registers

The contents of the time-of-day registers can be binary or BCD. The addressing for these registers are listed in Table 4-14.

Table 4-14. Time-of-Day Register Addressing

Address	BCD Mode	Binary Mode	Function/Time
9	99:0	63:0H	Year
8	12:1	0C:1H	Month
7	31:1	1F:1H	Date
6	7:1	7:1H	Day-of-week
5	12:1	0C:01H	Hours/alarm/am
5	92:81	8C:81H	Hours/alarm/pm
4	12:1	0C:01H	Hours/am
4	92:81	8C:81H	Hours/pm
3	60:0	0B:3H	Minutes/alarm
2	60:0	0B:3H	Minutes
1	60:0	0B:3H	Seconds/alarm
0	60:0	0B:3H	Seconds

Control Registers

The 146818 megacell contains four control registers: A, B, C, and D. All four registers are accessible by the Intel486 microprocessor and are fully accessible during update cycles (refer to Table 4-12).

All 128 bytes can be directly read and written by the Intel486 microprocessor except for the following:

- Registers C and D (read-only)
- Bit seven of register A (read-only)
- Bit seven of the seconds byte (read-only)

Control Register A

This register contains control bits for selecting periodic interrupts, input divisors, and an update-in-progress status bit. Refer to Table 4-15 for control register A bit assignments.

Table 4-15. Control Register A Bit Assignments

Bit	Description	Abbreviation
7	Update in progress	UIP
6	Divisor bit two	DV2
5	Divisor bit one	DV1
4	Divisor bit zero	DV0
3	Rate select bit three	RS3
2	Rate select bit two	RS2
1	Rate select bit one	RS1
0	Rate select bit zero	RS0

Control Register B

This register contains command bits to control various modes of operation and interrupt enables for the RTC. Refer to Table 4-16 for control register B bit assignments.

Table 4-16. Control Register B Bit Assignments

Bit	Description	Abbreviation
7	Set command	SET
6	Periodic interrupt enable	PIE
5	Alarm interrupt enable	AIE
4	Update end interrupt enable	UIE
3	Reserved	
2	Data mode (binary or BCD)	DM
1	24/12 mode	24/12
0	Daylight savings enable	DSE

Control Register C

This register contains status information relating to interrupts and the internal operation of the RTC. Refer to Table 4-17 for control register C bit assignments.

Table 4-17. Control Register C Bit Assignments

Bit	Description	Abbreviation
7	IRQ pending flag	IRQF
6	Periodic interrupt flag	PF
5	Alarm interrupt flag	AF
4	Update ended flag	UF
3:0	Reserved	

Control Register D

This register contains a bit indicating the status of the on-chip standby RAM. Refer to Table 4-18 for control register D bit assignments.

Table 4-18. Control Register D Bit Assignments

Bit	Description	Abbreviation
7	Valid RAM data and time	VRT
6	Not used (read as 0)	
5	Not used (read as 0)	
4	Not used (read as 0)	
3	Not used (read as 0)	
2	Not used (read as 0)	
1	Not used (read as 0)	
0	Not used (read as 0)	

82345 Data Buffer

The 82345 data buffer does all the data buffering functions required by the DECpc 433 Workstation's system board. By direction of the Intel486 microprocessor, the ISA data buffer routes data to and from the Intel486 microprocessor, memory, and ISA data buses. It also provides the data conversion necessary for 32- or 16-bit writes to 16- or 8-bit devices and, under the control of DMA or another bus master, allows 8- or 16-bit data routed to and from the ISA data bus and memory data bus.

82346 ISA System Controller

The 82346 system controller provides built-in paged mode operation, two-way interleaving, programmable DRAM timing, system board and ISA slot refresh, full EEMS support, shadowing, and provides the bus clock and signalling interface to the 82344 ISA bus controller (see Figure 4-6).

The system controller consists of the following:

- An Intel386 microprocessor interface
- An ISA bus/system controller communication channel
- A DRAM support subsystem
- I/O control registers
- Halt/shutdown detection

The following sections describe each of these functions in detail.

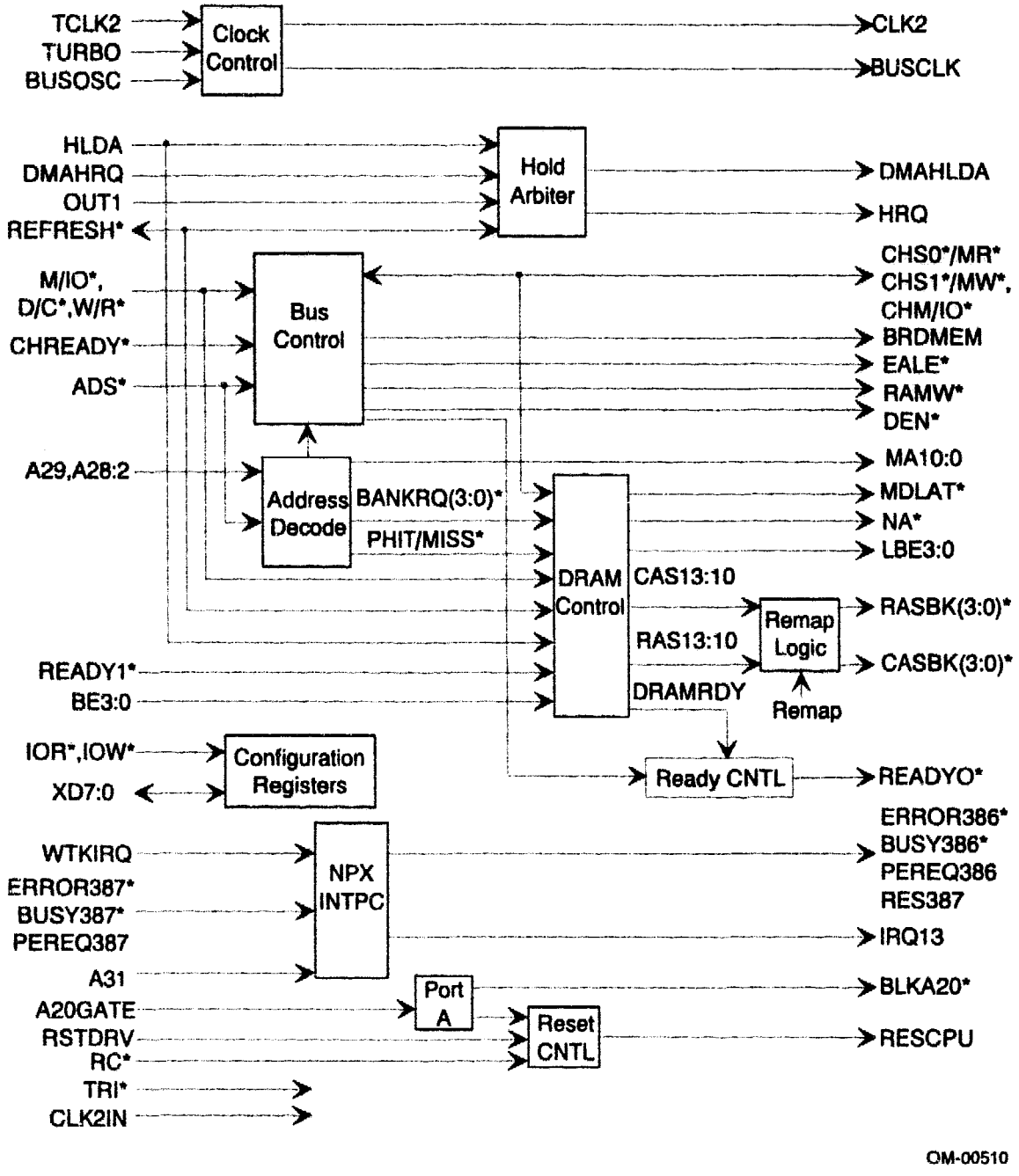


Figure 4-6. 82346 System Controller Functional Block Diagram

Intel486 Microprocessor Interface

This portion of the system controller handles the control interface between the Intel486 microprocessor bus, memory data bus (via the Corona ASIC), and the ISA bus. Its primary function is to intercept Intel486 microprocessor bus status and address signals, decode the bus access, and determine whether or not to process the bus request or allow the ISA bus controller to process it.

ISA Bus/System Controller Communication Channel

The asynchronous interface to the bus controller is handled by the group of signals listed in Table 4-19. These signals define the type of bus cycle to be run.

Table 4-19. Bus/System Controller Bus Cycle Types

CHM/IO*	CHS1*	CHS0*	Bus Cycle
0	0	0	INTA*
0	0	1	IOR*
0	1	0	IOW*
0	1	1	Reserved
1	0	0	REFRESH*
1	0	1	MEMR*
1	1	0	MEMW*
1	1	1	Reserved

DRAM Support Subsystem

The DRAM support subsystem provides RASBK*, CASBK, and LBE signals to each of the DRAM banks. Refer to Chapter 3, "Memory" for more information about DRAM.

I/O Control Registers

Table 4-20 lists the I/O port addresses for the system controller registers.

Table 4-20. Dedicated I/O Control Registers

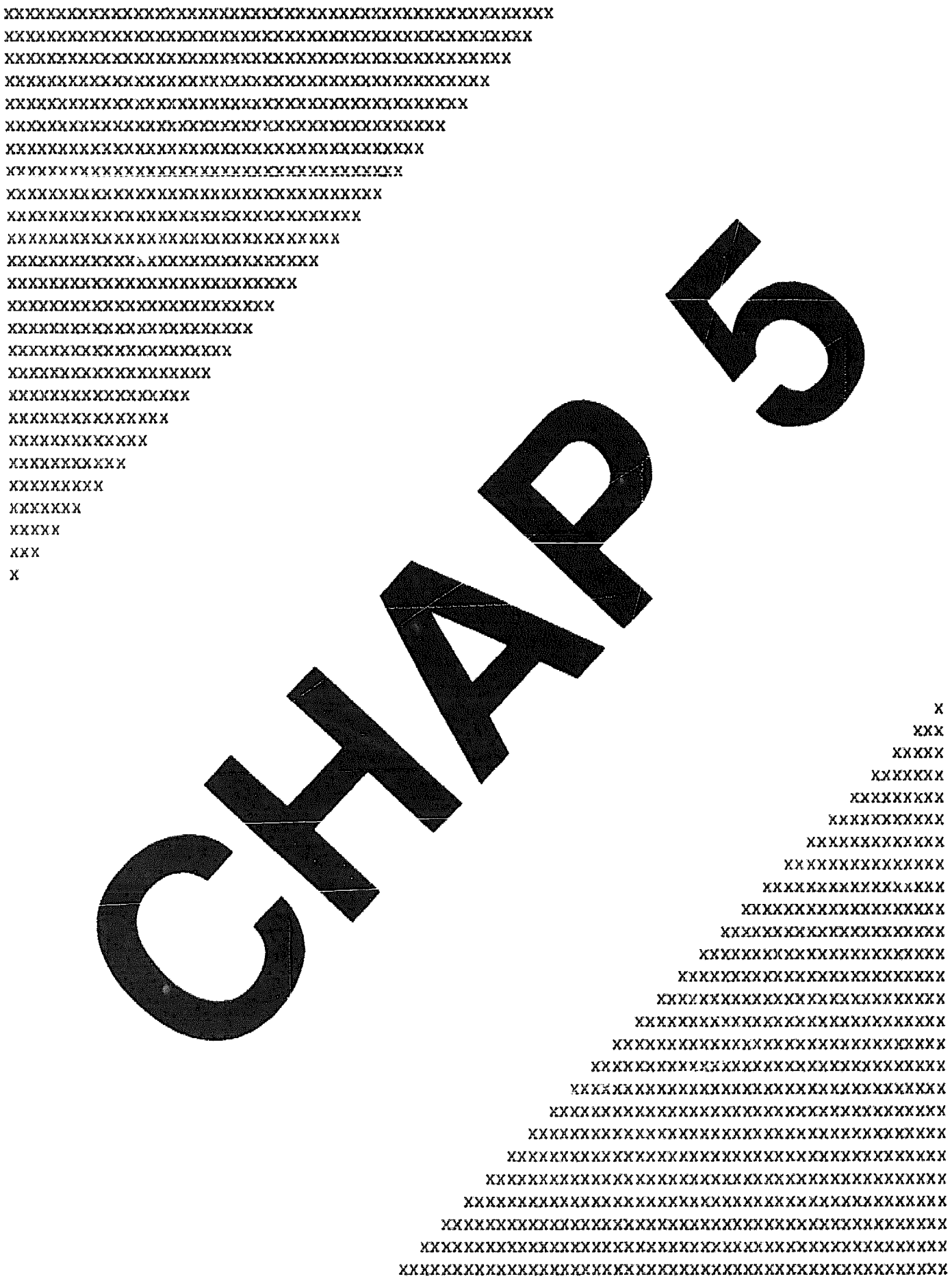
Port Address	Function
EBH:E8H	Not used
ECH	Configuration index register
EDH	Configuration data port
EEH	Fast A20
EFH	Fast reset
F4H	Slow CPU
F5H	Fast CPU
F9H	Configuration disable
FBH	Configuration enable

Halt/Shutdown Detection

The system controller detects and acts on Intel486 microprocessor halt and shutdown conditions. The signal levels listed in Table 4-21 determine the existence of halt and shutdown conditions.

Table 4-21. Halt/Shutdown Detection

Intel486 Mode	Signal Levels				
	M/IO*	D/C*	W/R*	BE0*	BE1*
Halt	1	0	1	1	0
Shutdown	1	0	1	0	1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5

82341 Peripheral Combo Controller

Introduction

The 82341 peripheral combo controller is a 128-pin integrated chip used in conjunction with the 82340DX ISA chip set. Its primary function is to provide peripheral support for the DECpc 433 Workstation system (see Figure 5-1). Supported peripherals include:

- Two software-compatible 16C450 UARTs (COM1 and COM2)
- One PS/2™ software-compatible bidirectional parallel port (LPT1)
- Control logic for Integrated Drive Electronics (IDE) support
- Seven programmable chip selects (three internal and four external)
- PS/2 compatible keyboard/mouse controller

The remainder of this chapter describes each of the supported peripherals in detail.

Serial Communications Ports

The peripheral combo controller contains two software-compatible 16C450 UARTs designated as COM1 and COM2. Both UARTs share a common baud rate of 1.8432 MHz and are internally accessed via chip selects CS1 and CS2.

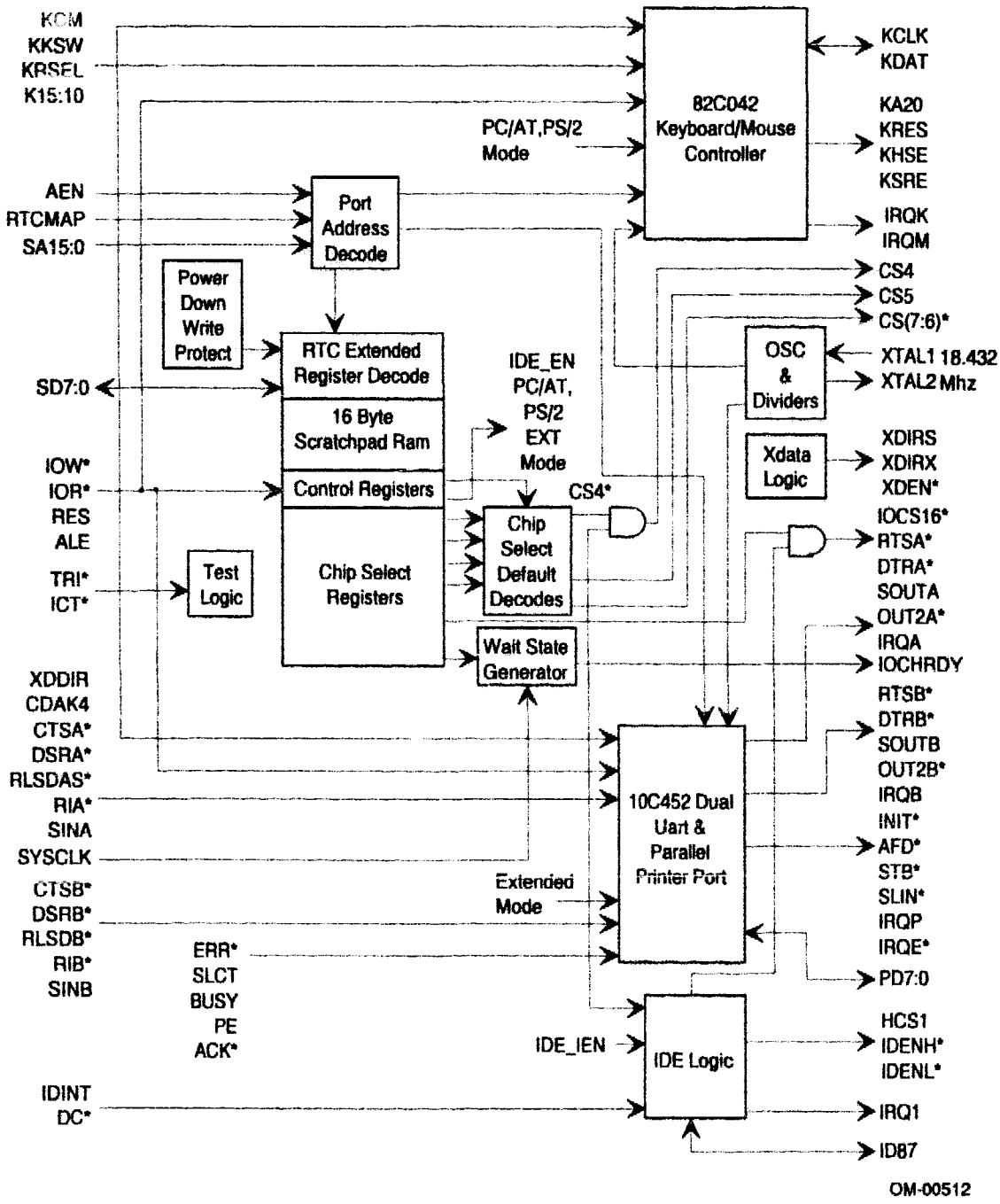


Figure 5-1. 82341 Combo Controller Functional Block Diagram

Serial Communications Ports Registers

Table 5-1 lists the registers used by the serial communications ports.

Table 5-1. Serial Communications Ports Registers

Reg Addr	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4
Bit	Receiver Buffer Register (read only)	Transmit Holding Register (write only)	Interrupt Enable Register	Interrupt Ident. Register (read only)	Line Control Register	Modem Control Register
7	Data bit 7	Data bit 7	0	0	DLAB	0
6	Data bit 6	Data bit 6	0	0	Set break	0
5	Data bit 5	Data bit 5	0	0	Stick parity	0
4	Data bit 4	Data bit 4	0	0	Even parity select	Loop
3	Data bit 3	Data bit 3	Modem status	0	Parity enable	Out two
2	Data bit 2	Data bit 2	Receiver line status	Interrupt ID bit one	No. of stop bits	Out one
1	Data bit 1	Data bit 1	Transmitter holding register empty	Interrupt ID bit zero	Word length select bit one	Request to send
0	Data bit 0	Data bit 0	Received data available	Zero if interrupt pending	Word length select bit zero	Data termina l ready

Table 5-1. Serial Communications Ports Registers *(continued)*

Reg Addr	5	6	7	0 DLAB = 1	1 DLAB = 1
Bit	**Line Status Register**	**Modem Status Register**	**Scratch Register**	**Divisor Latch (LS)**	**Divisor Latch (MS)**
7	0	Data carrier detect	Bit 7	Bit 7	Bit 15
6	Transmitter empty	Ring indicator	Bit 6	Bit 6	Bit 14
5	Transmitter holding register	Data set ready	Bit 5	Bit 5	Bit 13
4	Break interrupt	Clear to send	Bit 4	Bit 4	Bit 12
3	Framing error	Delta data carrier detect	Bit 3	Bit 3	Bit 11
2	Parity error	Trailing edge ring indicator	Bit 2	Bit 2	Bit 10
1	Overrun error	Delta data set ready	Bit 1	Bit 1	Bit 9
0	Data ready	Delta clear to send	Bit 0	Bit 0	Bit 8

Serial Communications Header

The J2A (COM1) and J2B (COM2) provide the serial communications channels for the DECpc 433 Workstation system. Table 5-2 lists the pinouts for J2A and J2B.

Table 5-2. Serial Communications Connector Pinouts

J2A/J2B Pin No.	Signal	Function
1 (J2A)	COM1DCD	Data carrier detect
2 (J2A)	COM1RXD*	Receive data
3 (J2A)	COM1TXD	Transmit data
4 (J2A)	COM1DTR*	Data terminal ready
5 (J2A)	GND	Ground
6 (J2A)	COM1DSR	Data set ready
7 (J2A)	COM1RTS*	Request to send
8 (J2A)	COM1CTS	Clear to send
9 (J2A)	COM1RING	Ring indicator
10 (J2B)	COM2DCD	Data carrier detect
11 (J2B)	COM2RXD*	Receive data
12 (J2B)	COM2TXD	Transmit data
13 (J2B)	COM2DTR*	Data terminal ready
14 (J2B)	GND	Ground
15 (J2B)	COM2DSR	Data set ready
16 (J2B)	COM2RTS*	Request to send
17 (J2B)	COM2CTS	Clear to send
18 (J2B)	COM2RING	Ring indicator
19	GND	Ground
20	GND	Ground

Parallel Printer Port

The parallel printer port contains the functionality of a 16C452 printer port plus a software programmable extended mode. This extended mode consists of a Direction Control Bit (DCB) and an Interrupt Status Bit (ISB). Both features are disabled at power-up and are enabled by clearing the EMODE* bit contained in control register zero. The parallel printer port is internally accessed via chip select CS3.

Parallel Printer Port Registers

The parallel printer port uses the following registers:

- Register zero — line printer port data
- Register one — LPT port status
- Register two — LPT port control

Line Printer Port Data Register

This register can be either unidirectional or bidirectional, depending on the state of the extended mode and data direction control bits. Each time EMODE* is deasserted, the line printer port data register returns the last data written to the LPT port; write operations immediately output data to the LPT port. Each time EMODE* is asserted, read operations return either the data last written to the LPT data register (if direction bit is set to zero) or the data present on the LPT port pins (if the direction bit is set to one). Write operations latch data into the output register and drive the LPT port (if the direction bit is set to output).

LPT Port Status

This read-only register contains interrupt status and real-time status for the LPT connector pins (refer to Table 5-3).

Table 5-3. LPT Port Status Bit Assignments

Bit	Function
7	BUSY*
6	ACK*
5	PE
4	SLCT
3	ERROR*
2	IRQ*
1	Reserved
0	Reserved

LPT Port Control

This read/write register controls the LPT direction and the printer control lines driven from the port. Write operations set or reset the bits listed in Table 5-4. Read operations return the status of the last write operation (except read only bit five).

Table 5-4. LPT Port Control Bit Assignments

Bit	Function
7	Reserved
6	Reserved
5	DIR (write-only)
4	IRQ EN
3	SLCT EN
2	INIT*
1	AUTO FD XT
0	STROBE

Parallel Printer Port Header

Header J4B provides the parallel printer port channel for the DECpc 433 Workstation. Table 5-5 lists header J4B's pinouts.

Table 5-5. Header J4B Pinouts

J15B Pin No.	Signal	Function
1	STB-R	Strobe
2	PRD0R	Printer data bit zero
3	PRD1R	Printer data bit one
4	PRD2R	Printer data bit two
5	PRD3R	Printer data bit three
6	PRD4R	Printer data bit four
7	PRD5R	Printer data bit five
8	PRD6R	Printer data bit six
9	PRD7R	Printer data bit seven
10	ACK*	Acknowledge
11	BUSY	Busy
12	PE	Paper end
13	SLCT	Select
14	AFD-R	Auto feed
15	ERR*	Error
16	INIT-R	Initialize printer
17	SLIN-R	Select input
18-27	GND	Ground

IDE Bus Interface Control

The peripheral combo controller provides the IDE bus control signals via signal IDE_EN, which corresponds to bit five of control register one (6AH). The peripheral combo controller also duplicates disk register bit one (I/O 3F6H) to enable IRQ1.

Chip Selects

The peripheral combo controller provides seven hard-wired default chip selects for the serial communications ports, parallel printer port, floppy disk, and hard disk. The chip selects are used after a reset until the battery-backed programmable values are enabled via control register 6AH bit three (refer to Table 5-6).

Table 5-6. Default Chip Select Addressing

Select/Device	Address
CS1 (COM1)	3F8H:3FFH (bit three of 69H = 1) 2F8H:2FFH (bit three of 69H = 0)
CS2 (COM2)	2F8H:2FFH (bit three of 69H = 1) 3F8H:3FFH (bit three of 69H = 0)
CS3 (LPT1)	03BCH:03BFH (bit five, six of 69H = 0, 0) 0378H:037BH (bit five, six of 69H = 1, 0) 0278H:027BH (bit five, six of 69H = 0, 1)
CS4* (floppy disk)	03F4H:03F5H
CS5* (hard disk)	01F0H:01F7H
CS6*	03F2H and IOW* active
CS7*	03F7H and IOW* active

Keyboard/Mouse Controller

The keyboard controller ROM contains the program required to support the PS/2 command set and 128 bytes of conversion code. Serial I/O is handled with receiver/transmitter hardware implementations that depend on an 8-bit timer for time-out detection.

User RAM support is also provided. This program writes a command 20-3FH (read) and 60-7FH (write) with the lower five bits representing the RAM address. Data from a read or write are accessed through port 60H DBB.

Keyboard/Mouse Interface

The keyboard/mouse interface consists of one register pair: ports 60H and 64H. Port 60H read operations output the contents of the output buffer to D7:0 and clear the status of the output buffer full bit. Port 60H write operations cause the input buffer to change. Command write operations are written to port 64H.

Keyboard/Mouse Port Interface Protocol

Data transmission to and from the keyboard and mouse consist of a synchronous bit stream over the data and clock lines (refer to Table 5-7).

Table 5-7. Interface Protocol Bit Assignments

Bit	Function
11	Stop bit (always one)
10	Parity bit (odd)
9	Data bit seven (MSB)
8:3	Data bits 6:1
2	Data bit zero (LSB)
1	Start bit (always 0)

Keyboard/Mouse Registers

Tables 5-8 and 5-9 list the bit assignments for the keyboard/mouse mode register and status register.

Table 5-8. Mode Register

Bit	Function
7	Reserved (always zero)
6	Keycode conversion 0 = no conversion 1 = conversion enabled
5	Disable mouse 0 = enabled 1 = disabled
4	Disable keyboard 0 = enabled 1 = disabled
3	Reserved (always zero)
2	System flag 0 sets status register two to zero 1 sets status register two to one
1	Enable mouse interrupt 0 = disabled 1 = enabled
0	Enable keyboard interrupt 0 = disabled 1 = enabled

Table 5-9. Status Register

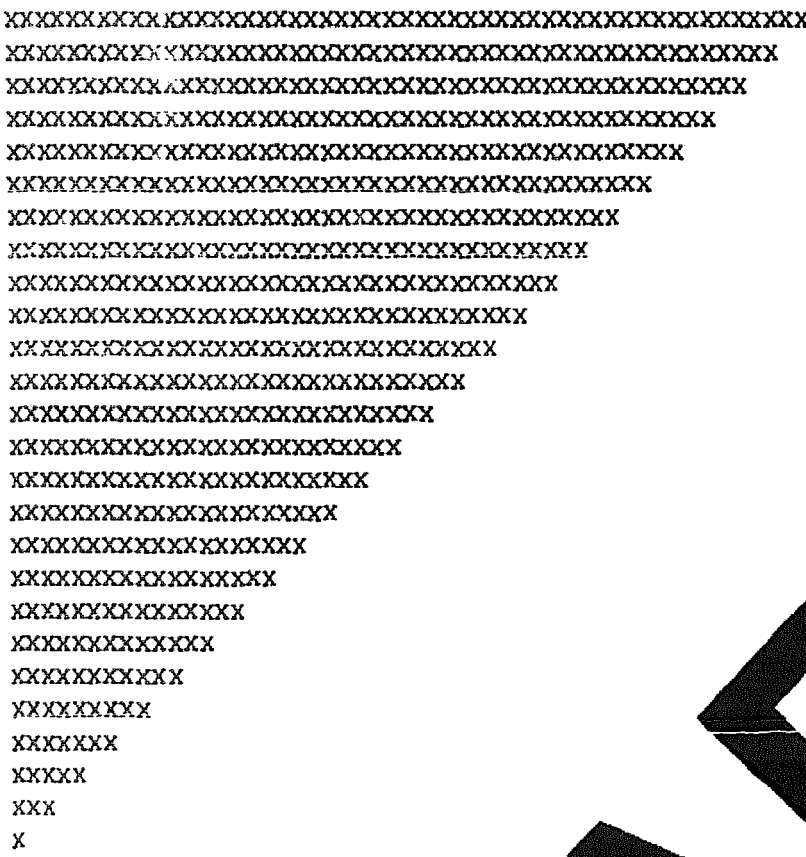
Bit	Function
7	Receive parity error 0 = normal 1 = parity error
6	General time-out 0 = normal 1 = time-out occurred
5	Output buffer source 0 = keyboard 1 = mouse
4	Keyboard enable 0 = disabled 1 = enabled
3	Command/data 0 = data or idle 1 = command or active
2	System flag 0 = hot reset did not occur 1 = hot reset occurred
1	Input buffer full 0 = empty 1 = full
0	Output buffer full 0 = empty 1 = full

Keyboard/Mouse Command Set

Table 5-10 lists the command set supported by the keyboard/mouse controller. Each command is implemented by writing the command byte to port 64H. Any subsequent data is read from or written to port 60H.

Table 5-10. Keyboard/Mouse Command Set

Command	Description	Command	Description
20	Read mode register	F0 to FF	Pulse output port (P27:20)
21 to 3F	Read keyboard controller RAM (byte 31:1)	A4	Test password
60	Write mode register	A5	Load password
61 to 7F	Write keyboard controller RAM (byte 31:1)	A6	Enable password
AA	Self test	A7	Disable mouse
AB	Kbd interface test	A8	Enable mouse
AC	Diagnostic dump	A9	Mouse interface test
AD	Disable keyboard	C1	Poll-in port low (P13:10 -> S7:4)
AE	Enable keyboard	C2	Poll-in port high (P17:14 -> S7:4)
C0	Read input port (P17:10)	D1	Write output port
D0	Read output port (P27:20)	D2	Write keyboard output buffer
D1	Write output port	D3	Write mouse output buffer
E0	Read test inputs 0(T1:0)	D4	Write to mouse



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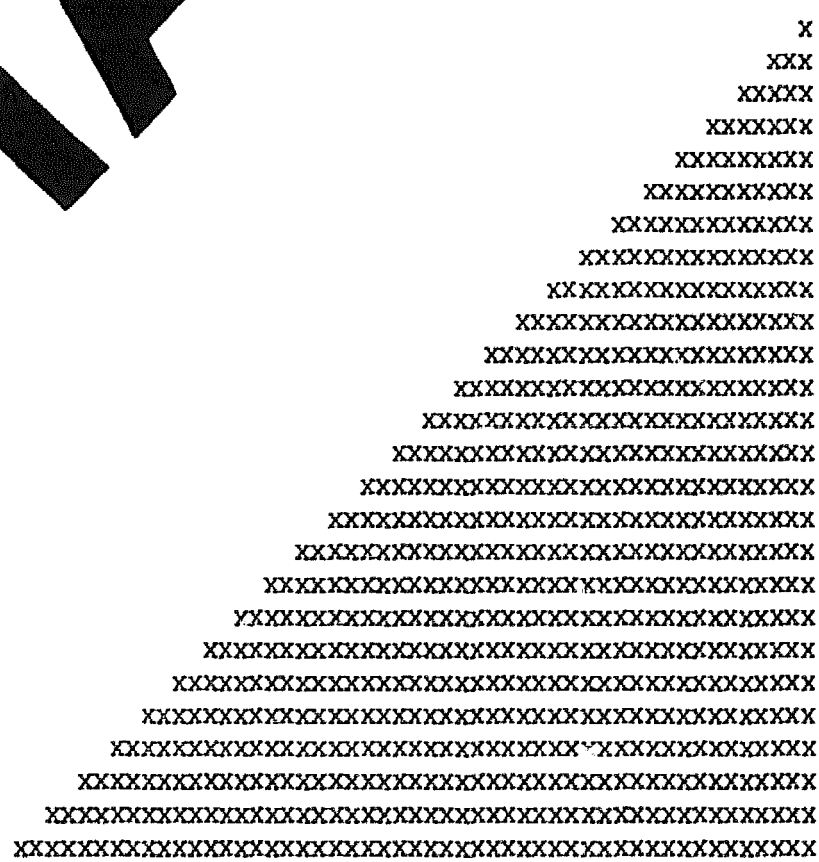


6

AIC-6260 SCSI Controller

Introduction

The Adaptec AIC-6260 onboard SCSI-2 controller manages the SCSI bus, including SCSI transfers and control signal decode/generation. SCSI-2 is functionally the same as SCSI; however, the interface speed is faster. The controller is primarily made up of SCSI status and transfer control registers data latch registers, and registers that provide the Intel486 microprocessor with direct access to and control over the SCSI bus. Figure 6-1 shows a block diagram of the SCSI controller.

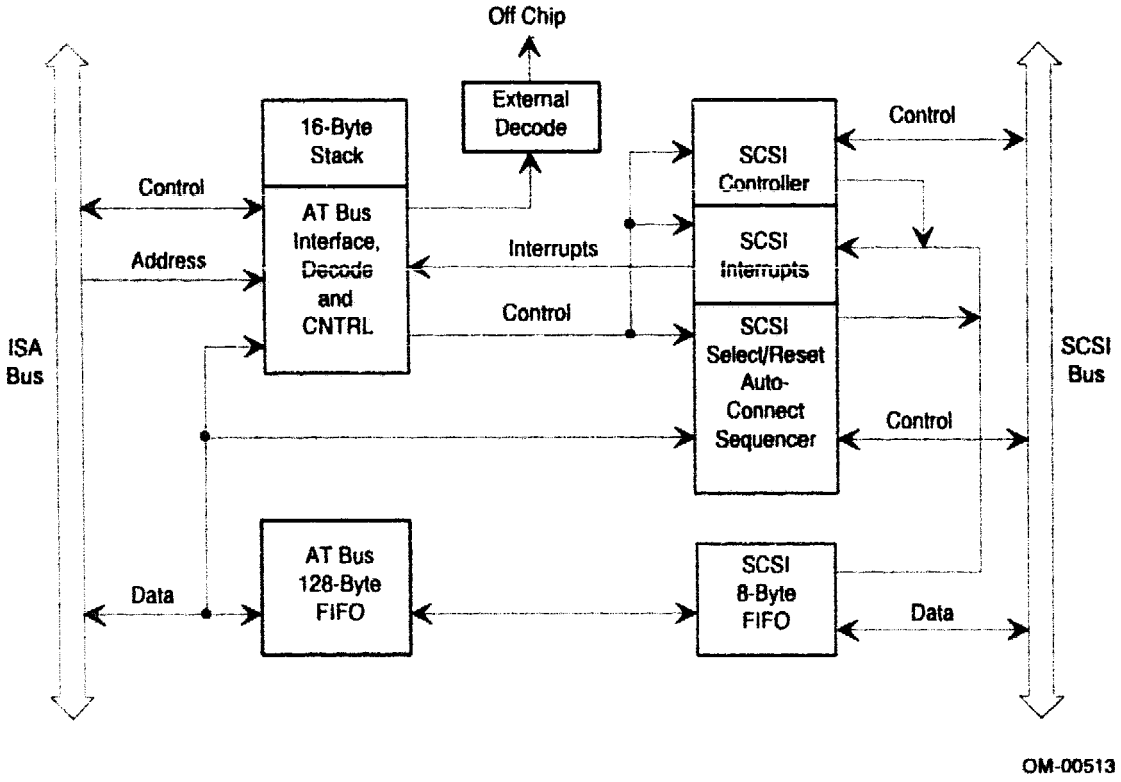


Figure 6-1. SCSI Controller Functional Block Diagram

Interrupt Logic

This logic provides interrupt masking, generation, and clearing for all interrupts relating to SCSI activity. The logic includes interrupt mask registers, interrupt clear registers, and status registers.

Select/Reselect Sequencer

This block provides automatic SCSI select and reselect sequences to eliminate the need for Intel486 microprocessor intervention.

FIFO

This FIFO (first-in-first-out) eight byte data buffer is used during normal mode data transfers. Its only purpose is to hold data during synchronous data transfers.

External Decode Logic

This logic provides the interface for two general purpose I/O ports. This logic must be supported off-chip.

ISA Bus Interface, Decode, and Control

This logic provides the interface to the ISA bus control signals. It also gives the address decoding for access to internal registers.

ISA Bus FIFO

This 128-byte data buffer holds data that is passed between the ISA bus and SCSI FIFO (except during SCSI PIO transfers).

Controller Registers

This section provides information on the SCSI controller's internal registers. Throughout this section, each register is described under its own heading and is identified by name and address.

There are 32 registers normally decoded from 340H through 35EH. If ALTERNATE* is asserted, the registers are decoded from 140H. All registers are written to and read from the Intel486 microprocessor I/O address space.

SCSI Sequence Control

This read/write register controls the selection/reselection process for the SCSI controller. Each bit enables a different portion of the selection/reselection process and can be read to allow bit manipulation instructions without saving a register in local scratch RAM. All bits (except bit zero) are cleared by a SCSI reset. Refer to Table 6-1 for bit assignments.

Table 6-1. SCSI Sequence Control Register

Bit	Signal Mnemonic	Signal Name
7	TEMODEO	Target enable mode out
6	ENSELO	Enable selection out
5	ENSELI	Enable selection in
4	ENRESELI	Enable reselection in
3	ENAUTOATNO	Enable auto attention out
2	ENAUTOANTI	Enable auto attention in
1	ENAUTOATNP	Enable auto attention parity
0	SCIRSTO	SCSI reset out

SCSI Transfer Control 0

This register enables transfers between the SCSI bus and the Intel486 microprocessor via the SCSI and ISA bus FIFOs, controls the selection of SCSI PIO as the transfer mode, and clears the SCSI FIFO and SCSI transfer counter. Refer to Table 6-2 for bit assignments.

Table 6-2. SCSI Transfer Control 0 Register

Bit	Signal Mnemonic	Signal Name
7	SCSIEN	Transfer enable
6	DMAEN	FIFO transfer enable
5	CH1/CH2	Channel select
4	CLRSTCNT	Clear SCSI transfer counter
3	SPIOEN	SCSI PIO enable
2	RSVD	Reserved
1	CLRCH1	Clear channel one
0	RSVD	Reserved

SCSI Transfer Control 1

This register enables various transfer controls associated with SCSI transfers. This register also controls the selection/reselection timer, byte alignment, and parity checking. Refer to Table 6-3 for bit assignments.

Table 6-3. SCSI Transfer Control 1 Register

Bit	Signal Mnemonic	Signal Name
7	BITBUCKET	SCSI bit bucket mode
6	SWRAPEN	SCSI wrap enable
5	ENSPCHK	Enable parity check
4:3	STIMESEL	Set selection timeout
2	ENSTIMER	Enable selection timer
1	BYTEALIGN	Byte align
0	RSVD	Reserved

SCSI Signal In

This register reflects the current state of the SCSI control lines on the SCSI bus. Refer to Table 6-4 for bit assignments.

Table 6-4. SCSI Signal In Register

Bit	Signal Mnemonic	Signal Name
7	CDI	Command/data in
6	IOI	Input/output in
5	MSGI	Message in
4	ATNI	Attention in
3	SELI	Selection in
2	BSYI	Busy in
1	REQI	Request in
0	ACKI	Acknowledge in

SCSI Signal Out

This register controls the actual or expected state of the SCSI control lines, depending on whether the SCSI controller is in target or initiator mode. All bits are cleared by bus free reset or hard reset conditions. Refer to Table 6-5 for bit assignments.

Table 6-5. SCSI Signal Out Register

Bit	Signal Mnemonic	Signal Name
7	CDO	Command/data out
6	IOO	Input/output out
5	MSGO	Message out
4	ATNO	Attention out
3	SELO	Selection out
2	BSYO	Busy out
1	REQO	Request out
0	ACKO	Acknowledge out

SCSI Rate Control

This rate control register controls the timing and offset parameters for synchronous SCSI transfers. Refer to Table 6-6 for bit assignments.

Table 6-6. SCSI Rate Control Register

Bit	Signal Mnemonic	Signal Name
7	RSVD	Reserved
6:4	SXFR	Synchronous transfer rate
3:0	SOFS	SCSI offset

Selection/Reselection ID

Each time the SCSI controller is selected or reselected, the SCSI ID bits of the target and the initiator are set in this register. Refer to Table 6-7 for bit assignments.

Table 6-7. SCSI Selection/Reselection ID Register

Bit	Signal Mnemonic	Signal Name
7	SELID7	Select ID seven
6	SELID6	Select ID six
5	SELID5	Select ID five
4	SELID4	Select ID four
3	SELID3	Select ID three
2	SELID2	Select ID two
1	SELID1	Select ID one
0	SELID0	Select ID zero

SCSI ID

This register contains the SCSI IDs of the SCSI controller and the other target or initiator involved in the SCSI operation. Refer to Table 6-8 for bit assignments.

Table 6-8. SCSI ID Register

Bit	Signal Mnemonic	Signal Name
7	RSVD	Reserved
6:4	OID	Own ID
3	RSVD	Reserved
2:0	TID	Other ID

SCSI Latched Data

This register is the data latch used for manual or SCSI PIO data transfers. Outbound data is written to this register; inbound data is read from it. Refer to Table 6-9 for bit assignments.

Table 6-9. SCSI Latched Data Register

Bit	Signal Mnemonic	Signal Name
7	DB7	Data bit seven
6	DB6	Data bit six
5	DB5	Data bit five
4	DB4	Data bit four
3	DB3	Data bit three
2	DB2	Data bit two
1	DB1	Data bit one
0	DB0	Data bit zero

SCSI Data Bus

This register reflects the current state of the SCSI data bus lines. It is used during manual selection or reselection. Refer to Table 6-10 for bit assignments.

Table 6-10. SCSI Data Bus Register

Bit	Signal Mnemonic	Signal Name
7	SDB7 (MSB)	SCSI data bit seven
6	SDB6	SCSI data bit six
5	SDB5	SCSI data bit five
4	SDB4	SCSI data bit four
3	SDB3	SCSI data bit three
2	SDB2	SCSI data bit two
1	SDB1	SCSI data bit one
0	SDB0 (LSB)	SCSI data bit zero

SCSI Transfer Count 2:0

The transfer count register consists of three 8-bit registers: SCSI transfer count 2:0. These registers contain the data transfer count for the current SCSI operation. The LSB is loaded at 348H; the MSB is loaded at 34AH. Refer to Table 6-11 for bit assignments.

Table 6-11. SCSI Transfer Count 2:0 Register

Bit	Signal Mnemonic	Signal Name
23:16	STCNT2	Most significant byte (34AH)
15:8	STCNT1	Middle byte (349H)
7:0	STCNT0	Least significant byte (348H)

SCSI Status 0

This register reflects the state of eight SCSI status bits. Refer to Table 6-12 for bit assignments.

Table 6-12. SCSI Status 0 Register

Bit	Signal Mnemonic	Signal Name
7	TARGET	Target
6	SELDO	Select out done
5	SELDI	Select in done
4	SELINGO	Selection initiated out
3	SWRAP	Transfer counter wrap
2	SDONE	SCSI done
1	SPIORDY	SCSI PIO ready
0	DMADONE	DMA done

Clear SCSI Interrupts 0

This register (except bit seven) clears the interrupts associated with the status bits in the SCSI status 0 register. Setting these bits clears the corresponding interrupt and deasserts IRQ. Refer to Table 6-13 for bit assignments.

Table 6-13. Clear SCSI Interrupt 0 Bit Assignments

Bit	Signal Mnemonic	Signal Name
7	SETSDONE	Set SCSI transfer done
6	CLRSELDO	Clear select out done
5	CLRSELDI	Clear select in done
4	CLRSELINGO	Clear select initiated out
3	CLRSWRAP	Clear transfer counter wrap
2	CLRSDONE	Clear SCSI done
1	CLRSPIORDY	Clear SCSI PIO ready
0	CLRDMADONE	Clear DMA done

SCSI Status 1

This register reflects the state of eight SCSI status bits. If the interrupts corresponding to these bits are enabled, interrupts are generated each time the status bits are set. Refer to Table 6-14 for bit assignments.

Table 6-14. SCSI Status 1 Register

Bit	Signal Mnemonic	Signal Name
7	SELTO	Selection timeout expired
6	ATNTARG	Target attention
5	SCSIRSTI	SCSI reset in
4	PHASEMIS	Phase mismatch
3	BUSFREE	Bus free
2	SCSIPERR	Parity error
1	PHASECHG	Phase change
0	REQINIT	REQ initiated

Clear SCSI Interrupts 1

This clears the interrupts associated with the status bits in the SCSI status 1 register. Setting any of these bits (except bit six) clears the corresponding interrupt and deasserts IRQ. Refer to Table 6-15 for bit assignments.

Table 6-15. Clear SCSI Interrupts 1 Register

Bit	Signal Mnemonic	Signal Name
7	CLRSELTIMO	Clear selection timeout
6	CLRANTO	Clear attention out
5	CLRSCSIRSTI	Clear SCSI reset in
4	RSVD	Reserved
3	CLRBUSFREE	Clear bus free
2	CLRSCSIPERR	Clear parity error
1	CLRPHASECHG	Clear phase change
0	CLRREQINIT	Clear REQ initiated

SCSI Status 2

This register reflects the status of the SCSI FIFO. Refer to Table 6-16 for bit assignments.

Table 6-16. SCSI Status 2 Register

Bit	Signal Mnemonic	Signal Name
7:6	RSVD	Reserved
5	SOFFSET	SCSI offset
4	SEMPTY	SCSI FIFO empty
3	SFULL	SCSI FIFO full
2:0	SFCNT	SCSI FIFO count

SCSI Status 3

This register contains status information on the state of the current synchronous SCSI transfer. Refer to Table 6-17 for bit assignments.

NOTE

Do not read this register until all transfers are complete.

Table 6-17. SCSI Status 3 Register

Bit	Signal Mnemonic	Signal Name
7:4	SCSICNT	Count difference
3:0	OFFCNT	Offset count

SCSI Status 4

This register contains status information on error conditions for the current SCSI transfer. Refer to Table 6-18 for bit assignments.

Table 6-18. SCSI Status 4 Register

Bit	Signal Mnemonic	Signal Name
7:3	RSVD	Reserved
2	SYNCERR	Synchronous transfer error
1	FWERR	FIFO write error
0	FRERR	FIFO read error

Clear SCSI Errors

This register clears the error condition status bits in the SCSI status 4 register. Refer to Table 6-19 for bit assignments.

Table 6-19. Clear SCSI Errors Register

Bit	Signal Mnemonic	Signal Name
7:3	RSVD	Reserved
2	CLRSYNCERR	Clear synchronous transfer error
1	CLRFWERR	Clear FIFO write error
0	CLRFRERR	Clear FIFO read error

SCSI Interrupt Mode 0

This register enables the interrupts associated with the status bits in the SCSI status 0 register. Refer to Table 6-20 for bit assignments.

Table 6-20. SCSI Interrupt Mode 0 Register

Bit	Signal Mnemonic	Signal Name
7	RSVD	Reserved
6	ENSELDO	Enable selection done out interrupt
5	ENSELDI	Enable selection done in interrupt
4	ENSELINGO	Enable initiate selection interrupt
3	ENSWRAP	Enable wrap interrupt
2	ENSDONE	Enable SCSI done interrupt
1	ENSPIORDY	Enable SCSI PIO ready interrupt
0	ENDMADONE	Enable DMA done interrupt

SCSI Interrupt Mode 1

This register enables the interrupts associated with the status bits in the SCSI status 1 register. Refer to Table 6-21 for bit assignments.

Table 6-21. SCSI Interrupt Mode 1 Register

Bit	Signal Mnemonic	Signal Name
7	ENSELTIMO	Enable selection timeout interrupt
6	ENATNTARG	Enable target attention interrupt
5	ENSCSIRST	Enable SCSI reset interrupt
4	ENPHASEMIS	Enable phase mismatch interrupt
3	ENBUSFREE	Enable bus free interrupt
2	ENSCSIPERR	Enable SCSI parity error interrupt
1	ENPHASECHG	Enable phase change interrupt
0	ENREQINIT	Enable REQ initiated interrupt

DMA Control 0

This register contains the basic controls for PIO and DMA transfer modes. Refer to Table 6-22 for bit assignments.

Table 6-22. DMA Control 0 Register

Bit	Signal Mnemonic	Signal Name
7	ENDMA	Enable DMA
6	8BIT/16BIT*	8-bit/16-bit* mode
5	DMA/PIO*	DMA/PIO* mode
4	RSVD	Reserved
3	WRITE/READ*	Transfer direction
2	INTEN	Master interrupt enable
1	RSTFIFO	Reset FIFO counter
0	SWINT	Software interrupt

DMA Control 1

This register is used to set the power-down feature and write to the stack offset pointer. Refer to Table 6-23 for bit assignments.

Table 6-23. DMA Control 1 Register

Bit	Signal Mnemonic	Signal Name
7	PWRDWN	Power down
6:4	RSVD	Reserved
3:0	STK	Stack offset pointer

DMA Status

This register reflects the real-time status of the current DMA or PIO transfer. Refer to Table 6-24 for bit assignments.

Table 6-24. DMA Status Register

Bit	Signal Mnemonic	Signal Name
7	ATDONE	Intel486 microprocessor done
6	WORDRDY	Word ready
5	INTSTAT	Interrupt status
4	DFIFOFULL	Intel486 microprocessor FIFO full
3	DFIFOEMP	Intel486 microprocessor empty
2:0	RSVD	Reserved

FIFO Status

This register provides a count of the current number of bytes in the Intel486 microprocessor FIFO. Refer to Table 6-25 for bit assignments.

Table 6-25. FIFO Status Register

Bit	Signal Mnemonic	Signal Name
7	FCNT7 (MSB)	FIFO count seven
6	FCNT6	FIFO count six
5	FCNT5	FIFO count five
4	FCNT4	FIFO count four
3	FCNT3	FIFO count three
2	FCNT2	FIFO count two
1	FCNT1	FIFO count one
0	FCNT0 (LSB)	FIFO count zero

Data Port High/Low

Data transfers between the SCSI controller and the Intel486 microprocessor take place through the data port high/low register in both DMA and PIO mode. Refer to Table 6-26 for bit assignments.

Table 6-26. Data Port High/Low Register

Bit	Signal Mnemonic	Signal Name
15:8	DATAH	High-order data byte
7:0	DATAL	Low-order data byte

Burst Control

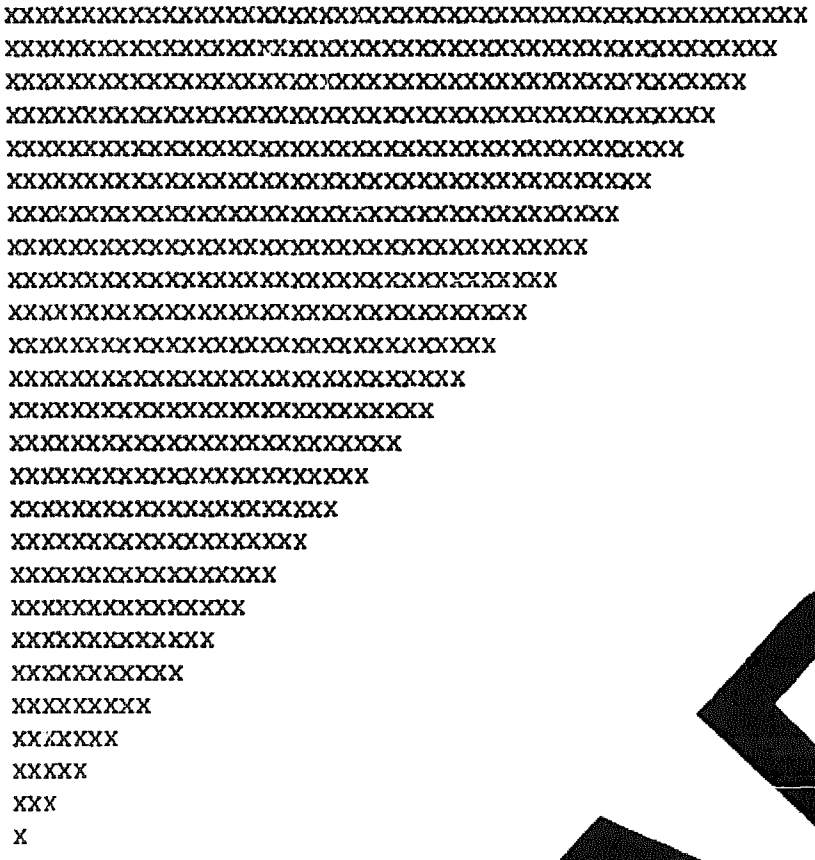
This register controls the burst on and burst off times for DMA transfers. Refer to Table 6-27 for bit assignments.

Table 6-27. Burst Control

Bit	Signal Mnemonic	Signal Name
7:4	BON	Burst on
3:0	BOFF	Burst off

Stack (35DH)

This 16-byte stack register is used for general purpose memory. It is addressed by writing to the lower four bits of the DMA control 1 register.



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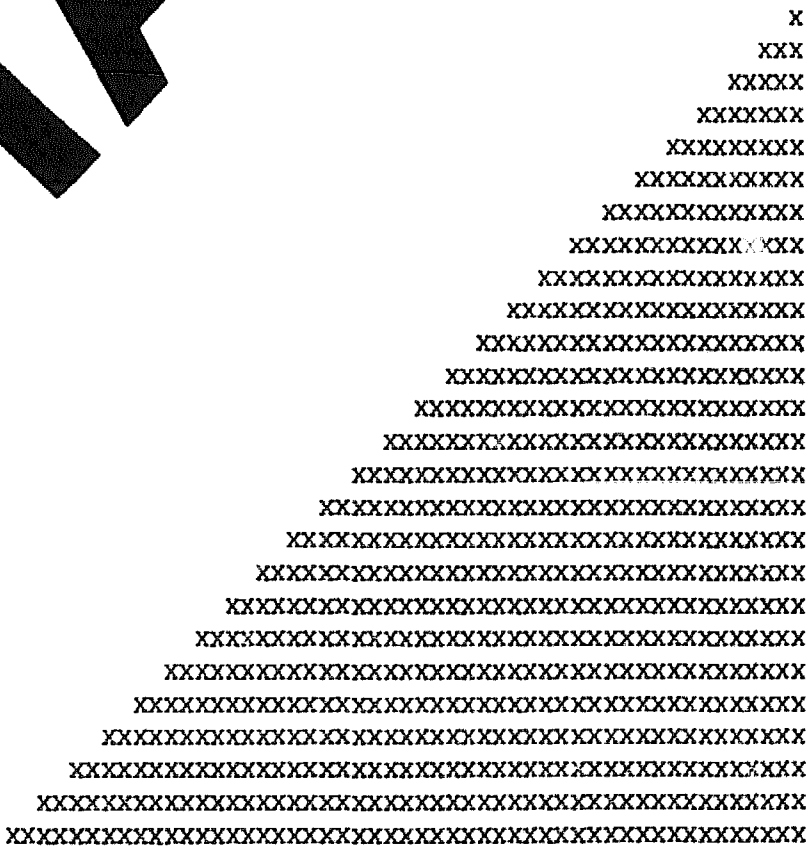


7

82077AA Floppy Disk Controller

Introduction

The DECpc 433 Workstation system board contains an integrated 82077AA Floppy Disk Controller (FDC) operating in AT mode. The FDC contains all the logic required for floppy disk control and provides the connection between the onboard ISA bus and the floppy disk drive connector. Figure 7-1 shows a block diagram of the FDC.

Functional Description

The FDC consists of the following functional units:

- FIFO
- Interface logic
- Serial interface logic
- Drive interface controller
- General registers

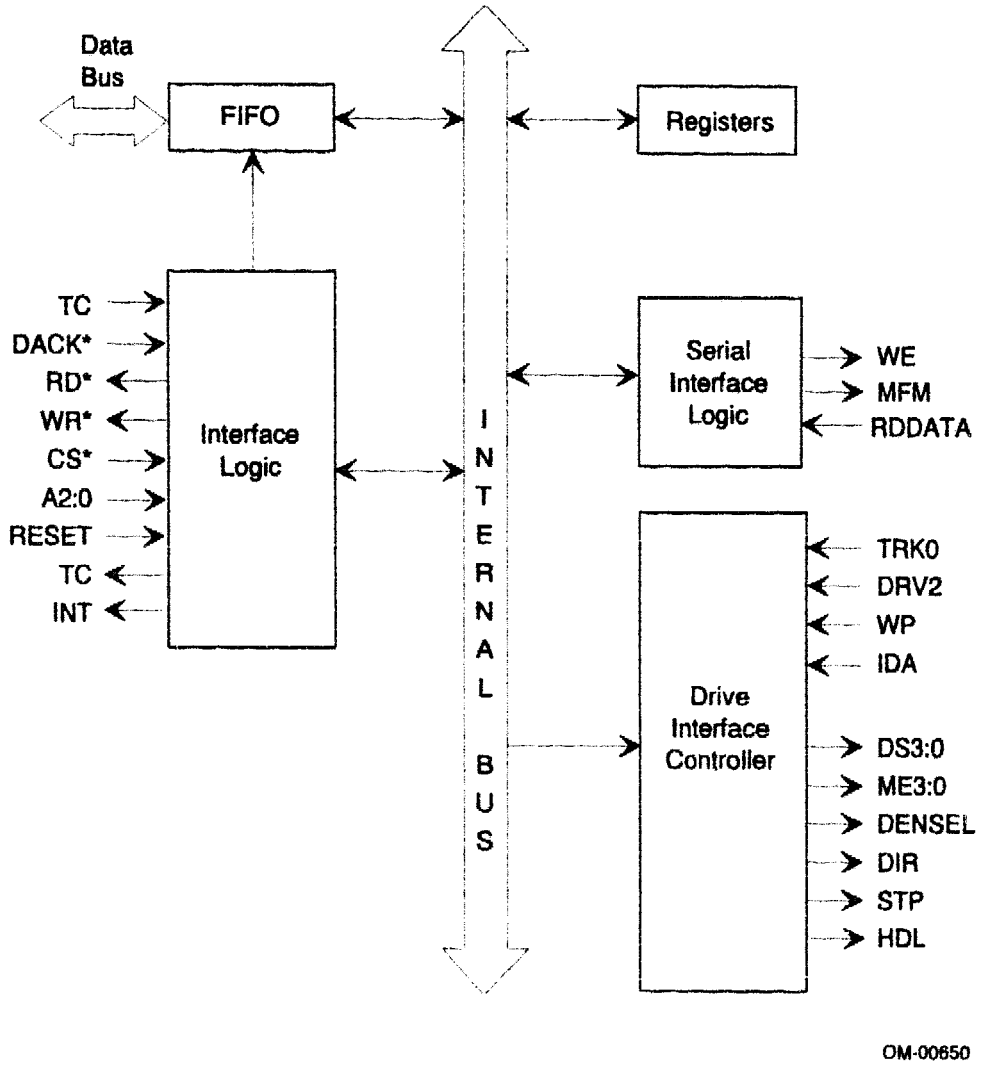


Figure 7-1. Floppy Disk Controller Block Diagram

FIFO

This 16-byte FIFO (first-in-first-out) is the gateway to the FDC. All command data and disk data goes through the FIFO. In addition, the FIFO has programmable threshold values.

Interface Logic

The interface logic receives the asynchronous CPU signals TC, DACK*, RD*, WR*, CS*, and A2:0. Outputs TC and INT cause the current disk transfer to terminate or cause an interrupt.

Serial Interface Logic

The serial interface logic controls data flow between the internal bus and the floppy disk drive. During read operations, serial data (RDDATA) is received from the floppy disk drive. During write operations, serial data (WRDATA) and write enable (WE) are output to the floppy disk drive.

Drive Interface Controller

The drive interface controller outputs the various control signals for the floppy disk drive. It also receives index (IDX), track 0 (TRK0), and write protect (WP) signals from the floppy disk drive. Input signal DRV2 indicates the presence of a second disk drive.

General Registers

Six general registers control FDC operations. They are accessed between addresses 3F0H and 3F7H. Table 7-1 lists the FDC register I/O addresses, specifies the I/O function required to access the registers, and briefly describes the registers. The following registers control FDC operations in AT mode:

- Digital output register (DOR)
- Tape drive register (TDR)
- Main status register (MSR)
- Data rate select register (DSR)
- Data register (FIFO)
- Digital input/configuration control register (DIR/CCR)

Table 7-1. FDC Register Address Map

Address	I/O Function	Register	Description
3F0H			Reserved
3F1H			Reserved
3F2H	Read/write	DOR	Digital output register
3F3H	Read/write	TSR	Tape drive register
3F4H	Read	MSR	Main Status register
3F4H	Write	DSR	Data rate select register
3F5H	Read/write	FIFO	Data register
3F6H			Reserved
3F7H	Read	DIR	Digital input register
3F7H	Write	CCR	Configuration control register

Digital Output Register

This read/write register contains the motor enable bits, a DMA gate bit, a reset bit, and drive selection bits. Refer to Table 7-2 for bit assignments.

Table 7-2. Digital Output Register (DOR) Bit Assignments

Bit	Signal Mnemonic	Function
7:4	MOT EN3:0	Motor enable 3:0
3	DMAGATE*	DMA gate
2	RESET*	Reset
1:0	DRIVE SEL1:0	Drive select 1:0

Tape Drive Register

This read/write register selects one of three possible tape drives (tape drive 1, 2, or 3). Refer to Table 7-3 for bit assignments.

Table 7-3. Tape Drive Register (TDR) Bit Assignments

Bit	Signal Mnemonic	Function
7:2	Reserved	
1:0	Tape SEL1:0	Tape drive select 1:0

Main Status Register

This read only register controls the data input and output modes. It also passes ready information to the Intel486 microprocessor. Refer to Table 7-4 for bit assignments.

Table 7-4. Main Status Register (MSR) Bit Assignments

Bit	Signal Mnemonic	Function
7	RQM	Request for master
6	DIO	Data in/out
5	NON DMA	Non DMA
4	CMD BUSY	Command busy
3	DRV 3 BUSY	Drive 3 busy
2	DRV 2 BUSY	Drive 2 busy
1	DRV 1 BUSY	Drive 1 busy
0	DRV 0 BUSY	Drive 0 busy

Data Rate Select Register

This write only register specifies the data transfer rate and precompensation delay for data transfers between the controller and the floppy disk drive. It also contains power down and software reset information. Refer to Table 7-5 for bit assignments.

Table 7-5. Data Select Rate (DSR) Register Bit Assignments

Bit	Signal Mnemonic	Function
7	S/W RESET	Software reset
6	POWER DOWN	Power down
5	Reserved	
4:2	PRECOMP 2:0	Precompensation selection
1:0	DRATE SEL 1:0	Data rate selection

Data Register

This read/write register is also the FIFO. All data and command information passes through the data register.

Digital Input Register

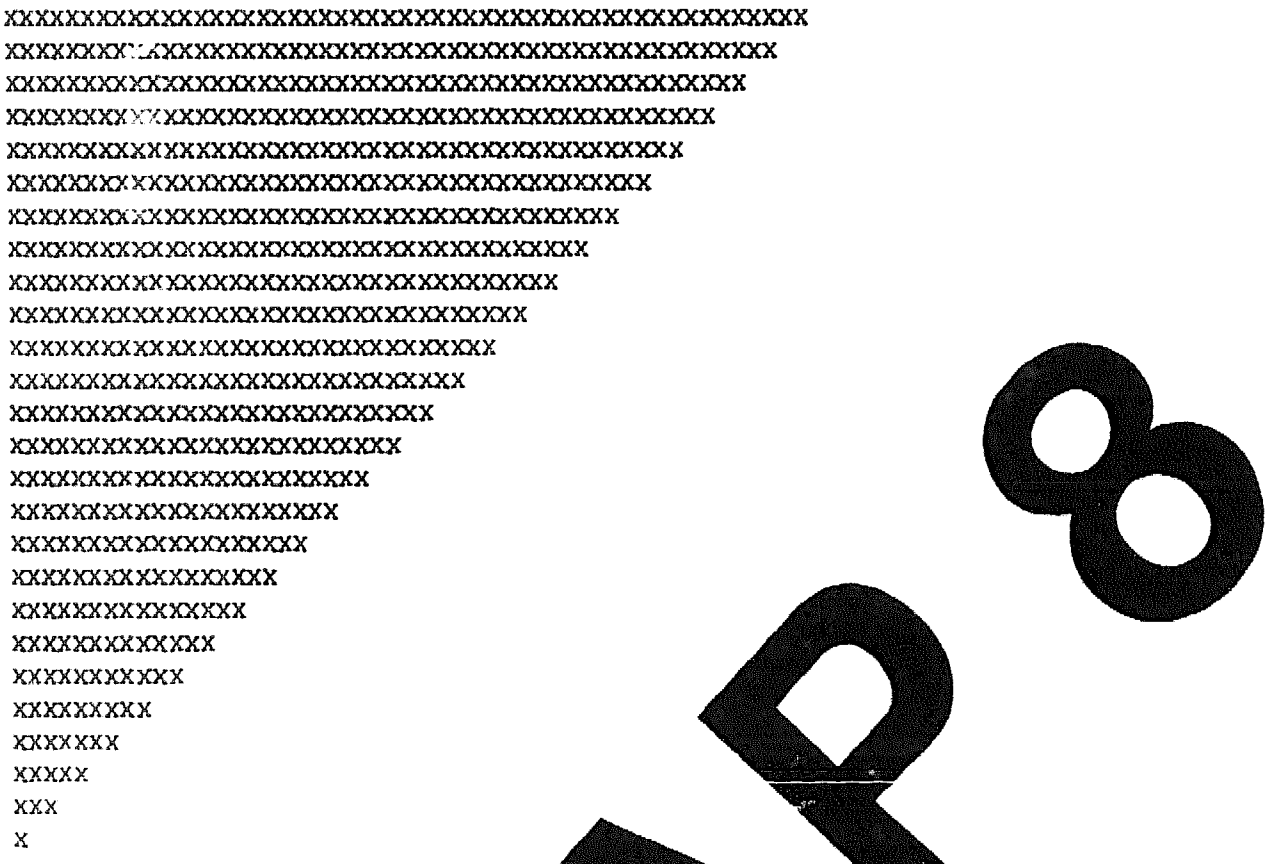
This read only register senses the state of the DSKCHG at bit 7. All other bits are tristated.

Configuration Control Register

This write only register sets the data rate. Refer to Table 7-6 for bit assignments.

Table 7-6. Config Control Register (CCR) Bit Assignments

Bit	Signal Mnemonic	Function
7:2	Reserved	
1:0	DRATE SEL 1:0	Data rate selection 1:0



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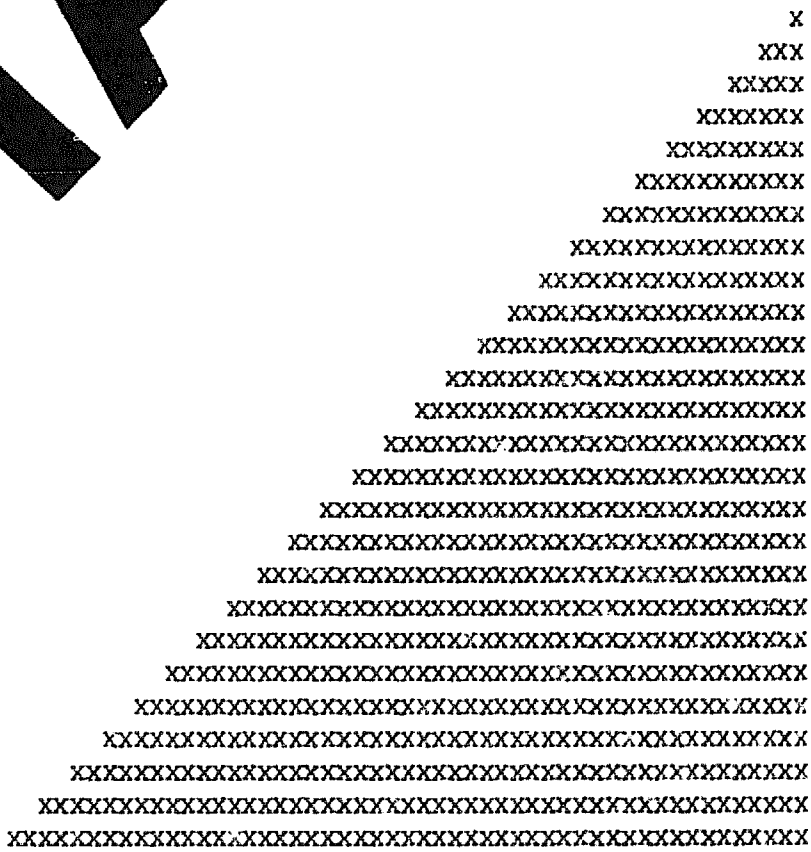


8

Ethernet LAN Subsystem

Introduction

The DECpc 433 Ethernet Workstation system board contains an integrated Ethernet LAN subsystem that handles either ThinWire or Twisted Pair Ethernet LAN transmissions. A pushbutton switch selects the cable type and routes signals to the appropriate hardware. Figure 8-1 shows a block diagram of the Ethernet LAN subsystem.

Functional Description

The Ethernet LAN subsystem consists of the following functional units:

- ThinWire interface
- Twisted pair interface
- LANCE controller
- ISA bus interface
- Network buffer RAM
- LAN address MUX
- DLL ROM
- Ethernet address ROM
- Data buffer

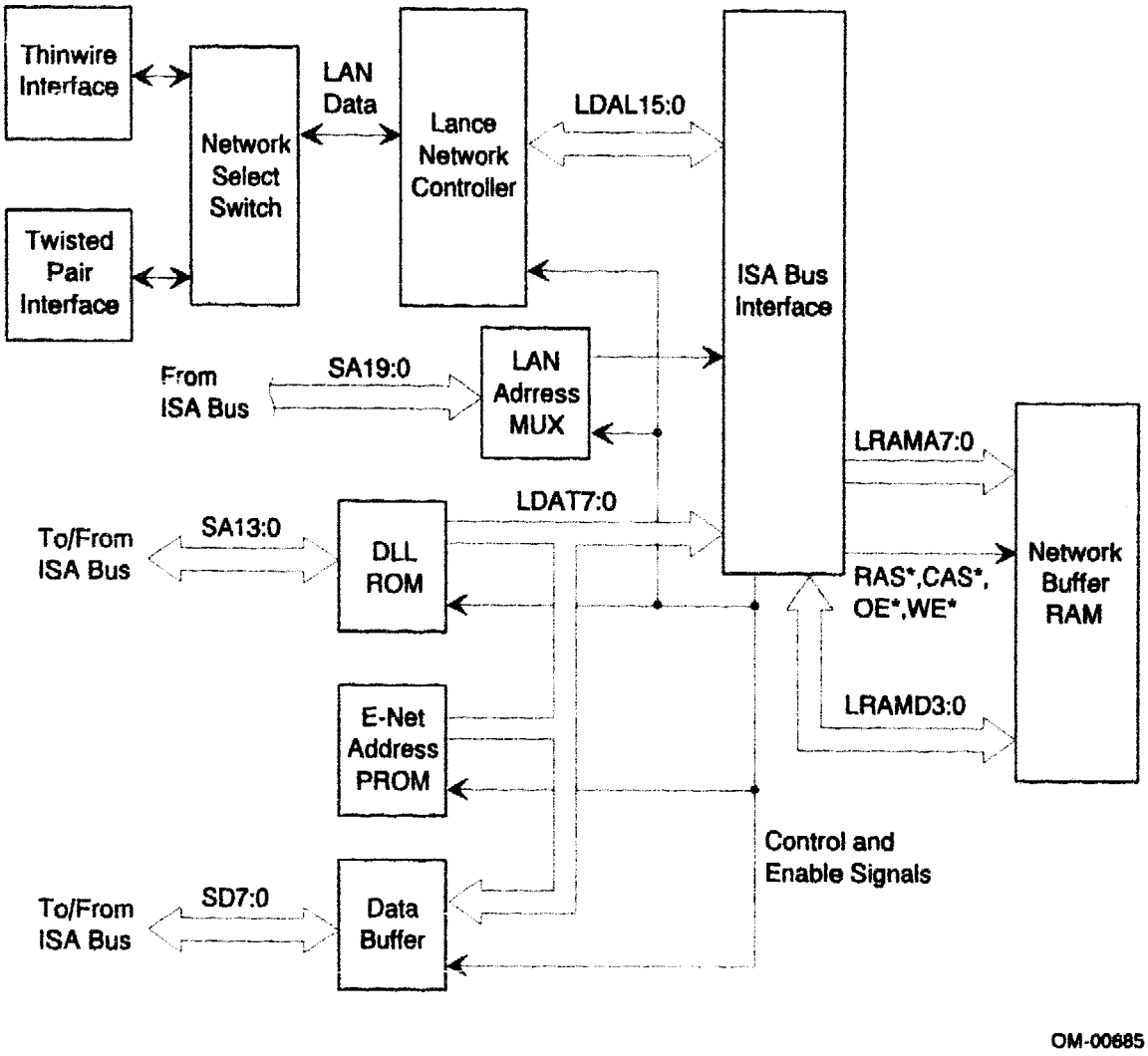


Figure 8-1. Ethernet LAN Subsystem Block Diagram

ThinWire Interface

The ThinWire interface receives and transmits LAN information transmitted via coax cable. It also protects against "jabber" by disabling data transmission when data packet transmission time exceeds LAN specifications. Connections to the LAN interface is via a BNC connector.

Twisted Pair Interface

The twisted pair interface receives and transmits LAN information transmitted via twisted pair wire. It also protects against "jabber" by disabling data transmission when data packet transmission time exceeds LAN specification. Connections to the LAN interface is through a MJ8 connector.

LANCE Controller

The LANCE (Local Area Network Controller for Ethernet) manages data packet transfers between either the ThinWire interface or twisted pair interface and the ISA bus interface. Its primary task is to convert the received serial data packets into a parallel 16-bit word and vice versa. The LANCE receives enable and control signals from the ISA bus interface.

ISA Bus Interface

The ISA bus interface provides the interface between the LANCE and the ISA bus. Interface with the LANCE is in word format (16-bit). Interface with the ISA bus is in byte format (8-bit). The ISA bus interface also performs bus arbitration for three buses: LANCE, ISA, and network buffer RAM refresh. Without bus arbitration, RAM refresh cycles could be missed because the LANCE or Intel486 microprocessor would always have bus control.

Network Buffer RAM

The 64 KB network buffer RAM provides data buffering for both receive and transmit transfers. It can be addressed by either 16-bit words or 8-bit bytes. LANCE does word addressing and the CPU does byte addressing. The memory control signals, CAS*, RAS*, WE*, and OE*, come from the ISA bus interface.

LAN Address MUX

The LAN address MUX multiplexes ISA bus addresses into the ISA bus interface where the addresses are decoded.

DLL ROM

The 16 KB Data Link Layer (DLL) ROM contains remote boot software for the LAN subsystem.

E-Net Address PROM

The E-Net (Ethernet) address PROM contains address information for the LAN node. It is accessed by a single I/O address and an address counter. The address counter sequences through the 32 PROM addresses.

Data Buffer

The data buffer provides data buffering between the ISA bus and the LAN data bus.

I/O Registers

Five I/O registers control Ethernet LAN subsystem operation. Table 8-1 lists the Ethernet LAN subsystem I/O register addresses, specifies the I/O function to access the registers, and briefly describes the registers. The following registers control Ethernet LAN subsystem operations:

- System board configuration port
- Network interface control and status
- Ethernet address PROM
- LANCE controller data port
- LANCE controller address port

Table 8-1. Ethernet LAN Subsystem Address Map

Addr	I/O	Register	Access	Description
800H	R/W	CFG_PORTA	Byte/Word	System board configuration port register
804H	R/W	CFG_PORTB	Byte/Word	System board configuration port register
200H	R/W	NICSR	Byte/Word	Network interface control and status register
20CH	R	ADP	Byte	E-Net Address PROM (upper byte)
20DH	R	ADP	Byte	E-Net Address PROM (lower byte)
204H	R/W	RDP	Word	LANCE controller data port
206H	R/W	RAP	Word	LANCE controller address port

System Board Configuration Port Registers

These read/write registers configure the Ethernet LAN subsystem. Refer to Tables 8-2 and 8-3 for bit assignments.

Table 8-2. CFG_PORTA Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7:4	Reserved		
3	LANRST*	LAN reset	0 = reset
2	L32KMD	LAN 32 KB mode	1 = 32 KB mode, 0 = 64 KB mode
1	L30ST0	LAN timeout	1 = 30 seconds, 0 = 2.5 minutes
0	LNBOOT	LAN boot	1 = enabled

Table 8-3. CFG_PORTB Register Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7:1	Reserved		
0	THINWIRE	LAN I/F type	1 = Thinwire

Network Interface Control and Status Register (NICSR) Bit Assignments

This read/write register sets Ethernet LAN subsystem operating parameters. Refer to Table 8-4 for bit assignments.

Table 8-4. NICSR Bit Assignments

Bit	Signal Mnemonic	Function	Definition
8	RBT	Remote boot timeout	1 = 30 seconds, 0 = 2.5 minutes
7	SHE	Shadow enable	1 = enable
6	SWAP32	Swap 32 KB	1 = enable
5	BUF	Network buffer RAM size	1 = 16 KB, 0 = 48 KB
4	RBE	Remote boot enable	1 = enable
3	Reserved		
2	IM	Interrupt mask	1 = LANCE interrupt inactive
1	IEN	Interrupt line tristate enable	1 = enable, 0 = tristate
0	Reserved		

LANCE Controller Data Port (RDP) Register Bit Assignments

This read/write register is an 8-bit data register. It holds data going to or comming from a control and status register. The control and status register is specified by the LANCE controller address port register.

LANCE Controller Address Port (RAP) Register Bit Assignments

This read/write register selects the control and status register to write data into or read data from. Refer to Table 8-5 for bit assignment.

Table 8-5. RAP Register Bit Assignments

Bit	Signal Mnemonic	Function
15:2	Reserved	
1:0	CSR3:0	Control and status register

Memory Addresses

Ethernet LAN software does not use all the available network buffer RAM space. In 64 KB mode, the Ethernet LAN software uses 48 KB. In 32 KB mode, the Ethernet LAN software uses 16 KB. Refer to Table 8-6 for memory address assignments for the network buffer RAM and the DLL ROM.

Table 8-6. Memory Addresses

Address	I/O Function	Address Mnemonic	Description
DFFFFH to D0000H	Read/write	BUF	Network buffer RAM in 64 KB mode
DBFFFH to D8000H	Read/write	BUF	Network buffer RAM in 32 KB mode
DFFFFH to DC000H	Read	ROM	DLL ROM


CHAP 9

9

Token Ring LAN Subsystem

Introduction

The DECpc Token Ring Workstation system board provides an integrated Token Ring LAN subsystem conforming to IEEE Std. 802.5. The Token Ring network connection is made via either a Shielded Twisted Pair (STP) or Unshielded Twisted Pair (UTP) network connector, selected via a STP/UTP pushbutton. Token Ring network speed, either 4 Mbps or 16 Mbps, can also be selected via the setup program.

Access to the Token Ring LAN subsystem occurs in one of two ways. During I/O operation, the Token Ring LAN subsystem receives and executes various network function commands issued by the Intel486 microprocessor. During ISA bus master operation, the Token Ring LAN subsystem transfers network data to and from the system's main memory using master mode DMA transfer.

Functional Description

The Token Ring LAN subsystem can be divided into two major sections (see Figure 9-1):

- ISA bus interface
- Token ring interface

The remainder of this chapter describes these sections and their associated I/O registers.

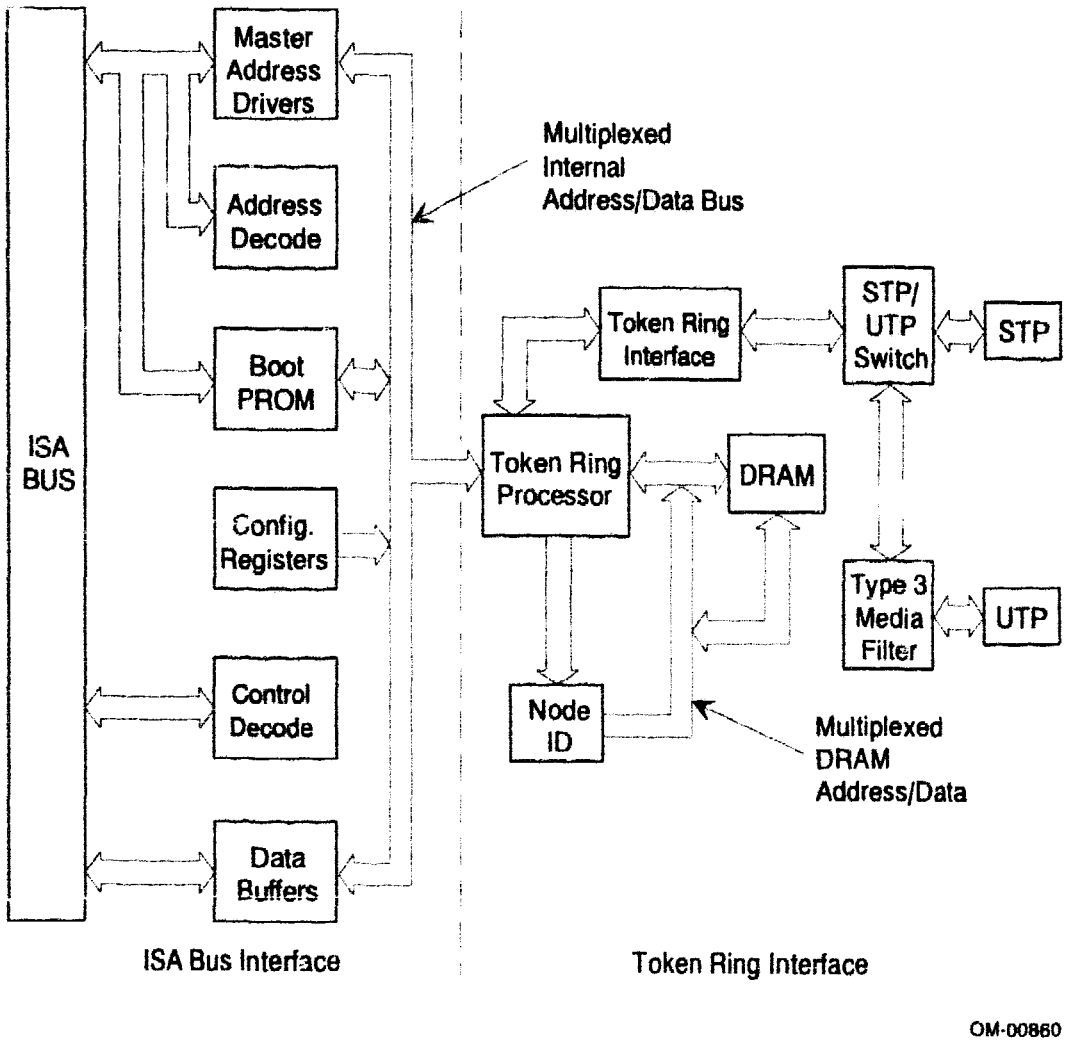


Figure 9-1. Token Ring Subsystem Block Diagram

ISA Bus Interface

The ISA bus interface consists of the following functional units:

- Master address drivers
- Address decode
- Boot PROM
- Configuration registers
- Control decode
- Data buffers

Master Address Drivers

The master address drivers provide address buffering between the Token Ring interface and the ISA bus. The drivers are only active while the Token Ring processor is in control of the ISA bus.

Address Decoders

The address decoders provide address detection. The address decode logic decodes ISA bus address information necessary to access the Token Ring interface

Boot PROM

The boot PROM contains firmware used to remote boot a diskless DECpc 433 Workstation.

Configuration Registers

The configuration registers contain current configuration information in two 8-bit registers: CONBUF1 and CONBUF2.

Control Decode

The control decode logic decodes control and status signals from the ISA bus and the Token Ring processor so all ISA bus data transfers are correctly performed.

Data Buffers

The data buffers provide data buffering between the ISA bus and the Token Ring interface.

Token Ring Interface

The Token Ring interface consists of the following functional units:

- Token Ring processor
- Token Ring DRAM
- Token Ring node ID
- Ring interface
- STP/UTP pushbutton switch
- Type 3 media filter

Token Ring Processor

The Token Ring processor executes the protocol stored in a 128 KB downloadable dynamic RAM. With the appropriate software downloaded, the Token Ring network standard (as specified in IEEE Std. 802.5) is implemented.

Token Ring DRAM

The Token Ring DRAM provides 128 KB of memory storage for the protocol software and data transfer buffers.

Token Ring Node ID

The Token Ring node ID is a bipolar PROM that contains a six-byte ring node address unique to each DECpc 433 Token Ring Workstation. The first six PROM locations contain the node ID, followed by a two-byte checksum. The remaining locations contain a test pattern used during manufacturing.

Token Ring Interface

Analog logic and passive components which make up the system board's electrical interface to the Token Ring network.

STP/UTP Pushbutton Switch

The STP/UTP pushbutton switch selects between the STP and UTP connectors. (STP and UTP are also called Type 1 and Type 3 connectors, respectively.)

Type 3 Media Filter

EMI and noise-suppression circuitry necessary to ensure operation of the Token Ring interface over an Unshielded Twisted Pair cable.

I/O Registers

Table 9-1 lists the Token Ring LAN subsystem I/O register addresses and specifies the I/O function required to access these registers. The following I/O registers control the Token Ring subsystem operations.

- CONBUF1
- CONBUF2
- Token Ring chipset I/O registers

Table 9-1. Token Ring LAN Subsystem Address Map

Address	I/O	Register	Description
0A20	R/W	SIFDAT/SIFDAT low register	Mirror image in Token Ring processor(1)
0A21	R/W	SIFDAT/SIFADR high register	Mirror image in Token Ring processor(1)
0A22	R	CONBUF1	RPL starting address and interrupt level configuration (1)
0A23	R/W	CONBUF2	RPL page select, DMA level, and speed configuration(1)

(1) IBM™ compatible I/O ports

Table 9-1. Token Ring Subsystem Address Map *(continued)*

Address	I/O	Master Mode DMA	Description
0A30	R/W	SIFDAT LSB	Address register
0A31	R/W	SIFDAT MSB	Address register
0A32	R/W	SIFDAT/INC LSB	Data register
0A33	R/W	SIFDAT/INC MSB	Data register
0A34		SIFADR LSB	Address register (same as A3A)
0A35		SIFADR MSB	Address register (same as A3B)
0A36	R/W	SIFSTS	Command and status information
0A37	R/W	SIFCMD	Command and status information
0A38	R/W	SIFACTL LSB	Control register
0A39	R/W	SIFACTL MSB	Control register
0A3A		SIFADR LSB	Address register (same as A34)
0A3B		SIFADR MSB	Address register (same as A35)
0A3C	R/W	SIFADX LSB	Extended address register
0A3D	R/W	SIFADX MSB	Extended address register
0A3E	R	DMALEN LSB	DMA length
0A3F	R	DMALEN MSB	DMA length

CONBUF1 Bit Assignments

This read only register indicates the starting address of the RPL PROM. It is hardwired for address DE000 and interrupt level 2 (9) (refer to Table 9-2).

Table 9-2. CONBUF1 Bit Assignments

Bit	Signal Mnemonic	Function	Definition
7	RPL A18	RPL address	Hardwired high
6	RPL A17	RPL address	(1)
5	RPL A16	RPL address	(1)
4	RPL A15	RPL address	(1)
3	RPL A14	RPL address	(1)
2	RPL A13	RPL address	(1)
1	INT01	Interrupt level	Hardwired low
0	INT00	Interrupt level	Hardwired low

(1) RPL A18:13 point to an 8 KB page in main memory where the RPL EPROM is located.

CONBUF2 I/O Register Bit Assignments

This read/write register indicates the status of these functions: RPL enable, DMA access level, Token Ring speed, and page select (refer to Table 9-3).

Table 9-3. CONBUF2 Bit Assignments

Bit	Signal Mnemonic	Function	Definition	I/O
7	RPLEN	RPL enable	1 = RPL EPROM enable(2)	R
6	RPL03		(1)	R/W
5	DMA01	DMA access	Hardwired low - DMA level 5	R
4	DMA00	DMA access	Hardwired low - DMA level 5	R
3	16/4	Speed select	1 = 16 Mbps(2) 0 = 4 Mbps	R
2	RPL02	Page select	(1)	R/W
1	RPL01	Page select	(1)	R/W
0	RPL00	Page select	(1)	R/W

(1) RPL3:0 choose one of eight 8 KB pages from the RPL EPROM and enables it into main memory at DE000.
(2) See CFG_PORTA register at port 800 for configuring information

SIFDAT LSB/MSB

Each of these two 8-bit registers contain a 16-bit data word.

SIFDAT/INC LSB/MSB (Master Mode Only)

Each of these two 8-bit registers contain a 16-bit data word.

SIFADR LSB/MSB

These two 8-bit address pointer registers contain the 16 LSBs of a 21-bit address. The remaining five MSBs of the 21-bit address are written to SIFADX.

SIFADX LSB/MSB

These two 8-bit address pointer registers contain the five MSBs of a 21-bit address. The remaining 16 LSBs of the 21-bit address are written to SIFADR.

SIFSTS (Master Mode Only)

This 8-bit register contains command and status information and is used in conjunction with SIFCMD to provide a 16-bit data word (refer to Table 9-4).

Table 9-4. SIFSTS Bit Assignments

Bit	Signal Mnemonic	Definition
7	SYSTEM_INTERRUPT	
6:0	Reserved	

SIFCMD

This 8-bit register contains command and status information and is used in conjunction with SIFSTS to provide a 16-bit data word (refer to Table 9-5).

Table 9-5. SIFCMD Bit Assignments

Bit	Signal Mnemonic	Definition
15	INTERRUPT	1 = Internal interrupt
14	RESET	1 = Reset if 2:7 = 1
13	SSB_CLEAR	
12	EXECUTE	
11	SCB_REQUEST	
10	EXECUTE	
9	SSB_CLEAR	
8	TRANSMIT_VALID	

DMALEN LSB/MSB I/O Register

These two 8-bit registers contain the current DMA length.

ACTL LSB/MSB I/O Register

These two 8-bit registers allow the Intel486 microprocessor to control and, to some extent, reconfigure the Token Ring subsystem under software control.

Table 9-6 ACTL LSB/MSB Bit Assignments

Bit	Signal Mnemonic	Definition
15:11	Reserved	
10		Current SDDIR signal value
9		Current SHRQ signal value
8	Reserved	
7		Software reset
6		Token Ring processor halt
5		RAM/ROM processor code
4	Reserved	Always writes as 0
3		Enable Token Ring processor interrupt
2:0	Reserved	


CHAP 10

10

Intelligent Graphics Controller

Introduction

The intelligent graphics controller is a high-performance, high-resolution video board. Its onboard processor is a TMS34020 Graphics System Processor (GSP) that includes a display controller generating all CRT timing signals. The GSP has a full 32-bit internal instruction set with a 512-byte instruction cache. The instruction set is graphics-oriented. Other intelligent graphics controller features include:

- VGA (640 × 480) emulation via hardware with VGA frame capture pass-through capability
- TIGA-340 and RGDI compatibility
- Software compatible with IBM 8514/AI
- 16 or 256 display colors (mode dependent) from a palette of 16.7 million possible colors
- Includes 2 MB dual-ported video RAM (VRAM)
- Optional 1 MB, 4 MB, or 16 MB DRAM via four SIMM sockets for use by graphic application programs
- Socket for an optional TMS34082 coprocessor

The intelligent graphics controller has two operating video modes: GSP and VGA. GSP video mode displays color or monochrome information on a high resolution display. Maximum GSP resolution is 1280 × 1024 with up to 256 colors. VGA video mode displays standard VGA graphics on the high resolution display, eliminating the need for a second lower resolution display.

Terms and Definitions

Following is an alphabetical list of terms and their definitions used in this chapter:

ASIC	Application Specific Integrated Circuit
Frame Buffer	Dual ported memory that contains display information. Also known as VRAM (video RAM)
GSP	The TMS34020 graphics system processor
GSP Video Mode	The high-resolution graphics mode. The GSP and VRAM produce the video display.
RAMDAC	Color palette RAM and digital-to-analog converters
VGA Frame Buffer	Memory that holds VGA display information
VGA Video Mode	Full IBM-compatible VGA graphics operating mode

Intelligent Graphics Controller Hardware

Figure 10-1 shows the location of the major intelligent graphics controller circuit board components. Components include:

- TMS34020 graphics system processor
- GSP DRAM
- Frame Buffer (VRAM)
- BT459 RAMDAC™
- ISA bus connectors
- Monitor connector
- Monitor select switch
- Optional TMS34082 coprocessor socket
- RVGA1 ASIC
- VGA frame buffer
- Video BIOS EPROM
- Frame grabber interface

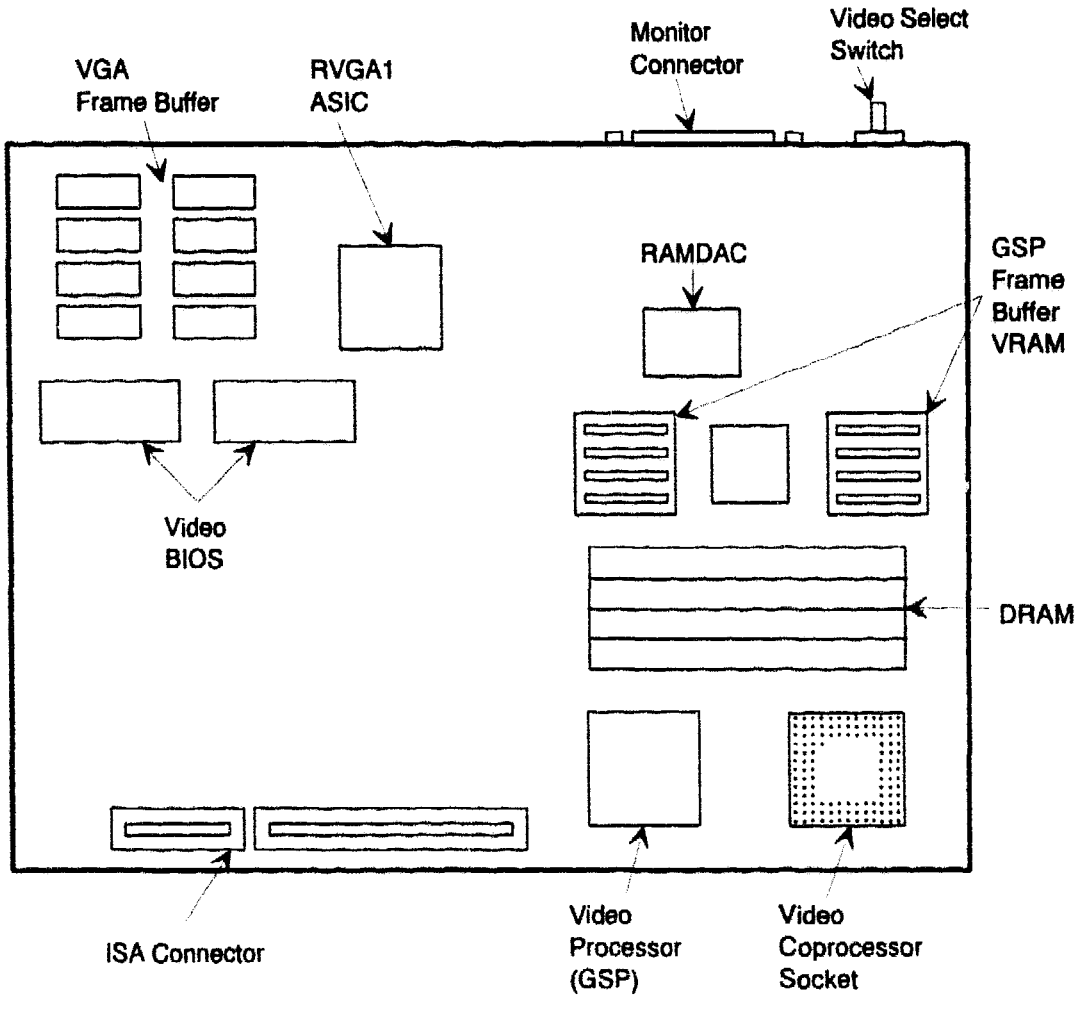


Figure 10-1. Intelligent Graphics Controller Board Layout

TMS34020 Graphics System Processor

The TMS34020 graphics system processor is a 32-bit general purpose microprocessor optimized for graphics display systems. Its main features include a 512 MB linear address range, a 512-byte instruction cache, 30 general purpose 32-bit registers, fifty-four 16-bit on-chip registers dedicated to peripheral control functions, and an integrated display controller. Figure 10-2 shows a block diagram the TMS34020. The following sections briefly describe the following major components:

- Internal functions
- Instruction cache
- Input/output registers
- Microcontrol ROM
- Clock timing logic
- Host control logic
- Page mode registers

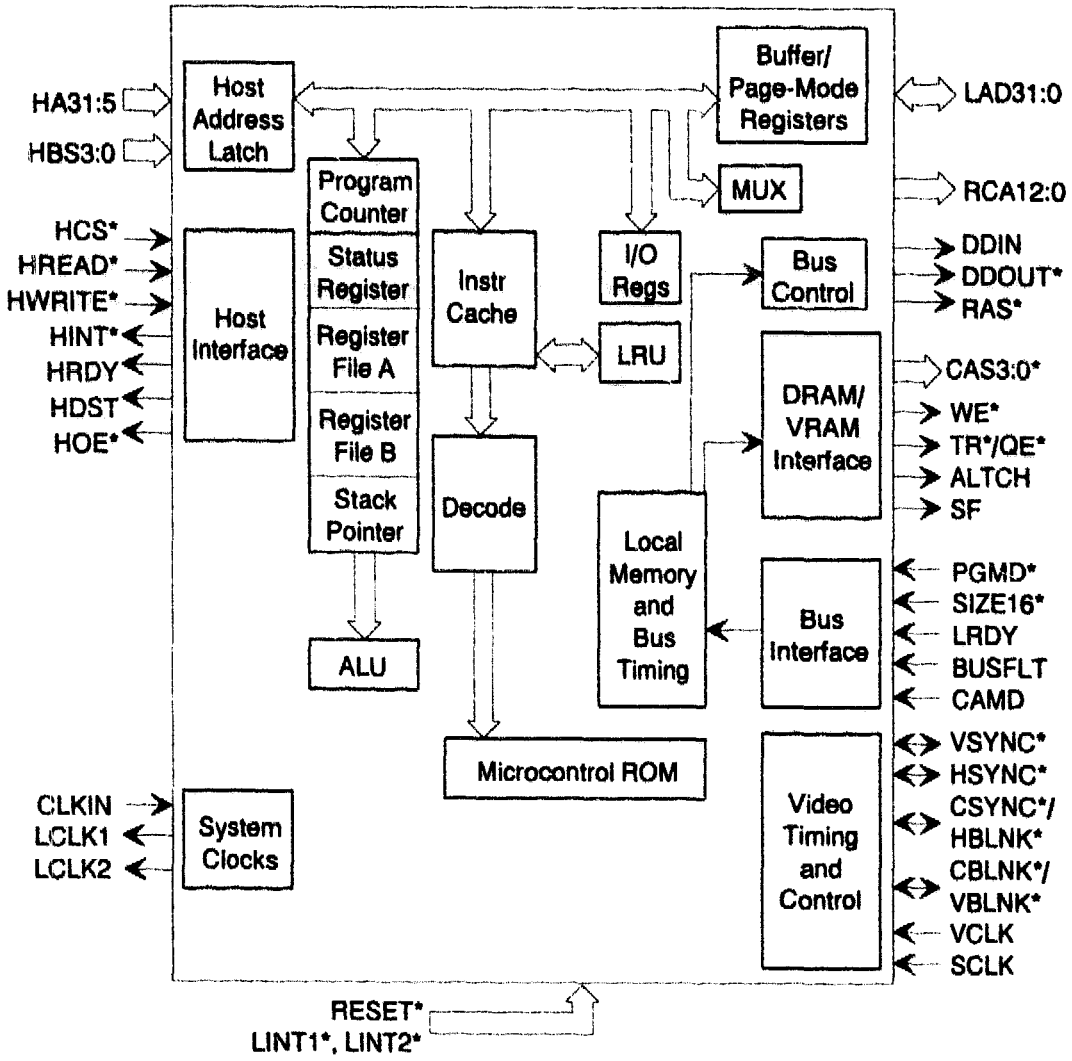


Figure 10-2. TMS34020 Block Diagram

Internal Functions

Internal functions of the TMS34020 include three control and status registers, two register files, and an arithmetic logic unit (ALU). The three control and status registers, status (ST), program counter (PC), and stack pointer (SP) are 32-bit registers.

The ST register contains information about the processor status and parameters that define the programmable data types being used. The PC register points to the next instruction word to be executed. The SP register contains the bit address of the system stack top.

The two register files, A and B, each contain fifteen 32-bit registers and share the SP register. All registers are dual-ported to allow simultaneous read/write operations to two separate registers.

The 32-bit ALU allows the TMS34020 to perform register-to-register operations during a single machine state.

Instruction Cache

The instruction cache is 512 bytes and can store up to 256 instruction words. The cache is enabled and disabled by setting/resetting a bit in one of the local memory input/output registers.

Input/Output Registers

There are fifty-four 16-bit on-chip registers dedicated to peripheral control functions that can be accessed directly by the TMS34020. These same registers can also be accessed by the Intel486 microprocessor through the host interface. There are five categories of input/output registers:

- Local memory
- Video timing and screen refresh
- Host interface
- Interrupt control
- CPU control

Local memory registers control addressing type (big/little endian), refresh rate, row/column mode, plane masking, refresh addressing, bus fault recovery, and the instruction cache.

Video timing and screen-refresh registers generate CRT sync and blanking signals, schedule screen refreshes, and allow external synchronization.

Host-interface registers communicate with the Intel486 microprocessor.

Interrupt control registers provide interrupt status and request information.

CPU-control registers configure the TMS34020 CPU.

Microcontrol ROM

The microcontrol ROM interprets decoded GSP instructions.

Clock Timing Logic

The clock timing logic converts the clock input signals (CLKIN) to internal timing signals and outputs clock signals LCLK1 and LCLK2.

Host Control Logic

The host control logic communicates commands, data, and status information to and from the Intel486 microprocessor via the ISA bus.

Page Mode Registers

The page mode registers buffer data to and from the local memory interface.

GSP DRAM

Standard GSP DRAM is 0 MB; however, it can be optionally increased to 16 MB using SIMM type integrated memory circuits. The optional memory hardware must support fast page mode operation to take full advantage of the intelligent graphics controller performance features. Either 1 MB × 4-bit or 4 MB × 4-bit memory can be used. Access time can not exceed 100 ns.

Frame Buffer

The frame buffer is 2 MB and stores the bit-mapped display image that the CRT displays. Without GSP DRAM, only 1.5 MBs are available to store the display image. The other 512 KBs are used for GSP program memory. When DRAM is installed, frame buffer is remapped and all 2 MBs are available for display image storage.

BT459 RAMDAC

The BT459 RAMDAC is a triple 8-bit RAMDAC designed for high performance/resolution graphics. It receives digital frame buffer outputs and provides analog RGB drive signals to the monitor. Figure 10-3 shows a block diagram of the BT459 RAMDAC. On-chip features include:

- 256 × 24 color palette
- 4:1 pixel multiplexing
- User definable 64 × 64 cursor
- Bit plane masking
- 1, 2, 4, or 8 bits/pixel

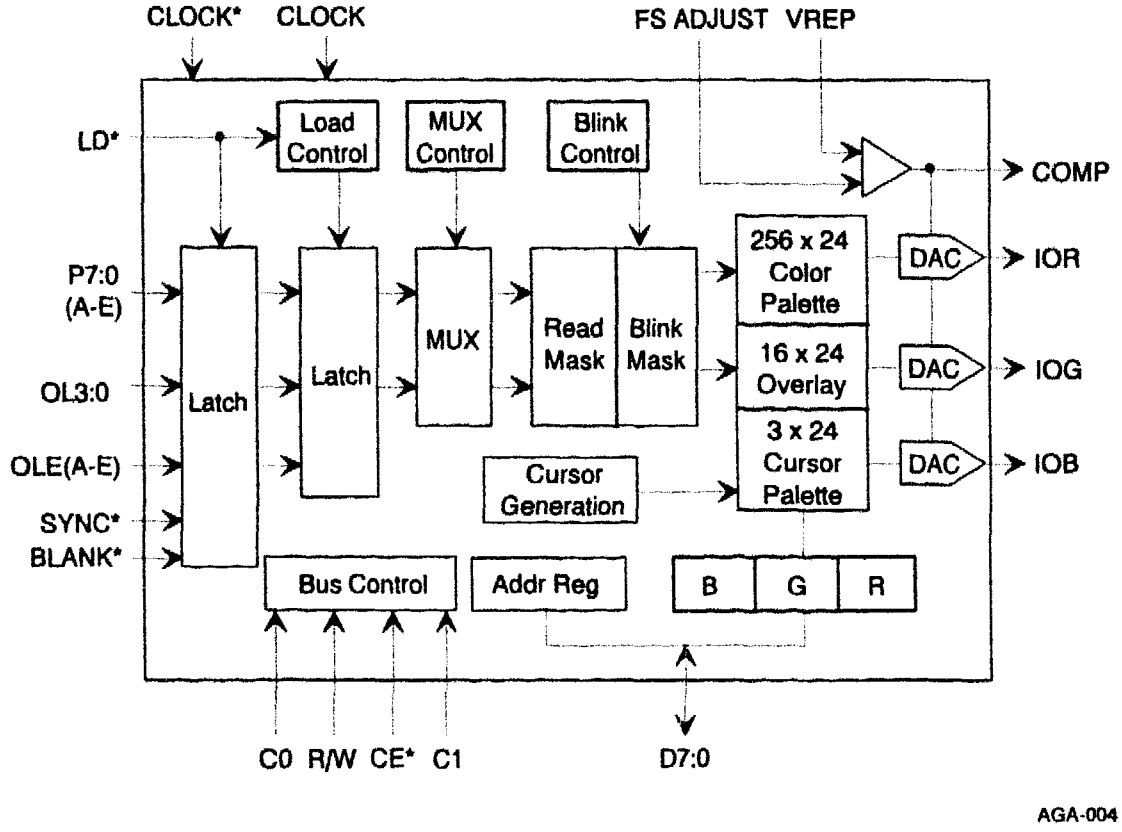


Figure 10-3. RAMDAC Block Diagram

ISA Bus Connectors

The ISA bus connectors provide an interface to the system board. Tables 10-1 and 10-2 list the pin assignments for the ISA bus 8-bit and 16-bit connectors, respectively.

Table 10-1. ISA 8-bit Connector Pin Assignments

Pin Number	Signal	Pin Number	Signal
B1	Ground	A1	IOCHCK*
B2	RSTDEV	A2	D07
B3	+5 V dc	A3	D06
B4	IRQ09	A4	D05
B5	-5 V dc	A5	D04
B6	DRQ2	A6	D03
B7	-12 V dc	A7	D02
B8	SRDY	A8	D01
B9	+12 V dc	A9	D00
B10	Ground	A10	IOCHRDY*
B11	MEMW*	A11	AEN
B12	MEMR*	A12	A19
B13	IOW*	A13	A18
B14	IOR*	A14	A17

Table 10-1. ISA 8-Bit Connector Pin Assignments *(continued)*

Pin Number	Signal	Pin Number	Signal
B15	Ground	A15	A16
B16	DRQ3	A16	A15
B17	DACK1*	A17	A14
B18	DRQ1	A18	A13
B19	MEMREF*	A19	A12
B20	SYSCLK*	A20	A11
B21	IRQ07	A21	A10
B22	IRQ06	A22	A09
B23	IRQ05	A23	A08
B24	IRQ04	A24	A07
B25	IRQ03	A25	A06
B26	DACK2*	A26	A05
B27	TC	A27	A04
B28	BUSALE	A28	A03
B29	+5 V dc	A29	A02
B30	84OSC	A30	A01
B31	Ground	A31	A00

Table 10-2. ISA 16-bit Connector Pin Assignments

Pin Number	Signal	Pin Number	Signal
D1	MCS16*	C1	SBHE*
D2	IOCS16*	C2	LA23
D3	IRQ10	C3	LA22
D4	IRQ11	C4	LA21
D5	IRQ12	C5	LA20
D6	IRQ15	C6	LA19
D7	IRQ14	C7	LA18
D8	DACK0*	C8	LA17
D9	DRQ0	C9	MRDC*
D10	DACK5*	C10	MWTC*
D11	DRQ5	C11	D08
D12	DACK6*	C12	D09
D13	DRQ6	C13	D10
D14	DACK7*	C14	D11
D15	DRQ7	C15	D12
D16	+5 V dc	C16	D13
D17	SECMAST*	C17	D14
D18	Ground	C18	D15

Monitor Connector

The monitor connector is a D-15 connector that provides the interface between the monitor and the intelligent graphics controller. Table 10-3 lists the pin assignments for monitor connector and Figure 10-4 shows its pin locations.

Table 10-3. Monitor Connector Pin Assignments

Pin Number	Description
1	Red video
2	Green video
3	Blue video
4	Not connected
5	Ground
6	Red video return
7	Green video return
8	Blue video return
9	Composite sync
10	Sync return
11	Not connected
12	Not connected
13	Horizontal sync
14	Vertical sync
15	Not connected

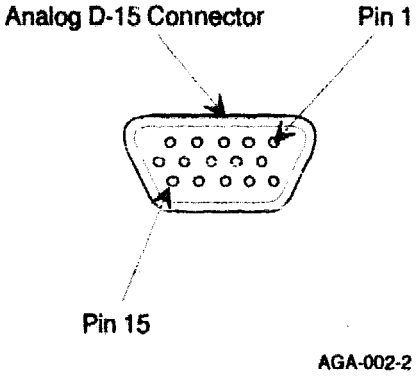


Figure 10-4. Monitor Connector Pin Locations

Video Select Switch

The video select switch positions define the type of monitor connected to the intelligent graphics controller. Table 10-4 lists the switch setting definitions.

Table 10-4. Video Select Switch Settings

Monitor Model	Horizontal Frequency	Vertical Frequency	Switch Setting
VR320-DA(1) VR319-DA(1)	77 KHz	72 Hz	1
VR320-CA(1) VR319-CA(1) VRT19	70 KHz	66 Hz	2
VRT16	70 KHz	66 Hz	3
			4 - 9 (reserved)
ISM(2)	64 KHz	60 Hz	10
			11 - 14 (reserved)

(1) A = Northern Hemisphere, 4 = Southern Hemisphere, e.g., VR320-DA = Northern Hemisphere

(2) Industry Standard Monitor (ISM) represents most common 1280 × 1024 monitors (Mitsubishi. Model 6905, NEC 5D, etc.).

Optional TMS34082 Coprocessor

A socket installed on the GSP board accommodates the TMS34082 floating point coprocessor. The coprocessor extends the TMS34020 capabilities without adding significant overhead. These additional capabilities extend the TMS34020 instruction set. The additional instructions invoke local-memory interface cycles that pass commands and data between the TMS34020, local memory, and the coprocessor.

Software

Figure 10-5 shows a block diagram of software relationships between the Intel486 microprocessor and the intelligent graphics controller.

Application

The application block is any program that uses GSP video mode. Typical examples are AutoCAD or X-windows.

Application Driver

The application driver block is software that supports the application with device-independent functions. Typical examples are the CAD application drivers, spreadsheet drivers, or the X-windows server.

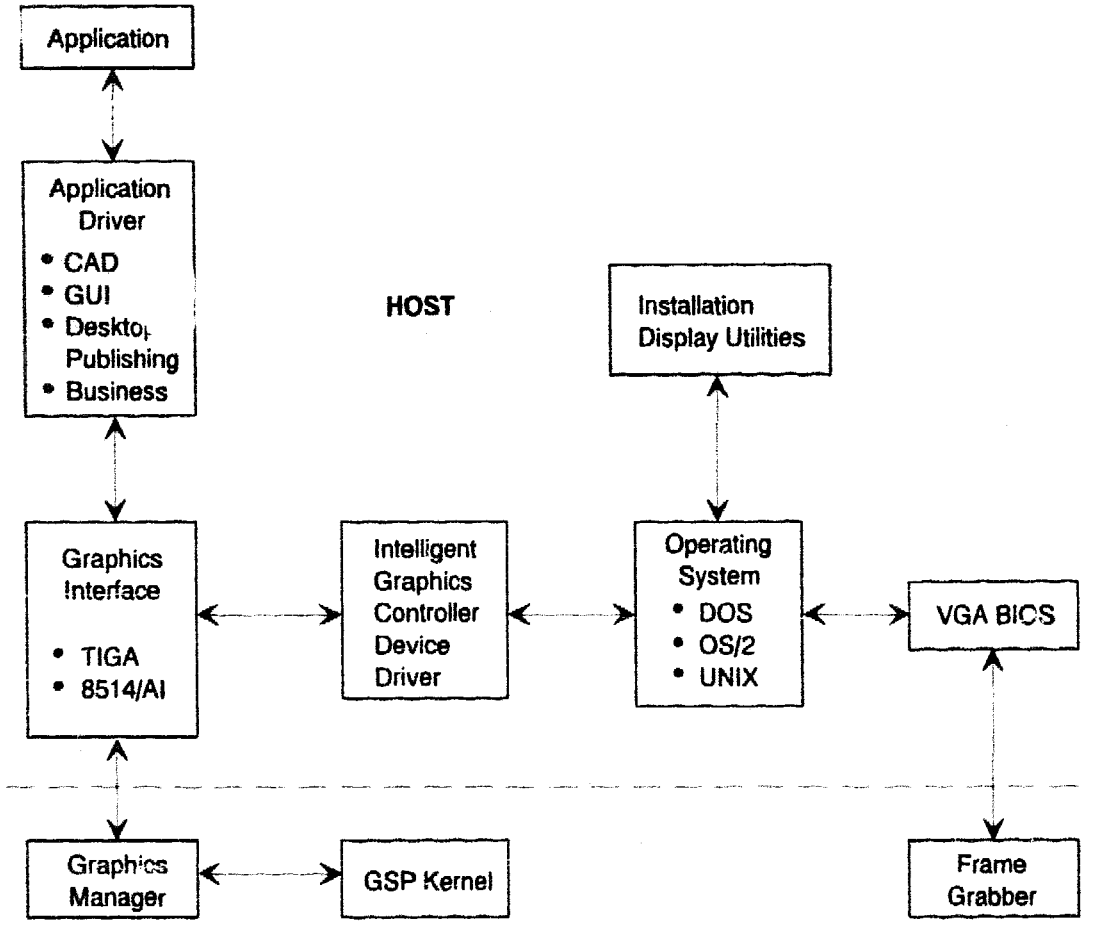


Figure 10-5. Software Block Diagram

Graphics Interface

The intelligent graphics controller supports IBM 8514/A and Texas Instrument Graphics Architecture (TIGA-340).

IBM 8514/AI

The IBM 8514/AI adapter interface provides software emulation of a 8514/AI adapter. This interface has three modules:

- Communications driver — supports the 8514/AI adapter interface functions and communicates with the GSP
- Interrupt handler — supports application communication and initializes access to the communication driver
- Graphics manager — contains graphics drawing primitives

TIGA-340

TIGA-340 is a software interface intended for use by application developers. This interface provides a set of graphics primitives that are extendible and hardware independent. TIGA-340 also enhances performance by optimizing communications between the Intel486 microprocessor and the GSP. This interface has five modules:

- Communications driver — supports TIGA functions and communicates with the GSP
- Interrupt handler — supports application communication and initializes access to the communication driver
- Graphics manager — contains the drawing primitives
- Linking loader — links TIGA compatible graphics manager extensions
- Graphics manager extension — contains TIGA graphics primitives that can be relocated

Graphics Manager

The graphics manager is software that runs on the GSP. It contains a command executive that handles Intel486 microprocessor communications and a standard set of graphics primitives. The graphics manager must be loaded after power-up.

GSP Kernel

The GSP kernel is the lowest level software for the GSP. It provides video, color palette, and memory management services. The GSP kernel must be loaded after power-up and is permanently resident in memory as well as operating system independent.

Intelligent Graphics Controller Device Driver

The intelligent graphics controller device driver verifies the presence of and initializes the intelligent graphics controller. It also installs the GSP kernel and graphics manager. The hardware dependent device driver is the primitive software interface between application drivers and the intelligent graphics controller hardware.

Utilities

Intelligent graphics controller utilities install and select the display format.

Display Utility

The display utility (DISP) selects the number of colors, 16 or 256, to display on the monitor.

VGA BIOS

The VGA BIOS contain standard VGA input and output service software. It is stored in EPROM. The VGA BIOS also contains the frame grabber control program.

Frame Grabber

The frame grabber is software that runs on the GSP that transfers VGA display information to the Frame buffer.

RVGA1 ASIC

The RVGA1 ASIC is the functional equivalent of an IBM video graphics array ASIC. In combination with other intelligent graphics controller board components, the RVGA1 ASIC provides the full functionality of the PS/2 display adapter. The RVGA1 contains logic that provides:

- ISA bus interface
- VGA I/O and memory map decoding and control
- VGA CRT controller
- A DRAM memory controller
- Memory and video timing generation
- A graphics controller
- An attribute controller

VGA Frame Buffer

The VGA frame buffer is 256 KB of DRAM. It stores the entire screen image when in VGA video mode.

Video BIOS EPROM

The video BIOS EPROM stores the VGA BIOS firmware. It also contains firmware that initializes GSP functions when the power-on self test executes.

Frame Grabber Interface

The frame grabber interface stores pixel data in FIFOs located between the VGA pixel data bus and the GSP system data bus.

Programmable Registers

The following sections describe the programmable intelligent graphics controller registers. This information includes address maps, register bit definitions, and interrupt assignments for hardware that is accessible by a graphics application programmer. Figure 10-6 shows a memory map for the intelligent graphics controller. The shaded portions of the memory map are described in this chapter.

Host Interface Registers

Host interface registers hold address, data, control, and status information that passes between the Intel486 microprocessor and the GSP. There are eight host interface registers that occupy 15 I/O ports at addresses 02B0H through 02BFH. The following sections briefly describe and provide bit definitions for the following host interface registers:

- Address
- Data
- Data plus
- Status
- Configuration
- Base address
- Block size
- GSP base address

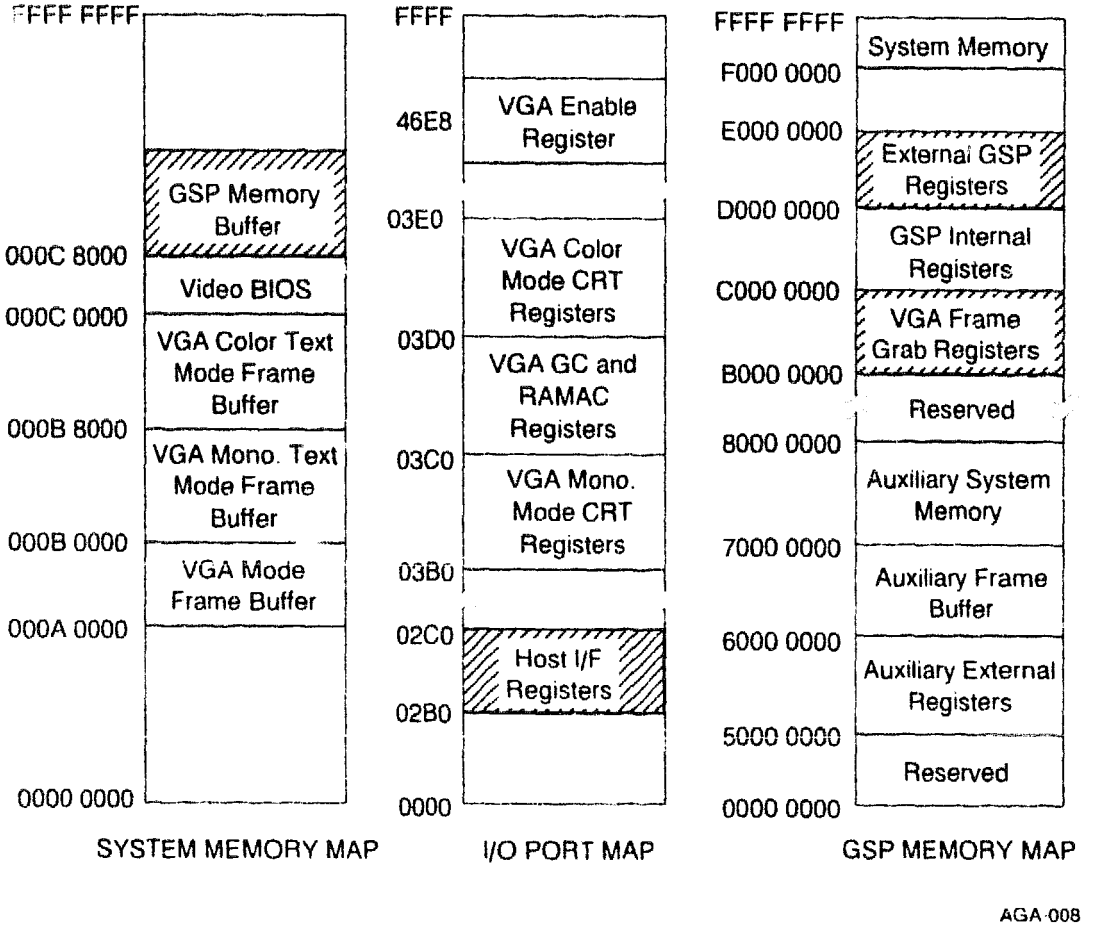


Figure 10-6. Intelligent Graphics Controller Memory Map

Address Register

The address register is a 32-bit read/write register that occupies four I/O ports. Data in the register is a 28-bit pointer into GSP memory space that identifies where to write the data in the data register. Note that address information must be in place before data transfers. Table 10-5 lists the address register's addresses and its bit definitions.

Table 10-5. Address Register Bit Definitions

Address (in hex)	Register	Bits	Definition
02B3	Address byte 3	7:0	Address bits 24 to 31
02B2	Address byte 2	7:0	Address bits 16 to 23
02B1	Address byte 1	7:0	Address bits 8 to 15
02B0	Address byte 0	3:0	Not used
		7:4	Address bits 4 to 7

Data Register

The data register is a 16-bit read/write register that holds data being transferred between the Intel48 microprocessor and the GSP. A write access to this register causes data to be written to the GSP address specified in the address register. A read access causes data to be transferred from the GSP address specified in the address register to this register. Table 10-6 lists the data register's addresses and its bit definitions.

Table 10-6. Data Register Bit Assignments

Address (in hex)	Register	Bits	Definition
02B5	Data MSB	15:8	Data bits 15:8
02B4	Data LSB	7:0	Data bits 7:0

Data Plus Register

The data plus register is a 16-bit read/write register that holds data being transferred between the Intel486 microprocessor and the GSP. A write access to this register causes data to be written to the GSP address specified in the address register. After a data write, the GSP address is incremented by one write. A read access causes data to be transferred from the GSP address specified in the address register. Again, after a data read the GSP address is incremented by one. A byte access to 2B6H causes the address to increment; however, the address increments after byte access to 2B7H. Table 10-7 lists the data plus register's addresses and its bit definitions.

Table 10-7. Data Plus Register Bit Definitions

Address (in hex)	Register	Bits	Definition
02B7	Data MSB	15:8	Data bits 15:8
02B6	Data LSB	7:0	Data bits 7:0

Status Register

The status register is read only and contains VGA capability, expansion slot type, Xilinx™ status, and circuit board revision level information. It is addressed at I/O port 02B8H. Table 10-8 lists the status register's bit definitions.

Table 10-8. Status Register Bit Definitions

Bit(s)	Descriptions	Definition
7:5	Revision code	Board version number
4	Xilinx status	0 = Xilinx devices not programmed 1 = Xilinx devices programmed
3	Xilinx ready	Valid only if bit 4 = 0 0 = Xilinx device ready 1 = Xilinx device not ready
2	Slot type status	1 = Installed in 16-bit ISA slot Always reads as one
1	VGA option status	0 = Daughter board installed Always reads as zero
0	VGA pass through status	0 = VGA pass through connected Always reads as zero

Reset Register

The reset register is write only and is addressed at I/O port 02B8H. A write to the reset register causes a reset of the intelligent graphics controller including the GSP and Xilinx programmable gate arrays. The reset is cancelled by a read from the status register.

Configuration Register Bit Definitions

The configuration register is a read/write register that holds hardware configuration information. It is addressed at I/O port 02B9H. Table 10-9 lists the configuration register's bit definitions.

Table 10-9. Configuration Register Bit Definitions

Bit(s)	Descriptions	Definition
7 and 0	MEMCS16 cycle control	0 0 = 32 KB address block decode, MCS16 held low for full cycle between BALE 0 1 = 128 KB address block decode, MCS16 held low for full cycle between BALE 1 0 = 32 KB address block decode, MCS16 asserted for duration of LA(23:17) 1 1 = 128 KB address block decode, MCS16 asserted for duration of LA(23:17)
6	Diagnostic LED	0 = On 1 = Off
5	GSP base address register bit 31	MSB of GSP base address register
4	Reserved	
3	I/O Bus width	0 = 8-bits, byte transfers 1 = 16-bit, word transfers
2	Memory bus width	0 = 8-bits, byte transfers 1 = 16-bit, word transfers
1	VGA pass through control	0 = VGA video mode selected 1 = GSP video mode selected (also indicates VGA video mode)

Memory Base Address Register

The memory base address register is a read/write register that contains shared memory enable, interrupt status, and block starting address information. This register defines the ISA bus starting address of a shared memory block. It occupies two I/O port addresses. Table 10-10 lists the memory base address register's addresses and bit definitions. The DECpc 433 Workstation has a 32 KB memory block reserved at address C000H.

Table 10-10. Memory Base Address Register Bit Definitions

Address (in hex)	Bit(s)	Descriptions	Definition
02BB	7:0	PC bus address	SA (23:16)
02BA	7:4	PC bus address	SA (15:12)
	3:2	Reserved	
	1	GSP host interrupt status (read only)	0 = Interrupt pending 1 = No interrupt pending
	0	Shared memory enable	0 = Disable 1 = Enable

Memory Block Size Register

The memory block size read/write register contains the size of the shared memory block. It is addressed at I/O port 02BCH. Table 10-11 lists the memory block size register's bit definitions.

Table 10-11. Memory Block Size Register Bit Definitions

Bit(s)	Descriptions	Definition
7:4	Reserved	
3:0	Block Size	0 0 0 0 = 4 KB 0 0 0 1 = 8 KB 0 0 1 1 = 16 KB 0 1 1 1 = 32 KB 1 1 1 1 = 64 KB

GSP Base Address Register

The GSP base address read/write register defines which 16 MB segment of GSP memory contains the shared memory block. Shared memory address bit 31 is defined by bit 5 of the configuration register. The GSP base address register occupies two I/O port addresses. Table 10-12 lists the GSP base address register's addresses and bit definitions.

Table 10-12. GSP Base Address Register Bit Definitions

Address (in Hex)	Bit(s)	Descriptions	Definition
02BF	7:0	Shared memory block MSB	GSP address bits 30:23
02BE	7:0	Shared memory block LSBs	GSP address bits 22:15

GSP Internal Registers

There are 42 GSP internal registers that provide control and status for:

- Communications between the GSP and Intel486 microprocessor
- GSP memory interface
- Interrupts
- Video timing and screen refresh
- Graphics drawing

These registers are located in the GSP memory space at addresses C000 0000 through C000 C03FF. For more information about the GSP internal registers refer to the TMS34020 User's Guide.

GSP Memory Map

Table 10-13 lists the GSP memory map. The amount of installed system memory and frame buffer memory changes the GSP memory map. These effects are also included in the table.

Table 10-13. GSP Memory Map

GSP Address Range (in Hex)	Function
F000 0000 to FFFF FFFF	System memory (DRAM)
E000 0000 to EFFF FFFF	Frame buffer memory (VRAM)
D000 0000 to DFFF FFFF	External GSP registers
C000 0000 to CFFF FFFF	Internal GSP registers
B000 0000 to BFFF FFFF	VGA frame grabber registers
8000 0000 to AFFF FFFF	Reserved
7000 0000 to 7FFF FFFF	Auxiliary program memory
6000 0000 to 6FFF FFFF	Auxiliary video display memory
5000 0000 to 5FFF FFFF	Auxiliary external registers
0000 0000 to 4FFF FFFF	Reserved for future use

VGA Frame Grabber Registers

VGA frame grabber registers provide status, pixel mask, pixel data, screen size, and FIFO reset when using VGA video mode. The following sections briefly describe and provide bit definitions for the following VGA frame grabber registers:

- Status
- Pixel mask
- VGA color palette
- Vertical count
- Horizontal count
- FIFO

Status Register

The status register is read only and provides VGA frame grabber mode status information to the GSP. It is addressed at B000 0000. Table 10-14 lists the status register's bit definitions.

Table 10-14. Status Register Bit Definitions

Bit(s)	Descriptions	Definition
31:8	Reserved	
7	VGA Vsync	1 = Horizontal retrace
6	VGA Hsync	1 = Vertical retrace
5	VGA blank	0 = VGA blanked 1 = VGA display active
4	VGA blank latched	0 = VGA blanked 1 = VGA not blanked
3	VGA palette change latched	0 = VGA palette changed 1 = VGA palette not changed
2	FIFO read error latched	0 = FIFOs read error 1 = FIFOs no read error
1	FIFO empty latched	0 = FIFOs empty 1 = FIFOs not empty
0	FIFO full latched	0 = FIFOs full 1 = FIFOs not full

The latched signals hold their value after a single occurrence until the status register is read.

Pixel Mask Register

The pixel mask register is read only and contains VGA video mode pixel mask data. It is addressed at B000 0020. Table 10-15 lists the pixel mask register's bit definitions. This register provides a copy of the VGA RAMDAC pixel mask register contents.

Table 10-15. Pixel Mask Register Bit Definitions

Bit(s)	Description
31:8	Reserved
7:0	VGA pixel mask

Palette Data Register

The palette data register is read only and contains color palette data. It is addressed at B000 0060. After a read from this register, the address of the data value is incremented. This allows the contents of the entire VGA RAMDAC color palette RAM to be accessed sequentially. Table 10-16 lists the data register's bit definitions.

Table 10-16. Data Register Bit Definitions

Bit(s)	Description
31:8	Reserved
7:0	VGA palette data

VGA Palette Index Clear Register

The VGA palette index clear register provides a mechanism to reset the VGA RAMDAC color palette location. A read from the index clear register resets the address of the data value to the first location. It is addressed at B000 0040. The data obtained during the read is undefined.

Vertical Count Registers

The bit combination in the two vertical count registers forms a number that equals the total number of horizontal scan lines being produced by the current VGA display mode. The vertical count low register holds the two low bits and the vertical count high register holds the upper eight bits. Both registers are read only. Table 10-17 lists the vertical count low register's address and bit definitions. Table 10-18 lists the vertical count high register's address and bit definitions.

Table 10-17. Vertical Count Low Register Bit Definitions

Address (in hex)	Bit(s)	Description
B000 0080	31:2	Reserved
	1:0	Number of horizontal scan lines, 2 LSBs

Table 10-18. Vertical Count High Register Bit Definitions

Address (in hex)	Bit(s)	Description
B000 00E0	31:8	Reserved
	7:0	Number of horizontal scan lines, 8 MSBs

Horizontal Count Register

The horizontal count register is read only and holds the number of pixels per scan line divided by four of the current VGA display mode. Table 10-19 lists the horizontal count register address and bit definitions.

Table 10-19. Horizontal Count Register Bit Definitions

Address (in hex)	Bit(s)	Description
B000 00A0	31:8	Reserved
	7:0	Pixels modulo 4

FIFO Reset Register Bit Definitions

The FIFO reset register is a read only register at address B000 00C0 that resets all FIFOs. Its 32 bits are undefined. A read from this register clears the contents of all FIFOs and resets all status flags.

External GSP Registers

External GSP registers configure the intelligent graphics controller outputs, control GSP internal interrupts, report status, and change color values in the color palette. The following sections briefly describe and provide bit definitions for the following external GSP registers:

- Configuration/status
- Color palette address
- Color palette control
- Color palette data

Configuration/Status Register

The configuration/status register is a 32-bit register at GSP address D0080 0000. Bits 15 through 0 are read/write. Bits 31 through 16 are read only. Table 10-20 lists the configuration/status register's bit definitions.

Table 10-20. Configuration/Status Register Bit Definitions

Bit(s)	Description	Definition
31:24	Reserved	
23	VSYNC signal level	0 = Vertical retrace
22	HSYNC signal level	0 = Horizontal retrace
21	VGA pass through status	0 = Pass through 1 = GSP video mode
20	Reserved	Always read as one
19:16	Monitor select switch setting	1 1 1 1 = VR320-DA, VR319-DA 1 1 1 0 = VR320-CA, VR319-CA, VRT19 1 1 0 1 = VRT16 1 1 0 0 = VR325, VR326 1 0 1 1 = VR325 stretch, VR326 stretch 1 0 1 0 = VR315 1 0 0 1 = VR315 stretch 1 0 0 0 = VR297, VR299 0 1 1 1 = VR262 0 1 1 0 = Industry Std. 1280 × 1024 All others are reserved
15:14	PFS serial load mode	0 0 = Normal 0 1 = Write mode 1 0 = Read mode 1 1 = Illegal

Table 10-20. Configuration/Status Register Bit Definitions *(continued)*

Bit(s)	Description	Definition
13	PFS serial data bit	
12	PFS serial clock	0 = No change 1 = Clock bit 13 into PFS
11	Reserved	
10	DRAM size	0 = 0 to 1 MB 1 = 4 MB
9:8	VRAM memory mapping	0 0 = None 0 1 = 256 KB from 1 MB 1 0 = 512 KB from 2 MB 1 1 = Undefined
7	VSYNC polarity	0 = Active low 1 = Active high
6	HSYNC polarity	0 = Active low 1 = Active high
5:4	Pixel size	0 0 = 1 bits per pixel 0 1 = 2 bits per pixel 1 0 = 4 bits per pixel 1 1 = 8 bits per pixel
3	Reserved	
2	Video clock rate 0 and 1	0 = Dotclock/4 1 = Dotclock/8
1:0	Dot clock select	0 0 = 130.808 MHz 0 1 = 119.843 MHz 1 0 = 110.000 MHz 1 1 = Programmable

BT459 RAMDAC Address Registers

The RAMDAC address registers hold address information that specifies where to write color palette and configuration data contained in the RAMDAC data register. Table 10-21 lists the RAMDAC address register's addresses and bit assignments. For programming specifics, refer to the manufacturer's data manual.

Table 10-21. RAMDAC Address Register Bit Definitions

Address (in Hex)	Read/ Write	Bit(s)	Description
D000 0600	Write	7:0	Address low byte
D000 0020	Write	7:0	Address high byte
D000 0080	Read	7:0	Address low byte
D000 00A0	Read	7:0	Address high byte

BT459 RAMDAC Control Register

The RAMDAC control register contains information bits that configure the RAMDAC mode of operation. For programming specifics, refer to the manufacturer's data manual. This register is written to at D0000 0040 and read from D000 00C0.

BT459 RAMDAC Data Register

The RAMDAC data register contains color data for the color palette. Data is written at the address specified in the RAMDAC address registers. Table 10-22 lists the RAMDAC register's addresses and bit definitions. For programming specifics, refer to the manufacturer's data manual.

Table 10-22. Color Palette Data Register Bit Definitions

Address (in Hex)	Read/ Write	Bit(s)	Description
D000 0060	Write	7:0	Color data
D000 00E0	Read	7:0	Color data

Interrupt

The GSP generates interrupt IRQ10 to the Intel486 microprocessor. The interrupt can be set by a program running on the GSP.

Operation

The following sections describe the operation of the two intelligent graphics controller subsystems: GSP and VGA. The GSP subsystem supports high resolution graphics (1280 × 1024) and translates VGA data so it can be displayed on the high-frequency high-resolution monitor. This eliminates the need for a second lower-resolution monitor. The VGA subsystem supports all standard VGA display modes and provides VGA data to the GSP subsystem for processing. Figure 10-7 shows the data flow between the two subsystems.

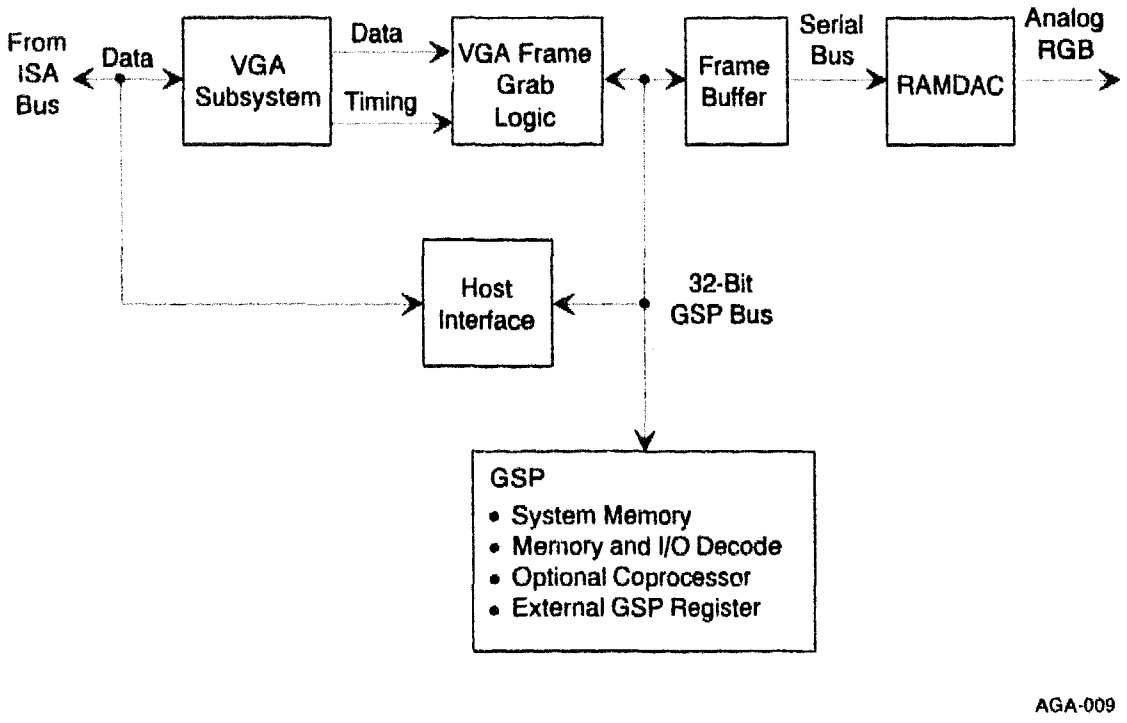


Figure 10-7. GSP and VGA Subsystems Data Flow

GSP Subsystem

The GSP subsystem processes all display information regardless of video mode. All GSP inputs are from either the host interface or the VGA subsystem. The host interface is a series of registers that hold address, data, control, and status information that passes between the ISA bus and the GSP. These registers are described earlier in this chapter. VGA subsystem inputs are eight data bits and timing signals. VGA timing signals include horizontal and vertical synchronization, blanking, and clock signals. The following sections describe the GSP subsystem functions:

- GSP
- VGA frame grabber logic
- Frame buffer (VRAM)

GSP

The GSP is a general purpose microprocessor optimized for graphics processing. As with all microprocessors, it requires supporting functions. Functions include:

- System memory (DRAM)
- Memory and I/O decode logic
- Optional coprocessor
- External GSP registers

The intelligent graphics controller device driver performs initialization functions then loads the GSP software. In GSP video mode, an application driver controls communication between the GSP and the application via a host resident device driver. A device driver is not needed for VGA video mode.

System memory (GSP DRAM) is optional. When system memory is not installed, the GSP uses a portion of the frame buffer for its memory. When system memory is installed, the frame buffer is remapped and none of it is used for system memory. Memory and I/O decode logic decodes GSP memory address and GSP I/O addresses. The external GSP registers configure outputs, control GSP internal interrupts, report status, and change color values in the color palette. When installed, the optional coprocessor enhances GSP performance.

VGA Frame Grabber Logic

The VGA frame grabber logic is only used when in VGA video mode. It allows the GSP to obtain a copy of the VGA screen image on a frame-by-frame basis. The GSP then redirects the screen image to the VRAM based frame buffer via FIFO memories. The VGA frame grabber logic also provides automatic VGA mode change detection. Full screen display of VGA images is provided by pixel replication.

VGA frame grabber logic monitors for VGA mode change by counting pixels and vertical scan lines. These counts are provided to the GSP where a software function checks changes in either the number of pixels or scan lines.

A near full screen VGA video mode display on a high-resolution monitor requires pixel replication. In some VGA modes pixel replication is straightforward. For example, in 640 × 480 display mode (ignoring borders) 640 doubles to 1280, the number of pixels in one horizontal line. Dividing the video dot clock in half replicates the original 640 pixels. However, in the standard VGA text mode (2+) the resolution is 720 × 400. In this mode, the video dot clock must be reduced by 56%. The divisor varies with each VGA display mode. A fully programmable frequency synthesizer allows the correct video clock division for each VGA display mode. Vertical scan replication is implemented by doubling or quadrupling each scan line, effectively doubling or quadrupling the vertical VGA size. Vertical scan replication is performed in hardware via the CRT controller in the GSP.

The update or frame rate in VGA video mode is 60 Hz in 480 line display mode and 70 Hz in all other display modes.

Monitor synchronization signal timing is implemented by the fully programmable CRT controller found in the GSP.

Frame Buffer

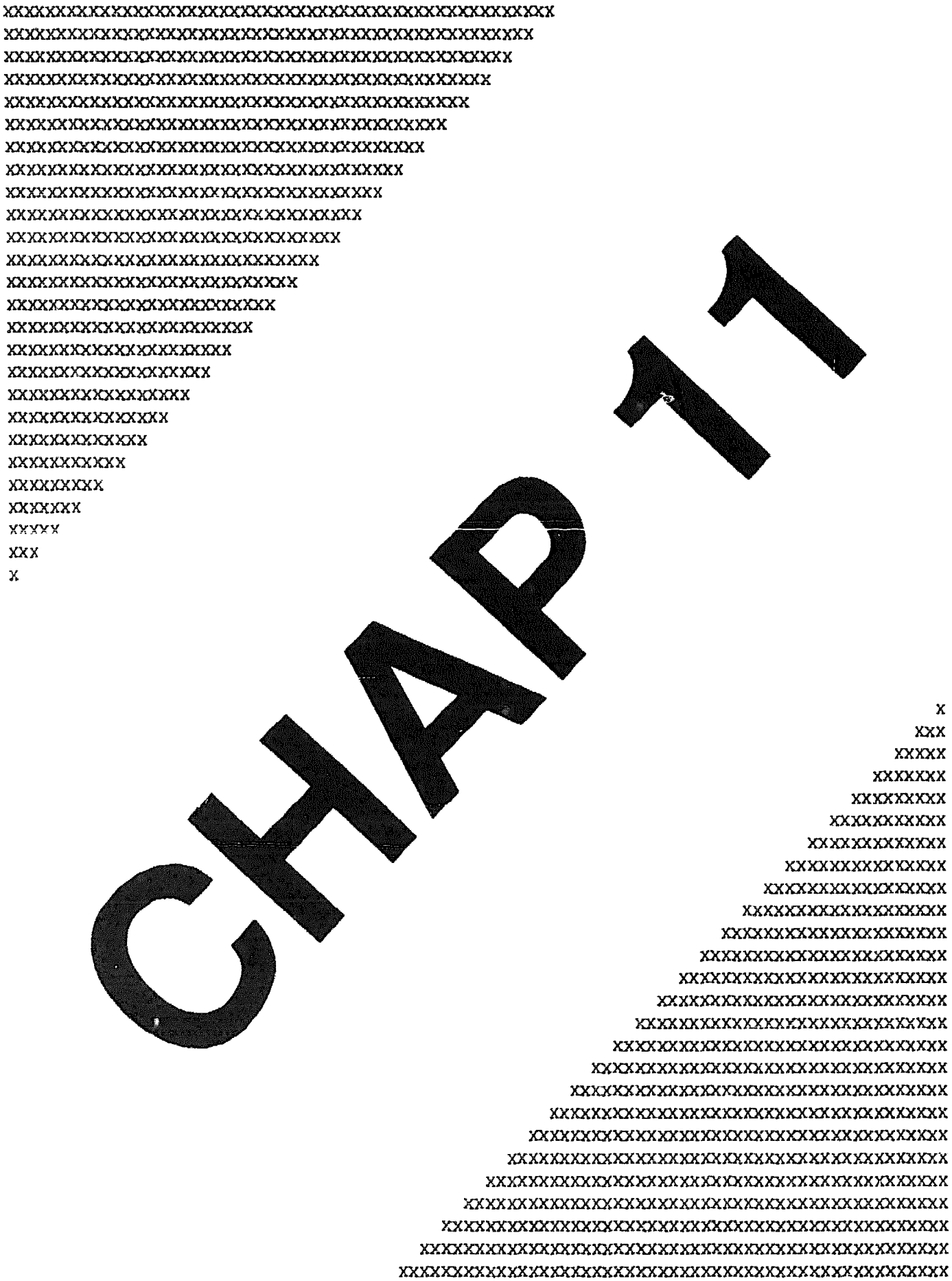
The frame buffer (VRAM) stores display information in dual ported RAM. Parallel accesses are performed to and from the GSP while its serial outputs drive the RAMDAC.

VGA Subsystem

The VGA subsystem supports all standard VGA text and graphics display modes. Its inputs and outputs are normal VGA signals. However, outputs are not sent to the RAMDAC. Instead, they go to the VGA frame grabber logic for capture and processing by the GSP as previously described.

RAMDAC

The RAMDAC receives serial display information from the frame buffer and outputs analog RGB signals to the monitor's electron guns. The electron guns then drive the electron beams that illuminate the display screen.


CHAPTER 11

11

Power Supply

Introduction

This chapter describes the specifications of the DECpc 433 Workstation power supply and the optional SCSI expansion box power supply. The workstation power supply is a 105 Watt power supply. The SCSI expansion box power supply is a 63 Watt power supply. Both power supplies sense input voltage level and automatically compensate for the two input voltage ranges (refer to Appendix A, "Specifications" for input voltage specifications).

105 Watt Power Supply Specifications

Table 11-1 lists the specifications for the 105 Watt power supply.

Table 11-1. 105 Watt Power Supply Specifications

Output Voltage (V dc)	Continuous Current Minimum	Continuous Current Maximum	Peak Surge For 15 Seconds	Maximum Power Output
+5 ±5%	3.5 A	18.0 A		90 Watts
+12 ±5%	0 A	1.0 A	2.0 A	12 Watts
-12 ±10%	0 A	0.2 A		2.4 Watts
-5 ±10%	0 A	0.2 A		1 Watt

63 Watt Power Supply Specifications

Table 11-2 lists the specifications for the 63 Watt power supply.

Table 11-2. 63 Watt Power Supply Specifications

Output Voltage (V dc)	Continuous Current Minimum	Continuous Current Maximum	Peak Surge For 15 Seconds	Maximum Power Output
+5 ±5%	0.5 A	3.0 A		15 Watts
+12 ±5%	0.5 A	4.0 A	8.0 A	48 Watts


APP A

A

Specifications

Introduction

This appendix gives information about the technical characteristics of the DECpc 433 Workstation. Information includes:

- System board specifications
- Video board specifications
- Environmental specifications
- Physical dimensions
- Power requirements
- System board current requirements

System Board Specifications

Table A-1 lists the system board specifications.

Table A-1. System Board Specifications

Attribute	Specification
CPU	Intel486
CPU clock speed	33 MHz
Master clock speed	66 MHz
ISA bus speed	8 MHz
Data path	8-, 16-, and 32-bits
Interrupts	15

Table A-1. System Board Specifications *(continued)*

Attribute	Specification
Memory addressing	
Physical	256 MB
Virtual	64 terabytes
Supported	16 MB
ROM BIOS Size	128 KB
DRAM memory	
Speed	80 ns or faster
Type	9-bit SIMM
Standard size	8 MB
Optional sizes	4, 12, 16, 24, 32, 48 MB
Error Protection	Byte parity
Alkaline system battery	3-year shelf life
Optional Turbocache	64 or 128 KB
Non-volatile RAM	114 bytes
Dimensions	10.5 inches by 12 inches
Layers	6
VLSI components	11

Video Board Specifications

Table A-2 lists the video board specifications.

Table A-2. Video Board Specifications

Attribute	Specification
Processor	TI 34020 microprocessor
Coprocessor	Optional TMS34082
Speed	32 MHz
DRAM	0 MB to 16MB
VRAM	2 MB
Colors	256 from a palette of 16.7 million

Environmental Specifications

Table A-3 list the system module and the SCSI expansion box environmental specifications.

Table A-3. Environmental Specifications

Attribute	Specification
Operating temperature	10° to 40° C
Storage temperature	-20° C to 60° C
Operating humidity	20-80% Relative humidity, max wet bulb @ 33° C
Non-operating humidity	95% Relative humidity, max wet bulb @ 35° C
Altitude	To 10,000 feet maximum
Maximum operating noise	42 dB at operator position
Shock, non-operating	30 G, 11 ms, 1/2 sine wave

Physical Dimensions

Table A-4 lists the physical dimensions of the system module and the SCSI expansion box.

Table A-4. Physical Dimensions

Attribute	Specification
Width	16.5 inches (41.9 cm)
Height	2.75 inches (6.9 cm)
Length	14.5 inches (36.8 cm)
Weight	15.9 lbs (35.1 kg)

Power Requirements

Table A-5 lists the power requirements for the system module and the SCSI expansion box.

Table A-5. Power Requirements

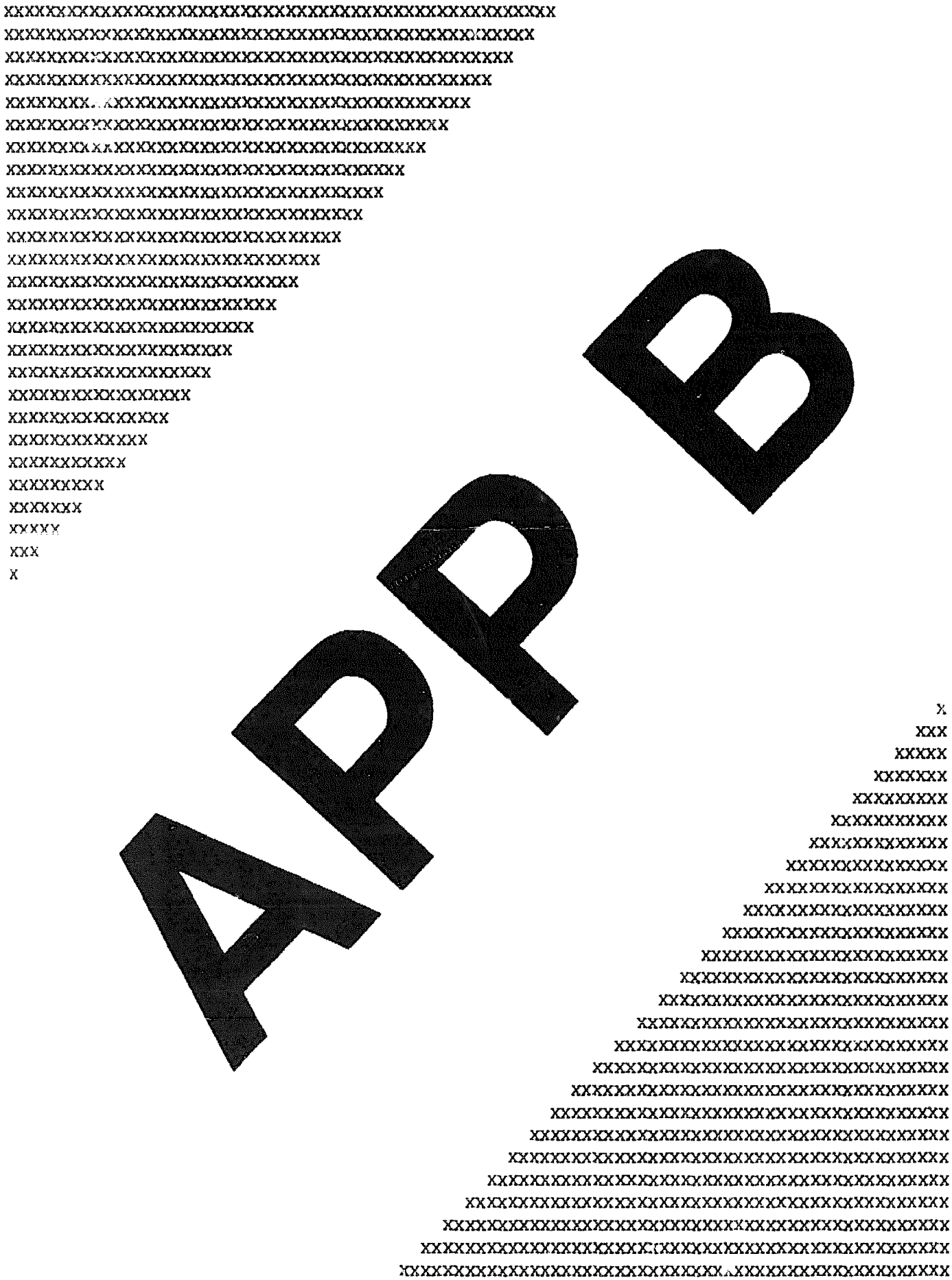
Voltage Source	Maximum Range	Input Current	Frequency Limits
100–120 V ac	90–132 V ac	10 A	47–63 Hz
200–240 V ac	180–264 V ac	5 A	47–63 Hz

System Board Current Requirements

Table A-6 lists the nominal current requirements for the system board and the parts that obtain power from the system board.

Table A-6. Current Requirements

Assemblies	+5.0 V dc	+12.0 V dc	-12.0 V dc
System board with 8 MB of system memory	5.3 A	0.2 A	0.1 A
Intelligent graphics controller	5 A	0.14 A	0 A
1.44 MB floppy disk drive	0.15 A	0.3 A	0 A
IDE fixed disk drive	0.3 A	0.3 A	0 A


APP B

B

BIOS Interrupt Routines

Introduction

This appendix describes the interrupt service routines available in the system BIOS. Information includes:

- Interrupt vector table
- Summary of BIOS services

Interrupt Vector Table

Table B-1 identifies each interrupt by function and type. Where applicable, it lists the interrupt vector address initialized by the BIOS at POST. System software may revector an interrupt at or shortly after the boot process is completed, so these values may not be the same in every system on every occasion.

Table B-1. Interrupt Functions and Types

INT	Function	Type	Vector
00H	Divide by zero	Exception	
01H	Single step	Exception	
02H	Nonmaskable interrupt (NMI)	Exception	FE2C3H
03H	Breakpoint	Exception	
04H	Overflow	Exception	
05H	Print screen	Software	FFF54H
05H	Bounds exception	Hardware	
06H	Invalid op code	Hardware	

Table B-1. Interrupt Functions and Types *(continued)*

INT	Function	Type	Vector
06H	Reserved (PC only)	Hardware	
07H	Reserved (PC only)	Hardware	
07H	Math coprocessor not present	Hardware	
08H	Double exception error	Hardware	
08H	System timer (IRQ 0)	Hardware	FFEA5H
09H	Keyboard (IRQ 1)	Hardware	FE987H
09H	Math coprocessor segment overrun	Logical	
0AH	IRQ 2 cascade from second programmable interrupt controller	Hardware	
0AH	Invalid task segment state	Logical	
0BH	Serial communications (COM2)	Hardware (IRQ 3)	
0BH	Segment not present	Logical	
0CH	Serial communications (COM1)	Hardware (IRQ 4)	
0CH	Stack segment overflow	Logical	
0DH	Parallel printer (LPT2)	Hardware (IRQ 5)	
0DH	General protection fault	Logical	
0EH	IRQ 6 diskette	Hardware	FEF57H
0EH	Page fault (80386 only)	Logical	
0FH	Parallel printer (LPT1) IRQ 7	Hardware	
10H	Video	Software	FF065H
10H	Numeric coprocessor fault	Logical	
11H	Equipment list	Software	FF84DH
12H	Memory size	Software	FF841H

Table B-1. Interrupt Functions and Types *(continued)*

INT	Function	Type	Vector
13H	Fixed disk/diskette	Software	FE3FEH
14H	Serial communication	Software	FE739H
15H	System services	Software	FF859H
16H	Keyboard	Software	FE82EH
17H	Parallel printer	Software	FEFD2H
18H	Process boot failure	Software	F1C90H
19H	Bootstrap loader	Software	FE6F2H
1AH	Time-of-day	Software	FFE6EH
1BH	Keyboard break	Software	FFF53H
1CH	User timer tick	User	FFF53H
1DH	Video parameter table	BIOS Table	FF0A4H
1EH	Diskette parameter table	BIOS Table	FEFC7H
1FH	Video graphics characters	User	F7F67H
20H to 3FH	Reserved for DOS		
40H	Diskette BIOS revector	Software	FEC59H
41H	Fixed disk parameter table	BIOS Table	FE401H
42H	EGA default video driver	BIOS Table	
43H	Video graphics characters	User	
44H to 45H	Reserved		
46H	Fixed disk parameter table	BIOS Table	FE401H
47H to 49H	Reserved		
4AH	User alarm	User	
4BH to 59H	Reserved		

Table B-1. Interrupt Functions and Types *(continued)*

INT	Function	Type	Vector
5AH	Cluster adapter		
5BH to 5FH	Reserved		
60H to 66H	Reserved for user program Interrupts	User	
67H	LIM EMS driver		
68H to 6FH	Reserved		
70H	Real-time clock (IRQ 8)	Hardware	(1)
71H	IRQ 2 redirect (IRQ 9)(2)	Hardware	(1)
72H	Reserved (IRQ 10)	Hardware	(1)
73H	Reserved (IRQ 11)	Hardware	(1)
74H	Reserved (IRQ 12)	Hardware	(1)
75H	80287 exception (IRQ 13)	Hardware	(1)
76H	Fixed disk (IRQ 14)	Hardware	(1)
77H	Reserved (IRQ 15)		(1)
78 to 7FH	Reserved (IRQ 15)		
80H to F0H	Reserved for BASIC	BASIC	
F1H to FFH	Reserved for user program interrupts	User	

(1) At FFF23H is a table of 8 vectors (offsets only) for interrupts 70H-77H (IRQ 8-15)
(2) Token ring

BIOS Services

Each BIOS service runs at least one function. When a BIOS service is capable of running more than one function, functions are selected by placing the proper function number in the AH register. Subfunctions are selected via either the AL register or the BL register.

Tables B-2 through B-12 briefly define each BIOS service and list each BIOS function and subfunction.

Table B-2. Print Screen Service

Int	Parameter	Function
05H	None	Print screen

Table B-3. Video Services

INT	Parameter	Function
10H	AH = 00H	Set video mode
	AH = 01H	Set text mode cursor size
	AH = 02H	Set cursor position
	AH = 03H	Read current cursor position
	AH = 04H	Read light pen position
	AH = 05H	Select active video page
	AH = 06H	Scroll active page up
	AH = 07H	Scroll active page down
	AH = 08H	Read character/attribute from screen
	AH = 09H	Write character/attribute to screen
	AH = 0AH	Write character only to screen
	AH = 0BH	Set color palette
	AH = 0CH	Write pixel
	AH = 0DH	Read pixel
	AH = 0EH	Write teletype to active page
	AH = 0FH	Return video status

Table B-3. Video Services *(continued)*

INT	Parameter	Function	
	AH = 10H	Set palette/color registers:	
		Parameter	**Subfunction**
		AL = 00H	Set single palette
		AL = 01H	Set overscan register
		AL = 02H	Set all palette registers and overscan
		AL = 03H	Toggle intensify/blinking bit
		AL = 04H-06H	Reserved
		AL = 07H	Read individual palette register
		AL = 08H	Read overscan register (border color)
		AL = 09H	Read all palette registers and overscan register (border color)
		AL = 10H	Set individual color register
		AL = 11H	Reserved
		AL = 12H	Set block of color registers
		AL = 13H	Select color paging mode (not valid for mode 13H)
		BL = 00H	Select paging mode
		BL = 01H	Select page
		AL = 14H	Reserved
		AL = 15H	Read single DAC color register
		AL = 16H	Reserved
		AL = 17H	Read block of color registers
		AL = 18H-19H	Reserved
		AL = 1AH	Read color paging status
		AL = 1BH	Sum color values to gray shades

Table B-3. Video Services *(continued)*

INT	Parameter	Function	
	AH = 11H	Load character generator:	
		Parameter	**Subfunction**
		AL = 00H	Load user text mode font
		AL = 01H	Load ROM 8×14 text mode font
		AL = 02H	Load ROM 8×8 double dot text mode font
		AL = 03H	Set block specifier (text mode only)
		AL = 04H	Load 8×16 ROM text mode font
		AL = 10H	Load user text mode font (after mode set)
		AL = 11H	Load ROM 8×14 text mode font (after mode set)
		AL = 12H	Load ROM 8×8 double dot text mode font (after mode set)
		AL = 14H	Load 8×16 ROM text mode font (after mode set)
		AL = 20H	Set user graphics characters pointer at INT 1FH (8×8 font)
		AL = 21H	Set user graphics font pointer at INT 43H
		AL = 22H	Use ROM 8×14 font for graphics
		AL = 23H	Use ROM 8×8 double dot font for graphics
		AL = 24H	Use ROM 8×16 font for graphics
		AL = 30H	Get font pointer information

Table B-3. Video Services *(continued)*

INT	Parameter	Function	
	AH = 12H	Alternate select:	
		Parameter	**Subfunction**
		BL = 10H	Return configuration information
		BL = 20H	Switch to alternate print screen routine
		BL = 30H	Select scan lines for text modes
		BL = 31H	Enable/disable default palette loading during set mode
		BL = 32H	Enable/disable video
		BL = 33H	Enable/disable summing to gray shades
		BL = 34H	Enable/disable cursor scaling
		BL = 35H	Switch display
		BL = 36H	Video screen off/on
	AH = 13H	Write string:	
		Parameter	**Subfunction**
		AL = 00H	Cursor not moved
		AL = 01H	Cursor is moved
		AL = 02H	Cursor not moved (text modes only)
		AL = 03H	Cursor is moved (text modes only)

Table B-3. Video Services *(continued)*

INT	Parameter	Function
	AH = 14H-19H	Reserved
	AH = 1AH	Read/write display combination code:
		Parameter **Subfunction** AL = 00H Read display combination code AL = 01H Write display combination code
	AH = 1BH	Return functionality/state information
	AH = 1CH	Save/restore video state
	AH = 1DH-FFH	Reserved

Table B-4. Equipment List Service

INT	Parameter	Function
11H	None	Read equipment list

Table B-5. Memory Size Service

INT	Parameter	Function
12H	None	Read memory size

Table B-6. Diskette Service

INT	Parameter	Function
13H	AH = 00H	Reset diskette system
	AH = 01H	Read diskette status
	AH = 02H	Read diskette sectors
	AH = 03H	Write diskette sectors
	AH = 04H	Verify diskette sectors
	AH = 05H	Format diskette track
	AH = 06H-07H	Reserved
	AH = 08H	Read drive parameters
	AH = 09H-14H	Reserved
	AH = 15H	Read drive type
	AH = 16H	Detect media change
	AH = 17H	Set diskette type
	AH = 18H	Set media type for format
	AH = 19H-FFH	Reserved

Table B-7. Fixed Disk Service

INT	Parameter	Function
13H	AH = 00H	Reset diskette(s) and fixed disk
	AH = 01H	Read fixed disk status
	AH = 02H	Read sectors
	AH = 03H	Write sectors
	AH = 04H	Verify sectors
	AH = 05H	Format cylinder
	AH = 08H	Read drive parameters
	AH = 09H	Initialize drive parameters
	AH = 0AH	Read long sectors
	AH = 0BH	Write long sectors
	AH = 0CH	Seek to cylinder
	AH = 0DH	Alternate fixed disk reset
	AH = 10H	Test for drive ready
	AH = 11H	Recalibrate drive
	AH = 14H	Controller internal diagnostic
	AH = 15H	Read fixed disk type
	AH = 16H-FFH	Reserved

Table B-8. Serial Communication Service

INT	Parameter	Function
14H	AH = 00H	Initialize serial communications port
	AH = 01H	Send character
	AH = 02H	Receive character
	AH = 03H	Read serial port status
	AH = 04H to FFH	Reserved

Table B-9. System Services

INT	Parameter	Function
15H	AH = 04H to 4EH	Reserved
	AH = 4FH	Keyboard intercept
	AH = 50H to 7FH	Reserved
	AH = 80H	Device open
	AH = 81H	Device close
	AH = 82H	Program termination
	AH = 83H	Set event wait interval
	AH = 84H	Joystick support
	AH = 85H	System request key
	AH = 86H	Wait
	AH = 87H	Move block
	AH = 88H	Read extended memory size (× 1 KB)
	AH = 89H	Switch processor to protected mode
	AH = 8AH to 8FH	Reserved
	AH = 90H	Device busy
	AH = 91H	Interrupt complete
	AH = 92H to BFH	Reserved
	AH = C0H	Return system configuration parameters

Table B-10. Keyboard Service

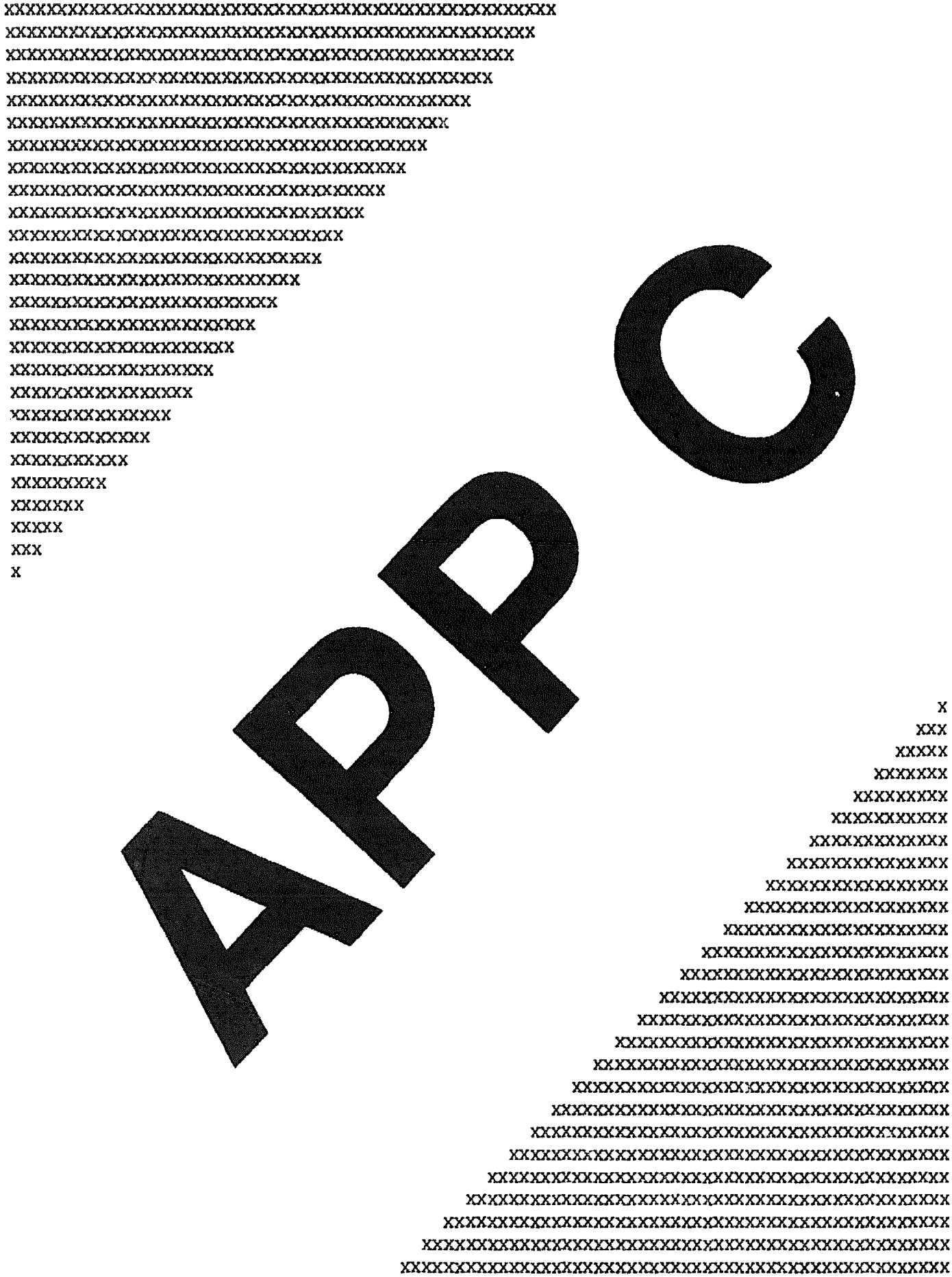
INT	Parameter	Function
16H	AH = 00H	Read keyboard input
	AH = 01H	Return keyboard status
	AH = 02H	Return shift flag status
	AH = 03H	Set typematic rate and delay
	AH = 05H	Store key data
	AH = 06H to 0FH	Reserved
	AH = 10H	Read extended keyboard input
	AH = 11H	Return extended keyboard status
	AH = 12H	Return extended shift flag status
	AH = 13H to FFH	Reserved

Table B-11. Parallel Printer Service

INT	Parameter	Function
17H	AH = 00H	Print character
	AH = 01H	Initialize printer
	AH = 02H	Read printer status
	AH = 03H to FFH	Reserved

Table B-12. Time-of-Day Service

INT	Parameter	Function
1AH	AH = 00H	Read system timer time counter
	AH = 01H	Set system timer time counter
	AH = 02H	Read real time clock time
	AH = 03H	Set real time clock time
	AH = 04H	Read real time clock date
	AH = 05H	Set real time clock date
	AH = 06H	Set real time clock alarm
	AH = 07H	Reset real time clock alarm


APPC

C

Device Mapping

Introduction

This appendix contains tables that list the system memory map, I/O address map, interrupt map, and LAN memory map for the respective Ethernet or Token Ring DECpc 433 Workstation system board. Also included are DMA device descriptions.

Table C-1. System Memory Map (Ethernet)

Address Range (in hex)	Function	Size	Shadow	Cache	WP(2)
0010 0000 to 02FF FFFF	Extended memory	47 MB	No	Yes(1)	No
000F 0000 to 000F FFFF	System BIOS/SCSI BIOS	64 KB	Yes(1)	Yes(1)	Yes
000E 0000 to 000E FFFF	System BIOS Setup/EMS	64 KB	Yes(1)	Yes(1)	Yes
000D 8000 to 000D FFFF	LAN BIOS/RAM	32 KB	No	No	No
000D 0000 to 000D 7FFF	LAN RAM	32 KB	No	No	No
000C 8000 to 000C FFFF	Video buffer	32 KB	No	No	No
000C 0000 to 000C 7FFF	Video BIOS	32 KB	Yes(1)	Yes(1)	No
000A 0000 to 000B FFFF	Video RAM	128 KB	No	No	No
0000 0000 to 0009 FFFF	Base memory	640 KB	No	Yes(1)	No

(1) Can also be disabled
(2) Write protected (not cached in the Intel486)

Table C-2. I/O Address Map (Ethernet)

Range (in hex)	Function
000 to 00F	DMA controller one
020 to 03F	Interrupt controller one
040 to 043	Programmable interval timer
060 to 06F	Keyboard (61 port B)
070 to 07F	Real-time clock (RTC), NMI
080 to 09F	DMA page register
0A0 to 0BF	Interrupt controller two
0C0 to 0DF	DMA controller two
0E8 to 0EB	Not used
0EC	82344/82346 configuration index register
0ED	82344/82346 configuration data port
0EE	82346 fast A20
0EF	82346 fast reset
0F0	Not used
0F4	82346 slow CPU
0F5	82346 fast CPU
0F8	Not used
0F9	82346 configuration disable
0FB	82346 configuration enable

Table C-2. I/O Address Map (Ethernet) *(continued)*

Range (in hex)	Function
0FC to 0FF	Reserved for numeric coprocessor
170 to 171	Secondary RTC (not used)
1F0 to 1F8	IDE controller
200 to 20C	LAN registers
2B0 to 2BF	Intelligent graphics controller registers
2F8 to 2FF	COM2
340 to 35C	SCSI registers
278 to 37F	LPT1
3B0 to 3DF	VGA registers
3C0 to 3CF	Registers
3F0 to 3F7	Floppy disk controller
3F8 to 3FF	Corona configuration port 1 (COM1)
800	Corona configuration port A (write/read)
804	Corona configuration port B (read only)
808	Corona configuration port C (write/read)
80C	Corona configuration port D (write/read)
46E8	VGA enable register

Table C-3. System Interrupt Levels (Ethernet)

Priority	Interrupt Controller	Interrupt Number	Interrupt Source
1	1	IRQ0	Timer tick
2	1	IRQ1	Keyboard controller
	1	IRQ2	Cascade interrupt
3	2	IRQ8	Real-time clock (RTC)
4	2	IRQ9	Reserved
5	2	IRQ10	TIGA video
6	2	IRQ11	SCSI interrupt
7	2	IRQ12	Mouse interrupt
8	2	IRQ13	Numeric coprocessor
9	2	IRQ14	Hard disk drive
10	2	IRQ15	Reserved
11	1	IRQ3	COM2
12	1	IRQ4	COM1
13	1	IRQ5	LAN interrupt or LPT2
14	1	IRQ6	Floppy disk drive
15	1	IRQ7	LPT1

Table C-4. Ethernet Memory Map

Mnemonic	Function	R/W(1)	B/W(2)	Address
BUF	Dual-port RAM in 64 KB mode	R/W	B/W	D0000 to DFFFF
BUF	Dual-port RAM in 32 KB mode	R/W	B/W	D8000 to DBFFF
ROM	Diagnostics/ remote boot	R	B/W	DC000 to DFFFF

(1) Read/write
(2) Byte/word

Table C-5. System Memory Map (Token Ring)

Address Range (in hex)	Function	Size	Shadow	Cache	WP(2)
0010 0000 to 02FF FFFF	Extended memory	47 MB	No	Yes(1)	No
000F 0000 to 000F FFFF	System BIOS/ SCSI BIOS	64 KB	Yes(1)	Yes(1)	Yes
000E 0000 to 000E FFFF	System BIOS Setup/EMS	64 KB	Yes(1)	Yes(1)	Yes
000D 0000 to 000D DFFF	Not used(3)	56 KB	No	No	No
000D E000 to 000D FFFF	Token ring LAN boot(4)	8 KB	No	No	No
000C 8000 to 000C FFFF	Video buffer	32 KB	No	No	No
000C 0000 to 000C 7FFF	Video BIOS	32 KB	Yes(1)	Yes(1)	No
000A 0000 to 000B FFFF	Video RAM	128 KB	No	No	No
0000 0000 to 0009 FFFF	Base memory	640 KB	No	Yes(1)	No

(1) Can also be disabled
(2) Write protected (not cached in the Intel486)
(3) Can be used for DOS "load high"
(4) Can be used for DOS "load high" after LAN boot completes

Table C-6. I/O Address Map (Token Ring)

Range (in hex)	Function
000 to 00F	DMA controller one
020 to 03F	Interrupt controller one
040 to 043	Programmable interval timer
060 to 06F	Keyboard (61 port B)
070 to 07F	Real-time clock (RTC), NMI
080 to 09F	DMA page register
0A0 to 0BF	Interrupt controller two
0C0 to 0DF	DMA controller two
0E8 to 0EB	Not used
0EC	82344/82346 configuration index register
0ED	82344/82346 configuration data port
0EE	82346 fast A20
0EF	82346 fast reset
0F0	Not used
0F4	82346 slow CPU
0F5	82346 fast CPU
0F8	Not used
0F9	82346 configuration disable
0FB	82346 configuration enable

Table C-6. I/O Address Map (Token Ring) *(continued)*

Range (in hex)	Function
0FC to 0FF	Reserved for numeric coprocessor
170 to 171	Secondary RTC (not used)
1F0 to 1F8	IDE controller
200 to 20C	LAN registers
2B0 to 2BF	Intelligent graphics controller registers
2F8 to 2FF	COM2
340 to 35C	SCSI registers
278 to 37F	LPT1
3B0 to 3DF	VGA registers
3C0 to 3CF	Registers
3F0 to 3F7	Floppy disk controller
3F8 to 3FF	Corona configuration port 1 (COM1)
800	Corona configuration port A (write/read)
804	Corona configuration port B (read only)
808	Corona configuration port C (write/read)
80C	Corona configuration port D (write/read)
A20 to A23	Token ring LAN
A30 to A3F	Token ring LAN
46E8	VGA enable register

Table C-7. System Interrupt Levels (Token Ring)

Priority	Interrupt Controller	Interrupt Number	Interrupt Source
1	1	IRQ0	Timer tick
2	1	IRQ1	Keyboard controller
	1	IRQ2	Cascade interrupt
3	2	IRQ8	Real-time clock (RTC)
4	2	IRQ9	Token ring LAN
5	2	IRQ10	TIGA video
6	2	IRQ11	SCSI interrupt
7	2	IRQ12	Mouse interrupt
8	2	IRQ13	Numeric coprocessor
9	2	IRQ14	Hard disk drive
10	2	IRQ15	Reserved
11	1	IRQ3	COM2
12	1	IRQ4	COM1
13	1	IRQ5	LPT2
14	1	IRQ6	Floppy disk drive
15	1	IRQ7	LPT1

Table C-8. Token Ring Memory Map

Mnemonic	Function	R/W(1)	B/W(2)	Address
ROM	Remote boot	R	B/W	DE000 to DFFFF

(1) Read/write
(2) Byte/word

Ethernet Workstation DMA Device

The floppy disk drive uses DMA request/acknowledge lines DRQ2/DACK2*. It is the only DMA device used.

Token Ring Workstation DMA Device

The floppy disk drive uses DMA request/acknowledge lines DRQ5/DACK5*.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