MINI-EXCHANGE

TECHNICAL MANUAL

EP-DFMSA-TM-001

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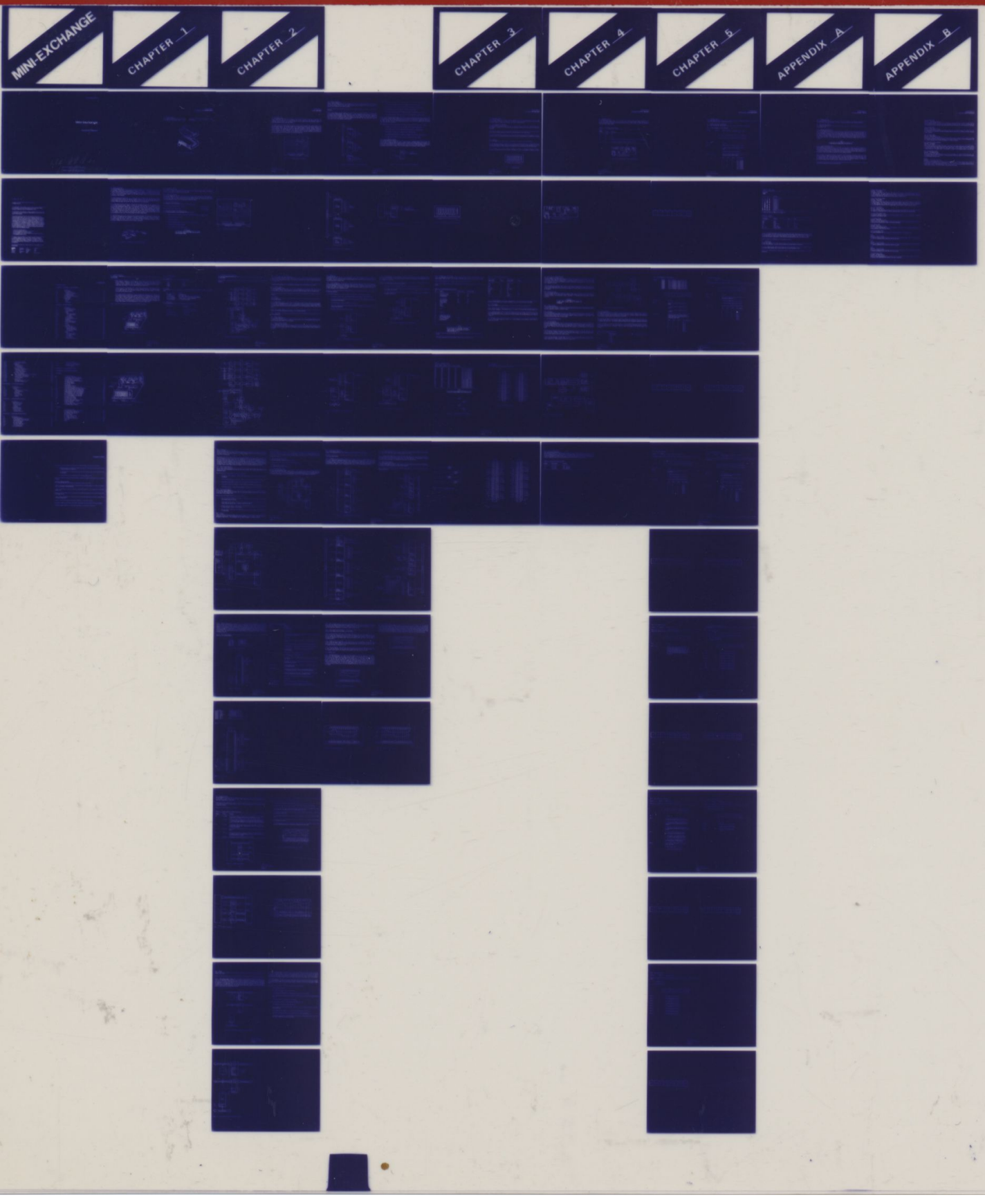

MINI-EXCHANGE

EK-DFMSA-TM-001

Mini-Exchange

Technical Manual

Prepared by Educational Services
of
Digital Equipment Corporation

1st Edition, April 1984

This equipment generates and uses radio frequency energy and if not installed and used properly, that is, in strict accordance with the manufacturer's instructions, may cause interference to radio and television reception It has been type tested and found to comply with the limits for a Class B computing device in accordance with specifications in subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference in a residential installation However, there is no guarantee that interference will not occur in a particular installation If this equipment does cause interference to radio or television reception, which can be determined by turning the equipment off and on, try to correct the interference by one or more of the following methods

- re-orient the receiving antenna
- relocate the computer with respect to the receiver
- move the computer away from the receiver
- plug the computer into a different outlet so that computer and receiver are on different branch circuits

If necessary, consult the dealer or an experienced radio/television technician for additional suggestions The booklet "How to Identify and Resolve Radio/TV Interference Problems," prepared by the Federal Communications Commission, may be helpful this booklet is available from the U S Government Printing Office, Washington D C 20402, Stock No 004-000-00345-00345-4.

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INTRODUCTION

This manual documents hardware functions for the Mini-Exchange and provides the following

- Documents systems' concepts and design information for field engineers and personnel trained by Digital Equipment Corporation
- Provides Field Service with the technical information needed to repair systems effectively and cost efficiently
- Provides information not duplicated in any other hardware manual

Refer to the *Mini-Exchange Installation/Owner's Manual* for operational information on the Mini-Exchange.

MANUAL ORGANIZATION

This section describes how the chapters are organized and what they contain

Chapter 1 General Information describes the Mini-Exchange, related documents, site selection and preparation, circuit boards, and specifications

Chapter 2 Logic Board provides the functional and detailed descriptions of the logic board to the block diagram level.

Chapter 3 Connector Board provides the functional and detailed descriptions of the connector board to the block diagram level

Chapter 4 Power Supply Board provides the functional and detailed descriptions of the power supply board to the block diagram level

Chapter 5 Firmware Descriptions provides bit definitions for the control registers

Appendix A Diagnostics provides testing modes and procedures, and a section on software problems.

Appendix B Signal Definitions provides signal definitions for the modem control lines

CHAPTER 1

CHAPTER 1
GENERAL INFORMATION

1.1 INTRODUCTION

This chapter describes the Mini-Exchange, related documents, site selection and preparation, circuit boards, and also specifications. Figure 1-1 shows the Mini-Exchange.

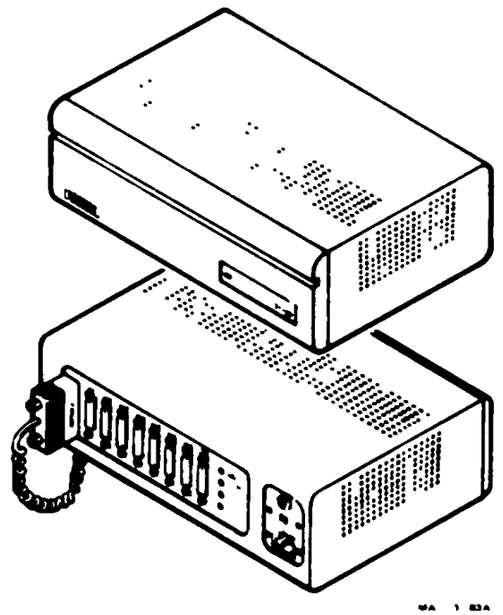

Figure 1-1 The Mini-Exchange

1.2 MINI-EXCHANGE

The Mini-Exchange system is a microprocessor-controlled communications switch It uses commands from your computer, or appropriate communications software, to connect a tot eight devices in a 60 m (200 ft) radius These devices can be personal computers, printers, or a modem . e modem can only connect to port 8) You can communicate with remote computers or host systems beyond the 60 m (200 ft) radius by using an auto-answer/autodial modem with the Mini-Exchange system or an auto-answer modem connected to a host computer

The Mini-Exchange switch has eight ports These ports are compatible with the Electrical Industry Association (EIA) RS232/RS423 pin connector standard There is a row of four diagnostic lights on the connector panel at the rear of the unit The green light on the front of the unit tells you that the power is turned on When this light does not turn on, your system unit is not operational

With a single Mini-Exchange configuration, each personal computer can access any other device connect ed to the Mini-Exchange system Figure 1-2 shows how the Mini-Exchange may be configured Each Mini-Exchange configuration supports up to four connections at the same time For example, a personal computer can print a file to a printer while at the same time another personal computer is transferring files Personal computers may also receive information from a remote host system through a modem attached to port 8 Each device connects to one other device at one time, multiple connections to one port are not possible After you make the connection, the Mini-Exchange system has no effect on the communications link until one of the devices drops the proper modem signal

The Mini-Exchange system can be used with the standard asynchronous communications software packages offered for all Digital personal computers If you use this software, you only need to remember the port number associated with your connector. A personal computer emulating a terminal can make a connection through the system without any special software Refer to the *Mini-Exchange Installation/Owner's Manual* for information on how to make a connection

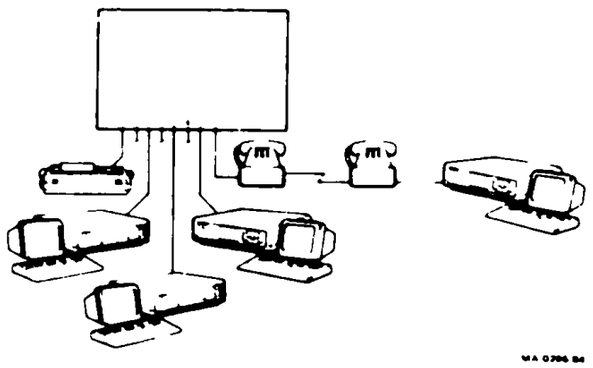

Figure 1-2 Configuration of the Mini-Exchange

1.2.1 Loopback Connector

The loopback connector and the diagnostic lights (on the rear panel) are used during the loopback connector test to check the operation of each connector on the Mini-Exchange system The loopback connector is attached to the bottom of the system unit

1.2.2 Cables and Connectors

If you have a modem, you can attach it to port 8 of your Mini-Exchange system Use the modem adapter cable (PN BC17R-0F) to attach to an EIA RS232/423 standard cable (PN BCC04) This cable allows you to place the modem up to 60 m (200 ft) away from the Mini-Exchange unit. All other devices, such as a personal computer or printer, may be connected with BCC04 cables

1.3 RELATED DOCUMENTS

The following is a list of related documents for the Mini-Exchange

Mini Exchange Installation/Owner's Manual	EK-DFMSA-IN
Mini Exchange Pocket Service Guide	EK-DFMSA-PS

1.4 SITE SELECTION AND PREPARATION

Use the following guidelines when positioning the Mini-Exchange.

- Allow six inches on all sides and the top of the Mini-Exchange for adequate airflow
- Keep all ventilation ports clear
- Avoid direct sunlight
- Locate the Mini-Exchange within 2 m (6 ft) of a power source
- Allow room for connection of cables
- Place all cables away from traffic areas

WARNING

If you place the Mini-Exchange system on a shelf, make sure the weight of the cables does not tip the Mini-Exchange system.

1.5 CIRCUIT BOARDS

The following is a brief description and gives the location of the three circuit boards that make up the Mini-Exchange

1. *Logic board* is a standard 8 × 10 4 inch printed circuit board It contains the CPU, EPROM, buffers, decoders, multiplexers, control registers, drivers and receivers This board is on the bottom of the box, component side up The logic board is connected to the connector board through two 50-pin connectors, and is also connected to the power supply board with a quick-release cable. See Chapter 2 for more information on the logic board

2. *Connector board* is a nonstandard 3 4 × 8 inch printed circuit board It has eight connectors and four diagnostic LEDs. This board is vertically mounted at the rear of the Mini-Exchange with its eight connectors and four LED's facing out of the box See Chapter 3 for more information on the connector board

3. *Power supply board* is a standard 3 2 × 10.4 inch printed circuit board. It is a switcher-type power supply that has rectifier circuits, regulator circuits, and a comparator that maintains the three dc output voltages at their proper level This board has two connectors One is an eight-pin and the other is a four-pin connector. The eight-pin connector supplies the dc voltages to the logic board. The four-pin connector receives the ac line voltage from an external source The power supply board is vertically mounted at the front of the Mini-Exchange, component side facing in See Chapter 4 for more information on the power supply board

Figure 1-3 shows how each board fits together to form the Mini-Exchange

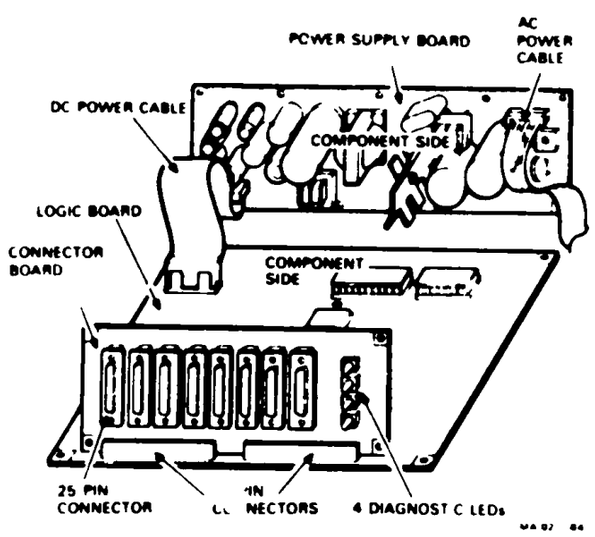

Figure 1-3 Mini-Exchange with Cover Removed

1.6 SPECIFICATIONS

1.6.1 Physical

The following are the dimensions of the Mini-Exchange

Length	12 5 in
Width	9 0 in
Height	4 0 in
Weight	6 0 lb

1.6.2 Power

The following are the power requirements for the Mini-Exchange See Chapter 4 for more on the power supply

Power supply type	Switcher
Vac input	Switch selectable
115 Vac nominal	90 to 128 V rms, 50 to 60 Hz line frequency
230 Vac nominal	180 to 268 V rms, 50 to 60 Hz line frequency
Power consumption	15 watts typical, 33 watts maximum
Circuit protection	0 75 A fuse (time delay)

1.6.3 Environment

The following are environmental requirements for the Mini-Exchange

Temperature	5 to 50° C (41 to 122° F)
Humidity	10% to 95% relative humidity
Maximun wet bulb	32° C (90° F)
Minimum dew point	2° C (36° F)

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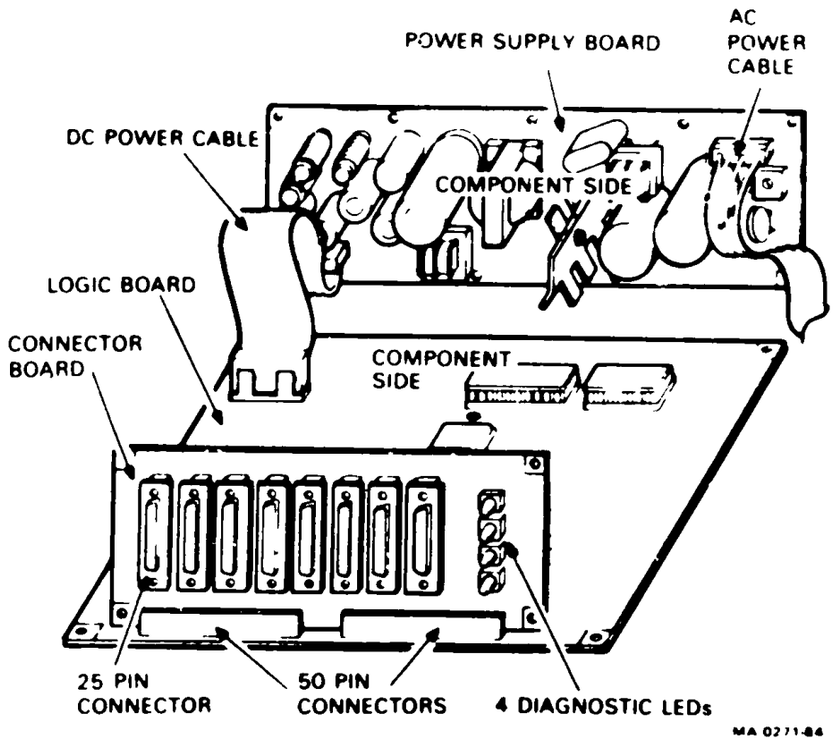

Figure 1-3 Mini-Exchange with Cover Removed

CHAPTER 2

CHAPTER 2
LOGIC BOARD

2.1 INTRODUCTION

The logic board contains the central processor unit (CPU) and circuits that support its operation The support chips allows the CPU to communicate with devices mounted on the logic board and with peripheral devices attached to the connector board on the rear panel of the Mini-Exchange Figure 2 1 shows the component side of the logic board.

The support circuits on the logic board are memory, buffers, decoders, multiplexers, control registers, and the drivers and receivers. The memory consists of external program memory The buffers consist of high and low address buffers and one data buffer The decoders consist of program memory decoder and address decoders The multiplexers consist of eight port multiplexers and one universal asyncronous receiver transmitter (UART) multiplexer. The registers consist of 16 control registers The drivers and receivers consist of 40 interface drivers (five on each port) and 21 interface receivers (two on each port with two more on port 8 and three that are shared by each port)

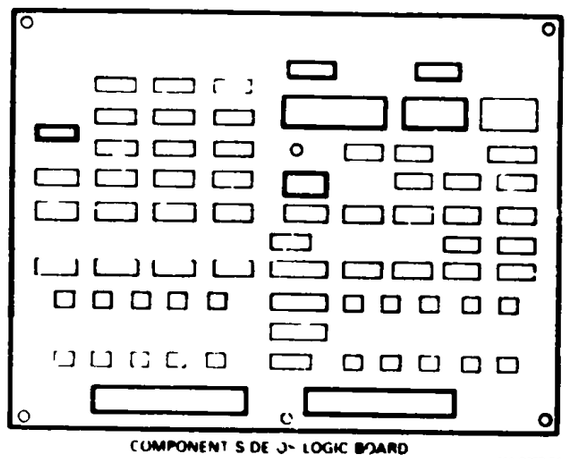

Figure 2-1 Component Side of Logic Board

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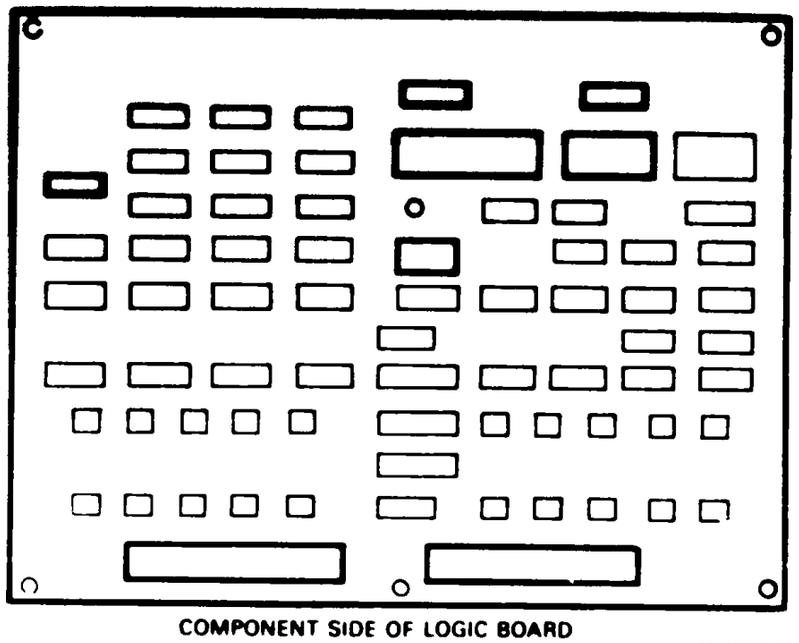

Figure 2-1 Component Side of Logic Board

2.2 FUNCTIONAL DESCRIPTION

The following paragraphs describe the basic functions performed by the devices and circuits that are on the logic board

Figure 2-2 shows the functional block diagram of the logic board Refer to this figure for the following discussion

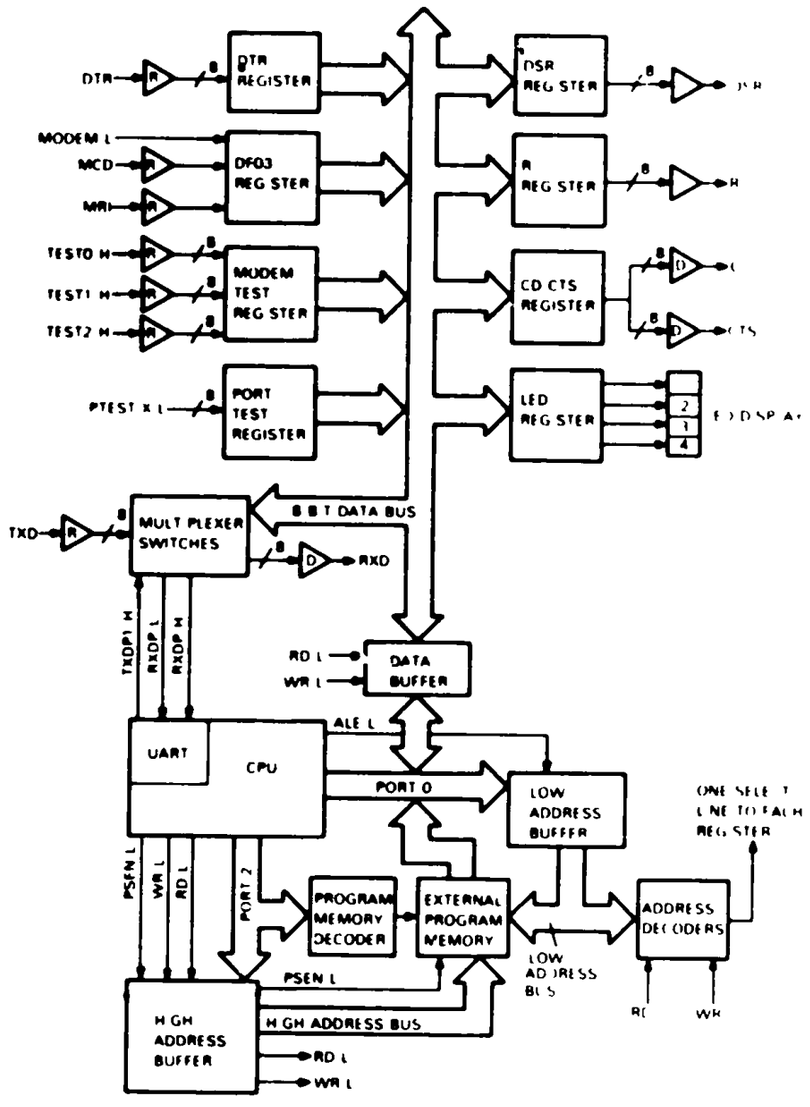

Figure 2-2 Logic Board Functional Block Diagram

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2.2.1 Central Processor Unit (Figure 2-2)

The CPU is a 40-pin single-chip microcomputer (8031) It uses external erasable programmable read only memory (EPROM) for program storage The CPU reads the program from the external program memory and executes the instructions stored there The CPU uses a high and a low address to fetch and send data to the logic board

The CPU's main elements are an arithmetic logic unit (ALU), accumulator, working registers, and conditional branching logic For transmitting and receiving serial data the CPU has a UART

2.2.2 Program Memory

The program memory is stored in one (4K × 8) bank of EPROM located outside the CPU chip The CPU uses the program memory read timing cycle to fetch the program from this device. This cycle is one of three the CPU uses to get program and data information from the support chips on the logic board

This is the only program memory storage device in the Mini-Exchange There are provisions for memory expansion

2.2.3 Buffers

There are three types of buffers on the logic board The first two described are address buffers and the third is a data buffer

2.2.3.1 High Address Buffer – This buffer is a dual 4 bit octal buffer that transfers the high address from the CPU to the program memory Also, the high address buffer transfers three data control signals from the CPU to appropriate devices. These control signals are program memory read control (PSEN), read control (RD), and write control (WR) See Section 2 3 for more information on PSEN, WR, or RD signals

2.2.3.2 Low Address Buffer – This buffer is an 8-bit transparent latch device It transfers the low address from the CPU to the program memory and the address decoders.

2.2.3.3 Data Buffer – This buffer is an octal tri-state transceiver It transfers data between the CPU and control registers

2.2.4 Address Decoders

There are three address decoders that are high speed 1-of-8 decoders. They decode an address, from the low address bus, and select one of 16 registers for data transfer Two of these decoders enable the write registers and the other enables the read registers

2.2.5 Program Memory Decoder

This is a high speed 1-of-4 decoder It decodes an address, from the low address bus, and selects one of four different external program memory configurations At this time the program memory decoder selects one program memory location (SELA) for all program instructions because three of these locations are inoperative

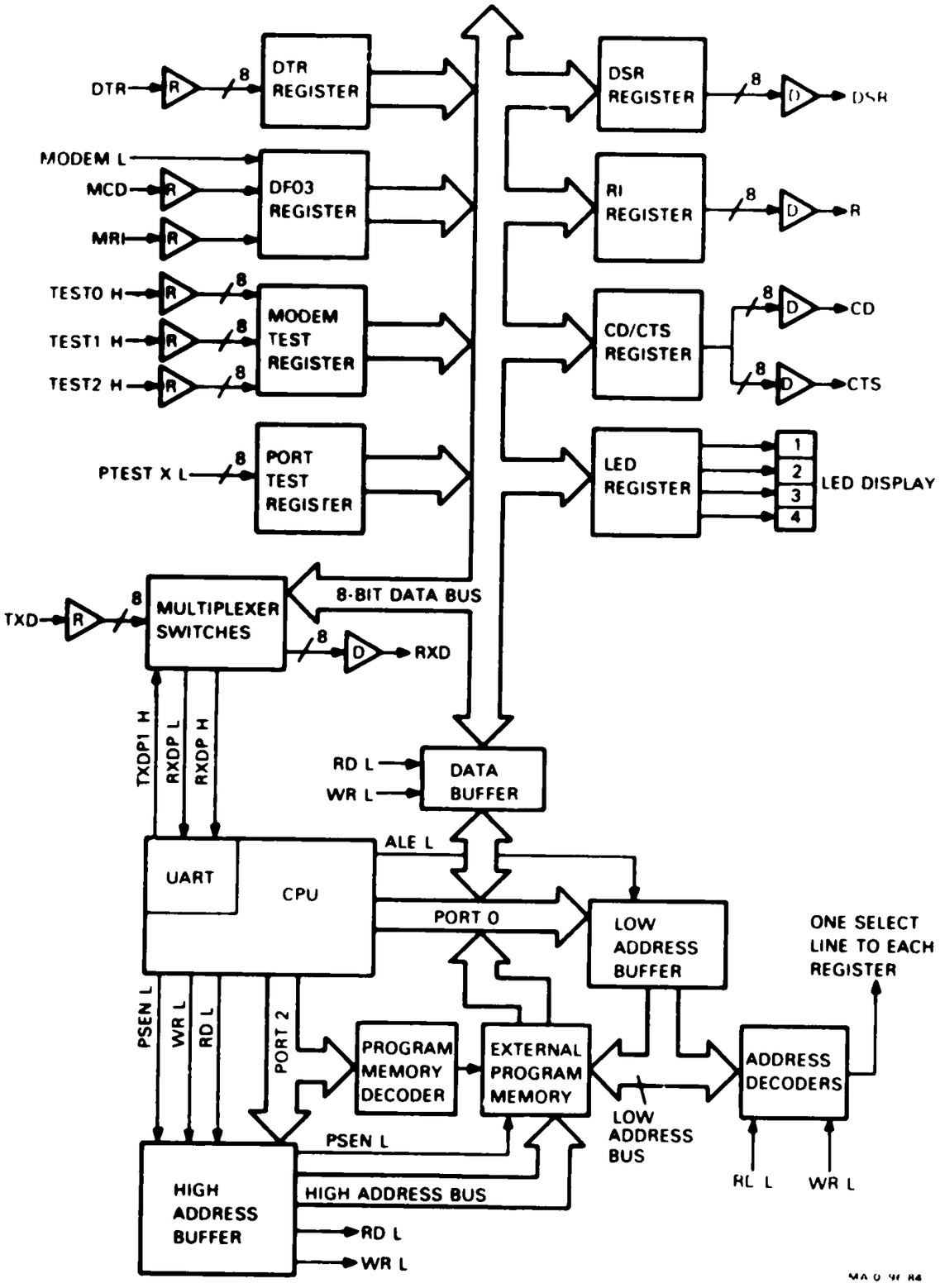

Figure 2-2 Logic Board Functional Block Diagram

2.2.6 Multiplexers

There are nine high speed 8 input multiplexers on the logic board They select one of eight input data lines and put it on their output line Eight of the multiplexers are port multiplexers and connect one communi cation port to another The other multiplexer is a UART multiplexer and transfers connection request data to the CPU for processing

For example, after port A asserts the proper modem control signals, it sends in a request (by way of the UART multiplexer to the CPU's UART) to be connected to port B If the requested port, port B, is not busy and returns the proper signals, the CPU enables port A's and port B's multiplexer These two multiplexers are latched together so that the transmitted data coming in port A is routed through port A's multiplexer to port B's multiplexer and then out port B When the CPU establishes a connection between the ports, the CPU is no longer involved with either of the port's multiplexers until one of the devices drops the proper modem control signal When this happens, the CPU starts the disconnection process

2.2.7 Write Control Registers

For the sake of clarity, the control registers that writes to the CPU will be called write registers These registers hold status information from the data bus Once enabled, they transfer data directly to the appropriate device

Here are the control registers (write only) and their functions

- Multiplexer control registers These quad edge-triggered D flip-flops enable and select multiplexers
- Data set ready (DSR) control register – This 8-bit latch controls the DSR discrete lines
- Ring indicator (RI) control register – This 8-bit latch controls the RI discrete lines
- Carrier detect (CD) control register This 8-bit latch controls the CD discrete lines
- LED display register This quad edge-triggered D flip-flop controls the LED display

2.2.8 Read Control Registers

For the sake of clarity, registers read by the CPU will be called read registers They transfer data directly to the data bus when addressed and enabled The CPU reads these regularly and performs the appropriate action when a status change occurs

Here are the control registers (read only) and their functions

- Data terminal ready (DTR) control register – This dual quad buffer indicates which of eight DTR discrete lines are asserted
- DF03 modem control register – This half of a dual quad buffer indicates which of three discrete modem lines are asserted when a modem is connected to port 8
- Modem control test register – This half of a dual quad buffer indicates which of three discrete test lines are good during loopback testing
- Port test register – This 8-line buffer indicates which port has the loopback test plug connected to it when used

2.2.9 Drivers

There are 40 driver circuits on the logic board, five for each port The drivers convert TTL voltage levels used by the circuits in the Mini-Exchange into the EIA voltage levels Five signals DSR, RI, CD, CTS, and Receive Data (RXD) are transmitted from the Mini-Exchange to a connected device

2.2.10 Receivers

There are 21 receivers on the logic board, two on each port with two more on port 8 and three that are shared by each port The receivers convert EIA voltage levels received by the Mini-Exchange into TTL voltage levels the internal circuits can use The two signals for each port are the DTR and transmit data (TXD) The two on port 8 are the MCD and MRI signals The three shared by each port are Test 0 through Test 2 signals

2.3 DETAILED DESCRIPTION

The following describes in detail logic board functions

To understand the CPU's functions refer to the following books

Intel MCS 51 User's Manual
Intel Microcontroller User's Manual

2.3.1 Central Processor Unit

The CPU is an 8031 microcomputer It is installed in a 40-pin package and uses a 5 V power supply On this single chip the 8031 has CPU, volatile read/write data memory, and a serial I/O channel for the UART The 8031 also uses an external oscillator for clock timing and uses 20 of 32 I/O lines The CPU also contains internal data memory described below Figure 2-3 is a block diagram of the CPU

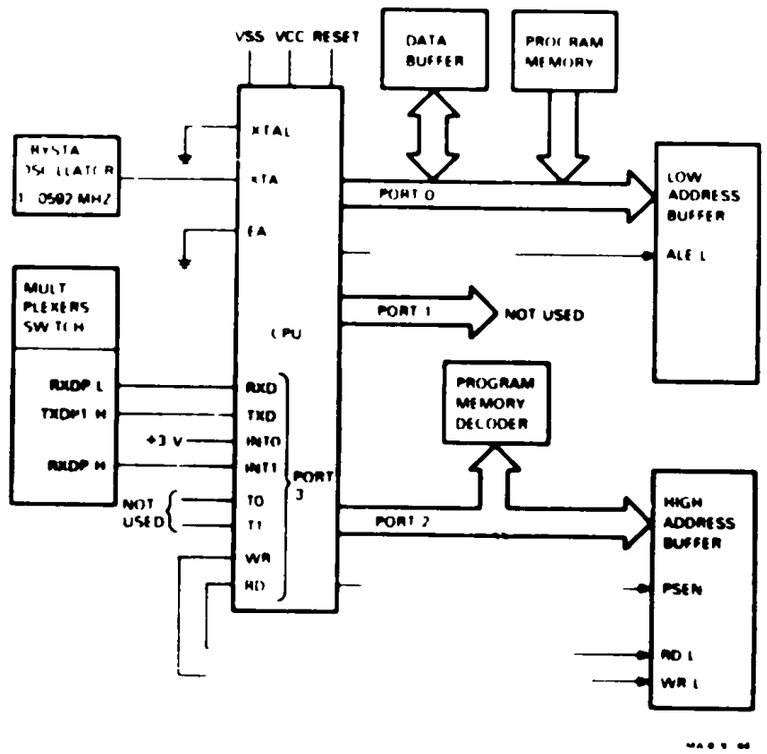

Figure 2-3 CPU Block Diagram

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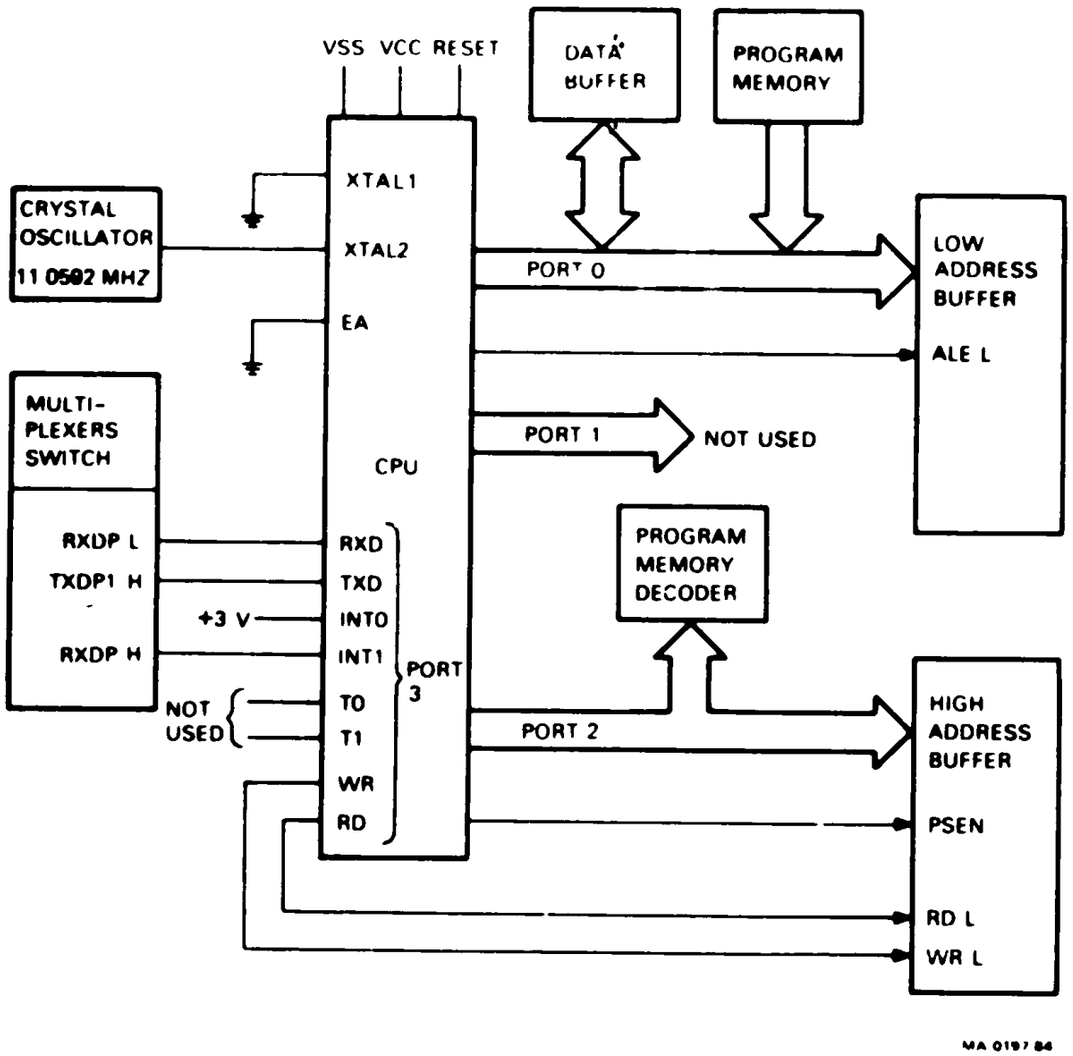

Figure 2-1 CPU Block Diagram

2.3.1.1 Internal Data Memory - The CPU has 256 individually addressable bytes of internal data memory. The first 128 bytes are in the internal data random access memory (RAM) and the second 128 bytes are in the special functions register. Locations 0 through 31 contain four 8-register banks. In addition, 128 bit locations of the on-chip RAM are accessible through direct addressing and are at byte location 32 through 47. Locations 48 to 127 contain general purpose RAM. The stack can be anywhere in internal data RAM. The special function register has all registers except the program counter and the four 8-register bands. This special function register's address space is 128 through 255. Figure 2-4 shows the internal data memory.

2.3.1.2 CPU Pin Descriptions - Table 2-1 describes the function of the pins on the CPU. Figure 2-5 shows the CPU pinning diagram.

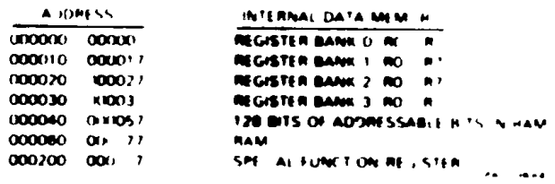

Figure 2-4 Internal Data Memory

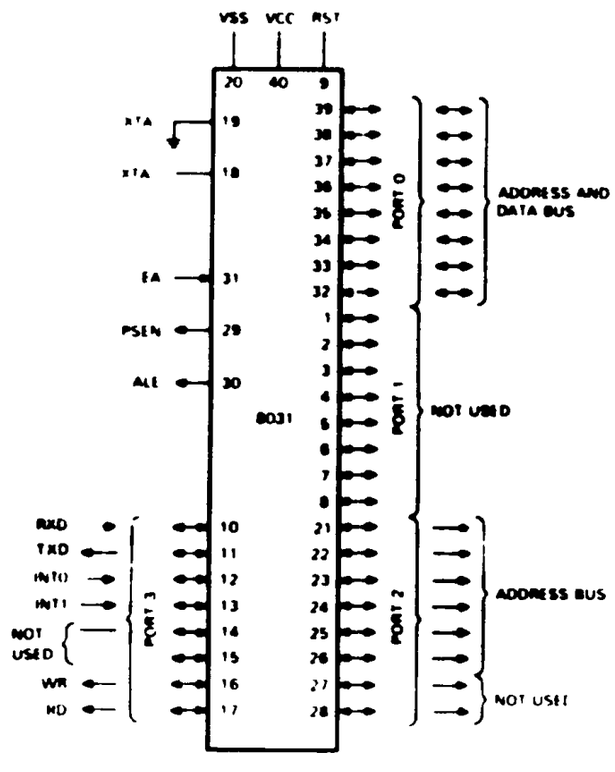

Figure 2-5 CPU Pinning

Table 2-1 CPU Pin Descriptions

Pin	Function
Vss	Circuit ground
Vcc	+5 Vdc power
Port 0	Port 0 is an 8-bit bidirectional input/output port. It is the multiplexed low-order address and data bus
Port 1	Not used
Port 2	Port 2 is used for the high-order address bits when accessing external memory
Port 3	Port 3 contains interrupts, serial port, and these RD and WR pins
	RXD (RXDP L) The serial port's receiver data input asynchronous
	TXD (TXDP1 H) The serial port's transmitter data output (asynchronous)
	INT0 (+3 V) The interrupt 0 line and is not used
	INT1 (RXDP H) The interrupt 1 line
	RD (RD L) - The read control signal enables external data on the data bus to port 0
	WR (WR L) - The write control signal latches the data word from port 0 onto the data bus
ALE (ALE L)	Provides address latch enable output used for latching the address into the low address buffer
PSEN (PSEN L)	The program store enable output is a control signal that enables the external program memory to the bus during fetch operations
EA	This pin is held low by jumper W1. This jumper allows the 8031 CPU to fetch all instructions from external program memory.
	When W1 is removed, the CPU fetchs internal memory first
XTAL1	Pin grounded
XTAL2 (PCLOCK H)	This is the input from the crystal oscillator output
RST (RESET H)	The CPU resets when this pin toggles from a low to a high

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ADDRESS	INTERNAL DATA MEMORY
000000 – 000007	REGISTER BANK 0 (R0 R7
000010 – 000017	REGISTER BANK 1 (R0 R7
000020 – 000027	REGISTER BANK 2 (R0 R7
000030 – 000037	REGISTER BANK 3 (R0 R7)
000040 – 000057	128 BITS OF ADDRESSABLE B TS N RAM
000060 – 000177	RAM
000200 000377	SPECIAL FUNCTION REGISTER

MA 0148 84

Figure 2-4 Internal Data Memory

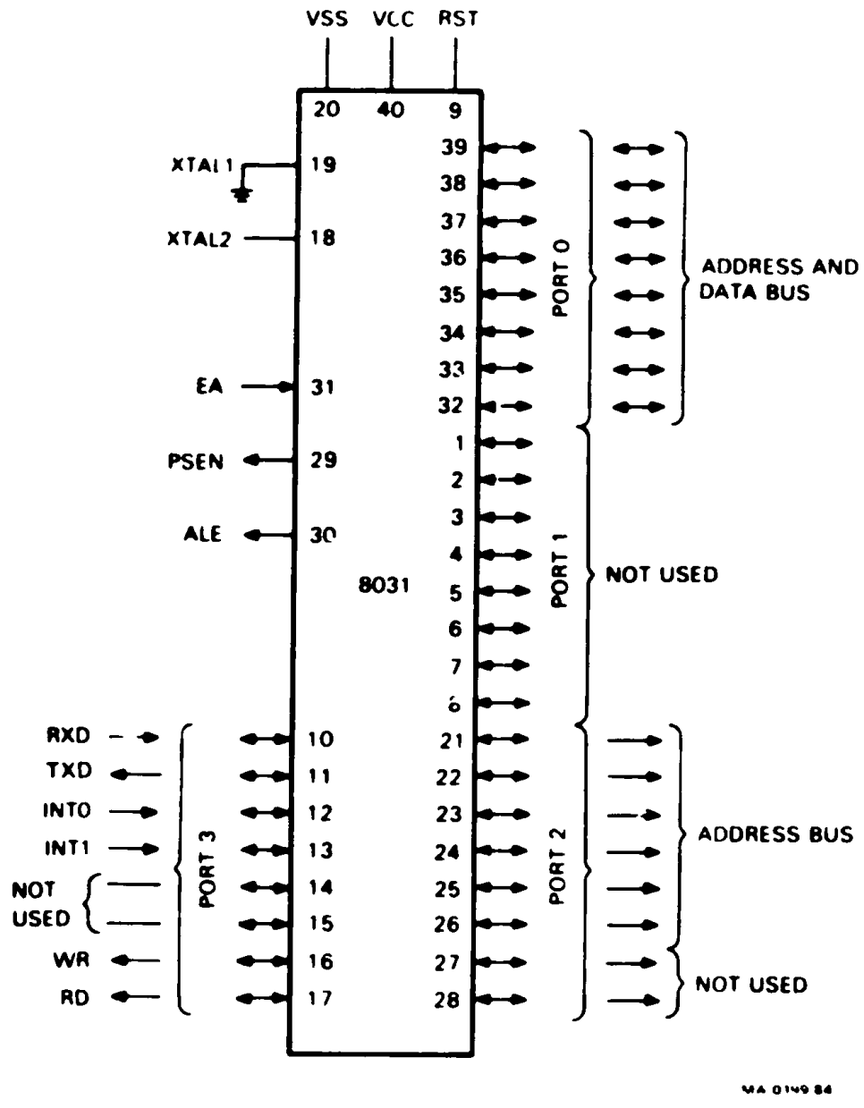

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Figure 2-5 CPU Pinning

2.3.2 Program Memory

The EPROM has two control functions which must be actively low to obtain data at the outputs SELA, the chip enable, is used to select the device PSEN, the output enable control, is used to gate data to the output pins, independent of chip enable

The program memory configuration jumpers route the program memory chip enable signals differently if a CPU other than the 8031 is used Table 2-2 shows the different configurations of the program memory configuration jumpers

Figure 2-6 is a block diagram of the EPROM

Table 2-2 Program Memory Configuration Jumpers

Jumper	Status	Function
W1	Installed	All instruction fetches are made from external program memory This jumper must be installed when the 8031 microprocessor is used
	Removed	Instruction fetches 0 through 4K are made from internal program memory External instruction fetches occur automatically when the program counter is above 4095 When W1 is removed, W2 must also be removed
W2	Installed	This jumper enables external program memory for Bank1 It must be installed when using the 8031 microprocessor When this jumper is used, W3 must be removed
	Removed	This jumper is removed if the CPU uses internal program memory for Bank1
W3	Installed	External memory Bank1 is mapped into Bank3 This allows a total of 12K for program memory if internal program memory is used W2 must be removed when W3 is installed
	Removed	This jumper must be removed when W2 is installed

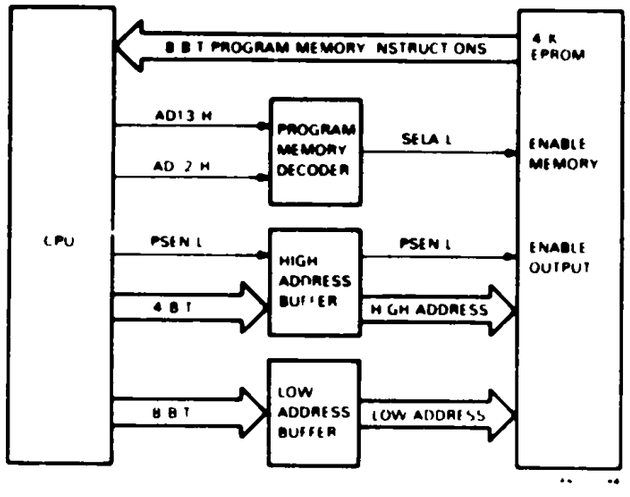

Figure 2-6 EPROM Block Diagram

Figure 2-7 shows the program memory read cycle timing Refer to this figure for the following discussion.

The following must occur before data is available at the outputs

1. An address is emitted from the CPU during the program memory read timing cycle
2. The high address is buffered through the high address buffer and arrives at EPROM
3. The low address is buffered through the low address buffer and arrives at EPROM The ALE signal latches the low address onto the low address bus at this time
4. The chip enable signal (SELA) from the program memory decoder must toggle low and stay low during the timing cycle
5. The output enable signal (PSEN) from the CPU must toggle low and stay low during the timing cycle
6. The CPU then floats (high impedence state) its bus drivers for one clock pulse and then waits for the program at port 0
7. Valid program instruction data is available on the bus at this time When PSEN returns to the high level, EPROM then has its buffers float, relinquishing the bus again

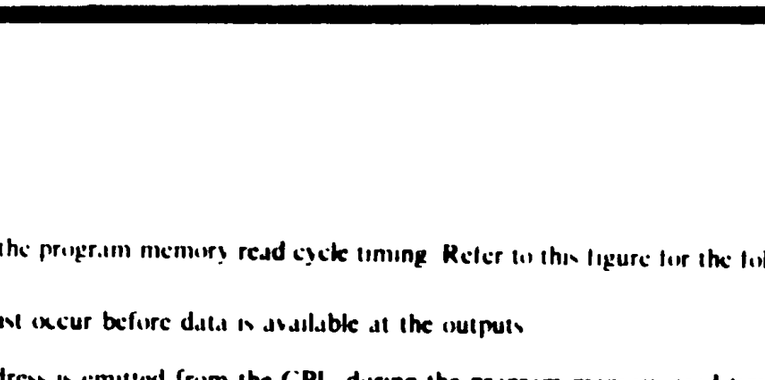

Figure 2-7 Program Memory Read Cycle Timing

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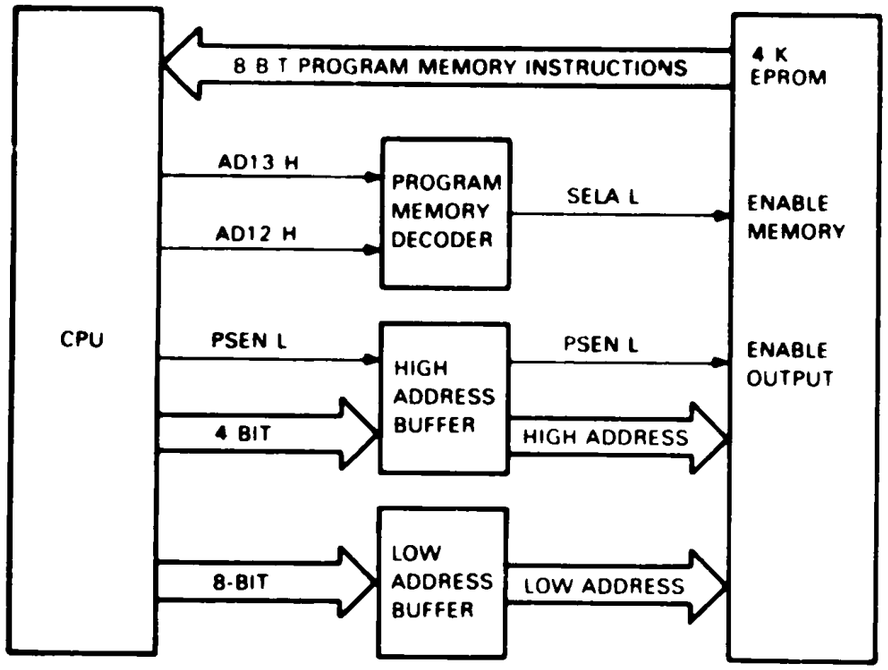

Figure 2-6 EPROM Block Diagram

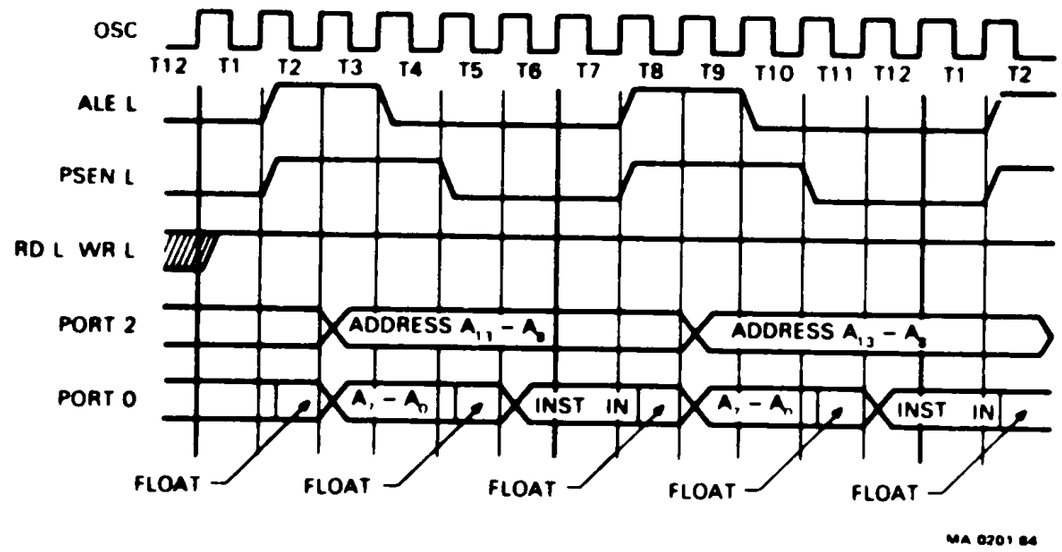

Figure 2-7 Program Memory Read Cycle Timing

2.3.3 Buffers

There are three types of buffers on the logic board The first two described are address buffers and the third is a data buffer

Figure 2-8 shows the three buffers with the buses Refer to this figure for the following discussion

2.3.3.1 High Address Buffer (Figure 2-8) – This buffer is a dual 4-bit octal buffer The CPU uses this buffer to drive the high address and three control signals to additional devices since the CPU cannot drive more than one TTL device Since the chip enable circuits are tied low by a grounded resistor (soft ground), the signals are sent through this buffer as soon as they are emitted from port 2 on the CPU The signals from the CPU on the high address bus are a 4-bit byte that uses half of the buffer The other half drives the PSEN signal, the RD (read) signal, and the $\overline{WR}$ (write) signal These signals are also sent through the buffer as soon as they are emitted from the CPU

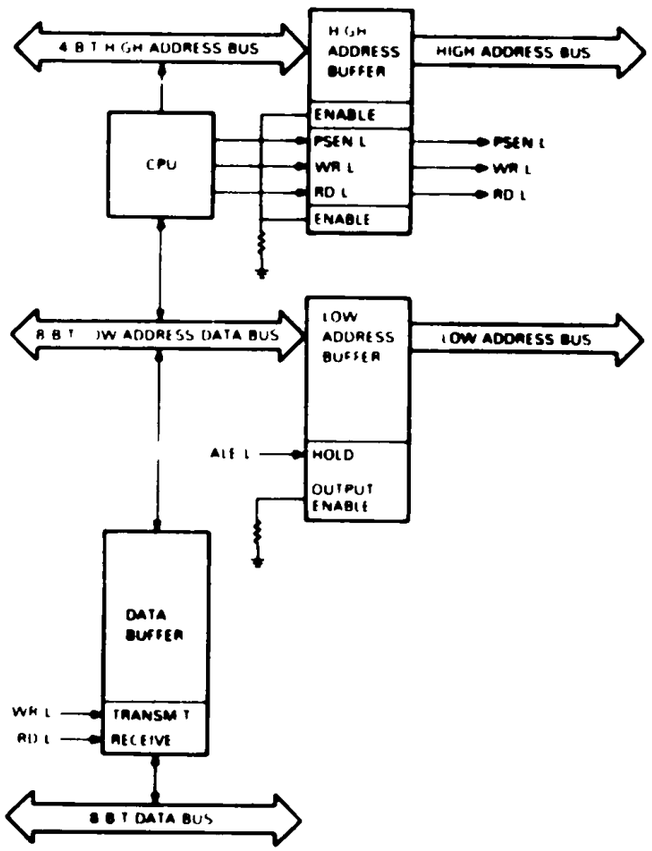

Figure 2-8 System Block Diagram with Buses and Buffers

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2.3.3.2 Low Address Buffer – This buffer is an 8 bit transparent latch device The low address is emitted from port 0 on the CPU and is sent only to the low address buffer The CPU uses this buffer to drive the low address to additional devices since the CPU cannot drive more than one TTL device This chip is enabled by the ALE signal The low address is latched on the output of the buffer on the falling edge of the ALE signal The output enable circuit on this chip is tied low by a grounded resistor (soft ground).

2.3.3.3 Data Buffer – This buffer is an octal tri-state transceiver It receives data from the CPU and also sends data into the CPU from the 8-bit data bus The CPU controls how the data flows through the buffer with the RD (read) and WR (write) control signals Refer to Section 2 3 9 for more information on these signals

When the CPU is instructed to read a control register, the following occurs

1 CPU addresses a register

2 Data from that register is put on the data bus

3 CPU toggles the RD signal low to enable the data buffer for the read cycle

4 Data buffer transfers the data on the data bus to the CPU by way of the 8-bit low address/data bus

5 CPU reads the data and deals with it accordingly

If the CPU is instructed to write to a control register, the following occurs

1 CPU addresses a register through other circuitry

2 Data is emitted from port 0 on the CPU and sent to the data buffer through the 8-bit low address/data bus

3 CPU toggles the WR signal low to enable the data buffer for the write cycle

4 Data buffer transfers this data onto the data bus and to the enabled register

5 Depending on which register was addressed, it either latches a discrete signal, selects a port on one of the multiplexers, or turns on an LED.

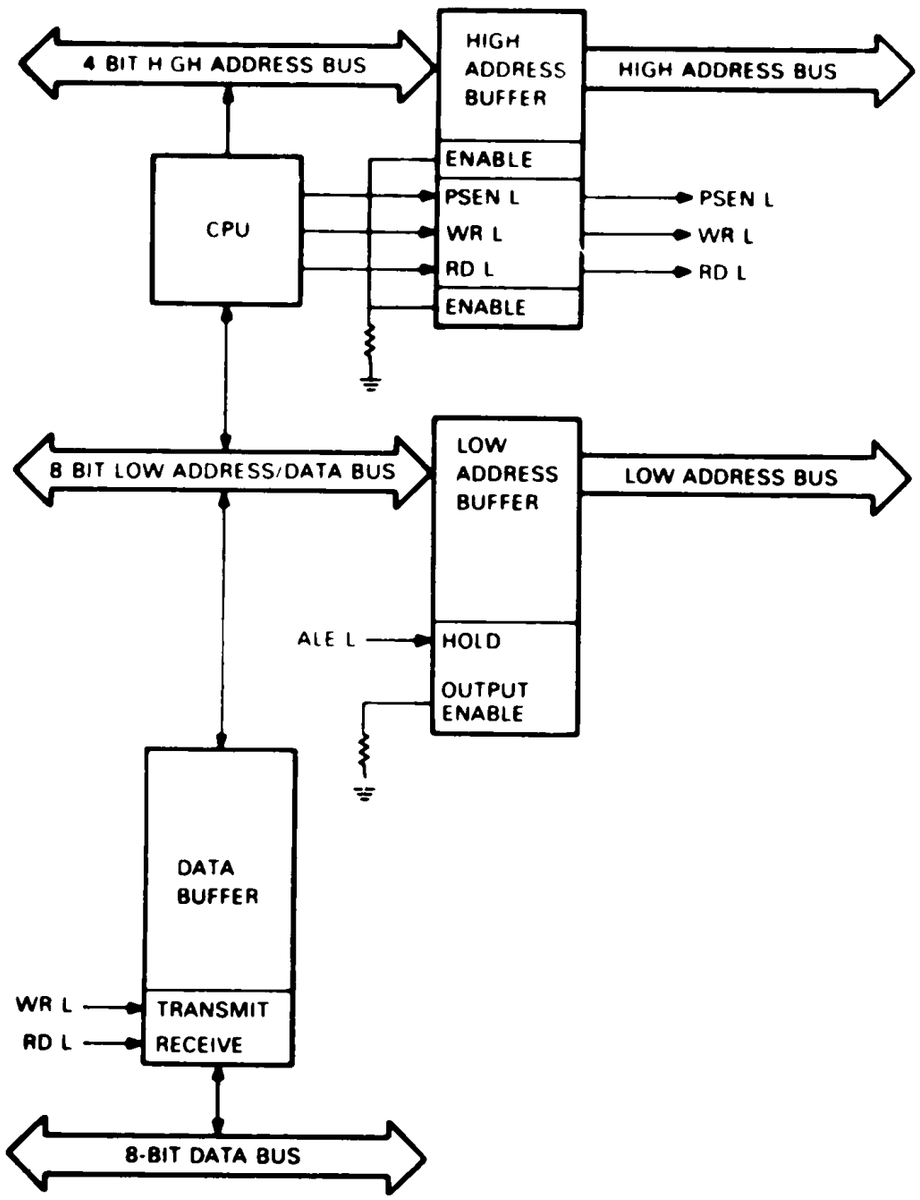

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Figure 2-8 System Block Diagram with Buses and Buffers

2.3.4 Address Decoders

There are three address decoders on the logic board. The first two described enable the write control registers. The third enables the read control registers. For the sake of clarity, the decoders that enable the write control registers will be called write address decoders and the decoder that enables the read control registers will be called the read address decoder.

Figure 2-9 shows the three address decoders and the low address bus. Refer to this figure for the following discussions.

2.3.4.1 Write Address Decoders (Figure 2-9) – There are two write address decoders. One enables eight port multiplexer control registers. The other enables a UART multiplexer control register, three discrete latch signals, and an LED display register. Both have output lines selected by the three lowest address bits (A0, A1, A2) on the low address bus. Both are enabled by the fourth address bit (A3) and the WR (write) signal. To prevent the two decoders from being enabled at the same time, the fourth address bit is inverted at the input of one of the decoder's enable circuitry.

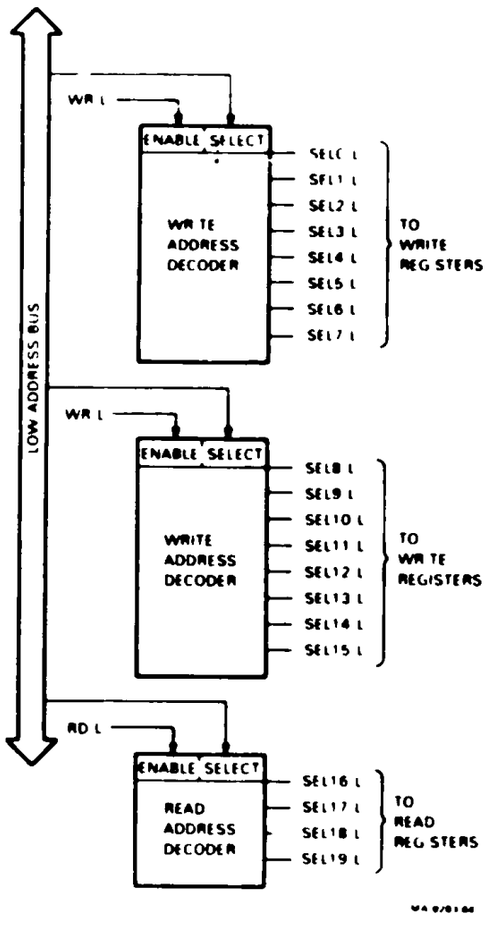

Figure 2-9 Address Decoders with Low Address Bus

The following must occur in order for a write address decoder to enable a write control register:

1. An address is emitted from port 0 of the CPU onto the low address bus.
2. The low address arrives at the address decoders through the low address buffer.
3. The WR signal goes low enabling one of the two write decoders.
4. The enabled decoder decodes the address and toggles the appropriate output line low.
5. The toggled output line enables one of the write control registers for data transfer.

2.3.4.2 Read Address Decoder (Figure 2-9) There is one read address decoder and it enables a DTR control register, a modem control register, and two test registers. As with the write address decoders, the read address decoder has the three lower address lines (A0, A1, A2) from the low address bus as its select lines. But it uses the fourth and fifth address lines (A3 and A4) from the low address bus and the RD signal from the CPU to enable it.

The following must occur in order for the read address decoder to enable a read control register:

1. An address is emitted from port 0 of the CPU and onto the low address bus.
2. The low address arrives at the address decoder through the low address buffer.
3. The RD signal is toggled low enabling the read address decoder.
4. The enabled decoder decodes the address and toggles one of the four output lines low.
5. The toggled line enables one of the read control registers for data transfer.

2.3.5 Program Memory Decoder

This decoder enables the program memory device. It uses the two highest address lines (A12 and A13) from the CPU to select an output line and is enabled through a grounded resistor (soft ground). This decoder enables the EPROM chip by toggling the SELA output line low during the program memory read timing cycle. The decoder has four output select lines. Only one is used at this time because there is only one program memory device. Figure 2-10 is a block diagram of the program memory decoder.

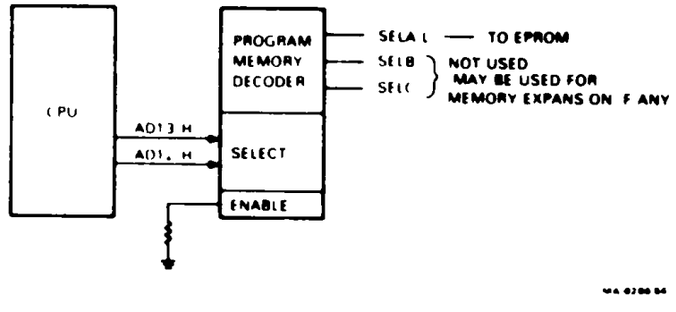

Figure 2-10 Program Memory Decoder Block Diagram

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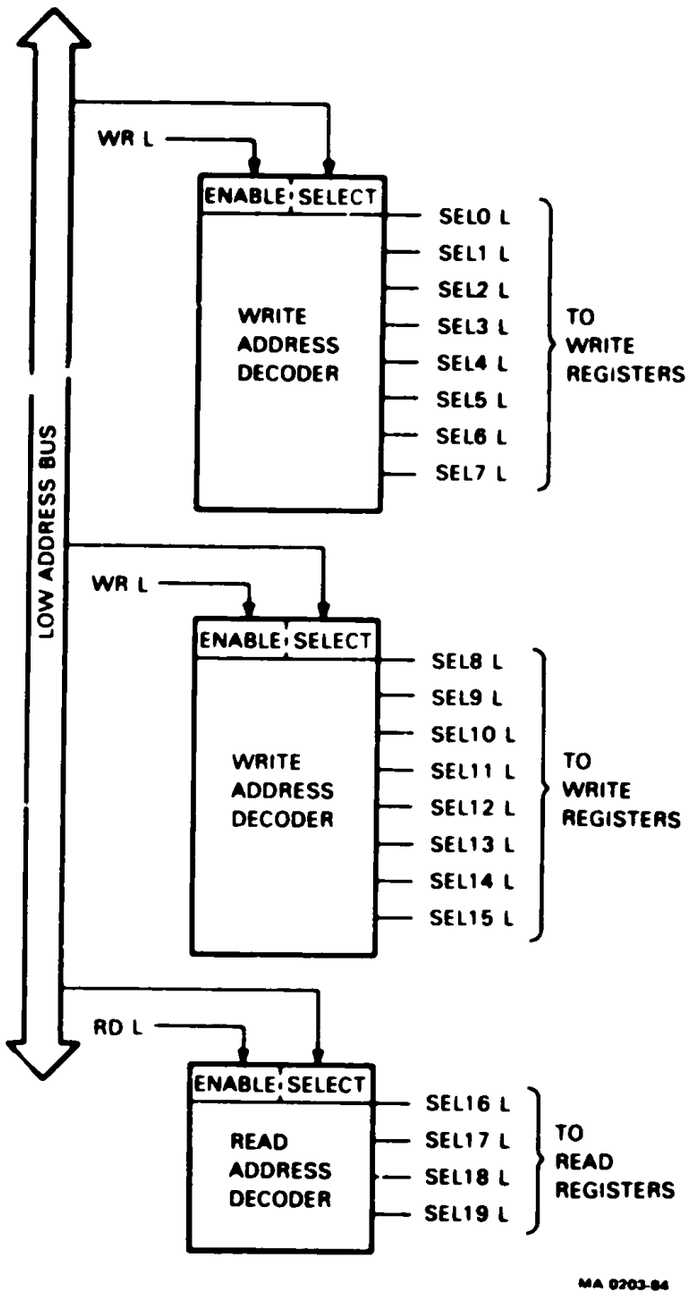

Figure 2-9 Address Decoders with Low Address Bus

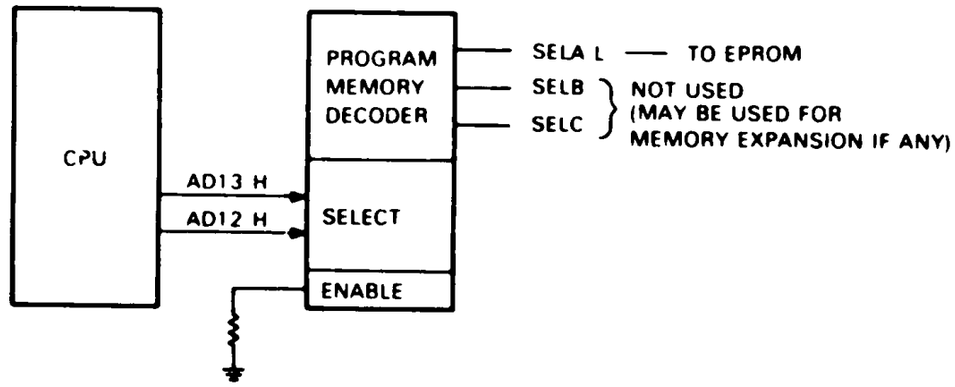

Figure 2-10 Program Memory Decoder Block Diagram

2.3.6 Multiplexers

Multiplexers do the switching for the Mini-Exchange The UART multiplexer directs the connection request data to the CPU The other eight multiplexers connect one communication port with another for data transfer For each multiplexer there is a control register that controls which communication ports are connected and when to connect them

2.3.6.1 UART Multiplexer – This multiplexer controls the serial input data lines to the UART Each communication port has its transmitted data pin (TXD) connected to the input of the UART multiplexer When the multiplexer is selected, the multiplexer allows data, from a terminal or similar device, to flow through to the UART for processing This single UART multiplexer transfers data such as the baud rate and port destination from a requesting device

Figure 2-11 is a block diagram of the UART multiplexer with its control register Refer to this figure for the following discussion

For the UART multiplexer to connect a TXD line to the UART, the following must occur

1 A terminal or similar device must send the proper modem signals to the Mini-Exchange

2 The CPU addresses and selects the UART's control register At this time information is sent on the data bus to this register.

3 The control register enables and selects the multiplexer

4 These select signals enable the one TXD line from the requesting communication port to the output of the multiplexer.

5 This data is sent to the UART for processing

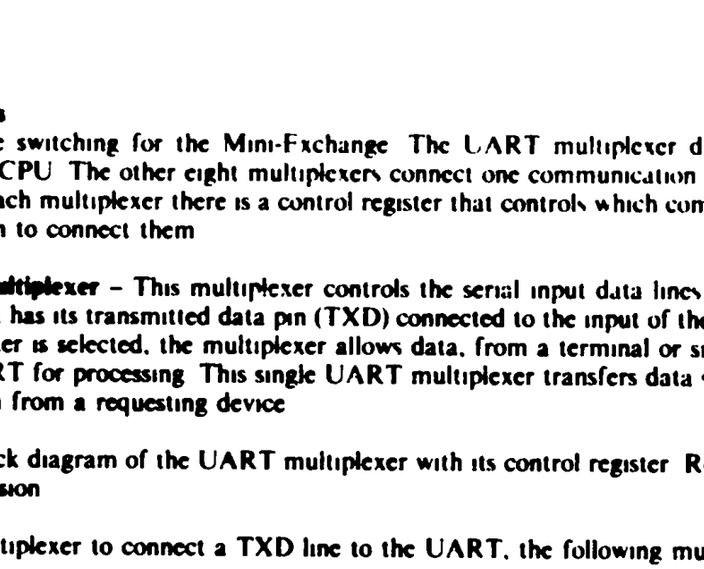

Figure 2-11 UART Multiplexer with Control Register

2.3.6.2 Port Multiplexers – These multiplexers control the data flow between the communication ports They operate similar to the UART multiplexer Each communication port has a port multiplexer's output line connected to its RXD pin Also each communication port has its TXD pin connected to each of the port multiplexer's input lines

Figure 2-12 is a block diagram of port 8's multiplexer and its control register Each of the eight ports are the same as this port except for these three differences

1 The select on the control register corresponds to the port number minus 1

2 The TXDP, from the UART is placed in the port numbers position so the UART can send data to each port when selected.

3 The RXD corresponds to the port number minus 1 The multiplexer control registers are described in Section 2 3 7

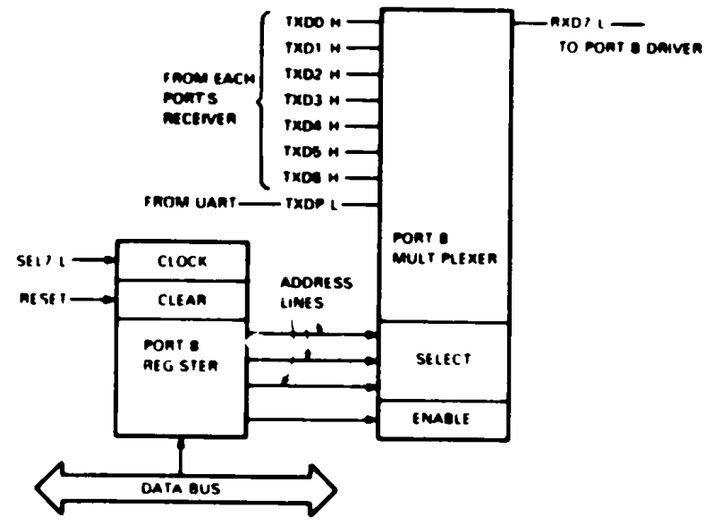

Figure 2-12 Port 8 Multiplexer with Control Register

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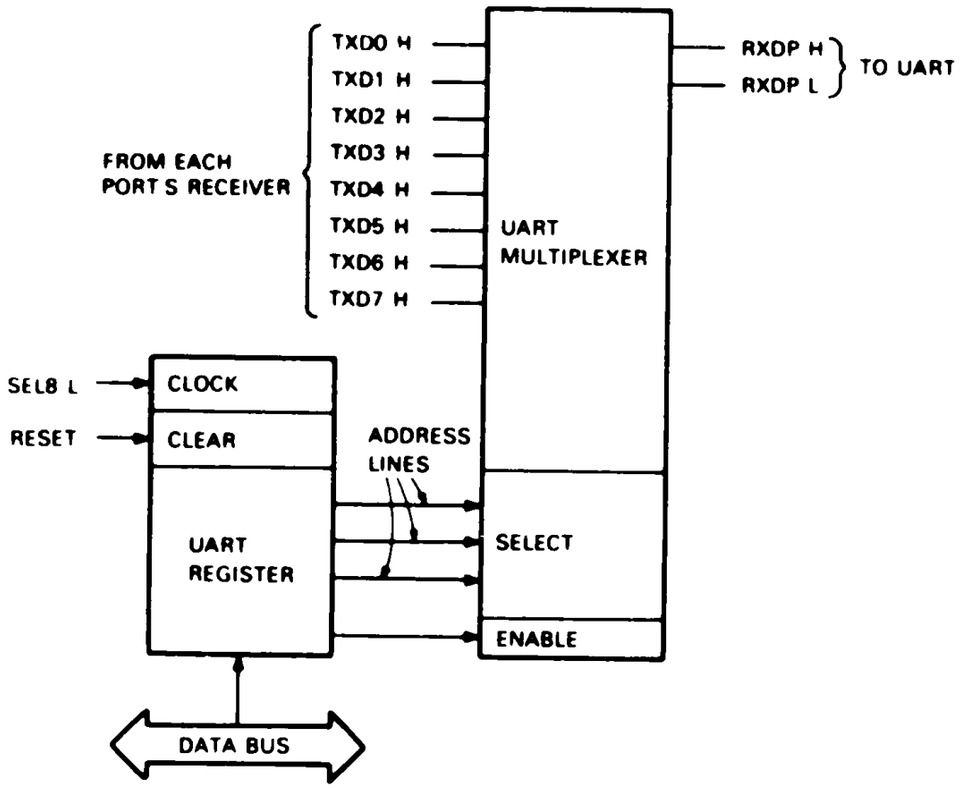

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Figure 2-11 UART Multiplexer with Control Register

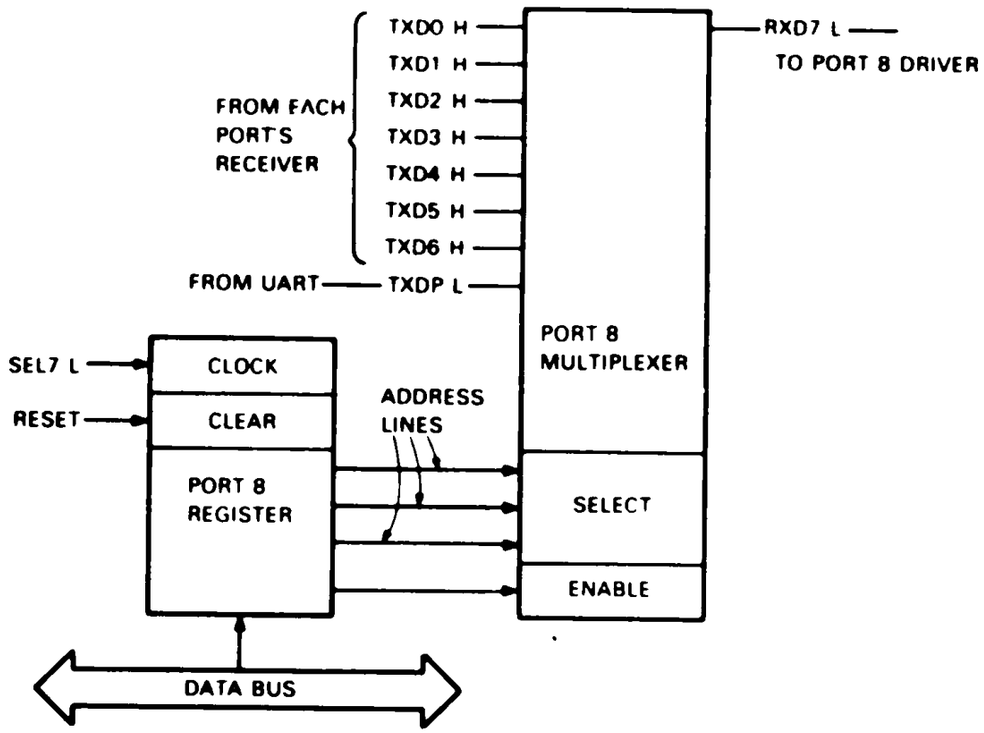

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Figure 2-12 Port 8 Multiplexer with Control Register

2.3.7 Write Control Registers

These control registers hold status information from the data bus. Once enabled, they transfer data directly to the appropriate device. See Chapter 5 for the bit definitions of these registers.

Figure 2-13 shows the write control registers with their select signals and the data bus. Refer to this figure for the following discussion.

2.3.7.1 Multiplexer Control Registers (Figure 2-13) – These registers are quad edge-triggered D flip-flops. There is one control register for each of the nine multiplexers on the logic board – eight for the port multiplexers and one for the UART multiplexer. Select signals SEL0 through SEL8 enable each of these control registers. When selected, the data from the data bus is latched at the output lines of the register. This data from the register is used to enable and select a port on the corresponding multiplexer.

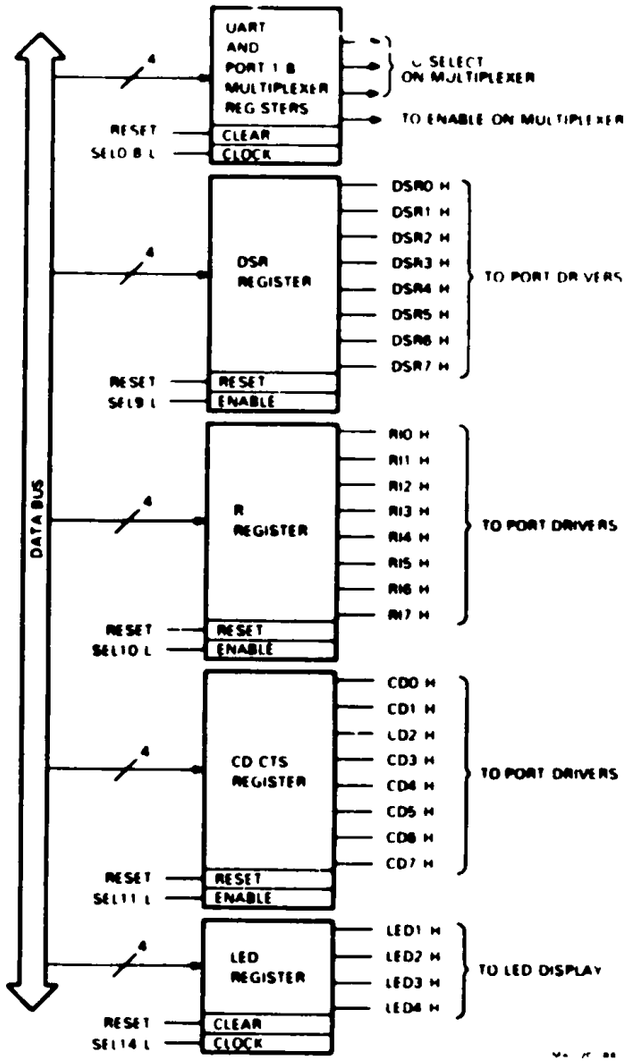

Figure 2-13 Write Control Registers with Data Bus

2.3.7.2 LED Display Register – This register is also a quad edge-triggered D flip-flop. It controls each of the four red LEDs. When the address decoders enable this chip (SEL14), the data from the data bus lights one or more of the LEDs. This register displays testing mode results.

2.3.7.3 Modem Control Registers – On the logic board three modem control registers are written to: DSR, RI, and CD/CTS. These control registers are 8-bit addressable latches. When the address decoders enable these chips, the data from the data bus latches one of the output lines. This output line is a discrete signal and latches either high or low depending on the data from the data bus.

2.3.8 Read Control Registers

These control registers hold status information from a device connected at the rear of the Mini-Exchange. All of these input signals are discrete. Once enabled, the registers transfer data directly to the data bus. See Chapter 5 for the bit definitions of these control registers.

Figure 2-14 shows the read control registers with their signals and the data bus. Refer to this figure for the following discussions.

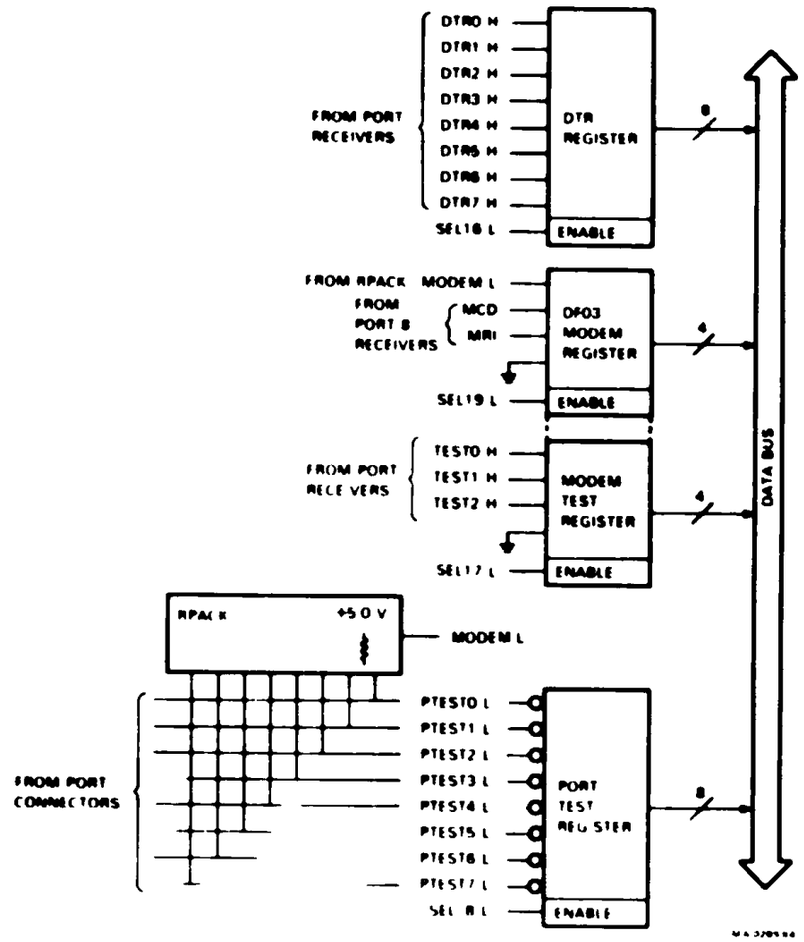

Figure 2-14 Read Control Registers with Data Bus

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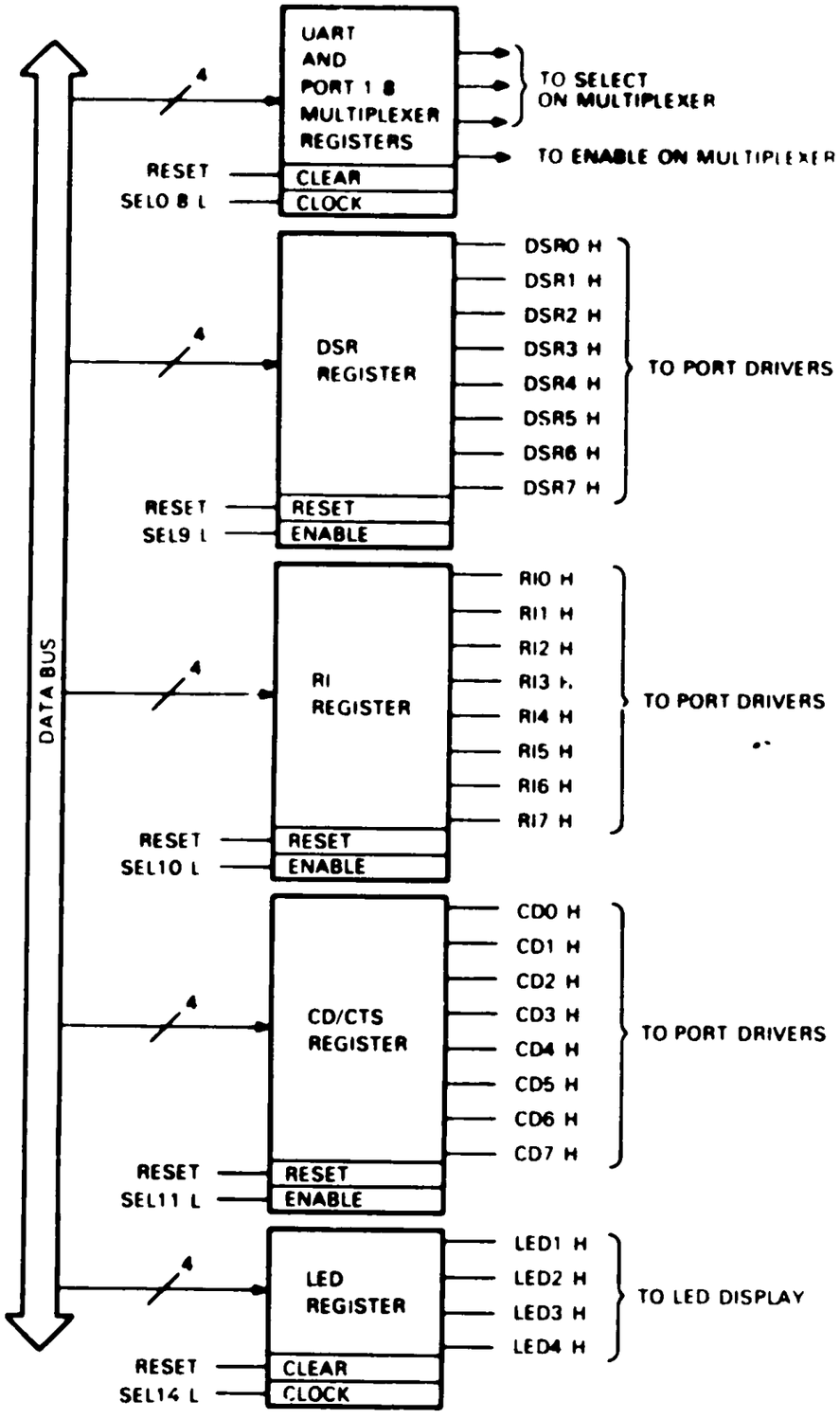

Figure 2-13 Write Control Registers with Data Bus

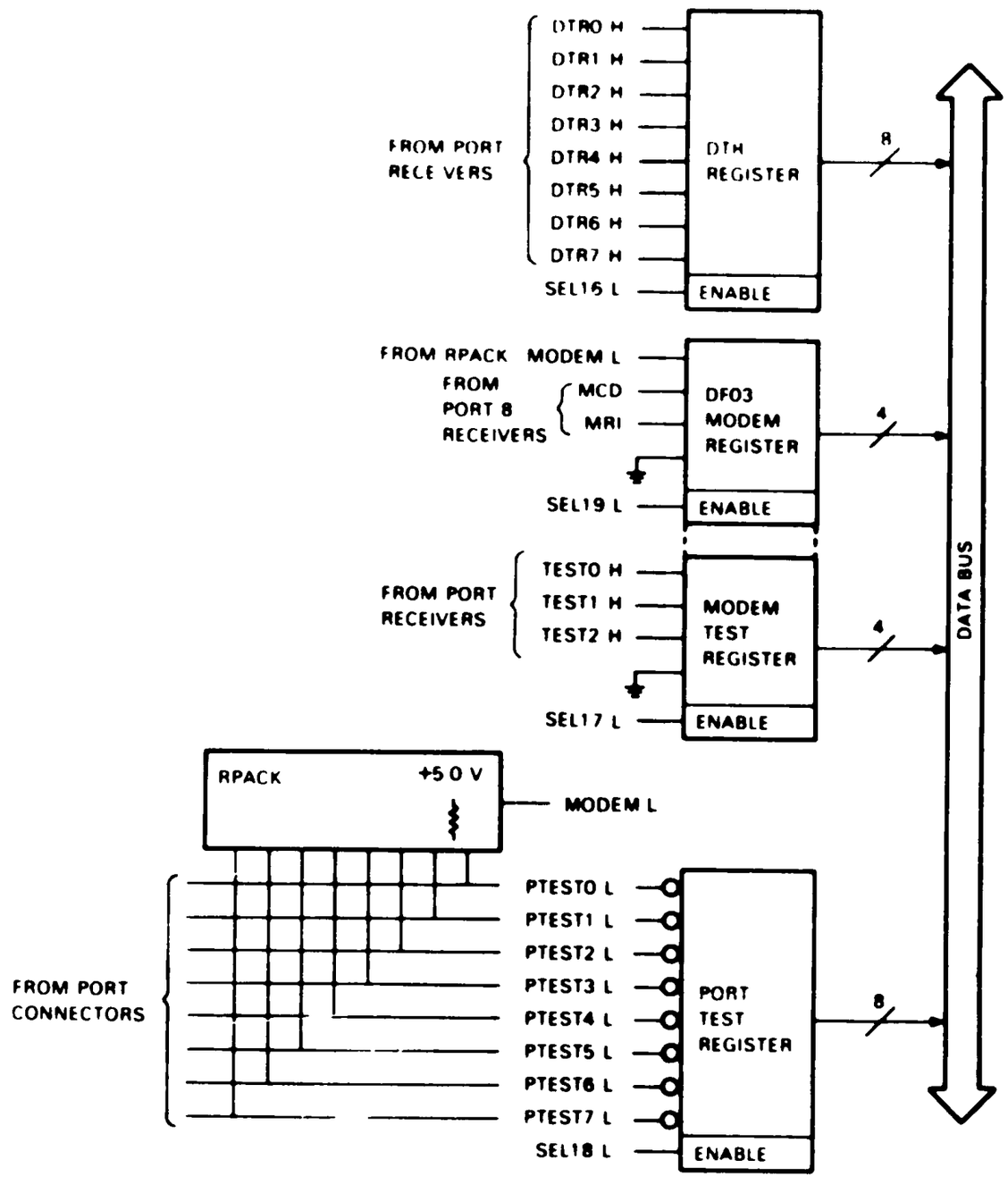

Figure 2-14 Read Control Registers with Data Bus

2.3.8.1 Data Terminal Ready (DTR) Control Register (Figure 2-14) This register is a dual quad buffer When the address decoders enable this register (SEL 16) the data from the input lines transfers to the data bus Each communication port has a DTR line connected to the DTR control register The CPU reads this DTR line to determine if a terminal is ready for data transfer

2.3.8.2 DF03 Modem Control Register – This register is half of a dual quad buffer The other half consists of the modem control test register described below

When the address decoders enable this control register (SEL 19), the data from the input lines is transferred to the data bus The data consists of the modem CD (MCD), the modem RI (MRI), and whether there is a modem cable (MODEM) attached to port 8 The MODEM line is either +5.0 Vdc or ground indicating the presence of the modem cable This control register is only used when a DF03 modem is connected to port 8

2.3.8.3 Modem Control Test Register – This register is half of a dual quad buffer When the address decoders enable this register (SEL17), the data from the input lines is transferred to the data bus This register tests the CD, CTS, and RI lines on each communication port This test register is used only when the loopback test plug is connected to a port

2.3.8.4 Port Test Register – This register is a dual quad 8-line driver When the address decoders enable this register (SEL18), the data from the input lines is transferred to the data bus This data is either +5.0 Vdc or ground which indicates the presence of the loopback test plug on one of the ports

2.3.9 Timing Cycles

2.3.9.1 Data Read Timing Cycle – The read cycle begins during T2, with the assertion of the ALE signal (Figure 2-15) The falling edge of this signal latches the address onto the low address bus This address selects which control register the read address decoder enables At T5, the address is removed from the port 0 bus The data read control signal (RD L) is asserted during T7 This signal allows the address decoder to enable the selected output line to toggle low When this happens, the data from the control register is released to the data bus The read control signal also enables the data buffer to transfer this data to the CPU for processing After T12, the read control signal returns to the unasserted state This causes the addressed device to float its bus drivers and relinquish the data bus Figure 2-15 shows the data read cycle timing

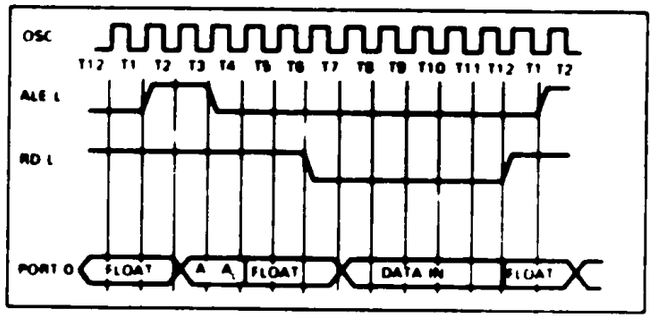

Figure 2-15 Data Read Cycle Timing

2.3.9.2 Data Write Timing Cycle – The write cycle like the read cycle begins with the assertion of the ALE signal which latches the address onto the low address bus as shown in Figure 2-16 This address selects which control register the write address decoders enables During T6, the CPU emits the data out of port 0 The write control signal (WR L) is asserted at T7 This signal enables the data buffer for data transfer and allows address decoders to toggle low the selected output line When this happens, the data on the data bus is transferred through the enabled control register and out to the appropriate device The cycle ends when write control signal is unasserted Figure 2-16 shows the data write cycle timing

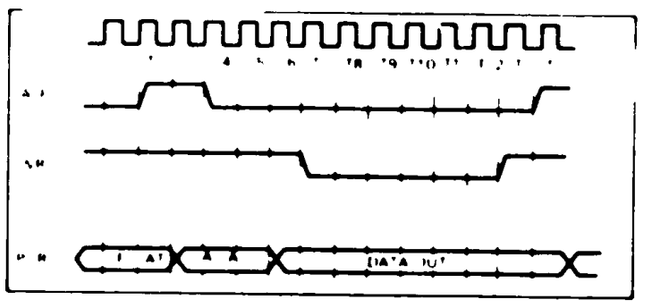

Figure 2-16 Data Write Cycle Timing

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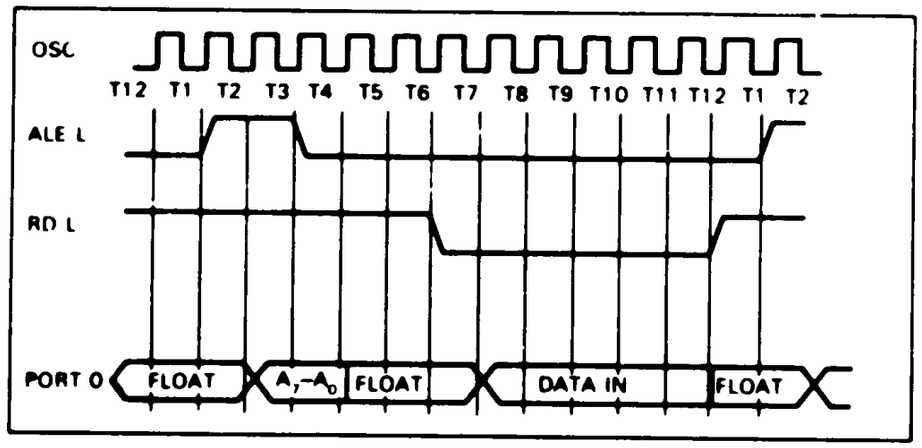

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Figure 2-15 Data Read Cycle Timing

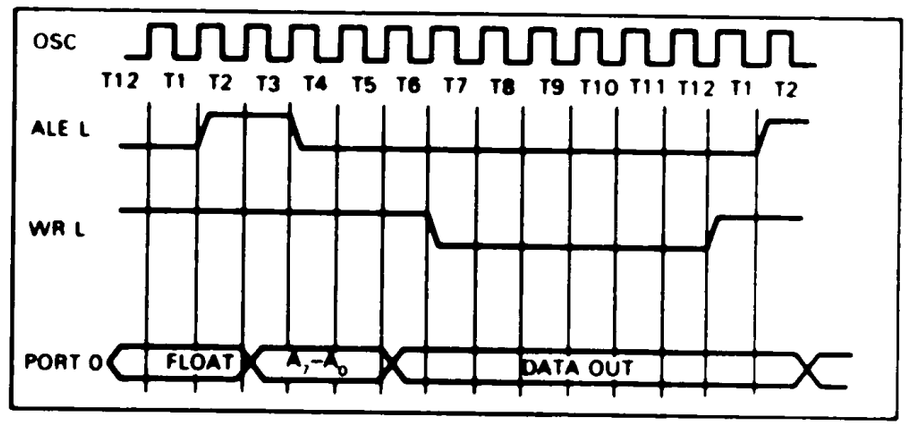

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Figure 2-16 Data Write Cycle Timing

CHAPTER 3

CHAPTER 3
CONNECTOR BOARD

3.1 INTRODUCTION

The connector board contains eight 25-pin D connectors, two 50-pin connectors, and four red light emitting diodes (LEDs) It is on the rear of the Mini-Exchange with eight D connectors and four LEDs facing out Figure 3-1 shows the component side of the connector board

3.2 FUNCTIONAL OVERVIEW

The eight 25-pin D connectors (EIA RS-232) are the communication ports of the Mini-Exchange The ports labeled 1 through 8 are for connecting the computer terminals and similar devices to the Mini-Exchange

The two 50-pin connectors are male connectors and they slide down into the female connectors on the logic board The two 50-pin connectors connect the connector board with the logic board

The four red LEDs display the operational status of the Mini-Exchange When the loopback test plug is inserted in one of the communication ports, the LEDs flash the corresponding port number from 1 through 4

3.2.1 Interface

This section describes the signals that are transmitted and received by the Mini-Exchange

The communication ports are connected to terminals and similar devices by a RS-423/RS-232-like interface The Mini-Exchange operates its communication ports using EIA voltage standards It converts these standard voltages to TTL voltage levels through the drivers and receivers on the logic board

Ports 1 through 8 can connect to either a terminal or a printer To connect a modem to the Mini-Exchange, you must connect it to port 8 Ports 1 through 7 do not have the capability to support a modem

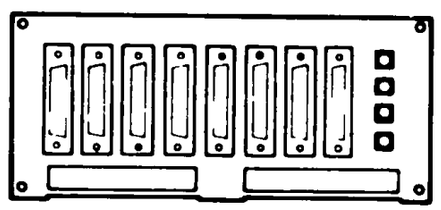

Figure 3-1 Component Side of the Connector Board

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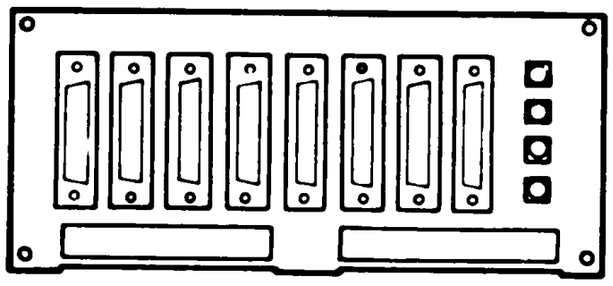

Figure 3-1 Component Side of the Connector Board

3.2.1.1 **Communication Port Pinning** – This section describes the signals on each pin used on port 8. Each of the eight ports have the same connector pinning, except that port 8 has four more signals for modem support. These are pins 11, 18, 19, and 21. For this reason only port 8 can support a modem.

Table 3-1 lists the signals on the connector pins of the communication ports.

Table 3-2 lists the signals and pin-out for a modem cable. This cable is used when connecting port 8 to modem.

Table 3-1 J8, Communication Port Pin-Out

Pin	Signal	CCITT V.24	EIA RS-232-C
1	Protective Ground	101	AA
2	Transmitted Data	104	BB
3	Received Data	103	BA
4			
5	Clear to Send	106	CB
6	Data Set Ready	107	CC
7	Signal Ground	102	AB
8	Carrier Detect	109	CF
9*	Test 0	-	-
10*	Test 1	-	-
11†	Modem	-	-
12			
13*	Test 2	-	-
14			
15			
16*	PTest X		
17			
18†	Modem Carrier Detect		
19†	Modem Ring Indicator	-	-
20	Data Terminal Ready	108/2	CD
21†	Remote Loopback		
22	Ring Indicator	125	CE
23			
24			
25			

NOTE

Pins 9, 10, 11, 13, 16, 18, and 19 are nonstandard RS-423 and RS-232 connections. Maximum voltages on pins 11 and 16 must not exceed the range of ground and +5 V.

* These pins are used only for the external loopback test. No external devices other than the loopback test plug can use these pins.

† Signals on these pins are present only on connector number 8. These pins are used only when a DF03 Modem and should not be used by other devices. The "Remote Loopback" signal is always in the unasserted state.

Table 3-2 DF03 Modem Cable Pin Out

Mini-Exchange Signal Name	Pin Number	DF03 Modem Signal Name	Pin Number
PROT GND	1	PROT GND	1
TXD	2	RXD	3
RXD	3	TXD	2
DSR	6	DTR	20
SIG GND	7	SIG GND	7
MODEM L	11	SIG GND	7
MCD	18	CD	8
MRI	19	RI	22
DTR	20	DSR	6
120 V	21	Loop Test	18,21
CD	8	DSRS	23

3.2.1.2 **Signal Definitions** – Some signal definitions may seem vague. For your convenience, there is a definition of each modem control signal in Appendix B, as well as the direction of the signal.

3.2.2 LED Display

There are five LEDs on the Mini-Exchange, one power on LED and four diagnostic LEDs.

3.2.2.1 **Power On LED** – The green power on LED is on the front of the box, and turns on when the Mini-Exchange is plugged in. This indicates the +5, +12, and -12 V source from the power supply is on.

3.2.2.2 **Diagnostic LEDs** – The four red LEDs indicate errors found during power-up self-test or errors found during the loopback tests. At power up, all four red LEDs turn on then turn off if no errors are found. If the LEDs stay on, there is an error in the Mini-Exchange. The decoded indicator error codes are in Table 3-3.

The LED display register turns these LEDs on or off according to data from the CPU. The LEDs light when the LED H signal toggles low. Figure 3-2 is a block diagram of the diagnostic LEDs. Table 3-3 decodes the red LEDs.

Table 3-3 LED Error Codes

LED 4	LED 3	LED 2	LED 1	Error Condition
Off	Off	Off	Off	None - no self test errors
Off	Off	Off	On	Port 1 error detected
Off	Off	On	Off	Port 2 error detected
Off	Off	On	On	Port 3 error detected
Off	On	Off	Off	Port 4 error detected
Off	On	Off	On	Port 5 error detected
Off	On	On	Off	Port 6 error detected
Off	On	On	On	Port 7 error detected
On	Off	Off	Off	Port 8 error detected
On	Off	Off	On	System module failed
On	Off	On	Off	System module failed
On	Off	On	On	System module failed
On	On	Off	Off	System module failed
On	On	Off	On	System module failed
On	On	On	Off	System module failed
On	On	On	On	System module failed*

NOTE

All the LEDs are lit at power up (lamp test). If they all stay lit, a system module error is being indicated.

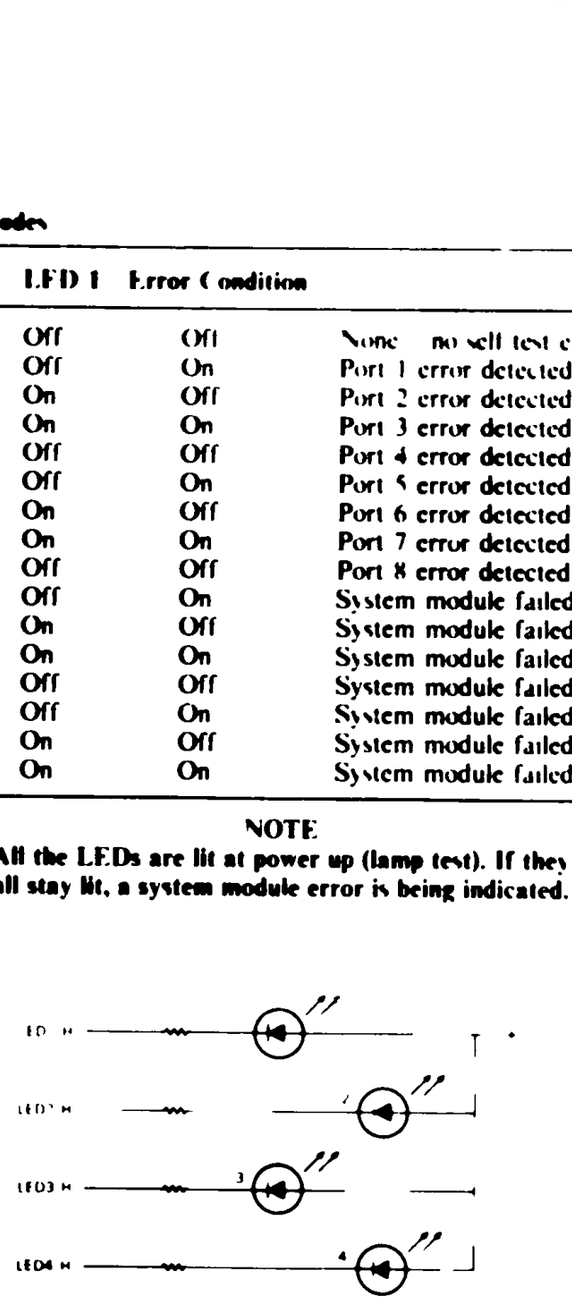

Figure 3 2 Diagnostic LEDs Block Diagram

3.2.3 Connectors

Connectors J9 and J10 are two 50-pin connectors. They connect the connector board with the logic board. Figure 3-3 shows the two 50-pin connector pin-outs.

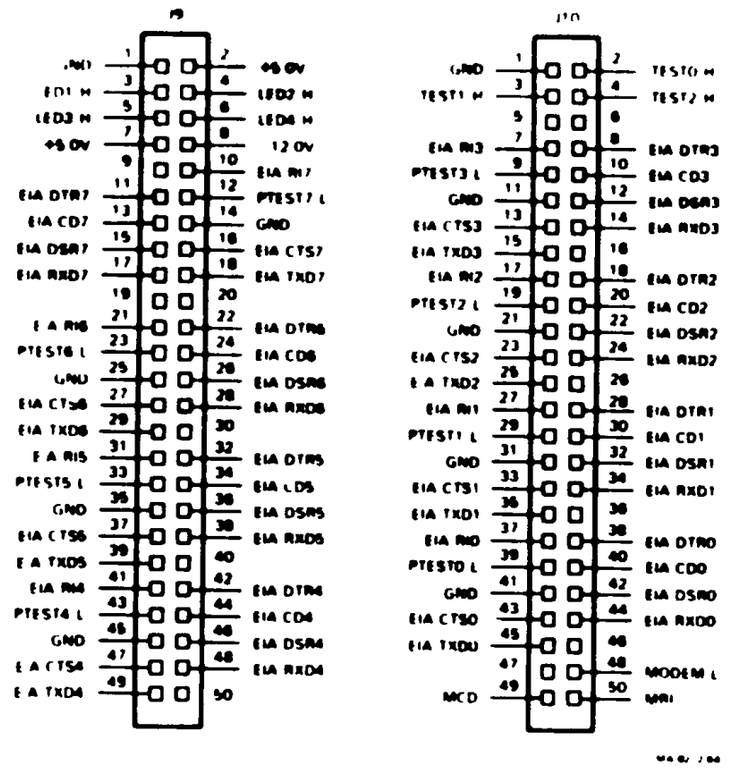

Figure 3-3 J9 and J10 Pin-Out

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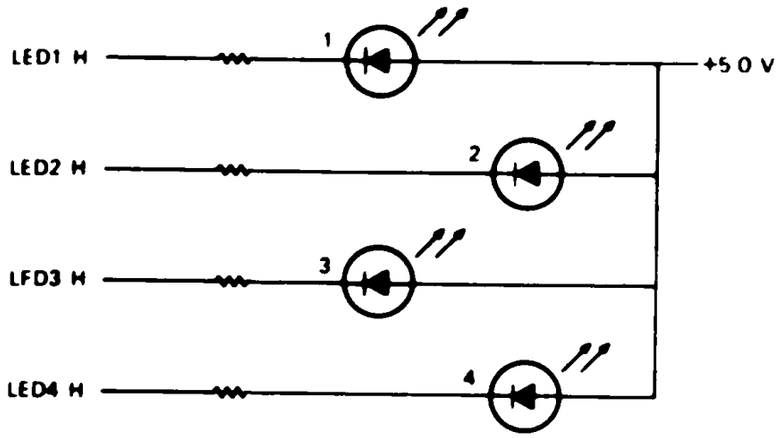

Figure 3-2 Diagnostic LEDs Block Diagram

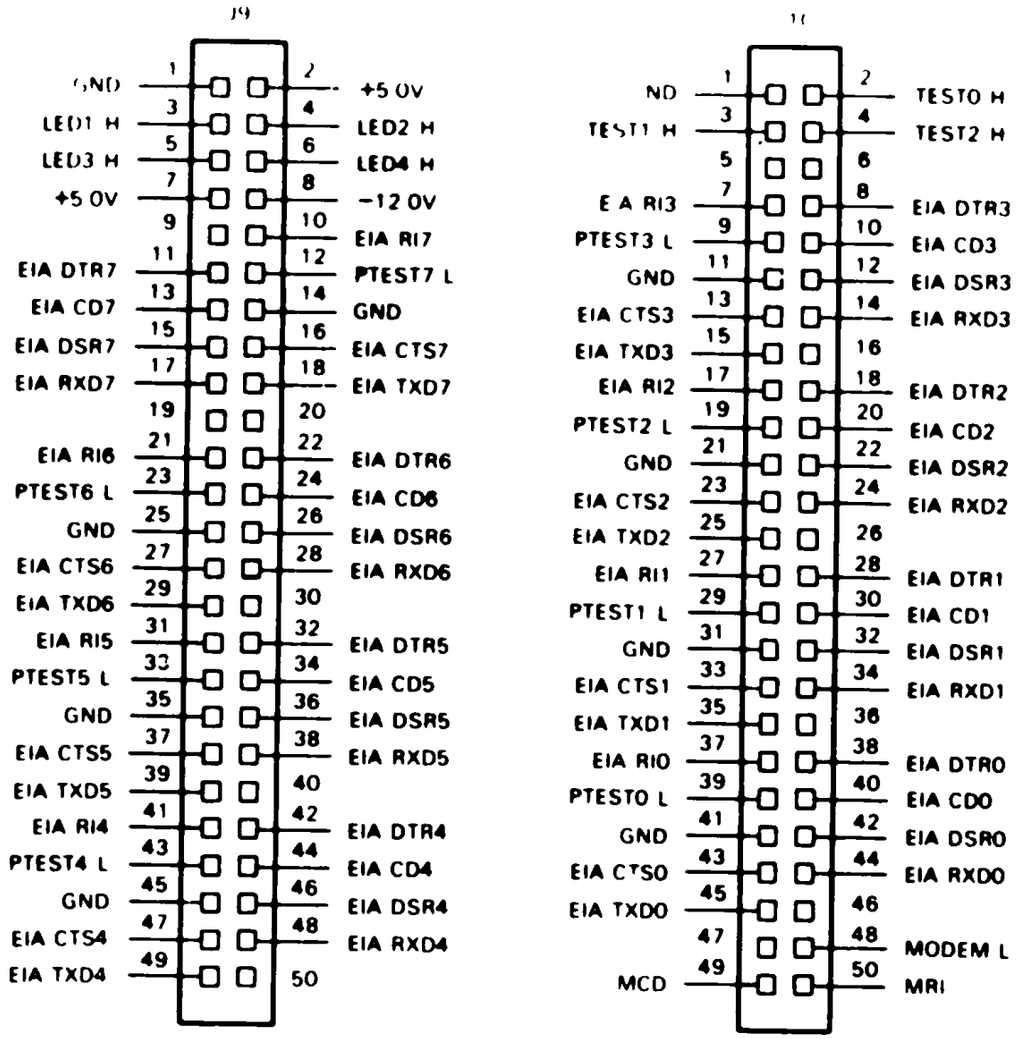

Figure 3-3 J9 and J10 Pin-Out

CHAPTER 4

CHAPTER 4
POWER SUPPLY BOARD

4.1 INTRODUCTION

The switching power supply converts ac line voltage to dc according to Mini-Exchange specifications The user sets the voltage selection slide switch on the rear panel for proper ac input Table 4-1 shows the two possible combinations of settings for this switch and the actual ac input Figure 4-1 shows the component side of the power supply board

Table 4-1 AC Voltage Switch Settings

Switch Setting	Voltage	Operation
120	120	OK
240	240	OK
120	240	External fuse blows Internal fuse and transistor Q1 may be damaged
240	120	No damage Green LED on front panel may be lit

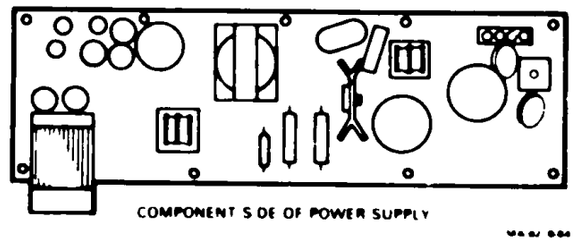

Figure 4 1 Component Side of Power Supply Board

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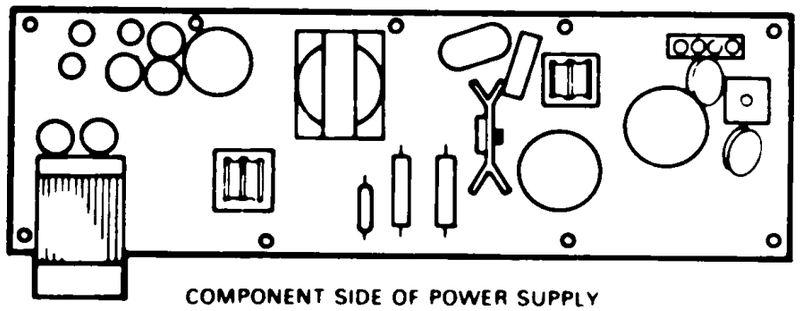

COMPONENT SIDE OF POWER SUPPLY

MA 07 0R4

Figure 4-1 Component Side of Po..

4.2 FUNCTIONAL DESCRIPTION

The power supply is an off-line, switch-mode type ac/dc voltage converter circuit It operates at a constant frequency (30 kHz) using pulse width modulator techniques to regulate the output voltages Input voltage can be either 120 or 240 Vac supplied from a single-phase/three wire distribution system The voltage select switch and system fuse are accessible on the rear of the Mini-Exchange system box Maximum input power required is 33 watts

The power supply board contains the line rectifiers, the power switching transistor, switching transformer, control circuits, and output filters They convert ac line voltage to regulated dc voltage The user sets the voltage selection slide switch on the rear panel and plugs the ac power cable into the Mini-Exchange and the ac source

4.2.1 Power Conversion

The ac line voltage is first filtered and then rectified to produce a dc voltage The dc is then switched by a switching transistor (in the base drive) that presents high voltage dc pulses to the power switching transformer primary The transformer's output – dc pulses are rectified and filtered again to produce smooth dc

WARNING

The input capacitors hold high voltages for up to 30 seconds after system power is turned off (unplugged).

4.2.2 Control Circuits

The error amp and comparator circuits control the switch pulse duration They switch off the transformer to decrease the output voltages Transistors in the base drive circuit switch the transformer back on again when the comparator removes its switch off signal

4.2.3 Protection

Protection circuits prevent damage from incorrect voltages There is the external fuse, internal fuse, short circuit, and overcurrent protection The fuses protect the input and switching circuitry The short-circuit protection circuit is used if one of the three output supplies is shorted to ground or to one another The overcurrent protection does what its name implies

4.3 DETAILED DESCRIPTION

4.3.1 Power Conversion

Incoming ac first passes through a line filter This prevents power supply and/or computer-generated noise pulses from feeding back into the ac lines A full-wave bridge rectifier then converts the ac to pulsing dc If the ac line voltage is 120 Vac, then the full-wave bridge serves also as a voltage doubler and rectifier This provides 250 350 Vdc to the two input capacitors The capacitors store the energy for the switching cycles

The regulation circuits make the base drive switching transistor pulse on and off This places a voltage across the primary winding of the power switching transformer turning it on and off The pulse has a frequency that stays constant at 30 kHz However, the pulse width changes to control the amount of power the transformer couples to the power supply outputs

There are three secondaries to the transformer, one for each of the output supply voltages Each output is rectified and passes through a rectifier diode and an LC filter to smooth the pulses and steady the dc outputs Figure 4-2 is a block diagram of the power supply board

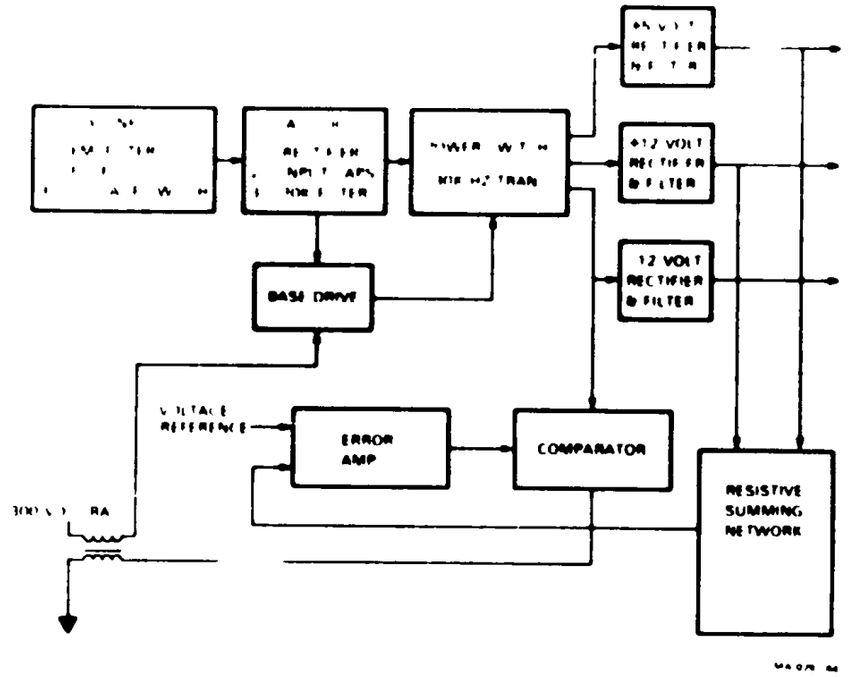

Figure 4-2 Power Supply Block Diagram

4.3.2 Control Circuits

The control circuits are the error amplifier, resistive summing network, and comparator The +5 and +12 Vdc voltages are compared by the resistive summing network that provides a constant input to the error amp The error amp then sends the difference of this voltage and a reference voltage to the comparator which provides a pulsing signal to the base drive transformer

The comparator determines the correct pulse width by comparing the output from the error amp to the 12 output voltage When current demand is high, voltage drops The comparator senses the voltage drop and increases the pulse width This permits additional energy transfer during this extended switch pulse

When the switching transformer is turned off, the 12 output voltage drops and turns the comparator transistor off This cuts off the base drive transformer which allows the switching transistor to turn on again charging the switching transformer Table 4-2 shows the pinning for J2, the dc voltage cable connector

Table 4-2 DC Voltage Connector, J2

Pin	Voltage/Signal
1	+5 Vdc
2	+5 Vdc
3, 4, 5, 7	Ground
6	+12 Vdc
8	12 Vdc

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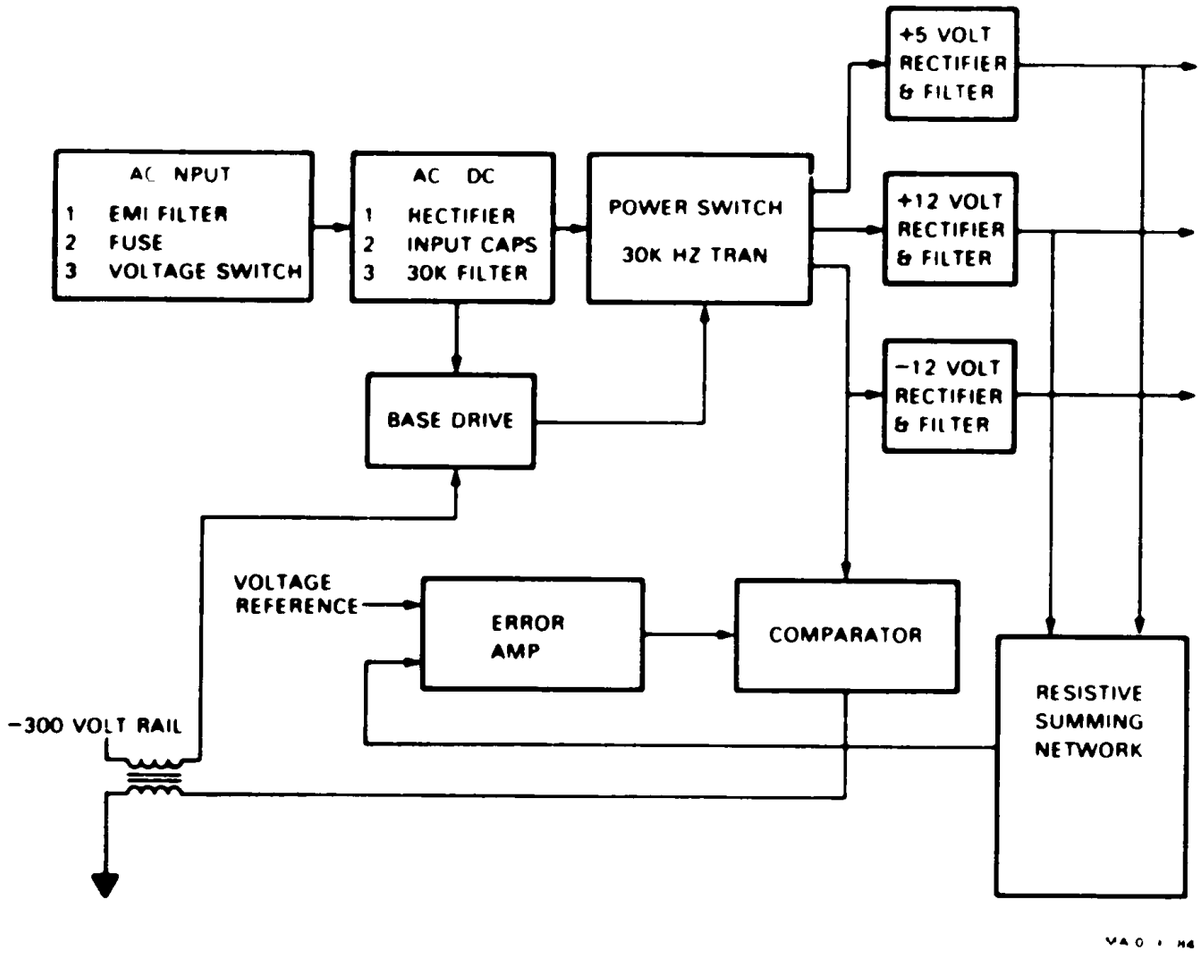


Figure 4-2 Power Supply Block Diagram

4.3.3 Overcurrent Protection

This circuit senses the peak current in the switching transformer primary. It automatically shuts the base drive switching transistor off when the primary current rises above the threshold value. In addition to this circuit is a separate protection circuit on the +5 Vdc output supply. It shuts off the switching transistor by driving the comparator on. Both of these circuits reset when the current reaches a safe operating limit. Table 4-3 shows the maximum and the nominal currents for the three voltage supplies.

Table 4-3 Current Protection Thresholds

Output	Overcurrent	Nominal
+5	6.5 A max	600 1200 mA
+12	5.0 A max	200 360 mA
-12	5.0 A max	200 360 mA

CHAPTER 5

CHAPTER 5
FIRMWARE DESCRIPTION

5.1 INTRODUCTION

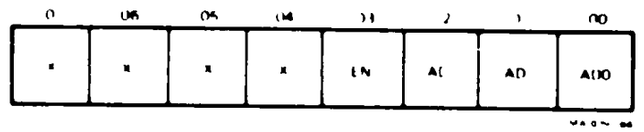
This chapter describes the bit definitions for each control register. These control registers are written to or read by the CPU from port 0 through the data bus.

5.2 WRITE CONTROL REGISTERS

This section describes the control registers that hold status information from the data bus.

5.2.1 UART Multiplexer Control Register

Address 000010 UART multiplexer control register (write only)



Bits 07 04 Not used

Bit 03 Enable bit, used to enable multiplexer output

1 - Enable output of the multiplexer to the UART

0 Disables output of the multiplexer

Bits 02 00 Address of which port's received data is to be transmitted to the UART's input

AD2	AD1	AD0	Port Address
0	0	0	Port 1 RXD0
0	0	1	Port 2 RXD1
0	1	0	Port 3 RXD2
0	1	1	Port 4 RXD3
1	0	0	Port 5 RXD4
1	0	1	Port 6 RXD5
1	1	0	Port 7 RXD6
1	1	1	Port 8 RXD7

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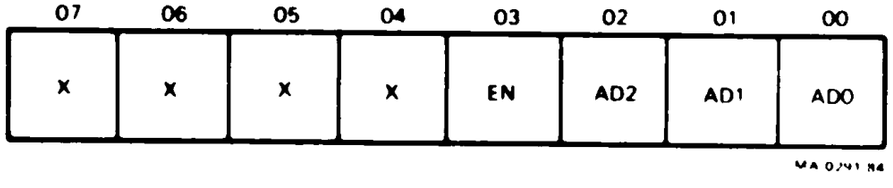

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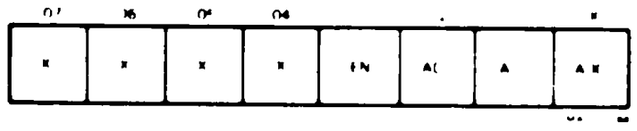
5.2.2 Port Multiplexer Control Registers

Address		
	000000	Port 1 multiplexer register (write only)
	000001	Port 2 multiplexer register (write only)
	000002	Port 3 multiplexer register (write only)
	000003	Port 4 multiplexer register (write only)
	000004	Port 5 multiplexer register (write only)
	000005	Port 6 multiplexer register (write only)
	000006	Port 7 multiplexer register (write only)
	000007	Port 8 multiplexer register (write only)



Bits 07 - 04 — Not used

Bit 03 — Enable bit, used to enable multiplexers output.

1 Enable output of multiplexer to the drivers

0 Places the driver output in the OFF condition

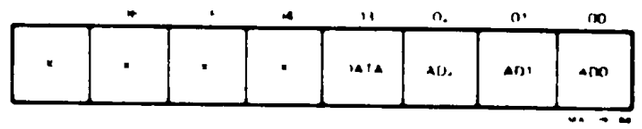
Bits 02 - 00 — Address of which port's received data is to be transmitted out on the channel. Instead a channel selecting its own received data, it is connected to the UART

AD0	AD1	AD2	Data Received On
0	0	0	Port 1
0	0	1	Port 2
0	1	0	Port 3
0	1	1	Port 4
1	0	0	Port 5
1	0	1	Port 6
1	1	0	Port 7
1	1	1	Port 8

5.2.3 DSR Control Register

Address 000011 — DSR (data set ready) control register

This register controls the DSR modem control lines. At power-up the DSR output is in the off state.



Bits 07 - 04 — Not used

Bit 03 — The value of this bit is used to control the selected port's DSR bit

1 Places the DSR output in the on state

0 Places the DSR output in the off state

Bits 02 - 00 — These bits select which port's DSR changes

AD2	AD1	AD0	Port Address
0	0	0	Port 1
0	0	1	Port 2
0	1	0	Port 3
0	1	1	Port 4
1	0	0	Port 5
1	0	1	Port 6
1	1	0	Port 7
1	1	1	Port 8*

* When port 8 is connected to the DF03 modem, this port's DSR line functions as the DTR line

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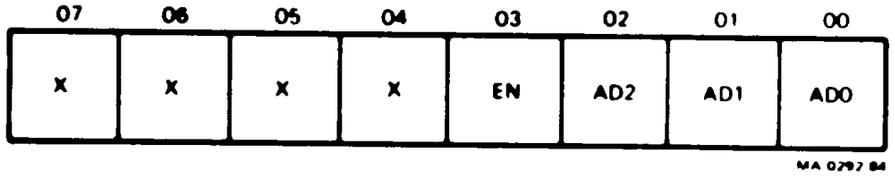
07
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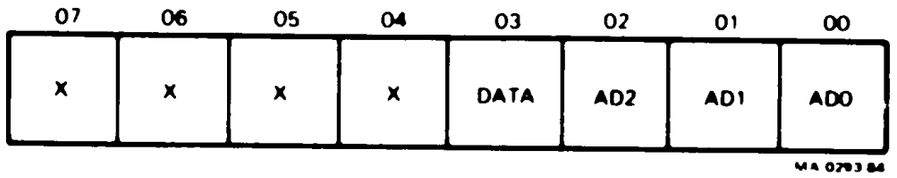
X
X
X
EN
AD2
AD1
AD0
MA 0797 84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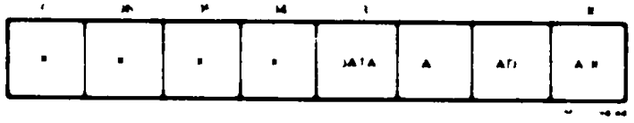
X
X
X
X
DATA
AD2
AD1
AD0
MA 0793 84

5.2.4 RI Control Register

Address 000012 RI (ring indicator) control register

This register controls the RI modem control lines. At power-up the RI outputs are in the off state.



Bits 07 - 04 Not used

Bit 03 The value of this bit controls the selected port's RI bit.

1 - Places the RI output in the on state.

0 - Places the RI output in the off state.

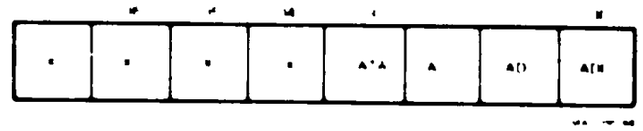
Bits 02 - 00 These bits select which port's RI changes.

AD2	AD1	AD0	Port Address
0	0	0	Port 1
0	0	1	Port 2
0	1	0	Port 3
0	1	1	Port 4
1	0	0	Port 5
1	0	1	Port 6
1	1	0	Port 7
1	1	1	Port 8

5.2.5 CD/CTS Control Register

Address 000013 CD (Carrier Detect)/CTS (Clear To Send) control register

This register controls the CD and CTS modem control lines. At power-up the CD and CTS outputs are in the off state.



Bits 07 - 04 Not used

Bit 03 The value of this bit controls the selected port's CD and CTS bit.

1 - Places the CD and CTS output in the on state.

0 - Places the CD and CTS output in the off state.

Bits 02 - 00 These bits select which port's CD and CTS changes.

AD2	AD1	AD0	Port Address
0	0	0	Port 1
0	0	1	Port 2
0	1	0	Port 3
0	1	1	Port 4
1	0	0	Port 5
1	0	1	Port 6
1	1	0	Port 7
1	1	1	Port 8*

* When the modem cable is attached to port 8, the CD signal acts as the "Data Signal Rate Selector" signal for the DF03 modem.

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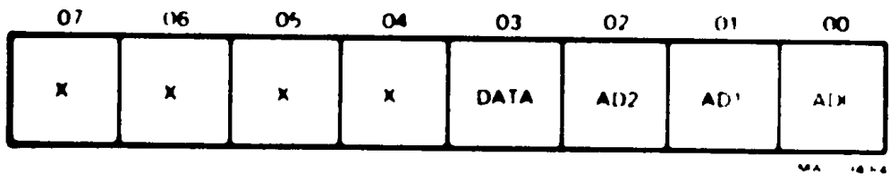
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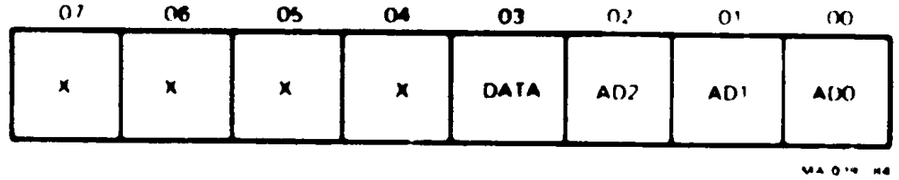
DATA
AD2
AD1
AD0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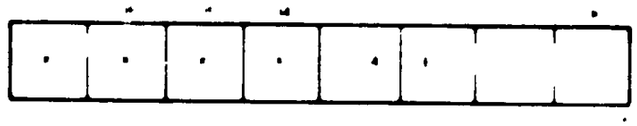
DATA
AD2
AD1
AD0

5.2.6 LED Display Register

Address 000016 LED Display Register

This register controls the state of the four red diagnostic LEDs on the Mini-Exchange. The LED display register uses only the low byte. This is a write only register.



Bits 07 04 Not used

Bits 03 00 LED4 LED1. These bits control the state of the four red LEDs on the rear of the Mini-Exchange. Setting one of these bits causes the corresponding LED to be turned off. Clearing a bit causes the corresponding LED to light. All four bits clear (light) momentarily at power-up.

5.3 READ CONTROL REGISTERS

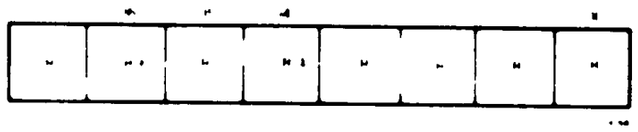
This section describes the registers that hold status information from a device connected at the rear of the Mini-Exchange.

5.3.1 DTR Control Register

Address 000020 DTR (data terminal ready) control register

This register indicates the present status of the DTR modem control lines.

1 On state of the DTR line
0 Off state of the DTR line



Bit 07 Present state of DTR for port 8 *

Bit 06 Present state of DTR for port 7

Bit 05 Present state of DTR for port 6

Bit 04 Present state of DTR for port 5

Bit 03 Present state of DTR for port 4

Bit 02 Present state of DTR for port 3

Bit 01 Present state of DTR for port 2

Bit 00 Present state of DTR for port 1

* When port 8 is connected to the DB-03 modem, the port's DTR line functions as the DSR line.

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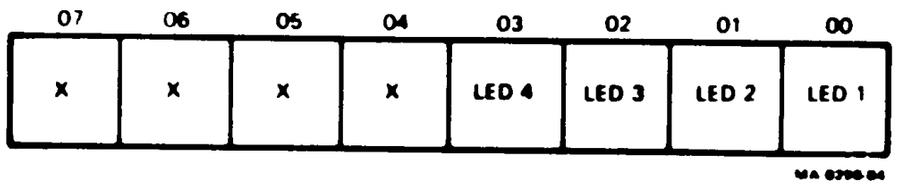
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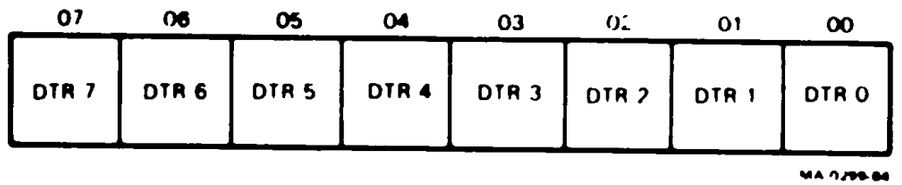
LED 4
LED 3
LED 2
LED 1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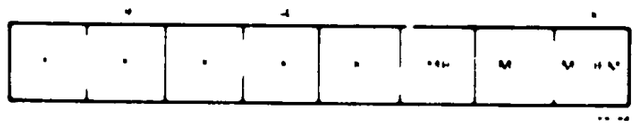
DTR 7
DTR 6
DTR 5
DTR 4
DTR 3
DTR 2
DTR 1
DTR 0

5.3.2 DF03 Modem Control Register

Address (000023) DF03 modem control register

This register indicates the present status of the modem control lines used with a DF03 modem



Bits 07 04 Not used

Bit 02 The value of this bit indicates the state of the ring indicator (RI) from the DF03 Modem

1 On state of the MRI normally indicates a ringing signal from the DF03 modem is being received

0 Off state of the MRI line indicates that no ringing signal from the DF03 modem is being received

Bit 01 The value of this bit indicates the state of the carrier detect from the DF03 modem

1 - On condition of the MCD line indicates that the DF03 is receiving the data carrier

0 Off condition of the MCD line indicates that no data carrier is being received

Bit 00 This bit indicates the presence of the DF03 modem and cable

1 - DF03 modem cable is not present

0 DF03 modem cable is present

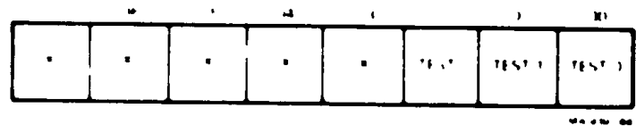
5.3.3 Modem Control Test Register

Address (000021) Modem control test register

During external loopback test, this register tests the modem control lines CD, CTS, and RI

1 Modem control is in the on state

0 Modem is in the off state



Bits 07 03 Not used

Bit 02 Loopback for carrier detect (CD)

Bit 01 Loopback for clear to send (CTS)

Bit 00 Loopback for ring indicator (RI)

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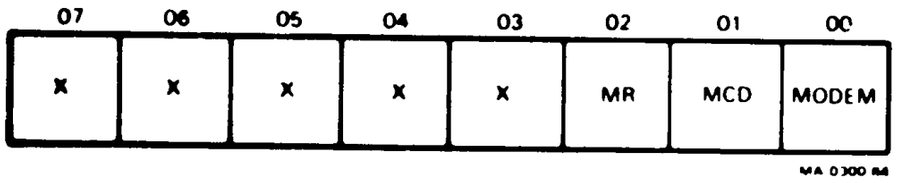
FRAME(S).


07
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02
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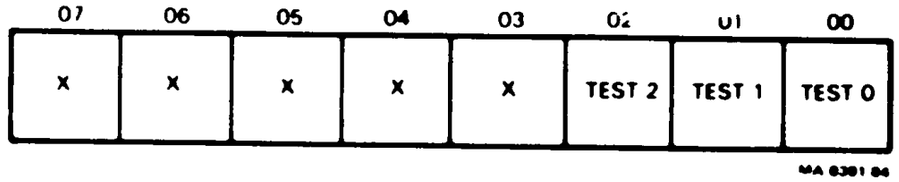
X
X
X
X
X
MR
MCD
MODEM
MA 0300 84


07
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05
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01
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X
X
X
X
TEST 2
TEST 1
TEST 0
MA 0301 84

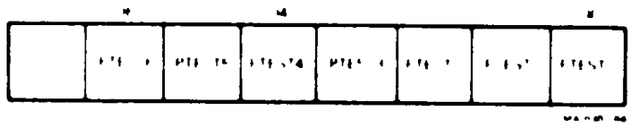
5.3.4 Port Test Register

Address 000022 Port Test Register

This register indicates the presence of the test plug. The bits of the register indicate which port has the test plug.

1 Test plug inserted

0 Test plug not inserted



Bit 07 Test plug indicator for port 8

Bit 06 Test plug indicator for port 7

Bit 05 Test plug indicator for port 6

Bit 04 Test plug indicator for port 5

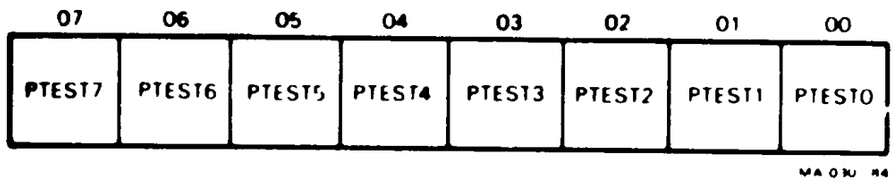
Bit 03 Test plug indicator for port 4

Bit 02 Test plug indicator for port 3

Bit 01 Test plug indicator for port 2

Bit 00 Test plug indicator for port 1

FOR ENLARGED ART
PLEASE SEE FOLLOWING
FRAME(S).


07
06
05
04
03
02
01
00
PTEST7
PTEST6
PTEST5
PTEST4
PTEST3
PTEST2
PTEST1
PTEST0

APPENDIX A

APPENDIX A
DIAGNOSTIC TESTS

A.1 INTRODUCTION

This appendix briefly explains the testing modes of the Mini-Exchange. The diagnostic tests for the Mini Exchange system unit are described, as well as a section on solving potential software problems.

A.2 DIAGNOSTIC TESTS

Two diagnostic programs test the Mini Exchange system unit itself: Mini-Exchange self-test and loopback connector test.

A.2.1 Mini-Exchange Self-Test

The Mini-Exchange switch has a system self-test that runs automatically each time the power is turned on. After you plug the power cord into a wall outlet, the green light on the front of the system unit lights. The system then begins a complete self-test and quickly flashes all diagnostic lights on the rear panel once and then stays off. If the green light on the front of the Mini-Exchange system unit does not turn on, there may be a problem with power. Check the power cord and voltage selection switch. Check the fuse, if the wire is broken, replace the fuse. If the light still does not turn on, the Mini-Exchange system unit must be serviced.

NOTE

If you run the test more than once, wait five or more seconds between turning power off and then on.

A.2.2 Loopback Connector Test

Plug the power cord into the wall outlet. Make sure the green indicator light is on. Do not disconnect the power cable during the loopback connector test. Test one connector at a time. Replace the cable prior to testing the next connector or tag the cables during this test with the port number of each connector so that you can put them back properly. It may be easier to disconnect all cables from the eight connectors but it's not necessary. Insert the loopback connector into the suspected bad port.

When you insert the loopback connector, the system tests the connector associated with that port and flashes the diagnostic lights on the rear panel slowly, in a light code pattern for that particular port. Table A-1 interprets the on/off combinations that form a light code. If the lights do not flash the proper code, that individual port is bad and cannot be used. When you remove the loopback connector, the lights turn off. If any or all lights stay on, the connector is bad and cannot be used.

The loopback test plug creates an external loopback of data and modem control lines. Table A-2 shows the signals the test plug shorts back into the same port.

Table A-1 Light Codes

Diagnostic Lights				Meaning
4	3	2	1	
○	○	○	○	System is working
○	○	○	●	Connector 1
○	○	●	○	Connector 2
○	○	●	●	Connector 3
○	●	○	○	Connector 4
○	●	○	●	Connector 5
○	●	●	○	Connector 6
○	●	●	●	Connector 7
●	○	○	○	Connector 8
●	●	●	●	System is not working

○ means the light is off ● means the light is on

Table A-2 Signals

Transmitter	Receiver	Pin	Pin
TXD	RXD	3	2
DSR	DTR	6	20
CD	Test0, MCD	8	9, 18
CTS	Test1	5	10
RI	Test2, MRI	22	13, 19
SIG GND	PtestX, Modem	7	16, 11

The CPU uses PTESTX signal to determine which port has the test plug inserted This signal sets a bit in the port test register The CPU then tests the data paths and modem control lines shown in Table A-2 If the received data is the same as the transmitted data, the CPU flashes the LEDs shown in Table A-1 to indicate that the port is operational If the LEDs do anything different, that port cannot be used

Table A-2 shows the configuration of the loopback test plug

A.3 SOFTWARE

Devices that connect to the Mini-Exchange system can use applications software, printers do not need software for connections. You may want to reload your software before testing again

If you are using software application packages for your connections, be sure your Software Product Description (SPD) specifies that it can be used with the Mini-Exchange system.

Refer to the *Mini-Exchange Installation/Owner's Manual* for more information on software applications

APPENDIX B

APPENDIX B
SIGNAL DEFINITIONS

Carrier Detect (CD)
Direction From Mini-Exchange
The on condition indicates the presence of a through connection in the Mini Exchange The calling device and the called device are connected The Mini-Exchange will hold this line in the on condition until the communication is broken See Data Signal Rate Selector signal definition for other functions of this signal

Clear to Send (CTS)
Direction From Mini Exchange
The on condition indicates presence of a through connection in the Mini-Exchange The calling device and the called device are connected The Mini-Exchange holds this line in the on condition until the communication is broken

Data Set Ready (DSR)
Direction From Mini-Exchange
Signals on this circuit indicate whether the Mini-Exchange is ready to operate The on condition indicates that the Mini-Exchange is ready to exchange further control signals and data with the calling device The off condition indicates that the Mini-Exchange is not ready to operate

Data Signal Rate Selector (DSRS)
Direction To Modem
When a modem cable is attached to port eight, the port's Carrier Detect signal acts as the DSRS signal This interface signal allows the Mini-Exchange to select high or low speed operation on the modem The on or asserted state of the DSRS selects the "high speed mode" at the modem The off or unasserted condition selects the "low speed mode" of the modem At power-up this signal defaults to the off state

Data Terminal Ready (DTR)
Direction To Mini-Exchange
The on condition of this signal indicates that a device is responding to or calling the Mini-Exchange The off condition indicates that a disconnect is being processed When this signal is off the Mini-Exchange stops all through communication

Modem
Direction From DF03 Mode Cable
This signal is on port eight only The signal should only be driven by the DF03 modem cable Voltages on this line must not exceed the range of ground and +5 Vdc The on or +5 Vdc condition indicates that no modem cable is present This line defaults to this value The off or 0 Vdc (pin grounded) indicates that the modem cable is present The DF03 modem cable grounds this signal

Modem Carrier Detect (MCD)
Direction From DF03
This signal is received on port eight only The signal is used only when the DF03 modem is connected to the Mini Exchange This signal indicates the status of the modem's Carrier Detect Signal The on or asserted condition of the MCD indicates that the DF03 is receiving the data carrier The off or unasserted condition of the MCD line indicates that no data carrier is being received

Modem Ring Indicator (MRI)
Direction From DF03
This signal is received on port eight only The signal is used only when the DF03 modem is connected to the Mini Exchange This signal indicates the status of the modem's ring indicator The on or asserted state of the MRI indicates that a ringing signal from the DF03 modem is being received The off or unasserted state of the MRI line indicates that no ringing signal from the DF03 modem is being received

Port Test X (PTESTX)
Direction From Test Plug
This signal identifies when the test plug is inserted The signal also indicates which port has the test plug This signal is a nonstandard RS-232, RS-423 connection and is used only with the test plug

Protective GND (PROT GND)
The protective ground is connected to the Mini-Exchange chassis It is also connected to the shielding conductors in the interface cable

Received Data (RXD)
Direction From Mini-Exchange
Signals in this circuit represent serially encoded characters generated by the user's equipment This line is connected to the received data output of the user's equipment

Ring Indicator (RI)
Direction From Mini-Exchange
The on condition indicates the start of a calling sequence to the DTE The off condition indicates that no calling sequence to the DTE has started

Signal Ground (SIG GND)
This circuit establishes the common ground reference potential for all interface circuits

Test0
Direction From Test Plug
When the test plug is inserted, this signal is the port's CD (carrier detect) signal This is a nonstandard RS-232, RS-423 connection and is used only with the test plug

Test1
Direction From Test Plug
When the test plug is inserted, this signal is the port's CTS (clear to send) signal This is a nonstandard RS-232 RS-423 connection and is used only with the test plug

Test2
Direction From Test Plug
When the test plug is inserted, this signal is the port's RI (ring indicator) signal This is a nonstandard RS-232,RS-423 connection and is used only with the test plug

Transmitted Data (TXD)
Direction To Mini-Exchange
Signals on this circuit represent serially encoded characters generated by the user's equipment This line is connected to the transmitted data output of the user's equipment