Perkin-Elmer Series 3200

MANAGEMENT SUMMARY

The Series 3200 is the first family of systems unveiled by Perkin-Elmer's Computer Systems Division, formerly Interdata, Incorporated, a unit of the Perkin-Elmer Corporation. Currently, the 3200 family consists of the 3220, unveiled in February, 1979, and the 3240, announced in September, 1979. The Series 3200 systems are user-level software compatible with the Interdata Model 7/32 and 8/32 systems.

Interdata introduced its first true 32-bit processor, the 8/32 Megamini, in March 1975. The 8/32, with 128K to one million bytes of directly addressable core memory, became the company's high-performance 32-bit entry in the high-end minicomputer marketplace. It did not, however, supersede the Interdata 7/32 (Report M11-683-101), an earlier machine with the external appearance of 32-bit architecture but a lower performance level, which has been retained by Perkin-Elmer as a low-price entry into the world of minicomputers. In the two years after the introduction of the 8/32 Megamini, Interdata enhanced the original processor with options for high-speed data handling, a high-performance (single and double precision) floating-point processor, and writable control store (WCS). These enhancements were accompanied by a name change, from the 8/32 Megamini to the 8/32C Megamini. Both the 7/32 and 8/32 Megamini are still being marketed by Perkin-Elmer.

The first two models of the Series 3200 introduced are the 3220 and 3240. Features of these models include:

- Directly addressable high-density MOS ECC memory using 16K RAM chips (256K to 4 million bytes of the 3220; 256K to 16 million bytes on the 3240 in four interleaved banks) in 256K-byte modules
- 128 32-bit registers in eight sets of 16 registers each
- Four levels of external interrupts

Perkin-Elmer's new "top-of-the-line" family of 32-bit minicomputers is the Series 3200, Models 3220 and 3240. Memory is MOS with error correcting code and is expandable from a basic 256K bytes to four million bytes on the 3220 and to sixteen million bytes on the 3240. Software is compatible with that of Perkin-Elmer's 16-bit and earlier 32-bit processors. A basic Model 3220 processor lists for $33,500, and a Model 3240 costs $85,000.

CHARACTERISTICS

MANUFACTURER: Perkin-Elmer Corporation, Computer Systems Division, 2 Crescent Place, Oceanport, New Jersey 07757. Telephone (201) 229-6800.

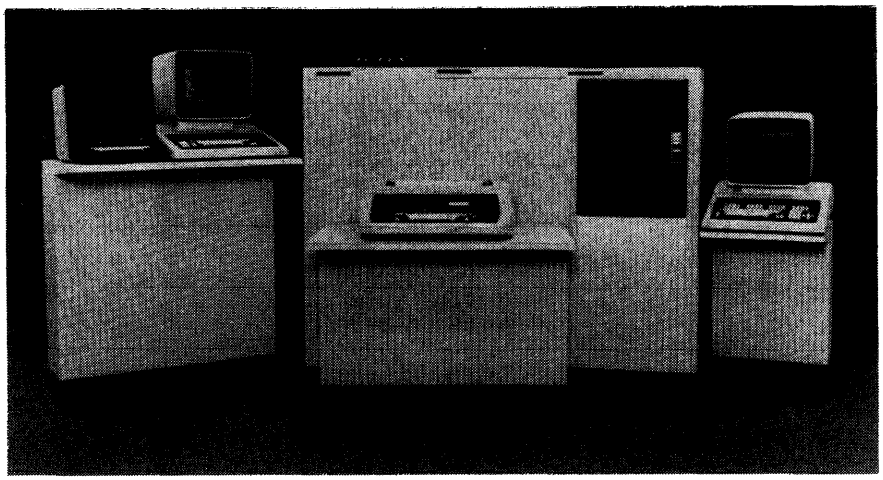
The Computer Systems Division of Perkin-Elmer was kwown as Interdata, Inc., before all data processing activities were unified under the name Perkin-Elmer. The Computer Systems Division, with 1,300 employees, specializes in minicomputer hardware, software, and systems for manufacturers and end-users in business/scientific computation, simulation, and all OEM markets. The company also supplies products for data communications, discrete manufacturing, industrial process control, and laboratory automation. The parent company, Perkin-Elmer, is an international corporation employing more than 12,000, with interests in instrumentation, optical and electro-optical systems, flame spray equipment, control systems, and navigational instructions, in addition to the Computer Systems Division's marketing areas.

MODELS: 3220 and 3240.

DATE ANNOUNCED: 3220, February 20, 1979; 3240, September 17, 1979.

DATE OF FIRST DELIVERY: 3220, April 1979; 3240, September 1979.

NUMBER INSTALLED TO DATE: Not available.



The first processor in Perkin-Elmer's 32-bit Series 3200 is the 3220, which can be configured with from 256K bytes to four megabytes of MOS ECC memory, eight sets of sixteen 32-bit registers, battery backup, and a 16-slot chassis. Available options include cache memory, Writable Control Store, and a floating-point processor.

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- 2K 32-bit words of fixed control store (ROM) to implement the standard instruction set
- An instruction set which includes a subset of commercial instructions and single/double precision instructions for mixed-mode floating-point operations
- Error correction on full 32-bit words
- Optional bipolar cache memory of 1K bytes on the 3220 and standard 8K bytes of the 3240
- Optional floating-point processor with 48 instructions
- Optional Writable Control Store of 2K words

To date, Perkin-Elmer has installed more than 2,500 32-bit systems throughout the world in the aerospace, simulation, scientific, and commercial fields. These are the application areas where these minicomputers' large-computer advantages become obvious. These advantages are: 1) large main storage, permitting large program and/or data areas, 2) system software that takes full advantage of the 32-bit architecture, large memory capacity, and direct addressability, 3) auto-driver channel input/output, 4) high-speed buffered selector channel I/O, and 5) high-performance features such as interleaved memory (on the 3240), multiple general register stacks, hardware floating-point arithmetic, hardware program relocation and protection. Schottky logic, writable control store, cache memory, and universal internal 32-bit data paths.

The optional Floating Point Processor includes 48 instructions, eight 32-bit single-protection registers, and eight 64-bit double-precision registers. A rounding algorithm called R-Star rounding, previously available only on mainframes according to Perkin-Elmer, provides more accurate results by equitably distributing and rounding results.

Other significant options are Writable Control Store (WCS) and the high-speed data handling feature. WCS allows sophisticated users to implement application-oriented macros, instructions, special mathematical or scientific algorithms, or FORTRAN or COBOL routines at the microcode level. The WCS option consists of 2K 32-bit words of high-speed RAM and four instructions: Read, Write, Branch, and Enter. Enter is the only nonprivileged instruction. It allows user-level programs to call routines implemented in WCS. A two-to-three-times speed advantage over conventional software can be obtained by the use of special algorithms or other functions implemented in WCS. A complete set of WCS development software is included with this option. Both the development and run-time systems operate under the OS/32 operating system.

The high-speed data handling option implements two instructions to make line handling easier for various data communications protocols. The Process Byte and Process Byte Register instructions are used to move and

DATA FORMATS

BASIC UNIT: 32-bit word.

FIXED-POINT OPERANDS: 16-bit halfwords, 32-bit fullwords, and 64-bit double words. In each format, the zero bit is the sign bit, and the remaining 15, 31, or 63 bits represent the magnitude. Positive values are represented in true binary form with a sign bit of zero; negative values are represented in two's complement form with a sign bit of one. Each group of four bits represents one hexadecimal digit.

FLOATING-POINT OPERANDS: 32-bit fullwords (single-precision operands) or 64-bit double words (double-precision operands). A floating-point number includes a single-bit sign (zero bit), a 7-bit exponent (bits 1-7) in excess-64 notation, and a fraction field consisting of six hexadecimal digits for single-precision operands or fourteen hexadecimal digits for double-precision operands.

LOGICAL OPERANDS: 8-bit bytes, 16-bit halfwords, and 32-bit fullwords. Logical operations can also be performed on single bits located in bit arrays.

INSTRUCTIONS: Instructions can be 16, 32, 48, 64, 80, or 96 bits in length, depending upon instruction type. There are eight instruction formats, seven of which have an eight-bit operation code and a four-bit general register operand indicator. The eighth format is essentially a pair of back-to-back instructions which can address two strings of data in memory and perform memory-to-memory operations.

The Register-to-Register (RR) type also has a second four-bit general register operand indicator. The Short Format (SF) type replaces the second register field with a four-bit data field. The Register-and-Immediate-Storage instructions expand the SF's data field to 16 (RI1) or 32 (RI2) bits and also pick up a four-bit register indicator as an index value.

There are three Register-and-Indexed-Storage instructions. The RX1 format consists of an eight-bit operation code, a four-bit general register first-operand indicator, a four-bit general register used as a second-operand index value, a two-bit code indicating RX1 format, and the 14-bit absolute address of the second operand, which is added to the index value to obtain the memory address of the second operand. The RX2 format differs in that the format indicator is a one-bit field, and a 15-bit relative address in the instruction is added to the index value *and* to the address of the next sequential instruction to obtain the address of the second operand. The RX3 format is similar to the RX1 except that RX3 allows two levels of indexing of the second operand.

The eighth format, Register and Indexed Storage/Register and Indexed Storage (RXRX), appears to be a pair of adjacent RX instructions but is actually only one instruction. Each member of the instruction pair may be any one of the three standard RX formats, and the two members do not have to be in the same RX format. The RXRX format therefore includes all options available to the RX1, RX2, and RX3 formats.

INTERNAL CODE: ASCII is standard. With the auto-driver channel (a standard feature), facilities are provided for automatic character translation and for the computation of cyclic redundancy checksums and longitudinal redundancy checksums for communication applications.

MAIN STORAGE

STORAGE TYPE: MOS.

CYCLE TIME: 500 nanoseconds.

CAPACITY: From 256K to 4 million bytes on the 3220 and from 256K to 16 million bytes on the 3240 in 256K-byte

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION & SPEED	MANUFACTURER
MAGNETIC TAPE EQUIPMENT		
M46-400	Intertape Cassette System; 500K bytes per cassette, 2 tracks, 800 bpi, PE, read-after-write, 10 ips, longitudinal redundancy read check, dual transports and interface, 1K to 480 bytes/second in read continuous mode with record size of 80 bytes	Perkin-Elmer Data Systems
M46-490, -492	9-track; 800 bpi, 75 ips, NRZI drive, 10.5-inch reels, dual gap recording, read-after-write; M46-490, -492 are master drives; M46-491, -493 are add-on drives; 60 KBS	Perkin-Elmer
M46-494, -496	9-track; 800/1600 bpi, 75 ips, NRZI/PE drive, 10.5-inch reels, dual gap recording, read-after-write; M46-494, -496 are master drives; M46-495, -497 are add-on drives; 60/120 KBS	Perkin-Elmer
M46-534, -535	Same as M46-490, -492 but includes 32-bit DMA; M46-491, -493 are add-on drives	Perkin-Elmer
M46-538, -539	Same as M46-494, -496 but includes 32-bit DMA; M46-495, -497 are add-on drives	Perkin-Elmer
M46-526, -527	9-track; 800 bpi, 45 ips, NRZI drive, 10.5-inch reels, dual gap recording, read-after-write, 32-bit DMA; M46-526, -527 are master drives; M46-501, -502 are add-on drives; 36KBS	Perkin-Elmer
M46-530, -531	9-track; 1600 bpi, 45 ips, PE drive, 10.5-inch reels, dual gap recording, read-after-write, 32-bit DMA; M46-530, -531 are master drives; M46-515, -516 are add-on drives; 72KBS	Perkin-Elmer
PRINTERS		
M46-221, -222	Serial printer; 132 positions, 64-character set, 10 characters per inch, 6 lines per inch, 4- to 14.8-inch paper, 5 x 7 dot matrix, 2-channel VFU; 120 cps	Centronics
M46-223, -224	Same as M46-221, -222 but 180 cps	Centronics
M46-300, -301, -302, -303	Line printer; drum, 132 positions, 64- or 96-character set, 10 characters per inch, 6 lines per inch, 3.5- to 19.5-inch paper, 8-channel VFU, 27.5-ips slew rate; 300 lpm	Data Products
M46-304, -305, -306, -307	Same as M46-300 thru -303 but 600 lpm	Data Products
PUNCHED CARD EQUIPMENT		
M46-238, -239	Reader; 80-column, 1500-card hopper, 500-card stacker; 400 cpm	True Data
M46-236, -237	Reader; 80-column, 1500-card hopper, 1500-card stacker; 1000 cpm	True Data
PUNCHED TAPE EQUIPMENT		
M46-240, -241	Reader; 5-, 6-, 7-, or 8-level code, fanfold tank for oiled or unoiled paper or Mylar tape; 300 cps	Remex
M46-242, -243	Reader/punch; 5-, 6-, 7-, or 8-level code, fanfold tank for 200 feet (reader) and 1000 feet (punch), oiled or unoiled paper or Mylar tape; 300/75 cps	Remex
TERMINALS		
M46-064, -065	Carousel 300 Keyboard Printer Terminal; 132 positions, 64-character ASCII subset (96 opt.), opt. pin-feed tractor, opt. electronic format control, standard keyboard and numeric tab, 128-character-per-line buffer, RS-232 interface, locally or remote; 30 cps	Perkin-Elmer
M46-041, -042, -046, -048	Model 1200 Video Display Unit; 1920 characters, 24 lines x 80 characters, 9 x 12 dot matrix, typamatic repeat key feature, transparent mode for program debugging, 128 ASCII character set, opt. numeric keypad, buffered print port, opt. X-4 coordinate line drawing capability, polling select option for multidrop communications; includes controls for inverse video, half intensity, blink, protected, numeric only, nondisplay, and modified field definitions; editing features include insert/delete character or line, clear screen, clear unprotected and clear line/field; programmable send keys for all or part of screen data; up to 9600 bps; M46-046, -048 include function keyset	Perkin-Elmer
M46-044, -045	Printer port for Model 1200 (M46-044 for RS-232C interface, M46-045 for current loop)	Perkin-Elmer
M46-066, -068	Model 650 thermal printer for use with Model 1200 VDU; requires M46-044 or M46-045	Perkin-Elmer
M46-110, -111, -112, -113, -114	Model 550 Video Display Unit; 1920 characters, 24 lines x 80 characters, 128-character set, 5 x 9 character matrix; transparent mode for program debugging; includes controls for transparent mode, inverse video, bps rate, one or two stop bits, parity, full- or half-duplex; upper- and lower-case characters; 12-key numeric pad; up to 9600 bps; M46-110 does not include printer port, M46-111 thru -114 include printer port	Perkin-Elmer
M46-080, -082	Model 655 thermal printer for use with Model 550 VDU (M46-111 thru -114)	Perkin-Elmer

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translate data as desired. They can also be used to calculate and checksum polynomial error check redundancy characters such as those utilized for Binary Synchronous Communications (BISYNC or BSC), Synchronous Data Link Control (SDLC), High-Level Data Link Control (HDLC), and Advanced Data Communications Control Procedure (ADCCP).

Automatic hardware program relocation and protection in the Series 3200 are accomplished by the standard Memory Access Controller (MAC).

The I/O architecture includes a low-speed multiplexer bus (on both the 3220 and 3240) with the capability to attach 1,023 devices via firmware memory auto-driver channels. Throughput on the multiplexer bus is 400K bytes per second. An Extended Direct Memory Access (EDMA) bus includes seven ports on the 3220 and eight on the 3240, each of which can serve 16 controllers, providing high-speed direct memory access at a throughput of 8 million bytes per second. High-speed memory access on the 3240 is furnished by from one to four Direct Memory Access (DMA) buses, each of which can support 10 million bytes per second of I/O throughput for a total of 40 million bytes per second, distributed over 32 channels.

The present level of operating system support is provided by the OS/32 Operating System (OS/32), announced in January 1975. OS/32 is a real-time operating system providing a multi-tasking, multi-programming environment to support event-driven user application programs. Up to 255 user tasks can execute concurrently at user-defined levels of task priority. Concurrent batch-oriented processing is also supported. OS/32 requires a Perkin-Elmer 32-bit processor with 128K bytes of memory, the Memory Access Controller, operator's console (Carousel, teletypewriter, or CRT), a universal clock, power fail/auto restart, and magnetic media. OS/32 supports the full range of Perkin-Elmer peripherals, including Mini-I/O, a system for analog and digital I/O introduced in November 1975. Mini-I/O is designed for use in such areas as laboratory automation and materials handling. Programming can be handled through Perkin-Elmer supervisory calls or via ISA real-time extensions to FORTRAN.

The Loader Storage Unit, the library loader, loads the automatic boot load program (which includes self-test features to check out memory and certain processor functions before loading the operating system) in memory. Other utilities are OS Edit, OS Copy, OS Text, OS Patch, and OS Aids. Additional OS/32 aids are CUP (Configuration Utility Program), TET (Task Establishing Task), DIC (Disk Integrity Checker), Disk Dump (disk backup and compression), and Disk Initializer.

Supported programming languages include the Common Assembly Language (CAL), a macro assembler called CAL MACRO, FORTRAN VII, COBOL, BASIC II, CORAL 66, and RPG II. Under the control of OS/32, the Multi-Terminal Monitor (OS/32 MTM), allows up

modules. Memory on the 3240 is configurable in up to four banks interleaved over a common memory bus. Both processors use high-density MOS employing 16K RAM chips.

MULTIPORT MEMORY SYSTEM: Allows up to fourteen 32-bit processors, selector channel (SELCH), or I/O devices to share a common memory; each device has direct access to a maximum of one megabyte of memory, both shared and local memory. Any device connected to an extended DMA bus can access the memory system through the 19-bit extended DMA address.

A Multiport Memory System consists of two major sections: the memory banks and an interface board. The interface is physically and electrically located between the extended bus and the memory banks; it acts as a buffer and allows the extended bus to access up to eight memory banks. Each bank operates independently; all can actively service processors (or other devices) simultaneously.

A bank consists of one or two 7-inch multiport memory chassis, the actual number of chassis depending on the number of multiport memory multiplexers (MMM) and/or the amount of memory in the bank. An MMM provides a two-port access for two multiport memory interfaces into a memory bank and determines access priority, interleaving option, and addressing. A minimum bank consists of the following: a chassis, a power supply, a multiport memory controller (MMC), a multiport memory multiplexer, and a 32KB or 64KB memory module. Only one MMC is ever needed per bank. An MMC determines priority of multiplexer service and controls access to the core memory in the memory bank. A fully expanded bank includes 2 chassis, each with its own power supply, 1 MMC, 7 MMM's to support 14 processors, and either 512KB of memory when using 64KB modules or 256KB of memory when using 32KB modules.

Any memory bank can be configured with twelve additional processors by adding multiplexer boards (and perhaps an additional chassis). A priority strapping option within a memory bank allows it to service each processor in either a fixed or sequential (round-robin) manner. The fixed priority option allows high-priority devices to receive service upon request by locking out low-priority devices. The round-robin technique services each device in turn.

Other strapping options on the interface, multiplexer, and memory control boards allow for coding the way shared memory is organized: no interleaving, halfword interleaving, full-word interleaving, and double full-word interleaving. (Interleaving stores sequential halfwords in different memory banks.) In addition, memories can be selectively write-protected on 1K-byte boundaries with ROM chips on the MMM. This allows certain processors to read from, and write into, a particular section of memory, while other processors can only read from that protected section of memory. Protection is established on 1K-byte boundaries by setting a bit in the ROM for each increment of protection required. This feature, because it is in hardware, protects the memory in two different situations. The user task running in a CPU that does not have access to a protected area cannot overwrite a sensitive data area. Additionally, if one processor in the system malfunctions, it is prevented through hardware from destroying valuable data in multiport memory.

Other features of the multiport memory system enable the interface to respond to half-word, full-word, and burst mode read and write commands as well as to the halfword Test and Set most significant bit command. A strap option allows the interface to operate in a deferred response mode when long access times to the multiport memory system are expected.

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to 32 concurrent users to program interactively with the system in any mix of the supported languages.

A telecommunications access, ITAM/32, has been available since February 1975. Its device-independent level allows users to access remote terminals and computers as simply as they would use local peripherals, according to Perkin-Elmer. Meanwhile, its device-independent level gives users direct device control. In September 1976, ITAM/32 was enhanced to provide line-level or device-dependent support for Synchronous Data Link Control (SDLC). All Perkin-Elmer 32-bit software is unbundled and compatible across the entire range of 32-bit equipment.

Perkin-Elmer sales offices are located in 32 U.S. cities in 22 states, while repair centers are located in 38 U.S. cities in 25 states. Depot report capabilities are located in five of these cities. Internationally, Perkin-Elmer has subsidiaries in the United Kingdom, West Germany, France, Canada, Singapore, and Australia. Distributors handle the rest of the world and are located in Tokyo, for the Far East market; Chile, Bolivia, and Venezuela, for the South American market; Turkey, for the Asian market; and South Africa. Service facilities are located in 26 cities for the international market. Eleven of these cities have depot repair capabilities.

Maintenance is available on a contract basis for one, two, or three shifts, as well as on-call/on-site service and depot repair service. Training is available on both software and hardware topics. A number of courses are currently offered on a regularly scheduled basis at varying tuitions per course.

USER REACTION

Datapro interviewed five Series 3200 users, chosen at random from a list supplied by the vendor, during November 1979. Among the users were a public utility, a supplier of systems for banks, and three development systems houses.

All systems in use were Model 3220's, and all had been purchased outright from Perkin-Elmer. One user had six 3220's, another had five, another had three, and the other two had one each. Memory ranged from the basic 256K bytes to 768K bytes. On-line disk storage ranged from ten megabytes to 300 megabytes.

Programming languages in use included COBOL, assembly, FORTRAN, BASIC, and IBM's COBOL, PL-1, and RPG II. The systems were being used for business data processing, data communications, data base management, scientific/engineering computing, and data acquisition. Applications programs were written by in-house personnel in all cases, while "ready-made" programs from the vendor, proprietary software packages, and contract programming houses were mentioned as other sources.

Parity is generated and checked on address transmissions; generated and checked on data transmissions during write operations; and checked on data transmissions during read operations. Address transmission errors are indicated and remembered in the memory bank in a flip-flop. Accesses are aborted on address errors. Data parity errors during write operations are indicated and remembered in a flip-flop, and the data is stored in the memory as is.

Read operations transmit data and parity as it comes from memory. If there is a memory parity failure in the bank, it is indicated via a failure lamp. The interface checks parity, also, and transmits a memory fail code if an error is detected.

Physically, the multiport memory system uses standard 15-inch boards for the interface, multiplexer, and controller. The memory bank chassis is in a separate rack with its own power supplies. The interface board is mounted in the processor or in an I/O expansion chassis and connects to the extended DMA bus. The interface is connected to the memory bank by a cable; maximum length is 50 feet.

The storage capacity of the multiport memory system is limited to one megabyte, less the storage capacity of the largest local memory.

Currently available packaged configurations can serve as building blocks for even larger systems. Packaged configurations are as follows:

- **One bank, two-port contiguous memory, 64K bytes of 750-nanosecond core (M48-035).**
- **Two bank, two-port halfword interleaved, 64K bytes of 750-nanosecond core (M48-038).**
- **Four banks, two-port (optional full-word or halfword interleaved), 128K bytes of 750-nanosecond core (M48-040).**

CHECKING: A modified 7-bit Hamming code is appended to each 32-bit word. All single-bit errors are corrected, and all double- and most multiple-bit errors are detected. This error detection and correction is standard on both the 3220 and the 3240. An optional memory error logger identifies the memory module reporting a fault and indicates the location of the faulty memory chip.

STORAGE PROTECTION: Each task operates in a segmented logical address space of up to one megabyte. There are four types of program segments: Pure, Impure, Re-entrant Library, and Task Common. Each task must contain one Impure segment and may contain a maximum of 16 segments in any combination of the following: one Pure segment, up to 15 Re-entrant Library segments, and/or up to 15 Task Common segments. Each segment has a minimum size of 256 bytes and a maximum of 1 megabyte in increments of 256 bytes, limited only by the amount of memory available. The logical addresses in the user program are automatically relocated into physical addresses by the Memory Access Controller (MAC) in the 3220 and the Memory Address Translator (MAT) in the 3240, which also apply access protection according to the type of program segment being addressed.

The segmentation of programs into Pure and Impure segments allows programs to be shared for efficient multi-access or multi-threading. The Pure segment of such a program contains the static, unchanging code of the program. The Impure segment contains the dynamic work space of the program plus any impure code, e.g., overlays. Regardless of the number of times such a program is required for concurrent use, only one copy of the Pure segment is loaded into memory by the operating system, whereas as Impure segment is loaded each time it is needed. The operating system assures

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The results of the survey are summarized below:

	Excellent	Good	Fair	Poor	WA*
Ease of operation	3	2	0	0	3.6
Reliability of mainframe	3	1	0	0	3.8
Reliability of peripherals	3	0	0	1	3.3
Maintenance service:					
Responsiveness	1	2	1	0	3.0
Effectiveness	1	1	1	1	2.5
Technical support	1	3	1	0	3.0
Manufacturer's software:					
Operating system	1	4	0	0	3.2
Compilers and assemblers	2	2	0	0	3.5
Applications programs	1	0	0	0	4.0
Ease of programming	2	3	0	0	3.4
Ease of conversion	2	1	0	0	3.7
Overall satisfaction	3	2	0	0	3.6

*Weighted Average on a scale of 4.0 for Excellent.

One aspect of the Series 3200 Model 3220 which was consistently praised was its price/performance ratio. Users were also pleased with the 32-bit architecture, the language compatibility, the sixteen registers, the system's expandability, reliability of the hardware, and the compatibility offered, both up and down. One user has been "a Perkin-Elmer user for a number of years" and called the 3220 "super," and another called it "a piece of cake" (although he failed to specify what flavor).

On the other hand, dissatisfaction was expressed with the nonstandard interface of power connections, the amount of heat dissipated by the system, and some aspects of OS/32 ("no job scheduler," "spooler only adequate." One user said that his only complaint was that the "mainframe runs out of gas," but he was also quick to explain that was only because the equipment was being put to uses for which Perkin-Elmer had not intended it.

The overall impression received from these interviews was one of general satisfaction with the product and with Perkin-Elmer.□

the integrity of a Pure segment by using the MAC access protection facility to allow read-only access to Pure segments.

Re-entrant Library segments, also composed of pure code, contain commonly required re-entrant subroutines, such as the FORTRAN Run-Time Library. Task Common segments are sharable data areas accessible to any number of tasks. Access to Task Common segments is achieved symbolically in FORTRAN or assembler programs. The linkages are resolved by the Task Establisher, which is also used to request Read/Write or Read Only access to Task Common. The relocation, protection, and MAC or MAT fault interrupt programmed into the MAC and the MAT can be enabled or disabled under program control.

RESERVED STORAGE: The 3200 processor reserves approximately 2,300 bytes in low memory for the single-precision floating-point register save area, power fail save area pointer, various program status words, bootstrap loader and device definition table, system pointers, the basic and expanded interrupt service pointers, and supervisor call location counters. In addition, certain locations are reserved for use by the MAC/MAT. The basic interrupt service pointer table utilizes 512 bytes. The expanded interrupt service pointer tables employ 1536 bytes.

Additionally, a System Q (system queue), a special circular list with an automatic pointer in memory locations 128-131, is built into the 3200 architecture. In the event of any change in the program status word, the System Q list location pointed to is checked for any new additions. A new entry becomes the new PSW, providing hardware CPU dispatching.

CENTRAL PROCESSOR

The Models 3220 and 3240 are Schottky TTL (transistor/transistor logic), MSI and LSI (medium- and large-scale integration), 5-board (3220) and 8-board (3240) processors with hardware multiply/divide and direct addressability of up to four million bytes of main memory on the 3220 and 16 million bytes on the 3240 in four interleaved banks.

CONTROL STORAGE: The 3220 and 3240 run under control of a 60-nanosecond bipolar ROM fixed control store of 2048 32-bit words. These work with a 260-nanosecond microinstruction processor with a repertoire of 60 instructions. The microinstruction processor uses only 32-bit words, not halfwords, bytes, or bits. Microcode in the 3200 CPU recognizes 257 operation codes: 253 standard instruction operation codes plus four that permit the user to employ WCS (Writable Control Store). Forty-seven operation codes each are recognized, respectively, by control store on the CPU for use in the optional single- and double-precision floating-point hardware features.

WRITABLE CONTROL STORE (WCS): This optional feature provides users with 2,048 words of dynamically alterable high-speed control store memory, organized as an extension to the 2,048 words of fixed read-only control store. A speed advantage of two to three times over conventional software can be realized when special algorithms or other functions are implemented in WCS. Each 32-bit word in writable or fixed control store represents one machine-level microinstruction. Four instructions support this feature: Enter Control Store (ECS), a nonprivileged instruction that can be located anywhere within a user-level routine to call a WCS routine; Branch to Control Store (BDCS), a privileged instruction to transfer processor control to WCS; Write Control Store (WDCS), a privileged instruction that transfers a data buffer from main memory to WCS; and Read Control Store (RDCS), a privileged instruction that transfers a data buffer from WCS to main memory.

The ECS instruction transfers control to one of 16 different locations in WCS to initiate one of 16 different microcoded functions. Control is returned to the fixed ROM upon completion of the function.

REGISTERS: The 3200 Series minicomputers have 128 32-bit general registers in eight sets of 16. Four dedicated sets (numbered 0, 1, 2, and 3) handle the four external interrupt levels. The remaining four sets (numbered 4, 5, 6, and 15) are allocated by the operating system as necessary. There are also eight optional single-precision floating-point registers, each 32 bits wide and identified by the even numbers zero through 14, and eight optional double-precision floating-point registers, each 64 bits wide and identified by the even numbers zero through 14. The single-precision and double-precision registers are separate. Floating-point operations must always specify even-numbered registers.

With the Memory Access Controller, 16 32-bit hardware segmentation registers are provided to allow segmentation, relocation, and memory protection of user programs and data.

ADDRESSING: Three addressing modes are available: direct, indexed, and relative. Depending on the format of the instruction, operand addresses can be indexed by one or two index registers or can directly address any part of main storage. Fifteen of the 16 32-bit registers in any of the general sets

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in use can be used as index registers. Instructions in the RX2 format automatically place the second operand relative to the program location counter. The RX3 format permits double-indexing to an absolute address up to the full memory capacity of a system.

Indirect addressing is not available. Memory is byte-addressable.

INSTRUCTION REPERTOIRE: 206 operations are standard, and 52 are optional. There are 4 WCS instructions, 21 single-precision floating-point instructions, 20 double-precision floating-point instructions, 5 mixed-mode floating-point instructions, and 2 high-speed data handling instructions, all optional.

The standard instructions are: 81 logical, 47 floating point, 17 fixed point, 8 string manipulation, 74 branch, 8 I/O, 18 status and control, and 4 Writable Control Store.

Bit manipulation instructions can be valuable to users with large amounts of binary data to handle, for example, in process control and data acquisition applications. The instructions provide the ability to index through bit arrays bit by bit while testing, setting, resetting, or complementing bits in the array.

List processing instructions can manipulate any number of circular lists (stacks with wraparound), each up to 65K words in length. They permit adding or deleting elements to or from the top or the bottom of the list. They can be used as two pushdown stacks back-to-back, as a queue (first-in/first-out; a stack, by comparison, is last-in/first-out), or a deque (double-ended queue). Condition codes reflect changes in the list (e.g., empty, full).

The high-speed data handling (communications) instructions are used to compute polynomial error check redundancy characters, as used by most data communications protocols. Communications protocols supported by this option include, but are not limited to: Binary Synchronous Communications (BISYNC or BSC), Synchronous Data Link Control (SDLC), Advanced Data Communications Control Procedure (ADCCP), and High Level Data Link Control (HDLC).

INSTRUCTION TIMINGS: The following timings are in microseconds for 32-bit fixed-point and 32-bit and 64-bit floating-point operations performed by 3220 hardware. Floating-point instructions use the RR and RX instruction formats. Timings for the 3240 are not available.

	32-bit fixed	32-bit floating	64-bit floating
Load/Store	0.70	1.75	2.60
Add/Subtract	0.45	1.25	1.25
Multiply/Divide	8.30/10.25	1.85/3.85	1.85/7.05
Compare & Branch	1.35	1.05	1.05

INTERRUPTS: The 3200's have four separate priority lines with 1,024 levels. Each level is automatically vectored and has automatic device identification. The average interrupt response time is given by the vendor as 5.9 microseconds with a 2-microsecond latency. There is a 25-microsecond timeout on all microprocessor operations to the I/O system to insure against any failing I/O device locking out the processor.

The four separate priority (external interrupt attention) lines automatically activate different general register stacks. All interrupts are through the multiplexer bus, even final device interrupts on the selector channels. The external interrupt attention lines feed into the dedicated register sets 0 to 3. These register sets are then utilized to determine which interrupt lines are enabled. The architecture of the 3200's could handle 15 attention lines to match the inherent ability of the architecture to handle 16 sets of general registers, but at present the user's general registers (4, 5, 6, and 15) have no strappable external interrupt attention line options available, and the second eight sets of registers are not implemented.

Perkin-Elmer quotes an interrupt response time of 5.9 microseconds as the maximum time taken to recognize the line, store the old program status word, load the new PSW, and activate at the new PSW location. The 2.0-microsecond latency is the average length of an uninterruptible instruction. These times do not include the time to "context switch," i.e., save and restore register stacks, which varies depending on stack lengths.

The OS/32 operating system supports interrupts in a way which Perkin-Elmer calls "task-handled traps." This amounts to a choice of whether an interrupt caused by a task-connected event will be processed by the task or by the operating system. For example, in a divide overflow the task handles the overflow rather than have the operating system "flush" the program for a simple data error. OS/32 places this trap and others at the user level.

PHYSICAL SPECIFICATIONS: The processors and all memory fit within a single upright cabinet that is 56 inches high and which can house two additional 7-inch chassis for I/O expansion. The CPU chassis is 14 inches high and 17 inches deep and has 16 slots.

The cabinet is cooled by forced air. Power requirements are 90-132 VRMS (brown-out protection), 47-63 Hertz, 13 Amperes. An additional power supply is required when any or all of the following options are included: memory above 256K bytes, the floating point processor, cache memory, and WCS. Power requirements for the additional power supply are 180-264 VRMS (brown-out protection), 47-63 Hertz, 6.5 Amperes.

The processor requires an environment of from 32 to 122 degrees Fahrenheit at 50 to 90% noncondensing humidity to operate; storage conditions can be more severe. The processor is subjected to vibration testing prior to shipment. Circuit boards are 15 inches square, use multi-wire technology, and are packaged horizontally, with 1/4-inch stiffeners. The backplane is a printed circuit, and contacts are pins to dual-contact receptacles with locating pins.

INPUT/OUTPUT CONTROL

The Model 3220 has two communications buses; one multiplexer bus and one Extended Direct Memory Access (EDMA) bus with seven channels. The Model 3240 has a multiplexer bus and from one to four Direct Memory Access (DMA) buses.

The multiplexer buses (man/machine interface) service slow- to medium-speed devices such as printers, consoles, card readers, etc., while the EDMA bus and the DMA buses serve as connections for high-speed secondary storage devices such as disks and tapes.

I/O CHANNELS: The multiplexer I/O channel supports up to 1,023 devices, divided among four priority levels. The user can assign device priorities. Data transfers over the multiplexer bus are accomplished in two ways: a byte or a halfword is transferred between a multiplexer bus device and memory under control of an I/O instruction or multiplexed blocks of data are transferred between a multiplexer bus device and memory. The transfer of blocks of data is accomplished by the Auto Driver Channel, which is driven by the fixed control store. The channel performs automatic character translation and computes cyclic redundancy checksums and longitudinal redundancy checksums used in communications devices. Throughput on the multiplexer bus is 400K bytes per second.

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The 3220's EDMA bus supports seven high-speed ports to and from memory. Each port is controlled by a selector channel, which initiates and terminates data transfers. Each selector channel can support 16 device controllers that can transfer either individual 16-bit halfwords or burst groups of two to 14 halfwords to or from memory. In burst mode, a selector channel can transfer 5.71 million bytes per second when writing to memory and 8 million bytes per second when reading from memory. The selector channels are programmed using the multiplexer bus; once a channel has been activated, the processor is free. A special EDMA logic interface is available for implementing custom-designed interfaces.

The 3240 DMA bus I/O throughput is 10 million bytes per second. A total throughput of 40 million bytes per second, distributed over 32 channels, is possible with the maximum four DMA buses available on the 3240.

CONFIGURATION RULES

The basic 3220 system consists of a 16-slot chassis, 256K bytes of MOS memory with ECC, Memory Access Controller (MAC), eight sets of 16 32-bit general registers, Loader Storage Unit, Power Fail/Auto Restart, Model 550 terminal as a systems console, two-line communications multiplexer, 20-minute battery back-up (256K bytes), a 50-amp power supply, cabinet with AC distribution panel, and system control panel. An additional power supply is required in configurations where any or all of the following options are installed: memory above 256K bytes, floating-point processor, cache memory, and writable control store.

The MAC creates the extended DMA (EDMA) bus. The MAC also contains the DMA buffer, which can support seven DMA channels over the EDMA. Each DMA channel can support up to 16 high-speed devices.

The basic 3240 system, a 3241, includes 512K bytes of MOS memory with ECC, floating point processor, eight sets of 16 32-bit general registers, Memory Address Translator (MAT), four levels of interrupts, 8K bytes of cache memory, eight DMA ports, Model 550 CRT, 2K words of Writable Control Store, 75-ips magnetic tape drive, and 80-megabyte disk drive.

MASS STORAGE

M46-617 10-MEGABYTE REMOVABLE CARTRIDGE DISK SYSTEM: Uses a 5-megabyte fixed disk and an IBM 5440-equivalent, 5-megabyte disk cartridge. Actual formatted drive capacity is 10,027,008 bytes. Average head positioning time for this top-loading, 200-tpi drive is 33 milliseconds. Track-to-track head movement time is 10 milliseconds. Movement time across all tracks is 60 milliseconds. Average rotational delay is 12.5 milliseconds. There are 408 tracks per surface with 4 tracks per cylinder (one from each surface), making a total of 408 cylinders per disk cartridge.

Unformatted track capacity is 7812 bytes. Formatted track capacity is 6144 bytes divided into 24 sectors of 256 bytes each. Bit density is 2200 bpi. Rotational speed is 2400 rpm, and the data transfer rate is 312,500 bytes per second.

The basic system includes a drive, controller, and disk cartridge. Three additional drives with built-in power supplies (M46-619) can be added to the basic controller. The M46-618 and the M46-620 are the 230-volt versions of the M46-617 and the M46-619, respectively. Hardware write protection is a standard feature. The manufacturer is Perkin-Elmer.

M46-604 MSM300 256-MEGABYTE REMOVABLE MEDIA MASS STORAGE MODULE SUBSYSTEM: Uses a 3330-technology 12-platter disk pack. Ten of the 12 platters are used as recording surfaces, with 19 surfaces for data and the remaining surface for servo use. The remaining two platters are for protection, with one located on top of the pack and the other on the bottom.

Each of the disk pack's 19 usable surfaces contains 808 data tracks plus 15 spares. Each cylinder is composed of 19 tracks. Track density is 384 tpi, while bit density is 6000 bpi. Total track capacity, unformatted, is 20,160 bytes. Formatted track capacity is 16,384 bytes divided among 64 sectors of 256 bytes each. Unformatted drive capacity is 300 megabytes. Perkin-Elmer's formatting limits the total drive capacity to 256 megabytes.

The basic system includes an MSM300 drive, a controller for up to four drives, and a removable disk pack. The add-on drive is the M46-605 Model MSM300E. The equivalent master and add-on 220-VAC 50-Hertz drives are, respectively, the M46-606 and M46-607.

The drives have a rotational speed of 3600 rpm, resulting in an average rotational delay of 8.3 milliseconds. Times of 10, 30, and 55 milliseconds, respectively, are given for the track-to-track, average, and across-all-tracks head movements. The data transfer rate is 1.2 megabytes per second. Data security techniques discussed under the M46-600 below apply here. The drives are manufactured by Control Data (9766).

M46-600 MSM80 67-MEGABYTE REMOVABLE MEDIA MASS STORAGE MODULE SUBSYSTEM: Uses a 3330-technology five-platter disk pack. Three of five platters are actually used, with five surfaces for data and the sixth for servo use. As in the MSM300, the remaining two surfaces provide protection. The basic system includes an MSM80 drive, a controller for up to four drives, and a removable disk pack. The add-on drive is the M46-601 Model MSM80E. The 220-VAC 50-Hertz versions of the master and add-on drives are, respectively, the M46-602 and M46-603.

Bit density for the storage module is 6000 bpi, while track density is 384 tpi. There are 808 data tracks plus 15 spares per surface. Each cylinder contains five tracks. Unformatted track capacity is 20,160 bytes. Formatted track capacity is 16,384 bytes divided among 64 sectors of 256 bytes each. Drive capacity, based on formatted data, is 67 megabytes; unformatted, the capacity is 80 megabytes.

Track-to-track, average, and across-all-tracks head movement times are 6, 30, and 55 milliseconds, respectively. Average rotational delay is 8.3 milliseconds, based on a rotational speed of 3600 rpm. The data transfer rate is 1.2 megabytes per second.

Data security is provided by a write protect feature with positive manual control, electronically inhibiting write functions upon detection of a seek error, track position error, loss of rotational speed, or loss of voltage. The last two malfunctions also cause head retraction. The drives are manufactured by Control Data (9762).

INPUT/OUTPUT UNITS

See Peripherals/Terminals table.

In addition to the conventional devices listed in the Peripherals/Terminals table, Perkin-Elmer offers a line of interface devices particularly useful in measurement and control applications. These devices are called Mini I/O.

A Mini I/O analog input subsystem includes up to 32 single-ended or 16 differential inputs operating at up to 20, 33, 40, or 75 kilohertz with a resolution of 10 or 12 bits. Options include four programmable system gain levels and an instrumentation amplifier, which enables the user to interface two low-level channels in addition to the high-level signals normally supported. All models include a sample and hold analog-to-digital converter.

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An analog output subsystem provides two or four output channels with any of five preselected output voltage ranges up to - 10.24 volts. Resolution is 12 bits. One model includes control signals for an oscilloscope.

A digital I/O subsystem provides 16 latch outputs (up to 50 volts) and interfaces 16 TTL, contact, or voltage sense, digital input (4 to 50 volts).

Programming of the Mini I/O subsystems via Perkin-Elmer supervisory calls or ISA real-time extensions to FORTRAN VII is supported under OS/32.

COMMUNICATIONS CONTROL

DIRECT MEMORY ACCESS I/O SUBSYSTEM (DIOS-M47-015): The DIOS is a high-performance, highly flexible intelligent communications controller for the Perkin-Elmer Series 3200. The DIOS provides Direct Memory Access (DMA) facilities between main memory and multiple I/O devices, allowing data transfers to take place with no processor intervention. The DIOS supports up to 63 two-wire or 31 four-wire communications devices. For asynchronous devices, the DIOS supports both the two-line and eight-line communications multiplexers as well as Perkin-Elmer's earlier PALS and PASLA equipment. For character-synchronous or bit-synchronous devices, the DIOS supports the Single Line Synchronous Adapter, the Quad Synchronous Adapter and the earlier 201/301 Data Set Adapter (character synchronous only).

The DIOS is fully supported under Perkin-Elmer's 32-bit operating system, OS/32, and provides a peak throughput of 100,000 characters per second, data rates up to 56 Kilobaud per line, hardware Cyclic Redundancy Check (CRC) generation and checking, and comes with built-in comprehensive diagnostic testing hardware.

The DIOS microcode contains special routines to support selected communications protocols. For asynchronous devices the DIOS microcode routines enable an entire terminal screen (maximum of 1,920 characters) in Perkin-Elmer's RELIANCE software environment to be transferred between the terminal and the processor. Processor intervention is required only to initiate and terminate the data transfer. During the transfer, the Perkin-Elmer Series 3200 processor is free to service other tasks. For synchronous devices the DIOS microcode routines support BISYNC protocol. Special character handling routines process the many control characters of the BISYNC protocol in a manner fully compatible with the OS/32 BISYNC line driver. This enables higher level software, such as Perkin-Elmer's 2780/3780 Emulation, HASP/32, 3270 Emulation and 3270 Support packages, to use DIOS hardware without modification.

For bit-synchronous devices the DIOS microcode routines provide full support for the continuous frame transfer capabilities of the Zero Bit Insertion/Deletion versions of the Quad Synchronous Adapter and Single Line Synchronous Adapter. Using OS/32's chained or queued buffer techniques, processor intervention is required only once per frame or buffer. The DIOS handles all device status checking and frame check sequence generation/validation. When used in conjunction with Perkin-Elmer's ZDLC Channel Terminal Manager software package, the DIOS provides a comprehensive high-throughput support package for all three industry standard bit-oriented protocols: SDLC, HDLC, and ADCCP.

The QUAD SYNCHRONOUS ADAPTER (QSA-M47-003) is an economical and highly flexible communications interface for Perkin-Elmer's Series 3200 computer systems and standard synchronous communication lines. QSA, constructed on one 15-inch board, contains all of the serializing, deserializing, and character buffering necessary to accommodate four synchronous lines. QSA is available in two versions; M47-002 accommodates traditional binary synchronous protocol or other similar character oriented protocols, and M47-003 accommodates both the new bit-stuffing features required by SDLC, ADCCP, or HDLC and the widely used binary synchronous or other character oriented protocols. Each line can operate individually in either half duplex or full duplex mode.

The transmission rate of the QSA is established by the particular modem, which must supply the clock signals. QSA is unaffected by the transmission rate as long as the rate does not exceed the upper limit of the unit—1.6M baud or 200,000 characters per second.

During binary synchronous transmission, data are transmitted bit serial and synchronization or character framing is achieved when the QSA detects a character match between the incoming characters and one previously established by the program. This match character called a sync character, is any 5, 6, 7, or 8-bit character in the range of X'03:X'FE' (with or without parity), it is program selectable for each line in non-bit stuffing mode.

The new "bit-stuffing" or zero bit insertion/deletion (ZBID) mode is required to support the recently implemented bit oriented protocols. When the QSA with ZBID capability is selected this function may be enabled/disabled under program control on a line basis. When enabled the flag character is fixed as to pattern and size. The flag character is automatically sent by QSA at the beginning and end of each transmission. QSA also automatically provides zero-bit insertion and deletion as the particular bit stream is transmitted or received.

The SINGLE LINE SYNCHRONOUS ADAPTER (SSA-M47-107) is a highly flexible data communications interface for Perkin-Elmer's 3200 family of computer systems. The SSA provides an economical telecommunications interface between the computer and the data set (modem) used with common carrier switched or leased facilities.

The SSA is a double-buffered communications interface and controller for the Bell Series 200 synchronous modems or equivalent. The SSA supports both half duplex (2-wire) and full duplex (4-wire) operations. Synchronous modems permit higher baud rates over voice grade facilities, allowing more efficient data transmission and lower line costs. The SSA is available in two versions; M47-106 accommodates the traditional binary synchronous protocol or other similar character-oriented protocols, and M47-107 accommodates both the traditional binary synchronous protocols and the Zero Bit Insertion/Deletion (ZBID) and flag insertion/deletion as required for bit-oriented protocols such as SDLC, HDLC, and ADCCP.

In the operational environment, the user-provided modem supplies the clock signals that determine the data transmission rate for the SSA. Perkin-Elmer's SSA is not affected by the transmission rate as long as it does not exceed the SSA's upper limit of 2M bits/second.

During binary synchronous transmission (or any similar character-oriented protocol), data is transmitted in a bit serial fashion. Synchronization, or character framing, is achieved when the SSA detects a character match between the incoming characters and the character previously set-up by the program. This match character, called a sync character, can be any 5, 6, 7, or 8-bit character in the range Hex '03' to Hex 'FE' (with or without parity). The sync character is program-selectable.

For bit-oriented protocols (SDLC, HDLC, etc.), the SSA is ordered with Zero Bit Insertion/Deletion (ZBID) capability. The ZBID function can be enabled or disabled under program control. When enabled, the pattern and size of the flag character are set. The flag character is automatically sent by

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the SSA at the beginning and end of each transmission. The SSA also automatically provides Zero Bit Insertion and Deletion, as required between flags, while the bit stream is transmitted and received, respectively.

The COMMUNICATIONS MULTIPLEXER (COMM MUX) provides an interface between the standard multiplexer bus and 103/202-type modems over switched or leased facilities. Local terminals requiring RS-232 or current loop connection can also be accommodated. The COMM MUX provides high reliability, lower cost per line, and lower power consumption per line. The COMM MUX affords maximum flexibility by providing program control over those functions most subject to variation and change: baud rate, line control, and character format. The COMM MUX is available in two versions, the M47-104 two-line COMM MUX, and the M47-105 eight-line COMM MUX. The eight-line COMM MUX is the same as the two-line COMM MUX except the eight line COMM MUX provides eight asynchronous communications lines with RS-232C interface only. All eight lines are individually programmable. All other features and options available on the two-line COMM MUX are available on the eight-line COMM MUX.

SOFTWARE

OPERATING SYSTEM: A hallmark of Perkin-Elmer operating systems is that they are all highly "Sysgenable;" that is, the system generation capabilities for incorporating exactly those operating system functions a user needs are usually effective. Also, the company's 32-bit OS/32 operating system emphasizes ease of use.

OS/32 Operating System (OS/32) was released in January 1975 and requires a 256K-byte Series 3200 processor with operator console panel, power fail/auto restart option, memory access controller, teletypewriter, Carousel, or CRT on a current loop interface for use as an operator command console, universal clock, and magnetic media (which may be nine-track magnetic tape or 10-megabyte disc). OS/32 supports nine-track, 800 or 1600 bpi magnetic tape; 2.5-, 10-, 67-, or 256-megabyte disc; paper tape reader/punch; cassette; card reader; all line printers; ASR 33/35 teletypewriters; CRT's; A/D and D/A conversion equipment; and digital I/O modules.

OS/32 is a real-time, multitask, multiprogramming monitor with up to 255 levels of task priority, concurrent batch background processing, and re-entrant I/O handlers. OS/32 also controls memory through memory segmentation and relocation via the memory access controller. File management consists of file protection at the file and task levels, named files and devices, system calls for file manipulation, file-oriented console commands, and two file structures. These structures are indexed and contiguous.

As should be expected in any multiprogramming system, OS/32 has traps for privileged instructions. OS/32 features task-handled traps, which allow a task to be either external event or time-driven, and also provide for intertask communications.

Tasks can be one of three types: foreground, user/executive, and background. Task scheduling priorities are user-defined. Events affecting priority are: operator requests, hardware interrupts, intertask communications/activations, and time-related events including time of day, elapsed time out, and periodical events.

LANGUAGES: Perkin-Elmer offers the Common Assembly Language (CAL), 32-bit FORTRAN VII, COBOL, BASIC Level II, and RPG II.

CAL is a cross assembler that can be executed on either a 16- or 32-bit Perkin-Elmer processor and can produce object code that can in turn be executed directly on either a 16- or 32-bit machine. Since CAL is an assembler that is target-machine-independent, and since Perkin-Elmer's OS/16 (for 16-bit computers) and OS/32 operating systems are compatible, the company in fact offers computer lines that are supported by fully compatible software.

CAL is a two-pass assembler that incorporates a multi-pass machine-code optimizer which is invoked by the SQUEZ (squeeze) command. CAL has a facility to process "common code," which is essentially similar to machine code but not specific to the processor architecture (16 or 32 bits). The assembler facilitates re-entrance by separating "pure" and "impure" program segments (i.e., code-only from code with data). It provides an annotated cross-reference listing of symbolic references to aid in debugging programs.

CAL permits eight-character alphanumeric symbols, provides common block definition and initialization that is FORTRAN-compatible, and allows conditional assembly pseudo-operations. A companion program, the *CAL Macro Processor*, establishes and processes the library of macros. These may be positional or keyword prototypes, nested macros, variable operation codes, operand sublists, and conditional macro expansions. A macro library is used to define the system environment, describe the register names, and perform I/O. The library includes task management, intertask communication, file management, and general services.

Perkin Elmer's 32-bit *FORTRAN VII* is a globally optimizing FORTRAN compiler with a comprehensive suite of support software. Real and double precision variables are supported by the processor's floating-point facilities, giving six digits of precision for real numbers and sixteen digits for double precision. In addition to sixteen general purpose registers, sixteen floating-point registers are available to the compiler for evaluating expressions and for temporary storage. Complex variables are represented by two real values. Two forms of INTEGER are supported, fullword (*4) and halfword (*2), allowing a choice between the wide range of 32-bit values and the space economy of halfwords. LOGICAL variables and Hollerith and hexadecimal constants are supported. Mixed mode arithmetic facilities add to the repertoire of data types.

The FORTRAN VII system provides two compilation modes: operational mode, using the full facilities of the global optimizations, and developmental mode, which provides high throughput compilation and debugging to multiple users. In operational mode, the compiler performs a wide range of optimizations globally across the scope of the whole program module. Optimizations are made at the FORTRAN-source level. FORTRAN VII analyzes its execution resource requirements and, from a global viewpoint, allocates the computer resources to the elements of the program. Through these machine-dependent optimizations, FORTRAN VII ensures that the best possible use is made of the 32-bit architecture.

Real-time extensions give FORTRAN VII programs access to the real-time facilities of OS/32. These facilities, based on the ISA proposals, include intertask communication and control, interaction with external events, time of day and interval clock awareness, file creation and access, analog/digital conversion and digital I/O, and internal fault detection and response. The input/output system supports READ and WRITE statements and includes the subprograms used by the diagnostic facilities to provide test and trace information. The formatter performs run-time interpretation of FORMAT statements to provide conversion and editing of information between internal representation and external character strings. The formatter also provides support for ENCODE and DECODE facilities which provide storage-to-storage data manipulation. In addition to being device-independent, FORTRAN I/O is dynamically file-independent; device numbers can be assigned, via OS, to any file-name or device before and during program execution.

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Accuracy is claimed as being better than five decimal digits for real functions and better than 14 decimal digits for double precision. As an option, many commonly used mathematical functions are implemented as microcode for execution in Writable Control Store at approximately double the speed. Language extensions provide users of FORTRAN VII with access to data types and operations not available within the language itself, including logical operations on bit strings, logical shift operations on integers, manipulation of individual bits, byte processing, and queueing and pushdown operations on Perkin-Elmer circular list structures.

In developmental mode, development facilities are provided under the OS/32 Multi-Terminal Monitor, which allows interactive program development by up to 16 terminal users simultaneously. During program development, individual FORTRAN VII programs are compiled, directly to linkable object code, at a speed in excess of 1,000 lines per minute. Under normal loads, terminal users receive almost immediate compilation turnaround.

The *3240 FORTRAN Enhancement Package (FEP)* is a fully-integrated firmware and software package which significantly improves FORTRAN VII program and compiler execution speeds. FEP improves performance by providing selected FORTRAN Run-Time Library (RTL) routines and compiler routines implemented in high-speed Writable Control Store (WCS). The FEP is transparent to a customer's system. FORTRAN programs are compiled normally and no special source statements are needed to take advantage of the package.

FEP provides FORTRAN users with a set of RTL routines whose speed and accuracy benefit users in almost every FORTRAN application and compiler support routines to increase the efficiency of the optimizing compiler. FEP contains software necessary to yield performance improvements, microcoded firmware, and a special WCS loader that also provides power fail recovery. Sixteen FORTRAN RTL and two compiler routines are implemented for the 2K-byte Writable Control Store. The degree to which performance improves depends on the extent to which user programs call the WCS RTL.

In addition to speed benefits, the FEP Run-Time Library routines offer extreme accuracy. Whereas many algorithms sacrifice speed for accuracy or vice versa, FEP routines optimize both. In testing FEP RTL routines, Perkin-Elmer says that the two major criteria under evaluation were that most errors must be one bit or less and that the worst case errors must not exceed three bits. Perkin-Elmer claims that FEP meets and exceeds these criteria for virtually all RTL routines.

The FORTRAN assembly language routines are replaced by the FEP Library, but no source FORTRAN need be altered. The new system automatically uses the WCS routines. When the user's program calls an RTL routine which is implemented in the WCS, the assembly RTL issues the linkage into WCS (to the entry point for the appropriate routine). For example, a program that calls the SIN routine still enters the assembly RTL entry point called SIN. The FEP assembly RTL immediately enters the WCS microcoded SIN implementation. CAL programs can also call the WCS RTL routines. Detailed documentation describes the entry and exit linkage necessary to interface through CAL.

System requirements include a Model 3240 processor with WCS, power fail/auto restart, and DFU option; OS/32 and associated system requirements; and FORTRAN VII.

COBOL, as implemented by Perkin-Elmer, conforms to ANSI Standard X3.23-1974 and supports many high-level ANSI 1974 features. Additional syntaxes are provided to facilitate the coding of programs for on-line concurrent use in a Reliance transaction processing environment. COBOL is integrated with other Perkin-Elmer software so as to provide for a variety of business data processing applications. Perkin-Elmer's COBOL includes these modules: nucleus, table handling, sequential I/O, relative I/O, interprogram communication, indexed I/O, sort, library, and debug.

COBOL is the procedural language for Data Management System/32. An enhanced indexed I/O module provides a standardized high-level language interface to the data management system, specifically designed for an on-line transaction processing environment and including such features as secondary indices and automatic record locking. Data integrity is safeguarded by the transaction unit concept. A COBOL run unit is divided into a series of consecutive transaction units, each of which includes a series of input/output statements. If any transaction unit fails to complete, any updates carried out are automatically and irreversibly nullified, returning any records affected by that transaction unit to their original state prior to the commencement of the transaction unit.

COBOL programmers can also exercise direct, explicit transaction unit control through the use of two new COBOL verbs: END TRANSACTION UNIT and FAIL TRANSACTION UNIT, created by Perkin-Elmer to facilitate the processing of transaction units. Users can code in a straightforward manner, updating files at the logical place in the program. If the user then decides to negate a set of updates, the FAIL statement is used to accomplish that end. Writing lengthy and complex backout and recovery procedures becomes unnecessary.

COBOL is available as a separate product or as a component of Reliance.

BASIC Level II conforms to the conventions of Dartmouth's BASIC and operates on the Series 3200 processor under OS/32. It is a superset of Dartmouth BASIC and, as such, includes enhanced I/O facilities, string and matrix extensions, and user-defined arithmetic functions. Enhancements to I/O facilities include file manipulation performed completely from within the BASIC program via the operating system, thus allowing such access as indexed and contiguous. String and matrix extensions inlcude matrix arithmetic performed within the BASIC program, subscripting of either end of a variable-length string, and substring deletion. A debugging feature traces line number execution throughout a program, while a program entry feature makes it impossible to create unexecutable instructions.

Both single- and double-precision arithmetic operations can be handled. Single precision to 6 digits of significance and double precision to 14 significant digits are standard.

BASIC Level II programs can be saved and restored from files. Programs can be segmented and overlayed and can call assembly-level subroutines; program sequences can be chained together and allowed to run autonomously. BASIC Level II requires 19K bytes of memory beyond the operating system requirements plus a minimum of 1K bytes per user. Also required are an operator console panel (either binary or hex display), an operator command console, and a magnetic medium. The command console may be either a Carousel terminal, teletypewriter, or display terminal. The magnetic medium may be a cassette tape, 9-track magnetic tape, 25-megabyte cartridge disk, or 10-megabyte cartridge disk.

Data Management System 32 (DMS/32) has been designed specifically for an on-line transaction processing environment and is a component of the Reliance software system. DMS/32 provides multi-keyed data update and retrieval from multiple user files in a single data base and manages real-time concurrent data access by maintaining data base integrity through automatic on-line recovery features, record and file locking, and means for rapid restoration of the data base in case of a system failure. Among the features of

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DMS/32 are: an unlimited number of secondary keys; random and sequential access; data access by full, approximate, and generic keys; multiple files with multiple extents; control of concurrent access; on-line rollback of failed transactions; automatic recovery from any system failure; central control of the data base; and access through COBOL, RPG II, and Perkin-Elmer's Common Assembler Language MACRO's.

Perkin-Elmer's *RPG II* is an implementation of standard RPG II. Originally designed for the sole purpose of aiding in the production of reports, RPG II now handles a wide variety of business applications. By using standard RPG II specification sheets, users describe files, data tables, arrays, and information relating to the processing of input data and to the generation of output data and reports. RPG II is compatible with IBM System 3 RPG II. Perkin-Elmer RPG II is designed to be used in conjunction with the Reliance transaction processing system and uses a fixed logic cycle to process a variety of file types. Indexed file processing in RPG II is accomplished via Data Management System/32 (DMS/32). RPG II includes industry-standard source specifications; sequential, random, and indexed file organizations; tables and arrays; compile and run-time array bounds checking; complete set of indicators; over 300 compile-time error messages; debugging with enhanced trace facilities; run time diagnostics, many with user-action options; and file and field symbol tables.

Reliance is a complete software system designed to implement transaction processing on any of Perkin-Elmer's 32-bit minicomputers and includes the Integrated Transaction Controller (ITC), Data Management System/32 (DMS/32), and COBOL. The system supports up to nine application programs running in parallel and maintains system performance at user terminals under extremely heavy transaction volume. ITC controls and monitors application programs and libraries, provides complete application facilities for system building, and enables the user to interactively create and modify screen formats while handling data validation and screen format control automatically. DMS/32 provides central data base-oriented file and data management and maintains file directories. Each file can have an unlimited number of keys to allow access from any user. DMS/32 also provides secondary indices, record locks, transaction units, secure logging, and fast recovery procedures. Facilities required by batch processing environments are also included. The DMS/32 portion of Reliance exists as a separate task, is shared by all users, and provides central control. Each user task "sees" a response from the data manager as if it were the only task in the system. DMS/32 includes automatic transaction rollback, automatic record locking and unlocking, a rollforward technique for data base reconstruction, and continuous automatic reconstruction. COBOL is the commercial language included for applications programming. COBOL data and media formats are compatible with industry standards, simplifying the conversion of existing application programs. The optional Multi-Terminal Monitor (MTM) enables up to 32 programmers to perform any mix of data processing activities, including source entry, compilation, and program testing, independently and concurrently.

COMMUNICATIONS SOFTWARE: The basic 32-bit operating system, OS/32, includes telecommunications support for modems, local or remote asynchronous terminals, a BISYNC line driver, and the software drivers for the DIOS intelligent communications controller.

ITAM/32 (Integrated Telecommunications Access Method) was released in July 1975. As of November 1979, the ITAM facility is provided as an OS/32 component. For synchronous lines, a Bell 201-type Data Set Adapter or Quad Synchronous Adapter is supported. Bell 103-type modems are supported at up to 300 bits per second. For asynchronous lines, either single- or multi-line controllers are supported. Bell 201-, 208-, and 209-type modems are supported at 2400, 4800, and 9600 bits per second, respectively. Dataphone Digital Service (DDS) Data Service Units (DSU's) are supported to 9600 bits per second.

The 2780/3780 RJE Emulator permits Perkin-Elmer's computer systems to emulate IBM 2780 or 3780 Remote Job Entry terminals. RJE enables the user to access the computing facilities of a central host computer via common carrier facilities. Industry standard binary synchronous (BISYNC) line protocol is used for transfer between the two locations. The RJE site can be at any distance from the host, limited only by the availability of appropriate common carrier lines. The RJE Emulator operates in a device-independent manner using the facilities of the operating system. In addition to the 2780/3780 standard card reader and printer, the 2780/3780 RJE Emulator permits the use of both disk and tape devices.

HASP/32 permits Perkin-Elmer's systems to emulate the IBM HASP workstation by allowing users to submit batch jobs at a remote site for transmission over a binary synchronous (BISYNC) communication line. Batch jobs are processed by a central host computer, and results are returned to the originating remote site. HASP multileaving protocol provides for bidirectional data transmission, which enables significantly higher throughput than is possible with standard bisync protocol used by Remote Job Entry terminals such as the IBM 2780/3780. These terminals can transmit data in only one direction for the duration of a job. HASP/32 supports up to seven concurrent input/output streams, a console, and a binary synchronous communication line. Multileaved communication allows concurrent operation of all card readers and printers. HASP/32's capabilities are provided in a device-independent manner, using the facilities of OS/32, the operating system. HASP/32 permits the use of both disk and tape for job stream I/O devices.

The 3270 EMULATOR package enables Perkin-Elmer's 32-bit systems to emulate IBM 3270 components. The 3270 Emulator provides two distinct operating environments and interfaces, hardware emulation and virtual terminal emulation. The hardware emulation facilities permit Model 1200 or 1250 VDU's to access a remote process on an IBM mainframe and also allow a terminal operator to communicate with a remote data processing system over data links using IBM 3270 protocol. The Emulator provides control, data formatting, and data translation in such a manner as to emulate an IBM 3277 or 3275 both to the operator and to the remote process. The virtual terminal emulation facilities enable user-written applications to communicate with a remote data processing system over data links using IBM 3270 protocol. The virtual terminal emulation facilities behave logically as if the terminal were an IBM 3270 terminal.

3270 Support enables the IBM 3270 Information Display system family of control units and CRT's to be used with Perkin-Elmer's 32-bit systems. Users can form complex point-to-point or multipoint terminal networks using a Perkin-Elmer host computer. By using cluster controllers, the common carrier facilities of such networks can be made less expensive than the required facilities in a point-to-point network of ordinary terminals. Also, the synchronous communications protocol used by 3270 devices allows higher speed on common carrier facilities than the asynchronous protocol used by many terminals.

The ZDLC Channel Terminal Manager provides full link protocol support for bit-oriented protocols including IBM's SDLC, the International Standard Organization's HDLC, and the U.S.'s ADCCP. It provides both multidrop and point-to-point support; either primary (master/host) or secondary (slave) support; normal response mode, asynchronous response mode, or symmetrical control mode line disciplines; normal and extended addressing; normal and

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extended command encoding; and TWS (two-way simultaneous or full duplex) or TWA (two-way alternate or half duplex) line activity. When using the multidrop facility between two Perkin-Elmer 32-bit processors, one system may act as if it were the host to multiple secondaries while the other acts as if it were multiple secondaries. This permits the multiplexing of multiple virtual circuits over one physical link. Statistical options for the ZDLC Channel Terminal Manager permit the counting of all commands transmitted/received, data passed, or errors encountered on a communications line. Sysgen options permit the user to exclude all protocol options not required with his system and to identify what supported features each attached line will provide. Multidrop features include increased polling of more active terminals as well as user-specified balance of input/output on TWA (2-wire) lines. The ZDLC Channel Terminal Manager software package provides link protocol support which permits the building of various network facilities including IBM SNA, X.25, and other networks above the Channel Terminal Manager. However, it should be emphasized that the ZDLC Channel Terminal Manager software package does not itself include IBM SNA or X.25 support. The ZDLC Channel Terminal Manager product is a high-level tool which permits the data communications OEM or sophisticated end user to provide bit-oriented link protocols within a network; it is *not* a high-level network within itself.

UTILITIES: Five major OS utilities are available, OS Edit, OS AIDS, OS/32 Text, OS/32 Copy, and OS/32 Patch.

OS/32 Edit is a fairly flexible text editor for ASCII and/or binary characters that runs under OS/32. It is basically line-oriented, but it also has facilities for character and column manipulation. A string search and replacement capability is also provided. OS Edit can be used for interactive editing and batch-stream job editing, and it has file manipulation capabilities. Text is read into an edit buffer in memory that is at least 1K bytes in size; it can be made larger by operator request. OS Edit is included at no charge with each operating system.

OS/32 AIDS (Automatic Interactive Debugging System) has breakpoint, snapshot, and trace facilities, and also a memory call or register monitor feature. It operates in interactive or batch mode. It is included at no charge with each operating system.

OS/32 Text is a document preparation facility usable on all Perkin-Elmer 32-bit processors. Entry can be from a terminal or a keyboard printer. OS Text provides for the creation, maintenance, storage, and printing of documents and permits the documents to be modified, appended, updated, and merged. A FIND command can display every occurrence of a selected word or phrase. Existing text can be stored on disk or tape, and stored text (or files) can be assigned "private," "accessible to a defined group," or "open" levels of priority. Automatic page numbering and positioning, footnoting, placing titles at top or bottom of page, left or right justification, overprinting and underlining, correct hyphenation, and widow prevention (not carrying only one word or line to the next page) are included. Text 1 provides all the facilities of OS Text, while Text 2 is a subset which includes all capabilities except text entry and editing. OS Text operates as a segmented task under OS/32.

OS/32 Copy provides for the copying of any file.

OS/32 Patch facilitates the entry of program patches.

The OS library also includes OS/32 source updater, disk integrity check, disk initialize, disk pump, and disk compress routines.

APPLICATION PROGRAMS: Application programs for Perkin-Elmer systems are generally available through the Perkin-Elmer users' group, Interchange. Programs from Interchange are nominal in cost. For information, write Perkin-Elmer's headquarters. There are similar groups outside the U.S. as well.

In addition to the packages listed in the Software Price section, Perkin-Elmer offers about 52 diagnostic/test programs at $25 to $150 each. Also available are 6 software routines at $25 to $30 each, plus media costs of up to $75.

PRICING

POLICY: Perkin-Elmer offers its systems on a purchase-only basis, with customer service provided. Field installations are performed by Customer Service on a fixed-price basis. Since system configurations and customers' locations vary, rates are provided on a quotation basis only. Customer Service must be contacted for a formal quotation on all such installations. A minimum installation charge of $200.00 plus the travel charge is applicable. Installation consists of functional, operational testing and system performance as demonstrated by Perkin-Elmer's applicable test programs. This service must be ordered prior to shipment of the equipment. A full on-site service warranty applies for 90 days from installation date.

The Perkin-Elmer Customer Service Division is organized to provide comprehensive maintenance service. The field force is supported by a staff of service specialists at Perkin-Elmer's national headquarters in Neptune, New Jersey, and at support depots in Flanders, New Jersey, and Garden Grove, California. Customer engineers are located in major cities throughout the United States to provide service on a local level. Each service office is stocked with spare parts, tools, and special test equipment to facilitate repairs.

Maintenance service can be obtained: 1) on a contract basis, with fixed monthly charges to cover the normal business week up to and including 24 hours a day, seven days a week at most locations, 2) on a full-time, on-site basis, 3) via a depot and fixed-rate exchange service, which provides users with repairs and exchange parts at predetermined rates, or 4) on a per-request basis, which provides service at hourly rates.

Training is offered on both software and hardware topics in a number of courses. For information regarding course content, location, and pre-requisites, contact the Technical Training Center in Neptune, New Jersey, (201) 988-0400. Information regarding on-site training courses is also available. Software courses include Introduction to Assembly Language, OS/32 MT I/O Subsystems, ITAM/32, COBOL/ISAM, FORTRAN, OS/32 I/O Internals, and WCS. Hardware maintenance courses include Introduction to Computer Hardware, System Diagnosis/PM, 3220 Module Level, and a number of courses on peripheral maintenance.

Both hardware and software subscription services are offered by Perkin-Elmer at $200 per year. The hardware service entitles a Perkin-Elmer user to receive product improvement notices, general information bulletins, and preventive maintenance procedures. The software service brings a user regular software bulletins describing new Perkin-Elmer software, software defects, and the patches or alternatives associated with such defects. Revisions to previously purchased software are available at reduced rates.

Software is separately priced.

Quantity discounts of 10 to 38 percent are provided on Series 3200 systems in quantities up to 100 systems; additional discounts are available for larger orders.

EQUIPMENT: Details on the various Series 3200 packaged systems are provided in the equipment price list that follows.■

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.**
PROCESSORS			
M32-200	3220 Processor with 256K bytes of MOS ECC memory, memory management hardware, eight sets of 16 32-bit general registers, Loader Storage Unit, power fail/auto restart, Model 550 terminal, 2-line communications multiplexer, 20-minute battery back-up, 16-slot chassis, 50-amp power supply, cabinet with AC distribution panel, system control panel	$33,500	$300
M32-201	50-Hertz version of M32-200	33,500	*
M32-210	Same as M32-200 but with 512K bytes of memory	43,000	360
M32-211	50-Hertz version of M32-210	43,000	*
M32-220	Same as M32-200 but with 768K bytes of memory	51,000	420
M32-221	50-Hertz version of M32-220	51,000	*
M32-230	Same as M32-200 but with 1 million bytes of memory	59,000	480
M32-231	50-Hertz version of M32-230	59,000	*
M32-400	3241 Processor with 256K bytes of ECC MOS memory (one bank expandable to 2 megabytes), eight sets of 16 32-bit general registers, four levels of interrupts (will handle 1,023 I/O devices), power fail/auto restart, Loader Storage Unit, universal clock, OS/32 Boot Loader, 8K bytes of 4-way set associative cache memory, 256 segmentation registers, Model 550 terminal, 2-line communications multiplexer, 8-slot I/O chassis, power supply, and 56-inch cabinet with power distribution panel; capable of directly addressing 16 megabytes of memory	85,000	540
M32-401	3242 Processor; same as M32-400 but with 512K bytes of memory (two banks expandable to 2 megabytes) and two cabinets	97,000	660
M32-402	3244 Processor; same as M32-400 but with 1024 bytes of memory (four banks expandable to 8 megabytes) and three cabinets	137,000	880
SYSTEMS			
3241	systems with MOS ECC memory, 8 sets of 16 32-bit general registers, 4 levels of interrupts, up to 1,023 I/O devices, 8K bytes of 4-way associative cache memory, 256 segmentation registers, 8 DMA ports, power fail/auto restart, Loader Storage Unit with boot loader, universal clock, systems console with interface, 75-ips 800-bpi magnetic tape system, 80-megabyte disk system, 8-line communications multiplexer, floating point processor, 2K words of WCS, battery backup; capable of directly addressing 16 megabytes of memory		
M32-485	Basic 3241 system with 512K bytes of memory, 60 Hertz	139,500	840
M32-493	50-Hertz version of M32-485	139,500	*
M32-486	Same as M32-485 but with 800/1600-bpi dual density tape system in lieu of 800-bpi system	149,500	865
M32-494	50-Hertz version of M32-486	149,500	*
M32-487	Same as M32-485 but with 300-megabyte removable media disk system in lieu of 80-megabyte system	152,500	940
M32-495	50-Hertz version of M32-487	152,500	*
M32-488	Same as M32-485 but with 800/1600-bpi tape system (M32-486) and 300-megabyte disk system (M32-487)	162,500	965
M32-496	50-Hertz version of M32-488	162,000	*
3242 systems have all the features of 3241 systems but with 16 DMA ports instead of 8			
M32-481	Basic 3241 system with 1024K bytes of memory, 60 Hertz	160,000	1,020
M32-489	50-Hertz version of M32-481	160,000	*
M32-482	Same as M32-481 but with 800/1600-bpi dual density tape system in lieu of 800-bpi system	170,000	1,045
M32-490	50-Hertz version of M32-482	170,000	*
M32-483	Same as M32-481 but with 300-megabyte removable media disk system in lieu of 80-megabyte system	173,000	1,120
M32-491	50-Hertz version of M32-483	173,000	*
M32-484	Same as M32-481 but with 800/1600-bpi tape system (M32-482) and 300-megabyte disk system (M32-483)	183,000	1,145
M32-492	50-Hertz version of M32-484	183,000	*
MEMORY			
M32-000	256K-byte MOS ECC memory expansion (for any 3200 model)	8,000	60
M32-430	1024-byte MOS ECC memory expansion (factory installation only with purchase of 3240 CPU)	19,900	240
PROCESSOR OPTIONS FOR 3240			
M32-429	Memory expansion chassis with one 18-slot memory chassis (with cables) capable of housing four megabytes of memory	2,950	—
M32-404	Memory expansion unit to expand one or two banks to above two megabytes of memory and to four banks; includes cabinet, chassis, and power to expand up to eight megabytes	12,800	20
M32-405	Memory bank expansion from one to two banks or, in increments, to four banks; includes required interfaces and cables	4,500	20
M32-420	I/O expansion cabinet to house additional I/O chassis and peripherals; includes cabinetry, 150 amp power supply, blower system, power distribution panel	7,500	20
M32-421	DMA bus expansion; provides for an additional DMA bus; includes I/O chassis, DMA interface, terminators, and cables	4,500	20
M32-422	I/O expansion chassis; includes 8-slot I/O chassis capable of handling eight 15-inch or sixteen 7-inch controllers; includes I/O cables	1,150	—
M32-428	High-speed data handling; adds instructions to calculate cyclic and longitudinal redundancy checksums for communications applications	1,000	10
M32-010	3200 selector channel; high-speed data module provides direct memory access to up to 16 million bytes of main memory; data transfer rate is up to 10 million bytes per second; accommodates up to 16 device controllers (for any 3200 model)	1,500	10
M32-423	Floating-point processor; provides high-speed implementation of 48 single- and double-precision floating-point instructions	9,500	40
M32-424	2K words of 3240 WCS; includes development software on 800-bpi magnetic tape	7,500	20
M32-425	Same as M32-424 but with software on 1600-bpi magnetic tape	7,500	20
M32-426	Same as M32-424 but with software on 10-megabyte disk	7,800	20
M32-427	3240 battery backup; provides 160 megabyte-minutes of battery backup	2,500	10
M48-061	3240 clock module; includes programmable precision interval clock with frequency and interval count under hardware control; includes AC line frequency-derived clock	750	5

Dash (—) indicates charge is not applicable.
* Requires special Customer Service quotation.
**Single-shift maintenance; 2-shift rates are 50 percent higher, and 3-shift rates are 100 percent higher.

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.**
PROCESSOR OPTIONS FOR 3220			
M32-001	1K bytes for bipolar cache memory	2,000	5
M32-002	Error logger for memory	750	—
M32-003	2K words of 3220 WCS on 800-bpi tape	5,000	20
M32-008	2K words of 3220 WCS on 1600-bpi tape	5,000	20
M32-009	2K words of 3220 WCS on 10-megabyte disk	5,300	20
M32-004	Floating-point hardware	5,600	40
M32-005	High-speed data handling	1,000	10
M32-006	Extended battery back-up	1,000	10
M32-007	Bootloader	500	—
MULTIPORT MEMORIES			
	Prices are based on an order which includes two 32-bit CPU's with parity option and the necessary available slots for the interface. The components of a multiport memory system may be ordered separately as spare parts but are tested only in a minimum configuration. Field installation information and charges are by request only.		
	Testing charge for order which also includes one 32-bit CPU (in addition to installation charge)	1,000	—
	Testing charge without order for 32-bit CPU (in addition to installation charge)	1,500	—
M48-035	Single-bank, two-port, 64K-byte multiport memory system; includes two interface boards, a multiplexer, a controller, a chassis, a power supply, a power control panel, a high-density systems cabinet, and two 32K-byte, 750-nanosecond core memory boards with parity	17,500	255
M48-038	Contiguous dual-bank, two-port, 64K-byte Multiport Memory System; includes two interface boards, two multiplexers, two memory controllers, two chassis, two power supplies, a high-density systems cabinet, a power control panel, and two 32K-byte, 750-nanosecond core memory boards with parity	29,000	325
M48-040	Same as M48-035 but with 128K bytes of memory	49,500	585
M48-042	64K-byte Multiport Memory Expansion; includes a chassis, a power supply, and a 750-nanosecond core memory board with parity	10,900	130
M48-043	96K-byte Multiport Memory Expansion; includes a chassis, a power supply, and three 32K-byte, 750-nanosecond core memory boards with parity	14,900	190
M48-044	128K-byte Multiport Memory Expansion; includes a chassis, a power supply, and two 64K-byte, 750-nanosecond core memory boards with parity	19,500	250
M48-025	Multiport Memory Interface; includes 15-inch circuit board, power supply, and chassis	3,000	30
M48-026	Multiport Memory Controller; includes 15-inch circuit board, power supply, and chassis	4,500	40
M48-027	Multiport Memory Multiplexer; includes 15-inch circuit board	3,200	30
M48-056	Power Control Panel; 60 Hertz; for up to four banks of multiport memory	2,100	5
M48-057	50-Hertz version of M48-056	2,100	5
SYSTEMS MODULES			
M48-000	Universal Clock Module; includes a programmable precision interval clock with both frequency and interval count under hardware control and an AC line frequency-derived clock	750	5
M48-001	8-Line Interrupt Module; to interface customer interrupt lines to the built-in processor interrupt system	900	5
M48-002	General Purpose Interface Board, mounts up to 117 14- or 16-pin dual in-line package IC's for custom design	550	—
M48-012	Line Frequency-Derived Clock; automatic interrupt each 8.3 (60 Hertz) or 10 (50 Hertz) milliseconds	250	5
M48-013	Universal Logic Interface; mounts up to 77 14- or 16-pin dual in-line package IC's for custom design; includes fully buffered logic for 8- and 16-bit transfers on multiplexer bus or selector channel	700	—
M48-055	I/O Bus Switch	1,700	20
M48-018	Manual Control Panel for I/O Bus Switch; manual override control for up to six processors sharing a single common switched bus	200	—
M48-019	Manual Control Panel for I/O Bus Switch; manual override control for up to three separate common switched busses, each shared by two processors	200	—
M48-020	Extended DMA Logic Interface	650	0
MASS STORAGE			
M46-617	10-megabyte Fixed/Removable Cartridge Disk System; includes drive, controller for up to four drives, power supply, and disk cartridge	10,000	90
M46-618	50-Hertz version of M46-617	10,100	*
M46-657	Same as M46-617 plus 32-bit DMA	10,900	100
M46-658	50-Hertz version of M46-657	10,900	*
M46-663	Same as M46-657 plus second drive	17,900	160
M46-664	50-Hertz version of M46-663	17,900	*
M46-659	10-megabyte add-on Fixed/Removable Cartridge Disk Drive	7,000	60
M46-660	50-Hertz version of M46-659	7,000	*
M46-421	Cartridge Disk Drive Interface for up to four drives	4,800	30
27-056	IBM 5440-type 10-megabyte Disk Cartridge	270	—
M46-600	MSM 80 80-megabyte Removable Media Mass Storage Module System; includes a drive, controller, and interface for up to four drives, power supply, and disk pack	22,000	195
M46-602	50-Hertz version of M46-600	22,000	*
M46-681	MSM 80/32; same as M46-600 plus 32-bit DMA	23,000	205
M46-682	50-Hertz version of M46-681	23,000	*
M46-601	MSM 80E 80-megabyte add-on Removable Media Mass Storage Module Drive	18,000	145
M46-603	50-Hertz version of M46-601	18,000	*
M46-609	Formatted 80-megabyte, 5-platter disk pack	750	—
M46-604	MSM 300 300-megabyte Removable Media Mass Storage Module System; includes a drive, controller and interface for up to four drives, power supply, and disk pack	35,000	295
M46-606	50-Hertz version of M46-604	35,000	*
M46-677	MSM 300/32; same as M46-604 plus 32-bit DMA	36,000	305
M46-678	50-Hertz version of M46-677	36,000	*
M46-605	MSM 300E 300-megabyte add-on Removable Media Mass Storage Module Drive	32,750	225
M46-007	50-Hertz version of M46-605	32,750	*
M46-610	Formatted 300-megabyte, 12-platter disk pack	1,700	—
M46-630	FMD-1 System; single drive, diskette system	2,900	29

Dash (—) indicates charge is not applicable.
* Requires special Customer Service quotation.
**Single-shift maintenance; 2-shift rates are 50 percent higher, and 3-shift rates are 100 percent higher.

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.**
MASS STORAGE (Continued)			
M46-636	50-Hertz version of M46-630	2,900	*
M46-631	Same as M46-630 plus second drive	3,900	39
M46-637	50-Hertz version of M46-631	3,900	*
M46-634	Second drive for M46-630	1,000	10
M46-640	50-Hertz version of M46-634	1,000	*
M46-635	Third drive for M46-630, -631	2,400	24
M46-641	Third drive for M46-635, -637	2,400	*
M46-643	Fourth drive for M46-630, -631	1,000	10
M46-644	Fourth drive for M46-636, -637	1,000	*
M46-642	FMD-1 Diskette, package of 10	120	—
MAGNETIC TAPE EQUIPMENT			
M46-400	Intertape Cassette System; includes dual transports and interface/controller	4,200	40
M46-490	9-track, 800-bpi, 75-ips Magnetic Tape System; includes master drive and controller for up to four drives; 60 Hertz	9,100	115
M46-492	50-Hertz version of M46-490	9,100	*
M46-494	9-track, 800/1600-bpi, 75-ips Magnetic Tape System; includes master drive, NRZI/PE formatter, and controller for up to four drives; 60 Hertz	19,100	140
M46-496	50-Hertz version of M46-494	19,100	*
M46-534	Same as M46-490 plus 32-bit DMA; 115V	10,000	125
M46-535	230V version of M46-534	10,100	*
M46-538	Same as M46-494 plus 32-bit DMA; 115V	20,000	150
M46-539	230V version of M46-538	20,100	*
M46-491	Add-on drive for M46-490, -534	8,425	90
M46-493	Add-on drive for M46-492, -535	8,425	*
M46-495	Add-on drive for M46-494, -538	9,625	*
M46-497	Add-on drive for M46-496, -539	9,625	*
M46-526	9-track, 800-bpi, 45-ips Magnetic Tape System; includes master drive, NRZI formatter, controller for up to four drives, and 32-bit DMA; 115V	8,000	100
M46-527	230V version of M46-526	8,100	*
M46-530	9-track, 1600-bpi, 45-ips Magnetic Tape System; includes master drive, PE formatter, controller for up to four drives, and 32-bit DMA; 115V	10,000	110
M46-531	230V version of M46-530	10,100	*
M46-501	Add-on drive for M46-526	5,300	70
M46-502	Add-on drive for M46-527	5,300	*
M46-515	Add-on drive for M46-530	5,900	80
M46-516	Add-on drive for M46-531	6,000	*
M46-500	Interface/Controller for up to four 9-track, 800-bpi, 45-ips drives	2,500	20
PRINTERS			
M46-221	Serial printer; 132 positions, 64-character set, 120 cps; 115V, 60 Hertz	3,500	45
M46-222	230V, 50-Hertz version of M46-221	3,500	*
M46-223	Same as M46-221 but 180 cps	5,500	55
M46-224	230V, 50-Hertz version of M46-223	5,500	*
M46-233	Interface/Controller for M46-221 thru -224	800	10
M46-227	U.K. Character Set for M46-221 thru -224	100	—
M46-229	French Character Set for M46-221 thru -224	100	—
M46-230	German Character Set for M46-221 thru -224	100	—
M46-232	Printer ribbons, case of 12	60	—
M46-300	Line printer; 132 positions, 64- or 96-character set, 300 lpm; 90-132 VAC, 60 Hertz; includes controller	9,000	105
M46-301	50-Hertz version of M46-300	9,000	*
M46-302	180-250 VAC, 60-Hertz version of M46-300	9,000	105
M46-303	50-Hertz version of M46-302	9,000	*
M46-312	USASCII 64-character set for 300-lpm printers	750	—
M46-313	USASCII 96-character set for 300-lpm printers	750	—
M46-314	U.K. 96-character set for 300-lpm printers	750	—
M46-316	German 96-character set for 300 lpm printers	750	—
M46-304	600-lpm version of M46-300	13,000	125
M46-305	600-lpm version of M46-301	13,000	*
M46-306	600-lpm version of M46-302	13,000	125
M46-307	600-lpm version of M46-303	13,000	*
M46-319	USASCII 64-character set for 600-lpm printers	750	—
M46-320	USASCII 96-character set for 600-lpm printers	750	—
M46-321	U.K. 96-character set for 600-lpm printers	750	—
M46-323	German 96-character set for 600-lpm printers	750	—
M46-309	Pedestal and paper shelf for line printers	500	—
M46-310	Acoustical package for line printers	1,000	—
M46-311	Ribbons for line printers	80	—
PUNCHED CARD EQUIPMENT			
M46-238	Reader; 400 cpm	4,000	40
M46-239	50-Hertz version of M46-238	4,100	*
M46-236	Reader; 1,000 cpm	8,000	80
M46-237	50-Hertz version of M46-236	8,100	*
M46-235	Interface/Controller for card readers	990	10
PUNCHED TAPE EQUIPMENT			
M46-240	Reader; unidirectional, 300 cps	1,300	20
M46-241	50-Hertz version of M46-240	1,400	*
M46-242	Reader/Punch; 300/75 cps	3,300	40
M46-243	50-Hertz version of M46-242	3,400	*
M46-250	Interface/Controller for punched tape equipment	900	10

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.**
TERMINALS			
M46-064	Carousel 300 Keyboard Printer Terminal; 132 positions, 64-character set, 30 cps	3,205	40
M46-065	50-Hertz version of M46-064	3,312	*
M46-810	Cable Connection to PASLA	60	—
M46-811	Cable Connection to Bell 103 modem	60	—
M46-860	Pin-Feed Adjustable Tractor	150	—
M48-024	20-ma Current Loop Interface	400	5
M46-041	1200 Alphanumeric Display Terminal; 1920 characters, editing facilities	2,322	24
M46-042	50-Hertz version of M46-041	2,394	*
M46-046	Same as M46-041 but with function keyset	2,435	24
M46-048	50-Hertz version of M46-046	2,507	*
M46-044	Printer Port, RS-232C	131	—
M46-045	Printer Port, 20-ma current	164	—
M46-050	Line Drawing Set	106	—
M46-066	650 Thermal printer for M46-041 thru -048; 115 VAC, 50/60 Hertz	1,327	14
M46-067	230 VAC, 50/60-Hertz power option for M46-066	50	—
M46-068	100 VAC, 50/60-Hertz version of M46-066	1,377	*
M46-110	550 VDU; 115 VAC, 60 Hertz, 1920-character screen	1,096	16
M46-111	Same as M46-110 but with printer port	1,170	16
M46-112	230 VAC, 50/60-Hertz version of M46-111	1,250	*
M46-113	115 VAC, 50/60-Hertz version of M46-111	1,250	*
M46-114	110 VAC, 50/60-Hertz version of M46-111	1,250	*
M46-115	20-ma Current Loop Interface	80	—
M46-116	French Character Set for M46-110 thru -114	75	—
M46-117	Swedish Character Set for M46-110 thru -114	75	—
M46-118	Danish Character Set for M46-110 thru -114	75	—
M46-119	German Character Set for M46-110 thru -114	75	—
M46-120	U.K. Character Set for M46-110 thru -114	75	—
M46-080	655 Thermal printer for M46-111 thru -114; 115 VAC, 50/60 Hertz	1,327	14
M46-081	230 VAC, 50/60-Hertz power option for M46-080	50	—
M46-082	100 VAC, 50/60-Hertz version of M46-080	1,377	*
M46-071	French Character Set for thermal printer	75	—
M46-072	Swedish Character Set for thermal printer	75	—
M46-073	Danish Character Set for thermal printer	75	—
M46-074	German Character Set for thermal printer	75	—
M46-075	U.K. Character Set for thermal printer	75	—
M46-070	Thermal Printer Paper	69	—
COMMUNICATIONS EQUIPMENT			
M47-014	Direct Memory Access I/O Subsystem (asynchronous protocols)	6,000	—
M47-015	Direct Memory access I/O Subsystem (asynchronous, character-synchronous, and bit-oriented protocols)	7,500	—
	Maintenance charges for M47-014 and M47-015 are not yet available.		
M47-000	Adapter for Bell 201-type data sets, synchronous	1,200	10
M47-001	Adapter for Bell 301-type data sets, synchronous	1,400	10
M47-106	Single line synchronous adapter	1,200	10
M47-107	M47-106 with zero-bit insertion/deletion and support for SDLC	1,500	10
M47-002	QUAD synchronous adapter (QSA)	1,600	30
M47-003	M47-002 with zero-bit insertion/deletion and support for SDLC	2,600	40
M47-004	Line Conditioning Module with interface for QSA and two CCITT modems	700	20
M47-005	Line Conditioning Module with interface for QSA and four RS-232C communications lines	400	10
M47-102	Programmable Asynchronous Single Line (PASLA) adapter (103/202 data sets of RS-232)	500	10
M47-100	Asynchronous Line Module Controller (for M47-101)	500	10
M47-101	Programmable Asynchronous Line Module (4 lines)	1,200	10
M49-021	Chassis for M47-101	550	—
M47-104	2-line Communication Multiplexer	700	15
M47-105	8-line Communication Multiplexer	2,000	30
M10-022	Automatic Dial Unit Controller (4 lines)	1,600	10
M47-202	Single-Address System, 360/370 Parallel Interface	5,000	100
M47-203	Multiple-Address System, 360/370 Parallel Interface	6,500	100
CABINETS & CHASSIS			
M49-020	System Expansion Chassis, prewired for up to eight 15-inch or sixteen 7-inch controllers without power; includes chassis signal cables	700	—
M49-040	System Cabinet; includes side skins, chassis support rails, exhaust fan and filter, filler panels or half door, casters, levelers, and I/O panel; sold and assembled only at Perkin-Elmer's plant for the housing of Perkin-Elmer systems	925	—
M49-107	56-inch Cabinet; beige, w/out power	1,100	—
M49-041	24-amp AC Distribution Panel; for 115V 50/60 Hertz 1 phase power; included with M49-040, -107	150	—
M49-042	48-amp AC Distribution Panel; for 115/230V 50/60 Hertz 2 phase power; included with M49-040, -107	200	—
M49-043	25-amp AC Distribution Panel; for 230V 50 Hertz 1 phase power; included with M49-040, -107	150	—
M49-044	15-amp AC Distribution Panel; for 230V 50 Hertz, 3 phase power; included with M49-040, -107	200	—
M49-051	50-amp MOS power supply; 115 VAC 50/60 Hertz, +5, +12 VDC	1,600	15
M49-052	50-amp MOS power supply; 230 VAC 50/60 Hertz, +5, +12 VDC	1,600	15
M49-053	50-amp MOS expansion power supply; 115 VAC 50/60 Hertz, +5 VDC	1,500	15
M49-054	50-amp MOS expansion power supply; 230 VAC 50/60 Hertz, +5 VDC	1,500	15
M49-003	10- to 15-inch Adapter Card	150	—

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.**
MAINTENANCE EQUIPMENT			
M49-411	3220 Test Aid	1,450	—
M49-402	IBM 360/370 Interface Maintenance Panel; includes isolation for assurance of Perkin-Elmer interface operation	500	—
28-009	PALS Test Connector	40	—
28-014	PASLA Test Cable	40	—
28-017	Conversion Equipment Test Simulator	1,500	—
M49-031	Half Board Kit	70	—

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**Single-shift maintenance; 2-shift rates are 50 percent higher, and 3-shift rates are 100 percent higher.

SOFTWARE PRICES

		Purchase Price
OS/32 Multitask Operating System		
S90-016-99	Documentation Package	$ 100
S90-016-31	On 9-track, 800-bpi tape	5,000*
S90-016-71	On 9-track, 1600-bpi tape	5,000*
S90-016-61	On 10-megabyte disk	5,600*
S90-016-91	Source listing	800

*Purchase price includes installation and one-year subscription to Software Subscriber's Service. Re-orders of this software for use at same location are at price reduction of $2,500. Re-order price does not include installation.

OS/32 Multi-Terminal Monitor—OS/32 MTM		
S90-017-99	Documentation Package	100
S90-017-31	On 9-track, 800-bpi tape	2,500*
S90-017-71	On 9-track, 1600-bpi tape	2,500*
S90-017-61	On 10-megabyte disk	2,800*
29-591	MTM Terminal User's Reference Manual	10

*Purchase price includes installation but not travel expenses. Re-orders of this software for use at same location are at price reduction of $500 without installation.

Telecommunications Access Method—ITAM/32		
S90-008-99	Documentation Package	50
S90-008-31	On 9-track, 800-bpi tape	2,500
S90-008-71	On 9-track, 1600-bpi tape	2,500
S90-008-61	On 10-megabyte disk	2,800
S90-008-91	Source listing	800
FORTRAN VII		
S90-216-99	Documentation Package	250
S90-216-31	On 9-track, 1600-bpi tape	5,000*
S90-216-71	On 9-track, 1600-bpi tape	5,000*
S90-216-61	On 10-megabyte disk	5,300*
S90-026-31	Development Package; 9-track, 800-bpi tape	2,500*
S90-026-71	Development Package; 9-track, 1600-bpi tape	2,500*
S90-026-61	Development Package; 10-megabyte disk	2,800*
S90-027-31	Optimizer only; 9-track, 800-bpi tape	4,000*
S90-027-71	Optimizer only; 9-track, 1600-bpi tape	4,000*
S90-027-61	Optimizer only; 10-megabyte disk	4,300*

*License required. Quantities for determining discounts can be any combination of media. Price includes one year of maintenance.

BASIC Level II		
S90-208-99	Documentation Package	25
S90-208-39	Source only; 800-bpi tape	2,000
S90-208-79	Source only; 1600-bpi tape	2,000
S90-208-69	Source only; 10-megabyte disk	2,000
S90-210-31	Double-precision floating-point; 800-bpi tape	400
S90-210-71	Double-precision floating-point; 1600-bpi tape	400
S90-210-61	Double-precision floating-point; 10-megabyte disk	450
S90-210-91	Double-precision floating-point; 32-bit source listing	200
S90-211-31	Single-precision floating-point; 800-bpi tape	400
S90-211-71	Single-precision floating-point; 1600-bpi tape	400
S90-211-61	Single-precision floating-point; 10-megabyte disk	450
S90-211-91	Single-precision floating-point; 32-bit source listing	200
Common Assembler Language (CAL)		
S90-204-99	Documentation Package	25
S90-204-31	Object; 9-track, 800-bpi tape	150
S90-204-71	Object; 9-track; 1600-bpi tape	150
S90-204-61	Object; 10-megabyte disk	450
S90-204-39	Source; 9-track, 800-bpi tape	1,000
S90-204-79	Source; 9-track, 1600-bpi tape	1,000
S90-205-99	CAL MACRO Documentation Package	25
S90-205-31	CAL MACRO; 9-track, 800-bpi tape	450
S90-205-71	CAL MACRO; 9-track, 1600-bpi tape	450
S90-205-61	CAL MACRO; 10-megabyte disk	750

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SOFTWARE PRICES

		Purchase Price
COBOL		
S90-217-99	Documentation Package	30
S90-217-31	On 9-track, 800-bpi tape	7,000*
S90-271-31	On 9-track, 1000-bpi tape	7,000*
S90-217-61	On 10-megabyte disk	7,000*
*License required. Quantities for determining discounts can be any combination of media.		
RPG II		
S80-024-BCM	Documentation Package	75
S80-024-ABB	On 9-track, 800-bpi tape	2,500*
S80-024-ABC	On 9-track, 1600-bpi tape	2,500*
S80-024-ABE	On 10-megabyte disk	2,800*
S80-024-CAA	Right-of-copy	250
*License required.		
RELIANCE		
S80-025-BCM	Documentation Package	200
S80-025-ABB	On 9-track, 800-bpi tape	12,500*
S80-025-ABC	On 9-track, 1600-bpi tape	12,500*
S80-025-ABE	On 10-megabyte disk	12,800*
S80-025-CAA	Right-of-copy	1,250
*License required.		
SORT/MERGE II		
S90-408-99	Documentation Package	25
S90-408-31	On 9-track, 800-bpi tape	1,000
S90-408-71	On 9-track, 1600-bpi tape	1,000
S90-408-61	On 10-megabyte disk	1,300
WCS Development Package		
S90-406-99	Documentation Package	50
S90-406-31	On 800-bpi tape	500
S90-406-71	On 1600-bpi tape	500
S90-406-61	On 10-megabyte disk	500
Loader Storage Unit Support Program		
S90-403-99	Documentation Package	10
S90-403-11	32-bit object on paper tape	50
Transaction Controller (ITC)		
S90-018-99	Documentation Package	25
S90-018-31	On 9-track, 800-bpi tape	6,500*
S90-018-71	On 9-track, 1600-bpi tape	6,500*
S90-018-61	On 10-megabyte disk	6,500*
*License required. Quantities for determining discounts can be any combination of media.		
Data Management (DMS/32)		
S80-022-BCM	Documentation Packages	100
S80-022-ABB	On 9-track, 800-bpi tape	6,000*
S80-022-ABC	On 9-track, 1600-bpi tape	6,000*
S80-022-ABE	On 10-megabyte disk	6,300*
S80-022-CAA	Right-of-copy	600
*License required.		
OS/32 TEXT		
S90-020-99	Documentation Package	35
S90-020-31	On 9-track, 800-bpi tape	1,000*
S90-020-71	On 9-track, 1600-bpi tape	1,000*
S90-020-61	On 10-megabyte disk	1,300*
29-677	User Guide	30
*License required. Quantities for determining discounts can be any combination of media.		
HASP/32		
S90-015-99	Documentation Package	25
S90-015-31	Object; on 9-track, 800-bpi tape	1,750
S90-015-71	Object; on 9-track, 1600-bpi tape	1,750
S90-015-61	Object; on 10-megabyte disk	1,970