Olivetti Computers OH 5500 Series

MANAGEMENT SUMMARY

Four months after creating a new company in September 1979 to market IBM plug-compatible mainframes, Olivetti Computers S.p.A. announced a second series of PCM's which will be manufactured by Hitachi of Japan. In order to distinguish them from the OC 5300 series manufactured by IPL, Olivetti has designated the series with the initials OH in front of the number: OH 5500.

With the OH 5500 models, Olivetti Computers entered the large-scale IBM-compatible mainframe market with three computers targeted at the middle and upper end of IBM's 303X series.

Olivetti's goal is to be a supplier of equipment covering the entire market for office automation and information management systems. Olivetti Computers provides, as an integral part of these PCM products, both system support and maintenance services by highly qualified technicians with long experience in data processing.

Based on the Hitachi M180, the Olivetti models are the OH 5520, OH 5530 and OH 5545. They are similar, although not exactly the same, as National Advanced Systems' 7000 family, also manufactured by Hitachi.

The basic OH 5520, a 2-megabyte, 7-channel processor expandable to 16 megabytes, offers 1.8 to 2.2 times the throughput of the IBM 3031.

The larger OH 5530, a system offering approximately 1.2 times the throughput of the IBM 3032, can be ordered as a 4-megabyte, 8-channel basic processor and can be expanded to 16 channels and 16 megabytes.

The OH 5545, a dual processor complex with throughput superior to the IBM 3033, is a high-availability processor which can be ordered as a 4-megabyte, 8-channel system expandable to 16 channels and 16 megabytes.

CPU power in terms of millions of instructions per second (MIPS) is 2.2 for the OH 5520, 3.2 for the OH 5530, and 5.2 for the OH 5545.

All models have a CPU cycle time of 72 nanoseconds and a memory cycle time of 360 nanoseconds for an 8-byte fetch.

All models have one input output processor as standard. A second I/O processor is optional. Each I/O processor can handle two byte multiplexer channels and up to six block multiplexer channels.

The two input/output processors on the OH 5545 may be attached to both processors and have the capability ➢

Olivetti's OH 5500 series of IBM plug-compatible systems are available in three models, all manufactured by Hitachi.

MODELS: OH 5520, OH 5530, and OH 5545.

CONFIGURATIONS: 2M to 16M bytes of memory; 1 or 2 byte multiplexer channels and six block multiplexer channels; the OH 5545 is a dual processor system.

COMPETITION: IBM's 3032 and 3033 and equivalent plug-compatible systems.

CHARACTERISTICS

SUPPLIER: Olivetti Computers S.p.A., Via del Giorgioni 63, 00147 Rome, Italy. Telephone (06) 38779. Telex 610662.

MANUFACTURER: Hitachi Ltd., 5-1, Marunouchi, 1-chome, Chiyoda-ku, Tokyo 100, Japan.

Olivetti Computers is a wholly owned subsidiary of Ing. C. Olivetti and C. S.p.A., Italy's largest data processing and office automation equipment manufacturer. Olivetti also has associated companies in Austria, the United Kingdom, Germany, Spain, Denmark, Belgium, France, Holland, Norway, Portugal and Switzerland as well as in several countries in North and South America, Asia, Australia, and Africa.

MODELS: OH 5520, OH 5530, and OH 5545.

DATA FORMATS

BASIC UNIT: 8-bit byte. Each byte can represent 1 alphanumeric character, 2 BCD digits or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word."

FIXED POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode: 1 halfword (16 bits) or 1 word (32 bits) in binary mode.

FLOATING-POINT OPERANDS: 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short" format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; or 4 words in "extended precision" format.

INSTRUCTIONS: 2, 4 or 6 bytes in length, specifying 0, 1, or 2 memory addresses, respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: Metal oxide semiconductor (MOS).

CAPACITY: OH 5520, 2 megabytes to 16 megabytes; OH 5530, 4 megabytes to 16 megabytes; OH 5545, 4 megabytes to 16 megabytes.

CYCLE TIME: 360 nanoseconds for an 8-byte fetch. ➢

Olivetti Computers OH 5500 Series

CHARACTERISTICS OF THE OH 5500 SERIES

SYSTEM CHARACTERISTICS	OH 5520	OH 5530	OH 5545
Primary IBM target	3031 AP	3032	3033
Date of introduction	January 1980	January 1980	January 1980
Number of processors	1	1	2
Principle operating systems	OS/VS1, SVS, MVS, VM/370	OS/VS1, SVS, MVS, VM/370	MVS, VM/370
Upgradable to	OH 5530	OH 5545	
MAIN STORAGE			
Type	16K RAM	16K RAM	16K RAM
Cycle time, nanoseconds	360	360	360
Minimum capacity, bytes	2 million	4 million	4 million
Maximum capacity, bytes	16 million	16 million	16 million
Bytes fetched per cycle	8	8	8
BUFFER STORAGE			
Cycle time, nanoseconds	144	144	144
Bytes fetched per cycle	8	8	8
Capacity, bytes	16K	64K	2x64K
CONTROL STORAGE			
Type	1K ECL bipolar	1K ECL bipolar	1K ECL bipolar
Access time nanoseconds	32	32	32
Word size	99 bits	99 bits	99 bits
Minimum capacity, words	6K	6K	6K
Maximum capacity, words	12K	12K	12K
PROCESSOR FEATURES			
Clock comparator and CPU timer	Standard	Standard	Standard
Direct control	Standard	Standard	Standard
Dynamic address translation	Standard	Standard	Standard
Floating point	Standard	Standard	Standard
Extended precision floating point	Standard	Standard	Standard
High speed arithmetic	—	Standard	Standard
Channel-to-channel adapter	Standard	Standard	Standard
Service processor	Standard	Standard	Standard
Light pen	Standard	Standard	Standard
Two-byte feature	—	Optional	Optional
Alternate console	—	Optional	Optional
CHANNELS			
Input/output processors			
Standard	1	1	1
Optional	1	1	1
Input/output channels/IOP			
Byte multiplexer	1-2	1-2	1-2
Block multiplexer	6	6	6
Channel Data Rate			
Byte multiplexer	100KB/sec.	100KB/sec.	100KB/sec.
Block multiplexer	1.86 MB/sec.	1.86 MB/sec.	1.8 MB/sec.
Aggregate one IOP	10MB/sec.	10MB/sec.	10MB/sec.
Aggregate two IOP's	—	16MB/sec.	16MB/sec.

to switch from one central processor to the other in case one processor goes down.

The maximum channel data rate is 1.86 megabytes per second for the block multiplexer, 100K bytes per second for the byte multiplexer. The aggregate maximum is 10 megabytes per second for one input/output processor and 16 megabytes per second for two.

Large-scale integrated (LSI) semiconductor circuits are used extensively throughout the system, resulting in increased processing speeds, higher reliability, and reduced space and cooling requirements. The central processor

CHECKING: Error checking and correction (ECC) circuitry in main memory performs automatic correction of all single-bit errors and detection of all double-bit and most other multiple-bit memory errors.

A reconfiguration capability is standard. In the event of an unrecoverable error, or any other problem with a memory module, the operator can "dial out" the problem module (one-half million or one million bytes) and reconfigure the remaining memory for continuous operation.

STORAGE PROTECTION: A Store and Fetch Protection feature, which guards against inadvertent overwriting and/or unauthorized reading of data in specified 2048-byte blocks of storage, is standard on all models.

Olivetti Computers OH 5500 Series

uses an LSI version of bipolar emitter-coupled logic (ECL) with very fast chip speeds.

Main memory in the OH 5500 uses metal oxide semiconductor (MOS) LSI circuits and has a cycle time of 360 nanoseconds, while ultra-high-speed bipolar components are used in the cache memory. Cache loading from main memory is performed in 32-byte blocks. Using the maximum (four-way) main storage interleaving capabilities, a maximum data transfer rate of one 32-byte "line" per 144 nanoseconds can be achieved between main memory and the high-speed cache memory.

Among the standard features are error checking and correcting code (ECC), program event recording, byte alignment, storage protection, instruction retry, clock comparator, CPU timer, interval timer, time of day clock, high-speed arithmetic (except on the OH 5520), extended precision floating-point, direct control, and channel-to-channel adapter. Other features include a service processor, a light pen and printer adapter for the video console, and System/370 extended facility and virtual machine assist. As an option on all models, an alternate console can be attached and the two-byte interface feature can be added to each input/output processor.

Expandability is the key to the OH 5500 series. To meet future data processing needs, an OH 5520 can be upgraded to the OH 5530 and OH 5545. This gives the user a growth path of up to 250 percent in performance.

COMPETITIVE POSITION

Although price obviously plays a role in an acquisition decision, the most essential ingredient to a successful relationship between vendor and customer is the service and technical support the vendor can provide.

Olivetti Computers has prepared itself for this role by setting up a network of trained technicians in Italy.

Outside of Italy, Olivetti faces stronger competition from the other European vendors such as Siemens of Germany, who now has its own PCM, CII-HB of France, with its new DPS 8 range, and ICL of the UK, with its large-scale 2900 Series models. Olivetti also will find stronger competition from the American-owned vendors in Europe such as Honeywell, Univac, Burroughs, NAS, and Amdahl.

But Olivetti, whose expertise is in distributed processing and office systems, has associated companies throughout the world and therefore has a ready-made marketing and after-sales infrastructure.

Specifically, the main competition to the OH 5520 is from IBM itself with either the 3031 AP or the 3032, from NAS's AS 7000N, and from the Siemens System 7.870. All are aimed at the customers who have already invested in IBM software.

CENTRAL PROCESSORS

At present there are three models. The processing power is shown below, in terms of millions of instructions per second (MIPS) and relative performance (the IBM 370/158-3 = 45).

MODEL	MIPS	RELATIVE PERFORMANCE
OH 5520	2.2	102
OH 5530	3.2	145
OH 5545	5.2	240

The largest available model, the OH 5545, uses dual processor technology, where all the features are doubled. The input/output processors may be attached to either central processor and switched to the other if one of the central processors goes down.

INDEX REGISTERS: Sixteen 32-bit general registers, used for indexing, base addressing, and as accumulators, plus four 64-bit floating-point registers per processor.

INSTRUCTION REPERTOIRE: The OH 5500 instruction set consists of the complete System/370 Univeral Instruction Set, including the five instructions for Dynamic Address Translation.

INSTRUCTION TIMES: Olivetti Computers states that individual instructions times are not currently available, but that the average execution times for the systems will equal or exceed the performance of the comparable System/370 processors.

OPERATIONAL MODES: Like the System/370, the OH 5500 computers can operate in either the Basic Control (BC) mode or Extended Control (EC) mode. The BC mode maintains general upward compatibility with the System/360 architecture and programming. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other system control functions; therefore, the virtual-storage-oriented operating systems must be used.

PROCESSOR FEATURES: The timing features of the System/370 architecture are included in the OH 5500 central processors. These include a CPU timer and a clock comparator; the latter provides a means of causing an interrupt when the standard time of day clock reaches a program-specified value. Additional instructions are provided to set and store the time of day clock, clock comparator and CPU timer.

The standard direct control feature provides six external interrupt lines which operate independently of the normal data channels, plus the Read Direct and Write Direct instructions which provide for single-byte data transfers between an external device and main storage.

The Floating-Point Arithmetic feature provides instructions to perform floating-point arithmetic operations on both short (1-word) and long (2-word) operands.

The extended precision arithmetic feature handles floating point operands of 28 hexidecimal digits. These operands can be rounded to long precision format, the long precision format operands can be rounded to short precision format.

The high speed arithmetic (HSA) feature provides significant increases in performance for multiplication and division operations.

The high speed multiply (HSM) works on MR, M, MH, MXR, MDR, MD, MXDR, MXD, MER, and ME, and

Olivetti Computers OH 5500 Series

The OH 5530 competes against IBM's 3032 and 3033S, Amdahl's 470 V5-2, and NAS's AS 7000. The OH 5545 with its dual processor competes with the IBM 3033N, Amdahl's 470, V6-2. NAS's AS/7000 DPC, and Siemens' 7.872.

BACKGROUND

This is not Olivetti's first go at the mainframe market. In 1959, Olivetti designed and produced the first Italian mainframe, the ELEA. In 1964, this activity was incorporated into a new company, Olivetti General Electric, in which GE (U.S.) had a 75 percent holding. In 1968, Olivetti withdrew from this company to concentrate on the design and production of small data processing systems and terminals.

Olivetti Computers S.p.A. is an associated company, completely owned by Ing. C. Olivetti and C. S.p.A., Italy's largest computer company, which employs over 59,000 people worldwide, and has 28 manufacturing and assembly plants throughout the world.□

performs a 16-bit multiply in a simultaneous shifter for each two bytes, adding the results in a loop adder. For floating point, the exponent adjustment is performed simultaneously and stored in a spill adder; the end result is obtained by combining the contents of the loop adder and the spill adder in a parallel adder.

High speed divide (HSD) works on DDR, DD, DER, DE and functions on a principle of quadratic convergence by exploiting HSM instead of successive subtractions.

The channel-to-channel adapter permits direct communication between OH 5500 processors or with a System/370 via a standard I/O channel. It can be attached to either a selector channel or a block multiplexer channel and uses one control unit position on either channel. Either system can be equipped with the channel-to-channel adapter, and it is required on only one of the interconnected channels.

The instruction retry feature analyzes errors and attempts recovery by retrying the failed instruction, if possible. If a retry is unsuccessful, it attempts to correct the malfunction or to isolate the affected task.

The virtual machine assist feature provides an assist to VM/370 firmware emulation of certain privileged operations.

CACHE MEMORY: All models have a high speed cache memory situated between main memory and the central processor. Its function is to buffer instructions and data prior to processing. The cache is made up of 1K ECL bipolar RAM chips. Cycle time is 144 nanoseconds for an 8-byte fetch.

The size of the cache memory for each model is as follows:

OH 5520	**16K bytes**
OH 5530	**64K bytes**
OH 5545	**2x64K bytes**

CONTROL MEMORY: On all models, the control memory stores microprograms for controlling the CPU, for maintenance operations, and for diagnostics. Separate control memories are provided for channel control and console control microcode.

Like the cache memory, the storage is composed of 1K ECL bipolar RAM chips. Access time is 32 nanoseconds. Word size is 99 bits. Minimum and maximum size is 6K and 12K words, respectively.

SERVICE PROCESSOR: This separately powered subsystem is made up of an Intel 8080 microprocessor, main memory, and a floppy disk, and connects either directly to the CPU via a special interface or via one of the I/O processors.

All maintenance procedures and diagnostic routines are carried out by the service processor, which is also responsible for editing error information, producing messages in clear text and supporting error recovery when a malfunctioning component can no longer perform this task. An integral part of the service processor is the program event recording (PER) feature which assists the debugging of programs by detecting and recording program events.

INPUT/OUTPUT CONTROL

All models have one microprogrammed input/output processor (IOP) and a second as an option. Each IOP has a 4K-byte control store and may have up to six block multiplexer channels and up to two byte multiplexer channels.

Maximum channel data rates are as follows:

Block Multiplexer	**1.86 megabytes/second**
Byte Multiplexer	**100K bytes/second**
Aggregate	**10 megabytes/second for one IOP**
	16 megabytes/second for two IOPs

PERIPHERAL EQUIPMENT

The OH 5500 family can utilize all IBM System/360 and 370 input/output and mass storage devices as well as their plug-compatible counterparts from independent vendors.

SOFTWARE

Olivetti Computers supports the following IBM operating systems: OS/VS1, SVS, MVS, and VM/ 370.

PRICING

At the time of writing the report, prices were not available.■