Honeywell Bull DPS 7 Series

ARCHIVE EDITION

CHARACTERISTICS

UPDATE: *The Honeywell Bull DPS 7 Series of medium-scale mainframes can only be obtained from the vendor on an as-available basis. The DPS 7, manufactured in France by Groupe Bull, has been replaced by the new DPS 7000 Series. For your convenience, Datapro is republishing here the DPS 7 Characteristics section and the last DPS 7 hardware price list. For information and full pricing on Honeywell Bull peripherals and GCOS 7 software, please refer to the DPS 7000 report on Page 70C-458ME-101 under this tab.*

MANUFACTURER: Honeywell Bull Inc., 300 Concord Road, Billerica, Massachusetts 01821. Telephone (617) 895-6000.

MODELS: DPS 7/40E, 7/55E, and 7/65E.

DATA FORMATS

BASIC UNIT: 8-bit byte plus one parity bit. The data paths are four bytes (32 bits) wide. Data can be interpreted as binary, decimal, hexadecimal, or alphanumeric.

FIXED-POINT OPERANDS: Data bits are interpreted in groups of four (packed or unpacked decimal data) or eight (alphanumeric EBCDIC), or in strings of between 16 and 64 (binary digits). The strings can be interpreted as signed for fixed-point binary numbers.

FLOATING-POINT OPERANDS: Data can be represented as floating-point operands with single- (16-bit) or double- (32-bit) precision formats.

INSTRUCTIONS: The DPS 7 instruction repertoire consists of 221 instructions, including operations for address computations, and arithmetic instructions for performing fixed- and floating-point decimal and binary operations on packed or unpacked data. Operands can be binary, fixed- or floating-point, or decimal in packed or unpacked format; bytes; byte strings; or bit strings. In addition, the microcode can include the Series 200/2000 "Program Mode" option, and execute the Series 200/2000 instruction set.

INTERNAL CODE: EBCDIC.

MAIN STORAGE

Memory is organized into consecutively numbered byte locations. Four-byte blocks are always accessed regardless of operand size. Half-word (16-bit) operands must begin on even-numbered byte locations, and full-word (32-bit) and double-word (64-bit) operands must begin on byte locations divisible by four.

STORAGE TYPE: 64K-bit or 256K-bit MOS chips. Current Mode Logic (CML), a fast, low-power, low-heat technology, is used. CML has a propagation time of one nanosecond per logic port. In addition, the DPS 7 uses a multilayer micropackaging technique that allows 10,000 to 15,000 functions per board.

CAPACITY: See Table 1.

CYCLE TIME: See Table 1.

The Honeywell DPS 7 Series medium-size systems have been designed primarily to serve as either host processors or remote satellite processors in a distributed processing environment. These systems offer a growth path for Level 62 and Level 64 users, and a hardware/software platform for Honeywell's Manufacturing System (HMS 7).

MODELS: DPS 7/40E, 7/55E, and 7/65E.
CONFIGURATION: From 2 to 8MB of memory and from 2 to 8 I/O channels.
COMPETITION: Burroughs B 3900 and Burroughs V Series; IBM System/38 and 4300 Series; NCR V-8500 Series; and Sperry System 80.
PRICE: Purchase prices range from $89,000 to $160,000.

CHECKING: Each item of data stored in memory units and in control store is accompanied by a Hamming code (seven bits for every four data bytes) which permits the correction of single-bit errors and the detection of double-bit errors. Data paths, and particularly, the bus perform parity checks to ensure data integrity. All registers and calculation circuits include a key check.

RESERVED STORAGE: The DPS 7 protects every segment individually with an automatic system of rings and protection levels. This protection system, implemented by hardware and firmware, protects segments on the basis of the information they contain rather than their physical location.

The main processor, while executing a process, may be at one of four levels of privilege, called "rings." Rings are numbered from zero to three, with zero being the most privileged. A ring number is allocated to each segment when it is created and, when the process is entered, the main processor adopts this ring number. Each segment is allocated three protection levels, one for each possible use: read, write, or execute. Each level can be anywhere within the range of zero to three. At every reference to an address in a segment, the protection level for the relevant type of use is checked against the current ring number of the main processor. Access is only allowed under the following conditions: for read and write access, the ring number is less than or equal to the protection level; for execute access, the ring number is within the range between the write and execute protection levels. At linking time, the programmer specifies protection levels; this feature controls access to process segments from other active programs.

CENTRAL PROCESSORS

The three DPS 7 processor complexes are microprogrammed units built around a multiprocessor configuration involving the CPU, peripheral processors, and network processor. The work load is distributed among these three elements to provide simultaneous processing and data transfer. Current mode logic (CML) technology is used extensively in CPU and input/output controller logic circuits and is said to provide faster gate speeds and less power consumption than comparable emitter-coupled logic (ECL) or transistor-transistor logic (TTL) circuits.

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TABLE 1. SYSTEM COMPARISON

MODEL	DPS 7/40E	DPS 7/55E	DPS 7/65E
SYSTEM CHARACTERISTICS			
Date announced	March 1986	November 1983	November 1983
Date first delivered	April 1986	January 1984	January 1984
Field upgradable to	7/55E, 65E	7/65E	—
Relative performance	1.00	1.58	2.34
Number of processors	1	1	1
Cycle time, nanoseconds	360	240	140
Word size, bits	32	32	32
Operating systems	GCOS 7, GCOS 64	GCOS 7, GCOS 64	GCOS 7, GCOS 64
MAIN MEMORY			
Type	64K-bit or 256K-bit MOS	64K-bit or 256K-bit MOS	64K-bit or 256K-bit MOS
Minimum capacity, bytes	2M	2M	2M
Maximum capacity, bytes	6M	8M	8M
Increment size, increment	1 or 2MB	1 or 2MB	1 or 2MB
Cycle time, nanoseconds	355 read, 290 write	355 read, 290 write	355 read, 290 write
BUFFER STORAGE			
Minimum capacity	Not applicable	Not applicable	Not applicable
Maximum capacity	Not applicable	Not applicable	Not applicable
Increment size	—	—	—
INPUT/OUTPUT CONTROL			
Number of channels:			
Byte multiplexer	0	0	0
Block multiplexer	0	0	0
Word	0	0	0
Other	2-4	4-6	4-8

A dash (—) indicates the category is not applicable.

DPS 7 central processors are in turn composed of seven subunits, a control store, and a high-speed processor bus. This processing "system" is connected to the central bus, which also services main memory and the input/output processors. Peripheral devices are connected to the I/O processors, which have their own control stores and main memories, which in turn are connected to the CPU via high-speed channels. This distributed architecture enables various subsystems to operate simultaneously without tying up the main processor.

The seven components in the CPU include:

- Pilot Machine (PIM): The PIM retrieves microinstruction sequences from the control store and routes them to the appropriate subunits. Microprograms are composed of two or more 32-bit words, each protected by four parity bits.
- Address Calculation Machine (ACM): The ACM handles all address translations, includes the base registers and an associative memory that stores up to eight segment addresses, and also handles data protection by checking rings under GCOS.
- Data and Instruction Management Machine (DIM): The DIM provides the interface between the main memory and the other processor units and includes a 32-byte look-ahead feature that allows it to begin interpreting another instruction while a previous instruction is still being executed.
- Arithmetic and Logic Machine (ALM): The ALM includes the data registers and executes fixed-point, decimal, and logic operations.
- Scientific Calculation Machine (SCM): The SCM executes floating-point operations.
- Timer: Using the main clock as a reference, the timer transmits a master frequency along the processor bus and also provides various types of information, such as real-time, elapsed time, and process time.
- Maintenance Interface Machine (MIM): The MIM provides the interface between the main processor and the service processor for system initialization and testing.

SPECIAL FEATURES: *Control Store* contains firmware held in 32-bit words. Each word contains up to five instructions to be executed by the seven subunits during a single cycle. The sequencing of firmware instructions is controlled by the pilot machine. Up to five microinstructions can be executed simultaneously by the subunits.

The control store of the main processor is implemented in firmware and normally contains 12K words (but can have up to 24K words) enabling the execution of the Series 200/2000 instruction set.

Firmware is also used in the DPS 7 to perform functions traditionally performed by software. These include task management, procedure calls, and data protection.

The main processor is capable of recognizing and controlling a task, a unit of a program more significant than a single instruction. A task is a sequence of interdependent instructions. A program can comprise a number of tasks, each able to execute in parallel with the others (multitasking). This parallel execution of tasks requires a dispatching mechanism. On traditional machines, this mechanism required software intervention. On the DPS 7, it is a built-in firmware function of the main processor.

The DPS 7 uses firmware-controlled semaphores to interpret external events such as physical input/output termination, peripheral interrupts, operator interrupts, and messages from terminals. Using semaphores, it also synchronizes the execution of competing processes, passes messages between processes, and controls competing demands for system services.

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		Purch. Price ($)	Monthly Maint. ($)	Monthly Charges 1-Year Lease ($)	3-Year Lease ($)	5-Year Lease ($)
PROCESSOR OPTIONS						
CMM4701	One-megabyte Memory Module	10,000	26	559	518	458
CMM4721	Two-megabyte Memory Module for DPS 7/E processors with four megabytes or six megabytes	15,000	52	843	783	692
CMM4947	Two-megabyte Memory Module for expansion from two megabytes to four megabytes	15,000	52	802	652	552
CPF4712	Peripheral Expansion Cabinet	13,808	47	516	482	429
CPF4713	H200/2000 Program Mode for CPS4940/CPS4957/CPS4967; includes cabinet	16,606	28	348	323	287
CPF4707	I/O Channel Expansion; for more than four channels	5,200	5	181	167	148
CPF4710	Two I/O Channels	9,200	4	290	270	236
CSF4104	Hard copy printer (120 cps); required peripheral	4,100	70	364	343	310
CSF4102	Pedestal for CSF4104; low for sitting	200	NA	NA	NA	NA
CSF4103	Pedestal for CSF4104; high for standing	200	NA	NA	NA	NA
PROCESSOR UPGRADES						
CPK4982	7/45E to 7/55E; minimum two megabytes C.P. memory is required	23,850	128	2,059	1,910	1,687
CPK4983	7/55E to 7/65E	40,000	198	2,010	1,871	1,661
CPK4987	7/35E to 7/55E; minimum two megabytes C.P. memory and two I/O channels are required	48,810	126	2,956	2,738	2,416
CPK4988	7/35E to 7/65E; minimum two megabytes C.P. memory and two I/O channels are required	81,335	324	4,966	4,609	4,077
CPK4989	7/45E to 7/65E; minimum two megabytes C.P. memory is required	64,395	326	4,069	3,781	3,348
CPK4991	7/40E to 7/55E; requires two I/O channels	31,000	150	1,240	1,022	877
CPK4992	7/40E to 7/65E; requires two I/O channels	61,800	348	3,438	2,820	2,408

NA—Not available. ■