Honeywell Bull DPS 88 Series

CHARACTERISTICS

UPDATE: ***Launched in 1982, the DPS 88 Series grew to rival the top-end models of the IBM 3090 product line. In 1985, however, Honeywell superseded the DPS 88 line with its considerably more powerful DPS 90 Series. Invigorated by its merger with Groupe Bull of France and NEC Corp. of Japan, Honeywell has since announced an even higher level of processing power in its DPS 9000 Series.***

Late in its life cycle, the DPS 88 Series received major revamping by Honeywell, with six new processors replacing the previous six DPS 88 products. The later DPS 88 versions featured larger main memory capacities, 256K-bit memory chips, new DATANET communications gear, the GCOS 8 Performance Enhancement Facility, and bundling of formerly optional software products—including the Rapid Access Data System (RADS), a facility for improving I/O throughput.

For your convenience, Datapro is republishing here the DPS 88 CHARACTERISTICS section and the last DPS 88 hardware price list. For information and full pricing on Honeywell Bull peripherals and GCOS 8 software, please refer to the DPS 90 report on Page 70C-458LT-801 under this tab.

MANUFACTURER: Honeywell Bull Inc., Deer Valley Computer Park, 13430 North Black Canyon Highway, Phoenix, Arizona 85029. Telephone (602) 862-8000.

MODELS: DPS 88/861, DPS 88/862, DPS 88/862T, DPS 88/891 and DPS 88/892, DPS 88/892T.

DATA FORMATS

BASIC UNIT: Nine-bit bytes organized functionally to process thirty-six-bit (word) groupings of information. Special features are also included for ease in manipulating 4-bit groups; 6-bit, 9-bit, and 18-bit groups; and 72-bit double-precision groups.

FIXED-POINT OPERANDS: Binary fixed-point numbers are represented with 18-bit half word, 36-bit single word, and 72-bit double-precision operands.

Decimal numbers used directly in hardware arithmetic commands are expressed as decimal digits in either the four-bit or nine-bit character format. They are expressed as unsigned numbers or as signed numbers using a separate sign character.

Alphanumeric data is represented by nine-bit, six-bit, or four-bit characters. A machine word contains either four, six, or eight characters, respectively.

FLOATING-POINT OPERANDS: There are two floating-point formats—binary and hexadecimal. Binary floating-point numbers are represented with 36-bit single-word and 72-bit double-word precision. In both operands, 0 represents the sign of the exponent, bits 1 to 7 the exponent, and bit 8 the sign of the fraction. The rest of the operand starting with bit 9 represents the rest of the fraction. Hexadecimal has an exponent of 16. The reason for two floating-point formats is to expand the exponent range of the floating-point operand.

No longer actively marketed, the Honeywell Bull DPS 88 is a large-scale processor line positioned between the DPS 8 medium- through large-scale processor line and the DPS 90.
MODELS: DPS 88/861, DPS 88/862, DPS 88/862T, DPS 88/891, DPS 88/892, and DPS 88/892T.
CONFIGURATION: One or two Central Processing Units (CPUs), 32 to 128 megabytes of main memory, 1 or 2 I/O processors, and 64 to 256 logical I/O channels.
COMPETITION: Amdahl 580 Series, CDC Cyber 180, IBM 3090 Series, NAS AS/9000 Series, Unisys B 7900 and 1100/90 Series.
PRICE: From $1,740,000 to $4,510,000.

INSTRUCTIONS: All basic instructions use one 36-bit word. The processor performs operations using 6-, 9-, 18-, 36-, and 72-bit operands. All single-word instructions use bits 0 through 17 for the address field, bits 18 through 27 for the op code, bit 28 as the interrupt inhibit bit, bit 29 as the address register bit, and bits 30 through 35 as the instruction address modifier. Multiword instructions use bits 0 through 17 for various functions as required, bits 18 through 27 as the op code, bit 28 as the interrupt inhibit bit, and bits 29 through 36 as the operand descriptor 1 modification field. Words 2, 3, and 4 contain the operand descriptor or indirect pointer for operands 1, 2, and 3, respectively.

INTERNAL CODE: Nine-bit ASCII code is standard.

MAIN MEMORY

The Main Memory Unit (MMU) on Honeywell processors uses memory interlacing techniques to allow simultaneous access to memory boards. This improves access time and enhances performance. Board groups are contained in memory arrays, each with its own power supply to insure availability. An MMU can contain up to two arrays.

STORAGE TYPE: Metallic oxide semiconductor (MOS).

CAPACITY: See Table 1.

CYCLE TIME: Information not supplied by vendor.

CHECKING: An 8-bit error-correcting Hamming code is appended to each 72-bit word pair. Single-bit errors are corrected automatically, and multiple-bit errors are detected and flagged for subsequent error recovery routines. Odd parity is utilized throughout the processor.

RESERVE STORAGE: Memory contains segment descriptors, a page table, and an associative memory. Segment descriptors indicate which working space a segment resides in, the size and base address of the segment, and

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access privileges allowed to the segment. The page table describes the physical location of each page of a working space. The associative memory is a kind of cache memory that provides fast access to page addresses. To implement storage protection, the DPS 88 uses read, write, and execute permission bits in the Segment Descriptor. The Page Table Word (PTW) contains a write permit bit. Hardware also checks that data addresses generated during program execution do not exceed specified boundaries.

CENTRAL PROCESSORS

The DPS 88 Central System hardware consists of 11 components:

- Central Processing Unit (CPU)
- Central Interface Unit (CIU)
- Main Memory Unit (MMU)
- Input/Output Processor (IOP)
- Channel Bus Unit (CBU)
- System Support Facility (SSF)
- System Support Unit (SSU)
- Thermal Exchange Pump (TEP)
- Thermal Exchange Air (TEA)
- Central System Console
- Maintenance Console

All processing is performed by the Central Processing Unit, with the Central Interface Unit supervising the transfer of information between the CPU, the Main Memory Unit, and the Input/Output Processor.

The Input/Output Processor coupled with the Channel Bus Unit (CBU), supplies the interface between the network or peripheral subsystems and a Central Interface Unit.

The System Support Facility is a freestanding, dedicated maintenance processor that performs diagnostic functions and supports resource management. The System Consoles and Maintenance Consoles are connected to and controlled by the SSF. System Consoles may also be connected to Front-end Network Processors (FNPs).

The architecture employed in the DPS 88 CPU is a five-stage execution pipeline design augmented by a pipeline instruction prefetch stage and a pipeline instruction wrap-up phase. The design increases the system performance by allowing as many as five instructions to be in process simultaneously.

The DPS 88/890 Series processors use two separate high-speed cache memories, the instruction cache (I-cache) and the operand cache (O-cache), each providing 32K bytes of storage. The I-cache stores blocks of unmodified instructions and indirect words, while the O-cache stores blocks of operands and modified instructions, and modified indirect words. By using cache memory in this manner, the instructions and data are effectively separated, and all store operations are directed to the O-cache, thereby reducing main memory traffic. The DPS 88/860 Series models, unlike the DPS 88/890 Series models, use a single high-speed cache memory providing 32K bytes of storage rather than two separate caches. The single cache stores both instructions and operands.

DPS 88 Systems also include:

- An instruction unit that queues instructions and performs a five-step instruction preparation and execution process. Each stage of the pipeline operates concurrently to decode instructions and generate memory addresses.
- Five specialized execution units that are designed to optimize actual execution. The central execution unit handles the execution of most of the Transfer Control instructions and other instructions that alter the processor states, and maintains the address registers and performs housekeeping functions. The basic operations unit performs binary fixed-point operations, Boolean operations, fixed-point comparisons, register loads, and shift operations. The virtual memory and security unit performs most instructions unique to virtual memory management. The binary floating-point unit (for multiply and divide) executes fixed-point multiply and divide instructions and all binary floating-point or hexadecimal floating-point instructions. The decimal and character unit executes those instructions involving decimal arithmetic and character manipulation.

The Central Interface Unit (CIU) acts as a traffic controller for information passing between the CPU, MMU, and IOP. The CIU, as all other Central System components, comes with an independent power supply that helps enhance system availability. CIU functions are:

- Bringing the Central System to an orderly halt when a critical error is detected.
- Supporting communications between Central System units through connect, interrupt, and similar steering procedures.
- Resolving memory access conflicts between system components.
- Directing all accesses to memory by the Central Processing Unit and the Input/Output Processor.
- Switching all control signals, addresses, and data into and out of main memory.
- Providing the control tasks for main memory, including error detection and correction (EDAC) to help minimize data errors.
- Supporting system start-up and restart through reconfiguration tasks.
- Initiating memory refresh cycles.

The Input/Output Processor (IOP), acting in conjunction with the Channel Bus Unit (CBU), handles the data transfers between main memory and communications lines, peripheral devices, and the System Support Facility with transfer rates up to 48 million bytes per second. The IOP is designed to:

- Accommodate the Input/Output data transfer demands involved in systems that run numerous programs concurrently (multiprogramming) and that operate more than one processor at a time (multiprocessing).
- Provide the high disk access rates needed in data base-oriented systems.
- Serve the heavy transaction processing needs of large organizations.

The CPU does not handle input or output directly; it is responsible for obtaining control segments (portions of a

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TABLE 1. SYSTEM COMPARISON

MODEL	DPS 88/861	DPS 88/862	DSP 88/862T	DPS 88/891	DPS 88/892	DPS 88/892T
SYSTEM CHARACTERISTICS						
Date announced	September 1986	September 1986	September 1986	September 1986	September 1986	September 1986
Date first delivered	Fourth-Quarter 1986	Fourth-Quarter 1986	Fourth-Quarter 1986	Fourth-Quarter 1986	Fourth-Quarter 1986	Fourth-Quarter 1986
Field upgradable to	DPS 88/862 or DPS 88/891	DPS 88/862T or DPS 88/892	DPS 88/892T	DPS 88/892	NA	NA
Relative performance	Not specified	Not specified	Not specified	Not specified	Not specified	Not specified
Number of processors	1	2	2	1	2	2
Cycle time, nanoseconds	Not specified	Not specified	Not specified	Not specified	Not specified	Not specified
Word size, bits	36	36	36	36	36	36
Operating systems	GCOS 8	GCOS 8	GCOS 8	GCOS 8	GCOS 8	GCOS 8
MAIN MEMORY						
Type	256K-bit MOS	256K-bit MOS	256K-bit MOS	256K-bit MOS	256K-bit MOS	256K-bit MOS
Minimum capacity, bytes	32M	32M	64M	32M	32M	64M
Maximum capacity, bytes	64M	128M	128M	64M	128M	128M
Increment size	16MB	16MB	16MB	16MB	16MB	16MB
Cycle time, nanoseconds	Not specified	Not specified	Not specified	Not specified	Not specified	Not specified
BUFFER STORAGE						
Minimum capacity	32KB	64KB	64KB	64KB	128KB	128KB
Maximum capacity	32KB	64KB	64KB	64KB	128KB	128KB
Increment size	NA	NA	NA	NA	NA	NA
INPUT/OUTPUT CONTROL						
Number of channels:						
Byte multiplexer	NA	NA	NA	NA	NA	NA
Block multiplexer	NA	NA	NA	NA	NA	NA
Word	NA	NA	NA	NA	NA	NA
Other	64-128	64-128	128-256	64-128	64-128	128-256

NA—Not applicable.

program) that describe the I/O operations to be performed, storing them in a memory mailbox area for the Input/Output Processor, and issuing a channel connect command to initiate processing by the IOP. Once initiated, the IOP and the CBU handle the Input/Output operations independently of central processing. Consequently, by off-loading this Input/Output traffic from the CPU, the IOP helps reduce system overhead and increases the number of actual transactions processed. A basic IOP has 64 logical channels and can be expanded to 128 logical channels.

The Channel Bus Unit (CBU) is a sophisticated high-speed unit with data throughput rates over 20 megabytes per second. The CBU can contain two channel buses (paths over which data is transmitted) for connections to the IOP. The CBU supports the connection of the I/O subsystems that comply with the Federal Information Processing Standard (FIPS). The CBU has an expansion option that doubles the channel capacity. All channel types allow multiple logical channels to be assigned to one physical channel.

The System Support Facility (SSF) is a small standalone computer that logically connects to all Central System components. Acting as the system monitor, the SSF initializes the system, checks processing and hardware operation, and diagnoses malfunctions on-line. The SSF supports the central system resource sharing and the protection mechanisms between the operating system and the functional test system. On the software side, the SSF performs the following functions:

- Initializes the Central System.
- Initializes blocks of memory in the Main Memory Unit for use by the operating system or test software.
- Loads control stores for each CPU.
- Loads and maintains hyperpage tables in the CPUs and IOXs to control memory isolation for the operating system or test software, and to provide contiguous memory addressing.
- Communicates with the CPU concerning shared processor utilization.
- Initializes CPU information on the I/O channels allocated to the operating system, using configuration information provided by the system administrator.
- Cooperates in system restart following a shutdown.
- Responds to Central System alarms and coordinates instruction retry.

The SSF hardware consists of a mainframe with a control panel and peripherals. The mainframe includes a Central Processing Unit, 512K words of EDAC-protected MOS memory, and several interface units:

- A mass controller, providing microprogrammed support of two removable media drives.
- A multiple-device controller, providing microprocessor control of the SSF flexible disk drive.
- A specialized interface, allowing direct access to DPS 88 system components via a logic interface within the system support unit.
- A multiline communications processor, permitting microprocessor control of system consoles and alternate remote Technical Assistance Center (TAC) interconnection path.
- A maintenance interface, supporting the maintenance console, the SSF itself, an optional hard copy audit trail, and the TAC connection through a customer-supplied modem.

The SSF peripherals include:

- An integrated diskette unit primarily used for saving files.

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- Two high-speed, random-access digital data storage devices, providing main mass storage for the SSF. The storage capacity of each device is 67 megabytes, formatted.

- Up to six system consoles per SSF.

The System Support Unit (SSU) is attached to the CPU and helps the SSF monitor performance and maintain service. Acting as a liaison between the SSF and all other Central System components, the SSU makes possible initialization and testing of circuitry, examination of hardware for alarm conditions, and collection of power and cooling information. The SSU provides the power-entry controls for the Central System power supply and houses the system clock.

The Thermal Exchange Pump (TEP) circulates liquid coolant to each DPS 88 component that incorporates CML circuitry, and dissipates the heat through four closed cooling loops into the customer's chilled water system. This system allows for lower, more controlled operating temperatures.

If the user cannot provide a chilled water supply, the TEP passes the heat to optional Thermal Exchange Air (TEA) units, which dissipate it into the room air.

The System Consoles (CSU8801 and CSU8802) are modular, freestanding keyboard/display units. Both models offer features to help simplify system interaction and increase processing throughput. The CSU8801 can be configured as the second, fourth, and sixth system console per SSF, while the CSU8802 can be configured as the third and fifth system console per SSF. Both system consoles offer the DPS 88 operators the following capabilities:

- On-line recall of recent messages.

- Off-line retrieval of older messages.

- Optional hard copy messages.

The DPS 88 uses virtual memory which provides the processor with a directly addressable virtual space of 2^{43} bytes. It also includes the capability of translating the virtual address to a real memory address. Two different addressing modes are provided: absolute and paging. In the absolute addressing mode, a virtual address is generated, but is not mapped to a real address. The paging mode maps the virtual memory address to a real memory address.

The DPS 88 processor models have a comprehensive instruction set for performing data movement, binary arithmetic, shifting, logic, and control operations. The instruction set includes arithmetic facilities for performing variable-length, fixed- and floating-point decimal arithmetic, and bit and byte string manipulation for processing bytes, BCD characters, packed decimal data, and bit strings.

The DPS 88's basic instruction set contains more than 300 instructions and exceeds the instruction complement of the DPS 8 which is more than 280 instructions.

The central processor has three modes of operation: master mode, privileged master mode, and slave mode. The privileged master mode permits unrestricted access to all memory, permits the initiation of data transfer operations through the Input/Output Processor, and the setting of control registers. Master mode allows access to certain authorized portions of memory, while the slave mode is utilized by the operating system, when appropriate, and for execution of all user programs. These modes provide operating control and security in a multiprogramming environment.

SPECIAL FEATURES: The DPS 88 line features fully redundant configurations to maintain fault tolerance within organizations running critical applications. The fully redundant DPS 88/862T and DPS 88/892T come with two of each Central System component.

PHYSICAL SPECIFICATIONS: DPS 88 systems must be located in a room with a raised floor or any arrangement providing at least 12 inches of space beneath the equipment. The room ceiling must be eight feet above the floor. Power requirements must meet these specifications: 208, 240, 440, or 480 V-AC ±10 percent for the motor-generator set; 60 Hz nominal frequency ±0.5 Hz; three-phase with a maximum phase variation of 5 percent from the nominal; and 120/208 V-AC, five-wire cable with ground for peripheral equipment (voltage variation is ±10 percent).

A design temperature between 68 and 78 degrees Fahrenheit with a relative humidity between 40 and 60 percent noncondensing is permissible, although a temperature of 73 degrees with a relative humidity of 50 percent is recommended. Once a temperature and relative humidity are selected, the temperature should not fluctuate more than ±2 degrees Fahrenheit or the relative humidity more than ±5 percent.

CONFIGURATION RULES

The DPS 88 family consists of six models: the DPS 88/861, DPS 88/862, DPS 88/862T, DPS 88/891, DPS 88/892, and the DPS 88/892T. The DPS 88/861 Central System includes a Central Processing Unit (CPU); a System Support Unit (SSU); a Central Interface Unit (CIU); a Main Memory Unit (MMU) with 32 megabytes of memory; an Input/Output Processor (IOP) with 64 logical channels; a Channel Bus Unit (CBU); a System Support Facility (SSF); a system console and table with pod; a maintenance console and table; a Thermal Exchange Pump (TEP); and Thermal Exchange Air (TEA), an option used when a source of chilled water is not available to the TEA.

The DPS 88/862 central processing system includes two CPUs; two SSUs; two TEPs; one CIU; one MMU with 32 megabytes of memory; one IOP with 64 logical channels; one CBU; one SSF; one system console and table with pod; one maintenance console and table; and optional TEA.

The basic DPS 88/891 Central System includes a CPU, a CIU, an MMU with 32 megabytes of main memory, an IOP with 64 logical channels, a CBU, an SSF, a maintenance console and table, a system console with table and pod, an SSU, a TEP, and optional TEA unit.

The DPS 88/892 includes two CPUs, two SSUs, two TEPs, one CIU, one MMU with 32 megabytes of memory, one IOP with 64 logical channels, one CBU, one SSF, one system console and table with pod, one maintenance console and table, and optional TEA.

The DPS 88/862T and the DPS 88/892T are fully redundant systems containing two of each Central System component. These systems also include a minimum 64 megabytes of main memory.

The basic system can be expanded to 64 megabytes of memory in 16-megabyte increments. Processors configured with two MMUs can be expanded from a minimum 64 megabytes to 128 megabytes. The IOP can be expanded from 64 to 128 logical channels. Systems configured with

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two IOPs can have up to 256 logical channels. A CBU can be expanded to twice its basic channel capacity. Up to two CBUs can be attached to each IOP. Up to six system consoles can be configured with each SSF, and additional system consoles may be attached to a network processor. In all, the DPS 88 system can support up to 16 system consoles, of which 15 can be connected via the network processors. All processor models within the DPS 88 Series can be field upgraded to a larger system as processing needs increase.

INPUT/OUTPUT CONTROL

The DPS 88 supports most peripherals that are used on the DPS 8 system. The following types of peripheral devices can be logically connected to the DPS 88:

- Front-end Network Processors (FNPs)
- Terminals
- Peripheral Processors
- Disk and Tape Units
- Card Readers and Punches
- On-line and Off-line Printers

DPS 88 peripheral subsystems communicate with the central system through the CBU and the IOP. FNPs connect to the CBU directly via individual channels. Mass storage, tape, and unit record devices are linked to the channel by way of peripheral processors. Up to two interfaces (buses) connect each CBU with the IOP for access from peripheral subsystems. Each CBU can transfer data at a rate of up to 24 million bytes per second.

MASS STORAGE

Please refer to "Honeywell Bull DPS 8000 Series" or "Honeywell Bull DPS 90 Series" (Report 70C-458LT-801) for the latest information about mass storage services.

INPUT/OUTPUT UNITS

Please refer to the DPS 8000 or DPS 90 report for the latest information about Input/Output units.

TERMINALS

As part of a DPS 88 system, users may select a unit record subsystem consisting of the URP0600 unit record processor and up to eight unit record devices. These devices can include card readers, a card punch, a reader/punch, and printers. Multiple unit record subsystems can be configured. The URP0600 unit record processor is a freestanding, microprogrammed controller that connects the Channel Bus Unit (CBU) to the unit record devices. Microcoded programs directing the URP0600 help to maximize the overall use of the peripheral devices and decrease costly turnaround. The URP8400/1/2 are embedded unit record processors for the CBU. Each URP can control up to two card or printer devices.

COMMUNICATIONS

For details on DATANET 8, please see Report 70C-458LT-801, on the DPS 90 Series, under this tab.

SOFTWARE

For details on the GCOS 8 operating system, please see Report 70C-458LT-801, on the DPS 90 Series, under this tab.

PRICING AND SUPPORT

For your convenience, Datapro has listed the latest published retail prices in addition to lease and maintenance charges for DPS 88 hardware. Please refer to the DPS 90 report for information on Honeywell Bull maintenance services, GCOS 8 charges, and software support information.

EQUIPMENT PRICES

		Purch. Price ($)	Monthly Maint. ($)	1-Year Lease ($)	4-Year Lease ($)	Soft. Support ($)
PROCESSORS						
CPS8867	DPS 88/861 Central Processor System with 32MB Memory	1,740,000	3,600	82,400	64,750	1,221
CPS8868	DPS 88/862 Central Processor System with 32MB Memory	2,775,000	4,320	131,400	103,250	1,738
CPS8869	DPS 88/862T Fully Redundant Processing System with 64MB Memory	3,475,000	5,760	164,800	129,500	1,738
CPS8891	DPS 88/891 Central Processor System with 32MB Memory	2,675,000	5,355	116,500	91,200	1,419
CPS8892	DPS 88/892 Central Processor System with 32MB Memory	3,810,000	6,345	179,500	141,100	2,057
CPS8893	DPS 88/892T Fully Redundant Central Processing System with 64MB Memory	4,510,000	7,785	218,400	172,800	2,057
SYSTEM UPGRADES						
CPK8841	CPS8867 (DPS 88/861) to CPS8868 (DPS 88/862)	1,035,000	720	49,000	38,500	517
CPK8842	CPS8868 (DPS 88/862) to CPS8892 (DPS 88/892) or CPS8869 (DPS 88/862T) to CPS8893 (DPS 88/892T)	1,035,000	2,025	48,100	37,850	319
CPK8843	CPS8867 (DPS 88/861) to CPS8891 (DPS 88/891)	935,000	1,755	34,100	26,450	198
CPK8884	CPS8891 (DPS 88/891) to CPS8892 (DPS 88/892)	1,135,000	990	63,000	49,900	638
PROCESSOR OPTIONS						
MXC8800	Additional CIU and MMU for CPS8868 and CPS8892; no memory included	282,000	450	12,000	10,000	NA
CMM8816	Additional 16MB Memory Module	245,000	585	13,900	11,100	NA

NA—Not applicable.

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		Purch. Price ($)	Monthly Maint. ($)	1-Year Lease ($)	4-Year Lease ($)	Soft. Support ($)
MXU8801	Additional IOP with 64 Logical Channels and Channel Bus Unit (CBU); for CPS8868 and CPS8892	250,000	450	10,000	8,100	NA
MXF8804	IOP Logical Channel Expansion (64 to 128). Max. of one per IOP	6,000	NA	240	200	NA
MXF8805	Additional Channel Bus Unit (CBU); max. of one per IOP	188,000	135	5,400	4,300	NA
MXF8811	CBU Expansion	94,000	86	4,000	3,300	NA
CPF8802	Additional System Support Facility (SSF) for CPS8842 and CPS8885 only. Includes system console with large-screen monitor interface, 15" CRT and keyboard, Console Table and Control Pod, Maintenance Console, 12" CRT and Keyboard, Table, and two Modem switches	75,000	135	3,000	2,500	NA
	Consoles and Features:					
CSU8801	Additional System Console with 15" CRT and Keyboard for 2nd, 4th, and 6th System Console per SSF	3,095	36	130	110	NA
CSU8802	Additional System Console with 15" CRT and Keyboard for 3rd and 5th System Console per SSF	4,095	42	166	140	NA
CSF8803	Large Screen Monitor Interface Feature for CSU8801/8802	400	NA	16	13	NA
CSF8804	System Console Table for CSU8801/8802	550	NA	NA	NA	NA
CSF8801	Printer for System Console; 100 cps	1,225	50	121	103	NA
CSF8802	Printer for Maintenance Console; 100 cps	1,225	33	105	90	NA
CSF8805	23" Large Screen Monitor	2,358	16	157	135	NA
CSF8806	Ceiling Mount for CSF8805	195	NA	NA	NA	NA
CSF8301	Printer Pedestal for CSF8801/8802	395	NA	NA	NA	NA
	Power and Cooling:					
MGS8801	Motor Generator and Control; 3-sec. ridethrough, 62.5kVA, 60 Hz, 208/240 or 440/480 V-AC Input	38,000	70	1,280	1,025	NA
MGF8801	Power Sequencer for use with MG	4,000	2	135	110	NA
MGF8802	Power Sequencer for use with full-system UPS	4,000	2	135	110	NA
CPF8801	Thermal Exchange Air Unit. One option required for each TEP when customer cannot provide chilled water source for TEP.	30,000	50	1,200	1,000	NA
	Peripheral and Network Processors Attachment Features:					
MXF8020	General-Purpose Adapter for disk	18,500	15	850	700	NA
MXF8021	General-Purpose Adapter for tape	18,500	15	850	700	NA
MXF8407	Exchange of disk or magnetic tape processor attachment feature; IOM/CAU to IOP/CBU system	3,000	NA	NA	NA	NA
MXF8408	Exchange of unit record processor attachment feature; IOM/CAU to IOP/CBU	3,000	NA	NA	NA	NA
MXF8409	Exchange of DATANET 8, page printing system, DPS 88 SSF, or document handler processor channel connection feature; IOM/CAU to IOP/CBU	3,000	NA	NA	NA	NA
MXF8412	Exchange of DN6600 network processor attachment feature; IOM/CAU to IOP/CBU	3,000	NA	NA	NA	NA
MXF8414	Hyperchannel attachment Feature for IOP/CBU Systems	14,000	111	1,111	745	NA
MXF8415	Exchange of Hyperchannel attachment feature from IOM/CAU to IOP/CBU Systems	4,000	NA	NA	NA	NA
MXF8801	Exchange of high-speed disk or tape processor attachment feature	4,500	NA	NA	NA	NA
MXF8802	Exchange of standard-speed peripheral processor attachment feature	4,500	NA	NA	NA	NA
MXF8803	Exchange of network processor or page printing system attachment feature	5,000	NA	NA	NA	NA
MXF8815	Exchange of Hyperchannel attachment feature from IOM/CAU to IOP/CBU systems	6,000	NA	NA	NA	NA

NA—Not applicable. ■