Cii Honeywell Bull Series 60, Level 64

MANAGEMENT SUMMARY

Designed primarily for business data processing, the medium-scale Level 64 systems offer a wide range of facilities for batch processing, transaction processing, and communications. The five Level 64 models fit into the Series 60 family between the small-scale Level 62 and the large-scale Level 66 systems, slightly overlapping them. Competitive with the IBM System/370 Models 115-2 through 145, the Level 64 systems are marketed worldwide by CII-HB and Honeywell Information Systems.

Although CII-HB is currently emphasizing the transaction-processing capabilities of the Level 64, these systems can be configured to be equally at home in batch or communications oriented environments. The Level 64 has much of the versatility of a large-scale system, thus its suitability for a particular environment is determined more by the amount of work to be performed than it is by the job mix.

In general, CII-HB sells only the low-end models of the Level 64, the 64/20 and 64/30. The larger models, the 64/40, 64/50, and 64/60, are intended to provide a growth path for existing Level 64 users. A user whose immediate needs would require one of these models usually is steered toward the Level 66. Although the Level 64 and 66 are software compatible, this policy helps to assure the customer that he won't have to replace a major portion of his hardware in the near future.

Level 64 systems run under a subset of the General Comprehensive Operating System (GCOS), the operating system used on all Series 60 systems. Level 64 GCOS provides COBOL, RPG, and FORTRAN compilers, two file management systems, a data base management system, communications control, a transaction processing system, interactive editing of source programs, and a standard complement of utility programs.

Designed and built in France, the Level 64 systems are the medium-scale members of the broad Series 60 family marketed worldwide by CII-HB and Honeywell Information Systems. Virtual-memory oriented, the five Level 64 models can support concurrent mixtures of batch, communications, and transaction processing jobs. Prices range from 2,000,000 FF for a basic 64/20 to 5,000,000 FF for a medium-sized 64/60.

CHARACTERISTICS

MANUFACTURER: Cii Honeywell Bull, 94, avenue Gambetta, B.P. 33, 75960 Paris, Cedex 20, France. Telephone 355 44 33. Telex 220 898 F.

MODELS: Series 60, Level 64, Models 64/20, 64/30, 64/40, 64/50, and 64/60.

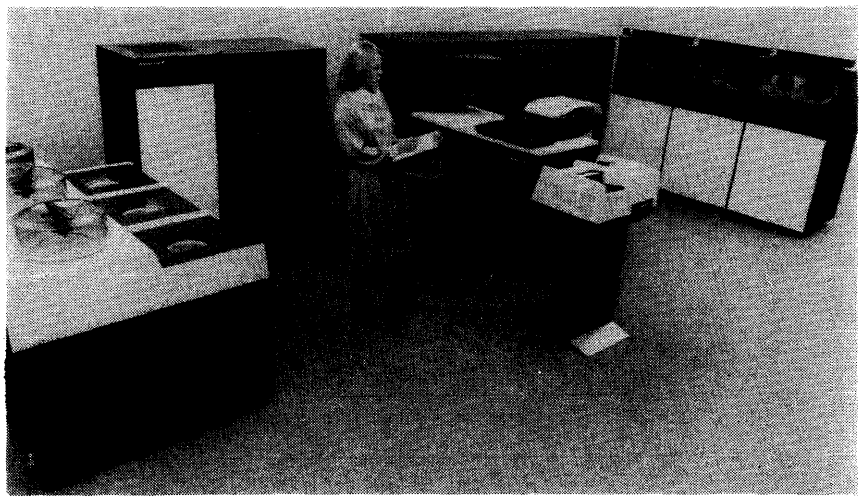
DATA FORMATS

BASIC UNIT: 8-bit byte plus one parity bit. Data paths are four bytes (32 bits) wide. Data can be interpreted as binary, decimal, hexidecimal, or alphanumeric. Data bits are interpreted in groups of four (packed or unpacked decimal data) or eight (alphanumeric EBCDIC), or in strings of 16 to 64 bits (binary digits). The strings can be interpreted as signed or fixed-point binary numbers or as floating-point operands with single (16-bit) or double (32-bit) precision formats. The optional scientific instruction set, used for floating-point operations, provides the capability for 128-bit quad words.

MAIN STORAGE

Memory is organized into consecutively numbered byte locations. Four-byte blocks are always accessed regardless of operand size. Halfword (16-bit) operands must begin on even-numbered byte locations, and full-word (32-bit) and double-word (64-bit) operands must begin on byte locations divisible by four.

STORAGE TYPE: Metal oxide semiconductor (MOS).



This Level 64 system includes, from left, 300 megabytes of removable disk storage, a 1,600-line-per-minute printer, 655,360 bytes of main memory, a console display, a console keyboard/printer, a 500-card-per-minute reader, and three tape drives.

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To help users move from other systems, CII-HB offers conversion software for the IBM System/3 and System/360 and 370 as well as for the older CII-HB/Honeywell Series 100 and Series 200/2000 systems. Level 64 systems also can be microprogrammed to run Series 100/200/2000 programs concurrently with Level 64 programs.

From a hardware standpoint, a Level 64 computer is a network of firmware-driven processors. Input/output processors can be added or reprogrammed to handle new peripheral devices without affecting user programs. CII-HB has taken advantage of this architecture to periodically refine and enhance the systems without obsoleting existing user software.

The first two models of the Level 64, the 64/20 and 64/40, were announced in April 1974. The remaining three, the 64/30, 64/50, and 64/60, were announced in April 1976. CII-HB's policy has been to introduce new facilities a few at a time, allowing users to absorb them before announcing more. While this may frustrate some sophisticated users, it has protected CII-HB's customers from the sort of disaster that can occur when new hardware and a new, full-blown operating system are introduced at the same time.

A minimum Level 64 system would consist of a 64/20 central processor with 64K bytes of memory, a console with a display or serial printer, a mass storage processor, a 29.2-megabyte disk drive, a unit record processor, a 600-line-per-minute printer, and a 300-card-per-minute card reader. Options include up to 256K bytes of memory, up to 400 megabytes of disk storage, up to eight tape drives, and a communications controller with up to 14 lines. Also available are faster printers and card readers plus card punches, and paper tape readers and punches.

Through a series of field upgrades, a Level 64 can grow into a 64/60 with up to 768K bytes of memory, 2400 megabytes of disk storage, 16 tape drives, and 42 communications lines. At both the 64/40 and 64/60 levels, the enhancements include faster central processor, memory, and read-only memory cycle times.

SOFTWARE

GCOS Level 64, a virtual memory, multi-tasking operating system, is implemented in hardware, firmware, and software. Parts of it reside in the memories of the input/output processors, enabling these controllers to function independently of the central processor.

The COBOL, RPG, and FORTRAN compilers divide programs into variable-length segments. CII-HB says these segments are more efficient than fixed-length pages because programs can be divided into logical entities that require less swapping. Code is never put in the same segments as variables and data, so it never has to be written back to disk. The compilers also assign protection levels to the segments to prevent unauthorized or improper use.

GCOS schedules the execution of jobs, the multiprogramming of job steps, and the concurrent execution of tasks

CAPACITY: See table.

CYCLE TIME: See table.

CHECKING: One parity bit is appended to each byte, and an additional 6-bit checking code is appended to each 36-bit word. Single-bit errors are corrected automatically, and multiple-bit errors are detected and flagged for error-recovery routines.

STORAGE PROTECTION: A 4-level ring protection scheme is implemented in system firmware with supporting hardware registers. Data and instruction coding are compiled into separate segments. Each user program segment has an associated segment descriptor that is stored in tables in main memory. Within each segment descriptor are two 2-bit fields that specify the security level required by a user program to execute or write to a particular segment. Hardware also checks that data addresses generated during program execution do not exceed specified boundaries. The segment descriptors also contain two bits that override the ring protection scheme by denying execution or write access to a user program.

CENTRAL PROCESSORS

The Level 64 systems are based on five versions of the same microprogrammed processor. The versions differ from each other in processor cycle time, memory capacity, and peripheral configurability.

The processor is divided into two major subsystems, CPU and I/O. The CPU is organized into eight functional units: the scratch memory, the address control unit, the data management unit, the channel control unit, the panel management unit, the arithmetic and logic unit, the timer unit, and the control store controller. The scratchpad unit contains the register set and working space for microinstruction execution. The address control unit contains the associative (cache) memory and address mapping logic. It generates all effective addresses by combining segment addresses with the relative addresses contained in instructions. The data management unit prefetches all instructions and data and passes them to the other functional units. The channel control unit is the link between the data management unit and the I/O subsystem. It aligns input and output data, stores transfer parameters, and provides I/O control functions. The panel management unit provides an interface to the system operator panel and to the maintenance panel and its special channel for diagnostic operations. The arithmetic and logic unit performs all arithmetic operations, both decimal and binary, and all logical operations on data. To increase reliability, the CPU has dual arithmetic and logic units running in parallel. All operations are performed concurrently and the results compared. The time unit consists of a 1-microsecond oscillator that drives three system timers: the processor timer, the internal timer, and the time-of-day clock. The control store controller extracts microinstructions from control storage and from main memory. It can address all ROM plus the first 64K bytes of main memory. Up to five microinstructions can be executed concurrently during one CPU cycle. The microprograms that perform central processing functions are separate from the input/output microprograms and have a lower priority for execution. I/O microprograms have priority levels within themselves, and the higher priorities are assigned to faster I/O devices.

REGISTERS: The Level 64 CPU has 29 registers that are visible only to the operating software. These include sixteen 32-bit general-purpose registers, eight 32-bit base address registers, one 32-bit Instruction Counter, one 8-bit Status Register, one 32-bit Stack Register, one 28-bit base address register, and one 8-bit Hardware Control Mask register. Eight of the 16 general-purpose registers can be used for address indexing. A CPU equipped with the optional Scientific Instruction Set also has four 64-bit scratchpad registers.

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CHARACTERISTICS OF THE LEVEL 64 SYSTEMS

	Model 64/20	Model 64/30	Model 64/40	Model 64/50	Model 64/60
MAIN STORAGE					
Type	MOS	MOS	MOS	MOS	MOS
Cycle time, nanoseconds	1000	1000	860/980	860/980	740/940
Minimum capacity, bytes	65,536	65,536	98,304	98,304	196,608
Maximum capacity, bytes	262,144	393,216	458,752	524,288	786,432
Bytes fetched per cycle	4	4	4	4	4
CENTRAL PROCESSOR					
Cycle time, nanoseconds	500	500	430	430	370
No. of registers	29	29	29	29	29
No. of instructions	195	195	195	195	195
CONTROL MEMORY					
Type	Bipolar	Bipolar	Bipolar	Bipolar	Bipolar
Cycle time	175	175	155	155	145
Capacity	40 to 64KB	40 to 64KB	40 to 64KB	40 to 64KB	40 to 64KB
Bytes fetched per cycle	4	4	4	4	4
INPUT/OUTPUT CONTROL					
Maximum channels	3	3	6	9	10
Maximum channel data rate, bytes per second	1,250,000	1,250,000	1,250,000	1,250,000	1,250,000
Total data rate (max.), bytes per second	3,750,000	3,750,000	4,080,000	4,080,000	4,250,000
CONFIGURATION					
Mass storage controllers (max.)	1	1	2	2	3
Drives per controller (max.)	4	8	8	8	8
Maximum disk capacity (megabytes)	400	800	1600	1600	2400
Magnetic tape controllers (max.)	1	1	1	2	2
Magnetic tape transports (max.)	8	8	8	16	16
Unit record controllers (max.)	1	1	2	2	2
Unit record devices (max.)	5	5	8	8	8
Communications controllers (max.)	1	1	2	3	3
Communications lines (max.)	14	14	28	42	42

within job steps. The Transaction Driven System (TDS/64) takes advantage of this multi-tasking facility to run multiple Transaction Processing Routines as tasks within a single job step.

GCOS supports two file management systems and a data base management system. The Basic File Access System (BFAS) handles 360/370 DOS and DOS/VS direct, sequential, and indexed sequential file formats. The Universal File Access System (UFAS) handles indexed random files of variable-length records. The Integrated Data Store (IDS/II) system is a subset of the data base management system developed for the Level 66 systems.

GCOS provides a two-level data communications control system that buffers applications programs from the nuts and bolts of network support and message handling. The Basic Terminal Network Support (BTNS) system runs in its own job slot and provides the interface between the network and the Message Access Method system which interfaces with the applications programs. BTNS also provides an interface for the TDS/64 transaction monitor.

A Level 64 system can communicate with another Level 64 or with Level 6, Level 61, and Level 66 systems as well as with a variety of terminals.

INSTRUCTION REPERTOIRE: All Level 64 CPU's have a set of 195 instructions, including logical operations, editing functions, operations for address computations, and arithmetic instructions for performing decimal and binary operations on packed or unpacked data. Operands can be binary, fixed-point, or decimal in packed or unpacked format; bytes; byte strings; or bit strings. The optional Scientific Instruction Set adds 26 instructions to the standard set.

The instruction repertoire also can be extended by implementing the Series 100 or Series 200/2000 Program Mode (emulation) option. These firmware packages add the Bull 100 or Honeywell-Bull 200/2000 instruction set.

CONTROL STORAGE: The CPU's control storage consists of both bipolar read-only memory (ROM) and firmware routines stored in main memory. Routines from both sources are executed by the CPU. Read-only memory cycle time is 175 nanoseconds for Models 64/20 and 64/30, 155 nanoseconds for Models 64/40 and 64/50, and 145 nanoseconds for Model 64/60.

CACHE MEMORY: An associative memory stores the eight most recently used segment descriptors and their associated segment numbers. This feature increases CPU performance by reducing the time required to calculate effective addresses.

PROCESSOR MODES: There are two modes of operation, master and slave. The master mode, used only by the GCOS operating system, allows unrestricted access to all of main memory, permits initiation of I/O operations, and permits setting of control registers. The slave mode is used by user

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RELIABILITY/MAINTAINABILITY FEATURES

Reliability and maintainability features in the Level 64 systems include several independent checking operations, although these systems lack the ability to perform diagnostics concurrently and to diagnose problems remotely. The Level 64 CPU's include five largely independent features that provide troubleshooting information. Parity is checked on every access to storage, whether mass storage or control storage. Further, parity is checked whenever data is transferred between any two system functional units. Main memory is error-correcting and detecting (EDAC) memory that appends a 6-bit error-correcting code to each 4-byte word. This code permits automatic correction of single-bit errors and flags multiple-bit errors after retrying the access. Main memory can be automatically reconfigured if a permanent error is diagnosed. Blocks of 32K bytes can be bypassed without re-initializing the systems. The Level 64 CPU's also have redundant arithmetic logic units that duplicate each operation and compare the results.

Internal diagnostics are performed by two units within the Level 64 systems. The central processor contains microprograms implemented in firmware that checks out individual elements at initialization. The peripheral processors each have similar circuitry for performing self-tests.

The Level 64 unit record processor also functions as a system diagnostic processor. If a failure is detected in either the central processor or a peripheral subsystem, diagnostic routines are loaded into the unit record processor read/write memory, enabling it to perform system tests and report results on the system console.

COMPETITIVE POSITION

The various models of the Level 64 line offer performance characteristics that compare favorably with the smaller models of the IBM System/370 family; the Univac 90/30 and 90/60 systems; various models of the Burroughs B 1800, B 2800, and B 3800 systems; and the NCR N-8450, N-8550, N-8560, and N-8570 systems.

More than 1,000 Level 64 systems have been installed or ordered by users in 30 countries.□

programs and also by GCOS when appropriate. In the slave mode, all storage references are relative to the base register's contents and are restricted to assigned boundaries, program execution times are limited by the timer registers, and input/output and certain control operations cannot be executed.

INTERRUPTS: Interrupt signals are generated by conditions such as successful completion of I/O operations, I/O errors, arithmetic overflow, timer runout, attempts to reference out-of-bounds storage locations, etc. Interrupts are referred to microprogrammed routines located in the central processor read-only memory for initiation of the appropriate servicing routines.

CONSOLE: The console includes a keyboard, a system operator panel, a tape cassette drive for system diagnostics, and either a CRT display or a 30-cps printer. Optionally, the console can include both the display and the printer.

COMPATIBILITY FEATURES: The Level 64 processors are equipped with a standard compatibility feature that enables them to execute programs written for the older Series 100 and Series 200/2000 systems. The 100 Program Mode supports the execution of the Series 100 operating systems EDOS and ETOS. The 200/0 Program Mode supports the execution of the Series 200 operating systems Modl MSR and Modl TR and the Series 2000 operating system OS/2000.

The Disk Operating System Program Mode supports the execution of programs written for IBM System/360 systems running under DOS.

Program modes are implemented by hardware/firmware housed in the read-only storage of the central processor and by compatibility routines that reside in main memory. Machine instructions, such as I/O operations, that cannot be directly executed are passed to the compatibility routines for interpretation and execution.

A program mode session is regarded by the GCOS operating system as a single job. A session can be submitted to the system through the input reader and GCOS will schedule the job, allocate resources, and initiate the session alongside other jobs in the multiprogramming environment. Once the program mode is initiated, the operator communicates directly with the old operating system. He can simulate the action of switches and pushbuttons by using a "mode control language." Commands are entered through the Level 64 console.

INPUT/OUTPUT CONTROL

CONFIGURATION RULES: The Model 64/20 consists of a single central processor, an integrated mass storage processor (IMSP), an integrated unit record processor (IURP), and an integrated magnetic tape channel. The IMSP can attach up to four disk pack drives, while the IURP has six ports, three of which connect the console device, the card reader or reader/punch, and the line printer. The remaining ports can be used to attach an additional card reader, card punch, or the integrated communications controller for up to 14 lines. The integrated magnetic tape channel requires a magnetic tape processor to attach up to eight magnetic tape units.

The Model 64/30 configuration rules differ from those of the Model 64/20 only in the number of disk pack drives that can be attached to the IMSP. The 64/30 can attach up to eight drives instead of the four that can be attached to a 64/20.

The Model 64/40 initial configuration includes the IMSP, the IURP, and the magnetic tape channel. It can be expanded by adding one magnetic tape channel and one non-integrated 8-drive mass storage processor. In addition, a second non-integrated URP can be added to provide three additional unit record ports. The additional mass storage processor can be used to provide an additional eight disk drives or to provide dual-access capabilities for the first eight drives. The additional magnetic tape channel is used to provide dual-access capabilities through a dual-access magnetic tape processor. In either single-access or dual-access configurations, a maximum of eight tape units can be attached. The additional URP permits the attachment of a second 14-line communications controller. Like the Models 64/20 and 64/30, the Model 64/40 requires a console device, a card reader or reader/punch, and a line printer.

The Model 64/50 basic system includes the IMSP, the IURP, and the integrated magnetic tape channel and, like the Model 64/40, supports one additional magnetic tape channel. Also, as with the other Level 64 models, a console device, card reader or reader/punch, and a line printer are required. The Model 64/50 mass storage subsystem can be

expanded to two 8-drive subsystems through an optional free-standing mass storage processor. The magnetic tape subsystem can include up to 16 single-access or dual-access magnetic tape units attached through two 8-drive magnetic tape processors. The 64/50 unit record subsystem can attach up to three 14-line communications controllers.

The Model 64/60 can attach up to 24 disk pack drives through the integrated mass storage processor and two additional 8-drive free-standing mass storage processors. Its magnetic tape subsystem capabilities are identical to those of the Model 64/50; up to 16 tape units can be attached either in a single-access configuration or in dual-access configuration through an additional magnetic tape channel. A third 14-line communications controller can be attached to the additional URP; however, this option is mutually exclusive with the third mass storage processor.

SIMULTANEOUS OPERATIONS: The Level 64 peripheral processing subsystems can operate concurrently with the central processor. Each subsystem operates under control of a microprogrammed peripheral processor. Each peripheral processor contains its own arithmetic and logic unit, read/write memory, and read-only memory and is attached to the central system through a high-speed channel with a maximum data transfer rate of 1,250,000 bytes per second. All three channels in the Models 64/20 and 64/30 can operate simultaneously at the maximum data transfer rate, producing a maximum total data rate of 3,750,000 bytes per second. Input/output channel data rates in Models 64/40, 64/50, and 64/60 are limited only by processor memory speed. The maximum total data rate for each of these systems is listed in the Characteristics Table. All devices and terminals attached to a unit record processor can operate simultaneously. Mechanical operations on a disk or tape subsystem, such as seek and rewind, can proceed simultaneously with a data transfer on the same subsystem.

MASS STORAGE

CII-HB currently offers five disk-pack drives for the Level 64 systems. Capacities range from 29.2 million bytes to 200 million bytes per drive. Transfer rates range from 312,500 bytes/second to 806,000 bytes/second.

MSU0310 MASS STORAGE UNIT: This unit uses packs with 11 disks and 20 recording surfaces to provide 29.2 million bytes of storage. Average seek time is 34 milliseconds, average rotational delay is 12.5 milliseconds. The transfer rate is 312,500 bytes/second. Rotational speed is 2,400 rpm. During data transfer on one drive, a simultaneous seek operation can be performed on other drives attached to the same mass storage processor. Features include the insertion of a checking code in each record during write operations and the provision of a "write protect" capability that allows individual disk packs to be limited to read operations. The drive uses Type M 4180 disk packs. Recording format is 203 tracks, including 3 spares.

MSU0350 MASS STORAGE UNIT: This unit uses packs with 12 disks and 19 recording surfaces to store up to 70 million bytes of data. Average seek time is 25 milliseconds, average rotational delay is 8.3 milliseconds. The transfer rate is 806,000 bytes/second. Rotational speed is 3,600 rpm. During data transfer on one drive, seek operations can be carried out simultaneously on other drives attached to the same mass storage processor. Features include offset track spacing under system control when initial read attempts fail, the insertion of checking codes during write operations, and a write protect capability. The drive uses Type M 4050 disk packs. Recording format is 288 tracks, including 7 spares.

MSU0351 MASS STORAGE UNIT: This unit uses packs with 12 disks and 19 recording surfaces to store up to 70 million bytes of data. Average seek time is 30 milliseconds, average rotational delay is 8.3 milliseconds. The transfer rate is 806,000 bytes/second. Rotational speed is 3,600 rpm. This unit offers the same features as the MSU0350 plus two options: a dual port capability that allows it to be attached to two mass storage processors and an extension capability that allows it to be upgraded on-site to an MSU0401. The drive uses Type M 4050A disk packs. Recording format is 288 tracks, including 7 spares.

MSU0400 MASS STORAGE UNIT: This unit has the same specifications as the MSU0350, except that it stores up to 100 million bytes. Recording format is 411 tracks, including 7 spares.

MSU0401 MASS STORAGE UNIT: This unit has the same specifications as the MSU0351, except that it stores up to 100 million bytes. Recording format is 411 tracks, including 7 spares.

MSU0402 MASS STORAGE UNIT: This unit has the same specifications as the MSU0401, except that it uses Type M 4451 disk packs and can be upgraded on-site to an MSU0452.

MSU0452 MASS STORAGE UNIT: This unit has the same specifications as the MSU0402, except that it stores up to 200 million bytes of data. Recording format is 822 tracks, including 14 spares.

INPUT/OUTPUT UNITS

MAGNETIC TAPE UNITS: CII-HB currently offers six tape drives for the Level 64. All can read/write in any of the following modes: 9-track, 1600 bpi, phase-encoded; 9-track, 800 bpi, NRZ; and 7-track, 200, 556, or 800 bpi, NRZ.

MTP0200 MAGNETIC TAPE PROCESSOR: This controller supports up to four MTU0100/0101 or MTU0200/0201 magnetic tape clusters. The standard recording mode supported is 9-track, 1600 bpi, phase-encoded. Other modes are options. The controller includes a microprocessor, read-only memory, scratchpad memory, peripheral subsystem interface control, and device level interface control. Microdiagnostics are automatically initiated at power up, at system initialization, and when software detects a fault. Maximum throughput is 312 kilobytes/second.

MTP0300 MAGNETIC TAPE PROCESSOR: A two-channel version of the MTP0200, this controller supports up to eight MTU0400 or MTU0500 Magnetic Tape Units. It can handle two data transfers simultaneously when equipped with a second channel and two of each option ordered. Maximum throughput is 312 kilobytes/second.

MTU0100/0101 MAGNETIC TAPE UNITS: These master/slave units operate at 18.75 inches/second and transfer data at 30 kilobytes/second at 1600 bpi. Each master unit can support two drives plus two slave drives. A maximum of eight drives can be connected by configuring two master and two slave clusters. Each drive can be equipped for either 9-track or 7-track recording.

MTU0200/0201 MAGNETIC TAPE UNITS: These master/slave units have the same specifications as the MTU0100/0101 units, except that they operate at 37.5 inches/second and transfer data at 60 kilobytes/second at 1600 bpi.

MTU0400 MAGNETIC TAPE UNIT: This unit operates at 75 inches/second and transfers data at 120 kilobytes/second at 1600 bpi. Error correcting features include read after write. Each drive can be equipped for either 9-track or 7-track recording, and up to eight drives can be connected to an MTP0300 controller.

MTU0500 MAGNETIC TAPE UNIT: This unit has the same specifications as the MTU0400, except that it operates

at 125 inches/second and transfers data at 200 kilobytes/second at 1600 bpi.

UNIT RECORD PROCESSOR: This integrated controller has five device ports plus ports dedicated to the console and communications. On the models 64/40, 64/50, and 64/60, a second processor, the URP1300, can be added, providing three more device ports plus a second communications port. Each peripheral device connects to a device port via an addressing attachment.

CRU0301 CARD READER: This table-top unit reads at 300 cards/minute and has 1000-card input and output hoppers. Options include IBM and Honeywell mark sensing adapters.

CRU0501 CARD READER: This table-top unit reads at 500 cards/minute, but otherwise is the same as the CRU0301.

CRU0600 CARD READER: This unit reads at 600 cards/minute and has a 3,000-card input hopper and a 2,500-card output stacker. In addition to reading 80-column cards punched in either Hollerith or binary, the unit can be equipped to read 51-column cards and 40-column mark sense cards. Each column is read twice and, in Hollerith mode, characters are checked for validity. When an error is detected, the reader, under software control, can either offset the card in the stacker or stop.

CRU1050 CARD READER: This unit has the same specifications as the CRU0600, except that it reads 1,050 cards/minute.

PCU0120 CARD PUNCH: This unit punches 120 cards/minute and has a 1,600-card input hopper and a 1,500-card output stacker. Cards can be punched in Hollerith or binary. When an error is detected, the punch can be told either to offset the card in the stacker or to stop. The unit automatically skips leading blank columns at high speed, resulting in higher punching rates.

CCU0400 CARD READER/PUNCH: This unit reads at 600 cards/minute and punches at 120 cards/minute. Hopper capacity is 1,600 cards, stacker capacity is 1,500 cards.

PTU0600 PAPER TAPE READER: This unit reads at 600 characters/second or, when equipped with the square hole option, at 580 characters/second. Format options include round hole, typesetting, or square hole. Features include odd, even, or no parity check; removal of shift codes, blank tape, and deleted characters; and programmed rewind on units equipped with a powered spooler. The unit can read both fixed length and variable length records, and can translate input codes. A PTU0110 punch can be added to the reader.

PTU1000 PAPER TAPE READER: This unit has the same specifications as the PTU0600, except that it reads 1,000 characters per second, or, when equipped with the square hole option, 847 characters/second.

PTU0110 PAPER TAPE PUNCH: This unit punches at 110 characters/second and mounts on top of the reader unit.

PRU0600 LINE PRINTER: A drum printer, this unit operates at up to 600 lines/minute when equipped with a 64-character set. Standard line length is 120 positions, optionally expandable to 132 positions. Line spacing of 6 or 8 lines/inch is program selectable. Form widths can range from 4.75 to 18.94 inches and lengths from 3 to 17 inches. Vertical forms movement, including skipping, is program controlled. Data is transferred to the printer buffer a line at a time. The printer can use up to 6-part paper. Various character sets are available to meet local requirements.

PRU0640 LINE PRINTER: Rated at 600 lines/minute when using a 64-character set, this buffered unit uses interchangeable belts containing 480 characters. A belt can include a maximum of 240 different characters. When belts are changed, the operating system must be instructed to load a corresponding belt image into the printer's controller. Forms control, including selection of 6 or 8 lines/inch and skipping, is under program control. Line length is 120 positions, optionally 136 positions. Form widths can range from 4 to 19 inches, lengths from 4 to 16 inches. The unit can print an original and five carbon copies or 10 self-carbon copies.

PRU0800 LINE PRINTER: This is an 800 line/minute version of the PRU0600.

PRU0840 LINE PRINTER: This is an 800 line/minute version of the PRU0640.

PRU1040 LINE PRINTER: This is a 1,000 line/minute version of the PRU0640/0840.

PRU1200 PRINTER UNIT: Using an interchangeable print belt, this unit operates at speeds up to 1,200 lines/minute. The standard belt contains 63 OCR-B characters, but belts can contain as many as 240 different characters. To increase speed, special belts can be designed so that the most used characters are repeated at different frequencies according to their use. The belts are identified by a magnetic code recorded on their base, and the printer uses this code to make sure it has the correct belt image stored in its buffer. Belt images are loaded into the buffer by the operating system. CII-HB says the unit produces smear-free printing because the fingers containing the characters are so flexible that they are momentarily immobilized when struck by a hammer.

Parameters for number of lines per inch (6 or 8) and vertical form positioning, including skipping, are under program control. An overtemperature control, however, can slow the skipping speed or halt the printer if the operating temperature exceeds pre-set limits. Skipping speed normally ranges from 23.5 inches/second for one to three lines up to 90 inches/second for more than six lines.

Standard line length is 136 positions, optionally expandable to 160 positions. The pitch is 10 characters/inch. Forms can range from 4 to 18.25 inches in width and from 4 to 16 inches in length. By leaving the cabinet door open, forms up to 22 inches wide and 24 inches long can be stacked externally. The unit can print one original and up to five carbon copies or 10 self-carbon copies.

PRU1600 PRINTER UNIT: This unit has the same specifications as the PRU1200, except that it prints at up to 1,600 lines/minute when using a 48-character set.

COMMUNICATIONS CONTROL

All Level 64 systems are equipped with an Integrated Communications Controller that interfaces with the Unit Record Processor. The controller supports up to 14 lines at speeds to 19,200 bits/second in any mixture of synchronous and asynchronous modes. On the 64/40, a second controller can be added, bringing the total number of lines supported to 28. On the 64/50 and 64/60, a third controller can be added, bringing the total number of lines to 42.

SOFTWARE

OPERATING SYSTEM: All Series 60 systems run under either a subset or the full implementation of the General Comprehensive Operating System (GCOS). Level 64 systems run under the GCOS Level 64 subset. The current release, 1C, is scheduled to be replaced by an enhanced release, 1D, late in 1978.

GCOS LEVEL 64 RELEASE 1C: Release 1C provides concurrent support for one batch job stream, one compatibility-mode job stream (Series 100 or Series 200/2000 emulation), a system input reader, a system output writer, communica-

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tions, and a transaction processing system. Additional batch job streams can be run in place of other activities up to a maximum of five. The sixth job slot is always taken by the output writer.

Although only six jobs can run concurrently, an unlimited number of jobs can be queued. Based on their priorities, these jobs will be started as job slots become available. Jobs are divided into job steps (individual programs), and job steps into processes (tasks). Steps of a job are run sequentially, but processes within steps are executed in parallel whenever possible.

Automatic memory management is based upon variable length program segments rather than fixed length pages. The compilers automatically divide a program into segments, placing code (always re-entrant) and data into different segments. Optionally, the programmer can define the segments he wants. COBOL programs normally are segmented by section, FORTRAN programs at natural boundaries, and RPG II programs by logical functions.

GCOS uses segment-relative addressing. Each address includes a segment number and a displacement number. When an address is referenced, GCOS first checks an associative memory containing the absolute addresses of the last eight segments referenced. If the segment is in real memory, GCOS places the real address in an index register. If the segment is on disk, GCOS brings it into real memory. If the segment's address is not in the associative memory, GCOS refers to a complete table of segments to locate it on disk and then brings it into real memory. If there is not enough space for the segment in memory, GCOS first tries to make adquate space by reorganizing memory. If this approach fails, GCOS will remove the least-active segment from memory to create space.

Each segment is protected by a four-level ring system. Rings are numbered 0 to 3, with 0 the most privileged level. Each possible use of the segment — read, write, or execute — is assigned a protection level. When an address is referenced, the appropriate protection level is compared to the current ring number of the central processor. Access is allowed only if the ring number is less than or equal to the protection level. Code is always assigned protection level 0, which effectively makes it unwritable and prevents accidental or unauthorized alterations. Rings 0 and 1 are reserved for system software, 2 and 3 for application programs.

Level 64 integrity features include error logging, file security, and recovery routines. Whenever the firmware of the Level 64 system discovers an error, it notifies the appropriate routine. This notification takes place whether the firmware recovered the error or not, so that GCOS is always aware of the state of the system. The routines diagnose the error and update an error accounting area in memory. Error accounting information is used to keep track of the state of all system components and to update a permanent accounting file. This permanent file eases routine maintenance of the system; extensive error accounting information allows failing components to be identified and replaced before they cause problems.

GCOS Level 64 also includes a variety of file security aids. A save/restore utility is available for taking security copies of files, and both copies and saved generations of a file can be included in the system catalog.

GCOS includes a journal function to speed file recovery. The journal is used to save all the updates to a file since the last security copy was taken. The journal, together with the catalog and the restore utility, provides all the information needed to rebuild a damaged file to its correct state.

To reduce the possibility of a system failure, GCOS Level 64 provides a fast recovery facility in rerun support. Rerun support allows processing to be restarted immediately, either at the beginning of the job step or at the last checkpoint. The restart procedure includes automatic repositioning of the user's files and the recovery of all files and queues used by the system, including the input reader and output writer files. The output writer can restart printing at any specified block.

Job flow through the Level 64 system is controlled by GCOS job management. The input reader reads the job input while other jobs are executing and translates the job control information into an internal format to speed job processing. A job scheduler schedules the execution of the job using a system of job classes and priorities within each class. Resources are allocated at file, volume, and device levels to each job step, and deallocated when each job step is completed. Job accounting information is collected at all stages of the job's passage through the system. Job accounting information, along with the results of the job, is provided by the output writer, asynchronously with job execution.

The file management routines of GCOS handle allocation and deallocation of space for files, automatic label checking, automatic volume recognition, control of multiple concurrent accesses to files, and control of multiple copies and generations of files through the catalog. Additionally, they provide various access methods to different file organizations and also file and volume utilities to support file housekeeping.

GCOS allocates resources to job steps rather than to whole jobs to ensure effective use of the available resources. Space is allocated for files, and files are assigned to programs at the start of the job step requesting them. The files are then unassigned, and space for temporary files is normally released as soon as the job step has completed.

When assigning a file, the user defines the file as either permanent or temporary. If the user wishes to retain a temporary file for several job steps, a parameter in the ASSIGN statement prevents the file space from being released until the end of the job.

To request space for a file, the user specifies the type of device, the identity of the volume, and the amount of space required. GCOS then searches the specified volume and automatically allocates any space available. Disk space need not be contiguous; GCOS can allocate space for a file using up to five separate areas on any one volume, and can spread the file over a number of volumes if required. On magnetic tape, GCOS supports any number of files on a single tape.

When a new file is created, file management automatically creates the appropriate labels, and these are subsequently checked every time the file is opened for processing. On disk, labels are stored in a special area called the volume table of contents (VTOC). On tape, the labels are created at the head and the tail of each file.

Disk files are sharable under Level 64 GCOS. However, if file protection is required, multiple access can occur only in read mode.

Volume mounting and dismounting is controlled automatically by the system, and warnings are given if the wrong volume is used. This control is based on the volume label, which contains a unique identifier for each volume. When a volume is mounted, the automatic volume recognition feature reads its label and the identifier is stored. When space is requested or a file is opened on a specific volume, the file management system is aware of its status. If the volume is not mounted, an operator message is issued.

Among the file characteristics recorded in the file catalog are the generation number and copy number of each file. The records for different generations and copies of the same file are linked together, and the catalog automatically controls the numbering and deletion of file generations to maintain the number of generations specified by the user. Each record also contains a list of the volumes on which that copy of the file resides.

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To access the latest generation of a cataloged file, the user's program refers to a file by name. This program internal name is matched to the external name of the required file when the file is assigned to that program, and the external name is used to access the catalog. The catalog automatically provides the latest generation of the required file, and supplies the file access system with the identifiers of the volume(s) on which that generation resides. Since automatic volume recognition has recorded the address of the device on which each volume is mounted, and the file label indicates the extent of the file, access to the file is complete.

The main file access system of GCOS Level 64, the Universal File Access System (UFAS), replaces random, sequential, and indexed sequential files. UFAS satisfies all the requirements of the ANSI Mass Storage Task Group recommendations for sequential, relative, and indexed access. It is independent of device characteristics, file organization, media addresses, and media formats.

Programs can access data sequentially, randomly by key, directly, or directly by relative position on the same UFAS file. The access method can change every time the file is accessed. UFAS files can be indexed or non-indexed; if indexes are used, they can be multiple-level, and records with indexes can be intermixed with records without indexes. UFAS can handle fixed-length, variable-length, and dynamically variable records, and a UFAS file can contain a mixture of different record types.

The file organization of a UFAS disk file is based on control intervals and control areas containing embedded free space, thereby eliminating the need for overflow areas. When records are inserted into a UFAS file, they can be physically located in their logical positions on the file; access time is reduced and the need for frequent reorganization removed. In addition, the physical record sizes in a UFAS file are independent of the lengths of the logical records. When the file is moved from one medium to another, the physical record size can change to adapt to the new medium without affecting the file or the programs using it.

GCOS also suports classical files with the Basic File Access System (BFAS). BFAS includes three subsystems:

- Basic Sequential Access, which supports sequential files on disk units EBCDIC code and on tape using either EBCDIC or ASCII code. Records can be fixed, variable, or undefined.
- Basic Indexed Sequential Access, which supports indexed sequential files on disk. Files can have up to six levels of index, with the highest-level index being resident in memory. Overflow space can be reserved within the prime data areas, on separate cylinders within the file.
- Basic Direct Access, which supports access by relative record number and by complete or partial physical address to disk-based files. Basic Direct Access includes a number of established randomizing algorithms.

A third set of access methods, the Honeywell File Access System (HFAS), gives full access to files in the format used on Series 200/2000 system. HFAS includes all the features available with BFAS.

The GCOS data communications software, together with the Level 64 communications hardware and firmware, handles networks of up to 42 lines, with up to 16 terminals per line on the DCC4100 Integrated Communications Controller. A network can include switched, private, and direct-connect lines, as well as variety of terminal types. The GCOS Message Access Method handles a system of queues to provide the interface between the data communications network and the user's programs. The Message Access Method transforms the random, time-dependent environment of data communications into a more structured environment, allowing serial or selective processing of messages by ordinary programming techniques.

Level 64 GCOS includes an extensive set of program and file conversion routines, including the following program translators and file translators: Series 100 COBOL, Series 200 Mode 1 COBOL D and H, Series 200 Mod 1 (MSR) COBOL, Series 200 Mod 1 COBOL F and I, OS/2000 COBOL, Series 100 files, and Series 2000 files.

INTEGRATED DATA STORE II (IDS II): The IDS II data base management system includes a data description language for describing the data base and a data manipulation language for accessing data. Data relationships can be multilevel, multipath, tree, network, and compound network structures. For a complete description of IDS II, see report number 70E-480-01.

TRANSACTION-DRIVEN SYSTEM LEVEL 64 (TDS/64): A communications monitor that runs with user-written COBOL 74 transaction processing routines (TPR's), TDS/64 supports a network of up to 254 terminals. Scheduled as a job, TDS/64 and its TPR's run as a single job step (program) which permits concurrent execution of the TPR's. TDS/64 also includes a batch interface which permits batch jobs running in other job slots to appear to TDS/64 as psuedo terminals.

TDS/64 interfaces with the Basic Terminal/Network Support (BTNS) software. BTNS, which runs in its own job slot, controls the operation of the hardware and firmware of the communication controllers and passes messages to and from TDS/64. TDS/64 identifies incoming messages, loads the appropriate TPR, and then controls the conversation between the TPR and the terminal that is using it.

TDS/64 also synchronizes the concurrent execution of a variety of transactions, controls file access by competing TPR's, and journalizes file updates and message movements. TDS/64 controls access to the system by checking passwords and user identifications and protects sensitive data by checking authority codes.

TDS/64 reduces memory overhead by allowing several terminals to share one copy of a TPR. Other features include file recovery and system restart facilities and on-line debugging facilities.

PROGRAMMING LANGUAGES: CII-HB offers three languages for the Level 64—COBOL, RPG, and FORTRAN.

COBOL: Based on American National Standard X3.23-1974, Level 64 COBOL offers automatic segmentation and data communications enhancements, including an optional COBOL Data Communications Extension program module.

The Level 64 COBOL language processor automatically segments the object programs it produces. Users classify each section of a program's Procedure Division by assigning it a status level between 0 and 99. Sections assigned to level 0 are permanent segments that cannot be overlaid. Sections assigned level numbers between 1 and 49 are fixed segments, and those given numbers above 49 are independent segments and will be selected for overlaying before fixed segments. Unassigned segments are given the default assignment of level 0, and multiple segments may be assigned to the same level. This last feature is important for segments that need to communicate with each other.

Users also control the segmentation process by specifying a maximum size for both procedure and data segments. The compiler produces segments as close as possible to these limits, but they are not regarded as absolute limits. The compiler ensures that no data items are split between seg-

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ments and will override the user-specified limits to reduce the swapping activity that would result. Segment sizes are specified in the Environment Division of the program, enabling fine tuning without the need to change the body of the program.

Level 64 COBOL data communications capabilities include the Message Access Method, which handles all message flow between user programs and the network by establishing queues and operating from these. The COBOL communications facility consists of a Communications Section to describe the queues, and ENABLE, DISABLE, SEND, and RECEIVE verbs to communicate, via the queues, with the network. The ENABLE and DISABLE verbs are used to open and close the connection between the Message Access Method and a given terminal. The RECEIVE statement causes a message from a specified queue to be passed to the program, and the SEND verb causes a message from the program to be placed in a specified queue. An ACCEPT MESSAGE COUNT statement can also be used to access counts of messages in the queues.

The COBOL Data Communications Extension (GTC/MCS) is an optional extension to the basic COBOL ANS 74 language processor that provides language and functions representing Level 1 support of the Communications Module of the 1974 COBOL ANS Standard. These standards are based on the recommendations of the Communications Task Group (CTG) to the CODASYL Committee, which were subsequently included in the CODASYL Journal of Development for the COBOL language. These language elements include such statements as SEND, RECEIVE, ENABLE, DISABLE, etc., and provide the required prerequisite to use of the Message Access Method (MAM) as well as TDS/64. In conjunction with Basic Terminal/Network Support (BTNS), MAM serves as the Level 64 GCOS response to the CTG requirement that the COBOL program interface with a Message Control Supervisor (MCS). These products jointly provide the MCS attributes and functions necessary to conform with the ANS standards.

FORTRAN: Based on ANS FORTRAN IV with some extensions, Level 64 FORTRAN consists of two packages, the compiler and the run-time package. FORTRAN executes in either compile-only mode or compile-and-go mode. It requires implementation of the scientific instruction set.

The Level 64 version segments the compiled output, generating a collection of "compile units" that each represent a program segment, subroutine, or data block. These compile units are written into a temporary library from which they can be cataloged into a permanent library or submitted to a linking loader for execution. The language processor further segments the compile units into code, local data, and global data. This segmentation process permits users to take advantage of the memory management facilities of GCOS and the Level 64 hardware.

Level 64 FORTRAN produces four levels of diagnostic messages. Level 1 diagnostics point out instances of code usage that could lead to less efficient execution. Level 2 diagnostics warn users of potential error conditions that could result from code usage. Level 3 diagnostics alert users to serious coding mistakes, and Level 4 diagnostics indicate fatal coding errors that would make further processing impossible. Level 4 diagnostics also cause the generation of the object program to be suppressed, but syntax checking continues. All other diagnostics do not affect comilation.

RPG: The RPG language processor permits the interchange of data files among RPG, FORTRAN, and COBOL programs. Programs written in RPG can be linked with programs written in COBOL, FORTRAN, or other languages.

The RPG compiler features automatic file manipulation and disk handling, support for sequential, indexed, and relative file organization, physical sequential reading of indexed files, relative access to index files, device independence of sequential files, dynamic table handling capabilities, and the use of standard data management access routines by object programs.

RPG uses five files: two work files; a compute unit library for the generated program; and two input files, one for job control and one for input data. The processor accepts data from card, tape, or disk, and its output can be directed to any device supported by the GCOS output writer.

The RPG language processor features a fixed logic cycle that uses default values and specifications for certain control functions. The need to make many processing decisions (such as file selection, record input, input record formatting, and description of matching fields) is eliminated by the fixed logic cycle. Record selection and output are reduced to operations described by previously defined specifications rather than by individual procedural statements. During each cycle, the fixed logic presents the user with a single input record already in the form required for calculations. Any number of output records can be produced by one cycle.

GCOS LEVEL 64 RELEASE 1D: Release 1D includes a number of major enhancements, including the ability to support up to 10 concurrent jobs plus the system input reader. Up to four output writers can be activated at the same time, and they can handle up to 26 classes of output.

New facilities include a job and process dispatching system, time-slicing, dynamic adjustment of job priorities, and automatic detection of thrashing.

BFAS can process common files on tape cassettes, and UFAS can make use of secondary indexes. TDS/64 can access IDS files. COBOL includes the Report Writer module and can access secondary indexes. IDS-II uses less memory and includes more aids.

Other new facilities include an interactive text editor; aids to convert IBM RPG II programs, System/3 3340 files, and System/370 DOS/VS COBOL programs to CII-HB standards; Level 64 to Level 64 intersystem communications; and support for Level 61 systems as remote batch terminals.

APPLICATIONS SOFTWARE: CII-HB packaged software for the Level 64 is limited to the manufacturing and distribution industries. For manufacturers, CII-HB offers an inventory management system and a production scheduling and control system. For distributors, CII-HB offers a sales order processing system, a distribution inventory management system, and, in Series 100 Program Mode, a programmed automated replenishment ordering system.

PRICING

EQUIPMENT: Level 64 equipment is available for purchase or for rent under a 1-year, 3-year, or 5-year lease. The 1-year and 3-year basic monthly rentals entitle the user to 176 hours of central processor usage per month with on-call remedial maintenance between the hours of 8 A.M. and 6 P.M. on Mondays through Fridays. For scheduled usage beyond this period, with on-call maintenance service, the user pays an additional charge which is a fixed percentage of the monthly maintenance charge. Alternatively, the user can obtain on-call maintenance service at standard hourly rates.

SOFTWARE: Generally, the basic operating system, basic job management and file systems, programming tools such as linking and debugging aids, the job control language, and conversion aids are provided at no additional cost. A basic kit of documentation is also provided with the system. Monthly license fees are charged for language processors, utilities, application packages, communications software, and advanced job management and file systems. Extra charges also are levied for customer services, such as education, program development, system design, implementation and conversion, and network design.■