Data General microNova

The microNova family is available in three basic configurations: chip sets, board computers, and fully packaged microNova minicomputers. All the packaged variations are built around the 40-pin mN602 NMOS microNova processor (foreground), which features a full 16-bit Nova architecture and main memory addressing capacity of up to 64K bytes.

Data General's microNova is fully compatible with the popular Nova Series minicomputers in architecture and utilizes the complete range of Nova software. The microNova is a 16-bit microprocessor in a 40-pin chip package, and is available by the board or by the box. Board prices start at $600, and minicomputer prices at $6,220.

MAIN MEMORY: 8K to 64K bytes
DISK CAPACITY: 315K to 200 megabytes
WORKSTATIONS: Application dependent—up to 18
PRINTERS: 30 cps to 80 lpm
OTHER I/O: Paper tape

MANAGEMENT SUMMARY

With the introduction of the 16-bit microNova in March 1976, Data General became the first major minicomputer manufacturer to introduce a full microprocessor-based computer line—from chips, through boards, to boxes. Using a DG-built microprocessor, the microNova is compatible with the older Nova line, enabling the full range of developed and tested Nova software to be used with the new processor, the mN602.

By manufacturing its own chips, Data General has reinforced and slightly redefined its OEM position. It is apparent that integrated-circuit manufacturers are fast becoming a significant factor in the manufacture of minicomputers, and moves such as this one by DG are designed to put the company in a better position in case the IC manufacturers begin to encroach on its territory.

Moreover, effective competition in the low end minicomputer business means cost-cutting procedures—procedures that would eliminate repackaging IC's and placing heavy reliance on original source manufacturers for those IC's. This has led Data General into production of its own chips, and ultimately to the microNova. A strong plus for Data General and similar companies is in the area of software and system support, where the ➢

CHARACTERISTICS

MANUFACTURER: Data General Corporation, Westboro, Massachusetts 01581. Telephone (617) 366-8911.

Data General is a leading manufacturer of minicomputers, peripherals, and associated equipment. The company maintains sales offices in most major North American cities and in South America, Europe, and Australia. Manufacturing operations are located at the company's Southboro, Massachusetts headquarters; in Westbrook, Maine; and in Sunnyvale, California. Assembly operations are also performed in Hong Kong and in Thailand.

MODELS: MP/100, MP/200, MBC/1, MBC/2, MBC/3, MBC/SDX.

DATE ANNOUNCED: MP/100 and MP/200, February 1979; MBC/1, May 1978; MBC/2, MBC/3, MBC/SDX, July 1980.

DATE OF FIRST DELIVERY: MP/100 and MP/200, April 1979; MBC/1, MBC/2, MBC/3, MBC/SDX, N.A.

DATA FORMATS

BASIC UNIT: 16-bit word or 8-bit byte.

FIXED-POINT OPERANDS: 16-bit words can be interpreted as signed or unsigned binary numbers, logical words, memory addresses, or portions of decimal character strings.

Decimal numbers can be either character decimal or packed decimal. In character decimal format, each digit is an 8-bit ASCII character, and the sign is either carried separately as an extra character at the beginning or end of the decimal string or by modifying either the first or last digit in the string. The packed decimal format places each digit in 4-bit hexadecimal code, with a separate sign character at one end of the string.

FLOATING-POINT OPERANDS: 32-bit single-precision operands with a 7-bit exponent and signed 24-bit fraction; and 64-bit double-precision operands with a 7-bit exponent and signed 56-bit fraction. Single and double-precision floating-point arithmetic is implemented through software subroutines. No hardware floating-point arithmetic is available. ➢

Data General microNova

minicomputer makers have a major advantage over the semiconductor manufacturers.

Data General, however, is not alone in this field. Computer Automation, General Automation, IBM, Microdata, and Texas Instruments have all employed microprocessor chips, in one form or another, as early as 1971. But Data General was the first to manufacture and offer its product as a chip set, on a board as a microcomputer, and in a box as a minicomputer.

For OEM accounts, the microNova offers some interesting possibilities. They can start with a minicomputer development system, and integrate downward to microNovas on boards or to chip sets with a minimum of difficulties. Such a move permits production economies as volume increases, but does not require the heavy front-end investment associated with IC development or software conversion.

The two compatible series within the current mNova family, the MP/100 and MP/200, offer more compact packaging, more economy, and up to three times the performance of previous microNova products, according to Data General. Like the rest of the microNova family, the new hardware is designed for OEM applications. It is software- and I/O-compatible with previous microNova products, while offering reduced board sizes, lower power consumption, and substantial price/performance improvements. Data General states that the new products are directed against Digital Equipment's LSI-11, Texas Instruments' 9900 family, and the Intel 8612 series.

The MP/100 series product line consists of the board-level computers MBC/1, MBC/2, MBC/3, and MBC/SDX, the box MP/100 in an 8-slot chassis, and packaged systems. The MP/200 series consists of the board-level MP/200 SPU, the box MP/200 in an 8-slot chassis, and the fully packaged MP/200 in a half-bay cabinet with a choice of peripherals.

All the MP/100 variations are built around the mN602 processor with the Nova 16-bit architecture and instruction set, a standard data channel as well as a 2-megabyte/second direct memory access channel, asynchronous memory to allow use of EPROM as well as PROM memories, support for up to 128K bytes of memory, an integral power monitor, a hardware stack and frame pointer with stack overflow protection, 16-bit hardware multiply and divide real-time clock, all memory control and timing, integral hidden refresh logic for dynamic RAM's, four general-purpose accumulators (two of which can be used for indexing), programmed priority interrupt to 16 levels, CPU and memory control for DMA, and separate memory and input/output buses.

The I/O Controller (IOC) provides the functions of the 47-line Nova I/O bus by decoding data from a two-line serial I/O bus up to 100 feet in length. The IOC also performs integral device identification, interrupt logic, and per-device interrupt masking.

INSTRUCTIONS: One-word instructions. There are six basic instruction types, each with different formats: Memory Reference (MRI), Arithmetic and Logical (ALC), Input/Output (I/O), Multiply/Divide (M/D), Stack Manipulation (STK), and Central Processor Control (CPU).

In MRI instructions the two-bit operation code is in bits 3 and 4 (no-accumulator operations) or in bits 1 and 2 (accumulator operations), and the effective address is computed from the contents of bits 5 through 15.

Bits 1 and 2 in ALC instructions specify the source accumulator, 3 and 4 the destination accumulator, 5 through 7 contain the operation code, and 8 through 15 contain shift and carry directives.

The multiply or divide op code is contained in bits 8 through 9 of the M/D instruction which, like the I/O, STK, and CPU, contains "011" in bits 1 through 2.

The STK and CPU instructions contain the op code in bits 5 through 9, and the STK instructions also include the accumulator containing stack data in bits 3 and 4.

For all memory reference instructions, bits 5 through 15 are used for addressing, using bits 8 through 15 as the displacement or direct address. Each instruction can address 256 words directly, or can use either relative or base register addressing.

INTERNAL CODE: ASCII and binary.

MAIN STORAGE

TYPE: Dynamic MOS RAM, requiring 64 refresh cycles every 1.8 milliseconds. Refresh is overlapped with CPU execution.

CYCLE TIME: 960 nanoseconds.

CAPACITY: 64K words in 4K-, 8K-, 16K-, and 32K-word increments.

CHECKING: None.

STORAGE PROTECTION: None.

RESERVED STORAGE: The microNova has 16 reserved words which function as auto-increment/auto-decrement registers.

CENTRAL PROCESSOR

The microNova processor 16-bit architecture includes frame-oriented stack support and programmable 16-level interrupt capability on a single 40-pin circuit. It executes the full Nova instruction set and includes a real-time clock, power monitor, and transparent refresh for 4K and 16K dynamic RAM's. Its serial I/O bus is functionally equivalent to the Nova I/O bus. Data General's mN615 I/O controller integrates all bus interface and protocol logic for each I/O device and generates a 16-bit local data bus.

The basic microNova is a chip set which includes the mN602 Microprocessor, mN606 4K RAM, and these System Buffer elements: mN634 Octal Memory Bus Transceiver, mN634 Octal Memory Address Driver, mN506 Quad Sense Amplifier, and two I/O Transceivers, mN629 and mN636.

Above this level, the microNova is available as a microcomputer on a 7.5 by 9.5-inch printed circuit board. The microNova board computers, MBC/1, MBC/2, MBC/3, and MBC/SDX include the mN602 CPU with hardware multiply/divide; absolute, relative, indexed, deferred, and

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PERIPHERALS/TERMINALS

DEVICE	DESCRIPTION	MANUFACTURER
PAPER TAPE EQUIPMENT		
6013	Reader; fanfold tape, 8-channel; 400 cps	Data General
TERMINALS		
6040/6042	Dasher terminal printer; 30, 60 cps	Data General
6052/6053	CRT display; 1920-character, 64- and 96-character set, switch-selectable speeds from 110 to 19.6K bps	Data General
6012	CRT display; 1920-character, variable codes, local editing, EIA or 20-mA current loop interface, full or half-duplex; up to 4800 bps	Data General
6106/7	Dasher D/100 CRT; 1920 character, 96-character set, 7 x 11 dot matrix, EIA or 20-mA current loop, 9600 bps (6107 includes printer interface)	Data General
6108/9	Dasher D/200 CRT; 1920 character, 96-character set, 7 x 11 dot matrix, EIA or 20-mA current loop, 9600 bps (6109 includes printer interface)	Data General
6073	Terminal printer, 7 x 9 dot matrix, 132 positions, 96 character set, 10 or 5 characters per inch, 6 or 8 lines per inch, RAM buffer, 4- to 15-inch forms; receive only; 300 lpm (20-character line) to 80 lpm (132-character line)	Data General

The board-level MBC/1 combines the mN602 chip with an asynchronous interface, automatic program load, and soft control panel on a 7.5-by-9.5 inch board. The soft control panel allows any ASCII console to supervise program execution, examine and modify memory and CPU registers, and support automatic program loading from any device. RAM boards of the same size are available with 8K, 16K, 32K, and 64K bytes, as are 8K and 16K PROM boards. RAM/EPROM boards with 8K or 32K bytes of RAM and sockets for 32K bytes of EPROM are also available.

The MBC/2, MBC/3, and MBC/SDX were introduced in July 1980. The MBC/2 and MBC/3 provide an mN602 central processor, three types of memory, and serial and parallel I/O on a single 7.5-by-9.5-inch board. The MBC/2 and MBC/3 differ only in the size of their random access memory capability, with 8K bytes for the MBC/2 and 32K bytes for the MBC/3. Both single-board computers have sockets for up to 1K bytes of programmable read only memory and for up to 32K bytes of eraseable programmable read only memory. The boards also have two independent, programmable asynchronous/synchronous communication interfaces, 16 lines of digital input, and 16 lines of digital output.

The MBC/SDX board is a debugging aid as well as an I/O expansion interface. It offers all the I/O features of the MBC/2. The SDX board is combined with an MP/100 or MP/200 central processor so that the SDX board acts as an input/output interface for the system.

The MBC/2, MBC/3, and MBC/SDX can be configured in a 4-slot card frame as well as an 8-slot MP/100 or MP/200 chassis. They are compatible with other board products in the DG microNova line.

auto increment/decrement addressing modes; four accumulators, two of which can be used as index words; hardware stack and frame pointers with stack overflow protection; separate memory and I/O busses; and control for DMA transfers.

CONTROL STORAGE: None.

REGISTERS: The microNova has four 16-bit accumulators, and a 15-bit program counter, stack pointer, and frame pointer. Two accumulators can be used for address indexing.

The microNova, like the Nova 3, has a last-in/first-out (LIFO) push-down/pop-up stack implemented in any 256 consecutive memory locations and two additional hardware registers (the stack pointer and the frame pointer). The stack pointer identifies the first memory location designed as the stack, and the frame pointer marks intra-stack boundaries to permit several "register saves" to be accumulated in the stack. The frame pointer can be set randomly to access words stored in stack frames without popping an entire frame.

Also, like the Nova 3, the microNova has 16 reserved memory locations which function as auto-increment or auto-decrement registers when addressed directly.

ADDRESSING MODES: The microNova has five addressing modes: absolute, relative, indexed, deferred, and auto increment/decrement.

INSTRUCTION REPERTOIRE: The basic complement includes six Memory Reference instructions, eight Arithmetic and Logic instructions, seven I/O instructions, two Multiply/Divide instructions, seven Stack Manipulation instructions, and eight CPU instructions. There are 256 variations on each of the Arithmetic and Logic instructions. Hardware multiply/divide instructions are standard.

INTERRUPTS: A 16-level programmed priority interrupt facility is used to recognize interrupts for I/O operations. Each device is wired to one of 16 bus positions, and is either authorized or denied authorization to interrupt particular service routines by an Interrupt Disable Mask Bit that corresponds to the bus positions of the device.

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The MP/100 is designed for instrumentation, remote data acquisition, and process control applications, as was the original microNova line. Its main attractions are the reduction in size from six or seven boards for a typical configuration to only two boards plus the reduction in price from the $4,000-plus range to less than $3,000.

The MP/200 is a bipolar implementation of the microNova architecture, featuring approximately three times the performance of the MP/100. It is designed for dedicated business and communications applications. Data General states that the MP/200 is rated at roughly the same performance as the Nova 4/C small computer it introduced late last year.

The MP/200, like the MP/100, is available on a 7.5-by-9.5-inch board. It executes an add in 840 nanoseconds and a multiply in 4.92 microseconds, 3 and 10 times faster, respectively, than previous microNova products. The MP/200 also provides a faster, 3.7-megabyte/second direct memory access channel and an extended instruction set that includes byte manipulation and multiply/divide operations. An optional basic controller board adds an asynchronous interface with full modem control, power fail/auto restart, automatic program load, programmable real-time clock, and a soft control panel.

Optional communications, sensor I/O, and terminal interfaces are available for both the MP/100 and MP/200. They include floppy and hard disk subsystems, single- and multi-line asynchronous and synchronous controllers; single-card A/D, D/A, and digital I/O interfaces and subsystems; and line printer and peripheral interfaces.

Software support for the new microNova products includes the firm's Disk Operating System (DOS) and Real-Time Operating System (RTOS); the Extended BASIC, Business BASIC, FORTRAN IV, and DG/L languages; and the Command Line Interpreter, Text Editor, Macro Assembler, Library File Editor, and Symbolic Debugger utilities.

Also supported is the MP/OS operating system providing development capability on the microNovas, as well as cross development capability with AOS on the Nova 4.

MP/OS supports MP/Pascal and MP/Fortran. The languages and MP/OS can be used to develop stand-alone programs, and applications based in PROM as well as diskette or hard disk.

USER REACTION

Nine microNova users responded to Datapro's 1980 user ratings survey. The nine sites included 15 systems that had been installed for an average of almost 11 months. Fourteen of the 15 computers were purchased and one was on lease.

Accounting was the most common application (4), followed by word processing (3), payroll/personnel (2),

PHYSICAL SPECIFICATIONS: The microNova in a minicomputer configuration is housed in a chassis with 8 slots. The chassis is 5.25 inches high, 19 inches wide, and 14.5 or 23 inches deep; the greater depth is with battery backup.

Power requirements for all chassis types are 100, 120, 220, or 240 VAC ±10 percent, 47 to 63 Hz. Operating temperatures are 32 to 132 degrees F. A relative humidity of up to 90 percent, noncondensing, can be tolerated. The processor outputs 2512 BTU/hour maximum. Air conditioning requirements are those of a normal office environment.

The chassis weighs approximately 37 pounds without battery backup. Add 5 pounds to the chassis weight for battery backup.

INPUT/OUTPUT CONTROL

INPUT/OUTPUT CHANNELS: An I/O bus and a Direct Memory Access (DMA) channel are standard.

The I/O bus is serial in structure and can be up to 100 feet long. Bipolar transceivers differentially drive the microNova serial I/O signal on a parallel two-line basis. This technique offers high noise immunity and ease of cabling.

The basic I/O bus is etched in the backplane. It functions to provide communication between mainframe-based I/O boards and the CPU board. The basic I/O bus is offered with a standard extension of 15 feet to connect the dual diskette subsystem. Longer extensions as discussed above are optional. Mainframe-based I/O boards are connected to free-standing peripherals by a 50-line device cable. Speed of the I/O bus is 16.6 megahertz, which translates to a data transfer rate of up to 1 million words per second.

The Input/Output Controller (IOC), a 40-pin chip located at each device interface, decodes the serial I/O signal and routes it into a parallel 16-line bidirectional data bus for I/O operations. This is the logical equivalent of the 47-line Nova I/O system. The IOC has the ability to address up to 61 I/O devices. The program I/O facility has six commands for each device. Also incorporated are controller start, clear, and I/O pulses and the facility for programmed I/O, program interrupt, and DMA functions.

For the DMA channel, rates are quoted as 148,000 words per second for input and 173,000 words per second for output. The DMA channel can be used to increment the contents of storage locations by 1.

CONFIGURATION RULES

The microNova can have up to 61 peripheral devices attached to the I/O bus. The eight-slot chassis is expandable in eight-slot increments. The actual number of peripherals that can be attached depends upon the available number of slots and the method of attachment.

Generally speaking, all peripherals require one slot for direct attachment. The processor is mounted on one board along with an Asynchronous Interface Board (AID), and requires one slot. Additional Asynchronous Interface Boards require one slot, as do General-Purpose I/O Boards.

WORKSTATIONS: The number of workstations that can be attached is dependent on the type of application, but Data General recommends a maximum of 18 workstations.

DISK STORAGE: A maximum of eight diskette/disk controllers can be attached to any microNova.

MAGNETIC TAPE UNITS: See above.

PRINTERS: See above.

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engineering/scientific (2), medical/health (2), retail (2), manufacturing (1), distributed processing (1), transaction processing (1), and software development (1). The major source of application software was in-house personnel. Most of the systems included 64K bytes of memory and 10 megabytes of disk storage. Two had 32K bytes of memory and three had from 0.3 megabytes to 1.26 megabytes of floppy disk main storage. One installation involved in medical transaction processing included seven CPU's with 0.3 megabytes of floppy disk storage. Three sites utilized two workstations while the other six used one.

BASIC and FORTRAN were the primary programming languages. Additional vendor software, proprietary software, and expanded data communications will be required by users during this year. Two users will replace their systems with equipment from a different vendor, and a third will get a larger Data General system this year.

The table below summarizes the ratings given to the microNova by the nine users.

	Excellent	Good	Fair	Poor	WA*
Ease of operation	4	4	1	0	3.3
Reliability of mainframe	3	3	1	1	3.0
Reliability of peripherals	2	3	2	1	2.8
Maintenance service:					
Responsiveness	4	1	2	0	3.3
Effectiveness	4	1	2	0	3.3
Technical support:					
Trouble-shooting	4	0	3	1	2.9
Education	3	0	2	2	2.6
Documentation	4	1	2	2	2.8
Manufacturer's Software:					
Operating system	3	4	0	1	3.1
Compilers & assemblers	3	2	2	1	2.8
Applications programs	4	1	1	1	3.1
Ease of programming	2	5	0	1	3.0
Ease of conversion	2	1	1	1	2.8
Overall satisfaction	3	4	1	1	3.0

*Weighted Average on a scale of 4.0 for Excellent.

There are two apparent inconsistencies in the ratings. One of the two users who gave the lowest ratings listed the highest number of principle applications, five. The other disgruntled user is very unhappy with the DOS operating system and Data General's implementation of the BASIC programming language. However, other users of DOS and BASIC gave two excellents and two goods, and two excellents and one good rating, respectively, to the software packages. Also, two users stated that their system costs were higher than expected, and two said they were lower.

Six out of nine of the users would recommend the microNova to other users in a similar situation.□

MASS STORAGE

6038 FLOPPY DISK SUBSYSTEM: Consists of a four-drive controller and either a 6038 single drive or a 6039 dual drive. Each floppy disk stores up to 315K bytes on 77 tracks. Maximum storage capacity is 1.26 million bytes on a four-drive subsystem. Average head positioning time is 260 milliseconds, and average rotational delay is 83 milliseconds. Data transfer rate is 31K bytes/second. The 6038 drives feature IBM 3740 compatibility and are supported by Data General's RDOS operating system. The controller occupies one slot. The 6038 drives are manufactured by Data General.

6039 FLOPPY DISK SUBSYSTEM: Consists of essentially the same components and specifications as the 6038 subsystem, except that it is a dual-drive system.

6095-N CARTRIDGE DISK SUBSYSTEMS: Each subsystem consists of a controller and up to four 10-megabyte, top-loading cartridge disk drives. The four systems are being manufactured at Data General's Westbrook, Maine, facility. These subsystems can be configured with one, two, three, and four cartridge disk drives.

Each drive employs two platters, one fixed and the other an IBM 5540-type removable cartridge, both mounted on a common spindle. Each platter is capable of storing 5,013,504 bytes, or 2,506,762 bytes per surface. There are 200 tracks per inch, 408 tracks per surface, 408 cylinders per drive, and 4 surfaces per drive. Recording density is 2200 bits per inch. All tracks are divided into 12 sectors of 512 bytes each, yielding a formatted track capacity of 6144 bytes. Each cylinder consists of four tracks, giving a formatted cylinder capacity of 24,576 bytes. Total drive capacity is 10,027,008 bytes.

Drive rotational speed is 2400 rpm. Track-to-track, average, and full-stroke head positioning times are 8, 38, and 70 milliseconds, respectively. The data transfer rate is 312,500 bytes per second. Drive start-up to full operating speed takes 30 seconds, and the drive requires 25 seconds to come to a full stop. All four subsystems are supported under the DOS and MP/OS operating systems.

6100, 6103, 6098, and 6099 DISK/DISKETTE SUB-SYSTEMS: Data General's 6100 disk series consists of integrated disk/diskette Winchester-type subsystems. The four models include a 12.5- or 25-megabyte fixed disk, either with or without a 1.26 megabyte diskette as a file transfer and backup medium. The 6104 and 6105 models include 25-megabyte disk drives while the 6101 and 6102 models include 12.5-megabyte units. Models 6101 and 6104 also contain the 1.26-megabyte diskettes. The units are stepper meter driven and are controlled by a microprocessor.

There are 384 tracks per surface in the 25 megabyte disks, with each of the four surfaces divided into two 192-track banks of 512-byte sectors. A separate read/write head accesses each band. Each eight-track cylinder has 131,072 bytes in 256 sectors.

The 12.5-megabyte disks are formatted the same way except that there are four tracks per cylinder.

The data transfer rate for both units varies with different system configurations.

The diskette has 77 tracks per side formatted into 16 sectors of 512 bytes. Average head positioning time is 100 ms, including settling time. Rotational delay is 83.3 milliseconds at 360 rpm. The data transfer rate is 62.5K bytes per second.

INPUT/OUTPUT UNITS

The Model 4222 Digital I/O Interface, Model 4223 A/D Interface, and Model 4224 D/A Interface each occupy a single microNova board. They plug directly into the microNova chassis and provide it with stand-alone data acquisition and control capabilities.

MODEL 4222 DIGITAL I/O INTERFACE: Provides a digital device interface for 16 parallel input and 16 parallel output lines. It also furnishes two strobe output lines and one

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strobe input line. All lines are TTL-compatible. An internal/external data comparator compares real-time external data against an internal software-programmable condition, allowing the system to detect transient deviations from the condition via polling or interrupts and selectively mask bits for interrupt requests.

MODEL 4223 A/D INTERFACE: Incorporates two 8-channel multiplexers, a differential input instrumentation amplifier, a sample-and-hold unit, and a 12-bit successive approximation converter. Its 16 single-ended or 8 differential inputs are program-configurable. Auto-channel scan (with wraparound capability) and triggering modes are also program-selectable. The A/O subsystem offers jumper-selectable input voltage ranges of 0 to 5, 0 to 10, or ±10V. According to the vendor, a complete conversion requires only 33 microseconds.

MODEL 4224 D/A INTERFACE: This dual-channel, 12-bit subsystem provides a user-selectable, full-scale output of 0 to 5, 0 to 10, ±5, or ±10V, and, according to the vendor, settles to ±0.01 percet full-scale of the desired output value in seven microseconds. Each channel's output range is individually set.

DG/DAC INTERFACE BOARD: Interfaces the microNova to sensors, actuators, and associated electrical circuits. Each DG/DAC chassis can accommodate up to 16 chassis control cards with up to 16 lines per card for a total of 256 signal lines per chassis. Any mix of digital and analog cards is allowed in one DG/DAC chassis, which measures 8.75 by 19 by 22 inches, weighs 60 pounds, and comes with power supply, bus terminator, and bus cables.

SENSOR ACCESS MANAGER (SAM): Provides software support for the 4222, 4223, and 4224 data acquisition and control boards, and for the DG/DAC interface. SAM is a library of device handlers and subroutines that control I/O transfers between user programs and analog and digital sensor devices. It is callable by FORTRAN IV and assembly language programs.

See the Peripherals/Terminals table for specifications for the terminals that can be used with the microNova.

COMMUNCATIONS CONTROL

GENERAL-PURPOSE CONTROLLER: Provides a generalized programmed I/O, program interrupt, and DMA interface. An area on the board is pre-drilled and allocated for user-designed and built circuitry. Up to four line interface boards in any combination can be controlled for a maximum of up to 16 asynchronous or 4 synchronous lines.

MODEL 4227 ASYNCHRONOUS LINE MULTIPLEXER: Controls up to four asynchronous communications lines. Each line can be configured for RS-232C or 20-mA current loop operation and individually programmed for number of bits per character (5 to 8), number of stop bits (1, 1.5, or 2) line speed (50 to 9600 bps), and parity (odd, even, or none). When enabled, parity is automatically checked/generated on each line. The multiplexer supports full- and half-duplex operation. The 4227 provides full character buffering on reception and transmission, program-controlled loopback testing, and modem control with automatic answer capabilities for Bell 103, 202, and 212 Series data sets.

MODEL 4426 SYNCHRONOUS LINE CONTROLLER: Interfaces to medium-speed (9600 bps) synchronous/bisynchronous communications lines, and provides a full- and half-duplex EIA RS-232C/CCITT V.24 interface and full character buffering on reception and transmission. When coupled with the optional Model 4228 hardware CRC generator, the synchronous line controller can select either of two standard check polynomials, CRC16 or CCITT16. Both idle and sync characters, as well as character size, parity, and loopback testing, are program-selectable. In receive mode, Model 4426 automatically synchronizes data and then strips out the sync character. Standard modem control is supplied for Bell 201, 203, 208, and 209 Series data sets. This synchronous controller also supports IBM Bisynch protocols with full transparency and is program code compatible with the SLM-2 Series synchronous multiplexer used on Data General Nova and Eclipse processors.

Up to four Model 4426 controllers can be configured with a single microNova minicomputer, allowing it to control a maximum of four synchronous lines. Only one CRC generator board is needed per system.

COMMUNICATIONS SOFTWARE

COMMUNICATIONS ACCESS MANAGER (CAM): A modular package that can be generated by the Communications System Generation Program (COMGEN) to include only those program segments required for each individual system. CAM operates under DOS and, since it uses the operating system's runtime-defined interrupt service, is brought into main memory from disk only as needed. This can free large segments of memory in a real-time communications system for other processing tasks.

CAM software can support both standard and special user-defined protocols, including Bisync (BSC) and an asynchronous terminal line procedure. Synchronous and asynchronous protocols can be intermixed. Multi-drop lines are supported through polling and selection sequences. Modem control support for auto answer/auto disconnect is a standard feature. CAM provides a queue for I/O completions that permits a single user task to control several asynchronous lines.

REMOTE JOB ENTRY CONTROL PROGRAM (RJE80): Allows for remote job entry and communications between microNova processors and IBM 360/370 systems, or between microNova processors and other Data General computers. Support is provided for four types of RJE systems:

- Point-to-point communications between a Nova, Eclipse, or microNova emulating an IBM 2780/3780 and an IBM 360/370 host.
- Point-to-point communications between two Data General systems running RJE80.
- Multi-drop Data General systems emulating IBM 3780 slave terminals, communicating with an IBM 360/370 host.
- Multi-drop Data General systems emulating IBM 3780 slave terminals, communicating with a Nova or Eclipse or microNova master system also running RJE80.

RJE80 is supported by DOS as well as CAM. Features include horizontal and vertical printer format control; error detection on transmission and reception; and disk, tape, or card transmission to remote systems. Transmission between host systems may be to unattended RJE80 systems, and because of device-independent I/O capabilities, any combination of I/O devices can be utilized without additional software.

IBM HASP WORKSTATION EMULATOR: Lets a microNova emulate an IBM HASP remote job entry workstation. Its multileaving capability can include up to seven input and seven output data streams. Efficiency of data transmission is achieved through interleaving and data compression.

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SOFTWARE

OPERATING SYSTEMS: Two levels are available, the DOS program development system, and the larger, real-time MP/OS.

DISK OPERATING SYSTEM (DOS): A subset of RDOS, DOS is designed for use in development systems only. DOS requires a minimum of 16K words and includes a Command Line Interpreter, Text Editor, Library File Editor, and Relocatable Loader. It supports a FORTRAN IV compiler, and single- and multiple-user Extended BASIC and Business BASIC interpreters. Since DOS is a compatible subset of RDOS, any program developed under DOS can be run under RDOS or RTOS.

DOS BASIC: A subset of RDOS Extended BASIC, upward-compatible with both RDOS and AOS Extended BASIC. The interpreter takes advantage of operating system features by supporting device independence, and features extensions to the Dartmouth BASIC language. These extensions include string arithmetic, matrix operations, user-controlled output formatting, and sequential, random, and contiguous file management. DOS BASIC also offers several program development features and an assembly-language interface that allows subroutine calls. Both single- and multi-user versions of DOS BASIC have been released by Data General.

DOS BASIC implements string variables and literals, string concatenation, and string subsetting. Users can determine the location of a character within a string or the number of characters assigned to a string variable. They can also convert a numeric expression to a string that is its decimal representation, and return the decimal representation of a string variable or literal. In addition, READ and IF/THEN statements may employ strings. Matrix manipulation is achieved through a set of statements such as ADD, SUBTRACT, MULTIPLY, INVERT, and TRANSPOSE. Data General states that matrix dimensioning and redimensioning can easily be accomplished. Complete matrices can be read or written in a single I/O call.

The minimum hardware configuration for single-user DOS BASIC is any Nova computer, microNova computer, or microNova computer on a board with 16K words of main memory, a dual diskette drive and controller, and one terminal with appropriate interface. The minimum hardware configuration for multi-user DOS BASIC is any microNova with 32K words of main memory, a dual diskette drive and controller, and two terminals with appropriate interfaces. Additionally, a wide variety of peripherals can be supported on a Nova-based DOS BASIC system, including diskette drives, magnetic tape drives, line printer, paper tape reader and punch, plotter, and multiple terminals. A maximum of 32K words of main memory can be supported.

MP/OS: A single-user, multi-tasking, disk-based, real-time operating system. Programs developed on AOS Eclipse systems can be run under MP/OS, within hardware constraints. MP/OS supports MP/PASCAL and MP/FORTRAN IV. It provides data management capabilities such as permanant file protection, device-independent I/O access, and hierarchical file directories. MP/OS utilities include a command line interpreter, text editor, macro assembler, binder (compiles object files into relocatable program files), debugger, and library editor.

The minimum hardware required for MP/OS is 64K bytes of memory, one megabyte of disk or diskette storage, and a console.

OTHER SOFTWARE: Along with the RJE80, HASP II, CAM, and SAM software packages discussed elsewhere in this report, Data General provides paper-tape software consisting of an editor, assembler, and debugger, designed to operate in 4K words of memory.

PRICING

POLICY: Data General offers the microNova series on a purchase-only basis, with two types of separately priced maintenance agreements: the On-Call Service contract and the Depot Service contract, which involves return of faulty equipment to a designated repair location. In either case, all parts and labor are included at no additional cost.

Normal prime-time on-call contract service hours are 8 a.m. to 6 p.m. Charges quoted in the price list are applicable to customers within 100 miles of a service center. Additional but uniform monthly charges are in effect beyond 100 miles of a Data General service center. These charges are $150 for customers between 100 and 300 miles from the center and $225 for customers beyond 300 miles.

Under a Depot Service contract, any portion of a system may be covered, the minimum contract being $75. The customer assumes all transportation and insurance costs. For non-contract on-site service, the hourly maintenance rates are $58 for prime time and $68 for other times. A three-hour minimum applies. Depot service hourly labor charges are $35 for prime time and $55 for all other times.

Prices shown are for single-unit quantities, OEM quantity discounts apply, and are available from Data General upon request.

Data General software is licensed so as to be included without charge on a system with sufficient Data General hardware to operate it. The software is also available for purchase for use on configurations utilizing other than Data General equipment (e.g., peripherals, add-on memory, etc.).

Data General provides training courses for customers at its Westboro, Massachusetts headquarters, at its Mid-Western center in Arlington Heights, Illinois, and at its Western Training Center in Los Angeles, California, and at six international locations. A special five-day course, "Designing with microNova," covering hardware components design and maintenance, memory systems, instruction set, interfacing, configuration, and program development, is offered. In addition to the centers listed above, this course can be taught at customer locations by special arrangement. Two training credits are given for each development system purchased by an end user, which entitle the customer to approximately one man-week of training. Schedules for training courses can be obtained at any Data General field office.

Software and Hardware Subscription Services are available. They provide automatic updates, additions, and documentation for a fixed yearly fee.

The Data General Users' Group provides a forum for interchange of programs. The programs are available for a fee to cover reproduction and distribution costs.■

Data General microNova

EQUIPMENT PRICES

		Purchase Price	On Call Service
PACKAGED SYSTEMS			
Model 9600 MP/100 packaged systems include MP/100 System Processing Unit (SPU), 32K bytes of memory, dual-diskette, chassis, asynchronous interface, and power supply.			
9060	Without terminal; for use with terminals with international fonts	$6,260	$76
9060-A	With 30 cps KSR Dasher Printer	8,660	101
9060-B	With 60 cps KSR Dasher Printer	8,910	104
9060-C	With 6052 CRT Display	8,450	96
9060-D	With 6053 Dasher CRT Display	8,910	96
Model 9061 MP/100 packaged systems are the same as Model 9160's except for 64K bytes of memory			
9061		6,840	80
9061-A		9,240	105
9061-B		9,490	108
9061-C		9,030	100
9061-D		9,490	100
Model 9062 MP/100 packaged systems are the same as Model 9061's except 10-megabyte disk subsystem (6095) instead of dual diskette			
9062		12,740	118
9062-A		15,140	143
9062-B		15,390	146
9062-C		14,930	138
9062-D		15,390	138
Model 9065 MP/100 packaged systems include an MP/100 SPU, 64K bytes of memory, asynchronous interface, multiply/divide, real-time clock, power fail/auto restart, and console debug with automatic program load			
9065-A	With 10-megabyte cartridge disk (6095-N)	12,740	118
9065-B	With 12.5-megabyte disk and 1.26-megabyte diskette (6101)	10,240	110
9065-C	With 25-megabyte disk and 1.26-megabyte diskette (6104)	13,140	118
9065-D	With dual 315K byte diskettes (6039)	6,840	80
Model 9064 MP/200 packaged systems include MP/200 System Processing Unit, 64K bytes of memory, 10 megabytes of disk storage (6095)			
9064	Without terminal; for use with terminals with international fonts	13,685	128
9064-A	With 30 cps KSR Dasher Printer	16,085	153
9064-B	With 60 cps KSR Dasher Printer	16,335	156
9064-C	With 6052 Dasher CRT Display	15,875	148
9064-D	With 6053 Dasher CRT Display	16,335	148
Model 9066 MP/200 packaged systems include an MP/200 SPU, 64K bytes of memory, asynchronous interface, multiply/divide, real-time clock, power fail/auto restart, and console debug with automatic program load			
9066-A	With 10-megabyte cartrige disk (6095-N)	13,685	128
9066-B	With 12.5-megabyte disk and 1.26-megabyte diskette (6101)	11,185	120
9066-C	With 25-megabyte disk and 1.26-megabyte diskette (6104)	14,085	128
9066-D	With dual 315K byte diskettes (6039)	7,785	90
MP/100 computers include an mN602 microprocessor, 8-slot chassis, hardware multiply/divide, real-time clock, standard or high-speed data channel, asynchronous memory bus, and power fail/auto restart.			
8520-A	With 8K bytes of MOS memory	1,785	28
8520-B	With 16K bytes of MOS memory	1,995	32
8520-C	With 32K bytes of MOS memory	2,360	36
8520-D	With 64K bytes of MOS memory	2,940	40
8520-E	With 8K bytes of MOS memory and sockets for 32K bytes of EPROM	1,995	—
8520-F	Same as 8520-E except 32K bytes of memory	2,570	—
MP/200 computers include an MP/200 System Processing Unit, 8-slot chassis, microNova instruction set plus load/store byte operations and signed multiply/divide, asynchronous console interface, real-time clock, soft control panel with auto load, and power fail/auto restart.			
8670-B	With 16K bytes of MOS memory	2,940	42
8670-C	With 32K bytes of MOS memory	3,300	46
8670-D	With 64K bytes of MOS memory	3,885	50

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EQUIPMENT PRICES

		Purchase price in quantities of: 1-9	10-24	25-49
The MBC/1 single-board computer includes 2K bytes of MOS memory, sockets for 4K bytes of PROM, asynchronous interface, 32-line digital I/O interface				
8320	MBC/1 single-board computer	$725	$638	$565
8318-A	MBC/1 console bebug and diagnostics option supplied on 2 512K-byte PROM's	90	—	—
The MBC/2 and MBC/3 single-board computers include sockets for 1K PROM and 32K EPROM, 2 asynchronous/synchronous interfaces, and 32-line digital I/O interface				
8321	MBC/2 with 8K bytes of MOS memory	725	—	—
8322	MBC/3 with 32K bytes of MOS memory	1,200	—	—
The MBC/SDX single-board computer includes 2 asynchronous/synchronous interfaces and 32-line digital I/O interface				
8323	MBC/SDX	600	—	—
MP/100 microcomputers include the MP/100 SPU board and memory on two boards				
8521-A	With 8K bytes of MOS memory	850	745	660
8521-B	With 16K bytes of MOS memory	1,000	877	778
8521-C	With 32K bytes of MOS memory	1,400	1,235	1,095
8521-D	With 64K bytes of MOS memory	1,950	1,709	1,515
8521-E	With 8K bytes of MOS memory	1,100	968	858
8521-F	Same as 8521-E except 32K bytes of MOS memory	1,600	1,412	1,252
MP/200 microcomputers include the MP/200 SPU board and memory on two boards				
8671-B	With 16K bytes of MOS memory	1,450	1,271	1,127
8671-C	With 32K bytes of MOS memory	1,800	1,585	1,405
8671-D	With 64K bytes of MOS memory	2,400	2,118	1,878
PROCESSOR OPTIONS				
8521-G	MP/100 SPU board	800	702	622
8676	MP/200 controller board with asynchronous interface, virtual console with auto load, real-time clock, and power fail/auto restart	600	528	468
4310/1	8-slot chassis with mounting box, fans, and power supply	1,000	880	780
4312	4-slot card cage with back panel and lugs for power supply	180	158	140
4313	Power supply board	550	484	429
4207	Asynchronous interface board for teleprinters and CRT's	260	—	—
4208	Console debug option	200	—	—
4210	General-purpose interface card	250	—	—
1112D	I/O bus cable	100	—	—

		Purchase Price	On-Call Service
4210	General purpose interface card accomodates I/O controller circuitry, logic for programmed I/O, program interrupt, and DMA interface	$250	—
4211	Interface Card Wire Wrap Pins and Sockets	200	—
2303	Circuit Card Extender	200	—
MEMORY			
8522	8K-byte MOS RAM board (not MP/200)	420	8
8523/8673	16K-byte MOS RAM board	575	12
8524/8674	32K-byte MOS RAM board	1,050	16
8525/8675	64K-byte MOS RAM board	1,940	20
8317	PROM socket board for up to 16K bytes of PROM (not MP/200)	200	—
8680	8K bytes of RAM, sockets for up to 32 bytes of PROM (not MP/200)	630	—
8681	Same as 8680 except 32K bytes of RAM	1,260	—
MASS STORAGE			
6038	Single-drive 315K-byte diskette subsystem with controller	2,900	33
6039	Same as 6038 except dual drive	3,900	40
6095-N	DG/Cartridge disk drive, F/R 10 megabytes with controller	9,800	78
6101	DG/Disk Storage Subsystem; includes 12.5-megabyte disk pack drive, 1.26 megabyte diskette drive, and controller	7,300	70
6102	Same as 6101 without diskette	5,200	39
6104	Same as 6101 except 25-megabyte disk pack	10,200	78
6105	Same as 6101 without diskette	8,100	47

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EQUIPMENT PRICES

		Purchase Price	On Call Service
PAPER TAPE EQUIPMENT			
4220	Paper tape reader control for 6013 reader	400	6
6013	High speed paper tape reader, 400 cps, fanfold, 8-channel tape	1,150	16
TERMINALS			
6042	Dasher terminal printer, 30 cps, KSR	2,400	25
6043	Dasher terminal printer, 30 cps, RO	2,200	23
6040	Dasher terminal printer, 60 cps, KSR	2,650	28
6041	Dasher terminal printer, 60 cps, RO	2,450	26
6052	CRT; 24 lines by 80 characters, 5 x 7 dot matrix, 64-char. set; to 19.6K bps	2,190	20
6053	CRT; 24 lines by 80 characters, 5 x 8 dot matrix, 96-char. set; additional features such as blink and underscore; to 19.6K bps	2,650	20
6106	Dasher D/100 CRT; 24 lines x 80 characters, 7 x 11 dot matrix, 96-character set, 9600 bps	1,750	18
6107	Same as 6106 plus printer interface, split baud option	2,150	23
6108	Dasher D/200 CRT; 24 lines x 80 characters, 7 x 11 dot matrix, 96-character set, 9600 bps	1,950	19
6109	Same as 6108 plus printer interface, split baud option	2,350	24
6073	Dasher LP2 line printer; 180 cps	3,250	34
6075	Dasher TP2 terminal printer, 180 cps, RO	3,550	34
4221	Printer controller for 6073, 6075	650	11
COMMUNICATIONS			
4220	Programmable Real-Time Clock	350	5
4225	Controller board for 4226 and 4227 controllers	350	4
4226	Programmable synchronous controller; maximum of 4 per 4225	400	5
4227	Programmable 4-line asynchronous controller; maximum of 4 per 4225	500	7
4300	DAC chassis; includes 16 I/O card slots with control card to support data acquisition and control sensor I/O subsystem modules	2,200	16
4228	CRC Generator	250	4
4222	Digital I/O interface; provides 16 input lines with strobe	400	6
4223	A/D Converter	1,150	11
4224	Analog voltage output module; includes 2 D/A converters	800	9
CABINETS AND HARDWARE			
1144	Bay with 19" rack cabinet; 60" x 30" x 25"	1,300	—
1148	Half bay	500	—