

ARCNET®

Transceiver Chip

FEATURES

- Works with NCR90C26 to transfer data at 2.5 Megabits per second
- Outputs the special clock signals required by the NCR90C26
- Generates output in NRZ format from incoming LAN data
- Provides two general purpose 4 MHz clock outputs for CPU interface
- Generates dual-pulse output signals for data transmission out to LAN
- Provides special 5 MHz clocks required by the Controller chip

INTRODUCTION

The NCR90C32 AT (ARCNET Transceiver) is a flexible data handling device that interfaces an NCR90C26 ARCNET Controller chip to special cable driving and receiving circuitry. Directed by a host microprocessor, these components comprise a node in an ARCNET Local Area Network. The main function of the NCR90C32 is to convert data between a NRZ format on the host side and dual-pulse on the cable side. The only additional component required by the AT is a 20 MHz clock oscillator.

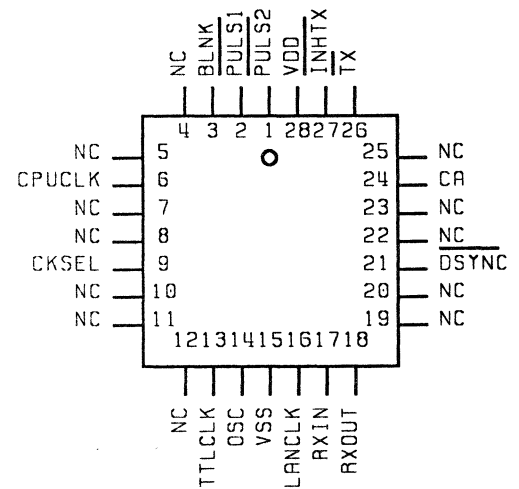
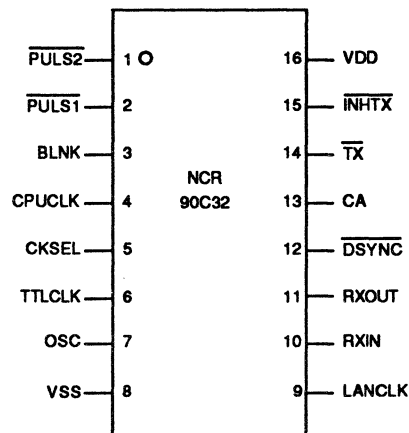


Figure 1 16-pin DIP and 28-pin PLCC

Symbol	Pin No.		I/O	Name and Function
	16-pin DIP	28-pin PLCC		
OSC	7	14	I	OSCILLATOR: 20 MHz input signal.
CKSEL	5	9	I	CLOCK SELECT: Chooses the clock options for the extra TTLCLK and CPUCLK pins. When CKSEL is high, the two extra clocks both output a constant four MHz derived from the OSC signal. When CKSEL is low, then CPUCLK outputs the inverse of the input on TTLCLK.
LANCLK	9	16	O	NETWORK CLOCK: A free-running 5 MHz clock used for timing of 90C26 bus cycles and other functions.
CA	13	24	O	AUXILIARY CLOCK: A gated 5 MHz clock used to control data transfers of the NCR90C26. CA is periodically halted by $\overline{\text{DSYNC}}$ and restarted by RX.
TTLCLK	6	13	I/O	TTL CLOCK: May be either input or output. See description for CKSEL above.
CPUCLK	4	6	O	CPU CLOCK: An additional clock output. See description for CKSEL.
$\overline{\text{TX}}$	14	26	I	TRANSMIT DATA: Serial data input to the AT for conversion and transmission over the LAN.
$\overline{\text{PULSE1}}$, $\overline{\text{PULSE2}}$	2, 1	2, 1	O	PULSE1 & PULSE2: These outputs are nonoverlapping negative going pulses that are asserted to the cable circuitry for every active pulse detected at TX. PULSE1 is the first, and PULSE2 is the second pulse in this dual-pulse process.
$\overline{\text{RXIN}}$	10	17	I	RECEIVE DATA IN: Serial input data from the LAN.
$\overline{\text{DSYNC}}$	12	21	I	DELAYED SYNC: This signal is asserted by the NCR90C26 to cause the AT to halt the CA clock.
RXOUT	11	18	O	RECEIVED DATA OUT: An NRZ form of the serial data input at the RXIN pin.
$\overline{\text{INH TX}}$	15	27	I	TRANSMIT INHIBIT: A Power-Reset input. $\overline{\text{INH TX}}$ active forces PULSE1 and PULSE2 high and BLNK low. These actions block the TX input from causing transmissions on the LAN.
BLNK	3	3	O	BLANK: A delayed and shortened version of $\overline{\text{TX}}$. This signal should be left unconnected when used in a typical circuit such as that on page 3.
VDD	16	28		+5 VOLT SUPPLY
VSS	8	15		GROUND

DESCRIPTION

The primary job of the NCR90C32 AT is to format data and synchronize transfers over the ARCNET node to which it is attached. The LANCLK output to the NCR90C26 Controller device assures that all transactions between the two chips are synchronous. The analog cable circuit converts all dipulses (logic ones) received on the LAN to single positive pulses on the RXIN pin into the AT. This data, after some delay, is converted into NRZ format and sent to the NCR90C26 device. After a full byte has been transferred, the NCR90C26 will

assert $\overline{\text{DSYNC}}$, which halts the CA clock. When the AT detects the first bit of the next byte, it will restart CA. The CA signal is used by the NCR90C26 to sample the levels on RXOUT at the times indicated in the timing diagrams. For outward transmissions, the NCR90C26 puts active-low pulses 200ns in duration on $\overline{\text{TX}}$ for every logic one it sends. Each of these active-low pulses is converted to two 100ns wide, nonoverlapping, active-low pulses on the $\overline{\text{PULSE1}}$ & $\overline{\text{PULSE2}}$ outputs. These signals will drive the cable circuitry to create the dipulse that signifies logic one on the LAN cable itself.

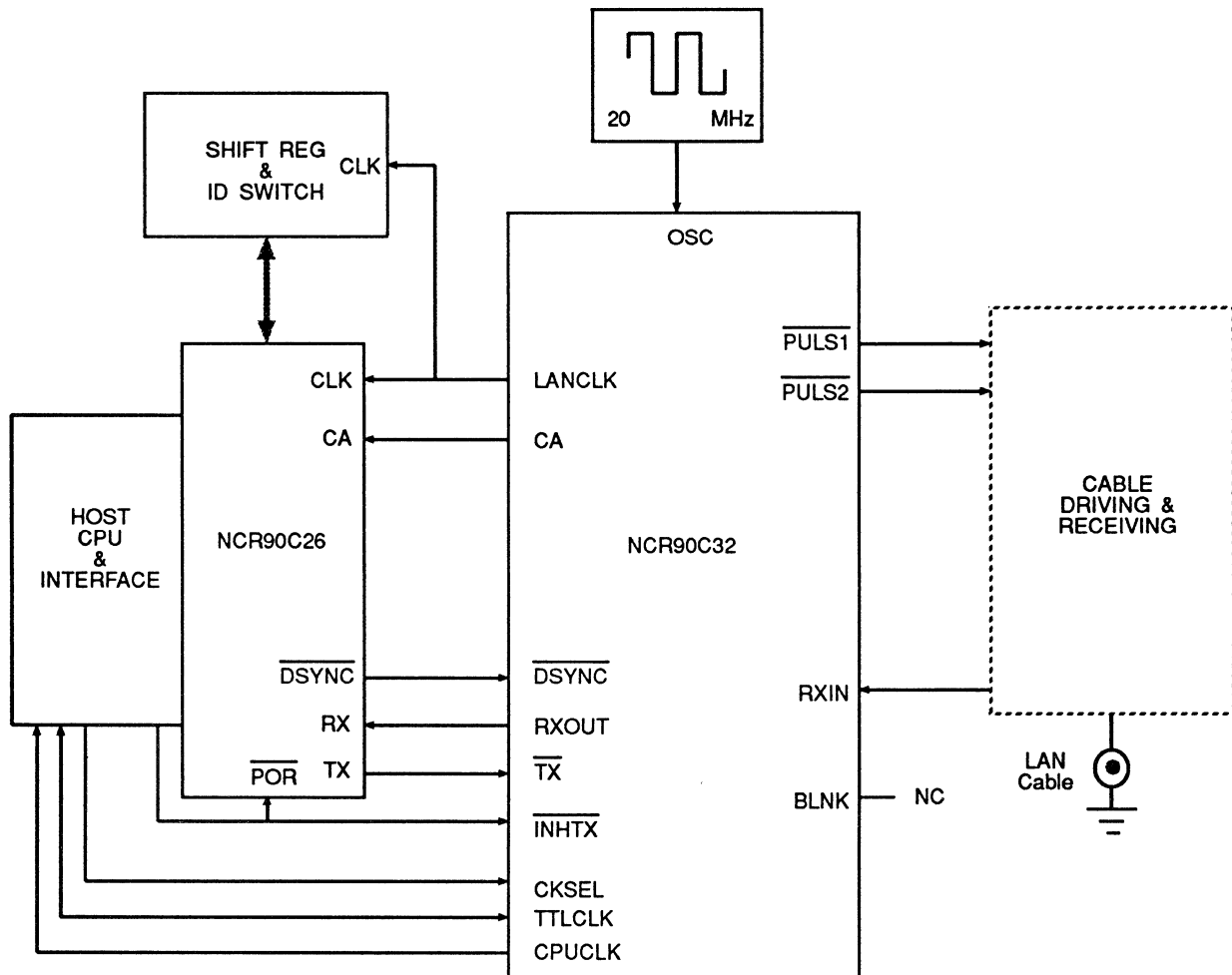


Figure 2 Typical NCR90C32 Hookup

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM STRESS RATINGS

Voltage on VDD pin with respect to Vss.....-0.3 to +7.0V

Voltage on any signal pin.....-0.3 to V_{DD} +0.3

Power Dissipation.....53 mW

Operating Temperature Range.....0°C to 70°C

Storage Temperature Range.....-65°C to +150°C

The values listed above are absolute maximums which, if exceeded, could cause permanent damage to the device. Voltages are with respect to circuit ground.

DC Characteristics

Symbol	Parameter	Min	Max	Units
V _{IL}	Input Voltage, Low (all inputs)	-0.3	0.8	V
V _{IH}	Input Voltage, High (all inputs)	2.7	V _{DD} +0.3	V
I _{OHX}	Transfer Output High Current (@ V _{OH} max=0.4V) PULS1, PULS2, RXOUT, and TTLCLK outputs for:		-400	μA
I _{OLX}	Transfer Output Low Current (@ V _{OL} max=0.4V) PULS1, PULS2, RXOUT, and TTLCLK outputs for:		+4.0	mA
I _{OHK}	Clock Output High Current (@ V _{OH} min=V _{DD} -0.5) for: CA, LANCLK, and CPUCLK		-100	μA
I _{OLK}	Clock Output Low Current (@ V _{OL} max=0.4V) for: CA and LANCLK		+400	μA
I _{OLU}	Output Low Current (@ V _{OL} max=0.4V) for: CPUCLK		+100	μA
C _{IN}	Input Capacitance		30	pF
I _{IT}	Input Leakage Current (TTLCLK pin as Input)		±50	μA
I _I	Input Leakage Current (all other inputs)		±10	μA
I _{DD}	Power Supply Current (V _{DD} =5.25V)		10	mA

Notes: All parameters are assured over the 0°C to 70°C temperature range and with 4.75≤V_{DD}≤5.25 Volts.
All voltages are with respect to circuit ground (V_{SS}).

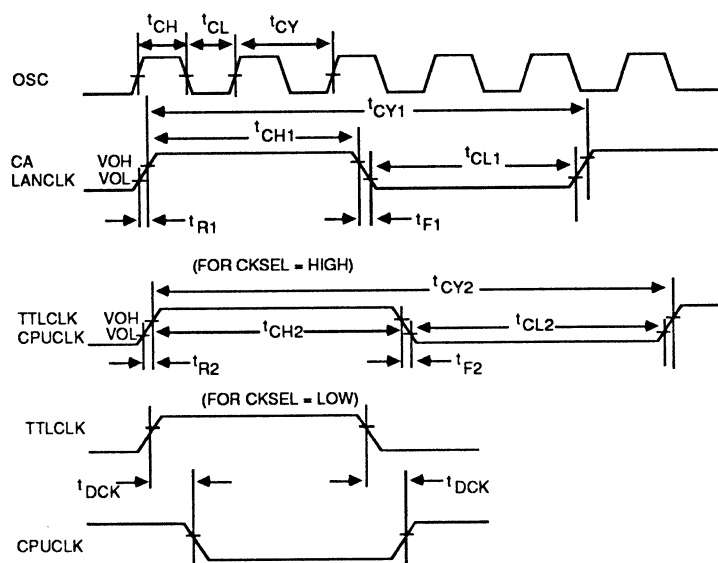


Figure 3 Clock Timing Parameters

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CH}	High Duration of OSC	20			ns
t_{CL}	Low Duration of OSC	20			ns
t_{CY}	Period of OSC		50		ns
t_{CH1}	High Duration of NCR90C26 Clocks	75			ns
t_{CL1}	Low Duration of NCR90C26 Clocks	75			ns
t_{CY1}	Period of NCR90C26 Clocks		200		ns
t_{R1}	Rise Time of NCR90C26 Clocks			20	ns
t_{F1}	Fall Time of NCR90C26 Clocks			20	ns
t_{CH2}	High Duration of Extra Clocks	110			ns
t_{CL2}	Low Duration of Extra Clocks	110			ns
t_{CY2}	Period of Extra Clocks		250		ns
t_{R2}	Rise Time of Extra Clocks			30	ns
t_{F2}	Fall Time of Extra Clocks			30	ns
t_{DCK}	CPUCLK Delay from TTLCLK Edges			45	ns

Note: All timings in this specification are taken from the 10% & 90% points with respect to the specified VOL & VOH of the waveforms.

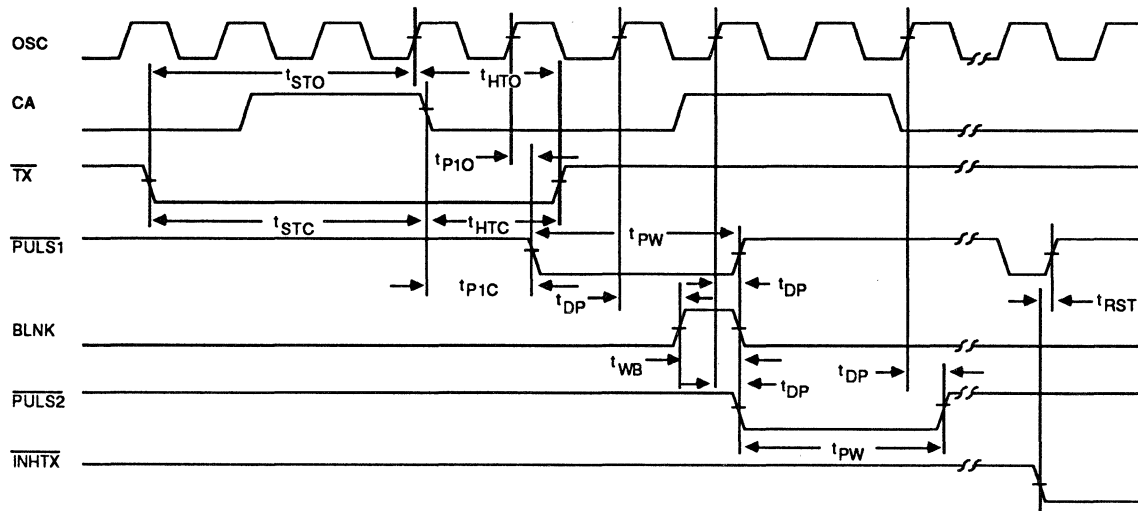


Figure 4 Transmit Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{STC}	\overline{TX} Setup to CA Falling Edge		10		ns
t_{STO}	\overline{TX} Setup to OSC Rising Edge	10			ns
t_{HTC}	\overline{TX} Hold after CA Falling Edge		10		ns
t_{HTO}	\overline{TX} Hold after OSC Rising Edge	10			ns
t_{P1C}	PULS1 Delay after CA Falling Edge	60			ns
t_{P1O}	PULS1 Delay after OSC Rising Edge			60	ns
t_{DP}	PULSE & BLNK Edge Delays after OSC Rising Edge			60	ns
t_{PW}	Duration of the two PULSE Signals		$2t_{CY}$		ns
t_{WB}	Pulse Duration for BLNK		t_{CY}		ns
t_{RST}	PULS1 Turnoff from \overline{INHTX} Falling Edge			40	ns

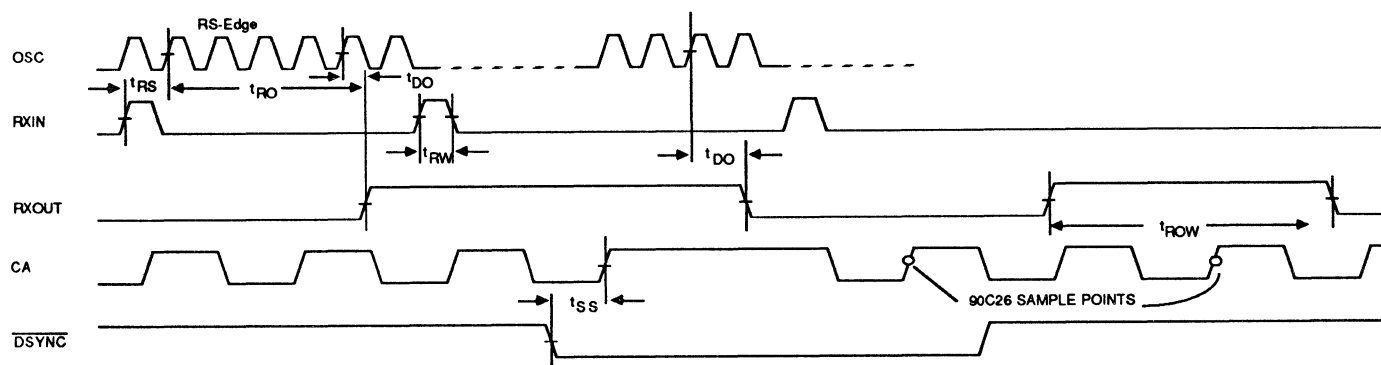


Figure 5 Receive Timing

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RS}	RXIN Setup to RS-Edge	10			ns
t_{RW}	RXIN Active Duration	10			ns
t_{DO}	RXOUT Delay from OSC Rising Edge			70	ns
t_{RO}	RXOUT Active after RS-Edge		$5t_{cv} + t_{DO}$		ns
t_{SS}	CA Turnoff after \overline{DSYNC}	10	20		ns
t_{ROW}	RXOUT Isolated '1' Duration		400		ns

SALES INFORMATION

For more information on the NCR92C32, or any other Communications Group device, please call the NCR hotline at

1 - 800 - 334 - 5454

or contact your local NCR Sales Representative or one of the following NCR Sales Offices.

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