NCR ARCNET® CONTROLLER/TRANSCEIVER

With PC AT Bus Interface

FEATURES

- Only twelve support chips needed to implement a 16-bit ARCNET node which is a reduction of 25 chips from a NCR90C26-based, 16-bit card
- Includes IBM PC AT interface
- Typical 2 wait states with 10MHz bus clock vs. 7 to 18 wait states for existing solutions
- Supports three reset options
  - Power-On-Reset
  - External Reset
  - Software Generated Reset
- 20MHz on-chip oscillator
- Includes RAM, ROM and I/O decoding
- Only one ROM needed for 16-bit compatibility
- Software compatible with the NCR90C26/NCR90C98
- Diagnostic routine for duplicate ID
- Duplicate ID status bit
- I/O and memory mapped registers
- Fully controls 8K of external SRAM
- Supports buffer chaining in external RAM
- Supports dual port memory
- 68-pin PLCC package

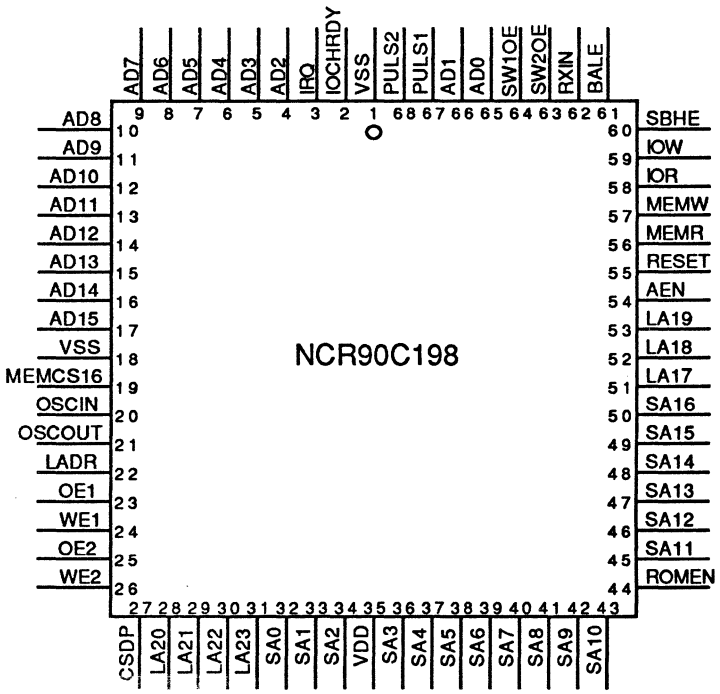

Figure 1 68-pin PLCC diagram

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Pinout Summary

Signal Name	Type	Pin No.	Pin Description
V_{SS}	Ground	1	Ground
IOCHRDY	Output	2	I/O channel ready
IRQ	Output	3	Interrupt request
AD2	In/Out	4	Mux address/data bus pin
AD3	In/Out	5	Mux address/data bus pin
AD4	In/Out	6	Mux address/data bus pin
AD5	In/Out	7	Mux address/data bus pin
AD6	In/Out	8	Mux address/data bus pin
AD7	In/Out	9	Mux address/data bus pin
AD8	In/Out	10	Mux address/data bus pin
AD9	In/Out	11	Mux address/data bus pin
AD10	In/Out	12	Mux address/data bus pin
AD11	In/Out	13	Mux address/data bus pin
AD12	In/Out	14	Mux address/data bus pin
AD13	In/Out	15	Mux address/data bus pin
AD14	In/Out	16	Mux address/data bus pin
AD15	In/Out	17	Mux address/data bus pin
V_{SS}	Ground	18	Ground
MEMCS16	Output	19	Memory Card Select 16
OSCIN	Input	20	Oscillator & clock input
OSCOUT	Output	21	Oscillator output
LADR	Output	22	Latch address
OE1	Output	23	Output enable 1
WE1	Output	24	Write enable 1
OE2	Output	25	Output enable 2
WE2	Output	26	Write enable 2
CSDP	Output	27	Dual Port Chip Select
LA20	Input	28	I/O channel address bus pin
LA21	Input	29	I/O channel address bus pin
LA22	Input	30	I/O channel address bus pin
LA23	Input	31	I/O channel address bus pin
SA0	Input	32	System address bus pin
SA1	Input	33	System address bus pin
SA2	Input	34	System address bus pin
V_{DD}	Power	35	+5 volt supply
SA3	Input	36	System address bus pin
SA4	Input	37	System address bus pin
SA5	Input	38	System address bus pin
SA6	Input	39	System address bus pin
SA7	Input	40	System address bus pin
SA8	Input	41	System address bus pin
SA9	Input	42	System address bus pin
SA10	Input	43	System address bus pin
ROMEN	Output	44	ROM enable

Pinout Summary

Signal Name	Type	Pin No.	Pin Description
SA11	Input	45	System address bus pin
SA12	Input	46	System address bus pin
SA13	Input	47	System address bus pin
SA14	Input	48	System address bus pin
SA15	Input	49	System address bus pin
SA16	Input	50	System address bus pin
LA17	Input	51	I/O channel address bus pin
LA18	Input	52	I/O channel address bus pin
LA19	Input	53	I/O channel address bus pin
AEN	Input	54	Address enable
RESET	Input	55	Reset
MEMR	Input	56	Memory read command
MEMW	Input	57	Memory write command
IOR	Input	58	I/O read command
IOW	Input	59	I/O write command
SBHE	Input	60	Byte high enable
BALE	Input	61	Address latch enable
RXIN	Input	62	Receive data in
SW2OE	Output	63	Switch 2 output enable
SW1OE	Output	64	Switch 1 output enable
AD0	In/Out	65	Mux address/data bus pin
AD1	In/Out	66	Mux address/data bus pin
PULS1	Output	67	Pulse 1 (transmitter out)
PULS2	Output	68	Pulse 2 (transmitter out)

GENERAL DESCRIPTION

The NCR90C198 Controller/Transceiver includes all logical functions of an ARCNET RIM (Resource Interface Module) plus an economical PC AT interface. See Figure 2. The 1.5 micron CMOS technology increases the level of integration, improves the performance and lowers the power consumption of the NCR90C198. ARCNET is a popular token-passing Local Area Network (LAN) scheme developed by Datapoint Corporation. The NCR90C198 handles all tasks for transferring data between the node and the LAN. It reads from and writes to Message Buffers in an external RAM, it initiates and responds to valid ARCNET transmissions, and it passes control between itself and the other RIMs on the network. The NCR90C198 also contains the interface to the cable-driving circuitry that connects to the physical LAN media.

The NCR90C198 consists of an ARCNET controller, ARCNET transceiver, on-chip oscillator, and an IBM PC AT interface. See Figure 3. A reduction of 25 support chips from a NCR90C26-based card can be achieved when implementing an ARCNET node on a PC AT compatible bus using the NCR90C198.

The NCR90C198-based ARCNET LAN requires only 2 to 3 additional wait states with PC AT buses up to 10MHz. Products other than the NCR90C198 require from 7 to 18 additional wait states from the PC AT bus to transfer the same data.

Both dual port and standard memory are supported with the NCR90C198. This chip controls up to 8K bytes of external buffer RAM.

The Token Received status bit is a diagnostic tool that enables the node to confirm its connection to the network. This bit allows the communication software to confirm that the token has been received and the node is connected to the network.

The NCR90C198 has a unique diagnostic routine to identify duplicate node IDs on an ARCNET LAN. If there is already a node on the network with that ID, the duplicate ID status bit is set. Without this diagnostic routine, the network would be in a constant state of reconfiguration when duplicate node IDs exist.

Buffer chaining improves the network performance especially in file server applications. When buffer chaining is enabled, the automatic receive function allows the receive buffer to accept multiple packets of data without interrupting the host between each reception. When transmitting, buffer chaining allows one command to enable the transmission of multiple packets without host intervention. Buffer chaining reduces overhead, and has improved system throughput by 20 to 80 percent depending on the specific hardware and software.

The NCR90C198 provides the ability to upgrade performance as needed. It is backward software compatible with the NCR90C26 and defaults to this mode of operation. Changing to the NCR90C98 mode after initialization allows the node to support buffer chaining.

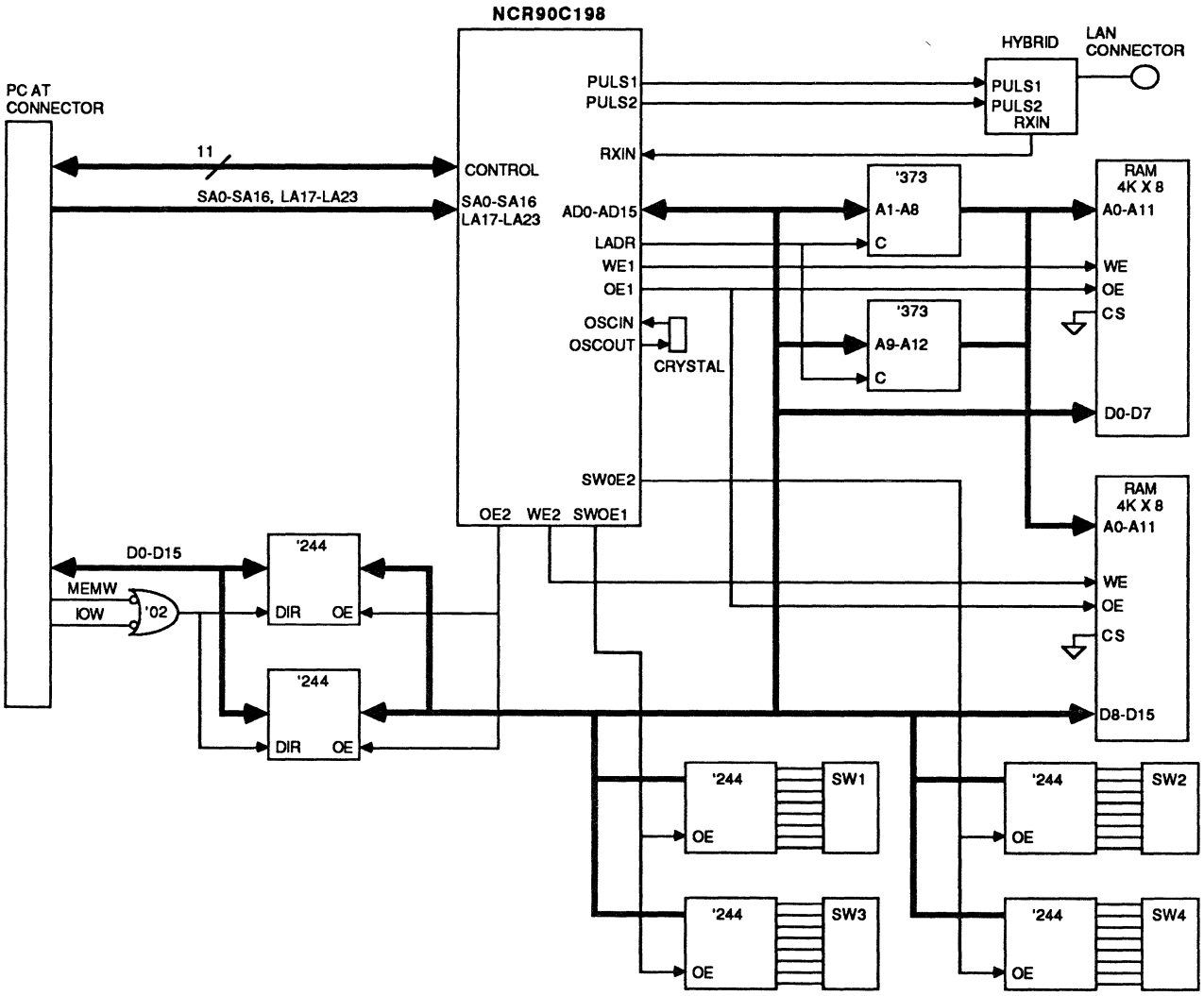


Figure 2 Minimum System Configuration Block Diagram

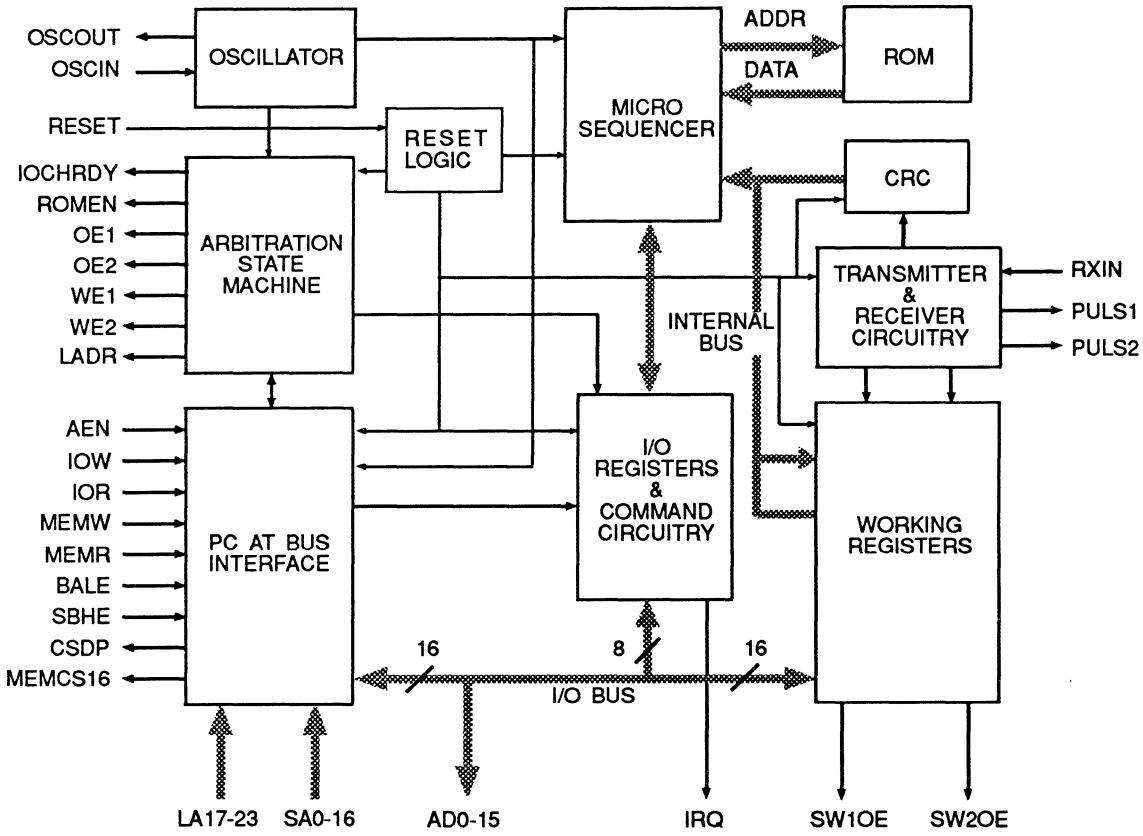


Figure 3 Chip block diagram

ARCNET OVERVIEW

LINE PROTOCOL

The NCR90C198 implements an asynchronous line protocol, with each Information Symbol Unit (ISU) consisting of the following:

- 2 clock units of mark (logic 1)
- 1 clock unit of space (logic 0)
- 8 clock units of data

A single clock unit is 400 nanoseconds in duration, so a byte of data is transmitted every 4.4 (400 ns x 11 clock units) microseconds. Thus, the time to transmit any message can be determined exactly. All transmissions start with an ALERT BURST, which is 6 clock units of mark. The line idles in a spacing condition. The five types of ARCNET transmissions follow:

Invitations To Transmit

An ALERT BURST followed by three ISUs: one EOT (End of Transmission) and two repeated DID (Destination IDentification) ISUs. This message passes control (the "token") from one node to another.

Free Buffer Enquiries

An ALERT BURST followed by three ISUs: one ENQ (ENQuiry) and two repeated DID ISUs. This message asks another node if it is able to accept a message packet.

Packets

An ALERT BURST followed by 8 to 516 ISUs:

- one SOH (Start Of Header) ISU
- one SID (Source IDentification) ISU
- two repeated DID ISUs
- two CRC (Cyclic Redundancy Check) ISUs
- one sytem code ISU
- from 0 to 507 data ISUs
- an inverse COUNT ISU = 256-N, for N data ISUs to be sent

Acknowledgments

An ALERT BURST followed by a single ACK (ACKnowledgment) ISU. This message is used as a positive response to FREE BUFFER ENQUIRIES, and also to acknowledge the valid reception of a PACKET.

Negative Acknowledgments

An ALERT BURST followed by a single NAK (Negative AcKnowledgment) ISU. This message gives a negative response to FREE BUFFER ENQUIRIES.

Line Protocol Notes:

- The codes (all in HEX) for the special ISUs mentioned above follow.
  - EOT - 04
  - ENQ - 85
  - SOH - 01
  - ACK - 86
  - NAK - 15
- The COUNT ISU for PACKETS may be equal to (512 - N) if a "long packet" is being sent. The CRC polynomial used for data packets is: $X^{16} + X^{15} + X^2 + 1$.
- As a receiving node, the NCR90C198 will verify all incoming transmissions by checking for:
  - At least one mark and exactly one space preceding each byte.
  - A valid EOT, ENQ, SOH, ACK, or NAK following the ALERT BURST.
  - Proper CRC for data packets.
  - Correct number of bytes, depending on the transmission

NETWORK CONTROL

All nodes in an ARCNET system are distinguished by a unique 8 bit ID (IDentification) value. This value is configurable with DIP switches associated with each NCR90C198 chip. An ID of '0' may not be assigned to any node, since that ID indicates a BROADCAST to all nodes. Control of the Local Area Network (LAN) is based on token passing. In order to send a message, a node must first receive the token. The token is received in an INVITATION TO TRANSMIT message containing its own ID. To send a message, the host processor loads the message data and the destination ID into its NCR90C198's buffer RAM. Then the host writes an "Enable Transmit" command to the NCR90C198. The NCR90C198 will know it has a message to send if the TA (Transmitter Available) bit in its Status Register is LOW. When the NCR90C198 has the token, it then transmits a FREE BUFFER ENQUIRY to the destination ID to see if it is able to receive the message. If the destination is able to receive, it transmits an ACK back to the controlling node. The controlling node then transmits the PACKET, complete with a 16-bit CRC. If there is no activity after sending this message, a "time out" (74.7 µs) occurs (see *Timecheck Function* Section). Upon Timeout, the NCR90C198 sets its TA bit, and passes the token. When an NCR90C198 receives the token, but its TA bit is high (it has no message to send), it sends an INVITATION TO TRANSMIT to pass the token.

When an NCR90C198 is sent a FREE BUFFER ENQUIRY, it will poll its RI (Receiver Inhibited) Status bit. If the RI bit is set, the NCR90C198 will transmit a NAK, and the controlling node will then pass the token. If an NCR90C198 with a packet to send gets a NAK, then it will pass the token and re-transmit a FREE BUFFER ENQUIRY the next time it receives the token. If there is no activity on the line within 74.7 µs of transmitting a FREE BUFFER ENQUIRY a time out occurs (see *Timecheck Function* Section). The NCR90C198 increments its NID (Next ID) pointer and tries again. After it has sent a PACKET, an NCR90C198 waits a specified response time. If within that time, it receives an ACK, it sets both the TMA (Transmit Message Acknowledged) and the TA Status bits and passes the token. If it does not receive an ACK in time, it only sets TA and then passes the token.

All nodes recognize a PACKET when they see the SOH ISU, and all NCR90C198s will write the SID into their Receive Buffers. If an NCR90C198 perceives the first DID as its own, or the PACKET is a Broadcast message (see the *Reconfiguration and Broadcast* section), the chip will write the second DID and the rest of the message into its Receive Buffer. Otherwise, the NCR90C198 will ignore the rest of the PACKET. After the PACKET has been fully received, it must pass three conditions to be considered a valid message:

- the CRC comparison
- correct length of ISUs, and
- valid DID in byte 0 of the Receive Buffer.

Valid DIDs are either '0' (indicating Broadcast), or the NCR90C198's own ID. An ACK is sent if a message is valid by these conditions and addressed to the NCR90C198's own ID. However if the message is a broadcast message no ACK will be sent. The NCR90C198 sets its RI status bit after receiving a valid message if no more receive buffers are available. In the buffer chaining mode, the Received Packet (RP) status bit is set when a valid message is received addressed to the NCR90C198's own ID. If any of the conditions fail, the NCR90C198 ignores the message and will write over it with future PACKETS.

RECONFIGURATION AND BROADCAST

There are two activities that involve all nodes on the ARCNET system. These are Reconfiguration of the system and Broadcasts to the system.

A **Reconfiguration** of the network is performed any time a node is removed from, or added to the system. Specifically, an NCR90C198 will instigate a Reconfiguration when it is first powered on, or when it has not received an INVITATION TO TRANSMIT within 840 milliseconds. It does this by transmitting a RECONFIGURATION BURST: 8 marks and 1 space repeated 765 times. This burst has the effect of terminating all activity on the network. This burst is longer than all the other types of transmissions. Thus, it will interfere with the next INVITATION TO TRANSMIT, destroying the token and no other node will take control of the line. The RECONFIGURATION BURST also provides enough line activity so the NCR90C198 that just sent the token will also release control of the network.

When any NCR90C198 sees the line idle for 78 µs it begins a network reconfiguration cycle. It sets the internal NID (Next ID) register to its own ID. The NID is normally the DID sent with an INVITATION TO TRANSMIT. Besides resetting the NID, the NCR90C198 also starts a timeout of 146 µs times the quantity 255 minus its own ID [146 µs x (255-ID #)]. If this timeout expires with no other line activity, the NCR90C198 will start transmitting INVITATIONS TO TRANSMIT with the DID pointing to itself. Only the NCR90C198 with the largest ID value will actually timeout.

After sending an INVITATION TO TRANSMIT, the NCR90C198 will look for any line activity, indicating that the DID is a valid node. If the sending NCR90C198 detects no activity after 74.7 µs, it increments its NID, and sends another INVITATION. Eventually, the NCR90C198 with the ID that is next will see its ID in the INVITATION and take control of the line. The previous NCR90C198 will then have its NID set correctly. The process repeats with the end result showing each NCR90C198 with a NID stored representing an active node to pass the token. The token is not sent to nonexistent nodes. If a node is removed from an active network, then the previous node will time out when passing the token. The previous NCR90C198 goes through a cycle of incrementing its NID and transmitting INVITATIONS TO TRANSMIT until it finds the next valid node. The total time to perform a Reconfiguration will vary depending on the system configuration, but is typically between 24 and 61 ms.

A **Broadcast** Packet is the second operation that pertains to all the nodes in the network. A PACKET is considered to be Broadcast if the DID is a value of '0'. No regular node may be assigned the Broadcast ID. Nodes are set up to receive Broadcasts by issuing a "Write Configuration" command with the most significant bit of the command set to '1'. All NCR90C198 commands are described in the *Command Register* sections.

TIMECHECK FUNCTIONS

A standard baseband system using RG-62 coax cable (the ARCNET standard) can take up to 31µs for a one-way propagation. This corresponds to a distance of about 4 miles. The maximum turn-around time that any NCR90C198 takes to respond to an incoming message is 12µs. A maximum Response Time for any transmission is 31 + 31 + 12 = 74µs. To allow a margin, the NCR90C198 uses 74.7 µs as its basic Response Timeout. This is the interval a controlling node expects to perceive any line activity after it makes a transmission.

An IDLE Timeout is the interval that transpires at the onset of a Reconfiguration. After the RECONFIGURATION BURST, all the nodes commence the Reconfiguration process when they detect no line activity for the Idle timeout. In a standard network, the Idle timeout is 78.2µs. The TRANSFER timeout is the ID-dependent interval associated with Reconfiguration. This timeout is given by 146 µs x (255-ID), and it transpires only for the node with the highest ID on the network. The last timeout is the interval that instigates a Reconfiguration. In a standard network, if any node has not received an INVITATION TO TRANSMIT within a Reconfiguration timeout of 840 ms, it issues a RECONFIGURATION BURST and starts a network Reconfiguration.

Table 1 Timeout Response and Reconfiguration Settings

ET2	ET1	Response Timeout	Reconfiguration Timeout
1	1	74.7 µs	0.84 seconds
1	0	283.4 µs	1.68 seconds
0	1	561.8 µs	1.68 seconds
0	0	1118.6 µs	1.68 seconds

The timeout values in Table 1 apply to a standard, or "basic" network with no 2 nodes farther apart than 4 miles. The network may operate over longer distances by appropriate setting of the ET1 and ET2 inputs. Table 1 shows the effect of ET1 and ET2 on two of the more pertinent timeouts. It is important that ET1 and ET2 be set to the same value for all nodes on the network.

HOST INTERFACE OVERVIEW

The NCR90C198 contains a full-featured PC AT bus interface. In a minimal configuration, only twelve integrated circuits are required to build a fully functional board (see Figure 2). Additions to the minimal system supported by the NCR90C198 are on-board ROM, LAN Driver disable, and hardware for dual port RAM. More information is available in the *DETAILED HOST INTERFACE DESCRIPTION* on page 18.

PC AT Interface

All transactions on the NCR90C198 board are controlled by the NCR90C198. Accesses to the NCR90C198 internal registers can be accomplished by I/O commands or memory commands. Access to the RAM buffer memory and/or the on-board ROM goes through the NCR90C198 and the multiplexed address/data bus. The NCR90C198 also uses the multiplexed address/data bus to store and retrieve data that is received and transmitted over the LAN.

I/O and Memory Accesses

The host has the option of accessing the registers within the NCR90C198 with an I/O command or with a memory command. With I/O commands the registers are mapped into a 16 address space in the I/O map. When accessing the registers with a memory command the registers appear in the 16 highest addresses in the ROM memory map. When SA13 is high, the ROM memory map is accessed. When SA13 is low, the RAM memory map is accessed. See Figure 4.

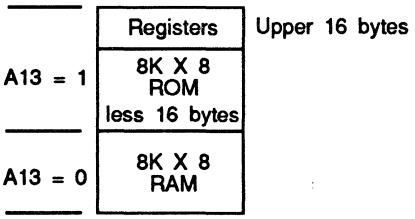


Figure 4 Memory Map

LAN Driver Control

The NCR90C198 supports the enabling and disabling of the LAN driver by receiving the LAN Driver Enable/Disable command issued from the host. See Command Register 3 for the NCR90C98 mode on page 13.

Dual Port Memory

Dual port memory is supported to offer faster system speed. When the dual port memory is enabled, no arbitration takes place on the multiplexed address/data bus.

FUNCTIONAL DESCRIPTION

Software Operating Modes (C26 and C98)

The NCR90C198 supports two software operating modes. The first is the NCR90C26 mode and the second is the NCR90C98 mode. In the NCR90C26 mode, the chip is programmed the same as the NCR90C26.

The NCR90C198 powers-up in the NCR90C26 mode. The power-on routine within the NCR90C198 writes the NCR90C26 hex signature D1 to address 0 in the buffer memory. When the host CPU writes to Command Register 2, the NCR90C198 switches to the NCR90C98 mode. All bits in Command Register 1 take on the new functions of the NCR90C98 mode. The chip must be reset (Power-on, Reset Signal or Reset Command) to switch back to the NCR90C26 mode.

BUFFER CHAINING

This feature relieves the host from the task of enabling a new receive buffer for each packet received. It also lets the host transmit multiple packets per transmit command.

Packet Reception

In the receive buffer chaining mode, the NCR90C198 automatically fills all the pages that are assigned to the receive buffer. If the circular mode is enabled, the NCR90C198 automatically restarts at the beginning of the receive buffer when the end has been reached. The NCR90C198 keeps track of available buffers and stops receiving when there are no more buffers available. The host must update the pointer that keeps track of the packets that have been read.

The pointers associated with the receive buffer are the Next Page to Receive (NPRX), Next Page to Read (NPRD) and Start of RX Buffer (SRXB). When a packet has been received successfully, the NCR90C198 increments the NPRX pointer and sets the RP bit which generates an interrupt. The host, after determining the source of the interrupt, reads the NPRX pointer which clears RP, reads the packet and then increments the NPRD pointer.

Packet Transmission

In the transmit buffer chaining mode the NCR90C198 transmits all the packets the host wrote into the transmit buffer. It is the responsibility of the host to update the pointer that points to the last packet to be transmitted. The NCR90C198 will keep track of which packets to send and when to stop. If the circular mode has been enabled, the NCR90C198 automatically restarts at the beginning of the transmit buffer when the end has been reached.

The pointers associated with the transmit buffer are the Next Page to Write (NPWR), Next Page to Transmit (NPTX) and Start of TX Buffer (STXB). When the host transmits a packet, it must write the packet into the page pointed to by the NPWR pointer. If the host transmits multiple packets, it must write the packets into the subsequent pages, and then move the NPWR pointer to the page that follows the last written page. The NCR90C198 will start to transmit one packet per token when the enable transmit or enable chain transmit commands are executed. Upon a successful transmission, the TA and TMA bit will be set.

See Figure 5 for a diagram depicting the relative function of each pointer. Descriptions of each pointer follow.

Next Page to Write (NPWR).

The NPWR pointer contains the page address (in the buffer RAM) for the host to write the next packet of data to be transmitted.

Next Page to Transmit (NPTX).

The NPTX pointer contains the page address for the next packet to be transmitted.

Start TX Buffer (STXB).

The STXB pointer contains the starting page address of the transmit buffer RAM. The transmit buffer memory ranges from this address to the end of memory.

Next Page to Receive (NPRX).

The NPRX pointer contains the page address of the next packet to be received.

Next Page to Read (NPRD).

The NPRD pointer contains the page address (in the buffer RAM) of the next packet to read.

Start RX Buffer (SRXB).

The SRXB pointer contains the starting page address of the receive buffer RAM. The receive buffer memory ranges from this address up to the STXB page address.

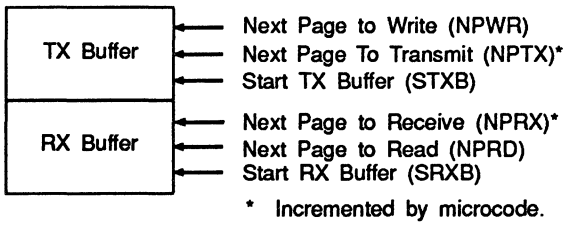


Figure 5 Buffer RAM Pointer Diagram

PIN DESCRIPTION

AD0-AD7: Low Order, Multiplexed Address/Data Bus

During host accesses to the NCR90C198, data is transferred on this bus. During host access to memory, the low address byte is output and latched by LADR during the first part of the cycle. During the second part of the cycle, these pins are in high impedance state. During the NCR90C198 accesses to memory, the low address byte is output and latched by LADR during the first part of the cycle, and data is transferred during the second part of the cycle. Data is transferred on this bus during the NCR90C198 read of configuration switches.

AD8-AD15: High Order, Multiplexed Address/Data Bus

During host accesses to the NCR90C198, data is unused. During host access to memory, the high address bits are output and latched by LADR during the first part of the cycle. During the second part of the cycle, these pins are in high impedance state. During the NCR90C198 accesses to memory, the high address bits are output and latched by LADR during the first part of the cycle, and data is transferred during the second part of the cycle. Bit AD15 is used to write a LAN driver disable bit during the first part of a NCR90C198 access to memory. During the NCR90C198 read of configuration switches, data is transferred on this bus.

AEN: Address Enable
This input enables address decoding when low.

BALE: Address Latch Enable
This input signal is provided by the bus arbitration IC to latch LA17-LA23 on the falling edge.

CSDP: Dual Port Memory Chip Select
This signal enables the dual port memory when low.

ET1, ET2: Extended Timeout Functions
These input signals select the timeout durations of the NCR90C198. They are primarily used to check responses from other nodes on the LAN. These pins should be tied high for normal operation. See Table 1.

IOCHRDY: I/O Channel Ready
The NCR90C198 uses this output signal to insert wait states during host accesses. When low, this output extends the access until it is released.

IOR: I/O Read
When low, this input from the PC AT bus instructs the NCR90C198 to put data on the data bus for the host to read.

IOW: I/O Write
When low, this input signal from the PC AT bus instructs the NCR90C198 to receive data from the data bus.

IRQ: Interrupt Request
The NCR90C198 drives this signal high to signal the host that an enabled interrupt condition has occurred. IRQ returns low after clearing the interrupt status condition or the corresponding mask bit.

LA17-23: I/O Address Lines
These input lines are used for accessing the extended address space.

LADR: Latch Address
The falling edge of this output latches the lower 8 address lines when accessing the RAM buffer memory. This signal is active during NCR90C198 memory accesses and host memory accesses.

MEMCS16: 16-Bit Memory
Decoded from LA17-LA23 or LA17-LA23 and SA14-SA16, this output signal gives notification to the PC of a 16-bit memory transfer.

MEMR: Memory Read Request
When low, this input signal from the PC AT bus instructs the NCR90C198 and on-board memory to put data on the PC AT bus.

MEMW: Memory Write Request
When low, this input signal from the PC AT bus instructs the NCR90C198 and on-board memory to receive data from the PC AT bus.

OE1: Output Enable 1
This output goes low to enable the RAM. When low, data from the RAM is expected on the multiplexed address/data bus. This signal goes low when the host is performing a memory read with the NCR90C198.

OE2: Output Enable 2
This output goes low to allow the host access to the multiplexed address/data bus. It goes high to allow the NCR90C198 access to the multiplexed address/data bus.

OSCIN & OSCOUT: Oscillator Input and Output
These input and output pins connect an external 20 MHz crystal to the internal oscillator. The OSCIN pin may also be used to drive the NCR90C198 with an external clock. OSCOUT is left floating in this case.

PULS1 & PULS2: Pulse 1 & 2 (Transmitter Out)
These outputs are nonoverlapping, negative-going pulses that control the cable-driving circuitry. The output signals correspond to the data being transmitted over the LAN from this node. Pulse 1 is the first and Pulse 2 is the second pulse in this dual-pulse process.

RESET: Reset
This input signal, when driven high, resets the state of the NCR90C198. Upon power-up, the internal power-on-reset cell resets the chip. During reset, the NCR90C198 sequence counter is set to zero and the Reset status bit is set to a 1. See Table 4.

ROMEN: ROM Enable
This output goes low to enable the ROM. When low, data from the ROM is expected on the multiplexed address/data bus. This signal goes low when SA13 is high and the host is performing a memory read with the NCR90C198. The 16 highest addresses in the ROM memory map access the internal registers. ROMEN is disabled when these addresses are accessed.

RXIN: Receive Data In

This input signal receives serial data from the LAN cable circuitry.

SA0-16: System Address Bus

This input bus is driven by the PC AT address lines. Addresses from this bus determine the I/O and memory addresses used when accessing this chip.

SBHE: Byte High Enable

This signal indicates a transfer of data on the eight most significant bits of the data bus.

SW1OE: Switch 1 Output Enable

This output goes low to read the switch settings for the memory and I/O select addresses. The NCR90C198 responds to these addresses when accessed by the host.

SW2OE: Switch 2 Output Enable

This output goes low to read the switch settings for the Node ID. This value is used to uniquely identify the node on the LAN.

WE1: Write Enable 1

This output goes low when a write occurs from the host or the NCR90C198 to an even address in the memory buffer RAM.

WE2: Write Enable 2

This output goes low when a write occurs from the host or the NCR90C198 to an odd address in the memory buffer RAM.

Table 2 NCR90C198 Reset State

Name	State
Registers and Pointers	**msb lsb**
Command Register 1	See Note 1
Command Register 2	See Note 1
Status Register 1 (See Note 2)	1 x x 1 0 0 0 1
Status Register 2 (See Note 3)	1 1 0 x x 0 0 0
Interrupt Mask 1	0 0 0 0 0 0 0 0
Interrupt Mask 2	0 0 0 0 0 0 0 1
Next Page to Write (NPWR)	1 1 1 1 1 1 1 1
Next Page to Transmit (NPTX)	1 1 1 1 1 1 1 1
Start TX Buffer (STXB)	1 1 1 1 1 1 1 1
Next Page to Receive (NPRX)	1 1 1 0 0 0 0 0
Next Page to Read (NPRD)	1 1 1 0 0 0 0 0
Start RX Buffer (SRXB)	1 1 1 0 0 0 0 0
Output Pins	
AD0-AD15, CSDP	Resistive high
IRQ, IOCHRDY, MEMCS16	High impedance
PULS1, PULS2, OE1, OE2, WE1, WE2, SW1OE, SW2OE, ROMEN	1 (high)
LADR	0 (low)

[1] See the *REGISTER DESCRIPTIONS* section following.
[2] In Status Register 1, bits 5 & 6 reflect the state of the ET1 & ET2 pins.
[3] In status Register 2, bits 3 & 4 reflect the state of the IL0 & IL1 pins.

REGISTER DESCRIPTIONS

The registers of the NCR90C198 occupy seven addresses in a Memory or I/O Map. The host system has access to 10 registers which are:

- Command Registers 1, 2 & 3
- Interrupt Mask Registers 1 & 2
- Status Registers 1 & 2
- NPRX Pointer Register
- NPTX Pointer Register
- RESET Command Register

Table 3

AD 3 2 1 0	WRITE	READ
0 0 0 0	Interrupt Mask 1	Status Register 1
0 0 0 1	Command Reg. 1	Reserved
0 0 1 0	Command Reg. 2	NPRX Pointer
0 0 1 1	Reserved	NPTX Pointer
0 1 0 0	Interrupt Mask 2	Status Register 2
0 1 0 1	Command Reg. 3	Reserved
1 0 0 0	Reset Chip	Reset Chip

Command Registers Description

NCR90C26 Mode. In the NCR90C26 mode, only Command Register 1 is valid. Command Register 1 is a write-only register accessed by writing to address 1. The commands recognized by Command Register 1 are described below.

Command Register 1

Data msb lsb	Function
0 0 0 0 0 0 0 1	Disable Transmitter: Causes the NCR90C198 to cancel any pending transmit command. This command will cause the TA bit to be set the next time the NCR90C198 receives the token.
0 0 0 0 0 0 1 0	Disable Receiver: Causes a pending receive command to be canceled. This command causes the RI bit to be set the next time the NCR90C198 receives the token. If a PACKET has already started arriving, then this command has no effect.

Command Register 1

Data msb lsb	Function
0 0 0 n n 0 1 1	Enable Transmit from Page nn: Tells the NCR90C198 to prepare for a transmit operation out of RAM buffer page nn when it next receives the token. The TA and TMA bits are reset when the NCR90C198 receives the command. The TA bit=1 at completion of the transmission. The TMA bit will be set when the destination node has sent back an acknowledgment. If TA=0, this command should not be issued. During reset, nn=11.
b 0 0 n n 1 0 0	Enable Receive to Page nn: Allows the NCR90C198 to receive messages in RAM buffer page nn. The RI bit is set to '0' by this command. If b=0, only messages addressed to the NCR90C198's ID are received. If b=1, then broadcast messages are also accepted. RI is set by a successful message reception. During reset, nn=00 and b=0.
0 0 0 0 s 1 0 1	Buffer Size: Tells the NCR90C198 the size of its RAM buffer. If s=0, the buffer is 1K bytes and only short packets are sent and received. If s=1, the buffer is 2K bytes and both short and long packets are used. During reset, s=0.
0 0 0 r p 1 1 0	Clear Flags: Resets the POR and/or the RECON status bits depending on the variable bits. If r=1, the RECON flag is cleared, and if p=1, then POR is cleared. During reset, r=0 and p=0.
0 0 0 0 t 1 1 1	Enable Duplicate ID routine: When t=0, the Duplicate ID (DPID) routine is disabled. When t=1, the DPID routine is enabled. During reset, t=0.

NCR90C98 Mode. Command Registers 1, 2 & 3 are write-only registers accessed by writing addresses 01, 02 or 05 respectively. Eight-bit commands transfer control information to the NCR90C198. The commands are described below.

Command Register 1

Data (msb lsb)	Function
0 0 0 0 0 0 0 1	Disable Transmitter causes the NCR90C198 to immediately cancel any pending transmit commands by setting the TA bit.
0 0 0 0 0 0 1 0	Disable Receiver causes the NCR90C198 to cancel any pending receive commands by setting the RI bit. If a packet has already started arriving when this command is executed, it finishes and no more packets are received.
n n n n n 0 1 1	Enable Transmit from page nnnnn: Transmits a packet out of buffer RAM nnnnn upon receipt of the token. This command clears TA and TMA. TA = 1 at the completion of the transmission. TMA = 1 when an ACK is received from the destination node. During reset, nnnnn = 11111.
n n n n n 1 0 0	Enable Receive to page nnnnn: The NCR90C198 receives packets in buffer RAM starting at page nnnnn. This command sets the pointers SRXB, NPRD and NPRX to nnnnn and clears the RI bit. RI is set when no more buffers are available. During reset, nnnnn = 00000.
p 0 0 s s 1 0 1	Size Definition: This tells the NCR90C198 the size of its buffer RAM and whether it can receive long or short packets. During reset, ss=00 and p=0.

ss	RAM	p	Packet
00	1K	0	256 bytes
01	2K	1	256/512 bytes
10	4K	When ss=00, only short packets are supported.	
11	8K		

When p=1, A8 is driven by an internal counter and not by the lsb in the NPTX or NPRX pointers. A page will be defined as 512 bytes and start on an even boundary.

0 0 0 r p 1 1 0	Clear Flags: Resets the RECON status bit if r=1 and/or the Reset status bits if p=1. During reset, r=0 and p=0
0 0 0 0 t 1 1 1	Enable Duplicate ID routine: The Duplicate ID (DPID) routine is disabled when t=0 and enabled when t=1. During reset, t=0.

Command Register 2

Data (msb lsb)	Function
n n n n n 0 0 1	Write Next Page to Write Pointer (NPWR): Initializes the NPWR pointer to page nnnnn. During reset, nnnnn = 11111.
n n n n n 0 1 0	Write Next Page to Read (NPRD) pointer: Initializes the NPRD pointer to page nnnnn. During reset, nnnnn = 00000.
n n n n n 0 1 1	Initialize Transmit pointers: Initializes Next Page to Transmit (NPTX), Next Page to Write (NPWR) and Start Transmit Buffer (STXB) pointers to page nnnnn. During reset, nnnnn = 11111.
0 0 0 0 0 1 0 0	Enable Chain Transmit: Tells the NCR90C198 to start transmitting from the page pointed to by the NPTX pointer. It stops when the NPTX pointer has reached the NPWR pointer. This command clears TA and TMA. The TA bit is set to a logic '1' at the completion of the transmission. TMA is set to a logic '1' when an ACK is received from the destination node.
b r c 0 0 1 0 1	Write Configuration: Tells the NCR90C198 what mode it is in. When b=1, broadcast messages will be accepted. When r=1, chain receive is enabled. When c=1, circular buffer chaining is enabled. During reset, b=0, r=0, and c=0.

Command Register 3

Data (msb lsb)	Function
0 0 0 0 e 0 0 0	LAN Driver Enable/Disable: When e=0, the LAN driver is disabled. When e=1, the LAN driver is enabled. Writing this command causes the NCR90C198 to perform a memory cycle and write the enable/disable bit on AD15. On reset, e=0. This is an optional command used to control the external LAN driver circuitry.

Status Register Description

Status Registers 1 & 2 are read-only registers that allow the host to monitor the status of the LAN. Status Register 1 is read from address 00 and Status Register 2 is read from address 04. In the NCR90C26 mode, only Status Register 1 is used.

Status Register 1

7	6	5	4	3	2	1	0
RI	ETS2	ETS1	Reset	DPID	RECON	TMA	TA

Bits	Name	Description
0	TA	Transmitter Available: When TA is set to a '1' the node is available to carry out a transmit sequence. It also indicates that any previous ENABLE TRANSMIT process has been completed. TA is cleared by the Enable Transmit and Enable Chain Transmit commands. TA is set after packet(s) have been transmitted and ACK'ed. TA is also set if there is no ACK and the node has timed out.
1	TMA	Transmit Message Acknowledged: When TMA is set to a '1' the message sent from a previous ENABLE TRANSMIT command was acknowledged by the receiving node. TMA is cleared by the Enable Transmit and Enable Chain Transmit commands. TMA is set after packet(s) have been transmitted and ACK'ed by the receiving node.
2	RECON	Reconfiguration Flag: When RECON is set to a '1' a system Reconfiguration took place due to the expiration of an Idle timeout. RECON is reset by the CLEAR FLAGS command.
3	DPID	Duplicate ID status bit. This bit is set when the Duplicate ID routine is enabled and a duplicate node ID is detected. It is cleared when the Duplicate ID routine is disabled. See DPID command description and the DPID Diagnostic Routine description for more information.
4	Reset	Reset: When the Reset bit is set to a '1' the NCR90C198 has experienced a reset from one of three sources. The reset could come from 1. an active signal on the RESET input, 2. the power-on cell has been triggered by the application of power, or 3. the Reset command has been executed. The Reset status bit is cleared by the Clear Flags command.
5-6	ETS1, ETS2	Extended Timeout Status 1 & 2: The state ETS2 of these bits reflects the logic level on the ETS1 & ETS2 pins. Under normal operating conditions ETS1 & ETS2 will be '1'.
7	RI	Receiver Inhibited: When RI is set to a '1' the NCR90C198 is not receiving any messages from other nodes. RI is cleared by the Enable Receive command and when a buffer has been made available in the Buffer Chain mode. RI is set when a packet has been received or when there are no more buffers available in the Buffer Chain mode.

Status Register 2 (NCR90C98 Mode Only)

7	6	5	4	3	2	1	0
1	1	1	TR	IL1	IL0	CD	RP

Bits	Name	Description
0	RP	Received Packet: When RP is set to a '1' a packet has been received in the Buffer Chain mode. RP is cleared by the read NPRX command.
1	CD	Carrier Detect: When CD is set to a '1' the NCR90C198 is detecting activity on the RXIN pin. CD is cleared when the NCR90C198 transmit/receive mode is enabled.
2,3	IL0,IL1	Interrupt Level Encode Bits. The user encodes the interrupt level at which the board is set using these bits. These are for software use only; no hardware function is associated with these bits.
4	TR	Token Received Status Bit. This bit is set each time the token is addressed to and received by this node.

Interrupt Mask Registers

The Interrupt Mask Registers are write-only registers that determine which of the five maskable conditions will cause an interrupt. (See *HOST INTERRUPTS* section on the next page for details).

Next Page to Receive (NPRX) Pointer Register

The Next Page to Receive (NPRX) pointer is read from address 02. The format of the data with the register follows.

1 1 1 A12 A11 A10 A9 A8 - Read NPRX pointer. By executing this read the RP bit will be reset.

Next Page to Transmit Pointer Register

The Next Page to Transmit Pointer is read from address 03. The format of the data with the register follows.

1 1 1 A12 A11 A10 A9 A8 - Read NPTX pointer.

Reset Register Description

When register 08 is accessed (read or write), the NCR90C198 is reset. This provides the host a means for resetting the NCR90C198 from software.

RESET OPTIONS

There are three reset options for the NCR90C198. When power is applied to the chip, the POR cell senses this and generates an internal signal to reset the chip. Another option resets the chip when a high signal is applied to the Reset pin for a minimum of 200ns. It is also possible to reset the controller section of the chip by reading or writing to I/O location 08.

The NCR90C198 executes a reset routine that writes D1H to address 0 and writes the node ID to address 1 in buffer RAM.

NCR90C98 MODE SOFTWARE CONSIDERATIONS

The transmit and receive buffers can be used as standard or circular buffers with the latter being the most efficient. The standard method for the host to transmit packets of information in the buffer chaining mode follows.

1. Initialize transmit pointers.
2. Write the packet(s) to the page(s).
3. Set the NPWR pointer to next free page.
4. Execute Enable Chain Transmit command.
5. When NPWR=NPTX, TA & TMA is set as described in the Status Register Description.
6. If more packets have been written, repeat steps 3 and 4.
7. If not, repeat steps 2, 3, and 4 or if not in the circular mode, repeat steps 1-4 when the end of the buffer has been reached.

The NPTX pointer will stop when it has reached the end of the buffer. However, if the circular mode has been enabled, the NPTX pointer will reload the STXB pointer when it has reached the end of the buffer. For short packets the last page of the buffer is unavailable if the circular mode is disabled.

The standard method for the host to receive packets of information in the buffer chaining mode follows.

1. Execute the Enable Receive command.
2. When the RP interrupt occurs, read the NPRX pointer. This resets the RP flag.
3. Read the packet, write the NPRD pointer.
4. If NPRX indicates missed interrupts, repeat step 3.
5. If not, go back to step 2 or if not in the circular mode, go back to step 1 when the end of the buffer has been reached.

With the circular mode disabled, NPRX=STXB after the last page has been filled with the RI bit set. With the circular mode enabled, the NPRX will reload the SRXB pointer when it has reached the end of the buffer. When NPRX=NPRD, the RI bit is set.

DPID DIAGNOSTIC ROUTINE

The Duplicate ID (DPID) routine functions as a diagnostic tool to be run before a node goes on line. It checks to see if there are other nodes on the network that respond to its own node ID during a token pass.

The routine listens for token passes to its own node ID. If one occurs, the node waits for the maximum time a node has to respond to a token pass. If activity is detected on the line during this time, another node is responding to the token pass, and the DPID bit is set. If no activity is detected, the routine restarts and listens for token passes to itself again.

The DPID bit has a maskable interrupt bit associated with it which generates an interrupt when the DPID bit is set. The minimum time it takes to detect a duplicate ID is one token rotation around the loop. The maximum time is the time it takes to reconfigure the system.

In the DPID mode the NCR90C198 does not reset the reconfiguration counter, thus this node experiences a reconfiguration when the counter expires. To avoid reconfiguring the network, the node should be designed so the LAN transmitter can be disabled/enabled by the software. This is done with the Enable/Disable LAN transmitter command. Bit AD15 controls the transmitter enable signal via an external flip-flop. By disabling the LAN transmitter, the node does not disturb the network. See Figure 7.

The following is the procedure for using the DPID routine.

- Disable the LAN transmitter.
- Enable the DPID interrupt by writing the correct mask to the interrupt mask register.
- Enable the DPID routine by the Enable Duplicate ID command which puts the node is in a listen only mode.
- After the proper time period, if no duplicate ID was detected, disable the DPID routine and enable the LAN transmitter. The node then goes through a normal reconfiguration to put itself on line.

HOST INTERRUPTS

The NCR90C198 generates an interrupt on the IRQ pin in response to several of the conditions that set status bits. The Interrupt Mask Registers determine which of the five conditions will cause an interrupt. The status bits TMA, ETS1, ETS2 and CD have no corresponding mask bits and do not cause interrupts. The five maskable status bits are outlined in the following diagram.

Interrupt Mask Register 1

7	3	2	0
RECEIVE INHIBIT	DPID	RECON TIMEOUT	TRANSMITTER AVAILABLE

Interrupt Mask Register 2

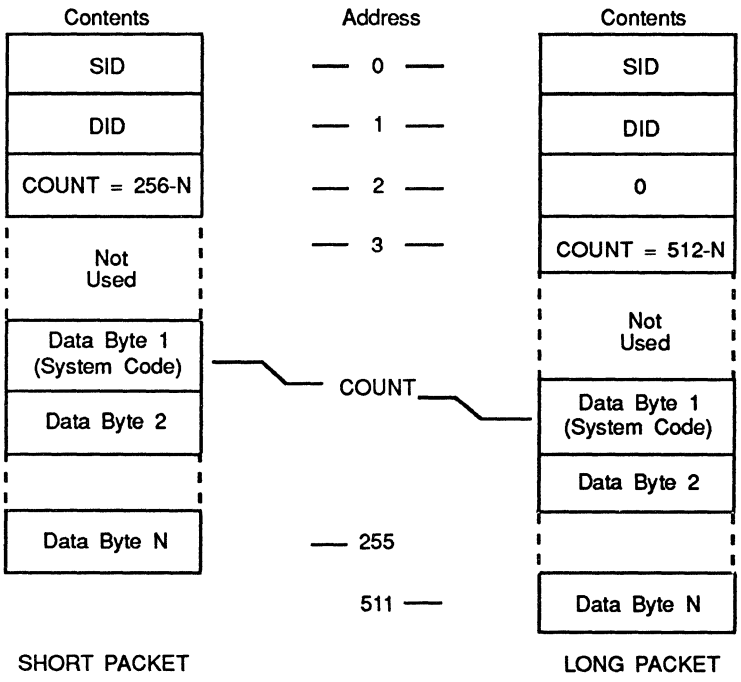
	0
	RECEIVED PACKET

Setting any of these bits to "1" will enable the IRQ signal to be asserted high when the corresponding status bits go high. The unused bits in the Interrupt Mask Register 2 must be written to a zero. Once the IRQ signal is high, it can be cleared by clearing the corresponding bit in the Status Register or the Mask Register. RP is cleared by reading the NPRX pointer.

Reset generates a nonmaskable interrupt. It is cleared by the Clear Flags Command.

RAM BUFFER MEMORY MAP

Figure 6 shows the locations of the major components for both Short (up to 256 bytes) and Long (up to 512 bytes) PACKETS.



NOTE: Addresses shown are relative to a Page, not absolute. SID = Source ID (not written in Transmit Packets). DID = Destination ID (set = 0 for Broadcasts). N = Message Length. "Not Used" bytes imply message is less than maximum length. These bytes would be written for Max. Messages: SHORT = 253 bytes, LONG = 508.

Figure 6 RAM Buffer Map

DETAILED HOST INTERFACE DESCRIPTION

PC AT Interface

The PC AT interface consists of 24 address lines, 16 data lines and 11 control lines. These correspond to similar signals on the PC AT bus. Figure 7 shows the NCR90C198 including the ROM and LAN driver control hardware. The address lines combined with the control lines are decoded by the chip to determine valid accesses. The NCR90C198 controls all the data transfers on the multiplexed address/data bus and does the arbitration between the host and itself. The transceivers ('245) are used to isolate the host and the local bus. The output drivers are controlled by OE2 and external logic ('02) is used to control direction.

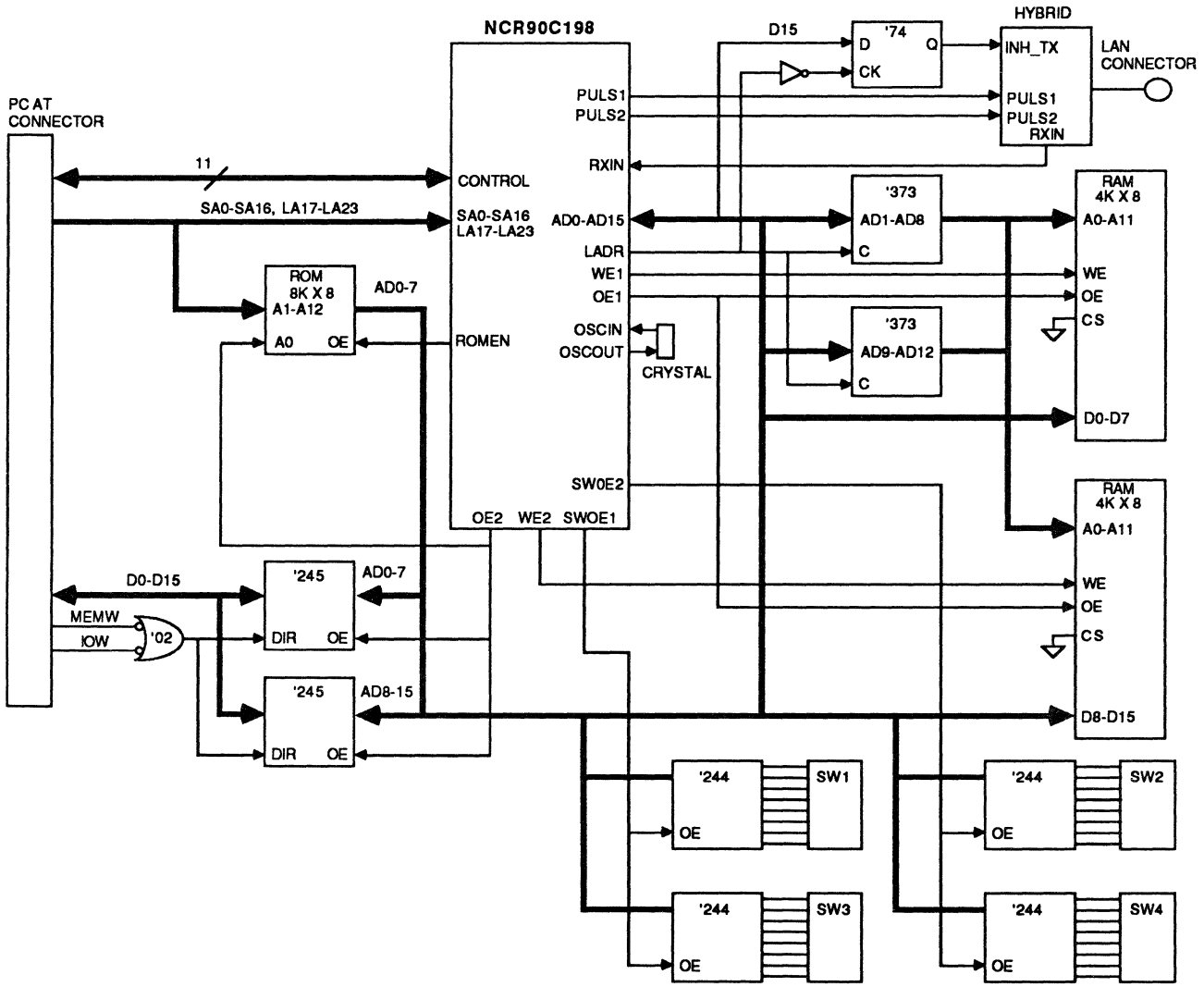


Figure 7 16-bit Standard Memory System Block Diagram

I/O and Memory Accesses

The internal registers are I/O and memory mapped. The internal registers are available in the memory map only if the MIO bit is set when the node ID value is read.

When the NCR90C198 accesses the RAM buffer memory over the multiplexed address/data bus, the ('373) latches the low/high order address bytes on the falling edge of LADR. The 16-bit data is then transfered over the multiplexed address/data bus during the second half of the cycle.

Figure 8 shows how the on-board ROM, RAM buffer memory and internal registers appear in the host's memory map.

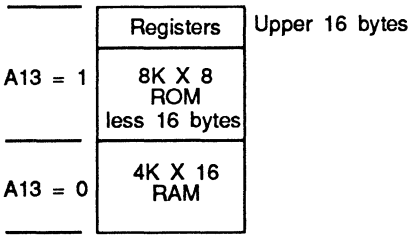


Figure 8 16K Byte Memory Organization

The switch settings and their symbols are described below. All bits must be driven when SW1OE and SW2OE are active for correct data to be read.

Node ID Switch Settings

AD line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	MIO	IL1	IL0	N/E	A23	A22	A21	A20	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

MIO Memory Mapped I/O. When set, this bit disables memory mapped access to the NCR90C198 registers. When cleared the registers are accessible through the memory map. The registers are always available through the I/O map.

IL0, IL1 Interrupt Levels. These bits reflect the switch settings on AD13 and AD14 when the node ID is read. They are available to the system designer to define as they wish. One use is for the software to read the interrupt level the board is set to.

N/E Normal (128K)/Expanded (16K). This decodes 128K memory segments when high and 16K memory segments when low.

A20-A23 1Mb Memory Segment Selection. These address lines are compared with LA20-LA23.

ID7-ID0 Node ID Bits. These node ID symbols represent the 8-bit node ID with ID0 being the least significant bit.

Memory & I/O Switch Settings

AD line	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	ET2	ET1	A9	A8	A7	A6	A5	A4	RD	S/D	A19	A18	A17	A16	A15	A14

ET2-ET1 Extended Timeout Functions. These bits provide the values for the extended timeout functions. Their value is reflected in bits 5 & 6 of Status Register 1.

A9-A4 I/O Address Bits. These bits indicate which address the NCR90C198 responds to when I/O reads or writes occur. When the system address bits (SA9-SA4) used in I/O accesses match these bits and the appropriate control lines are active, the NCR90C198 responds.

RD ROM Disable. This bit enables the use of an on-board ROM when set. When cleared the ROM is disabled. It is enabled during reset.

S/D Standard/Dual Port Memory. When set, this bit disables bus arbitration. It is cleared during reset.

A19-A14 Upper Memory Address Bits. These bits indicate which address range the NCR90C198 responds to when memory reads or writes occur. When the upper system address bits LA(19:17) and SA(16:14) match these bits and the appropriate control lines are active, the NCR90C198 responds.

LAN Driver Enable/Disable

If disabling of the LAN driver is desired, a flip-flop to hold the disable bit and an inverter ('04) must be added to the system. See Figure 7. The LAN Driver Enable/Disable command allows the host to selectively turn the LAN driver on or off. See the NCR90C98 mode command register description section.

Dual Port Memory

When the S/D bit is cleared, the NCR90C198 does not arbitrate during memory cycles. The ARCNET protocol ensures data integrity in RAM. However, care should be taken in test modes so the same location is not accessed by the NCR90C198 and host at the same time. In this case, the dual port RAM will inhibit one of the accesses. See Figure 9.

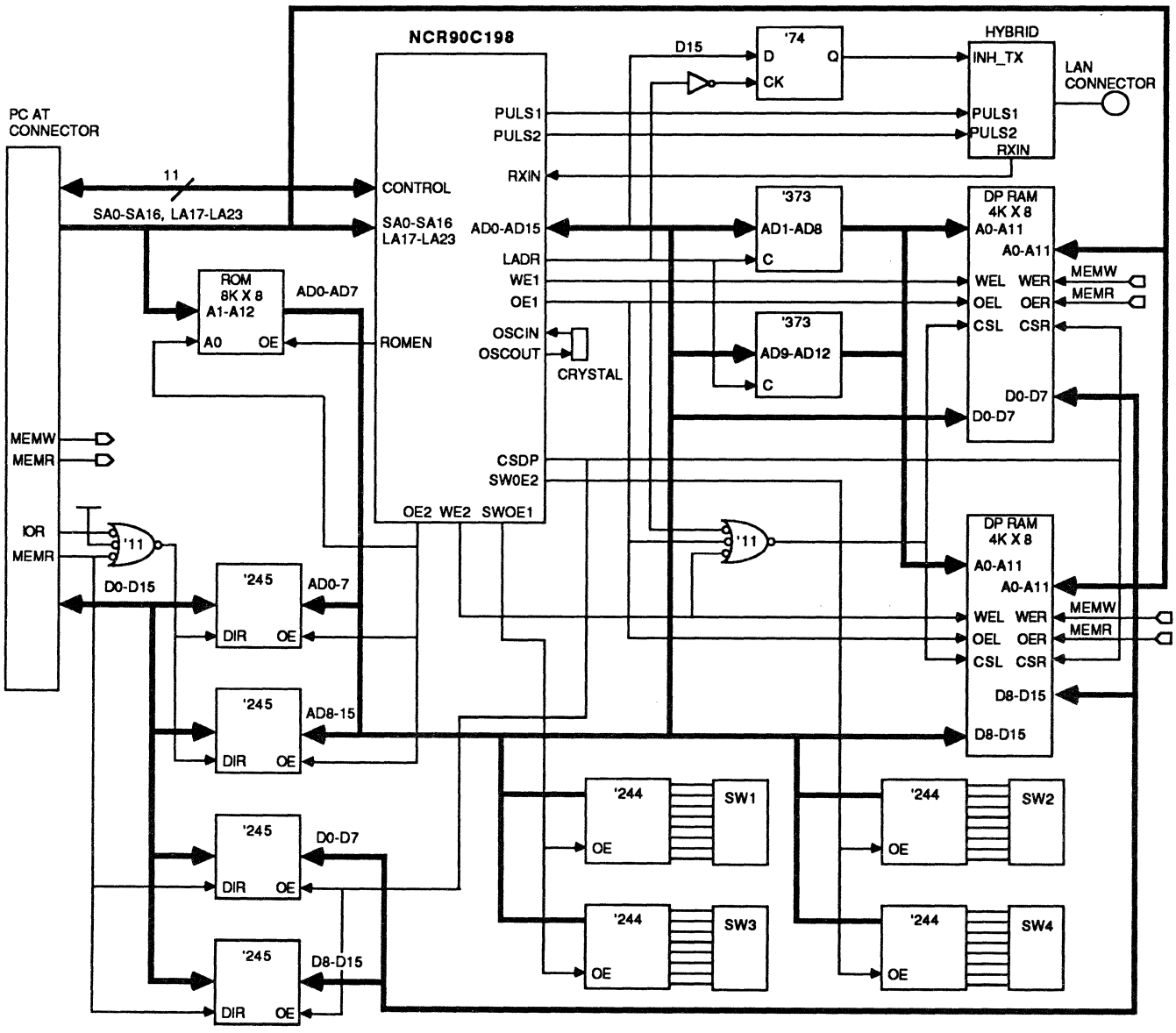
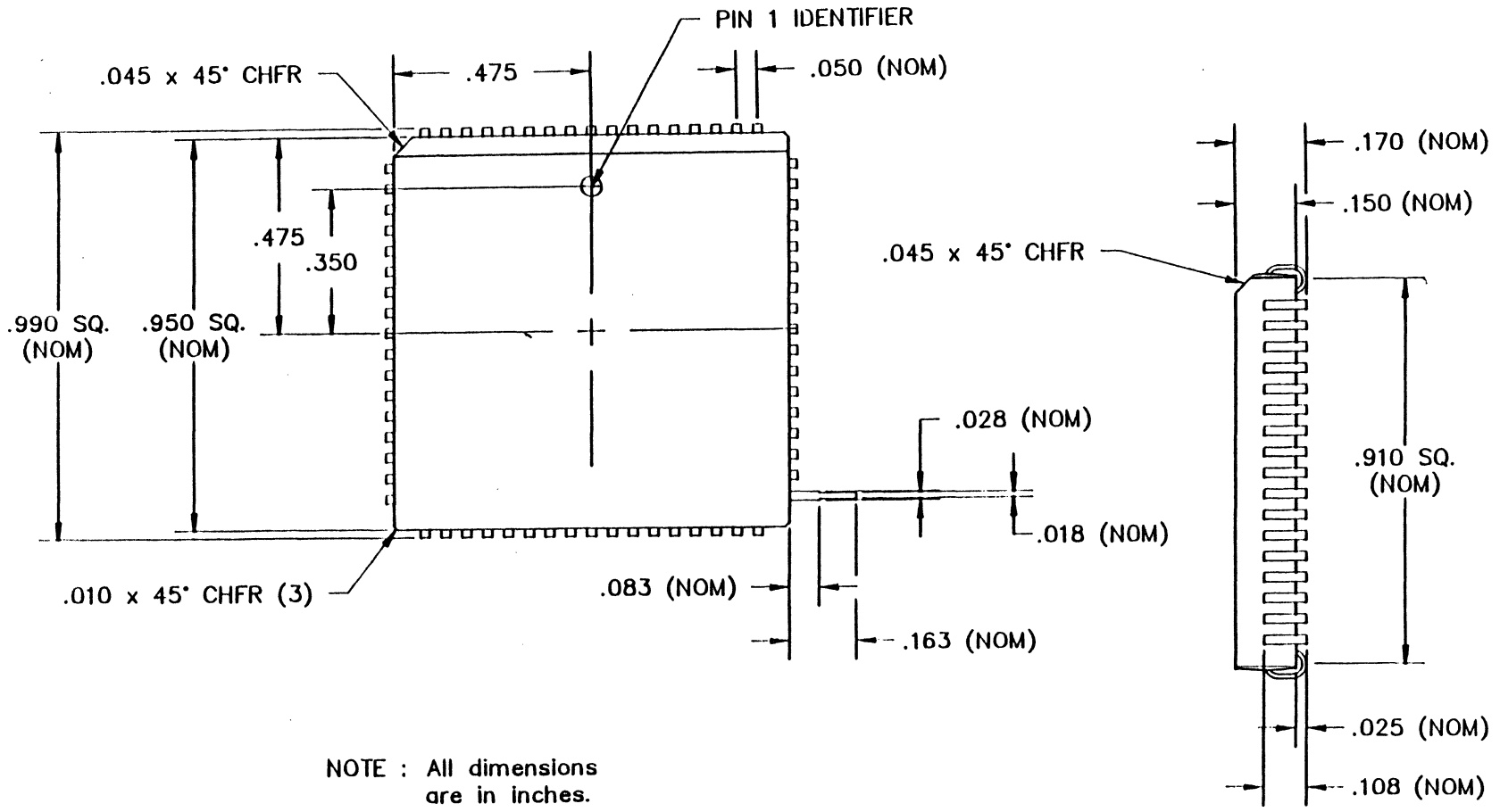


Figure 9 16-bit Dual Port Memory System Block Diagram



NOTE : All dimensions are in inches.

ORDERING INFORMATION

The NCR90C198 is available in a 68-pin Plastic Leaded Chip Carrier (PLCC). The following part number should be used to order the part.

Package Type	Part Number
68-pin PLCC	NCR90C198PP

ELECTRICAL SPECIFICATIONS

Absolute Maximums

Symbol	Parameter	Minimum	Maximum	Units
T_A	Ambient Temperature	0	70	°C
T_S	Storage Temperature	-55	150	°C
V_{DD}	Supply Voltage	-0.5	7.0	Volts
V_{IN}	Input Voltage	-0.5	V_{DD} + 0.5	Volts
V_{OUT}	Output Voltage,	-0.5	V_{DD} + 0.5	Volts
T_L	Lead Temperature (Soldering 10 seconds max)	-	250	°C

DC Characteristics (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A =0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
V_{IL}	Input Voltage, Low	V_{SS} - 0.5	0.8	Volts
V_{IH}	Input Voltage, High	2.0	V_{DD}	Volts
V_{IH} CLK	Clock Input High Voltage (OSCIN pin)	3.85	V_{DD}	Volts
V_{IL} CLK	Clock Input Low Voltage (OSCIN pin)	Vss	1.35	Volts
V_{OH}	Output Voltage, High (I_{OH} = -2mA, V_{DD} = 4.5V)	2.4		Volts
V_{OL}	Output Voltage, Low (I_{OL} = 4mA)		0.4	Volts
V_{IH}	Input Voltage, High (Schmitt trigger) (AEN, IOR, IOW, MEMR, MEMW, BALE, SBHE)	1.3	1.9	Volts
V_{IL}	Input Voltage, Low (Schmitt trigger) (AEN, IOR, IOW, MEMR, MEMW, BALE, SBHE)	0.9	1.5	Volts
C_{IN}	Input Capacitance		10	pF
I_P	Input Pullup Current (V_{IN} = 0.0V) (AD0-15, BALE, SBHE, LA20-23)	50	165	µA
I_I	Input Leakage Current		± 10	µA
I_{DD}	Power Supply Current (V_{DD} = 5.5V)		30	mA
I_{OL}	Output Current, Low (V_{OL} = 0.4V) (IOCHRDY, IRQ, MEMCS16)		24	mA

AC Characteristics (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

#	Description	Minimum	Typical	Maximum	Units
1	OSC low		25		ns
2	OSC period		50		ns
3	Request to IOCHRDY			27	ns
4	OE2 to IOCHRDY high		100		ns
5	Delay from request to OE1, OE2			20	ns
6	Address valid to MEMCS16			28	ns
7	LADR pulse width		25		ns
8	Address setup to LADR	15			ns
9	Address hold from LADR	15			ns
10	AD invalid to OE1, OE2	0			ns
11	OE2 to valid data			60	ns
12	Data setup to WE1, WE2 (90C198 cycle)	85			ns
13	Data hold from WE1, WE2 (90C198 cycle)	35			ns
14	WE1, WE2 pulse width		100		ns

AC Characteristics (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

#	Description	Minimum	Typical	Maximum	Units
15	OE2 to WE1, WE2 high	95			ns
16	OE1 pulse width (90C198 cycle)		100		ns
17	Synchronization time	50		100	ns
18	MEMR to ROMEN low			#17 + 35	ns
19	MEMR to OE2 low			#17 + 145	ns
20	OE2 to IOCHRDY high (ROM Access)		300		ns
21	Request to CSDP			30	ns
22	SW1OE, SW2OE pulse width		100		ns
23	Data setup to SW1OE, SW2OE high	30			ns
24	Data hold from SW1OE, SW2OE high	0			ns
25	RXIN pulse width	10			ns
26	OE2 to Data			50	ns

Oscillator/Crystal Specifications (V_{DD} = 4.5V to 5.5V, V_{SS} = 0V, T_A = 0°C to 70°C)

Parameter	Minimum	Typical	Maximum
XTAL			
Tolerance			±0.01%
Motional Resistance			25 Ω
Frequency		20 MHz	
External Clock			
Duty Cycle	40%		60%

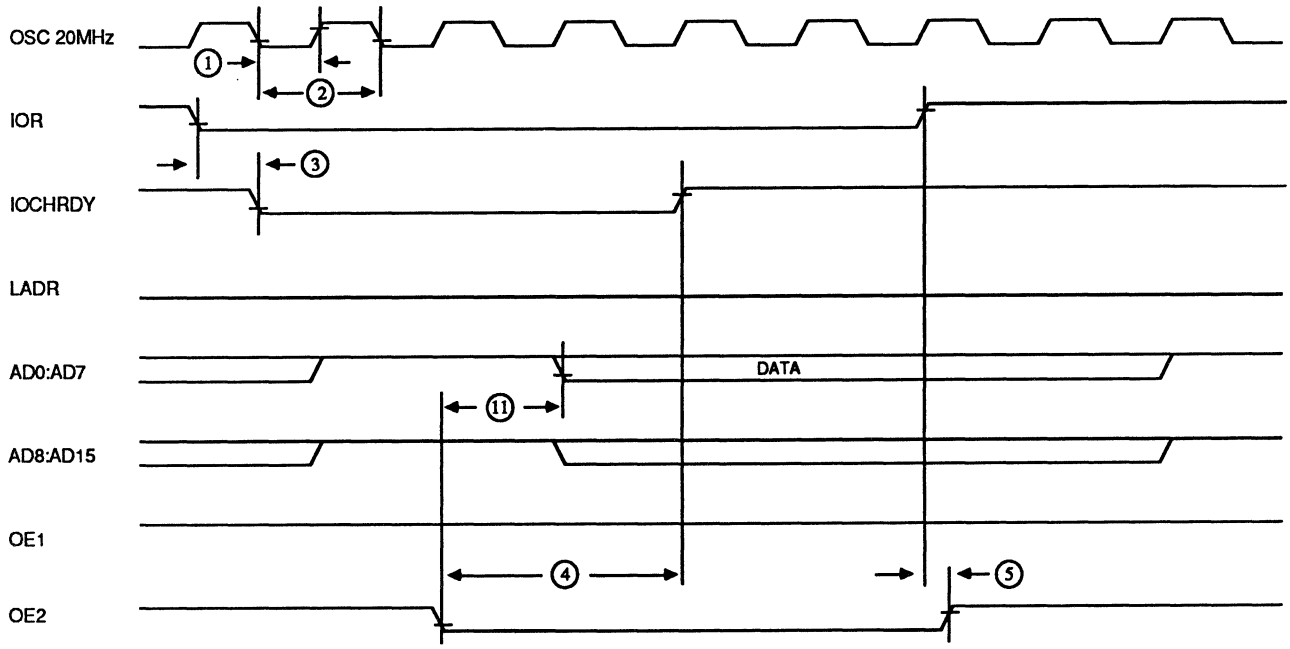


Figure 10 PC AT I/O Read Cycle

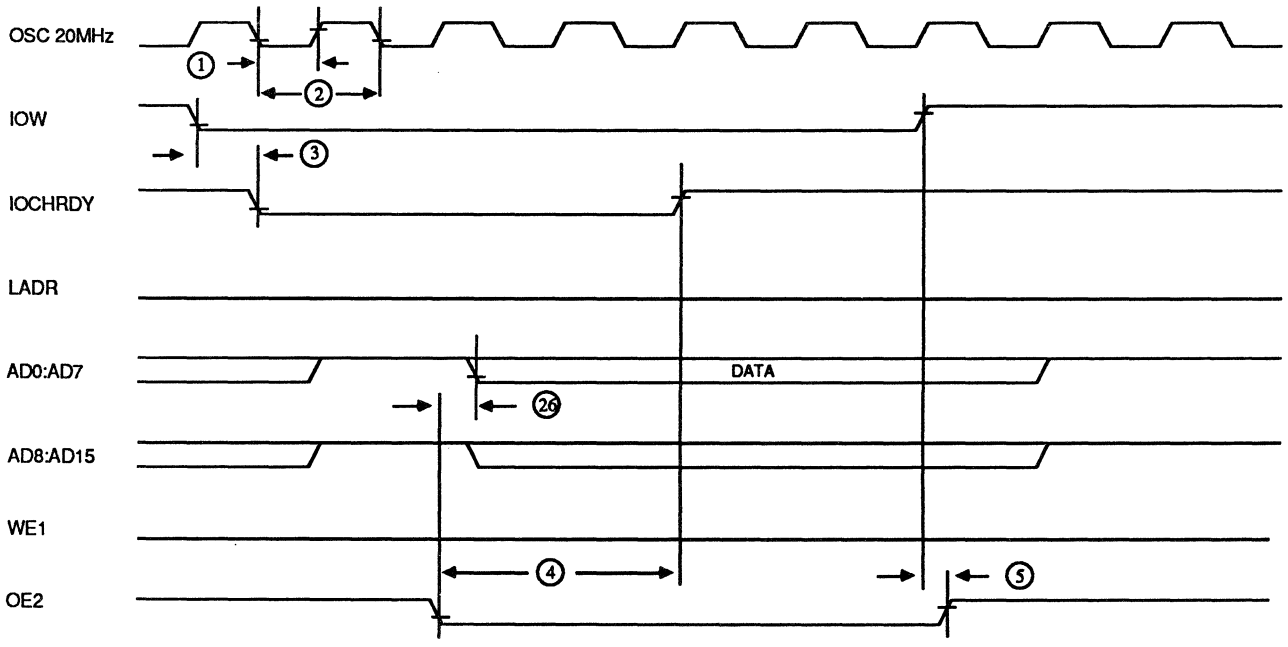


Figure 11 PC AT I/O Write Cycle

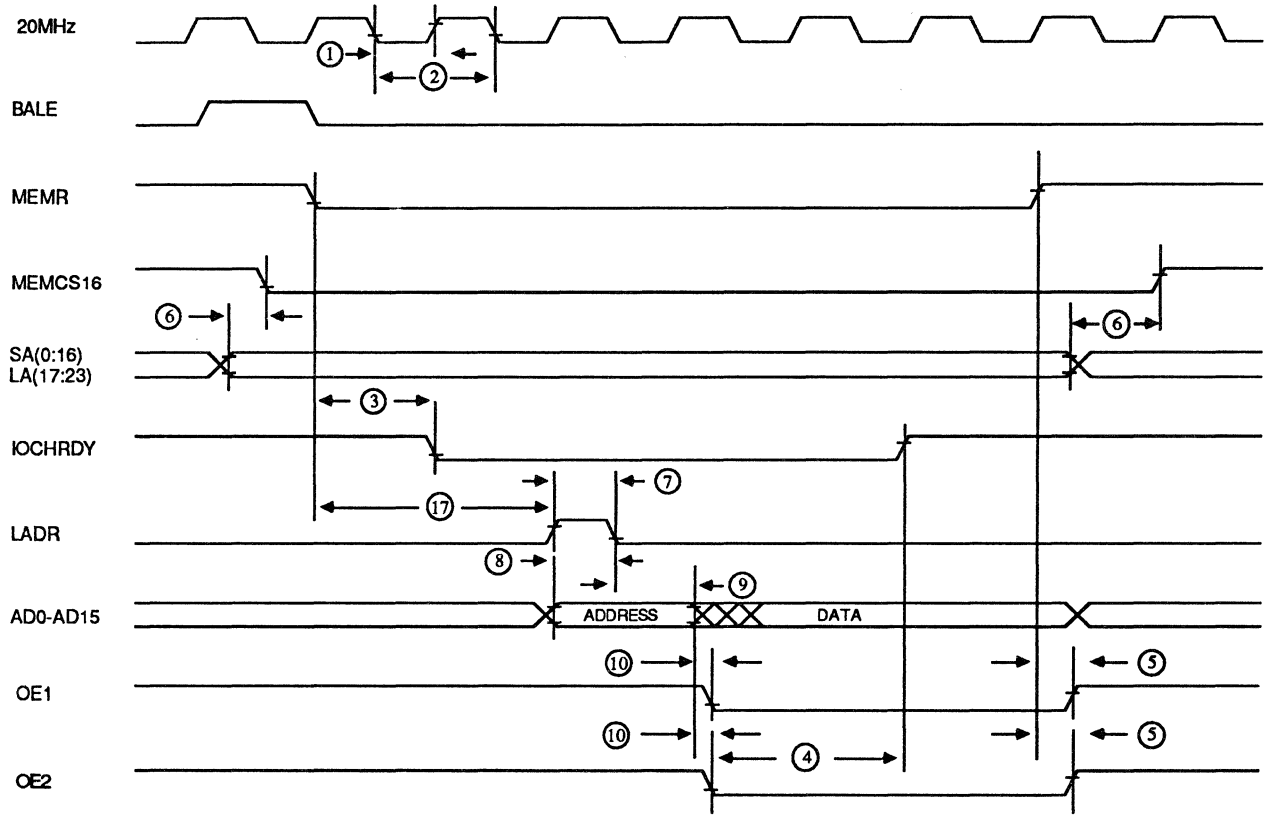


Figure 12 PC AT Memory Read Cycle

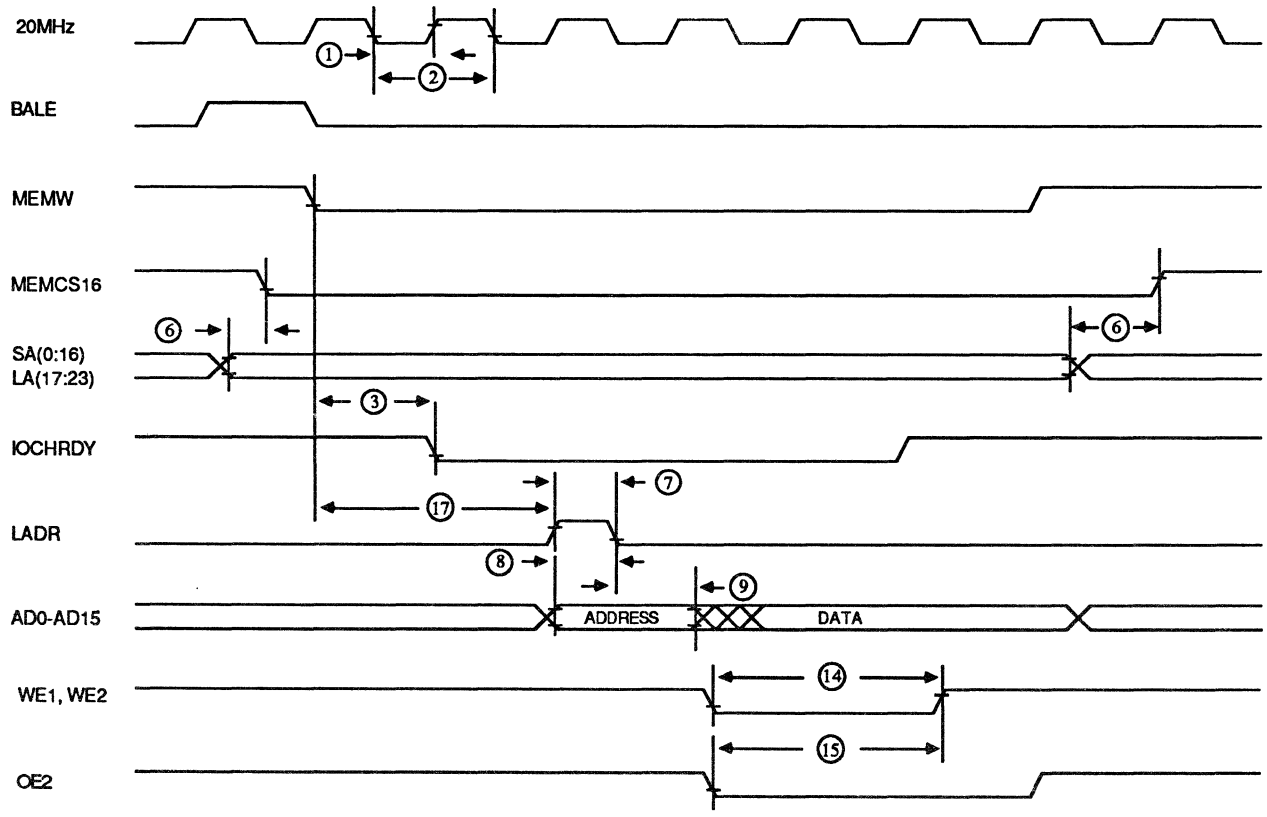


Figure 13 PC AT Memory Write Cycle

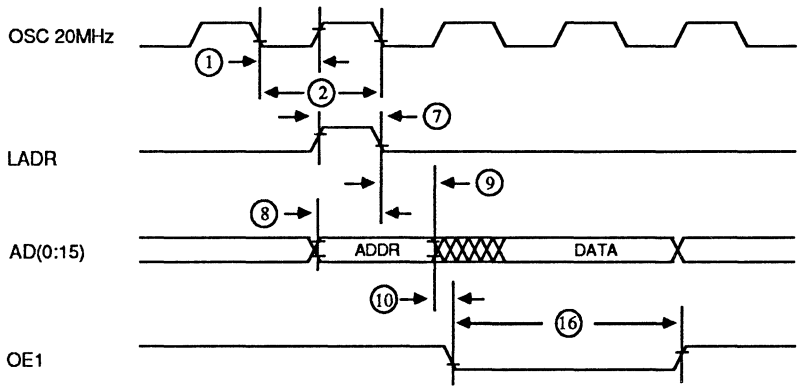


Figure 14 NCR90C198 Memory Read Cycle

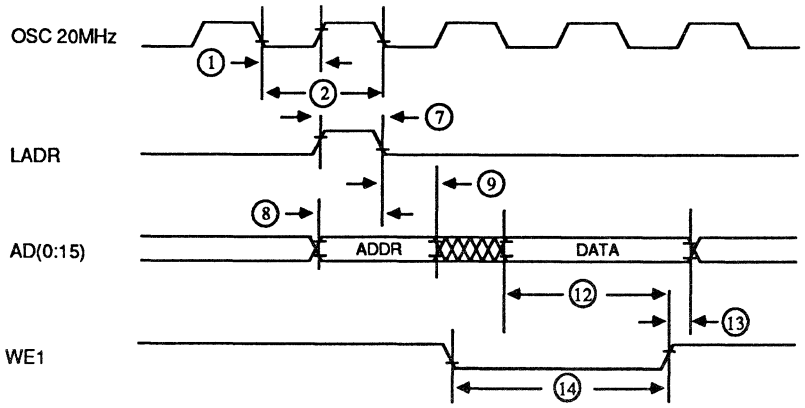


Figure 15 NCR90C198 Memory Write Cycle

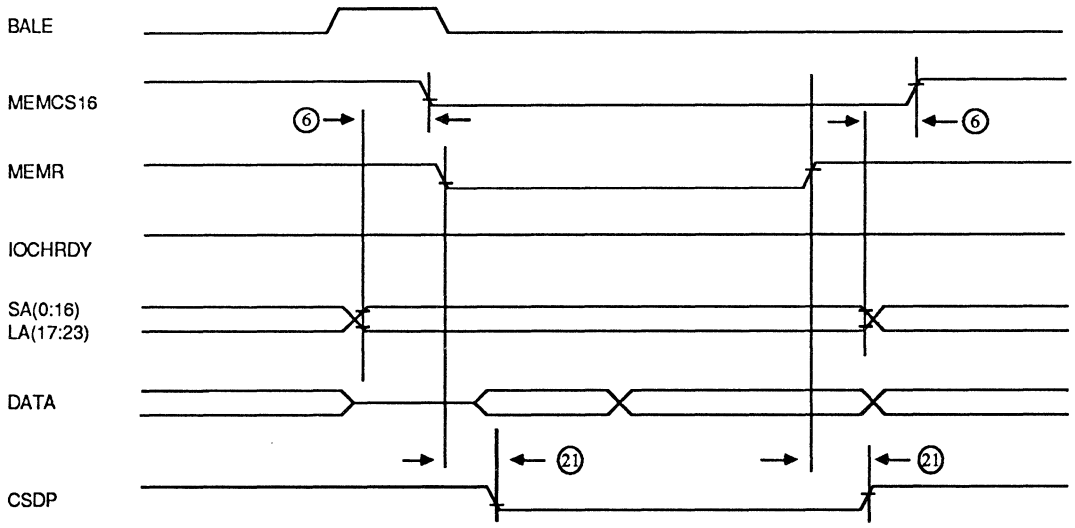


Figure 16 Dual Port Memory Read Cycle

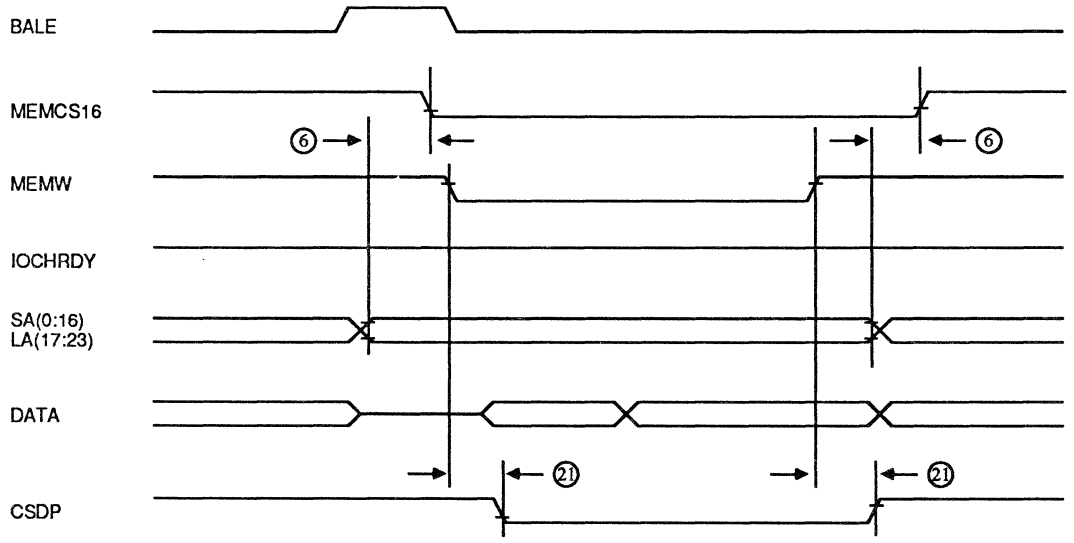


Figure 17 Dual Port Memory Write Cycle

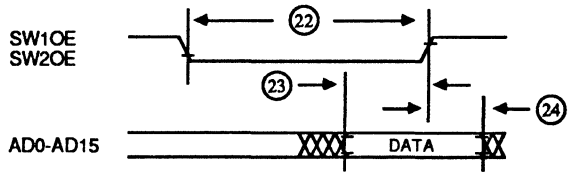


Figure 18 Read Switch Timing

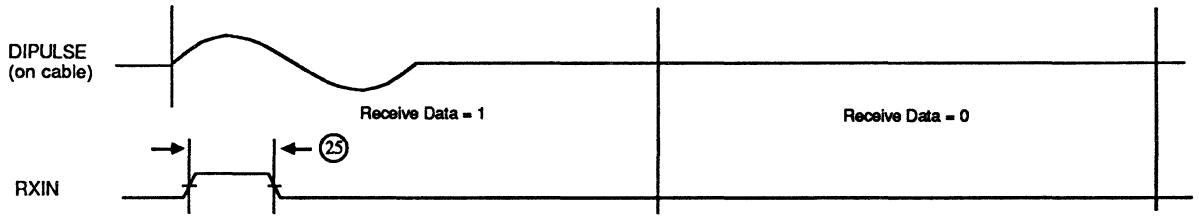


Figure 19 Receive Data

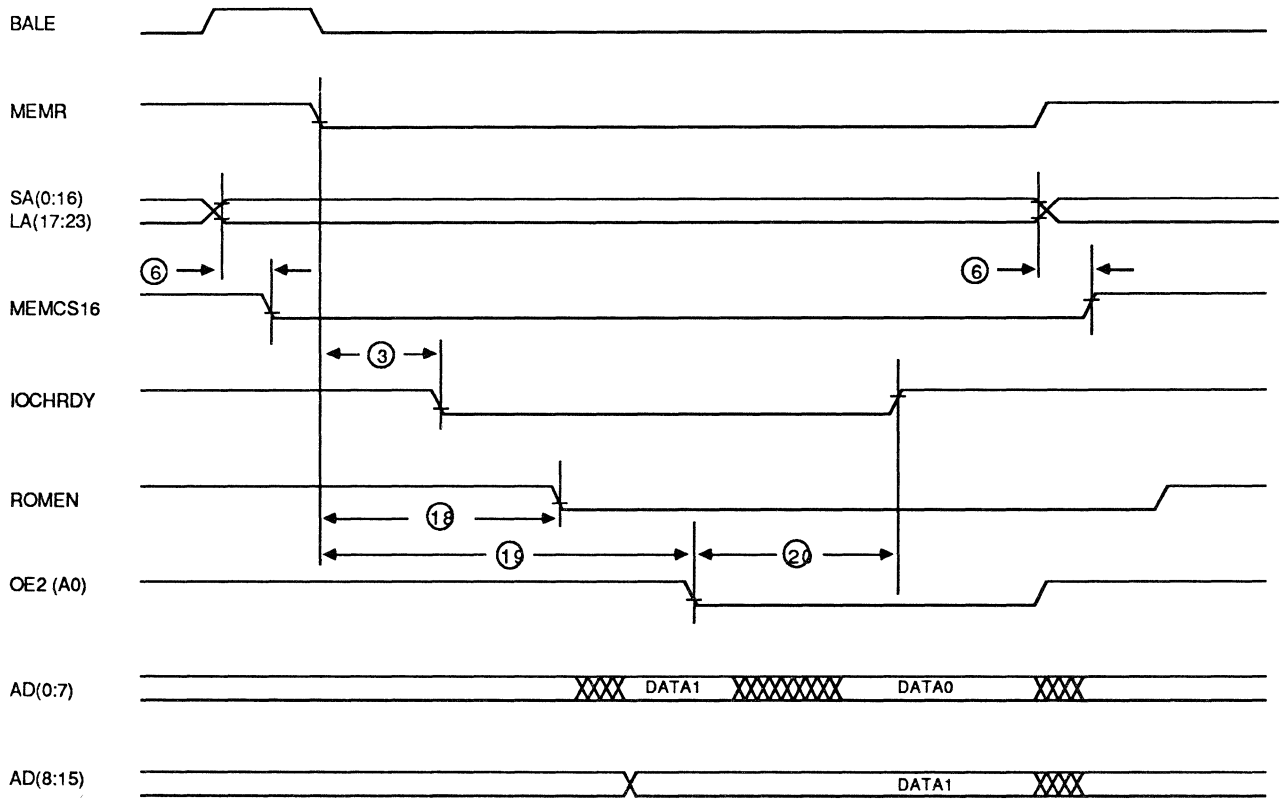


Figure 20 16-bit ROM Read from 8-bit Device

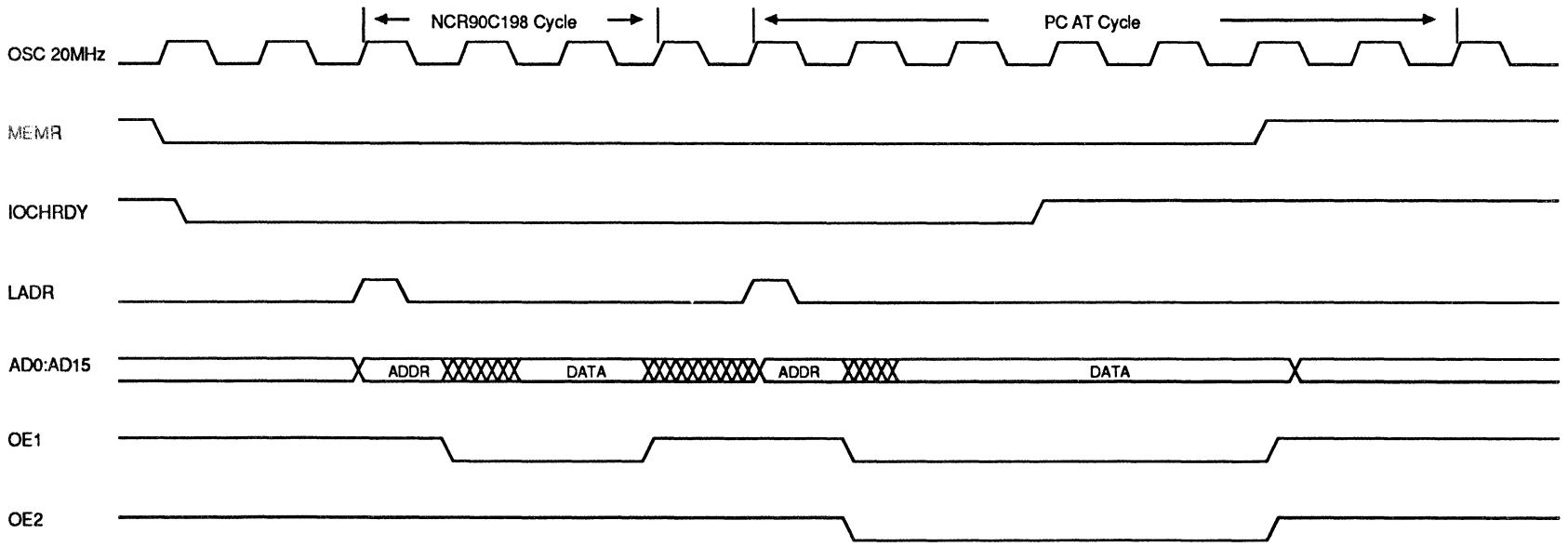


Figure 22 PC AT/NCR90C198 Memory Read Cycle, Worst Case

SALES INFORMATION

For more information on the NCR90C198, or any other Communications Group device, please call the NCR hotline at

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