

UNIVERSAL ASSEMBLER .VERSION 2.2.B JULY 29, 1979 (IN-HOUSE)

CONFIDENTIAL PROPRIETARY INFORMATION

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COMMAND LINE WAS: SNAP3 PROC14G3.PROD,,,PROC14G3;GBQLX

- INCLUSION A: PROCINC/TXT:DR0
- INCLUSION B: PROC14G3/LIB:DR0.PMACMIC
- INCLUSION C: PROC14G3/LIB:DR0.GMACROZ
- INCLUSION D: PROC14G3/LIB:DR0.PROCEQUS
- INCLUSION E: PROC14G3/LIB:DR0.BDEF1800
- INCLUSION F: PROC14G3/LIB:DR0.MDEF1800
- INCLUSION G: PROC14G3/LIB:DR0.PORTEQUS
- INCLUSION H: PROC14G3/LIB:DR0.PORTASGN
- INCLUSION I: PROC14G3/LIB:DR0.PROCPARM

PROGRAM NAME: PROD

PROGRAM ADDRESS BLOCKS:	010000	/ABSOLUTE/	SIZE=000000	(ABS)
	167400	/SYSIVR/	SIZE=000400	(ABS)
	170000	/SYSROM/	SIZE=000047	(ABS)
	002000	/PRODL/	SIZE=002000	(ABS)
	000000	/PRODP/	SIZE=004000	(REL)

EXTERNAL DEFINITIONS:

FETCHRW	002000	FETCHW	002003	FETCH	002005	FETCHN	002010
FETCHL	002013	SRVDO	002645	CALLCC	002026	NOJ	002444
CALL	002032	MEMPF\$	002221	PCMOD	002100	PSHST0	002054
PUSH	002111	PUSHI	002117	EIROJ	002142	JUMP	002447
RETURN	002152	RETCC	002147	RETS	002206	POPST0	002155
POP	002212	STKS	002277	RIN16	003202	SYSRETO	002372
SIR0	002421	SIRX	002430	JUMPC	002441	LD6	002467
LD7	002502	L7S	002523	LDS	002537	AP4	002542
AP7	002551	APS	002565	SRVRPT	002636	SRVNXT	002643
SRVRTW	002653	BEEP	002703	CLICK	002715	AC\$DO	002724
BT	003000	RIN256	003105	RIND	003210	RINST	003113
BCP	003123	BFSB	003215	BFAC	003221	BFS	003273
SLC	003341	SRC	003350	SRE	003361	CCS	003400
PLR	003405	PSR	003427	INCPA	003444	INCP	003451
DECPA	003473	DECP	003500	DECX	003522	INCX	003525
DS	003631	DLHL	003633	DL	003637	BRL	003714
EI	003730	DI	003741				

EXTERNAL REFERENCES (UNDEFINED SYMBOLS):

SCROMLI SCRAMI SYSRET1 IVIOL\$ DL\$DO SCDON SCLST

UNUSED LABELS:

BTR

- |     |          |     |    |      |    |   |
|-----|----------|-----|----|------|----|---|
| 1.  | . 2.14.G | HJS | 79 | NOV  | 30 | INSERT TIMING FOR THIS VERSION                    |
| 2.  | . 2.14.F | HJS | 79 | OCT  | 8  | CHANGE OVER TO HONEYWELL BEEPER (SOUNDS BETTER)   |
| 3.  | . 2.14.E | HJS | 79 | AUG  | 13 | FINAL CLEANUP BEFORE WORKING VERSION              |
| 4.  | . 2.14.D | HJS | 79 | AUG  | 10 | FIX THE BUGS STILL LEFT                           |
| 5.  | . 2.14.C | HJS | 79 | JUL  | 27 | CLEANUP NEW CODE BEFORE TEST IT                   |
| 6.  | . 2.14.B | HJS | 79 | APR  | 17 | RE-ORDER ROUTINES TO FIT BETTER                   |
| 7.  | . 2.14.A | HJS | 79 | APR  | 2  | START MODIFICATIONS FOR INTERNAL RIM 3800         |
| 8.  | *        |     |    |      |    |   |
| 9.  | . 2.13.B | HJS | 79 | FEB  | 7  | ENABLE COMM ON 3800 PROCESSORS                    |
| 10. | . 2.13.A | HJS | 79 | JAN  | 22 | FIX REGS BUG TO ALLOW ACCESS TO PROTECTED STACK   |
| 11. | *        |     |    |      |    |   |
| 12. | . 2.12.C | HJS | 78 | OCT  | 12 | CORRECT MEMORY FAULTS SO PC MATCHES 6600 PC       |
| 13. | . 2.12.A | HJS | 78 | SEP  | 05 | REFORMAT, RE-COMMENT, AND FIX STACK FOR ACCESS    |
| 14. | . 12     |     |    |      |    | SET VERSION NUMBERS TO MATCH ? FROM DEBUG         |
| 15. | *        |     |    |      |    |   |
| 16. | . 2.9.L  | HJS | 78 | JUL  | 18 | FIX ANOTHER HONEYWELL BUG                         |
| 17. | . 2.9.K  | HJS | 78 | JUN  | 16 | FIX BUG INTRODUCED IN HONEYWELL CODE (TZ TO FZ)   |
| 18. | . 2.9.K  | HJS | 78 | APR  | 23 | SPLIT PROC, MAKE RELOCATABLE, CHANGE APF, ADD AML |
| 19. | . 2.9.J  | HJS | 78 | MAR  | 20 | RESTRUCTURE INTERRUPT SEQUENCE & MINOR MODS       |
| 20. | . 2.9.I  | HJS | 78 | FEB  | 27 | CORRECT 9.H FOR FAULT CLEANUP                     |
| 21. | . 2.9.H  | HJS | 78 | FEB  | 16 | EVERYBODY MEMPF'S, KEYBOARD SCAN, & SIR CHANGE    |
| 22. | . 2.9.G  | HJS | 78 | FEB  | 3  | CORRECT TIMING, COMMENTS, & ADD POR TIMEOUT       |
| 23. | . 2.9.F  | HJS | 78 | JAN  | 11 | FIXING MIN/MOUT TIMINGS                           |
| 24. | . 2.9.E  | HJS | 78 | JAN  | 4  | TESTING REPEATED KEYIN CONTROLS                   |
| 25. | . 2.9.D  | HJS | 77 | DEC  | 21 | CORRECT STL INSTRUCTION                           |
| 26. | . 2.9.C  | HJS | 77 | DEC  | 13 | BACK OFF FROM KBD RPT & RE-DO STL FOR TIMING      |
| 27. | . 2.9.B  | HJS | 77 | NOV  | 20 | INCLUDE TIMINGS AS CALCULATED & FIX MINOR BUGS    |
| 28. | . 2.9.A  | HJS | 77 | NOV  | 14 | CHANGE KEYBOARD CODE TO AID REPEATED KEY CONTROL  |
| 29. | *        |     |    |      |    |   |
| 30. | . 2.8.B  | HJS | 77 | SEP  | 22 | MTI CHANGE SO LENGTH IS 2 BYTE NUMBER             |
| 31. | . 2.8.A  | HJS | 77 | SEP  | 19 | MTI CHANGE TO ALLOW MFRPT ON ANY INTERRUPT        |
| 32. | *        |     |    |      |    |   |
| 33. | . 2.7.   | HJS | 77 | SEP  | 7  | MINOR BUG-FIX AND OPTIMIZATION FOR RELEASE        |
| 34. | *        |     |    |      |    |   |
| 35. | . 2.H.B  | HJS | 77 | AUG  | 31 | MTI SPECIAL VERSION                               |
| 36. | *        |     |    |      |    |   |
| 37. | . 2.5.C  | HJS | 77 | AUG  | 16 | UPDATE COMMENTS ON THE CODE                       |
| 38. | . 2.5.B  | HJS | 77 | JULY | 13 | CORRECTED NAMES FOR COM REGISTERS                 |
| 39. | . 2.5.A  | HJS | 77 | JULY | 12 | UP TO NEXT NEW VERSION NUMBER                     |
| 40. | *        |     |    |      |    |   |
| 41. | . 2.4.B  | HJS | 77 | JULY | 12 | FIXED ILLEGAL MAR CHANGE IN REGL RETURN TO FETCH  |
| 42. | .        |     |    |      |    | FIXED FILE TO CONFORM TO VRP FORMAT (A LITTLE)    |
| 43. | . 2.4.A  | HJS | 77 | JULY | 7  | INITIAL PRE-RELEASE OF THE MICRO-CODE             |

44.			*			
45.				INC	PROCINC	
46.						
47.	002000	Fetchw: mwait, <del>REMPF2</del>		ORG	PROD	LOGICAL SPACE DEFINED IN PLACE
48.	000000	LDIP <del>MODW, PSWI</del>		ORG	0	PHYSICAL SPACE RELOCATABLE
49.	002000	TSTIT, SW64K		USE	PRODL	USE THEM BOTH
50.	000000	BAA <del>FETCH, TZ</del>		USE	PRODP	PUT THE CODE IN PHYSICAL SPACE
51.	002000L	<del>LDIP</del> <del>MODW, PSWI</del>		LOC	PRODL, 2	WITH ADDRESSES IN LOGICAL SPACE

LDX BR2DAH  
LDRK STW, ~~STKPE~~  
BAA FETCH

. FETCH NEXT INSTRUCTION

54.			*			
55.						
56.						
57.						
58.						
59.	002000L	11000100 11111111		FETCHRW: MWAIT	, IGNORE	ENTRY IF WRITE OPERATIONS & TEMPORARY MODW
60.					. 3.10	
61.	002001L	00110001 11011100		LDPP	MODW, PSWI	RESTORE CORRECT PROTECTION BEFORE FETCH
	002002L	00110111 00000100				
62.						(EXTRA MWAIT AS FAST AS BRANCH AROUND IT)
63.	002003L	11000100 11111100		FETCHW: MWAIT	, MEMPF2	ENTRY IF WRITE OPERATIONS LAST
	002004L	11000111 01101111				
64.					. 2.70	
65.	002005L	00110001 11001001		FETCH: DLDX	PC2MR, , IMAR	ENTRY IF MAR MUST BE LOADED (NORMAL)
	002006L	00110001 11101000				
	002007L	00110111 00001100				
66.					. 2.50	
67.	002010L	00110001 10001001		FETCHN: DLDX	MR2PC, , SMR	ENTRY FOR JUMP OR CALL (P.C. OK?)
	002011L	00110001 10101000				
	002012L	00110111 01000111				
68.					. 2.05	
69.	002013L	01010001 00000000		FETCHL: LDPI	LIMP, 0	IMPLICIT REGISTER ZERO
	002014L	00110111 00000001				
70.					. 1.60	
71.	002015L	00110001 00110000		TSTPT	FI, SRVREQ	SERVICE REQUEST?
72.	002016L	11010010 01011010		BRA	SRVDO, FZ	YES, DO IT & SAVE MAR ETC. FOR RETURN
73.						
74.	002017L			SRVEND		SERVICE RE-ENTRY, IMP, MAR & PC ALL OK?
75.	002017L	11000100 11110000		FETLIMP	MWAIT	, MEMPF2
	002020L	11000111 01101111				ERROR IF MEMORY FAULT
76.					. 1.10	
77.	002021L	00110111 00001100		STB	IMAR	!! SPEEDUP FOR THOSE THAT CAN USE IT !!
78.	002022L	00110001 00110110		LDPP	LIREG, MDR	LOAD INSTRUCTION REGISTER
	002023L	00110111 00000000				
79.	002024L	00111001 00110100		SRVID	BRPX	IDCOD
	002025L	10101111 00110011				GO TO THE ROUTINE
80.						
81.						
82.						
83.						

. NOTE: PC LEFT POINTING AT THE INSTRUCTION BYTE JUST FETCHED  
 . MAR LEFT POINTING AT THE NEXT BYTE SO IF MULTI-BYTE  
 . INSTRUCTION, CAN START WITH AN SMR FOR A LITTLE SPEEDUP.

*CALL POP:  
 BRA POPR, FC, IZ*

```

86.
87. 002026L
88.
89.
90.
91.
92.
93.
94.
95.
96.
97.
98.
99.
100.
101. 002026L 11001000 10011100
102. 002027L 00110001 00110001
    002030L 01000101 00000001
103. 002031L 11010011 11011011
104.
105. 002032L
106.
107.
108.
109.
110. 002032L 00110111 01000111
111. 002033L 01010001 00001001
    002034L 00110111 00000001
112. 002035L 11000100 11100010
    002036L 11000111 01101110
113. 002037L 00110111 00001100
114. 002040L 00110001 00110110
    002041L 01101111 11110010
115. 002042L 00110111 01000111
116. 002043L 11001110 11111111
    002044L 11000100 11011011
    002045L 11000111 01101110
117. 002046L 00110001 00110110
    002047L 01101111 11110001
118. 002050L 00110111 00001100
119. 002051L 00110001 10001001
    002052L 00110001 10101000
120. 002053L 01010001 10111111
    
```

```

*
CALLCC:
. ( 102) CCC.LSB.MSB      CONDITIONAL CALL
. 7.90 (1.05 NOT TAKEN)  (SP-2 | SP-1) <- PC
. ( 102) CFC.LSB.MSB      FALSE CARRY
. ( 112) CFZ.LSB.MSB      FALSE ZERO (.NE.)
. ( 122) CFS.LSB.MSB      FALSE SIGN (.GE.)
. ( 132) CFP.LSB.MSB      FALSE PARITY (EVEN)
. ( 142) CTC.LSB.MSB      TRUE CARRY
. ( 152) CTZ.LSB.MSB      TRUE ZERO (.EQ.)
. ( 162) CTS.LSB.MSB      TRUE SIGN (.LT.)
. ( 172) CTP.LSB.MSB      TRUE PARITY (ODD)

. 5.45 (111 102) UR      USER RETURN

BRA USERET, FC, IZ      USER RETURN, NOT A CALL!
TSTIP ,STUSCF,STATUS    IS USER CC CORRECT?

BRA NOJ,TZ              NO, DO NOJ NOT A RETURN

*
CALL:
. ( 106) CALL.LSB.MSB    UNCONDITIONAL CALL
. 7.45 (SP-2 | SP-1) <- PC
. SP <- SP - 2; PC <- NN
.
STB SMR
LDPI LIMP,PCL          PC TO BE PUSHED ONTO THE STACK

MWAIT ,MEMPF$

STB IMAR
LDRP  TEMPL,MDR        SAVE LSB

STB SMR
MWAIT NOOP,MEMPF$

LDRP  TEMPH,MDR        SAVE MSB

STB IMAR
DLDX  MR2PC            POINT MAR TO THE NEXT INSTRUCTION
                        SO PUSHED P.C. IS CORRECT

BAL ,PCMOD
    
```

*BRA POPR, FC, IZ*

. SUBROUTINE CALL AND STACK PUSH

121.  
 122. 002054L 01101111 10110000  
 123. 002055L  
 124.  
 125.  
 126.  
 127.  
 128.  
 129. 002055L 00110001 11011100  
 002056L 01010101 11111011  
 002057L 00110111 00000100  
 130. 002060L 00110001 11101010  
 131. 002061L 00110001 11011011  
 002062L 01010100 00000010  
 132. 002063L 01010011 01000000  
 002064L 00110111 10001011  
 133. 002065L 00110111 11000000  
 134. 002066L 00110001 11011111  
 002067L 00110111 00101001  
 135. 002070L 00110111 00001001  
 136. 002071L 00110001 11011111  
 137. 002072L 11000100 11000101  
 002073L 11000111 11000000  
 138. 002074L 00110111 00001100  
 139. 002075L 11001111 11000001  
 140. 002076L 00110111 00101001  
 141. 002077L 11101111 00000000  
 142.  
 143.  
 144.  
 145. 002100L  
 146.  
 147.  
 148. 002100L 11000100 10111111  
 002101L 11000111 01101110  
 149. 002102L 00110001 11011100  
 002103L 00110111 00000100  
 150. 002104L 01110001 11110010  
 002105L 00110111 11000000  
 002106L 01110001 11110001  
 002107L 00110111 11100000  
 151. 002110L 11001111 11110111

+  
 PSHSTO: BAS LINK,CC (2.80) IN-PAGE ENTRY TO PUSH  
 PSHSTK OFF-PAGE ENTRY (LINK RETURN PRE-LOADED)  
 . 2.70 + 0.20 INTO MEMORY WAIT MUST HAVE CARRY CLEAR TO USE THIS ENTRY

. NOTE: CAN NOT PARITY CHECK IN HERE OR LOST FOREVER WITH  
 MEMPF\$ & SYS CALL & PUSH !!!

DOPIP MODW,ND,-1-SWUSER,PSWI ALLOW STACK IN ACCESS PROTECTED MEM

LDX SP2MRH POINT TO MEMORY STACK  
 DOTIP ,SB,2,SPIL UPDATE THE SP

DOPI SPOL,OR,0100 MAKE SURE EVEN & WRAP AROUND (MOD 32/64)

LDPT MAROL SAVE UPDATED LSB  
 LDPP MDW,IMPI,DIRP STORE LSB THERE

STB DIMP  
 LDTP IMPI PRE-LOAD MSB DATA TO WRITE  
 MWAIT ,MEMPF\$ \*\*\* LET THE CALLER WORRY ABOUT IT \*\*\*

STB IMAR NOW POINT & DO THE MSB TO FINISH OFF  
 DELAY 2  
 LDPT MDW  
 MEMPF\$ BRR LINK

. \*\*\* NOTE ROUTINE CALLING PSHSTK OR PSHSTO MUST HAVE MWAIT ,ADDR \*\*\*  
 . \*\*\* AND MUST RESTORE MODW FROM THE PSW \*\*\*

\*  
 PCMOD: RETURN FROM PSHSTK AND SET NEW PC  
 . 1.60 (WITH MWAIT WITHOUT FETCHN)

MWAIT ,MEMPF\$

LDPP MODW,PSWI RESTORE CORRECT MODE

DL DPR MARO,TEMP LOAD UP SAVED P.C.

BRA FETCHN GO TO ADDRESS AT MACRO LEVEL

TSTIT  
 BRA  
 LDPR  
 SW64K  
 PSWSTN,TZ  
 STW, SSTKPE

TSTIT  
 BRA  
 LDPR  
 SW64K  
 PCMODX,TZ  
 STW, USTKPE

```

152.
153. 002111L
154.
155.
156.
157.
158.
159. 002111L 01010001 11111111
    002112L 01101111 10110000
    002113L 11001000 11010010
160. 002114L 01010001 00000110
    002115L 00110111 00000001
161. 002116L 11001111 11010010
162.
163. 002117L
164.
165.
166.
167. 002117L 00110111 01000111
168. 002120L 01010001 00001111
    002121L 00110111 00000001
169. 002122L 11000100 10101101
    002123L 11000111 01101110
170. 002124L 00110111 00001100
171. 002125L 00110001 00110110
    002126L 00110111 10001111
172. 002127L 00110111 01000111
173. 002130L 00110001 10001001
    002131L 00110001 10101000
    002132L 00110111 00001001
174. 002133L 11000100 10100100
    002134L 11000111 01101110
175. 002135L 00110001 00110110
    002136L 00110111 10001111
    002137L 00110111 00001000
176. 002140L 01010001 11111111
    002141L 11001111 11010011

```

```

*
PUSH:
. 4.05 ( 070) PUSH (SP-1 | SP-2) <- HL; SP <- SP - 2
. 3.70 (.062 070) PUSH BC
. 3.70 (.174 070) PUSH DE
. 3.70 (.022 070) PUSH XA
    BRS PSHSTK, F@, IZ, FETCH, CC REG PAIR SPECIFIED!
    LDPI LIMP, URL DEFAULT
    BRA PSHSTK
*
PUSHI:
. ( 051) PUSH.LSB.MSB PUSH CONSTANT (ADDRESS?) ONTO STACK
. 6.20 (SP-1 | SP-2) <- NN; SP <- SP - 2
    BAA LLOP, F@, IZ
    STB SMR GET THE IMMEDIATE VALUE
    LDPI LIMP, IMPL AND HIDING PLACE
    MWAIT ,MEMPF$
    STB IMAR
    LDPP IMPO, MDR GOT LSB
    STB SMR
    DLDX MR2PC,,DIMP SAVE THE UPDATED P.C.
    MWAIT ,MEMPF$
    LDPP IMPO, MDR, IIMP GOT MSB, POINT CORRECTLY FOR PUSH
    BRC PSHSTO,,FETCH, RETURN FROM PUSH TO FETCH WAIT
    WS

```

LLOP BAA X LLDL

. RETURN CODES USER & CONDITIONAL & REGULAR, AND STACK POPPING

179.								
180.	002142L							
181.								
182.								
183.								
184.								
185.	002142L	11011011	11011000		BRA	JUMP,TO,IO		
186.								
187.	002143L							
188.								
189.								
190.								
191.								
192.	002143L	00110001	11011100					
	002144L	01010011	00000100					
	002145L	00110111	10001100					
193.								
194.	002146L	11001111	10010101					
195.								
196.	002147L							
197.								
198.								
199.								
200.								
201.								
202.								
203.								
204.								
205.								
206.								
207.								
208.	002147L	00110001	00110001					
	002150L	01000101	00000001					
209.	002151L	11000011	11110111					
210.								
211.	002152L							
212.								
213.								
214.								
215.	002152L	01010001	00001001					
	002153L	00110111	00000001					
216.	002154L	01010001	01111001					

\* CALL UK

BRA CALLCC, T@, IZ

EIROJ:

. 6.40 (062 050) EUR

ENABLE INTERRUPTS & USER & PC ← (SP+1 | SP); SP ← SP + 2

. 4.10 (111 050) EJMP.LSB.MSB

ENABLE INTERRUPTS & PC ← NN

\* BRA JUMP,TO,IO

USERET

. 6.40 (062 050) EUR

ENABLE INTERRUPTS & USER & PC ← (SP+1 | SP); SP ← SP + 2

. 5.45 (111 102) UR

USER RETURN

DOPIP PSWO,OR,SWUSER,PSWI SET USER MODE

TSTIT , SW69K  
BAA Return, T2  
Load 17, 16, 15  
BAA Return

STB MODW  
BRA RETURN

EXTERNALLY ALSO IN EMULATION AIDS

\* RETCC:

( 0C3) RET

CONDITIONAL RETURN

. 5.00 (0.45 NOT TAKEN)

PC ← (SP+1 | SP); SP ← SP + 2

( 003) RFC

FALSE CARRY

( 013) RFZ

FALSE ZERO (.NE.)

( 023) RFS

FALSE SIGN (.GE.)

( 033) RFP

FALSE PARITY (EVEN)

( 043) RTC

TRUE CARRY

( 053) RTZ

TRUE ZERO (.EQ.)

( 063) RTS

TRUE SIGN (.LT.)

( 073) RTP

TRUE PARITY (ODD)

TSTIP ,STUSCF,STATUS

BRA FETCHN,TZ

\* RETURN:

. 4.65 ( 007) RET

UNCONDITIONAL RETURN

PC ← (SP+1 | SP); SP ← SP + 2

LDPI LIMP,PCL .POP STACK INTO PROGRAMME COUNTER

BAL ,RETS RETURN FROM POP TO SPECIAL STARTUP

ACC DOP BAA DOP, FE, IZ



217.				*				
218.	002155L	01101111	10110000	POPST0:	BAS	LINK,CC	(3.65)	IN-PAGE CALL
219.	002156L			POPSTK				POP THE STACK TO IMP AND IMP-1
220.				. 3.55				CARRY MUST BE CLEAR TO USE THIS ENTRY
221.								
222.	002156L	00110001	11101010		LDX	SP2MRH		POINT INTO THE STACK AREA
223.	002157L	00110001	11011100		DOPIP	MODW,ND,-1-SWUSER,PSWI		ALLOW ACCESS TO PROTECTED MEMORY
	002160L	01010101	11111011		<i>TEST</i>	<i>sw by P</i>		
	002161L	00110111	00000100		<i>BRA</i>	<i>POPSTKN, TZ</i>		
224.	002162L	00110001	11001011	<i>POPSTKN</i>	LDX	SP2MRL,SMR		(SAVE 150 N.SEC BY INVERTING ORDER)
	002163L	00110111	01000111					
225.	002164L	01010101	10111111		DOTI	,ND,-1-0100		TURN OFF WRAP-AROUND BIT
226.	002165L	01010010	00000010		DOTI	,AC,2		SKIP TO NEXT ENTRY TO POP
227.				.				NOTE: (STKS) ASSUMES FALSE CARRY
228.				.				GENERATED HERE (TO SAVE WORD)
229.	002166L	01010011	01000000		DOPI	SPOL,OR,0100		SET BIT ON TO FINISH WRAP-AROUND
	002167L	00110111	10001011					
230.	002170L	11000100	10000111		MWAIT	,MEMPF\$		
	002171L	11000111	01101110					
231.	002172L	00110111	00001100		STB	IMAR		
232.	002173L	00110001	00110110		LDPP	IMPO,MDR		SAVE LSB DATA
	002174L	00110111	10001111					
233.	002175L	00110111	01000111	<i>TEST SWB4K</i>	STB	SMR,DIMP		GET MSB DATA
	002176L	00110111	00001001	<i>BRA POPSTKX,TZ</i>				
234.	002177L	11000100	10000000	<i>BRA POPSTKX,TZ</i>	MWAIT	,IGNORE		PUT MEMPF\$ AFTER LDPP, BETTER STACK!
235.	002200L	00110001	11011100	<i>LDPP STW,STKPE</i>	LDPP	MODW,PSWI		
	002201L	00110111	00000100					
236.	002202L	00110001	00110110	<i>POPSTKX</i>	LDPP	IMPO,MDR		SAVE MSB DATA
	002203L	00110111	10001111					
237.	002204L	11100000	00000000		BRR	LINK,F@,MP		
238.	002205L	11001111	01101110		BRA	MEMPF\$		(AND DO A SLIGHT SPEEDUP)
239.				*				
240.	002206L			RETS:				
241.				. 0.65				
242.								
243.	002206L	00110001	11101000		DLRX	PC2MR,,SMR		LOAD THE MAR FROM P.C. VALUE (NO IMAR)
	002207L	00110001	11001001					
	002210L	00110111	01000111					
244.	002211L	11001111	11110100		BRA	FETCHL		
245.				*				
246.	002212L			POP:				
247.				. 4.30	( 060)	POP		HL IS POPPED FROM STACK
248.				. 3.95	(062 060)	POP		BC
249.				. 3.95	(174 060)	POP		DE
250.				. 3.95	(022 060)	POP		XA
251.				.				RP ← (SP+1   SP); SP ← SP + 2
252.								
253.	002212L	01010001	11111010		BRS	POPSTK,F@,IZ,FETCH,CC		IMP POINTS TO REG-PAIR ALREADY
	002213L	01101111	10110000					
	002214L	11001000	10010001					
254.	002215L	01010001	00000110		LDPI	LIMP,URL		DEFAULT USES HL
	002216L	00110111	00000001					

255. 002217L 11001111 10010001

BRA POPSTK

. MEMORY PARITY FAULT CODE! VERY WEIRD!

258.					
259.	002220L	01011001	11111011	MEMPF2	BPGX s IF FROM WRONG EVEN/ODD PAGE PAIR
260.	002221L			MEMPFs:	
261.				. *****	
262.				. P.C. UPPED TO NEXT INST. WHEN GET MEMPF, WILL ALWAYS ASSUME IT CORRECT	
263.				. HOPING TO POINT TO THE NEXT INSTRUCTION.	
264.				. *****	
265.					
266.	002221L	00110001	00110111	LDRP	TEMP1,STEK,CC GET AND SAVE STATUS WORD
	002222L	01101111	10110001		
267.				. STB	CMPF CLEAR THE FAULT (NOT NECESSARY)
268.				.	(THE NEXT READ/WRITE DOES IT)
269.	002223L	00110001	11011100	DOPIP	MODW,ND,-1-SWUSER,PSWI ENABLE MEMORY ACCESSING
	002224L	01010101	11111011		
	002225L	00110111	00000100		
270.	002226L	01010001	00001111	LDPI	LIMP,IMPL USING HIDDEN REGS AND PSHSTK
	002227L	00110111	00000001		
271.	002230L	00110001	10001111	DLDX	MR2IM,DIMP SAVE THE MAR ON THE STACK
	002231L	00110111	00001001		
	002232L	00110001	10101111		
272.	002233L	01010101	11000000	DOTI	,ND,0300
273.	002234L	01000000	10000000	TSTIT	XR,0200 HIGH BIT ON, NEXT BIT OFF?
274.	002235L	11000010	01010111	BRA	MEMNBAS,FZ NO, IN ANOTHER 16K CHUNK
275.	002236L	01010001	11101111	DLRPI	MAR0,SEBRLS,SMR IN BASED AREA, GET BASE REG VALUE
	002237L	00110111	11100000	TSTIP	,SW64K,PSWI
	002240L	01010001	10101011	BRA	MEMN64K,STZ
	002241L	00110111	11000000	LDPR	STW,ST16E
	002242L	00110111	01000111	-STB	STW
276.	002243L	00110001	11011111	LDTP	IMPI SO ADDRESS MATCHES 5500 VALUE
277.	002244L	11000100	01011011	MWAIT	,MEMPQ !!! HELP !!!
	002245L	11000111	01010100		
278.	002246L	00110010	00110110	DOPP	IMPO,AC,MDR ADD IN BASING
	002247L	00110111	10001111		
279.	002250L	00110111	00001000	MEMNBAS	STB IIMP POINT TO LSB TO SAVE
280.	002251L	01010001	01010100	BRC	<del>PSHSTO</del> STW,ST16E PUSH MAR VALUE ON THE STACK
	002252L	11001111	11010011		
281.	002253L	01010001	00000110	MEMPQ	LDTI SRSYSMF ASSUME THE WORST, GOT ANOTHER FAULT
282.	002254L	11000100	01010011	MWAIT	,MEMPX !!! HELP !!!
	002255L	11000111	01001001		
283.	002256L	01110001	11110001	TSTIR	,STLSP,TEMP1 SP: SECTOR TABLE PARITY FAULT
	002257L	01000101	10000000		
284.	002260L	11000010	01000111	BRA	MEMPS,FZ
285.	002261L	01000101	01000000	TSTIT	,STLW WV: WRITE VIOLATION FAULT
286.	002262L	11000010	01000011	BRA	MEMPW,FZ
287.	002263L	01000101	00000001	TSTIT	,STLA AV: ACCESS VIOLATION FAULT
288.	002264L	11000010	01000101	BRA	MEMPA,FZ
289.	002265L	01010001	00010010	LDTI	SRMEMPE
290.	>002266L	01011001	11111111	MEMPX	BRAX SCROMLI MP: MEMORY PARITY FAULT
	>002267L	11001111	11111111		THESE ERRORS GO TO ROM VECTORS!
291.					
292.	002270L	01010001	00011011	MEMPS	LDTI SRSTPE SECTOR, ROM VECTOR
293.	002271L	11001111	01001001	BRA	MEMPX

. MEMORY PARITY FAULT CODE! VERY WEIRD!

294.							
295.	002272L	01010001	00011000	MEMPA	LDTI	SVAVIOL	ACCESS, RAM VECTOR
296.	002273L	11001111	01000010		BRA	MEMPR	
297.							
298.	002274L	01010001	00010010	MEMPW	LDTI	SVWVIOL	WRITE, RAM VECTOR
299.	>002275L	01011001	11111111	MEMPR	BRAX	SCRAMI	AND THESE GO TO RAM VECTORS
	>002276L	11001111	11111111				

302.						
303.	002277L					
304.				( 065) STKS	SAVE STACK CONTENTS	
305.				-0.30 + C * 8.80	(HL+1   HL) <- (SP+1   SP)	
306.					HL <- HL + 2; SP <- SP + 2	
307.					C <- C - 1; UNTIL = 0 (16)	
308.						
309.				(111 065) STKL	LOAD STACK CONTENTS	
310.				-0.30 + C * 9.20	(SP-1   SP-2) <- (HL-1   HL)	
311.					HL <- HL - 2; SP <- SP - 2	
312.					C <- C - 1; UNTIL = 0 (16)	
313.						
314.				2.80 (022 065) SYSM	TO XA, MOVE SYSTEM SAVE AREA	
315.				2.80 (062 065) SYSM	TO BC	
316.				2.80 (174 065) SYSM	TO DE (SWAP WITH REG PAIR)	
317.				2.80 (176 065) SYSM	TO HL	
318.					SP-1   SP <-> RP	
319.						
320.	002277L	11001000	00100111	BRA STKL,F@,IZ	LOAD THE STACK (OR MOVE IT)	
321.	002300L	01010001	00001111	LDPI LIMP,IMPL	POINT TO HIDDEN REGISTERS	
	002301L	00110111	00000001			
322.	002302L	01010001	00111011	BRC POPST0	GET THE TOP STACK ENTRY (M. POINTER)	
	002303L	11001111	10010010			
323.	002304L	00110001	11100101	DLRX HL2MR,,IIMP	POINT TO MEMORY AND CORRECT IMP	
	002305L	00110001	11000110			
	002306L	00110111	00001000			
324.	002307L	00110001	11011111	LDPP MDW,IMPI	STORE THE LSB	
	002310L	00110111	00101001			
325.	002311L	00110001	11010110	DADDP URO+UR,URI+UR,2	UPDATE THE HL POINTER (POPST DOES CC)	
	002312L	01010010	00000010			
	002313L	00110111	10000110			
	002314L	00110001	11010101			
	002315L	00110110	10000101			
326.	002316L	11000100	00110001	MWAIT ,MEMPF\$		
	002317L	11000111	01101110			
327.	002320L	00110111	00001100	STB IMAR,DIMP	STORE THE MSB	
	002321L	00110111	00001001			
328.	002322L	00110001	11011111	LDPP MDW,IMPI		
	002323L	00110111	00101001			
329.	002324L	01010001	00000000	LDPI LIMP,0	RESET IMP FOR STKS OP-CODE	
	002325L	00110111	00000001			
330.	002326L	01011001	11111001	BRAX RIN16	DO REPEATED INSTRUCTION	
	002327L	11001111	01111101			

*Handwritten notes:*  
 LDX HL2DRL  
 DOP URO+UR,AC,2  
 LDX HL2DRL  
 DOP URO+UR,IT  
 STB IIMP  
 LDPP MDW,IMPI  
 NDCP

```

331.
332. 002330L
333.
334.
335.
336.
337.
338.
339.
340.
341.
342.
343.
344. 002330L 11011010 11111111
345. 002331L 00110001 11100101
    002332L 00110001 11000110
    002333L 00110111 01000111
346. 002334L 01010001 00001110
    002335L 00110111 00000001
347. 002336L 00010111 10110010
348. 002337L 00110001 11010110
    002340L 01010100 00000010
    002341L 00110111 10000110
349. 002342L 11000100 00011101
    002343L 11000111 00010110
350. 002344L 00110111 00001101
351. 002345L 00110001 00110110
    002346L 00110111 10001111
352. 002347L 00110111 01000111
    002350L 00110111 00001000
353. 002351L 00110001 11010101
    002352L 01010100 00000000
    002353L 00110111 10000101
354. 002354L 11000100 00010011
    002355L 11000111 01101110
355. 002356L 00110001 00110110
    002357L 00110111 10001111
356. 002360L 01010001 00001101
    002361L 11001111 11010011
357. 002362L 01010001 00000001
    002363L 00110111 00000001
358. 002364L 11000100 00001011
    002365L 11000111 01101110
359. 002366L 00110001 11011100
    002367L 00110111 00000100
360. 002370L 01011001 11111001
    002371L 11001111 01111101
    
```

\*  
 STKL  
 . (111 065) STKL  
 . -0.30 + C \* 9.20  
 .  
 .  
 . 2.80 (062 065) SYSM  
 . 2.80 (174 065) SYSM  
 . 2.80 (176 065) SYSM  
 . 2.80 (022 065) SYSM  
 .

LOAD STACK CONTENTS  
 (SP-1 | SP-2) <- (HL-1 | HL)  
 HL <- HL - 2; SP <- SP - 2  
 C <- C - 1; UNTIL = 0 (16)

TO BC, MOVE SYSTEM SAVE AREA  
 TO DE  
 TO HL (SWAP WITH REGISTER PAIR)  
 TO XA  
 SP-1 | SP <-> RP

BRA SYSM,F0,IO DO SYS AREA SWAP!  
 DLRX HL2MR,,SMR

LDPI LIMP,IMPH POINT TO HIDDEN SAVE MSB

CCLR  
 DOPIP URO+URL,SB,2,URI+URL DECREMENT L

MWAIT ,STKLPF IF ERROR BE SURE TO DECR. H

STB DMAR  
 LDPP IMPO,MDR GET MSB AND POINT FOR LSB

STB SMR,IIMP

STKLPF DOPIP URO+URH,SB,0,URI+URH DECREMENT H

MWAIT ,MEMPF\$

LDPP IMPO,MDR GET LSB DATA

BRC PSHSTO PUT IT ON THE STACK

LDPI LIMP,1 SET IMPLICIT ODD!

MWAIT ,MEMPF\$  
 LDPP MODW,PSWI RESTORE STATE HERE BEFORE REPEAT LOOP

BRAX RIN16 AND REPEAT IF NEEDED

PCX  
 RIN16  
 MODW,PSWI  
 RIN16

```

361.
362. 002372L
363. >002372L 01011001 11111111
      >002373L 11001111 11111111
364.
365. 002374L 11111111 11111111
      002375L 11111111 11111111
      002376L 11111111 11111111
      002377L 11111111 11111111

```

```


*
SYSRET0:                                     OFF PAGE JUMP FOR SYSRETURN CODE

```

```

BRAX      SYSRET1
.
TABPAGE   PRODL

```


  
TSTIT ,SW64K
BAA RIN16,TZ
LDPA STW,4STKPE
DMA @IN16

366.					
367.	002400L				
368.					
369.					
370.					
371.					
372.					
373.					
374.					
375.					
376.					
377.					
378.					
379.					
380.					
381.					
382.	002400L 00110001 11011100	TSTIP	,SWUSER,PSWI	NOT ALLOWED IF IN USER MODE	
	002401L 01000101 00000100				
383.	002402L 11010010 11100000	BRA	IVIOL2,FZ		
384.	002403L 00110001 11011111	DOTIP	,ND,-2,IMPI	LOW BIT MUST BE OFF	
	002404L 01010101 11111110				
385.	002405L 01010011 01000000	DOPI	MAROL,OR,0100	BIT 6 MUST BE ON	
	002406L 00110111 11000000				
386.	002407L 00110111 00001001	STB	DIMP		
387.	002410L 00110001 11101111	LDX	IM2MRH	SAVE NEW REG PAIR	
388.	002411L 00110001 11011010	LDPP	IMPO,SPIH,IIMP	MOVE STACK TO REG PAIR	
	002412L 00110111 10001111				
	002413L 00110111 00001000				
389.	002414L 00110001 11011011	LDPP	IMPO,SPIH		
	002415L 00110111 10001111				
390.	002416L 00110001 10001011	DLDX	MR2SP	MOVE SAVED NEW STACK POINTER	
	002417L 00110001 10101010				
391.	002420L 11001111 11111010	BRA	FETCH		

+

SYSM

. 2.80 (022 065) SYSM XA  
 . 2.80 (062 065) SYSM BC  
 . 2.80 (174 065) SYSM DE  
 . 2.80 (176 065) SYSM HL

MOVE SYSTEM AREA  
 (SWAP POINTER WITH REGISTER PAIR)

SP-1 | SP <-> RP

<8-MSB> <X1 PPPPP0>  
 WHERE: 8-MSB IS CORRECT MSB  
 X IS 128 BYTE BOUNDARY  
 PPPPP IS STACK POINTER  
 1 IS FORCED ONE AND  
 0 IS FORCED ZERO FOR  
 CORRECT OPERATION



394.								
395.	002421L							
396.								
397.								
398.	002421L	00110111	01000111	STB	SMR			START TO GET THE OP-CODE
399.	002422L	11011000	11100000	BRA	IVIOL2,F@,IZ			MULTIPLE IMPLICIT IN A ROW IS ERROR
400.	002423L	01010001	00010000	LDPI	LIMP,IMP8			
	002424L	00110111	00000001					
401.	002425L	00110001	10001001	DLDX	MR2PC			
	002426L	00110001	10101000					
402.	002427L	11001111	11110000	BRA	FETLIMP			
403.								
404.	002430L							
405.								
406.								
407.								
408.								
409.								
410.								
411.								
412.								
413.	002430L	00110111	01000111	STB	SMR			START TO GET REAL OP-CODE
414.	002431L	11011000	11100000	BRA	IVIOL2,F@,IZ			MULTIPLE IMPLICIT IN A ROW IS ERROR
415.	002432L	01010101	00000111	DOPI	LIMP,ND,7			
	002433L	00110111	00000001					
416.	002434L	00110001	10001001	DLDX	MR2PC			
	002435L	00110001	10101000					
417.	002436L	11001111	11110000	BRA	FETLIMP			
418.								
419.	>002437L	01011001	11111111	IVIOL2	BRAX	IVIOL\$		
	>002440L	11001111	11111111					

422.					
423.	002441L		*	JUMPCC:	
424.				( 100)	JCC.LSB.MSB
425.				3.30 (0.85	NOT TAKEN)
426.				( 100)	JFC.LSB.MSB
427.				( 110)	JFZ.LSB.MSB
428.				( 120)	JFS.LSB.MSB
429.				( 130)	JFP.LSB.MSB
430.				( 140)	JTC.LSB.MSB
431.				( 150)	JTZ.LSB.MSB
432.				( 160)	JTS.LSB.MSB
433.				( 170)	JTP.LSB.MSB
434.					
435.	002441L	00110001	00110001	TSTIP	,STUSCF,STATUS
	002442L	01000101	00000001		
436.	002443L	11010010	11011000	BRA	JUMP,FZ
437.				*	
438.	002444L			NOJ:	
439.				0.50	( 045) NOJ.LSB.MSB
440.					
441.	002444L	00110111	00001100	STB	IMAR,IMAR
	002445L	00110111	00001100		
442.	002446L	11001111	11110111	BRA	FETCHN
443.				BRA	USE RET, F@, IO
444.	002447L			JUMP:	
445.				2.85	( 104) JMP.LSB.MSB
446.					
447.					
448.	002447L	00110111	01000111	STB	SMR
449.	002450L	11001110	11111111	MWAIT	NOOP, MEMPF2
	002451L	11010100	11010110		
	002452L	11000111	01101111		
450.	002453L	00110111	00001100	STB	IMAR
451.	002454L	00110001	00110110	LDRP	TEMP1, MDR
	002455L	01101111	11110001		
452.	002456L	00110111	01000111	STB	SMR
453.	002457L	11001110	11111111	MWAIT	NOOP, MEMPF2
	002460L	11010100	11001111		
	002461L	11000111	01101111		
454.	002462L	00110001	00110110	LDPP	MAROH, MDR
	002463L	00110111	11100000		
455.	002464L	01110001	11110001	LDPR	MAROL, TEMP1
	002465L	00110111	11000000		
456.	002466L	11001111	11110111	BRA	FETCHN

*DOP JMP  
BAA DOP<sup>2</sup>, F@, IZ*

*EI ROJ  
\*  
BRA USE RET, F@, IO*

LOAD'S AND STORE'S

*LD6 BF*  
*\* BAA BFLA, F@, IZ*

459.								
460.	002467L							
461.				LD6:				
462.				. 1.95	( 0D6)	LD.VVV		LOAD REG WITH IMMEDIATE VALUE
463.				.				D ← N
464.				.	( 006)	LA.VVV		LOAD A-REG
465.				.	( 016)	LB.VVV		
466.				.	( 026)	LC.VVV		
467.				.	( 036)	LD.VVV		
468.				.	( 046)	LE.VVV		
469.				.	( 056)	LH.VVV		
470.				.	( 066)	LL.VVV		
471.				.	( 076)	LX.VVV		LOAD X-REG WITH IMMEDIATE VALUE
472.	002467L	00110111	01000111		STB	SMR		READ THE DATA BYTE
473.	002470L	11001110	11111111		MWAIT	NOOP, MEMPF2		
	002471L	11010100	11000110					
	002472L	11000111	01101111					
474.	002473L	00110111	00001100		STB	IMAR		
475.	002474L	00110001	00110110		LDPP	I350, MDR, SMR		GET THE DATA
	002475L	00110111	10001101					
	002476L	00110111	01000111					
476.	002477L	00110001	10001001		DLDX	MR2PC		(MAKE THE COMMONEST INSTRUCTION FASTER)
	002500L	00110001	10101000					
477.	002501L	11001111	11110100		BRA	FETCHL		AND GO TO THE NEXT INSTRUCTION
478.								
479.	002502L							
480.					LD7:			
481.				. 1.75	( 3D7)	LRM		LOAD BYTE FROM MEMORY INTO REG
482.				.				D ← (HL)
483.				. 2.10	(062 3D7)	LRM		D ← (BC)
484.				. 2.10	(174 3D7)	LRM		D ← (DE)
485.				. 2.10	(022 3D7)	LRM		D ← (XA)
486.	002502L	11011000	10111000		BRA	LD7I, F@, IZ		SPECIFIED IMP?
487.	002503L	00110001	11100101		DLRX	HL2MR.,, SMR		NO, THEN USE HL AS ADDRESS
	002504L	00110001	11000110					
	002505L	00110111	01000111					
488.	002506L	11011111	10110011		BRA	LD7CMN		
489.	002507L	00110001	11001111		LD7I	DLDX	IM2MR, DIMP	POINT AND START MEMORY READ
	002510L	00110111	00001001					
	002511L	00110001	11101111					
490.	002512L	11001110	11111111		DELAY	1		
491.	002513L	00110111	01000111		STB	SMR		
492.	002514L	11001110	11111111		LD7CMN	MWAIT	NOOP, \$+1	PUT IN STANDARD 200 NS DELAY FROM READY
	002515L	11010100	10110010					
	002516L	11010111	10110000					
493.	002517L	00110001	00110110		LDPP	I350, MDR		GET THE DATA FIRST, THEN
	002520L	00110111	10001101					
494.	002521L	11000110	11111010		BRA	FETCH, F@, MP		NO FAULT AFTER READ, THEN DONE
495.	002522L	11001111	01101111		BRA	MEMPF2		ELSE, GO TO FAULT ROUTINE

*BFLR*  
*\* BAA X BFLROP*

496.				*		
497.	002523L			L7S:		
498.				. 1.30	( 37S) LMR	STORE A BYTE IN MEMORY
499.				.		(HL) <- S
500.				. 1.55	(062 37S) LMR	USE REG PAIR BC
501.				. 1.55	(174 37S) LMR	USE REG PAIR DE
502.				. 1.55	(022 37S) LMR	USE REG PAIR XA
503.				.		(RP) <- S
504.						
505.	002523L	11011000	10100110		BRA L7SI,F@,IZ	ALMOST EXACTLY LIKE LD7
506.	002524L	00110001	11000110		DLDX HL2MR	
	002525L	00110001	11100101			
507.	002526L	00110001	11011110		LDPP MDW,I02I	
	002527L	00110111	00101001			
508.	002530L	11001111	11111100		BRA FETCHW	
509.	002531L	00110001	11001111	L7SI	DLDX IM2MR,DIMP	
	002532L	00110111	00001001			
	002533L	00110001	11101111			
510.	002534L	00110001	11011110		LDPP MDW,I02I	WRITE REGISTER IN MEMORY
	002535L	00110111	00101001			
511.	002536L	11001111	11111100		BRA FETCHW	
512.				*		
513.	002537L			LDS:		
514.				. 0.50	( 3DS) LRR	LOAD SOURCE REGISTER INTO ANOTHER REG
515.				.		D <- S
516.						
517.	002537L	00110001	11011110		LDPP I350,I02I	SAVE SOURCE REGISTER IN DESTINATION
	002540L	00110111	10001101			
518.	002541L	11001111	11110111		BRA FETCHN	AND DONE!

*LDSOP2: BAA DOP2, F@, IZ  
LDPP I350, I02I  
BAA FETCHN*

*DOP2: LDRT TEFPIZ  
BAA DBCP, F@, IZ  
BAA DBCP*

*LDS DOP:  
BAA DOP, F@, IZ*

*LDS: LDPP I350, I02I  
BAA FETCHN*

*DOP LDRT TEFPIZ  
BAA DBCP, F@, IZ  
BAA DBCP*

521.									
522.	002542L								
523.									
524.									
525.									
526.									
527.									
528.									
529.									
530.									
531.									
532.									
533.									
534.									
535.									
536.									
537.									
538.									
539.									
540.									
541.									
542.									
543.	002542L	00110111	01000111		STB	SMR			GET FOLLOWING IMMEDIATE DATA
544.	002543L	01101111	11110010		LDRT	TEMP2			SAVE ALU OP-CODE
545.	002544L	11010100	10011011		MWAIT	,MEMPF2			
	002545L	11000111	01101111						
546.	002546L	00110001	00110110		LDTP	MDR			THE DATA IS IN T
547.	002547L	00110111	00001100		STB	IMAR			
548.	002550L	11011111	10001000		BRA	ALUOP			
549.									
550.	002551L								
551.									
552.									
553.									
554.									
555.	002551L	01101111	11110010		LDRT	TEMP2			SAVE ALU OP-CODE
556.	002552L	00110001	11100101		DLRX	HL2MR,,SMR			GET THE DATA
	002553L	00110001	11000110						
	002554L	00110111	01000111						
557.	002555L	11001110	11111111		MWAIT	NOOP, MEMPF2			
	002556L	11010100	10010001						
	002557L	11000111	01101111						
558.	002560L	00110001	11001001		DLDX	PC2MR,,IMAR			SO ALUOP CAN USE FETCHN RETURN
	002561L	00110001	11101000						
	002562L	00110111	00001100						
559.	002563L	00110001	00110110		LDTP	MDR			THE DATA
560.	002564L	11011111	10001000		BRA	ALUOP			AND GO WORK WITH IT

\*

AP4:

. 2.75 ( OP4). OP.VVV  
. (IMP OP4) OP.VVV  
. +.45 IF 'AC' OR 'SB'  
. ( 004) AD.VVV  
. (IMP 004) AD.VVV  
. ( 014) AC.VVV  
. (IMP 014) AC.VVV  
. ( 024) SU.VVV  
. (IMP 024) SU.VVV  
. ( 034) SB.VVV  
. (IMP 034) SB.VVV  
. ( 044) ND.VVV  
. (IMP 044) ND.VVV  
. ( 054) XR.VVV  
. (IMP 054) XR.VVV  
. ( 064) OR.VVV  
. (IMP 064) OR.VVV  
. ( 074) CP.VVV  
. (IMP 074) CP.VVV

ALUOP ON IMMEDIATE VALUE  
ALUOP IS OTHER THAN TO A-REG.  
R <- R OP N  
ADD IMMEDIATE VALUE TO A-REG  
ADD IMMEDIATE VALUE TO IMP-REG  
ADD WITH CARRY IMM. TO A-REG  
ADD WITH CARRY IMM. TO IMP-REG  
SUB IMMEDIATE VALUE FROM A-REG  
SUB IMMEDIATE VALUE FROM IMP-REG  
SUB WITH CARRY IMM. FROM A-REG  
SUB WITH CARRY IMM. FROM IMP-REG  
AND IMMEDIATE VALUE TO A-REG  
AND IMMEDIATE VALUE TO IMP-REG  
XOR IMMEDIATE VALUE TO A-REG  
XOR IMMEDIATE VALUE TO IMP-REG  
IOR IMMEDIATE VALUE TO A-REG  
IOR IMMEDIATE VALUE TO IMP-REG  
SUB IMM. VALUE FROM A-REG TO SET FLAGS  
SUB IMM. VALUE FROM IMP-REG TO SET FLAG

\*

AP7:

. 3.45 ( 2P7). OPM  
. (IMP 2P7) OPM  
. +.45 IF 'AC' OR 'SB'

ALUOP WITH MEMORY DATA  
DEST. OTHER THAN A-REG  
R <- R OP (HL)

*POPRUN NOOP*

*POPR*

*STB*

*SMR*

*POPRI*

*LDRT*

*TEMP2*

*MWAIT*

*,MEMPF*

*LDX*

*XX2MRH+URX*

*LDTP*

*PAROL, POR, SMR*

*BRA*

*POPRUN*

561.  
 562. 002565L  
 563.  
 564.  
 565.  
 566.  
 567. 002565L 01101111 11110010  
 568. 002566L 00110001 11011110  
 569.  
 570.  
 571. 002567L  
 572.  
 573.  
 574.  
 575. 002567L 01101111 11110001  
 576. 002570L 01110001 11110010  
 577. 002571L 00010111 10010010  
 578. 002572L 01010101 00011100  
 579. 002573L 01010010 01100101  
 002574L 01101111 10110000  
 580. 002575L 11101111 00000000  
 581.  
 582.  
 583.  
 584.  
 585.  
 586. 002576L 00110001 11011111  
 002577L 01110100 00110001  
 002600L 00110111 00000110  
 587. 002601L 11001111 11110111  
 588.  
 589.  
 590.  
 591. 002602L 00110001 11011111  
 002603L 01110011 10110001  
 002604L 00110111 01101111  
 592. 002605L 11001111 11110111  
 593.  
 594.  
 595.  
 596. 002606L 00110001 11011111  
 002607L 01110000 10110001  
 002610L 00110111 01101111  
 597. 002611L 11001111 11110111  
 598.  
 599.  
 600.  
 601. 002612L 00110001 11011111  
 002613L 01110101 10110001  
 002614L 00110111 01101111  
 602. 002615L 11001111 11110111  
 603.

+  
 APS:  
 . 1.65 ( 2PS) OPR ALUOP WITH SOURCE REGISTER  
 . (IMP 2PS) OPR DEST. OTHER THAN A-REG  
 . +.45 IF 'AC' OR 'SB' R ← R OP S  
  
 LDRT TEMP2 SAVE ALU OP-CODE  
 LDTP I02I SELECT SOURCE REG.  
 . BRA ALUOP  
  
 ALUOP  
 . 1.40  
 . +.45 IF 'AC' OR 'SB'  
  
 LDRT TEMPI SAVE SOURCE REG.  
 LDTR TEMP2 GET OPCODE  
 SHIFT SR,CC GET ALUOP IN BITS 4-2  
 DOTI ,ND,034 SELECT 3 BITS  
 DORA LINK,AC,ALUXQT,,CC OFFSET TO THE EXEC TABLE  
  
 BRR LINK GO TO CORRECT ROUTINE  
  
 \*  
 . THE TABLE STARTS HERE AND IS BACKWARDS  
  
 . ( A7S) CP 2'S COMPLEMENT SUBTRACT TO SET FLAGS  
  
 . DOPRP LUF,SB,TEMPI,IMPI,CO  
  
 . BRA FETCHN  
  
 . ( A6S) OR LOGICAL INCLUSIVE OR  
  
 . DOPRP IMPFO,OR,TEMPI,IMPI,CC  
  
 . BRA FETCHN  
  
 . ( A5S) XR LOGICAL EXCLUSIVE OR  
  
 . DOPRP IMPFO,XR,TEMPI,IMPI,CC  
  
 . BRA FETCHN  
  
 . ( A4S) ND LOGICAL AND  
  
 . DOPRP IMPFO,ND,TEMPI,IMPI,CC  
  
 . BRA FETCHN

604.			. ( A3S) SB	2'S COMPLEMENT SUBTRACT WITH CARRY
605.				
606.	002616L	00110001	00110101	LDRP TEMP2,UCFLG
	002617L	01101111	11110010	
607.	002620L	01110010	00110010	DOTR ,AC,TEMP2,,CO SET THE CARRY
608.	002621L	11001110	11111111	NOOP
609.				
610.			. ( A2S) SU	2'S COMPLEMENT SUBTRACT
611.				
612.	002622L	00110001	11011111	DOPRP IMPFO,SB,TEMP1,IMPI
	002623L	01110100	11110001	
	002624L	00110111	01101111	
613.	002625L	11001111	11110111	BRA FETCHN
614.				
615.			. ( A1S) AC	2'S COMPLEMENT ADD WITH CARRY
616.				
617.	002626L	00110001	00110101	LDRP TEMP2,UCFLG
	002627L	01101111	11110010	
618.	002630L	01110010	00110010	DOTR ,AC,TEMP2,,CO SET THE CARRY
619.	002631L	11001110	11111111	NOOP
620.				
621.			. ( A0S) AD	2'S COMPLEMENT ADD
622.				
623.	002632L	00110001	11011111	ALUXQT DOPRP IMPFO,AC,TEMP1,IMPI
	002633L	01110010	11110001	
	002634L	00110111	01101111	
624.	002635L	11001111	11110111	BRA FETCHN

```

627.
628. 002636L
629.
630. 002636L 00110001 11011100
    002637L 01010011 00100000
    002640L 00110111 10001100
631. 002641L 11010100 01011110
    002642L 11000111 01101111
632.
633. 002643L
634.
635.
636.
637.
638. 002643L 00110001 00110000
639. 002644L 11010011 01010100
640.
641. 002645L
642.
643.
644.
645.
646.
647.
648.
649.
650.
651.
652.
653. 002645L 01000101 00010000
654. 002646L 11010010 01001010
655. 002647L 01000101 00100000
656. 002650L 11010010 01001000
657. 002651L 01000101 01000000
658. 002652L 11010010 00101110
659.
660. 002653L
661.
662. 002653L 11010100 01010100
    002654L 11000111 01101111
663. 002655L 00110001 11011100
    002656L 00110111 00000100
664. 002657L 01000101 00100000
665. 002660L 11000010 11101011
666.
667.
668. 002661L 00110001 11101000
    002662L 00110001 11001001
    002663L 00110111 01000111
669. 002664L 11001111 11110000
    
```

```

*
SRVRPT: REPEATED SERVICE REQUESTS
        DOPIP   PSWO,OR,SWRPT,PSWI SET REPEAT FLAG
        MWAIT   ,MEMPF2

SRVNXT:
. FOLLOWING TIMING ASSUMED OR CORRECTED TILL THIS POINT REACHED
. (NOT INCLUDING OFF-PAGE ROUTINES)
        TSTTP   FI,SRVREQ   RELOAD SERVICE REQUEST FLAGS
        BRA     SRVRTW,TZ   (SPEEDUP, REALLY NO MORE INTERRUPTS)

*
SRVDO: SERVICE LOOP - PRIORITY SEQUENCE
. *****
. NOTICE:: ALL SERVICE ROUTINES THAT USE THE MAR MUST FIRST HAVE A
.           MWAIT ,$,+1 SO THAT THE MEMORY BUS IS NOT OVERRUN.
.           ALSO, THE MODE-WORD SWUSER MODE BIT MAY NEED TO BE TURNED OFF
.           TO ALLOW ACCESS TO PROTECTED MEMORY
. *****
. NOTE: P.C. POINTS TO START OF INSTRUCTION BEING EXECUTED (REPEATED)
.       OR TO INST. THAT WAS TO BE EXECUTED (FETCH)
.       NOT INCLUDING THE IMP-SPEC.
. *****

        TSTIT   ,SCDSPNL   0.50
        BRA     DLDO,FZ     DISPLAY-KEYBOARD SERVICE
        TSTIT   ,SCONMS    1.80 (SCDON); 1.90 (SCLST)
        BRA     OMDO,FZ     ONE MILLI-SECOND INT
        TSTIT   ,SCHUMS    1.15 (DO NOTHING)
        BRA     HUMDO,FZ    HUNDRED MICRO-SEC INT

*
SRVRTW:
.
        MWAIT   ,MEMPF2    2.85 (RE-FETCH); 1.25 (RPT'D)
                           FOR TRAILING MDW'S
        LDPP    MODW,PSWI   RESTORE CORRECT MODE (IF CHANGED)
        TSTIT   ,SWRPT     REPEATED INSTRUCTION?
        BRA     SRVID,FZ   YES, DO IT ONLY
                           WARNING! SOME REPEATED CODE IN FUTURE
                           MAY NEED MAR TO MATCH THE PC
                           NO, CODE AS AT FETCH WITHOUT SERVICE
        DLRX    PC2MR,,SMR
        BRA     SRVEND     GO TO FETCH-EXECUTE
    
```



```

670.
671. >002665L 01011001 11111111
      >002666L 11001111 11111111
672.
673. 002667L
674.
675.
676.
677. 002667L 00110111 00001010
678. 002670L 01010001 00100100
      002671L 01101111 11110010
      002672L 01010001 11101111
      002673L 01101111 11110001
679.
680. 002674L 11010100 01000011
      002675L 11000111 01101111
681. >002676L 01011001 11111111
682. 002677L 00110001 11011100
      002700L 01000101 00100000
683. >002701L 11000011 11111111
684. >002702L 11001111 11111111
685.
686.
687.
688.
689.
690.
691.

```

```

*
DLDO      BRAX      DL$DO      DISPLAY - KEYBOARD

*
OMDO      ONE MILLISECOND INTERRUPT CONTROL
. 1.30 (TO SCDON), 1.40 (TO SCLST)
. SHOULD BE LAST INTERRUPT IN CHAIN BECAUSE DOESN'T RETURN AS OTHERS DO
. THROUGH SRVRET (GOES OFF ON ITS OWN)
      STB      COMF      CLEAR FLAG
      DLDRI    TEMP,SVONEMS  LOAD INTERRUPT VECTOR ADDRESS

      MWAIT    ,MEMPF2    ($+1 OR SRV. RTN. FAULT GENERATES MEMPF)
                          WAIT FOR UNUSED INST. FETCH TO COMPLETE

      BPGX     SCDON
      TSTIP    ,SWRPT,PSWI  WAS REPEATED INSTRUCTION?

      BRA      SCDON,TZ     NO, THE P.C. CORRECT (IMP - UNKNOWN)
      BRA      SCLST        YES, BACK UP P.C. TO IMP-SPEC.

. IF I-FETCH ENTRY PC POINTING TO NEXT INSTRUCTION TO EXECUTE SO CORRECT
.   IMP IS ZERO BY WAY FETCH CODE WRITTEN
. IF NON-I-FETCH (REPEATED) PC POINTING TO INSTRUCTION BEING REPEATED
.   IF IMP ZERO PC IS CORRECT, POINTING TO INST. TO CONTINUE
.   IF IMP NON-ZERO MUST BACK UP PC TO RE-DO IMP SPEC CODE WHEN MACRO-RETURNS
. COULD SIMPLIFY, IF IMP-NON-ZERO MUST BACKUP BECAUSE IS IMP-SPEC REPEATED

```

*OMDO IT*

```

OMDO
  STB      COMF
  LDTR     SMOD1NS
  BRA      OMDOIT,TZ
  DORI     SMOD1NS,SB,I
  BRA      SRVNEXT

```

MICRO-PROCESSOR EMULATION SUPPORT CODE - HJS - 79DEC12 16:20  
 . NOISE-MAKER INTERFACE. BEEPS, CLICKS & MAKES OTHER FUNNY NOISES

```

694.
695.
696.
697.
698.
699.
700.
701.
702.
703.
704.
705.
706.
707. 000203
708. 000253
709. 000310
710. 000316
711. 000360
712.
713. 000340
714. 000177
715.
716. 002703L
717.
718.
719.
720. 002703L 01010001 10000011
721. 002704L 01101111 11110001
722. 002705L 00110001 11011100
    002706L 01000101 00000100
723. 002707L 11010010 11100000
724. 002710L 00010001 11001101
725. 002711L 11000010 11110111
726. 002712L 01110001 11110001
    002713L 00000111 11111101
727. 002714L 11001111 11110111
728. 002715L
729.
730.
731.
732.
733.
734. 002715L 01010001 11110000
735. 002716L 11011010 00111011
736. 002717L 01010001 10101011
737. 002720L 11011111 00111011
    
```

```

*
. DEFINE THE CONTROL BITS FOR THE AUDIO CHANNEL
. TOGGLE B7      0  HIGH OUTPUT (IF NOT DELAYING)
.               1  LOW OUTPUT (ALWAYS)
. FCN   B6,5    00  BEEP WITH LONG DELAY (NORMAL)
.               01  BEEP WITH SHORT DELAY
.               10  DELAYING
.               11  CLICKING
. DONE   B4      0  CONTINUE DOING OPERATION
.               1  STOP, THE END (IF B7 IS 1)
. COUNTER B3,2,1,0 COUNT AT A 60/50HZ RATE (BY DL$DO)

. NOW, DEFINE THE CONTROL COMMANDS (INITIAL/FINAL VALUES)
BPINIT EQU B7+B4-13  STANDARD BEEP ENDS WITH B7+B4
BPSHRT EQU B7+B5+B4-5  SHORT LENGTH ENDS WITH B7+B5+B4
DLYLNG EQU B7+B6+B4-8  STANDARD DELAY ENDS WITH B7+B6+B4
DLYSRT EQU B7+B6+B4-2  SHORT DELAY ENDS WITH B7+B6+B4
CLKINI EQU B7+B6+B5+B4-0  NORMAL CLICK ENDS WITH B7+B6+B5+B4

CLKLVL EQU 0340  LEVEL THE CLICK USES ON THE D/A
BYPLVL EQU 0177  LEVEL THE BEEP USES ON THE D/A

*
BEEP:
. ( 151) EX BEEP  START AUDIBLE CHANNEL IF QUIET
. (IMP 151) EX BEEP  START AUDIBLE CHANNEL IF QUIET
. 1.15 (DO IT), 0.85 (PREVIOUS IN PROGRESS)
    LDTI  BPINIT  SETUP FOR BEEP OPERATION
CLICKS  LDRT  TEMP1  SAVE AWAY THE CONTROL BYTE
        TSTIP  ,SWUSER,PSWI  IS IT LEGAL TO DO THE INSTRUCTION?

        BRA  IVIOL2,FZ  NO, ERROR IT OUT
        TSTRT  FI,ACD  ANY SOUNDS IN PROGRESS
        BRA  FETCHN,FZ  YES, SO DO NOTHING
        LDRR  ACD,TEMP1  NO, SO INIT TO DO THE NEW SOUND

        BRA  FETCHN

CLICK:
. ( 153) EX CLICK  START AUDIBLE CHANNEL IF QUIET
. (IEV 153) EX CLICK  START AUDIBLE CHANNEL IF QUIET
. 1.35 (DO IT), 1.05 (PREVIOUS IN PROGRESS)
. (IOD 151) CLICKR  SPECIAL NOISE IF QUIET
. 1.55 (DO IT), 1.25 (PREVIOUS IN PROGRESS)
    LDTI  CLKINI  ASSUME NORMAL CLICK
        BRA  CLICKS,F@,IO  IT WAS!
    LDTI  BPSHRT  NO, WAS SPECIAL SHORT BEEP
        BRA  CLICKS
    
```

```

738.
739. 002721L
740. 002721L 00110111 00001011
741. 002722L 00010001 10111101
742. 002723L 11010011 01011100
743.
744.
745. 002724L
746.
747.
748.
749.
750.
751.
752.
753.
754.
755.
756. 002724L 01010010 10000000
757. 002725L 11010001 00011010
758. 002726L 01000101 00010000
759. 002727L 11010011 00011110
760. 002730L 01000101 01000000
761. 002731L 11010010 00011111
762. 002732L 01000101 00100000
763. 002733L 11010010 00100001
764. 002734L 01010001 11001000
765. 002735L 11011111 00011110
766. 002736L 01010001 11001110
767. 002737L 11011111 00011110
768.
769. 002740L 01010001 00000000
770. 002741L 00000111 11111101
771. 002742L 01010001 00000000
    002743L 00110111 00101010
772. 002744L 11011111 01011100
773.
774. 002745L 01000101 01000000
775. 002746L 11010011 00010010
776. 002747L 01000101 00100000
777. 002750L 11010011 00011110
778. 002751L 00000111 11111101
779. 002752L 01010001 11100000
    002753L 00110111 00101010
780. 002754L 11011111 01011100
781.
782. 002755L 00000111 11111101
783. 002756L 01010001 01111111
    002757L 00110111 00101010
784. 002760L 11011111 01011100
    
```

```

*
HUMDO          HUNDRED-MICRO-SECOND INTERRUPT (AUDIO)
                STB          CHUF          CLEAR INTERRUPT
                LDTR         ACD,CC       IF ZERO
                BRA          SRVNXT,TZ    THE CHANNEL IS OFF (1.15)
                BRAX         AC$DO       ELSE ON, SO DO IT
.
*
AC$DO:
. 1.05~1.75
. THE SPECIAL AUDIO CHANNEL CONTROL IS DONE HERE
. OPERATION IS TO ALTERNATE THE TOGGLE (B7).
. IF IT BECOMES SET (FC) OUTPUT LOW VALUE. IF IT BECOMES CLEAR (TC)
. THEN OUTPUT HIGH VALUE IF BEEPING OR CLICKING, DELAY IS A LOW VALUE.
. TEST FOR COMPLETION (FC & B4 SET) AND WHEN DONE THE TIMING, SEE IF MORE
. TO DO (THE DELAY). IF DELAY ALREADY DONE, THEN END. ELSE, LOAD UP THE
. DELAY CONTROL BYTE TO DO IT.
. NOTE: LOW ORDER BIT COUNTING IS DONE BY DL$DO ON EVERY BOTLINE (50 / 60 HZ)

                DOTI         ,AC,B7      TOGGLE THE TOGGLE BIT
                BRA          ACSIG,TC    WAS 1 (TO 0), DO RISING EDGE BEEP & CLICK
                TSTIT        ,B4        DO FALLING EDGE (OR LOW LEVEL)
                BRA          ACLOUT,TZ   WAS 0 (TO 1), NOT DONE, LOW OUTPUT
                TSTIT        ,B6        FINISHED BEEPING?
                BRA          ACEND,FZ    NO, FINISHED CLICK OR DELAY FOR GOOD
                TSTIT        ,B5
                BRA          ACSHRT,FZ
                LDTI         DLYLNG     FINISHED LONG BEEP, DO LONG DELAY
                BRA          ACLOUT
                ACSHRT       LDTI         FINISHED SHORT BEEP, DO SHORT DELAY
                BRA          ACLOUT

                ACEND        TCLR        FINISHED ALL OPERATIONS (ALLOW NEXT)
                ACLOUT       LDRT        ACD          SAVE THE NEW CONTROL BYTE
                LDPI         LSPKR,0    OUTPUT LOW TO THE SPEAKER

                BRA          SRVNXT

                ACSIG        TSTIT        ,B6        ARE WE BEEPING?
                BRA          ACHOUT,TZ   YES, PUT OUT ITS LEVEL
                TSTIT        ,B5        ARE WE CLICKING?
                BRA          ACLOUT,TZ   NO, DELAY OUTPUTS LOW LEVEL
                LDRT         ACD          SAVE THE NEW CONTROL BYTE
                LDPI         LSPKR,CLKLVL OUTPUT CLICK LEVEL

                BRA          SRVNXT

                ACHOUT       LDRT        ACD          SAVE THE NEW CONTROL BYTE
                LDPI         LSPKR,BYPLVL OUTPUT BEEP LEVEL

                BRA          SRVNXT
    
```

785.

786. 002761L 11111111 11111111  
002762L 11111111 11111111  
002763L 11111111 11111111  
002764L 11111111 11111111  
002765L 11111111 11111111  
002766L 11111111 11111111  
002767L 11111111 11111111  
002770L 11111111 11111111  
002771L 11111111 11111111  
002772L 11111111 11111111  
002773L 11111111 11111111  
002774L 11111111 11111111  
002775L 11111111 11111111  
002776L 11111111 11111111  
002777L 11111111 11111111

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TABPAGE PRODL

789.  
 790. 003000L  
 791.  
 792.  
 793.  
 794.  
 795.  
 796.  
 797.  
 798.  
 799.  
 800.  
 801.  
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 803.  
 804.  
 805.  
 806.  
 807.  
 808.  
 809.  
 810.  
 811. 003000L 11001001 11010100  
 812. 003001L 11001010 11100110  
 813.  
 814. 003002L 00110001 11100101  
 003003L 00110001 11000110  
 003004L 00110111 01000111  
 815. 003005L 00110001 11010000  
 003006L 01101111 11110001  
 816. 003007L 11000100 11111000  
 003010L 11010111 00010100  
 817. 003011L 00110111 00001101  
 818. 003012L 00110001 10000110  
 003013L 00110001 10100101  
 819. 003014L 00110001 11100011  
 003015L 00110001 11000100  
 820. 003016L 00110001 00110110  
 003017L 01110010 00110001  
 003020L 00110111 00101001  
 821. 003021L 01101111 10110001  
 822. 003022L 00110001 10010000  
 003023L 01010100 00000001  
 003024L 00110111 10000100  
 003025L 00110001 10110000  
 003026L 01010100 00000000  
 003027L 00110111 10000011  
 823. 003030L 11001111 10111111

\*  
 BT: ( 021) BT BLOCK TRANSFER  
 . -0.30 + N \* 5.30 - N \* 0.15 / ODDSTEP + 0.10 WHEN TCFZ / STEP - 0.50 IF MATCH  
 . (DE) ← T ← A + (HL)  
 . DE ← DE + 1; HL ← HL + 1  
 . STOP IF T = -B; C ← C - 1; UNTIL = 0  
 . (111 021) BTR BLOCK TRANSFER REVERSE  
 . -0.30 + N \* 5.60 - N \* 0.15 / ODDSTEP + 0.10 WHEN TCFZ / STEP - 0.50 IF MATCH  
 . (DE) ← T ← A + (HL)  
 . DE ← DE - 1; HL ← HL - 1  
 . STOP IF T = -B; C ← C - 1; UNTIL = 0  
 . (062 021) BCV BLOCK CONVERT  
 . -0.30 + N \* 6.85 - N \* 0.15 / ODDSTEP + 0.10 WHEN TCFZ / STEP - 0.50 IF MATCH  
 . (DE) ← T ← A ← (HL + (DE))  
 . DE ← DE + 1  
 . STOP IF T = -B; C ← C - 1; UNTIL = 0  
 . NOTE: NONE OF THESE CHANGE THE CONDITION FLAGS  
 . BRA BTX,T@,IZ BT (021)  
 . BRA BTV,F@,IO BTR (062 021)  
 \*  
 BTR DLRX HL2MR,,SMR BTR (111 021)  
 . LDRP TEMP1,URI+URA LOAD UP THE A-REG OFFSET  
 . MWAIT ,MEMPF3  
 . STB DMAR  
 . DLDX MR2HL DECREMENT HL FOR BTR  
 . DLRX DE2MR  
 . DOPRP MDW,AC,TEMP1,MDR,CO GET RESULTANT DATA  
 . LDRT TEMP1,,CC STORE DATA IN (DE)  
 . DDECP URO+UDE,MARI BACKUP DE FOR BTR  
 . BRA BTEND

824.					
825.	003031L	00110001	11100011	* BTX	DLRX DE2MR,,SMR BCV (062 021)
	003032L	00110001	11000100		
	003033L	00110111	01000111		
826.	003034L	00010111	10110010		CCLR
827.	003035L	00110001	11010110		LDTP URI+URL ADD DATA AT DE TO TABLE POINTER IN HL
828.	003036L	11000100	11100001		MWAIT ,MEMPF3
	003037L	11010111	00010100		
829.	003040L	00110010	00110110		DOPP MAROL,AC,MDR A ← MAR ← L + (DE)
	003041L	00110111	11000000		
830.	003042L	00110111	10000000		LDPT URO+URA STORE IN A SO CAN FIND STOP POINT
831.	003043L	00110001	11010101		LDTP URI+URH ADD IN CARRY ALSO
832.	003044L	00110110	11100000		DOP MAROH,IT
833.	003045L	01010001	00000000		TCLR NO A-REG OFFSETS
834.	003046L	00110111	01000111		STB SMR INDIRECT THROUGH THIS FOR TABLE ENTRY
835.	003047L	01101111	11110001		LDRT TEMP1
836.	003050L	11000100	11010111		MWAIT ,MEMPF3
	003051L	11010111	00010100		
837.	003052L	11001111	11001010		BRA BTCVT
838.				* BTX	DLRX HL2MR,,SMR GET DATA AT HL TO BE MOVED
839.	003053L	00110001	11100101		
	003054L	00110001	11000110		
	003055L	00110111	01000111		
840.	003056L	00110001	11010000		LDRP TEMP1,URI+URA SAVE THE A-REG OFFSET (ZERO FOR BCV)
	003057L	01101111	11110001		
841.	003060L	11000100	11001111		MWAIT ,MEMPF3
	003061L	11010111	00010100		
842.	003062L	00110111	00001100		STB IMAR
843.	003063L	00110001	10000110		DLDX MR2HL INCREMENT FOR FOR BT
	003064L	00110001	10100101		
844.	003065L	00110001	11000100	BTCVT	DLDX DE2MR POINT TO WHERE TO STORE RESULT
	003066L	00110001	11100011		
845.	003067L	00110001	00110110		DQPRP MDW,AC,TEMP1,MDR,CO STORE DATA IN (DE) AND IN TEMP1
	003070L	01110010	00110001		
	003071L	00110111	00101001		
846.	003072L	01101111	11110001		LDRT TEMP1
847.	003073L	00110001	10010000		DADDP URO+UDE,MARI INCREMENT DE FOR BT & BCV
	003074L	00010110	01110010		
	003075L	00110111	10000100		
	003076L	00110001	10110000		
	003077L	00110110	10000011		

848.  
849.  
850.  
851. 003100L 00110001 11010001  
003101L 01110010 00000001  
852. 003102L 11000000 10111010  
853. 003103L 11000011 01110111  
854.  
855.  
856. 003104L 00010111 10110010

\*  
. BT - 3.25, BTR - 3.55, BCV - 4.80 (TO HERE)  
BTEND TSTRP AC,TEMP1,URI+URB,CO AT THE ENDPOINT?  
BRA RIN256,FC NO, WANT CARRY TRUE & ZERO TRUE  
BRA RIND,TZ YES, END NOW!  
BRA RIN256 NO!  
. NO, REPEAT 256 TIMES (OR LESS)  
. ONLY CARRY SET RIN256 CASE  
CCLR

```

859.
860. 003105L
861.
862.
863.
864.
865.
866.
867. 003105L 00110001 11010010
      003106L 01010100 00000001
      003107L 00110111 10000010
868. 003110L 11000011 01110111
869. 003111L 01000101 00000001
870. 003112L 11000010 10110010
871.
872.
873. 003113L
874.
875.
876.
877.
878.
879. 003113L 00110001 00110000
880. 003114L 11000010 10101110
881. 003115L 11000100 10110010
      003116L 11010111 00010100
882. 003117L 00111001 00110100
      003120L 10101111 00110011
883.
884. 003121L 01011001 11111010
      003122L 11011111 01100001
    
```

```

*
RIN256:
. ODD = 1.45, RPT = 1.60, SRV = 1.35, END = 1.30
.
.   WARNING, CARRY MUST BE CLEAR ON ENTRY
.   BLOCK REPEATED INSTRUCTIONS (THOSE THAT COUNT C THROUGH 256 MAX STEPS
.   DO NOT CHANGE FLAGS)
.
.   DOPIP   URO+URC,SB,1,URI+URC IF ZERO, FINISHED
.
.   BRA     RIND,TZ
.   TSTIT   ,1
.   BRA     RINDO,FZ
.
.   DO THEM IN PAIRS SO CAN'T INTERRUPT
.   DURING DOUBLE BYTE MOVE
.   !CAN USE BT IN DISPLAY POINTER MOVES!
*
RINST:
. SRV = 0.65, RPT = 0.90
.
.   LOOP THROUGH REPEATED INSTRUCTIONS, SET THE REPEAT MODE AND DO
.   SERVICE REQUEST IF NEEDED ELSE RE-EXECUTE THE INSTRUCTION.
.
.   TSTPT   FI,SRVREQ   DO SERVICE IF NEEDED
.   BRA     RINRPT,FZ
RINDO     MWAIT        ,MEMPF3
.
.   BRPX    IDCOD       GO DO OPCODE AGAIN
.
RINRPT    BRAX         SRVRPT
    
```



```

887.
888. 003123L
889.
890.
891.
892.
893.
894.
895.
896.
897.
898.
899.
900.
901.
902.
903.
904. 003123L 11001000 10010000
905. 003124L 00110001 11100011
    003125L 00110001 11000100
    003126L 00110111 01000111
906. 003127L 00110001 10010000
    003130L 00010110 01110010
    003131L 00110111 10000100
    003132L 00110001 10110000
    003133L 00110110 10000011
907. 003134L 11000100 10100011
    003135L 11010111 00010100
908. 003136L 00110001 00110110
    003137L 01101111 11110001
909. 003140L 00110001 11100101
    003141L 00110001 11000110
    003142L 00110111 01000111
910. 003143L 00110001 10010000
    003144L 00010110 01110010
    003145L 00110111 10000110
    003146L 00110001 10110000
    003147L 00110110 10000101
911. 003150L 01110001 10110001
912. 003151L 11000100 10010110
    003152L 11010111 00010100
913. 003153L 00110100 00110110
    003154L 00110111 00000110
914. 003155L 11000011 10111010
915. 003156L 11001111 01110111
    
```

```

*
BCP:
. ( 041) BCP BLOCK COMPARE
. -0.30 + N * 5.25 - 0.15 * N / ODDSTEP - 0.5 IF MATCH
. (HL) - (DE); HL <- HL + 1; DE <- DE + 1
. STOP IF TZ; C <- C - 1; CONTINUE UNTIL = 0
.
. (111 041) DFAC DECIMAL FIELD ADD
. -0.30 + C * 7.45 (DE) <- B .OR. (DE) .DAD. (HL) + CRY
. DE <- DE - 1; HL <- HL - 1
. C <- C - 1; UNTIL = 0 (16)
.
. (062 041) DFSB DECIMAL FIELD SUBTRACT
. -0.30 + C * 7.65 (DE) <- B .OR. (DE) .DSB. (HL) - CRY
. DE <- DE - 1; HL <- HL - 1
. C <- C - 1; UNTIL = 0 (16)
.
BRA DFOP,F@,IZ GO TO DECIMAL STUFF
DLRX DE2MR,,SMR
.
DADDP URO+UDE,MARI GET DATA AND UPDATE DE
.
MWAIT ,MEMPF3
LDRP TEMP1,MDR
DLRX HL2MR,,SMR GET DATA AND UPDATE HL
.
DADDP URO+UR,MARI
.
LDTR TEMP1,CC GET DE DATA
MWAIT ,MEMPF3
DOPP LUF,SB,MDR SUBTRACT HL DATA AND SET COMPARE FLAGS
BRA RIN256,TZ CONTINUE IF A MATCH (CARRY ZERO TOO!)
BRA RIND END IF DATA DIFFERS
    
```

```

918.
919. 003157L
920.          (111 041) DFAC          DECIMAL FIELD ADD
921.          -0.30 + C * 7.25        (DE) <- B .OR. (DE) .DAD. (HL) + CRY
922.          .                        DE <- DE - 1; HL <- HL - 1
923.          .                        C <- C - 1; UNTIL = 0 (16)
924.
925.          (062 041) DFSB          DECIMAL FIELD SUBTRACT
926.          -0.30 + C * 7.25 (+ 0.20 PER BORROW) (DE) <- B .OR. (DE) .DSB. (HL) - CRY
927.          .                        DE <- DE - 1; HL <- HL - 1
928.          .                        C <- C - 1; UNTIL = 0 (16)
929.
930. 003157L 01010001 00001111      LDRI      TEMP2,017      SELECT 4 BITS, NOT ALL OF THEM
    003160L 01101111 11110010
931. 003161L 01010001 10000101      BAL      ,DFADD      (ASSUME THIS)
932. 003162L 11001011 01101011      BRA      BFOP,T@,IO  WAS ODD THEREFORE WAS DECIMAL ADD
933. 003163L 01010001 10001010      BAL      ,DFSUB
934. 003164L 11001111 01101011      BRA      BFOP      WAS EVEN SO IT WAS DECIMAL SUBTRACT
935.
936. 003165L          DFSUB
937. 003165L 01110100 11110001      DOPR      LUF,SB,TEMP1  SET FLAGS ON SUBTRACT
    003166L 00110111 00000110
938. 003167L 11000000 01111111      BRA      DFAEND,FC   NO CARRY, NO PROBLEMS
939. 003170L 01010010 00001001      DOTI     ,AC,10-1    CARRY, CORRECT THE VALUE (ADDS 10!)
940. 003171L 11001111 01111111      BRA      DFAEND
941.
942. 003172L          DFADD
943. 003172L 01110010 11110001      DORR      TEMP1,AC,TEMP1  ADD TOGETHER (CARRY FALSE ON RESULT)
    003173L 01101111 11110001
944. 003174L 01010010 11110110      DOPI     LUF,AC,-10    SET FLAGS & CORRECT IF OVERFLOW
    003175L 00110111 00000110
945. 003176L 11000001 01111111      BRA      DFAEND,TC   IF OVERFLOWED, CORRECTED NOW
946. 003177L 01110001 11110001      LDTR     TEMP1      NO CARRY, GET CORRECT VALUE
947. 003200L 00110011 11010001      DFAEND   DOPP      MDW,OR,URI+URB  SET THE ZONE BITS
    003201L 00110111 00101001
948.          .          BRA      RIN16
    
```

951.  
 952. 003202L  
 953.  
 954.  
 955.  
 956.  
 957. 003202L 00010111 10110010  
 958. 003203L 00110001 11010010  
 003204L 01010100 00000001  
 003205L 00110111 10000010  
 959. 003206L 01000101 00001111  
 960. 003207L 11000010 10110100  
 961.  
 962. 003210L  
 963.  
 964.  
 965. 003210L 00110001 11011100  
 003211L 01010101 11011111  
 003212L 00110111 10001100  
 966. 003213L 01011001 11111011  
 003214L 11001111 11111100

\*  
 RIN16:  
 . RPT - 1.70, SRV - 1.45, END - 1.40  
  
 . FIELD REPEATED INSTRUCTIONS ARE THOSE THAT COUNT C THROUGH 16 MAX STEP  
  
 CCLR  
 .DOPIP URO+URC,SB,1,URI+URC COUNT DOWN  
  
 TSTIT ,017 AT THE END (BASE 16)?  
 BRA R.INST,FZ NOT YET  
  
 \*  
 RIND:  
 . 0.70 REPEATED INSTRUCTION END  
  
 .DOPIP PSWO,ND,-1-SWRPT,PSWI  
  
 BRAX FETCHW

969.						
970.	003215L					
971.						
972.						
973.						
974.						
975.						
976.	003215L	01010001	11111111	LDRI	TEMP2,0377	SELECT ALL THE BITS
	003216L	01101111	11110010			
977.	003217L	01010001	01001000	BRC	BFOP,,BFSUB	
	003220L	11001111	01101011			
978.						
979.	003221L					
980.						
981.						
982.						
983.						
984.						
985.	003221L	01010001	11111111	LDRI	TEMP2,0377	SELECT ALL THE BITS
	003222L	01101111	11110010			
986.	003223L	01010001	01001100	BAL	,BFADD	
987.						
988.	003224L					
989.						
990.						
991.	003224L	01101111	10110000	BAS	LINK,CC	
992.	003225L	00110001	11100101	DLRX	HL2MR,,SMR	
	003226L	00110001	11000110			
	003227L	00110111	01000111			
993.	003230L	00110001	10010000	DDECP	URO+UR,MARI	GET (HL) DATA AND UPDATE HL
	003231L	01010100	00000001			
	003232L	00110111	10000110			
	003233L	00110001	10110000			
	003234L	01010100	00000000			
	003235L	00110111	10000101			
994.	003236L	01110001	11110010	LDTR	TEMP2	
995.	003237L	11000100	01100000	MWAIT	,MEMPF3	
	003240L	11010111	00010100			
996.	003241L	00110101	00110110	DORP	TEMP1,ND,MDR,,CC	PUT IT IN TEMP1
	003242L	01101111	10110001			
997.	003243L	00110001	11100011	DLRX	DE2MR,,SMR	
	003244L	00110001	11000100			
	003245L	00110111	01000111			
998.	003246L	00110001	10010000	DDECP	URO+UDE,MARI	GET (DE) DATA AND UPDATE DE
	003247L	01010100	00000001			
	003250L	00110111	10000100			
	003251L	00110001	10110000			
	003252L	01010100	00000000			
	003253L	00110111	10000011			
999.						
1000.	003254L	00110001	00110101	DOTPP	,AC,UCFLG,UCFLG	CARRY IGNORED, BITS 2&6 NOT BOTH HIGH SET THE CARRY
	003255L	00110010	00110101			

1001.	003256L	01110001	11110010	LDTR	TEMP2	
1002.	003257L	11000100	01010000	MWAIT	,MEMPF3	
	003260L	11010111	00010100			
1003.	003261L	00110101	00110110	DOTP	,ND,MDR	
1004.	003262L	11101111	00000000	BRR	LINK	SELECT ADD & SUBTRACT, BINARY & DECIMAL
1005.						
1006.	003263L	01110010	11110001	* BFADD	DOPR	MDW,AC,TEMP1 (DE) ← (DE) + (HL)
	003264L	00110111	00101001			
1007.	003265L	00110111	00000110	LDPT	LUF	
1008.	003266L	11001111	01111101	BRA	RIN16	
1009.						
1010.	003267L	01110100	11110001	BFSUB	DOPR	MDW,SB,TEMP1 (DE) ← (DE) - (HL)
	003270L	00110111	00101001			
1011.	003271L	00110111	00000110	LDPT	LUF	
1012.	003272L	11001111	01111101	BRA	RIN16	

```

1015.
1016. 003273L
1017.
1018.
1019.
1020.
1021.
1022.
1023.
1024.
1025.
1026.
1027. 003273L 00110001 11100101
      003274L 00110001 11000110
      003275L 00110111 01000111
1028. 003276L 11001001 00101110
1029.
1030. 003277L 00110001 10010000
      003300L 00010110 01110010
      003301L 00110111 10000110
      003302L 00110001 10110000
      003303L 00110110 10000101
1031. 003304L 00110001 00110101
1032. 003305L 00010111 10100010
1033. 003306L 00010111 10110010
1034. 003307L 11000100 00111000
      003310L 11010111 00010100
1035. 003311L 00110001 00110110
1036. 003312L 00010111 10010010
1037. 003313L 00110111 00101001
1038. 003314L 00010111 10010010
1039. 003315L 01101111 11110001
1040. 003316L 01110010 00110001
      003317L 00110111 00000111
1041. 003320L 11001111 01111101
1042.
1043. 003321L 00010111 10110010
1044. 003322L 00110001 10010000
      003323L 01010100 00000001
      003324L 00110111 10000110
      003325L 00110001 10110000
      003326L 01010100 00000000
      003327L 00110111 10000101
1045. 003330L 00110001 00110101
      003331L 00110010 00110101
1046. 003332L 11000100 00100101
      003333L 11010111 00010100
1047. 003334L 00110001 00110110
      003335L 00110010 00110110
      003336L 00110111 00101001
1048. 003337L 00110111 00000111
1049. 003340L 11001111 01111101
    
```

```

*
BFS:
. ( 075) BFSL          BINARY FIELD SHIFT LEFT
. -0.30 + C * 4.55    (HL) <- (HL) + (HL) + CRY; HL <- HL - 1
.                      C <- C - 1; UNTIL = 0 (16)

. (111 075) BFSR      BINARY FIELD SHIFT RIGHT
. -0.30 + C * 4.55    (HL) <- SHFTRGHT (HL); HL <- HL + 1
.                      C <- C - 1; UNTIL = 0 (16)

. NOTE: ONLY CHANGES THE CARRY FLAG

      DLRX      HL2MR,,SMR      GET DATA TO SHIFT & SELECT R/L ROUTINE

      BRA      BFSL,T@,IZ

. BFSR
      DADDP     URO+UR,MARI      UPDATE HL

      LDTP      UCFLG
      SHIFT     SL              PUT THE CARRY IN THE LSB (BIT 0)
      CCLR      AND INTO THE LINK
      MWAIT     ,MEMPF3

      LDTP      MDR              GET THE DATA
      SHIFT     SR              DO EXTENDED SHIFT
      LDPT      MDW              OUTPUT SHIFTED DATA
      SHIFT     SR              PUT LINK IN THE MSB
      LDRT      TEMPI
      DOPR      LUCF,AC,TEMPI,,CO SET THE CARRY FROM THE MSB (LINK)

      BRA      RIN16

*
BFSL
      CCLR      UPDATE HL
      DDECP     URO+UR,MARI      CARRY IS STOPPED IN BIT 2 OR 6 OR UCFLG

      DOTPP     ,AC,UCFLG,UCFLG  SET CARRY FROM USER CARRY

      MWAIT     ,MEMPF3

      DOPPP     MDW,AC,MDR,MDR   SHIFT LEFT!

      LDPT      LUCF              SET CARRY ON RESULT
      BRA      RIN16
    
```

. SHIFT OPERATIONS

1052.					
1053.	003341L				
1054.					
1055.					
1056.					
1057.	003341L	00110001	11011111	LDRP	TEMP1,IMPI
	003342L	01101111	11110001		
1058.	003343L	01110010	00110001	DOPR	LUCF,AC,TEMP1,,CO ADD TOGETHER AND SET USER CARRY
	003344L	00110111	00000111		
1059.	003345L	00110110	10001111	DOP	IMPO,IT PUT CARRY IN THE LSB
1060.	003346L	01011001	11111011	BRAX	FETCHN DON'T USE IMPFO, WILL GET BAD CARRY
	003347L	11001111	11110111		
1061.					
1062.	003350L				
1063.					
1064.					
1065.					
1066.	003350L	00110001	11011111	LDTP	IMPI
1067.	003351L	00010111	10110010	CCLR	SET THE LINK BIT ON LSB
1068.	003352L	00010111	10010010	SHIFT	SR RIGHT CIRCULAR
1069.	003353L	00110111	10001111	LDPT	IMPO STORE RESULT
1070.	003354L	01101111	11110001	LDRT	TEMP1
1071.	003355L	01110010	00110001	DOPR	LUCF,AC,TEMP1,,CO SET CARRY ON THE MSBIT
	003356L	00110111	00000111		
1072.	003357L	01011001	11111011	BRAX	FETCHN
	003360L	11001111	11110111		
1073.					
1074.	003361L				
1075.					
1076.					
1077.					
1078.	003361L	00110001	00110101	LDTP	UCFLG GET CARRY
1079.	003362L	00010111	10100010	SHIFT	SL IN LSBIT
1080.	003363L	00010111	10110010	CCLR	AND INTO LINK
1081.	003364L	00110001	11011111	LDTP	IMPI
1082.	003365L	00010111	10010010	SHIFT	SR DO RIGHT EXTEND
1083.	003366L	00110111	10001111	LDPT	IMPO
1084.	003367L	00010111	10010010	SHIFT	SR PUT LINK IN MSBIT
1085.	003370L	01101111	11110001	LDRT	TEMP1
1086.	003371L	01110010	00110001	DOPR	LUCF,AC,TEMP1,,CO SET CARRY ON LINK
	003372L	00110111	00000111		
1087.	003373L	01011001	11111011	BRAX	FETCHN
	003374L	11001111	11110111		

\*

SLC:

. 0.95 ( 002) SLC SHIFT LEFT CIRCULAR  
 . 0.95 (IMP 002) SLCR RN <- R(N-1); CRY <- R0 <- R7

\*

SRC:

. 1.15 ( 012) SRC SHIFT RIGHT CIRCULAR  
 . 1.15 (IMP 012) SRCR CRY <- R7 <- R0; R(N-1) <- RN

\*

SRE:

. 1.50 ( 032) SRE SHIFT RIGHT EXTENDED  
 . 1.50 (IMP 032) SRER R7 <- CRY; R(N-1) <- RN; CRY <- R0

1088.  
 1089. 003375L 11111111 11111111  
 003376L 11111111 11111111  
 003377L 11111111 11111111  
 1090.  
 1091. 003400L  
 1092.  
 1093.  
 1094.  
 1095. 003400L 00110001 00110101  
 003401L 01010101 11000011  
 003402L 00110111 10001111  
 1096. 003403L 01011001 11111011  
 003404L 11001111 11110111

\*  
 TABPAGE PRODL  
 \*  
 CCS:  
 . 0.70 ( 042) CCS CONDITION CODE SAVE  
 . 0.70 (IMP 042) CCSr R ← (CRY).(SGN)0000(¬ZRO.SGN)(¬ZRN.PTY)  
 ..DOPIP IMPO,ND,0303,UCFLG  
 BRAX FETCHN



```

1099.
1100. 003405L
1101.
1102.
1103.
1104.
1105.
1106.
1107.
1108.
1109.
1110.
1111.
1112.
1113.
1114.
1115.
1116.
1117. 003405L 00110111 01000111
1118. 003406L 00110001 10001001
    003407L 00110001 10101000
1119. 003410L 11010100 11110111
    003411L 11010111 00010100
1120. 003412L 00110001 11100111
1121. 003413L 00110001 00110110
    003414L 00110111 11000000
1122. 003415L 00110111 01000111
1123. 003416L 11001110 11111111
    003417L 11010100 11110000
    003420L 11010111 00010100
1124. 003421L 00110111 00001100
1125. 003422L 00110001 00110110
    003423L 00110111 10001101
1126. 003424L 11011001 01000000
1127. 003425L 00110111 01000111
1128. 003426L 11011111 01000100
1129.
1130. 003427L
1131.
1132.
1133.
1134.
1135.
1136.
1137.
1138.
1139.
1140.
1141.
1142.
1143.
1144.

*
PLR:
. 3.10 ( 1R4) PLR.IDX          LOAD REGISTER FROM PAGED LOCATION
.      ( 105) PLR.IDX          A-REG LOAD (104 IS NOT A PLR)
.      ( 114) PLR.IDX          R <- (X,IDX)
.      ( 124) PLR.IDX
.      ( 134) PLR.IDX
.      ( 144) PLR.IDX
.      ( 154) PLR.IDX
.      ( 164) PLR.IDX

. 4.25 (111 124) DPL.IDX       C <- (X,IDX); B <- (X,IDX+1)
.      (062 114) DPLR.IDX      B <- (X,IDX); C <- (X,IDX+1)
.      (113 144) DPL.IDX       E <- (X,IDX); D <- (X,IDX+1)
.      (174 134) DPLR.IDX      D <- (X,IDX); E <- (X,IDX+1)
.      (115 164) DPL.IDX       L <- (X,IDX); H <- (X,IDX+1)
.      (176 154) DPLR.IDX      H <- (X,IDX); L <- (X,IDX+1)

STB      SMR          GET THE INDEX
DLDX     MR2PC        AND SAVE AWAY NEW PC

MWAIT    ,MEMPF3

LDX      XX2MRH+URX   MSB ADDRESS
LDPP     MAROL,MDR    LSB ADDRESS

STB      SMR          AND GET DATA
MWAIT    NOOP,MEMPF3

STB      IMAR
LDPP     I350,MDR     GOT THE DATA

BRA      FETPL,T@,IZ  IF IMP NOT ZERO GET ANOTHER BYTE
STB      SMR
BRA      DPLOAD

*
PSR:
. 2.20 ( 1R6) PSR.IDX          STORE REG INTO PAGED LOCATION
.      ( 107) PSR.IDX          A REG SAVE (106 IS NOT A PSR)
.      ( 116) PSR.IDX          (X,IDX) <- R
.      ( 126) PSR.IDX
.      ( 136) PSR.IDX
.      ( 146) PSR.IDX
.      ( 156) PSR.IDX
.      ( 166) PSR.IDX

. 3.35 (111 126) DPSR.IDX       (X,IDX) <- C; (X,IDX+1) <- B
.      (062 116) DPSR.IDX      (X,IDX) <- B; (X,IDX+1) <- C
.      (113 146) DPS.IDX       (X,IDX) <- E; (X,IDX+1) <- D
.      (174 136) DPSR.IDX      (X,IDX) <- D; (X,IDX+1) <- E
.      (115 166) DPS.IDX       (X,IDX) <- L; (X,IDX+1) <- H
    
```

. SINGLE AND DOUBLE PAGED LOAD AND STORE

1145.						
1146.						
1147.	003427L	00110111	01000111	STB	SMR	GET THE INDEX
1148.	003430L	00110001	10001001	DLDX	MR2PC	UPDATE THE PC SO IT CORRECT
	003431L	00110001	10101000			
1149.	003432L	11010100	11100101	MWAIT	,MEMPF3	
	003433L	11010111	00010100			
1150.	003434L	00110001	11100111	LDX	XX2MRH+URX	AND MSB ADDRESS FROM X-REG
1151.	003435L	00110001	00110110	LDPP	MAROL,MDR	LSB ADDRESS
	003436L	00110111	11000000			
1152.	003437L	00110001	11011101	LDPP	MDW,I35I	SAVE THE REGISTER IN MEMORY
	003440L	00110111	00101001			
1153.	003441L	11011000	00111011	BRA	DPSTOR,F@,IZ	STORE MSB IF IMP NON-ZERO
1154.	003442L	01011001	11111011	BRAX	FETCHW	
	003443L	11001111	11111100			

1157.						
1158.	003444L					
1159.						
1160.						
1161.						
1162.						
1163.						
1164.						
1165.	003444L	11011000	11011000	BRA	INCPAS,F@,IZ	
1166.	003445L	01010001	00000110	LDPI	LIMP,URL	USE HL IF NO IMP SPECIFICATION
	003446L	00110111	00000001			
1167.	003447L	00110001	11010000	INCPAS	LDTP	URI+URA
1168.	003450L	11011111	11001111	BRA	INCPIT	T LOADED WITH VALUE TO ADD, GO DO IT
1169.						
1170.	003451L					
1171.						
1172.						
1173.						
1174.						
1175.						
1176.						
1177.						
1178.						
1179.						
1180.						
1181.	003451L	11011000	11010011	BRA	INCPS,F@,IZ	
1182.	003452L	01010001	00000110	LDPI	LIMP,URL	... DEFAULT TO HL PAIR
	003453L	00110111	00000001			
1183.	003454L	01010001	00000001	INCPS	LDTI	1
1184.	003455L	11011010	11001111	BRA	INCPIT,F@,IO	ASSUME ITS BY 1 (ODD)
1185.	003456L	01010001	00000010	LDTI		2
1186.	003457L	00110111	00001001	STB	DIMP	NO, BY 2 CAUSE WAS EVEN
1187.	003460L	01101111	11110001	INCPIT	LDRT	TEMP1
1188.	003461L	00110001	11011111	DOPRP	IMPFO,AC,TEMP1,IMPI,CO	INC THE LSB (T-SAVE NECESSARY)
	003462L	01110010	00110001			
	003463L	00110111	01101111			
1189.	003464L	01011001	11111011	BRAX	FETCHN,FC	IF NO CARRY FORGET THE MSB
	003465L	11000000	11110111			
1190.	003466L	00110111	00001001	STB	DIMP	
1191.	003467L	00110001	11011111	DOPIP	IMPFO,AC,0,IMPI	INC THE MSB (COULD USE IT)
	003470L	01010010	00000000			
	003471L	00110111	01101111			
1192.						CAN'T USE 'IT IMPFO' BECAUSE DELAYED
1193.						ALU CARRY THROUGH PROCESSOR CARRY
1194.	003472L	11001111	11110111	BRA	FETCHN	

```

1195.
1196. 003473L
1197.
1198.
1199.
1200.
1201.
1202.
1203. 003473L 11011000 11000001
1204. 003474L 01010001 00000110
      003475L 00110111 00000001
1205. 003476L 00110001 11010000
1206. 003477L 11011111 10111000
1207.
1208. 003500L
1209.
1210.
1211.
1212.
1213.
1214.
1215.
1216.
1217.
1218.
1219. 003500L 11011000 10111100
1220. 003501L 01010001 00000110
      003502L 00110111 00000001
1221. 003503L 01010001 00000001
1222. 003504L 11011010 10111000
1223. 003505L 01010001 00000010
1224. 003506L 00110111 00001001
1225. 003507L 01101111 11110001
1226. 003510L 00110001 11011111
      003511L 01110100 00110001
      003512L 00110111 01101111
1227. 003513L 01011001 11111011
      003514L 11000000 11110111
1228. 003515L 00110111 00001001
1229. 003516L 00110001 11011111
      003517L 01010100 00000000
      003520L 00110111 01101111
1230. 003521L 11001111 11110111
    
```

```

+
DECPA:
. 1.50 ( 037) DECP HL <- HL - A
. 1.35 (062 037) DECP BC <- BC - A
. 1.35 (174 037) DECP DE <- DE - A
. 1.35 (022 037) DECP XA <- XA - A
. +0.65 IF BRW FROM LSB

      BRA      DECPAS,F@,IZ
      LDPI     LIMP,URL          SELECT HL AS DEFAULT REG PAIR

DECPAS  LDTP    URI+URA
      BRA      DECPIT          GO DECR. USING A-REG AS DISP.

*
DECP:
. 1.45 ( 035) DECP HL <- HL - 1
. 1.45 (111 035) DECP XA <- XA - 2
. 1.30 (062 035) DECP BC <- BC - 1
. 1.45 (113 035) DECP BC <- BC - 2
. 1.30 (174 035) DECP DE <- DE - 1
. 1.45 (115 035) DECP DE <- DE - 2
. 1.45 (117 035) DECP HL <- HL - 2
. 1.30 (022 035) DECP XA <- XA - 1
. +0.65 IF BRW FROM LSB

      BRA      DECPS,F@,IZ
      LDPI     LIMP,URL

DECPS  LDTI    1          EXACTLY LIKE ABOVE BUT USING SB'S NOT A
      BRA      DECPIT,F@,IO
      LDTI     2

DECPIT STB     DIMP
      LDRT    TEMP1
      DOPRP   IMPFO,SB,TEMP1,IMPI,CO

      BRAX    FETCHN,FC          IF NO CARRY FORGET THE MSB

      STB     DIMP
      DQPIP   IMPFO,SB,0,IMPI

      BRA     FETCHN
    
```

1233.						
1234.	003522L					
1235.						
1236.						
1237.						
1238.						
1239.						
1240.						
1241.						
1242.						
1243.						
1244.						
1245.						
1246.						
1247.						
1248.	003522L	00110111	01000111	STB	SMR	GET DISPLACEMENT LSP
1249.	003523L	01010001	01111001	BRC	INDX,,DECIT	GO TO INDEX SPECIFYING DECIT SET
	003524L	11011111	10101000			
1250.						
1251.	003525L					
1252.						
1253.						
1254.						
1255.						
1256.						
1257.						
1258.						
1259.						
1260.						
1261.						
1262.						
1263.						
1264.						
1265.	003525L	00110111	01000111	STB	SMR	GET DISPLACEMENT LSP
1266.	003526L	01010001	10001111	BAL	,INCIT	

\*  
 DECX:  
 . ( 025) DECI.LSP.IDX (X,IDX+1 | X,IDX) <-  
 . 7.30 (X,IDX+1 | X,IDX) - DSP  
 . (111 025) DECI.LSP.MSB.IDX (X,IDX+1 | X,IDX) <-  
 . 8.90 (X,IDX+1 | X,IDX) - DSP  
 . (062 025) LFID.LSP.IDX RP <- (X,IDX+1 | X,IDX) - DSP  
 . (174 025) LFID.LSP.IDX  
 . (176 025) LFID.LSP.IDX  
 . 6.40 (113 025) LFID.LSP.MSP.IDX RP <- (X,IDX+1 | X,IDX) - DSP  
 . (115 025) LFID.LSP.MSP.IDX  
 . (117 025) LFID.LSP.MSP.IDX  
 . 8.00

\*  
 INCX:  
 . ( 005) INCI.LSP.IDX (X,IDX+1 | X,IDX) <-  
 . 7.20 (X,IDX+1 | X,IDX) + DSP  
 . (111 005) INCI.LSP.MSP.IDX (X,IDX+1 | X,IDX) <-  
 . 8.80 (X,IDX+1 | X,IDX) + DSP  
 . (062 005) LFII.LSP.IDX RP <- (X,IDX+1 | X,IDX) + DSP  
 . (174 005) LFII.LSP.IDX  
 . (176 005) LFII.LSP.IDX  
 . 6.50 (113 005) LFII.LSP.MSP.IDX RP <- (X,IDX+1 | X,IDX) + DSP  
 . (115 005) LFII.LSP.MSP.IDX  
 . (117 005) LFII.LSP.MSP.IDX  
 . 8.20

MICRO-PROCESSOR EMULATION SUPPORT CODE - HJS - 79DEC12 16:20  
 . INDEXED LOCATIONS, INCREMENT AND DECREMENT IN PLACE OR TO REG PAIR

1267.  
 1268. 003527L  
 1269.  
 1270.  
 1271.  
 1272.  
 1273. 003527L 01101111 11110000  
 1274. 003530L 11010100 10100111  
 003531L 11010111 00010100  
 1275. 003532L 00110111 00001100  
 1276. 003533L 00110001 00110110  
 003534L 01101111 11110010  
 1277. 003535L 00110111 01000111  
 1278. 003536L 01010001 00000000  
 1279. 003537L 11011010 10011001  
 1280. 003540L 11010100 10011111  
 003541L 11010111 00010100  
 1281. 003542L 00110111 00001100  
 1282. 003543L 00110001 00110110  
 1283. 003544L 00110111 00001001  
 003545L 00110111 01000111  
 1284. 003546L 01101111 11110001  
 1285. 003547L 00110001 10001001  
 003550L 00110001 10101000  
 1286. 003551L 11010100 10010110  
 003552L 11010111 00010100  
 1287. 003553L 00110001 11100111  
 1288. 003554L 00110001 00110110  
 003555L 00110111 11000000  
 1289. 003556L 00110111 01000111  
 1290. 003557L 11101111 00000000  
 1291.  
 1292. 003560L 11010100 10001111  
 003561L 11010111 00010100  
 1293. 003562L 00110111 00001100  
 1294. 003563L 00110001 00110110  
 003564L 01110010 00110010  
 1295. 003565L 00110111 01000111  
 1296. 003566L 01101111 11110010  
 1297. 003567L 11010100 10001000  
 003570L 11010111 00010100  
 1298. 003571L 00110001 00110110  
 003572L 01110010 11110001  
 1299. 003573L 11011000 01101101  
 1300.  
 1301. 003574L 00110111 00101001  
 1302. 003575L 00110111 00000110  
 1303. 003576L 01110001 11110010  
 1304. 003577L 11010100 10000000  
 003600L 11010111 00010100  
 1305. 003601L 00110111 00001101  
 1306. 003602L 11011111 01111100

+  
 INDX  
 . INDEXED OPERATIONS TAKES 2 BYTES ON PAGE X-REG ADDS DISPLACEMENT TO IT  
 . AND STORES THE RESULT IN A REG. PAIR OR BACK ON TOP OF ITSELF

BAS	LINK	FREE REGISTER FOR INC, DEC SELECT
MWAIT	,MEMPF3	
STB	IMAR	
LDRP	TEMPL,MDR	SAVE LSP (LSP DISPLACEMENT)
STB	SMR	GET MSP OR INDEX
TCLR		ASSUME MSP IS ZERO
BRA	INDGET,F@,IO	
MWAIT	,MEMPF3	NO, GET MSP OF DISPLACEMENT
STB	IMAR	
LDTP	MDR	GOT MSB
STB	DIMP,SMR	CORRECT IMP REG AND GET INDEX
INDGET	LDRT	SAVE MSP
	DLDX	PC SAVED AS CORRECT VALUE NOW
MWAIT	,MEMPF3	GOT INDEX
LDX	XX2MRH+URX	MAR MSB FROM THE X-REG
LDPP	MAROL,MDR	INDEX TO THE MAR LSB
STB	SMR	
BRR	LINK	SELECT DECIT OR INCIT
* INCIT	MWAIT	,MEMPF3
STB	IMAR	
DOTRP	,AC,TEMPL,MDR,CO	ADD DATA AND DISPLACEMENT LSB
STB	SMR	START TO READ FOR MSB
LDRT	TEMPL	
MWAIT	,MEMPF3	
DOTRP	,AC,TEMPH,MDR	ADD MSB PART, LEAVE RESULT IN T
BRA	INDXL,F@,IZ	SELECT LOAD REG PAIR OR RELOAD MEMORY
INDXS	LDPT	PUT MSB RESULT BACK IN MEMORY
	LDPT	SET CONDITION CODES
	LDTR	
	MWAIT	,MEMPF3
		PUT LSB DATA BACK ALSO
STB	DMAR	IN CORRECT SPOT
DELAY	2	

1307.	003603L	00110111	00101001		LDPT	MDW	
1308.	003604L	01011001	11111011		BRAX	FETCHW	
	003605L	11001111	11111100				
1309.							
1310.	003606L	11010100	01111001	DECIT	MWAIT	,MEMPF3	
	003607L	11010111	00010100				
1311.	003610L	00110111	00001100		STB	IMAR	
1312.	003611L	00110001	00110110		DOTRP	,SB,TEMPL,MDR,CO	SUBTRACT DISPLACEMENT FROM THE DATA
	003612L	01110100	00110010				
1313.	003613L	00110111	01000111		STB	SMR	START TO READ FOR MSB FAST
1314.	003614L	01101111	11110010		LDRT	TEMPL	
1315.	003615L	11010100	01110010		MWAIT	,MEMPF3	
	003616L	11010111	00010100				
1316.	003617L	00110001	00110110		DOTRP	,SB,TEMPH,MDR	SIMILARLY FOR THE MSB PART
	003620L	01110100	11110001				
1317.	003621L	11011001	10000011		BRA	INDXS,T@,IZ	SELECT LOAD REG PAIR OR RELOAD MEMORY
1318.							
1319.	003622L	00110111	00001001	INDXL	STB	DIMP	CORRECT POINTER TO MSB
1320.	003623L	00110111	01101111		LDPT	IMPFO,IIMP	LOAD THE INDEX INTO A REGISTER PAIR
	003624L	00110111	00001000				
1321.	003625L	01110001	11110010		LDPR	IMPO,TEMPL	THE LSB ALSO
	003626L	00110111	10001111				
1322.	003627L	01011001	11111011		BRAX	FETCH	
	003630L	11001111	11111010				

1325.								
1326.	003631L							
1327.								
1328.								
1329.								
1330.								
1331.								
1332.								
1333.								
1334.	003631L 01010001 00111110							
	003632L 11011111 01011111							
1335.								
1336.	003633L							
1337.								
1338.								
1339.	003633L 01010001 01001101							
	003634L 01101111 11110000							
1340.	003635L 01010001 00000110							
1341.	003636L 11011111 01010001							
1342.								
1343.	003637L							
1344.								
1345.								
1346.								
1347.								
1348.								
1349.								
1350.								
1351.								
1352.								
1353.	003637L 01010001 01001101							
1354.								
1355.	003640L							
1356.								
1357.	003640L 01101111 11110000							
1358.	003641L 11011001 01010010							
1359.	003642L 11011010 01010111							
1360.	003643L 00110111 00001001							
1361.	003644L 00110001 11000100							
1362.	003645L 11011001 01010100							
1363.	003646L 00110001 11100011							
1364.	003647L 11101111 00000000							
1365.	003650L 00110001 11000010							
1366.	003651L 00110001 11100001							
1367.	003652L 11101111 00000000							
1368.	003653L 01010001 00000010							
1369.	003654L 11011111 01010001							
1370.	003655L 01010001 00000100							
1371.	003656L 00110111 00000001							
1372.	003657L 00110001 11000110							
	003660L 00110001 11100101							
1373.	003661L 11101111 00000000							

```

*
DS:
. 3.35 ( 027) DS (HL) <- E; (HL+1) <- D
. 4.05 (111 027) DS (HL) <- C; (HL+1) <- B
. 3.35 (113 027) DS (DE) <- C; (DE+1) <- B
. 3.20 (174 027) DS (BC) <- E; (BC+1) <- D
. 3.20 (176 027) DS (BC) <- L; (BC+1) <- H
. 3.35 (117 027) DS (DE) <- L; (DE+1) <- H

BRC DLS,,DSTORE SELECT REG PAIRS & DO SAVE

*
DLHL:
. 3.95 ( 057) DL L <- (HL); H <- (HL+1)

BAL LINK,DLOAD LOAD REG PAIR

LDTI URL HL
BRA DLSLMP FROM (HL)

*
DL:
. 3.95 ( 047) DL E <- (HL); D <- (HL+1)
. 4.65 (111 047) DL C <- (HL); B <- (HL+1)
. 3.80 (062 047) DL C <- (BC); B <- (BC+1)
. 3.95 (113 047) DL C <- (DE); B <- (DE+1)
. 3.80 (174 047) DL E <- (BC); D <- (BC+1)
. 3.95 (115 047) DL E <- (DE); D <- (DE+1)
. 3.80 (176 047) DL L <- (BC); H <- (BC+1)
. 3.95 (117 047) DL L <- (DE); H <- (DE+1)

BAL ,DLOAD LOAD SELECT

*
DLS DECODE ADDRESS & REG SPEC. OPERATORS

BAS LINK
BRA DLSZRO,T@,IZ DE,HL - 000
BRA DLSBC,F@,IO XX,BC - 062, 114...
STB DIMP
LDX DE2MRL DELAY ONE FROM THE DIMP BEFORE BRA
BRA DLSONE,T@,IZ BC,HL - 111
LDX DE2MRH
BRR LINK XX,DE - 113, 115...
DLSBC LDX XX2MRL+URC XX,BC - 062, 114...
LDX XX2MRH+URB
BRR LINK
DLSONE LDTI URC BC,HL - 111
BRA DLSLMP
DLSZRO LDTI URE DE,HL - 000
DLSLMP LDPT LIMP
DLDX HL2MR XX,HL - 000, 111, HL,HL
BRR LINK
    
```



1374.									
1375.	003662L								
1376.									
1377.	003662L	00110111	01000111						
1378.	003663L	11001110	11111111						
	003664L	11010100	01001011						
	003665L	11010111	00010100						
1379.	003666L	00110111	00001100						
1380.	003667L	00110001	00110110						
	003670L	00110111	10001111						
1381.	003671L	00110111	01000111						
	003672L	00110111	00001001						
1382.	003673L	11010100	01000100	DPLOAD	MWAIT	,MEMPF3			
	003674L	11010111	00010100						
1383.	003675L	00110001	00110110						
	003676L	00110111	10001111						
1384.	003677L	01011001	11111011	FETPL	BRAX	FETCH			
	003700L	11001111	11111010						
1385.									
1386.	003701L								
1387.									
1388.	003701L	00110001	11011111						
	003702L	00110111	00101001						
	003703L	00110111	00001001						
1389.	003704L	00110001	11011111	DPSTOR	LDTP	IMPI			
1390.	003705L	11010100	00111010		MWAIT	,MEMPF3			
	003706L	11010111	00010100						
1391.	003707L	00110111	00001100						
1392.	003710L	11011111	00110110						
1393.	003711L	00110111	00101001						
1394.	003712L	01011001	11111011						
	003713L	11001111	11111100						

\*  
 DLOAD LOAD REGISTER PAIR FROM MEMORY

STB SMR  
 MWAIT NOOP,MEMPF3

STB IMAR  
 LDPP IMPO,MDR GET THE LSB DATA

STB SMR,DIMP

DPLOAD MWAIT ,MEMPF3

LDPP IMPO,MDR GET THE MSB

FETPL BRAX FETCH

\*  
 DSTORE SAVE REGISTER PAIR IN MEMORY

LDPP MDW,IMPI,DIMP OUTPUT LSB AND POINT TO MSB

DPSTOR LDTP IMPI  
 MWAIT ,MEMPF3

STB IMAR  
 DELAY 2  
 LDPT MDW OUTPUT MSB  
 BRAX FETCHW

```

1397.
1398. 003714L
1399.
1400.
1401.
1402. 003714L 00110001 11011100
      003715L 01000101 00000100
1403. 003716L 11010010 00010110
1404. 003717L 01010001 10101011
      003720L 00110111 11000000
      003721L 01010001 11101111
      003722L 00110111 11100000
1405. 003723L 00110001 11011111
      003724L 00110111 00000011
1406. 003725L 00110111 00101001
1407. 003726L 01011001 11111011
      003727L 11001111 11111100
1408.
1409. 003730L
1410.
1411.
1412.
1413.
1414.
1415. 003730L 00110001 11011100
      003731L 01000101 00000100
1416. 003732L 11010010 00010110
1417. 003733L 01010011 00000001
      003734L 00110111 10001100
1418. 003735L 00110111 00000100
1419. 003736L 01011001 11111011
      003737L 11001001 11110111
1420. 003740L 11001111 10011101
1421.
1422. 003741L
1423.
1424.
1425. 003741L 00110001 11011100
      003742L 01000101 00000100
1426. 003743L 11010010 00010110
1427. 003744L 01010101 11111110
      003745L 00110111 10001100
1428. 003746L 00110111 00000100
1429. 003747L 01011001 11111011
      003750L 11001111 11110111

```

```

*
BRL:
. 1.80 ( 072) BRL      BASE REGISTER LOAD
      (IMP 072) BRL    BASE <- (SEBRLS) <- R
      TSTIP      ,SWUSER,PSWI
      BRA        IVIOL3,FZ
      DLDPI      MARO,SEBRLS      SAVE BASE REG VALUE AWAY
      LDPP       BASW,IMPI        LOAD BASE REG BEFORE WRITE!
      LDPT       MDW
      BRAX       FETCHW

*
EI:
. 1.05 ( 050) EI      ENABLE INTERRUPTS
. 4.10 (111 050) EJMP.LSB.MSB  ENABLE INTERRUPTS & PC <- NN
. 6.40 (062 050) EUR    ENABLE INTERRUPTS & USER &
      PC <- (SP+1 | SP); SP <- SP + 2
      TSTIP      ,SWUSER,PSWI    NOT ALLOWED IN USER MODE
      BRA        IVIOL3,FZ
      DOPI       PSWO,OR,SWINTE  SET THE INTERRUPTS ON BIT
      LDPT       MODW
      BRAX       FETCHN,T@,IZ    IN EMULATION SUPPORT ALSO
                                      WAS SIMPLE EI
      BRA        EIROJ          WAS EJMP OR EUR

*
DI:
. 1.05 ( 040) DI      DISABLE INTERRUPTS
      TSTIP      ,SWUSER,PSWI    NOT ALLOWED IN USER MODE
      BRA        IVIOL3,FZ
      DOPI       PSWO,ND,-I-SWINTE  RESET THE BIT, DISABLING INTERRUPTS
      LDPT       MODW
      BRAX       FETCHN
                                      IN EMULATION SUPPORT ALSO

```

*TSTIP, SUB4K*

*BRA*

*LDPP STW, S STI 6E*

*LDPP MDW, IMPI*

*LDPT BASW*

*WAIT, MEMOR*

*BRA IDLAY, FC, IZ*

*IDLAY*

*LDAP STW, S STI 6E, UNK HUKA*

*BRAX FETCHN*

```

1430.
1431. >003751L 01011001 11111111
      >003752L 11001111 11111111
1432.
1433. 003753L 01011001 11111011
      003754L 11001111 01101110
1434.
1435. 003755L 11111111 11111111
      003756L 11111111 11111111
      003757L 11111111 11111111
      003760L 11111111 11111111
      003761L 11111111 11111111
      003762L 11111111 11111111
      003763L 11111111 11111111
      003764L 11111111 11111111
      003765L 11111111 11111111
      003766L 11111111 11111111
      003767L 11111111 11111111
      003770L 11111111 11111111
      003771L 11111111 11111111
      003772L 11111111 11111111
      003773L 11111111 11111111
      003774L 11111111 11111111
      003775L 11111111 11111111
      003776L 11111111 11111111
      003777L 11111111 11111111
1436. 002000
1437. 002000
1438. 002000
1439.

```

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*
IVIOL3  BRAX  IVIOL$
.
MEMPF3  BRAX  MEMPF$
.
TABPAGE  PRODL
.
PRODLN  EQU  $-PRODP
        USE  PRODL
        SKIP PRODLN
        END

```

DL PPI MARO, SE BALS  
TSTIP , SWSEK, PSWI  
BRA IVIOL3, FZ  
TSTIT , SW64K  
BRA , FZ  
LDP BASW, JMPI  
LDPT MDW  
BAAX FETCHW  
LDPR STW, SST16E  
LDP BASW, JMPI  
LDPT MDW  
NOOP  
MWAIT NOOP, TSTIP  
LDPR STW, LST16E  
BAAX FETCHW







003751	IVIOL3	*1431	1403	1416	1426									
020004	IZ	*17:I	101	159	253	320	399	414	486	505	811	904	1028	
		1126	1153	1165	1181	1203	1219	1299	1317	1358	1362	1419		
002447	JUMP	*444	185	436										
002441	JUMPC	*423												
010001	KBSCNT	*26:I												
002523	L7S	*497												
002531	L7SI	*509	505											
002467	LD6	*460												
002502	LD7	*479												
002514	LD7CMN	*492	488											
002507	LD7I	*489	486											
002537	LDS	*513												
	LIMP	69	111	160	168	215	254	270	321	329	346	357	400	
		415	1166	1182	1204	1220	1371							
030000	LINK	*41:I	122	141	159	218	237	253	579	580	991	1004	1273	
		1290	1339	1357	1364	1367	1373							
	LIREG	78												
	LSPKR	771	779	783										
	LUCF	1040	1048	1058	1071	1086								
	LUF	586	913	937	944	1007	1011	1302						
	MARIH	822	847	906	910	993	998	1030	1044					
	MARIL	822	847	906	910	993	998	1030	1044					
	MAROH	150	275	454	832	1404								
	MAROL	133	150	275	385	455	829	1121	1151	1288	1404			
	MDR	78	114	117	171	175	232	236	278	351	355	451	454	
		475	493	546	559	820	829	845	908	913	996	1003	1035	
		1047	1121	1125	1151	1276	1282	1288	1294	1298	1312	1316	1380	
		1383												
	MDW	134	140	324	328	507	510	820	845	947	1006	1010	1037	
		1047	1152	1301	1307	1388	1393	1406						
002250	MEMNBAS	*279	274											
002272	MEMPA	*295	288											
002221	MEMPF\$	*260	112	116	148	169	174	230	238	326	354	358	1433	
002220	MEMPF2	*259	63	75	449	453	473	495	545	557	631	662	680	
003753	MEMPF3	*1433	816	828	836	841	881	907	912	995	1002	1034	1046	
		1119	1123	1149	1274	1280	1286	1292	1297	1304	1310	1315	1378	
		1382	1390											
002077	MEMPFPS	*141	137											
002253	MEMPQ	*281	277											
002275	MEMPR	*299	296											
002270	MEMPS	*292	284											
002274	MEMPW	*298	286											
002266	MEMPX	*290	282	293										
020002	MO	*15:I	59	63	75	112	116	137	148	169	174	230	234	
		277	282	326	349	354	358	449	453	473	492	545	557	
		631	662	680	816	828	836	841	881	907	912	995	1002	
		1034	1046	1119	1123	1149	1274	1280	1286	1292	1297	1304	1310	
		1315	1378	1382	1390									
	MODW	61	129	149	223	235	269	359	663	1418	1428			
020003	MP	*16:I	63	75	112	116	137	148	169	174	230	277	282	
		326	349	354	358	449	453	473	492	494	545	557	631	





	SCDSPNL	653												
	SCHUMS	657												
	SCLST	684												
	SCONMS	655												
	SCRAMI	299												
	SCROMLI	290												
	SEBRLS	275	1404											
002421	SIRO	*395												
002430	SIRX	*404												
	SL	1032	1079											
003341	SLC	*1053												
	SMR	67	110	115	167	172	224	233	243	275	345	352	398	
		413	448	452	472	475	487	491	543	556	668	814	825	
		834	839	905	909	992	997	1027	1117	1122	1127	1147	1248	
		1265	1277	1283	1289	1295	1313	1377	1381					
	SP2MRH	130	222											
	SP2MRL	224												
	SPIH	388												
	SPIL	131	389											
	SPOL	132	229											
	SR	577	1036	1038	1068	1082	1084							
003350	SRC	*1062												
003361	SRE	*1074												
	SRMEMPE	289												
	SRSTPE	292												
	SRSYSMF	281												
002645	SRVDO	*641	72											
002017	SRVEND	*74	669											
002024	SRVID	*79	665											
002643	SRVNXT	*633	742	772	780	784								
	SRVREQ	71	638	879										
002636	SRVRPT	*628	884											
002653	SRVRTW	*660	639											
	STATUS	102	208	435										
	STEK	266												
002330	STKL	*332	320											
002351	STKLPF	*353	349											
002277	STKS	*303												
	STLA	287												
	STLSP	283												
	STLW	285												
	STUSCF	102	208	435										
	SVAVIOL	295												
	SVONEMS	678												
	SVWVIOL	298												
	SWINTE	1417	1427											
	SWRPT	630	664	682	965									
	SWUSER	129	192	223	269	382	722	1402	1415	1425				
002400	SYSM	*367	344											
002372	SYSRET0	*362												
	SYSRET1	363												
030001	TEMP1	*42:I	44:I	266	283	451	455	575	586	591	596	601	612	

