Artist
TRANSFORMER
High Resolution Graphics Controller

PRELIMINARY

Technical Reference

and

Guide to Operation

CONTROL SYSTEMS, INC.
Minneapolis, MN

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High Resolution Graphics Controller

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TRANSFORMER Installation Guide

Of course, the first thing you'll want to do when you get your TRANSFORMER is try it out. This setup guide will help install your TRANSFORMER hardware in your IBM PC, IBM PC XT, or compatible computer system. It will also show you how to load and run a special program which allows you to test the installation.

You can usually install the TRANSFORMER and have it up and running in only a few minutes. In these installation instructions, we assume that you are somewhat familiar with your computer's hardware and with DOS software operation. We also assume that the TRANSFORMER will be installed as shipped, without modification, and that it will be operated in addition to or as a direct replacement for an IBM display adapter (that is, using the same I/O port addresses). Read through these setup instructions before you begin. If you are unsure about any of the procedures, consult the references mentioned.

2.1 What's Shipped in the TRANSFORMER Package?

The TRANSFORMER package includes both hardware and software. The package includes:

- The TRANSFORMER board -- configured at the factory for your monitor. A DAC chip is installed if you are using an analog monitor.

- (OPTIONAL) A video interface cable. If you are using an analog monitor, a cable with separate 75 ohm BNC-type connectors for RGB input to your monitor is shipped in the TRANSFORMER package. If you have a TTL monitor, you will be using the video interface cable supplied with your monitor, unless you specifically ordered a monitor cable with your TRANSFORMER.

- A plastic adapter card guide.

- The Artist TRANSFORMER Utilities and Graphics Primitives diskette.

- The Artist TRANSFORMER Tutor 3 diskette (includes INTRO3.COM).

- The TRANSFORMER Setup Specification sheet.

- This User's Guide.

Verify that you have these items. If anything is missing or damaged, contact your dealer. Note that Appendix A of this guide lists the files currently shipped on each distribution diskette.

2.2 What You Need

In addition to the items shipped in the TRANSFORMER package, you will need the following items to complete the TRANSFORMER installation and setup:

- IBM PC, IBM PC XT, IBM PC AT or compatible system with at least one double-sided diskette drive.

- Your graphics monitor (the one specified for use with the TRANSFORMER).

- The video interface cable (if you are supplying this cable).

- A medium size flat head screwdriver or a 3/16" nut-driver or wrench.

- DOS Version 2.0 or later operating system files.

- Two or more blank diskettes.

Optional, but extremely helpful, are your computer and monitor hardware manuals as well as the operating system manuals.

2.3   Preparing the Test Software

1.   If possible, you should make back-up copies of all the disks shipped in your TRANSFORMER package before you proceed with the hardware installation.   If you have only one computer and the TRANSFORMER is your only display adapter, ·you can make the back-up copies after the board is installed.   See **Section 2.6 Testing the System** for more information.

2.   Before you begin the installation, prepare a bootable test diskette so that you can check out the system after the TRANSFORMER is installed.

If you are using a TTL monitor with your TRANSFORMER, you can use any bootable DOS system disk to start the system and operate in a standard IBM mode. All you need to do to prepare a new test disk is to copy the files from the Tutor 3 diskette to any bootable system disk.

If you are using an analog monitor with your TRANSFORMER, you must prepare a bootable DOS system disk which also contains the initialization file LDLT.COM, the system start up file AUTOEXEC.BAT (which includes the command to run LDLT.COM), as well as the files shipped on the Tutor 3 diskette.

If you do not have a display adapter card installed in your system and a working monitor, you can make the bootable system disk after you complete the TRANSFORMER installation. **Section 2.6 Testing the System** explains how to start the system without the test diskette prepared in the steps below.

Follow these steps to prepare the test diskette:

a. Power up the system and start DOS.

b. With the DOS system disk in drive A and a blank diskette in drive
    B, enter the command:

        A>**FORMAT B:/S**

    When the formatting operation is completed, exit FORMAT by typing
    "N" at the prompt.

c. Insert the TRANSFORMER Tutor 3 disk in drive A and enter this
    command:

        A>**COPY A:*.* B:**

    When the copy operation is completed, remove the TRANSFORMER Tutor
    3 diskette from drive A and put it in a safe place.

d. The test program you will be using is INTRO3.COM.   This program
    should not be operated after the DOS console device driver program
    ANSI.SYS has been loaded because ANSI.SYS contains a value which
    resets the TRANSFORMER mode register to 80 x 25 text mode whenever
    the screen is scrolled.   So that a ANSI.SYS device driver is not
    loaded at start up, you can erase the CONFIG.SYS file shipped on
    the Tutor 3 diskette and copied to your new diskette in step "c"
    above. To erase the file, enter the command:

        A>**ERASE B:CONFIG.SYS**

Put the diskette that you just made aside.   You will use this diskette
to test the system when you have completed the installation.

In addition to the test program INTRO3, the TRANSFORMER Tutor 3
diskette contains a program called TUTOR3 which allows you to try out
the functions of the ARTLIB graphics primitives library. You may want
to prepare a TUTOR3 diskette at this time.   To do that, use the second
blank diskette and follow these steps:

a. With the DOS system disk in drive A and a blank diskette in drive
    B, enter the command:

        A>**FORMAT B:/S**

    When the formatting operation is completed, exit FORMAT by typing
    "N" at the prompt.

b. TUTOR3 uses the ANSI.SYS console device driver.   To copy the DOS
    file ANSI.SYS to the new diskette, enter this command:

        A>**COPY A:ANSI.SYS B:**

c. Insert the TRANSFORMER Tutor 3 disk in drive A and enter this command:

A)**COPY A:*.* B:**

When the copy operation is completed, remove the TRANSFORMER Tutor 3 diskette from drive A and put it in a safe place.

Whenever you want to use the TUTOR3 program, load DOS from this new diskette (at power up or reset the system with CTRL-ALT-DEL) so ANSI.SYS becomes the console driver. When you exit from the TUTOR3 program, reset the system again using a system disk which does NOT contain ANSI.SYS.

NOTES for Users of the TRANSFORMER Analog Version:

If you are using an analog version of the TRANSFORMER, the program LDLT.COM **must** be run whenever the system is turned on in order to initialize the TRANSFORMER for standard color output. Although the values loaded by LDLT into memory at power-up are not disturbed at a system reset (CTRL-ALT-DEL), loading LDLT whenever DOS is booted does no harm.

The command file AUTOEXEC.BAT that you copied from the Tutor 3 diskette includes the LDLT command, which tells DOS to search for and load LDLT.COM at each system start up. While you can use this diskette as your boot disk whenever you power up the system, you will probably want to prepare a new system boot disk or modify your present boot disk and include only the TRANSFORMER files necessary for system initialization.

2.4   Setting Up the TRANSFORMER

1.   Remove the TRANSFORMER from its packing material.

2.   When you ordered your TRANSFORMER, the board was individually configured at the factory to match your monitor type. The **TRANSFORMER Setup Specification** sheet describes the configuration of your TRANSFORMER board. Check that the board is configured properly for your monitor and system setup.

If you are using an analog monitor, be sure that the DAC chip is installed in the upper right corner of the card. If you ordered a TTL compatible version of the TRANSFORMER, the socket should be empty.

You may also want to check that the TRANSFORMER's video sync outputs match your monitor's inputs. Your monitor manual should list the monitor's video sync input specifications.

Chapter 7 of this manual explains how the TRANSFORMER configuration options are set and how they can be modified.

3.   Install a jumper block across two (2) pins of J1 to select the
      TRANSFORMER's operating mode -- that is, it selects the I/O port base
      address.   This jumper determines whether the TRANSFORMER operates like
      an IBM monochrome display adapter, an IBM color/graphics display
      adapter, or both.

      Jumper J1 is a Berg-strip header, located in the lower middle section
      of the card, below the uPD7220 and MC6845 chips.   Your jumper options
      are "M" -- monochrome, "C" -- color, or "B" -- both.
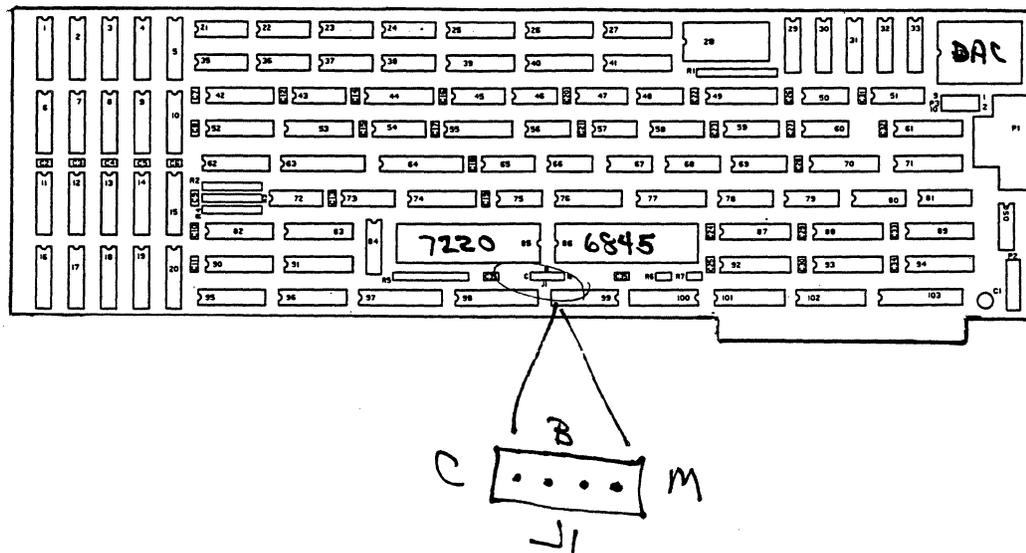
Figure 2.1   TRANSFORMER Board Layout and Jumper J1

      If the TRANSFORMER is the **ONLY** display adapter card installed in the
      system and you want the TRANSFORMER to simulate both the IBM
      color/graphics adapter and the IBM monochrome adapter, be sure that the
      jumper block is installed across the two middle pins of J1.

      If you want the TRANSFORMER to operate as if it were an IBM monochrome
      adapter, place the jumper block across the two pins at the right of J1.
      Select this option if an IBM color/graphics adapter is also installed
      in the system.

      If you want the TRANSFORMER to operate as if it were an IBM
      color/graphics adapter, place the jumper block across the two pins at
      the left of J1.   Select this option if an IBM monochrome display
      adapter is also installed in the system.

2.5 Installing the TRANSFORMER

Follow the steps outlined here to install the TRANSFORMER board in your IBM
PC or IBM PC XT.   If you are not using an IBM PC or PC XT, these
installation instructions may not be exactly correct. If you are using some
other compatible hardware system, you will need to consult your computer's
hardware manual for guidance in installation of expansion boards.

1.   Turn the power off the computer's System Unit and all peripherals
      connected to it.

2.   Disconnect all power cords and cables from the System Unit.

3.   If necessary, move the System Unit to a clear work surface.

4.   Using the screwdriver, nut-driver, or wrench, remove the cover mounting
      screws on the back of the system unit cabinet.   Some System Unit
      cabinets have only two mounting screws on the lower corners.   Other
      units have five screws, one at each corner and one at the center of the
      cabinet's back panel.
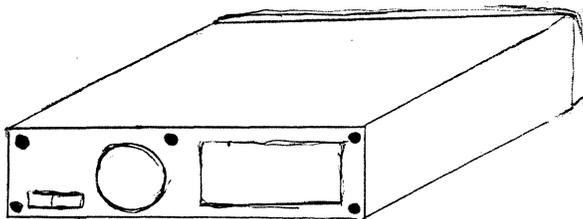
Figure 2.2 System Unit Back Panel Mounting Screws

5.   Remove the System Unit cover.   To do this, gently slide the cover
      forward until it stops and then lift slightly to completely remove it.

6.   Locate the system expansion slot where you will install the TRANSFORMER
      board. The TRANSFORMER can be installed in any full length slot.

7.   If there is no other display adapter already installed in the system,
      or if you are installing the TRANSFORMER in a new slot as a second
      adapter, remove the blank expansion slot cover from the cabinet back
      panel at the position where you want to install the TRANSFORMER.
      First, remove the screw that holds the metal slot cover in place and
      then, pull the slot cover out. Save the slot cover for later use.

      Figure 2.3 illustrates the interior of the System Unit.   It shows the
      expansion slots and the expansion slot covers.
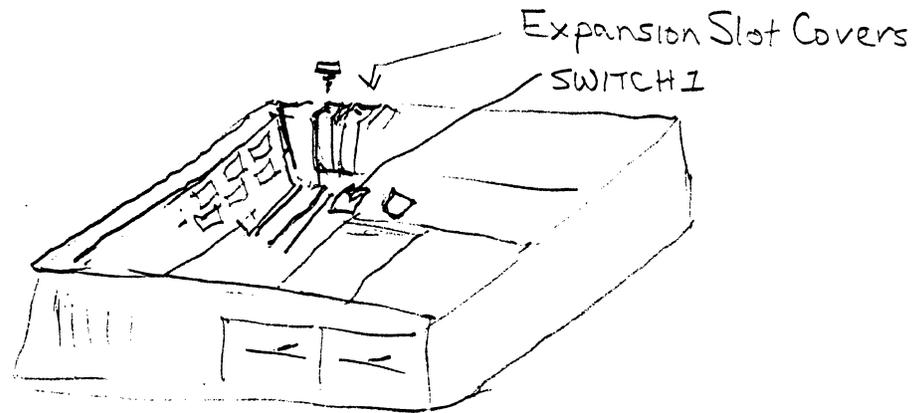
Figure 2.3 Interior of System Unit

8.   Snap the plastic card guide into the front of the cabinet opposite the
     expansion slot you selected.   Look for a double row of holes at the
     front of the cabinet.   Position the card guide vertically, parallel to
     the holes and push it into place.

9.   If you are replacing a previously installed display adapter card, you
     must first remove the card you want to replace.   Locate the card and
     remove the screw in the back panel which holds the card's retaining
     bracket in place.   Grasp the top edge of the card and pull firmly to
     lift the card out of the cabinet.

10. Insert the TRANSFORMER card into the selected system expansion slot.
     Be sure that the front edge of the card slips into the card guide's
     groove.   Then   press the TRANSFORMER squarely into   the selected
     expansion slot.   Be sure that the TRANSFORMER's 62-pin bus connector is
     firmly seated in the expansion slot.

11. Align the hole on the TRANSFORMER's retaining bracket with the threaded
     hole on the upper edge of the cabinet's back panel.   Insert the screw
     you removed earlier and tighten it.

12. You must set up System SWITCH 1 located on the System Board to
     correspond to your display adapter setup.   This switch setting
     indicates to the system software the type of display adapter(s)
     installed and the operating mode you want at system start up.

     SWITCH 1 is an 8-position DIP switch.   When the System Unit is viewed
     from the front, you can see SWITCH 1 on the floor of the System Unit
     cabinet closest to the last system expansion slot on the right, near
     the center of the System board.   Figure 2.3 shows the location of this
     switch.

     Positions 5 and 6 of SWITCH 1 must be configured.   Table 2.1 explains
     the possible settings.   Use a pointed object like a ball point pen to
     set the switches.

Table 2.1   System SWITCH 1 Settings

Monitor Adapter Type	SW5	SW6
MONOCHROME or BOTH (more than 1 adapter)	OFF	OFF
COLOR (in 80 x 25 mode)	ON	OFF
COLOR (in 40 x 25 mode)	OFF	ON

If the TRANSFORMER is the only display card installed in the system, you can select any of the these settings. Be sure to set the system switch to **BOTH** if you have a monochrome display adapter and a TRANSFORMER installed in the system, or the monochrome monitor may be damaged.

13.   Replace the System Unit cover and refasten the screws on the System Unit back panel.

14.   Connect the monitor to TRANSFORMER board now installed in the System Unit.   Locate the TRANSFORMER's 9-pin D-Sub video output socket and connect the 9-pin D-Sub monitor cable plug to it.   Connect the other end of the monitor cable to the monitor.   If you are using an analog monitor where a separate output is provided for each color, match the output plugs on the cable (they are color coded) to the sockets on your monitor.

15.   Reconnect the keyboard and all other peripheral cables to the System Unit and reconnect all power cables.

2.6 Testing the System

Now that the TRANSFORMER is installed, you are ready to power up the system to check that the installation is OK. You may also need to make some adjustments to the monitor.

1.   Turn on the monitor and power up the system.

2.   Load DOS.

   a.   Using the test diskette you made earlier, load DOS from drive A.

   At this point, the normal system start up should occur. That is, the system memory check should proceed as normal.   When that is completed, DOS loads and you should see the DOS system DATE prompt.   Enter the date and, at the TIME prompt, enter the time. Alternatively, press ENTER twice until the system prompt **A)** appears.

   b.   If you were not able to make a test diskette earlier, you will have to use your master diskettes to get up and running.   Don't forget to make back-up copies as soon as possible.   If you are using a TTL monitor, start DOS as described . above from any bootable DOS system disk.   Then put your TRANSFORMER Tutor 3 disk

in drive A.   If you have an analog monitor,   start DOS   from   any
bootable DOS system disk.   When random color appears on   the
monitor   screen,   press ENTER twice.   Then,   put the TRANSFORMER
Tutor 3 disk in drive A and type blindly **LDLT** and press ENTER.

3.   Don't be disturbed if you can't read the prompts and the image on your
     screen is garbled or distorted.   It is' very common for monitors to
     require adjustments to the vertical and horizontal hold or height and
     width (vertical and horizontal sync) controls.

     On some monitors,   these can be adjusted by controls located on the
     outside of the monitor.   On other monitors,   the controls are located
     inside the monitor case.   Locate these controls on your monitor and
     gradually adjust the controls until the system prompt is readable and
     displayed in the correct location on the screen.

     If you have trouble locating the adjustment controls or adjusting the
     monitor,   consult your monitor manual.   Most monitor manuals contain
     details of where and how to adjust the monitor controls in order to
     display an undistorted image.

     If you need to make adjustments inside the monitor case,   be sure to
     turn off the monitor (and power down the system) before you remove the
     case.   After you have removed the case, you can turn on the monitor and
     restart DOS.   Be very careful when adjusting an unprotected monitor;
     there are very high voltages present.

4.   When you are satisfied with the image displayed at the system prompt,
     start the TRANSFORMER test program INTRO3.   This program allows you to
     quickly check the TRANSFORMER card functions,   including those of the
     uPD7220 chip.   At the system prompt, enter:

          A> **INTRO3**

     After INTRO3 is started,   a series of four prompts are displayed on the
     monitor.   You must answer these prompts to completely initialize the
     system.   If you need to exit from INTRO3 at any time during the
     initialization procedure,   you must type **Ctrl-Alt-Del** to reset the
     system.   After you have initialized the system by answering the first
     four prompts,   you can exit from INTRO3 by entering **A** from the main
     menu.

5.   At the first prompt:

          TTL or Analog?
          ■■■■■■■■■■■■■■

          1) TTL
          2) Analog

     Enter the option, **1** or **2**,   which corresponds to your monitor type.   If
     you enter any other value or type a number from numeric keypad or the
     function keys, the computer beeps and waits for an acceptable response.
     It is not necessary to press the enter or return key.

6.   The next prompt requests the TRANSFORMER's I/O port base address.   At
      the prompt:

            Enter I/O Port Base Address
            ███████████████████████████████

      Seven possible I/O port base addresses are shown.   An arrow is
      displayed beside default factory setting 3D0.   Enter **7** to select this
      address.   If your board uses an alternate address, select the correct
      option.

7.   INTRO3 next asks you for your monitor parameters.   These parameters are
      used to synchronize operation of the TRANSFORMER and your monitor.
      This is the prompt :

            Graphics controller initialization
            ██

            1) Input parameters from terminal
            2) Input parameters from file

            Press 1, 2 or use Function Keys

      The initialization parameters can be entered either from a file or from
      the keyboard.

      Files containing parameter lists for most monitors used with the
      TRANSFORMER are supplied on your Tutor 3 disk.   They were copied to
      the test disk during the software setup.   The parameter files are
      supplied for a variety of monitors. Files are included for these non-
      interlaced displays:

Display Type:	**At Resolution:**	**Parameter File name:**
NEC 1401	640 x 400	640X400N.NEC
	640 x 480	640X480N.NEC
NEC 1410	640 x 400	640X400N.410
Gigatek 1331	640 x 400	640X400N.GIG
	640 x 480	640X480N.GIG
PGS SR-12	640 x 400	640X400N.PGS
	640 x 480	640X400N.PGS
Radio Shack Tandy CM-1	640 x 400	640X400N.TAN
IBM Professional	640 x 400	640X400N.PRO
Graphics Display	640 x 480	640X480N.PRO
TAXAN 440	640 x 400	640X400N.TAX
Electrohome G09	640 x 400	640X400N.ELH

Parameter files are supplied for these monitors operating in interlaced mode:

Display Type:	At Resolution:	Parameter File name:
IBM Color	640 x 400	640X400I.IBM
Graphics Display	640 x 480	640X480I.IBM
50Hz European	640 x 400	640X400I.EUR
Display	640 x 480	640X480I.EUR
CS GENLOCK Option	640 x 400	640X400I.GEN
	640 x 480	640X480I.GEN
Zenith ZVM136	640 x 400	640X400I.ZVM
	640 x 480	640X480I.ZVM

If your monitor is one of those for which a parameter file is supplied, select option **2** for file input. At the prompt:

Specify file name:

Enter the file name.   Specify a 640 x 400 pixel resolution file for this test.   After you enter the file name, INTRO3 reads the data from the file.   If INTRO3 cannot find the file you entered, it displays the message **File Not Found** and again asks you to enter the file name.   Be sure that the file you enter is on the current disk or specify the drive.   INTRO3 will not proceed until you have entered an acceptable file name.   If the file or parameters you specify are not correct for your monitor, the screen may display trash.   Do not operate the monitor with incorrect parameters; the monitor could be damaged.

If a parameter file is not supplied for your monitor, you must   enter each of the monitor parameters from the keyboard.   Select option **1** and at each prompt enter the required information.   These values must be entered:

```
1.   Interlace mode
2.   Active words per line (i.e. pitch)
3.   Horizontal sync (hs)
4.   Vertical sync (vs)
5.   Horizontal front porch (hfp)
6.   Horizontal back porch (hbp)
7.   Vertical front porch (vfp)
8.   Vertical back porch (vbp)
9.   Active display lines (al)
10.  Display area length (len)
```

As each prompt is displayed you must enter a value.   From these values, INTRO3 calculates the horizontal and vertical resolutions. INTRO3 also asks you if you want to save these parameters in a file. If you answer yes, INTRO3 prompts you to enter the file name where the parameters are to be saved.

If you are unsure of the correct monitor initialization values to
enter, Appendix B describes how these values are calculated and how
they can be changed based on the monitor's specifications.   Contact
your dealer or Control Systems if you need additional assistance.

8.   The last initialization prompt displayed by INTRO3 allows you to
     configure the TRANSFORMER's display planes.   For this test, at the
     prompt:

     Enter number of planes [3,4,5]
     ================================

     Enter **5** which configures the TRANSFORMER so that five display planes
     are possible.   In this mode, one plane of display memory is used by the
     MC6845 chip in text mode and four planes are reserved for use by the
     uPD7220 chip which displays the high resolution bit-mapped graphics.

9.   As soon you enter the final initialization value, INTRO3 initializes
     the system using these values.   INTRO3 then draws the Control Systems
     logo.   This graphics screen is the first screen displayed during the
     test which uses and is controlled by the uPD7220 chip. If the logo is
     distorted or not properly synchronized, the monitor may need additional
     minor adjustment or the monitor initialization values you entered may
     not be correct for your system.

10. When the logo screen is completely drawn, a menu of possible functions
     appears in the upper half of the screen.   This menu is overlaid on top
     of the graphics screen.

     Enter **C** to clear the logo from the graphics screen.   Then, select any
     of the menu options and enter the corresponding letter from the
     keyboard.   INTRO3 prompts you to enter any additional information it
     needs to complete the operation you chose.   After you enter any
     necessary information, INTRO3 performs the selected operation and the
     results appear on the screen.   Enter **A** at any sub-menu to return to the
     previous menu level or to exit from INTRO3.

     Try several of the operations to be sure that your monitor is properly
     adjusted and that the cabling is correct.   Be sure to check the color,
     especially if you are using an analog monitor.   Analog RGB cables can
     be connected incorrectly.

11. When you are satisfied that your system is operating as expected, enter
     A to exit INTRO3 and return to the system prompt.

2.7 What To Do If You Have a Problem?

Sometimes things go wrong.   Although you've read though all of the
instructions and followed them to the letter, your TRANSFORMER won't work
right.   Well, don't panic and don't give up yet.   Read through this
checklist of problems and possible solutions first.   Be sure to turn off
the power to all units before you remove or replace cabinets or boards.

PROBLEM: POSSIBLE SOLUTIONS:

No image at all after system power up:

● Be sure the monitor is plugged in and turned on.

● Check that the cables are correctly installed and that all the plugs are correctly seated.

● Be sure that the monitor contrast and brightness adjustments are correct.

● Verify that the jumper is correctly installed at J1.

● Check that System SWITCH 1 is properly configured and that it agrees with the jumper configuration of J1.

● Check that the TRANSFORMER is completely seated in the expansion slot.

System fan doesn't work:

● The system power supply may be overloaded. Each TRANSFORMER board configured for TTL operation draws 3.2 amps. A TRANSFORMER configured for analog operation requires 3.5 amps. If your system power requirements are high, for instance if you are using more that one display adapter and a hard disk sub-system installed in a standard IBM PC, we suggest that you use an IBM PC XT compatible power supply and an external fan.

The IBM PC XT has a 135 watt power supply that allows 11.0 amps in the expansion slots. The IBM PC requires 4.0 amps with 7.0 amps remaining for expansion boards. The IBM PC power supply is rated for 63 watts only.

Screen rolls vertically or horizontally :

● Check that the vertical and horizontal (hold) adjustments on the monitor are correct.

● Verify that the TRANSFORMER's sync type outputs and polarity are correct for your monitor. Compare the TRANSFORMER's sync outputs (see the Setup sheet) with your monitor's input signal requirements.   Some monitors have switches inside the cabinet which allow you to select sync options. Be sure that these are set to agree with the video output of the TRANSFORMER.

PROBLEM: POSSIBLE SOLUTIONS:

Screen rolls vertically or horizontally (cont.):

The default sync output of the TRANSFORMER is compatible with the IBM monochrome display adapter's output.   That is:

Sync on Green
External Composite Sync
+ Horizontal Sync
- Vertical Sync

On the IBM color/graphics adapter, both horizontal and vertical sync are positive. If necessary, you can modify the TRANSFORMER to adjust the video output sync type and polarity to match your monitor's requirements. Chapter 7 explains how to make these modifications.

Trash on the screen at power up:

● Does the pixel clock installed in the TRANSFORMER match your monitor's scan rate.

● If you are using an analog monitor, did you run LDLT.COM? This file loads the color look-up into the TRANSFORMER's RAM. If the look-up table is not loaded, the RAM retains random values from system power up. It does no harm to run LDLT.COM even if you have a TTL or monochrome monitor.

Trash on the screen after initialization:

● The initialization parameters you entered, either from a file or from the keyboard, may have been incorrect for your monitor.   Do   not operate the monitor with   incorrect parameters; the monitor could be damaged.

No image or out of sync image in text plane (IBM emulation):

● Are you using the monitor originally specified for use with the TRANSFORMER.   Although it is possible to use a different monitor than originally specified, the values sent to the MC6845 chip by the TRANSFORMER's ROM will not be correct for your monitor.   The graphics planes generated by the uPD7220 chip should still operate as expected.

PROBLEM: **POSSIBLE SOLUTIONS:**

Unexpected colors:

- If you are using an analog monitor, check that the color outputs of the monitor cable are correctly connected to the monitor's video input connectors.

- If you are using a TTL monitor, be sure that the monitor cable is correctly wired for your monitor.

If you are still not able to pinpoint the problem, there may be a malfunction in your System or in the TRANSFORMER card itself. You may want to try reinstalling your original display adapter card if you have one. Then, consult your dealer or an experienced technician for additional suggestions.

<p align="center">End of Chapter 2</p>

Chapter 4
TRANSFORMER I/O Port Selection and Addressing

The TRANSFORMER is designed for use as an integral part of the IBM PC family and closely compatible computers. Because the TRANSFORMER can be used as a replacement for both the IBM monochrome and color/graphics adapters or can be installed as the second display adapter in a system with an IBM monochrome or color/graphics adapter already installed, the basic I/O port addresses used by the TRANSFORMER are compatible with those of the IBM display adapters.

The initial I/O port address used by the system to talk to the TRANSFORMER is determined by the configuration of a jumper on the TRANSFORMER and by the monitor type setting of SWITCH 1 on the system board. After the system start up, the currently active I/O port address and the graphics display mode can be selected in software. In most cases, when the standard IBM compatible video I/O port addresses are used, selection of the I/O port address visibly affects only the MC6845 display plane.

4.1 TRANSFORMER I/O Port Address Selection

The operating mode of the TRANSFORMER board is determined by the system bus I/O port addresses used to configure the internal registers of the TRANSFORMER's MC6845 and uPD7220 chips. I/O port address selection is dependent on the TRANSFORMER'S base address which is determined by board jumpering.

The base address used for system I/O is provided on the TRANSFORMER as a hardware selectable base address pair. The configuration of board jumper J1 selects the current active base address. This arrangement allows the TRANSFORMER to emulate both IBM monochrome and color/graphics adapters, depending on the configuration of J1.

The standard TRANSFORMER base addresses are the I/O ports 3B0 and 3D0. These addresses are the same as those used by IBM for their monochrome adapter (3B0) and color/graphics adapter (3D0). This address pair allows you to operate the TRANSFORMER immediately with no change to standard software packages configured for the IBM PC.

If required for special applications, alternative I/O base addresses are possible. However, you must physically modify the TRANSFORMER board if you wish to use one of the alternate base address pairs. This modification procedure is described in Chapter 7. If you use an alternate base address pair, you may also need to modify existing software which normally ignores the IBM ROM BIOS and talks directly to the IBM hardware (not an unusual situation).

4.2 Selecting an Active Base Address

From the base address pair, an active base address must be selected for system I/O. This address is determined by the position of a jumper across two pins of header J1. J1 is a four-pin single-row Berg type header located on the component side of the TRANSFORMER board. Figure 4.1 shows the general board location and configuration of J1. Look for J1 below the uPD7220 and MC6845 chips. You will notice that the four pins of J1 are not actually numbered on the TRANSFORMER; however, they are numbered here for clarity.

```
 ┌──────────────────────────┐      ┌──────────────────────────┐
 │      uPD7220             │      │        MC6845            │
 └──────────────────────────┘      └──────────────────────────┘
                            B
                      C │ 1 2 3 4 │ M
                            J1
```
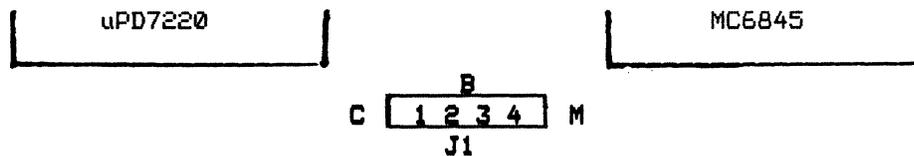
Figure 4.1   TRANSFORMER Board Header J1

Because the jumper configuration determines the actual base address used for system I/O, a jumper block or wire should be installed across the appropriate pins of J1 before the TRANSFORMER is installed in your system.

There are three possible jumper configurations for J1 -- **M** for monochrome, **C** for color, or **B** for both. Assuming that the standard base address pair 3B0 and 3D0 are used:

● If the jumper is installed in position "M" across the two pins on the right (pins 3 and 4), the lower base address of the pair (3B0) is selected. The TRANSFORMER responds to the addresses defined for the monochrome adapter. Select this jumper position if the TRANSFORMER is used in system with another color/graphics board already installed.

● If the jumper is installed in position "C" across the two pins on the left (pins 1 and 2), the higher base address of the pair (3D0) is selected. The TRANSFORMER responds to addresses defined for the color/graphics adapter. Use this jumper position when a separate monochrome board is also installed in the system.

● If a jumper is installed in position "B" across the two middle pins (pins 2 and 3), either of the two possible base addresses (3B0 or 3D0) can be software selected. In this configuration, the TRANSFORMER can respond as either a color/graphics or monochrome adapter depending on the base address used by software to access the MC6845's Mode Register. This is the normal jumper setting.

You must jumper J1 before installing the TRANSFORMER if another display adapter card is also installed in the system. If you intend to operate your system with only the TRANSFORMER board installed, the jumper does not actually need to be installed at J1. Pins 2 and 3 of J1 are grounded and position "B" is really only a "storage" position.

4.3 System Board Address Settings

You must configure the system board to reflect the display adapter type(s)
installed in your system when you install the TRANSFORMER.   Switch settings
on the system board indicate to the system software what type of display
adapter is installed and the default display adapter operating mode at
system start up.

On IBM PC and IBM XT system boards, set SWITCH 1 so that positions 5 and 6
are set to OFF if you have both an IBM monochrome display adapter and a
TRANSFORMER installed in your system.   If you have a installed the
TRANSFORMER in place of the IBM display adapter card, you can select any of
the system board switch setting.   Set both switch positions 5 and 6 to OFF
if you want the system to start up in monochrome display mode.   Set position
5 to ON and position 6 to OFF for 80 column color operation at every system
start.   If you want the TRANSFORMER to start in 40 column mode at boot time,
set position 5 to OFF and position 6 to ON.
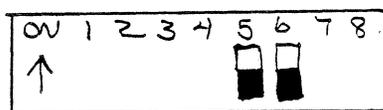
Monitor Adapter Type	SW5	SW6
MONOCHROME only or BOTH (or more than 1 adapter)	OFF	OFF
COLOR (in 80 x 25 mode)	ON	OFF
COLOR (in 40 x 25 mode)	OFF	ON

Figure 4.2 System SWITCH 1 Settings

Be sure to set the system switch to MONOCHROME or BOTH if you have a
monochrome display adapter and a TRANSFORMER installed in the system, or the
monochrome monitor may be damaged.

If you are installing your TRANSFORMER in an IBM PC AT or some other PC
compatible system, these switch settings may not be correct.   Check your
system's technical reference for details regarding proper system board
settings.

4.4 Software Selection of the Board Address and Graphics Display Mode

If the TRANSFORMER is configured to emulate either IBM display adapter or if
you have another display adapter installed in your system, the system will
always start up with the monitor mode selected by the setting of SWITCH 1.
After start up, you can change the TRANSFORMER's display mode by using the

DOS MODE command or by running one of the display mode selection programs
supplied on the TRANSFORMER Utilities diskette.

These files are supplied:

    Executable Files: Assembler Files: Board and Mode:

        MONO.COM   MONO.ASM   Monochrome board – monochrome
        80COLOR.COM   80COLOR.ASM   Color board – 80 x 25 color
        40COLOR.COM   40COLOR.ASM   Color board – 40 x 25 color
        80BLACK.COM   80BLACK.ASM   Color board – 80 x 25 B & W
        40BLACK.COM   40BLACK.ASM   Color board – 40 x 25 B & W
        32X20BW.COM   32X20BW.ASM   Color board – 320 x 200 B & W
        32X20CR.COM   32X20CR.ASM   Color board – 320 x 200 color
        64X20BW.COM   64X20BW.ASM   Color board – 640 x 200 B & W

These files contain all the code necessary to alter the "equipment flag" (a
memory location whose value is set by the ROM BIOS at start up by reading
SWITCH 1) and to change the ROM BIOS routines which control the graphics
display modes.   If the TRANSFORMER is the only board installed and J1 is
jumpered to be selectable, running any of these programs after start up will
select the alternate board address and/or graphics display mode.   If you
have a TRANSFORMER and another display adapter installed, you can use one of
these programs to switch from one board to another without any other system
changes.   Note that if you are using the TRANSFORMER with a monochrome
adapter, the system should be set to always come up in the monochrome.

The .COM files can be run immediately. At any time after start up, enter the
command that corresponds to the display mode you want.   For example if you
set J1 and the System SWITCH 1 to BOTH, the display will come in monochrome
mode.   To change to 80 x 25 color mode, at the system prompt simply enter
the command **80COLOR.**   The monitor is blanked and the system returns in the
new mode. The .ASM files are included as examples of how to prepare your own
programs to alter the equipment flag and change the graphics display modes.

                        End of Chapter 4

Chapter 5
I/O Port Address Registers: Functions, Bit Maps, and Programming

5.1 The TRANSFORMER I/O Ports

The TRANSFORMER's default I/O port addresses are completely compatible with those used by IBM on its display adapter cards. However, the TRANSFORMER uses several additional I/O ports not used by the IBM display adapters. Briefly, several I/O port addresses reserved by IBM but not normally used for addressing the IBM display adapter cards are used with the TRANSFORMER for control of the uPD7220 graphics controller. The TRANSFORMER also uses two additional ports to control the MC6845 through the TRANSFORMER's on board ROM.

The table below names and briefly describes the function of each I/O address assigned to the TRANSFORMER. The function of each register defined here is separately described in detail in the sections that follow.

Table 5.1 TRANSFORMER I/O Port Addresses and Functions

I/O PORT ADDRESS defaults MONO/COLOR			REGISTER FUNCTION
Base Address	3B0	3D0	uPD7220 Status/Parameter Registers
Base +1	3B1	3D1	uPD7220 Data/Command Registers
Base +2	3B2	3D2	uPD7220 LUT / Zoom Register
Base +3	3B3	3D3	Memory Configuration Register
Base +4	3B4	3D4	IBM Index Register
Base +5	3B5	3D5	IBM Data Register
Base +6	3B6	3D6	6845 Index Register
Base +7	3B7	3D7	6845 Data Register
Base +8	3B8	3D8	Mode Select Register
Base +9	3B9	3D9	Color Register
Base +10	3BA	3DA	Status Port
Base +11	3BB	3DB	Clear Light Pen
Base +12	3BC	3DC	Set Light Pen
Base +13	3BD	3DD	Not Used
Base +14	3BE	3DE	Not Used
Base +15	3BF	3DF	Not Used

The default I/O addresses shown in the table are based on the TRANSFORMER's default base address pair. If your TRANSFORMER has been configured to use some other base address pair, each I/O port address can be determined by substituting your board's base addresses for 3B0/3D0 and then adding one (+1) for each succeeding register.

In the default configuration, when the TRANSFORMER is set up to operate in monochrome mode (J1 pins 3 and 4 jumpered), the addresses in the MONO column are used for system I/O. If the TRANSFORMER is set up for color operation (J1 pins 1 and 2 jumpered), the addresses shown in the COLOR column are used. When the TRANSFORMER is set up to operate in BOTH mode (J1 pins 2 and 3 jumpered), the addresses shown in both columns are accessible through software control.

Under software control, the TRANSFORMER's mode of operation and system I/O addressing is determined by the specific address used to access the Mode Select Register. As explained in Chapter 4, you can use the IBM DOS MODE command, one of the mode selection commands included in the TRANSFORMER package, or prepare your own software for mode selection.

The function of each I/O port is described below. Each description includes the bit assignment for that address register and additional information which affects programming of that port.

Remember that the addresses noted in the table above and described in detail here assume that you are using the standard IBM PC compatible I/O port addresses. If your system uses another base address pair, the actual address registers used in your system are incremented from those base addresses. For example, the Configuration Register is normally accessed at I/O port base address + 3, that is at 3B3 and/or 3D3. If you are using the alternate base address pair at 2A0/2C0, the Configuration Register is then located at 2A3 or 2C3.

5.2 Programming the uPD7220 Graphics Display Controller

The NEC uPD7220 Graphics Display Controller (GDC) has a bi-directional interface to the system bus. Two addresses are assigned to the uPD7220 through which the uPD7220's status register and FIFO are accessed. Commands and parameters are written into the uPD7220 and the status register and FIFO are read based on the address selected. Commands are written to the uPD7220 in the form of a command byte followed by a series of parameter bytes, as necessary. The status register contains the 8 register flags which allow coordination of the uPD7220 with the monitor and the flow of data between the FIFO buffer and the system bus.

The LUT/Zoom register is used to control the hardware required for proper timing when the uPD7220 ZOOM command is used to zoom the display. While register does not actually talk to the uPD7220, its value must correspond to the zoom value of the uPD7220 for proper display magnification.

5.3 uPD7220 Status/Parameter Register (I/O Base Address -- '3B0' or '3D0')
     and
     uPD7220 Data/Command Register (I/O Base +1 -- '3B1' or '3D1')

The two ports which control both read and write access to the uPD7220's status registers and FIFO are defined below.

TRANSFORMER I/O Port	7220 Addr	READ MODE		WRITE MODE
3B0 or 3D0	A0	Read Status Register		Write parameter to FIFO
		Status Flag	**Bit Definition**	
		0	Data Ready 0 = no data or CPU now transferring data 1 = byte for CPU read	
		1	FIFO Full 0 = room for at least one byte in FIFO 1 = GDC FIFO full	
		2	FIFO Empty 0 = data in FIFO 1 = FIFO empty, commands and parameters sent	
		3	Drawing in Progress 0 = GDC not drawing now 1 = GDC drawing graphics	
		4	DMA Execute 0 = no DMA in progress 1 = DMA transfer occurring	
		5	Vertical Sync 0 = no vertical sync occurring 1 = vertical sync occuring	
		6	Horizontal Blanking 0 = no horizontal sync 1 = horizontal retrace blanking occurring	
		7	Light Pen Detect 0 = no data to transfer 1 = value ready for read	
3B1 or 3D1	A1	Read data from uPD7220 FIFO		Write command into FIFO

The uPD7220's status register can be read at any time. All other read/write operations through these ports are determined by the state of the bit flags in the status register.   The FIFO data register can be read, and commands and parameters are written into the GDC's FIFO using the same two ports, depending on the state of the status register flags.   The FIFO read and command and parameter write functions of these two ports is described in Appendix C, which contains detailed programming information for the uPD7220.

5.4 uPD7220 LUT / Zoom Register   (I/O Base +2 -- '3B2' or '3D2')

The color look-up table and zoom control or LUT/Zoom I/O port is a write-
only port used for two separate functions.   This port, along with the Mode
Register port and the Color Register port, is used to program the look-up
table located in the output DAC.   This port also controls a hardware circuit
which, when used in conjunction with the uPD7220 commands, allows the
uPD7220 to be zoomed.

5.4.1 uPD7220 Color Look-Up Table (LUT) Function

The digital-to-analog (DAC) converter used in the TRANSFORMER has a 16 word
by 4 bit look-up table for each of the three analog outputs.   During normal
system display operation, the four bits of information received from the
display memory are used as an index of addresses in the look-up table.
These addresses call up previously loaded data which is passed on to the
digital-to-analog converters.

To enable loading the DAC look-up tables, the Mode Register I/O port is
first loaded with the value 40 hex or the binary value of 01x000xx (where x
indicates a doesn't care condition).   This allows the lower four bits of the
color register to pass directly to the look-up table address inputs.

While the look-up table is being loaded, the LUT/Zoom bits are defined as
shown here:

```
    MSB                              LSB

    +---+---+---+---+---+---+---+---+
    | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
    +---+---+---+---+---+---+---+---+
      |   |   |   |   |   |   |   |
      |   |   |   |   |   |   |   +------- Look-up table data
      |   |   |   |   |   |   +----------- Look-up table data
      |   |   |   |   |   +--------------- Look-up table data
      |   |   |   |   +------------------- Look-up table data
      |   |   |   +----------------------- 0 = enable blue
      |   |   +--------------------------- 0 = enable green
      |   +------------------------------- 0 = enable red
      +----------------------------------- 1 = write data
```
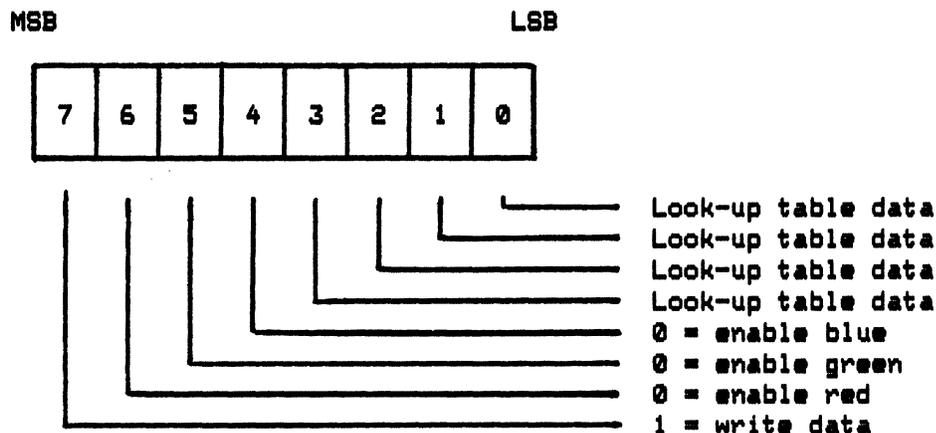
The upper four bits of the LUT/Zoom I/O port are control lines.   The lower
four bits are data lines.

Bit 7 must be low while the color register and the look-up tables are
loaded.   Only one of the enable bits (bits 4, 5 and 6) should be low to
enable one of the look-up tables to be loaded at a time.

After a byte of the color look-up table data has been written to the
LUT/Zoom, the port must be rewritten with the same data except that bit 7

must be high.   The LUT/Zoom port must then be written again with bit 7 low.
This procedure produces a write pulse to the look-up tables while keeping
all other data constant.   This same procedure must be repeated for all 48
data locations (16 locations in each of three look-up tables).

After the look-up tables have been loaded, the top four bits in the LUT/Zoom
port should be set low (0).   This enables the normal reading action of all
three look-up tables.   The lower four bits are no longer used by the look-up
tables and they can be programmed as needed for the zoom function.   The Mode
Register and Color Register should also be reloaded with their correct
values at this time.

Note that this procedure is not required if the TRANSFORMER is operated in
TTL mode, which does not use the DAC look-up tables.

5.4.2 uPD7220 Hardware Zoom Function

The uPD7220 can display on the monitor a zoomed image of the information
contained in its portion of display memory.   The display zoom or
magnification is implemented by pixel replication.   Because the uPD7220 uses
two additional clock cycles for each increase in zoom magnification, the
TRANSFORMER video timing hardware must be controlled to slow the output of
pixels to the monitor to match the zoom factor used by the uPD7220.   The
LUT/Zoom port controls this hardware.

The uPD7220 uses four bits of the its Zoom command byte to control the
display zoom factor.   A zoom factor of zero (0) specifies no zoom. Fifteen
(15) specifies the maximum zoom factor.   The complement of uPD7220 display
zoom value must be loaded into the lower four bits of the LUT/Zoom port.
This means that if the GDC display zoom factor is set to zero (no zoom), the
LUT/Zoom register must be set to '0F'.   Be sure that only the lower four
bits are set and the upper four bits remain low.   If any value is sent to·
the upper four bits, the color look-up table is enabled and the value of the
lower four bits is passed to the DAC.

Except at those times when the look-up table is being loaded, the Zoom
register bits are defined as follows:

LUT/ZOOM Register: GDC Display Zoom Factor:

MSB   LSB

7	6	5	4	3	2	1	0
0	0	0	0	1	1	1	1
0	0	0	0	1	1	1	0
0	0	0	0	1	1	0	1
0	0	0	0	1	1	0	0
0	0	0	0	0	0	0	0

when GDC zoom = 0
when GDC zoom = 1
when GDC zoom = 2
when GDC zoom = 3 ... to
when GDC zoom = 15

5.5 Memory Configuration Register (I/O Base +3 -- '3B3' or '3D3')

The Memory Configuration Register is a write-only register used to control
the TRANSFORMER's display memory organization and operation.

```
       MSB                              LSB

      ┌───┬───┬───┬───┬───┬───┬───┬───┐
      │ 7 │ 6 │ 5 │ 4 │ 3 │ 2 │ 1 │ 0 │
      └───┴───┴───┴───┴───┴───┴───┴───┘
```

Bits 0 - 3 - Write planes:
  1 ———— write plane 0 - blue
  1 ———— write plane 1 - green
  1 ———— write plane 2 - red
  1 ———— write plane 3 - intensity

Bits 4 & 5 - Read Planes:
  0 0 ———— read plane 0 - blue
  0 1 ———— read plane 1 - green
  1 0 ———— read plane 2 - red
  1 1 ———— read plane 3 - intensity

Bits 6 & 7 - Define memory:
  0 0 ———— for 5 planes
  0 1 ———— for 4 planes
  1 0 ———— for 3 planes
  1 1 ———— not defined
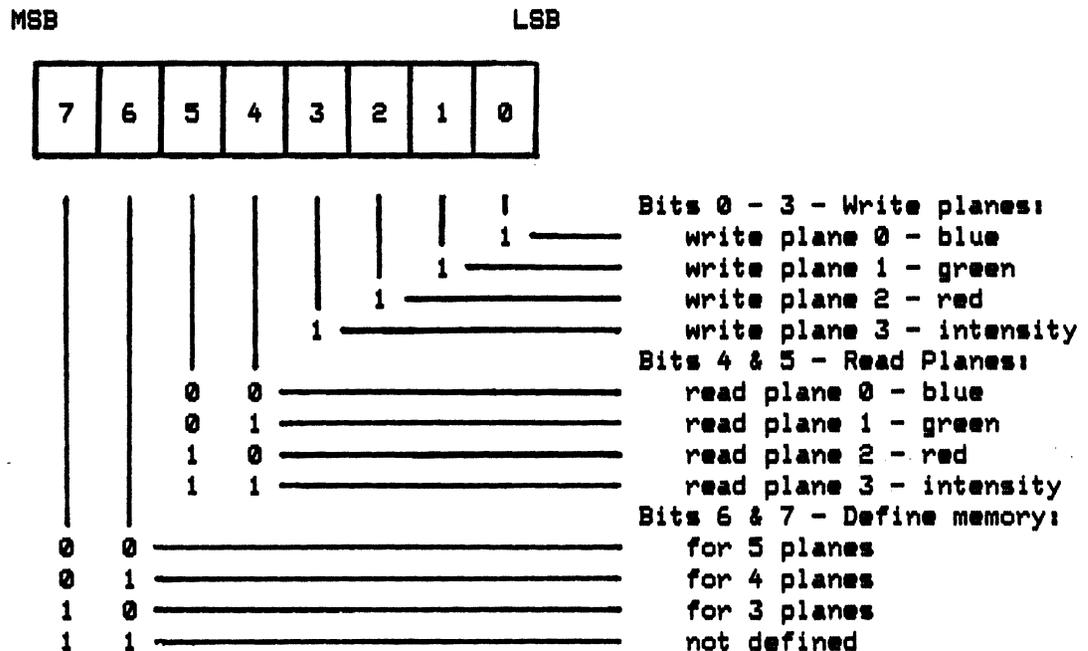
Bits 0 to 3 define which the uPD7220 display planes can be written. Bits 4
and 5 define which uPD7220 display planes can be read by the system.   Bits 6
and 7 define the configuration of uPD7220 display memory.   The color
definition of each plane is meaningful in TTL mode only.   In analog versions
of the TRANSFORMER, the display color of each plane is defined by the color
look-up table values loaded into the DAC.

Bits 0 through 3 of this register are used to define which uPD7220 display
memory planes will be written.   If more than one bit is set high, both the
system and the uPD7220 can write to multiple display planes.   This allows
any color to be written with a single memory access.   These bits are used by
both the system and the uPD7220 to determine which display plane to write.

Bits 4 and 5 of the Configuration register define which memory plane will be
read by the system.   This separate plane read definition is necessary
because multiple plane reads are not possible.   You should also note that no
planes can be read if all four write bits are set to zero.

This plane read bit configuration allows multiple TRANSFORMER cards to be
installed with all uPD7220 planes located at location A0000.   The read bits
are used to define the system accesses to the display memory only.   The
uPD7220 uses its address bits A16 and A17 to read the display memory planes.
The uPD7220 chip, where A16 is the LSB and A17 is the MSB, defines which
memory plane to read using the same logical bit values as bits 4 and 5 of
this register

The TRANSFORMER has 160K bytes of display memory.   This physical memory is
used to store both uPD7220 and MC6845 data.   The size and location of the
logical memory is controlled by the top two bits of the Configuration
Register.   The table below shows how the memory mapping is affected by the
value of bits 6 and 7.

Table 5.2 Logical Memory and uPD7220 Plane Configuration

Base +3 Bits 7 6	Display Resolution	7220 Plane Configuration No. Size Memory Address	Memory Shared By MC6845 At B0000 or B8000
0 0	640 x 400	4 32K A0000 - A7FFF	separate 32k memory plane
0 1	640 x 480	4 40K A0000 - A9FFF	shares 32K with plane 0
1 0	640 x 480	3 48K A4000 - AFFFF	shares 16K with plane 0

The MC6845 can access up to 32K bytes of the TRANSFORMER's total display
memory.   The uPD7220 can use the entire 160K bytes of memory.

The five plane configuration evenly allocates memory for each of five
display planes -- four planes of 32Kbytes each are allocated for the
uPD7220, leaving 32Kbytes of memory free for the MC6845 plane.

In three and four plane memory configurations, the MC6845 and the uPD7220
must actually share physical memory even though the logical memory address
is different.   This means that writing into the MC6845.memory buffer may
modify the data in the uPD7220 display memory. The four plane configuration
allocates 40Kbytes of memory for each of the four uPD7220 display planes.
This enables the uPD7220 to be operated at a higher resolution; but, this
configuration should not be used when the MC6845 is active because the data
written into shared memory locations (the first 32K of plane 0) overwrites
and destroys data already present at that address.

To enable the uPD7220 to display at 640 x 480 pixel resolution with a MC6845
display overlay,   the three plane configuration moves the start location of
the uPD7220 memory away from the normal memory buffer start address of A0000
to A4000.   This mode also physically disables plane 3, the uPD7220 intensity
plane, which limits the uPD7220 graphics display to a total of eight colors
at any one time.   The uPD7220 and MC6845 also share 16Kbytes of memory in
this mode.   However, because the IBM normally only knows about and uses the
first 16Kbytes of memory in its display memory buffers, memory sharing in
this configuration normally presents no problems. However, if the MC6845 is
operated in the 640 x 400 color/graphics mode, the display memory accessed
at B8000 will overwrite the uPD7220 graphics.

5.6 Talking to the MC6845 CRT Controller

IBM assigns two ports for access to the MC6845 CRT controller's internal
registers -- the Index Register at 3B4 or 3D4 and the Data Register at 3B5
or 3D5.   The TRANSFORMER assigns four I/O ports to this function.   Two of
the ports -- the IBM Index Register (Base +4) and the IBM Data Register
(Base +5) -- are the two ports which IBM normally uses to control the
MC6845.   When these ports are used,   the TRANSFORMER's on-board ROM
intercepts and modifies the data before it is sent to the MC6845,   allowing
the IBM-compatible data to be correctly interpreted by the hardware for high
resolution display.   The other two ports -- the 6845 Index Register (Base
+6) and the 6845 Data Register (Base +7) -- allow direct access from the
system bus to the MC6845.

Software written for the IBM PC which talks to an IBM display adapter
through the BIOS uses the I/O ports at Base +4 and Base +5.   Whenever the
TRANSFORMER is used with such software,   the values sent to the TRANSFORMER
hardware are intercepted,   and the values contained in the on-board ROM are
substituted and passed on to the MC6845.   If the software is not "well
behaved" and talks directly to the hardware through another I/O port,   the
information contained in the TRANSFORMER's ROM is not passed to the IBM Data
Register.   The display operating modes are,   as a result,   incorrectly
defined.   The correct values can also be sent directly to the MC6845 data
registers through the second set of I/O ports at Base +6 and Base +7.   These
ports are also useful if you want to initialize the TRANSFORMER using
display values which are different from those contained in the TRANSFORMER's
ROM.

The following table defines the MC6845 data registers and the values that
are normally loaded into those registers as well as the values substituted
by the TRANSFORMER's ROM.   The ROM values shown here are those contained in
the ROM firmware used with standard non-interlaced monitors such as the
Gigatek 1331 and the Princeton Graphics SR-12.   Remember that the values
resident in the ROM firmware are dependent on the type of monitor you
specified.   The MC6845 register initialization values for your monitor type
may not be the same as those shown in the table below.

Table 5.3 Summary of Standard IBM and TRANSFORMER MC6845 Register Values

Addr	Register Number & Type	Units	R/W	Mono		40 x 25 Alpha		80 x 25 Alpha		Graphics	
				IBM	ROM	IBM	ROM	IBM	ROM	IBM	ROM
00	R0 Horizontal Total	Char	W	61	67	38	33	71	67	38	33
01	R1 Horizontal Displayed	Char	W	50	50	28	28	50	50	28	28
02	R2 Horizontal Sync Position	Char	W	52	56	2D	2B	5A	56	2D	2B
03	R3 Horizontal Sync Width	Char	W	0F	06	0A	06	0A	06	0A	06
04	R4 Vertical Total	Char Row	W	19	1F	1F	1F	1F	1F	7F	7F
05	R5 Vertical Total Adjust	Scan Line	W	06	09	06	09	06	09	06	09
06	R6 Vertical Displayed	Char Row	W	19	19	19	19	19	19	64	64
07	R7 Vertical Sync Position	Char Row	W	19	1C	1C	1C	1C	1C	70	70
08	R8 Interlace Mode	See notes	W	02	02	02	02	02	02	02	02
09	R9 Maximum Scan Line Address	Scan Line	W	0D	0F	07	0F	07	0F	01	03
0A	R10 Cursor Start	Scan Line	W	0B	0C	06	0C	06	0C	06	0C
0B	R11 Cursor End	Scan Line	W	0C	0E	07	0E	07	0E	07	0E
0C	R12 Start Address (High)	----	W	00	--	00	--	00	--	00	--
0D	R13 Start Address (Low)	----	W	00	--	00	--	00	--	00	--
0E	R14 Cursor Address (High)	----	R/W	00	--	--	--	--	--	--	--
0F	R15 Cursor Address (Low)	----	R/W	00	--	--	--	--	--	--	--
10	R16 Light Pen (High)	----	R	Rsvd	-	--	--	--	--	--	--
11	R17 Light Pen (Low)	----	R	Rsvd	-	--	--	--	--	--	--

Notes:

1. All register values are shown in hexadecimal notation. The TRANSFORMER does not intercept or change values sent to registers R12 through R17.

2. The MC6845 supports non-interlaced (where R8 value = 0 or 2); interlace sync (value = 1), and interlaced sync and video (value = 3) modes of operation.   IBM display adapters supports only non-interlaced monitors and IBM always specifies that mode with the value of 2 at R8.   The TRANSFORMER firmware also uses that value when operating in non-interlaced mode for IBM compatibility.   The TRANSFORMER also supports use of monitors operating in interlaced mode using the MC6845 interlace sync and video mode.   In this mode, the value of R8 is 3.

5.7 IBM Index Register (I/O Base +4 -- '3B4' or '3D4')

The IBM Index Register port accesses the address register of the MC6845.
This write-only register is used as pointer to direct the transfer of data'
to and from the correct data register. As with IBM display adapter cards,
the five least significant bits of the I/O bus are loaded from the system
into this register with the necessary pointer to the required register.

When a value is detected in this register, the TRANSFORMER ROM intercepts
the pointer value and the IBM Data Register value. The ROM firmware then
compares these values to the ROM register values.   If the register pointed
to is one with which the ROM is concerned and if the value of the data sent
from the system bus is different from the value of that register contained
in the ROM value table,   then the value sent from the system is discarded
and the data value contained in the ROM is loaded into the IBM Data
Register.

5.8 IBM Data Register (I/O Base +5 -- '3B5' or '3D5')

The IBM Data Register is the I/O port which the IBM normally uses to load
data into the MC6845.   The TRANSFORMER modifies the data sent to the MC6845
from this port.   The values loaded in this register are determined by the
values contained in the TRANSFORMER's ROM. Each ROM contains a table of
register values in firmware which is calculated for operation with a
specific monitor.   If the installed ROM isn't configured for the current
display monitor, these values will be incorrect.

5.9 6845 Index Register (I/O Base +6 -- '3B6' or '3D6')

The 6845 Index Register directly accesses the MC6845 address register.   This
write-only register is a pointer which is used to direct the transfer of
data to the correct MC6845 register. Use this port to send data directly to
the MC6845's address register without going through the TRANSFORMER's
interceptor ROM.

5.10 6845 Data Register (I/O Base +7 -- '3B7' or '3D7')

The 6845 Data Register is a write-only I/O port which accesses the MC6845
register pointed to by the 6845 Index Register.   The value to be sent
directly to the MC6845 register pointed to by the 6845 Index Register is
loaded into this port.   This value is transferred to the MC6845 register
without intervention of the TRANSFORMER ROM.

5.11 Mode Select Register (I/O Base +3 -- '3B8' or '3D8')

The Mode Select Register is an 8-bit write-only register   used to control
the video output of the TRANSFORMER.   While the TRANSFORMER uses the same
basic bit definition as IBM display adapters to maintain compatibility with
software written for the IBM adapters, the TRANSFORMER also uses the top two
bits to define the uPD7220 operating mode.

When the jumper at J1 is installed in the "BOTH" position, the operating
mode of the TRANSFORMER is defined by accesses to the Mode Select Register.
If the Mode Select Register is accessed at `3B8', the TRANSFORMER emulates
the IBM monochrome adapter where the MC6845 responds only to IBM monochrome
compatible mode selections.   Accessing the Mode Select Register at `3D8'
causes the TRANSFORMER to emulate the IBM color/graphics adapter, permitting
selection of only those modes which are compatible with the IBM
color/graphics adapter.

This following diagram shows the bit definitions of the Mode Select port:

MSB   LSB

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bit 0
0 = low resolution text 40x25
1 = high resolution text 80x25

Bit 1
0 = alphanumeric (text) mode
1 = graphics mode

Bit 2
0 = color mode if bit 7 = 0
0 = 6845 (color) in foreground
        if bit 7 = 1
1 = b & w mode if bit 7 = 0
1 = 6845 (color) in background
        if bit 7 = 1

Bit 3
0 = disable MC6845 video
1 = enable MC6845 video

Bit 4
0 = 320 pixels horizontal graphics
1 = enable 640 pixels horizontal
        for high resolution graphics

Bit 5
0 = no blink/16 color background
1 = alphanumeric blink enable/8
        color background

Bit 6
0 = load LUT if bit 7 = 0
0 = overlay if bit 7 = 1
1 = 6845 only if bit 7 = 0
1 = window if bit 7 = 1

Bit 7
0 = disable uPD7220
1 = enable uPD7220

The following table is a summary of the video output modes defined for the
TRANSFORMER.

Table 5.4   TRANSFORMER Supported Video Output Modes

```
                        ┌──────────────────── 7 = 7220 enable
                        │ ┌────────────────── 6 = 7220 window or overlay mode
                        │ │ ┌──────────────── 5 = 6845 blink enable
                        │ │ │ ┌────────────── 4 = 6845 640 dot enable
                        │ │ │ │ ┌──────────── 3 = 6845 video enable
                        │ │ │ │ │ ┌────────── 2 = 6845 B & W select
                        │ │ │ │ │ │ ┌──────── 1 = 6845 graphics select
                        │ │ │ │ │ │ │ ┌────── 0 = 6845 high resolution select (dot clock)
   IBM                  │ │ │ │ │ │ │ │
   Adapter              │ │ │ │ │ │ │ │       ↑
   Emulation 7 6 5 4 3 2 1 0  (- Bits        Mode description
```

IBM Adapter Emulation	7	6	5	4	3	2	1	0	(- Bits	Mode description
Either	0	0	x	0	0	0	y	y	(2)	RESET - Screen blanked
Either	0	1	x	0	0	0	y	y	(2)	Load color LUT / COLOR REG passes to DAC
Either	1	0	x	0	0	0	y	y	(2)	7220 only
Mono	0	0	x	x	1	x	x	1		MONO
Mono	1	0	x	0	1	0	0	1		MONO over 7220
Mono	1	0	x	0	1	1	0	1		7220 over MONO
Mono	1	1	x	0	1	1	0	1	(4)	7220 with window to MONO
Color	0	0	x	0	1	1	0	0		40 x 25 B/W Alpha
Color	0	0	x	0	1	0	0	0		40 x 25 Color Alpha
Color	0	0	x	0	1	1	0	1		80 x 25 B/W Alpha
Color	0	0	x	0	1	0	0	1		80 x 25 Color Alpha
Color	0	0	x	0	1	1	1	0		320 x 200 B/W Graphic
Color	0	0	x	0	1	0	1	0		320 x 200 Color Graphic
Color	0	0	x	1	1	x	1	0		640 x 200 Graphic
Color	1	0	x	0	1	0	0	0	(3,5)	40 x 25 over 7220
Color	1	0	x	0	1	0	0	1	(3,5)	80 x 25 over 7220
Color	1	0	x	0	1	0	1	0	(3,5)	320 x 200 over 7220
Color	1	0	x	0	1	1	0	0	(3,5)	7220 over 40 x 25
Color	1	0	x	0	1	1	0	1	(3,5)	7220 over 80 x 25
Color	1	0	x	0	1	1	1	0	(3,5)	7220 over 320 x 200
Color	1	1	x	0	1	1	0	0	(3,4)	7220 with window to 40 x 25
Color	1	1	x	0	1	1	0	1	(3,4)	7220 with window to 80 x 25
Color	1	1	x	0	1	1	1	0	(3,4)	7220 with window to 320 x 200
Color	0	0	x	1	1	x	1	1		IBM 640 x 400
Color	0	0	1	0	0	1	0	1		No load - will not change previous value

Notes:

1.   x = doesn't care or not defined
     y = determined by preceeding and following modes

2.   Bits 0 and 1 should be the same as the preceding and following
     modes initialized.   If the value of these bits is changed, a sync
     procedure must be executed.

3.   If bits 0 and 1 are changed from their previous values, a sync
      procedure must be executed.

4.   A window is defined whenever a pixel with the color index value of
      7 or unintensified white   is written to the uPD7220 display
      memory.   At color index 7, the bit values corresponding to planes
      0, 1, 2 have a value of 1 and plane 3 is equal to 0. Wherever a
      pixel of color index 7 is encountered, the TRANSFORMER hardware
      turns on the MC6845 output.   Note that the window must be defined
      in uPD7220 memory to enable display of the MC6845 plane.   The
      MC6845 plane is not displayed where no window is defined, although
      the contents of the MC6845 memory buffer are undisturbed.   When
      the MC6845 plane is displayed in a window,   the background is
      retained.

5.   In overlay modes, only the contents of the MC6845 foreground is
      displayed; the MC6845 background is suppressed.   The contents of
      the uPD7220 display planes are output to the monitor instead of
      the MC6845 background color.   In effect, whatever is written to
      the uPD7220 display planes becomes the MC6845 background.

      Whenever the uPD7220 is enabled (bit 7 = 1), the MC6845 color
      select function is enabled by the TRANSFORMER hardware.   The
      value of bit 2 then determines which overlay mode is used. If bit
      7 equals 1 and bit 2 equals 0, the MC6845 foreground is displayed
      in foreground.   If both bit 7 and bit 2 equal 1,   the MC6845
      foreground is displayed in background. .

5.12 Color Select Register (I/O Base +9 -- '3B9' or '3D9')

The Color Select Register is an 8-bit write-only register.   The first 6 bits
are used to determine the color of certain aspects of the MC6845 plane
image.   Its actual color control function varies with the video output mode
specified.   This high order bit is used to synchronize the MC6845 and
uPD7220 chips.

In general, this register functions like the IBM color/graphics adapter
Color-Select Register when the TRANSFORMER is operated in IBM compatible
modes.

The following diagram describes the function of each bit in this register.

MSB   LSB

```
┌───┬───┬───┬───┬───┬───┬───┬───┐
│ 7 │ 6 │ 5 │ 4 │ 3 │ 2 │ 1 │ 0 │
└───┴───┴───┴───┴───┴───┴───┴───┘
```

Bit 0 look-up table address
       blue background in 320 x 200
       blue foreground in 620 x 200/400

Bit 1 look-up table address
       green background in 320 x 200
       green foreground in 620 x 200/400

Bit 2 look-up table address
       red background in 320 x 200
       red foreground in 620 x 200/400

Bit 3 look-up table address
       intensity background - 320 x 200
       intensity foreground - 640 x 200/400

Bit 4 foreground color intensity in 320 x 200 mode

Bit 5 polarity of blue plane in 320 x 200 mode

Bit 6 not used

Bit 7 1 = synchronize MC6845 and uPD7220

Bits 0 through 3 of this register control the 320 x 200 graphics mode background, and 640 x 200 or 640 x 400 graphics mode foreground color selection. Because the TRANSFORMER does not display a border in the text modes, these bits have no effect on the colors displayed by the MC6845 when it is operated in color alphanumeric modes. However bits 0 through 3 can be used to determine the color of displayed text when monochrome mode is selected. The TRANSFORMER hardware sets the value of 1010 to produce a default character color of intensified green. Use these bits to change the text display color. The four low order bits also supply the color index address to the DAC look-up table, but only when that device is being programmed.

Bit 4 selects the intensity of the displayed foreground colors of the 320 x 200 graphics mode. If bit 4 is low (0), the foreground palette selected by bit 5 is not displayed in high intensity. If bit 4 is high (1), then the selected palette is intensified.

Bit 5 selects which of the two foreground palettes possible in 320 x 200
graphics mode is used.   The palette selection is determined by the polarity
of the MC6845 blue plane.   If bit 5 is set to 0, there is no blue plane.   If
bit 5 is set to 1, the blue plane is always present. The red and green
elements of the medium resolution color palettes are selected by the high
and low order bits of the 320 x 200 pixel.   If both bits are 0, the
background color selected by bits 0 to 3 are displayed.   When the blue plane
is disabled (bit 5 = 0), this palette of colors is possible in 320 x 200
graphics mode:

C1 (red)	C0 (green)	Color Selected
0	0	Background defined by bits 0 to 3
0	1	Green
1	0	Red
1	1	Brown (or dark yellow)

When the blue plane is enabled (bit 5 = 1), this is the 320 x 200 palette:

| C1 (red)	C0 (green)	Color Selected
0	0	Background defined by bits 0 to 3
0	1	Cyan
1	0	Magenta
1	1	White

Bit 7 is used to synchronize the uPD7220 and MC6845 chips so that video
output of each is directly overlaid.   For synchronous operation, first
initialize both graphic controllers so their horizontal and vertical sync
rates are identical.   Then, bit 7 must be set high (1) through one blanking
interval and then set low (0) at the end of blanking before the next uPD7220
vertical sync.

To determine the correct interval in software, first set bit 7 to 1. Then,
at the end of the uPD7220 vertical sync pulse wait for a period of about 100
horizontal blanking pulses.   Then set bit 7 to 0 before the next uPD7220
vertical sync occurs.   The uPD7220 vertical sync and horizontal blanking
pulse status can be determined by reading the value of uPD7220 status
register bits 5 and 6 respectively.   This delay ensures that the MC6845 is
started at the end of the blanking interval and before the next uPD7220
vertical sync.   Setting the sync bit 7 to 0 permanently enables the MC6845.
If bit 7 is left high, the MC6845 display is permanently turned off.

Bit 6 of this register is not used.

5.13 Status Port (I/O Base +10 -- '3BA' or '3DA')

The Status Port is an 8-bit read-only register which can be used by any program to determine the state of certain TRANSFORMER hardware parameters. The following table defines the bit functions of this port.

MSB   LSB

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

0 = Mono - video display or
        vertical retrace
0 = Color - video display
1 = Mono - horizontal retrace
1 = Color - horizontal or
        vertical retrace

0 = no light pen read possible
1 = light pen read strobe latch
        on

0 = light pen switch off
1 = light pen switch on

0 = Mono - no video display
0 = Color - video display or
        horizontal retrace
1 = Mono - video display
1 = Color - vertical sync

pixel count at pen strobe

The functions of bits 0 and 3 duplicate the functions of the IBM status port bits 0 and 3. The definitions of these bits are dependent on the TRANSFORMER'S operating mode, whether color or monochrome.

Bits 1 and 2 reflect the current light pen status. These bits are meaningful in both monochrome and color/graphics modes of operation. Although the TRANSFORMER supports use of a light pen in monochrome mode, light pens function only with standard persistence monitors such as the IBM color monitor.

When bit 1 is high, you can read the light pen location from the MC6845 registers R10 and R11. This bit is set to 1 when a trigger pulse is detected by the light pen. The bit is set low (0) whenever a system reset occurs or a command to clear the light pen is sent to the Clear Light Pen port at I/O base address +10 (3BB or 3DB). Bit 2 is set high when the light pen switch is open and low when the light pen switch is closed. Note that this bit is not latched and the switch must be polled for continuous update.

Bits 4 through 7 of this port are used to define a pixel count when the light pen strobe occurs. Both the MC6845 and the uPD7220 only define a light pen strobe to the work level. These four bits are read from a four bit counter which counts the pixels as they are displayed by the TRANSFORMER.

5.14 Clear Light Pen (I/O Base +11 -- '3BB' or '3DB')

Any access to this I/O port (either read or write) clears the light pen latch and forces bit 1 of the Status Port to 0.

5.15 Set Light Pen (I/O Base +12 -- '3BC' or '3DC')

Any access to this I/O port (either read or write) sets the light pen latch high, forcing bit 1 of the Status Port to 1. This register can be used in diagnostic routines to simulate the action of an actual light pen.

Note that on the IBM Monochrome display adapter, this port is used as the parallel printer data port. If you are using a parallel printer, access to this port simply strobes the light pen latch.

5.16 Printer Status Port (I/O Base +13 -- '3BD' or '3DD')
and Printer Control Port (I/) Base +14 -- '3BE' or '3DE')
and I/O Port Base +15 -- '3BF' or '3DF'

These ports are not used on the TRANSFORMER.

<div align="center">End of Chapter 5</div>

Chapter 7
Modifying TRANSFORMER Default Outputs

The default output configuration of the TRANSFORMER is predetermined in the
board layout and wiring.   With some simple board modifications, you can
adjust these standard outputs for compatible operation with a variety of
different monitors.   You can also modify the board to change   the
TRANSFORMER's I/O port base addresses.   The following outputs can be
modified:

- Sync on Green (default = ON)
- Composite Sync Polarity (default = NEGATIVE)
- Composite Sync (default = INTERNAL, EXTERNAL for Genlock Option)
- Composite Blanking (default = INTERNAL, EXTERNAL for Genlock Option)
- Horizontal Sync Polarity (default = POSITIVE)
- Vertical Sync Polarity (default = NEGATIVE)
- Color Output (default = TTL)
- Base I/O Address (default = 3B0/3D0 = IBM I/O port base address)

All modifications are made on the back or solder side of the TRANSFORMER
card.   No modifications are required on the component side.   When you look
at the back of the card, the modification locations are all in a vertical
row on the left side of the card above the 62-position I/O connecter.   Each
output modification location is identified on the back of the board by an
upper-case letter and a box outlining the traces and feedthroughs affected.

Generally, a modification is made by cutting the etched trace between two of
the numbered feedthrough points.   A jumper wire is then installed between
one of the original numbered points and the alternate feedthrough point.

> **NOTE:** It is possible to damage the board in making these modifications.
> If you have never made this kind of hardware modification, use
> extreme care when making these changes. Or, ask someone who is
> experienced to make the changes for you.

Figure 7.1 reproduces the layout of the back or solder side of the
TRANSFORMER board where the output modifications are made.   Notice that
there are nine boxes lettered A through G.   Each lettered box corresponds to
one of the outputs that can be modified.   There are two D boxes -- more
about that later.   To change one of the default outputs, find the letter
that corresponds to that output in the table below.   In each case, the
output signal is named first and the relevant board location is identified.
The table lists the possible signal states and then describes any
modifications which may be necessary.
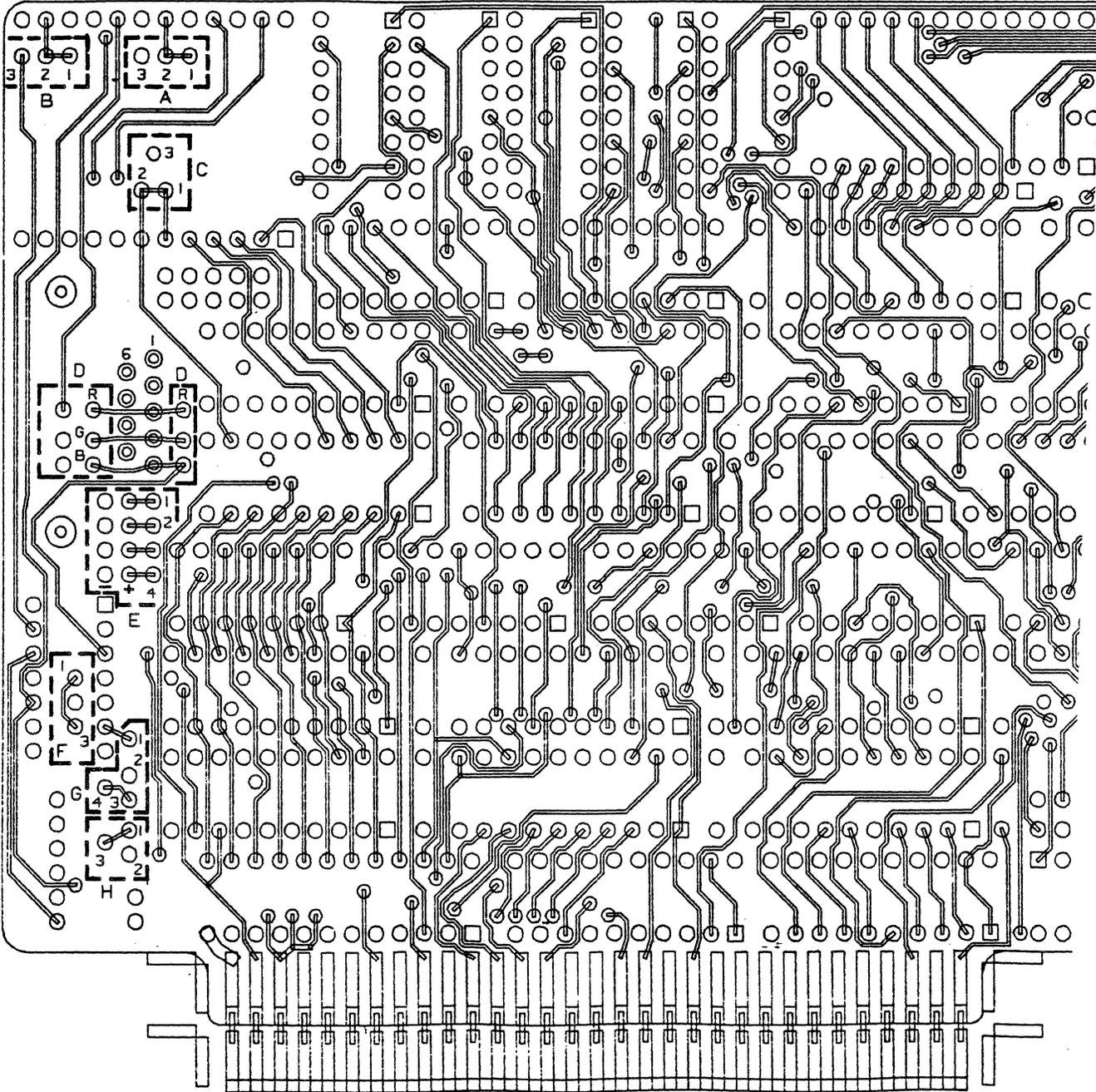
Figure 7.1   TRANSFORMER Board -- Back or Solder Side

How to Make the Modifications

Output To Modify	Board Location	Signal State	Modification Description
Sync On Green	A	ON OFF	DEFAULT 1. Cut trace between 1 and 2 2. Install jumper between 2 and 3
Composite Sync	B	Internal External	DEFAULT 1. Cut trace between 1 and 2 2. Install jumper between 2 and 3
Composite Blanking	C	Internal External	DEFAULT 1. Cut trace between 1 and 2 2. Install jumper between 2 and 3
Color Output	D	TTL Analog	DEFAULT 1. Cut traces between the D box on the right (the one with only 3 feedthroughs) and the 9-pin D-Sub connector pins 3, 4 and 5. 2. Within the D box on the left, install a jumper between each point on the right side of the box (labelled R, G, and B) and the parallel point on the left side of the box.
I/O Port Base Address	E	3B0/3D0	DEFAULT -- Each feedthrough in the the numbered row of four feedthroughs on the right side of E is connected with a board trace to the parallel feedthrough in the middle row (the row marked +).
		Change for Alternate Address	1. Cut the appropriate traces between the right row (numbered) and the middle row (+) of feedthroughs in box E. 2. At locations where traces cut, install a jumper between the feedthrough at the right and the parallel feedthrough at the left side of box E (in the row marked -).

I/O Port Base
    Address (cont.)

A total of sixteen (16) pairs of alternate I/O port base addresses are
possible. The table below shows each possible alternative pair and
lists which jumper positions to modify to select that pair.

Address Pair MONO/Color	Jumper Modified (Change to –)	Resulting Connections 1 2 3 4
020 / 040	1, 2, 3, 4	– – – –
030 / 050	2, 3, 4	+ – – –
0A0 / 0C0	1, 3, 4	– + – –
0B0 / 0D0	3, 4	+ + – –
120 / 140	1, 2, 4	– – + –
130 / 150	2, 4	+ – + –
1A0 / 1C0	1, 4	– + + –
1B0 / 1D0	4	+ + + –
220 / 240	1, 2, 3	– – – +
230 / 250	2, 3	+ – – +
2A0 / 2C0	1, 3	– + – +
2B0 / 2D0	3	+ + – +
320 / 340	1, 2	– – + +
330 / 350	2	+ – + +
3A0 / 3C0	1	– + + +

Alternate I/O port selection changes the address of the IBM-compatible
memory buffers on the TRANSFORMER card.   This can cause problems   with
IBM-compatible software and with system operation.   If you intend to
use an alternate I/O port base address pair, please consult Control
Systems before proceeding with this modification.

Horizontal Sync	F	Positive	DEFAULT
Polarity		Negative	1. Cut trace between 1 and 3
			2. Install jumper between 1 and 2

Composite Sync	G	Negative	DEFAULT
Polarity		Positive	1. Cut trace between 3 and 4
			2. Install jumper between 2 and 4

Vertical Sync	H	Negative	DEFAULT
Polarity		Positive	1. Cut trace between 1 and 3
			2. Install jumper between 2 and 3

The next two illustrations are included to help you understand the
modifications described above.

Figure 7.2 is a simplified schematic showing the output lines configured by the modifications D, F, G and H.
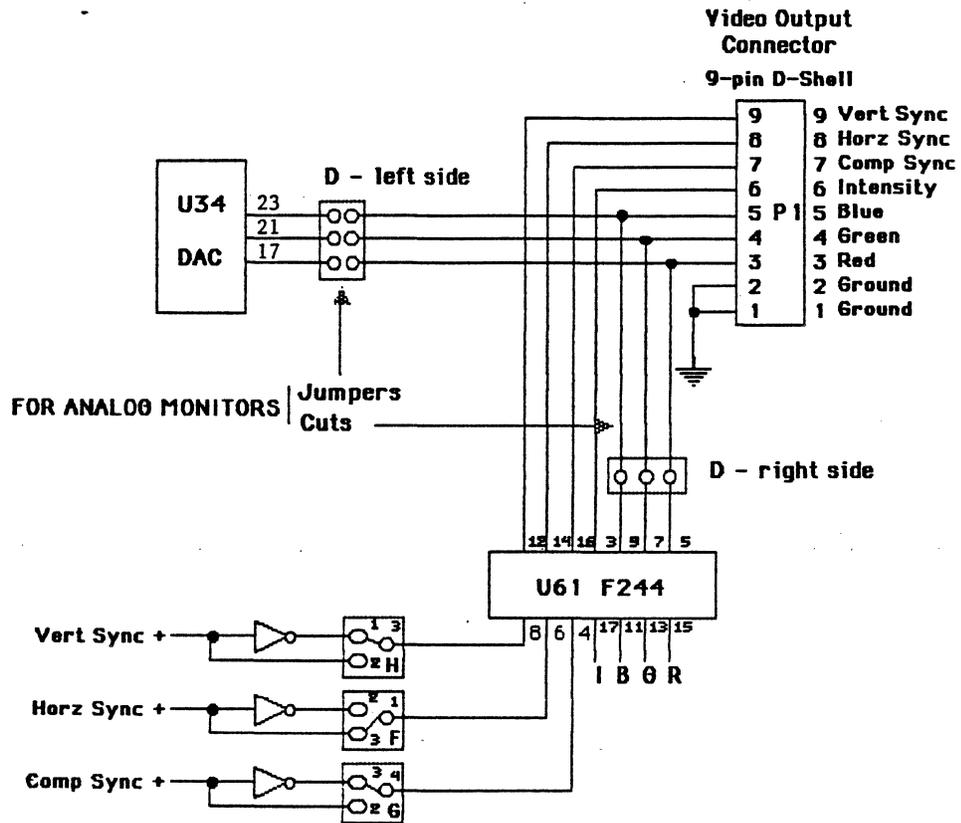
Figure 7.2 Schematic of Output Jumpers to 9-Pin D-Shell Connector

Figure 7.3.a below shows the layout of E for the default I/O port base address pair 3B0 and 3D0.   Figure 7.3.b shows the connections required to change to the alternate I/O address pair 2A0/2C0.

Default
Configured for 3B0/3D0   Configured for 2A0/2C0

Figure 7.3 Jumper E Configuration

End of Chapter 7

Appendix A
Files Distributed in the TRANSFORMER Package

The TRANSFORMER package includes two distribution diskettes which contain the files you need to start using your TRANSFORMER immediately. The first disk, labeled **Artist Transformer Tutor 3**, contains the test program INTRO3 an interactive tutorial program called TUTOR3, sample demonstration files, and parameter files. The other disk shipped with the package, **Artist Transformer Utilities and Graphics Primitives**, contains the ARTLIB library of graphics primitives and other utilities useful for TRANSFORMER operation.

The files distributed with your TRANSFORMER are hardware and language specific. This means that the files on your distribution diskettes are intended for use only with the Artist TRANSFORMER hardware and with the language and compiler you specified when ordering your TRANSFORMER.

In addition to the files listed here, you may find a file called README on your distribution diskettes. This file will contain any new information about changes to the files, implementation notes, comments, and cautions which have not been included in this manual. If you find a README file, be sure to read it first.

We assume that you are using IBM PC DOS version 2.00 or greater, or a compatible version of Microsoft MS-DOS.

A.1 Files Shipped on Both Artist TRANSFORMER Distribution Diskettes

Both distribution disks shipped in the TRANSFORMER package contain a number of monitor parameter files. Each of these files contains the optimum initialization parameters for a particular monitor when the monitor is used with the TRANSFORMER. These ASCII text files are used as is by some programs to initialize the monitor (For example, INTRO3, TUTOR3, and with one minor change, AutoCAD). However, if you simply need a listing of the values, these files can also be printed.

The parameter files shipped on the TRANSFORMER disks are listed below, separated into groups for non-interlaced and interlaced monitors. The 640X400 parameter files are used when the TRANSFORMER is operated with a five plane memory configuration. The 640X480 parameter files are used when the TRANSFORMER is operated in four plane and three plane memory configurations. Note that your disk may contain only some of these files.

Parameter Files for Non-Interlaced Monitors:

- 640X400N.NEC — NEC 1401
- 640X480N.NEC — NEC 1401
- 640X400N.GIG — Gigatek 1331
- 640X480N.GIG — Gigatek 1331
- 640X400N.PGS — Princeton Graphics Systems PGS SR-12
- 640X480N.PGS — Princeton Graphics Systems PGS SR-12
- 640X400N.TAN — Tandy CM-1 (Radio Shack)

Parameter Files for Non-Interlaced Monitors (cont.):

- 640X400N.PRO - IBM Professional Graphics Display
- 640X480N.PRO - IBM Professional Graphics Display
- 640X400N.410 - NEC 1410
- 640X400N.TAX - TAXAN 440
- 640X400N.ELH - Electrohome G09

Parameter Files for Interlaced Monitors:

- 640X400I.IBM - IBM Color Graphics Display
- 640X480I.IBM - IBM Color Graphics Display
- 640X400I.EUR - 50Hz European Display
- 640X480I.EUR - 50Hz European Display
- 640X400I.GEN - GENLOCK Option
- 640X480I.GEN - GENLOCK Option
- 640X400I.ZVM - Zenith ZVM136
- 640X480I.ZVM - Zenith ZVM136

We suggest that you use the parameter file supplied for your monitor.   If
there is no file listed in the directory or supplied on the TRANSFORMER disk
for use with your monitor, you can prepare your own file.   Check your
TRANSFORMER Setup Specification sheet for the correct values.   Use any text
entry program which outputs standard ASCII text.

Here is the format for parameter files:

        Line 1 - Interlace mode (non-interlaced=0, interlaced=1 or 9)
        Line 2 - Pitch (Active words)
        Line 3 - Horizontal Sync (HS - words)
        Line 4 - Vertical Sync (VS - lines)
        Line 5 - Horizontal Front Porch (HFP - words)
        Line 6 - Horizontal Back Porch (HBP - words)
        Line 7 - Vertical Front Porch (VFP - lines)
        Line 8 - Vertical Back Porch (VBP - lines)
        Line 9 - Active Lines (AL - lines)
        Line 10 - Display Length (LEN - lines)
        Line 11 - Maximum X Resolution (MAX X - pixels)
        Line 12 - Maximum Y Resolution (MAX Y - pixels)

If you are using an analog version of the TRANSFORMER and an analog monitor,
you will need to use these files:

- LDLT.COM   - A command file which loads the look-up table on the
                Artist TRANSFORMER with a TTL-like palette.   This file
                must be loaded whenever an analog version of the
                TRANSFORMER is powered up.   A TTL version TRANSFORMER
                does not require that this command be executed.

Although it can be executed at any time, we recommand
that this file be listed as a command in an AUTOEXEC.BAT
file located in the root directory of the disk from
which you load DOS.   Then,   at each system power up or
restart,   DOS automatically runs the LDLT program which
initializes the analog look-up table.

● AUTOEXEC.BAT - A batch file that can be used to load LDLT.COM at each
system power up or restart.   This file contains the
commands LDLT,   DATE,   and TIME; however,   it can be
altered to suit your system requirements.

A.2 Artist TRANSFORMER Tutor 3 Diskette Files

These files are shipped on the **Artist TRANSFORMER Tutor 3** diskette:

● INTRO3.EXE   - An interactive program which demonstrates most of the
basic TRANSFORMER functions.   It is used as a test
program during installation.

● TUTOR3.EXE   - An interactive tutorial program for the TRANSFORMER.
Use TUTOR3 to experiment with the Artlib3 primitives.

● CONFIG.SYS - A text file that DOS loads from the root directory of
the drive from which it was started at each system
start.   This file contains the command **DEVICE=ANSI.SYS**
which tells DOS to load the extended screen and keyboard
device drivers.   The file ANSI.SYS must also be resident
in the same directory at system start up (or specify the
drive and path name).   The ANSI.SYS file is supplied on
your DOS system disks.

Use this file to load ANSI.SYS whenever you intend to
use the **TUTOR3** program.   Unfortunately, ANSI.SYS uses a
value which sets the TRANSFORMER to 80 x 25 text mode
whenever the screen is scrolled while ANSI.SYS is the
console driver.

To avoid this problem,   prepare a separate bootable
system disk and copy the CONFIG.SYS and ANSI.SYS files
to that disk.   Then reset the system (Ctrl-Alt-Del) and
load DOS from that disk whenever you want to use the
TUTOR3 program.   When you exit from TUTOR3,   reboot the
system again using a system disk which does not contain
an ANSI.SYS device driver file.   If you operate the
system with the ANSI.SYS file loaded,   be sure that your
application programs uses only the 80 x 25 text mode or
doesn't scroll the screen.

● HCHAR.DAT   - An 8 x 16 character data file used by INTRO3 and TUTOR3.

● NECCEXP.EXE - An executable demo program for the NEC 1401 monitor.

● GIGCEXP.EXE - An executable demo program for the Gigatek 1331 monitor.

A.3   Artist TRANSFORMER Utilities and Graphics Primitives Diskette Files

The **Artist TRANSFORMER Utilities and Graphics Primitives** diskette contains the following utilities and sample program files.

The following executable command files can be used to change the TRANSFORMER's display between the various IBM compatible display modes.

- ● MONO.COM   - 80 column x 25 line monochrome text mode.
- ● 40BLACK.COM   - 40 column x 25 line black and white text mode.
- ● 40COLOR.COM   - 40 column x 25 line color text mode.
- ● 80BLACK.COM   - 80 column x 25 line black and white text mode.
- ● 80COLOR.COM   - 80 column x 25 line color text mode.
- ● 32X20BW.COM   - 320 x 200 pixel black and white graphics mode.
- ● 32X20CR.COM   - 320 x 200 pixel color graphics mode.
- ● 64X20BW.COM   - 640 x 200 pixel black and white graphics mode.

These assembler files contain the source code of the mode selection command files listed above:

- ● MONO.ASM   - 80 column x 25 line monochrome text mode.
- ● 40BLACK.ASM   - 40 column x 25 line black and white text mode.
- ● 40COLOR.ASM   - 40 column x 25 line color text mode.
- ● 80BLACK.ASM   - 80 column x 25 line black and white text mode.
- ● 80COLOR.ASM   - 80 column x 25 line color text mode.
- ● 32X20BW.ASM   - 320 x 200 pixel black and white graphics mode.
- ● 32X20CR.ASM   - 320 x 200 pixel color graphics mode.
- ● 64X20BW.ASM   - 640 x 200 pixel black and white graphics mode.

Several other sample source files are also included on this diskette:

- ● LDLT.ASM   - The assembler source code of the LDLT.COM executable file.

- ● INITA3.BAS   - An interpretive BASIC file which demonstrates how to initialize the TRANSFORMER for operation at 640 x 400 resolution with a five plane memory configuration.

- ● GENLKA3.BAS   - An interpretive BASIC file that shows how to initialize the TRANSFORMER for operation at 640 x 400 resolution with a five plane memory configuration and **with an Artist GENLOCK option.**

- ● INIT480A.BAS - An interpretive BASIC file that illustrates TRANSFORMER initialization at 640 x 480 resolution with a four plane memory configuration.

- ● HCHAR.DAT   - A data file containing 8 x 16 pixel characters.

Note that the BASIC files contain monitor parameters which may need to be modified to correspond to your display monitor specifications.

The files currently distributed for use with each language compiler
supported by ARTLIB are listed below by compiler.

- Macro Assembler:

        ART3ASM.LIB   - linkable library
        MK3ASM.BAT   - batch file to compile and link programs
        ASM3DEMO.ASM - demonstration program source file
        ASM3DEMO.EXE - demonstration program executable file

- BASIC:

        ART3BAS.LIB   - linkable library
        MK3BAS.BAT   - batch file to compile and link programs
        BAS3GIG.BAS   - demonstration program source file
        BAS3GIG.EXE   - demonstration program executable file

- Computer Innovations C86:

        ART3LCS.LIB   - linkable library for use with small model programs
        ART3LCL.LIB   - linkable library for use with large model programs
        MK3LCS.BAT   - batch file to compile and link small model programs
        MK3LCL.BAT   - batch file to compile and link large model programs
        NECCEXP.C   - demonstration program source file
        NECCEXP.EXE   - demonstration program executable file

- Lattice C:

        ART3LCS.LIB   - linkable library for use with S model programs
        ART3LCP.LIB   - linkable library for use with P model programs
        ART3LCD.LIB   - linkable library for use with D model programs
        ART3LCL.LIB   - linkable library for use with L model programs
        MK3LCS.BAT   - batch file to compile and link S model programs
        MK3LCL.BAT   - batch file to compile and link L model programs
        NECCEXP.C   - demonstration program source file

- FORTRAN:

        ART3FOR.LIB   - linkable library
        MK3FOR.BAT   - batch file to compile and link programs
        FORDEMO3.FOR - demonstration program source file
        FORDEMO3.EXE - demonstration program executable file

- Pascal:

        ART3PAS.LIB   - linkable library
        MK3PAS.BAT   - batch file to compile and link programs
        PAS3DEMO.PAS - demonstration program source file
        PAS3DEMO.EXE - demonstration program executable file

                        End of Appendix A

NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

μ**PD7220/GDC**
μ**PD7220-1/**μ**PD7220-2**
GRAPHICS DISPLAY
CONTROLLER

Description

The μPD7220 Graphics Display Controller (GDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the GDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the GDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the GDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the GDC is ideal for advanced computer graphics applications.

For a more detailed description of the GDC's operation, please refer to the GDC Design Manual.

System Considerations

The GDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the GDC's design, each of the system components is used to the maximum extent through six-level hierarchy of simultaneous tasks. At the lowest level, the GDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the GDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the GDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the GDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

Features

- [ ] Microprocessor Interface
  DMA transfers with 8257- or 8237-type controllers
  FIFO Command Buffering
- [ ] Display Memory Interface
  Up to 256K words of 16 bits
  Read-Modify-Write (RMW) Display Memory cycles in under 800ns
  Dynamic RAM refresh cycles for nonaccessed memory
- [ ] Light Pen Input
- [ ] External video synchronization mode
- [ ] Graphics Mode
  Four megabit, bit-mapped display memory
- [ ] Character Mode
  8K character code and attributes display memory
- [ ] Mixed Graphics and Character Mode
  64K if all characters
  1 megapixel if all graphics
- [ ] Graphics Capabilities
  Figure drawing of lines, arc/circles, rectangles, and graphics characters in 800ns per pixel
  Display 1024-by-1024 pixels with 4 planes of color or grayscale
  Two independently scrollable areas
- [ ] Character Capabilities
  Auto cursor advance
  Four independently scrollable areas
  Programmable cursor height
  Characters per row: up to 256
  Character rows per screen: up to 100
- [ ] Video Display Format
  Zoom magnification factors of 1 to 16
  Panning
  Command-settable video raster parameters
- [ ] Technology
  Single +5 volt, NMOS, 40-pin DIP
- [ ] DMA Capability
  Bytes or word transfers
  4 clock periods per byte transferred

Pin Configuration

```
2xWCLK ⊏ 1        40 ⊐ Vcc
  DBIN ⊏ 2        39 ⊐ A17
 HSYNC ⊏ 3        38 ⊐ A16
V/EXT SYNC ⊏ 4    37 ⊐ AD15
 BLANK ⊏ 5  μPD   36 ⊐ AD14
   ALE ⊏ 6  7220  35 ⊐ AD13
   DRQ ⊏ 7        34 ⊐ AD12
  DACK ⊏ 8        33 ⊐ AD11
    RD ⊏ 9        32 ⊐ AD10
    WR ⊏ 10       31 ⊐ AD9
    A0 ⊏ 11       30 ⊐ AD8
   DB0 ⊏ 12       29 ⊐ AD7
   DB1 ⊏ 13       28 ⊐ AD6
   DB2 ⊏ 14       27 ⊐ AD5
   DB3 ⊏ 15       26 ⊐ AD4
   DB4 ⊏ 16       25 ⊐ AD3
   DB5 ⊏ 17       24 ⊐ AD2
   DB6 ⊏ 18       23 ⊐ AD1
   DB7 ⊏ 19       22 ⊐ AD0
   GND ⊏ 20       21 ⊐ LPEN
```
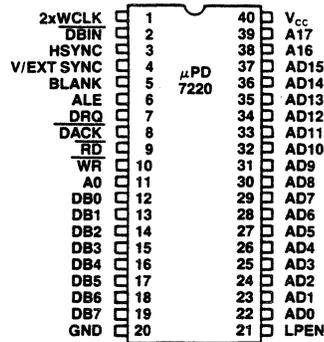
Pin Identification

Pin No.	Symbol	Direction	Function
1	2xWCLK	IN	Clock Input
2	DBIN	OUT	Display Memory Read Input Flag
3	HSYNC	OUT	Horizontal Video Sync Output
4	V/EXT SYNC	IN/OUT	Vertical Video Sync Output or External VSYNC Input
5	BLANK	OUT	CRT Blanking Output
6	ALE (RAS)	OUT	Address Latch Enable Output
7	DRQ	OUT	DMA Request Output
8	DACK	IN	DMA Acknowledge Input
9	RD	IN	Read Strobe Input for Microprocessor Interface
10	WR	IN	Write Strobe Input for Microprocessor Interface
11	A0	IN	Address Select Input for Microprocessor Interface
12-19	DB0 to 7	IN/OUT	Bidirectional Data Bus to Host Microprocessor
20	GND	—	Ground
21	LPEN	IN	Light Pen Detect Input
22-34	AD0 to 12	IN/OUT	Address and Data Lines to Display Memory
35-37	AD13 to 15	IN/OUT	Utilization Varies with Mode of Operation
38	A16	OUT	Utilization Varies with Mode of Operation
39	A17	OUT	Utilization Varies with Mode of Operation
40	Vcc	—	+ 5V ± 10%

Character Mode Pin Utilization

Pin No.	Name	Direction	Function
35-37	AD13 to 15	OUT	Line Counter Bits 0 to 2 Outputs
38	A16	OUT	Line Counter Bit 3 Output
39	A17	OUT	Cursor Output and Line Counter Bit 4*

Mixed Mode Pin Utilization

| Pin No.	Name	Direction	Function
35-37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Attribute Blink and Clear Line Counter* Output
39	A17	OUT	Cursor and Bit-Map Area* Flag Output

*Output 10 clock cycles after trailing edge of HSYNC. See figure for timing example.

Graphics Mode Pin Utilization

Pin No.	Name	Direction	Function
35-37	AD13 to 15	IN/OUT	Address and Data Bits 13 to 15
38	A16	OUT	Address Bit 16 Output
39	A17	OUT	Address Bit 17 Output

Block Diagram
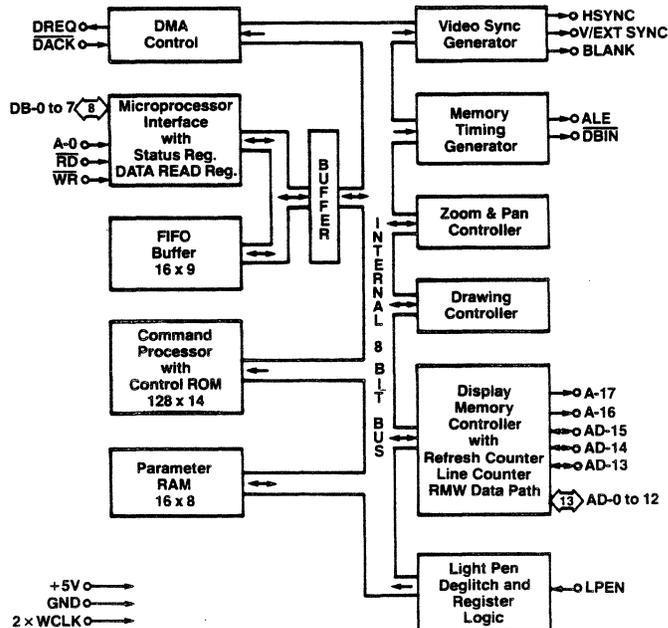
GDC Components

Microprocessor Bus Interface
Control of the GDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal GDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor
The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destinations within the GDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control
The DMA control circuitry in the GDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a μPD8257 or μPD8237 DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM
The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator
Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple GDCs.

Memory Timing Generator
The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the GDC's ALE and DBIN outputs.

Zoom & Pan Controller
Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independently of the other display areas.

Drawing Controller
The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing controller needs no further assistance to complete the figure drawing.

Display Memory Controller
The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMs. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher
Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address.

Programmer's View of GDC
The GDC occupies two addresses on the system microprocessor bus through which the GDC's status register and FIFO are accessed. Commands and parameters are written into the GDC's FIFO and are differentiated based on address bit A0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	Status Register	Parameter Into FIFO
1	FIFO Read	Command Into FIFO
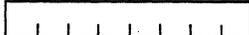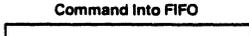
GDC Microprocessor Bus Interface Registers

Commands to the GDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacks the parameters, loads them into the appropriate registers within the GDC, and initiates the required operations.

The commands available in the GDC can be organized into five categories as described in the following section.

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GDC Command Summary

Video Control Commands
1. RESET   Resets the GDC to its idle state.
2. SYNC   Specifies the video display format.
3. VSYNC   Selects master or slave video synchronization mode.
4. CCHAR   Specifies the cursor and character row heights.

Display Control Commands
1. START   Ends Idle mode and unblanks the display.
2. BCTRL   Controls the blanking and unblanking of the display.
3. ZOOM   Specifies zoom factors for the display and graphics characters writing.
4. CURS   Sets the position of the cursor in display memory.
5. PRAM   Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
6. PITCH   Specifies the width of the X dimension of display memory.

Drawing Control Commands
1. WDAT   Writes data words or bytes into display memory.
2. MASK   Sets the mask register contents.
3. FIGS   Specifies the parameters for the drawing controller.
4. FIGD   Draws the figure as specified above.
5. GCHRD   Draws the graphics character into display memory.

Data Read Commands
1. RDAT: Reads data words or bytes from display memory.
2. CURD: Reads the cursor position.
3. LPRD: Reads the light pen address.

DMA Control Commands
1. DMAR   Requests a DMA read transfer.
2. DMAW   Requests a DMA write transfer.

Status Register Flags
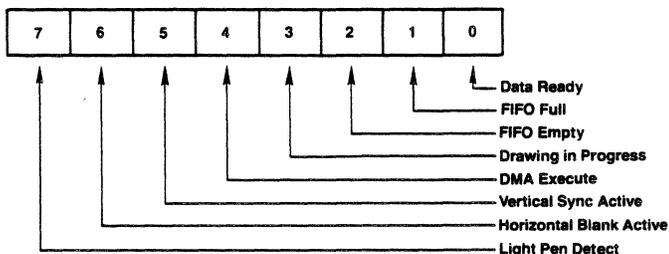
Status Register (SR)

SR-7: Light Pen Detect
When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blanking Active
A 1 value for this flag signifies that horizontal retrace blanking is currently underway.

SR-5: Vertical Sync
Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute
This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress
While the GDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty
This bit and the FIFO Full flag coordinate system microprocessor accesses with the GDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the GDC have been interpreted.

SR-1: FIFO Full
A 1 at this flag indicates a full FIFO in the GDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the GDC.

SR-0: Data Ready
When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation & Command Protocol
The first-in, first-out buffer (FIFO) in the GDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the GDC's command set. The host microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the GDC requires differentiation of the first byte of a command sequence from the succeeding bytes. The first byte contains the operation code and the remaining bytes carry parameters. Writing into the GDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the GDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the GDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the GDC always put the FIFO into write mode if it wasn't in it already.

If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require a GDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the GDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the GDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the GDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic Unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT parameters or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic Unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic Unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with 1s in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a four-bit dAD field to specify the dot address. The command processor converts this parameter into the one-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

The Logic Unit combines the data read from display memory, the Pattern Register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the Pattern Register data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The GDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 5MHz, this is equal to 800ns. During the RMW cycle the GDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the GDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the GDC's internal RMW logic.

During the drawing process, the GDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The GDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.
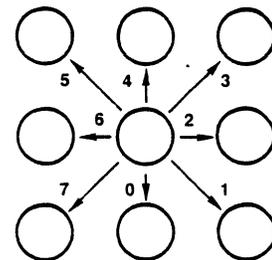
Drawing Directions

Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left.

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The table below summarizes these operations for each direction.

Dir	Operations to Address the Next Pixel
000	EAD + P → EAD
001	EAD + P → EAD dAD (MSB) = 1:EAD + 1 → EAD dAD → LR
010	dAD (MSB) = 1:EAD + 1 → EAD dAD → LR
011	EAD − P → EAD dAD (MSB) = 1:EAD + 1 → EAD dAD → LR
100	EAD − P → EAD
101	EAD − P → EAD dAD (LSB) = 1:EAD − 1 → EAD dAD → RR
110	dAD (LSB) = 1:EAD − 1 → EAD dAD → RR
111	EAD + P → EAD dAD (LSB) = 1:EAD − 1 → EAD dAD → RR

Where P = Pitch, LR = Left Rotate, RR = Right Rotate,
EAD = Execute Word Address, and
dAD = Dot Address stored in the Mask Register.

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to effect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:

Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45 degrees in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the GDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45 degree diagonal path by pixels.

Drawing Parameters

In preparation for graphics figure drawing, the GDC's Drawing Processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the GDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The GDC Drawing Controller coordinates the RMW circuitry and address registers to draw the specifed figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the GDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

Drawing Type	DC	D	D2	D1	DM
Initial Value*	0	8	8	−1	−1
Line	$\|\Delta I\|$	$2\|\Delta D\| - \|\Delta I\|$	$2(\|\Delta D\| - \|\Delta I\|)$	$2\|\Delta D\|$	−
Arc**	$r\sin\phi$	$r−1$	$2(r−1)$	−1	$r\sin\theta\downarrow$
Rectangle	3	$A−1$	$B−1$	−1	$A−1$
Area Fill	$B−1$	A	A	−	−
Graphic Character***	$B−1$	A	A	−	−
Write Data	$W−1$	−	−	−	−
DMAW	$D−1$	$C−1$	−	−	−
DMAR	$D−1$	$C−2$	$(C−2)/2†$	−	−
Read Data	W	−	−	−	−

*Initial values for the various parameters remain as each drawing process ends.
**Circles are drawn with 8 arcs, each of which span 45°, so that sin ϕ = 1/$\sqrt{2}$ and sin θ = 0.
***Graphic characters are a special case of bit-map area filling in which B and A ≤ 8. If A = 8 there is no need to load D and D2.
Where:
−1 = all ONES value.
All numbers are shown in base 10 for convenience. The GDC accepts base 2 numbers (2s complement notation where appropriate).
− = No parameter bytes sent to GDC for this parameter.
ΔI = The larger Δx or Δy.
ΔD = The smaller Δx or Δy.
r = Radius of curvature, in pixels.
ϕ = Angle from major axis to end of the arc. ϕ ≤ 45°.
θ = Angle from major axis to start of the arc. θ ≤ 45°.
↑ = Round up to the next higher integer.
↓ = Round down to the next lower integer.
A = Number of pixels in the initially specified direction.
B = Number of pixels in the direction at right angles to the initially specified direction.
W = Number of words to be accessed.
C = Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected.)
D = Number of words to be accessed in the direction at right angles to the initially specified direction.
DC = Drawing count parameter which is one less than the number of RMW cycles to be executed.
DM = Dots masked from drawing during arc drawing.
† = Needed only for word reads.

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Graphics Character Drawing

Graphics characters can be drawn into display memory pixel-by-pixel. The up to 8-by-8 character display is loaded into the GDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the zoom command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command. Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The GDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is less than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the GDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mozaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8.)

Parameter RAM Contents: RAM Address RA 0 to 15

The parameters stored in the parameter RAM, PRAM, are available for the GDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the GDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern Register to allow the GDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing locations 8 through 15 are referenced for the pattern or character to be drawn.

Details of the bit assignments are shown for the various modes of operation.

Character Mode

Display Partition Area 1 starting address with low & high significance fields (word address)

Length of Display Partition 1 (line count) with high and low significance fields

A Wide Display cycle width of two words per memory cycle is selected for this display area if this bit is set to a 1. The display address counter is then incremented by 2 for each display scan cycle. Other memory cycle types are not influenced.

Display Partition 2 starting address and length

Display Partition 3 starting address and length

Display Partition 4 starting address and length

Graphics and Mixed Graphics and Character Modes

Reg				Field
RA-0		SAD1$_L$		Display Partition Area 1 starting address with low, middle, and high significance fields (word address)
1		SAD1$_M$		
2	LEN1$_L$	0 0	SAD1$_H$	
3	WD1 IM	LEN1$_H$		Length of Display Partition Area 1 with low and high significance fields (line count)

In mixed mode, a 1 indicates an image or graphics area, and a 0 indicates a character area. In graphics mode this bit must be 0. When 1, the DAD is incremented every other display cycle.

Reg				Field
RA-4		SAD2$_L$		Display Partition Area 2 starting address and length with image bit as in area 1
5		SAD2$_M$		
6	LEN2$_L$	0 0	SAD2$_H$	
7	WD2 IM	LEN2$_H$		

Reg				Field
RA-8	PTN$_L$	or	GCHR8	Pattern of 16 bits used for figure drawing to pattern dotted, dashed, etc. lines
9	PTN$_H$	or	GCHR7	
RA-10			GCHR6	
11			GCHR5	
12			GCHR4	Graphics character bytes to be moved into display memory with graphics character drawing
13			GCHR3	
14			GCHR2	
15			GCHR1	

Command Bytes Summary

Command	b7	b6	b5	b4	b3	b2	b1	b0
RESET	0	0	0	0	0	0	0	0
SYNC	0	0	0	0	1	1	1	DE
VSYNC	0	1	1	0	1	1	1	M
CCHAR	0	1	0	0	1	0	1	1
START	0	1	1	0	1	0	1	1
BCTRL	0	0	0	0	1	1	0	DE
ZOOM	0	1	0	0	0	1	1	0
CURS	0	1	0	0	1	0	0	1
PRAM	0	1	1	1	SA			
PITCH	0	1	0	0	0	1	1	1
WDAT	0	0	1	TYPE		0	MOD	
MASK	0	1	0	0	1	0	1	0
FIGS	0	1	0	0	1	1	0	0
FIGD	0	1	1	0	1	1	0	0
GCHRD	0	1	1	0	1	0	0	0
RDAT	1	0	1	TYPE		0	MOD	
CURD	1	1	1	0	0	0	0	0
LPRD	1	1	0	0	0	0	0	0
DMAR	1	0	1	TYPE		1	MOD	
DMAW	0	0	1	TYPE		1	MOD	

Video Control Commands

Reset

RESET: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
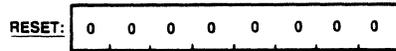
Blank the display, enter Idle mode, and initialize within the GDC:
— FIFO
— Command Processor
— Internal Counters

This command can be executed at any time and does not modify any of the parameters already loaded into the GDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below. Idle mode is exited with the START command.

P1 | 0 | 0 | C | F | I | D | G | S | ← Mode of Operation select bits See below

P2 | , | AW | ← Active Display Words per line − 2 Must be even number with bit 0 = 0

P3 | VS$_L$ | HS |
← Horizontal Sync Width − 1
← Vertical Sync Width, low bits

P4 | HFP | VS$_H$ | ← Vertical Sync Width, high bits
← Horizontal Front Porch Width − 1

P5 | 0 | 0 | HBP | ← Horizontal Back Porch Width − 1

P6 | 0 | 0 | VFP | ← Vertical Front Porch Width

P7 | AL$_L$ | ← Active Display Lines per Video Field, low bits

P8 | VBP | AL$_H$ | ← Active Display Lines per Video Field, high bits
← Vertical Back Porch Width

In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any. The number of active words per line must be an even number from 2 to 256. An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field for vertical parameters. All horizontal widths are counted in display words. All vertical intervals are counted in lines.

Horizontal Back Porch Constraints

1. In general:
   HBP ⩾ 3 Display Word Cycles (6 clock cycles).
2. If the IMAGE or WD modes change within one video field:
   HBP ⩾ 5 Display Word Cycles (10 clock cycles).
3. If interlace or mixed mode is used:
   HBP ⩾ 5 Display Word Cycles (10 clock cycles).

Horizontal Front Porch Constraints

1. If the display ZOOM function is used at other than 1X:
   HFP ⩾ 2 Display Word Cycles (4 clock cycles).
2. If the GDC is used in the video sync Slave mode:
   HFP ⩾ 4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP ⩾ 6 Display Word Cycles (12 clock cycles).
4. If interlace mode is used:
   HFP ⩾ 3 Display Word Cycles (6 clock cycles).

Horizontal SYNC Constraints

1. If Interlaced display mode is used:
   HS ⩾ 5 Display Word Cycles (10 clock cycles).

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed Graphics & Character
0	1	Graphics Mode
1	0	Character Mode
1	1	Invalid

I	S	Video Framing
0	0	Noninterlaced
0	1	Invalid
1	0	Interlaced Repeat Field for Character Displays
1	1	Interlaced

Repeat Field Framing: 2 Field Sequence with ½ line offset between otherwise identical fields.

Interlaced Framing: 2 Field Sequence with ½ line offset. Each field displays alternate lines.

Noninterlaced Framing: 1 field brings all of the information to the screen.

Total scanned lines in interlace mode is odd. The sum of VFP + VS + VBP + AL should equal one less than the desired odd number of lines.

D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — STATIC RAM
1	Refresh — Dynamic RAM

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.

SYNC Format Specify

SYNC: | 0 | 0 | 0 | 0 | 1 | 1 | 1 | DE |

└─ The display is enabled by a 1, and blanked by a 0.

P1: | 0 | 0 | C | F | I | D | G | S | ◄─ Mode of Operation select bits See below

P2: | AW | ◄─ Active Display Words per line − 2   Must be even number with bit 0 − 0

P3: | VS₁ | HS |

└─ Horizontal Sync Width − 1
└─ Vertical Sync Width, low bits

P4: | HFP | VS_H | ◄─ Vertical Sync Width, high bits

└─ Horizontal Front Porch Width − 1

P5: | 0 | 0 | HBP | ◄─ Horizontal Back Porch Width − 1

P6: | 0 | 0 | VFP | ◄─ Vertical Front Porch Width

P7: | AL₁ | ◄─ Active Display Lines per Video Field,   low bits

P8: | VBP | AL_H | ◄─ Active Display Lines per Video Field, high bits

└─ Vertical Back Porch Width

This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The GDC is not reset nor does it enter idle mode.

Vertical Sync Mode

VSYNC: | 0 | 1 | 1 | 0 | 1 | 1 | 1 | M |

└─ 0 — Accept External Vertical Sync — Slave Mode

1 — Generate & Output Vertical Sync — Master Mode
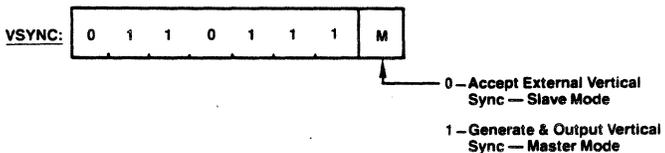
When using two or more GDCs to contribute to one image, one GDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all GDCs are connected together.

A few considerations should be observed when synchronizing two or more GDCs to generate overlayed video via the VSYNC INPUT/OUTPUT pin. As mentioned above, the Horizontal Front Porch (HFP) must be 4 or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave GDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave GDC to complete the operation before the start of the HSYNC interval.

Once the GDCs are initialized and set up as Master and Slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the Master GDC and

wait until after one or more VSYNC pulses have been generated before the display process is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated for the Slaves to synchronize to.

Cursor & Character Characteristics

CCHAR: | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |

P1: | DC | 0 | 0 | LR | ◄─ Lines per character row − 1

└─ Display Cursor if 1

P2: | BR_L | SC | CTOP | ◄─ Cursor Top line number in the row

└─ 0 — Blinking Cursor / 1 — Steady Cursor
└─ Blink Rate, lower bits

P3: | CBOT | BR_U | ◄─ Blink Rate, upper bits

└─ Cursor Bottom line number in the row CBOT < LR
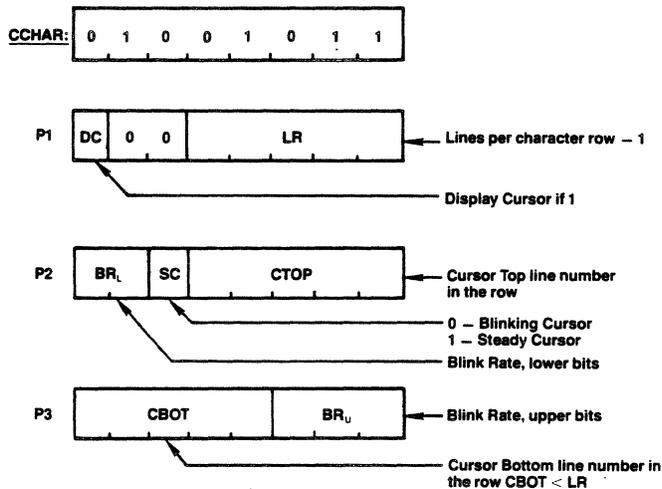
In graphics mode, LR should be set to 0. The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always ½ the cursor rate but with a ¾ on-¼ off duty cycle. All three parameter bytes must be output for interlace displays, regardless of mode. For interlace displays in graphics mode, the parameter $BR_L = 3$.

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Display Control Commands

Start Display & End Idle Mode

START: | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
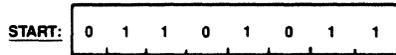
Display Blanking Control

BCTRL: | 0 | 0 | 0 | 0 | 1 | 1 | 0 | DE | ← The display is enabled by a 1, and blanked by a 0.
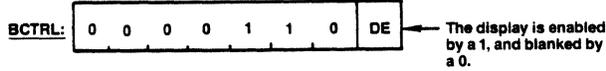
Zoom Factors Specify

ZOOM: | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

P1: | DISP | GCHR | ← Zoom factor for graphics character writing and area filling
← Display zoom factor
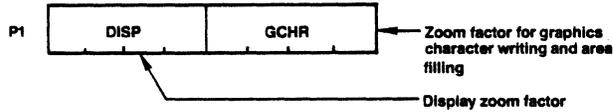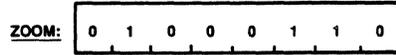
Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

Cursor Position Specify

CURS: | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |

P1: | EAD | ← Execute Word Address, low byte

P2: | EAD | ← Execute Word Address, middle byte

P3: | dAD | 0 | 0 | EAD | ← (Graphics Mode only)
← Word Address, top bits
← Dot Address within the word
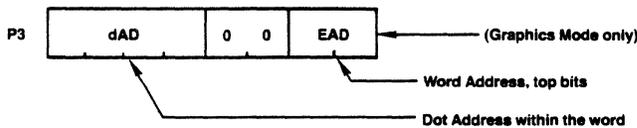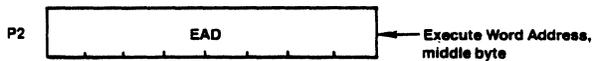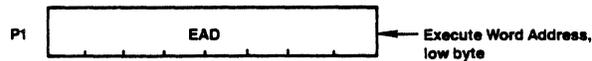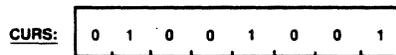
In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address. In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

Parameter RAM Load

PRAM: | 0 | 1 | 1 | SA | ← Starting Address in parameter RAM

P₁ ⋮ Pₙ | | ← 1 to 16 bytes to be loaded into the parameter RAM starting at the RAM address specified by SA
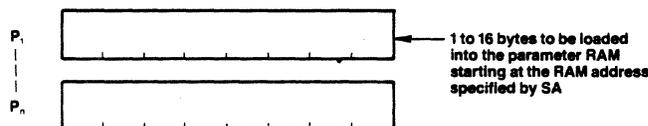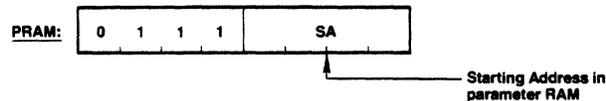
From the starting address, SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is terminated by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

Pitch Specification

PITCH: | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

P1: | P | ← Number of word addresses in display memory in the horizontal direction
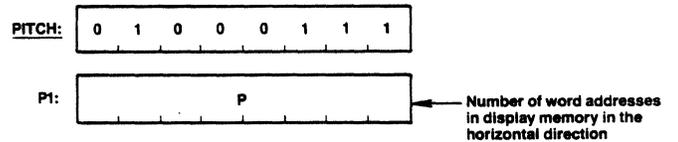
This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active words per line" parameter, which specifies the width of the raster-scan display, also sets the Pitch of the display memory. Note that the AW value is two less than the display window width. The PITCH command must be used to set the proper memory width larger than the window width.

Drawing Control Commands

Write Data into Display Memory

WDAT: | 0 | 0 | 1 | TYPE | 0 | MOD |
← RMW Memory cycle Logical Operation:
0 0 ← REPLACE with Pattern
0 1 ← COMPLEMENT
1 0 ← RESET to zero
1 1 ← SET to 1
← Data Transfer Type:
0 0 ← Word, Low then High byte
1 0 ← Low Byte of the Word
1 1 ← High Byte of the Word
0 1 ← Invalid

P1: | WORD_L OR BYTE | ← Word Low Data Byte or Single Byte Data value

P2 etc.: | WORD_H | ← Word transfer only: High Data Byte
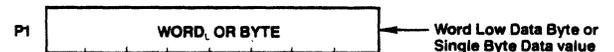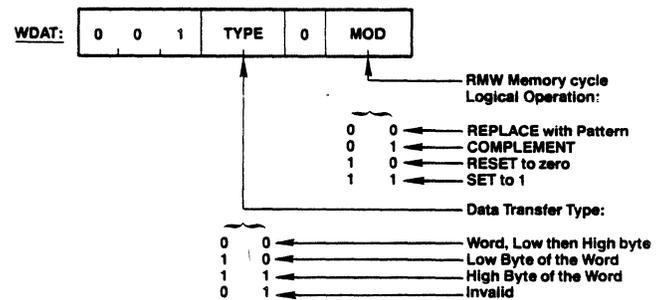
Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into Video Memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires

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parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceded by a FIGS command and its parameters. Only the first three parameters need be given following the FIGS opcode, to set up the type of drawing, the DIR direction, and the DC value. The DC parameter +1 will be the number of RMW cycles done by the GDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed per set of parameters.

Mask Register Load

MASK: | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |

P1 | M_L | Low significance byte

P2 | M_H | High significance byte
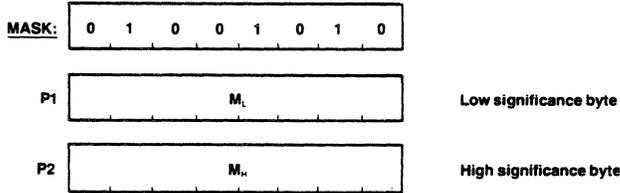
This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

The Mask register is loaded both by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16 bits can be individually one or zero, under program control. The CURS command on the other hand, puts a "1 of 16" pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing operations using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output. The Mask register should be set to all "ONES" for any "word-at-a-time" operation.

Figure Drawing Parameters Specify

FIGS: | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |

P1 | SL | R | A | GC | L | DIR | ← Drawing Direction Base

Figure Type Select Bits:
— Line (Vector)
— Graphics Character
— Arc/Circle
— Rectangle
— Slanted Graphics Character

P2 | DC_L | ← DC Drawing Parameter

P3 | 0 | GD | DC_H |
— Graphics Drawing flag for use in Mixed Graphics and Character Mode

P4 | D_L | ← D Drawing Parameter

P5 | 0 | 0 | D_H |

P6 | $D2_L$ | ← D2 Drawing Parameter

P7 | 0 | 0 | $D2_H$ |

P8 | $D1_L$ | ← D1 Drawing Parameter

P9 | 0 | 0 | $D1_H$ |

P10 | DM_L | ← DM Drawing Parameter

P11 | 0 | 0 | DM_H | ← The parameters take on different interpretations for different figure types.

Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing, Individual Dot Drawing, DMA, WDAT, and RDAT
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area filling with graphics character pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted Graphics Character Drawing and Slanted Area Filling

Only these bit combinations assure correct drawing operation.

Figure Draw Start

FIGD: | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
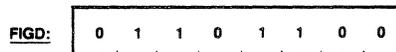
On execution of this instruction, the GDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

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Graphics Character Draw and Area Filling Start

GCHRD: | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
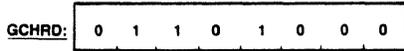
Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in Parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

Data Read Commands

Read Data from Display Memory

RDAT: | 1 | 0 | 1 | TYPE | 0 | MOD |

Data Transfer Type:

0	0	Word, low then high byte
1	0	Low byte of the Word only
1	1	High byte of the Word only
0	1	Invalid
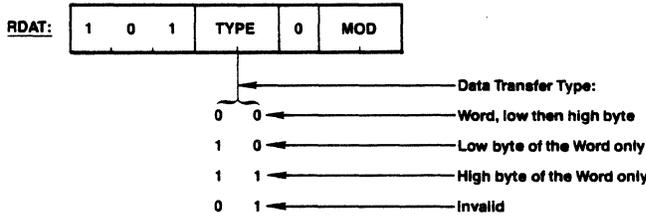
Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the GDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.

Cursor Address Read

CURD: | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

The following bytes are returned by the GDC through the FIFO:

P1 | A7 | EAD$_L$ | A0 | — Execute Address (EAD), low byte

P2 | A15 | EAD$_M$ | A8 | — Execute Address (EAD), middle byte

P3 | 0 | 0 | 0 | 0 | 0 | 0 | EAD$_H$ | — Execute Address (EAD), high bits

P4 | dAD$_L$ | — Dot Address (dAD), low byte

P5 | dAD$_H$ | — Dot Address (dAD), high byte
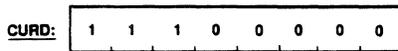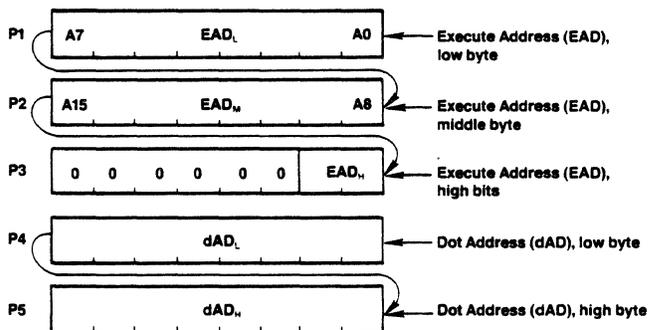
The Execute Address, EAD, points to the display memory word containing the pixel to be addressed.

The Dot Address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read

LPRD: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

The following bytes are returned by the GDC through the FIFO:

| A7 | LAD$_L$ | A0 | — Light Pen Address, low byte

| A15 | LAD$_M$ | A8 | — Light Pen Address, middle byte

| 0 | 0 | 0 | 0 | 0 | 0 | LAD$_H$ | — Light Pen Address, high byte
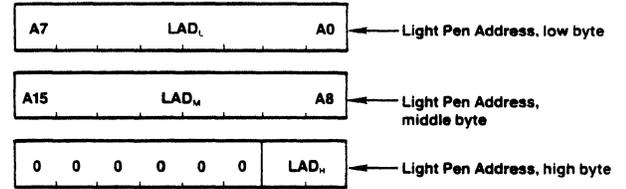
The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Read Request

DMAR: | 1 | 0 | 1 | TYPE | 1 | MOD |

Data Transfer Type:

0	0	Word, Low then High Byte
1	0	Low Byte of the Word
1	1	High Byte of the Word
0	1	Invalid

DMA Write Request

DMAW: | 0 | 0 | 1 | TYPE | 1 | MOD |

RMW Memory Logical Operation:

0	0	REPLACE with Pattern
0	1	COMPLEMENT
1	0	RESET to Zero
1	1	SET to One

Data Transfer Type:

0	0	Word, Low then High Byte
1	0	Low Byte of the Word
1	1	High Byte of the Word
0	1	Invalid
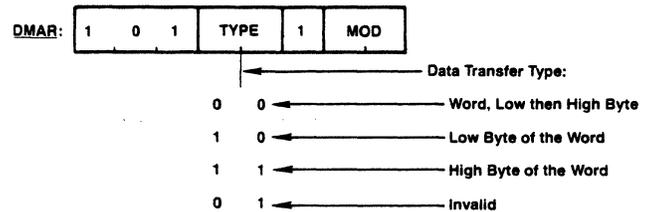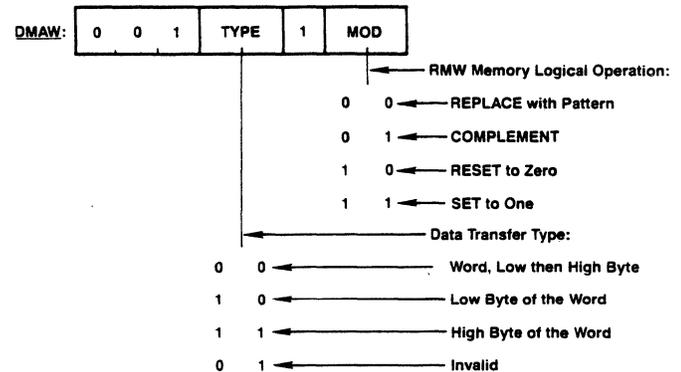
AC Characteristics, μPD7220D

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 10%; GND = 0V

Read Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Address Setup to RD↓	t_{AR}	0		0		0		ns	
Address Hold from RD↑	t_{RA}	0		0		0		ns	
RD Pulse Width	t_{RR1}	t_{RD1} + 20		t_{RD1} + 20		t_{RD1} + 20		ns	
Data Delay from RD↓	t_{RD1}		120		80		70	ns	C_L = 50 pF
Data Floating from RD↑	t_{DF}	0	120	0	100	0	90	ns	
RD Pulse Cycle	t_{RCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	

Write Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Address Setup to WR↓	t_{AW}	0		0		0		ns	
Address Hold from WR↑	t_{WA}	0		0		10		ns	
WR Pulse Width	t_{WW}	120		100		90		ns	
Data Setup to WR↑	t_{DW}	100		80		70		ns	
Data Hold from WR↑	t_{WD}	0		0		10		ns	
WR Pulse Cycle	t_{WCY}	4 t_{CLK}		4 t_{CLK}		4 t_{CLK}		ns	

DMA Read Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
DACK Setup to RD↓	t_{KR}	0		0		0		ns	
DACK Hold from RD↑	t_{RK}	0		0		0		ns	
RD Pulse Width	t_{RR2}	t_{RD2} + 20		t_{RD2} + 20		t_{RD2} + 20		ns	
Data Delay from RD↓	t_{RD2}		1.5 t_{CLK} + 120		1.5 t_{CLK} + 80		1.5 t_{CLK} + 70	ns	C_L = 50 pF
DREQ Delay from 2XWCLK↑	t_{REQ}		150		120		100	ns	C_L = 50 pF
DREQ Setup to DACK↓	t_{QK}	0		0		0		ns	
DACK High Level Width	t_{DK}	t_{CLK}		t_{CLK}		t_{CLK}		ns	
DACK Pulse Cycle	t_E	4 t_{CLK}*		4 t_{CLK}*		4 t_{CLK}*		ns	
DREQ↓ Delay from DACK↓	$t_{KQ(R)}$		t_{CLK} + 150		t_{CLK} + 120		t_{CLK} + 100	ns	C_L = 50 pF

* for high byte and low byte transfers: t_E = 5 t_{CLK}

DMA Write Cycle (GDC ↔ CPU)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
DACK Setup to WR↓	t_{KW}	0		0		0		ns	
DACK Hold from WR↑	t_{WK}	0		0		0		ns	
DREQ↓ Delay from DACK↓	$t_{KQ(W)}$		t_{CLK} + 150		t_{CLK} + 120		t_{CLK} + 100	ns	C_L = 50 pF

R/M/W Cycle (GDC ↔ Display Memory)

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Address/Data Delay from 2XWCLK↑	t_{AD}	30	160	30	130	30	110	ns	C_L = 50 pF
Address/Data Floating from 2XWCLK↑	t_{OFF}	30	160	30	130	30	110	ns	C_L = 50 pF
Input Data Setup to 2XWCLK↓	t_{DIS}	0		0		0		ns	
Input Data Hold from 2XWCLK↓	t_{DIH}	t_{DE} − 20		t_{DE} − 20		t_{DE} − 20		ns	
DBIN Delay from 2XWCLK↓	t_{DE}	30	120	30	90	30	80	ns	C_L = 50 pF
ALE↑ Delay from 2XWCLK↑	t_{RR}	30	125	30	100	30	90	ns	C_L = 50 pF
ALE↓ Delay from 2XWCLK↓	t_{RF}	30	100	30	80	30	70	ns	C_L = 50 pF
ALE Width	t_{RW}	½ t_{CLK}		½ t_{CLK}		½ t_{CLK}		ns	C_L = 50 pF
ALE Low Width	t_{RL}	t_{CLK} + 30		t_{CLK} + 30		t_{CLK} + 30		ns	

AC Characteristics, µPD7220D (Cont'd)

Display Cycle   **(GDC ↔ Display Memory)**

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Video Signal Delay from 2XWCLK ↑	t_{VD}		150		120		100	ns	C_L = 50 pF

Input Cycle   **(GDC ↔ Display Memory)**

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Input Signal Setup to 2XWCLK ↑	t_{PS}	30		20		15		ns	
Input Signal Width	t_{PW}	t_{CLK}		t_{CLK}		t_{CLK}		ns	

Clock   **(2XWCLK)**

Parameter	Symbol	7220D Limits Min	7220D Limits Max	7220D-1 Limits Min	7220D-1 Limits Max	7220D-2 Limits Min	7220D-2 Limits Max	Unit	Test Conditions
Clock Rise Time	t_{CR}		20		20		20	ns	
Clock Fall Time	t_{CF}		20		20		20	ns	
Clock High Pulse Width	t_{CH}	105		80		70		ns	
Clock Low Pulse Width	t_{CL}	105		80		70		ns	
Clock Cycle	t_{CLK}	250	2000	200	2000	180	2000	ns	

DC Characteristics
T_a = 0°C to 70°C; V_{CC} = 5V ± 10%; GND = 0V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	①
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	②
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 µA
Input Low Leak Current	I_{IL}			−10	µA	V_I = 0V
Input High Leak Current	I_{IH}			+10	µA	V_I = V_{CC}
Output Low Leak Current	I_{OL}			−10	µA	V_O = 0V
Output High Leak Current	I_{OH}			+10	µA	V_O = V_{CC}
Clock Input Low Voltage	V_{CL}	−0.5		0.6	V	
Clock Input High Voltage	V_{CH}	3.5		V_{CC} + 1.0	V	
V_{CC} Supply Current	I_{CC}			270	mA	

Capacitance
T_a = 25°C; V_{CC} = GND = 0V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	V_I (unmeasured) = 0V
Output Capacitance	C_{OUT}			20	pF	
Clock Input Capacitance	$C\phi$			20	pF	

Notes:
① For 2XWCLK, V_{IL} = −0.5V to +0.6V.
② For 2XWCLK, V_{IH} = +3.9V to V_{CC} +1.0V.

Absolute Maximum Ratings* (Tentative)

Ambient Temperature under Bias	0°C to 70°C
Storage Temperature	−65°C to 150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Power Dissipation	1.5 W

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Timing Waveforms

Microprocessor Interface Write Timing
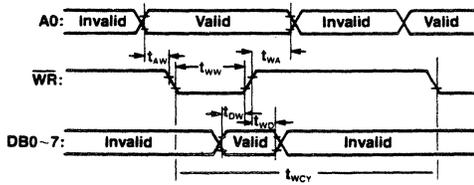
Microprocessor Interface Read Timing
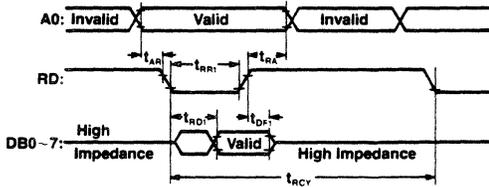
Microprocessor Interface DMA Write Timing

t_{WH} (WR ↑ to HSYNC ↑) ≥ t_{CLK}

t_{KH} (DACK ↓ to HSYNC ↑) ≥ t_{CLK}
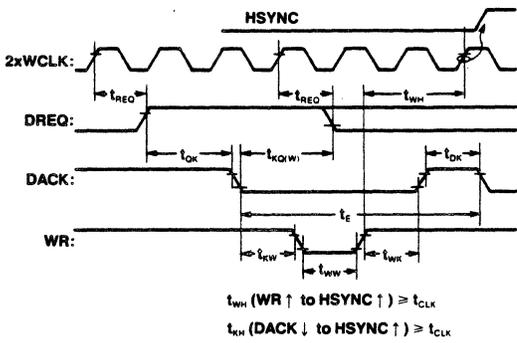
Microprocessor Interface DMA Read Timing
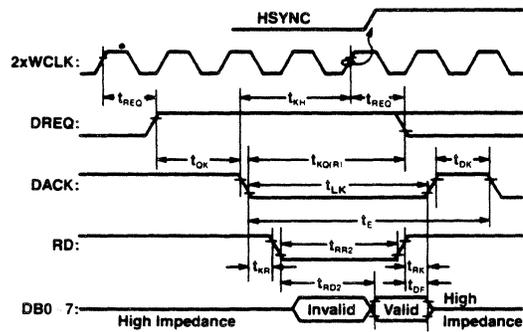
Display Memory Display Cycle Timing
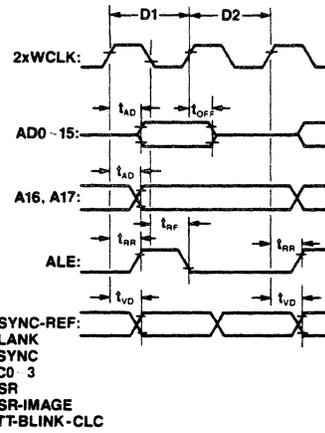
Display Memory RMW Timing

16
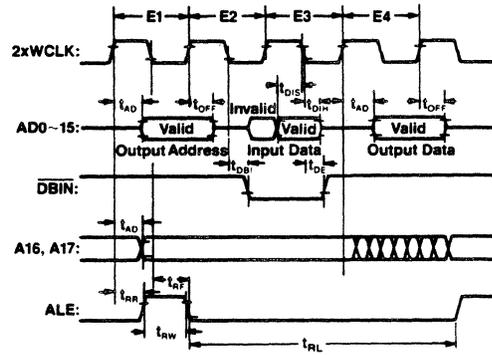
Timing Waveforms (Cont.)

Display and RMW Cycles (1x Zoom)
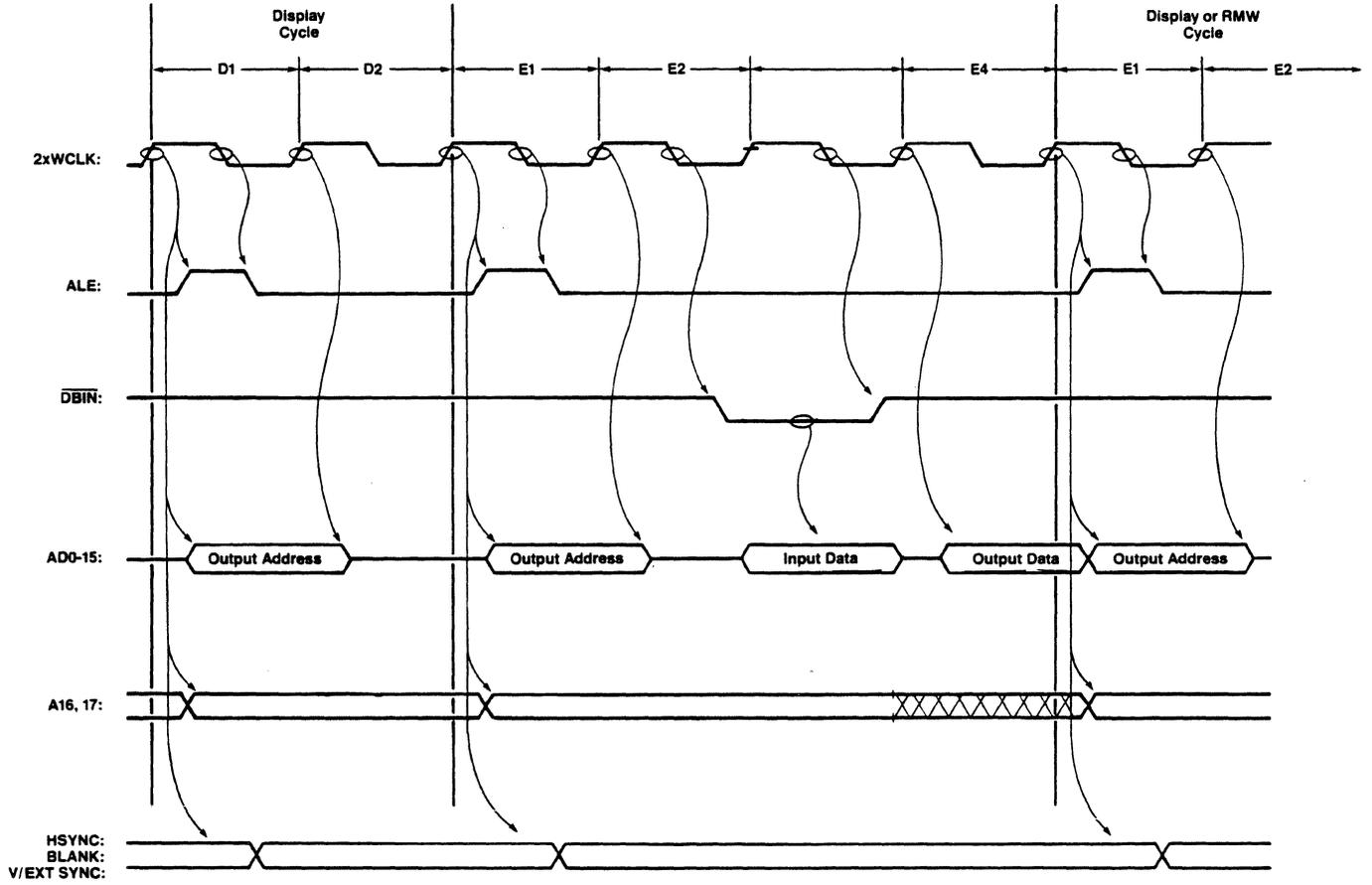
Display and RMW Cycles (2x Zoom)
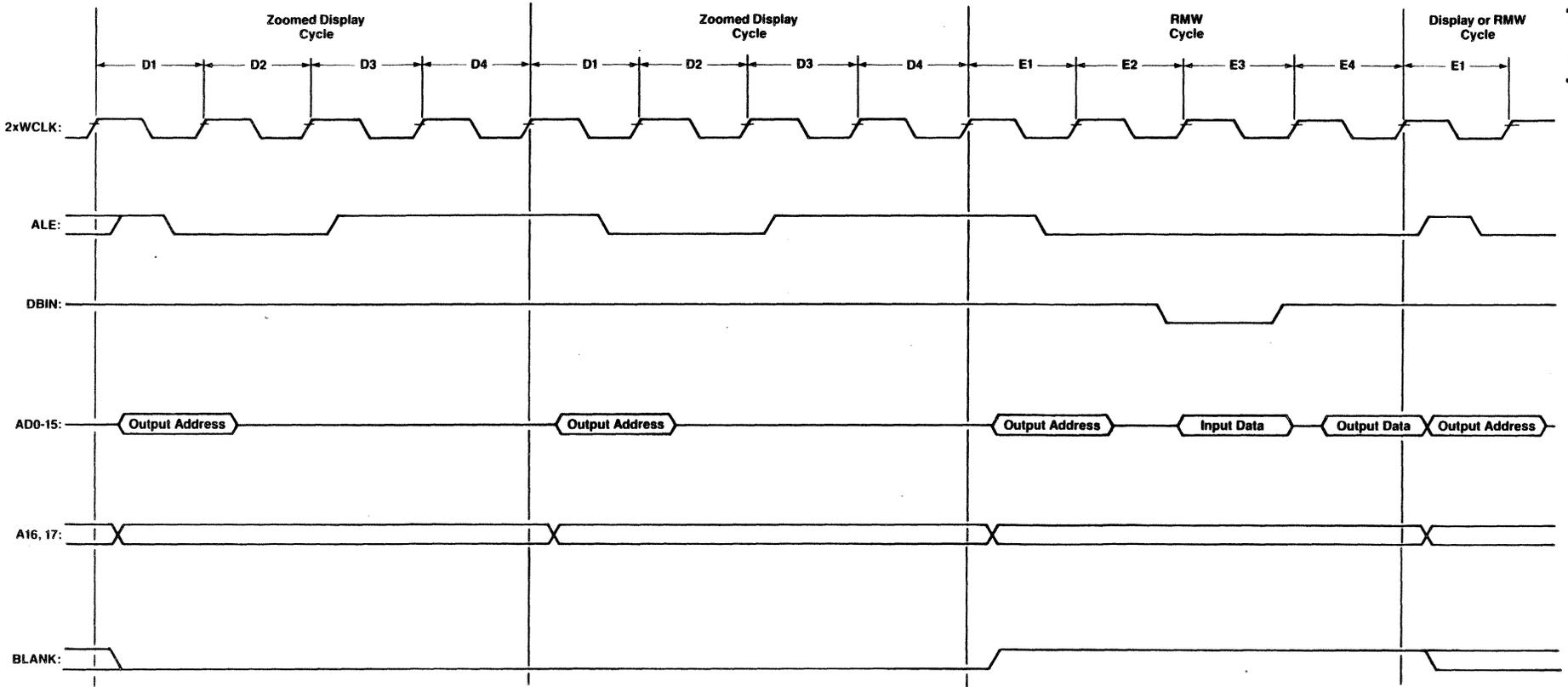
Zoomed Display Operation with RMW Cycle (3x Zoom)
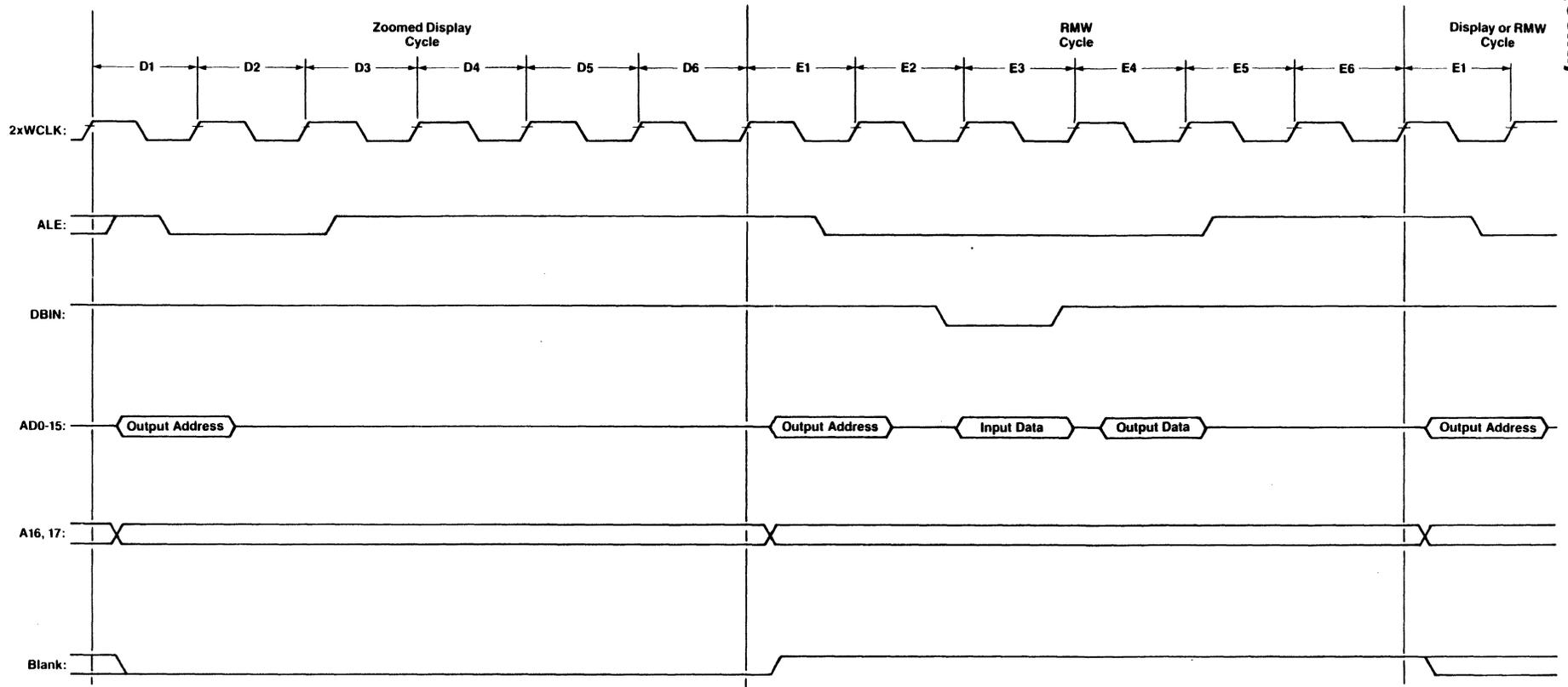
Timing Waveforms (Cont.)

Light Pen and External Sync Input Timing

2xWCLK:

t_{PS}

LPEN,
EX. SYNC:

t_{PW}

Clock Timing (2XWCLK)

t_{CR} t_{CF} t_{CH}

2xWCLK: $V_{CH} = 3.9$ $V_{CL} = 0.6$
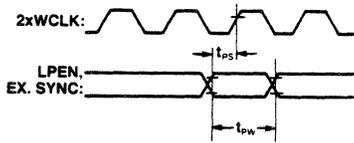
t_{CL} t_{CLK}
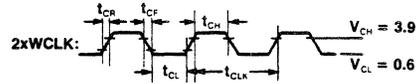
Test Level (for AC Tests, except 2XWCLK)

2.4 2.0 2.0

Miscellaneous: Test Point

0.45 0.8 0.8

$V_{OH} = 2.0$
$V_{IH} = 2.0$
$V_{OL} = 0.8$
$V_{IL} = 0.8$
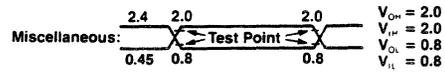
Video Sync Signals Timing

1 H

2xWCLK:

HBLANK:

HSYNC:

AD0-15:

LC0-4:

1 H

AD0-15:

LC0-4:

Row:

Row:

VBLANK:

VSYNC:

1 V (Frame)
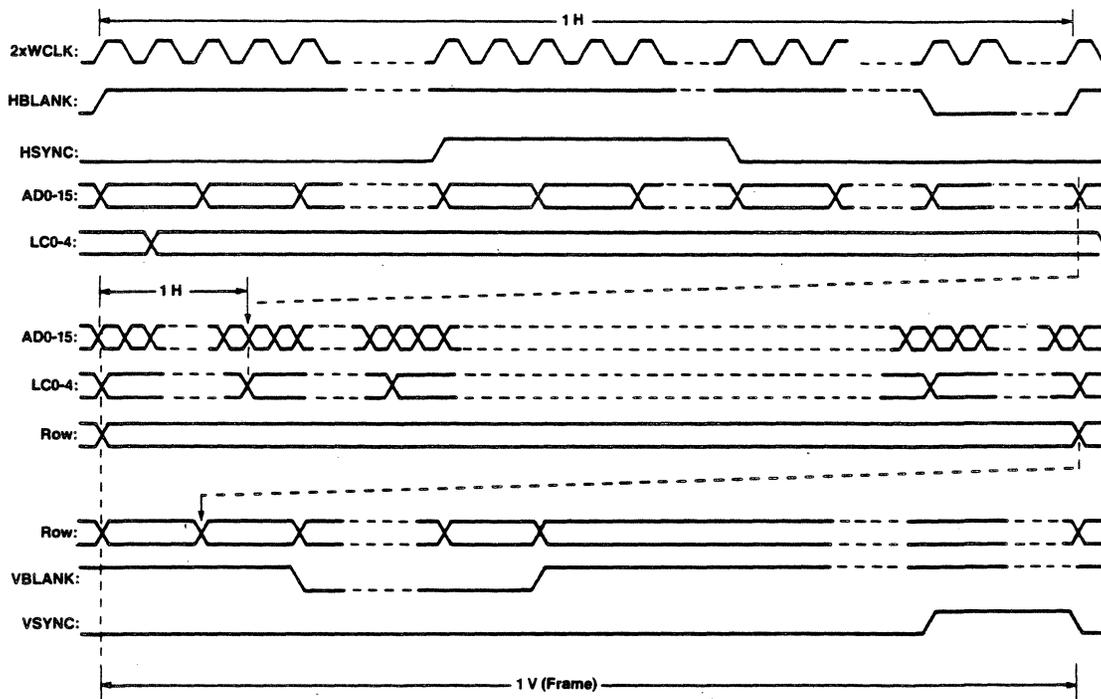
Interlaced Video Timing

HBLANK:

VBLANK:

VSYNC:
(Interlace)

Odd Field   Even Field

VSYNC:
(No Interlace)

20
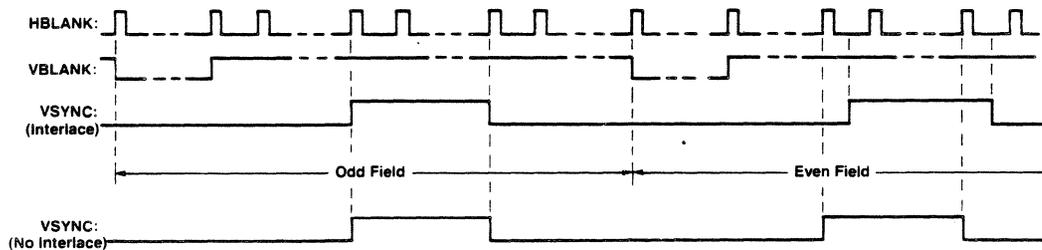
Timing Waveforms (Cont.)

Video Horizontal Sync Generator Parameters
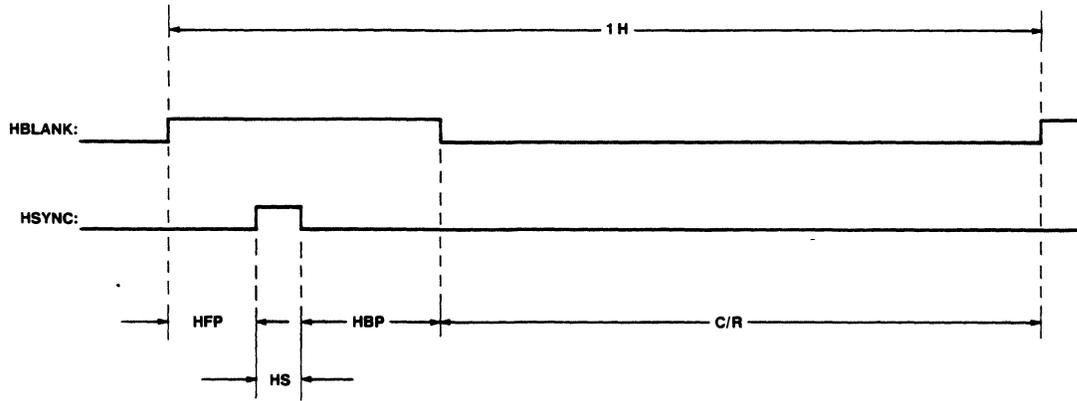
Video Vertical Sync Generator Parameters

Cursor — Image Bit Flag

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Video Field Timing

HSYNC Output
BLANK Output
Vertical SYNC Lines
Vertical Back Porch Blanked Lines
Horizontal SYNC Pulse
Horizontal Front Porch Blanking
Active Display Lines
Horizontal Back Porch Blanking
Vertical Front Porch Blanked Lines
VSYNC Output
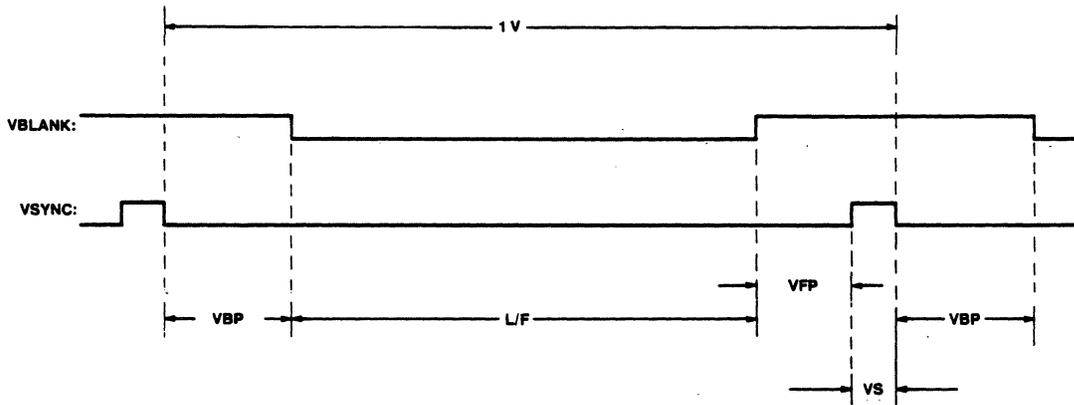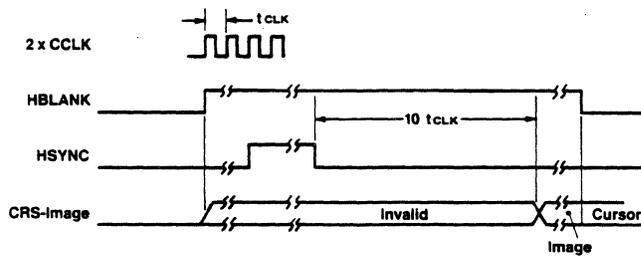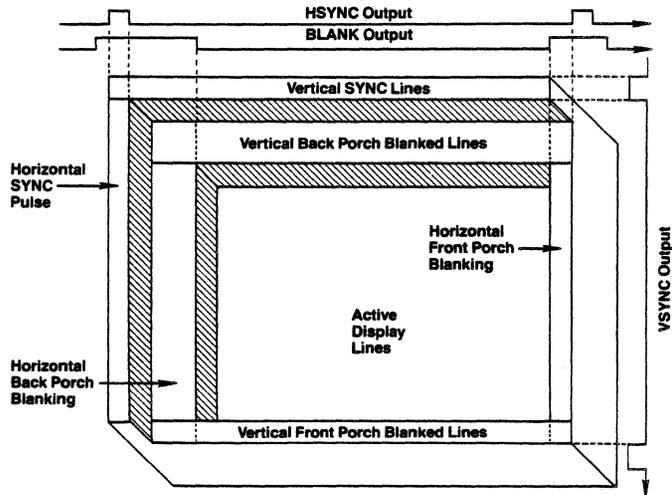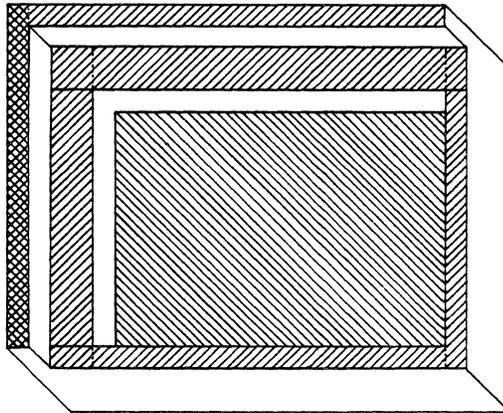
Drawing Intervals

Drawing Interval

Additional Drawing Interval When in Flash Mode

Dynamic RAM Refresh if Enabled, Otherwise Additional Drawing Interval

DMA Request Intervals
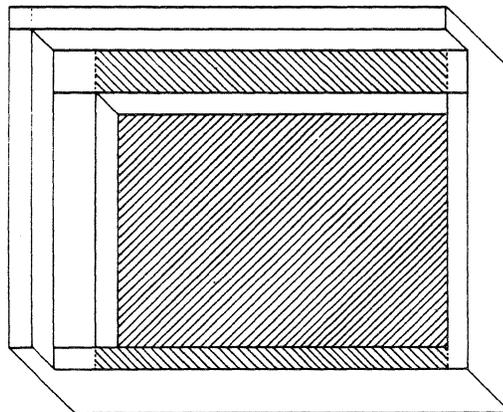
DMA Request Interval

Additional DMA Request Intervals When in Flash Mode

Block Diagram of a Graphics Terminal
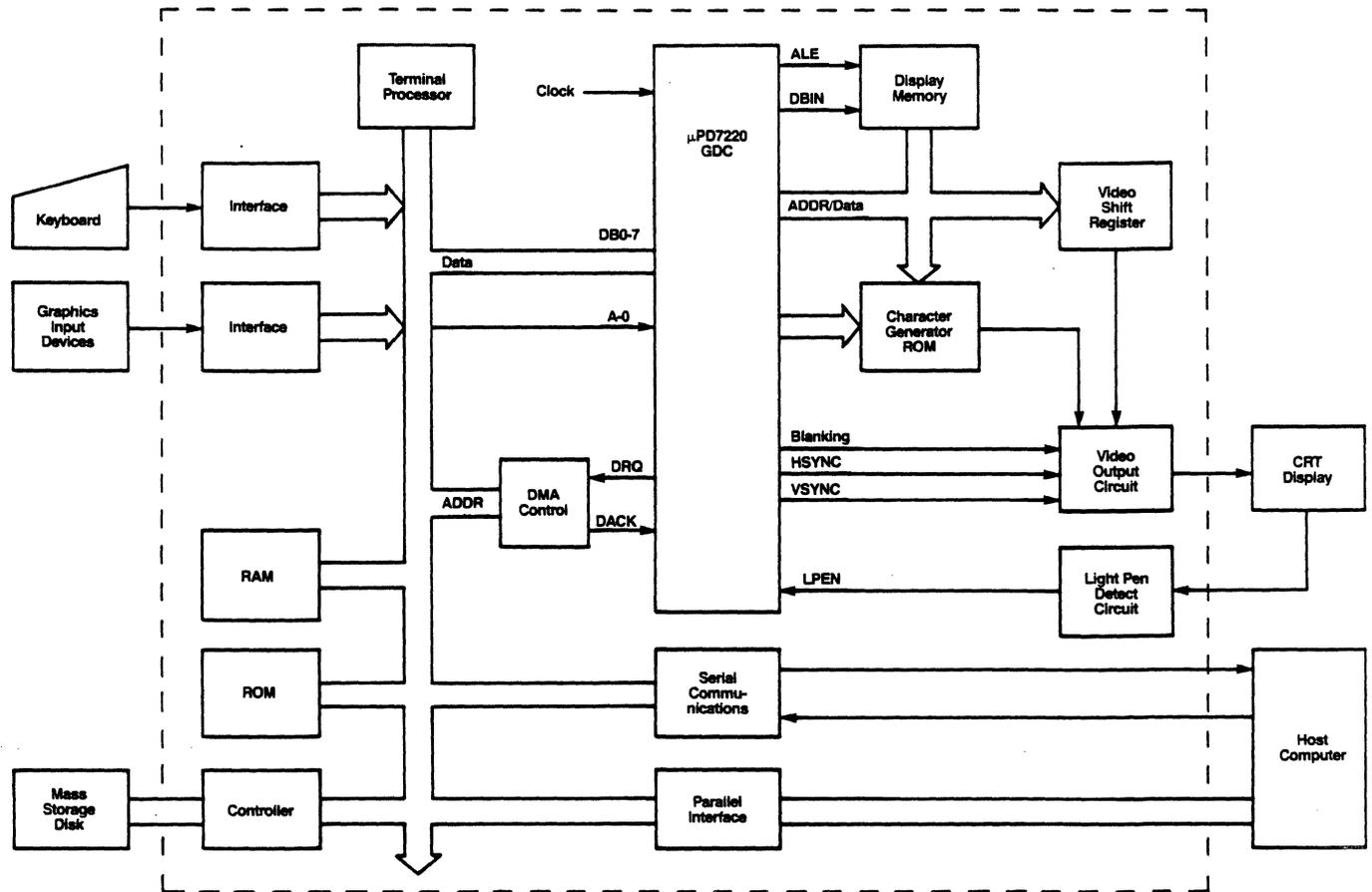
Multiplane Display Memory Diagram
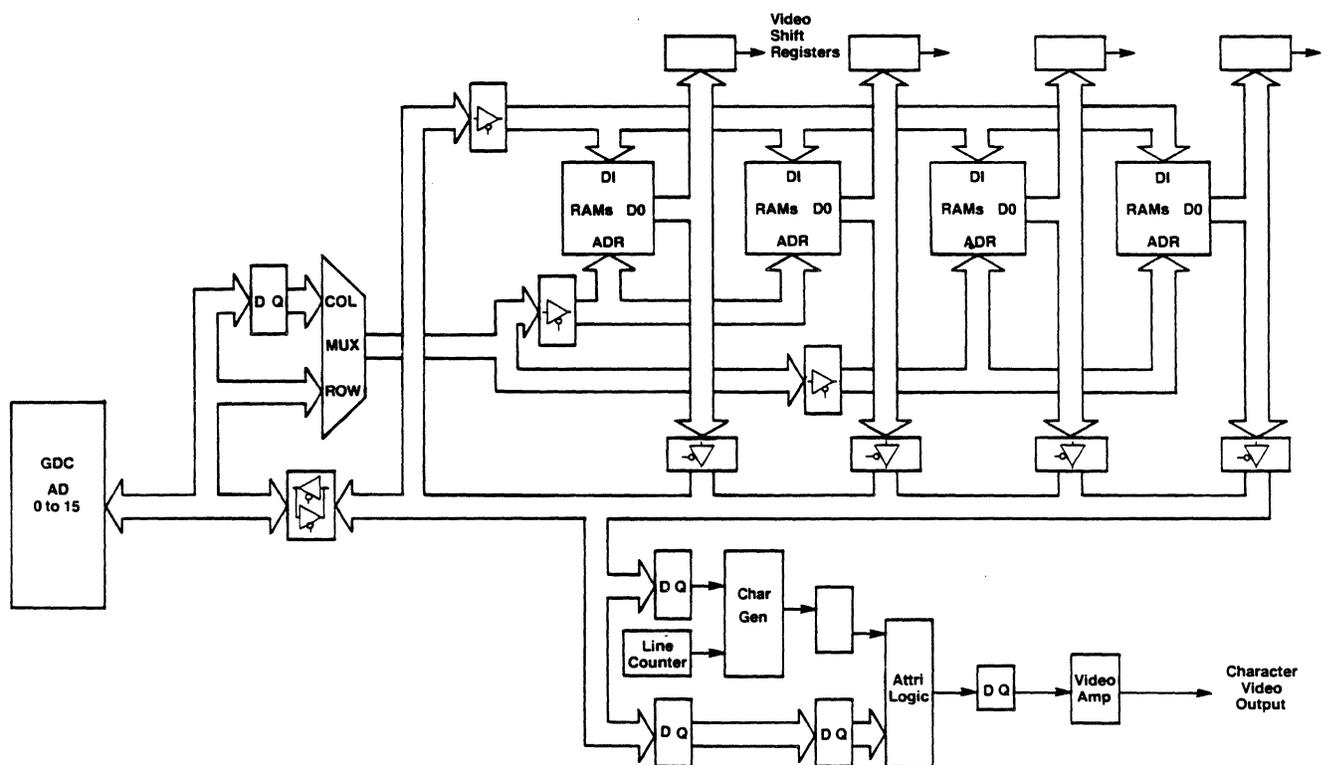
Package Outline
µPD7220D (Ceramic)
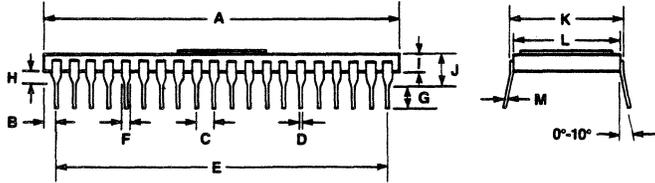
	Ceramic	
Item	Millimeters	Inches
A	51.5 Max	2.03 Max
B	1.62 Max	0.06 Max
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 Min	0.04 Min
G	3.2 Min	0.13 Min
H	1.0 Min	0.04 Min
I	3.5 Max	0.14 Max
J	4.5 Max	0.18 Max
K	15.24 Typ	0.6 Typ
L	14.93 Typ	0.59 Typ
M	0.25 ± 0.05	0.01 ± 0.0019

MC6845

MOS
(N-CHANNEL, SILICON-GATE)

**CRT CONTROLLER
(CRTC)**

CRT CONTROLLER (CRTC)

The MC6845 CRT controller performs the interface between an MPU and a raster-scan CRT display. It is intended for use in MPU-based controllers for CRT terminals in stand-alone or cluster configurations.

The CRTC is optimized for the hardware/software balance required for maximum flexibility. All keyboard functions, reads, writes, cursor movements, and editing are under processor control. The CRTC provides video timing and refresh memory addressing.

- Useful in Monochrome or Color CRT Applications
- Applications Include "Glass-Teletype," Smart, Programmable, Intelligent CRT Terminals; Video Games; Information Displays
- Alphanumeric, Semi-Graphic, and Full-Graphic Capability
- Fully Programmable Via Processor Data Bus. Timing May Be Generated for Almost Any Alphanumeric Screen Format, e.g., 80 × 24, 72 × 64, 132 × 20
- Single +5 V Supply
- M6800 Compatible Bus Interface
- TTL-Compatible Inputs and Outputs
- Start Address Register Provides Hardware Scroll (by Page or Character)
- Programmable Cursor Register Allows Control of Cursor Format and Blink Rate
- Light Pen Register
- Refresh (Screen) Memory May be Multiplexed Between the CRTC and the MPU Thus Removing the Requirements for Line Buffers or External DMA Devices
- Programmable Interlace or Non-Interlace Scan Modes
- 14-Bit Refresh Address Allows Up to 16K of Refresh Memory for Use in Character or Semi-Graphic Displays
- 5-Bit Row Address Allows Up to 32 Scan-Line Character Blocks
- By Utilizing Both the Refresh Addresses and the Row Addresses, a 512K Address Space is Available for Use in Graphics Systems
- Refresh Addresses are Provided During Retrace, Allowing the CRTC to Provide Row Addresses to Refresh Dynamic RAMs
- Pin Compatible with the MC6835

L SUFFIX
CERAMIC PACKAGE
CASE 715

S SUFFIX
CERDIP PACKAGE
CASE 734
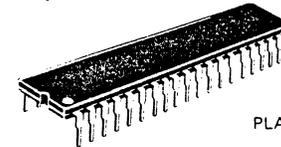
P SUFFIX
PLASTIC PACKAGE
CASE 711

PIN ASSIGNMENT

GND	1	40	VS
RESET	2	39	HS
LPSTB	3	38	RA0
MA0	4	37	RA1
MA1	5	36	RA2
MA2	6	35	RA3
MA3	7	34	RA4
MA4	8	33	D0
MA5	9	32	D1
MA6	10	31	D2
MA7	11	30	D3
MA8	12	29	D4
MA9	13	28	D5
MA10	14	27	D6
MA11	15	26	D7
MA12	16	25	$\overline{CS}$
MA13	17	24	RS
DE	18	23	E
CURSOR	19	22	R/$\overline{W}$
V$_{CC}$	20	21	CLK

ORDERING INFORMATION

Package Type	Frequency (MHz)	Temperature	Order Number
Ceramic L Suffix	1.0	0°C to 70°C	MC6845L
	1.0	−40°C to 85°C	MC6845CL
	1.5	0°C to 70°C	MC68A45L
	1.5	−40°C to 85°C	MC68A45CL
	2.0	0°C to 70°C	MC68B45L
Cerdip S Suffix	1.0	0°C to 70°C	MC6845S
	1.0	−40°C to 85°C	MC6845CS
	1.5	0°C to 70°C	MC68A45S
	1.5	−40°C to 85°C	MC68A45CS
	2.0	0°C to 70°C	MC68B45S
Plastic P Suffix	1.0	0°C to 70°C	MC6845P
	1.0	−40°C to 85°C	MC6845CP
	1.5	0°C to 70°C	MC68A45P
	1.5	−40°C to 85°C	MC68A45CP
	2.0	0°C to 70°C	MC68B45P

DS9838-R1

FIGURE 1 — TYPICAL CRT CONTROLLER APPLICATION
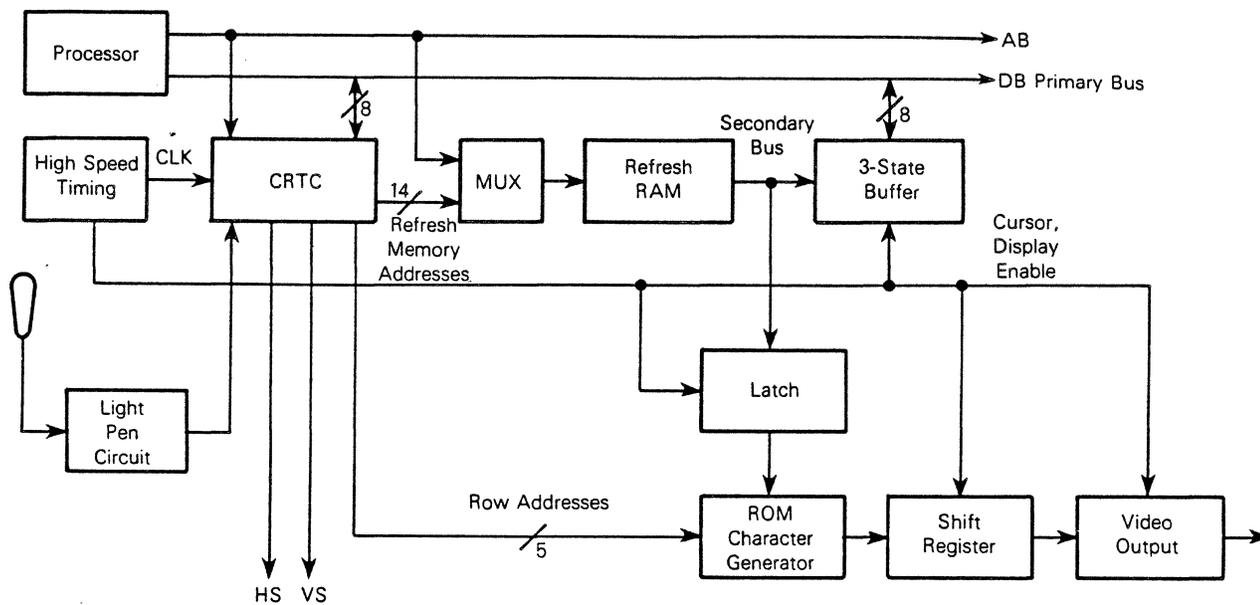
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature Range MC6845, MC68A45, MC68B45 MC6845C, MC68A45C	T_A	T_L to T_H 0 to 70 −40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Rating

Thermal Resistance
  Plastic Package
  Cerdip Package
  Ceramic Package
	θ_{JA}	100
		60
		50
			°C/W

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

RECOMMENDED OPERATING CONDITIONS

Characteristics	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input Low Voltage	V_{IL}	−0.3	—	0.8	V
Input High Voltage	V_{IH}	2.0	—	V_{CC}	V

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POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \tag{1}$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \tag{2}$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \tag{3}$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0$ Vdc ± 5%, $V_{SS} = 0$, $T_A = 0$ to 70°C unless otherwise noted, see Figures 2-4)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	2.0	—	V_{CC}	V
Input Low Voltage		V_{IL}	-0.3	—	0.8	V
Input Leakage Current		I_{in}	—	0.1	2.5	μA
Hi-Z State Input Current ($V_{CC} = 5.25$ V) ($V_{in} = 0.4$ to 2.4 V)		I_{TSI}	-10	—	10	μA
Output High Voltage		V_{OH}				V
($I_{Load} = -205$ μA)	D0-D7		2.4	3.0	—	
($I_{Load} = -100$ μA)	Other Outputs		2.4	3.0	—	
Output Low Voltage ($I_{Load} = 1.6$ mA)		V_{OL}	—	0.3	0.4	V
Internal Power Dissipation (Measured at $T_A = 0$°C)		P_{INT}	—	600	750	mW
Input Capacitance	D0-D7	C_{in}	—	—	12.5	pF
	All Others		—	—	10	
Output Capacitance	All Outputs	C_{out}	—	—	10	pF

BUS TIMING CHARACTERISTICS (See Notes 1 and 2) (Reference Figures 2 and 3)

Ident. Number	Characteristic	Symbol	MC6845		MC68A45		MC68B45		Unit
			Min	Max	Min	Max	Min	Max	
1	Cycle Time	t_{cyc}	1.0	10**	0.67	10	0.5	10**	µs
2	Pulse Width, E Low	PW_{EL}	430	—	280	—	210	—	ns
3	Pulse Width, E High	PW_{EH}	450	—	280	—	220	—	ns
4	Clock Rise and Fall Time	t_r, t_f	—	25	—	25	—	20	ns
9	Address Hold Time (RS)	t_{AH}	10	—	10	—	10	—	ns
13	RS Setup Time Before E	t_{AS}	80	—	60	—	40	—	ns
14	R/$\overline{W}$ and $\overline{CS}$ Setup Time Before E	t_{CS}	80	—	60	—	40	—	ns
15	R/$\overline{W}$ and $\overline{CS}$ Hold Time	t_{CH}	10	—	10	—	10	—	ns
18	Read Data Hold Time	t_{DHR}	20	50*	20	50*	20	50*	ns
21	Write Data Hold Time	t_{DHW}	10	—	10	—	10	—	ns
30	Peripheral Output Data Delay Time	t_{DDR}	—	290	—	180	0	150	ns
31	Peripheral Input Data Setup Time	t_{DSW}	165	—	80	—	60	—	ns

*The data bus output buffers are no longer sourcing or sinking current by t_{DHR} maximum (high impedance).

**The E clock may be low for extended periods provided the CLK input is active.

FIGURE 2 — MC6845 BUS TIMING
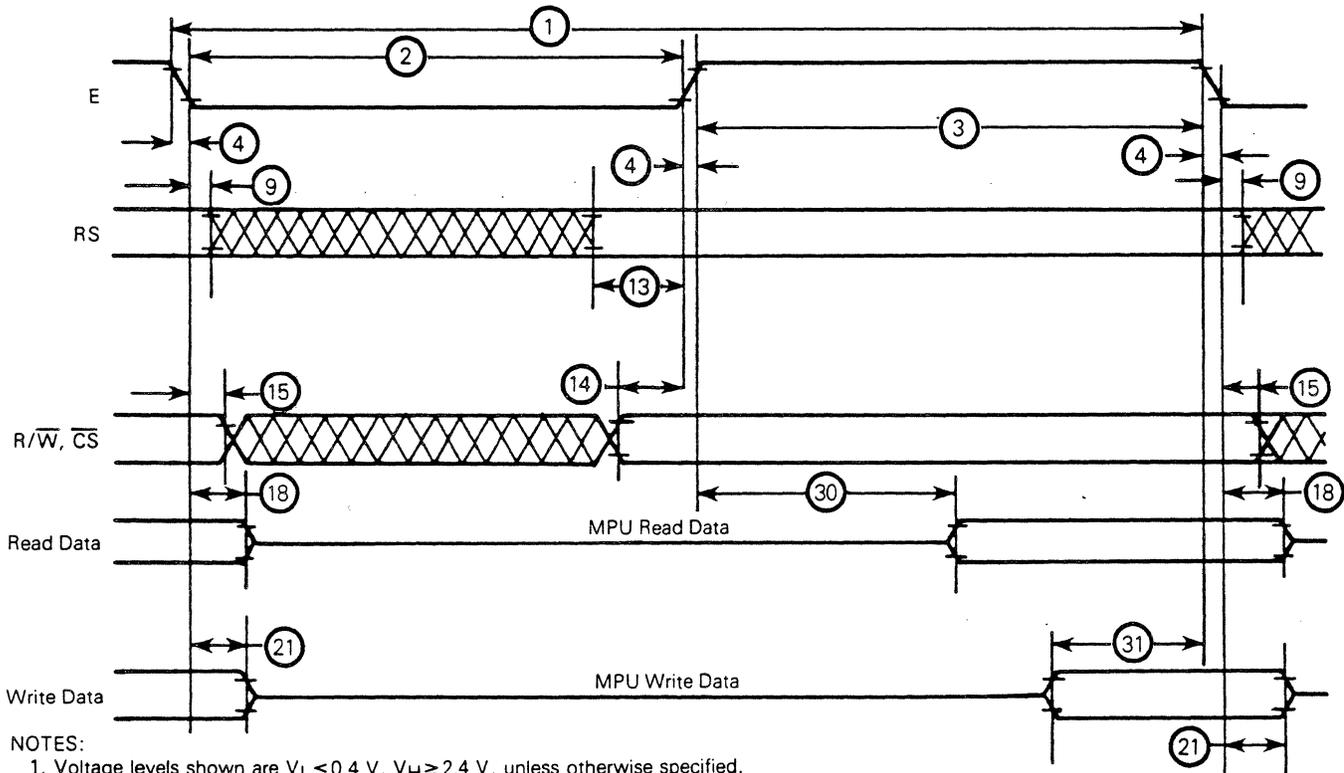
NOTES:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

FIGURE 3 — BUS TIMING TEST LOAD

C = 130 pF for D0-D7
= 30 pF for MA0-MA13, RA0-RA4, DE, HS, VS, and CURSOR
R = 11 kΩ for D0-D7
= 24 kΩ for All Other Outputs

R_L = 2.4 kΩ

MMD6150 or Equiv.
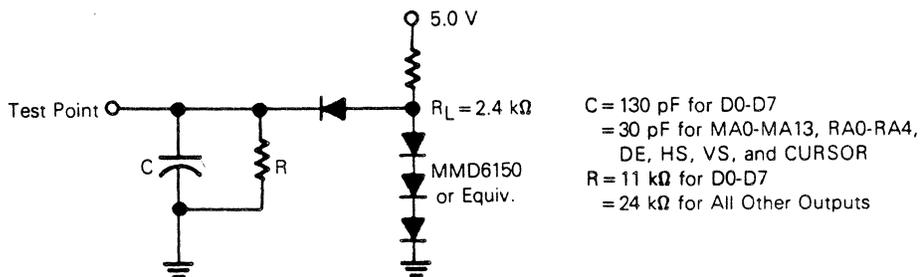
(M) MOTOROLA *Semiconductor Products Inc.*

CRTC TIMING CHARACTERISTICS (Reference Figures 4 and 5)

Characteristic	Symbol	Min	Max	Unit
Minimum Clock Pulse Width, Low	P_{WCL}	150	–	ns
Minimum Clock Pulse Width, High	P_{WCH}	150	–	ns
Clock Frequency	f_C	–	3.0	MHz
Rise and Fall Time for Clock Input	t_{cr}, t_{cf}	–	20	ns
Memory Address Delay Time	t_{MAD}	–	160	ns
Raster Address Delay Time	t_{RAD}	–	160	ns
Display Timing Delay Time	t_{DTD}	–	250	ns
Horizontal Sync Delay Time	t_{HSD}	–	250	ns
Vertical Sync Delay Time	t_{VSD}	–	250	ns
Cursor Display Timing Delay Time	t_{CDD}	–	250	ns
Light Pen Strobe Minimum Pulse Width	PW_{LPH}	80	–	ns
Light Pen Strobe Disable Time	t_{LPD1}	–	80	ns
	t_{LPD2}	–	10	ns

NOTE: The light pen strobe must fall to low level before VS pulse rises.

FIGURE 4 — CRTC TIMING CHART
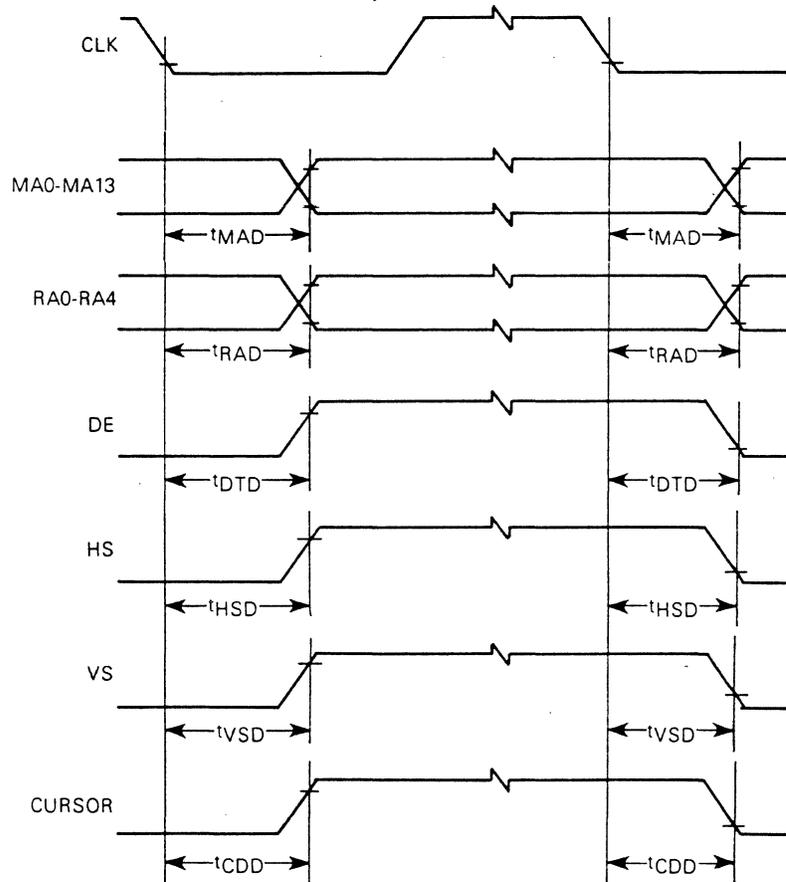
NOTE: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise noted.

FIGURE 5 — CRTC-CLK, MA0-MA13, AND LPSTB TIMING DIAGRAM

NOTE: Timing measurements are referenced to and
from a low voltage of 0.8 volts and a high
voltage of 2.0 volts, unless otherwise noted.

When the CRTC detects the rising edge of LPSTB in
this period, the CRTC sets the Refresh Memory Ad-
dress 'M + 2' into the LIGHT PEN REGISTER.

t_{LPD1}, t_{LPD2}: Period of uncertainty for the Refresh
Memory Address.
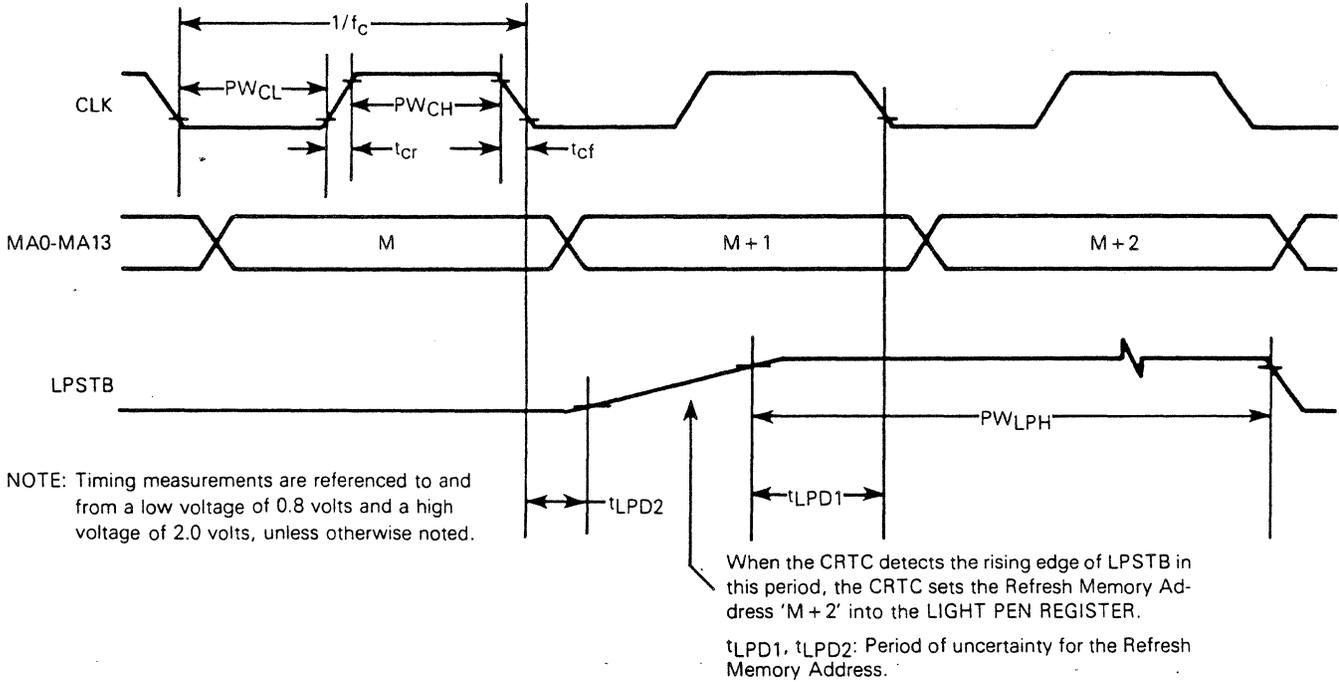
CRTC INTERFACE SYSTEM DESCRIPTION

The CRT controller generates the signals necessary to in-
terface a digital system to a raster scan CRT display. In this
type of display, an electron beam starts in the upper left
hand corner, moves quickly across the screen and returns.
This action is called a horizontal scan. After each horizontal
scan the beam is incrementally moved down in the vertical
direction until it has reached the bottom. At this point one
frame has been displayed, as the beam has made many
horizontal scans and one vertical scan.

Two types of raster scanning are used in CRTs, interlace
and non-interlace, shown in Figures 6 and 7. Non-interlace
scanning consists of one field per frame. The scan lines in
Figure 6 are shown as solid lines and the retrace patterns are
indicated by the dotted lines. Increasing the number of
frames per second will decrease the flicker. Ordinarily, either
a 50 or 60 frame per second refresh rate is used to minimize
beating between the CRT and the power line frequency. This
prevents the displayed data from weaving.

Interlace scanning is used in broadcast TV and on data
monitors where high density or high resolution data must be
displayed. Two fields, or vertical scans are made down the
screen for each single picture or frame. The first field (even
field) starts in the upper left hand corner; the second (odd
field) in the upper center. Both fields overlap as shown in
Figure 7, thus interlacing the two fields into a single frame.

In order to display the characters on the CRT screen the
frames must be continually repeated. The data to be
displayed is stored in the refresh (screen) memory by the
MPU controlling the data processing system. The data is
usually written in ASCII code, so it cannot be directly
displayed as characters. A character generator ROM is
typically used to convert the ASCII codes into the "dot" pat-
tern for every character.

The most common method of generating characters is to
create a matrix of dots "x" dots (columns) wide and "y" dots
(rows) high. Each character is created by selectively filling in

FIGURE 6 — RASTER SCAN SYSTEM (NON-INTERLACE)
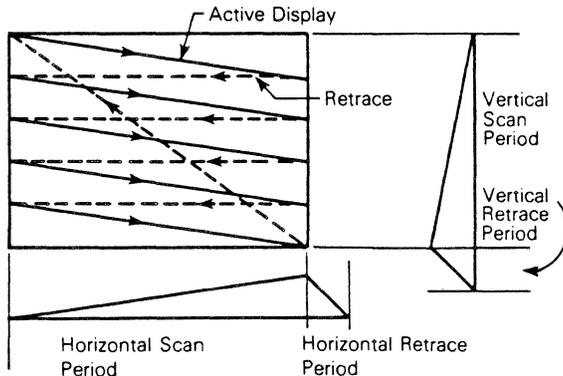
FIGURE 7 — RASTER SCAN SYSTEM (INTERLACE)

Even Number Field (First)
Odd Number Field (Second)

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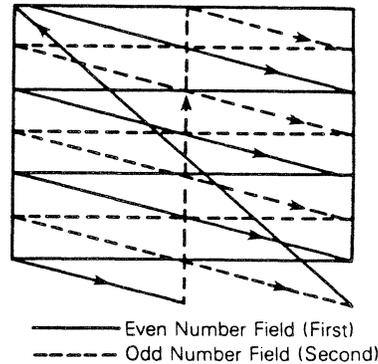
the dots. As "x" and "y" get larger a more detailed character may be created. Two common dot matrices are 5×7 and 7×9. Many variations of these standards will allow Chinese, Japanese, or Arabic letters instead of English. Since characters require some space between them, a character block larger than the character is typically used, as shown in Figure 8. The figure also shows the corresponding timing and levels for a video signal that would generate the characters.

Referring to Figure 1, the CRT controller generates the refresh addresses (MA0-MA13), row addresses (RA0-RA4), and the video timing (vertical sync — VS, horizontal sync — HS, and display enable — DE). Other functions include an internal cursor register which generates a cursor output when its contents compare to the current refresh address. A light pen strobe input signal allows capture of the refresh address in an internal light pen register.

All timing in the CRTC is derived from the CLK input. In alphanumeric terminals, this signal is the character rate. The video rate or "dot" clock is externally divided by high-speed logic (TTL) to generate the CLK input. The high-speed logic must also generate the timing and control signals necessary for the shift register, latch, and MUX control.

The processor communicates with the CRTC through an 8-bit data bus by reading or writing into the 19 registers.

The refresh memory address is multiplexed between the processor and the CRTC. Data appears on a secondary bus separate from the processor's bus. The secondary data bus concept in no way precludes using the refresh RAM for other purposes. It looks like any other RAM to the processor. A number of approaches are possible for solving contentions for the refresh memory:

1. Processor always gets priority. (Generally, "hash" occurs as MPU and CRTC clocks are not synchronized.)

2. Processor gets priority access anytime, but can be synchronized by an interrupt to perform accesses only during horizontal and vertical retrace times.

3. Synchronize the processor with memory wait cycles (states).

4. Synchronize the processor to the character rate as shown in Figure 9. The M6800 processor family works works very well in this configuration as constant cycle lengths are present. This method provides no overhead for the processor as there is never a contention for a memory access. All accesses are transparent.

FIGURE 8 — CHARACTER DISPLAY ON THE SCREEN AND VIDEO SIGNAL
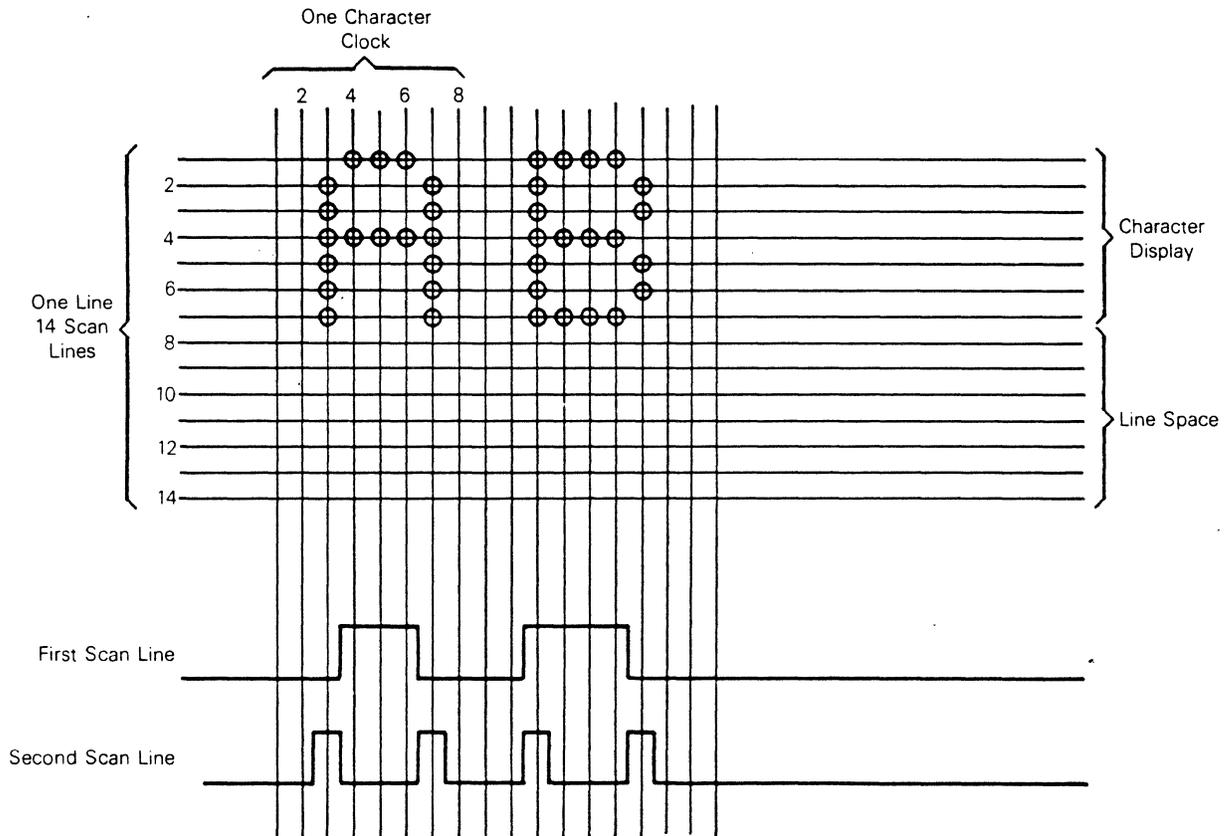
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$\overline{E}$ | CRTC Accesses Refresh Memory

E | MPU Accesses Refresh Memory

$t_{cyc} = n \times t_c$ or t_c/m
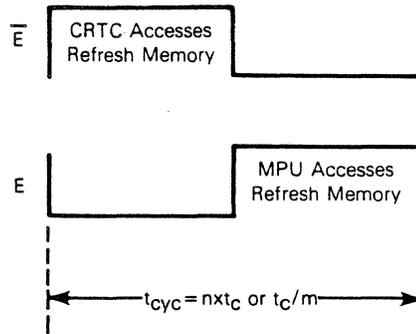
Where: m, n are integers; t_c is character period

PIN DESCRIPTION

PROCESSOR INTERFACE

The CRTC interfaces to a processor bus on the bidirectional data bus (D0-D7) using $\overline{CS}$, RS, E, and R/$\overline{W}$ for control signals.

Data Bus (D0-D7) — The bidirectional data lines (D0-D7) allow data transfers between the internal CRTC register file and the processor. Data bus output drivers are in the high-impedance state until the processor performs a CRTC read operation.

Enable (E) — The enable signal is a high-impedance TTL/MOS compatible input which enables the data bus input/output buffers and clocks data to and from the CRTC. This signal is usually derived from the processor clock. The high-to-low transition is the active edge.

Chip Select ($\overline{CS}$) — The $\overline{CS}$ line is a high-impedance TTL/MOS compatible input which selects the CRTC, when low, to read or write to the internal register file. This signal should only be active when there is a valid stable address being decoded from the processor.

Register Select (RS) — The RS line is a high-impedance TTL/MOS compatible input which selects either the address register (RS = 0) or one of the data register (RS = 1) or the internal register file.

Read/Write (R/$\overline{W}$) — The R/$\overline{W}$ line is a high-impedance TTL/MOS compatible input which determines whether the internal register file gets written or read. A write is defined as a low level.

CRT CONTROL

The CRTC provides horizontal sync (HS), vertical sync (VS), and display enable (DE) signals.

NOTE

Care should be exercised when interfacing to CRT monitors, as many monitors claiming to be "TTL compatible" have transistor input circuits which require the CRTC or TTL devices buffering signals from the CRTC/video circuits to exceed the maximum-rated drive currents.

Vertical Sync (VS) and Horizontal Sync (HS) — These TTL-compatible outputs are active high signals which drive the monitor directly or are fed to the video processing circuitry to generate a composite video signal. The VS signal determines the vertical position of the displayed text while the HS signal determines the horizontal position of the displayed text.

Display Enable (DE) — This TTL-compatible output is an active high signal which indicates the CRTC is providing addressing in the active display area.

REFRESH MEMORY/CHARACTER GENERATOR ADDRESSING

The CRTC provides memory addresses (MA0-MA13) to scan the refresh RAM. Row addresses (RA0-RA4) are also provided for use with character generator ROMs. In a graphics system, both the memory addresses and the row addresses would be used to scan the refresh RAM. Both the memory addresses and the row addresses continue to run during vertical retrace thus allowing the CRTC to provide the refresh addresses required to refresh dynamic RAMs.

Refresh Memory Addresses (MA0-MA13) — These 14 outputs are used to refresh the CRT screen with pages of data located within a 16K block of refresh memory. These outputs are capable of driving one standard TTL load and 30 pF.

Row Addresses (RA0-RA4) — These five outputs from the internal row address counter are used to address the character generator ROM. These outputs are capable of driving one standard TTL load and 30 pF.

OTHER PINS

Cursor — This TTL-compatible output indicates a valid cursor address to external video processing logic. It is an active high signal.

Clock (CLK) — The CLK is a TTL/MOS-compatible input used to synchronize all CRT functions except for the processor interface. An external dot counter is used to derive this signal which is usually the character rate in an alphanumeric CRT. The active transition is high-to-low.

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Light Pen Strobe (LPSTB) — A low-to-high transition on this high-impedance TTL/MOS-compatible input latches the current Refresh Address in the light pen register. The latching of the refresh address is internally synchronized to the character clock (CLK).

V$_{CC}$ and V$_{SS}$ — These inputs supply +5 Vdc ±5% to the CRTC.

RESET — The $\overline{\text{RESET}}$ input is used to reset the CRTC. A low level on the $\overline{\text{RESET}}$ input forces the CRTC into the following state:

(a) All counters in the CRTC are cleared and the device stops the display operation.

(b) All the outputs are driven low.

NOTE

The horizontal sync output is not defined until after R2 is programmed.

(c) The control registers of the CRTC are not affected and remain unchanged.

Functionality of $\overline{\text{RESET}}$ differs from that of other M6800 parts in the following functions:

(a) The $\overline{\text{RESET}}$ input and the LPSTB input are encoded as shown in Table 1.

TABLE 1 — CRTC OPERATING MODE

$\overline{\text{RESET}}$	LPSTB	Operating Mode
0	0	Reset
0	1	Test Mode
1	0	Normal Mode
1	1	Normal Mode

The test mode configures the memory addresses as two independent 7-bit counters to minimize test time.

(b) After $\overline{\text{RESET}}$ has gone low and (LPSTB = 0), MA0-MA13 and RA0-RA4 will be driven low on the falling edge of CLK. $\overline{\text{RESET}}$ must remain low for at least one cycle of the character clock (CLK).

(c) The CRTC resumes the display operation immediately after the release of $\overline{\text{RESET}}$. DE and the CURSOR are not active until after the first frame has been displayed.

CRTC DESCRIPTION

The CRTC consists of programmable horizontal and vertical timing generators, programmable linear address register, programmable cursor logic, light pen capture register, and control circuitry for interface to a processor bus. A block diagram of the CRTC is shown in Figure 10.

All CRTC timing is derived from the CLK, usually the output of an external dot rate counter. Coincidence (CO) circuits continuously compare counter contents to the contents of the programmable register file, R0-R17. For horizontal timing generation, comparisons result in: 1) horizontal sync pulse (HS) of a frequency, position, and width determined by the registers; 2) horizontal display signal of a frequency, position, and duration determined by the registers.

The horizontal counter produces H clock which drives the scan line counter and vertical control. The contents of the raster counter are continuously compared to the maximum scan line address register. A coincidence resets the raster counter and clocks the vertical counter.

Comparisons of vertical counter contents and vertical registers result in: 1) vertical sync pulse (VS) of a frequency and position determined by the registers; 2) vertical display of a frequency and position determined by the registers.

The vertical control logic has other functions.

1. Generate row selects, RA0-RA4, from the raster count for the corresponding interlace or non-interlace modes.

2. Extend the number of scan lines in the vertical total by the amount programmed in the vertical total adjust register.

The linear address generator is driven by the CLK and locates the relative positions of characters in memory with their positions on the screen. Fourteen lines, MA0-MA13, are available for addressing up to four pages of 4K characters, eight pages of 2K characters, etc. Using the start address register, hardware scrolling through 16K characters is possible. The linear address generator repeats the same sequence of addresses for each scan line of a character row.

The cursor logic determines the cursor location, size, and blink rate on the screen. All are programmable.

The light pen strobe going high causes the current contents of the address counter to be latched in the light pen register. The contents of the light pen register are subsequently read by the processor.

Internal CRTC registers are programmed by the processor through the data bus, D0-D7, and the control signals — R/$\overline{\text{W}}$, $\overline{\text{CS}}$, RS, and E.

REGISTER FILE DESCRIPTIONS

The nineteen registers of the CRTC may be accessed through the data bus. Only two memory locations are required as one location is used as a pointer to address one of the remaining eighteen registers. These eighteen registers control horizontal timing, vertical timing, interlace operation, row address operation, and define the cursor, cursor address, start address, and light pen register. The register addresses and sizes are shown in Table 2.

ADDRESS REGISTER

The address register is a 5-bit write-only register used as an "indirect" or "pointer" register. It contains the address of one of the other eighteen registers. When both RS and $\overline{\text{CS}}$ are low, the address register is selected. When $\overline{\text{CS}}$ is low and RS is high, the register pointed to by the address register is selected.

TIMING REGISTERS R0-R9

Figure 11 shows the visible display area of a typical CRT monitor giving the point of reference for horizontal registers as the left-most displayed character position. Horizontal registers are programmed in character clock time units with respect to the reference as shown in Figure 12. The point of reference for the vertical registers is the top character position displayed. Vertical registers are programmed in scan line times with respect to the reference as shown in Figure 13.

Horizontal Total Register (R0) — This 8-bit write-only register determines the horizontal sync (HS) frequency by defining the HS period in character times. It is the total of the displayed characters plus the non-displayed character times (retrace) minus one.

FIGURE 10 — CRTC BLOCK DIAGRAM

TABLE 2 — CRTC INTERNAL REGISTER ASSIGNMENT

$\overline{CS}$	RS	Address Register 4	3	2	1	0	Register #	Register File	Program Unit	Read	Write	Number of Bits 7	6	5	4	3	2	1	0
1	X	X	X	X	X	X	X	—	—	—	—								
0	0	X	X	X	X	X	AR	Address Register	—	No	Yes								
0	1	0	0	0	0	0	R0	Horizontal Total	Char.	No	Yes								
0	1	0	0	0	0	1	R1	Horizontal Displayed	Char.	No	Yes								
0	1	0	0	0	1	0	R2	H. Sync Position	Char.	No	Yes								
0	1	0	0	0	1	1	R3	Sync Width	—	No	Yes					H	H	H	H
0	1	0	0	1	0	0	R4	Vertical Total	Char. Row	No	Yes								
0	1	0	0	1	0	1	R5	V. Total Adjust	Scan Line	No	Yes								
0	1	0	0	1	1	0	R6	Vertical Displayed	Char. Row	No	Yes								
0	1	0	0	1	1	1	R7	V. Sync Position	Char. Row	No	Yes								
0	1	0	1	0	0	0	R8	Interlace Mode and Skew	Note 1	No	Yes							I	I
0	1	0	1	0	0	1	R9	Max Scan Line Address	Scan Line	No	Yes								
0	1	0	1	0	1	0	R10	Cursor Start	Scan Line	No	Yes		B	P		(Note 2)			
0	1	0	1	0	1	1	R11	Cursor End	Scan Line	No	Yes								
0	1	0	1	1	0	0	R12	Start Address (H)	—	No	Yes	0	0						
0	1	0	1	1	0	1	R13	Start Address (L)	—	No	Yes								
0	1	0	1	1	1	0	R14	Cursor (H)	—	Yes	Yes	0	0						
0	1	0	1	1	1	1	R15	Cursor (L)	—	Yes	Yes								
0	1	1	0	0	0	0	R16	Light Pen (H)	—	Yes	No	0	0						
0	1	1	0	0	0	1	R17	Light Pen (L)	—	Yes	No								

NOTES:
1. The interlace is shown in Table 3.
2. Bit 5 of the cursor start raster register is used for blink period control, and bit 6 is used to select blink or no-blink.

FIGURE 11 — ILLUSTRATION OF THE CRT SCREEN FORMAT

NOTE 1: Timing values are described in Table 5.

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Horizontal Displayed Register (R1) — This 8-bit write-only register determines the number of displayed characters per line. Any 8-bit number may be programmed as long as the contents of R0 are greater than the contents of R1.

Horizontal Sync Position Register (R2) — This 8-bit write-only register controls the HS position. The horizontal sync position defines the horizontal sync delay (front porch) and the horizontal scan delay (back porch). When the programmed value of this register is increased, the display on the CRT screen is shifted to the left. When the programmed value is decreased the display is shifted to the right. Any 8-bit number may be programmed as long as the sum of the contents of R2 and R3 are less than the contents of R0. R2 must be greater than R1.

Sync Width Register (R3) — This 8-bit write-only register determines the width of the horizontal sync (HS) pulse. The vertical sync pulse width is fixed at 16 scan-line times.

The HS pulse width may be programmed from 1-to-15 character clock periods thus allowing compatibility with the HS pulse width specifications of many different monitors. If zero is written into this register then no HS is provided.

Horizontal Timing Summary (Figure 12) — The difference between R0 and R1 is the horizontal blanking interval. This interval in the horizontal scan period allows the beam to return (retrace) to the left side of the screen. The retrace time is determined by the monitor's horizontal scan components. Retrace time is less than the horizontal blanking interval. A good rule of thumb is to make the horizontal blanking about 20% of the total horizontal scanning period for a CRT. In inexpensive TV receivers, the beam overscans the display screen so that aging of parts does not result in underscanning. Because of this, the retrace time should be about one third the horizontal scanning period. The horizontal sync delay, HS pulse width, and horizontal scan delay are typically programmed with a 1:2:2 ratio.

Vertical Total Register (R4) and Vertical Total Adjust Register (R5) — The frequency of VS is determined by both R4 and R5. The calculated number of character row times is usually an integer plus a fraction to get exactly a 50 or 60 Hz vertical refresh rate. The integer number of character row times minus one is programmed in the 7-bit write-only vertical total register (R4). The fraction of character line times is programmed in the 5-bit write-only vertical total adjust register (R5) as the number of scan lines required.

Vertical Displayed Register (R6) — This 7-bit write-only register specifies the number of displayed character rows on the CRT screen, and is programmed in character row times. Any number smaller than the contents of R4 may be programmed into R6.

Vertical Sync Position (R7) — This 7-bit write-only register controls the position of vertical sync with respect to the reference. It is programmed in character row times. When the programmed value of this register is increased, the display position of the CRT screen is shifted up. When the programmed value is decreased the display position is shifted down. Any number equal to or less than the vertical total (R4) and greater than or equal to the vertical displayed (R6) may be used.

Interlace Mode and Skew Register (R8) — The MC6845 only allows control of the interlace modes as programmed by the low order two bits of this write-only register. Table 3 shows the interlace modes available to the user. These modes are selected using the two low order bits of this 6-bit write-only register.

TABLE 3 — INTERLACE MODE REGISTER

Bit 1	Bit 0	Mode
0	0	Normal Sync Mode (Non-Interlace)
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync and Video Mode

In the normal sync mode (non-interlace) only one field is available as shown in Figures 6 and 14a. Each scan line is refreshed at the VS frequency (e.g., 50 or 60 Hz).

Two interlace modes are available as shown in Figures 7, 14b, and 14c. The frame time is divided between even and odd alternating fields. The horizontal and vertical timing relationship (VS delayed by one half scan line time) results in the displacement of scan lines in the odd field with respect to the even field.

In the interlace sync mode the same information is painted in both fields as shown in Figure 14b. This is a useful mode for filling in a character to enhance readability.

In the interlace sync and video mode, shown in Figure 14c, alternating lines of the character are displayed in the even field and the odd field. This effectively doubles the given bandwidth of the CRT monitor.

Care must be taken when using either interlace mode to avoid an apparent flicker effect. This flicker effect is due to the doubling of the refresh time for all scan lines since each field is displayed alternately and may be minimized with proper monitor design (e.g., longer persistence phosphors).

In addition, there are restrictions on the programming of the CRTC registers for interlace operation:

1. The horizontal total register value, R0, must be odd (i.e., an even number of character times).
2. For interlace sync and video mode only, the maximum scan-line address, R9, must be odd (i.e., an even number of scan lines).
3. For interlace sync and video mode only, the number (Nvd) programmed into the vertical display register (R6) must be one half the actual number required. The even numbered scan lines are displayed in the even field and the odd numbered scan lines are displayed in the odd field.
4. For interlace sync and video mode only, the cursor start register (R10) and cursor end register (R11) must both be even or both odd depending on which field the cursor is to be displayed in. A full block cursor will be displayed in both the even and the odd field when the cursor end register (R11) is programmed to a value greater than the value in the maximum scan line address register (R9).

FIGURE 12 — CRTC HORIZONTAL TIMING
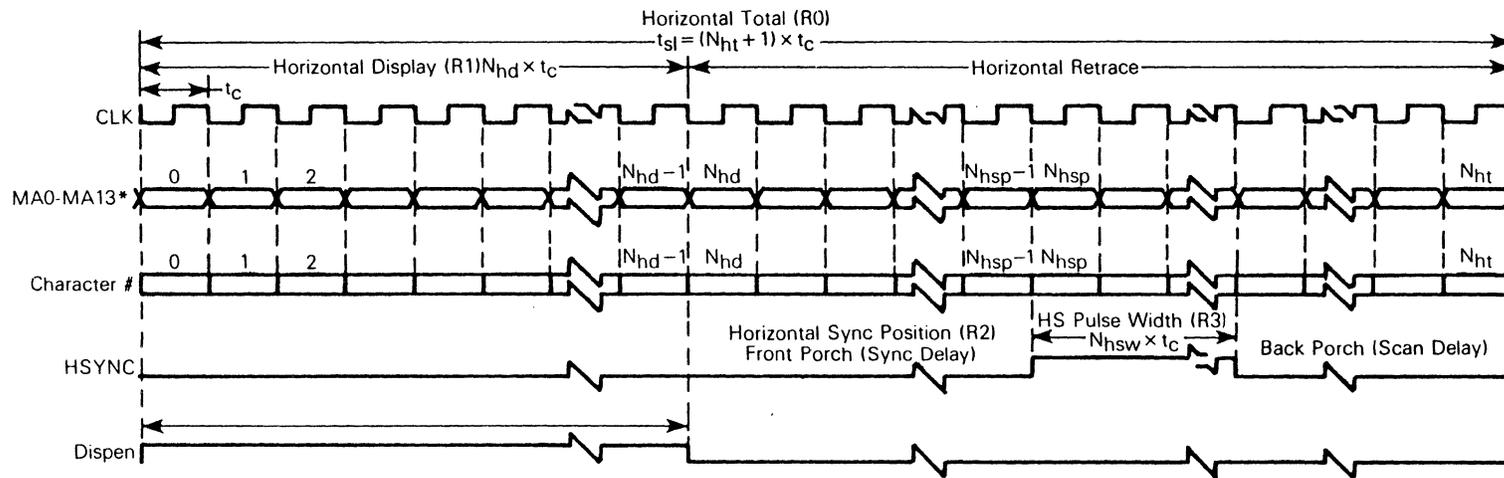
* Timing is shown for first displayed scan row only. See chart in Figure 15 for other rows. The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0.

NOTE: Timing values are described in Table 5.

FIGURE 13 — CRTC VERTICAL TIMING
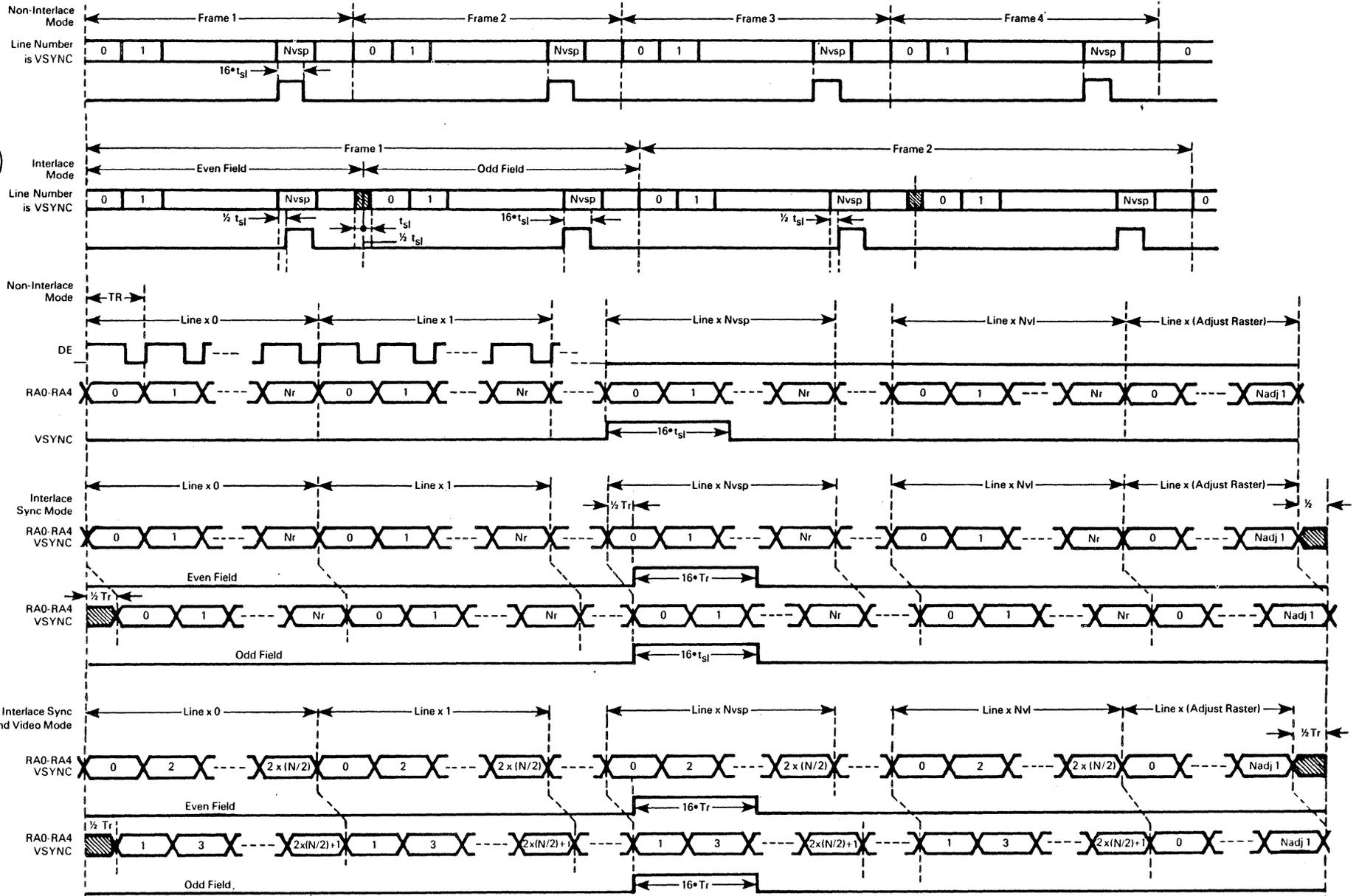
NOTES: 1. In interlace sync and video mode, maximum raster address (Nr) shall be odd.

2. In interlace mode, Nht shall be odd.

FIGURE 14 — INTERLACE CONTROL

| (a) Normal Sync | (b) Interlace Sync | (c) Interlace Sync and Video |
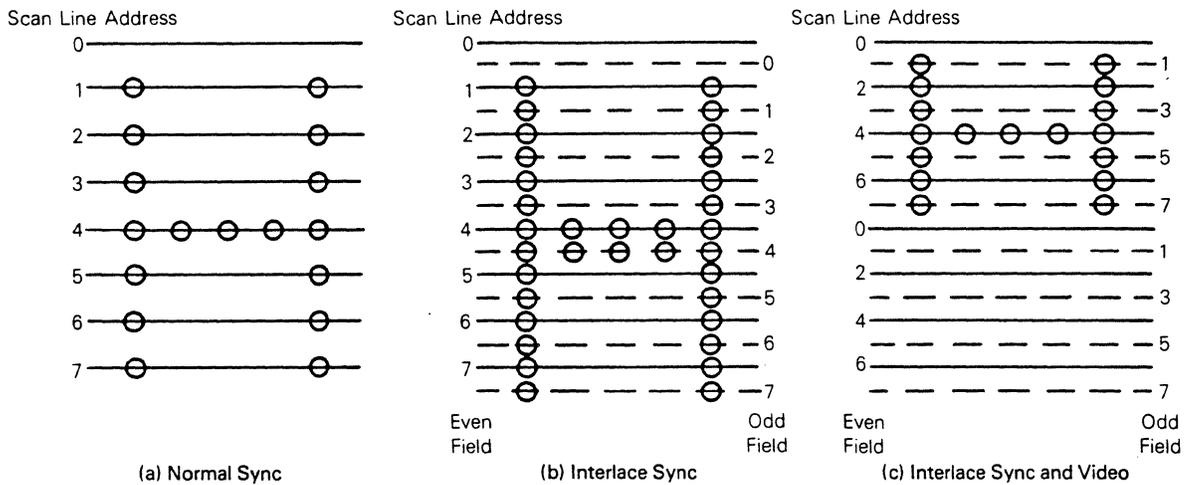
Maximum Scan Line Address Register (R9) — This 5-bit write-only register determines the number of scan lines per character row including the spacing; thus, controlling operation of the row address counter. The programmed value is a maximum address and is one less than the number of scan lines.

CURSOR CONTROL

Cursor Start Register (R10) and Cursor End Reigster (R11) — These registers allow a cursor of up to 32 scan lines in height to be placed on any scan line of the character block as shown in Figure 15. R10 is a 7-bit write-only register used to define the start scan line and the cursor blink rate. Bits 5 and 6 of the cursor start address register control the cursor operation as shown in Table 4. Non-display, display, and two blink modes (16 times or 32 times the field period) are available. R11 is a 5-bit write-only register which defines the last scan line of the cursor.

TABLE 4 — CURSOR START REGISTER

Bit 6	Bit 5	Cursor Display Mode
0	0	Non-Blink
0	1	Cursor Non-Display
1	0	Blink, 1/16 Field Rate
1	1	Blink, 1/32 Field Rate

Example of cursor display mode

When an external blink feature on characters is required, it may be necessary to perform cursor blink externally so that both blink rates are synchronized. Note that an invert/non-

invert cursor is easily implemented by programming the CRTC for a blinking cursor and externally inverting the video signal with an exclusive-OR gate.

Cursor Register (R14-H, R15-L) — This 14-bit read/write register pair is programmed to position the cursor anywhere in the refresh RAM area; thus, allowing hardware paging and scrolling through memory without loss of the original cursor position. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register.

OTHER REGISTERS

Start Address Register (R12-H, R13-L) — This 14-bit write-only register pair controls the first address output by the CRTC after vertical blanking. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register. The start address register determines which portion of the refresh RAM is displayed on the CRT screen. Hardware scrolling by character or page may be accomplished by modifying the contents of this register.

Light Pen Register (R16-H, R17-L) — This 14-bit read-only register pair captures the refresh address output by the CRTC on the positive edge of a pulse input to the LPSTB pin. It consists of an 8-bit low order (MA0-MA7) register and a 6-bit high order (MA8-MA13) register. Since the light pen pulse is asynchronous with respect to refresh address timing an internal synchronizer is designed into the CRTC. Due to delays (Figure 5) in this circuit, the value of R16 and R17 will need to be corrected in software. Figure 16 shows an interrupt driven approach although a polling routine could be used.

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FIGURE 15 — CURSOR CONTROL

Cursor Start Adr. = 9
Cursor End Adr. = 9

Cursor Start Adr. = 9
Cursor End Adr. = 10

Cursor Start Adr. = 1
Cursor End Adr. = 5
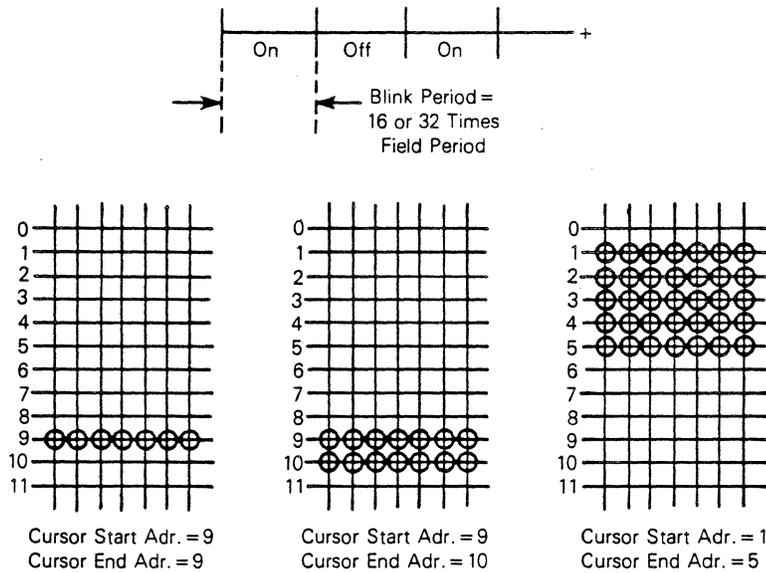
FIGURE 16 — INTERFACING OF LIGHT PEN
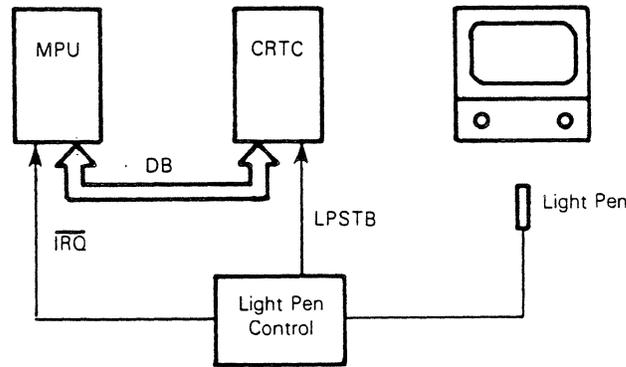
OPERATION OF THE CRTC

TIMING CHART OF THE CRT INTERFACE SIGNALS

Timing charts of CRT interface signals are illustrated in this section. When values listed in Table 5 are programmed into CRTC control registers, the device provides the outputs as shown in the timing diagrams (Figures 12, 13, 17, and 18). The screen format is shown in Figure 11 which illustrates the relation between refresh memory address (MA0-MA13), raster address (RA0-RA4), and the position on the screen. In this example, the start address is assumed to be zero.

TABLE 5 — VALUES PROGRAMMED INTO CRTC REGISTERS

Reg. #	Register Name	Value	Programmed Value
R0	H. Total	$N_{ht} + 1$	N_{ht}
R1	H. Displayed	N_{hd}	N_{hd}
R2	H. Sync Position	N_{hsp}	N_{hsp}
R3	H. Sync Width	N_{hsw}	N_{hsw}
R4	V. Total	$N_{vt} + 1$	N_{vt}
R5	V. Scan Line Adjust	N_{adj}	N_{adj}
R6	V. Displayed	N_{vd}	N_{vd}
R7	V. Sync Position	N_{vsp}	N_{vsp}
R8	Interlace Mode		
R9	Max. Scan Line Address	N_{sl}	N_{sl}

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FIGURE 17 — CURSOR TIMING
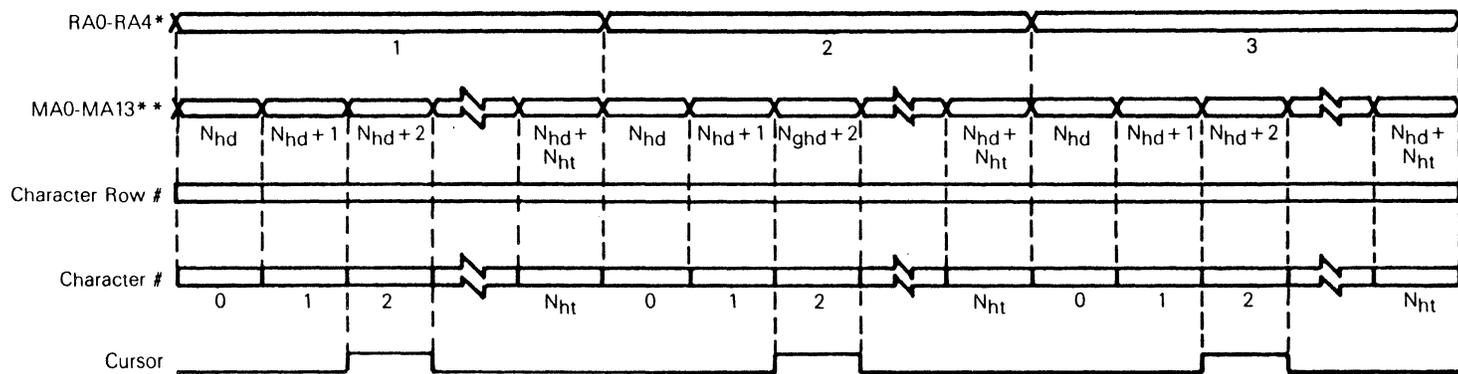
*Timing is shown for non-interlace and interlace sync modes.
  Example shown has cursor programmed as:
    Cursor Register = N_{hd} + 2
    Cursor Start = 1
    Cursor End = 3
**The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0.

NOTE 1: Timing values are described in Table 5.

FIGURE 18 — REFRESH MEMORY ADDRESSING (MA0-MA13) STAGE CHART

Character Row	Scan Line	Horizontal Display				Horizontal Retrace (Non-Display)		
		Character 0	1	→	$N_{hd}-1$	N_{hd}	→	N_{ht}
0	0	0	1	→	$N_{hd}-1$	N_{hd}	→	N_{ht}
	N_{sl}	0	1	→	$N_{hd}-1$	N_{hd}	→	N_{ht}
1	0	N_{hd}	$N_{hd}+1$	→	$2 \times N_{hd}-1$	$2 \times N_{hd}$	→	$N_{hd}+N_{ht}$
	N_{sl}	N_{hd}	$N_{hd}+1$	→	$2 \times N_{hd}-1$	$2 \times N_{hd}$	→	$N_{hd}+N_{ht}$
2	0	$2 \times N_{hd}$	$2 \times N_{hd}+1$	→	$3 \times N_{hd}-1$	$3 \times N_{hd}$	→	$2N_{hd}+N_{ht}$
	N_{sl}	$2 \times N_{hd}$	$2 \times N_{hd}+1$	→	$3 \times N_{hd}-1$	$3 \times N_{hd}$	→	$2N_{hd}+N_{ht}$
$N_{vd}-1$	0	$(N_{vd}-1) \times N_{hd}$	$(N_{vd}-1) \times N_{hd}+1$	→	$N_{vd} \times N_{hd}+1$	$N_{vd} \times N_{hd}$	→	$(N_{vd}-1) \times N_{hd}+N_{ht}$
	N_{sl}	$(N_{vd}-1) \times N_{hd}$	$(N_{vd}-1) \times N_{hd}+1$	→	$N_{vd} \times N_{hd}-1$	$N_{vd} \times N_{hd}$	→	$(N_{vd}-1) \times N_{hd}+N_{ht}$
N_{vd}	0	$N_{vd} \times N_{hd}$	$N_{vd} \times N_{hd}+1$	→	$(N_{vd}+1) \times N_{hd}-1$	$(N_{vd}+1) \times N_{hd}$	→	$N_{vd} \times N_{hd}+N_{ht}$
	N_{sl}	$N_{vd} \times N_{hd}$	$N_{vd} \times N_{hd}+1$	→	$(N_{vd}+1) \times N_{hd}-1$	$(N_{vt}+1) \times N_{hd}$	→	$N_{vd}+N_{hd}+N_{ht}$
N_{vt}	0	$N_{vt} \times N_{hd}$	$N_{vt} \times N_{hd}+1$		$(N_{vt}+1) \times N_{hd}-1$	$(N_{vt}+1) \times N_{hd}$		$N_{vt} \times N_{hd}+N_{ht}$
	N_{sl}	$N_{vt} \times N_{hd}$			$(N_{vt}+1) \times N_{hd}-1$	$(N_{vt}+1) \times N_{hd}$		$N_{vt} \times N_{hd}+N_{ht}$
$N_{vt}+1$	0	$(N_{vt}+1) \times N_{hd}$	$(N_{vt}+1) \times N_{hd}+1$		$(N_{vt}+2) \times N_{hd}-1$	$(N_{vt}+2) \times N_{hd}$		$(N_{v}+1)N_{hd}+N_{ht}$
	$N_{adj}-1$	$(N_{vt}+1) \times N_{hd}$	$(N_{vt}+1) \times N_{d}+1$		$(N_{vt}+2) \times N_{hd}-1$	$(N_{vt}+2) \times N_{hd}$		$(N_{vt}+1)N_{hd}+N_{ht}$

Left-margin labels: Vertical Display ; Vertical Retrace (Non-Display)

NOTE 1: The initial MA is determined by the contents of start address register, R12/R13. Timing is shown for R12/R13 = 0. Only non-interlace and interlace sync modes are shown.

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DETERMINING REGISTER CONTENTS

Some of the register contents are determined rather easily. They are:

Register	Name	Contents
R8	Interlace Mode Register	See Table 3
R10	Cursor Start	See Figure 15 and Table 4
R11	Cursor End	See Figure 15
R12	Start Address (H)	User programs first memory location to be displayed
R13	Start Address (L)	
R14	Cursor (H)	User programs desired cursor location
R15	Cursor (L)	
R16	Light Pen (H)	Can be loaded via light-pen strobe only
R17	Light Pen (L)	

The remaining register contents must be determined from some basic data related to the CRT monitor and from the user-desired display format. The CRTC reference sheet (see Figure 19) gives a set of formulas for calculating the register contents as well as other useful characteristics of the display. This type of data is summarized under basic parameters in Figures 20 and 21; most or all of this data must be supplied by the user before he can determine the contents for registers R0-R7 and R9. All variables B_1-B_{10} are equal to basic parameters 1 through 10.

FIGURE 19 — CRTC REFERENCE SHEET

Register Function		Intermediate Calculations			Register Calculations	
R0	Horizontal Total	Symbol	Description	Calculation	Register	Calculation
R1	Horizontal Displayed	f'	Dot frequency (1st approx.)	$\dfrac{B_5 \bullet (B_7 + B_9)}{(1/B_1) - B_3}$	R0	$\dfrac{f'}{B_1 \bullet (B_7 + B_9)} - 1$
R2	Horizontal Sync Position					
R3	Horizontal Sync Width	t_c	Character Time	$\dfrac{1}{[(R0) + 1] \bullet B_1}$	R1	B_5
R4	Vertical Total	f	Dot frequency	$\dfrac{B_7 + B_9}{t_c}$		
R5	Vertical Total Adjust				R2	$(R1) + \dfrac{(R3)}{2}$
R6	Vertical Displayed	t_{sl}	Scan line time	$[(R0) + 1] \bullet t_c$	R3	$\dfrac{(R0) - (R1)}{3}$
R7	Vertical Sync Position	n	Total # of scan lines	$\dfrac{1}{B_2 \bullet t_{sl}}$		
R8	Interlace Mode				R4	$N - 1$
R9	Maximum Scan Line Address	N	Integer and	$\dfrac{n}{B_8 + B_{10}} = N + \dfrac{R}{B_8 + B_{10}}$	R5	R
R10	Cursor Start	R	Integer remainder			
R11	Cursor End				R6	B_6
R12	Start Address (H)	t_{cr}	Character row time	$(B_8 + B_{10}) \bullet t_{sl}$	R7	$[(R4) + 1] - \dfrac{16 - (R5)}{B_8 + B_{10}} \geq (R7) \geq (R6)$
R13	Start Address (L)	t_{hr}	Horizontal retrace time	$\leq \dfrac{[(R0) + 1 - B_5] \bullet (B_7 + B_9)}{f}$		
R14	Cursor (H)				R9	$(B_8 + B_{10}) - 1$
R15	Cursor (L)	t_{vr}	Vertical retrace time	$\leq \dfrac{B_1}{B_2} - B_6(B_8 + B_{10}) \bullet t_{sl}$		
R16	Light Pen (H)					
R17	Light Pen (L)					

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In Figures 20 and 21, worksheet example calculations are shown for 32 × 16 and 80 × 24 display formats respectively. The following items are keyed to the figures. Basic parameters ① through ⑩ have been provided; items ① through ④ are data about the CRT monitor and items ⑤ through ⑩ are data about the user's desired display.

① Calculate the approximate dot frequency. The user should verify that the bandwidth of his CRT monitor will accomodate this frequency.

② Calculate R0. The resultant answer will usually be an integer plus a fraction. Assume the next high integer.

③ Fill in value for R1.

④ Calculate R3. Use the next highest integer. In these examples the sync width was chosen to be one third of the horizontal blanking interval.

⑤ Calculate R2. Again, use the next highest integer.

⑥ Calculate t_C, character tie. This is the time required for one scan line of one character block to be written.

⑦ Calculate the exact dot frequency.

⑧ Calculate t_{sl}, scan line time. This is the time required for one scan line of one character row to be written including retrace time.

⑨ Calculate n. This is the total number of scan lines for each frame. Discard any fraction.

⑩ Calculate N and R.

⑪ Calculate R4.

⑫ Fill in R5.

⑬ Fill in R6.

⑭ Calculate R7. If there is no possible value for R7, then the display demands for the CRT monitor exceed its capability. A compromise adjustment must be made in basic parameter 6, 8, or 10.

⑮ Calculate R9.

⑯ Calculate t_{cr}. This the time required for one character row to be written.

⑰ Calculate t_{hr}. $t_{hr} > B_3$.

⑱ Calculate t_{vr}. $t_{vr} > B_4$.

In Figure 20, calculation Ⓑ verifies that the vertical period is 16.667 milliseconds or 60 hertz. The expression used is:

$$t_{cr} \times [(R4) + 1] + [t_{sl} \times (R5)] = V_P.$$

Another check is calculation of horizontal sync pulse width R3. $t_C = PW_{HS}$ (typically approximately equals 4 microseconds).

For convenience, a blank worksheet is provided in Figure 22.

FIGURE 20 — CRTC WORKSHEET EXAMPLE CALCULATION (32 × 16)

Basic Parameters (B1-B10)

	Symbol
1. Horizontal frequency	$= \underline{15750 \pm 500}$ ① f'
2. Vertical frequency	$= \underline{\quad 60 \quad}$ ⑥ t_C
3. Minimum Horizontal retrace time	$= \underline{11 \times 10^{-6}}$ ⑦ f
4. Minimum vertical retrace time	$= \underline{\quad 10^{-3} \quad}$ ⑧ t_{sl}
5. # of displayed characters per row	$= \underline{\quad 32 \quad}$ ⑨ n
6. # of displayed charactor rows	$= \underline{\quad 16 \quad}$ ⑩ N
7. # of dots in character dot matrix row	$= \underline{\quad 5 \quad}$ R
8. # of scan lines in charactor • matrix column	$= \underline{\quad 7 \quad}$ ⑯ t_{cr}
9. Number of dots between horizontal adjacents	$= \underline{\quad 2 \quad}$ ⑰ t_{hr}
10. Number of scan lines between vertical adjacents	$= \underline{\quad 8 \quad}$ ⑱ t_{vr}

Intermediate Calculations

$$\frac{32 \times (5+2)}{\dfrac{1 - 11 \times 10^{-6}}{15750}} = 4.27 \times 10^6$$

$$\frac{1}{39 \times 15750} = 1.63 \times 10^{-6}$$

$$\frac{5+2}{1.63 \times 10^{-6}} = 4.29 \times 10^6$$

$$39 \times 1.63 \times 10^{-6} = 63.6 \times 10^{-6}$$

$$\frac{1}{60 \times 63.6 \times 10^{-6}} = 262$$

$$\frac{262}{7+8} = 7$$

$$(7+8) \times 63.6 \times 10^{-6} = 954 \times 10^{-6}$$

$$\frac{(38 + 1 - 32) \bullet (5+2)}{4.29 \times 10^6} = 11.42 \times 10^{-6}$$

$$[\frac{15750}{60} - 16(7+8)] \times 63.6 \times 10^{-6} = 1.431 \times 10^{-3}$$

Register Calculations

Value	Register		Decimal	Hex
$= \underline{4.27 \times 10^6}$	② R0	$\dfrac{4.27 \times 10^6}{15,750 \times (5+2)} - 1 =$	38	26
$= \underline{1.63 \times 10^{-6}}$	③ R1	$B_5 = 32$	32	20
	⑤ R2	$\dfrac{32 + 3}{2}$	33	21
$= \underline{4.29 \times 10^6}$	④ R3	$\dfrac{38 - 32}{3} =$	2	2
$= \underline{63.6 \times 10^{-6}}$	⑪ R4	$17 - 1 =$	16	10
$= \underline{\quad 262 \quad}$	⑫ R5	$R = 7$	7	7
$\underline{\quad 17 \quad}$	⑬ R6	$B_6 = 16$	16	10
$= \underline{\quad 7 \quad}$	⑭ R7	Ⓐ	16	10
	R8			
$= \underline{954 \times 10^{-6}}$	⑮ R9	$7 + 8 - 1 =$	14	0E
	R10			
$= \underline{11.42 \times 10^{-6}}$	R11			
$= \underline{1.431 \times 10^{-3}}$	R12			
	R13			
	R14			
	R15			

Ⓐ $16 + 1 - \dfrac{16 - 7}{7 + 8} \geq (R7) \geq 16$

$17 - .6 \geq (R7) \geq 16$

Ⓑ $954 \times 10^{-6} \times 17 = 16.218 \times 10^{-3}$

$+ \dfrac{63.6 \times 10^{-6} \times 7 = .445 \times 10^{-3}}{16.663 \text{ ms}} = \dfrac{1}{f}$

$f \approx 60 \text{ Hz}$

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FIGURE 21 — CRTC WORKSHEET EXAMPLE CALCULATION (80×24)

Basic Parameters (B1-B10)　　　　**Intermediate Calculations**　　　　**Register Calculations**

		Symbol		Value	Register		Decimal	Hex

1. Horizontal frequency　$= \underline{18,600}$　①　f'　　$\dfrac{80 \bullet (7+2)}{\dfrac{1}{18600} - 11 \times 10^{-6}}$　　$16 \bullet 836 \times 10^6$　② R0　$\dfrac{16.836 \times 10^6 - 1}{(18,600)(9)}$　$\underline{100}$　$\underline{64}$

③ R1　$B5 = 80$　$\underline{80}$　$\underline{50}$

2. Vertical frequency　$= \underline{60}$　⑥　t_c　　$\dfrac{1}{(100+1) \bullet 18600}$　532.31×10^{-9}　⑤ R2　$80 + \dfrac{7}{2}$　$\underline{84}$　$\underline{54}$

3. Minimum Horizontal retrace time　$= \underline{11 \times 10^{-6}}$　⑦　f　　$\dfrac{7+2}{532.31 \times 10^{-9}}$　16.907×10^6　④ R3　$\dfrac{R0 - R1}{3}$　$\underline{7}$　$\underline{07}$

4. Minimum vertical retrace time　$= \underline{1 \times 10^{-3}}$　⑧　t_{sl}　$(100+1)(532.31 \times 10^{-9})$　53.76×10^{-6}　⑪ R4　$28 - 1$　$\underline{27}$　$\underline{1B}$

5. # of displayed characters per row　$= \underline{80}$　⑨　n　$\dfrac{1}{(60)(53.76 \times 10^{-6})}$　310　⑫ R5　$R = 2$　$\underline{02}$　$\underline{02}$

6. # of displayed charactor rows　$= \underline{24}$　⑩　N　　　28　⑬ R6　$B6 = 24$　$\underline{24}$　$\underline{18}$

7. # of dots in character dot matrix row　$= \underline{7}$　R　$\dfrac{310}{11}$　2　⑭ R7　Ⓐ　$\underline{25}$　$\underline{19}$

R8　$\underline{0}$　$\underline{0}$

8. # of scan lines in charactor • matrix column　$= \underline{9}$　⑯　t_{cr}　$(9+2)(53.76 \times 10^{-6})$　591.39×10^{-6}　⑮ R9　$(9+2) - 1$　$\underline{10}$　$\underline{0A}$

R10　$\underline{00}$　$\underline{00}$

9. Number of dots between horizontal adjacents　$= \underline{2}$　⑰　t_{hr}　$\leq \dfrac{(101-80)(7+2)}{16.907 \times 10^6}$　11.17×10^{-6}　R11　$\underline{11}$　$\underline{0B}$

R12　$\underline{}$　$\underline{00}$

10. Number of scan lines between vertical adjacents　$= \underline{2}$　⑱　t_{vr}　$\leq \left[\dfrac{18600}{60} - 24(11) \right] 53.76 \times 10^{-6}$　2.47×10^{-3}　R13　$\underline{128}$　$\underline{80}$

R14　$\underline{128}$　$\underline{00}$

Ⓐ $(27+1) - \dfrac{(16-2)}{11} \geq R7 \geq 24$

$26.72 \geq R7 \geq 24$

R15　$\underline{}$　$\underline{80}$

Ⓑ $B2 = 1/[(t_{cr})(R4+1) + (t_{sl})(R5)]$

$= 1/[(591.39 \times 10^6)(28) + (53.76 \times 10^{-6})(2)]$

$= 1/16.667 \times 10^{-3}$

$= 60$

FIGURE 22 — CRTC WORKSHEET

Basic Parameters			Symbol	Intermediate Calculations	Value	Register	Register Calculations	Decimal	Hex
1. Horizontal frequency	=	_____	f'		_____	R0		____	____
2. Vertical frequency	=	_____	t_c		_____	R1		____	____
						R2		____	____
3. Minimum Horizontal retrace time	=	_____	f		_____	R3		____	____
						R4		____	____
4. Minimum vertical retrace time	=	_____	t_{sl}		_____	R5		____	____
						R6		____	____
5. # of displayed characters per row	=	_____	n		_____	R7		____	____
						R8		____	____
6. # of displayed charactor rows	=	_____	N		_____	R9		____	____
						R10		____	____
7. # of dots in character dot matrix row	=	_____	R			R11		____	____
					_____	R12		____	____
8. # of scan lines in charactor • matrix column	=	_____	t_{cr}			R13		____	____
					_____	R14		____	____
9. Number of dots between horizontal adjacents	=	_____	t_{hr}			R15		____	____
					_____	R16		____	____
10. Number of scan lines between vertical adjacents	=	_____	t_{vr}			R17		____	____
					_____	R18		____	____
						R19		____	____

CRTC INITIALIZATION

Register R0-R15 must be initialized after the system is powered up. The processor will normally load the CRTC register file from a firmware table. The program required to initialize the CRTC for a 80 × 24 format (example calculation #2) is shown in Figure 23.

The CRTC registers will have an initial value at power up. When using a direct drive monitor (sans horizontal oscillator) these initial values may result in out-of-tolerance operation. CRTC programming should be done immediately after power up especially in this type of system.

ADDITIONAL CRTC APPLICATIONS

The foremost system function which may be performed by the CRTC controller is the refreshing of dynamic RAM. This is quite simple as the refresh addresses continually run.

Note that the LPSTB input may be used to support additional system functions other than a light pen. A digital-to-analog converter (DAC) and comparator could be configured to use the refresh addresses as a reference to a DAC composed of a resistive adder network connected to a comparator. The output of the comparator would generate the LPSTB input signifying a match between the refresh address analog level and the unknown voltage.

The light-pen strobe input could also be used as a character strobe to allow the CRTC refresh addresses to decode a keyboard matrix. Debouncing would need to be done in software.

Both the VS and HS outputs may be used as a real-time clock. Once programmed, the CRTC will provide a stable reference frequency.

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FIGURE 23 — MC6800 PROGRAM FOR CRTC INITIALIZATION

```
PAGE 001   CRTCINIT.SA:0   MC6845 CRTC Initialization Program

00001                              NAM    MC6845
00002                              TTL    / MC6845-1 CRTC initialization program
00003                              OPT    G,S,LLE=85 print FCB's, FDB's & XREF table
00004                              ****************************************************
00005                       * Assign CRTC addresses
00006                       *
00007         9000  A CRTCAD EQU   $9000       Address Register
00008         9001  A CRTCRG EQU   CRTCAD+1    Data Register
00009                              ****************************************************
00010                       * Initialization program
00011                       *
00012A 0000                        ORG    0           a place to start
00013A 0000 5F                     CLRB               clear counter
00014A 0001 CB 1020  A             LDX    #CRTTAB     table pointer
00015A 0004 F7 9000  A CRTC1       STAB   CRTCAD      load address register
00016A 0007 A6 00    A             LDAA   0,X         get register value from table
00017A 0009 B7 9001  A             STAA   CRTCRG      program register
00018A 000C 08                     INX                increment counters
00019A 000D 5C                     INCB
00020A 000E C1 10    A             CMPB   $10         finished?
00021A 0010 26 F2 0004             BNE    CRTC1       no: take branch
00022A 0012 3F                     SWI                yes: call monitor
00023                              ****************************************************
00024                       * CRTC register initialization table
00025                       * 80 x 24 non-interlaced format
00026A 1020                        ORG    $1020       start of table
00027A 1020    65    A CRTTAB FCB   $64,$50    R0, R1 - H total & H displayed
     A 1021    50    A
00028A 1022    56    A             FCB   $54,$07    R2, R3 - HS pos. & HS width
     A 1023    09    A
00029A 1024    18    A             FCB   $1B,$02    R4, R5 - V total & V total adj.
     A 1025    0A    A
00030A 1026    18    A             FCB   $18,$19    R6, R7 - V displayed $ VS pos.
     A 1027    18    A
00031A 1028    00    A             FCB   $00,$0A    R8, R9 - Interlace & Max scan line
     A 1029    0B    A
00032A 102A    00    A             FCB   $00,$0B    R10,R11- Cursor start & end
     A 102B    0B    A
00033A 102C  0080    A             FDB   $0080      R12,R13- Start Address
00034A 102E  0080    A             FDB   $0080      R14,R15- Cursor Address
00035                              END
TOTAL ERRORS 00000--00000

CRTC1    0004   CRTCAD 9000   CRTCRG 9001    CRTTAB 1020
```

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PACKAGE DIMENSIONS

L SUFFIX
CERAMIC PACKAGE
CASE 715-05
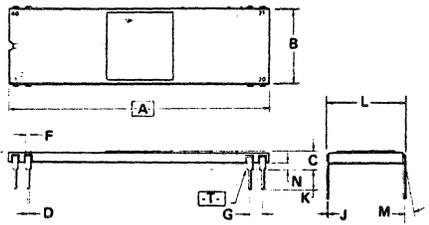
NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

⊕ 0.25 (0.010) Ⓜ T A Ⓜ

3. T IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

| DIM | MILLIMETERS | | INCHES | |
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

S SUFFIX
CERDIP PACKAGE
CASE 734-04
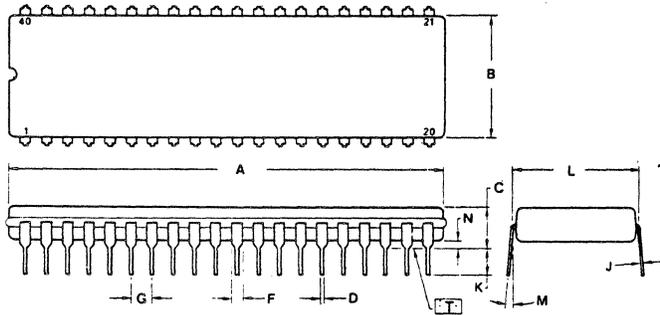
NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:

⊕ ∅ 0.25(0.010) Ⓜ T A Ⓜ

3. T IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

| DIM | MILLIMETERS | | INCHES | |
	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

P SUFFIX
PLASTIC PACKAGE
CASE 711-03
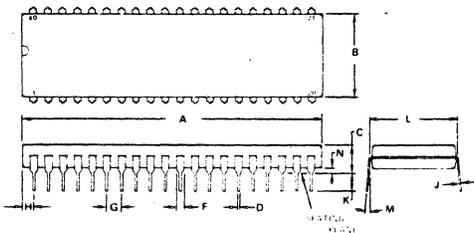
NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | MILLIMETERS | | INCHES | |
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

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   Date of Purchase _____

   Purchased From _____

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   Address: _____

   City _____ State _____ Zip _____

   Name of Technical User _____ Phone Number _____

3. What equipment and software are you using?

   Computer _____   Application Software:

   Operating System _____   _____

   Language _____   _____

4. How did you first learn of our product?

   ☐ Recommendation ☐ Advertisement ☐ News Article ☐ Review Article

   ☐ System/Software Vendor ☐ Brochure

   Name of Magazine/Vendor _____

5. What will you use our product for?

   ☐ Business Graphics

   ☐ Computer Aided Design

      ☐ Electrical ☐ Mechanical ☐ Architectual ☐ Art ☐ Other

   ☐ Video Production

      ☐ Training ☐ Art ☐ Broadcast ☐ Other

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   ☐ Scientific Engineering ☐ Real Time Display

      ☐ Tektronix Emulation ☐ Other

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