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SYSTEMS TECHNOLOGY DIVISION

ENGINEERING SPECIFICATION ES-28-02 REV. A

TITLE PROGRAMMABLE COMMUNICATION UNIT (PCU) (4-Layer)

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NOTE

This specification reports to the following ECO-controlled documents (see the revision correspondence table on page 2): none

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1.0 INTRODUCTION

THE PROGRAMABLE COMMUNICATIONS UNIT (PCU) is an intelligent, microprocessor-controlled communications interface used in several Computervision communications systems. As an intelligent interface, the PCU has the capability to be configured for a variety of applications.

The PCU uses a Z80 microprocessor system consisting of a central processing unit (CPU),a serial input/output device (SIO), a counter timmer circuit (CTC), and a direct memory access controller (DMA). In addition to the Z80 devices, the PCU contains 16k bytes of dynamic Random Access Memory (RAM) and up to 12k bytes of Read Only Memory (ROM). All are Z80A devices operating at a 3.6865 MHZ. clock rate.

The basic PCU is a two port controller. Both ports fully support modems and/or terminals and are EIA RS-232C and/or current loop compatible. In addition, port 0 meets RS-423A specifications. Each port has dedicated CGP device code logic allowing switch-selectable device addresses for individual devices,as well as a unique device code for the Z80 itself.

In anticipation of another controller port being required, a provision is made for a daughter board which will connect to and actually reside on the PCU. The daughter board may contain an entire peripheral controller (such as a floppy disk controller), or several Z80 devices (SIO,DMA), and or additional memory. (See Figure 1-1 PCU Block Diagram)

1.1 Purpose of This Document

The purpose of this document is to aid in the development of CGP software, Z80 software, and hardware interfaces for the PCU board.

1.2 Physical Description and Specifications

1.2.1 Physical description

Dimensions 15" X 15" X 1" (38cm X 38cm X 2.5cm)
Weight 1.75 pounds (0.8 kilograms) approximate

1.2.2 Environmental Specifications

Temperature 32 - 140 deg. F (0 - 60 deg. C)
Humidity 10% - 95% (noncondensing)
Altitude 0 -10,000 feet (0 - 3050 meters)

1.2.3 Electrical Specifications

Power Requirements +5 VDC @ 3A (+ 0.5A)
+12 VDC @ 0.5A
-12 VDC @ 100mA
-5 VDC @ 100mA

1.3 Reference Documentation

EIA Standerd RS-232C
EIA Standard RS-423A & RS-449
DATA GENERAL " HOW TO USE THE NOVA COMPUTER "
Zilog Z80A CPU Technical Manual
Zilog Z80A DMA Technical Manual
Zilog Z80A SIO Technical Manual
Zilog Z80A CTC Technical Manual
ECAB Specification ES-14-36
Current Loop Spec ES-14-32
RS-422 Daughter Board TM-14-110

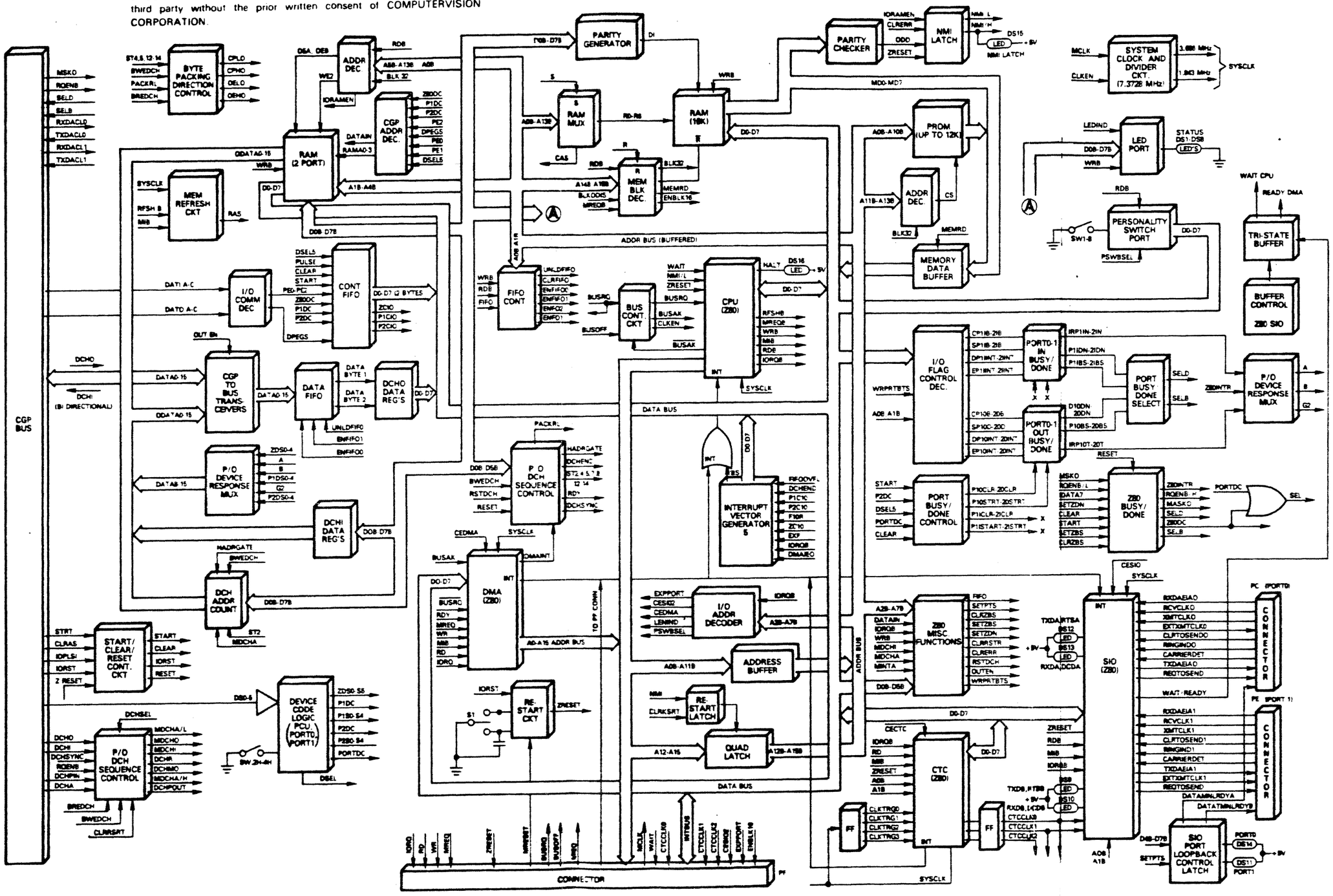


Figure 1-1 PCU BLOCK DIAGRAN

TITLE Programmable Communication Unit (PCU) Specification (4-Layer)	ENGG. NO. ES-28-02	REV. A
	TOTAL SHEETS	SHEET NO. 6

2.0 FUNCTIONAL DESCRIPTION / PERSONALITY MODES

The PCU has three FIRMWARE BASED PERSONALITY MODES of operation: MONITOR MODE, MDB EMULATOR MODE, and 200X MONITOR MODE. All three modes run an Initialization Sequence Diagnostic for testing the board on POWER UP or RESET. MONITOR MODE and 200X MONITOR MODE each have three special functions.

These are: 1) Downline load of application code for execution
2) Diagnostic execution function
3) Debug function

* NOTE : ALL MODES, AND DEBUG FUNCTION, ARE CONFIGURED BY THE USE OF SWITCHES LOCATED ON THE PCU BOARD. (See Section 8.x for switch locations and configurations)

2.1 Initialization Sequence Diagnostic

The PCU Initialization Sequence Diagnostic, tests the basic functions of the PCU board. These self-test diagnostics are initiated in several ways.

1. ON POWER-UP
2. A CGP I/O RESET
3. A CGP NIOP INSTRUCTION TO A NON-Z80 PCU DEVICE CODE
4. DEPRESSING THE RESET SWITCH ON THE PCU BOARD

Tests in the power-on sequence can also run under control of the monitor. During testing, the active port's device code will look "busy" to the CGP. The tests include the following:

1. ROM checksum test
2. SIO Loopback test
3. CGP input RAM diagnostic
4. Z80 dynamic RAM diagnostic
5. DMA memory to memory transfer diagnostics
6. Data Channel Diagnostic (This test is not executed during normal Initialization Sequence)

All self test diagnostic error codes will be placed in sequential locations in the Z80 parameter table, which can subsequently be read by the CGP via DOA and DIA instructions. Abnormal test results will be indicated on the debug port specified by the personality switches. On completion of the self-test diagnostics, the PCU assemes the MODE specified by the personality switches. (Error codes for the test results are given in table 2-6 See section 7. on PCU Status Reporting). On completion of the diagnostics, the PCU assumes the mode specified by the personality switches.

2.2 Monitor Mode

In Monitor Mode,the PCU is waiting for 1 of 2 events to occur:

1. The CGP to issue a PI/O command which the PCU will INTERPRET AND EXECUTE. (See table 2-1 for list of implemented CGP I/O Commands)

2. The user to type a "D" or "control C" on the Debug terminal connected to PCU output port 0 or 1 if selected (See Table 2-2 for implemented Debug Commands).

The CGP PI/O Commands provide two basic functions for the PCU:

1. To allow the transfer of application programs, in HEX Loader Format, from CGP to PCU,for execution (see Figure 2-1 for HEX Loader Format).

2. To allow for execution of diagnostic tests called tasks and check the results (see Table 2-3 for DIAGNOSTIC MODE TEST DEFINITIONS).

NOTE: Diagnostic tasks are also executable from DEBUG TERMINAL.

Parameter Table Conventions - when under the monitor

a) The table is limited in length to ØFF Hex bytes, starting at location 3DØØ in PCU RAM.

b) When used to log errors during the self test diagnostic, the parameter table location following the last error code entry will be 0, to indicate that this was the last error encountered.

c) When the Z80 receives a CGP I/O command instructing it to transfer an application program in HEX Loader format, the parameter table will be destroyed.

In MONITOR MODE two pairs of devices codes are enabled. The Z80 device code pair (input/output) and either port 0 or 1's device code pair. Under the monitor, only CGP PI/O commands to the Z80 device codes are recognized, all others are ignored.

2.2.1 Debug Mode

The prompt % is sent to the debug port when the monitor is started. The monitor has debug capability similar to Debug I: one breakpoint, read/modify RAM, read/modify registers (see Table 2-2 for DEBUG COMMAND LIST).

NOTE: While in DEBUG MODE, Z80 interrupts are disabled.

2.2.2 Diagnostic Mode

Diagnostic Mode can be entered by executing tasks via Debug Mode (see Table 2-4 for Debug Diagnostic Task Definitions) or by CGP PI/O commands to the Z80 Port device codes. (se Table 2-1 for CGP PI/O commands).

2.3 MDB Emulator Mode

The MDB EMULATOR MODE operates as two asynchronous serial I/O ports per Data General Reference Manual ("How to use the Nova"). Only mask bit 7 is supported on the PCU. The standard mask bits associated with the MDB board, 14 & 15, are not supported.

2.4 200X Monitor Mode (200X Mode)

200X MONITOR MODE functions are the same as MONITOR MODE with the following exceptions:

1. The Z80 PORT device code pair is disabled.

2. CGP PI/O commands are sent to either PORT 0 or 1, whichever is enabled.

3. PCU 200X Monitor mode is used only in CGP-200X systems (i.e. with ICP, EACPU, and EAMAP).

Table. 2-1. CGP to PCU Programmed I/O Commands
(These commands will be implemented in PCU Firmware)
For Monitor Mode or 200X Monitor Mode

1. IORST is the normal hardware PCU restart. Port busy is set during diagnostic and cleared at end.

2. NIOP to the Z80 port (monitor mode only) is the software restart of the PCU operating mode with no self-test diagnostic. Done will be set and Busy cleared upon completion of the restart. An NIOP to port 0 or 1 device code in any mode will result in a hardware reset of the PCU as in IORST.

3. NIOC is the software restart of the PCU operating mode with no self-test diagnostic. DONE will be set and BUSY cleared upon completion.

4. DOA AC, PCU (input or output device code) initiates PCU Diagnostic FUNCTION defined in Table 2-3. BUSY is set during task; DONE set, BUSY cleared on completion of most functions.

5. DOAS AC, PCU (input or output device code). Starts Z80 execution at address specified in AC. BUSY set by hardware, not normally cleared.

6. DOAP AC, PCU. AC specifies the logical Z80 RAM address of transfer. Device code specifies direction of transfer. No change to BUSY or DONE.

7. DOB AC, PCU. Performs a data channel transfer in hex loader format. AC specifies logical CGP address of transfer. Direction of transfer is always from CGP to PCU with byte packing as in DOBP. No change to busy or done. (See Figure 2-1 for the HEX loader format)

8. DOBP, AC PCU. Specifies a data channel transfer of raw data (i.e., data not in Mostek format, packed first byte in left half, 2 bytes to a CGP word). AC specifies CGP address of transfer. Device code implies the direction of transfer; output device code indicates CGP to PCU transfer whereas input device code refers the PCU to CGP transfer. No change to busy or done.

9. DOCS AC, PCU (input or output device code). AC specifies the byte count for the data channel transfer. The 'S' signal starts the transfer. The transfer is actually word oriented. Both bytes in the word are always transferred. Busy set in hardware during XFR: done set, busy cleared on completion. On a DMA/DCH BLK XFER, an even byte count must be specified. This XFERs even # of bytes to DCH. If DCH receives odd # of bytes, it will never go done and will hang.

10. DIA AC, PCU (retrieves 'A' register which contains information specified by a previous DOA. (see Table 2-3)

11. DIB AC. PCU. Contains PCU identification information used under application software. Also used in FIFO wrap around test.

12. DIC AC, PCU (input or output device code). Retrieves 'C' register which contains Z80 status information, (see Table 2-5).

13. The mask out signal with bit 7 set to 1 from the CGP will mask out the entire PCU. This includes Z80 Port, Port 0, Port 1. If the bit 7 is not set, it will clear the mask for all the PCU Ports. The mask out COMMAND will not get LOADED into the PCU FIFO.

In addition to the above firmware functions, the following hardware functions will occur: S will set busy and clear done; C will clear both busy and done. Standard CGP programming conventions should be observed. A busy device should not be used unless the current task needs to be terminated.

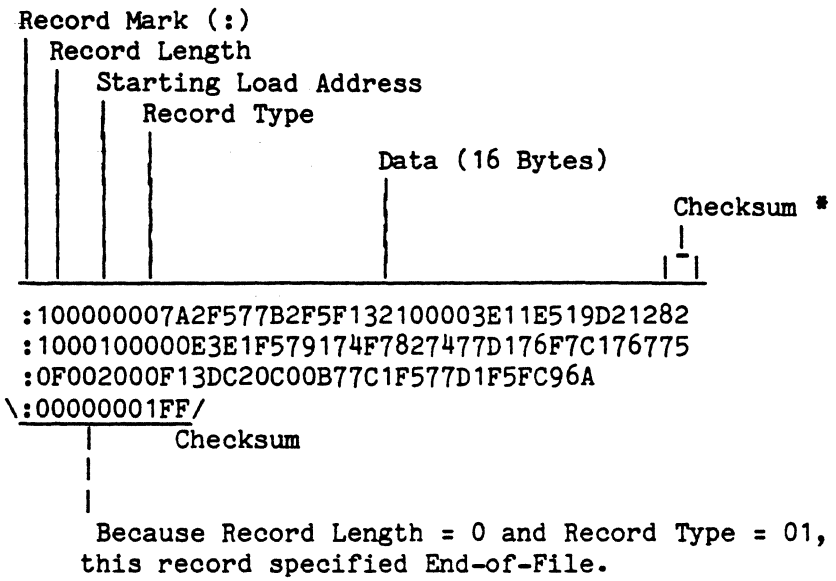


Figure 2-1. Format for Absolute Hex Loader

* The checksum field contains the ASCII hexadecimal representation of the twos complement of the 8-bit sum of the 8-bit bytes that result from converting each pair of ASCII hexadecimal digits to one byte of binary, from the record length field to and including the last byte of the data field. Therefore, the sum of all the ASCII pairs in a record after converting to binary, from the record length field to and including the checksum field, is zero.

Table 2-2. PCU Debugger Command Summary

Command	Definition
HHHH/	Open memory location HHHH
/	Examine last memory location opened-address not displayed
$/	Display address and examine last memory location opened
LF(Linefeed)	Open next memory location
/\	Open previous memory location
RAA/	Open register AA
R'AA	Open register AA'
R/	Examine all register (no header)
R1	Examine all registers (with header)
HHHH$X	Execute from location HHHH*
HHHH$B	Insert breakpoint at location HHHH**
$B	Remove breakpoint
$C	Continue from breakpoint
HH$P	Open port HH+
HH$T	Execute task HH
$|	Initialize CPU, then enter monitor mode with no diagnostic execution
CRTL C	Break -- return to debugger

* Typing 9006$X causes full power-on diagnostic sequence plus a complete data channel test to be executed.

** Care must be taken when using the breakpoint feature of the debugger. HHHH$B replaces the contents of HHHH, HHHH+1, and HHHH+2 with a 3 byte call to the breakpoint routine. If these locations contain Data Values used by the program being breakpointed, it may not operate correctly. The original values are restored if the breakpoint is reached or removed with $B. Breakpoint at location 0000H is not allowed.

\+ If a change is desired, enter the new value followed by (CR) to write new value into the port.

NOTES

H = hexadecimal input
AA = ASCII designation of Z80 register pair
$ = escape key on debug terminal

Table 2-3. PCU Diagnostic Mode Test Definitions

AC CONTENTS (HEX)	FUNCTION
0000	NULL: set DONE, clear busy when complete
1000	Normal PCU monitor restart as in power-up. Normal diagnostic execution. Set BUSY during restart; clear BUSY on completion.
2000	PCU restart with full diagnostic execution. Includes a diagnostic execution which tests full Data channel capability by writing and reading from a block of CGP memory. Also includes manual intervention test such as the SIO diagnostic. Set BUSY during exeuction, clear BUSY when complete.
3000	PCU restart without diagnostic execution. (Same as NIOC). Set BUSY during exeuction; clear BUSY, set DONE on completion.
4000	Unused
50XX	Execute a Z80 task specified by XX and set BUSY. Clear BUSY when task finishes. (see table 2-4 for task definitions)
6YXX	Write XX to the parameter table, where Y is the parameter table index, and set BUSY. Clear BUSY and set DONE when finished.
7Y00	Execute the contents of the parameter table (Y = parameter table index) as a Z80 instruction, and set BUSY. Clear BUSY, set DONE on completion.
8000	Terminate SIO loopback mode. Clear BUSY and set DONE.
8001	Initiate SIO loopback mode. Clear BUSY and set DONE.
8002	Initiate FIFO wrap around to CGP registers A & B. Clear BUSY and set DONE when complete. This is a one-shot mode only.
8003	Initiate FIFO overflow condition. Z80 goes to wait loop, clears BUSY when finished.
90YY	Load the parameter table contents (YY - parameter table index) into the CGP 'A' register (low order). This would, for example, allow the CGP to examine all diagnostic error encountered by the PCU Z80 during diagnostic execution. Set DONE and clear BUSY when complete.

Table 2-3. PCU Diagnostic Mode (continued)

AC CONTENTS (HEX)	FUNCTION
A0XX	Examine the PCU address specified in XX (low address) and YY (high address). The CGP will first issue a DOA with AC = A0XXH, then a DOA with AC = A1YYH. After receiving the last PIO command (A1YY), the Z80 will place the contents of the specified location into the 'A' register (low order). Clear BUSY and set DONE when finished.
B000	UNUSED
F000	

Table 2-4. Diagnostic Task Definitions

Task No. (HEX)	Task Name	Function	Comments
0	RTNTSK	Return	NOP
1	SITSK1	SIO loopback diagnostic, S10-1A	
2	SITSK2	SIO loopback diagnostic, S10-1B	
3	CRMDIA	CGP input RAM diagnostic	
4	ZRMDI1	Z80 RAM diagnostic-HILIM = PAROR	Checks memory up to but not including parameter table.
5	ZRMDI2	Z80 RAM diagnostic-HILIM = ACDAT	Set stack ppointer = 801C prior to invoking this task.
6	DMTSK1	RAM diagnostic	
7	DCTSK1	Data channel diagnostic	
8	DIALOP	Loop on all self test diagnostics	Tasks 1,2,3,4,6,7
9	SIOLOP	Loop on SIO internal wraparound	
A	ZRM1LP	Loop on task 4 (ZRMDI1)	Restart PCU to exit
B	ZRM2LP	Loop on task 5 (ZRMDI2)	
C	CRMLP	Loop on task 3 (CRMDIA)	
D	DAMLOP	Loop on task 6 (DMTSK1)	
E	DCLOPW	Loop on task 10 (DCHIW1)	Wipes out CGP memory
F	DCLOPB	Loop on task 12 (DCHIB1)	
10	DCHIW1	Single DCH input word transfer	
11	DCHOW1	Single DCH output word transfer	CGP MUST BE IN RUN
12	DCHIB1	Single DCH input block transfer	STATE
13	DCHOB1	Single DCH output block transfer	
14	SEDTSK	Set done, clear busy on all DC	
15	FFWRTS	FIFO wraparound task	Wraps FIFO contents to CGP A and B registers.
16	PTBINI	Clear parameter table	Continues to task 17 when done.
17	STAINI	Initialize status word and lights	
18	CLMTSK	Clear SIO wrap and FIFO wrap modes	
19	SEBZTS	Set busy on Z80 device code	
1A	SDZ8TS	Set done on Z80 device code	
1B	SIDP1T	Set port 0 input done	
1C	SODP1T	Set port 0 output done	
1D	SIDP2T	Set port 1 input done	
1E	SODP2T	Set port 1 output done	
1F	DIIP1T	Disable port 0 input interrupts	

Table 2-4
Debug Mode Task Definition (continued)

Task No. (HEX)	Task Name	Function	Comments
20	EIIP1T	Enable port 0 input interrupts	
21	DOIP1T	Disable port 0 output interrupts	
22	EOIP1T	Enable port 0 output interrupts	
23	DIIP2T	Disable port 1 input interrupts	
24	EIIP2T	Enable port 1 input interrupts	
25	DOIP2T	Disable port 1 output interrupts	
26	EOIP2T	Enable port 1 output interrupts	
27	CBSYTS	Clear all busy bits on all ports	
28	RTNTSK	Return	NOP
29	RTNTSK	Return	NOP
2A	STSILP	Initiate SIO loopback mode	
2B	FFWRMD	Initiate FIFO wraparound mode	
2C	FLFIFO	Flush entire contents of FIFO	
2E	RTNTSK	Return	NOP
2F	RTNTSK	Return	NOP
30	SIEXT0	External SIO wraparound, port 0	
2F	SOEXT1	External SIO wraparound, port 1	

Table 2-5. PCU Status Definitions

VALUE HEX	DESCRIPTION
1	PCU O.K. - Diagnostic completed without failure
2	PCU soft failure - For example, loader format error, FIFO overflow.
4	PCU Hard failure - For example, RAM diagnostic or Data channel error.
8	Z80 in maintenance mode
10	Z80 Halted
20	PCU waiting for CGP command
40	Memory Parity Error
80	Reserved for errors
100	multiple soft errors
200	multiple hard errors
400	Hex loader format error
800	Hex loader data error
1000	Hex loader checksum error
2000	FIFO overflow

The low order status byte is displayed in the LED register.

Status is also read by CGP DIC to Z80 Device Code in Monitor mode or DIC to Port 0 or 1 in 200X monitor mode.

Table 2-6. Self Test Result Error Codes
(Found in Z80 parameter table)

CODE (HEX)	NATURE OF ERROR
81	ROM CHKSUM
85	Dynamic RAM data Pattern
86	Dynamic RAM Addressing
87	CGP input RAM data test
88	CGP input RAM address test
91	CTC TEST
9B	SIO special condition
9F	SIO Register Read
A0	SIO-1A Data Loopback (port 0)
A1	SIO-1B Data Loopback (port 1)
A2	SIO Timeout
A3	DMA Register Read
A4	Timeout on DMA done
A5	DMA Data Transfer
A7	Data Channel Block Transfer
A8	Timeout on DCH DONE
A9	Data Channel Block Transfer
B1	Loader format error
B2	Loader data error
B3	Loader checksum error

NOTE: When there is an error reported in the status/error LED;s the Most Significant Bit (MSB, LED DS1) will be lit.

3.0 MEMORY

The memory address space of the Z80 CPU is limited to 64K bytes of memory. The following sections discuss the allocation of this space on the PCU.

3.1 Memory Map

Figure 3-1 shows a block diagram that outlines the entire memory section. The user memory (16K dynamic RAM) has been allocated the space between addresses 0000H and 3FFFH. The next 16K block (4000H-7FFFH) is assigned for future RAM expansion. In the memory space 8000H-801FH resides the CGP input RAM. This is a status RAM, 32 bytes long. The Z80 can read and write in this RAM. The CGP can also read from it simultaneously two bytes (one word) from adjacent locations. The support firmware for PCU (12K PROM) resides in the memory space 9000H-BFFFH. The remaining 16K block (C000H-FFFFH) is reserved for future RAM or PROM expansion.

3.2 ROM Program

The ROM program contains the firmware to support all the personality modes and functions of the PCU board including the debugger and diagnostic functions. The revision level and ROM number (i.e., 0, 1, 2, 3, etc) will be contained in each ROM and ink stamped on the ROM. It will be readable by both the debugger and CGP. ROM 5 contains the hardware revision level of the PCU board.

Table 3-1 shows the location of each of these parameters in each ROM.

Table 3-1. ROM Number and Revision Level Address

ROM	(HEX) ADDRESS RANGE FROM	TO	(HEX) REVISION ADDRESS	(HEX) IDEN ADDR
0	9000	97FF	9003	9004
1	9800	9FFF	9800	9801
2	A000	A800	A050	A051
3	A800	AFFF	A800	A801
4	B000	B7FF	B000	B001
5	B800	BFFF	B800	B801

3.3 RAM

Figure 3-2 shows a block diagram of the user memory (16K dynamic RAM). 512 bytes (memory space 3C00H-3DFFH) of this memory block is used for converting the input data from CGP, which is in Mostek Loader format to Binary Code. Memory space 0000H - 3BFFH's used for application programs. the PCU stack is located 3E00H to 3EFF. Interrupt vectors are contained at 3F00H to 3F7FH and firmware storage is located at 3F80H to 3FFFH.

3.3.1 Parity

The dynamic RAM has odd parity which is generated and checked by the hardware. Parity failure results in a non-maskable interrupt (NMI) to the Z80 CPU which causes the Z80-CPU to attempt to restart at location 0066(Hex). The NMI sets a restart latch which forces the Z80 to execute at location 9066 in PCU Firmware. The PCU firmware puts the error status (55 Hex) into the CGP 'C' register low order byte then halts with Z80 interrupts enabled for CGP or Debug Mode interrogation of the PCU.

NOTE: When the PCU Halts, Busy will remain set on the PCU Device Code Active at the time of the error. This is a hard failure and the PCU must be reset i.e. IORST or NIOP.

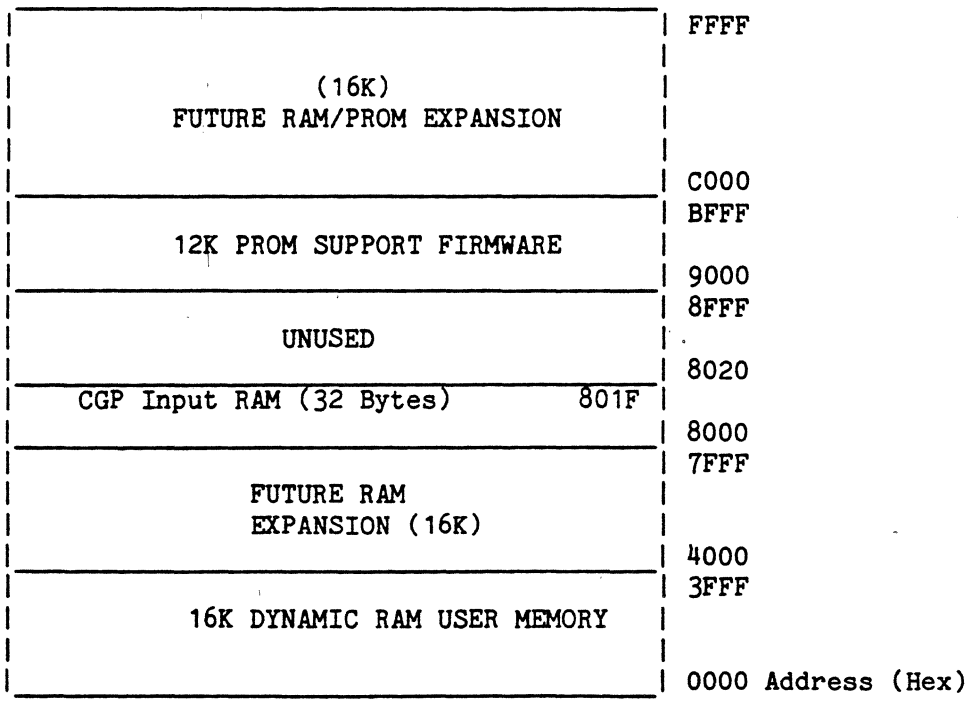


Figure 3-1. PCU Memory Map

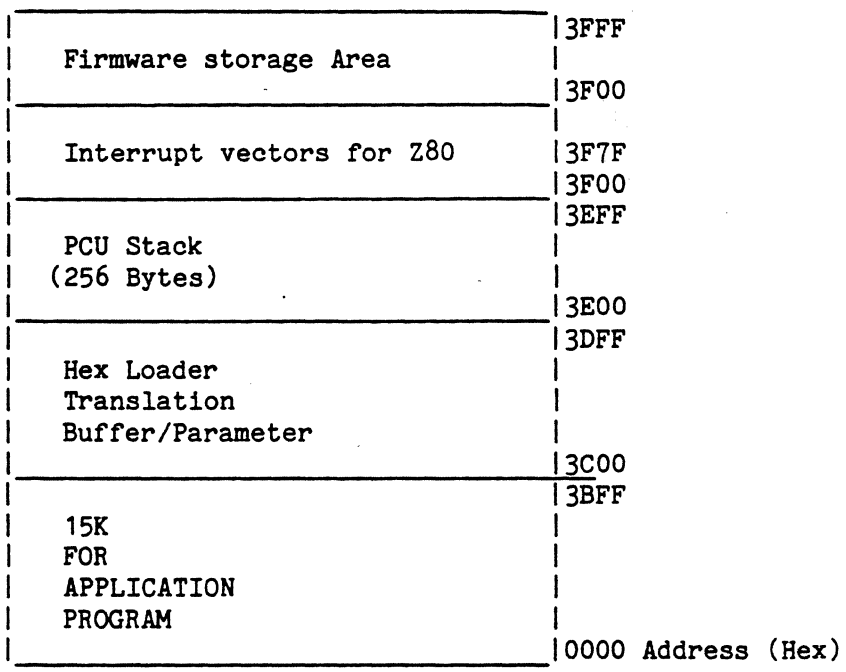


Figure 3-2. Map Of 16K Dynamic RAM

4.0 PCU/CGP HARDWARE INTERFACE

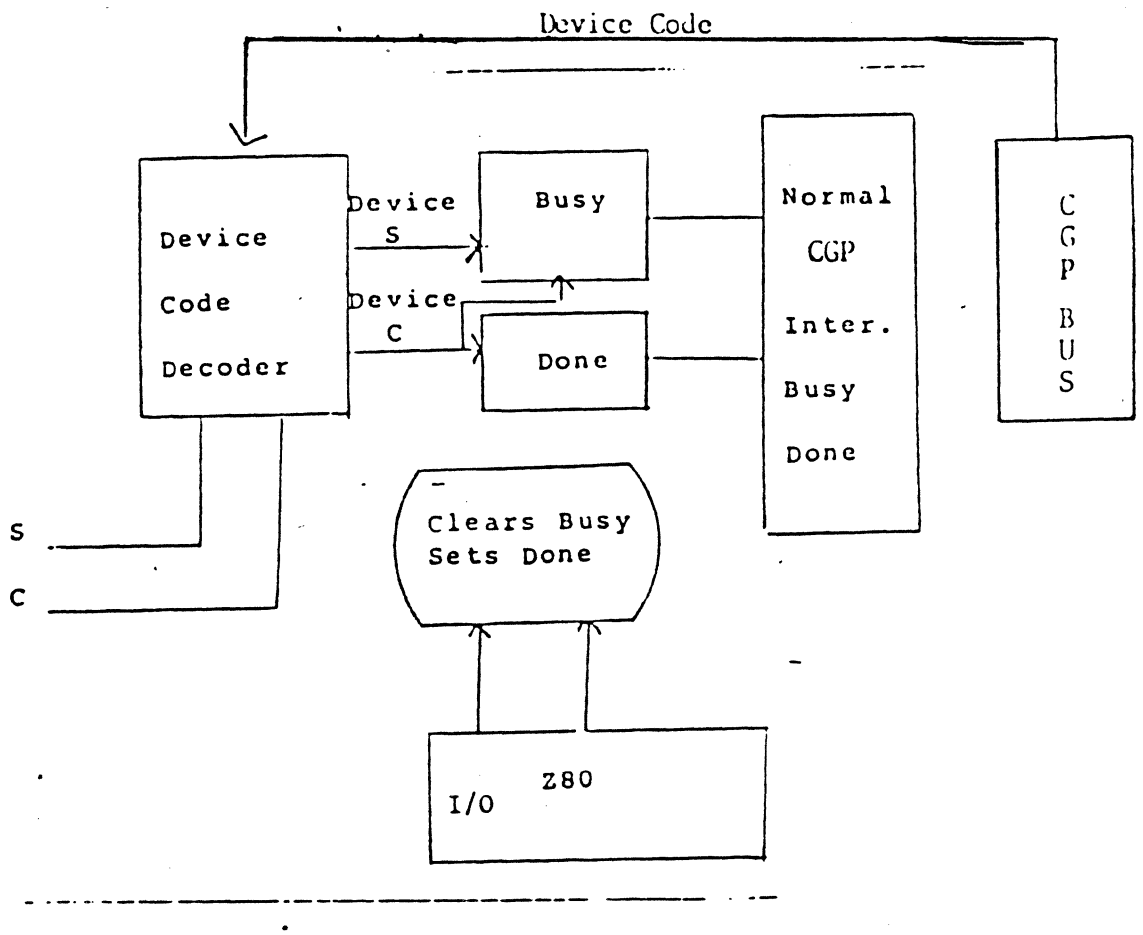
The PCU/CGP HARDWARE INTERFACE consists of Device Code logic, Busy/Done logic,Programed I/O and interupt logic,Data Channel and interupt logic, and all associated hardware. (see Figure 1-1 PCU Block Diagram)

4.1 Device Codes

The PCU has three CGP addressable ports, each port has a device code pair switch selectable from 00/01 to 76/77. The even device code is the CGP input address, the odd device code is the CGP output address. (Device code selection is shown in section 8.2)

4.2 BUSY/DONE

Each device code assigned to the PCU has standard CGP busy/done logic (see figure 4-1), except the Z80 device code pair which has only one set of busy/done logic.



S Sets busy, clears done

C Clears busy, done

P Special

Figure 4-1 BUSY DONE

4.3 CGP To Z80 Via Programmed I/O

Program I/O transfers from the CGP to the Z80 pass thru a FIFO. Each trasnfer consists of 16 bits of data plus encoded ID, signified to Z80 by a vectored interrupt. The address of the vectored interrupt directly indicates to the Z80 the identity of the port (see table 4-1). The Z80 must interpret the data Format described below. In case the programed I/O, input FIFO goes full, the Z80 will receive an interrupt. Its program should cause an error interrupt to the CGP by the Z80 device going DONE (Active Port Device Code if 200X Mode). The status in the C register will indicate fatal error condition. Data entering the FIFO in association with DOA, B, C or NIO, has direct hardware support which translates the associated device code into a port designator encoded in byte 1, and the CGP condition causing the interrupt encoded in byte 2. (Figure 4-2 shows the input FIFO.)

Table 4-1. Z80 Interrupt Vectors

DEVICE OR FUNCTION	INTERUPT VECTOR (HEX)
FIFO overflow	00
DCH end	04
Expansion port (piggy back)	06
PORT 0 CGP I/O	08
PORT 1 CGP I/O	0A
Z80 CGP I/O	0C
CTC 1	20
CTC 2	22
CTC 3	24
CTC 4	26
DMA controller	28
SIO 1B (port 1)	30
SIO 1A (port 0)	38
*SIO 2B (port 3)	40
*SIO 2A (port 2)	48

*If SIO 2 is used on piggyback board

The interrupt vector is the low order byte of the interrupt address. The I-register supplies the high order byte.

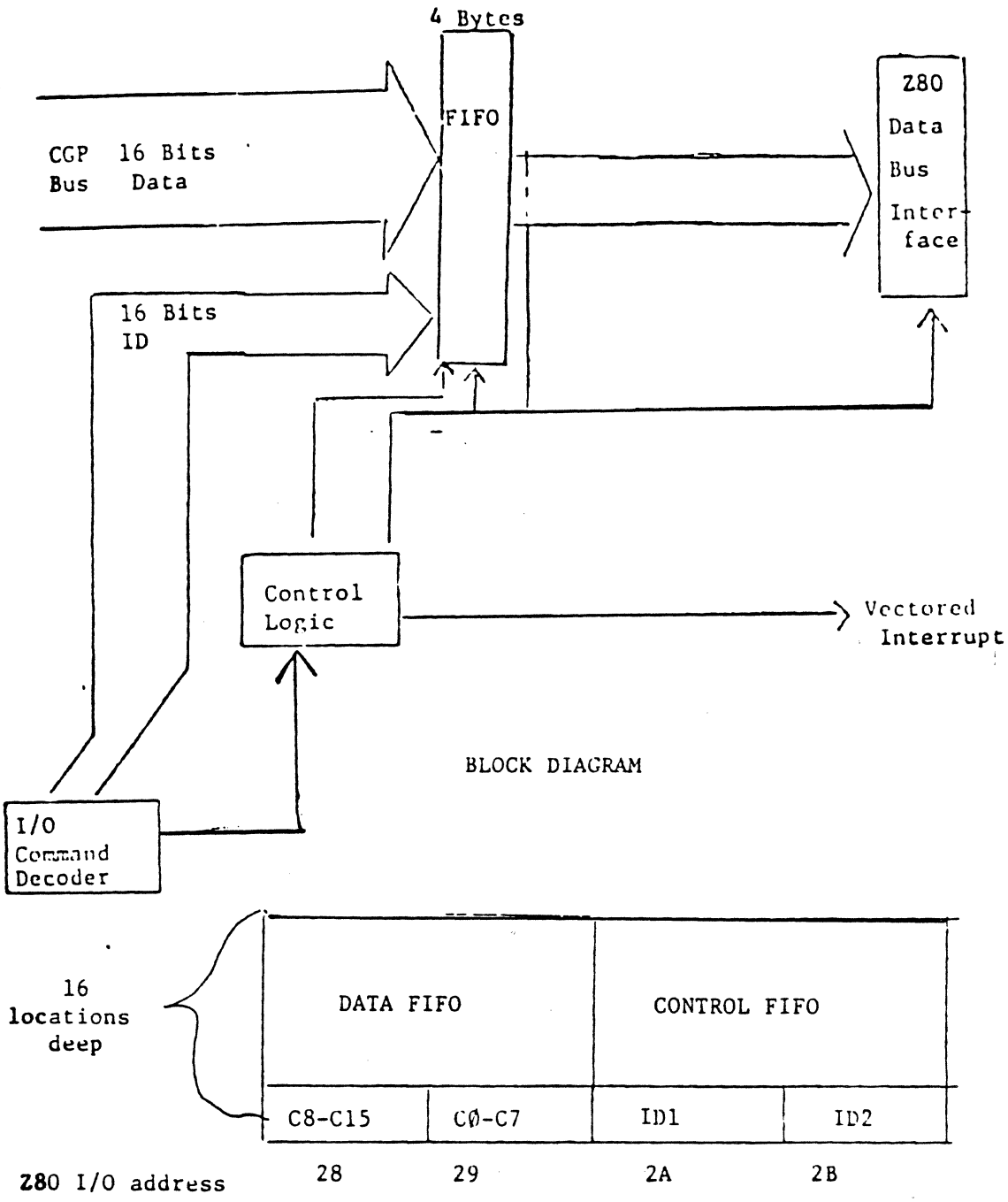


Figure 4-2. INPUT FIFO

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	TOTAL SHEETS	SHEET NO. 25

4.3.1 FIFO DATA FORMAT

1. The FIFO can be read as four sequential Z80 I/O ports as follows:

I/O Address 28 data, CGP bits 8-15
I/O Address 29 data, CGP bits 0-7
I/O Address 2A encoded ID, byte 1
I/O Address 2B encoded ID, byte 2

NOTE: All Z80 I/O device addresses can be found in Table 4-2

2. After the FIFO contents have been read the FIFO data in all four FIFO locations must be advanced by writing to Z80 I/O Device Address 28. The entire FIFO contents can be cleared by writing to 29 or by IORESET (NIOP to port 0 or 1 device code) from the CGP. This is not normally required since the FIFO is automatically cleared, when power is first applied, as part of the hardware power-up sequence.

3. ENCODED ID BYTE 1

bit 0 Z80 DC
bit 1 Port 0
bit 2 Port 1
bit 3 Not Used
bit 4 Link bit
bit 5 Not Used
bit 6 Not Used
bit 7 Not Used

4. ENCODED ID BYTE 2

bit 0 Port Direction: 0 = CGP input device 1 = CGP output device
bit 1 Encoded I/O Instruction
bit 2 Encoded I/O Instruction
bit 3 Encoded I/O Instruction
bit 4 P (Pulse)
bit 5 C (Clear)
bit 6 S (Start)
bit 7

	3	2	1
NIO	0	0	0
DIA	0	0	1
DIB	0	1	0
DIC	0	1	1
Not Used	1	0	0
DOA	1	0	1
DOB	1	1	0
DOC	1	1	1

If an S, P, or C pulse is present with the current PIO instruction, bits 4, 5, & 6 of ID byte 2 will be in the next FIFO location. In addition, the link bit will be set at this time. (Next FIFO location). For example, suppose the following PIO instruction is issued:

DOBP 2, Z80 device code (INPUT)

The FIFO will contain the following information:

	ID BYTE 1	ID BYTE 2	AC2 HI	AC2LO
BIT #	76543210	76543210		
NEXT FIFO LOC	XXX1X001	XXX1XXXX		
CURRENT FIFO LOC	XXX0X001	XXXX1100		

X = Don't Care

Table 4-2. Z80 I/O Device Address

DEVICE	Z80 I/O ADDR (HEX)	READ FUNCTION	WRITE FUNCTION
CTC 1	00		
CTC 2	01		SEE CTC TECH. MAN.
CTC 3	02	N/A	PROGRAMMING
CTC 4	03		EXAMPLE
PORT 0	04	RCVR DATA	XMTR DATA
(SIO 1 A)	05	COMMAND REG.	COMMAND REG.
PORT 1	06	RD REG	TRMT DATA REG.
(SIO 1 B)	07	COMMAND REG.	COMMAND REG.
SUBASSEMBLEY	0C		
PORT	0D	UNASSIGNED	UNASSIGNED
	0E		
	0F		
DCH CONTROL	10	N/A	MODE & CGP ADDRESS
DMA CONTROLLER	14	See Z80 - DMAC Spec	
DSR/LED INDICATOR	18	Port 1 DSR	LED STATUS REG
PORT PERSONALITY SWITCHES	1C	See Sect. 8	N/A
Z80 MISC FUNCTION*	20	N/A	BUSY, DONE MISC
PORT 0 CGP I/O STATUS *	24	N/A	BUSY, DONE *
PORT 1 CGP I/O STATUS *	25	N/A	BUSY, DONE *
INPUT FIFO	28	DATA BYTE 1	FLUSH CURRENT WORD
INPUT FIFO	29	DATA BYTE 2	RESET FIFO
INPUT FIFO	2A	ID BYTE 1	N/A
INPUT FIFO	2B	ID BYTE 2	N/A
SIO CONTROL *	2C	N/A	LOOP BACK, DTR,

* FOR ENCODING SEE TABLE 4-3

NOTE 1: Due to block decoding technique in the hardware, the following device addressed (in Hex) should never be used.

11, 12, 13, 15, 16, 17, 1D, 1E, 1F, 21, 22, 23

Table 4-3. Bit Encoding For Various Control Functions

	BIT	DEVICE ADDR: 20 HEX Z80 Miscellaneous Functions	DEVICE ADDR 24 HEX Port 0 CGP I/O Status	DEVICE ADDR 25 HEX Port 1 CGP I/O Status	DEVICE ADDR 2C HEX SIO Control
LSB	0	Clear Z80 CGP Busy FF	Clear Port CGP Input BUSY	Clear Port CGP Input BUSY	
	1	Set Z80 CGP Busy FF	Set Port 0 CGP Input DONE	Set Port 1 CGP Input DONE	
	2	Set Z80 CGP DONE FF	* Disable Port 0 CGP Input Interrupt	* Disable Port 1 CGP Input Interrupt	
	3	Clear Z80 Restart FF & DCH Int.	* Enable Port 0 CGP Input Interrupt	* Enable Port 1 CGP Input Interrupt	
	4	Clear Z80 Memory Parity FF Reset Z80 FIFO Overflow FF	Clear Port 0 CGP Output BUSY	Clear Port 1 CGP Output BUSY	Data terminal ready SIO 1A Port 0 1 = ON Ø = OFF
	5	Data Channel Reset	Set Port 0 CGP Output DONE	Set Port 1 CGP Output DONE	Data terminal ready SIO 1B Port 1 1 = ON Ø = OFF
	6	N/A	* Disable Port 0 CGP Output Interrupt	* Disable Port 1 CGP Output Interrupt	Loopback SIO 1A & 2A
MSB	7	N/A	* Enable Port 0 CGP Output Interrupt	* Enable Port 1 CGP Output Interrupt	Loopback SIO 1B & 2B

*NOTE: Performing disable and enable interrupt on the same port at the same time is not a valid operation and will have unpredictable results.

which way is output/input? CGP → PCU

PCU → CGP

4.4 Z80 To CGP Via Programmed I/O

All PIO output from the PCU to CGP is implemented by virtue of the Z80 via its memory bus to dedicated memory locations.

1. Each port has a set of six 16-bit registers that can be read by the commands DIA, DIB, and DIC. One set for the input device code, one for the output device code. The Z80 device code has only three registers.

2. The I/O addressing (8000H to 801FH) uses a logical scheme incorporating port ID and the encoded register ID. Each 16 bit register can be addressed by the Z80 as two sequential bytes, the first being the left byte, second the right. This is shown in Table 4-4 Input RAM Addresses.

3. A block diagram of the Z80 to RAM to CGP data flow is shown in Figure 4-3. Figure 4-1 illustrates how the Z80 establishes the desired Nova busy/done states in conjunction with these data transfers.

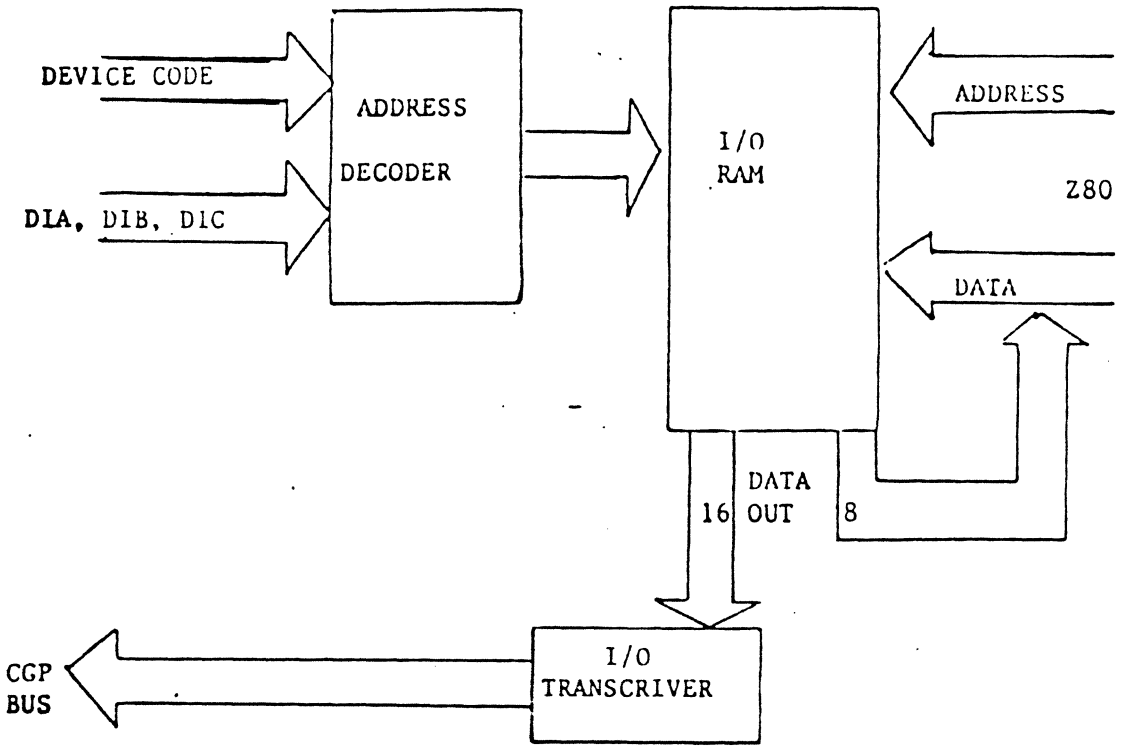


Figure 4-3 Input Ram - Z80 to CGP Data Flow

Table 4-4. CGP Input Ram Addresses

DEVICE/REGISTER	Z80 LOGICAL ADDRESS (CGP LEFT BYTE)	Z80 LOGICAL ADDRESS (CGP RIGHT BYTE)	CGP SIDE Ram Addr.
Z80 DIA both odd & even	8000	8001	00
Z80 DIB device codes read	8002	8003	01
Z80 DIC same registers	8004	8005	02
Port 0 DIA Even Device Code	8006	8007	03
Port 0 DIB Even Device Code	8008	8009	04
Port 0 DIC Even Device Cdoe	800A	800B	05
Port 0 DIA Odd Device Code	800C	800D	06
Port 0 DIB Odd Device Code	800E	800F	07
Port 0 DIC Odd Device Code	8010	8011	08
Port 1 DIA Even Device Code	8012	8013	09
Port 1 DIB Even Device Code	8014	8015	0A
Port 1 DIC Even Device Code	8016	8017	0B
Port 1 DIA Odd Device Code	8018	8019	0C
Port 1 DIB Odd Device Code	801A	801B	0D
Port 1 DIC Odd Device Code	801C	801D	0E
Not Used	801E	801F	0F

* The CGP output device has the odd device code, input device the even. The RAM address on the CGP side is generated by a PROM from the encoded "data-in" command plus device addressed.

4.5 Data Channel

The vehicle for controlling transfers of data to (DCH I) or from (DCH0) the CGP is the data channel controller (see figure 4-4).It has two modes of operation to provide a direct path between Z80 memory and CGP memory. Acting alone it provides for single word transfers. In conjunction with the Z80/DMA controller it allows block transfers.

The control byte is used to specify block or single word mode, DCHI or DCH0, data byte packing direction, AND DMA/SIO transfers. The first time a transfer is attempted, a DCH clear must be given by writing bit 5 = 1 to the Z80 miscellaneous function I/O address 20H, before the DCH controller setup is started. (see Figure 4-5 for Control Byte Encoding)

1. DCH0 - 3 bytes in case of single transfer of word

   1st byte - control byte (bit 2 = 0), DMAC is not used
   2nd & 3rd byte - CGP Address

   3 bytes in case of block transfer

   1st byte - Control of byte (bit 2=1), DMAC is set up
   2nd and 3rd byte - CGP Address
   Block length is implied by DMA End Signal

2. DCHI - 5 bytes in case of single transfer of word

   1st byte - control byte (bit 2 = 0), DMAC is not used
   2nd and 3rd byte - CGP Address
   4th and 5th byte - data

   3 bytes in case of block transfer

   1st byte - Control byte (bit 2 = 1), DMAC is set up
   2nd and 3rd byte - CGP Address
   Block length is implied by DMA End Signal

NOTE: The CGP address is always given with the low order byte first, followed by the high order byte.

4.5.1 Z80 SINGLE WORD TRANSFER MODE

The single word mode allows transfers of two data bytes between Z80 memory and CGP memory. It requires a three byte setup for each single word transfer. These bytes specify control functions (first byte) and CGP address (next two bytes). These are followed by the data bytes, if its DCHI. At the end of the transfer the DCH controller interrupts the Z80. At that time, if it was DCH0, the Z80 can read the two data bytes. All reads and writes by the Z80 to the DCH controller are via I/O device address 10(H). The interrupt vector generated is 04H.

4.5.2 DMA Block Transfer Mode

The block mode requires setup of not only the DCH controller, but also the Z80/DMA controller. It does not matter which is started first, since the READY line is activated by the DCH controller only after setup is complete. The same type of three byte setup is required by the DCH controller as in single word mode, except that data bit 2 must be set= 1 in the control byte. This specifies block mode. Once the setup is complete (i.e., both devices started) the data transfer between Z80 memory and the DCH controller is handled by the Z80/DMA controller. When the transfer is completed the Z80/DMA controller will interrupt the Z80/ CPU. This is sensed by the DCH controller and it will interrupt immediately, if DCH0, or after completing the last transfer, if DCHI.

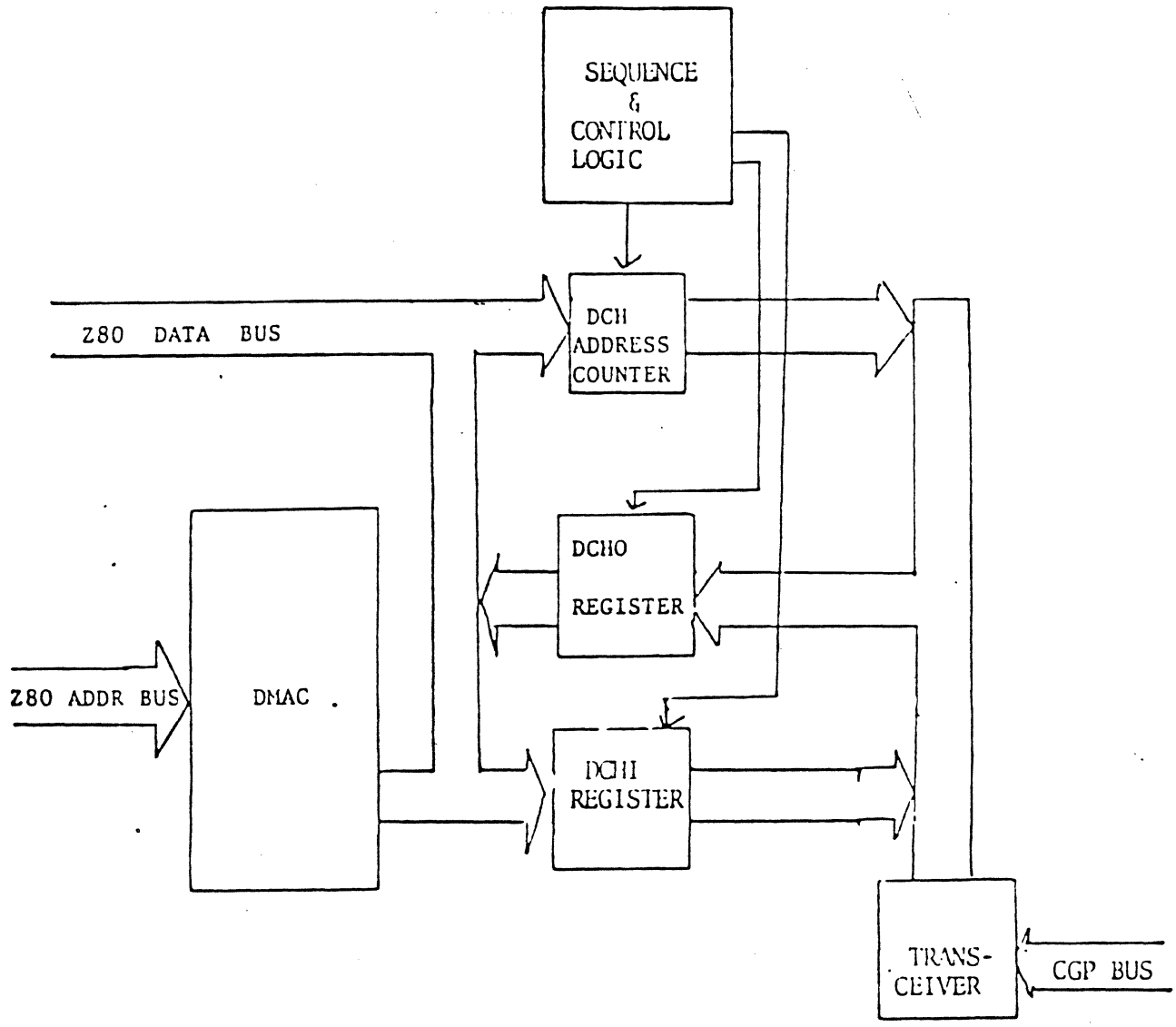


Figure 4-4 Data Channel Controller

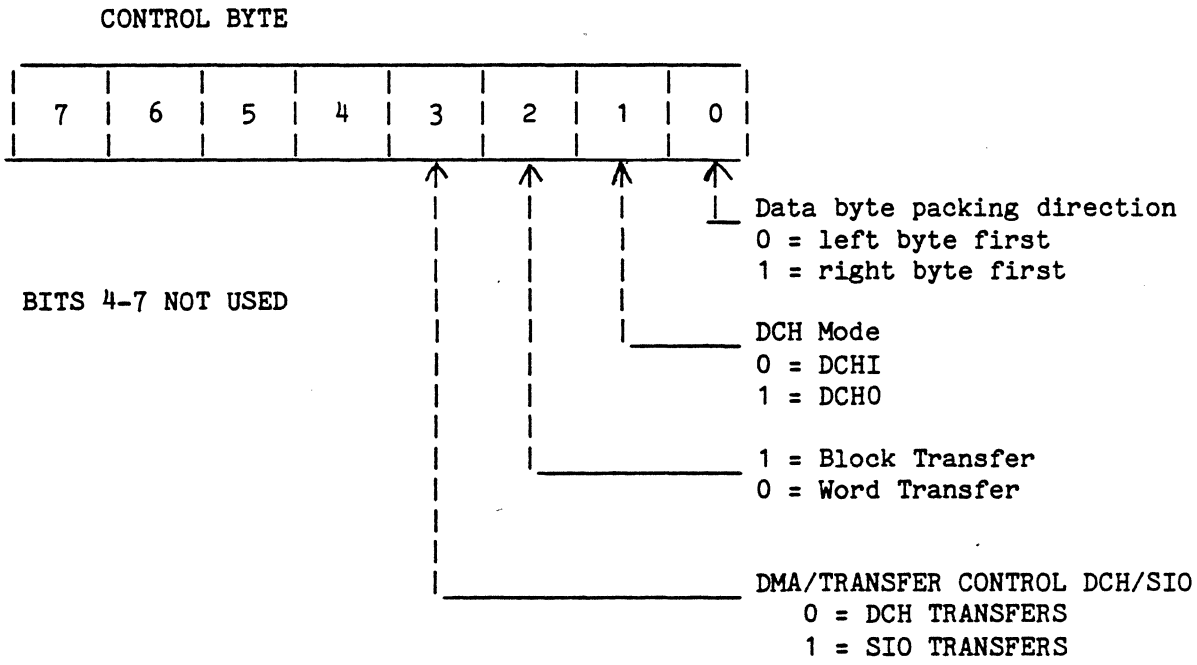


Figure 4-5. DCH Control Byte Encoding

5.0 Z80 INTERFACE DEVICES

The Z80 Interface Devices consist of the Direct Memory Access (DMA) controler, Counter Timer Circuit (CTC), and the Serial Input/Output (SIO) controler.

5.1 Direct Memory Access (DMA)

The DMA controler is a programmable, single-channel device which provides all address, timing, and control signals to effect the transfer of blocks of data between two ports within the PCU. These ports can be either system main memory or any system I/O interface device. The DMA also has the capability to search within a block of data for a particular byte (bit maskable), with or without simultaneous transfer. The DMA on the PCU is a dual purpose DMA, it handles data transfers between CGP and PCU memory via DCH as well as data transfers between PCU memory and SIO-1A.

5.2 Counter Timer Circuit (CTC)

The CTC is a programmable device with four independent channels that provide counting and timing functions for the PCU. Channels 0 and 1 are used primarily for Baud rate clock generation, which is used in conjunction with the SIO device. Channels 2 and 3 are generally used for event timing.

5.3 Serial Input/Output (SIO)

The SIO is a programmable, dual-channel device which provides formatting of data for serial data communications. It is capable of handling asynchronous, synchronous, and synchronous bit oriented protocols such as IBM Bisync, HDLC, SDLC, AND virtually any other serial protocol. It generates Cyclic Redundancy Check (CRC) codes in any synchronous mode and can be programmed for any traditional asynchronous format.

5.3.1 DMA/SIO SUPPORT for Port 0

The PCU also provides a very powerful data block transfer between the SIO channel A and Z80 memory through the DMA controller. This function can be enabled by programming bit position 3 of the DCH Control Byte (Z80 I/O address 10 Hex) to a 1, and the proper program for the DMA controller, the data will transfer between the Z80 memory and port 0 automatically without intervention from the Z80 CPU. This supports the high speed data rate up to 456 KB. Because this option shares the data channel address and control byte, a data channel clear must be issued by writing bit 5 = 1 to the Z80 miscellaneous function register (I/O address = 20 hex) before the SIO/DMA set up is started. (See Figure 4-5 on Control Byte Encoding)

6.0 Z80/COMMUNICAIONS PORT INTERFACE

6.1 Control Feature Summary

Generally, the control is as specified for the Z80 SIO. Here is a summary of control features set by mode words:

1. Synch Characters
   a. Programmable quantity, 1 or 2
   b. Programmable SYN and/or DLE stripping (receiver transparency)
   c. Programmable SYN idle (by disabling transmitter)
   d. Programmable SYN or DLE SYN1 insertion (transmitter transparency)
   e. Programmable interrupt on SYN insertion

2. Parity selection: odd/even/none

3. Character length selection: 7/8

4. Remote or local diagnostic loop back

5. "Data terminal ready" control

6. "Request to send" control

7. Interrupt on "ring indicator" or "loss of carrier"

6.2 Reading Port Control Bytes

Each communication port has two I/O addresses permanently assigned to allow Z80 reading of the "set up" bytes per port. These assignents as well as the "mode set up" assignments are listed in Table 4-2.

6.3 Operation With Modems

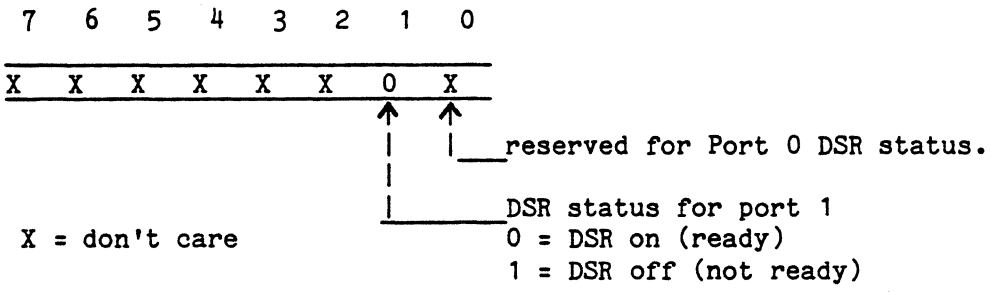
1. Due to lack of Data Terminal Ready on SIO-1B, DTR is controlled by writing to I/O device 2C. Bit 4 controls DTR for SIO 1A, bit 5 for SIO 1B.

2. Clear to send has a dual usage. It is used for both detection of ringing and clear to send. If no request to send has been issued, a 1 in the CTS status means ringing. to answer, just assert DTR and the ringing status should go to 0.

3. Clocks are normally provided by synchronous modems. For all other cases they must be provided by the PCU. Provision has been made for connecting the CTC 0 output to either receiver or transmitter clock (or both) for SIO 1A and CTC 1 similarly for SIO 1B.

4. Hardware connections for the modem interface are at the extractor end of the PCU board. Two 3M 26 pin connectors have been provided, one for each port. Connector D, located toward the bottom of the CGP card bin, is the port 0 connector. Connector E, located nearer the top of the CGP card bin, is the port 1 connector. (See Figure 6-1 for connector pin assignments)

5. DSR Support for Port 1
The DSR handshaking signal is required by some countries for EIA RS232 standard communication signaling. The software can read the Port 1 DSR status bit any time by issuing a Z80 I/O read command to I/O address 18 HEX. A "1" (high) in bit 1 means DSR off (not ready) and a "0" (low) in bit 1 means DSR on (ready).



6.4 EIA vs Current Loop Operations

1. Normally the operation of the PCU serial interface is EIA RS-232C or RS-423. Provision has been made for current loop by closing switch 8 of the device code switches for each port selected. Port 0 (SIO 1A) selection is at location 3E, port 1 (SIO 1B) at location 4E, (see section 8.2).

2. The hardware connections for current loop are at the CGP backplane on the same pins used by the MDB dual- port asynchronous controller. (see Figure 6-2 for backplane connections)

6.5 PCU Adapter Board

The PCU board can support a 100-pin adapter board for some additional circuitry to serve difference applications. The main assembly for port 0 and port 1 are EIA RS423 and RS232C interfaces. Through the Adapter board subassembly, a different type of interface can be built for both ports, such as RS422 interface for port 0 to support high speed data transfers (456KB), long distance (2000 ft) for the local networking application, and the current loop interface to support the CV plotter and PCU communication. (See Figure 6-3 for 100 pin connector signal list)

PIN	NAME	DTE DCE	FUNCTION	(CCITT)	(EIA)
1	FG	<-------->	FRAME GROUND	101	(AA)
2	TD	>-------->	TRANSMITTED DATA	103	(BA)
3	RD	<--------<	RECEIVED DATA	104	(BB)
4	RTS	>-------->	REQUEST TO SEND	105	(CA)
5	CTS	<--------<	CLEAR TO SEND	106	(CB)
6	DSR	<--------<	DATA SET READY	107	(CC)
7	SG	<--------<	SIGNAL GROUND	102	(AB)
8	DCD	<--------<	DATA CARRIER DETECT	109	(CF)
15	TC	<--------<	TRANSMITTER CLOCK	114	(DB)
17	RC	<--------<	RECEIVER CLOCK	115	(DD)
20	DTR	>-------->	DATA TERMINAL READY	108.2	(CD)
22	RI	<--------<	RING INDICATOR	125	(CE)
24	TC	>-------->	EXT. TRANSMITTER CLOCK	113	(DA)

Figure 6-1. RS-423A/RS-232C PORT 0/1 INTERCHANGE CIRCUITS

PORT 0	PORT 1	SIGNAL NAME
A1	A2	Ground
A6	A6	-5V (data in-)
A83	A73	Data out + (20 ma)
A85	A71	Data out -
B69	A61	Data in +

Figure 6-2. Current Loop BAckplane Connections

1	GND	26	A11/H	51	GND	76	CESIO2/L
2	+5V	27	A13/H	52	+5V	77	EXPORT/L
3	PARCL/L	28	A14/H	53	SPARE	78	CTCLLK0/L
4	PARGEN/L	29	A15/H	54	SPARE	79	SYSCLK/H
5	PARDIS/L	30	D0/H	55	BAO/L	80	DMAIE0/H
6		31	D1/H	56	NMI/L	81	TTLTXDA/H
7	MIEO/H	32	D2/H	57	MCLK/H	82	TTLRXDA/H
8	-5VM	33	D3/H	58	BLKODIS/L	83	TTLRTSA/L
9	EXP/L	34	D4/H	59	INT BUS/L	84	TTLRINGIND1/H
10	+12V	35	D5/H	60	MREQ/L	85	TTLCTSB/L
11	IORAMEN/L	36	D6/H	61	MIB/L	86	TTLPRTODIS/L
12	-12V	37	D7/H	62	IORQ/L	87	TTLTXDB/H
13	ENBLK16/L	38	DOB/H	63	RFSHB/L	88	RXDAEIAI/H
14	A0/H	39	DIB/H	64	RD/L	89	TTLRTSB/L
15	A1/H	40	D28/H	65	WR/L	90	SPARE
16	A2/H	41	D3B/H	66	WAIT/L	91	TTLDCDB/L
17	A3/H	42	D4B/H	67	ZRESET/L	92	TTLDTRA/L1
18	A4/H	43	D5B/H	68	BUSOFF/L	93	TTLRXCA/L
19	A5/H	44	D6B/H	69	MRESET/H	94	TTLTXCA/H
20	A6/H	45	D7B/H	70	CTCCLK1/L	95	TTLDSR/L
21	A7/H	46	SPARE	71	CTCCLK2/L	96	TTLRIA/H
22	A8/H	47	TTLDCDA/L	72	TTLCTSA/H	97	TTLRXDB/L
23	A9/H	48	TTLTXCB/L	73	TTLDTRB/L1	98	TTLRXCB/L
24	A12/H	49	+5V	74	BUSRQ/L	99	+5V
25	A10/H	50	GND	75	TTLPRTIDIS/L	100	GND

Figure 6-3. 100 Pin Connector Signal List (PF)

7.0 PCU STATUS REPORTING

During the self test diagnostic execution, the error codes, if any, will be displayed in the status lights (8 LED's) readable from the extractor end of the PC board. At the completion of the diagnostic, the PCU assumes the Personality Mode selected by the Personality Switches, displayes the status in the LED's and makes it available to the CGP 'C' register (low order byte) (see Table 2-5).

PCU status is reported in several ways:

1) The CGP'C" register (low order byte)
2) The PCU parameter table
3) Status indicator LEDs

7.1 CGP C Register

The CGP C register (low order byte) will contain the current status of the PCU while under control of the monitor (refer to Table 2-5).

7.2 PCU Parameter Table

The PCU Parameter table is used for the following:

a) to store self test diagnostic error codes. (Primary use)
b) to store task parameters sent by CGP via DOA and DIC
c) to store task outputs to be read by CGP via DOA and DIC
d) to load (by the CGP, a sequence of parameter table locations in Z80 machine code and cause the Z80, via DOA, to execute that code.

When an error is encountered during the self test diagnostics, the error code will be displayed in the eight status lights with the Most Significant Bit on. Therefore, the status lights can be distinguished over the error lights by the MSB (MSB on for error). (See Figure 7-1 for LED locations).

7.3 Status Indicator LEDS

There are three groups of status indicator LEDs. These are:

1) PCU Status LEDs
2) Z80-CPU Status LEDs
3) EIA Status LEDs

7.3.1 PCU Status LEDs

There are eight PCU Status LEDs located at the top of the stiffener end of the PCU board. (See Figure 7-1 for LED locations).

During self-test diagnostic execution, the error codes, if any, will be displayed in the PCU Status LEDs. The error codes can be distinguished from normal status by the most significant bit (MSB) of the LEDs being on. (See Tables 2-5 and 2-6 for status and error codes).

7.3.2 Z-80 CPU Status LED'S

1. The last 2 LEDs on the stiffener end of the board are NMI (non-maskable Interrupt) and HALT. These are located next to the Port 0 EIA connector (PD). (See Figure 7-1 for exact locations).

2. The MNI LED will be on when a memory parity error occurs. When an error occurs a message will output to the debug port (if there is a debug port chosen) and the error code will be put in the CGP 'C' Reg. Low Order Byte and be showing in the ERROR/STATUS LEDs. (See Table 2-6 for the error codes.) To recover from an NMI, the PCU will have to be RESET. If the error still exists, the microdiagnostics should point to an error in the PCU dynamic RAM.

3. The HALT LED will be on whenever the Z-80 CPU is in the HALT state due to an error. To restart the PCU, a RESET command must be issued (by hitting the PCU reset switch, or the CGP reset switch, or by a software RESET command from the CGP i.e IORST or NIOP to the Non-Z80 Device Code).

NOTE: NMI will result in a error halt to the PCU. However, Z80 Interrupts will be enabled for PCU interrogation.

7.3.3 EIA Indicator LEDs

1. The PCU contains LEDs that report the EIA interface status. These LEDs (3 per port) are located at the stiffener end of the board (see Figure 7-1 for exact locations).

2. The three LEDs (T, R, and DTR) are obained by ANDing certain EIA signals together. The following is how they are derived (see Figure 7-2 for EIA LED INDICATOR EXPLANATIONS):

   T: Request to send (CA) ANDed with XMIT Data (BA)
   R: Carrier Detect (CF) ANDed with Receive Data (BB)
   DTR: Data Terminal Ready (CD)

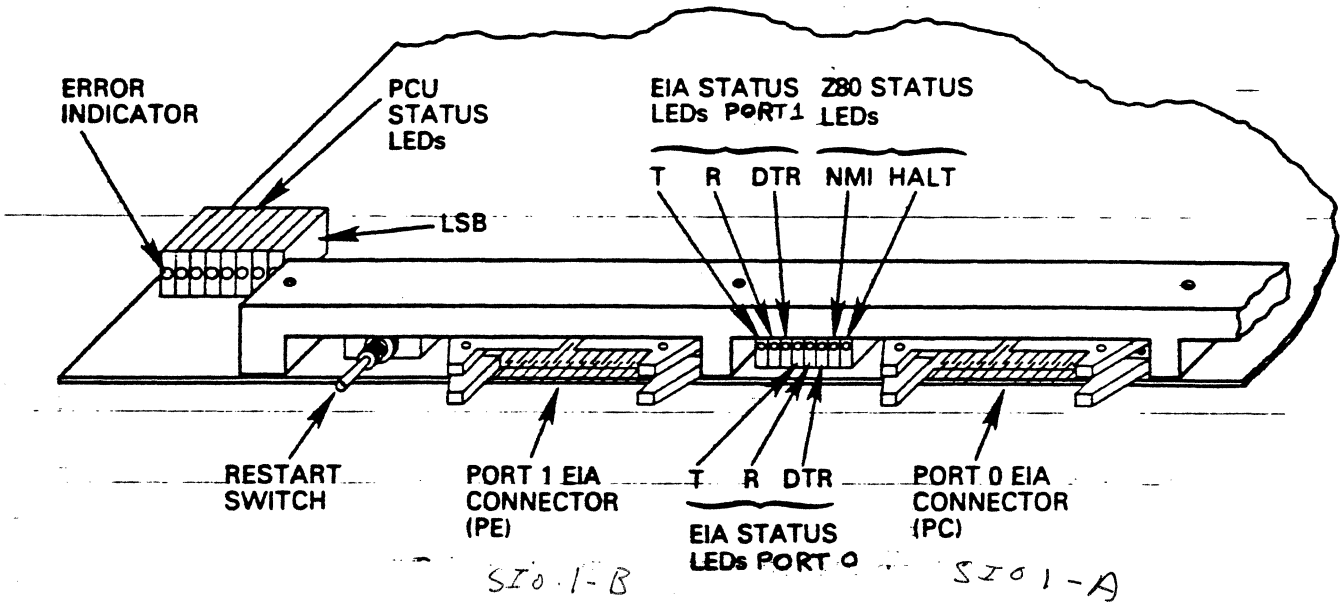
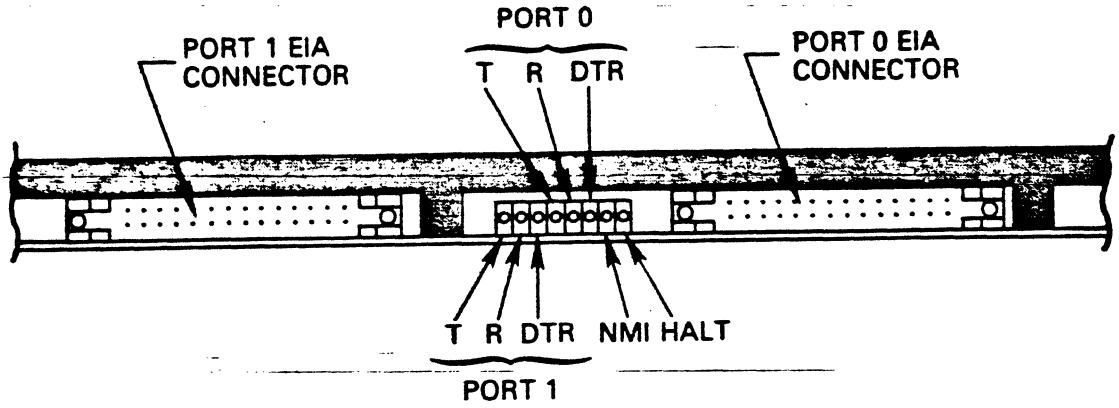


Figure 7-1. PCU Indicator LEDs



T:	OFF	NO REQUEST TO SEND (RTS)
	ON	RTS,BUT NO TRANSMIT DATA
	FLASHING	RTS AND TRANSMIT DATA PRESENT

R:	OFF	NO DATA CARRIER DETECT (DCD)
	ON	DCD,BUT NO RECEIVE DATA
	FLASHING	DCD AND RECEIVE DATA PRESENT

DTR:	OFF	NO DATA TERMINAL READY (DTR)
	ON	DATA TERMINAL READY PRESENT

Figure 7-2 EIA LED Indicator Explanations

8.0 PCU SWITCH DEFINITIONS

The PCU contains 5 switch packs with 8 switches per pack. Each switch pack is labeled for its primary function and each switch, or group of switches, on each pack, controls different functions. The switch packs are divided into 3 groups, 1 Personality switch pack, 3 Device Code switch packs, and 1 EIA Clock Control switch pack. The function of all switches is given in the following paragraphs. (see Figure 8-1 PCU Board Layout for physical locations)

8.1 Personality Switch Pack

The PCU personality switch pack is located in location 9F. Switches 7 and 8 specify the operating mode of the PCU (Monitor mode,MDB mode and 200X mode). The remaining switches are used for other related functions peculiar to each mode and can be read by the Z80 software allowing the Z80 to select the characteristics chosen for each Mode. (See Tables 8-1A,B,& C for switch definitions in each MODE)

8.2 Device Code Switch Packs

There are three Device Code switch packs on the PCU board. Each port (Z80, Port 0, Port 1) has a switch pack, in locations 2E,3E,and 4E respectively, to specify its own device code. The device code selection switches (switches 2-5) control the CGP device code port address only. This is independent of the Z80's control over a given port. Each switch pack has a hardware enable/disable switch (switch 1) for its port.

There are two other switches on the Device Code switch packs. Switch 7 and 8 are not used on the Z80 port, but Port 0 and 1 use switch 7 for EIA Ring detect enable/disable,and switch 8 for CURRENT LOOP/EIA selection. (See Table 8-3 for Device Code switch pack definitions)

8.3 EIA (Port 0 & 1) Clock Control Switch Pack

EIA Clock Control switch pack in location 11N is used to enable the clocking of serial data, for each port, to be from an internal or external source. There is also a switch to enable program control of Data Terminal Ready (DTR). (See Table 8-4 for connection configuration and switch definitions).

Table 8-1A Monitor Mode Personality Switch Definitions

SWITCHES

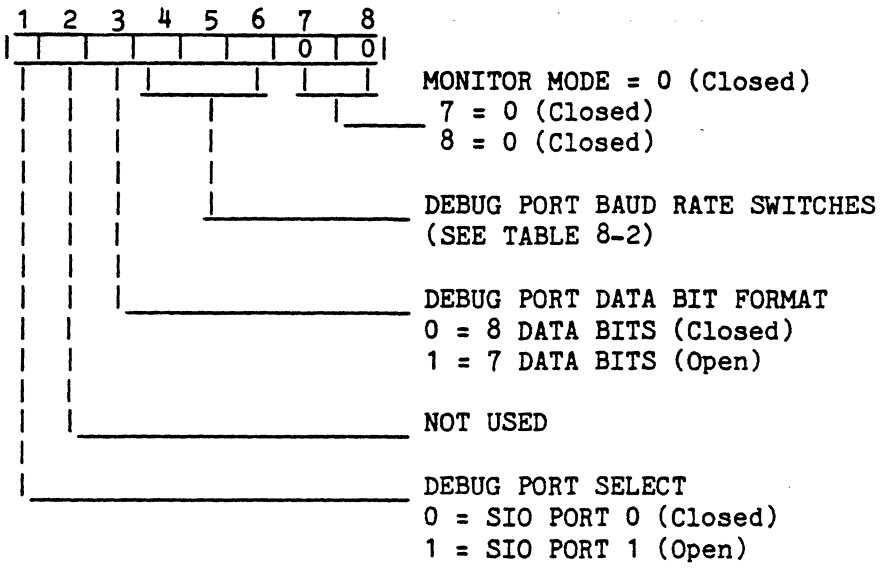


Table 8-1B MDB Emulator Mode Personality Switch Definitions

SWITCHES

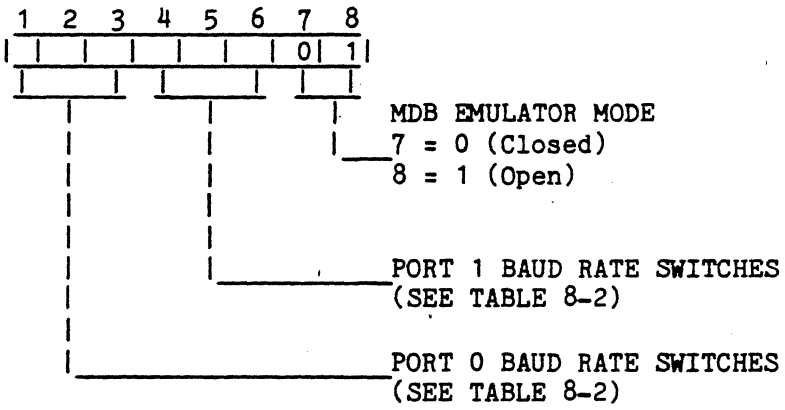


Table 8-1C 200X MONITOR MODE PERSONALITY SWITCH DEFINITIONS

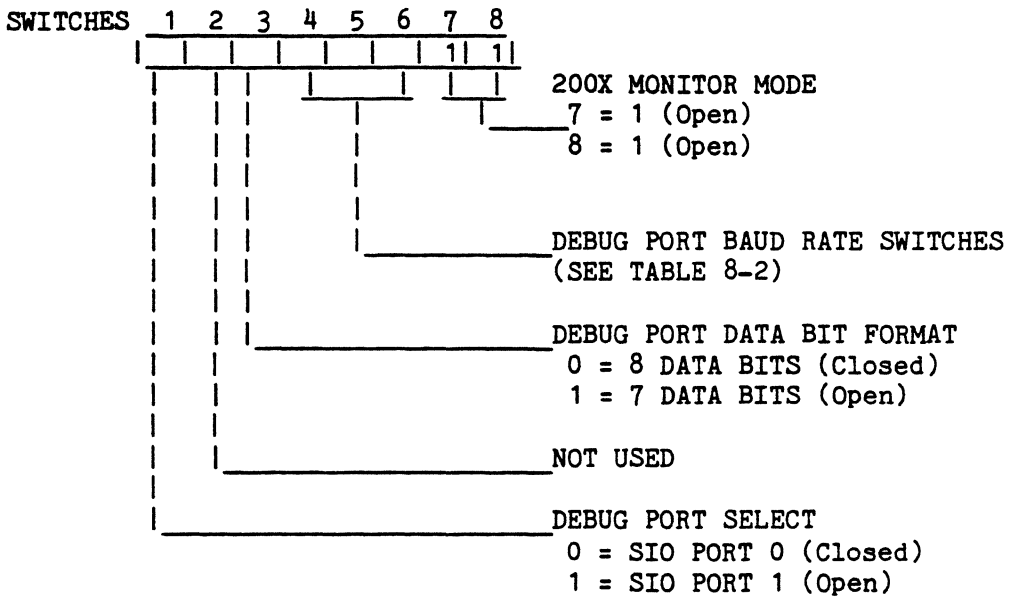


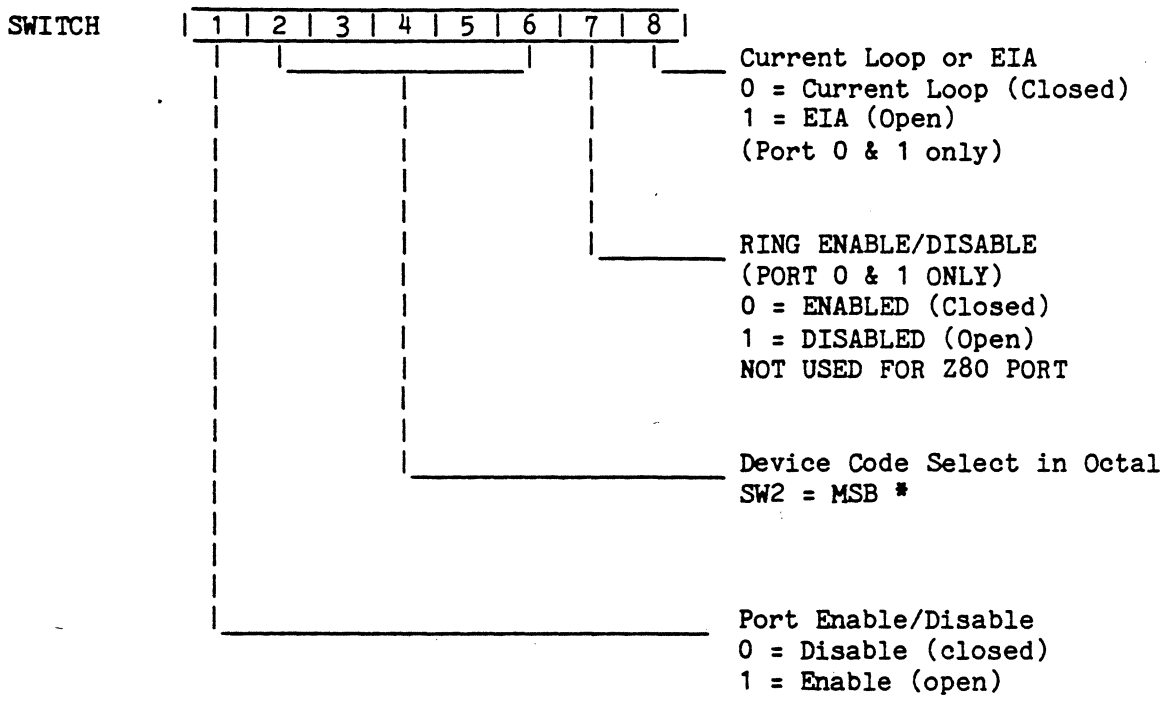
Table 8-2 Baud Rate Select Switches

BAUD RATE SELECTED	SWITCHES 3	2	1	MDB Port 0
	SWITCHES 6	5	4	MDB Port 1 or Debug Port
110	0	0	0	
300	0	0	1	
1200	0	1	0	
2400	0	1	1	
4800	1	0	0	
9600	1	0	1	
19.2 K Baud	1	1	0	
PORT DISABLED	1	1	1	

SWITCH OPEN = 1

Table 8-3 Device Code Switch Definitions

LOCATIONS: Z80 Device code 2E
Port 0 device code 3E
Port 1 device code 4E



SWITCH OPEN = 1

*By CGP programming convention, the low order bit of the device code is even for the input device, odd for outpt device. PCU hardware supports the toggling of the least significant bit (LSB) for input or output.

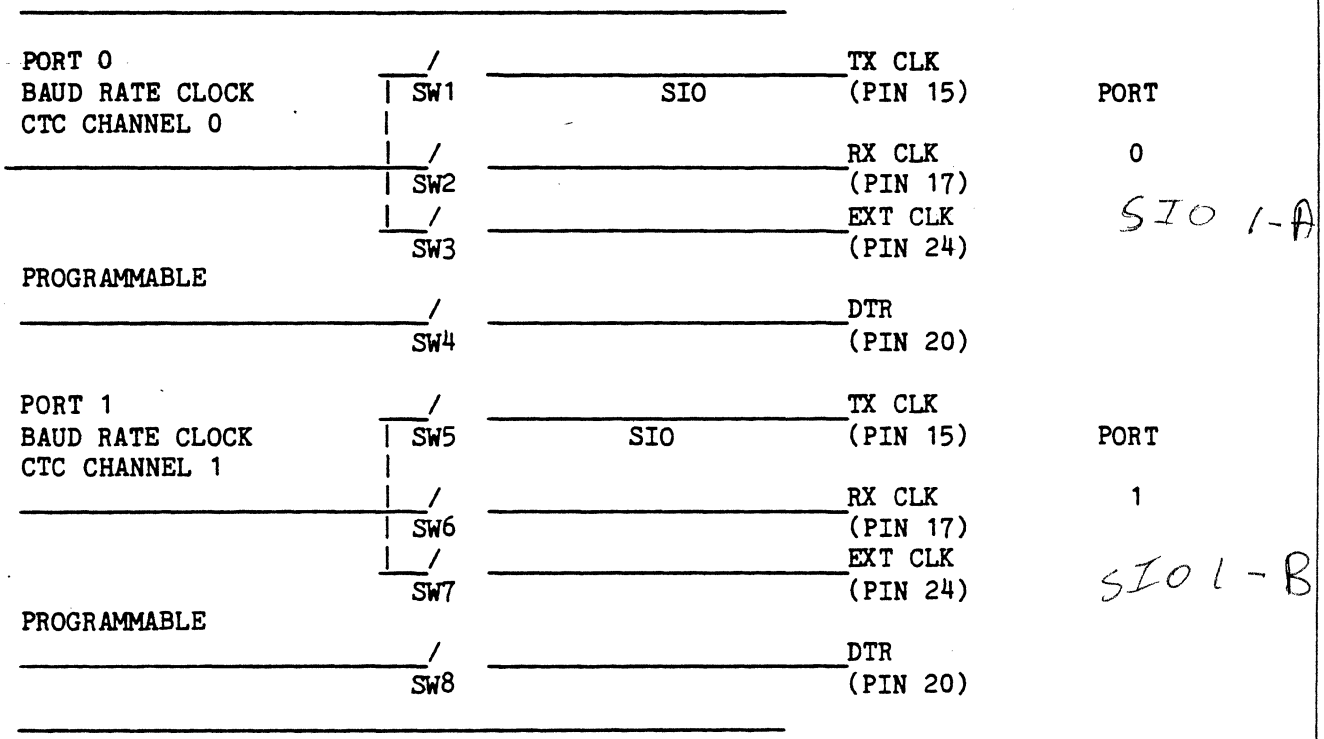
EXAMPLE:

	1	2	3	4	5	6	7	8
CLOSED			X				X	
OPEN	X	X		X	X	X		X

For this example:
1) Port enabled
2) Device Code = 56 (octal)
3) EIA

X - Denotes switch depressed in open or closed position

PCU CLOCK CONTROL SWITCHES (PROTOCOL SWITCHES)

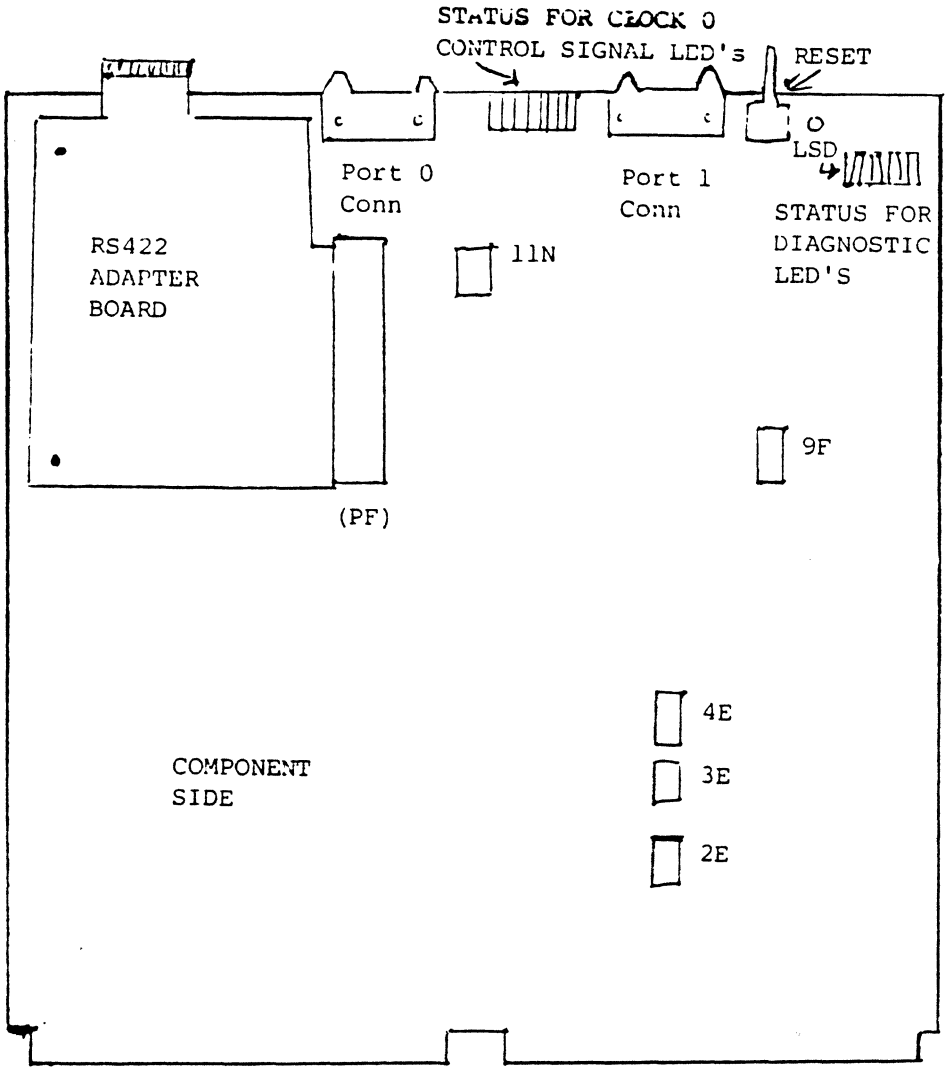


SWITCH DEFINITIONS

1 - Port 0 XMT CLK (closed = internal clocking)
2 - Port 0 RCV CLK (closed = internal clocking)
3 - Port 0 CLK OUT (closed = provide external clock)
4 - Port 0 DTR (closed = programmable, open = continuously on)

5 - Port 1 XMT CLK (closed = internal clocking)
6 - Port 1 RCV CLK (closed = internal clocking)
7 - Port 1 CLK OUT (closed = provide external clock)
8 - Port 1 DTR (closed = programmable, open = continuously on)

Figure 8-1 Interconnection Diagram of PCU Clock Control Switches (Protocol Switches)



SWITCHES

2E	Z80 DEVICE CODE
3E	PORT 0 DEVICE CODE
4E	PORT 1 DEVICE CODE
9F	PERSONALITY SWITCH
11N	CLOCK AND CONTROL SIGNALS

Figure 8-2. 4-Layer PCU Board Layout

9.0 PCU PROGRAMMING CONSIDERATIONS

1. The reset command forces the Z80 program counter to zero, clears the DMA controller (DMAC) and CTC, and initializes the busy/done logic as well as to force the starting address at 9000H. The reset condition is caused by I/O reset from the CGP or an NIOP to either the port 0 or 1 device code.

2. The non-maskable interrupt (NMI) causes the Z80 to restart at location 0066H. This will be used to indicate a memory parity failure in the RAM. Since location 0066H falls in RAM, the restart latch is used to force the address to 9066H in prom.

   When an NMI occurs, the PCU firmware halts with Z80 interrupts enabled. Z80 interrupts are enabled to allow error checking and recovery of the PCU. (Refer to Section 3.3.1).

   NOTE: To recover from an NMI, the CGP must issue an I/O reset or NIOP to Port 0 or 1.

3. Mode 1 interrupt response causes the Z80 to restart at location 0038H. This mode is not used by the monitor.

4. Mode 2 interrupt response allows the interrupting device to supply the low order half of the interrupt vector. The high order is supplied by the I-register. This is used for data protocol to/from all ports, CTC timer, DMA controller, the data input FIFO. Table 4-1 shows the mapping between the ports, devices, functions, and Z80 memory.

5. Z80 I/O addresses are used to communicate from the Z80 to all ports, the data channel controller, the CGP busy done logic, and the CTC timer. Table 4-2 shows the mapping of these assignments to Z80 I/O address space.

6. It is assumed that all Z80 programs (CVNET, GNA, 2780, etc..) will respond to NIOC PIO instruction by restarting the PCU personality mode (monitor mode, etc..) configured.