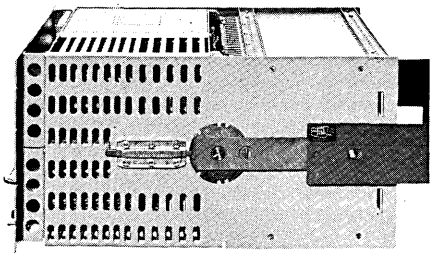
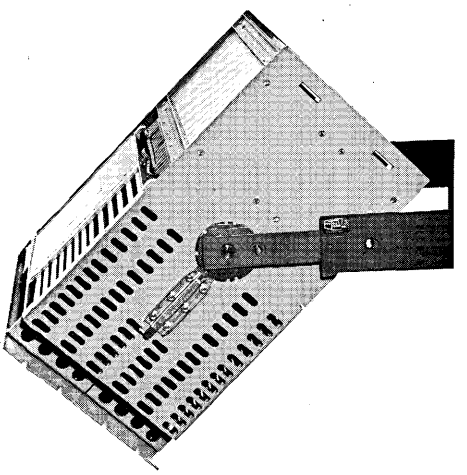
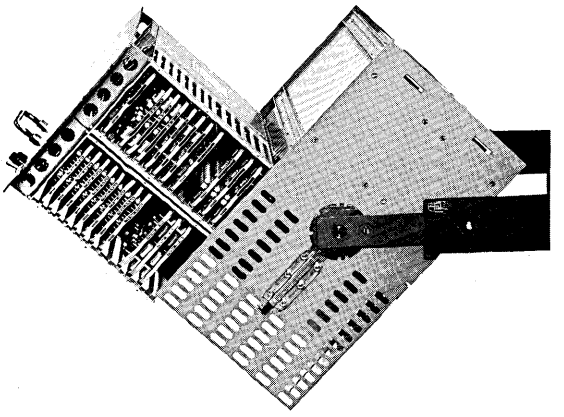
TCM-32

Magnetic Core Memory
Operating and Maintenance Manual







COMPUTER CONTROL COMPANY, INC.

Document No. 71-218

INSTRUCTION MANUAL
MAGNETIC CORE MEMORY SYSTEMS
SERIES TCM-32

May 1964

Computer Control Company, Inc.
Old Connecticut Path
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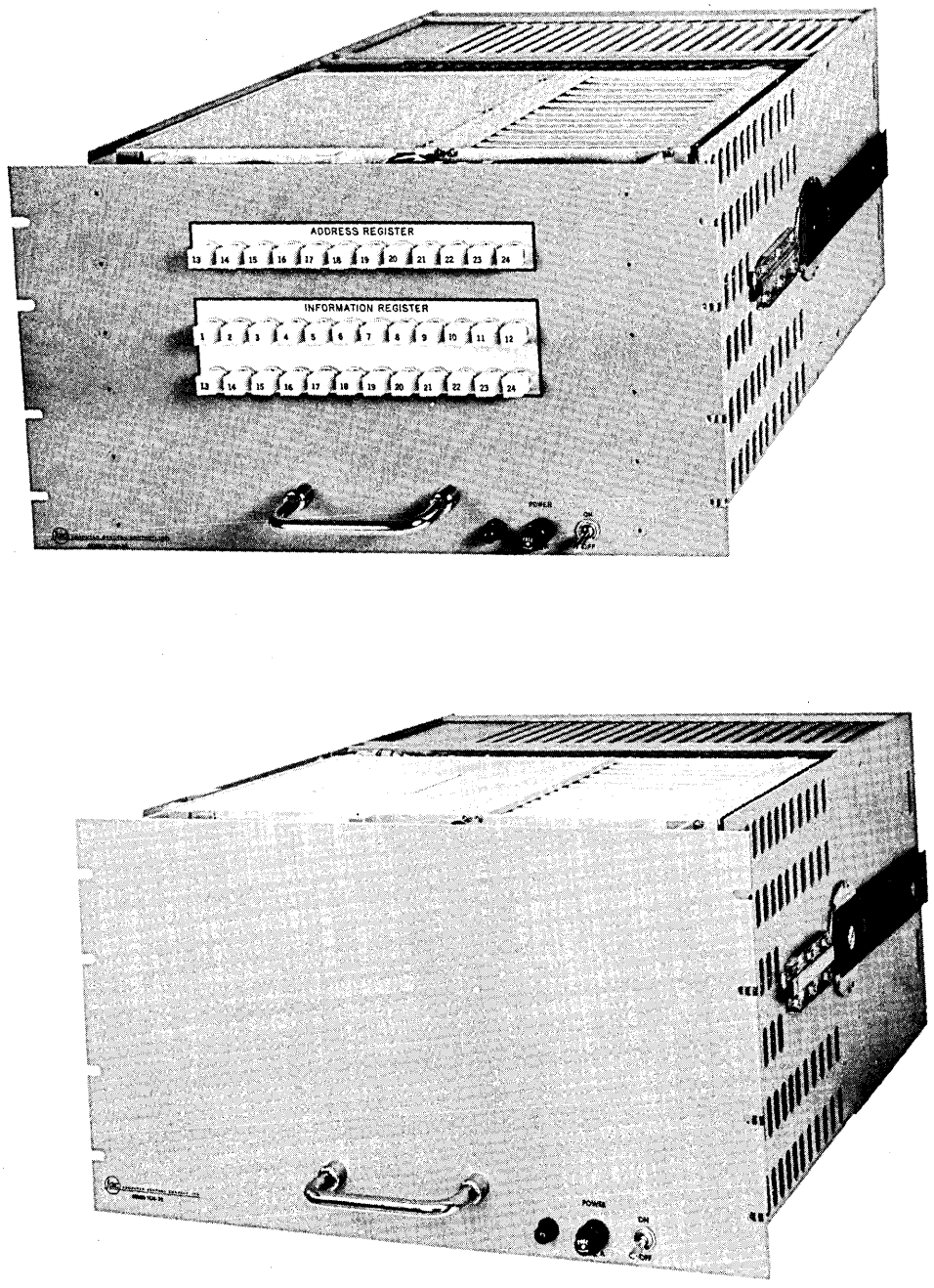


Figure 1-1. TCM-32 Magnetic Core Memory System

SECTION I
INTRODUCTION

1-1 PURPOSE AND SCOPE OF THIS MANUAL

This manual contains information on the theory of operation and instructions for the installation, operation, and maintenance of Series TCM-32, Magnetic Core Memory Systems (Figure 1-1). It is intended that this manual will contain all information required to properly operate and maintain the magnetic core memory system.

1-2 SYSTEM DESIGNATION

The TCM-32 is a high-speed magnetic core memory system that stores data in binary form at specific locations or addresses within the system. The storage capacity and speed of any TCM-32 memory system is indicated in the designation. For example, a storage system designated TCM-32 512/30-3.0/5.0 is identifiable as a TCM-32 system having 512 words of storage, each word of which contains 30 bits. The "3.0/5.0" portion of the designation indicates that the system has a half-cycle (load or unload) operating time of 3 μsec and a full-cycle (clear/write or read/regenerate) time of 5.0 μsec.

1-3 GENERAL DESCRIPTION

The basic storage elements of the TCM-32 system are toroidal ferrite cores. The cores are contained in a coincident-current core stack consisting of a number of mats or planes equal to the number of bits per word. A mat or plane contains a number of cores equal to the number of words of storage provided. Each core is capable of storing one bit of information; therefore, the total capacity of the memory equals the product of the number of cores per plane and the number of planes.

The TCM-32 magnetic core storage systems provide economical, efficient, fast-access storage. The memory is equipped to retain the magnetically stored information for an indefinite period even though primary power is removed.

The data signal interface between the TCM-32 and the external digital equipment with which it is used is achieved via flip-flop registers. This allows the address and the information signals from the external equipment to be specified as digital logic signals in the form of levels. Command signals are received by gates and are specified in the format of pulses.

Memory operation is controlled by internal timing circuits and occurs in response to one of several external command signals. Certain constraints exist between the timing of the command signals relative to the data signals; however, once the timing requirements are satisfied in the design of the system, memory operation is essentially independent of the associated equipment. Supervisory signals defining the status of the memory operation or signaling the completion of various phases of operation can be supplied to further augment the compatibility of the TCM-32 with the associated external equipment (Figure 1-1).

1-4 BASIC ELEMENTS AND ORGANIZATION

Figure 1-2 presents a simplified block diagram showing the basic elements and organization of a typical core memory system. In brief, the functions of these elements are as follows.

a. Memory Timing and Control provides the sequence of pulses necessary to perform a specified operation in response to a given command (clear/write, read/regenerate, load, unload or read/modify/write). (This unit generates the necessary timing signals for both the internal and external requirements.)

b. Address Register stores the specified address in binary form (static flip-flops) for a specified cycle. The outputs of the address register are used to drive the X and Y decoders.

c. X and Y Decoders and Switches decode the contents of the address register to select only the one proper address. The selected switches

are set up to allow the drive current to read from or write into the ferrite cores. The current pulses are directed by the switches through the proper X and Y drive lines.

d. Core Stack utilizes a conventional four-wire coincident-current wiring scheme. The construction and operation of the core stack is described in detail in Section III of this manual.

e. Information Register stores the information, one word at a time, to be inserted into the memory during a clear/write or load cycle. The information register receives the output information of a selected address during read/regenerate or unload cycles. This register also provides double-rail outputs to the external equipment.

f. Sense Amplifiers receive the output of selected cores, reject noise, and amplify the outputs to set the information register. One sense amplifier is required for each bit of the information word. The amplifiers employ time and amplitude discrimination to determine a ONE or a ZERO core output.

g. Inhibit Drivers are controlled by the information register and timed by the inhibit timing pulse. Each plane or bit is selectively driven in the memory by its inhibit driver circuit during a write period. When a ZERO is to be written in the selected core, the inhibit driver produces a current pulse which acts in opposition to the selected drive current. If a ONE is to be written, the inhibit driver is gated off by the appropriate flip-flop in the information register.

1-4.1 Memory System Layout

Figure 1-3 identifies the unit layout of the memory system. The memory system is mechanically designed for standard 19-inch relay rack mounting. Brief descriptions of each unit are listed below.

Unit 1 contains part of the information register, timing and control circuits, and partitioning option.

Unit 2 contains selection switches, current drivers, read-write gate driver, and inhibit drivers.

Unit 3 contains part of the information, and address registers.

Unit 4 contains inhibit drivers, and address decoders.

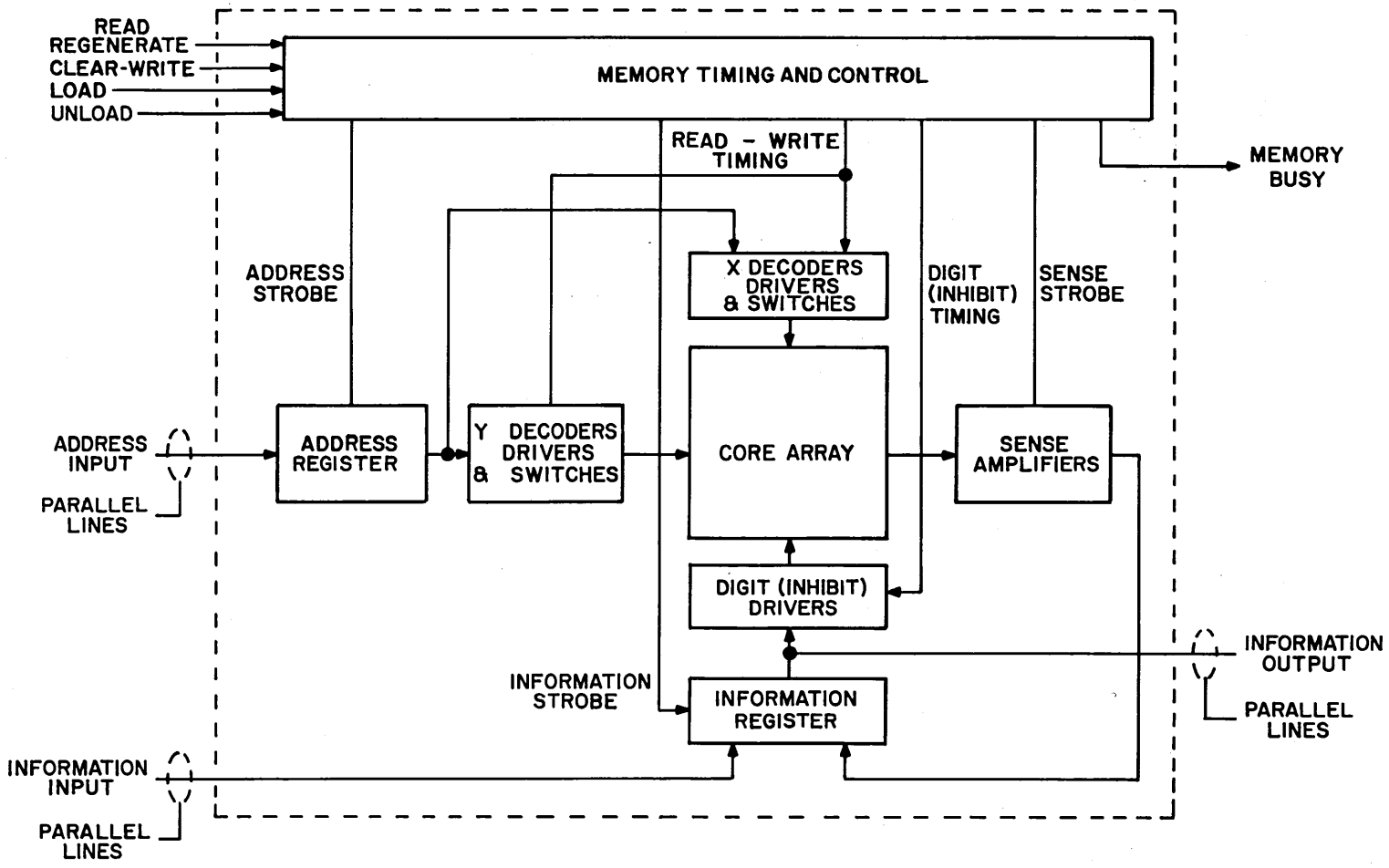


Figure 1-2. Memory System, Block Diagram

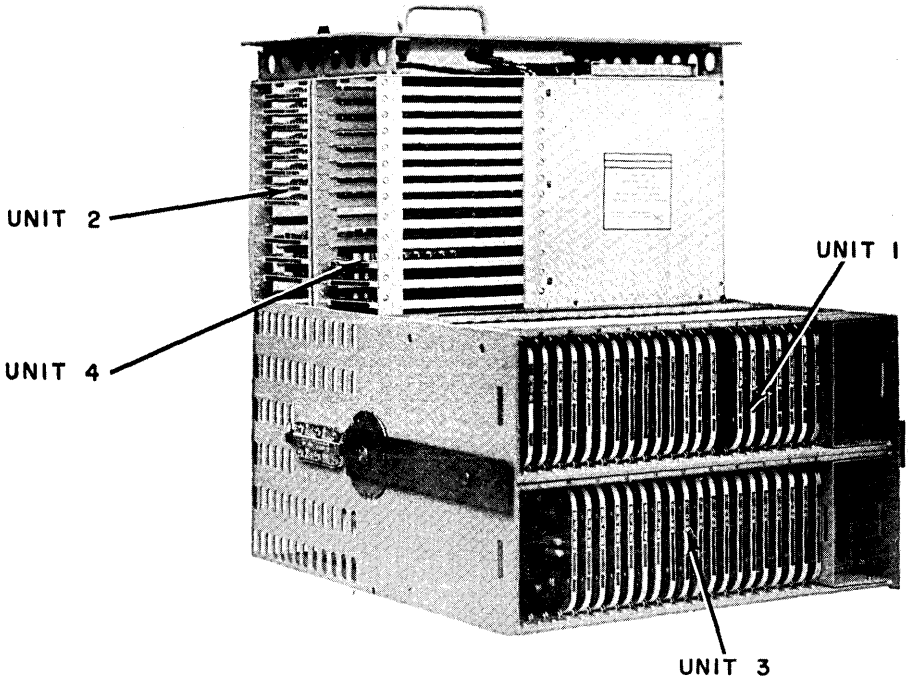


Figure 1-3. Memory System Layout

1-5 INPUT SIGNALS

The address register varies from 7 to 12 bits, depending on memory capacity (size). The minimum period of time and the time at which inputs must be present for a random-address operation are shown in the timing diagrams of Section III.

Clear/write command initiates a cycle which clears the cores at the address specified by the address register, and writes the information provided in the information register.

Read/regenerate initiates a cycle which reads the cores at the address specified by the address register and rewrites this information in the cores previously read. The information is held in the information register until another cycle is started. The size of the information register corresponds to the number of bits per word. Information is provided in parallel to this register and must be timed as indicated in the timing diagrams of Section III.

SECTION II
SYSTEM INSTALLATION

2-1 GENERAL

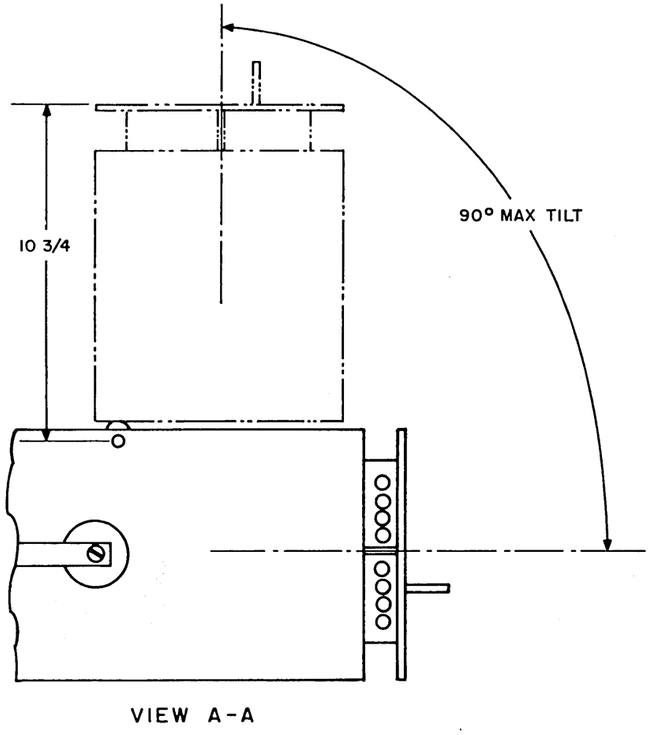
After unpacking the equipment, conduct a visual mechanical inspection to determine whether the equipment was damaged during shipment, and immediately report any damage to the carrier or shipping agency.

During positioning and installation of the equipment, do not disturb any factory adjustments. Check that the AC power switch, located on the front panel of the memory unit (Figure 1-1), is in the OFF position before making any electrical connections.

The system is shipped with the core matrix, all S-BLOC chassis, and 3C S-PACs® prewired and properly secured in place. After completing the mechanical installation of the equipment in the rack, conduct a second inspection to ensure that all wiring and PACs are secured. Mechanical installation is illustrated in Figure 2-1.

2-2 ELECTRICAL INTERCONNECTIONS

The wiring of connectors J-102 through J-107 are defined in Tables 2-1 through 2-6. The physical location of these connectors is shown in Figure 2-2; the pin numbering scheme is illustrated in Figure 2-3. A diagram showing the power wiring of the TCM-32 is presented in Figure 2-4. The AC and DC power connections should be provided via the mating connectors furnished by Computer Control Company. Refer to the pin connections in Figure 2-4 and note that two -18 volt connections are shown. These connections should not be connected in P101 but wired as separate leads back to the power supply. This will utilize the filtering capacitors in the power supply and reduce noise on the -18 volt logic buses due to inhibit pulse current.



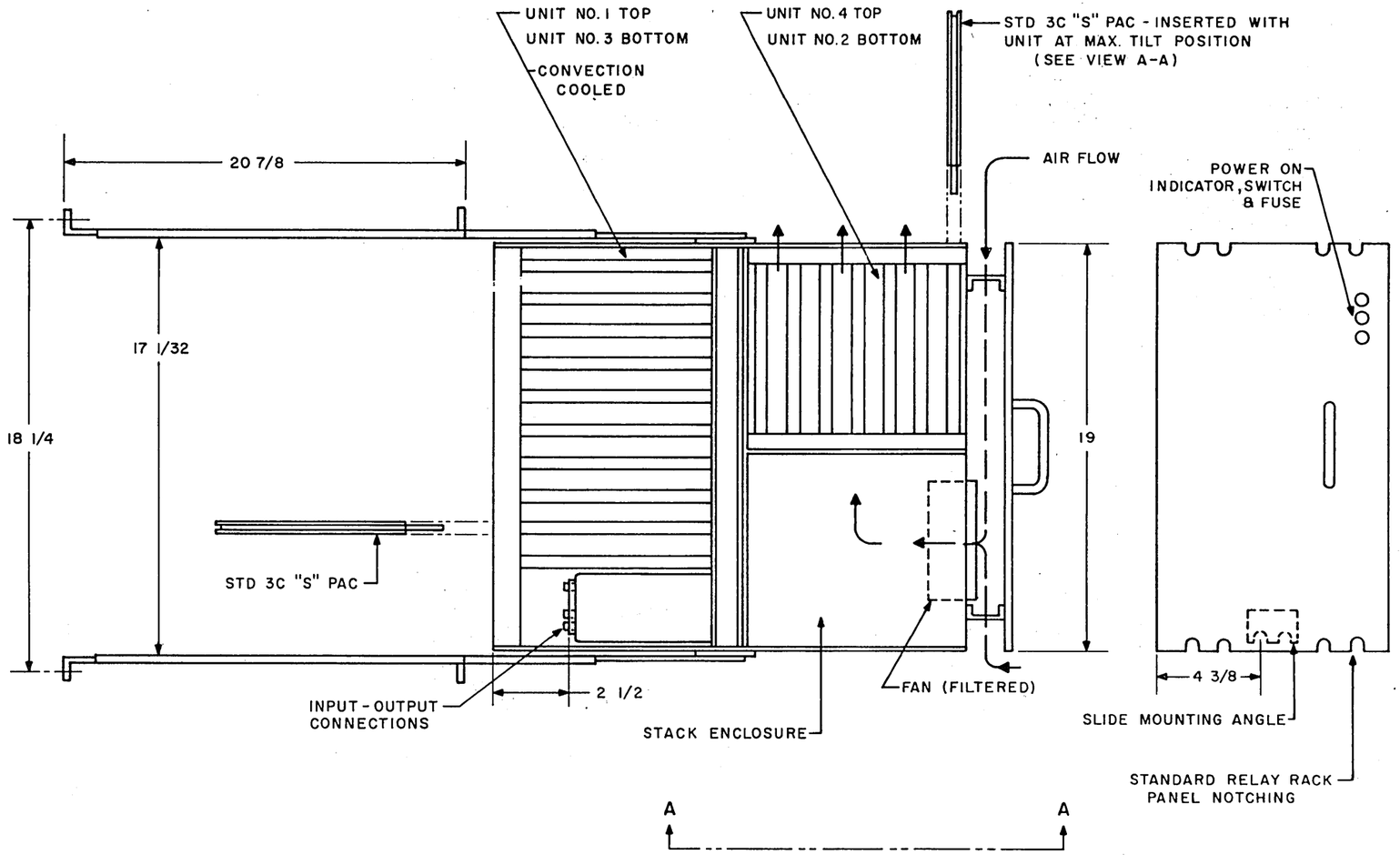


Figure 2-1. Installation Drawing
(Sheet 1 of 2)

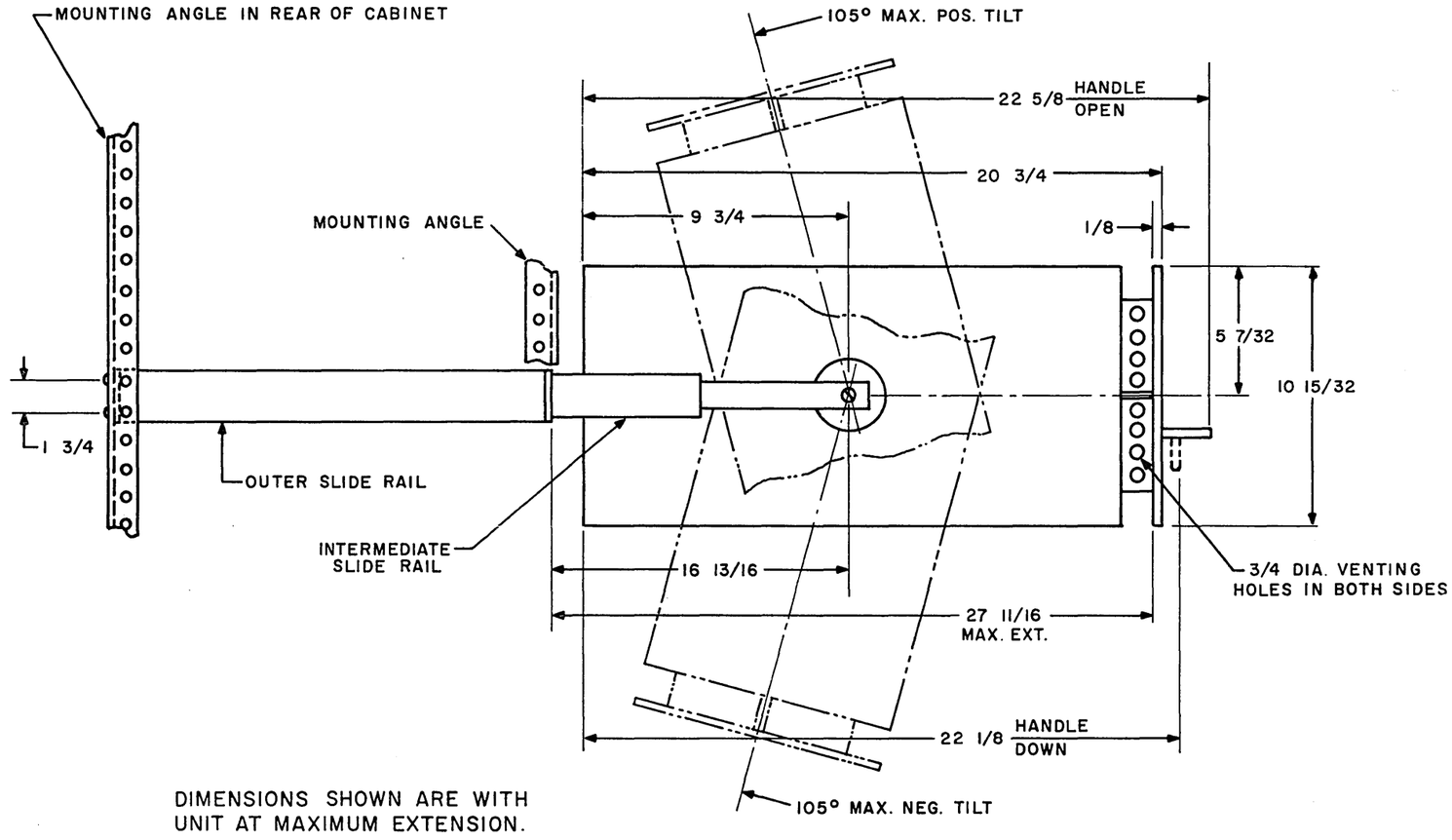
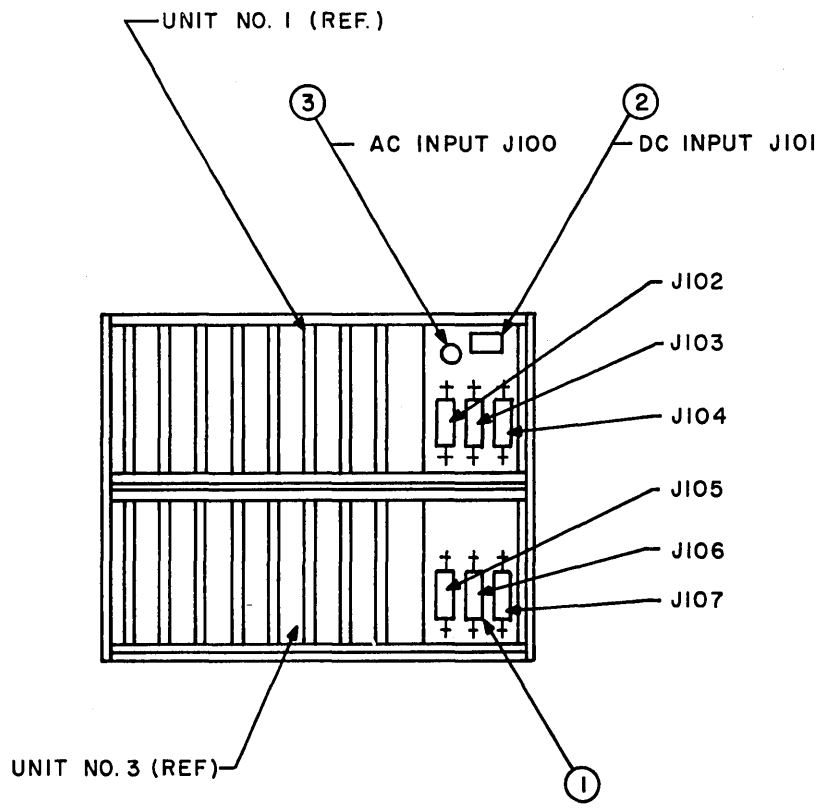


Figure 2-1. Installation Drawing
(Sheet 2 of 2)



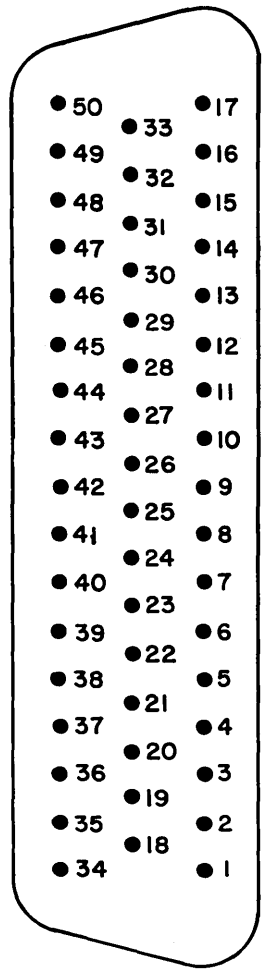
MATING CONNECTORS (SHIPPED WITH TCM-32)

1. CONNECTOR, DD-50P 3C PART NO. 941 105 001
2. PLUG, MRA-14S-JTC-H 3C PART NO. 941 114 001
3. PLUG, M4S-LS 3C PART NO. 941 115 001

NOTES:

1. UNIT WEIGHT (EMPTY) APPROX. 40 LB
2. MAX. PAC EXTRACTION FORCE REQD 20 LB
3. POWER INPUT -115 V AC FUSED ON FRONT PANEL. DC INPUT INTERLOCKED THRU AC ACTUATED RELAY.
4. MEMORY NORMALIZER BOARD (MN) IS LOCATED BEHIND CONNECTORS J102, J103, J104, IN UNIT 1.
5. INDICATOR POWER SUPPLY (WHEN INCLUDED AS AN OPTION) IS LOCATED BEHIND CONNECTORS J105, J106, J107, IN UNIT 3.

Figure 2-2. Connector Detail



CONNECTOR TYPE:
CANNON DD-50

(NOT TO SCALE)

Figure 2-3. Pin Numbering, Connectors J-102 through J-107

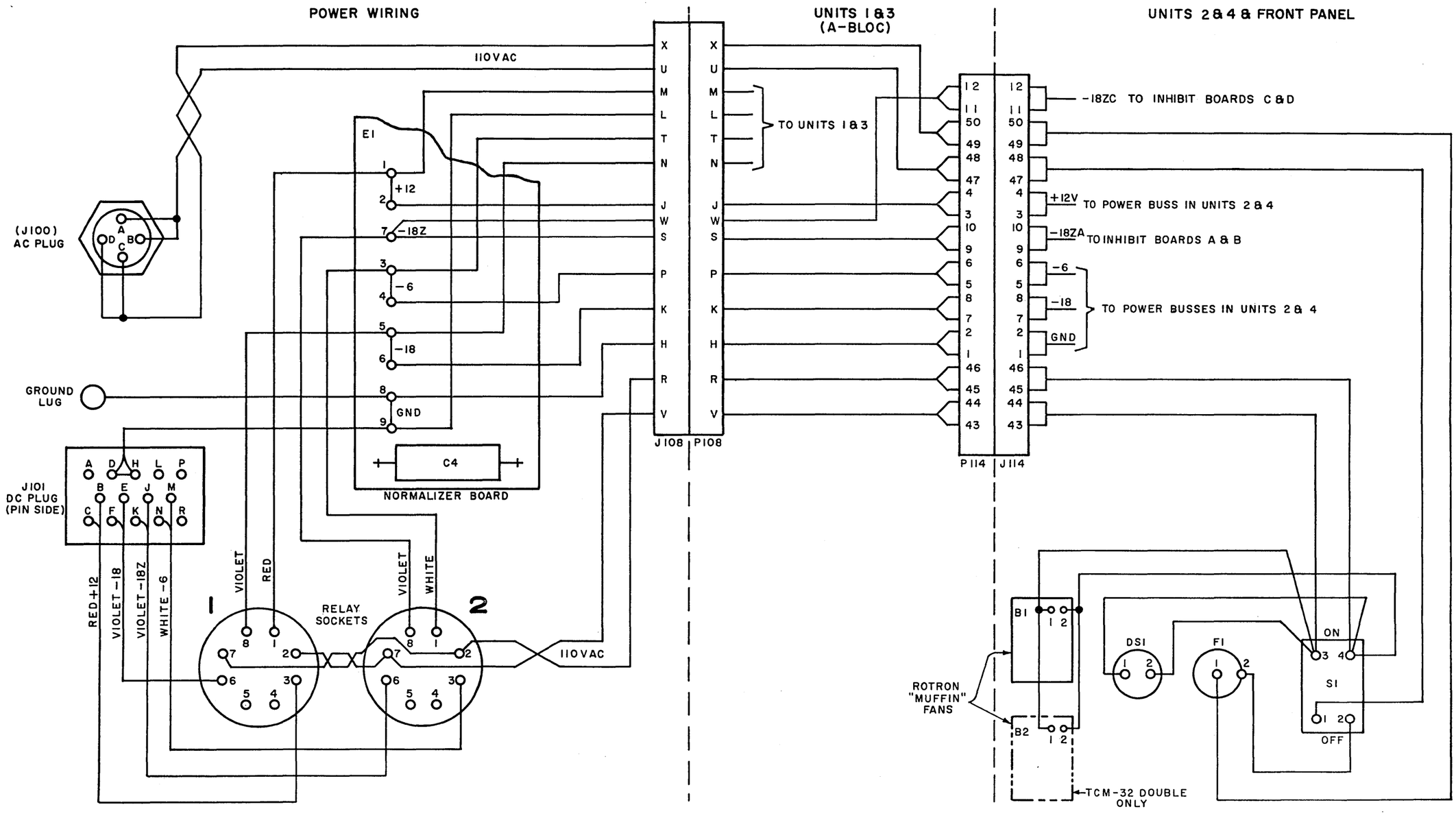


Figure 2-4. TCM-32 Power Wiring Diagram

TABLE 2-1.
WIRING CONNECTOR J-102

(Connector location is found in Figure 2-2
Figure 2-3 shows pin numbering)

Pin Number	Signal	Function	Pin Number	Signal	Function
1	I-1	Information In	26	$\overline{\text{I-13}}$	Information In
2	$\overline{\text{I-1}}$	Information In	27	I-14	Information In
3	I-2	Information In	28	$\overline{\text{I-14}}$	Information In
4	$\overline{\text{I-2}}$	Information In	29	I-15	Information In
5	I-3	Information In	30	$\overline{\text{I-15}}$	Information In
6	$\overline{\text{I-3}}$	Information In	31	I-16	Information In
7	I-4	Information In	32	$\overline{\text{I-16}}$	Information In
8	$\overline{\text{I-4}}$	Information In	33	I-17	Information In
9	I-5	Information In	34	$\overline{\text{I-17}}$	Information In
10	$\overline{\text{I-5}}$	Information In	35	I-18	Information In
11	I-6	Information In	36	$\overline{\text{I-18}}$	Information In
12	$\overline{\text{I-6}}$	Information In	37	I-19	Information In
13	I-7	Information In	38	$\overline{\text{I-19}}$	Information In
14	$\overline{\text{I-7}}$	Information In	39	I-20	Information In
15	I-8	Information In	40	$\overline{\text{I-20}}$	Information In
16	$\overline{\text{I-8}}$	Information In	41	I-21	Information In
17	I-9	Information In	42	$\overline{\text{I-21}}$	Information In
18	$\overline{\text{I-9}}$	Information In	43	I-22	Information In
19	I-10	Information In	44	$\overline{\text{I-22}}$	Information In
20	$\overline{\text{I-10}}$	Information In	45	I-23	Information In
21	I-11	Information In	46	$\overline{\text{I-23}}$	Information In
22	$\overline{\text{I-11}}$	Information In	47	I-24	Information In
23	I-12	Information In	48	$\overline{\text{I-24}}$	Information In
24	$\overline{\text{I-12}}$	Information In	49		Signal Ground
25	I-13	Information In	50		Chassis Ground

TABLE 2-2.
WIRING CONNECTOR J-103

Pin Number	Signal	Function	Pin Number	Signal	Function
1	IR-1	Information Out	26	$\overline{\text{IR-13}}$	Information Out
2	$\overline{\text{IR-1}}$	Information Out	27	IR-14	Information Out
3	IR-2	Information Out	28	$\overline{\text{IR-14}}$	Information Out
4	$\overline{\text{IR-2}}$	Information Out	29	IR-15	Information Out
5	IR-3	Information Out	30	$\overline{\text{IR-15}}$	Information Out
6	$\overline{\text{IR-3}}$	Information Out	31	IR-16	Information Out
7	IR-4	Information Out	32	$\overline{\text{IR-16}}$	Information Out
8	$\overline{\text{IR-4}}$	Information Out	33	IR-17	Information Out
9	IR-5	Information Out	34	$\overline{\text{IR-17}}$	Information Out
10	$\overline{\text{IR-5}}$	Information Out	35	IR-18	Information Out
11	IR-6	Information Out	36	$\overline{\text{IR-18}}$	Information Out
12	$\overline{\text{IR-6}}$	Information Out	37	IR-19	Information Out
13	IR-7	Information Out	38	$\overline{\text{IR-19}}$	Information Out
14	$\overline{\text{IR-7}}$	Information Out	39	IR-20	Information Out
15	IR-8	Information Out	40	$\overline{\text{IR-20}}$	Information Out
16	$\overline{\text{IR-8}}$	Information Out	41	IR-21	Information Out
17	IR-9	Information Out	42	$\overline{\text{IR-21}}$	Information Out
18	$\overline{\text{IR-9}}$	Information Out	43	IR-22	Information Out
19	IR-10	Information Out	44	$\overline{\text{IR-22}}$	Information Out
20	$\overline{\text{IR-10}}$	Information Out	45	IR-23	Information Out
21	IR-11	Information Out	46	$\overline{\text{IR-23}}$	Information Out
22	$\overline{\text{IR-11}}$	Information Out	47	IR-24	Information Out
23	IR-12	Information Out	48	$\overline{\text{IR-24}}$	Information Out
24	$\overline{\text{IR-12}}$	Information Out	49		Signal Ground
25	IR-13	Information Out	50		Chassis Ground

TABLE 2-3.
WIRING CONNECTOR J-104

Pin Number	Function	Remarks
1	Input: Read/Regenerate (SIG)	1 and 2: Twisted Pair
2	Input: Read/Regenerate (GND)	
3	Input: Clear/Write (SIG)	3 and 4: Twisted Pair
4	Input: Clear/Write (GND)	
5	Input: Unload Buffer (SIG)	5 and 6: Twisted Pair
6	Input: Unload Buffer (GND)	
7	Input: Load Buffer (SIG)	7 and 8: Twisted Pair
8	Input: Load Buffer (GND)	
9	Input: Random/Sequential Operation	-6 V: Random 0 V: Sequential
10	Input: Memory Clear (SIG)	10 and 11: Twisted Pair
11	Input: Memory Clear (GND)	
12	Input: Reset Unload Counter	
13	Input: Reset Load Counter	(Address register)
14	Input: Reset Information Register (SIG)	Pulse: -6 V to 0 V 14 and 15: Twisted Pair
15	Input: Reset Information Register (GND)	
16	Input: Drop-in (SIG)	Pulse: -6 V to 0 V 16 and 17: Twisted Pair
17	Input: Drop-in (GND)	
18	Input: Read/Modify/Write	$\overline{\text{RMW}}$
19	Input: Load Counter (Advance SIG)	Pulse: -6 V to 0 V 19 and 20: Twisted Pair
20	Input: Load Counter (Advance GND)	
21	Input: Unload Counter (Advance SIG)	Pulse: -6 V to 0 V 21 and 22: Twisted Pair
22	Input: Unload Counter (GND)	
23	Input: Address Register Strobe (SIG)	Pulse: -6 V to 0 V Twisted Pair

TABLE 2-3. (Cont)
WIRING CONNECTOR J-104

Pin Number	Function	Remarks
24	Input: Address Register Strobe (GND)	
25	Input: Address Register Shift (SIG)	25 and 26: Twisted Pair
26	Input: Address Register Shift (GND)	
27	Input: Information Shift (SIG)	27 and 28: Twisted Pair
28	Input: Information Shift (GND)	
29	Input: Information Register	Zone A } partitioning option
30	Input: Information Register	Zone B } partitioning option
31	Input: Information Register	Zone C } partitioning option
32	Input: Information Register	Zone D } partitioning option
33		Wired Spare
34		Wired Spare
35		Wired Spare
36		Wired Spare
37		
38	Output: End of Cycle	Pulse: -6 V to 0 V 38 and 39: Twisted Pair
39	Output: End of Cycle	
40	Output: Information Ready (SIG)	Pulse: -6 V to 0 V 40 and 41: Twisted Pair
41	Output: Information Ready (GND)	
42	Random Access	-6 V
43	Sequential Access	-6 V
44	Load Mode	-6 V
45	Unload Mode	-6 V
46	Power	+12 V
47	Power	-6 V
48	Power	-18 V
49		Signal Ground
50		Chassis Ground

TABLE 2-4.
WIRING CONNECTOR J-105

Pin Number	Signal	Function	Pin Number	Signal	Function
1	A-1	Address Reg. In	26	$\overline{\text{AR-7}}$*	Address Reg. Out
2	A-2	Address Reg. In	27	AR-8	Address Reg. Out
3	A-3	Address Reg. In	28	$\overline{\text{AR-8}}$*	Address Reg. Out
4	A-4	Address Reg. In	29	AR-9	Address Reg. Out
5	A-5	Address Reg. In	30	$\overline{\text{AR-9}}$*	Address Reg. Out
6	A-6	Address Reg. In	31	AR-10	Address Reg. Out
7	A-7	Address Reg. In	32	$\overline{\text{AR-10}}$*	Address Reg. Out
8	A-8	Address Reg. In	33	AR-11	Address Reg. Out
9	A-9	Address Reg. In	34	$\overline{\text{AR-11}}$*	Address Reg. Out
10	A-10	Address Reg. In	35	AR-12	Address Reg. Out
11	A-11	Address Reg. In	36	$\overline{\text{AR-12}}$*	Address Reg. Out
12	A-12	Address Reg. In	37	ARU-1*	Unload AR Out
13	AR-1	Address Reg. Out	38	ARU-2*	Unload AR Out
14	$\overline{\text{AR-1}}$*	Address Reg. Out	39	ARU-3*	Unload AR Out
15	AR-2	Address Reg. Out	40	ARU-4*	Unload AR Out
16	$\overline{\text{AR-2}}$*	Address Reg. Out	41	ARU-5*	Unload AR Out
17	AR-3	Address Reg. Out	42	ARU-6*	Unload AR Out
18	$\overline{\text{AR-3}}$*	Address Reg. Out	43	ARU-7*	Unload AR Out
19	AR-4	Address Reg. Out	44	ARU-8*	Unload AR Out
20	$\overline{\text{AR-4}}$*	Address Reg. Out	45	ARU-9*	Unload AR Out
21	AR-5	Address Reg. Out	46	ARU-10*	Unload AR Out
22	$\overline{\text{AR-5}}$*	Address Reg. Out	47	ARU-11*	Unload AR Out
23	AR-6	Address Reg. Out	48	ARU-12*	Unload AR Out
24	$\overline{\text{AR-6}}$*	Address Reg. Out	49		
25	AR-7	Address Reg. Out	50		

*ARU and $\overline{\text{AR}}$ signals on request only

TABLE 2-5.
WIRING CONNECTOR J-106

Pin Number	Signal	Function	Pin Number	Signal	Function
1	I-25	Information In	26	$\overline{\text{I-37}}$	Information In
2	$\overline{\text{I-25}}$	Information In	27	I-38	Information In
3	I-26	Information In	28	$\overline{\text{I-38}}$	Information In
4	$\overline{\text{I-26}}$	Information In	29	I-39	Information In
5	I-27	Information In	30	$\overline{\text{I-39}}$	Information In
6	$\overline{\text{I-27}}$	Information In	31	I-40	Information In
7	I-28	Information In	32	$\overline{\text{I-40}}$	Information In
8	$\overline{\text{I-28}}$	Information In	33	I-41	Information In
9	I-29	Information In	34	$\overline{\text{I-41}}$	Information In
10	$\overline{\text{I-29}}$	Information In	35	I-42	Information In
11	I-30	Information In	36	$\overline{\text{I-42}}$	Information In
12	$\overline{\text{I-30}}$	Information In	37	I-43	Information In
13	I-31	Information In	38	$\overline{\text{I-43}}$	Information In
14	$\overline{\text{I-31}}$	Information In	39	I-44	Information In
15	I-32	Information In	40	$\overline{\text{I-44}}$	Information In
16	$\overline{\text{I-32}}$	Information In	41	I-45	Information In
17	I-33	Information In	42	$\overline{\text{I-45}}$	Information In
18	$\overline{\text{I-33}}$	Information In	43	I-46	Information In
19	I-34	Information In	44	$\overline{\text{I-46}}$	Information In
20	$\overline{\text{I-34}}$	Information In	45	I-47	Information In
21	I-35	Information In	46	$\overline{\text{I-47}}$	Information In
22	$\overline{\text{I-35}}$	Information In	47	I-48	Information In
23	I-36	Information In	48	$\overline{\text{I-48}}$	Information In
24	$\overline{\text{I-36}}$	Information In	49		Signal Ground
25	I-37	Information In	50		Chassis Ground

TABLE 2-5. (Cont)
WIRING CONNECTOR J-107

Pin Number	Signal	Function	Pin Number	Signal	Function
1	IR-25	Information Out	26	$\overline{\text{IR-37}}$	Information Out
2	$\overline{\text{IR-25}}$	Information Out	27	IR-38	Information Out
3	IR-26	Information Out	28	$\overline{\text{IR-38}}$	Information Out
4	$\overline{\text{IR-26}}$	Information Out	29	IR-39	Information Out
5	IR-27	Information Out	30	$\overline{\text{IR-39}}$	Information Out
6	$\overline{\text{IR-27}}$	Information Out	31	IR-40	Information Out
7	IR-28	Information Out	32	$\overline{\text{IR-40}}$	Information Out
8	$\overline{\text{IR-28}}$	Information Out	33	IR-41	Information Out
9	IR-29	Information Out	34	$\overline{\text{IR-41}}$	Information Out
10	$\overline{\text{IR-29}}$	Information Out	35	IR-42	Information Out
11	IR-30	Information Out	36	$\overline{\text{IR-42}}$	Information Out
12	$\overline{\text{IR-30}}$	Information Out	37	IR-43	Information Out
13	IR-31	Information Out	38	$\overline{\text{IR-43}}$	Information Out
14	$\overline{\text{IR-31}}$	Information Out	39	IR-44	Information Out
15	IR-32	Information Out	40	$\overline{\text{IR-44}}$	Information Out
16	$\overline{\text{IR-32}}$	Information Out	41	IR-45	Information Out
17	IR-33	Information Out	42	$\overline{\text{IR-45}}$	Information Out
18	$\overline{\text{IR-33}}$	Information Out	43	IR-46	Information Out
19	IR-34	Information Out	44	$\overline{\text{IR-46}}$	Information Out
20	$\overline{\text{IR-34}}$	Information Out	45	IR-47	Information Out
21	IR-35	Information Out	46	$\overline{\text{IR-47}}$	Information Out
22	$\overline{\text{IR-35}}$	Information Out	47	IR-48	Information Out
23	IR-36	Information Out	48	$\overline{\text{IR-48}}$	Information Out
24	$\overline{\text{IR-36}}$	Information Out	49		Signal Ground
25	IR-37	Information Out	50		Chassis Ground

SECTION III
PRINCIPLES OF OPERATION

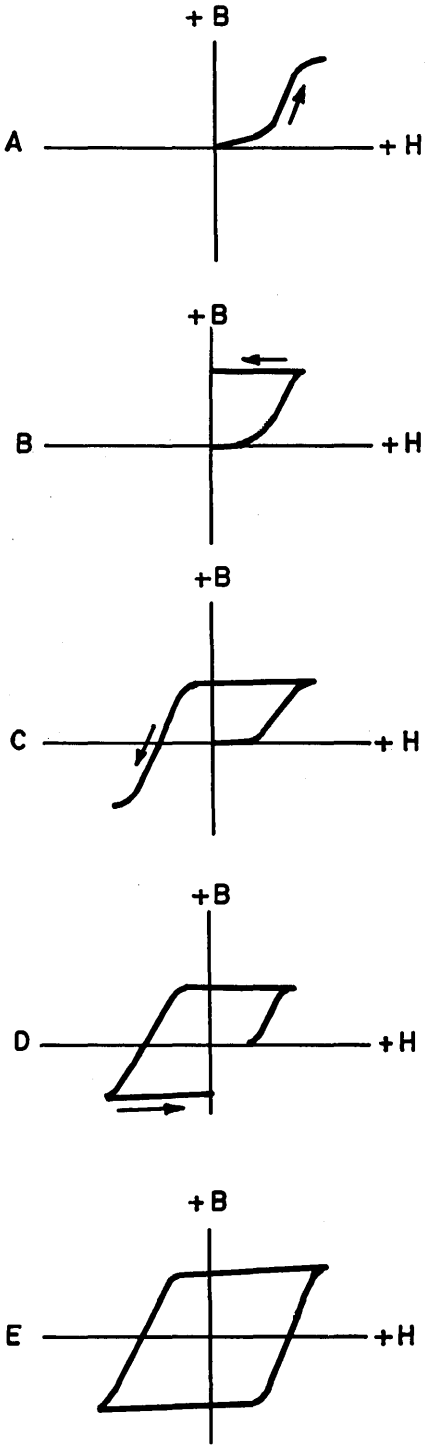
3-1 PRINCIPLES OF MAGNETIC CORE MEMORIES

3-1.1 Magnetic Core Storage

The memory core stack, housed in the magnetic core unit, is a matrix configuration of individual small (50 mils O.D., 30 mils I.D.) ferrite cores. The cores are arranged in identical planes, each plane having X-rows and Y-columns. Basically, the ferrite core is a 1-bit storage element in the form of a ferrite ceramic ring that can be magnetically saturated to either positive or negative flux density. The ferrite material retains a large part of the magnetic flux developed at the time the core is saturated which is an important characteristic of the core. The time required to switch a core from one polarity or state to another is primarily dependent on the core material and size. Consequently, cores measuring only millimeters in diameter are used in the memory core array to permit fast switching speeds.

A similarity exists between the magnetic core and the flip-flop in that both provide storage for one bit of data. The two extremes of saturation in a magnetic core represent ZERO and ONE, as do the two stable states of a flip-flop. A core can be set to a ONE state by the application of a current pulse of similar magnitude applied in the opposite direction. Similarly, a flip-flop is set or reset by applying pulses to the appropriate inputs. Both the magnetic core and the flip-flop provide memory of the last pulse applied, but the core does so without requiring power to hold its state.

The ferrite core has a nearly rectangular hysteresis loop. The hysteresis loop is a graphical representation of the flux density produced in a magnetic material, plotted against the magnetizing force that produces it. Figure 3-1 is a simplified drawing showing the generation of a typical ferrite



As Positive Current Increases Rising Flux Density is Limited by Core Saturation

Most of the Flux Remains after the Current is Removed.

As Negative Current Reaches the Switching Point, the Core is Driven to Negative Saturation

As with Positive Current, when Negative Current is Removed, Most of the Flux Remains

Thus, the Core is always Saturated in the Positive or Negative Direction

Figure 3-1. Ferrite Core Hysteresis Loop

core hysteresis loop. Starting with an unmagnetized core, an increase in magnetizing current (H) increases the flux density (B) along the S-shaped curve (3-1A). The flux density levels off when the core is saturated, and any additional current applied does not appreciably increase the flux density because the core material is supporting as much flux as it can. As the current is decreased, then made to flow in the opposite direction, the flux does not collapse along the same line (3-1B); and most of the flux remains even after the current has fallen to zero. The amount of flux actually remaining is a function of the retentivity of the magnetic material. As a magnetizing current is applied in the opposite direction, it has little effect on the flux level until the current reaches the knee of the hysteresis loop. (Note that a certain amount of current is required to overcome the residual magnetism to return the core to a neutral condition.)

A slight increase in current beyond the knee of the curve switches the core rapidly to negative saturation (3-1C). The point on the curve representing the amount of current required to change the state of the core is termed the coercive current. When the negative magnetizing current is removed, most of the flux is retained as before (3-1D). Note that the original sweep from a magnetically neutral condition is never repeated (3-1E). A memory core in coincident-current use is never in a neutral condition, but is switched from one saturated state to the other. The core is thus an extremely useful binary component because it can exist in either of two stable states and can switch rapidly from one to the other.

For any given toroidal magnetic core, the necessary magnetomotive force required to effect switching is a function of the product of the number of turns of wire and the current driven through those turns. It is not economically feasible to wind multiple turns of wire around the small toroidal cores used in core memories; rather the number of turns is reduced to two, one in each of the perpendicular driving coordinates, and the current in these coordinate wires is of such a magnitude as to cause switching (rapid flux change) to occur.

In addition to the perpendicular (X and Y) coordinate selection lines, each core is also threaded by two other wires, each of which passes through every core in a plane. One is the sense winding, which detects flux-change

due to switching of a core and thus provides a readout signal from the plane. The other winding is the inhibit winding which is used, as its name suggests, to inhibit or prevent the writing of a ONE into the core, thereby causing ZERO to be stored. A single memory core, with its associated control windings is illustrated in Figure 3-2.

A disadvantage of the memory core is that it does not provide a static indication of its state, as does a flip-flop. To obtain an indication of the condition of the flux in a memory core, the state of the core must be switched.

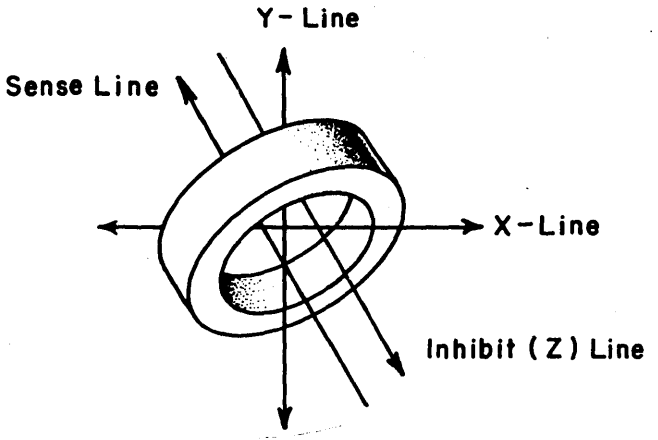


Figure 3-2. Core Control Windings

3-1.2 Addressing

The complete core stack for a magnetic core unit consists of a number of individual matrices or planes. Each plane contains memory cores assembled in a rectangular configuration. The memory cores are threaded by X- and Y-lines in each plane so that one memory core is physically located at each junction of an X-line and Y-line.

As previously stated, pulses of current applied along the X- and Y-lines switch a memory core from one state to another. If one-half of the current required to switch a core is applied along the X-line, and one-half of the necessary current is applied along the Y-line, the core situated at the

junction of the energized X- and Y-lines will receive the full switching current. This type of operation is termed coincident-current operation.

A coincident-current magnetic core memory depends upon the coincidence of two half-currents to read data from or to write data into the cores. Two additive half-current pulses will set the core to the ONE state, while two half-current pulses applied in the opposite direction will reset the core to the ZERO state. A core with two half-current inputs is essentially an AND circuit requiring that half-current be applied to both X- and Y-lines in the same direction to change the state of the flux at the core. A half-current applied to one line without a similar half-current applied to the other line has no effect on the core.

Only one X-line and one Y-line of a plane are energized during a single cycle, and only that core situated at the junction of the activated X- and Y-lines will respond to the coincident half-current pulses. Therefore, only one core in each plane will be affected during a single cycle. A simplified diagram of coincident-current selection of a memory core is illustrated in Figure 3-3. In effect, the X-line selects one row (X-row), and the Y-line selects one column (Y-column).

In coincident-current memories, the X- and Y-lines are wired in series through all planes of the memory core array. Thus each X-line and each Y-line threads corresponding rows or columns of cores in all memory planes. Energizing one of the X-lines (designated X_1 through X_m in Figure 3-3) supplies a half-current pulse to the appropriate row of cores in every plane. Similarly, energizing one of the Y-lines (designated Y_1 through Y_n), supplies a half-current pulse to the appropriate column of cores in every plane. When pulses occur simultaneously on two lines (X and Y), they select the same core position in each of the planes. Therefore, the X- and Y-lines select a word in the memory core array and enable read or write operations.

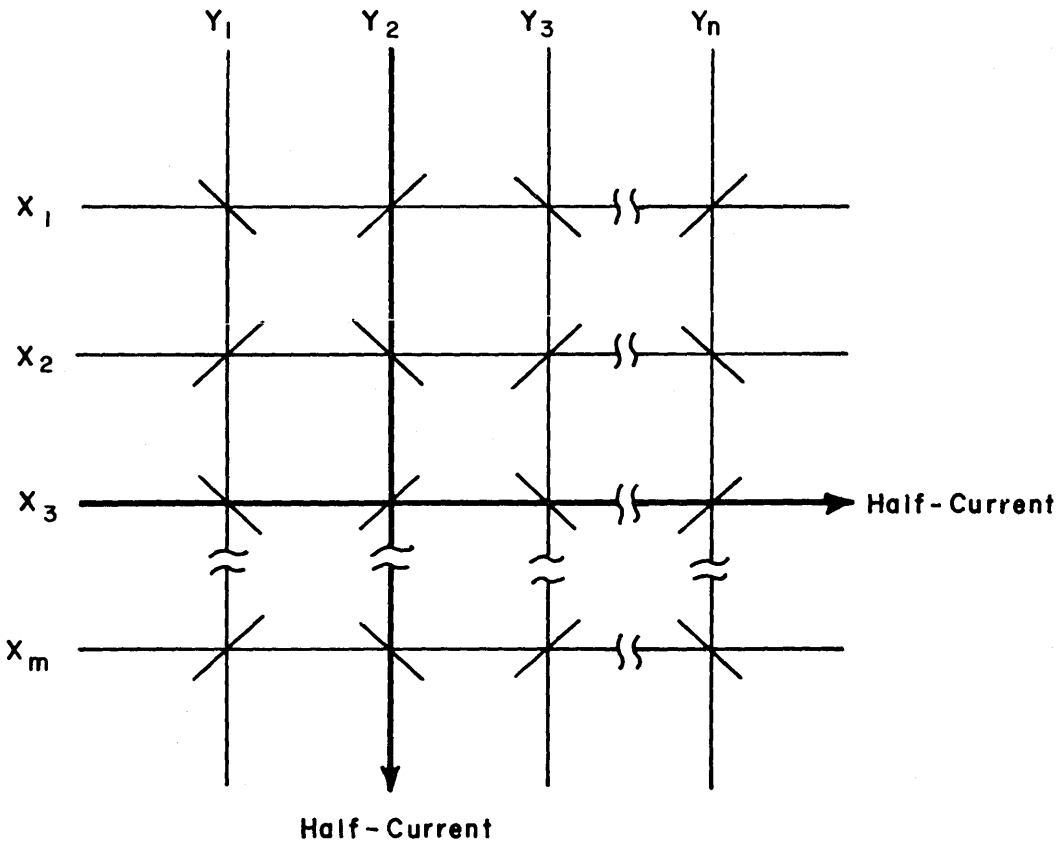


Figure 3-3. Coincident-Current Selection

3-1.3 Information Sensing

Sense lines allow the reading of information stored in the cores. One sense line (Figure 3-2) is threaded through all memory cores of each plane.

To read any of the words stored in memory, half-currents in the proper direction are generated in the selected X- and Y-lines (Figure 3-3). The read half-currents combine at the coincident junction of the X- and Y-lines to change the state of the affected core in each memory plane. If the affected core is storing a ONE at that instant, the effect of the read half-currents will change the state of the core to ZERO. If the core was previously in the ZERO state, the read half-currents will have no effect on the core. When the core is switched from the ONE to the ZERO state, the rapid

change in flux from positive saturation to negative saturation induces a voltage pulse in the corresponding sense line. Therefore, the presence of a voltage pulse in the sense line during the read operation indicates that a ONE had been stored in the indicated core. If no voltage pulse occurs in a sense line during read operation, a ZERO is indicated. The sense lines designated S_o through S_k in the memory core stack are connected to sense amplifiers. A ONE input to any of the sense amplifiers is amplified and applied to the information register. Thus, output data is transferred from its storage location in the core stack to the information register.

3-1.4 Writing

Inhibit lines are used to enable a computer word or instruction to be written into memory at a selected address location. A single inhibit line is threaded through each memory core in a plane (Figure 3-2), and each plane of the magnetic core unit requires an individual inhibit line.

To write information into memory, half-current pulses in the direction opposite to those generated for read operation are applied to the selected X- and Y-coincident junction to switch the affected core in each memory plane.

Since all the cores at the selected address have been cleared to the ZERO state prior to the application of the write half-currents, the write half-currents operate to switch all cores to the ONE state. If the incoming data dictates that a ZERO is to be written into a specific core, some means must be used to prevent the core from switching to the ONE state when the write half-currents are generated. This is accomplished by the inhibit (Z) lines designated Z_1 through Z_k. An inhibit pulse, when transmitted through the inhibit line of the memory plane at the same time that the write half-currents are applied through the X- and Y-lines, prevents the writing of a ONE because the inhibit current subtracts from X- and Y-write current.

The inhibit pulse is of the same magnitude but of the opposite polarity to the write half-current pulses. Therefore, the inhibit pulse directly cancels the effect of one write half-current pulse. The net effect of the two write half-current pulses and an inhibit pulse, is equivalent to a single write

half-current pulse on the addressed core. This prevents the core from switching from the ZERO to the ONE state.

Information to be written into memory is stored in the information register prior to being transferred to the memory core stack. During the transfer operation, a binary ONE from the register flip-flop will prevent the generation of an inhibit pulse whereas a binary level ZERO from the register flip-flop allows an inhibit pulse to be generated. In this way information is rewritten (or new information is written) into the selected memory location exactly as it appears in the information register.

3-1.5 Information Retention

The magnetic core unit does not require power to provide static memory capability. A pulse of power is required to switch the cores from one state to another, but not to hold cores in their respective states. All cores remain in the state to which they have been switched, because of the retentivity of the core magnetic material. If power is removed or lost without a severe transient pulse being generated, the core stack retains the stored information indefinitely.

3-2 GENERAL SPECIFICATIONS, TCM-32 MEMORY SYSTEM

Capacity:

Words: 128, 256, 512, 1024, 2048, and 4096

Word Length: 8 to 48 bits (in 2-bit increments)

Cycle Time:

Full Cycle: 5 μsec

Half Cycle: 3 μsec

Access: 2.3 μsec

Modes of Operation:

Clear/Write

Read/Regenerate

Load

Unload

Read/Modify/Write

Operating Temperature:

0°C to 50°C

Humidity:

95% without condensation

Power:

+12 VDC
-6 VDC
-18 VDC

As supplied by S-PAC Series RP-31 or equivalent

Options:

Read/Modify/Write

Sequential Addressing

Random-Sequential Addressing

Sequential-Interlace Addressing

Serial Address-Register Operation

Memory Clear

Information-Register Partitioning

Serial Information-Register Operation

Physical Description:

Standard 19-in. drawer mount

10-1/2 in. high

20-3/4 in. deep

135 lb maximum

Input Signal Specifications:

a. All input circuits are designed to operate between 0 V and -6 V.

b. All inputs are diode coupled/isolated and provide noise rejection margins of 1.5 V minimum.

c. Each input requires a flow of approximately 2.5 ma, when the driving source is at ground and approximately 0 ma when the driving source is at -6 V.

d. Each input that is not strobed or clocked must have a maximum rise time of 0.2 μsec (10% amplitude point to 90% amplitude point). Minimum pulse width is 0.3 μsec.

e. Those inputs which are clocked or strobed may rise at any desired rate as long as they fulfill specified timing requirements.

Output Signal Specifications:

a. Outputs will swing between 0 V and -6 V. All outputs clamped.

b. All outputs are capable of driving 400 μμf of stray capacitance in addition to 20 ma from ground.

c. Typical rise times are 0.1 μsec. Typical fall times are 0.15 μsec.

3-3 TCM-32 FUNCTIONAL DESCRIPTION

The basic function of the TCM-32 memory system is the magnetic core storage of information which is fed to the memory by an external system (typically, a computer) and the restoration of the information to the external system upon command. A block diagram of the TCM-32 memory is presented in Figure 3-4, to which this functional description is referenced.

3-3.1 Address Register

The address register (AR) of the memory system is composed of MF-30 flip-flops. The AR stores the selected address in static flip-flops for a specified cycle, and the AR outputs drive the X- and Y-decoders. In any of the optional sequential-addressing arrangements, the AR is wired and operated as a counter.

3-3.2 X- and Y-Decoders, Switches, and Drivers

The X- and Y-decoders and switches decode the contents of the AR so that only one memory location is selected. A specific address input activates one X-row of memory cores and one Y-column of memory cores, as shown in Figure 3-3. The selected switches allow the drive currents to read from and write into the corresponding cores of the memory array. (The current pulses are generated from temperature-compensated, dynamically regulated drivers, the outputs of which are essentially independent of supply voltages.)

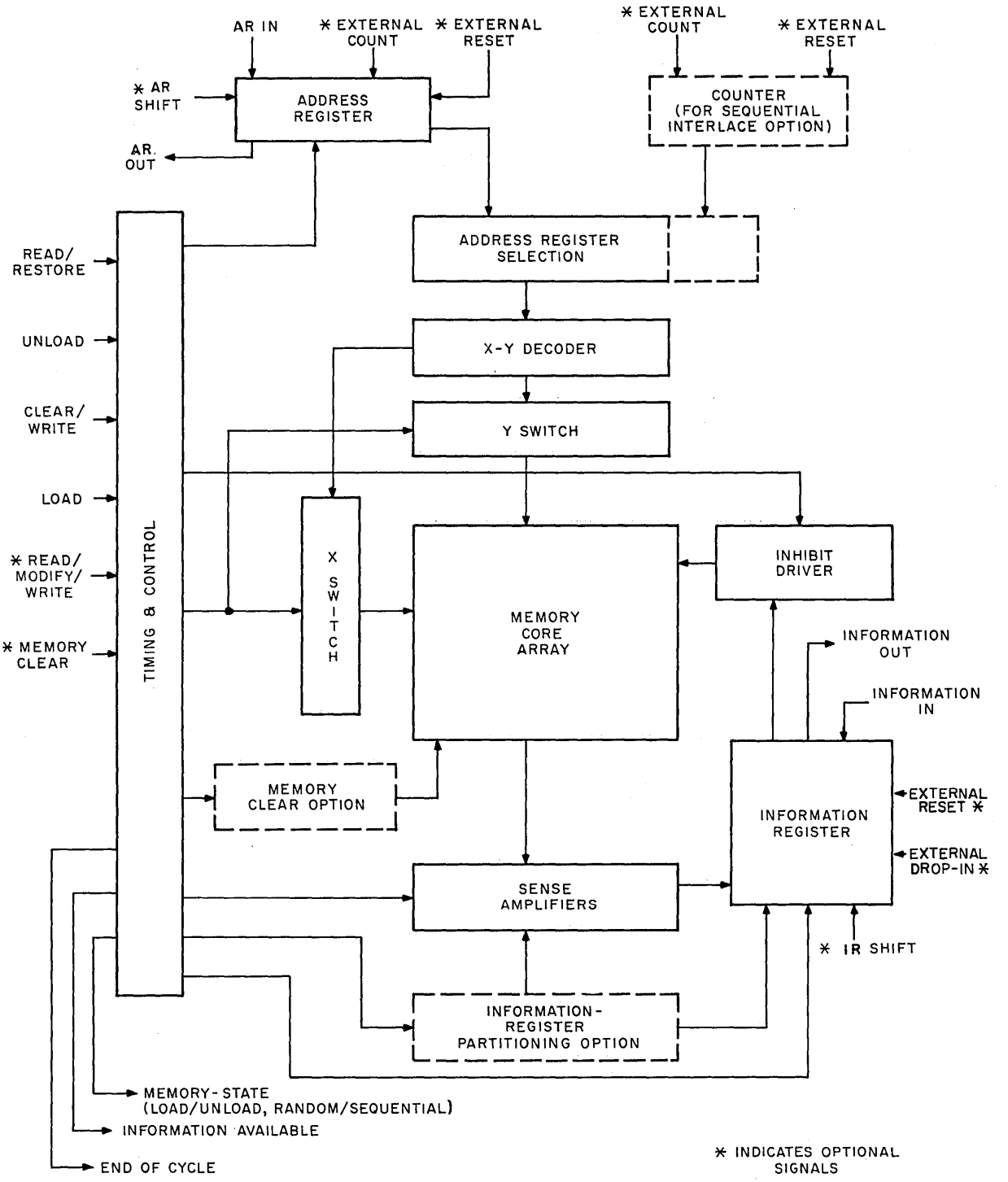


Figure 3-4. TCM-32 Memory System, Block Diagram

3-3.3 Memory Timing and Control

The memory timing and control circuits provide the sequence of pulses necessary to carry out the specific operation (read/regenerate, clear/write, load, unload, and optionally, read/modify/write). Timing and control also generates the memory-busy signal, memory-state indicator signal, an information-available marker, and an end-of-cycle marker pulse.

3-3.4 Memory Core Stack

The principles of the memory core stack are described in detail in Section 3-1. The core stack utilizes a four-wire coincident-current wiring scheme and consists of a number of individual planes, each of which contains magnetic cores assembled in an X- and Y-configuration.

3-3.5 Information Register

The information register (IR) stores one information word which is to be inserted into the memory during a load or clear/write cycle. The IR also provides output information during an unload or read/regenerate cycle. This register is composed of flip-flops, and if the IR partitioning option is employed, the portions, or zones, of the IR may be operated independently. The IR provides double-rail outputs to the external system.

3-3.6 Sense Amplifiers

The sense amplifiers receive the output of the selected cores through the sense lines, reject noise, and amplify the outputs to set the information register. The memory system has a separate sense amplifier for each bit of an information word. A sense winding common to all cores in a memory plane detects a change of state of an addressed core and provides an input signal to the associated sense amplifier. One bit of the selected word is applied to each sense amplifier, thus transferring the addressed word from storage to the IR, for further transfer to the external equipment.

3-3.7 Inhibit Drivers

Each inhibit Driver PAC, Model MI-32, contains eight circuits and controls eight bits of a word. Each channel of an MI-32 PAC receives an input from the assertion output of one information register flip-flop. A timing signal (ZS or Z-step) is also received which is amplified to enable and properly time any channel. The MI-32 PAC is described in the PAC appendix. Each inhibit driver controls the flow of inhibit current through one plane of the memory core stack. Inhibit-driver conduction produces a half-select current when a ZERO is to be stored during load, clear/write or read/regenerate memory operations. An IR flip-flop disables its associated inhibit driver when a ONE is to be stored.

3-3.8 Current Drivers

The two Current Driver PACs, Model MD-32 are used in each TCM-32. A channel receives input signals from the $\overline{RS}$ or $\overline{WS}$ (read step or write step) gate and provides a selection current of proper rise-time, fall-time, and amplitude to a selected line. The MD-32 is described in the PAC appendix. Potentiometers for setting the output current amplitude are located adjacent to the core stack enclosure in unit 2.

3-4 FUNCTIONAL DESCRIPTION OF SELECTION AND DRIVING TECHNIQUE

3-4.1 Memory Core Stack

A typical schematic diagram of the memory core stack used in the memory system is illustrated in Figure 3-5. The ends of one side of the Y drive lines are connected in groups. Each group connects to a transistor switch on a Selection Switch PAC. The other side of the Y drive lines connect to outputs 16 through 31 of a Selection Switch PAC. The decoded input address information selects a transistor switch on each side of the Y drive lines. The logic design of the selection switches is such that only one line is selected for any input address. The X drive line connections are similar to the Y drive line connections.

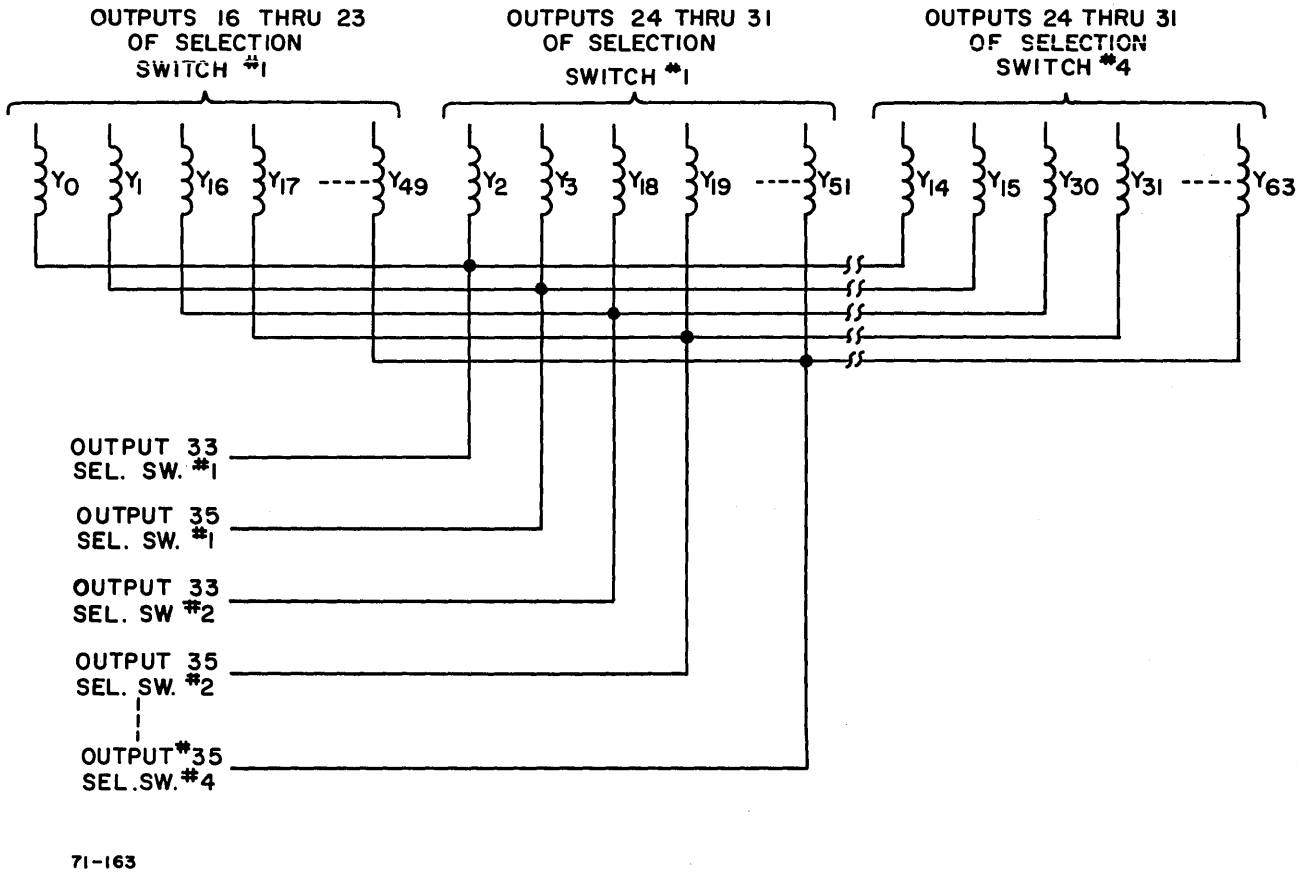


Figure 3-5. Memory Core Stack, Simplified Schematic Diagram of Y-Coordinate Sense, and Inhibit

Inhibit driver outputs are applied to the corresponding inhibit lines designated Z_k. Resistors located on separate component boards control inhibit current amplitude and provide transient damping. (Information on the component board is included in the appendix.) The inhibit lines control the insertion of data into the memory core stack for storage

The sense lines control the extraction of data from storage within the memory core unit. A sense winding threads every core in a plane to minimize output signals due to inductive or capacitive coupling to other windings and those due to certain nonideal electrical characteristics of the magnetic cores.

3-4.2 Selection Switches

The X-row selection and Y-column selection are composed of Selection Switch PACs. Relevant sets of digits of the address register are decoded and applied to the Y-column selection switches. Similarly, other sets of digits are decoded and applied to the X-row selection switches. Since only one X drive line and one Y drive line are selected for a given address register content, only one address receives the full coincident-current.

The method of selecting only one X drive line (or similarly one Y drive line) is demonstrated by the simplified selection diagram (Figure 3-6). To select drive line X_o, switches Q1 and Q3 are turned on by coincidence of decoded address information (OD_A and OD_B) and the read pulse (RP). The other six switches are off. Read current flows from ground through Q3, memory line X_o, CR1 and Q1 to the read current source. The diodes are needed to steer the current through only the selected line. For instance, the current can not flow through the path Q3-X2-CR6-CR8-X3-X1-CR3 and Q1 because of the reversed biased diode CR6.

During the write portion of the cycle, Q2 and Q4 are turned on by coincidence of the write pulse (WP) and OD_A and OD_B, respectively. Switches Q1 and Q3 are off due to the absence of a read pulse, and Q5, Q6, Q7, and Q8 are off due to the absence of an OD pulse. The write current flows from ground through Q2, CR2, X_o and Q4 to the write current source. The actual method used by the memory system to select the memory lines is explained as follows.

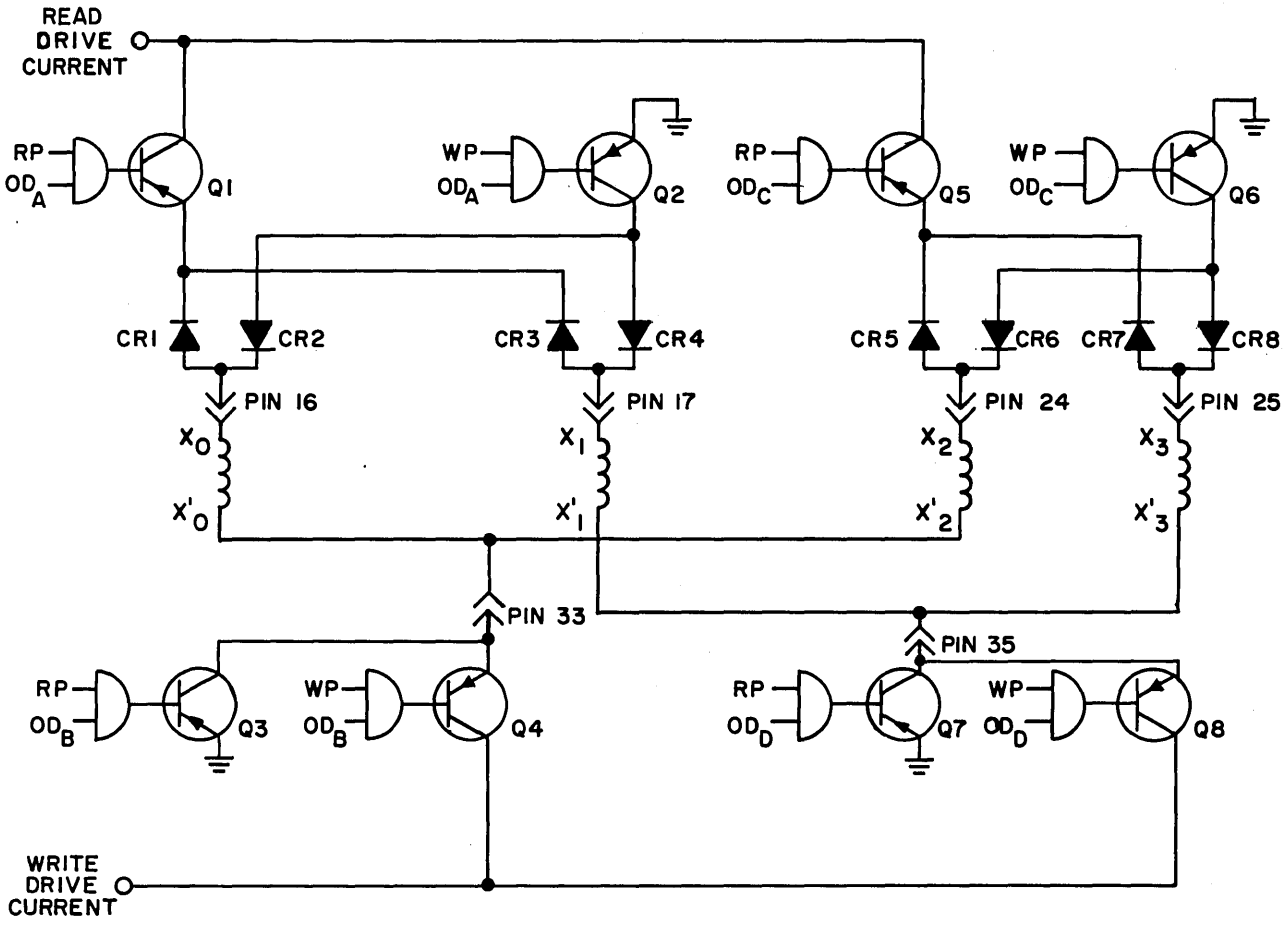


Figure 3-6. Simplified Selection Diagram

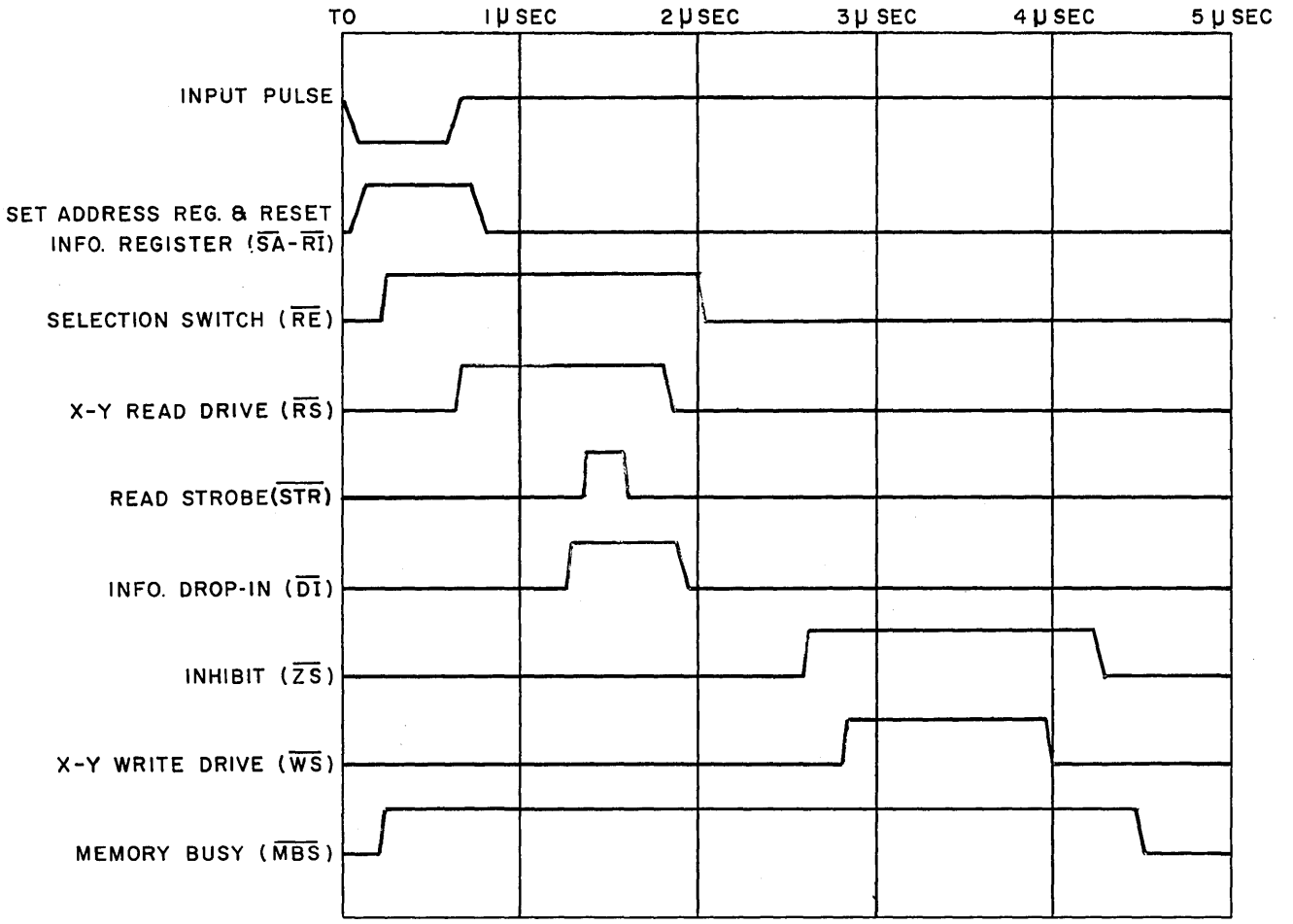


Figure 3-7. Internal Timing

Contents of the address register are decoded in groups; that is, groups of three bits may be decoded into one of eight outputs via DP-32 (S-117).

Enabled outputs of the decoders go to particular inputs of Selection Switch PAC, SS-32, in which they are in turn gated against a read pulse or write pulse input to enable driver current flow of one polarity or the other through the selected coordinate lines.

3-4.3 Indicator Option

When used, the indicator option includes incandescent indicators on the front panel, associated LD-30 Driver PACs, and the Indicator Power Supply, Model PI.

3-5 OPERATING CYCLES

3-5.1 Standard Cycles

The four standard operating cycles of the TCM-32 Magnetic Core Memory are load, unload, clear/write and read/regenerate. The operating cycle or mode is selected by separate control pulses which are generated by the computer or external system. The control circuits are shown in the memory block diagram of Figure 3-4. The internal timing signals are shown in Figure 3-7, and the various internal logic signals are identified in Table 3-1.

3-5.1.1 Read/Regenerate Cycle (Figure 3-8). - The read/regenerate cycle transfers a selected word from storage to the information register upon command. As the reading process requires the resetting of all selected cores to ZERO (destructive readout) the information in the information register is reinserted into core storage to avoid loss of the information. The information is also retained in the information register for use by the external system. A read/regenerate command is required for each word unloaded.

The read/regenerate sequence is as follows.

1. A core storage location corresponding to the word in the address register is selected.

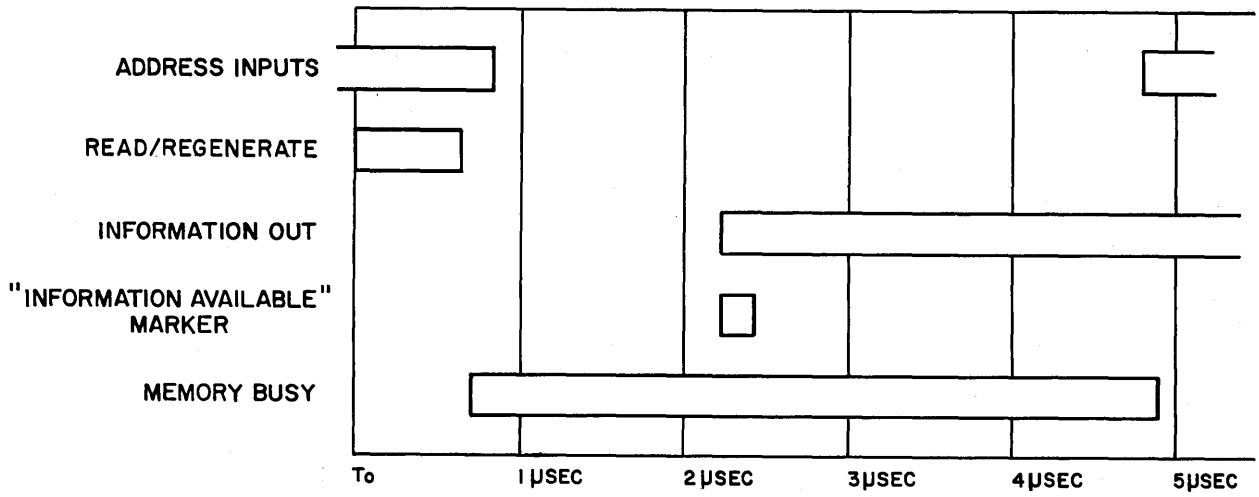


Figure 3-8. Read/Regenerate Cycle External Timing

2. Information stored in the selected core storage location is read out into the information register, from which it is available to the external system. The information is also held in the information register.

3. The information in the information register is regenerated into core storage at the selected address.

The internal timing of the read/regenerate cycle is generated by two TD-32 PACs in the timing and control section of the memory (positions 22 and 23 of Unit 1). The first TD-32 generates the proper timing signals for the read half of the cycle; the second TD-32 generates the outputs and internal timing signals required for the regenerate portion.

Upon the initiation of a read/regenerate pulse, two timing pulses are generated by the TD, set address (SA), and reset information register ($\overline{RI}$). These pulses set up the new address in the address register and clear the information register to all ZEROs. Pulse RE next enables the selection switches to direct read the drive currents to the proper address. After the selection switches are enabled, the X and Y drive currents are turned on and timed by $\overline{RS}$. The outputs from the bits of the selected word are amplified by the sense amplifier. The read strobe pulse ($\overline{STR}$) forms a part of the

detection of a logical ONE. Pulse $\overline{STR}$ follows the X-Y drive currents so that it occurs at the exact time when the core turnover of a ONE being read out is at its peak. The outputs from the read amplifier are directed to the information register which is then set up according to the information read from the memory stack. The outputs of the information register supply the word to the external system.

The regenerate portion of the read/regenerate cycle is started by the inhibit drive pulse (ZS) which turns on the inhibit drivers. The width of this pulse brackets the X-Y drive pulse ($\overline{WS}$) and, together with $\overline{WS}$, will restore the information word into the selected storage location. The end of ZS signifies the end of the read/regenerate cycle.

3-5.1.2 Clear/Write Cycle (Figure 3-9). - The clear/write cycle sets all the storage cores of the selected address to ZERO, thenloads the cores with an information word. A separate clear/write command is required for each word loaded and information is not read out when the cores are cleared.

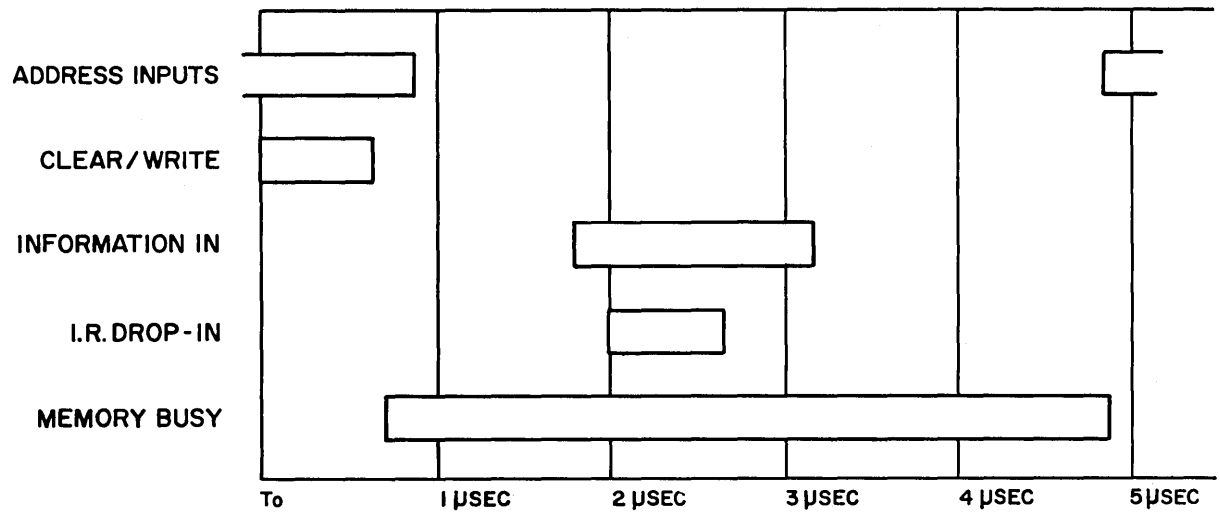


Figure 3-9. Clear/Write Cycle External Timing

The clear/write cycle is made up of the following steps.

1. The core storage location corresponding to the word in the address register is selected.

2. The selected location is cleared of all previously stored information.

3. New information from the external system or computer is loaded into the information register.

4. The information in the information register is then written into the cleared storage location.

The clear/write cycle is initiated by an input pulse on the clear/write line. This cycle follows the same timing as does the read/regenerate cycle with one exception: a DI (information drop-in) signal will be generated to transfer the information into the information registers, and the read strobe ($\overline{\text{STR}}$) pulse will not be present. The functional differences between the clear/write cycle and the read/regenerate cycle are as follows. The former will select a location, clear the information from that location, and write in the new information generated by the external system. The read/regenerate operation, on the other hand, will select a location, read the information from this location into the information register from which it can be sampled, and then restore the identical information back into the selected location in storage.

3-5.1.3 Load Cycle (Figure 3-10). - In the load cycle one information word is transferred from the information register to the storage cores at a selected address in response to a load command. The number of words stored is limited only by the word capacity of the core storage, but a separate load command is required for each word. Unless one of the optional methods of sequencing the address register is used, an externally generated address is required for each load command.

A load cycle consists of the following steps.

1. A core storage location is selected which corresponds to the address word held in the address register.

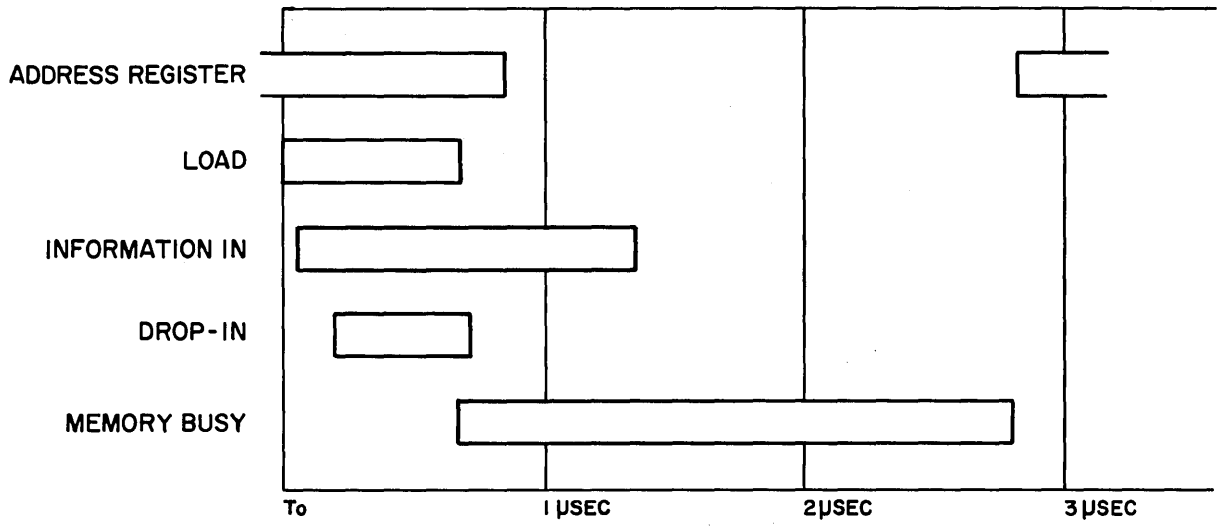


Figure 3-10. Load Cycle External Timing

2. An information word from the external system is loaded into the information register.

3. The information word in the information register is written into the selected core storage location.

The load cycle is identical to the second half of a read/regenerate or clear/write operating cycle. Upon the application of an externally generated load pulse, the second TD-32 PAC in the timing chain is activated. The load cycle has no provision for clearing the location to be written into. Therefore, this location must have been cleared (reset to ZERO) at the start of the load cycle.

3-5.1.4 Unload Cycle (Figure 3-11). - The unload cycle transfers one information word from core storage into the information register upon command. An externally generated address is required for each unload command unless the memory system is equipped with an optional method of automatically sequencing the address.

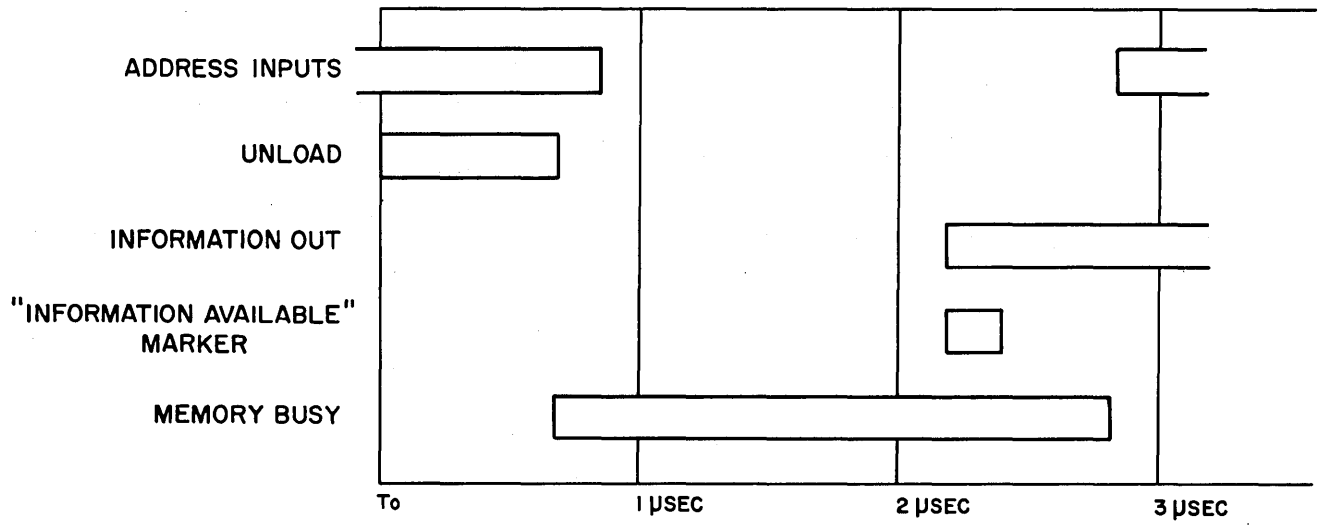


Figure 3-11. Unload Cycle External Timing

The unload cycle is identical to the first half of the read/regenerate or clear/write cycle. It is initiated by an external pulse applied to the unload command line. This pulse triggers the first TD-32 PAC in the timing chain. The timing chain produces the same timed sequences which are described in the read portion of the read/regenerate cycle. The second TD-32 is prevented from being triggered by the "not half cycle" signal ($\overline{HC}$). The $\overline{HC}$ signal is generated by the output of a flip-flop, which is controlled by the unload input command. Because the unload cycle results in a destructive readout, it will leave the addressed location in a cleared or "reset to ZERO" state.

TABLE 3-1.
INTERNAL LOGIC SIGNALS

NOTE

Positive-going (-6 volts to 0 volt) signals are indicated by a bar over the signal designations.

Designation	Identification
CW	Clear/write command
RR	Read/regenerate command
LB	Load command
UB	Unload command
SA	Set address register
RI	Reset information register
RE	Enable read selection switches
$\overline{\text{RS}}$	X-Y read drivers
$\overline{\text{STR}}$	Read strobe
DI	Information drop-in
ZS	Inhibit step and enable write selection switches
$\overline{\text{WS}}$	X-Y write drivers
MBS	Memory busy signal
$\overline{\text{RMW}}$	Read/modify/write
RDM	Random access input
$\overline{\text{LBA}}$	Load set address
UCT	Unload address count pulse
LCT	Load address count pulse
RU	Reset unload counter
RL	Reset load counter
LC	Load counter
UC	Unload counter
HC	Half cycle
RAN	Random address
RRF	Permit $\overline{\text{STR}}$ (read/regenerate flip-flop)
L	Load state
U	Unload state

TABLE 3-1. (Cont)
INTERNAL LOGIC SIGNALS

Designation	Identification
$\overline{SB}$	Set busy
$\overline{SR}$	Start read
$\overline{ER}$	End read
$\overline{EE}$	End extract
$\overline{SZ}$	Start inhibit
$\overline{EZ}$	End inhibit
$\overline{EB}$	End busy

3-5.2 Optional Cycles

3-5.2.1 Read/Modify/Write. - A read/modify/write cycle can be incorporated into the operation of a TCM-32 Core Memory System on request. This option requires the addition of a read/modify/write control level. The read/modify/write cycle consists of an unload operation in which information modified by the external equipment is read out. The modified information is then returned to storage at the same address. The presence of the read/modify/write signal (RMW) inhibits the address from changing while the load cycle (LB) is being performed. If the operation is sequential, RMW prevents the generation of a count pulse at the end of the unload portion of this operation. Because both the load and the unload operations must be performed at the same location, the address must remain the same for both half cycles. Thus an RMW operation consists of the following steps.

1. Provide a ground level on the RMW line and hold it throughout the extent of the operations below
2. Provide a UB command pulse
3. Receive data and supply new data to the TCM
4. Provide an LB command pulse

3-6 OPTIONAL MODES AND FEATURES

3-6.1 Sequential Addressing

When a memory is specified with a sequential method of addressing, the address register is wired as a counter. This is implemented in the wiring of the three MF-30 PACs in positions 14, 15, and 16 of Unit 3 (Figure 3-10). An external control is employed which will allow the operator to clear the address register to all ZEROs, so that either load or unload operations may be initiated at a defined address. If an address-clear signal is given, addressing will start at ZERO and at each subsequent load or clear/write command, the memory will sequence to the next address until the desired information is written into the memory. At this point an address-reset command signal can clear the address register back to the ZERO address, and information can be read from the memory by a read/regenerate or an unload command until the information has been read from memory in the same order as it was written.

3-6.2 Random-Sequential Addressing

The random-sequential mode of addressing is similar to the sequential method described above except that a random address may be provided to the memory at any time and the memory can sequence from that point to any of the operating modes. Random-sequential addressing requires the addition of two S-169 S-PACs in positions 12 and 13 of Unit 3 (Figure 3-12).

3-6.3 Sequential-Interlace Addressing

The sequential-interlace mode of addressing requires the addition of a second address register, which is provided by the three MF-30 PACs in positions 21, 22, and 23 of Unit 3 (Figure 3-12). This register is wired to operate as a counter and stores the unload address. The register consisting of the MF-30 PACs in positions 14, 15, and 16 of Unit 3 functions as the load counter. Gating of the load or unload register content to be used is performed by the S-169 S-PAC in position 18 (load) or the S-179 S-PAC, position 20 of Unit 3 (unload).

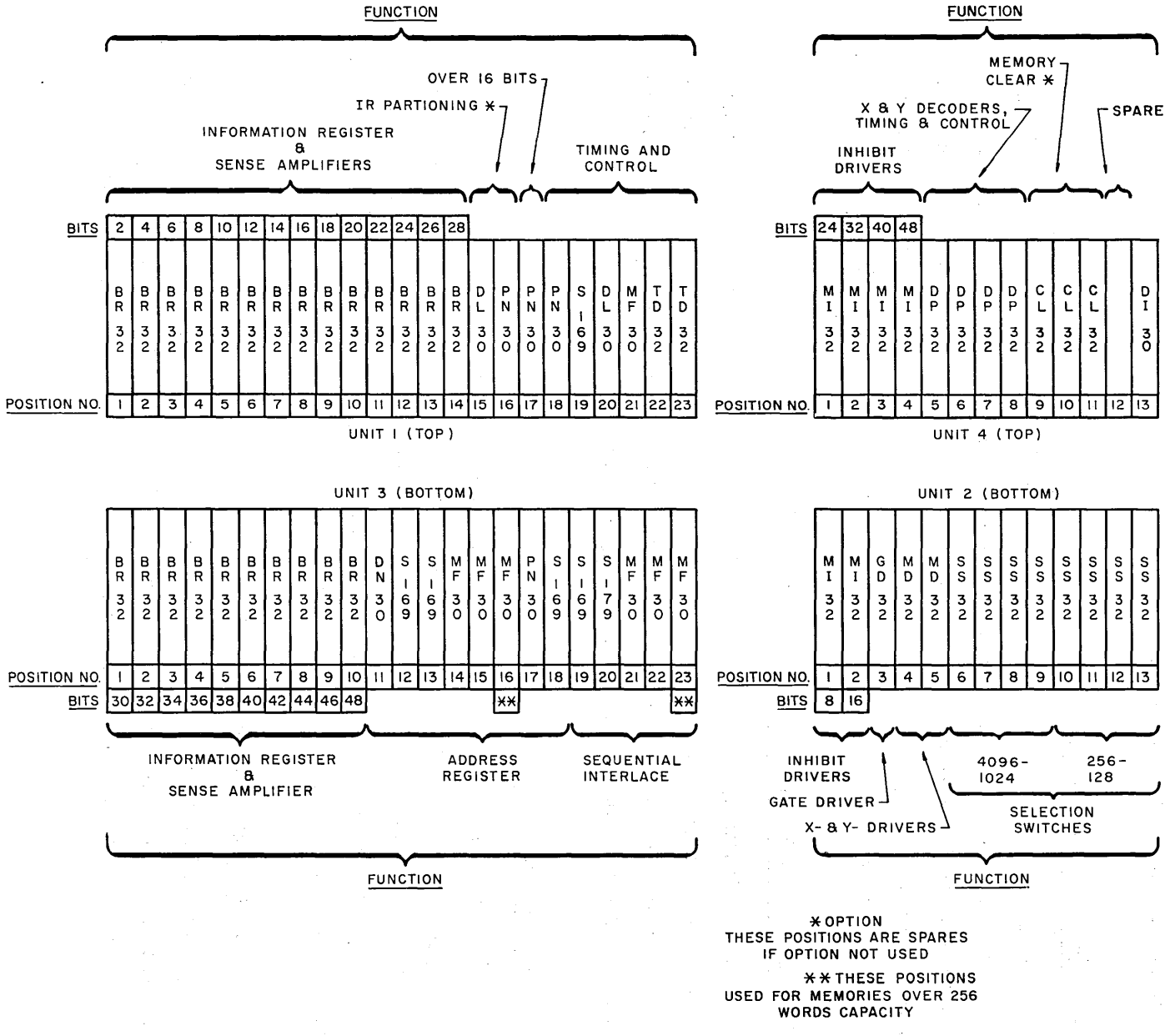


Figure 3-12. S-PAC Location and Functions

The sequential-interlace option allows load and unload cycles to be interlaced. That is, the memory may be loaded, and while continuing to be loaded, unload operations can be performed between the load cycles. Load and unload cycles may be interlaced in any sequence at any speed up to that allowed by the minimum cycle time.

3-6.4 Serial Addressing

The serial-addressing option is employed when it is desired to load the address register in a bit-serial manner. This is accomplished by wiring the address register (positions 14 through 16 of Unit 3) to operate as a shift register. When this option is used the address register can be loaded in a bit serial manner with a maximum shift rate of one megacycle.

3-6.5 Serial-Information Inputs

The information register may be wired to operate in a serial shift mode to receive a bit-serial input. In a similar manner, data in the information register can be shifted out bit-serial at a rate up to 1 MC, to convert a parallel output of the memory to a single chain of pulses.

3-6.6 Memory Clear

The memory-clear option, implemented by the inclusion of CL-32 PACs into positions 9, 10, and 11 of Unit 4 (Figure 3-12), provides a means of clearing all information contained in the core stack with one operation. This is accomplished by the application of a single positive-going pulse (from -6 volts to 0 volt) which has a duration of at least 1.5 μsec.

3-6.7 Partial Substitution

This optional feature provides the division of the information register into independently controlled groups of flip-flops. One group may be undergoing a clear/write operation while another group is simultaneously

operating in a read/regenerate mode. The partial-substitution option allows a portion of the information word to be changed without changing or destroying other parts of the word.

The implementation of this option, shown in Figure 4-8, utilizes the PACs located in positions 15, 16, 17, and 18 of Unit 1 (Figure 3-12). These PACs control the drop-in pulse to the information register and the strobe of the sense amplifier so that the information register can be separated into two, three, or four zones.

3-6.8 Signal Compatibility

Signal compatibility with voltage swings other than standard can be accommodated.

3-6.9 Indicators

Individual display lamps for address register and information register flip-flops can be added to the front panel of the TCM-32. Other control flip-flops can also be displayed to indicate the operating mode or condition of the memory.

SECTION IV
LOGIC

4-1 LOGIC DIAGRAMS

This section provides detailed logic diagrams of the various memory elements shown in the block diagram of Figure 3-4. The implementation of both standard and optional modes and operations are given as follows.

The logic diagram for the memory timing and control functions is presented in Figure 4-1.

Figure 4-2 illustrates the logical connections of the address register for random addressing, sequential addressing, and random-sequential addressing.

Figure 4-3 presents the logic diagram for the address registers as connected for the optional sequential-interlaced addressing mode.

The logic diagram for the X-Y decoders and selection switches is given in Figure 4-4.

Logic diagrams for the information register, sense amplifiers, and inhibit drivers are presented in Figure 4-5 (bits 1 through 16); Figure 4-6 (bits 17 through 32), and Figure 4-7 (bits 33 through 48).

Figure 4-8 is a logic diagram of the partial substitution option which shows the partitioning of the information register into two and four zones.

The optional memory-clear feature is shown in the logic diagram of Figure 4-9.

The locations of the PACs which provide these logic functions are shown in Figure 3-12.

4-2 INPUT/OUTPUT LOGIC SIGNALS

The various input and output logic signals used in the TCM-32 memory system are identified and defined in Table 4-1. The designations given in the following table are employed in the logic diagrams of Figures 4-1

through 4-9. Positive-going signals (-6 volts rising to 0 volt) are indicated by a bar over the designations.

TABLE 4-1.
LOGIC SIGNAL LIST

Designation	Identification
Standard inputs	
RR	Read/regenerate – operation command pulse
CW	Clear/write – operation command pulse
LB	Load – command pulse
UB	Unload – command pulse
A-1	AR input – address information for random access (levels)
I-1	IR input – input data for information register (double-rail levels)
RDM	Random – level to distinguish random access from sequential addressing
Standard outputs	
AR-1	AR outputs – address information from one side of flip-flop
IR-1	IR outputs – output data from both sides of flip-flop
Optional Inputs	
$\overline{\text{RMW}}$	Read/modify/write – level which allows memory to unload, delay, then load at the same address
$\overline{\text{MC}}$	Memory clear – pulse which clears all information from memory
$\overline{\text{AC}}$	AR clear – pulse which clears the address register
$\overline{\text{ARS}}$	AR shift – pulse which shifts the address register bit-serially (serial address option)
$\overline{\text{LAC}}$	Load address clear – pulse which clears the load address register (sequential-interlace option)
$\overline{\text{UAC}}$	Unload address clear – pulse which clears the unload address register (sequential-interlace option)
LCT	Load address count – count pulse which advances load address register (sequential-interlace option)

TABLE 4-1. (Cont)
LOGIC SIGNAL LIST

Designation	Identification
Optional Inputs (Cont)	
UCT	AR count – pulse which advances address register (all other sequential modes of addressing)
SA	AR set – pulse which strobes addressing data into address register
DI	IR set – pulse which strobes information into information register
RI	IR clear – pulse which clears information register
ICT	IR count – pulse which advances information register
TA, TB, TC, TD	Partial substitution (IR partitioning) – levels which control the information register zones as to RR or CW mode
IRS	IR shift – pulse which shifts information register (in bit-serial mode of operation)
Optional Outputs	
EC	End of cycle – pulse which signals the end of any cycle
MBS	Memory busy – level which will be -6 volts throughout any operating cycle
IA	Information available – pulse which signals that information can be sampled from the information register
PR	Power failure – indication of a power failure in the system
RAN	Random – level which indicates that the memory is operating in a random-addressing mode
SEQ	Sequential – level which indicates that the memory is operating in one of the sequential-addressing modes
L	Load – level which indicates that the memory is operating in a load mode
U	Unload – level indicating that the memory is operating in an unload mode

TABLE 4-1. (Cont)
LOGIC SIGNAL LIST

Designation	Identification
Operating Voltages	
+12 volts	Output of the power supply
- 6 volts	Output of the power supply
-18 volts	Output of the power supply
Signal ground	Ground level of the logic circuitry
Chassis ground	Ground level of the memory frame and rack

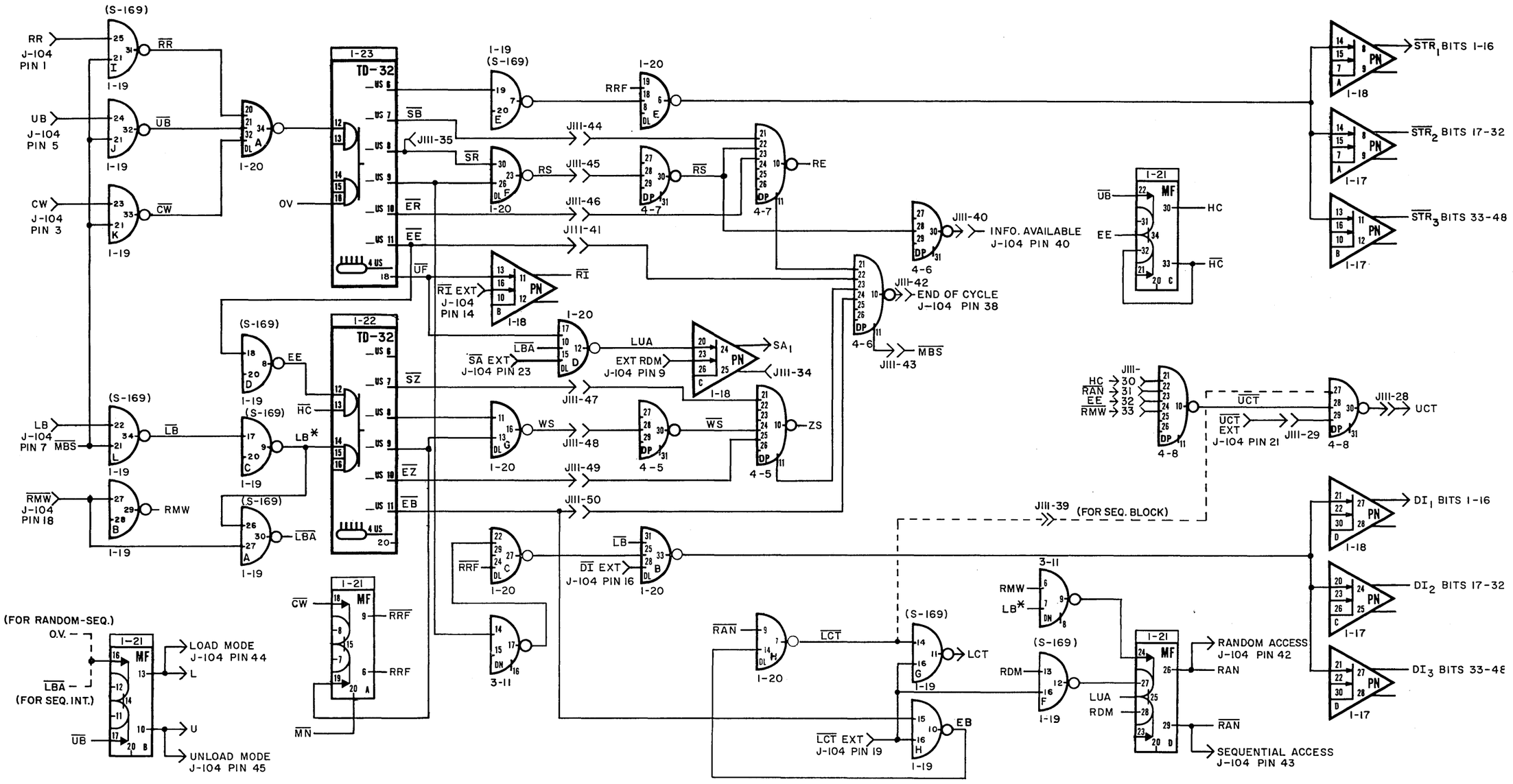


Figure 4-1. Memory Timing and Control, Logic Diagram

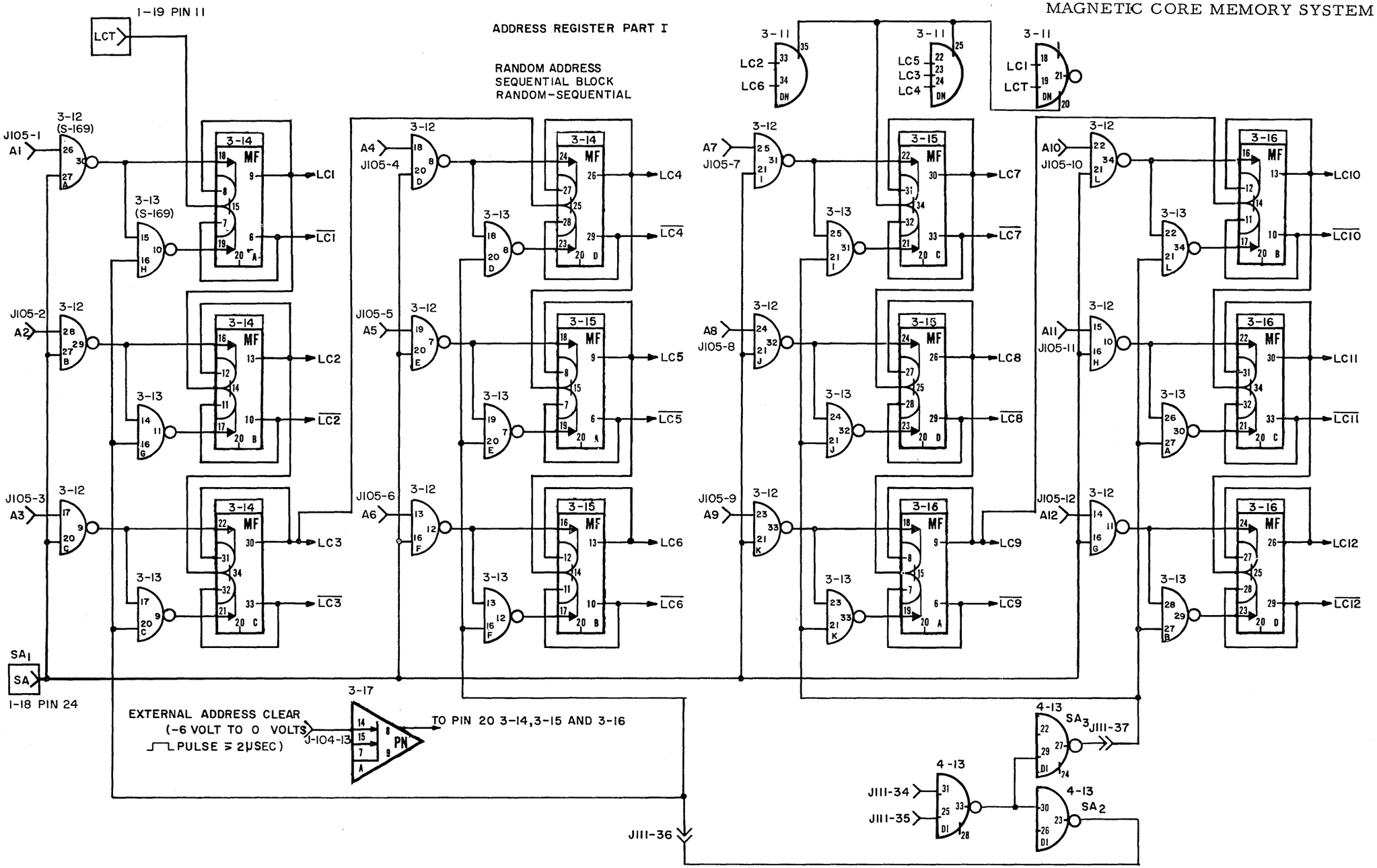


Figure 4-2. Address Register, Logic Diagram (Random Addressing, Sequential Addressing, and Random-Sequential Addressing)

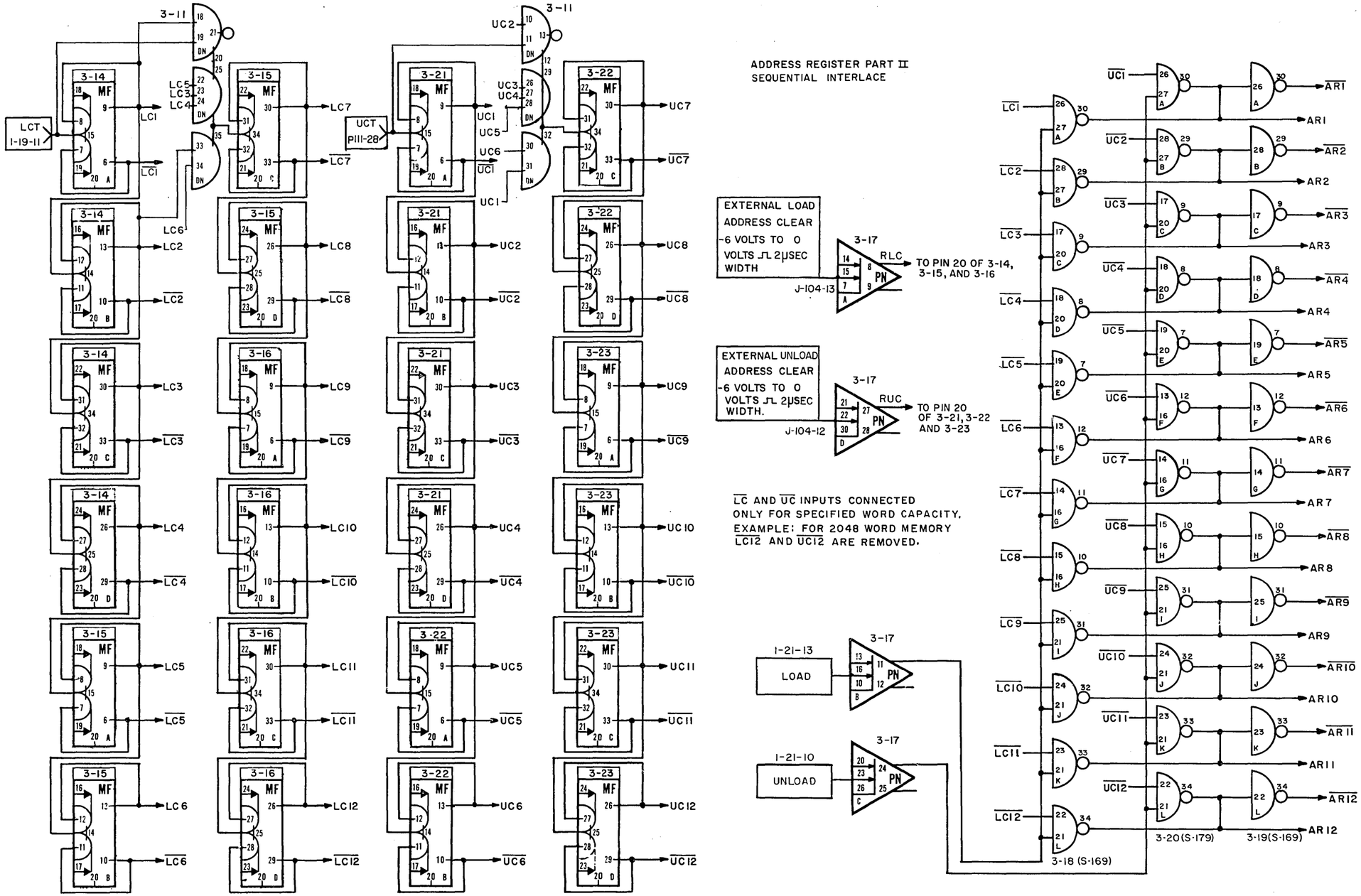
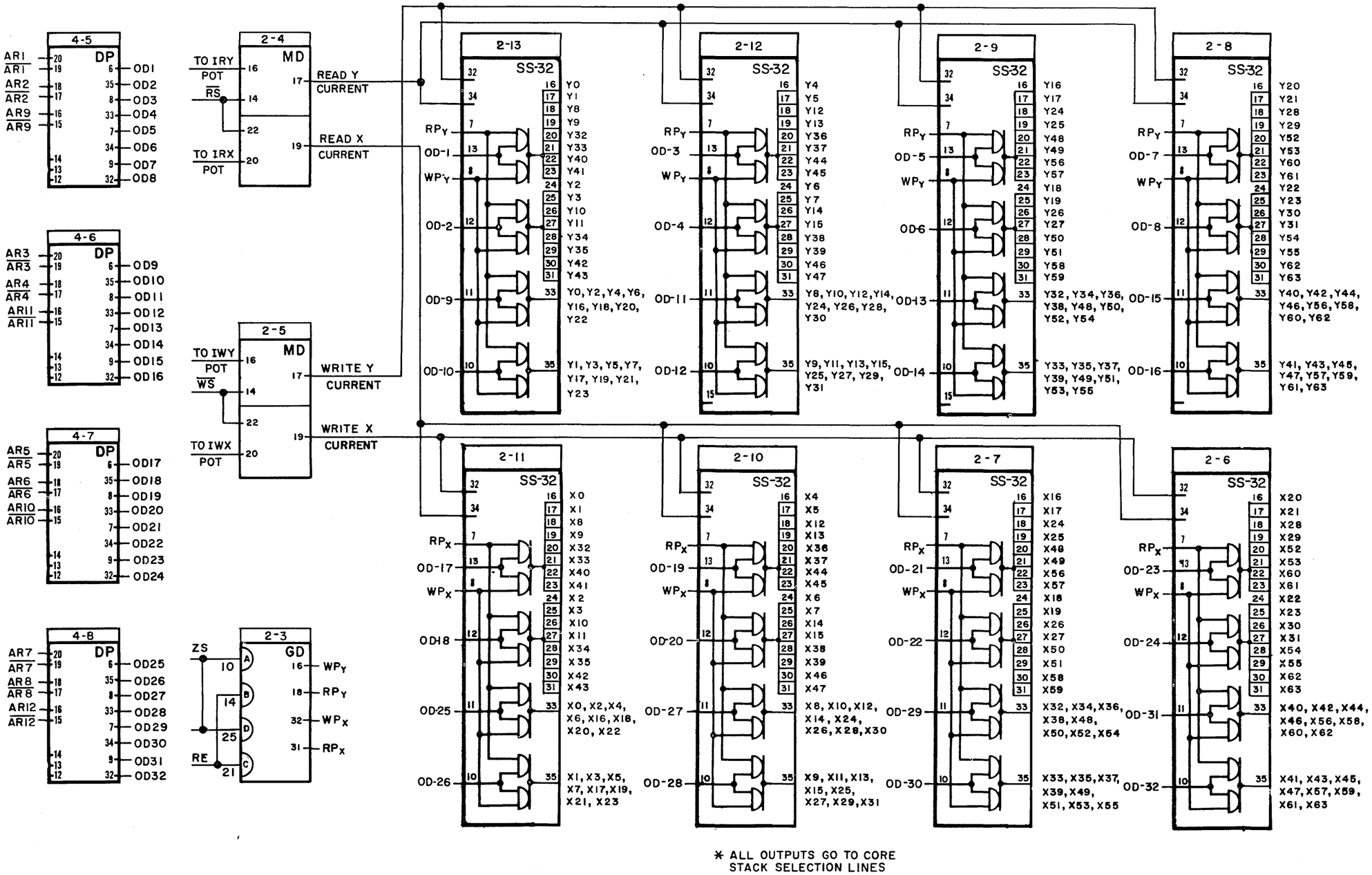
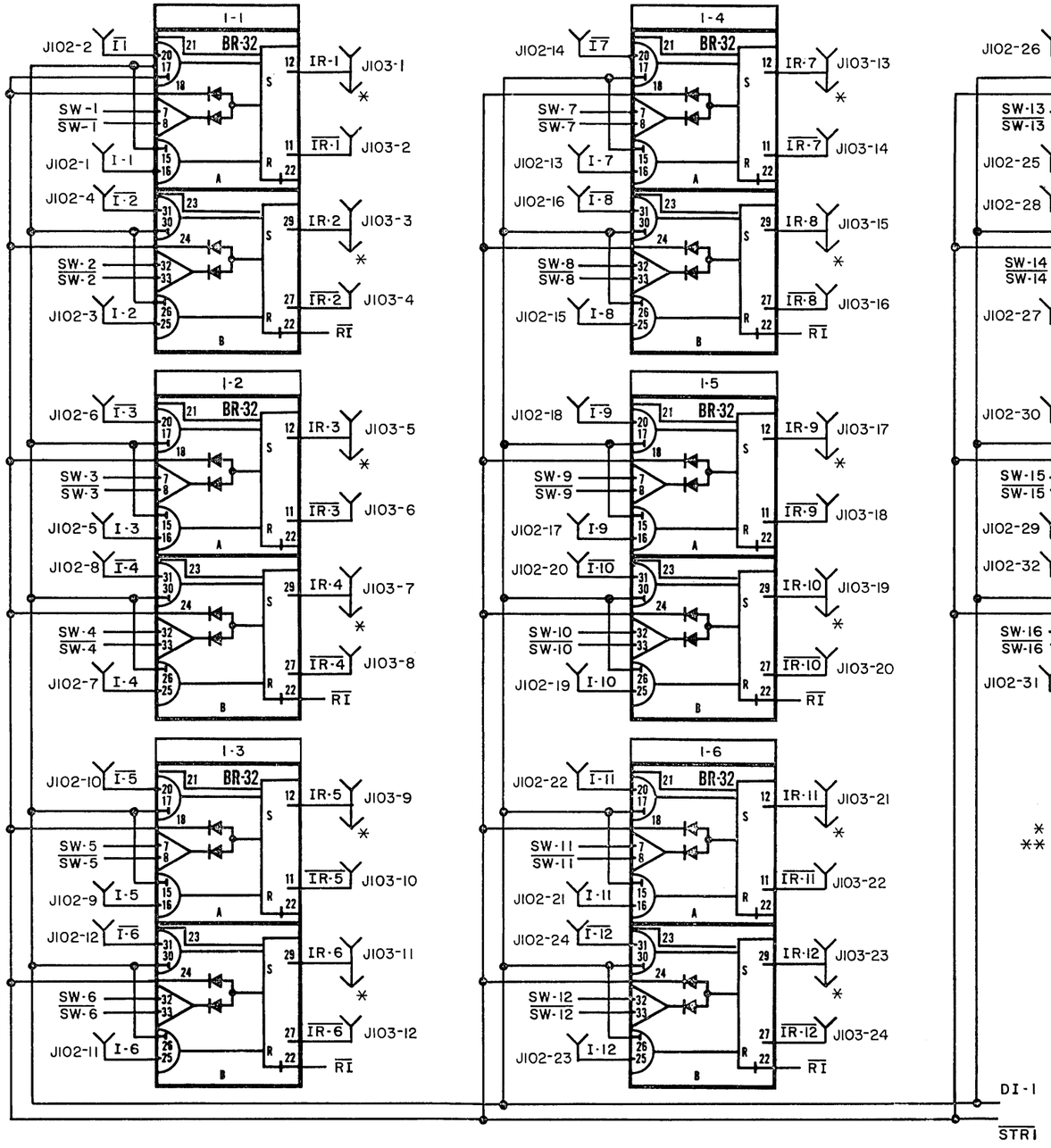


Figure 4-3. Address Register, Logic Diagram (Sequential-Interlace Addressing Option)



* ALL OUTPUTS GO TO CORE STACK SELECTION LINES

Figure 4-4. X-Y Decoders and Selection Switches, Logic Diagram



* TO MI-32 PAC'S
** TO CORE STACK VIA INHIBIT BOARD

71-166

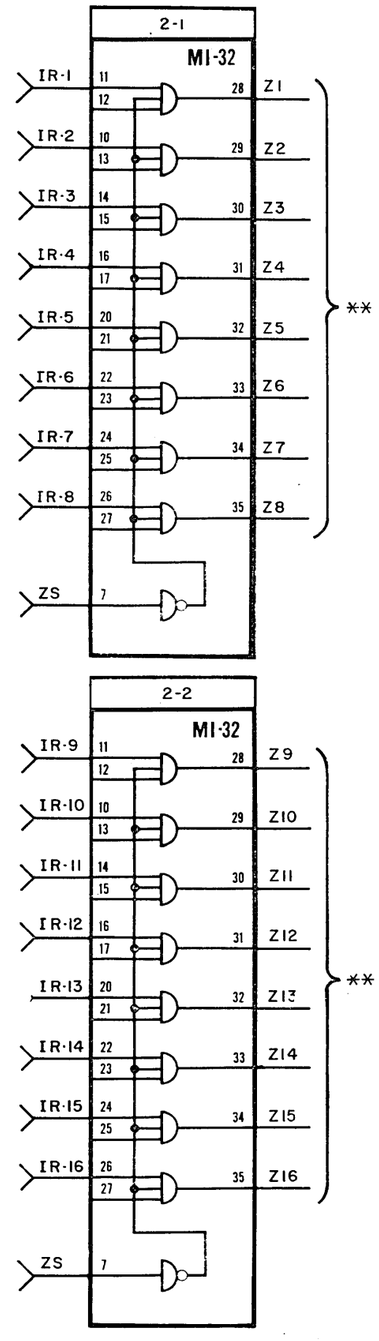
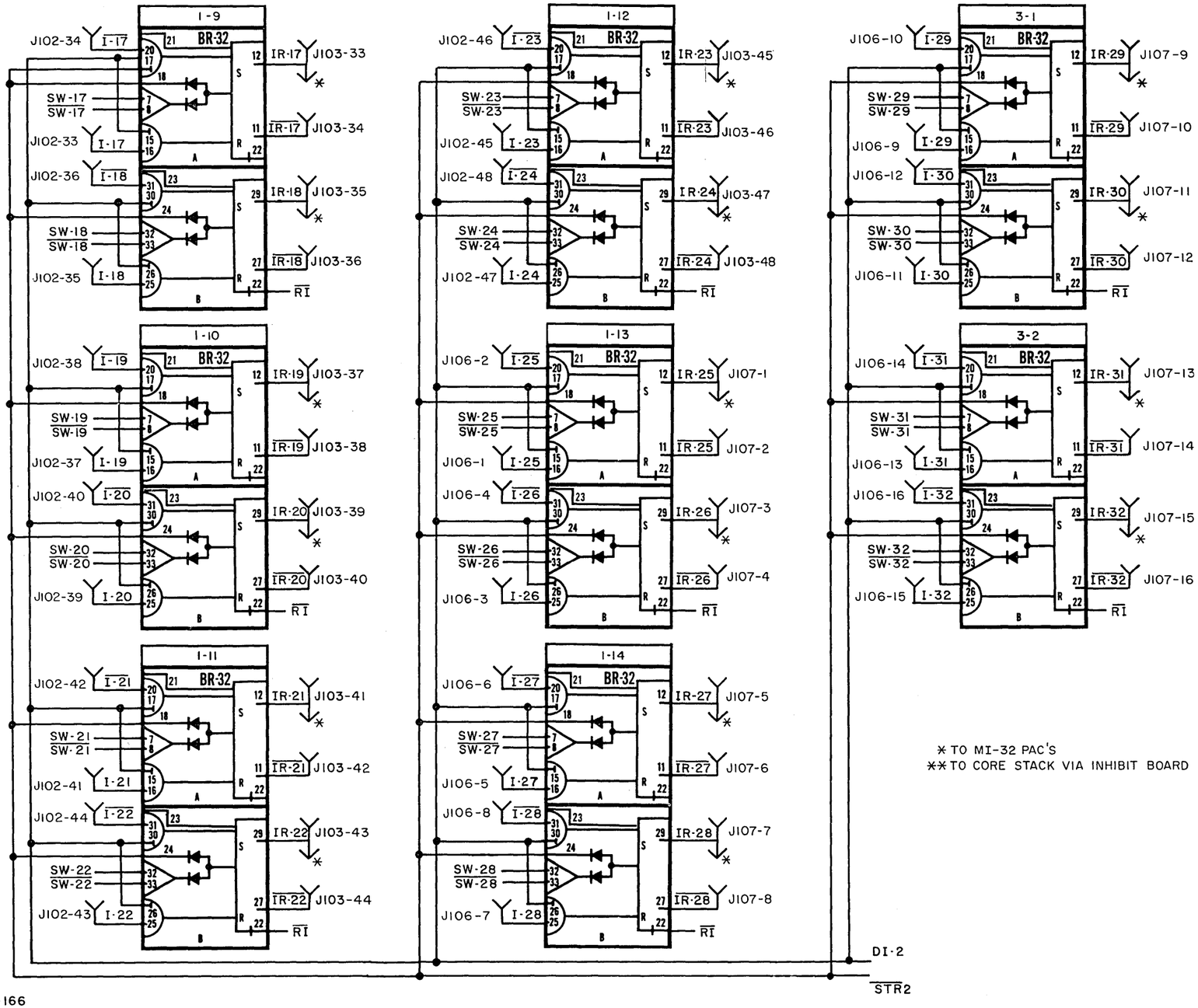


Figure 4-5. Information Register, Sense Amplifiers, and Inhibit Drivers, Logic Diagram (Bits 1 through 16)



* TO MI-32 PAC'S
** TO CORE STACK VIA INHIBIT BOARD

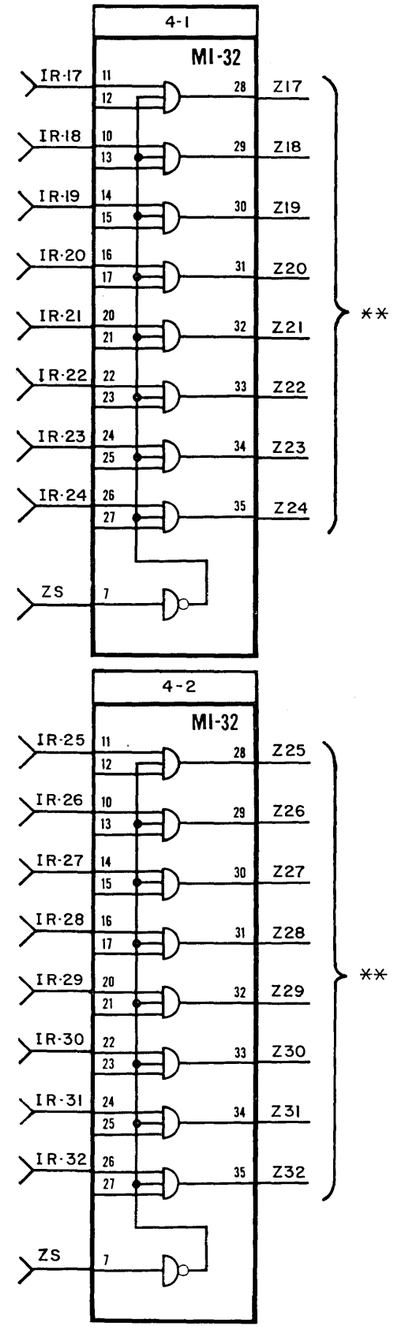
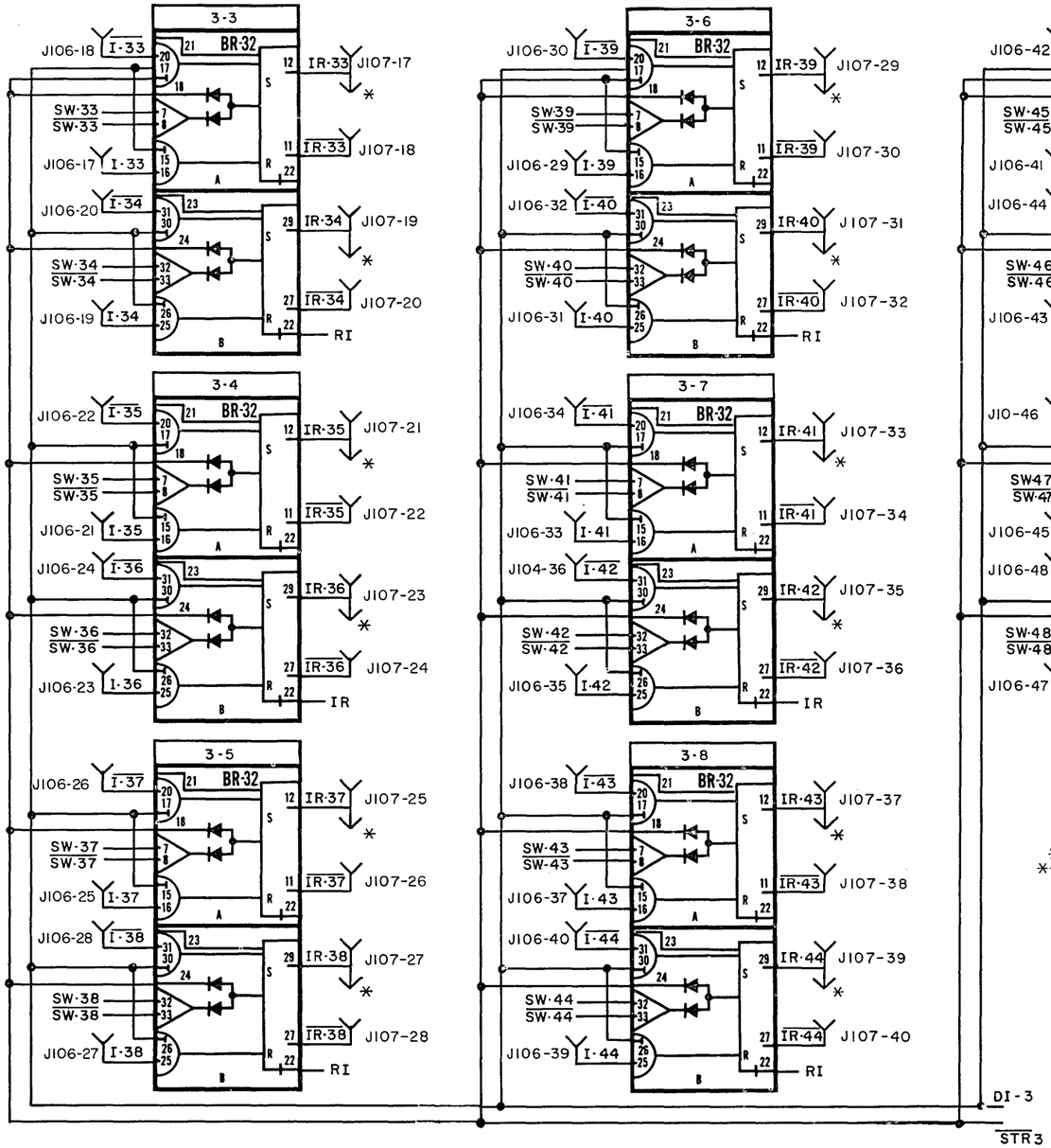


Figure 4-6. Information Register, Sense Amplifiers, and Inhibit Drivers, Logic Diagram (Bits 17 through 32)



* TO MI-32 PAC'S
** TO CORE STACK VIA INHIBIT BOARD

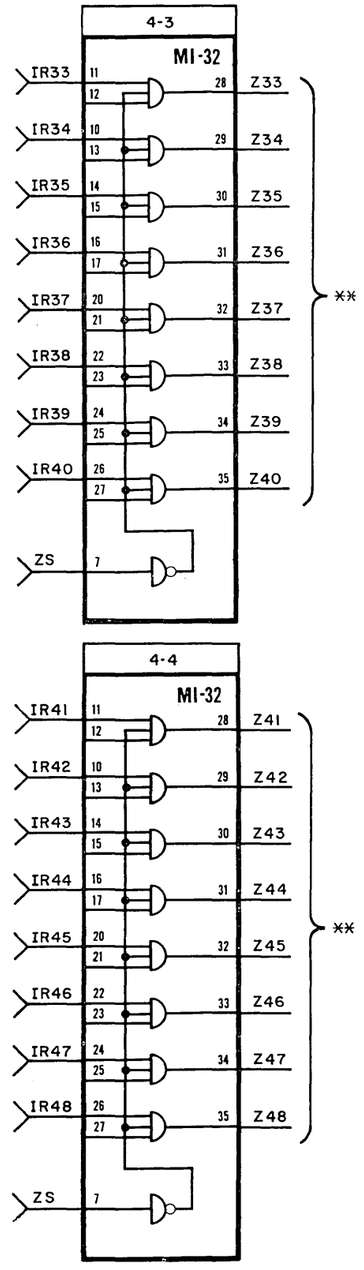
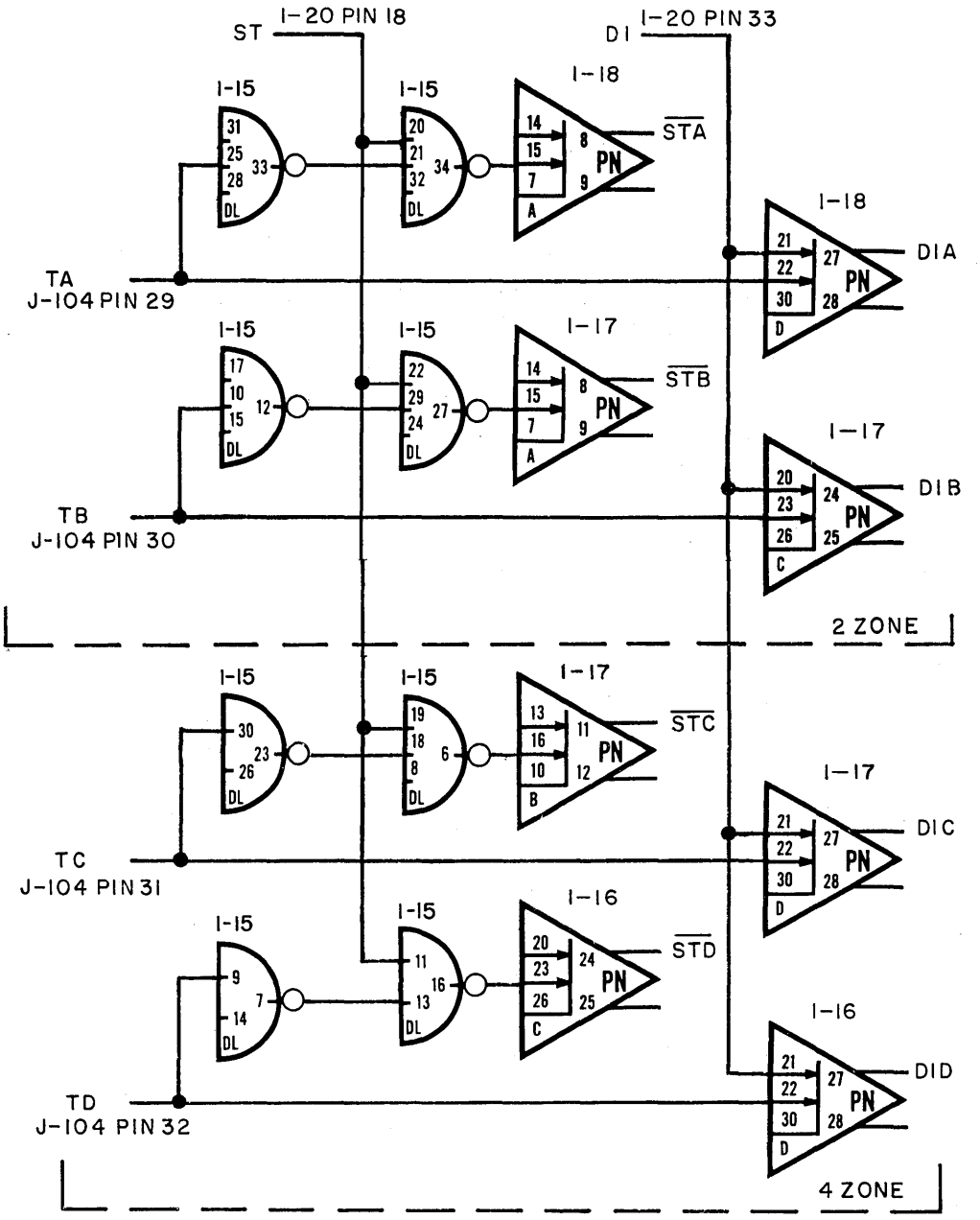


Figure 4-7. Information Register, Sense Amplifiers, and Inhibit Drivers, Logic Diagram (Bits 33 through 48)

71-166



INPUTS T(A,B,C,OR D)

0V FOR READ/RESTORE
-6V FOR CLEAR/WRITE
CLEAR/WRITE PULSE WILL START EITHER CYCLE

Figure 4-8. Partial Substitution Option, Logic Diagram (Two-Zone, Three-Zone, or Four-Zone Information-Register Partitioning)

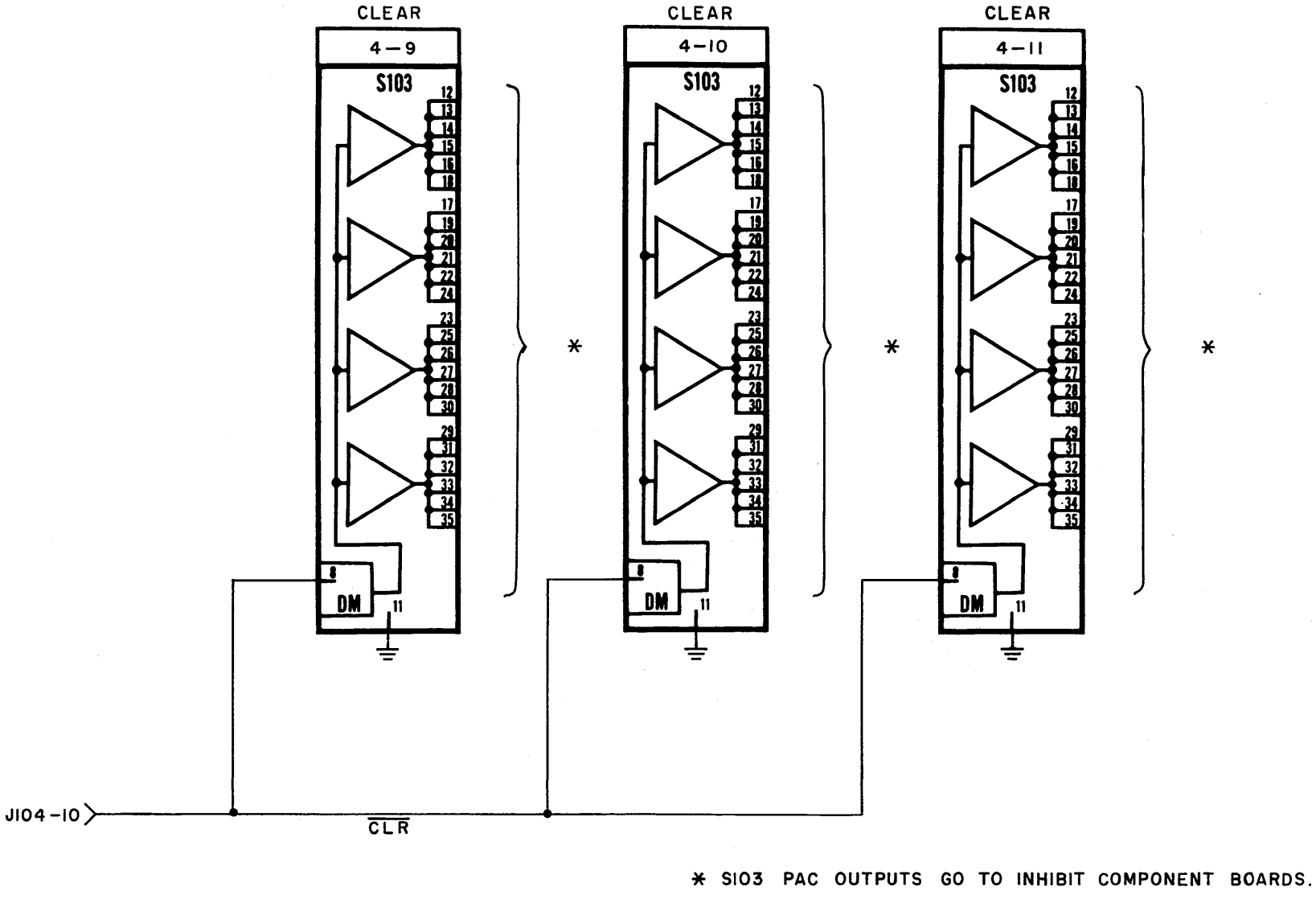


Figure 4-9. Clear Option, Logic Diagram

SECTION V
MAINTENANCE

5-1 GENERAL

This section of the manual contains information on the maintenance of the TCM-32 system. Data is included on the preventive maintenance, corrective maintenance, service, and repair for the Model TCM-32 Magnetic Core Memory. Detailed PAC descriptions are included in the appendix of this manual.

5-2 TEST EQUIPMENT

Table 5-1 lists the test equipment required to properly service the memory system.

TABLE 5-1.
TEST EQUIPMENT REQUIRED

Oscilloscope	Tektronix, Inc., Type 545A, or equivalent
Dual Trace Preamplifier	Tektronix, Inc., Type CA, or equivalent
Multimeter	Simpson, Type 260, or equivalent
Extender Card with Current Probe Leads	3C PAC, Model XP-30
AC Current Probe	Tektronix P6016 probe and passive termination (or Type 131 amplifier), or equivalent

5-3 PAC LOCATIONS

The PAC locations in each BLOC of the TCM-32 system are shown in Figure 3-1.

5-4 PAC HANDLING AND REPAIR PROCEDURES

5-4.1 Inserting and Removing System PACs

a. Never remove or insert printed circuit cards without turning off the DC power to the unit. Failure to turn off the power may result in damage to the PAC.

b. S-PAC insertion is accomplished by engaging the S-PAC in the appropriate slot of the S-BLOC and pressing the S-PAC into position until the connector engages and sets. The S-PAC is inserted with components on the left.

c. S-PAC removal in S-BLOCs is accomplished by engaging the two holes at the handle end of the S-PAC with the S-PAC extractor tool. A 20-lb force is sufficient to disengage any S-PAC from its mating connector. The S-PAC can then be removed with the fingers. The tool should be engaged from the component side of the S-PAC to ensure against possible damage to the etched wiring.

d. A hold-down bar is provided which clamps the S-PACs in place in the S-BLOC. The bar is equipped with a quick release thumb latch and bears against the S-PACs with a sponge rubber pad.

e. Polarization of the connectors is accomplished by inserting two nylon pegs in the appropriate slots of the connector. This prevents any but the desired S-PAC type from being inserted in that slot.

5-4.2 PAC Troubleshooting

The Extender PAC, Model XP-30, can be used to gain access to points on the PACs. Signals on the pins of the PACs may be ascertained from the PAC descriptions. The actual PAC signals can be compared with the waveforms shown in Figure 5-2. Leads for observing current waveforms with an AC current probe are provided on special Extender PACs.

5-4.3 Component Checking

a. General. Many PACs have several identical channels. In most cases components can be checked by resistance comparision with parts on other channels or other PACs.

b. Transistor checking. Transistors on a PAC can be checked with an ohmmeter. This should be done carefully to avoid damaging the transistors by large meter currents. Check the base-emitter and collector-emitter junctions in both directions, by using the meter scale which will apply the least amount of current to the transistor and still provide a reading. Replace any transistors that have open or shorted junctions, or whose resistance readings differ considerably from those obtained from a transistor on an identical channel or PAC.

c. Diode checking. Check diodes by comparing their forward and back resistances with diodes of the same type on other channels or PACs.

d. Resistor and Capacitors. Using an ohmmeter in the conventional manner, free one end of the component and check its resistance. To check most small capacitors for opens, a vacuum-tube ohmmeter will be needed to induce a needle "kick".

5-4.4 Component Replacement

a. Use only top quality rosin-core 60/40 solder (60% tin, 40% lead).

b. A small hot soldering iron should be used. A heat sink in the form of a pair of pliers or an alligator clip on the lead of the component is recommended to conduct heat away from the body of the component while soldering.

c. Remove excess solder from the etched side of the printed circuit board. A piece of spaghetti, large in diameter, can be used for blowing excess solder out of eyelets.

d. Insert leads of the new component into and through the drilled hole or eyelet, clip off excessive wire, and solder from the etched circuit side of the PAC.

e. Examine the PAC carefully for excess solder. Remove rosin deposits with a commercial cleaning solvent. Wipe the PAC clean with a dry lint-free cloth.

f. Recommended replacement parts for PAC components are shown in the PAC parts list in Appendix A.

5-5 SPARE PARTS

Table 5-2 lists the PACs suggested as spare parts for maintenance and as aids in troubleshooting.

TABLE 5-2.
SPARE PARTS LIST

PAC Designation	Model	Number Required Per System	Spares*
Selection Switch PAC	SS-32	4-8	2
Dynamic Current Driver PAC	MD-32	2	1
Bit Register PAC	BR-32	4-24	2
Inhibit Driver PAC	MI-32	1-6	
Gate Driver PAC	GD-32	1	1
Address Decoder PAC	DP-32	4	1
Memory Normalizer Board	MN	1	1
Inhibit Component Board	IB	1-4	1
Gate PAC	DN-30	1	1
NAND PAC	DI-30	1	1
NAND PAC	DL-30	1	1
Multi-Purpose Flip-Flop PAC	MF-30	3-7	1
Non-Inverting Power Amplifier PAC	PN-30	2-4	1
Memory Clear Driver PAC	CL-32	0-3	1
Timing Distributor PAC	TD-32	2	1

*Suggested number of spares (if PAC is used in customers system)

5-6 MAINTENANCE INSPECTION

Conduct a visual inspection periodically. In conducting this inspection, watch specifically for accumulations of dust and dirt, improperly seated PACs, and damaged or improperly dressed cable and signal leads. Check to see that all connectors are securely mated.

5-7 PREVENTIVE MAINTENANCE PROCEDURE

a. The TCM-32 system is extensively tested at Computer Control Company, Inc. prior to shipment. All planes are tested simultaneously under all ZEROs, all ONEs, and worst pattern conditions. The inhibit and drive line currents are set so that optimum operating margins result. The memory should be tested periodically as a preventive maintenance procedure using a memory test program or an optionally supplied Computer Control Company memory exerciser.

b. Voltage Adjustments. The three power supply voltages are factory preset to their nominal values. A screwdriver adjustment of ±2% is provided if recalibration is necessary. The power supply should be mounted physically near the TCM-32 system to minimize voltage drops and noise due to long lead lengths.

c. Drive Current Adjustments. The drive current amplitudes are adjusted by means of the four potentiometers. The adjustment procedure is as follows.

(1) Turn off the DC power and remove the Dynamic Current Driver PAC, Model MD-32

(2) Put the MD-32 PAC on a special extender PAC. Clip a calibrated AC current probe around the pin 17 lead. Turn on the DC power and adjust the current to 210 ma using the associated potentiometer (connected to pin 16 of the MD-32 PAC).

(3) Clip the current probe around pin 19 of the MD-32 PAC and adjust the current pulse amplitude to 210 ma.

(4) Repeat steps 1 through 3 for the other MD-32 PAC.

(5) The current amplitude of 210 ma is the nominal drive current at 25°C which gives best operating margins, unless noted elsewhere. This current can vary typically ±10% under most pattern testing without error. The current is temperature compensated by a Thermistor-Zener diode network on the MD-32 PAC. The current varies nominally -0.5%/°C to match the temperature characteristics of the magnetic cores used.

(6) The drive line current amplitude is nominally 40 ma higher than the current out of the MD-32 PAC due to the base current of the emitter-follower circuit on the Selection Switch PAC (Model SS-32). The drive line

current amplitude observed by a current probe at the output of the Selection Switch PAC is thus nominally 250 ma.

d. Inhibit Current Adjustment. The inhibit current is determined by the -18-volt supply and two precision resistors and does not require amplitude adjustment. The value of the inhibit current is nominally 210 ma, and may be varied typically ±15% under worst-pattern testing without causing errors. The amplitude may be checked by putting the MI-32 PAC on a special extender card and attaching a calibrated current probe to the appropriate output lead.

e. Strobe Adjustment. The most critical adjustment in a core memory is the timing of the sense amplifier strobe. Strobe is that signal which samples the sense winding voltage in order to discriminate between noise and signal. If strobe occurs too early, relative to the sense winding signal, it may give erroneous sense amplifier outputs as a result of sampling ZERO noise. If strobe is too late, it may attempt to sample the proper ONE signal after the signal amplitude has decreased to a value too low.

With reference to Figure 5-1, the upper trace shows proper strobe timing, and the lower trace shows a strobe timing too late. Proper strobe timing is such that the strobe-enabled signal occurs superimposed upon a pedestal which is due to the amplified core signal. If there is no pedestal ahead of the strobe pulse, strobe is too early.

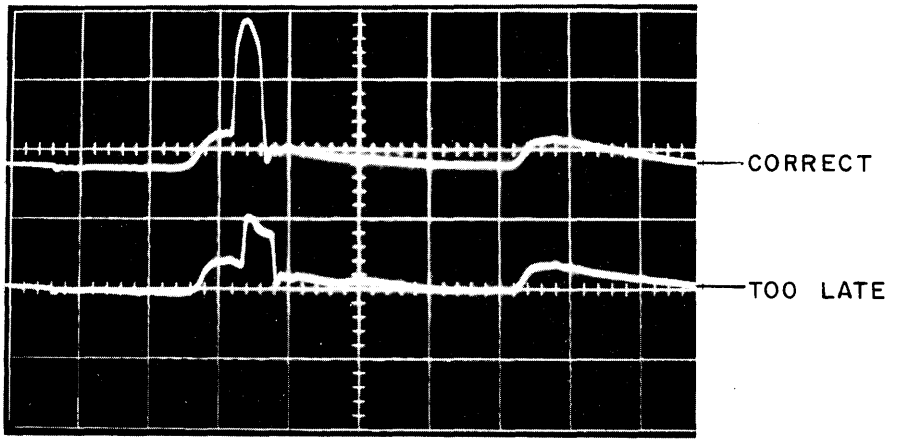


Figure 5-1. Strobe Adjustment Waveform

This waveform is observed at TP1 test point of any BR-32 which is sensing a ONE signal; this test point is the outermost one on the BR-32 adjacent to the handle, and may be probed with a Tektronix scope probe without removing the PAC.

Rarely should it be necessary to adjust strobe timing; an apparent shift in timing may be due to a maladjusted drive current in the memory. If it becomes necessary to change the strobe timing, this is done on the TD-32 board by moving jumpers. Refer to the TD-32 PAC write-up for this operation.

5-8 CORRECTIVE MAINTENANCE PROCEDURE

Corrective maintenance procedures consist of electrical and mechanical inspection, power supply troubleshooting procedures, and memory system troubleshooting procedures.

a. Corrective Maintenance Inspection. Before beginning troubleshooting procedures, a thorough inspection of the system should be performed. Check to see that the system is not physically damaged and that no wires have been torn accidentally from the equipment. Make sure electrical connectors and PACs fit firmly in their sockets.

b. Power Supply Troubleshooting Procedures. Lamps indicating AC and DC power-on are provided on the power supply. The DC outputs are protected by fast acting circuit breakers, and an indicator is provided to indicate DC power failure.

c. Memory Troubleshooting Procedures. Memory troubleshooting consists of determining the type of faulty memory operation, predicting the type of PAC at fault, and locating the particular faulty circuit. Test procedures to aid in troubleshooting are listed below.

(1) The normal waveforms at various test points and PAC connector pins are shown in Figure 5-2. A time scale of 0.5 μsec/cm is used throughout with 5 V/cm for voltages and 0.2 amp/cm for currents. An extender PAC should be used when checking the operating voltage and current waveforms at the PAC connectors. Oscilloscope probes should be used carefully because shorting of connector terminals or test points may damage the PAC.

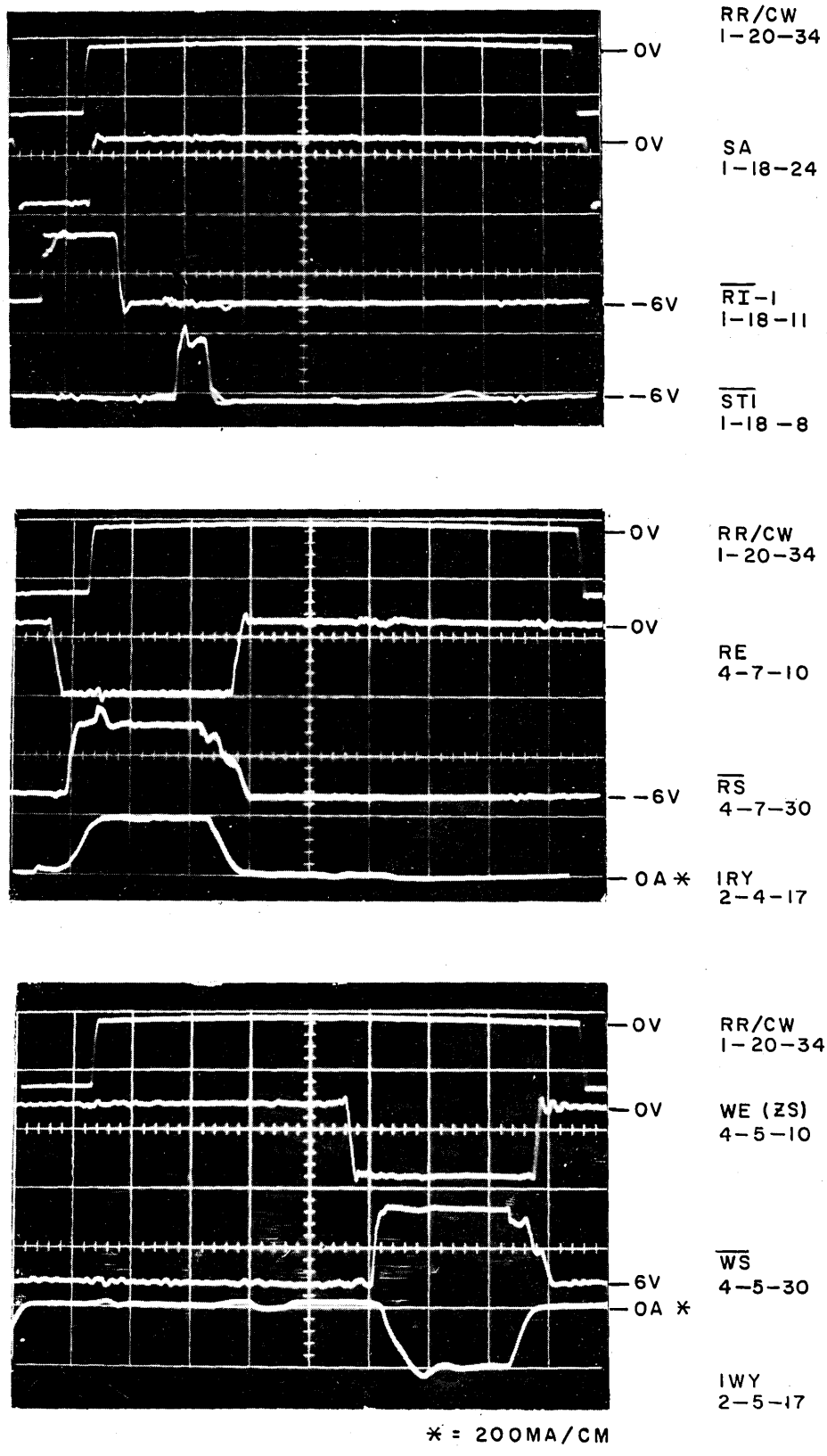


Figure 5-2. Waveforms (Sheet 1 of 3)

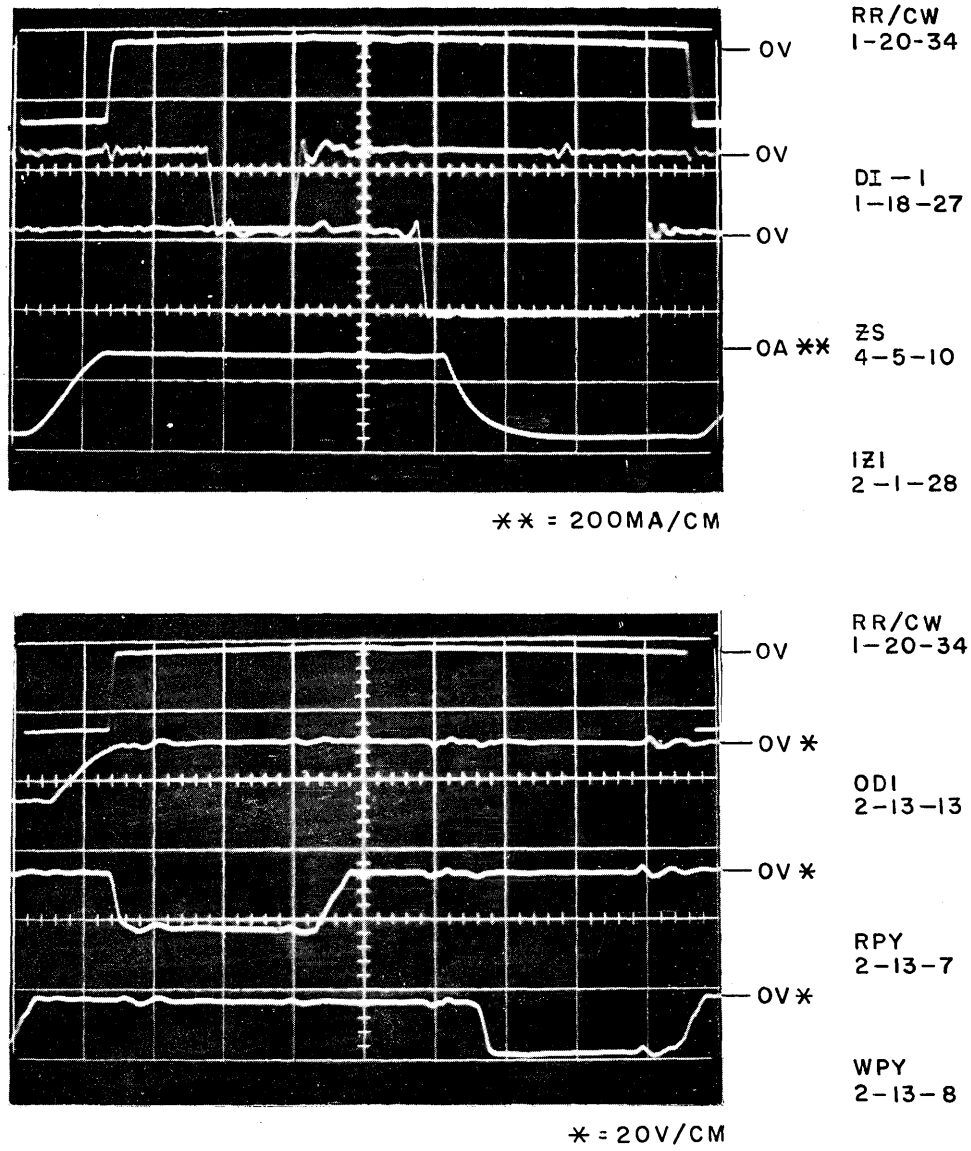


Figure 5-2. Waveforms (Sheet 2 of 3)

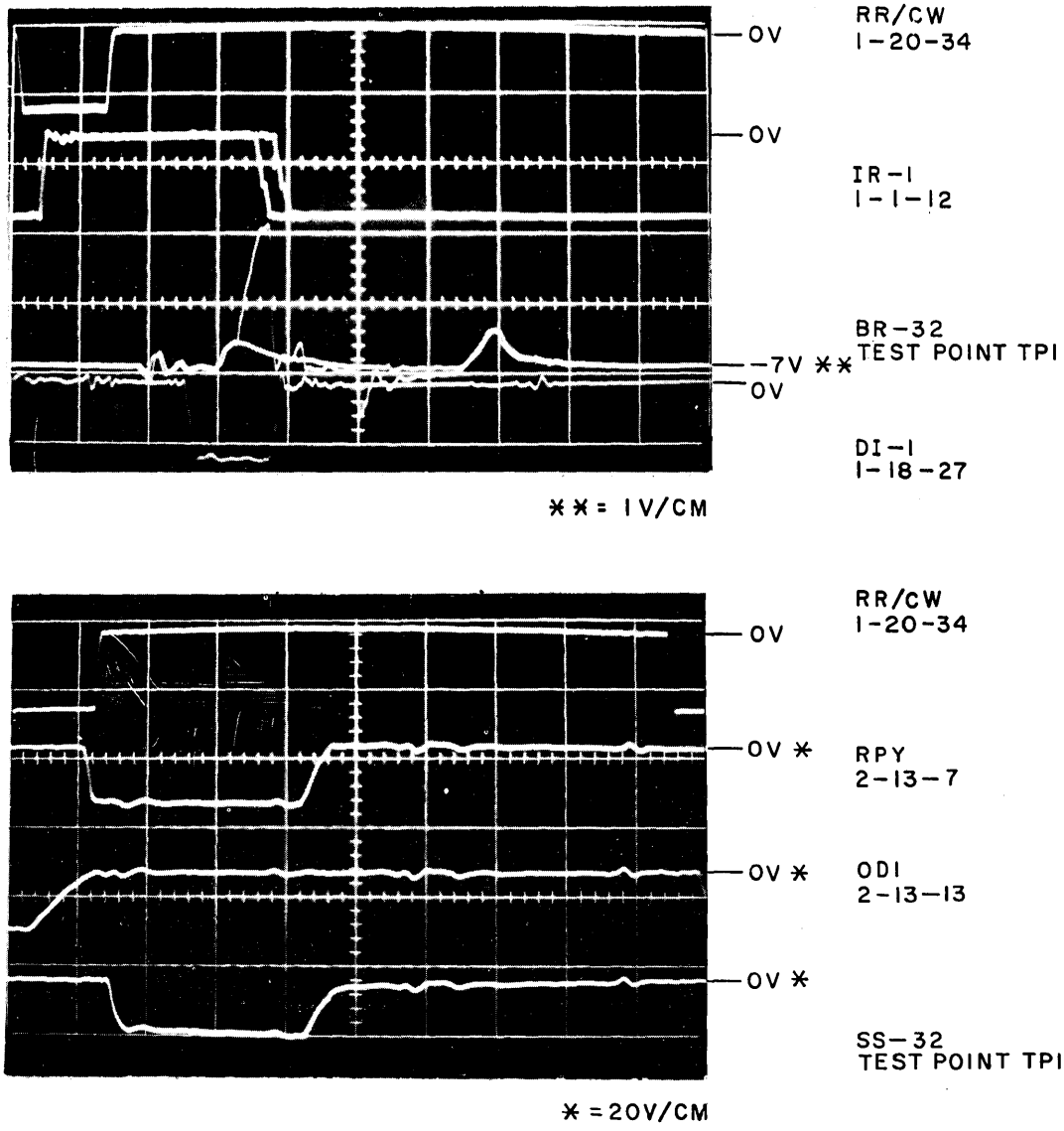


Figure 5-2. Waveforms (Sheet 3 of 3)

(2) Spare PACs may be used to isolate faulty circuits, in some cases, by interchanging identical PACs and noting any shift in the faulty bits or addresses.

(3) Refer to the PAC schematic and assembly drawings in Section 6 to isolate and replace the defective components on the printed circuit card.

(4) Memory failures are generally of the following types: operation failures, which are caused by faulty timing and control circuits; partial information word failures, which are caused by faulty bit register circuits (sense amplifier and information register flip-flop); and address failures which are caused by faulty address register decoding or selection circuits.

(5) Memory failures may be localized by the following procedure.

(a) Load the test pattern into the memory.

(b) Initiate a read operation at each address sequentially and check each readout information word.

(c) Check the readout information words for the following failures.

1. Operation failures. No apparent response to commands applied to the memory, or faulty operation at all addresses (see Table 5-3).
2. Partial information word failures. Failures of one bit or a series of two or more adjacent bits at all addresses (see Table 5-4).
3. Address failures. Faulty memory operation at particular addresses only (see Table 5-5).

5-9 MAGNETIC CORE MATRIX MAINTENANCE

Troubles occuring within the magnetic core matrices are unlikely under normal operating conditions. However, continuity measurements of the inhibit, sense, and drive windings will enable maintenance personnel to check the wiring of the core stack. The stack measurements should be done carefully to avoid damaging the matrix windings.

a. Inhibit Windings (Table 5-6)

(1) Turn off memory power. Remove the MI-32 Inhibit Driver PAC associated with the inhibit winding to be checked.

TABLE 5-3.
OPERATION FAILURES

Trouble	Probable Cause	Remedy
		Check Waveforms (At pin indicated)
No apparent response to memory commands (or faulty operation) at all addresses	Faulty input circuit	1-19, 1-22, 1-23 1-20
	Faulty Timing Distributor PAC	
	Faulty read, write gates	4-5, 4-7
	Faulty Gate Driver PAC	2-3-16, 18, 31, 32
	Faulty Dynamic Current Driver PAC	2-3-17, 19 2-4-17, 19
Readout information is all ZEROs or all ONEs at all addresses	Faulty inhibit step	4-5-10
	Faulty Gate Driver PAC	2-3-16, 18, 31, 32
	Faulty Dynamic Current Driver PAC	2-3-17, 19 2-4-17, 19
	Faulty Strobe Amplifier PAC	1-18-8 (1-16 bits) 1-17-8 (17-32 bits) 1-17-11 (33-48 bits)

(2) Place one ohmmeter lead on -18-volt output (pin 2 of the S-BLOC or at the inhibit component board).

(3) Place the other ohmmeter lead on the output connector pin of the inhibit driver channel in question, as shown on the logic block diagram. For example, to check the bit 4 inhibit winding, place the ohmmeter leads on connector pin 31 of the MI-32 connector.

(4) The inhibit winding resistance is a function of the word length. It will vary from 0.5 to 15 ohms for 128 to 4096 word memories. The resistance from the inhibit driver connector pin to the -18-volt supply includes the resistors on the inhibit component board. The total resistance, including the inhibit resistors and the inhibit line resistance, should read between 70 and 100 ohms, with a typical value of 83 ohms. The resistance readings of all bits should agree within ±10%.

b. Sense Windings (Table 5-7)

(1) Turn off memory power. Remove the BR-32 Bit Register PAC associated with the sense winding to be checked.

(2) Place the ohmmeter leads across the sense wire input terminations at the Bit Register PAC connector. (Refer to Table 5-8 for intra-unit wiring.) For example, to check the continuity of the bit 4 sense winding, place the ohmmeter leads on connector pins 32 and 33 of the BR-32 connector in location 1-2.

(3) Resistance readings should be between 1 and 20 ohms for memory planes of 128 to 4096 words. The resistance readings for all bits should agree within ±10%.

c. Drive Windings

(1) Turn off memory power. Remove the Selection Switch PAC, Model SS-32, from the PAC connectors associated with the X or Y drive line to be checked.

(2) Place one ohmmeter probe on the appropriate single drive line output of the Selection Switch PAC.

(3) Place the other ohmmeter probe on the other end of the drive line, at the appropriate bussed drive line output of the selction PAC. For example, to check continuity of the X5 drive line in a 2048 or 4096 word memory, place the ohmmeter leads on pins 2-10-17 and 2-11-35.

(4) Drive line resistance is a function of memory size (length of word and number of bits). Readings will vary from 1 ohm for small memories to approximately 15 ohms for large memories up to 4096/48. All the resistance readings in a given coordinate should agree within ±10%. The drive line resistance for the X- and Y-coordinates should agree within ±10% for square matrices (i. e., 64 x 64) but will be different for non-square planes (i. e., 32 x 64).

d. X-Windings (See Table 5-9)

(1) Place the ohmmeter leads at the appropriate SS-32 selection switch output indicated in the X-winding checklist.

(2) A normal reading is approximately 2 to 12 ohms. All readings should agree within ±10%.

e. Y-Windings (See Table 5-10)

(1) Place the ohmmeter leads at the appropriate SS-32 selection switch output indicated in the Y-winding checklist.

(2) A normal reading is approximately 2 to 12 ohms. All readings should agree within ±10%.

5-10 LOGIC CIRCUIT MAINTENANCE

Replacing malfunctioning packages is the quickest procedure for logic circuit maintenance and is highly recommended. Troubleshooting to the package level is best accomplished with a thorough understanding of the Principles of Operation, Section III. Some aids for troubleshooting the logic circuits are listed below.

Aid	Location
(a) System Block Diagram	Section III
(b) Logic Diagrams	Section IV
(c) Timing Diagram	Section III
(d) Maintenance	Section V
(e) Circuit Schematics	Appendix A
(f) Special PAC Information	Appendix
(g) Instruction Manual, S-PAC Digital Modules	Supplementary Publication

Suspected faulty packages can be repaired by referring to the appropriate PAC circuit description, schematic diagram, and assembly drawing, isolating the faulty component or components, and repairing the PAC by making replacements with the recommended parts.

5-11 DC POWER DISTRIBUTION

The memory power supply receives AC power and supplies the following DC system power, distributed as indicated below.

-18 V: To all PACs, to inhibit component boards.

-6 V: To all PACs.

+12 V: To all PACs.

TABLE 5-4.
PARTIAL INFORMATION WORD FAILURES

Trouble	Probable Cause	Remedy
		Check Waveforms (At pin indicated)
Failure of one bit (ZERO or ONE) at all addresses	Faulty Bit Register PAC stage	See Logic Diagram (Figures 4-5, 4-6, 4-7) for Pin Number (Function of word length)
	Faulty Inhibit Driver PAC channel	2-1 (1-8 bits) 2-2 (9-16 bits) 4-1 (17-24 bits) 4-2 (25-32 bits) 4-3 (33-40 bits) 4-4 (41-48 bits)
One bit is a ZERO at all addresses	Faulty Bit Register PAC stage	See Logic Diagram (Figures 4-5, 4-6, 4-7) for Pin Number (Function of word length)
	Shorted sense winding	(See Table 4-7)
	Faulty Inhibit Driver PAC channel	2-1 (1-8 bits) 2-2 (9-16 bits) 4-1 (17-24 bits) 4-2 (25-32 bits) 4-3 (33-40 bits) 4-4 (41-48 bits)
One bit is a ONE at all addresses	Open inhibit winding Shorted inhibit winding	(See Table 4-6)
	Faulty inhibit Driver PAC channel	2-1 (1-8 bits) 2-2 (9-16 bits) 4-1 (17-24 bits) 4-2 (25-32 bits) 4-3 (33-40 bits) 4-4 (41-48 bits)
	Faulty Bit Register PAC stage	See Logic Diagram (Figures 4-5, 4-6, 4-7) for Pin Number (Function of word length)
	Open sense winding	(See Table 4-7)

TABLE 5-4. (Cont)
PARTIAL INFORMATION WORD FAILURES

Trouble	Probable Cause	Remedy
		Check Waveforms (At pin indicated)
Failure of eight adjacent bits (ZERO or ONE) at all addresses	Faulty timing amplifier on Inhibit Driver PAC	2-1 (1-8 bits) 2-2 (9-16 bits) 4-1 (17-24 bits) 4-2 (25-32 bits) 4-3 (33-40 bits) 4-4 (41-48 bits)
Failure of up to 16 adjacent bits (ZERO or ONE) at all addresses	Faulty information Register drop-in power circuit	1-18-27 (1-16 bits) 1-17-24 (17-32 bits) 1-17-27 (33-48 bits)

TABLE 5-5.
ADDRESS, DECODING, AND SELECTION FAILURES

Trouble	Probable Cause	Remedy
		Check Waveforms (At pin indicated)
Faulty operation at 1/2 of memory capacity; normal drive voltage and current waveforms	Faulty address register flip-flop circuit	See Logic Diagram (Figures 4-2, 4-3) for Pin Number (Function of word capacity)
Faulty operation at particular addresses; incorrect drive voltage and/or current waveforms	Faulty Selection Switch PAC channel	See Logic Diagram (Figure 4-4) for Pin Number (Function of word capacity)
Read (or write) drive current missing in either the X- or Y-coordinate for all addresses	Bad channel on Gate Driver PAC	2-3-16, 18, 31, 32
	Bad channel on Dynamic Current Driver PAC	2-3-17, 19 2-4-17, 19
	Faulty read or write gates (No signal inputs to Gate Driver PAC or Dynamic Current Driver PAC)	4-5-30, 4-7-30
No drive current flow during read (or write) operation at particular addresses	Open current steering diode on Selection Switch PAC	See Logic Diagram (Figure 4-4) for Pin Number (Function of word capacity)
No drive current flow in either direction (read and write) at a number of addresses equal to the number of X- or Y-drive lines	Open drive line	(See Tables 4-9, 4-10)
	Faulty address decoder	4-5 through 4-8
Reduced drive current amplitude in one or both directions	Defective Dynamic Current Driver PAC	2-3 and 2-4
	Shorted current steering diode or transistor on Selection Switch PAC	See Logic Diagram (Figure 4-4) for Pin Number (Function of word capacity)

TABLE 5-6.
INHIBIT WINDING CHECKLIST
(Resistance measured between PAC terminal and -18-volt inhibit)

Memory Signal	Memory	Memory Signal	Memory
Z-1	2-1-28	Z-25	4-2-28
Z-2	2-1-29	Z-26	4-2-29
Z-3	2-1-30	Z-27	4-2-30
Z-4	2-1-31	Z-28	4-2-31
Z-5	2-1-32	Z-29	4-2-32
Z-6	2-1-33	Z-30	4-2-33
Z-7	2-1-34	Z-31	4-2-34
Z-8	2-1-35	Z-32	4-2-35
Z-9	2-2-28	Z-33	4-3-28
Z-10	2-2-29	Z-34	4-3-29
Z-11	2-2-30	Z-35	4-3-30
Z-12	2-2-31	Z-36	4-3-31
Z-13	2-2-32	Z-37	4-3-32
Z-14	2-2-33	Z-38	4-3-33
Z-15	2-2-34	Z-39	4-3-34
Z-16	2-2-35	Z-40	4-3-35
Z-17	4-1-28	Z-41	4-4-28
Z-18	4-1-29	Z-42	4-4-29
Z-19	4-1-30	Z-43	4-4-30
Z-20	4-1-31	Z-44	4-4-31
Z-21	4-1-32	Z-45	4-4-32
Z-22	4-1-33	Z-46	4-4-33
Z-23	4-1-34	Z-47	4-4-34
Z-24	4-1-35	Z-48	4-4-35

TABLE 5-7.
SENSE WINDING CHECKLIST
(Resistance measured across terminals A and B;
BR-32 PACs must be removed)

Memory Signal	Memory Test Point	Memory Signal	Memory Test Point
SW-1	1-1-7	SW-13	1-7-7
$\overline{\text{SW-1}}$	1-1-8	$\overline{\text{SW-13}}$	1-7-8
SW-2	1-1-32	SW-14	1-7-32
$\overline{\text{SW-2}}$	1-1-33	$\overline{\text{SW-14}}$	1-7-33
SW-3	1-2-7	SW-15	1-8-7
$\overline{\text{SW-3}}$	1-2-8	$\overline{\text{SW-15}}$	1-8-8
SW-4	1-2-32	SW-16	1-8-32
$\overline{\text{SW-4}}$	1-2-33	$\overline{\text{SW-16}}$	1-8-33
SW-5	1-3-7	SW-17	1-9-7
$\overline{\text{SW-5}}$	1-3-8	$\overline{\text{SW-17}}$	1-9-8
SW-6	1-3-32	SW-18	1-9-32
$\overline{\text{SW-6}}$	1-3-33	$\overline{\text{SW-18}}$	1-9-33
SW-7	1-4-7	SW-19	1-10-7
$\overline{\text{SW-7}}$	1-4-8	$\overline{\text{SW-19}}$	1-10-8
SW-8	1-4-32	SW-20	1-10-32
$\overline{\text{SW-8}}$	1-4-33	$\overline{\text{SW-20}}$	1-10-33
SW-9	1-5-7	SW-21	1-11-7
$\overline{\text{SW-9}}$	1-5-8	$\overline{\text{SW-21}}$	1-11-8
SW-10	1-5-32	SW-22	1-11-32
$\overline{\text{SW-10}}$	1-5-33	$\overline{\text{SW-22}}$	1-11-33
SW-11	1-6-7	SW-23	1-12-7
$\overline{\text{SW-11}}$	1-6-8	$\overline{\text{SW-23}}$	1-12-8
SW-12	1-6-32	SW-24	1-12-32
$\overline{\text{SW-12}}$	1-6-33	$\overline{\text{SW-24}}$	1-12-33

TABLE 5-7. (Cont)
SENSE WINDING CHECKLIST
(Resistance measured across terminals A and B;
BR-32 PACs must be removed)

Memory Signal	Memory Test Point	Memory Signal	Memory Test Point
SW-25	1-13-7	SW-37	3-5-7
$\overline{\text{SW-25}}$	1-13-8	$\overline{\text{SW-37}}$	3-5-8
SW-26	1-13-32	SW-38	3-5-32
$\overline{\text{SW-26}}$	1-13-33	$\overline{\text{SW-38}}$	3-5-33
SW-27	1-14-7	SW-39	3-6-7
$\overline{\text{SW-27}}$	1-14-8	$\overline{\text{SW-39}}$	3-6-8
SW-28	1-14-32	SW-40	3-6-32
$\overline{\text{SW-28}}$	1-14-33	$\overline{\text{SW-40}}$	3-6-33
SW-29	3-1-7	SW-41	3-7-7
$\overline{\text{SW-29}}$	3-1-8	$\overline{\text{SW-41}}$	3-7-8
SW-30	3-1-32	SW-42	3-7-32
$\overline{\text{SW-30}}$	3-1-33	$\overline{\text{SW-42}}$	3-7-33
SW-31	3-2-7	SW-43	3-8-7
$\overline{\text{SW-31}}$	3-2-8	$\overline{\text{SW-43}}$	3-8-8
SW-32	3-2-32	SW-44	3-8-32
$\overline{\text{SW-32}}$	3-2-33	$\overline{\text{SW-44}}$	3-8-33
SW-33	3-3-7	SW-45	3-9-7
$\overline{\text{SW-33}}$	3-3-8	$\overline{\text{SW-45}}$	3-9-8
SW-34	3-3-32	SW-46	3-9-32
$\overline{\text{SW-34}}$	3-3-33	$\overline{\text{SW-46}}$	3-9-33
SW-35	3-4-7	SW-47	3-10-7
$\overline{\text{SW-35}}$	3-4-8	$\overline{\text{SW-47}}$	3-10-8
SW-36	3-4-32	SW-48	3-10-32
$\overline{\text{SW-36}}$	3-4-33	$\overline{\text{SW-48}}$	3-10-33

TABLE 5-8.
INTRA-UNIT WIRING CONNECTOR J-110

Pin Number	Designation	Pin Number	Designation
1	SW-1	26	SW-13
2	$\overline{\text{SW-1}}$	27	$\overline{\text{SW-13}}$
3	SW-2	28	SW-14
4	$\overline{\text{SW-2}}$	29	$\overline{\text{SW-14}}$
5	SW-3	30	SW-15
6	$\overline{\text{SW-3}}$	31	$\overline{\text{SW-15}}$
7	SW-4	32	SW-16
8	$\overline{\text{SW-4}}$	33	$\overline{\text{SW-16}}$
9	SW-5	34	SW-17
10	$\overline{\text{SW-5}}$	35	$\overline{\text{SW-17}}$
11	SW-6	36	SW-18
12	$\overline{\text{SW-6}}$	37	$\overline{\text{SW-18}}$
13	SW-7	38	SW-19
14	$\overline{\text{SW-7}}$	39	$\overline{\text{SW-19}}$
15	SW-8	40	SW-20
16	$\overline{\text{SW-8}}$	41	$\overline{\text{SW-20}}$
17		42	SW-21
18	SW-9	43	$\overline{\text{SW-21}}$
19	$\overline{\text{SW-9}}$	44	SW-22
20	SW-10	45	$\overline{\text{SW-22}}$
21	$\overline{\text{SW-10}}$	46	SW-23
22	SW-11	47	$\overline{\text{SW-23}}$
23	$\overline{\text{SW-11}}$	48	SW-24
24	SW-12	49	$\overline{\text{SW-24}}$
25	$\overline{\text{SW-12}}$	50	

TABLE 5-8. (Cont)
INTRA-UNIT WIRING CONNECTOR J-111

Pin Number	Designation	Pin Number	Designation
1	$\overline{\text{AR-1}}$	26	Twisted Pair $\overline{\text{CL}}$
2	AR-1	27	Gnd
3	$\overline{\text{AR-2}}$	28	Twisted Pair Unload Counter
4	AR-2	29	Gnd
5	$\overline{\text{AR-3}}$	30	Half Cycle
6	AR-3	31	$\overline{\text{RAN}}$
7	$\overline{\text{AR-4}}$	32	ER
8	AR-4	33	$\overline{\text{RMW}}$
9	$\overline{\text{AR-5}}$	34	SA
10	AR-5	35	$\overline{\text{SR}}$
11	$\overline{\text{AR-6}}$	36	SA_2
12	AR-6	37	SA_3
13	$\overline{\text{AR-7}}$	38	
14	AR-7	39	$\overline{\text{LCT}}$
15	$\overline{\text{AR-8}}$	40	IA
16	AR-8	41	$\overline{\text{EE}}$
17		42	EC
18	$\overline{\text{AR-9}}$	43	$\overline{\text{MBS}}$
19	AR-9	44	$\overline{\text{SB}}$
20	$\overline{\text{AR-10}}$	45	RS
21	AR-10	46	$\overline{\text{ER}}$
22	$\overline{\text{AR-11}}$	47	$\overline{\text{SZ}}$
23	AR-11	48	WS
24	$\overline{\text{AR-12}}$	49	$\overline{\text{EZ}}$
25	AR-12	50	$\overline{\text{EB}}$

TABLE 5-8. (Cont)
INTRA-UNIT WIRING CONNECTOR J-112

Pin Number	Designation	Pin Number	Designation
1	IR-1	26	IR-26
2	IR-2	27	IR-27
3	IR-3	28	IR-28
4	IR-4	29	IR-29
5	IR-5	30	IR-30
6	IR-6	31	IR-31
7	IR-7	32	IR-32
8	IR-8	33	IR-33
9	IR-9	34	IR-34
10	IR-10	35	IR-35
11	IR-11	36	IR-36
12	IR-12	37	IR-37
13	IR-13	38	IR-38
14	IR-14	39	IR-39
15	IR-15	40	IR-40
16	IR-16	41	IR-41
17	IR-17	42	IR-42
18	IR-18	43	IR-43
19	IR-19	44	IR-44
20	IR-20	45	IR-45
21	IR-21	46	IR-46
22	IR-22	47	IR-47
23	IR-23	48	IR-48
24	IR-24	49	
25	IR-25	50	

TABLE 5-8. (Cont)
INTRA-UNIT WIRING CONNECTOR J-113

Pin Number	Designation	Pin Number	Designation
1	SW-25	26	SW-37
2	SW-25	27	SW-37
3	SW-26	28	SW-38
4	SW-26	29	SW-38
5	SW-27	30	SW-39
6	SW-27	31	SW-39
7	SW-28	32	SW-40
8	SW-28	33	SW-40
9	SW-29	34	SW-41
10	SW-29	35	SW-41
11	SW-30	36	SW-42
12	SW-30	37	SW-42
13	SW-31	38	SW-43
14	SW-31	39	SW-43
15	SW-32	40	SW-44
16	SW-32	41	SW-44
17		42	SW-45
18	SW-33	43	SW-45
19	SW-33	44	SW-46
20	SW-34	45	SW-46
21	SW-34	46	SW-47
22	SW-35	47	SW-47
23	SW-35	48	SW-48
24	SW-36	49	SW-48
25	SW-36	50	

TABLE 5-9.
X-WINDING CHECKLIST

X_k	Drive Line	X'_k	X_k	Drive Line	X'_k
2-11-16	0	2-11-33	2-11-20	32	2-7-33
2-11-17	1	2-11-35	2-11-21	33	2-7-35
2-11-24	2	2-11-33	2-11-28	34	2-7-33
2-11-25	3	2-11-35	2-11-29	35	2-7-35
2-10-16	4	2-11-33	2-10-20	36	2-7-33
2-10-17	5	2-11-35	2-10-21	37	2-7-35
2-10-24	6	2-11-33	2-10-28	38	2-7-33
2-10-25	7	2-11-35	2-10-29	39	2-7-35
2-11-18	8	2-10-33	2-11-22	40	2-6-33
2-11-19	9	2-10-35	2-11-23	41	2-6-35
2-11-26	10	2-10-33	2-11-30	42	2-6-33
2-11-27	11	2-10-35	2-11-31	43	2-6-35
2-10-18	12	2-10-33	2-10-22	44	2-6-33
2-10-19	13	2-10-35	2-10-23	45	2-6-35
2-10-26	14	2-10-33	2-10-30	46	2-6-33
2-10-27	15	2-10-35	2-10-31	47	2-6-35
2-7-16	16	2-11-33	2-7-20	48	2-7-33
2-7-17	17	2-11-35	2-7-21	49	2-7-35
2-7-24	18	2-11-33	2-7-28	50	2-7-33
2-7-25	19	2-11-35	2-7-29	51	2-7-35
2-6-16	20	2-11-33	2-6-20	52	2-7-33
2-6-17	21	2-11-35	2-6-21	53	2-7-35
2-6-24	22	2-11-33	2-6-28	54	2-7-33
2-6-25	23	2-11-35	2-6-29	55	2-7-35
2-7-18	24	2-10-33	2-7-22	56	2-6-33
2-7-19	25	2-10-35	2-7-23	57	2-6-35
2-7-26	26	2-10-33	2-7-30	58	2-6-33
2-7-27	27	2-10-35	2-7-31	59	2-6-35
2-6-18	28	2-10-33	2-6-22	60	2-6-33
2-6-19	29	2-10-35	2-6-23	61	2-6-35
2-6-26	30	2-10-33	2-6-30	62	2-6-33
2-6-27	31	2-10-35	2-6-31	63	2-6-35

TABLE 5-10.
Y-WINDING CHECKLIST

Y_k	Drive Line	Y'_k	Y_k	Drive Line	Y'_k
2-13-16	0	2-13-33	2-13-20	32	2-9-33
2-13-17	1	2-13-35	2-13-21	33	2-9-35
2-13-24	2	2-13-33	2-13-28	34	2-9-33
2-13-25	3	2-13-35	2-13-29	35	2-9-35
2-12-16	4	2-13-33	2-12-20	36	2-9-33
2-12-17	5	2-13-35	2-12-21	37	2-9-35
2-12-24	6	2-13-33	2-12-28	38	2-9-33
2-12-25	7	2-13-35	2-12-29	39	2-9-35
2-13-18	8	2-12-33	2-13-22	40	2-8-33
2-13-19	9	2-12-35	2-13-23	41	2-8-35
2-13-26	10	2-12-33	2-13-30	42	2-8-33
2-13-27	11	2-12-35	2-13-31	43	2-8-35
2-12-18	12	2-12-33	2-12-22	44	2-8-33
2-12-19	13	2-12-35	2-12-23	45	2-8-35
2-12-26	14	2-12-33	2-12-30	46	2-8-33
2-12-27	15	2-12-35	2-12-31	47	2-8-35
2-9-16	16	2-13-33	2-9-20	48	2-9-33
2-9-17	17	2-13-35	2-9-21	49	2-9-35
2-9-24	18	2-13-33	2-9-28	50	2-9-33
2-9-25	19	2-13-35	2-9-29	51	2-9-35
2-8-16	20	2-13-33	2-8-20	52	2-9-33
2-8-17	21	2-13-35	2-8-21	53	2-9-35
2-8-24	22	2-13-33	2-8-28	54	2-9-33
2-8-25	23	2-13-35	2-8-29	55	2-9-35
2-9-18	24	2-12-33	2-9-22	56	2-8-33
2-9-19	25	2-12-35	2-9-23	57	2-8-35
2-9-26	26	2-12-33	2-9-30	58	2-8-33
2-9-27	27	2-12-35	2-9-31	59	2-8-35
2-8-18	28	2-12-33	2-8-22	60	2-8-33
2-8-19	29	2-12-35	2-8-23	61	2-8-35
2-8-26	30	2-12-33	2-8-30	62	2-8-33
2-8-27	31	2-12-35	2-8-31	63	2-8-35

SECTION VI
PAC COMPLEMENT LIST

6-1 GENERAL

This section contains a Magnetic Core Memory System PAC complement list (Table 6-1).

Parts lists for special S-PACs (p/o units 1 and 2) used in this system are contained in the appendix of this manual. The parts lists for all standard S-PAC modules are contained in the Instruction Manual for 1 MC Series S-PAC Digital Modules.

TABLE 6-1.
PAC COMPLEMENT LIST

Temporary Designation	Designation	Description	Quantity
		STANDARD PACS	
		TCM-32 Assembly	1
	DL-30	NAND PAC	2
	DC-30	Diode PAC	1
	MF-30	Flip-Flop PAC	7
	PN-30	Non-Inverting Power Amplifier PAC	4
		NON-STANDARD PACS	
S-086	BR-32	Bit Register PAC	24
S-117	DP-32	Address Decoder PAC	4
S-091	GD-32	Gate Driver PAC	1
S-083	MD-32	Dynamic Current Driver PAC	2
S-087	MI-32	Inhibit Driver PAC	6
S-026	SS-32	Selection Switch PAC	8
S-219	TD-32	Timing Distributor PAC	2
S-103		Memory Clear Driver PAC	2
S-169		Transfer Gate PAC	5
S-179		Parallel Transfer Gate PAC	1

APPENDIX

The appendix to this manual contains circuit descriptions, schematic diagrams, and assembly drawings for the following digital modules and component boards used in the Magnetic Core Memory System. These modules are not covered in the Instruction Manual for S-PAC Digital Modules. They are arranged in this appendix in the following order.

Bit Register PAC, model BR-32
Address Decoder PAC, model DP-32
Gate Driver PAC, model GD-32
Dynamic Current Driver PAC, model MD-32
Inhibit Driver PAC, model MI-32
Selection Switch PAC, model SS-32
Timing Distributor PAC, model S-219
Inhibit Component Board
Memory Normalizer Board
Memory Clear Driver PAC, model S-103
Transfer Gate PAC, model S-169
Parallel Transfer Gate PAC, model S-179

BIT REGISTER PAC, MODEL BR-32

GENERAL DESCRIPTION

The Bit Register PAC, Model BR-32 (Figures 1 and 2), contains two sense amplifiers with associated information register flip-flops. The sense amplifiers provide amplitude discrimination, time discrimination, and a high ratio of common-mode noise rejection. The circuit amplifies the core signal appearing on the sense line. The amplified core signal is time-strobed to provide a digital form of output that sets a standard flip-flop circuit. Inputs to the information register flip-flops are provided for writing external information into the memory.

CIRCUIT DESCRIPTION

Transistors Q1 and Q2 (Figure 3) are on and their emitters are at approximately 0 volt, without a sense signal applied. The collectors of Q1 and Q2 are at a +6-volt potential and transistors Q3 and Q4 are off. The collectors of Q3 and Q4 are clamped at -6.3 volts by the strobe input and resistor network R11-R13. Transistor Q5 is reverse-biased, and its collector is clamped to +0.3 volt by resistor R16 and diode CR4. Transistor Q6 is normally off, with its collector clamped at -6.3 volts. The flip-flop is reset at the beginning of the memory cycle that places Q7 on and Q8 off.

The sense inputs are connected directly to the base of input transistors Q1 and Q2. Resistors R1 and R12 terminate the sense winding. Resistors R3, R6, and potentiometer R5 provide AC stabilization for the differential amplifier (Q1 and Q2). Resistor R8 is a DC stabilizing resistor, and resistors R4 and R7 increase the resolution of potentiometer R5. Common-mode noise is cancelled by the high impedance of resistor R8 and no differential signal appears at the collectors of Q1 and Q2. Transistors Q3 and Q4 remain off, giving the sense amplifier a high common-mode noise rejection ratio.

During the read cycle a ONE appears on the sense input. When the base of Q1 goes positive, its conduction increases and its collector voltage goes negative. The negative pulse on the base of Q2 causes its collector to go positive. The pulse clamps to the Q1 collector voltage through the emitter-base junction of Q3.

The potentiometer adjusts the DC gain and balance of transistors Q1 and Q2. Diodes CR1 and CR2 form an AND gate for positive signals. When the strobe input goes to 0 volt, and the collector of Q3-Q4 goes sufficiently positive

(due to the amplified ONE input signal), the strobe clamps the collector of Q1 or Q2 to ground. Resistor R10 prevents the differential stage (Q1 or Q2) from saturating during a large digit transient and allows the base of Q5 to become positive with respect to the emitter. The positive pulse at the collector of Q6 sets the flip-flop that turns off Q7 and saturates Q8. The flip-flop therefore registers a binary ONE which corresponds to the state of the selected memory core.

A ZERO output does not have sufficient amplitude at strobe time to saturate transistor Q5. Resistor divider network R11-R13 holds Q5 in the OFF state. The flip-flop will not receive a set input so it remains in the zero state (since it was reset at the start of the cycle).

NOTE

For all applications of the BR-32 , pin 35 should be jumpered to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Frequency of Operation

The maximum frequency of operation of the sense amplifier is 500 KC. Frequency of operation of the flip-flop is DC to 1 MC (max).

Input

The minimum ONE input signal required is 50 MV (25 MV to each base of the differential amplifier), while the maximum ZERO input signal is 15 MV.

The strobe input is a -6-volts to 0-volt pulse with a nominal width of 0.20 μsec. The load on the strobe driver is 0.5 ma per channel (1 ma per PAC) with the input at -6 volts, and 0 ma with the strobe at 0 volt.

The inputs to the flip-flop portion of the circuit include AC set and reset inputs, set and reset node inputs, a common reset input, and AC set inputs from the strobed sense amplifiers. Load and signal requirements are the same as for the FA-30 S-PAC.

Output

The outputs are flip-flop set and reset outputs. The output characteristics are the same as for the FA-30 S-PAC.

Circuit Delay

The analog signal delay between sense input and monitor point (at the collectors of Q3 and Q4) is 0.20 to 0.30 μsec. The turn-on delay between the strobe input and sense amplifier strobed output (at the collector of Q6) is typically 0.20 μsec, while the turn-off delay is 0.30 to 0.40 μsec.

Output Waveform Characteristics

The strobed output of the sensed amplifier (on the collector of Q6) is a 0.30 to 0.40 μsec width pulse with a maximum rise time of 0.10 μsec and a fall time of typically 0.20 μsec.

The flip-flop output pulses are standard S-PAC signals. The waveform characteristics are the same as for the FA-30 S-PAC.

Current Requirements

-18 V: 100 ma
- 6 V: 34 ma
+12 V: 50 ma

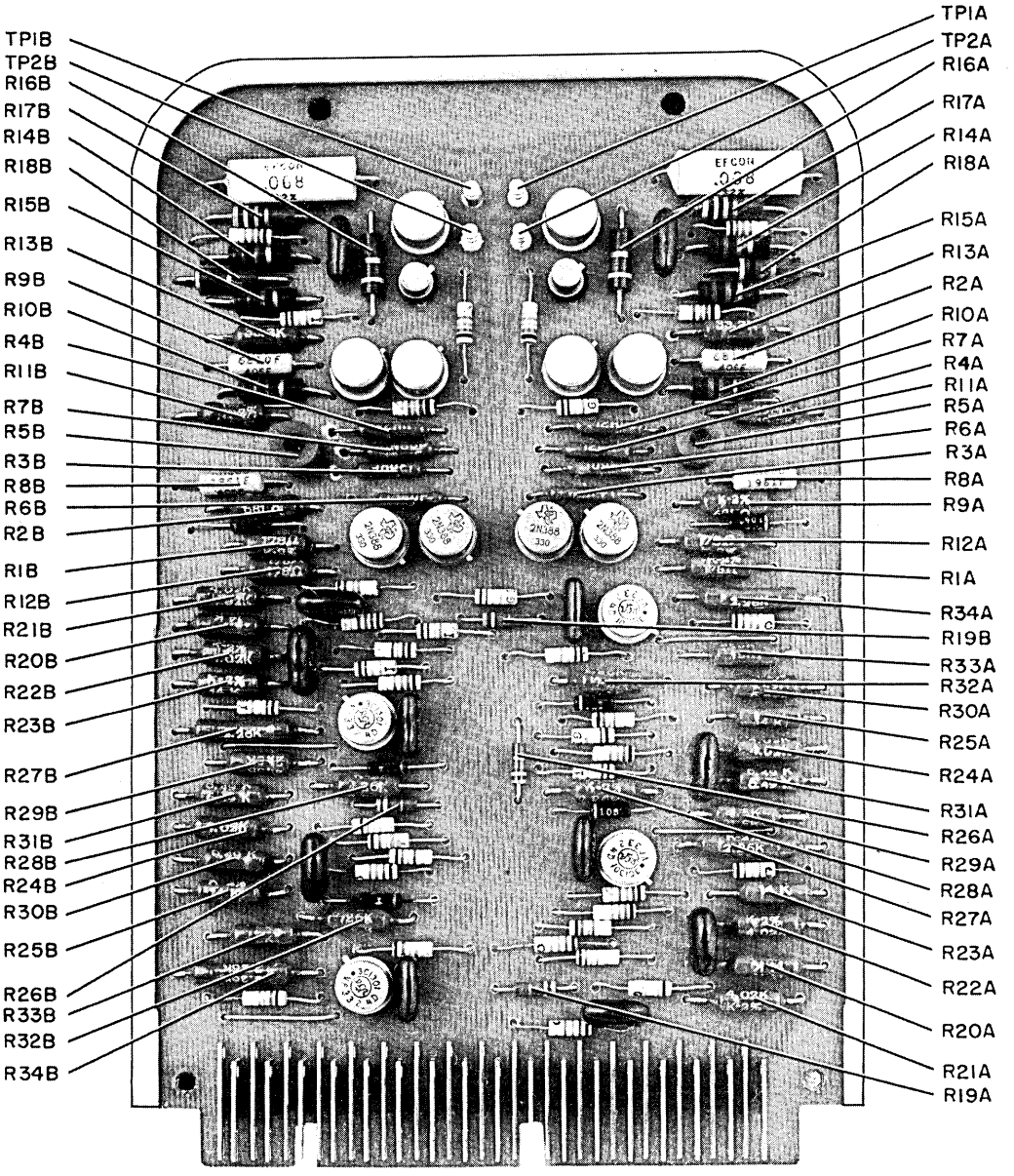


Figure 1. Bit Register PAC, Model BR-32,
Parts Location (Resistors and Test Points)

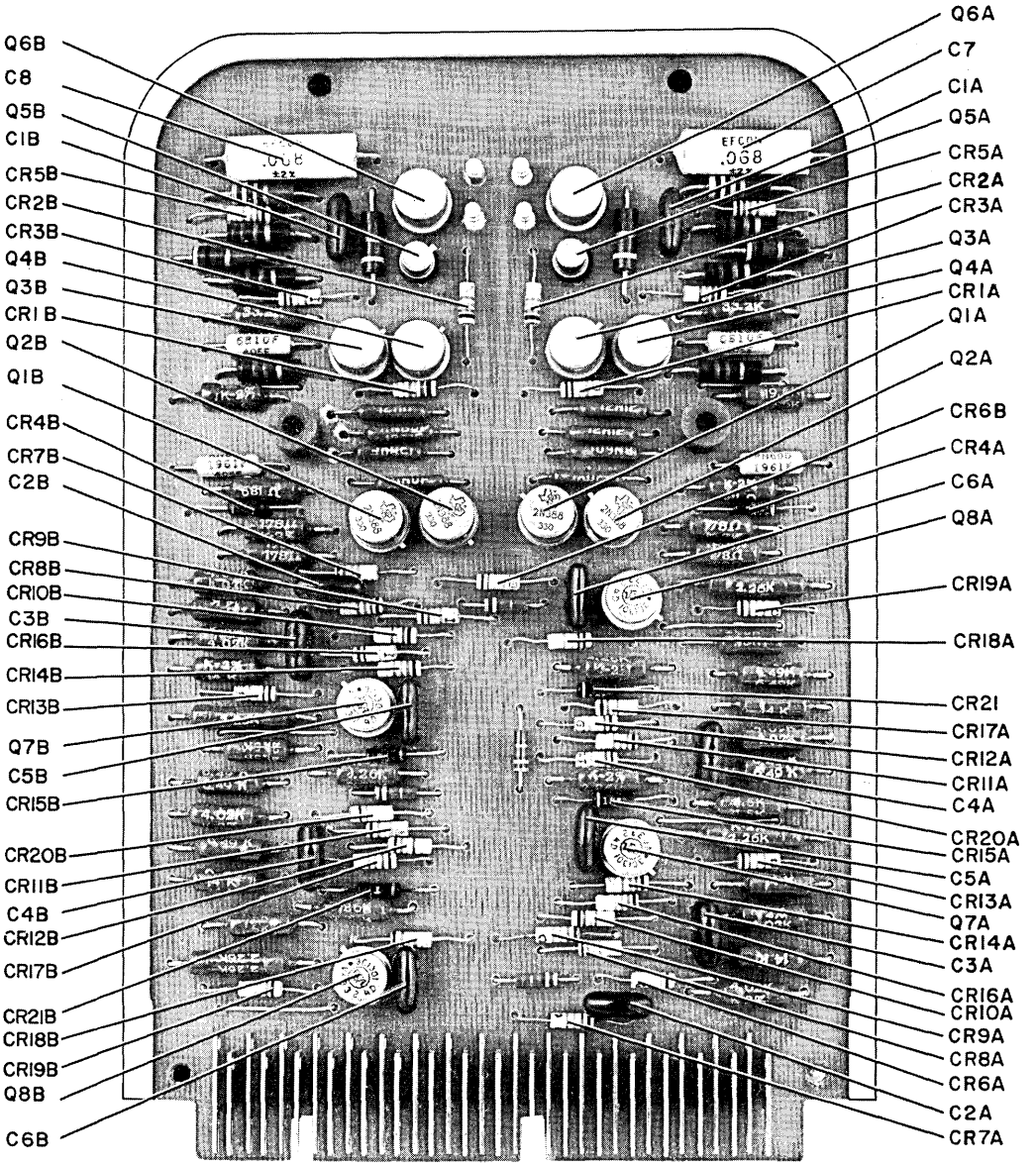


Figure 2. Bit Register PAC, Model BR-32,
Parts Location (Capacitors, Diodes, and Transistors)

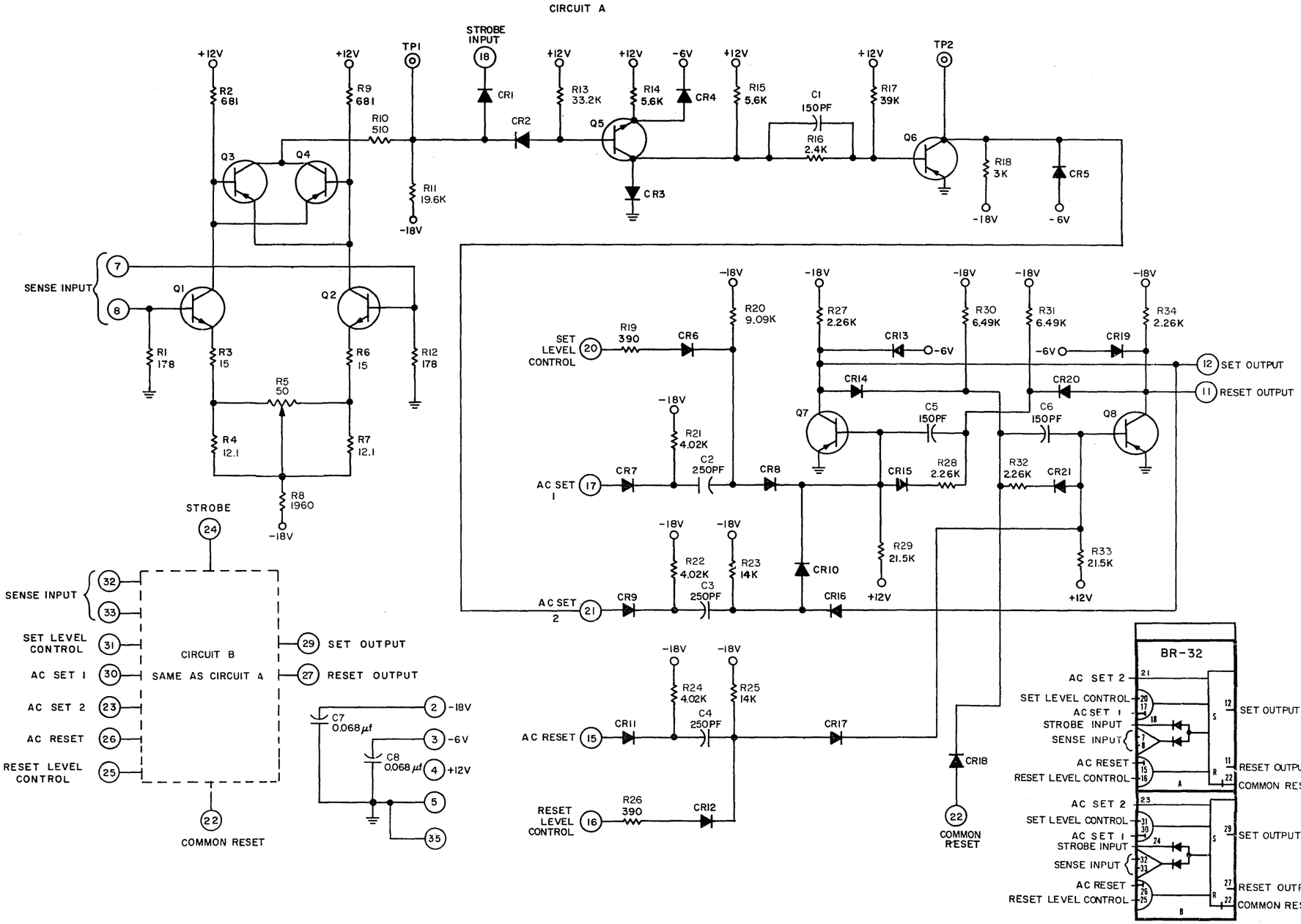


Figure 3. Bit Register PAC, Model BR-32, Schematic and Logic Diagram

BIT REGISTER PAC, MODEL BR-32, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F — DESCRIPTION	3C DWG NO.
C1, C5, C6	CAP, fxd, mica dielec: 150 pf ±5%, 100 VDC	930 011 131
C2, C3, C4	CAP, fxd, mica dielec: 250 pf ±5%, 100 VDC	930 011 137
C7, C8	CAP, fxd, plastic dielec: 0.068 μf ±20%, 100 VDC	930 301 015
CR4, CR15,	DIODE: Replacement type 1N816	943 105 001
CR21		
CR1-CR3,	DIODE: Replacement type 1N695	943 023 001
CR5-CR14,		
CR16-CR20		
R1, R12	RES, fxd, film: 178 ohms ±2%, 1/4 W	932 102 113
R2, R9	RES, fxd, film: 681 ohms ±1%, 1/4 W	932 108 181
R3, R6	RES, fxd, film: 15.0 ohms ±1%, 1/4 W	932 108 018
R4, R7	RES, fxd, film: 12.1 ohms ±1%, 1/4 W	932 108 009
R5	RES, variable wirewound: 50 ohms ±10% 1/4 W	933 205 002
R8	RES, fxd, film: 1.96 K ±1%, 1/4 W	932 108 229
R10	RES, fxd, comp: 510 ohms ±5%, 1/2 W	932 004 042
R11	RES, fxd, film: 19.6 K ±2%, 1/4 W	932 102 315
R13	RES, fxd, comp: 33.2 K ±2%, 1/4 W	932 102 326
R14, R15	RES, fxd, comp: 5.6 K ±5%, 1/2 W	932 004 067
R16	RES, fxd, comp: 2.4 K ±5%, 1/2 W	932 004 058
R17	RES, fxd, comp: 39 K ±5%, 1/2 W	932 004 087
R18	RES, fxd, comp: 3 K ±5%, 1/2 W	932 004 060
R19, R26	RES, fxd, comp: 390 ohms ±5%, 1/4 W	932 007 039
R20	RES, fxd, film: 9.09 K ±2%, 1/4 W	932 102 247
R21, R22, R24	RES, fxd, film: 4.02 K ±2%, 1/4 W	932 102 230
R23, R25	RES, fxd, film: 14 K ±2%, 1/4 W	932 102 308
R27, R34	RES, fxd, film: 2.26 K ±2%, 1/2 W	932 103 218
R28, R32	RES, fxd, film: 2.26 K ±2%, 1/4 W	932 102 218
R29, R33	RES, fxd, film: 21.5 K ±2%, 1/4 W	932 102 317
R30, R31	RES, fxd, film: 6.49 K ±2%, 1/4 W	932 102 240

BIT REGISTER PAC, MODEL BR-32, PARTS LIST (Cont)

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
Q1, Q2		TSTR: Replacement type 2N388	943 507 001
Q3, Q4, Q6		TSTR: Replacement type 2N1303	943 537 001
Q5		TSTR: Replacement type 2N706	943 700 001
Q7, Q8		TSTR: Replacement type 2N1301	943 535 002

ADDRESS DECODER PAC, MODEL DP-32

GENERAL DESCRIPTION

The Address Decoder PAC, Model DP-32 (Figures 1 and 2), contains a prewired binary-to-octal decoder. The octal matrix has nine input lines and eight output lines. Six inputs (three complementary pairs) are wired to activate one of the eight outputs. The three additional input lines are provided to permit the matrix to be expanded to 16, 32, or 64 outputs by connecting additional PACs in parallel. Two additional independent NAND gates are included on each PAC.

CIRCUIT DESCRIPTION

Octal Matrix

The octal matrix has nine input lines driving eight NAND gates (Figure 3). Six of the nine input lines (pins 15 through 20 inclusive) are driven by the assertions and negations of a 3-bit binary number. These six input lines are prewired to three inputs on each of the eight gates. The three inputs then become discrete combinations of the three binary bits and their negations. As an example, the gate driving output line six (pin 9) has $\overline{2}^0$, 2^1, and 2^2 as the three inputs.

Each of the eight gates has six inputs. Three inputs recognize a discrete binary number from 000 through 111 as described above. The other three inputs are common to all eight gates and are brought out to pins 12, 13, and 14 on the connector. The six inputs to any gate must be a ONE (-6 V) to activate the gate output. Since pins 12, 13, and 14 form three common and direct inputs to all eight gates, all the inputs must be ONEs to have one of the eight output lines activated (0 V). When deactivated an output line is -18 volts.

No connection to pins 12, 13, or 14 is equivalent to having the input at ONE. The application of a ZERO to any one of the common input lines inhibits the octal matrix. This feature is useful for application on multioctal matrices, BCD-to-decimal decoding, and strobing.

Multioctal Matrices

Matrices having 16, 32, or 64 outputs are formed by driving multiple octal matrices in parallel. It is necessary to inhibit all but the one matrix that contains the significant output line. As an example, in a 64-output matrix, eight octal matrices are used. It is necessary to inhibit seven of these

to activate one of 64 output lines. The seven octal matrices are inhibited by applying ZERO to either pin 12, 13, or 14. For example, if the binary bits 2^3, 2^4, and 2^5 are true (ONE), the seven matrices containing outputs 0 through 55 inclusive are inhibited. Only one output from 56 to 63 is activated, depending on the states of bits 2^0, 2^1, and 2^2.

SPECIFICATIONS

Input Loading

Binary-to-Octal and Multioctal Matrices

8 output decoder (3 bits): 3 unit loads each

16 output decoder (4 bits): 4 unit loads each

32 output decoder (15 bits): 7 unit loads each

64 output decoder (6 bits): 14 unit loads each

BCD-to-Decimal Decoder

Binary bits 2^0, and $\overline{2}^0$	4 unit loads each
Binary bits 2^1, $\overline{2}^1$, 2^2, and $\overline{2}^2$	3 unit loads each
Binary bits 2^3	2 unit loads each
Binary bit $\overline{2}^3$	5 unit loads each

Frequency of Operation

DC to 500 KC

Circuit Delay

Turn-on delay:	0.05 μsec (typ) 0.10 μsec (max)
Turn-off delay:	0.10 μsec (typ) 0.15 μsec (max)

Output Waveform Characteristics

Rise time:	0.40 μsec (typ) 0.60 μsec (max)
Fall time:	0.80 μsec (typ) 1.0 μsec (max)

Output Drive Capability

17.5 ma and 500 pf each output (selection switch load)

Power Requirements

-18 V: 77 ma

- 6 V: 11 ma (current from supply)

+12 V: 5 ma

Total Power

1.6 W

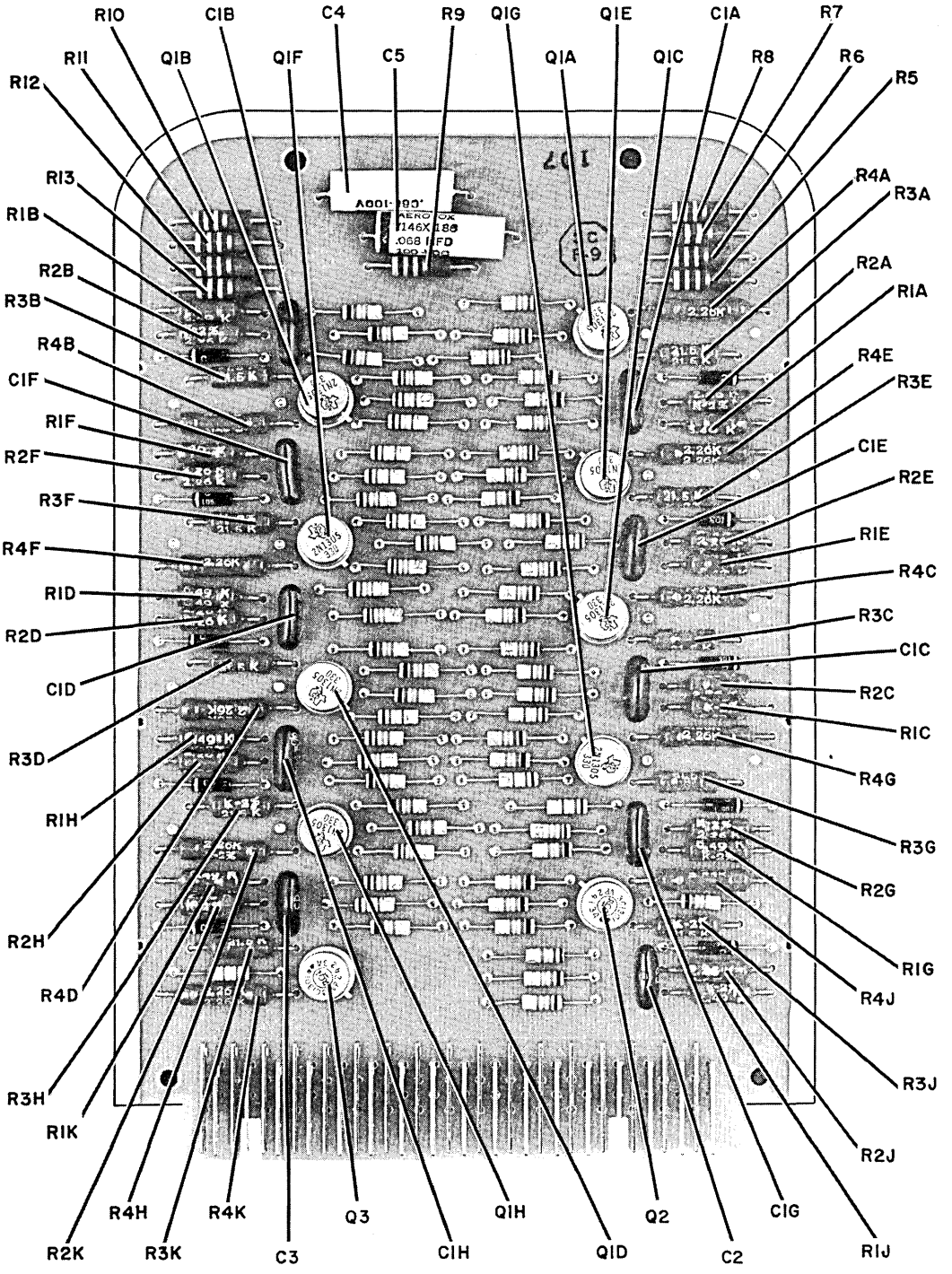


Figure 1. Address Decoder PAC, Model DP-32, Parts Location (Resistors, Capacitors, and Transistors)

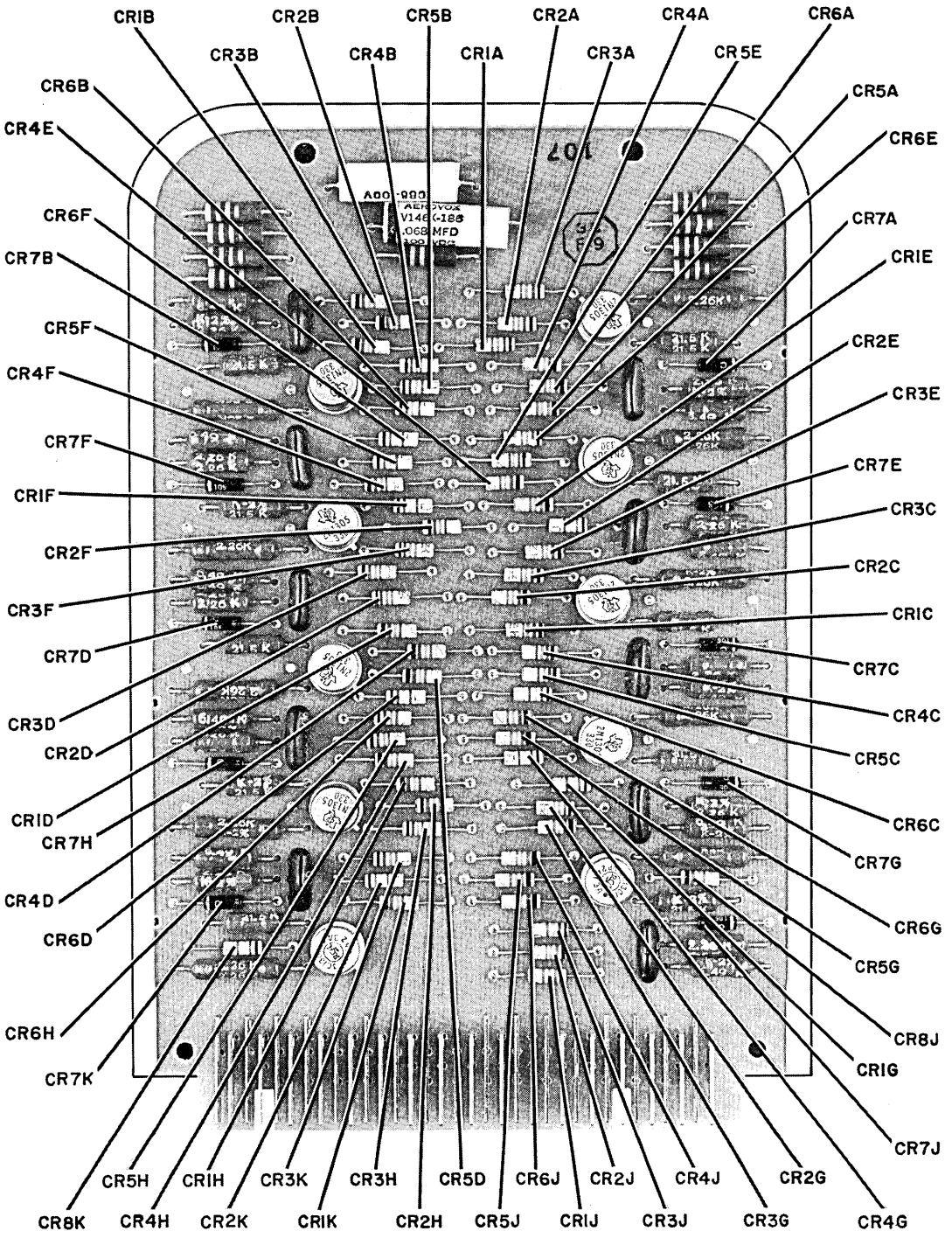
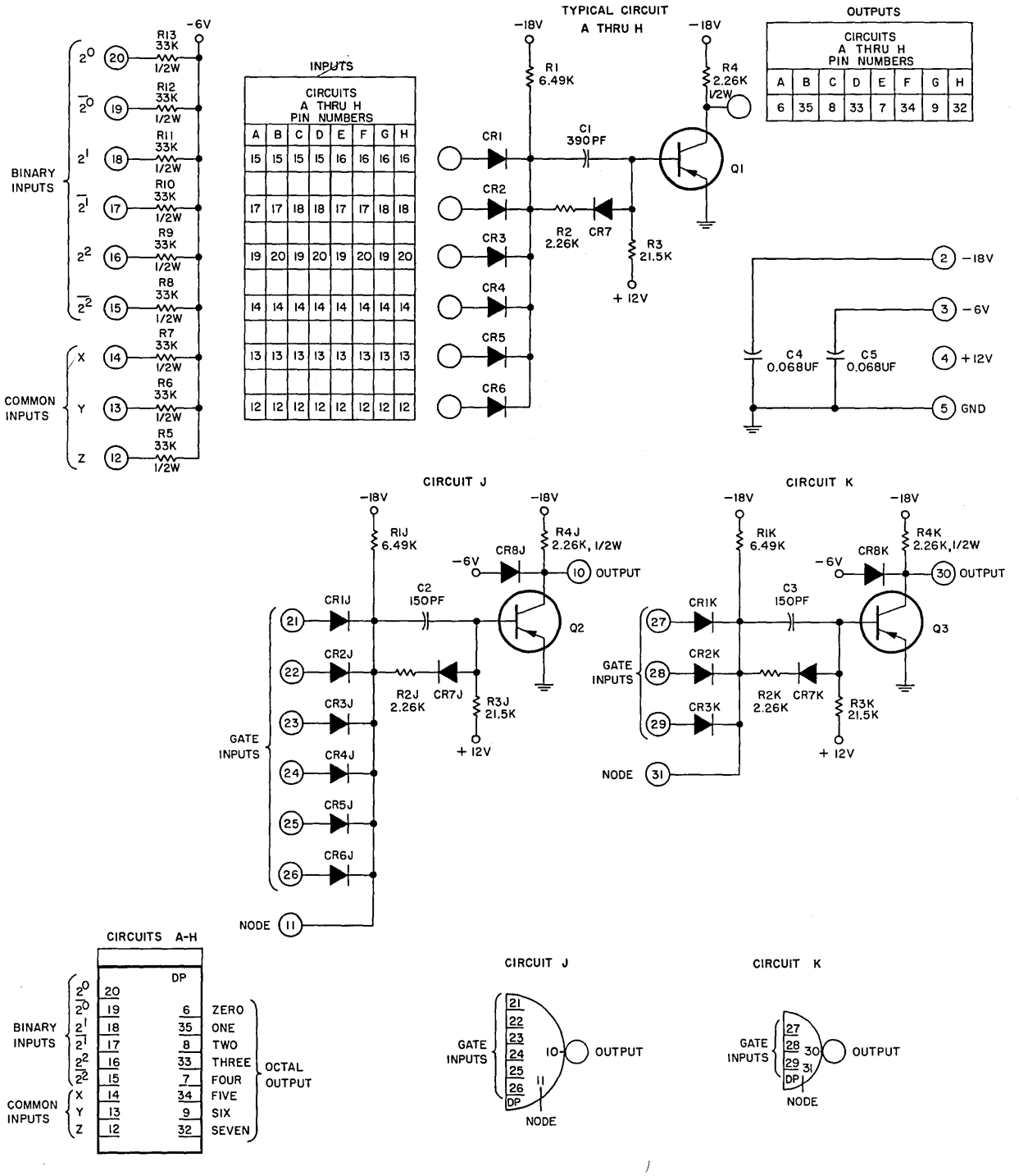


Figure 2. Address Decoder PAC, Model DP-32, Parts Location (Diodes)



Address Decoder PAC, Model DP-32, Schematic and Logic Diagram

ADDRESS DECODER PAC, MODEL DP-32 PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F — DESCRIPTION	3C DWG NO.
C1	CAP, fxd, mica dielec: 390 pf ±10%, 100 VDC	930 011 142
C2, C3	CAP, fxd, mica dielec: 150 pf ±5%, 100 VDC	930 011 131
C4, C5	CAP, fxd, plastic dielec: 0.068 µf ±20%, 100 VDC	930 301 015
CR1-CR6	DIODE: Replacement type 1N695	943 023 001
CR7	DIODE: Replacement type 1N816	943 105 001
R1	RES, fxd, film: 6.49 K ±2%, 1/4 W	932 102 240
R2	RES, fxd, film: 2.26 K ±2%, 1/4 W	932 102 218
R3	RES, fxd, film: 21.5 K ±2%, 1/4 W	932 102 317
R4	RES, fxd, film: 2.26 K ±2%, 1/2 W	932 103 218
R5-R13	RES, fxd, comp: 33 K ±5%, 1/2 W	932 004 085
Q1	TSTR: Replacement type 2N1305	943 537 002
Q2, Q3	TSTR: Replacement type 2N1301	943 535 002

GATE DRIVER PAC, MODEL GD-32

GENERAL DESCRIPTION

The Gate Driver PAC, Model GD-32 (Figures 1 and 2), consists of four identical amplifier stages that provide read and write gating pulses to X and Y selection switches.

CIRCUIT DESCRIPTION

A 0-volt input to the NAND gate (Figure 3) holds transistor Q1 off. The collector of Q1 is clamped to -6.3 volts by ON transistor Q2. Diodes CR4 and CR5 are normally off. Transistor Q3 is off due to diode CR6 and resistor R8. The output at the collector of Q3 is clamped to +0.6 volts by diode CR7 and resistor R7.

When all inputs to the NAND gate are at -6 volts, transistor Q1 saturates. The resulting +6-volt pulse at the collector of Q1 turns on diode CR4 and transistor Q3 through capacitor C2. Transistor Q2 is reverse-biased by diode CR4. The collector of Q3 falls to -17 volts and diode CR7 is reverse-biased. During the fall time of the input pulse the collector of transistor Q1 is clamped to -6.3 volts by transistor Q2. Diode CR4 becomes reverse-biased. The negative pulse at the emitter of Q2 is coupled through capacitor C2 and turns off transistor Q3. Capacitor C2 discharges rapidly through transistor Q2 and diode CR5.

NOTE

For all applications of the GD-32, pin 35 should be jumpered to pin 5 (ground). The jumper attenuates noise picked up by distributed impedance of the etched circuit.

SPECIFICATIONS

Frequency of Operation

The GD-32 can be used at frequencies up to 500 KC.
The minimum time between pulses is 1 μsec.
The maximum input pulse width is 5 μsec.

Input

The input is a standard S-PAC signal. The input loading is 1 unit load and 320 pf per channel.

Output

The output is a +0.6 to -17-volt pulse. Each output will provide 70 ma when it is at -17 volts and 0 ma when it is at +0.6 volt.

Circuit Delay

Turn on delay (10% to 10%):
0.30 μsec (typ)
0.50 μsec (max)

Turn off delay (90% to 90%):
0.30 μsec (typ)
0.50 μsec (max)

Output Waveform Characteristics

Rise time (10% to 90%):
0.06 μsec (typ)
0.10 μsec (max)

Fall time (90% to 10%):
0.25 μsec (typ)
0.30 μsec (max)

Current Requirements

All channels off:
-18 V: 57 ma
- 6 V: 21 ma (from supply)
+12 V: 48 ma

Normal operating conditions:
2 μsec: read channels on, write channels off
2 μsec: write channels on, read channels on
1 μsec: all channels off
-18 V: 172 ma
- 6 V: 12 ma (from supply)
+12 V: 78 ma

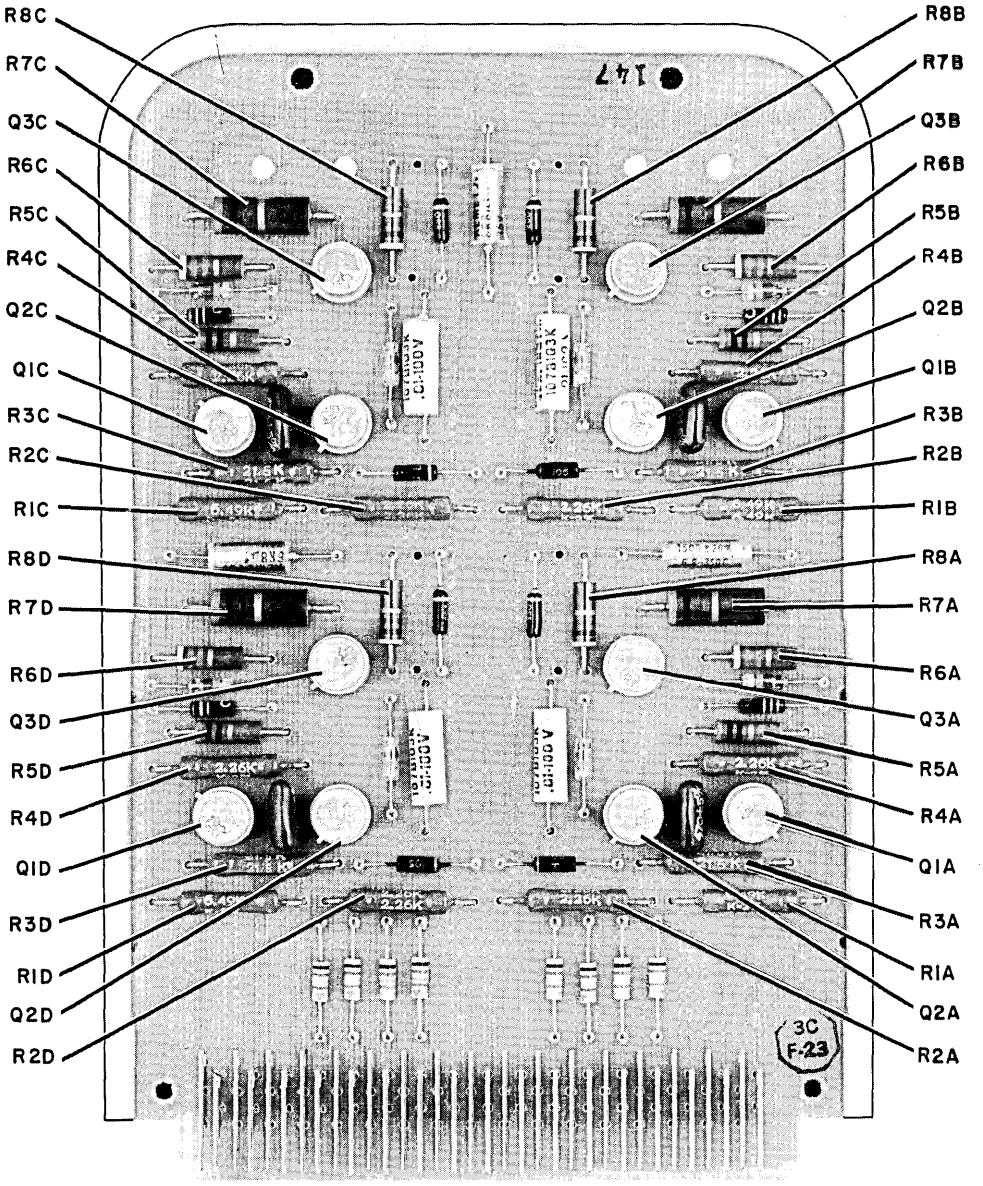


Figure 1. Gate Driver PAC, Model GD-32,
Parts Location (Resistors and Transistors)

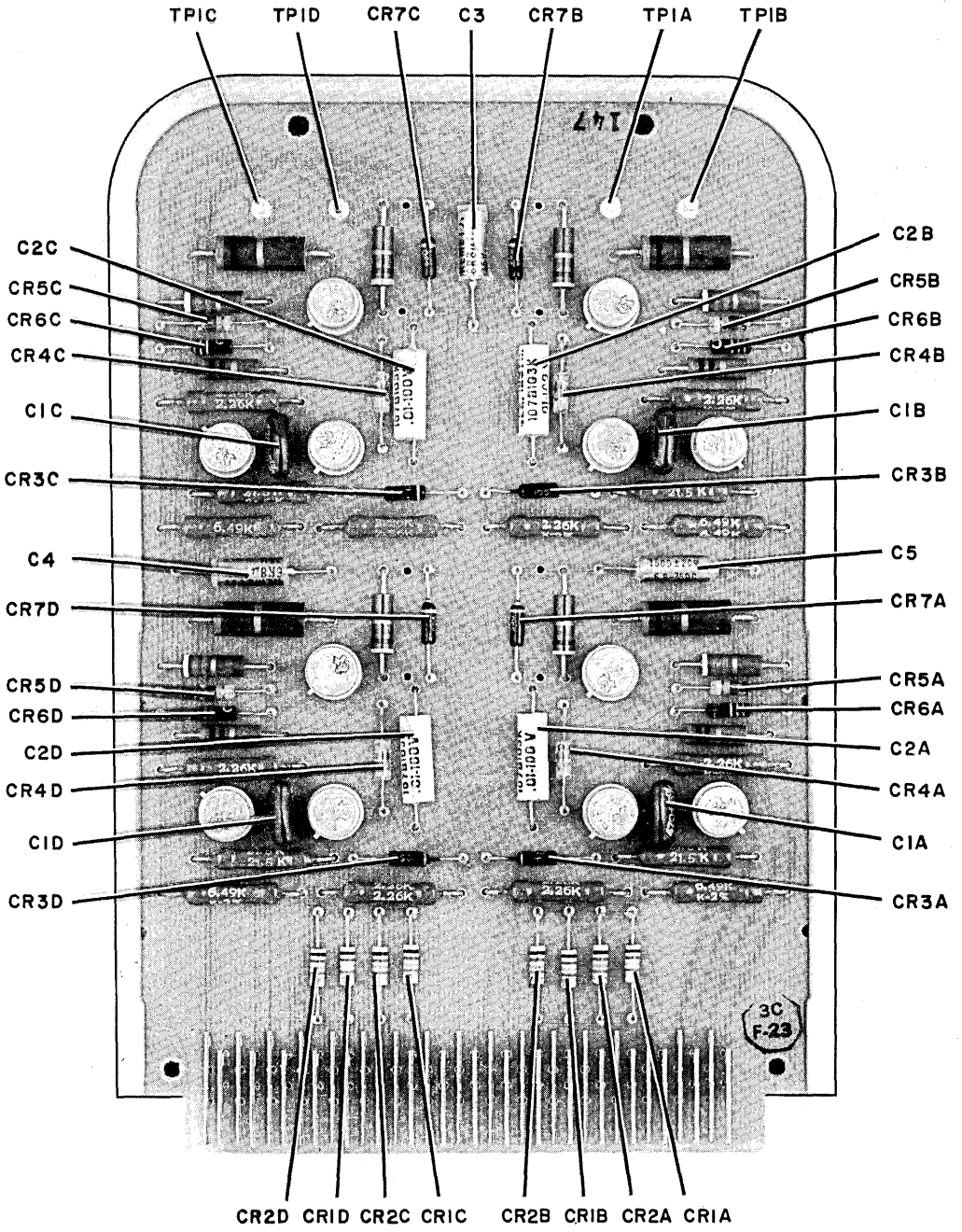
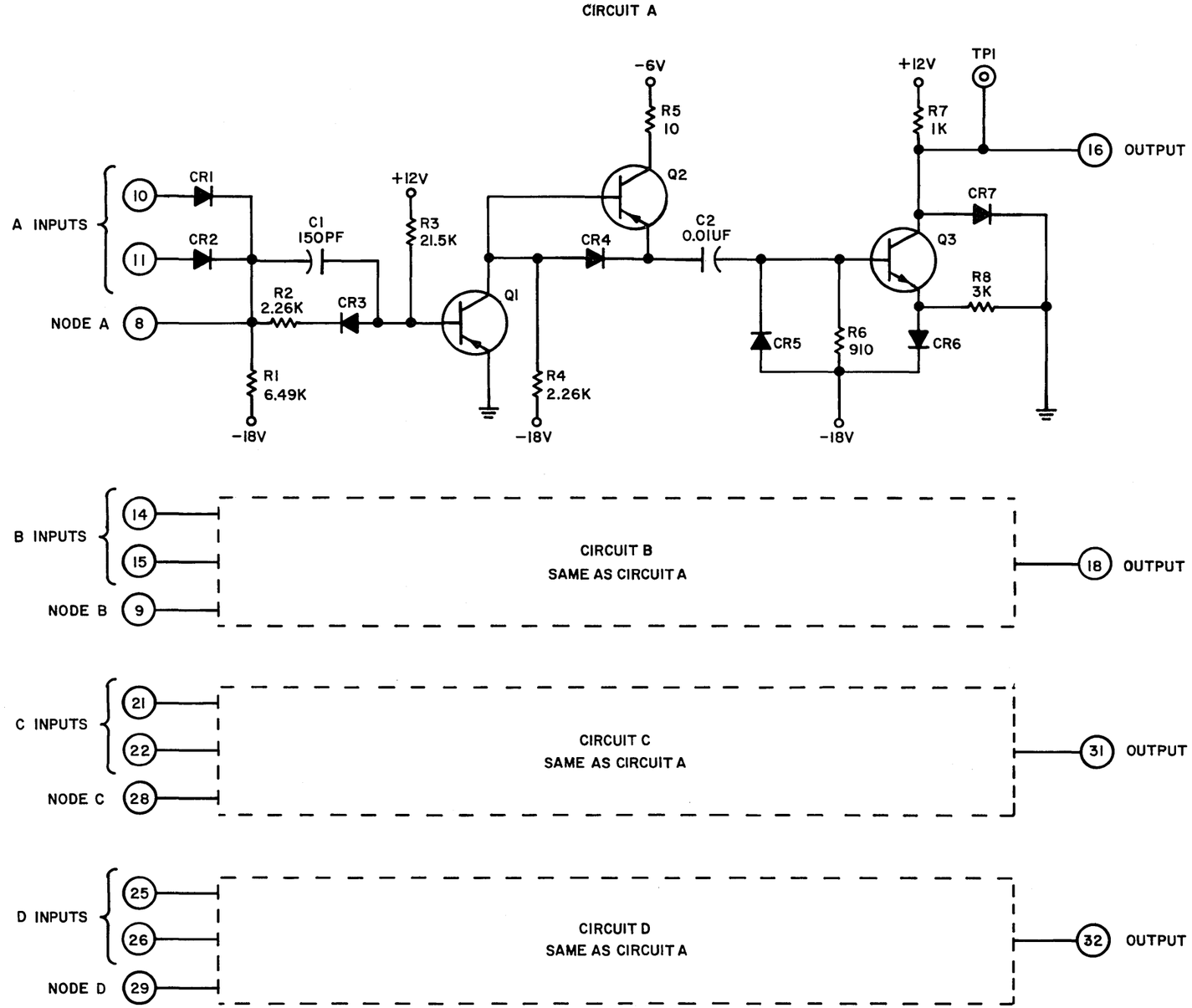
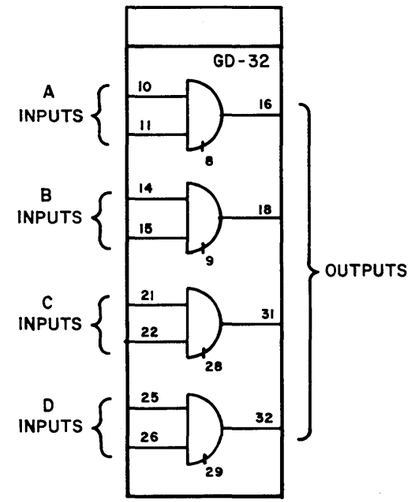


Figure 2. Gate Driver PAC, Model GD-32,
Parts Location (Capacitors, Diodes, and Test Points)





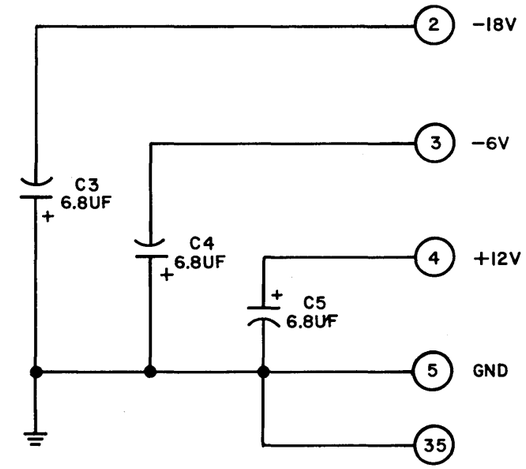


Figure 3. Gate Driver PAC, Model GD-32, Schematic and Logic Diagram

GATE DRIVER PAC, MODEL GD-32, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
C1		CAP, fxd, mica dielec: 150 pf ±10%, 100 V	930 011 131
C2		CAP, fxd, plastic dielec: 0.01 μf ±20%, 100 V	930 301 009
C3-C5		CAP, fxd, elec TANTalum: 6.8 μf ±20%, 35 V	930 217 020
CR1, CR2		DIODE: Replacement type 1N695	943 023 001
CR3		DIODE: Replacement type 1N816	943 105 001
CR4, CR5		DIODE: Replacement type CTP462	943 001 001
CR6		DIODE: Replacement type 1N816	943 008 001
CR7		DIODE: Replacement type 1N916	943 083 001
R1		RES, fxd, film: 6.49 K ±2%, 1/2 W	932 103 240
R2, R4		RES, fxd, film: 2.26 K ±2%, 1/2 W	932 103 218
R3		RES, fxd, film: 21.5 K ±2%, 1/2 W	932 103 317
R5		RES, fxd, comp: 10 ohms ±5%, 1/2 W	932 004 001
R6		RES, fxd, comp: 910 ohms ±5%, 1/2 W	932 004 048
R7		RES, fxd, comp: 1 K ±5%, 1 W	932 005 049
R8		RES, fxd, comp: 3 K ±5%, 1/2 W	932 004 060
Q1, Q2		TSTR: Replacement type 3C1301	943 535 002
Q3		TSTR: Replacement type 2N388	943 507 001

DYNAMIC CURRENT DRIVER PAC, MODEL MD-32

GENERAL DESCRIPTION

The Dynamic Current Driver PAC, Model MD-32 (Figure 1), contains two identical amplifier and current regulator stages that provide temperature-compensated currents of up to 300 ma to memory drive lines. Each channel is a read or write constant-current source and is switched on and off by memory control pulses. A thermistor-controlled voltage reference network provides currents that are compensated to match the temperature characteristics of the magnetic cores. Rise and fall times of the output current are controlled by passive components. The current amplitude is adjusted by means of an externally mounted potentiometer.

CIRCUIT DESCRIPTION

Transistors Q1, Q3, Q4, and Q5 (Figure 2) are off and Q2 is on with no input pulse applied. Transistor Q2 and diode CR3 hold the base of Q3 at -18 V. Diode CR4 is reverse-biased and its cathode is held at -14 V (at 25°C) by the thermistor-controlled reference voltage network.

A positive control input pulse (-6 to 0 V) turns on Q1. The negative pulse on the collector of Q1 is coupled through capacitor C2 to turn off transistor Q2. When Q2 is turned off, its collector is clamped to -6 volts by diode CR2. This voltage turns off CR3 which clamps the base of Q3 to the -14-volt reference voltage.

The positive pulse at the base of Q3 turns on the emitter-follower and applies a 4-volt pulse to turn on Q4 and Q5. The emitter currents of transistors Q4 and Q5 are determined by the reference voltage and their respective emitter resistors. The output current flow is the sum of the collector currents on Q4 and Q5. Since transistors Q4 and Q5 are not saturated, the output current is independent of the load voltage. The output current amplitude varies nominally -0.5%/°C over a 0 to 50°C range to match the temperature coefficient of the magnetic cores.

SPECIFICATIONS

Frequency of Operation

The maximum operating frequency is 400 KC with a maximum duty cycle of 50%.

Input

The input is a standard S-PAC (-6 to 0 V) signal with a duration determined by the output current pulse width desired. The input loading is 1 unit load plus 360 pf (input at 0 V) and 0.3 ma with input at -6 volts.

Output

Each output will provide constant-current pulses of 150 ma to 300 ma (determined by setting of the externally mounted potentiometer) into grounded loads. The currents will remain regulated for load back voltages up to -12 volts. The output current rise and fall times are controlled by C3 and C4 respectively.

Circuit Delay (at 250 ma, 25°C)

Turn on delay (10% to 10%):	0.25 μsec (typ) 0.50 μsec (max)
Turn off delay (90% to 90%):	0.25 μsec (typ) 0.50 μsec (max)

Output Current Waveform Characteristics (at 250 ma, 25°C)

Rise time (10% to 90%):	0.25 μsec (typ) 0.30 μsec (max)
Fall time (90% to 10%):	0.25 μsec (typ) 0.30 μsec (max)

Current Requirements

Both Channels Off	Split Cycle (50% duty cycle)	Full Cycle (25% duty cycle)
-18 V: 125 ma	-18 V: 280 ma	-18 V: 140 ma
- 6 V: <0.1 ma	- 6 V: 36 ma (into supply)	- 6 V: 18 ma (into supply)
+12 V: 36 ma	+12 V: 26 ma	+12 V: 13 ma

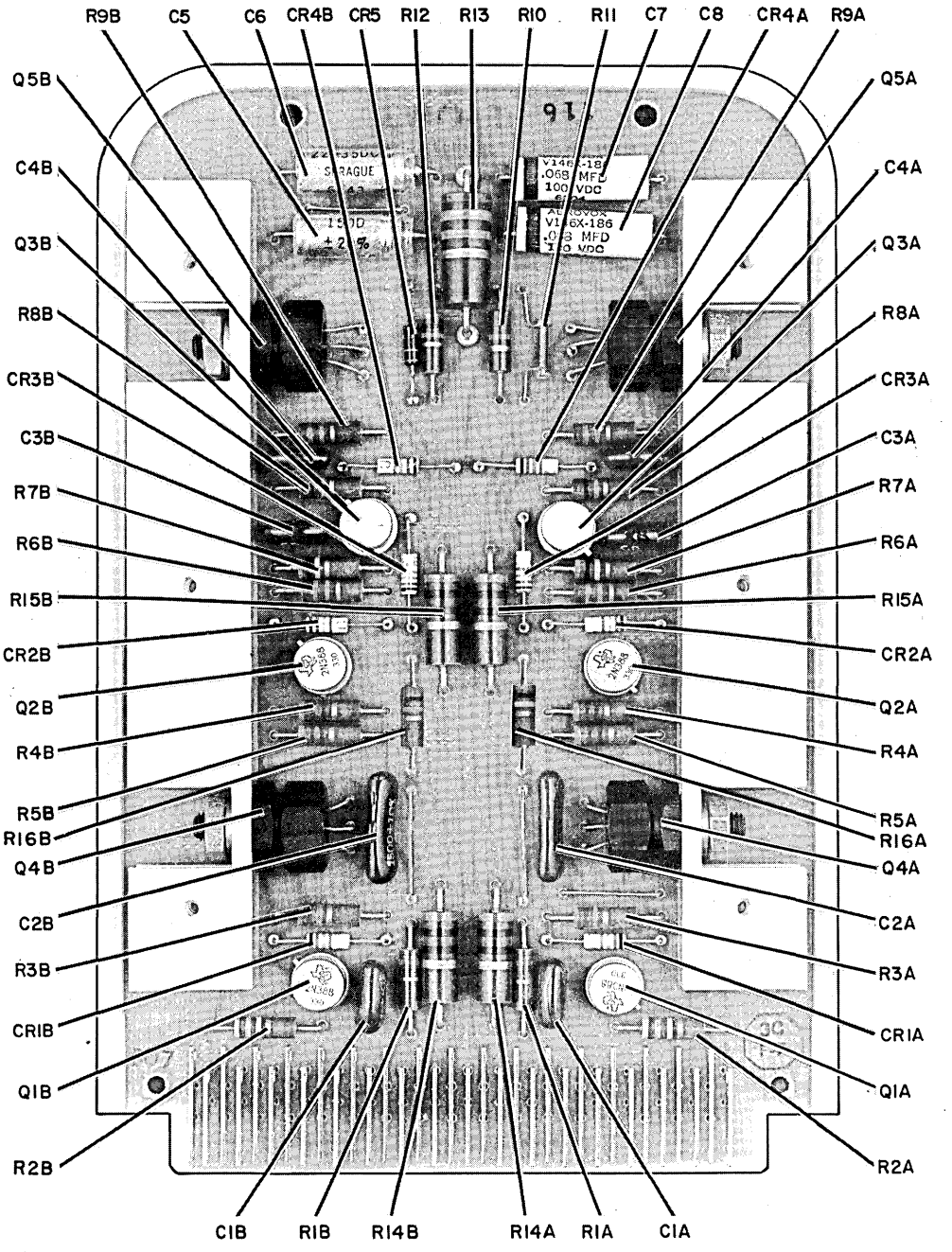


Figure 1. Dynamic Current Driver PAC, Model MD-32, Parts Location

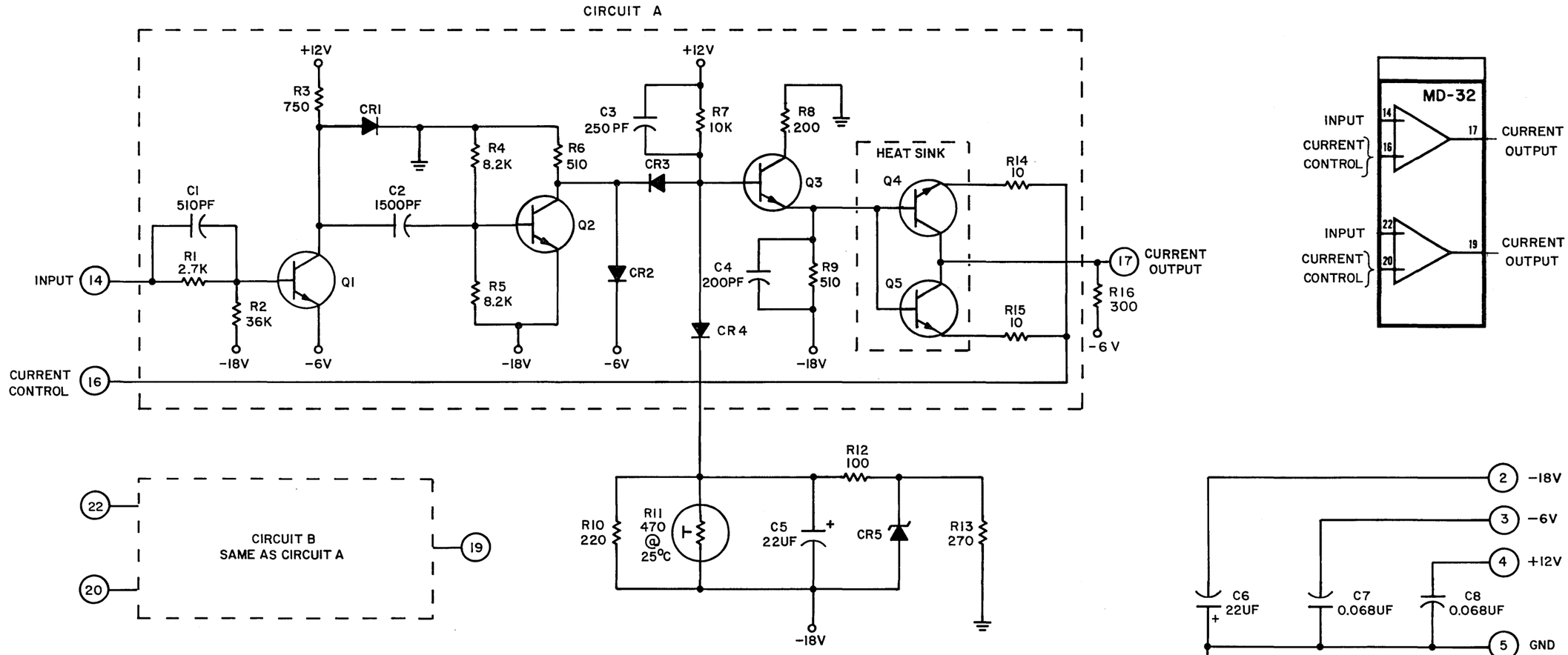


Figure 2. Dynamic Current Driver PAC, Model MD-32, Schematic and Logic Diagram

DYNAMIC CURRENT DRIVER PAC, MODEL MD-32, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F — DESCRIPTION	3C DWG NO.
C1	CAP, fxd, mica dielec: 510 pf ±10%, 100 VDC	930 011 046
C2	CAP, fxd, mica dielec: 1500 pf ±10%, 100 VDC	930 006 057
C3	CAP, fxd, mica dielec: 250 pf ±5%, 100 VDC	930 011 137
C4	CAP, fxd, mica dielec: 200 pf ±10%, 100 VDC	930 011 034
C5, C6	CAP, fxd, elec TANTalum: 22 µf ±20%, 35 VDC	930 217 023
C7, C8	CAP, fxd, plastic dielec: 0.068 µf ±20%, 100 VDC	930 301 015
CR1-CR4	DIODE: Replacement type 1N695	943 023 001
CR5	DIODE: Replacement type 1N706	943 102 001
R1	RES, fxd, comp: 2.7 K ±5%, 1/2 W	932 004 059
R2	RES, fxd, comp: 36 K ±5%, 1/2 W	932 004 086
R3	RES, fxd, comp: 750 ohms ±5%, 1/2 W	932 004 046
R4, R5	RES, fxd, comp: 8.2 K ±5%, 1/2 W	932 004 071
R6, R9	RES, fxd, comp: 510 ohms ±5%, 1/2 W	932 004 042
R7	RES, fxd, comp: 10 K ±5%, 1/2 W	932 004 073
R8	RES, fxd, comp: 200 ohms ±5%, 1/2 W	932 004 032
R10	RES, fxd, comp: 220 ohms ±5%, 1/2 W	932 004 033
R11	RES, THERMal: 470 ohms (25°C)	932 300 002
R12	RES, fxd, comp: 100 ohms ±5%, 1/2 W	932 004 025
R13	RES, fxd, comp: 270 ohms ±5%, 2 W	932 006 035
R14, R15	RES, fxd, comp: 10 ohms ±5%, 1 W	932 005 001
R16	RES, fxd, comp: 300 ohms ±5%, 1/2 W	932 004 036
Q1, Q2	TSTR: Replacement type 2N388	943 507 001
Q3	TSTR: Replacement type 2N1959	943 703 001
Q4, Q5	TSTR: Replacement type 2N2219	943 705 003

INHIBIT DRIVER PAC, MODEL MI-32

GENERAL DESCRIPTION

The Inhibit Driver PAC, Model MI-32 (Figures 1 and 2), contains eight identical channels that provide inhibit current of 150 to 300 ma. An amplifier is provided to supply a common amplified timing signal to each driver circuit. The MI-32 can also be used as a solenoid driver or for other high-power driving applications.

CIRCUIT DESCRIPTION

The PAC contains eight switching circuits (Figure 3) that have positive logic AND gate inputs. Each switch can be inhibited by the output of timing amplifier Q1 which supplies one input to each switch with an amplified, inverted, memory inhibit input signal (ZS). Any gate input at -6 volts will hold output transistor Q4 off.

Transistors Q2 and Q3 are on and transistors Q4 and Q1 are off with no signal applied. When a negative input (ZS) is applied, transistor Q1 saturates. When all inputs to the positive AND gate are at 0 volt, transistor Q2 is cut off. The Q2 collector voltage rises toward -18 volts but it is clamped at -6 volts by transistor Q3. The negative pulse at the emitter of transistor Q3 saturates transistor Q4. The inhibit current flows from ground, through transistor Q4 and the inhibit board precision resistors, to the -18-volt supply. (During the fall time of the (ZS), input transistor Q1 turns off, turning on transistor Q2.) The positive pulse at the collector of transistor Q2 turns off transistor Q3 and turns on diode CR5. Transistor Q2 and diode CR5 provide a low impedance discharge path for capacitor C2 to allow a fast turnoff of transistor Q4.

SPECIFICATIONS

Frequency of Operation

The maximum operating frequency is dependent on the reactance of the load. Full cycle operation is at repetition frequencies of 200 KC with a duty cycle of 40 percent. Split cycle operation results in repetition frequencies of 400 KC with a duty cycle of 80 percent.

Input

The inputs are standard S-PAC 1-MC signals. The load on each -6-volt gate input is 2.2 ma (to hold the output channel in the OFF condition). The load on a 0-volt gate input is 1/2 unit load. The timing amplifier presents a load of 1.2 units plus 50 pf to the inhibit step timing input.

Output

Each output can switch load currents between 150 and 300 ma. The PAC can handle inductive loads as large as 20 μh (provided an appropriate current-limiting resistor is connected in series). Inductive back voltage up to 20 volts can be tolerated.

Circuit Delay

Turn on delay (10% to 10%):	0.15 μsec (typ) 0.20 μsec (max)
Turn off delay (90% to 90%):	0.40 μsec (typ) 0.60 μsec (max)

Output Current Waveform Characteristics (at 200 ma)

	No Load Inductance	4096-word plane L=15 μh (approx)
Rise time (10% to 90%):	0.30 μsec (typ) 0.40 μsec (max)	0.6 μsec (typ) 0.8 μsec (max)
Fall time (90% to 10%):	0.40 μsec (typ) 0.80 μsec (max)	0.60 μsec (typ) 1.0 μsec (max)

Current Requirements

The current requirements of the MI-32 are catalogued according to operation conditions below. The inhibit current drain from the -18-volt supply is not included as it appears under the specifications of the Inhibit Component Board.

	Split Cycle (80% Duty Cycle)		Full Cycle (40% Duty Cycle)	
	All Channels OFF	All Channels ON	All Channels OFF	All Channels ON
-18 V:	40 ma	58 ma	60 ma	43 ma
+12 V:	12 ma	60 ma	38 ma	29 ma
- 6 V: (current into supply)	1 ma	110 ma	14 ma	46 ma

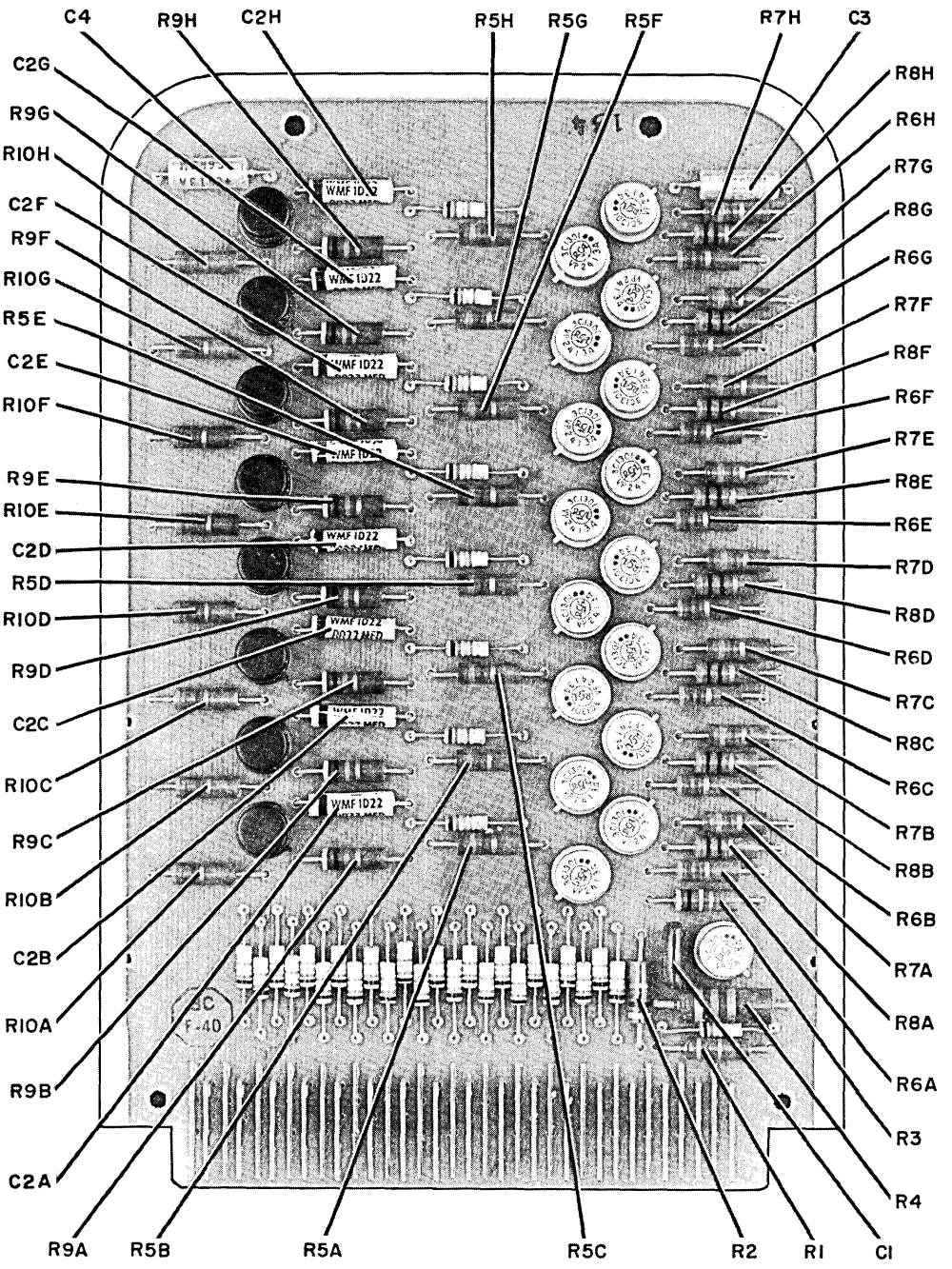


Figure 1. Inhibit Driver PAC, Model MI-32, Parts Location (Resistors and Capacitors)

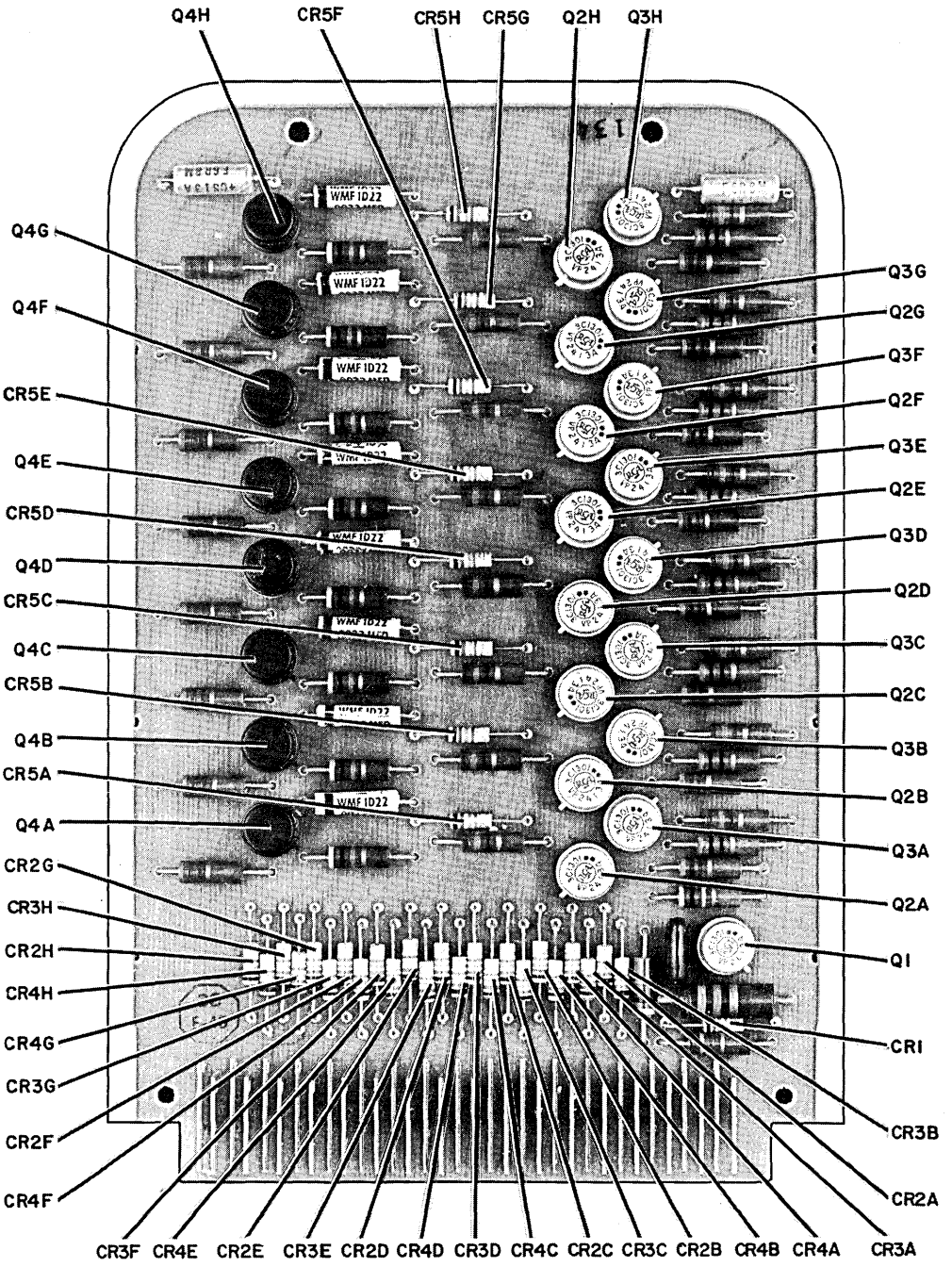


Figure 2. Inhibit Driver PAC, Model MI-32, Parts Location (Transistors and Diodes)

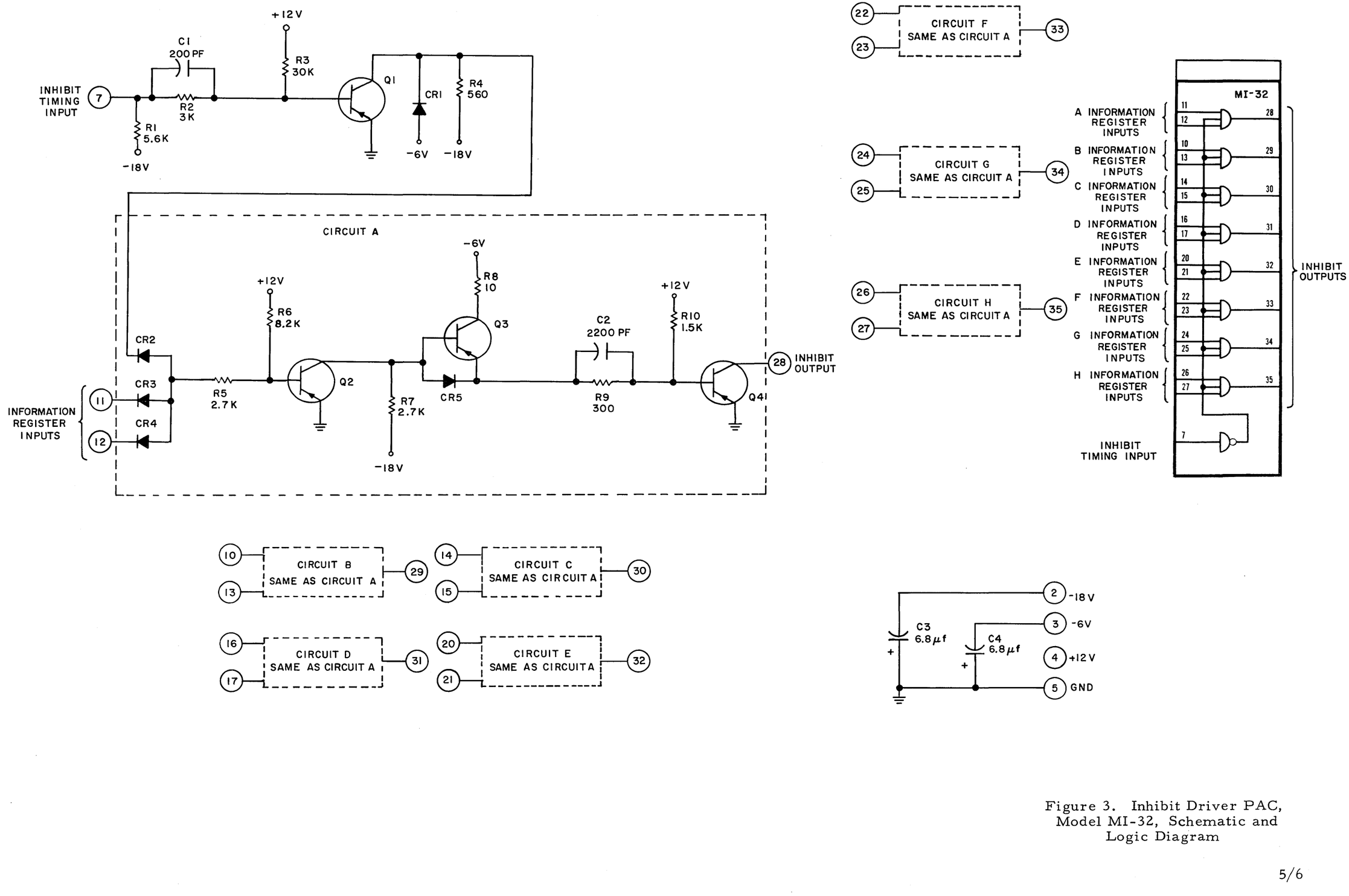


Figure 3. Inhibit Driver PAC, Model MI-32, Schematic and Logic Diagram

INHIBIT DRIVER PAC, MODEL MI-32, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
C1		CAP, fxd, mica dielec: 200 pf ±10%, 100 VDC	930 011 034
C2A-C2H		CAP, fxd, plastic dielec: 2200 pf ±20%, 100 VDC	930 301 004
C3, C4		CAP, fxd, elec, TANTalum: 6.8 µf 20%, 35 VDC	930 217 020
CR1-CR5		DIODE: Replacement type 1N695	943 023 001
R1		RES, fxd, comp: 5.6 K ±5%, 1/2 W	932 004 067
R2		RES, fxd, comp: 3 K ±5%, 1/2 W	932 004 060
R3		RES, fxd, comp: 30 K ±5%, 1/2 W	932 004 084
R4		RES, fxd, comp: 560 ohms ±5%, 1 W	932 005 043
R5, R7		RES, fxd, comp: 2.7 K ±5%, 1/2 W	932 004 059
R6		RES, fxd, comp: 8.2 K ±5%, 1/2 W	932 004 071
R8		RES, fxd, comp: 10 ohms ±5%, 1/2 W	932 004 001
R9		RES, fxd, comp: 300 ohms ±5%, 1/2 W	932 004 036
R10		RES, fxd, comp: 1.5 K ±5%, 1/2 W	932 004 053
Q1-Q3		TSTR: Replacement type 2N1301	943 535 002
Q4		TSTR: Replacement type 2N2374	943 553 002

SELECTION SWITCH PAC, MODEL SS-32

GENERAL DESCRIPTION

The Selection Switch PAC, Model SS-32 (Figures 1 and 2) contains eight gated transistor switches with current steering diodes for double-ended selection of memory drive lines. The proper output switch is turned on in response to the decoded address information. The read or write pulse input and the dynamic current source input determine the direction of current through the memory drive lines.

CIRCUIT DESCRIPTION

The eight input transistors, Q1 and Q2 (Figure 3), are gating transistors that are normally off. They are logical AND gates that saturate when a simultaneous -18 to 0-volt level and a +0.6 to -17-volt pulse are present.

Four output transistors, Q3A-Q4A and Q3B-Q4B, are the top switch pairs and are normally off. Each top switch pair is connected through current-steering diodes CR3-CR18 to eight memory drive lines. The four output transistors Q3C-Q4C and Q3D-Q4D are the bottom (normally off) switch pairs and connect to bused drive lines.

Selecting an individual drive line in the X or Y coordinate is accomplished by turning on one top switch pair and one bottom switch pair. The selected switch pairs are activated by the presence of a decoder input level. The read or write pulse input determines which input transistor in each switch pair is selected. The PAC outputs are connected to allow the decoded address register data to select an individual drive line.

Transistor Q2A is turned on by coincidence of a 0-volt decoder input level and a -17-volt read pulse. The -17-volt pulse on the collector of Q2A saturates transistor Q4A. At the same time one bottom switch pair turns on if 0-volt level is present at decoder input C, and transistors Q1C and Q3C will saturate. Read current flows from ground through the top switch transistor (Q4A), a steering diode and selected drive line, and through the bottom switch transistor (Q3C) to the current source.

The write portion of the cycle is similar except that alternate transistors in the top and bottom switch pairs turn on and the write current is steered through the drive line in a direction opposite to the read current. Application of a decoder input A level and a write pulse turns on transistors Q1A and Q3A. The decoder C level and write pulse saturates Q2C and Q4C. Write current flows from ground, through Q4C and the selected drive line, a steering diode, and through Q3A to the current source.

NOTE

In all applications of the SS-32 PAC, pin 15 should be jumpered to pin 5 (ground) at the PAC connector.

SPECIFICATIONS

Frequency of Operation

Frequency of operation is determined by load impedance and the timing relationship between the address signals and the load currents. The SS-32 is used normally at repetition frequencies from 200 KC to 400 KC.

Input

The inputs are a -18 to 0-volt level at the decoder input and a +0.6 to -17-volt pulse at the read or write pulse input. The load on the address decoder circuit is 14 ma with the input at 0 volt (during read or write time) and less than 0.1 ma with the input at -18 volts.

The load on the read (or write) pulse input circuit is 70 ma when the input is at -17 volts and less than 0.1 ma with the input at +0.6 volts.

Output

The circuit will provide bipolar memory drive line currents of up to 300 ma and will tolerate load back voltages of 10 volts.

Circuit Delay (at 250 ma drive current)

The circuit delay is measured from the read or write pulse input to the output emitter follower current flow (decoder level input at 0 volt).

Turn on delay (10% of WP or RP to 10% of Q3 or Q4 emitter current):

0.15 μsec (typ)
0.30 μsec (max)

Turn off delay (90% of WP or RP to 90% of Q3 or Q4 emitter current):

0.10 μsec (typ)
0.20 μsec (max)

Output Current Waveform Characteristics

The output current waveform is determined by the current source input except for the 40 ma pedestal caused by the output emitter-follower stage.

Current Requirements

All Circuits off	One Top Switch Output Stage on, Rest off	One Bottom Switch Output Stage on, Rest off	Two Output Stages on. (One Top Switch and One Bottom Switch) Rest off
-18 V: <0.1 ma	8 ma	8 ma	17 ma
-12 V: 32 ma	43 ma	34 ma	35 ma

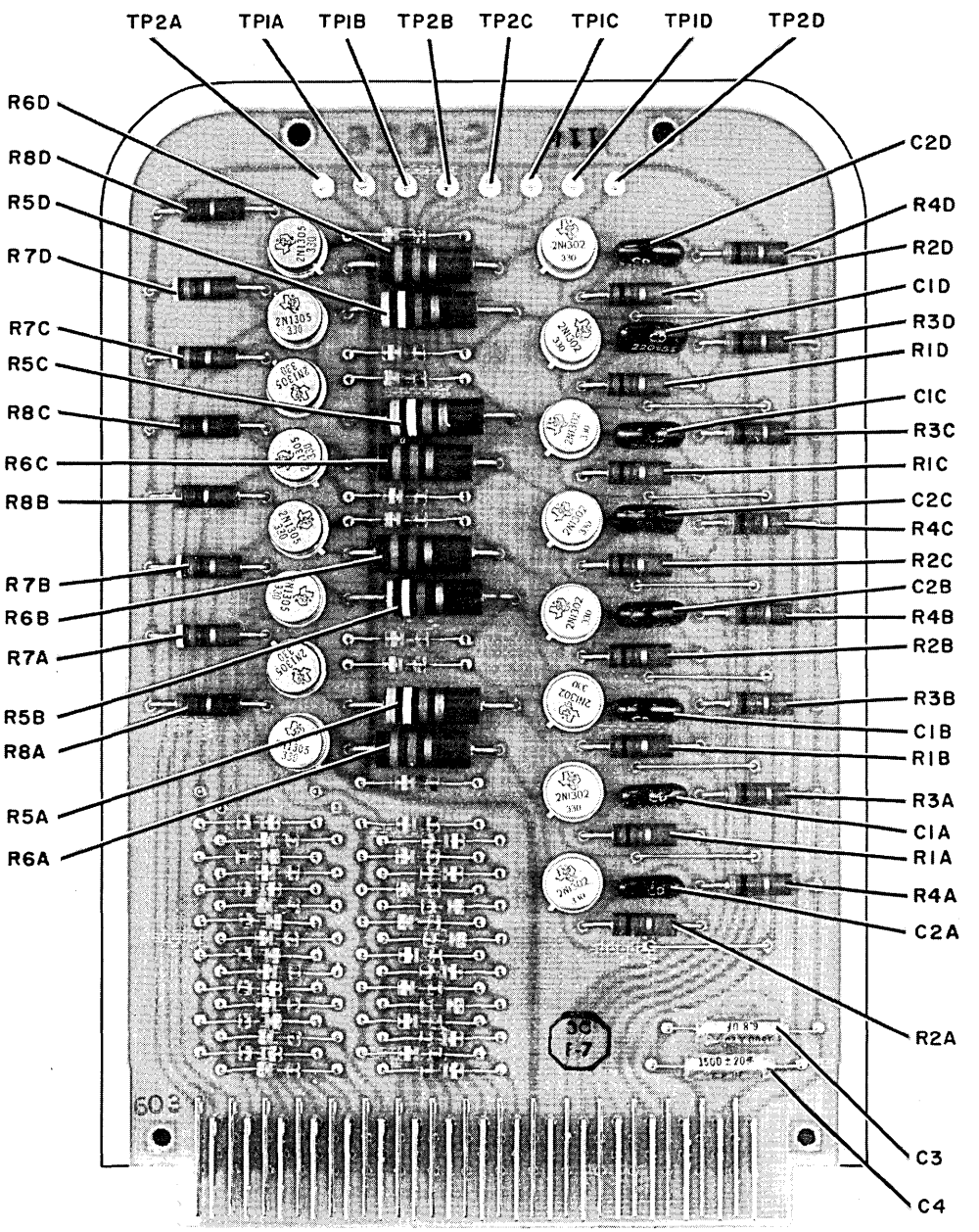


Figure 1. Selection Switch PAC, Model SS-32, Parts Location (Resistors, Capacitors and Test Points)

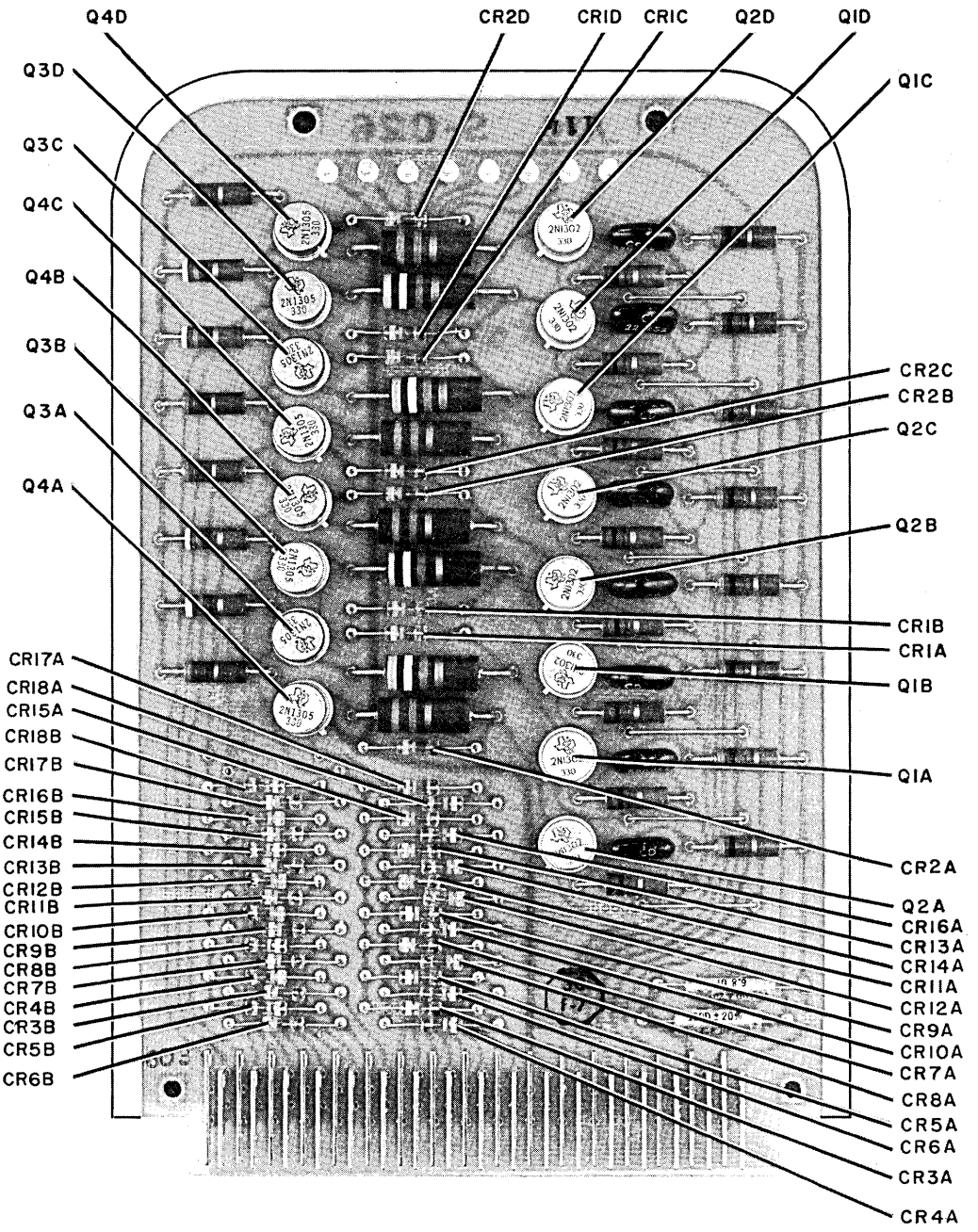
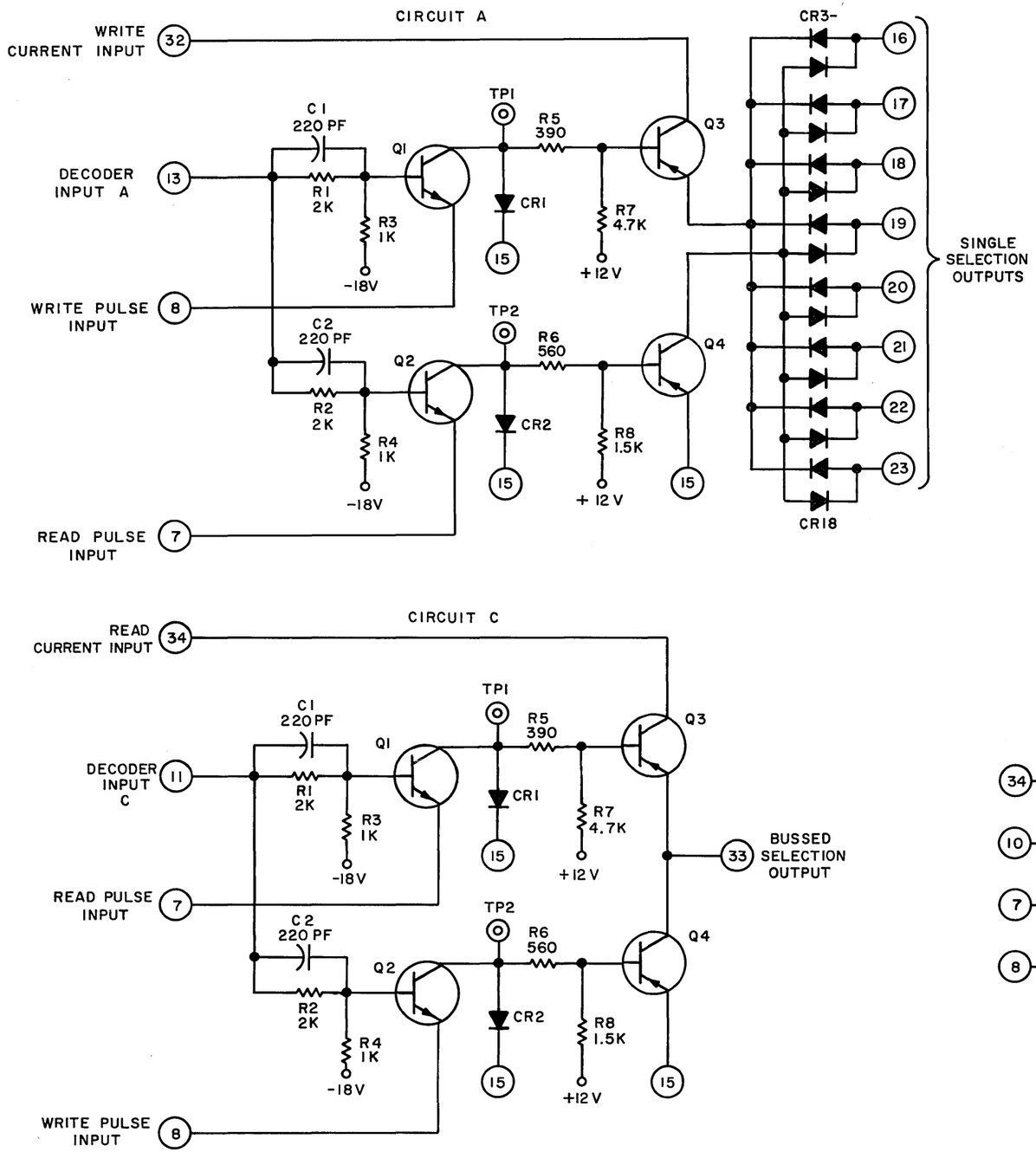
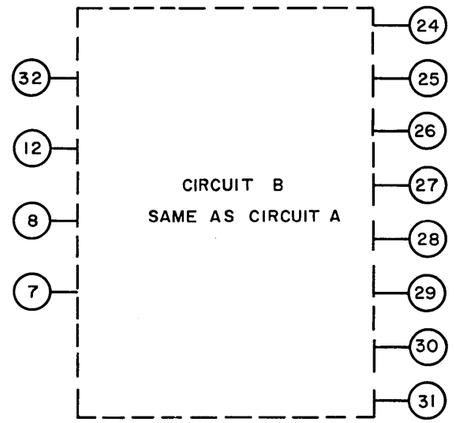


Figure 2. Selection Switch PAC, Model SS-32, Parts Location (Diodes and Transistors)





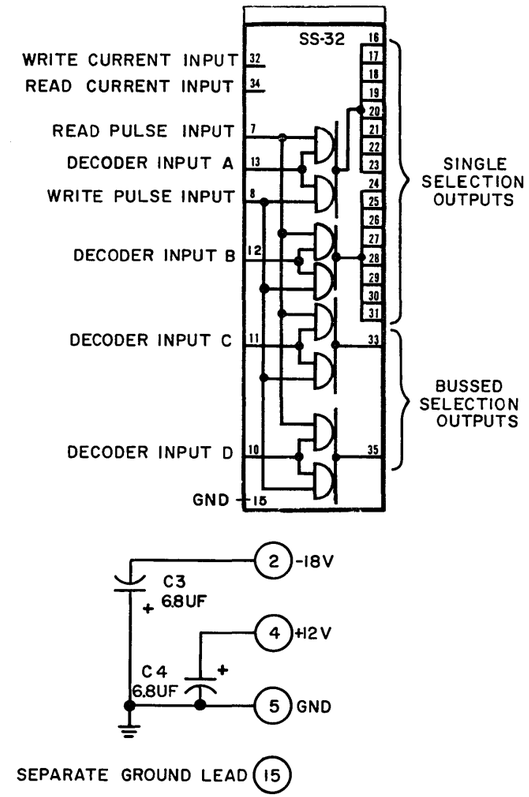


Figure 3. Selection Switch PAC, Model SS-32, Schematic and Logic Diagram

SELECTION SWITCH PAC, MODEL SS-32, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F — DESCRIPTION	3C DWG NO.
C1, C2	CAP, fxd, mica dielec: 220 pf ±5%, 100 VDC	930 011 135
C3, C4	CAP, fxd, elec TANTalum: 6.8 μf ±20%, 35 VDC	930 217 020
CR1-CR18	DIODE: Replacement type CTP462	943 001 001
R1, R2	RES, fxd, comp: 2 K ±5%, 1/2 W	932 004 056
R3, R4	RES, fxd, comp: 1 K ±5%, 1/2 W	932 004 049
R5	RES, fxd, comp: 390 ohms ±5%, 1 W	932 005 039
R6	RES, fxd, comp: 560 ohms ±5%, 1 W	932 005 043
R7	RES, fxd, comp: 4.7 K ±5%, 1/2 W	932 004 065
R8	RES, fxd, comp: 1.5 K ±5%, 1/2 W	932 004 053
Q1, Q2	TSTR: Replacement type 2N1302	943 550 001
Q3, Q4	TSTR: Replacement type 2N1305	943 537 002

TIMING DISTRIBUTOR PAC, MODEL S-219

GENERAL DESCRIPTION. The Timing Distributor PAC, model S-219 (Figures 1 and 2), provides accurately timed positive pulse sequences to drive S-PACs. The positive pulses are selected from a delay line. The S-219 contains a gated input pulse generator, a 4 μsec passive delay line, and six independent amplifiers. The input to each amplifier can be connected to taps on the delay line to provide output pulse sequences

CIRCUIT FUNCTION. Input negative logic signals activate a pair of AND gates (2-legged and 3-legged) which are buffered through an OR gate to the base of gating transistor Q6 (Figure 5). A logic ONE (-6V) at the base of Q6 turns it on which, in turn, sets flip-flop Q2 and Q3. The reset output from Q3 (a logical zero) will cause Q4 to cut-off and Q5 to start conduction. This causes a pulse to be sent down the 4-μsec delay line. The pulse width may be adjusted by selecting taps on the delay line Flip-flop reset is also dependent on the delay line tap. Values of delay from the delay line can be obtained from Table 1 and Figure 3. Each delay line tapped output can be amplified and inverted to provide an accurately timed, positive output pulse capable of driving five S-PAC unit loads. Input connection points for each amplifier are located on the PAC to facilitate jumper connections to delay line tap points (Figures 3 and 4). Amplifiers A and B have AND gate inputs that can be connected to any two separate points on the delay line. This will provide arbitrarily narrow output pulses. A typical jumper connection arrangement is illustrated in Figure 4.

SPECIFICATIONS

Input Loading

1/2 unit load (each gate)

Output

5 unit loads (each output)

Output Pulse Width

(max pulse width not to exceed 49% of the duty cycle) Adjustable from 0.1 to 1.0 μsec. Two of six channels can provide narrower pulses.

Maximum Operating, Frequency

500 KC

Input Delay

100 nsec, typical delay from input to first delay line tap

Power Requirements

Quiescent:

+12 V: 6 ma
- 6 V: 35 ma (rev,)
-18 V: 120 ma
Total power 1.2 W
Cycling at maximum rate:

65 ma

35 ma (rev.)

120 ma

Total power 1.75 W

TABLE 1

DELAY LINE TAP POINTS WITH
CORRESPONDING DELAY LINE DELAYS
(Refer to Figure 3)

Delay Line Jumper Connection NR	Delay Line Delay (ns ±3%)	Delay Line Jumper Connection NR	Delay Line Delay (ns ±3%)
1	0	32	2036
2	36	33	2107
3	107	34	2179
4	179	35	2250
5	250	36	2322
6	322	37	2393
7	393	38	2465
8	465	39	2536
9	536	40	2608
10	608	41	2679
11	679	42	2751
12	751	43	2822
13	822	44	2894
14	894	45	2965
15	965	46	3000
16	1000	47	3036
17	1036	48	3107
18	1107	49	3179
19	1179	50	3250
20	1250	51	3322
21	1322	52	3393
22	1393	53	3465
23	1465	54	3536
24	1536	55	3608
25	1608	56	3679
26	1679	57	3751
27	1751	58	3822
28	1822	59	3894
29	1894	60	3965
30	1965	61	4000
31	2000		

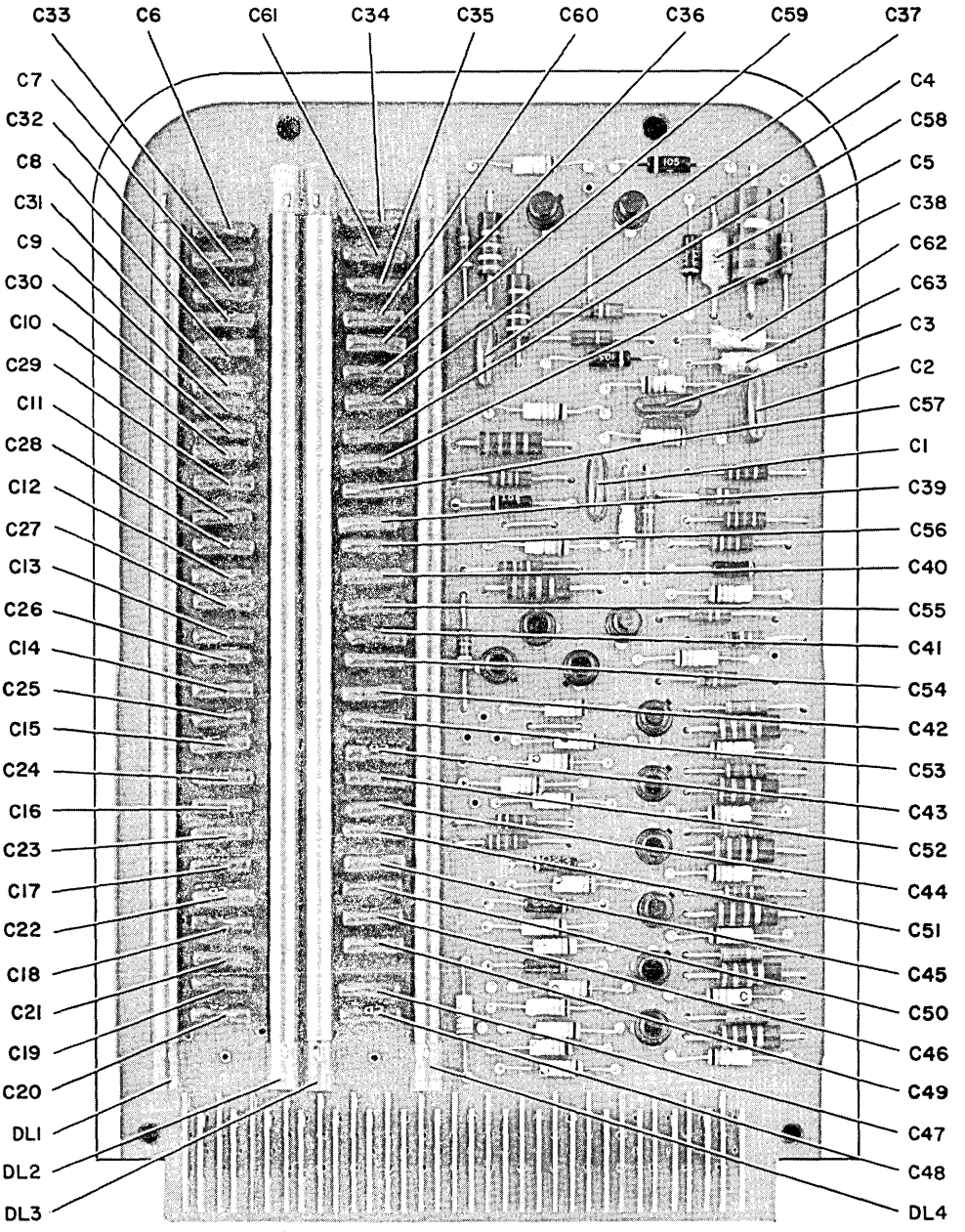


Figure 1. Timing Distributor PAC, Model S-219, Parts Location (Capacitors and Delay Lines)

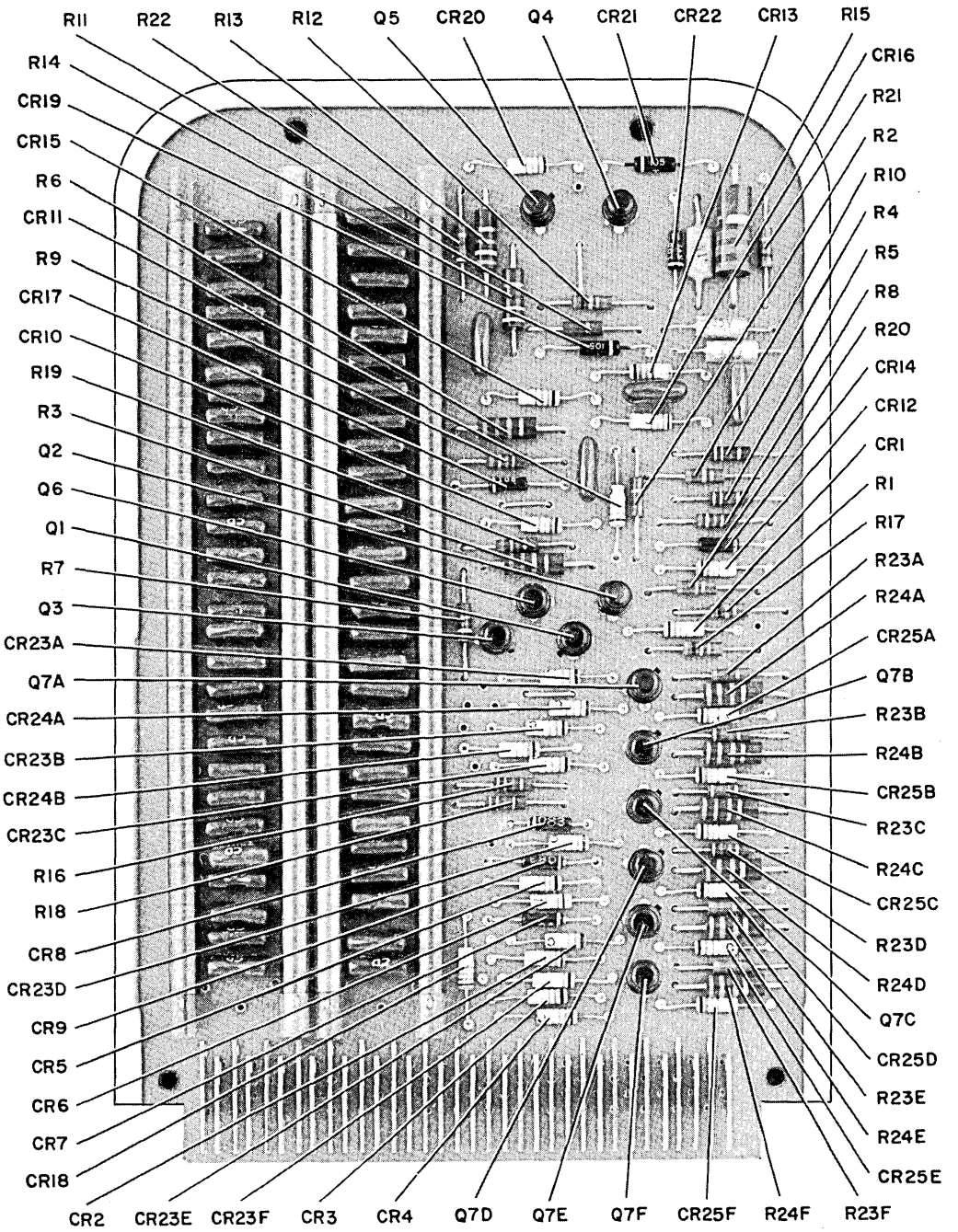


Figure 2. Timing Distributor PAC, Model S-219, Parts Location (Transistors, Diodes and Resistors)

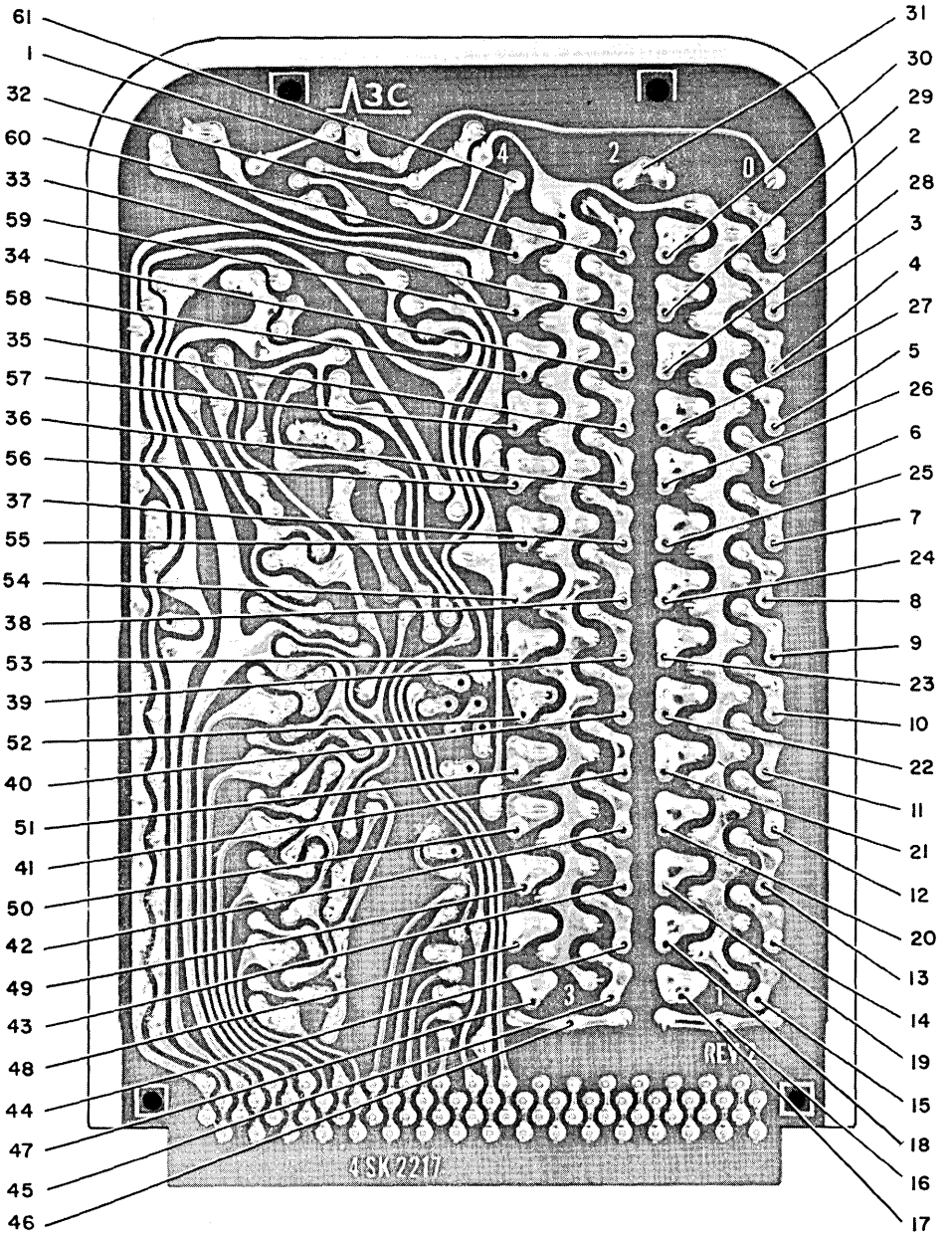


Figure 3. Timing Distributor PAC, Model S-219, Jumper Interconnection Diagram

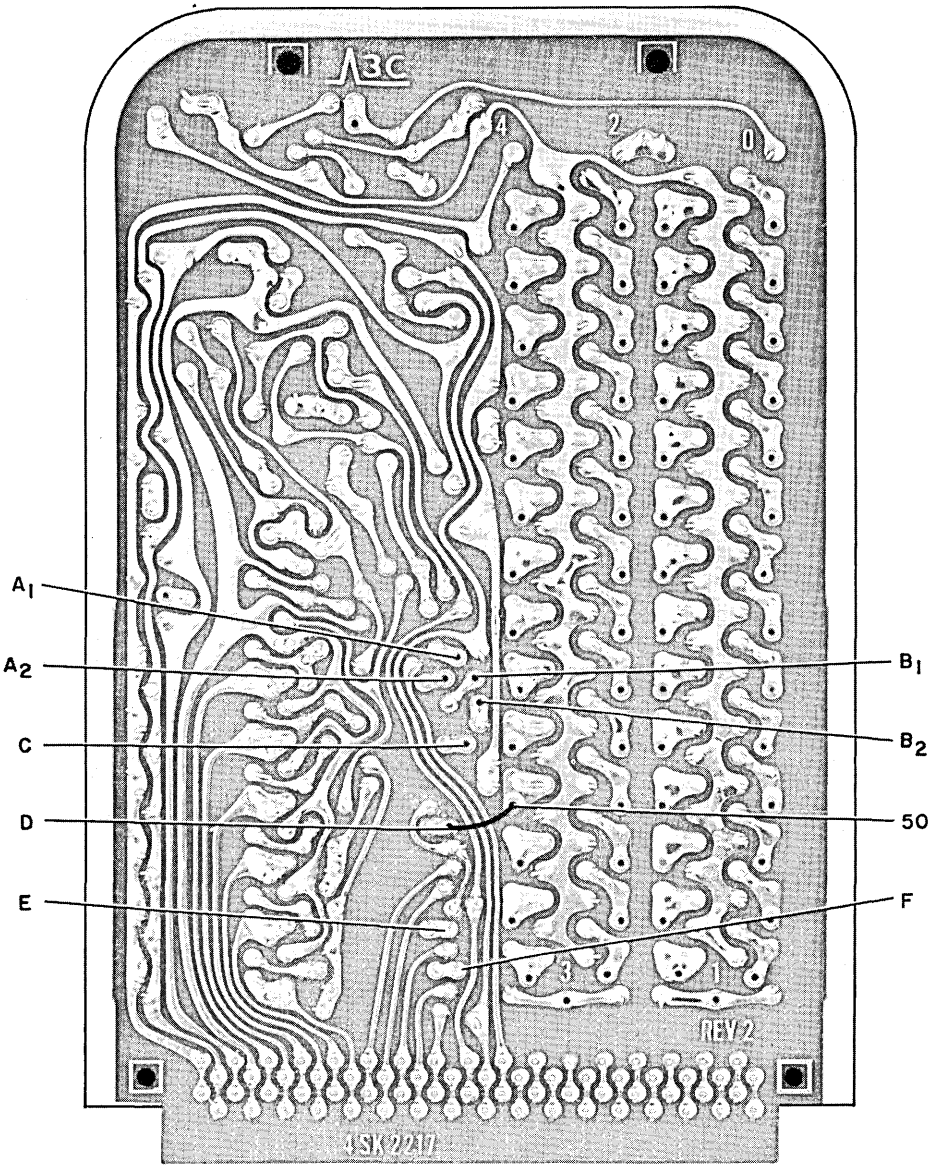


Figure 4. Timing Distributor PAC, Model S-219, Jumper Interconnection Diagram

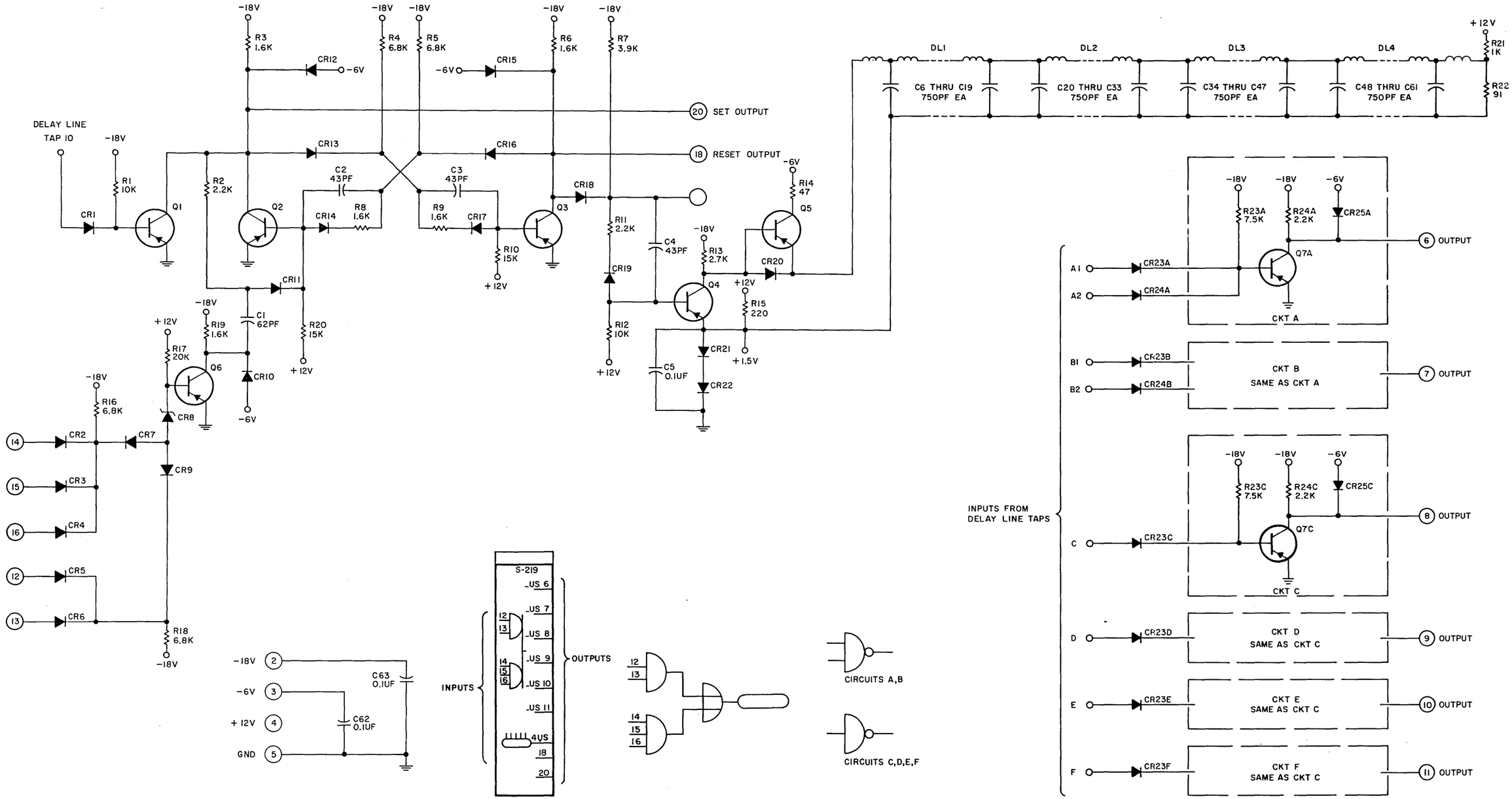


Figure 5. Timing Distributor PAC, Model S-219 Schematic and Logic Diagram

TIMING DISTRIBUTOR PAC, MODEL S-219, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
C1		CAP, fxd, mica dielec: 62 pf ±5%, 100 VDC	930 011 122
C2, C3, C4		CAP, fxd, mica dielec: 43 pf ±5%, 100 VDC	930 011 116
C5		CAP, fxd, ceramic dielec: 0.1 µf ±20%, 25 VDC	930 171 007
C6-C61		CAP, fxd, mica dielec: 750 pf ±2%, 100 VDC	930 001 001
C62, C63		CAP, fxd, plastic dielec: 0.1 µf ±20%, 35 VDC	930 217 009
CR1-CR6,		DIODE: Replacement Type 1N695	943 023 001
CR10-CR13,			
CR15-CR16,			
CR18-CR20,			
CR23A-			
CR23F,			
CR25A-			
CR25F			
CR7, CR9		DIODE:	943 083 001
CR8		DIODE: Replacement Type 1N702A	943 102 004
CR14, CR17,		DIODE: Replacement Type 1N816	943 105 001
CR19, CR21,			
CR22			
DL1-DL4		COIL, Delay Line	991 005 001
R1, R12		RES, fxd, comp: 10 K ±5%, 1/4 W	932 007 073
R2, R11		RES, fxd, comp: 2.2 K ±5%, 1/4 W	932 007 057
R3, R6		RES, fxd, comp: 1.6 K ±5%, 1/2 W	932 004 054
R4, R5, R16,		RES, fxd, comp: 6.8 K ±5%, 1/4 W	932 007 069
R18			
R7		RES, fxd, comp: 3.9 K ±5%, 1/4 W	932 007 063
R8, R9, R19		RES, fxd, comp: 1.6 K ±5%, 1/4 W	932 007 054

TIMING DISTRIBUTOR PAC, MODEL S-219, PARTS LIST (Cont)

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
R10, R20		RES, fxd, comp: 15 K ±5%, 1/4 W	932 007 077
R13		RES, fxd, comp: 2.7 K ±5%, 1/2 W	932 004 059
R14		RES, fxd, comp: 47 ohms ±5%, 1/2 W	932 004 017
R15		RES, fxd, comp: 220 ohms ±5%, 1 W	932 005 033
R17		RES, fxd, comp: 20 K ±5%, 1/4 W	932 007 080
R21		RES, fxd, comp: 1 K ±5%, 1/4 W	932 007 049
R22		RES, fxd, comp: 91 ohms ±5%, 1/4 W	932 007 024
R23A-R23F		RES, fxd, comp: 7.5 K ±5%, 1/4 W	932 007 070
R24A-R24F		RES, fxd, comp: 2.2 K ±5%, 1/2 W	932 004 057
Q1-Q7A-Q7F		TSTR: Replacement Type 2N965	943 543 004

INHIBIT COMPONENT BOARD

GENERAL DESCRIPTION

The Inhibit Component Board (Figures 1 and 2) contains the current-determining resistors and energy-storage capacitors used in the inhibit and clear processes. This board provides inhibit and clear currents for up to 12 inhibit windings. Bypass capacitors are provided to reduce voltage transients on the power supply. Table 1 provides the component values and reference designations for two inhibit board configurations.

CIRCUIT DESCRIPTION

In the inhibit process, current flows from ground to the Inhibit Component Board (Figure 3). It is passed through a precision resistor, an inhibit line, and another precision resistor to the -18-volt supply. The amplitude of the inhibit current is determined by the series resistance of the inhibit winding and two precision resistors.

During the memory clear process, current flows from ground to the Inhibit Component Board, through the inhibit line, and a precision resistor to the -18-volt supply. The amplitude of the clear current, determined by the series resistance of the inhibit winding and one precision resistor, is approximately equal to the sum of the X and Y drive line currents.

Provision is made on the board for additional resistors. The clear and inhibit currents through the memory-inhibit line can be reduced by shunting the inhibit winding with a resistor. This also serves to terminate the inhibit line and reduce transients. The currents through the inhibit line can be increased by shunting one of the precision resistors.

SPECIFICATIONS

Frequency of Operation

The frequency of operation is determined by the input currents.

Output Waveform Characteristics

The output waveform characteristics are determined by the input currents.

Current Requirements

Inhibit Process

-18 V: Nominal inhibit current of 270 ma
(270 ma) · N · K
where N = number of bits inhibited
(0 to 12 per board)
K = duty cycle (40% full cycle, 80% split cycle)

- 6 V: None

-12 V: None

Clear Process

-18 V: Nominal clear current of 600 ma
(600 ma) · N · K
where N = number of bits cleared
(0 to 12 per board)
K = duty cycle (10% max)

TABLE 1
COMPONENT VALUES AND REFERENCE DESIGNATIONS

Inhibit Board	Word Length	R1 3 W, 1%	R2 1/2 W, 5%	R3 3 W, 1%	R4 3 W, 1%
IB1	128 to 2048	40	100	50	40
IB2	4096	40	100	33	33

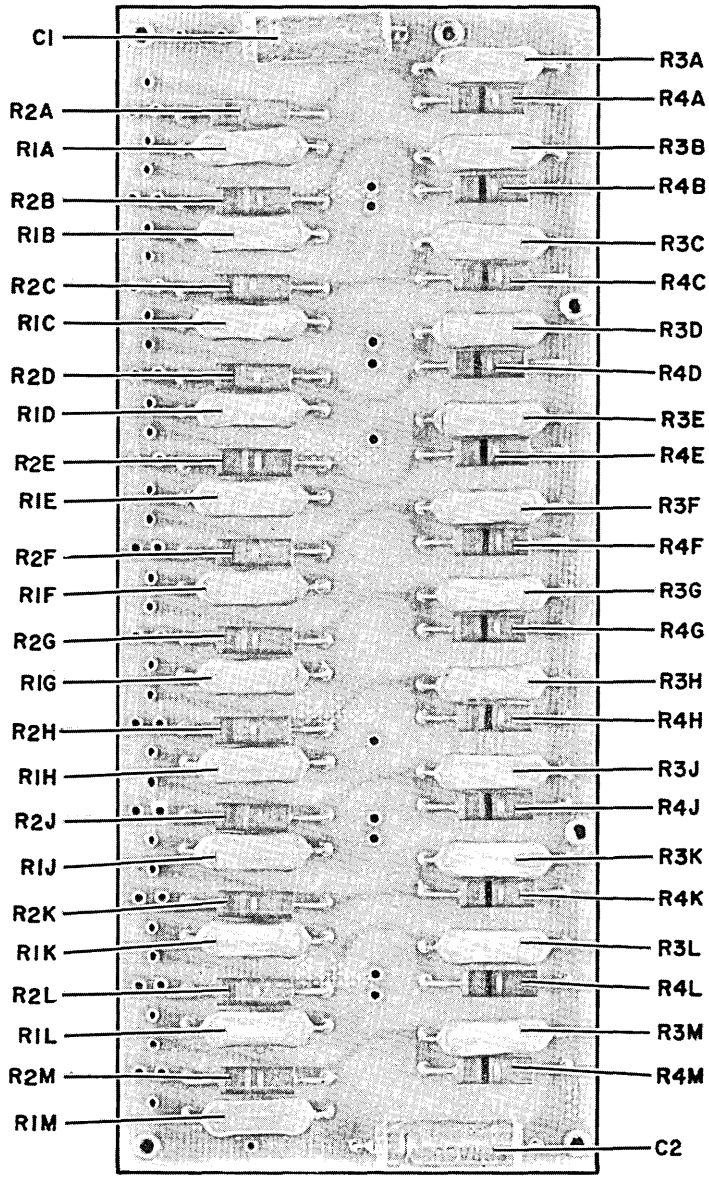


Figure 1. Inhibit Component Board, Model IB Parts Location
(Resistors and Capacitors)

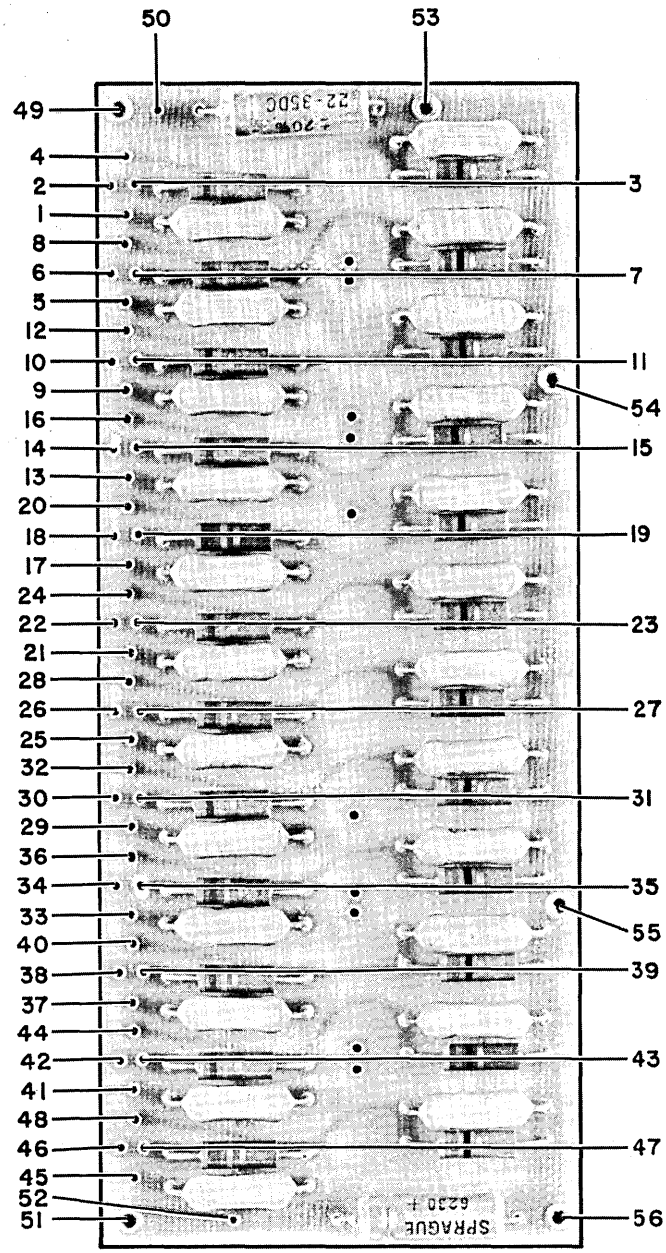


Figure 2. Inhibit Component Board, Model IB Parts Location
(Pin Connections)

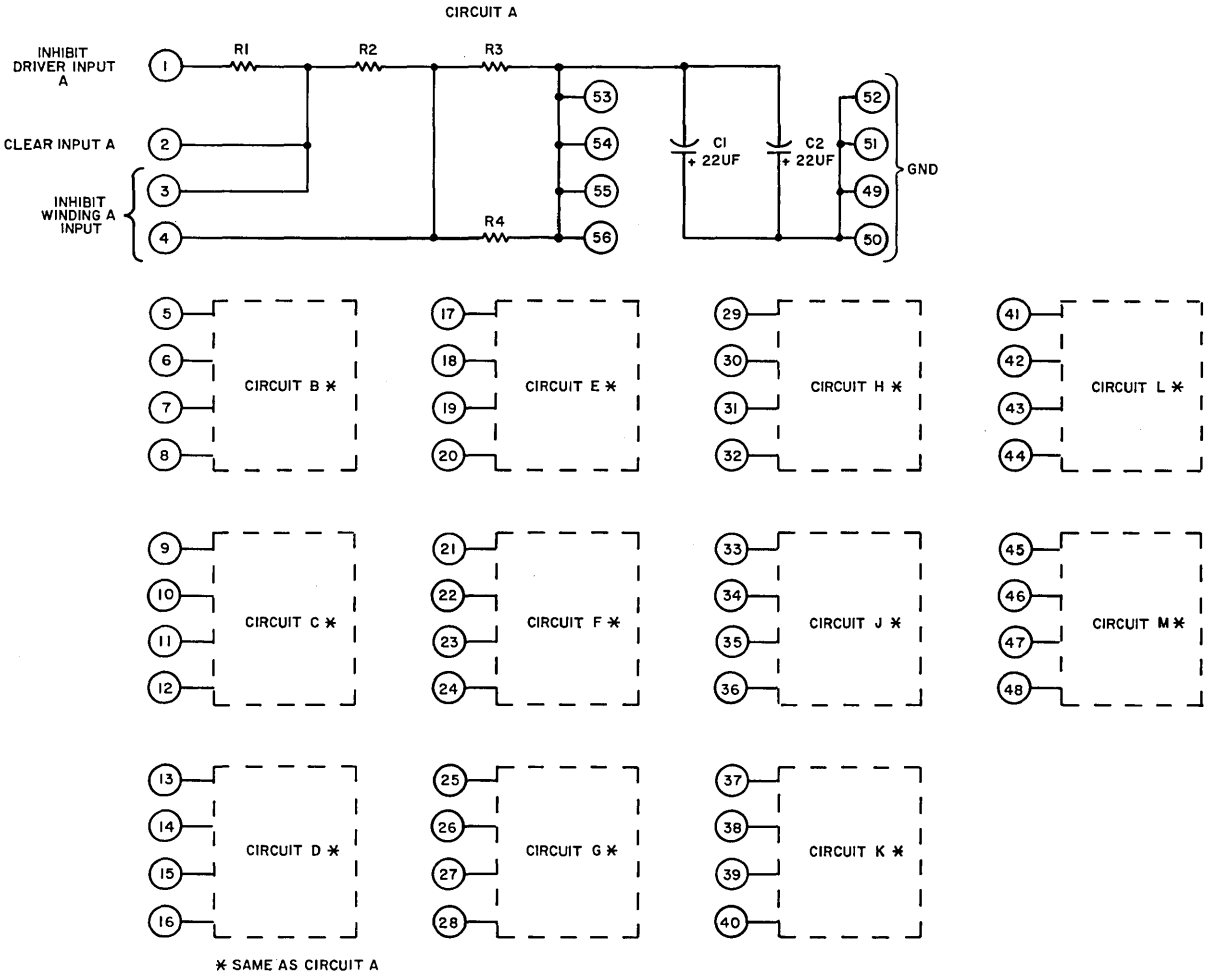


Figure 3. Inhibit Component Board, Model IB Schematic Diagram

INHIBIT COMPONENT BOARD, MODEL IB-1, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F — DESCRIPTION	3C DWG NO.
C1, C2	CAP, fxd, elec TANTalum: 22 μf ±20%, 35 VDC	930 217 023
R1, R4	RES, fxd, wire wound: 40 ohms ±1%, 3 W	932 206 410
R2	RES, fxd, comp: 100 ohms ±5%, 1/2 W	932 004 025
R3	RES, fxd, wire wound: 50 ohms ±1%, 3 W	932 206 411

INHIBIT COMPONENT BOARD, MODEL IB-2, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
C1, C2		CAP, fxd, elec TANTalum: 22 μf ±20%, 35 VDC	930 217 023
R1		RES, fxd, wire wound: 40 ohms ±1%, 3 W	932 206 410
R2		RES, fxd, comp: 100 ohms ±5%, 1/2 W	932 004 025
R3, R4		RES, fxd, wire wound: 33 ohms ±1%, 3 W	932 206 440

MEMORY NORMALIZER BOARD

GENERAL DESCRIPTION

The Memory Normalizer Board (Figure 1) contains a time delay circuit used to normalize control flip-flops in the memory system when power is turned on (initially condition the flip-flops to a proper state). It also has power supply bypass capacitors and a protection diode to keep the -6-volt supply from accidentally going more positive than ground.

CIRCUIT DESCRIPTION

The circuit (Figure 2) has a single form A relay contact and an RC delay in the coil circuit. The relay is normally open and permits a positive current source, clamped to ground, to be supplied to the output terminals. After a delay of approximately 0.1 second (in which time all supply voltages become stabilized), the relay contact closes and the voltage at the output terminals falls to -6 volts. This action frees the control flip-flops for normal operation.

SPECIFICATIONS

Input

DC supply voltage: +12 V, -6 V, -18 V (two)

Output

Ground or -6 volts, directed through diodes. The Memory Normalizer Board will drive 8 unit loads.

Power Requirements

-18 V: 48 ma

- 6 V: 5 ma (current from supply)

+12 V: 28 ma

Total Power (Static Dissipation)

1.1 W

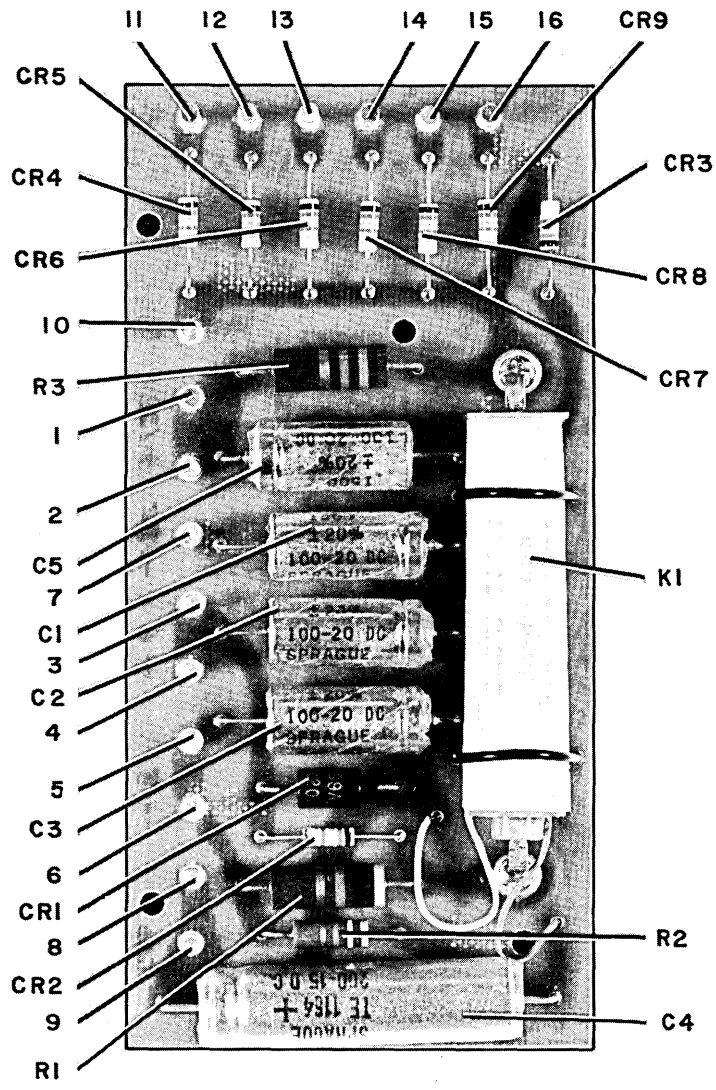


Figure 1. Memory Normalizer Board, Model MN-1, Parts Location

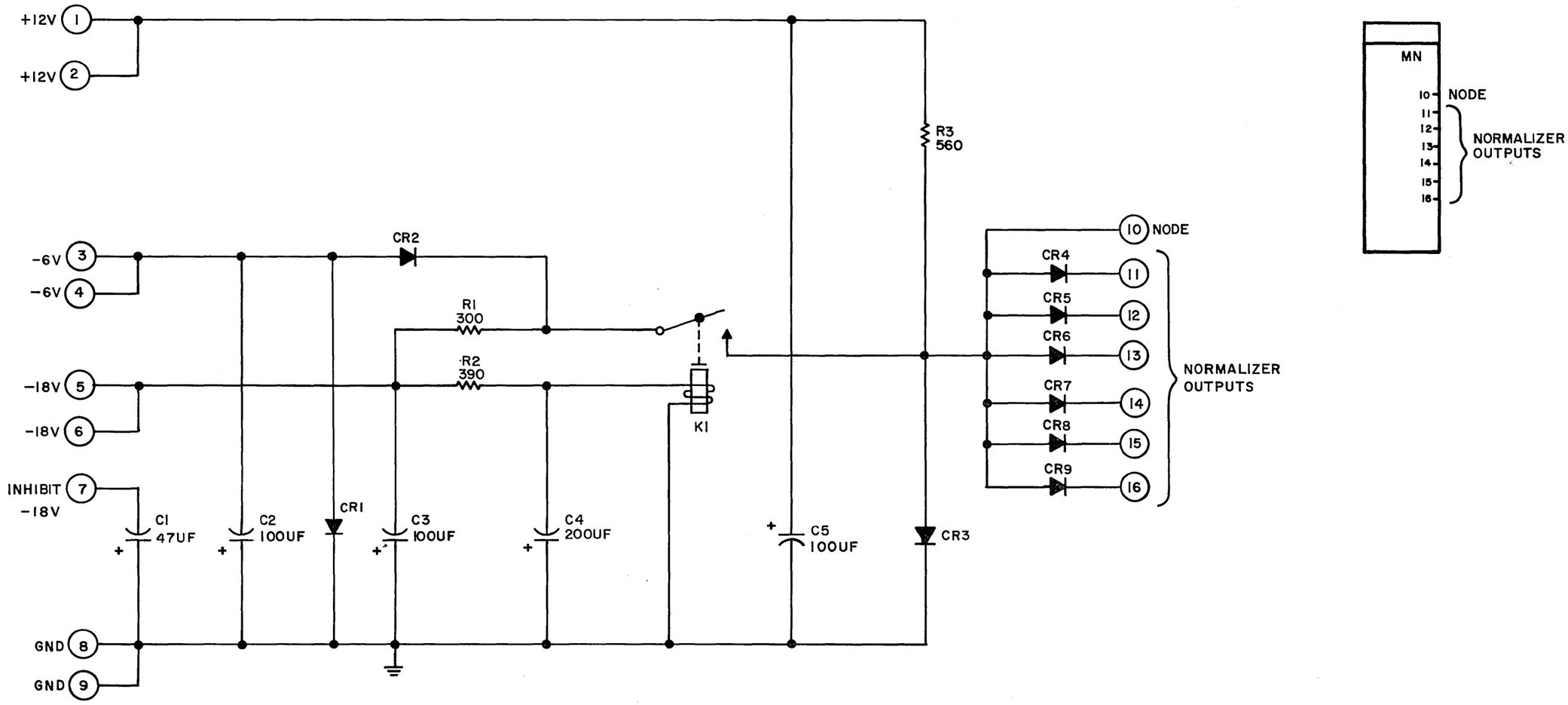


Figure 2. Memory Normalizer Board, Model MN-1, Schematic and Logic Diagram

MEMORY NORMALIZER BOARD, MODEL MN-1, PARTS LIST

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
C1		CAP, fxd, elec TANTalum: 47 µf ±20%, 20 VDC	930 217 025
C2, C3, C5		CAP, fxd, elec TANTalum: 100 µf ±20%, 20 VDC	930 216 027
C4		CAP, fxd, elec TANTalum: 200 µf ±20%, 15 VDC	930 220 317
CR1		DIODE: Replacement type 1N2069	943 303 001
CR2-CR9		DIODE: Replacement type 1N695	943 023 001
K1		RELAY: Replacement type CRZ1056	963 002 001
R1		RES, fxd, comp: 300 ohms ±5%, 1 W	932 005 036
R2		RES, fxd, comp: 390 ohms ±5%, 1/2 W	932 004 039
R3		RES, fxd, comp: 560 ohms ±5%, 1 W	932 005 043

MEMORY CLEAR DRIVER PAC, MODEL S-103

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
C1		CAP, fxd, mica dielec: 1000 pf ±5%, 100 VDC	930 011 153
C2, C5		CAP, fxd, ceramic dielec: 0.01 µf GMV, 75 VDC	930 156 001
C3		CAP, fxd, mica dielec: 91 pf ±5%, 100 VDC	930 011 126
C4, C6		CAP, fxd, plastic dielec: 6800 pf ±10%, 100 VDC	930 307 227
C7		CAP, fxd, mica dielec: 680 pf ±5%, 100 VDC	930 011 149
C8		CAP, fxd, mica dielec: 820 pf ±5%, 100 VDC	930 006 151
C9		CAP, fxd, plastic dielec: 0.1 µf ±10%, 100 VDC	930 307 239
C10		CAP, fxd, ELECTrolytic: 22 µf ±20%, 35 VDC	930 217 023
C11, C12		CAP, fxd, ELECTrolytic: 2.2 µf ±20%, 20 VDC	930 216 017
CR1, CR2, CR4,		DIODE: Replacement Type 1N695	943 023 001
CR5, CR8, CR9,			
CR11-CR15,			
CR17			
CR3, CR6, CR7		DIODE: Replacement Type 1N816	943 105 001
CR16			
CR10		DIODE: Replacement Type 1N705	943 102 002
CR18-CR23		DIODE: Replacement Type 1N2069	943 303 001
R1, R8, R13		RES, fxd, comp: 8.2 K ±5%, 1/2 W	932 004 071
R2		RES, fxd, comp: 2.7 K ±5%, 1/2 W	932 004 059
R3		RES, fxd, comp: 30 K ±5%, 1/2 W	932 004 084
R4		RES, fxd, comp: 16 K ±5%, 1/2 W	932 004 078
R5		RES, fxd, comp: 750 ohms ±5%, 1/2 W	932 004 046
R6		RES, fxd, comp: 18 K ±5%, 1/2 W	932 004 079
R7, R17		RES, fxd, comp: 6.8 K ±5%, 1/2 W	932 004 069
R9		RES, fxd, film: 4.02 K ±2%, 1/2 W	932 103 230
R10		RES, fxd, comp: 220 K ±5%, 1/2 W	932 004 105
R11		RES, fxd, comp: 200 K ±5%, 1/2 W	932 004 104
R12		RES, fxd, comp: 10 K ±5%, 1/2 W	932 004 073

MEMORY CLEAR DRIVER PAC, MODEL S-103 (Cont)

REF. DESIG.	ASSY LEVEL A B C D E F	DESCRIPTION	3C DWG NO.
R14		RES, fxd, comp: 3.9 K ±5%, 1/2 W	932 004 063
R15		RES, fxd, comp: 1.3 K ±5%, 1/2 W	932 004 052
R16		RES, fxd, comp: 20 K ±5%, 1/2 W	932 004 080
R18		RES, fxd, comp: 470 ohms ±5%, 1/2 W	932 004 041
R19		RES, fxd, comp: 36 K ±5%, 1/2 W	932 004 086
R20, R22		RES, fxd, comp: 1 K ±5%, 1/2 W	932 004 049
R21		RES, fxd, comp: 27 ohms ±5%, 1 W	932 005 011
Q1-Q3		TSTR: Replacement Type 2N404A	943 519 002
Q4		TSTR: Replacement Type 2N388	943 507 001
Q5		TSTR: Replacement Type CRP-1732A	943 522 001

MEMORY CLEAR DRIVER PAC, MODEL S-103

GENERAL DESCRIPTION. The Memory Clear Driver PAC, model S-103, (Figures 1 and 2) contains a monostable multivibrator, a pulse amplifier, and four identical output stages. The PAC can provide up to 500 ma of clear current to each of 24 inhibit windings in a magnetic core memory system. The clear current provided by the PAC resets all cores to the ZERO state.

CIRCUIT FUNCTION. The Memory Clear Driver PAC (Figure 3) functions quiescently with Q2 on and Q1, Q3, Q4, and Q5 off. The application of a positive input pulse triggers the multivibrator which turns off Q2 and turns on Q1, Q3, Q4, and Q5. The negative pulse produced at the assertion output turns on the NAND gate (Q3). The positive pulse at the collector of Q3 turns on the Q4 transistors, which in turn saturate the Q5 output transistors.

SPECIFICATIONS

Frequency of Operation

The maximum operating frequency is 5 KC. A memory clear pulse must not be applied during the normal memory cycle. After a clear pulse is applied, no other pulses should be applied to the system for 200 μsec. This precaution will provide the required recovery time for the power supply. Not more than 20 clear pulses should be applied in any 10-msec period.

Input

The input to the multivibrator is a -6-volt to 0-volt pulse with a maximum rise time of 1 μsec. The trigger input must remain positive at least 1.5 μsec and must be negative for at least 200 μsec prior to triggering action. The input loading is 2 W-loads.

Output

The multivibrator pulse width is nominally 30 μsec. The assertion output will drive 2 W-loads, and the negation will drive 4 W-loads. Each clear output can provide up to 500 ma of clear current to a memory inhibit winding. The output transistors will tolerate an inductive back voltage of 50 volts.

Multivibrator Output Characteristics

a. Assertion output (negative pulse measured from -0.6 volt to -4.5 volts).

Rise time: 1.0 μsec or 0.2 percent of pulse width, whichever is longer.

Fall time: 0.8 μsec (typ)

b. Negation output.

Rise time: 0.5 μsec (typ).

Fall time: 0.8 μsec (typ).

Circuit Delay

(Measured at 10% of voltage input to 10% of output current)

0.5 μsec (typ)
1.0 μsec (max)

Output Current Waveform Characteristics

Rise time: 10% to 90%

4 μsec (typ)
5 μsec (max)

Fall time: 90% to 10%

10 μsec (typ)
15 μsec (max)

Power Requirements

Quiescent condition: 18 V

-18 V: 23 ma
+12 V: 1 ma
- 6 V: 6 ma (clamp current from power supply)

Output stage on (duty cycle less than 20%)

-18 V: 24 ma (not including the 12 amperes of current supplied at the inhibit component board)
+12 V: 120 ma
- 6 V: 864 ma (current into power supply)

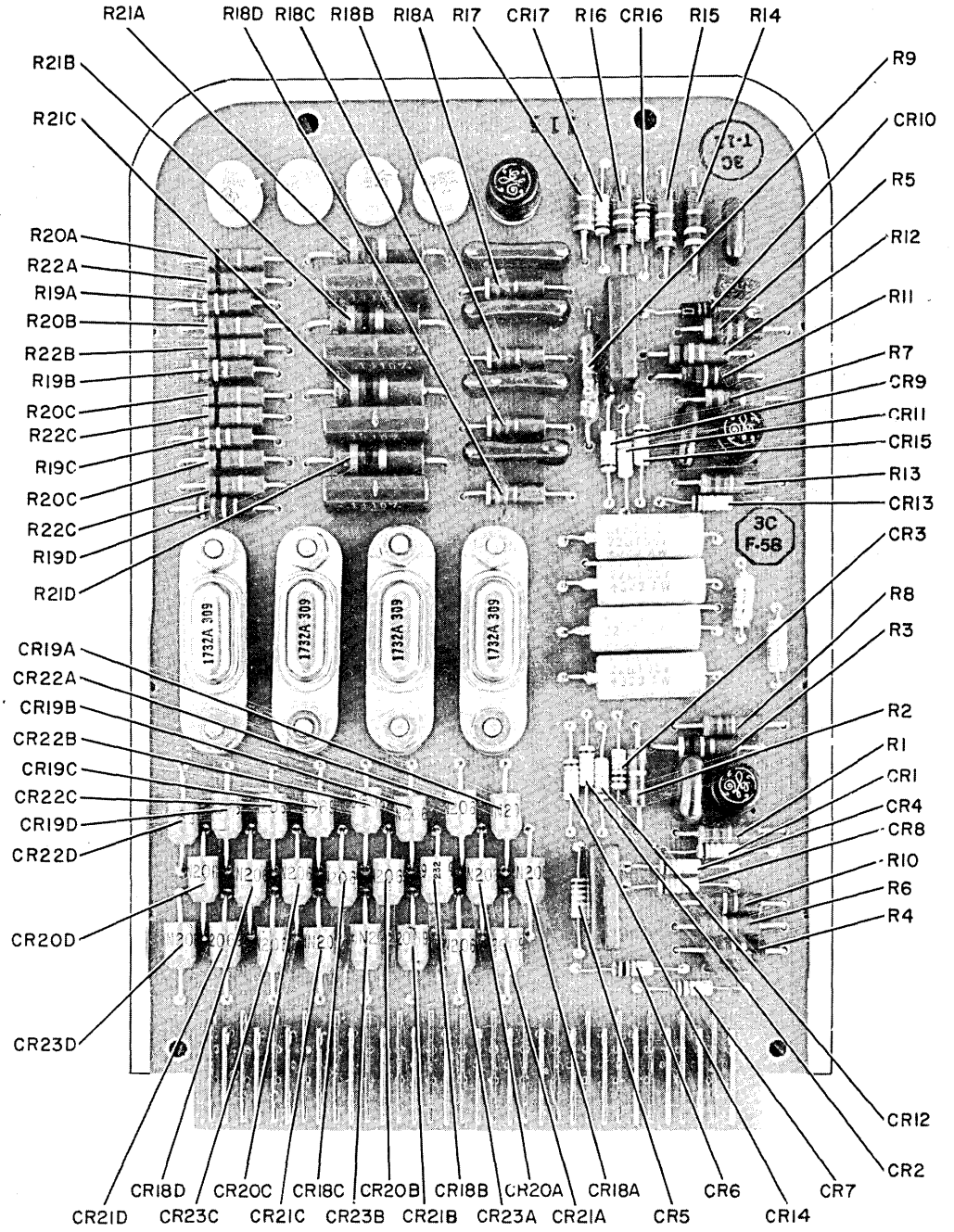


Figure 1. Memory Clear Driver PAC, Model S-103, Parts Location (Diodes and Resistors)

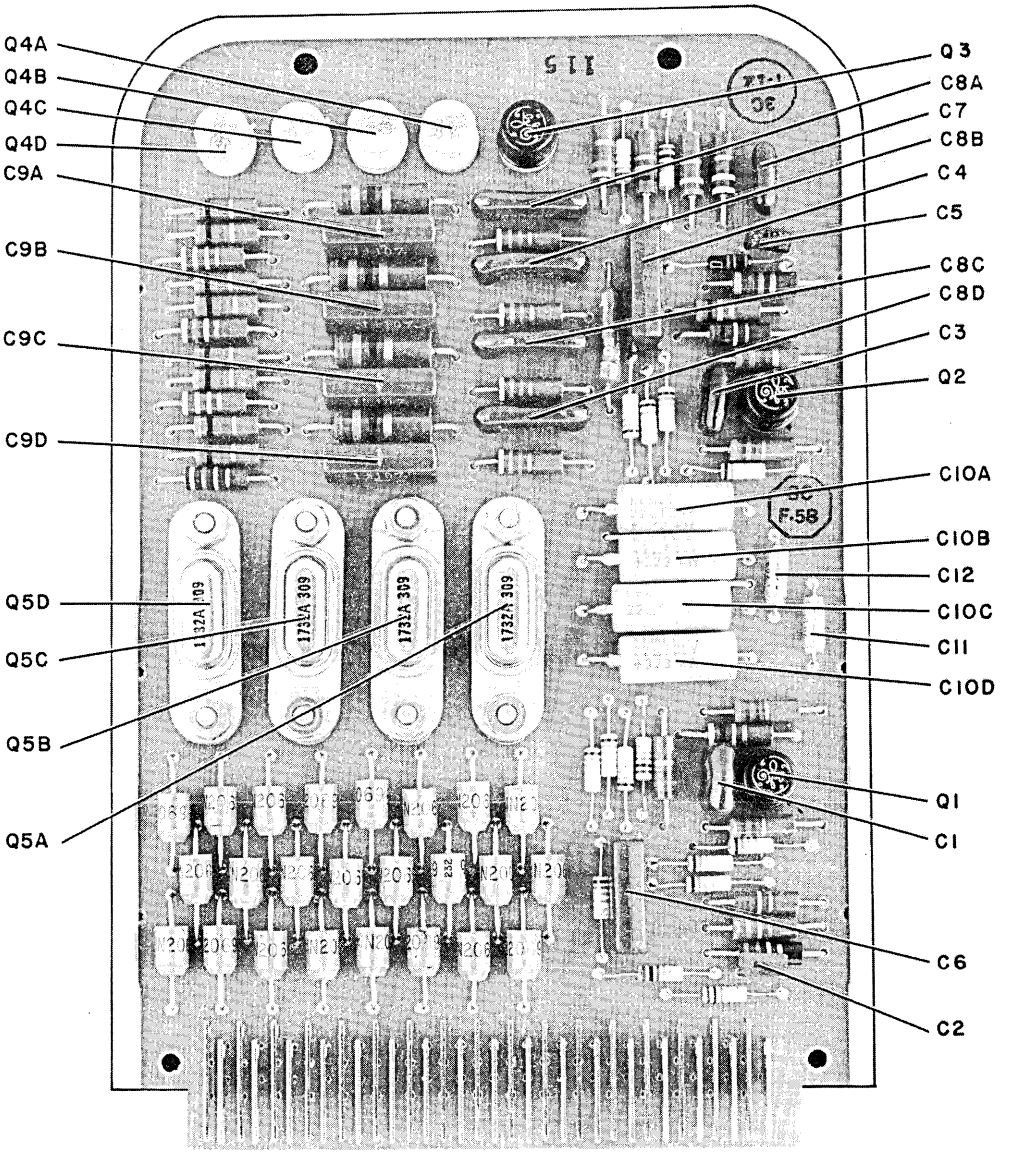


Figure 2. Memory Clear Driver PAC, Model S-103, Parts Location (Transistors and Capacitors)

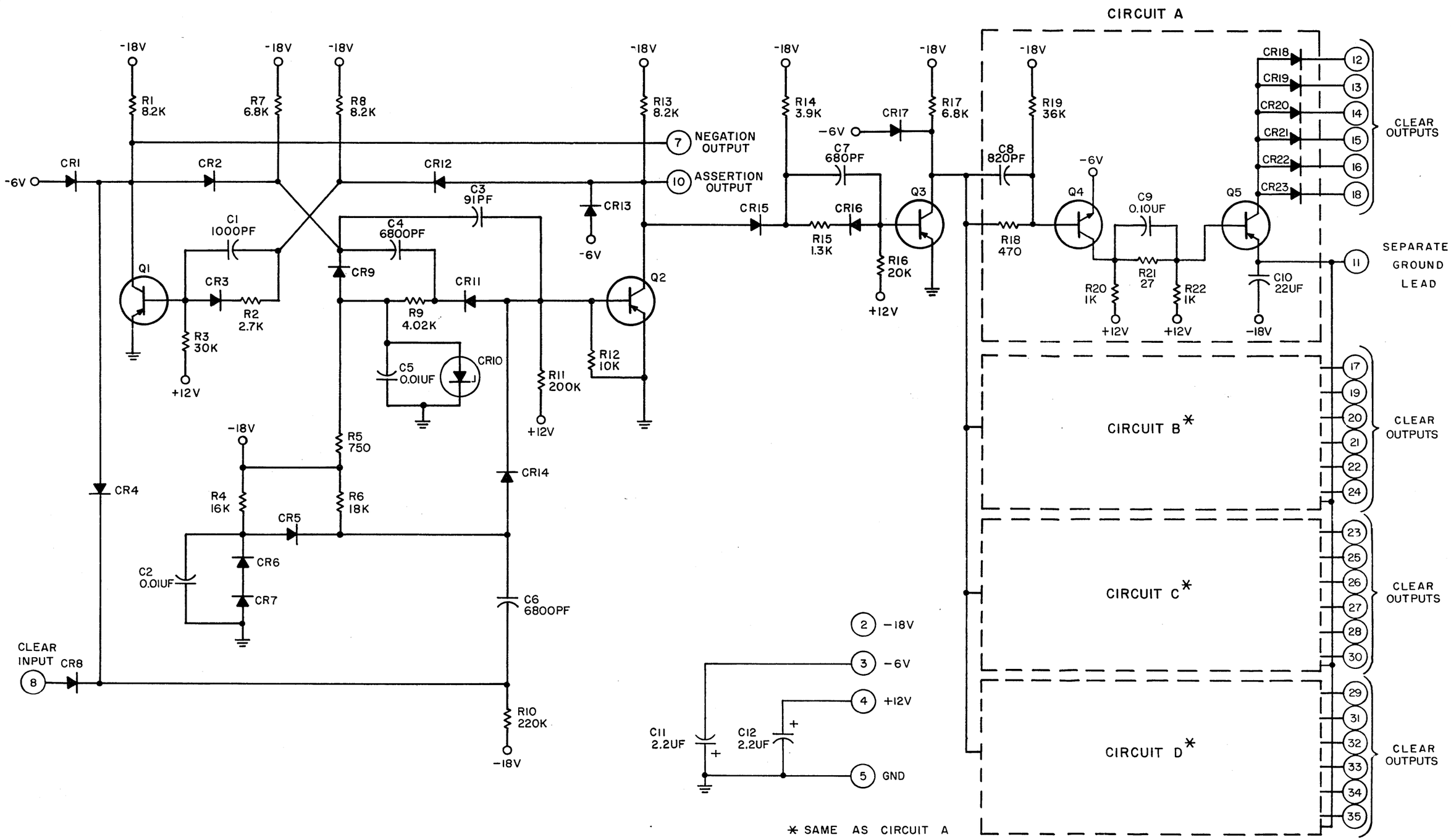


Figure 3. Memory Clear Driver PAC, Model S-103, Schematic Diagram

TRANSFER GATE PAC, MODEL S-169

GENERAL DESCRIPTION. The Transfer Gate PAC, Model S-169, Figures 1 and 2, contains 12 identical 2-input NAND gates. The PAC is designed to perform parallel loading of registers with a minimum of logic and external connections.

CIRCUIT FUNCTION. The Transfer Gate PAC contains 12 NAND gates, Figure 3, arranged in four groups. There is one 2-gate, two 3-gate, and one 4-gate group. Each group of gates has one common prewired input and one free input to each gate. The NAND gate circuits are standard; if both inputs are a ONE (-6 V), the output is a ZERO (0 V). If either input goes to ZERO, the output becomes a ONE.

The common inputs can be externally connected to transfer a maximum of 12 bits of data simultaneously. With this arrangement, the data to be transferred is connected to the individual input of each gate and a strobe input is applied to the common input. Additional S-169 PACs may be used to expand the data bit transfer.

SPECIFICATIONS.

Input Loading

Individual inputs: 1 unit load per circuit
Common inputs: 1 unit load per gate

Circuit Delay (measures at -3 V averaged over two stages)

0.1 μsec (max)
0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance

Total Power

2.2 W

Polarization

None

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Current Requirements

-18 V: 120 ma
- 6 V: 63 ma (reverse current into supply)
+12 V: 8 ma

Handle Color Code

None

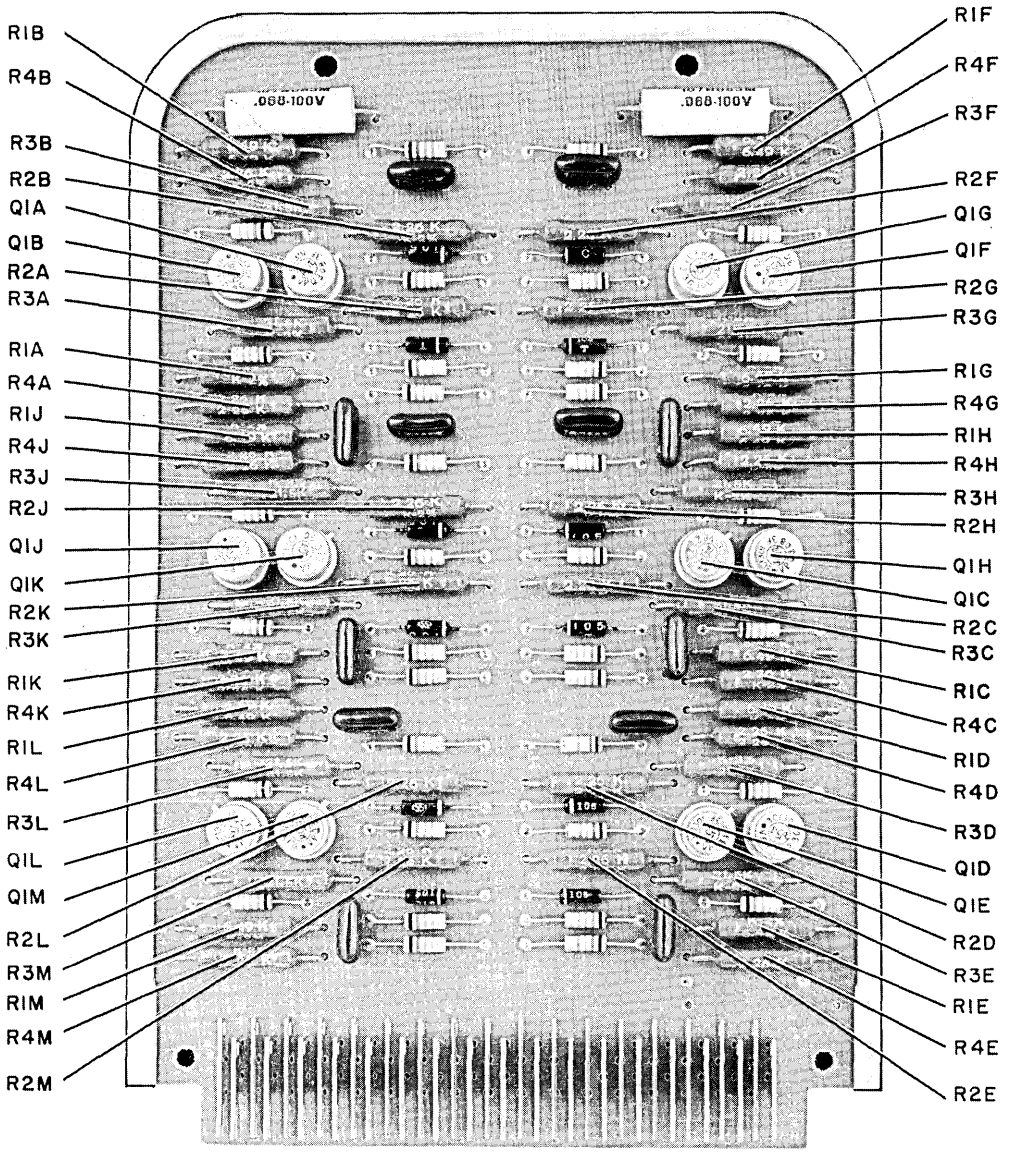


Figure 1. Transfer Gate PAC, Model S-169, Parts Location (Resistors and Transistors)

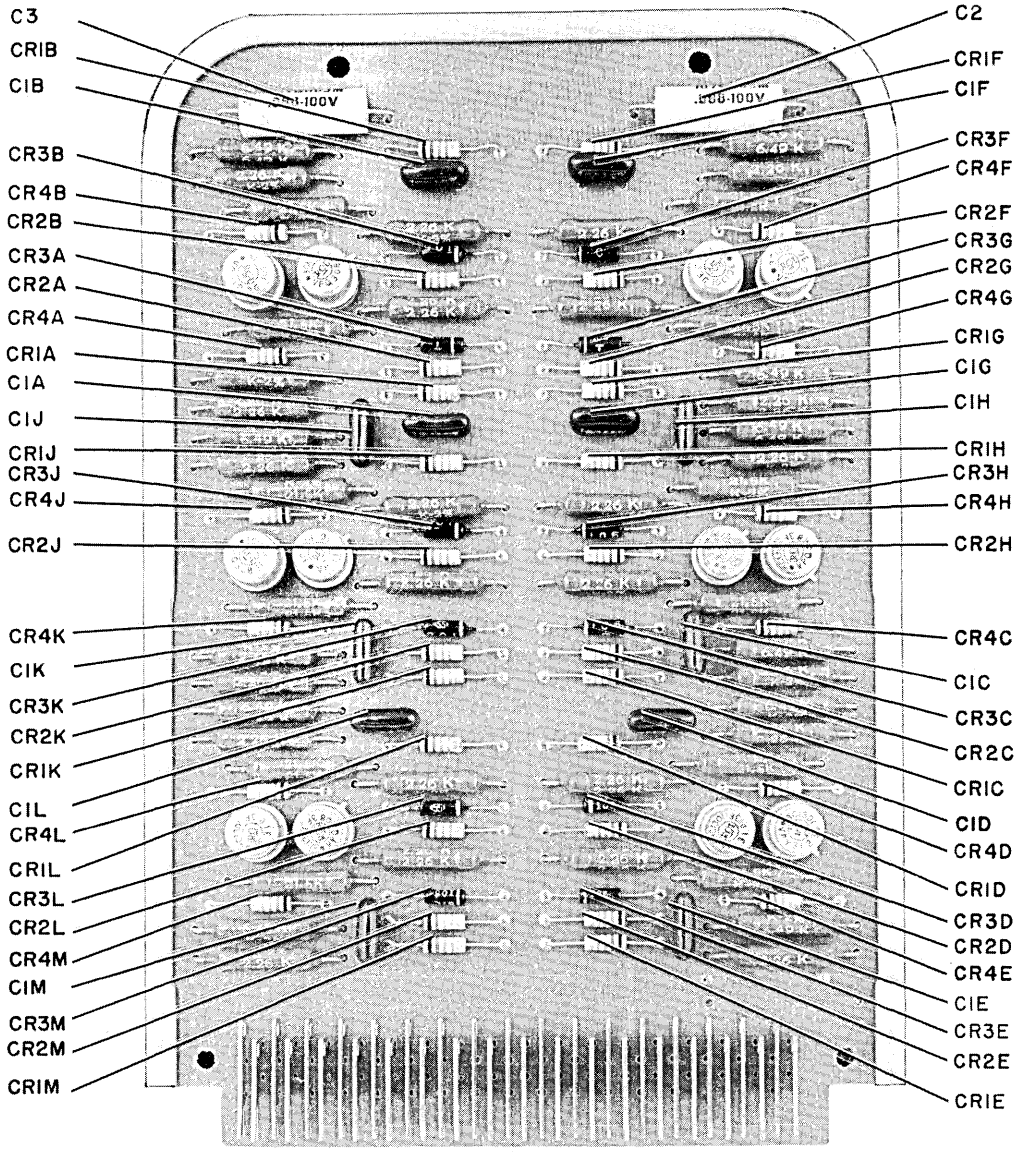
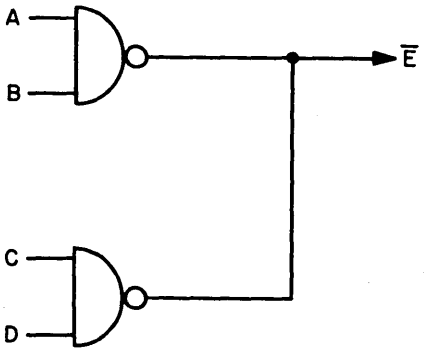


Figure 2. Transfer Gate PAC, Model S-169, Parts Location (Capacitors and Diodes)

PARALLEL TRANSFER GATE PAC, MODEL S-179

GENERAL DESCRIPTION. The Parallel Transfer Gate PAC, Model S-179 (Figures 1 and 2), contains twelve 2-input NAND gates without collector resistors and clamp diodes; one 2-gate, two 3-gate, and one 4-gate group. These circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability (fanout). The gates operate with levels, pulses, or with a combination of both. The PAC is designed to perform a variety of functions which includes multiplexing of parallel groups of bits; parity generation; decoding; and etc. These functions are performed with groups of NAND gates connected in parallel.

NAND gates with parallel collectors perform logic functions as follows:

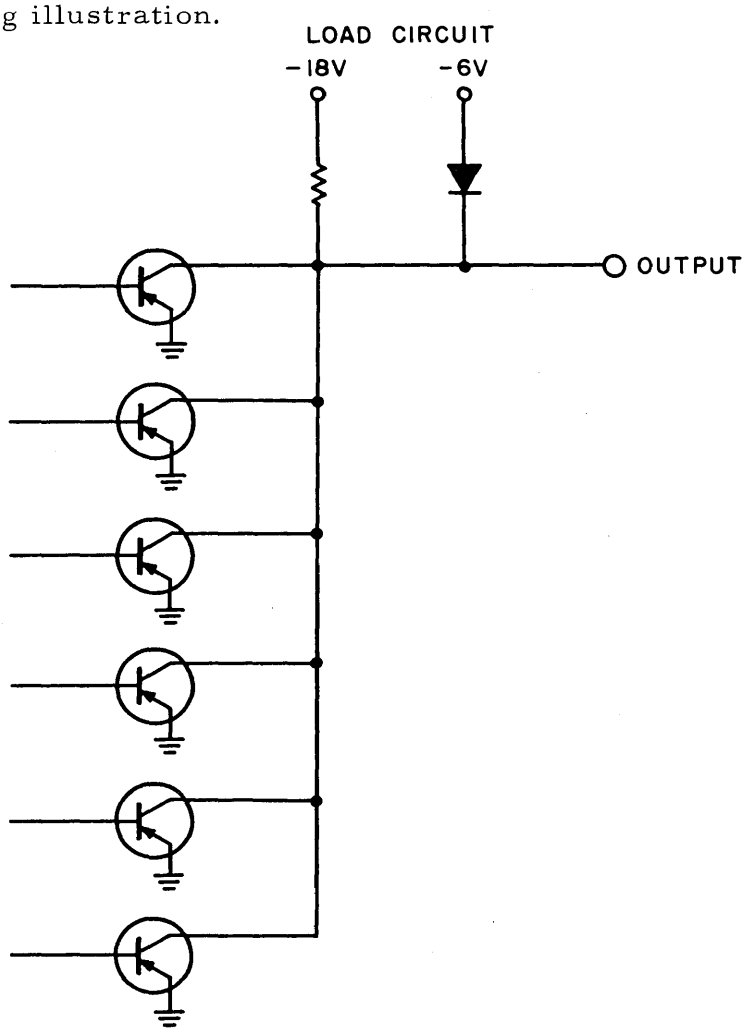


$$\overline{E} = AB \vee CD$$

CIRCUIT FUNCTION. The Parallel Transfer Gate PAC contains twelve NAND gates (Figure 3), arranged in four groups, and one load circuit. Each group has one common, pre-wired input and one free input to each gate. The NAND gate circuits are standard with the exception of the common load circuit; if both inputs are a ONE (-6 V), the output is a ZERO (0–V). If either input goes to ZERO, the output becomes a ONE.

The load circuit contains a pull-up resistor (to -18V) and a clamp diode (to -6 V). Each gate or group of gates used on the PAC must have the load circuit or a similar circuit connected to the output. The load circuit connected to the output of the parallel gate groups does not affect the fanout. If the inputs are such that only one transistor is conducting, the

output will be at zero volt. The maximum drive capability, regardless of how many collector outputs are jumpered in parallel, is 7 unit loads as shown in the following illustration.



The common inputs can be externally connected to transfer a maximum of twelve bits of data simultaneously. With this arrangement, the data to be transferred is connected to the free input of each gate and a strobe input is applied to the common input. Additional S-179 PACs may be used to expand the data bit transfer.

SPECIFICATIONS

Input Loading

Free inputs; 1 unit load per circuit
Common inputs: 1 unit load per gate

Circuit Delay (measured at -3 V averaged over two stages)

0.1 μsec (max)
0.06 μsec (typ)

Output Drive Capability

7 unit loads and 400 pf stray capacitance

Frequency of Operation

DC to 1 MC (max)

Output Waveform Characteristics

Rise time: 0.1 μsec (typ)
Fall time: 0.15 μsec (typ)

Current Requirements

-18 V: 35 ma
- 6 V: 0 ma
+12 V: 8 ma