PARALLEL INPUT/OUTPUT
DIRECT MEMORY ACCESS

CGC 7900 SERIES
COLOR GRAPHIC COMPUTERS

CHROMATICS

CGC 7900
Parallel Input/Output
Direct Memory Access

User's Manual

March 25, 1982

DOCUMENT NUMBER 070205
PUBLICATION DATE 1/82

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PREFACE - The purpose of this document is to define the CGC 7900'S Parallel Input/Output, Direct Memory Access Circuit board (PIO/DMA). It describes the overall attributes of the board as well as goes into detail about the operation and design of the board.

1-1 PIO/DMA GENERAL HARDWARE - The CGC 7900 PIO/DMA consists of one standard size digital circuit board, which will occupy one card slot in the 7900 mother board. The circuit board has five connectors along its card edge, two for the PIO interface, two for the DMA interface and one for Interrupt and Bus Grant Level Prioritizing.

The PIO/DMA circuit board consists of four separate 16 bit parallel interfaces. Two are programmable ports which the processor has full control over and the other two are DMA ports which once activated perform all transfers independent of the CPU.

1-2 PIO GENERAL DESCRIPTION - The programmable port can be operated by way of polling or by way of interrupts. Polled operation requires the CPU to write or read data to or from the port and then test the PIO status register to determine the readiness of the port. The second mode of operation is interrupt driven I/O. When the interface has a data word or byte for the CPU or is ready to transfer another word or byte out the port it notifies the CPU via an interrupt forcing the CPU to stop what it is doing and service the parallel port.

The Parallel Port consists of two 16 bit data registers one for input and the other for output. Each of these two ports can be subdivided into two 8 bit ports each with its own status, interrupt, and control circuitry.

The main features of the Parallel Port are:

1) Two 16 bit ports; one for input, one for output, each with its own control signals.

2) Word or byte transfers.

3) CPU interaction by polling or interrupts.

4) All receivers and drivers are differential according to RS-422 and RS-423 standards.

5) Transfer rates of up to 150K words or bytes per second.

1-3 DMA GENERAL DESCRIPTION - The DMA interface is compatible with three DEC DMA interfaces, the DRV11-B, DR11-W and DR11-B, each being used with a different type of DEC computer. Below are listed the main features of the DMA interface.

1) Two 16 bit ports one for input and one for output.

2) Data transfers up to 500K per second.

3) Separate 40 pin connector for input and output.

4) Transfer of up to 64K words at once without processor intervention.

5) Capable of Burst or Single Cycle Operation.

2-1 PIO/DMA HARDWARE OPTIONS - The purpose of this section is to describe certain hardware options that are applicable to both PIO and DMA portions of the board. There are additional options which apply strictly to either the PIO or DMA hardware which will be discussed in the appropriate sections of this manual.

2-2 MEMORY ADDRESS SELECTION - By use of a switch located at UF3 on the board the starting base address of all the registers on the board can be relocated in memory between FF8400 to and FF84F0. See Table 1 for switch setting versus memory address information.

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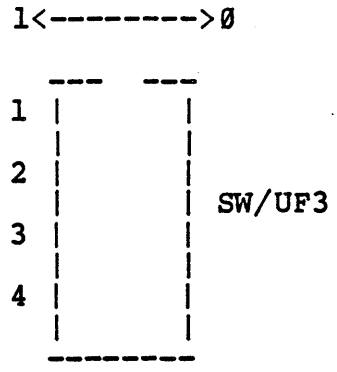


Base Address	1	2	3	4
FF8400	Ø	Ø	Ø	Ø
FF8410	1	Ø	Ø	Ø
FF8420	Ø	1	Ø	Ø
FF8430	1	1	Ø	Ø
FF8440	Ø	Ø	1	Ø
FF8460	Ø	1	1	Ø
FF8470	1	1	1	Ø
FF8480	Ø	Ø	Ø	1
FF8490	1	Ø	Ø	1
FF84A0	Ø	1	Ø	1
FF84B0	1	1	Ø	1
FF84C0	Ø	Ø	1	1
FF84D0	1	Ø	1	1
FF84E0	Ø	1	1	1
FF84F0	1	1	1	1

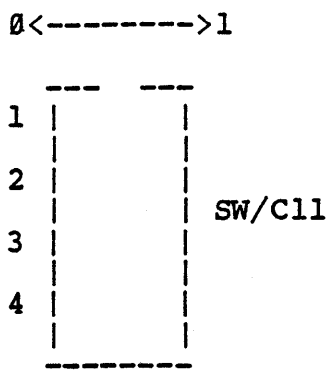
Base Address Switch Postions
Table 1.

2-3 INTERRUPT LEVEL SELECTION - If any of the interrupt capability on the board is to be used the two interrupt level jumpers must be installed. These jumpers select the interrupt level at which all the interrupts on the board will operate.

The interrupt levels that are available for use are levels 1, 2, 3 and 6. Levels 4 and 5 are reserved for the CPU board and level 7 is reserved for the power up interrupt. Jumpers J2 and J3 are the interrupt level jumpers. The level of interrupt desired must be reflected on both of these jumpers and must be the same. Example: if J2 has a jumper in position two J3 must also have its jumper in position two. Each header must have only one jumper. In order to complete interrupt acknowledge decoding there must also be a jumper installed on header J1 at position IN0. Refer to Section 5.0 HARDWARE EXPANSION if more than one board is to be installed at the same interrupt level.

2-4 VECTOR ADDRESS SELECTION - The interrupt vector addresses of all the interrupts occurring on the board are switch selectable. Vector addresses between 100 and 13F are reserved for the interrupts on the CPU card. There is a possibility of eight interrupts occurring on the PIO/DMA board including the spare. Thus, the base address of the interrupt vectors must move at even intervals of eight. The switch used to select the vector addresses is located at position UC11. See Table 2 for vector address selection.

2-5 BUS GRANT SELECTION - The level of bus master control granted to each PIO/DMA board is selectable by means of jumpers located at J4 and J5. In a single board system there must be one jumper installed in both J4 and J5 headers and they must agree with each other. Example: If bus master level three is desired, J4 must have a jumper at three and J5 must have a jumper at three in the 2 thru 5 positions. Refer to Section 5.0 HARDWARE EXPANSION if more than one board is to share the same Bus Master level.



Base Vector Adress	Switch Position 1	2	3	4
200H	0	0	0	0
220H	1	0	0	0
240H	0	1	0	0
260H	1	1	0	0
280H	0	0	1	0
2A0H	1	0	1	0
2C0H	0	1	1	0
2E0H	1	1	1	0
300H	0	0	0	1
320H	1	0	0	1
340H	0	1	0	1
360H	1	1	0	1
380H	0	0	1	1
3A0H	1	0	1	1
3C0H	0	1	1	1
3E0H	1	1	1	1

Base Interrupt Vector Switch Positions
Table 2.

3-1 HARDWARE EXPANSION - The purpose of this section is to describe methods in which more than one PIO/DMA board can be used in one system. The types of expansion referred to are Interrupt Expansion and Bus Master Expansion.

The first step to be taken when expanding either an interrupt level or a bus grant level is that of installing the Priority Cable between the two boards at position P3. This cable is a 26 pin card edge to card edge cable available from Chromatics (P/N 100428).

3-2 INTERRUPT EXPANSION - When selecting interrupt levels if it is desirable to have two boards share the same interrupt level the hardware priority cable must be installed between the two boards, see above. The interrupt priority jumpers must also be positioned properly on the two boards. The board which is to have the highest priority within the level must have a jumpers at positions IN 0 and OUT 1. The next board in the chain must have jumpers at positions IN 1 and OUT 2 and so on down the line. The maximum number of boards to share the same interrupt level is 10.

3-3 BUS MASTER EXPANSION - Bus Master Expansion is accomplished in much the same manner that Interrupt Expansion is. The board which is to have the highest priority within the bus grant level must have a jumper at position IN2 and position OUT1 on J5. The next board in the chain will have jumpers at position IN 5+1 and position OUT2 and so on. This sequence will continue up until the last board in the chain. All boards in the same level must have the jumper at J4 in the same position indicating a shared level. Thus, any board in the chain can request the bus causing the CPU to grant it. The first board in the chain will receive the bus grant signal from the processor and if it does not want the bus at the present time it will propagate the signal out to the next board and so on down the chain.

NOTE: It must be assured that there are no conflicts in the switch settings for either the memory or vector addresses.

4-1 PIO THEORY OF OPERATION - This section of the manual will describe functionally how the PIO portion the PIO/DMA board operates.

4-2 PROGRAMMABLE PORT CONTROL REGISTERS - The programmable parallel port consists of one 16 bit control register and two 16 bit data registers. The addresses of these registers are as follows:

FF84XØ low data byte read or write address
FF84X1 high data byte read or write address
FF84X2 Parallel Port Status byte (See Below)
FF84X3 Parallel Port Interrupt mask (See Below)

Figure 1 is a definition of the Parallel Port Control Register. Following the figure is the definition of each bit.

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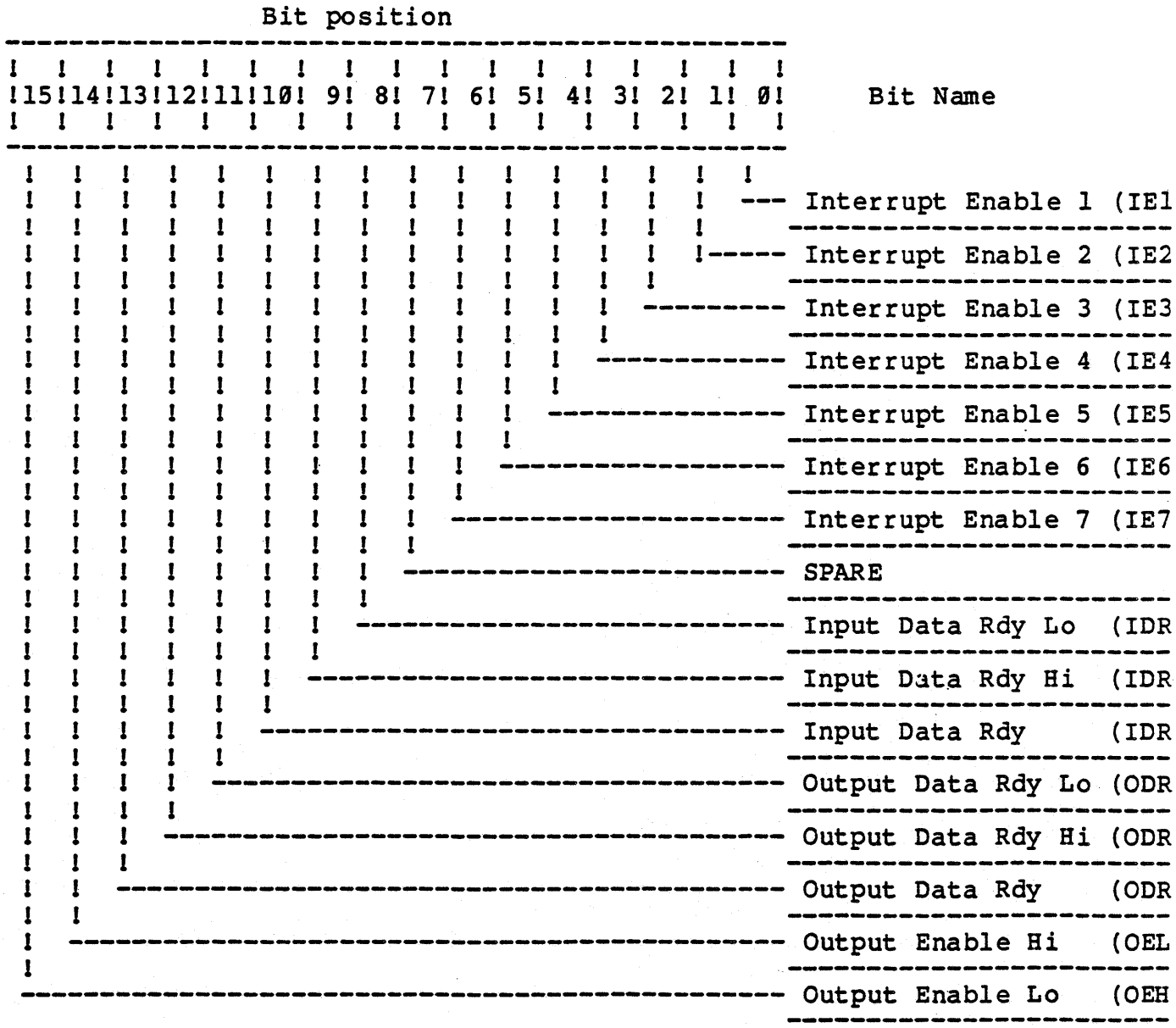
Register name PROGRAMMABLE PORT CONTROL REGISTER (PPCR)

Memory location FF84X2 (Base word address)

FF84X2 Status Byte bits 8 - 15

FF84X3 Interrupt mask bits 0 - 7



Programmable Control Register Definition
Figure 1.

The interrupt enables bits located in the low byte of the control word are used to enable any one of seven interrupts and are defined as follows:

IE1 - Enables interrupts to occur when the present DMA transfer is complete. This indicates to the CPU that the interface must now be re-programmed in order to perform another transfer. (Ø=Interrupt Enabled, 1=Interrupt Masked)

IE2 - Enables interrupts on the low byte of the out going data word. This interrupt indicates to the CPU that more data can now be sent out to this byte of the port. (Ø=Interrupt Enabled, 1=Interrupt Masked)

IE3 - Enables interrupts on the high byte of the out going data word. This interrupt indicates to the CPU that more data can now be sent out to this byte of the port. (Ø=Interrupt Enabled, 1=Interrupt Masked)

IE4 - Enables interrupts on the entire sixteen bit output word. This interrupt indicates to the CPU that the entire word is now ready to transmit more data. (Ø=Interrupt Enabled, 1=Interrupt Masked)

IE5 - Enables interrupts on the low byte of incoming data word. Indicates to the CPU that a byte has been received on input data bits Ø-7 and is ready to be read. (Ø=Interrupt Enabled, 1=Interrupt Masked)

IE6 - Enables interrupts on the high byte of the incoming data word. Indicates to the CPU that a byte has been received on input data bits 8-15 and is ready to be read. (Ø=Interrupt Enabled, 1=Interrupt Masked)

IE7 - Enables interrupts on the incoming data word, indicates to the CPU that data has been received on input data bits Ø-15 and is now ready to be read. (Ø=Interrupt Enabled, 1=Interrupt Masked) The high byte of the input data buffers.(Active=1)

IDRLO - Status bit indicating to the CPU that there is data present at the low byte of the input data buffers.(Active=1)

IDR - Status bit indicates to the CPU that there is data present at the input word to the data buffers.(Active = 1)

ODRHI - Status bit indicates to the CPU that the data on the high byte of the output data buffers has been transferred and more data can now be written out to it.(Active=1)

ODRLO - Status bit indicates to the CPU that the data on the low byte of the output data buffers has been transferred and more data can now be written out to it.(Active=1)

ODR - Status bit indicates to the CPU that the entire output

word has been transferred and more data can now be written out to it. (Active=1)

OELO - This is a read write control bit which when set to one enables the output data drivers DØ - D11, which are otherwise tri- state.

OEHI - This is a read write control bit which when set to one enables the output data drivers D12- D15, which are otherwise tri- state.

NOTE: OELO and OEHI must be set to one's for output port to work at all.

4-3 POLLING THEORY OF OPERATION - This portion of the manual will describe how to use the programmable parallel port in polling mode. There are two polling sequences the CPU can go thru in relation to the programmable port, the first is polling waiting to write and the second is waiting to read.

4-4 PIO POLLING TO WRITE - When the CPU is ready to write out either a word or a byte, the appropriate status bit can be tested. If the bit is found to be in the active state it indicates to the CPU that the previous data has been transferred and more data can now be sent. This operation can continue as long as there is more data to be transmitted or until the device on the other end of the interface stops reading the data being transmitted.

4-5 PIO POLLING TO READ - When the CPU is expecting input data from the parallel port it may initiate a polling sequence on the appropriate byte or word status bit. If the status bit is found to be active the CPU may read the byte or word, store it and continue to poll for as long as is required.

All control signals to the interface are manipulated by hardware which is triggered from the CPU reads or writes.

4-6 PIO WRITE OPERATIONS USING INTERRUPTS - There are three types of interrupts which can trigger the CPU to transfer data out of the parallel output port. The first is the write word interrupt. This interrupt occurs when the PIO output hardware has transferred both the high and the low bytes out to the user device and can now accept another word for transmission. The second type of write interrupt which can occur is the write high byte interrupt. This interrupt occurs when the PIO output hardware has completed the transmission of the data on the high byte of the parallel output latch and can now accept more data to be transmitted out on that byte. The final type of write interrupt which can occur is the write low byte interrupt. This interrupt occurs when the parallel output hardware has completed the transmission of the data on the low byte of the parallel output port and can now accept more data to be transmitted

on that byte. For any of these interrupts the appropriate interrupt mask bit must be set to a zero in the control status word.(See above).

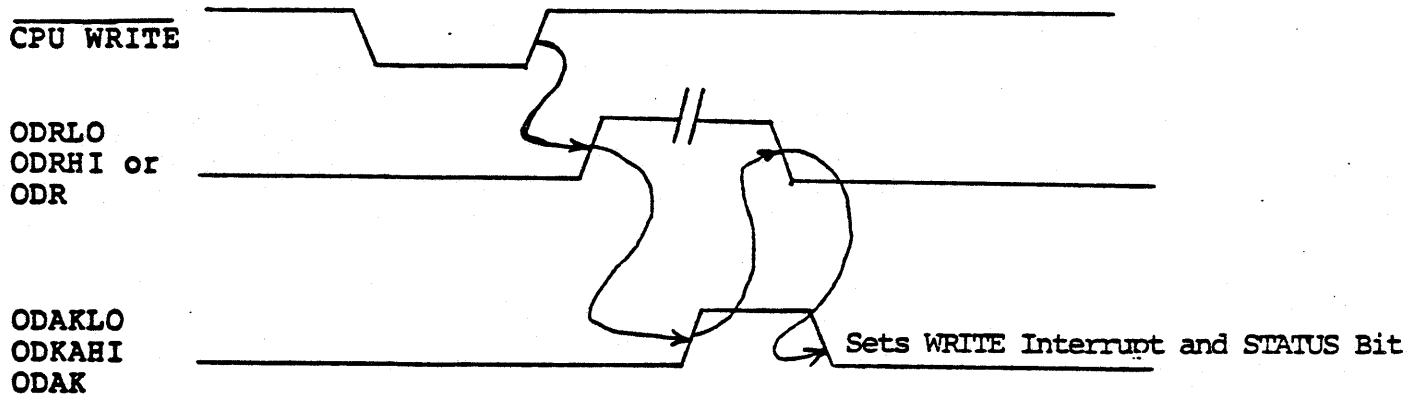
4-7 PIO READ OPERATIONS USING INTERRUPTS - Three types of interrupts exist from which the 7900 CPU can receive an interrupt from the parallel port. The first type is the Read Word Interrupt. This interrupt occurs when all 16 bits of input data have been presented to the parallel port input buffers and is ready to be read by the CPU. The second type of read interrupt which can occur is the read high byte interrupt. This interrupt occurs when data has been presented to the high input data buffer of the parallel port and is ready to be read by the CPU. The final type of read interrupt which can occur is the read low byte interrupt. This interrupt occurs when data has been presented to the high byte of the parallel port input buffers and is ready to be read by the CPU.

5-1 PIO HARDWARE DESCRIPTION - Once the CPU has determined that the output port desired is available for transfer a write operation is performed to the appropriate location in memory. On the trailing low to high transition of the write operation the output date is latched into the output buffers and the appropriate OUTPUT DATA READY signals are set active as follows:

ODRLO - Output Data Ready Low Byte
ODRHI - Output Data Ready High Byte
ODR - Output Data Ready Word

These signals will remain active until the appropriate Output Data Acknowledgements are received at the interface as follows:

ODAKLO - Output Data Acknowledge Low Byte
ODAKHI - Output Data Acknowledge High Byte
ODAK - Output Data Acknowledge Word



PIO Write Timing
Figure 2.

Once the appropriate data acknowledgements go inactive, again status bits will be set to indicate to the CPU that another transfer can now be performed.

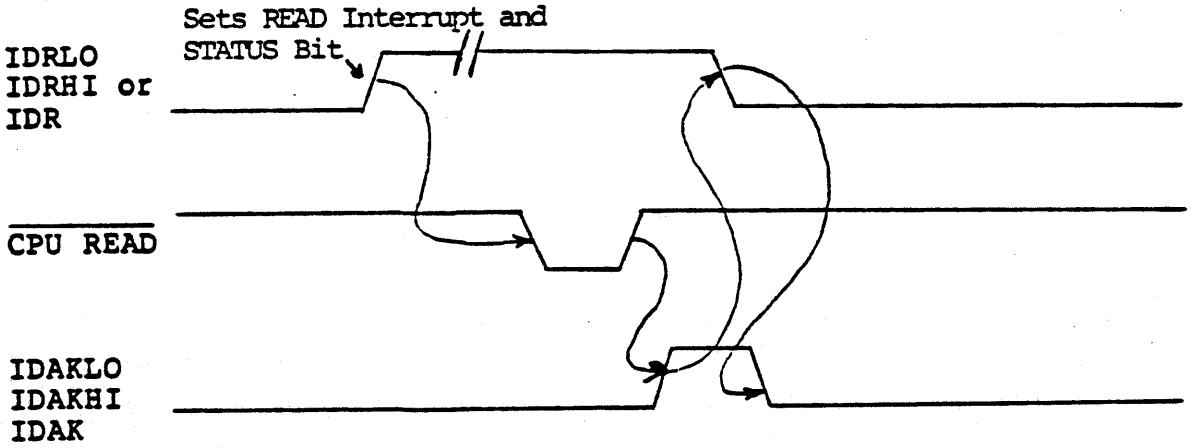
5-2 HARDWARE THEORY OF OPERATION - If a user device has data to be input to the CPU it must first set up the data at the appropriate data inputs. It must then bring the appropriate positive input data ready signal positive with the respect to the minus input as follows:

IDRLO - Input Data Ready Low Byte
IDRHI - Input Data Ready High Byte
IDR - Input Data Ready Word

These signals as well as the data inputs must remain active until the data has been read by the CPU. On the low to high trailing edge of the CPU read of the input data port the appropriate input data acknowledges signals will be set active as follows:

IDAKLO - Input Data Acknowledge Low Byte
IDAKHI - Input Data Acknowledge High Byte
IDAK - Input Data Acknowledge Word

Signal timing should be as follows:



PIO Read Timing
Figure 3.

5-3 PIO OPTIONING - There are three configurations which the PIO receivers can be operated under. One is as straight differential receivers with no bias or terminating resistors. The second is differential receivers with a shunt terminating resistor across the positve to minus inputs. The third configuration is that of a single ended receiver with terminating resistors at the minus input holding it at a threshold of approximately 3.Ø volts and a single resistor terminator to ground on the positive input. To implement each of the three configurations see Table 3 for resistor pack values and locations.

Configuration	A	B	C
R4	-	-	T
R5	-	S	P
R6	-	S	P
R7	-	-	T
R8	-	-	T
R9	-	S	P
R1Ø	-	S	P
R11	-	-	T
R16	-	S	T
R17	-	-	P
R18	-	-	1/4 W 33Ø ohm *
R19	-	-	1/4 W 47Ø ohm *
R2Ø	-	-	1/4 W 33Ø ohm *
R21	-	-	1/4 W 33Ø ohm *
R23	-	-	1/4 W 47Ø ohm *
R24	-	-	1/4 W 33Ø ohm *

PIO Terminator Options
Table 3.

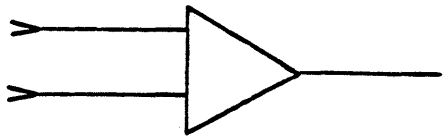
Configuration A is straight Differential with no resistors.
Configuration B is straight Differential with shunt resistors.
Configuration C is single ended receivers with 2.2 volt bias at the minus input and a terminator to ground on the PLU input.

Resistor S is an 8 pin 22Ø ohm series resistor pack
Resistor P is an 8 pin 22Ø ohm common end resistor pack
Resistor T is an 1Ø pin 47Ø ohm/33Ø ohm terminating resistor pack.

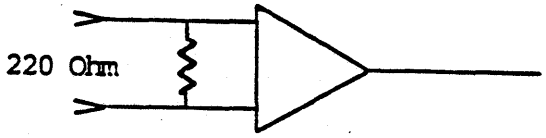
* NOTE:

When configuration B is selected a 1/4 Watt 22Ø ohm resistor must be installed between the signal ends of R18 and R19, and R23 and R24.

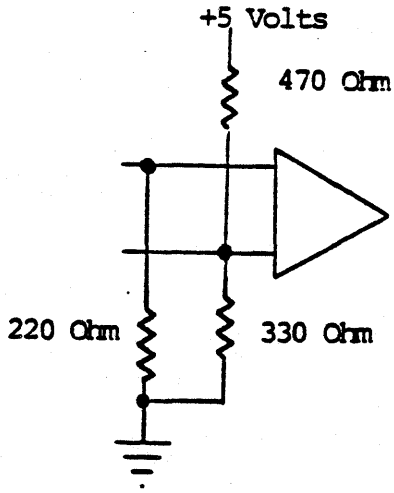
Below are three schematic representations of each of the available configurations that can exist on the input to the PIO card.



CONFIGURATION A



CONFIGURATION B



CONFIGURATION C

PIO Terminator Configurations
Figure 4.

5-4 PIO INPUT/OUTPUT OPTIONING - On the P4 connector of the PIO port there are the 16 data outputs, three output control lines, three input control lines, three connections for ground, and three connections for +5 volts. These signals are all that is needed for the parallel port to operate in the mode that is described in the theory of operation of the parallel port. There are certain conditions with some interfaces that a static input is needed for some sort of status of a device. To accomplish this static input operation two mechanisms have been included in the design of the output parallel port. The first is the ability to tri-state the upper 4 bits of the sixteen output data bits and the second is the four pin header located at J6 on the circuit board. The upper four bits are made tri-state by the clearing of bit 6 in the PIO control register, this operation is described further in section 6.Ø PIO Theory of Operation. Once these bits are tri-state the four jumpers located at J6 can be installed and thus the four most significant ouptuts bits on the P4 connector have been turned into static inputs that can be tested by the CPU.

5-5 PIO CONNECTOR DEFINITION - The PIO/DMA circuit has two 5Ø Pin card edge connectors which are designed to be used strictly for programmed parallel transfers to and from the CPU. The two connectors are designated P4 and P5, P4 being the data output connector and P5 being the data input connector. Below are lists of all the pins available at the connectors, the associated signal name for each pin and a brief description of each is given.

PIO/DMA P4 Connector Designation

Pin Number		Signal Name	Pin Number		Signal Name
1		DATA OUT Ø	26	*	DATA OUT 12
2	*	DATA OUT Ø	27		DATA OUT 13
3		DATA OUT 1	28	*	DATA OUT 13
4	*	DATA OUT 1	29		DATA OUT 14
5		DATA OUT 2	3Ø	*	DATA OUT 14
6	*	DATA OUT 2	31		DATA OUT 15
7		DATA OUT 3	32	*	DATA OUT 15
8	*	DATA OUT 3	33		GND
9		DATA OUT 4	34		+5 Volts
1Ø	*	DATA OUT 4	35		GND
11		DATA OUT 5	36		+5 Volts
12	*	DATA OUT 5	37		GND
13		DATA OUT 6	38		+5 Volts
14	*	DATA OUT 6	39		ODRHI
15		DATA OUT 7	4Ø	*	ODRHI
16	*	DATA OUT 7	41		ODRLO
17		DATA OUT 8	42	*	ODRLO
18	*	DATA OUT 8	43		ODR
19		DATA OUT 9	44	*	ODR
2Ø	*	DATA OUT 9	45		ODAKHI
21		DATA OUT 1Ø	46	*	ODAKHI
22	*	DATA OUT 1Ø	47		ODAKLO
23		DATA OUT 11	48	*	ODAKLO
24	*	DATA OUT 11	49		ODAK
25		DATA OUT 12	5Ø	*	ODAK

PIO/DMA P4 Connector Designation
Table 4.

*SIGNAL COMPLEMENT

PIO/DMA P5 Connector Designation

Pin Number	Signal Name	Pin Number	Signal Name
1	DATA IN Ø	26	* DATA IN 12
2	* DATA IN Ø	27	DATA IN 13
3	DATA IN 1	28	* DATA IN 13
4	* DATA IN 1	29	DATA IN 14
5	DATA IN 2	3Ø	* DATA IN 14
6	* DATA IN 2	31	DATA IN 15
7	DATA IN 3	32	* DATA IN 15
8	* DATA IN 3	33	GND
9	DATA IN 4	34	+5 Volts
1Ø	* DATA IN 4	35	GND
11	DATA IN 5	36	+5 Volts
12	* DATA IN 5	37	GND
13	DATA IN 6	38	+5 Volts
14	* DATA IN 6	39	IDRHI
15	DATA IN 7	4Ø	* IDRHI
16	* DATA IN 7	41	IDRLO
17	DATA IN 8	42	* IDRLO
18	* DATA IN 8	43	IDR
19	DATA IN 9	44	* IDR
2Ø	* DATA IN 9	45	IDAKHI
21	DATA IN 1Ø	46	* IDAKHI
22	* DATA IN 1Ø	47	IDAKLO
23	DATA IN 11	48	* IDAKLO
24	* DATA IN 11	49	IDAK
25	DATA IN 12	5Ø	* IDAK

PIO/DMA P5 Connector Designation
Table 5.

*SIGNAL COMPLEMENT

6-1 DMA THEORY OF OPERATION - The purpose of this section is to describe how general purpose Direct Memory Transfers are accomplished to and from the CGC 7900.

The DMA portion of the PIO/DMA card has been designed to be compatible with DEC's DR11-W, DRV11-B and DR11B DMA parallel interfaces. The details concerning the DMA hardware are in Section 7 "DMA Hardware Description". This section deals with the overall operation of the interface.

6-2 DMA TRANSFER MODES - There are two modes in which data can be transferred to or from the DMA interface. These are Burst Mode transfers and Single Cycle Mode transfers. In both modes of operation the interface is armed by the CPU, all subsequent transfers up until the end of the specified transfer size are then done without further CPU intervention. The difference lies in how the bus arbitration is handled between the CPU and the DMA board. In Burst Mode once the interface is armed the logic on the DMA board will acquire the system bus and not relinquish it until the entire transfer is complete. In Single Cycle Mode the DMA logic will share the system bus with the processor using every other memory cycle while the CPU uses the ones in between. Inside the Burst Mode and Single Cycle Mode there are two types of data transfers that can be performed, they are:

1 Write Words (7900 to DEC)
2 Read Words (DEC to 7900)

NOTE: The DR11-W, DRV11-B and DR11-B interfaces also support read-modify write mode and byte transfers, these two modes are not supported on the CGC DMA board.

How each of these modes are selected and their effects on the system will be discussed in the control register definition.

6-3 DMA THEORY OF OPERATION - There are two types of transfers that can be performed to or from a DEC machine, one is a program controlled transfer and the other is a DMA type of transfer. The program controlled transfer is very similar to that of the PIO transfer in that all transfers are performed under control of the CPU. However, the protocol as to when data is valid and not valid is completely up to the user. Data is transferred via the data buffer registers using the STATUS and FUNCTION lines to determine data availability. The purpose of this section of the manual is to describe in detail how a DMA transfer operation is performed from the CGC 7900 to a receiving device.

6-4 DMA REGISTER INITIALIZATION - Before a DMA transfer is initiated by the CGC 7900 the following registers must be set up:

1) Word Count Register

2) Control Register

3) Bus Address Register

4) Extended Address Register

The final write to the Extended Address Register is the trigger to the interface to begin transferring data. Depending on whether the transfer is from CGC 7900 to DEC or from DEC to CGC 7900 the DMA logic will perform one of two sequences descibed in the following section.

6-5 DMA BUS CYCLES

7900 Bus Request Cycle

The DMA control circuitry will drive low the selected Bus Request Line on the CPU control bus and wait for the corresponding Bus Grant Signal from the CPU. Once the CPU has granted the bus and completed its present bus cycle the DMA control logic will remove its Bus Request and drive low the Bus Grant Acknowledge Signal (BGACK). The activation of this signal causes the CPU buffers to go tri-state and thus removes the CPU from the system bus. The BGACK signal causes the CPU card to remove its Bus Grant. The CPU is now completely off the bus and the DMA circuitry has full access to the entire system.

7900 DMA Logic Data Fetch Cycle

When the DMA control logic has been granted the bus by the CPU it immediately enables its output buffers, containing the address and all control bus information for the desired data. After a period of approximately 70 nanoseconds the DMA control logic asserts Address Strobe, Upper and/or Lower Data Strobe and then waits for the Data Transfer Acknowledge signal back from the selected memory (DTACK). When the DTACK signal is received the DMA logic will wait 200 nanoseconds and then latch the data into data output buffers. It will also remove Address Strobe, Upper and/or Lower Data Strobe, remove its address buffers from the bus, increment its word count register and bus address registers and release its hold of the bus by de-asserting BGACK. The CPU will then begin normal execution exactly where it left off before the bus was relinquished to the DMA control logic.

7900 Cycle Request to the DR11-W, DRV11-B or DR11-B

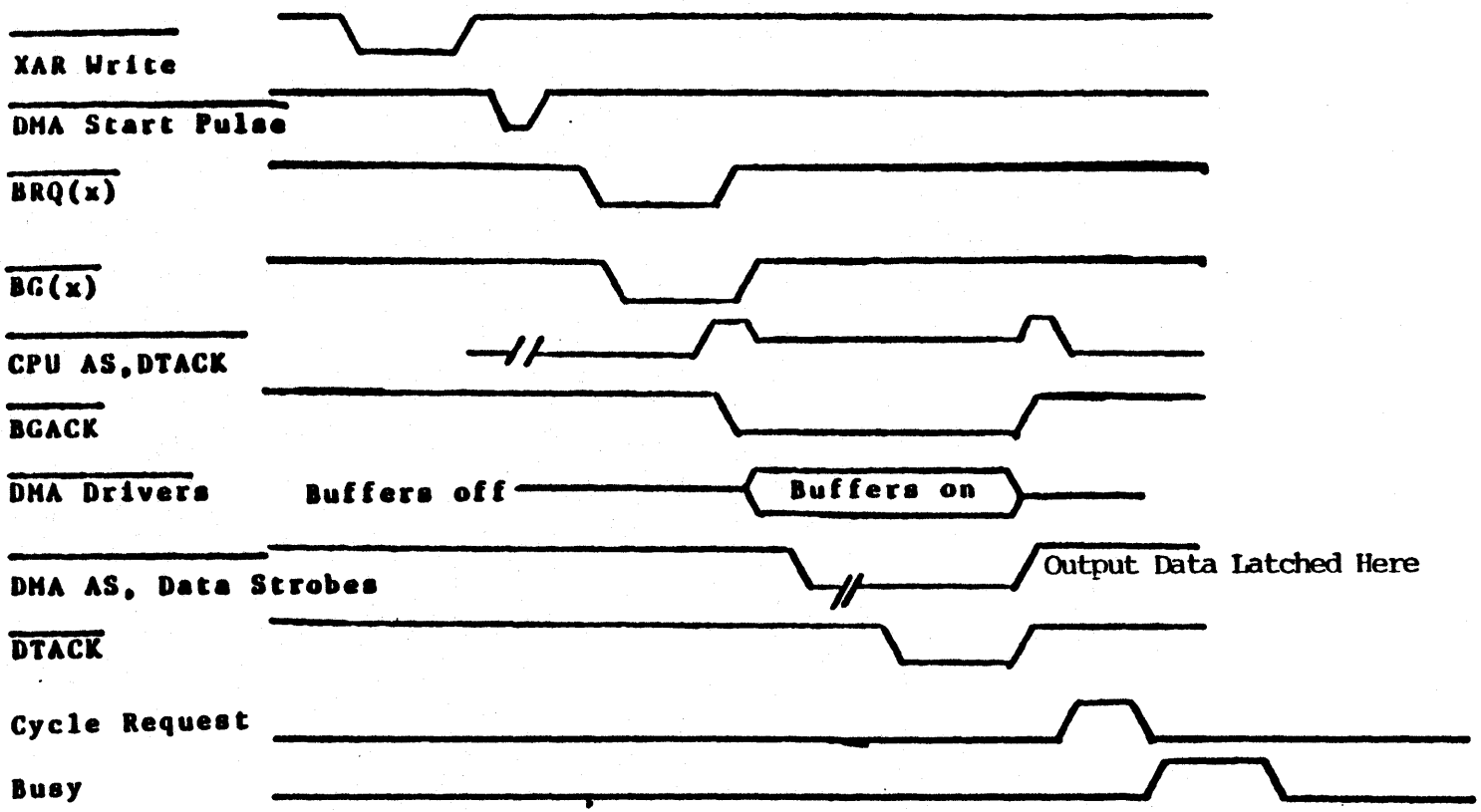
Once the data has been loaded into the output data buffers and is ready for transfer to the DEC interface the DMA control logic will assert CYCLE REQUEST. This will cause the DEC interface to initiate a bus cycle. This will be indicated to the 7900 DMA control logic by the assertion of the BUSY signal by the DEC interface. The 7900 DMA control logic will then remove its cycle request and wait for the BUSY signal to be de-asserted. The 7900 DMA control logic will then check to see if the transfer is complete. If not it will continue the transfer by once again requesting the system bus. If the transfer is complete the DMA logic can interrupt the CPU or can be polled by the CPU by testing the appropriate bit in the DMA Status Register.

If the transfer is to be from the DEC interface to the 7900 the 7900 Cycle Request is performed first, thus acquiring the data to be written into the 7900 memory. The 7900 DMA control logic will then perform a Bus Request Cycle as described above. Once the system bus has been acquired the following sequence will be performed:

7900 Data Write Operation

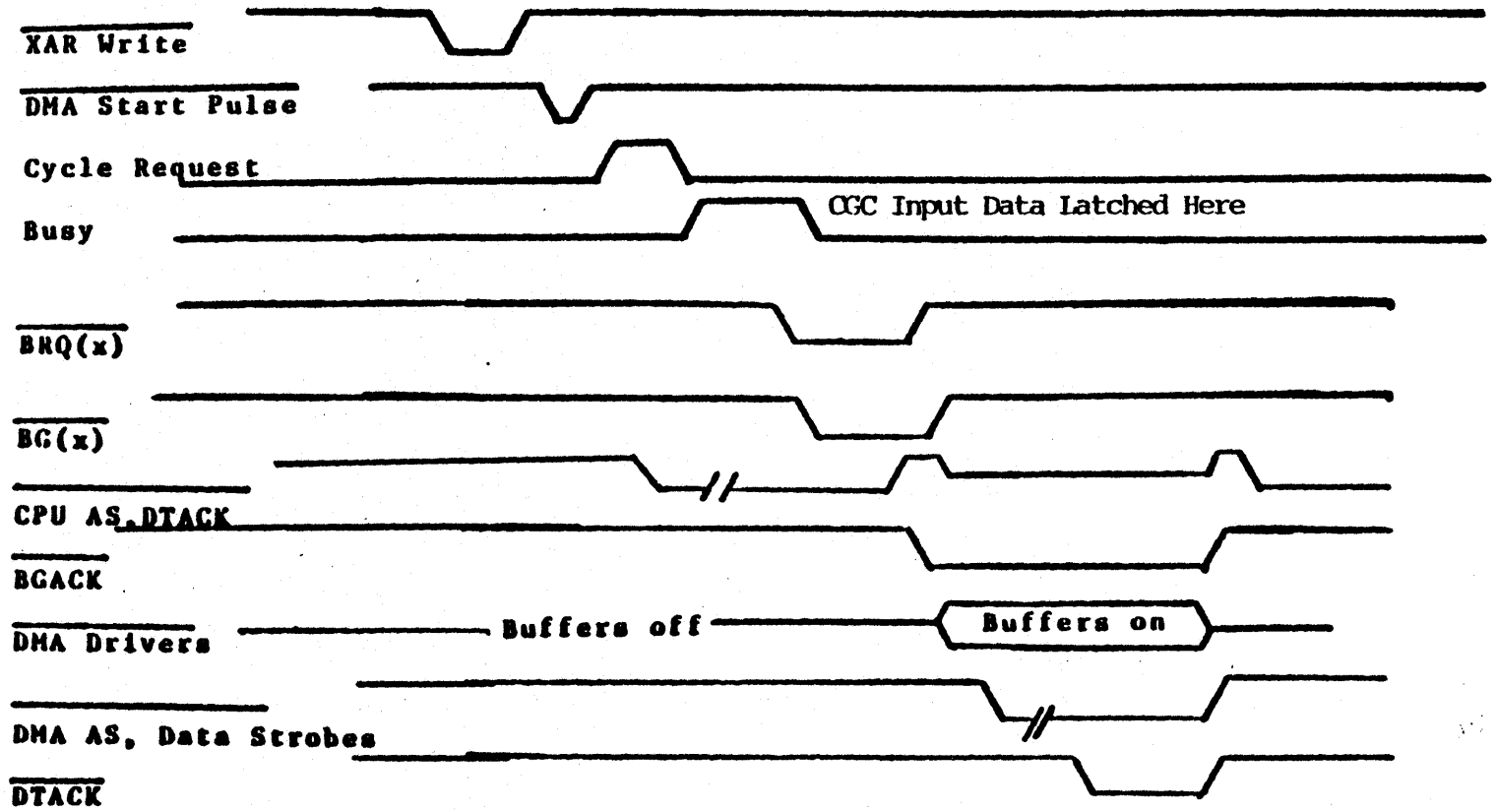
Once the system bus has been acquired the DMA control logic will enable its address buffers, data buffers, function code buffers and write signal buffer. Approximatly 70 nanoseconds later Address Strobe Upper and/or Lower Data Strobes will be asserted. When the selected memory responds with DTACK the DMA logic will wait 200 nanoseconds and then de-assert address strobe, the data strobes as well as remove all of its other buffers from the data bus. It will finally relinquish the bus by de-asserting BGACK.

See timing figures five and six for signal relationships.



CGC to DEC Host Timing

Figure 5.



DEC Host to CGC
Timing

Figure 6.

6-6 DMA REGISTER DEFINITION - There are six registers which are used strictly by the DMA portion of the DMA/PIO circuit board. This section of the manual describes how those registers are used.

OUTBUF - This is a 16 bit output data latch which can be written to by the CPU directly or through the DMA hardware. The CPU can write to this buffer only when the DMA is not active, once the interface is armed and until the transfer is complete all transfers to the OUTBUF are under control of the DMA hardware.

INBUF - This is a 16 bit input latch used to receive data from the DEC or other host device. This buffer can be read either directly by the CPU, or via the DMA hardware. Once the interface is armed and until the transfer is complete all control of the INBUF is via the DMA hardware.

Bus Address Register(BAR) - This register contains the least significant 16 address bits of the address to be transferred. This is a write only register.

Control Register(CTRLREG) - The Control Register is an 8 bit read/write register which is used to control all of the details of the type of transfer to be done. The Control Register along with the Extended Address Register combine to make up one 16 bit register, the control register being the least significant 8 bits. (See Below)

Extended Address Register(XAR) - This is an 8 bit write only register containing the most significant 7 bits of address information. This along with the Control Register make up a 16 bit register, the XAR being the most significant 8 bits with the MSB not being used. The loading of this register triggers the transfer. (See Below)

Word Count Register - This is a write only register which is loaded with the two's complement of the word count to be transferred.

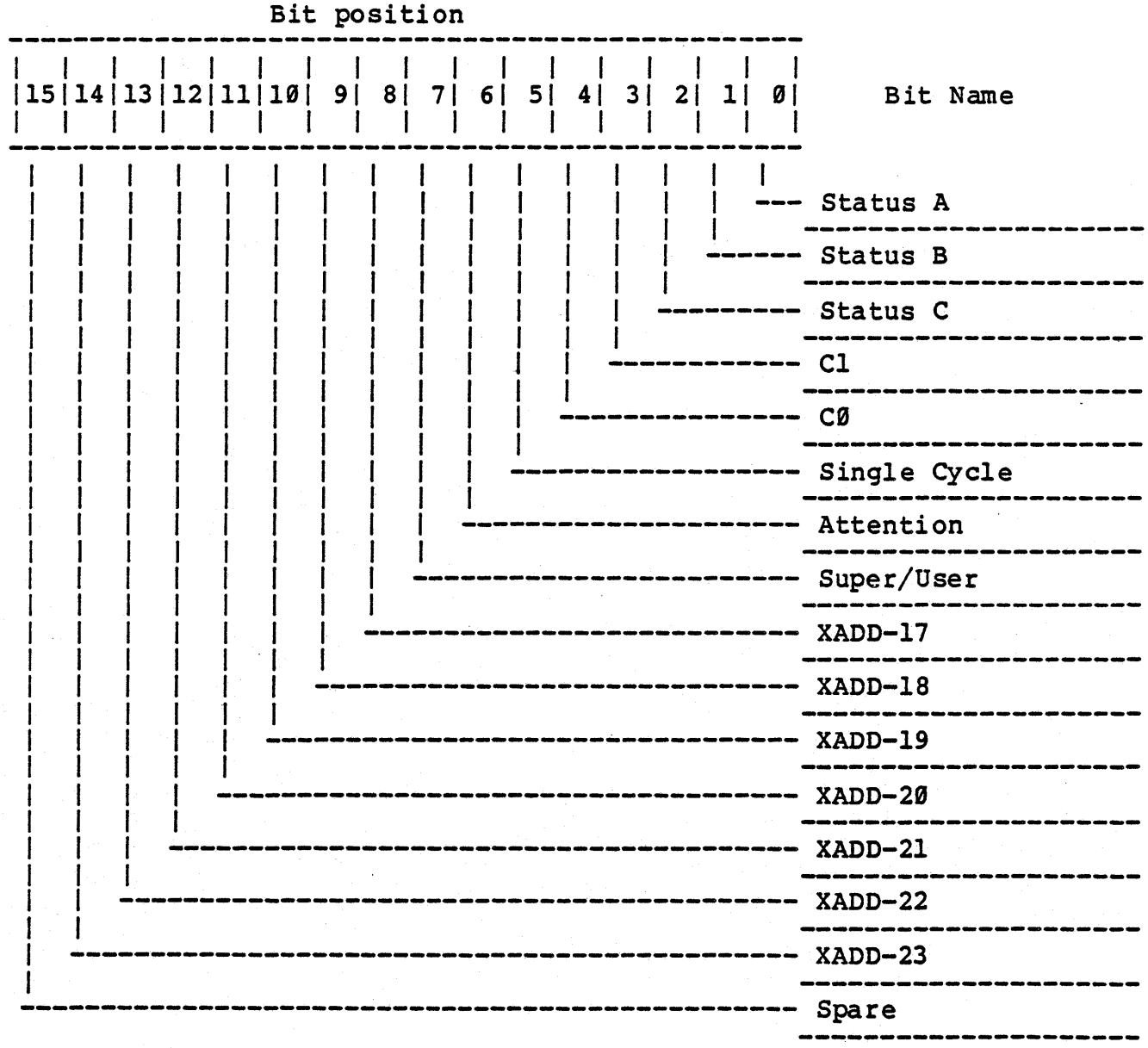
The addresses for all registers pertaining to the DMA portion of the PIO/DMA card are as follows:

FF84X4 Address Bits 17-23 of the DMA address (See Below)
FF84X5 Read Write Control bits pertaing to DMA transfers (See Below)
FF84X6 Bits 8 - 15 of the word count
FF84X7 Bits Ø - 7 of the word count
FF84X8 address bits 1 - 16 of the starting DMA address
FF84XA Read/Write DMA High data word
FF84XD DMA Status byte (See Below)

X Selected by address switch, see Hardware Optioning

Register name Control/Extended Addresss

Memory location $FF84X4



Extended Address/Control Regsiter Definition
Figure 7.

XADD17 THRU XADD23 - Used to hold the most significant 7 bits of the CGC address to or from which the transfer is to be performed.

Status A, B and C - User defined status bits, used for program controlled transfers to indicate data ready and data received.

CØ and C1 - These two output control signals are used by the DEC machine to indicate the type of bus cycle to be performed, they are defined as follows:

CØ	C1	Bus Cycle
Ø	Ø	Word Transfer from PDP to CGC
1	Ø	Not Used
Ø	1	Word Transfer from CGC to PDP
1	1	Not Used

Bus Cycle Definitions
Table 6.

Single Cycle - This signal indicates to the DEC machine the bus master mode under which the transfer is to take place. When this bit is high the transfer is done one cycle at a time, thus sharing the bus with the CPU. When this bit is low the transfer is done all at once and the system bus is not relinquished until the transfer is complete.

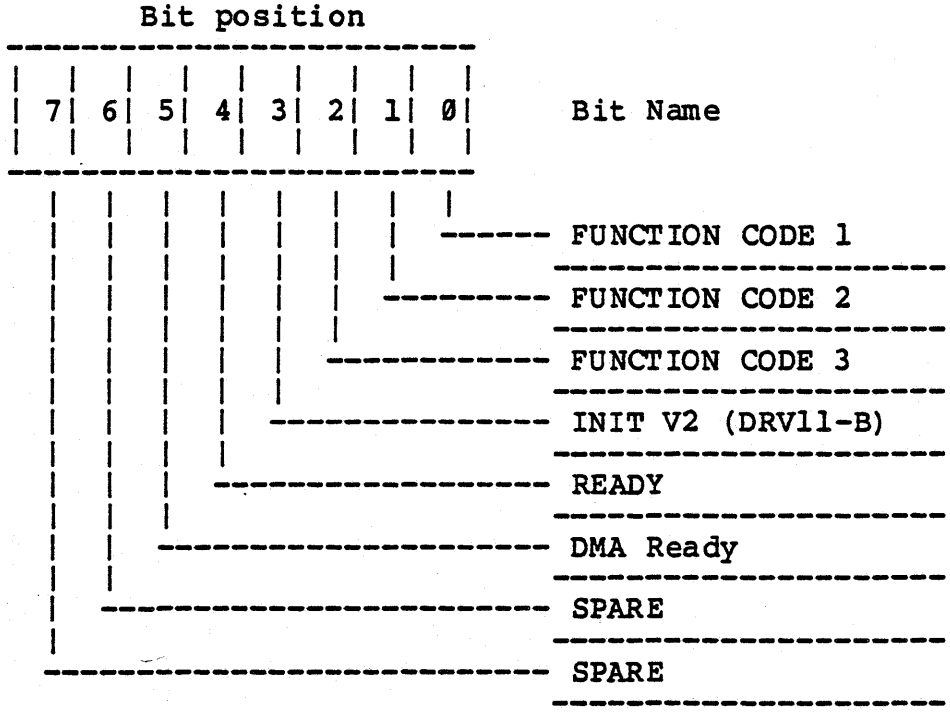
Attention - Used to notify the PDP-11 that some sort of exception has occurred and that the present transfer must be aborted.

Super/User - Used to define the type of memory area in which the CGC transfer is to take place. When it is high it will be a supervisor data area transfer and when it is low it will be a user data area transfer.

DMA Status Register - The DMA status register contains five signals from the interface which are used in determining the state of the interface. These bits are not part of the control register due to the fact that the CGC has no control over them, they are read only. Below is the definition of the Status Register with a description of each bit following.

Register name DMA Status Register

Memory location $FF84XD (Byte)



DMA Status Register Definition
Figure 8.

FUNCTION CODES 1, 2 and 3 - These are status bits which can be used to convey to the 7900 some sort of interface information. The function of these bits are user defined. If FUNCTION CODE 2 is set high by the user device it will cause an interrupt to occur in the 7900. If the DMA interrupt enable bit is cleared in the interrupt mask register. This is a level and must be cleared by the user after some sort of acknowledgement has occurred.

INIT V2 - Used for interprocessor communication it will reflect the state of FUNCTION CODE 2.

READY - Indicates to the CGC that the user device is ready to begin a transfer. (Acive = 1)

DMA Ready - This bit when active indicates that the DMA hardware has completed the most recent transfer and is now ready to be initialized for another transfer.

7-1 DMA HARDWARD DESCRIPTION - As was mentioned earlier there are two 40 pin right angle connectors located on the card edge of the PIO/DMA card which are used strictly for transfers to a DEC computer. All signals on these connectors are compatible with DEC's DR11-W, DR11-B and DRV11-B DMA interfaces, with a few minor differences which will be discussed here. Connections are made to the DEC computer system via a pair of 40 pin flat ribbon cables. If connection is to be made into a DRV11-B these cables will connect directly onto the DRV11-B circuit board on the DEC Q-Bus. If connection is to be made into a DR11-B these cables will connect directly into the CGC 7900 to DR11-B adapter board supplied by Chromatics (P/N 100428). See Cable Diagrams A and B for these two cable inter-connections. If connection is to be made to the DR11-W the cables will be plugged directly into the DR11-W on the UNIBUS.

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7-2 DMA SIGNAL DEFINITION - All signals described in this section of the manual are also described in the Associated DEC User Manuals for the DRV11-B, DR11W, and the DR11-B DMA interfaces.

ØØ OUT - 15 OUT	16 TTL output lines to the DEC interface.
ØØ IN - 15 IN	16 TTL input lines from the DEC interface.
STATUS A,B,C	Three TTL output lines to the DEC interface. The function of these lines are defined by the user.
FUNCT 1,2,3	Three TTL input lines from the DEC interface. The function of these lines are defined by the user. *
INIT	One TTL input Status line from the DEC interface.
INIT V2 (DRV11-B)	One TTL input line from the DEC interface. Used by DEC machines for inter-processor. User defined for CGC 7900 applications.
AØØ	AØØ One TTL output line to the DEC interface. This line is normally for word transfers. During byte transfers this line controls address bit ØØ in the DEC machine.
BUSY	One TTL input line from the DEC interface. BUSY is low when the DRV11-B or the DR11-B control logic is requesting control of the LSI-11 bus or when a DMA cycle is in progress. A low to high transition indicates the end of the cycle. Busy is high when the DR11-W is requesting the bus or performing a data transfer. A high to low transition indicates the end of the cycle.
READY	One TTL input line from the DEC interface. When the READY line goes low DMA transfers may be initiated by the CGC 7900.
CØ,C1	CØ, C1 Two TTL output lines to the DEC interface. These lines control the type of bus cycle that the DMA

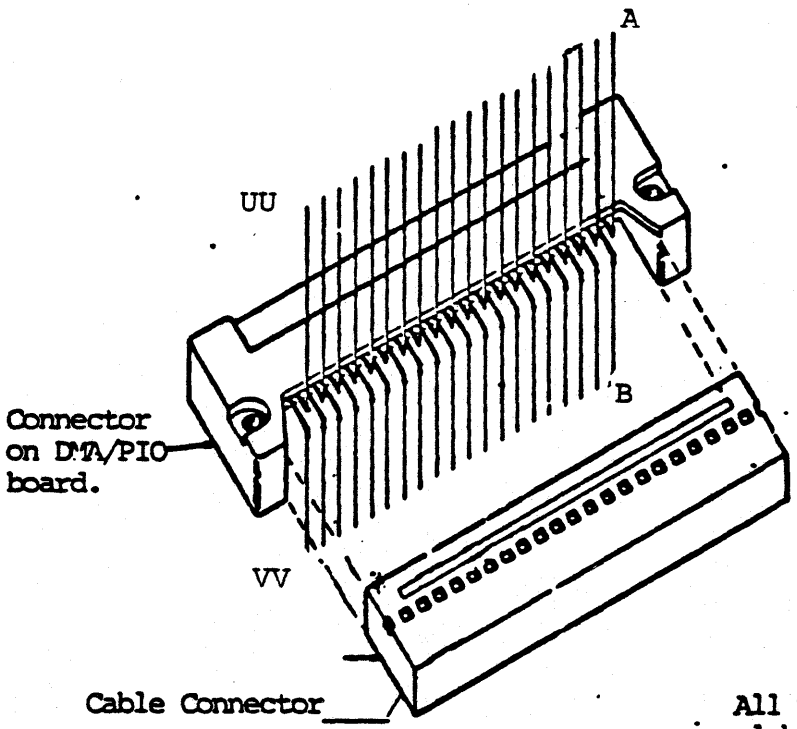
	hardware logic will execute.
SINGLE CYCLE	One TTL output line to the DEC interface. This line is pulled high on the DEC interface. When it goes low it indicates a burst mode transfer to the DEC machine.
WC-INC ENB	One TTL output line to the DEC interface. This line is normally high to enable incrementing the Bus Address Counter. Low inhibits incrementing.
BA INC ENB	One TTL output line to the DEC interface. This line is normally high to enable incrementing the bus address counter inside the DEC DMA logic. A low on this line inhibits incrementing.
CYCLE REQUEST	One TTL output line to the DEC interface. A low to high transition of this line initiates a DMA request.
ATTN	One TTL output line to the DEC interface. This line is driven high to terminate DMA transfers, to set the READY bit and request an interrupt if the interrupt enable bit is set.

* Whenever the DEC computer drives the F2 line high at the CGC interface it will cause the interrupt bit to be set and the present transfer if there is one to be terminated. This is level activated not edge.

7-3 DMA CONNECTOR PIN ASSIGNMENTS

P6 Connector Pin	Signal	P7 Connector Pin	Signal
B	CYCLE REQUEST	B	BUSY
D	INIT V2	D	ATTN
F	READY	F	A00
J	WC INC ENB	J	BA INC ENB
K	SINGLE CYCLE	K & L	FNCT 3
L	STATUS A	N	C0
N	INIT	R	FNCT 2
R	STATUS B	T	C1
T & V	STATUS C	V	FNCT 1
DD	08 IN	DD	08 OUT
FF	09 IN	FF	09 OUT
JJ	10 IN	JJ	10 OUT
LL	11 IN	LL	11 OUT
NN	12 IN	NN	12 OUT
RR	13 IN	RR	13 OUT
TT	14 IN	TT	14 OUT
VV	15 IN	VV	15 OUT
CC	07 IN	CC	07 OUT
EE	06 IN	EE	06 OUT
HH	05 IN	HH	05 OUT
KK	04 IN	KK	04 OUT
MM	03 IN	MM	03 OUT
PP	02 IN	PP	02 OUT
SS	01 IN	SS	01 OUT
UU	00 IN	UU	00 OUT

CGC 7900 DMA Connector Pin Outs
Table 7.

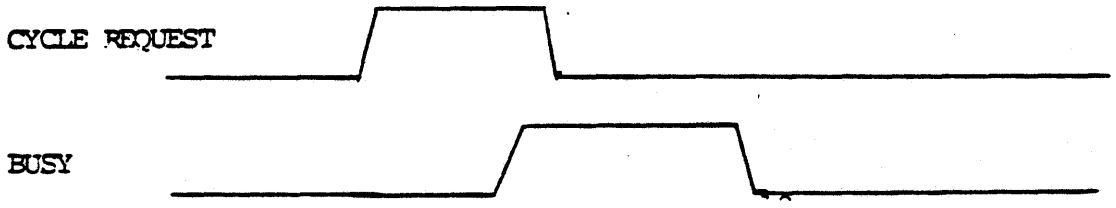


All pins are lettered in alphabetical order A thru Z and AA thru VV.
Skipping G,I,O,Q,GG,II,OO and QQ.

P6 or P7 Pin Definition
Figure 9.

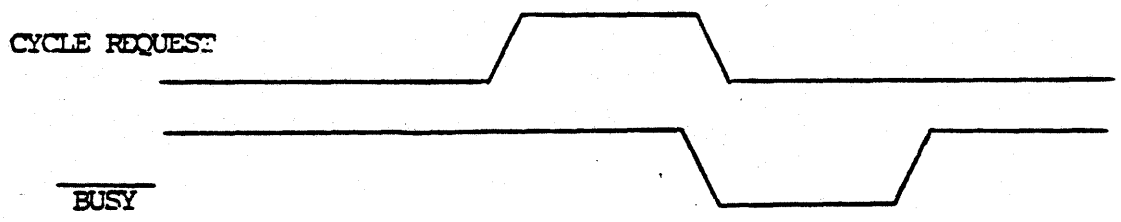
7-4 DMA JUMPER OPTIONS - There are two jumper headers that are related strictly to the DMA portion of the circuit, these are J8 and J9. These two jumpers are available in order to select the polarity of CYCLE REQUEST and BUSY at the user interface connections. The following is a description of each possibility and the exact position of each jumper for each. Refer to Figure 14 for jumper relative positions.

OPTION 1 - The first jumper configuration is the one which is to be used for the DR11-W interface. With both jumpers in their A positions a high CYCLE REQUEST and a high BUSY signal is selected meaning that the active state of these signals at the user interface will be between 2.2 volts and 5 volts.



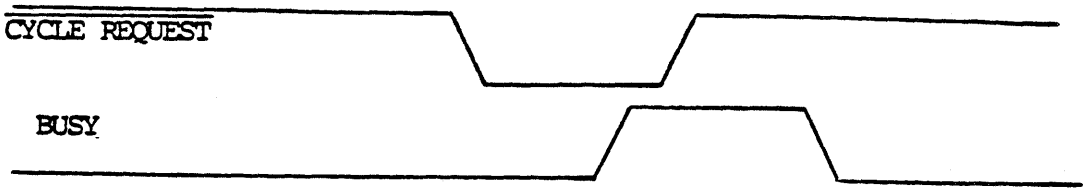
OPTION 1 Waveforms
Figure 10.

OPTION 2 - The second jumper configuration is for DRV11-B applications. With jumper J9 in its B position and jumper J8 in its A position a high CYCLE REQUEST and A low BUSY signal is selected.



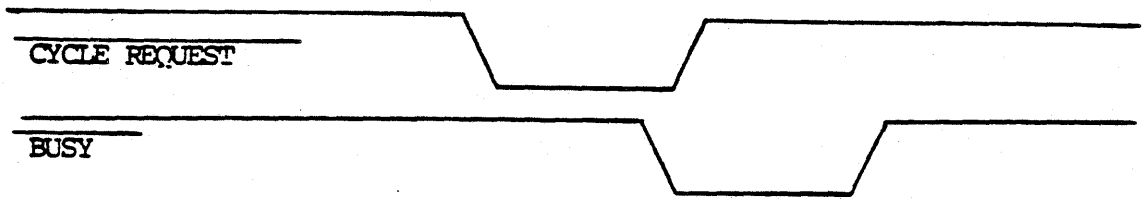
OPTION 2 Waveforms
Figure 11.

OPTION 3 - The third jumper configuration is for DR11-B applications. With jumper J8 in its position A and jumper J9 in its position B, a low CYCLE REQUEST and a high BUSY signal is selected.



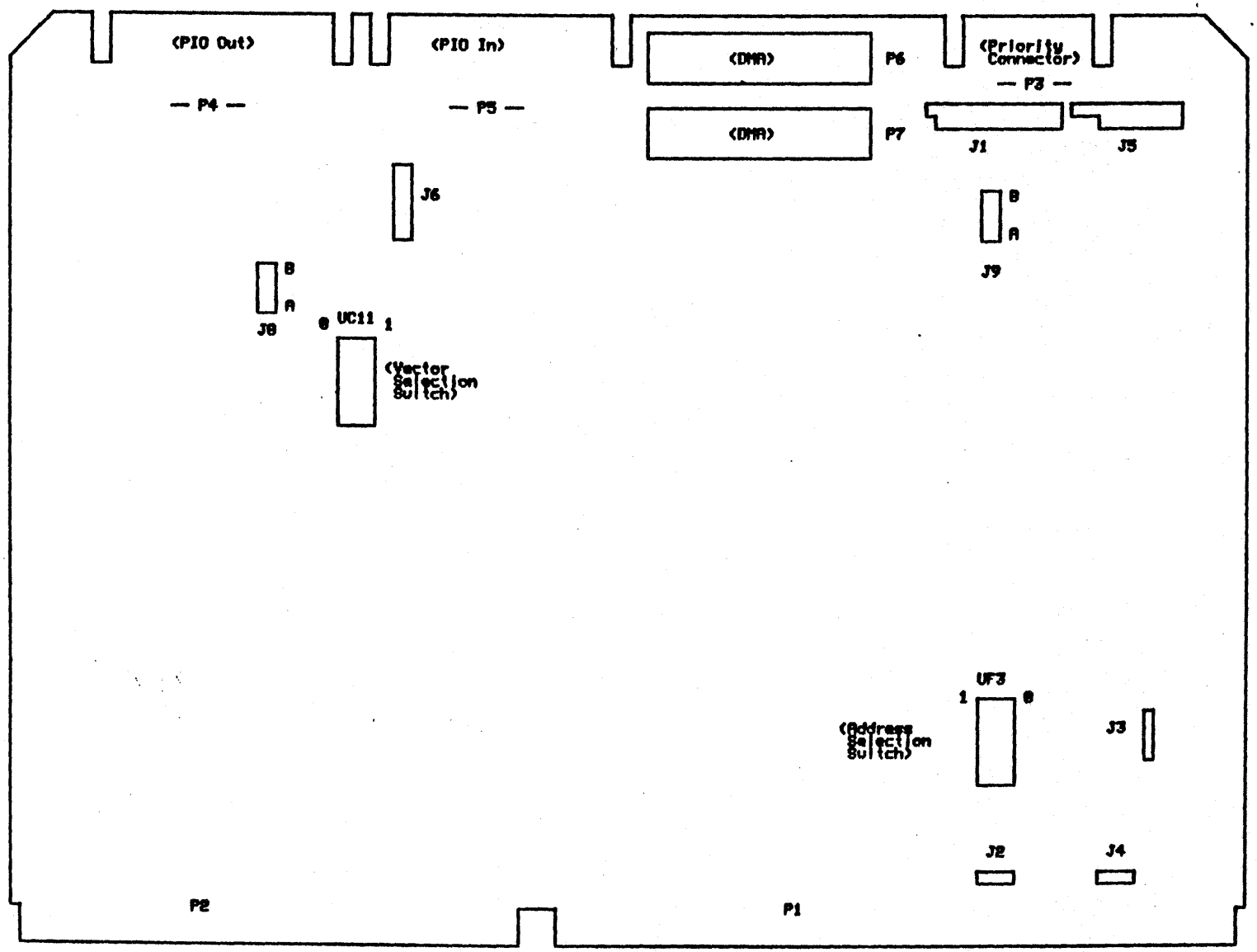
OPTION 3 Waveforms
Figure 12.

OPTION 4 - The fourth and final possibility is with both jumpers in position B. In this configuration a low CYCLE REQUEST and a low BUSY signal is selected.



OPTION 4 Waveforms
Figure 13.

NOTE: The BUSY signal in all of the above configurations must be in its inactive state in order for CYCLE REQUEST to ever go active. The above waveforms illustrate that requirement.

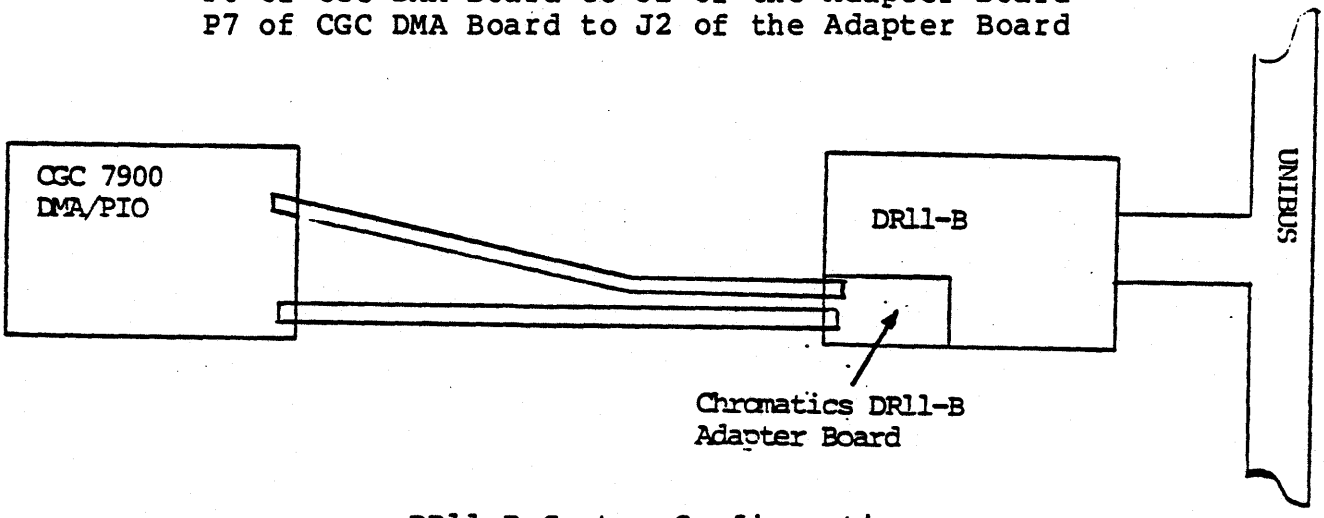


PIO/DMA Component Locations

7-5 DMA CONFIGURATIONS

CGC 7900 to DR11-B Hardware Configuration - The DR11-B is a Direct memory access I/O device which is designed to be used with DEC UNIBUS. This interface consists of a small card cage which is mounted inside the DEC computer framework. Inside the card cage is all the logic necessary to perform a DMA transfer to the DEC UNIBUS. To complete a connection from the CGC 7900 DMA board to a DEC computer having a DR11-B two operations must be performed. First the DR11-B to CGC 7900 adapter board must be inserted into the DR11-B card cage at location C and D-4. The second step is to connect up the two 40 ribbon cables as follows:

P6 of CGC DMA Board to J1 of the Adapter Board
P7 of CGC DMA Board to J2 of the Adapter Board

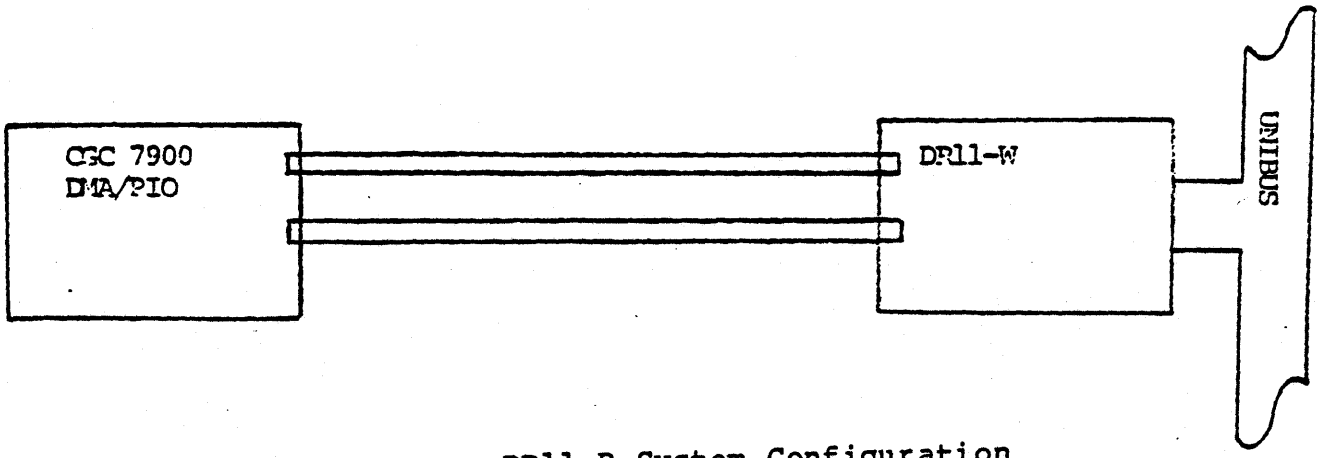


DR11-B System Configuration
Figure 15.

CGC 7900 to DR11-W Configuration

CGC 7900 to DR11-W Hardware Configuration - The DR11-W is a single board replacement for the DR11-B. It is a general purpose DMA device used to transmit data to and from the DEC UNIBUS. To complete a hook up to a DR11-W connect up the two 40 pin ribbon cables as follows:

P6 CGC 7900 DMA Board to J1 of the DR11-W
P7 CGC 7900 DMA Board to J2 of the DR11-W



DR11-B System Configuration
Figure 16.

```
Chromatics M68000 Assembler — Version 1.1 — Copyright (C) 1982

Pass #1

Pass #2

000000                  0001 *
000000                  0002 *
000000                  0003 *
000000                  0004 *
000000                  0005 *                      Appendix A
000000                  0006 *
000000                  0007 *
000000                  0008 *
000000                  0009 *
000000                  0010 *
000000                  0011         LLEN    132
000000                  0012 ************************************************************************
000000                  0013 ************************************************************************
000000                  0014 ****                                                                ****
000000                  0015 ****                                                                ****
000000                  0016 ****      Module Name : DmaDr                                       ****
000000                  0017 ****      Function    : DMA I/O driver                              ****
000000                  0018 ****                                                                ****
000000                  0019 ****                                                                ****
000000                  0020 ****      Discription - The purpose of this modlue is to            ****
000000                  0021 ****      provide an easy interface for the system programmer       ****
000000                  0022 ****      to the CGC 7900's DMA interface board.  All entrance      ****
000000                  0023 ****      and exit registers are defined below, this infor-         ****
000000                  0024 ****      along with the Users Manual should provide all the        ****
000000                  0025 ****      information needed to make use of the DMA portion         ****
000000                  0026 ****      of the DMA/PIO circuit board.                             ****
000000                  0027 ****         When this module is invoked it is assumed that         ****
000000                  0028 ****      the specified data areas have been carefully              ****
000000                  0029 ****      selected by the system programmer.                        ****
000000                  0030 ****         All Addresses are based at ff8400 if the user          ****
000000                  0031 ****      has reconfigured the adress switches the addresses        ****
000000                  0032 ****      must be changed accordingly, this also pertains           ****
000000                  0033 ****      to the Vector address selection.                          ****
000000                  0034 ****                                                                ****
000000                  0035 ****                                                                ****
000000                  0036 ************************************************************************
000000                  0037 ************************************************************************
000000                  0038 ************************************************************************
000000
```

```
                    0039          PAGE
000000              0040 *
000000              0041 *
000000              0042 *                Hardware Register Address Designations
000000              0043 *
000000              0044 *
000000              0045 PHI      EQU     $FF8400         High Data Byte Parellel Port
000000              0046 PLO      EQU     $FF8401         Low Data Byte Parelle Port
000000              0047 PSTAT    EQU     $FF8402         Status Byte for the Parellel Port
000000              0048 IMASK    EQU     $FF8403         Interrupt Mask for PIODMA board
000000              0049 ARHI     EQU     $FF8404         The High Seven Bits of Address for DMA xf
000000              0050 DMACTRL  EQU     $FF8405         Control Register for DMA Transfer
000000              0051 WCREG    EQU     $FF8406         High Byte Word Count Register DMA Transfe
000000              0052 WCLO     EQU     $FF8407         Low Byte Word Count Register DMA Transfer
000000              0053 AREG     EQU     $FF8408         High Byte (A9-A16) Address Register DMA
000000              0054 ARLO     EQU     $FF8409         Low Byte (A1-A8) Address Register DMA
000000              0055 DMADAT   EQU     $FF840A         Read DMA Data Word, Write DMA High Byte
000000              0056 DMALO    EQU     $FF840B         Write DMA Data Low Byte
000000              0057 DMASTAT  EQU     $FF840D         DMA Status Byte
000000              0058
000000
```

```
                        0059          PAGE
000000                  0060 *
000000                  0061 *              Mask Bits in The Interrupt Mask Register
000000                  0062 *
000000                  0063
000000                  0064 MRDWD    EQU     $6            Mask Interrupt Bit for Read Word
000000                  0065 MRDLO    EQU     $4            Mask Interrupt Bit for Read Low Byte
000000                  0066 MRDHI    EQU     $5            Mask Interrupt Bit for Read High Byte
000000                  0067 MWRWD    EQU     $3            Mask Interrupt Bit Write Word
000000                  0068 MWRLO    EQU     $1            Mask Interrupt Bit Write Low Byte
000000                  0069 MWRHI    EQU     $2            Mask Interrupt Bit Write High Byte
000000                  0070 MDMADON  EQU     $0            Mask interrupt Bit for DMA done
000000
```

```
                        0071          PAGE
000000                  0072 *
000000                  0073 *              Status Register Bit Definition Parellel Port
000000                  0074 *
000000                  0075
000000                  0076 IDRLO    EQU   $0           Input Data Ready Low byte
000000                  0077 IDRHI    EQU   $1           Input Data Ready High byte
000000                  0078 IDR      EQU   $2           Input Data Ready Word
000000                  0079 ODRLO    EQU   $3           Ready to Write Low Byte
000000                  0080 ODRHI    EQU   $4           Ready to Write High Byte
000000                  0081 ODR      EQU   $5           Ready to Write Word
000000
```

```
                        0082          PAGE
000000                  0083 *
000000                  0084 *                Interrupt Vector Locations
000000                  0085 *
000000                  0086
000000                  0087 Vlbytin  EQU     $20C          Interrupt Vector Low Byte Read
000000                  0088 Vhbytin  EQU     $208          Interrupt Vector High Byte Read
000000                  0089 Vwordin  EQU     $204          Interrupt Vector Word Read
000000                  0090 Vlbytwr  EQU     $218          Interrupt Vector Low Byte Write
000000                  0091 Vhbytwr  EQU     $214          Interrupt Vector high Byte Write
000000                  0092 Vwordwr  EQU     $210          Interrupt Vector Write Word
000000                  0093 Vdmadon  EQU     $21C          Interrupt Vector DMA done
000000                  0094
000000
```

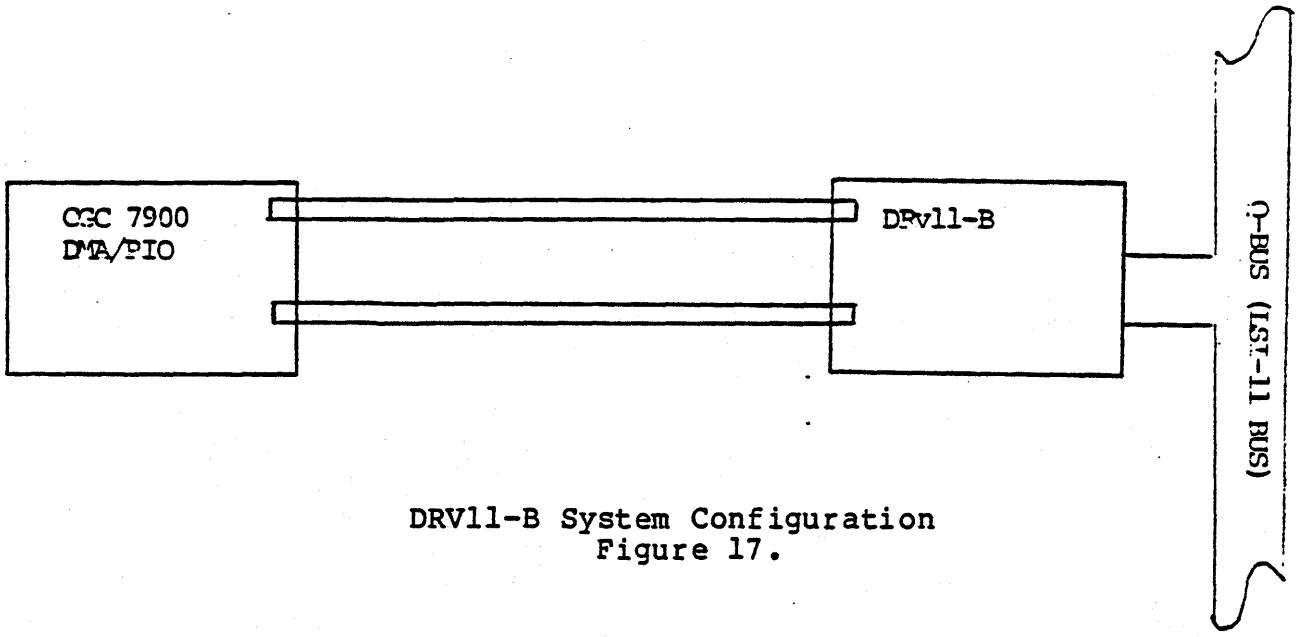
```
                        0095          PAGE
000000                  0096          ORG.L   $1F000
01F000                  0097
01F000                  0098
01F000                  0099 *
01F000                  0100 *
01F000                  0101 *
01F000                  0102 *        This subroutine actually enables the hardware
01F000                  0103 *
01F000                  0104 *        Enter with:
01F000                  0105 *              D0 = 0 for a DMA read; 1 for a DMA write
01F000                  0106 *              D1 = Number of words to be transferred
01F000                  0107 *              D2 = Byte address to start transfer (buffer pointer)
01F000                  0108 *              D3 = Vector Address Location
01F000                  0109 *
01F000                  0110 *        Exit with:
01F000                  0111 *
01F000                  0112 *              <Registers unchanged>
01F000                  0113 *
01F000                  0114 *
01F000 0839000000FF
            840D        0115 DMA      BTST    #0,DMASTAT      Reset the interrupt
01F008 48E7F000         0116          MOVEM.L D0-D3,-(SP)     Save the registers
01F00C 23C30000021C     0117          MOVE.L  D3,Vdmadon      Set up the Vector address
01F012 E788             0118          LSL.L   #$3,D0          Get the read/write bit in position
01F014 008000000020     0119          OR.L    #$20,D0         Or in the Single Cycle bit
01F01A 13C000FF8405     0120          MOVE.B  D0,DMACTRL      Write to control register
01F020                  0121 *
01F020 4441             0122          NEG.W   D1              Get the 2's complement of the word count
01F022 33C100FF8406     0123          MOVE.W  D1,WCREG        Set up the word count register
01F028                  0124 *
01F028 E28A             0125          LSR.L   #1,D2
01F02A 33C200FF8408     0126          MOVE.W  D2,AREG         Set up low 16 bits of address
01F030 4842             0127          SWAP    D2              Get the upper seven in lower eight
01F032 13C200FF8404     0128          MOVE.B  D2,ARHI         Write out hi seven bits of the address
01F038 4CDF000F         0129          MOVEM.L (SP)+,D0-D3     Restore the registers
01F03C                  0130 *
01F03C 4E75             0131          RTS
01F03E                  0132 *
01F03E                  0133 *        A write to the High address register initiates the transfer
01F03E                  0134 *
01F03E                  0135 *
01F03E                  0136          END     DMA
01F03E                  0137 *
01F03E                  0138 *
01F03E                  0139 *
01F03E                  0140 *
01F03E                  0141
01F03E                  0142
01F03E                  0143
01F03E                  0144

Error Count : 0000
```

CGC 7900 to DRV11-B Configuration

The DRV11-B is a general purpose DMA device used to transfer data to and from the DEC Q-BUS. This is the bus which is used in LSI-11 computer systems. The DRV11-B is a single board which plugs directly into the Q-BUS. To complete a hook up to the DRV11-B the two 40 pin ribbon cables must be installed as follows:

P6 of the CGC 7900 DMA board to J1 of the DRV11-B
P7 of the CGC 7900 DMA board to J2 of the DRV11-B



DRV11-B System Configuration
Figure 17.