CONTROL DATA CORPORATION

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# CONTROL DATA®

# LARK™ POWER SUPPLY AND I/O ADAPTER (PIO)

GENERAL DESCRIPTION
OPERATION
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

MAGNETIC PERIPHERALS INC.
a subsidiary of
CONTROL DATA CORPORATION

## MODULE I

HARDWARE MAINTENANCE MANUAL

# PREFACE

Module I of this manual provides the information needed to install, operate, maintain, and troubleshoot the Power Supply and I/O Adapter (PIO), when used with the 50MB Lark Micro Unit (LMU).

This module is a compilation of Control Data Corporation's PIO Hardware Installation/Operation Manual (# 77711033) and PIO Hardware Maintenance Manual (# 77711038).

The total content of this module is comprised of seven sections:

| SECTION | TITLE |
|---|---|
| 1 | GENERAL DESCRIPTION |
| 2 | OPERATION |
| 3 | INSTALLATION AND CHECKOUT |
| 4 | THEORY OF OPERATION |
| 5 | DIAGRAMS |
| 6 | MAINTENANCE |
| 7 | PARTS DATA |

NOTE

The Lark Micro Unit (LMU) and the Power Supply & I/O Adapter (PIO) are separate and distinct devices, with their own unique documentation. The LMU is identified as Model 9454 (the 16MB unit) or 9457 (the 50MB unit). The 16MB unit is used with the No Problem Shared System™ and requires Lanier Service Manual Z-200-299 for the PI/O and Z-200-300 for the Model 9454 Micro Unit. This manual on the 50MB unit consists of three modules--Module I covers the PI/O, Module II covers the Model 9457 Micro Unit, and Module III contains a listing of the Lark Status Codes.

EMI NOTICE: This equipment has been designed as a component to high standards of design and construction. The product, however, must depend on receiving adequate power and environment from its host equipment in order to obtain optimum operation and to comply with applicable industry and governmental regulations. Special attention must be given by the installers and CSRs in the areas of safety, input power, grounding, shielding, and environment temperature of the device to insure specified performance and compliance with all applicable regulations.

## OPERATOR SAFETY INSTRUCTIONS

1. This unit is designed for use with the Lark Micro Unit.

2. The unit is to be installed according to the installation instructions.

3. The power plug must be connected to a power source that has the protection of not greater than 16 amps. The power plug is to be used as the disconnect device.

4. The unit is to be operated in an ambient temperature between 10° C and 40° C.

5. This unit is to be serviced by qualified technical personnel only after pulling the power plug.

## BENUTZER SICHERHEITSANWEISUNG

1. Dieses Netzgerat ist nur in Verbindung mit dem Magnetplattenalufwerk Lark Micro Unit zu verwenden.

2. Die Zusammenschaltung wird wie im Manual unter "Installations Information" beschrieben, vorgenommen.

3. Die Netz - Stromversorgung wird uber eine Steckdose mit nicht mehr als 16A Absicherung vorgenommen.

4. Das Netzgeraet ist konstruiert fur eine Umgebungstemperature von 10°C bis 40° C.

5. Reparaturen am Netzgerat sind nur von qualifizierten Service Technikern, nach Adschalten bzw. durch Ziehen des Netzsteckers, vorzunehmen.

# MODULE I

## TABLE OF CONTENTS

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## 1.1 INTRODUCTION

The LARK ™ Power Supply and Adapter Assembly (PIO) provides the LARK Micro Unit with DC and AC power and provides it with the CDC Module family interface to the host controller.

## 1.2 GENERAL DESCRIPTION

The PIO consists of a power supply section and a section for the I/O Adapter PWA. See Figure 1-1. The power supply furnishes power to the LARK Micro Unit and also to the I/O Adapter PWA. Voltages generated for the drive are +5 V, -5.2 V, +16.5 V, and -16.5 V. The I/O PWA requires +5 V and -5.2 V. The power supply also provides AC voltage for the LMU.

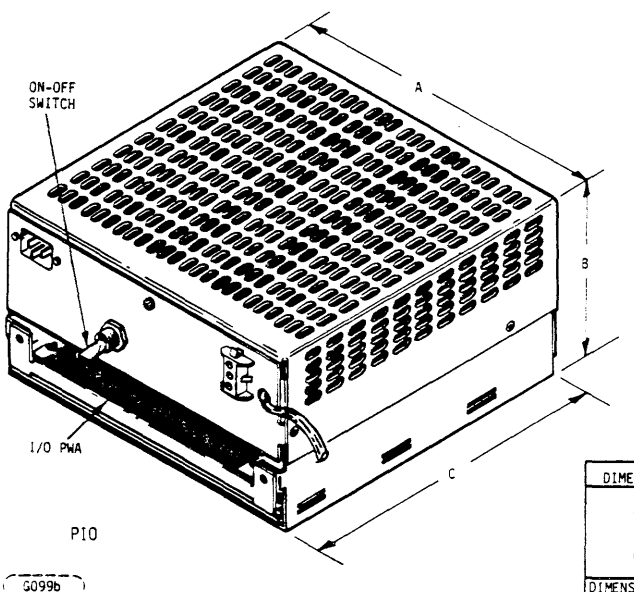
The I/O PWA converts the external SMD interface to an internal microcomputer based interface. The PWA also provides proper line termination and noise isolation for both interfaces.

NOTE

The PIO is a component and therefore does not require a FCC label.

## 1.3 FUNCTIONAL BLOCK DIAGRAM

A functional block diagram is shown in Figure 1-2. The power supply regulator circuitry is mounted on a single PWA within the power supply section. The I/O Adapter circuitry is mounted on one PWA in a section below the power supply. The Terminator PWA plugs into the I/O PWA.




WEIGHT = APPROX. 15 lbs (6.75 Kg)

| DIMENSION | in. | mm |
|---|---|---|
| A | 8.58 | 217.9 |
| B | 4.63 | 117.6 |
| C | 10.0 | 254.0 |
| DIMENSIONS DO NOT INCLUDE A "FRONT" PANEL | | |
| WEIGHT - 15 LBS. (6.75 kg) | | |

FIGURE 1-1. PIO PHYSICAL CHARACTERISTICS

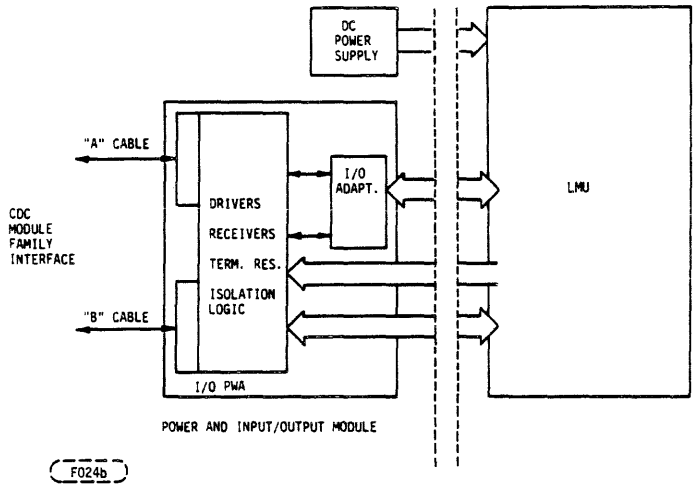



FIGURE 1-2. FUNCTIONAL BLOCK DIAGRAM

## 2.1 INTRODUCTION

This section provides the instructions and information required to operate the Lark Module Drive PIO.

## 2.2 CONTROLS

The only control on the PIO is the AC power ON/OFF switch shown in Figure 2-1. This switch operates the AC power circuit breaker CB-1. This switch is not available to the equipment operator. It is expected that only maintenance personnel will operate the ON/OFF switch.

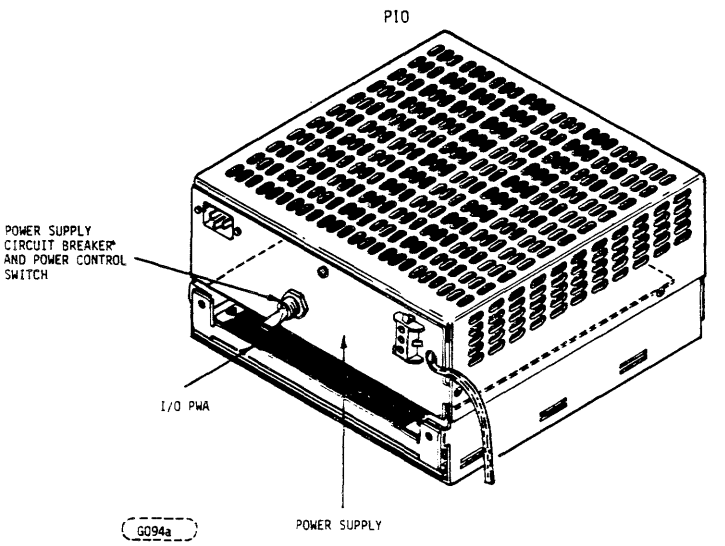



FIGURE 2-1. OPERATOR CONTROLS

## 3.1 INTRODUCTION

This section provides the information and procedures necessary to install the PIO.

## 3.2 UNPACKING

During unpacking, exercise care so that tools being used do not cause damage to the unit. As the unit is unpacked, inspect it for possible shipping damage. All claims for this type of damage should be filed promptly with the transporter involved.

Retain the shipping container and packing material if a claim is to be filed for damage, unit is to be reshipped, or shipped to service center.

Unpack the unit as follows:

a. Remove the tape from the shipping container.

b. Open the container and remove the PIO and cables.

c. Do not connect the input power cable between the PIO and LMU until all other installation steps have been completed and the LMU is ready for initial checkout.

## 3.3 SPACE ALLOCATION

Figure 1-1 shows the PIO overall dimensions for determining space allocation. Detailed mounting hole data is provided in Figure 3-1. Example configurations are shown in Figure 3-2. Interconnecting cables are supplied to interface the PIO to the LMU.

The PIO is designed so that, in its final installed configuration, only a blank front panel (to be furnished by the user) is to be accessible to the equipment operator.

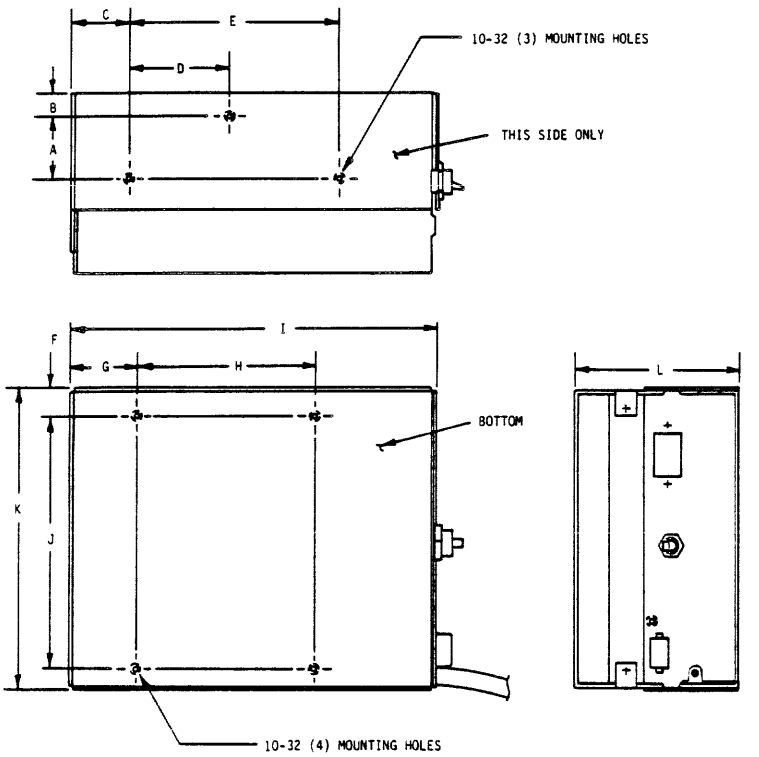
## 3.4 PIO COOLING

The PIO is cooled by means of convection. Thus, the ambient temperature of incoming air near the bottom of the PIO must not exceed 104°F (40°C) when measured within 1/2 inch of the PIO enclosure.

## 3.5 POWER REQUIREMENTS

### 3.5.1 PRIMARY POWER REQUIREMENTS

The primary voltage and current requirements are shown in Tables 3-1 and 3-2 for one PIO and one LMU. The operational line currents are described in Figure 3-3.




NOTE

PENETRATION OF MOUNTING HARDWARE NOT TO EXCEED 0.25 in (6.35 mm). DIMENSIONS DO NOT INCLUDE USER FURNISHED FRONT PANEL

| DIMENSION | INCHES | mm |
|---|---|---|
| A | 1.50 | 38.1 |
| B | 0.69 | 17.5 |
| C | 1.75 | 44.5 |
| D | 2.50 | 63.5 |
| E | 5.75 | 146.1 |
| F | 0.54 | 13.7 |
| G | 1.81 | 46.0 |
| H | 4.88 | 123.8 |
| I | 10.0 | 254.0 |
| J | 7.50 | 190.5 |
| K | 8.57 | 217.7 |
| L | 4.63 | 117.6 |

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FIGURE 3-1. PIO MOUNTING HOLE DATA

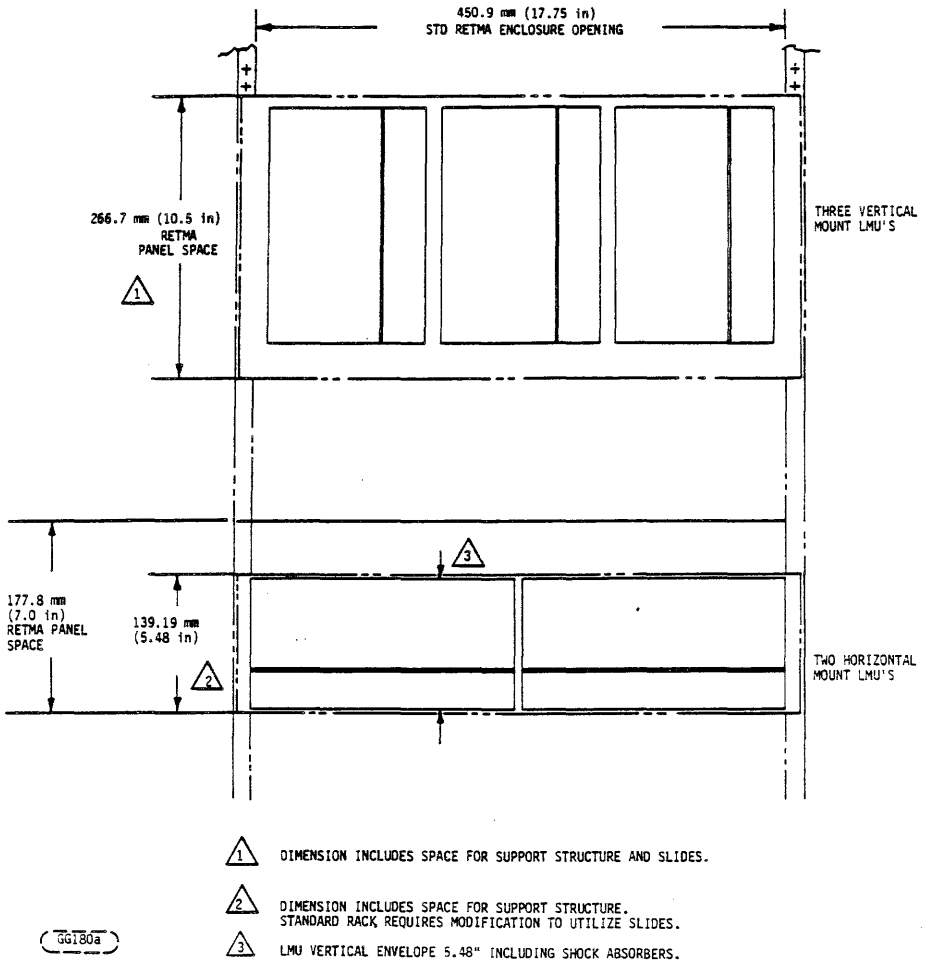



FIGURE 3-2. EXAMPLE LMD CONFIGURATIONS

## 3.5.2 POWER CABLE AND MATING CONNECTOR

The AC power cable supplied with the PIO is 7.5 feet (2.29 meters) long. The cable connector plug requiring a mating receptical is described as follows:

| DESCRIPTION | CDC P/N | NEMA Configuration |
|---|---|---|
| 120 V, 15 A, 60 Hz, 2-pole, 3-wire receptacle connector at PIO end, 2-pole, 3-wire plug connector at power source end (see Figure 3-4). | 75778702 | 5-15 P |

The mating receptacle connector required at the AC power source is NEMA Configuration: 5-15R

A color-coded power cable is supplied with the 50 Hz drive, but the 50 Hz power source end connector must be furnished by the user. The cable color code and unit power requirements are as follows:

| DESCRIPTION | | COLOR-CODE | |
|---|---|---|---|
| 220-240 V 50 Hz | Brown | - Phase One | |
| | Blue | - Neutral | #18 AWG |
| | Green and Yellow | - AC Equipment Ground | WIRE |

Do not connect the AC power cable between power source and PIO until all other installation steps have been completed and the drive is ready for initial checkout.

The PIO 60 Hz power supply contains two fuses and the PIO 50 Hz power supply contains four fuses located inside the chassis. Refer to the Maintenance Manual section 6 for removal and replacement procedures.

## 3.6 CABLING AND FEATURE SELECTION

The connectors for interfacing the PIO to the controller and LMU to the PIO as well as the drive address selection switch are located on the I/O board. Remove the I/O board as follows:

1. Remove the two screws holding the I/O board in the PIO base pan (see Figure 3-5).
2. Slide out the I/O board until the I/O connectors and drive address selection switch are accessible.

The I/O board is now ready to accomplish drive address selection, terminator board installation and cabling.

TABLE 3-1. PRIMARY VOLTAGE REQUIREMENTS *

| VOLTAGE (VAC) | TOLERANCE (VAC) | FREQUENCY (Hz) | TOLERANCE (Hz) |
|---|---|---|---|
| 120 | -16, +8 | 60 | +0.5, -1.0 |
| 220-240 | -29, +16 | 50 | +0.5, -1.0 |

TABLE 3-2. CURRENT/POWER REQUIREMENTS *

| DRIVE INPUTS | CURRENTS AND (WATTAGE) | | | | | |
|---|---|---|---|---|---|---|
| | ON TRACK | | SEEKING | | STARTING | |
| | NOMINAL | MAXIMUM | NOMINAL | MAXIMUM | NOMINAL | MAXIMUM |
| 120 VAC | 0.7 A (60 W) | | 0.7 A (60 W) | | | |
| 220-240 VAC | 0.35 A (60 W) | | 0.35 A (60 W) | | | |
| +16.5 V | 0.4 A (6.6 W) | | 0.72 A (11.9 W) | | - | - |
| -16.5 V | 0.35 A (5.8 W) | | 0.67 A (11.1 W) | | - | - |
| +5 V | 1.4 A (7.0 W) | | 1.4 A (7.0 W) | | - | - |
| -5 V | 2.88 A (14.4 W) | | 2.88 A (14.4 W) | | - | - |
| TOTAL WATTAGE | (94.4 W) | | (104.4 W) | | - | - |
| I/O INPUTS | | | | | | |
| +5.0 V | 0.9 A (4.5 W) | | 0.9 A (4.5 W) | | | |
| -5.0 V | 0.3 A (1.5 W) | | 0.3 A (1.5 W) | | | |
| TOTAL WATTAGE | (6.0 W) | | (6.0 W) | | | |
| POWER SUPPLY INPUTS | RUN CURRENT | | START CURRENT | | START TIME (SECONDS) | |
| | NOMINAL | MAXIMUM | NOMINAL | MAXIMUM | NOMINAL | MAXIMUM |
| 120 VAC | 1.18 A (142 W) | | 1.6 A (192 W) | | 60 | |
| 220-240 | 0.7 A (154 W) | 0.9 A (200 W) | 0.9 A (203 W) | | 60 | |

* Combined LMU and PIO requirements.

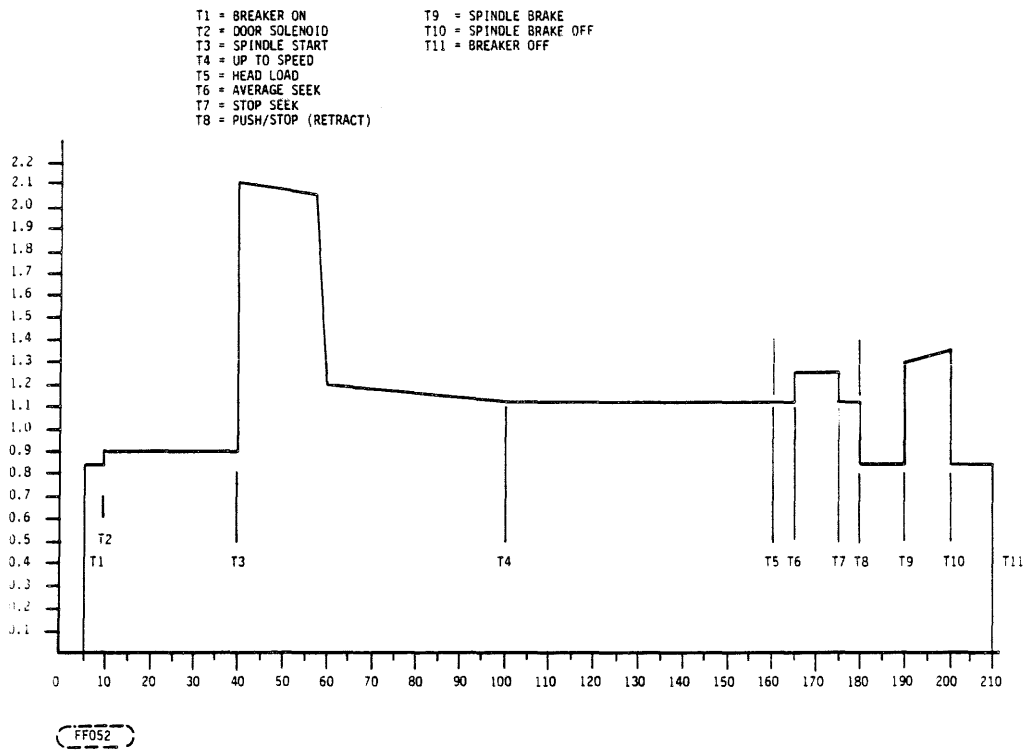



FIGURE 3-3. OPERATIONAL NOMINAL LINE CURRENTS TO POWER SUPPLY VS TIME (120 V INPUT)

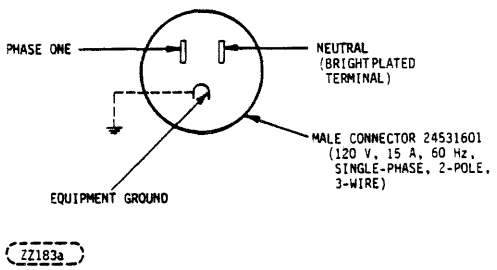



FIGURE 3-4. INPUT POWER CABLE CONNECTOR PLUG (120 V 60 HZ POWER SOURCE END)

## 3.6.1 FEATURE SELECTION

The PIO is provided with a dip switch module which allows a binary address to be selected to operate in a multiple drive system. The drive can only be selected as unit 0 through 3. The dip switch module is located in the I/O board in the PIO (see Figure 3-5).

## 3.6.2 RADIAL OR DAISY-CHAIN SELECTION

Figure 3-6 shows the intercabling and terminator placement for various drive arrangements. Shown are the radial daisy chained systems configurations. A single drive is connected as shown for the radial configuration.

Insure the terminator PWA is plugged into the PIO I/O Board (J2) and the connector ejector arms are closed (see Figure 3-5).

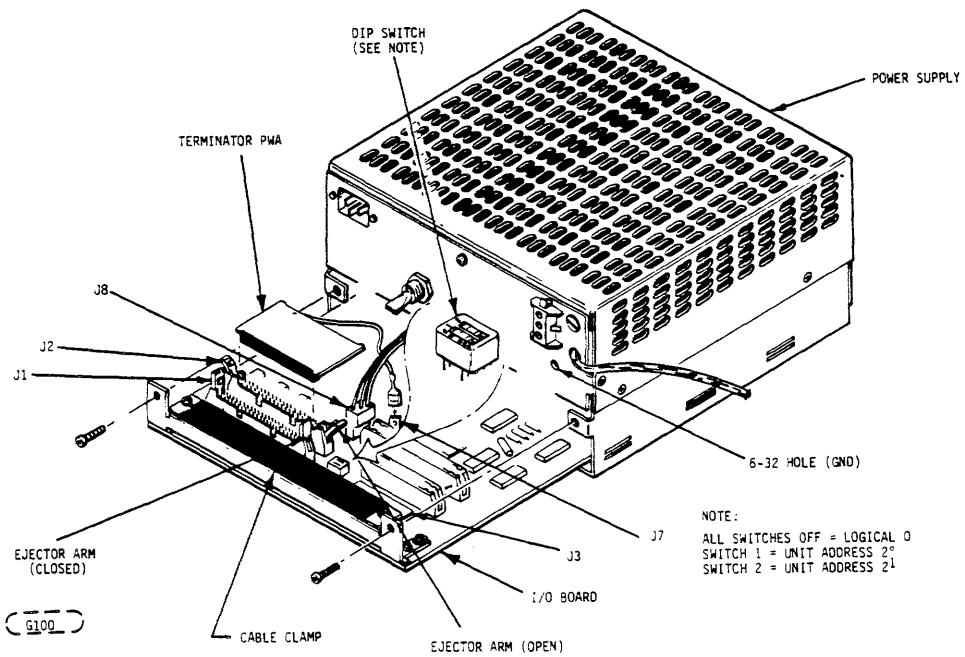
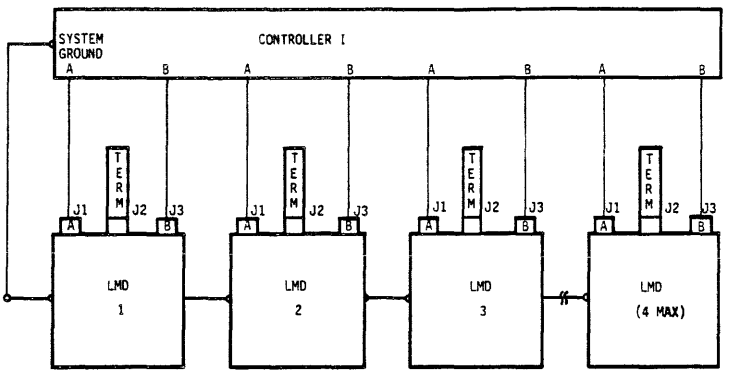



FIGURE 3-5. POWER SUPPLY AND I/O BOARD

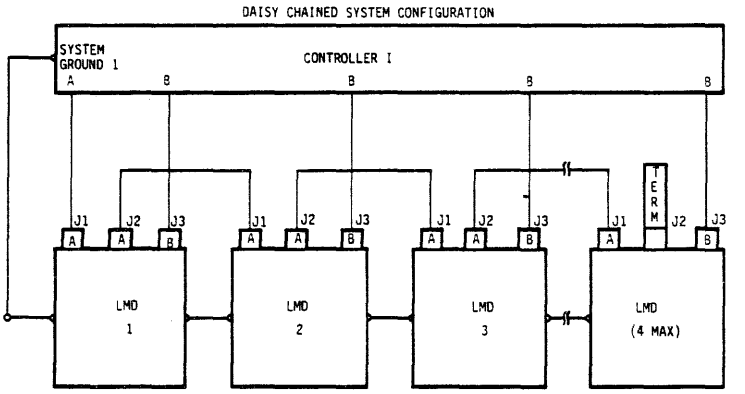
RADIAL SYSTEM CONFIGURATION




NOTES

1. MAXIMUM TOTAL A CABLE LENGTHS = 100 FEET (30.48 METERS)
2. MAXIMUM INDIVIDUAL B CABLE LENGTHS = 50 FEET (15.24 METERS)

DAISY CHAINED SYSTEM CONFIGURATION




NOTES

1. TERMINATION OF "A" CABLE LINES ARE REQUIRED AT CONTROLLER AND THE LAST UNIT OF THE DAISY CHAIN OR EACH UNIT IN A RADIAL CONFIGURATION.
2. TERMINATION OF "B" CABLE RECEIVER LINES ARE REQUIRED AT THE CONTROLLER AND ARE ON THE UNIT'S RECEIVER CARDS.
3. MAXIMUM CUMULATIVE A CABLE LENGTH PER CONTROLLER = 100 FEET (30.48 METERS) MAXIMUM INDIVIDUAL B CABLE LENGTH = 50 FEET (15.24 METERS).

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FIGURE 3-6. LMD SYSTEM CABLING

### 3.6.3 LMU TO PIO INTERCABLING

Four cables are used to connect the LMU to the PIO: unshielded cables can be used for lengths of 4 feet or less. Shielded cables must be used for lengths between 4 feet and 10 feet (maximum length).

1. One 40 Conductor Flat Ribbon Cable ("C" Cable).
2. One 26 Conductor Flat Ribbon Cable ("D" Cable).
3. One AC Power Cable (3-Wire).
4. One DC Power Cable (6-Wire, Part of PIO).

Connect these cables as follows: (See Figure 3-7)

1. Remove two screws holding AC Distr PWA Cover in place and remove the cover.
2. Connect 40 conductor clat ribbon ("C") cable between LMU Base PWA (J1 on Base PWA) and PIO I/O PWA (J4).
3. Connect 26 conductor flat ribbon ("D") cable between LMU Base PWA (J2) and PIO I/O PWA (J5).
4. Connect DC power cable for PIO to LMU Base PWA (J3).
5. Connect AC power cable between LMU AC Distr PWA (J1) and PIO Power Supply.
6. Reinstall AC Distr PWA Cover.

### 3.6.4 PIO TO CONTROLLER CABLING

Standard SMD/CMD flat "A" and "B" cables can be used to interface the PIO to the controller. Refer to Section 3-10 "ACCESSORIES" for applicable cable/ connector part numbers and cable length restrictions. The connector pin and signal name assignments are shown in Figures 3-8 and 3-9. Figure 3-10 is a table that shows the decoding of the TAG bus lines.

Install the cables as follows: (See Figures 3-5 and 3-7)

1. Connect "A" cable to PIO I/O PWA (J1) and close connector ejector arms.

2. Connect "B" cable to PIO I/O PWA (J3). Ensure connectors are oriented correctly on I/O PWA i.e., Pin 1 to Pin 1.

3. Connect other end of cables (Steps 1 and 2) to controller.

4. Route all cables through cable clamp on I/O PWA.

CAUTION

Insure J1 and J2 connector ejector arms are fully closed before reinstalling I/O PWA.

5. Reinstall I/O PWA in base pand of power supply.

### 3.6.5 I/O AND POWER CABLE ROUTING

For sliding rack mounted drives, it is recommended that a cable retract mechanism be incorporated in the rack design. Retract mechanisms can be purchased from a number of available manufacturers.

## 3.7 GROUNDING

Connect a low impedance ground strap, 19 mm (0.75 in) braid, from controller system ground-to-PIO (GND on front plate)-to-LMU casting.

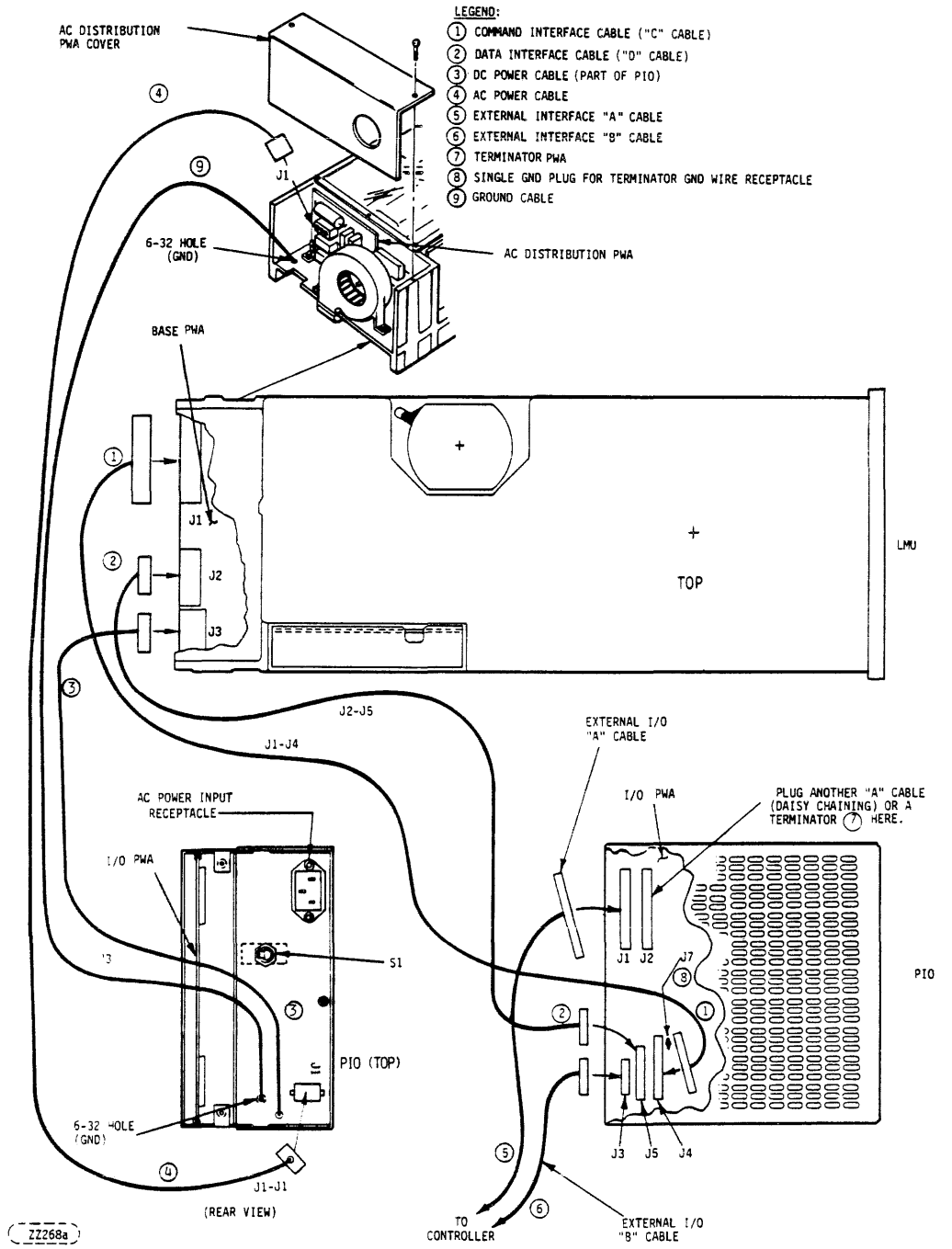
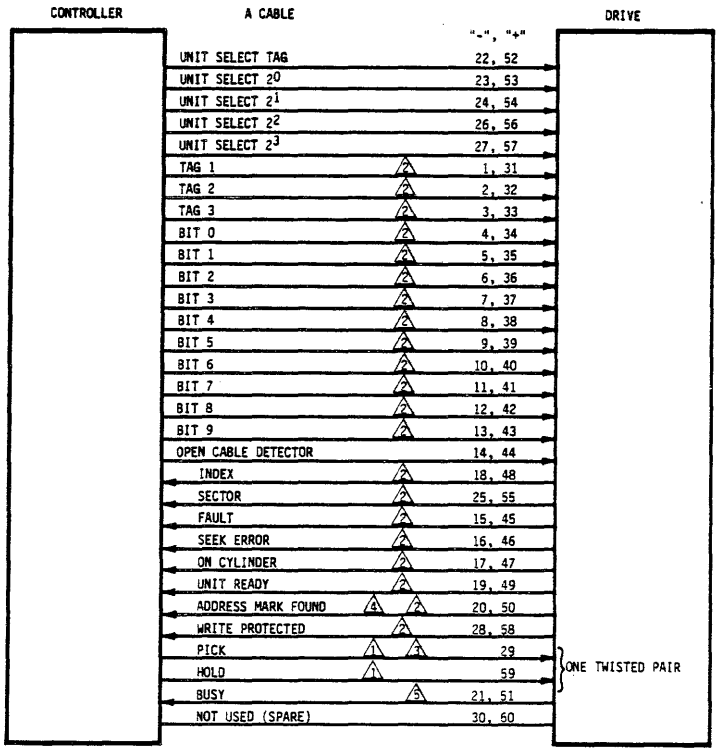



FIGURE 3-7. LMD CABLE CONNECTIONS




NOTE: 60 POSITION
30 TWISTED PAIR - STRAIGHT FLAT CABLE
MAXIMUM LENGTH - 100 FT (30.48 METERS) (CUMULATIVE)

1. SPECIAL SIGNAL, NOT A BALANCED TRANSMISSION SIGNAL
2. GATED BY UNIT SELECTED
3. NOT INTERPRETED, IS DAISY CHAINED, NO DRIVER CONNECTION WITHIN THE LMD.
4. NOT ACTIVATED, IS DAISY CHAINED, ALWAYS A LOGIC ZERO OUTPUT IF UNIT IS SELECTED
5. NOT GENERATED, IS DAISY CHAINED, NO DRIVER CONNECTION WITHIN THE LMD

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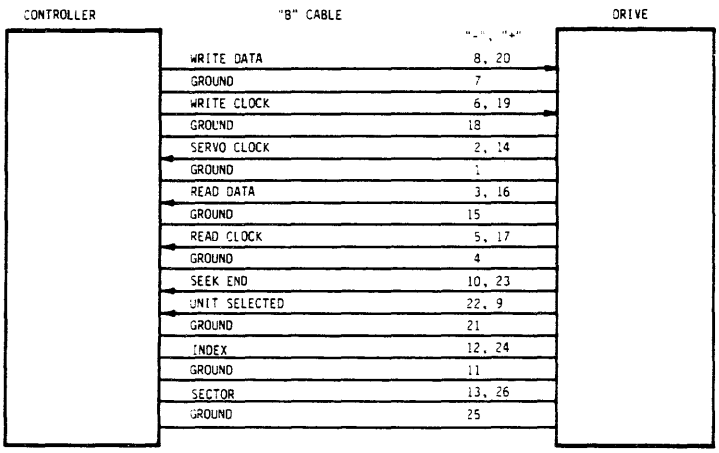
FIGURE 3-8. TAG BUS I/O INTERFACE ("A" CABLE)




NOTES: 1. 26 CONDUCTOR FLAT CABLE.
MAXIMUM LENGTH - 50 FT. (15.24 METERS)

2. NO SIGNALS GATED BY "A" CABLE UNIT SELECT.

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FIGURE 3-9. "B" CABLE INTERFACE

| | TAG 1 | TAG 2 | TAG 3 |
|---|---|---|---|
| BUS | CYLINDER ADDRESS | HEAD/VOLUME SELECT | CONTROL SELECT |
| BIT 0 | $2^0$ | $2^0$ (1) | WRITE GATE |
| BIT 1 | $2^1$ | $2^1$ (1) | READ GATE |
| BIT 2 | $2^2$ | (2) | SERVO OFFSET PLUS |
| BIT 3 | $2^3$ | (2) | SERVO OFFSET MINUS |
| BIT 4 | $2^4$ | (2) | FAULT CLEAR |
| BIT 5 | $2^5$ | (2) | (2) |
| BIT 6 | $2^6$ | (2) | RTZ |
| BIT 7 | $2^7$ | (2) | DATA STROBE EARLY |
| BIT 8 | $2^8$ | (2) | DATA STROBE LATE |
| BIT 9 | $2^9$ | (2) | (2) |

(1) HEAD CHANGES ARE NOT INITIATED UNTIL A VALID SEEK IS RECEIVED FOLLOWING A HEAD CHANGE COMMAND IF THE SEEK-ON-HEAD-CHANGE OPTION IS NOT SELECTED. IF THE SEEK-ON-HEAD-CHANGE OPTION IS SELECTED, THE HEAD CHANGES AND A ZERO DISTANCE SEEK WILL BE INITIATED AS A RESULT OF THE HEAD CHANGE.

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(2) NOT INTERPRETED BY THE LMD.

FIGURE 3-10. TAG BUS DECODE

## 3.8 ENVIRONMENT

Temperature

a. Operating

50°F (10.0°C) to 104°F (40°C) with a maximum gradient of 18°F (10°C) per hour. Maximum operating temperature should be reduced as a function of altitude by 1.95°F/1000 ft. (1.08° C/304.8 m).

b. Transit Temperatures

-40°F (-40.4°C) to 158°F (70.0°C) with a maximum gradient of 36°F (20°C) per hour. This specification assumes that the PIO is packaged in the shipping container designed by manufacturer for use with the PIO.

c. Storage Temperature

14°F (-10°C) to 122°F (50.0°C) with a maximum gradient of 27°F (15.°C) per hour.

Relative Humidity

a. Operating

20% to 80% RH (providing there is no condensation) with a maximum gradient of 10% per hour.

Transit (as packed for shipment)

5% to 95% (providing there is no condensation).

b. Storage 10% to 90% (providing there is no condensation).

c. Altitude (actual or effective)

1. Operating

983 ft (300 m) below sea level to 6560 ft (2000 m) above sea level.

2. Transit (as packed for shipment)

983 ft (300 m) below sea level to 8200 ft (2500 m) above sea level.

## 3.9 INITIAL CHECKOUT AND STARTUP PROCEDURE

This procedure should be used to make the first power application to the LMD. The procedure assumes that the preceding procedures and requirements of this section have been performed. (LMU to PIO cabling - 3.6.3) (PIO to controller cabling - 3.6.4).

1. Insure system AC power circuit breaker is OFF.
2. Insure PIO power switch is positioned to OFF.
3. Verify LMU START/STOP switch is in STOP (out) position.
4. Unscrew LMU carriage locking pin (CCW direction) until head of screw is flush with top of cover (see Figure LMU Installation/Operation Manual). Resistance to turning will be felt as locking pin nears the correct position.
5. Install the AC power cable between power source and PIO AC power input receptical.
6. Turn on Subsystem AC power circuit breaker.
7. Position PIO AC power switch to ON. The LMU cooling fan should operate and front panel door should unlock when START/STOP switch is in STOP position (out).
8. Verify proper disk cartridge is available and insert into LMU.
9. Operate LMU START/STOP switch to START (in). Spindle motor should rotate. Head loading sequence is initiated, START/STOP indicator blinks until heads are loaded then, remains illuminated. Also, front panel door locks when spindle rotation begins.
10. Perform on-line diagnostics, as applicable.

## 3.10 ACCESSORIES

### 3.10.1 I/O INTERFACE ACCESSORIES-PIO TO/FROM CONTROLLER

I/O Interface PIO to Controller Accessory items required, but not furnished with the device unless specifically ordered are shown in Table 3-3 and 3-4.

TABLE 3-3. EXTERNAL I/O CABLES AND TERMINATOR PART NUMBERS

| CABLE | QUANTITY | | PART NO. |
|---|---|---|---|
| "A" Cable (Controller to PIO) (Same connector on each end. See Paragraph 3.10.2) | One per PIO in radial, one per multispindle installation in Daisy chain. | ⚠ | 775642XX |
| "A" Cable (PIO to PIO) (Same connector on each end. See Paragraph 3.10.2) | One less than total devices in the Daisy chain. | ⚠ | 775642XX |
| "B" Cable (Controller to PIO) | One per PIO | ⚠ | 775643XX |
| Terminator | One per PIO in radial, one per multispindle installation in Daisy chain (One is provided with each I/O PWA). | | 75886100 |
| ⚠ Last two digits denote length. (For cable length, see Table 3-4). | | | |

TABLE 3-4. I/O CABLE LENGTH AND TABS

| | PART NO. | CABLE LENGTH IN METERS / FEET | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1.52 / 5 | 1.83 / 6 | 2.44 / 8 | 3.05 / 10 | 4.58 / 15 | 6.96 / 20 | 7.63 / 25 | 9.15 / 30 | 12.2 / 40 | 15.24 / 50 |
| TAB (XX) | "A" Cable 775642XX | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 |
| | "B" Cable 775643XX | 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | 08 | 09 |

## 3.10.2 I/O CABLE CHARACTERISTICS AND CONNECTOR PART NUMBERS

### 3.10.2.1 "A" CABLE

| ITEM* | DESCRIPTION | CDC P/N | BERG P/N | SPECTRA-STRIP P/N |
|---|---|---|---|---|
| 1 | Connector (60 Pos) | 94361115 | 65043-007 | |
| 3 | Contact, Insert | 94245603 | 48048 | ---------- |
| 2 | Flat Cable (twisted-pair), 30 pair, 28 AWG | 95043902 | | 138-2899-992 |

"A" Cable Mating Receptacle on Unit or Controller.

*These cables are for in-cabinet use only.

| ITEM | DESCRIPTION | CDC P/N | 3M P/N |
|---|---|---|---|
| 4 | 60 pin, vertical header | 91904653 | 3372-2302 |

### 3.10.2.2 "B" CABLE

| ITEM* | DESCRIPTION | CDC P/N | 3M P/N |
|---|---|---|---|
| 5 | Connector (26 pos.) | 65853402 | 3399-3000 |
| 6 | Connector Pull Tab | 92004801 | 3490-2 |
| 7 | Flat Cable (26 pos.) with ground plane and drain wire. | 95028509 | 3476-26 |

"B" Cable Mating Receptacle on Unit or Controller.

| ITEM | DESCRIPTION | CDC P/N | BERG P/N |
|---|---|---|---|
| 8 | 26 pin, vertical header | 96752044 | 65610-126 |

### 3.10.2.3 I/O CABLE CHARACTERISTICS

"A" Cable

Type: 30 twisted pair, flat-cable
Twists per inch: 2
Impedance: 110 ± 10 Ohms
Wire Size: 28 AWG, 7 strands
Propagation time: 1.6 to 1.8 ns/ft (0.49 to 0.55 ns/m)
Maximum cable length: 100 ft (30.48 meters) cumulative
Voltage Rating: 300 V rms

"B" Cable (with ground plane)

Type: 26 conductor, flat cable with ground plane and drain wire
Impedance: 65 ohms (3M P/N 3476-26)
Wire Size: No. 28 AWG, 7 strands
Propagation time: 1.5 to 1.8 ns/ft (0.46 to 0.55 ns/m)
Maximum cable length: 50 ft (15.24 meters)
Voltage Rating: 300 V rms

*These cables are for in-cabinet use only.

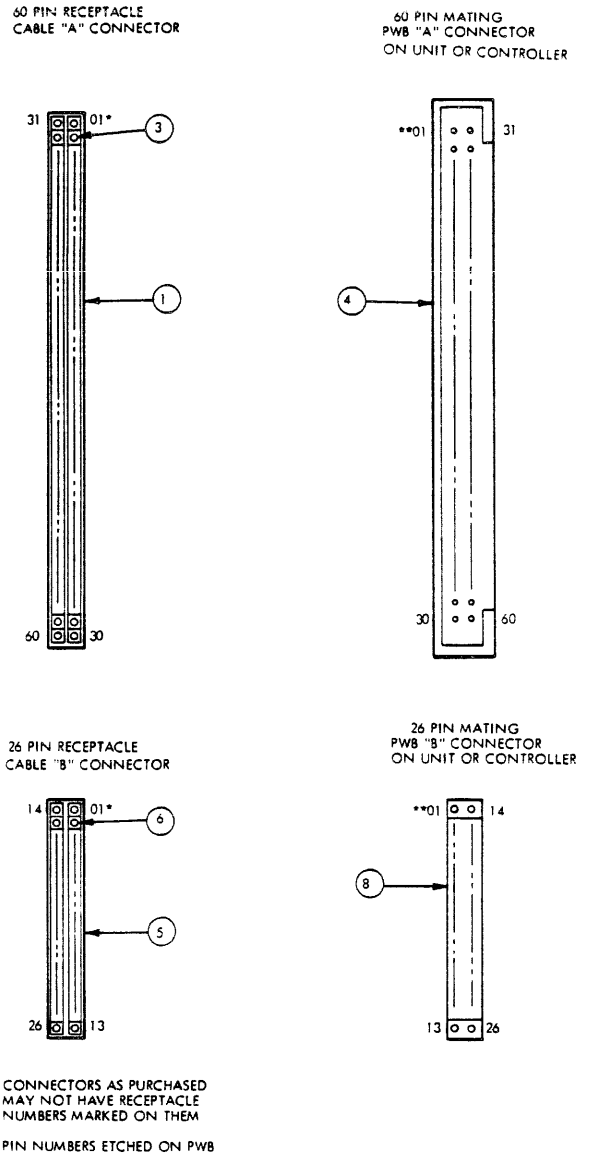



FIGURE 3-11. I/O CONNECTORS

## 4.1 INTRODUCTION

### 4.1.1 POWER AND INPUT/OUTPUT MODULE

The Power and Input/Output Module (PIO) is subdivided into a power supply and an I/O Adapter Printed Circuit Board.

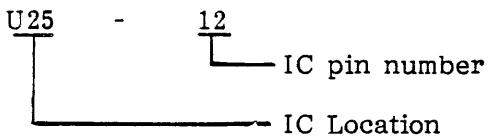
### 4.1.2 GENERAL

General Electronics Information

Logic signal names are followed by the symbol +L or -L indicating that the active (logic "1") level of the signal is high (+4 Volts for TTL) or low (nominal 0 Volts for TTL) respectively. For example, the signal SEQ-END-INT/+L indicates the signal is at a nominal +4 Volt level when active (logic "1").

Figure 4-1 shows a general block diagram of the PIO Adapter - I/O PWA, while detailed diagrams are in Section 5.

Integrated circuit components are designated as follows:




Functional descriptions are frequently accomplished by simplified diagrams for instructional purposes and as an aid in troubleshooting. The diagrams have been simplified to illustrate the principles of operation. Therefore, some elements are omitted. The logic diagrams in Section 5 of this manual should take precedence over the diagrams in this section whenever there is a conflict between the two types of diagrams.

The theory describes typical operations and does not list variations of unusual conditions resulting from unique system hardware or software environments. Personnel using this manual should already be familiar with principles of operation of the computer system, the controller, programming considerations (including the correct sequencing of I/O commands and signals).

## 4.2 I/O BOARD

The I/O adapter board is used to convert the SMD interface to an internal LMU interface, see Figures 4-3 and 4-4. The LMU interface is a byte oriented asynchronous interface with additional lines devoted to high speed information transfer.

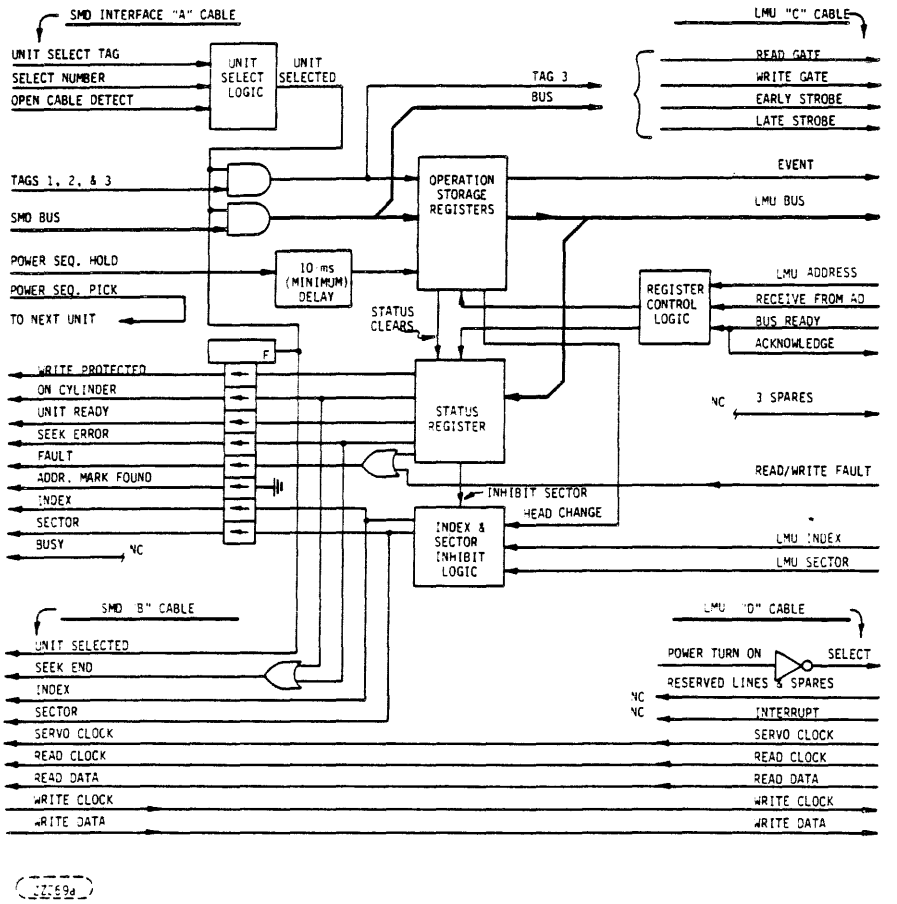



FIGURE 4-1. OVERALL BLOCK DIAGRAM OF I/O ADAPTER PWA (SHOWN IN POSITIVE LOGIC)

## 4.2.1 POWER ON/OFF AND SPINDLE START/STOP FUNCTIONS

### 4.2.1.1 POWER SEQUENCING HOLD AND PICK

SPINDLE MOTOR CONTROL (See Figure 4-2), (Option enabled by Jumper W9)

The Hold line enables the interface to start or stop the LMU spindle motor provided the PIO DC power is on, the PIO AC power is on, and the LMU control panel START/STOP switch is in the Start position. Activation of the Hold input (i.e., a logic 1 or low level) will initiate rotation of the spindle motor. The spindle motor is up to speed within 120 seconds maximum after application of the hold signal. The spindle motor up to speed condition is reflected in the interface "Ready" line to Host. The spindle motor may be stopped by deactivation of the Hold line by the Host. The spindle motor is stopped within 60 seconds maximum after the Hold input is deactivated. Note the "Ready" status goes false when the Hold input is deactivated.

It is to be noted that the LMU provides a 10 ms minimum noise filter to the Hold line to guard against false detection of the Hold line due to noise. In addition, individual devices may be started and stopped via the control panel START/STOP switch if the interface Hold signal is activated (Low Level or logic 1).

The LMU will directly pass the Pick signal for daisy chained operation but will not functionally interpret this signal.

### 4.2.1.2 POWER ON SEQUENCE

Manually closing the equipment AC POWER circuit breaker* starts the LMU blower motor running and applies AC power to the power supply, which in turn supplies DC voltages to the electronics. The DC power is fused and not switchable and powers the electronics whenever the AC POWER circuit breaker is on. Once DC power is on, the spindle start up sequence can begin. (See LMU Manual)

### 4.2.1.3 POWER OFF

To power off the LMU after the spindle has stopped, open the system circuit breaker or PIO power switch. It is to be noted that the PIO power switch is not operator accessible.

*System circuit breaker external to PIO.

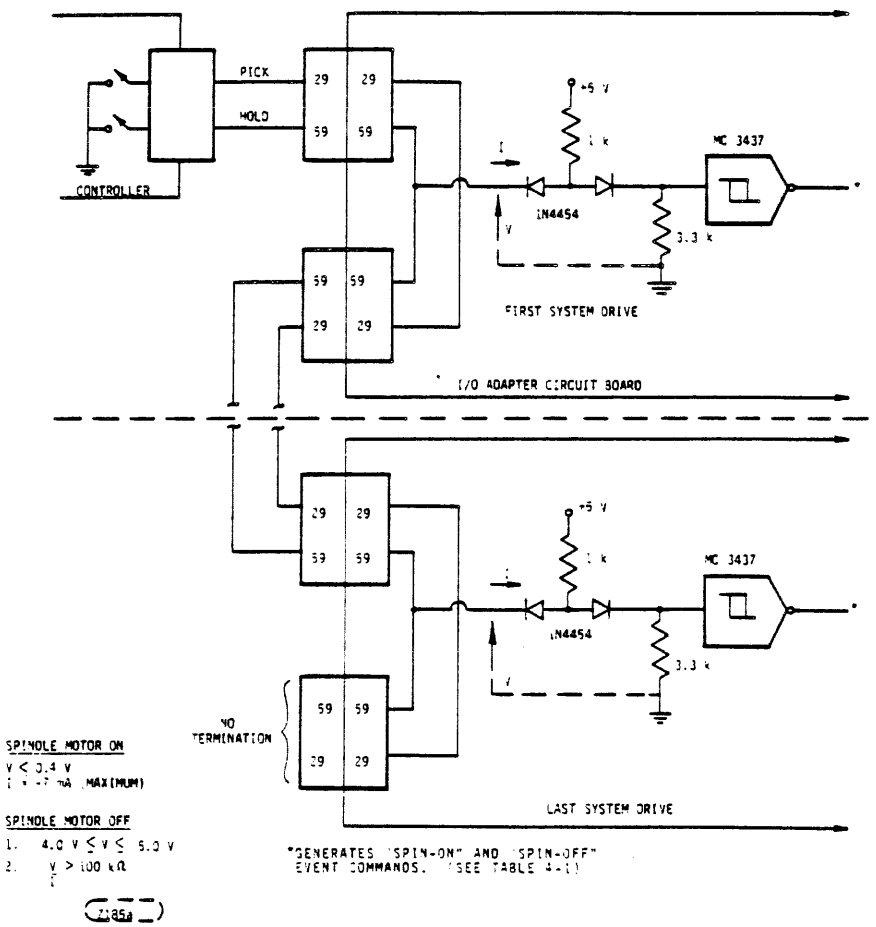



FIGURE 4-2. SPINDLE MOTOR POWER SEQUENCING CONTROL

## TABLE 4-1 COMMAND/STATUS BUS DEFINITION

| SENT FROM ADAPTER | | ADDRESS ($2^2$, $2^1$, $2^0$) | (MSB) 8US BIT (LSB) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| COMMAND BYTES SENT TO THE LMU | 1 | EVENT (111) 7 | READ ESCAPE REG | SEEK | HEAD SELECT | RTZ | SPINDLE POWER ON | FAULT RESET | 0 △3 | SPINDLE POWER OFF |
| | 1 | ESCAPE (000) 0 | 0 △3 | 0 △3 | SERVO OFFSET MINUS | SERVO OFFSET PLUS | 0 △3 | 0 △3 | 0 △3 | 0 △3 |
| | 1 | LOW CYL (110) 6 | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| | 1 | HIGH CYL (100) 4 | △3 RESERVED FOR HIGH CYLINDER EXPANSION | | | | | | $2^9$ | $2^8$ |
| | 1 | HEAD (101) 5 | △3 RESERVED FOR HEAD EXPANSION | | | | | | $2^1$ △1 | $2^0$ △1 |
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| STATUS BYTES SENT FROM THE LMU | 0 | STATUS (111) 7 | | WRITE PROTECTED | ON CYLINDER | UNIT READY | | SEEK ERROR | △3 | FAULT |

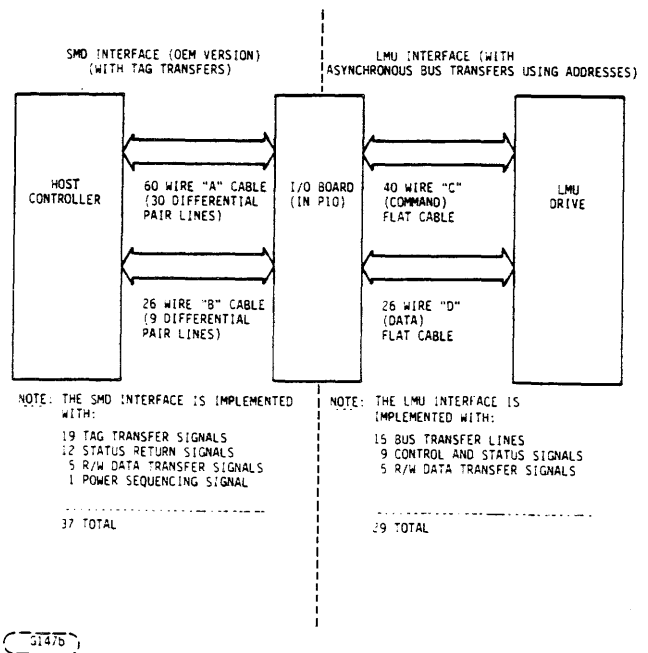
FALSE OR INACTIVE STATE = LOGIC "0" = 2.4 VOLTS MIN ON THE BUS.
TRUE OR ACTIVE STATE = LOGIC "1" = 0.4 VOLTS MAX ON THE BUS.

△1 HEAD ADDRESS BITS INTERPRETED BY THE LMU

△2 HIGH ORDER CYLINDER ADDRESS BITS MUST BE ZERO.

△3 RESERVED - MUST BE ZERO

F078a




3147b

FIGURE 4-3. HOST CONTROLLER TO LMU INTERFACE DIAGRAM

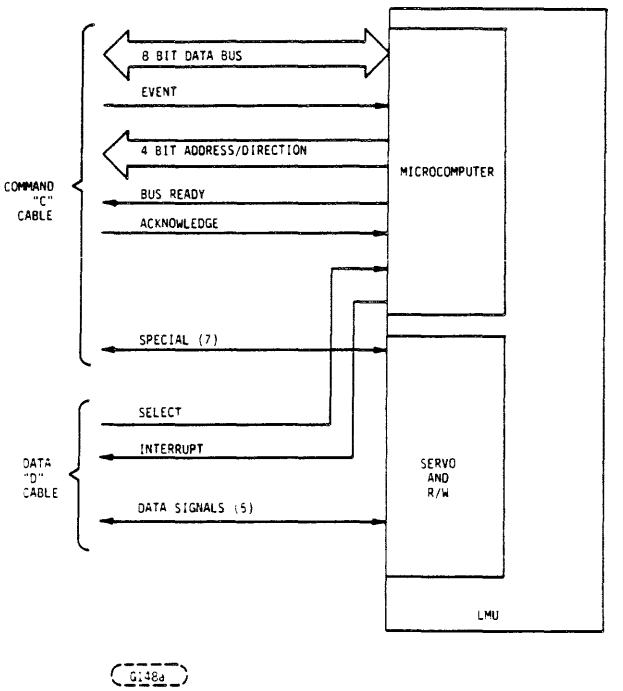



FIGURE 4-4. LMU INTERFACE

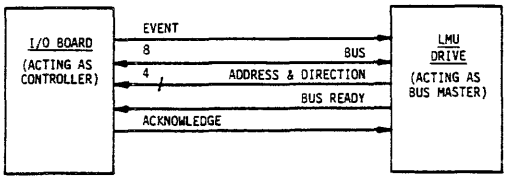
## 4.2.2 INTERFACE LINES

### 4.2.2.1 BUS TRANSFER LINES

The asynchronous portion of the interface uses a bidirectional bus for information transfer. The LMU drive directs the flow of information across the bus using the address and Bus Ready lines (see Figure 4-5). This situation allows a large amount of information to be transferred over the Bus without a great deal of logic in the I/O board. The I/O board maintains control over the bus by initiating transfers of commands over the bus using the event line and controlling the rate of transfer using the acknowledge line. This is shown in Figures 4-6 and 4-7. Figure 4-6 shows the transfer of a seek command and cylinder address to the drive. Figure 4-7 shows the resulting status information that is transferred back to the I/O Board. Any status change in the drive is automatically transferred back to the I/O Board.

### 4.2.2.2 HIGH SPEED LINES

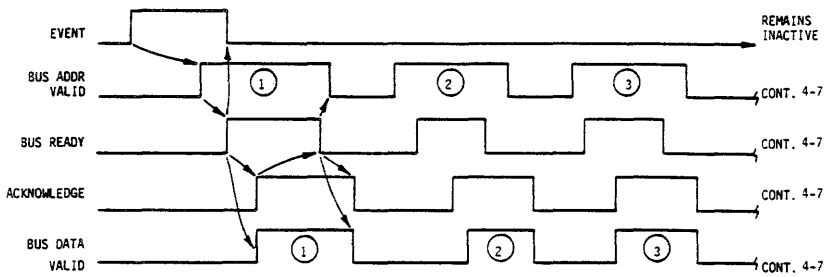
Certain signals must be transferred "instantaneously" across the interface to maintain critical timing. These signals are shown in Figure 4-8. All differential pair signals are transmitted and received according to the requirements for the SMD "B" cable. All single ended signals use tristate 74LS drivers and 74LS receivers. The receiver requires input by hysteresis and input clamping diodes to provide low noise termination of incoming signals.




EVENT - REQUESTS TRANSFER OF COMMANDS (OPERATIONS)
BUS - EIGHT LINES TO TRANSFER INFORMATION (BOTH WAYS).
ADDRESS - INDICATES WHAT IS TO BE TRANSFERRED.
BUS READY - USED BY DRIVE TO INITIATE EACH TRANSFER.
ACKNOWLEDGE - USED BY I/O ADAPTER BOARD TO ACKNOWLEDGE EACH TRANSFER.
* NOT PART OF LMU - AVAILABLE AS AN OPTION

G147a

FIGURE 4-5. LMU INTERFACE BUS TRANSFER LINES (SINGLE-ENDED)



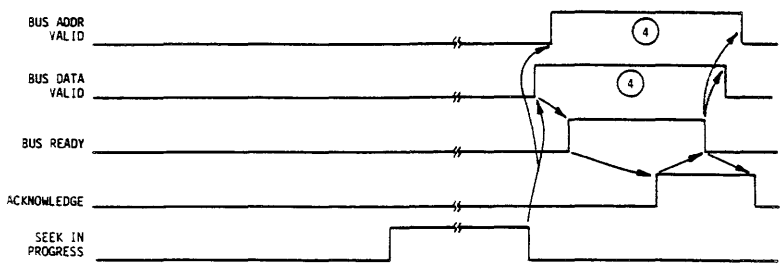

(1) - DRIVE REQUESTS A LIST OF OPERATIONS TO BE PERFORMED USING BUS READY AND ADDRESS LINES. I/O ADAPTER BOARD ACKNOWLEDGES REQUEST AND SENDS DATA ACROSS THE BUS. THE DRIVE TAKES DATA THEN DROPS BUS READY.

(2) - DRIVE REQUESTS HIGH ORDER BITS OF CYLINDER ADDRESS. TIMING IDENTICAL TO (1). (IF USED)

(3) - DRIVE REQUESTS LOW ORDER BITS OF CYLINDER ADDRESS. TIMING IDENTICAL TO (1). SEEK THEN STARTS.

G149a

FIGURE 4-6. TYPICAL BUS TRANSFERS FOR A SEEK I/O BOARD-TO-LMU TRANSFERS




(4) - THE LMU SENDS STATUS WITH "ON CYLINDER" ACTIVE. STATUS IS PLACED ON THE BUS AND TRANSFERRED TO I/O BOARD USING ADDRESS AND BUS READY LINES. THE I/O BOARD TAKES THE DATA AND ACKNOWLEDGES THE TRANSFER.

FF010

FIGURE 4-7. TYPICAL BUS TRANSFERS FOR A SEEK (LMU-TO-I/O BOARD TRANSFERS)

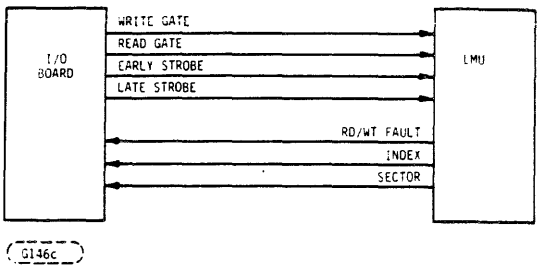



FIGURE 4-8. OTHER COMMAND CABLE LINES

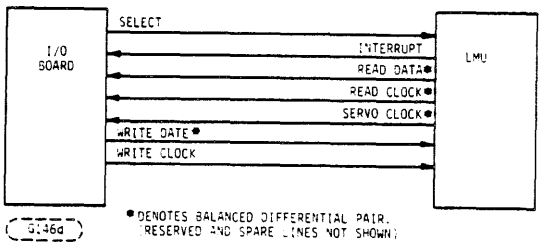



FIGURE 4-9. DATA ("D") CABLE LINES

## 4.2.2.3 DESCRIPTION OF I/O BOARD BLOCK DIAGRAM

The I/O board basically acts as a mailbox where information is stored by one interface until needed by the other. Certain SMD interface commands will, however, modify SMD interface statuses (like a seek clearing ON CYLINDER). Figures 4-1 and 4-10 show how the I/O board takes the SMD Tags and stores them for later transfer over the LMU Bus. Status transfers from the LMU bus are also shown stored in the status register for the SMD interface.

Most of the LMU high speed interface lines shown in Figures 4-8 and 4-9 are wired directly to (or from) the SMD interface. Index and Sector are basically the only high speed LMU signals that are modified. Figure 4-11 shows that the Sector and Index pulses will be disabled the instant a head change becomes effective. This may be due to a normal head change with seek, a pseudo seek, or an RTZ. Index and Sector pulses will be re-enabled with the first index pulse after the head change is completed.

It should be noted that a Tag 2 with no change in the head address will not be transferred to the drive, will not cause a pseudo seek, and will not inhibit index or sector.

The Unit Selection Logic does not allow the unit to be selected with an open cable. The unit will select on the rising edge of Unit Select Tag if the cable is intact and the correct select number is received.

The I/O board is in the following state after power turn on: Unit Selected, Unit Ready, Write Protected, On Cylinder, Seek Error, and Seek End are cleared; Index and Sector are enabled; Fault is set; all operation requests are cleared from the Operation Storage Registers (except Spindle Off if applicable); and the LMU is selected.

## SMD INTERFACE UNIT NUMBER AND OPTION SELECTION

The SMD unit number is selected at the I/O board DIP switch. Bits 0, 1, 2, and 3 are coded in switches 1 and 2. See Section 3, Installation and Checkout Manual.

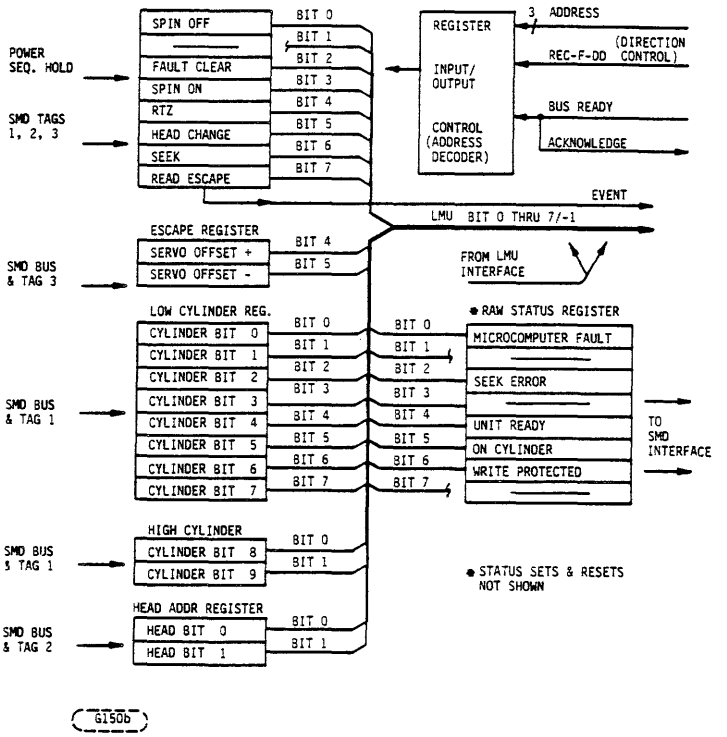



FIGURE 4-10. LMU BUS TRANSFER LOGIC

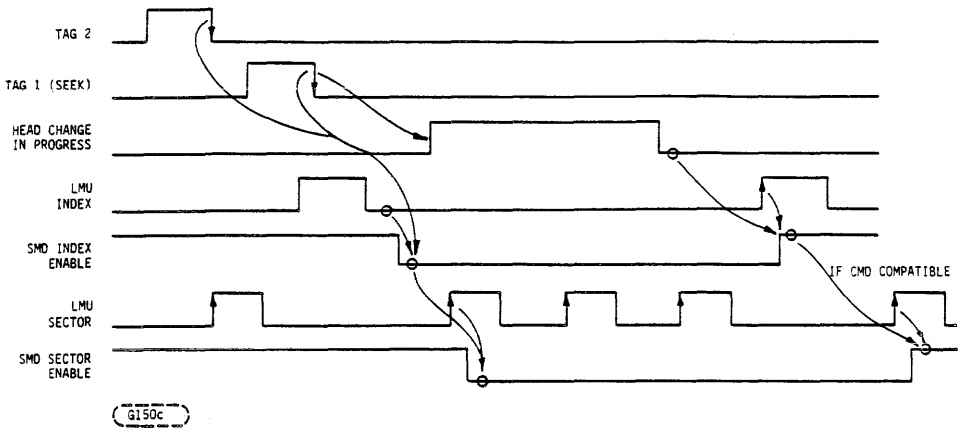



FIGURE 4-11. INDEX, SECTOR INHIBIT DURING HEAD CHANGES

## 4.3 INTERFACE, CONTROLLER TO PIO ADAPTER CIRCUIT BOARD

This section defines the input/output signal interface between the system controller and the PIO Adapter circuit board. Figures 4-12 through 4-19 are timing diagrams that illustrate the interface signal relationships.

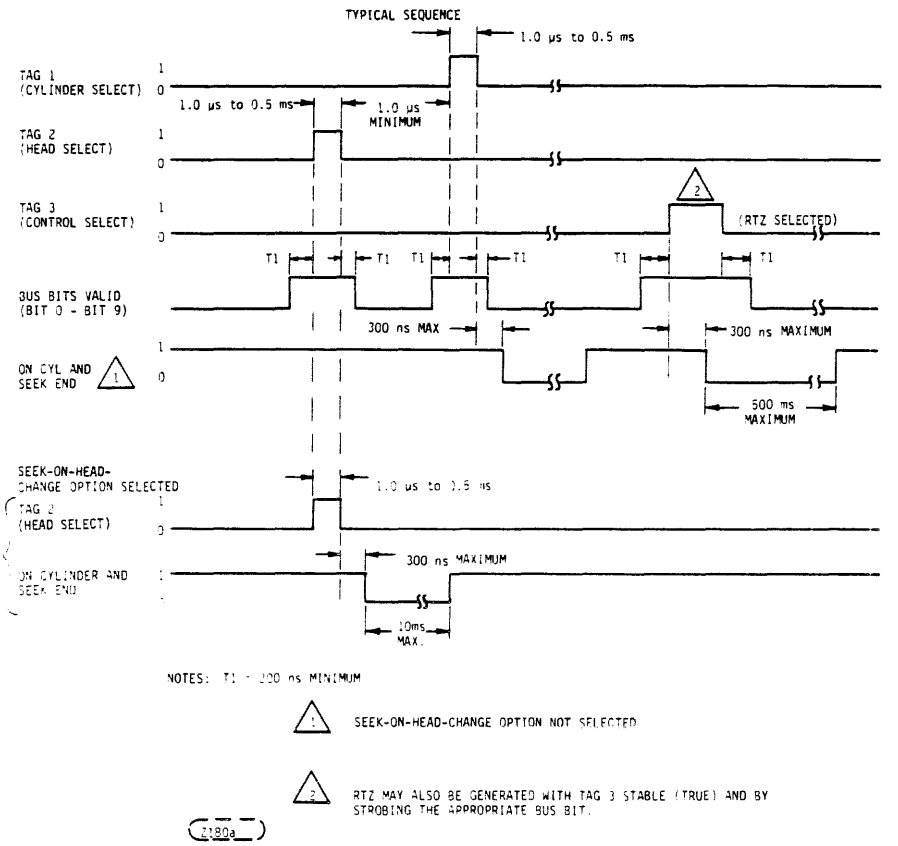
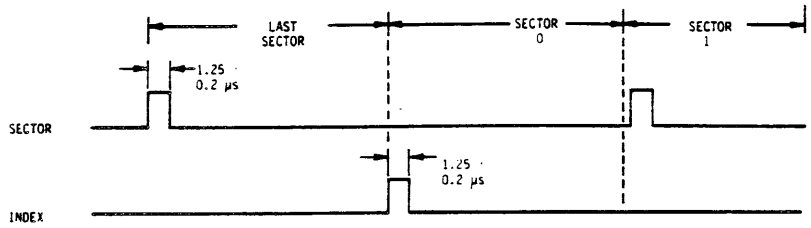
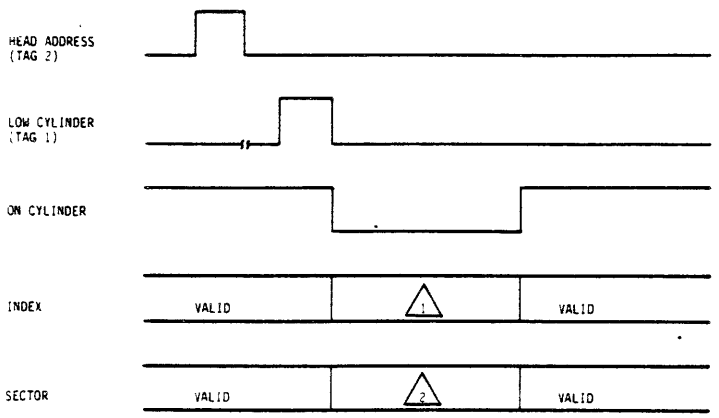



FIGURE 4-12. TAG AND BUS TIMING




Z182a

FIGURE 4-13. RELATIVE INDEX AND SECTOR RELATIONSHIP




1 DURING THE INTERVAL OF THE RESULTANT SEEK FOR A HEAD CHANGE, PHASE DISCONTINUITIES BETWEEN INDEX PULSES ARE POSSIBLE.

2 DURING THE INTERVAL OF THE RESULTANT SEEK FOR A HEAD CHANGE, PHASE DISCONTINUITIES BETWEEN SECTOR PULSES ARE POSSIBLE.

NOTE: 1) THE SERVO CLOCK TIMING INTEGRITY IS MAINTAINED DURING THE SEEK FUNCTION.

2) INDEX AND SECTOR TIMING INTEGRITY IS MAINTAINED IF NO HEAD CHANGE OCCURS

Z183a

FIGURE 4-14. INDEX AND SECTOR PULSES DURING SEEK

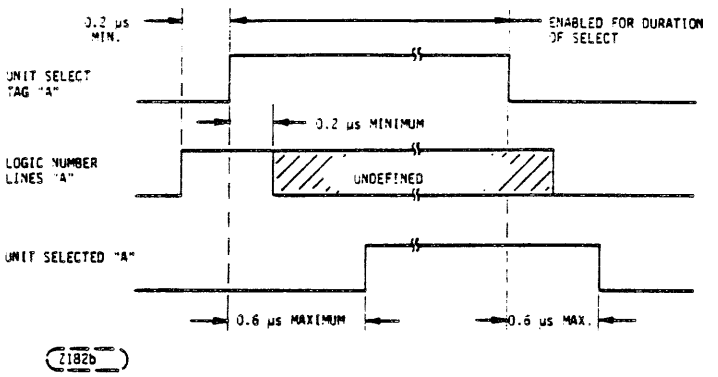



FIGURE 4-15. LOGIC NUMBER SELECT AND TIMING DIAGRAM

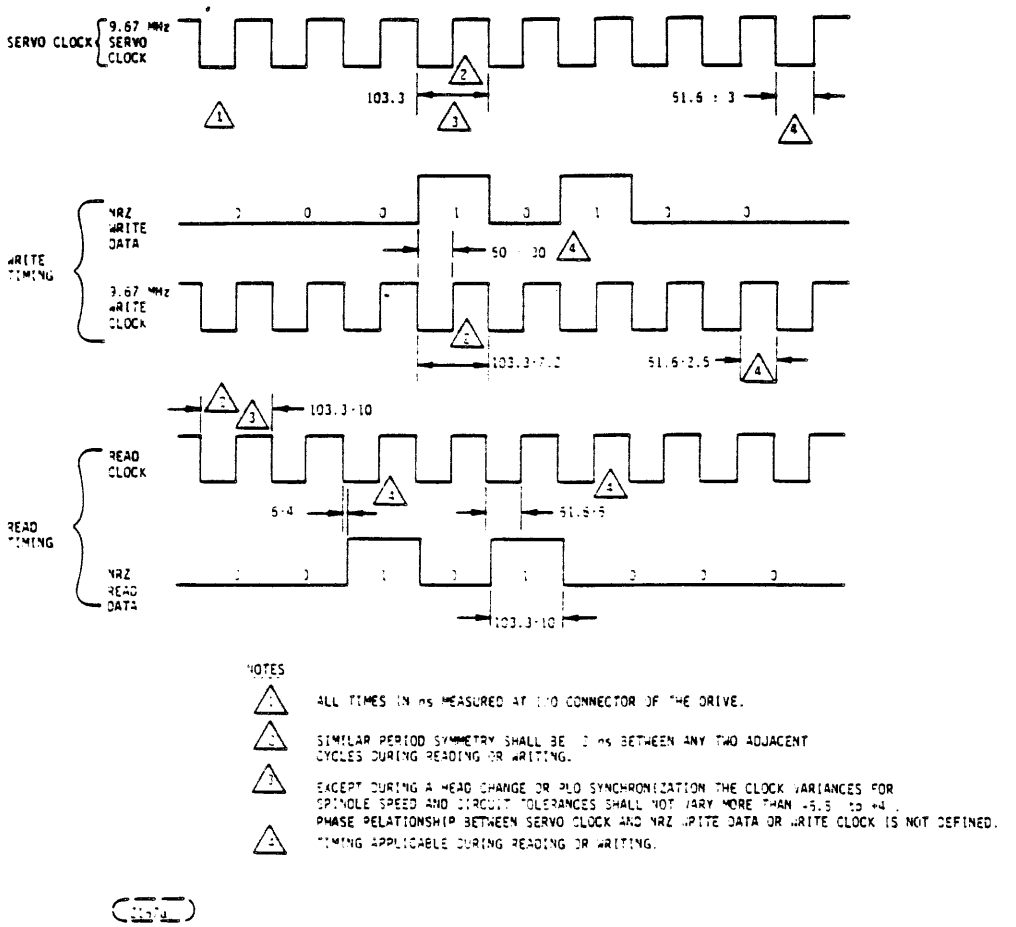
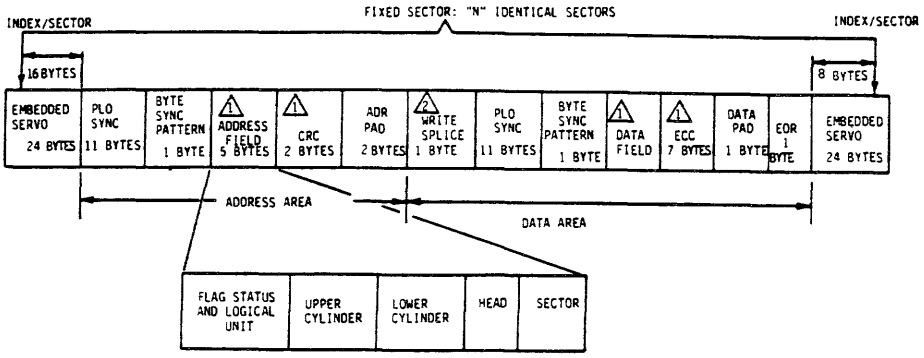



FIGURE 4-16. NRZ DATA AND CLOCK TIMING




EXAMPLE NO. 1: DATA FIELD LENGTH USING 64 SECTORS

$$\text{DATA FIELD} = \frac{\text{TOTAL BYTES/TRACK}}{\text{NUMBER OF SECTORS/TRACK}} - \text{(SYNC FIELDS, TOLERANCE GAPS, AND ADDRESS)}$$

$$\text{DATA FIELD} = \frac{20,672}{64} - 67$$

$$\text{DATA} = 256 \text{ BYTES/SECTOR}$$

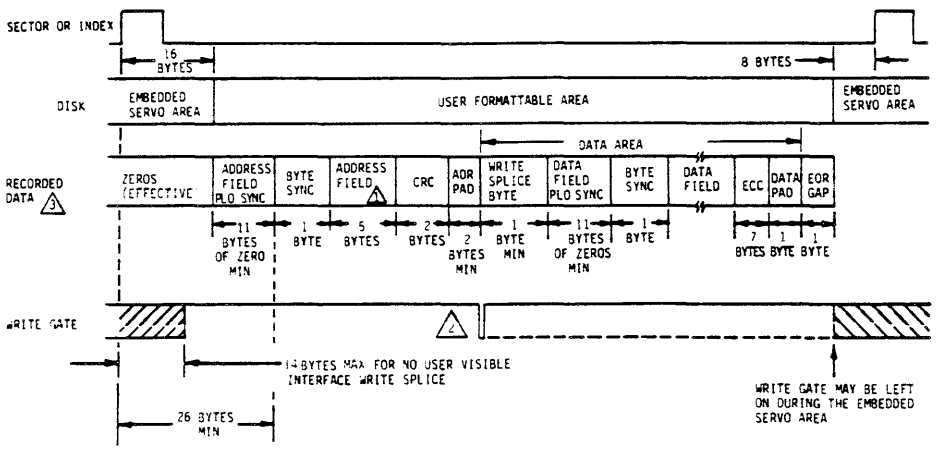
$$\text{EFFICIENCY} = \frac{256 \times 64}{20,672} = 79$$

1. THESE AREAS ARE EXAMPLES ONLY AND MAY BE STRUCTURED TO SUIT INDIVIDUAL CUSTOMER REQUIREMENTS.

2. THIS WRITE SPLICE BYTE IS IN THIS LOCATION AS A RESULT OF A RECORD UPDATE. FOR FORMATTING CONSIDERATIONS THIS BYTE MAY BE ALLOWED FOR AT THE END OF THE DATA SECTOR BY INCREASING THE NUMBER OF EOR (END OF RECORD) BYTES FROM 1 TO 2.

Z271a

FIGURE 4-17. SECTOR FORMAT




1. THE ADDRESS FIELD INCLUDES THE CYLINDER HEAD AND SECTOR LOCATION.

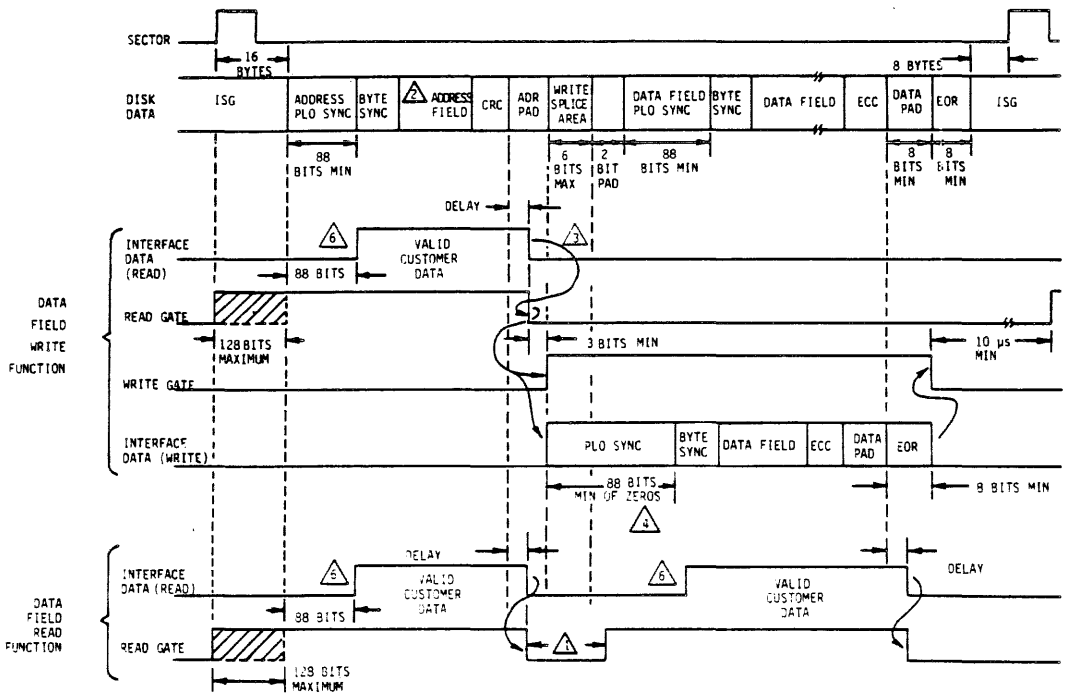
2. WRITING THE DATA AREAS ARE OPTIONAL. THESE AREAS ARE USEFUL TO VERIFY THE INTEGRITY OF THE SECTOR IF THE ADAPTER READ VERIFIES THESE AREAS AFTER A FORMAT OPERATION WHICH ALSO WRITES THE DATA AREAS. IF DATA FIELDS ARE TO BE WRITTEN, WRITE GATE MUST BE DEACTIVATED FOR A MINIMUM OF ONE BIT TIME AFTER THE ADDRESS PAD.

3. SHOWS DATA AS RECORDED ON THE DISK. TRANSMISSION OF THIS DATA BEGINS 8 BITS EARLIER TO ALLOW FOR ENCODER DELAY.

4. THIS FIGURE IS NOT DRAWN TO SCALE.

G030a

FIGURE 4-18. FORMAT TIMING




1. READ GATE MUST BE DEACTIVATED PRIOR TO THE WRITE SPLICE. IT MUST BE REINITIATED AT LEAST ONE BIT AFTER THE WRITE SPLICE AND WITH AT LEAST 11 BYTES OF PLO SYNC REMAINING IN THE SYNC FIELD.
2. THE ADDRESS FIELD INCLUDES THE TRACK, HEAD, AND SECTOR LOCATION.
3. CABLE ADAPTER DELAY NOT SHOWN. ALL TIMING SPECIFIED AT THE DRIVE CONNECTOR.
4. THE WRITE SPLICE BYTE WILL BE PROVIDED BY THE DRIVE ENCODER.
5. THIS FIGURE IS NOT DRAWN TO SCALE.
6. DATA IS VALID AND GUARANTEED TO BE ZEROS.

G052a

* VALUES ARE FOR THIS EXAMPLE.

FIGURE 4-19. TYPICAL READ/WRITE TIMING

## 4.4 POWER SUPPLY

The power supply uses a ferroresonant design. This design provides ±10% regulation on the ±16.5V outputs. The ±5 V outputs achieve 2% regulation using series regulators after the ferroresonant transformer. Isolation from line noise is provided by an RFI filter. Further protection for the system is provided by an AC circuit breaker, DC output fuses, and DC overvoltage protection. Refer to Section 5.5 for Power Supply Schematics. See Table 4-2 for DC output characteristics.

TABLE 4-2 POWER SUPPLY DC OUTPUTS

| | OUTPUT | |
|---|---|---|
| | +5 V/5.2 V | ±16.5 V |
| AVAILABLE CURRENT | 2.8/3.5 A | 1.3 (AVG) |
| REGULATION (AT SUPPLY) | 2% | 10% |
| RIPPLE VOLTAGE (P-P) | 50 mV | 500 mV |
| OUTPUT FUSES (Slow Blow) | (50 Hz ONLY) 5A* | 2.5 A MDA* |
| OVER VOLTAGE PROTECTION | 6 → 6.8 V | NONE |
| *SUBJECT TO CHANGE | | |

## 5.1 INTRODUCTION

This section contains the intercabling diagram, a key to logic diagram symbology, printed circuit board documentation and subassembly schematics.

## 5.2 INTERCABLING DIAGRAM

The intracabling diagram (Figure 5-1) shows the cabling between the PIO and LMU.

## 5.3 CIRCUIT BOARD DIAGRAMS

Table 5-1 lists printed circuit board assembly part numbers and the figure numbers of the schematic set. Refer to Figure 7-1 for diagram which shows location of circuit boards within the PIO.

TABLE 5-1. PIO CIRCUIT BOARDS

| CKT PWA IDENT | FIGURE NUMBER | CROSS REF NO. | TITLE |
|---|---|---|---|
| 75886100 | 5-3 | - | Terminator PCB |
| 77683750 | 5-4 | - | I/O Adapter PCB |
| 77611432* | 5-5 | - | Power Supply (50 Hz) |
| 77611431* | 5-6 | - | Power Supply (60 Hz) |
| 54186104 | 5-7 | - | Power Supply PWA Type EVRV |

*CONVENTIONAL WIRING - NOT A PWA

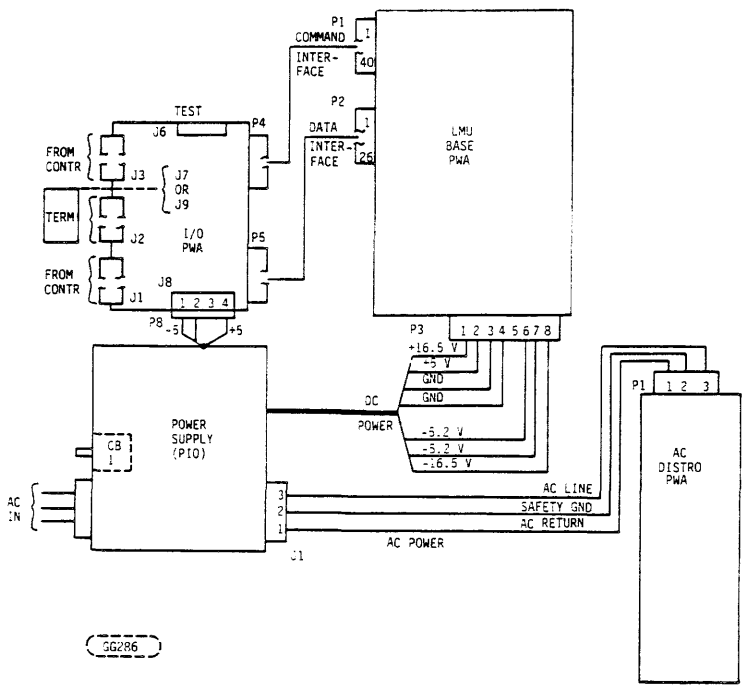



FIGURE 5-1. INTERCABLING DIAGRAM

## 5.4 LOGIC DIAGRAM SYMBOLOGY

### 5.4.1 GENERAL INFORMATION

Logic symbols are drawn with inputs on the left and outputs on the right whenever space and layout permit.

Power supply connections, discrete timing components, etc. may be shown connected to the top or bottom of the symbol. Unused pins and unused elements need not be shown. Figure 5-2 illustrates functionally equivalent symbols.

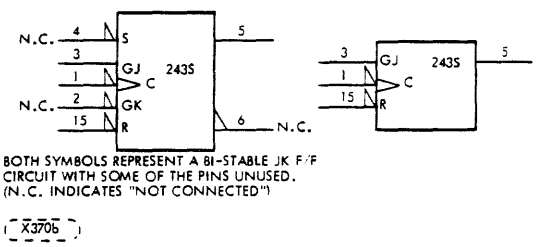



FIGURE 5-2. FUNCTIONALLY EQUIVALENT SYMBOLS

## 5.4.2 GENERAL SIGNAL ANNOTATION

S = Set input to bistable device

R = Reset (Clear) input to bistable device

G = Gate input has no direct action on circuit, but must be present before inputs (and/or outputs) are able to function. If more than one gate is used, a numeric suffix is added (G1, G2, etc.).

D = Identifies a signal which requires the presence of another signal to perform its function.

C = Strobe pulse. Usually used to gate "D" inputs into a bistable device.

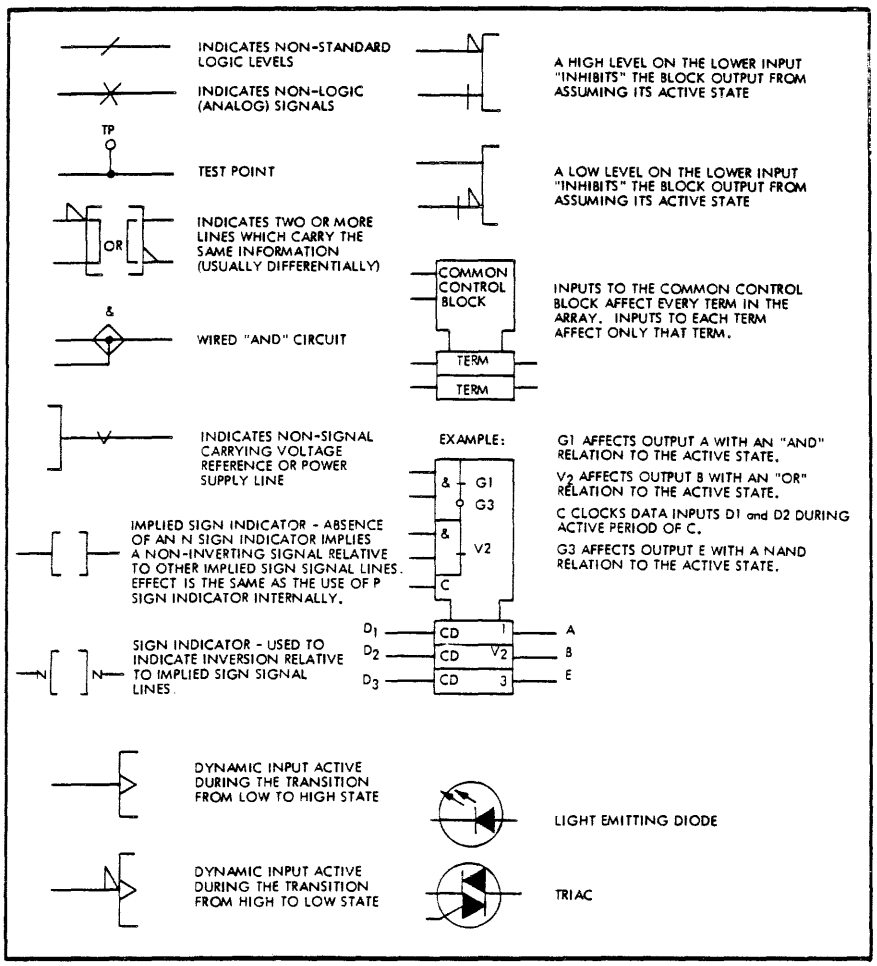
F = Enable output on tristable chips.

243S= Example CDC element identifies.

## 5.4.3 SYMBOLOGY

Logic Symbols are as described in Table 5-2.

TABLE 5-2. LOGIC SYMBOLOGY

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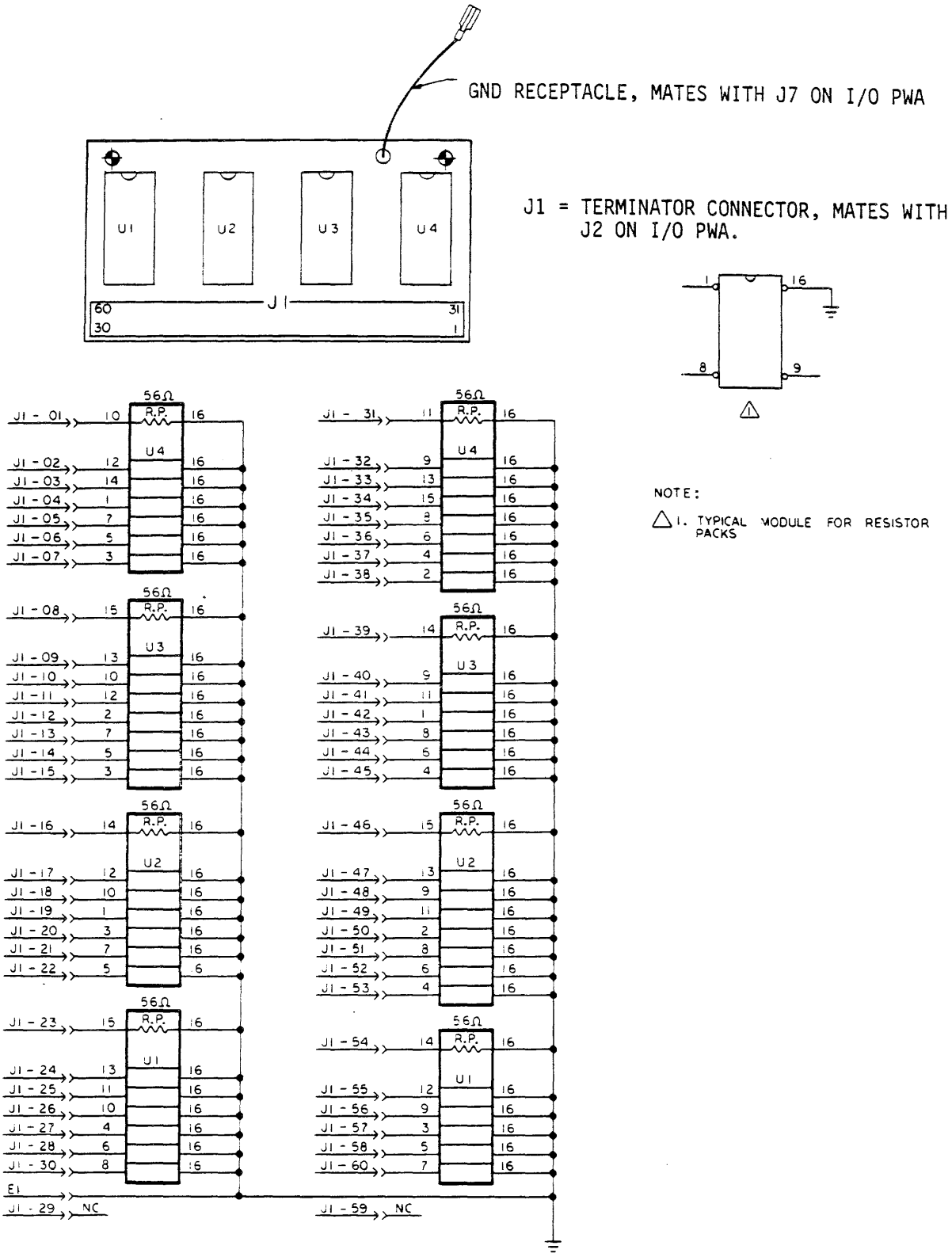



FIGURE 5-3. TERMINATOR CIRCUIT PWA

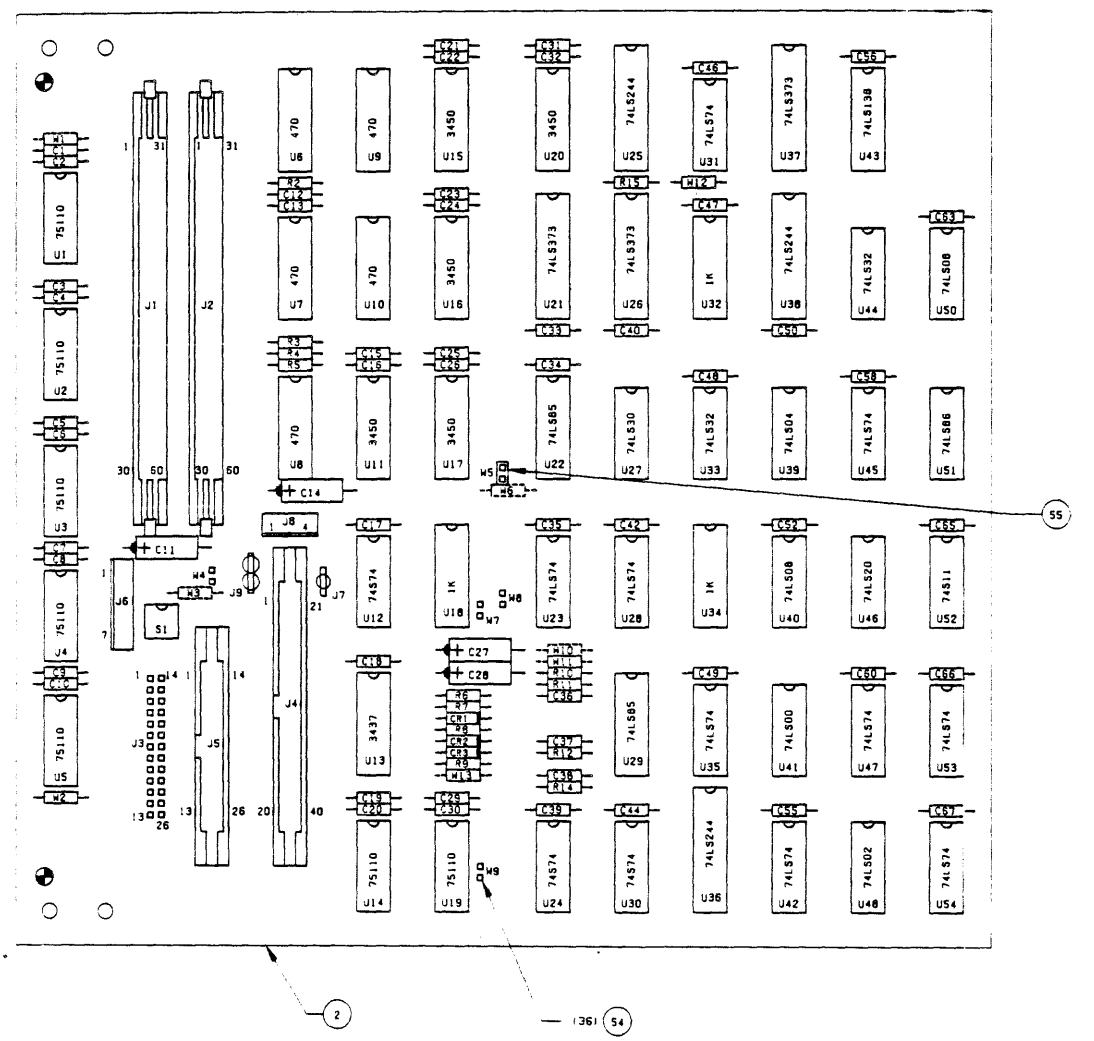
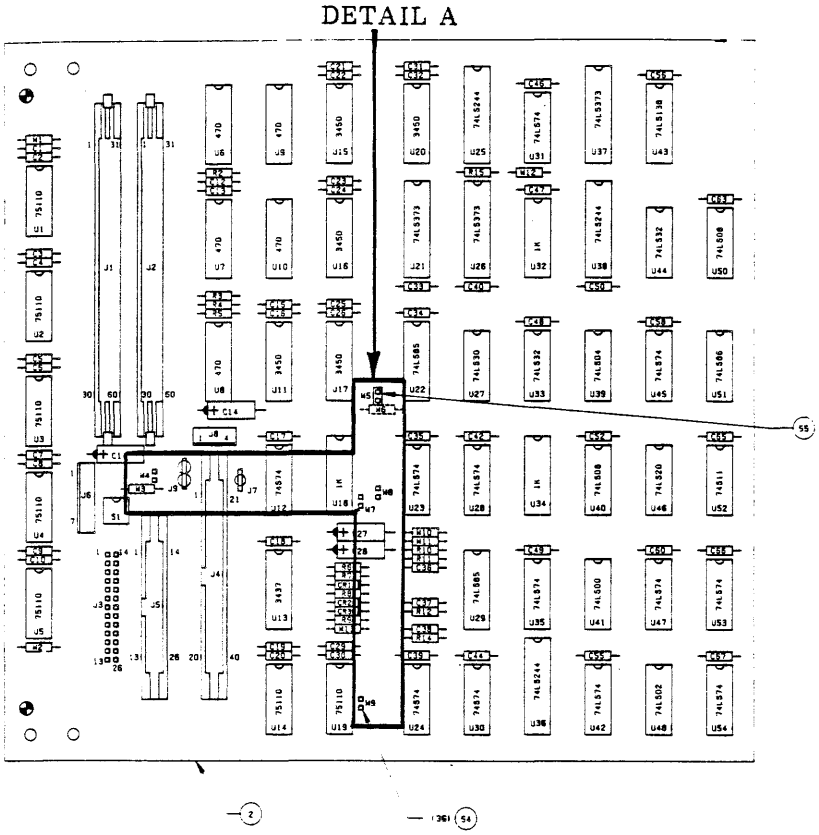



FIGURE 5-4. I/O ADAPTER PWA ASSEMBLY




| PIO HPC | POWER SUPPLY HERTZ | INTERFACE | JUMPERS* INSTALLED | TEST NUMBER OF PIO TESTER | I/O ADAPTOR PWA |
|---|---|---|---|---|---|
| 77708100 | 50 | SMD INTERFACE | W5 | 00 | 77700100-9 |
| 77708101 | 60 | SMD INTERFACE | W5 | 00 | 77700100-9 |
| 77708105 | 60 | CMD COMPATIBLE | W8 | 4C | 77700104-1 |
| 77708106 | 60 | CMD COMPATIBLE WITH DELAYED OFF CYLINDER | W8, W7 | 5B | 77700105-8 |
| 77708107 | 60 | CMD COMPATIBLE WITH PSEUDO SEEK | W8, W4 | 6A | 77700106-6 |
| 77708112 | 50 | CMD COMPATIBLE | W8 | 4C | 77700104-1 |
| 77708113 | 50 | CMD COMPATIBLE WITH DELAYED OFF CYLINDER | W8, W7 | 5B | 77700105-8 |
| 77708114 | 50 | CMD COMPATIBLE WITH PSEUDO SEEK | W8, W4 | 6A | 77700106-6 |
| 77708116 | 60 | SMD INTERFACE WITH REMOTE SPIN | W5, W9 | 88 | 77700108-2 |
| 77708117 | 50 | SMD INTERFACE WITH REMOTE SPIN | W5, W9 | 88 | 77700108-2 |
| 77708118 | 60 | CMD COMPATIBLE WITH REMOTE SPIN | W8, W9 | C4 | 77700112-4 |
| 77708119 | 50 | CMD COMPATIBLE WITH REMOTE SPIN | W8, W9 | C4 | 77700112-4 |
| 77708120 | 60 | CMD COMPATIBLE WITH REMOTE SPIN AND DELAYED ON CYLINDER | W7, W8, W9 | D3 | 77700113-2 |
| 77708121 | 50 | CMD COMPATIBLE WITH REMOTE SPIN AND DELAYED ON CYLINDER | W7, W8, W9 | D3 | 77700113-2 |
| 77708122 | 60 | CMD COMPATIBLE WITH PSEUDO SEEK AND REMOTE SPIN | W4, W8, W9 | E2 | 77700114-0 |
| 77708123 | 50 | CMD COMPATIBLE WITH PSEUDO SEEK AND REMOTE SPIN | W4, W8, W9 | E2 | 77700114-0 |

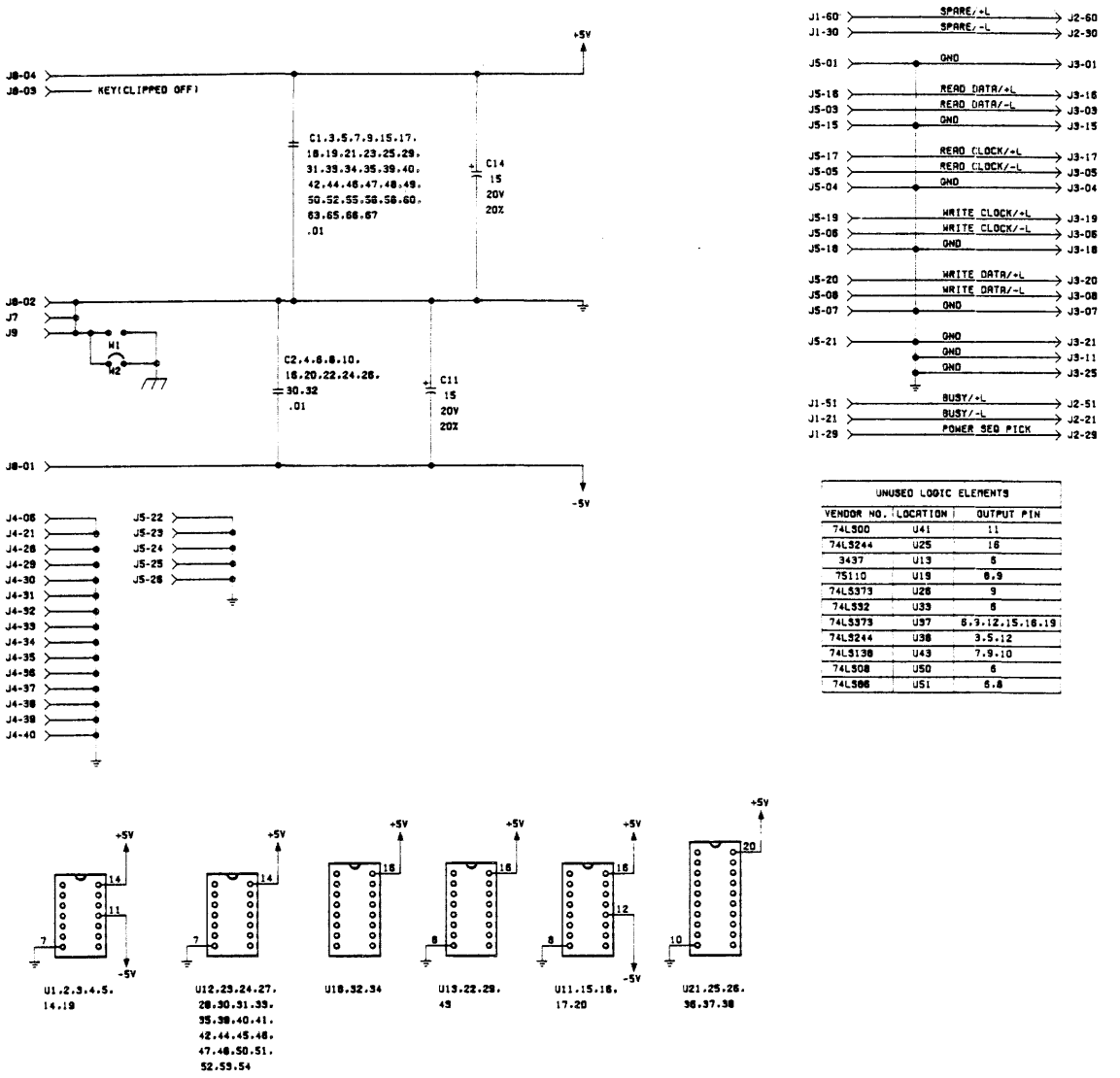
*JUMPER POSITIONS ARE SHOWN ON I/O ASSEMBLY DRAWING (SEE FIGURE 5-4 SHEET 1)

JUMPER W5 MUST BE REMOVED WHEN W8 INSTALLED.

JUMPER W8 MUST BE REMOVED WHEN W5 INSTALLED.

FF009a

FIGURE 5-4. I/O ADAPTER PWA OPTIONS




UNUSED LOGIC ELEMENTS

| VENDOR NO. | LOCATION | OUTPUT PIN |
|---|---|---|
| 74LS00 | U41 | 11 |
| 74LS244 | U25 | 16 |
| 3437 | U13 | 6 |
| 75110 | U19 | 8,9 |
| 74LS373 | U26 | 9 |
| 74LS32 | U33 | 6 |
| 74LS373 | U37 | 6,9,12,15,16,19 |
| 74LS244 | U38 | 3,5,12 |
| 74LS138 | U43 | 7,9,10 |
| 74LS08 | U50 | 6 |
| 74LS86 | U51 | 6,8 |

FIGURE 5-4. I/O ADAPTER PWA SCHEMATIC (SHEET 1 OF 6)

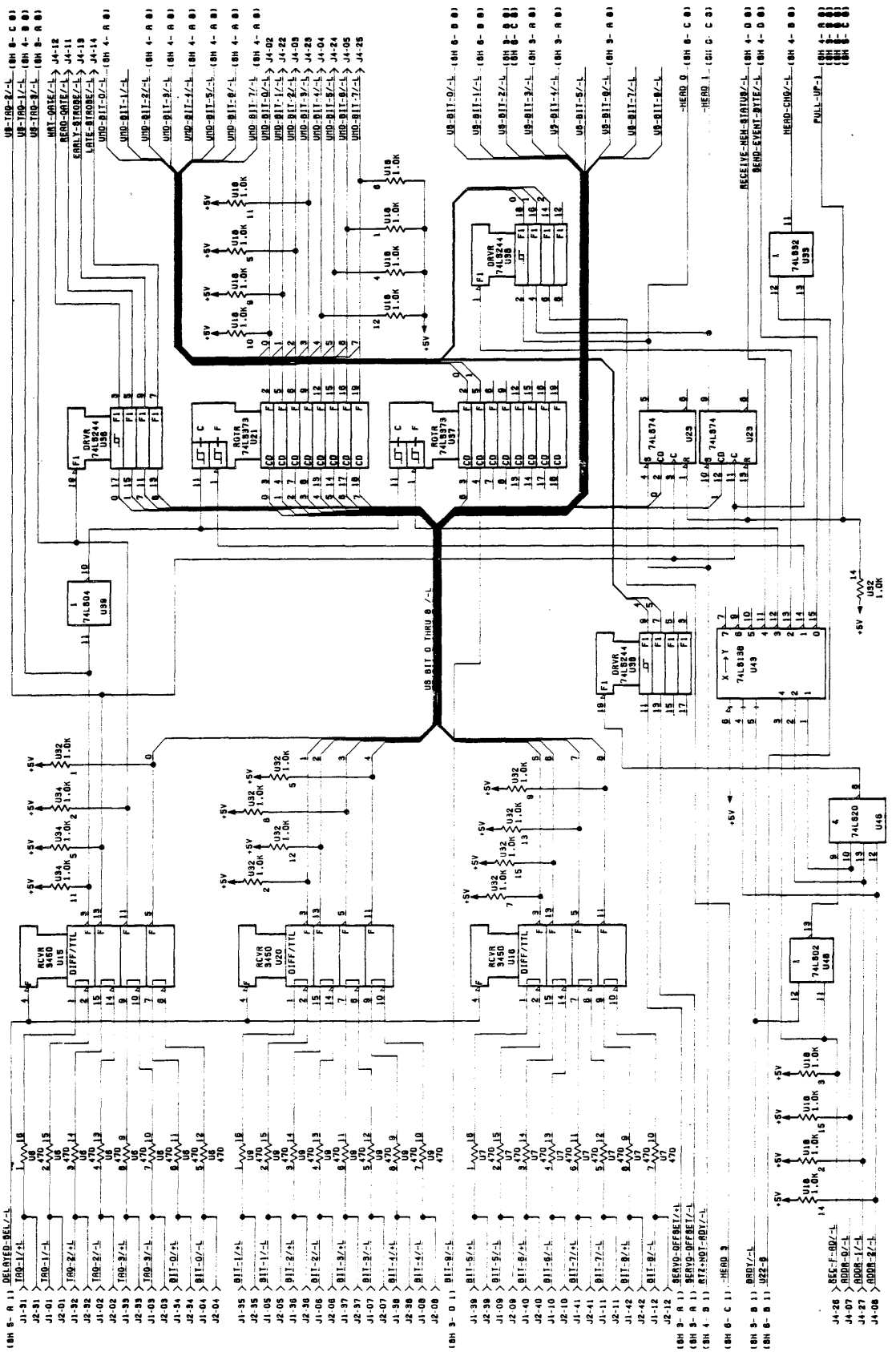


FIGURE 5-4. I/O ADAPTER PWA SCHEMATIC (SHEET 2 OF 6)

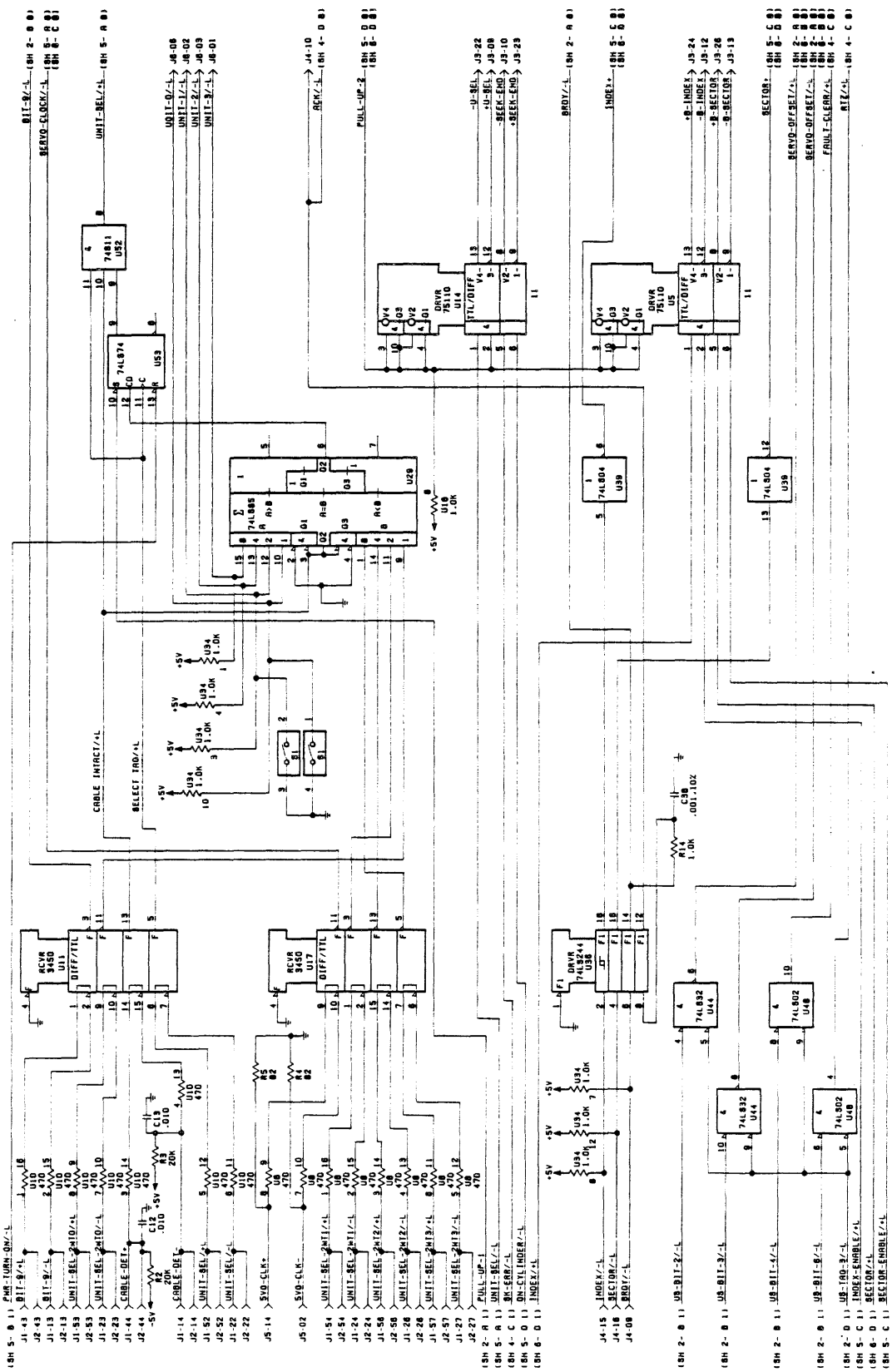


FIGURE 5-4. I/O ADAPTER PWA SCHEMATIC (SHEET 3 OF 6)

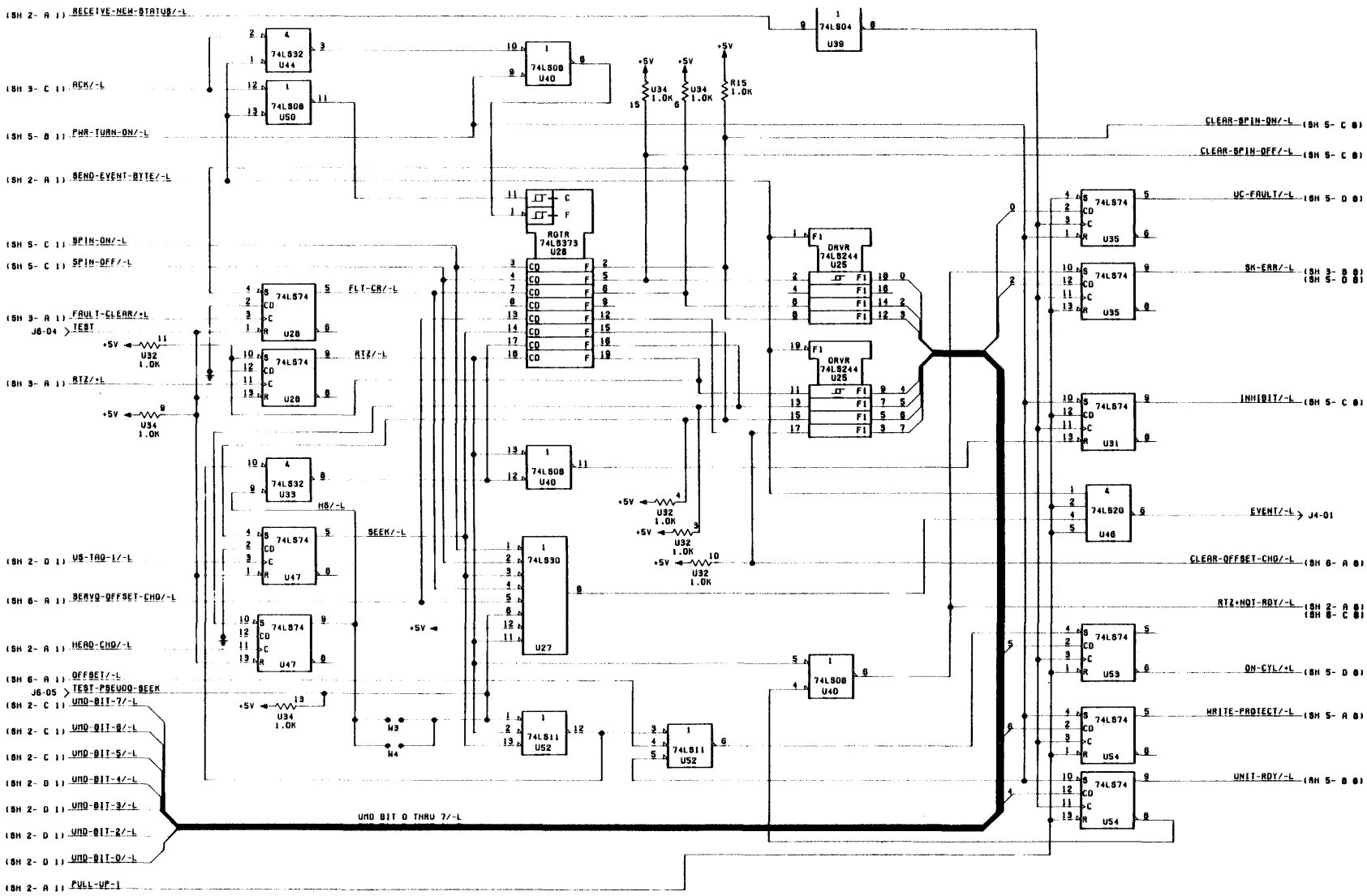



FIGURE 5-4. I/O ADAPTER PWA SCHEMATIC (SHEET 4 OF 6)

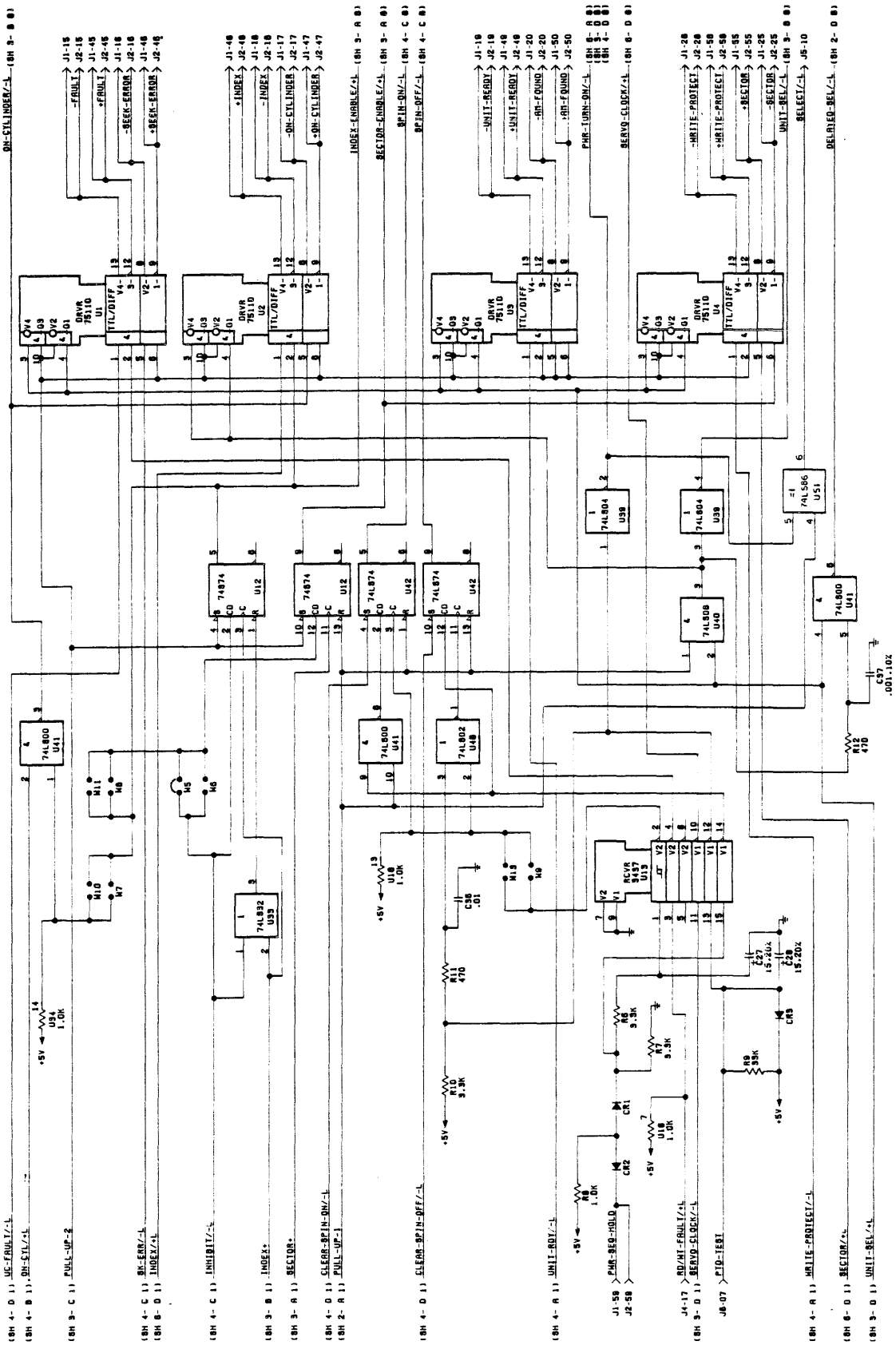


FIGURE 5-4. I/O ADAPTER PWA SCHEMATIC (SHEET 5 OF 6)

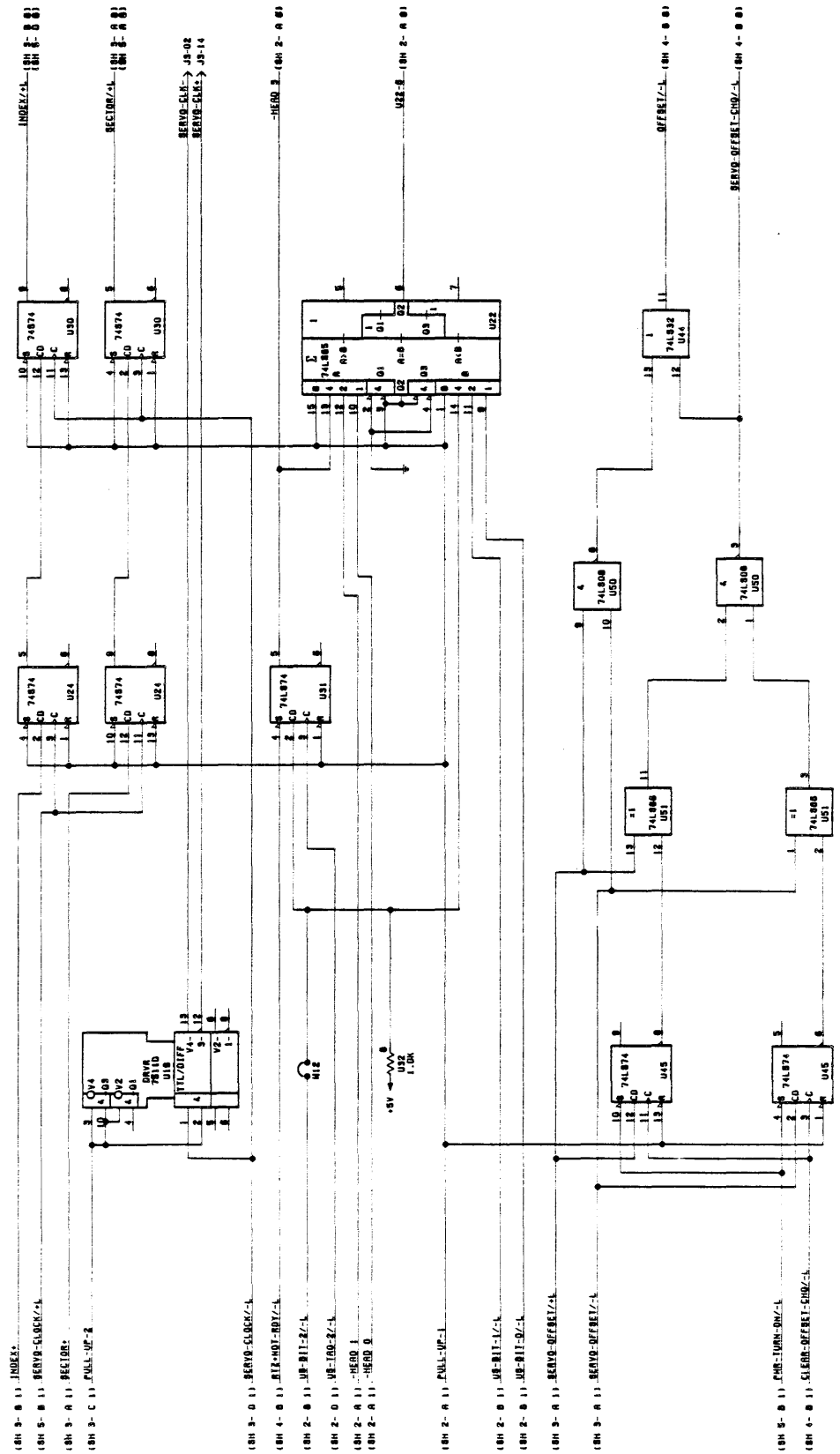


FIGURE 5-4. I/O ADAPTER PWA SCHEMATIC (SHEET 6 OF 6)

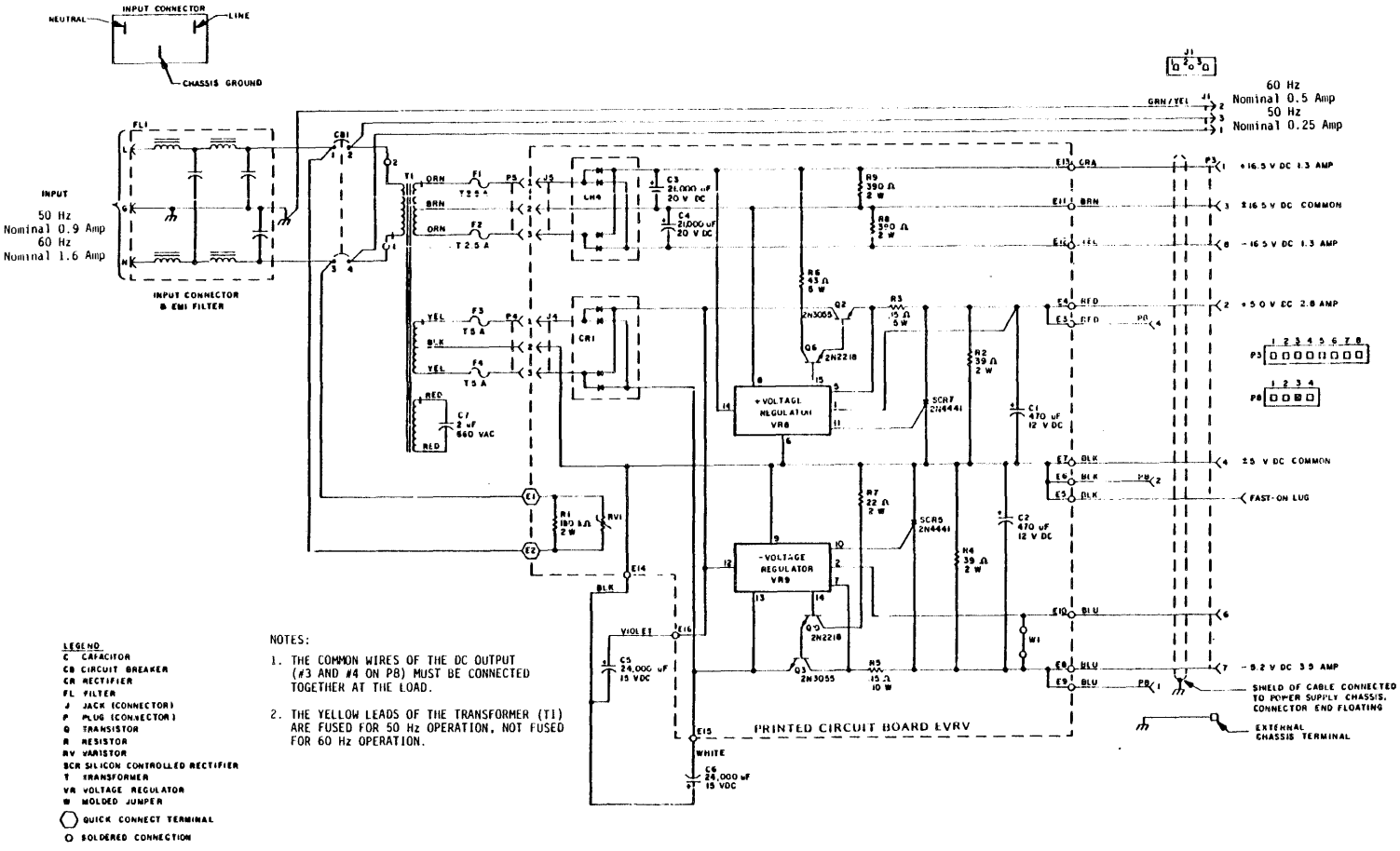



FIGURE 5-5, POWER SUPPLY SCHEMATIC

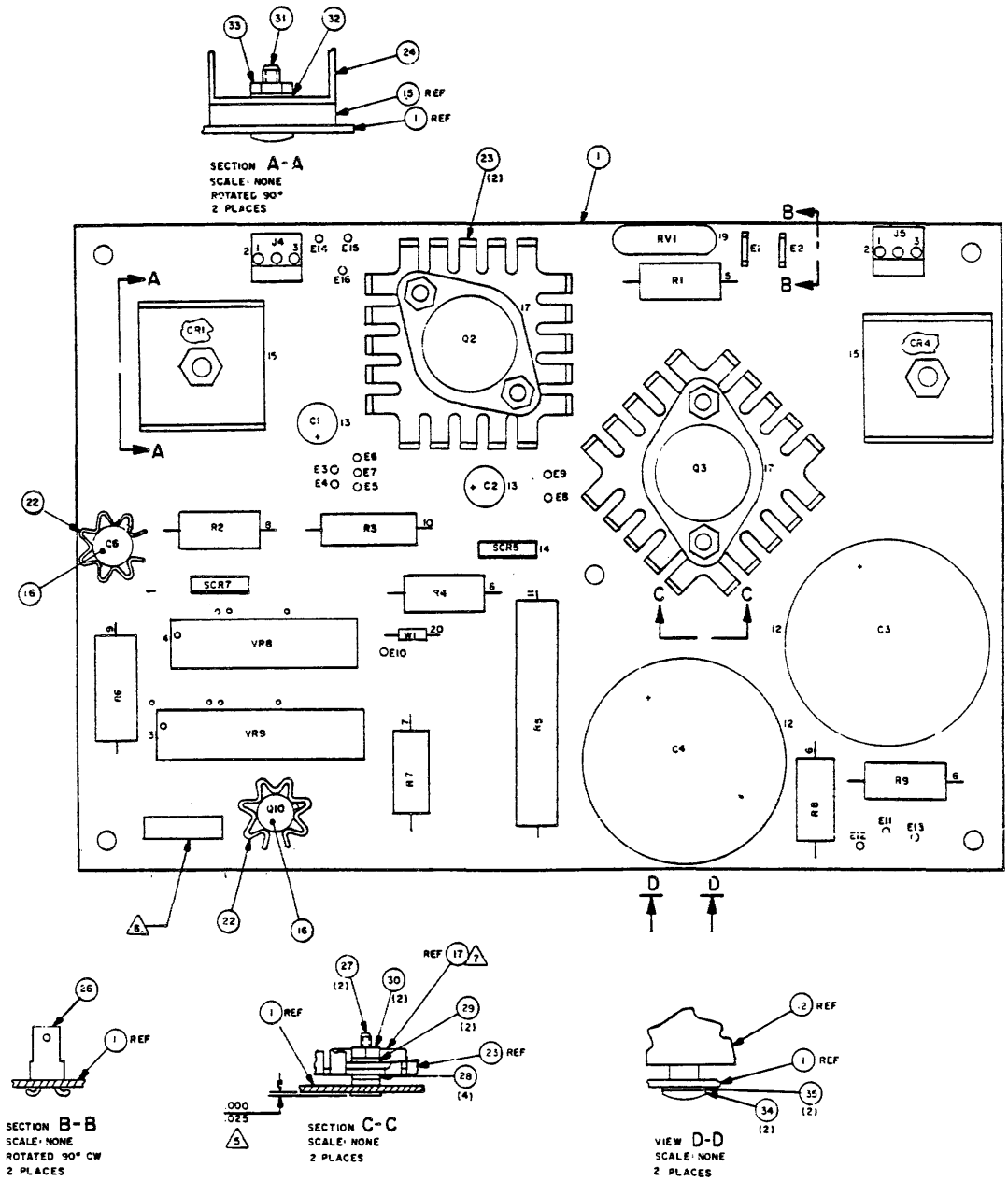



FIGURE 5-6. POWER SUPPLY PWA TYPE EVRV

## 6.1 INTRODUCTION

This section contains the instructions required to maintain the Power and I/O Adapter (PIO). The information presented is provided in the form of corrective maintenance. There is no preventive maintenance to be performed. All maintenance should be performed by qualified and trained service personnel.

## 6.2 SAFETY AND SPECIAL MAINTENANCE PRECAUTIONS

Before preceeding with any maintenance, maintenance personnel should become familiar with the precautions given in paragraphs 6.2.1 and 6.2.2.

### 6.2.1 SAFETY PRECAUTIONS

- Use care when power is applied to the PIO. AC voltages are present on the inside so the cover should not be removed unless absolutely necessary.

### 6.2.2 SPECIAL MAINTENANCE PRECAUTIONS

- Avoid overtightening hardware (screws, nuts, etc.) when replacing assemblies and components. All scres and nuts are of the low carbon variety.
- Do not connect or disconnect cables without first removing all power from the drive.

WARNING

The circuit assemblies contained in this equipment can be degraded or destroyed by ELECTRO-STATIC DISCHARGE (ESD).

Static electrical charges can accumulate quickly on personnel, clothing, and synthetic materials. When brough in close proximity to, or in contact with delicate components, ELECTRO-STATIC DISCHARGE OR FIELDS can cause damage to these parts. This damage may result in degraded reliability or immediate failure of the affected component or assembly.

To insure optimum/reliable equipment operation, it is required that technical support personnel discharge themselves by periodically touching the chassis ground prior to and during the handling of ESD susceptable assemblies/parts. This procedure is very important when handling printed circuit boards.

Printed circuit boards should be handled or transported in electrically conductive plastic bags to insure optimum protection against potential ESD damage.

## 6.3 MAINTENANCE TOOLS

No special tools are required to maintain the PIO.

## 6.4 MAINTENANCE PROCEDURES

### 6.4.1 INDEX AND SCHEDULE

The PIO is designed to require no preventative maintenance at the user site. Unless requrested by the user of the unit it is expected that only corrective maintenance will be performed. No special testing is required to confirm repairs other than the test that is used to isolate the fault.

## 6.4.2 REMOVAL AND REPLACEMENT PROCEDURE LIST

Table 6-1 lists the Removal and Replacement procedures provided in this section. The procedures are for the removal and replacement of recommended spare assemblies and components for the PIO.

TABLE 6-1. LIST OF REMOVAL AND REPLACEMENT PROCEDURES

| PARAGRAPH NUMBER | REMOVAL AND REPLACEMENT PROCEDURE |
|---|---|
| 6.4.2.1 | Top Cover |
| 6.4.2.2 | Connector/Switch Panel |
| 6.4.2.3 | PIO Power Supply Printed Circuit Boards |
| 6.4.2.4 | I/O Printed Circuit Board |
| 6.4.2.5 | Terminator Printed Circuit Board |
| 6.4.2.6 | Fuse Removal & Replacement |
| 6.4.2.7 | Power Supply Components |

### 6.4.2.1 REMOVAL AND REPLACEMENT OF TOP COVER

1. Remove power supply AC power cable from power source.
2. Disconnect all cables and remove PIO from its mountings.
3. Refer to Figure 6-1. Remove nine (9) screws (A) around the top and back side opposite the connectors of the cover. Depending on how it is mounted, the "back" of the cover may be used as the front of the PIO, in which case a user attached front cover may have to be removed before the screws along the "back" could be removed to allow removal of the top cover of the PIO.
4. Remove cover by lifting up and toward "back".
5. Replace by reversing the above steps.

### 6.4.2.2 REMOVAL AND REPLACEMENT OF CONNECTOR/SWITCH PANEL

1. Remove top cover per 6.4.2.1.
2. Remove two screws (E) from sides.
3. Though still connected to the power supply by wiring, the panel can be rotated up and out of the way for some purpose. The components attached to front panel can be removed at this point without removing the panel completely. To completely remove the panel, continue to next step.
4. Remove ground wires (G) from stud on side of unit.
5. Disconnect wires E1, E2 and the two black wires connected to the transformer as shown in Figure 6-1.
6. Remove panel.
7. Refer to Figure 6-1 when re-connecting wiring. Connections of E1 and E2 are interchangeable and so are the two to the transformer. Reverse the preceding steps to replace panel. Make certain that ground wire lugs are installed between two lock washers.

### 6.4.2.3 PIO POWER SUPPLY PRINTED CIRCUIT BOARD REMOVAL AND REPLACEMENT

1. Remove top cover per 6.4.2.1.
2. Refer to Figure 6-2. Remove screws securing I/O Adapter PWA and slide it out far enough to disconnect J8, the DC power connector to the I/O PWA.
3. Refer to Figure 6-1. Disconnect connectors P4, P5, E1 and E2 from the PWA EVRV.
4. Remove clamp and hardware (C) that secure cable to slide of power supply frame.

5. Remove the two screws (E) securing connector/switch panel and swing panel out of way.
6. Remove the four (4) screws (B) that secure the EVRV PWA and lift PWA out.
7. Replace EVRV PWA by reversing the above steps. Note that lug on ground wire from cable is installed between two lock washers.

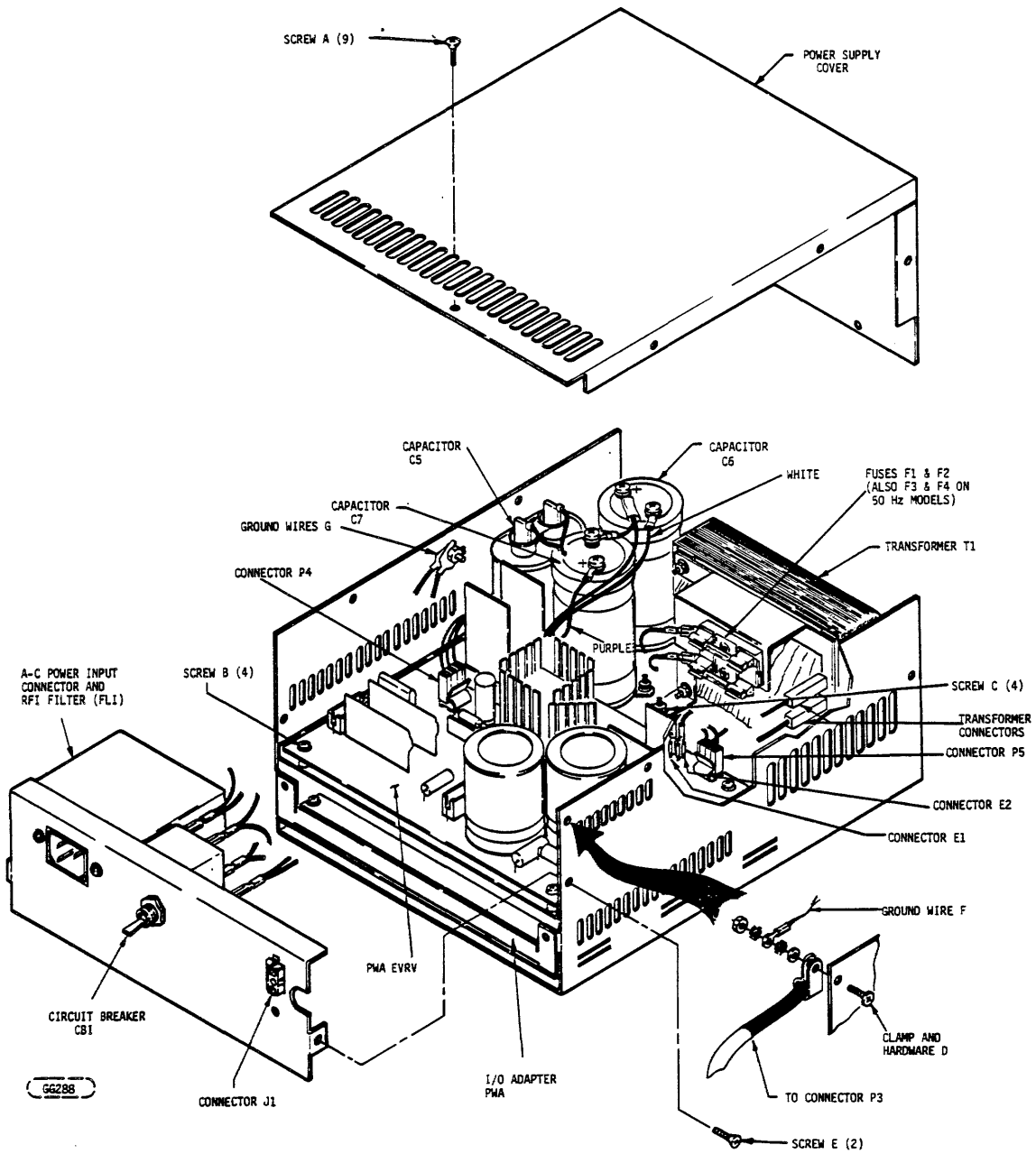



FIGURE 6-1. PIO ASSEMBLY SHOWING REMOVABLE COMPONENTS

### 6.4.2.4 REMOVAL AND REPLACEMENT OF I/O ADAPTER PWA

1. Refer to Figure 6-2. Remove two (2) screws that secure the I/O Adapter PWA bracket to the Power supply frame.
2. Slide the I/O Adapter PWA out a ways and disconnect the J8 DC power connector from the PWA.
3. Finish removing the PWA from the PIO.
4. Replace by following the reverse of the above steps.

### 6.4.2.5 REMOVAL AND REPLACEMENT OF TERMINATOR PWA

1. Remove I/O Adapter PWA per paragraph 6.4.2.4. Remove ground lead from J7 and unplug the terminator from J2 on I/O Adapter PWA.
2. Replacement of terminator is reverse of removal.

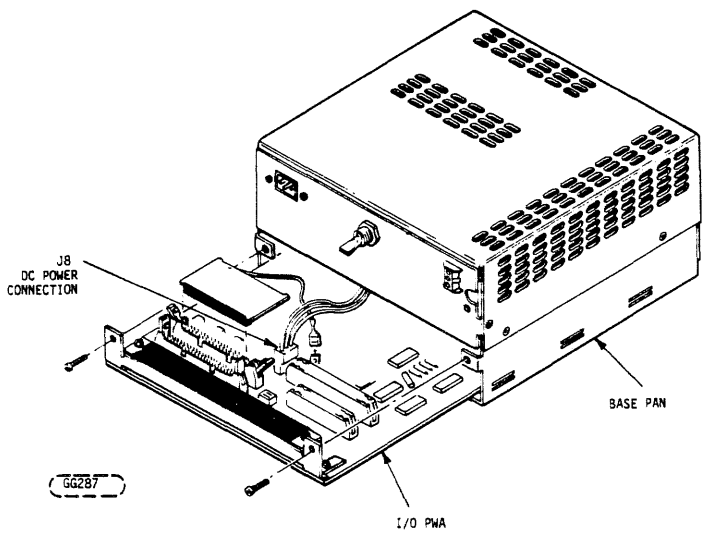



FIGURE 6-2. I/O PWA REMOVAL

### 6.4.2.6 FUSE REMOVAL AND REPLACEMENT

1. Remove top cover per 6.4.2.1. Refer to Figure 6-1. Fuses are mounted on a bracket that is mounted on the side of power transformer. 60 Hz power supplies have two fuses; 50 Hz supplies have four fuses.
2. Replacement is reverse of removal.

### 6.4.2.7 REMOVAL OF VARIOUS POWER SUPPLY COMPONENTS

For a list of the spareable components in the power supply see Section 7.

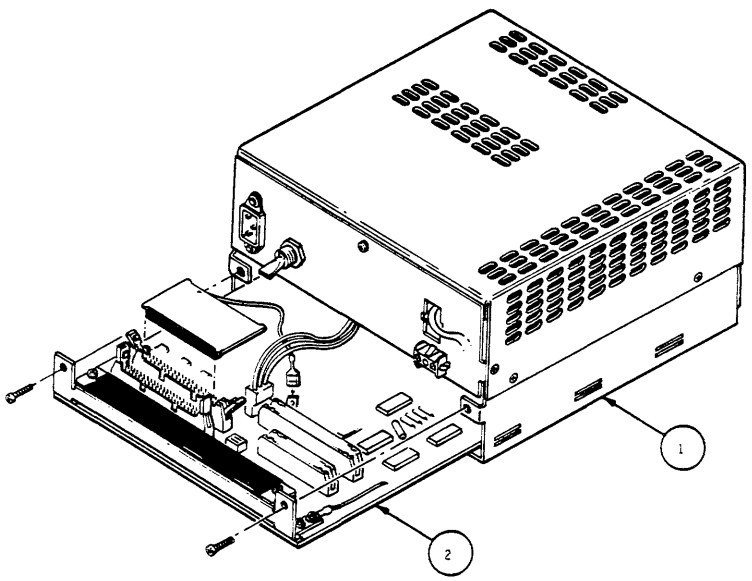
1. Remove top cover per paragraph 6.4.2.1.
2. Power Transformer Removal.
   a. Disconnect wires at capacitor C5.
   b. Disconnect connectors P4 and P5 from EVRV PWA.
   c. Disconnect wires from transformer to fuseholder.
   d. Remove nuts that secure the fuseholder bracket to the transformer.
   e. Remove fuseholder bracket from transformer.
   f. Remove four (4) screws (C) that secure the transformer to chassis. Remove transoformer from unit.
   g. Replacement is reverse of removal.
3. Capacitor Removal and Replacement (Not on PWA EVRV)
   a. Remove electrical connections to capacitor to be removed. Leads to C5 can be pulled off. On C6 or C7 remove the screws that secure the connector lugs and remove the connections from the applicable capacitor.
   b. With cross point screw driver loosen screw that tightens band around applicable capacitor body. This applies to C5, C6 or C7.
   c. Remove and replace applicable capacitor. Tighten securing screw.
   d. Replace electrical connections. C5 is non-polarized so it doesn't matter which of the removed wires are connected to which terminal. Refer to Figure 6-1 for aid in reconnecting the leads to C6 and C7.

## 7.1 INTRODUCTION

This section provides the information necessary to order the recommended replaceable parts for the Power Supply and I/O Adapter unit (PIO).

## 7.2 ORDERING PARTS

When ordering replacement parts for the PIO, include the equipment identification number to insure positive identification of parts.

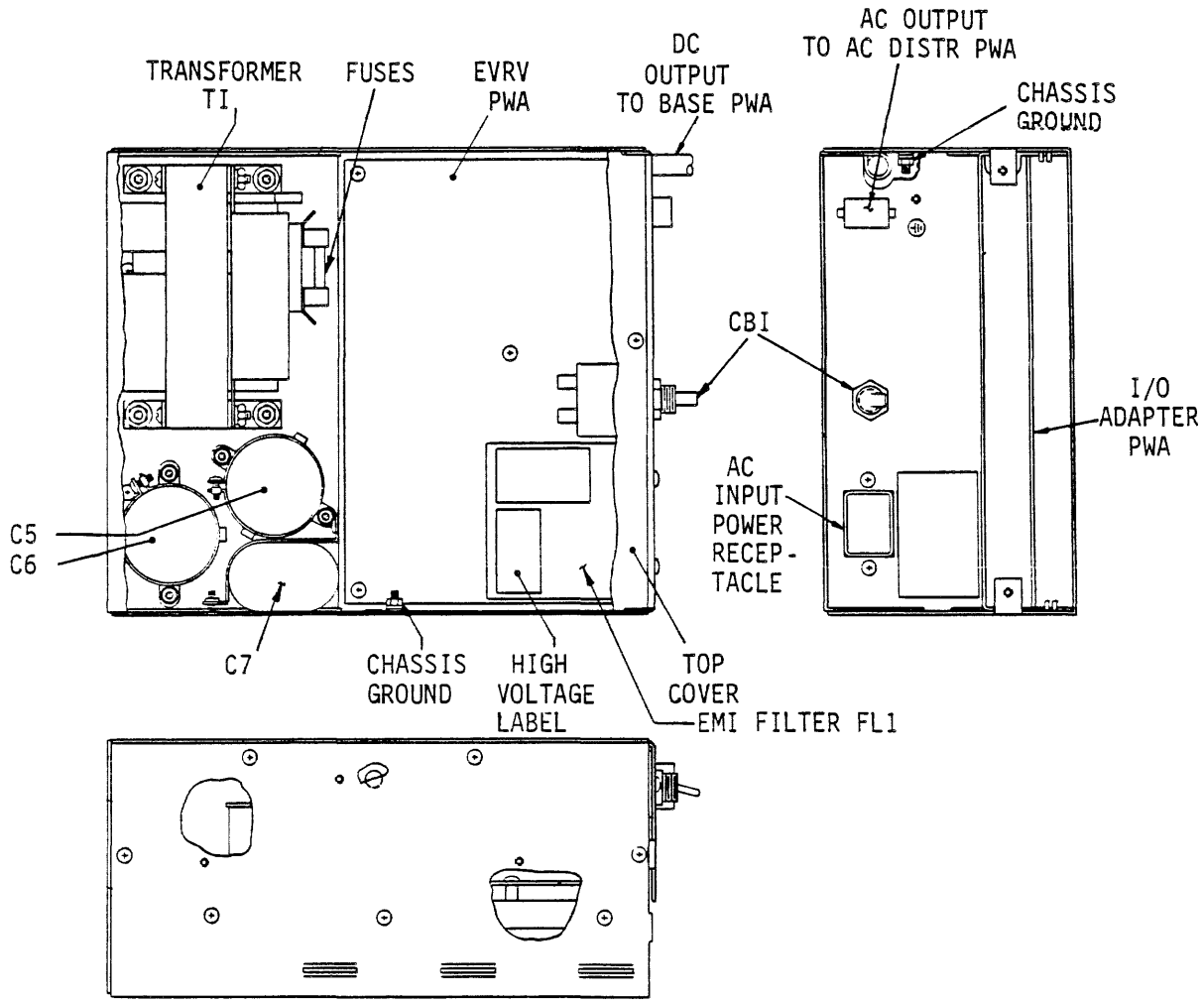



G144a

FIGURE 7-1. POWER AND INPUT/OUTPUT ASSEMBLY

| ITEM | IDENT NO. | DESCRIPTION |
|---|---|---|
| 1 | 77611431 | Power Supply Assembly, 60 Hz |
| 1 | 77611432 | Power Supply Assembly, 50 Hz |
| 2 | * | I/O Adapter PWA Configuration |

*Refer to Figure 5-4 for printed circuit board identification number after configuration.




NOTE: SEE SECTION 7-3 FOR PART IDENTIFICATION OF REPLACEABLE PARTS.

FIGURE 7-2. POWER SUPPLY

## 7.3 LIST OF REPLACEABLE PARTS FOR PIO*

| QUANTITY PER UNIT | SYMBOL | PART DESCRIPTION | PART NUMBER |
|---|---|---|---|
| 1 | C7 | Capacitor 2 uF, 660 VAC | 76879002 |
| 2 | C1,2 | Capacitor 470 uF, 20 V | 95691112 |
| 2 | C3,4 | Capacitor 21,000 uF, 20 V | 95595906 |
| 2 | C5,6 | Capacitor 24,000 uF, 15 V | 95661329 |
| 2 | CR2,4 | Rectifier Bridge | 15165577 |
| 2 | F1,2 | Fuse 2.5A Slo Blo 60 Hz | 51650226 |
| 2 | F1,2 | Fuse T2.5A 50 Hz | 15165930 |
| 2 | F3,4 | Fuse T5A 50 Hz | 15165931 |
| 2 | SCR5,7 | Silicon Controller Rectified 2N4441 | 94825900 |
| 2 | Q2,3 | Transistor 2N3055 | 95658800 |
| 2 | Q6,10 | Transistor 2N2218 | 92162039 |
| 1 | VR8 | Voltage Regulator Hybrid (+) | 15162002 |
| 1 | VR9 | Voltage Regulator Hybrid (-) | 15162001 |
| 1 | RV1 | Voltage Suppressor | 77612023 |
| 1 | P3 | Connector 8 Pt. | 10128944 |
| 1 | P8 | Connector 4 Pt. | 77613502 |

*Not including PWAs listed in Table 5-1.

See Figure 7-2, 5-5 and 5-6.

| LANIER PART NUMBER | DESCRIPTION | CDC PART NUMBER |
|---|---|---|
| E-066-421 | I/O PCB | 77683750 |
| E-066-365 | Power Supply, 60 Hz, w/o I/O PWA | 77611431 |
| E-066-365A | Power Supply, 50 Hz, w/o I/O PWA | 77611432 |
| E-066- | Power Supply PCB, EVRV | 54186104 |
| E-066-371 | Terminator PCB | 75886100 |