89637300

CONTROL DATA CORPORATION

CONTROL DATA®
LINE PRINTER CONTROLLER
FF524-A

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA
WIRE LIST

HARDWARE MAINTENANCE MANUAL

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or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

MANUAL REV	FCO OR ECO	EQUIPMENTS					
		SERIES FF524-A	S/N	LOGIC DIAGRAM 89639900			
		01	01	02			
01	ECO CK085	02	51, 103 104 & 110	04			
02	ECO CK485	03	101	06			
03	ECO CK937	03	-	-			
04	ECO CK1046	03	-	-			
A	ECO CK1229	03	-	A			
B	ECO CK1097	04	401	B			
B	ECO CK1311	05	501	B			
B	ECO CK1502	06	537	B			

PREFACE

This manual supplies reference information for the CONTROL DATA® FF524-A Line Printer Controller. This equipment is used with the AB107-A/AB108-A Computer to control the CL408-A/B or CL409-A/B Line Printers. A knowledge of the computer and line printer is required before using this line printer controller.

The following Control Data publications may be useful as references:

Title	Publication No.
1742 Line Printer Controller Reference Manual	89637200
1784 Computer Reference Manual	89633400
AB107-A/AB108-A Computer Customer Engineering Manual	89633300
I/O Specification Manual	89673100

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FIGURES

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GENERAL DESCRIPTION 1

INTRODUCTION

This section contains the functional and operational description of the CONTROL DATA® FF524-A Line Printer Controller.

The line printer controller logic circuitry is mounted on a single 50-PAK board. The line printer controller interfaces with the A/Q channel of the AB107-A or AB108-A to control line printer operations. Refer to the 1742 Reference Manual for controller placement in CPU. Each controller will handle one of the CONTROL DATA® CL408-A/B or CL409-A/B Line Printers. It contains the logic that interprets AB107-A/AB108-A function codes, controls line printer operations, transfers data to the line printer, and provides line printer status information to the CPU. The line printer controller may be accommodated in any unused A/Q slot within the AB107-A/AB108-A enclosure or the BT148-A Expansion Enclosure. Table 1-1 supplies a list of specifications for the controller.

INTERFACE CONNECTORS AND CABLES

The cables required for the operation of the controller and the line printer are listed in Section 7, Parts Data.

DATA TRANSFER

To perform data transfer, bit Q00 of the Q register shall be zero (Q00 = 0) and an Output-from-A instruction executed. Bits A00 through A07 of the A register shall contain the character bits to be transmitted, with leading zeros. The first character of a line is identified as the control character and will not be printed. (See Page 2-8 for description)

The Data Transfer command is rejected if one of the following conditions occurs:

1. Printer is not Ready.
2. Printer is Busy.
3. Data Status is false.
4. Protect Violation.

Data Transfer command clears EOP and ERROR status.

Table 1-1. Specifications

SPECIFICATIONS	EXPLANATION
PHYSICAL CHARACTERISTICS	
Dimensions	
Width	6-13/16 inches
Length	12-3/8 inches
Depth	3/8 inches
ENVIRONMENT	
Temperature	
Shipping	-40° F to 158° F (-40° C to 70° C)
Storage	14° F to 122° F (10° C to 50° C)
Operating	40° F to 120° F (5° C to 50° C)
Humidity	
Shipping	0 to 100% RH non-condensing
Storage	10% to 90% RH non-condensing
Operating	10% to 90% RH non-condensing
POWER	
Input Requirements	5 volts dc
Signal Level	
Low State (0)	0.4 volts dc, or less
High State (1)	2.4 volts dc, or more
Ground	Logic ground is connected to computer logic ground

PROGRAMMING AND OPERATION 2

This section describes the programming for the FF524-A Line Printer Controller. Preparation for operation and operation are described in Section 3.

PROGRAMMING

Table 2-1 and Figures 2-1 through 2-4 provide programming information. A description of the codes follows the figures.

Table 2-1. Addressing Codes

COMMAND CODE	INPUT-TO-A	OUTPUT-FROM-A
Q00 = 0	Illegal	Data transfer
Q00 = 1	Director Status	Director Function

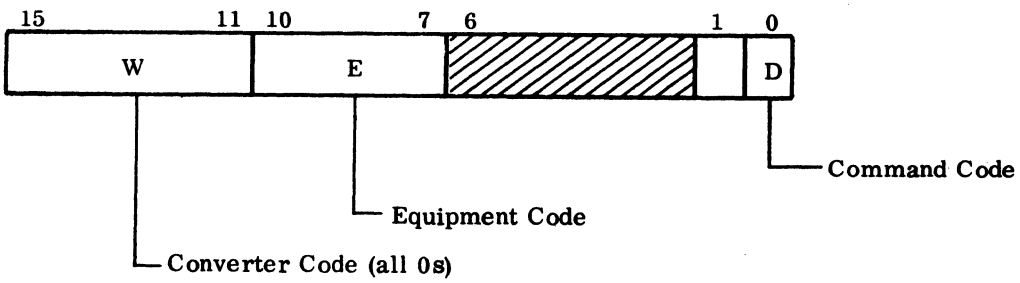


Figure 2-1. Q Register Format

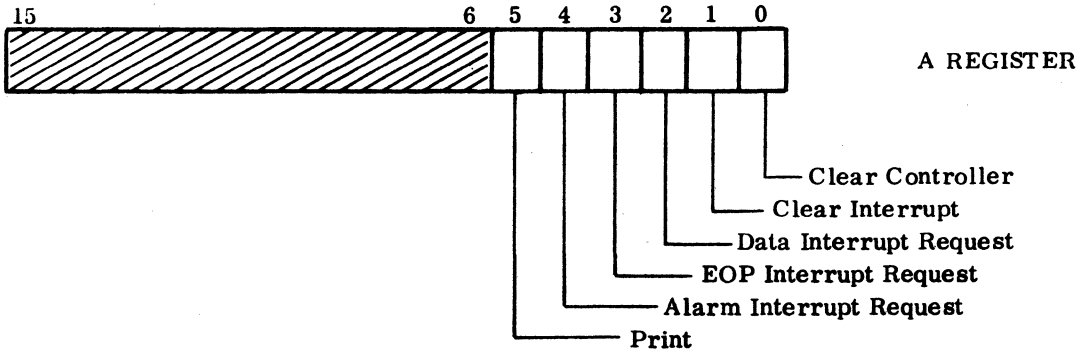


Figure 2-2. Function Code Format

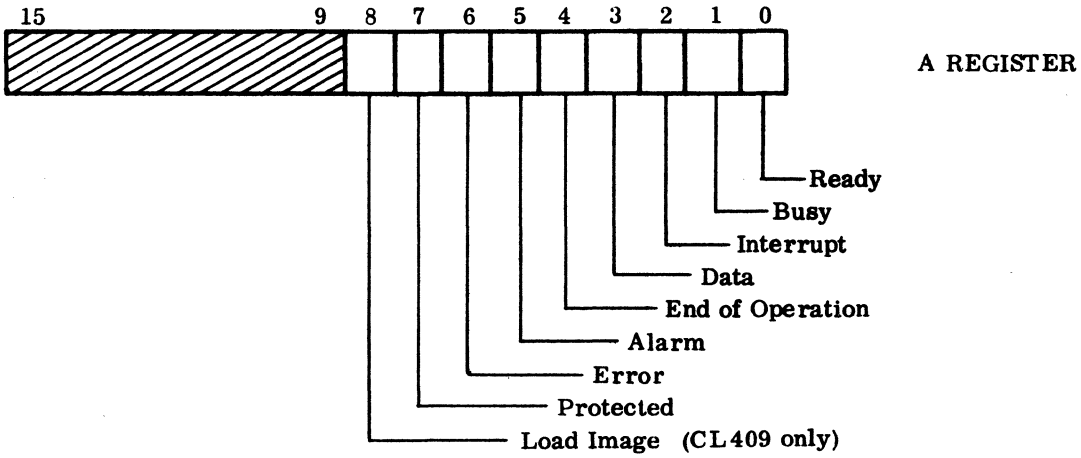


Figure 2-3. Status Code Format

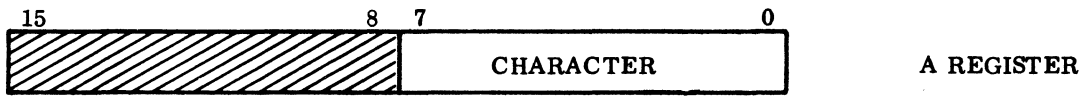


Figure 2-4. Data Transfer Format

CODES

Equipment codes and Command codes are described in the following.

CONVERTER

The W portion of the Q register (Q11 through Q15) must be all zeros for all line printer operations.

EQUIPMENT

The E portion of the Q register (Q07 through Q10) defines the line printer equipment code. This code should match the setup of the four Equipment Select jumper plugs shown in Figure 2-5.

COMMAND

The Command code (bit 00 of the Q register) defines the operation to be performed by the line printer. It must be accompanied by an Equipment code and either a Read or a Write signal. Table 2-1 gives the Command code functions.

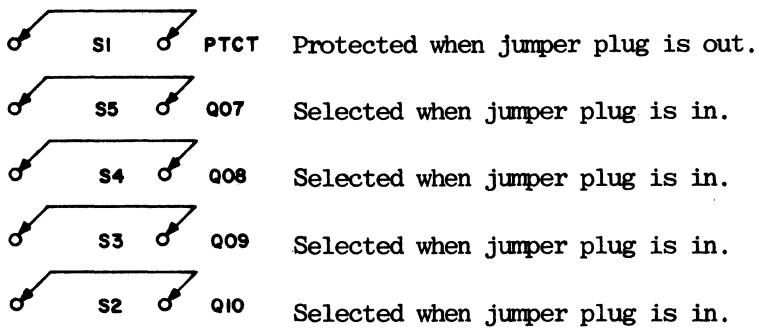


Figure 2-5. Jumper Plug Selection

DATA TRANSFER (Q00 = 0)

When bit Q00 is zero and an Output-from-A instruction is executed, the controller is directed to perform a data transfer. Data will be accepted unless one or more of the following reject conditions is present: the line printer is Not Ready, the line printer is Busy with a Print operation, data status is false, or a protect violation exists.

Bits 00 through 07 of the A register contain the character bits to be transmitted with leading zeros (A08 through A15 are zero). The first character of a line is identified as the control character and is not printed. (See Page 2-8 for description of control characters)

When six-bit characters are transmitted, bits 06, 07 of A should be zeros.

The Data Transfer command clears EOP and ERROR status.

DIRECTOR FUNCTIONS (Q00 = 1)

When Q00 is a 1 and it is accompanied by both an Equipment code and Output-from-A instruction, the controller is directed to perform a director function. Director functions are accepted if no protect violation occurs, with the following constraints: Print directive is accepted if controller is Ready, Not Busy, and Data Status is true (bit A03 = 1).

Director functions, except the Print directive, may be stacked; that is, two or more functions may be issued at the same time.

CLEAR PRINTER (A00 = 1)

This function clears the controller logic, clears EOP status, and generates the Buffer Clear signal to the line printer. It generates Clear Interrupt functions. It is subordinate to all other bits in this group except Print (A05).

CLEAR INTERRUPT (A01 = 1)

This function clears all interrupt requests and interrupt responses. It is subordinate to all interrupt requests.

DATA INTERRUPT REQUEST (A02 = 1)

This function sets the Data Interrupt Request flag. This in turn enables the generation of an interrupt when the Data status flag is true indicating that data transfer to the line printer is permitted. The interrupt request is cleared by Clear Printer or Clear Interrupt.

The interrupt response may be cleared by clearing the interrupt request as stated above, or by Data Transfer or Print functions. Before Data Transfer to the printer, Data Interrupt may be requested and the response will signal the computer that the printer is ready to receive another data transfer. Without reselecting or clearing this interrupt response, the data transfer can take place. During this data transfer, interrupt response will be removed until the printer is ready to receive another data transfer.

END-OF-OPERATION INTERRUPT REQUEST (EOP) (A03 = 1)

This function enables the generation of an interrupt on completion of an operation, when EOP occurs. The interrupt may be selected before or during the operation. An interrupt response will not occur for an operation which was ended before the selection was made. The interrupt request may be cleared by Clear Controller or Clear Interrupt.

The interrupt response may be cleared by clearing the request or by Data Transfer or Print functions.

ALARM INTERRUPT REQUEST (A04 = 1)

This function enables the generation of an interrupt when an alarm condition exists. An alarm condition that exists at the time this interrupt request is made will immediately provide a response. If the alarm condition does not exist at the time of the interrupt request, the interrupt response will be provided as soon as an alarm condition is detected. These conditions are listed in the Alarm section. The interrupt request may be cleared by Master Clear or by either A00 = 1 or A01 = 1 with A04 = 0.

The interrupt response may be cleared by clearing the request or by Data Transfer or Print functions.

PRINT FUNCTION (A05 = 1)

This function directs the line printer to initiate a print operation. A print operation lasts between the acceptance of a Print function and completion of a line of print.

A register bits 06 through 15 in this group are not used.

DIRECTOR STATUS

The line printer always replies to a status request. It therefore replies when Q00 = 1 and it is accompanied by an equipment code and a Read signal. The status responses are described below.

READY (A00 1)

Indicates that a Ready condition exists. The Ready condition must be existing before the printer can operate, and the absence of any one of several requirements can prevent this.

BUSY (A01 = 1)

Indicates that the line printer is Busy. The line printer becomes Busy:

1. After the initiation of a print cycle and until the characters have been printed.
2. If the Clear Printer (A00 = 1) directive was issued directly after the control character has been issued.

INTERRUPT (A02 = 1)

This signal indicates that an interrupt occurred. The other status bits must be monitored to determine the cause of the interrupt: bits A03 through A05 define which interrupt occurred. This status is cleared by either the Clear Printer (A00 = 1) or Clear Interrupt (A01 = 1).

DATA (A03 = 1)

This signal indicates that the line printer is ready to receive a character. If Interrupt on Data has been selected, this status will also indicate that this interrupt has occurred. The status is cleared by Clear Printer (A00 = 1) and by either Data Transfer or Print directive.

END-OF-OPERATION (EOP) (A04 = 1)

This signal indicates that the line printer has completed an operation. If Interrupt on End-of-Operation has been selected, this status bit will also indicate that this interrupt has occurred. This status is true whenever the Line Ready signal goes high. The status is cleared by Clear Printer, Data Transfer, Print.

ALARM (A05 = 1)

This signal indicates that an alarm condition is present, that is, an error or printer malfunction occurred. The status is cleared by Clear Printer (A00 = 1), Data Transfer or Print directive provided that the cause of the alarm has been corrected.

ERROR (A06 = 1)

a. For the CL408 Line Printer this signal indicates that data transfer parity error occurred. The parity error occurs when an incorrect character code is received by the line printer. The incorrect character code is printed as blank if it is a data character and ignored if a control character, i.e., it is performed as if Suppress Space was issued. The line printer stays Ready when this condition occurs. The status is cleared by Clear Printer (A00 = 1) or either Data Transfer or Print directive.

b. For the CL409 Line Printer this signal indicates that any one or any combination of Parity Error, Synchronization Error or Compare Error (indicated on the Printer console) occurred. In case of Parity Error the Line Printer stays Ready. The condition is cleared by Clear Printer (A00 = 1) or either Data Transfer or Print directive.

   In case of Synchronization Error or Compare Error the line printer becomes Busy. The condition is cleared by Clear Printer (A00 = 1) only.

PROTECTED (A07 = 1)

This bit indicates that the controller is in the protect state; that is, the protect jumper plug is absent. See Protection Logic, page 4-3. In this state, the controller accepts only instructions having a 1 on the Program Protect line. All other instructions except Director Status will be rejected. The Program Protect bit is ignored when the controller is not in the Protect state.

LOAD IMAGE (A08 = 1)

In the CL409 Line Printer this bit indicates that the next 288 characters will be transferred to the Line Printer Image Memory. If Parity Error occurs no further transmission takes place until Clear Printer (A00 = 1) is issued. Load Image status is not applicable to the CL408.

Bits A09 through A15 are not used.

CONTROL CHARACTERS

The first data character after a print operation is defined as the Control Character. It controls the paper vertical motion and will not be printed.

The printer operates in 'pre-print' mode, i.e. paper motion is performed before printing. The printer executes the Control Character immediately upon reception and does not set Busy Status. The Busy Status will be set after reception of a Print Directive.

NOTE: If a Control Character is issued, which performs a vertical paper motion and CLRP Directive is issued immediately thereafter, the Busy Status will be set until paper motion stops.

TABLE 2-2. LP control bit settings in Register A.

Bits in A							Function
A06	A05	A04	A03	A02	A01	A00	
0	x	x	x	x	0	0	Suppress space
0	x	x	x	x	0	1	Single space
0	x	x	x	x	1	0	Double space
0	x	x	x	x	1	1	Triple space
							Vertical Format Control
1	x	x	0	0	0	0	Channel 1 (T0F)
1	x	x	0	0	0	1	Channel 2 (B0F)
1	x	x	0	0	1	0	Channel 3
1	x	x	1	0	1	1	Channel 12
1	x	x	1	1	0	0	
1	x	x	1	1	0	1	Illegal as vertical
1	x	x	1	1	1	0	format
1	x	x	1	1	1	1	

Notes: a. x - don't care
b. When an illegal Vertical Control is issued the character is decoded as if A05=0.

INSTALLATION AND CHECKOUT 3

INSTALLATION

UNPACKING

1. Carefully remove wrapping from the 50-PAK controller card. Check for physical damage to the card and record any damage on the packing list. Check that the part number agrees with the parts list.
2. Remove the wrapping from the cable and check for physical damage. Record any damage on the packing list. Check that the part number agrees with the packing list.

PHYSICAL LIMITATIONS

Care must be taken to prevent damage to the controller card. The card must not be flexed, bent, or dropped.

POWER REQUIREMENTS

The controller card requires +5 vdc derived from the power supply of the computer.

CABLING AND CONNECTORS

An external interconnecting cable is available for use with the controller for connection between the computer and the line printer. The external cable (Part No. 89818500) is 25 feet long and shielded.

The internal cable (Part No. 89641800) used between the back of the computer and the connector pins on the back plane is 15.5 inches long.

The interrupt cable (Part No. 89724702) is 13.8 inches long.

The wire lists for pin assignments are in Section 8.

COOLING REQUIREMENTS

The controller card is cooled by the forced air system of the computer. No further cooling is required. Refer to the 1784 Computer Customer Engineering Manual (Publication No. 89633300) for further information concerning the cooling capabilities of the computer.

ENVIRONMENTAL CONSIDERATIONS

The environmental considerations necessary for operation (or storage) of the controller are listed in the specifications (Table 1-1).

PREPARATION AND INSTALLATION

Before installing the controller card, perform the following:

1. Remove the air-flow block from the lower slide of the card slot to be used.
2. Inspect the enclosure, card slot, PW board slides, and connector pins for physical damage.
3. Place the Equipment Number and Protect jumpers in the proper positions on the card. Refer to Tables 3-1 and 3-2 and Figure 3-1.

CAUTION

Do not install or remove controller card or cables from computer or expansion enclosure with power on.

4. Carefully install the controller card in the assigned A/Q slot. The PWA must slide in smoothly. The slot must be selected according to the equipment configuration. Refer to Figure 3-2 and to the 1784 Computer CE Manual for card placement.
5. Place the interrupt cable in the position on the backplane as indicated in Table 3-3.
6. Install the internal cable between connector P2 of the position the controller PWA is placed in and the applicable output connector position of the CPU or expansion enclosure connector panel.
7. Install the external cable between the internal cable output connector and the line printer.

Table 3-1. Jumper Plug Selection

SELECTION	LOCATION	PINS	REMARKS
PROTECT (S1 on logic diagram)	U54	1 and 10 (Marked PTCT on PW Assy)	Protected when Jumper plug is out.
EQUIPMENT CODE SELECT (S5 on logic diagram)	U54	5 and 6 (Marked Q07 on PWB)	Selected when jumper plug is in.
(S4 on logic diagram)		4 and 7 (Marked Q08 on PWB)	
(S3 on logic diagram)		3 and 8 (Marked Q09 on PWB)	
(S2 on logic diagram)		2 and 9 (Marked Q10 on PWB)	

Table 3-2. Equipment Number Selection

LINKS		Q10 (S2)	Q09 (S3)	Q08 (S4)	Q07 (S5)
Hexadecimal Code	0	0	0	0	0 *
	1	0	0	0	1 **
	2	0	0	1	0
	3	0	0	1	1
	4	0	1	0	0
	5	0	1	0	1
	6	0	1	1	0
	7	0	1	1	1
	8	1	0	0	0
	9	1	0	0	1
	A	1	0	1	0
	B	1	0	1	1
	C	1	1	0	0
	D	1	1	0	1
	E	1	1	1	0
	F	1	1	1	1

NOTE: * A binary 0 indicates jumper plug out.
** A binary 1 indicates jumper plug in.

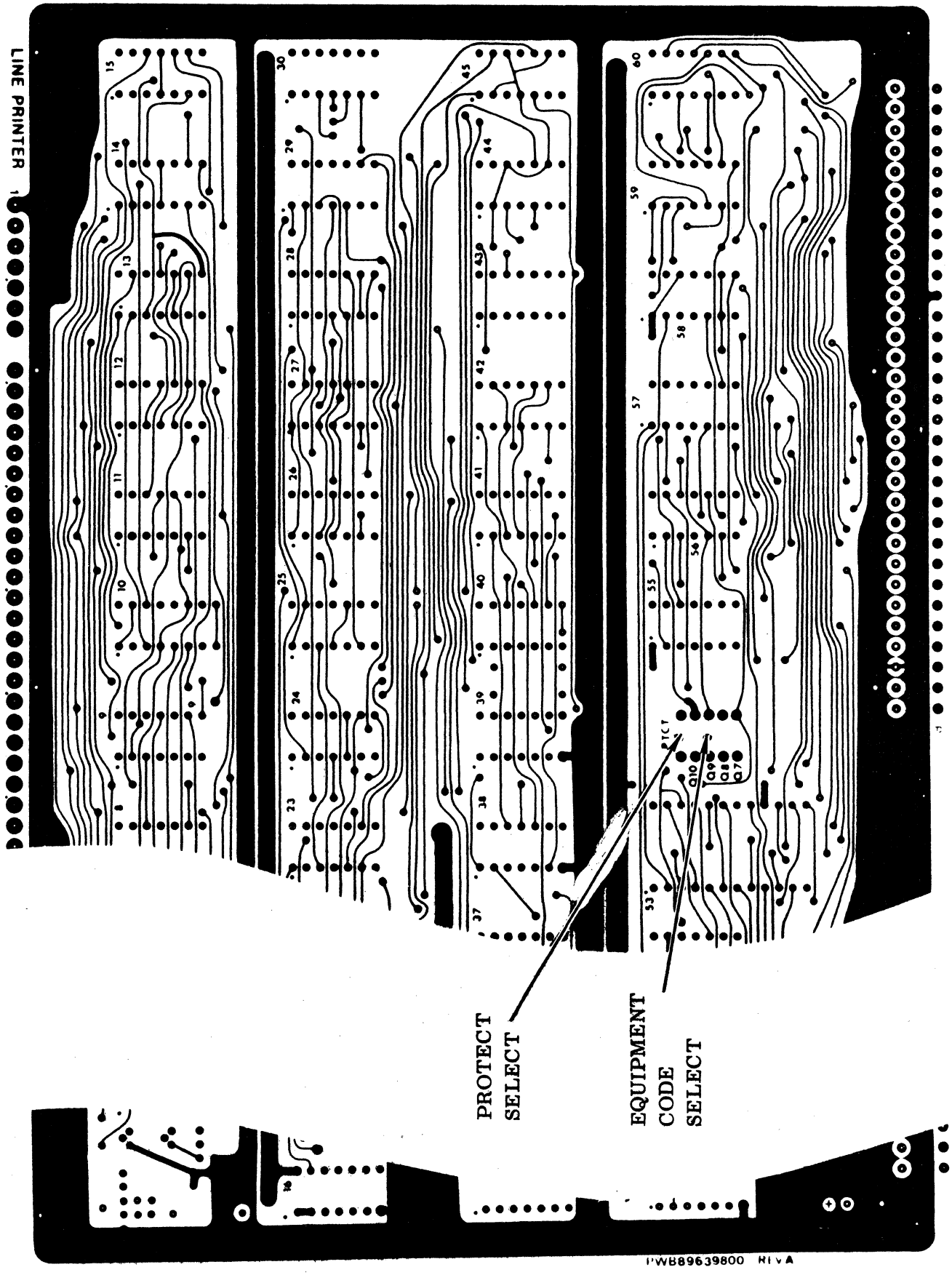


Figure 3-1. Jumper Plug Location on PWA

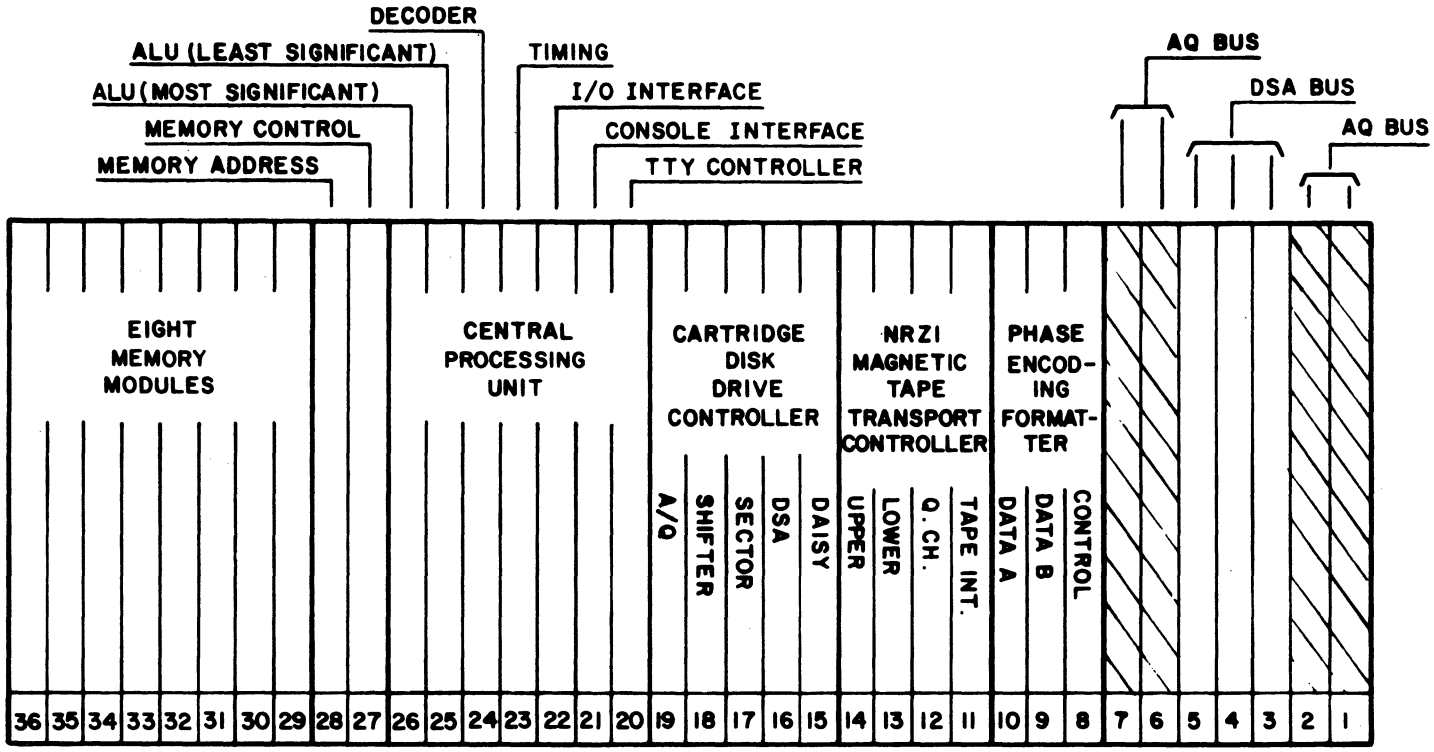


Figure 3-2. Location for Installation of Controller PW Assembly (A/Q Bus)

Table 3-3. Interrupt Pin Assignments

Line Printer Controller	
EOP Interrupt	P1B24
Common Interrupt	P1B25
Data Interrupt	P1B26
Alarm Interrupt	P1B27

Connections may be made to any of the following:

CPU	Position	
Line 1	25	P1B10
Line 2	25	P1A7
Line 3	25	P1B7
Line 4	25	P1A5
Line 5	25	P1A6
Line 6	25	P1B6
Line 7	25	P1B5
Line 8	26	P1A10
Line 9	26	P1B10
Line 10	26	P1A7
Line 11	26	P1B7
Line 12	26	P1A5
Line 13	26	P1A6
Line 14	26	P1B6
Line 15	26	P1B5

CHECKOUT

1. Refer to Section 2 of this manual and the 1784 Computer Reference Manual for operation of the controller.
2. Determine that proper voltages are supplied to the controller card by measuring +5 vdc between test points 1 (ground) and 63 on the PWA.
3. Perform diagnostics check as described in the Systems Maintenance Monitor (SMM17) Manual, Publication Number 60182000.

THEORY OF OPERATION 4

This section presents a general description of the equipment, using an overall block diagram (Figure 4-1) and timing diagrams (Figures 4-2 through 4-4). Descriptions are keyed to the detailed logic diagrams in Section 5 and afford a basis for understanding the detailed description of the specific circuits in that section.

NOTE

It is assumed that the reader is familiar with Control Data equipment and with the programming characteristics of the computer as described in the 1784 Computer System Reference Manual, Publication Number 89633400.

GENERAL

The controller interfaces the computer through the A/Q channel.

In Write Data operation the data is transferred to the line printer from the eight least significant bits of the A register. The line printer incorporates a full line of buffered characters and the data is stored there until the controller issues a Print command.

The operation of the line printer can be divided into two phases: 1) when it receives data from the controller and stores it, and 2) the Print cycle, in which it prints directly from the buffer without intervention from the controller. The controller interfaces the line printer on a one-to-one basis.

When the line printer receives a character, it deactivates the Character Request signal.

The data from the controller's data register, together with the Parity bit, is strobed by the Strobe signal, from the controller to the line printer.

When the data has been sampled, the line printer activates the Character Request again (see Figure 4-4).

When the line printer enters the Print cycle, after a reception of a Print command, it deactivates the Line Ready and Character Request signals, until the Print cycle is ended. Then it activates the Line Ready and Character Request signals again, and the data for the next line can be transmitted (see Figure 4-3).

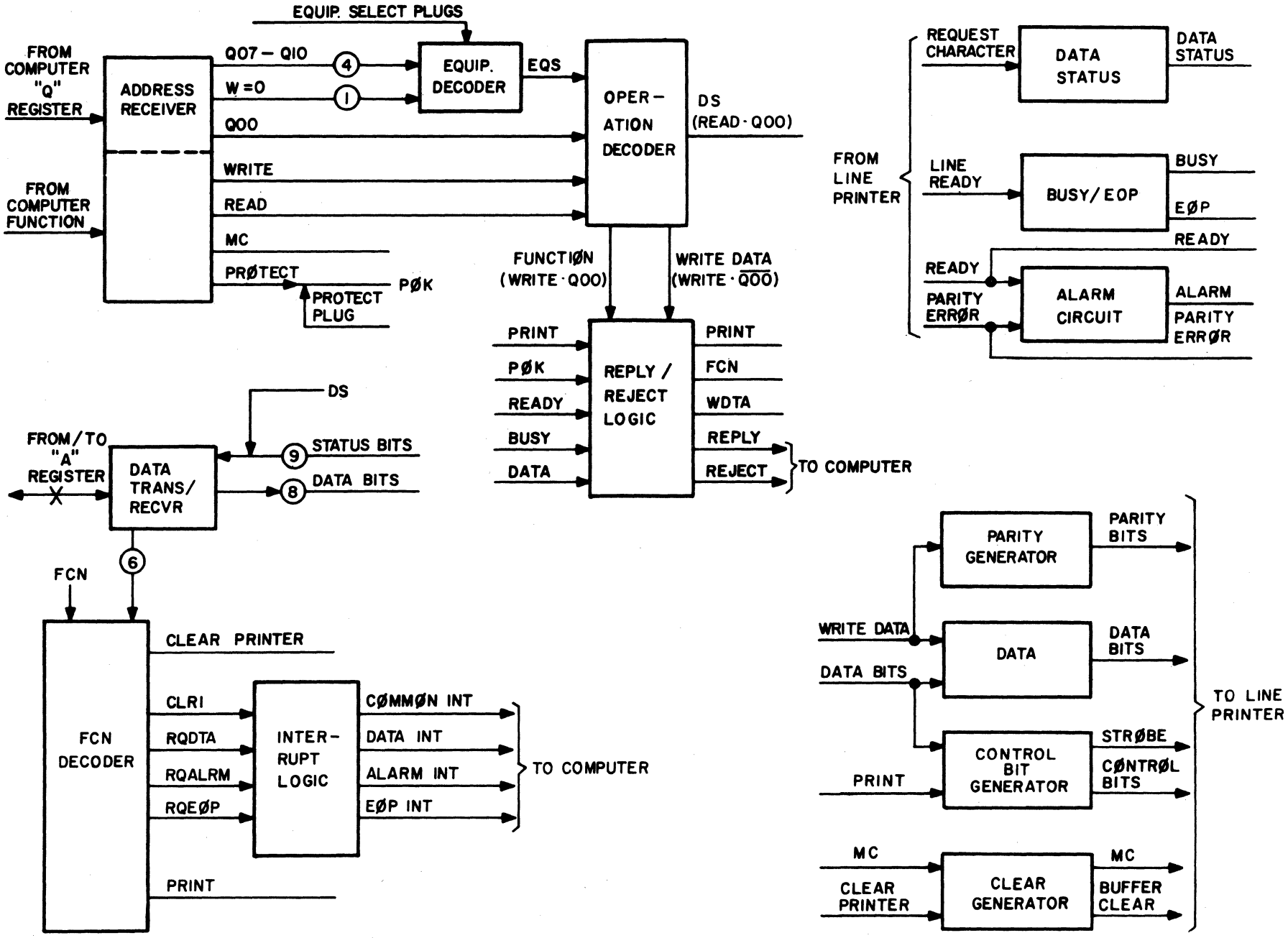


Figure 4-1. Line Printer Controller Block Diagram

A/Q RECEIVERS/TRANSMITTERS

The receivers of the A/Q channel are TTL inverters or gates. Each receiver dissipates one TTL load from the channel.

The transmitters are open collector TTL buffers (7438s).

PROTECTION LOGIC

The circuit disables controller operation from an unprotected input during I/O instructions.

When the Protect jumper is absent (device protected) and the A/Q Protect bit is high at time of Read or Write, the POK (protect OK) signal is generated. If the A/Q Protect bit is low at that time, POK will not be generated. POK signal will always be generated when the Protect jumper is present (unprotected).

EQUIPMENT AND OPERATION DECODER

When bits Q07 through Q10 match the equipment number of the controller, bits Q11 through Q15 are all zeros (W=0 is low) and Read or Write signals are present, the EQST flip-flop sets on the leading edge of the T1 clock pulse. The EQST signal enables the Operation decoder, which selects the operations to be executed, according to Table 4-1.

Table 4-1. Read/Write Functions

Q00	WRITE	READ
1	Director Function (FCN)	Director Status (DS)
0	Write Data (WDTA)	Illegal

After the selection is made, checks are performed to determine whether the operation can be executed. If yes, the Reply signal is generated to the computer, otherwise the Reject signal is generated.

The illegal operation ($\overline{Q00}$·READ) is always rejected.

Director Status operation is always executed. It transfers the current status bits of the controller to the computer.

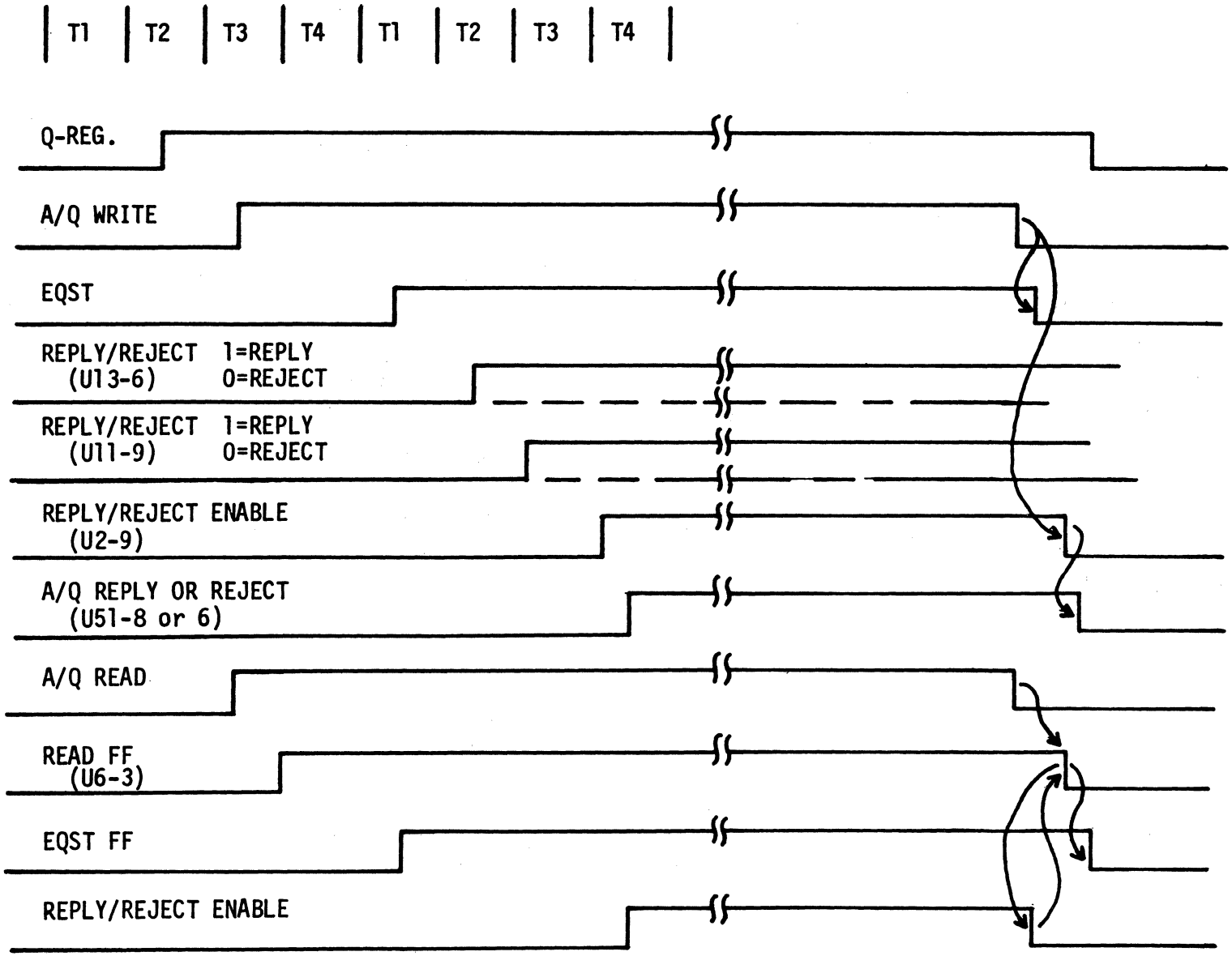


Figure 4-2. A/Q Timing Read/Write

DATA TRANSFER

Data transfer to the line printer is performed by Write Data (WDTA) operation. The operation transfers bits A00 through A07 from the computer to the line printer. The operation is executed and Reply generated, provided the following equation holds true:

$$\text{DATA} \cdot \text{POK} \cdot \text{READY} \cdot \overline{\text{BSY}} \quad 1$$

i.e., conditions for Reply are:

1. DATA STATUS is high (Character Request from line printer is active).
2. No protect violation.
3. The line printer is Ready (Ready signal from line printer is active).
4. The line printer is Not Busy and the Line Ready signal is active.

When the controller can execute this operation it performs the following:

1. Stores bits A00 through A07 into the Data register.
2. Generates the parity bit and stores it in the Parity FF.
3. Generates a reply to the computer.
4. Starts the counter, which will generate the strobe signal to the line printer approximately 1.5 microseconds after the data is present on the lines to the line printer.
5. Clears the Data FF.

After the line printer has sampled the data, it deactivates the Character Request signal. When CHARACTER REQUEST drops, the one-shot simulator generates a pulse 400 nsec wide, which clears the Strobe FF. When CHARACTER REQUEST is activated again, it sets the Data FF and enables transfer of another character. Should a parity error occur during transfer of a character, the Parity Error signal from line printer becomes active, setting the Parity Error FF, which in turn sets the alarm indicator.

The Parity Error FF can be cleared by either CLRP, WDTA, or PRINT functions.

DIRECTOR FUNCTION

This operation is performed provided the following equation holds:

$$\text{POK} \ (\overline{\text{A05}} + \text{READY} \cdot \overline{\text{BSY}} \cdot \text{DATA}) = 1$$

The Director Function is further decoded according to the contents of the A register, as shown in Table 4-2.

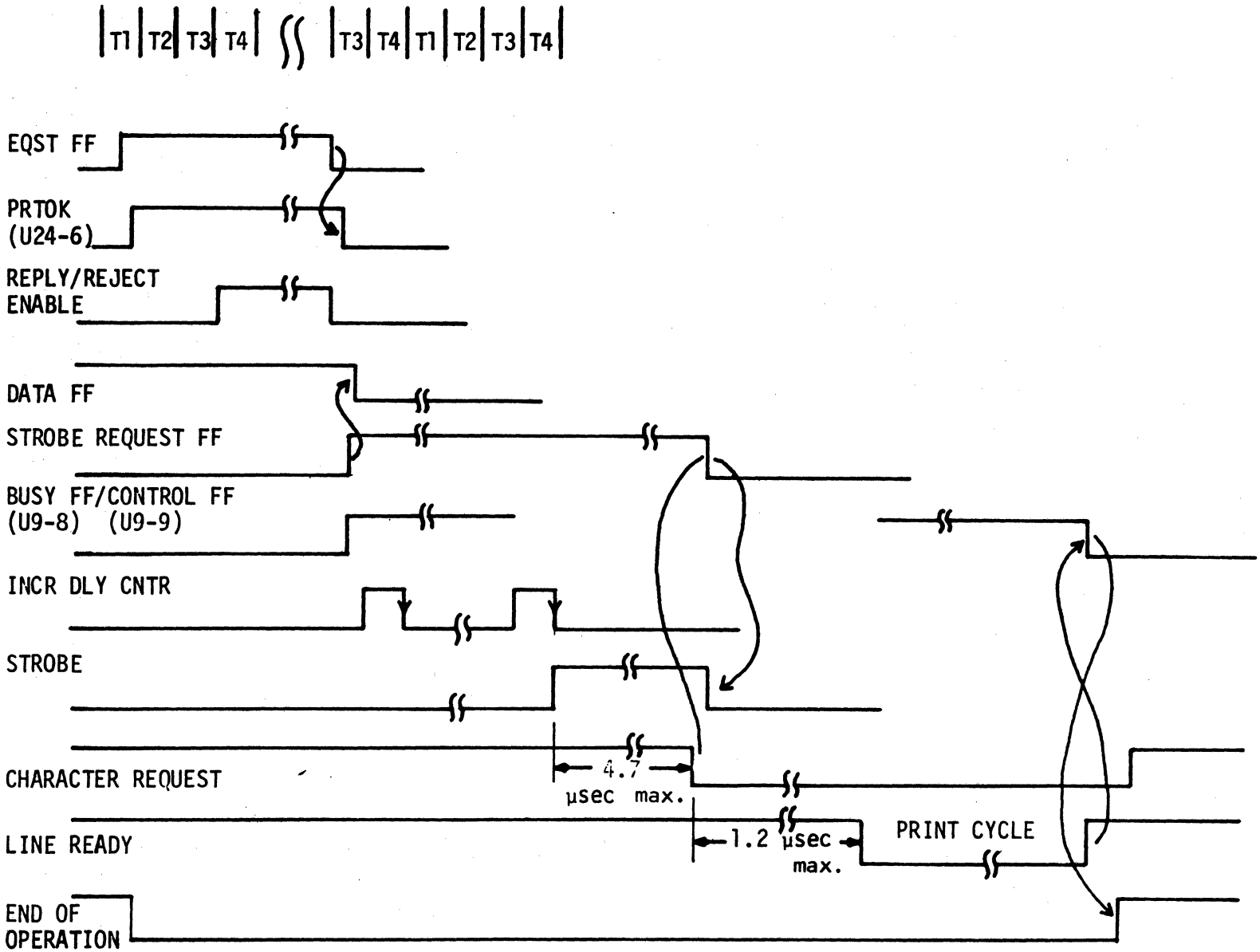


Figure 4-3. Print Operation Timing

Table 4-2. Director Functions

A REGISTER	SIGNAL	
A00 = 1	Clear Controller	(CLRP)
A01 = 1	Clear Interrupt	(CLRI)
A02 = 1	Request Interrupt on Data	(RQDTA)
A03 = 1	Request Interrupt on EOP	(RQEOP)
A04 = 1	Request Interrupt on Alarm	(RQALRM)
A05 = 1	Print command	

The reply conditions can be divided as follows:

a. If the Print command is issued (A05 = 1), the controller has to be Ready, Not Busy, and DATA STATUS should be set, in addition to POK being active.

b. If A05 = 0, the only condition is POK being active.

The CLRP function clears the controller, and generates the Buffer Clear signal to the line printer.

The CLRI and Interrupt Request functions are used in the interrupt logic circuit.

The Print function starts the Print cycle. It performs the following:

1. Sets the Print FF, which generates the control bit to the line printer. As the timing of that bit is similar to the data bits, the Data Status FF has to be set to enable that function.
2. Starts the Strobe generating counter.
3. Clears the Data FF.

When the line printer accepts the Control bit, it deactivates the Character Request and Line Ready signals.

When the Print FF is set, an early Busy condition is set. That condition remains until the line printer terminates the Print cycle; then it activates the Line Ready signal again, which sets EOP (End of Operation) condition in the controller, and activates the Character Request, which sets the Data FF and enables the controller to accept data for next line.

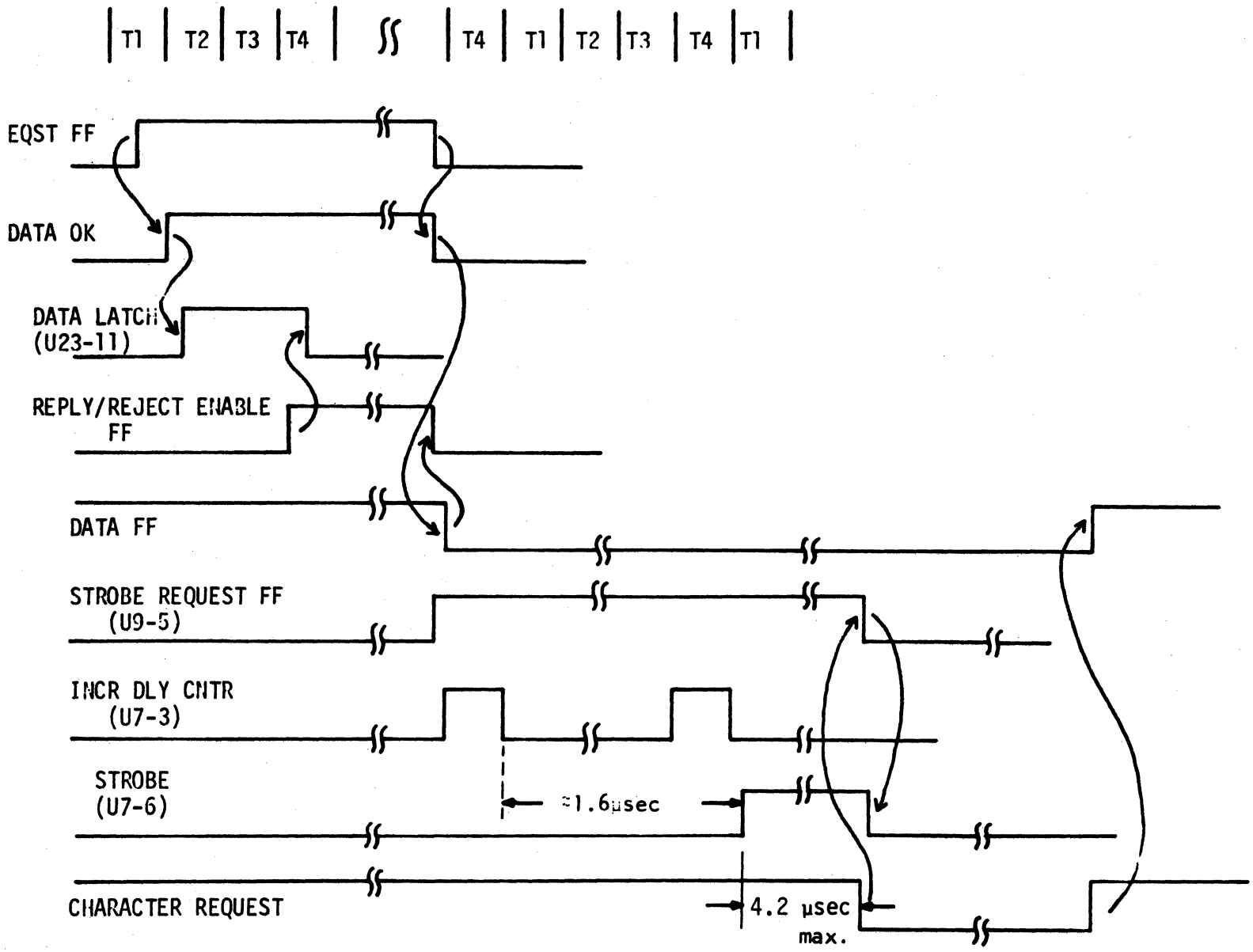


Figure 4-4. Data Transfer

INTERRUPT LOGIC

The controller generates interrupt signals to the computer on three conditions, provided the interrupt has been selected:

1. Data FF is set.
2. EOP has occurred (the Print cycle has terminated).
3. Alarm has occurred.

Interrupt generation is selected by the program by means of bits A02 through A04 with FCN.

When the bit in A is set, the proper Request FF will be set on the trailing edge of the Write pulse, enabling the Interrupt Transmitter gate.

CLRI function clears all request flip-flops, thereby preventing interrupts from being transmitted.

The CLRI and Request function can be executed in the same FCN operation. In that case the Request function takes precedence over the CLRI function.

When the Data or Alarm Request FFs are set, the interrupt is generated immediately when the Data or Alarm condition becomes true.

The EOP Interrupt is generated only if the Request FF has been set before the EOP condition occurred. The Alarm condition will exist if either of the following has occurred:

1. The Parity Error FF is set, or
2. The Ready signal from the line printer drops, indicating that a malfunction has occurred.

The interrupts are transmitted to the computer as DATA INT, EOP INT, and ALARM INT signals as well as the COMMON INT which is active whenever any of the other three are active.

CLOCK GENERATOR AND TIMING COUNTER

The clock pulses are generated by a Johnson counter, working at a frequency of 10 MHz. The counter generates four clock pulses of 100 nsec (T1, T2, T3, T4) at a repetition rate of 400 nsec.

The T4 clock pulse is the input to the timing counter, which generates the Strobe and Clear signals.

KEY TO LOGIC SYMBOLS

Publication No. 89723700 (Key to Logic Symbols) or its equivalent lists the symbols used in the logic diagrams in this manual and gives a short description of the functions they represent. The symbols conform generally to Control Data usage (Microcircuit Handbook, Publication Number 15006100), using the polarity logic convention.

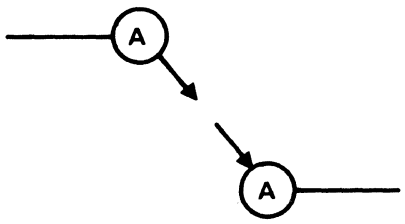
The following paragraphs describe the signal flow conventions used.

SIGNAL FLOW

Input signals are drawn coming from the left or above; output signals are drawn going to the right or down.

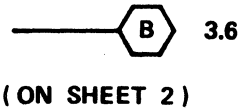
The signal lines are sometimes interrupted to allow logical grouping of components. At each such interruption one of the following indicators is used:

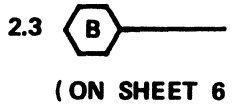
ON-SHEET CONTINUATION REFERENCE SYMBOLS



These symbols when used with the logic symbols in the following diagrams indicate that a connection exists between two points on a sheet. The arrows attached to each circle point from signal origin to signal destination. The letters C, H, I, O, and P are not used inside the circles, since they bear special significance on logic diagrams.

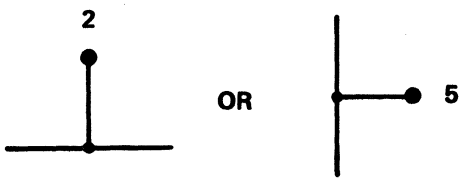
OFF-SHEET CONTINUATION REFERENCE SYMBOLS (Q00 = 0)





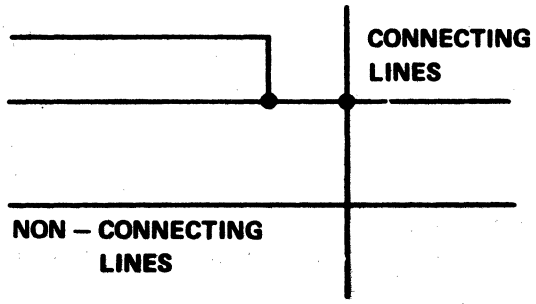
These symbols when used with the logic symbols in the following diagrams indicate that a common signal point exists between two sheets in a series of related drawings. These symbols point from output to direction of input as shown in the illustration. The letters C, H, I, O, and P are not used in the hexagons, since they bear special significance on logic diagrams. The number(s) next to each hexagon indicate the sheet(s) that the signal is continued from or on. For instance, the numbers 3.6 refer to sheets 3 and 6, while 2.3 refers to sheets 2 and 3. It should be noted that the referenced sheet number(s) is always placed opposite the line extending from the hexagon.

TEST POINTS



The test point symbol on the logic diagram shows the connection of a test point on the printed wiring board (PWB). The number adjacent to the symbol refers to the test point position on the PWB at the edge opposite the connectors. Only test point 1 is labeled on the edge of the PWB.

CONNECTING AND NON-CONNECTING LINES

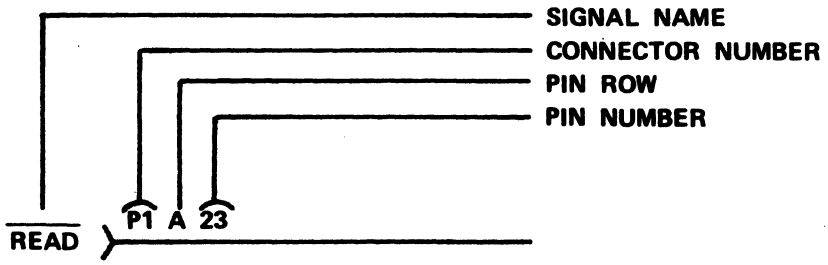


Lines connected to a common point or at a junction point are shown in the upper part of this illustration. No more than four lines are connected to a common point in the diagrams.

Lines crossing but not connected are shown in the lower part of this illustration.

CONNECTORS

Connectors are represented on the logic diagram by the symbol for a female connector, for both input and output signals. The name of the signal is placed in the open end of the connector symbol, using the full name of the signal or the common abbreviation applicable to logic diagrams. The connector number, pin row, and pin number are located above the line extending from the connector symbol.



EQUIPMENT AND OPERATION DECODER

Refer to Sheet 5 of Logic Diagram 89639900.

The function of this circuit is to decode and define the operations to be performed by the controller. The inputs to the circuit are derived from the computer A/Q channel. The controller is capable of performing the following operations:

1. WRITE DATA (WRDTA) = WRITE·$\overline{Q00}$
2. Write Director Function (FCN = WRITE·Q00)
3. Read Director Status (DS=READ·Q00)

To address the controller, the equipment code contained in bits Q07 through Q10 must match the setting of the Equipment Select jumper plugs (S2-S5) on the controller. In addition the W portion of the Q register (Q11-Q15) must be all zeros; i.e., $\overline{W=0}$ signal must be true.

If the Q register and the jumper settings match, W=0 is true, and a $\overline{READ}$ or $\overline{WRITE}$ signal is present, the controller generates a Reply signal to the computer provided the condition exists. When an illegal operation is detected the controller generates a Reject. The controller always responds with Reply to a Read Director Status operation.

EQUIPMENT NUMBER DECODER (SHEET 5)

The equipment number of the controller is determined by the setting of four jumpers (S2-S5). Each jumper, when made, connects one of the inputs of the Exclusive OR (XOR) gate (U56) to a low. Bits Q7 through Q10 are then compared to the corresponding settings of the jumper plugs. The outputs of the four XOR gates (U56) are ANDed at the U40 AND gate. When the output of that gate is true a match exists. The output of that gate is ANDed to the W=0 signal (gate U4-4 and 5). When the W=0 is low, the gate generates the EOK signal.

PROTECT LOGIC (SHEET 5)

This circuit protects the controller from operating for an I/O instruction issued from an unprotected core. When the controller is in the Protected state (jumper S1 out), and the $\overline{\text{PROTECT}}$ signal from the computer not active, the POK signal from U43-11 is not active and the I/O operation is rejected. A Director Status (DS) request is not rejected when a protect violation occurs.

WRITE OPERATION (SHEET 5)

When the controller is addressed and the $\overline{\text{WRITE}}$ signal is active, gate U20-6 enables the EQST FF (U2-5). The FF sets on the leading edge of clock pulse T1, generating the EQST signal. The signal enables the operation decoding gates (U12). When Q00 is a 0, gate U12-8 generates the WDTA signal. When the Q00 is a 1, gate U12-6 generates the FCN signal.

WRITE DATA (SHEET 5)

When the WDTA signal (U12-8) is generated, a check is performed to determine whether the operation can be performed. The conditions are ANDed at gate U24 and the $\overline{\text{DTAOK}}$ signal is generated by gate U24-8. The $\overline{\text{DTAOK}}$ signal generates the $\overline{\text{REPLY}}$ signal and starts the timing sequence to transfer the data to the line printer.

DIRECTOR FUNCTION (SHEET 5)

When gate U12-6 generates the FCN signal, a check is performed to determine whether that particular operation is a Print request. If A05=1, the $\overline{\text{PRTOK}}$ signal is generated by gate U24-6 provided the conditions for execution

exist. If A05=0, request gate U15-8 generates the FCNOK signal. Either of them generates the REPLY signal (U13-6). $\overline{\text{PRTOK}}$ starts the timing sequence for printing. Any of the signals is used to decode the A-channel bits to determine the particular operation to be performed, i.e., Clear Controller and Printer (CLRP, U15-11→U14-11), Clear Interrupt (CLR1, U14-11→U14-8), or Interrupt Requests. U14-11 and U14-8 are located on sheet 2.

Write operations are terminated when the computer drops the $\overline{\text{WRITE}}$ signal.

READ OPERATION (SHEET 5)

When the $\overline{\text{A/Q READ}}$ signal is active and the controller is addressed (gate U20-6), it enables the EQST FF (U2) and the Read Delayed FF (U6). The Read Delayed FF is incorporated to delay the Read operation of the controller until after the $\overline{\text{REPLY}}$ to the computer is dropped. The EQST FF sets on the leading edge of clock pulse T1. The EQST signal (U2-5) enables the decoder gate (U13-8), which generates the $\overline{\text{DS}}$ signal if Q00=1. The signal generates the REPLY (U13-6) and enables the status bits to the A channel to ensure stable data until the Reply drops.

REPLY/REJECT LOGIC (SHEET 5)

When the EQST FF (U2) is set on T1, the operation to be performed is checked to determine whether it can be executed. On the leading edge of clock pulse T3, the REPLY signal (U13-6) is strobed into the RR Control FF (U11-9). If the REPLY signal is a 1 the FF is set and Reply conditions exist, otherwise it does not set. Both outputs of that FF (U11-9 and 8) are enabled to the computer when the RR Enable FF (U2-9) is set (on the leading edge of the T4 clock pulse). When the computer drops the $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ signals, the RR Enable FF is reset, terminating the $\overline{\text{REPLY/REJECT}}$ signal to the computer.

DATA REGISTER AND PARITY GENERATOR, INTERRUPT LOGIC

Refer to sheet 2, 3 and 5 of Logic Diagram 89639900.

The Data register (U53 SHEET 2) is used to hold the characters, which may consist of up to eight bits each, to be sent to the line printer through U48-U52 (see sheet 3). The Data register is enabled by the WDTAOK• $\overline{\text{R/RENABLE}}$ signal from U23-11 and U58-2 (sheet 5), and its output is connected directly to the data transmitters. The parity generator (U38 SHEET 2) generates an odd parity bit that is transmitted to the line printer through the Parity Bit FF (U11) and U52 (sheet 3) together with the data. Nine bits (eight data bits plus parity) are actually transmitted to the line printer.

INTERRUPT LOGIC (SHEET 2)

This logic is used to generate the interrupt response requested by the computer.

Four interrupt lines are provided: Interrupt on EOP, Interrupt on Data, Interrupt on Alarm, and a common interrupt which is the logical OR of the other three. The interrupt responses are enabled by the request flip-flops.

The Data Interrupt Request FF (U27-6) is enabled by bit A02 (U44-3 on sheet 5) at the time of the Director Function, the EOP Interrupt Request FF (U27-8 SHEET 2 by A03 (U44-8 on sheet 5), and the Alarm Interrupt FF (U26-6 SHEET 2) by A04 (U44-11 on sheet 5). When the FFs are set they enable the corresponding transmitting gates (U55 SHEET 2).

CONTROL LOGIC AND TIMING GENERATOR

Refer to sheet 4 of Logic Diagram 89639900.

CONTROL LOGIC

The function of this logic is to provide the correct timing needed to operate the line printer. When either a WDTA or Print operation is to be performed, the Strobe Request FF (U9-9) sets on the trailing edge of the WRITE pulse. When the FF is set, $\overline{\text{RQSTRB}}$ (U9-8) clears the Data FF (U19) and enables the timing counter (U10). The clock to the counter is the T4 clock pulse. After four clock pulses, output 3 (U10-6) of the counter is true, enabling the $\overline{\text{STROBE}}$ pulse from U7-6. The $\overline{\text{STROBE}}$ is then transmitted to the line printer. When the line printer drops the Character Request Signal, FF U5 enables the Strobe Request FF, terminating the Strobe signal. When the line printer is ready to receive another character, it activates the Character Request signal again. The Data FF (U19-9) is then set, enabling further transmission.

When the Print operation is to be performed, the Busy FF (U26-8) is set on the trailing edge of the Write signal.

Gate U26-9 generates the Control Bit signal, which, when strobed by the Strobe signal, instructs the line printer to enter the Print cycle. The cycle is initialized at the line printer, dropping the Character Request and Line Ready signals. When the Print cycle terminates, the line printer activates the Line Ready signal again. On the leading edge of the signal, the EOP FF (U25-5 SHEET 2) is set and the Busy FF is reset. Later the Data FF is set by the leading edge of Character Request.

TIMING GENERATOR (SHEET 4)

Four consecutive clock pulses (T1, T2, T3, T4) are generated. Each of them is 100 nsec in duration and occurs every 400 nsec. These pulses are generated by a counter (U3-8 and U19-5). The main frequency of 20 MHz is obtained from the oscillator circuit and then divided by two in U3-5.

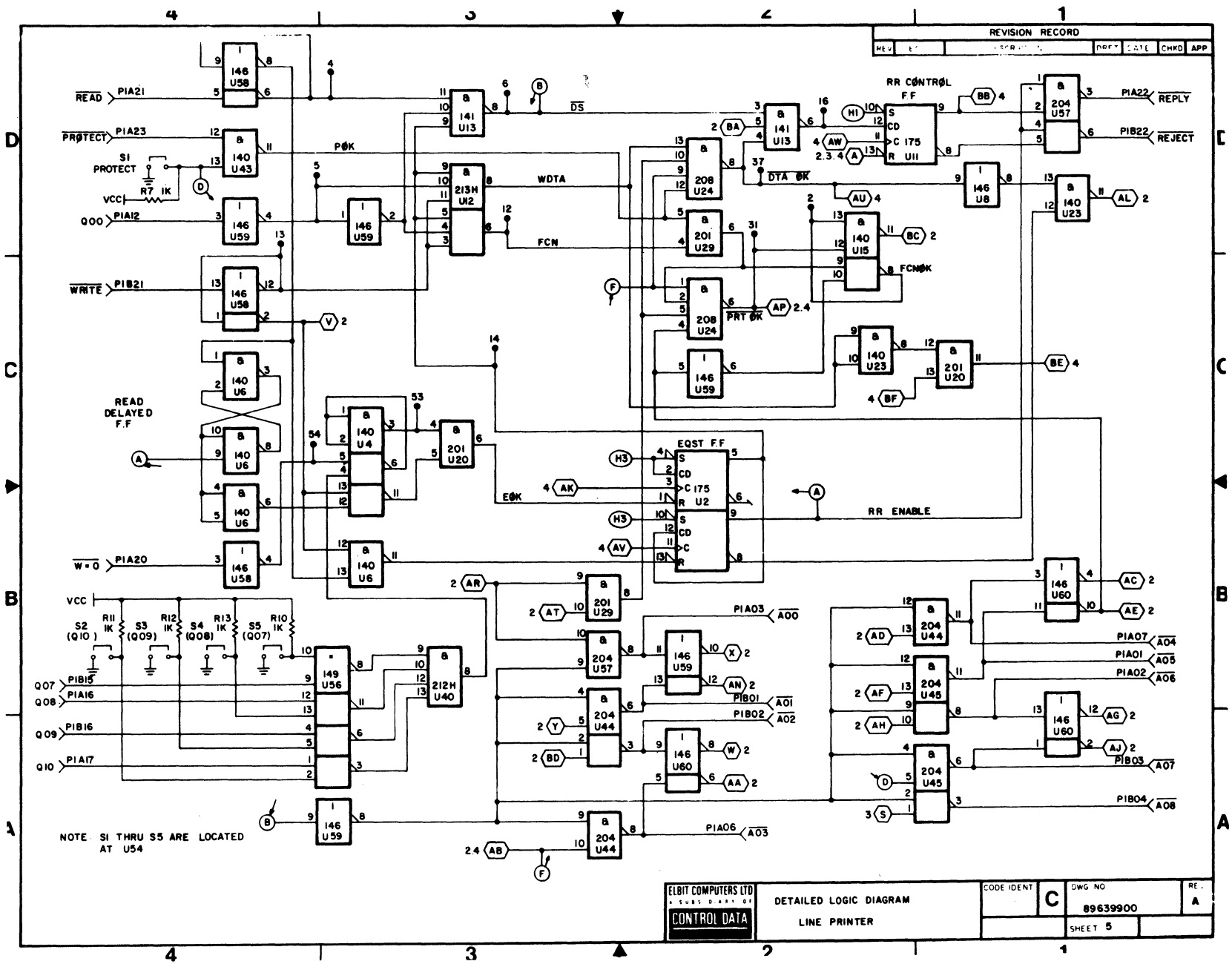
DIFFERENTIAL TRANSMITTERS/RECEIVERS

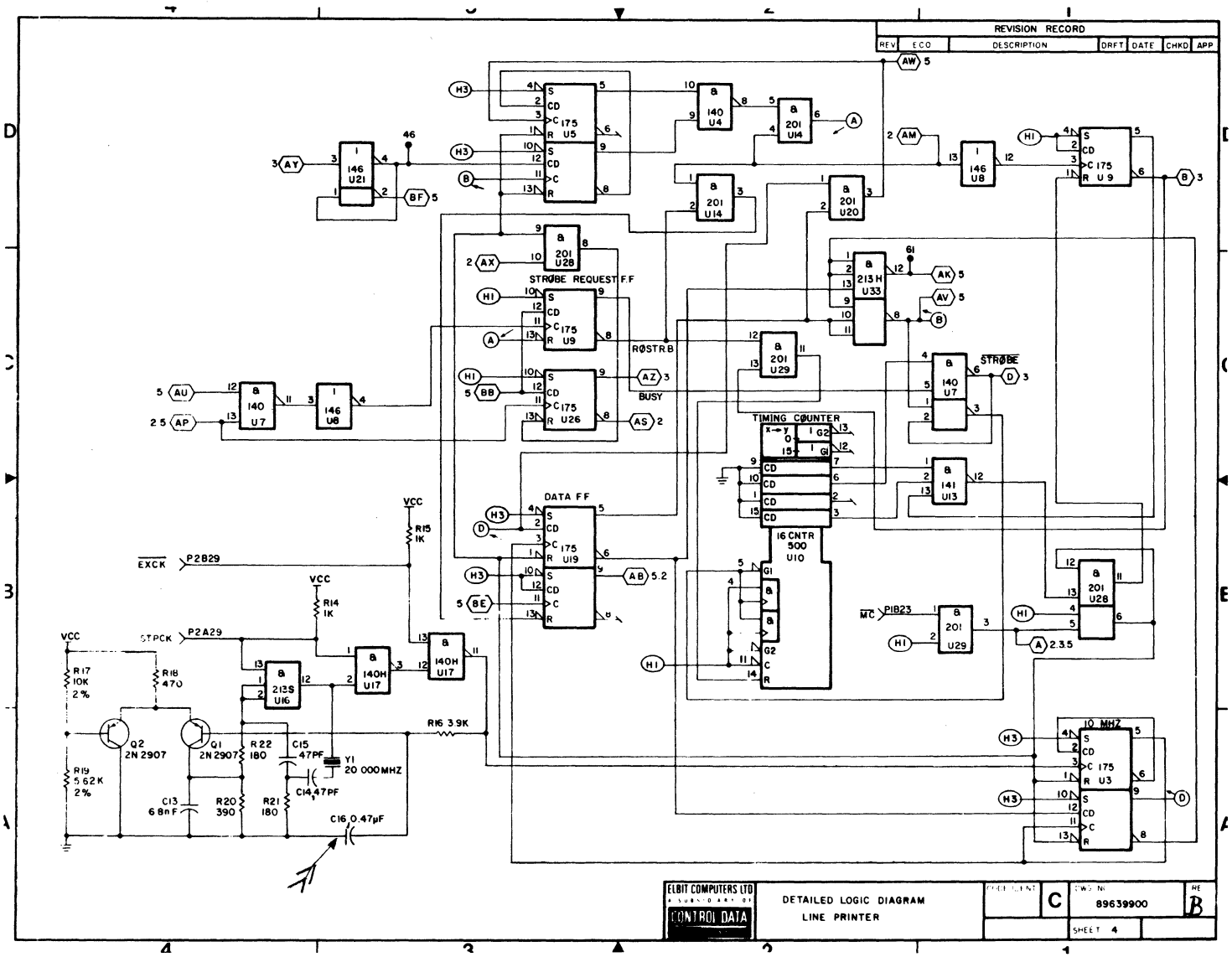
Refer to sheet 3 of Logic Diagram 89639900.

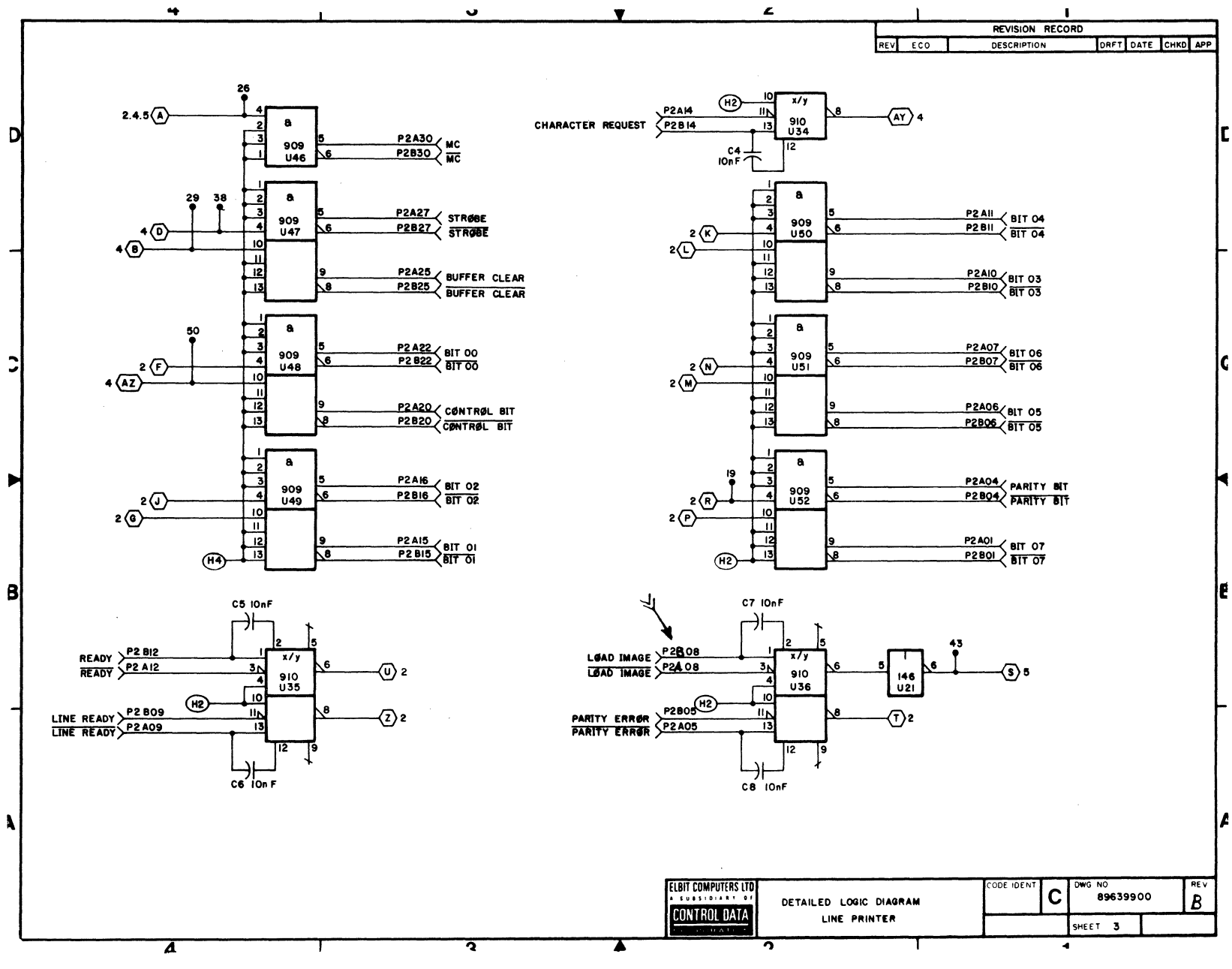
Interface between the controller and the line printer is accomplished by using logic transmitters/receivers in differential mode.

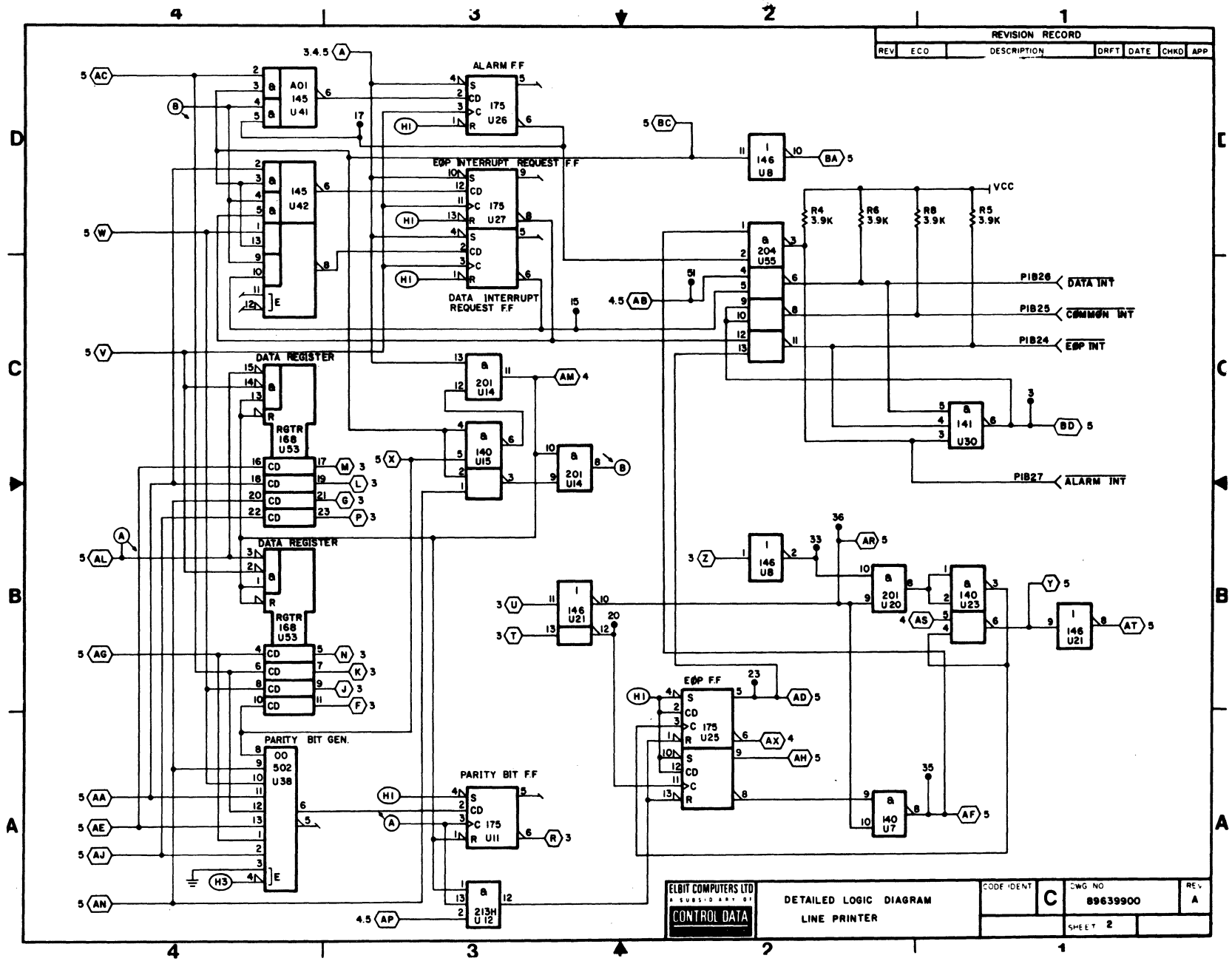
The receivers (U34, U35, and U36) are type 910, and the transmitters (U46 through U52) are type 909.

Ready, Line Ready, Character Request, Parity Error, and Load Image are each received from the line printer affecting the related circuitry as discussed.


REVISION RECORD
READ PIA21
PROTECT PIA23
S1 PROTECT
R7 1K
VCC
Q00 PIA12
WRITE PIB21
W=0 PIA20
READ DELAYED F.F
S2 (Q10)
S3 (Q09)
S4 (Q08)
S5 (Q07)
R11 1K
R12 1K
R13 1K
R10 1K
Q07 PIB15
Q08 PIA16
Q09 PIB16
Q10 PIA17
NOTE S1 THRU S5 ARE LOCATED AT U54
DS
PØK
WDTA
FCN
EQST F.F
EØK
RR CONTRØL F.F
DTA ØK
PRT ØK
FCNØK
RR ENABLE
PIA03 A00
PIB01 A01
PIB02 A02
PIA06 A03
PIA07 A04
PIA01 A05
PIA02 A06
PIB03 A07
PIB04 A08
PIA22 REPLY
PIB22 REJECT
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
LINE PRINTER
CODE IDENT C
DWG NO 89639900
REV A
SHEET 5


REVISION RECORD
REV | ECO | DESCRIPTION | DRFT | DATE | CHKD | APP
STROBE REQUEST F.F
DATA F.F
TIMING COUNTER
16 CNTR 500 U10
10 MHZ
RØSTRB
BUSY
STRØBE
VCC
R15 1K
R14 1K
R16 3.9K
R17 10K 2%
R18 470
R19 5.62K 2%
R22 180
R20 390
R21 180
C15 47PF
C14 47PF
C13 6.8nF
C16 0.47μF
Y1 20 000MHZ
Q1 2N2907
Q2 2N2907
EXCK
P2829
STPCK
P2A29
MC
P1B23
ELBIT COMPUTERS LTD
CONTROL DATA
DETAILED LOGIC DIAGRAM
LINE PRINTER
C
89639900
B
SHEET 4


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
2.4.5 A
26
909 U46
P2A30 MC
P2B30 MC
29 38
4 D
4 B
909 U47
P2A27 STROBE
P2B27 STROBE
P2A25 BUFFER CLEAR
P2B25 BUFFER CLEAR
50
2 F
4 AZ
909 U48
P2A22 BIT 00
P2B22 BIT 00
P2A20 CONTROL BIT
P2B20 CONTROL BIT
2 J
2 G
909 U49
P2A16 BIT 02
P2B16 BIT 02
P2A15 BIT 01
P2B15 BIT 01
H4
CHARACTER REQUEST
P2A14
P2B14
H2
910 U34
AY 4
C4 10nF
2 K
2 L
909 U50
P2A11 BIT 04
P2B11 BIT 04
P2A10 BIT 03
P2B10 BIT 03
2 N
2 M
909 U51
P2A07 BIT 06
P2B07 BIT 06
P2A06 BIT 05
P2B06 BIT 05
19
2 R
2 P
909 U52
P2A04 PARITY BIT
P2B04 PARITY BIT
P2A01 BIT 07
P2B01 BIT 07
H2
C5 10nF
READY P2B12
READY P2A12
LINE READY P2B09
LINE READY P2A09
910 U35
U 2
Z 2
C6 10nF
C7 10nF
LOAD IMAGE P2B08
LOAD IMAGE P2A08
PARITY ERROR P2B05
PARITY ERROR P2A05
910 U36
146 U21
43
S 5
T 2
C8 10nF
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
LINE PRINTER
CODE IDENT C
DWG NO 89639900
REV B
SHEET 3


REVISION RECORD
REV ECO DESCRIPTION DRFT DATE CHKD APP
ALARM F.F
EOP INTERRUPT REQUEST F.F
DATA INTERRUPT REQUEST F.F
DATA REGISTER
DATA REGISTER
PARITY BIT GEN.
PARITY BIT F.F
EOP F.F
VCC
R4 3.9K
R6 3.9K
R8 3.9K
R5 3.9K
PIB26 DATA INT
PIB25 COMMON INT
PIB24 EOP INT
PIB27 ALARM INT
ELBIT COMPUTERS LTD
A SUBSIDIARY OF
CONTROL DATA
DETAILED LOGIC DIAGRAM
LINE PRINTER
CODE IDENT C
DWG NO 89639900
REV A
SHEET 2

89637300 B

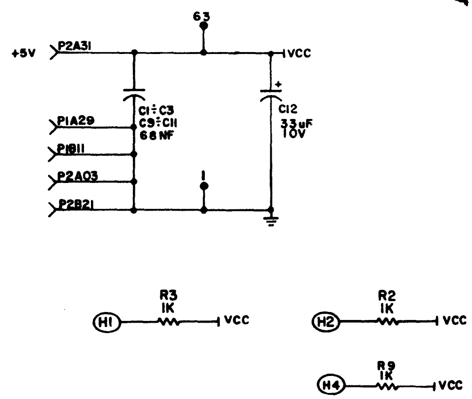
5-19/5-20

ØFF-SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SHEET LØCATION 2	3	4	5
A	D-3	D-4	B-1	D-2
B		D-4	D-1	
D		D-4	C-1	
F	B-3	C-4		
G	B-3	B-4		
J	B-3	B-4		
K	B-3	D-2		
L	B-3	C-2		
M	C-3	C-2		
N	B-3	C-2		
P	B-3	B-2		
R	A-3	B-2		
S		B-1		A-2
T	B-3	A-2		
U	B-3	B-3		
V	C-4			C-3
W	D-4			A-2
X	C-3			B-2
Y	B-1			A-3
Z	B-2	A-3		
AA	A-4			A-2
AB	C-2		B-2	A-3
AC	D-4			B-1
AD	B-2			B-2
AE	A-4			B-1
AF	A-1			B-2
AG	B-4			A-1
AH	A-2			A-2
AJ	A-4			A-1
AK			C-1	B-3
AL	B-4			D-1
AM	C-3		D-2	
AN	A-4			B-2
AP	A-3		B-4	C-2
AR	B-2			B-3
AS	B-2		C-2	
AT	B-1			B-3
AU			B-4	D-2
AV			C-1	B-2
AW			D-2	D-2
AX	A-2		C-3	
AY		D-2	D-4	
AZ		C-4	C-2	
BA	D-2			D-2
BB			C-3	D-1
BC	D-2			D-2
BD	C-2			A-3
BE			B-3	C-1
BF			D-3	C-2

SHEET REVISION STATUS				
1	2	3	4	5
04	04	04	04	04
05	04	04	04	05
06	05	05	05	06
06	06	06	06	06
A	A	A	A	A
B	A	B	B	A

REV	ECO	DESCRIPTION	DRFT	DATE	CHKD	APP
04	CK 984 CK 240	USE ECO'S 984 & 240 TO DRAW REV 04 REDRAWN PER CDC STD.	Jona	OCT.13		
05	CK 435	PAGE 5, PIN P1A12, $\overline{Q00}$ WAS Q00	Dayan	Jan, 21, 74	SHS	
06	CK 576	DRAWING IMPROVEMENTS REVISED PER W.L: SIGNAL NAMES AT P2A25, P2B25 ADDED GND AT TP1 PER ARTWORK AND REF. DESIGN S1 - S5 000 WAS $\overline{Q00}$ (PER W.L) U16 WAS IC 74H11 (ELEMENT INDENTIFIER 213H)	Dayan	March, 19 74		
06	CK 632	SHT 3. C4÷C8 WERE 10µF SHT4. Q07 ÷ Q10 ADDED ECO'S 576 AND 632 REQUIRED TO DRAW LOGIC REV. 06	Dayan	JUNE.74		
A	CK 1121	RELEASED TO CLASS A C3 ADDED TO REF. LTR. V VCC WAS +5V SHT4. U14 WAS U28, U33 WAS 7410	S.D	FEB, 75		
B	CK 1097	POLARITY ERROR IN LOAD IMAGE SIGNAL SH3 B-2: P2B08/U36-1 REPLACES P2A08/U36-1, AND P2A08/U36-3 REPLACES P2B08/U36-3. FITS ASSY 89898200-A				



NOTE:

ALL RESISTORS ARE 0.25 WATT 5 %

AY. 89898200	
AW. 89639800	
DETACHED LISTS	
UNLESS OTHERWISE SPECIFED DIMENSION ARE IN INCHES TOLERANCES 3 PLACE ± 2 PLACE ± ANGLES ±	
DO NOT SCALE DRAWING	
MATERIAL	
FINISH	
ELBIT COMPUTERS LTD A SUBSIDIARY OF CONTROL DATA	FIRST USED ON FF 524-A
DWN	IONA. Z. 31.10.73
CHKD	ZEEV GUSBAND NOV-12/73
ENGR	Avi Tamar NOV 13 73
MFG	
APPR	
QA	
TITLE	DETAILED LOGIC DIAGRAM LINE PRINTER
CODE IDENT	C
DRAWING NO	89639900
SCALE	
NHA:	89639700
SHEET	1 OF 5

This section supplies maintenance references and procedures for the equipment listed in Section 1 of this manual.

TOOLS AND SPECIAL EQUIPMENT

The following tools are recommended for maintenance of this equipment:

PART NUMBER	PART DESCRIPTION	QUANTITY
89688700	Board Extender	1
89670300	Board Extractor	1
	Oscilloscope, Tektronix 453 or Equivalent	1
	Voltmeter	1

The publications listed below are applicable to the equipment:

Title	Publication No.
1784 Computer Customer Engineering Manual	89633300
1784 Computer Reference Manual	89633400
1700 Computer System Codes Manual	60163500
System Maintenance Monitor (SMM17)	60182000

MAINTENANCE

Preventive maintenance of the controller is not required. After it is determined that the controller has failed, remove and replace the PW assembly with an identical problem-free assembly. For removal and replacement of the assembly, refer to Section 3 of this manual. After replacement, a diagnostic check should be run as described in SMM17.

CAUTION

Do not remove or replace cables or PW assembly with the power on.

The following parts list is applicable to the line printer controller:

Name	Part Number
LINE PRINTER Printed Wiring Assembly	89898200
Interrupt Cable Assembly	897247 02
Internal Cable Assembly	89641800
External Cable Assembly, Shielded (FF524-A04 and up)	89818500

WIRE LIST 8

The included wire list is applicable to the FF524-A Line Printer Controller. Wire size, color, origin, destination, and name of the signal normally found on that wire are included in Table 8-1 for the external cable and in Table 8-2 for the internal cable.

A pin list for the line printer controller PWB is also included in this section in Table 8-3.

Table 8-1 External Shielded Cable Wire List

CONNECTOR PIN AT BACK	COLOR	CONNECTOR PIN AT DEVICE	SIGNAL NAME
1	WHT	W	BIT07 +
2	BLK	X	BIT07 -
3			N.A.
4			N.A.
5	RED	x	GND
6			N.A.
7	WHT	d	$\overline{\text{PARITY BIT}}$ +
8	ORN	c	$\overline{\text{PARITY BIT}}$ -
9	WHT	v	$\overline{\text{PARITY ERROR}}$ +
10	YEL	w	$\overline{\text{PARITY ERROR}}$ -
11	WHT	S	BIT05 +
12	GRN	T	BIT05 -
13	WHT	U	BIT06 +
14	BLU	V	BIT06 -
15	WHT	z	$\overline{\text{LOAD IMAGE}}$ -
16	VIO	AA	$\overline{\text{LOAD IMAGE}}$ +
17	BLU	k	$\overline{\text{LINE READY}}$ -
18	BLK	m	$\overline{\text{LINE READY}}$ +
19	WHT	M	BIT03 +
20	BRN	N	BIT03 -
21	BRN	P	BIT04 +
22	BLK	R	BIT04 -
23	RED	h	$\overline{\text{READY}}$ +
24	BRN	j	$\overline{\text{READY}}$ -
25			N.A.
26			N.A.
27	YEL	D	$\overline{\text{CHARACTER REQUEST}}$ +
28	BRN	C	$\overline{\text{CHARACTER REQUEST}}$ -
29	GRN	H	BIT01 +
30	BRN	J	BIT01 -

Table 8-1 External Shielded Cable Wire List (Cont'd)

CONNECTOR PIN AT BACK	COLOR	CONNECTOR PIN AT DEVICE	SIGNAL NAME
31	BLU	K	BIT02 +
32	BRN	L	BIT02 -
33			N.A.
34			N.A.
35			N.A.
36			N.A.
37			N.A.
38			N.A.
39	BRN	a	CONTROL BIT +
40	VIO	b	CONTROL BIT -
41			N.A.
42			N.A.
43	ORN	E	BIT00 +
44	RED	F	BIT00 -
45			N.A.
46			N.A.
47			N.A.
48			N.A.
49	BLU	e	$\overline{\text{BUFFER CLEAR}}$ +
50	RED	f	$\overline{\text{BUFFER CLEAR}}$ -
51			N.A.
52			N.A.
53	YEL	A	$\overline{\text{STROBE}}$ +
54	RED	B	$\overline{\text{STROBE}}$ -
55			N.A.
56			N.A.
57			N.A.
58			N.A.
59	BLK	n	$\overline{\text{M.C.}}$ +
60	ORN	p	$\overline{\text{M.C.}}$ -
66	BARE	---	SHIELD GND

Table 8-2 Internal Cable Wire List

CONNECTOR PIN AT BACKPLANE	COLOR	CONNECTOR PIN AT BACK OF CPU	SIGNAL NAME
1	WHT-BLK	P2A01	BIT 07 +
2	BLK	P2B01	BIT 07 -
3	WHT-BRN	P2A02	N.A.
4	BLK	P2B02	N.A.
5	WHT-RED	P2A03	GND
6	BLK	P2B03	N.A.
7	WHT-ORN	P2A04	$\overline{\text{PARITY BIT}}$ +
8	BLK	P2B04	$\overline{\text{PARITY BIT}}$ -
9	WHT-YEL	P2A05	$\overline{\text{PARITY ERROR}}$ +
10	BLK	P2B05	$\overline{\text{PARITY ERROR}}$ -
11	WHT-GRN	P2A06	BIT 05 +
12	BLK	P2B06	BIT 05 -
13	WHT-BLU	P2A07	BIT 06 +
14	BLK	P2B07	BIT 06 -
15	WHT-VIO	P2A08	$\overline{\text{LOAD IMAGE}}$ -
16	BLK	P2B08	$\overline{\text{LOAD IMAGE}}$ +
17	WHT-GRA	P2A09	$\overline{\text{LINE READY}}$ -
18	BLK	P2B09	$\overline{\text{LINE READY}}$ +
19	WHT-BLK	P2A10	BIT 03 +
20	BRN	P2B10	BIT 03 -
21	WHT-BRN	P2A11	BIT 04 +

Table 8-2 Internal Cable Wire List (Cont'd.)

CONNECTOR PIN AT BACKPLANE	COLOR	CONNECTOR PIN AT BACK OF CPU	SIGNAL NAME
22	BRN	P2B11	BIT 04 -
23	WHT-RED	P2A12	$\overline{\text{READY}}$ +
24	BRN	P2B12	$\overline{\text{READY}}$ -
25	WHT-ORN	P2A13	N.A.
26	BRN	P2B13	N.A.
27	WHT-YEL	P2A14	$\overline{\text{CHARACTER REQUEST}}$ +
28	BRN	P2B14	$\overline{\text{CHARACTER REQUEST}}$ -
29	WHT-GRN	P2A15	BIT 01 +
30	BRN	P2B15	BIT 01 -
31	WHT-BLU	P2A16	BIT 02 +
32	BRN	P2B16	BIT 02 -
33	WHT-VIO	P2A17	N.A.
34	BRN	P2B17	N.A.
35	WHT-GRA	P2A18	N.A.
36	BRN	P2B18	N.A.
37	WHT-BLK	P2A19	N.A.
38	RED	P2B19	N.A.
39	WHT-BRN	P2A20	$\overline{\text{CONTROL BIT}}$ +
40	RED	P2B20	$\overline{\text{CONTROL BIT}}$ -
41	WHT-RED	P2A21	N.A.
42	RED	P2B21	N.A.

Table 8-2 Internal Cable Wire List (Cont'd.)

CONNECTOR PIN AT BACKPLANE	COLOR	CONNECTOR PIN AT BACK OF CPU	SIGNAL NAME
43	WHT-ORN	P2A22	BIT 00 +
44	RED	P2B22	BIT 00 -
45	WHT-YEL	P2A23	N.A.
46	RED	P2B23	N.A.
47	WHT-GRN	P2A24	N.A.
48	RED	P2B24	N.A.
49	WHT-BLU	P2A25	$\overline{\text{BUFFER CLEAR}}$ +
50	RED	P2B25	$\overline{\text{BUFFER CLEAR}}$ -
51	WHT-VIO	P2A26	N.A.
52	RED	P2B26	N.A.
53	WHT-GRA	P2A27	$\overline{\text{STROBE}}$ +
54	RED	P2B27	$\overline{\text{STROBE}}$ -
55	WHT-BLK	P2A28	N.A.
56	ORN	P2B28	N.A.
57	WHT-BRN	P2A29	N.A.
58	ORN	P2B29	N.A.
59	WHT-RED	P2A30	$\overline{\text{MC}}$ +
60	ORN	P2B30	$\overline{\text{MC}}$ -

Table 8-3. PWB Pin List

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P1A1	$\overline{A05}$	P1B1	$\overline{A01}$
2	$\overline{A06}$	2	$\overline{A02}$
3	$\overline{A00}$	3	$\overline{A07}$
4		4	$\overline{A08}$
5		5	
6	$\overline{A03}$	6	
7	$\overline{A04}$	7	
8		8	
9		9	
10		10	
11		11	GND
12	Q00	12	
13		13	
14		14	
15		15	Q07
16	Q08	16	Q09
17	Q10	17	
18		18	
19		19	
20	$\overline{W=0}$	20	
21	$\overline{READ}$	21	$\overline{WRITE}$
22	$\overline{REPLY}$	22	$\overline{REJECT}$
23	$\overline{PROTECT}$	23	
24		24	$\overline{EOP\ INT}$
25		25	$\overline{COMMON\ INT}$
26		26	$\overline{DATA\ INT}$
27		27	$\overline{ALARM\ INT}$
28		28	
29	GND	29	
30		30	
P1A31		P1B31	

Table 8-3. PWB Pin List (Continued)

CONNECTOR/PIN	SIGNAL NAME	CONNECTOR/PIN	SIGNAL NAME
P2A1	BIT 07	P2B1	$\overline{\text{BIT 07}}$
2	$\overline{\text{CHARACTER REQUEST}}$	2	CHARACTER REQUEST
3	GND	3	
4	PARITY BIT	4	$\overline{\text{PARITY BIT}}$
5		5	
6	BIT 05	6	$\overline{\text{BIT 05}}$
7	BIT 06	7	$\overline{\text{BIT 06}}$
8		8	
9	$\overline{\text{LINE READY}}$	9	LINE READY
10	BIT 03	10	$\overline{\text{BIT 03}}$
11	BIT 04	11	$\overline{\text{BIT 04}}$
12	$\overline{\text{READY}}$	12	READY
13		13	
14		14	
15	BIT 01	15	$\overline{\text{BIT 01}}$
16	BIT 02	16	$\overline{\text{BIT 02}}$
17		17	
18		18	
19		19	
20	CONTROL BIT	20	$\overline{\text{CONTROL BIT}}$
21		21	GND
22	BIT 00	22	$\overline{\text{BIT 00}}$
23		23	
24		24	
25	BUFFER CLEAR	25	$\overline{\text{BUFFER CLEAR}}$
26		26	
27	STROBE	27	$\overline{\text{STROBE}}$
28		28	
29	STPCK	29	$\overline{\text{EXCK}}$
30	MC	30	$\overline{\text{MC}}$
P2A31	VCC	P2B31	

COMMENT SHEET

MANUAL TITLE Control Data® FF524-A Line Printer Controller

Hardware Maintenance Manual

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