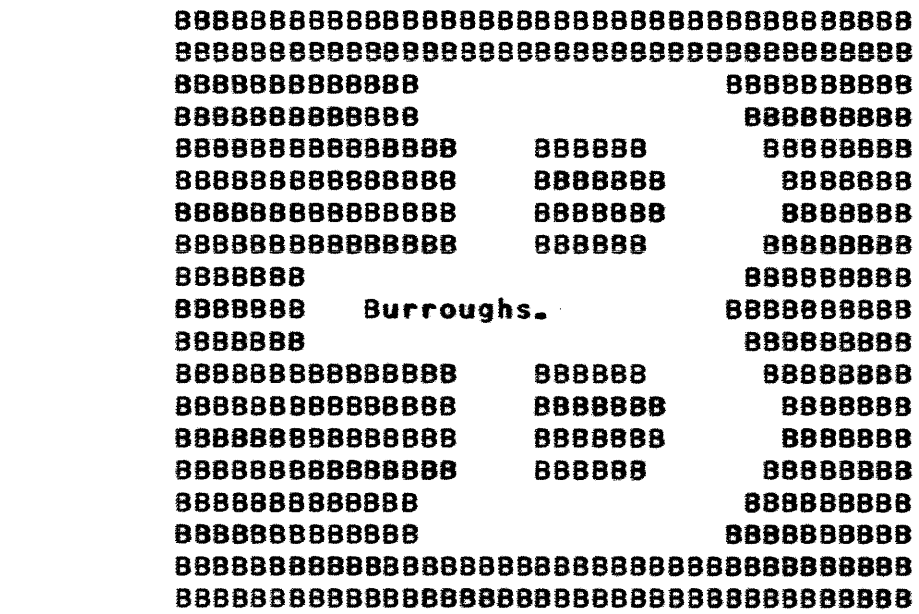
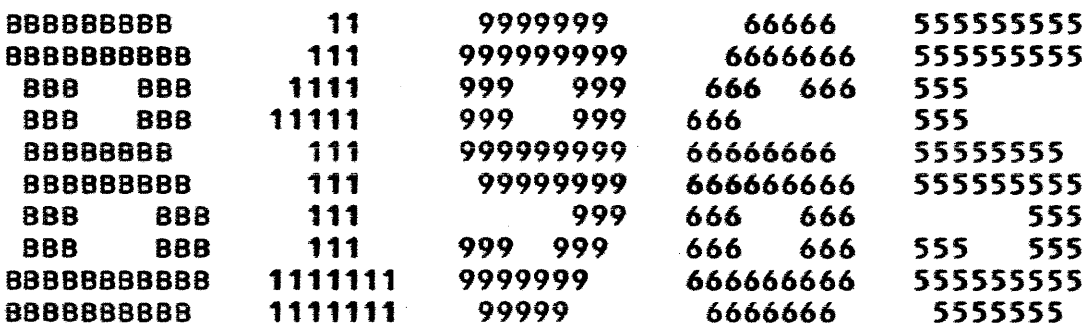
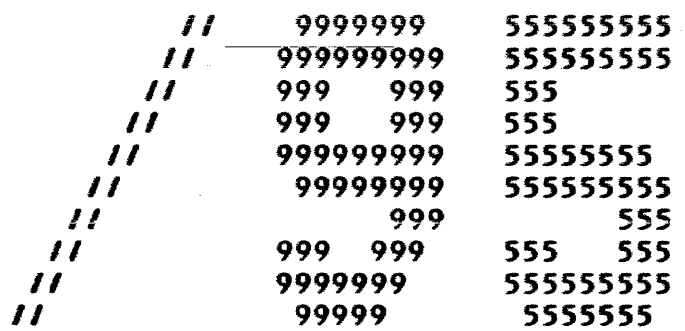
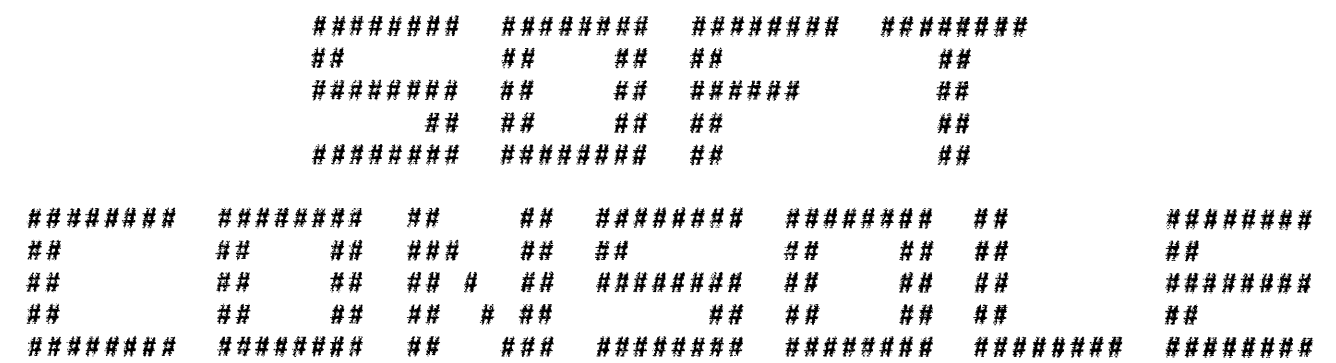

Burroughs.





05/03/85



B1965/1995 SOFT CONSOLE MODEL II OPERATION

SOFT CONSOLE OPERATION

INTRODUCTION

This section of the SYSTEMS MAINTENANCE GUIDE describes the functions, features, and operational procedures associated with the SOFT CONSOLE and MAINTENANCE PROCESSOR of the B1965/B1995 systems.

CONTENTS

MAINTENANCE SUBSYSTEM POWER UP ACTIVITY

When power is turned on, the following actions take place. The actions are not necessarily listed in chronological order:

- the micro-processor on the Maintenance Card (H10) is reset.
- a self-test of the Maintenance Card is run and if an error is encountered, a display message is attempted. (Note: Particular positions of a switch on the Maintenance Card can be used to inhibit the normal CRT display and to indicate error type via on-card indicators.) Depending upon the type of error, the micro-processor may halt or may attempt to complete the execution of the self-test and enter the operator input-display mode of operation.
- Processor waits for a disk present, loads the bootstrap and executes it.
- appropriate registers in the MASTER and SLAVE processors are cleared. For example, CACHE VALIDITY bits, A-register, PERM-register, PERP-register.
- Processor A is set to MASTER.
- Processor B is set to SLAVE.
- the SLAVE processor is set ON-LINE.
- the SLAVE processor is set to NORMAL mode.
- the MASTER processor is set to NORMAL mode.
- both processors are set to HALT mode.
- entire memory is initialized with "0" data and correct ECC.
- an initial screen display is transmitted to the terminal and displayed on page 1. (MCP messages will be directed to page 2. Toggling between pages is accomplished via the CTRL and right or left pointing arrow keys or by program control).

Before operated a floppy disk must be inserted in disk drive.

If the terminal is in LOCAL when the maintenance control attempts to transmit, the maintenance control will retry up to ten times. Each attempt will cause an alarm to sound if the terminal has the alarm option enabled. If the operator switches to RECEIVE mode, the message will be displayed. If the terminal is in TRANSMIT mode, the input message will be accepted and then the output message displayed.

SCREEN DISPLAY - MENU SECTION

The screen display consists of a MENU SECTION followed by a DATA SECTION. Formats for the DATA SECTION are shown in Figures 1 thru 9, beginning on page 18. The format of the MENU SECTION is as follows:

```
COMMAND >                                                    <
 Mode. .Switches. .Display ..Reads.. .....Writes..... ......Actions.....
NORMAL MASTER: A  REG S16  SRnn:addr SWnn:addr=values CLEAR RESET UNLOAD
SONLY   SLAVE:OFF STK S24  CR:addr    CW:addr=values  MTR CLRELOG NOTEXT
CONLY  REMOTE:OFF CK  S39  BACK or -  register=data   CCLR  STEP  RUN GO
DISK   SINGLE:OFF CSE MAC  NEXT or +  ALLREGS=data    RC   SCREEN HTEST
FROZEN INTRPT:OFF OPR DIR  RDTEXT     TEXT characters LOAD AUTO [ON,OFF]
DISK: pack-name /file-name   SLAVE:ABSENT     MASTER:HALTED     ERROR
```

The COMMAND line is followed by a set of reserved words which may be entered on the COMMAND line to effect a MODE change, a SWITCH change, a DISPLAY change, a REGISTER-MEMORY READ-WRITE or an ACTION. The last line of the menu indicates SYSTEM STATUS as follows:

- o DISK: File-name indicates the reference file which is associated by default in a MAC to HOST xfer This name is used by default in the MTR, LOAD & AUTO command.
- o SLAVE: Status can be ABSENT or OFFLINE or HALTED or RUNNING.
- o MASTER: Status can be HALTED or RUNNING.
- o ERROR: Indicated if any bit of the master processor's PERP or PERM registers was true when the processor halted or if any ERROR condition arose during the last interaction of the processor with the maintenance control or whenever the MASTER processor is RUNNING despite having received a HALT request.

The MODE of the master processor, STATES of the SWITCHES, the SCREEN being displayed and the status on the STATUS line are highlighted.

Except for the COMMAND line, the entire screen is write protected, i.e., cannot be changed from the keyboard.

Entries on the COMMAND line are free format, i.e., any number of spaces may be added between commands or elements of commands. At least one space is required between commands.

Space(s) also may be used in lieu of ":", "=" and "/" in the READ and WRITE commands even though those symbols are shown in the menu.

Abbreviations are permitted as long as the abbreviation is unique. Exceptions are: HT for HTEST and CLRE for CLRELOG. Also, alternate forms, not shown on the menu, may be used. These forms are:

NORMAL FORM	ALTERNATE FORM	
CLEAR or CLE	CLR	
RUN or GO	START	
GO (letter O)	GO (number 0)	
CK	CACHE	
SWnn	SnnW	
SRnn	SnnR	
SnA	SOnA	
SnB	SOnB	(n = 0 through 9)

In case of spelling, syntactical or procedural errors, an appropriate error message will be displayed and THE CURSOR WILL BE LEFT AT THE START OF THE WORD IN ERROR.

When the COMMAND line is transmitted, it is left unchanged except as noted below for memory WRITES. Transmission is from home to cursor or if cursor is at home, from home to end of the COMMAND line.

Entries on the COMMAND line are executed from left to right. The execution of RUN (except when SINGLE micro toggle is ON) or MASTER (change of master status) will cause subsequent commands, if any, to be ignored.

If commands cannot be executed for some reason, a "CONTROL" error message will be displayed on the COMMAND line.

ACTION COMMANDS

The SCREEN command or the SPCFY key will cause a redisplay of the most recently displayed screen. This command is useful to restore a screen which had been altered or cleared by the operator.

The CLEAR command will clear the master processor. It will cause the slave processor to CLEAR only if online or to RESET if offline (See RESET below). CLEAR will cause a running slave processor to halt. CLEAR will clear the following registers : PERP, PERM, MSSW, CC, CD, INCN, A, BR, "M", ELOG and also the CACHE if mode is not CONLY.

The CCLR command will cause all VALIDITY bits in the CACHE Memory of the master processor to be cleared.

The RESET command will cause a CLRB signal to be issued to the master processor (also slave), to memory and to the I/O. RESET will clear the following registers : PERP, PERM, MSSW, CC, CD and INCN. CLRB will also cause a running slave processor to halt.

The CLRELOG command will cause the ELOG in the memory subsystem to be cleared.

The UNLOAD command will cause the head of the disk drive to be restored, the file pointer to be repositionned on the first logical record of the MTR file and will cause subsequent commands, if dependent upon the completion of the unload, to be delayed until the restore is completed (e.g., RUN in DISK mode).

The DIR command reads the directory of the floppy disk and displays the first 60 file names & creation dates on the ODT.

The LOAD "<file-name>" command sets DISK mode, searches the directory for the file-name and, if found, reads the first record of the file (this file-name will be reflected on line 8 of the screen display). LOAD will not cause RUN to be executed automatically.

The MTR "<file-name>" will cause the directory to be reloaded in memory, CLEAR the system, and proceed with a LOAD "<file name>" command as described above.

The AUTO "<file-name>" ON/OFF writes the file-name specified in the command at a specific location on the diskette (if the file-name was omitted, the default name found in line 8 of the screen display will be used). Along with this file name, the status of the ON/OFF variant of the command, the current ON/OFF status of the slave processor (if any), and the status of the remote ODT line (i.e. ON/OFF, SYNC/ASYNC, Baud rate if ASYNC) will be written on the diskette.

No other commands are allowed to interfere between the AUTO command keywords described by the above syntax. After each POWER-ON/CARD-RESET, the system configuration will be restored as memorized above, and, if the ON variant was specified, the MTR "<file-name>" GO commands will be executed without operator intervention. The non-standard automatic start conditions will be displayed on the ODT screen using the DIR command.

The RC command will cause the RC signal to be sent on the I/O bus.

The HTEST command will cause the micro-processor on the maintenance card to run a self diagnostic test and then display the H10 MAINTENANCE PROCESSOR SELF TEST SUMMARY (assuming switches on H10 card are set in the position for display). After completion of the self test, the AUTO configuration (if any) will be restored, but the execution of the selected MTR file will not be started, even though the AUTO ON option had been specified by the operator.

The TEXT command will cause all <characters> (including all blanks) to the right of the word TEXT and to the left of the cursor or if the cursor is at home postion, to the end of the command line to be written into decending S-Memory locations starting at the end of the previous <character> string, if any; otherwise, starting at one byte location from MAXS. A binary value (0 to 255) indicating the number of characters in the total string is stored at the byte location immediately prior to SMAX. If the total number of text characters would cause an overflow of the 255 byte count, the final line is not written and an error message is displayed. Execution of a NOTEXT command or power up will cause the byte count to be initialized to "0". The <characters> are stored in ASCII. The intent of this command is to allow flexibility in the manner in which cold start variables are loaded. Interpretation of the TEXT <characters> is a software function. A display of the TEXT <characters> on the CSE display may be obtained by a RDTEXT command. A CSE command will cause the TEXT <characters> to be removed from the display.

The RUN (or GO,or START) command will start only the master processor if the master is in DISK or FROZEN modes or if the slave is OFFLINE. If the master processor programmatically changes from DISK mode and continues to run, the MTR indicator on the cabinet will be extinquished. The RUN command, except when executed with SINGLE micro on, will clear the PERM and PERP registers and bit #3 of the CD register.

The STEP command is equivalent to executing the RUN command with SINGLE micro ON. STEP will step both processors if the slave is on-line. The STEP command is invalid and will cause an error message response if attempted when the processor is in DISK mode.

Whenever two processors are started as a result of either RUN or STEP, the order in which they start is random.

MODE COMMANDS

NORMAL is a mode, which if on when RUN is executed, causes the processor to obtain its string of M-instructions in a normal manner, i.e. from Cache. Instructions not in Cache are automatically loaded to Cache from S-Memory.

CONLY is a mode, which if on when RUN is executed, causes the processor to obtain its string of M-instructions from Cache only. Instructions not in Cache will cause a halt.

SONLY is a mode, which if on when RUN is executed, causes the processor to obtain its string of M-instructions from S-Memory only.

DISK is a mode, which if on when RUN is executed, causes floppy data to be transferred to the master processor. Floppy data may be M-instructions or M-instructions followed by a data field.

FROZEN is a mode, which if on when RUN or STEP is executed, causes the master processor to retain the micro-instruction contained in the M register after execution of the command. For RUN with SINGLE micro OFF, the micro-instruction is executed repeatedly until halted via the Halt switch on the cabinet. For STEP or for RUN with SINGLE micro ON, the micro-instruction is executed once. The A register is incremented for each execution.

SWITCHES

MASTER is a toggle which causes a switch of master status between processors. When master status is switched, the MODE of the slave is forced to NORMAL. The INTRPT, the SINGLE micro and the SLAVE on-off toggles are not changed.

SLAVE is a toggle which causes the slave processor to change its ON-LINE/OFF-LINE status.

INTRPT is a toggle which, when ON, causes BIT 0 in the CC register of a running processor to be set each clock time. INTRPT OFF does not affect BIT 0 in any manner. The state of the INTRPT switch is not changed if master status is changed.

SINGLE micro is a toggle which, if ON when RUN or STEP is executed, causes the master processor and the slave, if on, to execute one micro-instruction, then halt and then automatically update the last version of the screen display. The state of the SINGLE micro switch is not changed if master status is changed. SINGLE micro ON and DISK mode are mutually exclusive and will result in an error message response if both are true when a RUN or STEP is attempted.

SPECIAL REGISTERS

A write to the CMND register will cause the write data and a CA signal to be transmitted on the I/O bus. Displayed in the CMND register will be the data last transmitted.

A write to the DATA register will cause the write data and a RC signal to be transmitted on the I/O bus. Displayed in the DATA register will be the data on the I/O bus being received from the I/O, not the write data sent by the processor. Note: The DATA register will always reflect data on the I/O bus that is currently being received from the I/O. It will be updated after each action by the processor.

CNS is cleared by power up. It is not cleared by switching master status or by CLEAR.

Operator changes in MSSW will not cause a change in MODE. MODE changes by the operator must be effected by a MODE change entry on the command line. The current MODE being displayed will be forced into the MSSW register prior to execution of RUN or STEP. Similarly, the value in MSSW will cause the appropriate MODE to be displayed when the processor changes from a RUN to a HALT state. MSSW is set appropriately (0000 for master and 1000 for slave) by power up, CLEAR, or by a change in master status.

SCREEN DISPLAYS

OPR will cause a display of the operator information registers and some system operating instructions (see Figure 1).

STK will cause a display of all 32 locations of the A-Stack as well as TAS (see Figure 2).

REG will cause a display of the processor's registers, psuedo-registers and scratchpad-registers (see Figure 2).

CSE will cause a display of the ELOG and a selected set of registers that are particularly important to the system's operation (see Figure 3).

A RDTEXT operation will also cause a display of the CSE page. But, in addition to the display of the CSE set of registers, it will cause a display of up to 255 text <characters> from memory.

MAC will cause a display of the micro-processor's input/output ports and key variables of the firmware (see Figure 5).

S16, S24 and S39 will cause a display of S-Memory while CK will cause a display of Cache Memory (see Figures 7, 8, and 9). The memory locations displayed will be those locations that were most recently displayed for the particular screen requested. Power up or halt will cause a default starting location of zero.

The HTEST command will cause a display of the H10 MAINTENANCE PROCESSOR SELF TEST ERROR SUMMARY display. This display is also attempted at power up time if an error occurs (see Figure 4).

The DIR command will cause a display of the floppy disk directory.

READS AND WRITES

The S-Memory (SRnn) and Cache Memory (CR) read commands cause a screen display of the appropriate memory page starting with the location specified by <addr>. If the S-memory subsystem indicates an error, ERROR will be displayed on the status line as a result of PERM being nonzero. For SR16 and SR24 reads, the location of the last logged S-Memory error may be obtained by switching to the CSE page which displays the ELOG. For SR39 reads, the micro-processor will clear PERM and ELOG prior to reading each memory word and display its value along with each word after the individual word is read. Cache Memory errors are not indicated but the key parity and the micro-instruction parity bits are included in the cache display.

The NEXT and BACK (or + and -) commands are applicable only when on a CACHE or S-MEMORY page. On a memory page they cause scrolling forward or backwards by one page. Wraparound is permitted in either direction. On a non-memory page they cause no action other than a display of an error message.

A READ or WRITE to Cache or to S-Memory will not cause the A-register or FA-register or any other register to be changed. Registers, except for those carrying specific control or status information can be changed only by designating them as a destination. Note however, that the A register counts during RUN and STEP.

An automatic screen update will occur on a Cache page if a Cache Write is executed, or, on an S-Memory page if an S-Memory Write is executed. Also an automatic screen update of the currently displayed page will occur if it is possible that the page could have been changed by any type of register write, memory write or command execution.

<addr> may be one or more hex digits. If less than six digits are entered, <addr> will be right justified and zeros assumed on the left. If greater than six digits, an error message will be displayed if any of the leading digits to the left of the first six are non-zero. <addr> is interpreted as a bit address. For CACHE (CR & CW) and for S-Memory (SR16, SW16, SR39 and SW39) accesses, an appropriate number of rightmost bits of <addr> are ignored and zeros assumed. The ":" preceeding <addr> is optional.

<value> may be one or more hex digits. <value> will be right justified and either zero filled or truncated on the left as required. Truncation of non-zero digits will be reported as an error. The "=" preceeding <value> is optional. Formats for <value> depend upon the page being written:

S39:	xx xxxx xxxx or xx/xxxx/xxxx	SW39 FF0 EC DATA DATA
S16:	xxxx	SW16 F20 DATA (16)
S24:	xxxxxx	SR24 121
CK:	xxxx	CK FF0 (cache read)

The EC displayed in the S39 page contains a parity bit in the lower ordered bit position. This bit is generated by the memory control on the data read from memory. When writing, this bit of the EC is ignored.

In the CK display, a micro-instruction parity bit (contained in the fifth digit from the right) preceeds the micro-instruction. When writing, this bit is generated by the maintenance control. Also when writing into cache, the hit bit, the validity bit and the key parity bit are generated by the processor. The key is taken from <addr>.

A S-memory or Cache write command can have a multiple number of values associated with the write. The values are separated by commas and are written into memory starting with the given <addr> and proceeding to higher addressed locations. If a comma is the last entry on the command line, a new memory write command is prompted on the command line starting in the leftmost position. The <addr> will be six digits long and will point to the memory location next to be written. The cursor will be left in the position immediately to the right of the = in the prompted command. If a comma does not follow the last value, the command line will not change. Note that a prompted Write command will overwrite any characters on the command line in the first 10 to 12 positions. It will not affect the rest of the line.

The RDTEXT operation forces the CSE page and displays the TEXT <characters>, if any, contained in memory.

CNS REGISTER

This register is used by the processor as a source or a destination. When used as a destination, hex values may be passed to the maintenance control to effect an action as noted below. Responses to the requests are returned in CNS immediately or after completion of the requested action as indicated below.

REQUEST	CNS VALUE	CNS RESPONSE	ACTION
Enable Commands	000081	000081	Subsequent values of 000001-000006 and 000040-000042 moved to CNS will be interpreted as commands. Commands 000040-000042 are valid for master only.
Enable U Parity	000082	000082	Subsequent reads of floppy data will have a parity bit included, suitable for writing to cache.
Disable Commands	000083	000083	CNS command interpretation is disabled. Also disabled are any pending deferred responses. Disabled is the normal or default state.
Disable U Parity	000084	000084	Floppy data transferred to the processor will not include a parity. This is the normal or default state.
Set "keep-page"	000085	000085	This command sets the "keep-page" toggle. If this toggle is true when the processor halts, a message will be displayed on the 25th line of the ODT, indicating that the status information is available on page 1. The keep-page toggle is set false each time the processor is started.
Set Interrupt	000001	000000	Set interrupt toggle ON. Effective only for processor performing the move to CNS.

(continued next page)

REQUEST	CNS VALUE	CNS RESPONSE	ACTION
Get Status	000002		Return a status vector (see below).
Halt Slave	000003	000000	Set slave's halt request.
Halt Processors	000004	000000	Set both master's & slave's halt request.
Reset Interrupt	000005	000000	Reset interrupt toggle. Effective only for the processor performing the move to CNS.
Get Baud Rate	000006	Baud Rate	Returns the presently set Remote Link Async baud rate. (see notes below)
Reload Disk	000021	lluu00	Read FAT(file allocation table) and 9 sectors of directory ll = lower byte of buffer address uu = upper byte
Specify file name			
byte 1 & 2	aabb22	------	update first and second bytes of MTR file name. aa = first byte,bb = second
byte 3 & 4	ccdd23	------	update third and fourth bytes of MTR file name. cc = third byte,dd = fourth
byte 5 & 6	eeff24	------	update fifth and sixth bytes of MTR file name. ee = fifth byte,ff = sixth
byte 7 - 8 and search	gghh25	lluuss	update seventh and eighth bytes of MTR file name and search for file name pattern gg = seventh bytes,hh = eighth ll = lower byte of buffer address uu = upper byte,ss = search status

(continued next page)

REQUEST	CNS VALUE	CNS RESPONSE	ACTION
Read Diskette	ldud26	lluurs	read disk. ld = lower disk address, ud = upper address,rs = read status.
Write Diskette	ldud27	lluuws	write disk.ld,ud = same read. ws = write status.
Read Ram Data	lluu11	d1d2d3	Read RAM. ll = lower address, uu = upper address, d1,d2,d3 = first,second,thirth data.
Write Ram Address	lluu12	------	Write ram address
data	d1d213	lnun--	write data on ram d1 = lower byte data d2 = upper byte data,ln = lower byte of next address,un = upper byte.
Halt Restart	000040	000040	Master is re-started after a halt. CNS is set to 000000.
MTR Restart	000041	000041	A CLEAR, set DISK mode, UNLOAD and RUN (restart) is executed after the processor halts.
ALLREGS Restart	000042	000042	All processor's registers (including STK) are set to tthe value of the X register, except CNS, which is set to 000000. Action is after processor halts.
Invalid	others		Treated as Disable commands, Disable U parity, and Reset keep-page. Any pending deferred command is lost.

Commands 000001-000042 are recognized only if an Enable Command (000081) has been executed.

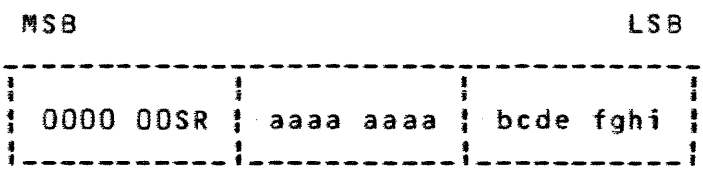
Commands 000081 to 000085 are completely independent.

Commands 000040-000042 are valid only for master processor. They are ignored by a slave.

Only one CNS command can be retained; therefore the deferred action of only the last received command will be done. This is especially important in using the restart commands (000040-000042).

The Baud Rate returned is not defined if link is set for Synchronous operation. The format of the Baud Rate is BCD. Presently allowable baud rates are 300, 1200 and 1800.

STATUS VECTOR (24 bits):



a. Firmware level number
b. Slave online (not valid in single processor system)
c. Not running
d. Not A-processor
e. Halt requested
f. Other processor halted (not valid for single processor
g. Not DISK mode
h. A-processor is master
i. B-processor is absent (valid for A-processor only)

R. Remote Switch ON.
S. Remote Link is synchronous (not valid when R=0).

OPR DISPLAY

B1900 (****) PROCESSOR SYSTEM

TO INITIATE OPERATING SYSTEM :
1) Set system disk drive labeled DPA to RUN.
2) Type MTR GO on COMMAND line and push XMT.

TO TOGGLE STATE OF SWITCH :Type name of switch and push XMT.
TO CHANGE DISPLAY PAGE :Type name of page and push XMT.

OPERATOR INFORMATION REGISTERS:

T = xxxxxx	X =	PERM =	A =
L =	Y =	PERP = 1	LR =

CPU CONDITION : DISKETTE ERROR

(****) = SINGLE or DUAL

FIGURE 1 - DISPLAY FORMAT -- OPR

REGISTER DISPLAY

```
TA=.....x     FU=.....x     X=xxxxxx  SUM=        S0A=        S0B=
TB=           FT=           Y=        CMPX=       S1A=        S1B=
TC=          FLC=           T=        CMPY=       S2A=        S2B=
TD=          FLD=           L=        XANY=       S3A=        S3B=
TE=          FLE=           A=        XEOY=       S4A=        S4B=
TF=          FLF=         "M"=.xxxxx  MSKX=       S5A=        S5B=
CA=         BICN=          BR=        MSKY=       S6A=        S6B=
CB=         FLCN=          LR=        XORY=       S7A=        S7B=
LA=         NULL=          FA=        DIFF=       S8A=        S8B=
LB=         RSVD=          FB=        MAXS=       S9A=        S9B=
LC=         PERM=          FL=        NULL=      S10A=       S10B=
LD=         PERP=         TAS=         "U"=..xxxx S11A=       S11B=
LE=         XYCN=          CP=....xx  NULL=       S12A=       S12B=
LF=         XYST=        NULL=        DATA=       S13A=       S13B=
CC=         INCN=         CNS=        CMND=       S14A=       S14B=
CD=         MSSW=        TIME=        NULL=       S15A=       S15B=
```

STK DISPLAY

```
TAS= xxxxxx          STACK 00=xxxxxx          STACK 10=
                     STACK 01=                STACK 11=
                        .                        .
                        .                        .
                        .                        .
                     STACK 0F=                STACK 1F=
```

FIGURE 2 - DISPLAY FORMATS -- REG and STK

CSE DISPLAY (with TEXT)

```
X = xxxxxx      PERP = .....x      LR = xxxxxx      "M" = .xxxxx

Y = PERM = BR = A =

T = CC = FA = TAS =

L = CD = FB = INCN = .....x

ELOG = xxxxxx CNS = xxxxxx

TEXT IS nn BYTES ----------------
```

("nn" bytes of S-Memory starting with the byte at SMAX-8 and proceeding to lower numbered locations. "nn" is 0 to 255.)

FIGURE 3 - DISPLAY FORMAT --CSE

HTEST DISPLAY

```
H10 MAINTENANCE PROCESSOR SELF TEST ERROR SUMMARY

                    PROCESSOR  A

-----     -------          ------------
  1      *ROM              xxxxxxxx
  2      *RAM
  3      *CLOCK
  4       MPPI
  5       USART
  6       DISK
  7       LOGIC A
  8       LOGIC B
  9       LOGIC C
  A      *CPU CLEAR
  B       MEX ECHO         xxxxxx xxxxxx xxxxxx
  C       IO ECHO          xxxxxx xxxxxx xxxxxx
  D       INTERRUPT

 * FAILURES IN THESE TEST MAY INVALIDATE SUCCEEDING RESULTS

 press SPCFY (or xmit SCREEN) for state display
```

FIGURE 4 - DISPLAY FORMAT -- HTEST

MAC DISPLAY

```
 H CARD MEX OPERATION              CPU CONTROL (FOR H CARD)
--------------------------      ---------------------------------

Driver port     =   xxxxxx       During last MAC micro (xxxx)
  Enabled :  YES                 Expected :  WRITE TO MAC (CNS<=MEX)
  (inverted)                     Observed :  WRITE TO MAC (CNS<=MEX)
Receiver port   =   xxxxxx
  Selected:   NO                 Current  :   READ "U" (MEX<=U -FETCH
                                                        MAC IF HALTED)

      Saved CPU Registers : "M" = xxxxxx "A1" = xxxxxx "CNS" = xxxxxx

 RS232 Information                  DISKETTE INFORMATION
--------------------------      ---------------------------------

Last Attempt : SELECT            Disk status : NO ERROR
Baud Rate    : 1200              Record Count: xx
Status       : NO ERROR          Micro Count : xx
```

Figure 5 - DISPLAY FORMAT -- MAC

RUN DISPLAY

```
COMMAND >                                        <
 Mode.  .Switches.
NORMAL MASTER: A
SONLY   SLAVE:OFF
CONLY  REMOTE:OFF          RUNNING  <f i l e - n a m e>
DISK   SINGLE:OFF
FROZEN INTRPT:OFF
  DISPLAY OF CPU STATE AT TIME OF LAST START (NOT UPDATED DURING RUN)
```

FIGURE 6 - DISPLAY FORMAT -- RUN

S24 DISPLAY

Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
000000=	xxxxxx	000120=		000240=		000360=		000480=	
000018=		000138=		000258=		000378=		000498=	
000030=		000150=		000270=		000390=		0004B0=	
000048=		000168=		000288=		0003A8=		0004C8=	
000060=		000180=		0002A0=		0003C0=		0004C8=	
000078=		000198=		0002B8=		0003D8=		0004E0=	
000090=		0001B0=		0002D0=		0003F0=		000510=	
0000AB=		0001C8=		0002E8=		000408=		000528=	
0000C0=		0001E0=		000300=		000420=		000540=	
0000D8=		0001F8=		000318=		000438=		000558=	
0000F0=		000210=		000330=		000450=		000570=	
000108=		000228=		000348=		000468=		000588=	

S16 DISPLAY

Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
000000=	..xxxx	0000C0=		000180=		000240=		000300=	
000010=		0000D0=		000190=		000250=		000310=	
000020		0000E0=		0001A0=		000260=		000320=	
000030		0000F0=		000180=		000270=		000330=	
000040		000100=		0001C0=		000280=		000340=	
000050		000110=		0001D0=		000290=		000350=	
000060		000120=		0001E0=		0002A0=		000360=	
000060		000130=		0001F0=		0002B0=		000370=	
000080		000140=		000200=		0002C0=		000380=	
000090		000150=		000210=		0002D0=		000390=	
0000A0		000160=		000220=		0002E0=		0003A0=	
0000B0		000170=		000230=		0002F0=		0003B0=	

FIGURE 7 - DISPLAY FORMATS -- S24 and S16

S39 DISPLAY

```
Address   EC Data EC Data PERM/ELOG  Address   EC Data EC Data PERM/ELOG

000000 = xx xxxx xx xxxx x  xxxxxx   000180 =
000020 =                             0001A0 =
000040 =                             0001C0 =
000060 =                             0001E0 =

000080 =                             000200 =
0000A0 =                             000220 =
0000C0 =                             000240 =
0000E0 =                             000260 =

000100 =                             000280 =
000120 =                             0002A0 =
000140 =                             0002C0 =
000160 =                             0002E0 =
```

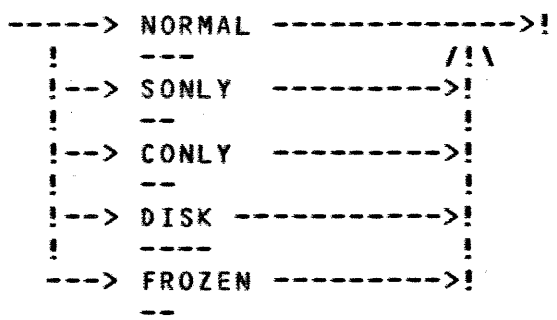
FIGURE 8 - DISPLAY FORMAT -- S39

CK DISPLAY

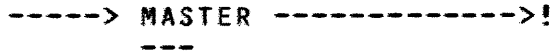
```
Addr   Key P H V Cache  Addr   Key P H V Cache  Addr   Key P H V Cache
000000  xx x x x .xxxxx 0000C0  xx x x x .xxxxx 000180  xx x x x .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx

000040  xx x x x .xxxxx 000100  xx x x x .xxxxx 0001C0  xx x x x .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx

000080  xx x x x .xxxxx 000140  xx x x x .xxxxx 000200  xx x x x .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx
                .xxxxx                 .xxxxx                 .xxxxx
```

FIGURE 9 - DISPLAY FORMAT -- CK

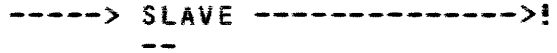
COMMAND LINE SYNTAX



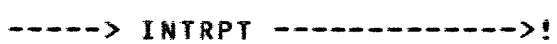
Determines the source of the master processor micro-instructions when RUN or STEP is commanded.



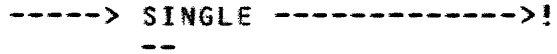
Toggles master processor between processor A and processor B, forces new slave to normal mode and switches control of the display to the new master.



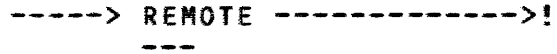
Toggles slave processor ON and OFF.



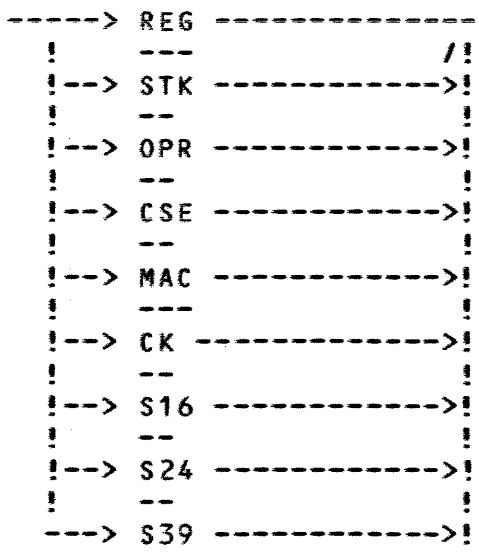
Toggles interrupt ON and OFF. ON causes bit #0 in cc-register of each processor to be set each clock time during RUN or STEP. OFF causes no action.



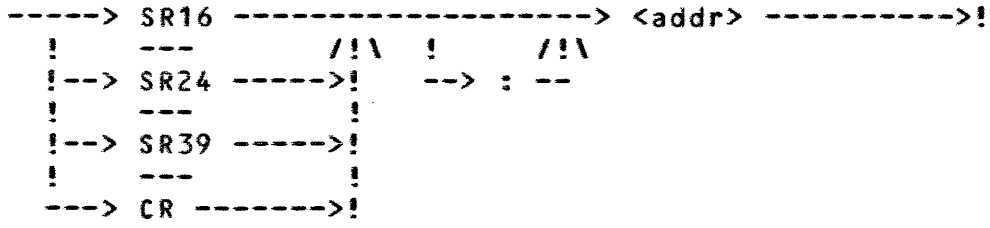
Toggles SINGLE micro ON and OFF. ON causes execution of one micro-instruction when RUN is commanded.



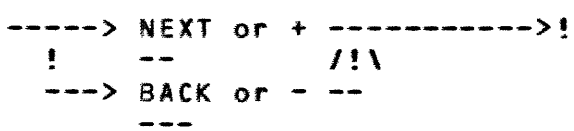
Toggles REMOTE link switch ON and OFF. ON causes the remote diagnostic link to be activated.



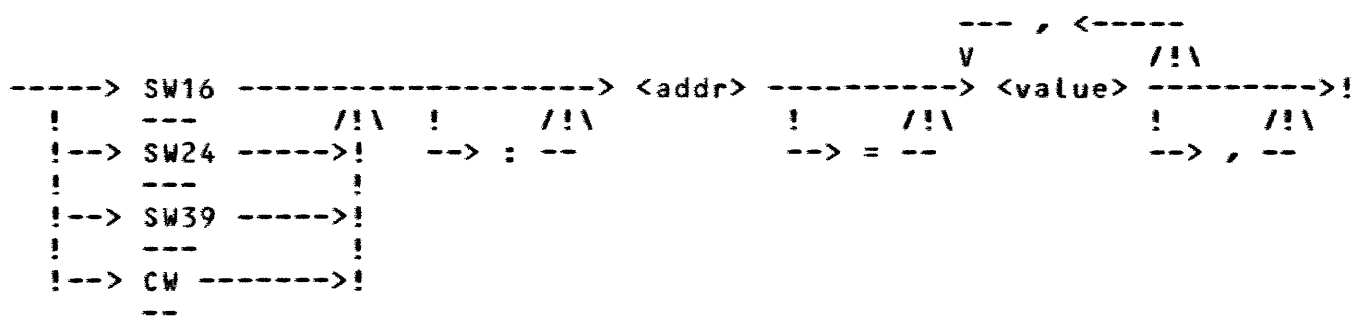
Displays registers, stack, selected registers, maintenance control information, Cache-Memory or S-Memory.



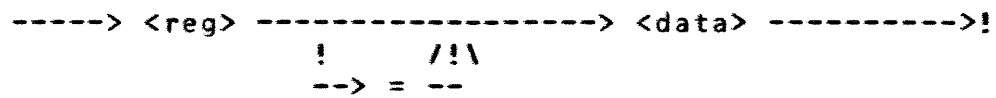
Displays S-Memory or Cache starting at the specified <addr>.



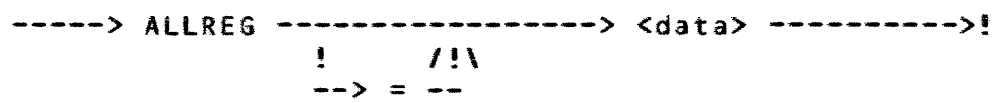
Scrolls forwards/backwards by one page. Valid only on memory page.



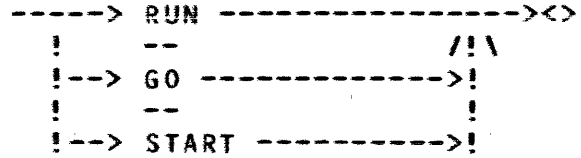
Writes <value> string into corresponding consecutive memory location starting with location <addr>. Commas separate more than one <value>. If a comma is the last entry on the command line, a new <addr> pointing to the memory location next to be written is prompted. <value> may be one to six hex digits preceeded by any number of leading zeros. Usual formats are CW: XXXX, S16: XXXX, S24: XXXXXX, S39: XX XXXX XXXX or XX/XXXX/XXXX.



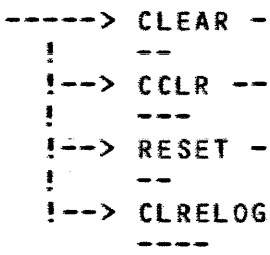
Writes <data> into specified register. <data> is one to six hex digits preceeded by any number of leading zeros.



Writes <data> into a predetermined set of processor's registers. <data> is one to six hex digits preceeded by any number of leading zeros.



Starts master processor. Also starts slave if slave is on-line and master is not in DISK or FROZEN mode.

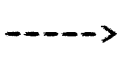


CLEAR initializes certain processor registers (PERP, PERM, MSSW, CC CD, INCN, A, BR, "M", ELOG and CACHE (unless in CONLY mode)) in the master processor. CLEAR does the same to slave also if ONLINE else performs the subset function RESET.

CCLR initializes all validity bits in the master processor's cache to indicate absence of micro-instructions.

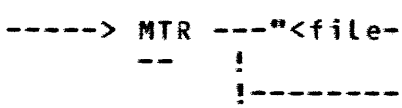
RESET is similar to CLEAR but initializes only a subset of those registers initialized by CLEAR, namely : PERP, PERM, MSSW, CC, CD, INCN.

CLRELOG initializes the Memory Subsystem Error Log (ELOG) alone.

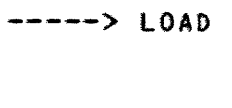


Executes one micro-instruction in master and if on-line, the slave. Screen is updated afterwards.

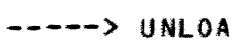
Reads the directory of the floppy disk, then displays the 60 first file names-creation dates (month-day-year) and non-standard automatic start conditions on the ODT(s).



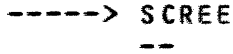
Sets DISK mode, CLEARs system, LOADS directory and fat & search the directory for the specified file name.
On succefull searches reads the first file sector.
If file-name is omited, the current reference file-name is used.
See menu section.



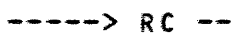
Sets DISK mode, UNLOADS and LOADS "file-name" from floppy disk to MAC RAM. If file-name is omited, the current reference file-name is used.
See menu section.



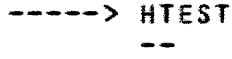
Restores head to track 0



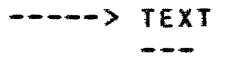
Redisplays the most recently displayed screen. Equivalent to SPCFY key.



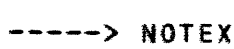
Generates RC signal on the I/O bus.



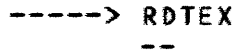
Initiates a self test of maintenance control card. This also results type fuction to the system.



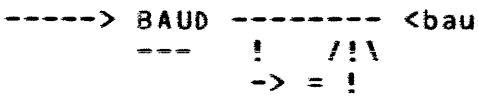
Writes <text> into descending S-Memory locations starting at the end of the previous <text> string, if any; otherwise starting at one byte location from SMAX. <tex> consist of alpha-numeric ASCII characters.



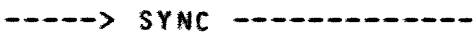
Resets byte count (kept at location SMAX) to zero. See TEXT command.



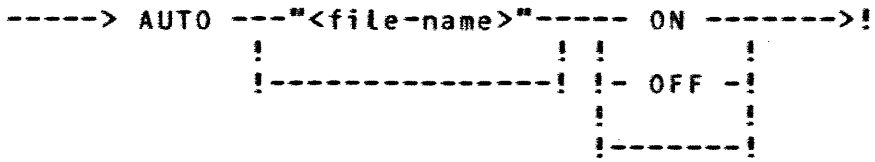
Forces display to CSE page with TEXT string displayed.



Specifies the Baud Rate for Asynchronous Remote Link operation. The Baud Rate is in BCD and the allowable values are 300, 1200, 1800.



Specifies the Remote Link operation to be Synchronous. The baud rate is determined by the modem.



AUTO will cause the specified file name to be used as the reference in a "MTR GO" command. The ON/OFF variant set or reset a flag that will cause the reference file to be MTR GO-ed at then power on/reset time without operator intervention
If no file name is specified than no change occurs to the currently referenced file.
If no variant specified the ON variant is defaulted.

CABINET PUSHBUTTON SWITCHES

Cabinet switches cause the action specified below somewhat independently of the maintenance control. If the maintenance control is performing some action such as clear, the operator should allow sufficient time for the clear to complete prior to depressing a switch such as RUN/HALT a second time.

POWER

The power switch will toggle DC power on and off. The on condition is lighted.

HALT/RUN (RUN A & B LAMPS)

Depression of RUN/HALT switch will cause both processors to halt if either is running. If both are halted, action depends on the state of the MTR mode. In MTR mode, the RUN/HALT switch will start the MAC RAM read and cause the data from the floppy to be transferred to the master processor. The slave processor is not affected. In non-MTR mode(non-FROZEN also) depression will cause the master processor to start and the slave, if on-line, to start. A change from non-MTR run to halt will stop the processor with the next micro in the M-Register. Run state is indicated by one or more of the RUN indicators lighted. A halt (programmatic, error or switch) by a processor will cause its associated lamp to be extinquished.

INTERRUPT (STATE A & B LAMPS)

If a processor is in a run state, the interrupt switch will set bit #0 in its CC-register. The interrupt signal will be active as long as interrupt button is depressed. If the processor is halted, the interrupt switch is inactive.

State lamps A and B will indicate the state of bit #3 in each processor's CC-register. A true (1) bit will cause the appropriate lamp to light while a false (0) bit will cause the lamp to be extinquished.

MODE (MTR & OVERTEMP LAMPS)

This switch will toggle the mode of the master processor between DISK (MTR) and NORMAL modes if the system is halted.

Turning on MTR equal a MTR command. It will not initiate run. Depressing the switch in run mode will not affect the system in any manner. Toggling MTR mode causes the MTR light to toggle on and off appropriately. The lamp will not accurately indicate the mode when the processor changes programmatically to MTR and continues to run. In a halt state, the MTR lamp is always accurate.

The OVERTEMP LAMP indicates detection of over temperature in the system, fan error, slave breaker off and master breaker on.

MASTER A/B (MASTER A & MASTER B LAMPS)

This switch will toggle master processor status between A and B. The master status can also be changed via the CRT terminal. The purpose of the switch is to disable a non-working processor maintenance card or a non-haltable processor which is incapable of switching master status via the CRT terminal. The switch is active if the master processor is in a halt state or, if running, the master processor is receiving a halt request (prior depression of halt switch).

The lamps will indicate which processor is currently master.

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