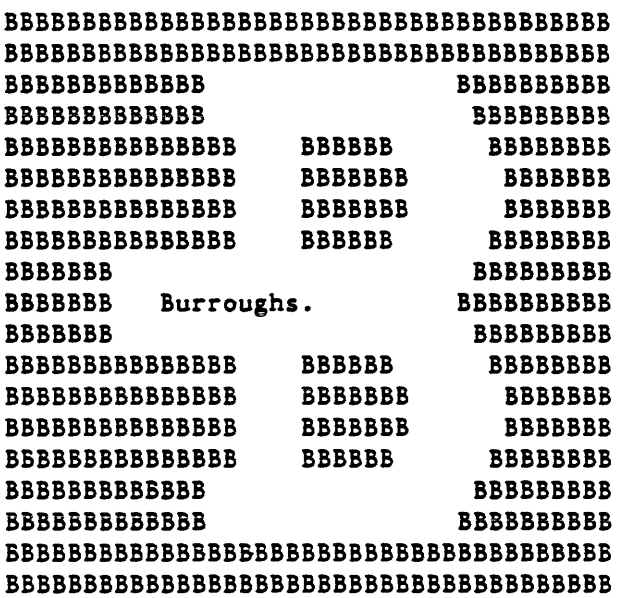
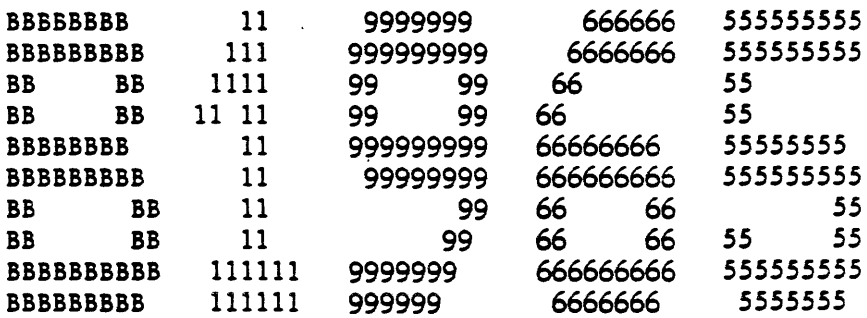
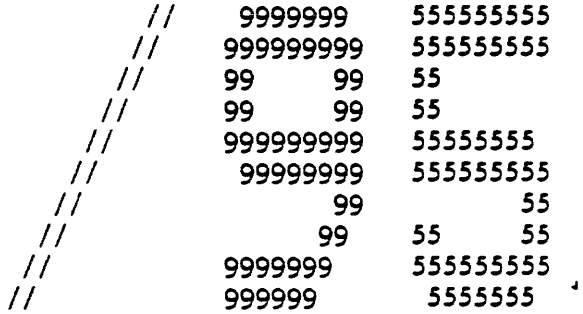
Burroughs Corporation
Parc industriel des Hauts-Sarts
B4400 Herstal
BELGIUM







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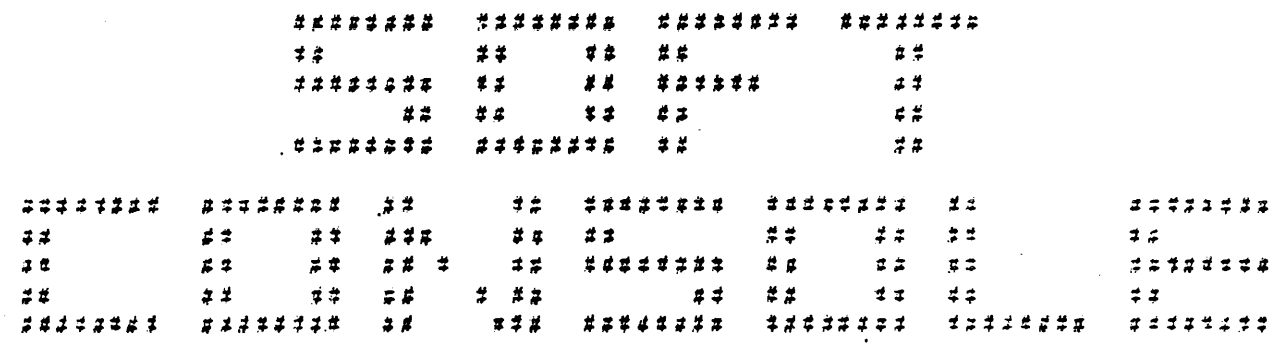

81965/1995 SOFT CONSOLE OPERATION

PROPRIETARY PROGRAM MATERIAL

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SOFT CONSOLE OPERATION

INTRODUCTION

This section of the SYSTEMS MAINTENANCE GUIDE describes the functions, features, and operational procedures associated with the SOFT CONSOLE and MAINTENANCE PROCESSOR of the 31965/31995 systems.

CONTENTS

MAINTENANCE SUBSYSTEM POWER UP ACTIVITY

When power is turned on, the following actions take place. The actions are not necessarily listed in chronological order:

- o the micro-processor on the Maintenance Card (H9) is reset.
- o a self-test of the Maintenance Card is run and if an error is encountered, a display message is attempted. (Note: Particular positions of a switch on the Maintenance Card can be used to inhibit the the normal CRT display and to indicate error type via on-card indicators.) Depending upon the type of error, the micro-processor may halt or may attempt to complete the execution of the self-test and enter the operator input-display mode of operation.
- o appropriate registers in the MASTER and SLAVE processors are cleared. For example, CACHE VALIDITY bits, A-register, PERM-register, PERP-register.
- o Processor A is set to MASTER.
- o Processor B is set to SLAVE.
- o the SLAVE processor is set ON-LINE.
- o the SLAVE processor is set to NORMAL mode.
- o the MASTER processor is set to NORMAL mode.
- o both processors are set to HALT mode.
- o entire memory is initialized with "0" data and correct ECC.
- o an initial screen display is transmitted to the terminal and displayed on page 1. (MCP messages will be directed to page 2. Toggling between pages is accomplished via the CTRL and right or left pointing arrow keys or by program control).

If the terminal is in LOCAL when the maintenance control attempts to transmit, the maintenance control will retry up to ten times. Each attempt will cause an alarm to sound, if the terminal has the alarm option enabled. If the operator switches to RECEIVE mode, the message will be displayed. If the terminal is in TRANSMIT mode, the input message will be accepted and then the output message displayed.

SCREEN DISPLAY - MENU SECTION

The screen display consists of a MENU SECTION followed by a DATA SECTION. Formats for the DATA SECTION are shown in Figures 1 thru 9, beginning on page 16. The format of the MENU SECTION is as follows:

```
COMMAND >                                                <
 Mode. .Switches. .Display ..Reads.. .....Writes..... ......Actions.....
NORMAL MASTER: A  REG S16  SRnn:addr Swnn:addr=values CLEAR RESET REWIND
SCNLY   SLAVE:OFF STK S24  CR:addr    CW:addr=values  MTR CLRELOG NOTE:
CCNLY  REMOTE:OFF CK  S39  BACK or -  register=data   CCLR  STEP  RUN GO
TAPE   SINGLE:OFF CSE MAC  NEXT or +  ALLREGS=data    MC    SCREEN HPTEST
FROZEN INTRPT:OFF OPR      RDTEXT     TEXT characters (= : are optional)
   CASSETTE: BOT        SLAVE:ABSENT        MASTER:HALTED       ERROR
```

The COMMAND line is followed by a set of reserved words which may be entered on the COMMAND line to effect a MODE change, a SWITCH change, a DISPLAY change, a REGISTER-MEMORY READ-WRITE or an ACTION. The last line of the menu indicates SYSTEM STATUS as follows:

- CASSETTE: Status can be BOT or READY or NOT READY.
- SLAVE: Status can be ABSENT or OFFLINE or HALTED or RUNNING.
- MASTER: Status can be HALTED or RUNNING.
- ERROR: Indicated if any bit of the master processor's PERP or PERM registers was true when the processor halted or if any ERROR condition arose during the last interaction of the processor with the maintenance control or whenever the MASTER processor is RUNNING despite having received a HALT request.

The MODE of the master processor, STATES of the SWITCHES, the SCREEN being displayed and the status on the STATUS line are highlighted.

Except for the COMMAND line, the entire screen is write protected, i.e., cannot be changed from the keyboard.

Entries on the COMMAND line are free format, i.e., any number of spaces may be added between commands or elements of commands. At least one space is required between commands.

Space(s) also may be used in lieu of ":", "=" and "/" in the READ and WRITE commands even though those symbols are shown in the menu.

Abbreviations are permitted as long as the abbreviation is unique. Exceptions are: H9 for H9TEST and CLRE for CLRELOG. Also, alternate forms, not shown on the menu, may be used. These forms are:

NORMAL FORM	ALTERNATE FORM	
CLEAR or CLE	CLR	
RUN or GO	START	
GO (letter O)	GO (number 0)	
CK	CACHE	
SWnn	SnnW	
SRnn	SnnR	
SnA	S0nA	
SnB	S0nB,	(n = 0 through 9)

In case of spelling, syntactical or procedural errors, an appropriate error message will be displayed and THE CURSOR WILL BE LEFT AT THE START OF THE WORD IN ERROR.

When the COMMAND line is transmitted, it is left unchanged except as noted below for memory WRITES. Transmission is from home to cursor or if cursor is at home, from home to end of the COMMAND line.

Entries on the COMMAND line are executed from left to right. The execution of RUN (except when SINGLE micro toggle is ON) or MASTER (change of master status) will cause subsequent commands, if any, to be ignored.

If commands cannot be executed for some reason , a "CONTROL" error message will be displayed on the COMMAND line.

ACTION COMMANDS

The SCREEN command or the SPCFY key will cause a redisplay of the most recently displayed screen. This command is useful to restore a screen which had been altered or cleared by the operator.

The CLEAR command will clear the master processor. It will cause the slave processor to CLEAR only if online or to RESET if offline (See RESET below). CLEAR will cause a running processor to halt. CLEAR will clear the following registers : PERP, PERM, MSSW, CC, CD, INCN, A, BR, "M", ELOG and also the CACHE if mode is not CONLY.

The CCLR command will cause all VALIDITY bits in the CACHE Memory of the master processor to be cleared.

The RESET command will cause a CLRB signal to be issued to the master processor (also slave if online), to memory and to the I/O. RESET will clear the following registers : PERP, PERM, MSSW, CC, CD and INCN. CLRB will also cause a running processor to halt.

The CLRELOG command will cause the ELOG in the memory subsystem to be cleared.

The REWIND command will cause the cassette tape to rewind to BOT and will cause subsequent commands, if dependent upon the completion of the rewind, to be delayed until the rewind is completed (e.g., RUN in TAPE mode).

The MTR command sets TAPE mode, rewinds the cassette tape to BOT and causes the CLEAR command to be executed. MTR will not cause RUN to be executed automatically.

The PC command will cause the PC signal to be sent on the I/O bus.

The H9TEST command will cause the micro-processor on the maintenance card to run a self diagnostic test and then display the H9 MAINTENANCE PROCESSOR SELF TEST SUMMARY (assuming switches on H9 card are set in the position for display).

The TEXT command will cause all <characters> (including all blanks) to the right of the word TEXT and to the left of the cursor or if the cursor is at home postion, to the end of the command line to be written into decencing S-Memory locations starting at the end of the previous <character> string, if any; otherwise, starting at one byte location from MAXS. A binary value (0 to 255) indicating the number of characters in the total string is stored at the byte location immediately prior to SMAX. If the total number of text characters would cause an overflow of the 255 byte count, the final line is not written and an error message is displayed. Execution of a NOTEXT command or power up will cause the byte count to be initialized to "0". The <characters> are stored in ASCII. The intent of this command is to allow flexibility in the manner in which cold start variables are loaded. Interpretation of the TEXT <characters> is a software function. A display of the TEXT <characters> on the CSE display may be obtained by a PDTEXT command. A CSE command will cause the TEXT <characters> to be removed from the display.

The RUN (or GO,or START) command will start only the master processor if the master is in TAPE or FROZEN modes or if the slave is OFFLINE. If the master processor programmatically changes from TAPE mode, stops the tape and continues to run, the MTR indicator on the cabinet will be extinguished. The RUN command, except when executed with SINGLE micro on, will clear the PERM and PERP registers and bit #3 of the CD register.

The STEP command is equivalent to executing the RUN command with SINGLE micro ON. STEP will step both processors if the slave is on-line. The STEP command is invalid and will cause an error message response if attempted when the processor is in TAPE mode.

Whenever two processors are started as a result of either RUN or STEP, the order in which they start is random.

MODE COMMANDS

NORMAL is a mode, which if on when RUN is executed, causes the processor to obtain its string of M-instructions in a normal manner, i.e. from Cache. Instructions not in Cache are automatically loaded to Cache from S-Memory.

CONLY is a mode, which if on when RUN is executed, causes the processor to obtain its string of M-instructions from Cache only. Instructions not in Cache will cause a halt.

SONLY is a mode, which if on when RUN is executed, causes the processor to obtain its string of M-instructions from S-Memory only.

TAPE is a mode, which if on when RUN is executed, causes cassette data to be transferred to the master processor. Cassette data may be M-instructions or M-instructions followed by a data field.

FROZEN is a mode, which if on when RUN or STEP is executed, causes the master processor to retain the micro-instruction contained in the M register after execution of the command. For RUN with SINGLE micro OFF, the micro-instruction is executed repeatedly until halted via the Halt switch on the cabinet. For STEP or for RUN with SINGLE micro ON, the micro-instruction is executed once. The A register is incremented for each execution.

SWITCHES

MASTER is a toggle which causes a switch of master status between processors. When master status is switched, the MODE of the slave is forced to NORMAL. The INTRPT, the SINGLE micro and the SLAVE on-off toggles are not changed.

SLAVE is a toggle which causes the slave processor to change its ON-LINE/OFF-LINE status.

INTRPT is a toggle which, when ON, causes BIT 0 in the CC register of a running processor to be set each clock time. INTRPT OFF does not affect BIT 0 in any manner. The state of the INTRPT switch is not changed if master status is changed.

SINGLE micro is a toggle which, if ON when RUN or STEP is executed, causes the master processor and the slave, if on, to execute one micro-instruction, then halt and then automatically update the last version of the screen display. The state of the SINGLE micro switch is not changed if master status is changed. SINGLE micro ON and TAPE mode are mutually exclusive and will result in an error message response if both are true when a RUN or STEP is attempted.

SPECIAL REGISTERS

A write to the CMND register will cause the write data and a CA signal to be transmitted on the I/O bus. Displayed in the CMND register will be the data last transmitted.

A write to the DATA register will cause the write data and a RC signal to be transmitted on the I/O bus. Displayed in the DATA register will be the data on the I/O bus being received from the I/O, not the write data sent by the processor. Note: The DATA register will always reflect data on the I/O bus that is currently being received from the I/O. It will be updated after each action by the processor.

CNS is cleared by power up. It is not cleared by switching master status or by CLEAR.

Operator changes in MSSW will not cause a change in MODE. MODE changes by the operator must be affected by a 'MODE' change entry on the command line. The current MODE being displayed will be forced into the MSSW register prior to execution of RUN or STEP. Similarly, the value in MSSW will cause the appropriate MODE to be displayed when the processor changes from a RUN to a HALT state. MSSW is set appropriately (0000 for master and 1000 for slave) by power up, CLEAR, or by a change in master status.

SCREEN DISPLAYS

OPP will cause a display of the operator information registers and some system operating instructions (see Figure 1).

STK will cause a display of all 32 locations of the A-Stack as well as TAS (see Figure 2).

REG will cause a display of the processor's registers, psuedo-registers and scratchpad-registers (see Figure 2).

CSE will cause a display of the ELOG and a selected set of registers that are particularly important to the system's operation (see Figure 3).

A RDTEXT operation will also cause a display of the CSE page. But, in addition to the display of the CSE set of registers, it will cause a display of up to 255 text <characters> from memory.

MAC will cause a display of the micro-processor's input/output ports and key variables of the firmware (see Figure 5).

S16, S24 and S39 will cause a display of S-Memory while CK will cause a display of Cache Memory (see Figures 7, 8, and 9). The memory locations displayed will be those locations that were most recently displayed for the particular screen requested. Power up or halt will cause a default starting location of zero.

The H9TEST command will cause a display of the H9 MAINTENANCE PROCESSOR SELF TEST ERROR SUMMARY display. This display is also attempted at power up time if an error occurs (see Figure 4).

READS AND WRITES

The S-Memory (SRnn) and Cache Memory (CR) read commands cause a screen display of the appropriate memory page starting with the location specified by <addr>. If the S-memory subsystem indicates an error, ERROR will be displayed on the status line as a result of PERM being nonzero. For SR16 and SR24 reads, the location of the last logged S-Memory error may be obtained by switching to the CSE page which displays the ELOG. For SR39 reads, the micro-processor will clear PERM and ELOG prior to reading each memory word and display its value along with each word after the individual word is read. Cache Memory errors are not indicated but the key parity and the micro-instruction parity bits are included in the cache display.

The NEXT and BACK (or + and -) commands are applicable only when on a CACHE or S-MEMORY page. On a memory page they cause scrolling forward or backwards by one page. Wraparound is permitted in either direction. On a non-memory page they cause no action other than a display of an error message.

A READ or WRITE to Cache or to S-Memory will not cause the A-register or FA-register or any other register to be changed. Registers, except for those carrying specific control or status information can be changed only by designating them as a destination. Note however, that the A register counts during RUN and STEP.

An automatic screen update will occur on a Cache page if a Cache write is executed, or, on an S-Memory page if an S-Memory write is executed. Also an automatic screen update of the currently displayed page will occur if it is possible that the page could have been changed by any type of register write, memory write or command execution.

<addr> may be one or more hex digits. If less than six digits are entered, <addr> will be right justified and zeros assumed on the left. If greater than six digits, an error message will be displayed if any of the leading digits to the left of the first six are non-zero. <addr> is interpreted as a bit address. For CACHE (CR & CW) and for S-Memory (SR16, SW16, SR39 and SW39) accesses, an appropriate number of rightmost bits of <addr> are ignored and zeros assumed. The ":" preceeding <addr> is optional.

<value> may be one or more hex digits. <value> will be right justified and either zero filled or truncated on the left as required. Truncation of non-zero digits will be reported as an error. The "=" preceeding <value> is optional. Formats for <value> depend upon the page being written:

S39: "Address" xx xxxx xxxx or xx:xxxx:xxxx	SW39 FF0 EC DATA DATA
S16: "Address" xxxx	SW16 F20 DATA (16)
S24: "Address" xxxxxx	SR24 121
CK: "Address" xxxx	CK FF0 (cache read)

The EC displayed in the S39 page contains a parity bit in the lower ordered bit position. This bit is generated by the memory control on the data read from memory. When writing, this bit of the EC is ignored.

In the CK display, a micro-instruction parity bit (contained in the fifth digit from the right) preceeds the micro-instruction. When writing, this bit is generated by the maintenance control. Also when writing into cache, the hit bit, the validity bit and the key parity bit are generated by the processor. The key is taken from <addr>.

A S-memory or Cache write command can have a multiple number of values associated with the write. The values are separated by commas and are written into memory starting with the given <addr> and proceeding to higher addressed locations. If a comma is the last entry on the command line, a new memory write command is prompted on the command line starting in the leftmost position. The <addr> will be six digits long and will point to the memory location next to be written. The cursor will be left in the position immediately to the right of the = in the prompted command. If a comma does not follow the last value, the command line will not change. Note that a prompted Write command will overwrite any characters on the command line in the first 10 to 12 positions. It will not affect the rest of the line.

The PDTEXT operation forces the CSE page and displays the TEXT <characters>, if any, contained in memory.

CNS REGISTER

This register is used by the processor as a source or a destination. When used as a destination, hex values may be passed to the maintenance control to effect an action as noted below. Responses to the requests are returned in CNS immediately or after completion of the requested action as indicated below.

REQUEST	CNS VALUE	CNS RESPONSE	ACTION
Enable Commands	000081	000081	Subsequent values of 000001-000036 and 000040-000042 moved to CNS will be interpreted as commands. Commands 000040-000042 are valid for master only.
Enable U Parity	000082	000082	Subsequent reads of cassette data will have a parity bit included, suitable for writing to cache.
Disable Commands	000083	000083	CNS command interpretation is disabled. Also disabled are any pending deferred responses. Disabled is the normal or default state.
Disable U Parity	000084	000084	Cassette data transferred to the processor will not include a parity. This is the normal or default state.
Set "keep-page"	000085	000085	This command sets the "keep-page" toggle. If this toggle is true when the processor halts, a message will be displayed on the 25th line of the ODT, indicating that the status information is available on page 1. The keep-page toggle is set false each time the processor is started.
Set Interrupt	000001	000000	Set interrupt toggle ON. Effective only for processor performing the move to CNS.
Get Status	000002		Return a status vector (see below).
Halt Slave	000003	000000	Set slave's halt request.

(continued next page)

REQUEST	CNS VALUE	CNS RESPONSE	ACTION
Halt Processors	000004	000000	Set both master's & slave's halt request.
Reset Interrupt	000005	000000	Reset interrupt toggle. Effective only for the processor performing the move to CNS.
Get Baud Rate	000006	Baud Rate	Returns the presently set Remote Link Async baud rate. (see notes below)
Halt Restart	000040	000040	Master is restarted after a halt. CNS is set to 000000.
MTR Restart	000041	000041	A CLEAR, set TAPE mode, REWIND and RUN (restart) is executed after the processor halts.
ALLREGS Restart	000042	000042	All processor's registers (including STK) are set to the value of the "X" register, except CNS, which is set to 000000. Action is after processor halts.
Invalid	others		Treated as Disable commands, Disable U parity, and Reset Keep-page. Any pending deferred command is lost.

Commands 000001-000042 are recognized only if an Enable Command (000081) has been executed.

Commands 000081 to 000085 are completely independent.

Commands 000040-000042 are valid only for master processor. They are ignored by a slave.

Only one CNS command can be retained; therefore the deferred action of only the last received command will be done. This is especially important in using the restart commands (000040-000042).

The Baud Rate returned is not defined if link is set for Synchronous operation. The format of the Baud Rate is BCD. Presently allowable baud rates are 300, 1200 and 1800.

STATUS VECTOR (24 bits):

MSB																							LSB
!	0	0	0	0	0	0	S	R	a	a	a	a	a	a	b	c	d	e	f	g	h	i	!

a. Firmware level number
b. Slave online (not valid in single processor system)
c. Not running
d. Not A-processor
e. Halt requested
f. Other processor halted (not valid for single processor
f. Other processor halted (not valid for single processor
g. Not TAPE mode
h. A-processor is master
i. B-processor is absent (valid for A-processor only)

R. Remote Switch ON.
S. Remote Link is synchronous (not valid when R=0).

OPR DISPLAY

B1965/95 PROCESSOR SYSTEM

```
TO INITIATE OPERATING SYSTEM :1)Place CLEAR/START cassette in Drive.
                              2)Set System Disk Drive to RUN.
                              3)Type MTR GO on COMMAND line and push XMT
TO INITIATE MEMORY DUMP      :1)Type TEXT DUMP and push XMT.
                              2)Initiate Operating System as above.
TO TOGGLE STATE OF SWITCH    :Type name of switch and push XMT.
TO CHANGE DISPLAY PAGE       :Type name of page and push XMT.

OPERATOR INFORMATION REGISTERS:
      T = xxxxxx    X =          PERM =          A =
      L =           Y =          PERP = 1        LR =

              CPU-CONDITION : CASSETTE ERROR
              :
```

FIGURE 1 - DISPLAY FORMAT -- OPR

REGISTER DISPLAY

TA=.....x	FU=.....x	X=xxxxxx	SUM=	S0A=	S0B=
TB=	FT=	Y=	CMPX=	S1A=	S1B=
TC=	FLC=	T=	CMPY=	S2A=	S2B=
TD=	FLD=	L=	XANY=	S3A=	S3B=
TE=	FLE=	A=	XEQY=	S4A=	S4B=
TF=	FLF=	"M"=.xxxxx	MSKX=	S5A=	S5B=
CA=	BICN=	BR=	MSKY=	S6A=	S6B=
CB=	FLCN=	LR=	XORY=	S7A=	S7B=
LA=	NULL=	FA=	DIFF=	S8A=	S8B=
LB=	RSVD=	FB=	MAXS=	S9A=	S9B=
LC=	PERM=	FL=	NULL=	S10A=	S10B=
LD=	PERP=	TAS=	"U"=..xxxx	S11A=	S11B=
LE=	XYCN=	CP=....xx	NULL=	S12A=	S12B=
LF=	XYST=	NULL=	DATA=	S13A=	S13B=
CC=	INCN=	CNS=	CMND=	S14A=	S14B=
CC=	MSSW=	TIME=	NULL=	S15A=	S15B=

STK DISPLAY

TAS= xxxxxx

STACK 00=xxxxxx
STACK 01=
.
.
.
STACK 0F=

STACK 10=
STACK 11=
.
.
.
STACK 1F=

FIGURE 2 - DISPLAY FORMATS -- REG and STK

CSE DISPLAY (with TEXT)

```
X = xxxxxx      PERP = .....x      LR = xxxxxx      "M" = .xxxxx

Y = PERM = BR = A =

T = CC = FA = TAS =

L = CD = FB = INCN = .....x

ELOG = xxxxxx CNS = xxxxxx

TEXT IS nn BYTES ----------------
```

("nn" bytes of S-Memory starting with the byte at SMAX-3 and proceeding to lower numbered locations. "nn" is 0 to 255.)

FIGURE 3 - DISPLAY FORMAT --CSE

H9TEST DISPLAY

H9 MAINTENANCE PROCESSOR SELF TEST ERROR SUMMARY

PROCESSOR A

1	*ROM	xxxxxxxx
2	*RAM	
3	*CLOCK	
4	MPPI	
5	USART	
6	CASSETTE	
7	LOGIC A	
8	LOGIC B	
9	LOGIC C	
A	*CPU CLEAR	
B	MEX ECHO	xxxxxx xxxxxx xxxxxx
C	IO ECHO	xxxxxx xxxxxx xxxxxx
D	INTERRUPT	

* FAILURES IN THESE TEST MAY INVALIDATE SUCCEEDING RESULTS

. press SPCFY (or xmit SCREEN) for state display

FIGURE 4 - DISPLAY FORMAT -- H9TEST

MAC DISPLAY

```
 H CARD MEX OPERATION                CPU CONTROL (FOR H CARD)
-------------------------           --------------------------------

Driver port     =    xxxxxx         During last MAC micro (xxxx)
  Enabled :  YES                    Expected :  WRITE TO MAC (CNS<=MEX)
  (inverted)                        Observed :  WRITE TO MAC (CNS<=MEX)
Receiver port   =    xxxxxx
  Selected:    NO                   Current  :   READ "U" (MEX<=U -FETCH
                                                          MAC IF HALTED)

      Saved CPU Registers : "M" = xxxxxx "A1" = xxxxxx "CNS" = xxxxxx

 RS232 Information                  CASSETTE INFORMATION
-------------------------           --------------------------------

Last Attempt : SELECT               Tape status : NO ERROR
Baud Rate    : 1200                 Record Count: xx
Status       : NO ERROR             Micro Count : xx
```

Figure 5 - DISPLAY FORMAT -- MAC

RUN DISPLAY

```
COMMAND >                                          <
 Mode.  .Switches.
NORMAL MASTER: A
SONLY   SLAVE:OFF
CONLY  REMOTE:OFF          S Y S T E M    R U N N I N G
TAPE   SINGLE:OFF
TAPE   SINGLE:OFF
  DISPLAY OF CPU STATE AT TIME OF LAST START (NOT UPDATED DURING RUN)
```

FIGURE 6 - DISPLAY FORMAT -- RUN

S24 DISPLAY

Address Data	Address Data	Address Data	Address Data	Address Data
000000=xxxxxx	000120=	000240=	000360=	000480=
000018=	000138=	000258=	000378=	000498=
000030=	000150=	000270=	000390=	0004B0=
000048=	000168=	000288=	0003A8=	0004C8=
000060=	000180=	0002A0=	0003C0=	0004C8=
000078=	000198=	0002B8=	0003D8=	0004E0=
000090=	0001B0=	0002D0=	0003F0=	000510=
0000A8=	0001C8=	0002E8=	000408=	000528=
0000C0=	0001E0=	000300=	000420=	000540=
0000D8=	0001F8=	000318=	000438=	000558=
0000F0=	000210=	000330=	000450=	000570=
000108=	000228=	000348=	000468=	000588=

S16 DISPLAY

Address Data	Address Data	Address Data	Address Data	Address Data
000000=..xxxx	0000C0=	000180=	000240=	000300=
000010=	0000D0=	000190=	000250=	000310=
000020	0000E0=	0001A0=	000260=	000320=
000030	0000F0=	0001B0=	000270=	000330=
000040	000100=	0001C0=	000280=	000340=
000050	000110=	0001D0=	000290=	000350=
000060	000120=	0001E0=	0002A0=	000360=
000060	000130=	0001F0=	0002B0=	000370=
000080	000140=	000200=	0002C0=	000380=
000090	000150=	000210=	0002D0=	000390=
0000A0	000160=	000220=	0002E0=	0003A0=
0000B0	000170=	000230=	0002F0=	0003B0=

FIGURE 7 - DISPLAY FORMATS -- S24 and S16

S39 DISPLAY

```
Address   EC Data EC Data PERM/ELOG  Address   EC Data EC Data PERM/ELO

000000 = xx xxxx xx xxxx x  xxxxxx   000180 =
000020 =                             0001A0 =
000040 =                             0001C0 =
000060 =                             0001E0 =

000080 =                             000200 =
0000A0 =                             000220 =
0000C0 =                             000240 =
0000E0 =                             000260 =

000100 =                             000280 =
000120 =                             0002A0 =
000140 =                             0002C0 =
000160 =                             0002E0 =
```

FIGURE 8 - DISPLAY FORMAT -- S39

CK DISPLAY

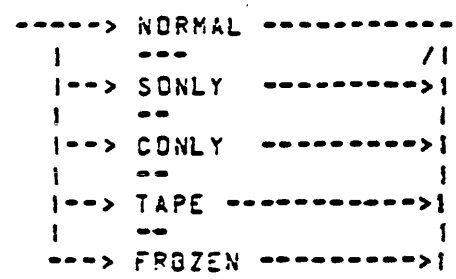
```
Addr   Key P H V Cache  Addr   Key P H V Cache  Addr   Key P H V Cache
000000 xx x x x .xxxxx 0000C0 xx x x x .xxxxx 000180 xx x x x .xxxx
                .xxxxx                .xxxxx                .xxxx
                .xxxxx                .xxxxx                .xxxx
                .xxxxx                .xxxxx                .xxxx

000040 xx x x x .xxxxx 000100 xx x x x .xxxxx 0001C0 xx x x x .xxxx
                .xxxxx                .xxxxx                .xxxx
                .xxxxx                .xxxxx                .xxxx
                .xxxxx                .xxxxx                .xxxx

000080 xx x x x .xxxxx 000140 xx x x x .xxxxx 000200 xx x x x .xxxx
                .xxxxx                .xxxxx                .xxxx
                .xxxxx                .xxxxx                .xxxx
                .xxxxx                .xxxxx                .xxxx
```

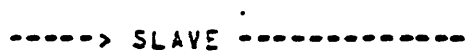
FIGURE 9 - DISPLAY FORMAT -- CK

COMMAND LINE SYNTAX

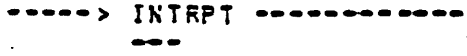


Determines the source of the master processor micro-instructions when RUN or STEP is commanded.

Toggles master processor between processor A and processor B. forces new slave to normal mode and switches control of the display to the new master.

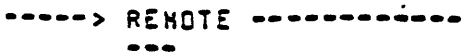


Toggles slave processor ON and OFF.

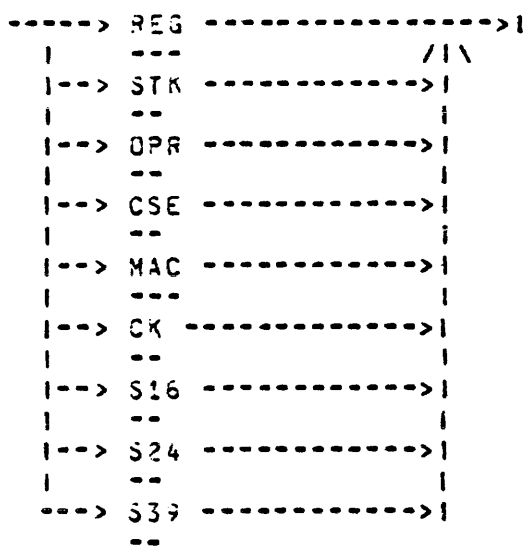


Toggles interrupt ON and OFF. ON causes bit #0 in cc-register of each processor to be set each clock time during RUN or STEP. OFF causes no action.

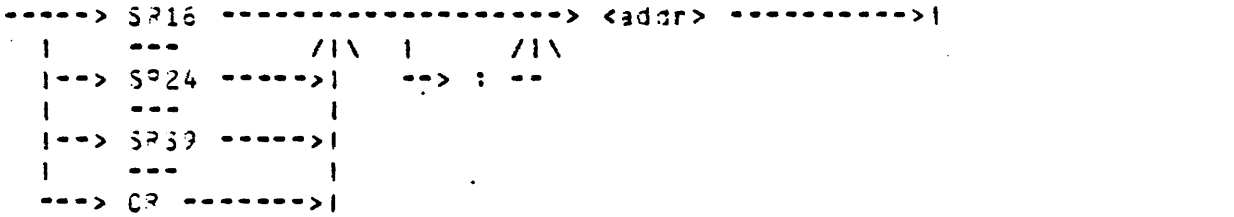
Toggle SINGLE micro ON and OFF. ON causes execution of one micro-instruction when RUN is commanded.



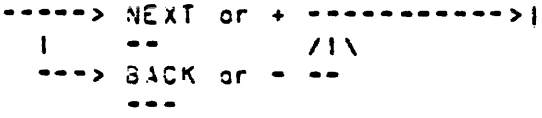
Toggles REMOTE link switch ON and OFF. ON causes the remote diagnostic link to be activated.



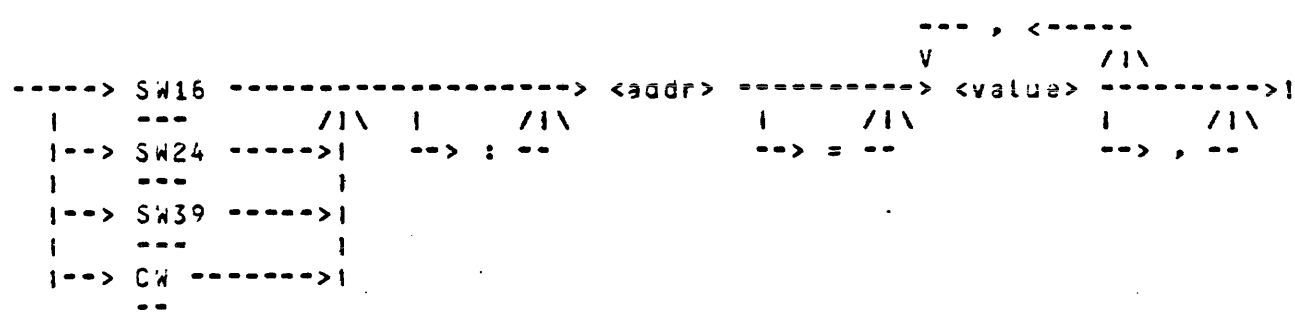
Displays registers, stack, selected registers, maintenance control information, Cache-Memory or S-Memory.



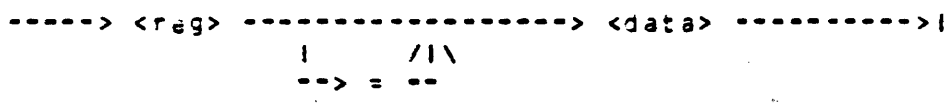
Displays S-Memory or Cache starting at the specified <addr>.



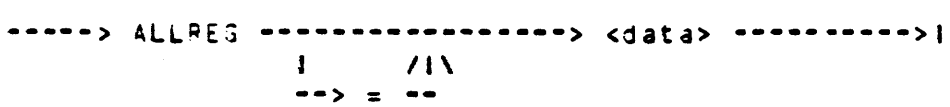
Scrolls forwards/backwards by one page. Valid only on memory page.



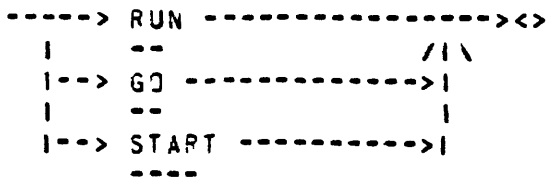
Writes <value> string into corresponding consecutive memory location starting with location <addr>. Commas separate more than one <value>. If a comma is the last entry on the command line, a new <addr> pointing to the memory location next to be written is prompted. <value> may be one to six hex digits preceeded by any number of leading zeros. Usual formats are CW: XXXX, S16: XXXX, S24: XXXXXX, S39: EE XXXX XXXX or EE/XXXX/XXXX. Where EE are the ECC bits



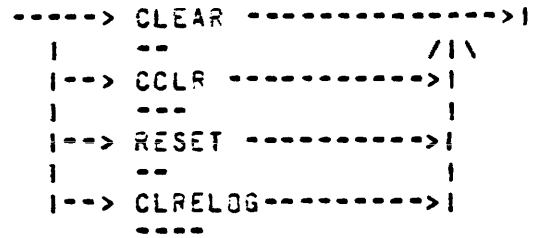
Writes <data> into specified register. <data> is one to six hex digits preceeded by any number of leading zeros.



Writes <data> into a predetermined set of processor's registers. <data> is one to six hex digits preceeded by any number of leading zeros.



Starts master processor. Also starts slave if slave is on-line and master is not in TAPE or FROZEN mode.

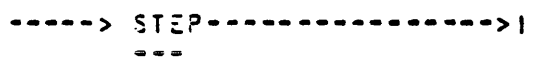


CLEAR initializes certain processor registers (PERP, PERM, MSSW, CC CD, INCN, A, BR, "M", ELOG and CACHE (unless in CONLY mode)) in the master processor. CLEAR does the same to slave also if ONLINE else performs the subset function RESET.

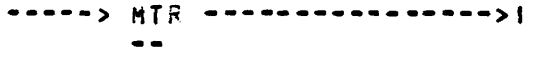
CCLR initializes all validity bits in the master processor's cache to indicate absence of micro-instructions.

RESET is similar to CLEAR but initializes only a subset of those registers initialized by CLEAR, namely : PERP, PERM, MSSW, CC, CD, INCN,

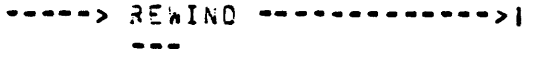
CLRELOG initializes the Memory Subsystem Error Log (ELOG) alone.



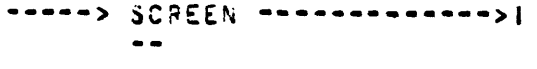
Executes one micro-instruction in master and if on-line, the slave. Screen is updated afterwards.



Sets TAPE mode, CLEARs system and REWINDs tape.



Rewinds tape.



Redisplays the most recently displayed screen. Equivalent to SPCFY key.

-----> RC ---------->|
--

Generates RC signal on the I/O bus.

-----> H9TEST ---------->|
--

Initiates the Maintenance Control card's self test.

-----> TEXT ---------- <text> ---------->|

Writes <text> into descending S-Memory locations starting at the end of the previous <text> string, if any; otherwise starting at one byte location from SMAX. <tex> consist of alpha-numeric ASCII characters.

-----> NOTEXT ---------->|

Resets byte count (kept at location SMAX) to zero. See TEXT command.

-----> RDTEXT ---------->|
--

Forces display to CSE page with TEXT string displayed.

-----> BAUD -------- <baud rate in BCD>-->|
--- | /|\
-> = |

Specifies the Baud Rate for Asynchronous Remote Link operation. The Baud Rate is in BCD and the allowable values are 300, 1200, 1800.

-----> SYNC ---------->|
--

Specifies the Remote Link operation to be Synchronous. The baud rate is determined by the modem.

CABINET PUSHBUTTON SWITCHES

Cabinet switches cause the action specified below somewhat independently of the maintenance control. If the maintenance control is performing some action such as clear, the operator should allow sufficient time for the clear to complete prior to depressing a switch such as RUN/HALT a second time.

POWER

The power switch will toggle DC power on and off. The on condition is lighted.

HALT/RUN (RUN A & B LAMPS)

Depression of RUN/HALT switch will cause both processors to halt if either is running. If both are halted, action depends on the state of the MTR mode. In MTR mode, the RUN/HALT switch will start the MTR tape read and cause the data from the cassette to be transferred to the master processor. The slave processor is not affected. In non-MTR mode(non-FROZEN also) depression will cause the master processor to start and the slave, if on-line, to start. A change from non-MTR run to halt will stop the processor with the next micro in the M-Register. Run state is indicated by one or more of the RUN indicators lighted. A halt (programmatic, error or switch) by a processor will cause its associated lamp to be extinguished.

INTERRUPT (STATE A & B LAMPS)

If a processor is in a run state, the interrupt switch will set bit #0 in its CC-register. The interrupt signal will be active as long as interrupt button is depressed. If the processor is halted, the interrupt switch is inactive.

State lamps A and B will indicate the state of bit #3 in each processor's CC-register. A true (1) bit will cause the appropriate lamp to light while a false (0) bit will cause the lamp to be extinguished.

MODE (MTR & OVERTEMP LAMPS)

This switch will toggle the mode of the master processor between TAPE (MTR) and NORMAL modes if the system is halted.

Turning on MTR rewinds the tape to BOT if not at BOT and clears the system. It will not initiate run. Depressing the switch in run mode will not affect the system in any manner. Toggling MTR mode causes the MTR light to toggle on and off appropriately. The MTR lamp is extinguished if the processor is running and the cassette is halted. This could occur only by a programmatic change from MTR to non-MTR mode. If the cassette is not halted after a programmatic change from MTR, the MTR lamp will not accurately indicate the mode. Also the lamp will not accurately indicate the mode when the processor changes programmatically to MTR and continues to run. In a halt state, the MTR lamp is always accurate.

The OVERTEMP LAMP indicates detection of over temperature in the system.

MASTER A/B (MASTER A & MASTER B LAMPS)

This switch will toggle master processor status between A and B. The master status can also be changed via the CRT terminal. The purpose of the switch is to disable a non-working processor maintenance card or a non-haltable processor which is incapable of switching master status via the CRT terminal. The switch is active if the master processor is in a halt state or, if running, the master processor is receiving a halt request (prior depression of halt switch).

The lamps will indicate which processor is currently master.

NOTES

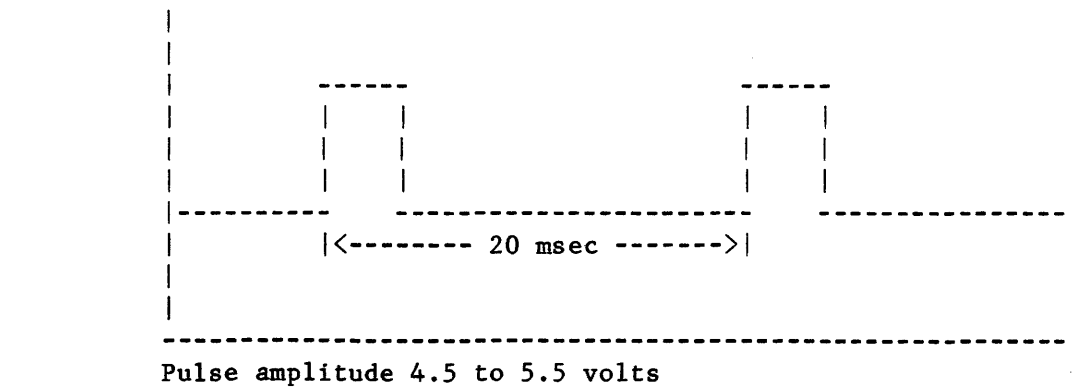
B1990 FAN FAILURE GUIDE

1. When audible alarm is heard, an intermittent high-pitched tone, one of the fans in the bottom of the processor cabinet is either stopped or slowed down.

2. To determine which of the eight fans is bad, refer to the AIR LOSS board and read the LED display. Using the following table, decode the fan which is bad:

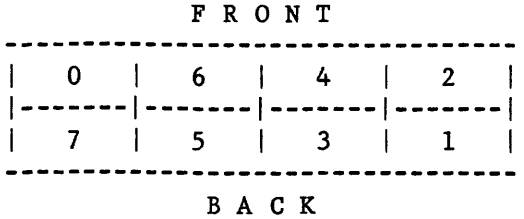
BINARY BIT WEIGHT				FAULTY
8	4	2	1	FAN NO.
ON	ON	ON	ON	All Ok
OFF	OFF	OFF	ON	1
OFF	OFF	ON	OFF	2
OFF	OFF	ON	ON	3
OFF	ON	OFF	OFF	4
OFF	ON	OFF	ON	5
OFF	ON	ON	OFF	6
OFF	ON	ON	ON	7
OFF	OFF	OFF	OFF	8

3. Another fan check involves attaching an O-scope to each resistor on the HALL EFFECT SENSE board behind the rear power supplies. Check for the proper pulse durations and time periods as compared to the disgram below:



Pulse amplitude 4.5 to 5.5 volts

4. Fan Layout in Processor cabinet:



FROM 12.0 SOG (Native System) not CMS

SECTION 4
CLEAR/START and Memory Dump Procedure

The CLEAR/START program is a stand-alone utility that is used to bring a B 1000 system to an operable state. The process has three parts: (1) bootstrapping: loading the CLEAR/START program from the cassette into system memory, (2) clear-starting, performed by the CLEAR/START program itself, and (3) system initialization, performed by the SYSTEM/INIT program. This program is brought into memory from disk at the appropriate time by the CLEAR/START program.

Execution of the CLEAR/START program is required after any of the following events:

- Execution of the COLDSTART/DISK or COLDSTART/TAPE programs.
- A system power-up; to start a day, for example.
- A system failure that results in an irrecoverable system loop or system halt.
- Execution of another stand-alone program such as PACK/INIT, DISK/DUMP, or STANDALONE/DISK-DUMP.
- Certain of the system software changes that can be specified by the CM system command.
- Setting or resetting of any of the following options: BRGR, FLMP, MPRI, LOG, RFAC, THR, TOUT, VLCP, VLIO.
- A change in the size of the Interpreter Dictionary specified by the IC system command.

CLEAR START FUNCTIONS

The CLEAR/START program performs the following functions:

1. Dumps a copy of main memory to the disk file SYSTEM/DUMPFILE when a memory dump is requested.
2. Clears main memory, writing zeros and correct parity throughout.
3. Scans the I/O subsystem to locate the system disk.
4. Saves certain registers and toggles that specify temporary environment changes for the SYSTEM/INIT (system initializer) program.
5. Loads the SYSTEM/INIT program into memory from the system disk.
6. Turns control over to the SYSTEM/INIT program.

SYSTEM INITIALIZATION FUNCTIONS

After receiving control from the CLEAR/START program, the SYSTEM/INIT program performs the following functions:

1. Supplements the information in SYSTEM/DUMPFILE, when a memory dump is requested, by adding (copying) certain MCPII structures such as the Name Table and the ODT Queue.

2. Allocates space for the initial structures in memory required for MCP operation, such as the Interpreter Dictionary and the MCP Stacks.

3. Loads the GISMO program into memory from the system disk, builds the Interpreter Dictionary entry for GISMO, and discards all GISMO segments not required because of the system hardware configuration, or because certain MCP options (such as MPRI) are not set.

4. Loads segment zero (non-overlayable) and segment one (overlayable initialization routines) of the MCPII into memory from the system disk, and sets up the initial memory link structures required.

5. Loads segment zero of the SDL2 Interpreter into memory from the system disk and builds the required Interpreter Dictionary entry.

6. Turns control over to the MCP.

MCP FUNCTIONS

When the MCP receives control from the SYSTEM/INIT program, a number of operations are performed before the system is actually ready to begin program execution. The MCP performs the following routines as part of system initialization:

1. Tests the I/O subsystem to determine the system configuration. The Input/Output Assignment Table (IOAT), constructed from this information, contains entries that describe the characteristics of all peripheral units present on the system.

2. Constructs the initial chain of DISK I/O descriptors, as well as TEST I/O descriptors for all other peripheral units present on the system.

3. Restores entries in the Temporary Disk Available Table to the Working Available Table.

4. Reads the disk directory and every disk file header (DFH) present on the system disk, clearing the user count in any DFH that was in use prior to the CLEAR/START. Disk files marked as TEMPORARY (such as compile and go code files) are removed from the disk directory.

5. Places entries identifying the CLEAR/START in the SYSTEM/LOG (if the LOG option is set) and the SYSTEM/ELOG.

6. Initiates the SYSTEM/ODT program and, if the AMCS option is set, the MCS program.

7. Displays the CLEAR/START message on the operator display terminal (ODT), and then makes the system available for use.

OPERATING INSTRUCTIONS

Two sets of procedures for beginning the CLEAR/START operation follow. The first is for B 1965/B 1995 systems and the second is for all other B 1000 systems.

Clear-starting B 1965/B 1995 Systems

To begin a clear-start for B 1965/B 1995 systems:

1. Halt the system by entering the MCP command HALT via the ODT and pressing XMT. The RUN A light goes out in a single-processor (B 1965) system; both RUN A and RUN B go out in a dual-processor (B 1995) system.

   NOTE
   Instructions for using the B 1965/B 1995 Soft Panel in this fashion are hereafter presented as follows:

   <keyword-1> <keyword-2> ... [XMT]

   A looping condition could deny access to the ODT. In such cases, press the INTRPT push button. If the system still does not halt, press the HALT/RUN push button.

2. Place the CLEAR/START cassette into the cassette reader and observe that the tape rewinds to BOT. (Blue light on the drive unit comes on; BOT appears on the ODT. If rewind does not complete, enter REWIND [XMT] from the keyboard.

3. Enter any temporary environment changes (such as a memory dump request) with the appropriate TEXT Soft Panel command. For details, refer to the subsection titled Temporary Environment Changes.

4. CLEAR MTR GO [XMT]

The clear-start operation automatically rewinds the cassette on B 1965/B 1995 systems.

Clear-starting Other B 1000 Systems

To begin a clear-start for all other B 1000 systems:

1. Halt the system using either the INTRPT push button or the console INTERRUPT switch. If the INTERRUPT switch is used, return it to initial position following the halt. If the system continues to run, press the HALT push button. If the system still continues to run, press the HALT and CLEAR push buttons simultaneously. For dual-processor systems be sure both processors are halted (both RUN lights are out).

2. Place the CLEAR/START cassette into the cassette drive and ensure that the tape rewinds to BOT.

3. Press (1) the CLEAR push button, (2) the MODE push button to obtain the MTR mode, and (3) the START push button.

4. After the bootstrap loader is read from the cassette tape, the processor halts. The L register must contain @AAAAAA@ at this time; if not, the cassette must be rewound and the procedure restarted from step 3, above.

5. Any temporary environment changes to be made (such as a memory dump request) must now be entered into the appropriate registers now. For details, refer to the subsection titled Temporary Environment Changes.

6. Press the MODE push button to enter the NORMAL mode; then press the START push button. Reading of the cassette resumes. When the CLEAR/START program is completely loaded, it takes control and executes through the system initialization procedure to completion.

7. Rewind the cassette tape by pressing REWIND. (Rewind is automatic in B 1900 systems.)

DESCRIPTION OF THE NAME TABLE

The Name Table is a structure that is initialized on a system disk by the COLDSTART/TAPE or COLDSTART/DISK programs. The Name Table contains entries identifying the names of system firmware and software available for use in the operational environment of the system. Name Table functions are shown in table 4-1.

Table 4-1. Name Table Functions, Entries, and Mnemonics

Name Table Item	- Type	Entry #	Mnemonic
System Initializer	- Standard	0	N
System Initializer	- Experimental	1	NX
GISMO	- Standard	2	G
GISMO	- Experimental	3	GX
SDL2 Interpreter	- Standard	4	I
SDL2 Interpreter	- Experimental	5	IX
MCPII	- Standard	6	M
MCPII	- Experimental	7	MX
Micro-MCP	- Standard	8	MM
Micro-MCP	- Experimental	9	MMX
Network Controller	- Standard	10	C
Network Controller	- Experimental	11	CX
MCS Program	- Standard	12	MCS
MCS Program	- Experimental	13	MCX
SYSTEM/ODT Program	- Standard	14	ODT
SYSTEM/ODT Program	- Experimental	15	ODX
SYSTEM/COPY Program	--	16	CPY
Usercode/Password File	--	17	US

Software and firmware routines are selected by the CLEAR/START and SYSTEM/INIT programs from entries in the Name Table. This is based on the system's hardware configuration as well as on certain optional specifications that can be entered by the system operator. Normally, it is unnecessary for the system operator to enter any specifications for the CLEAR/START program. Changes to the default selections are usually made only by Burroughs software development and support personnel in the course of system design and debugging, and are not required during normal system operation.

The Name Table design allows certain system software or firmware routines to be identified as "experimental" without affecting those routines identified as "standard". This permits a CLEAR/START to be performed with non-standard or untested routines by Burroughs software development personnel without the danger of not being able to recover to the "standard" software in an irrecoverable failure occurs in an experimental routine. Such a design also has application in a normal operating environment: backup copies of system software or firmware can be created and identified as experimental in the Name Table to enable recovery in the event the standard routines are corrupted.

The Name Table itself consists of 18 entries, each identified by an entry number and a mnemonic. The entry number is used by the CLEAR/START and SYSTEM/INIT programs and the mnemonic is used by the MCP and the system operator. Each entry contains the file identifier of the code file on the system disk. Each Name Table entry also has a specific defined function (for example, MCP or GISMO) and a condition (standard or experimental) for its selection by the CLEAR/START routine. These are shown in table 4-1.

Both the COLDSTART/TAPE and COLDSTART/DISK stand-alone utility programs construct the initial Name Table, and load and identify the following default files on the system disk:

Name Table Mnemonic	File Identifier
N	SYSTEM/INIT
G	GISMO
I	SDL2/INTERP
M	MCPII
MM	MCPII/MICRO-MCP
ODT	SYSTEM/ODT

These defaults are selected from the Name Table when a standard CLEAR/START operation is performed. If temporary changes to the operating environment have been specified, the CLEAR/START program overrides the default Name Table selections with the entries required by the environment specified.

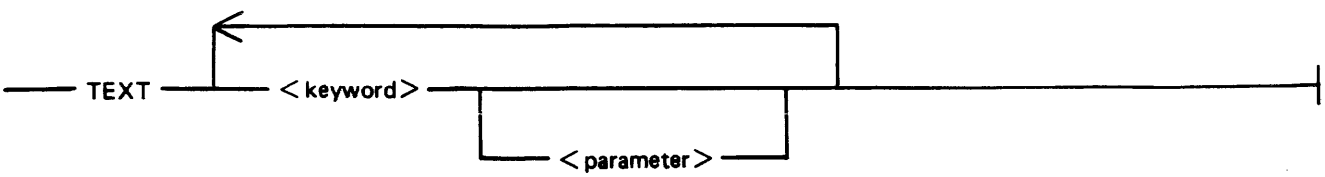
TEMPORARY ENVIRONMENT CHANGES

Several changes to the default selections made by the CLEAR/START routine can be specified. On B 1965/B 1995 systems these changes are made before entering CLEAR MTR GO [XMT] to begin the clear-start process. On other B 1000 systems, the changes are made after the bootstrap loading process halts with @AAAAAA@ in the L register.

B 1965/B 1995 Systems — Works with CMS Too!

Temporary environment changes for B 1965/B 1995 systems are made by using the Soft Panel command TEXT before the CLEAR MTR GO [XMT] entry.

Syntax:



<keyword> descriptions follow. <parameter> applies to the keywords DC, IC,. PM, and DD; which are discussed following the keyword descriptions.

Keyword	Function Requested
DM	Memory dump. Refer to the subsection entitled Supplementary Information Required With a Memory Dump for additional information.
DUMP	Same as DM.

Keyword	Function Requested
M	Select the MCP. (This is the default.)
MX	Select the experimental MCPII (MX entry), rather that the default MCP (M entry).
NX	Select the experimental System Initializer (NX entry), rather than the standard System Initializer (N entry).
IX	Select the experimental SDL2 Interpreter (IX entry), rather than the default SDL2 Interpreter (I entry).
GX	Select the experimental GISMO (GX entry), rather than the default GISMO (G entry).
MMX	Select the experimental Micro MCP (MMX entry), rather than the default Micro MCP (MM entry).
CX	Select the experimental Controller (CX entry), rather than the standard NDL Controller (C entry).
MCX	Select the experimental MCS (MCX entry) rather than the standard MCS program (MCS entry).
ODX	Select the experimental ODT (ODX entry), rather than the standard SYSTEM/ODT program (ODT entry).
IH	Enable debug halts in the System Initializer. For use by Burroughs software development personnel only.
AMC	Initiate the MCS program that is in the MCS Name Table entry if the AMCS option is reset. Do not initiate the MCS program if the AMCS option is set.
DC	Override the default selection of the system disk channel. Refer to the System Disk Channel Selection Override subsection for details.
IC	Delete I/O channels artificially. Refer to the I/O Channel Deletion subsection for details.
PM	Artificially reduce the system memory size. Refer to the Pseudo-memory Size Specification subsection for details.
DD	(B 1965/B 1995 systems only.) Change the disk drive unit order. See the Disk Drive Unit Order subsection for details.

The following example requests a memory dump and specifies the experimental MCP (MX entry):

```
TEXT DUMP MX [XMT]
```

Other B 1000 Systems

Changes to the default selections made by the CLEAR/START routine can be specified by entering parameters in certain registers after the bootstrap loading process completes with @AAAAAA@ in the L register during the clear-start process.

Register entries are made by using the REGISTER GROUP and REGISTER SELECT rotary switches to access the desired register, setting the appropriate bits by means of the 24 toggle switches, pressing the LOAD push button, and observing the pattern that appears in the 24 display lights associated with the toggles.

Changes to the system software and firmware that is selected by the CLEAR/START program, as well as a request for a memory dump, are specified by setting certain T register bits. Bit meanings follow (bit 0 is leftmost):

Bit	Function Requested
0	Memory dump. Refer to the following subsection entitled Supplementary Information Required With A Memory Dump for additional information.
1-3	Not used.
4	Select the experimental MCPII (MX entry), rather than the default MCPII (M entry).
5	Select the experimental System Initializer (NX entry), rather than the standard System Initializer (N entry).
6	Select the experimental SDL2 Interpreter (IX entry), rather than the default SDL2 Interpreter (I entry).
7	Select the experimental GISMO (GX entry), rather than the default GISMO (G entry).
8	Select the experimental Micro MCP (MMX entry), rather than the standard Micro MCP (MM entry).
9	Select the experimental Controller (CX entry), rather than the standard NDL Controller (C entry).
10	Select the experimental MCS (MCX entry), rather than the standard MCS program (MCS entry).
11	Select the experimental ODT (ODX entry), rather than the standard SYSTEM/ODT program (ODT entry).
12	Enable debug halts in System Initializer. For use by Burroughs software development personnel only.
13-15	Not used.
16	Initiates the MCS program that is in the MCS Name Table entry if the AMCS system option is reset. Does not initiate the MCS program if the AMCS option is set.
17-23	Not used.

The system disk channel, I/O channel deletion, and pseudo memory size can also be specified. Refer to the System Disk Channel Selection Override subsection, the I/O Channel Deletion subsection, and the Pseudo-Memory Size Specification subsection for details.

System Disk Channel Selection Override

The CLEAR/START program normally selects Electronics Unit Zero (EU 0) or Drive Zero of the highest-speed disk device present as the base systems disk. The selection hierarchy is as follows (from highest to lowest):

B 9470 Head-per-Track disk
Head-per-Track disk (other than B 9470)
Disk Pack

When two or more channels contain identical disk device types, the CLEAR/START program selects the lowest-numbered channel as the systems disk channel.

This default system disk selection can be overridden during the clear-start operation by using the TEXT DC command on B 1965/B 1995 systems, or by loading the X register on other B 1000 systems.

System disk selection is valid for the current clear-start operation only; that is, the default disk is always selected during a clear-start unless the override is invoked.

The syntax of the TEXT DC command is

```
TEXT DC x [XMT]
```

where x is a hexadecimal literal representing the desired system disk channel. For example, to specify channel 10, the TEXT command would be

```
TEXT DC A [XMT]
```

On other B 1000 systems, channel selection is made by selecting the X register and loading it during the intermediate halt of the clear-start process. The port and channel of the desired system disk channel are entered in the X register as follows:

Bits	Contents
0-16	Not used
17-19	Port number (must be 7)
20-23	Channel number

For example, to specify Port 7, channel 10, the X register would be set to:

```
@00007A@ (0000 0000 0000 0000 0111 1010)
```

I/O Channel Deletion

The ability is provided to artificially delete I/O devices (that is, to make certain channels appear unassigned to the system software) during the clear-start procedure. This feature is primarily of value to Burroughs Field Engineers when trying to isolate hardware malfunctions involving the I/O control subsystem. The specifications are made by entering the TEXT IC command on B 1965/B 1995 systems, or by loading the FA register on other B 1000 systems.

The syntax of the TEXT IC command is as follows:

TEXT IC xxxx [XMT]

The xxxx refers to four hexadecimal digits representing the channel specification.

On the other B 1000 systems, the FA register is loaded during the intermediate halt of the clear-start process. The FA register is divided into two groups, as follows:

Bits	Contents
0-15	Channel specification
16-23	Not used.

The channels to be deleted are specified by setting one or more of bits 0 through 14 of the channel specification. Bit 0 represents channel 0, bit 1 represents channel 1, and so forth. (Channel 15 cannot be deleted.)

As an example, the following value causes the CLEAR/START and SYSTEM/INIT programs to delete channels 2, 5, 7, and 12 (port 7 is always implied):

@2508@ (0010 0101 0000 1000)

For B 1965/B 1995 systems, the appropriate TEXT command to delete these channels is

TEXT IC 2508 [XMT]

For other B 1000 systems, the FA register would be set to

@250800@ (0010 0101 0000 1000 0000 0000)

Channels deleted during the CLEAR/START operating procedure appear unassigned to the MCP.

Pseudo-Memory Size Specification

The memory used on a system can be artificially reduced. This can be done by the TEXT PM command on B 1965/B 1995 systems, or by loading the LR register on other B 1000 systems.

The syntax of the TEXT PM command used in B 1965/B 1995 systems is

TEXT PM xxxxxx [XMT]

The x's refer to six hexadecimal digits, reflecting a hexadecimal value. The meaning of the value is explained next.

On the other B 1000 systems, the LR register is loaded during the intermediate halt of the clear-start process. The LR register is functionally divided into two portions, as follows:

Bit	Function
0-11	Hexadecimal value
12-23	Not used

The CLEAR/START program multiplies the value specified by 512 bytes to obtain the pseudo-size of the main memory. The following table of values depicts sample main memory sizes that might be specified:

Value	Main Memory Size	
@400000@	524,288 bytes	(0.5 MB)
@800000@	1,048,576 bytes	(1.0 MB)
@C00000@	1,572,864 bytes	(1.5 MB)

For example, to artificially set the main memory of a B 1965/B 1995 system to 524,288 bytes, the following TEXT command would be used:

TEXT PM 400000 [XMT]

To obtain the equivalent pseudo-memory size on other B 1000 systems, the LR register would be set to

@400000@ (0100 0000 0000 0000 0000 0000)

NOTE
Values larger than the actual physical size of main memory should not be specified.

Disk Drive Unit Order Selection

On B 1965/B 1995 systems only, the DSC can be programmed to change the order of the disk units. For example, DPD (unit 3) can be made to be DPA (unit 0). This is done with the TEXT DD command as follows:

TEXT DD xxxxxxxx [XMT]

Each of the eight x's stands for a digit from 0 through 7. From left to right, the x's represent the order of the disk units: leftmost is DPA, next is DPB, and so on. The default order is 01234567.

For example, to specify that unit 3 is to be DPA and unit 0 is to be DPD (that is, to interchange DPA with DPD) while leaving the remaining units as is, the following TEXT command is used:

TEXT DD 31204567 [XMT]

All eight digits must be specified, even if the system does not have eight drives on the DSC. The changing of the disk unit order is in effect for the current clear-start only; if a change is not specified upon another clear-start, the DSC reverts to the default order.

SUPPLEMENTARY INFORMATION REQUIRED WITH A MEMORY DUMP

If the system comes to an orderly halt, with the RUN and ERROR lights out (RUN light out, no Soft Panel ERROR indication on B 1965/B 1995 systems), then this usually means that the software halted the system. The L register defines the halt. (A list of system halts is available in section 8 of Volume 1 of the B 1000 Systems System Software Operation Guide.) Any relevant facts about the halt should be documented and given to the Burroughs Technical Representative with the dump that is taken.

If the RUN light is out and the ERROR indicator is on, register settings must be recorded. The halt should be treated as if a system hang had occurred and the HALT push button had been pressed, as is described in the following paragraphs. When ERROR is indicated, either the PERP register or the PERM register has a value indicating the cause of the halt.

Many system problems are defined to be hangs, meaning that the system is running (RUN light on) but no work is being completed. This situation is a loop; the system is repetitively executing an instruction sequence but not exiting from it.

Before attempting a clear-start operation, two tests must be tried and the results documented:

1. Determine whether ODT interaction is possible by attempting a simple system command such as MX or WT.

2. Press the INTRPT push button.

If the INTRPT push button halts the system (RUN light goes out), the L register displays @0D0010 or @000010@.

If the INTRPT push button fails to halt the system (RUN light stays on), it is extremely important to record the values of certain registers (for both processors in a dual-processor system) after the halt is achieved. The dump is almost always useless if it is submitted without register contents or with erroneous contents such as @FFFFFF@ in all registers, obtained because the system was still running.

Press the HALT push button to stop the system. (In B 1965/B 1995 systems, this is labeled HALT/RUN.)

In the rare instance that the HALT push button fails to stop the system (that is, the RUN light remains lit), press the HALT and CLEAR push buttons simultaneously. This halts the system. This situation reflects a processor problem and a Burroughs Field Engineer should be contacted. B 1965/B 1995 systems have no CLEAR push button but it is extremely unlikely that the HALT/RUN push button would fail to halt one of these systems.

Following are the registers of interest:

L, T, X, Y, A, FA, LR, CC, CD, PERM, PERP

On dual-processor systems, results must be recorded for each processor.

At this point, the operator can clear-start the system and take the memory dump previously described. After the clear-start operation, the dump should be "packaged" as soon as possible. This is done with the PM system command. (Refer to the B 1000 Software Operation Guide, volume 1.) This creates a packaged dumpfile labeled "DUMPFILE/PM" which can be printed or copied to another medium and given to the Burroughs Technical Representative, along with the supplementary information outlined previously.