B 1800/B 1700 DATA COMMUNICATIONS LINE ADAPTERS

TECHNICAL MANUAL VOLUME 1:

OPERATION and MAINTENANCE

Burroughs

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PREFACE

This manual provides information on line adapters used in B 1800/B 1700 data communication subsystems in conjunction with B 1800/B 1700 single-line and multi-line controls. Section 1, Function and Operation, and Section 2, Installation, are applicable to all B 1800/B 1700 line adapters.

Section 3, Documentation and Components, and Section 4, Maintenance Techniques, are dummy sections in this manual. Relevant information on these subjects is included in parallel sections of the Field Engineering Technical Manuals (FETMs) for the data communications controls.

Each of the sections from 5 through 13 provides theory of operation for one of the line adapters:

Section	Adapter
5	Standard Synchronous Line Adapter
6	Standard Asynchronous Line Adapter
7	Standard Direct Connect Line Adapter
8	Automatic Dial-Out Line Adapter
9	TTY Direct Asynchronous Line Adapter
10	TTY Asynchronous Line Adapter
11	Wideband Line Adapter
12	Binary Synchronous Line Adapter
13	Burroughs Direct Interface Line Adapter

SECTION 1
FUNCTION AND OPERATION

B 1800/B 1700 DATA COMMUNICATIONS SUBSYSTEMS

Figure 1-1 is a block diagram of the two basic data communications (data comm) subsystems used in B 1800/B 1700 systems.

Single-line subsystems are based on (1) the B 1800/B 1700 Single Line Control-1 (SLC-1), (2) the B 1800/B 1700 Single Line Control-2 (SLC-2), or (3) the Universal Single Line Control (SLC-3).

SLC-1, in its own 4-card backplane, can incorporate any one of the B 1800/B 1700 line adapters described in this manual, plus, optionally, a B 1800/B 1700 Automatic Dial-Out (ADO) line adapter. SLC-2 is used singly or in pairs in conjunction with a 6-card backplane (B 1800/B 1700 Dual Single Line Base-1). The SLC-2 configuration permits two line adapters to be used in the base, but excludes use of an ADO line adapter.

SLC-3, a 1-card unit, is the logical equivalent of SLC-1 plus any one of the line adapters described in this manual except those designated as TTY asynchronous and direct asynchronous, wideband, and automatic dial-out.

Multi-line subsystems are based on the B 1800/B 1700 Multi-Line Control-1 (MLC-1) or the B 1800/B 1700 Multi-Line Control-2 (MLC-2). MLC-1, in a 12-card backplane, can service any 8 line adapters. MLC-2, in an 8-card backplane, can service any 4 line adapters. In addition, the B 1800/B 1700 Multi-Line Extension-1 (MLE-1) can be connected to either MLC-1 or MLC-2, permitting the inclusion of up to 8 more line adapters, for a total of 12 line adapters in an MLC-2 subsystem or 16 line adapters in an MLC-1 subsystem. Two multi-line subsystems can be included in B 1835, B 1860, B 1865, or B 1870 systems.

COMMUNICATION LINES

B 1800/B 1700 data communications subsystems can service narrowband, voiceband, and wideband communication facilities.

Narrowband communication facilities provide bandwidths of up to 300 Hz. The transmission rate is usually either 150 or 300 baud. (Baud is defined here as bits per second). These facilities are either private or TELEX/TWX services.

Voiceband communication facilities provide a nominal bandwidth of 4 kHz and transmission rates of 600, 1200, 1800, and 2000 baud. These facilities are either private line or dial line. Specially conditioned private lines are used to provide transmission rates of 2400, 4800, and 9600 baud.

Wideband facilities, which provide bandwidths of 48 kHz and up and transmission rates 40,800 baud and higher, are generally private, but Bell Dataphone* 50, a dial service, is wideband.

Either multipoint or point-to-point service can be accommodated. Multipoint service implies a central processor and a single, non-switched communication line to which more than one data communication device is attached. Point-to-point service implies a pair of devices, usually the processor and a data communications device, connected to each other by either dedicated or switched lines.

*Registered service mark of AT&T Co.

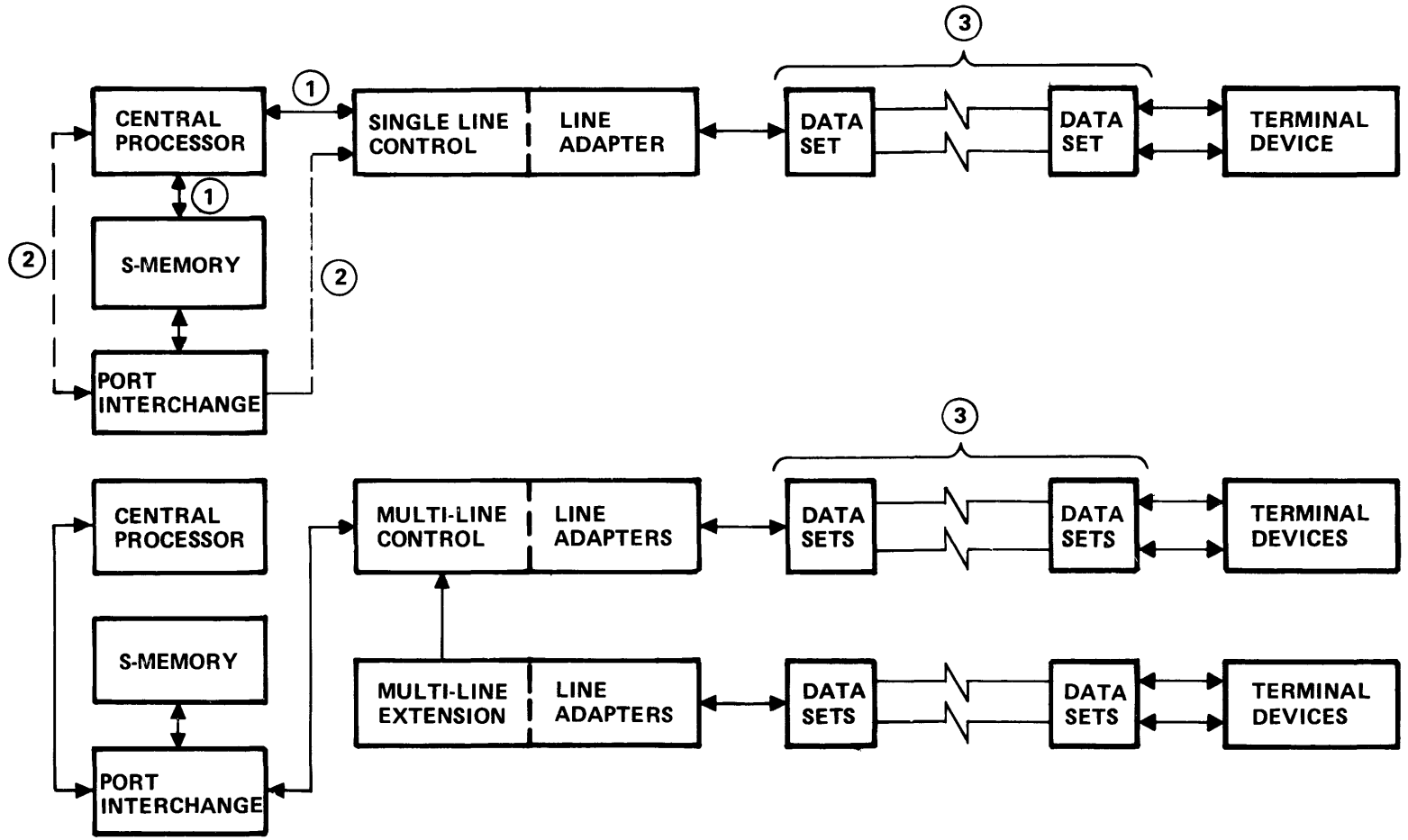


Figure 1-1. B 1800/B 1700 Data Communications Subsystems

LINE ADAPTER CHARACTERISTICS

Each line adapter described in this manual (except the ADO adapter; see section 8) has the following characteristics:

The entire adapter is contained on a single logic card.

The adapter operates in half-duplex mode.

The adapter is character oriented.

The adapter has provision for the accumulation of one full character.

The adapter performs character assembly and disassembly, timing comparison, block check character insertion and checking, and other logical operations.

Line adapters that use the RS-232-C interface can also be used with the RS-232-B interface but only to the extent of the correspondence between the interfaces.

Adapters designated as "standard" respond to Burroughs message protocol and, in general, are used with compatible data sets and terminals.

Adapters designated as "direct" do not require data sets; these adapters are connected directly to appropriate terminals.

The terms "synchronous" and "asynchronous" relate to the character formats acceptable to the line adapter. In synchronous transmission, data is synchronized with synchronization characters so that transmitter and receiver can determine message configuration. In asynchronous transmission, configuration is established by framing the 8-bit character with a start bit (SPACE) and one or two stop bits (MARK).

The character format for synchronous data communication consists of 8 equally-timed intervals representing 8 bits of information. (For 7-bit code structures the eighth bit provides parity; parity is odd.) Each character follows the preceding character; there is no interchange interval. The idle condition (no data on the line) is represented by a 1 (MARK).

The character format for asynchronous data communication consists of 10 equally-timed intervals. The first interval is a start bit equal to 0 (SPACE). The next seven intervals comprise the 7-bit character. Character parity (even) is carried in the ninth interval. The tenth interval is a stop bit equal to 1 (MARK).

DATA COMMUNICATIONS SOFTWARE

Software requirements for a B 1800/B 1700 data communications subsystem are listed below:

The Master Control Program (MCP).

The Software Development Language (SDL) compiler and interpreter.

The Central Service Module (CSM), which contains the I/O Driver program.

The associated application programs and, for any language other than SDL and UPL, the appropriate interpreter.

A Message Control System (MCS) program if the system contains certain multidrop configurations.

The Network Definition Language (NDL) compiler.

A network controller, generated by the NDL. The network controller:

- performs all application programs and the associated data communications input/output tasks,
- monitors and logs all I/O data communications messages and all exception conditions,
- services the communication lines and terminals, based on management priorities,
- provides automatic error recovery procedures and notification to the central processor of data communication errors,
- processes and supervises the message flow between the application programs and the data terminals.

The MCP provides dispatch operation through communication with the I/O Driver. (In single-line subsystems, the MCP also utilizes the I/O Driver for data and information flow.)

Application programs provide all output data to the subsystem and, in addition, generally provide the station identification number to the network controller.

TRANSMISSION CODES

The only codes used with B 1800/B 1700 data communication subsystems are (1) the American Standard Code for Information Interchange (ASCII) and (2) the Extended Binary Coded Decimal Interchange Code (EBCDIC).

The ASCII code used is the 7-bit version specified by the American National Standards Institute (ANSI) in 1967. EBCDIC, an 8-bit code, is used internally in B 1800/B 1700 systems. Translators within the data communications controls convert EBCDIC to ASCII on output and ASCII to EBCDIC on input.

For international applications, 7-bit character codes specified by the European Computer Manufacturers Association (ECMA), the International Standards Organization (ISO), and the International Committee on Telegraphy and Telephony (CCITT) can be accommodated.

Tables 1-1 and 1-2 define the EBCDIC/ASCII code correspondence. Table 1-1 is in EBCDIC sequence and shows all 256 codes. Table 1-2 is in ASCII sequence and presents the 128 ASCII-7 codes.

The columns in tables 1-1 and 1-2 contain the following information:

COLUMN A: EBCDIC sequence number and decimal value.

COLUMN B: EBCDIC hexadecimal representation.

COLUMN C: ASCII-7 sequence number and decimal value.

COLUMN D: ASCII-7 hexadecimal representation.

COLUMN E: Graphic or code.

"Hexadecimal representation" means that standard convention is followed for the 8-bit internal codes, which are presented as pairs of hexadecimal numbers that are translated as shown in the following examples:

Decimal Value	Hexadecimal Pair	Binary Pair	
		8 4 2 1	8 4 2 1
57	3/9	0 0 1 1	1 0 0 1
190	B/E	1 0 1 1	1 1 1 0
15	0/F	0 0 0 0	1 1 1 1

Control codes and special characters are discussed in the sections that follow the tables.

Table 1-1. B 1800/B 1700 Codes in EBCDIC Sequence

A	B	C	D	E	
0	0/0	0	0/0	NUL	(Null)
1	0/1	1	0/1	SOH	(Start of Heading)
2	0/2	2	0/2	STX	(Start of Text)
3	0/3	3	0/3	ETX	(End of Text)
4	0/4				
5	0/5	9	0/9	HT	(Horizontal Tab)
6	0/6				
7	0/7	127	7/F	DEL	(Delete)
8	0/8				
9	0/9				
10	0/A				
11	0/B	11	0/B	VT	(Vertical Tab)
12	0/C	12	0/C	FF	(Form Feed)
13	0/D	13	0/D	CR	(Carriage Return)
14	0/E	14	0/E	SO	(Shift Out)
15	0/F	15	0/F	SI	(Shift In)
16	1/0	16	1/0	DLE	(Data Link Escape)
17	1/1	17	1/1	DC1	(Device Control 1)
18	1/2	18	1/2	DC2	(Device Control 2)
19	1/3	19	1/3	DC3	(Device Control 3)
20	1/4				
21	1/5			NL	(New Line)
22	1/6	8	0/8	BS	(Backspace)
23	1/7				
24	1/8	24	1/8	CAN	(Cancel)
25	1/9	25	1/9	EM	(End of Medium)
26	1/A				
27	1/B				
28	1/C	28	1/C	FS	(File Separator)
29	1/D	29	1/D	GS	(Group Separator)
30	1/E	30	1/E	RS	(Record Separator)
31	1/F	31	1/F	US	(Unit Separator)
32	2/0				
33	2/1				
34	2/2				
35	2/3				
36	2/4				
37	2/5	10	0/A	LF	(Line Feed)
38	2/6	23	1/7	ETB	(End of Transm. Block)
39	2/7	27	1/B	ESC	(Escape)
40	2/8				
41	2/9				
42	2/A				
43	2/B				
44	2/C				
45	2/D	5	0/5	ENQ	(Enquiry)
46	2/E	6	0/6	ACK	(Acknowledge)
47	2/F	7	0/7	BEL	(Bell)

Table 1-1. B 1800/B 1700 Codes in EBCDIC Sequence (Cont.)

A	B	C	D	E	
48	3/0				
49	3/1				
50	3/2	22	1/6	SYN	(Synchronous Idle)
51	3/3				
52	3/4				
53	3/5				
54	3/6				
55	3/7	4	0/4	EOT	(End of Transmission)
56	3/8				
57	3/9				
58	3/A				
59	3/B				
60	3/C	20	1/4	DC4	(Device Control 4)
61	3/D	21	1/5	NAK	(Negative Acknowledge)
62	3/E				
63	3/F	26	1/A	SUB	(Substitute)
64	4/0	32	2/0		(Space)
65	4/1				
66	4/2				
67	4/3				
68	4/4				
69	4/5				
70	4/6				
71	4/7				
72	4/8				
73	4/9				
74	4/A	91	5/B	[	(left bracket)
75	4/B	46	2/E	.	(period, decimal point)
76	4/C	60	3/C	<	(less-than)
77	4/D	40	2/8	(	(left parenthesis)
78	4/E	43	2/B	+	(plus)
79	4/F	33	2/1	|	(vertical bar)
80	5/0	38	2/6	&	(ampersand)
81	5/1				
82	5/2				
83	5/3				
84	5/4				
85	5/5				
86	5/6				
87	5/7				
88	5/8				
89	5/9				
90	5/A	93	5/D	]	(right bracket)
91	5/B	36	2/4	$	(dollar sign)
92	5/C	42	2/A	*	(asterisk)
93	5/D	41	2/9	)	(right parenthesis)
94	5/E	59	3/B	;	(semicolon)
95	5/F	94	5/E	¬	(logical NOT)

Table 1-1. B 1800/B 1700 Codes in EBCDIC Sequence (Cont.)

A	B	C	D	E	
96	6/0	45	2/D	-	(minus, hyphen)
97	6/1	47	2/F	/	(slash)
98	6/2				
99	6/3				
100	6/4				
101	6/5				
102	6/6				
103	6/7				
104	6/8				
105	6/9				
106	6/A	124	7/C		
107	6/B	44	2/C	,	(comma)
108	6/C	37	2/5	%	(percent)
109	6/D	95	5/F	_	(underscore)
110	6/E	62	3/E	>	(greater-than)
111	6/F	63	3/F	?	(question mark)
112	7/0				
113	7/1				
114	7/2				
115	7/3				
116	7/4				
117	7/5				
118	7/6				
119	7/7				
120	7/8				
121	7/9	96	6/0		
122	7/A	58	3/A	:	(colon)
123	7/B	35	2/3	#	(number or pound sign)
124	7/C	64	4/0	@	(at sign)
125	7/D	39	2/7	'	(apostrophe)
126	7/E	61	3/D	=	(equal)
127	7/F	34	2/2	"	(quotation mark)
128	8/0				
129	8/1	97	6/1	a	
130	8/2	98	6/2	b	
131	8/3	99	6/3	c	
132	8/4	100	6/4	d	
133	8/5	101	6/5	e	
134	8/6	102	6/6	f	
135	8/7	103	6/7	g	
136	8/8	104	6/8	h	
137	8/9	105	6/9	i	
138	8/A				
139	8/B				
140	8/C				
141	8/D				
142	8/E				
143	8/F				

Table 1-1. B 1800/B 1700 Codes in EBCDIC Sequence (Cont.)

A	B	C	D	E	
144	9/0				
145	9/1	106	6/A	j	
146	9/2	107	6/B	k	
147	9/3	108	6/C	l	
148	9/4	109	6/D	m	
149	9/5	110	6/E	n	
150	9/6	111	6/F	o	
151	9/7	112	7/0	p	
152	9/8	113	7/1	q	
153	9/9	114	7/2	r	
154	9/A				
155	9/B				
156	9/C				
157	9/D				
158	9/E				
159	9/F				
160	A/0				
161	A/1	126	7/E	¢	(cents sign)
162	A/2	115	7/3	s	
163	A/3	116	7/4	t	
164	A/4	117	7/5	u	
165	A/5	118	7/6	v	
166	A/6	119	7/7	w	
167	A/7	120	7/8	x	
168	A/8	121	7/9	y	
169	A/9	122	7/A	z	
170	A/A				
171	A/B				
172	A/C				
173	A/D				
174	A/E				
175	A/F				
176	B/0				
177	B/1				
178	B/2				
179	B/3				
180	B/4				
181	B/5				
182	B/6				
183	B/7				
184	B/8				
185	B/9				
186	B/A				
187	B/B				
188	B/C				
189	B/D				
190	B/E				
191	B/F				
192	C/0	123	7/B	{	(left brace)
193	C/1	65	4/1	A	
194	C/2	66	4/2	B	
195	C/3	67	4/3	C	
196	C/4	68	4/4	D	

Table 1-1. B 1800/B 1700 Codes in EBCDIC Sequence (Cont.)

A	B	C	D	E	
197	C/5	69	4/5	E	
198	C/6	70	4/6	F	
199	C/7	71	4/7	G	
200	C/8	72	4/8	H	
201	C/9	73	4/9	I	
202	C/A				
203	C/B				
204	C/C				
205	C/D				
206	C/E				
207	C/F				
208	D/0	125	7/D	}	(right brace)
209	D/1	74	4/A	J	
210	D/2	75	4/B	K	
211	D/3	76	4/C	L	
212	D/4	77	4/D	M	
213	D/5	78	4/E	N	
214	D/6	79	4/F	O	
215	D/7	80	5/0	P	
216	D/8	81	5/1	Q	
217	D/9	82	5/2	R	
218	D/A				
219	D/B				
220	D/C				
221	D/D				
222	D/E				
223	D/F				
224	E/0	92	5/C	\	(reverse slash)
225	E/1				
226	E/2	83	5/3	S	
227	E/3	84	5/4	T	
228	E/4	85	5/5	U	
229	E/5	86	5/6	V	
230	E/6	87	5/7	W	
231	E/7	88	5/8	X	
232	E/8	89	5/9	Y	
233	E/9	90	5/A	Z	
234	E/A				
235	E/B				
236	E/C				
237	E/D				
238	E/E				
239	E/F				
240	F/0	48	3/0	0	
241	F/1	49	3/1	1	
242	F/2	50	3/2	2	
243	F/3	51	3/3	3	
244	F/4	52	3/4	4	
245	F/5	53	3/5	5	
246	F/6	54	3/6	6	
247	F/7	55	3/7	7	

Table 1-1. B 1800/B 1700 Codes in EBCDIC Sequence (Cont.)

A	B	C	D	E	
248	F/8	56	3/8	8	
249	F/9	57	3/9	9	
250	F/A				
251	F/B				
252	F/C				
253	F/D				
254	F/E				
255	F/F				
0	0/0	0	0/0	NUL	(Null)
1	0/1	1	0/1	SOH	(Start of Heading)
2	0/2	2	0/2	STX	(Start of Text)
3	0/3	3	0/3	ETX	(End of Text)
55	3/7	4	0/4	EOT	(End of Transmission)
45	2/D	5	0/5	ENQ	(Enquiry)
46	2/E	6	0/6	ACK	(Acknowledge)
47	2/F	7	0/7	BEL	(Bell)
22	1/6	8	0/8	BS	(Backspace)
5	0/5	9	0/9	HT	(Horizontal Tab)
37	2/5	10	0/A	LF	(Line Feed)
11	0/B	11	0/B	VT	(Vertical Tab)
12	0/C	12	0/C	FF	(Form Feed)
13	0/D	13	0/D	CR	(Carriage Return)
14	0/E	14	0/E	SO	(Shift Out)
15	0/F	15	0/F	SI	(Shift In)
16	1/0	16	1/0	DLE	(Data Link Escape)
17	1/1	17	1/1	DC1	(Device Control 1)
18	1/2	18	1/2	DC2	(Device Control 2)
19	1/3	19	1/3	DC3	(Device Control 3)
60	3/C	20	1/4	DC4	(Device Control 4)
61	3/D	21	1/5	NAK	(Negative Acknowledge)
50	3/2	22	1/6	SYN	(Synchronous Idle)
38	2/6	23	1/7	ETB	(End of Transm. Block)
24	1/8	24	1/8	CAN	(Cancel)
25	1/9	25	1/9	EM	(End of Medium)
63	3/F	26	1/A	SUB	(Substitute)
39	2/7	27	1/B	ESC	(Escape)
28	1/C	28	1/C	FS	(File Separator)
29	1/D	29	1/D	GS	(Group Separator)
30	1/E	30	1/E	RS	(Record Separator)
31	1/F	31	1/F	US	(Unit Separator)
64	4/0	32	2/0		(space)
79	4/F	33	2/1	|	(vertical bar)
127	7/F	34	2/2	"	(quotation mark)
123	7/B	35	2/3	#	(number or pound sign)
91	5/B	36	2/4	$	(dollar sign)
108	6/C	37	2/5	%	(percent)
80	5/0	38	2/6	&	(ampersand)
125	7/D	39	2/7	'	(apostrophe)
77	4/D	40	2/8	(	(left parenthesis)
93	5/D	41	2/9	)	(right parenthesis)
92	5/C	42	2/A	*	(asterisk)
78	4/E	43	2/B	+	(plus)
107	6/B	44	2/C	,	(comma)
96	6/0	45	2/D	-	(minus, hyphen)

Table 1-2. B 1800/B 1700 Codes in ASCII Sequence

A	B	C	D	E	
75	4/B	46	2/E	.	(period)
97	6/1	47	2/F	/	(slash)
240	F/0	48	3/0	0	
241	F/1	49	3/1	1	
242	F/2	50	3/2	2	
243	F/3	51	3/3	3	
244	F/4	52	3/4	4	
245	F/5	53	3/5	5	
246	F/6	54	3/6	6	
247	F/7	55	3/7	7	
248	F/8	56	3/8	8	
249	F/9	57	3/9	9	
122	7/A	58	3/A	:	(colon)
94	5/E	59	3/B	;	(semicolon)
76	4/C	60	3/C	<	(less-than)
126	7/E	61	3/D	=	(equal)
110	6/E	62	3/E	>	(greater-than)
111	6/F	63	3/F	?	(question mark)
124	7/C	64	4/0	@	(at sign)
193	C/1	65	4/1	A	
194	C/2	66	4/2	B	
195	C/3	67	4/3	C	
196	C/4	68	4/4	D	
197	C/5	69	4/5	E	
198	C/6	70	4/6	F	
199	C/7	71	4/7	G	
200	C/8	72	4/8	H	
201	C/9	73	4/9	I	
209	D/1	74	4/A	J	
210	D/2	75	4/B	K	
211	D/3	76	4/C	L	
212	D/4	77	4/D	M	
213	D/5	78	4/E	N	
214	D/6	79	4/F	O	
215	D/7	80	5/0	P	
216	D/8	81	5/1	Q	
217	D/9	82	5/2	R	
226	E/2	83	5/3	S	
227	E/3	84	5/4	T	
228	E/4	85	5/5	U	
229	E/5	86	5/6	V	

Table 1-2. B 1800/B 1700 Codes in ASCII Sequence (Cont.)

A	B	C	D	E	
230	E/6	87	5/7	W	
231	E/7	88	5/8	X	
232	E/8	89	5/9	Y	
233	E/9	90	5/A	Z	
74	4/A	91	5/B	[	(left bracket)
224	E/0	92	5/C	\	(reverse slash)
90	5/A	93	5/D	]	(right bracket)
95	5/F	94	5/E	¬	(logical NOT)
109	6/D	95	5/F	_	(underscore)
121	7/9	96	6/0		
129	8/1	97	6/1	a	
130	8/2	98	6/2	b	
131	8/3	99	6/3	c	
132	8/4	100	6/4	d	
133	8/5	101	6/5	e	
134	8/6	102	6/6	f	
135	8/7	103	6/7	g	
136	8/8	104	6/8	h	
137	8/9	105	6/9	i	
145	9/1	106	6/A	j	
146	9/2	107	6/B	k	
147	9/3	108	6/C	l	
148	9/4	109	6/D	m	
149	9/5	110	6/E	n	
150	9/6	111	6/F	o	
151	9/7	112	7/0	p	
152	9/8	113	7/1	q	
153	9/9	114	7/2	r	
162	A/2	115	7/3	s	
163	A/3	116	7/4	t	
164	A/4	117	7/5	u	
165	A/5	118	7/6	v	
166	A/6	119	7/7	w	
167	A/7	120	7/8	x	
168	A/8	121	7/9	y	
169	A/9	122	7/A	z	
192	C/0	123	7/B	{	(left brace)
106	6/A	124	7/C		
208	D/0	125	7/D	}	(right brace)
161	A/1	126	7/E	¢	(cents sign)
7	0/7	127	7/F	DEL	(Delete)

CONTROL CODES AND SPECIAL CHARACTERS

Certain ASCII and EBCDIC characters or combinations of characters are used as data communication control codes or special characters. These characters are used to specify various data communications operations. Their placement within messages is determined by the line discipline under which the line adapter and the terminal devices operate. All these characters are available for use with any line adapter that responds to the specified line discipline; the character set used by each line adapter is listed in the section of this manual that covers that adapter. Some of these characters are used both by software and hardware.

Table 1-3 lists all control and special characters and identifies them as valid (X) in ASCII, EBCDIC or both. The paragraphs that follow identify, define, and describe all the control and special characters used in B 1800/B 1700 data communication subsystems.

Control Codes

ACK (Acknowledgement)

ACK is an affirmative response to either a normal selection, indicating ready-to-receive, or to a transmission, indicating message-accepted. As an affirmative response to a selection, ACK may be preceded by station identification, the special characters AD1 and AD2 (Address 1 and Address 2), or other information such as a reply number. (The affirmative response to a poll is the transmission of a message.)

ACK0/ACK1 (Affirmative Acknowledgement)

The ACK0 and ACK1 characters, in proper sequence, indicate that the previous block was accepted without error and that the receiver is ready to accept the next block of the transmission. ACK0 is the positive response to selection (multipoint) or line bid (point-to-point). ACK0 and ACK1 are used in alternation as affirmative replies, providing a sequential checking control for a series of replies and making it possible to maintain a running check to ensure that each reply corresponds to the immediately preceding message block. (The affirmative response to a poll is the transmission of a message.)

Individually, ACK0 and ACK1 are 2-character control sequences. For ACK0, the sequence is DLE 7 and for ACK1, it is DLE 6.

Table 1-3. Control Codes and Special Characters

Control Codes			Special Characters		
Characters	**ASCII**	**EBCDIC**	**Characters**	**ASCII**	**EBCDIC**
ACK	X	-	AD1 AD2	X	-
ACK0/ACK1	-	X	BL#	X	-
BCC	X	-	BSL	X	-
DEOT	X	X	CON	X	-
DLG	X	X	CRC16	-	X
ENQ	X	X	FSL	X	-
EOT	X	X	GSL	X	-
ETB	X	X	PAD	-	X
ETX	X	X	POL	X	X
ITB	-	X	SEL	X	X
NAK	X	X	SEQ	X	-
RVI	-	X	XM#	X	-
SOH	X	X			
STX	X	X			
SYN	X	X			
TTD	-	X			
WACK	-	X			

X = Valid

BCC (Block Check Character)

BCC is a redundant control sequence that is added to the end of a transmission block for the purpose of error detection and control. This character is formed by creating a binary sum (without carry) on each of the seven bits of the transmitted characters that follow SOH (or STX if there is no SOH), including ETB or ETX but excluding any SYN (synchronous idle) characters. The BCC parity bit must be the same as that of the text characters (odd or even). BCC immediately follows ETB or ETX in a transmission block.

DEOT (Mandatory Disconnect)

DEOT is a communication control sequence (DLE EOT) used to signal that a disconnect of a switch circuit must be initiated.

DLE (Data Link Escape)

DLE changes the meanings of a limited number of immediately following contiguous characters. These characters then become supplementary data transmission control functions. Only graphics and transmission control characters are used in DLE sequences.

ENQ (Enquiry)

ENQ is a request for a response of station status or for a retransmission of control characters. This control character is used as either the final character of a poll or as a response from the other station on a select.

EOT (End of Transmission)

EOT indicates the conclusion of a communication sequence. Receipt of EOT sets the terminal into a control state, waiting for a poll, select, or contention sequence. The EOT can be transmitted by a master station to abort a transmission sequence. To assure that terminals are in a control state, EOT can precede a communication control sequence. The EOT is transmitted by a remote terminal as a "no-traffic" response to a poll.

ETB (End of Transmission Block)

ETB indicates the end of a data block in either headings or text, and may be used to segment a long message into smaller transmission blocks. The heading or text resumes after transmission of a block number followed by SOH or STX. The use of ETB requires a reply that indicates the status of the receiving station.

ETX (End of Text)

ETX indicates the end of a contiguous flow of characters identified as text. ETX requires a reply that provides the status of the receiving station.

ITB (End of Intermediate Transmission Block)

ITB is a control sequence that enables a message (heading or text) to be segmented for error checking purposes without causing reversal of transmission direction. The BCC character immediately follows ITB and resets the block-check count. After the first intermediate block containing text, successive intermediate blocks need not be preceded by STX or SOH. (For transparent data, each successive intermediate block must begin with DLE STX).

Normal line turnaround occurs after the last intermediate block that is terminated by ETB or ETX (DLE ETB or DLE ETX in transparent mode). When one of these ending characters is received, the receiving station responds to the entire transmission. If a BCC error is detected for any of the intermediate blocks, a negative reply is sent, requiring retransmission of all intermediate blocks. All binary synchronous stations must have the ability to receive ITB character as a station option.

NAK (Negative Acknowledgement)

NAK is a negative response to (1) a normal selection, indicating the responder is not ready to receive, (2) a transmission, indicating character parity failure for any character of a block, or (3) a BCL error or a block number sequence check failure. The NAK may be preceded by station identification, AD1 AD2, or other information such as a reply number. NAK is also used as a response to the EBCDIC control character TTD.

RVI (Reverse Interrupt)

RVI is a control sequence that consists of the DLE character followed by the "at" sign (@; EBCDIC 7/C). RVI, a positive response used in place of the ACK0 or ACK1 positive acknowledgement, is transmitted by the receiving station to request termination of the current transmission because a high-priority message must be transmitted to the sending station. In a multipoint environment, the control station, acting as a receiver, can use RVI to communicate with another station on the line. Successive RVIs cannot be transmitted, except in response to ENQ. The sending station interprets the RVI as a positive acknowledgement and responds by transmitting all the available data. More than one block transmission can be required to transmit all data in response to RVI.

The ability to receive RVI is mandatory for all binary synchronous stations, but the ability to transmit RVI is optional.

SOH (Start of Heading)

SOH is required only when a heading is to be sent on a transmission. When used, SOH is the first of a sequence of characters that form the heading. This sequence also can contain terminal identification (AD1 AD2) and may contain other information pertinent to the transmission, such as a transmission number (XM#). A heading is ended by STX.

STX (Start of Text)

STX ends a heading and precedes a sequence of characters that form the text of the transmission.

SYN (Synchronous Idle)

The synchronizing pattern for establishing character phase consists of at least two contiguous SYN characters. If more than two are sent, the sync pattern ends with the last transmitted SYN.

Character phase must be re-established for each transmission. This is accomplished when the receiving station recognizes at least two contiguous SYN characters in the bit stream. Character phase remains established at the receiving station until (1) a line-turnaround character is received, (2) an end-of-transmission character is received, or (3) a time-out occurs.

To provide and monitor for synchronization during transmission of the message, additional sync patterns must be inserted in the message by the transmitter. The sync-idle sequence is required in heading or text data at 1-second intervals. For normal mode of operation, two sync characters are inserted at least once per second. For transparent mode, a DLE SYN character is inserted at least once per second.

This synchronizing technique permits receiving stations to verify that they are in step with the transmitting station. Sync-idle characters are not included in the BCC accumulation, and are stripped from the message at the receiving station.

TTD (Temporary Text Delay)

The TTD control sequence is sent by a sending station in message transfer state when the station wants to retain the line, but is not ready to transmit. The TTD control sequence (STX ENQ) is normally sent after approximately 2 seconds if the sending station is not capable of transmitting the next text block or initial text block within that time. This 2-second time-out avoids the nominal 3-second receive time-out at the receiving station.

The receiving station responds to the TTD sequence with a NAK and waits for transmission to begin. If the sending station is still not ready to transmit, the TTD sequence can be repeated one or more times.

This delay in transmission can occur when the sending station's input device has not completely filled the buffer. The TTD is also transmitted by a sending station in message-transfer mode to indicate to the receiver that the current transmission is being aborted.

After receiving NAK as a response to the TTD sequence, the sending station sends EOT, resetting the stations to control mode (forward abort).

WACK (Wait Before Transmitting Positive Acknowledgement)

WACK is a 2-character control sequence. The first character is a DLE, the second character is EBCDIC 6/B (comma). WACK allows a receiving station to indicate "temporarily not ready to receive" to the transmitting station and can be sent as (1) a response to a text or heading block selection sequence (multipoint), (2) line bid (point-to-point with contention), or (3) an identification (ID) line bid sequence (switched network). WACK is a positive acknowledgement of the received data block or selection.

The normal transmitting station response to WACK is ENQ; however, EOT is also a valid response (DLE EOT in the transparent mode). The ability the receive WACK is mandatory for all binary synchronous stations, but the ability to transmit WACK is optional.

Special Characters

AD1 AD2 (Address 1 Address 2)

AD1 AD2 special character, a 2-character address established as the address of a device or a terminal, is used to address a terminal in polling or selection sequence or, in the message heading, to identify the terminal from which a message is transmitted. AD1 AD2 may also be used as an identification prefix to indicate that a terminal is ready to receive a message or as identification for a station that transmits a NAK. On receipt of a message, the receiving station may use AD1 AD2 to verify that the message originated at the polled terminal. For broadcast, AD1 AD2 identifies the terminal that is to acknowledge receipt of the message.

AD1 AD2 may be represented by any pair of ASCII characters from 2/10 to 7/F or any pair of EBCDIC characters from 4/0 to F/F. However, the DLE character, though present in both sets, may not be used.

In systems for which terminal-to-terminal (downstream) communication is precluded, AD1 AD2 in the header transmitted by the central processor may be defined to represent the terminal address and is used for address checking.

AD1 can be used as a station address, with the accompanying AD2 used to identify a terminal at that station.

BSL (Broadcast Select)

The BSL character specifies "this is a broadcast message." It is sent to all stations. In the broadcast sequence, AD1 AD2 identifies the station which acknowledges receipt of the message. BSL is followed immediately by a transmission block without requiring acknowledgement of the selection. BSL is represented by ASCII 7/4 (t).

BL# (Block Number)

The BL# character can be used when data must be subdivided into separate units for transmission. It consists of a 2-character sequence that identifies the sequential block number in a blocked message.

The BL# character is represented by pairs of ASCII characters:

Block Number	Character Pair
0 (BL0)	DLE p
1 (BL1)	DLE q
2 (BL2)	DLE r
3 (BL3)	DLE s
4 (BL4)	DLE t
5 (BL5)	DLE u
6 (BL6)	DLE v
7 (BL7)	DLE w

CON (Contention)

The CON character instructs all receiving terminals to go to contention mode of operation. Two NUL characters replace AD1 AD2 in the contention sequence. There is no acknowledgement of the contention instruction. The CON character is represented by ASCII 0/7 (BEL).

CRC-16 (Cyclic Redundancy Character)

CRC-16, a 16-bit redundant character, is added to the end of a transparent transmission block for error detection and control. All characters following STX or SOH (except SYN and the first DLE of a DLE DLE sequence) are included in the CRC accumulation.

A cyclic redundancy check is a division performed by both the transmitting station and the receiving station, using the binary value of the message as a dividend and the constant given below as the divisor:

$$X^{16} + X^{15} + X^2 + 1$$

The quotient is discarded and the remainder serves as the check character, which is transmitted immediately following a checkpoint character (ITB, ETB, or ETX) as the block check character. The receiving station compares the transmitted remainder to its own computer remainder; if equal, no error condition exists.

FSL (Fast Select)

The FSL character specifies "this is a fast select," in a selection sequence transmitted by the central computer. The FSL is represented by ASCII 7/3 (s). FSL is followed immediately by a transmission block; acknowledgement of the selection is not required.

GSL (Group Select)

The GSL character specifies "this is a message for a group of stations". In the group select sequence, AD1 AD2 identifies the station which acknowledges receipt of the message. The GSL is followed immediately by a transmission block; acknowledgement of selection is not required. GSL may be represented by any agreed-on ASCII character in the range 2/0 through 6/F.

PAD Characters

All binary synchronous stations add a PAD character following any response code, BCC, or ETX, on all transmissions to ensure that the last character of the transmission is properly transmitted by the data set. The line adapter also transmits a PAD character after each ending code in lieu of BCC if the start code is not received. The PAD character consists of eight ones (F/F). Although eight bits of the trailing PAD character are sent, the receiver checks only the first four bits. The ability to receive PAD is optional.

POL (Poll)

The POL character specifies "do you have a message to send?" POL precedes ENQ in a polling sequence. For ASCII, POL is represented by 7/0 (p); for EBCDIC, POL may be represented by 9/7 (p) or by any agreed-on character in the range 4/0 through F/F.

SEL (Select)

The SEL character specifies "I have a message for you." SEL precedes ENQ in a selection sequence. SEL is represented by ASCII 7/1 (q) or by EBCDIC 9/8 (q) or any agreed-on EBCDIC character in the range 4/0 through F/F

SEQ (Sequential Select)

The SEQ character indicates that a group of remote terminals is being selected to receive a message addressed to that group. The last terminal selected in the group acknowledges receipt of SEQ. SEQ is represented by ASCII 7/2 (r) and is followed by the AD1 AD2 of another terminal. When this option is employed, AD1 AD2 must not be represented by any ASCII character in the range 7/0 through 7/F.

XM# (Transmission Number)

The XM# is used to identify transmission from or transmissions to a terminal. This character may also be used as part of a message header to assist in message recovery. Each digit of XM# is represented by an ASCII character in the range 2/0 through 6/F. One to three digits may be used. The XM# sequences used for broadcast cannot be the same as the sequences used for group addressed messages.

MESSAGE STRUCTURES

The structure of a data communication message is determined by the mode of operation of the data communication subsystem and the line discipline that is used.

In multipoint service, either poll/select or a modified contention mode of operation may be used. In point-to-point service, the modes of operation are conversational or contention.

The following terms are fundamental in discussions of message structures:

CONTROL:
The device that controls the data communications network. This is usually a central processor.

MESSAGE:
A message is all the information that is moved across a line. A message includes control and special characters, headings, and text.

MASTER:
The device that transmits the information constituting the messages.

SLAVE:
A device that is controlled by a master.

Standard Adapters

The following illustrates message structures for standard adapters. Multipoint service poll/select structures are followed by point-to-point service formats.

Multipoint (Poll/Select)

Standard message:
STX text ETX BCC

Standard message with heading:
SOH heading STX text ETX BCC

Poll:
EOT AD1 AD2 POL ENQ

Select:
EOT AD1 AD2 SEL ENQ

Fast select:
EOT AD1 AD2 FSL SOH heading STX text ETX BCC

Acknowledgement: (Message received, ready for new message.)
ACK

Negative acknowledgement: (Not ready for new message; received message had error receiver is busy.)
NAK

End of transmission: (Reply from receiving device that it received the last positive acknowledgement and has no message to send.)
EOT

Point-to-Point

Standard message:
STX text ETX BCC

Standard message with heading:
SOH heading STX text ETX BCC

Enquiry: (Control character for a device requesting the use of the line.)
ENQ

Acknowledgement: (Message received, ready for new message.)
ACK

Negative acknowledgement: (Not ready for new message; received message had error receiver is busy.)
NAK

End of transmission: (Reply from receiving device that it received the last positive acknowledgement and has no message to send.)
EOT

Poll/Select

Poll

The purpose of the poll message is to determine if the slave is ready to transmit; the slave must receive a poll before beginning transmission. The poll message starts with EOT, is followed by the address of the terminal (AD1 AD2) and the poll character (POL = p), and is terminated with ENQ. The EOT may be the termination of a previous transmission sequence. To minimize the effect of noise, the polling sequence can immediately follow EOT.

If the slave does not receive or recognize an EOT followed by an address (AD1 AD2), it does not respond to the poll message. This no-response condition causes a timeout at the master. The master programmatically repolls a given number of times; the number of retries is determined by the NDL program.

If the slave does not have data to send when it is polled, it transmits an EOT as a response to the poll. An error condition exists if the master receives something other than data, EOT, or timeout as a response to a poll. The decision as to whether the data is valid or invalid is based on a valid slave address, character parity, and correct BCC. Message content, transaction codes, or account numbers for example, do not affect this decision. If the slave receives a message for which the character parity, block check, or address validity fails, a NAK is transmitted. A NAK received from a slave is interpreted by the master as a request to repeat the transmission.

An ACK response to a data message indicates that the message has been received properly (good parity and correct BCC). The master responds with EOT, which completes the polling cycle.

Select

The select message is sent by the master to determine if a slave is ready to receive a message from the master. The first character in the select message is an EOT, followed by the address of the slave (AD1 AD2), followed by the select character (ASCII 7/1=q) and terminated by ENQ. EOT may also be the termination of a previous transmission sequence; to minimize the effect of noise, the selection sequence can follow immediately. When the slave does not receive or recognize an EOT followed by the address (AD1 AD2), it does not respond to the select message. This "no response" condition causes a timeout at the master.

Time-out at the master is caused by the failure of the slave to respond to a select message either with ACK or NAK. The master programmatically reselects the device in a manner determined by the NDL program.

If the slave is not ready to receive, as indicated by the transmission of NAK, the master normally retries the selection of the slave in proper sequence; however, the selection sequence may be retransmitted immediately.

An error condition exists if the master receives a response other than ACK, NAK, or time-out in response to a select message. The master programmatically reselects the device in a manner specified in the NDL program.

ACK in response to a select message indicates that the slave is a receive-ready status. The master then transmits the data message to the slave. If the master does not receive a response (ACK or NAK), it times out and programmatically retransmits the data. If an error occurs, the message is retained by the master for transmission on the next selection sequence to that slave.

If character parity, block check, or slave identification are not validated, the slave transmits a NAK. The master retransmits the data on the next selection sequence to that slave. An error condition exists if the master receives other than an ACK, NAK, or time-out response to a data message.

A slave's response to a data message with an ACK is an indication that the message was received properly (valid character parity, slave address, and BCC). The master responds with EOT (which may be the beginning of another select or poll message) to complete the select cycle. Receipt of ACK by the master indicates normal completion of the select cycle. It is the option of the master to initiate another select or another line discipline at this time. At this point the slave can check for another control character such as POL, FSL, BSL, or GSL, since the format of these messages (up to the FSL, BSL, or GSL character) is the same as the select message. The decision that data is good or bad is based on a valid slave address, character parity, and BCC. Message content (transaction codes or account numbers, for example) does not affect this decision.

Fast Select

Fast selection is used when the central system needs to send a message to a terminal without first testing to make sure that the terminal is ready to receive. In such cases, the selection and the message are transmitted together. The ACK response from the terminal applies both to the select and to the successful message transfer. A NAK response indicates (1) the terminal is not ready to receive, or (2) invalid parity, or (3) block check exists. The fast select consists of an EOT, AD1 AD2, FSL, SOH, or STX, followed by either the heading then the message, or the message alone. The EOT may be the termination of a previous transmission sequence. To minimize the effect of noise, the fast select sequence follows immediately.

If the slave does not receive or recognize an EOT followed by its address (AD1 AD2), the slave does not respond to the fast select message. This no-response condition causes a time-out at the master.

An ACK response indicates that the slave was receive-ready and that the message was received properly; that is, character parity and BCC were valid. The master next transmits an EOT, which can be the beginning of another select or poll message, to complete the fast select cycle.

Receipt of ACK by the master indicates normal completion of the fast select cycle. It is the option of the master to initiate another fast select, or a different line discipline, at this time.

If the slave is not receive-ready, or if character parity, block-check, or slave identification are invalid, the slave sends a NAK to the master. The master retransmits the data on the next selection sequence to that slave.

An error condition exists if the master receives something other than an ACK, NAK, or time-out response to a fast select message. The master programmatically reselects on the next selection sequence to that slave. At this point, the slave checks for other control characters such as POL, SEL, BSL, or GSL, since the format of these messages (up to this character) is the same as the format of the fast select message. Determination of data validity is based on valid character parity, BCC, and slave identification; message content (transaction codes, account numbers, for example,) does not affect this decision. Even if a message is to be discarded, the slave must wait for reception of the entire message before responding with NAK.

Point-to-Point

Point-to-point operation implies that there are only two stations using a communications line to establish the link. The line can be either dedicated or switched. There are two modes of operation with point-to-point communications: (1) contention mode and (2) conversational mode.

Contention Mode

The contention mode provides that either station may bid for the use of the line to transmit a message. A station requests the line by transmitting the ENQ control character. If the other station is busy, it replies with a NAK; if it is ready to receive, the message, it replies with an ACK. On receiving the ACK, the station that initiated the ENQ sends the message. If no errors occur, the receiving station returns an ACK at the completion of the message. Then, the original sending station sends another message or an EOT control character. EOT in this situation indicates that ACK has been received from the receiving station and that there are no more messages from that station at this time.

Figure 1-2 shows the basic format of this interchange between two stations.

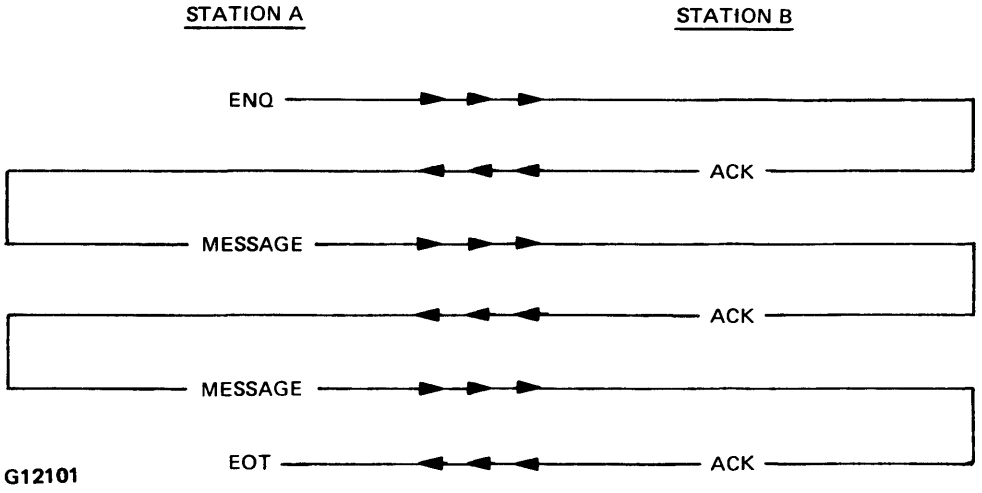


Figure 1-2. Message Interchange STD Adapters, Contention

Conversational Mode

Conversational mode, like contention mode, implies that there are only two stations using a communications line. The line can be either dedicated or switched. In the conversational mode, the initiating station transmits ENQ and waits for ACK from the receiving station. Upon receiving ACK, the original station sends a message. The receiving station responds to the message by returning a message. This interchange of messages continues until one of the stations has no additional messages to send. This station then sends ACK as its response to the last message from the other station. Discontinuation of the conversational model is accomplished by sending an ending-code message.

Figure 1-3 shows the basic format.

Binary Synchronous and Wideband Adapters

Common message structures (poll/select, point-to-point, and transparent mode) for binary synchronous and wideband adapters are illustrated in following paragraphs. Message formatting for these adapters requires the use of EBCDIC control characters, including some special characters that are preceded by the DLE character. These adapters can be used in either multipoint or point-to-point environments. Multipoint requires either poll/select or modified contention mode of operation. Point-to-point requires conversational mode and/or contention mode.

BISYNC Adapter Multipoint Poll/Select Formats

Standard message:
SYN SYN STX text ETX BCC PAD

Standard message with heading:
SYN SYN SOH heading STX text ETX BCC PAD

Abort heading:
SYN SYN SOH heading ENQ

Abort heading and message:
SYN SYN SOH heading STX text ENQ PAD

Standard message in blocks:
SYN SYN SOH heading STX text ETB BCC STX text ETX BCC PAD

Poll:
SYN SYN EOT AD1 AD2 POL ENQ PAD

Select:
SYN SYN EOT AD1 AD2 SEL ENQ PAD

Fast select:
SYN SYN EOT AD1 AD2 FSL SOH heading STX text ETX BCC PAD

Message received; ready: (Ready for new message.)
SYN SYN ACK

Message received; not ready: (Busy, or error in received message.)
SYN SYN NAK

Message received; none to send:
SYN SYN EOT

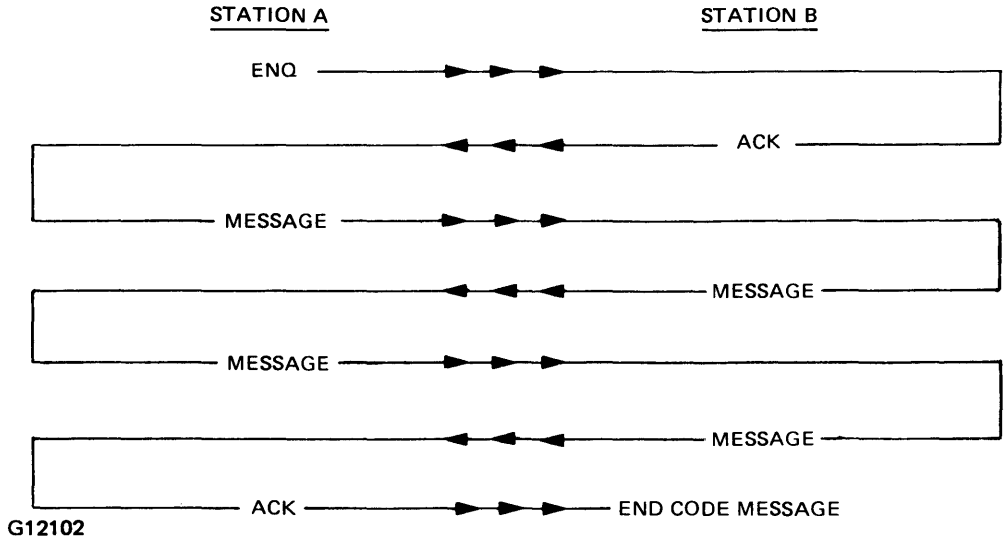


Figure 1-3. Message Interchange STD Adapters, Conversational

BISYNC Point-to-Point Formats

Standard message:
SYN SYN STX text ETX BCC PAD

Standard message with heading:
SYN SYN SOH heading STX text ETX BCC PAD

Request for line:
SYN SYN ENQ

Message received; ready: (Ready for new message.)
SYN SYN ACK

Message received; not ready: (Busy, or error in received message.)
SYN SYN NAK

Message received; none to send:
SYN SYN EOT

BISYNC Transparent Mode Formats

Message Sequence (read down)	
SYN	
SYN	
SOH	
heading	
DLE*	
STX*	Start transparent mode
text*	
DLE*	identifier for special character (inserted by line adapter)
DLE*	DLE character in text
text*	
DLE*	identifier for special character (inserted by line adapter)
SYN*	synchronization signal (inserted by line adapter)
text*	
DLE*	
ETX*	Stop transparent mode
BCC	
PAD	

* in transparent mode

Normal Text Structure

For accuracy and efficiency, text is transmitted in blocks. A message may include no text or one or more blocks of text. Each block is preceded by STX (start of text) for identification. Each text block except the last one is immediately followed by either ETB (end of transmission block) or ITB (end of intermediate transmission block). The last text block is followed by ETX (end of text).

A block of text may be preceded by a heading, which is a block of data starting with SOH (start of heading) and containing one or more characters that can be used for message control purposes such as message identification routing, and priority. The SOH initiates BCC (block check character) accumulation. (The initial SOH is not included in the accumulation.) A heading block, which can be of fixed or variable length depending on the specific terminals and applications, is terminated by the STX that precedes text.

Only the first SOH or STX in a transmission block that follows a line turnaround causes the BCC to reset. All succeeding STX or SOH characters (until a line turnaround) are included in the BCC. This permits the entire transmission (excluding the first SOH or STX and all SYN characters inserted in the message by the adapter) to be block checked.

Control characters or control sequences within a block of text (with the exception of SYN characters) are not allowed. If a control character is encountered, the station treats it as data and waits for the block check character (BCC) to detect a possible error. If an error is detected, the transmission is treated as invalid data. A text block can be terminated prematurely by means of an ENQ character, which signals the receiver to disregard the block in which it occurs.

Transparent Text Structure

The transparent mode expands the range of coded data that can be transmitted because all data, including the normally restricted control characters, is treated as patterns of bits when transmitted. For this reason, coding of data is unrestricted.

Unrestricted coding is particularly useful for transmitting binary data, floating point numbers, packed-decimal data, unique specialized codes, or machine-language computer programs. Control characters can be transmitted as transparent data without taking on control meaning.

Data-link control characters transmitted during transparent mode must be preceded by DLE if recognition as a control function is desired. Data link control sequences effective during operation in transparent mode follow.

DLE STX
Initiates the transparent mode for following text.

DLE ETB
Terminates a block of transparent text, returns the data link to normal mode, and requests a reply.

DLE ETX
Terminates the transparent text, returns the data link to normal mode, and requests a reply.

DLE SYN
Used to maintain sync or as a time-fill sequence for transparent mode.

DLE ENQ
Indicates "disregard this block of transparent data" and returns the data link to normal mode.

DLE DLE
Used to permit transmission of DLE as data when a bit pattern equivalent to DLE appears within the transparent data. One DLE is disregarded; the other is treated as data.

DLE ITB
Terminates an intermediate block of transparent data and returns the data link to normal mode. No reply is requested. The block check character follows DLE ITB. Transparent intermediate blocks can have a particular fixed length for a given system. If the next intermediate block is transparent, it must start with DLE STX.

The DLE STX following an intermediate transparent block can be preceded by SYN SYN, to permit any station "out of sync" to correctly synchronize with the transmission.

All replies, enquiries, and headers are transmitted in normal mode. Transparent data is received on a character-by-character basis; thus character phase is maintained.

The boundaries of transparent data are determined by the DLE STX and the DLE ITB, DLE ETB, or DLE ETX sequences that initiate and terminate the transparent mode. Therefore, the length of a transparent message can vary with each transmission.

TIME-OUTS

Time-outs are used to prevent indefinite data-link connections, due to false sequences or missed turnaround signals, by providing a fixed time within which a specific event must occur. Due to the different requirements for the various operations, four specific time-out functions are provided: (1) transmit, (2) receive, (3) disconnect, and (4) continue.

Transmit Time-Out

Transmit time-out is a nominal 1-second time-out that establishes the rate that sync-idles are automatically inserted into transmitted heading and text data. In normal data, two consecutive sync-idle characters (SYN SYN) are inserted every second. For transparent data, one transparent sync-idle sequence (DLE SYN) is inserted every second. Sync-idle characters are inserted into messages for timing purposes only, and have no effect on the message format.

Receive Time-Out

Receive time-out, a nominal 3-second-time out, provides the following capabilities:

Limits the waiting time tolerated for a transmitting station to receive a reply.

Permits any receiving or monitoring station to check the line for sync-idle signals. These sync-idle signals indicate that the transmission is continuing. For this reason, this time-out is reset and restarted each time a sync-idle is detected.

Limits the time any tributary station in a multipoint network remains in control mode while monitoring the line for its address code. Receive time-out runs whenever the station is in control mode. As long as the station remains in control mode, receive time-out is reset and restarted each time an ending control code (EOT, ENQ, NAK, WACK, ACK) is recognized.

Disconnect Time-Out

Disconnect time-out, an option on switched network data links, is a nominal 20-second time-out used to prevent a station from holding a connection for prolonged periods of inactivity. After 20 seconds of inactivity, the station disconnects from the switched network.

Continue Time-Out

Continue time-out is a nominal 2-second time-out associated with the transmission of TTD and WACK. The continue time-out is used by stations for which the speed of input devices (for transmitting stations) or the speed of output devices (for receiving stations) can cause transmission delays by affecting buffer availability.

TTD is sent by the transmitting station up to two seconds after receiving acknowledgement of the previous block if the transmitting station is not capable of sending the next transmission block prior to that time. A receiving station must transmit WACK to indicate a temporary not ready to receive condition when it is not able to receive within the 2-second period. The time-out interval permits the receiving station to immediately send an affirmative reply if it becomes appropriate within the interval.

SYNCHRONIZATION

Whenever synchronization (sync) is to be established, the transmitting station sends a sync character (SYN) a specified number of times in continuous sequence. The received stream is continuously monitored in a search for the contiguous eight bits that form this SYN character. If SYN is found, tentative character sync is assumed. If SYN is not found, the eight bits are shifted so that the longest resident bit is shifted out, a new bit is shifted in, and the test is repeated. This procedure continues until tentative character sync is achieved or until recovery techniques are initiated.

Once tentative character sync has been achieved, the receiver must confirm the establishment of sync. A specified number of following characters (or what are assumed to be characters) is examined for the continuous sequence of SYNs that confirms synchronization. If such a sequence is not found, the checking procedure is reinitiated. For the binary synchronous adapter, synchronization is established upon the receipt of two contiguous SYN characters.

INTERNATIONAL ADAPTATION (SWITCHING KITS)

The international data communications interface that is compatible with the RS-232-C interface is the CCITT COM SPA No. 100, V24. To allow additional switching on international data communications lines, CCITT switching kits are available for all line adapters.

These kits provide the ability to switch circuits CCITT 111 and CCITT 116/126 by means of manual switches mounted on the backplane of the SLC, the MLC, or the MLE. A single kit is used for one adapter and a quad kit is available for groups of four adapters (MLC and MLE only). These kits can be used with Datel 200, 600, and 1200 service. The switch module is pictured in figure 1-4; the switch settings to be used for the desired data rates and types of modulation are shown in table 1-4.

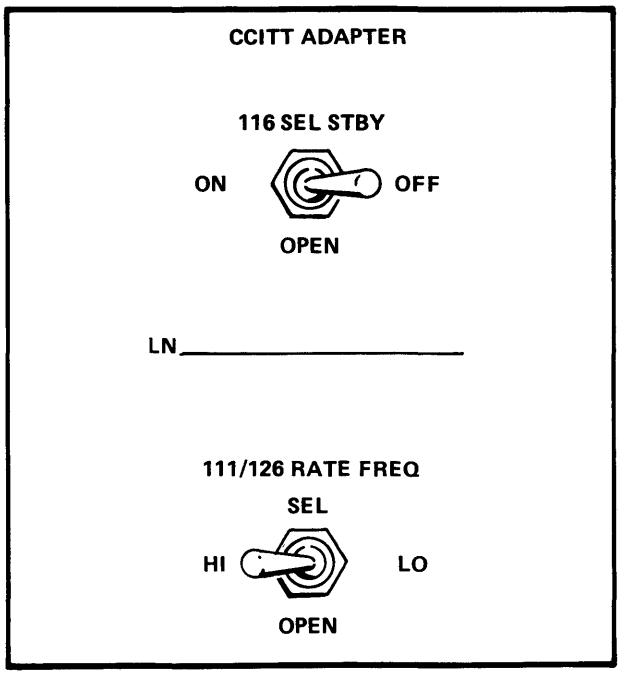


Figure 1-4. CCITT Switch Module

For asynchronous FDX Datel 200 service, switching the 111/126 RATE FREQ SEL switch to HI controls the answer mode and switching it to LO controls the call mode. The 116 SEL STBY switch has no function in this grade of service and should remain in the OPEN position.

For synchronous Datel 600 service, the switches are used together or independently as required. Data rate selection is made by switching 111/126 to HI for 1200 bps or LO for 600 bps. Rate can be either 1200 or 600 bps on leased facilities or switched standby facilities.

The selection of standby facilities is normally made at the data set. The 116 switch can be used to properly condition the line adapter to switched line configuration by switching it ON. The switched line configuration is then reported in the result descriptor.

In the specific case of a type 7C data set, because the data set is used for switched line service only, switches 116 and 111/126 are used only for speed selection. Accordingly, the STD/SYN line adapter must be configured for switched line operation.

Table 1-4. CCITT Kit Switch Settings

Switch Settings		Data Rate	Modulation Technique
116	111/126		
ON	LO	600 bps	FSK
ON	HI	1200 bps	FSK
OFF	LO	1200 bps	PSK
OFF	HI	2400 bps	PSK

SECTION 2
INSTALLATION PROCEDURES

INTRODUCTION

The line adapters described in this manual can be installed in any of the following I/O controls:

B 1800/B 1700 Single Line Control-1 (4-card backplane; see figure 2-1).

B 1800/B 1700 Single Line Control-2 (for installation into B 1800/B 1700 Dual Single Line Base-1, 6-card backplane; see figure 2-2).

B 1800/B 1700 Multi-Line Control-1 (12-card backplane; see figure 2-3).

B 1800/B 1700 Multi-Line Control-2 (8-card backplane; see figure 2-3).

B 1800/B 1700 Multi-Line Extension-1 (10-card backplane; see figure 2-4).

Installation procedures for any line adapter are contained in the Field Engineering Technical Manual for the pertinent I/O control. Installation instructions are also provided in the Field Test and Reference (FT&R) documentation supplied with I/O controls and line adapters. FT&R documentation also contains specific strapping instructions for line adapters.

B 1800/B 1700 SINGLE LINE CONTROL-1

The Single Line Control-1 (SLC-1) consists of an independent 4-card backplane mounted in either the B 1800 or B 1700 system card chassis. The control backplane contains two locations for the two single-line control logic cards, one location for a line adapter, and one location reserved for an automatic dial-out unit (ADO).

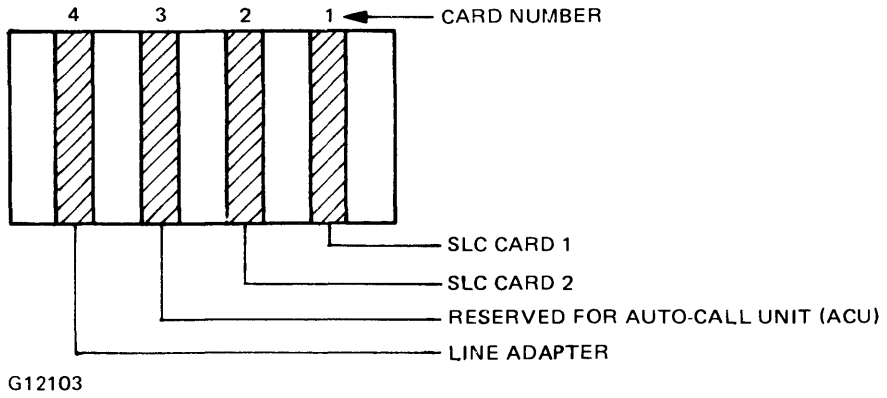


Figure 2-1. Single Line Control-1 (Card Insertion Side View)

B 1800/B 1700 DUAL SINGLE LINE CONTROL-1

The Dual Single Line Control-1 (DSLC-1) consists of an independent 6-card backplane mounted in either a B 1800 or B 1700 System card chassis. The control backplane provides locations for two individual single line controls. However, the ADO cannot be used with the DSLC-1 because two controls and the associated line adapters completely fill the backplane.

B 1800/B 1700 MULTI-LINE CONTROL-1

The Multi-Line Control-1 (MLC-1) consists of an independent 12-card backplane mounted in either a B 1800 or B 1700 card chassis. This control contains four positions for logic cards, and eight positions to accommodate eight line adapters. The first line adapter must be placed in line adapter position 0 (card location 12), and it is recommended that additional line adapters be placed sequentially in line adapter positions 1 through 7 (card locations 11 to 5).

B 1800/B 1700 MULTI-LINE CONTROL-2

The Multi-Line Control-2 (MLC-2) consists of an independent 8-card backplane mounted in either a B 1800 or B 1700 system card chassis. This control contains four positions for logic cards and four positions for line adapters. The first line adapter must be placed in line adapter position 0 (card location 8). It is recommended that additional line adapters be placed sequentially in line adapter positions 1 through 3 (card locations 7 to 5).

B 1800/B 1700 MULTI-LINE EXTENSION-1

The Multi-Line Extension-1 (MLE-1) consists of an independent 10-card backplane mounted adjacent to the MLC-1. The extension contains one logic card position, one unused position, and eight positions to accommodate up to eight line adapters. The first line adapter must be placed in line adapter position 8 (card location 1), and it is recommended that additional line adapters be placed sequentially in line adapter positions 9 through 15 (card locations 2 through 8).

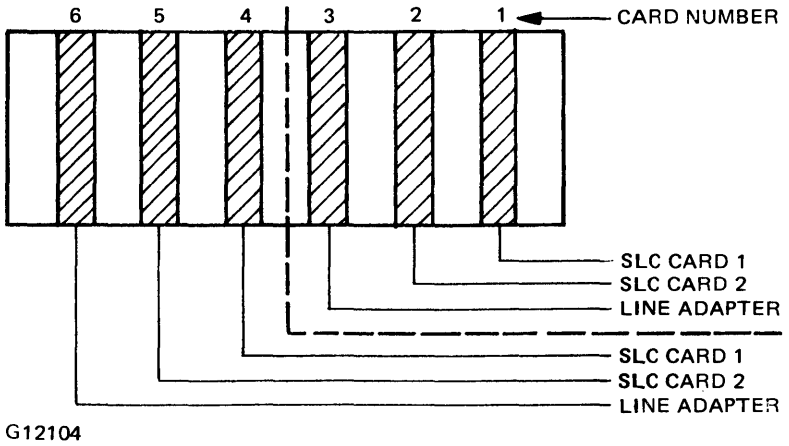


Figure 2-2. Dual Single Line Control-1 (Card Insertion Side View)

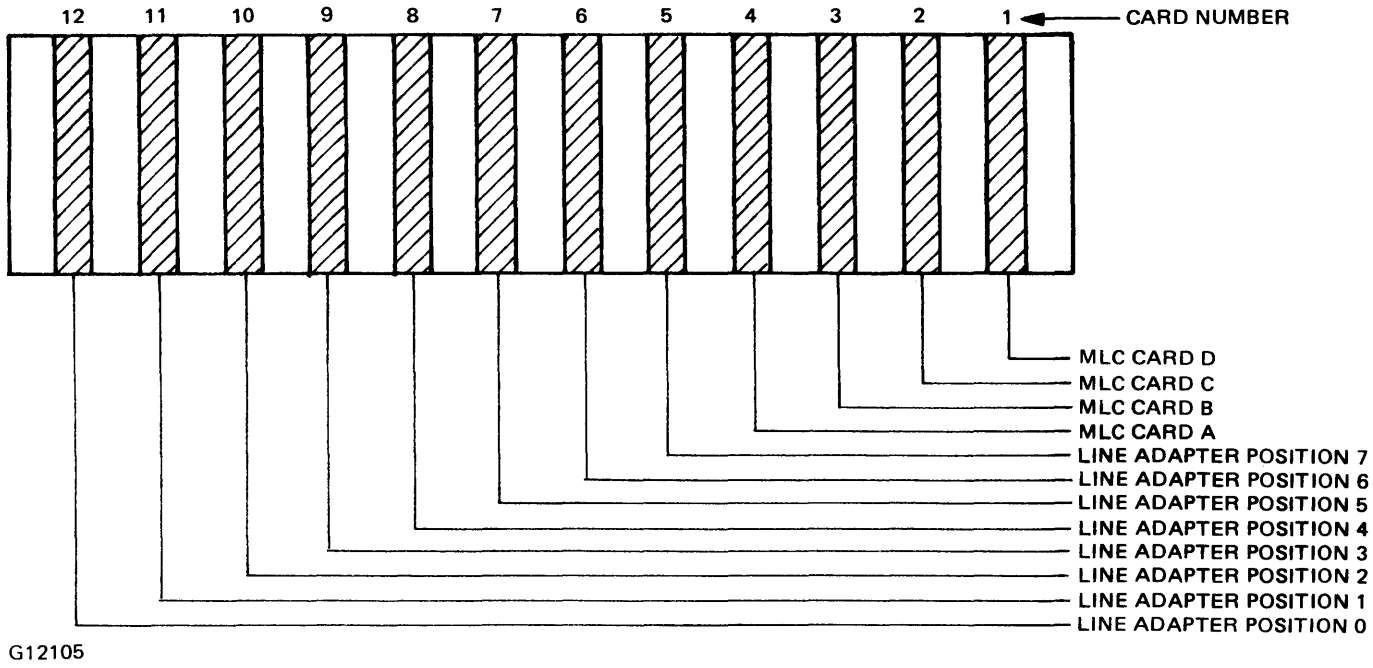


Figure 2-3. Multi-Line Control-1, -2 (Card Insertion Side View)

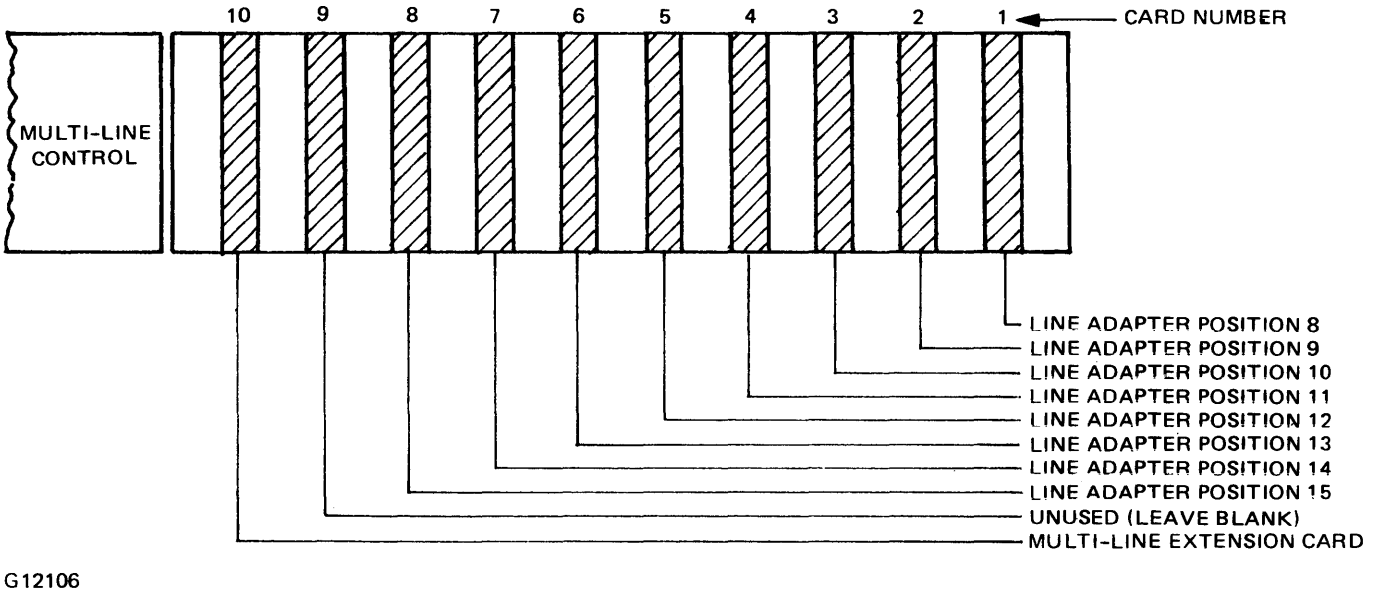


Figure 2-4. Multi-Line Extension-1 (Card Insertion Side View)

SECTION 3
DOCUMENTATION AND COMPONENTS

This section is not included in this document. Pertinent information is included in FETM 1066461, B 1800/B 1700 Single Line Controls, and FETM 1066842, B 1800/B 1700 Multi-Line Controls.

SECTION 4
MAINTENANCE TECHNIQUES

This section is not included in this document. Pertinent information is included in FETM 1066461, B 1800/B 1700 Single Line Controls, and FETM 1066842, B 1800/B 1700 Multi-Line Controls.

SECTION 5
STANDARD SYNCHRONOUS LINE ADAPTER

INTRODUCTION

THE B 1800/B 1700 Standard Synchronous (STD/SYN) line adapter provides an interface between an single-line or multi-line control and synchronous data sets employing the RS-232-C interface. The STD/SYN adapter provides the following data handling procedures:

Character assembly and disassembly.

Data character synchronization.

Vertical and longitudinal parity generation and checking.

ASCII control character identification.

Some of the data sets that can be connected to the standard synchronous line adapter are listed in table 5-1. The adapter can be connected to a data set using either 2-wire or 4-wire service. Four-wire service provides minimum turnaround time.

Field-strappable options for the STD/SYN line adapter provide the following capabilities:

Either switched or leased line selection.

Read squelch permitted for 2-wire operation.

Controlled continuous carrier permitted for 4-wire operation.

Conditioning of the New Sync line allowed, resulting in minimum resynchronization time for receive mode.

For a Write operation, the adapter is allowed to interpret 15 milliseconds of spacing on the receive pair of a 4-wire service as a Break. The Write terminates with an exception condition.

The adapter can omit generation or reception of a block check character (BCC).

Provides for a 2.5-second character time-out for a Read operation. An unstrapped jumper automatically provides

Table 5-1. Some Data Sets Used With the STD/SYN Line Adapter

Speed (bps)	Service	Data Sets	Burroughs Data Sets
600/1200/2400	Leased	WE 26	-----
2000	Dial (DDD)	WE 201A3	-----
2400	Leased	WE 201B3/201B1	TA 734-24, 774-24
4800	Leased	WE 208	TA 733-48, 773-48
9600	Leased	Rixon DS 9601	-----

UNIT IDENTIFICATION

The STD/SYN line adapter is contained on one logic card, identified by the Burroughs Manufacturing and Engineering (M&E) number 2201 2322. This number is imprinted on a metalized unit identification label supplied in the FT&R documentation for this adapter and designed to be affixed on the end of the card housing assembly into which the adapter is installed.

CONTROL CODE SENSITIVITY

Control code sensitivity for the standard synchronous line adapter is listed in table 5-2. Two contiguous sync codes (SYN SYN) must be received before a synchronous adapter becomes sensitive to any other codes. Sync codes are not stored in memory. After receipt of the last leading sync code, the adapter stores all subsequent codes except sync in memory up to, but not including, a block check code. SYN is not included in a BCC sum. At least four sync codes are automatically generated by the adapter prior to the transmission of data.

A start code is used to start the accumulation of a BCC with the next non-sync character. After the receipt of a start code, only an ending code terminates the operation.

A response code terminates an operation only if the control code is not preceded by the start code.

During Writes, ending codes terminate only those operations that are preceded by start codes. During Reads, ending codes terminate all operations, but an operation not preceded by a start code causes a BCC error to be reported in the Result.

A variant is provided to ignore EOT as a response code for Read and Write. During a Read, this variant causes the system to act as a terminal and receive a polling sequence from other systems. However, hardware recognition of addresses is not provided. During a Write, this variant allows the control to ignore EOT in order to transmit polling and other sequences that use EOT as the first code in a message as a line clearing code.

Table 5-2. STD/SYN Line Adapter Control Code Sensitivity

Function	Code
Sync	SYN
Start	SOH, STX
Ending	ETX, ETB
Positive Response	ACK, ENQ, BEL, NAK, EOT (time-out optional)

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

Read

The Read operator causes data to be accepted from the remote device and stored into ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

0000 T0D- -EVV P--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII to EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
VV=00: Normal linking.
=01: 2,2· Only if negative response is received.
=10: Link only if positive response is received.
=11: Undefined.
P = 0: Do not Poll.
= 1: Poll.

Write

The Write operator causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B-minus-1th location is reached.

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the Result Descriptor for the terminated operation.

0100 T000 0E00 PLLL L--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
P = 0: Do not Poll.
= 1: Poll. (Start with the location specified by the E address.)
LLLL: (0010-1101) Length of poll sequence (SLC only).

Break (Disconnect)

The Break operator causes an in-process operation, if any, to be terminated. A Break signal is transmitted to the remote terminal. A Break signal is a sustained transmission of spacing for either 32 bits (transmit) or 15 bits (receive). The result descriptor for a Break operation is returned immediately.

1100 00V- ---- ---- ---- UUUU

V = 0: Send Break; do not disconnect.
= 1: Disconnect; do not send Break. Loss of Data Set Ready reported in result descriptor. (Switched adapters only, other adapters send Break.)

Test

The Test operator is a request for the reporting (in the result descriptor) of the adapter's identification and the conditions specified by the V and M variant combination.

100V --M- ---- ---- ---- UUUU

VM=00: Complete the operation normally. Do not change the status of the Data Terminal Ready signal.
=01: Make the Data Terminal Ready signal true, then complete the operation.
=11: Make the Data Terminal Ready signal false, then complete the operation.
=10: Forbidden – causes the adapter to wait "forever." (Switched adapters only; other adapters complete immediately.)

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the standard synchronous line adapter are listed below, together with their meanings when set. Omitted bits in the 0-23 sequence are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception Conditions (Except for the Test operator, this bit is set if any of bits 2-15 are set.)
3	Parity Error - character or BCC (Read).
4	Memory Access Error (Read).
5	Memory Parity Error (Write).
6	Time-out (Read or Write).
7	Break Received (Write).
8	Ending Control Code expected but not received (Read or Write).
9	Linking terminated (Read; VV = 01 or 10).
11	Loss of Data Set Ready (Read, Write, Break). Absence of Data Set Ready (Read, Write, Break).
12	Loss of Clear To Send (Write). Loss of carrier (Read).
16	Operation completed.
17	Data communications device (Test).
18-23	Adapter ID (Test): 000000 = adapter not present 000010 = private adapter 100010 = switched adapter

FUNCTIONAL DESCRIPTION

Sequence Counter

The functions of the standard synchronous line adapter are controlled primarily by a sequence counter located in the adapter. This sequence counter, which functions independently of the counter in the data communication control, counts from 00 through 63, but counts 40 through 63 have no specific functions.

Figure 5-1 shows the basic flow of this counter. (Figure 5-1 is applicable to all standard adapters.

Block Diagrams

Figure 5-2 is a detailed block diagram of the standard synchronous line adapter, and figure 5-3 is a functional block flow diagram applicable to all B 1800/B 1700 standard line adapters.

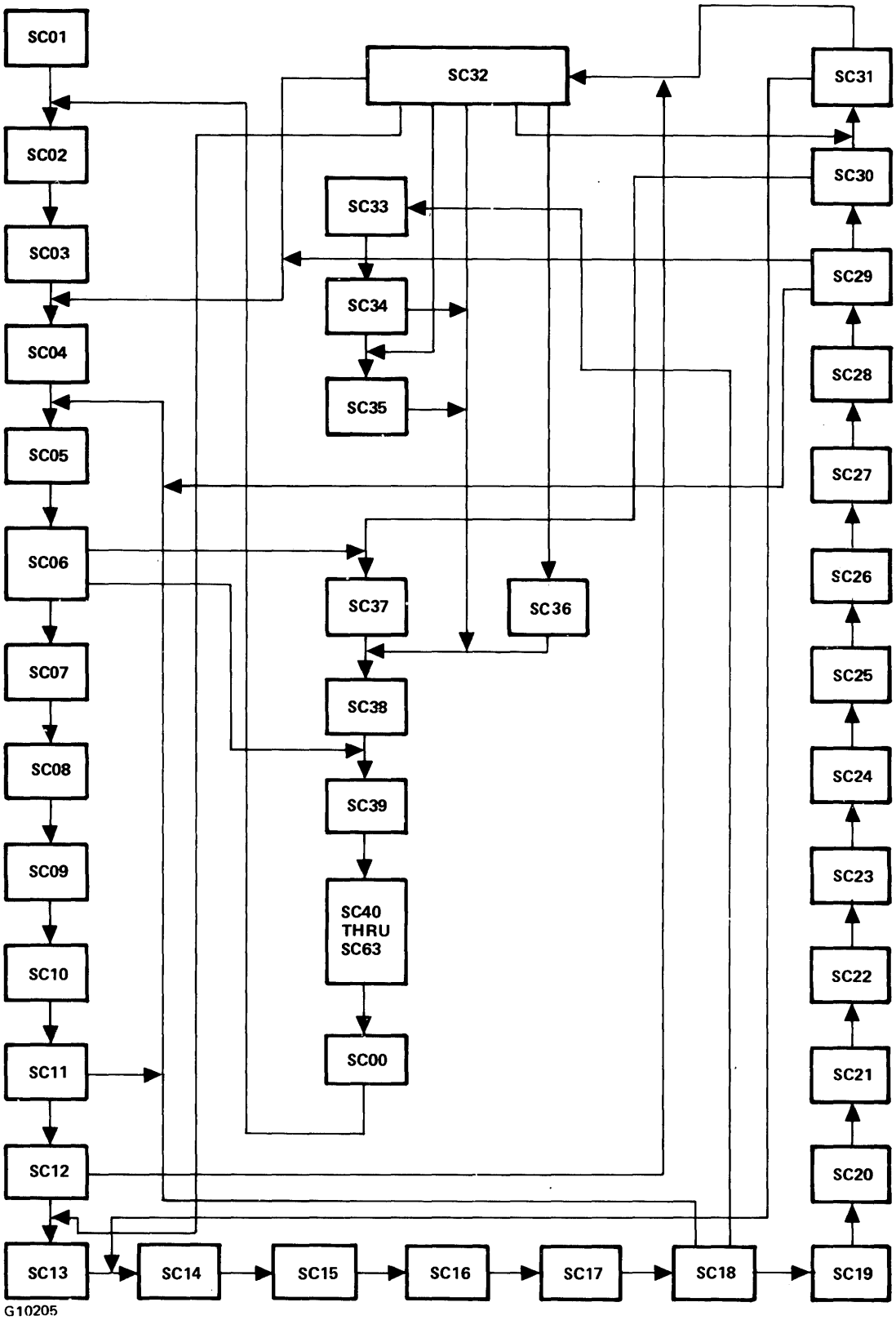


Figure 5-1. Basic Sequence Count Flow, Standard Line Adapters

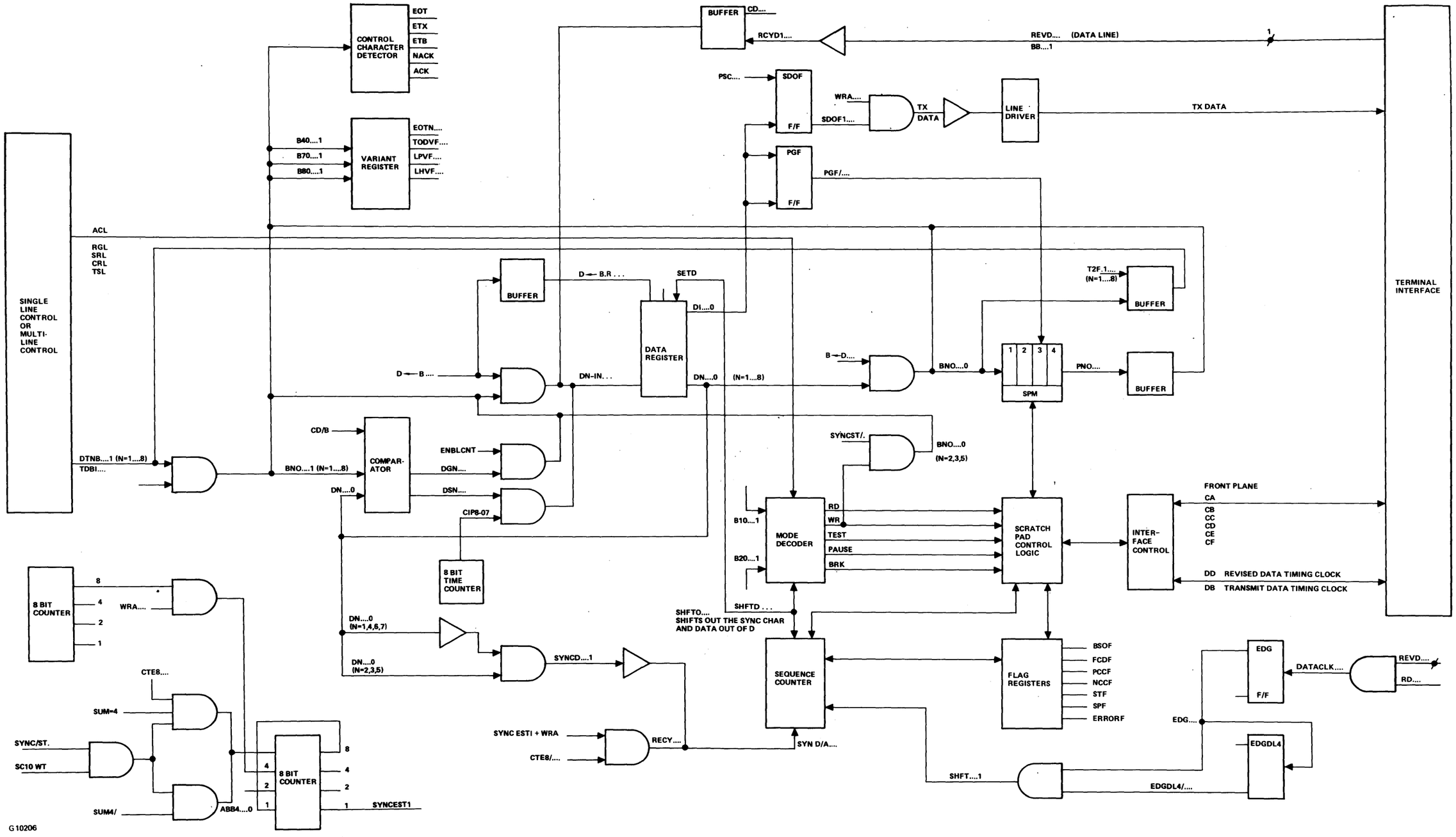


Figure 5-2. Detailed Block Diagram, STD/SYN Line Adapter

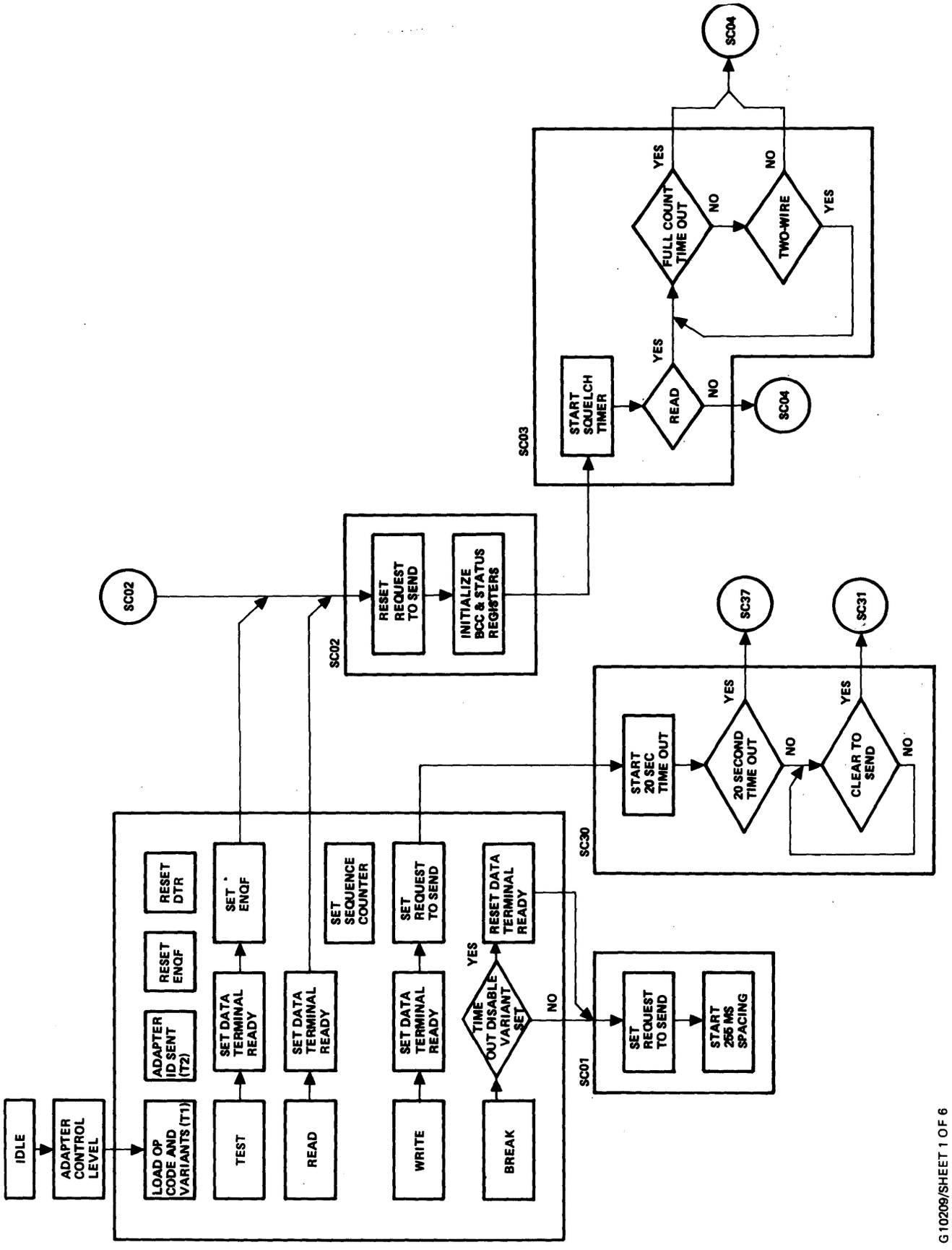
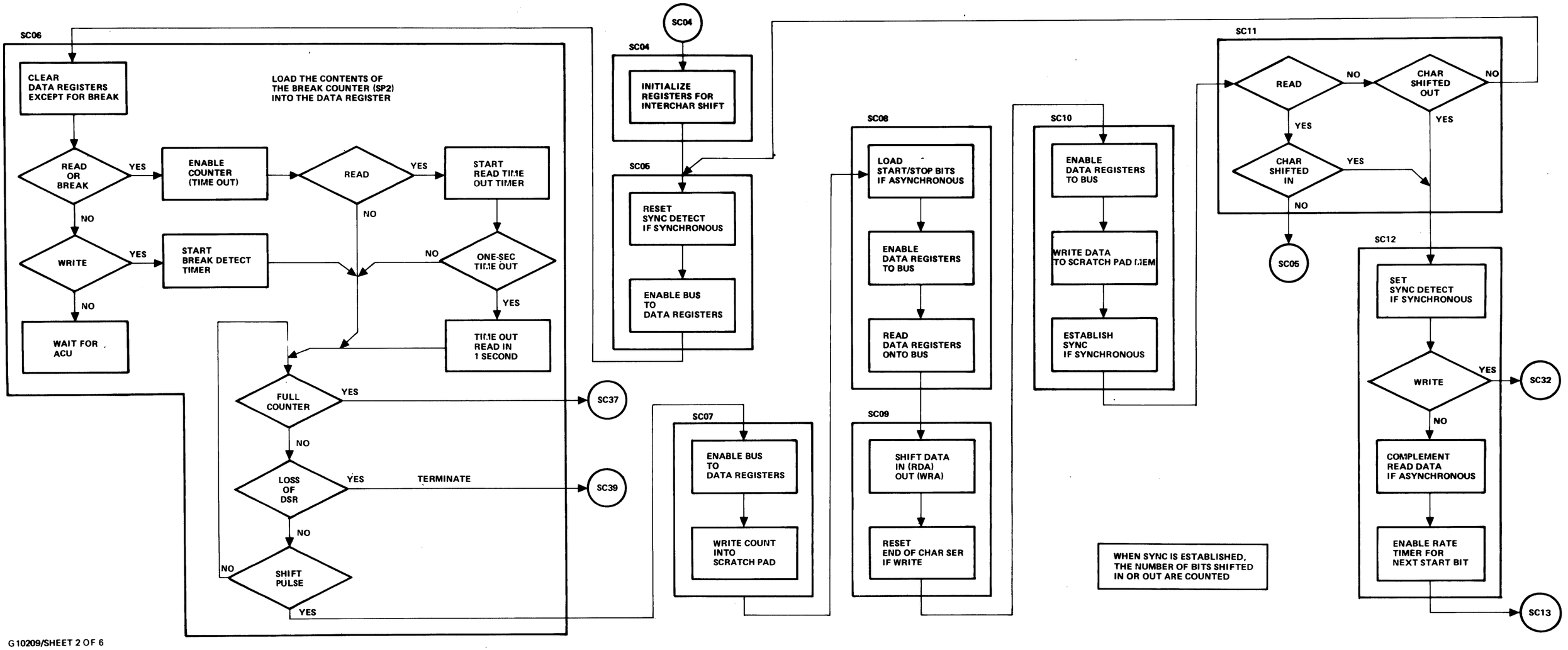


Figure 5-3. Flow Chart, Standard Line Adapters (Sheet 1 of 6)



G10209/SHEET 2 OF 6

Figure 5-3. Flow Chart, Standard Line Adapters (Sheet 2 of 6)

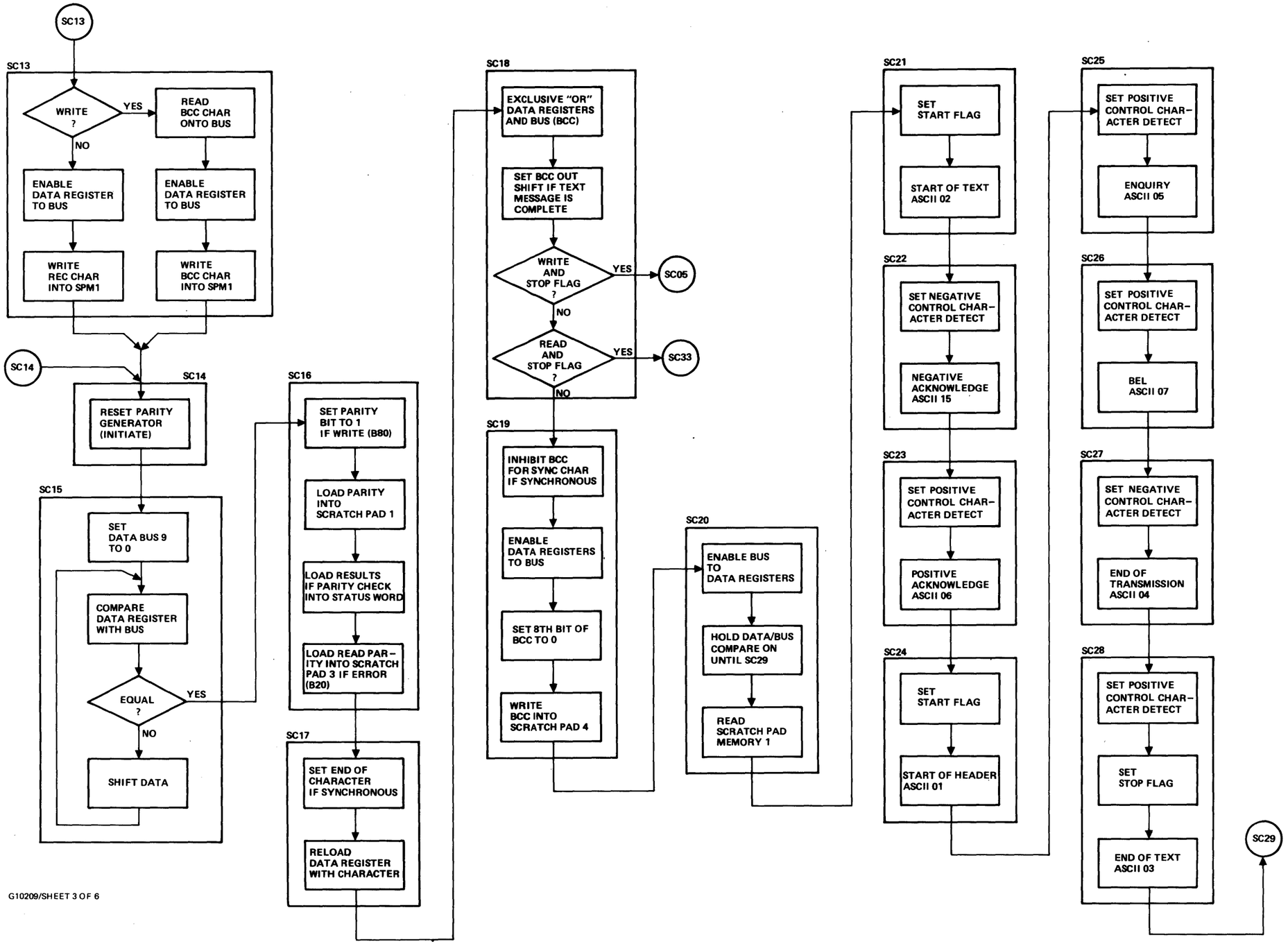
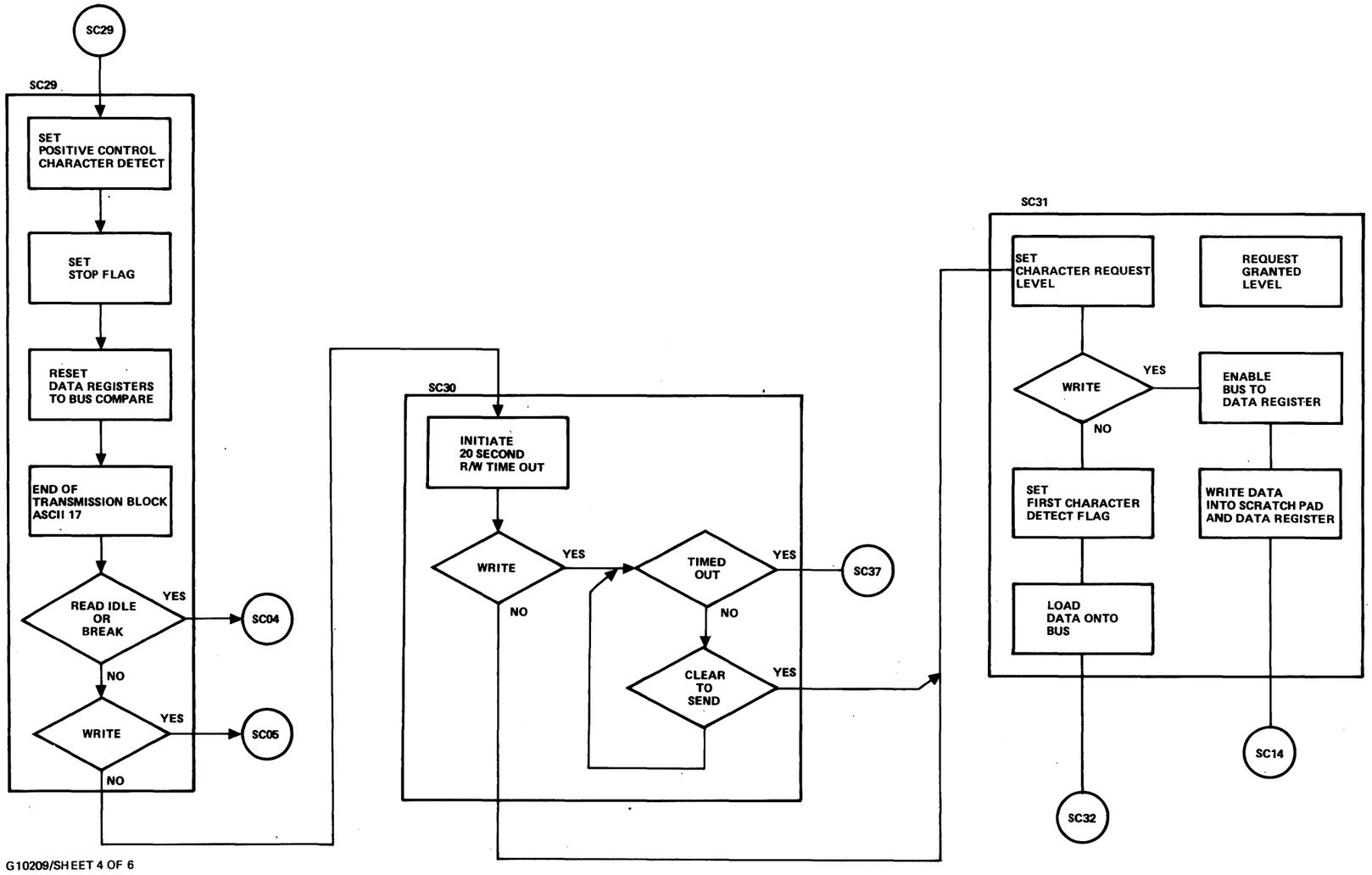


Figure 5-3. Flow Chart, Standard Line Adapters (Sheet 3 of 6)



G10209/SHEET 4 OF 6

Figure 5-3. Flow Chart, Standard Line Adapters (Sheet 4 of 6)

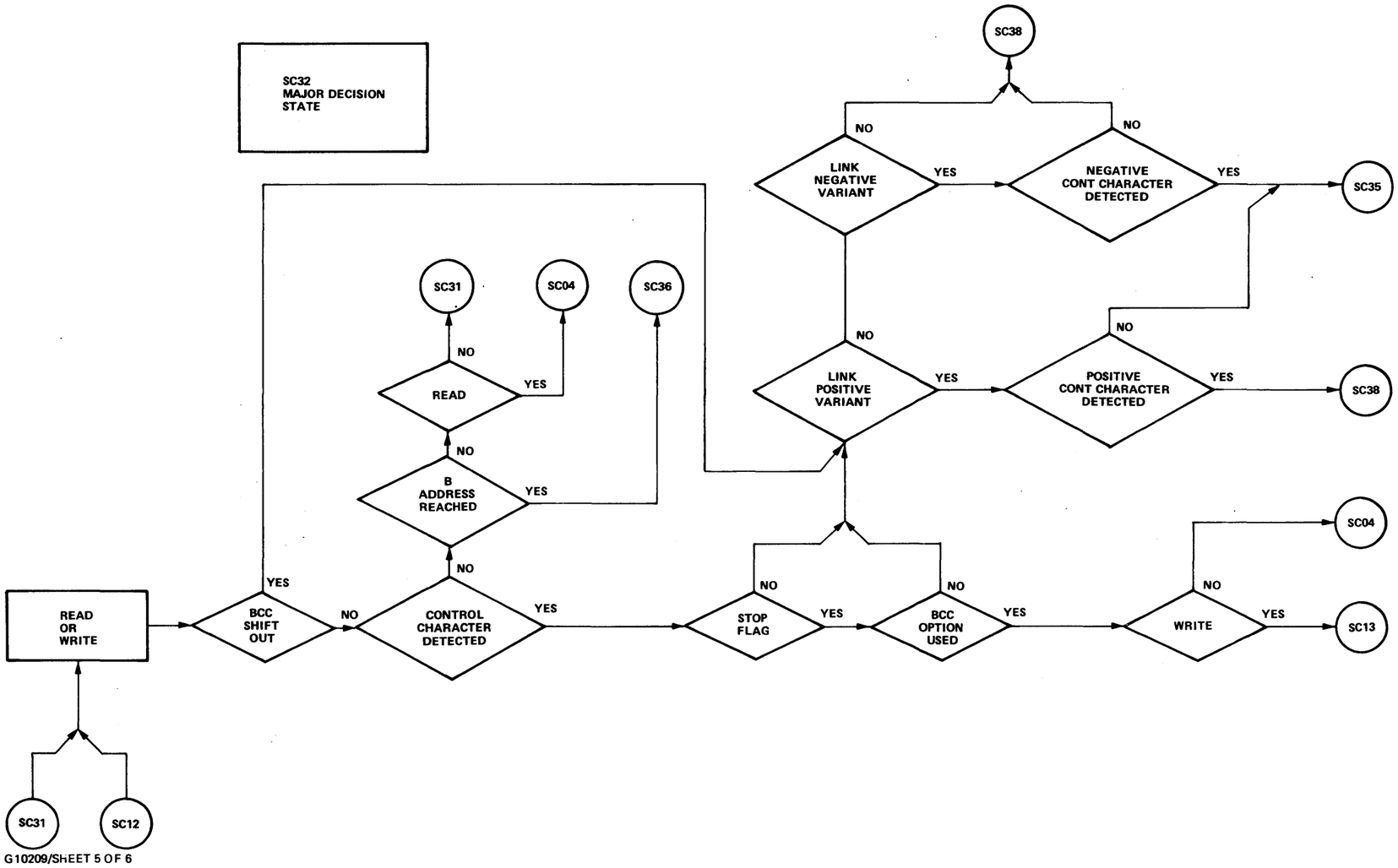
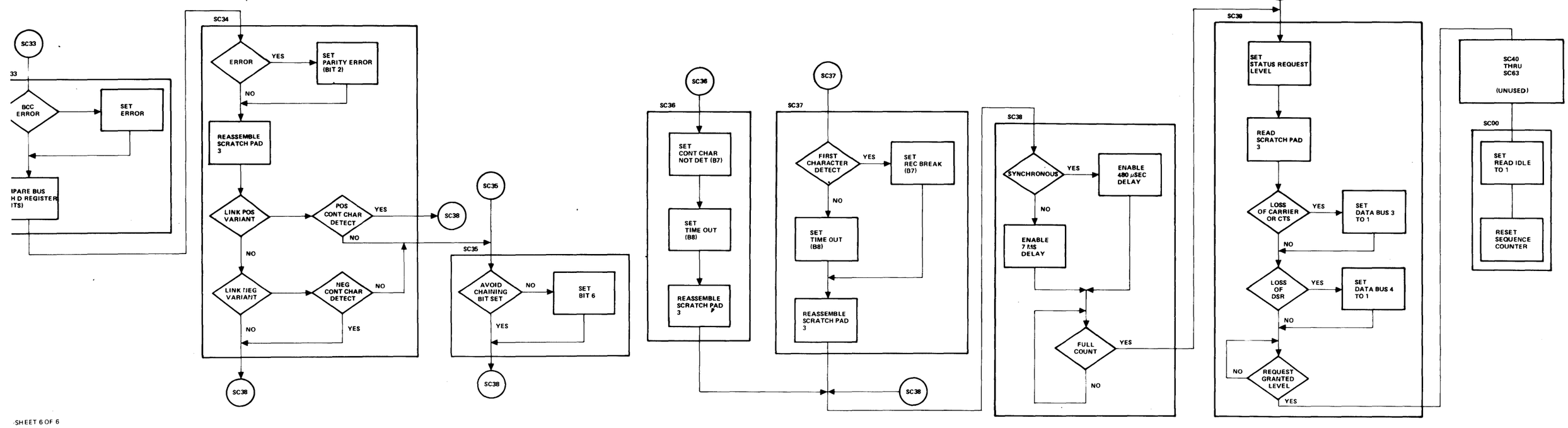


Figure 5-3. Flow Chart, Standard Line Adapters (Sheet 5 of 6)



SHEET 6 OF 6

Figure 5-3. Flow Chart, Standard Line Adapters (Sheet 6 of 6)

SECTION 6
STANDARD ASYNCHRONOUS LINE ADAPTER

INTRODUCTION

The B 1800/B 1700 Standard Asynchronous (STD/ASYN) line adapter provides an interface between a single-line or multi-line control and data sets employing an RS-232-C interface. The STD/ASYN line adapter provides the following data handling procedures:

Character assembly and disassembly.

Timing comparison.

Vertical and longitudinal parity generation and checking.

ASCII control character identification. Some of the data sets that may be used in conjunction with the STD/ASYN adapter are listed in table 6-1.

The STD/ASYN line adapter can be connected to a data set using either 2-wire or 4-wire service. Four-wire service provides minimum turnaround time.

The following field-strappable options are available:

Switched or leased line selection.

Read squelch for 2-wire operation.

Controlled continuous carrier for 4-wire operation.

With the WE103A-type data set, a pseudo-carrier-detect condition may be used. This reduces turnaround time.

Speed selection: 150, 300, 600, 1200, or 1800 bps.

In the Write mode, the adapter can be enabled to interpret 15 milliseconds of spacing on the receive pair of a 4-wire service as a break. The Write terminates with an exception condition.

The adapter may be strapped to omit generation or reception of a block check character (BCC).

A 2.5-second character time-out for Read operations can be provided. (A 1.2-second time-out is provided in the unstrapped mode.

Table 6-1. STD/ASYN Data Set Characteristics

Speed (bps)	Dial (DDD)		Leased		
	WE	V	WE	TA	V
150	103A	V21	103F	TA 713/753	V21
300	103A	--	103F	TA 713/753	V21
600	202C	--	202D	TA 713/753	V23
1200	202C	--	202D	TA 713/753	V23
1800	--	--	202D	TA 783	--

WE - Western Electric TA - Burroughs V - International

UNIT IDENTIFICATION

The STD/ASYN line adapter is contained on one logic card, identified by the Burroughs Manufacturing and Engineering (M&E) number 2201 2330, imprinted on a metalized unit identification label supplied in the FT&R documentation for this adapter and designed to be affixed on the end of the card housing assembly into which the adapter is installed.

CONTROL CODE SENSITIVITY

The control code sensitivity for the standard asynchronous line adapter is listed in table 6-2.

A start code is used to start the accumulation of a BCC with the next character. After the receipt of a start code, only an ending code can terminate the I/O operation.

A response code terminates the I/O operation only if the response code is not preceded by a start code.

During a Write operation, an ending code terminates the I/O operation if the ending code is preceded by a start code. During a Read operation, an ending code always terminates the operation. However, if the ending code is not preceded by a start code, a BCC error is reported.

A variant is provided to ignore EOT as a response code for a Read or Write operation. During a Read operation this variant allows the control and the associated computer system to act as a terminal and receive a polling sequence from other systems. However, hardware recognition of addresses is not provided. During a Write operation, this variant allows the control to ignore an EOT in order to transmit polling and other sequences that use EOT as the first code in a message as a line clearing code.

Table 6-2. STD/ASYN Line Adapter Control Codes

Function	Code
Sync	SYN
Start	SOH,STX
Ending	ETX,ETB
Positive Response	ACK, ENQ, BEL
Negative Response	NAK, EOT (timeout optional)

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

Read

The Read operator causes data to be accepted from the remote device and stored into ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

0000 T0D- -EVV P--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII to EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
VV=00: Normal linking.
=01: Link only if negative response is received.
=10: Link only if positive response is received.
=11: Undefined.
P = 0: Do not Poll.
= 1: Poll.

Write

The Write operation causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B-minus-1th location is reached.

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the result descriptor for the terminated operation.

0100 T000 0E00 PLLL L--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
P = 0: Do not Poll.
= 1: Poll. (Start with the location specified by the E address.)
LLLL 0010-1101: Length of poll sequence (SLC only).

Break (Disconnect)

The Break operator causes an in-process operation, if any, to be terminated. A Break signal, transmitted to the remote terminal, is a sustained transmission of spacing for either 32 bits (transmit) or 15 bits (receive). The result descriptor for a Break operation is returned immediately.

1100 00V- ---- ---- ---- UUUU

V = 0: Send Break; do not disconnect.
= 1: Disconnect; do not send Break. Loss of Data Set Ready reported in result descriptor. (Switched line only, other adapters send Break.)

Test

The Test operator is a request for the reporting (in the result descriptor) of the adapter's identification and the conditions specified by the V and M variant combination.

100V --M- ---- ---- ---- UUUU

VM=00: Complete the operation normally. Do not change the status of the Data Terminal Ready signal.
=01: Make the Data Terminal Ready signal true, then complete the operation.
=11: Make the Data Terminal Ready signal false, then complete the operation.
=10: Forbidden – causes the adapter to wait "forever." (Switched adapters only; other adapters complete immediately.)

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the standard asynchronous line adapter are listed below, together with their meanings when set. Omitted bits in the sequence (0-23) are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception Conditions. (Except for the Test operator, this bit is set if any of bits 2-15 are set.)
3	Parity Error - character or BCC (Read).
4	Memory Access Error (Read).
5	Memory Parity Error (Write).
6	Time-out (Read or Write).
7	Break Received (Write).
8	Ending Control Code expected but not received (Read or Write).
9	Linking terminated (Read; VV = 01 or 10).
11	Loss of Data Set Ready (Read, Write, Break). Absence of Data Set Ready (Read, Write, Break).
12	Loss of Clear To Send (Write). Loss of carrier (Read).
16	Operation completed..
17	Data communications device (Test)
18-23	Adapter ID (Test): 000000 = adapter not present 000010 = private adapter 100010 = switched adapter

FUNCTIONAL DESCRIPTION

Sequence Counter

Functions of the standard asynchronous line adapter are controlled primarily by an internal sequence counter that is independent of the sequence counters in the associated data communications control. Counts are from 00 through 63, but counts 40 through 63 have no specific functions. Figure 5-1 (section 5) shows the basic flow of this counter.

Block Diagrams

Figure 6-1 is a detailed block diagram of the standard asynchronous line adapter. Figure 5-3 (section 5) is a functional block flow diagram applicable to all B 1800/B 1700 standard line adapters.

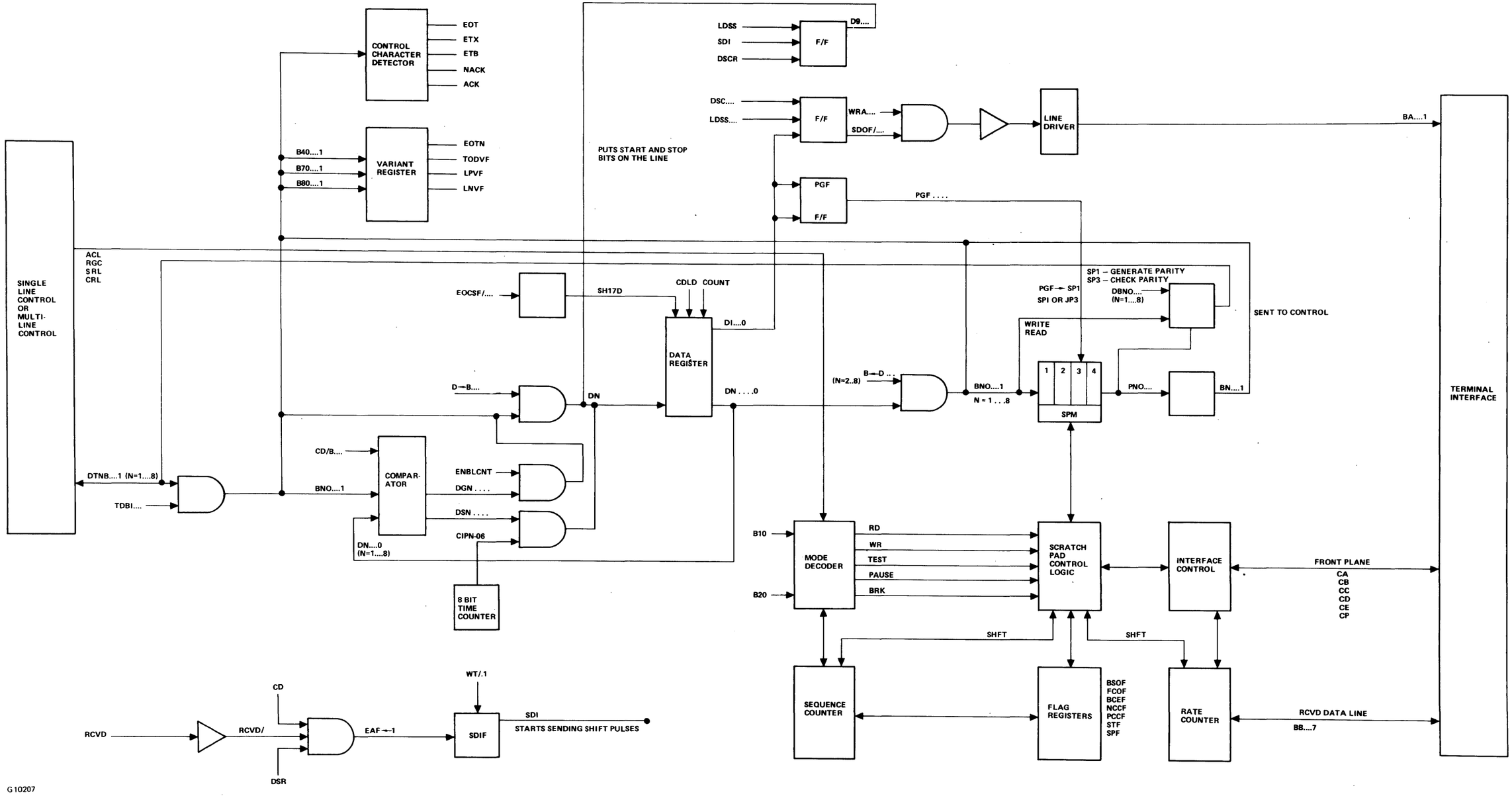


Figure 6-1. Detailed Block Diagram, STD/ASYN Line Adapter

SECTION 7
STANDARD DIRECT CONNECT LINE ADAPTER

INTRODUCTION

The Standard Direct Connect (STD/DIR) line adapter, an asynchronous adapter, provides for a 2-wire direct connection between a single-line or multi-line control and the following representative terminal devices:

TC500
TC700
TC3500
TU500/TU910
TU700/TU910
TU500/DC140
TU700/DC140
TD700
TD800

Direct-connect cable length can be up to 1000 feet (305 meters). This adapter must be strapped by the Burroughs Field Engineer for one of the following transmission speeds : 150, 300, 1200, 1800, 2400, 4800, or 9600 bps.

USASCII-7 transmission code is used. Seven data bits are transmitted, least significant bit first, followed by one parity bit. Character parity is even. The adapter generates and checks parity. The 8-bit (7 data, 1 parity) sequence is framed by a start bit (SPACE; polarity = 0) and a stop bit (MARK; polarity = 1).

A block check character (BCC) is transmitted following every message that contains a start code. BCC is formed by taking the modulo-2 sum following the start code on every data bit up to and including the ending code. The adapter may be strapped by the Burroughs Field Engineer to prevent BCC generation and checking.

For Write operations, EBCDIC code, from system memory, is translated to ASCII-8 by the control. The adapter drops the high-order bit, resulting in ASCII-7 to the line. On Read operations, ASCII-7 is translated to ASCII-8 by the adapter. ASCII-8 is translated to EBCDIC by the control.

Field-strappable options provide the STD/DIR adapter with the following capabilities:

Speed selection: 150, 300, 1200, 1800, 2400, 4800, or 9600 bps.

Interpretation of 15 milliseconds of spacing as a Break on Write. This spacing can be obtained by having the terminal or the adapter force a MARK condition on the 2-wire cable for 15 milliseconds while the other device on the line (terminal or adapter) is transmitting. Break causes the device that is in the Write mode to terminate with an exception condition.

Initial time-out period of 2.5 seconds. (The unstrapped timeout period is 1 to 2 seconds.)

Choice of 1.2, 2.5, or 20 seconds time-out before detection of the absence of data following a start code.

Choice of 0.0, 3.0, or 15 milliseconds Write delay before turnaround.

UNIT IDENTIFICATION

The STD/DIR line adapter is contained on one logic card, identified by Burroughs Manufacturing and Engineering (M&E) number 2201 2438. This number is imprinted on a metal unit identification label supplied with the Field Test and Reference (FT&R) documentation for the unit. When the adapter is installed into the system, this label must be affixed on the end of the 28-position card housing assembly that contains the adapter.

CONTROL CODE SENSITIVITY

Control code sensitivity is listed in table 7-1. On a Read operation, a start code is used to signal BCC accumulation, which begins with the next character. After the receipt of a start code, only an ending code terminates the I/O operation, unless the operation did not begin with a start code, in which case a response code terminates the operation.

A Write operation is terminated by an ending code only if the operation is preceded by a start code. During a Read operation, an ending code always terminates the operation. However, if the ending code is not preceded by a start code, a BCC error is reported.

A variant (E) permits EOT to be ignored as a response code for a Read or a Write operation. During a Read, this variant allows the I/O control and the associated computer system to act as terminal and receive a polling sequence from other systems. However, hardware recognition of addresses is not provided. During a Write, this variant allows the I/O control to ignore EOT in order to transmit polling and other sequences in which EOT is the first code in a message and serves as a line clearing code.

The Read variant C permits a failure to receive the first character within the strapped timeout period to be treated as if a negative response character had been received. Normally this variant is used in conjunction with the poll (P) and chain (VV) variants in order to permit non-present terminals to be ignored.

Table 7-1. STD/DIR Adapter Control Code Sensitivity

Function	Code
Sync	SYN
Start	SOH; STX
Ending	ETX; ETB
Positive Response	ACK; ENQ, BEL
Negative Response	NAK, EOT (timeout optional)

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

Read

The Read operator causes data to be accepted from the remote device and stored into ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

0000 T0D- CEVV P--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII to EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
C = 0: Do not treat time-out on first character as negative response.
= 1: Treat time-out on first character as negative response.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
VV=00: Normal linking.
=01: Link only if negative response is received.
=10: Link only if positive response is received.
=11: Undefined.
P = 0: Do not Poll.
= 1: Poll.

Write

The Write operation causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B-minus-1th location is reached.

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the result descriptor for the terminated operation.

0100 T000 0E00 PLLL L--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
P = 0: Do not Poll.
= 1: Poll. (Start with the location specified by the E address.)
LLLL 0010-1101: Length of poll sequence.

Break (Disconnect)

The Break operator causes an in-process operation, if any, to be terminated. A Break signal, transmitted to the remote terminal, is a sustained transmission of spacing for either 32 bits (transmit) or 15 bits (receive). The result descriptor for a Break operation is returned immediately.

1100 00-- ---- ---- ---- UUUU

Test

The Test operator is a request for the reporting (in the result descriptor) of the adapter's identification and the conditions specified by the V and M variant combination.

100V --M- ---- ---- ---- UUUU

VM=00: Complete the operation normally. Do not change the status of the Data Terminal Ready signal.
=01: Make the Data Terminal Ready signal true, then complete the operation.
=11: Make the Data Terminal Ready signal false, then complete the operation.
=10: Forbidden. Causes the adapter to wait "forever."

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the standard direct connect line adapter are listed below, together with their meanings when set. Omitted bits in the 0-23 sequence are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception conditions. (Except for the Test operator, this bit is set if any of bits 2-15 are set.)
3	Parity Error - character or BCC (Read).
4	Memory Access Error (Read).
5	Memory Parity Error (Write).
6	Time-out (Read or Write).
7	Break Received (Write).
8	Ending Control Code expected but not received (Read or Write).
9	Linking terminated (Read; VV = 01 or 10).
16	Operation complete.
17	Data communications device (Test).
18-23	Adapter ID (Test): 000000 = adapter not present 000010 = STD/DIR adapter

FUNCTIONAL DESCRIPTION

Sequence Counter

Functioning of the standard direct connect line adapter is primarily controlled by a sequence counter located within the adapter. This counter functions independently of the sequence counters in the data communications control. It counts from SC00 to SC63, but SC40 through SC63 have no specifically assigned functions.

Figure 5-1 (section 5) shows the basic flow of this counter.

Block Diagrams

Figure 7-1 is a detailed block diagram of the STD/DIR line adapter.

Figure 5-3 (section 5) is a functional block diagram that is applicable to all B 1800/B 1700 standard line adapters.

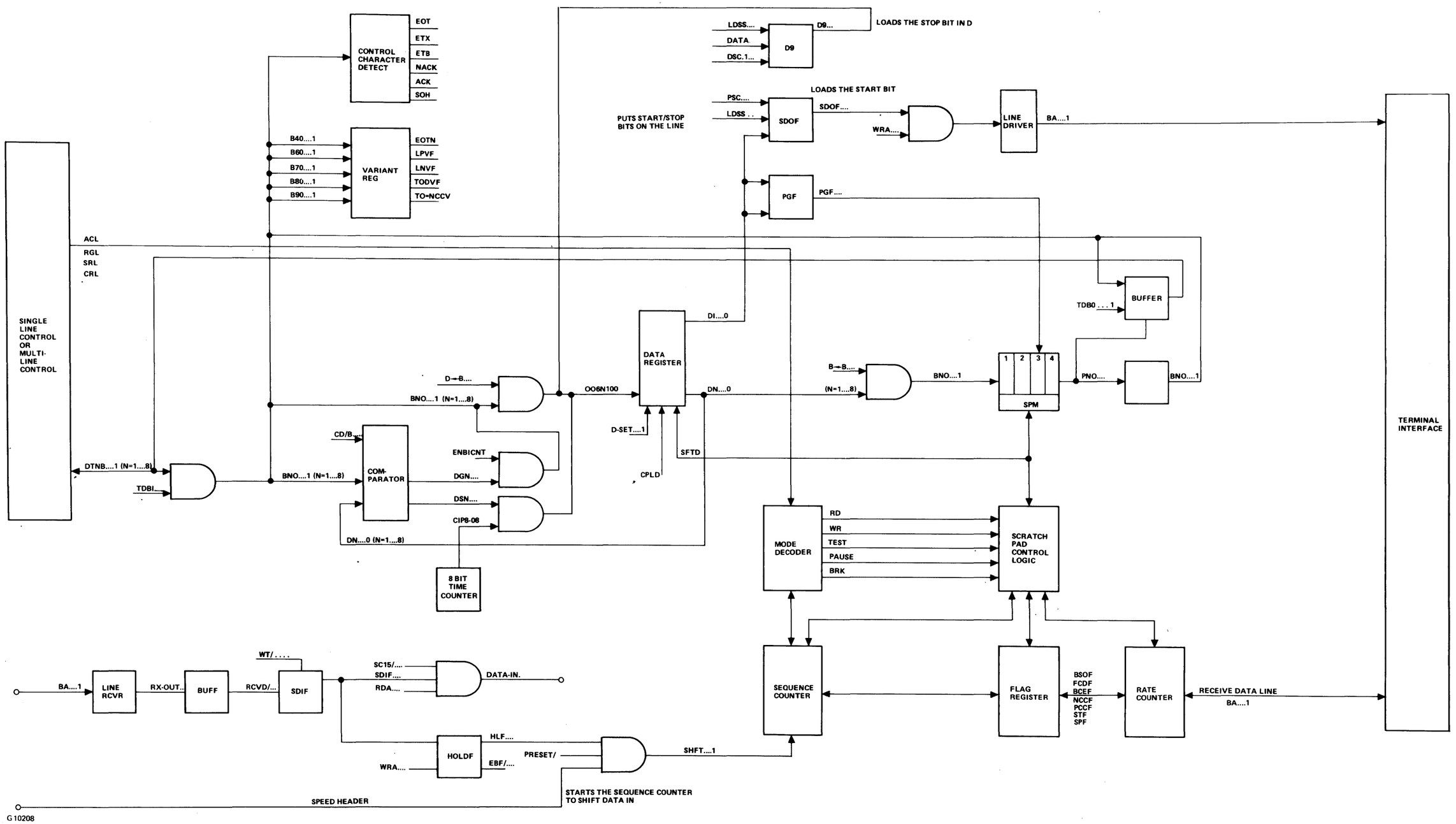


Figure 7-1. Block Diagram, STD/DIR Line Adapter

SECTION 8
AUTOMATIC DIAL-OUT LINE ADAPTER

INTRODUCTION

The Automatic Dial-Out (ADO) line adapter, also known as the Automatic Calling Unit (ACU) line adapter, can operate with up to four external devices when installed in the multi-line control, or with one external device when installed in the single line control. External devices include Bell System Series 801 auxiliary data sets (referred to as the "801 unit" in this section), or any of several Burroughs data sets that include automatic dial-out capability. When installed in the MLC, the ADO adapter services up to four 801 units or one Burroughs data set and three 801 units; in the SLC, the ADO adapter services either a Burroughs unit or and 801 unit.

Operation with more than one external device is on a one-at-a-time basis. Two variant bits in the I/O operator define which external device is to be selected, and a second I/O initiate must not be issued until the result descriptor has been returned for the operation specified for the first device. If an I/O initiate is directed to a busy ADO adapter, the adapter is forced to accept the new operation and all traces of the first operation are lost.

UNIT IDENTIFICATION

The ADO line adapter is contained on one logic card, identified by Burroughs Manufacturing and Engineering (M&E) number 2211 1454. This number is imprinted on a metal unit identification label supplied with the Field Test and Reference (FT&R) documentation for the unit. When the adapter is installed into the system, this label must be affixed on the end of the 28-position card housing assembly that contains the adapter.

I/O OPERATORS AND RESULT DESCRIPTORS

General Information

Table 8-1 illustrates valid I/O operators for the ADO line adapter.

Table 8-1. I/O Operators; ADO Line Adapter

	←Bit 0 (MSB)				Bit 23 (LSB)→	
Write (Dial)	010-	-D--	--AA	----	----	UUUU
Diagnostic Write	010-	-D-W	--AA	----	----	UUUU
Test	100-	-D--	--AA	----	----	UUUU
Diagnostic Test	100-	-D-W	--AA			

The variants represented by the letters D, AA, and UUUU, which appear in all four I/O operators, have identical usage for each operator:

D
Used by the SLC to direct the op code to the ADO adapter. This variant is ignored by the MLC.

UUUU
A number used by the MLC to define the unit (line adapter) number. The UUUU field is ignored by the SLC.

AA
Required by the MLC when more than one external device is used, specifies which device is to be acted upon. Operation with a Burroughs data set requires that AA = 00 regardless of the control (SLC or MLC) in which the adapter is installed. The ADO adapter can support only one external device when used in the SLC. It is recommended that the AA variants be reset (00) for SLC operation with an 801 unit.

Write (Dial)

Discussion

The adapter pauses for approximately 320 milliseconds to allow the local exchange to clear from the previous call. This clearing time is required if a call is terminated and immediately followed by the initiation of a dialing operation.

Following the pause, and provided that the external device is ready to accept dial digits, the ADO adapter requests the first digit from the control. Each digit consists of 8-bit words. The four most significant bits of each word are ignored, the four least significant bits contain one of the following:

(1) a dial digit (hexadecimal 0 through 9),
(2) a tandem dialing code (hexadecimal C or F), or
(3) an invalid digit (hexadecimal A, B, D or E).

The A and B addresses associated with the Write operation must precisely bracket the dial digits. (This means that the last digit must be located in the last word position of the assigned buffer area.) The ADO adapter generates an End-of-Number code (hexadecimal C, binary 1100)and transfers this code to the 801 unit. Transfer of the EON code is required in either of two situations:

The called data set does not send out an answer tone when a connection has been established.

The remote terminal is not equipped to automatically answer a call.

The ADO adapter includes four straps, one for each external device, that must be wired by the Burroughs field engineer if EON code transfer is to be specified.

Invalid digits, should they occur, are treated as if they were dial digits. The occurrence of an invalid digit results in the dialing of an indeterminate number. The probable result of an invalid digit is the return of a result descriptor indicating time-out or Abandon-Call-and-Retry.

The tandem dialing code is used if the calling station must wait for more than one dial tone. For example, on long distance calls some exchanges require that the digit 1 be dialed before the area code is dialed. In some cases the second dial tone will be heard approximately one second following the dialing of the digit 1. In this situation, it is necessary for the ADO adapter to provide a delay so that the second dial tone is detected before the remaining digits are dialed. The ADO adapter provides a delay of 3 seconds upon detecting the tandem dialing code. This code must be provided programmatically; therefore, the user must be aware of the significance of the tandem dialing code. Longer delays, if needed, are obtained by programmatically inserting contiguous tandem dialing codes.

For example, if the number 1 213 714 6285 is to be dialed, the adapter must receive the sequence 1F2137146285. Since the digits are received in 8-bit words, the hexadecimal information stored in memory must be: X/1 X/F X/2 X/1 X/3 X/7 X/1 X/4 X/6 X/2 X/8 X/5

where X represents the unused upper four bits of each digit.

Result Descriptor

A result descriptor is returned either upon completion of the dialing operation or following detection of an error condition. If the operation completes without error, the result descriptor is returned with both operation-complete bits (0, 16) set. If the operation does not complete properly, bits 0 and 16 are set, along with the exception condition bit (2) and the pertinent error definition bit. Table 8-2 explains the result descriptor for the Write (Dial) operation.

Table 8-2. Result Descriptor; ADO Adapter, Write Operator

Bit	Function
0	Operation complete.
1	Exception condition.
2	Power off.
3	Not used.
5	Memory parity error.
6	Time-out.
7-10	Not used.
11	Abandon call and retry.
12	Dial Line Occupied on or Data Set Ready on.
13-15	Not used.
16	Operation complete.
17-23	Not used.

NOTES

Bit 2

The power on or off status of the 801 unit is sent to the ADO adapter. A Write (Dial) OP to the ADO when the power-status line indicates 801 power off results in immediate termination of the Write operation. The result descriptor returned has bit 2 on.

Bit 6

The time-out bit, generated by a timer located on the ADO adapter, is set if the call is not established within 60 seconds. When operating with Burroughs data sets, this result descriptor bit provides the only indication that the call has not been established. This bit is also returned when operating with the 801 unit if the call is not completed or the abandon call and retry bit is not returned within 60 seconds.

Bit 11

The abandon call and retry bit, which is valid only when operating with the 801 unit, indicates that a call has not been established within a specified time. The time period is set by a switch located on the 801 unit. Available settings are 7, 10, 15, 25 or 40 seconds. The Abandon Call and Retry signal is generated by the ADO adapter and is the means by which the adapter is notified that a wrong number or a busy condition has been encountered.

Bit 12

Dial Line Occupied (DLO) is a signal generated from the 801 unit. This signal is on whenever the telephone line associated with the 801 unit is in use. The dialing process cannot begin unless DLO is in the off state. A comparable situation exists when operating with any Burroughs data set. In this case, the on state of Data Set Ready (DSR) is the indication that the telephone line is in use. The issuance of a Write (Dial) operator to the ADO adapter when either DLO or DSR is in the on state causes immediate termination. Bit 12 in the result descriptor indicates the error condition. ct RM 10 NO RJ FTE

Diagnostic Write

Discussion

The presence of the W variant distinguishes Diagnostic Write from Write (Dial). The purpose of the Diagnostic Write operator is twofold: (1) it allows the Field Engineer to determine that the data path through the control to the adapter is functional, and (2) it permits the adapter to operate in a repetitive mode, enabling signal observation and tracing on a dynamic basis.

The connection(s) between the adapter and the external devices (801 units and/or a Burroughs data set) must be removed or the external devices must be powered off. Upon receipt of the OP, adapter action begins in a manner similar to that during the Write (Dial) operation. The adapter simulates the handshaking signals that are normally provided by the external devices, then it repetitively requests dial digits from the control until the ending address is reached. Shortly thereafter, a result descriptor is returned.

Result Descriptor

One bit of the result descriptor (table 8-3) denotes the value of the AA bits received in the Diagnostic Write OP code. This bit is 8, 9, 10, 13, or 14, as appropriate.

Bits 2, 3, 11, and 12 comprise a 4-bit field that contains the value of the last hexadecimal byte received from the control if the decoded state of AA is 1, 2 or 3. These bits return the same value if the decoded state of AA is 0 and the external device is an 801 unit (bit 9 = 1). However, if the decoded state of AA is 0 and the external device is a Burroughs data set (bit 8 = 1), the 4-bit field does not contain the last-byte value; instead, it contains one of the following:

1111 (HEX F) Tandem Dialing digit

1100 (HEX C) End of Number (EON) code

Any other number is counted down to 1.

Result descriptor bit 2, exception condition, is always set because it represents an OR of bits 3 through 16. Consequently, on repetitive initiations of the Diagnostic Write operation, a dispatch operation rather than a linkage operation must be used, because the on status of bit 2 prevents linking.

Table 8-3. Result Descriptor, ADO Adapter, Diagnostic Write Operator

Bit	Meaning
0	Operation complete.
1	Exception condition.
2	Bit 8 of last byte received.
3	Bit 4 of last byte received.
4-7	Not used.
8	True if AA=00 and adapter is strapped for a Burroughs data set.
9	True if AA=00 and adapter is strapped for an 801 unit.
10	True if AA=01.
11	Bit 2 of last byte received.
12	Bit 1 0f last byte received.
13	True if AA=10.
14	True if AA=11.
15	Not used.
16	Operation complete.
17-23	Not used.

Test

The purpose of the Test operator is to return the device identification (ID) to the ADO adapter. The following result descriptor is returned:

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0 0

Bits 0, 16: operation-complete bits.
Bit 17: data communication device.
Bits 18-23: ADO line adapter.

Diagnostic Test

The W variant, when on (1), is used in conjunction with the AA variants to indicate the unit number of the data adapter associated with the dialing device. This information is set by the field engineer during installation by wiring strap patterns on the ADO adapter. The following device ID is returned in the result descriptor:

1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 1 J U U U U U 0

The U terms represent the unit (adapter) number of the line adapter associated with the dialing device addressed by variants AA in the operator. Bit J = 1 if the dialing device is connected and power is on.

ADO OPERATING PROCEDURES

Introduction

Operation with the ADO adapter requires the following initiation sequence:

1. A Test operation is sent to the adapter. This turns on the Data Terminal signal and completes immediately.
2. A Write (Dial) operator is sent to the ADO adapter. (The ADO adapter determines when the call has been established.)
3. When the call is established (indicated by the return of a Dial Result Descriptor with no exception) the line adapter can be initiated for a Read or Write operation.

If a call cannot be established, an exception condition is returned in the result descriptor for the Dial operation. In this case, a Break operator with the Disconnect variant set must be issued to the adapter before another call is attempted.

A Break (Disconnect) operator is required to allow the data adapter to go "on hook".

Operation With an 801 Unit

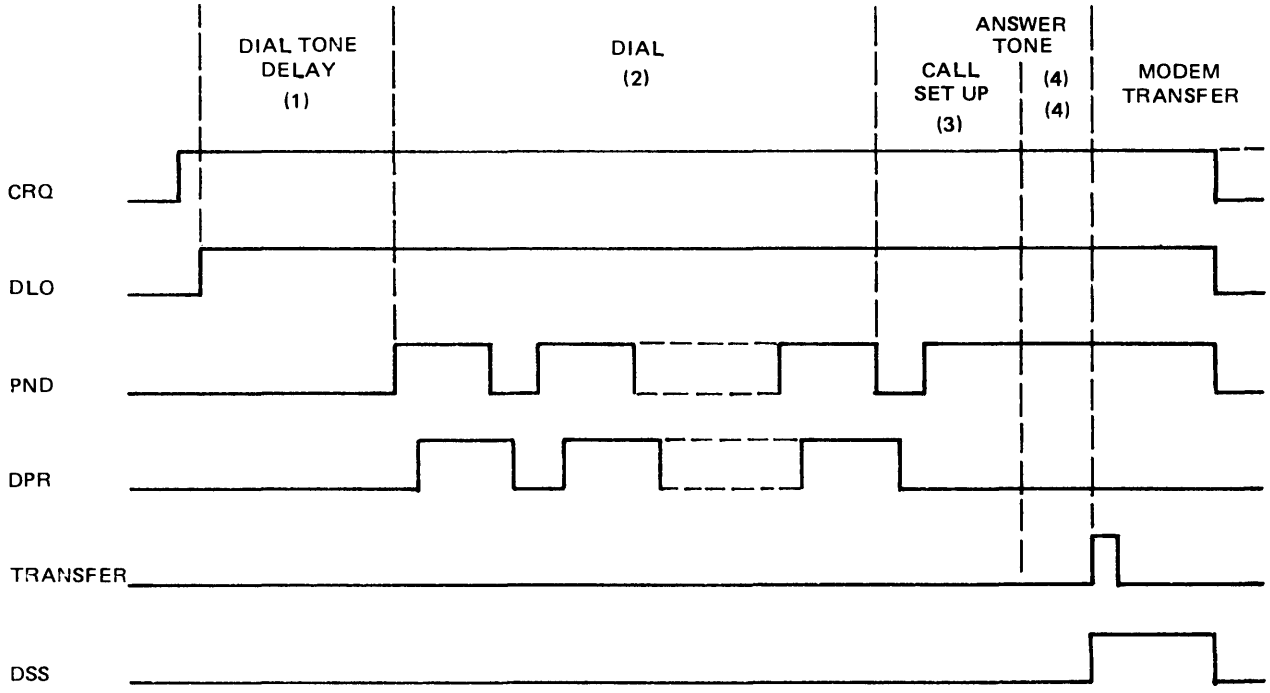
Procedures

The 801 unit has a 4-bit interface for receiving digits of the number to be dialed. This interface is defined in EIA Standard RS-366 and involves the following signals:

CRQ	Call Request
DLO	Data Line Occupied
PND	Present Next Digit
DPR	Digit Present
DSS*	Data Set Status
ACR	Abandon Call and Retry
DIGITS	NB8, NB4, NB2, NB1

DSS is synonymous with COS (Call Origination Status), the term used in RS-366. DSS, the more common term, is used in Bell technical references.

The dialing sequence is shown in figure 8-1. The adapter turns CRQ on provided that DLO is off. After the 801 unit detects the dial tone, digits are transferred to it one at a time. The 801 unit converts each digit to signals which duplicate the function of rotating-dial pulses or are compatible with Touch-Tone* frequencies. These signals are then transmitted to the phone line. At call completion, DSS comes on to signify receipt of the answer tone from the called data set. Receipt of DSS allows the line to be transferred to the ADO-associated data set. If DSS fails to come on, the Abandon Call and Retry (ACR) timer begins timing out.



AUTOMATIC DIALING SEQUENCE: DIAL TONE DELAY (1) VARIES WITH THE CALL AND IS USUALLY LESS THAN 3 SECONDS. FOR PULSE TYPE DIALING (2), PRESENT NEXT DIGIT IS ON FOR 100 MS TIMES THE NUMBER OF PULSES, THEN IS OFF FOR 600 MS (NOMINAL). FOR TOUCH-TONE DIALING, PND IS ON FOR 50 MS, THEN OFF FOR 70 MS. FOR CALL SET-UP (3), THE ADO ADAPTER SIGNALS END OF NUMBER BY NOT RAISING (DPR) AGAIN. ANSWER TONE (4) IS TRANSMITTED AT 2025 OR 2225 HZ.

G12112

Figure 8-1. Dialing Sequence, ADO Line Adapter

*Registered service mark of AT&T Co.

With pulse dialing, a typical 10-digit number takes 15 seconds to dial; for Touch-Tone dialing, the same number requires approximately 1 second. The answer sequence begins some time after the last digit has been sent by the 801. Several outcomes are possible:

A voice recording is on the line.

A Busy signal occurs on the line. Specified busy tones are 480 Hz and 620 Hz, interrupted 30 times a minute for paths that are busy, 60 times a minute for lines that are busy, and 120 times a minute for trunks that are busy.

A variant code tone occurs on the line. This is a rising and falling tone (200-400 Hz; sometimes called the "crybaby" tone). It indicates an unassigned telephone number.

A dial tone reoccurs on the line.

Nothing happens.

A wrong number is reached.

A data set responds with an answer-back tone.

Except when the data set responds with an answer-back tone, (the only successful data call), retry is required. The remote data set responds with a 2025-Hz tone. (Exception: WE103 responds with a 2225-Hz tone.)

The 801 unit resolves unsuccessful calls by means of an Abandon Call and Retry (ACR) timer. The time-out interval may be set for a minimum period of 7, 10, 15, 25, or 40 seconds by means of a screwdriver-operated switch on the 801 unit. For most telephone switched network operations, a period of 25 or 40 seconds is recommended to allow sufficient time for the call to go to completion.

The 801 unit provides an End of Number (EON) option which gives control of the line to the data set at the end of the dialing sequence. If this option (which requires straps in both the 801 unit and the ADO adapter) is installed, the adapter generates and transfers the EON code to the 801 unit after the last dial digit has been sent. The 801 unit recognizes EON immediately and connects the telephone line to the data set. DSS is set to 1 to indicate that the line has been transferred to the data set; however, some period of time elapses before the call is established. In this mode of operation the on state of DSS does not indicate that the connection has been made. If strapped for EON operation, the ADO adapter waits 20 seconds after DSS goes on before returning a Result Descriptor. It is reasonable to expect that most calls will connect within this period. However, EON termination does not provide a positive indication that the connection has been made.

The EON mode of termination is required only if the called data set does not send out an answer-back tone. Some of the WE 101 series of data sets do not transmit answer-back tones. Detection of the answer-back tone is the only reliable means of determining that the connection has been made.

Required or Recommended 801 Configurations

Interface

The voltage interface specified in EIA standard RS-366 must be used. The relay-closure interface (models 801 A2 and 801 A3) is electrically incompatible with the ADO adapter.

Mode of Termination

The 801 unit must be configured to allow Call Request (CRQ) to be turned off when the call has been established. Call termination is achieved by issuing a Break (Disconnect) operator to the data adapter; this turns Data Terminal Ready off. The option "terminate call via data set after DSS goes on" (called the "Z" option) provides this method of operation.

Answer-Back Signal Detection

Units that are able to detect the Answer-Back tone from the called data set are recommended. WE101 is permissible, recommendation is operation with the WE101-type data but WE103 should be used rather than WE101 whenever possible.

801-to-ADO Connection

Units are connected as shown in figure 8-2. Split cables are used to permit four 801 units to be connected to the ADO adapter frontplane connectors ($Y, $Y). Connectors $X and $X are reserved for operation with a Burroughs data set.

Operation With Burroughs Data Sets

A strap pattern, called the "BDS strap," must be installed in the ADO adapter when operation with a Burroughs data set is planned. Also, a telephone-type CBS coupler must be connected between the telephone line and the Burroughs data set. For additional information on this device, refer to the Bell System Technical Reference: Data Couplers CBS and CBT for Automatic Terminals.

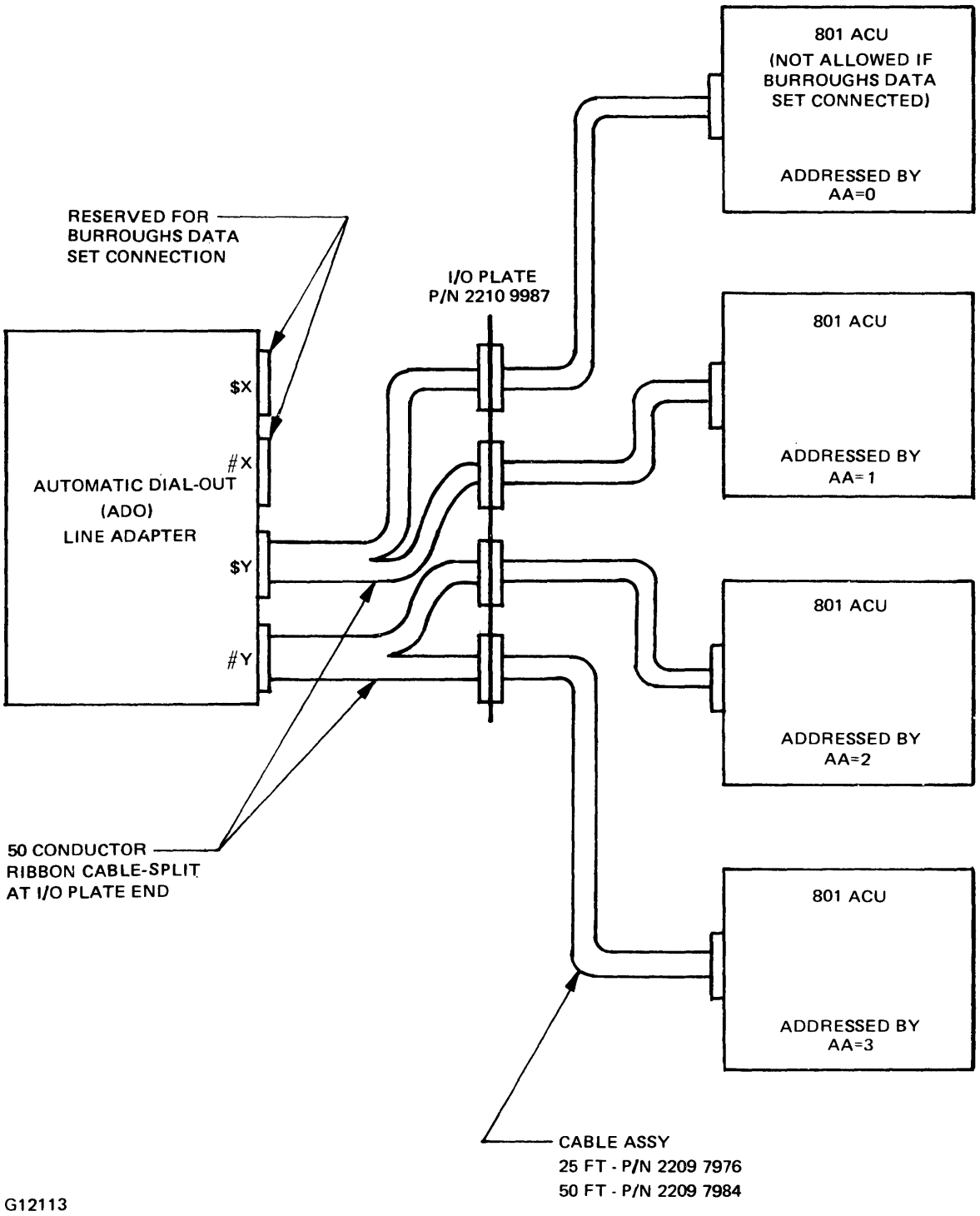


Figure 8-2. ADO Adapter Connector to Multiple 801 Units

Operation with Burroughs TA714

The TA714 and other Burroughs data sets having automatic dialing capability operate at the telephone line interface in a manner similar to the 801A series units; that is, the number dialed is converted into a serial train of pulses which are transferred to the telephone line. However, the interface between a Burroughs data set and the ADO adapter is significantly different from the interface between an 801 unit and the ADO adapter.

In allowing the Burroughs data set to dial a number, the Data Terminal Ready signal must be switched on and off with the desired number. The source of Data Terminal Ready can be any of the existing data adapters having an EIA RS-232 voltage interface The following line adapters currently satisfy this interface requirement:

Burroughs Standard Synchronous

Burroughs Standard Asynchronous

Binary Synchronous

TTY Direct Asynchronous (RS-232 interface)

The interconnection of the three elements (the data line adapter, the ADO adapter, and the Burroughs data set) is shown in figure 8-3.

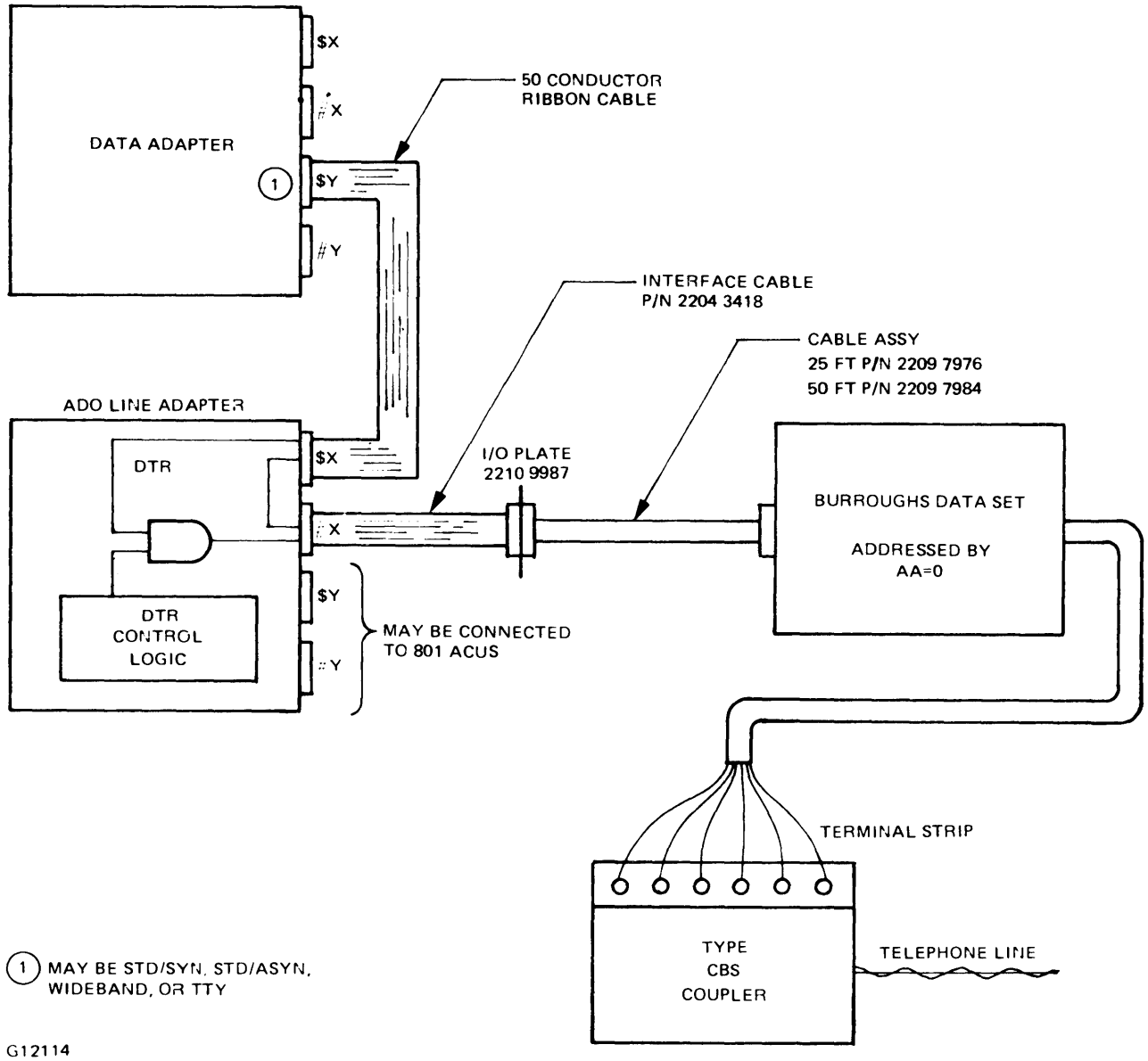


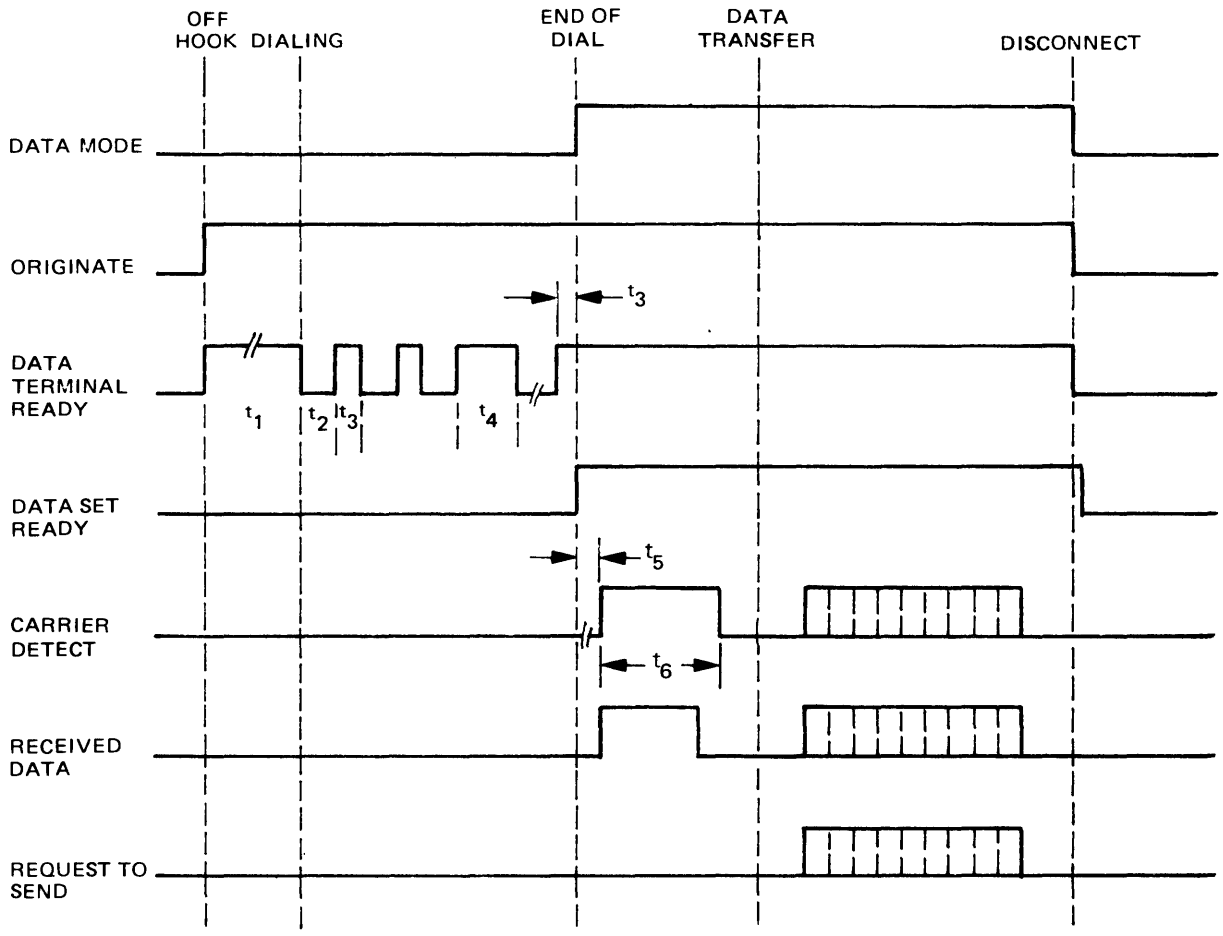
Figure 8-3. ADO Connections to Burroughs Data Sets

For dialing to take place, Data Terminal Ready must be initially on. The ADO adapter switches DTR off as required to dial the number.

In addition to DTR, the TA714 requires the Originate (OR) and Data Mode DM signals. These signals are generated by the ADO adapter. The timing relationships of these signal lines are shown in figure 8-4. The following paragraphs describe operation of the TA714.

Upon receiving a Write OP, the ADO adapter pauses for 324 milliseconds and then raises OR. DTR is on until switched off by the adapter. After a pause of 3 seconds to allow the dial tone to come on, the number to be dialed is pulsed by switching DTR off for 60 milliseconds and then on for 40 milliseconds. This cycle repeats N times where N is the integer value of the digit. Each digit in the pulse string is separated by an interdigit delay period of 729 milliseconds. During this period, DTR is on.

When dialing is complete, DTR is on and must remain on throughout the period of data transmission. DM is turned on 40 milliseconds after completion of dialing. This signal must also remain on throughout the period of data transmission.



t_1 = DIAL TONE DELAY

t_2 = 60 MILLISECONDS

t_3 = 40 MILLISECONDS

t_4 = INTERDIGIT DELAY - 729 MILLISECONDS

t_5 = TIME NECESSARY FOR CALLED STATION TO ANSWER

t_6 = 2 TO 5 SECONDS

G12115

Figure 8-4. Timing Diagrams, TA714 Terminals

Data Set Ready (DSR) comes on within 10 milliseconds after DM comes on. However, the off-to-on transition of DSR does not indicate that the call has been established. Call establishment in the TA714 occurs when the Received Data line goes from MARK level to SPACE level. Prior to the actual start of data transmission, the SPACE level on the Received Data line is derived from the answer-back tone arriving from the remote data set. Logic within the ADO adapter is used to determine that the Received Data line remains at SPACE level for at least one second. This procedure is provided so that a noise spike due to line perturbation is not interpreted as a call-established indicator. The answer-back tone is on the line for 2 to 5 seconds.

The ADO adapter completes its operation when it detects the return of the Received Data line to a MARK level. The adapter reports operation complete, no error in its status message to the control, which, in turn, issues operation complete, no exceptions, in its result descriptor to the system.

If an answer-back tone is not received within 60 seconds, the ADO adapter times out and the control reports the time-out in the Result Descriptor. Time-out is one of the two possible exception conditions that can be returned when operating with Burroughs data sets. The other exception condition occurs if DTR is off at the time the ADO adapter receives a Write operation code.

Once a call has been established, the operation of the ADO adapter is complete. Data transmission is now under total control of the data adapter. Call termination occurs only when the data adapter drops DTR in response to a Break (Disconnect) operator, and DTR off causes the signals OR (Originate) and DM (Data Mode) to be turned off.

A Break (Disconnect) operator should be issued even if the call is terminated at the remote end first. Failure to issue the Break operator may keep the telephone line open thus preventing further use. It is important to employ a communication discipline that enables one station to convey to the other its intention of going "on hook".

DSR remains on even if the call is not established within 60 seconds (TA714 only). In this case, it is mandatory to issue a Break operator to the data adapter before attempting to re-dial.

Operation with TA1203 or TA2403 Data Set

The connection procedure for either the TA1203 or TA2403 data set is similar to that described for the TA714 with the following exceptions:

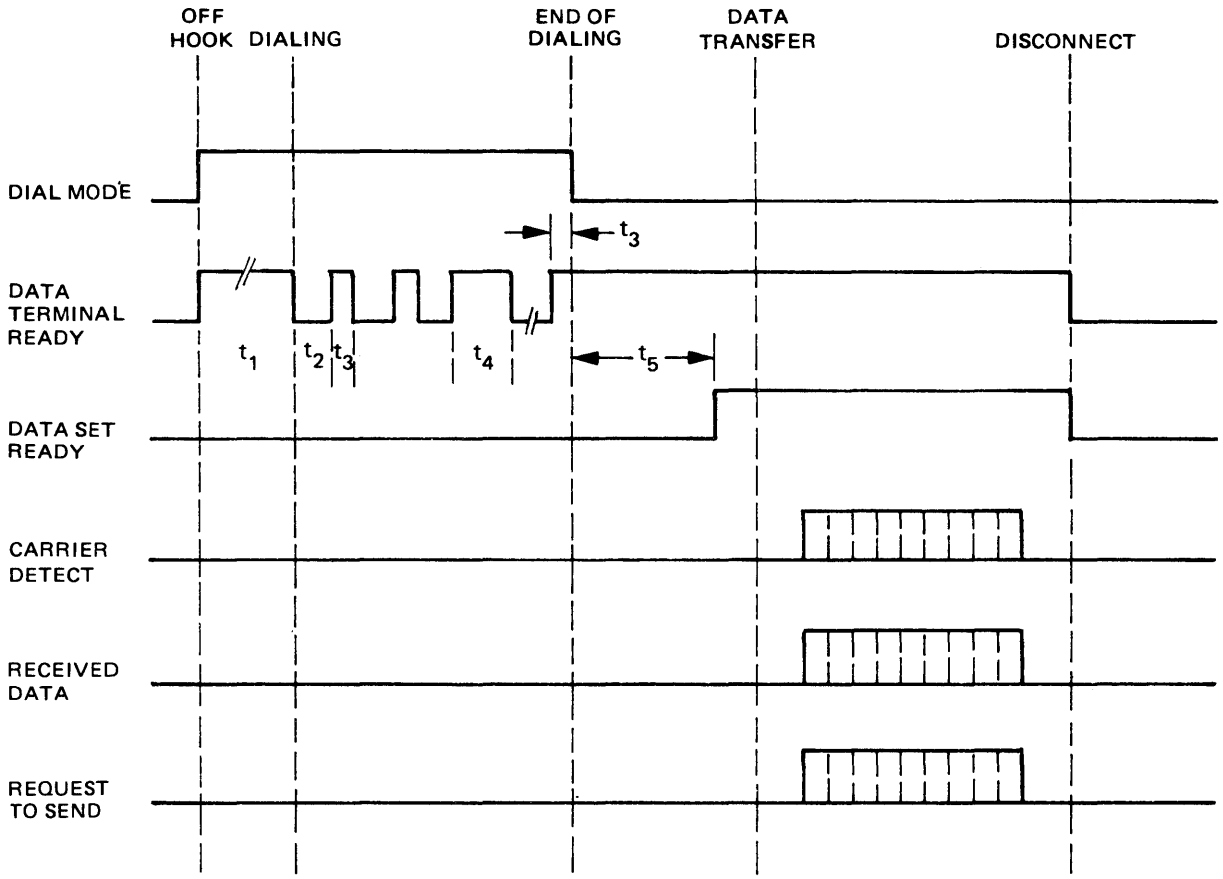
The Originate (OR) and Data Mode (DM) signals are absent.

A signal termed Dial Mode is required. This signal is on during the dialing operation and off at all other times.

Both the TA1203 and the TA2403 data sets turn DSR on upon detecting the Answer-Back tone. When DSR goes on, the ADO adapter completes its operation and returns operation complete, no exception in the Result Descriptor to the system. Timeout error is returned in the Result Descriptor if DSR does not come on within 60 seconds following completion of dialing.

A strap pattern (designated TA714/) must be installed in the ADO adapter when operating with the data sets covered in this section, or with any data sets that use similar connection procedures.

The timing procedure for TA1203 and TA2403 is shown in figure 8-5.



t_1 = DIAL TONE DELAY

t_2 = 60 MS

t_3 = 40 MS

t_4 = INTERDIGIT DELAY - 724 MS

t_5 = TIME NECESSARY FOR CALLED STATION TO ANSWER

G12116

Figure 8-5. Timing Diagrams, TA1203 and TA2403 Terminals

FUNCTIONAL DESCRIPTION

Figure 8-6 is a block diagram of the major elements of the ADO adapter. The function of each of these elements is described in the following subsections.

D Register

The D register is a 4-bit register used primarily to receive a 4-bit dial digit from the SLC or MLC control. The digit is transferred from the control to the ADO adapter by means of a 9-bit bus (Data Transfer bus DT1B through DT9B). The dial digit is contained in the four least-significant bits of the bus (DT1B through DT4B).

The D register can also place bits on the bus for presentation to the I/O control during the Diagnostic Write operation. Specifically, the last digit received from the I/O control is returned to the control to be formatted into the result descriptor.

The D register operates in both a D-set mode and in a decrement mode. The D-set mode is used to strobe data from the bus into the register or to force the register to either a value of 10 or the hexadecimal value C. The hexadecimal value C is the EON code which under certain circumstances must be transferred to the 801 unit. The register is forced to a hexadecimal 10 (1010) when operating with a Burroughs data set in order to dial the digit.

Burroughs data sets with autodialing capability pulse the Data Terminal Ready line in order to dial a digit. This procedure is similar to the operation of rotary dial mechanism. If the digit to be pulsed is in the range 1 through 9, the Data Terminal Ready line is pulsed the number of times defined by the integer value of the digit. If the digit is 0, the Data Terminal Ready line must be pulsed 10 times. Consequently, the D register is examined after a dial digit is received from the control. If the dial digit is 0, the D register is forced to (hex) 10.

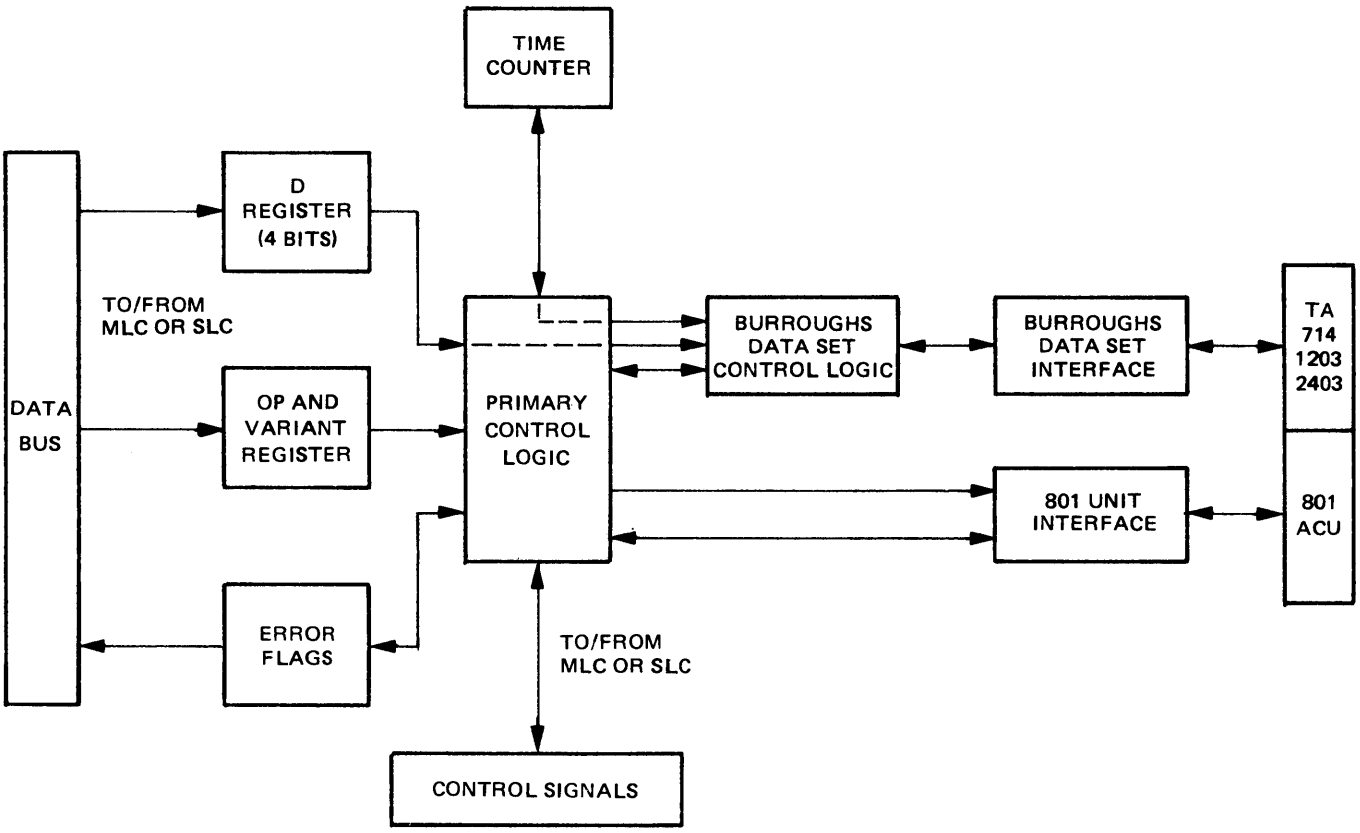


Figure 8-6. Block Diagram, ADO Line Adapter

When operating with Burroughs data sets, the D register is decremented with each on-off transition of Data Terminal Ready until the value contained in the D register equals 1. Neither the decrement mode of operation nor the force-to-10 operation is used when operating with an 801 unit.

OP and Variant Register

The OP and Variant register consists of a 4-bit latch. The latch is used to store the AA variants, the W variant, and a Write/Test bit. Write/Test bit equal to 1 denotes Write; 1 denotes Test.

Time Counter

Time-related signals generated by the 10-bit Time Counter are described in the subsections that follow.

60 msec, 100 msec

This delay is used to toggle the Data Terminal Ready line when operating with a Burroughs data set. DTR is off for 60 milliseconds, then it is switched on. The Time Counter continues to run. After 100 milliseconds, DTR is switched off. Therefore, the DTR cycle is 60 milliseconds off followed by 40 milliseconds on. Both signals are clocked by the crystal-controlled oscillator used to generate slow clocks.

324 msec +0/-81 msec

This is a delay between the reception of an I/O initiate at the beginning of the dialing process to allow the local exchange to clear from the previous call. This delay is necessary if a call is terminated and followed immediately by the initiation of a dialing operation.

729 msec +0/-81 msec

This period, used as the delay between digits (interdigit delay), is generated only for operation with Burroughs data sets.

1 second +0/-81 msec

This delay is used to sample the received data line when operating with a Burroughs TA714 data set. The TA714 data set call establishment occurs when the received data line goes from MARK to SPACE condition and remains in the SPACE condition for from 2 to 5 seconds. The 1-second time period begins at the MARK-to-SPACE transition. After 1 second, the received data line is checked to determine if it is still at SPACE level. If not, the initial MARK-to-SPACE transition is assumed to have been a transient condition due to line noise.

3 seconds +0/-81 msec

This delay is used in conjunction with the 324-millisecond delay to provide an additional delay of 3 seconds between the reception of an I/O initiate and the beginning of the dialing process. The delay is required only with Burroughs data sets, which do not detect dial tone (801 units detect dial tone and emit a signal on detection), to cover the interval between going "off hook" and the arrival of the dial tone. This delay is also used for the tandem dialing function.

20 seconds +0/-81 msec

This delay is used if the ADO adapter is strapped for end-of-number operation. In this situation, DSS is raised immediately following transfer of the EON code from the ADO adapter to the 801 unit, but call establishment does not occur immediately. This delay provides time needed for the call to be established.

60 seconds +0/-81 msec

This delay is used to force termination of the operation if the external device fails to communicate to the ADO adapter within 60 seconds. Normally the call is established or an Abandon-Call-and-Retry signal is returned from an 801 unit within 40 seconds. The operation terminates after 60 seconds if (1) a failure has occurred in the 801 unit or (2) the Burroughs data set has established a connection within 60 seconds. If a Burroughs data set is being used this timeout provides the only means of determining that the call has not been established.

801 Unit Interface

The 801 unit interface block consists of the driver and receive circuits necessary to interface up to four 801 units. Since the ADO adapter can operate with only one unit at a time, this block also includes the logic to selectively operate on the interface lines to only one 801 unit. Interface signals from the ADO adapter to the unselected units are maintained in the off state, interface signals from these units are ignored by the ADO adapter.

Burroughs Data Set Control Logic

The Burroughs Data Set Control Logic (BDSCL) block primarily consists of the logic needed to toggle Data Terminal Ready. In addition, this block contains logic used to control the Originate, Data Mode and Dial Mode lines. Originate and Data Mode are required only by the Burroughs TA714 data set; Dial Mode is required by the Burroughs TA1203 and TA2403 data sets.

This block also includes logic designed to communicate with the Primary Control Logic block (see figure 8-6). The BDSCL interface to the Primary Control Logic block does not differ from the 801 unit interface to this block.

Burroughs Data Set Interface

Most of this block consists of lines routed through two frontplane connectors on the adapter. Other elements are the Originate Flip-Flop (ORGF), the Dial/Data Mode Flip-Flop (DMF), and the Data Terminal Ready Enable Flip-Flop (DTREF).

Primary Control Logic

This block contains the Sequence Counter and the combinatorial elements that control most of the ADO adapter's functions. The BDSCL has its own sequence counter and to some extent runs asynchronously with respect to the primary control logic.

SEQUENCE COUNTER

Figure 8-7 shows sequence count flows for the ADO adapter in operation with the 801 unit (A) and in operation with a Burroughs unit (B).

Referring to figure 8-7A, once the adapter is initiated by an ACL signal from the SLC or MLC and the status is returned to the control, the adapter enters SC01 to monitor the 801 unit levels, which determine whether a dialing sequence is to begin or the operation (normally, a Write) is to be aborted.

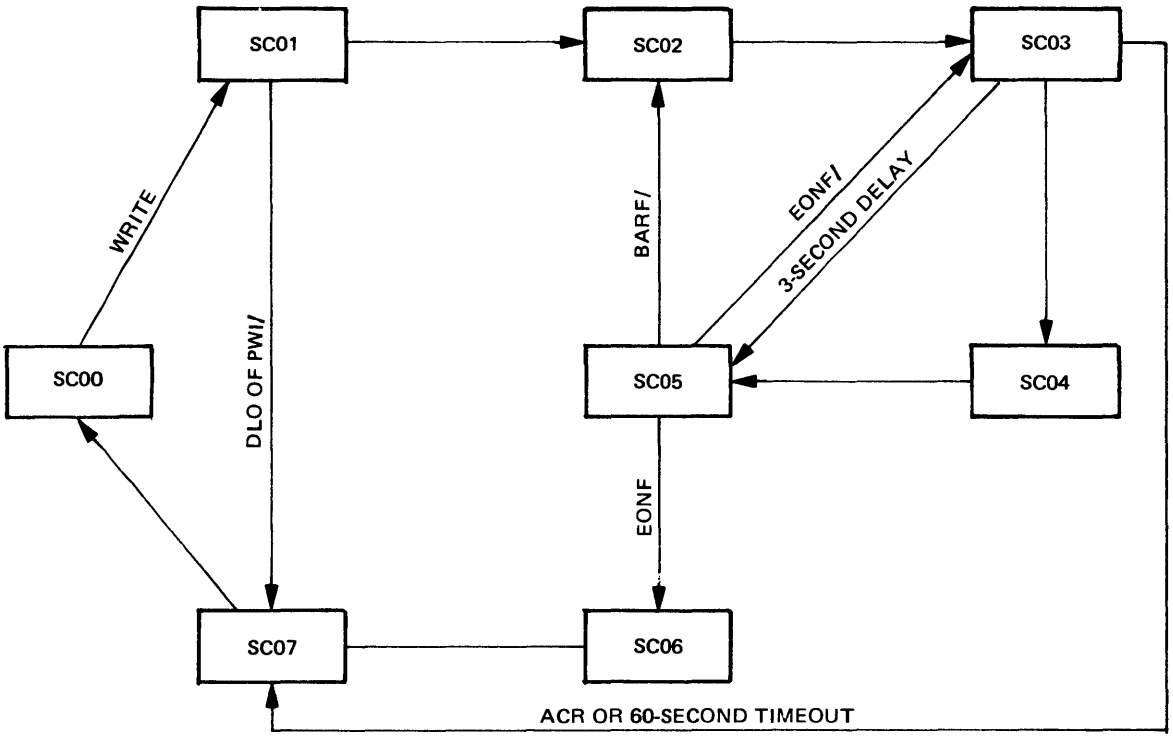
A normal operation causes the adapter to advance sequentially from SC01 through SC07 to SC00. Any exception condition causes an abort to SC07, where the ADO adapter is cleared and goes idle (SC00).

Referring to B (note that the counts are labelled BSC for Burroughs sequence count), the count emulates the responses of an 801 unit in order to enable the ADO to complete the dialing function. The sequence count flow (BSC0 through BSC6), which runs asynchronously with reference to SC00 through SC07 (figure 8-7), is implemented whenever a Burroughs data set is selected as an external device. Normally, the adapter advances from BSC0 through BSC6. Any exception condition resets the BSC counter and causes the 801 sequence to abort through SC07 and go idle at SC00.

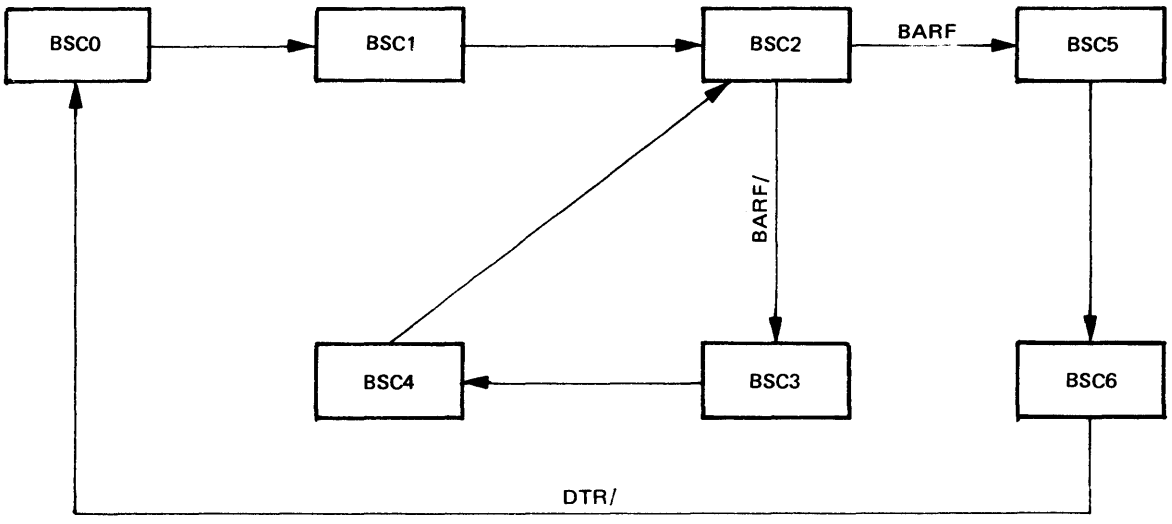
MAINTAINABILITY

The ADO adapter can be tested with the Burroughs B 1800/B 1700 field card tester. A small amount of additional logic has been included on the adapter so that the EIA RS-232 receiver and driver chips can be exercised at the field card test level.

Testing at a level that approximates the operating environment is done by using the Diagnostic Test and Diagnostic Write operations.



A. SEQUENCE COUNTS FOR 801 UNIT



B. SEQUENCE COUNTS FOR BURROUGHS DATA SETS

G12118

Figure 8-7. Basic Sequence Count Flows; ADO Adapter

SECTION 9
TTY DIRECT ASYNCHRONOUS LINE ADAPTER

INTRODUCTION

The TTY Direct Asynchronous (TTY/DIR) line adapter provides an interface between a single-line or multi-line control and Teletype* Model 33, 35, and 37 units. This line adapter provides data character synchronization, vertical parity generation (Write operation), vertical parity checking (option selected by a variant in the Read operator), and identification of ASCII control characters.

A 2-wire cable is used to connect the adapter to a peripheral device. (No data set is required.) Maximum cable length permissible is 1000 feet (305 meters).

UNIT IDENTIFICATION

The TTY/DIR line adapter, contained on one logic card, is identified by the 8-digit Manufacturing and Engineering (M&E) number 2201 2363. This number is imprinted on the metalized unit identification label that is supplied as part of the Field Test and Reference FT&R) documentation. When the adapter is installed, this label is affixed on the end of the 28-position card housing assembly that contains the line adapter.

CONTROL CODE SENSITIVITY

Control code sensitivity for the TTY/DIR line adapter is listed in table 9-1.

Table 9-1. TTY/DIR Line Adapter Control Codes

Function	Code
Starting code	Not required; the TTY/DIR line adapter does not accumulate a BCC.
Ending code	EOT, DC1, EXT, ETB, ENQ, NAK, ACK, or (optionally) CR.
Positive response code	ACK
Negative response code	DEL

The TTY/DIR line adapter and the attached device use ASCII-7 as a communication code. Each character transmitted between the line adapter and the peripheral device consists of either 11 or 10 consecutive bits. An 11-bit character (used with either a Model 33 or a Model 35 Teletype) consists of one start bit, seven data bits, one parity bit, and two stop bits. A 10-bit character (used with a Model 37 Teletype consists of one start bit, seven data bits, one parity bit, and one stop bit.

*Registered Trademark of Teletype Corp.

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

Read

The Read operator accepts data from the remote device and stores it into ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

000- T0D- CEVV 0--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII to EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
C = 0: Do not check character parity.
= 1: Check character parity.
E = 0: Ignore CR as a response code.
= 1: Recognize CR as a response code.
VV=00: Normal linking.
=01: If non-negative response is received, the Linking Terminated bit (result descriptor) is set and linking is terminated.
=10: If non-positive response is received, the Linking Terminated bit is set and linking is terminated.
=11: Undefined.

Write

The Write operation causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B-minus-1th location is reached.

Write is generally terminated by the transmission of an ending control code (normally CR).

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the result descriptor for the terminated operation.

010- T000 000- 0000 0--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.

Break (Disconnect)

The Break operator terminates the in-process operation, if any, and transmits a Break signal to the remote terminal. A Break signal is a sustained transmission of spacing for either 32 bits (transmit) or 15 bits (receive). The result descriptor for a Break operation is returned after the adapter has failed to receive data for 600 msec for transmit and for a period equivalent to 11 bits for receive.

1100 00-- ---- ---- ---- UUUU

Test

The Test operator is a request for the reporting (in the result descriptor) of the adapter's identification.

1000 0000 0--- ---- ---- UUUU

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the TTY/DIR line adapter are listed below, together with their meanings when set. Omitted bits in the 0-23 sequence are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception conditions. (For all operators except Test, this bit is set if any of bits 2-15 are set.)
3	Vertical character parity error or BCC error (Read).
4	Memory access error (Read).
5	Memory parity error (Write).
6	Time-out (Read or Write).
7	Break received (Write).
8	Ending control code expected but not received (Read or Write).
9	Linking terminated (Read; VV = 01 or 10).
11	Loss or absence of Data Set Ready (Read, Write, Break).
16	Operation complete.
17	I/O control is present (Test).
18	Line indicator; 0 = direct line (Test).
19-23	Adapter ID (Test): 01000 = TTY/DIR adapter.

FUNCTIONAL DESCRIPTION

The two basic modes of operation for the TTY/DIR line adapter are Read and Write. During a Write operation, each character is transferred in parallel from the control and stored in a data register in the line adapter. Each character is then shifted bit-serially to the communications line, with the adapter generating the appropriate start and stop bits. The line adapter also generates vertical parity (7-bit ASCII code plus one parity bit) for each character.

The transfer rate is determined by an adjustable timer located in the line adapter. This timer must be strapped to provide the correct bit interval required by the communications device.

During a Read operation, data from the communications device is transferred bit-serially to the line adapter. Bits are stored sequentially in the data register until a complete character is accumulated. The line adapter checks the vertical parity of each character as it is received.

When the data register contains a full character (7-bit ASCII code plus a parity bit) the line adapter sends a "request to transfer character" signal to the data communications control (SLC or MLC).

The line adapter also provides identification of control code characters transmitted to or from the communications device.

Sequence Counter

Operations of the TTY/DIR line adapter are primarily controlled by a 16-bit sequence counter contained in the line adapter. The actual sequence this counter follows is determined by the type of operation to be performed and conditions that occur during execution of the I/O operator. Figure 9-1 is simplified flow diagram of sequence counter operations. Counter operation is described in the subsections that follow.

Figure 9-2, at the end of this section, is a detailed flow diagram of the sequence count functions.

SC00

The line adapter waits for control (ACL). Upon receipt of ACL, the line adapter is initialized with both the OP code and variants. The exit from SC00 is via SC01.

SC01

Adapter ID is sent to the control. The exit from SC01 is via SC02.

SC02

SC02 is the Op code interpretation state. The three least significant bits of the D Register are decoded to indicate what operation is to be performed. The adapter exits from SC02 as follows:

TEST: CD2 = 1; exit is via SC00.
READ: CD2 = 0; exit is via SC11.
BREAK: CD2 = 3; exit is via SC04.
WRITE: CD2 = 2; exit is via SC12.

SC04

SC03 is the transmit Break state. The data line is held at ground potential for 648 milliseconds. Exit from SC04 is via SC05.

SC05

Adapter status is sent to the control prior to the completion of the operation. The exit from SC05 is via SC00.

SC08

The adapter is synchronized to the bit rate of a received character. The character is shifted into the D Register until the flag bit (D1=1) is detected. The exit from SC08 is via SC09.

SC09

SC09 is the character recognition state. The received character is checked for control significance, and the adapter requests character service (CRL). Exit from SC09 is via SC11.

SC11

SC11 is the character transfer state for a Read operation. The adapter transfers characters until the B Address (BARF) is reached or a character time-out occurs. Exits from SC11 are as follows:

SC05: After a 40-second time-out period during which no characters are received, or whenever a terminate condition occurs.

SC08: The normal exit path to receive the next character from the line.

SC12

The adapter requests and accepts characters from the control. The exit from SC12 is via SC13.

SC13

The adapter sets flags indicating the polarity or type of control code encountered. The exit from SC13 is via SC14.

SC14

The adapter loads and transmits a start bit (SPACE) prior to the transmission of data. Exits from SC14 are as follows:

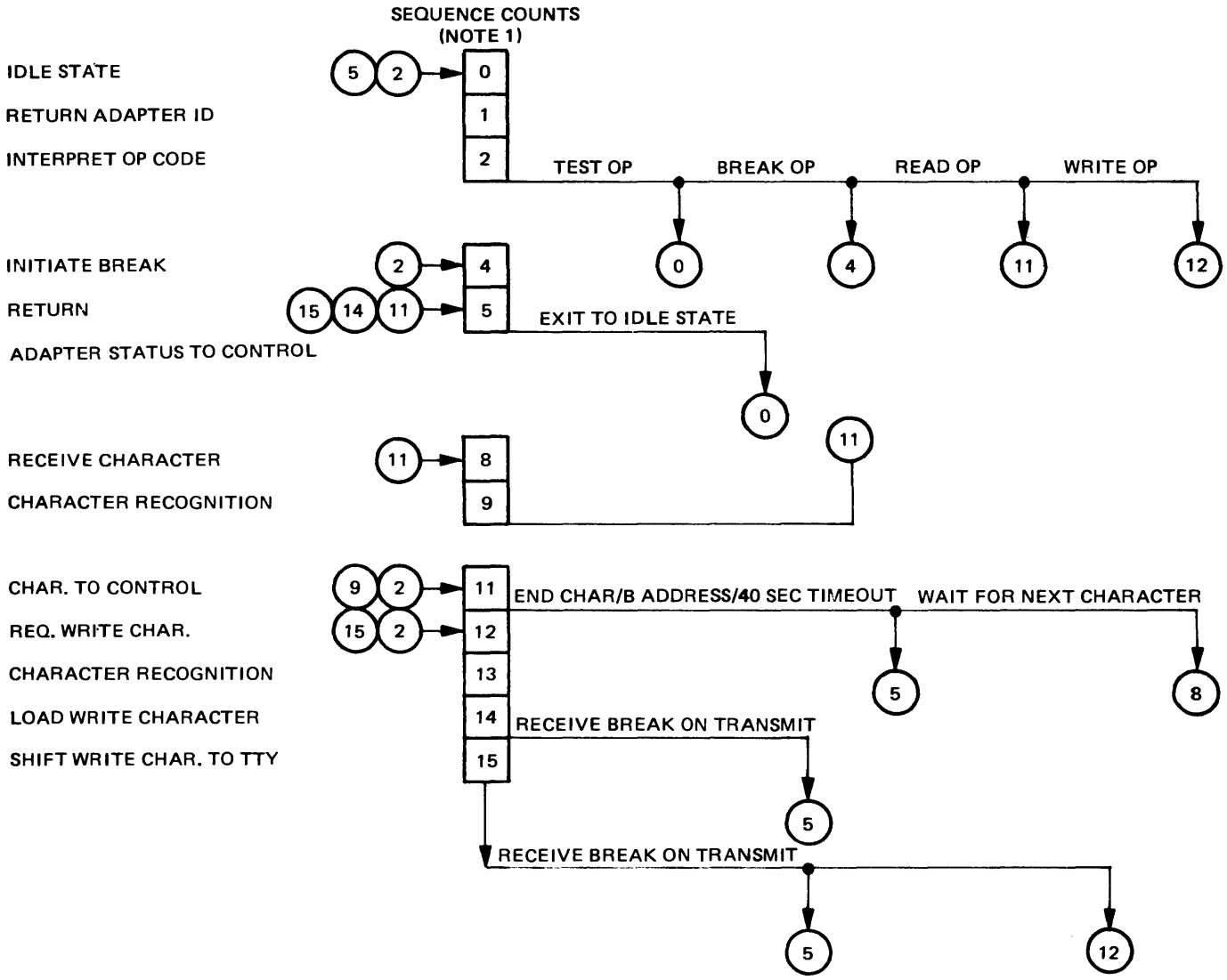
SC05: Receive Break detected.

SC15: Normal exit.

SC15

The adapter shifts the character onto the line. Parity is generated and either one or two stop bits (MARKs) are transmitted at the end of the data. Exits from SC15 are as follows:

SC05: Receive Break detected (terminate condition).
SC12: Normal exit from SC15 to transmit next character.

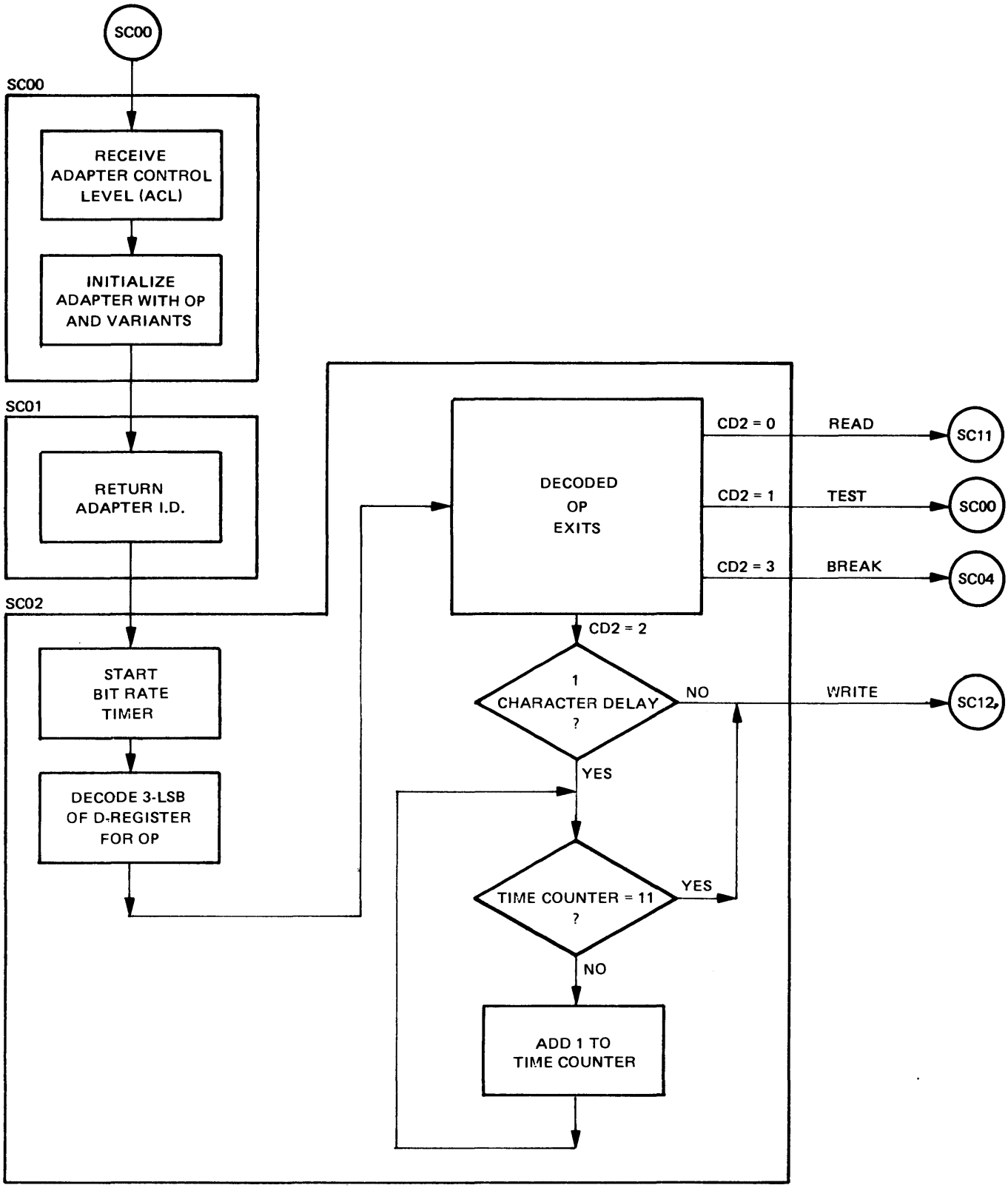


NOTES

1. ONLY THE SEQUENCE COUNTS THAT ARE ACTUALLY USED ARE LISTED.
2. CONSECUTIVE SEQUENCE COUNTS (BOXED NUMBERS) INDICATE NORMAL SEQUENCE COUNT PROGRESSION UNLESS OTHERWISE SPECIFIED BY A BRANCH CONDITION.
3. NAMES TO THE LEFT OF EACH COUNT INDICATE THAT COUNT'S BASIC FUNCTION.
4. CIRCLED NUMBERS TO THE RIGHT OF THE COUNTS INDICATE POSSIBLE EXITS.
5. CIRCLED NUMBERS TO THE LEFT OF THE COUNTS INDICATE BRANCH POINTS TO THE SEQUENCE COUNT.

G12107

Figure 9-1. Basic Sequence Count Flow, TTY/DIR Line Adapter



G12108/SHEET 1 OF 8

Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 1 of 8)

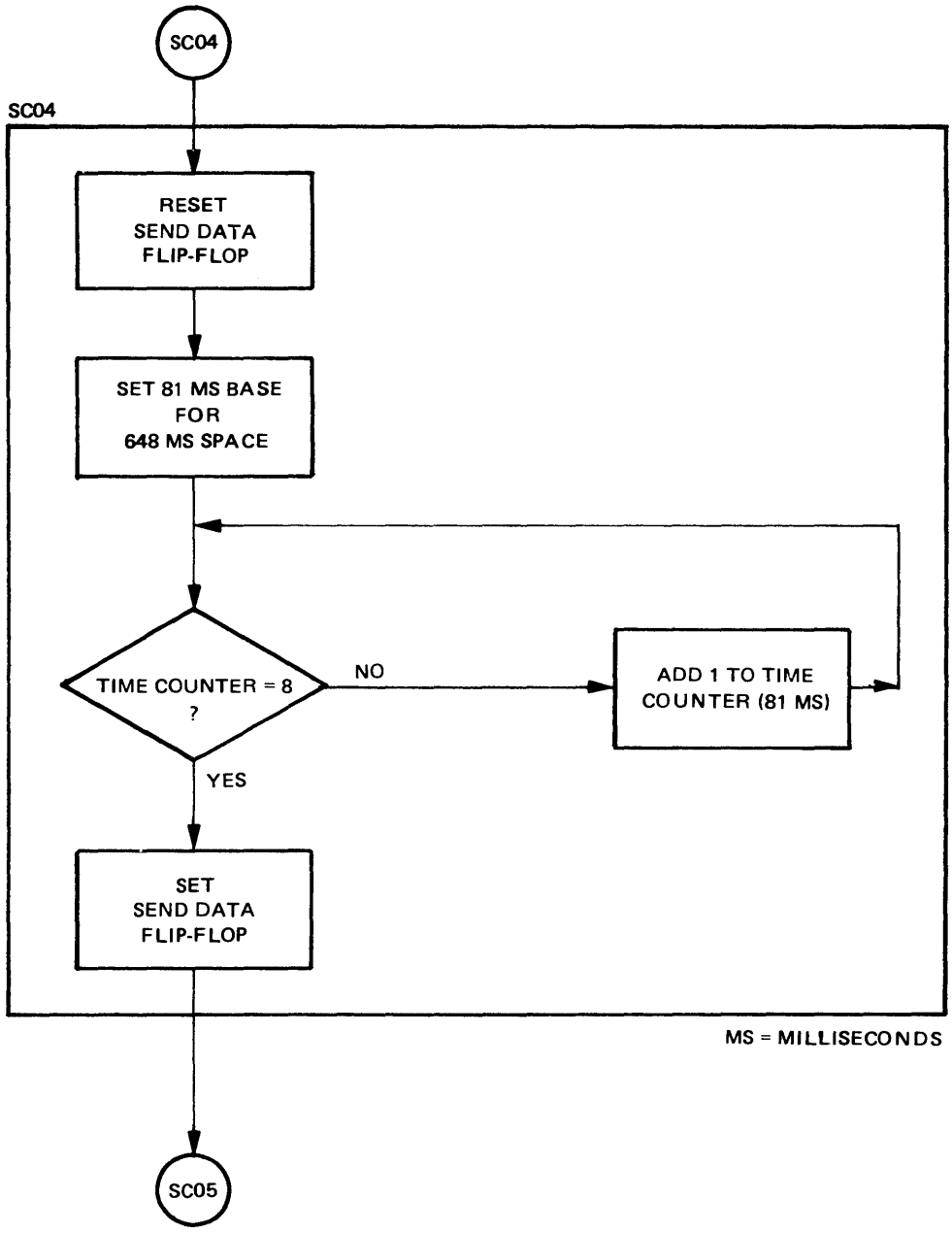


Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 2 of 8)

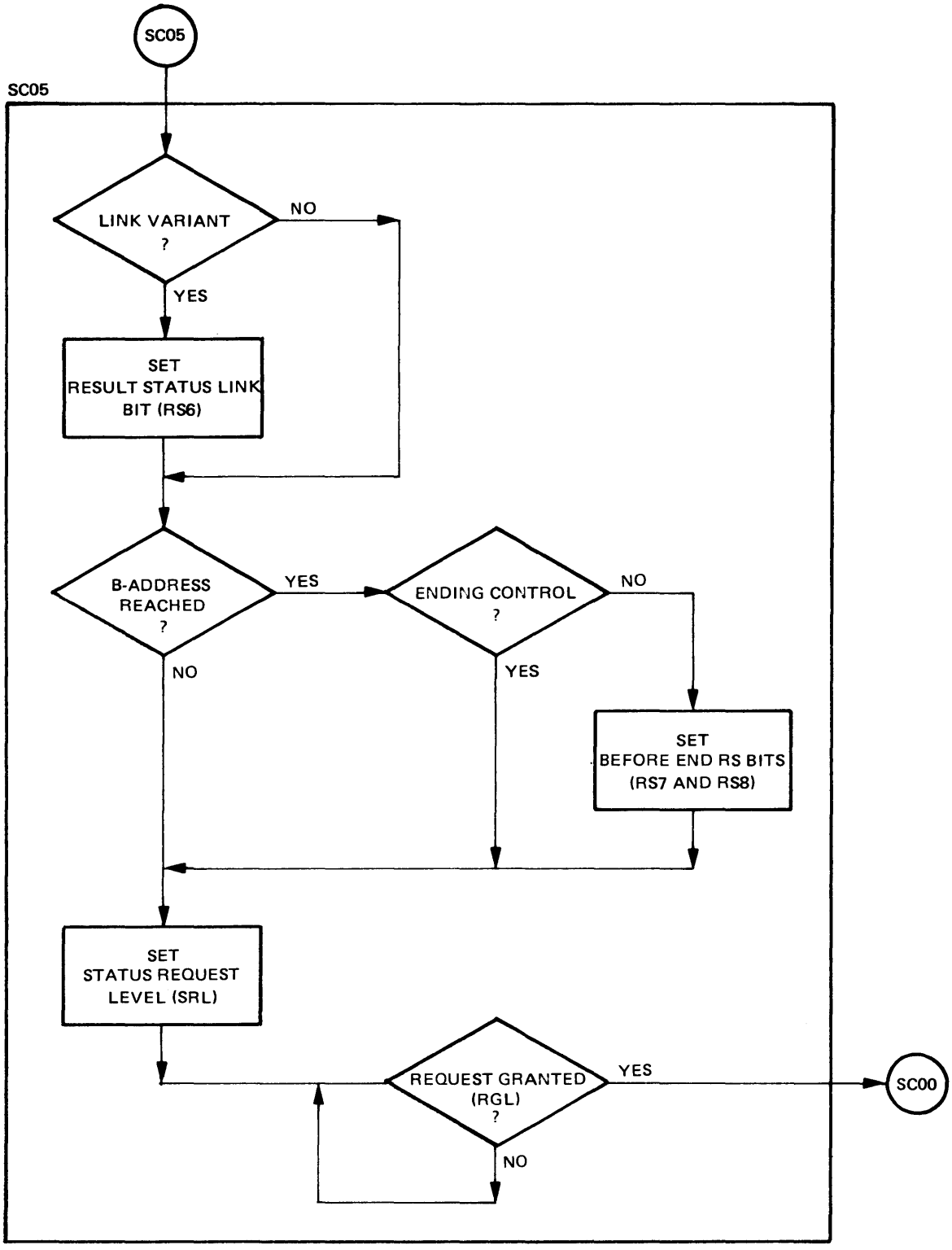
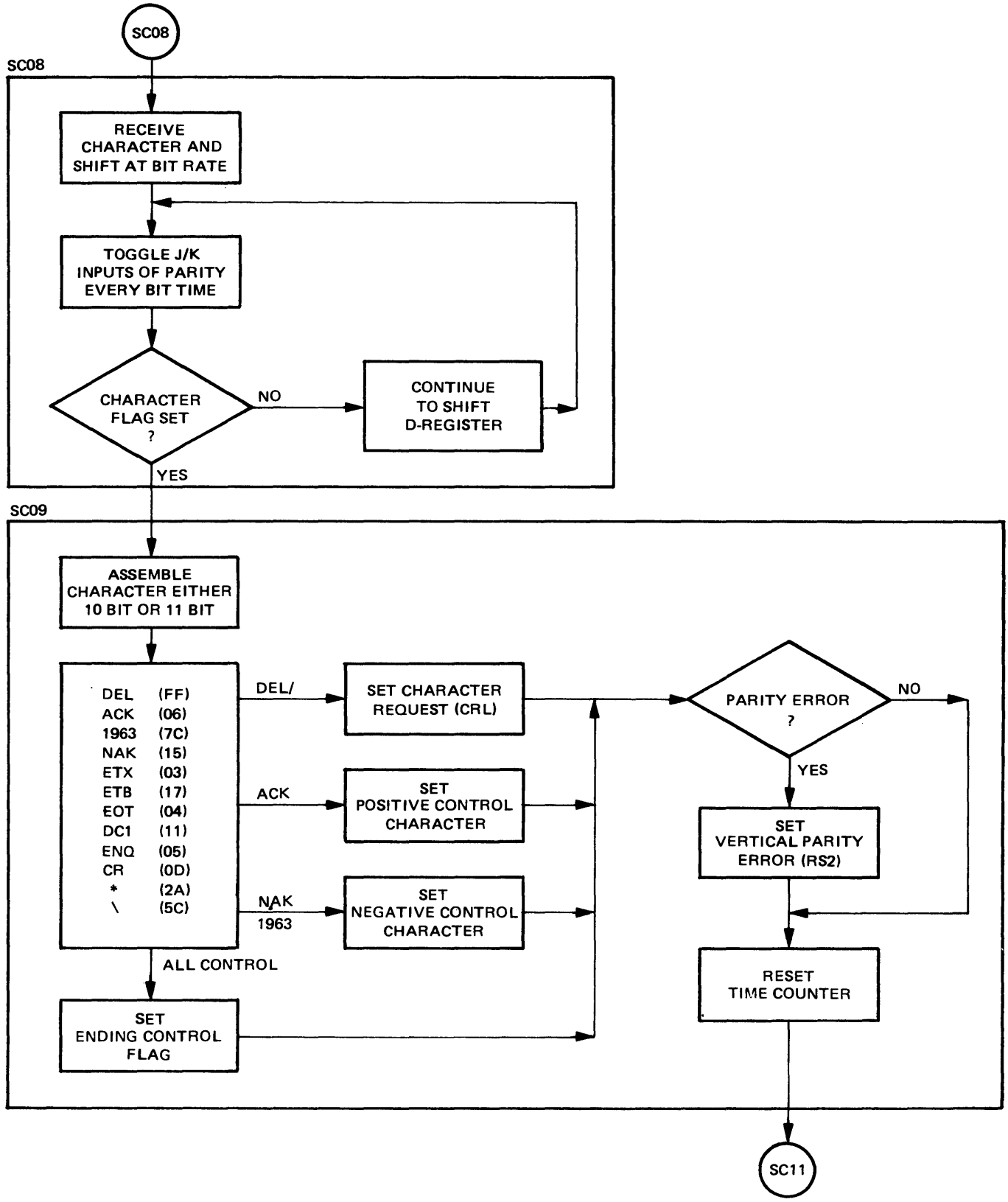
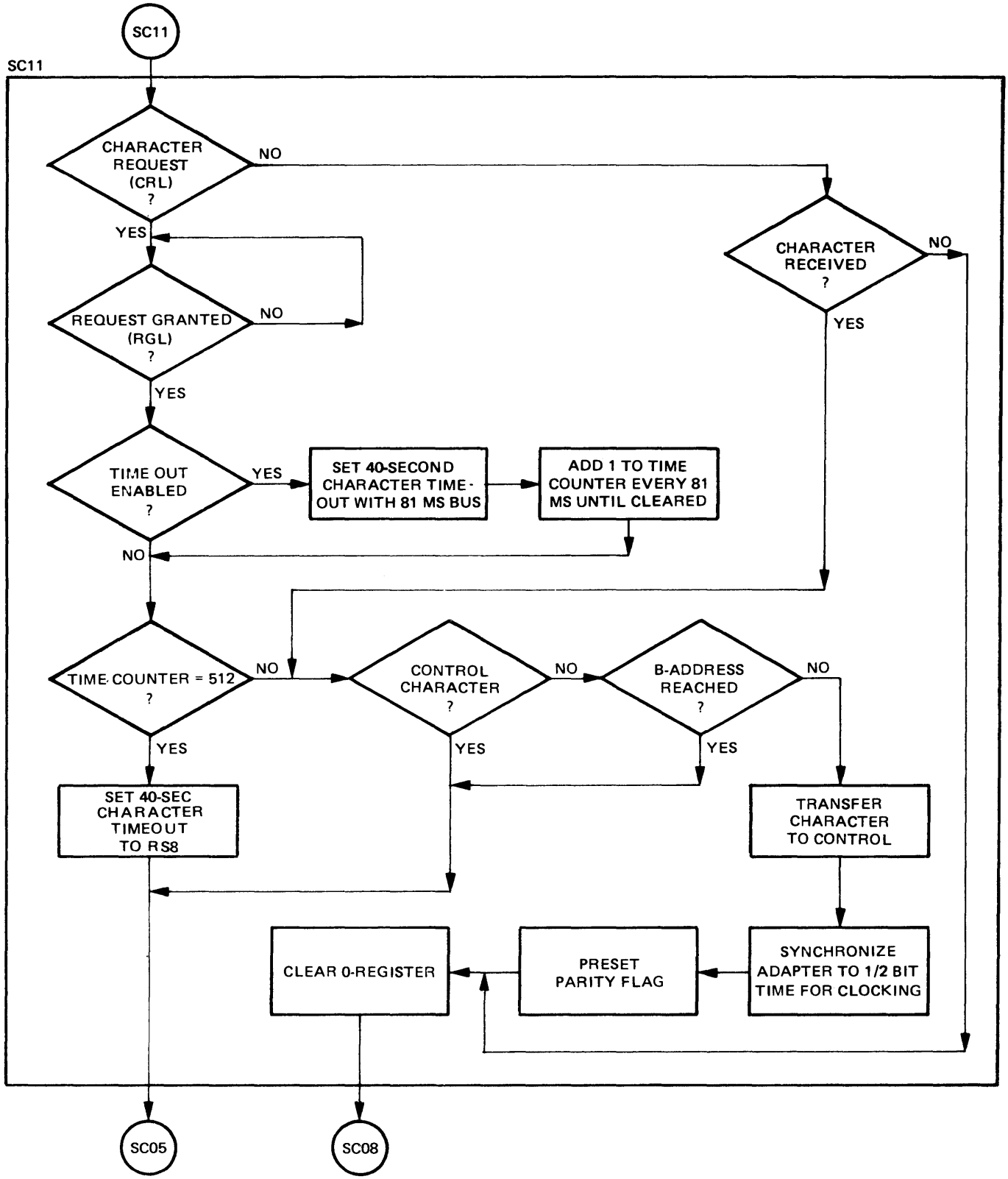


Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 3 of 8)



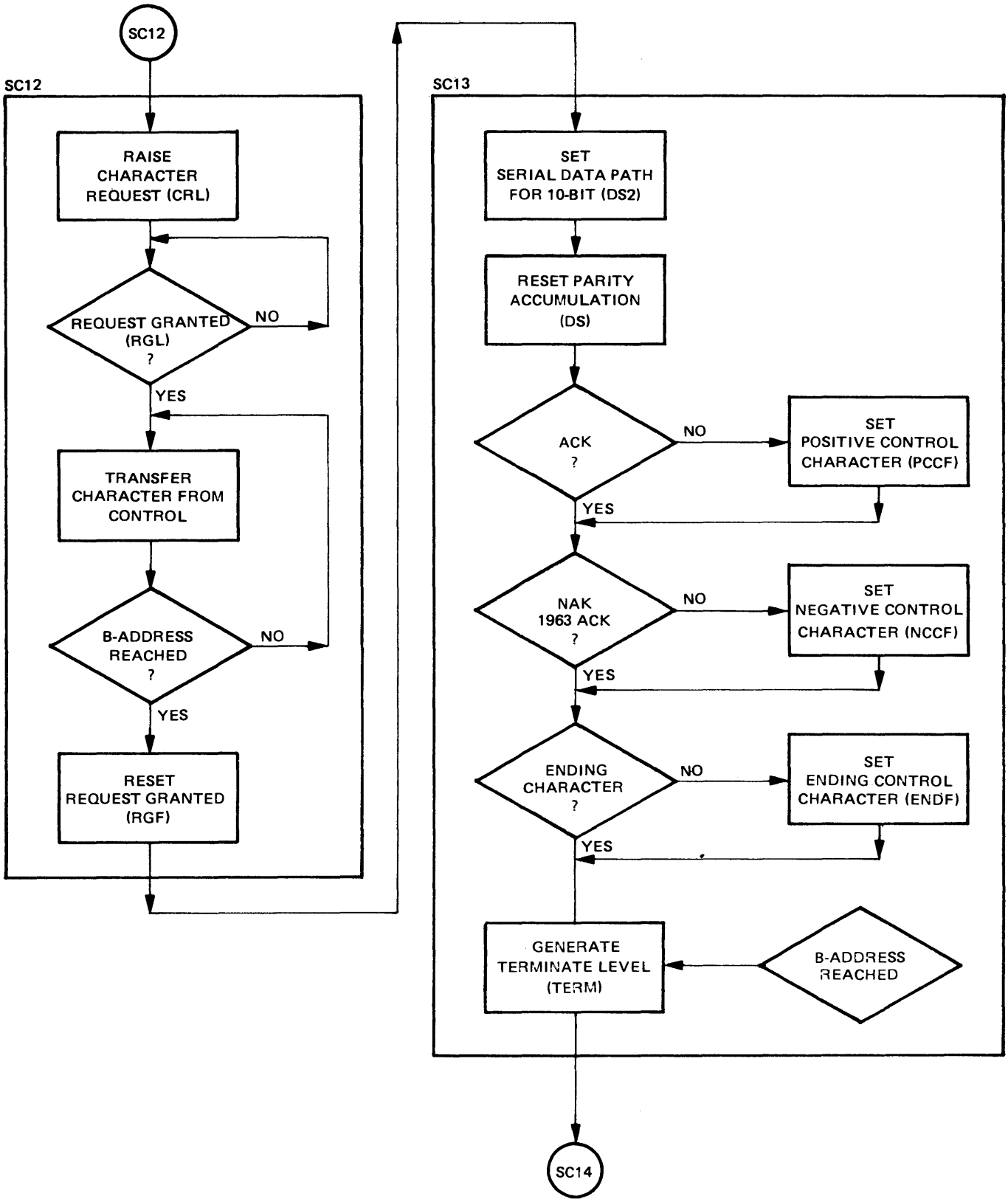
G12108/SHEET 4 OF 8

Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 4 of 8)



G12108/SHEET 5 OF 8

Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 5 of 8)



G12108/SHEET 6 OF 8

Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 6 of 8)

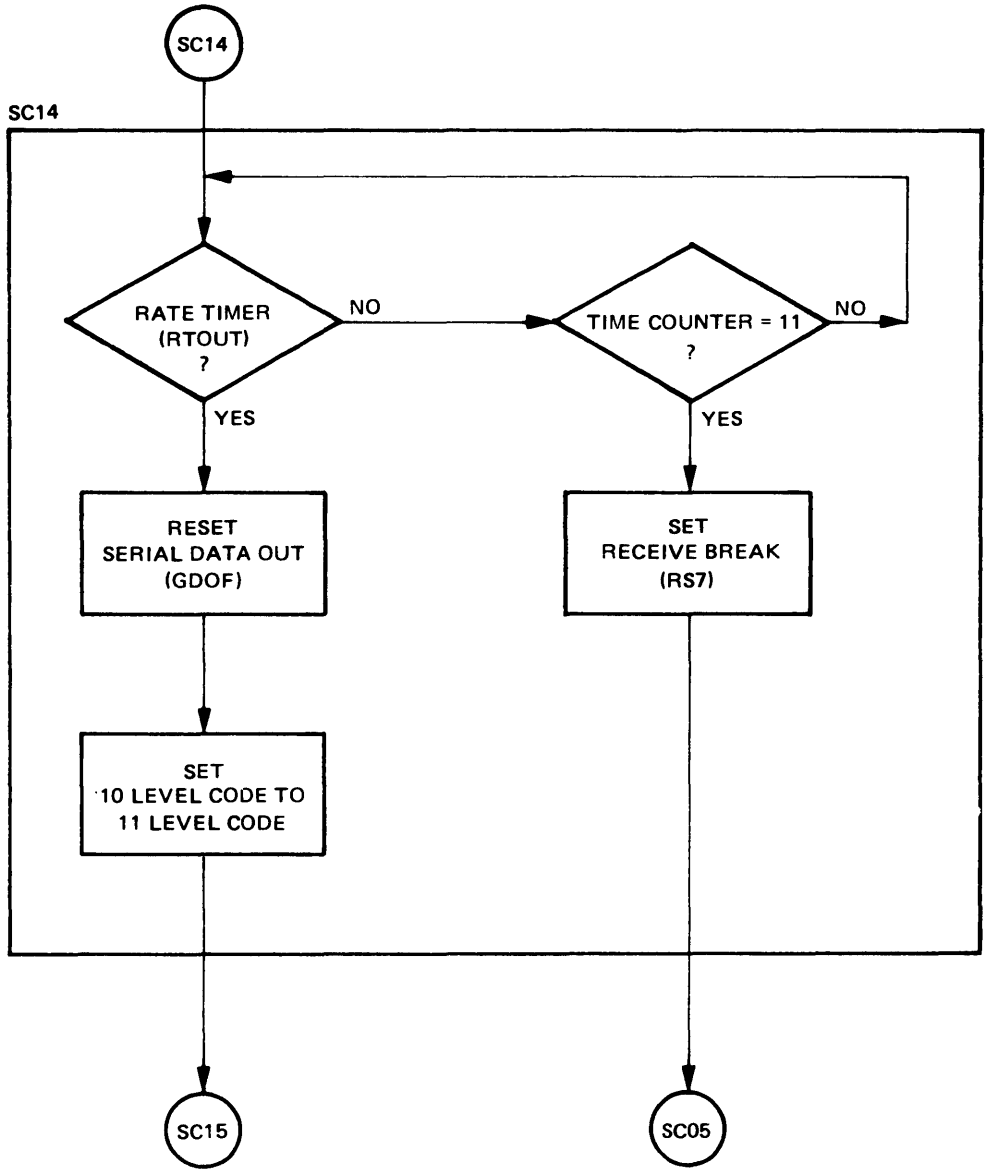


Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 7 of 8)

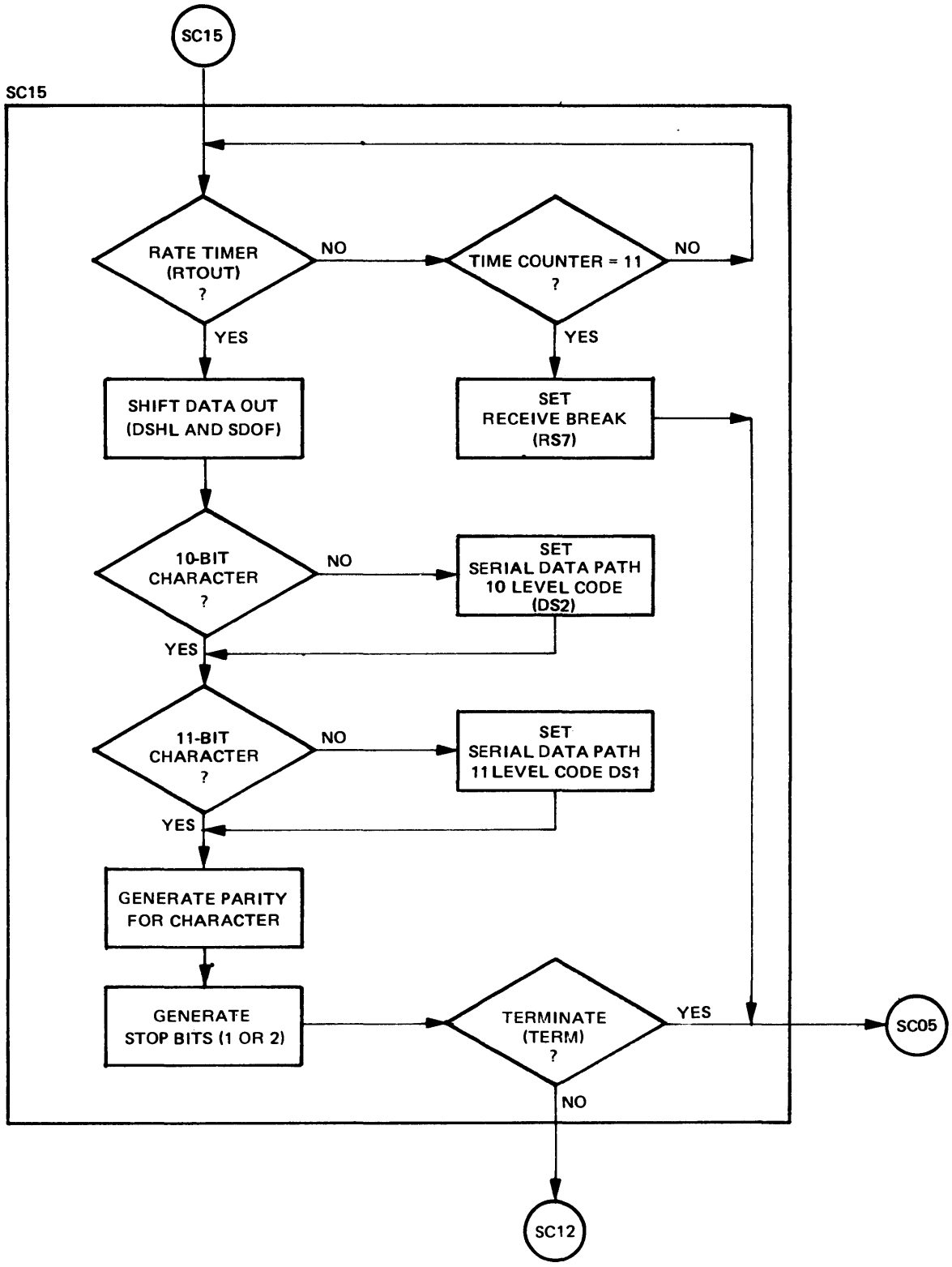


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Figure 9-2. Detailed Flow Chart, TTY/DIR Line Adapter (Sheet 8 of 8)

SECTION 10
TTY ASYNCHRONOUS LINE ADAPTER

INTRODUCTION

The TTY Asynchronous (TTY/ASYN) line adapter provides an interface between a single-line or multiline control and Teletype Model 33, 35, or 37 units. This adapter provides (1) data synchronization, (2) vertical parity generation (Write operation), (3) vertical parity checking (option selected by a variant in the Read operator), and (4) identification of ASCII control characters.

The TTY/ASYN line adapter connects to a data set employing an RS-232-C interface. Some of the data sets that can be used with the TTY/ASYN line adapter are listed in table 10-1.

Table 10-1. Data Set Characteristics, TTY/ASYN Line Adapter

Speed (bps)	Service	Data Sets
110, 150, 300	Dial (DDD)	WE103A
110, 150, 300	Leased	WE103F, WE202D, TA713/753
110	TWX-CE	WE103E
110	TWX-CPT	WE81181/2/3/4

UNIT IDENTIFICATION

The TTY/ASYN line adapter, contained on one logic card, is identified by the 8-digit Manufacturing and Engineering (M&E) number 2201 2355. This number is imprinted on the metalized unit identification label that is supplied as part of the Field Test and Reference (FT&R) documentation. When the adapter is installed into the system, the identification label is mounted on the end of the 28-card housing assembly that contains the line adapter.

CONTROL CODE SENSITIVITY

Control code sensitivity for the TTY/ASYN line adapter is listed in table 10-2. This adapter and its peripheral devices use ASCII-7 as a communication code. Each character transmitted between the line adapter and the peripheral device consists of either 11 or 10 consecutive bits. An 11-bit character (used with either a Model 33 or a Model 35 Teletype) consists of 1 start bit, 7 data bits, 1 parity bit, and 2 stop bits. A 10-bit character (used with a model 37 Teletype) consists of 1 start bit, 7 data bits, 1 parity bit, and 1 stop bit.

Table 10-2. Control Codes, TTY/ASYN Line Adapter

Function	Code
Starting code	Not required; TTY/ASYN does not accumulate a BCC.
Ending code	EOT, DC1, EXT, ETB, ENQ, NAK, ACK, or (optionally) CR.
Positive response code	ACK
Negative response code	DEL

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

Read

The Read operator causes data to be accepted from the remote device and stored into ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

000- T0D- CEVV P--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII to EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
C = 0: Do not check parity.
= 1: Check parity.
E = 0: Ignore CR as an ending code.
= 1: Recognize CR as an ending code.
VV=00: Normal linking.
=01: If non-negative response is received, set linking terminated bit (result descriptor) to 1 and terminate linking.
=10: If non-positive response is received, set linking terminated bit to 1 and terminate linking.
=11: Undefined.
P = 0: Do not Poll.
= 1: Poll.

Write

The Write operation causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B-minus-1th location is reached. The Write operation is ordinarily terminated by the transmission of an ending control code character (normally CR).

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the result descriptor for the terminated operation.

010- T000 000- 0000 0--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.

Break (Disconnect)

The Break operator terminates the in-process operation, if any, and transmits a Break signal to the remote terminal. A Break signal is a sustained transmission of spacing for either 32 bits (transmit) or 15 bits (receive). The result descriptor for a Break operation is returned after the adapter has failed to receive data for the following time periods:

MODEL 37: Transmit: 486-567 msec; receive: 255 msec
OTHER SETS: Transmit: 255 msec; receive: 127 msec

1100 00-- ---- ---- ---- UUUU

Test

The Test operator is a request for the reporting (in the Result Descriptor) of the adapter's identification and the conditions specified by the V and M variant combination.

100V --M- ---- ---- ---- UUUU

VM=00: Complete the operation normally. Do not change the status of the Data Terminal Ready signal.
=01: Make the Data Terminal Ready signal true, then complete the operation.
=10: Make the Data Terminal Ready signal false, then complete the operation.
=10: Forbidden – causes adapter to wait "forever."

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the TTY/ASYN line adapter are listed below, together with their meanings when set. Omitted bits in the 0-23 sequence are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception conditions. (For all operators except Test, this bit is set when any of bits 2-15 are set.)
3	Character vertical parity or block check error (Read).
4	Memory access error (Read).
5	Memory parity error (Write).
6	Time-out (Read or Write).
7	Break received (Write).
8	Ending control code expected but not received (Read or Write).
9	Linking terminated (Read; VV = 01 or 10).
11	Loss or absence of Data Set Ready signal.
12	Loss of carrier (Read) or loss of Clear To Send (Write)
16	Operation completed..
17	I/O control is present (Test)
18	Line indicator: 0 = leased line, 1 = switched line (Test)
19-23	Adapter ID (Test): 000000 = adapter not present 010000 = TTY/ASYN adapter

FUNCTIONAL DESCRIPTION

General Information

The TTY/ASYN line adapter provides an RS-232-C interface between the data communications control and an asynchronous data set. The data set that is connected to the other end of the communications line must provide an interface to either a Model 33, 35, 37 Teletype unit or a communications device employing the same type of interface.

This line adapter has two basic modes of operation, Read or Write. During a Write operation, a write character is loaded (in parallel) from the I/O control into the line adapter's data register. The line adapter generates the appropriate start and stop bits as the character is transferred bit-serially from the data register to the data set. The line adapter also generates vertical parity (seven bit ASCII code plus one parity bit) for each character.

The Write data transfer bit-repetition rate is determined by an adjustable timer located in the line adapter. This timer must be strapped to provide the interval required by the communications device connected to the other end of the communications line.

During a Read operation, data from the communications device is transferred bit-serially to the line adapter. The read bits are stored sequentially in the data register. The line adapter checks the parity of each character. When the data register contains a complete character, the line adapter indicates to the I/O control that a character is available for transfer.

The line adapter also provides identification of control code characters transmitted by either the I/O control or the communication device.

Sequence Counter

Operations of the TTY/ASYN line adapter are primarily controlled by a 16-bit sequence counter contained in the line adapter. The actual sequence this counter follows is determined by the type of operation to be performed and conditions that occur during execution of the I/O operator. Figure 10-1 is a simplified flow diagram of sequence counter operations. Figure 10-2, at the end of this section, is a detailed flow diagram of the actions of this counter. The paragraphs that follow figure 10-1 provide count-by-count descriptions of counter action.

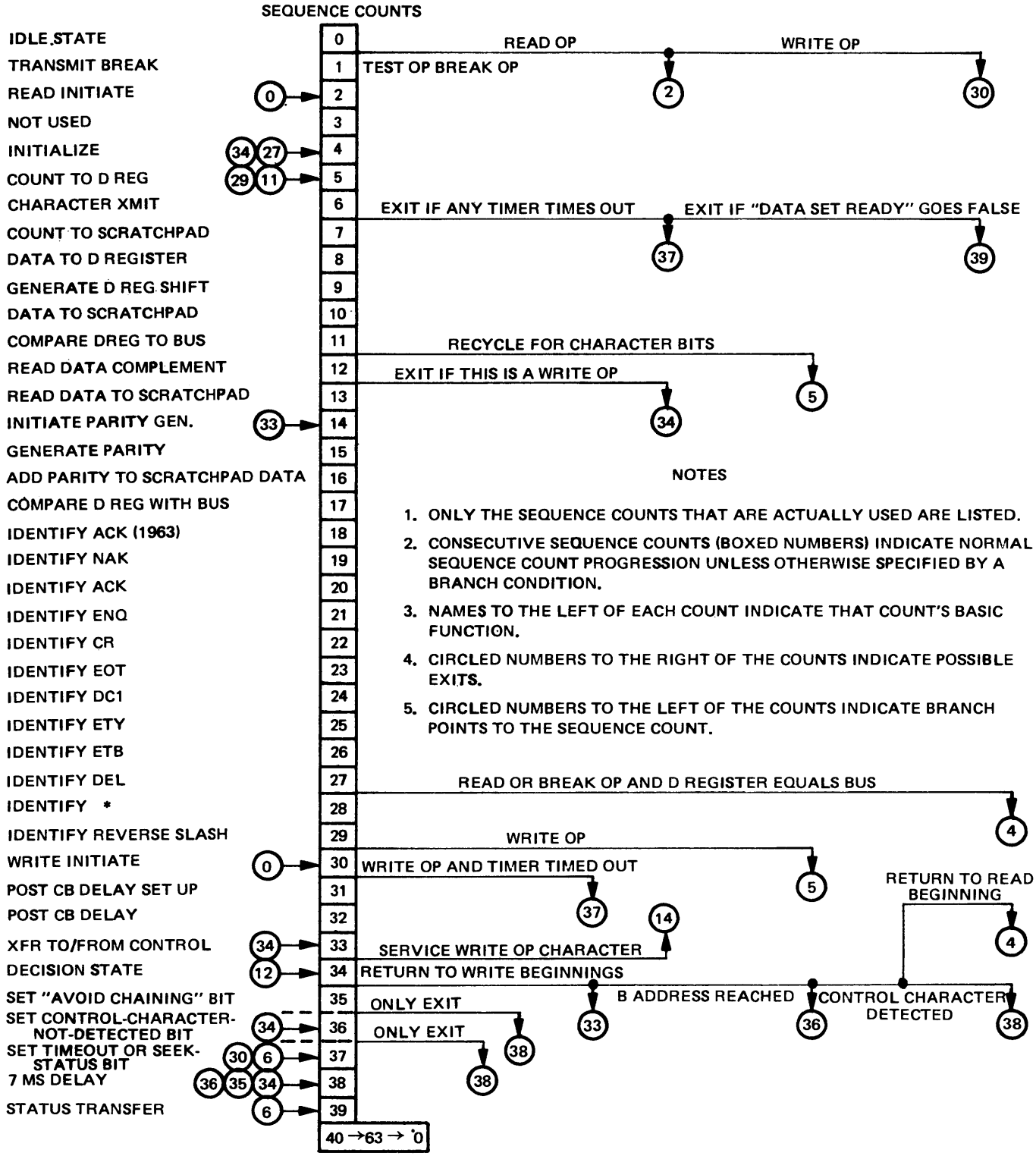

Figure 10-1. Basic Sequence Count Flow, TTY/ASYN Line Adapter

SC01

At SC01, the adapter is in the break-transmission state. Either a normal Break (256 ms) or a long break (656 ms) is transmitted. The exit from SC01 is via SC02 when the Break timer times out.

SC02

SC02 is the Read-initiate state. The Status Scratchpad (SPM3) is cleared. Exit from SC02 is via SC03.

SC03

SC03 is unused; exit is via SC04.

SC04

At SC04, the adapter is in the Initialization state. The character scratchpad (SPM1) and the time-out scratchpad (SPM2) are cleared. The rate timer (data rate) is also initialized. Serial data timing and shifting begins during this sequence count. The exit from SC04 is via SC05.

SC05

Initialization state, continued. The time-out base for the serial data shift is read to the D Register. Exit from SC05 is via SC06.

SC06

At SC06, the adapter is in the timing state. Received Break time-outs are initiated during a Write operation and 20-second time-outs are initiated for either Reads or Writes. Write data is shifted onto the communications line during this state. The adapter exits from SC06 as follows:

SC07: when a character has been shifted in or out,

SC37: when a time-out has occurred,
SC39: when loss of Data Set Ready (DSR) occurs.

SC07

The time-out value is loaded into scratchpad (SPM2) when a normal exit from SC06 occurs. This value is reinitialized in SC04. The exit from SC07 is via SC08.

SC08

Data is loaded to the D register from scratchpad (SPM1) and start/stop bits are added to the Write data character if End of Character Service (EOCS) is true during a Write operation. Exit is via SC09.

SC09

The D Register is shifted when EOCS is not detected. If a Write operation is being performed, EOCS is reset. The exit from SC09 is via SC10.

SC10

Data is loaded from the D register to the scratchpad (SPM1). Exit is via SC11.

SC11

Character-evaluation state; the logic that compares the D register to the bus is initiated for use by a Write operation. Exit is as follows:

SC05: When any of the following recycle conditions exist:

A Write operation, and the D register and the bus do not compare (WRA and EQ/).

A Write operation, and start/stop bits have been loaded (WT and D9).

A non-Write operation, and no character is detected (WT/ and CDET/).

SC12: The normal exit when a character is evaluated.

SC12

Read data is complemented in the D register. (Data originally enters the D register in inverted form.) Exits from SC12 are as follows:

SC34: Write operation.
SC13: Read operation.

SC13

Read data is loaded into scratchpad (SPM1) from the D register. Exit from SC13 is via SC14.

SC14

Initiate-parity-generation state. The parity generator is reset so that parity can be generated for a new character. Exit from SC13 is via SC15.

SC15

Parity-generation state. The D register is compared to the bus. If they are equal, the adapter exits. If they are not equal, the D register is shifted until they are equal. Exit from SC15 is via SC16.

SC16

Load parity. The parity bit is loaded into bit 08 of scratchpad (SPM1) during a Write operation, and a parity error is loaded into bit 02 of scratchpad (SPM3) if detected during a Read operation. Exit from SC16 is via SC17.

SC17

Reload data. Scratchpad (SPM1) is read onto the bus and loaded into the D register prior to control character recognition. Exit from SC17 is via SC18 through SC29.

SC18

Identify ACK (1963). The 1963 ACK is a negative control character. For 8-bit ASCII, BUS08 is set.

SC19

Identify NAK. NAK (1/5) is a negative control character. For 8-bit ASCII, BUS08 is set.

SC20

Identify ACK. ACK (0/6) is a positive control character.

SC21

Identify ENQ. ENQ (0/5) is an ending control character. ENQF is set when the adapter is in Read-idle.

SC22

Identify CR. CR (0/D) is an ending control character and is detected as such if the identify-carriage-return variant (IDCRU) is set. An 8-bit ASCII code sets BUS08.

SC23

Identify EOT. EOT (0/4) is an ending control character. An 8-bit ASCII code sets BUS08.

SC24

Identify DC1 (XON). DC1 (1/1) is an ending control character.

SC25

Identify ETX. ETX (0/3) is an ending control character.

SC26

Identify ETB. ETB (1/7) is an ending control char The D register/bus compare logic is disabled.

SC27

Identify DEL. The DEL (F/F) character in the D register forces an exit via SC04 whenever the adapter is in the Read mode. Read-idle (RDI) or Break will also force an exit via SC04. This character is not sent to the control during a Read operation.

SC28

Identify asterisk (*, 2/A). The asterisk causes the start/reg logic to be set. If 8-bit ASCII code is used, then BUS08 is set.

SC29

Identify reverse slash (\, 5/C). The reverse slash causes the start/reg logic to be set. If a Write operation is in progress, then EOCSF is set and an exit via SC05 occurs. Otherwise, the exit is via SC30.

SC30

Write-initiate state. A 20-second time-out is initiated and the Write operation waits until the adapter receives a Clear To Send (CTS). Exits from SC30 are as follows:

SC31: Clear To Send or an operation other than Write.

SC37: Time-out, awaiting Clear To Send.

SC31

The post-Clear To Send (CB) delay state. The D register is cleared. Exit is via SC32.

SC32

Continuation of the post-Clear To Send (CB) delay state. A 255 millisecond timer is initiated during a Write operation and the adapter waits until it can exit via SC33. If not a Write or delay, then an exit to SC23 is immediate.

SC33

Parallel-character-transfer-to/from-control state. Data is transferred to/from the control whenever CRL or RGF are active. Data is read from SPM1 to the control during a Read operation and data is written to SPM1 from the control during a Write operation. Whenever a Write operation is in progress, Request Granted will cause an exit to SC14; otherwise the exit is via SC34.

SC34

SC34 the major decision state in which the type of operation and control character are compared with the linking variants to decide what logic branch to take in order to service the data. Exits from SC34 are via the following sequence counts:

SC04: A Read operation and no control character and B address not reached (WRA/·BARF/·CCD/).

SC33: A Write operation and no control character and B address not reached (WRA·BARF/·CCD/).

SC35: Whenever a control character is detected and the link variant disagrees with the polarity of the control character or stream mode.

SC36: No control character (CCD/) and B Address Reached (BARF).

SC38: Whenever a control character is detected and the link variant agrees with the polarity of the control character and the adapter is in stream mode.

SC35

Avoid-chaining state. Bit 06 of scratchpad (SPM3) is set. Exit is via SC38.

SC36

Control-character-not-detected state. Bits 07 and 08 of scratchpad (SPM3) are set. Exit is via SC38.

SC37

Time-out-or-Break state. Clear To Send time-out (bit 08) or Break-received (bit 07) is set in scratchpad (SPM3). If the adapter is performing a Read operation, the time-out (TOF) sets to terminate a stream Read. Exit from SC37 is via SC38.

SC38

Turnaround-delay state. The adapter initiates a 7-ms delay prior to requesting status. Exit from SC38 is via SC39.

SC39

Transfer status. The adapter issues a transfer request for status information resident in scratchpad (SPM3). If the adapter senses a loss of DSR, carrier, or CTS during this sequence count, the information will be impressed on either data bus 3 or data bus 4. Exit from SC39 is via SC40 through SC03 whenever RGL is sensed.

SC40-SC63

SC40 through SC63 are unused states that are incremented to SC00.

SCxx (Any Sequence Count)

Asynchronous states that allow or control the selection of interface information between the control and the adapter and between the data set and the adapter. If any of the control terms occur in certain sequence counts, then some additional logic is implemented to allow the adapter to utilize the information as immediate and valid control logic. The SCxx states do not require a set exit but may force the standard sequence count to exit as the logic dictates.

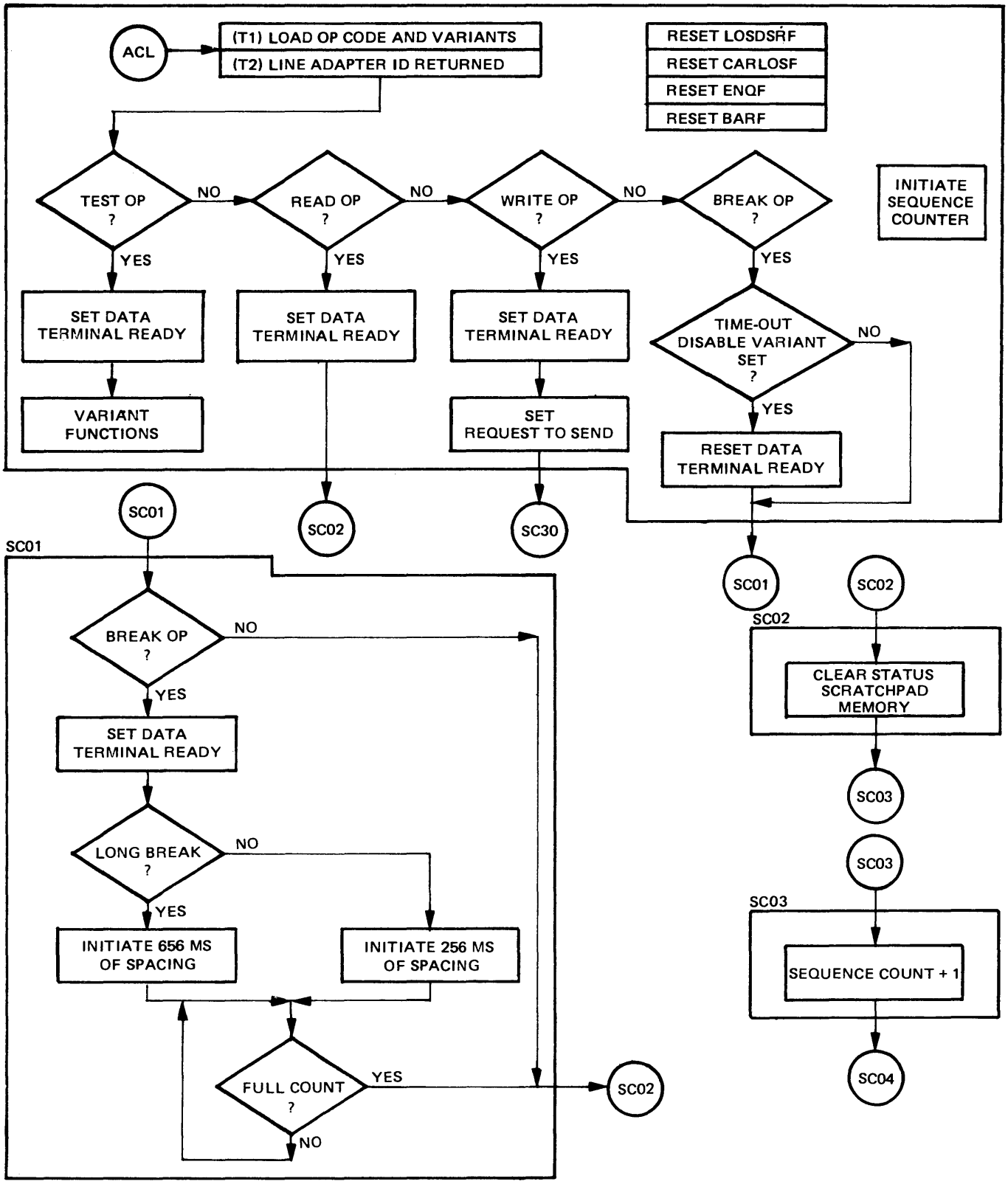

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 1 of 13)

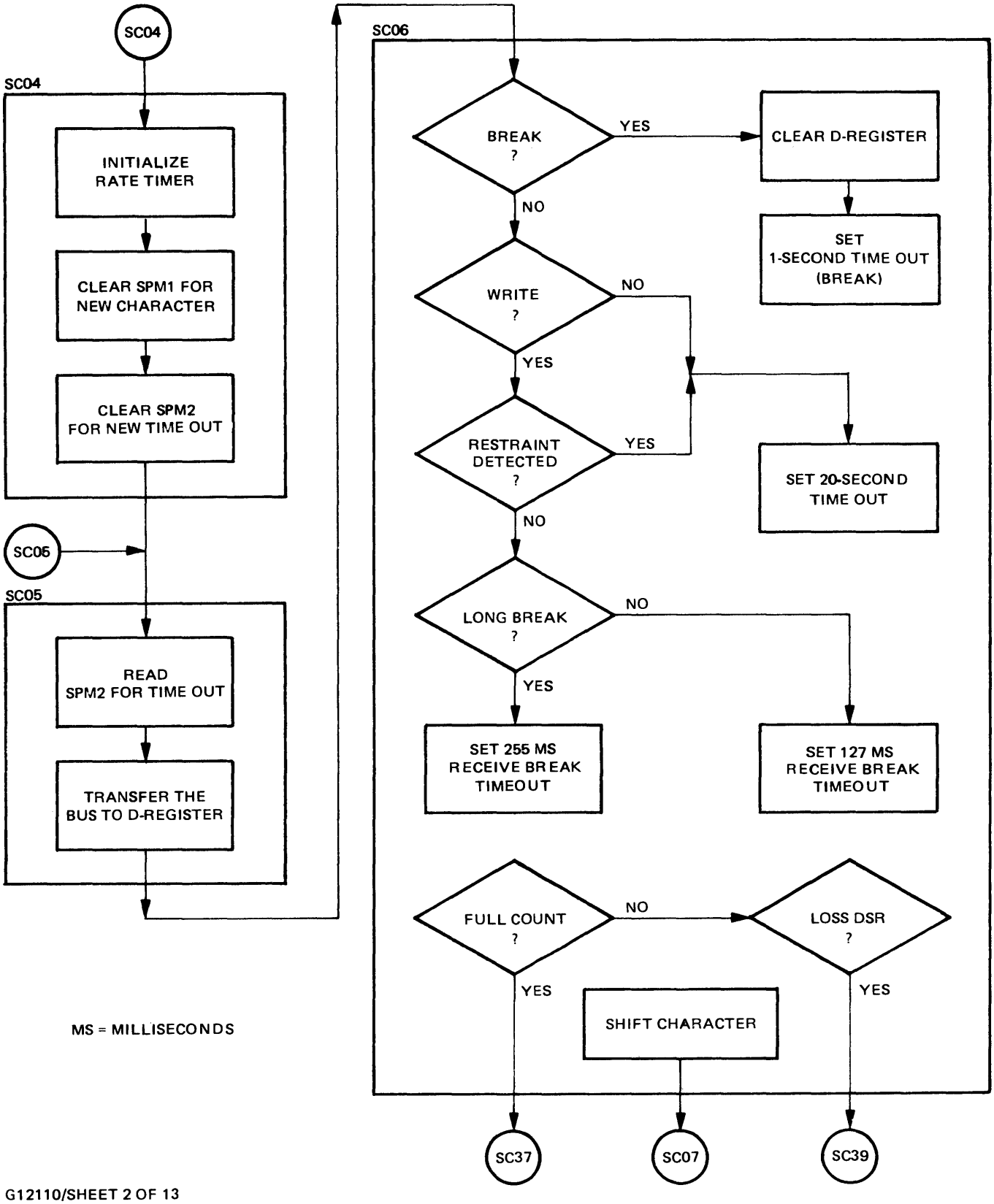

Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 2 of 13)

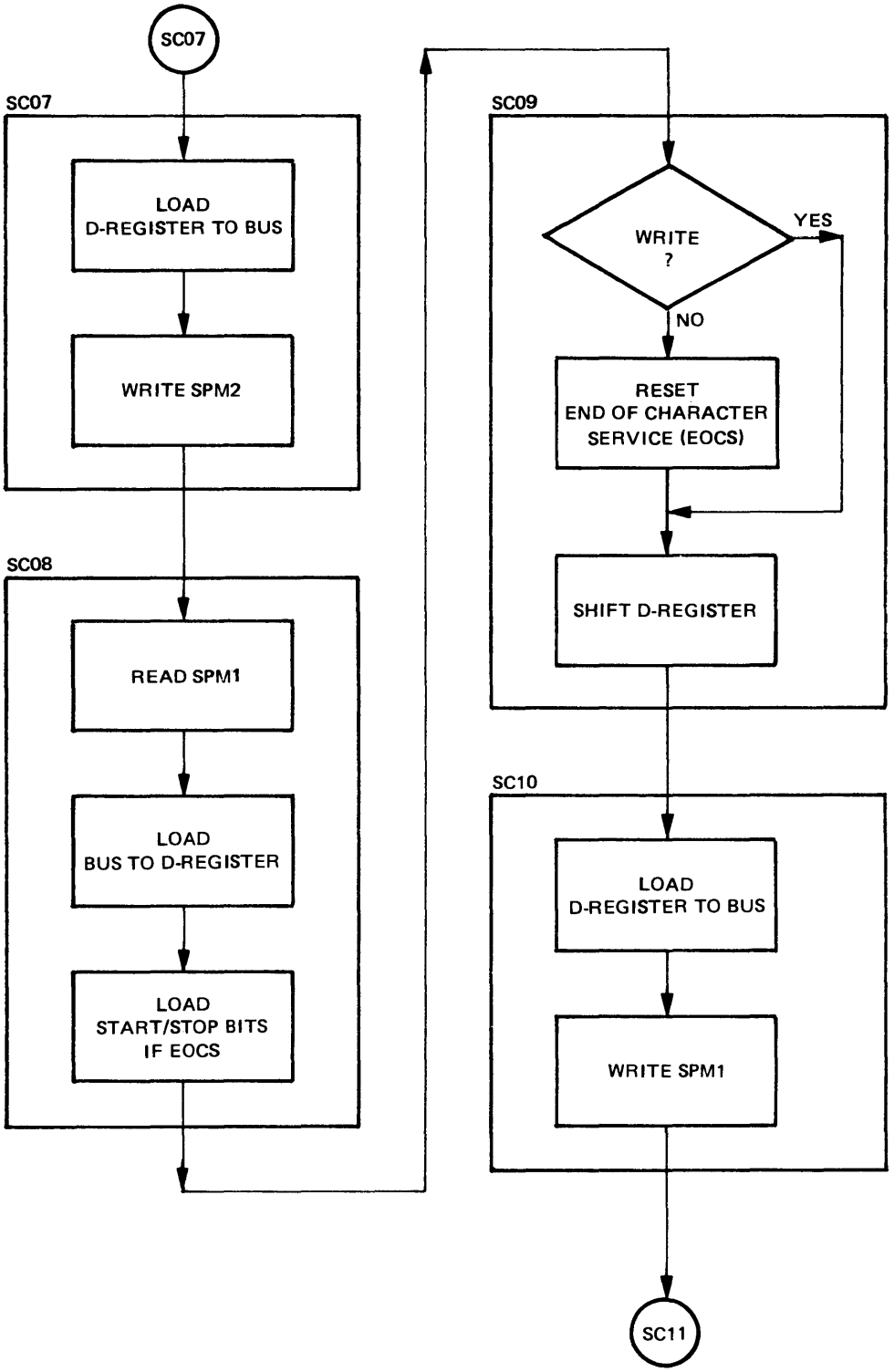

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 3 of 13)

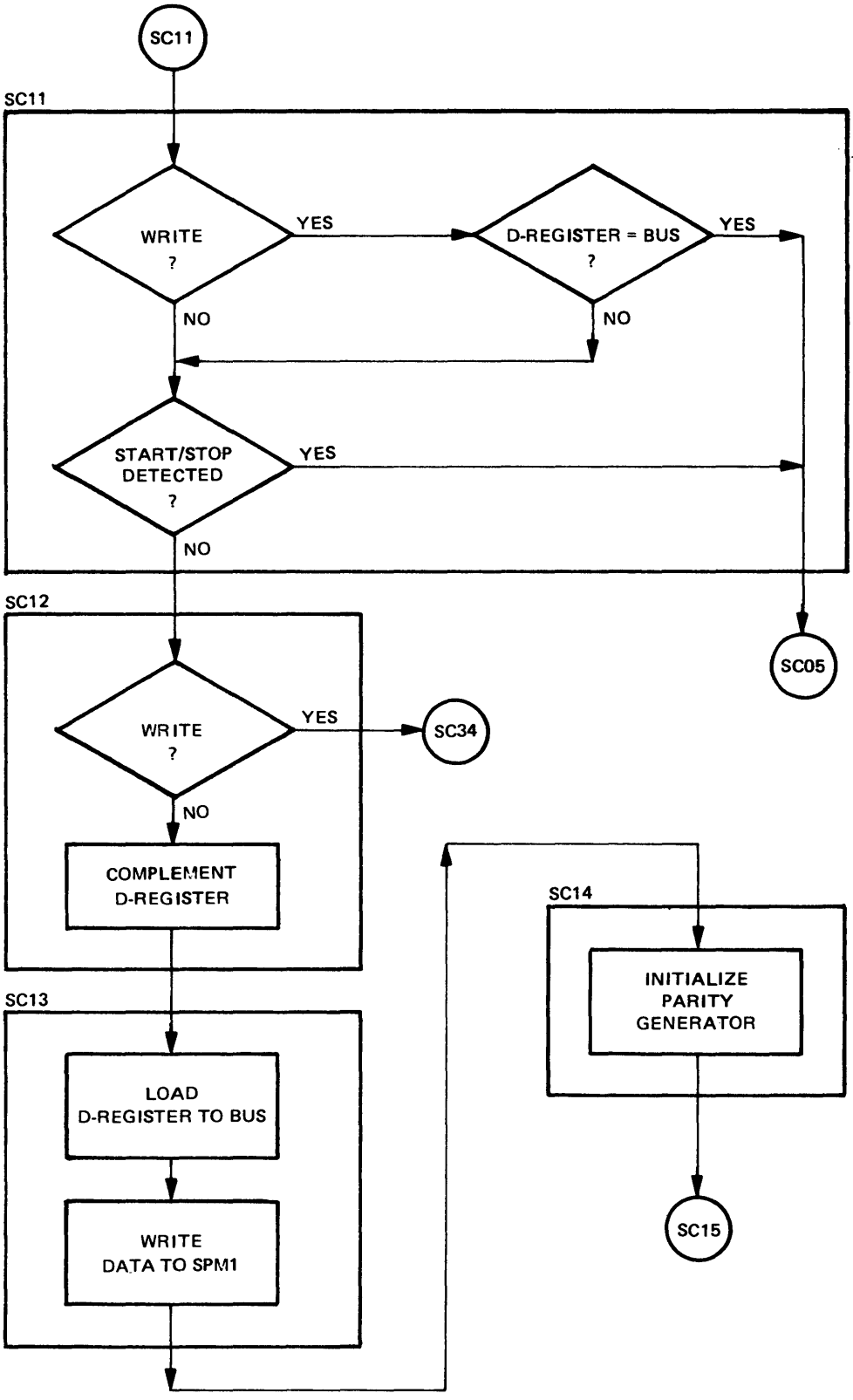

Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 4 of 13)

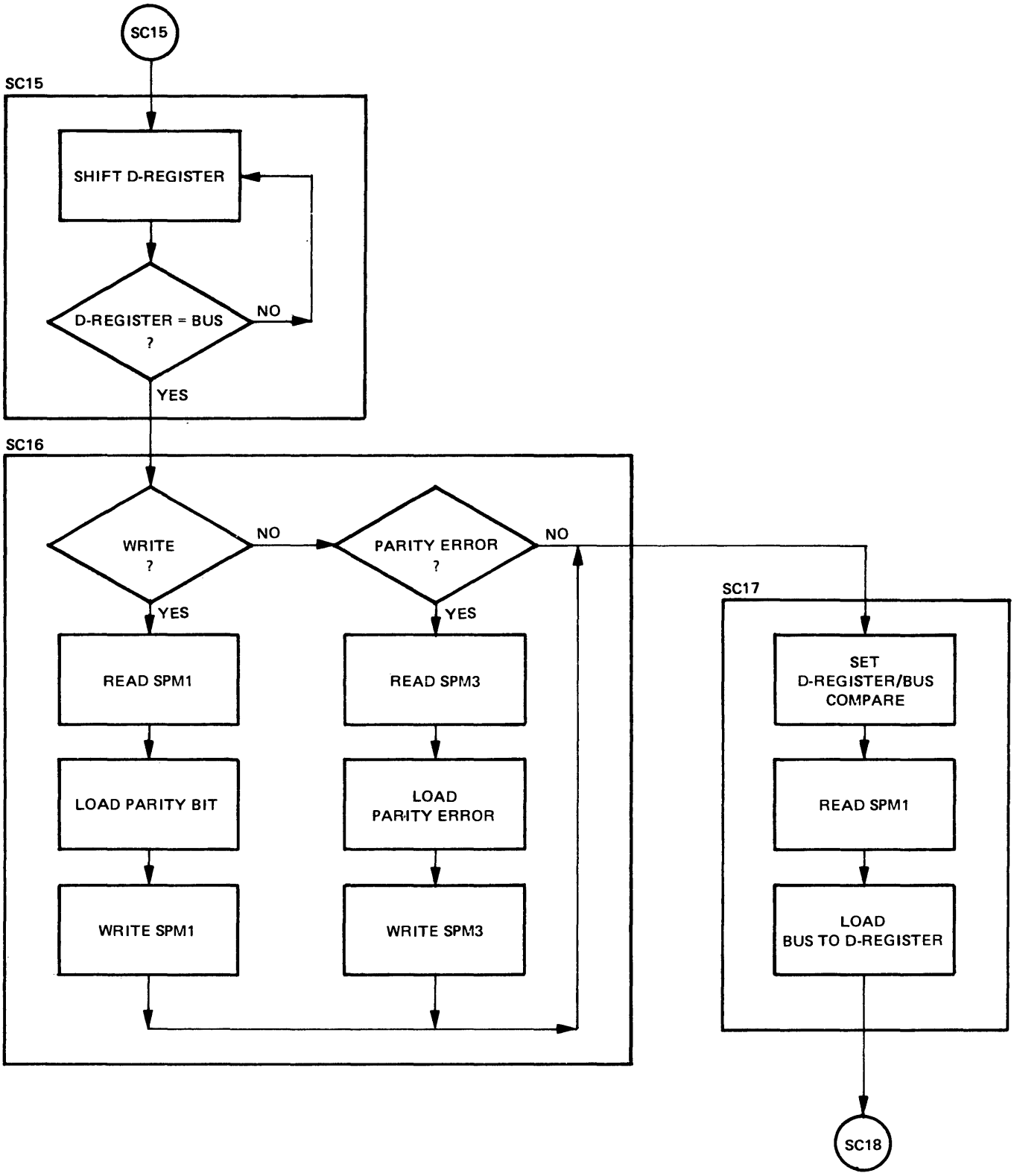

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 5 of 13)

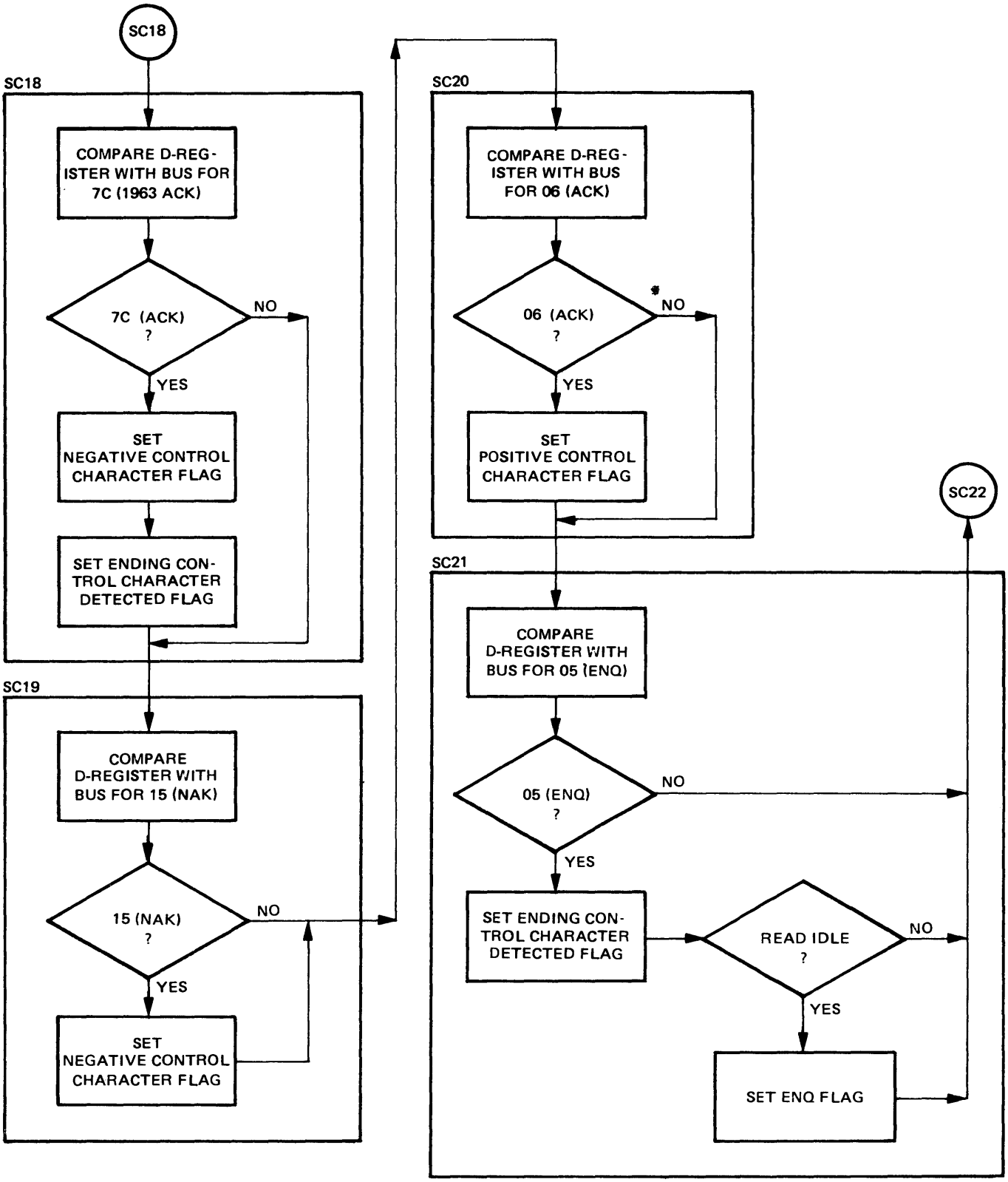

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 6 of 13)

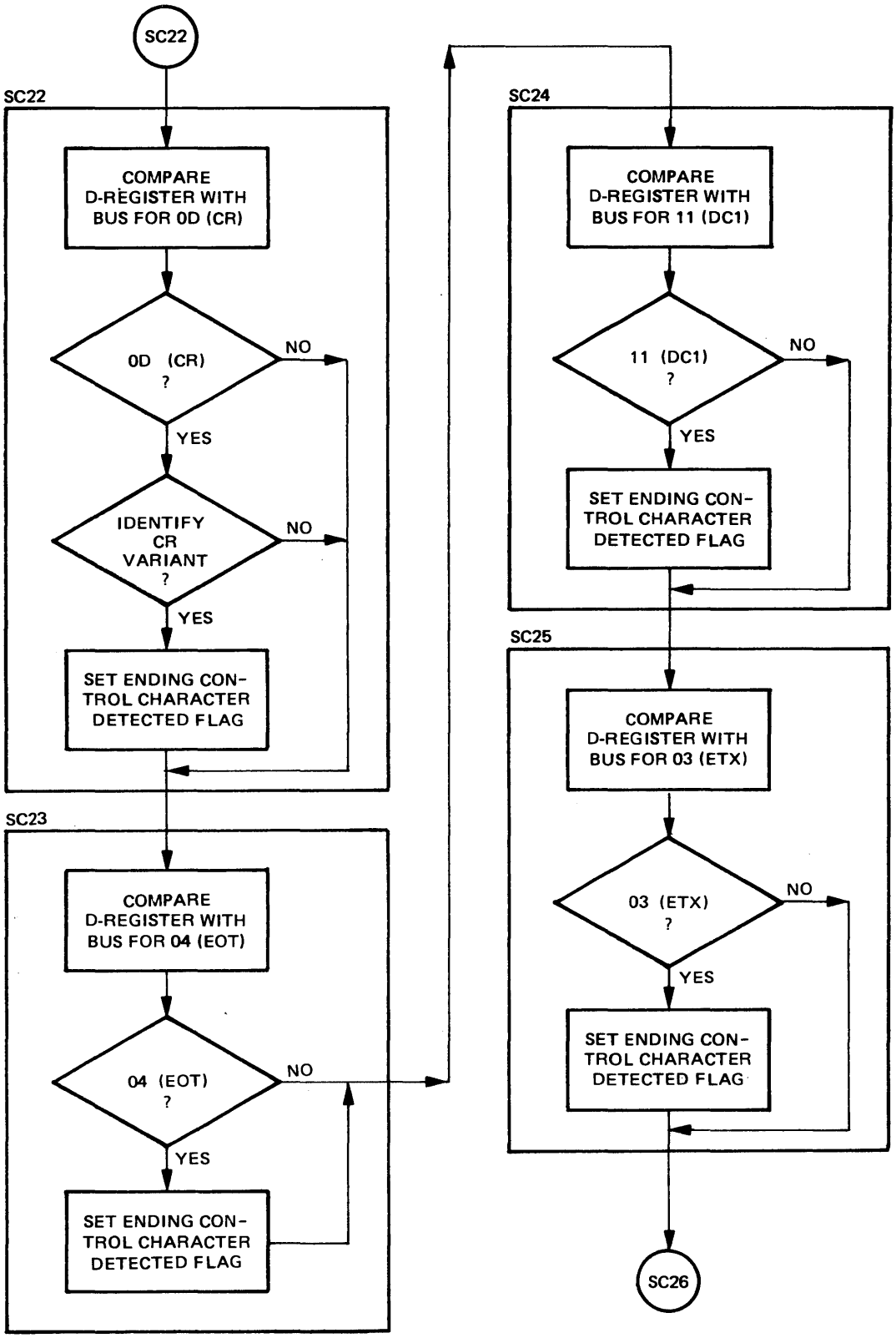

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 7 of 13)

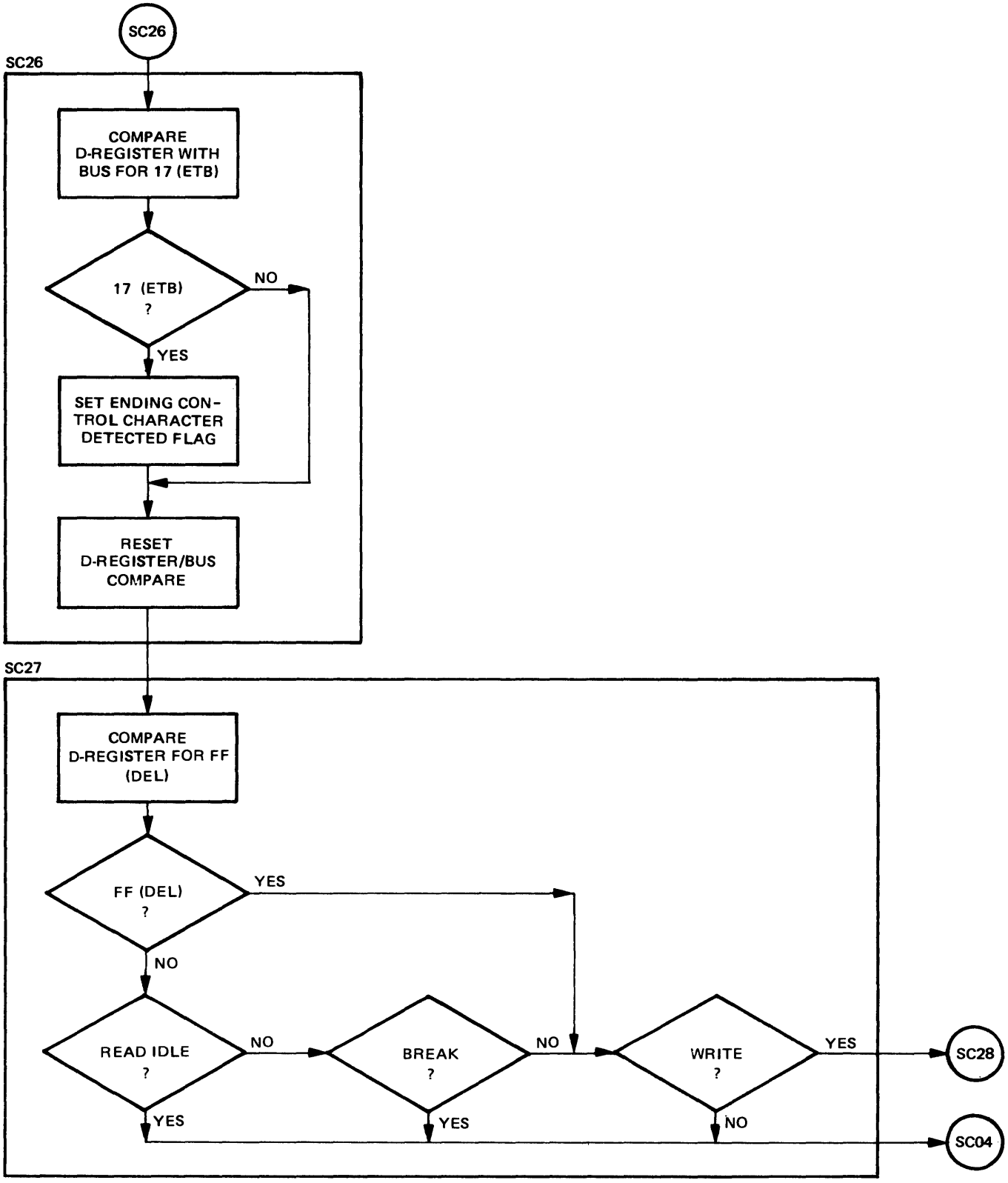

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 8 of 13)

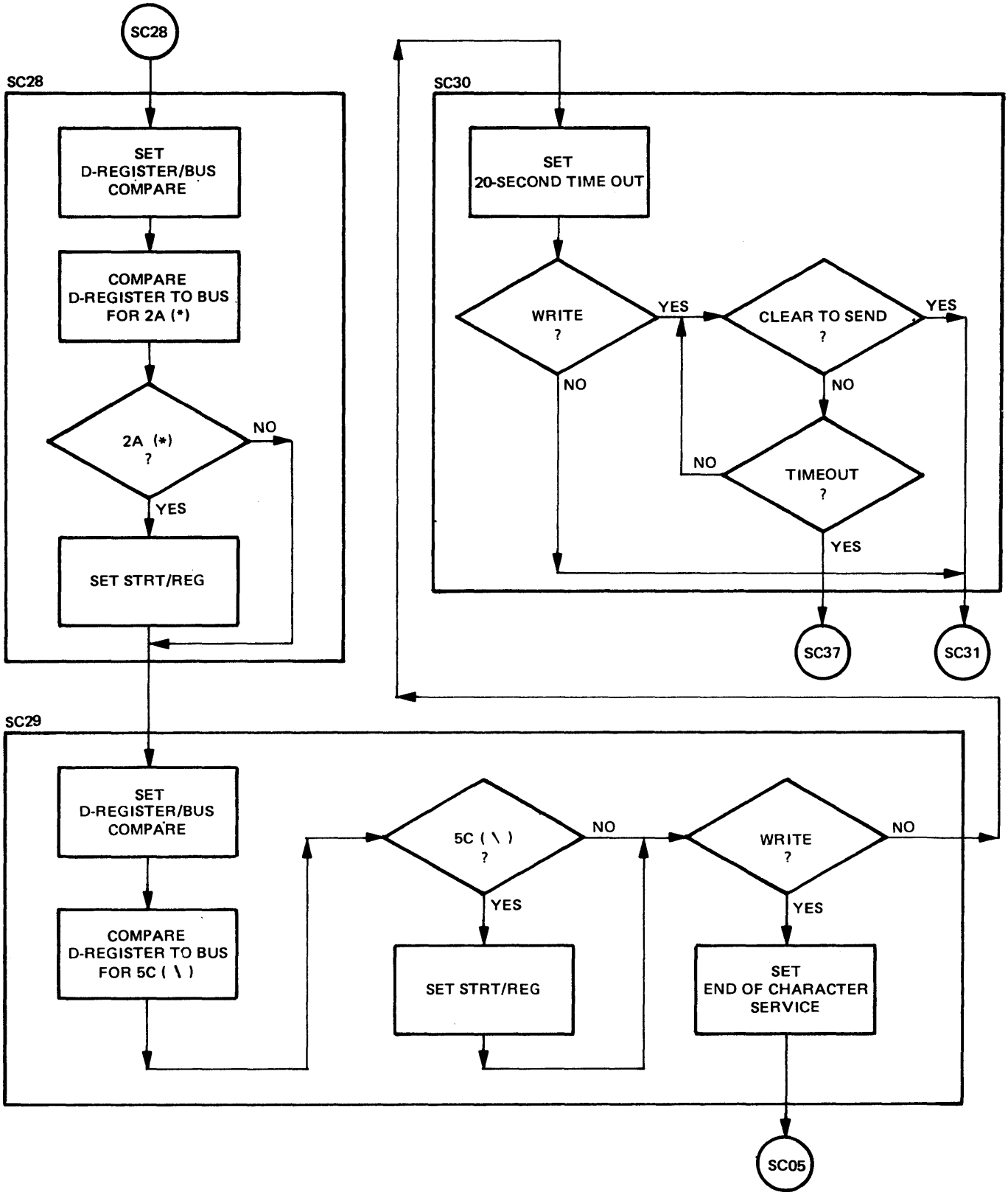

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 9 of 13)

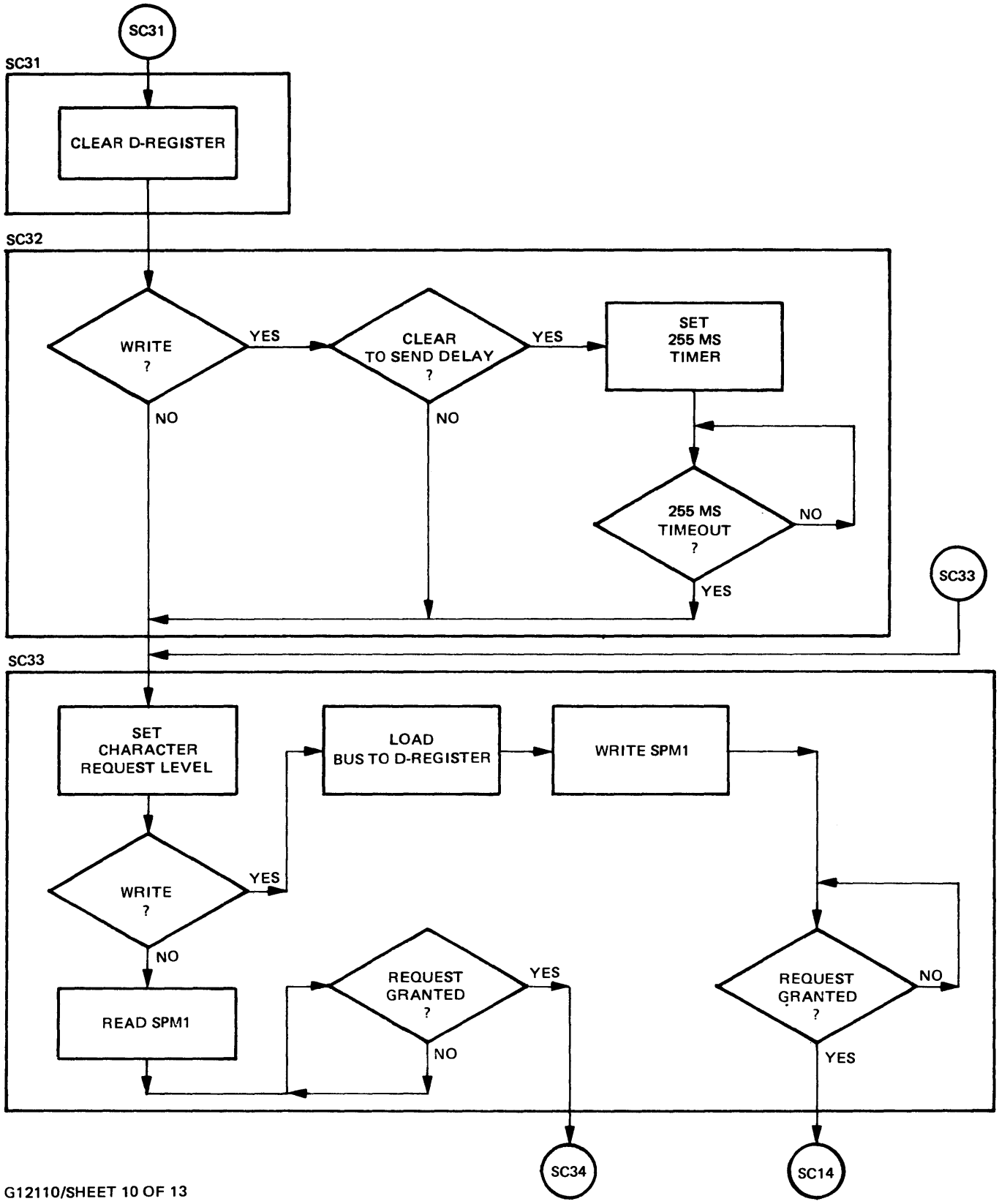

Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 10 of 13)

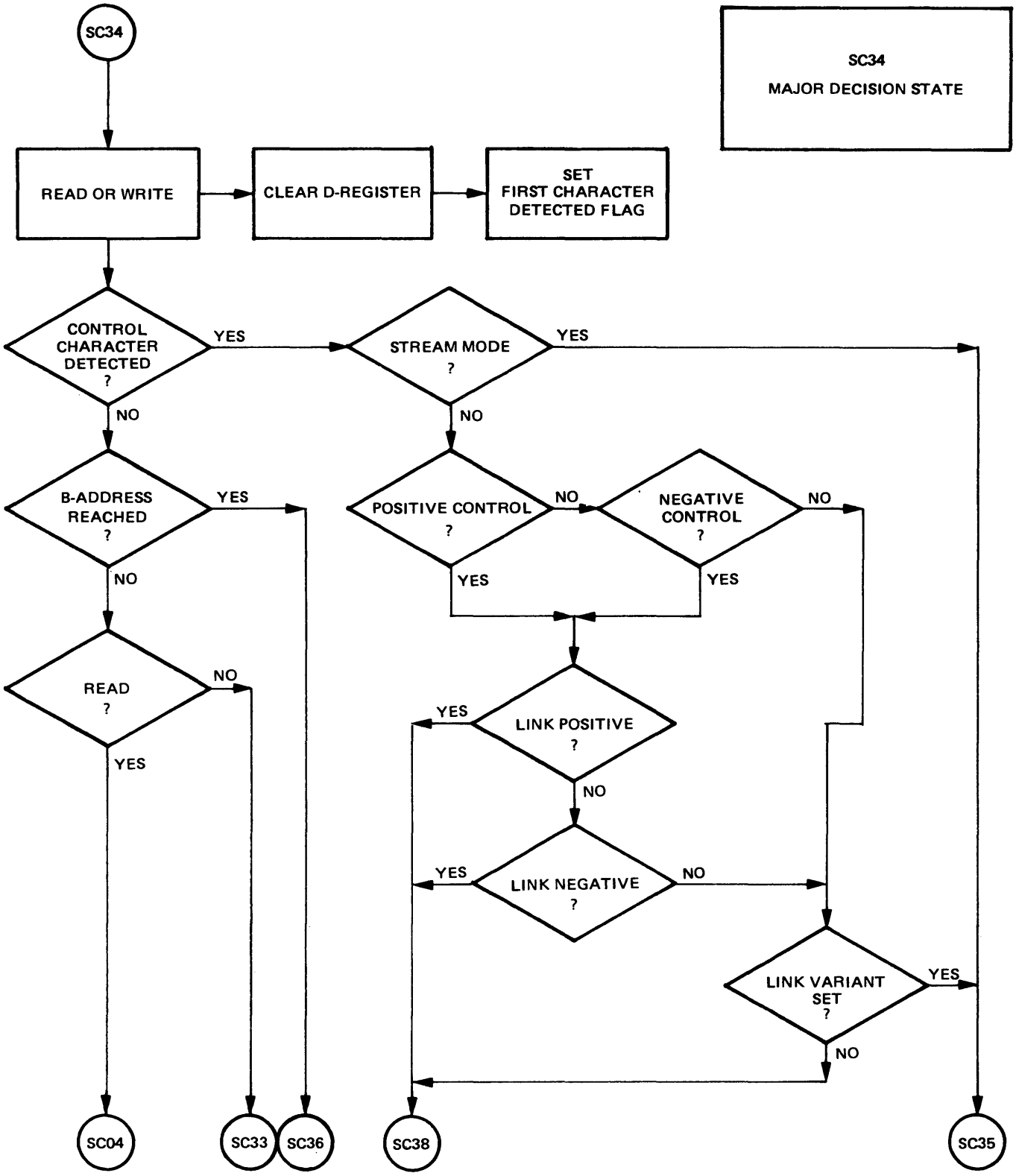

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 11 of 13)

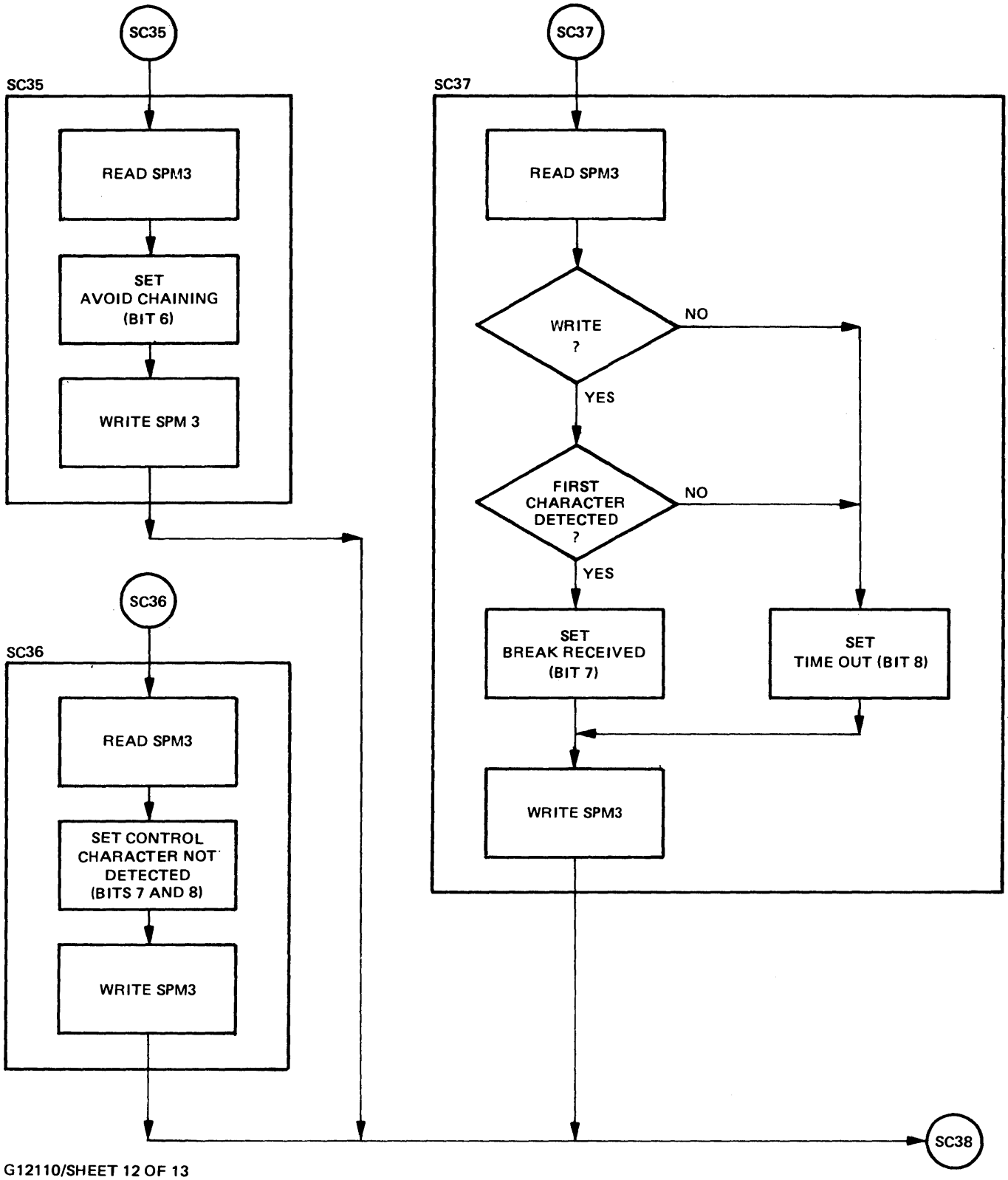

Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 12 of 13)

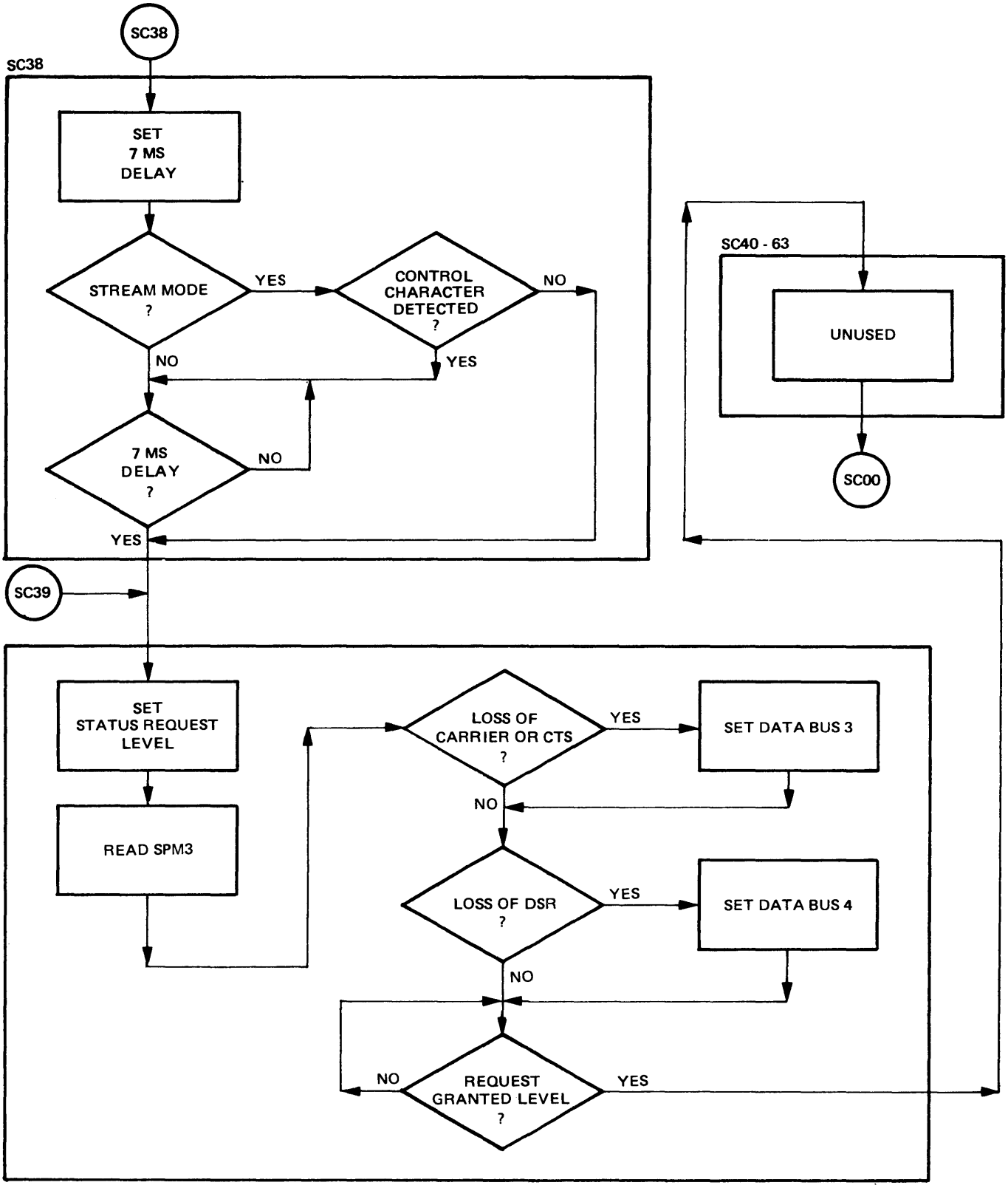

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Figure 10-2. Detailed Flow Chart, TTY/ASYN Line Adapter (Sheet 13 of 13)

SECTION 11
WIDEBAND LINE ADAPTER

INTRODUCTION

The Wideband (WIDEBAND) line adapter is a binary synchronous device that provides the interface between a single-line or multi-line control and Western Electric* WE303-type data sets. This adapter handles EBCDIC data and operates in normal mode as well as transparent mode.

Attached data sets must operate at either 19,200 bps or 50,000 bps using the half-duplex mode of operation. (Timing clocks are generated by the data set.) Data sets must be supplied with 105-129 Vac at 54-66 Hz. To avoid ground noise problems, it is recommended that data set input power (62 W) and computer system input power source be derived from the same source.

UNIT IDENTIFICATION

The WIDEBAND line adapter is contained on one logic card, identified by the 8-digit Burroughs Manufacturing and Engineering (M&E) number 2212 2089. This number is imprinted on a metal unit identification label supplied with the Field Test and Reference (FT&R) documentation for the unit. When the adapter is installed into the system, this label must be affixed on the end of the 28-position card housing assembly that contains the adapter.

CONTROL CODE SENSITIVITY

The WIDEBAND adapter is sensitive to the control codes listed in table 11-1.

Table 11-1 WIDEBAND Adapter Code Sensitivity

Code or Sequence	Function
SOH STX	Start
DLE STX	Start-transparent
ETX ETB	Ending
DLE ETX DLE ETB	Ending-transparent
ENQ	Positive response
DLE ACK0	
DLE ACK1	
DLE WACK	
DLE RVI	
NAK	Negative response
EOT (optional)	
ITB	Intermediate transmission block
DLE ITB	Intermediate Transmission block-transparent
DLE	Data Link Escape
SYN	Synchronization code
DLE SYN	Synchronization code-transparent
ENQ	Abort
DLE ENQ	Abort-transparent
1111 1111	Pad
STX ENQ	Temporary text delay (TTD)

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

*Registered Trademark of Western Electric.

Read

The Read operator causes data to be accepted from the remote device and stored into ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

0000 T0D- CEVV P--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII to EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
C = 0: Do not treat time-out on first character as negative response.
= 1: Treat time-out on first character as negative response.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
VV=00: Normal linking.
=01: Link only if negative response is received.
=10: Link only if positive response is received.
=11: Undefined.
P = 0: Do not Poll.
= 1: Poll.

Write

The Write operation causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B-minus-1th location is reached.

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the result descriptor for the terminated operation.

0100 T000 0E00 PLLL L--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
P = 0: Do not Poll.
= 1: Poll. (Start with the location specified by the E address.)
LLLL 0010-1101: Length of poll sequence (SLC only).

Break (Disconnect)

The Break operator causes an in-process operation, if any, to be terminated. The adapter is disconnected by turning Data Terminal Ready off. The result descriptor is returned one second after DTR goes off; the result indicates operation complete.

1100 00-- ---- ---- ---- UUUU

Test

The Test operator is a request for the reporting (in the result descriptor) of the adapter's identification and the conditions specified by the V and M variant combination.

100V --M- ---- ---- ---- UUUU

VM=00: Complete the operation normally. Do not change the status of the Data Terminal Ready signal.
=01: Make the Data Terminal Ready signal true, then complete the operation.
=10: Wait until a ringing condition is true before completing the operation (switched line only; other adapters wait "forever").
=11: Make the Data Terminal Ready signal true, then wait until Data Set Ready signal is true, before completing the operation.

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the WIDEBAND line adapter are listed below, together with their meanings when set. Omitted bits in the sequence 0-23 are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception Conditions (For all operators except Test, this bit is set if any of bits 2-15 are set.)
3	Parity error character or BCC (Read).
4	Memory access error (Read).
5	Memory parity error (Write).
6	Time-out (Read or Write).
7	Break received (Write).
9	Linking terminated (Read; VV = 01 or 10).
16	Operation completed.
17	Data communications device (Test).
18-23	Adapter ID (Test): 000000 = adapter not present, 001110 = WIDEBAND adapter, leased line, 101110 = WIDEBAND adapter, switched line.

FUNCTIONAL DESCRIPTION

Adapter to Data Set Interface

The WE303 data set uses a current interface on all but two of the interface circuits (table 11-2). For circuits using the current interface, a control level ON or a data level SPACE (0) is by a current greater than 23 mA into a 100-ohm termination. A control level off or data level MARK (1) is a current less than 5 mA into a 100-ohm termination. Open lines are interpreted by the receiver as an off (MARK) hold.

The two exceptions to the current interface are the signals Data Terminal Ready (DTR) and Ring Indicator (RI). Both of these signals are RS-232-C voltage-type control levels, and each is routed electrically on an outer conductor of one of the coaxial cable lines.

Serial Clock Receive

Serial Clock Receive is a symmetrical timing pulse used to sample data at appropriate times. The phase relation between this clock and the received data line is such that the middle of a data bit element occurs within 10 percent of the negative-going transition of the timing signal.

AGC Lock

The AGC lock circuit is on while the data set is receiving a signal of sufficient amplitude and quality from the incoming telephone lines. This signal is comparable in function to the Received-Line-Signal-Detector signal specified for RS-232-C.

Data Terminal Ready (DTR)

DTR, a signal generated by the WIDEBAND adapter to control the switching of the data set to the communication channel, provides automatic answering and disconnecting capability. Optionally, this line can be strapped on in the adapter when using dedicated rather than switched service. When not strapped to the ON state, this signal is turned on only by a Test operator with the wait-for-DSR variant set. The signal is turned off with a Break operator or a system clear.

Table 11-2. Interface Lines, WIDEBAND Adapter to Data Set

Data Set Pin	Adapter Pin	Description
L	$TY	Serial Clock Receive
M	$CY	AGC Lock
M shield	$DY	Data Terminal Ready
C	$NY	Clear To Send
D	$RY	Request To Send
E	$PY	Send Data
F	$IY	Data Set Ready
F shield	$HY	Ring Indicator
J	$SY	Serial Clock Transmit
K	$WY	Receive Data

Clear To Send (CTS)

CTS is a level returned from the data set as a response to the Request-To-Send level. This signal indicates that the data set is ready to transmit information. There is no significant delay between Request To Send and Clear To Send. The main function of CTS in the WE303 data set is to indicate that the data set is not in the Remote Test mode.

Request-To-Send (RTS)

RTS is a level is generated by the adapter when the system wants to transmit information. Request To Send is permanently on if the Data Terminal Ready level is strapped on in the adapter. Two strappable options are available if Data Terminal Ready is not permanently strapped on:

Request To Send follows DTR. Request To Send and DTR change to the same level simultaneously.

Request To Send goes on at the beginning of each transmission and off at the completion of transmission.

Send Data

Send Data signals that data is to be transmitted. The data is timed by the data set's internal transmit clock. When data is not being transmitted, the adapter maintains Send Data at the hold (MARK) level.

Data Set Ready (DSR)

DSR, when on, indicates that the data set is capable of transmitting and receiving wideband data, including voiceband data if so equipped. When off, DSR indicates the following conditions:

A local or remote test or a power-off condition.

The voice frequency coordination channel is not capable of operating.

The local data set is not connected to the communication channel.

Ring Indicator

The Ring Indicator line is turned on for each ring on the voice frequency coordination line. When Data Terminal Ready is turned on, the call is answered. Data Set Ready comes on approximately 5 seconds later.

Serial Clock Transmit

Serial Clock Transmit is a symmetrical timing wave generated by the data set to control the movement of data from the adapter to the data set. A data bit shift occurs at the positive-going transition of Serial Clock Transmit.

Receive Data

The Receive Data signal is delivered serially to the adapter on this line. The data is strobed at the negative-going transition of Serial Clock Receive.

Codes

Synchronization Code

In transmit mode, the WIDEBAND adapter sends four contiguous SYN characters before sending data. In receive, the adapter achieves synchronization by detecting two contiguous SYN characters.

Block Check Character Code

The WIDEBAND adapter generates a 16-bit block check character.

Start Codes

A control code classified as a start code is used to start the accumulation of a BCC. The accumulation starts wih the next non-SYN code and includes all codes except SYN up to and including an ending code or an intermediate transmission block code. In transparent mode, however, the first DLE of all DLE XXX sequences and the SYN code in all DLE SYN sequences are not included in the BCC summation. A SYN code (if not part of a DLE SYN sequence) is included. The DLE STX sequence invoking the transparent mode is included only when a start code has preceded it.

NOTE

A STX ENQ sequence can be sent or received to indicate temporary text delay. No BCC follows this sequence.

Transparency

A control code sequence classified as a start-transparent code sequence starts a transparent mode of operation, and begins the accumulation of a BCC if accumulation has not begun as the result of a prior start code.

Termination Codes

In transparent mode, only an ending transparent code sequence or an abort transparent code sequence terminates a Read operation. A Write operation is terminated when the last two characters contained in the assigned Write buffer area are DLE ETX, DLE ETB, DLE ITB, or DLE ENQ. If none of these code sequences are present, a DLE ENQ sequence is generated in lieu of the BCC by the control.

In non-transparent mode, after receipt of a start code, only those codes classified as ending codes or abort codes terminate a Read operation. A Write operation is terminated by an intermediate transmission block (ITB) code.

In non-transparent mode, a control code classified as a response code terminates the operation only if it is not preceded by a code classified as a start code. A response code is defined only in non-transparent mode.

In non-transparent mode, a control code classified as an intermediate transmission block code terminates a Write operation. The control generates a BCC after the ITB code. Since character synchronization is re-established at the beginning of each Write operation, it is not possible to transmit successive messages ending in ITB and maintain character synchronization between the end of one message and the start of the next.

Receipt of an ITB code does not terminate a Read operation. The adapter deletes the ITB and stores neither the ITB nor nor the cyclic redundancy check (CRC) character. Subsequent codes are stored, however, and BCC is checked.

In transparent mode, a DLE ITB code in the last two positions of the Write buffer area terminates a Write operation. During Read, receipt of DLE ITB does not terminate the operation. The adapter checks the BCC, remains in character sync, and reverts to non-transparent mode. The DLE ITB, BCC, and all subsequent codes (up to and including a DLE STX code sequence) are not stored. Codes following the DLE STX sequence are stored normally.

NOTE

The codes ETX, ETB, and ITB always terminate an operation. If these codes are not preceded by STX or SOH, a BCC error is reported on Read. On Write, the BCC is omitted but the Pad character is sent.

Abort Code

The abort code follows a start code to abort the operation. The BCC follows the abort code. The WIDEBAND adapter automatically generates this pattern upon detection of a memory parity error or upon reaching the B address without detecting an ending code. If an abort is received, the operation is terminated in the normal manner and no error is reported.

Positive and Negative Codes

A control code defined as a positive response causes an error termination (linking terminated) on a Read OP code if the variant bit denoting link-on-negative-response is true. Otherwise, the Read completes with operation complete and no exception indicated in the Result Descriptor (provided that no other exception conditions exist).

A control code defined as a negative response causes an error termination (linking terminated) on a Read OP code if the variant bit denoting link-on-positive-response is true. Otherwise, the Read operation completes as above.

Pad Character

To ensure that the last characters of a transmission are properly transmitted by the data set, the WIDEBAND adapter adds a pad character consisting of all ones after the BCC, ENQ and response code sequence for all transmissions. On input, the first four bits after a response code are checked for all ones; if this is not the case, the adapter continues to receive and store data. The pad character is optional for transmitting data but mandatory for receiving data.

Variants

A variant is provided to permit EOT to be ignored as a response code on Read and Write operations. On a Read operation this variant allows the I/O control and the system to which it is attached to act as a terminal and receive a polling sequence from other systems. (No hardware recognition of addresses is provided.) On a Write operation, this variant allows the I/O control to ignore EOT and transmit polling and other sequences that use the first EOT in a message as a line clearing code.

Failure to receive the first character within 1 second is treated exactly as like reception of a negative response character by means of the Read character. Normally, this variant is used in conjunction with the poll variant and the link-on-negative-response variant to allow non-present terminals to be ignored.

DLE Insertion and Deletion

In a transparent Write mode, the WIDEBAND adapter automatically inserts a DLE code on encountering any DLE DLE sequence (except one that precedes the last character received from memory). In a transparent Read mode, the WIDEBAND adapter automatically deletes the first DLE of all DLE XXX sequences received, including the DLE portion of an ending control code sequence.

SYN Insertion

During text transmission in non-transparent mode, the WIDEBAND adapter inserts pairs of SYN characters in the data stream at 1-second intervals. During transparent mode, the adapter inserts DLE SYN patterns, also at 1-second intervals; however, DLE SYN patterns are not inserted if the last character transmitted is the first DLE of a DLE DLE pair. The DLE SYN sequence is transmitted following the second DLE of the DLE DLE pair.

SYN Detection

In a receive mode prior to synchronization, the WIDEBAND adapter detects the absence of two contiguous sync characters for more than 4 seconds (or 1 second if so specified by the "treat-time-out-as-a-negative-response" variant). Once synchronization has been established, the adapter detects the absence of either a sync pattern or a control character for more than 4 seconds. The 4-second time-out (but not the optional 1-second time-out) can be inhibited programmatically.

Memory Access Error

A memory access error occurring during a Write operation results in transmission of a SYN sequence: SYN in non-text mode, SYN SYN in non-transparent text mode, and DLE SYN in transparent text mode.

NOTE

A DLE SYN pattern is not inserted in the data stream if the last character transmitted is the first DLE of a DLE pair (transparent operation). DLE SYN is transmitted following the second DLE of the DLE pair.

A memory access error occurring during a Read operation results in a data loss. A result descriptor indicating the access error is returned at the completion of the Read operation.

Disconnect

The adapter disconnects the line by turning the Data Terminal Ready signal off (if the adapter is strapped for switched line operation). The result descriptor, returned 1 second after DTR is turned off, specifies operation complete, no exceptions.

Test Operation Codes

A Test operation with the Test-and-Wait variants off (VM = 00) results in immediate return of a result descriptor giving adapter identification. If VM = 01, 10, or 11, return of the result descriptor is be delayed until the condition necessary for the operation to complete occurs.

The WIDEBAND adapter is also responsive to the following Test and Wait operations:

Test and Wait for Ringing,

Test and wait for Data Set Ready.

One of two adapter identification codes may be returned in response to Test:

DEDICATED LINE: 1000 0000 0000 0000 0100 1110

SWITCHED LINE: 1000 0000 0000 0000 0110 1110

Components

The functions of the Wideband EBCDIC line adapter are primarily controlled by a sequence counter (SCXX), an instruction counter (I counter), and an instruction register (I register). The sequence counter defines the basic operating states of the adapter (00 through 15), the 3-bit I register defines specific operations concerning data transfer, and the I counter controls the duration of an operation. I register and I counter functions are listed in table 11-3.

Block Diagram

Other basic components in the WIDEBAND adapter are listed below. Figure 11-1 is a block diagram that shows the hardware relationships of all the basic components.

Time counter (T counter)

D register

E register

L register

Cyclic Redundancy Character (CRC) register

Op and Variant register

Character decoder

During a Write operation, the D register receives a character from the bus. The character is (1) inspected for control significance by the character decoder, (2) transferred to the E register, (3) shifted from the E register to the communication line, and (4), if the character is text, moved to the CRC register.

The contents of the D register are also transferred to the E register and, if text, from the E register to the CRC register. When a complete text message has been received, the accompanying CRC character is compared with the contents of the CRC register. A non-comparison causes the Block-Check-Error flip-flop to be set.

The CRLF (Character-Request-Level flip-flop) indicates to the control that the adapter is ready to receive/send a character from/to the control.

Table 11-3. Functions of the I Register and I Counter

A	B	Function	I Counter	Mode
000	0	Idle		
001	1	Shift E to CRC	8 clocks	Read
010	2	Shift E to line	8 shift pulse	Write
011	3	Shift E to line	8 shift pulses	Write
100	4	Compare accumulated CRC incoming CRC	16 shift pulses	Read
101	5	Shift CRC to line	16 shift pulses	Write
110	6	Rotate E and shift to line	24 shift pulses	Write
111	7	Shift bits in until SYN SYN pattern is detected		Read

A: I register contents.
B: Instruction number.

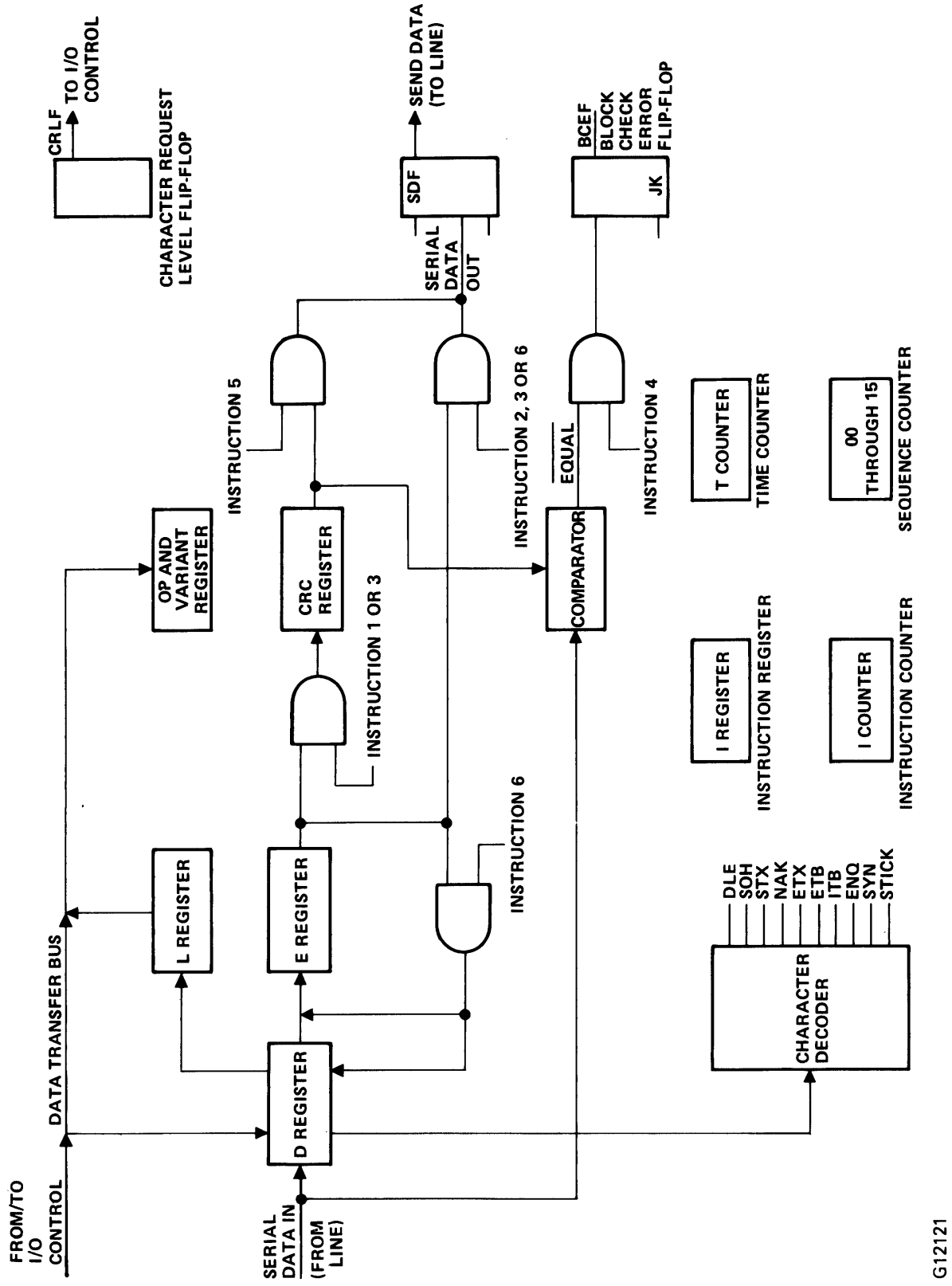

Figure 11-1. Block Diagram, WIDEBAND Adapter

Sequence Counter

The sequence counter is a 4-bit counter that counts from 00 through 15. The function of each sequence count is provided in the following paragraphs. Figure 11-2 is a simplified flow diagram of the count sequences. Figure 11-3, at the end of this section, is a detailed flow diagram of the actions of the WIDEBAND line adapter.

SC00

Idle state. The adapter waits in SC00 for a new initiation from the control. Exit from SC00 is determined by the operation initiated by the control.

SC01

Initial delay state. The adapter waits in SC01 for specific time periods (depending on the operation) before continuing. Exit from SC01 is determined by the type of operation, as follows:

SC02: This exit is taken following the execution of Instruction 7 (detection of two contiguous sync characters).
SC10: This exit is taken when one of the following conditions exists:

A Clear To Send (CTS) is not returned from the data set within 20 seconds when starting a Write operation.

A Disconnect is issued and 1 second has elapsed.

SC14: This exit is taken following a Write initiation to allow a 1-clock delay before writing four contiguous sync characters.

SC02

Read non-text state. The adapter waits for the establishment of synchronization and then searches for control characters that precede the actual text of the message. Any exit from SC02 is determined by one of the following conditions:

SC03: A Start of Heading (SOH) or Start of Text (STX) character has been detected.

SC08: Ending control character (ETX, ETB or ITB) detected without a prior starting control character (SOH or STX).

SCL0: Three possibilities: (1) End of Buffer (EBF) reached without detection of an ending control character (ETX, ETB or ITB), (2) time-out (4 seconds) before detection of 2 time-out (1 second) during detection of non-text characters (OP code variant set).

SC12: An ending control character (ETX, ETB or ITB) is detected following the detection of a start code (SOH or STX).

SC03

Read-text state. The adapter reads normal text (message) data. Any exit from SC03 is determined by one of the following conditions:

SC08: An ending control character has been detected.

SC09: An ENQ character has been detected.

SC11: Two possibilities: (1) the end of the buffer has been reached, or (2) time-out (4 seconds) has occurred.

SC04

Write-non-text state. The adapter sends control characters following transmission of a contiguous sync pair. Exit from SC04 is determined by one of the following conditions:

SC05: After a starting code (SOH or STX) has been sent.

SC09: End of buffer has been reached without having sent a starting code, or an ending code has been sent.

SC05

Write-text state. The adapter writes either normal text or transparent text messages. Transparent text is entered via a DLE STX sequence of characters; the adapter becomes insensitive to control codes until it detects DLE ETX, DLE ETB, or DLE ITB.

DLE insertion into the text occurs whenever a Transfer-Suppress-Level (TSL) occurs and a sync character fill is required or a DLE character is detected.

Exit from SC05 is determined by one of the following conditions:

SC06: When a TSL is received and a sync character fill is required, or the end of buffer is reached without detection of an ending control code.

SC08: An ending control code is sent. (This is the normal end of SC05.)

SC09: An ENQ is sent from the control; this indicates termination of the data block.

SC06

Write-sync-character or Write-ENQ-character state. The adapter sends either a sync or ENQ character. Exit is via one of the following sequence counts:

SC05: Send SYN and return to sending text.

SC09: Send ENQ character and go to write Pad character.

SC08

Read or Write CRC manipulation state. The adapter either shifts in or shifts out a CRC accumulation. Exit from SC08 is determined by the following conditions:

SC03: The previous block was an ITB (Read only).

SC09: The previous block was not an ITB.

SC09

Read or Write pad manipulation state. The adapter shifts a pad character (FF) in or out. Exit from SC09 is via SC10 after the pad has been shifted or, in a Read operation, when the carrier drops.

SC10

Transfer-status state. The adapter raises SRL and waits for RGF. Loss-of-line conditions (DSR, CO and CTS) are reported along with Block Check Error, time-outs, End of Buffer, and linking terminated. Exit is via SC00 (idle state).

SC11

This sequence count is identical to SC10.

SC12

Check Read pad character state. The adapter checks the first four bits of the pad character for all ones (1111). Exits from SC09 are as follows:

SC02: First 4 bits are not all ones (1111).

SC09: First 4 bits are all ones (1111).

SC14

Write delay state. The adapter waits for one clock before exiting to SC04 to write four sync characters.

Adapter Control Level (ACL)

Initiation state. The adapter is loaded with the OP code and variants during T1F, and adapter ID is returned during T2F. Exit from ACL is via SC01.

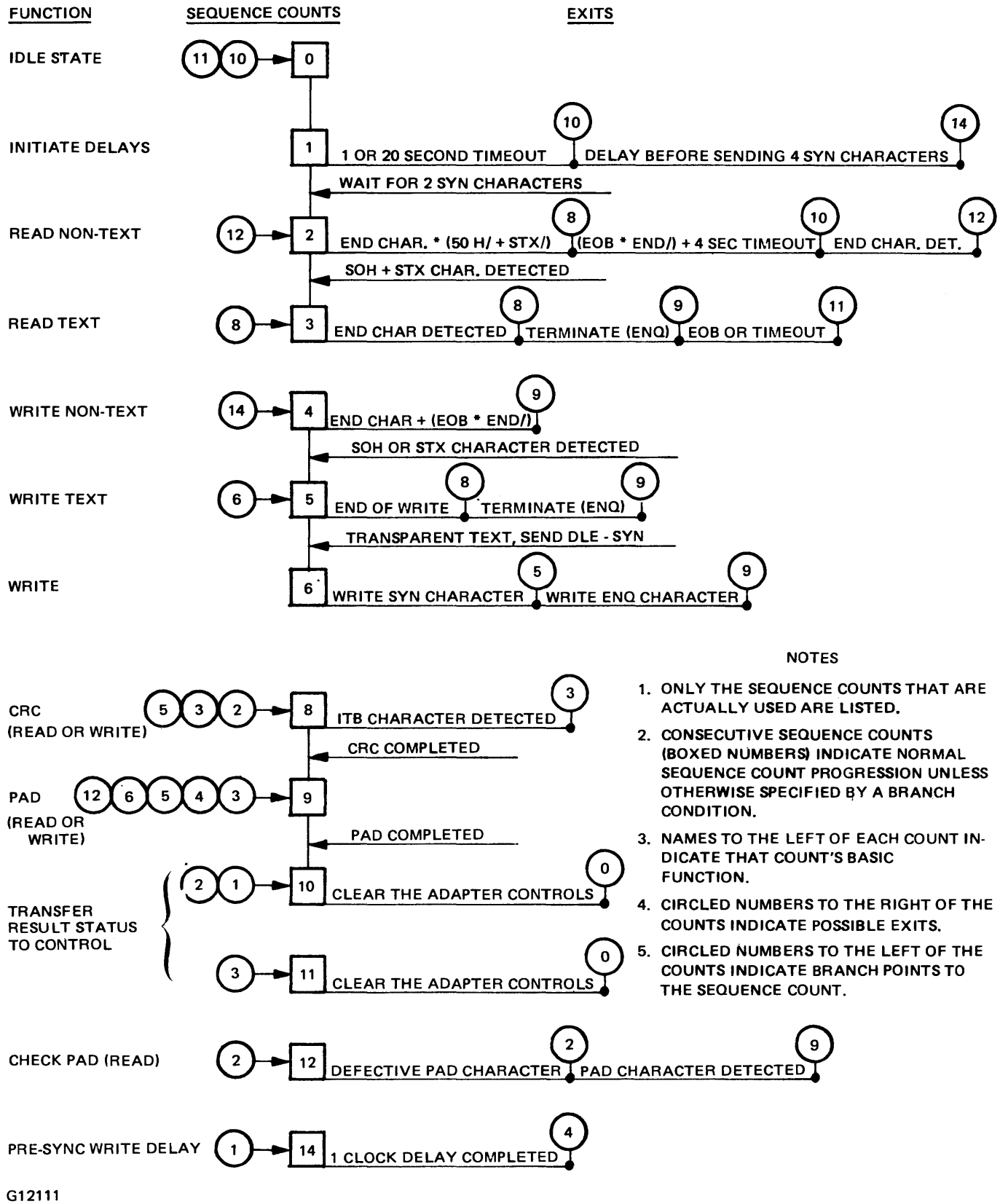

Figure 11-2. Basic Sequence Count Flow, WIDEBAND Adapter

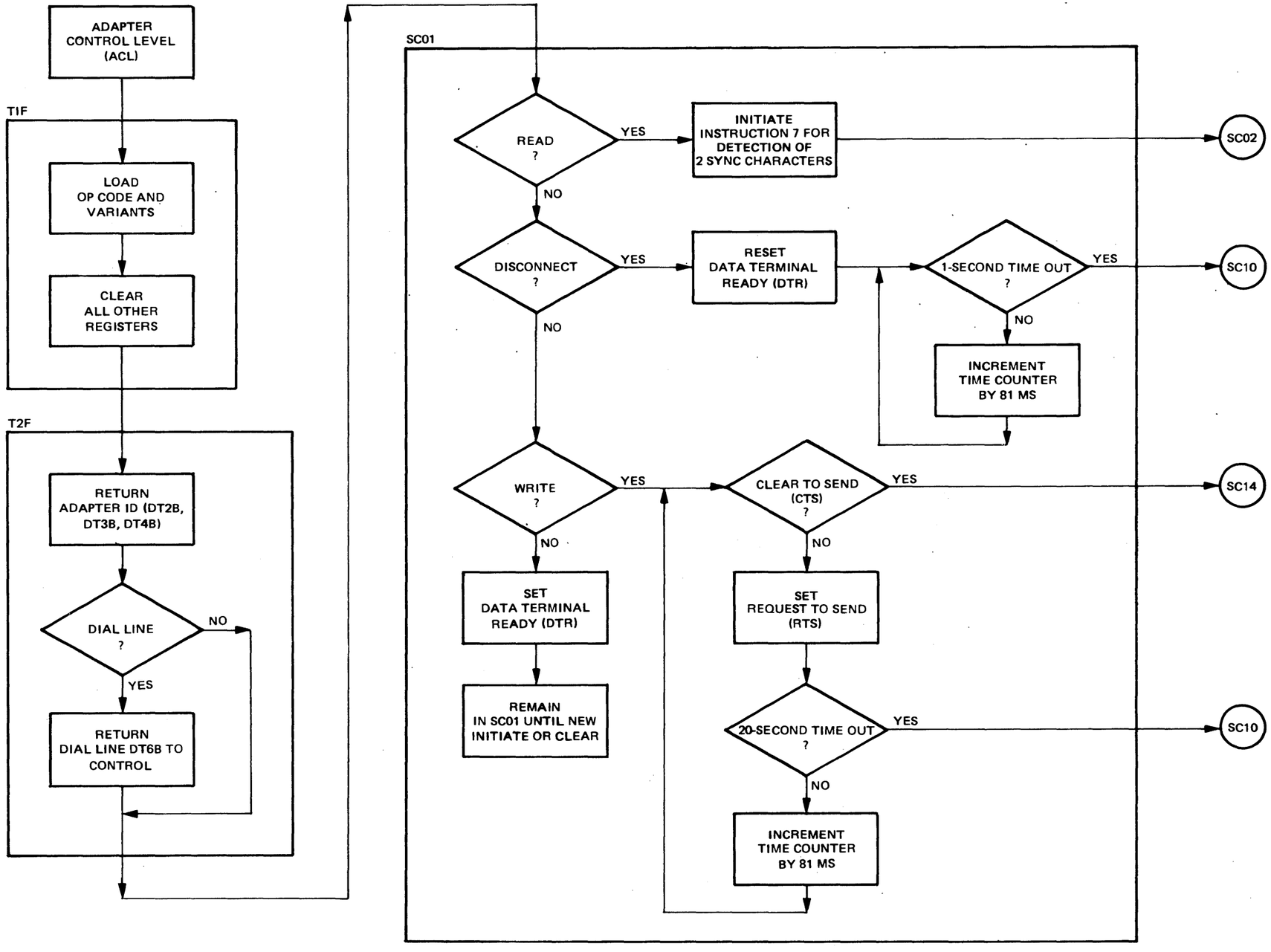

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Figure 11-3. Detailed Flow Chart, WIDEBAND Adapter (Sheet 1 of 7)

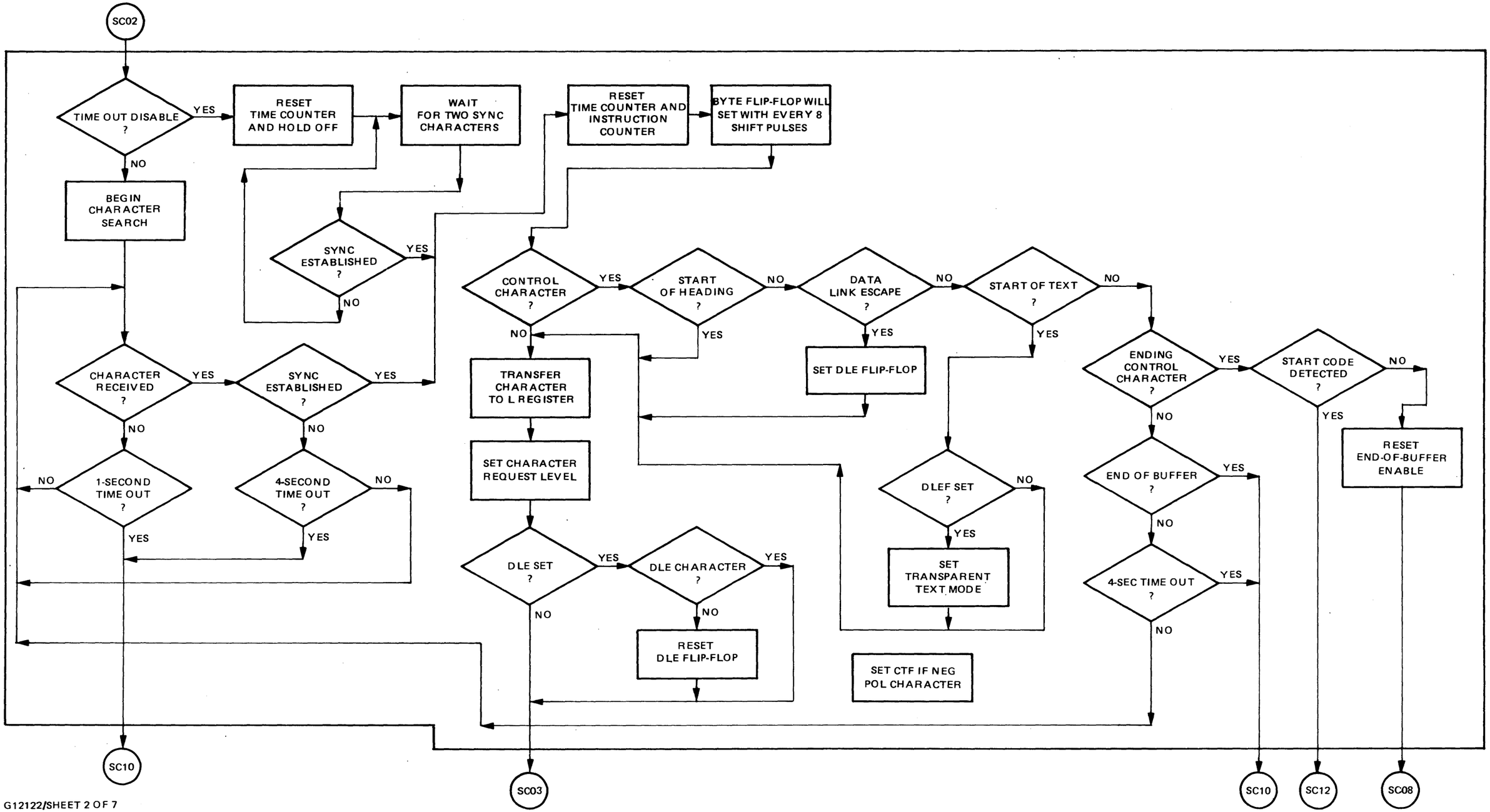

Figure 11-3. Detailed Flow Chart, WIDEBAND Adapter (Sheet 2 of 7)

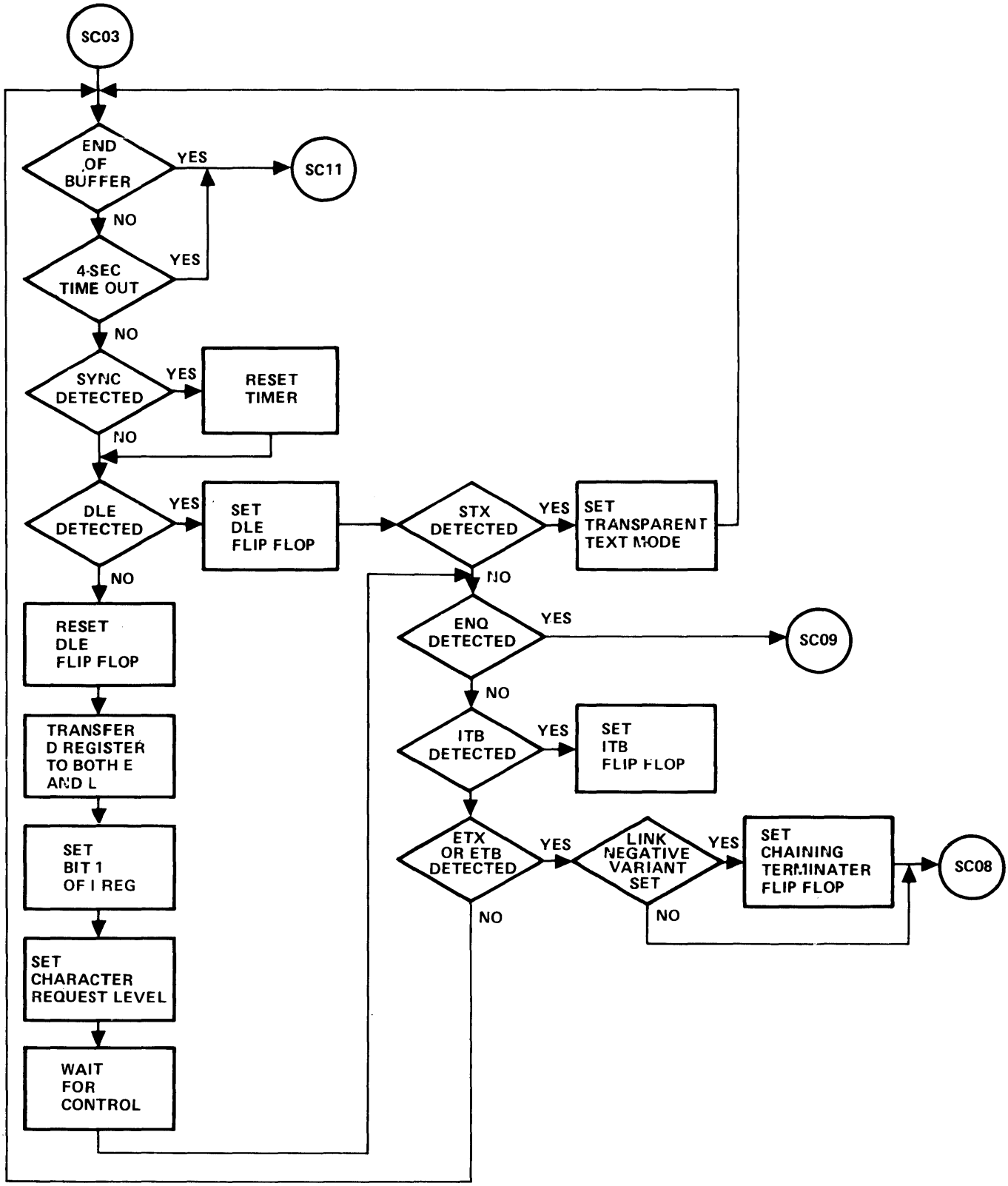

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Figure 11-3. Detailed Flow Chart, WIDEBAND Adapter (Sheet 3 of 7)

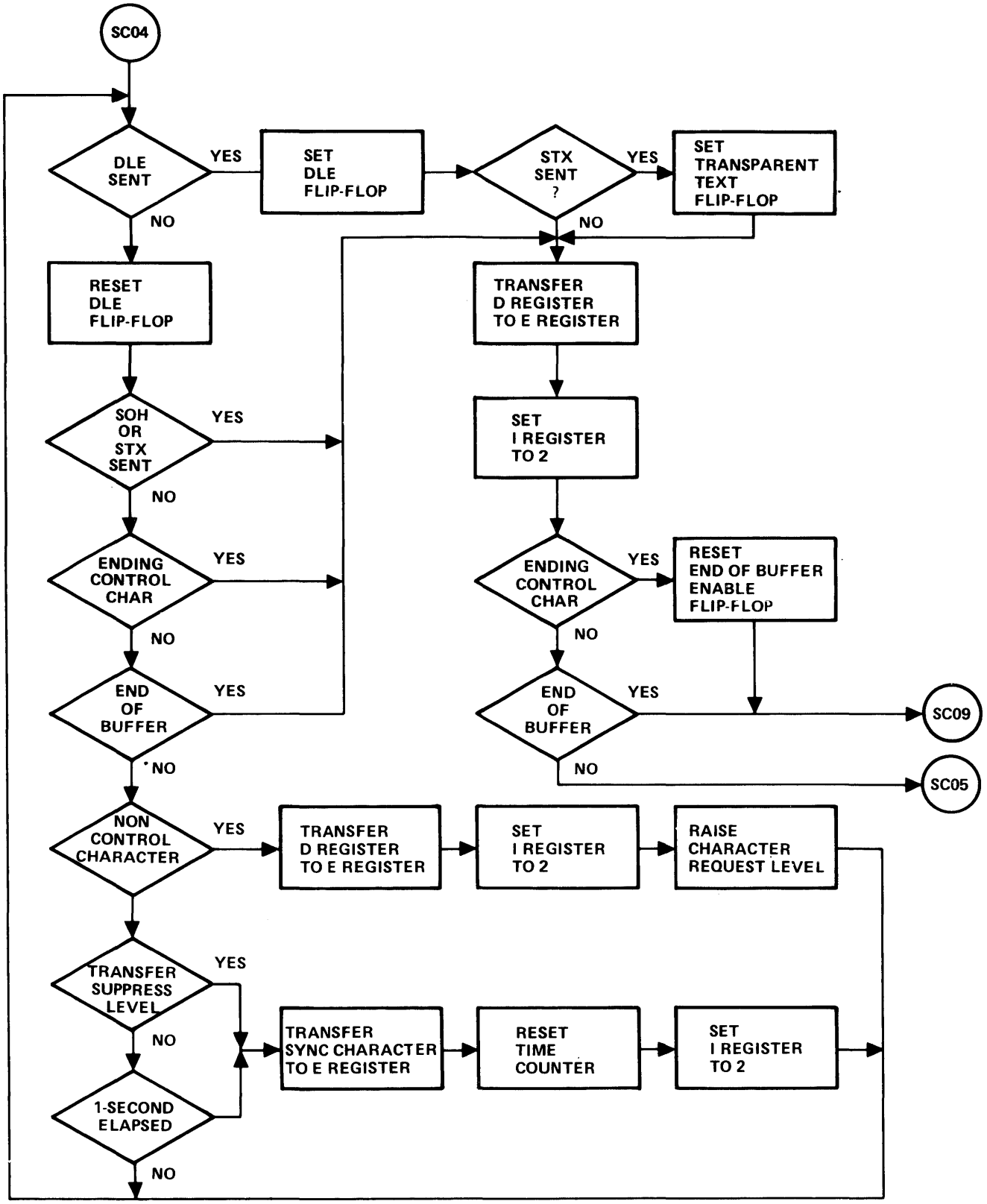

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Figure 11-3. Detailed Flow Chart, WIDEBAND Adapter (Sheet 4 of 7)

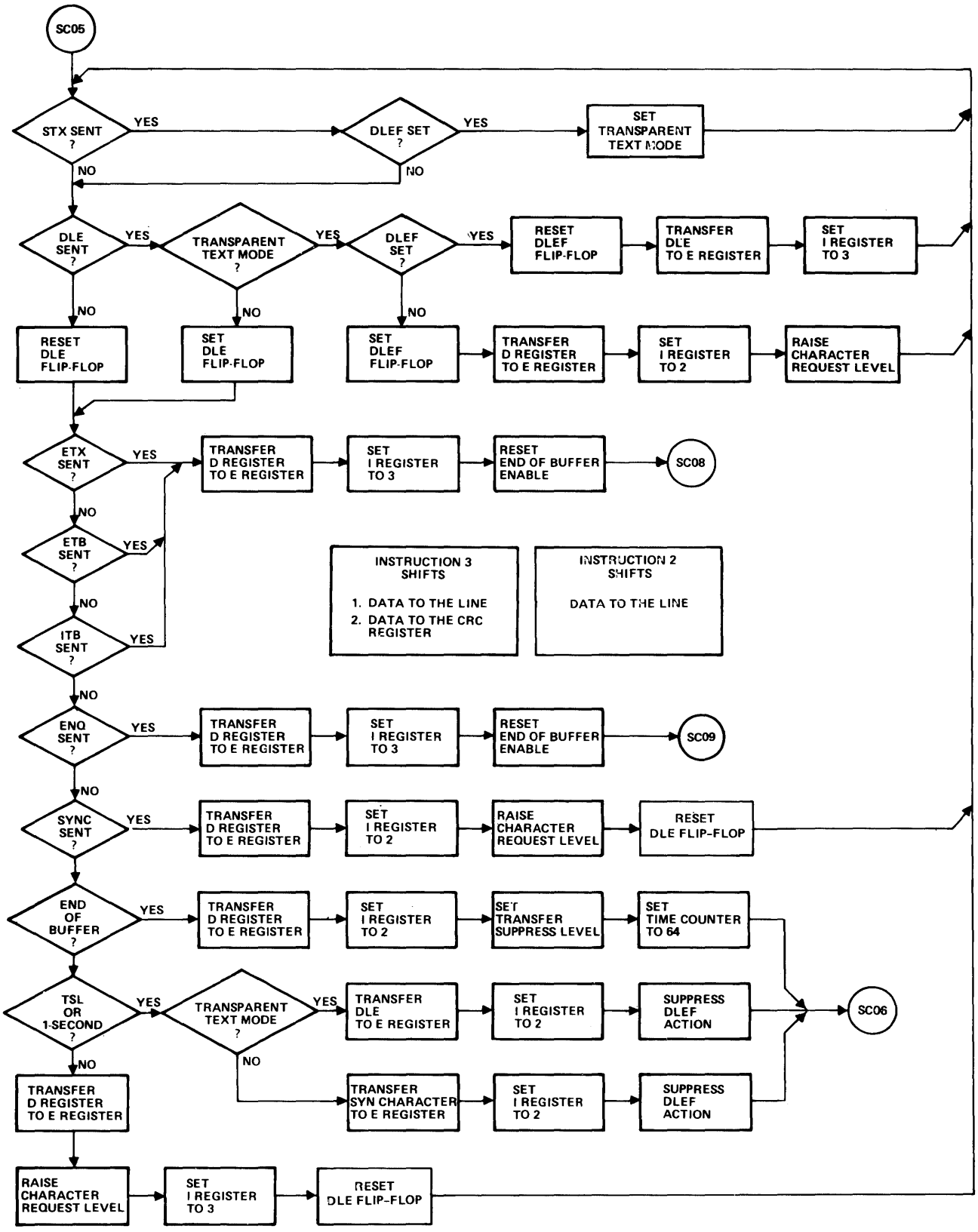
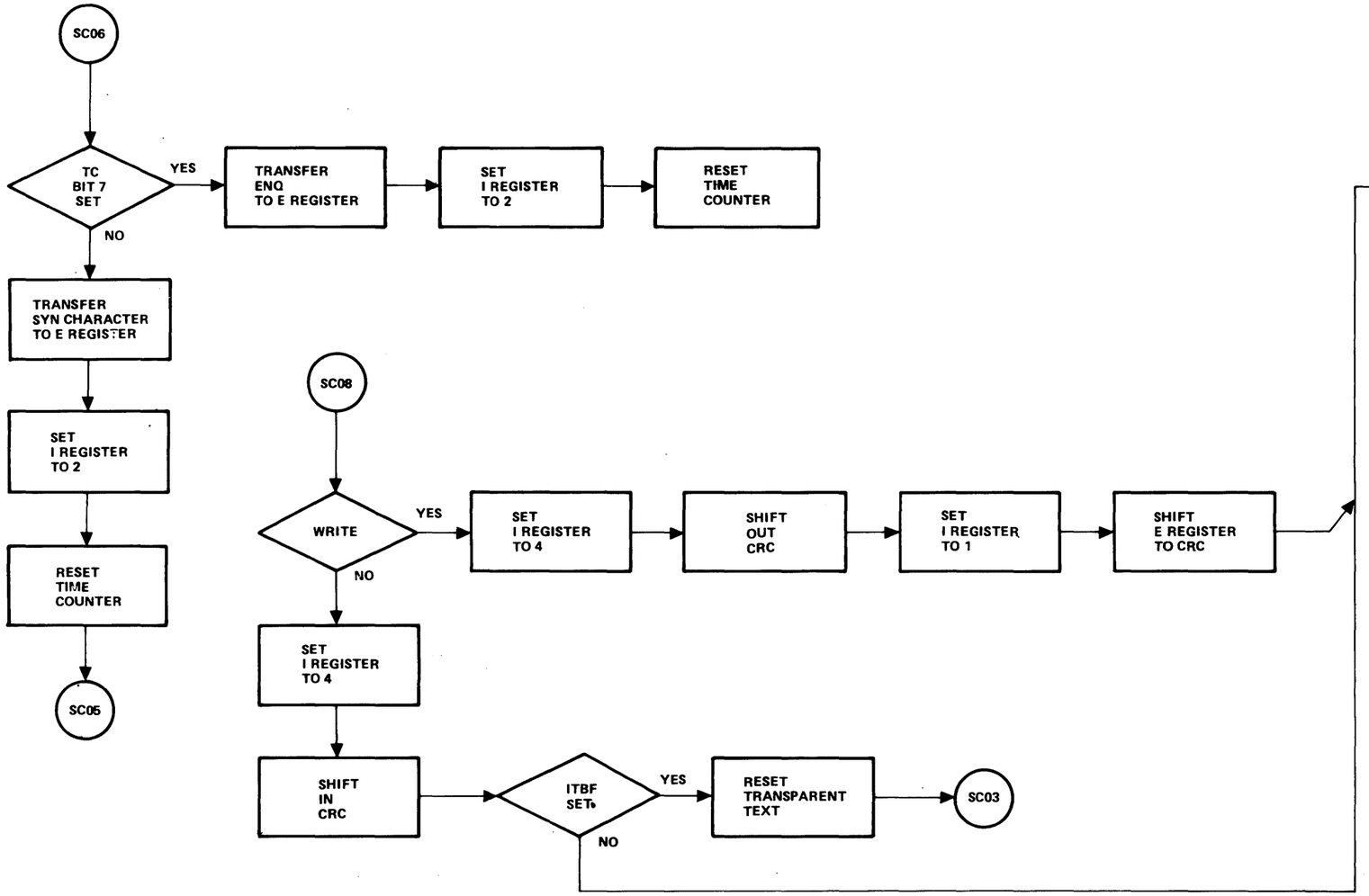


Figure 11-3. Detailed Flow Chart, WIDEBAND Adapter (Sheet 5 of 7)



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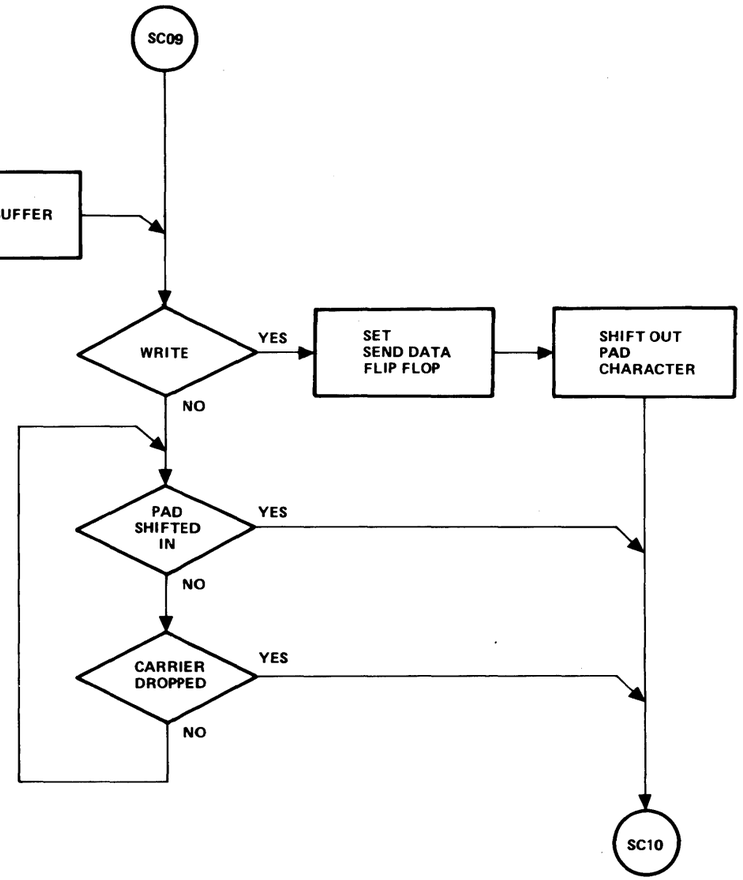

Figure 11-3. Detailed Flow Chart, WIDEBAND Adapter (Sheet 6 of 7)

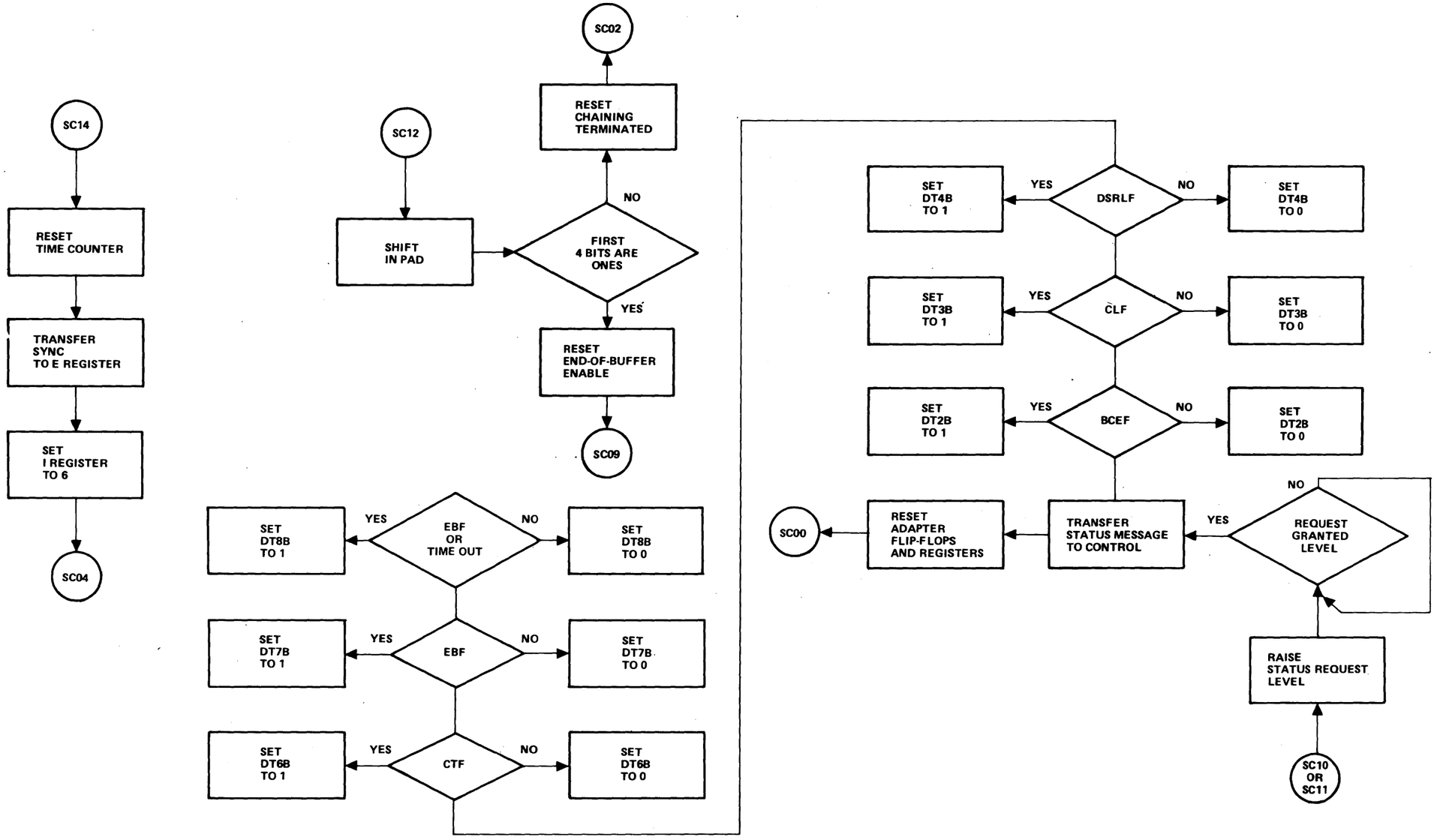

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Figure 11-3. Detailed Flow Chart, WIDEBAND Adapter (Sheet 7 of 7)

SECTION 12
BINARY SYNCHRONOUS LINE ADAPTER

INTRODUCTION

The Binary Synchronous (BISYNC) line adapter is the interface between a single-line or multi-line control and synchronous data sets employing the RS-232-C interface. This adapter uses the standard 8-bit, 256-character EBCDIC code set.

Terminal devices for BISYNC adapters must have binary synchronous capabilities. Some of the data sets that can be connected are listed in table 12-1.

The BISYNC adapter may be strapped for either 2-wire or 4-wire operation. When strapped for 2-wire operation, the adapter enables a circuit that squelches all input data for 96 milliseconds. Continuous Carrier is a strappable option that eliminates data set turnaround time on 4-wire operation.

Table 12-1. BISYNC Data Set Characteristics

Speed (bps)	Service	Data Set
600		Datel 7 V.26
1200		Datel 7 V.26
2400		Datel 7 V.26
2000	Dial (DDD)	WE201A3
2400	Leased	WE201B3, WE201B1, TA734-24, TA774-24
3600	Leased	
4800	Leased	WE208 TA733-48, TA733-48
7200	Leased	
9600	Leased	

In receive mode prior to synchronization, the adapter detects the absence of two contiguous sync characters for more than 4 seconds (or 1 second if so specified by the C variant in the Read OP. Once synchronization has been established, the adapter detects the absence of a sync pattern or a control character for more than 4 seconds. The 4-second time-out can be programmatically inhibited, but the variant-specified 1-second time-out cannot be so inhibited.

In transmit mode, time-out occurs if a Clear To Send or Data Set Ready signal is not returned within 20 seconds after Request To Send. This time-out cannot be inhibited. The adapter can be strapped for 4, 32, or 128 milliseconds of write delay time in order to allow sufficient turnaround time for certain remote units.

The following options can be strapped by the Burroughs field engineer:

Switched or leased Line.

2-wire or 4-wire operation.

Controlled or continuous carrier, with or without New Sync control.

Enabling or disabling of checking for the pad character following a control code on Read.

Write delay time selection: 4, 32, or 128 milliseconds.

EBCDIC or transparent data may be transmitted. Data from system memory is transmitted in 8-bit groups, LSB first. No character parity is employed. BCC characters, which are included in all messages containing a start code, are generated by the following polynomial: $X^{16} + X^{15} + X^{15} + X^2 + 1$

BCC is inserted immediately after each ITB (DLE ITB in transparent mode) and immediately after the ending (or ending-transparent) code.

Read, Write, and Test OPs set the Data Terminal Ready (DTR) line to the on state. If Data Set Ready (DSR) is not returned within 4 seconds on a Read OP with the time-out variant set, absence of DSR and time-out are reported in the result descriptor. A Read OP with the time-out variant reset (0) is not reported; the adapter remains inoperative until it is cleared. On a Write OP, if Clear To Send is not returned within 20 seconds, time-out and absence of DSR are reported.

UNIT IDENTIFICATION

The BISYNC line adapter is contained on one logic card, identified by the 8-digit Burroughs M&E number 2209 7778 imprinted on a metal unit identification label supplied with the unit's Field Test and Reference (FT&R) documentation. When the adapter is installed into the system, this label must be affixed on the end of the 28-position card housing assembly that contains the adapter.

CONTROL CODE SENSITIVITY

Control code sensitivity for the BISYNC line adapter is listed in table 12-2.

A control code classified as a start code is used to start the accumulation of a block check character (BCC). The accumulation starts with the next non-sync code and includes all codes except SYN up to and including an ending code or an ITB. However, in transparent mode, the first DLE of all DLE XXX sequences and the SYN code in all DLE SYN sequences are not included in the BCC summation. A SYN code, if not part of a DLE SYN sequence, is included. The DLE STX sequence invoking the transparent mode is included only when it is preceded by start code.

A control code sequence classified as a start-transparent code sequence is used to start a transparent mode of operation. It is also used to start accumulation of a BCC if this has not already been started by a prior start code. Some examples of BISYNC code sensitivity are shown in figure 12-1.

Table 12-2. BISYNC Line Adapter Control Code Sensitivity

Code	Function
SOH	Start
DLE STX	Start-transparent
ETX	Ending
ETX	Ending-transparent
DLE ETB	Positive response
ENQ	
DLE ACK0	Negative response
DLE ACK1	
DLE WACK	
DLE RVI	
NAK	
EOT (optional)	Intermediate transmission
ITB	block
DLE ITB	Intermediate Transmission block-transparent
DLE	Data Link Escape
SYN	Synchronization code
DLE SYN	Synchronization code-transparent
ENQ	Abort
DLE ENQ	Abort-transparent
1111 1111	Pad
STX ENQ	Temporary text delay (TTD)

In transparent mode, only an ending-transparent code sequence or an abort-transparent code sequence terminates a Read operation. A Write operation is terminated when the write data memory address equals the B address. The applications program must ensure that the last two codes in the data to be transmitted are DLE ETX, DLE ETB, DLE ITB, or DLE ENQ. If none of these code sequences are present, the control will add a DLE ENQ sequence in place of the BCC.

In non-transparent mode, after receipt of a start code, only an ending code or an abort code terminates a Read operation. A Write operation is terminated by an an ending code, an abort code, or an intermediate transmission block code.

In non-transparent mode, a response code terminates the operation only if it is not preceded by a start code (abort code excepted). A response code is defined only in non-transparent mode.

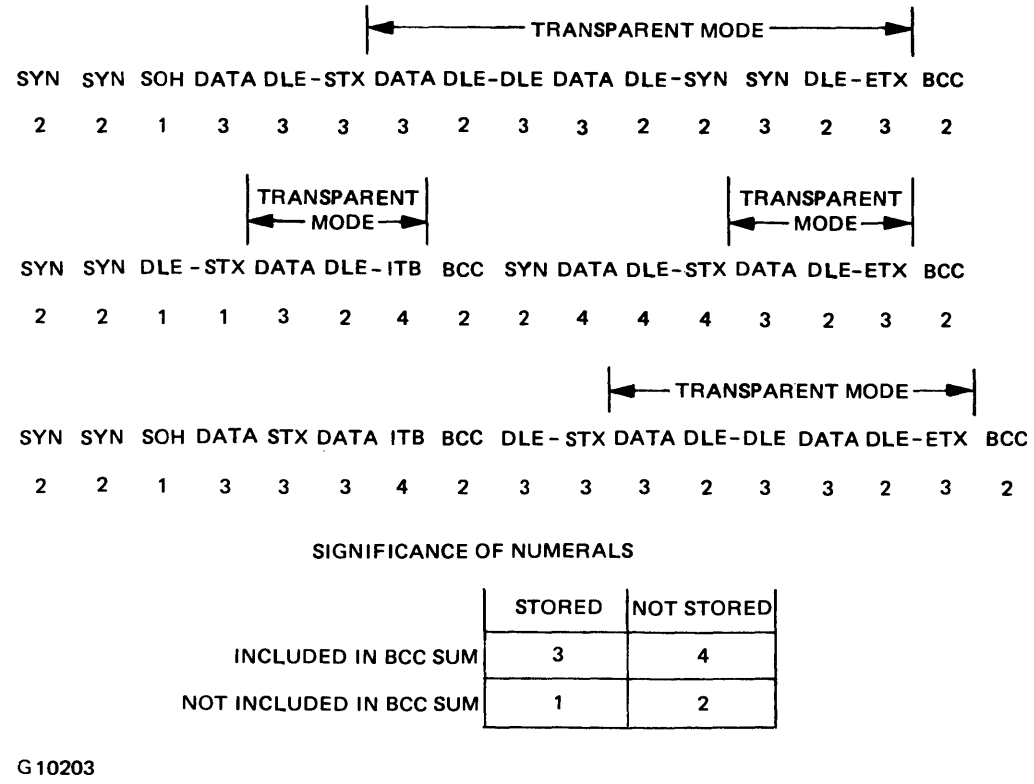


Figure 12-1. Examples of Control Code Sensitivity; BISYNC Adapter

In non-transparent mode, an ITB code terminates a Write operation. The control appends a BCC after the ITB code. On a Read operation, receipt of an ITB code does not terminate the operation. The adapter deletes and does not store the ITB and BCC, but remains in character sync and stores subsequent codes. However, the BCC for the intermediate block is checked.

In transparent mode, an ITB transparent code sequence does not terminate a Write operation. On a Read operation, receipt of the DLE ITB code sequence also does not terminate the operation. The adapter checks the BCC, remains in character sync, and reverts to non-transparent mode. The DLE ITB, the BCC, and all subsequent codes up to and including a DLE STX code sequence are not stored. The characters that follow the DLE STX sequence are stored normally.

In a Write-transparent mode, the adapter automatically inserts a DLE code any time it receives a DLE from memory, forming a DLE DLE sequence. (Exception: this is not the case when the DLE code immediately precedes the last character received from memory.) In a Read-transparent mode, the adapter automatically deletes the first DLE of all DLE XXX sequences received, including ending code sequences.

Two sync codes must be received before the adapter is sensitive to any other codes. Sync codes are not stored in memory. After the receipt of the last leading sync code, the adapter stores in memory all subsequent codes except sync codes and ITB up to and including the BCC. A sync code is not included in the BCC sum. Four sync codes are inserted by the adapter and are transmitted prior to transmission of data. During transmission, the adapter automatically inserts a pair of sync codes (or one DLE SYN if in transparent mode) once per second as well as any time data is unavailable due to a memory access error. However, if a memory access error occurs on the STX portion of a DLE STX character (start code, transparent mode) or the ETX, ETB, or ITB portion of one of the stop-transparent mode characters (DLE ETX, DLE ETB, DLE ITB), the adapter terminates the operation.

When a parity error occurs in the start-transparent mode, the control terminates the operation by sending DLE DLE and SYN ENQ. In the ending-transparent mode, a parity error causes the control to terminate the operation by sending DLE DLE ETX-DLE ENQ.

The abort code is used (following a start code) to abort the operation. No BCC follows the abort code. The adapter automatically generates this pattern upon detection of a memory parity error or upon detecting a data memory address equal to the B address without an ending code. If abort is received, the operation is terminated in the normal manner and no error is reported. The SLC does not provide the adapter with memory parity error information.

To ensure that the last characters of all transmissions are properly transmitted by the data set, the adapter adds a pad character, following BCC, ENQ, and the response code. On output, the adapter checks only the first four bits for ones (1111) after receiving a response code. If the first four bits are not 1111, the adapter continues to receive and store data.

A variant allows EOT to be ignored as a response code on Read and Write. On Read, the same variant allows the control and the associated system to act as a terminal and receive a polling sequence from other systems. However, hardware recognition of addresses is not provided. On Write, variant allows the data communications control to ignore EOT in order to transmit polling and other sequences that use EOT as the first code in a message for line clearing.

A variant is provided on Read to allow the time-out caused by a failure to receive the first character within 1 second to be treated exactly as if a negative response character had been received. Normally, this variant is used in conjunction with two other variants (poll, link on negative response) to allow non-present terminals to be ignored. A STX ENQ can be sent or received to indicate temporary text delay. No BCC follows the STX ENQ sequence.

ETX, ETB, and ITB always terminate an operation. If these codes are not preceded by STX or SOH, a BCC error is reported on Read; on Write, BCC is omitted but the pad character is transmitted.

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

Read

The Read operator causes data to be accepted from the remote device and stored into ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

0000 T0D- CEVV P--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII to EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
C = 0: Do not treat time-out on first character as negative response.
= 1: Treat time-out on first character as negative response.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
VV=00: Normal linking.
=01: Link only if negative response is received.
=10: Link only if positive response is received.
=11: Undefined.
P = 0: Do not Poll.
= 1: Poll.

Write

The Write operation causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B address minus one is reached.

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the Result Descriptor for the terminated operation.

0100 T000 0E00 PLLL L--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
P = 0: Do not Poll.
= 1: Poll. (Start with the location specified by the E address.)
LLLL 0010-1101: Length of poll sequence.

Break (Disconnect)

The Break operator causes an in-process operation, if any, to be terminated. A Break disconnects the adapter by turning the Data Terminal Ready (DTR) signal off. The result descriptor is returned one second after DTR is turned off.

1100 00-- ---- ---- ---- UUUU

Test

The Test operator is a request for the reporting (in the result descriptor) of the adapter's identification and the conditions specified by the VM variant combination.

100V --M- ---- ---- ---- UUUU

VM=00: Complete the operation normally. Do not change the status of the Data Terminal Ready signal.
=01: Wait until a ringing condition is true, then completes the operation. (Switched line only; others wait "forever.")
=10: Make the Data Terminal Ready signal true, then complete the operation.
=11: Make DTR true, then wait until the Data Set Ready signal is true before completing the operation. (Switched line only.)

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the STD/BDI line adapter are listed below, together with their meanings when set. Omitted bits in the sequence 0-23 are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception conditions. (Except for Test, this bit is set if any of bits 2-15 are set.)
3	Parity error character or BCC (Read).
4	Memory access error (Read).
5	Memory parity error (Write).
6	Time-out (Read or Write).
7	Break received (Write).
9	Linking terminated (Read; VV = 01 or 10).
16	Operation completed.
17	Data communications device (Test).
18-23	Adapter ID (Test): 000000 = adapter not present 001010 = BISYNC adapter, leased line 101010 = BISYNC adapter, switched line

FUNCTIONAL DESCRIPTION

Block Diagram

Figure 12-2 is a block diagram of BISYNC adapter hardware. The functions of the BISYNC adapter are primarily controlled by a sequence counter (SC), the instruction counter (I counter), and the instruction register (I register). The sequence counter defines the basic operating states of the adapter (SC00 through SC15). The I register is a 3-bit register that defines specific operations concerning data transfer. The I counter controls the duration of an operation. I register and I counter functions are listed in table 12-3.

Other components essential to the functioning of the BISYNC line adapter are listed below.

Time counter (T counter)

D register

E register

L register

Cyclic redundancy character register (CRC register)

OP variant register

Character decoder

Table 12-3. Functions of the I Register and I Counter

A	B	Function	I Counter	Mode
000	0	Idle		
001	1	Shift E to CRC	8 clocks	Read
010	2	Shift E to line	8 shift pulse	Write
011	3	Shift E to line	8 shift pulses	Write
100	4	Compare accumulated CRC incoming CRC	16 shift pulses	Read
101	5	Shift CRC to line	16 shift pulses	Write
110	6	Rotate E and shift to line	24 shift pulses	Write
111	7	Shift bits in until SYN SYN pattern is detected		Read

A: I register contents.
B: Instruction number.

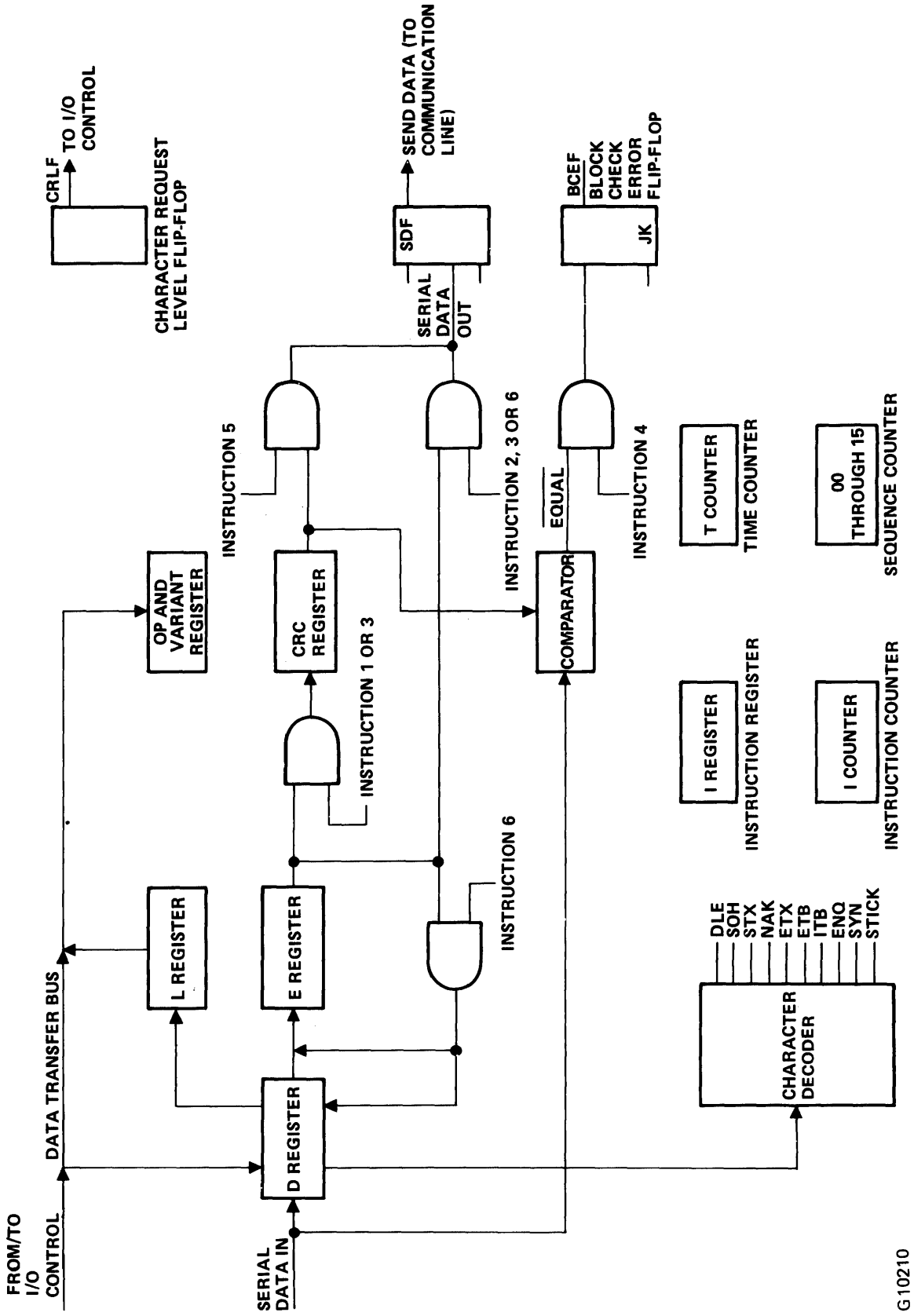


Figure 12-2. Block Diagram, BISYNC Adapter

On a Write operation, the D register receives a character from the bus. The character is inspected for control significance by the character decoder. If it is a control code, it is transferred to the E register, then shifted from the E register to the communication line. If the character is text, it is shifted to the CRC register where the cyclic redundancy count is made and stored, and then shifted to the communication line. (CRC logic is depicted in figure 12-3.)

When a complete text message has been received, the accompanying CRC character is compared with the contents of the CRC register. Non-correspondence causes the Block Check Error flip-flop to be set.

The CRLF (Character Request Level flip-flop) indicates to the control that the adapter is ready to either receive or send a character to or from the control.

The time counter generates 1-second markers for insertion of SYN characters. The time counter also provides squelch delay time-out periods of 4 and 20 seconds.

The D, E, and L registers are each 8-bit registers. The D register operates in shift mode during Read to stabilize an incoming character. This character is transferred to the L register where it is held until it can be transferred over the data transfer bus to the control.

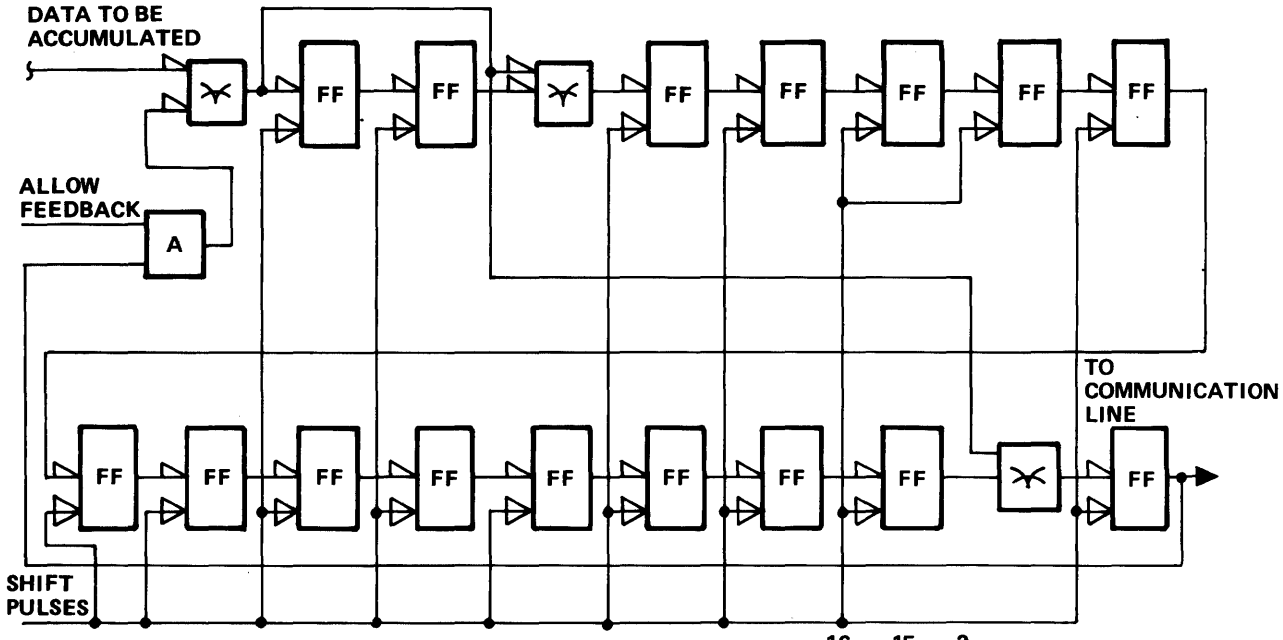


Figure 12-3. CRC Logic, BISYNC Adapter

Sequence Counter

The sequence counter is a 4-bit counter providing sequence counts of 00 through 15. The functions fulfilled by the individual counts are described in the subsections that follow.

SC00

SC00 is the no-action state of the adapter.

SC01

Initial delay state. Time-out periods are generated for Read, Write, and Break. Test causes the adapter to remain in SC01 until the next initiation or until a system general-clear occurs. Any other operation code causes an exit from SC01. A Read operation exits to SC02, a Write operation exits to SC04, and a Break (Disconnect) exits to SC10.

SC02

Read, non-text mode. This mode terminates when an ending control code, an SOH, or an STX character is detected. An ending control code causes an exit to SC12. An SOH or STX causes an exit to SC03. This mode also terminates when Data Set Ready goes false, or if a SYN character is not detected in the data stream within a period of 4 seconds. Transparent operation cannot occur in this mode.

SC03

Read, text mode. SC03 terminates with the detection of an ENQ, EXT, ETB or ITB character. Data received during this mode can be either transparent or non-transparent. An ENQ causes an exit to SC09. An ETX, ETB, or ITB causes an exit to SC08. The operation terminates during SC03 if Data Set Ready goes false or if a SYN character (or DLE SYNC during transparent operation) is not detected in the data stream within a period of 4 seconds.

SC04

Write, non-text mode. This mode terminates when an ending control code, an SOH, or an STX is transmitted. An ending control code causes an exit to SC09. An SOH or STX character causes an exit to SC05. The operation terminates during SC04 if Data Set Ready goes false or if an end of buffer condition occurs before an ending control code is transmitted. A pair of contiguous SYN characters are inserted in the data stream at 1-second intervals during the sequence mode.

SC05

Write, text mode. This mode terminates when an ENQ, ETX, ETB, or ITB character is transmitted. Data transmitted during this state can be either transparent or nontransparent. An ENQ causes an exit to SC09. An ETX, ETB or, ITB causes an exit to SC08. The operation terminates during SC05 when Data Set Ready goes false or if an end of buffer condition occurs before an ending control code is transmitted. A pair of contiguous SYN characters (DLE SYN during transparent operation) are inserted into the data stream at 1-second intervals.

SC06

SC06 occurs only during a Write operation. During SC06, the second SYN of a SYN SYN (or the SYN of a DLE SYN in transparent mode) is transmitted. SC06 is also used to append an ENQ to the transmitted message in certain error situations, to inform the receiving station to ignore the message.

SC07

Not used.

SC08

During this mode, the 16-bit CRC is transmitted when the operation is a Write, or received when it is a Read. During a Read operation, the incoming CRC character is compared with the accumulated CRC character. A comparison error sets BCEF (the Block Check Error flip-flop).

SC09

During this mode, a pad character consisting of all ones is shifted out if the operation is a Write and shifted in if the operation is a Read.

SC10

During SC10, the adapter transfers a result status word to the I/O control. The transfer signifies that the operation is terminated. Bits in the result descriptor convey exception-condition information.

SC11

Same as SC10. A logical simplification of the adapter resulted from the inclusion of two identical sequences, the only reason for the existence of SC11.

SC12

SC12, which occurs only during a Read operation, is used to check the first four bits of the pad character for 1111.

SC13

Not used.

SC14

SC14, used for the Write operation only, delays transmission of the first character by a strap-selectable time interval. The interval may be 4, 32, or 128 milliseconds.

SC15

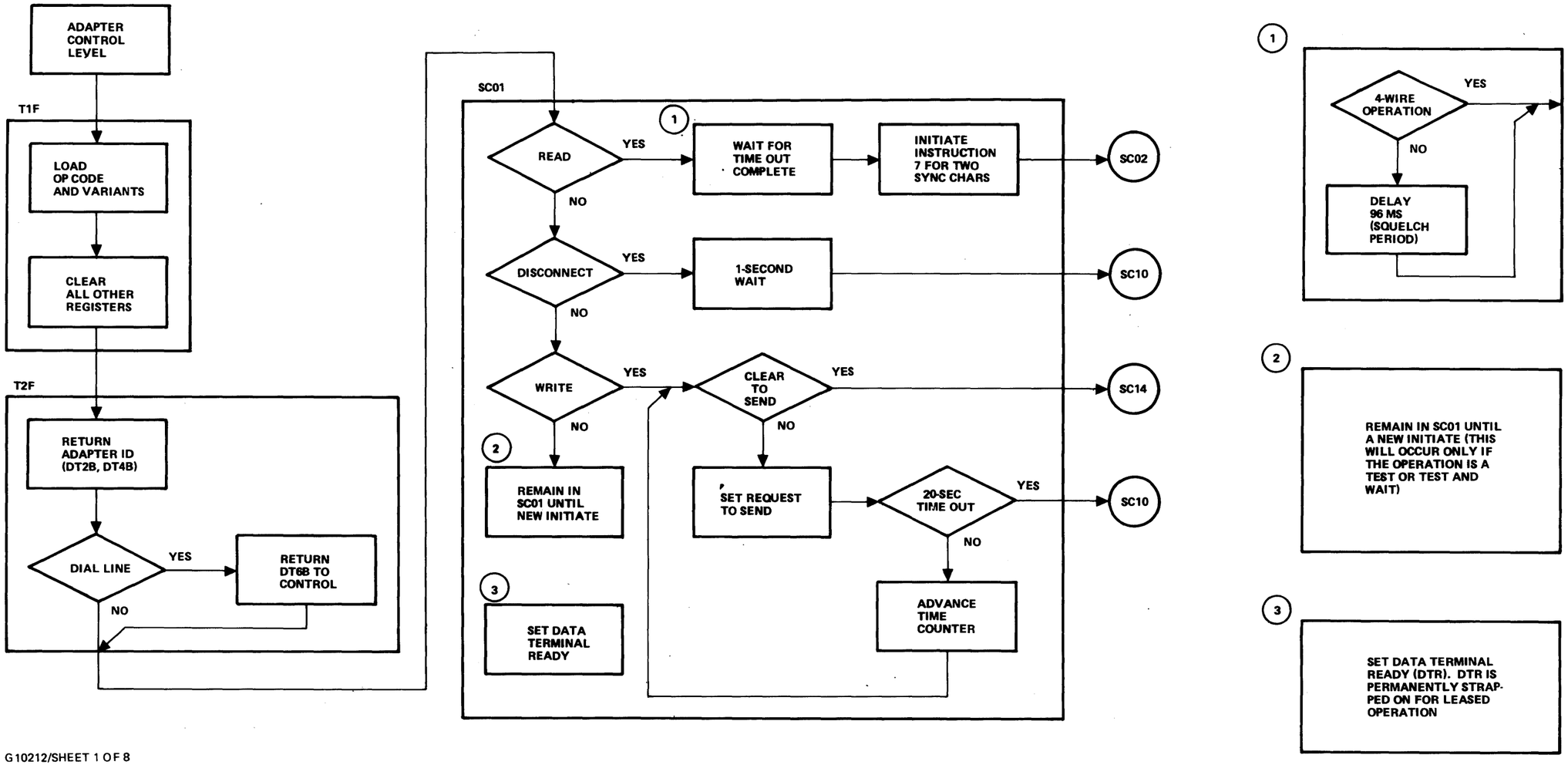
Not used.

SUMMARY

Characteristics of the BISYNC line adapter that distinguish it from standard adapters include the following:

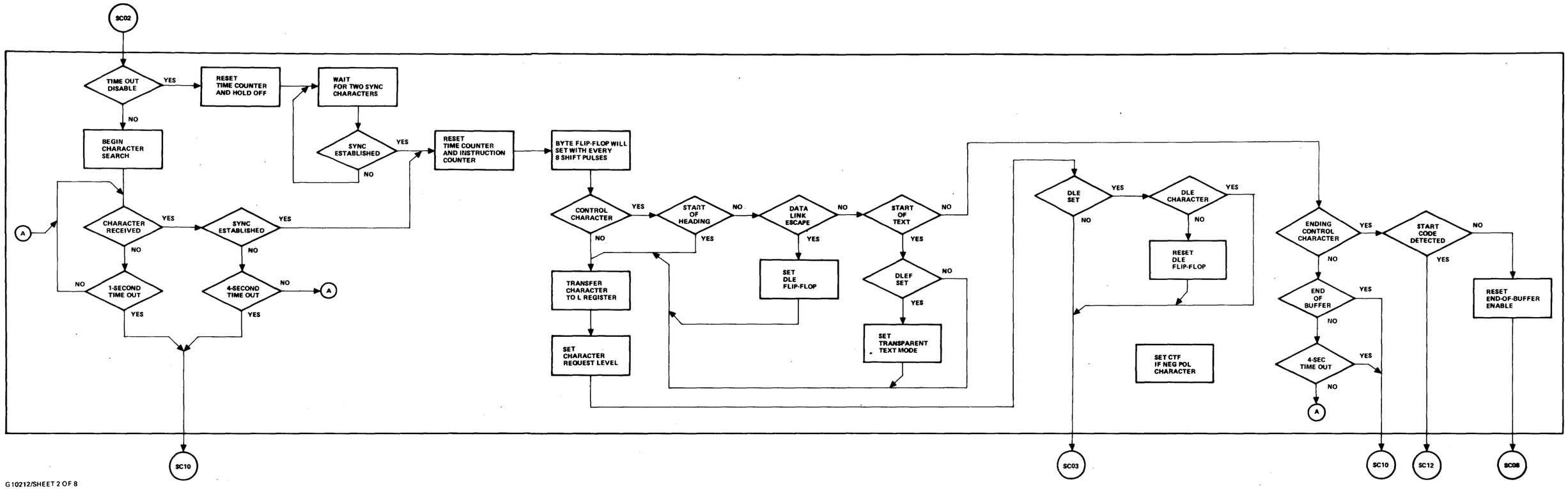
1. Normal data transmission (non-transparent) is in EBCDIC rather than USASCII.
2. A transparent mode is available. In this mode all data, including normal line control characters, is treated as bit-patterns. This permits unrestricted coding of data.
3. A 16-bit cyclic redundancy code is used for block error checking; character parity is not used.
4. A SYN character (or DLE SYN for transparent operation) is inserted into the data stream at 1-second intervals. The detection of this character by the receiving terminal ensures that character synchronization is maintained.

Figure 12-4 is a detailed flow chart of this line adapter.



G10212/SHEET 1 OF 8

Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 1 of 8)



G10212/SHEET 2 OF 8

Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 2 of 8)

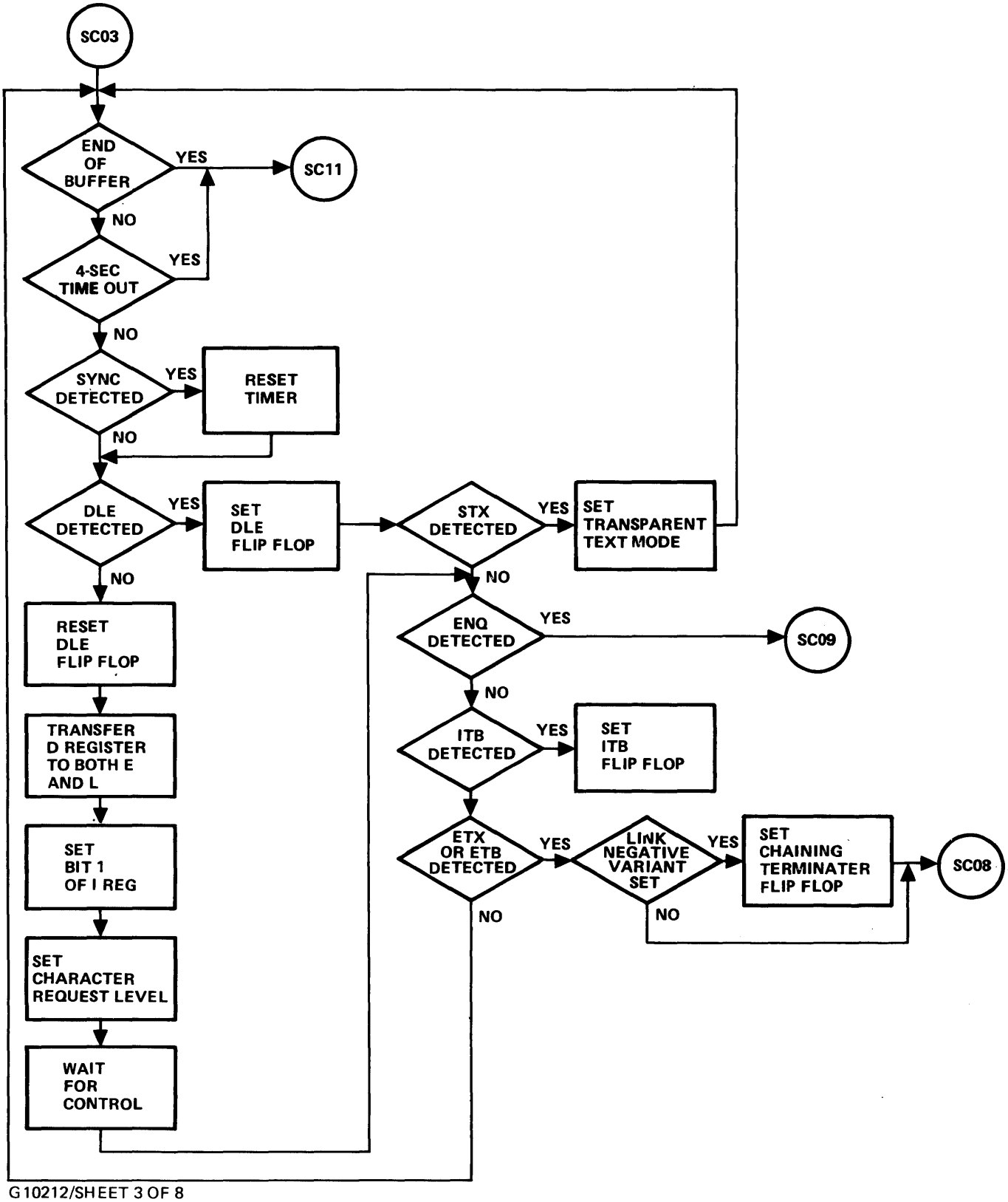


Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 3 of 8)

SC04

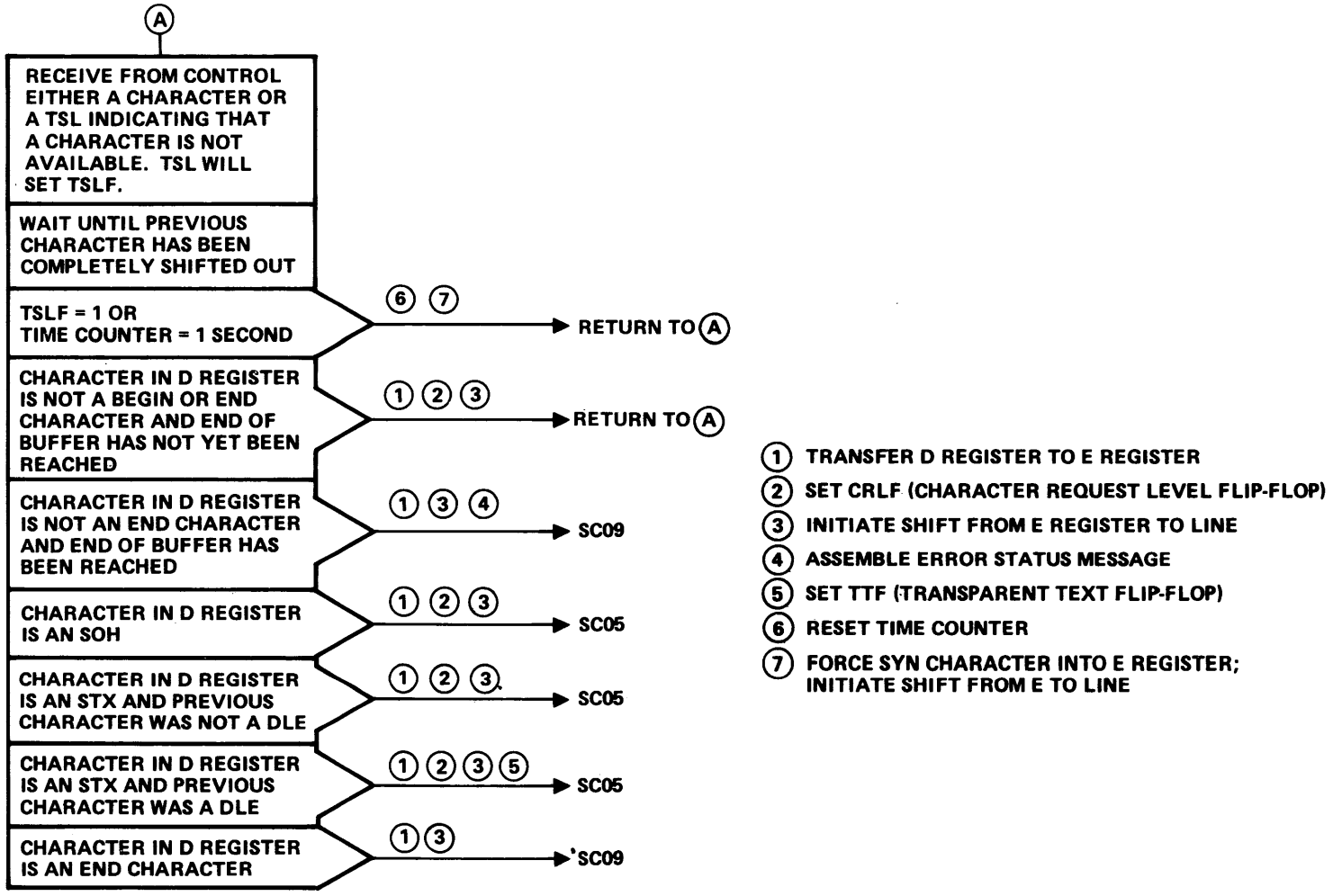


Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 4 of 8)

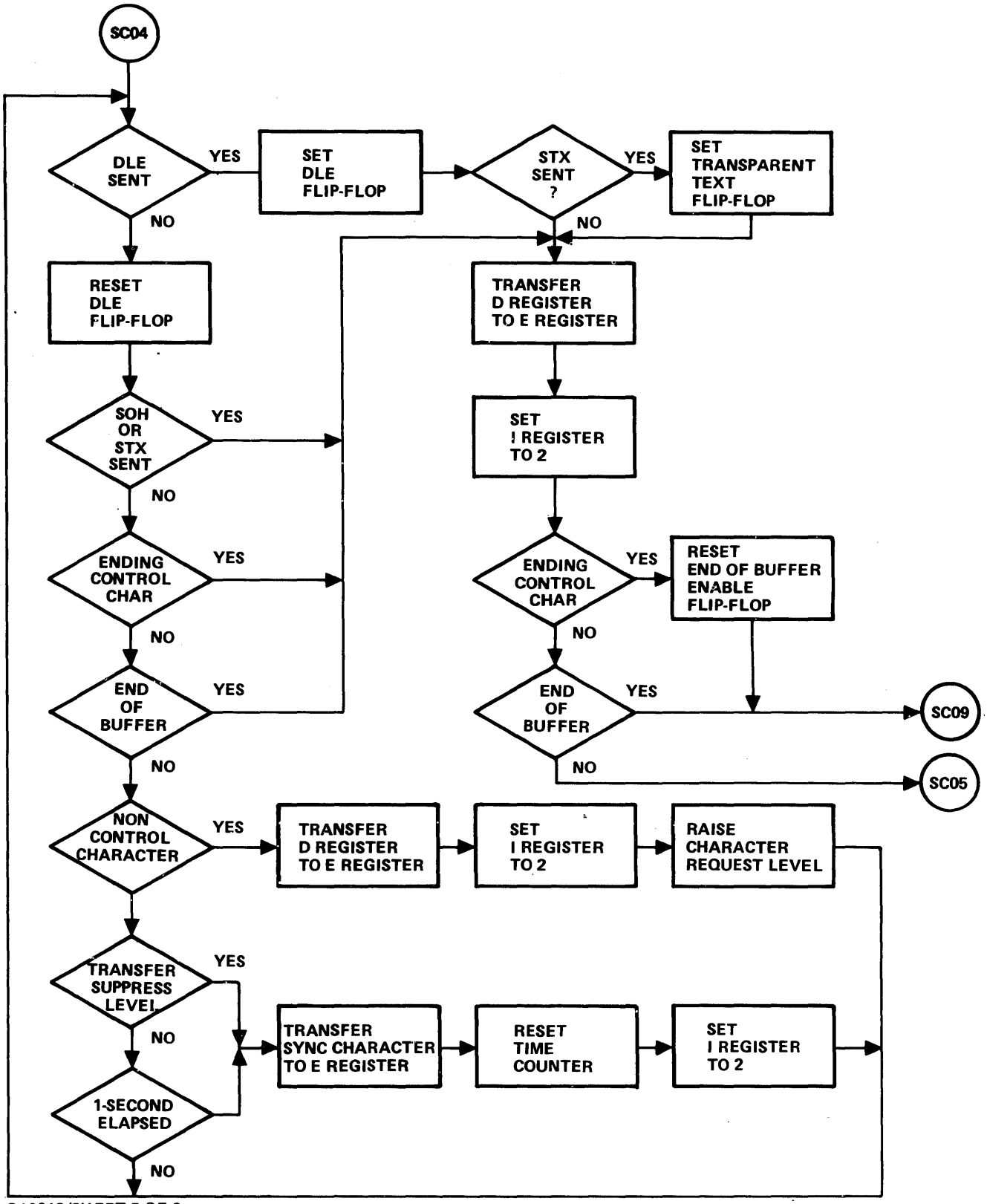


Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 5 of 8)

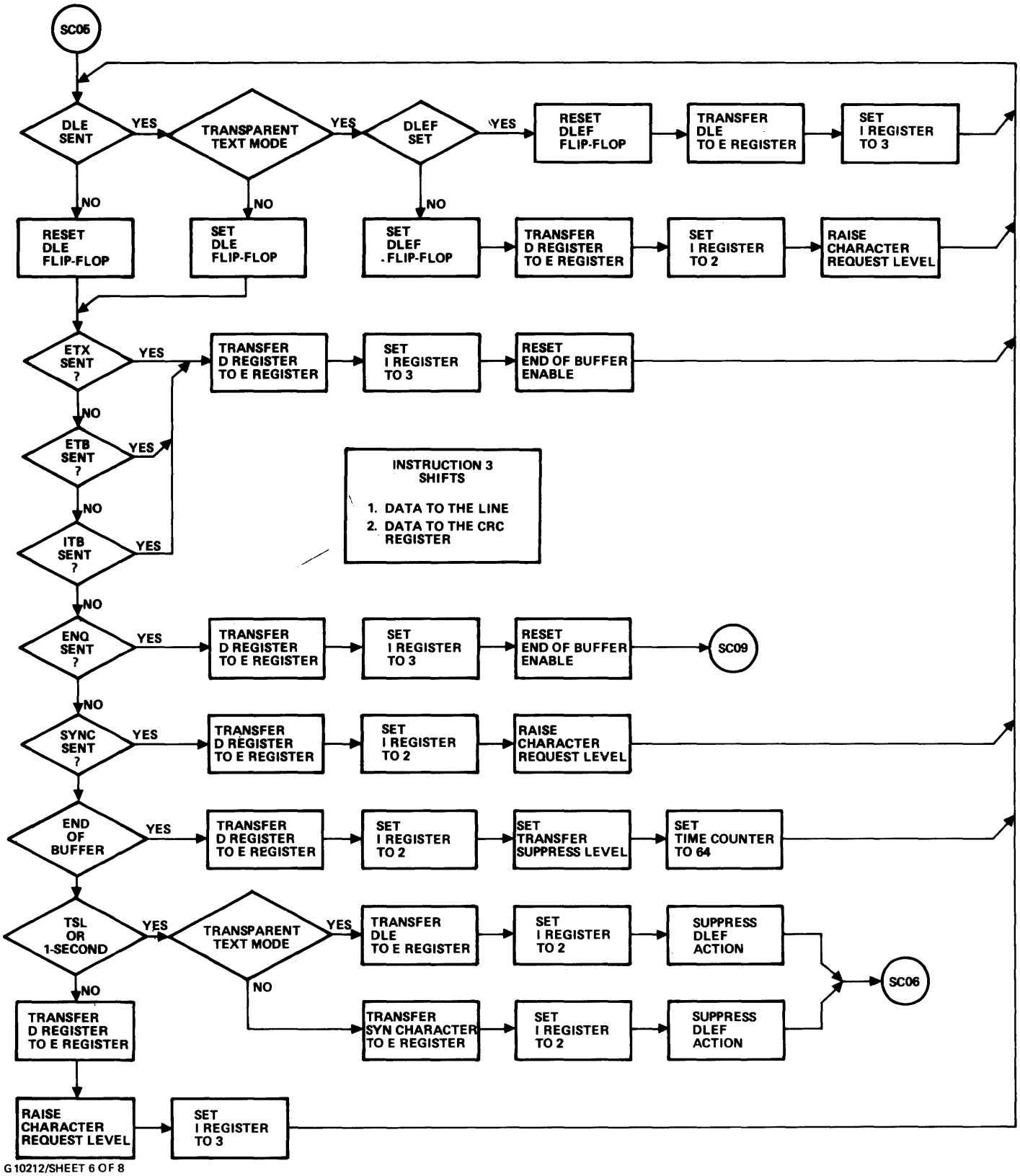
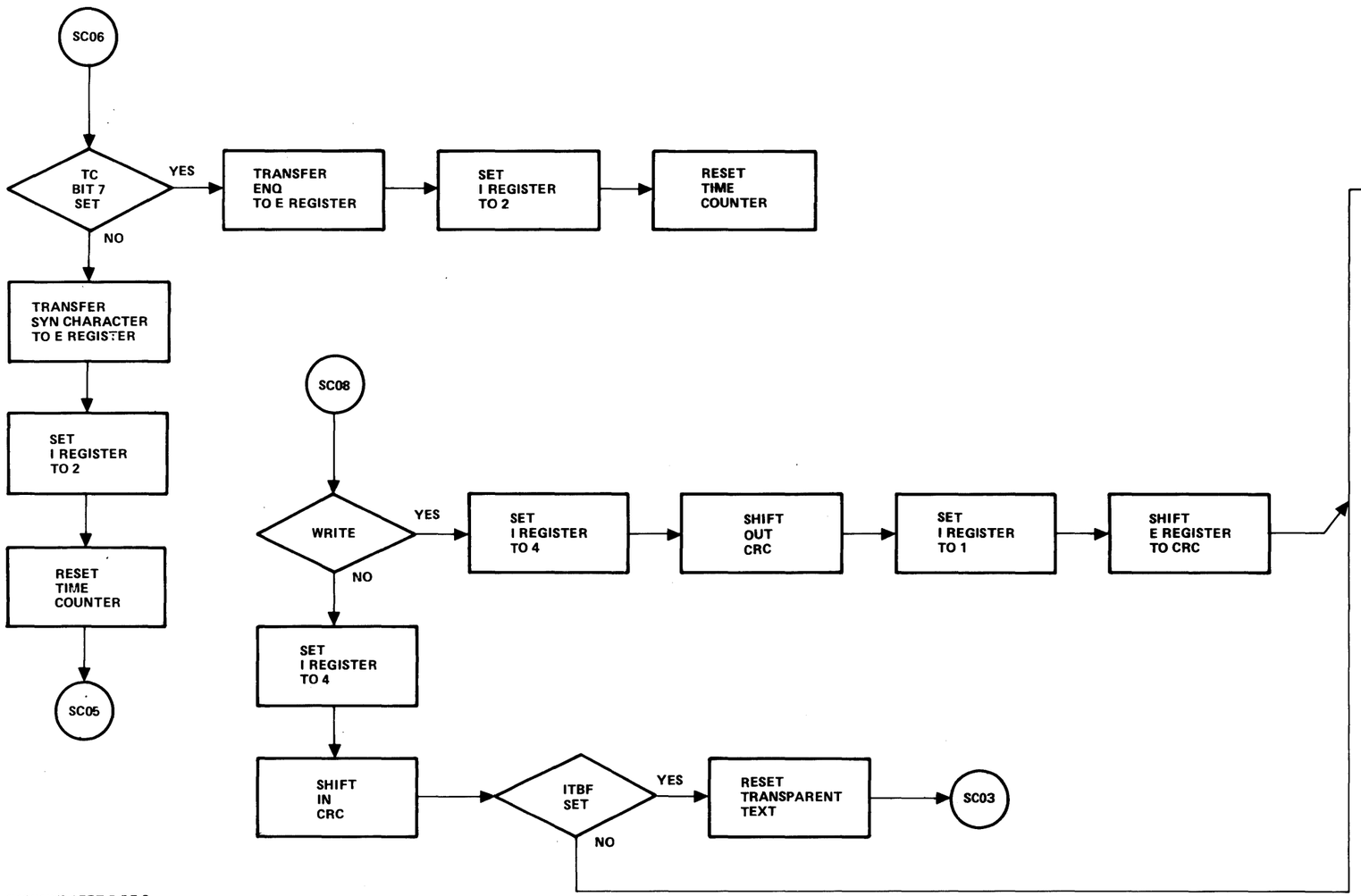


Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 6 of 8)



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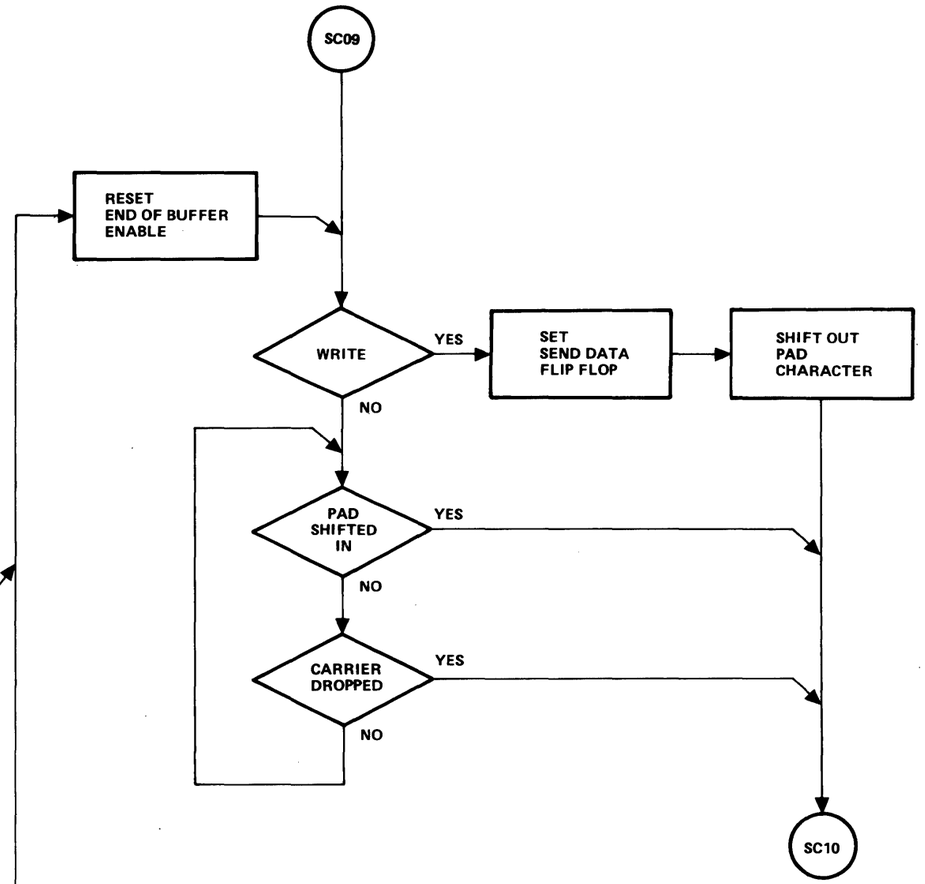
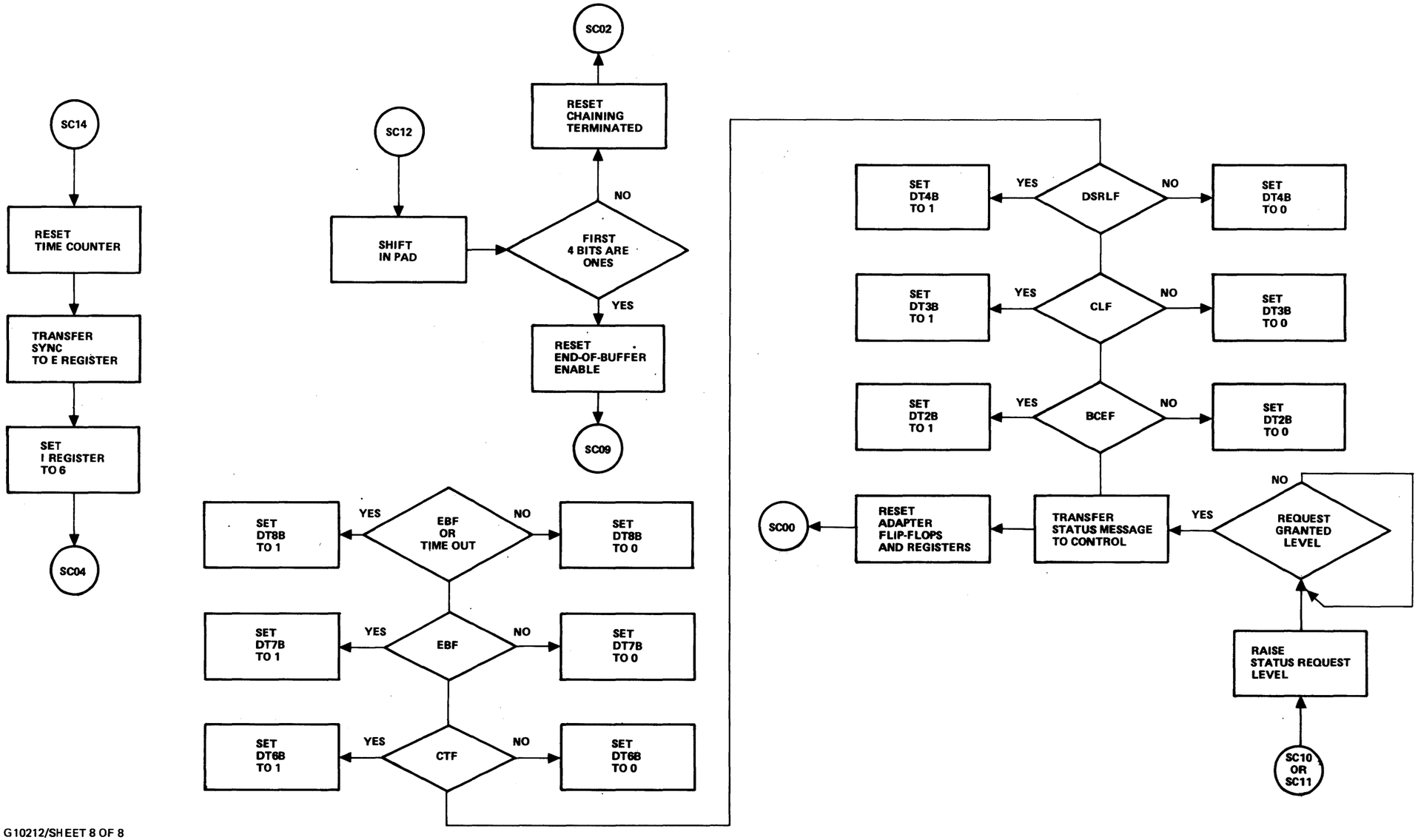


Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 7 of 8)



G10212/SHEET 8 OF 8

Figure 12-4. Detailed Flow Chart, BISYNC Adapter (Sheet 8 of 8)

SECTION 13
BURROUGHS DIRECT INTERFACE LINE ADAPTER

INTRODUCTION

The Burroughs Direct Interface (STD/BDI) line adapter provides a direct connection between a single-line or multi-line control and up to 20 data communication devices. The adapter can be strapped for the following data rates (bps): 150, 300, 1200, 1800, 2400, 4800, 9600, 19200. It operates in half-duplex, bit-serial, asynchronous mode through a shielded twisted-pair transmission line. At data rates of up to 9600 bps, maximum transmission line length is 15,000 feet (4573 meters); at 19,200 bps, line length is limited to 11,000 feet (3350 meters). The adapter provides data character synchronization, generation and checking of both vertical and horizontal parity, and identification of USASCII-7 control characters.

UNIT IDENTIFICATION

The STD/BDI adapter is contained on one logic card, identified by the 8-digit Burroughs Manufacturing and Engineering (M&E) 2212 2071. This number is imprinted on the metalized unit identification label supplied as part of the Field Test and Reference (FT&R) documentation. When the adapter is installed in the system, the identification label is affixed on the end of the 28-position card housing that contains the adapter.

CONTROL CODE SENSITIVITY

Control code sensitivity for the STD/BDI adapter is listed in table 13-1.

A start code is used to begin accumulation of a BCC with the next character. After the receipt of a start code, only an ending code can terminate the I/O operation. A response code terminates the I/O operation only if the response code is not preceded by a start code.

During Write, an ending code terminates the operation if the ending code is preceded by a start code. During Read, an ending code always terminates the operation, but a BCC error is reported if the ending code is not preceded by a start code.

A variant enables EOT to be ignored as a response code for Read or Write. During a Read, this variant allows the control and the associated system to act as terminal and receive a polling sequence from other systems. Hardware recognition of addresses is not provided. During a Write, this variant allows the control to ignore an EOT in order to transmit polling and other sequences that use EOT as the first code in a message for line-clearing.

Table 13-1. BDI Line Adapter Control Code Sensitivity

Function	Code
Sync	SYN (Non Character)
Start	SOH, STX
Ending	ETX, ETB
Positive Response	ACK, ENQ, BEL
Negative Response	NAK, EOT, Time-out
	Optional

I/O OPERATORS

The 24-bit I/O operators are displayed and explained below. The leftmost bit is bit 0 (MSB); the rightmost bit is bit 23 (LSB). Bit positions with "-" are unused and should be reset (0). UUUU signifies adapter number; 0000-1111 (0-15) for 16 possible adapters.

Read

The Read operator accepts data from the remote device and stores it in ascending memory locations beginning with the location specified by the A address and ending with the location specified by the B address minus one. (Receipt of an ending code before the B-minus-1th location is reached terminates data.)

0000 T0D- -EVV P--- ---- UUUU

T = 0: No translation.
= 1: Translate ASCII or EBCDIC.
D = 0: Do not disable timer.
= 1: Disable timer.
E = 0: Ignore EOT as a response code.
= 1: Recognize EOT as a response code.
VV=00: Normal linking.
=01: Link on negative response only.
=10: Link on positive response only.
=11: Undefined.
P = 0: Do not poll.
= 1: Poll.

Write

The Write operation causes data to be transmitted to the remote device. Data is obtained from ascending memory locations beginning with the location specified by the A Address and ending with the location specified by the B address minus one. Receipt of an ending code can terminate data transmission before the B address minus one is reached. Write is generally terminated by the transmission of an ending control code (normally CR).

If a Break is received from the remote unit, the adapter terminates the in-process operation and reports receipt of the Break in the result descriptor for the terminated operation.

0100 T000 0E00 PLLL L--- UUUU

T = 0: No translation.
= 1: Translate EBCDIC to ASCII.
E = 0: Do not ignore EOT as a response code.
= 1: Ignore EOT as a response code.
P = 0: Do not poll.
= 1: Poll.
LLLL 0010-1101: Length of poll sequence (SLC only).

Break (Disconnect)

The Break operator terminates the in-process operation, if any, and transmits a Break signal to the remote terminal. A Break signal is a sustained transmission of spacing for either 32 bits (transmit) or 15 bits (receive). The result descriptor for a Break operation is returned after the adapter has failed to receive data for 600 msec for transmit and for a time period equivalent to 11 bits for receive.

1100 00V- ---- ---- ---- UUUU

V = 0: Send Break, do not disconnect.
= 1: Disconnect, do not send Break. (Switched line adapters only; other adapters send Break.) The result descriptor reports loss of Data Set Ready.

Test

The Test operator is a request for the reporting (in the result descriptor) of the adapter's identification.

100V --M- ---- ---- ---- UUUU

VM=00: Complete operation normally; do not change DTR signal status.
=01: Make DTR signal true, then complete the operation.
=10: Wait until a ringing condition is true before completing the operation. (Switched line adapters only; other adapters complete immediately.
=11: Make DTR signal true, then wait until DSR signal is true before completing the operation. (Switched line adapters only, other adapters complete normally.)

RESULT DESCRIPTOR

The 24 bits of the result descriptor for the BISYNC line adapter are listed below, together with their meanings when set. Omitted bits in the sequence 0-23 are reserved (not used).

Bit	Meaning
0	Operation complete.
1	Exception conditions (Except for the Test operator, this bit is set if any of bits 2-15 are set.)
3	Vertical character parity error or BCC error (Read).
4	Memory access error (Read).
5	Memory parity error (Write).
6	Time-out (Read or Write).
7	Break received (Write).
8	Ending control code expected but not received (Read or Write).
9	Linking terminated (Read; VV = 01 or 10).
11	Loss or absence of Data Set Ready (Read, Write, Break).
12	Loss of Clear To Send (Write) or loss of carrier (Read).
16	Operation complete.
17	Data communication device (Test).
18-23	000000 = Adapter not present 000010 = STD/BDI adapter

FUNCTIONAL DESCRIPTION

Block Diagram

Figure 13-1 is a functional block diagram of the BDI line adapter.

The adapter accepts initiation information from the control and generates status messages to be transmitted to the control. Data to or from a remote terminal passes through the data register, scratchpad memory, control interface, and terminal interface.

On an Write operation, data enters the adapter from the control and is loaded in parallel to the data register (D-Reg). Following processing of this data, it is shifted from the data register one bit at a time (at a rate determined by an adjustable, internal rate timer) to the terminal interface. The reverse of this sequence takes place during a Read operation.

Sequence Counter

Adapter functions are primarily controlled by an internal sequence counter. This sequence counter (SCxx), which functions independently of the sequence counter in the control, provides a count of 00 through 63. (Counts 40 through 63 have no specifically assigned functions.)

Figure 13-2, at the end of this section, is a detailed diagram of the sequence count flow, which is described in the subsections that follow.

SC00

Initiation state. The adapter waits for Adapter Control Level (ACL) from the control initiate operation. Initiation of an operation causes the adapter to exit from SC00 to one of the following sequence counts:

SC01: Break operation.
SC02: Read/Test operations.
SC30: Write operation.

A general Clear signal during any sequence count causes the adapter to return to SC00.

SC01

A delay state for the adapter during a Break operation. The adapter waits in SC01 for one clock period and then exits to SC02.

SC02

A delay state for the adapter during either a Read operation, Test operation or Break operation. The adapter waits in SC02 for one clock period and then exits to SC03.

SC03

A delay state for the adapter from SC02. After one clock period, the adapter exits to SC04.

SC04

Read initialization state. The adapter starts timing for a start bit on the line. The exit from SC04 is to SC05.

SC05

Intracharacter serial shift state. The adapter is restarted from SC11 for a Read operation or started for a Write operation. The exit from SC05 is to SC06.

SC06

Timer initialization state. The adapter's counter is enabled so that, depending on the operation, timing considerations can be detected. The timing considerations and their associated exits from SC06 are as follows:

BREAK
The D Register is held clear until a full count (FC) is accumulated. Exit is to SC07.

Read, Write
If a first character has been detected (FCDF) or a character other than a negative control (NCCF) has not been detected and a full counter exists, the adapter times out and exits to SC37. Otherwise, if the time-out is dependent on a negative control character, a full counter and failure to detect a first character causes an exit to SC32. Normal exit from SC06 (without time-out) is to SC07.

SC07

Store time-count state. The time count previously accumulated in SC06 is stored into scratchpad for later use by the adapter. The exit from SC07 is at SC08.

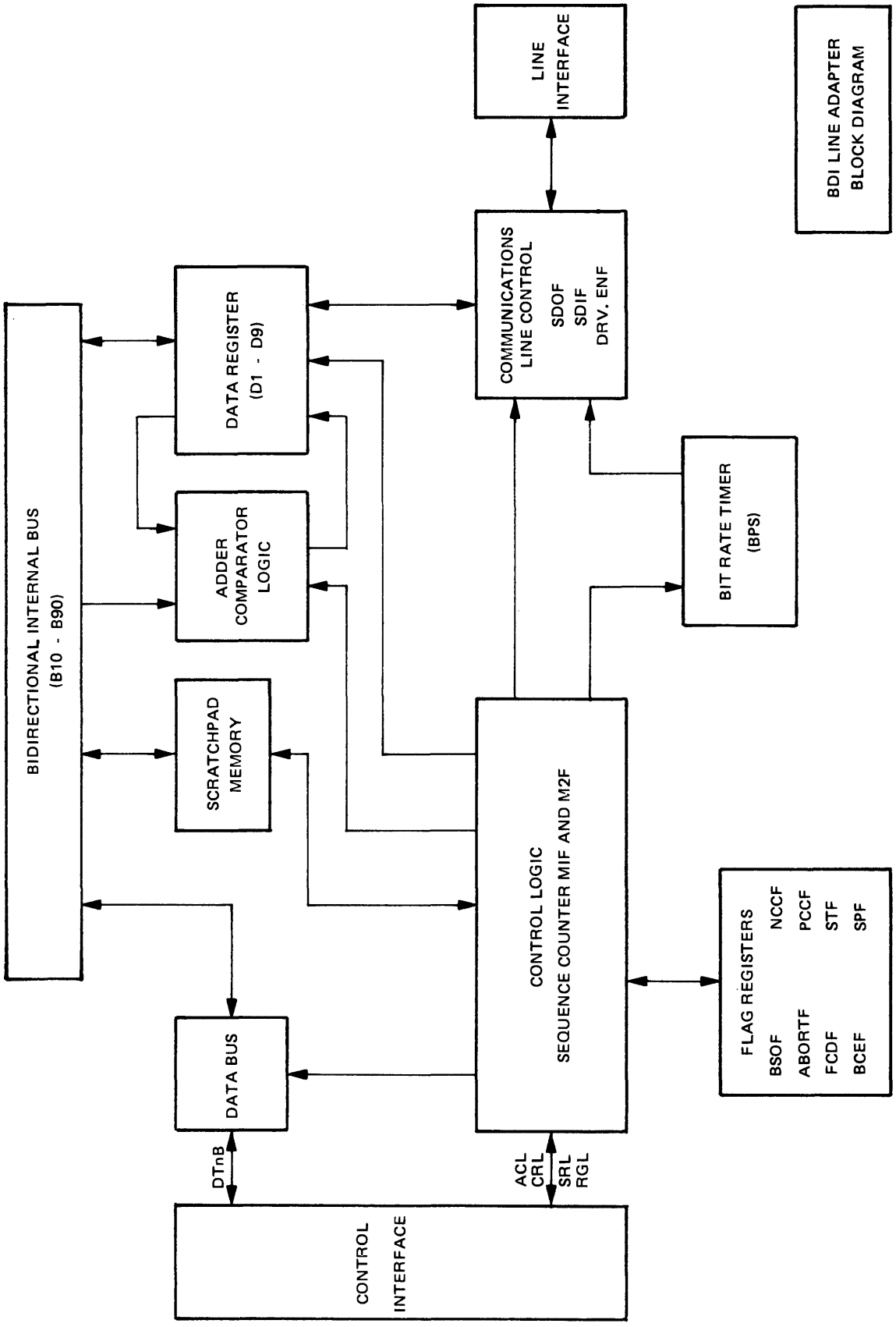


Figure 13-1. Block Diagram, STD/BDI Line Adapter

SC08

Load Start/Stop-bits state. During a Write operation, when the End of Character Service flag (EOCSF) is detected, the data is loaded from scratchpad and the start/stop bits are added. If a Break operation is in progress, the stop bit is not loaded because the line needs to keep spacing and a stop bit is a MARK. The exit from SC08 is to SC09.

SC09

The start bit is shifted out onto the line for a Write operation, or data is shifted in from the line for a Read operation. The exit from SC09 is to SC10.

SC10

In SC10, the adapter stores received data into the scratchpad. The exit from SC10 is to SC11.

SC11

In SC11, the direction of shift of the data is determined. Data is shifted in on Read and shifted out on Write. Exit is to SC12 if character shifted in or out is complete or to SC05 if the character shifted in or out is incomplete or if the operation is Break.

SC12

Complement read-data state. If a Read operation is in progress, the D Register is complemented and the rate timer is restarted for start bit detection. Exit is to SC13 on Read or to SC32 on Write.

SC13

In SC13, receive data is saved in scratchpad while a BCC comparison is being made (Read). The BCC character is loaded into the D Register (Write). The exit from SC13 is to SC14.

SC14

Parity generation is initiated. The exit from SC14 is to SC15.

SC15

Parity is either generated or checked as data is shifted in or out by the adapter. Bits 8 and 9 are set to zero and the D Register and Bus are compared. When they are equal, the exit from SC15 is to SC16.

SC16

The parity bit (B8) is loaded into scratchpad and the result of a parity check is loaded into the status scratchpad. If an error is detected, bit 2 of SPM3 is set. The exit from SC16 is to SC17.

SC17

The character (stored during SC13) is reloaded into the D Register and End-of-Character-Service (EOCSF) is set so that serial transmission of a start bit can begin. The exit from SC17 is to SC18.

SC18

The Block Check Character (BCC) is compiled during Read or Write operations. If a Read operation is in progress, a start flag (STF) must be set prior to the detection of a stop flag (SPF). If a Write operation is in progress, an abort flag will complement the D Register. Exits from SC18 are as follows:

SC05: Write operation and detection of both STF and SPF.

SC18: Read or Write and no STF or SPF.

SC33: Read and detection of SPF with no detection of SPF.

SC19

The BCC is stored in scratchpad when a start flag (STF) is detected. The exit from SC19 is to SC20.

SC20

Data is reloaded into the D-Register for character identification during a Read operation. The exit from SC20 is to SC21.

SC21

STX (start-of-text) is identified. The start flag (STF) is set if a STX is detected. The exit from SC21 is to SC22.

SC22

NAK (negative acknowledgement) is identified. The Negative Control Character flag (NCCF) is set if a NAK is detected. The exit from SC22 is via SC23.

SC23

ACK (positive acknowledgement) is identified. The Positive Control Character Flag (PCCF) is set if an ACK is detected. The exit from SC23 is to SC24.

SC24

Start of Heading (SOH) is identified. STF is set if a SOH is detected. The exit from SC24 is to SC25.

SC25

Enquiry (ENQ) is identified. The Positive Control Character Flag (PCCF) is set if an ENQ is detected. The exit from SC25 is to SC26.

SC26

BEL (bell), a control character used to signal contention, is identified. The Positive Control Character Flag (PCCF) is set if a BEL is detected. The exit from SC26 is to SC27.

SC27

End of Transmission (EOT) is identified. The Negative Control Character flag (NCCF) is set if an EOT is detected. The exit from SC27 is to SC28.

SC28

End of Text (ETX) is identified. The Positive Control Character Flag (PCCF) and the Stop Flag (SPF) are set when an ETX is detected. The exit from SC28 is to SC29.

SC29

End of Transmission Block (ETB) is identified. The Positive Control Character Flag (PCCF) and the Stop Flag (SPF) are set when an ETB is detected. The exits from SC29 are as follows:

SC04: Break
SC05: Write
SC30: Read

SC30

The initial delay for a Write operation is performed. The Write delay is dependent upon the strapping options:

fast turnaround – strap for 2 bit times or for 3 msec.

slow turnaround – strap for 15 or 63 msec.

The exit from SC30 is to SC31.

SC31

SC31 is the parallel character transfer state. Data is transferred to the control during a Read operation and transferred from the control during a Write operation. The exits from SC31 are to SC14 on a Write with Request Granted Level (RGL) true or to SC32 on a Read with RGL true.

SC32

SC32 is the major decision state of the adapter. The type of operation and the control character is compared with the linking variants to determine which logic branch to take in order to service the data. Exits are to the following sequence counts:

SC04: A Read operation and no control character and B Address not reached. (WRA/·CCD/·BARF/)

SC04: Read operation, control character, Stop flag, no BCC option. (CCD·SPF·BCCN/·BSOF/)

SC13: Write operation, control character, Stop flag, no BCC option. (CCD·SPF·BCCN/·BSOF/)

SC31: Write operation, no control character, B-Address not reached. (CCD/·BARF/)

SC35: Write operation, BCC shift, link positive, no Positive-Control-Character flag. (WRA·BSOF·LPVF·PCCF/)

Write operation, BCC shift, link negative, no Negative Control Character Flag. (WRA·BSOF·LNVF·NCOF/).

Read operation, control character, no Stop flag (or a Stop flag and no BCC option), link positive, no Positive Control Character Flag. [CCD·(SPF/+BCCN)·(LPUF·PCCF/]

Read operation, control character, no Stop flag (or a Stop flag and no BCC option), link negative, no Negative Control Character Flag. [CCD·(SPF/+BCCN)·LNVF·NCCF/)]

SC36: B Address reached, no control character. (CCD/·BARF)

SC38: Write operation, BCC shift, link positive, Positive Control Character Flag. (WRA·BSOF·LPVF·PCCF)

Write operation, BCC shift, link negative, Negative Control Character Flag. (WRA·BSOF·LNVF·NCCF)

Write operation, BCC shift, no link positive, no link negative. (WRA·BSOF·LPVF/·LNVF/)

Read operation, control character, no Stop flag (or Stop flag, no BCC option),link positive, Positive Control Character Flag. [CDD·(SPF/+BCCN)·LPVF·PCCF]

Read operation, control character, no Stop flag (or Stop flag, no BCC option), link negative, Negative Control Character Flag. [CCD·(SPF/+BCCN)·LNVF·NCCF]

Read operation, control character, no Stop flag (or Stop flag, no BCC option), no link positive, no link negative. [CCD(SPF/+BCCN)·LPVF/·LNVF/]

SC33

Error conditions are checked. Both the BCC received and the Stop flag without receipt of a Start flag during Read operations are detected. The exit from SC33 is to SC34.

SC34

Error conditions are loaded into the status scratchpad. The exits from SC34 are dependent on the linking variants and are as follows:

SC35: Link positive, no Positive Control Character Flag. (LPVF·PCCF/)

Link negative, no Negative Control Character Flag. (LNVF·NCCF/)

SC38: Link positive, Positive Control Character Flag. (LPVF·PCCF)

Link negative, Negative Control Character Flag. (LNVF·NCCF)

SC35

The avoid-linking bit in the status scratchpad is set whenever the control character and the linking variant are not matched. The exit from SC35 is to SC38.

SC36

The control-character-not-found bit in the status scratchpad is set whenever B Address is reached without detection of a control character. The exit from SC38 is to SC38.

SC37

The Read time-out detected in SC06 or a Break detected during a Write is set in the status scratchpad. The exit from SC37 is to SC38.

SC38

The adapter waits for a shift pulse during a Write operation or exits in 1 clock for a Read operation so that a minimum delay is experienced prior to ending an operation. The exit from SC38 is to SC39.

SC39

SC39 is the status transfer state. The adapter raises a Status Request (SRL) and waits for a Request Granted (RGL) from the control prior to transferring the status of an operation to the control. The exit from SC39 is to SC40, from SC40 through SC63, and from SC63 to SC00 (idle). is to SC38.

SC37

The Read time-out detected in SC06 or a Break detected during a Write is set in the status scratchpad. The exit from SC37 is to SC38.

SC38

The adapter waits for a shift pulse during a Write operation or exits in 1 clock for a Read operation so that a minimum delay is experienced prior to ending an operation. The exit from SC38 is to SC39.

SC39

SC39 is the status transfer state. The adapter raises a Status Request (SRL) and waits for a Request Granted (RGL) from the control prior to transferring the status of an operation to the control. The exit from SC39 is to SC40, from SC40 through SC63, and from SC63 to SC00 (idle).

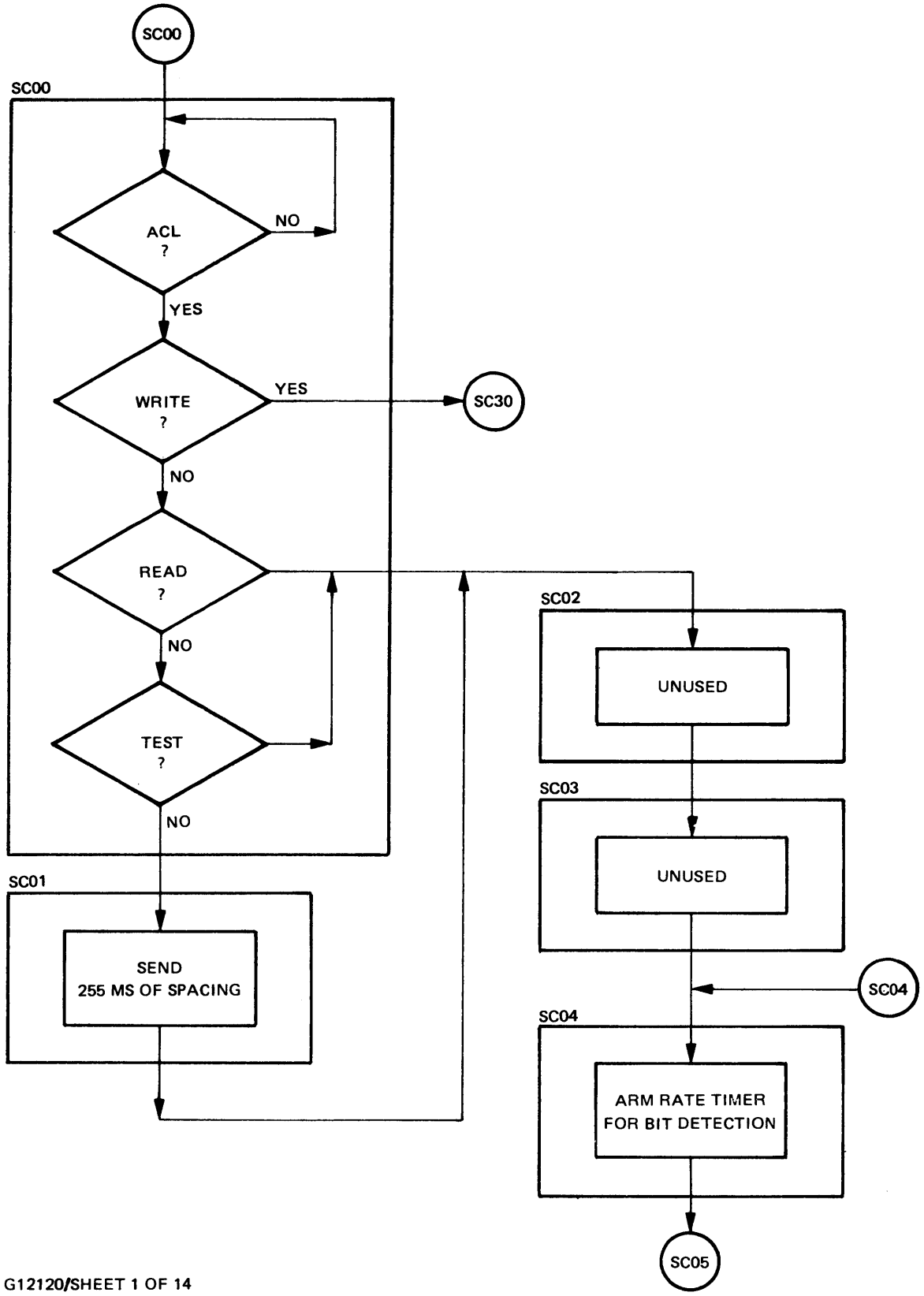


Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 1 of 14)

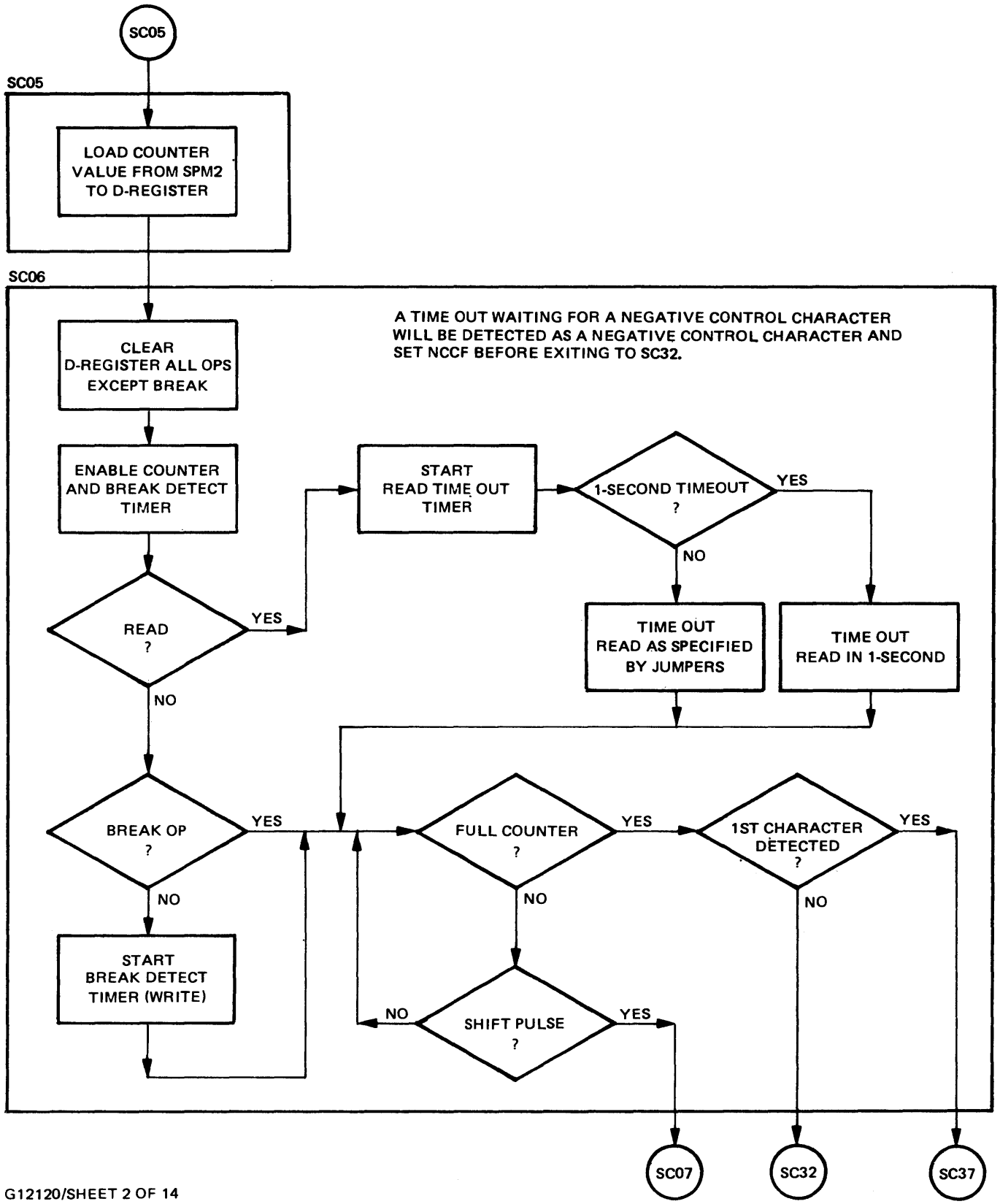


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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 2 of 14)

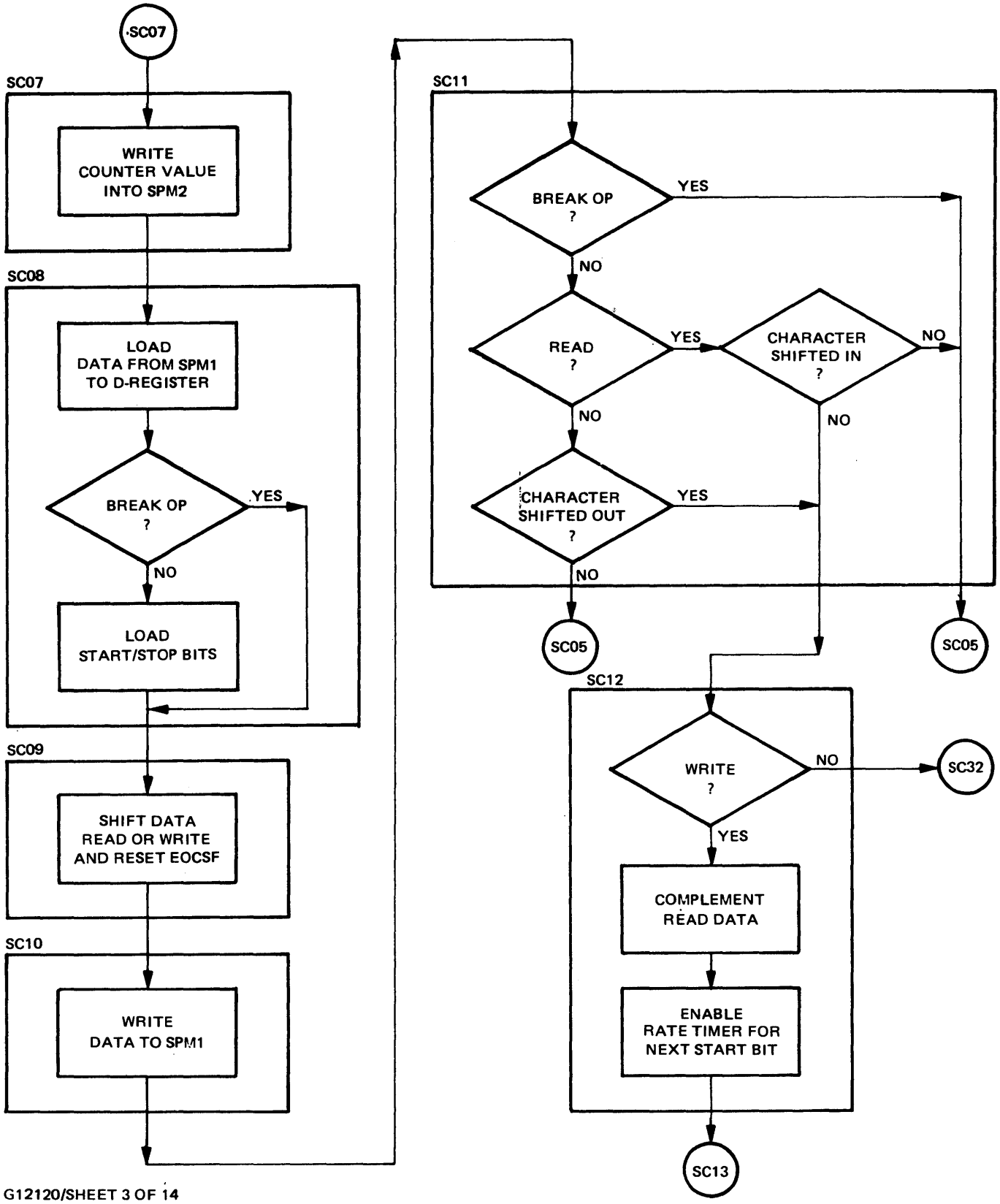

Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 3 of 14)

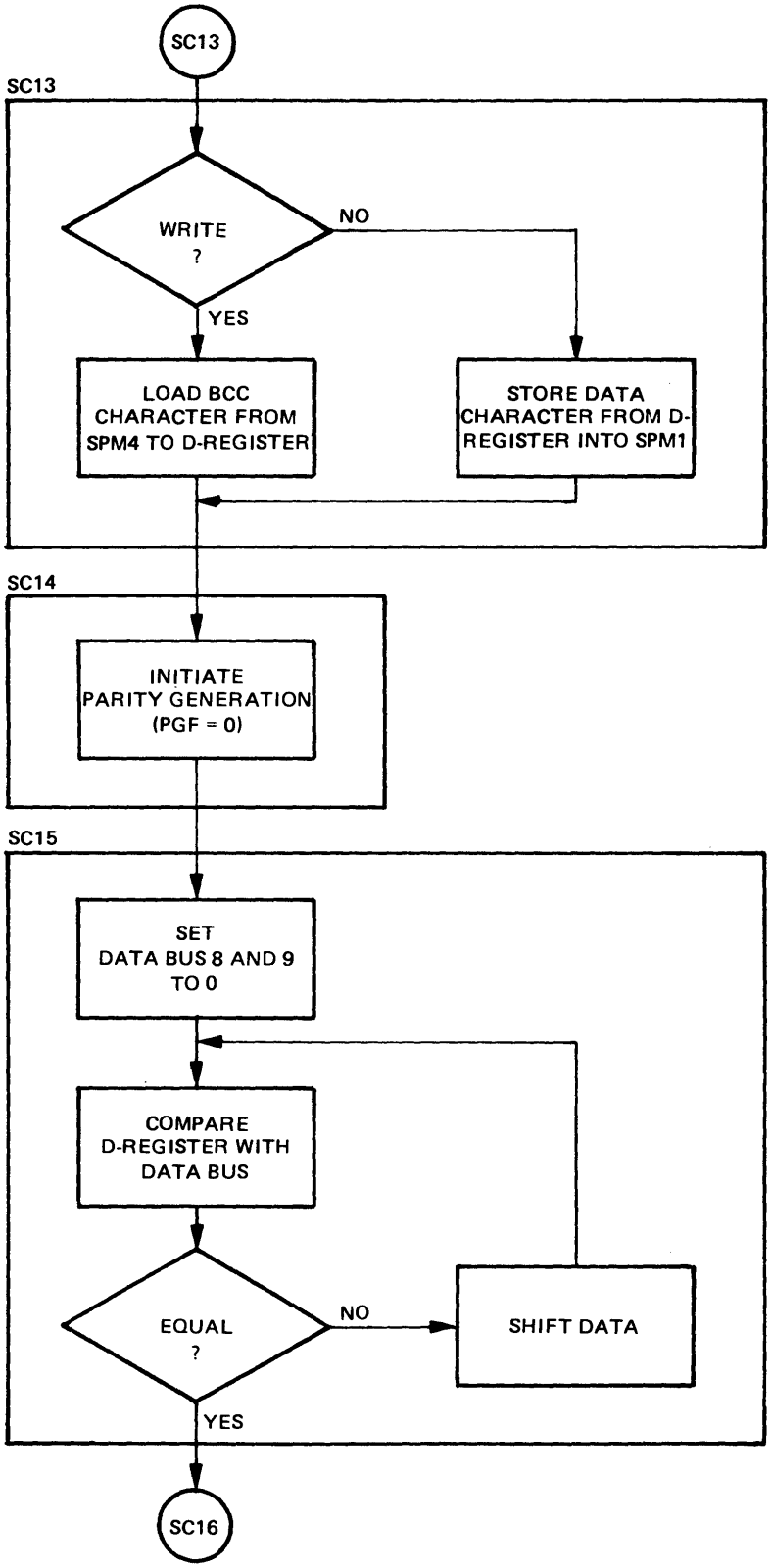

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 4 of 14)

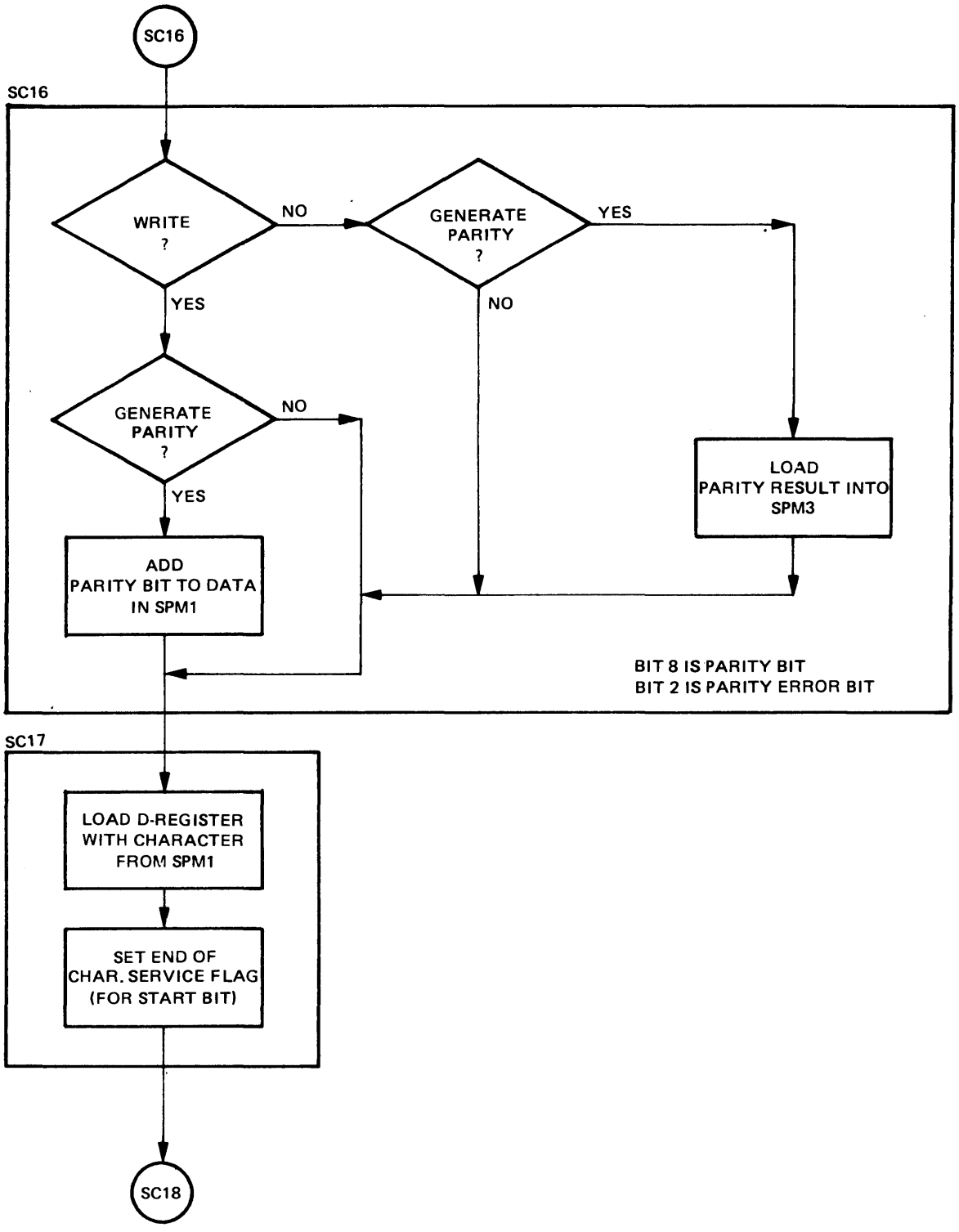

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 5 of 14)

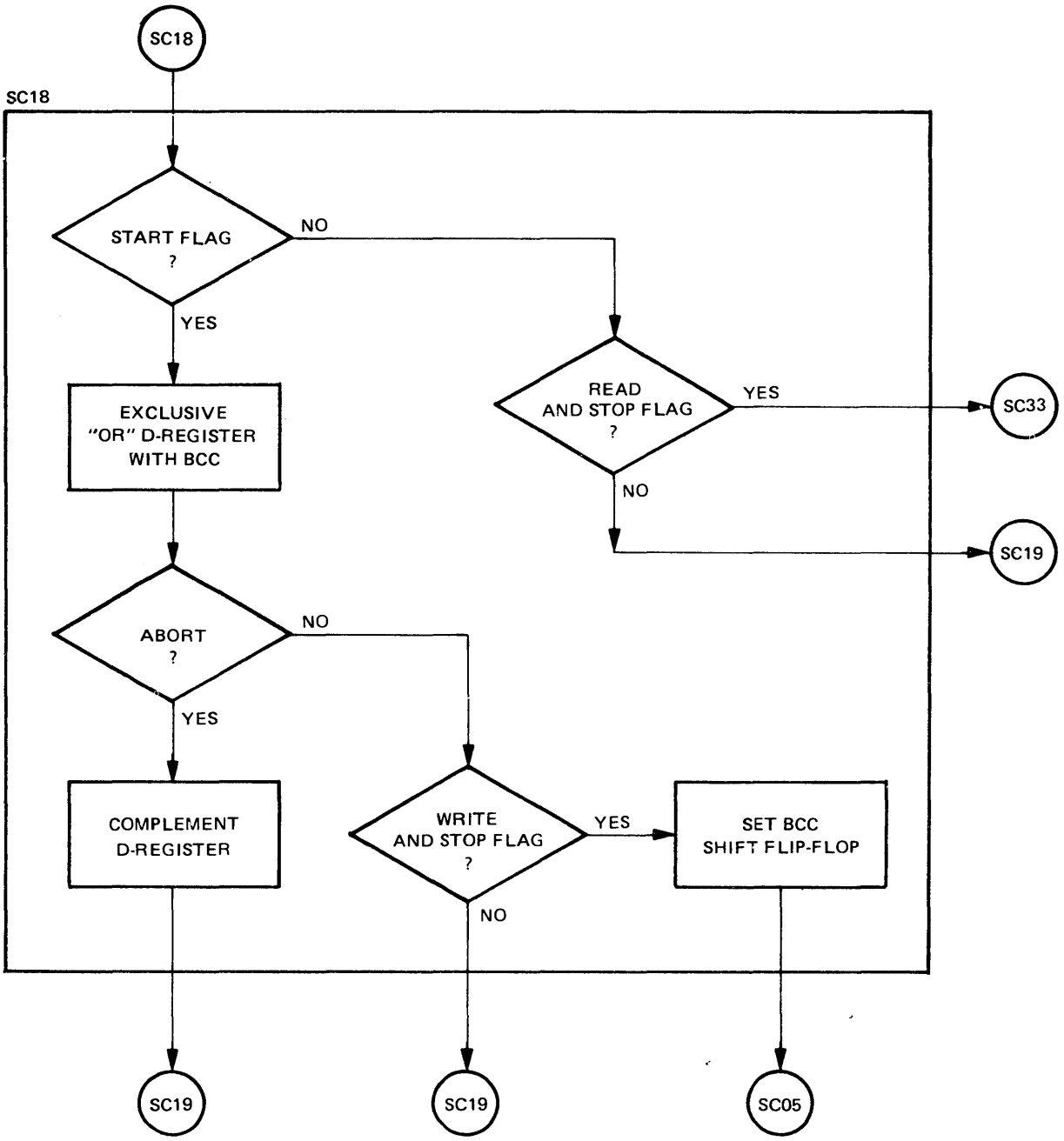

Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 6 of 14)

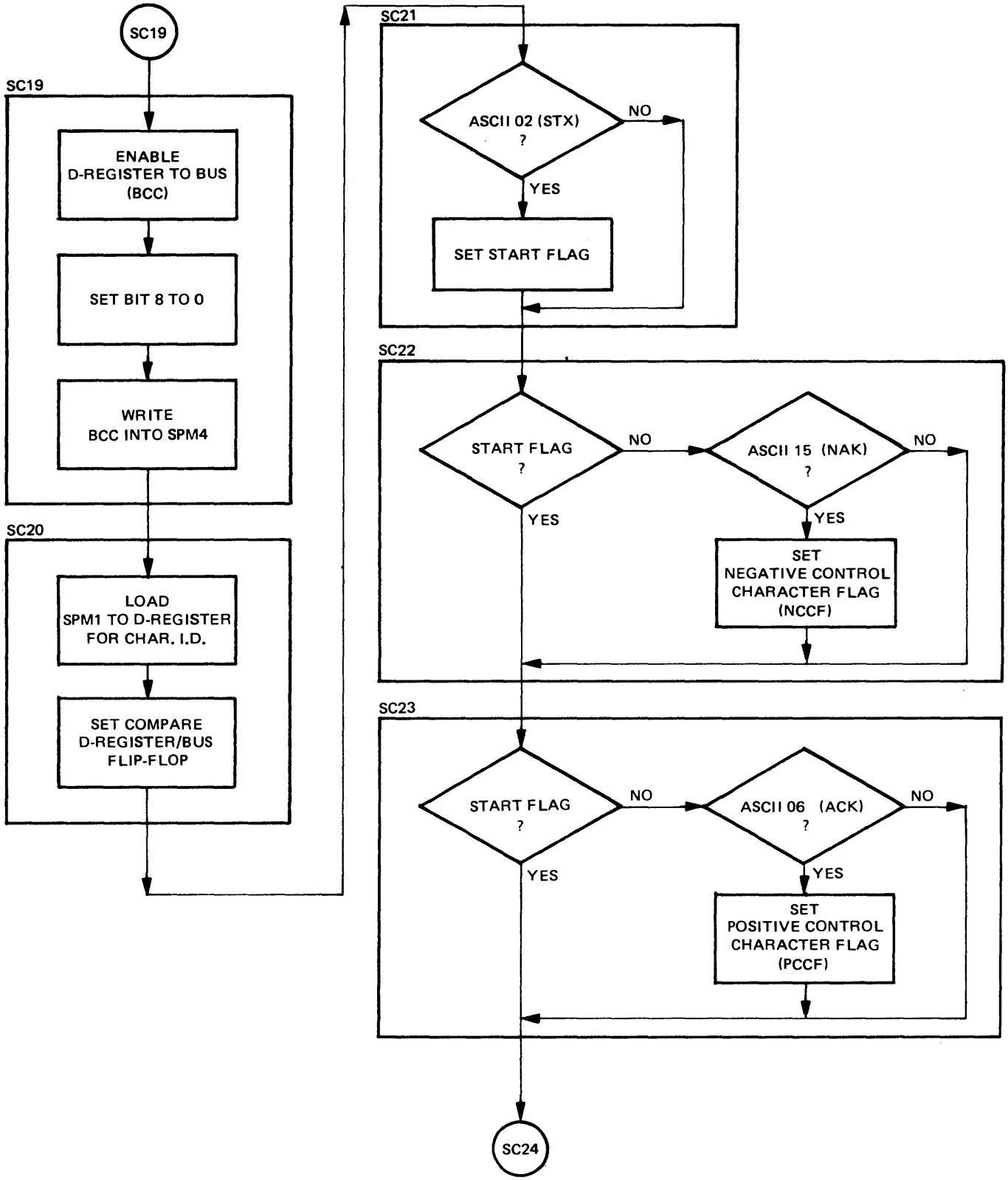

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 7 of 14)

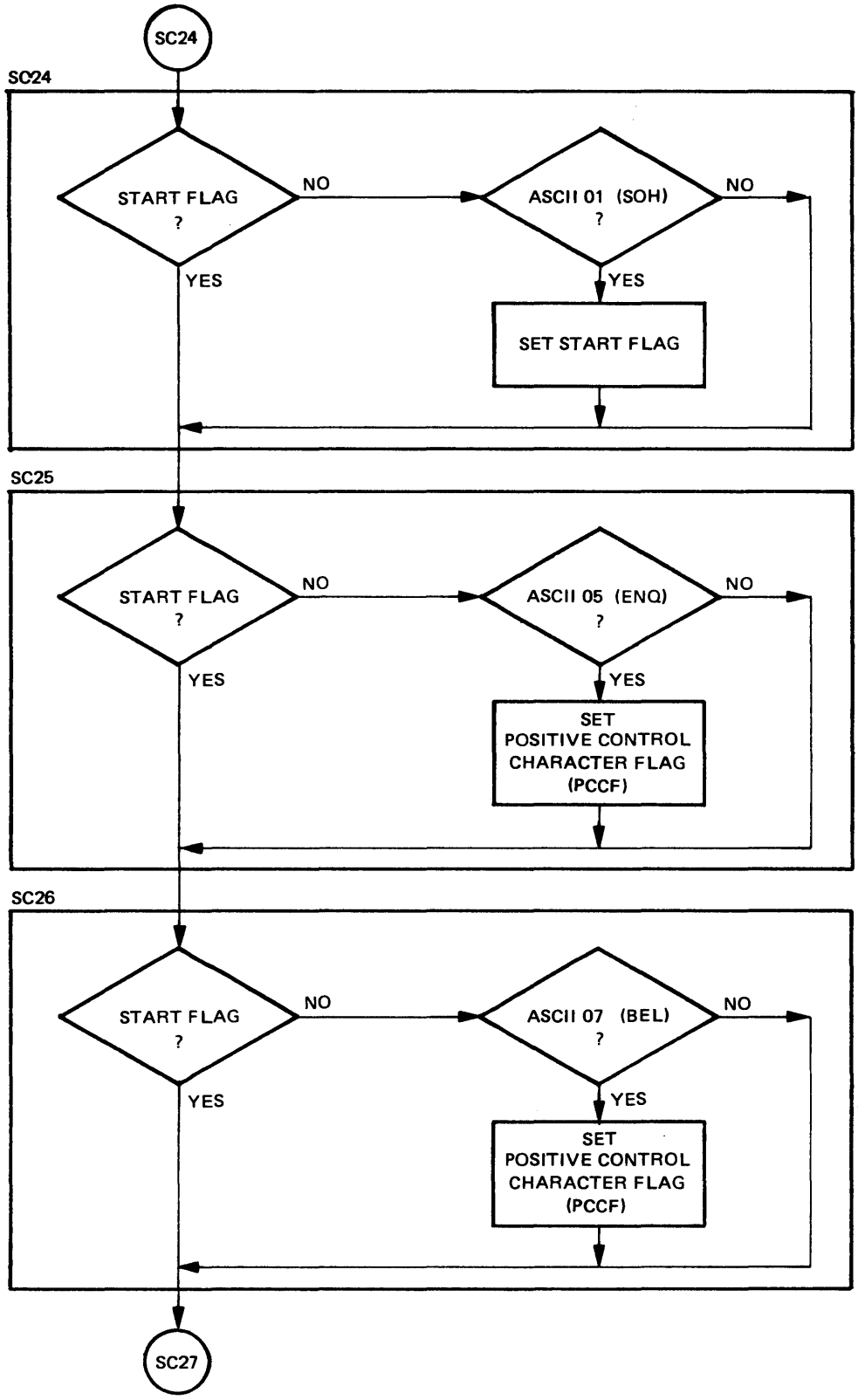

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 8 of 14)

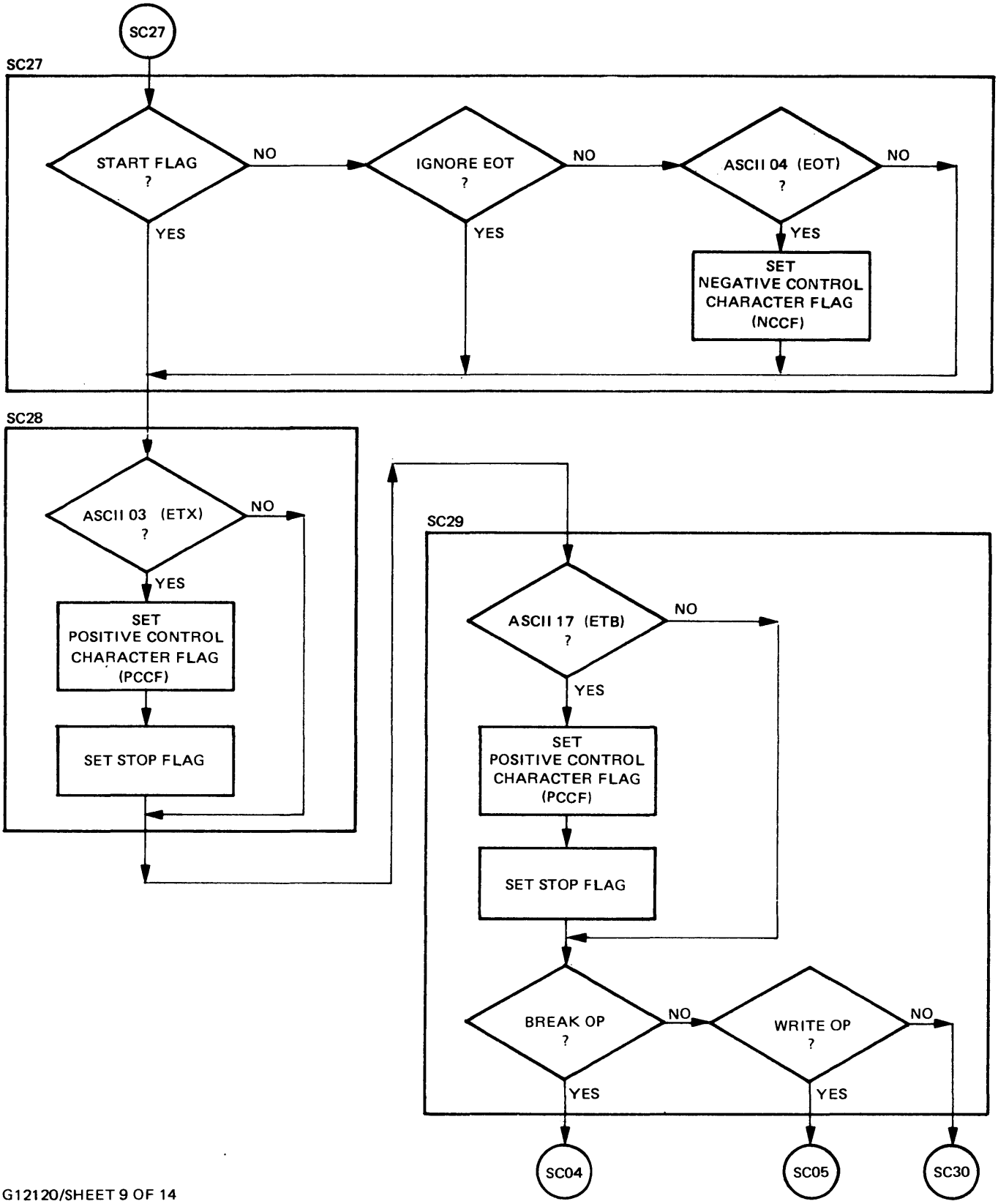

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 9 of 14)

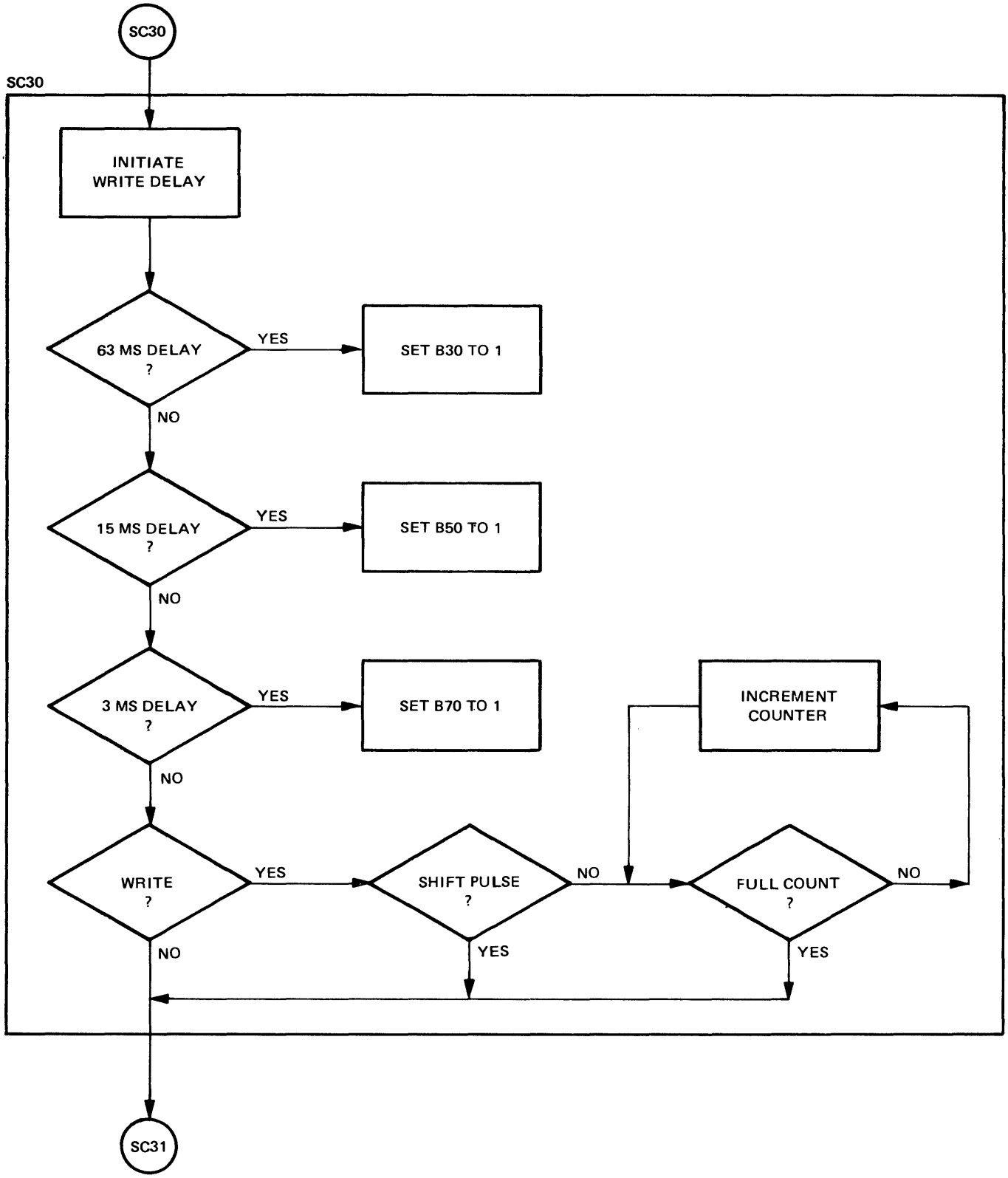

Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 10 of 14)

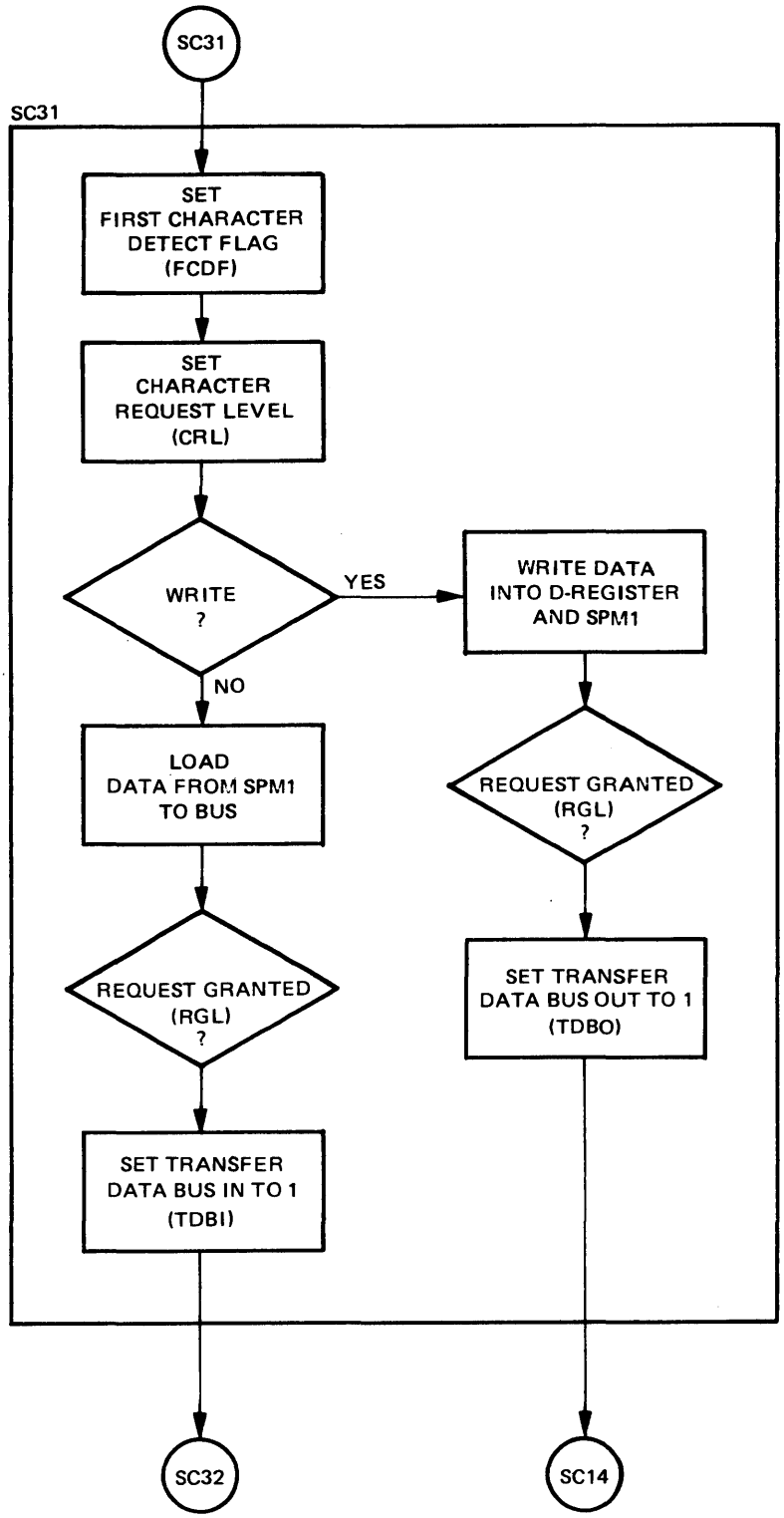

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 11 of 14)

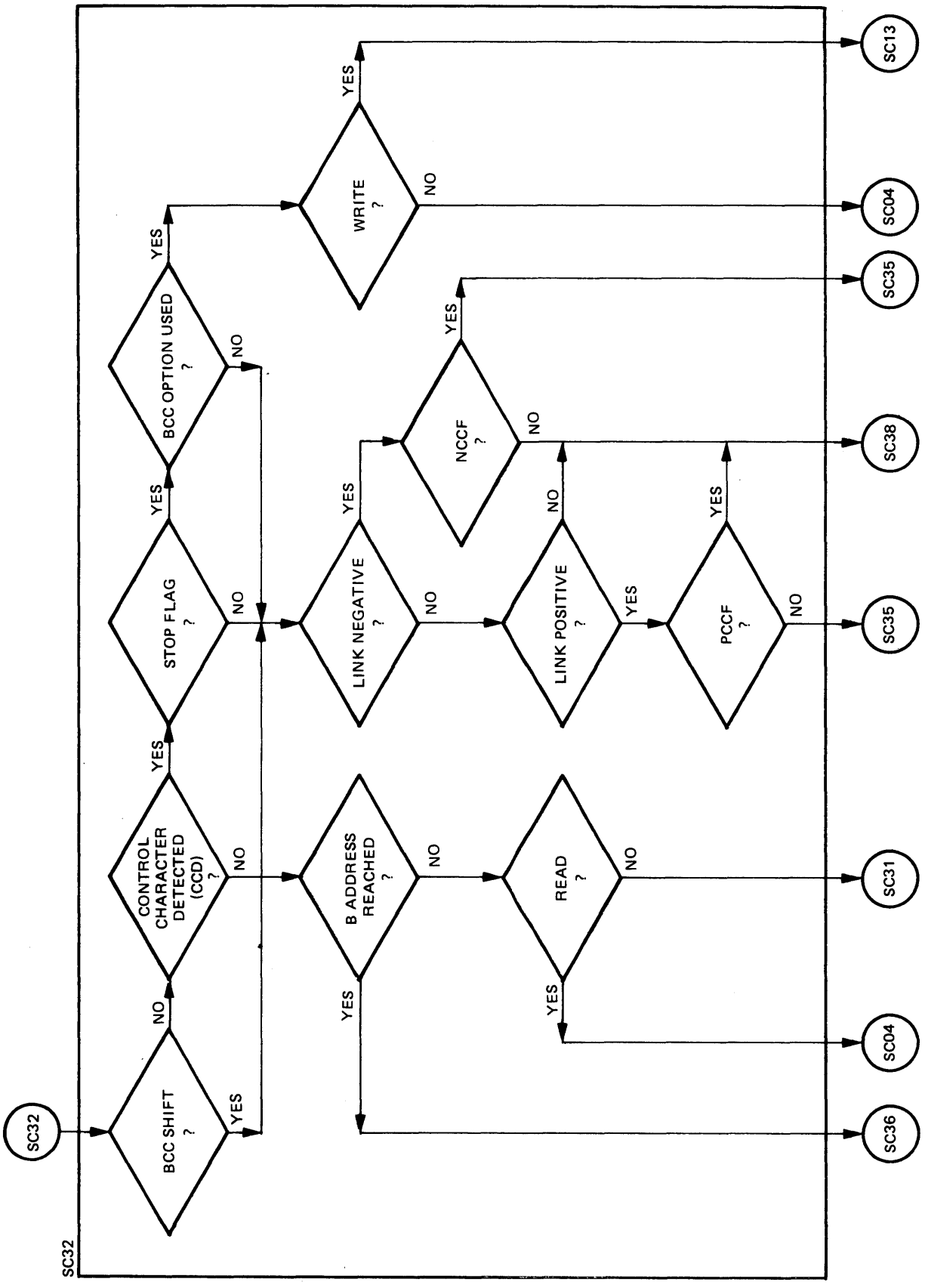

Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 12 of 14)

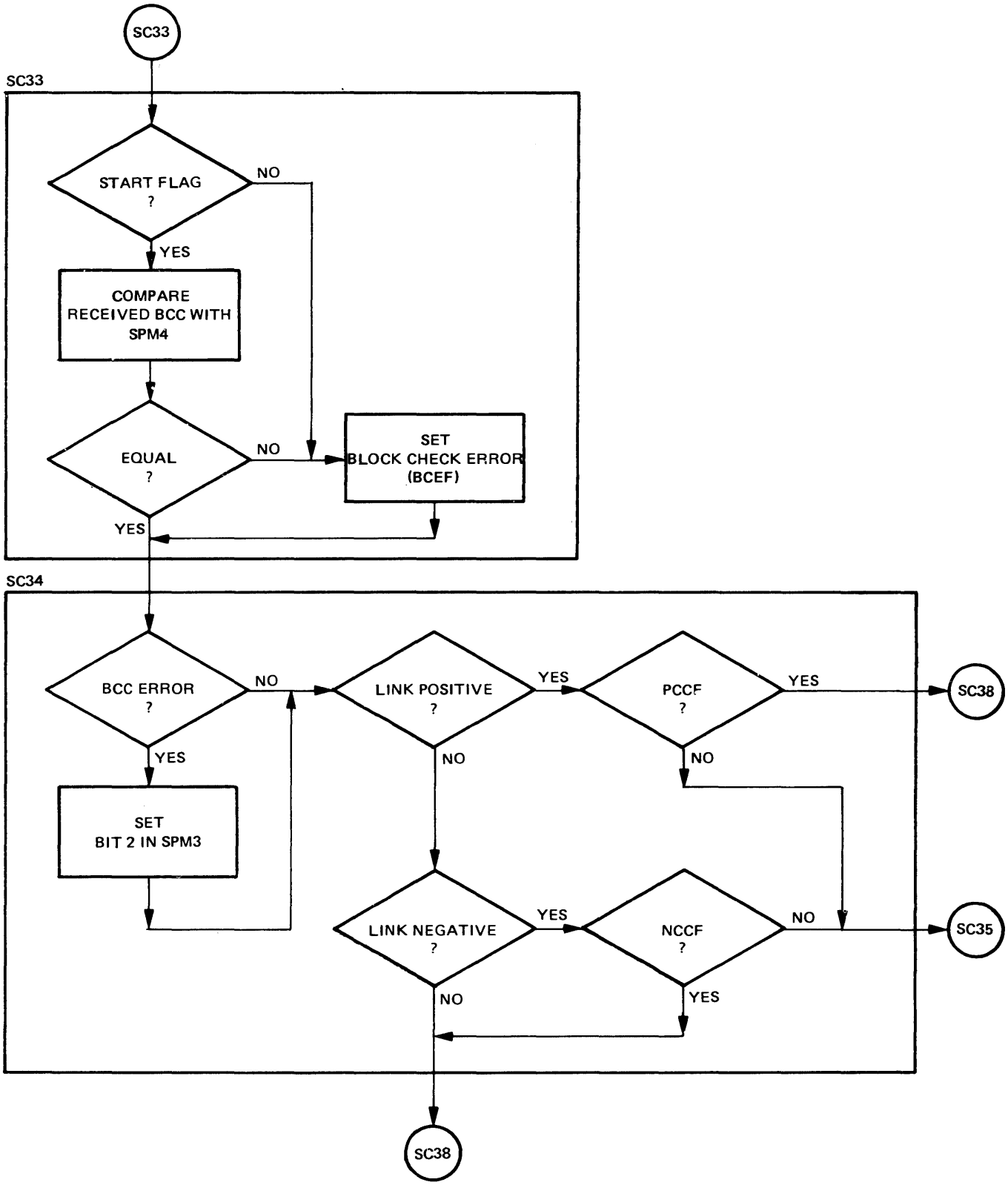

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 13 of 14)

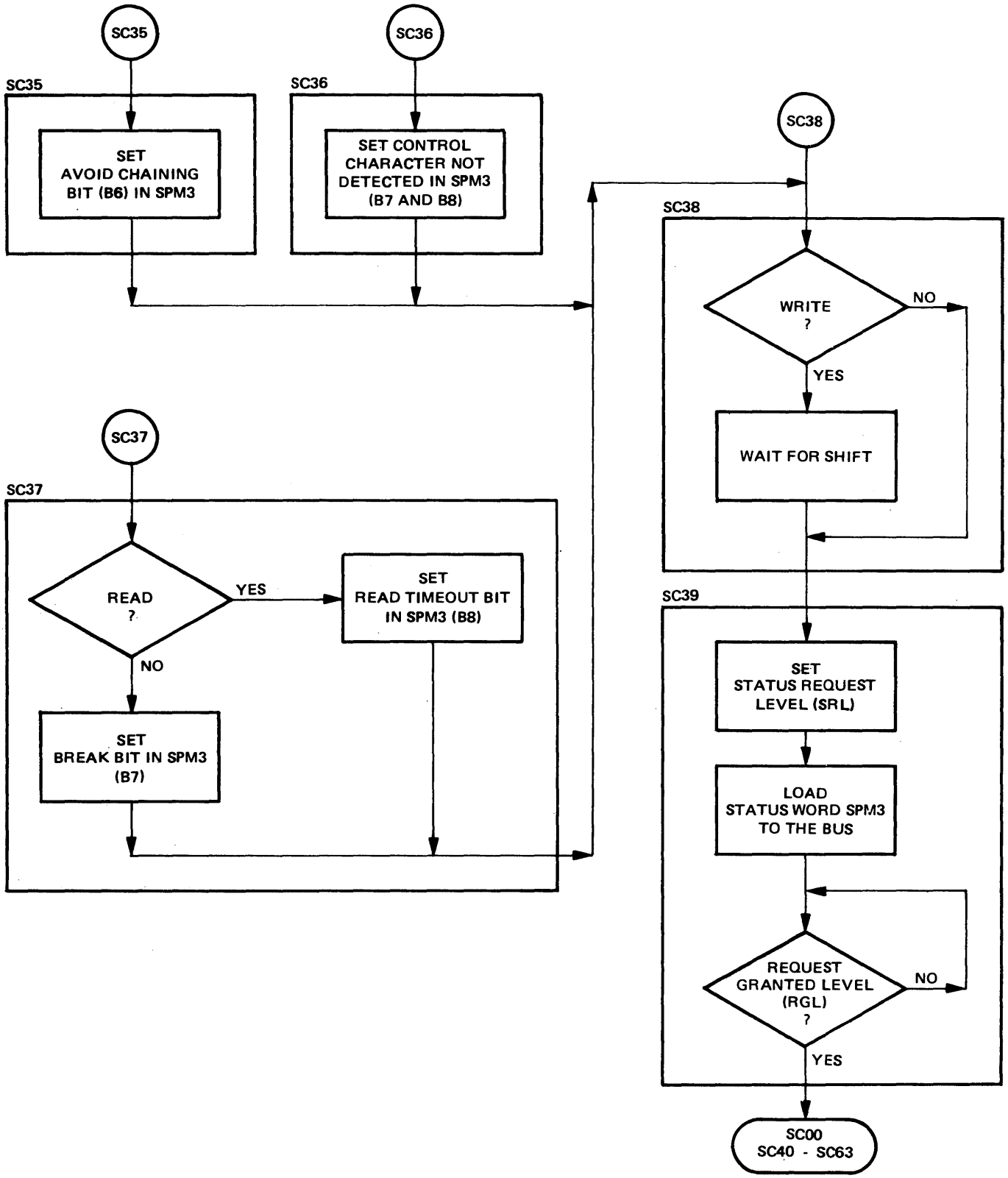

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Figure 13-2. Detailed Flow Chart; STD/BDI Adapter (Sheet 14 of 14)