BURROUGHS CORPORATION
MILITARY FIELD SERVICE DIVISION
TECHNICAL TRAINING DEPARTMENT
June 12, 1959

INFORMATION SHEET

FERRITE CORE DEVICES

SUBCOURSE: Fundamentals

OBJECTIVES: To show the relationship of single and multiaperture core devices to computer design functions.

REFERENCES:

(1) Bimag Circuits for Digital Data-Processing Systems, by W. Michle, John Pavine and J. Wyler - Burroughs Research Center and David Loew - Weizman Institute.

(2) The Transfluxor, J. A. Rajchman and A. W. Lo, Proceedings of the IRE, March 1956, pp 321 - 332.

(3) Multihole Ferrite Core Configurations and Applications, H. W. Abbott, and J. J. Suran, Proceedings of the IRE August 1957, pp 1081 - 1093.

(4) End Fined Memory uses Ferrite Plates, by V. L. New House, N. R. Kernfield and M. N. Faufman, Electronics; October 10, 1958.

WRITTEN BY: John Turner

INTRODUCTION

The single aperture core has been utilized in various diversified programs but our discussion will be restricted to the basic physics and application of the core in computer and Data Processing systems. A comparison of the single aperture cores will be developed. The theory presented should be absorbed to allow for its later application to more complex core analogies. The tape wound and Ferrite core will be used as the basic vehicle of presentation.

PERMANENT AND ELECTRO-MAGNETS

A review of the classical physics of magnetism will allow a more detailed understanding of the tape wound and Ferrite cores. Since magnetism is the ability of metals to attract other metals, it was found that magnetic lines of induction exists in the magnets immediate area. The magnetic lines of induction are the flux lines, also one flux line is a maxwell. Figure 1 shows that the number of lines of flux passing thru one square centimeter is a measurement of the flux density in this area.

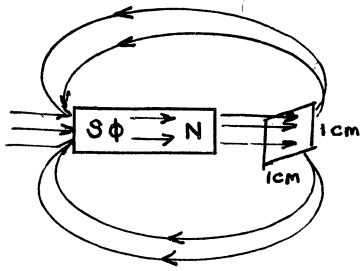


Figure 1.

The symbol Φ is used for flux and the unit is the Maxwell; the symbol B is used for flux density and the unit is maxwells per square centimeters (gauss):

(1) $$B = \frac{\Phi}{CM^2} = \frac{\Phi}{A}$$

The permanent magnet in Figure 1 allows for the presentation of many anologies. Two related magnets, Figure 2, show that there must be attraction or repulsion between two magnets (Like poles repel - unlike poles attract).

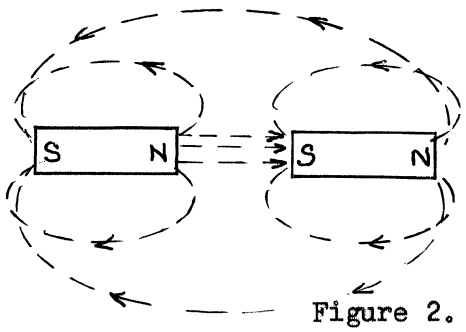


Figure 2.

The force in dynes has been expressed by the following equation:

(2) $$F = \frac{M_1 \cdot M_2}{d^2}$$

Where M_1, M_2 unit magnetic strength in unit poles; d = distance between poles in centimeter.

The law states that the force in dynes is equivalent to the product of the unit pole strengths and the reciprocal of distance separating the poles (squared). When the force is viewed over a length of one centimeter, we are looking at the flux intensity, H, in oersteds:

(3) $$H = \frac{F}{l}$$

F = force in dynes,
l = length in CM, and
H = intensity (flux) in oersteds

ELECTROMAGNETISM

The field of electricity and magnetism were combined when a magnetic field was discovered to exist about a current carrying conductor. The intensity is a function of the current and distance from the conductor. (H)

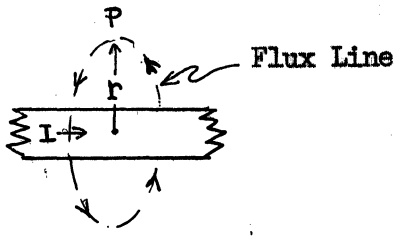


Figure 3.

at point (P) is found to be a product of twice the current and the reciprocal of ten times the radius.

(4) $H = \frac{2I}{10r}$ Where I is in amps and r is the distance in centimeters.

The intensity about the circumscribed point (P) is found by the equation:

(5) $H = \frac{2\pi I}{10r}$

It is further seen that the flux intensity is a function of the current which is causing it and that the above equations are simplifications of complex mathematical derivations. When a grouping of the conductor occurs, it is found that a solenoid exists if the length is 10 times greater than the radius.

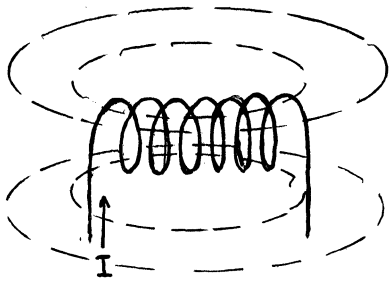


Figure 4.

The intensity at the center of the solenoid (all flux linkages) is given by the equation following which includes the number of looped conductors that are adding to the field.

(6) $H = \frac{4\pi N I}{10 l}$; where (N) is the number of turns, (I) is the current in amperes, and (l) is the length in centimeters. Since principles of magnetism in this paragraph are relative to electromagnetic theory in contrast to permanent magnet theory, the insertion of iron in the center of the solenoid tends to increase the amount of flux linkage by allowing an easier medium of flux travel. However, the ease of flux flow is the permeability of a substance and air has an easiness of magnitization constant of one. We find that there must be a method of classifications of materials in use. Permeability is the reciprocal of reluctance or

(7) Mu (permeability) = $\frac{1}{\text{reluctance}}$ and the symbol is μ .

Materials are classified accordingly as

(8) (Mu) $\mu \geq$ 1, paramagnetic material;

(Mu) $\mu <$ 1, diamagnetic material; and

(Mu) $\mu >>$ 1, ferromagnetic materials.

Note: (See Chart 1)

Then reluctance of air equals one equals the permeability of air. The reluctance is a function of the length of the flux paths and the area while the ease of flux flow is a constant (μ);

(9) $R = \frac{l}{\mu A}$

The Ohms' Law of magnetism is that the Force in Gilberts is equal to the product of reluctance and flux.

(10) $mmf = \phi \text{ Rel}$,

or $\phi = \frac{mmf}{\text{Rel}}$,

or $\text{Rel} = \frac{mmf}{\phi}$.

To reduce a lengthy review it will suffice to state that $H = f\left(\frac{\text{Force}}{l}\right)$ or that the intensity is a function of the gilbert and centimeter. By plotting a simple graph of the following figure it is possible to define the many forms of permeability.

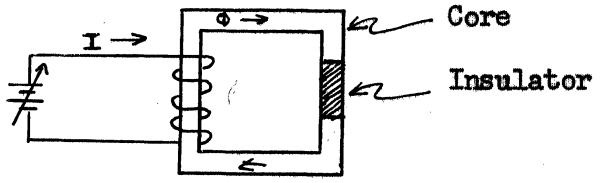


Figure 5.

Mu equals the quotient of density and intensity, $\mu = B/H$.

Figure 6 displays various values of permeability as well as the hysteresis characteristics of this metallic core. Hysteresis, to lag behind, is a graphical plot showing the various degrees of the magnetization lagging behind the magnetizing intensity. It is clearly seen that the ratio of Flux Density to its corresponding Flux Intensity is constantly varying and is constant only upon that particular point of inspection.

GRAPHICAL ANALYSIS OF THE HYSTERESIS LOOP

Assuming no past magnetic history of the material, it is seen that an increasing intensity in a positive direction will increase the flux density in an arbitrary north pole direction. As the intensity is reduced to zero, the magnetization remains at some point above zero (remanence point). When the magnetizing intensity is reversed, a certain amount of intensity is required to reduce the magnetization to zero (point B) and this intensity is known as the coercive force, usually a loss of signal induction. A further increase in the same direction will bring the material to a maximum south pole magnetization (-Bm). Once the intensity is brought back to zero the magnetization will remain at -Br or +Br, depending upon the direction of the applied intensity +Hm or -Hm. Permeability being defined as the ratio of magnetization (B) to magnetizing intensity (H) allows the following definitions to be established.

Mu initial

The slope of the line (1) projected and then calculated with its origin at zero.

Mu maximum

If the vertical axis is rotated to become tangent with the rising magnetization curve (3), the slope of the tangent line will be the value of the maximum permeability of the material. Most manufacturers will specify this value for magnetic calculations.

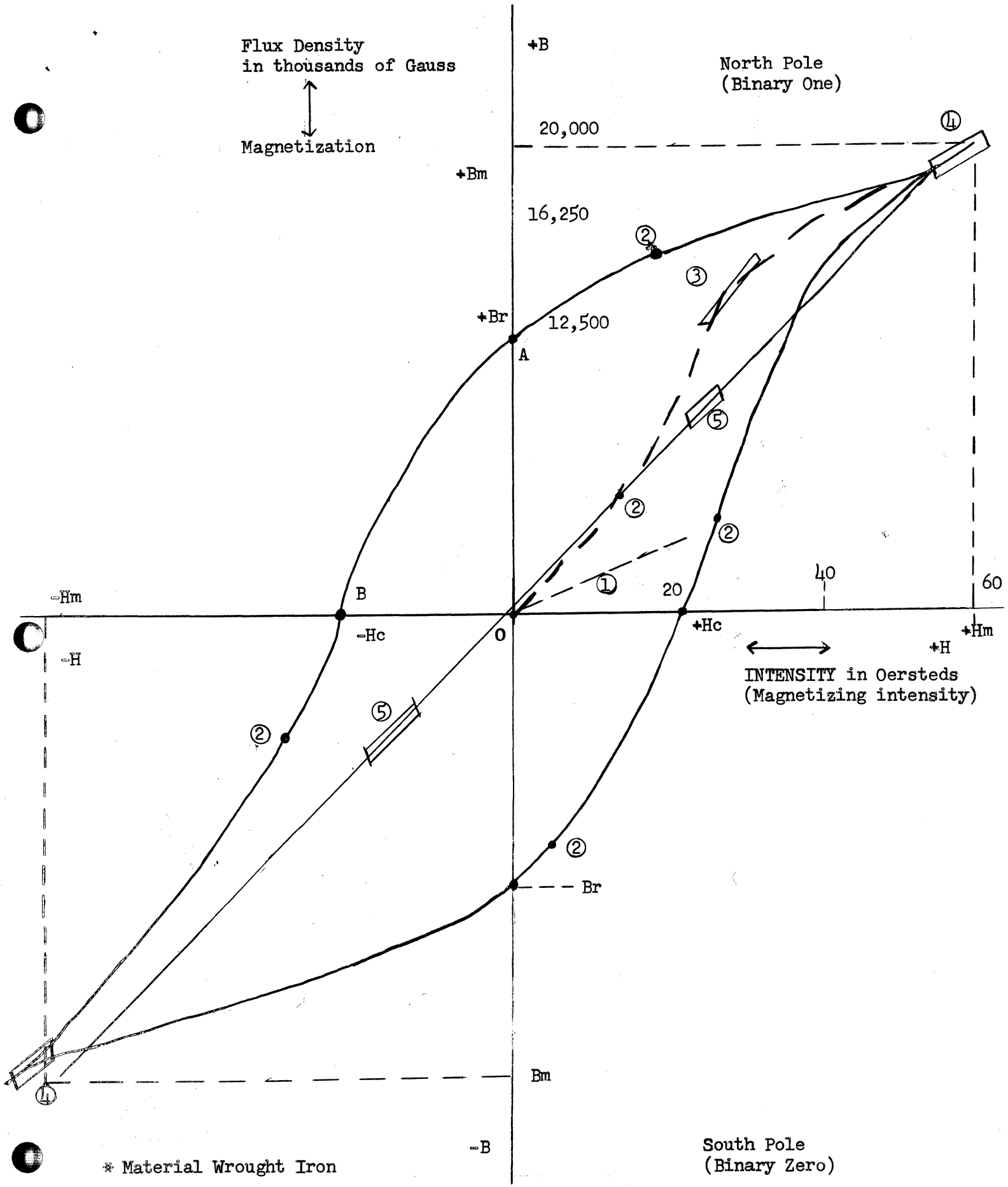


Figure 6 - Typical Hysteresis Loop

Mu differential

The differential permeability is the permeability of the material at any point along the curve (2) . This value is usually expressed as

(11) $\text{Mu } d = \frac{d B}{d H}$,

and is the most concise form of permeability calculation, although very seldom utilized because of the required complex mathematical manipulations.

Mu at saturation

Actually Mu saturation is the Mu of air (4) and corresponds to a direct variation of

(12) B to H or $\text{Mu}_S = \frac{B}{H} = 1$,

and saturation always occurs when the slope of B/H is equal to 1.

Mu incremental

The value of any lines slope calculated between given limits and expressed as

(13) $\text{Mu} = \frac{\Delta B}{\Delta H}$ is incremental mu.

Mu Average

The line drawn from positive saturation to negative saturation through zero (5) will represent the average Mu. Since the area above zero is equivalent to the below zero area the slope of the line is constant and

(14) $\text{Mu avg} = \frac{\Delta B}{\Delta H}$ along this line (5) .

While plotting the graph it might be significant to indicate that the area of the hysteresis loop represents the power loss of the given material. This power loss occurs because there is no induction taking place from the remanence points to the coercive force points. (Assuming that a secondary winding is attached to the core for induction reaction purposes and the I^2R = power loss.)

When the flux intensity is found to be zero, one of two conditions must exist. These conditions are +Br (North Pole remaining magnetization) or -Br (South Pole remaining magnetization). These conditions will exist once the material has been exposed to a magnetic field and since this corresponds to two stable states, it is seen that this metalic core has bimagnetic stable properties. A signal induced force driving the core from +Br to -Bm would cause a ΔB_s change. A signal driving the core from +Br to +Bm would

cause a Bn change. A comparison of the ratio of Br to Bm would indicate the signal to noise (Bs to Bn) ratio in the form of a squareness ratio for the hysteresis loop, expressed as

$$(15) \quad Rs = \frac{/Br/}{/\overline{Bm}./}$$

This (15) is true because as Br approach Bm the difference Bn decreases whereas Bs the difference of +Br to -Bm approaches 2 Bm. Cores used to store information in one of the two stable remenant conditions usually have squareness ratios of .85 or better for significant reasons that will be discussed in a later section.

Cores with air gaps are usually used in the Audio or Power frequency ranges whereas cores with the toroid or closed lap properties are usually associated with pulse applications (hi frequency components). Since pulse like signals are to be stored in digital systems, it will be more important to restrict our discussion to toroid type cores; more over, the advent of core storage devices brough about the need for more detailed theories of operation and applications of these devices. Higher permeabilities are required to approach the ideal data handling conditions, thus we see the introduction of the tape wound and Ferrite cores in toroidal form for storage purposes.

HIGH MU MATERIALS - CHEMICAL COMPOSITION

After many years of studying the atomic structures of various types of metals, the ferromagnetic core was developed. It has been found that materials such as iron (Fe), Nickel (Ni), Manganese (Mn), and other materials have valuable magnetic properties when chemically combined with other substances. Since the discovery of the natural ferrite ($Fe_3 O_4$) lodestone experimentation has proved that any divalent material substituted chemically in this molecular arrangement will display a much greater ease of magnetization characteristics. The Equation for a ferrite ($Ni Fe_2 O_4$) indicates that NiO may be blended with $Fe_2 O_3$ to form a nickel type ferrite, that FeO may be blended with $Fe_2 O_3$ to form iron ferrite, and that $Mn O \cdot Fe_2 O_3$ may be blended chemically with $Fe_2 O_3$ to become a manganese oxide type ferrite. The percentage of mixture and chemical blending is a carefully controlled process of firing the oxides at a pre-determined temperature to produce a material that will be referred to as the ferrite. Ferrites are usually poured in a toroid or closed loop solid core form of various specific dimensions. It is natural to assume that the more carefully blended and formed ferrites require greater care in the manufacturing process, consequently, they cost more as the quality increases.

The alternate method of manufacturing ferromagnetic (permeability much greater than one) cores is to chemically mix various types of metallic substances to form an alloy that is usually cast in thin sheets. These sheets are cut in small strips and then wound on a toroidal ceramic bobbin to become the well known tape wound core. The tape wound core is usually much cheaper to manufacture than the ferrite core.

VOLTAGE CALCULATIONS

Utilizing Figure 7 we see that the two basic forms of the ferrite are the (a) cylindrical and the (b) rectangular toroid. The difference between the two is the shape and means of determining the cross-sectional area of the core. As indicated by (d), the mean length of flux travel is computed in a similar fashion for both cores. Figure 7 shows that the tape wound core area and length of flux travel may be calculated in a similar manner. Notice that the mean length of flux travel in inches is equal to the produce of pi and one half the sum of the inner and outer diameter of the material or

(16) $l = \pi\frac{(D + d)}{2}$ inches; where l is the mean length of flux travel in inches, D is the outer diameter in inches, and d is the inner diameter in inches. The area for a circular toroid is defined as:

(17) $a = \pi r^2$; whereas the rectangular toroid is

(18) $a = S^2$. The radius and sides are usually in inches.

The length computation is due to the fact that flux travels only within the material and takes the form of a solenoid. For the convenience of the reader, the next concept will be presented in a step by step analysis.

VOLTAGE VS PERMEABILITY

(19) Recall that $ED = L\frac{di}{dt} = N\frac{d\phi}{dt}10^{-8}$; where E is induced voltage, i = current in amperes, t is time of change in seconds, and N is the number of turns, Φ = flux in maxwells where one maxwell is equal to 10^{-8} Webers (law: 1 weber cutting one turn in one second = 1 volt) then $ED = E_0$.

(20) $L\frac{di}{dt} = N\frac{d\phi}{dt}10^{-8}$

and

$L = N \cdot \frac{d\Phi}{di} \times 10^{-8}$ but i cause change of Φ and

$\Phi = BA$ or $B = \frac{\Phi}{A}$, and $\mu = \frac{B}{H}$, and $\frac{I}{A} = \mu H$

(21) If $\frac{\Phi}{A} = \mu H$ then $\Phi = \mu HA$ but $H = \frac{4\pi N I}{10l}$ where l is in cm.

(22) Substitution for Phi gives ($\Phi = \mu HA$)

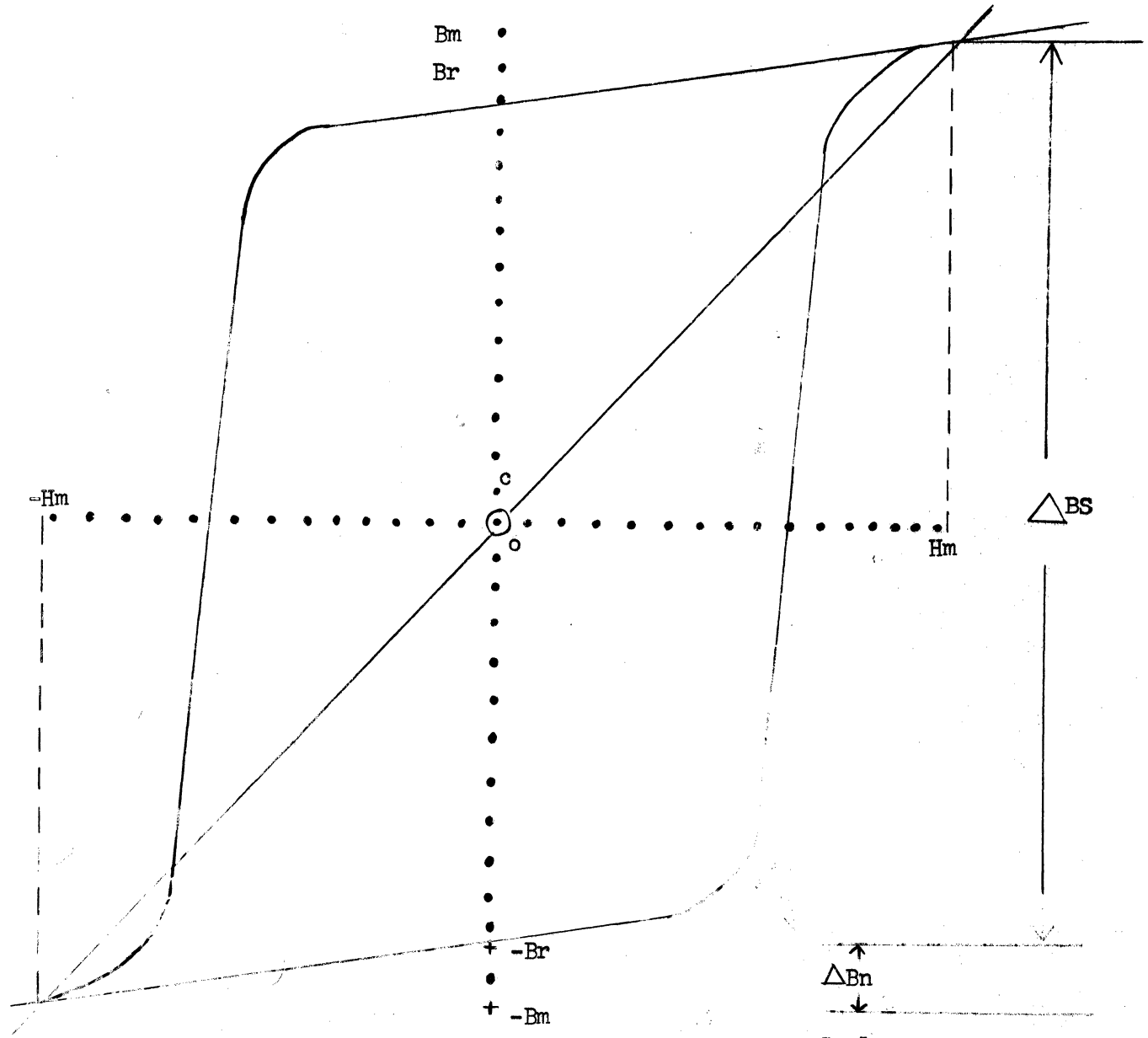
(23) $L = \frac{N\Phi}{I}10^{-8}$, $L = \frac{N}{I}(\mu AH)10^{-8}$,

then $L = \frac{N}{I}\mu A\left(\frac{4\pi NI}{10l}\right)10^{-8}$

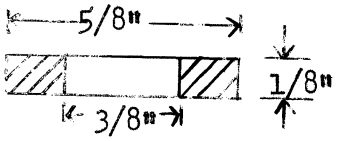
simplifying $L = \frac{N A \mu \; 4\pi N 10^{-8}}{10l}$

HYSTERESIS LOOP

of a Ferromagnetic Material



Core Dimensions



N = 10 turns

Scale

H = .01 Oerstedsper Division

B = 1 Kilogauss per Division

Hm = .14 Oersteds

Figure 8

(24) $L = (4\pi N^2 A \mu)(10^{-9})$(l in cm) = inductance in Henries

(25) but if $H = \frac{4\pi N I}{103L}$ where l (length) is in meters

(26) then $L = \frac{4\pi N^2 A u}{l}$ 10^{-11} for length in meters

It might be important to notice that the inductance and [illegible] are functions of permeability and consequently,

$E_o = L \frac{di}{dt} = N \frac{d\Phi}{dt}$, the voltage induced will be a function of permeability.

The permeability is a function of the average inductance and flux; consequently, the voltage induced by equation (19) would be the average voltage and also a function of the permeability. The developed equation (25) was introduced to show the relationship of flux intensity in the M.K.S. system in comparison to the C.G.S. systems. The centimeter - Grams-Seconds system has been utilized in the past to deal with small units but more recent experimentation has introduced a system for the analysis of much larger parameters with a minimum of cumbersome manipulations. The meters - kilogram - second system has been called the rational system of computation. (Most articles written on cores today utilize the M.K.S. system for explanation purposes.)

Figure 8 gives the hysteresis loop and core dimensions of a typical core. Assuming that a set of signals are applied to drive the core in the same direction (North pole saturation) how are the following computed with the given characteristics?

1. Find R_S (using Figure 8.)
2. Compute Δ Bn
3. Compute Δ Bs
4. The core is in the ZERO state-how much current is required to drive the core to the ONE state?
5. For an average time of 3 microseconds the ΔBn is developed, what is the induced voltage?
6. ΔBs occurs within an average time of 10 microseconds; determine the signal-to-noise ratio.

Solutions:

1. $Rs = \frac{Br}{Bm} = \frac{13\ (10^3)}{15\ (10^3)} = .866$ (Eq. 15)

2. $\Delta Bn = Bm - Br = 15\,(10^3) - 13\,(10^3) = 2\,(10^3)$ gauss (Eq. 24)

3. $\Delta Bs = Bm + Br = 15\,(10^3) + 13\,(10^3) = 28\,(10^3)$ gauss (Eq. 25)

4. $Hm = \frac{4\pi N\, Im}{10^3\, l}$ $\therefore$ $I\,m = \frac{Hm\, 10^3\, I}{4\ N}$, when using M.K.S. (Eq. 25) system N = 10 turns, Hm = .14 oersteds, $l = \pi\left(\frac{D + d}{2}\right)$ inches = $\pi\,(5/8 + 3/8)$ inches = $\pi(1/2^{n}) = \pi(1/2)(2.54)(10^{-2})$ meters thus substituting

$$Im = \frac{.14\,(10^3)\ (\pi)\ (1/2)\ (2.54)\ (10^{-2})}{4\ \pi\ 10}$$

simplifying

$$Im = \frac{.14(\cancel{10^3})(1/2)(2.54)\cancel{10^{-3}}}{4} = \frac{.14\ (2.54)}{8} = .14\ (.317) = 44.38 \text{ milliamperes (Eq. 16)}$$

5. (a) $Eavg\ \cancel{3}_{as} = N\,\frac{\Delta\,\Phi \text{ webers}}{\Delta t}$ but we must find N, Φ, and t.

N = 10 turns from the diagram.

(b) $\Phi n = B_n A$; Bn = 2 (10^3) gauss or $\frac{\text{Max.}}{Cm^2}$ and

$A = S^2 = (1/8)^2 = 1/64$ sq. inches.

(1 sq. inch = 6.45 sq. centimeters) 1/64 x 6.45 = .1 sq. cm. of area, substituting in (b) gives [Φn as 2 (10^3) max] . (10^{-1}) or 2 (10^2) maxwells. Substitution in equation (a) gives:

$Eavg\ \cancel{3}_{as} = \frac{2(10^2)(10^{-8})\ \ 10}{2\ (10^{-6})}$, where 1 maxwell = 10^{-8} webers.

Simplification yields (2/3) 10 volts or 6.66 volts. Thus we develop 6.66v as a noise voltage.

(c) $Eavg\ \cancel{3}_{as} = N\,\frac{\Delta\Phi s}{\Delta t}$ webers (Eq 16) for the signal voltage.

Since A = .1 sq. cm, $\Delta\,\Phi s$ = 28 (10^2) maxwells and $\Delta\,t$ = 10 (10^{-6}) seconds. The equation can be solved by substitution.

$$Eavg\ \cancel{3}_{as} = \frac{10\ (28)\ \ (10^2)\ \ (10^{-8})}{10\ (10^{-6})}$$

$$= \frac{\cancel{10}\ (28)\ \ (10^2)\ \ (10^{-2})}{\cancel{10}}$$

= 28 volts as signal voltage.
Notice that the calculations for the signal and noise voltages are average values.

6. The signal to noise ratio may be expressed as (Eq. 50)

$$\frac{ES}{En} = \frac{28v}{6.66v} = 4.2$$

The section solutions were based on average values to avoid the more complex differential equation type solution. A further analysis will allow the average permeability to be computer which will lead to the value of the average inductance of the 10 turn winding. The slope of the line "c" will give the average value of Mu as:

(28) $$\text{Mu avg} = \frac{\Delta Bt}{\Delta Ht} = \frac{30\ (10^3)\ \text{gauss}}{.28\ \text{oersteds}} = 107{,}142$$

Upon substituting the value of Mu average in the equation (Eq. 23) the value of the average inductance may be found.

(Eq. 23) $$L\ \text{avg} = \frac{4\pi N^2 A \mu}{l}\ 10^{-11};$$

where L is inductance in Henries, N is the number of turns, A is the cross-sectional area of the core is square centimeters, and l is the mean length of flux travel in meters. The inductance computed for this specific case and the following values would be:

a. N = 10 turns
b. A = .1 sq. cm.
c. l = (1/2) (2.54) (10^{-2}) meters
d. Mu avg = 107,142
then

(Eq. 23) $$L\ \text{avg} = \frac{4\pi N^2 A \mu}{l}\ 10^{-11},$$

becomes $$L_a = \frac{4\pi (100)\ (.1)\ (107{,}142)}{\pi\ (1/2)\ (2.54)\ (10^{-2})}\ 10^{-11}$$

$$= \frac{4\pi\ (100)\ (.1)\ (107{,}142)}{\pi\ (1/2)\ \ (2.54)\ (10^{-2})}\ 10^{-9}$$

$$= \frac{400\ (.1)\ (107{,}142)}{1.27}\ 10^{-9}$$

$$= \frac{40\ \ (107{,}142)}{1.27}\ 10^{-9}$$

$$= 1374000\ \ (10^{-9})\ \text{henries}$$

$$= 3.374\ \ (10^{-3})\ \text{henries or } 3.374\ \text{mh}$$

The value of inductance (average) for the 10 turns of the core is 3.374 millihenries.

CORE APPLICATIONS

The ferrite and tape wound cores have been employed in many fashions but the most significant utilization was in data handling devices. This value is true because of many factors, including the storage capability of this type of device. Recorded proof has shown an ability of the core to store data for several years without using any form of power consumption. After discussing transformer notation we will develop a few simple data handling networks to exemplify the typical usage of cores. Transformer notations - The transformer is a device utilizing the principle of magnetic induction for voltage transfer characteristics.

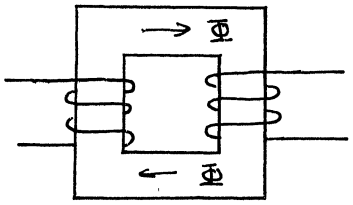


Figure 9

(N_1) primary winding - the winding in which a current has been directed

(N_2) secondary winding - the winding in which a voltage has been induced. The dot notation is used to give an indication of the induced potential from the primary winding into the secondary winding. The conventional current application causes I_1 to flow into the dot side of the primary winding (Figure 9). The current sets up a flux travel which induces the indicated polarity in the unloaded secondary winding. The current I_2 flows into (N_2) the secondary winding through the leakage and mutual inductance.

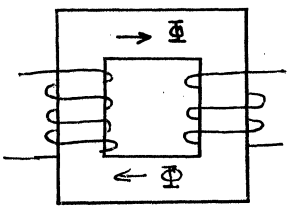


Figure 10

The conventional current flowing in the primary winding (N_1) caused by e_1 will cause a flux to exist as indicated (Figure 10). The flux will induce a voltage (e_2) in the secondary (N_2) as in the previous case (Figure 9). The current flowing in the secondary (I_2) will be in a direction to oppose the flux change which causes the current change (L enz's law). The current will flow thru the load and back thru the secondary (N_2). The flux direction in the secondary (using the right hand rule) will be now opposing the initial flux. An alternate theory is that the voltage in the secondary (induced) must act as a generator for the load and consequently establish the necessary counter electromotive force to produce the opposing flux change.

Since the transformer polarity of output is dependant upon the common point, it would be wise to notice that any polarity may be obtained with the proper phasing (grounding connections). Two examples are shown in Figures 11 and 12.

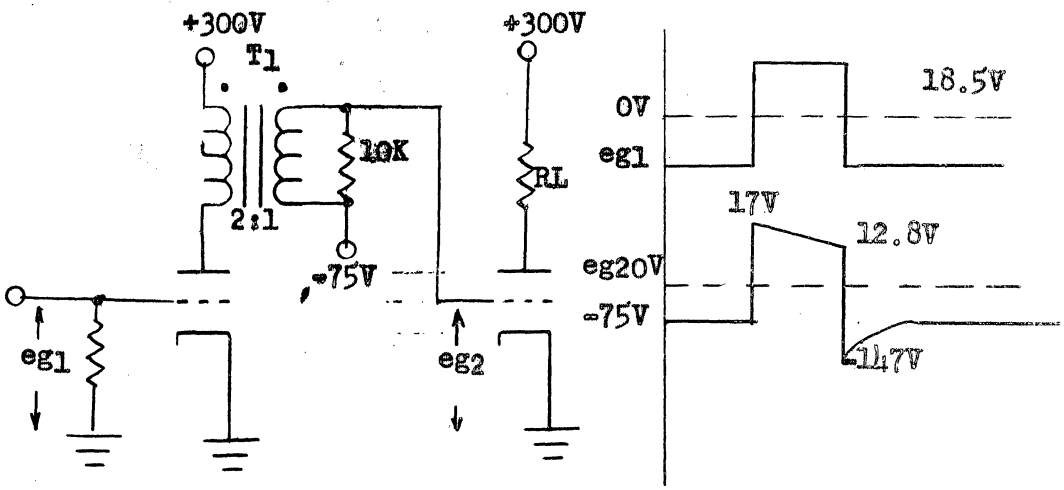


Figure 11

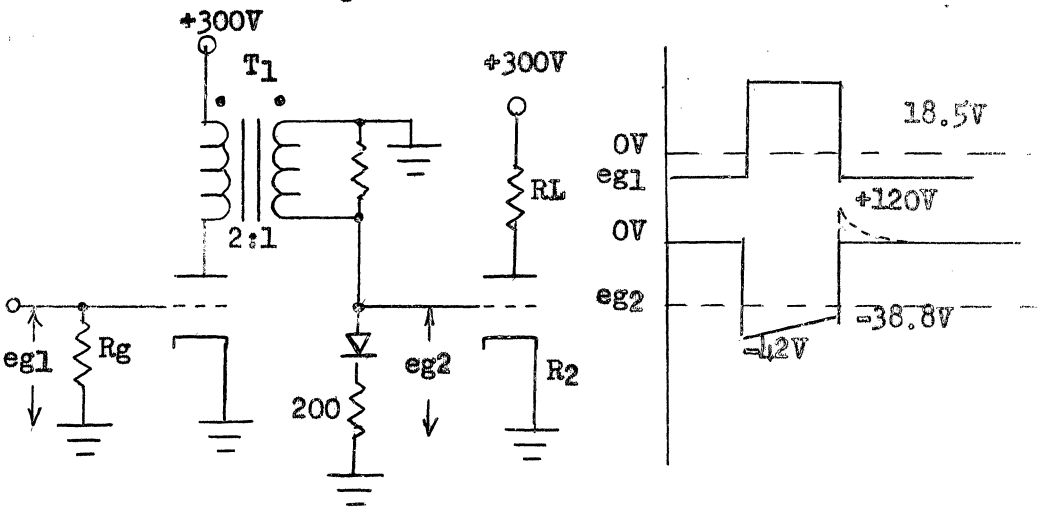


Figure 12

Figure 11 shows a method of driving the second amplifier, through the use of a pulse transformer, with the same signal polarity as the input signal. The second stage is being gated on or allowed to conduct. Figure 12 shows the same pulse transformer arranged to drive the second stage into its cut-off region. The only restrictions on transformer wiring arrangements are the number of leads on the transformer. The usual case will find four leads which will allow any reasonable circuit orientation. A unique case is found when two leads are made common by the manufacturer to restrict the number of leads to three at the transformer base. Obviously, the later case may only be used in specific design applications.

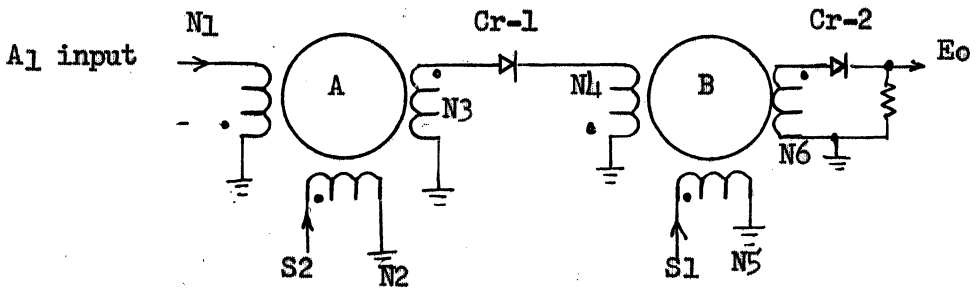
Although the transformers of the previous discussions were analyzed on the basis of perfection, practically the practical power losses due to Eddy currents will be large in a conventional transformer core. Laminated and powdered core forms have been used as the conventional means of reducing these effects. A pulse transformer utilizing a ferrite core will not be greatly concerned with this problem because of the high resistive characteristics of the semi-conductor core.

BASIC DATA HANDLING CIRCUITS

The cost of a batch of cores usually determines the design characteristics. As the squareness ratio and reciprocal of switching time increases the cost per core will usually increase. The cores to be discussed may either be ferrites or tape wound and will have a squareness ratio of 0.85 to 0.95 with a switching time of from 10 microseconds to 1 microsecond. Figure 13 and the following figures will be presented to further the understanding of basic core logic, while preparing us for the eventual fabrication of a core type serial full adder.

The single diode transfer loop is an example of a typical basic data handling network. The following analysis will show the basic considerations for a two core system.

SCHEMATIC



LOGICAL

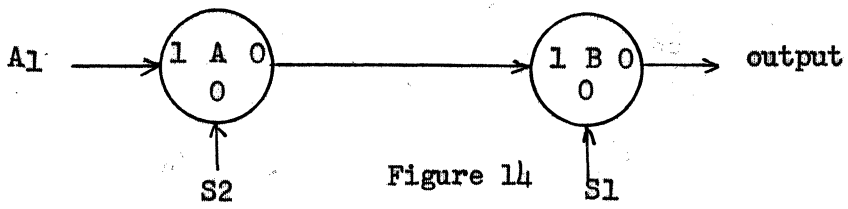


Figure 14

Figure 14 is a representation of the single diode loop with the core characteristics as indicated on Figure 13. The rules of design are

1. Current directed into the dot side of a core winding will produce a flux intensity which will be sufficient to drive the core flux to negative saturation. The core is said to be in the ZERO state of flux density and data storage.

2. Current directed into the non dot side of a core winding will produce a flux intensity that will cause the flux density to be at positive saturation. The resulting state of the core is labeled the ONE state or data stored condition of the core.

3. While the signal is applied, the core flux density will be at saturation. Figure 13 determined by Hm. When the signal is reduced to zero the core flux density will assume its remanence condition Br.

4. A signal applied will always produce a current and intensity of magnetizing magnitude.

5. Primary design parameters will be majorly concerned with forward flow of information, from input to output.

6. A core will always be cleared before loaded.

An analysis is now possible since we have established the rules of operation. The analysis will use the conventional current flow rule - current flows from the most positive to most negative points. The following is a detailed sequence analysis:

a. A shift pulse is applied to winding (N5) clearing the core "B" to the ZERO state.

b. A shift pulse is applied to winding (N2) clearing the core "A" to the ZERO state.

c. Data (A1) is applied setting core "A" to the ONE state.

d. A pulse (S1) is applied to clear core "B" to the ZERO state.

e. A pulse (S2) is applied causing core "A" to be set to the ZERO state and produces an output signal (Figure 13 - Bs) which causes core "B" to be set to the ONE state.

The timing of pulses will be as follows in Figure 15.

Notice in step e, data bit number one is stored in core "B" and since this represents (I and II) the end of one cycle of operation (Data bit plus a set of shift pulses), the data is being stored in core "B". The two core arrangement with the satisfying shift pulse organization will only be able to store "one bit of data per two cores". Often we call this a two-core per bit storage system.

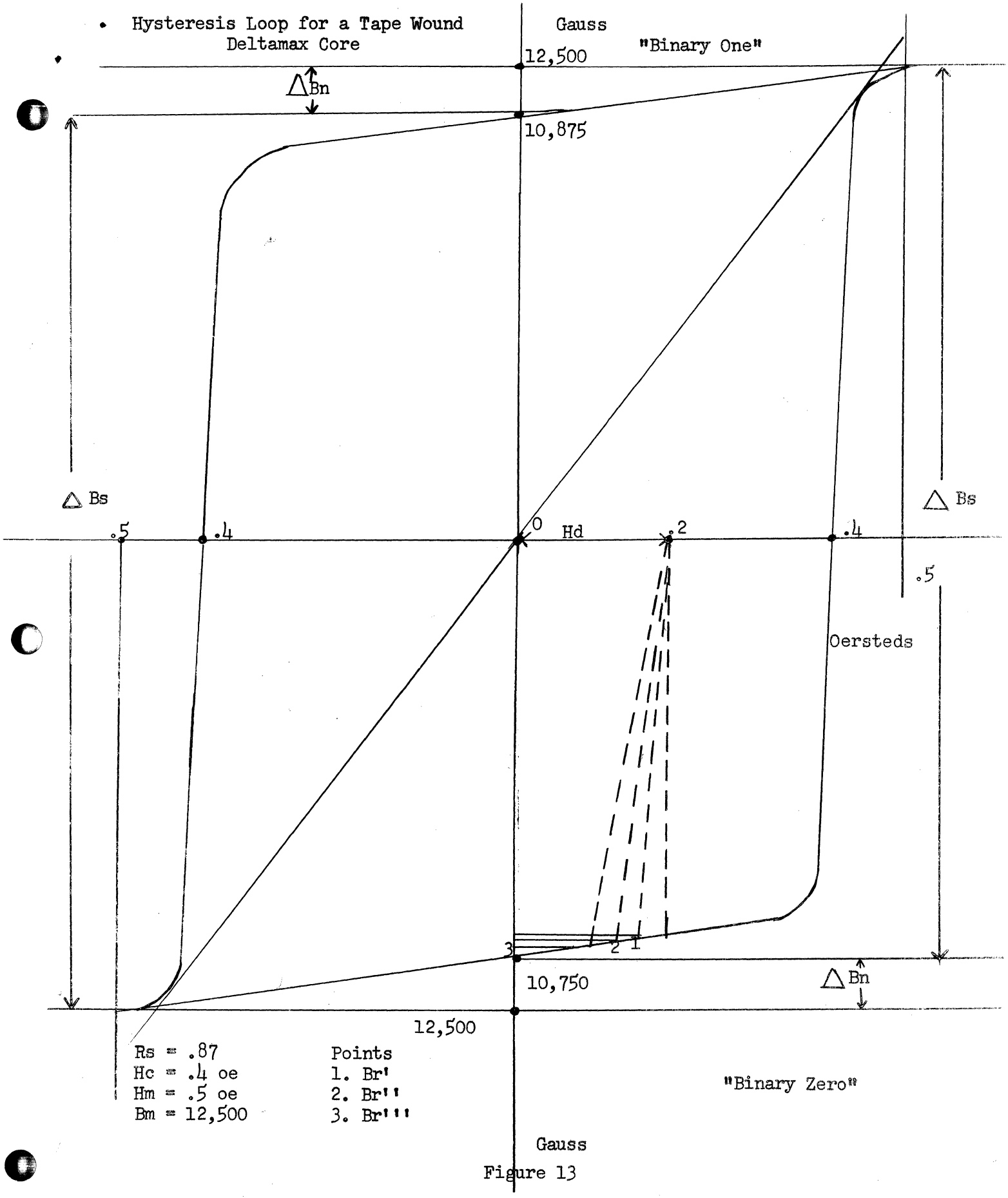

Hysteresis Loop for a Tape Wound Deltamax Core
Gauss
12,500
"Binary One"
ΔBn
10,875
ΔBs
ΔBs
.5
.4
0
Hd
.2
.4
.5
Oersteds
3
2
1
10,750
ΔBn
12,500
Rs = .87
Hc = .4 oe
Hm = .5 oe
Bm = 12,500
Points
1. Br'
2. Br''
3. Br'''
"Binary Zero"
Gauss

Figure 13

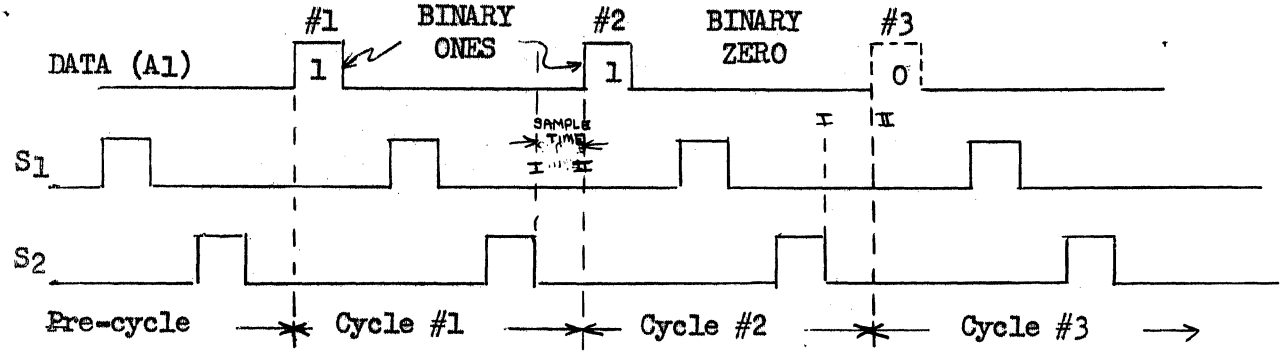


Figure 15

Utilizing the presented transformer theory and the pulses established in the previous paragraphs, a current flow analysis will be evolved. Current flowing in the non dot side of winding N1 will cause the core "A" to be set to the ONE state, this change of flux will be a function of a large flux density change (Figure 13). The current flow from the winding N3 will attempt to flow into the dot side of winding N4, but the current is also attempting to flow against the high back impedance of the crystal rectifier cr-1 which limits the current in winding N4 to a few micro-amperes (see Figure 16). The core "A" is now temporarily storing the input data (Figure 10), while core "B" has retained a "disturbed" zero state (Figure 13). The disturbed ZERO occurs when the resulting applied current is one half Hc or less an produces a small output voltage.

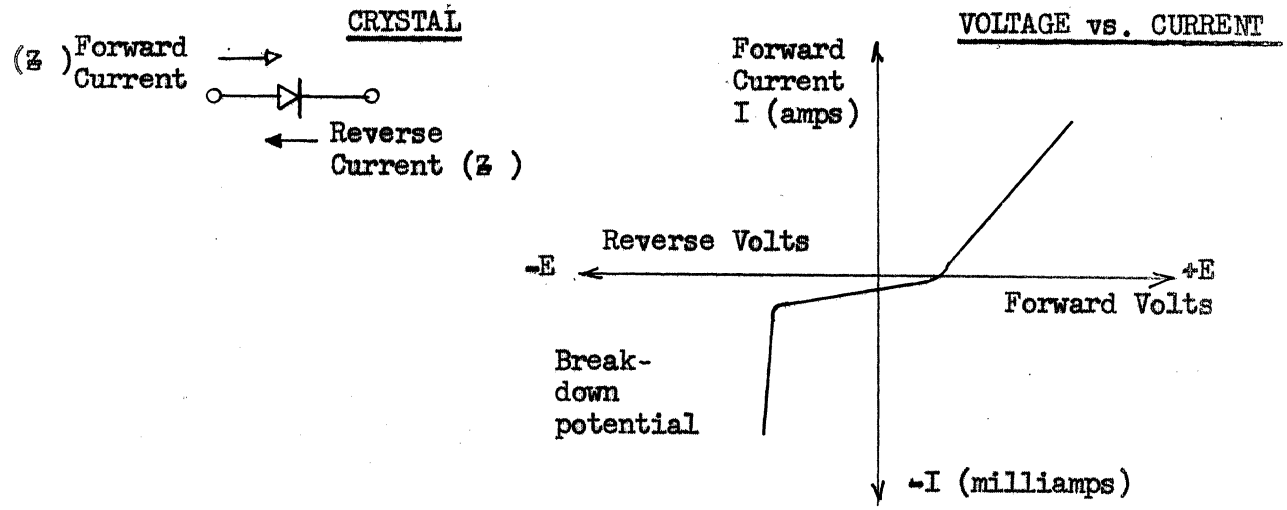


Figure 16

CRYSTAL CHARACTERISTIC CURVE

When the shift pulse (S1) is applied to core "B" (Figure 13, point 3), the core is driven from Br' to saturation - Bm the noise voltage caused by Bn will increase by a small fraction in the output (Noise signal growth). The pulse (S2) applied to core "A" now causes "A" to switch states, producing a flux change of Bs. The step up ratio of N2 to N3 causes Cr-1 to pass a greater current into the non-dot side of the winding N4. This N4 current causes core "B" to switch from the ZERO state to the ONE state, consequently impressing a noise voltage across the load resistor. At the end of cycle number one we again notice that the data is held by core "B" not core "A" - proving that this is a two core per bit storage system. A read out of core "B" with a stored binary one will now be considered. A shift pulse (S1) applied to N5 will cause a flux reversal within the core material. The flux reversal will induce a voltage in the winding N6 which will be of a magnitude determined by the flux change value; the crystal Cr-1 will pass the current through R_L to cause a voltage drop representing the signal change. In coincidence with this change, a voltage will be induced into winding N4 which will cause a current to flow through the Cr-1 forward impedance after passing into the non-dot side of the winding N3. This current will attempt to set core "A" to the ONE state (back transfer of data). The N5 to N4 step down ratio will attenuate the back transfer voltage so that the small voltage will drive a minute value of current into the high impedance 60 turns of N3. The non linear operations of Cr-1 will also aid in reducing the back transfer of data (see Figure 16, area 2). The signal to noise voltage comparison is seen in Figure 17. Point "A" indicates the conventional ratio (4:1), while point "B" indicated the sense time ratio of signal to noise.

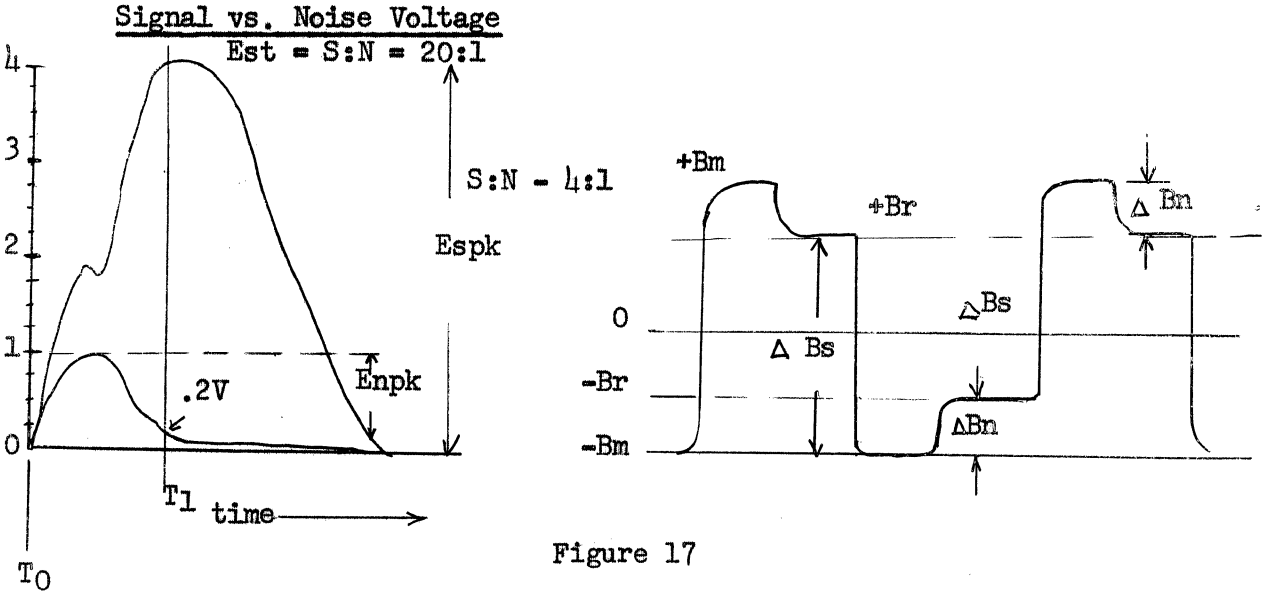


Figure 17

The Es_t signal to noise ratio may be obtained by reading the output (T1) time from (T0) time zero. This sense time arrangement is usually incorporated in memory plane configurations rather than the conventional data processing and storage register circuitry. Chart 4 and Figure 13 may be studied as an indication of the Noise Signal Growth convictions. The

transfer of data from any core in the single diode loop establishes a resultant ZERO state, therefore the name of a destructive read-out system.

The logical representation of the single diode transfer loop is represented in Figure 16. Each core representation is a circle with the core identification inscribed. Arrows directed towards the core indicates the signal application; wherein, the number within the core indicates the state of the core after that particular signal has been applied. The connection from core to core indicates the transfer ability of the device. The ZERO in the preceding core indicates that the diode connection is such that a signal will be passed to the following core when the preceding core is switched to the ZERO state. The ONE in the second core indicates the condition of this second core after the signal has been fed from the preceding core. The arrows to the ZEROS in the cores indicate with S1 and S2, the shift pulses, the condition of the core after these pulses are applied.

When a number of cores are hooked in series, they are usually utilized to shift and possibly store data from unit to unit.

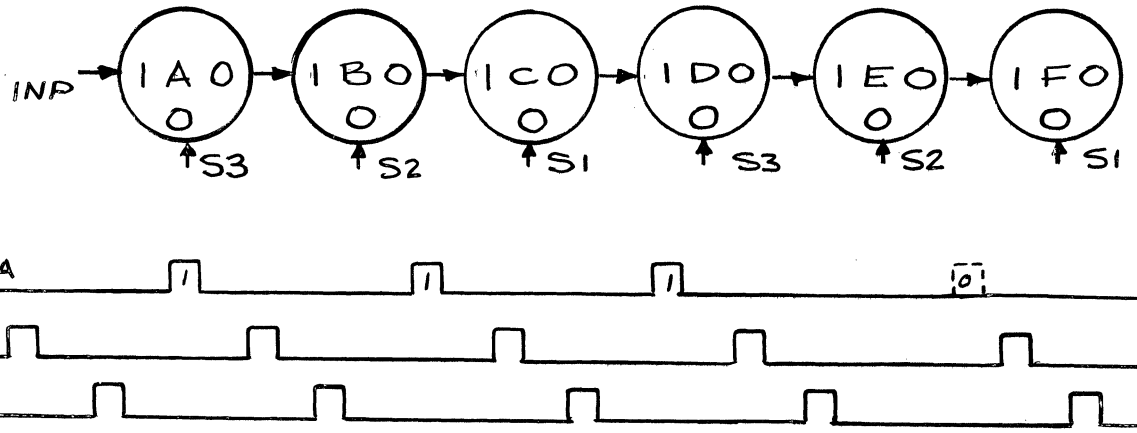


Figure 18 - Two Core Per Bit Shift Register and Timing

Since for each two cores only one stores data, we see that for six cores we may store three bits of data. System of analysis - overall arrangement

Basic Arrangements:	2 cores	6 total cores
bits stored	1	3 total bits stored

but assuming any number of cores or for example - 96 cores in a two core per one bit system - basic arrangements

shift pulses (cores) $\frac{2}{1} = \frac{96}{X}$ cores total bits stored
bits

(h) $2X = 96$

$X = 48$ bits total storage

Notice that this arrangement only requires two shift pulses per set of cores; however, they are used over and over again, therefore in (h) the two represents the number of shift pulses per set. (X) also represents the number of sets (S1 and S2) of shift pulses required to load or unload the shift register. Power assumption is at a minimum because we only have two lines for the shift pulses - example:

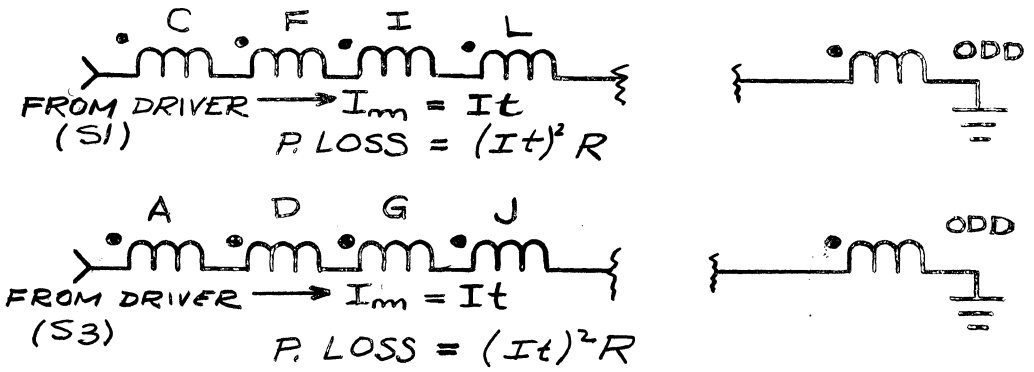


Figure 19 - Drive Winding Arrangement (series) for Figure 18

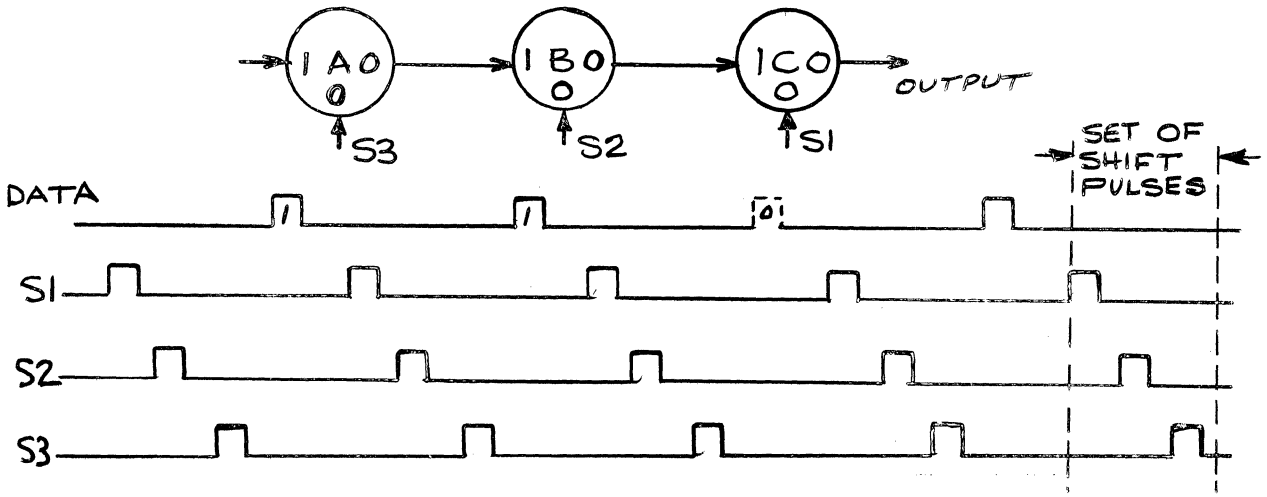


Figure 20 - Three Core Per Two Bit System and Timing

Figure 20 shows a 3 core per two bit shift register which will be analyzed the same as the previous register.

Original system

$$\frac{\text{(shift pulses)}\quad\text{(cores)}\quad 3}{\text{bits stored}\qquad\qquad 2}$$

Total system

$$\frac{24 \quad \text{cores total}}{X \quad \text{bits total storage (load or unload sets of shift pulses)}}$$

or

$$\frac{3}{2} = \frac{1}{2}\,\frac{24}{X}$$

$3X = 48$

$X = 16$ bits total storage

$*$ (sets of pulses for loading)

If 72 cores were used in the same system -

$$\frac{(\text{Shift pulses per set})\ (\text{cores})\ 3}{\text{Basic bits stored}\quad 2} = \frac{72 \text{ cores total}}{X \text{ bits total storage}\ *(\text{sets shift pulse for load})}$$

$3X = 144$

$*X = 48$

48 bits of data stored and 48 sets of shift pulses for loading or unloading the entire system.

The greater the number of cores used in a system, the greater number of bits stored, and the greater becomes the power losses in respect to other core systems. The core registers are more efficient than vacuum tubes because no power is consumed in cores while storage is in process. For a more detailed description of the various shift and storage register core configuration consult - Bimag Circuits for Digital Data-Processing by W. Michle, Burroughs Corporation.

The double diode loop was assembled to compensate for the disadvantages of the single diode transfer loops. It may be seen that problems of unconditional transfer of data, noise growth, and many other problems common to the single diode loop will become extinct with the analysis of the double diode loop (see Figure 21).

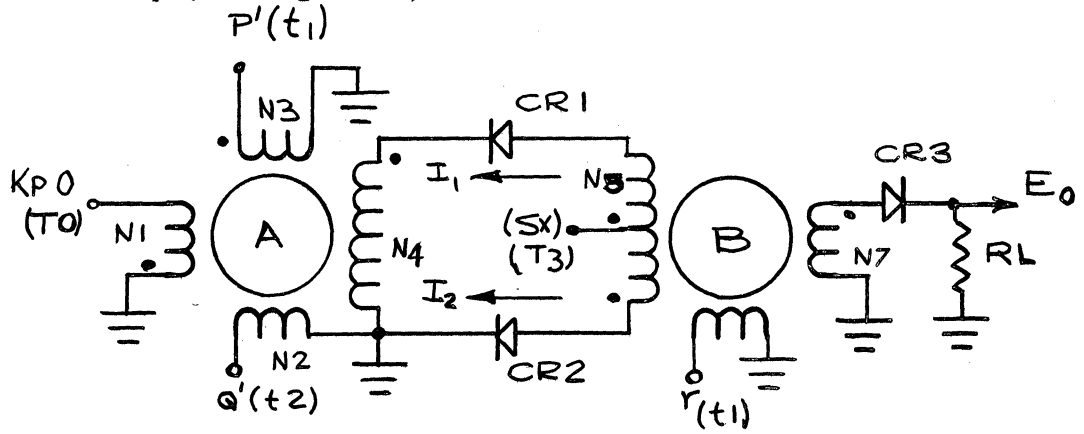


Figure 21 - Double Diode Transfer Loop

DOUBLE DIODE TRANSFER LOOP

Figure 21a shows the schematic diagraom of the double diode transfer loop with a resistive load on the output line to develop the systems indicated voltage.

Static conditions -

(Kp) N1 - set winding which puts core "A" in the ONE state.

(q') N2 - signal winding - puts core "A" in the ZERO state.

(p') N3 - signal winding - puts core "A" in the ZERO state.

(Op) N4 - output winding of core "A"

N5 - split winding - upper half sets core "B" to the ZERO state, while the lower half sets core "B" to the ONE state.

(r) N6 - signal winding - sets core "B" to the ZERO state.

(op2) N7 - output winding core "B" - feeds cr3 and R1 to develop Eo.

Operation -

*Note: (See Figure 21a and c). A. Cycle #1 - The application of Kp sets cores "A" to the ONE state. Signal p' applied causes core "A" to be set to the ZERO state. The induced voltage in N4 has no path for current flow so that core "B" is not disturbed. Signal q' applied attempts to set the already established ZERO state of core "B". The application of Sx finds the following sequences of reactions:

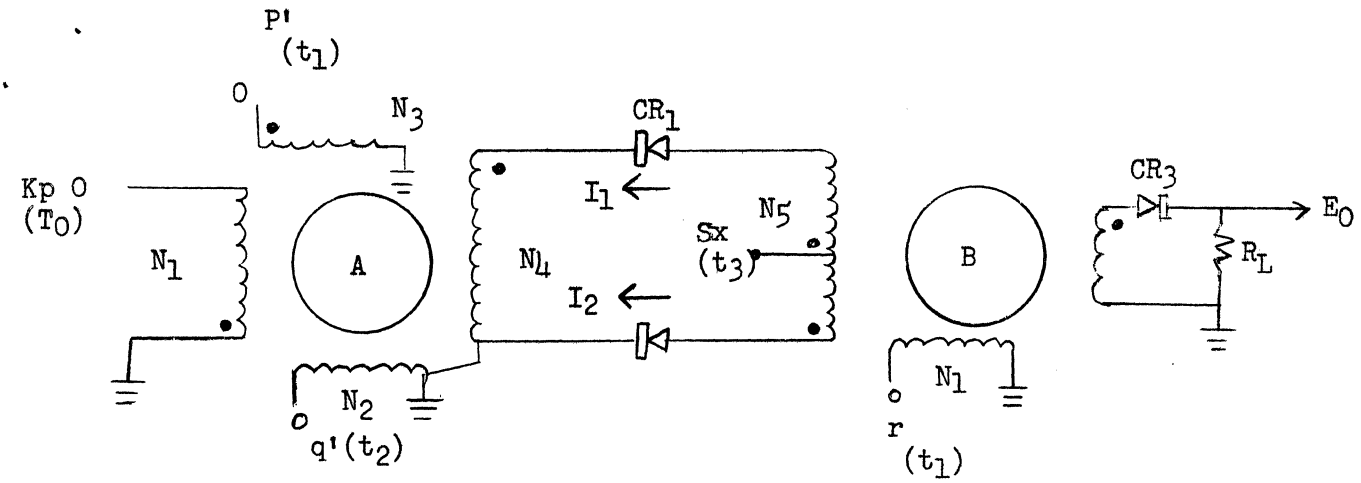
1. The Sx current splits to flow through cr1 and cr2 thus becoming I1 and I2. Since the crystal characteristics are equal the currents are equal.

2. Each half of N5's intensities are equal and opposite, moreover the intensities cancel to cause no effect on core "B".

3. Winding N4 has a very low impedance while core "A" is being driven in the same ZERO saturation direction. Cores "A" and "B" remain in the ZERO state, while the signal r which is applied to core "B" has no effect in producing an output Eo. Cycle 3 and 5 will cause the same effective operation of the loop.

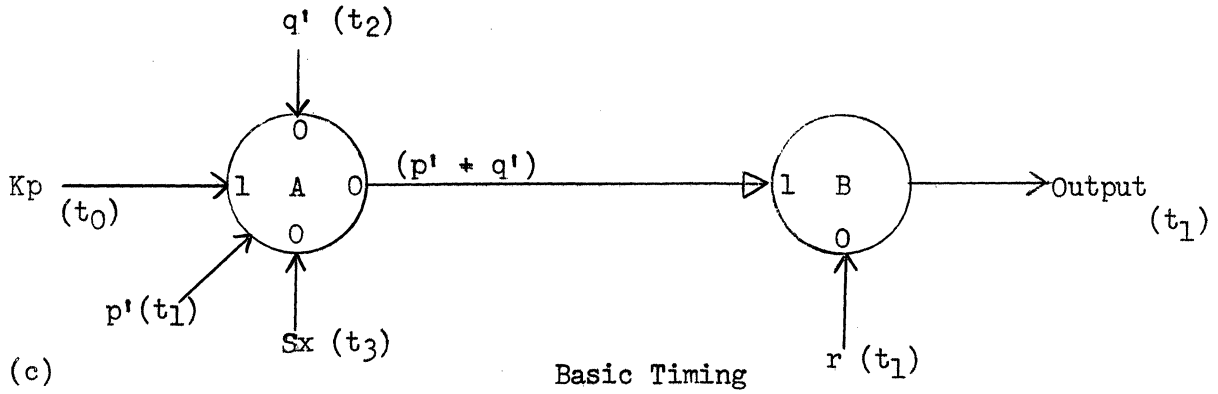
B. Cycle #2

The clock pulse will cause core "A" to be set to the ONE state. The absence of signals p' and q' will allow a static ONE state condition of core "A" until Sx is applied. Sx applied will cause the following actions:



(a) Schematic of Double Diode Transfer Loop

Logical of Double Diode Loop



(c) Basic Timing

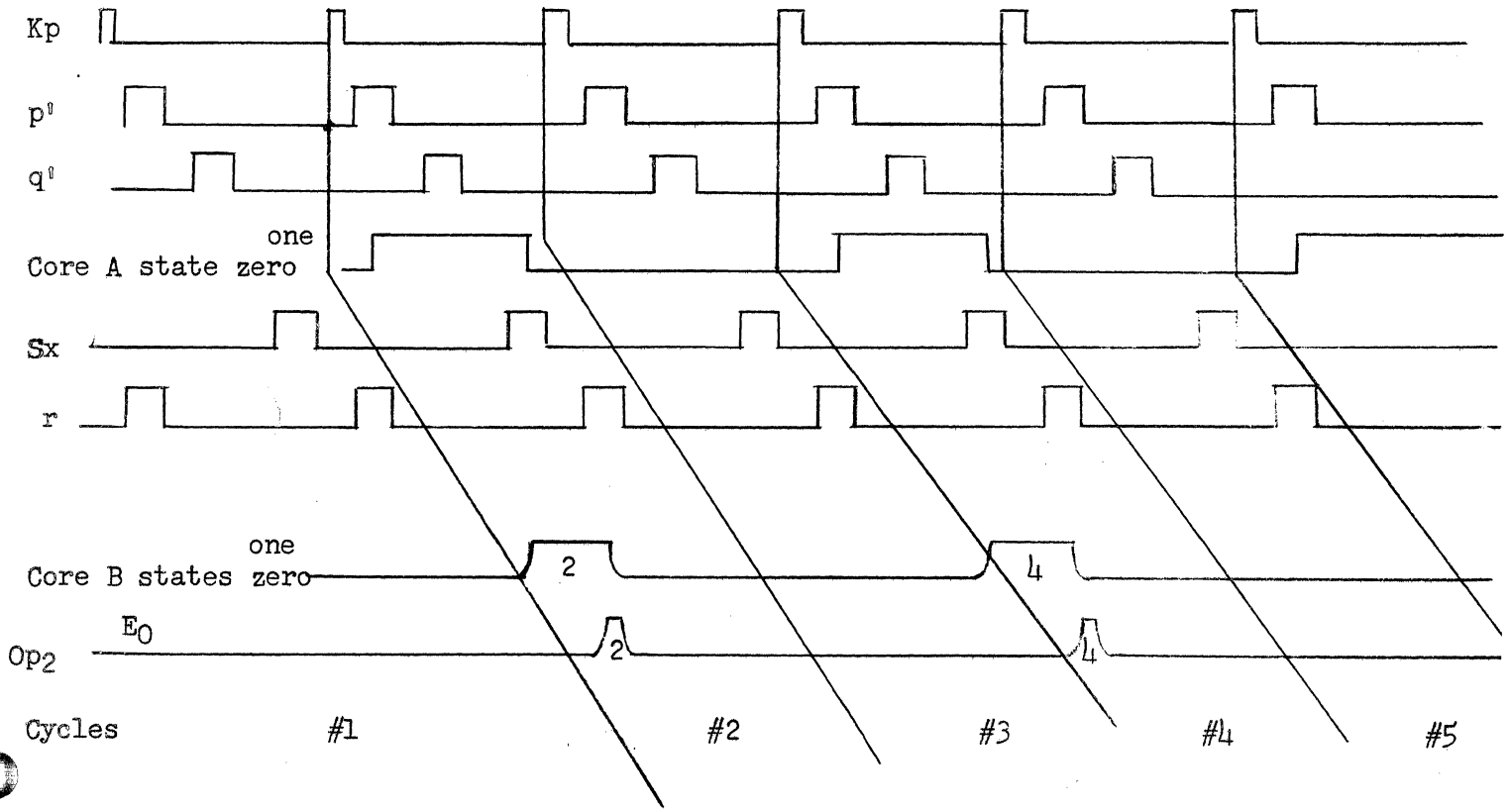


Figure 21

1. Sx current splits thru each half of N5 to become equally I1 and I2. The crystals cr1 and cr2 will pass the currents because of their forward characteristics.

2. I1 will cause core "A" to switch to the ZERO state which causes the N4 impedance to increase with the effect of reducing the magnitude of current I1 (see Figure 22).

3. I2 seeing I1 on the decline produces an intensity which drives core "B" to the ONE state. The currents again become balanced but the cores continue to switch after having gained the required switch inertia.

The result is core A now in the ZERO state with its data appropriately stored in core "B". The signal r applied to core "B" causes "B" to switch

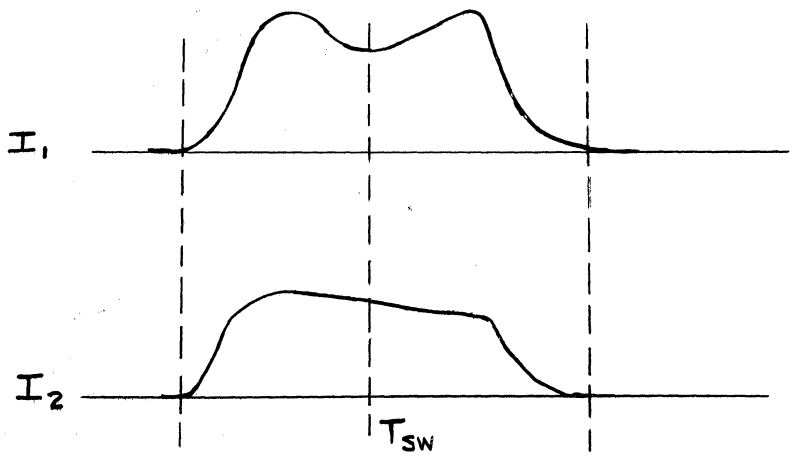


Figure 22-Switching Currents

to the ZERO state, to produce an output voltage in N7, to force cr3 into conduction, to produce a current flow into R1 and to produce an output Eo which indicates that data has been processed through the double diode loop.

The operational characteristics should have clearly established the advantages of this circuit compared to the single diode loop as

1. A transfer of data from core "A" to core "B" happens only at Sx time and if the core "A" is in the ONE state (conditional transfer).

2. Core "A" switching operations have no related effect controllable by core "A" or core "B".

The data in both cores will be last at read-out time (Destructive read-out).

Logically we see another inherent function of this loop. When feeding core B, the line is represented as signals p' or q' notted - $(p' + q')'$ and functionally is p·q. This signal is fed to core "B" and in order to produce an output Eo little r must be present.

Functionally Eo = $(p' + q')' \cdot r = q \cdot q \cdot r$

Core "A"'s arrangement serves as an OR gate, while core "B" functions as an AND gate.

The "Exclusive OR" circuit

Figure 23 shows a schematic and logical representation of the "Exclusive OR" circuit. The truth chart indicates the binary operational reactions of the circuit; moreover, it is noticed that an output occurs only when either A or B is present but not when A and B are present. It must be recalled that when a core is switching states the impedance is relatively large because $Z = f(L)$ or $Z \cdot XL \cdot L \cdot M$ wherein Mu at this time is large in magnitude. Remembering this we will proceed to consider the following three cases:

1. A and B are not present -

   a. cores A, B, C, and D are in the ZERO state.

   b. Tx applied causes I1 = I2 to be generated and flow through the upper and lower legs.

   c. cores A and B being in the ZERO state offer a small impedance which has little effect on current caused series bucking effect of the cores C and D set windings. C and D remains in ZERO state.

   d. T_Z applied attempts to set core E to its already ZERO state causing no output signal to be present when S, the shift pulse is applied.

   e. conclusions - A' and B' = Eo'

2. A is present and B is not

   a. core A is in the ONE state, while core B is in the ZERO state.

   b. Tx applied finds I, attempting to switch core "A" to the ZERO state (high Z), thus the flow of I2 exceed I1 and switches core "D" to the ONE state. Core "A" continues to switch to the ZERO state, while cores "C" and "B" retain their initial conditions. The data stored in "A" is now in core "D".

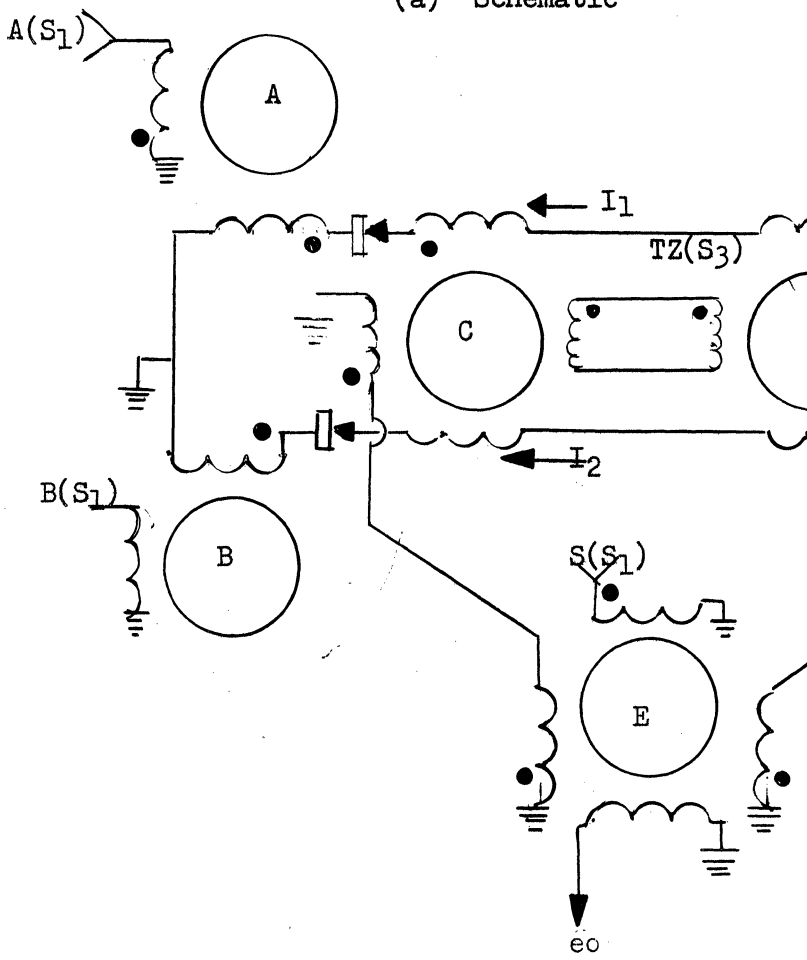
   c. T_Z applied will set cores C and D to the ZERO state and "D" will generate an output voltage to set core "E" to the ONE state. The data stored in D is now found in "E".

   d. The shift pulse, S, causes core E to switch to the ZERO state and produce an output, Eo.

Figure 23

Exclusive "OR" Circuit

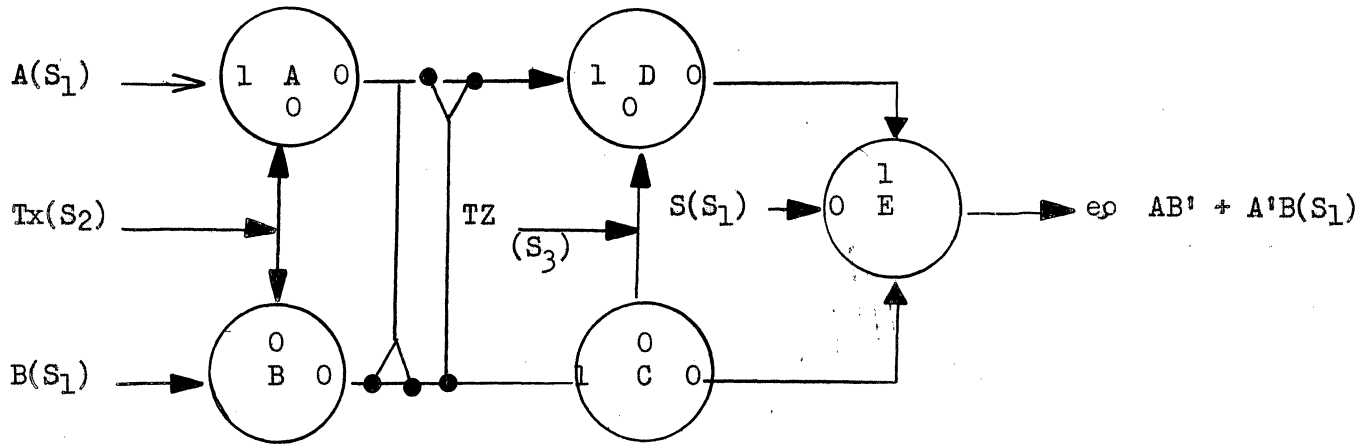
(a) Schematic



Signal Truth Chart

A	B	Currents	eo
0	0	$I_1 = I_2$	0
1	0	$I_1 \quad I_2$	1
0	1	$I_1 \quad I_2$	1
1	1	$I_1 = I_2$	0

(b) Logical



e. Conclusions: - If A · B' or A' · B are present an output, Eo will be generated. A signal delay of one cycle is present from A or B input to e_o generation.

3. "A" and "B" are present -

a. cores "A" and "B" are set to the ONE state.

b. Tx applied will cause I1 and I2 to flow through legs 1 and 2, attempting to set "A" and "B" to the ZERO state (high Z). Since both legs are looking into the windings of switching cores, the resulting currents will remain equal and the opposing winding arrangement will inhibit data transfer.

c. T_Z finds no output generated from cores "C" and "D", thus no signal is transferred to core "E".

d. S applied will cause no change in the output winding of core "E", consequently e_o will remain at a zero level.

e. Conclusion: - If A and B are present or A' and B', (A·B or A'·B'), the data is inhibited to cause no output effects.

4. Rules of operation - An output, e_o will only be produced if A or B is present but not if both A and B are present. The Exclusive OR functional notation will be the encircled plus sign, ⊕ , see Figure 24)

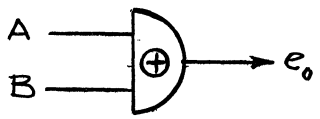


Figure 24.

Exclusive OR Functional representation

$$e_o = AB' + A'B = A + B$$

$$e_o' = AB + A'B' = (A + B)'$$

SERIAL FULL ADDER FABRICATION

Having developed the basic logical circuits required for the adding functions, we may now proceed to consider the requirements of a Serial Full Adder. The basic equations may be derived from an analysis of the basic adding functions of the given orders a, b, and c.

	msb			Lsb	
orders	x_1	c	b	a	Designation
Augend	0	1	1	1	A
Addend	0	1	0	1	B
Old Carry	1	1	1	0	C_1
New Carry		1	1	1	C_2
Sum	1	1	0	0	S

Figure 25

When adding A and B it is found that either may have one of two possible conditions (Binary system), and in order to generate sum in Figure 25 we must have A, B, and a carry. The total number of possible conditions will be found to be $2^3 = 8$ which is the basic count of from zero to seven.

Truth Chart: cases	A	B	C_1	S	C_2
	0	0	0	0	0
	0	0	1	1	0
	0	1	0	1	0
	0	1	1	0	1
	1	0	0	1	0
	1	0	1	0	1
	1	1	0	0	1
	1	1	1	1	1

Figure 26

From Figures 25 and 26 general equations for the sum and carry may be stated as:

$$S = f(A, B, C) \text{ and}$$

$$C = g(A, B, C).$$

Upon recording the conditions of Figure 26 (blocked), we may derive specific equations for the sum and carry.

By case - Sum = 1, 2, 4, and 7

$$S = A'BC + AB'C + ABC' + ABC$$

and the Carry = cases 3, 5, 6, and 7

$$C = A'BC + AB'C + ABC' + ABC$$

Notice:

1. In a true multi-order adder device the carry is a function of the machine and not the output (see Figure 27).

2. The speed of addition is determined by the speed of the carry generation.

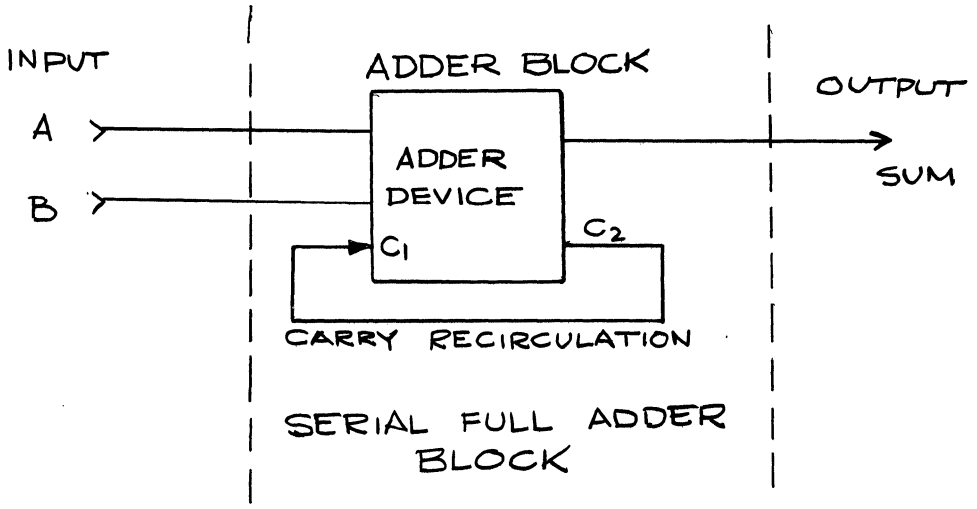


Figure 27

Recalling the "Exclusive OR" arrangement, it is seen that the following is true.

(1)

	B	C	x						
a.	0	0	0	=	B'	x	C'	=	x' =
b.	1	0	1	=	B	x	C'	=	x =
c.	0	1	1	=	B'	x	C	=	x =
d.	1	1	0	=	B	x	C	=	x' =

(2) or $x = B \cdot C' + B'C = B + C$

(3) $x = B \cdot C + B'C' = (B + C)'$

The above equations will allow an "Exclusive OR" revision of the specific sum and carry equations as seen above.

$$S = AB'C' + ABC + A'BC' + A'B'C$$

$$S = A(B'C' + BC) + A'(BC' + B'C)$$

simplified from

$$(3)\quad (B'C' + BC) = (B + C)'$$

$$(2)\quad (BC' + B'C) = (B + C),$$

$$S = A(B + C)' + A'(B + C)$$

then let $(B + C) = Z$, then substitution gives

$$S = AZ' + A'Z$$

from (2) $(AZ' + A'Z) = (A + Z)$

$$S = A + Z$$

substituting gives $S = A + (B + C)$

and the carry is found to be

$$C = ABC' + AB'C + A'BC + ABC$$
$$= A(BC' + B'C) + BC(A' + A)$$
$$= A(BC' + B'C) + BC$$
$$C = A(B + C) + BC$$

simplified from

$$(2)\quad (BC' + B'C) = B + C$$

Notice that the carry equation has been arranged to allow for utilization of the common exclusive or circuit. Figure 28 indicates the exact functional arrangement.

Figures 28 and 29 will indicate the functional and operational core arrangement which produces the serial full adder. The following two cases will be discussed to show the general operational procedures (see Figure 29).

1. A and B are present (Binary 1's) with NO carry.

   a. Shift time one, (S_1).

      (1) A at S_1 time sets cores V_{21} to the ONE state, while setting A22 to the ZERO state.

      (2) B at S_1 time sets V_{11} to the ONE state, while setting A10 to the ZERO state.

      (3) Carry, Co being "0" is shifted to V_{10} at S_1 time.

   b. Shift time two, S_2

      (1) S_2 transfers the binary one in V_{11} to V_{13} and the logical "0" from V_{10} to V_{12}.

(2) S_2 finds no transfer of data from A_{10} to A_{11}.

c. Shift time three, S_3

(1) S_3 transfers the data from V_{13} to A_{21} and V_{20} while V_{12}'s output is not present.

(2) S_3 does not cause A_{11} to set A_{12} to the ZERO state.

d. Shift time four, S_4

(1) S_4 finds cores V21 and V_{20} containing binary ones, thus a transfer is inhibited.

(2) S_4 does NOT cause A_{22} to set A_{21} to the ZERO state.

e. Shift time five, S_5

(1) S_5 transfers nothing from V_{22} and V_{23} so that the sum indicated by the state of TR1 is ZERO.

(2) S_5 finds A_{21} in the ONE state, thus core A_{12} is set to the ONE state for an indication of carry ONE to the next order.

(3) S_5 presets A_{22} and A_{10} to the ONE state.

f. Conclusions: Since we fed in two binary ones, extracted a sum of zero and indicated a carry for the next order, we may conclude that this circuit will perform the basic adding functions required.

2. Assume that A and Co are present (Binary "1") and B is not present (Binary "0")

a. Shift time one, S_1

(1) S_1 applied will allow A to set V_{21} to the ONE state.

(2) S_1 will cause A to set core A_{22} to the ZERO state.

(3) Core A_{12} will shift a "1" to cores V_{10} and A_{11}, while "B" input has no effect.

b. Shift time two, S_2

(1) S_2 will allow A_{10} to set A_{11} to the ZERO state.

(2) S_2 applied shifts the "1" in V_{10} to V_{12} and the "0" from V_{11} to V_{13}.

c. Shift time three, S_3

(1) S_3 will allow A_{11} to have no effect on A_{12}.

(2) S_3 will shift the "1" in core V_{12} to V_{20} and A_{21}

d. Shift time four, S_4

(1) S_4 finding data in V_{21} and V_{20}, will not cause data transfer to V_{22} and V_{23}.

(2) S_4 will allow A_{22} to have no effect on A_{21}.

e. Shift time five, S_5

(1) S_5 will transfer the "1" in A_{21} to A_{12} to indicate a new carry for the next order.

(2) S_5 will not find any data to be transferred to core TR1, thus an indication of a sum "0".

(3) S_5 will preset A_{10} and A_{22} to the ONE state.

f. Conclusions: - The applied A = "1" and Co = "1" with B = "0" produced a sum of zero and an indication of a new carry, thus we may conclude that the carry circuit will function properly.

A complete Serial Full Adder assembly will resemble the example system shown in Figures 31 and 32. Although the M.S.R. shown is organized to handle a five order arrangment in the input circuit, it is possible to alter the system to allow for a more elaborate input section. The only basic requirement is that the output section M.S.R. must be designed to facilitate one additional order for the generated sum. The input and output section timing is a function of the adder's timing necessities. Figure 30 indicates the core winding configurations required for the Serial Full Adder. It is advisable for the reader to plot the timing diagram of the least one complete set of orders to gain a better understanding of the function operation (flux diagrams found in Figure 17 will be helpful).

SUMMARY

The advent of the ferrite and metallic core has paved the way for many new computer solid state designs. The information presented on the cores, data handling loops, and the adder was organized to give the reader more insight as to possible core applications not the atomic theory of the core itself. The analogies are to be accepted more as a general aid and not as a conclusive report. Chart V will give a brief survey of the various applications and characteristics of ferrites, while a leter information sheet will be devoted to the atomic theory of bimagnetic core analysis. That temperature of operation in an inverse function of the ferromagnetic core is clearly seen in the later atomic studies and should be considered in the general core's circuit design. The bibliography found on the last page of this information sheet should prove to be most enlightening to the progressive reader who desires additional specific information.