FIELD ENGINEERING TECHNICAL MANUAL

Burroughs

B 475

DISK FILE STORAGE MODULE

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1.1 GENERAL DESCRIPTION

The B475 Storage Module is one of the three units which make up the Disk File Subsystem. The basic Subsystem consists of:

The B450 Basic Control Unit which is a B5500 cabinet with Power Supplies and a B470 Disk File Control Assembly.

The B472 which consists of two units butted together. The cabinet on the left houses the B471 Electronics Unit (E.U.). The cabinet on the right encloses the B475 Storage Module (S.U.).

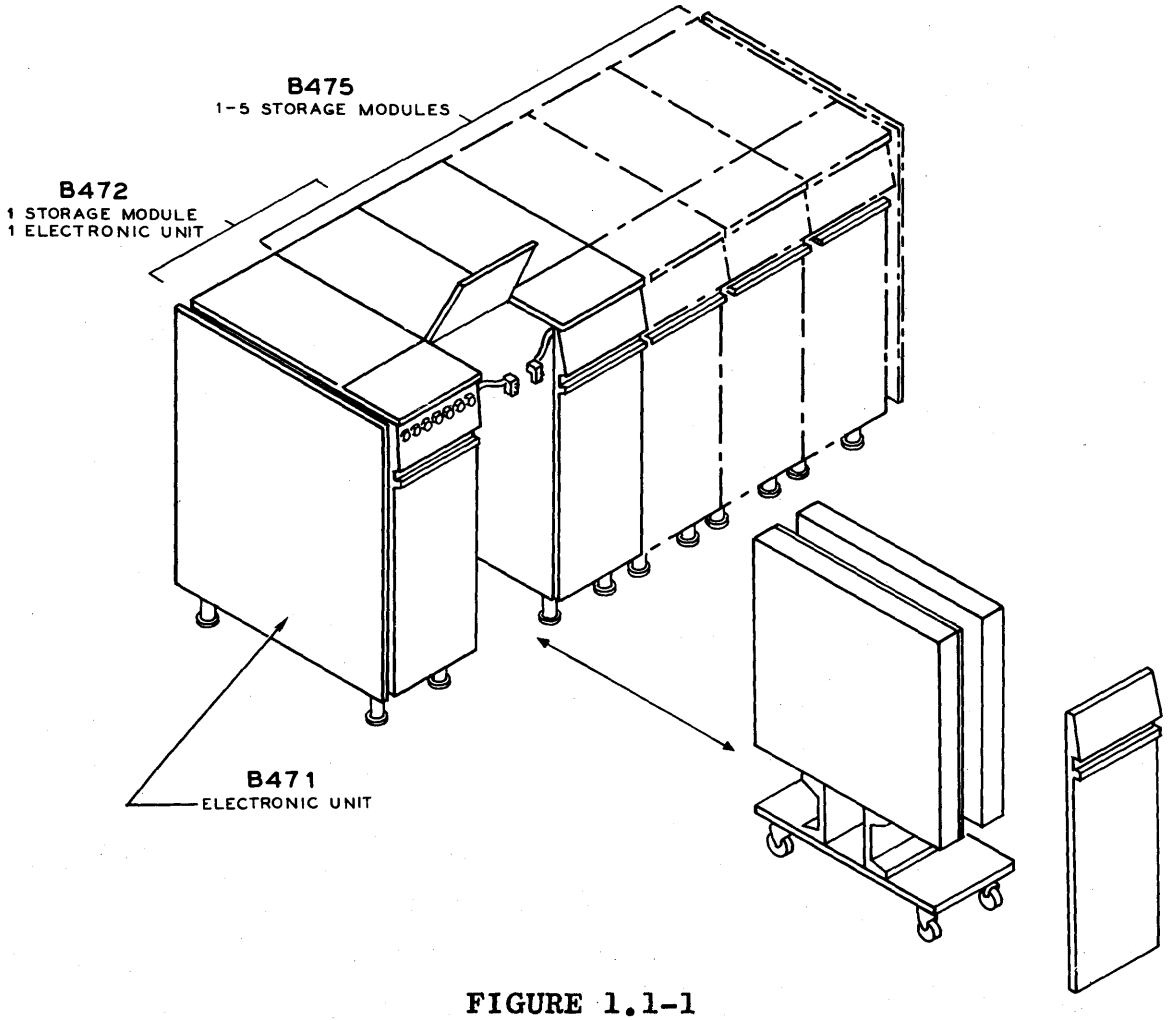

FIGURE 1.1-1
MODULAR DESIGN - DISK FILE

Refer to Figure 1.1-1. Four more cabinets and four more B475's can be added to the right. Five B475's represent the maximum that can be handled by one B471 E.U. A B200 series Central Processor can handle up to 10 E.U.'s. A B5500 system can handle up to 20 E.U.'s when a

second B470 Control Unit is added.

The B475's are mounted on casters and housed in a garage type of cabinet. With this type of modularity, an S.U. may readily be added to existing equipment in the field.

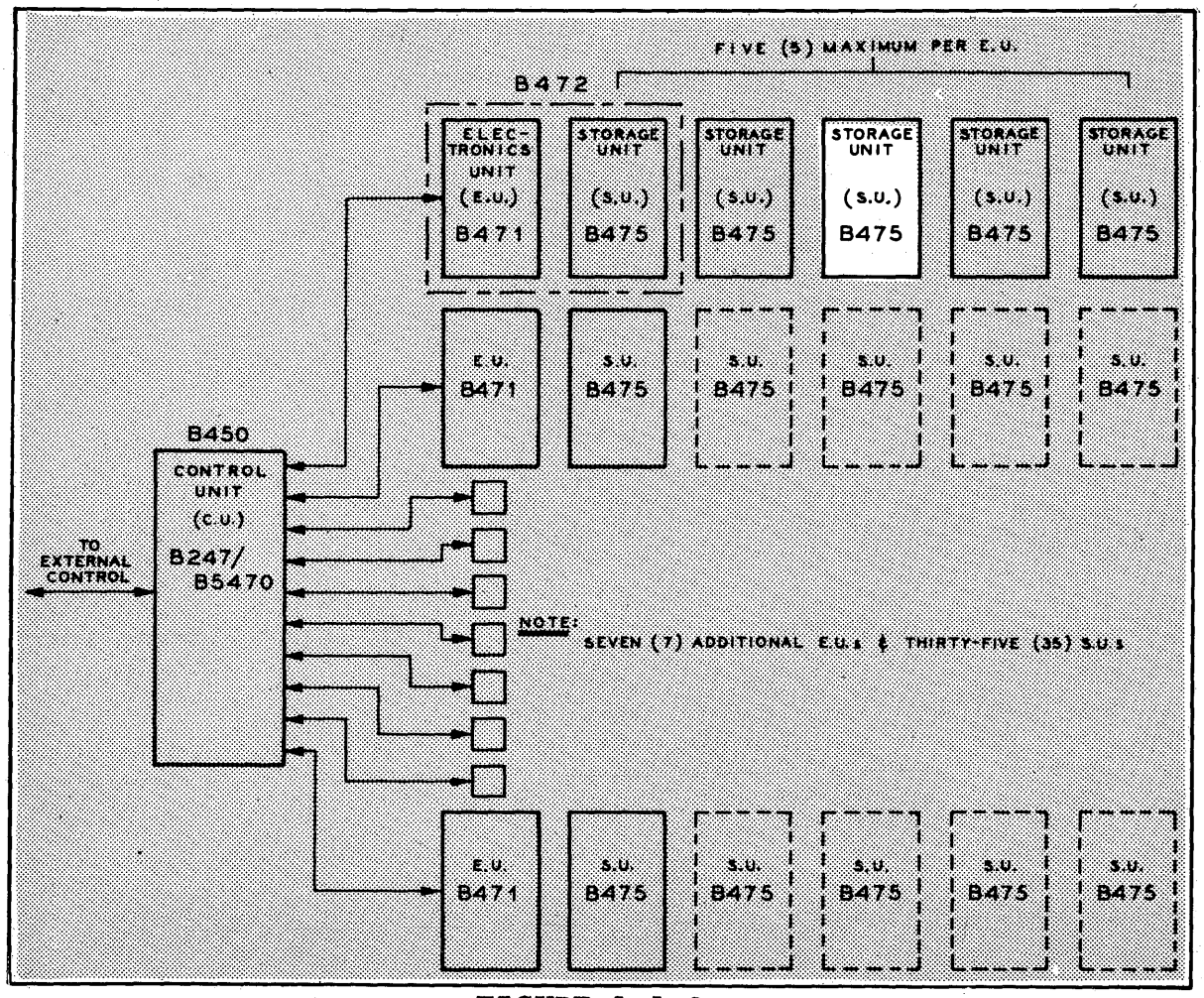

FIGURE 1.1-2
DISK FILE SUBSYSTEM

Figure 1.1-2 is a block diagram showing the location of the B475 Modules in the Subsystem.

Each Module or S.U. is capable of storing 9.6 million, six-bit alphanumeric characters of information. The information is recorded on four disks. Recorded information remains on the disk indefinitely until replaced by new data. There is one head per track, therefore, head positioning is not required. The information is stored on the disks in fixed record or segment lengths. Three different segment options are available. They are:

96	characters per segment	(12 words)
240	characters per segment	(30 words)
480	characters per segment	(60 words)

	MAX ALPHA CHARACTERS PER	MAX SEGMENTS PER	MAX DISKS PER	MAX STORAGE MODULES PER	MAX DISK FILE ELEC. UNITS PER	MAX DISK FILE CONT. UNIT PER
SEGMENT	96 240 480					
DISK	2,400,000	5,000 480 CHAR. 10,000 240 CHAR. 25,000 96 CHAR.				
MODULE	9,600,000	20,000 480 CHAR. 40,000 240 CHAR. 100,000 96 CHAR.	4			
ELEC. UNIT	48,000,000	100,000 480 CHAR. 200,000 240 CHAR. 500,000 96 CHAR.	20	5		
CONT. UNIT	480,000,000	1,000,000 480 CHAR. 2,000,000 240 CHAR. 5,000,000 96 CHAR.	200	50	10	
B200	480,000,000	1,000,000 480 CHAR. 2,000,000 240 CHAR. 5,000,000 96 CHAR.	200	50	10	1
B5500	960,000,000	2,000,000 480 CHAR. 4,000,000 240 CHAR. 10,000,000 96 CHAR.	400	100	20	2

FIGURE 1.1-3
STORAGE CAPACITY

All Modules connected to an E.U. must be of the same character option. Figure 1.1-3 is a table showing the storage capacity for various unit combinations. The disks rotate at 1500 rpm. With a read/write head for every track, any segment in the file can be accessed in an average time of 20 milliseconds.

1.2 EQUIPMENT SPECIFICATIONS

B475 STORAGE MODULES

Height ..... 53 inches
Length ..... 23 inches
Depth ..... 45 inches
Weight ..... 575 pounds

HEAT DISSIPATION

1•46 KVA 3800 BTU per hour

CLEARANCE FOR MAINTENANCE AND OPERATIONAL PURPOSES

Front ..... 4 feet
Rear ..... 1 1/2 feet
Left Side ... 0
Right Side .. 0

ENVIRONMENTAL

The operating environment for the disk file equipment is identical to the requirement for magnetic tape in terms of air temperature, relative humidity and cleanliness. These are Burroughs Class "C" environmental specifications:

Temperature 65° to 80° F.
Relative Humidity 40 - 60%.
Air Cleanliness - See page 15 of B200 Installation Planning Manual or page 4-1 of the B5500 Installation Planning Manual.

AC POWER REQUIREMENTS

The B475 receives all AC power from the B471 Electronics Unit. The Modules are started in sequence beginning with the Module closest to the E.U. A B475 will draw about 30 amperes at start up for approximately 35 seconds, dropping to 7.5 amperes at the 45 second interval. Additional B475's are sequenced on only after the one previous has come up to operational speed. The running current taken by five B475's is approximately 37.5 amperes. Maximum current for a B471 and five B475's would occur during the start up of the fifth B475. This would amount to approximately 63 amperes. The main circuit breaker in the B471 is rated at 70 amperes.

Power is supplied at 208VAC or 230VAC from two phases and a neutral.

DC POWER REQUIREMENTS

The following DC voltages are supplied to the Modules from the E.U.:

+20 volts
-20 volts
+12 volts
-12 volts
-4.5 volts

1.3 PHYSICAL DESCRIPTION

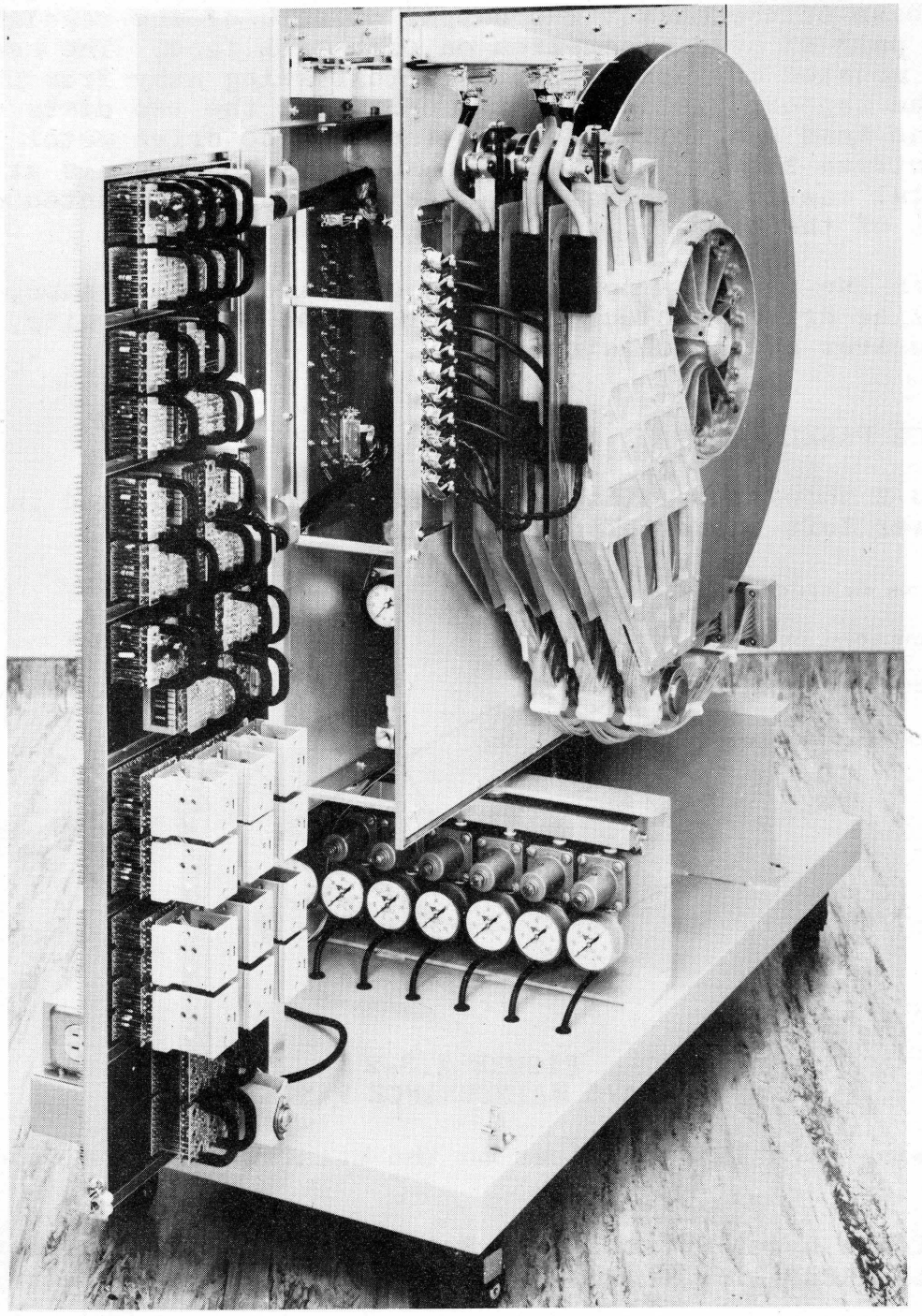

FIGURE 1.3-1
STORAGE UNIT

The B475 Storage Unit is shown in Figure 1.3-1 with all covers removed. The logic gate, Rack A, is shown open. The disks are mounted vertically, two on each side of the pedestal casting. Each pair of disks is normally enclosed in an air tight cover for purposes of cleanliness.

This cover has been removed on the right side. The seven air-pressure regulators, each with an air-pressure indicator, can be seen mounted near the base of the unit. The output of each of the regulators is sent to a pair of head assemblies on each disk face. The head assemblies are mounted on support castings that swing away from the disk faces. The support castings in the center of the two disks will contain the head assemblies for two faces. The drive motor is mounted between the two channel iron supports to which is attached the pedestal casting. A small Maintenance Panel is mounted on the left front of the base.

Included in the plug-ins in the logic gate are the pre-amps, write drivers, line drivers, clock generator, tachometer circuits, air solenoid driver and touch circuits.

MAINTENANCE PANEL

Figure 1.3-2 shows the Maintenance Panel which is located in the front, lower left corner of each Module.

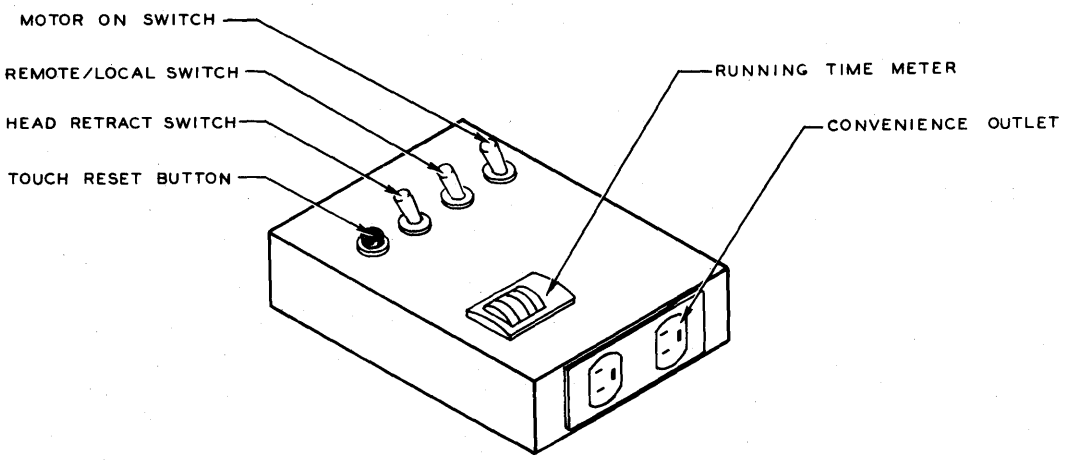

FIGURE 1.3-2
B475 MAINTENANCE PANEL

The following is a list of items on the Maintenance Panel and their uses:

1. Touch Reset Switch (Push Button) applies a false level on the RESL line to reset the touch and ready circuits.

2. Head Retract Switch removes ground from the air solenoid which will allow the head assemblies to retract.

3. Local/Remote Switch - In Local, this switch will cause SURL/ (Storage Unit Ready Level) in the E.U. to go true when this Module is addressed.

4. Motor On Switch - When off, prevents the Motor Relay and the air solenoid from being energized, but allows other units to be sequenced on.

5. Running Time Meter - This meter is connected directly across the motor and indicates AC power on in the Module.

6. Convenience Outlets - These outlets will be on any time the AC circuit breaker in the E.U. is closed.

Figure 1.3-3 shows a B471 and one B475 viewed from the front with the skins removed to show the physical location of many of the components.

Note the access plates located at the lower front of each bulkhead. The left access plate is visible through the disk window and the right access plate can be seen between the bulkheads.

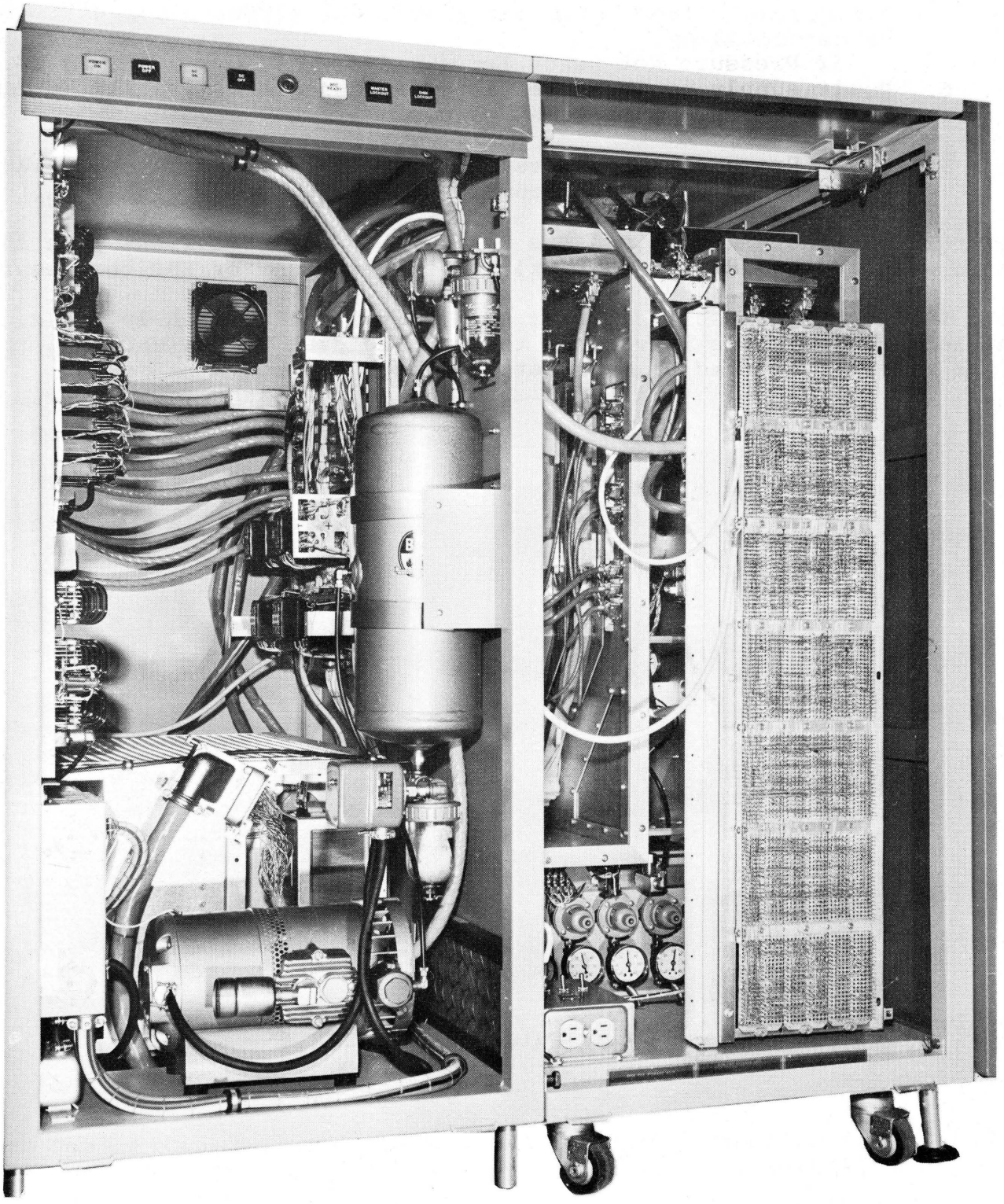

FIGURE 1.3-3
B471 AND B475

1.4 GLOSSARY

ANRL	Air Pressure Not Ready Level. Ground when the main trunk air supply to the heads is less than 45 psi; floats (true) when air pressure is at or over 45 psi.
APRL	Air Pressure Ready Level. Ground when the air supply to the heads is 45 psi or more; floats (true) when air pressure is less than 45 psi.
ASRL ASRL/	Address Read Level. The output levels from FF Line Drivers to the E.U. representing flux changes read from the address track.
BITL-01 BITL-02 BITL-03 BITL-04 BITL-05	Bit Pulse Level. Negative pulse from the clock generators in each of the five possible S.U.s connected together.
CAG-01	The output from this three-input AND gate is a series of negative pulses used to clock the set and reset of the Bit FF during a write operation.
CALP CALP/	Clock Address Lower Pulse. Input pulses to the lower face pre-amp caused by flux changes read from the selected lower face address track (CALP-12 or CALP-34).
CALP-D1 CALP/-D1 thru CALP-D4 CALP/-D4	Clock Address Lower Pulse - Disk 1 through Disk 4. Output of the selected address track head from Disk 1 through Disk 4. D1 and D2 are bussed on the "H" board and D3 and D4 are bussed on the "J" board.
CALP-12 CALP/-12	Clock Address Lower Pulse - Disk 1 and Disk 2. The bussed outputs from the "H" board.
CALP-34 CALP/-34	Clock Address Lower Pulse - Disk 3 and Disk 4. The bussed outputs from the "J" board.
CAUP CAUP/	Clock Address Upper Pulse (see CALP).
CAUP-D1 CAUP/-D1 thru CAUP-D4 CAUP/-D4	Clock Address Upper Pulse - Disk 1 through Disk 4 (see CALP-D1).
CAUP-12 CAUP/-12	Clock Address Upper Pulse - Disk 1 and Disk 2 (see CALP-12).

CAUP-34 CAUP/-34	Clock Address Upper Pulse - Disk 3 and Disk 4 (see CALP-34).
CBLP CBLP/	Clock Bit Lower Pulse. Input pulses to the lower face pre-amp caused by flux changes read from the selected lower face bit track.
CBLP-D1 CBLP/-D1 thru CBLP-D4 CBLP/-D4	Clock Bit Lower Pulse - Disk 1 through Disk 4.
CBLP-12 CBLP/-12	Clock Bit Lower Pulse - Disk 1 and Disk 2.
CBLP-34 CBLP/-34	Clock Bit Lower Pulse - Disk 3 and Disk 4.
CBUP CBUP/	Clock Bit Upper Pulse.
CBUP-D1 CBUP/-D1 thru CBUP-D4 CBUP/-D4	Clock Bit Upper Pulse - Disk 1 through Disk 4.
CBUP-12 CBUP/-12	Clock Bit Upper Pulse - Disk 1 and Disk 2.
CBUP-34 CBUP/-34	Clock Bit Upper Pulse - Disk 3 and Disk 4.
CC1L CC2L CC3L CC4L	Counter Clockwise 1 through 4 Level. Normally negative levels from the TUDL circuits enable the Ready Level, HFML/, and cause the pick of the Air Solenoid. If a touch is sensed from any counter-clockwise head, the respective level will become ground, HFML/ will be negative (Not Ready) and the Air Solenoid will be dropped.
CDSL	Correct Disk Speed Level. Negative level when the disks are rotating at the correct speed, 1500 rpm.
CHCL-11 CHCL-12 CHCL-13	Clock Head Center Tap Level - Disk 1, Zones 1, 2 and 3.
CHCL-21 thru CHCL-23	Clock Head Center Tap Level - Disk 2, Zones 1, 2 and 3.

CHCL-31 thru CHCL-33 — Clock Head Center Tap Level - Disk 3, Zones 1, 2 and 3.

CHCL-41 thru CHCL-43 — Clock Head Center Tap Level - Disk 4, Zones 1, 2 and 3.

CS1L/ CS2L/ — Characters per Segment Levels. Indicate the option:

CS1L/ ground and CS2L/ negative - 480 characters per seg.
CS1L/ negative and CS2L/ ground - 240 characters per seg.
CS1L/ ground and CS2L/ ground - 96 characters per seg.

CW1L CW2L CW3L CW4L — Clockwise 1 through 4 Level. Normally negative to enable the Ready Level and to pick the Air Solenoid (see CC1L).

DA0L DA1L — Differentiated Address Level. The output pulses from the Address Differentiator corresponding to flux changes read from the address track.

DBØL — Differentiated Bit Level. The output pulses from the Bit Differentiator corresponding to every flux change read from the bit track.

DFSL/ DFSS — Disk Face Select Level and Disk Face Select Switch. These levels are always in the opposite state. DFSL/ is negative to select the output of the lower face clock pre-amps corresponding to the selection of information tracks 00=>49. DFSS is negative to select the output of the upper face clock pre-amps corresponding to the selection of information tracks 50=>99.

DISC-01 DISC-01/ thru DISC-04 DISC-04/ — Disk Select Levels. The prime levels are received from the E.U. and are ground to select a disk. The corresponding switched levels are negative to select clock head center taps.

DI0L DI1L — Differentiated Information Level. The output pulses from the Information Differentiator corresponding to flux changes read from the information track.

GSSL — Gain Select Level. When negative from the E.U., selects low gain in the Information Gain Controlled Sense Amp (AMGC).

HFML-01/ thru HFML-05/ — Storage Unit Ready Level (originally, Heads Flying, Motor Up to Speed). Positive level indicates S.U. is:

a. Ready - Disks up to speed, no touch circuits triggered, air pressure up, or
b. S.U. is in LOCAL and not designated.

HRWL-11 HRWL/-11 thru HRWL-43 HRWL/-43	Head Read Write Lines - Disk 1, Zones 1, 2 and 3 through Disk 4, Zones 1, 2 and 3. During read, the lines represent the one/zero output pulses from the selected information head. During write, the lines represent the one/zero output from the Bit FF to the selected information head.
HSDL-00 thru HSDL-99	Head Select Drive Level. Information Head 00 through 99. Level is positive (+12V) to select.
ICFF	Interlace Control FF. Negative level during an active word.
IRAL IRAL/	Information Read Level. The output levels from FF Line Drivers to the E.U. representing flux changes read from the information track.
IXHS/	Index Holdover Switch. Negative level used to reset the Address Read FF during dead space.
LØCL	Local Level. Ground when LOCAL-REMOTE switch is in REMOTE.
MAGP	Magnetic Pick-up. Sine wave generated by a hole in the drive shaft passing under an inductive magnetic pick-up head.
MAGP-SH	Magnetic Pick-up Shield. Grounded shield from pick-up head.
MØ1L MØ2L MØ3L MØ4L MØ5L	Module Select Levels. Negative level from the E.U. to designate a Module.
NCL-1-GND NCL-2-GND	Noise Clip Level 1 and 2 - Ground.
PA0L PA1L	Pre-Amp Address Level. The bussed output levels from the two Word Mark/Address pre-amps (lower and upper).
PB0L PB1L	Pre-Amp Bit Level. The bussed output levels from the two Bit track pre-amps (lower and upper).
PI0L PI1L	Pre-Amp Information Level. The bussed output levels from the three information pre-amps (Zones 1, 2 and 3).
RESL	Reset Level. Ground level when the Reset switch is depressed to reset any "latched" touch circuit.
SCTL	Spare Center Tap Level. Ground level to back bias the spare heads.

SMIL — Start Motor Input Level. Ground level from the E.U. to permit the pick of MPR (Motor Power Relay).

SMØL — Start Motor Output Level. After motor is nearly up to speed, MSR (Motor Started Relay) picks and in turn picks NMSR (Next Motor Start Relay). This sends a ground level back through the E.U. to the next Module to permit it to start.

SØLL — Solenoid Level. Ground level from the solenoid driver when no touch circuits have been activated and the disks are up to speed. Will permit the pick of the Air Solenoid to actuate the heads.

SPFD — Space FF Driver Level. Negative level from the E.U. when SPFF is set.

SU0
SU1 — Storage Unit Level. The output levels from the Bit FF which cause a zero or one flux change to be written.

SU1FW
SU1FW/ — Storage Unit 1 Write FF Level. The output levels from the E.U. which set or reset the Bit FF to cause a zero or one to be written.

TD1L
TD2L
TD3L
TD4L
TD5L — Threshold Detect Levels. Negative pulses from any Module to the E.U. to set the Gain Select circuit for low gain.

TØCL — Touch Circuit Level (misleading name). The output level from one of two cross-coupled switches which create the Ready level to the E.U. TØCL is true when the Module is Ready, Air Pressure Ready and the unit is in REMOTE.

T1CC
T1CW
T2CC
T2CW
T3CC
T3CW
T4CC
T4CW — The common touch pin circuits for Disks 1 through 4 clockwise and counter-clockwise. Ground level, when a head touches, will latch the appropriate TUDL circuit.

WCSL — Write Current Select Level. During the active word of a Write operation, supplies 150 ma at a negative level to the selected Write Driver.

WRSD/
WRSS — Write Select Level and Write Select Level Switched. The ground level from the E.U., for a Write operation, is switched to supply a negative input level to WCSL and CAG 101.

ZØ1L-01 ZØ1L-01/ thru ZØ3L-01 ZØ3L-01/	Zone Select Levels. The prime lines from the E.U. are ground and are switched to select a zone.
Z1RP Z1RP/ thru Z3RP Z3RP/	Zone Read Pulses. The output levels from both sides of all the information heads in a zone.

Principles of Operation

✓INDEX - SECTION II

✓Changes or additions since last issue.

2.1 INFORMATION ORGANIZATION

Information is recorded on the disks serially by bit, character and word. The recording method is non-return to zero where a magnetic flux change is written only when information changes from a one to a zero or from a zero to a one. Information is recorded serially in 54-bit words, separated by a two-bit space. Figure 2.1-1 shows the word format.

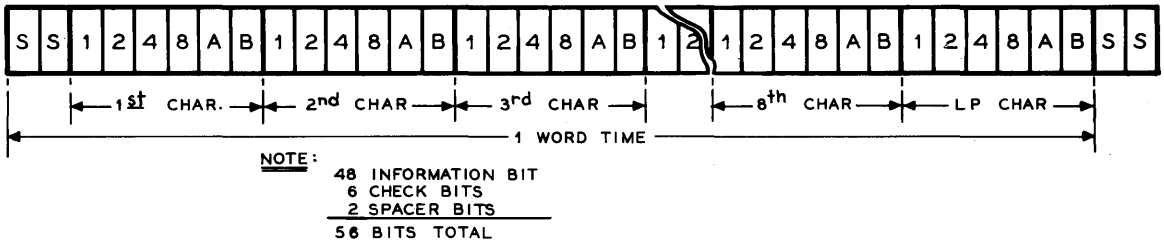

FIGURE 2.1-1
WORD FORMAT

The 56-bit word time consists of eight (six bit) alphanumeric characters plus one (six bit) check character and two space bits. The check character is the odd longitudinal parity for the word. The space bits are used to allow the write drivers to be turned on and off without destroying information characters.

Information is organized in three concentric areas called zones. Each zone is separately clocked because of the change in surface speed from zone 1 to zone 3. Zone 1 is nearest the hub. The clock tracks for all three zones are located between zones 2 and 3. The clock frequencies are such that the average packing density in each zone is approximately 1000 bits per inch. With this packing density, the maximum bit rate is approximately 1.8 mc. This is a character rate of approximately 300 kc. For further details of the disk layout, refer to Sections 3.6 and 4.3.

The minimum information transfer operation involves one record or segment. The segment size is a customer option.

The Character per Segment Levels, CS1L/ and CS2L/ are sent through the E.U. to the D.F.C.U. to denote the segment option and produce the correct logic gating to access the required areas on the disk. The option is determined as follows:

CS1L/ false and CS2L/ false indicates 96 characters per segment.

CS1L/ true and CS2L/ false indicates 240 characters per segment.

CS1L/ false and CS2L/ true indicates 480 characters per segment.

2.2 CLOCK TRACKS

There is a word mark/address track and a bit track for each zone on each disk face. Recorded in the address track are:

1. A flux change to generate a pulse at the beginning of each word.

2. A three character address preceding the start of each segment. The word mark pulse is coincident with the first space bit of the word. The three characters of an address coincide with the first three characters of an information word. The bit track has 56 pulses for each word pulse on the disk. Figure 2.2-1 is typical of address format.

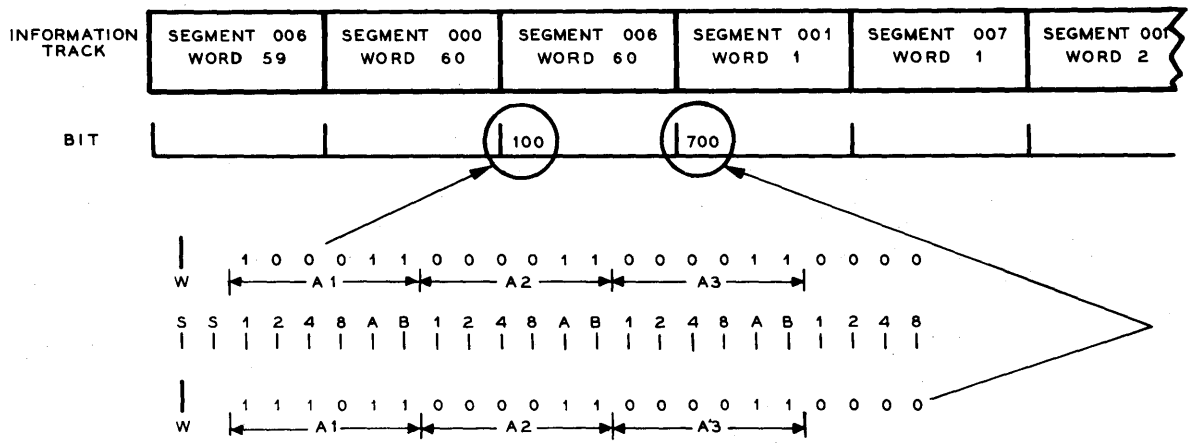

FIGURE 2.2-1
WORD MARK/ADDRESS TRACK

Addresses are recorded least significant digit first with the A and B bits written as ones. The A and B bits are required to enable a zero address character to be recognized.

2.3 STORAGE UNIT OPERATION

Figure 2.3-1 is a block diagram of the S.U. showing the association of the read/write circuits and head select circuits. The information heads are grouped in 12 sets of 100 heads. Each set is connected to a write driver/select circuit. The 100 information head select lines are connected in parallel to the center taps of the 100 heads in each head set. An information head is accessed by enabling one of the 100 information head select lines and one of the 12 write driver/select circuits. The clock heads are accessed by enabling the center taps to the two bit heads and two address heads of a disk and zone and selecting the output from one face.

Normally the center tap lines are held at a negative level with respect to the head set output. This bias level is such that all of the head switching diodes are reverse biased and in the nonconducting state; therefore, neither reading nor writing can take place with any head. To select one of the heads, the bias level on the head select line is changed in the direction to forward bias the two diodes associated with the desired head and the two diodes common to the head assembly desired. In the forward biased condition, the head switching diodes will pass current and permit reading or writing with the designated head. All of the other head switching diodes are still reverse biased; therefore, only one head in the head set is selected.

Since the 100 head select lines are common to all head sets, one head in each head set will be selected along with the desired head. However, only one read amplifier and write driver select circuit is activated; therefore, the output from the undesired head sets will be ignored.

The head switching diodes for the unselected heads, even when reverse biased, have a small capacity which tends to pass noise signals. The seemingly extra diodes for each head assembly prevent any noise signal problems by placing a small capacity in series with the capacity of the head switching diodes, thereby reducing the total effective capacity.

In order to perform a Read or Write operation in one S.U., the following must be accomplished:

1. One bit and one address track must be selected out of a possible 24 bit tracks and 24 address tracks.

2. One information track must be selected out of 1200.

3. The read or write circuits must handle the information transfer from or to the head.

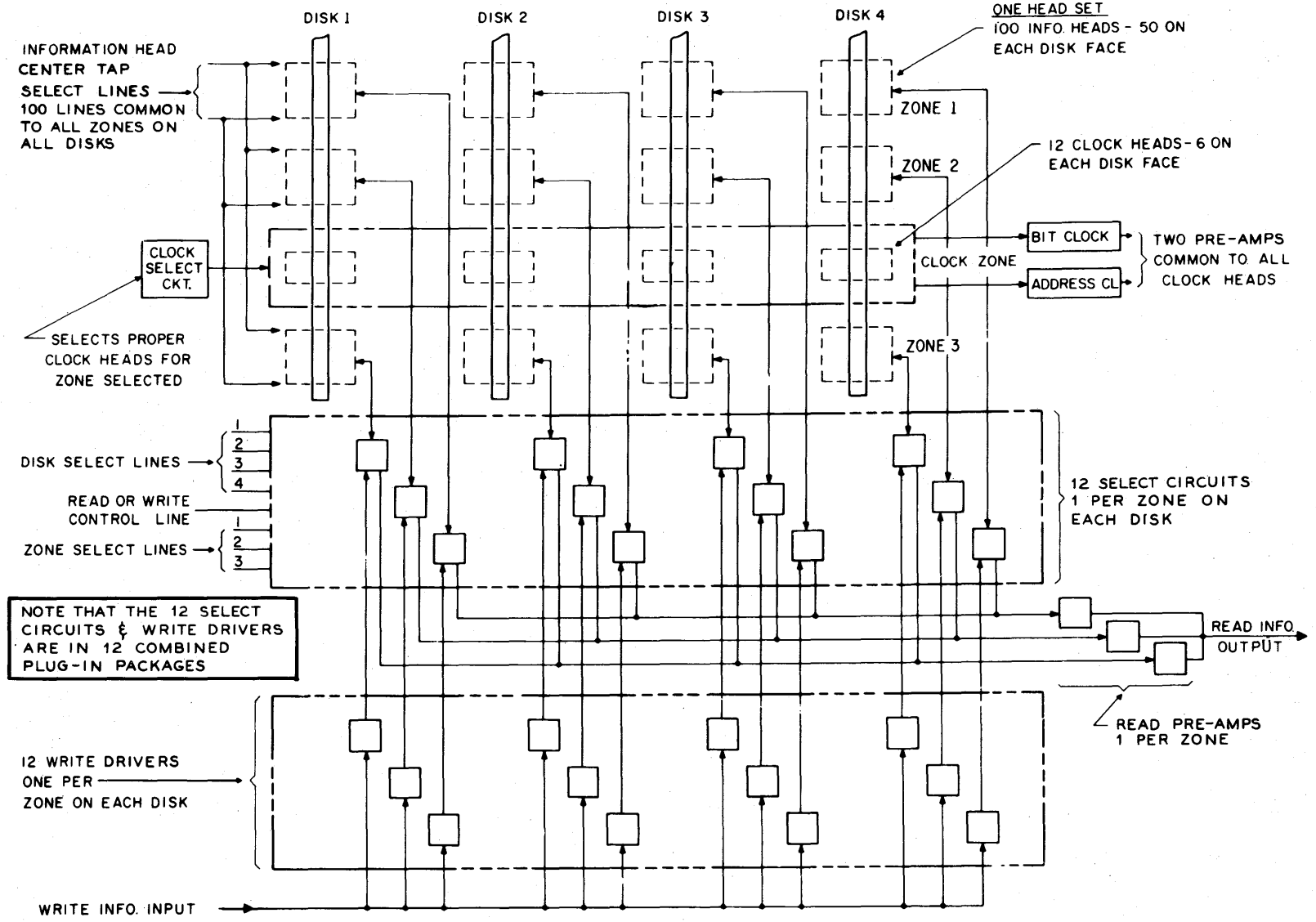

FIGURE 2.3-1
STORAGE UNIT BLOCK DIAGRAM

BIT AND WORD ADDRESS SELECTION

The logic levels from the E.U. to the S.U.'s are sent as shown in Figure 2.3-2. The Zone Levels (ZØ1L/, ZØ2L/ and ZØ3L/) together with the Disk Levels (DISK-01 through DISK-04) produce 12 levels called Clock Center Tap select levels (CHCL-nn). The number following each of these levels (nn) is used to indicate the disk and zone, the first digit being the disk and the second digit the zone. For example, CHCL-13 would be connected to the Clock Center taps for disk 1, zone 3. Each CHCL-nn is connected to the four center taps of the clock heads for that zone on that disk (one bit and one address on each face).

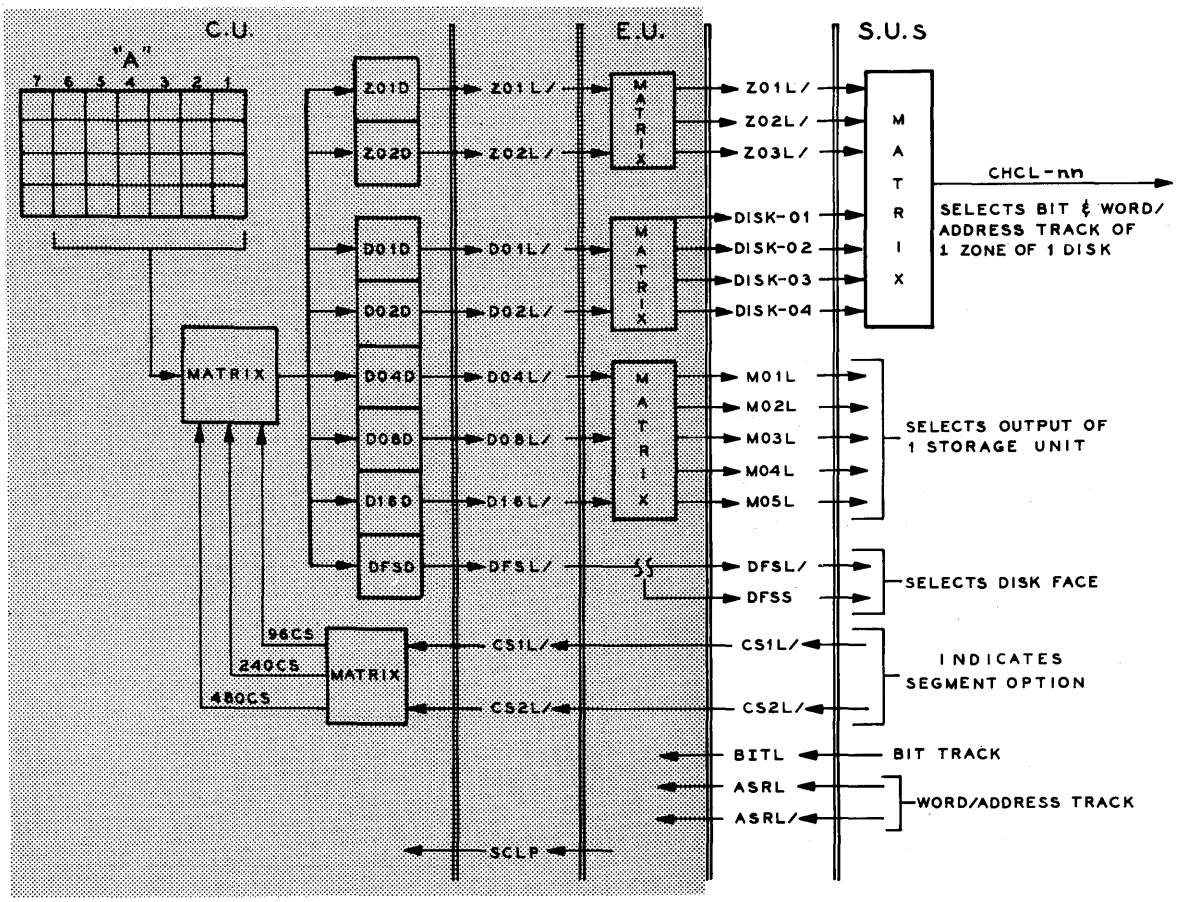

FIGURE 2.3-2
BIT AND WORD/ADDRESS SELECTION

The outputs of all the similar bit heads and the outputs of all the similar address heads are connected in parallel to the inputs of two pre-amplifiers. That is, all lower face bit track heads are connected to the CBLP pre-amp, all upper face address track heads are connected to the CAUP pre-amp and so on. The outputs of the pre-amps are enabled by DFSL/ and DFSS.

INFORMATION TRACK SELECTION

One of the 100 HSDL's will enable the center taps of one track in each zone of one face of all four disks (12 heads). One of the 12 write driver select circuits will select the output of the enabled head in a set of 100. The output of the head (Read operation) goes to the selected zone pre-amp. The input to the head (Write operation) comes from the Write Driver.

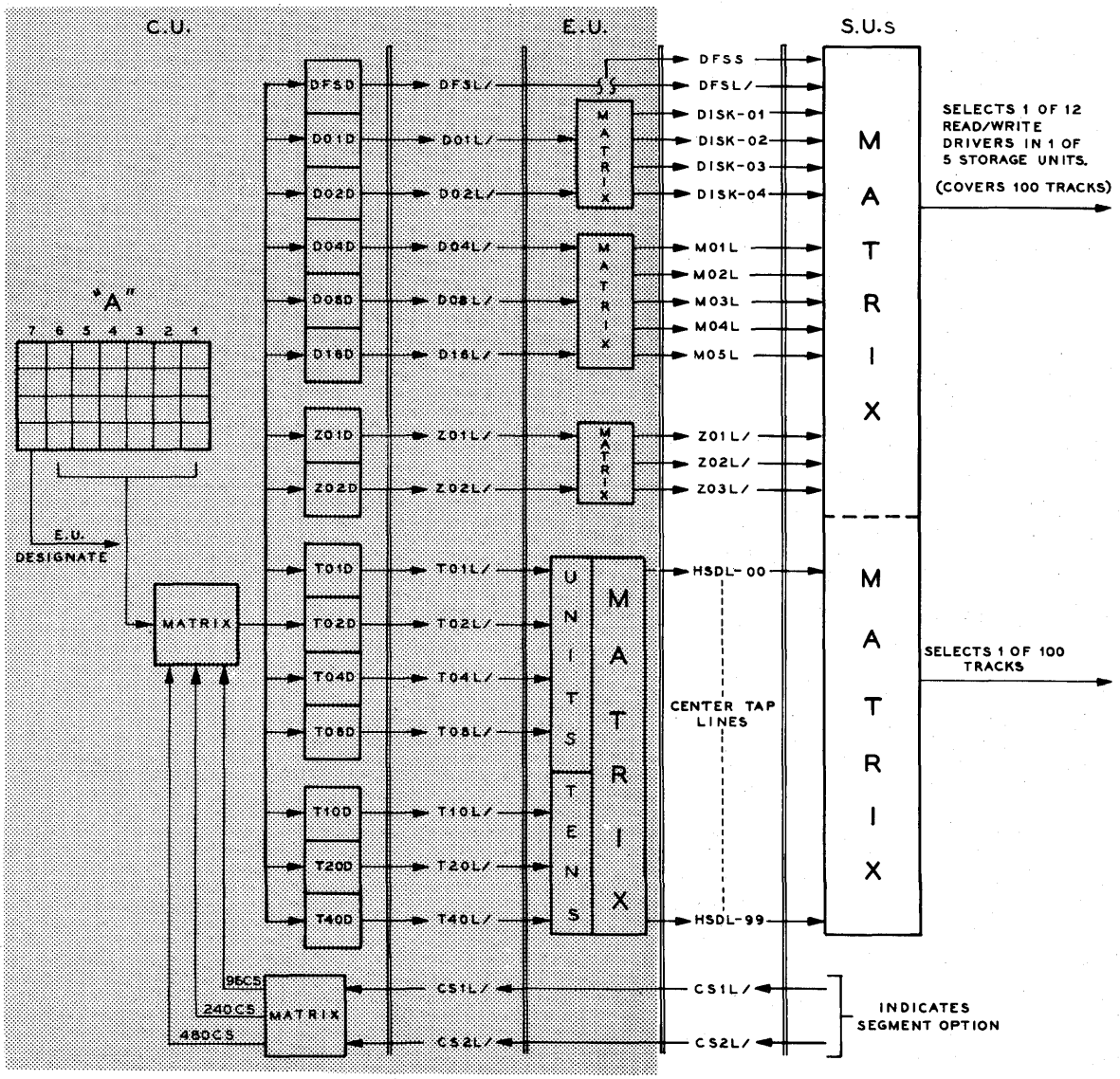

FIGURE 2.3-3
INFORMATION TRACK SELECTION

SEGMENT ADDRESSES

Segment addresses are read from the selected address track and transmitted to the E.U. serially by bit. The D.F.C.U. compares segment addresses until coincidence is found and then a read or write cycle is initiated.

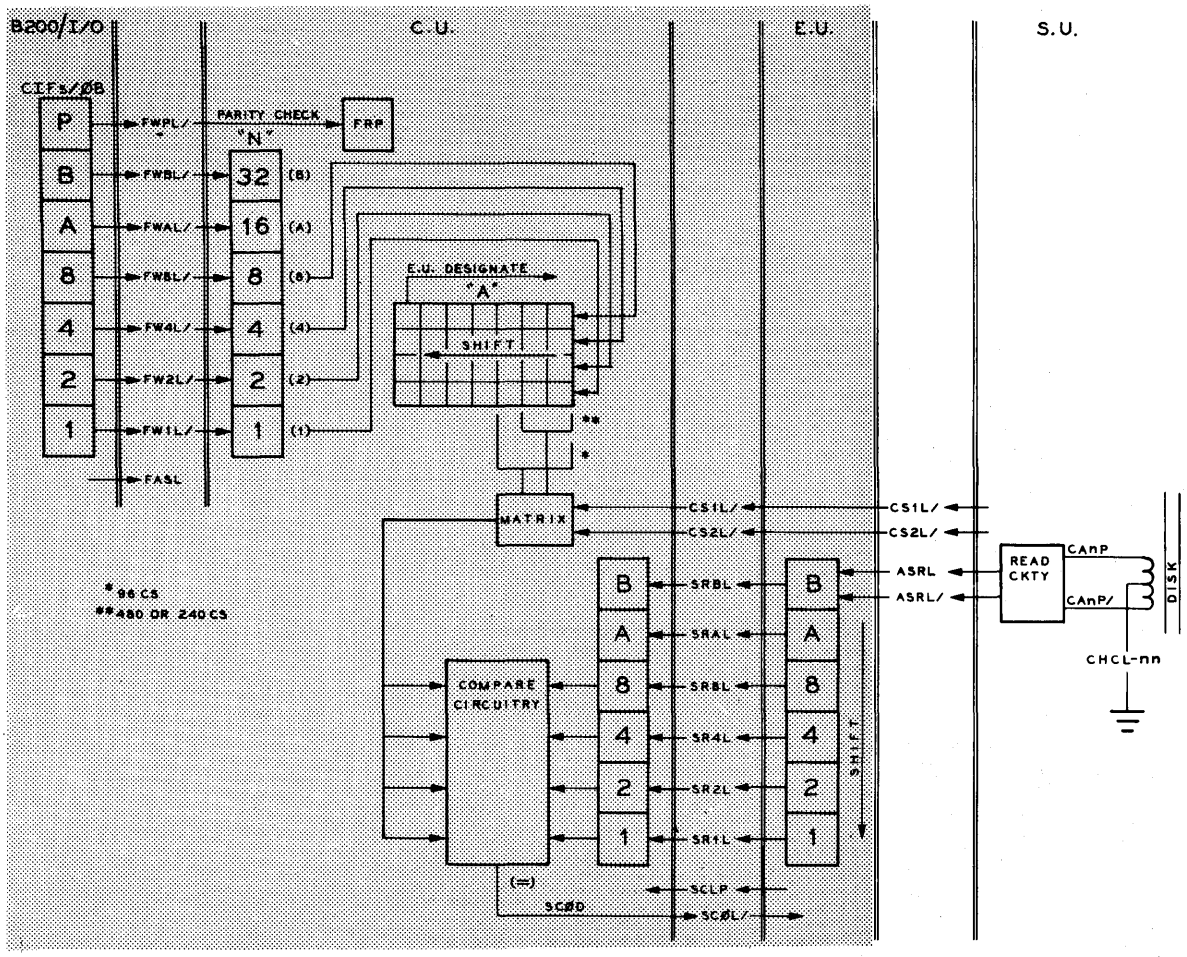

FIGURE 2.3-4
SEGMENT ADDRESS FLOW

INFORMATION FLOW

The word pulse following coincidence will set the Action Flip-Flop (ACFF) and Interlace Control Flip-Flop (ICFF) in the E.U. The ACFF determines when the operation will be terminated. ICFF will permit the active word to be read or written and ICFF/ permits the E.U. to scan for a segment address during the inactive word. ICFF is complemented by each WØMP.

During a Write operation, a character is transmitted serially by bit from the E.U. The Write Current Control circuit is turned on in the selected Module with ICFF and WRSD (Storage Write level). With Write Control on, the bit stored in SU1Fw is shifted into the Bit FF (SUF). The Bit FF controls the Write Driver. The character is recorded serially by bit by the previously selected information head. This process is repeated for nine characters (eight information and one check character) after which the WØMP from the Word/Address clock track turns off ICFF to inhibit writing the next word. The next WØMP sets ICFF and another nine-character word is written. This process continues

until an address is read when ICFF is off. If ACFF is reset, the operation is complete; otherwise writing continues as before until the required number of segments have been written.

The Read operation, as far as the Module is concerned, begins as soon as the heads are selected. A Write Driver is selected during a Read operation, but Write Current Control is not enabled so writing is inhibited. Read signals from the head are gated to the selected pre-amp. The output of the pre-amp and associated read circuitry are the Information Read levels (IRAL and IRAL/).

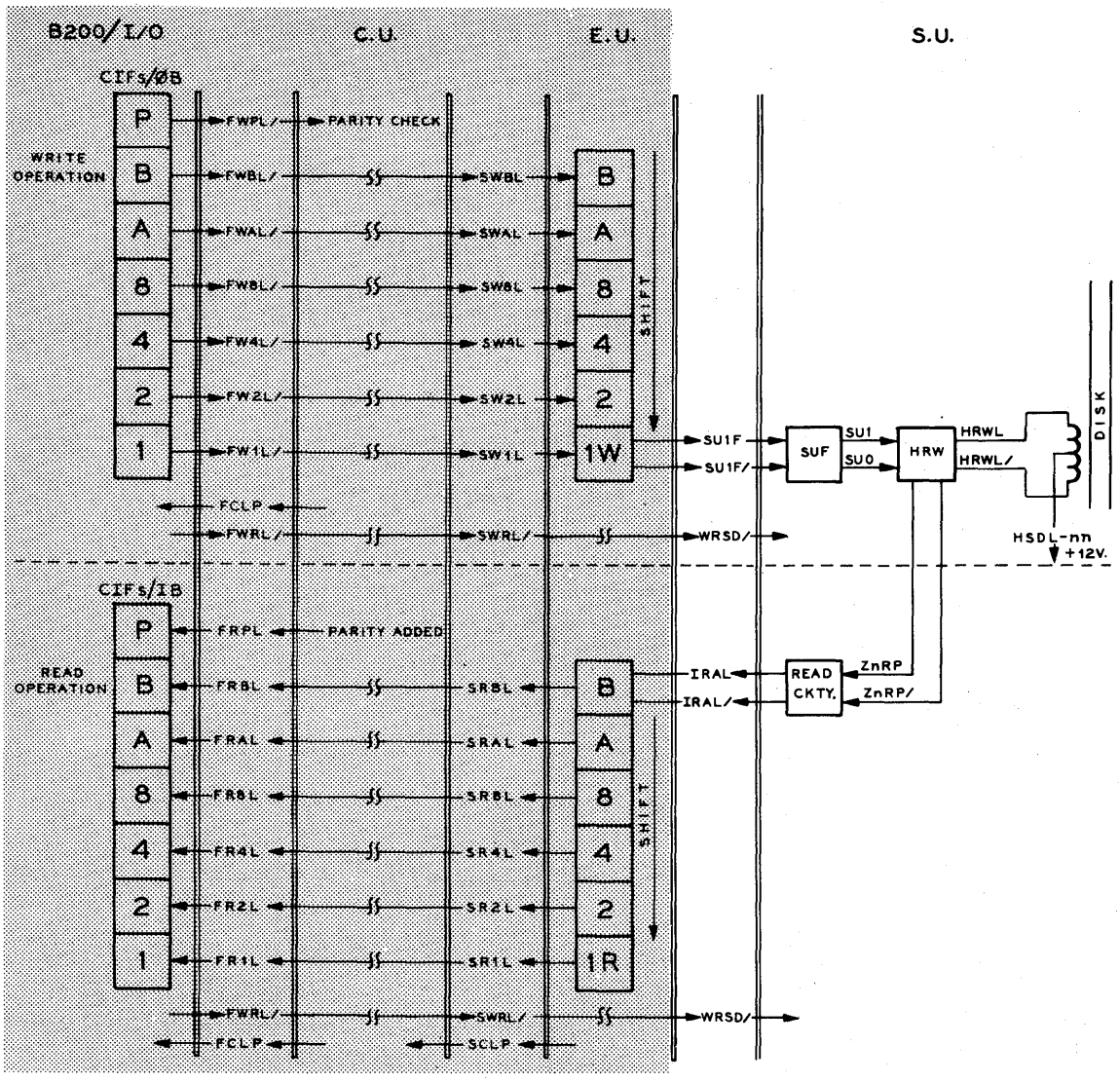

FIGURE 2.3-5
INFORMATION FLOW

Functional Description - Electronic

✓INDEX - SECTION III

✓Changes or additions since last issue.

3.1 CABLING

All logic and power cables internal to, leaving from, or coming to a Module are shown on pin cross-reference tables. See Figure 3.1-1.

LOGIC CABLES INTER-UNIT

TABLE 3.1-1

*E.U.	**MOD.	LEVEL	MOD.	*E.U.	**MOD.	LEVEL	MOD.	*E.U.	**MOD.	LEVEL	MOD.
ACB0A7	GAJ5		GAJ4	ACB0N2	GAL5		GAL4	ACB0N7	GAK5		GAK4
A5	19	HSDL-90	1	N0	19	HSDL-08	1	19	N5	HSDL-13	1
B5	18	HSDL-88	2	P0	18	HSDL-06	2	18	P5	HSDL-11	2
C5	17	HSDL-74	3	R0	17	HSDL-12	3	17	R5	HSDL-33	3
D5	16	HSDL-98	4	S0	16	HSDL-00	4	16	S5	HSDL-05	4
E5	15	HSDL-96	5	T0	15	HSDL-26	5	15	T5	HSDL-03	5
F5	14	HSDL-89	6	U0	14	HSDL-16	6	14	U5	HSDL-29	6
H5	13	HSDL-67	7	V0	13	HSDL-32	7	13	V5	HSDL-45	7
J5	12	HSDL-69	8	W0	12	HSDL-34	8	12	W5	HSDL-47	8
K5	11	HSDL-85	9	X0	11	HSDL-20	9	11	X5	HSDL-25	9
A6	10	HSDL-59	10	N1	10	HSDL-40	10	10	N6	HSDL-60	10
B6	9	HSDL-61	11	P1	9	HSDL-42	11	9	P6	HSDL-54	11
C6	8	HSDL-81	12	R1	8	HSDL-24	12	8	R6	HSDL-52	12
D6	7	HSDL-51	13	S1	7	HSDL-48	13	7	S6	HSDL-64	13
E6	6	HSDL-53	14	T1	6	HSDL-23	14	6	T6	HSDL-78	14
F6	5	HSDL-77	15	U1	5	HSDL-39	15	5	U6	HSDL-80	15
H6	4	HSDL-99	16	V1	4	HSDL-17	16	4	V6	HSDL-68	16
J6	3	HSDL-97	17	W1	3	HSDL-15	17	3	W6	HSDL-86	17
A7	2	GND-03	18	N2	2	GND-01	18	2	N7	GND-02	18
B7	1	GND-03	19	P2	1	GND-01	19	1	P7	GND-02	19
A8	37	HSDL-72	20	N3	37	HSDL-10	20	37	N8	HSDL-35	20
B8	36	HSDL-94	21	P3	36	HSDL-04	21	36	P8	HSDL-09	21
C8	35	HSDL-92	22	R3	35	HSDL-02	22	35	R8	HSDL-07	22
D8	34	HSDL-91	23	S3	34	HSDL-14	23	34	S8	HSDL-31	23
E8	33	HSDL-71	24	T3	33	HSDL-28	24	33	T8	HSDL-01	24
F8	32	HSDL-73	25	U3	32	HSDL-30	25	32	U8	HSDL-43	25
H8	31	HSDL-87	26	V3	31	HSDL-18	26	31	V8	HSDL-27	26
J8	30	HSDL-63	27	W3	30	HSDL-36	27	30	W8	HSDL-49	27
K8	29	HSDL-65	28	X3	29	HSDL-38	28	29	X8	HSDL-58	28
A9	28	HSDL-83	29	N4	28	HSDL-22	29	28	N9	HSDL-56	29
B9	27	HSDL-55	30	P4	27	HSDL-44	30	27	P9	HSDL-62	30
C9	26	HSDL-57	31	R4	26	HSDL-46	31	26	R9	HSDL-50	31
D9	25	HSDL-79	32	S4	25	HSDL-41	32	25	S9	HSDL-76	32
E9	24	HSDL-95	33	T4	24	HSDL-21	33	24	T9	HSDL-66	33
F9	23	HSDL-93	34	U4	23	HSDL-19	34	23	U9	HSDL-82	34
J9	22	HSDL-75	35	W4	22	HSDL-37	35	22	W9	HSDL-84	35
L9	21	SPARE-2	36	X4	21	SPARE-1	36	21	X9	HSDL-70	36
L7	20	GND-03	37	X2	20	GND-01	37	20	X7	GND-02	37

*3 Center Tap Cables from E.U. to 1st Module.

ACB0A7
ACB0N2 — Quad Connectors in E.U. Logic Gate
ACB0N7

**3 Center Tap Cables from a Module to the next Module.

GAJ5
GAL5 — Connectors - Rack G Storage Module.
GAK5

Refer to Table 3.1-1.

ACB0N7 .... GAK4
ACB0N2 .... GAL4
ACB0A7 .... GAJ4
→ Information center tap select cables from Electronic Unit logic gate to center tap distribution board in Module 1.

GAJ5 ..... GAJ4
GAK5 ..... GAK4
GAL5 ..... GAL4
→ Information center tap select cables from the center tap distribution board of a Module to the center tap distribution board of the next Module.

Refer to Figure 3.1-2.

AAB0N2 .... AAB0A2 → Logic cable from the Electronic Unit logic gate to first Module.

LOGIC CABLES INTERNAL

Refer to Table 3.1-2.

GAK0 ..... Rack L
GAJ1 ..... Rack M
GAK2 ..... Rack N
→ Information center tap select cables from center tap distribution board to Information Heads on Head Support boards. (Disks 1 & 2.)

Refer to Table 3.1-3.

GAK7 ..... Rack P
GAJ8 ..... Rack R
GAK9 ..... Rack S
→ Information center tap select cables from center tap distribution board to Information Heads on Head Support boards. (Disks 3 & 4.)

Refer to Tables 3.1-4 & 3.1-5.

Rack L HAU0
Rack M HAV0
Rack N HAW0
→ Information and Touch circuit output cables from Head Support boards (Disks 1 & 2) to interconnection board H.

Refer to Tables 3.1-6 & 3.1-7.

Rack P JAU0
Rack R JAV0
Rack S JAW0
→ Information and Touch circuit output cables from Head Support boards (Disks 3 & 4) to interconnection board J.

TABLE 3.1-2

RACK G TO RACK L				RACK G TO RACK M				RACK G TO RACK N			
GAK0	LEVEL	INFORMATION HEADS		GAJ1	LEVEL	INFORMATION HEADS		GAK2	LEVEL	INFORMATION HEADS	
PIN	HSDL	PIN		PIN	HSDL	PIN		PIN	HSDL	PIN	
3	01-1	5		3	51-12	5		3	01-2	5	
20	03-1	6		20	53-12	6		20	03-2	6	
4	05-1	7		4	55-12	7		4	05-2	7	
21	07-1	8	1 (LAN7)	21	57-12	8	1 (MAN7, MAM7)	21	07-2	8	1 (NAM7)
5	09-1	9		5	59-12	9		5	09-2	9	
22	11-1	10	5 (LAL7)	22	61-12	10	5 (MAL7, MAK7)	22	11-2	10	5 (NAK7)
6	13-1	11	11 (LAJ3)	6	63-12	11	11 (MAJ3, MAJ2)	6	13-2	11	11 (NAJ2)
23	15-1	12		23	65-12	12		23	15-2	12	
7	17-1	13		7	67-12	13		7	17-2	13	
24	19-1	14		24	69-12	14		24	19-2	14	
8	21-1	15		8	71-12	15		8	21-2	15	
25	23-1	16		25	73-12	16		25	23-2	16	
15	00-1	4		15	50-12	4		15	00-2	4	
32	02-1	5		32	52-12	5		32	02-2	5	
16	04-1	6		16	54-12	6		16	04-2	6	
33	06-1	7		33	56-12	7		33	06-2	7	
17	08-1	8	2 (LCJ1)	17	58-12	8	2 (MCJ1, MCJ0)	17	08-2	8	2 (NCJ0)
50	10-1	9	8 (LBJ7)	50	60-12	9	8 (MBJ7, MBJ6)	50	10-2	9	8 (NBJ6)
49	12-1	10		49	62-12	10		49	12-2	10	
48	14-1	11	12 (LBJ5)	48	64-12	11	12 (MBJ5, MBJ4)	48	14-2	11	12 (NBJ4)
47	16-1	12		47	66-12	12		47	16-2	12	
46	18-1	13		46	68-12	13		46	18-2	13	
45	20-1	14		45	70-12	14		45	20-2	14	
44	22-1	15		44	72-12	15		44	22-2	15	
43	24-1	16		43	74-12	16		43	24-2	16	
34	25-1	4		34	75-12	4		34	25-2	4	
35	27-1	5		35	77-12	5		35	27-2	5	
36	29-1	6		36	79-12	6		36	29-2	6	
37	31-1	7		37	81-12	7		37	31-2	7	
38	33-1	8	3 (LAJ7)	38	83-12	8	3 MAJ7, MAJ6)	38	33-2	8	3 (NAJ6)
39	35-1	9	7 (LAJ5)	39	85-12	9	7 (MAJ5, MAJ4)	39	35-2	9	7 (NAJ4)
40	37-1	10		40	87-12	10		40	37-2	10	
41	39-1	11	13 (LAJ1)	41	89-12	11	13(MAJ1, MAJ0)	41	39-2	11	13 (NAJ0)
42	41-1	12		42	91-12	12		42	41-2	12	
19	43-1	13		19	93-12	13		19	43-2	13	
2	45-1	14		2	95-12	14		2	45-2	14	
18	47-1	15		18	97-12	15		18	47-2	15	
1	49-1	16		1	99-12	16		1	49-2	16	
31	26-1	5		31	76-12	5		31	26-2	5	
14	28-1	6		14	78-12	6		14	28-2	6	
30	30-1	7		30	80-12	7		30	30-2	7	
13	32-1	8	4 (LBJ9)	13	82-12	8	4 (MBJ9, MBJ8)	13	32-2	8	4 (NBJ8)
29	34-1	9	6 (LBJ3)	29	84-12	9	6 (MBJ3, MBJ2)	29	34-2	9	6 (NBJ2)
12	36-1	10		12	86-12	10	14 (MBJ1, MBJ0)	12	36-2	10	
28	38-1	11	14 (LBJ1)	28	88-12	11		28	38-2	11	14 (NBJ0)
11	40-1	12		11	90-12	12		11	40-2	12	
27	42-1	13		27	92-12	13		27	42-2	13	
10	44-1	14		10	94-12	14		10	44-2	14	
26	46-1	15		26	96-12	15		26	46-2	15	
9	48-1	16		9	98-12	16		9	48-2	16	

INFORMATION CENTER TAP INPUTS FOR DISKS 1 & 2.

TABLE 3.1-3

RACK G TO RACK P				RACK G TO RACK R				RACK G TO RACK S			
GAK7	LEVEL	INFORMATION HEADS		GAJ8	LEVEL	INFORMATION HEADS		GAK9	LEVEL	INFORMATION HEADS	
PIN	HSDL	PIN		PIN	HSDL	PIN		PIN	HSDL	PIN	
36	01-3	5		36	51-34	5		36	01-4	5	
20	03-3	6		20	53-34	6		20	03-4	6	
37	05-3	7		37	55-34	7		37	05-4	7	
21	07-3	8	1 (PAN7)	21	57-34	8	1 (RAN7, RAM7)	21	07-4	8	1 (SAM7)
38	09-3	9		38	59-34	9	5 (RAL7, RAK7)	38	09-4	9	5 (SAK7)
22	11-3	10	5 (PAL7)	22	61-34	10		22	11-4	10	
39	13-3	11	11 (PAJ3)	39	63-34	11	11 (RAJ3, RAJ2)	39	13-4	11	11 (SAJ2)
23	15-3	12		23	65-34	12		23	15-4	12	
40	17-3	13		40	67-34	13		40	17-4	13	
24	19-3	14		24	69-34	14		24	19-4	14	
41	21-3	15		41	71-34	15		41	21-4	15	
25	23-3	16		25	73-34	16		25	23-4	16	
48	00-3	4		48	50-34	4		48	00-4	4	
32	02-3	5		32	52-34	5		32	02-4	5	
49	04-3	6		49	54-34	6		49	04-4	6	
33	06-3	7		33	56-34	7		33	06-4	7	
50	08-3	8	2 (PCJ1)	50	58-34	8	2 (RCJ1, RCJ0)	50	08-4	8	2 (SCJ0)
17	10-3	9	8 (PBJ7)	17	60-34	9	8 (RBJ7, RBJ6)	17	10-4	9	8 (SBJ6)
16	12-3	10		16	62-34	10		16	12-4	10	
15	14-3	11	12 (PBJ5)	15	64-34	11	12 (RBJ5, RBJ4)	15	14-4	11	12 (SBJ4)
14	16-3	12		14	66-34	12		14	16-4	12	
13	18-3	13		13	68-34	13		13	18-4	13	
12	20-3	14		12	70-34	14		12	20-4	14	
11	22-3	15		11	72-34	15		11	22-4	15	
10	24-3	16		10	74-34	16		10	24-4	16	
1	25-3	4		1	75-34	4		1	25-4	4	
2	27-3	5		2	77-34	5		2	27-4	5	
3	29-3	6		3	79-34	6		3	29-4	6	
4	31-3	7		4	81-34	7		4	31-4	7	
5	33-3	8	3 (PAJ7)	5	83-34	8	3 (RAJ7, RAJ6)	5	33-4	8	3 (SAJ6)
6	35-3	9	7 (PAJ5)	6	85-34	9	7 (RAJ5, RAJ4)	6	35-4	9	7 (SAJ4)
7	37-3	10		7	87-34	10		7	37-4	10	
8	39-3	11	13 (PAJ1)	8	89-34	11	13 (RAJ1, RAJ0)	8	39-4	11	13 (SAJ0)
9	41-3	12		9	91-34	12		9	41-4	12	
19	43-3	13		19	93-34	13		19	43-4	13	
35	45-3	14		35	95-34	14		35	45-4	14	
18	47-3	15		18	97-34	15		18	47-4	15	
34	49-3	16		34	99-34	16		34	49-4	16	
31	26-3	5		31	76-34	5		31	26-4	5	
47	28-3	6		47	78-34	6		47	28-4	6	
30	30-3	7		30	80-34	7		30	30-4	7	
46	32-3	8	4 (PBJ9)	46	82-34	8	4 (RBJ9, RBJ8)	46	32-4	8	4 (SBJ8)
29	34-3	9	6 (PBJ3)	29	84-34	9	6 (RBJ3, RBJ2)	29	34-4	9	6 (SBJ2)
45	36-3	10		45	86-34	10		45	36-4	10	
28	38-3	11	14 (PBJ1)	28	88-34	11	14 (RBJ1, RBJ0)	28	38-4	11	14 (SBJ0)
44	40-3	12		44	90-34	12		44	40-4	12	
27	42-3	13		27	92-34	13		27	42-4	13	
43	44-3	14		43	94-34	14		43	44-4	14	
26	46-3	15		26	96-34	15		26	46-4	15	
42	48-3	16		42	98-34	16		42	48-4	16	

INFORMATION CENTER TAP INPUTS FOR DISKS 3 & 4.

TABLE 3.1-4

DISK 1

CONNECTOR RACK H	PIN	LEVEL	HEADS RACK L	HEADS RACK M	PIN
HAVO & HAUO	13	HRWL-11-2	1Ø-LAN7	1Ø-MAN7	1
			2Ø-LCJ1	2Ø-MCJ1	2
	5	HRWL-11-2/	3Ø-LAJ7	3Ø-MAJ7	1
			4Ø-LBJ9	4Ø-MBJ9	2
	15	HRWL-12-2	5Ø-LAL7	5Ø-MAL7	1
			6Ø-LBJ3	6Ø-MBJ3	2
	7	HRWL-12-2/	7Ø-LAJ5	7Ø-MAJ5	1
			8Ø-LBJ7	8Ø-MBJ7	2
	10	HRWL-13-2	11Ø-LAJ3	11Ø-MAJ3	1
			12Ø-LBJ5	12Ø-MBJ5	2
	2	HRWL-13-2/	13Ø-LAJ1	13Ø-MAJ1	1
			14Ø-LBJ1	14Ø-MBJ1	2
HAUO & HAVO & HAWO	8	SCTL-L-2	1Ø-LAN7	1Ø-MAN7	4
			4Ø-LBJ9	4Ø-MBJ9	
			5Ø-LAL7	5Ø-MAL7	
			6Ø-LBJ3	6Ø-MBJ3	
			11Ø-LAJ3	11Ø-MAJ3	
			14Ø-LBJ1	14Ø-MBJ1	
HAUO	4	T1CW-1	2Ø-LCJ1		3
			4Ø-LBJ9		
			6Ø-LBJ3		
			8Ø-LBJ7		
			12Ø-LBJ5		
			14Ø-LBJ1		
		T1CW-2	1Ø-LAN7		
			3Ø-LAJ7		
			5Ø-LAL7		
			7Ø-LAJ5		
			11Ø-LAJ3		
			13Ø-LAJ1		
HAVO	4	T1CC-1		3Ø-MAJ7	3
				7Ø-MAJ5	
				13Ø-MAJ1	
		T1CC-2		1Ø-MAN7	
				5Ø-MAL7	
				11Ø-MAJ3	
		T1CC-3		4Ø-MBJ9	
				6Ø-MBJ3	
				14Ø-MBJ1	
		T1CC-4		2Ø-MCJ1	
				8Ø-MBJ7	
				12Ø-MBJ5	

HRWL & TOUCH CIRCUIT LINES FROM RACKS L & M TO RACK H

TABLE 3.1-5

DISK 2					
CONNECTOR RACK H	PIN	LEVEL	HEADS RACK N	HEADS RACK M	PIN
HAWO & HAVO	14	HRWL-21-2	1E-NAM7	1E-MAM7	1
			2E-NCJ0	2E-MCJ0	2
	6	HRWL-21-2/	3E-NAJ6	3E-MAJ6	1
			4E-NBJ8	4E-MBJ8	2
	11	HRWL-22-2	5E-NAK7	5E-MAK7	1
			6E-NBJ2	6E-MBJ2	2
	3	HRWL-22-2/	7E-NAJ4	7E-MAJ4	1
			8E-NBJ6	8E-MBJ6	2
	9	HRWL-23-2	11E-NAJ2	11E-MAJ2	1
			12E-NBJ4	12E-MBJ4	2
	1	HRWL-23-2/	13E-NAJ0	13E-MAJ0	1
			14E-NBJ0	14E-MBJ0	2
HAUO & HAVO & HAWO	8	SCTL-L-2	1E-NAM7	1E-MAM7	4
			4E-NBJ8	4E-MBJ8	
			5E-NAK7	5E-MAK7	
			6E-NBJ2	6E-MBJ2	
			11E-NAJ2	11E-MAJ2	
			14E-NBJ0	14E-MBJ0	
HAWO	12	T2CC-1	2E-NCJ0		3
			4E-NBJ8		
			6E-NBJ2		
			8E-NBJ6		
			12E-NBJ4		
			14E-NBJ0		
		T2CC-2	1E-NAM7		
			3E-NAJ6		
			5E-NAK7		
			7E-NAJ4		
			11E-NAJ2		
			13E-NAJ0		
HAVO	12	T2CW-1		3E-MAJ6	3
				7E-MAJ4	
				13E-MAJ0	
		T2CW-2		1E-MAM7	
				5E-MAK7	
				11E-MAJ2	
		T2CW-3		4E-MBJ8	
				6E-MBJ2	
				14E-MBJ0	
		T2CW-4		2E-MCJ0	
				8E-MBJ6	
				12E-MBJ4	

HRWL & TOUCH CIRCUIT LINES FROM RACKS N & M TO RACK H

TABLE 3.1-6

DISK 3					
CONNECTOR RACK J	PIN	LEVEL	HEADS RACK P	HEADS RACK R	PIN
JAUO & JAVO	13	HRWL-31-2	1Ø-PAN7	1Ø-RAN7	1
			2Ø-PCJ1	2Ø-RCJ1	2
	5	HRWL-31-2/	3Ø-PAJ7	3Ø-RAJ7	1
			4Ø-PBJ9	4Ø-RBJ9	2
	15	HRWL-32-2	5Ø-PAL7	5Ø-RAL7	1
			6Ø-PBJ3	6Ø-RBJ3	2
	7	HRWL-32-2/	7Ø-PAJ5	7Ø-RAJ5	1
			8Ø-PBJ7	8Ø-RBJ7	2
	10	HRWL-33-2	11Ø-PAJ3	11Ø-RAJ3	1
			12Ø-PBJ5	12Ø-RBJ5	2
	2	HRWL-33-2/	13Ø-PAJ1	13Ø-RAJ1	1
			14Ø-PBJ1	14Ø-RBJ1	2
JAUO & JAVO & JAWO	8	SCTL-R-2	1Ø-PAN7	1Ø-RAN7	4
			4Ø-PBJ9	4Ø-RBJ9	
			5Ø-PAL7	5Ø-RAL7	
			6Ø-PBJ3	6Ø-RBJ3	
			11Ø-PAJ3	11Ø-RAJ3	
			14Ø-PBJ1	14Ø-RBJ1	
JAUO	12	T3CW-1	2Ø-PCJ1		3
			4Ø-PBJ9		
			6Ø-PBJ3		
			8Ø-PBJ7		
			12Ø-PBJ5		
			14Ø-PBJ1		
		T3CW-2	1Ø-PAN7		3
			3Ø-PAJ7		
			5Ø-PAL7		
			7Ø-PAJ5		
			11Ø-PAJ3		
			13Ø-PAJ1		
JAVO	12	T3CC-1		3Ø-RAJ7	3
				7Ø-RAJ5	
				13Ø-RAJ1	
		T3CC-2		1Ø-RAN7	
				5Ø-RAL7	
				11Ø-RAJ3	
		T3CC-4		4Ø-RBJ9	
				6Ø-RBJ3	
				14Ø-RBJ1	
		T4CC-1		2Ø-RCJ1	
				8Ø-RBJ7	
				12Ø-RBJ5	

HRWL & TOUCH CIRCUIT LINES FROM RACKS P & R TO RACK J

TABLE 3.1-7

DISK 4					
CONNECTOR RACK J	PIN	LEVEL	HEADS RACK S	HEADS RACK R	PIN
JAWO & JAVO	14	HRWL-41-2	1E-SAM7	1E-RAM7	1
			2E-SCJ0	2E-RCJ0	2
	6	HRWL-41-2/	3E-SAJ6	3E-RAJ6	1
			4E-SBJ8	4E-RBJ8	2
	11	HRWL-42-2	5E-SAK7	5E-RAK7	1
			6E-SBJ2	6E-RBJ2	2
	3	HRWL-42-2/	7E-SAJ4	7E-RAJ4	1
			8E-SBJ6	8E-RBJ6	2
	9	HRWL-43-2	11E-SAJ2	11E-RAJ2	1
			12E-SBJ4	12E-RBJ4	2
	1	HRWL-43-2/	13E-SAJ0	13E-RAJ0	1
			14E-SBJ0	14E-RBJ0	2
JAUO & JAVO & JAWO	8	SCTL-R-2	1E-SAM7	1E-RAM7	4
			4E-SBJ8	4E-RBJ8	
			5E-SAK7	5E-RAK7	
			6E-SBJ2	6E-RBJ2	
			11E-SAJ2	11E-RAJ2	
			14E-SBJ0	14E-RBJ0	
JAWO	4	T4CC-1	2E-SCJ0		3
			4E-SBJ8		
			6E-SBJ2		
			8E-SBJ6		
			12E-SBJ4		
			14E-SBJ0		
		T4CC-2	1E-SAM7		3
			3E-SAJ6		
			5E-SAK7		
			7E-SAJ4		
			11E-SAJ2		
			13E-SAJ0		
JAVO	4	T4CW-1		3E-RAJ6	3
				7E-RAJ4	
				13E-RAJ0	
		T4CW-2		1E-RAM7	
				5E-RAK7	
				11E-RAJ2	
		T4CW-3		4E-RBJ8	
				6E-RBJ2	
				14E-RBJ0	
		T4CW-4		2E-RCJ0	
				8E-RBJ6	
				12E-RBJ4	

HRWL & TOUCH CIRCUIT LINES FROM RACKS S & R TO RACK J

Refer to Table 3.1-8.

1L ..... HAKO	3L ..... JAKO
1U ..... HANO	3U ..... JANO
2L ..... HAPO	4L ..... JAPO
2U ..... HALO	4U ..... JALO

Clock Head output cables from Clock Heads to interconnection boards.

TABLE 3.1-8

DISK 1					DISK 2				
CONNECTOR RACK H	PIN	LEVEL	PIN	CLOCK HEAD	CONNECTOR RACK H				CLOCK HEAD
HAKO	1	GND-AB-3	1	10 CWL HAK1	HAPO	1	GND-AB-3	1	10 CWL HAP1
	2	CBLP-D1/	2			2	CBUP-D2	2	
	3	CALP-D1/	3			3	CAUP-D2	3	
	4	T1CW-D1-1	4			4	T2CW-D2-1	4	
	5	CHCL-11-1	5			5	CHCL-21-1	5	
	6	CBLP-D1	6			6	CBUP-D2/	6	
	7	CALP-D1	7			7	CAUP-D2/	7	
	8	CHCL-13-1	8			8	CHCL-23-1	8	
	9	CHCL-12-1	9			9	CHCL-22-1	9	
HANO	1	GND-AB-3	1	10 CCWL HAN1	HALO	1	GND-AB-3	1	10 CCWL HAL1
	2	CBUP-D1	2			2	CBLP-D2/	2	
	3	CAUP-D1	3			3	CALP-D2/	3	
	4	T1CC-0	4			4	T2CC-D2-1	4	
	5	CHCL-11-2	5			5	CHCL-21-2	5	
	6	CBUP-D1/	6			6	CBLP-D2	6	
	7	CAUP-D1/	7			7	CALP-D2	7	
	8	CHCL-13-2	8			8	CHCL-23-2	8	
	9	CHCL-12-2	9			9	CHCL-22-2	9	

DISK 3					DISK 4				
CONNECTOR RACK J	PIN	LEVEL	PIN	CLOCK HEAD	CONNECTOR RACK J	PIN	LEVEL	PIN	CLOCK HEAD
JAKO	1	GND-AB-5	1	10 CWR JAK1	JAPO	1	GND-AB-5	1	10 CWR JAP1
	2	CBLP-D3/	2			2	CBUP-D4	2	
	3	CALP-D3/	3			3	CAUP-D4	3	
	4	T3CW-D3-1	4			4	T4CW-D4-1	4	
	5	CHCL-31-1	5			5	CHCL-41-1	5	
	6	CBLP-D3	6			6	CBUP-D4/	6	
	7	CALP-D3	7			7	CAUP-D4/	7	
	8	CHCL-33-1	8			8	CHCL-43-1	8	
	9	CHCL-32-1	9			9	CHCL-42-1	9	
JANO	1	GND-AB-5	1	10 CCWR JAN1	JALO	1	GND-AB-5	1	10 CCWR JAL1
	2	CBUP-D3	2			2	CBLP-D4/	2	
	3	CAUP-D3	3			3	CALP-D4/	3	
	4	T3CC-D3-1	4			4	T4CC-D4-1	4	
	5	CHCL-31-2	5			5	CHCL-21-2	5	
	6	CBUP-D3/	6			6	CBLP-D4	6	
	7	CAUP-D3/	7			7	CALP-D4	7	
	8	CHCL-33-2	8			8	CHCL-43-2	8	
	9	CHCL-32-2	9			9	CHCL-42-2	9	

Refer to Table 3.1-9.

HAX0, JAX0 — AADON2 — Information output cables from interconnection boards to Module logic gate.

TABLE 3.1-9

AADON2	LEVEL	HAX0	AADON2	LEVEL	JAX0
		1			1
		2			2
		3			3
		4			4
H1	T1CW-0	5	H4	T3CW-0	5
K1	SCTL-L-1	6	K4	SCTL-R-1	6
A1	HRWL-12-1/	7	A4	HRWL-32-1/	7
C0	HRWL-21-1/	8	C3	HRWL-41-1/	8
C1	HRWL-11-1/	9	C4	HRWL-31-1/	9
J1	T1CC-0	10	J4	T3CC-0	10
A0	HRWL-22-1/	11	A3	HRWL-42-1/	11
E1	HRWL-13-1/	12	E4	HRWL-33-1/	12
E0	HRWL-23-1/	13	E3	HRWL-43-1/	13
		14			14
		15			15
		16			16
J0	T2CC-0	17	J3	T4CC-0	17
		18			18
B1	HRWL-12-1	19	B4	HRWL-32-1	19
D0	HRWL-21-1	20	D3	HRWL-41-1	20
D1	HRWL-11-1	21	D4	HRWL-31-1	21
H0	T2CW-0	22	H3	T4CW-0	22
B0	HRWL-22-1	23	B3	HRWL-42-1	23
F1	HRWL-13-1	24	F4	HRWL-33-1	24
F0	HRWL-23-1	25	F3	HRWL-43-1	25

Refer to Table 3.1-10.

HAM0, JAM0 — AAA0A2 — Clock output cables from interconnection boards to Module logic gate.

POWER CABLES INTER-UNIT

Refer to Table 3.1-11.

Rack E Panel A — CAJ0 — (Motor Power Relay Box in Module) — AC power cables from Sequence Panel in Electronic Unit to each Module.

Refer to Table 3.1-12.

Rack E Panel B — AAB0N2 — DC power cables from Sequence Panel in Electronic Unit to each Module.

TABLE 3.1-10

AAA0A2	LEVEL	HAM0	AAA0A2	LEVEL	JAM0
A2	GND-AB-2	1	B2	GND-AB-1	1
B1	CHCL-22-0	2	B3	CHCL-42-3	2
C1	CHCL-21-0	3	C3	CHCL-41-3	3
F2	CHCL-13-3	4	L2	CHCL-33-0	4
D1	CHCL-13-0	5	D3	CHCL-33-3	5
C2	CHCL-23-3	6	H2	CHCL-43-0	6
A1	CHCL-23-0	7	A3	CHCL-43-3	7
D0	CAUP-2/	8	D4	CAUP-1/	8
A0	CBUP-2/	9	A4	CBUP-1/	9
		10			10
		11			11
L0	CBLP-2/	12	L3	CBLP-1/	12
H0	CALP-2/	13	H4	CALP-1/	13
F1	CHCL-12-3	14	F3	CHCL-32-3	14
F0	CHCL-11-0	15	F4	CHCL-31-3	15
E1	CHCL-12-0	16	E3	CHCL-32-0	16
H1	CHCL-11-3	17	H3	CHCL-31-0	17
D2	CHCL-22-3	18	J2	CHCL-42-0	18
E2	CHCL-21-3	19	K2	CHCL-41-0	19
E0	CAUP-2	20	E4	CAUP-1	20
B0	CBUP-2	21	B4	CBUP-1	21
		22			22
		23			23
L1	CBLP-2	24	L4	CBLP-1	24
J0	CALP-2	25	J4	CALP-1	25

TABLE 3.1-11

E.U.	VOLTAGE	MODULE
RACK E PANEL A		CAJ0
EAR0	-24V	A
EAM0	110VAC-CONV.	B
EAJ0	208VAC-A	D
EAK0	208VAC-B	E
EAN0	NEUTRAL	F
ECL0	SMIL	G
ECK0	SMØL	H

TABLE 3.1-12

ELECTRONICS UNIT SEQUENCE PANEL	VOLTAGE	MODULE RACK A
RACK E PANEL B		AABON2
EBN0	+12V - AB	N0
EBR0	GND - AB	U0
	GND - CD	V0
	GND - E	W0
	GND - F	X0
	GND - G	Y0
EBJ0	-4.5VDC - AB	N3
	-4.5VDC - CD	P3
	-4.5VDC - E	R3
	-4.5VDC - F	S3
	-4.5VDC - G	T3
EBK0	-20VDC - AB	U3
	-20VDC - CD	V3
EBP0	-12VDC - AB	N4
	-12VDC - CD	P4
	-12VDC - E	R4
	-12VDC - F	S4
	-12VDC - G	T4
EBL0	+20VDC - AB	U4
	+20VDC - CD	V4
	+20VDC - E	W4
	+20VDC - F	X4
	+20VDC - G	Y4

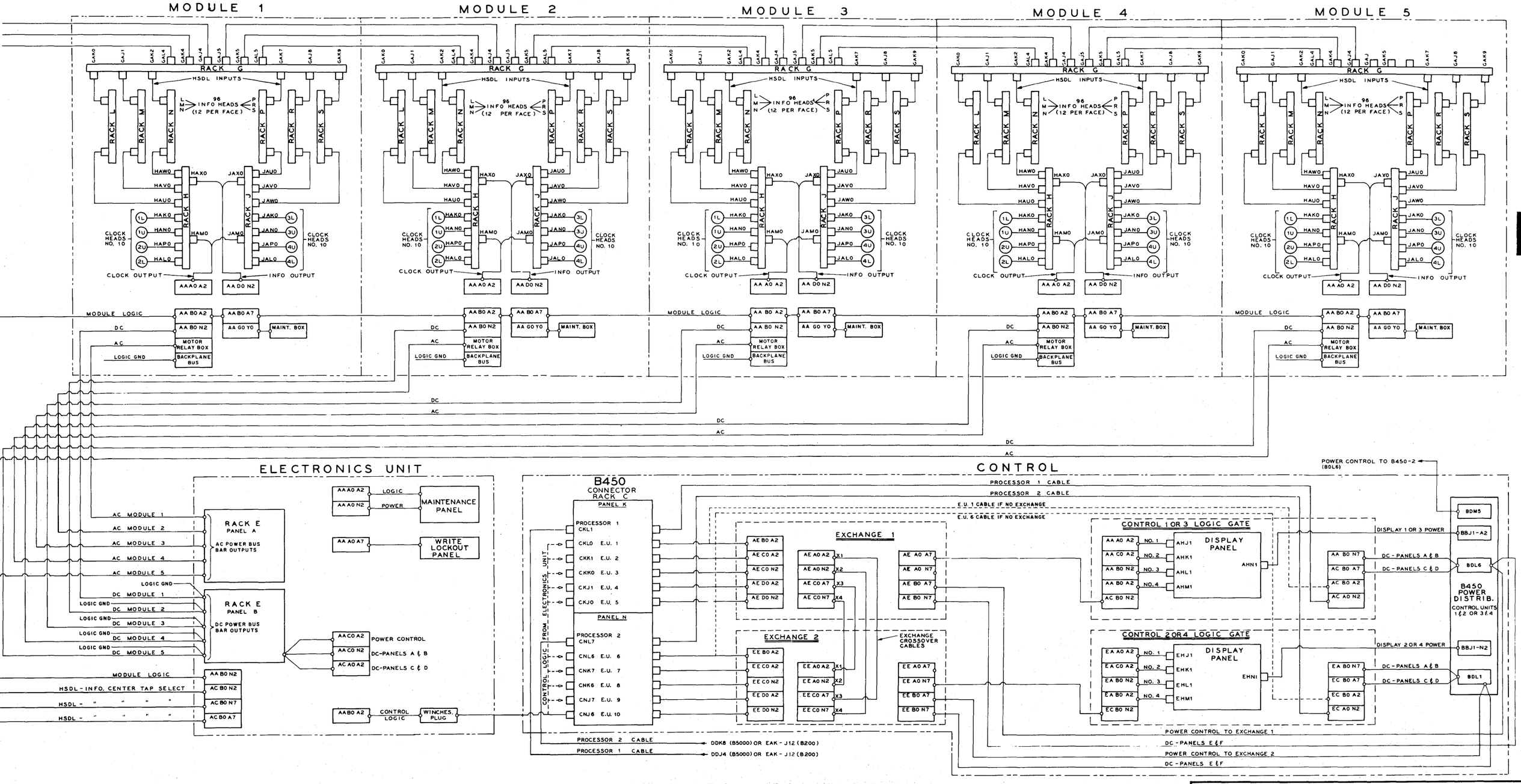

FIGURE 3.1-1
SUBSYSTEM CABLING DIAGRAM

FIGURE 3.1-1
SUBSYSTEM CABLING DIAGRAM

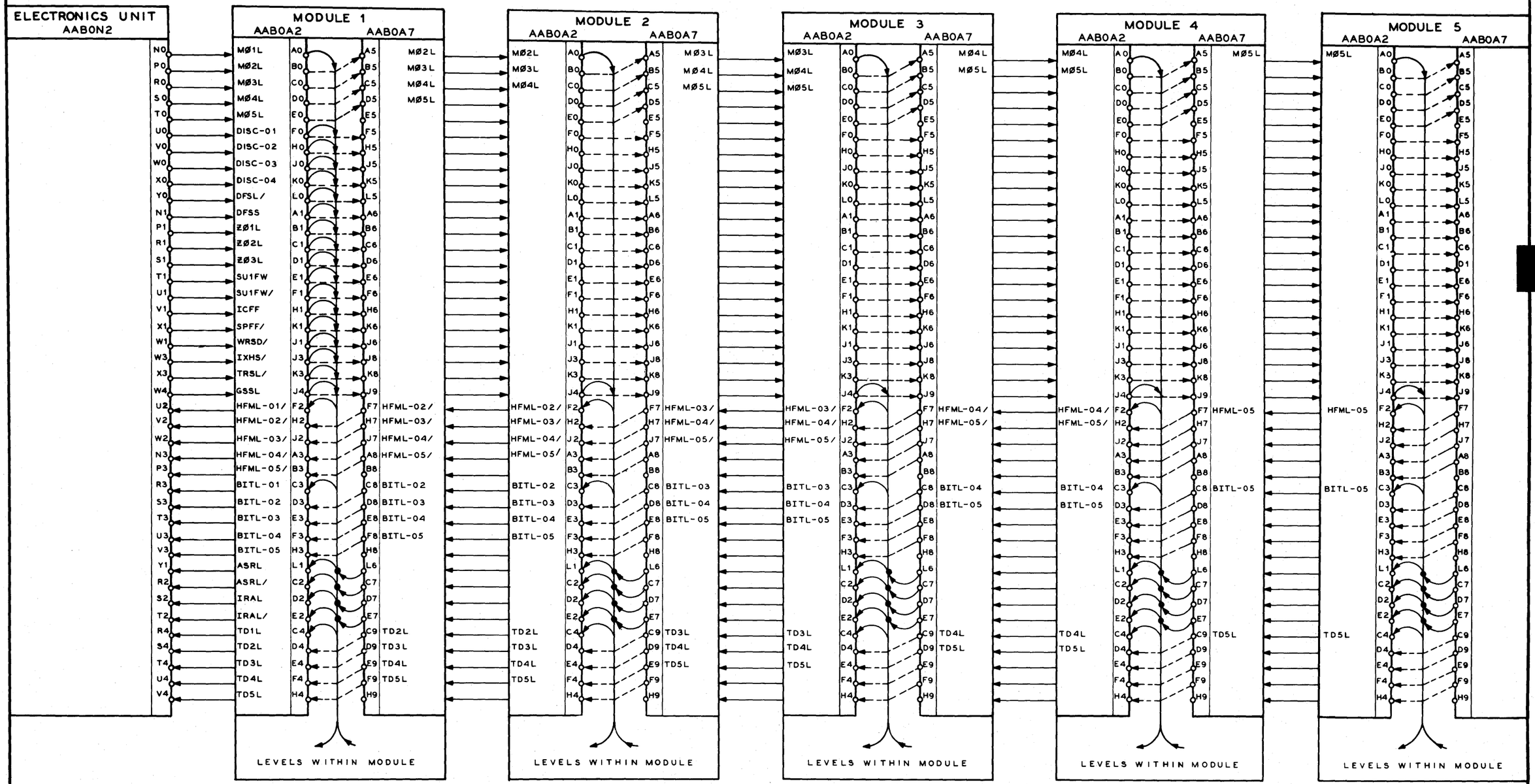

FIGURE 3.1-2
MODULE LOGIC CABLE

FIGURE 3.1-2
MODULE LOGIC CABLE

3.2 POWER SEQUENCING

All power for a Module is supplied by the Electronics Unit. Each Module has separate AC and DC cables which route from the E.U. Sequence Panel, Rack E, to connector CAJ0 for AC and AAB0N2 for DC. Refer to Section 3.1 B471 Manual for Power Sequencing to Module.

MOTOR ON SEQUENCE

Reference Figure 3.2-1.

Conditions

Motor Run Switch in Run position.

Heat Exchange Blowers off.

Running Time Meter off.

Disk Drive Motor off.

AC-ON-Cycle in E.U. complete	208VAC Legs A and B to contacts L2-L3 of MPR. -24V to pin C3 coil circuit MPR. Ground SMIL line.
SMIL	Pick MPR (ground pin C3 coil circuit through contacts 1-2 of Motor Run Switch). If the Motor Run Switch is in the Off position, SMIL will be coupled to the next Module through contacts 2-3 and MPR will not pick.
MPR contacts L2-T2 L3-T3	Start Heat Exchange Blower Motors, Running Time Meter and Disk Drive Motor.
contacts L1-T1	Closes starter winding line from pin 6 on motor to Leg B 208VAC. The motor will take approximately thirty seconds to reach normal operating speed, during which time the starter winding will pull 16 to 17 amps through the two-phase shift capacitors. As the motor speed increases, current through the line will decrease while the voltage increases. When the voltage reaches 350 volts, MSR

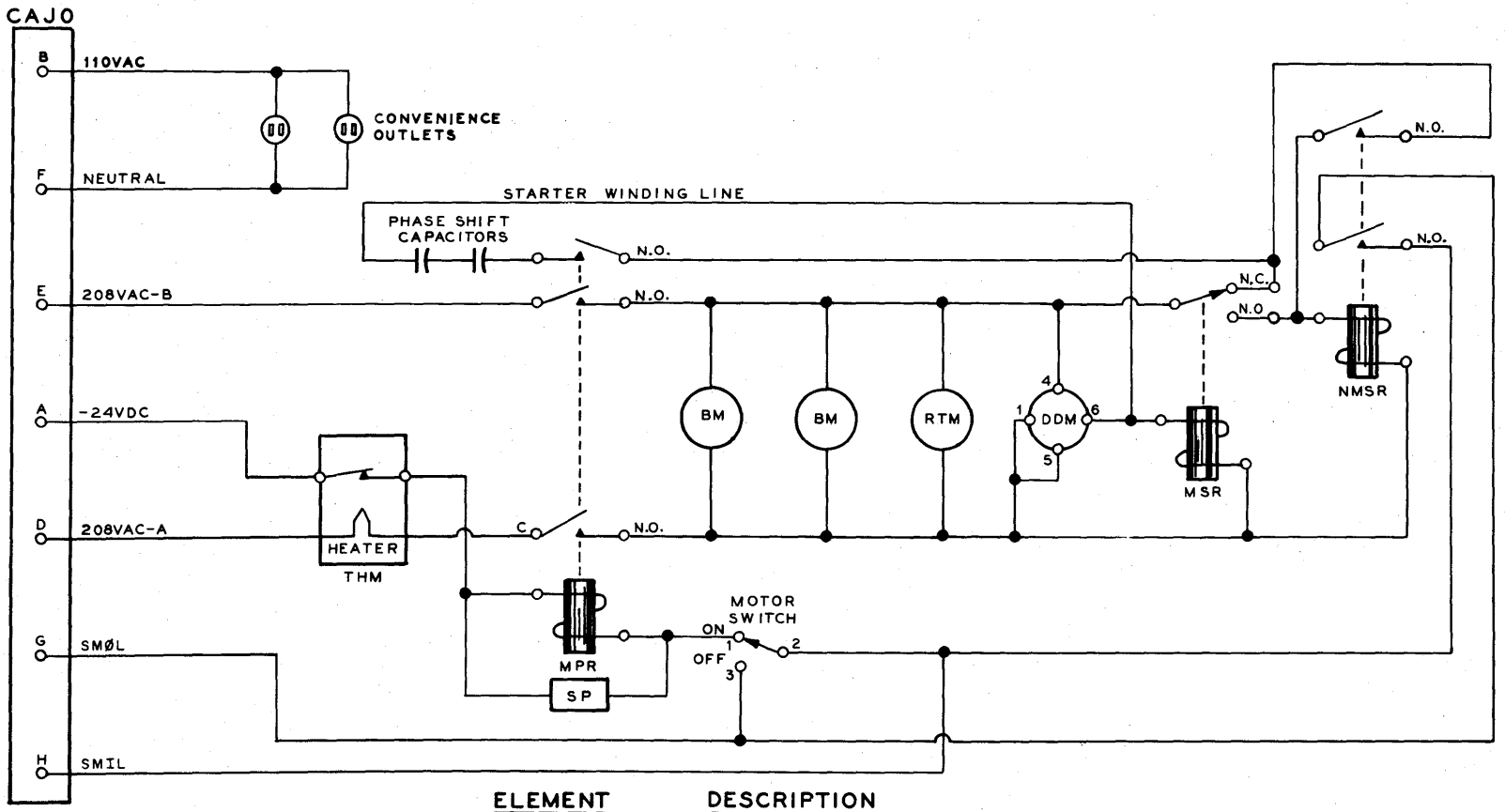

FIGURE 3.2-1
MOTOR ON SEQUENCE

ELEMENT	DESCRIPTION
THM	THERMAL OVERLOAD RELAY
MPR	MOTOR POWER RELAY
MSR	MOTOR START RELAY
NMSR	NEXT MOTOR START RELAY
DDM	DISK DRIVE MOTOR
BM	HEAT EXCHANGER BLOWER MOTORS
RTM	RUNNING TIME METER
SP	ARC SUPPRESSOR

	(Motor Started Relay) will pick.
MSR contacts 1-2	Open starter winding line; motor should be up to normal running speed.
contacts 2-6	Pick NMSR (Next Motor Start Relay) (208VAC Leg B to pin 4 coil circuit).
NMSR contacts 5-7	Couple SMIL to next Module (SMOL).
contacts 9-10	Hold NMSR picked.

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3.3 CIRCUIT BOARD DESCRIPTION

RACK G - CENTER TAP DISTRIBUTION BOARD

Reference Figure 3.3-1.

Rack G is located between the two disk enclosure bulkheads and extends into the two disk enclosures. Connectors GAK0, GAJ1 and GAK2 are inside the left enclosure (disks 1 and 2) and GAK7, GAJ8 and GAK9 are inside the right enclosure (disks 3 and 4). Connectors GAL4, GAK4, GAJ4, GAL5, GAK5 and GAJ5 are between the bulkheads.

The 100 center tap select levels (HSDL 00 through 99) from the Electronics Unit or preceeding Module are routed on three cables to connectors GAL4, GAK4 and GAJ4. From these connectors the HSDL levels are routed via printed circuit lines to GAK2, GAJ1 and GAK0 for the left enclosure; GAK7, GAJ8 and GAK9 for the right enclosure; and GAL5, GAK5 and GAJ5 for the next Module. Refer to Section 3.1 for pin cross-reference tables.

RACKS L, M, N, P, R AND S - HEAD SUPPORT BOARDS

Reference Figure 3.3-2.

Racks L, M and N are located inside the left enclosure (disks 1 and 2) and Racks P, R and S are located inside the right enclosure (disks 3 and 4). The six boards are identical in size and printed circuitry. They differ in diode configuration and information head location depending on which disk face they are associated with. The Ø (odd) and E (even) callouts refer to disk number. Each information head and diode location is marked with the head number (1 through 14) and Ø for disks one and three and E for disks two and four.

Since the two center boards, Racks M (left) and R (right), are associated with the inside faces of an odd and even disk, they will have diodes and information heads in all locations. The clockwise left (Rack L) and clockwise right (Rack P) boards have diodes and information heads in the Ø locations only since they are associated with the odd disks one and three. The counter-clockwise left (Rack N) and counter-clockwise right (Rack S) boards have diodes and information heads in the E locations only since they are associated with the even disks two and four.

There are two cables permanently attached to each board; a center tap select cable which routes the HSDL levels from Rack G to the board, and an information cable which routes the HRWL and touch circuit output levels from the board to Rack H or J (inter-connection boards). The board and the two cables make up a unit.

RACKS H AND J - INTERCONNECTION BOARDS

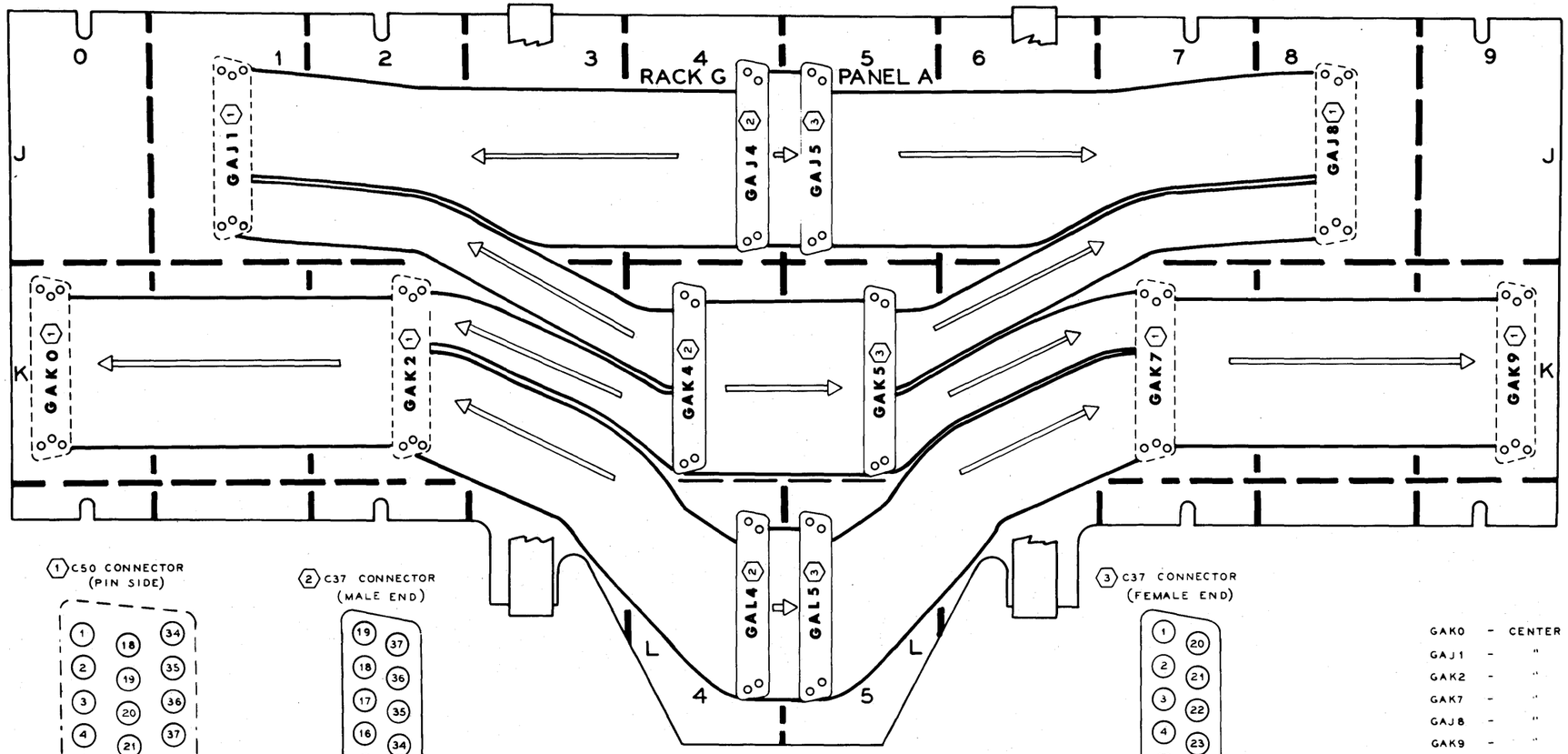
Reference Figures 3.3-3 and 3.3-4.

Rack H is located on the left disk enclosure bulkhead, Rack J is located on the right disk enclosure bulkhead. Racks H and J act as tie points for common clock and information head output lines.

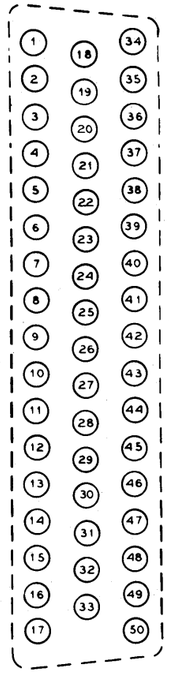
The four clock head cables associated with two disks in an enclosure plug into connectors HAK0-JAK0, HAL0-JAL0, HAN0-JAN0 and HAP0-JAP0. Common levels from these four connectors tie together by printed circuit lines to form two sets of output lines at connectors HAM0-JAM0. Cables from HAM0 and JAM0 combine to make one clock output cable which routes to the Module logic gate.

The three information output cables from Racks L, M and N and P, R and S plug into connectors HAU0-JAU0, HAV0-JAV0 and HAW0-JAW0. Common levels at these connectors tie together by printed circuit lines to form two sets of output lines at connectors HAX0-JAX0. The cables from HAX0 and JAX0 combine to make one information output cable which routes to the Module logic gate.

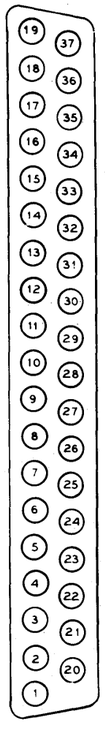
The four coils mounted on the boards are noise suppressors for the touch circuits in the four clock heads in each enclosure.



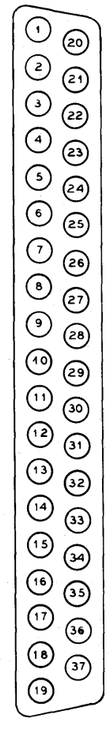
(1) C50 CONNECTOR (PIN SIDE)



(2) C37 CONNECTOR (MALE END)



(3) C37 CONNECTOR (FEMALE END)



(1)(2)(3) = TYPICAL PIN ARRANGEMENTS AS VIEWED FROM TOP OF ETCHED BOARD.
FOR SIGNAL TABLE SEE PAGE

GAK0 - CENTER TAP SELECT LEVELS 00 ⇒ 49 FOR DISK 1. (LOWER FACE)
GAJ1 - " " " " 50 ⇒ 99 FOR DISKS 1 & 2. (UPPER FACES)
GAK2 - " " " " 00 ⇒ 49 FOR DISK 2. (LOWER FACE)
GAK7 - " " " " 00 ⇒ 49 FOR DISK 3. (LOWER FACE)
GAJ8 - " " " " 50 ⇒ 99 FOR DISKS 3 & 4. (UPPER FACES)
GAK9 - " " " " 00 ⇒ 49 FOR DISK 4. (LOWER FACE)

GAJ4, GAK4, GAL4 - CENTER TAP SELECT LEVEL INPUTS FROM PRECEDING MODULES OR ELECTRONICS UNIT.

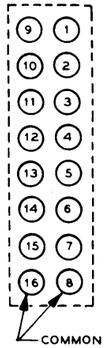
GAJ5, GAK5, GAL5 - CENTER TAP SELECT LEVEL OUTPUTS TO NEXT MODULE.

FIGURE 3.3-1
CENTER TAP DISTRIBUTION BOARD

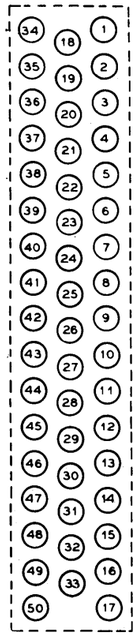
FIGURE 3.3-1
CENTER TAP DISTRIBUTION BOARD

(1) TYPICAL INFORMATION HEAD CONNECTOR

(2) C16 - OUTPUT HRWL LINES TO RACK H (LEFT) RACK J (RIGHT)



(3) C50 - INFORMATION CENTER TAP SELECT LINES FROM RACK G



(1)(2)(3) = PIN ARRANGEMENTS AS VIEWED FROM PIN SIDE OF ETCHED BOARD.

NOTE:

1. THIS DRAWING ILLUSTRATES RACKS L, M & N - (LEFT SIDE OF MODULE). RACKS P, R & S (RIGHT SIDE OF MODULE) THE SAME EXCEPT DIODES & CONNECTORS ARE MOUNTED ON OPPOSITE SIDE OF BOARDS.
2. DIODE & HEAD CONNECTOR CALLOUTS (ODD OR EVEN) REFER TO DISK NUMBER. INFORMATION HEADS FOR DISKS 1 & 3 USE Ø (ODD); DISKS 2 & 4 USE E (EVEN).

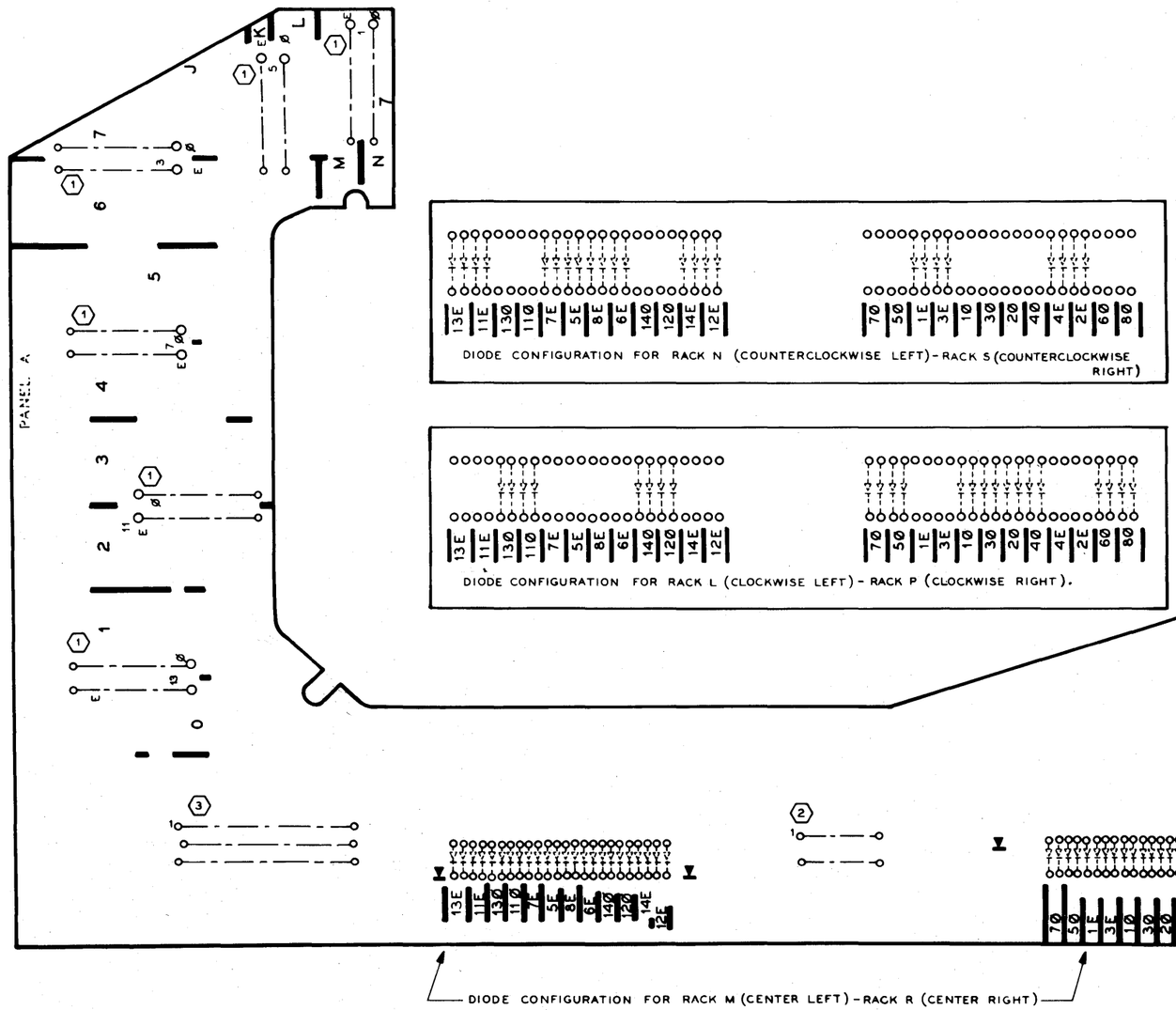
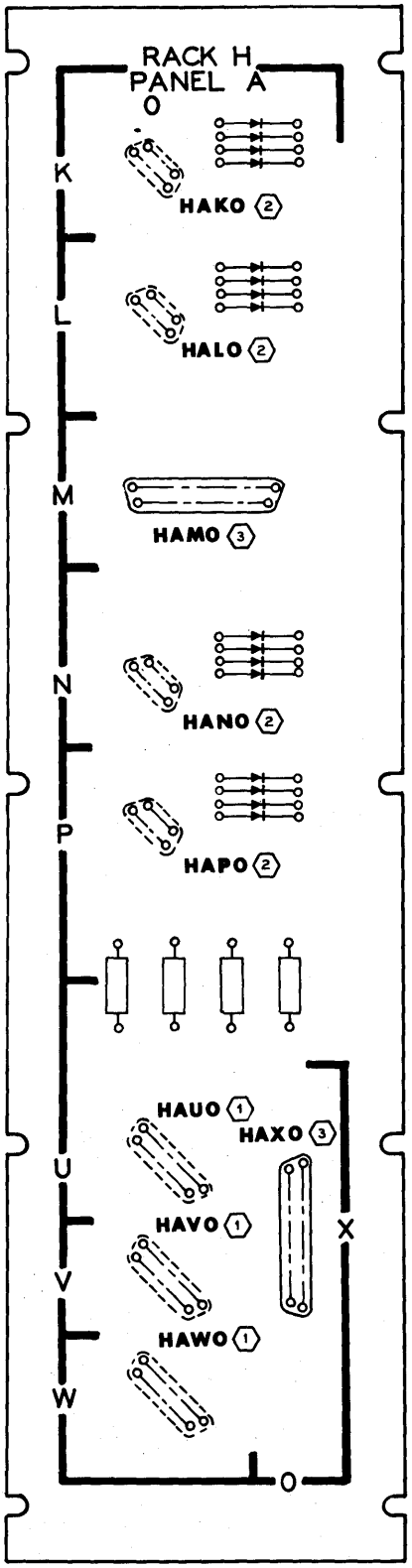
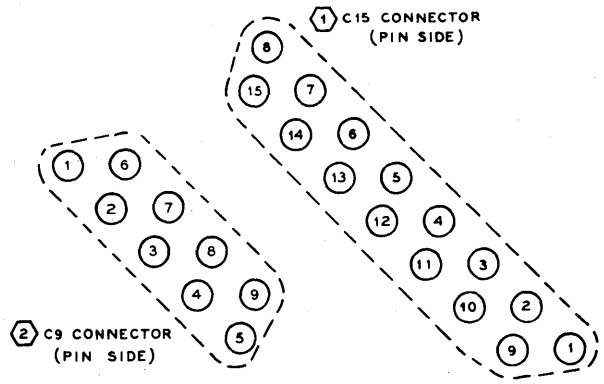
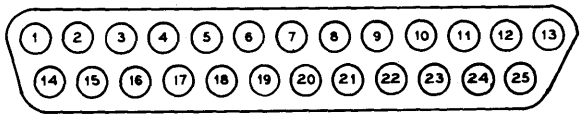


FIGURE 3.3-2
HEAD SUPPORT BOARD

FIGURE 3.3-2
HEAD SUPPORT BOARD







(3) C25 CONNECTOR (MALE END)

(1)(2)(3) = PIN ARRANGEMENTS AS VIEWED FROM COMPONENT SIDE OF ETCHED BOARD.

HAK0 = RACK H INTERCONNECTIONS TO DISK 1-LOWER FACE FOR CLOCK HEAD CENTER TAP INPUTS, BIT TRACK & ADDRESS TRACK OUTPUTS.

HAN0 = DISK 1 - UPPER FACE (SAME AS HAK0)

HAP0 = DISK 2 - UPPER FACE (SAME AS HAK0)

HAL0 = DISK 2 - LOWER FACE (SAME AS HAK0)

HAM0 = INTERCONNECTIONS BETWEEN RACK H & LOGIC GATE FOR DISKS 1 & 2 CLOCK HEAD CENTER TAP INPUTS, BIT TRACK & ADDRESS TRACK OUTPUTS.

THE CABLE FROM THIS CONNECTOR JOINS THE CABLE FROM JAM0. THE C50 END PLUGS INTO THE LOGIC GATE AT AAA0A2.

HAU0 = RACK H INTERCONNECTIONS TO DISK 1-LOWER FACE FOR INFORMATION HEAD READ/WRITE LINES & TOUCH CIRCUIT LINES.

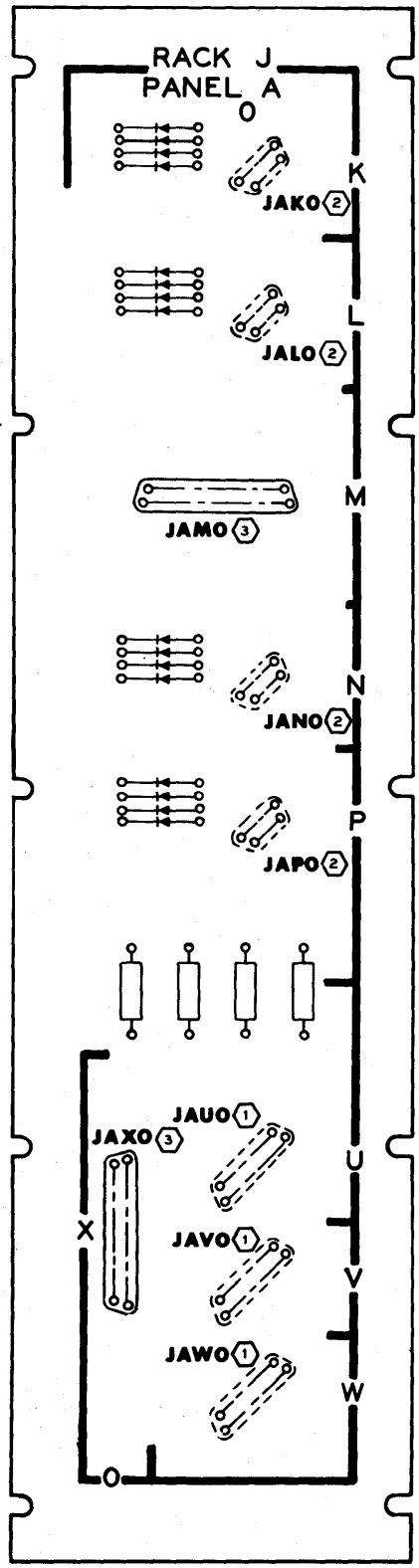
HAV0 = RACK H INTERCONNECTIONS TO DISKS 1 & 2-UPPER FACES. (SAME AS HAU0)

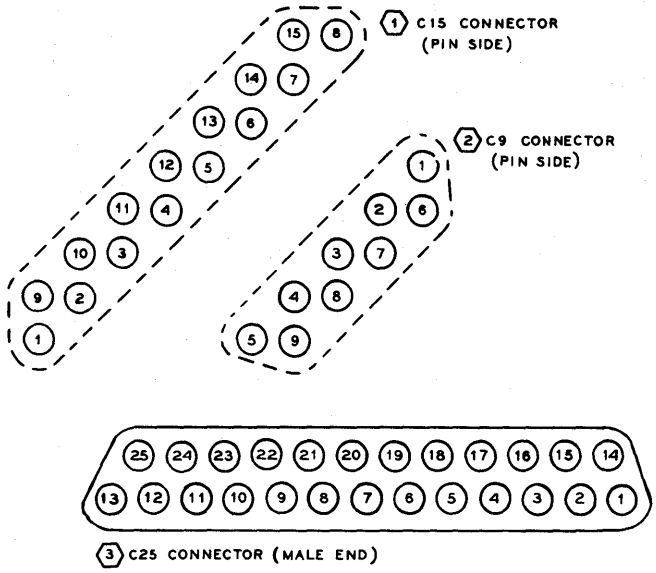
HAW0 = RACK H INTERCONNECTIONS TO DISK 2-LOWER FACE (SAME AS HAU0)

HAX0 = INTERCONNECTION BETWEEN RACK H & LOGIC GATE FOR DISKS 1 & 2 INFORMATION READ/WRITE LINES & TOUCH CIRCUIT LINES.

THE CABLE FROM THIS CONNECTOR JOINS THE CABLE FROM JAX0. THE C50 END PLUGS INTO THE MODULE LOGIC GATE AT AAD0N2.

FIGURE 3.3-3
INTERCONNECTION BOARD - RACK H





(1)(2)(3) = PIN ARRANGEMENTS AS VIEWED FROM COMPONENT SIDE OF ETCHED BOARD.

JAK0 = RACK J INTERCONNECTIONS TO DISK 3-LOWER FACE FOR CLOCK HEAD CENTER TAP INPUTS, BIT TRACK & ADDRESS TRACK OUTPUTS.

JAN0 = DISK 3-UPPER FACE (SAME AS JAK0)

JAP0 = DISK 4-UPPER FACE (SAME AS JAK0)

JAL0 = DISK 4-LOWER FACE. (SAME AS JAK0)

JAM0 = INTERCONNECTIONS BETWEEN RACK J & LOGIC GATE FOR DISKS 3 & 4 CLOCK HEAD CENTER TAP INPUTS, BIT TRACK & ADDRESS TRACK OUTPUTS.
THE CABLE FROM THIS CONNECTOR JOINS THE CABLE FROM HAM0. THE C50 END PLUGS INTO THE LOGIC GATE AT AAA0A2.

JAU0 = RACK J INTERCONNECTIONS TO DISK 3-LOWER FACE FOR INFORMATION HEAD READ/WRITE LINES & TOUCH CIRCUIT LINES.

JAV0 = RACK J INTERCONNECTIONS TO DISKS 3 & 4-UPPER FACES. (SAME AS JAU0)

JAW0 = RACK J INTERCONNECTIONS TO DISK 4-LOWER FACE. (SAME AS JAU0)

JAX0 = INTERCONNECTION BETWEEN RACK J & LOGIC GATE FOR DISKS 3 & 4 INFORMATION READ/WRITE LINES & TOUCH CIRCUIT LINES.

THE CABLE FROM THIS CONNECTOR JOINS THE CABLE FROM HAX0. THE C50 END PLUGS INTO THE MODULE LOGIC GATE AT AAD0N2.

FIGURE 3.3-4
INTERCONNECTION BOARD - RACK J

3.4 TACHOMETER CIRCUIT

The Tachometer Circuit monitors the disk speed by checking that the drive shaft is revolving at the correct speed. A small hole in the stainless steel drive shaft will induce a signal in the magnetic pick-up, mounted at the top of the pedestal casting, whenever the hole passes under the pick-up. The Correct Disk Speed Level, CDSL, is produced by one side of two cross-coupled switches. Refer to Figure 3.4-1 during the following explanation.

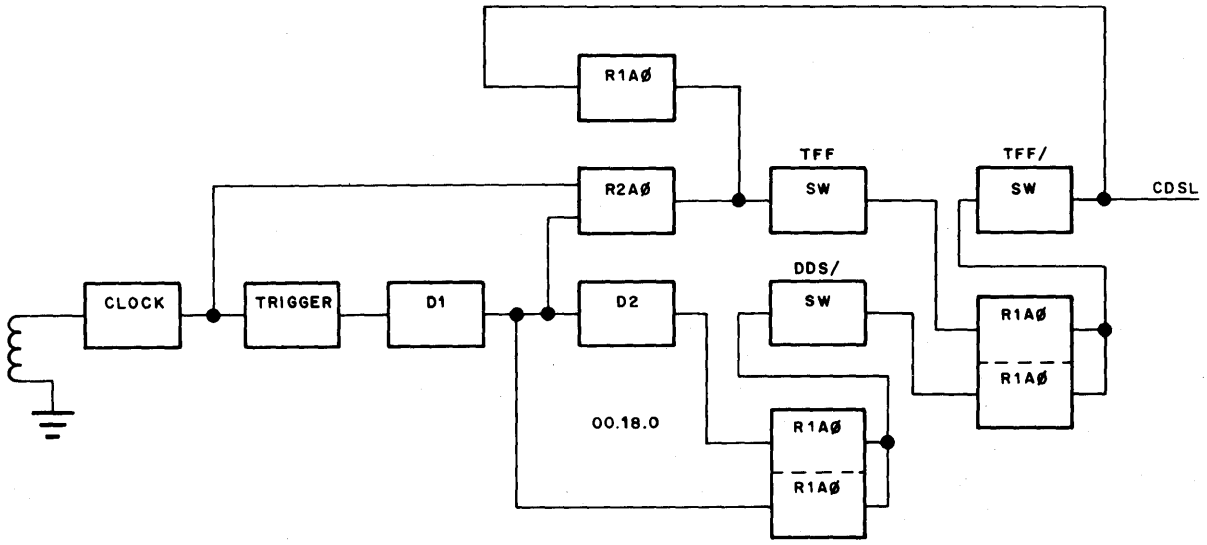


FIGURE 3.4-1
TACHOMETER LOGIC

SPEED UP SEQUENCE

Initially, the output of D1 and D2 will both be false, so the output of DDS/ will be true and CDSL will be false. This is the reset and "unlatching" logic. Refer to Figure 3.4-2 for timing reference.

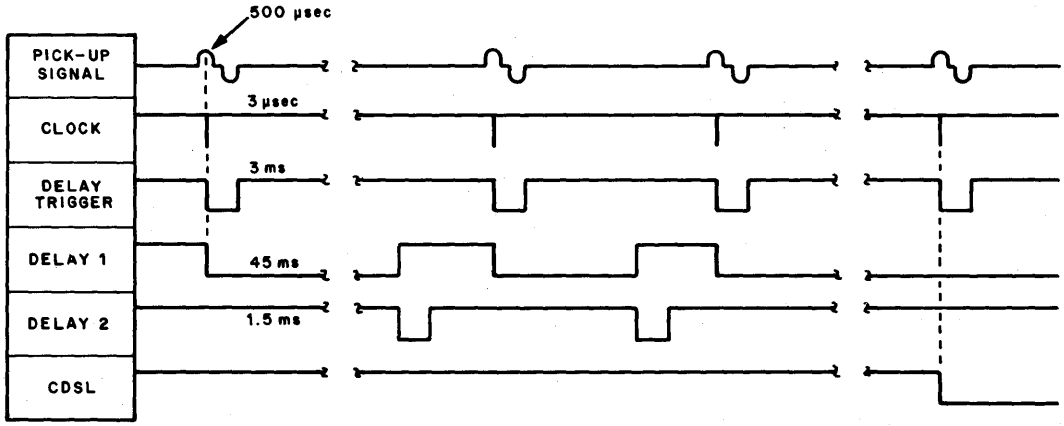


FIGURE 3.4-2
SPEED UP TIMING

During the positive half of the sine wave signal from the pick-up, a 3 microsecond clock pulse is produced. The trailing edge of each clock pulse fires the Trigger which is a 3 millisecond pulse. The leading edge of the Trigger output fires Delay 1 which is a 45 millisecond pulse. The trailing edge of Delay 1 fires Delay 2 which is a 1.5 millisecond pulse. As clock pulses occur at increasing frequency, the time between D1 output pulses becomes shorter until, at approximately 1425 RPM, D1 will not time out. With D1 true, Double Delay Not (DDS/) output is false. With the next clock pulse, the input to the Tachometer FF Switch, TFF, is true and now both inputs to TFF/, the Tachometer FF Not Switch, are false making CDSL true. CDSL will maintain a true input to TFF holding CDSL latched.

SLOW DOWN SEQUENCE

As clock pulses decrease in frequency, D1 will time out momentarily. Refer to Figure 3.4-3. When the disk speed has dropped to approximately 1325 RPM, D1 output will still be false when D2 times out. The output of DDS/ will be true and CDSL will go false.

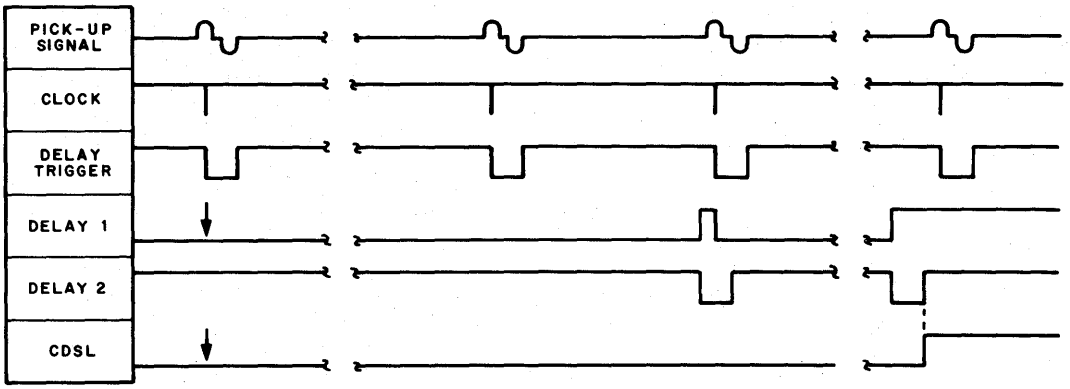


FIGURE 3.4-3
SLOW DOWN TIMING

DETAILED CIRCUIT DESCRIPTION

Clock and Delay Trigger

Refer to Figure 3.4-4. In quiescence, Q3 is on with base drive from the divider R27 and R25. With the collector of Q3 at near ground, Q1 is off. Q2 is on with base drive from the divider R3 and R6. In the Delay Trigger circuit, Q5 is on with base drive from divider R15 and R13. The collector of Q5 is near ground, removing base drive from Q4. Q4 is off.

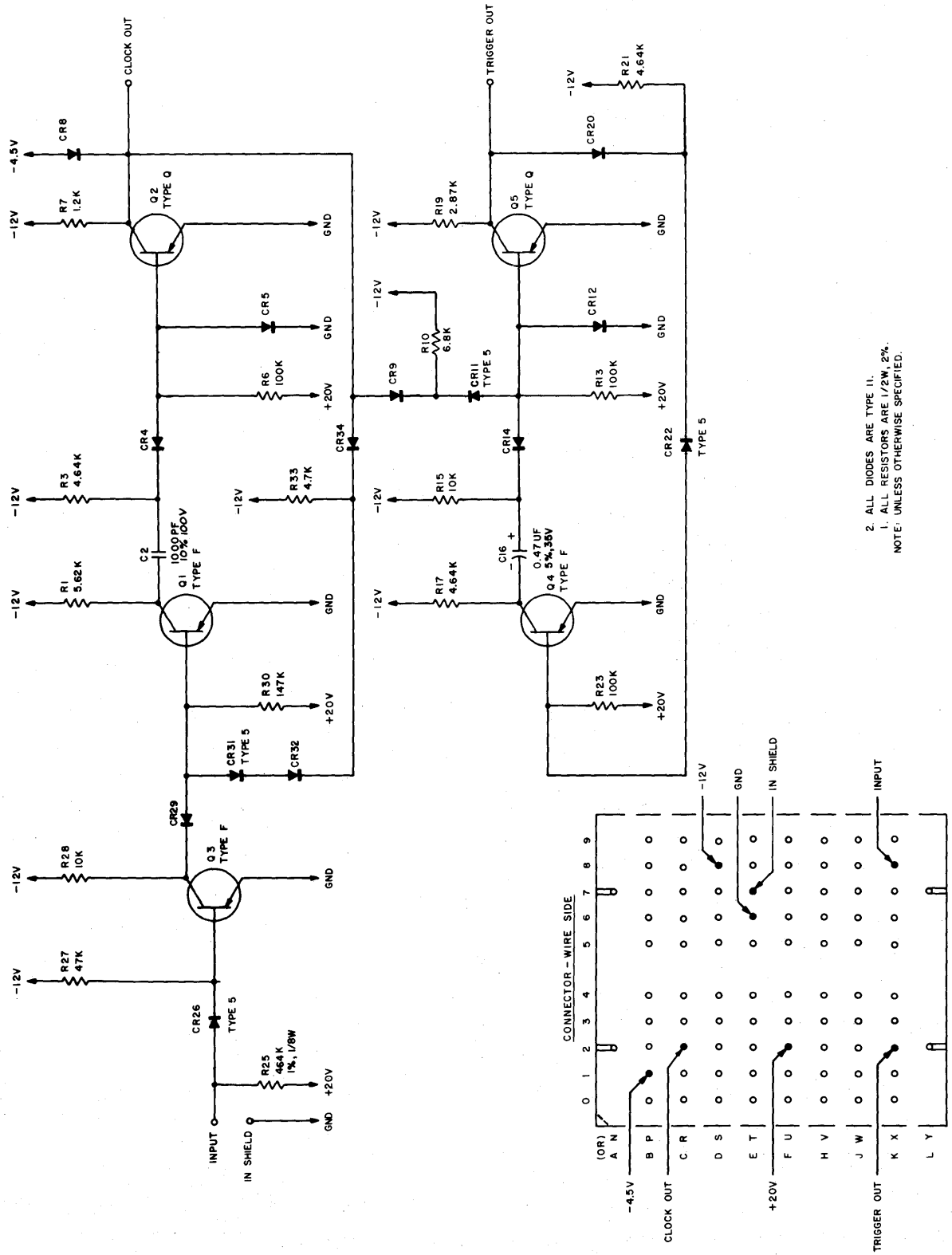


FIGURE 3.4-4
CLOCK AND DELAY TRIGGER

With a positive signal at the input (minimum 1V for 2 microseconds), base drive to Q3 is removed and Q3 turns off. -12V through R28, CR29, R30 to +20V supplies base drive to turn on Q1. The collector of Q1 goes to near ground and the positive change across C2 removes base drive from Q2 until C2 charges through R3 (RC time constant 3 microseconds). Q2 goes off for 3 microseconds.

With Q2 off, CR9 is reverse biased. Some extra base drive to Q5 from -12V through R10, CR11, R13 to +20V, puts cathode of CR11 at about -.9V.

When C2 has charged, R3 again supplies base drive to turn on Q2. With Q2 on, CR9 is forward biased and the cathode of CR11 goes to about -.4V. The stored charge of .5V in CR11 will remove base drive to Q5 and Q5 turns off.

With Q5 off, CR20 is reverse biased and R21 supplies base drive to turn on Q4. The collector of Q4 goes to near ground and the positive change is reflected across C16. Until C16 charges through R15, base drive is removed from Q5 (RC time constant 3.4 milliseconds). When C16 has charged, base drive is supplied to Q5 to turn it on. With Q5 on, CR20 is forward biased removing base drive to Q4. Q4 turns off.

Double Delay

Refer to Figure 3.4-5. The false level output of Delay Trigger at Input removes base drive from Q3 and Q3 is off. The base of Q1 is about -8V with divider network R1, R3 and R4. Emitter-base junction of Q1 forward biased and Q1 is on supplying base drive to Q2. Q2 is on and, with the collector near ground, CR7 is forward biased with the cathode about -.4V.

The Trigger Input signal is a negative 3.4 millisecond pulse which will permit base drive to Q3 from R25. The collector of Q3 goes to near ground. As soon as it is more positive than -8V, the base-emitter junction of Q1 is reverse biased and Q1 goes off. With Q1 off, there is no base drive to Q2 and Q2 goes off.

With Q2 off, CR7 is reverse biased and the cathodes of CR7 and CR9 are about -1.2V (two stabistor drops to base of Q5 which is about -.2V). The fall and rise time of the Delay 1 output from Q2 are speeded up by feedback through R5 to the base of Q1.

The Trigger Input goes false and removes base drive to Q3. Q3 goes off. The collector of Q3 will go toward -12V as C30 charges through R35, R28 and R29 (RC time constant 35-50 milliseconds). R35 is

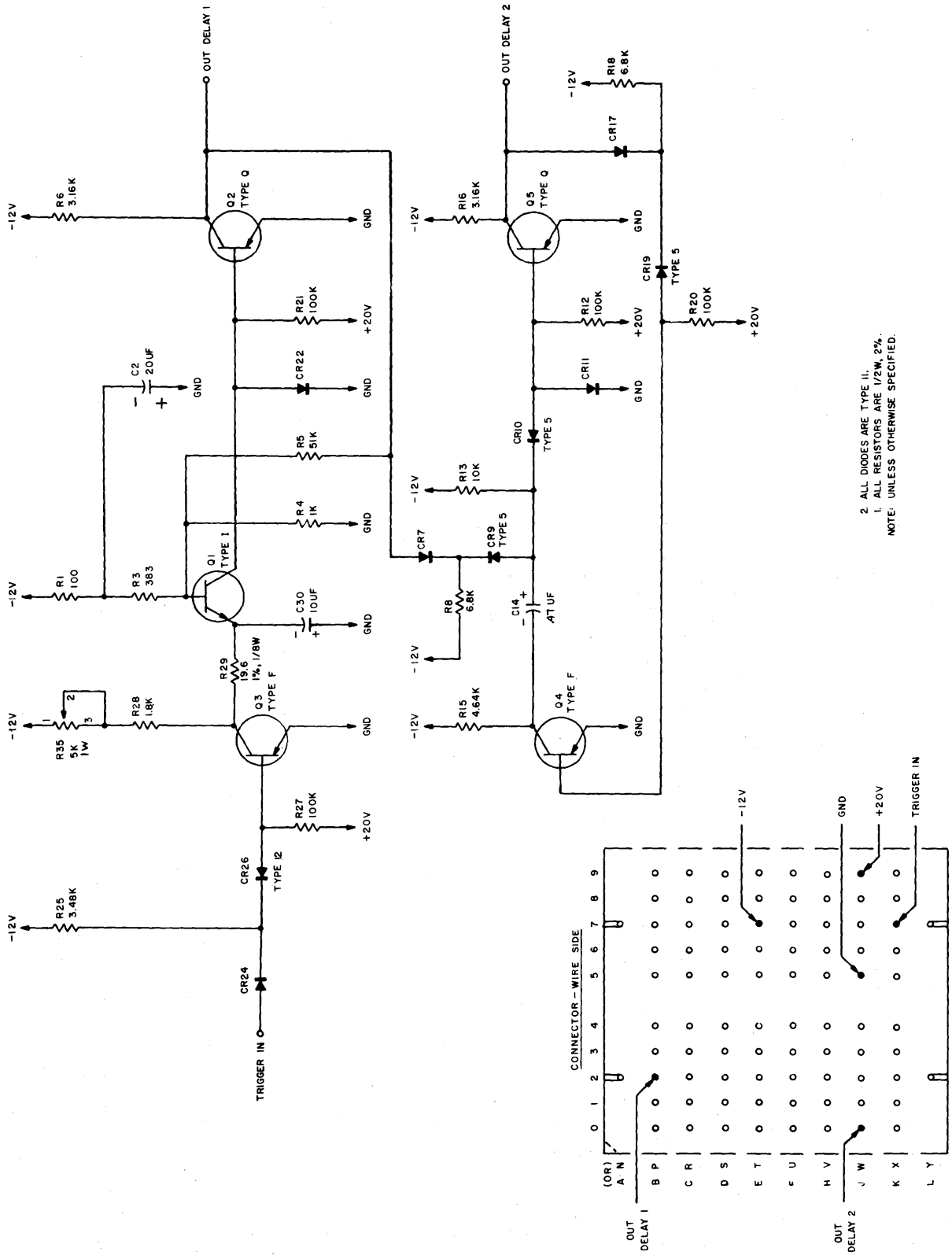


FIGURE 3.4-5
DOUBLE DELAY

nominally set for Delay 1 output of 45 milliseconds. With the collector of Q3 more negative than -8V, Q1 will turn on. Q1 will supply base drive to turn on Q2. The collector of Q2 will go to near ground and CR7 will be forward biased. The cathodes of CR7 and CR9 will now go to -.4V. The stored charge in CR9 will remove base drive from Q5 and Q5 will go off.

With Q5 off, CR17 is reverse biased. Base drive from R18 will turn on A4. The collector of Q4 goes to near ground and the positive change is reflected across C14. Until C14 charges through R13 and R8 in parallel, base drive is removed from Q5 (RC time constant 1.6 milliseconds). When C14 has charged, base drive is supplied to Q5 and Q5 turns on. With Q5 on, CR17 is forward biased and removes base drive to Q4. Q4 turns off.

3.5 TOUCH CIRCUIT

GENERAL DESCRIPTION

Reference Figure 3.5-2.

Each Module has touch circuitry which detects when any one of the 104 information and clock heads touch a disk. A touch is defined as either the physical contact of a head with a disk or the presence of foreign particles bridging the gap between the head assembly and the disk face. Each head assembly has two small touch probes cast in the head block which are flush with the block area exposed to the disk face. These probes have a one volt potential applied to them and will arc to the grounded disk face when the head flies too close or foreign particles pile up to bridge a head to the disk.

A touch failure must exist for a minimum of 200 microseconds before the touch circuit logic will take action and retract the heads. This delay is internal to TUDL (Touch Delay package) and eliminates all but genuine touch failures. Foreign particles smaller than the distance from head to disk will pass through the gap without making physical contact. Since these particles do not disturb Read or Write operations, the delay in the TUDL will not allow the touch circuit to take action. In summary, the touch circuit is designed to act only on conditions which will harm Read or Write operations or cause physical damage to the disk.

The touch probe outputs from the twelve information heads on a disk face join at the head support board associated with that face (Racks L, M or N for left side of Module - Racks P, R or S for right side of Module). The lines combine to make up one output and are brought to the interconnection boards (Rack H for left side of Module - Rack J for right side of Module). Here they are connected with their associated clock head touch outputs (one per face) which route directly from the clock heads to Racks H and J. These eight lines which represent the information and clock head touch outputs for each disk face are brought to the logic gate Rack A where they become the eight inputs to the four TUDL packages.

Reference Figure 3.5-1.

The touch circuit logic uses four TUDL packages which have the eight touch outputs from the eight disk faces as inputs. Each TUDL package acts as two separate cross-coupled switches, each with internal latching action and a 200 microsecond input delay. When an input is true, indicating a "no touch" condition, the output will be true; if an input should go false for 200 microseconds, in the case of a genuine touch failure, the output will go false and the circuit will latch in this state. A change of input level after that will not affect its state; it can only be reset by grounding the reset input which will make the output true.

TERMS

T1CC = Information and clock head touch probe outputs for disk 1 counter clockwise face.

T1CW = Information and clock head touch probe outputs for disk 1 clockwise face.

T2CC = Disk 2 (same as T1CC)

T2CW = Disk 2 (same as T1CW)

T3CC = Disk 3 (same as T1CC)

T3CW = Disk 3 (same as T1CW)

T4CC = Disk 4 (same as T1CC)

T4CW = Disk 4 (same as T1CW)

CC1L = TUDL output for disk 1, counter clockwise face (ground for "touch").

CW1L = TUDL output for disk 1, clockwise face (ground for "touch").

CC2L = Disk 2 (same as CC1L)

CW2L = Disk 2 (same as CW1L)

CC3L = Disk 3 (same as CC1L)

CW3L = Disk 3 (same as CW1L)

CC4L = Disk 4 (same as CC1L)

CW4L = Disk 4 (same as CW1L)

CDSL = Correct Disk Speed Level - true when disk drive motor at proper speed (1500 RPM)

SOLL = Solenoid Level - ground to pick air solenoid.

TØCL = Touch Level - true for a "no touch" condition, false for a "touch".

$\overline{\text{HFML}}$ = Heads Flying, Motor Up to Speed Level - false when S.U. Ready, true when Not Ready.

RESL = Reset Level - ground to reset TUDL packages.

ANRL = Air Pressure Not Ready Level - ground when air pressure to heads is less than 45 psi, floating (true) when air pressure at 45 psi.

APRL = Air Pressure Ready Level - ground when air pressure at 45 psi, floating (true) when air pressure less than 45 psi.

LØCL = Local Level - ground when LOCAL-REMOTE Switch is in REMOTE, floating (true) in LOCAL position.

MØ1L = Module Select Level - false when Module selected, true when not.

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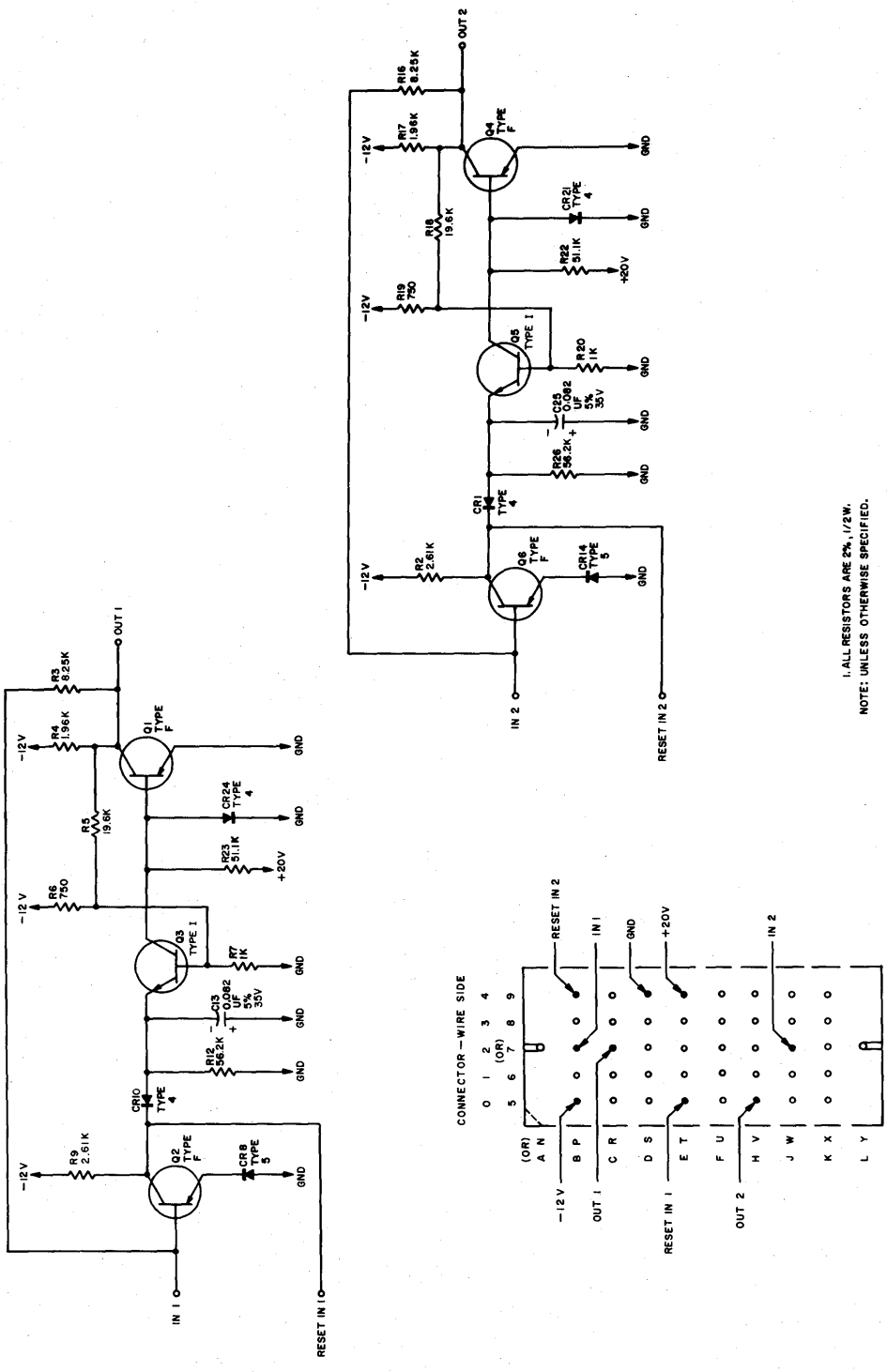


FIGURE 3.5-1
TUDL SCHEMATIC

OPERATIONAL DESCRIPTION

Conditions

MOTOR switch in RUN
LOCAL-REMOTE switch in REMOTE
HEAD RETRACT switch in FLY
TOUCH RESET switch open
AIR PRESSURE switch in normally closed position
Heat Exchange air flow switches open
Air solenoid de-energized

Power On Sequence

When AC and DC are applied to a Module and the above conditions are true, the disk drive motor will start, the heads will fly and the unit will go Ready. This sequence will happen automatically if no touch or air system failures occur. This description covers the sequence of events from AC ON to Unit Ready and explains what happens when a touch or air system failure is encountered.

AC To Module

AC to the Module via the MOTOR switch starts the disk drive motor and heat exchange fans. The heat exchange air flow switches will close and complete the air solenoid circuit from the DRPS (inverting solenoid driver) through the MOTOR switch, HEAD RETRACT switch, two heat exchange air flow switches and the solenoid coil to -24V DC. When the disk drive motor reaches the proper RPM, CDSL (Correct Disk Speed Level) from the tachometer logic will go true.

DC To Module - Package Power On

With air solenoid de-energized, the AIR PRESSURE switch will be in its normally closed position grounding input ANRL to Gate C. A false output from Gate C makes switch 5 output, HFML/, true and indicates S.U. Not Ready. HFML/ and APRL (from normally closed AIR PRESSURE switch) true to Gate D will make switch 4 output, TØCL, false. TØCL fed back to Gate C latches circuit and holds HFML/ true.

With heads not flying, the eight touch inputs to the TUDL packages will be true, making the eight outputs true. With the TOUCH RESET switch open, the RESL input to Gate B will be true. When CDSL goes true, the ten inputs to Gates A and B will be true which will make the inputs to the DRPS and Gate C true. With a true in, the DRPS will pick the air solenoid and the heads will fly. When the air pressure reaches 45 psi, the AIR PRESSURE switch will move to its normally open position, grounding APRL and making ANRL true (floating). The false output of Gate D will make TØCL true which is again fed back to Gate C. All inputs to Gate C true makes switch 5 output, HFML/, false

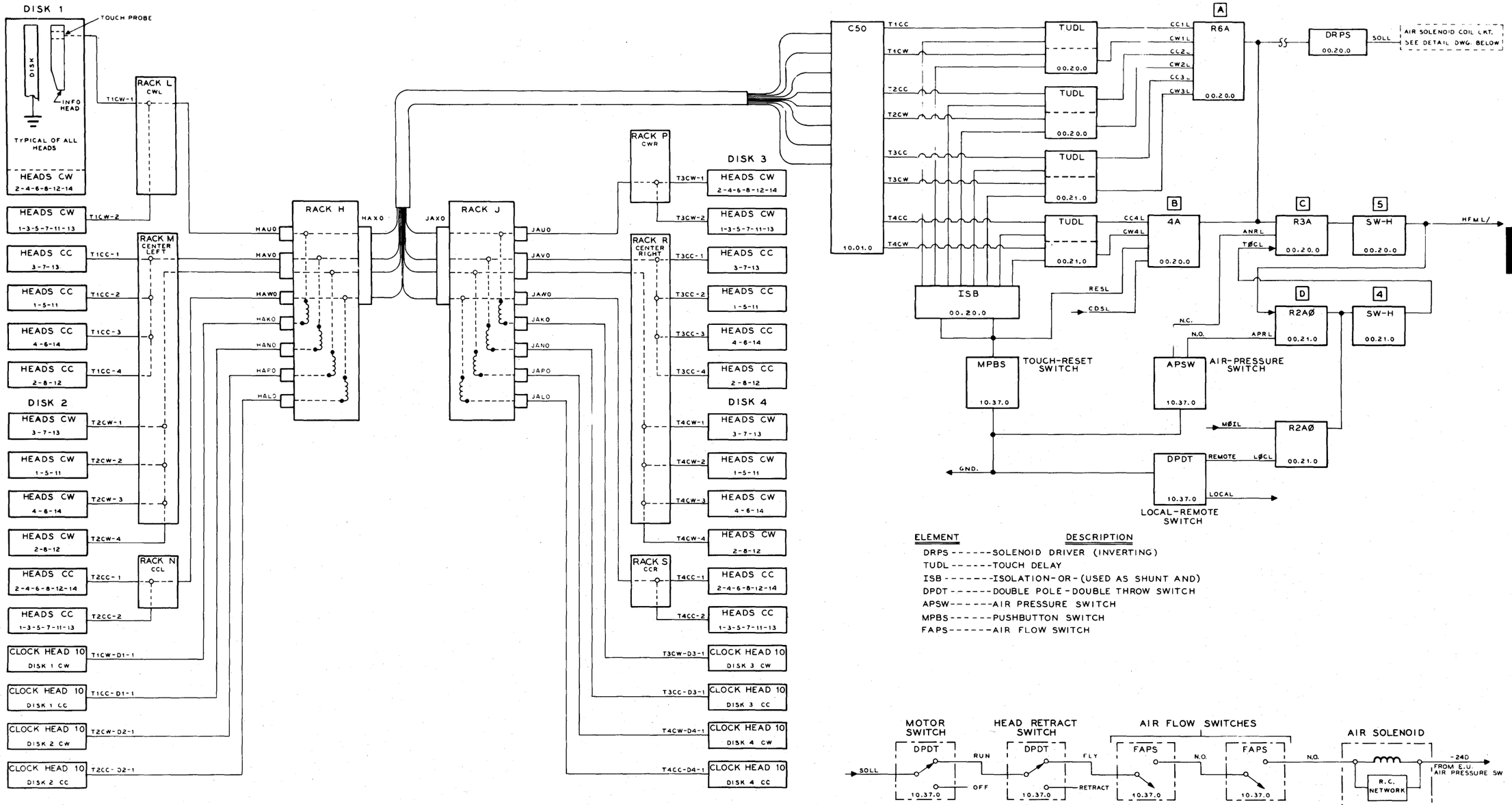
indicating Unit Ready. TØCL held true by Gate D will latch circuit in this state. At this time, the heads are flying and the unit is Ready. It will remain in this condition until a touch or air system failure or one of the switches in the air solenoid circuit is thrown.

Touch Failure

When a touch failure occurs, one of the eight inputs to the TUDL packages will go false (ground). If it is a genuine touch, it will last for 200 microseconds or more and overcome the TUDL input delay. The TUDL will latch up with a false output to Gate A or B. With one input to Gate A or B false, the input to the DRPS will be false which de-energizes the air solenoid. The heads will retract and the AIR PRESSURE switch will return to its normally closed position making ANRL false and APRL true. A false from Gate C to switch 5 will make HFML/ true and the unit will go Not Ready. HFML/ and APRL true to Gate D makes TØCL false which is again fed back to Gate C to latch the circuit up.

Heads are now retracted, the unit is Not Ready and the circuit will stay latched. It can only be reset by depressing the TOUCH RESET switch which grounds the RESL inputs to the TUDL packages.

The air solenoid may also be de-energized by heat exchange air flow failure, MOTOR switch OFF or HEAD RETRACT switch to RETRACT position. Unit may go Not Ready without de-energizing the air solenoid by throwing the LOCAL-REMOTE switch to LOCAL. This will make HFML/ true but will have no affect on the air solenoid circuit.



ELEMENT	DESCRIPTION
DRPS	SOLENOID DRIVER (INVERTING)
TUDL	TOUCH DELAY
ISB	ISOLATION-OR-(USED AS SHUNT AND)
DPDT	DOUBLE POLE-DOUBLE THROW SWITCH
APSW	AIR PRESSURE SWITCH
MPBS	PUSHBUTTON SWITCH
FAPS	AIR FLOW SWITCH

FIGURE 3.5-2
TOUCH CIRCUIT LOGIC SCHEMATIC

FIGURE 3.5-2
TOUCH CIRCUIT LOGIC SCHEMATIC

3.6 DISK LAYOUT

Refer to Figures 3.6-1, 3.6-2 and 3.6-3.

Information on the disk is organized in three zones. There are four information head assemblies for each zone. Each head assembly has thirteen channels providing a total of 52 tracks per zone. Normally, therefore, there will be two spares in a zone. The tracks of information head assemblies 1 and 2 are interlaced along the radius and the tracks of information head assemblies 3 and 4 are also radially interlaced. This pattern of interlaced head pairs is repeated in zones 2 and 3. Between zone 2 and zone 3 is a head assembly (#10) with only six channels. These six channels are the bit and address clock heads for the three zones.

A description of word structure and segments is helpful at this point in understanding the disk layout.

For operational versatility, Storage Modules are optional in any one of the following three different segment (record) lengths: 96, 240 or 480 character segments. The Disk File information word consists of eight BCL characters written serially by bit. Twelve of these eight-character words make up one 96 character option segment. The 240 character, 30-word segment is two and a half times longer than the 96 option; while the 480 character segment with 60 words is five times longer. All four disks in one Storage Module and all modules associated with one Electronics Unit must have the same segment option. The bit and address clock tracks determine the segment type and are the only difference between modules of different options. Clock tracks are pre-recorded before a module leaves the factory.

The maximum transfer rate from the disk is 308 kilocharacters per second. In order to adapt this to a rate allowing sufficient B200 or B5500 memory access time, the words from two different segments are interlaced along the information tracks. Therefore, while in a Read or Write operation, every other word encountered is an "inactive" word. Skipping over the inactive words reduces the maximum transfer rate to 154 kilocharacters/second, thereby providing time for memory accessing and address track sampling.

Figures 3.6-1 and 3.6-2 illustrate the organizational layouts for the 240 and 480 options. The organization of the 96 option follows the same pattern. Beginning at the dead space, interlaced segment pairs fall into sectors with an ascending number sequence which can be followed from zone 1 through zone 3. To consecutively read or write in all the segments along one track requires two disk revolutions. For example, the 12 segments on "Track 23, Zone 1" of a 480 option would be read 0 through 5 on the first revolution followed by 6 through 11 on the second.

Regardless of the basic option, each disk has two special segments designated M1 and M2 located at the end of every track in each zone. These are 96 character segments reserved for maintenance purposes.

Figure 3.6-3 represents a portion of a disk with the 96 character information segment option. The segment word interlace pattern illustrated is typical of all options as well as all maintenance segments. Note the relationship between word marks and the position of the words in their corresponding information zones. The first word of each segment is always the next word after its segment address. The bits in each bit clock track following the last word mark before dead space are called "pusher" bits. Their purpose is to shift the last four characters of word twelve of the M2 segments for the B200. Note the 20μsec dead space does not begin until after the last pusher bit has been read. The M3 addresses are psuedo addresses written to terminate an operation using an M1 segment.

Refer to Figure 3.6-4 for each option to find the number of segments per zone, the disk face and the disk set layout. For addressing purposes, the 240, 480 and 96 option have one, two and four disks per set, respectively.

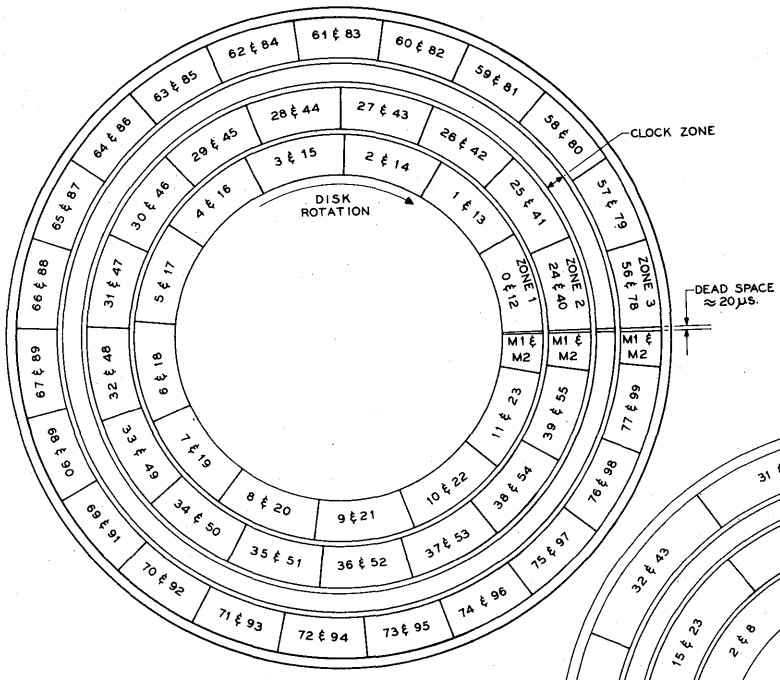


FIGURE 3.6-1
240 SEGMENT OPTION
CW DISK LAYOUT

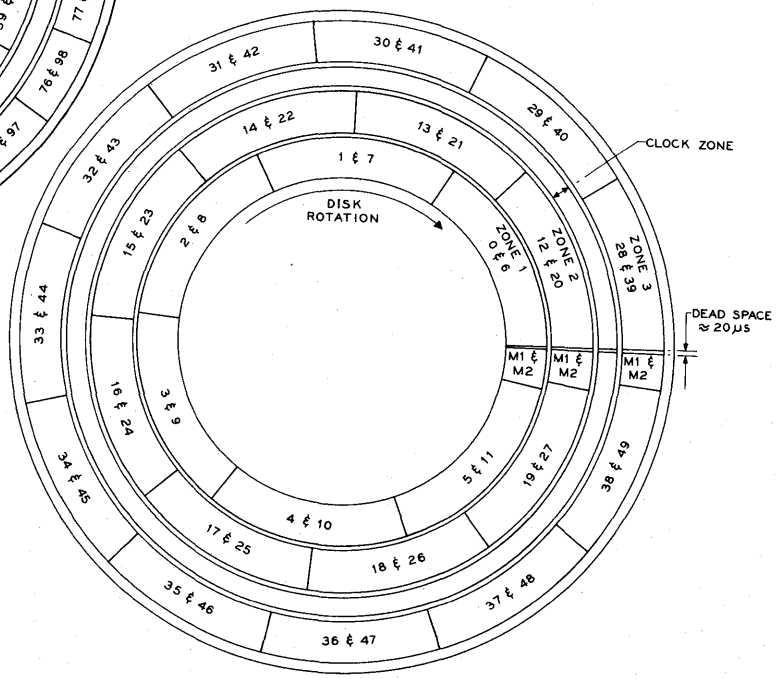
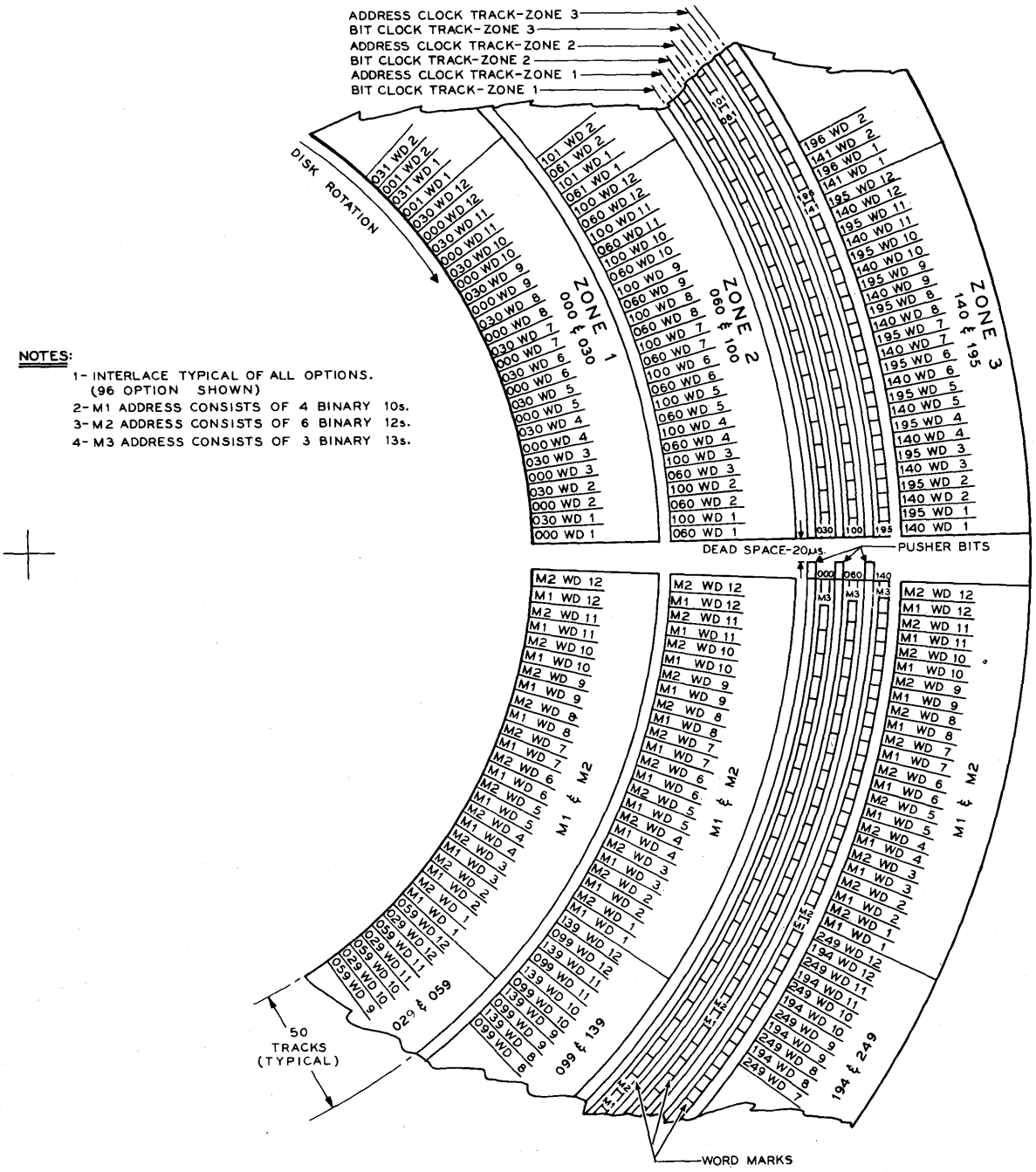


FIGURE 3.6-2
480 SEGMENT OPTION
CW DISK LAYOUT



NOTES:
1- INTERLACE TYPICAL OF ALL OPTIONS. (96 OPTION SHOWN)
2- M1 ADDRESS CONSISTS OF 4 BINARY 10s.
3- M2 ADDRESS CONSISTS OF 6 BINARY 12s.
4- M3 ADDRESS CONSISTS OF 3 BINARY 13s.

FIGURE 3.6-3
DISK LAYOUT - SEGMENT/WORD INTERLACE

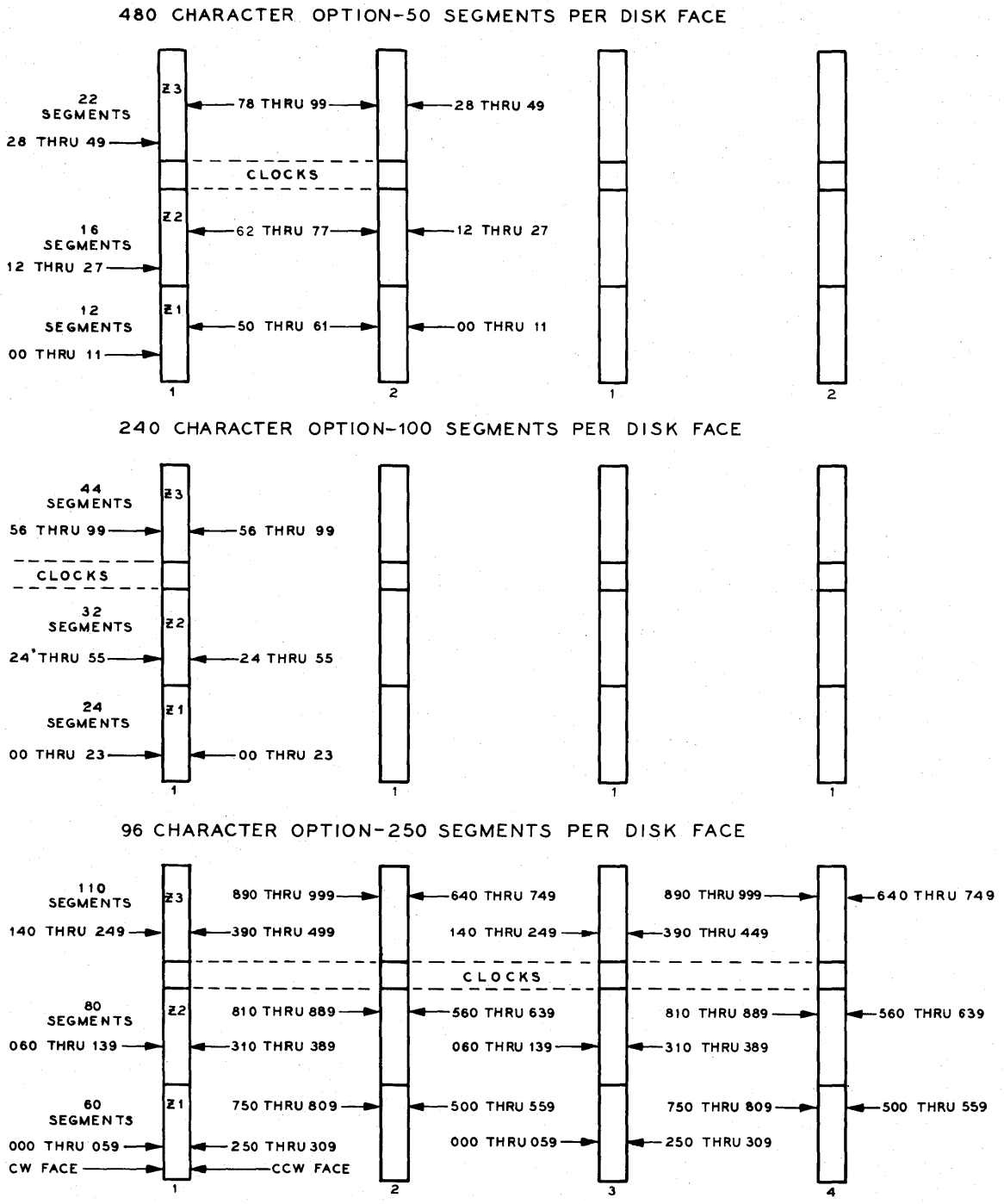


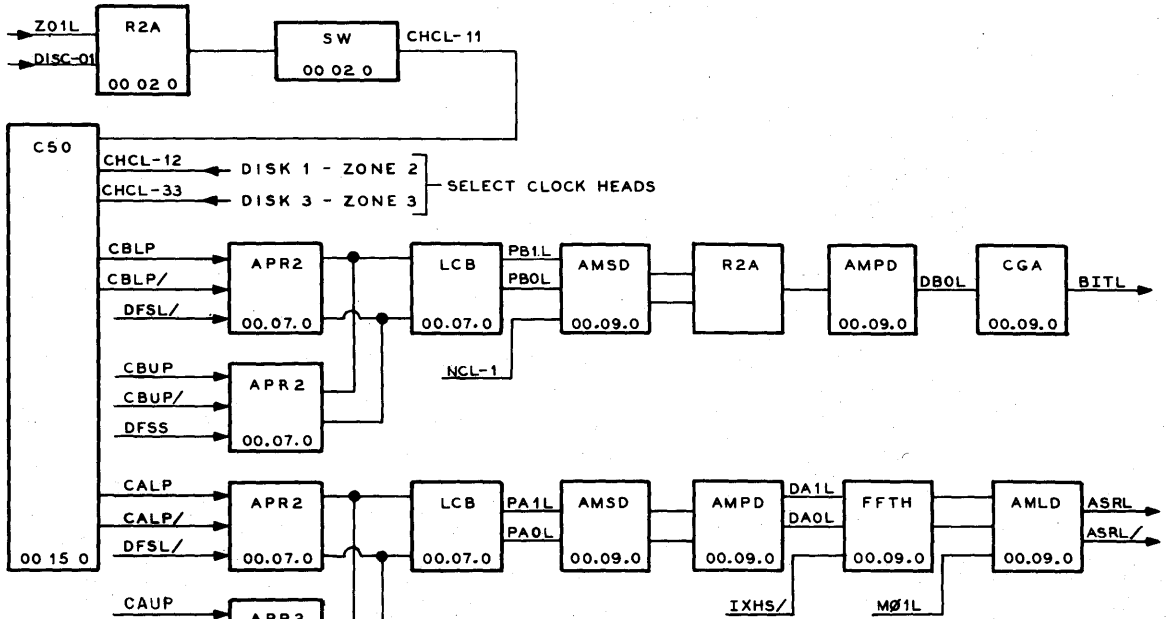
FIGURE 3.6-4
SEGMENTS - ZONE & DISK FACE

3.7 CLOCK CIRCUITS

Operations in the Disk File Subsystem are clocked by timing pulses which originate on the disk. The address word will select an information track and two corresponding clock tracks, the word/address track and the bit track. The word/address track generates a pulse to mark the beginning of each word. The word/address track also contains segment addresses for the segments in the associated zone. The six clock tracks are located between zone 2 and zone 3 on each disk face, with one bit track and one word mark track per zone.

The word mark track produces outputs called ASRL and ASRL/. The timing of the word mark track coincides with the bit track. A bit pulse occurs at word mark time and is followed by bit pulses for each bit time during the following word time.

The bit and word mark tracks are selected by grounding the center tap on four of the 48 clock heads in each of the Modules associated with the designated E.U. These four heads will be one bit clock head and one word mark head on both sides of one disk in one zone. The outputs from the four heads are connected to Pre-Amp Select circuits. Two of these circuits (one bit and one word mark) will be enabled by the disk face level. The Bit Clock output is sent to the E.U. ungated. The ASRL and ASRL/ outputs to the E.U. are gated by the Module select level.



ELEMENTS	DESCRIPTION
APR2	PRE-AMP SELECT 2
LCB	STICK (COIL-CAPACITOR)
AMSD	SENSE AMP - D.F.
AMPD	DIFFERENTIATOR
CGA	CLOCK GENERATOR
FFTH	TD FLIP-FLOP
AMLD	F/F LINE DRIVER

FIGURE 3.7-1
CLOCK CIRCUITS

Figure 3.7-1 shows the clock circuits and a portion of the clock center tap select circuits.

The selected center taps are grounded by one of twelve lines called CHCL - nn. The four Disk Select levels (Disk - 01 through Disk - 04) are ANDED with each of the three Zone Select levels (ZØ1L through ZØ3L) to produce the center tap select lines.

The Clock Head Center Tap levels (CHCL - nn) are numbered according to the disk and zone with the first "n" being the disk and the second the zone. CHCL - 11, shown on Figure 3.7-1, will select the Bit and Word Mark heads for zone 1 on Disk 1 lower face and upper face.

The outputs of all the lower face bit clock heads are connected in parallel to the input of a pre-amp. Similarly, the outputs of all the upper face bit clock heads are connected to the input of another pre-amp. The CW face of Disks 1 and 3 and the CCW face of Disks 2 and 4 are the lower face group. The Word Mark clock heads are divided in the same manner. The inputs to the pre-amps indicate which of the groups it is connected to. For example, CBLP is the Clock Bit Lower Pulse.

The desired Bit and Word Mark pre-amps are enabled by the Disk Face Select Levels (DFSL/ or DFSS). DFSL/ is true when the information head desired is on the CW face of Disks 1 or 3, or the CCW face of Disks 2 or 4. DFSL/ will enable the clock pre-amps connected to the lower face head assemblies.

NOTE

The voltages given in parentheses are only typical and considerable variations will be found.

Each output of the Bit pre-amp is a saw-tooth wave (250 millivolts peak to peak). The two outputs are directly out of phase. They are sent to a Sense Amp DF (AMSD) where they are separately amplified and clipped (1.5V positive pulses). The outputs of the Sense Amps are connected through two isolation diodes (R2A) to a differentiator circuit (AMPD). The output of the AMPD is a clamped sine wave with the half wave point occurring at the peak of the input (4.5V peak to peak). The sine wave is then sent to the Clock Generator (CGA). This circuit uses the negative going halves of the sine wave to develop 120 nanosecond negative pulses out (1.7V).

The circuitry for the output of the word mark track is the same as that for the bit up to the output of the AMSD. Since the word mark track contains information, it must be determined whether a flux change read is a "1" bit or "0" bit. The two outputs of the Sense Amp DF will be positive pulses for the positive going portion of the input signal. The pulses go to the Differentiator circuits whose outputs will set the Threshold Detecting Flip-Flop (FFTH). Refer to Figure 3.7-6. Output 2 of the TDFF will be true if a one bit was read and Output 1 false. These outputs are sent to the Flip-Flop

Line Driver where they are sent to the E.U. The TDFF is reset during the dead space by the level IXHS/.

CIRCUIT DESCRIPTIONS

Below is a list of the circuits described on the following pages:

Figure 3.7-2	Pre-Amp Select II	APR 2
Figure 3.7-3	Sense Amplifier DF	AMSD
Figure 3.7-4	Differentiator	AMPD
Figure 3.7-5	Clock Generator A	CG A
Figure 3.7-6	Threshold Detecting FF	FFTH
Figure 3.7-8	Flip-Flop Line Driver	AMLD

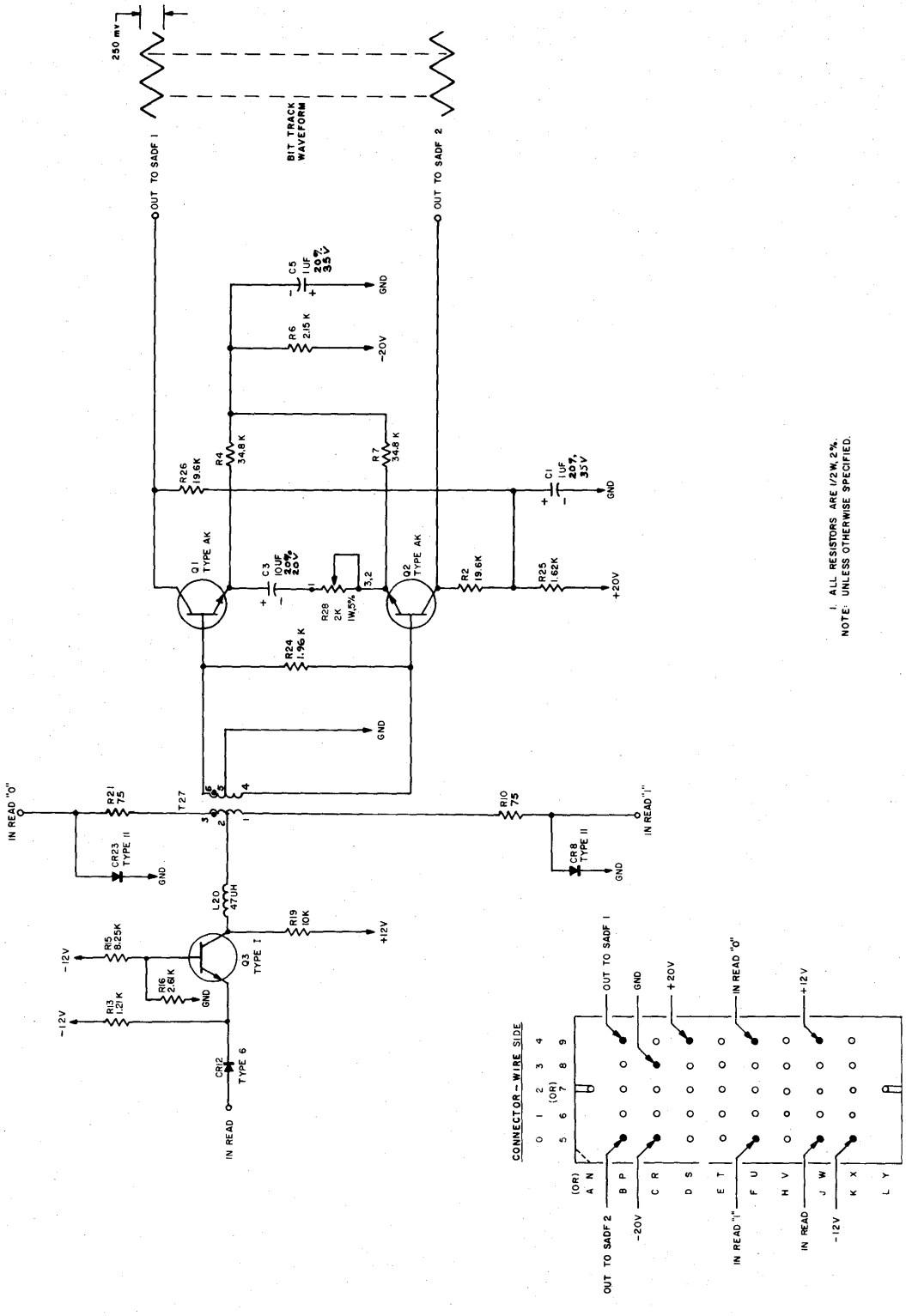


FIGURE 3.7-2
PRE-AMP SELECT II

PRE-AMP SELECT II

Refer to Figure 3.7-2.

The Pre-Amp II circuit (ARP 2) is the first stage of amplification for both the bit clock and word mark information. The circuit may be divided into two parts for purposes of explanation. The first part is the input switch which is used in conjunction with the clock center tap select circuits to select the proper bit or word mark track output. The second part is the output consisting of a push-pull amplifier operating class A.

The input switch, in quiescence, will have a false input and Q3 will be cut off. With Q3 cut off, diodes CR23 and CR8 will be forward biased holding the read inputs at approximately +.5V. This small positive voltage will keep the isolation diodes on the selected head reverse biased preventing any read signals being felt across the primary of transformer T27. In the amplifier section, both NPN transistors (Q1 and Q2) are conducting. Base drive is furnished by ground at the center tap of T27. The emitters are at a negative value from -20V. Variable resistor, R28, in the emitters of both stages is used to control the gain.

When the Disk Face Select Level (DFSS, DFSL/) becomes true, the base emitter junction of Q3 is forward biased and Q3 conducts. With Q3 conducting, the two "In Read" lines are held approximately -2.5V. When a clock head is selected by grounding the center tap, the signal from the disk is received at "0" and "1" read inputs of opposite polarity. The signal is coupled across T27 to the base of Q1 and Q2. The amplified output at Out 1 and Out 2 will be the same polarity as the input signal. The outputs are then sent to the Sense Amplifier DF for further amplification.

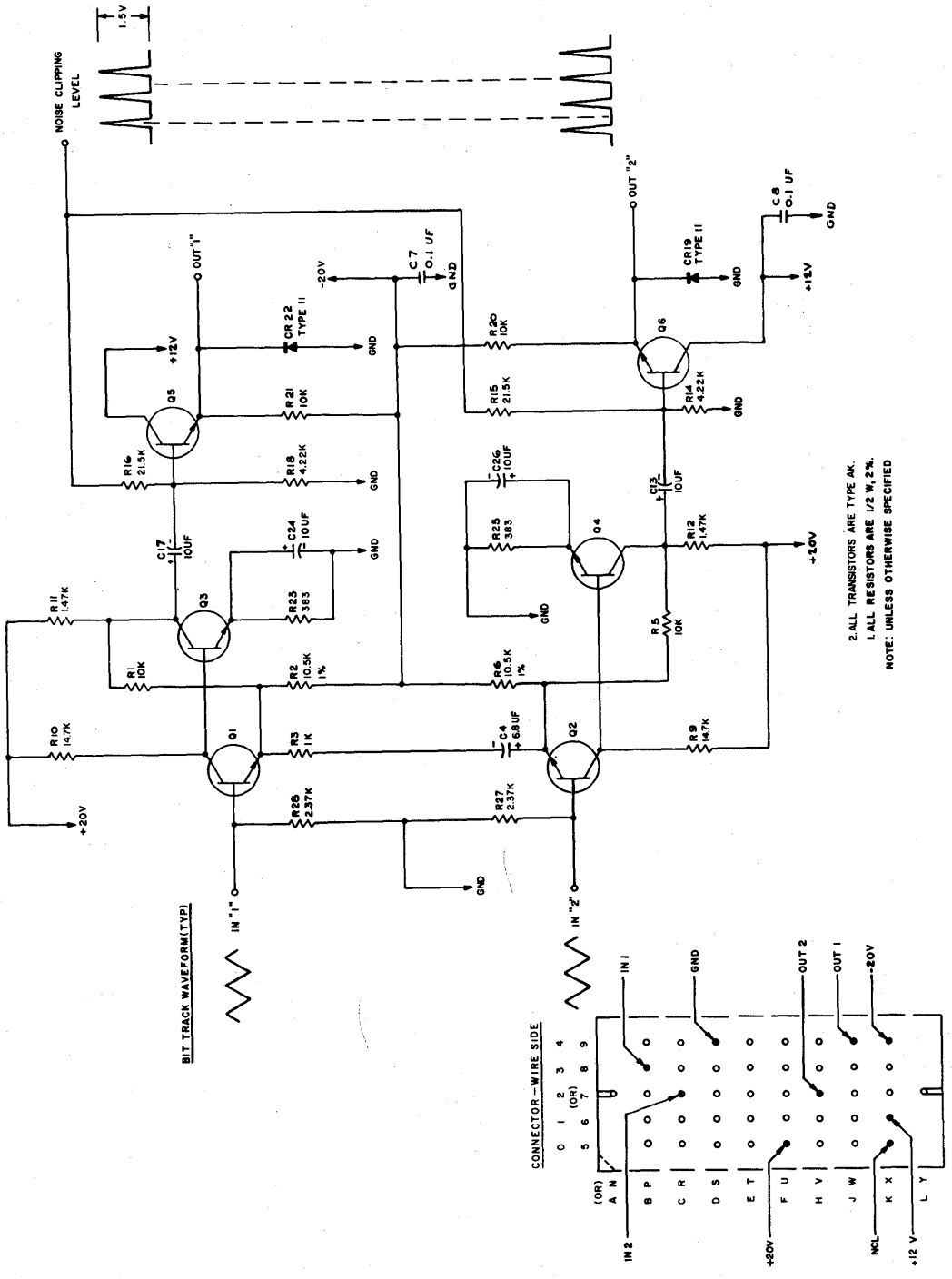


FIGURE 3.7-3
SENSE AMPLIFIER DF

SENSE AMPLIFIER DF

Refer to Figure 3.7-3.

The Sense Amplifier (AMSD) consists of two class A amplifiers with emitter followers. In quiescence all three transistors on each half will be in conduction with the outputs of Q5 and Q6 at a near ground potential.

The first two stages have an amplification factor of 20. The two out-of-phase saw-tooth inputs from the pre-amp circuit will become signals of about 4V on the base of the emitter follower. The output signal on the emitter will follow the positive base signal only with the negative signal clamped at ground. The noise clipping level is tied to ground at present. (If a small negative voltage were used, small positive noise spiked would be clipped out.) The output signals will be positive pulses of about 1.5V.

The Sense Amplifier DF circuit is used in both the Bit Clock circuits and the Word Mark circuits. The outputs of the Bit Clock Sense Amp are connected to an R2A gate which in turn is connected to the input of the Differentiator. Since one output of the Bit Clock Sense Amp represents a flux change on the clock track in one direction, the other output is for a flux change in the opposite direction. Combining the two produces a clock pulse for every flux change regardless of direction.

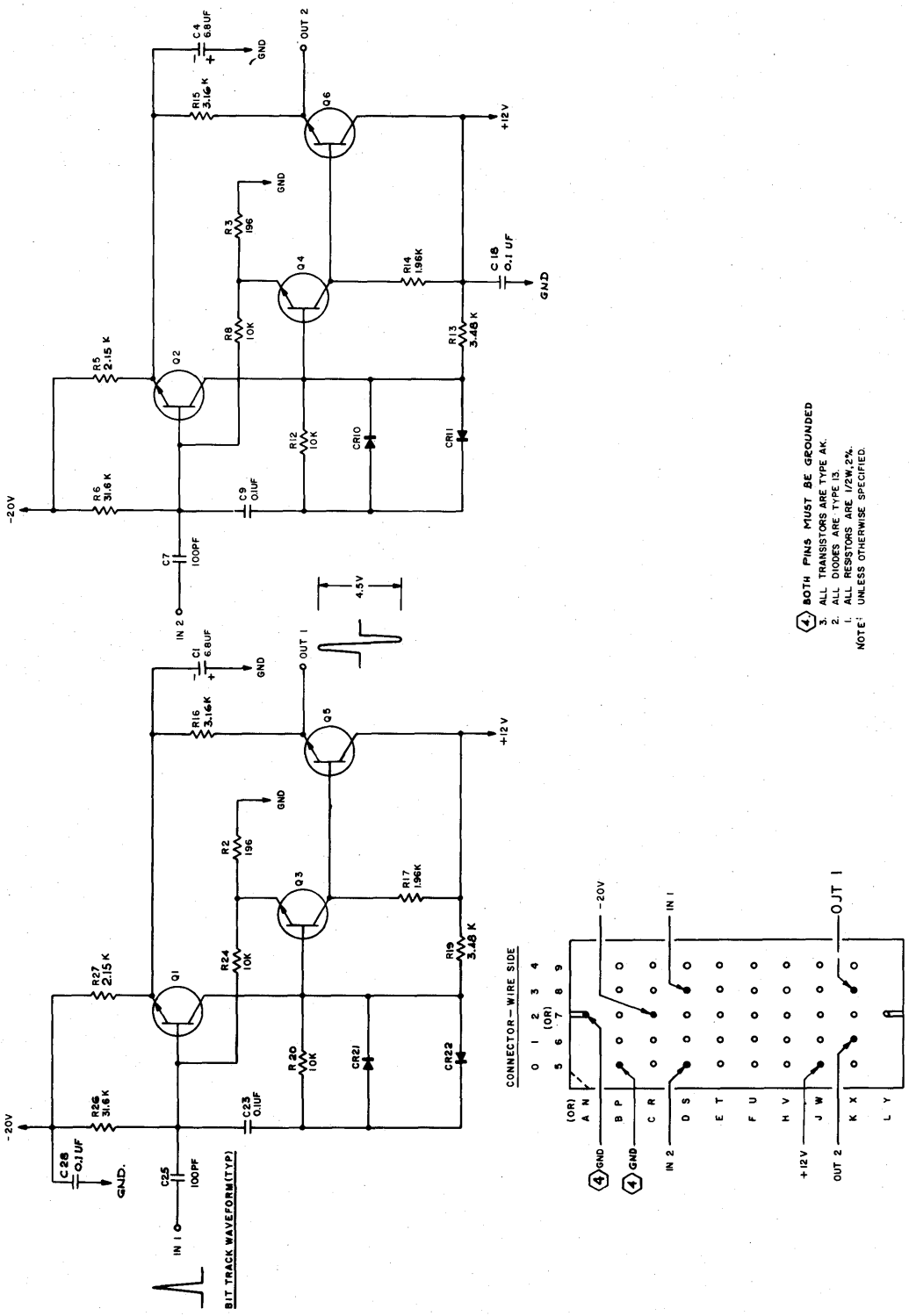


FIGURE 3.7-4
DIFFERENTIATOR

DIFFERENTIATOR

Refer to Figure 3.7-4.

The Differentiator circuit (AMPD) is used in both Clock circuits and also in the Information circuits (Section 3.8). The input to the Differentiator is a positive pulse of about 1.5V. The output is a 4.5V peak to peak clamped sine wave with the half wave point occurring at the peak of the input.

There are two circuits per package. Since both operate identically, only the first circuit is explained. Q1 and Q3 form a two-stage amplifier with Q5 being an emitter follower output. All three stages operate class A. Resistor R24 provides negative feedback to the base of Q1. The positive input signals are differentiated across C25 and R26 in the base circuit of Q1. Diodes CR21 and CR22 clamp the signal at the input to Q3 to square off the peaks of the differentiated signal. The clamped sine wave is amplified by Q3 and appears at the output from emitter follower Q5.

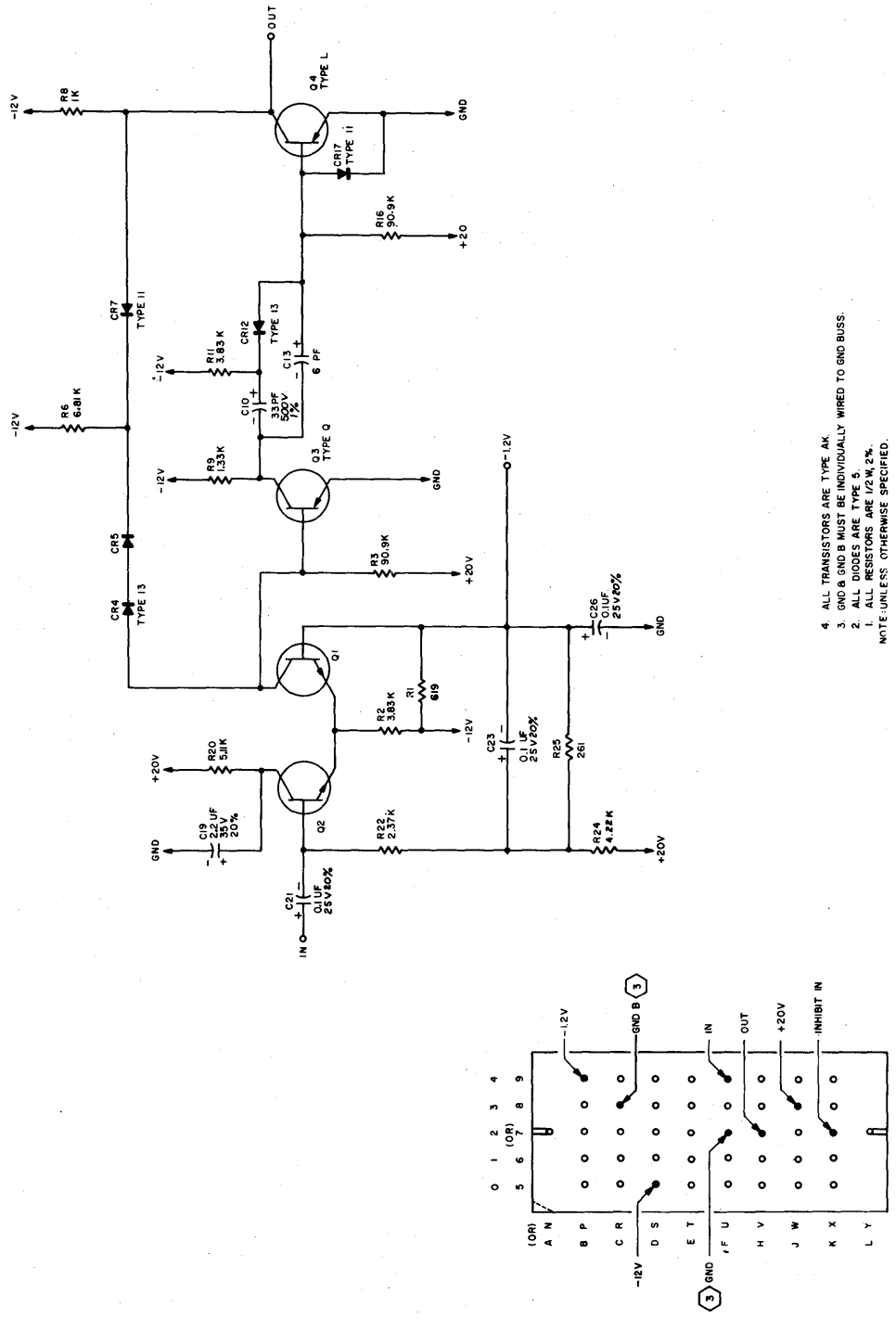


FIGURE 3.7-5
CLOCK GENERATOR

CLOCK GENERATOR

Refer to Figure 3.7-5.

The Clock Generator (CG A) is the Bit Clock output stage. The circuit will generate a 120 nanosecond negative pulse with an input from the Differentiator circuit ranging from .5 microseconds in zone 3 to 1.2 microseconds in zone 1. In quiescence, Q2 and Q4 are in conduction and Q1 and Q3 cut off. With Q4 conducting, the output is held at a near ground potential.

The positive portion of the input signal from the Differentiator will not affect the circuit. When the negative portion of the signal drives the emitter of Q2 more negative than -1.2V, the emitter base junction of Q1 is forward biased and Q1 conducts. Q1 will supply base drive to Q3 and Q3 will conduct. Q3 was being held off because, with CR7 forward biased, base drive could not be supplied from -12V through R6, CR5 and CR4.

When Q3 turns on, the positive going change across C13 and C10 cuts off Q4. Q4 will remain off for the RC time constant of 120 nanoseconds. Q1 and Q3 will remain on for the duration of the negative half of the input signal; however, this will have no effect on Q4 as base drive from R11 and CR12 will turn on Q4 again after 120 nanoseconds.

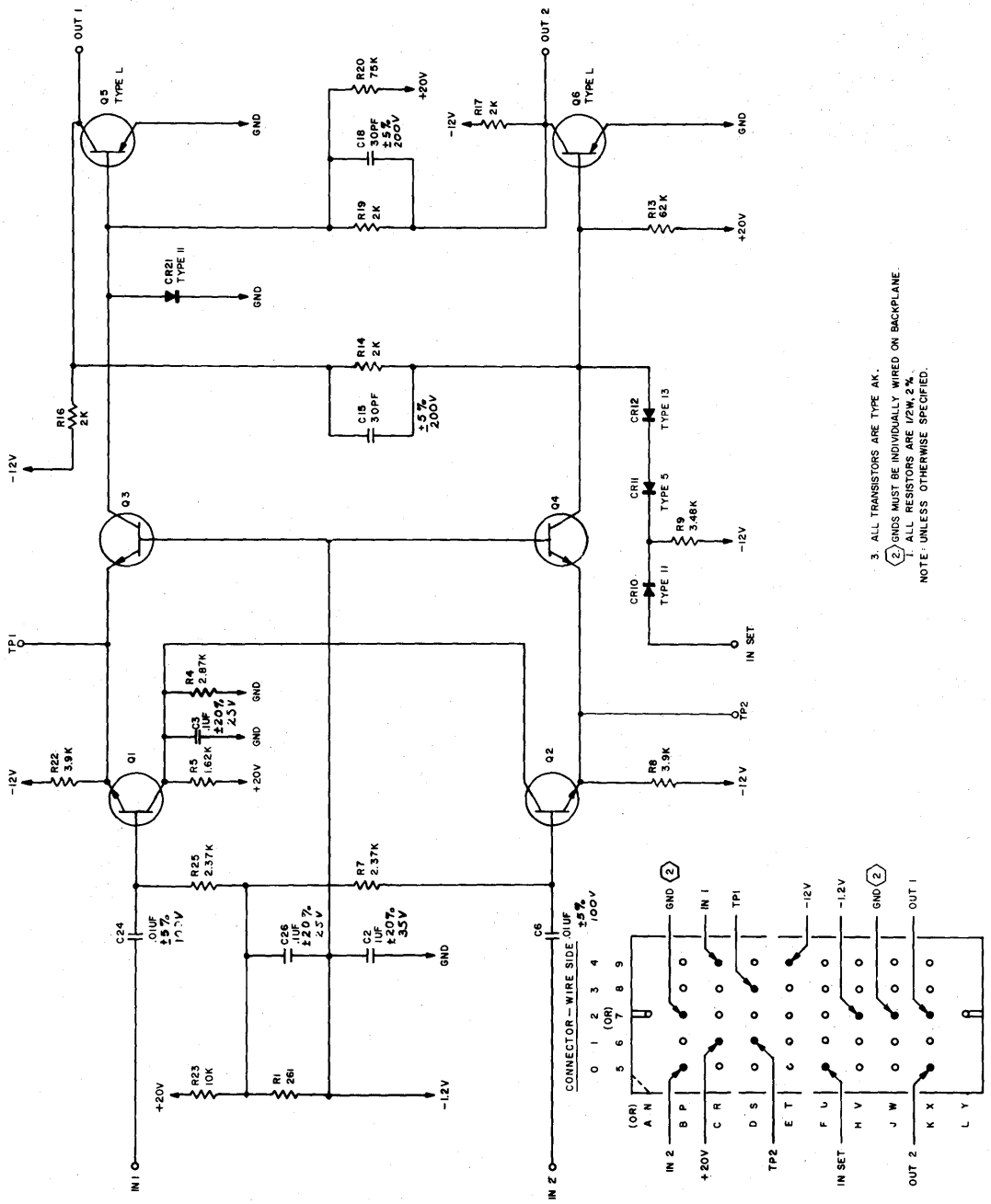


FIGURE 3.7-6
THRESHOLD DETECTING FLIP-FLOP

THRESHOLD DETECTING FLIP-FLOP

Refer to Figure 3.7-6.

The Threshold Detecting Flip-Flop (FFTH) is used in the word mark clock circuit and the information read circuit. The inputs to the TDFF come from two Differentiator circuits.

Quiescent Condition (Reset)

Q1, Q2, Q6 - ON
Q3, A4, Q5 - OFF

With Q6 on, the Out 2 level is false. This false level is coupled through R19 to the base of Q5 keeping Q5 cut off and a negative output at Out 1.

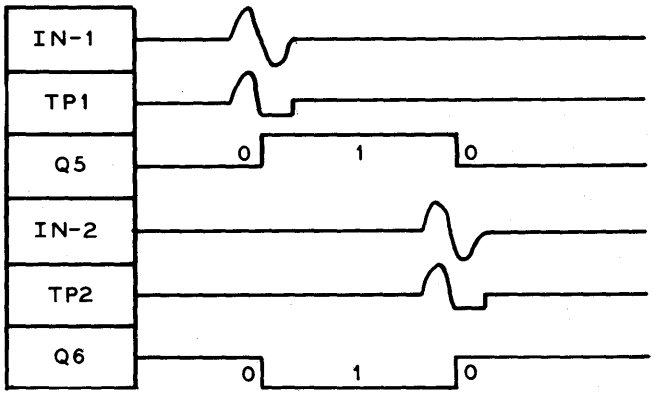


FIGURE 3.7-7
TDFF WAVEFORMS

Figure 3.7-7 shows the inputs from the Differentiators to set the flip-flop first to "1" and then to "0". During the negative portion of the differentiated input to In 1, the emitter of Q1 will go more negative than the -1.2V on the base of Q3. Q3 will conduct and furnish base drive to turn on Q5. The near ground potential at Out 1 will remove base drive to Q6 and Q6 turns off. Out 2 will be negative true for "1".

The input to In 2, from the other Differentiator, would make Q4 conduct. Q4 conducting would supply base drive to turn on Q6. When Q6 conducts, the positive rise at the collector will remove base drive to Q5. Q5 will turn off. The negative voltage at the collector of Q5 supplies base drive to Q6 keeping it on. The flip-flop is now back in the "0" state.

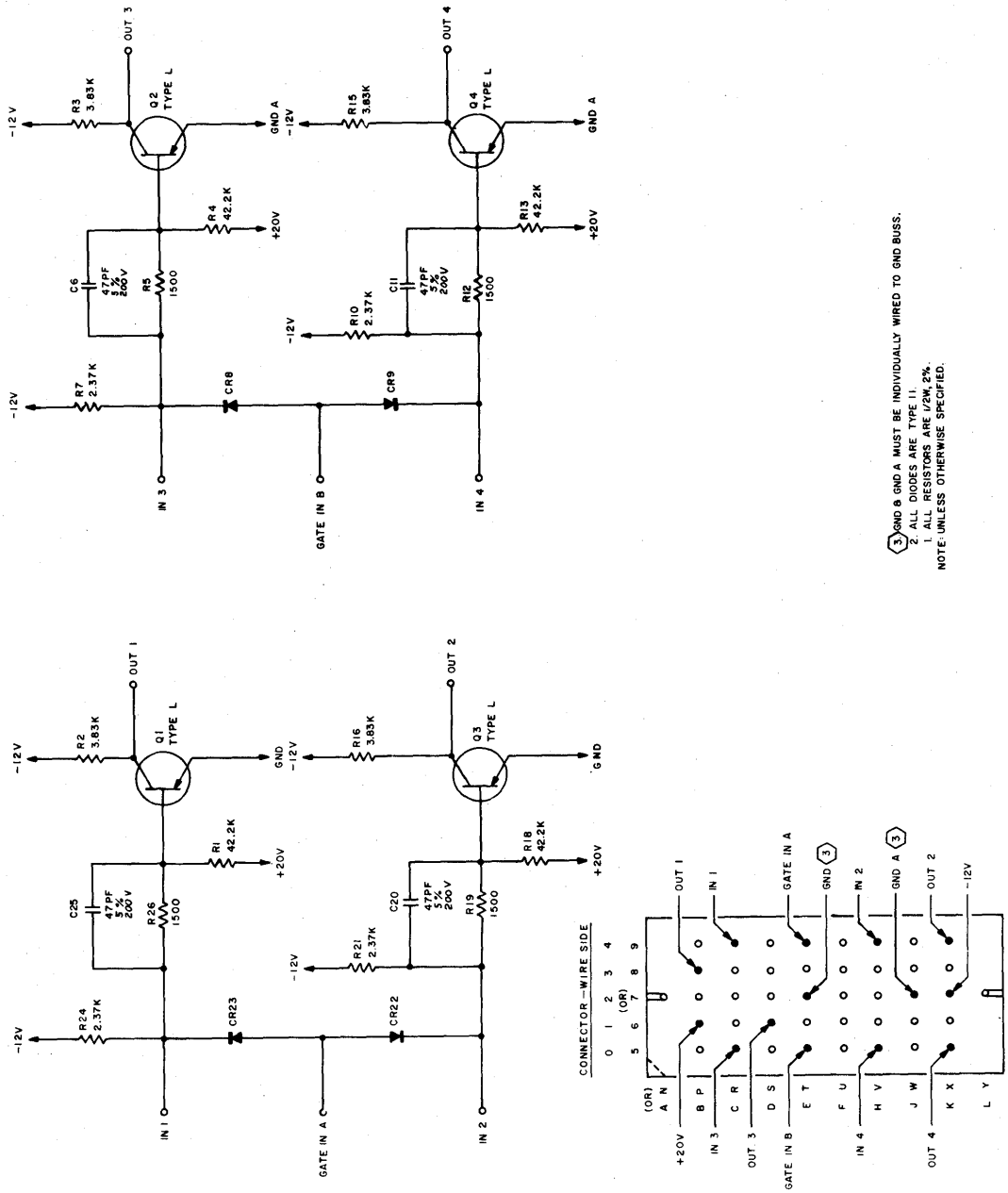


FIGURE 3.7-8
FLIP-FLOP LINE DRIVER

FLIP-FLOP LINE DRIVER

Refer to Figure 3.7-8.

Flip-Flop Line Drivers (AMLD) are used as the output stage for both the information circuitry and the word mark circuitry in the S.U. The inputs to the Line Driver are the outputs from the TDFF with the "0" side of the TDFF connected to "In 1" and the "1" side to "In 2". The outputs are ASRL from "Out 1" and ASRL/ from "Out 2". The shunt and condition on both inputs at Gate In A is connected to the Module Select Level (MØnL).

When MØnL is false, if either input is true, the diode connected to that input (CR22 or CR23) shunts the current so that both Q1 and Q3 will be cut off and both outputs will be true.

When MØnL is true, the diodes (CR22, CR23) are reverse biased and allow the inputs to control Q1 and Q3.

3.8 INFORMATION CIRCUITS

The information read circuitry is used to develop true and false levels to the E.U. corresponding to the signals recorded on the disk face. In order that a level to the E.U. may correctly represent a bit, a zero reference must be established. When SPFF occurs, the outputs to the E.U. (IRAL, IRAL/) represent a "0". After SPFF is reset, there will be no change in IRAL and IRAL/ unless a "1" bit is read from the disk, then the levels will switch. The next change detected from the disk will represent a return to the "0" condition.

The heads in the Module are grouped into 12 sets of 100 heads. There are 100 heads in one zone, three zones per disk and four disks per Module. The outputs HRWL-nn and HRWL/-nn from each head set are connected to a Write Driver circuit. The Head Select Level, HSDL-nn, will go to the center taps of 12 heads, one in each head set. The disk and zone levels will select one head set.

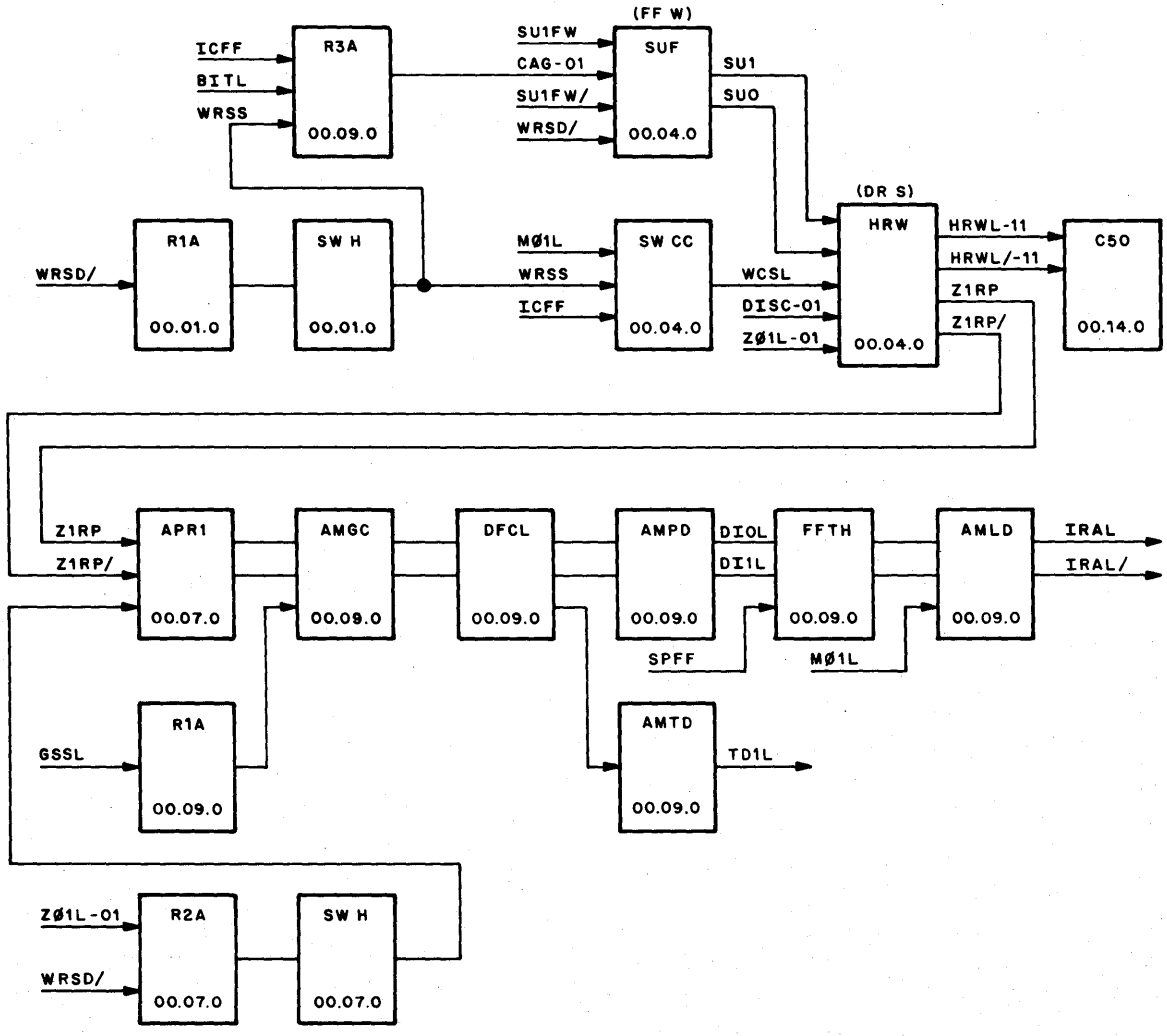


FIGURE 3.8-1
INFORMATION CIRCUITS

WRITE

The bit configuration of the information to be recorded will determine changes of current flow through the head winding. The head switching diodes of only one head are forward biased.

The selected Write Driver will perform this function when the Storage Write level, WRSD, is true from the E.U. The direction of current flow in the head to write a "1" or a "0" is determined by SUF which reflects the state of SUlFw in the E.U. The write current is supplied by the Write Current Control circuit.

READ

During Read, the selected head will produce a negative or positive going signal depending on the direction of flux change on the disk.

The four Write Drivers for each zone are connected to a Pre-Amp Select I (APR 1). The input lines are called Z1RP, Z1RP/, Z2RP, Z2RP/ and Z3RP, Z3RP/ depending on the zone. The outputs from the APR 1 go to a Gain Controlled Sense Amp (AMGC).

The output of the AMGC goes to the Disk File Clipper (DFCL) which will clip the negative portion of the signal and square up the positive portion. The next stage, the Differentiator (AMPD), will differentiate the input signal. The negative portion of the output signal will set or reset the TDFF. The state of the TDFF conditions the information levels, IRAL and IRAL/, to the E.U.

DETAILED DESCRIPTION OF READ/WRITE CIRCUITS

There are 1200 heads in each Module with up to five Modules connected to each E.U. The heads are connected in a 100 x 12 matrix considering only one Module. The 100 represents the 100 center tap select lines sent to all five Modules from the E.U. To complete the selection, one of 12 Write Driver Select circuits must be enabled in a particular Module.

There are 13 heads per assembly. Each head is isolated by diodes to enable the selection process to be performed. The 13 heads are connected in parallel to another pair of isolation diodes. These isolation diodes are then connected in parallel with seven other head assemblies (four on each disk face) to a Write Driver.

Figure 3.8-2 shows some of the information Read/Write circuitry. With a false level applied to one of the 100 Center Tap Select Circuits (DRCH),

both transistors will be turned on and +12V will be applied to the center taps of 12 heads in each Module. All other Center Tap Select circuits will have a true input causing their outputs to be at ground. Eleven of the 12 heads will be connected to Write Drivers that are not selected. The output of an unselected Write Driver is +20V. This will keep the head diodes reverse biased and prevent any reading or writing these heads.

The 12 Write Driver circuits each select one set of 100 heads. The operation of the Write Driver differs for Read and Write and is discussed separately.

During either operation, the zone and disk inputs will be true to select the Driver. During Write, the Bit "1" and "0" inputs will determine which side of the driver conducts. If the "0" input is true, Q1 and Q4 will turn on. With Q4 on, the collector will start to go negative. This will forward bias one of the head isolation diodes and allow current to flow through half the head winding, making the collector of Q4 about +11.2V. The current required to write on the disk is approximately 125 ma. This current is supplied from the Write Current Control Circuit (SWCC). The Write Current Control Circuit is turned on in the desired Module for the Active word (ICFF at Interlace). This will supply 125 ma from -12V to the Write Driver. The Write Driver will remain in this state until the Bit FF changes states. With the Bit FF in the "1" state, the "1" side of the Write Driver turns on and the "0" side off. This will change the direction of current flow through the selected head and a flux change is written on the disk.

During Read, the Write Driver is again used to select the proper head. The Write Current Control Circuit is turned off. Both sides of the Bit FF are forced true so both sides of the Write Driver will be turned on. With both sides of the Write Driver on, both isolation diodes of the selected head are forward biased. The Pre-Amp circuit is selected by a false input. This will turn Q4 off and allow current to flow from the Write Driver to the center tap of the Pre-Amp transformer. Each side of the Write Driver can supply about 7 ma of current. This current is then divided with approximately half going to the head center tap and half going to the Pre-Amp transformer. The read signal is transferred from the selected head to the Pre-Amp transformer due to the fact that the small DC bias current flowing through the diodes causes them to have a low AC impedence. All unselected diodes are reverse biased, presenting a very high impedence to the AC signal.

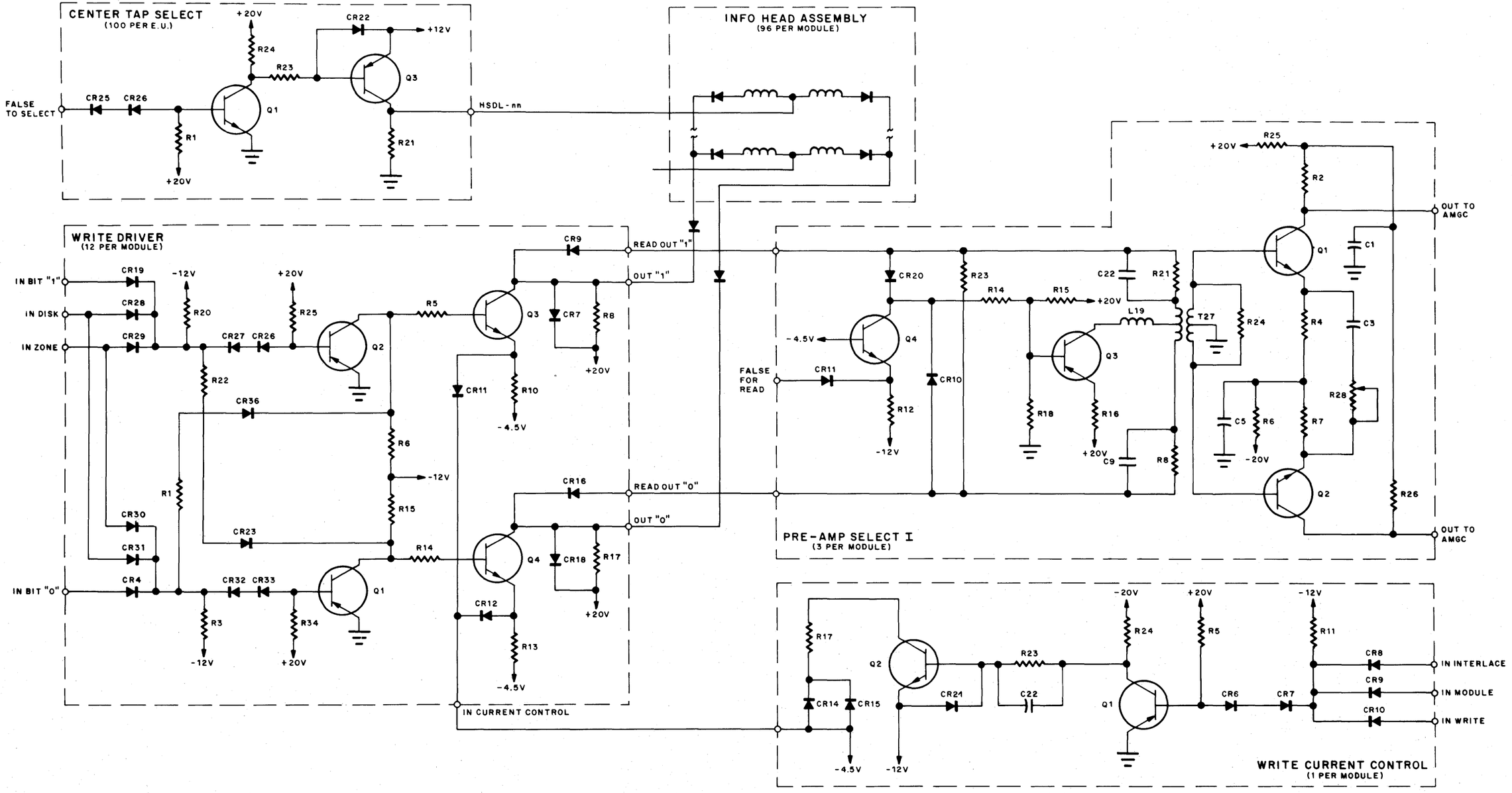


FIGURE 3.8-2
INFORMATION
READ/WRITE CIRCUITRY

FIGURE 3.8-2
INFORMATION
READ/WRITE CIRCUITRY

SPECIAL CIRCUITS

Below is a list of the circuits described on the following pages:

Figure 3.8-3	Bit Flip-Flop (SUF)	FF W
Figure 3.8-4	Write Current Control	SWCC
Figure 3.8-5	Write Driver	DR S
Figure 3.8-6	Pre-Amp Select I	APR 1
Figure 3.8-7	Gain Controlled Sense Amp	AMGC
Figure 3.8-8	Disk File Clipper	DFCL
Figure 3.8-9	Gain Threshold Detector	AMTD

For circuit descriptions of the Differentiator (AMPD), Threshold Detecting Flip-Flop (FFTH) and Flip-Flop Line Driver (AMLD), see Section 3.7.

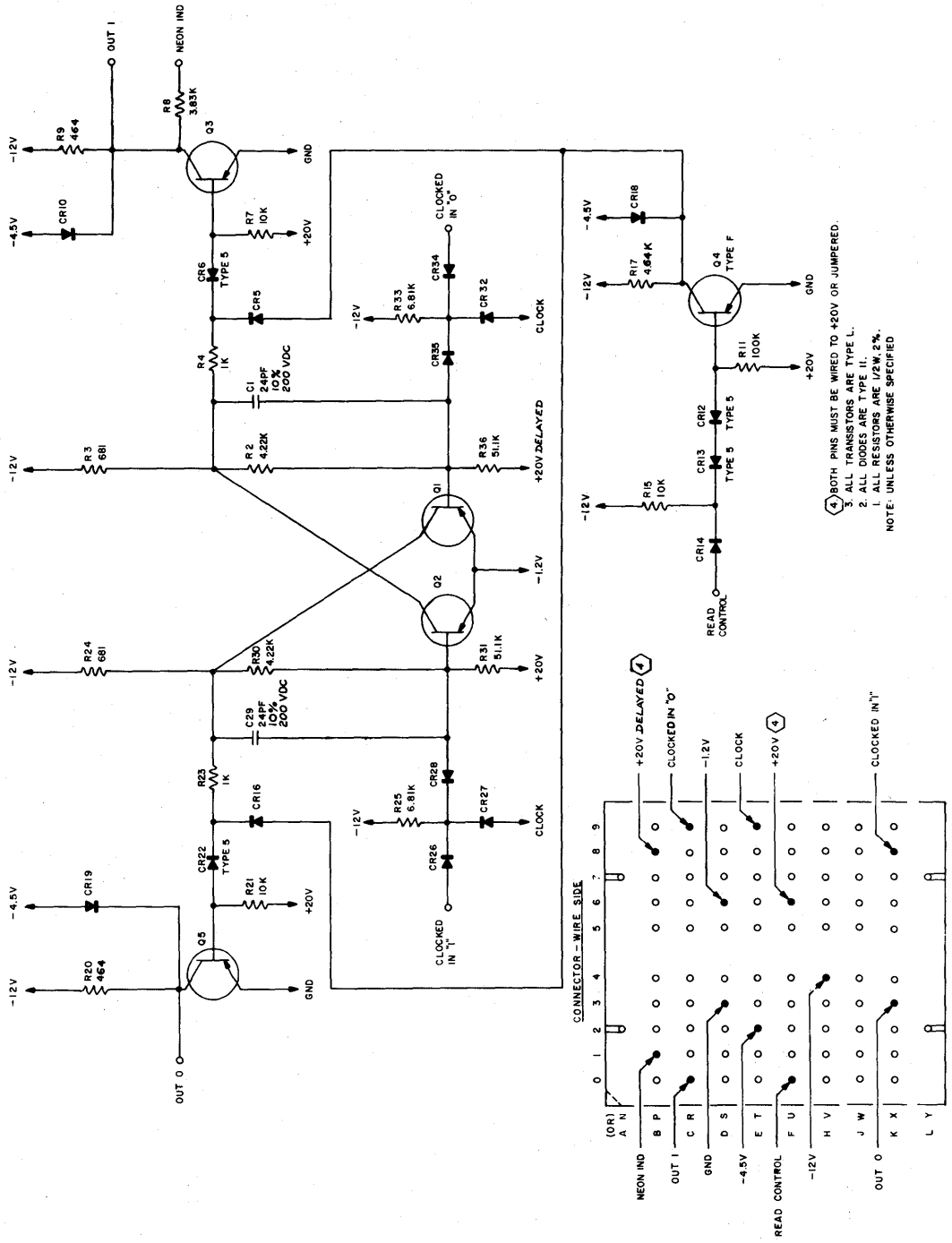


FIGURE 3.8-3
BIT FLIP-FLOP

BIT FLIP-FLOP

Refer to Figure 3.8-3.

The Bit Flip-Flop (FF W) is a modified 20 - 70 flip-flop. The modification consists of two parts. The first is the removal of the delay lines and complementing diodes. The second part is the addition of a single transistor circuit which is used to make both outputs true during Read operations. The Bit Flip-Flop controls the state of the selected Write Driver during both Read and Write operations. During a Write, the flip-flop will follow the state of SU1Fw in the E.U. and control which side of the Write Driver is turned on. During a Read, the output transistors of the Bit Flip-Flop are turned off making both outputs true. This will turn both sides of the selected Write Driver on.

The operation of the flip-flop circuit will not be explained here since it is so similar to the operation of the standard B5000 flip-flop.

The Read Control input will be true for Read turning Q4 on. This will shunt base drive to Q3 and Q5 and both transistors will remain off. Both outputs will be true.

WRITE CURRENT CONTROL

Refer to Figure 3.8-4.

The Write Current Control Circuit (SWCC) is a constant current source for the Write Driver. During a Write operation, the Write Current Control Circuit is turned on to supply 125 ma to the selected Write Driver.

In the quiescent state, both transistors are off. Q2 is held off by the drop across diode CR21. During a Write operation, when all inputs are true, base drive is supplied to Q1. With Q1 on, base drive is supplied to Q2 turning it on. Q2 will remain on as long as base drive is furnished by Q1. Q2 will supply a constant current from the -12V supply despite variations in load. The output is clamped at -4.5V by CR14 and CR15.

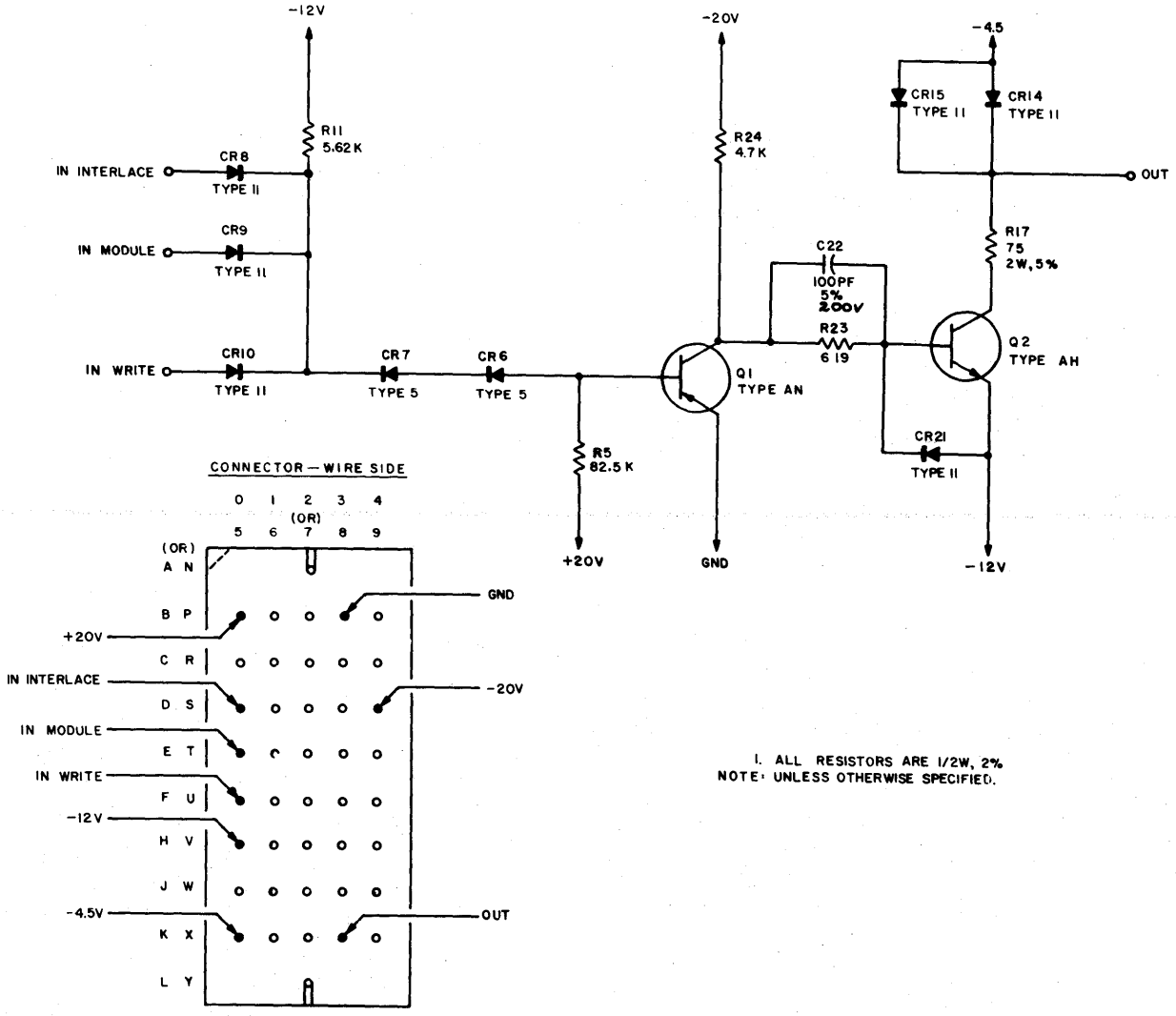


FIGURE 3.8-4
WRITE CURRENT CONTROL

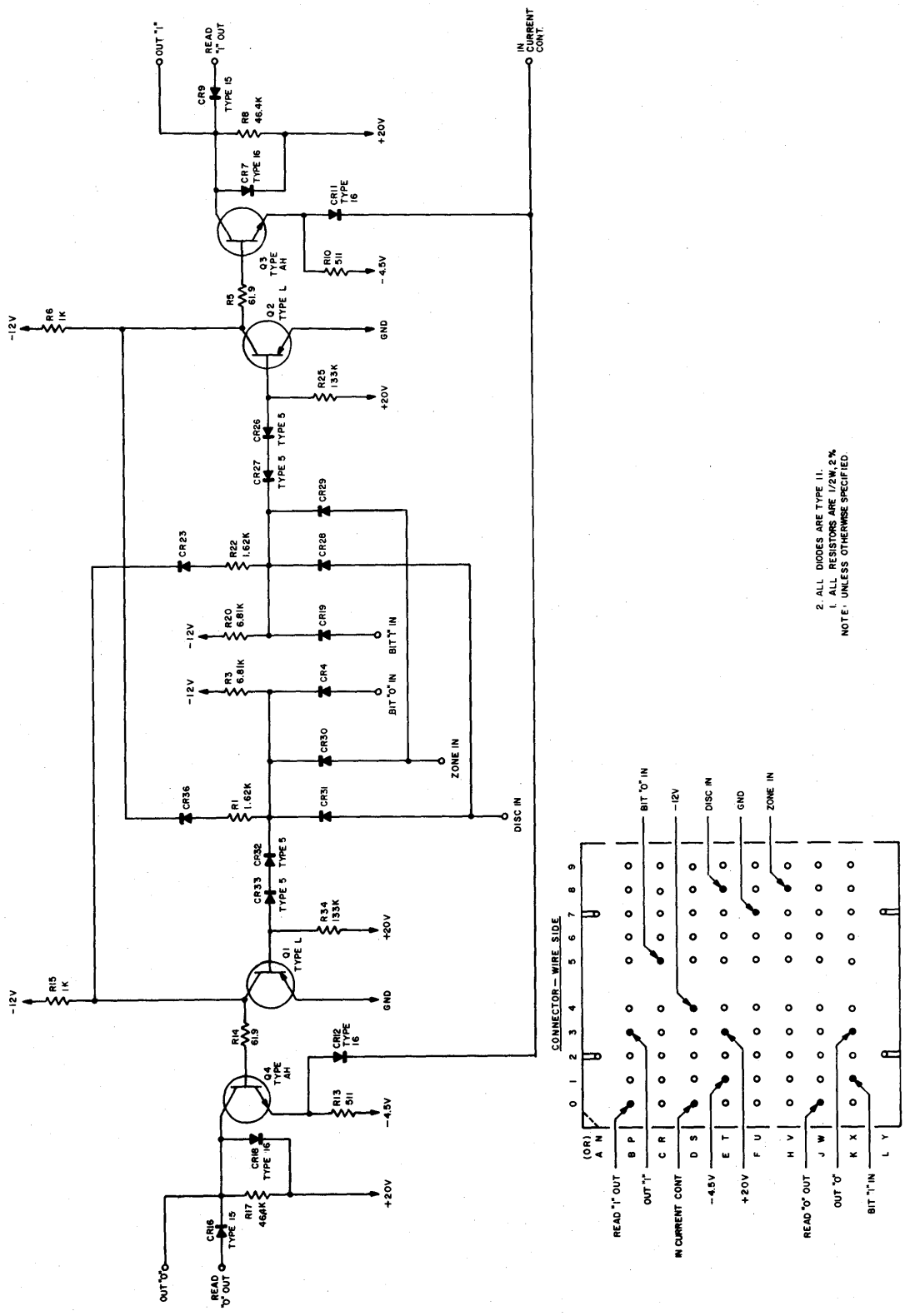


FIGURE 3.8-5
WRITE DRIVER

WRITE DRIVER

Refer to Figure 3.8-5.

The Write Driver (DR S) controls current flow through the selected head. Each side of the Write Driver may be considered as a separate driver with three modes of operation. The driver may be off and have an output of +20V which will reverse bias the head diodes. The driver may be on the write status where the output will be supplied from the constant current source. In this mode of operation, 150 ma of current would flow through half of the head to write on the disk. The third mode of operation would be during read status. The driver would be on and supply 3.5 ma to the head and 3.5 ma to the Pre-Amp. This will allow the read signals from the disk to be coupled through the Write Driver into the Pre-Amp.

In the quiescent state, all four transistors will be cut off and both the "1" and "0" outputs will be +20V. The Current Control input has no effect.

During a Write operation, with true inputs to Disc In and Zone In, the driver will follow the inputs from the Bit Flip-Flop. If the Bit FF is reset, the three input AND gate for the "0" side would have a true output allowing Q1 to turn on. With Q1 on, base drive is supplied to transistor Q4 turning it on. Since this is a Write operation, the current path through the Write Driver is from the -12 volts in the current control package, through Q4, out through half the selected head winding to the +12 volts in the center tap select circuit. The current flow will remain in this direction until the Bit FF changes states.

When the Bit FF is set to the one state, the Bit inputs to the Write Driver will switch and the "0" side will turn off and the "1" side will turn on. The current path will now be from the Current Control input, through Q3, through the opposite half of the selected head to the center tap select circuit. This will change the direction of current through the head, thereby writing a flux change on the disk. The coupling diodes between the two sides of the driver supply the initial current surge during the switching time.

During a Read operation, both inputs to the Write Driver from the Bit FF are held true. This allows both sides to turn on. The current control circuit is not turned on so current through Q3 and Q4 is supplied from the -4.5V through the emitter resistor of each transistor. This will forward bias the head diodes and the Read output diodes of both sides.

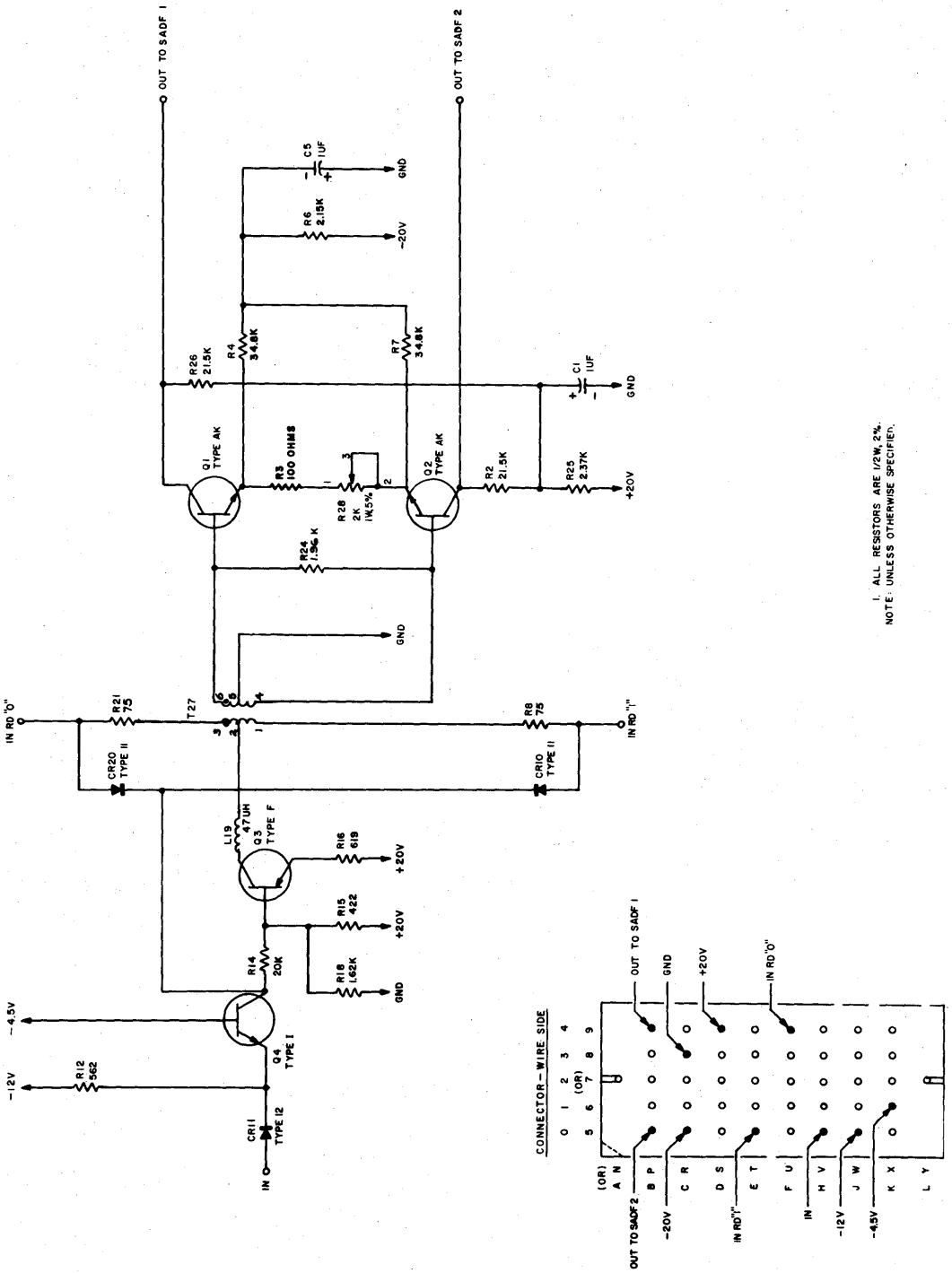


FIGURE 3.8-6
PRE-AMP SELECT I

PRE-AMP SELECT I

Refer to Figure 3.8-6.

The Pre-Amp Select I circuit (APR 1) is connected to the output of the four Write Drivers for one zone. It is the first stage of amplification of the read signal from the head.

During a Write operation, the amplifier is disabled by a true input to diode CR11. This will turn Q4 on and -4.5V on diodes CR20 and CR10 will prevent any signals from being felt across transformer T27. Transistor Q3 will be on at all times with base drive supplied from the +20V divided through R15 and R18 to ground.

The Pre-Amp is enabled by a false level at CR11, removing base drive from Q4, turning it off. With Q4 off, CR10 and CR20 are reverse biased. Q3 will supply a current path to +20V from the output of the Write Driver. Read signals from the information head are felt across the 1:2 transformer T27. These read signals are amplified by Q1 and Q2, which is a single stage amplifier with gain control in the emitter circuit. The output signals will be out of phase.

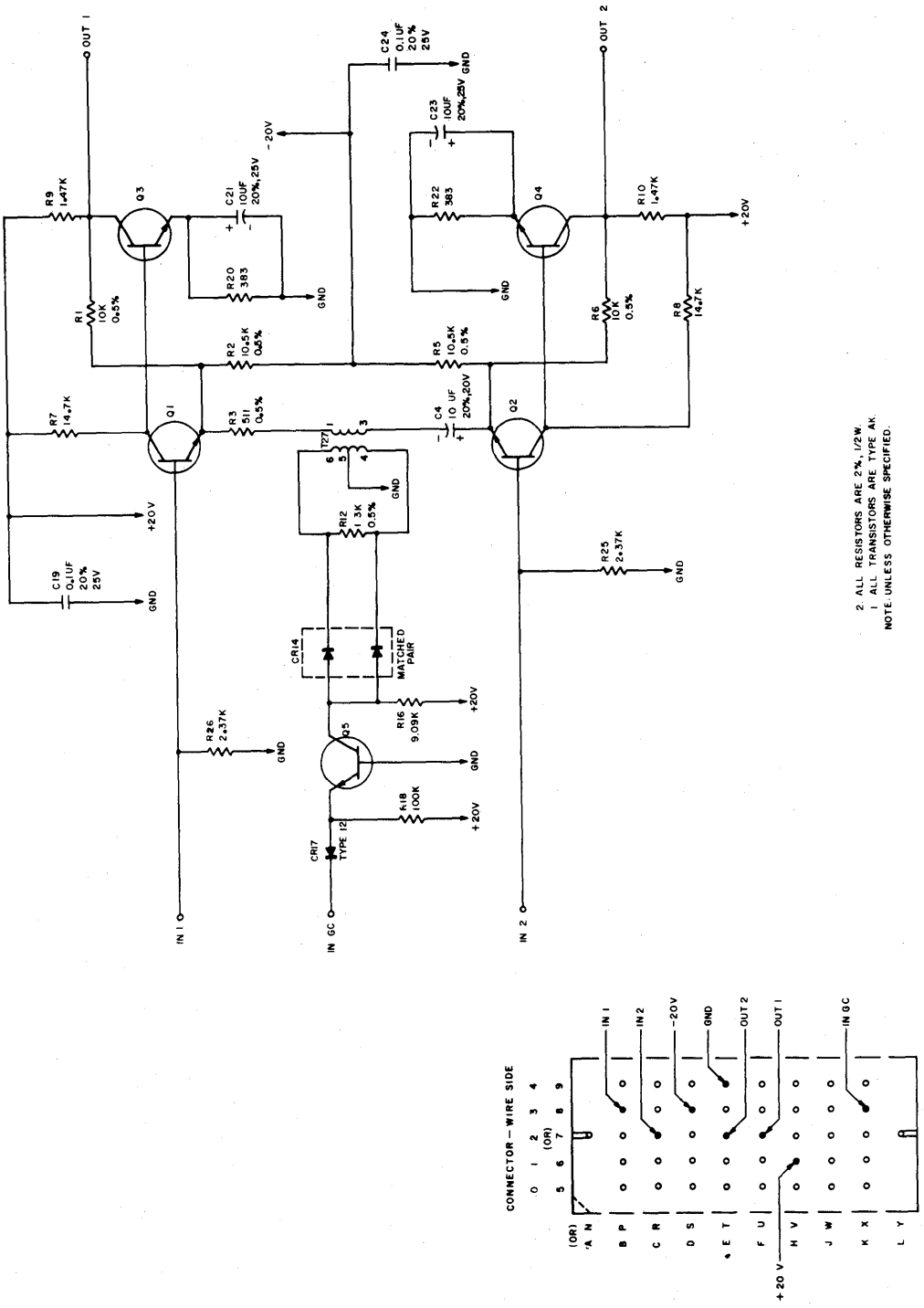


FIGURE 3.8-7
GAIN CONTROLLED SENSE AMP

GAIN CONTROLLED SENSE AMP

Refer to Figure 3.8-7.

The Gain Controlled Sense Amp (AMGC) consists to two two-stage class A amplifiers with a common circuit which provides two-step gain control. The output signals from the Sense Amp will be directly out of phase and approximately 3V peak to peak.

The two-step gain control circuit consists of capacitor C4, transformer T27 and resistor R3. Gain control is accomplished by changing the impedence of T27 secondary. When transistor Q5 is cut off, the diode pair CR14 is forward biased and current will flow from ground through both sides of T27 primary to +20V. With current through the primary of T27, the primary of T27 is almost shorted. This reflects a low impedence in the secondary and the gain of the amplifier is high. When transistor Q5 is conducting, the diode pair is reverse biased and there is no current flow in the primary of T27. The primary of T27 is loaded by R12 which reflects a high impedence into the secondary and the gain is low.

The Gain Select Level (GSSL) is connected to In GC to control Q5. When GSSL is true, the emitter of Q5 will go negative to turn Q5 on for low gain. When GSSL is false, transistor Q5 will turn off and the amplifiers will operate at high gain.

DISK FILE CLIPPER

Refer to Figure 3.8-8.

The Disk File Clipper circuit (DFCL) will clip the negative portion of the signals to the two inputs and produce positive pulses at Out 1 and Out 2A. A third output at Out 2B is a replica of the input signal at In 2. This output is sent to the Gain Threshold Detector circuit.

Q3 and Q1 are in two identical clipper circuits which pass the positive portion of their respective input signals. -1.2V is connected to the Noise Clipping Level (NCL) input which will hold the bases of Q1 and Q3 at -.5V with no signals at the inputs. The emitter outputs are clamped at approximately -.3V by diodes CR1 and CR9. This will keep Q1 and Q3 off until a positive input is received. When the positive excursion of the input signal reaches +.5V, the associated transistor will turn on and the output will go positive. When the input returns to +.5V, the transistor is turned off again. With an input signal of 3V peak to peak, the output will be a 1.5V positive pulse.

Transistor Q2 is an emitter follower circuit. The output of this circuit will be the same as the input at In 2 except for the voltage drop across R23.

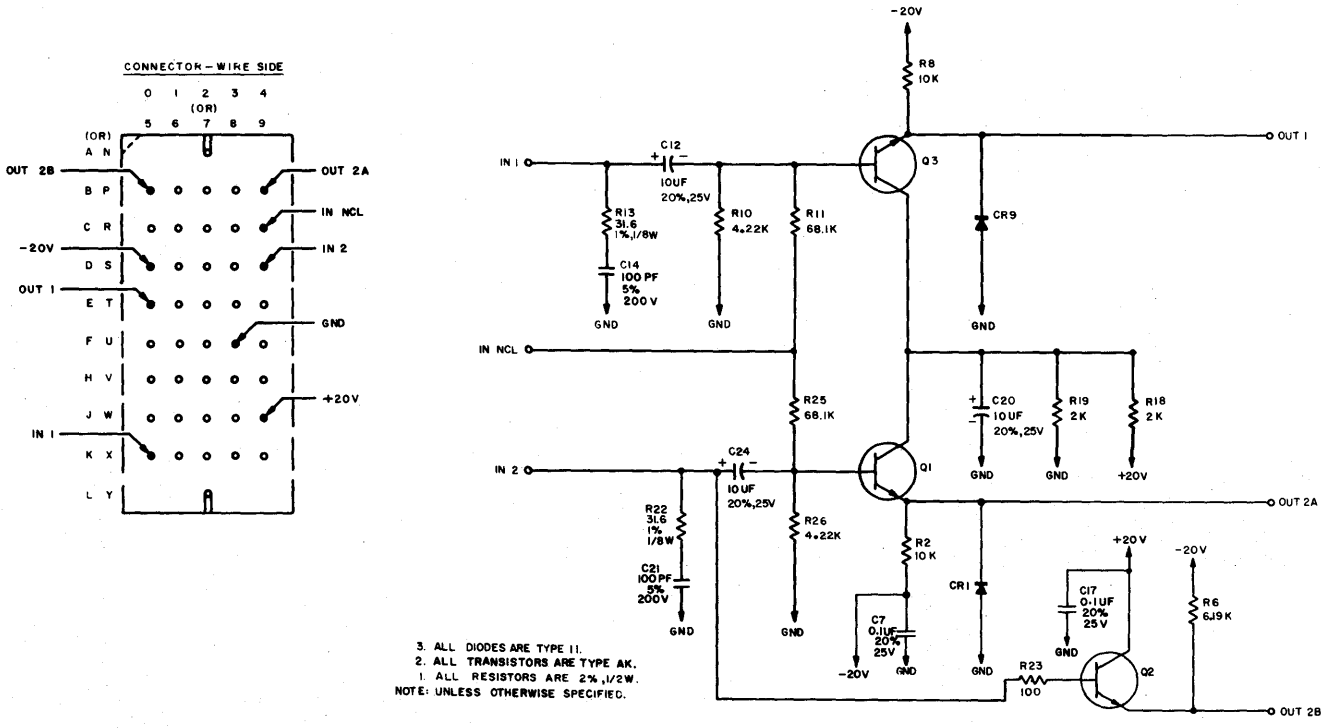


FIGURE 3.8-8
DISK FILE CLIPPER

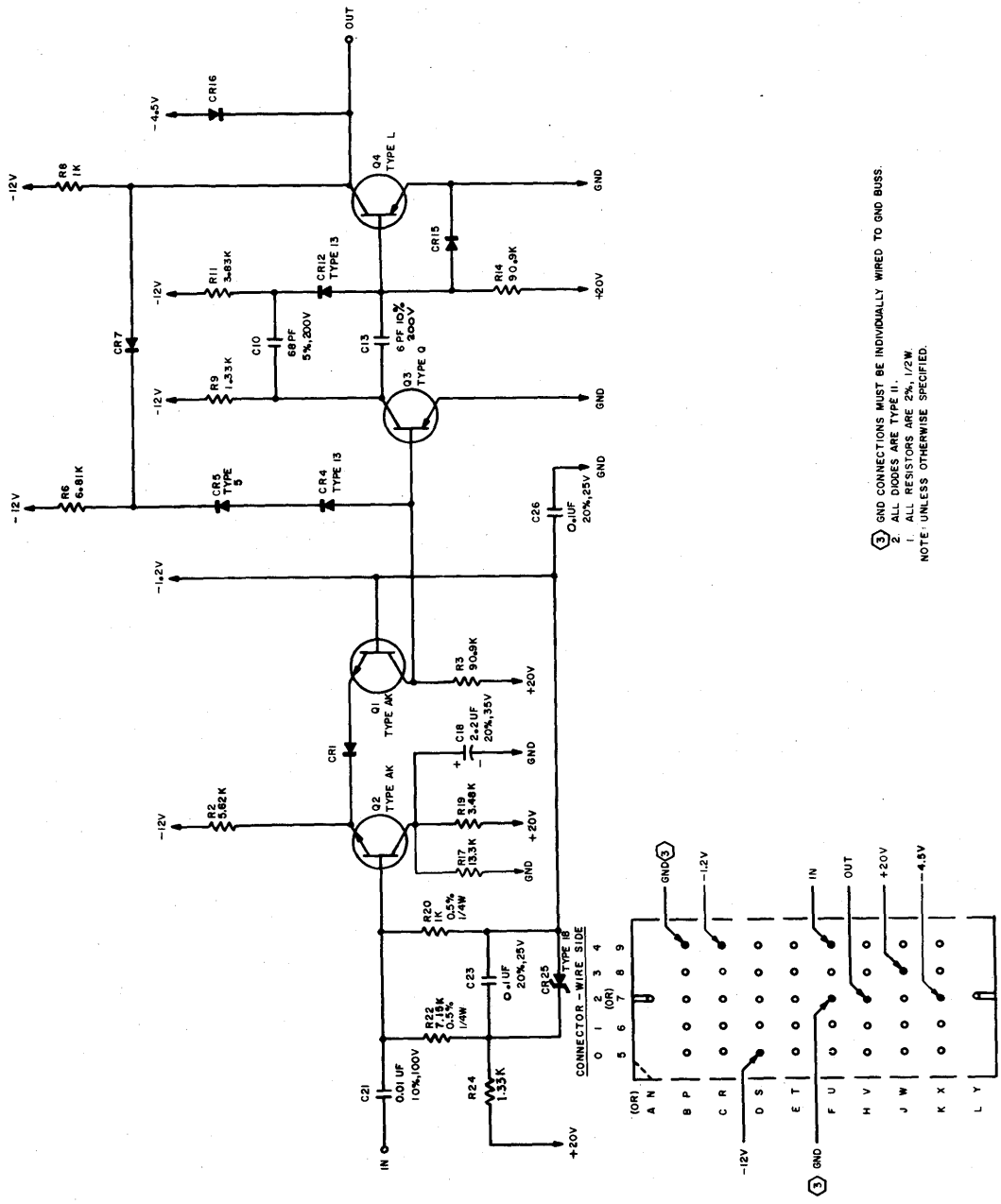


FIGURE 3.8-9
GAIN THRESHOLD DETECTOR

GAIN THRESHOLD DETECTOR

Refer to Figure 3.8-9.

The Gain Threshold Detector (AMTD) is used to sense the incoming signal for amplitude. This is accomplished by establishing a threshold of -1.2V. If the signal is higher than the threshold level of -1.2V, a multi is fired emitting 150 nanosecond negative pulses. These pulses are used in the E.U. to set a flip-flop which will hold the AMGC in normal gain. If the input signal is less than the threshold level, the multi is not fired and the Sense Amp gain will switch to high for a Read operation.

The Threshold Detector consists of two sections. The first section is an emitter follower and a base clamped amplifier which establishes a threshold for the second section. The second section is the output multi section which produces the 150 nanosecond negative pulses.

In the quiescent stage, Q1 and Q3 are cut off while Q2 and Q4 are turned on. Q2 is on due to the slight positive potential on the base. The emitter of Q2 is held at approximately ground keeping CR1 reverse biased and Q1 cut off. Q4 will be on due to the base drive furnished from the -12 volts through R11 and forward biased diode CR12. With Q4 on, the output will be at a near ground potential. Diode CR7 will be forward biased with approximately -.5V on its cathode. This will hold the base of Q3 at +.5V keeping it cut off.

With an input signal of approximately 3V peak to peak applied to the base of Q2, the transistor will conduct harder during the positive portion, which has no effect. However, with a negative signal of more than the threshold established at -1.2V by Q1 base, CR1 is forward biased turning Q1 on. The collector of Q1 goes negative and Q3 is turned on. The positive change on the collector of Q3 is coupled through C13 to cut off Q4. This produces a -4.5V output pulse. The duration of the output pulse is determined by the charge time of C13 through R11 and is approximately 150 nanoseconds.

✓INDEX - SECTION IV

✓Changes or additions since last issue.

4.1 PEDESTAL, BULKHEADS, SHAFTS AND DISKS

Refer to Figure 4.1-1.

The Storage Module is physically separated into two disk chambers mounted on opposite sides of a pedestal. This in turn is mounted on a base assembly provided with casters.

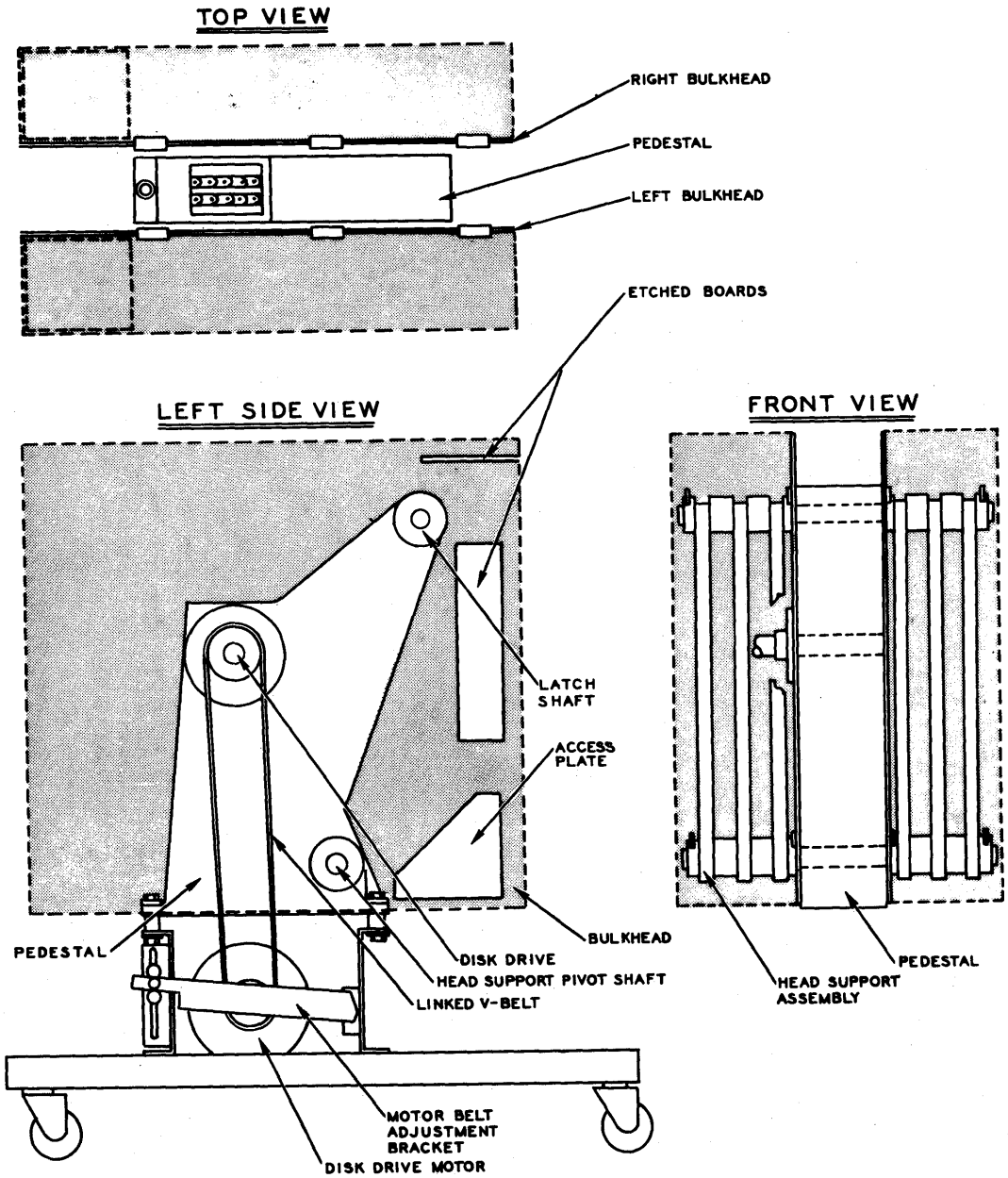


FIGURE 4.1-1
STORAGE UNIT MECHANICAL ASSEMBLIES

The purpose of the pedestal is to provide a rigid support for the three shafts which extend into both chambers. A bulkhead for each chamber is bolted to the pedestal in the areas where the shafts feed through.

Both bulkheads have an access plate which can be removed to facilitate reaching the mounting screws for "inside, lower" heads. Head selection and information lines are brought out of the disk chambers through etched circuit boards mounted in the bulkheads. The disk chambers must be air tight; therefore, gaskets are used around access plates, etched boards and hardware passing through the bulkheads.

As stated above, the pedestal supports three shafts. Head support assemblies mount with bronze bearings on the bottom shaft. When a head support is lowered from a disk, it pivots on this shaft called the head support pivot shaft.

The upper shaft is called the head support latch shaft. As the name implies, its function is to provide the stop for the head support assemblies when they are latched in the raised position. It can be seen that lowering and raising the head support could have disastrous results on head tracking unless the heads returned to exactly their original positions with respect to the disk. With that in mind, the pivot shaft, latch shaft, bronze bearings and latch mechanism are machined so accurately that head tracking is virtually undisturbed after a head support is relatched.

The remaining shaft is the disk drive shaft. The two disks in each chamber are mounted on this shaft. The bearings and shaft machining and balancing also have very close tolerances to prevent vibrations and disk wobble.

With the exception of head surfacing, the disks are the most precision-made components within the Storage Module. The basic disks are brass, 26 1/2 inches in diameter and 1/8 inch thick. Each disk undergoes special flattening, lapping and polishing processes. Disk wobble must not exceed .005 inch totally, surface flattness must be less than 20 microinches when measured in any one inch area and the average surface roughness must be less than 4 microinches at any point. Electroplating is used to deposit a magnetic film approximately 15 microinches thick. As a final process, each disk is dynamically balanced and tested on special equipment to ensure there are no flaws in the track areas.

4.2 MOTOR ASSEMBLY AND DRIVE BELTS

Refer to Figure 4.1-1.

The Storage Module disks are driven by a 1 H.P., 208VAC, single phase motor. The motor shell is drip-proof and the bearings are permanently lubricated and sealed. Input power can be either 50 or 60 cycle. Motor RPM is 1425 ± 5% or 1725 ± 5% for a 50 or 60 cycle source, respectively. The belt drive pulleys come in either 50 or 60 cycle size to match motor RPM to the required disk speed of 1500 RPM.

Two linked, pre-stretched V-belts couple the belt drive pulleys to the disk drive shaft. The motor mount pivots to allow belt adjustment. Links can be removed from the V-belts to compensate for stretch.

4.3 HEAD FLYING, HEAD ASSEMBLIES AND HEAD SUPPORT CASTINGS

BASIC DESIGN REQUIREMENTS

The design and arrangement of the heads, plus the shape and function of the head support castings, was developed to meet the following basic requirements:

1. The size of the disk must be held to a minimum, contingent upon practical information capacity and transfer rate.

2. To optimize packing density, each head assembly must use the "air-borne" principle when in the operating position.

3. Each track must have its own head to minimize access time.

4. For addressing and information layout, each disk face must be divided into three concentric zones with 50 information tracks per zone.

5. A remote means of controlling head "flying" and retraction must be employed.

6. For physical access, it must be possible to expose the head assemblies associated with a disk face without disturbing track alignment.

FLYING HEAD PRINCIPLES

To achieve high packing densities, it is necessary to operate the head in very close proximity to the recording medium. The following description covers the principles which enable the heads to be operated at approximately 125 microinches from the disk surface.

Considering a rotating disk, it is known that a moving layer of air is developed by the disk surface and this layer can provide an aerodynamic cushion for a head to float on. The velocity and force of the developed air layer increases linearly along the disk radius toward the outer edge. An "air-borne" head is repelled by this force and, therefore, "flys" on top of the air layer. It can be seen that the disk gap of a head mounted near the outer edge would tend to be greater than the gap of a head closer to the disk hub. To overcome the repellant force of the laminar air, a calibrated amount of air pressure is applied to the head actuator assembly. The head is controlled by this method and can be positioned to the desired distance from the disk. With a compliant head mounting, such as the gimbal spring, the head can make small self-adjustments in attitude while it is being "landed" (forced into "flying" position). By

utilizing these principles, an extremely small head to disk gap can be achieved.

The desired results are not available simply by placing a head close to a spinning surface. Rigid standards must be maintained in the finish of the disk to prevent turbulence in the laminar air. The head must have the proper aerodynamic shape and surfacing to "fly" parallel with the disk. It must ride the laminar air cushion without fluttering or creating its own turbulence.

A bevelled edge gives the Storage Module head its "flying" capability. Actually, the effect is created by a bevel of less than one degree with respect to the base of the head. The head is always mounted so that the angular edge is headed into the laminar air flow.

HEAD ASSEMBLIES

Introduction

Each information head assembly has 13 channels (individual heads). Because size is a consideration, it is desirable for adjacent channels to be as close together as possible. Crosstalk, a basic problem with all types of heads, limits the minimum spacing between the individual cores on one head assembly. The Storage Module information head assemblies are interlaced in pairs to minimize crosstalk and optimize useful recording area. Refer to Figure 4.3-1 and Figure 4.3-4 Section A-A.

Description

Thirteen cores for an information head or six cores for a clock head are mounted in "shoes" made of a special compound. Adjacent core separation is 40 - 45 mils and 110 - 115 mils for information and clock heads, respectively. Two "touch" pins are embedded in each shoe. The small bevel is machined off the leading edge and then the surface lapped and polished. The flatness of each of the two surfaces must be within two "light bands" (46 microinches) over their entire areas.

Each head is mounted on an etched circuit board. A common board can be used for all information heads regardless of whether the head will be in an upper or lower position. This is made possible by specially designed board circuitry which allows connection of cable leads to either end of the board. The 16 head assembly leads are brought out by a 7-inch cable to a connector which plugs into the head support "C" board.

The 26 isolation diodes per head assembly are encapsulated in two 13-diode "sticks" before their connections are made to the board circuitry. A back plate made of the same compound as the head is mounted on the bottom of the circuit board. This plate covers the

core leads and is the mounting point for the gimbal spring. A clock head circuit board follows the same assembly and description except that it only requires circuitry for six cores, always mounts in a lower position and only six diodes in each of the two "sticks" are connected to the board. The 9 leads are brought out in a 25-inch cable to a connector which plugs into either the "H" or "J" board mounted on the left or right bulkhead.

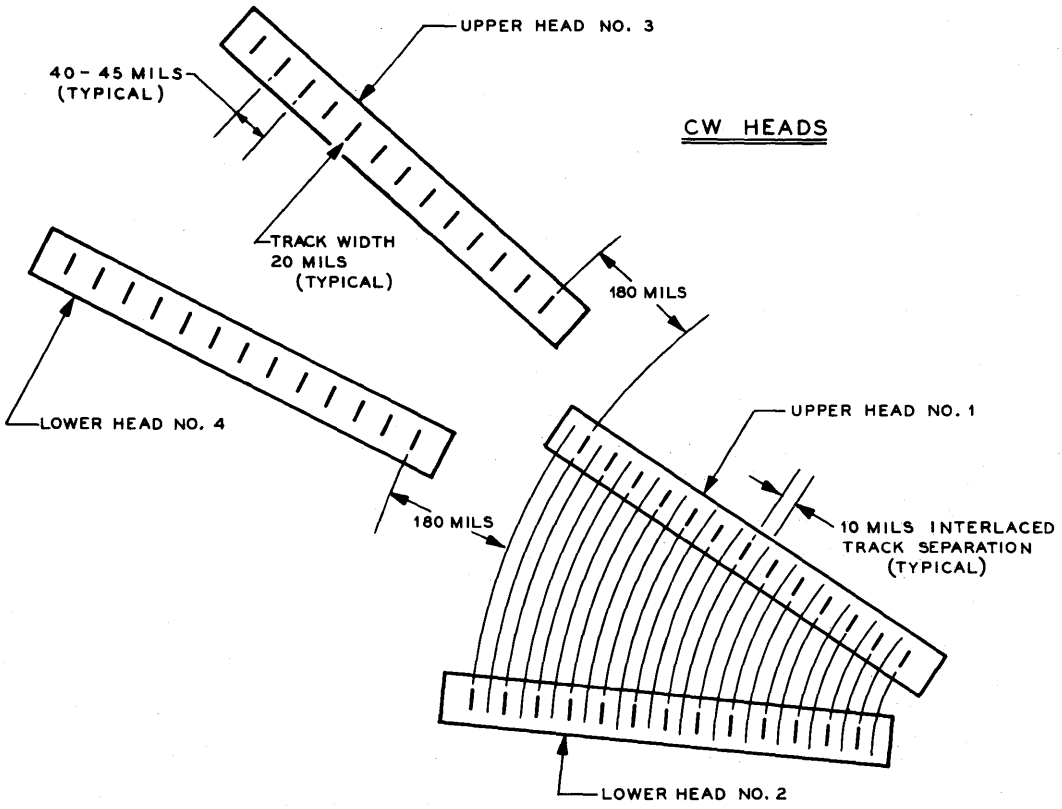


FIGURE 4.3-1
TRACK INTERLACE

The gimbal spring is a compliant mounting which connects the head assembly to its support bracket. The following requirements are met by this device:

1. The head can approach the disk surface "heel" first at an angle of up to 4 degrees to make a safe landing and then align itself parallel with the disk for normal flying.

2. It provides a flexible mounting which allows the head to move to and from its retracted position and follow undulations in the disk surface without introducing any skew factor.

3. It supplies the force for retracting the head when the actuator pressure is released. The center of the gimbal spring is bonded to the head back plate and the outside is riveted to the support bracket at the same two points where

the mounting stud pins are located.

The components described above are mounted on a support bracket to complete the final individual head assembly. Two configurations of support brackets suffice for all the different mounting situations. All lower clockwise and upper counter-clockwise heads require one type of support bracket. The other type is required for all upper clockwise and lower counter-clockwise heads. The head assemblies use a three point mounting for head alignment. A fourth mounting point secures the support arm. As in the case of other head assembly components, the support bracket is also made to strict tolerances. Correct track alignment is thus ensured following head assembly removal and replacement or replacement with a different head assembly.

Refer to Figures 4.3-2 and 4.3-3 for an example of the mounting configuration for each of the different head assembly types.

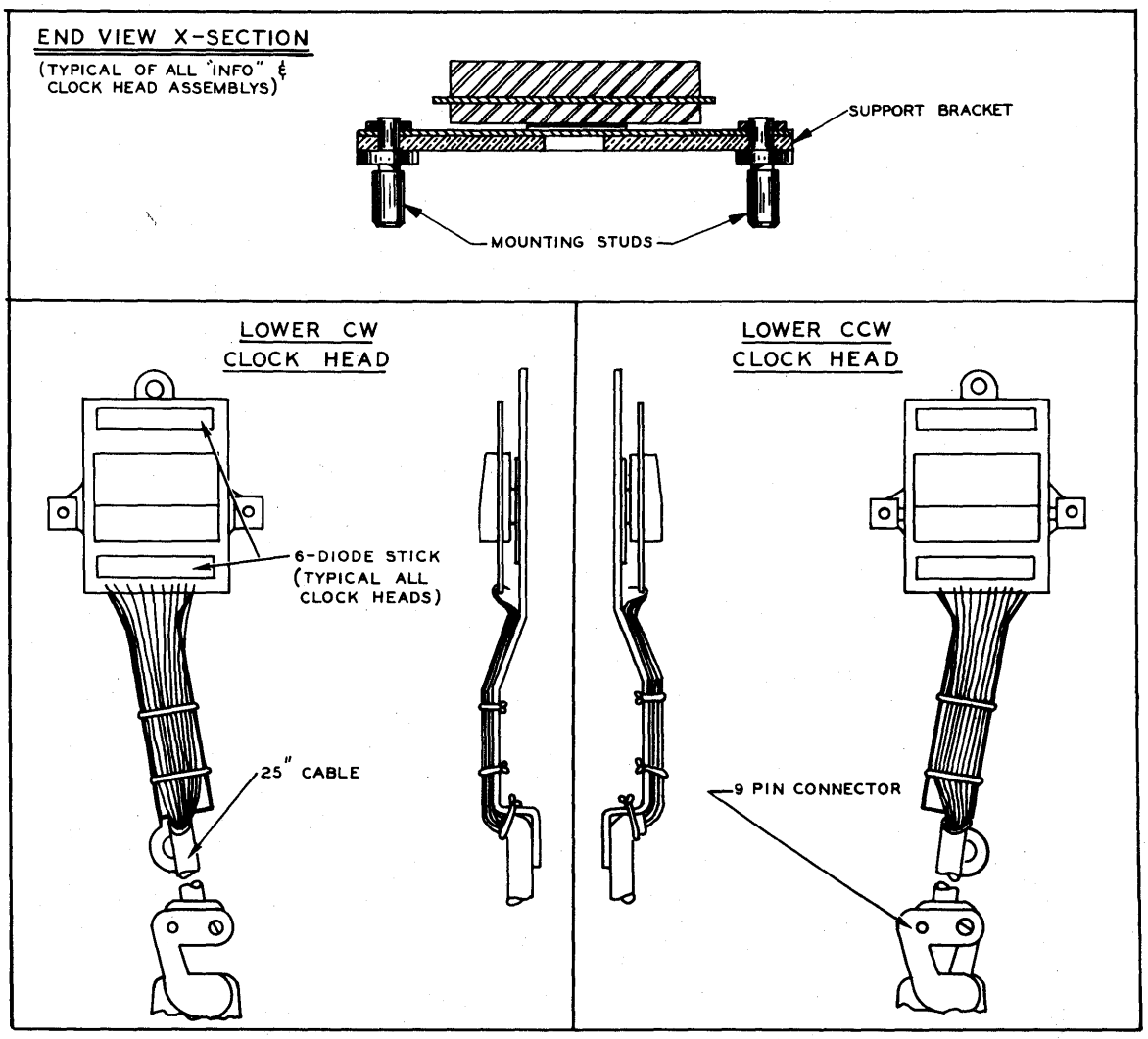


FIGURE 4.3-2
CLOCK HEADS

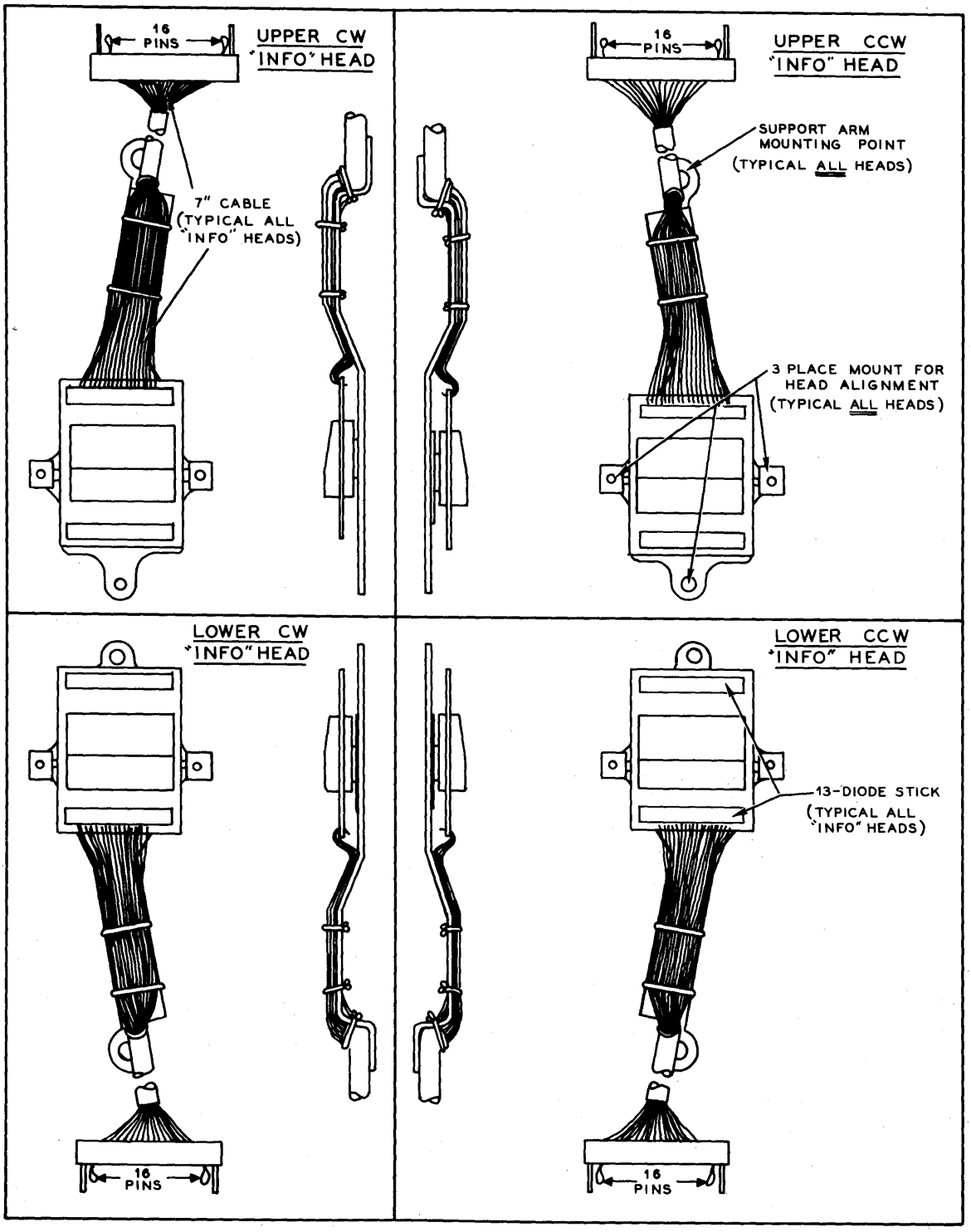


FIGURE 4.3-3
INFORMATION HEADS

Head Support Assemblies

Refer to Figures 4.3-4 and 4.3-5.

To provide the necessary information and clock tracks for one disk face, 13 head assemblies are required. These 13 are arranged in an arc-shaped cluster facing one side of a disk. The casting which provides the mountings for this configuration is called a head support assembly.

Figure 4.3-5 shows the disk and head support arrangement for a Storage Module. Only six head support assemblies are required as the center supports have heads on both sides. Head assemblies and their supports are constructed mechanically for either clockwise or counter-clockwise locations. The CW or CCW designation is determined by the direction of disk rotation with reference to the heads opposite a particular disk face.

Refer again to Figure 4.3-4. Heads mounted with the head support bracket arm pointing up are called "upper" heads. The support bracket arms of "lower" heads point down. Note that odd numbered heads are always upper heads while the converse is true for even numbered heads. Head number one is closest to the disk hub. It is followed by head two, head three, head four and the others in the same sequence, except that there is no head nine.

As described earlier, to conserve radial space and eliminate cross-talk, the tracks from two head assemblies are interlaced. An interlaced pair of heads form a group of 25 consecutive tracks. In relation to their positions along the disk radius, the even numbered head of an interlaced pair is displaced only 20 - 22.5 mils farther from the disk hub than its odd numbered mate. Disk velocity increases along the surface toward the circumference and the pressure of the air layer developed increases at the same rate. Therefore, in terms of repellant pressure encountered, two interlaced pairs (four heads) occupy the same pressure zone. Figure 4.3-6 indicates how the disk is divided into three ascending pressure zones and the head pairs associated with each zone. Head number ten, the clock head, occupies the third zone along with heads eleven, twelve, thirteen and fourteen.

Each head assembly is mounted over an actuator assembly in the head support casting. Because they have heads on both sides, the center supports require double actuators.

A head actuator is operated by air pressure from the Storage Module's air system. Each head pair on a head support has a separate air line carrying the calibrated pressure to fly heads in that particular pressure zone. An air line is routed first to the actuator for the lower mounted head and then coupled to the actuator of its upper mounted mate.

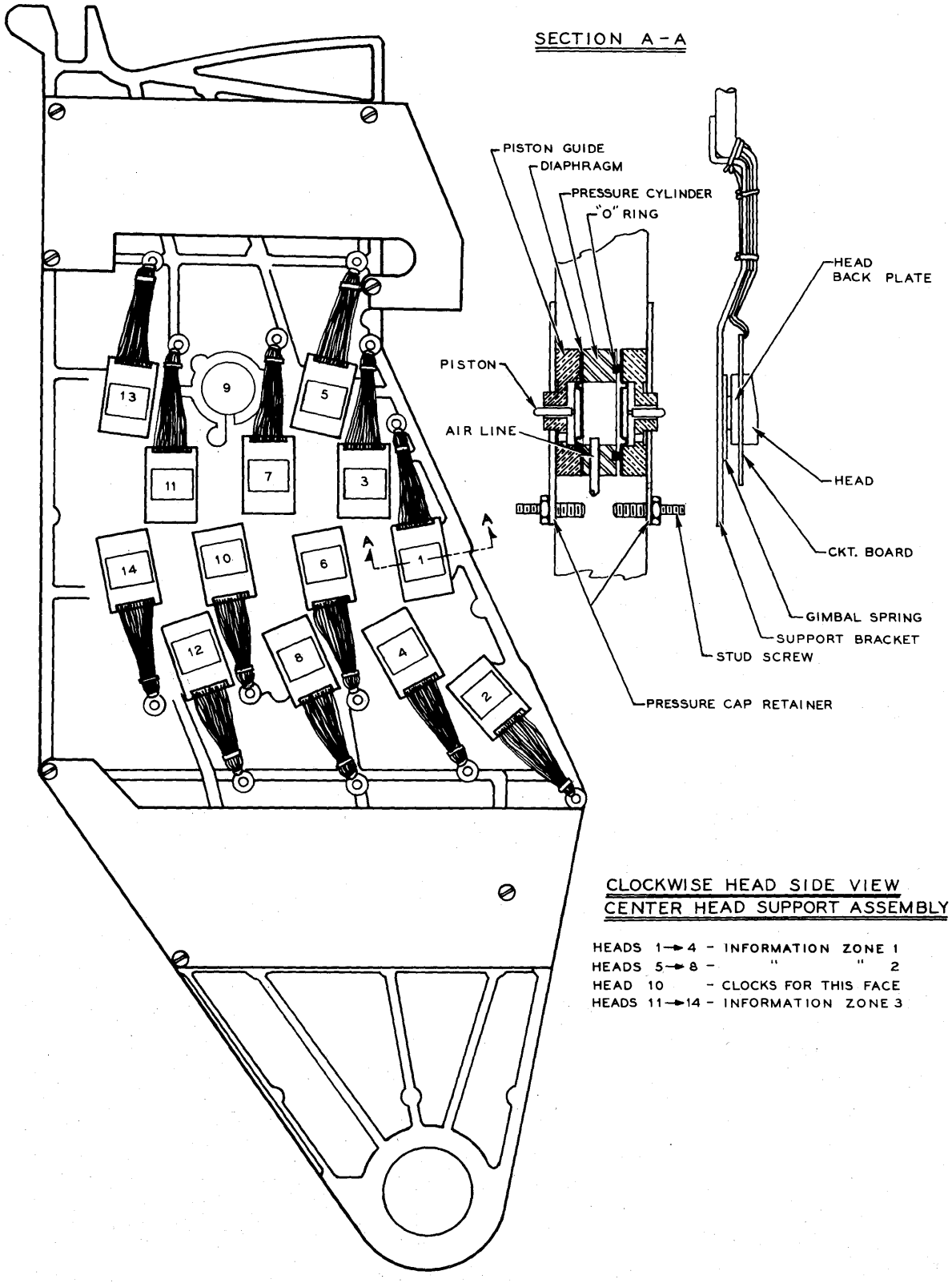


FIGURE 4.3-4
CENTER HEAD SUPPORT ASSEMBLY

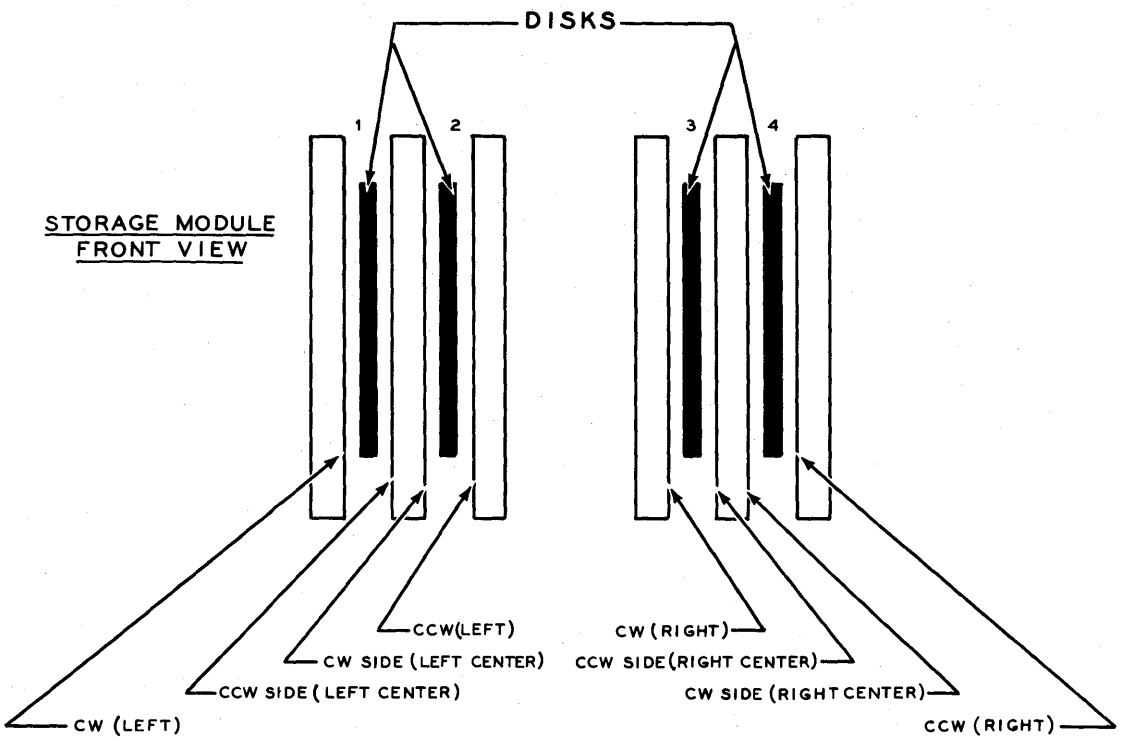


FIGURE 4.3-5
STORAGE MODULE - FRONT VIEW

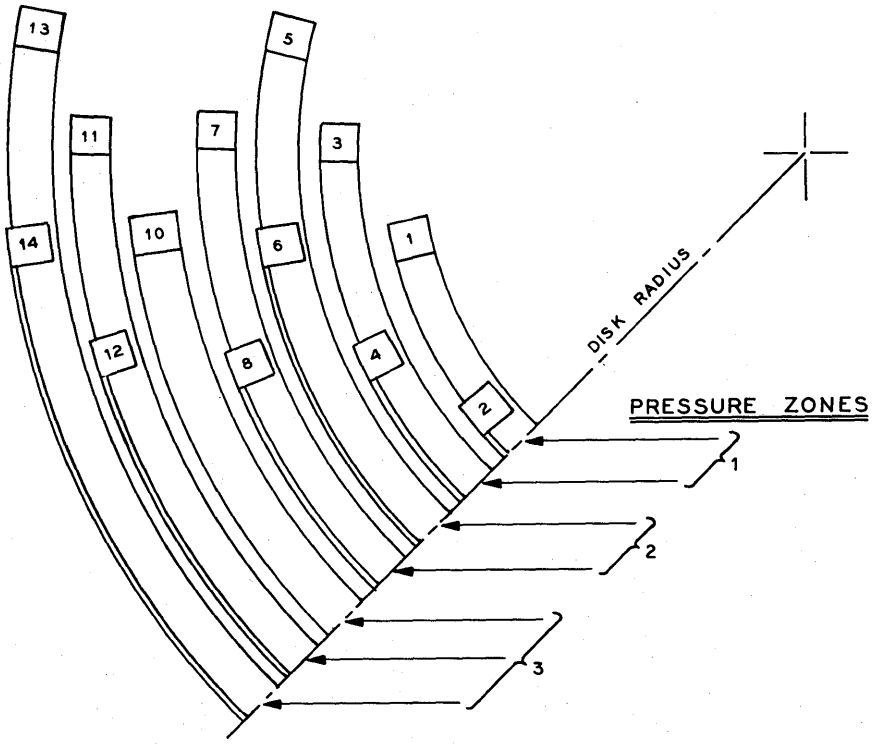


FIGURE 4.3-6
PRESSURE ZONES

Section A-A of Figure 4.3-4 illustrates the actuator mechanism of a center head support assembly. Note the components and their relationship. The air line terminates through a hole in the bottom of the pressure cylinder. A different type pressure cylinder having another hole for an outgoing air line is required in lower mounting positions. Rubber diaphragms completely cover both ends of the pressure cylinder. The pistons, guides and pressure cap retainers are then mounted over both ends. When the pressure cap retainers are tightened, the diaphragms act as gaskets sealing the ends of the cylinder. Sealant is used to prevent leakage around the air line. Air pressure applied to the cylinder drives the diaphragms, pistons and the head assemblies toward the disks. A predetermined amount of air pressure is required in each pressure zone to drive the heads to their proper flying distance. When that pressure is applied, the actuator mechanism drives the heads to their operating position within 125 microinches of the disks. Releasing the air pressure allows the gimbal springs to return the heads, pistons and diaphragms to their retracted positions.

The four other head supports in a Storage Module require single type head actuator mechanisms. All pressure cylinders have an "O" ring groove in one end. By installing the cylinder with the groove facing the end to be blocked off, it is possible to replace one diaphragm, piston and guide with a blank pressure cap.

A "C" shaped, etched circuit board is mounted on the pedestal side of each head support assembly. The connectors from the information heads plug into these boards. A complete description of the "C" boards is covered in Section 3.3.

The six head supports are bearing-mounted at their lower end on a pivot shaft. They latch at the top on a latch shaft. The bronze bearings, latch mechanism and stop are manufactured and installed to rigid specifications so the supports can be lowered and raised without any disturbance of head tracking.

4.4 STORAGE MODULE AIR SYSTEM AND DISTRIBUTION

INTRODUCTION

The purpose of the Storage Module Air System can be stated as follows:

1. Divide the filtered, regulated, compressed air input into seven different regulated pressure lines.

2. Distribute the pressure lines to the three respective pressure zones on each head support.

3. Activate the heads in each pressure zone.

As described in Section 4.3, each head is mounted on a gimbal spring which holds the head retracted from the disk unless this constant tension is overcome. Also, the spinning disk develops an air "layer" on its surface. To override the gimbal spring and the repellant air layer, compressed air is applied to the head actuator piston which forces the head to the proper operating distance from the disk face. However, the outward repellant force of the air layer increases in a direct relation to the increase in velocity along the disk radius. One standard level of compressed air is not practical therefore, because heads at different radial distances would not fly at the same desired head to disk gap. Heads 1 through 4 are in pressure zone 1 which is 25.5 psi; heads 5 through 8 are in pressure zone 2 which is 31.5 psi; heads 11 through 14 and clock head 10 are in pressure zone 3 which is 40.0 psi. The difference in pressure settings for the three zones is necessary to fly all heads at 125 micro inches.

DESCRIPTION

Refer to Figure 4.4-1 for the air distribution to the head pairs on a head support assembly; Figure 4.4-2 for the physical location of air system components; and Figure 4.4-3 for a functional diagram of the air system and as a reference for the following description.

The module air line connects into a T fitting in the main air trunk line running through the garage. Air flowing into the module must first pass through a 10 micron, porous bronze filter and then through an air gauge monitoring the incoming 50 psi line.

The Air Solenoid operates a valve in the incoming air line. One side of the coil is connected to -24V when DC is on. To pick the solenoid requires a ground level to the other side of the coil indicating the following conditions: No touch failure; the Touch Reset switch is not being held on; the disk speed is correct; the Head Retract switch is in the Fly position; and the two heat exchange air switches are closed by air flow. When the solenoid is energized, the valve allows incoming air to flow to the regulator manifold; when it is de-energized, the valve closes the incoming line and allows the air in the distribution system to exhaust to the outside atmosphere.

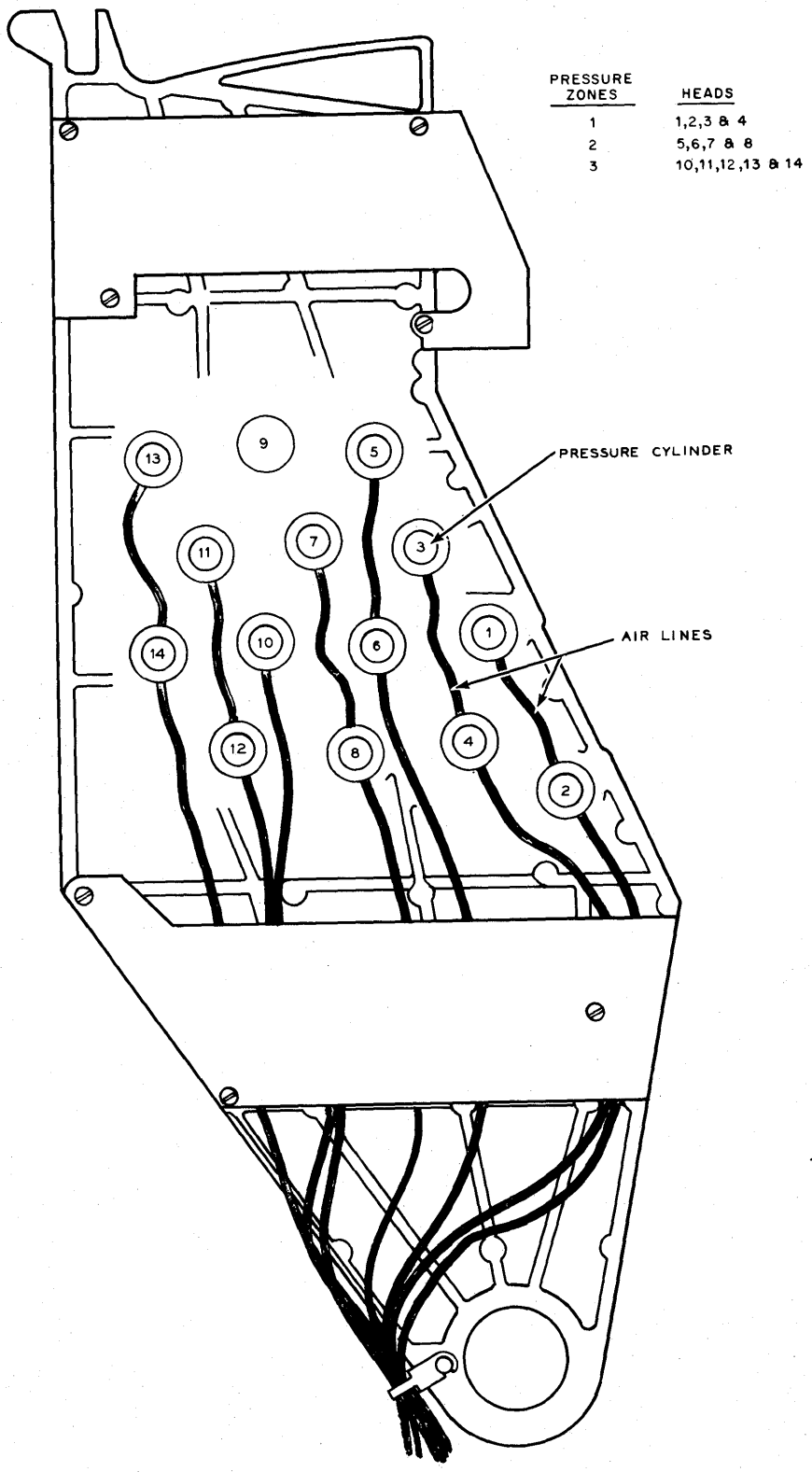


FIGURE 4.4-1
HEAD SUPPORT ASSEMBLY AIR DISTRIBUTION

FIGURE 4.4-2
STORAGE MODULE
AIR SYSTEM COMPONENTS

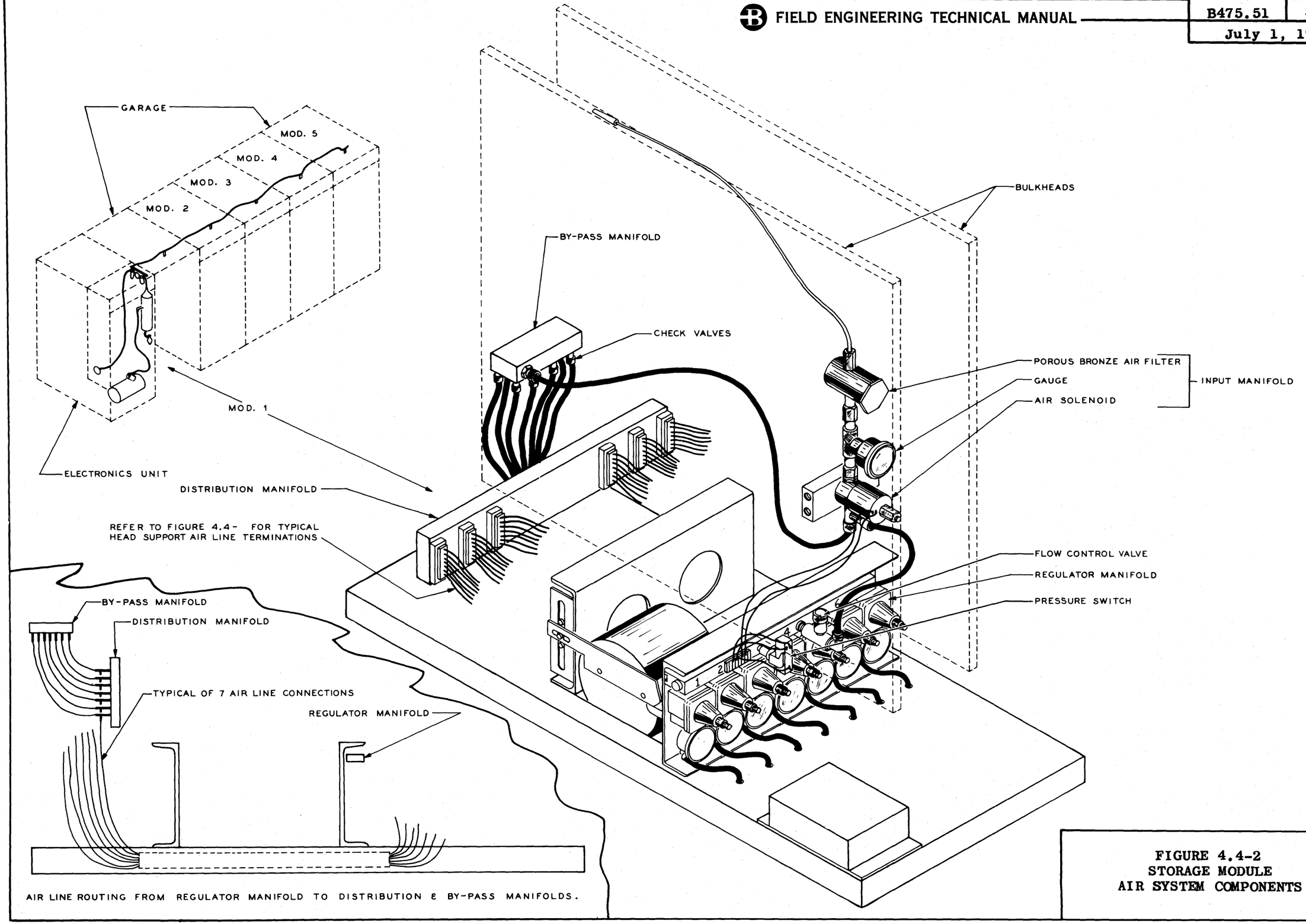


FIGURE 4.4-2
STORAGE MODULE
AIR SYSTEM COMPONENTS

FIGURE 4.4-3
BLOCK DIAGRAM AIR SYSTEM

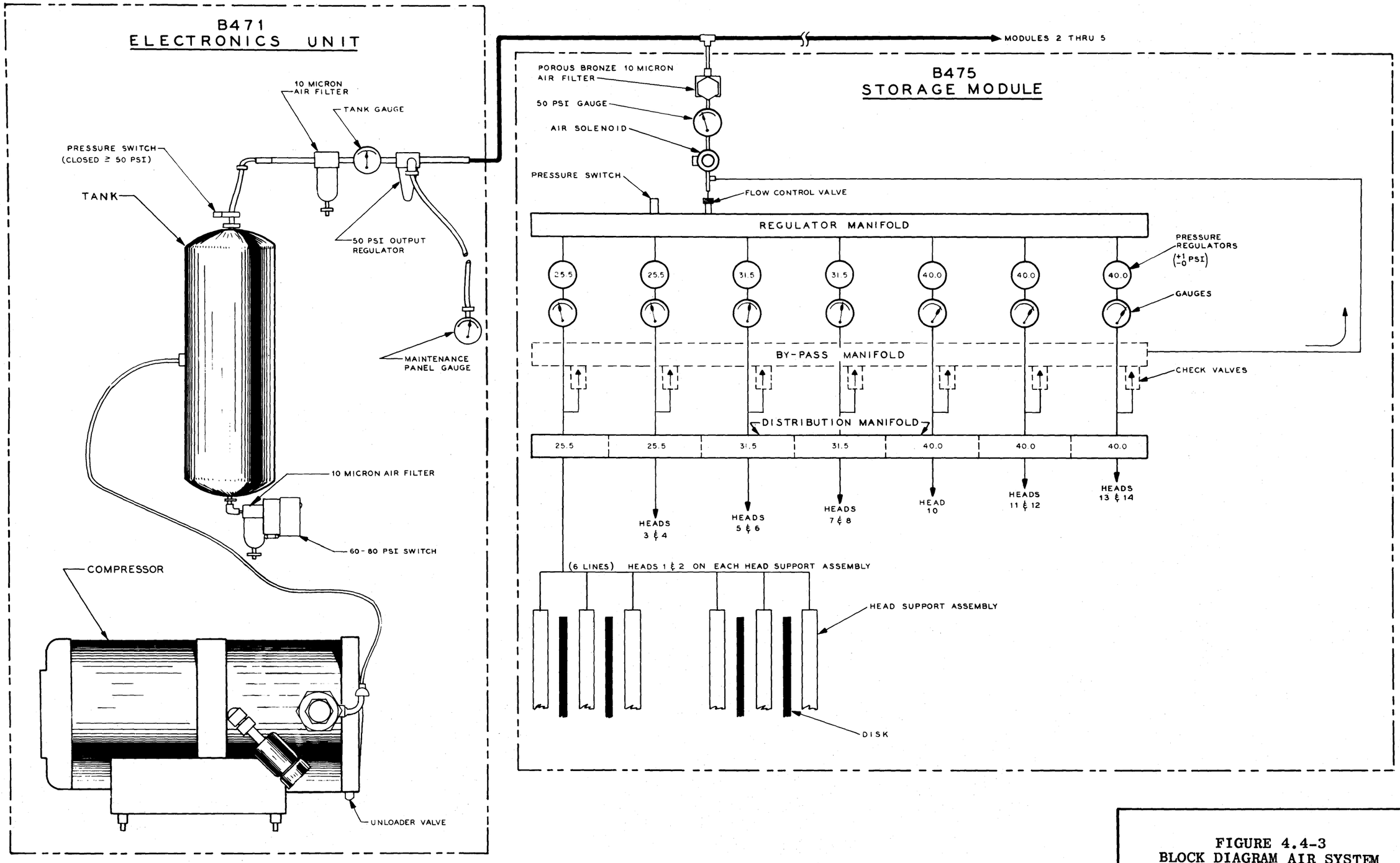


FIGURE 4.4-3
BLOCK DIAGRAM AIR SYSTEM

Air from the energized solenoid must pass through the Flow Control Valve before entering the Regulator Manifold. This valve can be adjusted to regulate the flow of air into the distribution system. Its purpose is to control the time it takes to fly the heads.

The Regulator Manifold Assembly consists of a manifold pressure switch, seven regulators and gauges on the output lines. The regulators divide the 50 psi input into the separate lines required by the three different head pressure zones. Each regulator's output is adjustable. The zone one regulators are set to 25.5 +1, -0 psi as registered on the output line gauges. The regulators for zone two are set at 31.5 psi and 40.0 psi for zone 3. The pressure switch is an adjustable, pressure actuated switch mounted on the Regulator Manifold. It is set to drop out at 42 psi and will actuate at 45 psi. By controlling the HFML/ level, the pressure switch holds the S.U. Not Ready during head activation until the heads have reached flying pressure. When the air pressure is dropped, due to a touch for example, the pressure switch causes the unit to go Not Ready.

The Distribution Manifold "distributes" the air from the seven regulators to the corresponding head pairs on the head support assemblies. The manifold is divided into seven "chambers". The chambers for zone one distribute air at 25.5 psi to heads one through four on each of the six head supports. The chambers for zone two distribute 31.5 psi air to heads five through eight. The distribution of air to the head pairs in zone 3 follows the same pattern.

The By-Pass Manifold is a safety device used to accelerate head retraction by rapidly discharging the air pressure from the head activation mechanisms. Without this by-pass, the air would have to exhaust back through the gauges, regulators and flow control valve before being released to the outside atmosphere. Because the by-pass system is in parallel with the Regulator Manifold, the By-Pass Manifold is pressurized at 50 psi whenever the Air Solenoid is energized. Each of the seven pressure lines is connected to the By-Pass Manifold through a unidirectional check valve. The valves are held closed if the air in the manifold is at 50 psi. However, if the Air Solenoid is de-energized, the check valves will open when the manifold pressure drops 1.5 psi. Opening the check valves allows the pressurized air in the head actuator mechanisms to discharge through the exhaust port of the Air Solenoid valve.

4.5 DISK COVERS AND HEAT EXCHANGES

DISK COVERS

The two disks in each half of the Module are enclosed in an airtight cover. The cover is a metal shell except for the front section which is a glass window in a metal frame. The window and the metal shell, as a unit, attach to the bulkhead by screws. All joints between the window, metal shell and bulkhead have sponge gaskets which make the enclosure airtight.

In the rear of each metal shell, there are two purge holes with covers and gaskets, a heat exchange blower motor and 40 heat exchange tubes.

HEAT EXCHANGES

The Module is equipped with a heat exchange cooling system for the disk enclosures. The system consists of two 100 cfm blower motors mounted on the bottom rear of the metal covers, two air flow switches mounted in the fan enclosures, 40 heat exchange tubes in each disk cover and a disposable fiberglass filter covering the intakes of the two blowers.

The blower motors operate on 208VAC and cycle on and off with the Disk Drive Motor and Running Time Meter. Air from the garage is drawn through the filter, driven up the tubes and out the top of the disk covers back into the garage.

Air is exhausted from the garage by two 100 cfm muffin fans mounted on the rear skin.

Heat generated inside the disk enclosures is absorbed by the tubes and carried off by the air flow. With the heat exchanges on and room temperature at 65 to 80 degrees, the disk enclosure temperature will be approximately 20 degrees higher or from 85 to 100 degrees.

Assembly - Disassembly - Adjustments

✓INDEX - SECTION V

✓Changes or additions since last issue.

5.1 STORAGE MODULE - REMOVAL AND REPLACEMENT

REMOVAL

Before removing the module from its garage, cycle all power off and open the 15, 50 and 70 amp AC circuit breakers at the E.U.

1. Remove the front panel and the bottom front spacer.
2. Open the top panel lid and unplug the six Head Select Cables (three input and three output) from the Center Tap Distribution Board (Rack G).
3. Unhook air line by sliding back the spring-loaded sleeve on the air TEE connector. This sleeve must be slid back in the same manner when re-connecting.
4. Unplug the following cables from the logic gate (Rack A):

   AAB0A2 - Logic In
   AAB0A7 - Logic Out
   AAB0N2 - DC Power

5. Remove logic ground wire bolted to logic gate.
6. Remove short frame ground wire located at bottom left of unit.
7. Roll module from garage far enough to allow access to the AC power cable. Hold all loose cables away from the unit.
8. Unplug AC power cable at Motor Power Relay box located at bottom center on the right side of the unit.
9. Remove module from garage being careful again to hold loose cables away from unit.

REPLACEMENT

To replace module, reverse the above procedure.

5.2 LOGIC GATE - REMOVAL AND REPLACEMENT

REMOVAL

1. Remove the following cables from the gate:

   AAA0A2 - Clock Head In
   AAD0N2 - Information Head In
   AAB0A2 - Logic In
   AAB0A7 - Logic Out
   AAB0N2 - DC Power

2. Remove Maintenance Panel power stick - location AAG0Y0.

3. Remove the two ground straps bolted to gate.

4. Bend top hinge bar up far enough to clear pivot peg on gate.

5. Pull the top of the gate forward enough to clear the hinge bar and lift gate up and out of its bottom hinge peg hole.

REPLACEMENT

To replace gate, reverse above procedure.

5.3 DISK COVERS - REMOVAL AND REPLACEMENT

Refer to Section 5.1 for module removal

REMOVAL

1. Remove logic gate following procedure outlined in Section 5.2.
2. Disconnect heat exchange blower motor cable, TAJ4 or TAJ5.
3. Completely remove heat exchange filter assembly.
4. Remove glass window taking care to avoid tearing the sponge gasket.
5. Remove screws holding cover to bulkhead.
6. Slide cover back and off using handle provided taking care to avoid tearing the sponge gasket.

   During handling, care should be taken not to bend cover or scratch the mounting lip.

REPLACEMENT

Reverse the above procedure after making sure mounting lip is clean, gaskets are properly aligned, and heat exchange tubes and cover are not damaged.

5.4 INSTRUCTIONS FOR REPAIRS WITHIN THE DISK ENCLOSURE

SECTION I - REMOVAL AND REPLACEMENT OF A HEAD

CAUTION

Before proceeding with the head replacement, use the appropriate head locating chart at Figure 5.4-1, 5.4-2 or 5.4-3 to verify the repair will be made on the correct head.

Removal Procedure

1. Remove module from garage and move to a room/area where there is a minimum or no air movement.
2. Disconnect the blower connectors.
3. Remove the filter assembly.
4. Disconnect all cable connectors to the logic gate.
5. Remove the logic gate and set it aside carefully.
6. The two tubes at the top of the purge unit blow filtered air out. The single tube at the bottom is the intake to the absolute filter. Remove the output tubes from the plates on which they rest and start the purge unit. This will blow filtered air through the output tubes to clean them. Run the purge unit for at least 30 minutes.
7. Attach the hose to the vacuum cleaner so that it is blowing and dust off the module.
8. Attach the hose to the vacuum cleaner for normal cleaning and carefully clean the disk enclosure, window and bulkhead, especially all the joints.
9. Stop the purge unit after it has run 30 minutes as per Step #6 above. Do not subject the purge unit to any rough handling after purging.
10. Remove the purge port plates from the rear of the disk cover and place them together with the clean sides face to face.
11. Use Freon TF and a lint-free wiper to clean the exposed flanges of the purge ports and the flanges of the purge tubes.
12. Attach both output tubes from the purge unit to the purge ports.
13. Remove the window assembly and protect it from dust particles as much as possible.

14. Start the purge unit.

15. The even numbered heads are all lower heads and require the use of the head protection hood if a replacement is made. In this case, refer to Section II - Assembly.

16. For a repair to an odd numbered head, which are the upper heads on the head support assembly, the hood is not required and the Field Engineer should proceed to Step #17.

17. Wash hands thoroughly.

18. Refer to Figures 3.3-1, 3.3-2, 3.3-3, 3.3-4, 4.3-5 and 4.3-6 in the B475 Technical Manual to identify locations referred to in the following steps.

19. Unlatch and remove all the cable connectors from the Rack H board (Rack J board for repairs in the right-hand disk enclosure)

20. Unlatch and remove the appropriate cable connectors from the Rack G Center Tap distribution board.

21. Unlatch and lower the head support assembly.

    Use EXTREME CAUTION when lowering the head support assembly to insure that the heads do not touch the disk face and that no cables drag across the heads.

    Note that if this is an upper head repair and the hood is not used, the head support assembly will be resting on the C head support board. Use extreme care to prevent unnecessary stress or strain on this board.

22. Due to the overlap of some head assembly mounting brackets, certain heads must be removed prior to the removal of others. The following list of heads shows the prerequisites for each:

Head #1	None
Head #2	First remove heads #6 and #4.
Head #3	First remove head #1.
Head #4	First remove head #6.
Head #5	First remove heads #1, #3 and #7.
Head #6	None
Head #7	None
Head #8	First remove heads #6 and #10.
Head #10	None
Head #11	None
Head #12	First remove heads #10 and #14.
Head #13	First remove head #11.
Head #14	None

23. If the clock head is to be replaced, remove the cable clamp from the head support casting.

    If an information head is to be replaced, remove the appropriate lead cover to expose the head assembly cable connector.

24. Remove the cable connector from the C board. These miniature Amphenol connectors are VERY FRAGILE. The suggested method of removing them is to push alternately on the two guide pins from the other side of the board until the connector is half out. It can then be easily extracted.

    NOTE

    DO NOT disconnect the cable connectors of the prerequisite heads.

25. To remove a head assembly from the support casting, perform the following steps in sequence:

    a. Remove the screw holding the head assembly bracket.

    b. Remove the nut from the mounting stud bolt.

    c. Grasp the head assembly bracket at the two side alignment studs. USE NO TOOLS. Carefully pull the head assembly away from the support casting. Let "prerequisite" heads hang from their cable connectors taking care to minimize flexing of the leads.

Replacement Procedure

1. If more than one head was removed, the heads must be replaced in reverse sequence to their order of removal.

2. Carefully clean the new replacement head with Freon TF and a lint-free wiper. Extreme care must be taken in the following respects:

    a. Fragile connector

    b. Fragile leads

    c. Mounting bracket must not be bent

    d. Head is glued to gimbal spring - do not stress

    e. Head flying face must not be scratched.

3. Grasp the head assembly by the two side alignment studs and carefully insert them fully in the guide slots. NO FORCE IS REQUIRED.

4. Very carefully check to insure the head is fully seated before replacing the mounting stud nut.

CAUTION

If the alignment studs are not fully inserted and the head not correctly seated, the head will not fly properly and a crash will result.

5. Replace the mounting stud nut and use a torque wrench to tighten it to 4 inch-lbs. Check again for correct seating of the head.

6. Replace the pan head screw in the arm of the mounting bracket. Note that this will place tension on the arm. This is normal. Use a torque wrench to tighten the screw to 13 inch-lbs.

7. Replace the head assembly cable connector. The large and small guide pins determine the orientation. Great care must be exercised to insure that the delicate wire form contact pins are not bent causing a short to an adjacent pin.

8. Replace the lead cover plate and/or clock head cable clamp.

9. Replace "prerequisite heads" as per Steps #3, 4, 5, 6, 7 and 8 above.

10. Use Freon TF and a lint-free wiper to wipe down the heads and other areas that have been contaminated by handling.

11. Carefully raise and latch the head support assembly insuring cables do not drag across heads and heads do not hit a disk face.

12. With the head support assembly in position, check that all head cables are well clear of any disk surface.

13. Replace and latch the cable connector in the G board.

14. Replace all cables removed from the H board (or J board). Use the cable lables, silk-screening and Figures 3.3-3 and 3.3-4 to identify correct locations. Insure cable connectors are latched.

15. If the hood is being used for this repair, refer to Section II - Disassembly.

16. Make a final check that head cables are clear of disk faces, head support assemblies securely latched, all cable connectors correctly replaced and latched.

17. Clean the window assembly with Freon TF and a lint-free wiper. Wipe out the accessible area of the bottom of the disk enclosure.

18. Replace the window assembly by inserting all the holding screws loosely with the purge unit still blowing.

19. When all the window assembly screws have been replaced, tighten them evenly.

20. Turn off the purge unit.

21. Remove the hose from the lower purge port and secure it on the bracket.

22. Remove the intake hose from the bracket, wipe the flange and the lower purge port and attach the intake hose to the lower port.

23. Roll the module and purge unit close to the module garage with the front of the module facing toward the E.U. Unless this is the fifth module on line, the AC cable can readily be plugged in. If this is the fifth module, then it will have to be exchanged with a module in another position. If available, use the Disk File Coupler to extend the module.

24. Replace the logic gate and plug in the DC cable, logic cable and the H and J board cables. Plug in the stick from the maintenance box. Use the air hose extension to couple the air line to the module.

25. Replace the filter assembly.

26. Re-connect the blowers.

27. Purge the module for 15 minutes with the disks stopped.

28. Purge the module for a further 30 minutes with the disks turning and heads retracted.

29. Purge the module for a further 15 minutes with disks turning and heads flying.

30. Retract the heads and stop the drive motor.

31. When the disks have come to a COMPLETE STOP, turn off the purge unit and remove the hoses.

32. Clean the purge ports and plates with Freon TF and a lint-free wiper and replace the purge port plates.

33. Restore the module and purge unit to normal.

Gain Control and Pre-Amp Setting

1. After replacing a head, MS1 must be re-written to enable the gain control circuitry to function correctly. Run B200 D.F. Test Routine 2122, Part 5 or 6 or B5500 D.F. Test Routine 5561, Part 1, Section A.

MS2 can be re-written if desired as a local, manual function if point AAD2N1 in D.F. Control is grounded.

2. The signal amplitude of each track of the new head should be noted. Check to see if any track amplitude falls outside of those listed on Form T.S. 39335 and, if so, re-calculate the required pre-amp gain using the formula given in Section 5.12 (or 5.13).

FIGURE 5.4-1
HEAD LOCATING CHART
240 C/S OPTION

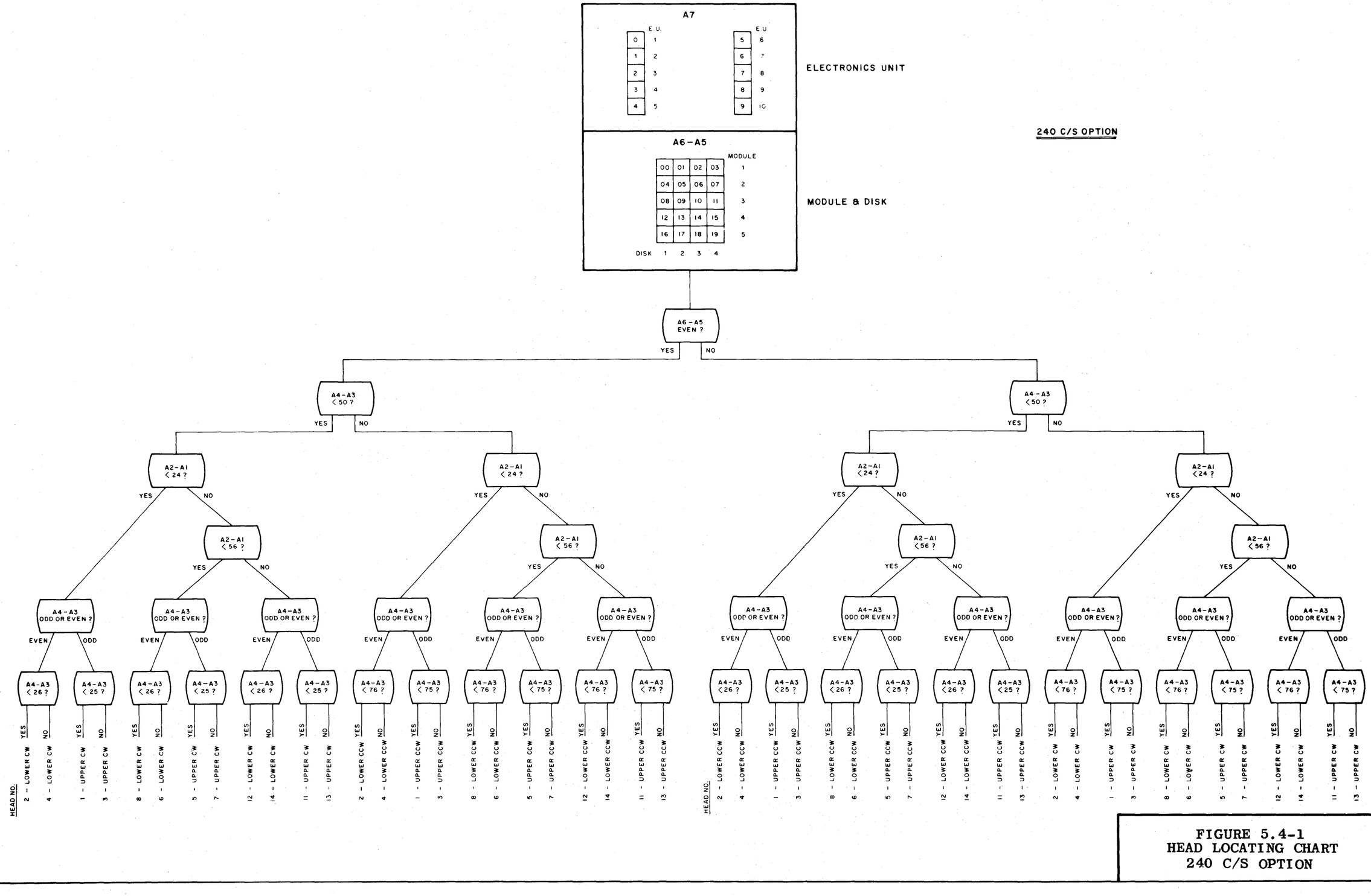
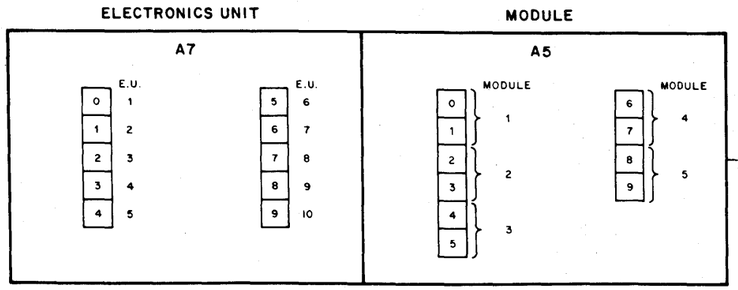


FIGURE 5.4-1
HEAD LOCATING CHART
240 C/S OPTION

FIGURE 5.4-2
HEAD LOCATING CHART
480 C/S OPTION



480 C/S OPTION

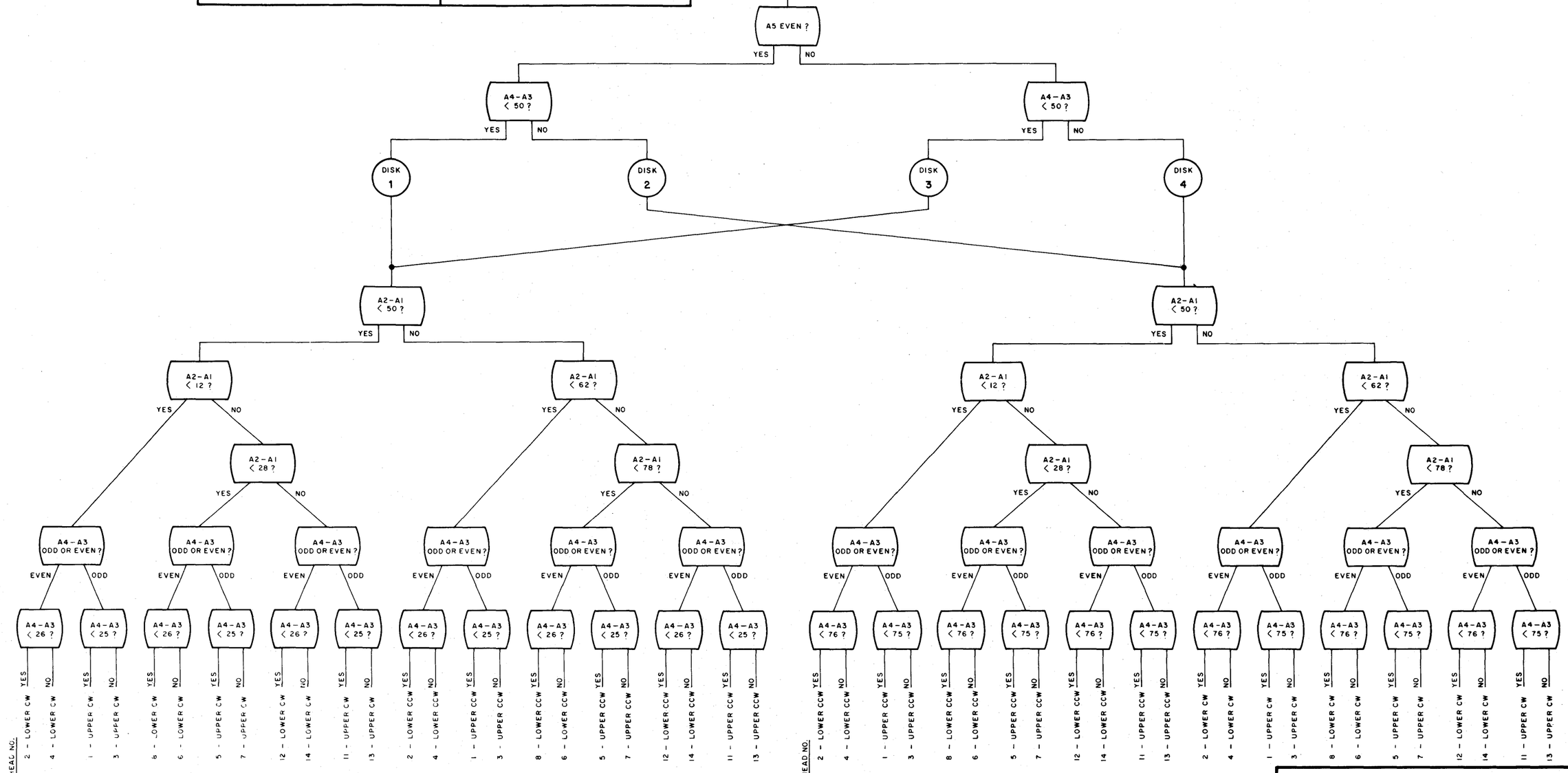


FIGURE 5.4-2
HEAD LOCATING CHART
480 C/S OPTION

FIGURE 5.4-3
HEAD LOCATING CHART
96 C/S OPTION

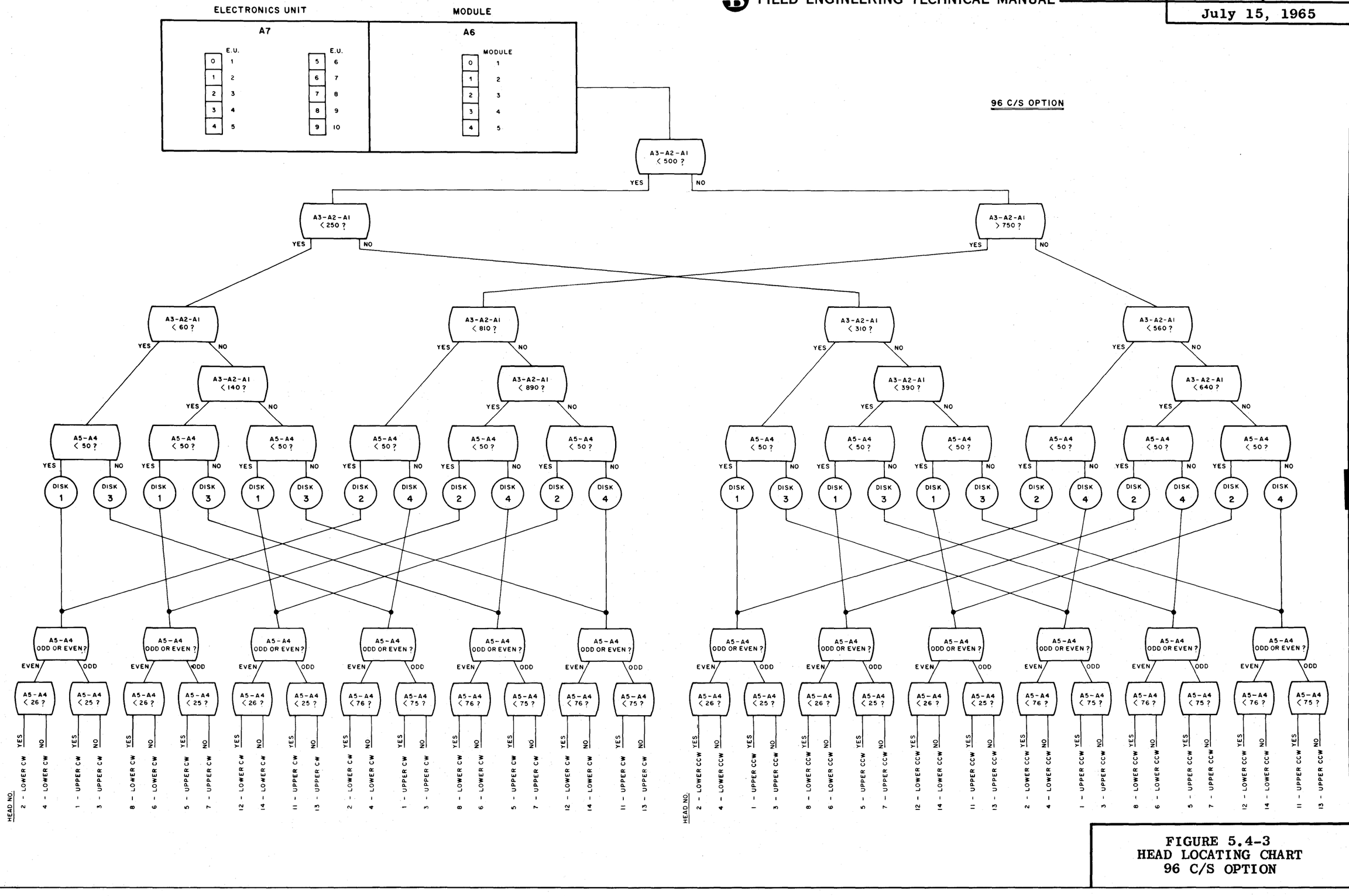


FIGURE 5.4-3
HEAD LOCATING CHART
96 C/S OPTION

SECTION II - ASSEMBLY AND DISASSEMBLY - HEAD PROTECTION HOOD

NOTE

Both assembly and disassembly procedures require two men.

Assembly

1. Vacuum the outside of the hood.
2. Remove the head protection hood cover and protect it from dust particles as much as possible.
3. Vacuum the inside of the hood.
4. Slide the hood flanges over the top and bottom of the window frame and fasten the two outside clamps.
5. Remove all the screws holding the disk cover to the bulkhead plate.
6. Stop the purge unit.
7. Slide the disk cover, with hood attached, toward the back of the unit until the inside flange of the hood is positioned against the window frame on the bulkhead plate.

CAUTION

The two Field Engineers should take the weight of the cover and hood to prevent the cover flanges scraping the top of the bulkhead and take every care to prevent creating particles which will fall into the cover.

8. Replace four screws to hold the disk cover to the bulkhead. Do not tighten the screws.
9. Remove the head protection plate from the head protection hood cover and mount it on the rear of the disk cover. Do not tighten the screws.
10. Fasten the two inside clamps of the hood to the bulkhead.
11. Align and tighten the screws replaced in Step #8 and #9 above.
12. Start the purge unit.
13. Open the front door of the hood.
14. Wash hands thoroughly.

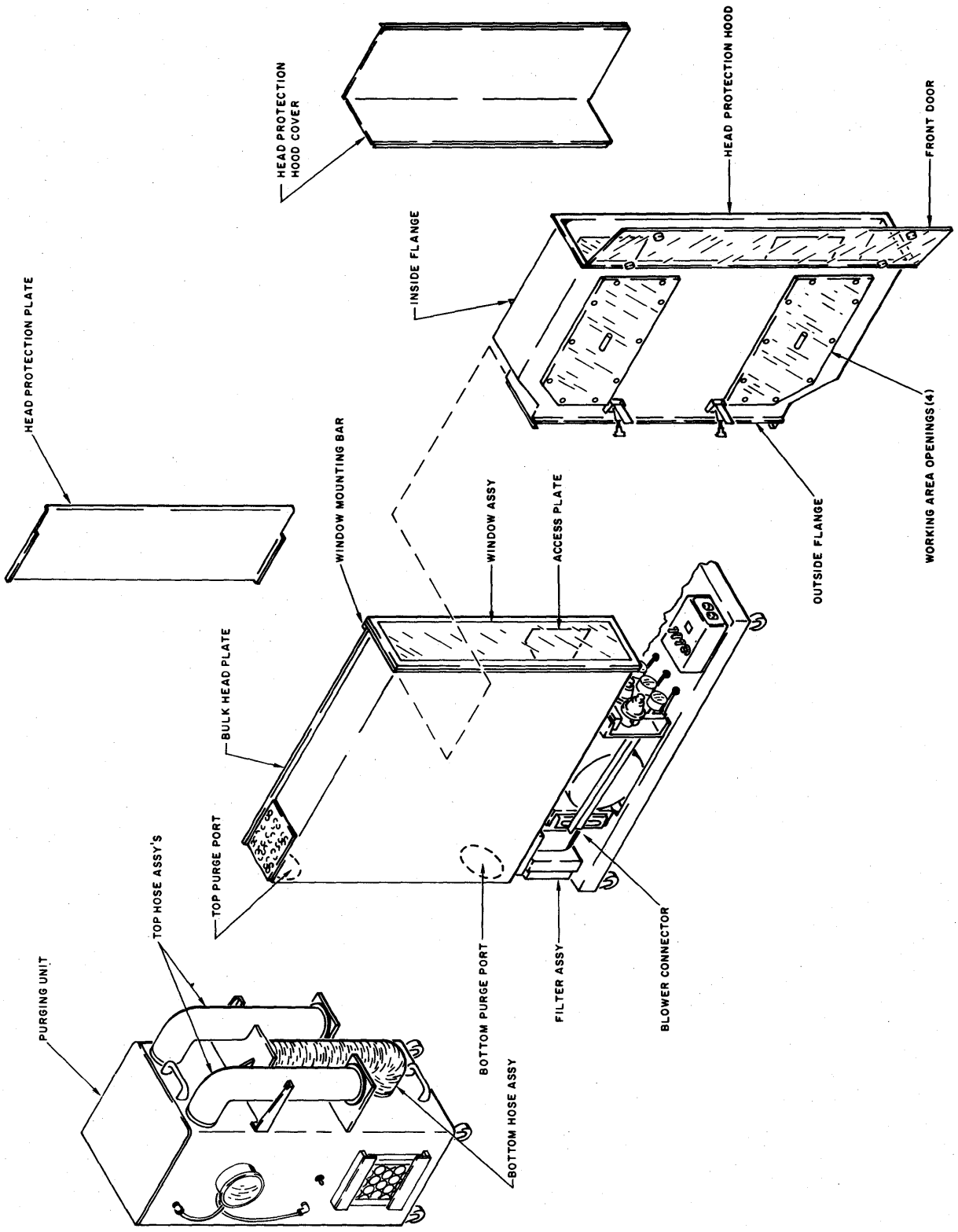


FIGURE 5.4-4
PURGE UNIT AND HOOD INSTALLATION

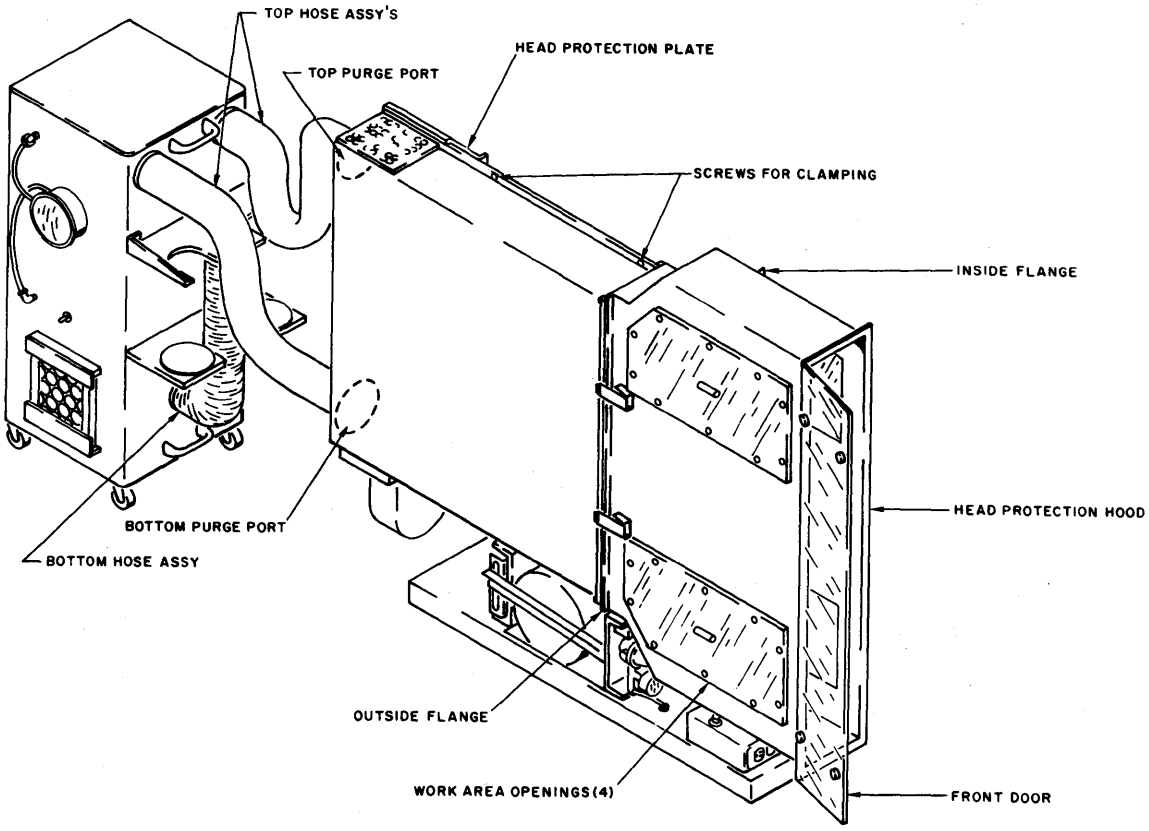


FIGURE 5.4-5
PURGE UNIT AND HOOD ASSEMBLED

15. Remove the access plate from the bulkhead. Remove plastic windows as required by the repair. Never leave more than two openings open at any time including the front door.

16. Return to Section I, Removal Procedure, Step #18.

Disassembly

1. Replace the access plate in the bulkhead.

2. Replace all plastic windows and close the front door of the hood.

3. Stop the purge unit.

4. Remove the head protection plate.

5. Remove the four screws which fasten the cover to the bulkhead.

6. Unfasten the two inside clamps.

7. Slide the cover forward to its normal position. Two Field Engineers should take the weight of the cover and hood to avoid scraping the top of the bulkhead and creating undue contamination.

8. Unfasten the outside clamps and remove the hood.

9. Replace all the screws in the disk cover. Do not tighten the screws until all screws have been started.

10. Start the purge unit.

11. Vacuum the head protection plate and mount it on the head protection hood cover.

12. Vacuum the inside of the hood.

13. Replace the head protection hood cover.

14. Return to Section I, Replacement Procedure, Step #16.

5.5 BELT REMOVAL AND REPLACEMENT

Old belts should be removed and replaced with new belts when the distance between the top of the motor arm and the base is less than 4 1/16 inches after adjustment. Refer to Figure 5.5-1. Belts must be replaced as a matched pair (P/N 1113 8526).

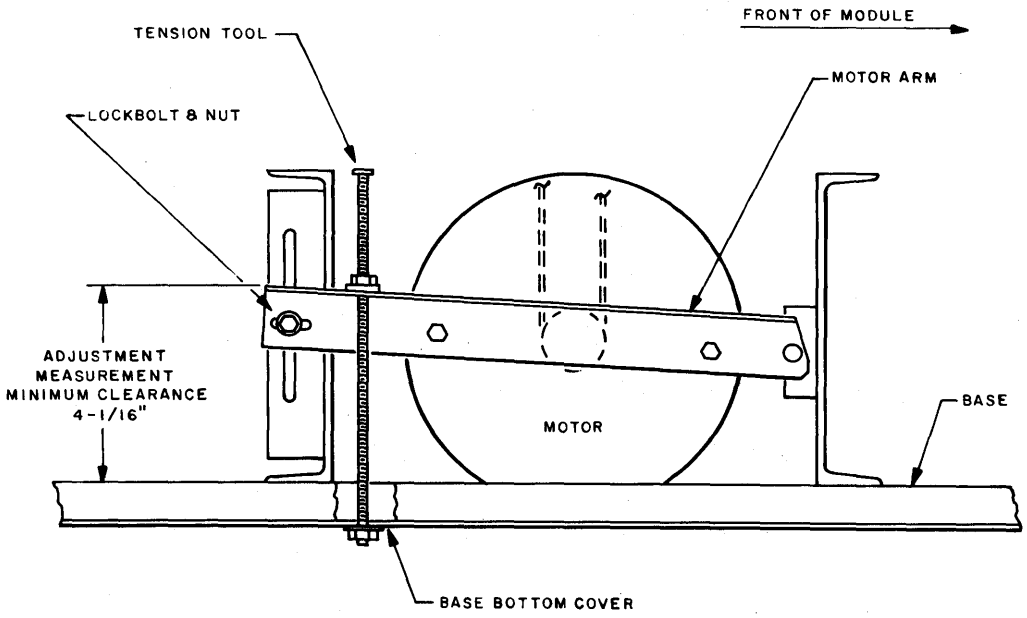


FIGURE 5.5-1
BELT ADJUSTMENT-MAXIMUM

REMOVAL

1. With the lock bolt and nut loosened, lift the motor up to slacken the belts. Prop the motor up by placing an object between the bottom of the motor and the base pan.

CAUTION

The motor is heavy so care must be taken to prevent injury to fingers.

2. Slip the belts off the motor pulley.

3. Lift the belts through the top of the pedestal casting in order to uncouple the links.

4. Since three links overlap each other, as illustrated in Figure 5.5-2, it is necessary to work a link off of two metal studs. Flexing the belt opposite to its normal curvature is often helpful while working the links off studs. Use the belt-link tool (P/N 1622 8454). Insert this tool into the

hole of a link by holding the tool at a right angle to the link length. Rotate the tool until it is parallel with the link. Spread the jaws and work the link off the metal stud.

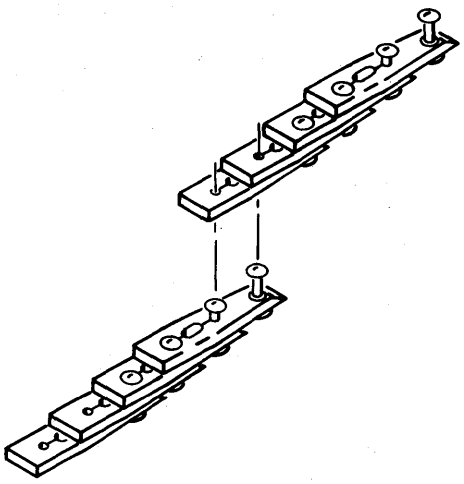


FIGURE 5.5-2
BELT LINKS

5. Pull the uncoupled belts out through the top of the pedestal.

REPLACEMENT

1. Remove the pair of new belts from the belt stretching fixture (P/N 1622 7142) and uncouple them with the belt-link tool.

NOTE

New belts must be stretched for 24 hours prior to installation and should be installed within 30 minutes after removal from the stretching fixture.

2. Insure that the belt links are oriented as indicated in Figure 5.5-3.

3. Lower the belts onto the disk-drive pulley letting the uncoupled ends down to the motor pulley.

4. Facing the right side of the module, reach over the relay box and temporarily hook the ends of each belt together.

5. Pull the belts up through the top of the pedestal and properly couple them together with the belt-link tool.

6. Lower the belts onto the disk-drive pulley.

7. Slip the belts (in the proper sequence) into the motor pulley grooves. Remove the object used to prop up the motor and lower the drive motor until the belts support the motor weight.

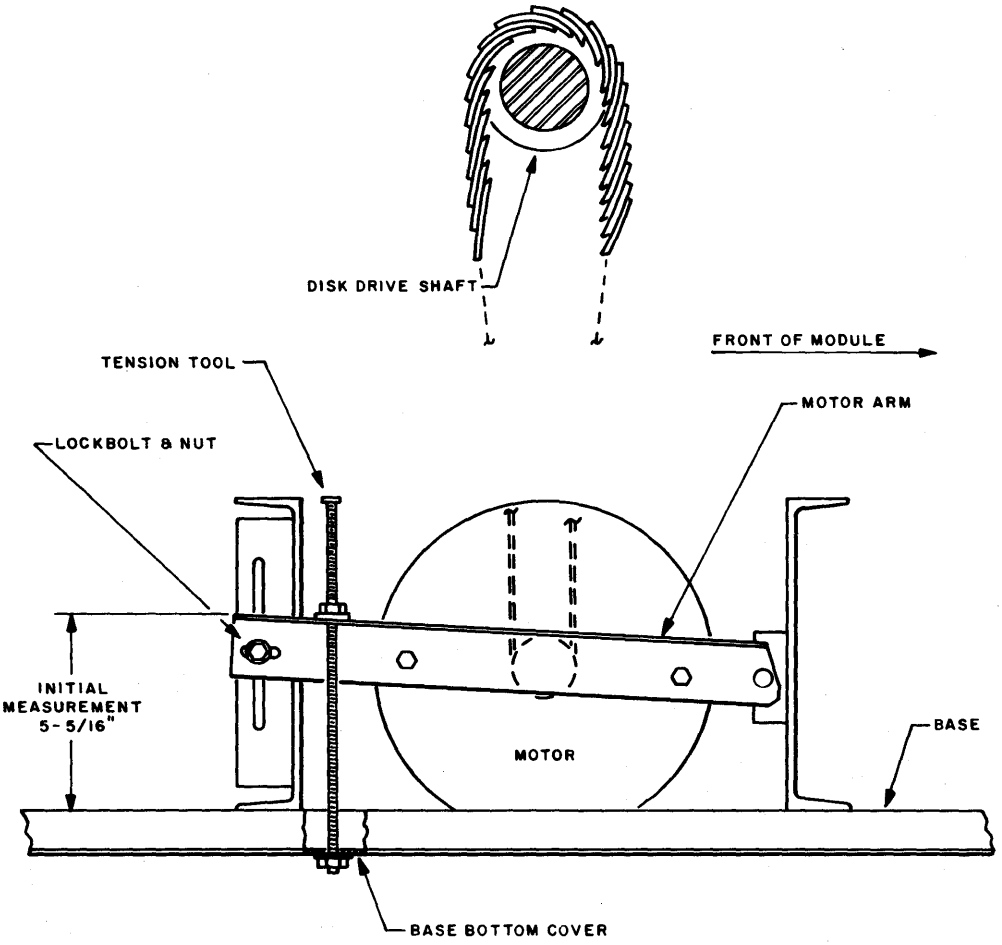


FIGURE 5.5-3
BELT ADJUSTMENT-INITIAL

8. The initial measurement after installing new, pre-stretched belts should be 5 5/16 inches. Using the belt tension tool (P/N 1622 7134), adjust the motor arm clearance to this dimension as illustrated in Figure 5.5-3.

9. Tighten the lock bolt and nut.

NOTE

Perform the belt check outlined in Section 6.3 and adjust if necessary. Make two further checks at weekly intervals and then establish quarterly maintenance from the date of the second check.

5.6 REGULATOR - REMOVAL AND REPLACEMENT

Refer to Section 5.1 for removal of the Module from the garage.

REMOVAL

Before attempting the removal of the Regulator, release air pressure from the manifold.

The Regulator is removed in the following manner: (Refer to Figure 5.6-1.)

1. Remove the plastic air line from the bottom of the Regulator.
2. Remove the two bolts on the inside of the support beam which hold the manifold in place.
3. Remove the nut, washers and "O" ring from the top of the manifold supporting the Regulator to be removed.
4. Remove the nipple hardware from the top of the Regulator.
5. Remove the "tee" from the bottom of the Regulator along with its fittings and gauge.

REPLACEMENT

Reverse the above procedure for replacement of a Regulator. To insure against air leaks, apply sealant (P/N 11117165) to all fittings before assembly, except for the plastic air line. Refer to B471 Technical Manual, page 5.7-1, paragraph 4. Refer to Section 5.21 for adjustment of the Regulator before air pressure is applied.

NOTE

If the new Regulator is a replacement for an old style Regulator (see Figure 5.6-1), then items 13 and 14 on page 6 of the B475.54 Storage Module Parts Catalog must be installed as well.

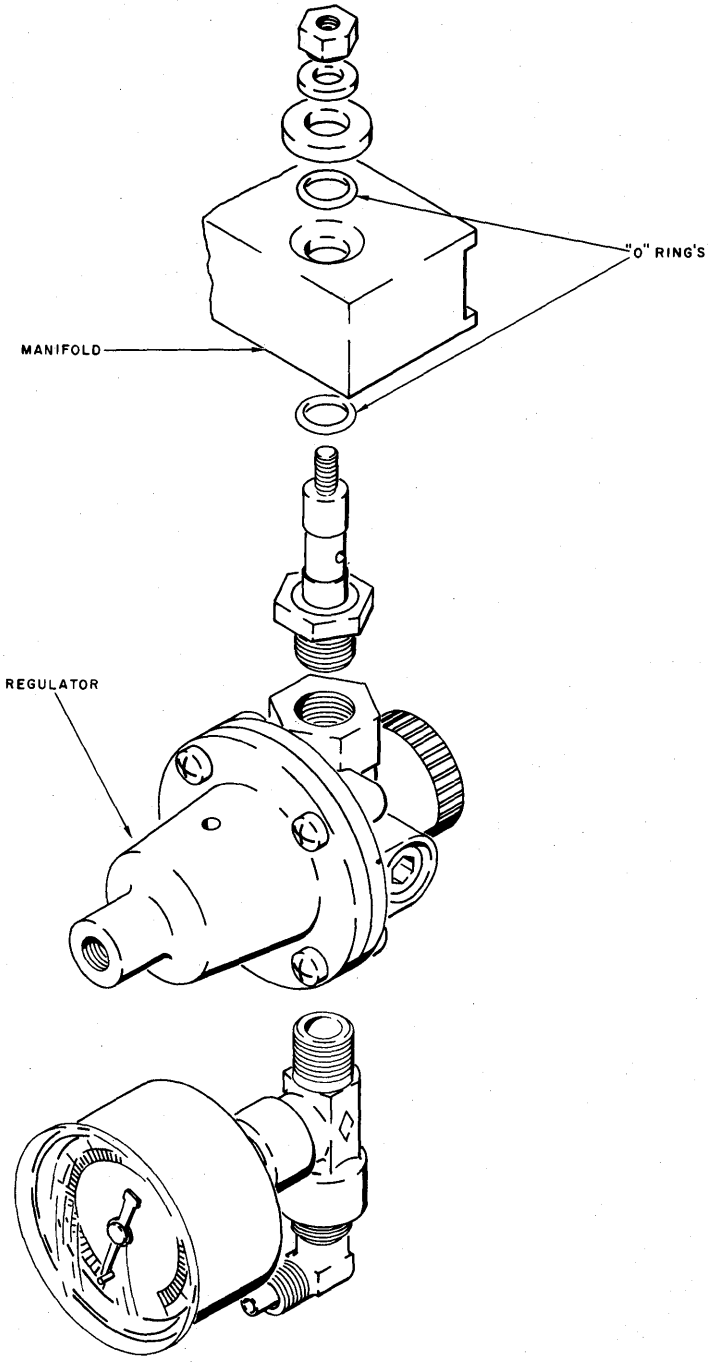


FIGURE 5.6-1
AIR PRESSURE REGULATOR

5.11 VARIABLE BIAS ADJUSTMENT

Before making this adjustment, check the -4.5V supply in the E.U. It must be -4.5V ± .25V.

Check the output of the VB package at AAD1K2. It should be -1.2V.

5.12 CLOCK PRE-AMP GAIN ADJUSTMENT

This adjustment is made at the Manufacturing Plant and under normal circumstances will not be made in the field. The following description of the procedure is for information only.

1. Monitor the signal at the collector of Q3 in the Sense Amp DF (AMSD) for the Bit Clock. Record the baseline to peak signal amplitude for the 12 lower face tracks.
2. Monitor the signal at the collector of Q4 in the Sense Amp DF. Record the baseline to peak signal amplitude for the 12 lower face tracks.
3. Note the highest and lowest signals recorded in Steps 1 and 2. Use the following formula:

$$A = 1.5 + 0.33 \left(\frac{\text{Highest Amplitude}}{\text{Lowest Amplitude}}\right) \text{ Volts (baseline to peak)}$$

4. Monitor the largest signal at the point where it was observed either Q3 or Q4. Set the gain of the lower face Bit Pre-Amp Select 2 so that the signal will be equal to A, the amplitude determined in Step 3.
5. Repeat Steps 1 thru 4 for the 12 upper face Bit Clock Tracks, adjusting the upper face Bit Pre-Amp Select 2.
6. Repeat Steps 1 thru 4 for the 12 lower face Word Mark Tracks. The signal is monitored at the Address Track Sense Amp DF and the gain adjusted at the lower face Address Pre-Amp Select 2.
7. Repeat Steps 1 thru 4 for the 12 upper face Word Mark Tracks. Adjust the gain of the upper face Address Pre-Amp Select 2.

After these gain adjustments have been made in the factory, a record of the amplitude of one track connected to each of the four Pre-Amps is included with the Test and Field Reference documents.

To adjust the gain of a Clock Pre-Amp Select 2, refer to the Test and Field Reference document and adjust for the recorded amplitude. This would apply after replacing a Pre-Amp or as a P.M. check.

5.13 INFORMATION PRE-AMP GAIN ADJUSTMENT

The Pre-Amp Gain Adjustment is made in the Manufacturing Plant and under normal circumstances will not be made in the field. The following description of the procedure is for information only.

1. Force low gain to be selected continuously by grounding the input to the Gain Select Switch, AB9J9 (refer to the B471 Manual, Section 3.8).

2. With GSSL true, monitor the signal at the emitter follower output of the Disk File Clipper (AC1P5).

3. Record the baseline to peak amplitude of the signals from every Zone 1 track on all eight disk faces (400 signals).

4. Repeat Step 3 for Zone 2 tracks.

5. Repeat Step 3 for Zone 3 tracks.

6. Use the following formula with the record made in Step 3:

$$A = 1.1 \sqrt{\frac{\text{Highest Amplitude}}{\text{Lowest Amplitude}}} \text{ Volts (baseline to peak)}$$

7. Set the gain of the Zone 1 Pre-Amp Select 1 for the baseline to peak amplitude A determined in Step 6.

8. Repeat Steps 6 & 7 for Zone 2 and Zone 3.

After these gain adjustments have been made in the factory, a record of the amplitude of one track in each zone is included in the Test and Field Reference documents.

To adjust the gain of an information Pre-Amp Select 1, refer to Test and Field Reference document and adjust for the recorded amplitude. This would apply after replacing a Pre-Amp or on a P.M. check.

5.21 AIR PRESSURE REGULATOR ADJUSTMENTS

Each of the seven regulators must be set to the specific pressure value indicated by the red arrow on the gauge. The regulators must maintain these pressures within a tolerance of +2 -0 psi providing the regulators have been pressurized at least fifteen minutes. Adjustments are made by turning the adjusting screw in or out to raise or lower the pressure respectively. While under pressure, the regulators do not respond accurately to an adjustment intended to lower the pressure of the output. For that type of adjustment, retract the heads to depressurize the regulators, back out the adjusting screw, actuate the heads, and adjust the pressure upward to two psi over the red arrow. After actuating the heads, allow fifteen minutes before taking final gauge readings. Hold the knurled body of the regulator firmly while loosening the adjusting screw lock nut.

ADJUSTMENTS

1. For a regulator with low output, increase the pressure to the proper point by slowly turning the adjusting screw in.

2. For a regulator with an output exceeding its specified pressure by one psi, decrease the pressure with the following method:

   a. Place the HEAD/RETRACT switch in RETRACT.

   b. Back out the adjusting screw 1-1/2 turns.

   c. Place the HEAD/RETRACT switch to HEAD to actuate the heads.

   d. Increase the pressure to the proper point +2 psi by slowly turning the adjusting screw in.

3. Retract and actuate the heads. Check the pressure gauge reading after fifteen minutes.

4. Repeat the above procedure if necessary.

5.22 AIR FLOW CONTROL VALVE ADJUSTMENT

The Air Flow Control Valve is located on the Regulator Manifold and is readily accessible with the logic gate swung open. Refer to Figure 4.4-2. Designate the appropriate module from the Control Unit.

1. Retract the heads. The white NOT READY indicator on the E.U. control panel will go on.

2. Using a 5/64 inch Allen wrench, loosen the lock screw located just below the adjusting nut on the valve.

3. To INCREASE head flying time, turn the adjusting nut counter-clockwise; to DECREASE head flying time, turn the adjusting nut clockwise. Make adjustments in 1/8 turn increments.

4. Fly the heads. Check the time between head actuation and when the NOT READY indicator goes off. This should be from 8 to 9 seconds and may require several adjustments (Step #3) to accomplish.

5. Tighten lock screw.

5.23 BELT ADJUSTMENT

If the motor pulley slips during start up, the motor will speed up causing MSR to pick too soon. This results in the starter windings being cut out before the motor has sufficient torque to carry the load. The motor will then slow down causing MSR to de-energize and the starter windings will be put in the circuit again. This condition, apparent from the audible chattering of MSR, causes additional belt stress and may pick the Motor Overload Relay.

To correct this condition, belts should be adjusted in 1/4 inch increments. After a series of adjustments, the minimum clearance of 4 1/16 inches will be reached as illustrated in Figure 5.23-1. When the minimum clearance is reached, new belts should be installed.

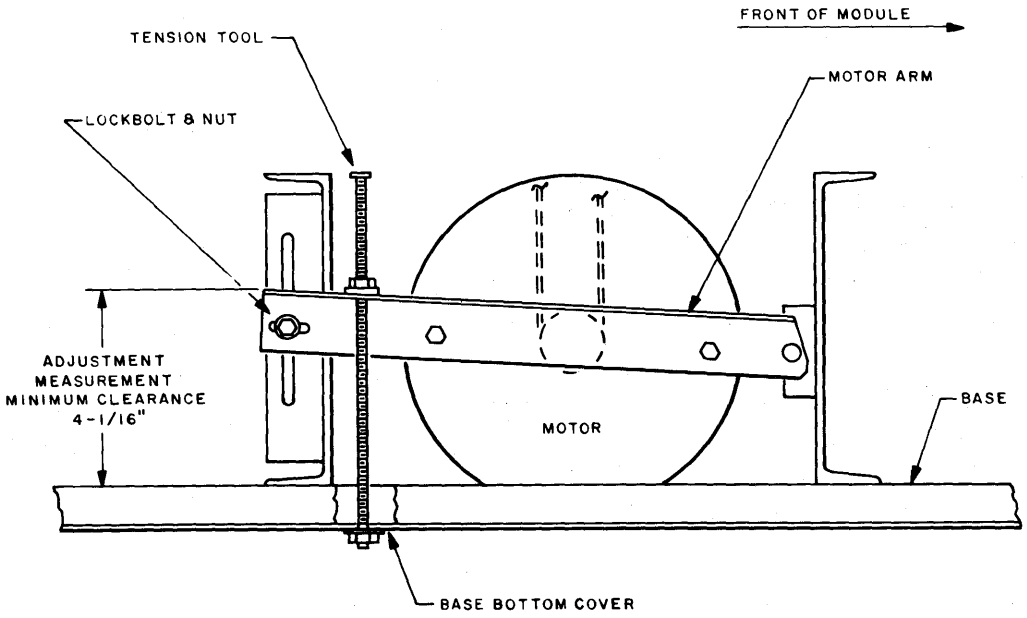


FIGURE 5.23-1
BELT ADJUSTMENT

1. Turn off DC and AC power.
2. Remove the module from the garage as outlined in Section 5.1, but do not disconnect the AC power cable.
3. Refer to Figure 5.23-1.
4. Install the belt tension tool (P/N 1622 7134), and turn down the upper nut until it is against the motor arm.
5. Loosen the lock bolt and nut on the motor arm.

6. Measure the adjustment between the top of the motor arm and the pedestal base as illustrated in Figure 5.23-1. Tighten the belts by decreasing this measurement by 1/4 inch using the tension tool.

   a. If the minimum clearance has not been reached, proceed to Step 7.

   b. If the minimum clearance has been reached, replace both belts. For belt removal and replacement, refer to Section 5.5.

7. Lock the motor arm by tightening the lock bolt and nut.

8. Turn the AC on to start the disk-drive motor.

9. If relay chattering still occurs, turn off the AC to the drive motor, loosen the lock bolt and return to Step 6.

10. If no chattering occurs, turn off the AC to the drive motor and remove the belt tension tool.

11. Replace the module in the garage by reversing the procedure outlined in Section 5.1.

12. Check the unit for "jitter". Refer to Section 6.11.

5.24 AIR TANK PRESSURE SENSING SWITCH ADJUSTMENT

This switch is located at the top of the air tank. Adjust it to open at 35 psi $\pm$ 1 using the following procedure:

1. Turn off the 70 amp circuit breaker. This will prevent the compressor from cycling and remove -24V from the air pressure switch.

2. Open the drain cock of the filter bowl by the top of the tank and lower the tank pressure to 36 psi as measured by the tank gauge. Close the drain cock.

3. Put an ohmmeter across the air pressure switch and adjust the switch so that it is just closed.

4. Lower the tank pressure to 35 psi and check that the switch is open. Readjust the switch if necessary.

5. Close the 70 amp circuit breaker.

Maintenance Procedures and Aids

✓INDEX - SECTION VI

✓Changes or additions since last issue.

6.2 MONTHLY PREVENTIVE MAINTENANCE

1. FILTER

There is one fiberglass disposable filter located at the bottom rear of the unit covering the heat exchange blower motor intakes. It should be checked frequently and changed at least once a month or when necessary.

Since the filter is readily accessible by opening the door at the rear of the unit, power need not be dropped during changing.

2. PRESSURE REGULATORS

The pressure regulators should be checked by monitoring the gauges monthly and each time the heads are actuated. (Allow five minutes for the regulators to stabilize after the heads have been actuated.)

a. Remove the front door from the garage.

b. Check the seven regulator gauges.

c. If any specific pressure exceeds the +2 -0 tolerance, refer to Section 5.21 for adjustments.

3. VARIABLE BIAS

Check -1.2 volt Variable Bias. Refer to Section 5.11 for adjustment procedure.

4. INFORMATION AND CLOCK PRE-AMPS

Pre-Amp settings must be checked on a monthly basis. Use the following procedure when verifying these settings.

Bit Track Pre-Amps

a. Select the lower Bit track specified on Form 39335.

b. Monitor the signal at the collector of Q3, Sense Amp DF (AMSD - AAA1N2).

c. Sync on INXP at the E.U. Maintenance Panel.

d. Observe the Bit track for one revolution; the amplitude of the largest pulse (zero to peak) in that track must be set to the voltage recorded on Form 39335.

e. Select the upper Bit track and repeat Steps b, c and d.

Address Track

a. Select the lower Address track specified on Form 39335.

b. Monitor the signal at the collector of Q3, Sense Amp DF (AMSD - AAA2N2).

c. Sync on INXP at the E.U. Maintenance Panel.

d. Observe the Address track for one revolution; the amplitude of the largest pulse (zero to peak) in that track must be set to the voltage recorded on Form 39335.

Information Pre-Amps

a. Force low gain to be selected by grounding the input to the Gain Select Switch in the E.U. (AAB9J9).

b. Monitor the signal at the emitter follower output of the Disk File Clipper (AC1P5).

c. Sync on INXP at the E.U. Maintenance Panel.

d. Select the information track for Zone 1 as specified on Form 39335.

e. Observe the information track for one revolution; the amplitude of the largest pulse (zero to peak) in that track must be set to the voltage recorded on Form 39335 for that zone.

f. Repeat Steps d and e for Zone 2 and Zone 3.

5. PURGE UNIT

If there is a purge unit on site, perform the following check monthly:

a. Remove both top hoses from the stop bracket. Leave the intake hose between the stops.

b. Disconnect the tube connected to the bottom part of the pressure gauge. (Tube from upper part of purge unit.)

c. Start the blower and read the gauge.

d. Remove the fiberglass pre-filters from the intakes and read the gauge again.

e. Change the pre-filters if the difference in readings is more than .4.

6. AIR FLOW CONTROL VALVE

The Air Flow Control Valve regulates the speed in which the heads travel from their retracted positions to their flying positions. It should be checked monthly using the following procedure:

a. Retract the heads. The white NOT READY indicator on the E.U. control panel will go on.

b. Fly the heads. The time between head actuation and when the NOT READY indicator goes off should be from 8 to 9 seconds.

If adjustment is necessary, refer to Section 5.22.

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6.3 QUARTERLY PREVENTIVE MAINTENANCE

1. BELTS

The linked disk drive belts should be checked quarterly to insure against excessive slippage.

a. Remove the front door from the garage.

b. Place the Head/Retract switch in "Retract".

c. Place the Motor/On switch in the Off position.

d. Allow the disks to come to a complete stop.

e. Place the Motor/On switch in the On position and listen for audible chattering of the MSR relay while the disks are accelerating. The disks must be up to speed within 60 seconds.

f. If chattering occurs or the disks are not up to speed, refer to Section 5.23 for adjustments.

g. If no chattering occurs, restore the module to normal operation.

NOTE

Between PM periods, the Field Engineer should not overlook any AC "start up" of a module as an opportunity to listen for MSR chatter caused by belt slippage.

2. PURGE UNIT

If there is a purge unit on site, perform the following check quarterly:

a. Remove both top hoses from the stop bracket. Leave the intake hose between the stops.

b. Remove the pre-filters.

c. Start the blower and read the gauge.

d. Change the absolute filter if the gauge reads more than 2.

e. First remove the two upper hoses.

f. The absolute filter is replaced with a Cambridge Absolute Filter, Model 1A-200-2 or equivalent.

g. The absolute filter must seat properly against the back-up plate gasket to insure dust-proof seating.

h. After installing a replacement filter, the upper (clean air side) part of the filter and the purge unit must be thoroughly cleaned by vacuuming and wiping with Freon TF and lint-free wipers.

i. After the initial cleaning, put pre-filters in position and run the purge unit for 72 hours.

j. Stop the unit and wipe out the upper part by reaching through the openings.

k. Run the unit another 10 minutes.

l. Replace the upper hoses.

6.5 ANNUAL PREVENTIVE MAINTENANCE

1. FANS

The three cabinet exhaust fans located on the inside rear skin of the garage assembly should be oiled annually using the following procedure:

Oil	EDD Part #11838596
Oil injector	EDD Part #11838588

a. Remove air from oil injector by holding the needle up and pressing on the plunger.

b. Project the injector needle through the louvres (in back skin) and place the needle at the center of circle marked on the gold label.

c. Position the needle at an angle of approximately 45° to the label surface and point it toward the center of the rubber cap. (These fans are lubed by inserting the oil injector needle through a self-sealing rubber cap located in the center of the motor hub.)

d. Pierce the label and the concealed self-sealing rubber cap located under the label.

e. Insert the needle approximately 1/4".

f. Depress the plunger of the oil injector approximately 1/16" to force the oil to flow. Rotating the fan will relieve air pressure and allow oil to flow into the oil chamber.

6.6 "TOUCH" PROCEDURE

When a Storage Module goes Not Ready as the result of a "touch", the field engineer should be aware of the potentially hazardous condition which exists.

DO NOT immediately attempt to re-fly the heads by hitting the Touch Reset button. This would not only remove the indication of which disk face the "touch" occurred on but, if the "touch" had damaged the disk, more widespread damage will result.

The field engineer should proceed as follows: Check the eight outputs of the TUDL packages to determine on which disk face the "touch" occurred. Refer to Section 3.5 of the B475 Technical Manual and Logic Schematics 25.00.20.0 and 25.00.21.0. The outputs of the packages are normally true, but when a "touch" is sensed, the output is latched false (ground).

Having determined the disk face, do not open the disk enclosure but use a trouble-light or flashlight and carefully check the disk face for scratches. If no signs of damage can be seen, inspect the bottom of the disk enclosure for foreign particles (dirt, brass filings, white granules, etc). If the disk face is scratched, the module must be returned to Pasadena for repair and a replacement ordered. If there are foreign particles in the disk enclosure, shut down the unit and, using a purge unit, open the disk enclosure to determine what is damaged.

If the disk face is not scratched and there are no other visible signs of damage, proceed as follows: Reduce all seven pressure regulators by three turns counter-clockwise. Hit the Touch Reset switch and fly the heads. Adjust each regulator to normal setting in the following sequence: 1, 7, 2, 6, 3, 5 and 4. If a "touch" occurs, one of the two heads controlled by that regulator (the disk face already has been determined) can be assumed to be flying incorrectly. The module must be shut down and, using a purge unit, the disk enclosure should be opened and the heads examined.

If all the regulators are restored to normal without another "touch" occurring, the original "touch" possibly was caused by a small dirt particle which did not scratch the disk or a sensitive TUDL package or noise on the touch circuit. Normal operation may be resumed, keeping a check for pressure regulator drift.

6.7 LOCATING HEAD FAILURES

This section is written as an aid in the location of head failures. It starts by listing some typical symptoms which may be encountered, gives a systematic procedure for locating and checking the head, and explains some possible troubles which may occur that have the appearance of, but are not head failures.

Due to the large expense and time involved in the changing of a head, the engineer should attempt to rule out all other possible causes for the failure before performing the change. When a head is definitely found bad, always verify its correct location before changing. Use the correct Head Locating Chart, Figure 5.4-1, for 240 C/S option, Figure 5.4-2 for 480 C/S option or Figure 5.4-3 for 96 C/S option.

Listed below are some of the symptoms encountered in head failures. The list, of course, cannot cover each and every case; it is meant, rather, to aid the engineer in recognizing the most common types of failures.

1. Information parity errors during a read operation. Failures occurring consistently or intermittently on a group of sequential segment addresses associated with one specific information track. For example: A 240 character option, track 27, segment addresses 00 through 23; a 480 character option, track 99, segment addresses 62 through 77; a 96 character option, track 00, segment addresses 140 through 249. Note the segment address groups given in the examples are those of complete zones.

   This is the most common type of head failure: One track, in one zone, on one disk face, and in one module. For verification, set up the following conditions:

   D.F.C.U. to LOCAL

   READ/WRITE Switch to READ

   N-SET Switch to 2

   ERROR STOP Switch ON

   By use of the indicator-switches, set the failing address in the A Register with the segment address portion equal to the lowest numbered segment in the zone. This will be the address of the first segment in the zone. Depress the MAINTENANCE START Switch. If the track in question is bad, the Control Unit should stop with SOlF true indicating an error. Keep depressing MAINTENANCE START observing the segment address portion of the A Register; it should step sequentially through the entire group of failing addresses with a constant error. When the A Register reaches the last segment in the zone, one more depression of the switch should increment the A Register and select a different track. With this, the file should run continuously until stopped.

Reset the A Register to an all zero address. Depress MAINTENANCE START and observe the A Register as it increments through the file; it should stop with an error on the first segment of the failing track. Depress MAINTENANCE START continuously, as done earlier, until the A Register again selects another track and runs continuously. Let the operation continue until the end of the file is reached; this is to insure that there are no other failures in the file which may be common to the track in question.

Before continuing, some important points should be brought out on the procedure thus far. By letting the file read sequentially from beginning to end, assuming no failures other than the track in question, eliminates a number of possible causes for the failure. First, since information was successfully read from the zone associated with that of the failing track and from the same zone on other disks in the module, the possibilities of a defective Information Pre-Amp, Write Driver, Head Select Driver, Head Isolation Diodes, and Air Pressure Regulator setting, as well as zone, track, disk face, disk, and module select levels are eliminated. Second, since the failure occurred on all segment addresses in the zone, first revolution cross-over timing and the possibility of failures occurring in the first or second revolution only are eliminated.

If not done previously, the engineer should now determine exactly the head assembly, disk, disk face, zone, center tap select line (HSDL), and Write Driver associated with the failing track.

Change N-SET Switch to 1 and throw ERROR STOP Switch OFF. Set the failing address in the A Register and depress MAINTENANCE START. The file should read one segment from the failing track continuously. Set the scope up to read a DC voltage level and scope the output of the selected Write Driver at the collectors of Q3 and Q4; that is, pins B3, K3 or P3, X3 (refer to Figure 3.8-5). Normally, during a read, these points should be slightly less than +12V which is the center tap voltage from the Head Select Driver. If either the "0" or "1" side of the head is open, the corresponding output will be slightly less than ground, or around -0.3 to -0.5 volts. If these conditions exist, the head is definitely open and should be changed. If, however, both outputs are the normal +12V indicating an open condition does not exist, the head has probably lost its ability to "erase" flux changes properly and is leaving residual "noise" in the information track. This noise can be of sufficient amplitude to trigger the Information Pre-Amp during readback.

Leaving the track selected, set the scope up as follows:

Sync EXT. POS. on ICFF/ at the E.U. Maintenance Panel.

Set TIME/CM to view two words of the selected track.

Attach the A trace probe to one of the outputs of the Gain Controlled Sense Amp (AAD2F2 for the "1" side or AAD2E2 for the "0" side).

Sync the scope and observe the peak-to-peak noise level of the first word; a level greater than 1.2 volts will exceed the threshold in the Disk File Clipper and trigger the read circuitry. Noise of this sort also has a tendency to be impressed on legal flux changes and can be seen as spikes "riding" the sides of the readback sine wave. To get a proper signal-to-noise ratio, compare other tracks to the track in question.

2. Information parity errors during a read operation. Failures occurring consistently or intermittently on a group of sequential segment addresses associated with all the tracks in one head assembly. From the standpoint of addressing, tracks will either be even, in the case of a lower head, or odd for an upper head; this is true regardless of the character option used. For example: The even numbered tracks between 00 and 24 are on lower heads 2 (Zone 1), 8 (Zone 2) and 12 (Zone 3); odd numbered tracks between 01 and 23 are on upper heads 1 (Zone 1), 5 (Zone 2) and 11 (Zone 3). The groups of segment addresses used as examples in symptom 1 could be applied here also. The engineer should fully understand the addressing scheme for the character option he is working on in order to be able to determine exactly the module, disk, disk face, zone and head assembly.

   The only components common to a single head assembly are the Head Isolation Diodes so this is the most likely cause of the failure. Since these diodes, two per head assembly, are mounted on the Head Support Boards and, like head assemblies, will require opening the disk enclosure to change, all other possible causes should be examined and ruled out before performing a change. To check, use a similar procedure as outlined in symptom 1. First, step through each of the failing tracks using the MAINTENANCE START Switch and A Register indicator switches. Second, reset the A Register to an all zero address and read the entire file to insure no other failures. Then scope the selected Write Driver; it should give the same indications except now all tracks in the head assembly will appear open.

Listed below are some symptoms which may, at first inspection, have the appearance of head failures:

1. Information parity errors during a read operation. Failures occurring consistently or intermittently on the group of sequential segment addresses associated with one zone, on all disk faces of one module, and on the sequential tracks associated with a pair of interlaced heads. For example: In a 240 character option, segment addresses 56 through 99 (Zone 3) on all disk faces, tracks 00 through 24 for the lower faces and 50 through 74 for the upper faces (heads 11 and 12). From the standpoint of addressing again, in a 240 character option the complement of track 00 on a lower face would be track 50 on an upper face, 01 and 51, etc.

The only factor common to interlaced head pairs on all disk faces is the Air Pressure Regulator associated with them; this would be the probable cause. Refer to Section 5.21 for the Regulator adjustment procedure.

2. Information parity errors during a read operation. Failures occurring consistently or intermittently on the group of segment addresses associated with one zone, both faces of one disk, and all tracks in the zone. For example: In a 96 character option, disk 3 of a module, zone two segment addresses 060 through 139 (lower face) and 310 through 389 (upper face), and tracks 50 through 99 on both faces. From the standpoint of addressing again, tracks 50 through 99 apply to both faces of disks 3 and 4 in a 96 character option module.

   The common component to one zone, one disk, both faces and all tracks in the zone is the associated Write Driver. Use a similar checking procedure as done in symptom 1 and, for further verification, plug the suspected Write Driver into one of the other 11 locations and run a similar check.

3. Information parity errors during a read operation. Failures occurring consistently or intermittently on one track and group of segment addresses associated with either the upper or lower faces of all disks, in all modules associated with an E.U. For example: In a 480 character option, tracks 05 (disks 1 and 3) and 55 (disks 2 and 4), and segment addresses 00 through 99 on all modules.

   The common component here is the Head Select Driver associated with the track. This can readily be seen since the failure occurs in all modules. To check, set the scope up to read a DC voltage level and monitor the selected HSDL level at the E.U. gate. It should be +12V when selected and ground when unselected; in this case, it is probably at ground disabling the track in all modules.

   Another common failure in this category is that of two HSDL levels being selected simultaneously. With this condition, two heads will attempt to write flux changes at the same time while sharing the write current normally supplied for one head. The resultant information written in both tracks will be ragged and low in amplitude causing errors during readback. To check, set the failing address in the A Register and carefully scope all 100 HSDL levels at the E.U. gate; only the one selected should be at +12V, all others must be ground. Even a small positive voltage can sufficiently forward bias head diodes and cause this type of failure.

6.8 COMPONENT LOCATIONS

Refer to the following figures as an aid in locating Storage Module Components:

1. DA RACK LOCATOR - STORAGE MODULE LEFT VIEW - Figure 6.8-1
2. DA RACK LOCATOR - STORAGE MODULE RIGHT VIEW - Figure 6.8-2
3. STORAGE MODULE RACK A COMPONENTS - Figure 6.8-3
4. STORAGE MODULE RACK B COMPONENTS - Figure 6.8-4
5. STORAGE MODULE RACK C COMPONENTS - Figure 6.8-5
6. STORAGE MODULE AIR SYSTEM COMPONENTS - Figure 4.4-1

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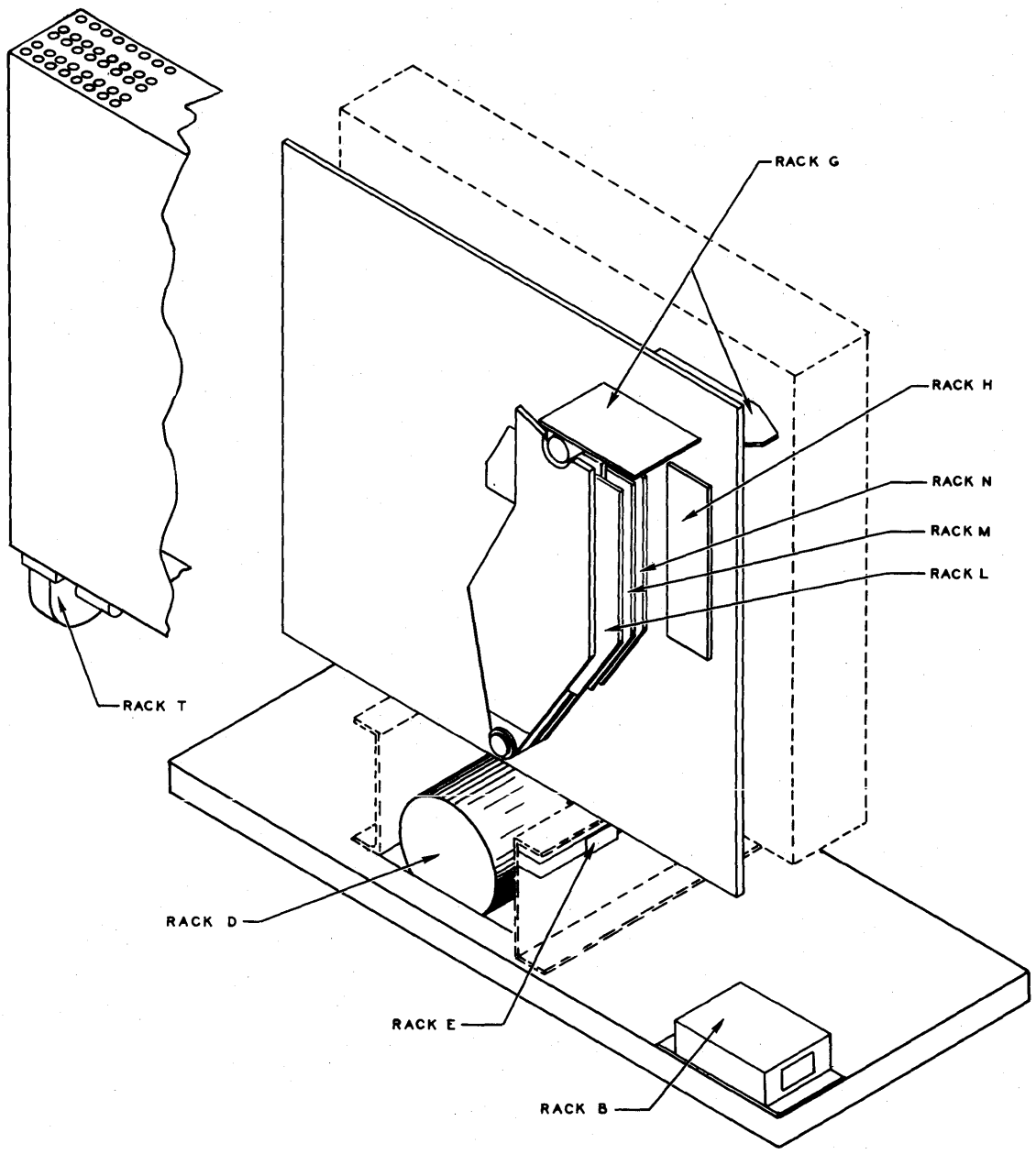

FIGURE 6.8-1
STORAGE MODULE LEFT VIEW

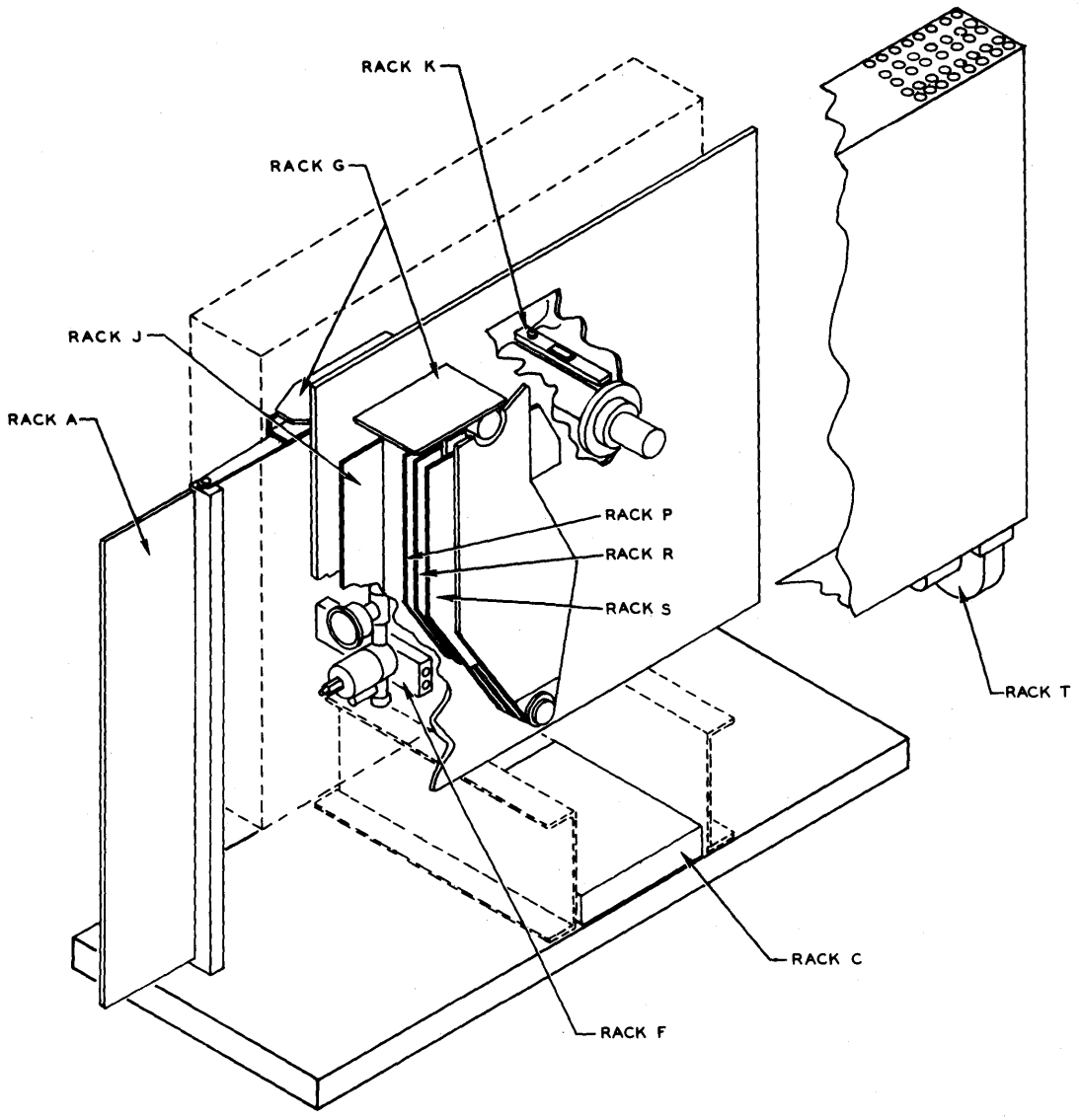

FIGURE 6.8-2
STORAGE MODULE RIGHT VIEW

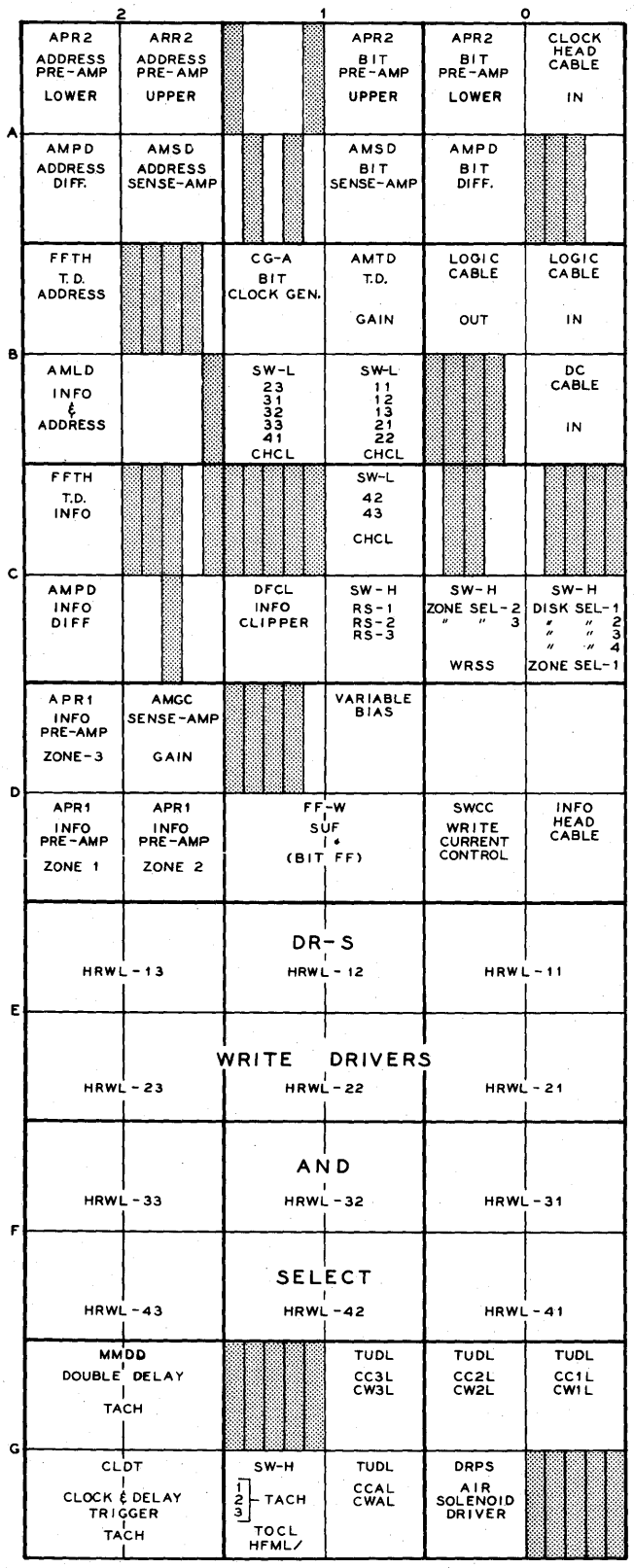

FIGURE 6.8-3
RACK A COMPONENTS

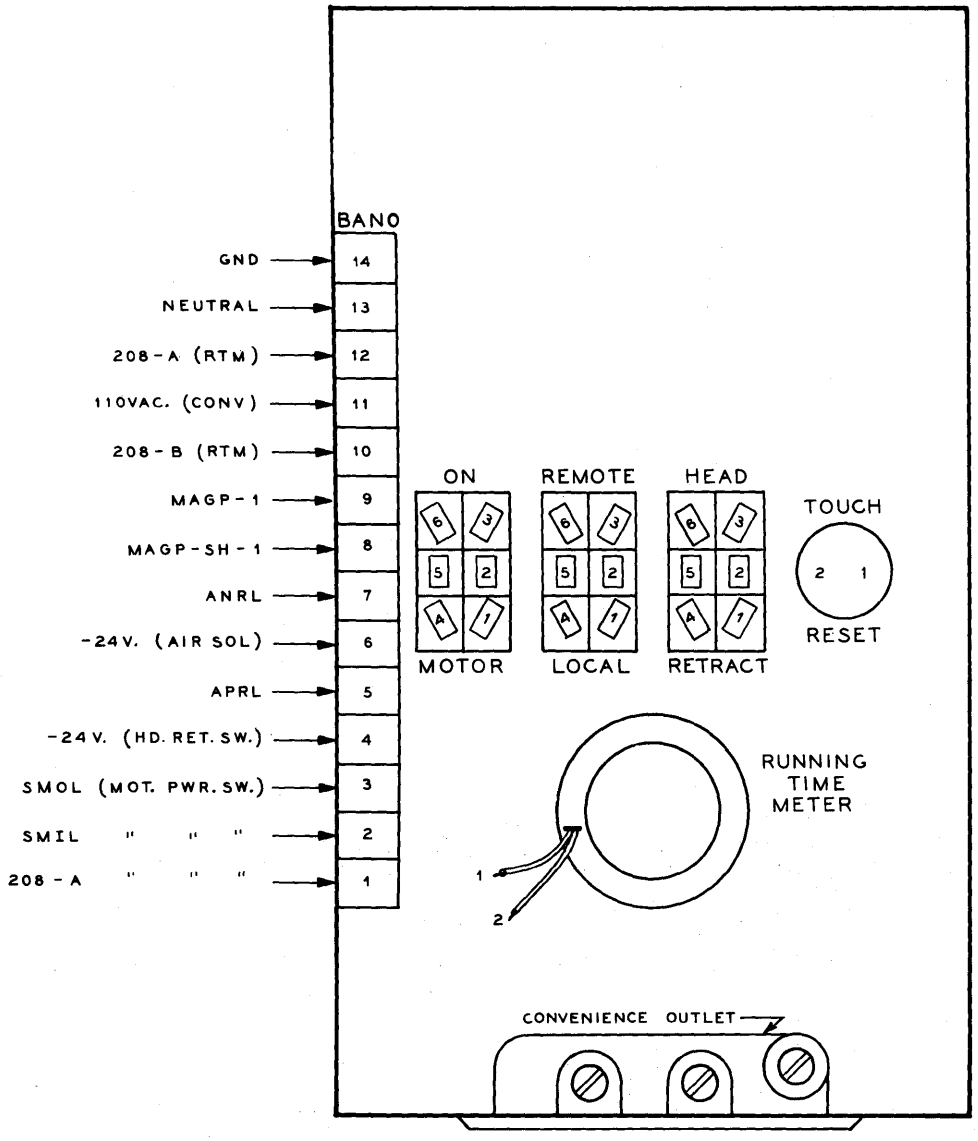

FIGURE 6.8-4
RACK B COMPONENTS

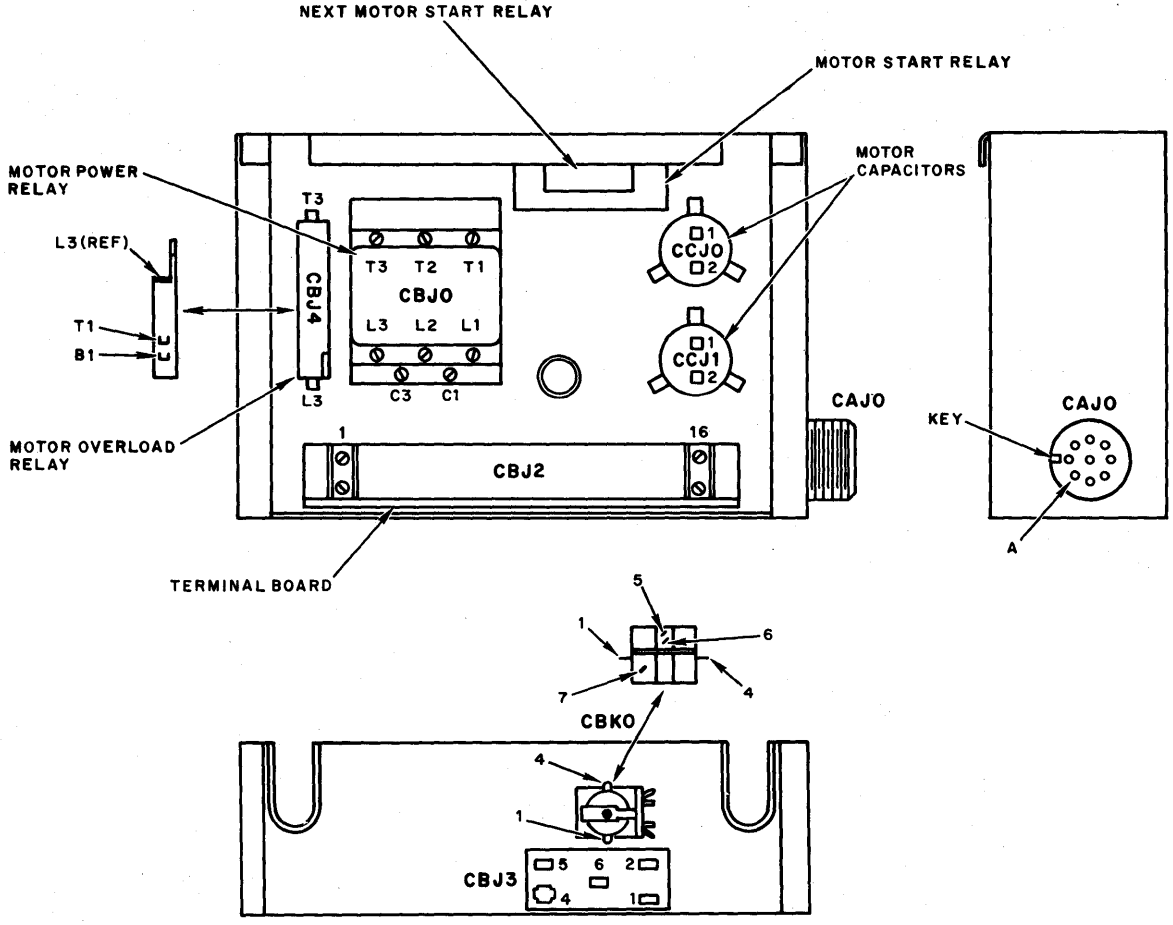

FIGURE 6.8-5
RACK C COMPONENTS

6.9 TEST ROUTINES

The following are the Test Routines available for use with the Disk File Subsystem and a brief description of their use.

B200 - TR 2122 This routine will test the subsystem under the control of the B200. The operator has control of the program section to be run by use of the Operator's Panel. The routine is made up of eight sections and will test any and all subsystem configurations and character options.

B5000 - TR 5561 This routine will test the subsystem under control of the B5500. The operator has control of the program section to be run by the use of the Supervisory Printer. The routine is made up of three sections and will test any and all subsystem configurations and character options.

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6.10 TESTING FOR "JITTER"

The varying time relationship between information pulses and clock pulses is known as "jitter". The primary cause of "jitter" is mechanical vibration. The maximum effect is noticed in the first track of the disk face as this head is furthest away from the clock head.

Excessive "jitter" can cause intermittent read failures in Zone 1. To check the amount of "jitter", use the following procedure:

1. (a) Set up the D.F. Control for a one-segment write with recycle off.

   (b) Set BA1F, BB1F, BC1F and BD1F.

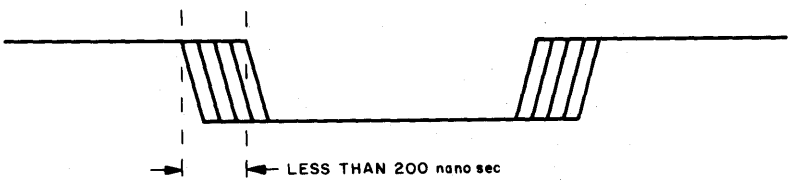
   (c) Write one segment in the first track of each disk face. for a 240 C/S option, addresses 00000, 05000, 10000, 15000, 20000, 25000, 30000 and 35000. For a 96 C/S option, 00000, 00250, 00500, 00750, 50000, 50250, 50500 and 50750.

   If writing in these locations would interfere with the customer's permanent file, then the above addresses can be modified with the addition of a 5 in A6 to address Maintenance Segment 1.

2. (a) Set up the D.F. Control for a one-segment read with recycle on.

   (b) Sync the scope externally positive on the ICFF/ test point. Put one trace on AAC7C4 in the E.U. This is the IRAS line. Time base 0•5 microsec/cm and 5X magnifier on.

   (c) Execute read cycles on the addresses previously written. Measure the amount of "jitter" on each face (see sketch below). It should not exceed 200 nanosec.



3. If "jitter" does exceed 200 nanosec., the most probable cause of mechanical vibration is the drive belt adjustment. Refer to Section 5.23. Reduce belt tension by raising the motor arm 1/8 inch. Check "jitter". If necessary, this adjustment may be repeated ONCE.

Increase belt tension in two 1/8 inch increments from the original setting. Check "jitter" after each increment. If the final optimum adjustment results in reduced belt tension, shut the motor off and allow the disks to come to a complete stop. Then turn the unit on and check for belt slippage (indicated by relay chatter).

Other sources of mechanical vibration are the two heat exchange blowers.

6.11 TEST AND FIELD REFERENCE DOCUMENT - FORM 39335

The Test and Field Reference Documents supplied with each Storage Unit will include Form 39335. The information recorded on this form contains the following.

INFORMATION SIGNAL REFERENCE

Address of the reference track in each zone and zero to peak voltage setting of each zone pre-amp. These are the highest amplitude heads.

CLOCK SIGNAL REFERENCE

Address of the upper and lower clock reference tracks and zero to peak voltage setting of each clock pre-amp.

LOW AMPLITUDE HEADS

1. Address of information head with lowest read signal in each zone.

2. Address of clock heads with lowest read signal.

DEAD SPACE INDEX

If a disk has a flaw in dead space, the address of the track where the flaw in dead space occurs will be recorded.

NOTE

The five-digit address information is recorded as it would appear in the Address Register of the D.F.C.U.

SPARE TRACK STATUS

When spare tracks are utilized to mask disk flaws, the following information will be recorded.

Face __#__.

Disk face utilizing spare track (1 through 8 from left to right).

Heads __#__ and __#__ interchanged.

If a flaw appears under a head assembly in which there is no spare head, the head connectors will be plugged into different locations on the "C" board as follows:

Flaw under head assy.	Connectors Interchanged
2	2 & 4
3	3 & 1
7	7 & 5
8	8 & 6
12	12 & 14
13	11 & 13

Head __#__, pins __#__ and __#__ interchanged.

The head number utilizing the spare track and the numbers of the two center tap pins interchanged.

A short piece of black tubing slipped over each of the two wires will flag the wires at the head connector which were interchanged.

6.12 RIN INDEX FOR DISK FILE STORAGE UNIT 11986924

RIN NO.	INSTALL. TIME IN HOURS	PRE-REQUISITE	UNITS AFFECTED	DESCRIPTION
4805	1.5	None	101 ⇒ 339	FF line driver improvement.
4806	2.5	None	101 ⇒ 339	Pre-Amp oscillation damping.
4816	3.0	None	101 ⇒ 339	Isolates vibration between motor & assembly.
4822	1.0	None	101 ⇒ 339	Undesignated module write inhibit.
4825	0.5	None	101 ⇒ 339	WICD level removal from Write FF.

✓ INDEX - SECTION VII

✓ Changes or additions since last issue.

7.1 INSTALLATION

This procedure begins after the Module and garage parts have been unpacked. For pre-installation instructions, refer to Installation Planning, Field Facilities, Pasadena, California.

GARAGE

For garage erection procedure, refer to special instruction packet included with each Disk File Subsystem. This packet will normally be taped to one of the garage skins. After the garage has been erected, it should be leveled using the adjustable legs.

PRE-CABLING

1. Remove the shipping bolt on motor clamp bracket. This bolt is used to prevent motor arm from vibrating out of adjustment during shipment.

2. Check plug-ins on logic gate for tightness and correct locations. Refer to Figure 6.8-3.

   NOTE

   Each Module attached to an E.U. will have one terminator stick in location AAB0Y9. The last Module only, however, should have three additional terminator sticks in locations AAB0Y6, AAB0Y7 and AAB0Y8. Refer to DA Schematic page 25.00.10.0.

3. Check entire Module for loose nuts, bolts, etc.

4. Vacuum entire Module.

CABLING

The following steps should be done in sequence:

1. Mounted on the inside of the rear skin of each Module garage are three Rotron muffin fans. The left and right fans are 115VAC wired in series and the center fan is a 208VAC wired in parallel. There are two AC wires (Legs A and B, 208VAC) on terminals 1 and 4 of the small terminal board mounted directly below the fans (DA location UAJ2). For Module 1, these wires route through the small access hole provided in the E.U. side closest to the Module and attach to terminals 1 and 4 of the small terminal board mounted below the E.U. muffin fans (DA location NAK1). For Modules 2 through 5, these wires route to terminal board UAJ2, terminals 2 and 3, in the preceding Module.

2. Roll Module up to garage and connect AC cable. This cable should route over the rear cable tray and down the right side of the Module to its connector. Roll Module into garage, making sure the AC cable does not pinch between the base assembly and the garage.

3. Connect Module air line to main air trunk line at "TEE" connector mounted on front cable tray.

4. Connect the three center tap select cables to their respective locations at the center tap distribution board (Rack G).

5. Connect DC cable (red quad) to logic gate, location AAB0N2.

6. Connect logic cable (green quad) to logic gate, location AAB0A2.

7. Connect ground cable to logic gate ground bus bar using third mounting bolt from top.

8. Connect short, base ground cable at front lower left of Module to garage frame using mounting hole provided.

9. Plug Maintenance Panel power stick into logic gate, location AAG0Y0.

All other interconnecting cables between the E.U. and first Module and between Modules should be routed on the front cable trays of each Module. Only the AC cable routes on the rear cable tray.

After cabling the units, check for pinches, binds and unusual stress on all cables. Special care should be taken with the Rack G connectors; the printed circuitry may be damaged easily.

PRE-POWER

Set the Maintenance Panel switches to the following:

Head Retract Switch to RETRACT.

Motor Switch to ON.

LOCAL-REMOTE Switch to REMOTE.

Power may now be turned on at the E.U. The heads may be flown after DC is up by throwing the Head Retract Switch to FLY.

7.2 ADDING A MODULE

Use the following procedure when adding a second, third, fourth or fifth D.F.S.U. to an E.U.

1. The module shipment should consist of:

   a. The module itself, with logic gate, internal cabling and extender air line with TEE connector.

   b. A complete set of required inter-unit cables--one AC (cannon), one DC (red quad.), one logic (green quad.), one logic ground wire and three head select.

   c. A garage kit which is an extension to the existing garage.

   Carefully check all items for proper quantity and type.

   NOTE

   Insure that the module received is the correct character option. All modules attached to any one E.U. must be the same.

2. Drop all power at the E.U. and open the 15, 50 and 70 amp circuit breakers.

3. Remove the module, which at present is the last module, to allow access to the inside of the garage.

4. Remove the side panel (#11067618).

5. Install the additional bottom rear and top rear spacers (#11071552) to the support frame.

6. Attach support frame assembly (#11071891) to spacers.

7. Install AC cable tray (#11145471), front cable tray assembly (#11068087) and support spacer (#11088077) between support frames.

8. Install rear panel assembly. This consists of the rear upper panel (#11124591) with three Rotron fans attached and the rear lower panel (#11124476) which is a hinged door.

9. Hook up power to the fans by attaching the two AC leads to terminals 2 and 3 of the terminal strip on the preceding module's rear panel--DA location UAJ2.

10. Install side panel, removed in Step #2, to frame support added in Step #4.

11. Route AC cable over the AC cable trays and feed the lugged ends through the rear access hole in the side of the E.U.

12. Hook seven of the nine lugged unds of the AC cable to their proper bus bar output terminals at Rack E, Panel A.

    Use the following table in conjunction with Figure 5.4-1, B471 Technical Manual, for correct terminal and wire color code:

Color Code	Voltage	Location
Solid white	208-A	EAJ0
Red/white	208-B	EAK0
Violet/white	208-B	EAL0
Green/white	Neutral	EAM0
Orange/white	Ground	EAN0
Black/white	-24V	EAP0
Brown/white	208-B	EAR0

    The two power control wires, color coded yellow/white for SMIL and blue/white for SMOL, hook to terminal strips ECL0 and ECK0. Refer to Figure 3.1-1, B471 Technical Manual, for rearrangement of existing wiring to accommodate the added module.

13. Remove the extender air hose with TEE connector from the module to be added. Install this on the front cable tray using bracket provided and hook up extender air hose to TEE connector in preceding module.

14. Route DC cable and logic ground wire across front cable trays and feed the lugged ends into the front access hole in the side of the E.U.

15. Hook the seven lugged ends of the DC cable and logic ground wire to their proper bus bar output terminals at Rack E, Panel B.

    Use the following table in conjunction with Figure 5.4-1, B471 Technical Manual, for correct terminal and wire color code:

Color Code	Voltage	Location
Orange/white	-4.5V	EBJ0
Blue/white	-20V	EBK0
Yellow/white	+20V	EBL0
Red/white	-24D	EBM0
Solid white	+12V	EBN0
Brown/white	-12V	EBP0
Black/white	Ground	EBR0
Solid green	Ground	EBR0

16. Roll preceding module, removed in Step #3, back into its garage and re-cable.

17. Connect the three head select jumper cables to the center tap distribution board and let the ends rest in the front cable tray of the added garage. Do likewise with the logic jumper cable which connects to the gate.

18. Install top panel (#11071545).

19. Install the two hinges, left half support (#11035953) and right half support (#11035961), and panel lid (#11125325).

20. Perform PRE-CABLING and Steps #2 through #9 of CABLING in Section 7.1 of this manual.

NOTE

Pay special attention to the note in Step #2 of PRE-CABLING which concerns the terminator sticks in the module gate.

21. The front panel assembly (#11125762), removed in Step #3, will differ from the front panel assembly (#11103371) sent with the garage kit. Assembly #11125762 has a Burroughs nameplate and should be used with the added module.

22. Perform PRE-POWER check in Section 7.1 of this manual.