Burroughs

B 5370

POWER SUPPLY AND REGULATORS

TECHNICAL MANUAL

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SECTION 1

PREVENTIVE MAINTENANCE

1.1 DAILY

Not Applicable.

1.2 WEEKLY

1. Monitor all AC and DC voltages from the Power Supply meters.
2. Check fan operation.

1.3 MONTHLY

1. Inspect the air filters and replace if necessary.
2. Clean fan screens.

1.4 QUARTERLY

1. Verify voltage sensing. Refer to Section 5.6 for procedure.

2. Monitor the voltage regulator outputs according to Section 5.5. Use a precision voltmeter.

3. Check terminals for tightness.

1.5 SEMI-ANNUALLY

1. Scope all DC supplies for ripple. For ripple specifications, see Table 5.6-1.

2. Check the DC meter and the ammeter for proper adjustment. See Section 3 for adjustment procedure.

3. Visually check all capacitors for any leakage and replace if necessary.

4. Lubricate Rotron Muffin fans with Anderol L-826 using special oil injector.

Oil injector .... Part No. 11838588
Oil ..... Part No. 11838596

PROCEDURE

The exhaust fans are lubricated by inserting the Oil Injector needle through a self-sealing rubber cap, located in the center of the motor hub.

NOTE

On most units, a Gold Seal label is mounted over the rubber plug. This series of fans is called the Gold Seal series.

There are 8 fans in the Power Supply. Five are located at the top of the cabinet, and three directly above the transformers. These three are accessible by removing two screws and swinging the assembly down. The assembly is hinged to allow this access.

1. Fan grill, remove and clean as necessary.

2. Remove air from Oil Injector by holding the needle up, and pressing on the plunger.

3. Place Oil Injector needle at the center of circle marked on the Gold label (on the 034 series, place the needle approximately 1/8" from the edge of the rubber cap).

4. Position the needle at an angle of approximately 45 degrees to the center of the rubber cap.

5. Pierce the label and the concealed self-sealing rubber cap located under the label.

6. Insert the needle approximately 1/4" deep.

7. Depress the plunger of the Oil Injector to allow approximately 1/16" of oil to escape. Rotating the fan will relieve air pressure and allow oil to flow into the oil chamber.

1.6 ANNUALLY

1. Visually check the Surge Suppressors for any trace of overloads.

2. General visual inspection of all components and wire for overloads, overheating, or any other general damage.

SECTION 2

TROUBLESHOOTING

2.1 PRECAUTIONS

1. Do not use a battery-buzzer for continuity checking. The buzzer current exceeds the maximum current rating for diodes and transistors in the system.

2. Do not use the first two low scales (X1 or X10) on the Triplett ohmmeter for continuity checking. For these scales, the meter current exceeds the maximum current rating for diodes and transistors in the system.

3. Do not remove packages or diode sticks when Power is UP.

4. Care must be taken when using Scope or Jumper Clip Leads to prevent touching adjacent pins. Use Minigator Clips with insulators or the Wire Wrap Pin Probe Tip (Part No. 1183854?).

5. Use extreme caution when working on the plug-in side of the panels. Avoid hitting packages when moving the scope.

6. Do not attempt to force a TRUE level with -12V. In all cases, the desired effect can be obtained either by the use of a ground clip, or by taping off one or more diodes.

7. A ground jumper may be used to force a FALSE level.

NOTE

Connect clip to the point to be grounded prior to making ground connection.

8. Do not pull Cable Plugs with POWER ON at either end of the cable.

9. Only soldering irons that have an isolation transformer may be used.

10. Scope ground - to prevent ground loops and noise interference use only the ground clip on the scope probe. Attach it to a suitable ground as near as possible to the point being observed.

2.2 AC CIRCUITS

The convenience outlets, the -24V and the 120V Supplies, are controlled by the primary wall breaker.

The AC Input to the DC Power Supplies is controlled by K11 and K12 contactors.

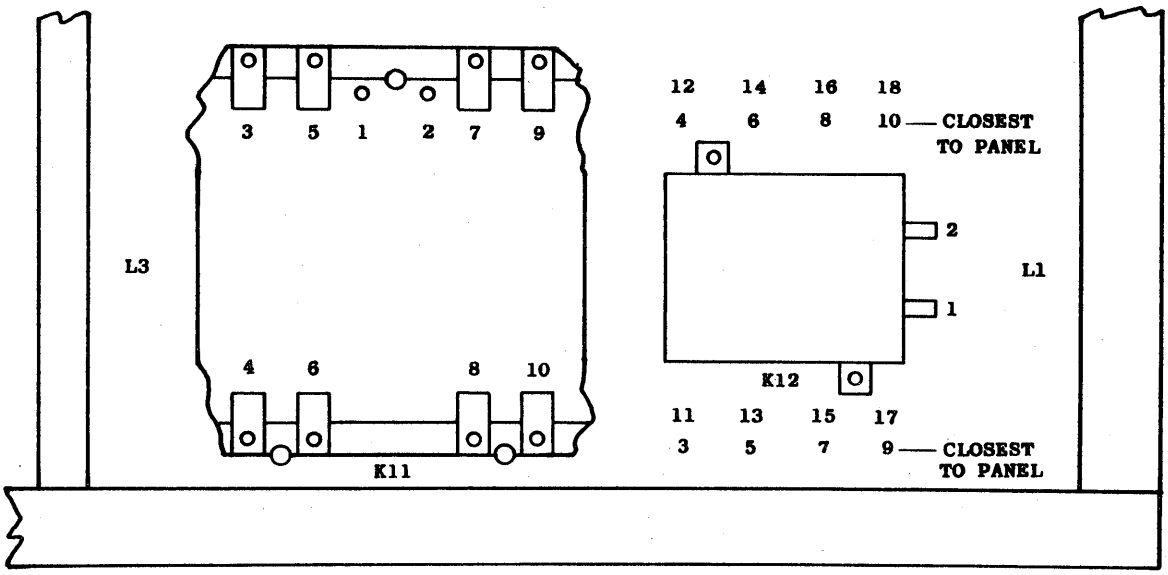


FIGURE 2.2-1. AC CONTROL CONTACTORS

2.3 DC POWER SUPPLIES

The DC Power Supplies are all of the constant voltage type. The transformers have associated tuning capacitors. See Section 4 for the physical layout of Power Supply components.

The SP (Surge Suppressors) in the secondary are selenium type rectifiers. These are active for high surge currents and can possibly short. They are used to protect the diode rectifiers.

There are two supplies whose outputs are controlled by electronic switches. They are the +20V and +100V supplies.

When troubleshooting these voltages, the Power Supply monitoring system will show that the voltages are present even though they are not being delivered to the system.

If the +20V electronic switch is open, the power regulators of the system will not operate. If it is shorted, the DC LOCKOUT switch on the Display and Distribution Panel will not turn the power regulators off.

If the +100V electronic switch circuit is open, the undervoltage sensing will indicate +100V undervoltage. If it is shorted, the system Flip-flops will be in random on-off conditions when power is applied. If the +100V switch is working properly, they should come on cleared.

2.4 VOLTAGE REGULATORS

The -12V regulator controls the -4.5V and -1.2V regulators. The -4.5V and -1.2V regulators cannot operate until -12V is present.

It is possible for the -12V regulator to operate with one or more of the output transistors open, depending on load requirement. Each heatsink assembly contains three (3) power transistors with common collector and base connections. See Figure 2.4-1.

If an output transistor opens, it can be located by checking the voltage drop across the 0.2 ohm emitter resistor while the regulator is operating.

The regulator will not shut down due to an open output transistor unless the current load becomes too high for the remaining transistors. When this occurs, one of the remaining transistors will short, and an overvoltage condition will be displayed by the voltage sensing panel.

If an output transistor shorts, the output of the regulator will go from -12V to -19V. A -12 overvoltage will be indicated, and the power supply will shut down. The voltage sensing panel will also indicate in which cabinet the failure occurred. With power off, disable the voltage sensing for the cabinet indicated on the voltage sensing panel.

Refer to Table 3.1-1 for the Inhibit points. Disconnect the emitter terminals of one heatsink. Refer to Figures 2.4-1 and 2.4-2.

Apply power and monitor the output of the -12V regulator if it is still at -19V. Shut power down and reconnect the emitter terminals. Continue this procedure until the shorted heatsink assembly is located. When the proper heatsink assembly is located, the output of the regulator should read -12V. Remove the heatsink and locate the shorted transistor. Another cause of -12V overvoltage is the loss of one of the control voltages on the regulator. These are the -33V and +50V. Do not leave the -19V from the regulator on the system for longer than necessary.

If a failure occurs in the -4.5V regulator or the -1.2V regulator, the same procedure can be used as described for the -12V regulator.

NOTE

If the -12V regulator fails in Central Control (no output), there will be no voltage sensing available. The voltage sensing circuits are supplied operating voltages from Central Control. Power could be applied and the system would look normal, except there would be no +100V for Flip-flop clear.

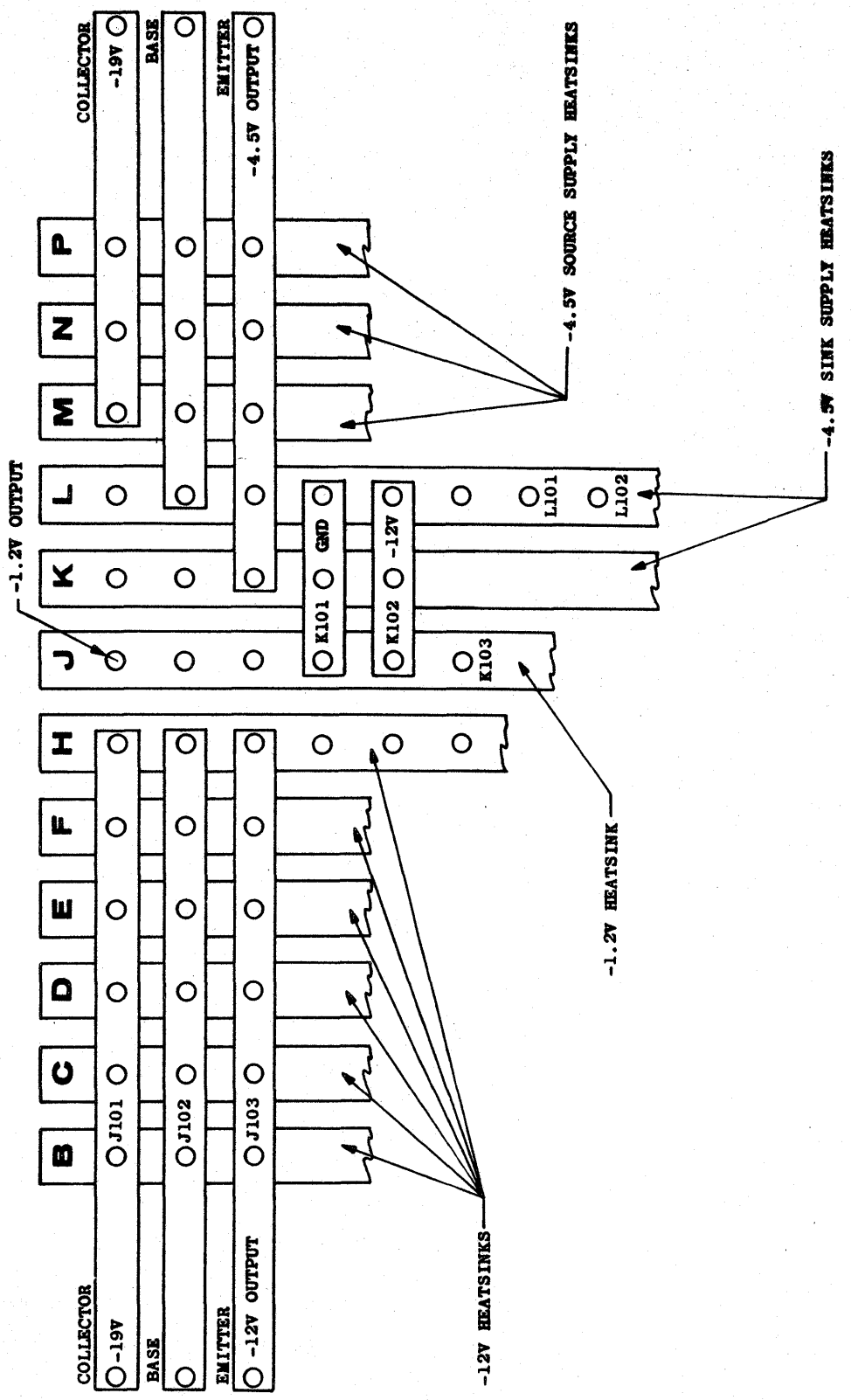


FIGURE 2.4-1 HEATSINK CONNECTION

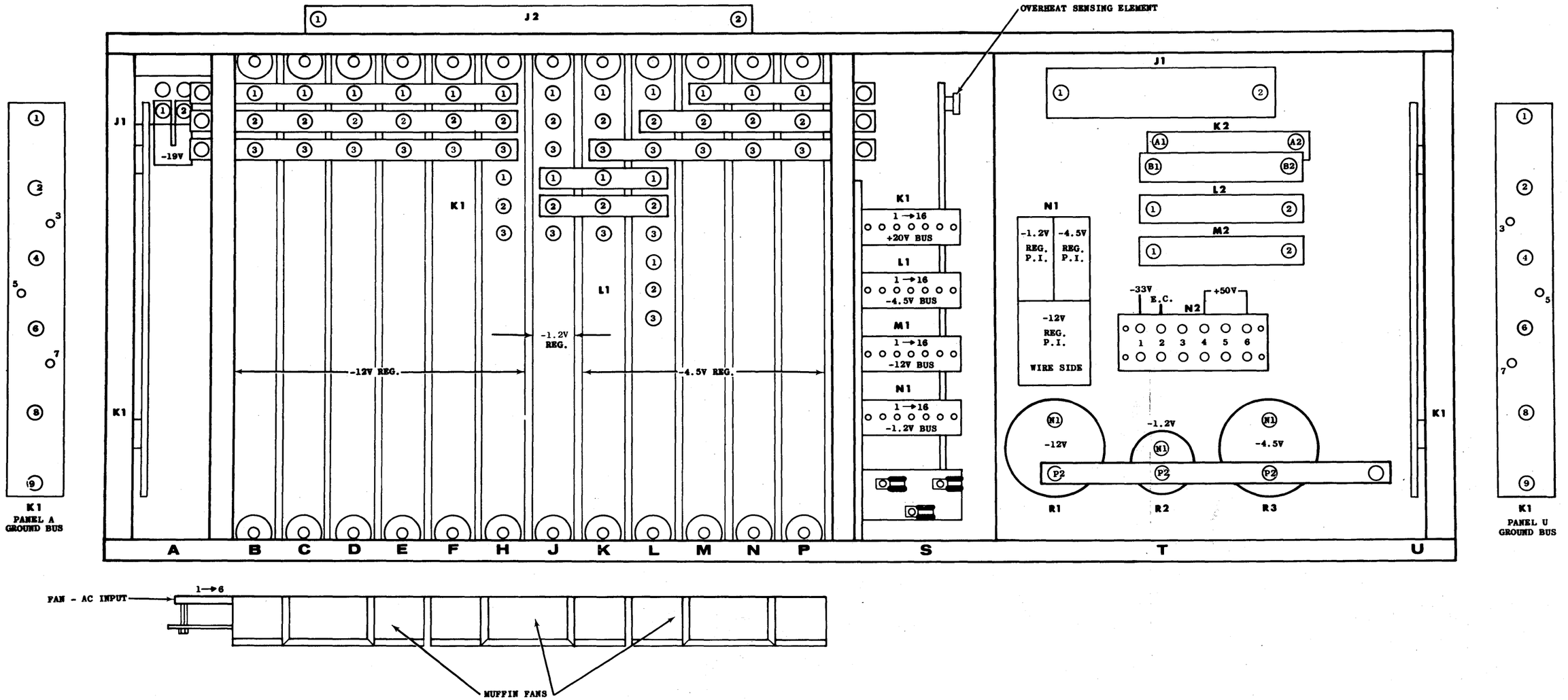


FIGURE 2.4-2. VOLTAGE REGULATOR LOCATOR

2.5 VOLTAGE SENSING

The Voltage Sensing circuits can be checked by comparing the operation of one to another. If the voltage regulator outputs are at the proper value and a fail condition is still displayed, disable sensing for that unit. Refer to Table 3.1-1.

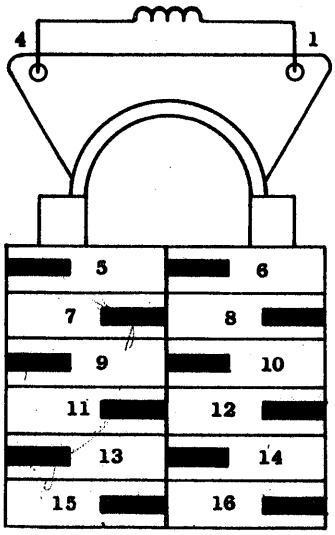
After sensing is disabled, apply power and compare the failing circuit to an operating one. See Figure 2.5-1 for Sensing Package Layout.

	PANEL – F										PANEL – E																					
	4		3		2		1		0		9		8		7		6		5		4		3		2		1		0			
A											SW-L 1. PA FAIL 2. PB FAIL 3. CC FAIL 4. I/O FAIL 5. O.H. POWER SUPPLY		VSC -4.5 CC		VSC -4.5 PB		VSC -4.5 PA		VSC -1.2 CC		VSC -1.2 PA				C50 FROM AH-S1 ON CC DISPLAY PANEL CABLE NO. 64			C50 POWER FROM CC REGULATOR CABLE NO. 140	C50 PA SENSE & POWER CABLE NO. 62
											SW-L 1. CM-1 FAIL 2. CM-2 FAIL 3. O.H. FAIL 4. EC CM-1 5. EC CM-2		VSC -4.5 CM-2		VSC -4.5 CM-1		VSC -4.5 I/O		VSC -1.2 I/O		VSC -1.2 PB				C50 I/O 2 SENSE & POWER CABLE NO. 65-2				C50 I/O 1 SENSE & POWER CABLE NO. 65-1
				CONNECTORS TO INDICATORS & CLEAR BUTTON	KPK CM-1 CM-2 POWER OVERHEAT	KPK PA PB CC I/O	SW-L 1. CM-1 RELAY 2. CM-2 RELAY 3. O.H. RELAY 4. POWER RELAY	SW-L 1. I/O RELAY 2. PA RELAY 3. PB RELAY 4. CC RELAY			SW-L 1. INH. LEVEL 2. EC I/O 3. EC CC 4. EC PB 5. EC PA		VSC -12 CC		VSC -12 PB		VSC -12 PA		VSC -1.2 CM-1		VSC +20	VRP			C50 I/O 4 SENSE & POWER CABLE NO. 65-4				C50 I/O 3 SENSE & POWER CABLE NO. 65-3
B					KPK -12 -1.2 -4.5 +100	KPK EC UV OV +20	SW-L 1. +20 RELAY 2. -12 RELAY 3. -1.2 RELAY 4. 4.5 RELAY 5. +100 RELAY		SW-L 1. EC RELAY 2. OV RELAY 3. UV RELAY		SW-L 1. +20V OV/UV 2. -12 FAIL 3. -1.2 FAIL 4. -4.5 FAIL 5. +100V OV/UV		VSC -12 CM-2		VSC -12 CM-1		VSC -12 I/O		VSC -1.2 CM-2		VSC +100	VRP			C50 SPECIAL D/D VOLTAGES NOT SENSING LEVELS CABLE NO. 66				C50 PB SENSE & POWER CABLE NO. 63

FIGURE 2.5-1. SENSING PACKAGE LAYOUT (PACKAGE SIDE)

2.6 POWER CONTROL RELAYS

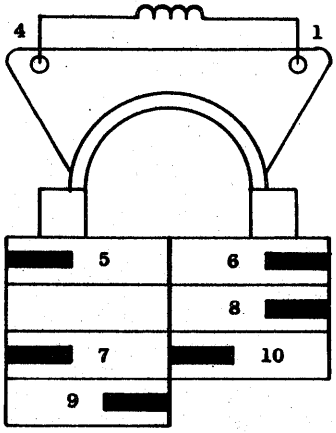
The Power Control Panel Relays are shown in the following figures.



COIL CHARACTERISTICS

COIL RESISTANCE: 300 OHMS ± 10 PERCENT @ 25° C.
OPERATING CURRENT: .080 AMPS NOMINAL.
OPERATING VOLTAGE: 12V DC.

FIGURE 2.6-1. K13, 18, 19 (S-52066-21)



COIL CHARACTERISTICS

COIL RESISTANCE: 500 OHMS ± 10 PERCENT @ 25° C.
OPERATING CURRENT: .048 AMPS NOMINAL.
OPERATING VOLTAGE: 24V DC.

FIGURE 2.6-2. K14 and K15 (S-11895380)

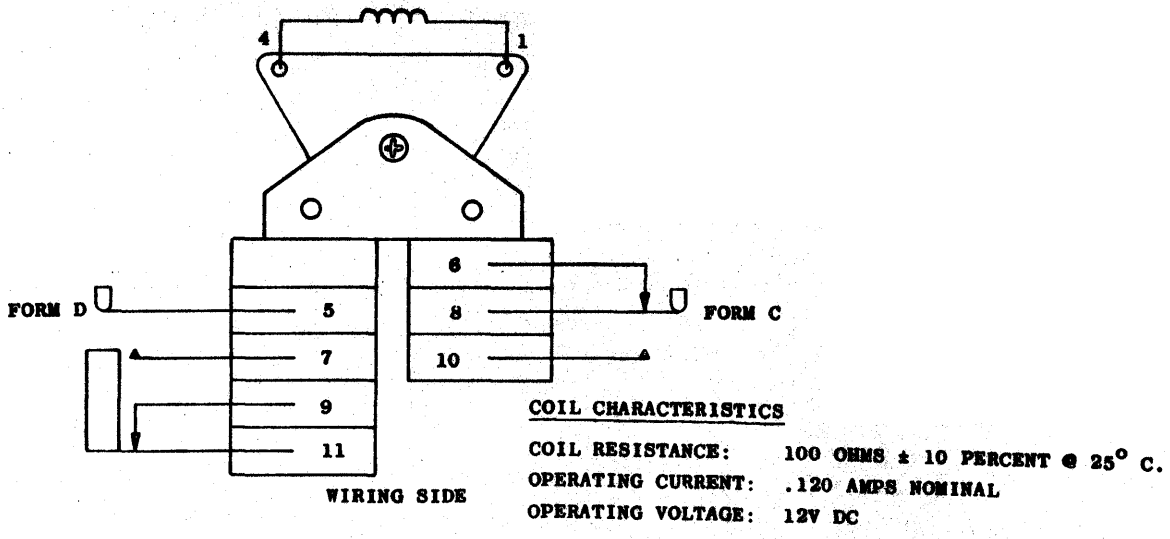


FIGURE 2.6-3. K17 (S11895398)

The Power ON-OFF sequencing is controlled by relays located in the D and D cabinet. Refer to Figure 2.6-4 for component layout.

POWER ON CYCLE

Refer to Figure 2.6-5 for Power Control Schematic.

1. Pushing the ON button will pick K13 (DHJ1), which will then latch in.
   a. The -24VA-R line should go from open to -24V.
2. K18 (DHR1) should pick approximately 400 ms later than K13 (DHJ1).
   a. PGDL' should go from -0.3V to -12V.
   b. DC Lockout to core memory should go from ground to -24V.
3. K19 (DHM1) should drop out.
   a. +20V control line should go to -1.5V.
   b. Inhibit-B line should remain true for approximately 20 ms.
   c. The Power Interlock line will go to -12V if K17 (DHP1) is picked.
4. K14 (DHK1) is also picked by pushing the ON button. It should drop out approximately 150 ms after release of the ON button.

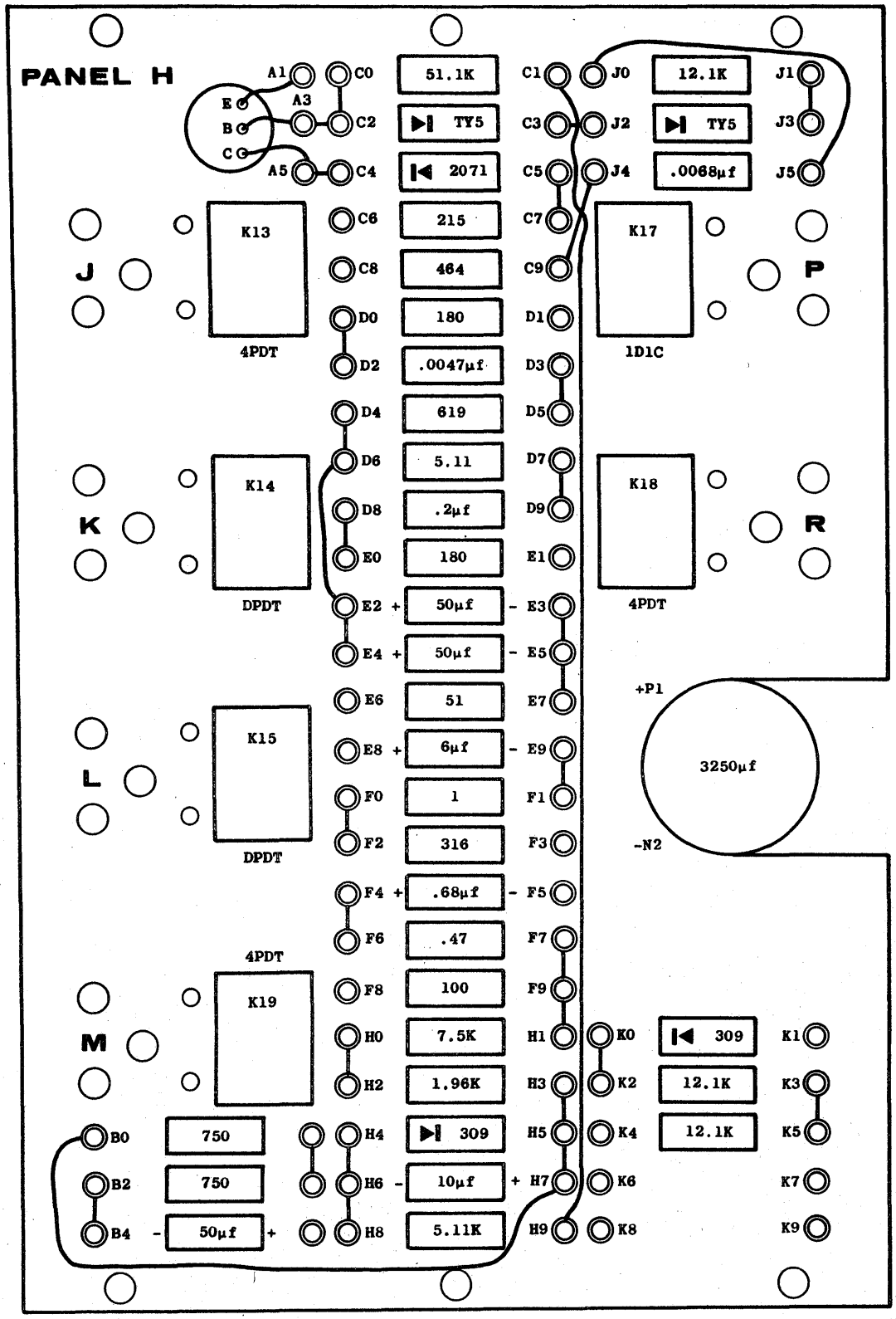


FIGURE 2.6-4. RELAY PANEL D & D

a. While K14 (DHK1) is picked, the peripheral unit ON bus should have -24V on it.

5. Applying -12V to K17 (DHP1) will cause it to pick.

   a. The Power Interlock line should go from ground to the same level as the +20V control line. (Ground, if K19 (DHM1) is picked; -12V if K19 (DHM1) is dropped out).

   b. The -24V-B line should go from open to -24V.

POWER OFF CYCLE

Refer to Figure 2.6-5 for Power Control Schematic.

1. Pushing the OFF button will cause K13 (DHJ1) to drop out.

   a. The -24VA-R line will go from -24V to open.

2. K18 (DHR1) will drop out.

   a. PGDL' will go from -12V to -0.3V.

   b. DC Lockout to core memories will go to ground.

3. K19 (DHM1) will pick approximately 35 ms after DC Lockout becomes grounded.

   a. Inhibit-B will go to approximately -5V.

   b. The +20V control line will go to ground.

   c. The Power Interlock line will go to ground if K17 (DHP1) is picked.

4. K14 (DHK1) and K15 (DHL1) should both pick and remain picked for approximately 150 ms after the OFF button is released.

   a. The peripheral unit OFF bus should go from open to -24V and remain as long as K14 (DHK1) is picked.

5. Removing the -12V from K17 (DHP1) causes it to drop out.

   a. The Power Interlock level becomes grounded.

6. K20 (DCK2) Neon Power Interlock. This relay is controlled by the neon interlock switch located on the D & D cabinet.

NOTE

When measuring the -20V, special attention should be given the reading because -100V is also present thru the neon drivers. It may appear that -120V is present when it is not.

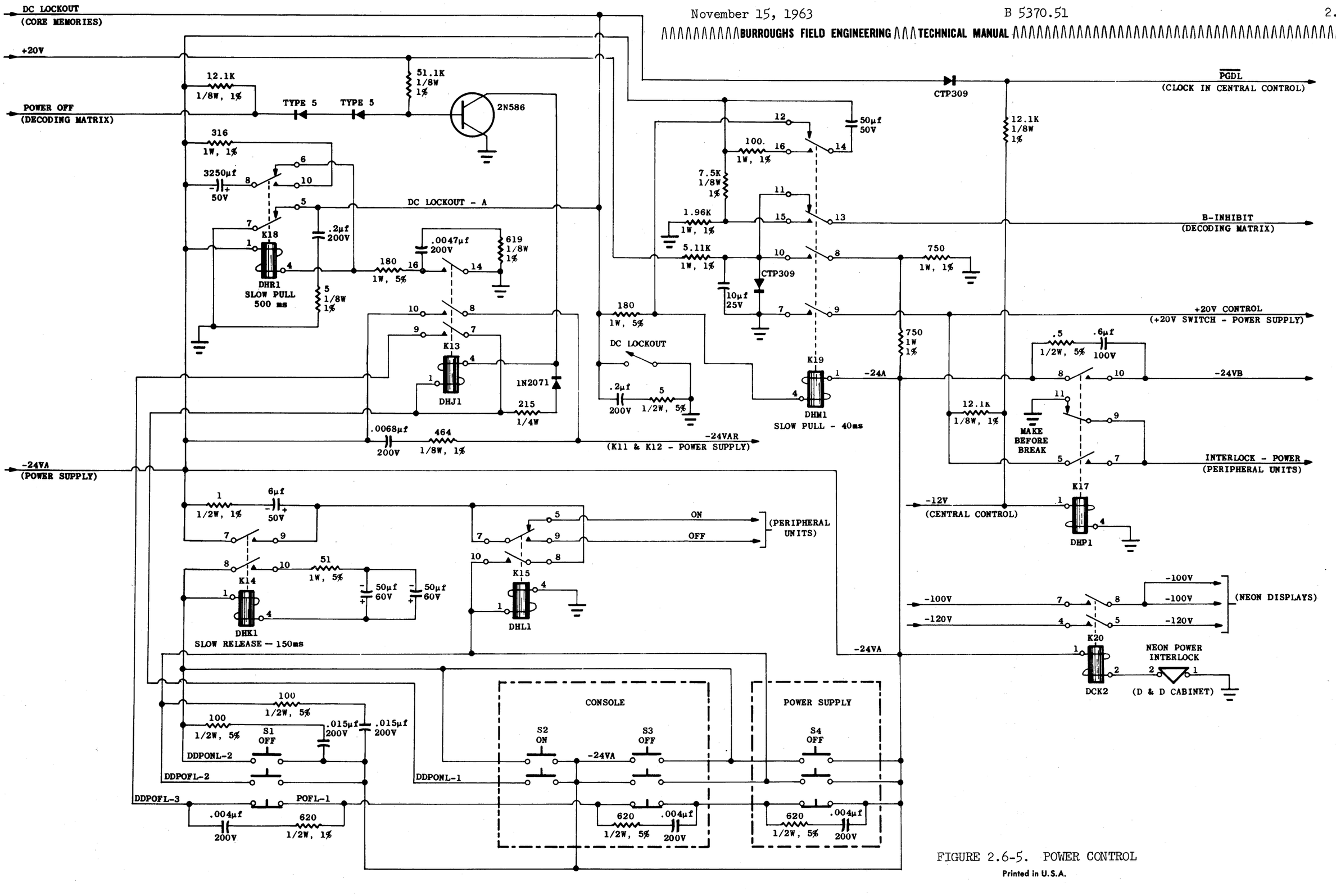


FIGURE 2.6-5. POWER CONTROL

2.7 RIN INDEX

RIN INDEX FOR THE B 5370 POWER SUPPLY AND REGULATORS (11831450)

RIN NO.	INSTAL. TIME IN HOURS	PRE-REQUISITE	UNITS EFFECTED	DESCRIPTION
5002	1.0		102 ⇒ 143	Improve reliability of the +20V switch.
5007	0.5		102 ⇒ 143	Replacement of the AC input box cover.
5008	1.0		102 ⇒ 143	Replacement of the K12 relay to improve reliability.
5011	1.0		102 ⇒ 143	Addition of a resistor to reduce transient surge current in the -24V supply.
5024	1.0		102 ⇒ 143	Replace end panel washers with the proper size.
5034	2.0		102 ⇒ 143	Improve heat dissipation of the 30 watt resistors by removing insulation from leads.
5035	1.0		102 ⇒ 143	Installation of spacers to high wattage resistors mounts, in order to provide better air circulation.

SECTION 3

ADJUSTMENTS

3.1 VOLTAGE REGULATOR

The Voltage Regulators are adjustable in each cabinet.

PROCEDURE

To make adjustments on the voltage regulator, perform the following steps:

1. Connect a precision voltmeter to terminal CSM1 of the voltage regulator. Check for -12V.
2. Adjust R36 on the -12V regulator parallel plate package until the output is -12V.
3. Connect the precision voltmeter to terminal CSL1 of the voltage regulator. Check for -4.5V.
4. Adjust R27 on the -4.5V regulator parallel plate package until the output is -4.5V.
5. Connect the precision voltmeter to terminal CSN1 of the voltage regulator. Check for -1.2V.
6. Adjust R27 on the -1.2V regulator parallel plate package until the output is -1.2V.

-12V EXCESS CURRENT ADJUSTMENT

The overcurrent potentiometer should be adjusted so that the sensing threshold is 10 to 15 percent above the desired operating range of the regulator.

In order to determine the threshold setting for the overcurrent potentiometer, it is desirable to inhibit the power failure sensing so that the indicator lights will come on without power going down. This can be done by grounding the test inhibit line for the cabinet of interest. Refer to Table 3.1-1. This line is located on the Power Sensing Panel in the D and D cabinet.

With the potentiometer R35 all the way clockwise, begin turning it counterclockwise until the AMP light comes on. The threshold setting will then be equal to the -12V load current at the time of setting.

To achieve the 10 to 15 percent margin for operation, set the threshold at nominal load and then back potentiometer R35 off (clockwise) by the proper amount. Potentiometer R35 is designed so that the threshold changes approximately 5 amps per turn.

TABLE 3.1-1. TEST INHIBIT

UNIT	TEST INHIBIT PIN (D & D)
PA	AFAO U5
PB	AFAO T4
CC	AFAO V4
I/O	AFAO T3
CM-1	AFAO V3
CM-2	AFAO T2

In order to lower the range of potentiometer R35 and increase its sensitivity at low normal loads, it is recommended that one of the two parallel .02 ohm resistors in the output of the -12V regulator be disconnected. This may be done for nominal load less than 40 amps. The sensitivity of potentiometer R35 is then increased to about 2.5 amps per turn and the minimum threshold lowered to about 15 amps.

3.2 CALIBRATION PROCEDURE FOR METER CHECK CIRCUIT

1. Remove hole plug located below test points on the meter panel.
2. Pre-set R1 and R2 fully counterclockwise.
3. Rotate meter selector switch to "Meter Check" position.
4. Apply POWER to the system.
5. Adjust R1 clockwise for 5.0 ± .05 volts at TP1 (1) to common TP2 (-).
6. Adjust R2 clockwise for 50.0 ± .5 millivolts at TP3 (+) to common TP2 (-).
7. Recheck voltage at TP1. If it is not 5.0 ± .05 volts, repeat steps 5, 6, 7 and 8. If the voltage is correct, calibration is complete and both the Ammeter and Voltmeter should indicate full scale deflection. Accuracy of both meters should be 2 percent or better.
8. Insert hole plugs.

SECTION 4

ASSEMBLY AND DISASSEMBLY

4.1 POWER SUPPLY

INTRODUCTION

This section of the manual contains illustrations of each DC Power Supply by panel.

Layouts of the Heatsink Assemblies used within the Power Supply are also illustrated.

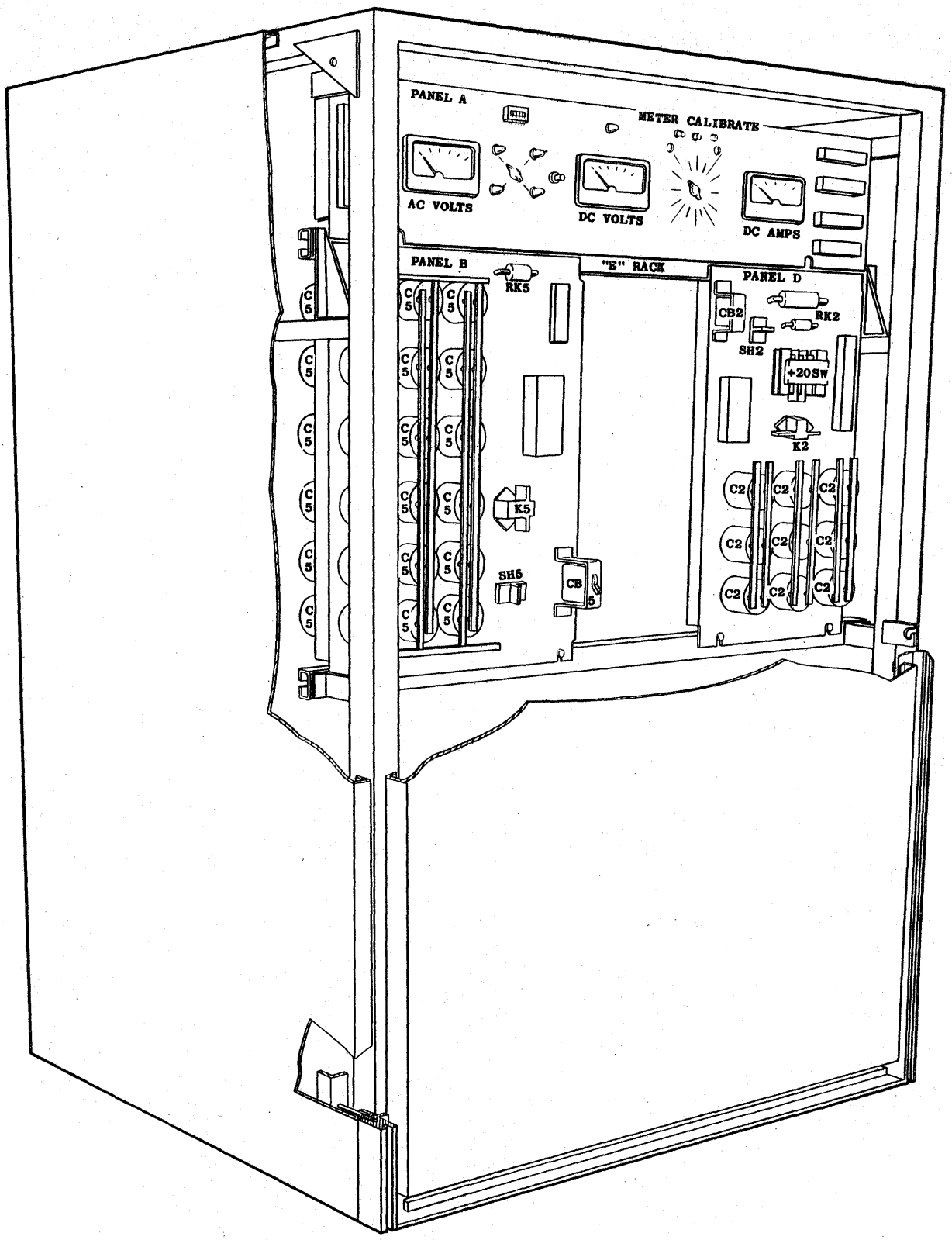


FIGURE 4.1-1. POWER SUPPLY (FRONT VIEW)

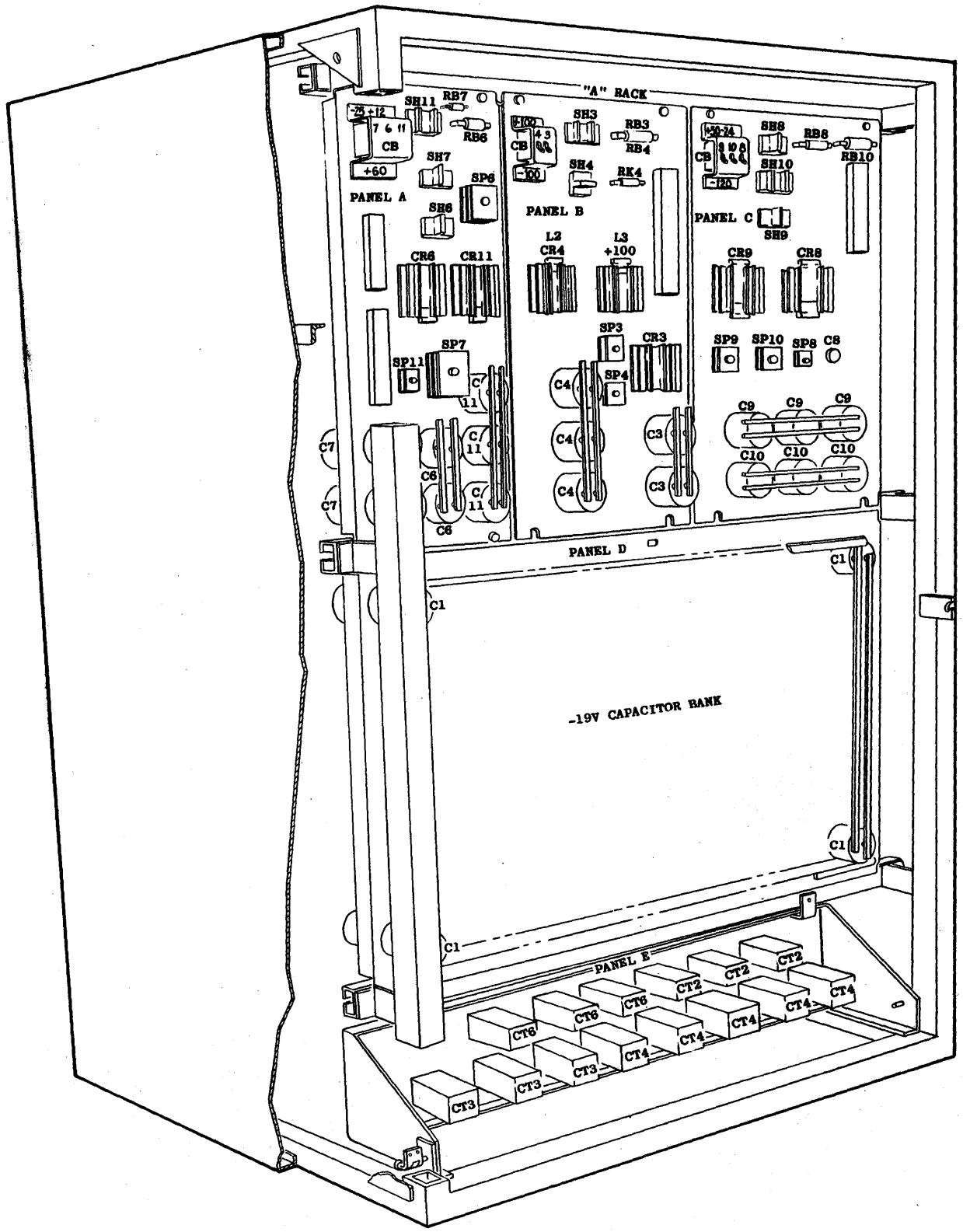


FIGURE 4.1-2. POWER SUPPLY (REAR VIEW)

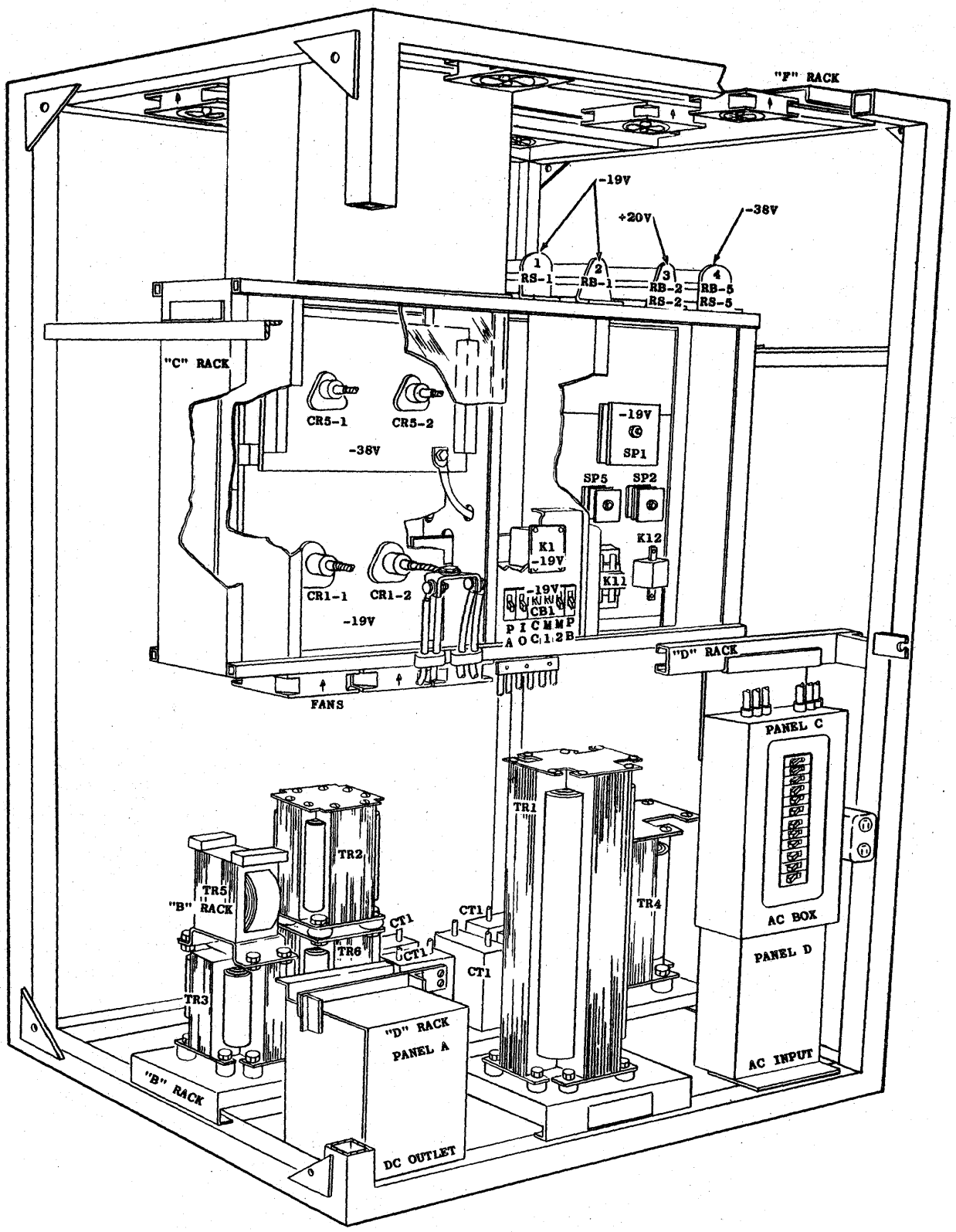


FIGURE 4.1-3. POWER SUPPLY (INTERIOR)

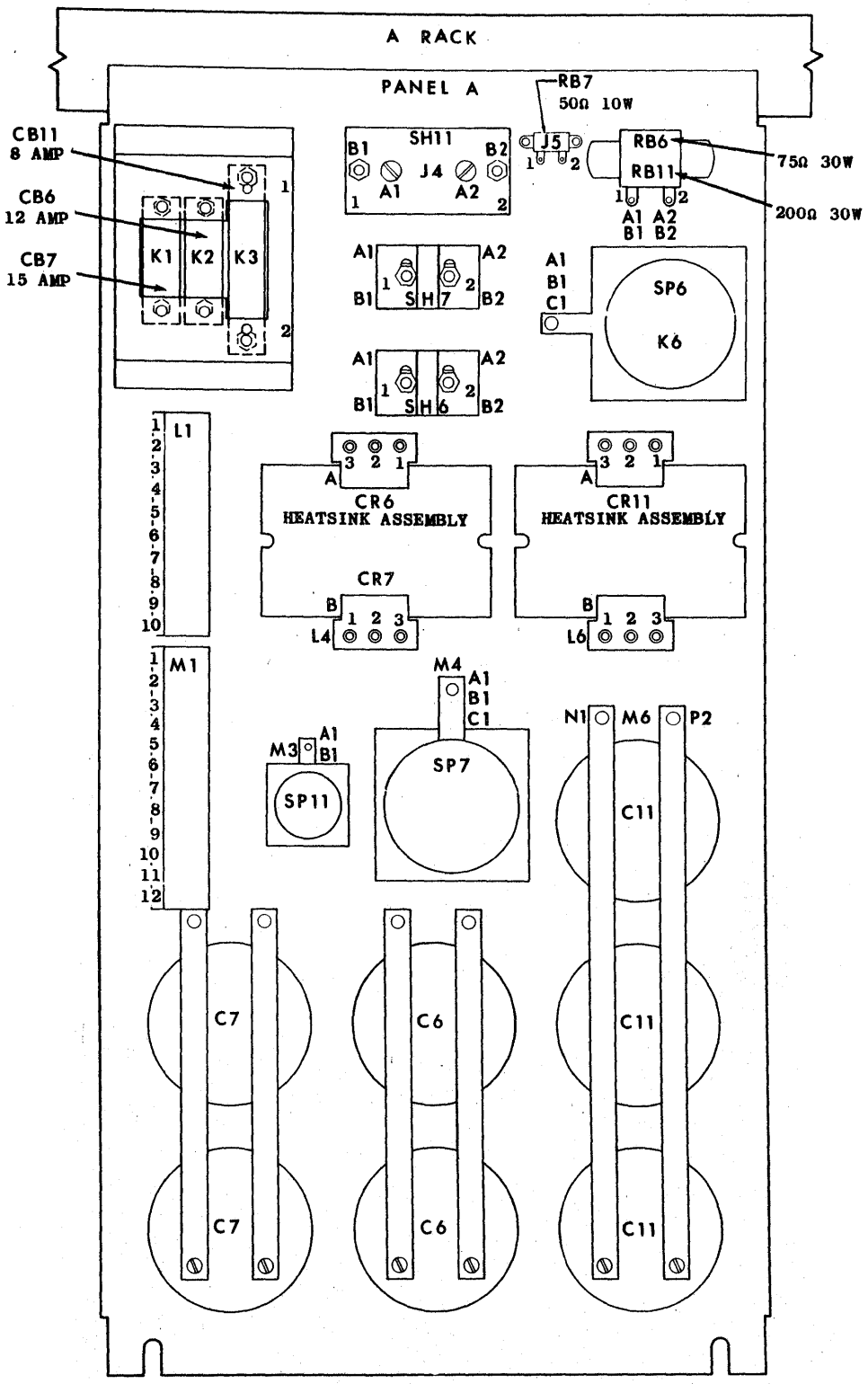


FIGURE 4.1-4 PANEL LAYOUT (-33V, +19V, +74V)

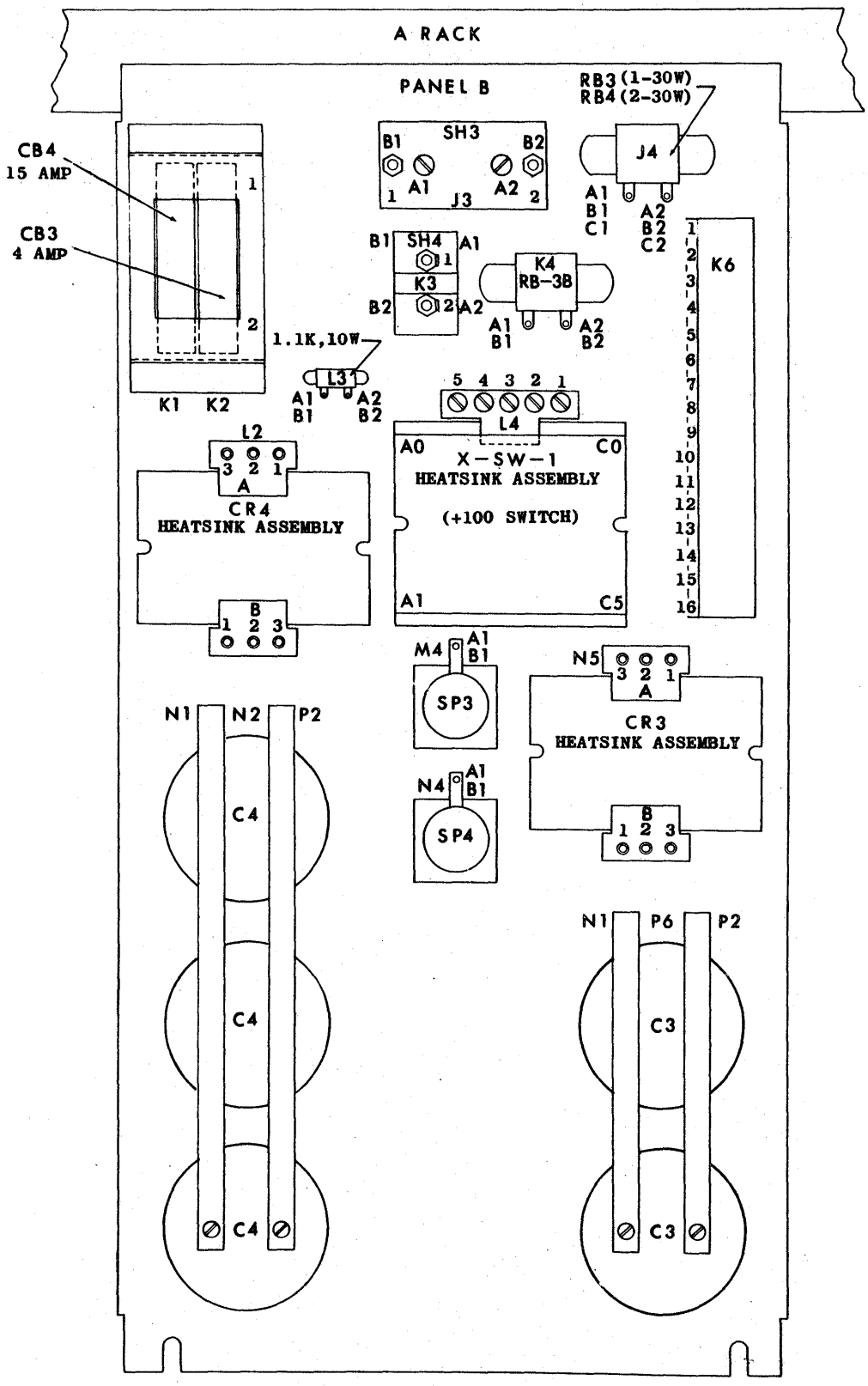


FIGURE 4.1-5. PANEL LAYOUT (+100V, -100V)

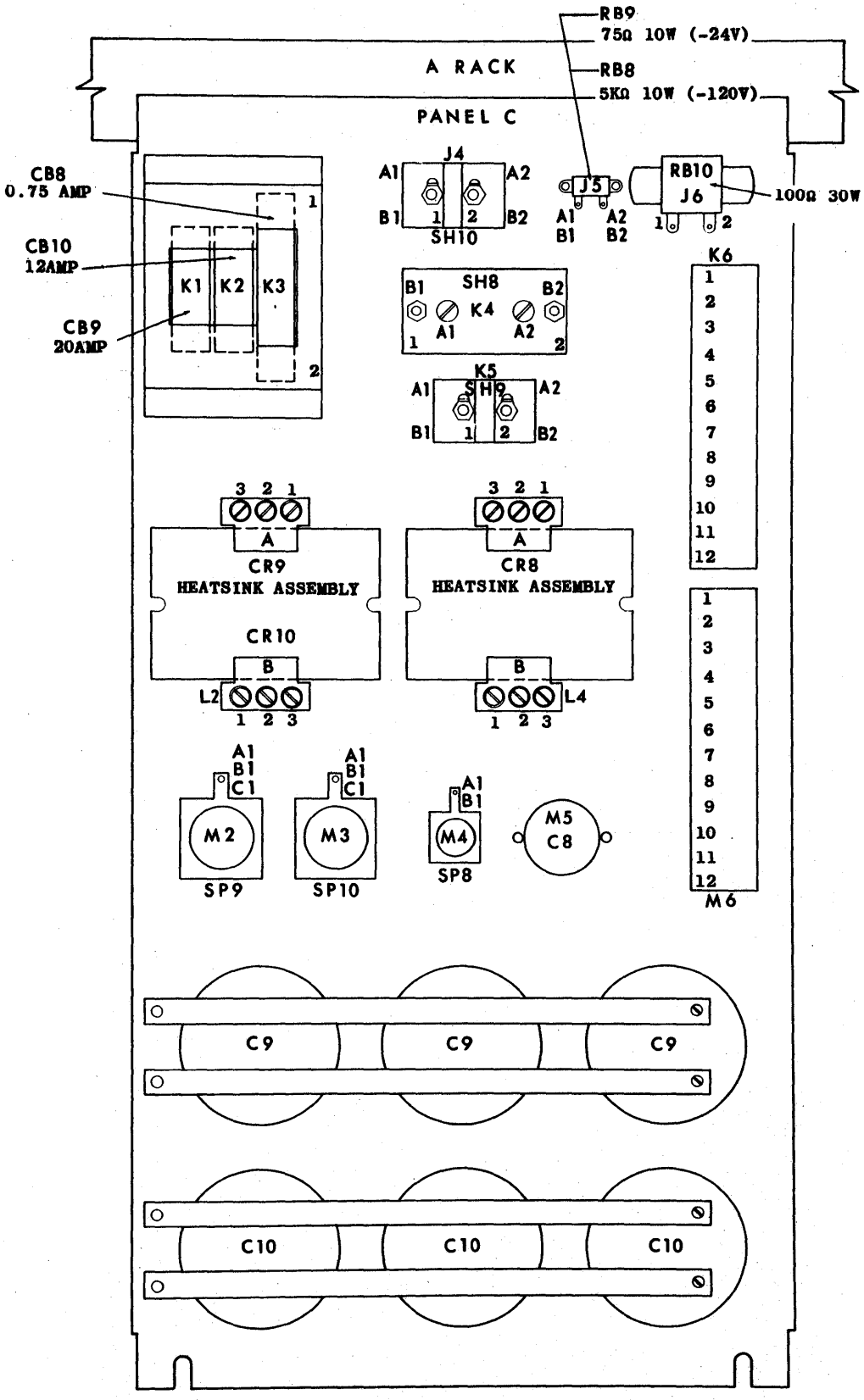


FIGURE 4.1-6. PANEL LAYOUT (+50V, -24V, -120V)

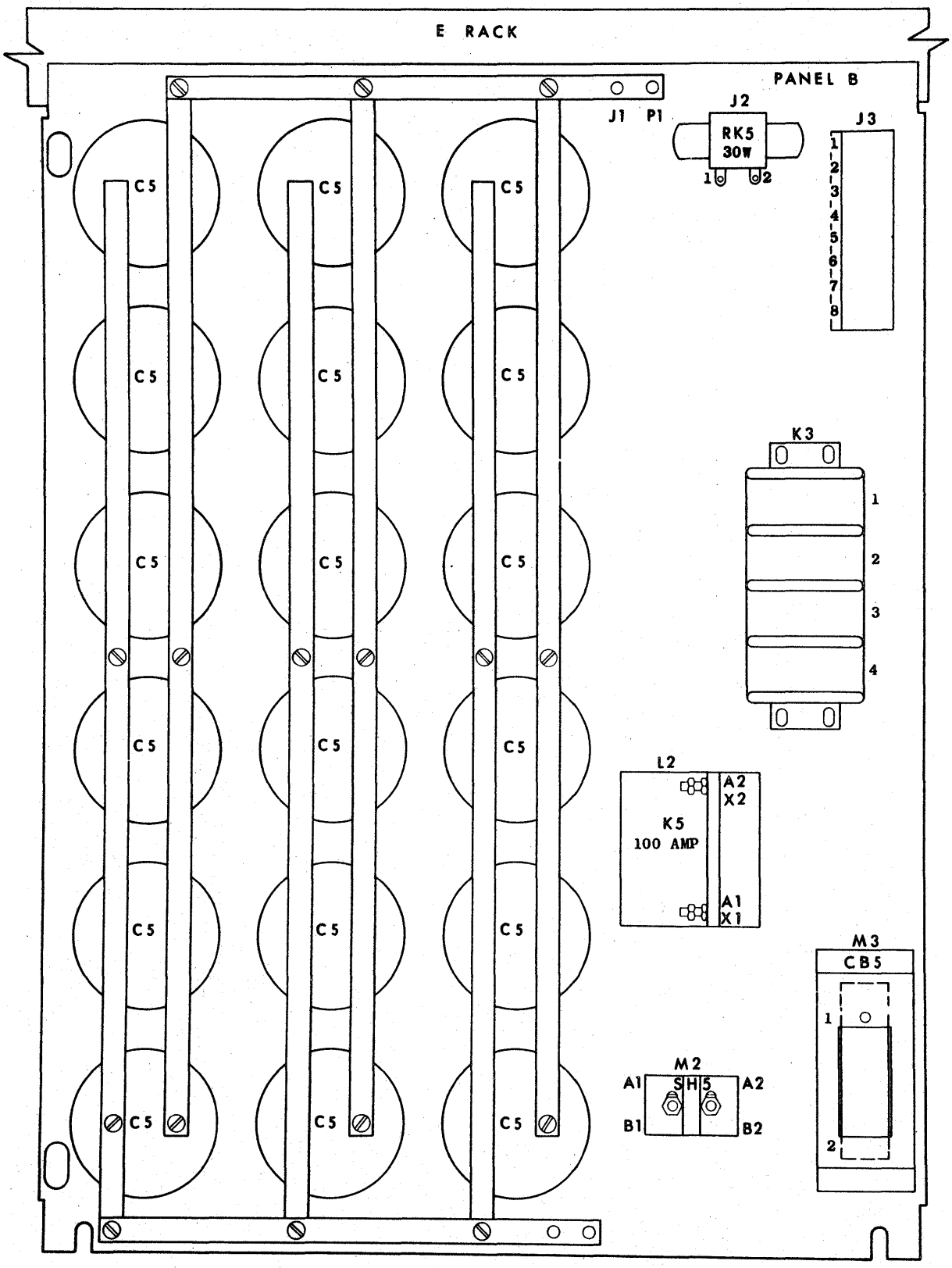


FIGURE 4.1-7. PANEL LAYOUT (-38V)

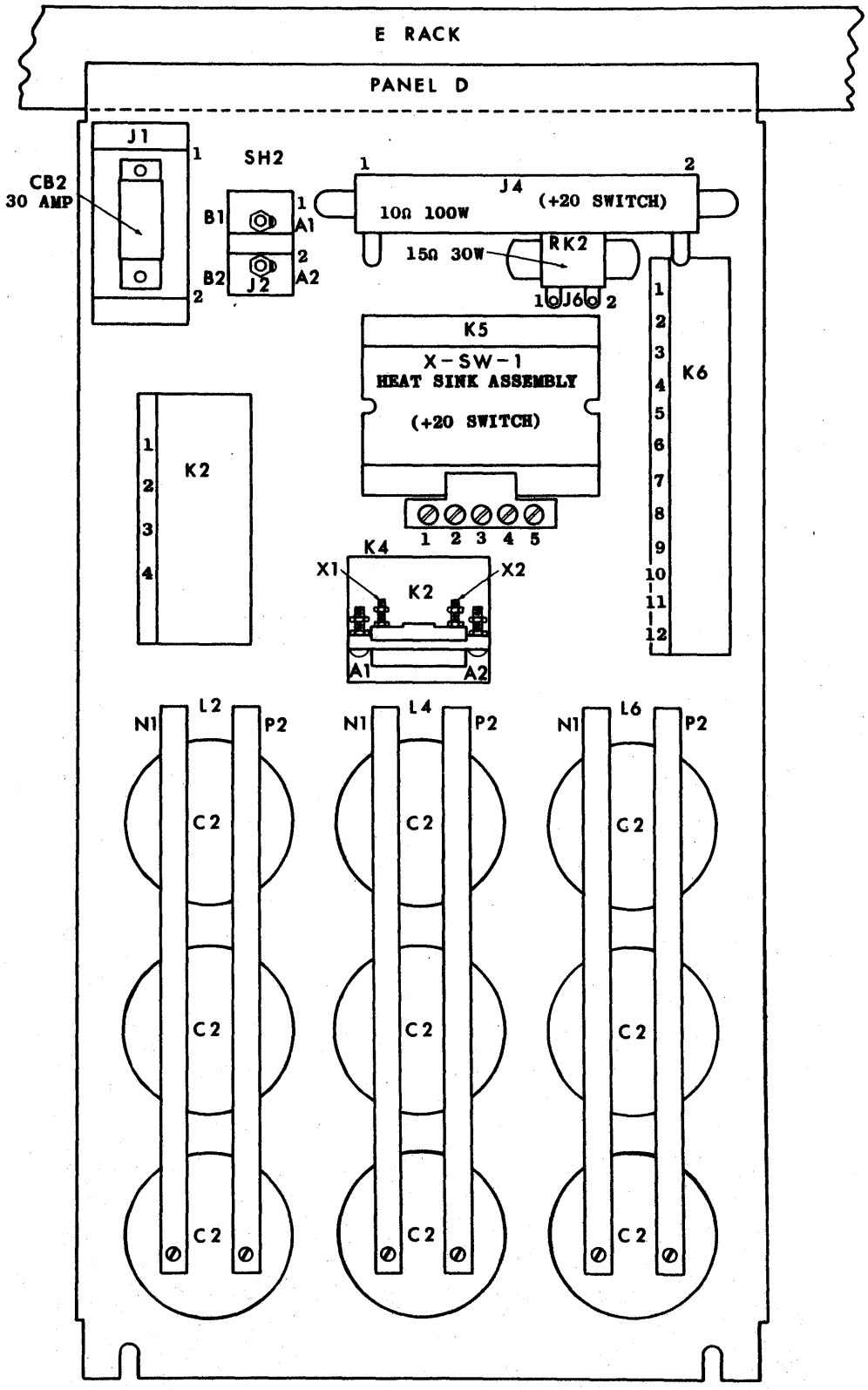


FIGURE 4.1-8. PANEL LAYOUT (+20V)

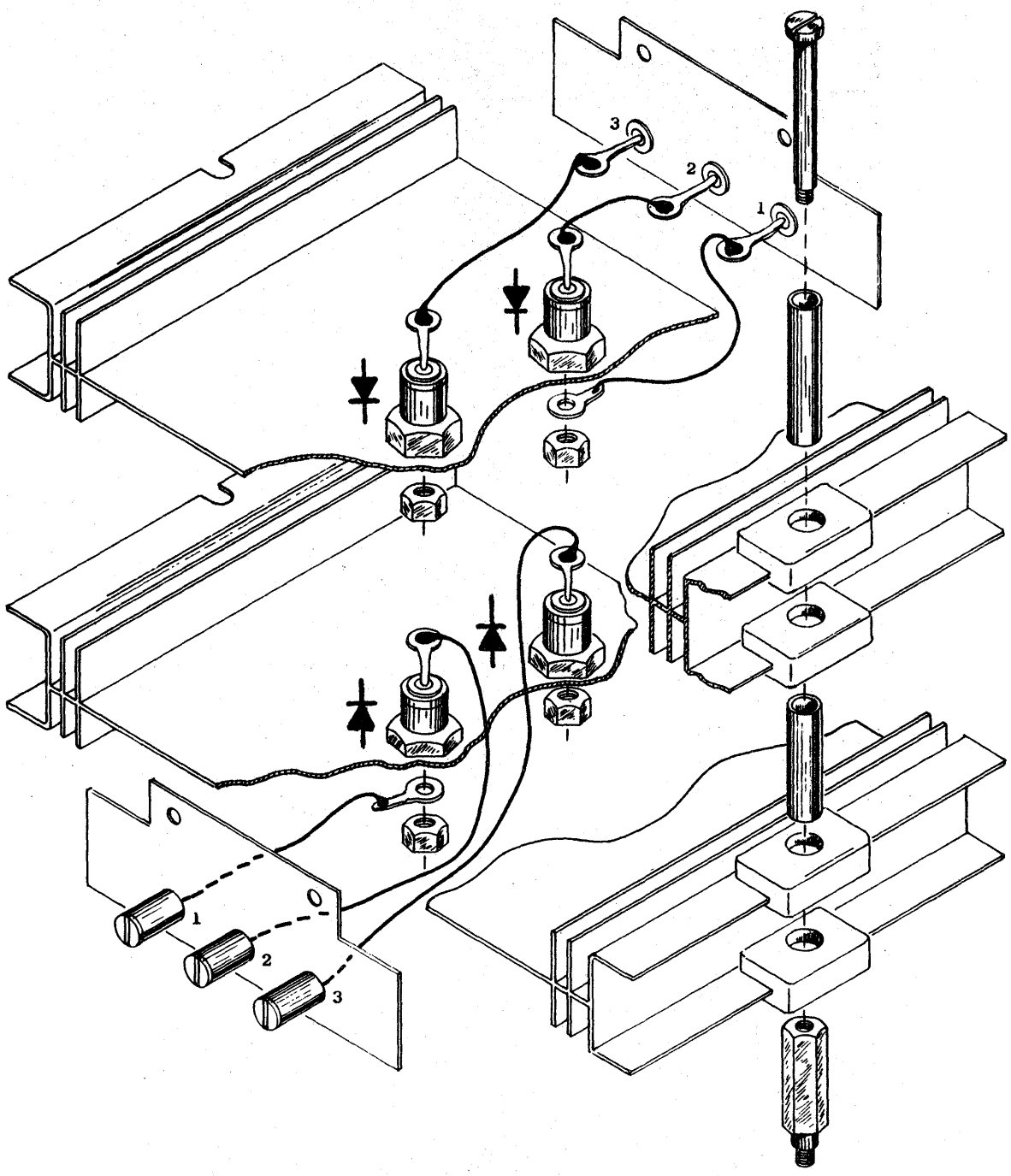


FIGURE 4.1-9. COMMON HEATSINK ASSEMBLY

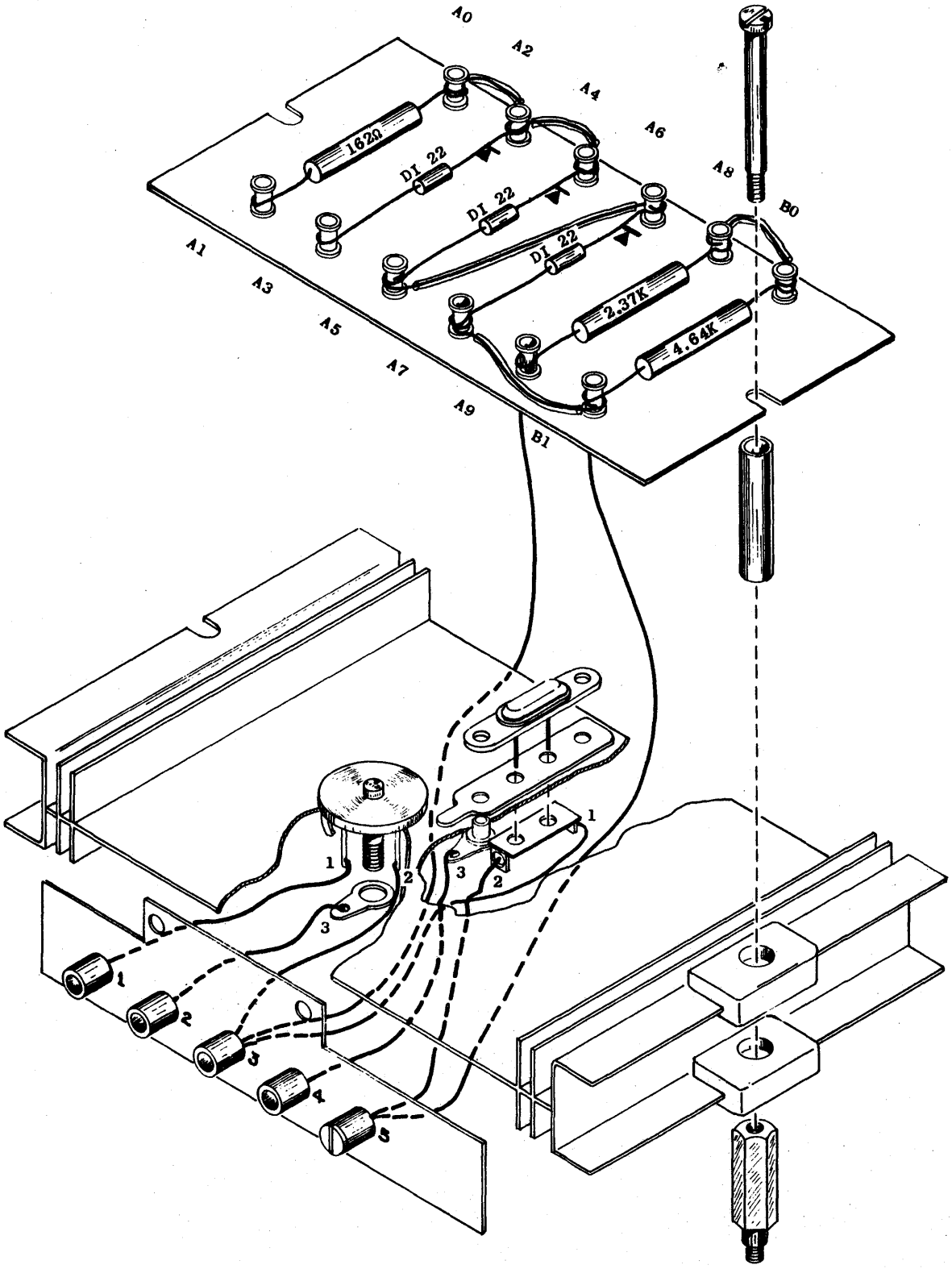


FIGURE 4.1-10. +20 ELECTRIC SWITCH

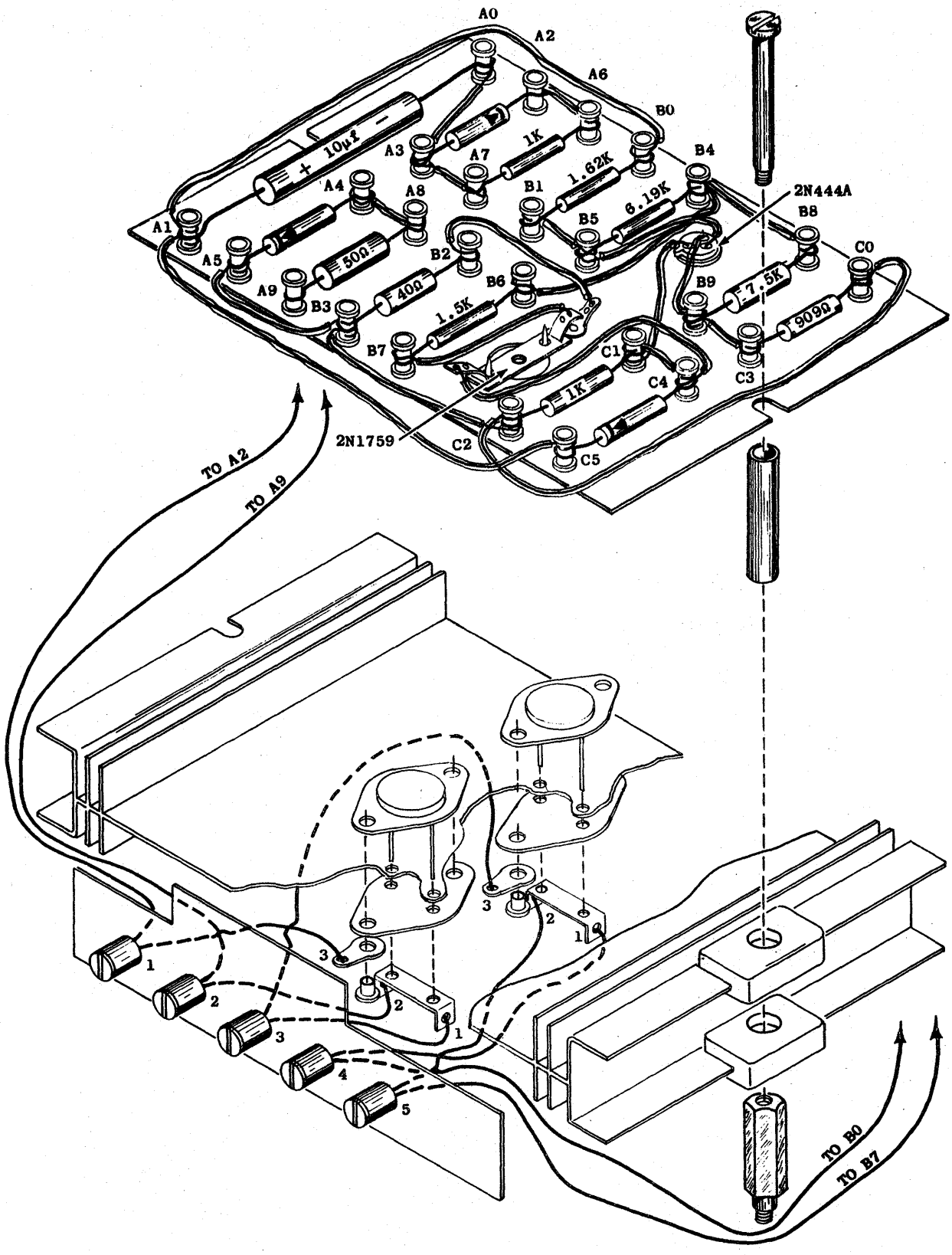


FIGURE 4.1-11. +100 ELECTRIC SWITCH

4.2 VOLTAGE REGULATORS

INTRODUCTION

The Power Regulator Unit Heatsink Assemblies are illustrated in this section of the manual.

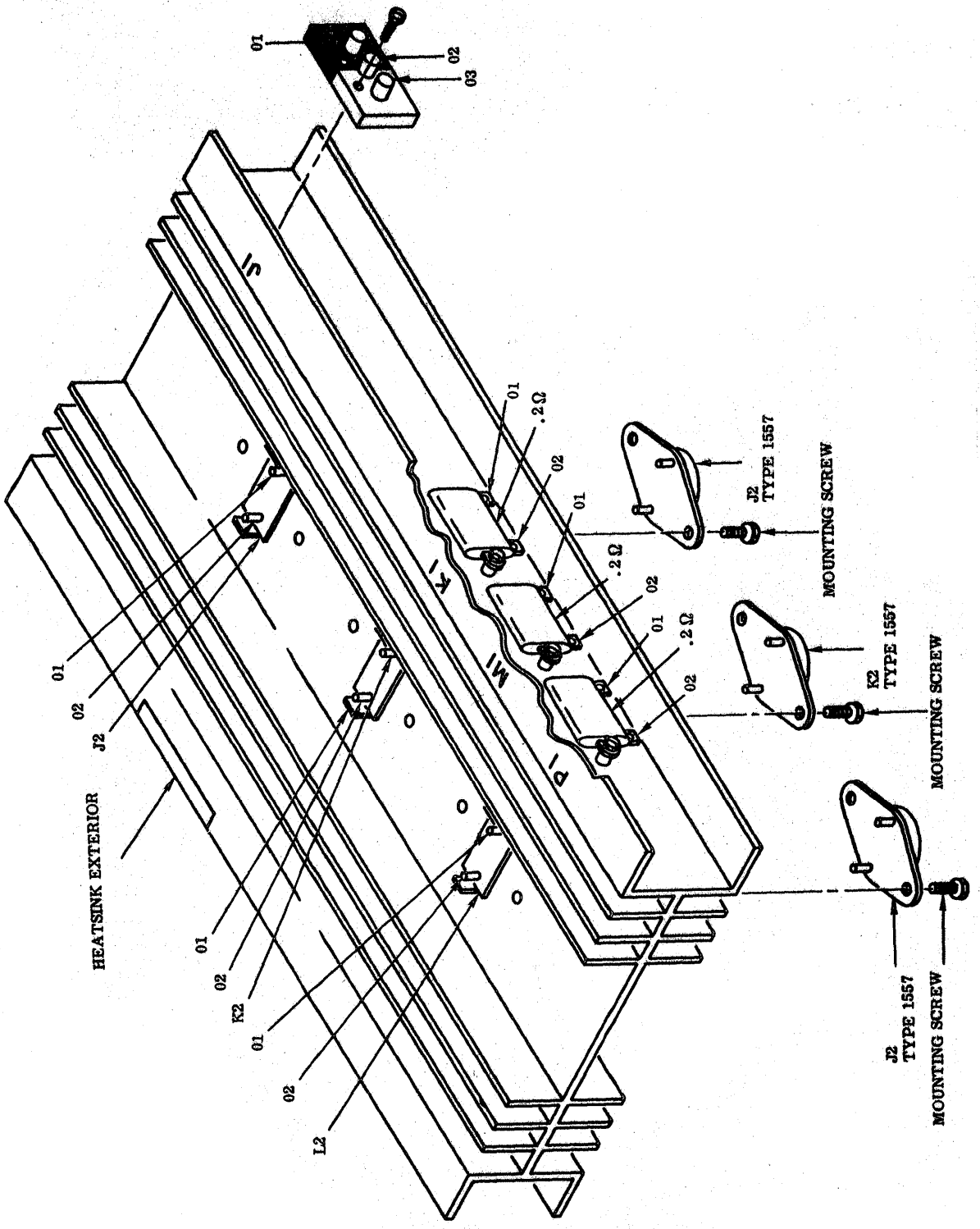


FIGURE 4.2-2. HEATSINK ASSEMBLY #11896255 (TYPE 2)

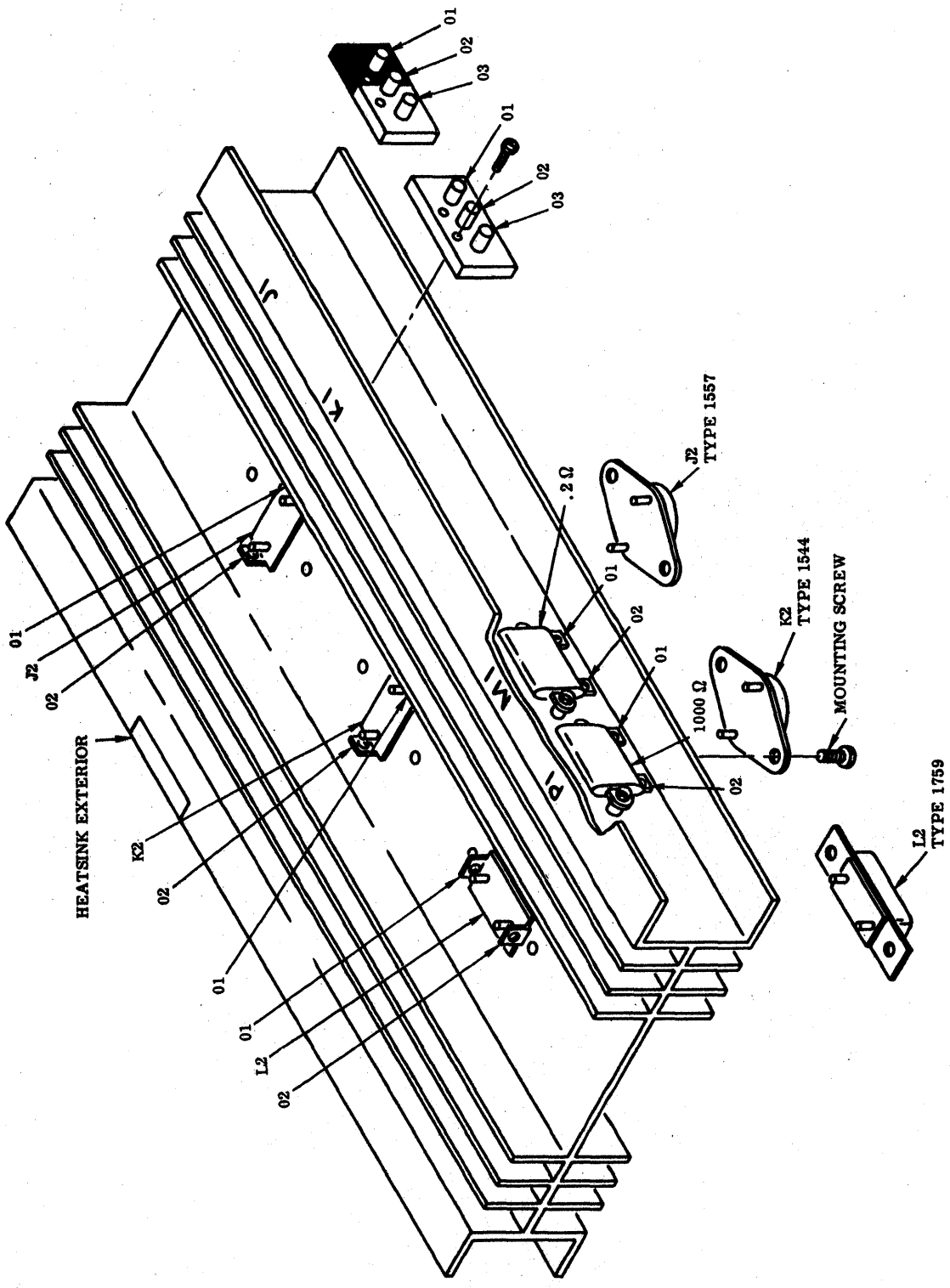


FIGURE 4.2-1. HEATSINK ASSEMBLY #1189627l (TYPE 1)

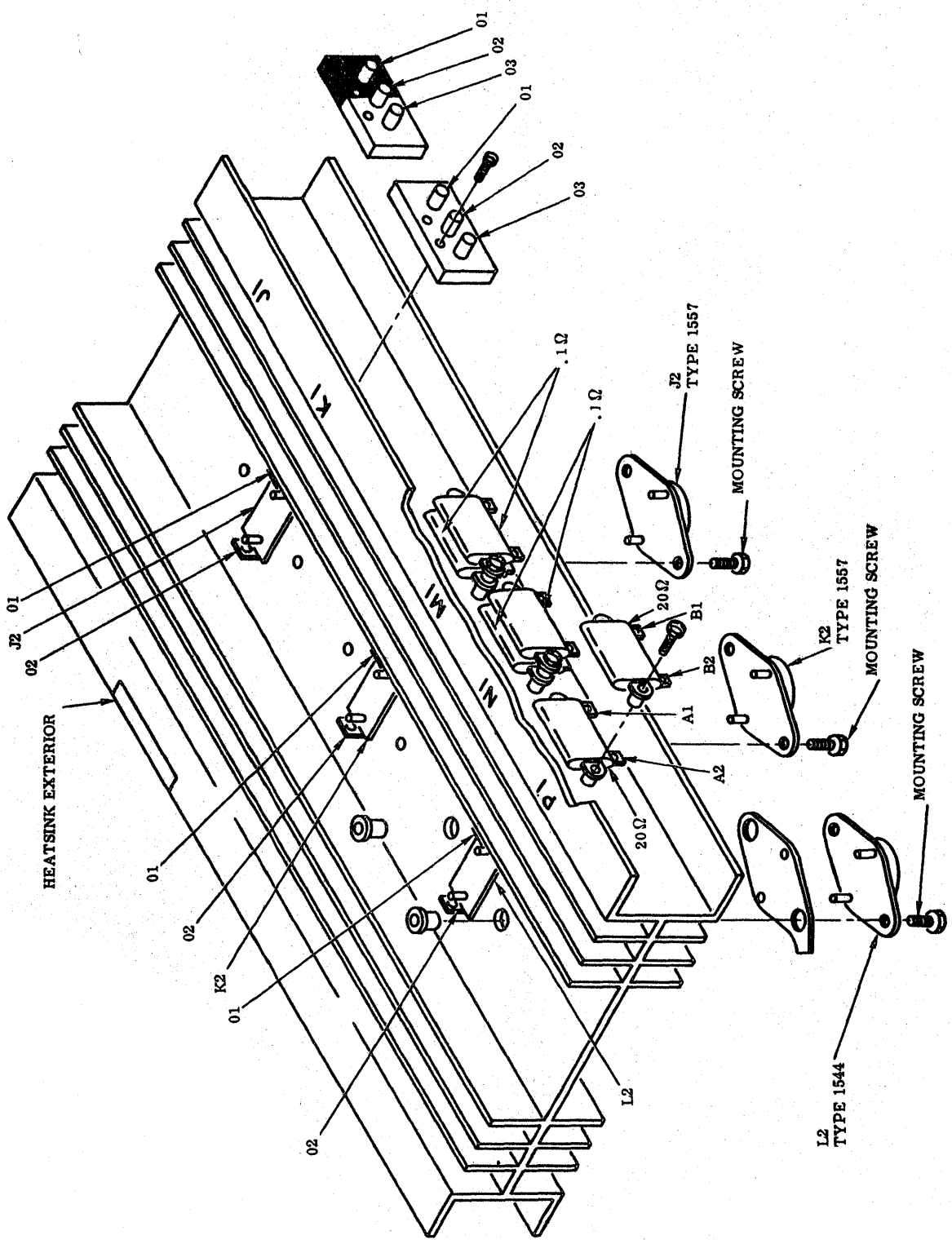


FIGURE 4.2-3. HEATSINK ASSEMBLY #11896297 (TYPE 3)

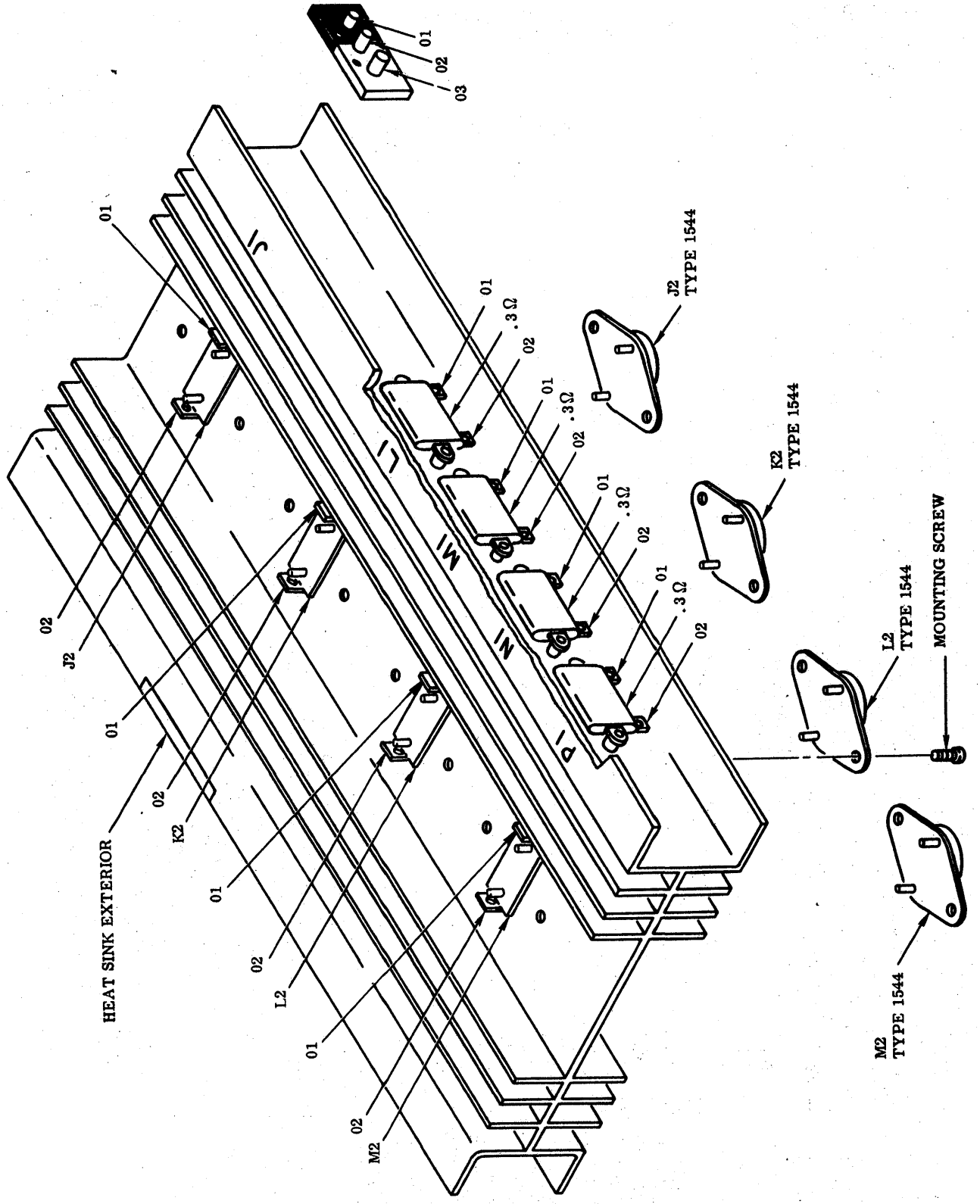


FIGURE 4.2-4. HEATSINK ASSEMBLY #11896313 (TYPE 4)

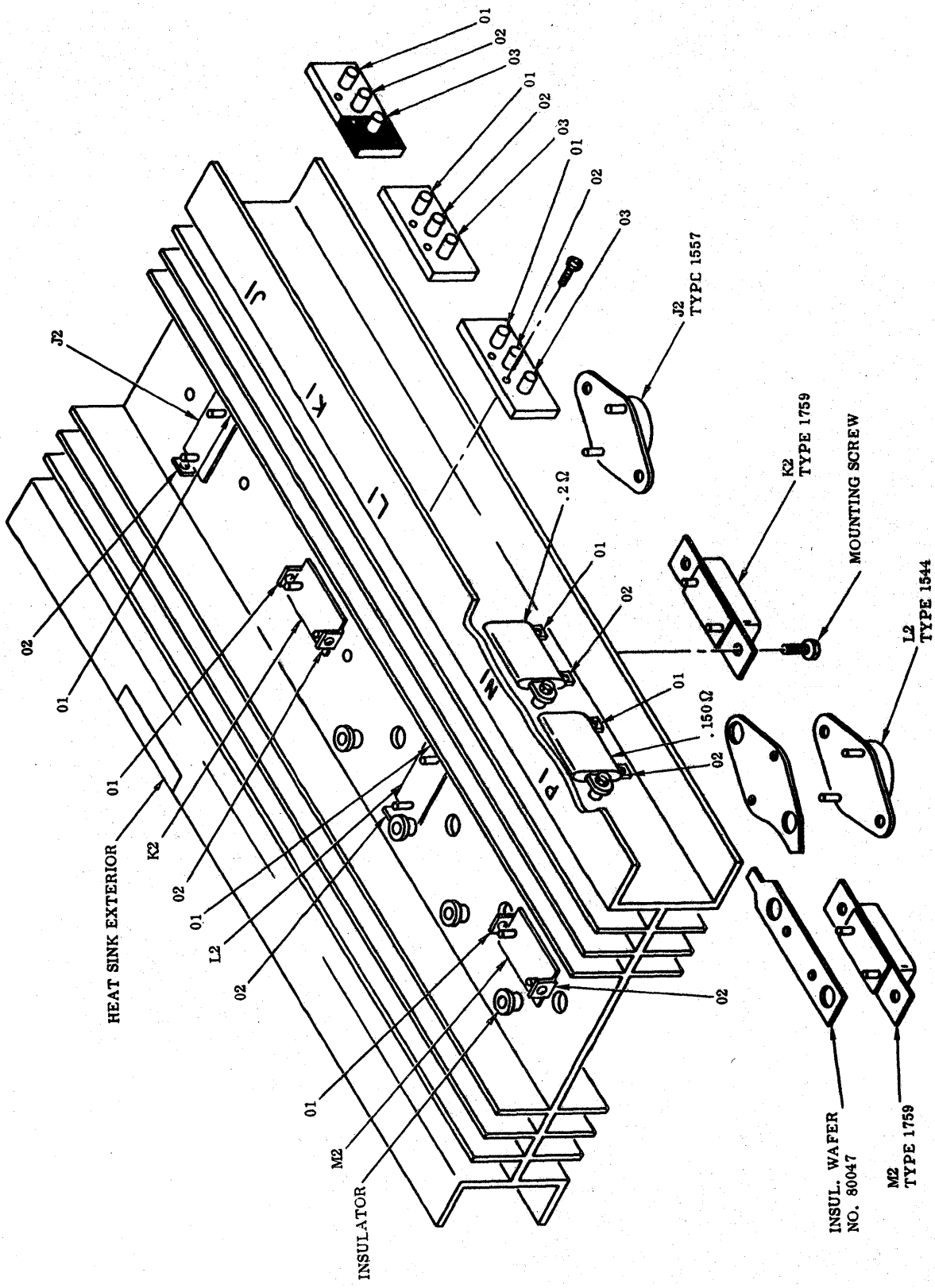


FIGURE 4.2-5. HEATSINK ASSEMBLY #11896339 (TYPE 5)

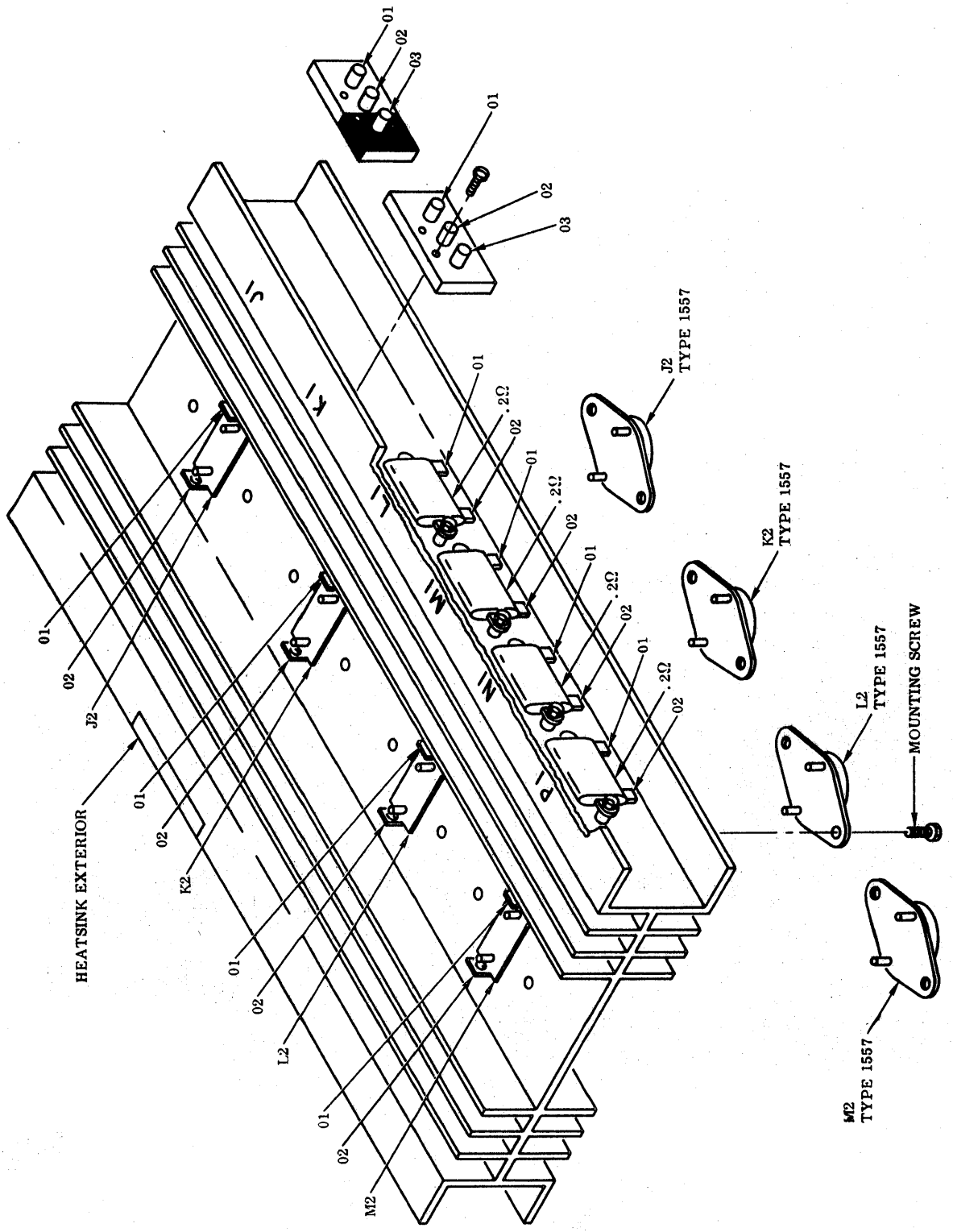


FIGURE 4.2-6. HEATSINK ASSEMBLY #11896354 (TYPE 6)

5.1 INTRODUCTION

The installation procedures described, pertain to the B 5000 Power Supply and the associated controls (from the remainder of the system) necessary to operate the Power Supply for check-out.

The Voltage Regulator and Sensing circuit check-out will also be described. Site preparation such as power, floor space and floor load requirements are assumed completed according to the Pre-Installation Planning Manual and customer specifications. The unpacking and physical placement of the system is assumed completed.

5.2 PRIMARY POWER CONNECTIONS

The 3 wire AC input, neutral, and building ground lines from the Main Power Disconnect are connected to the Power Supply.

For Primary Power Connections, See Figure 5.2-1.

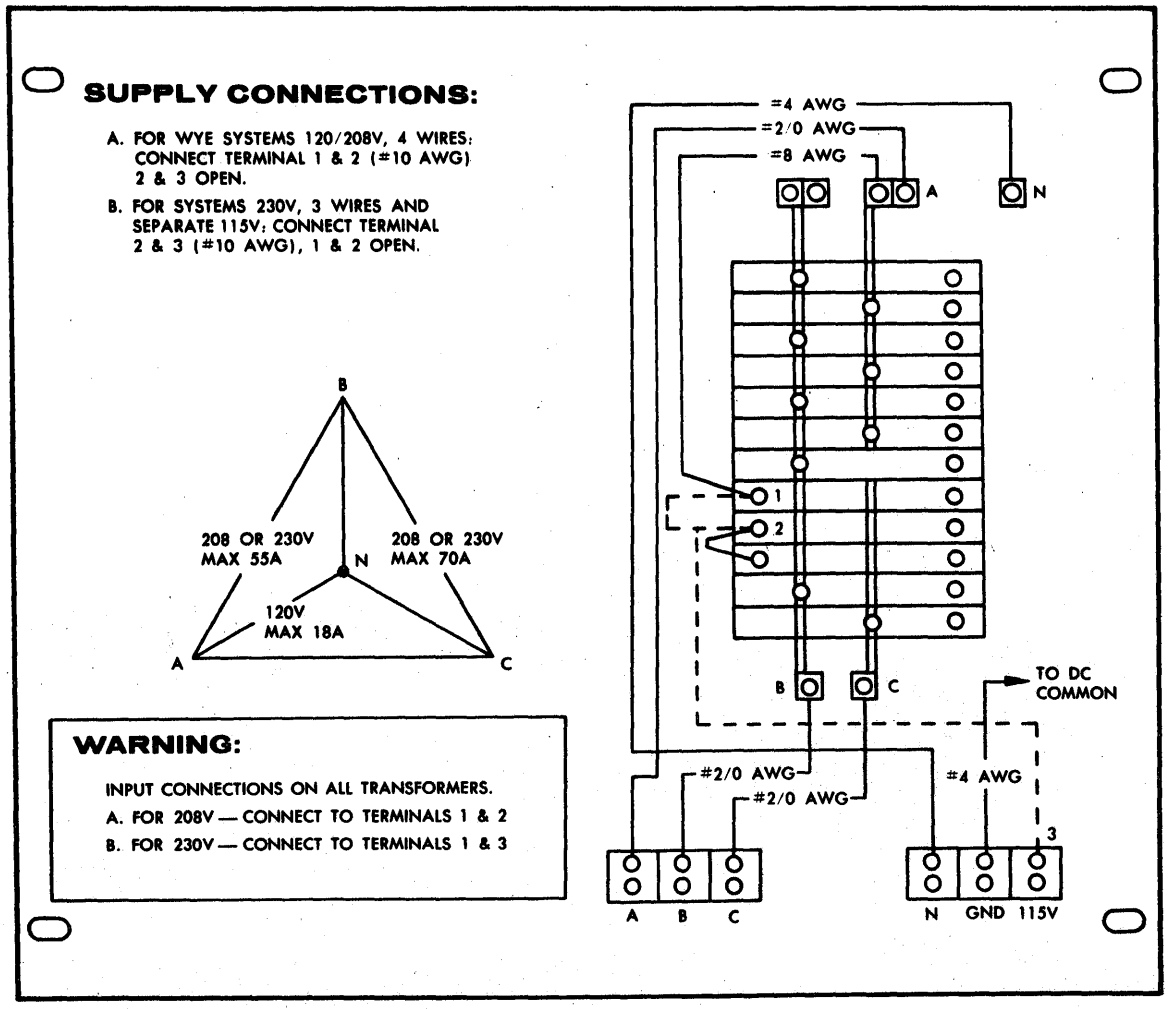


FIGURE 5.2-1. AC POWER CABLE CONNECTION

5.3 CABLING AND POWER SUPPLY TO D & D

SINGLE CONDUCTOR CABLES

Connect the Single Conductor Cables listed in Table 5.3-1 between the Power Supply and the D & D Unit.

Install the Cables in the sequence listed in Table 5.3-1.

TABLE 5.3-1. SINGLE CONDUCTOR CABLES

CABLE NO.	POWER SUPPLY	DISPLAY & DISTRIBUTION	WIRE SIZE	FUNCTION	ASSEMBLY NO.
200	DAJ1 13	DAJ1 02	#4/0	GND	11891629
201	DAJ1 14	DAJ1 01	#4/0	GND	11891629
202	DAJ1 15	DAJ1 01	#4/0	GND	11891629
203	DAK1 06	DAJ1 13	#0	+20 GND	11891611
210	DAK1 05	DBL4 01	#0	+20	11891611
211	DAK8 12	DBL3 01	#4	+19	11891595
212	DAK1 07	DBK3 01	#0	-38	11891611
213	DAK8 13	DBT2 01	#4	-33	11891595
216		DF GND	#4	CABINET GND	11891595

See Figure 5.3-1 for Distribution Box Layout.

CABLING - MINUS 19 VOLTS

The -19V cables (4 minimum, 6 maximum) from the Power Supply to the other units of the system (for example, Processor, I/O Control, etc.) are routed through Display and Distribution, but are not physically connected to it.

Perform the following steps to install the -19V cables.

1. Trip the -19V output circuit breakers in the Power Supply.
2. Insulate the regulator end of each cable until it is ready to be connected to its respective regulator.

Refer to Table 5.5-1, Regulator Power for Regulator Cabling.

MULTIPLE WIRE CABLE

Cable #198 is the only multiple wire cable connected between the Power Supply Unit and the Display and Distribution Unit. This cable carries several low current voltages and miscellaneous control signals. Connect the harness breakouts as indicated in Figure 5.3-2.

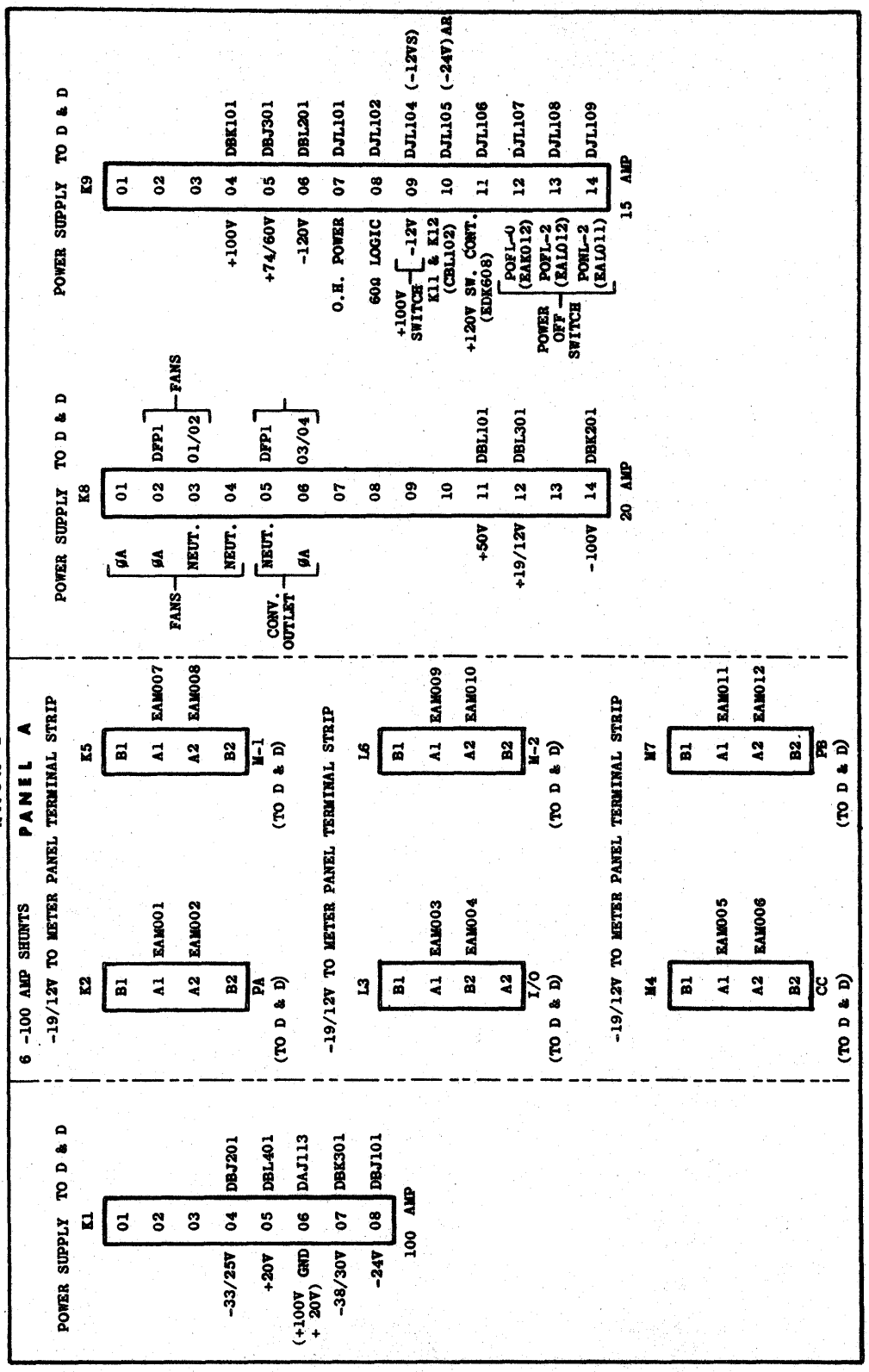


FIGURE 5.3-1. DC DISTRIBUTION BOX

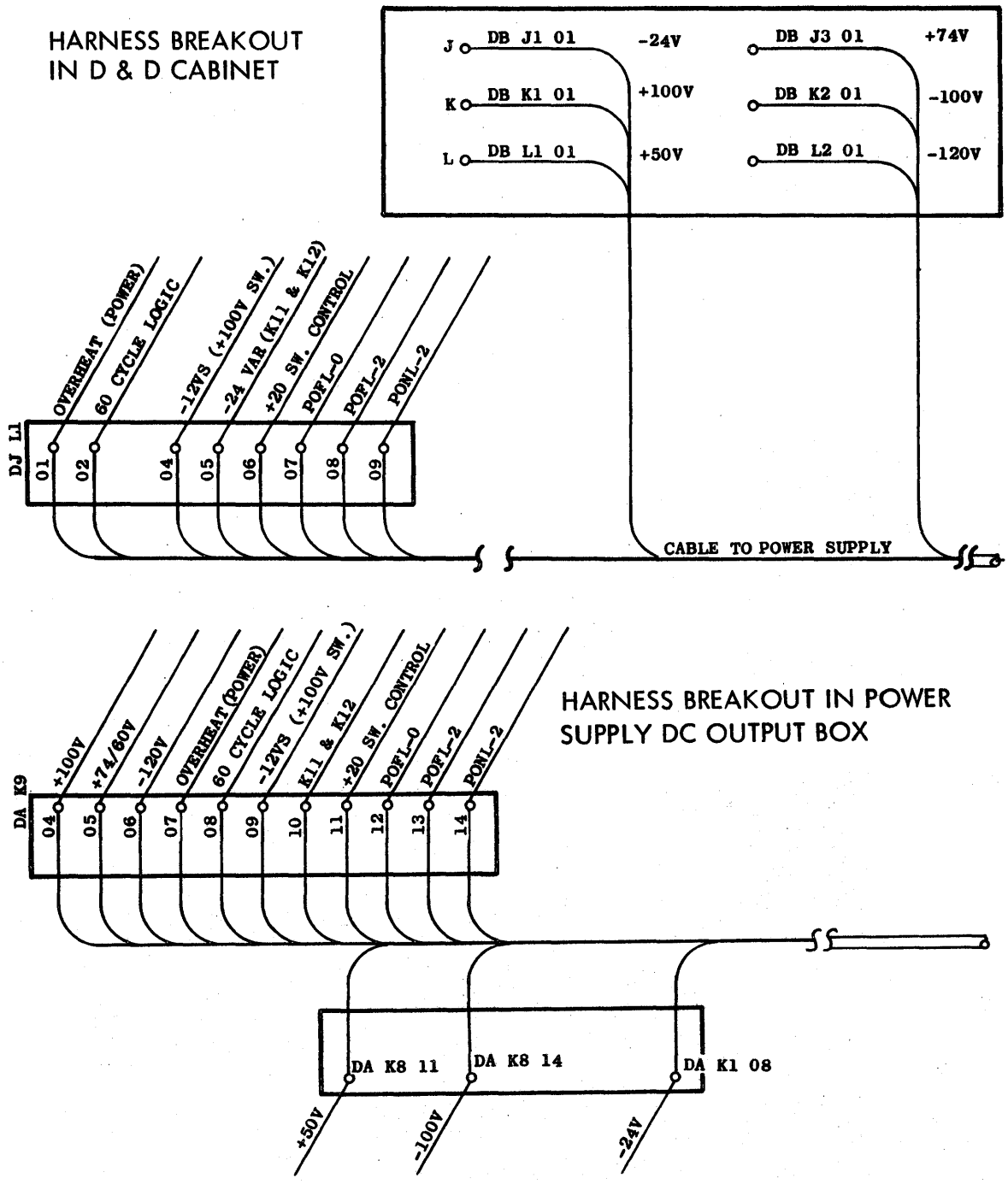


FIGURE 5.3-2. POWER SUPPLY TO D & D CONNECTIONS (FOR CABLE #198)

CONVENIENCE AND FAN POWER CABLES

Install Cable #224 from PS DAK8 05/06 to D & D DFP1 03/04 and from PS DAK8 02/03 to D & D DFP1 01/02. Cable #224 is the Fan Power Cable and convenience outlet power cable.

5.4 POWER ON-OFF

Before the Power Supply can be operated, the Console and Display and Distribution units must be cabled according to Figure 5.4-1 Power On-Off Cabling Requirements.

Only one POWER ON button exists. It is located on the Console.

There are three POWER OFF switches located on the Power Supply, the Console, and the Central Control Panel of D & D. The operation of each of these circuits will be checked.

When the above cabling has been accomplished, perform the following steps:

1. Turn all of the Power Supply Output circuit breakers ON, except the -19V circuit breakers.

2. Close the primary wall breaker and monitor the AC voltage from the Power Supply meter.

3. Check the -24V indicator on the Power Supply Cabinet. It should be ON.

4. Put the DC Lockout Switch (located on the CC Display and Distribution Panel) in the DC on position.

5. Depress the POWER ON button on the Console.

6. Calibrate the Voltmeter and Ammeter on the Power Supply. See Section 3 for procedure.

7. Monitor all DC Supplies from the Power Supply meters.

NOTE

The +20V and +100V will indicate normal on the voltage monitor. However, the monitoring is accomplished on the supply side of the electronic switch. It does not indicate that the electronic switch is functioning properly. The +100 switch will not operate until -12V is available from CC.

8. Turn off the Power Supply from all positions. After Power Off check, leave Power OFF.

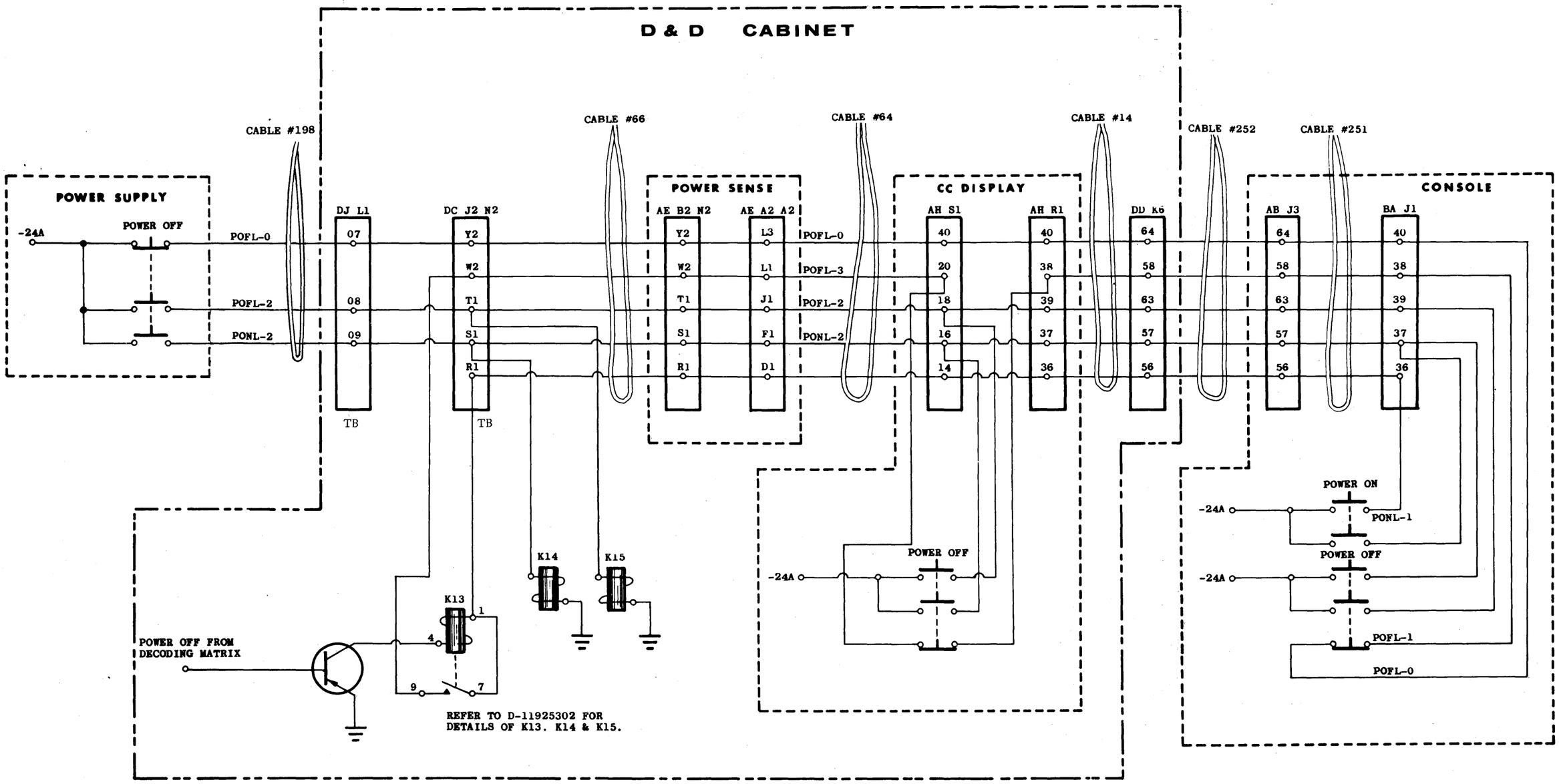


FIGURE 5.4-1. POWER ON-OFF CABLING REQUIREMENTS

5.5 REGULATOR CONNECTIONS AND CHECK OUT

The +50V, +20V, -19V, and -33V Cables must be connected to the regulators. See Table 5.5-1 for connections from PS and D & D to each regulator. See Figure 2.4-2 for pictorial of Voltage Regulator.

TABLE 5.5-1. REGULATOR POWER CONNECTIONS

CABLE NO.	FUNCTION	FROM UNIT	CONNECTOR	TO UNIT	CONNECTOR (ON REG.)	VIA TRAY
204	-19V	PS	DAL3B2	I/O-SS	CAJ101	2R
205	-19V	PS	DAK2B2	PA	CAJ101	2R
206	-19V	PS	DAM7B2	PB	CAJ101	2R
207	-19V	PS	DAL6B2	M-SS2	CAJ101	2R
208	-19V	PS	DAK5B2	M-SS1	CAJ101	2R
209	-19V	PS	DAM4B2	CC	CAJ101	2R
25 - 41	-33V	D & D	DBJ205	CC	CTN201	1R
25 - 42	-33V	D & D	DBJ204	I/O-SS	CTN201	1R
25 - 43	-33V	D & D	DBJ203	DP-A	CTN201	2F
25 - 44	-33V	D & D	DBJ202	DP-B	CTN201	2F
25 - 46	-33V	D & D	DBJ206	M-SS1	CTN201	2F
25 - 47	-33V	D & D	DBJ207	M-SS2	CTN201	2F
25 - 30	+50V	D & D	DBL106	M-SS1	CTN204	2F
25 - 31	+50V	D & D	DBL107	M-SS2	CTN204	2F
25 - 32	+50V	D & D	DBL105	CC	CTN204	1F
25 - 33	+50V	D & D	DBL104	I/O-SS	CTN204	1F
25 - 34	+50V	D & D	DBL103	DP-A	CTN204	2F
25 - 35	+50V	D & D	DBL102	DP-B	CTN204	2F
25 - 21	+20V	D & D	DBL406	M-SS1	CSK112	2F
25 - 22	+20V	D & D	DBL407	M-SS2	CSK112	2F
25 - 23	+20V	D & D	DBL405	CC	CSK112	1F
25 - 24	+20V	D & D	DBL404	I/O-SS	CSK112	1F
25 - 25	+20V	D & D	DBL403	DP-A	CSK112	2F
25 - 26	+20V	D & D	DBL402	DP-B	CSK112	2F

Turn power ON and measure the outputs of all regulators in the system. Use a precision meter.

The regulator output terminals are -12V (CSM1), -4.5V (CSL1), and -1.2V (CSN1). Refer to Figure 2.4-2. These terminals are located on the regulator. The regulator outputs should measure their true values. If not, adjust the following potentiometers.

1. Adjust R36 on the -12V Regulator Amplifier package until the -12V regulator output reads -12V. DO NOT ADJUST R35 ON THE -12V PACKAGE.

2. Adjust R27 on the -4.5V Regulator Package. Adjust R27 on the -1.2V Regulator Package.

5.6 SYSTEM POWER APPLICATION AND VOLTAGE SENSING VERIFICATION

Apply all power. When all units of the system have power applied, perform the following procedure for under and over voltage detection.

1. Install a temporary ground wire to package AFB1A7, Pin K5 on the Sensing Panel of D & D. The ground wire will allow power to remain on, and only the power fail indicators will light for the following check:

   a. Vary all regulator voltages ±10 percent.

      Monitor each voltage with a precision meter. Refer to Figure 2.4-2 for terminals.

      DO NOT VARY THE EXCESS CURRENT POTENTIOMETER (R35) ON THE -12V REGULATOR PACKAGE. This potentiometer is factory set. If adjustment is necessary, see Section 3 for proper procedure.

      The ±10 percent voltage variation should light the proper indicators for each cabinet, voltage condition, and the voltage that failed. Once all regulators have been checked, insure that all voltages are returned to their proper value.

2. Remove the ground wire at AFB1A7, Pin K5 of D & D.

3. Vary one of the regulator voltages to a FAIL condition. The Power Supply should completely shut down except for the -24V Supply.

   a. Adjust the potentiometer to approximately its original position and apply power.

   b. Reset the regulator voltage to its proper value. Refer to Section 5.5 for proper procedure.

DC VOLTAGE RIPPLE

Scope all DC voltages for ripple. Maximum allowable ripple is indicated in Table 5.6-1.

Scope at the input terminals of the D & D Cabinet.

Scope the -19V at one of the regulator units.

DC LOCKOUT

Turn the DC Lockout to the lockout position. The regulator units in the system should shut down. The +20V and +100V output to the system should also shut down.

NOTE

ALL OTHER VOLTAGES WILL BE PRESENT IN D & D

TABLE 5.6-1. POWER SUPPLY RIPPLE

CLASS	POWER SUPPLY DESCRIPTION			QUALIFYING SPECIFICATION				REMARKS
	NO.	DC VOLTAGE	DC CURRENT	MAX. DC VOLTAGE @ NO EXT. LOAD	MIN. DC VOLTAGE @ FULL LOAD	MAX. DC VOLTAGE @ FULL LOAD	MAX. RIPPLE Vpp @ FULL LOAD @ NOM. LINE ±3%	
3	9	-24V	18A	27.0	23.5	25.5	3.5	@ -120V LOADED 80%
3	8	-120V	0.75A	129.0	118.0	124.0	SEE REMARKS	@ -24V LOADED 80% ADJUST C_{F8} SO V PEAK $\leqslant$ 140V
1	2	+20V	30A	22.5	19.5	21.5	1.0	@ +50V LOADED 80%
1	10	+50V	12A	55.0	49.0	52.0	3.5	@ +20V LOADED 80%
2	5	-38/30V	90A	42.0	36.5	38.5	2.2	
1	3	+100V	4A	106.0	99.0	103.0	2.2	@ -100V LOADED 80%
1	4	-100V	14A	108.0	99.0	103.0	3.5	@ +100V LOADED 80%
2	11	+74/60V	8A	78.0	72.0	75.0	3.5	@ +19/12V & -33/25V LOADED 80%
2	6	+19/12V	14A	22.0	18.2	20.0	2.0	@ +74/60V & -33/25V LOADED 80%
2	7	-33/25V	12A	36.0	31.5	33.5	3.5	@ +74/60V & +19/12V LOADED 80%
2	1	-19/12V	500A	21.0	18.2	20.0	1.5	

5.7 FCN INSTALLATION

The purpose of this section is to recommend a procedure to expedite wiring changes when installing FCN's and to explain the new "B" size Circuit List Transcription Form (EDD 1760).

EXPEDITING FCN INSTALLATION

In order to eliminate clerical errors, the circuit list change sheets are not modified from the original engineering instructions. Therefore, the add/delete sequence indicated on the change sheet is not always the most convenient. The following procedure is recommended to expedite wiring changes:

1. Remove all access wires (code 6 in column 71).
2. Remove all level "2" deletes (code 1 in column 71). Levels are encoded in column 25.
3. Remove all level "1" deletes (code 1 in column 71).
4. Add all level "1" adds (code 4 in column 71).
5. Add all level "1" to level "2" adds (code 4 in column 71).
6. Add all level "2" adds (code 4 in column 71).
7. Add all access wires (code 6 in column 71).

When making wire changes which require a wire to be removed and then replaced on the same pin, (status 6, column 71) do not rewrap previously wrapped wire. If length permits, clip off the previously wrapped part and then wrap. If length does not permit clipping, replace the wire.

CIRCUIT LIST TRANSCRIPTION FORM (EDD 1760)

1. The circuit list will consist of a B size sheet as shown one-half scale in Figure 5.7-1.
2. The Circuit List Transcription Form EDD 1760, is a hand prepared document. It is a vellum 17 inches wide and 11 inches in length. The working area of the document is comprised of 34 horizontal rows, each row contains 80 character positions. One (1) character is the maximum allowed in any one character position.
3. The 80 character positions are divided into 21 vertical column increments, each increment is separated by a thick vertical partitioning line (Figure 5.7-1).
4. The usage of the 80 character positions is as follows:

CHARACTER POSITIONS	EXPLANATION
1 ➔ 10	Circuit Number (Single Origin)

A circuit number is derived from the location of the circuit origin on the logic schematic and is comprised of the page number, horizontal row and vertical column of the logic schematic from which the circuit originates. It is thus possible to read the circuit number directly from the schematic.

The illustration (Figure 5.7-2A and 5.7-2B) shows how the circuit numbers of single origin circuits are determined on the logic schematic and transcribed onto the transcription form (Figure 5.7-2C).

Circuit Number (Multiple Origins)

The circuit number of a circuit with multiple origins (if on the same page) is derived from the origin within the circuit which has the lowest horizontal row number and vertical column number on the logic schematic. If the origins are on more than one page, the circuit number is derived from the lowest page number.

The illustration (Figure 5.7-3) shows a circuit with three origins, and how the circuit number is depicted and transcribed.

11 ➔ 14 Circuit Continuity Number

Each wire within a circuit is identified by a continuity number. A continuity number is comprised of four (4) numeric characters. All continuity numbers are assigned in a numerical sequence which allows for the future insertion of additional wires.

The continuity field indicates the order in which the individual wires within a circuit appear on the circuit list.

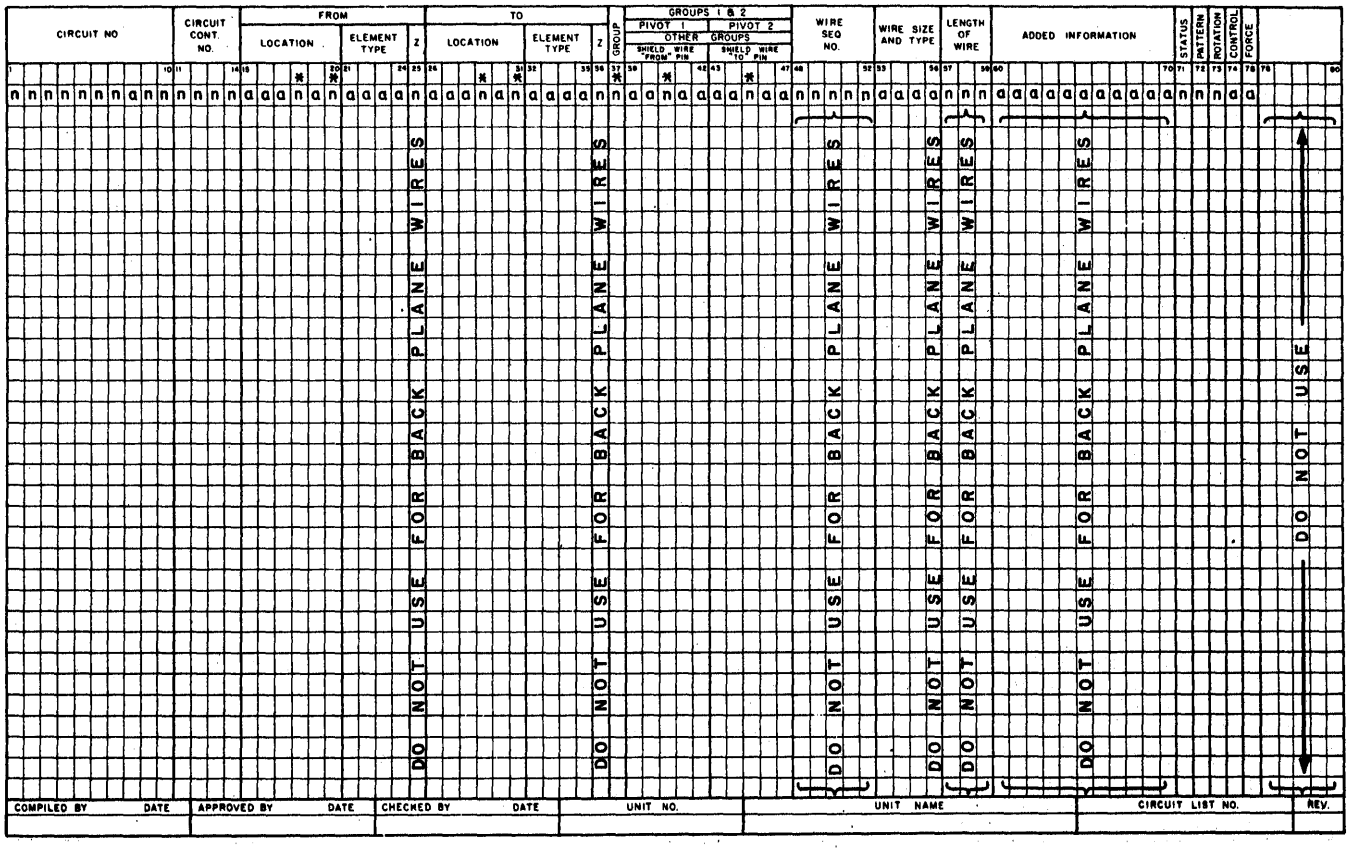


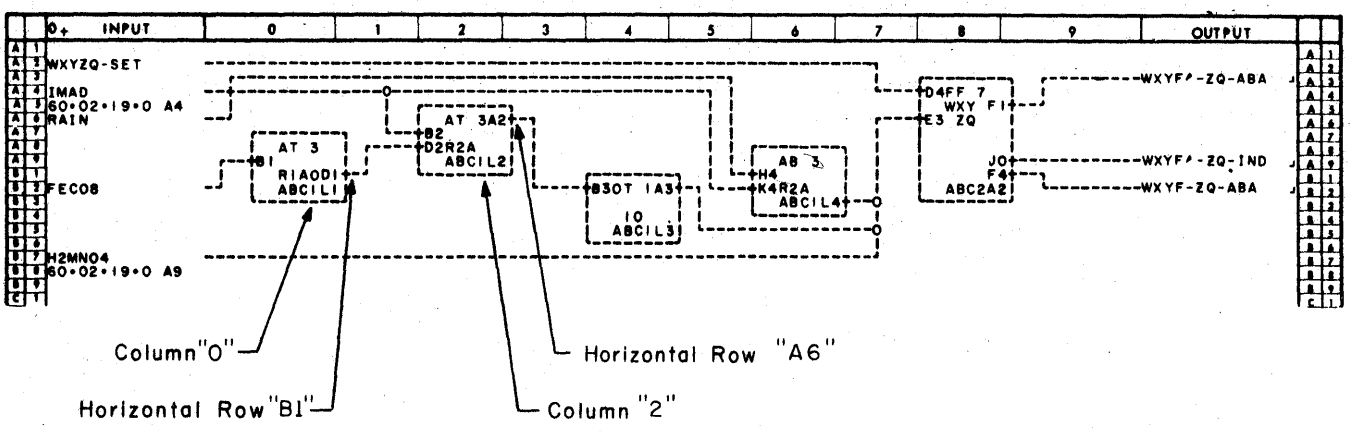
FIGURE 5.7-1. CIRCUIT LIST TRANSCRIPTION FORM, EDD 1760

a - denotes use of alpha character

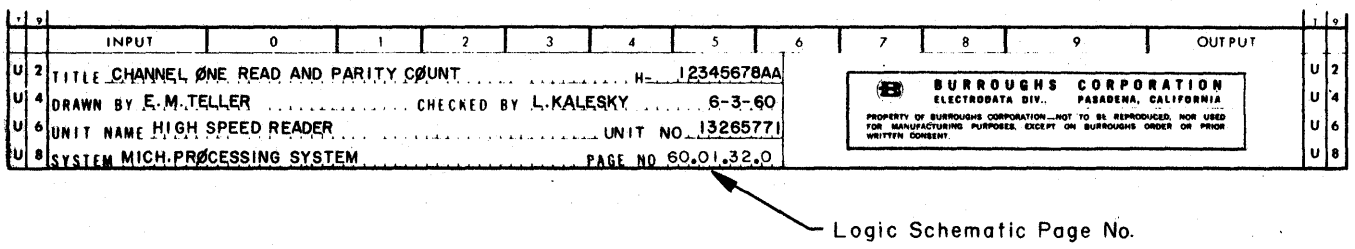
n - denotes use of numeric character

* - denotes that an alpha character may be used for Non Back Plane wires

LOGIC SCHEMATIC



(A)



(B)

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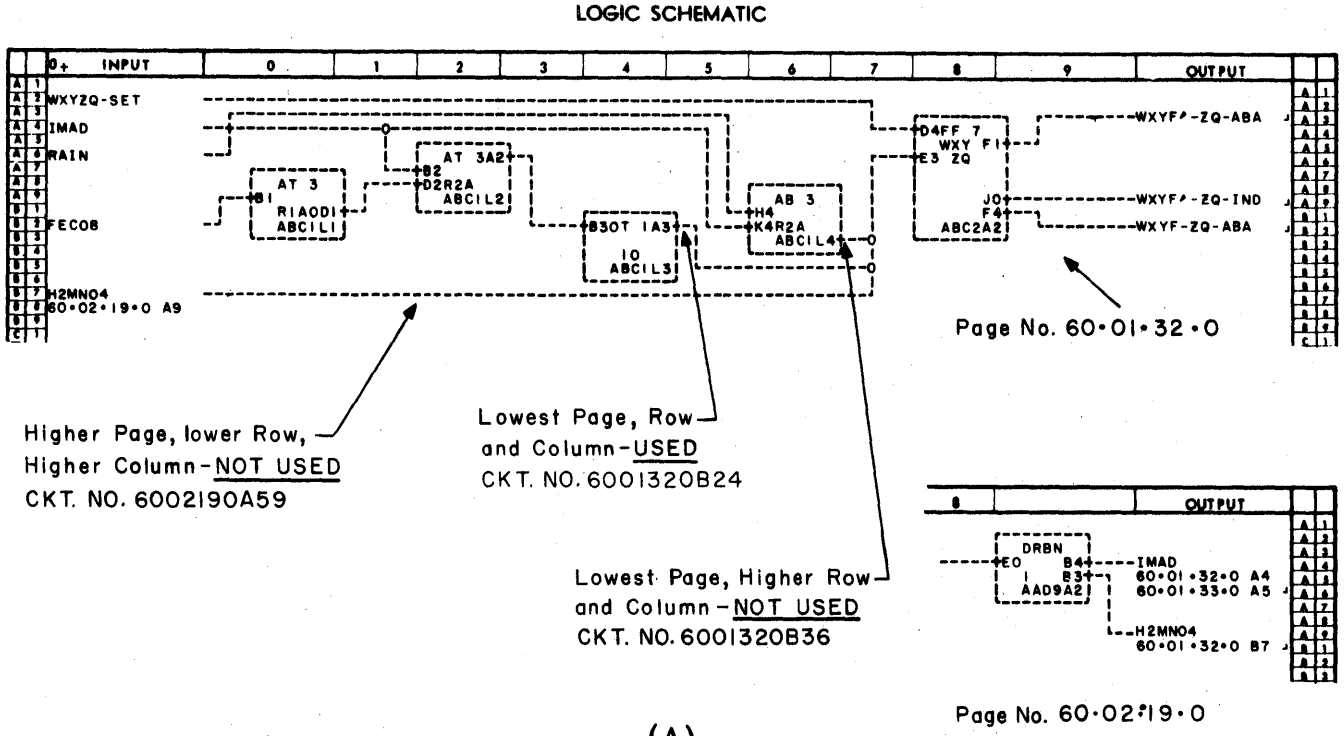
TRANSCRIPTION FORM
CIRCUIT LIST

CIRCUIT NO	CIRCUIT CONT NO	FROM LOCATION	FROM ELEMENT TYPE	FROM Z	TO LOCATION	TO ELEMENT TYPE	TO Z	GROUP	GROUPS 1 & 2 PIVOT 1	GROUPS 1 & 2 PIVOT 2	WIRE SEQ NO	WIRE SIZE AND TYPE	LENGTH OF WIRE	ADDED INFORMATION	STATUS	PATTERN ROTATION	CONTROL	FORCE
6001320B10																		
6001320A62																		

(C)

FIGURE 5.7-2. DETERMINATION AND TRANSCRIPTION OF THE ORIGIN OF SINGLE CIRCUIT



(A)

Burroughs Corporation
ELECTRODATA DIVISION PASADENA CALIFORNIA

TRANSCRIPTION FORM
CIRCUIT LIST

CIRCUIT NO	CIRCUIT CONT NO	FROM LOCATION	FROM ELEMENT TYPE	FROM Z	TO LOCATION	TO ELEMENT TYPE	TO Z	GROUP	GROUPS 1 B 2 PIVOT 1 OTHER GROUPS SHIELD WIRE FROM PIN	GROUPS 1 B 2 PIVOT 2 OTHER GROUPS SHIELD WIRE TO PIN	WIRE SEQ NO	WIRE SIZE AND TYPE	LENGTH OF WIRE	ADDED INFORMATION	STATUS	PATTERN	ROTATION	CONTROL	FORCE
6001320B24																			

(B)

FIGURE 5.7-3. DETERMINATION AND TRANSCRIPTION OF CIRCUIT NUMBER FROM A CIRCUIT WITH MULTIPLE ORIGINS

CHARACTER POSITIONS	EXPLANATION
15 ⇒ 20	Location (FROM)

The location of an Element is depicted in character positions 3 thru 6 on the bottom row of an element box, Figure 5.7-4, and is comprised of the Rack (3), Panel (4), Connector Block Row (5) and Connector Block Column (6). The 'From' or 'To' pin designations are depicted in character positions 1 and 2 for a line entering an element box or character positions 7 and 8 for a line leaving an element box. Figure 5.7-5 gives examples of the above.

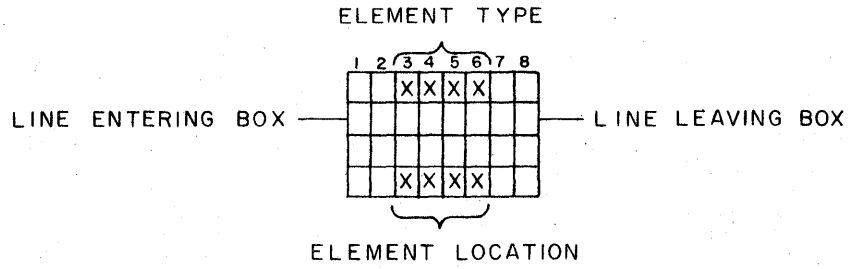


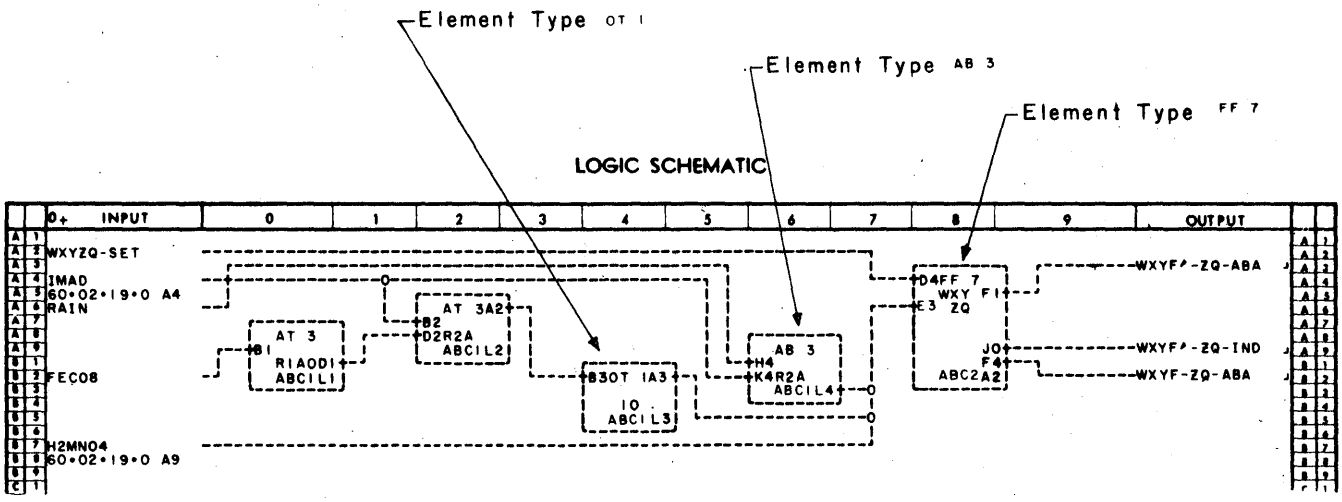
FIGURE 5.7-4. ELEMENT LOCATION AND TYPE DESIGNATION

21 ⇒ 24 Element Type (FROM)

The Element Type is depicted in character positions 3 thru 6 on the top row of an element box (Figure 5.7-4). The Element Type transcription for 'From' pins appears in Vertical Columns 21 thru 24 and for 'To' pins, in Vertical Columns 32 thru 35, (Figure 5.7-5B). These character positions contain abbreviations which indicate the type of elements connected together. Most of the abbreviations may be found in the Design Automation Element representation book. The following list contains additional abbreviations that may appear in these columns:

P	Plug
J	Jack
TB or Y	Terminal Bd.
C	Capacitor (also used as connector)
DS	Buzzer or bell
HS	Heat Sink
L	Choke
M	Meter
NE	Neon

RY	Relay Sec. (K)
SORSw5	Switch
T	Transformer
X	Diode See (CR)
Y	See TB
BG	Building Ground
PHCL	Photo Cell



	'FROM'	'TO'
6001320B24	0100	ABCIA3 → ABCIL4
	0110	ABCIL4 → ABC2E3

PAGE NO. 60•01•32•0

(A)

Burroughs Corporation
ELECTRODATA M & E DIVISION
PASADENA CALIFORNIA

TRANSCRIPTION FORM
CIRCUIT LIST

CIRCUIT NO	CIRCUIT CONT NO	FROM LOCATION	FROM ELEMENT TYPE	FROM Z	TO LOCATION	TO ELEMENT TYPE	TO Z	GROUP	GROUPS 1 & 2 PIVOT 1 / PIVOT 2 / OTHER GROUPS / SHIELD WIRE "FROM" PIN / SHIELD WIRE "TO" PIN	WIRE SEQ NO	WIRE SIZE AND TYPE	LENGTH OF WIRE	ADDED INFORMATION	STATUS	PATTERN	ROTATION	CONTROL	FORCE
6001320B2401 00		ABCIA3	0T	1	ABCIL4	AB	3											
6001320B2401 10		ABCIL4	AB	3	ABC2E3	FF	7											

(B)

FIGURE 5.7-5. 'FROM' AND 'TO' PIN LOCATIONS

CHARACTER POSITIONS	EXPLANATION
25	"Z" (FROM)

The 'Z' Level (Figure 5.7-6) depicts the physical location of the wire wrap on a connector block pin. Two wire wraps are permitted to one pin. The 'Z' Level is applicable to Back Plane wires only. Vertical Character Position 25 is used to designate the 'From' pin 'Z' Level, and Vertical Character Position 36 is used to designate the 'To' pin 'Z' Level. The ground strip pins are allowed one (1) wrap only; the level is assigned as Z1 automatically.

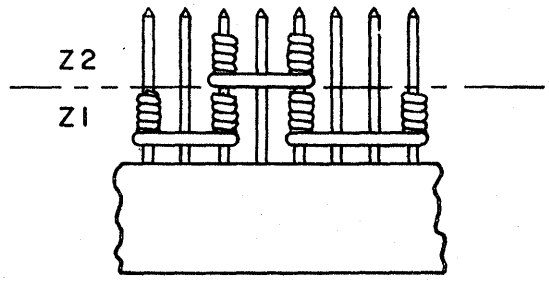


FIGURE 5.7-6. 'Z' LEVELS

26 ⇒ 31	Same as 15 ⇒ 20 except this is the "TO" location.
32 ⇒ 35	Same as 21 ⇒ 24 except this is the "TO" location.
37	Group

Group denotes the type of connection and method of wiring used. Five Groups exist. The character used to denote the Group is transcribed into Vertical Column 37.

The five Groups refer to connections as defined below:

(0) Between two pins not on a wire wrap frame.

(1) Between two pins on the same wire wrap frame (machine installation).

(2) Between two pins on the same wire wrap frame (manual installation).

(3) Between two pins on the same frame non-wire wrap connection such as current loops, etc.

(4) Manual calculation of Gardner-Denver installed wires which cannot be handled through the normal Back Plane processing, specifically ground wires along the 'M' or 'R' pin columns of a connector block. The cards for these wires are entered directly into the Circuit List. No wire entered through the normal Back Plane processing may carry this group number. At present this group is special for the B 5000 System.

(5) Between two pins of different frames of the same rack (Inter-Frame Jumpers and Cables).

38 ⇒ 47 Gardner Denver Wire Wrap Information

If the wire is a twisted pair, columns 38 thru 42 are used to identify the return "FROM" pins. If the wire is a twisted pair, columns 43 thru 47 are used to identify the return "TO" pins.

48 ⇒ 52 Wire Sequence Number

The Wire Sequence Number indicates the order in which wires are installed on frames and is applicable to Back Plane wires only.

53 ⇒ 56 Wire Size and Type

Gage size 12 ⇒ 36
Type - TW - Thin Wall
BS - Buss
TP - Twisted Pair
CX - Coaxial Cable
SD - Solid Wire

57 ⇒ 59 Length of Wire

Gardner Denver Wire Wrap Information

The length of wires between "FROM" and "TO" pins is measured in increments of two tenths of an inch, which is the approximate physical distance between two wire wrap pins. A figure of 24 in character positions 57 ⇒ 59 indicates the length of wire in terms of 24 wire wrap pins resulting in 24 x .2" or 4.8 inches.

60 ⇒ 70 Added Information

Used for Engineering Project Information or specific information on a given connector.

71 Status

STATUS CODE	NAME	DESCRIPTION
1	Wire	Physically remove this wire from the equipment. (Also delete from C/L).
4	Wire Add	Physically add this wire to the equipment. (Also add to C/L).
5	Clerical	Delete this wire from the C/L only. This change does not affect the wiring in any way.
6	Access Wire	This wire must be removed with the deletes and added with the adds to facilitate adding or deleting a wire underneath it.
8	Clerical Add	Add this wire to the C/L only. This code will always have a matching wire listed under code 5.

72 Pattern

Gardner Denver Wire Wrap Patterns for wires.

73 Garnder Denver Wire Wrap Routing for wires.

74 Control

a. A "blank" denotes that the wire is under Schematic Control.

b. A "P" denotes that the wire is under Project control. A "P" must be carried on all wires whose pins are not on the schematic and may be carried on other schematic wires.

c. An "H" denotes a wire produced by the Program whose front pin is obtained not from the schematic but from a "TO" pin of a project control wire.

75 Force

The letter "F" appearing in column 75 indicates that a wire has been rerouted because the routing assigned automatically is unacceptable.

76 ⇒ 80 Undefined.

5.8 INSTALLATION CHECK LIST

1. Remove packing and locate cabinets. Section 5.1-1 of D & D Manual.

2. Bolt cabinets (Processor, I/O, D & D, CC and Core Memory) together. Level and install trim.

NOTE

The process of bolting these cabinets together will necessitate swinging gates open. Where a unit has gates on both sides, open both sides as there is a slight possibility of unbalance with only one side open when the unit is free standing. On units with only one gate, bolt the side with no gate first and then swing the gate to bolt the other side.

3. As the process of adjusting the heads on the drum may be lengthy, it is suggested that the Drum Cabinet be placed in position and wired up first so that the head adjustment can go on concurrently with the hook up on the system. Refer to Section 3.3-1 of the Drum Memory Technical Manual. Prior to applying power, refer to Section 5 of the B 430 Manual.

4. While electricians are hooking up primary power to Power Supply, install convenience and fan cables in the main frame cabinets. Refer to Figure 5.2-3, Detail B, of the D & D Manual. Install the ground straps between the cabinets. Refer to Section 5.3-1 of the D & D Technical Manual.

5. Install ground cables from D & D to Individual Cabinet Regulators.

6. Install power cables (DC and AC) from Power Supply Cabinet to D & D (where required by special conduit, it may be necessary to cut off and relug certain cables at the D & D panel). Refer to Section 5.3-1 of Power Supply Technical Manual.

7. Connect inter-unit cables. Refer to B 5000 System Special Instruction. Document A11891660.

8. Lay out all peripheral unit cables. Do not hook up the D & D end until after power checkout on main frame units.

9. Make resistance checks in Core Memory according to the B 460 Manual, Section 5.4-1.

10. Check out power as described in Power Supply Manual, Section 5.

11. Check out maintenance panel functions (unit checks).

12. Hook up peripheral equipment and check LOCAL and REMOTE operation of each. Manpower permitting, the LOCAL check of peripheral equipment may have been accomplished concurrently with other operations.

13. Check all multis and record settings.

14. Run system tests.

15. Place MCP on Drum and run test ALGOL and/or test COBOL programs.

SECTION 6

CIRCUIT ANALYSIS

6.1 GENERAL

INTRODUCTION

The B 5000 System Power Supply provides all DC voltages required for proper operation of the system, and 115V AC for the Convenience Outlets and Fan Motor Power.

The voltages are distributed through the Display and Distributions Cabinet to the Central Processors, Central Control, Core Memories and the Input/Output which are the Main cabinets of the system; and also to the Control Console.

All power is supplied through the Distribution Panel in the D & D Unit EXCEPT -19V which comes from the Power Supply via the D & D Cabinet to the cabinets with regulator units.

The peripheral units not receiving power from the Main Supply for example, the Drum Memories, Readers, Punches, Printer, Magnetic Tapes, etc., will be dealt with separately and connected electrically for optimum phase balance according to the Pre-Installation Planning Manual.

The raw voltages of the System Supply are developed from transformers of the constant voltage type, and are used as inputs to voltage regulators, drive voltage sensing and shut-down circuits, and energize Control Relays. The raw supplies are also used directly without external regulation within the B 5000 system.

The voltage regulators (B 5000 Regulator Power Unit) develop the regulated voltages -1.2V, -4.5V and -12V. The regulator units are physically separate and each unit provides its own three (3) regulated voltages. There are six (6) of these power units in a maximum system configuration, one in each of the Main cabinets except the Display and Distribution cabinet, Drum cabinet and the Power Supply cabinet. Each of the three voltages, provided by the power unit of each cabinet, is sensed for over and under voltage within the Display and Distribution cabinet. The status is shown by indicator lights.

Excess Current is also sensed from the power unit (-12V Regulator), and indicated on the Power Maintenance Panel located in the Display and Distribution cabinet. In addition, the +20V and +100V Supplies are sensed only in the Display and Distribution cabinet and indicated on the Power Maintenance Panel.

Overheat in the cabinets, and excess current drawn from a power unit (-12V Regulator) and the other FAIL conditions provide automatic shut-down of the system Power Supply.

Voltage is controlled by DC relays. The relays sequence the supplies ON and OFF, provide delays, control peripheral units and Core Memories, and serve inhibit functions.

The operation of the fans in each cabinet, and power for the running of the Elapsed Time Meter is under the control of the relay contactors. Also under power control, but not directly associated with the contactors, is a manual switch to remove DC power from Core Memories and the Regulator Units.

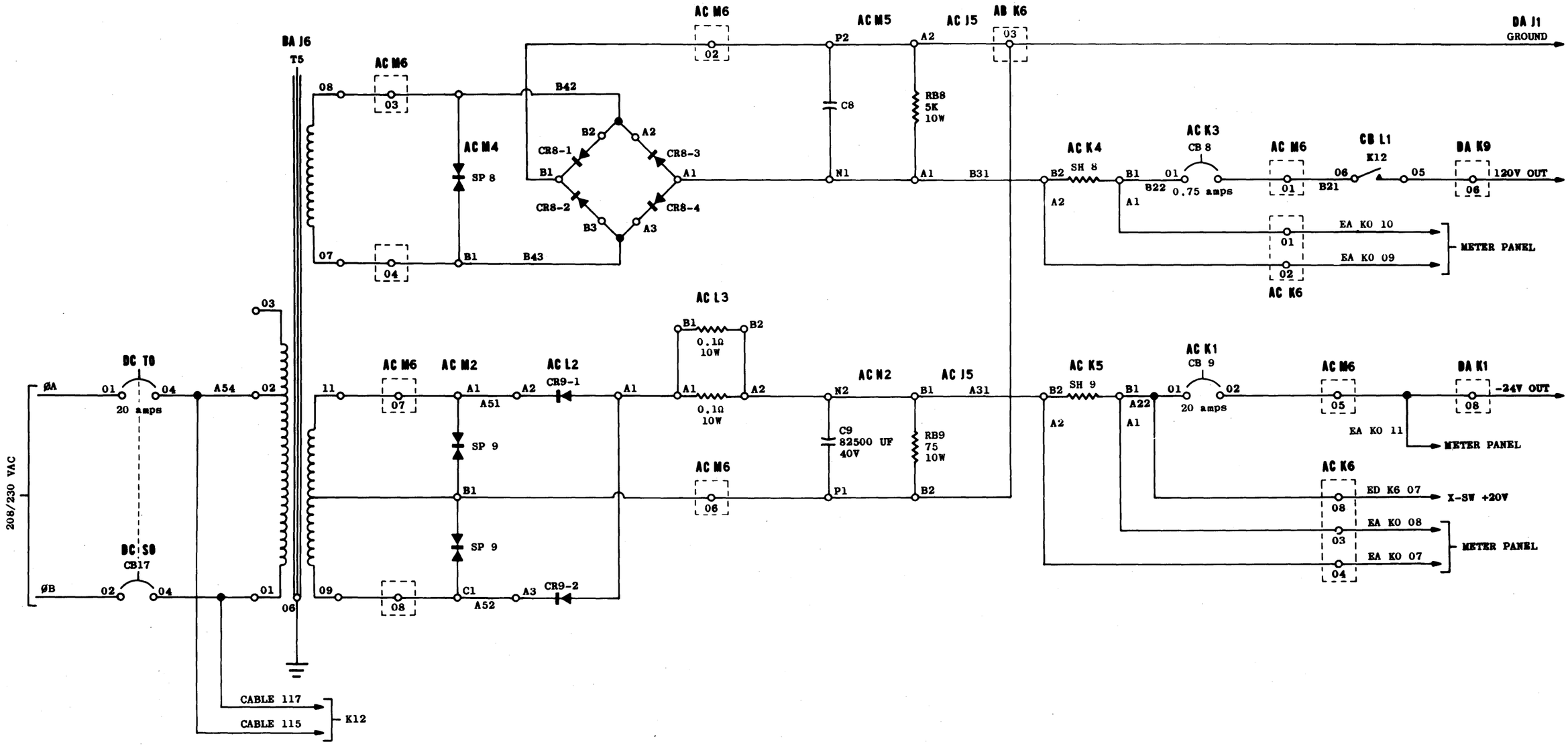
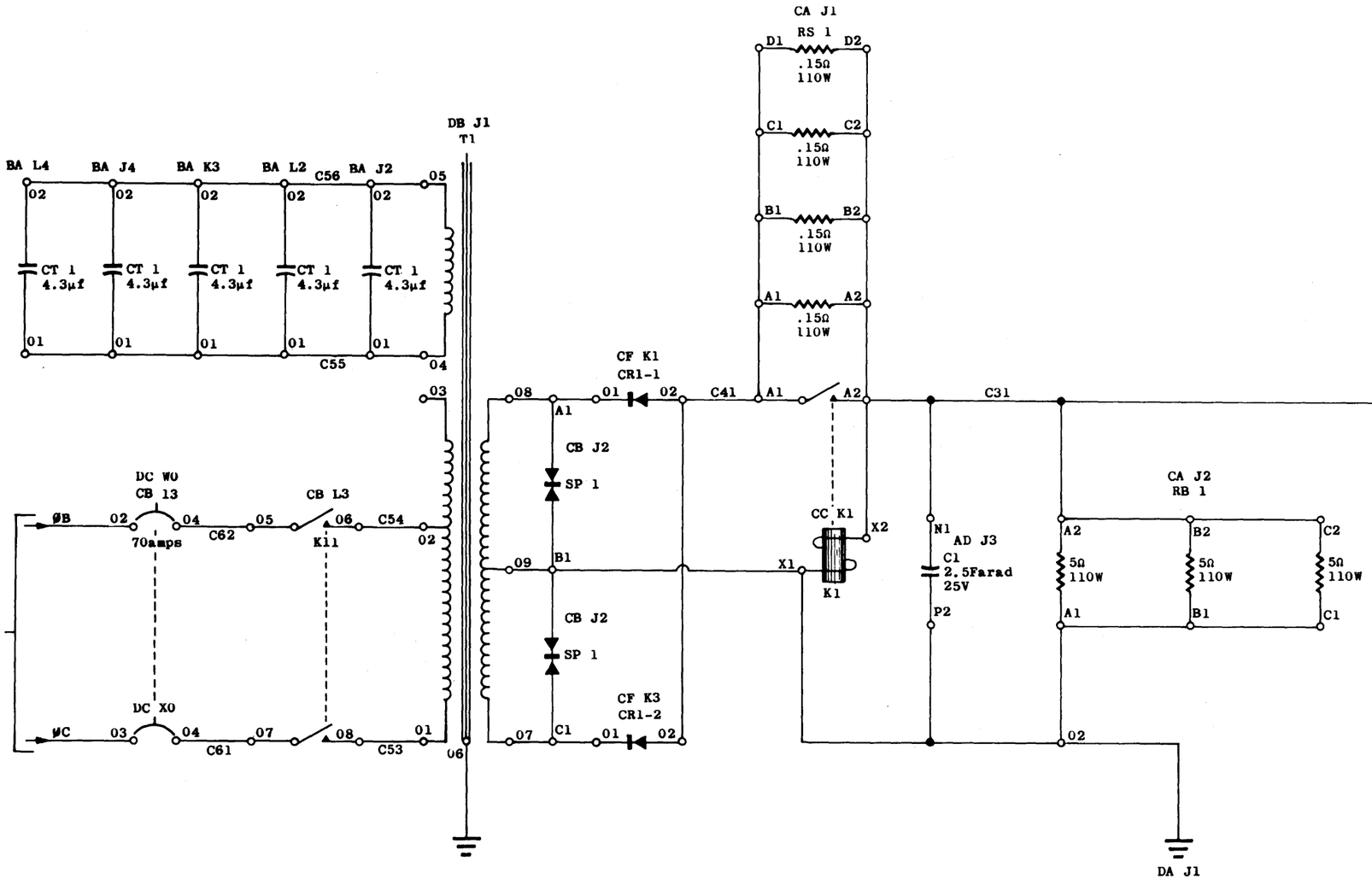


FIGURE 6.2-1. -24V AND -120V SUPPLY



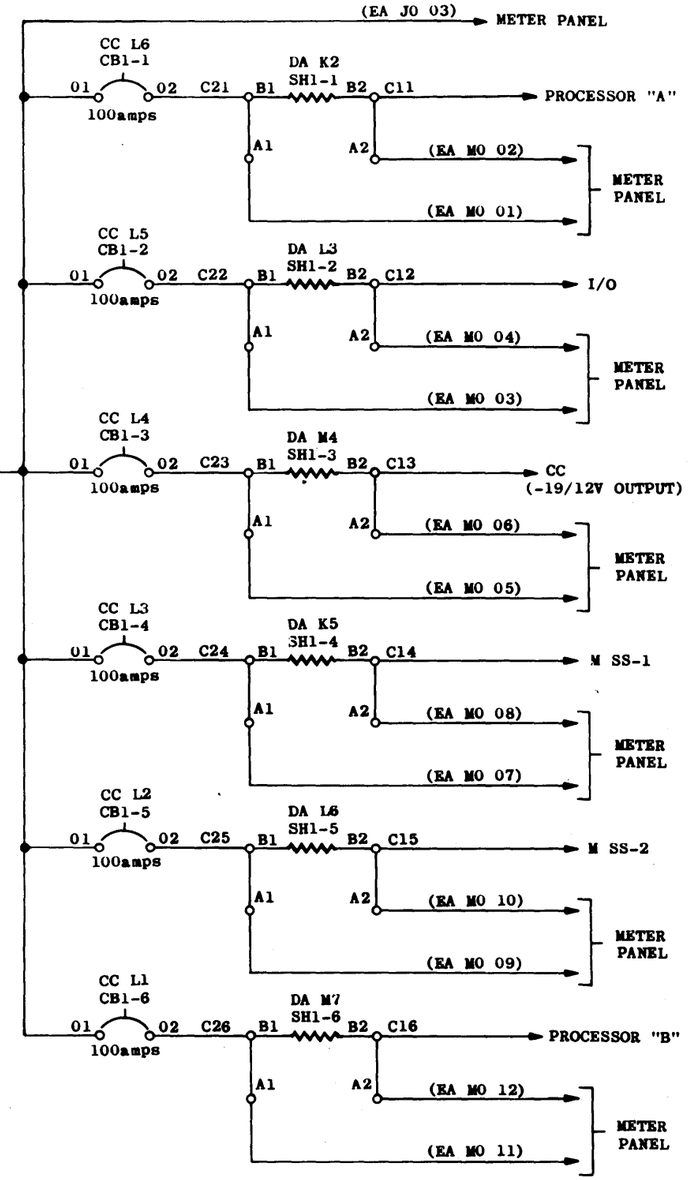


FIGURE 6.2-2. -19/12V SUPPLY

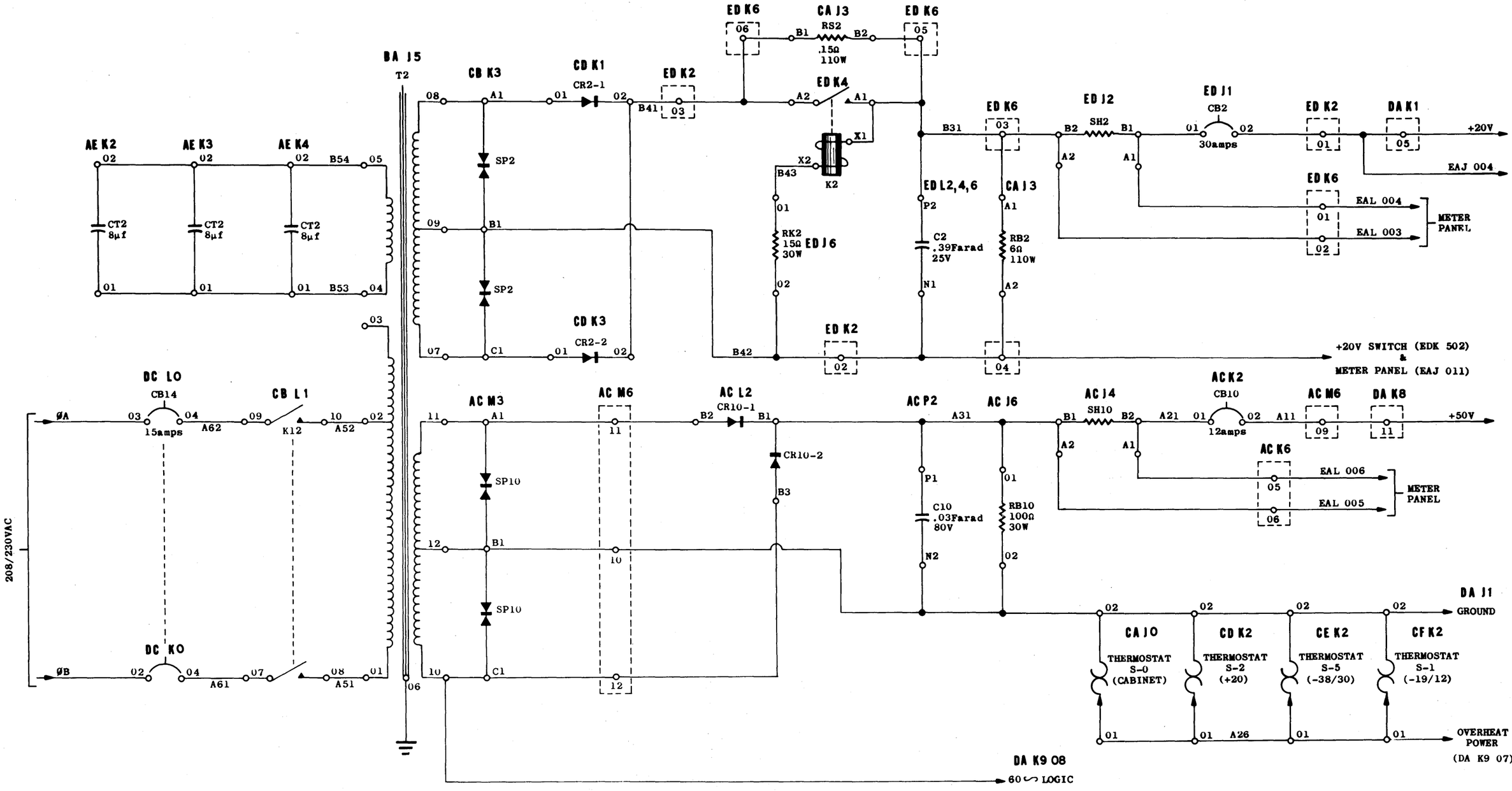


FIGURE 6.2-3. +20V AND +50V SUPPLIES

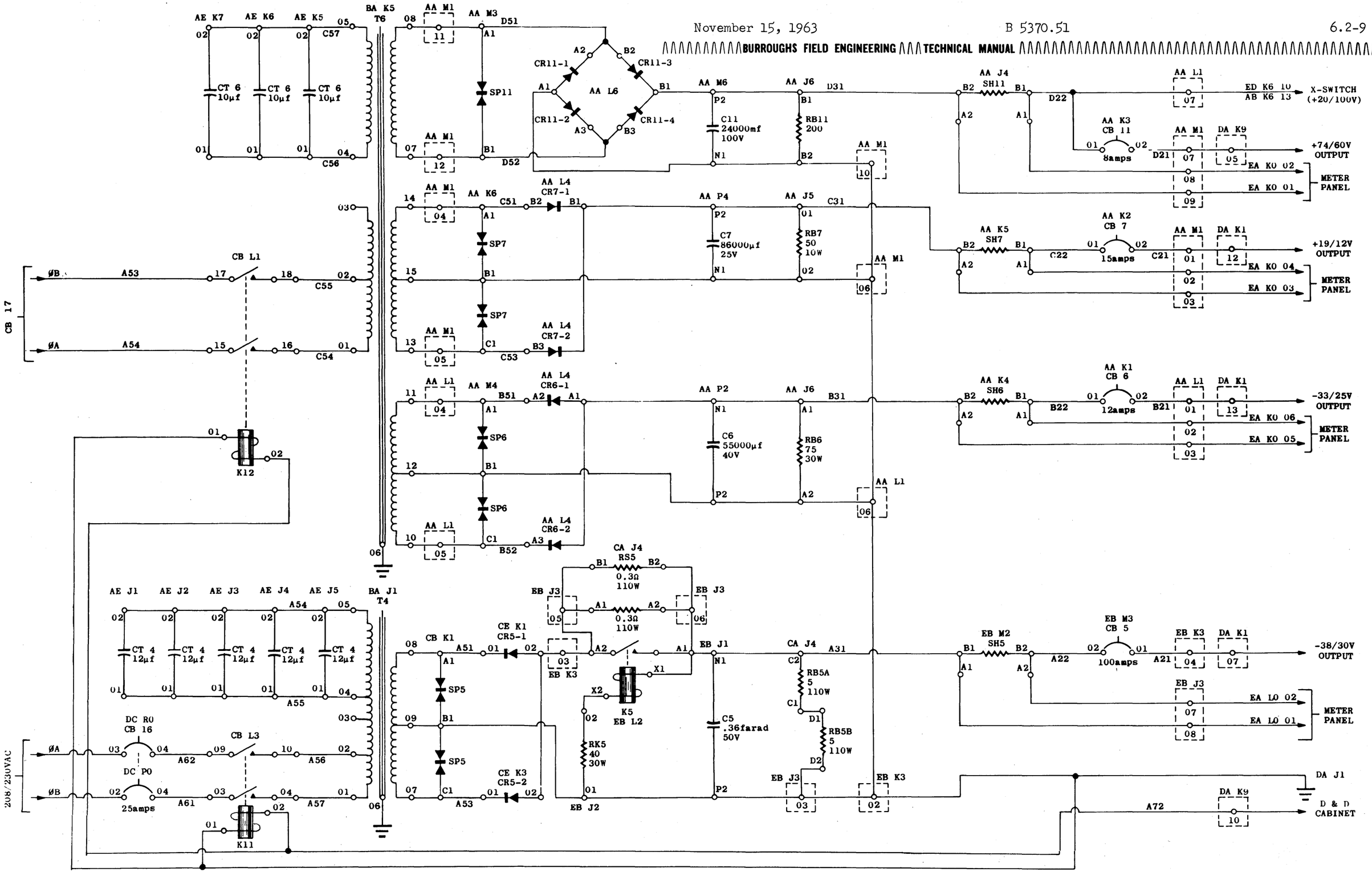


FIGURE 6.2-4. +74/60V, +19/12V, -33/25V, and -38/30V SUPPLIES

6.2 UNREGULATED SUPPLIES

There are six (6) Power Transformers supplying eleven (11) separate raw voltages: ±19V, +20V, -24V-A, -33V, -38V, +50V, +74V, ±100V, and -120V. These transformers are supplied from the input line voltage.

The primary windings of all the transformers except transformer 5 are controlled through contacts of power control relays. Transformer 5 provides -24V-A (control voltage) for power sequencing and -120 neon voltage as soon as primary power is applied. Refer to Figure 6.2-1. The -120 neon voltage is only available in the Power Supply unit until K12 is picked. Also, at this time, 115V, 60 cycle power is supplied to the convenience outlets. Each transformer primary is protected by a circuit breaker.

CIRCUIT DESCRIPTION

Refer to Figures 6.2-2, 3, 4, and 5.

Transformers 1, 2, 3, 4 and 6 are of the constant voltage type. These transformers stabilize line input fluctuations from ±13 percent to approximately ±1 percent, and are used with supplies requiring this regulation.

When supplies require the use of the complete secondary tranformer winding, bridge rectifiers are used. Circuits of this type are +74V, -120V, and the ±100V supplies. Other circuits requiring only partial use of their transformer secondaries use the two full wave diode rectifier circuits.

The Surge Suppressors (SP) across the transformer secondary windings are of the selinium stack type and are used to suppress the starting surge, due to the large amount of capacitance. They have no function during normal supply operation.

The relays K1, K2 and K5 are used to shunt the current limiting series resistor circuits which prevent the filter capacitors from drawing an excess of current which could damage the rectifier circuits at the onset of power. As the capacitors charge, the relays pick and shunt the current around the limiting resistors.

The fans in each unit, which are tied in parallel across the 115V AC line, are used to cool the individual unit cabinets.

The Elapsed Time Meter indicates the time in hours that the DC Power has been available to the system.

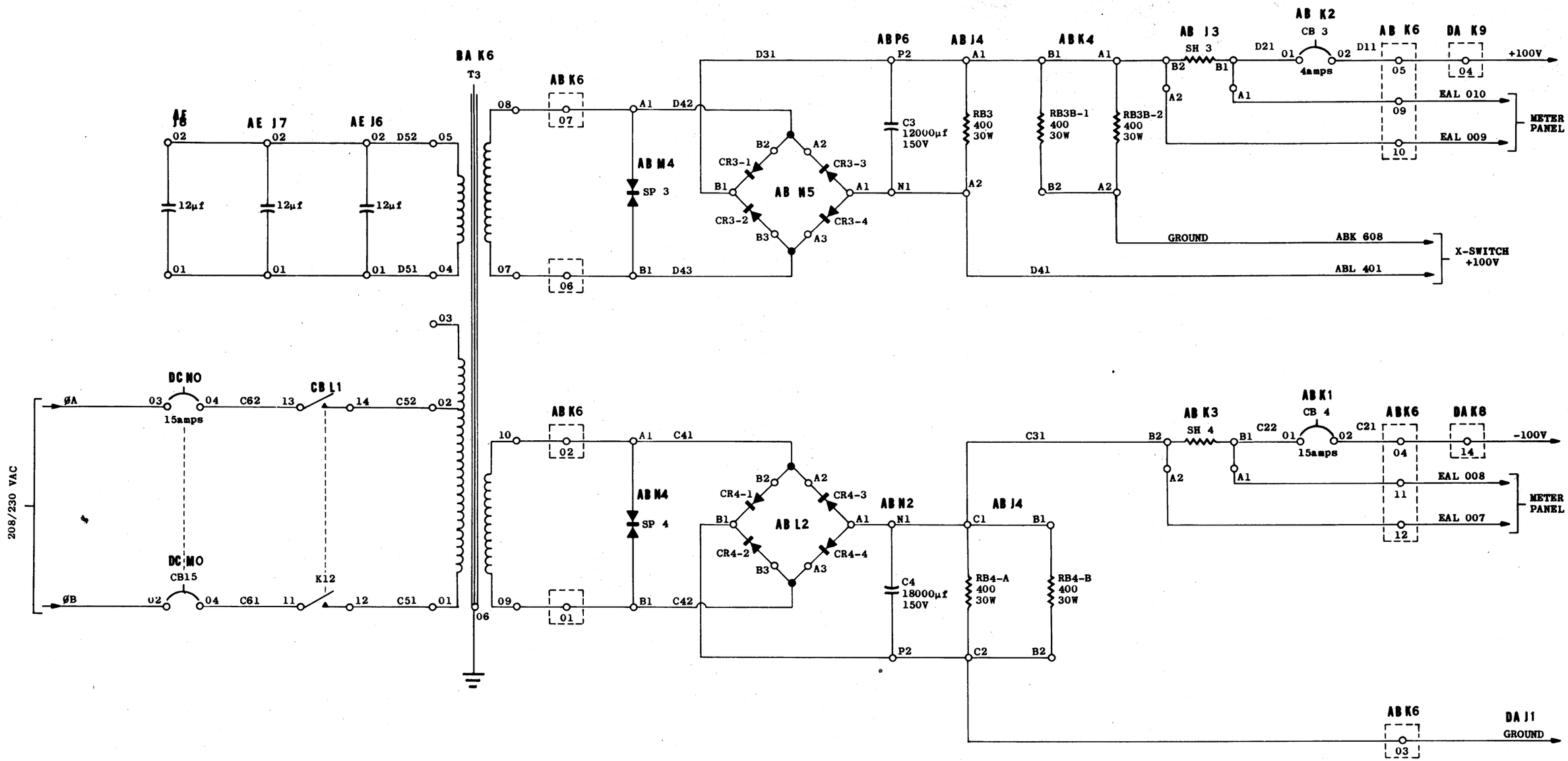


FIGURE 6.2-5. +100V AND -100V SUPPLIES

6.3 +20 VOLT ELECTRICAL SWITCH

INTRODUCTION

The +20V Electrical Switch is a circuit which provides the means of controlling the +20V Power Supply. This circuit is used to insure that the +20V power is supplied to the transistor circuit prior to the negative voltages. In this way, damage to circuit components is prevented.

This circuit also provides a means of removing the negative potentials from the circuitry, prior to removal of the bias voltage when power is lost due to a power failure, or during power shut down.

CIRCUIT DESCRIPTION

Refer to Figure 6.3-1.

In the quiescent state, the emitter follower transistor Q1 has a ground input at DA K9 11 and Q2 is cut off. (This is for Power OFF state.)

The collector voltage of Q2 is from the +20V Supply Common and, depending on whether the transistor Q2 is cut off or saturated, this +20 Common is completed or open, thereby acting as a switch. The +7.4V and the -24V are bias voltages used in this switch. The -24V is used on the collector of Q1 rather than -12V which is not available prior to the +20V switch. The -24V is available with the wall circuit breaker ON.

The input at DA K9 11 (+20 Control from D & D cabinet), is the input from Control Relay K19 in the Display and Distribution cabinet. When the power fails in any manner, the +20V Supply is the first supply that starts down. All other voltages follow in sequence.

During normal operation -12V is supplied thru a 12.1K resistance to DA K9 11. Negative 24V is available with the wall circuit breaker on. This back biases the diode CR3, allowing base drive current to flow through diodes CR2 and CR1. With the emitter of Q1 tied to +7.4V, transistor Q1 is saturated. With Q1 on, negative drive current is supplied to the base of Q2 turning it on through the forward biased base emitter junction to ground. With the transistor Q2 on, the +20V Common circuit is complete and +20V is available to the system.

During a power failure or shut down, DA K9 11 is false (ground), shunting the Q1 base drive current, and allowing +7.4V through resistor R4 to take Q1 to less conduction. With Q1 conducting less, +7.4V through resistor R1 cuts off Q2, opening the +20V common. This drops the +20V Supply and subsequent voltage will follow.

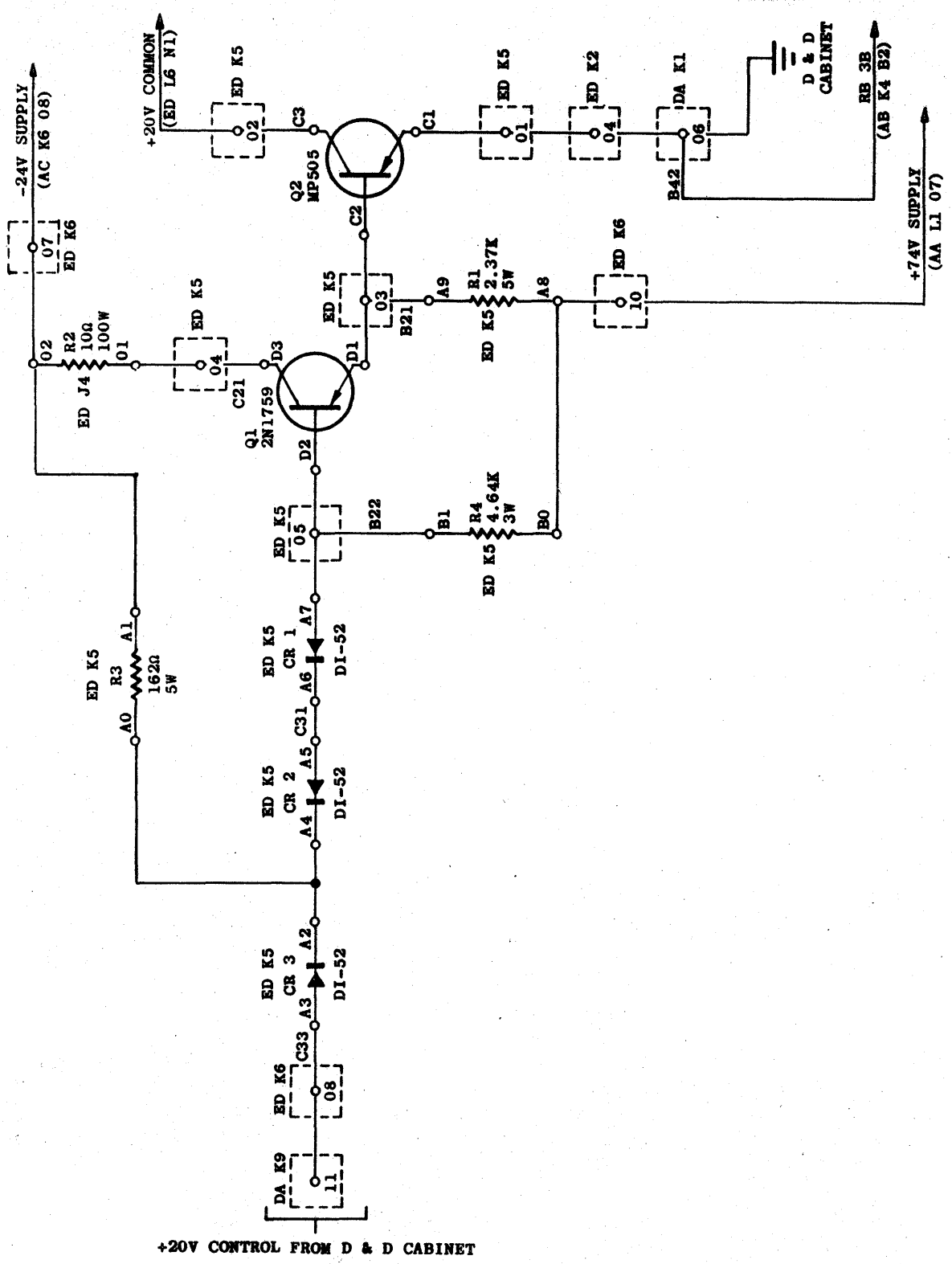


FIGURE 6.3-1. +20V ELECTRICAL SWITCH

6.4 +100 VOLT ELECTRICAL SWITCH

INTRODUCTION

The +100V Electrical Switch provides a means of controlling the +100V Power Supply. The switch circuit is used to insure that all other voltages are present on the system prior to the +100V. The +100V is used to develop the +20V delayed to clear all flip-flops when power is applied.

CIRCUIT DESCRIPTION

Refer to Figure 6.4-1.

In the quiescent state Q1 is in saturation due to the input at DA K9 09 being at ground. The emitter follower, Q2, is conducting enough to hold its emitter at approximately +0.9V. Q3 will be cut off due to Q2. Q4 will also be cut off due to Q3 being at cut off. The +100V Supply will not have a ground reference due to Q3 and Q4. When the circuit goes from the quiescent state to operating state, Q1 senses the change from ground to -12V at DA K9 09. When the emitter of Q1 reaches approximately -9V, Q1 will cut off. At this time, Q2 will be biased on to almost full drive. Q3 will remain off until Q3 receives full drive current. At that time, Q3 will switch to saturation. When Q3 switches, Q4 will also switch to saturation due to the collector emitter circuit of Q3 and Q4. Q4 receives its base drive from the -12V thru CR2. This action causes the collector of Q4 to reference the +100 common line to near ground.

The capacitor and diode circuit in the collector of Q4 allows Q3 and Q4 to turn off at a very low collector voltage. During turnoff transistion, the current normally supplied by Q3 and Q4 comes out of C1 thru CR3. The voltage +100 common decays toward -100V as C1 becomes charged. To lower the surge current of Q3 and Q4 during turn on transistion, the amount of currrent going into C1 is limited by R10. C1 charges on an RC time constant at this time.

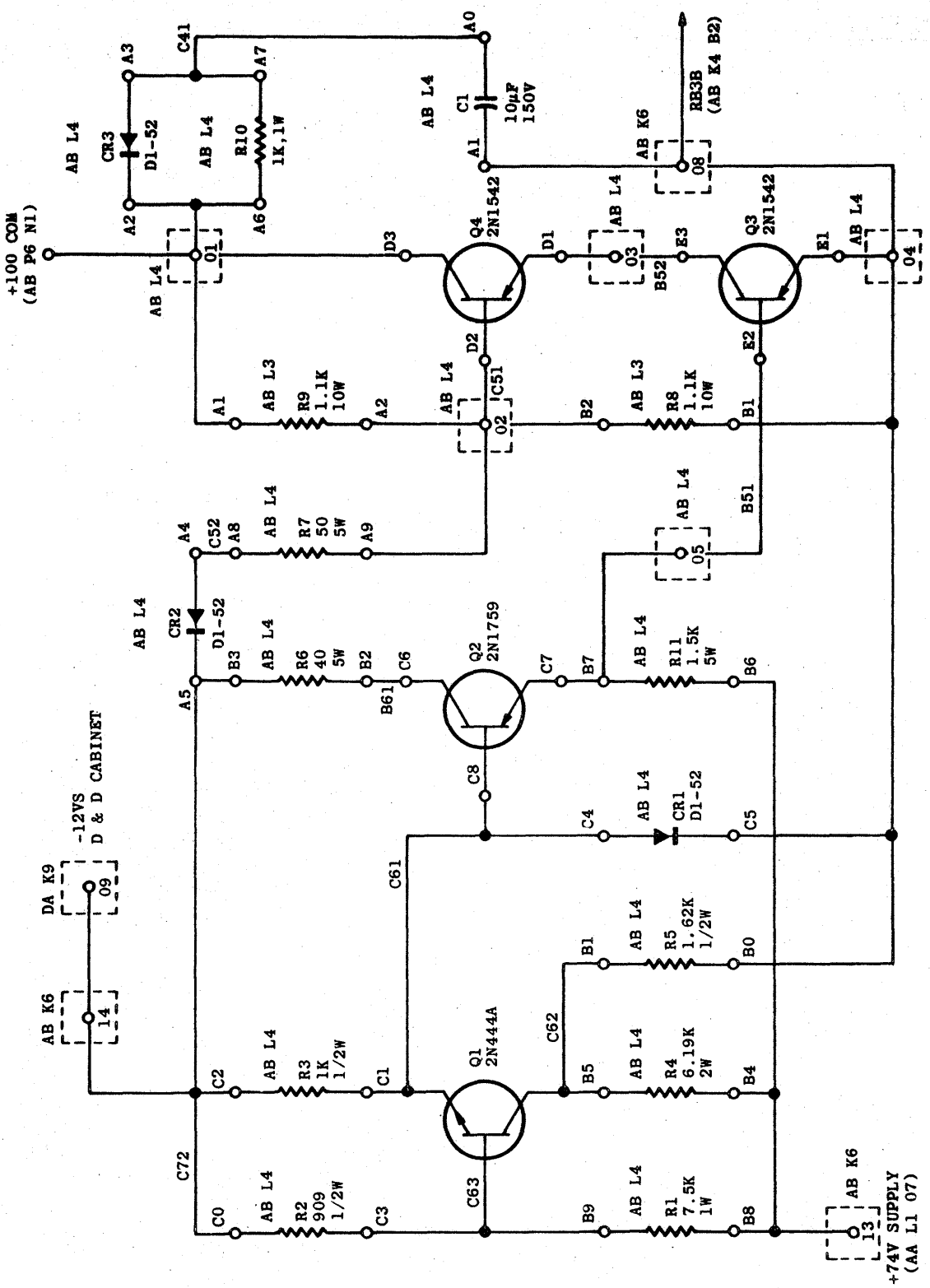


FIGURE 6.4-1. +100V ELECTRICAL SWITCH

6.5 AC METER

INTRODUCTION

The AC Meter indicates the voltage across any two legs of the input lines. It is controlled through a four position, two layer, rotary switch and provides monitoring of the three phase (3Ø) AC input.

There are four neon indicators located on the Power Supply cabinet, adjacent to the AC Meter. When lit, they indicate Power ON. There is one light for each of the following combinations: ØAB, ØBC, ØAC and ØAN.

CIRCUIT DESCRIPTION

Refer to Figure 6.5-1, AC Monitoring Circuit.

In the following explanation, only one position of the AC Meter switch and the accompanying light will be considered. The other three positions and circuits are similar.

With the rotary switch in the position shown in the figure, the AC Meter is monitoring the potential across phases A and N (neutral). The circuit runs from ØA to D1, O1 or the rotary switch, through the meter, O2, D2 to neutral: the meter will read the voltage between these two legs.

Also across these two legs is the neon and its resistor EA M7. When this light is ON, it indicates there is power across these two phases.

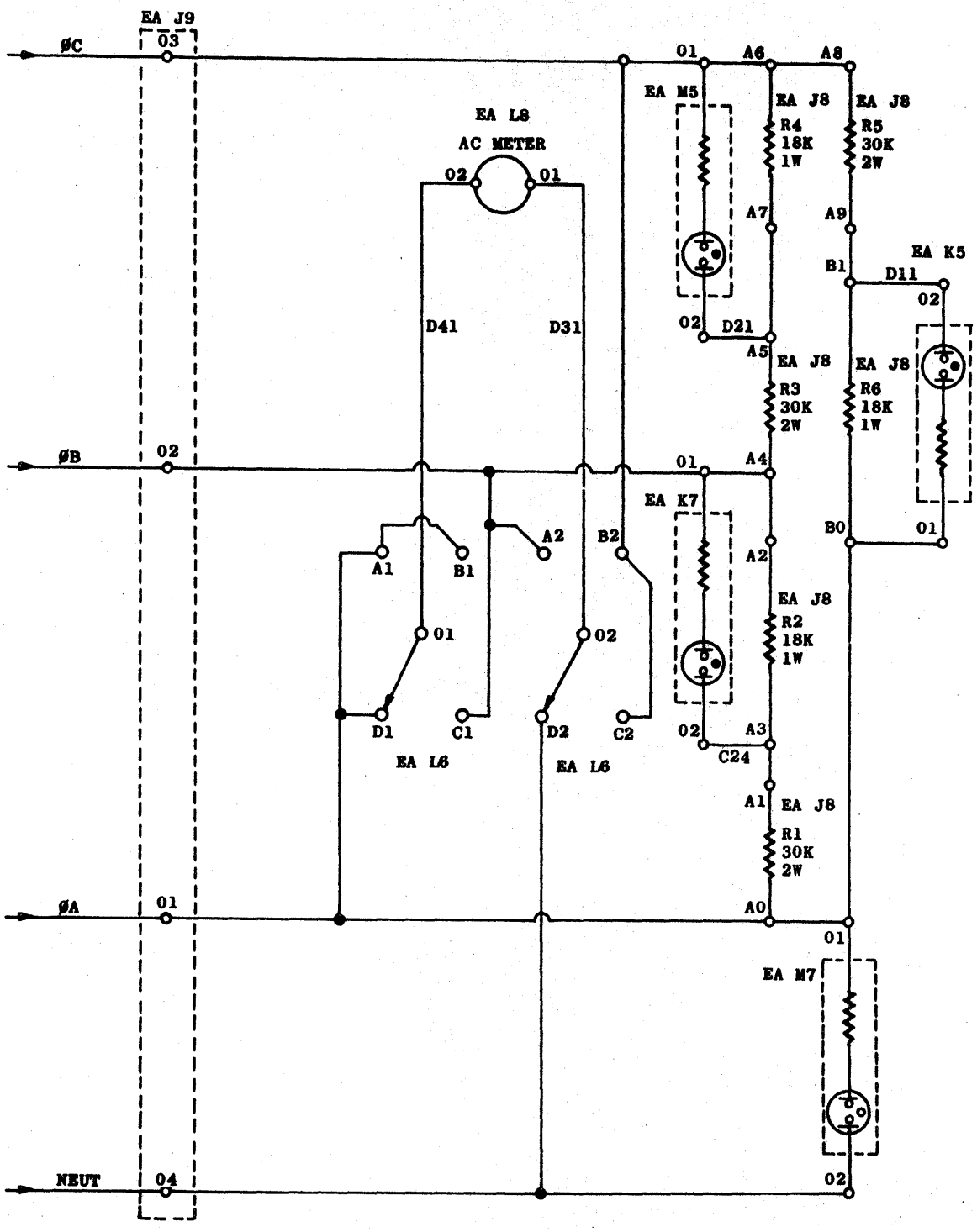


FIGURE 6.5-1. AC MONITORING CIRCUIT

6.6 ELAPSED TIME METER

INTRODUCTION

The Elapsed Time Meter indicates in hours the time that DC power is available to the system. This meter is located on the system Power Supply cabinet.

CIRCUIT OPERATION

Refer to Figure 6.6-1.

The meter is connected between ØA and Neutral of the input power line. The meter is protected by a 15 amp. circuit breaker, and is controlled through the 03, 04 contacts of power contactor K12. The contactor is energized and its contacts close any time power is applied to the system. Also shown in the figure is the distribution of the ØA and Neutral, for use with system fans and convenience outlets.

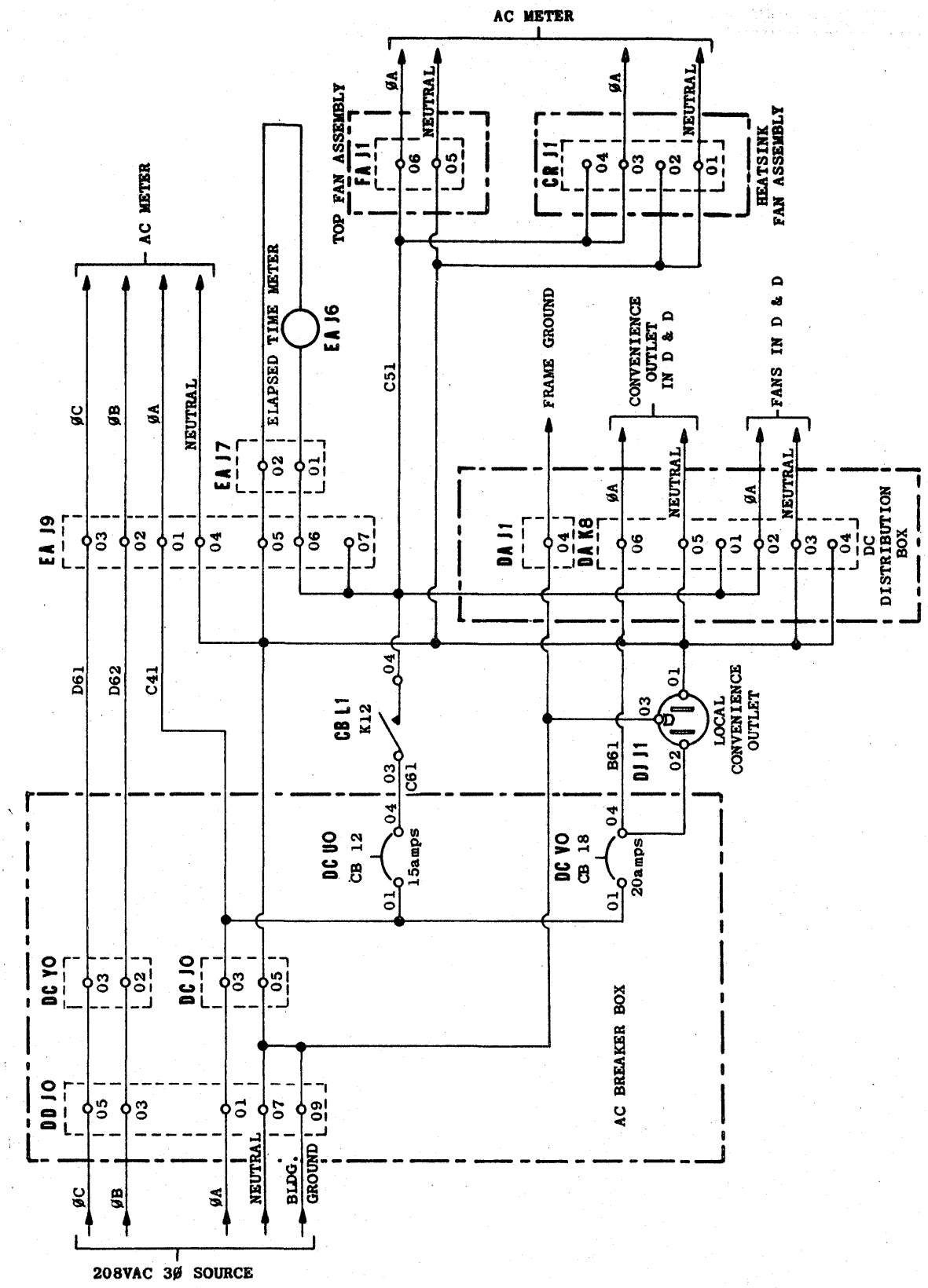


FIGURE 6.6-1. AC DISTRIBUTION, ØA

6.7 METER CHECK SWITCH

INTRODUCTION

The Meter Check switch is a five deck rotary wafer switch located on the Power Supply Indicator Panel. The Meter Check switch is used to individually monitor the voltage and amperage of the DC supplies.

The voltmeter is 1 millamperes movement and ranges 0-50V. The ammeter is 50 millivolt movement and ranges 0-5A, 0-10A, 0-50A, and 0-100A.

The Meter Check switch is used in conjunction with a voltmeter and an ammeter to select and monitor a given DC Supply.

CIRCUIT OPERATION

In the following discussion, only the monitoring of the +20V DC Supply will be explained, all others are similar.

For the output of the +20V Supply refer to Figure 6.2-3. At the terminal board ED K6 01 and ED K6 02 of the schematic, two lines go out to the Meter Panel. These lines are labeled EA LO 04 and EA LO 03 and continue in Figure 6.7-1.

In Figure 6.7-1 a table indicates that when monitoring the +20V Supply, the rotary switch will be in a position "M", and the voltmeter should read +20V, and the ammeter should be read on the 50 amp scale.

The +20V at EA LO 03 goes to pin M of Deck-1, through the swinger to pin A, through the voltmeter, the 50K resistor EA J2, pins M and A of Deck-5, pins A and M of Deck-2 to +20V common EA JO 11. This circuit monitors the +20V DC voltage.

The current is monitored through the following circuit: EA LO 03, pins M and A of Deck-3, the emitter, pin A and M of Deck-4 to EA LO 04 and back to the Power Supply.

CLOCKWISE FROM METER CHECK POSITION		
A	OFF	
B	-120V	5A
C	-24V	50A
D	+50V	50A
E	-19V/12V-1	100A
F	-19V/12V-2	100A
H	-19V/12V-3	100A
J	-19V/12V-4	100A
K	-19V/12V-5	100A
L	-19V/12V-6	100A
M	+20V	50A
N	+100V	5A
P	-100V	50A
R	-38V/30V	100A
S	-33V/25V	50A
T	+19V/12V	50A
U	+74V/60V	10A
V	METER CHECK	

NOTE:
1. SWITCH SHOWN IN "METER CHECK" POSITION.
2. D.C. VOLTMETER IS 1 MA. MOVEMENT.
3. D.C. AMMETER IS 50MV. MOVEMENT.
4. VOLTMETER RANGES: 0-50V, 0-150V.
5. AMMETER RANGES: 0-5A, 0-10A, 0-50A, 0-100A.

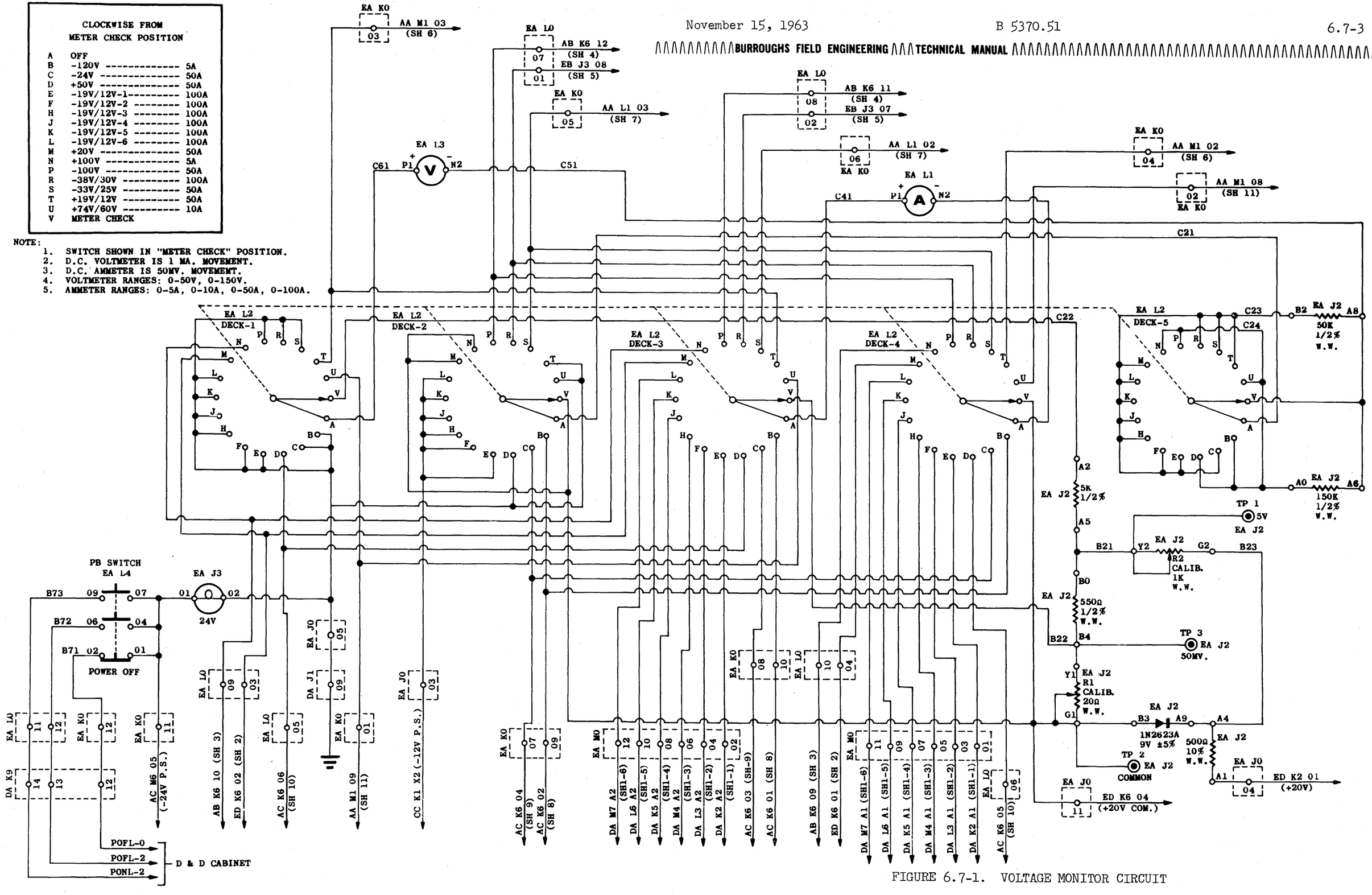


FIGURE 6.7-1. VOLTAGE MONITOR CIRCUIT

6.8 METER CHECK CIRCUIT

INTRODUCTION

The Meter Check Circuit provides a means by which the meters themselves can be checked.

Fixed potentials are supplies such that with the rotary switch in Meter Check position (V), the meters are examined for full deflection of their needles. These potentials are +5V and 50 milliamperes.

CIRCUIT OPERATION

Refer to Figure 6.7-1.

The voltmeter check is through the following circuit: The +20V Common (EA JO 11), Deck-2 pins A and V, Deck-5 pins A and V, the voltmeter, A and V Deck-1, 5K resistor R2, the 1K potentiometer to +20V. The potentiometer R2 is adjusted to establish +5V for the voltage check.

The ammeter check is from the +20V Common, pins A and V of Deck-4, ammeter, pins A and V of Deck-3 through the variable resistor R1 to +9V. This +9V is established from +20V Common, 9V zener diode, 500 ohm resistor to +20V. The 1K potentiometer R1 is used to adjust the ammeter current to 50 ma.

6.9 POWER OFF SWITCH

INTRODUCTION

The Power OFF pushbutton switch is used to shut down power and is located on the Indicator Panel of the Power Supply cabinet.

CIRCUIT DESCRIPTION

Refer to Figure 2.6-5.

There are three sets of contacts in the Power OFF switch. One set is in the HOLD circuit fo relay K13, the Main Power relay. The second pair picks relay K15, sending a Power OFF signal to the peripheral units. The third pair of contacts holds the drop relay K14 to provide the delay for the peripheral to shut down.

6.10 POWER CONTROL

GENERAL

Power for the B 5000 system is controlled through the use of DC relays and contactors. There are seven (7) DC relays which control the distribution of DC Power to the main units and the peripheral equipment. These relays provide DC Power to the system in the proper sequence when applying power, and provide the removing of DC Power in the proper order when removing power or during a power failure either within the Power Supply itself or a power failure within one of the units of the system. There are two (2) DC contactors which control the AC input to the system.

CONTACTOR OPERATION

Relay K11

Refer to Figure 6.2-4 for Relay K11.

This relay opens and closes the primary winding of Power Tranformers 1 and 4.

Relays K12

Refer to Figure 6.2-4 for Relay K12.

This relay opens and closes the primary windings of Transformers 2, 3 and 6. Relay K12 also controls the -12OV Supply, Cabinet Fans and the Elapsed Time Meter.

CONTROL RELAY OPERATION

Relay K13

Refer to Figure 2.6-5.

K13 controls the pick and drop of K11 and K12. It is the main Power ON relay, and is controlled through the Power ON and Power OFF buttons, the overvoltage, excess current and overheat sensing.

Relay K14

K14 allows 150 ms delay during Power OFF to insure that the peripheral units have time to function. K14 is a slow release relay.

Relay K15

Sends Power ON and Power OFF signals to the peripheral equipment.

Relay K17

Inhibit Interlock to peripheral units and -24VB to DC Indicators.

Relay K18

Removes Lockout ground to Core Memories and 1 MC clock in Central Control.

Relay K19

Decoding matrix inhibit, +20V switch control and Core Memory Supply delay.

Relay K20

Display and Distribution cabinet cover interlock.

The following list explains the use of the various contacts of the control relay.

RELAY CONTACT FUNCTION

RELAYS	PIN NOS.	FUNCTION
K13	7 & 9	K13 hold circuit
	8 & 10	Pick K11 and K12
	14 & 16	Pick K18
K14	8 & 10	150 ms slow release
	7 & 9	Power ON to peripheral units
K15	8 & 10	Hold circuit to insure K15 does not drop prior to K14
	7 & 9	Power OFF to peripheral
	5 & 7	Power ON to peripheral
K17	5 & 7	Inhibit power to peripheral units
	9 & 11	Ground interlock to peripheral
	8 & 10	-24VB for DC Indicators
K18	5 & 7	Remove Lockout ground to Core Memories and 1 MC clock
	8 & 10	Discharge K18 slow pull capacitor
	8 & 6	Charge K18 delay capacitor providing 500 ms delay

RELAY CONTACT FUNCTION (Continued)

RELAYS	PIN NOS.	FUNCTION
K19	7 & 9	Control to +20V switch
	11 & 13	False to inhibit (decoding Matrix)
	14 & 16	40 ms delay
	13 & 15	True to inhibit (decoding Matrix)
	8 & 10	A delay allowing Core Memory Supplies to start down first
K20	4 & 5	-120V to neon displays
	7 & 8	-100V to neon displays

6.11 POWER ON

Refer to Figure 2.6-5.

The main wall breaker supplies -24V relay control voltage, and 115V AC for convenience outlets through the system.

With the depression of the Power ON button S2 (A5), Relay K14 (6B) energizes, sending through its contacts 7 and 9 a true (Power ON signal) to the peripheral units. Contacts 8 and 10 charge the two 50 μfd capacitors which effect the slow release of K14. The slow release, 150 ms, insures that a signal of sufficient length has been generated independent of the length of time the Power ON button is depressed.

The Power ON button completes the following circuit for the pick of Relay K13, the Main Power Control relay: -24VA (5A), S2 switch, pins 1 and 4 of relay K13 (5C), K13 coil and the saturated transistor Q1 to ground. With the pick of K13 contacts 8 and 10 pick the two relay contactors K11 and K12. These relays close the primary windings of the Power Transformers. (Reference Drawing D119184 48 - Supplying DC Power.)

Contacts 7 and 9 of K13 provide the following hold circuit for K13: -24VA (4B), the three Power OFF switches in series, the contacts 7 and 9, the coil, pins 1 and 4 of K13 and the saturated transistor Q1 (5D).

This relay remains energized during normal operation. The contacts 14 and 16 of K13 close the pick path for K18 (6D). However, the K18 contacts 6 and 8 allow the charge of the 325 μfd capacitor which delays the pick of K18 for 500 ms. This delay is necessary to provide time for the DC Supplies to settle down.

With K14 picked and dropped, turning on peripheral units, K13 picked and held, giving DC Power, K18 to inhibit undervoltage sensing during Power ON and all power interlocks removed, the system supply is in a normal operation status.

6.12 POWER OFF

Refer to Figure 2.6-5.

The depression of the Power OFF button either on the Display and Distribution cabinet, the Power Supply cabinet, or the System Console, will open the HOLD circuit for K13. With the drop of K13, K11 and K12 will both drop, opening the primary windings of the power transformers removing DC Power. The -24VA and 115V AC remain on the system.

6.13 UNDERVOLTAGE INHIBIT

Refer to Figure 2.6-5.

Prior to the depression of the Power ON button, but with the relay voltage available (-24VA), relay K19 will be energized through the normally closed contacts 7 and 5 of relay K18.

With the Power ON button activated, K18 picks dropping K19. However, K18 is a slow pick relay (500 ms), and during this time a true level (-12V), through contacts 13 and 15 of K19, is sent to the undervoltage sensing during the time required for the DC Supplies to come up and settle down. Upon the completion of the 500 ms delay, K18 picks. K19 drops and the line to the inhibit circuitry goes false through the transferred contacts 11 and 13 of K19. The -12V Inhibit Level is sent to the D & D sensing panel to inhibit any sensing during the Power ON period.

6.14 PRE-STOP ($\overline{\text{PGDL}}$) 1 MEGACYCLE CLOCK IN CENTRAL CONTROL

Refer to Figure 2.6-5.

This control line is used to inhibit the 1 MC Clock in Central Control in the event that the Main System Power is not normal. For example; Power failure, Power shut-down, or DC Lockout.

6.15 +20V SWITCH CONTROL LEVEL

Refer to Figure 2.6-5.

This control line in normal operation is true and provides the ON condition for the +20V electrical switch in the common line of the +20V Power Supply. It is turned ON or OFF through contacts of K19. Relay K19 is picked by the drop of K18, which is dropped by the drop of K13. Relay K13 is de-energized by any Power OFF or Power failure condition. Through the transferred contacts 7 and 9 of K19, the +20V switch opens the +20V Supply. This supply is instrumental in initiating and sequencing down of all DC system Power except the -20VA.

6.16 -24 VOLT B

Refer to Figure 2.6-5.

The -24VB is DC indicator voltage and is applied through contacts 8 and 10 of relay K17. K17 is picked with the -12V regulated Supply. The -24VB differs from the -24VA only in that it is controlled through K17, insuring that DC Power is on the system prior to the indicators being lit. Were -24VA used on the DC indicators, false indications would occur.

As -24VA is available with the activation of the circuit breaker, it is independent of the DC Supplies.

6.17 POWER INTERLOCK (PERIPHERAL UNITS)

Refer to Figure 2.6-5.

There are two control lines connected with this function, one labeled ON the other OFF. With the Power ON button activated, relay K14, (slow release 150 ms) is energized. The contacts 8 and 10 provide a charge path for the two 50 μfd capacitors across the coil. These capacitors effect the slow release of K14. The contacts 7 and 9 transfer and provide a true, out to the peripheral units through the contacts 7 and 5 of K15. K15 is not picked at this time.

The purpose of the slow release of K14 is to insure that a peripheral ON or OFF signal is of sufficient duration for the peripheral unit to activate, independent of the time the button is manually activated.

During a Power OFF operation, relay K15 is energized supplying a true through the transferred contacts 8 and 10, holding contacts for K15 and 7 and 9 of K15 to the peripheral units as a Power OFF signal. Relay K14 is picked also at this time to supply the delayed release. However, there will be no peripheral ON signal due to the transferred contacts 7 and 9 of K15.

In the event of a Power failure, K17 is de-energized as soon as the -12V regulated Supply is lost. This is lost immediately following the +20V Supply. which drops with the pick of K19 through the +20V electrical switch. With the drop of K17, the Interlock Line is grounded through the transferred contacts 9 and 11 of K17.

6.18 COVER INTERLOCK

Refer to Figure 2.6-5.

This Interlock insures that the neon indicators within the Display and Distribution Cabinet are inoperative any time the machine covers are in place. Power is supplied to the neon indicators through this Interlock switch and the contacts of K20 any time the covers are removed.

With the covers in place on the Display and Distribution cabinet, K20 is de-energized and the neon displays are inoperative.

With the covers removed, K20 picks and contacts 7 & 8, and 4 & 5 supply Power to the indicators.

6.19 VOLTAGE SENSING

GENERAL DESCRIPTION

The B 5000 system has facilities for sensing over and under voltage conditions for the -12V, -4.5V, -1.2V, +20V and +100V. In addition, excess current from the -12V Regulator and overheat conditions are sensed. These conditions will shut down the Power Supply. The +20V and +100V are sensed in the Display and Distribution cabinet. The remainder of the voltages and excess current and overheat conditions are sensed in the Display and Distribution, but they are also sensed by cabinet.

Using this method, a visual indication can be presented. For example: the voltage that failed, over or under voltage, and the cabinet where the failure occurred. Overheat is indicated by the cabinet causing the failure. Excess current is indicated by cabinet, -12V Indicator ON, and EC Indicator ON. Only the -12V regulator Supply is sensed for excess current.

CIRCUIT DESCRIPTION

Figure 6.19-1 shows the sensing for Processors A and B. It also includes the gating for other sensing circuits. The following theory will discuss only the -12V sensing for Processor A. All other sensing is accomplished in a similar manner.

CABINET FAIL INDICATOR

Each cabinet in the B 5000 system will contain a Voltage Regulator Power Unit which will develop -12V, -4.5V and -1.2V. The outputs of the regulator are monitored in the Display and Distribution cabinet for overvoltage and undervoltage conditions.

The Voltage Sensing Circuit (VSC) has an input from the -12V of Processor A at pin B4. Pins J6 and E1 receive a constant reference voltage of -4.5V from the Voltage Reference Package (RV). The reference voltages are used to sense for a ±10 percent change in the -12V Supply.

Assuming the -12V Supply developed an undervoltage condition, the output of the Voltage Sensing Package, Pin K1, would go false indicating a FAIL condition. The FAIL condition is sensed at the AND gate AE A9 L1, pin D1. The output of the AND gate, pin A1, will then become false and pin B9 of AE A9 A7 will become false. The output of the switch, pin C9 will become true. The output of the AND gate AE B0 L6 will become true at pin L6, switch AF B1 A2 will have a false output at C0. The false at C0 is sensed at B3 of the Relay Package. The relay will now pick (see inset schematic of the Relay Package in Figure 6.19-1), supplying a ground return for the Processor A.

The -24V applied to the other coil is a HOLD circuit until the CLEAR button is depressed. The -24V is from the Main Power Supply and is always present unless the Main Power switch to the Power Supply is OFF. Due to this condition, even

though the Power Supply shuts down, a visual indication of the failure will exist until it is cleared.

VOLTAGE INDICATOR

The false output of the Voltage Sensing Circuit (VSC) at pin K1 feeds AND gate AE B9 Y2, pin P2, which in turn will make the output at N2 false. This output is sensed at AE B9 Y3, Pin X3. The output of AE B9 Y3, pin Y3, becomes false, which in turn makes switch AF B9 Y7 cut OFF, making its output at R5 true. The true into AND gate AF B1 Y2, pin 2, will make its output true, which is then switched by switch AF B1 N7. The false from switch AF B1 N7 picks the relay in package AF B2 N7 which turns ON the -12V Indicator.

UNDER VOLTAGE FAIL INDICATOR

The false output of AND gate AE B9 Y2, pin N2, also feeds AND gate AF B0 Y1, pin U1. The output pin Y1 of AF B0 N7, turns switch AF B0 N7 OFF. The true output of switch AF B0 N7, pin W5, makes the output of AND gate AF B0 Y2, pin N2, true. The true is inverted by switch AF B0 N7. Its output at pin S7 picks the relay in Relay Package AF B2 N2 which turns ON the -12V Under Voltage Indicator.

POWER OFF CIRCUIT

The true output of switch AE A9 A7, pin C9, feeds AND gate AE B0 L6, pin K6, and AND gate AF A0 Y7, pin X5. AND gate AF A0 Y5, pin Y5, will have a true output feeding pin P6 of AF A0 Y6, the Power OFF OR gate. The true output causes the output of switch AF B1 A7, pin J5, to become false. The false output is transmitted to the control transistor of K13 in the Power Control circuitry. This transistor will cut OFF, breaking the K13 coil circuit. K13 will drop out, dropping primary power to the Power Supply. The primaries of the input transformers have two contactors in the AC line; K11 and K12, which are dropped by K13.

INHIBIT OPERATION

The Power Supply Inhibit Input to switch AE B9 A7, pin B9, controls the sensing circuits for Power ON operation. The input from Power Supply will be true for 25 ms when Power is applied. This will be switched to a false switch AE B9 A7, which will inhibit any type of sensing until the Power Supply voltages are settled down.

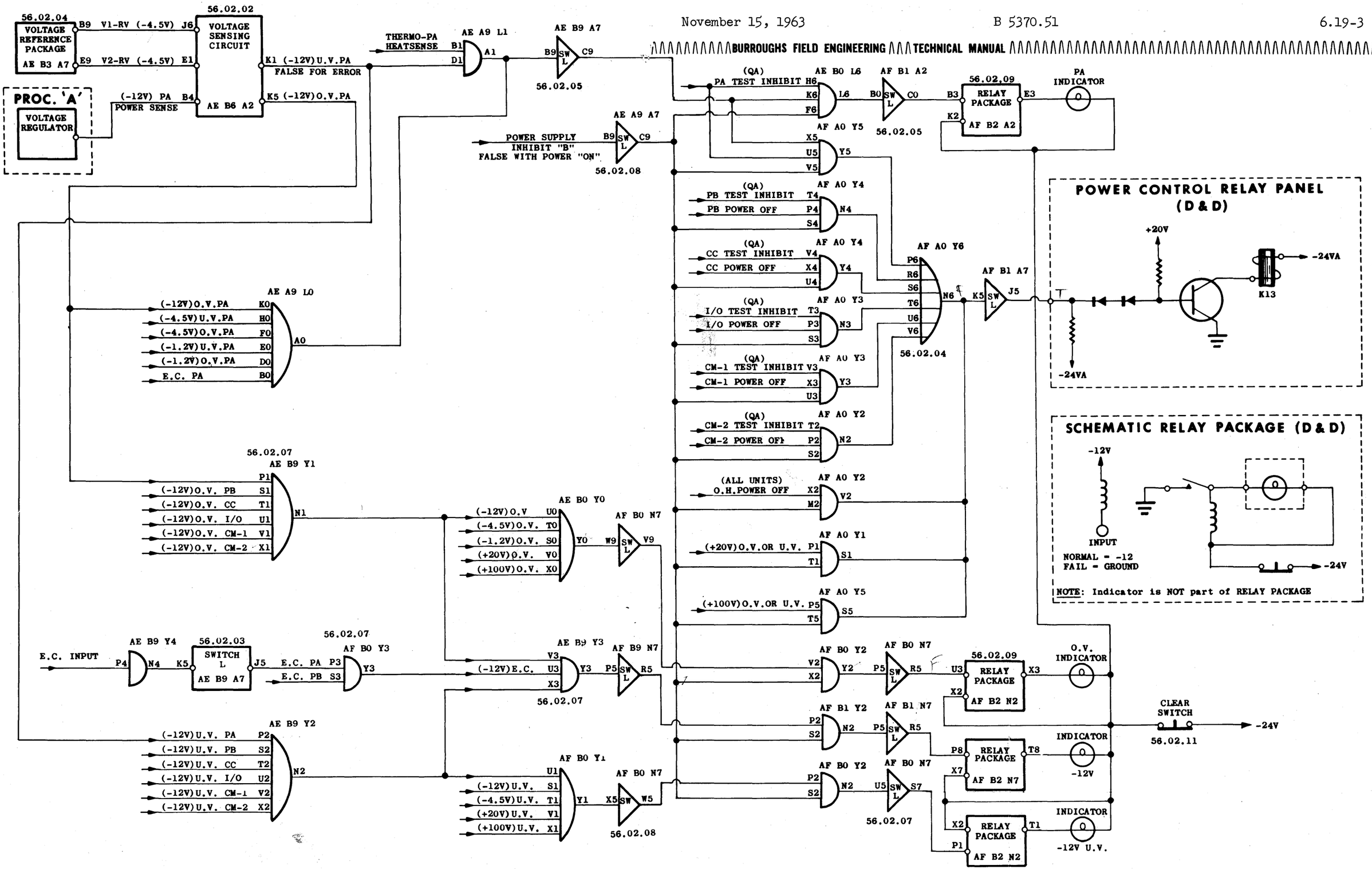


FIGURE 6.19-1. VOLTAGE SENSING

6.20 VOLTAGE SENSING PACKAGE

INTRODUCTION

There are twenty Voltage Sensing Packages such as shown in Figure 6.20-1. One circuit is used for each of the three separate voltages (-1.2V, -4.5, and -12V) in the B 5000 Power Regulator Unit. There are six power regulator units in a maximum system. A total of eighteen voltage sensing circuits are used for these voltages. The +20V and the +100V are also sensed for undervoltage and overvoltage requiring two additional sensing circuits for a total of twenty. These packages are located in the Display and Distribution Cabinet.

The Voltage Sensing Package is a circuit providing two separate outputs. An output when an overvoltage is sensed and an output when an undervoltage is sensed. Both outputs in normal operation (neither an overvoltage or undervoltage condition exists) have a negative output (true). With the detection of an overvoltage, output 1 becomes false. With an undervoltage detection, output 2 becomes false. At no time are both outputs false at the same time.

Figure 6.20-1 shows multiple inputs to the base of transistor Q2 and four separate collector resistors. Any one, or any combination of these four resistors is used to supply the collector voltage for any chosen voltage to be sensed. The input to the Q1 base is also determined by the voltage sensing.

For the following explanation, the sensing package used with the -1.2V regulated Supply will be used.

CIRCUIT DESCRIPTION

When used to sense the -1.2V regulated Supply, the input IN-RV is at -9V obtained from the voltage reference package. Inputs IN-A, IN-B, and IN-C are not used. IN-D is -1.2V from the -1.2V regulator output. With the base and collector voltage set, transistor Q1 is in conduction, and the junction of the Q1 collector and the Q2 base is approximately -4.5V. This potential keeps Q2 in conduction and the emitter at approximately -4.5V. With the Q3 emitter at -4.5V and Q3 base (IN V2) at -4.5V from the voltage reference package, transistor Q3 is in conduction. Transistors Q2 and Q3 comprise a difference amplifier whose emitters are at -4.5V.

Transistors Q4 and Q7 make up an amplifier and output stage for the sensing of overvoltage and are cut off. With Q7 OFF, the output 1 is true. Transistors Q5 and Q6 make up the final output for undervoltage sensing and also are cut off. With Q6 OFF, output 2 is true.

This is the normal state with Power Up and all conditions normal.

Should an overvoltage be sensed and the base of Q1 driven more negative, Q1 would go toward saturation and its collector increase in a positive direction. This positive switch would be felt on the base of Q2 and emitters of Q3 and Q5. Because Q2 and Q3 form a difference amplifier and work opposite and equal to each other, (Q2 increases conduction when Q3 decreases conduction), their emitter voltage does not change. However, the increased conduction of Q3 supplies the

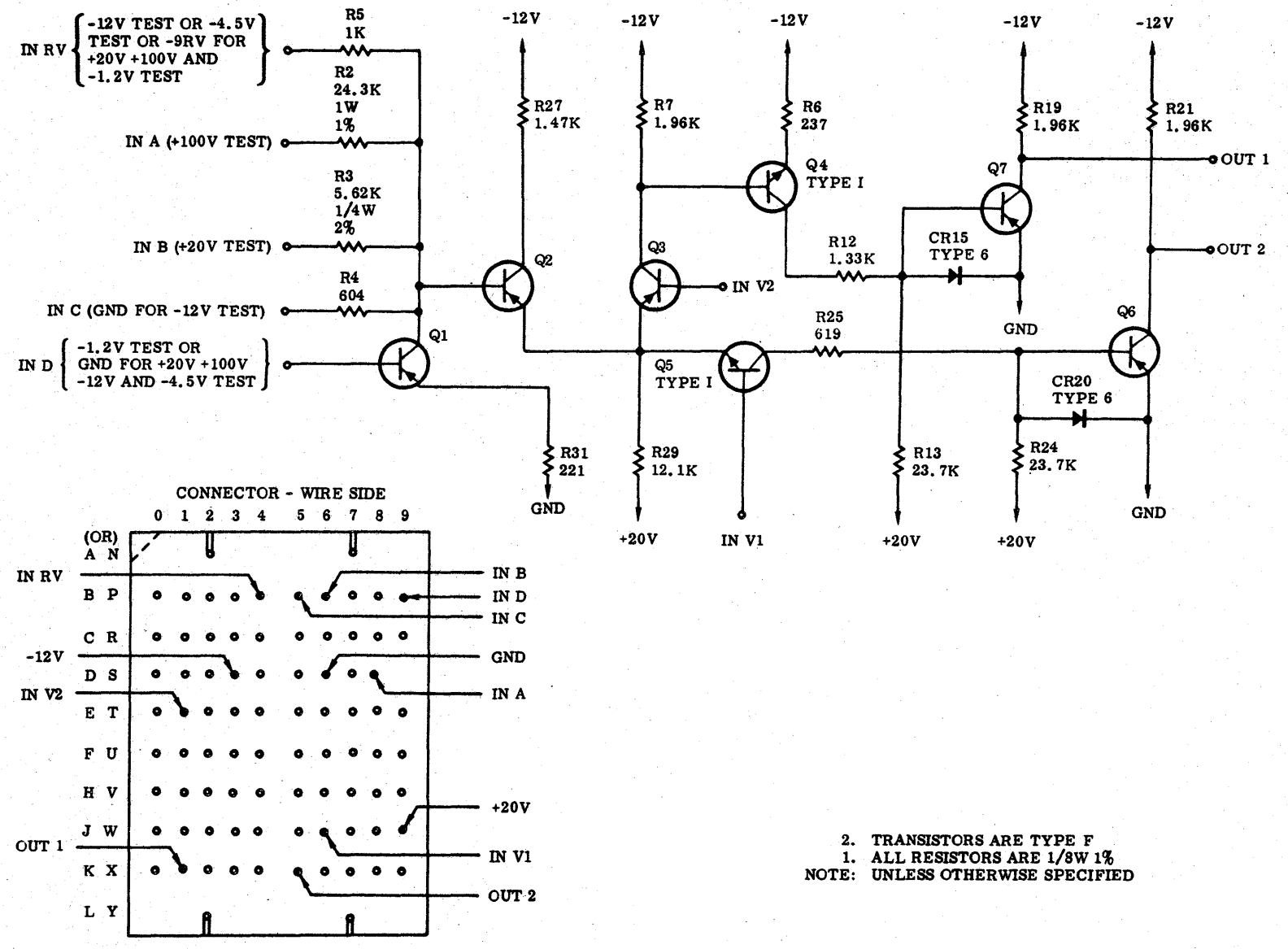


FIGURE 6.20-1. VOLTAGE SENSING CIRCUIT

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base drive for Q4 taking it out of cutoff and into conduction. Q4 in conduction turns on Q7 giving a false out. Under the conditions of overvoltage, the emitter base junction of Q5 is reversed biased and the output of Q6 remains true.

On an undervoltage condition, the swing on the Q5 emitter would be negative and with its base at -4.5V from the reference voltage package, Q5 would conduct, driving Q6 ON and the output false.

The diodes, CR20 and CR15, are ground clamps and prevent excessive positive voltage on the base of Q6 and Q7 when in cut off.

6.21 VOLTAGE REFERENCE PACKAGE

INTRODUCTION

The Voltage Reference Package is made up of a circuit that develops three separate voltages for use in the voltage sensing circuits. These three voltages, -9V and two separate voltages of -4.5V each, are used as reference voltages in sensing for overvoltage and undervoltage.

CIRCUIT DESCRIPTION

Refer to Figure 6.21-1.

In the quiescent condition, the transistors Q1, Q2 and Q3 are all in conduction.

Transistor Q2 is supplied base drive current through the bias circuit of R8, CR7 and Zener diode (CR27 (9V). This network establishes -9.2V on the base of Q2. Through the emitter follower action of Q2 and its voltage divider network, R3 and the variable resistor R28, base drive current is supplied to turn on transistor Q3. With Q3 in conduction, the voltage divider consisting of resistors R20, R22 and R21 provides a reference voltage of -9V at the terminal "output -9 RV", for use in the voltage sensing package.

The two -4.5V reference voltages at the output terminals labeled "OUT V1" and "OUT V2", are taken from the emitter of transistor Q1. The base voltage of approximately -3V is taken from the voltage divider consisting of resistors R22 and R21. With the emitter tied to a positive potential, Q1 is turned on and through the network of R23, Q1, CR25 and R24 the two outputs are obtained. The output at V1 will be -4.5V and V2, due to the diodes CR25 will be somewhat less negative, approximately -4.2V.

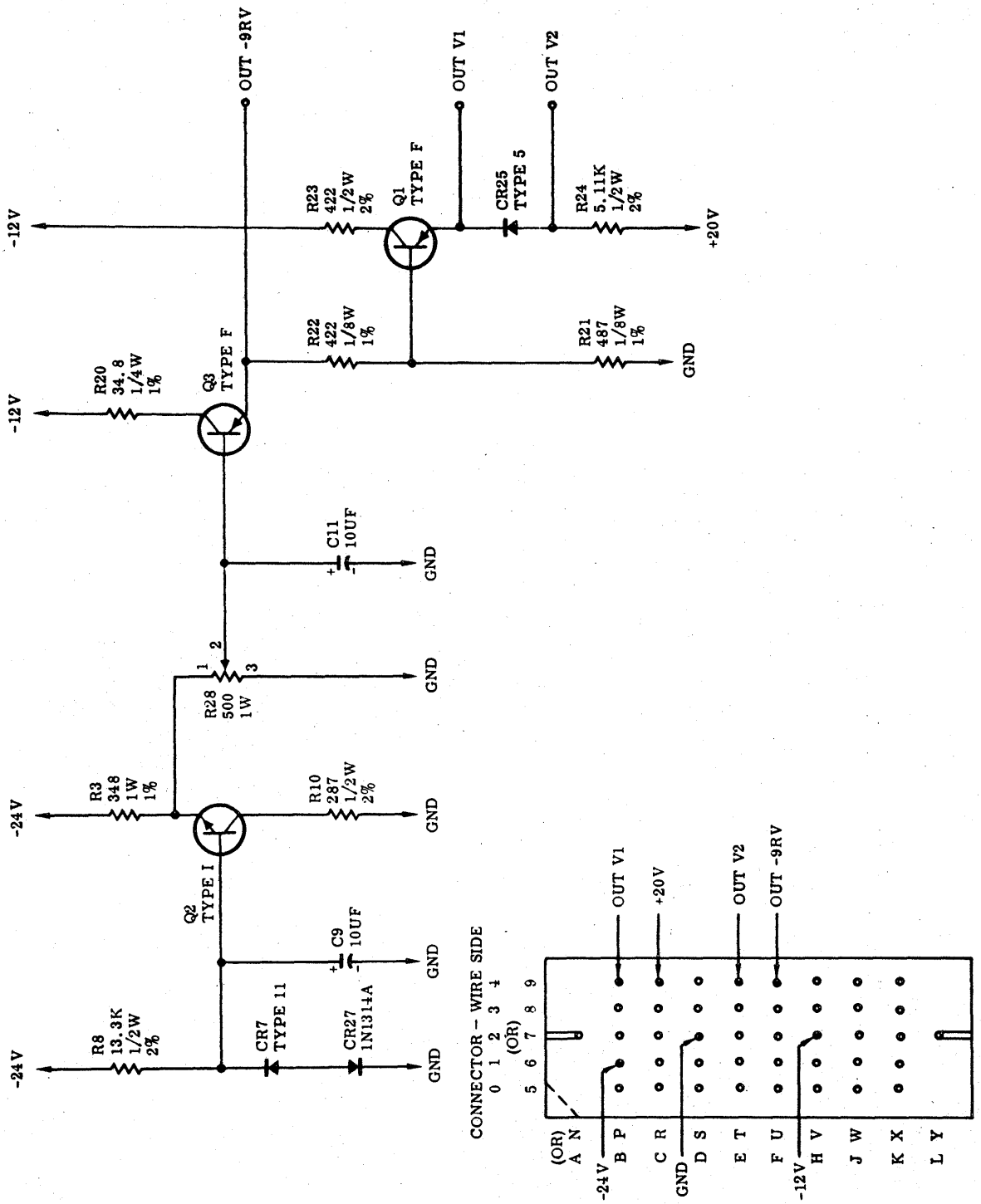


FIGURE 6.21-1. VOLTAGE REFERENCE CIRCUIT

6.22 -12V REGULATOR

GENERAL DESCRIPTION

The -12V Regulator is of the standard series type with the output being sensed through a difference amplifier. The difference is amplified, inverted, and applied to the output as a corrective signal.

The -12V Regulator provides circuitry for the detection of excess current being drawn from the supply. If excess current is drawn from the supply, the Main Power source is shut down automatically through a sensing circuit.

A -12V regulator is located in each of the major units except the Display and Distribution cabinet.

CIRCUIT DESCRIPTION

Refer to Figure 6.22-1.

Transistor Q5 detects variations in the output of the regulator through the voltage divider R19, R36 and R17.

With the base of Q4 at a constant potential, developed by R22 and the Zener diode CR23, a constant potential will be developed at the emitters of both Q4 and Q5 through the common load resistor R20. Therefore, the emitter of Q5 of the difference amplifier is used as a reference against which the fluctuations of the base are compared.

The inverted difference is fed through diodes CR12 and CR10 to the base of the emitter follower transistor Q2 from the emitter to the two following stages if emitter followers, through the parallel regulator stages to the output.

Transistor Q3, whose base is held at a constant potential by the voltage divider R6, R9 and the emitter tied to ground, provides a constant current source to increase the base drive current to transistor Q2.

Transistor Q1 is biased through the variable resistor R35, R30 and R31. The variable resistor R35 is adjusted such that transistor Q1 is cut OFF. If the load on the regulator draws excess current, the emitter of the NPN transistor Q1 will go negative and cause conduction which provides a true or negative output under a fail condition. Under normal operation and with Q1 just cut OFF, the output is false, or near ground.

THE -4.5 VOLT REGULATOR

Refer to Figure 6.22-2.

The -4.5V Regulator provides regulation for the -4.5V from the source portion of the regulator. It also regulates the incoming current through the sink portion of the regulator.

The regulator, at times, supplies Power to the circuit loads that terminate at a voltage more negative than -4.5V. At these times, current will flow in the reverse direction, or toward the positive potential. In this case, the -4.5V. This negative source is flowing into the regulator through the -4.5V normal output terminal, thereby overriding the -4.5V source. With this condition existing, the incoming current must also be regulated, as it will vary the -4.5V output. This is done in the sink regulator section.

CIRCUIT DESCRIPTION

All transistors in this regulator are operating in conduction. They are biased in such a way as to handle both positive and negative excursions of the -4.5V output.

QUIESCENT STATE

Transistor Q1 is conducting through the circuit -12V, R5, its base emitter junction, and resistor R6, to +20V. From the emitter of Q1, a base drive current is supplied to the base of the emitter follower which controls the voltage regulator stages. These stages supply the -4.5V source output.

The sink regulator portion is controlled by Q5. Q5 is supplied its base drive by Q3 of the difference amplifier. Q5 drives the first stage of the sink supply which in turn drives the 5 emitter followers.

CIRCUIT OPERATION

For the following analysis, the -4.5V output will be assumed to have changed in the positive direction, approximately 0.5V. The positive change is felt on the base of Q2. Q2 and Q3 form a difference amplifier. The base of Q3 is held constant by the circuit consisting of Q4, R27 and CR22. R27 is adjusted for the desired output of -4.5V. The difference amplifier will sense any variation and regulate accordingly. The positive change felt on the base of Q2 will cause Q2 to conduct less. The emitter of Q2 will become more negative, supplying more base drive for Q1. The emitter of Q1 will supply more base drive to the emitter follower, which in turn will drive the regulator source supply transistors harder, causing the output to become more negative. The sink regulators controlled by the positive change felt on the collector of Q5 and a positive change also felt on its base due to the increased conduction of Q3. The emitter of Q5 will become more positive. The positive is felt on the base of the emitter follower controlling the sink regulator. The sink regulator will decrease in conduction.

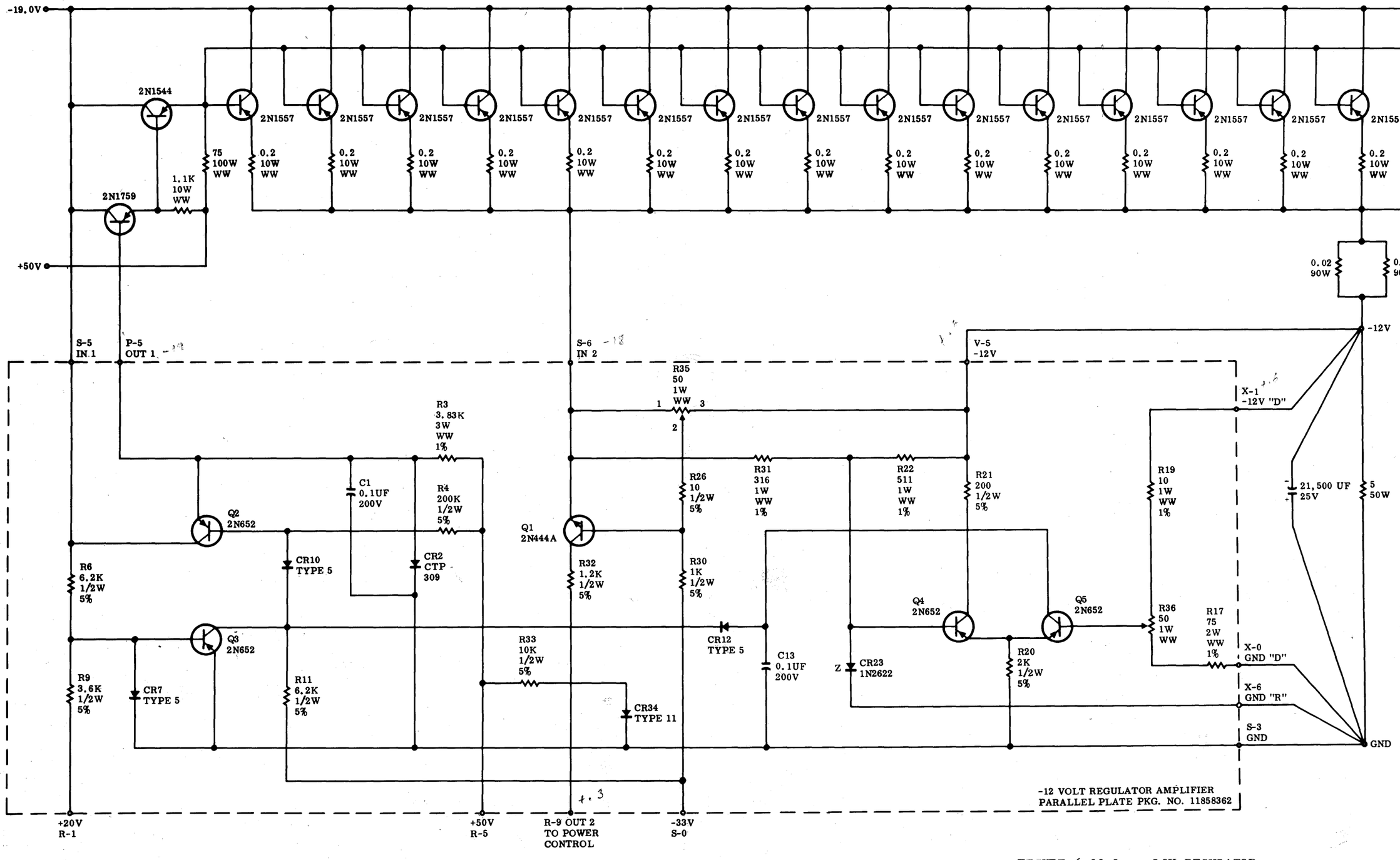


FIGURE 6.22-1. -12V REGULATOR

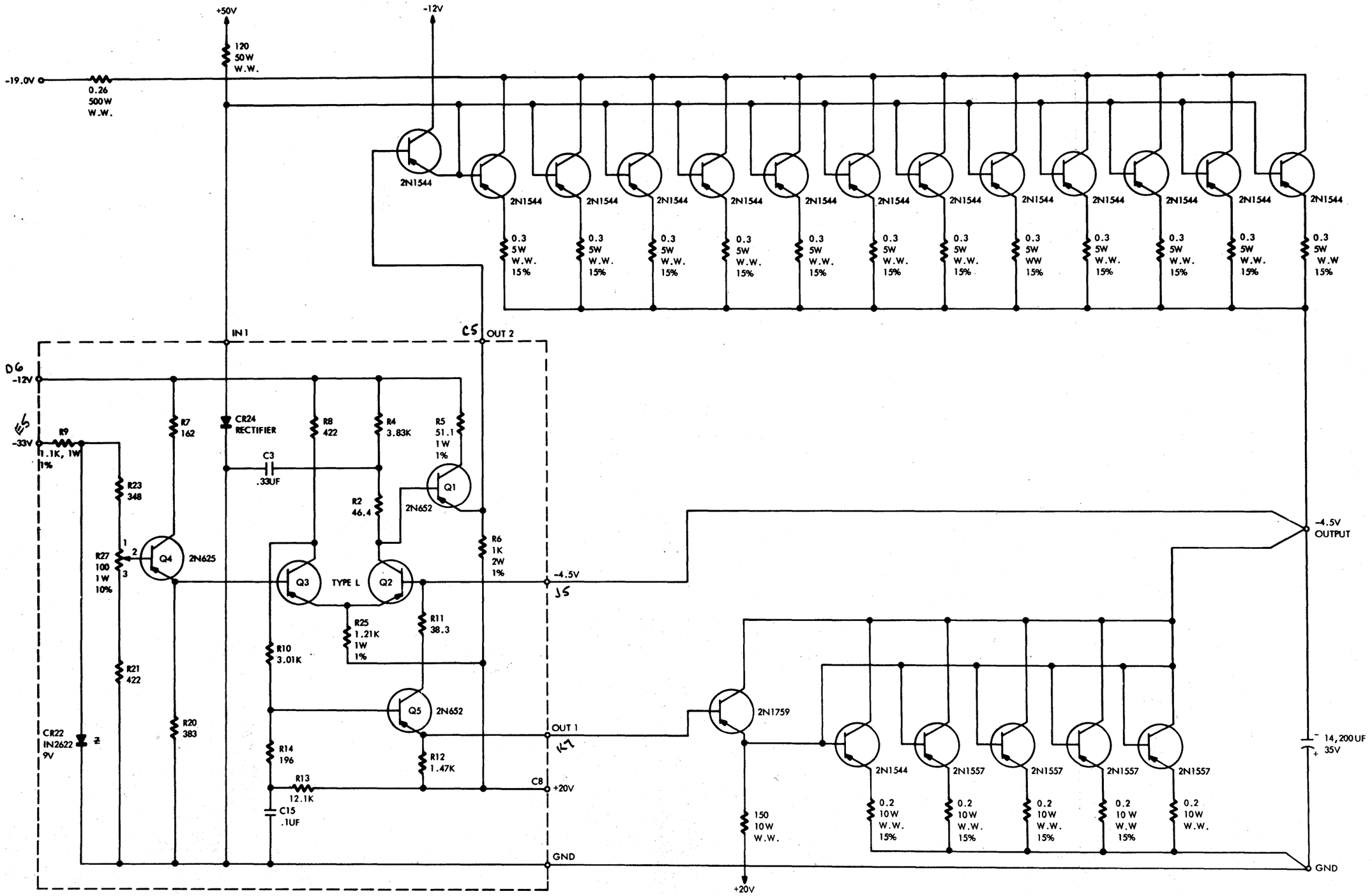


FIGURE 6.22-2. -4.5 REGULATOR

THE -1.2 VOLT REGULATOR

Refer to Figure 6.22-3.

The purpose of a voltage regulator is to maintain a given DC voltage output despite normal changes in input voltage to the Power Supply, or normal load changes. A regulator contains essentially, a reference voltage against which the output voltage is compared, a difference amplifier for comparison, a buffer and a variable resistor (transistor stage, or stages) in series with the load. This transistor resistance is controlled by a sensing circuit which monitors the regulated output voltage.

The negative 10.8V is dropped across the regulator and -1.2V is dropped across the load.

CIRCUIT DESCRIPTION

In the quiescent state, all transistors Q1 through Q7, are biased into conduction. Q2 and Q3 make up a difference amplifier. Q1 is a constant current source. Transistor Q4 is a voltage amplifier. Q5 is a driver. Q6 and Q7 are the variable resistance regulators.

Zener diode CR2 develops a constant voltage on the base of transistor Q1 (9.0V). Resistor R1 is used to drop the remaining input voltage. With the collector and emitter of Q1 both tied to a fixed potential, Q1 is a constant current source to supply drive current to the base of Q2 through the variable resistor R27. This allows the emitter resistor R20 to develop -1.2V on the emitters of Q1 and Q3. Any variation in the output, either in the positive or negative direction, is felt on the base of Q3 which causes either an increase or decrease in conduction of Q3.

This difference in potential is amplified and inverted through Q3 and Q4, and applied through the emitter follower Q5 to the bases of the two paralleled transistors Q6 and Q7. Transistors Q6 and Q7 are power transistors. Varying their resistance, regulates the output. Should the -1.2V output go positive, this rise should be reflected on the base of Q3, causing Q3 to increase conduction. This increased conduction would develop a more negative potential on the base of Q4. This negative base drive on Q4 increases the conduction of Q4, forcing the collector to rise in a positive direction. A positive signal on the base of Q5 drives the emitter in a positive direction, providing less base drive to Q6 and Q7, thus driving their collectors and the output negative (back to -1.2V).

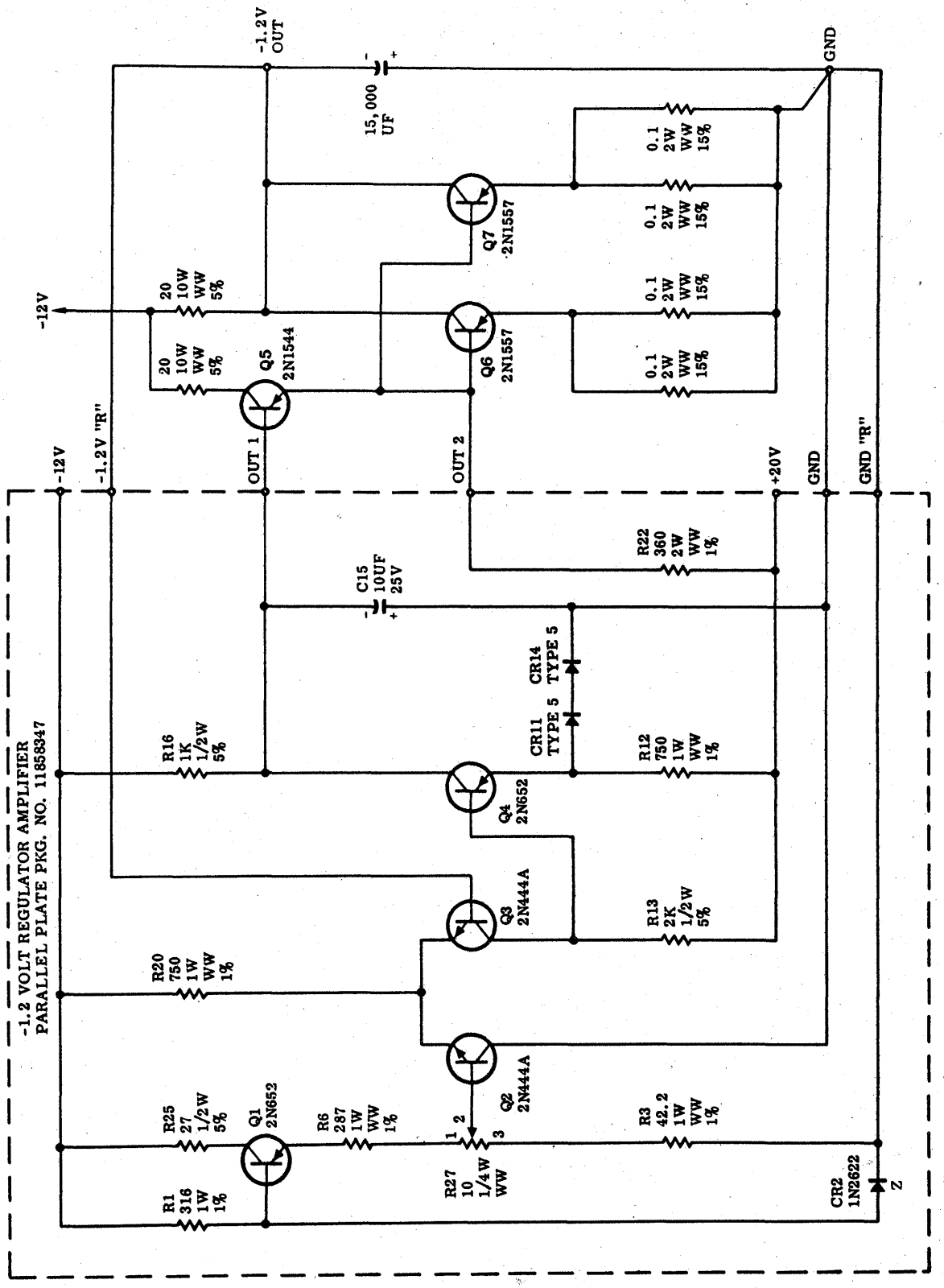


FIGURE 6.22-3. -1.2V REGULATOR

6.23 B 5000 PARALLEL PLATE PACKAGES

INTRODUCTION

The basic operations of the standard Parallel Plate Packages used in the B 5000 system are described in this section. Included in this description is an explanation of the characteristics and use of these packages in the B 5000 system.

The description by no means exhausts the subject. It is only meant to give anyone who might work with these packages a general idea of their operation and use in the B 5000 system.

The following is a table of the B 5000 Parallel Plate Packages described in this text.

TABLE 6.23-1. PARALLEL PLATE PACKAGES

DESCRIPTION	SCHEMATIC NO.
SWITCH I	C-80661
FLIP-FLOP 20-70	C-1182424
B.O. & LINE DRIVER	C-1182507
CLOCK OSCILLATOR & SQUARE AMP.	C-1182681
MULTI 5.5μs	C-11833100
MULTI 20μs	C-11833118
MULTI 115μs	C-11833126
MULTI 300μs	C-11833134
MULTI 2.0ms	C-11844719
MULTI 4.9ms	C-11833142
MULTI 55ms	C-11833159
MULTI 85ms	C-11833167
DC LOCAL CLOCK DRIVER	C-11832771
DELAY A 30μs	C-11833175
DELAY A 77μs	C-11837143
DELAY C 1.5μs	C-10025518
DELAY C 10μs	C-10025476
DELAY C 10ms	C-11836681
DRIVER 50-90	C-11836392
SYNCHRONIZER	C-11844735
COMPRESSOR	C-11844743
DOUBLE DRIVER 90	C-11918307
INVERTER DRIVER 90	C-11902400
FLIP-FLOP AMPLIFIER	C-11900347

6.24 FLIP-FLOP 20-70

GENERAL DESCRIPTION

The high speed, 20-70, flip-flops are intended for use as active elements in current steering diode logic circuitry operating at frequencies up to 2 megacycles. It serves both as a one-bit memory and as a current amplifier.

BLOCK DIAGRAM DESCRIPTION

The basic high speed flip-flop is shown as a block diagram in Figure 6.24-1. The flip-flop has two input sides, 1 and 0, two corresponding outputs, and a clock line. The outputs are complements of one another, when one output is true, the other is false. An input signal may be in either of two states, true or false.

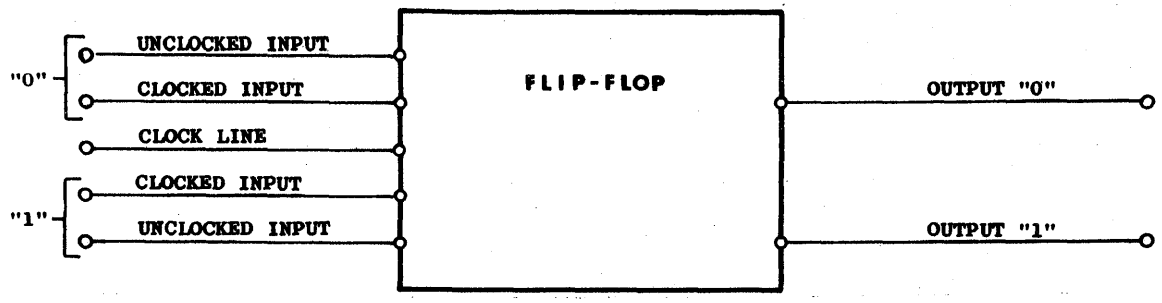


FIGURE 6.24-1. FLIP-FLOP BLOCK DIAGRAM

A false input signal will have no affect on the condition of the flip-flop. A true input signal will determine the state of the flip-flop at the next clock time.

The effect of a true input signal on the flip-flop depends upon which side, 0 or 1, it appears. If it appears on the 0 side, the flip-flop will switch to the "0 State" within a few tenths of a microsecond. If the flip-flop is already in the "0 State", it will remain there. Similarly, a true input signal on the 1 side will cause the flip-flop to switch to the "1 State". If the flip-flop is already in the "1 State", it will remain there. A true signal may occur at either of the two inputs on a side; the unclocked input or the clocked input. If the signal occurs at the unclocked input, it will unconditionally set the flip-flop to the corresponding state. If the signal occurs on a clocked input, it will not set the flip-flop unless the clock is simulataneously true.

If both clocked inputs are true when the clock is true, the flip-flop will complement. That is, it will go from the stable state it is in to the other stable state.

STATIC CONDITIONS

The analysis of the flip-flop can be simplified by first studying its two stable states. The circuit of Figure 6.24-2 shows only those components essential to these states. Since a DC condition is represented, capacitors are shown as open circuits and the delay line is shown as a resistor.

The flip-flop is shown in the "0 State". Since Q2 is in saturation, V_{c2} is only a few tenths of a volt more negative than V_2. The collector current, I_{c2}, will adjust itself to maintain this condition.

There are two resistor networks running from V_1 to the collector of Q2. The first network consists of RD2A and R1A. The resistance ratio is such that when Q2 is in saturation, V_{b3} is more positive than ground. Therefore, the base of Q3 is back biased, Q3 is OFF, and the 0 output is true.

The second network consists of resistors R4A and R5A. This resistance ratio is such that the base of Q1 is more positive than V_2, so that Q1 is held OFF. When Q1 is OFF, V_{c1} is approximately -6V. This voltage is determined by the resistance of R3, R4 and RD2.

The resistance of RD2 is such that when Q1 is OFF, I_2 is much greater than I_1. The resulting I_{b4} is enough to hold Q4 in saturation and thereby make the 1 output false.

The value of R4 is such that I_4 is much larger than I_5 when Q1 is OFF. The resulting I_{b2} is sufficient to hold Q2 in saturation. Therefore, if Q2 is made to saturate, the circuit alone will maintain Q2 in saturation.

R2 = R2A, R3 = R3A, etc.

Q1 and Q2 are interchangeable, as are Q3 and Q4. A signal applied to the 1 input will force Q1 into saturation. From symmetry it is apparent that once Q1 saturates, the circuit will maintain it in saturation. In this state, Q3 will also be in saturation while Q2 and Q4 will be OFF.

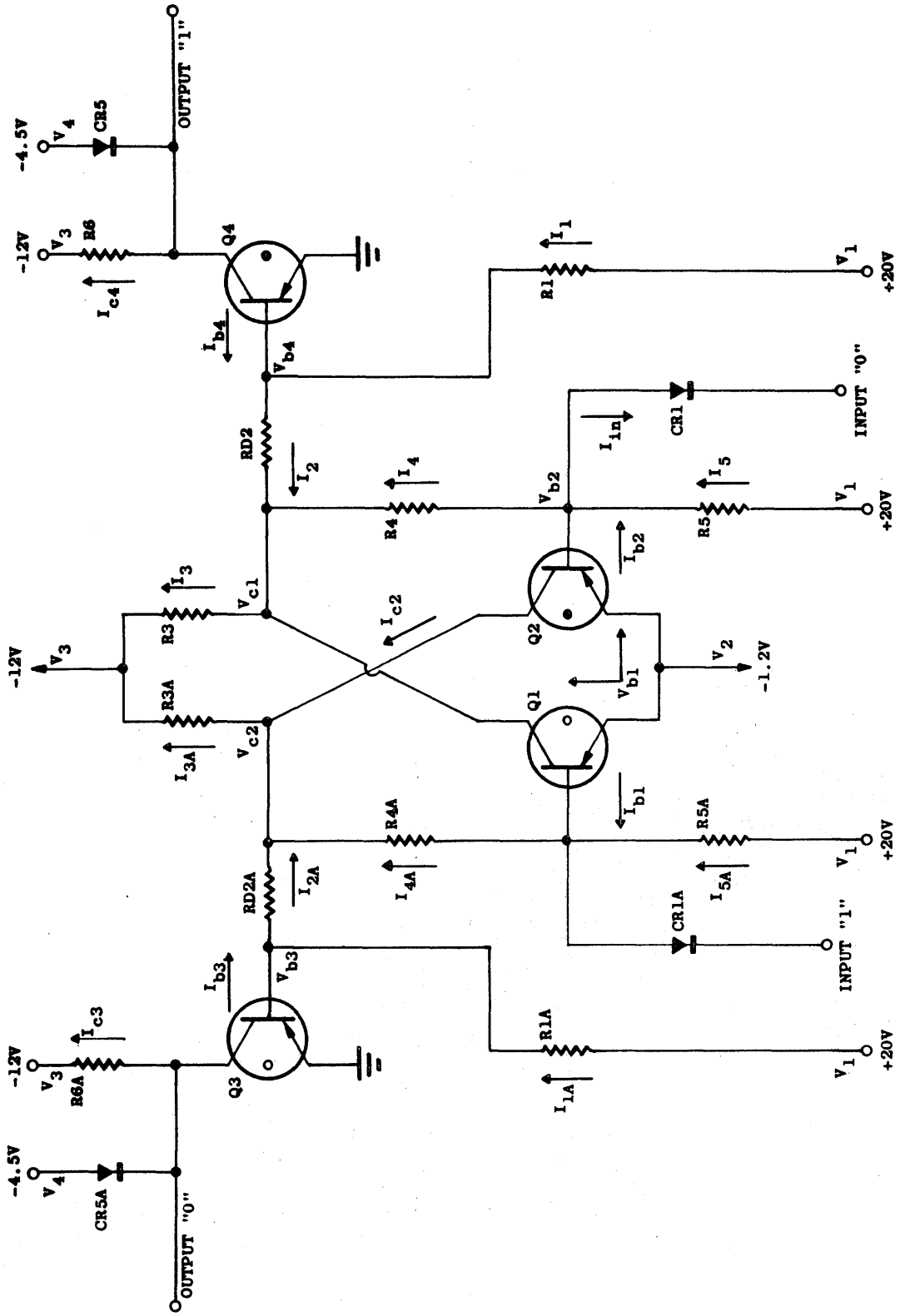


FIGURE 6.24-2. FLIP-FLOP STATIC CONDITION

SWITCHING

Refer to Figures 6.24-3 through 6.24-7.

The process followed by the circuit in going from one stable state to the other is described below. Refer to Figures 6.24-4 through 6.24-7 while going through this description. The amplitudes and timing shown in these figures are only nominal.

Until time, T_0 the flip-flop is in the "1 State", and all voltages and currents have attained a steady state value. At T_0 a current pulse I_{in}, is drained from the 0 input. This current is sufficient to drive Q2 into saturation. As Q2 goes from cut off to saturation, V_{c2} rises towards V_2. As V_{c2} changes, I_{4A} decreases and capacitor C_{7A} discharges, inducing a negative I_{7A}. Sometime during the rise of V_{c2}, I_{7A} becomes greater than $I_{4A} - I_{5A}$. At this time, the base of Q1 becomes back biased and Q1 starts turning OFF.

As Q1 goes off, V_{c1} goes negative. This charges C7 thereby inducing I_7. I_4 is also increased. Both of these currents provide more base drive to Q2.

As Q2 went into saturation, the voltage across RD2A, a series resistance delay element, was decreased by several volts. The delay characteristics of the element prevent the current $I_{2A/0}$ from changing for a time T_d after the change in voltage on the input. After that time $I_{2A/0}$ decreases and stops supplying the base current I_{b3}.

Meanwhile, the change in V_{c1} increases the voltage across RD2, a component identical to RD2A. The amplitude of $I_{2/0}$ cannot change for the same time T_d, but after this, time increases rapidly to its upper limit. As this current change occurs the base emitter diode of Q4 is forward biased and the base current I_{b4} starts to flow.

By the time T_1 the inside transistors, Q1 and Q2 have exchanged states. Q1 is OFF, Q2 is in saturation. The input current I_{IN} may be turned OFF at this time or even before. After T_1, the base current in Q3 decreases and Q3 starts to turn OFF. Simultaneously, the base current in Q4 increases and Q4 starts to turn ON. As Q4 turns ON V_{c4} rises towards ground and as Q3 turns OFF, V_{c3} heads for V_3 due to I_{6A}, but is clamped by CR5A at around -5V.

Finally Q4 is in saturation and Q3 is OFF. Q4 is maintained in saturation by the current $I_{2/0}$ which is now larger than I_1. Q3 is held OFF because its base is back-biased. The flip-flop has reached its second stable state, the "0 State".

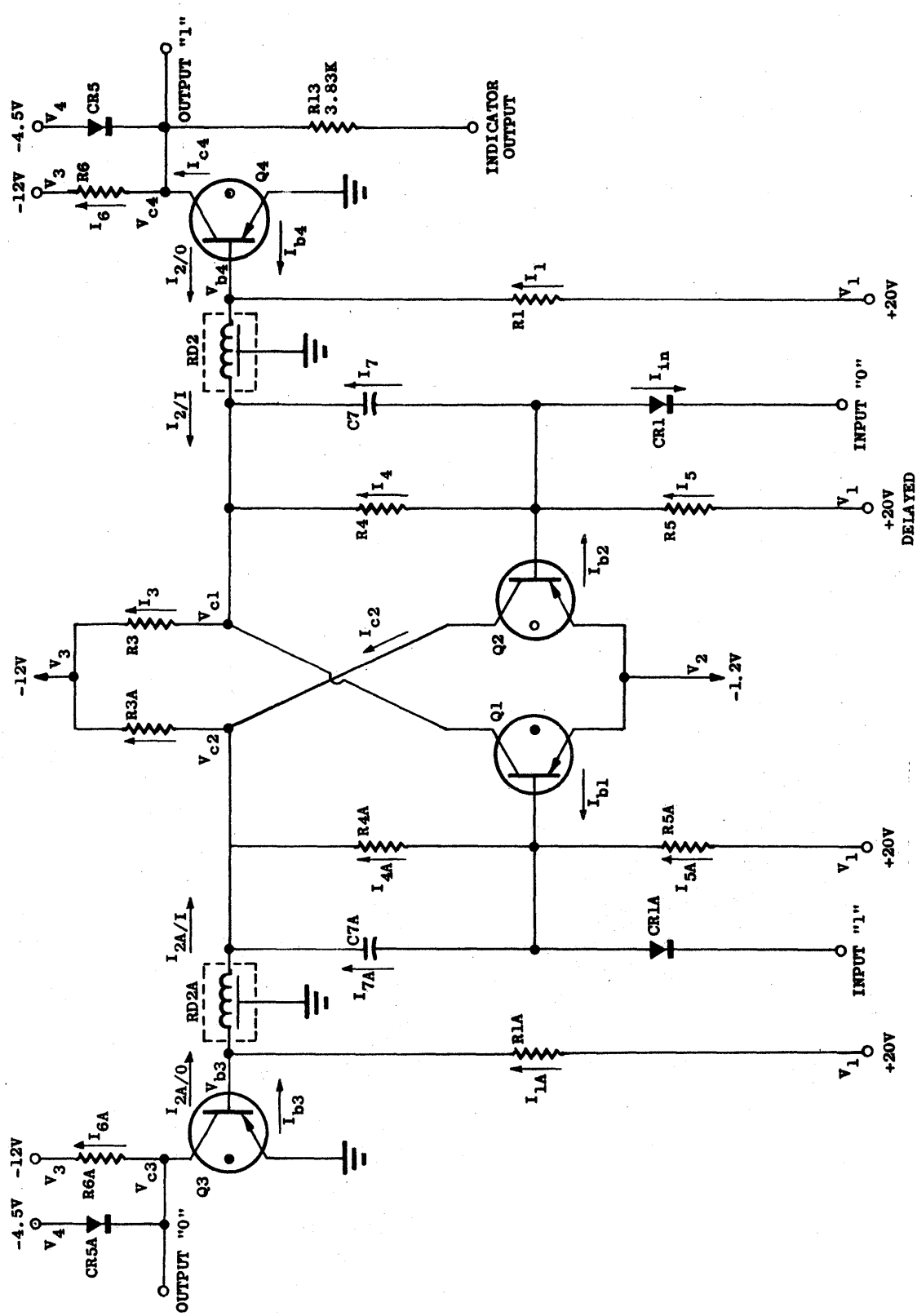


FIGURE 6.24-3. SWITCHING ANALYSIS SCHEMATIC OF THE FLIP-FLOP

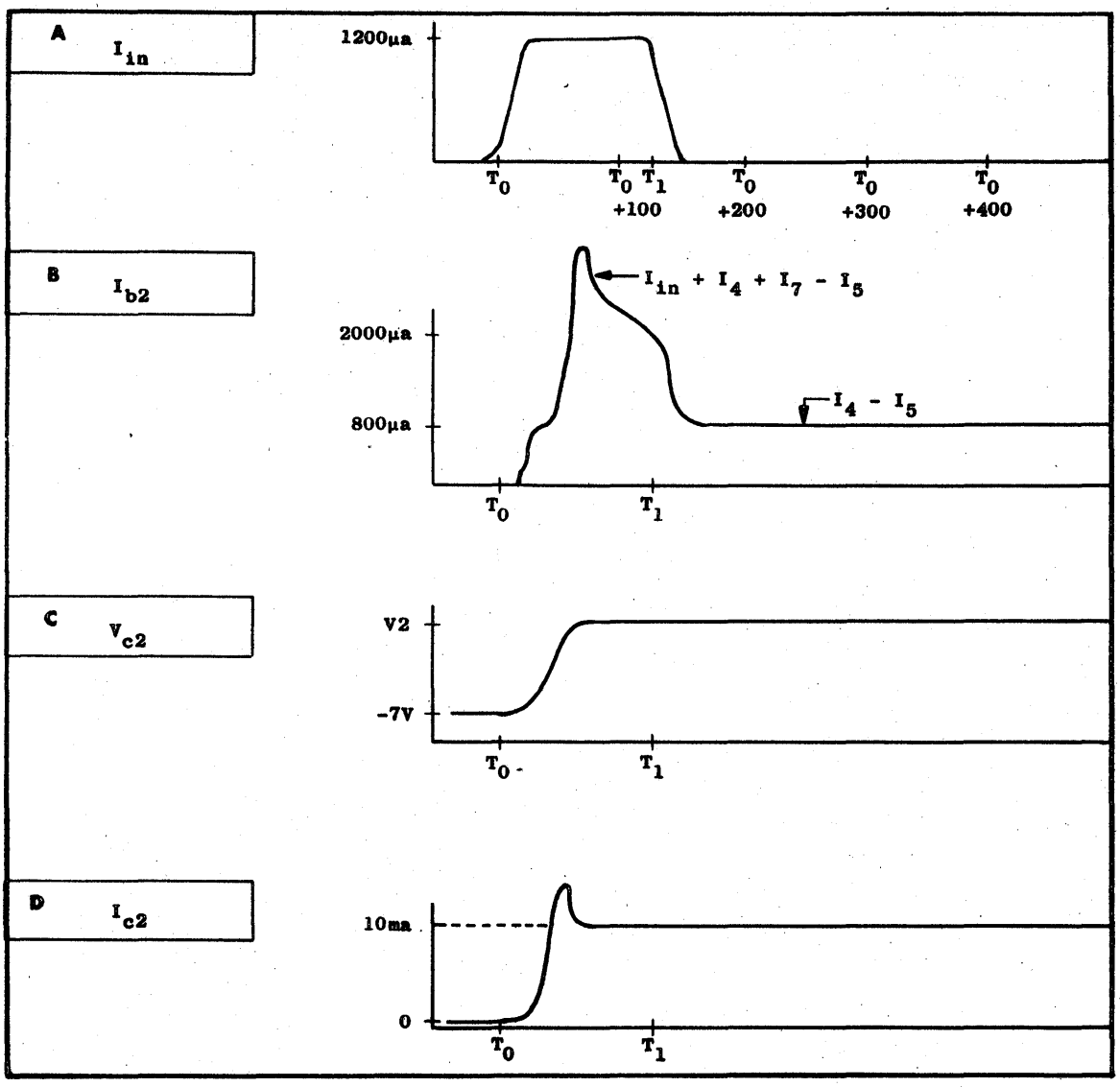


FIGURE 6.24-4. Q2 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

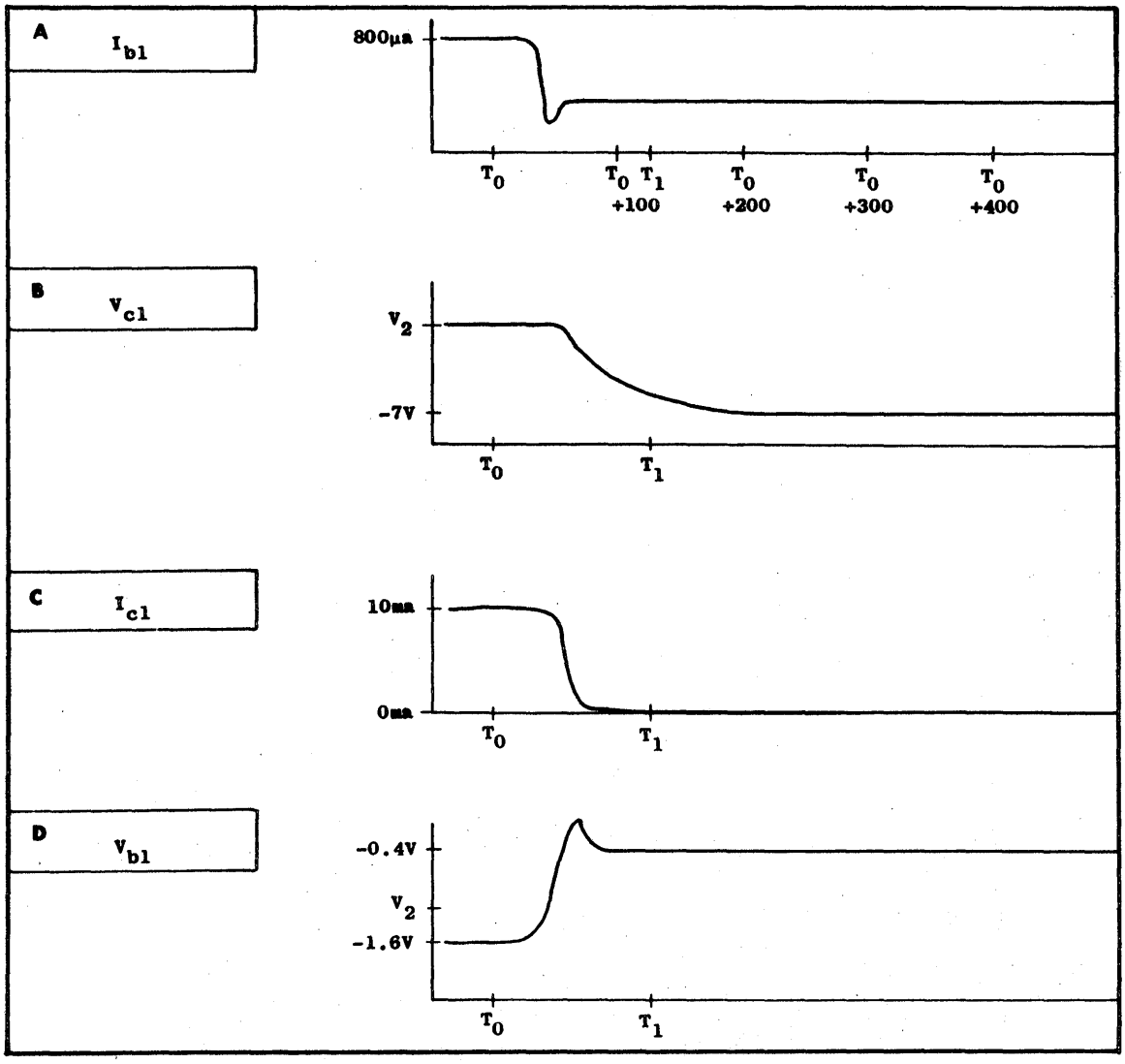


FIGURE 6.24-5. Q1 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

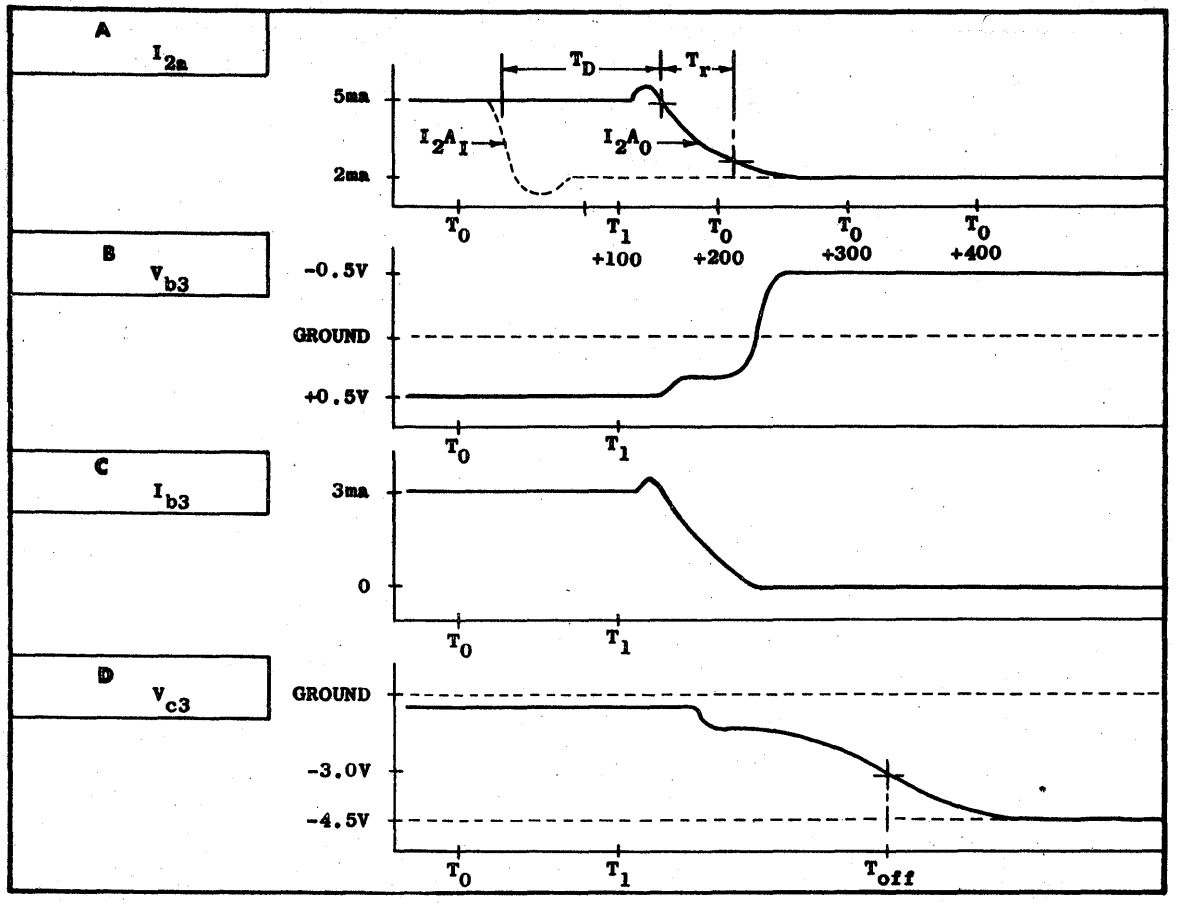


FIGURE 6.24-6. Q3 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

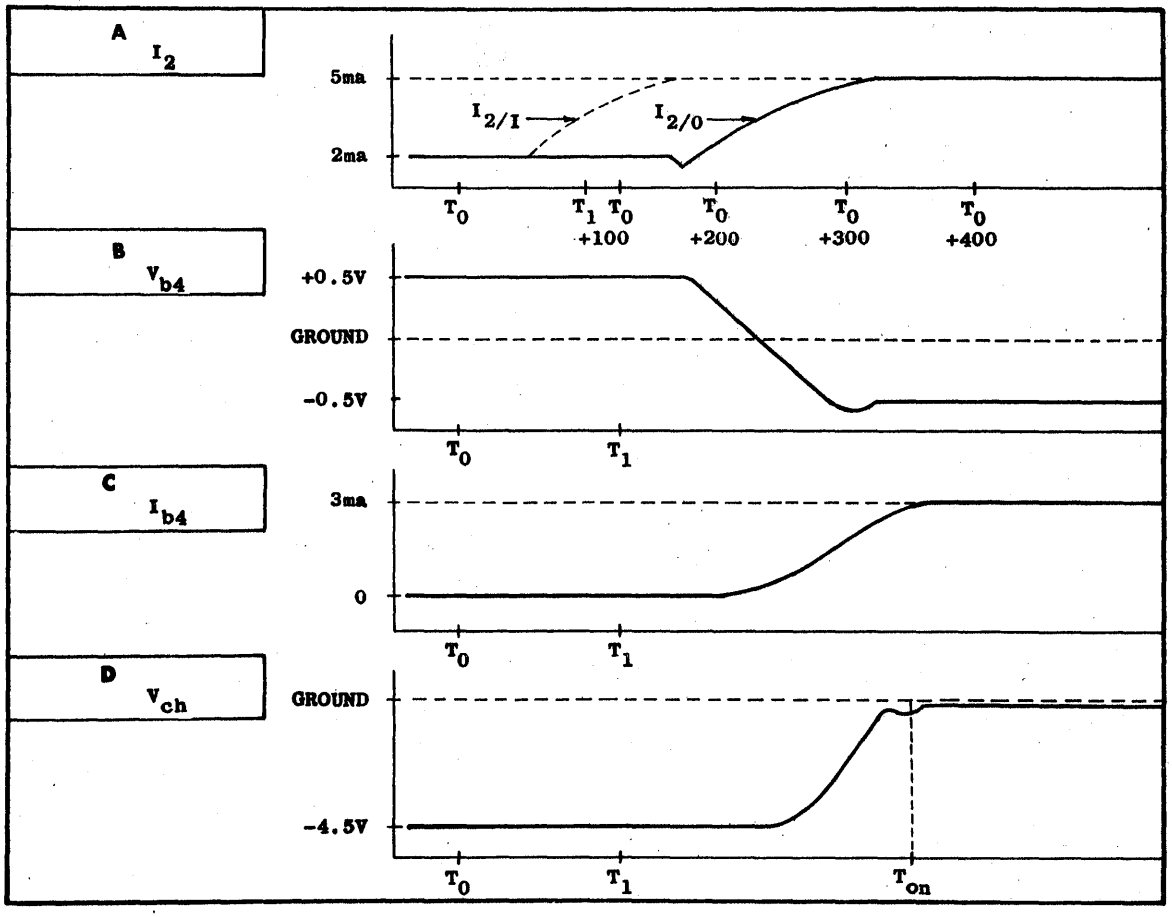


FIGURE 6.24-7. Q4 SWITCHING WAVEFORMS FOR A FLIP-FLOP GOING FROM THE "1" STATE TO THE "0" STATE

INPUTS

The input signals in Figure 6.24-2 and Figure 6.24-3 are shown as coming in through diodes CR1 and CR1A. These are the unclocked inputs. When the gate attached to one of these inputs goes true, the associated transistor will be driven into saturation and the flip-flop will be set. Figure 6.24-8 shows the arrangement of diodes for both the clocked and unclocked inputs on each side.

Each clocked input line is connected to three diodes. On the 0 side (base of Q2) the diodes are CR2, CR3, and CR4. On the 1 side (the base of Q1), the diodes are CR2A, CR3A and CR4A. In order to turn ON Q1 through the clocked input, CR2A must conduct the input current. CR2 must do likewise in order to turn Q2 ON.

Assume that 1 clocked input is true I_{IN} (1) is applied. If the clock is false, V_{c1} will be -0.6V. Therefore, V_{in} (1) cannot go more negative than -0.9V since CR3A will supply a current equal to I_{in} (1) at that voltage. If the clock is true during the time I_{in} (1) is present, CR3A is back biased and CR2A conducts, driving Q1 into saturation.

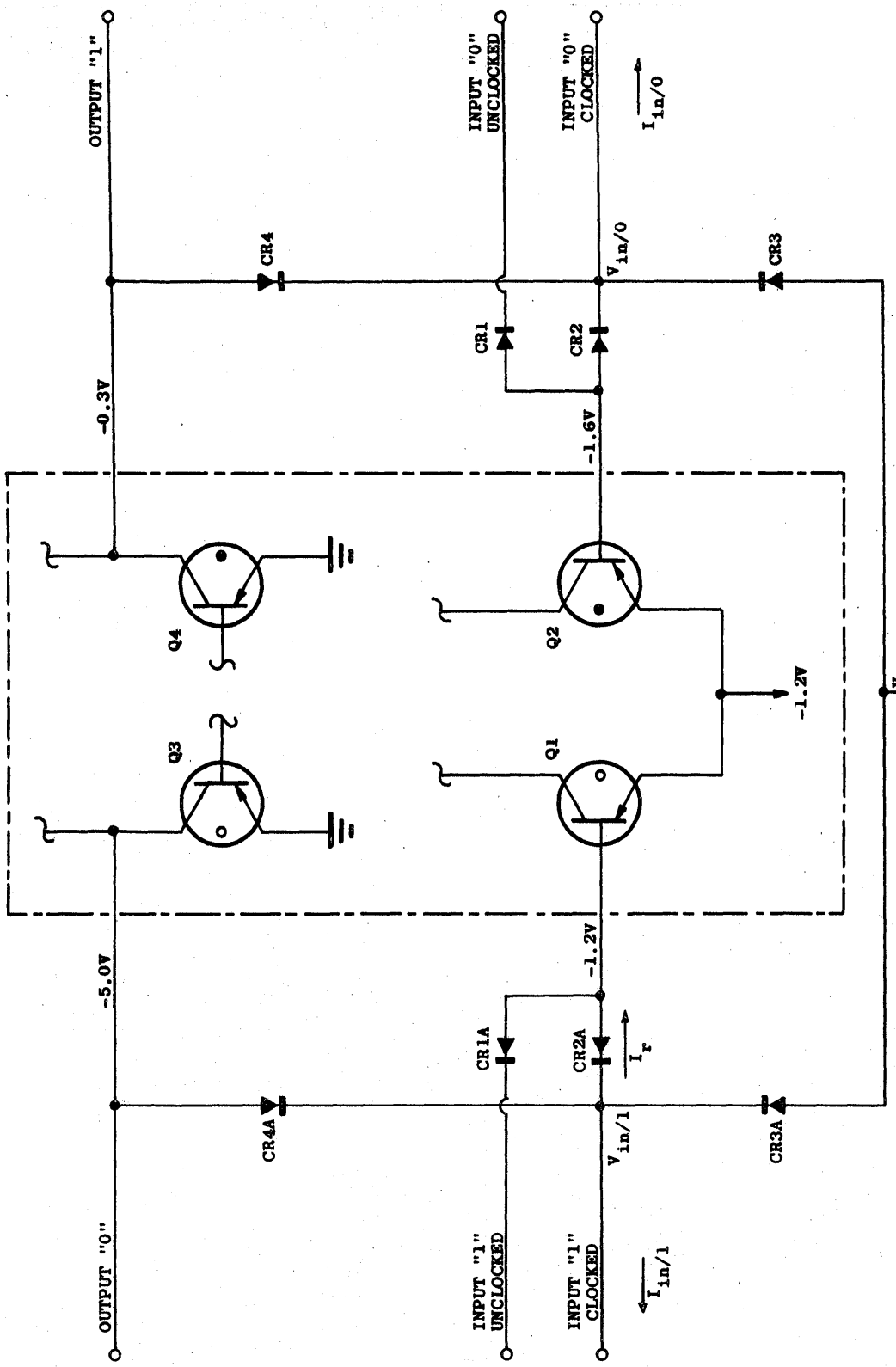


FIGURE 6.24-8. INPUT GATING SCHEMATIC

If instead I_{in} (0) drives the 0 clocked input (trying to set the flip-flop to the "0 State") CR2 cannot conduct, even at clock time, as CR4 clamps V_{in} to -0.6V. However, if Q4 is in saturation, the flip-flop is already in the "0 State".

If I_{in} (1) and I_{in} (0) are applied simultaneously and the clock is also true, the flip-flop will complement, that is, it will change state. If the flip-flop is in the "0 State", then CR2 will not see I_{in} (0) due to the clamping effect of CR4, but CR2A will conduct I_{in} (1). The flip-flop would therefore switch to the "1 State". If the flip-flop started in the "1 State", it would switch to the "0 State".

LOGICAL OUTPUTS

There are two logical outputs per flip-flop. These outputs are logical complements of one another.

When an output is false, it must supply currents to the gates attached to it. These currents are usually the major part of the collector current through the saturated transistor. When an output is true, the output transistor is OFF. The collector resistor and the -12V Supply pull the output voltage negative until it is clamped by the diode to the -4.5V Supply.

INDICATOR OUTPUTS

The resistor $R_{ind/A}$ may be connected to neon indicator light drivers. These lights will visually indicate the state of a flip-flop.

SEQUENCING POWER SUPPLIES ON

The flip-flop will be in the "0 State" immediately after the power is turned ON if the supplies are activated in the sequence +20V, -1.2V, -4.5V, -12V, then +20V delayed.

When the -12V Supply is turned ON, the collectors of Q1 and Q2 will start to go negative. As the collector of Q1 goes negative, Q2 will get the base current and start conducting since it has no cut off current. However, though the collector of Q2 may go a little negative, Q1 will not go on because of the cut off current supplied by +20V Supply through R5A. Since Q1 is held OFF, Q2 will go into saturation. When +20V delayed goes ON, Q2 will be in saturation and Q1 will be cut off (the 0 state). In this condition, the cut off current through R5 cannot affect the state of the flip-flop.

MANUAL CONTROL

The flip-flops can be set to either state through a manual switching operation which is completely decoupled from the logical inputs. This operation is performed on the input normally connected to the +20V delayed input. R5 in conjunction with an external switching arrangement can supply drive current to manually SET and RESET the flip-flop.

Figure 6.24-9 shows an arrangement which will provide this manual SET/RESET feature. S_1 is a make before break switch normally set to position B. While the switch is in this position the flip-flop can be used in a normal fashion by the machine.

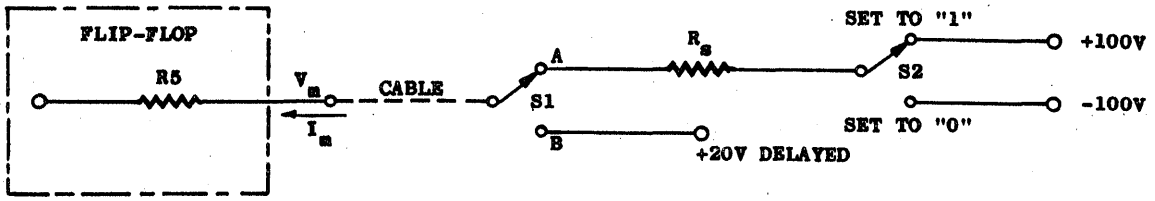


FIGURE 6.24-9. MANUAL CONTROL SWITCH

To manually set the flip-flop to the "1" or "0 State", S_2 is set to the appropriate position. S_1 is momentarily set to position A and returned to position B. By the time S_1 is returned to position B, the flip-flop will be in the desired state.

If S_2 were connected to the -100V Supply, then an I_{IN} would be induced through R5 which would drive Q2 into saturation and force the flip-flop to the "0 State".

S_1 is a make before break switch. If it were not, then in the interval that no contact was made at either A or B, the connection to R5 would be open circuited. At this time the flip-flop would have no noise threshold on the 0 input and might be spuriously set to an undesired state.

POWER SUPPLY VOLTAGES

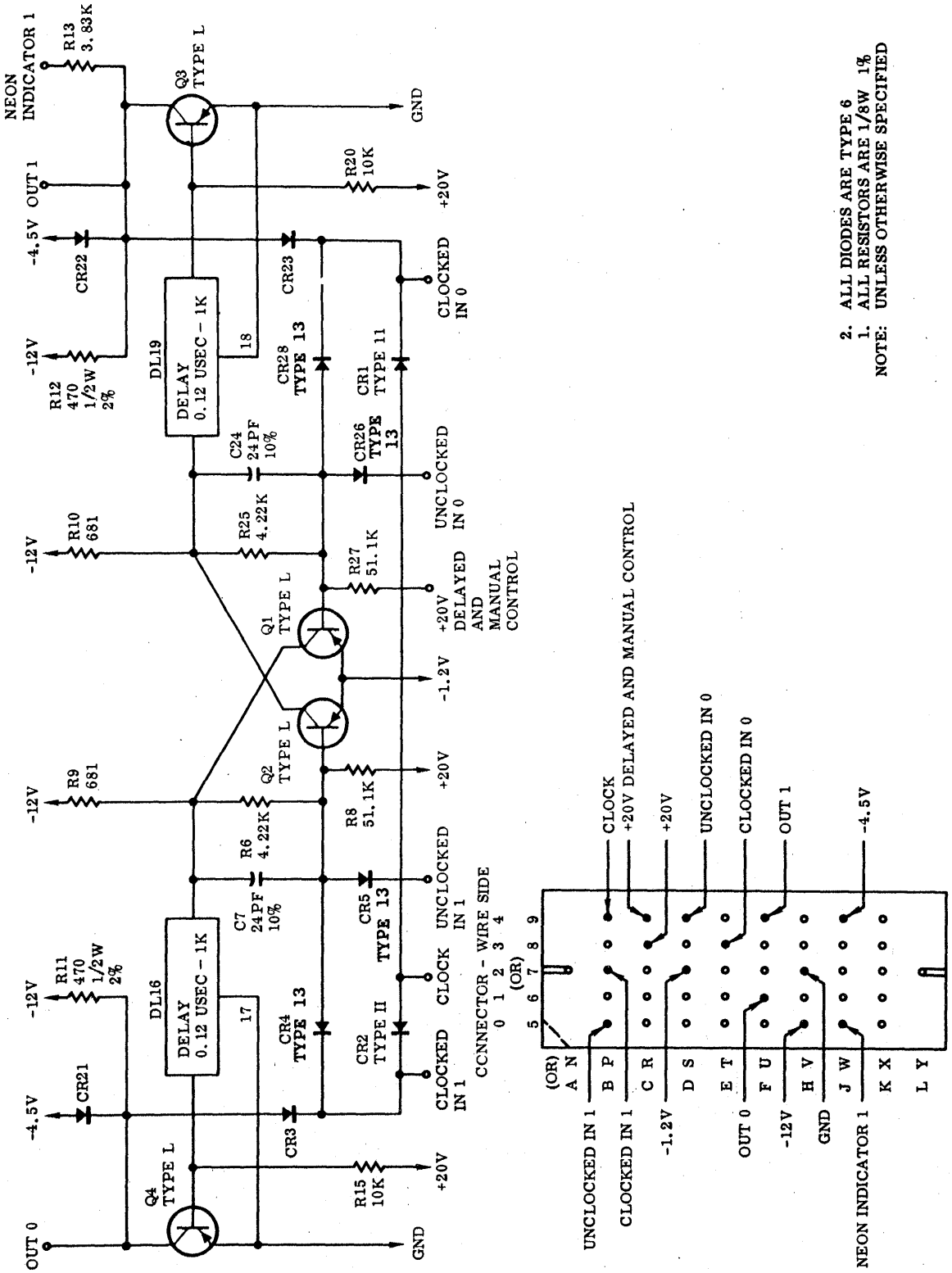
The +20V, and +20V Delayed provide the off bias for the transistors. The -1.2V is used to give an input voltage threshold. If the emitter of Q1 and Q2 were grounded, a false input level, V_{IN}, no more negative than -0.5V could trigger the flip-flop. This is unacceptable for logical operation since the false levels of the input gates may be as negative as -1.2V.

The -12V provides collector voltages and the base currents for the circuit.

The -4.5V prevents the true output levels from going excessively negative. This reduces voltage swings and the time required to charge and discharge stray capacitance. This also reduces the collector voltages on Q3 and Q4.

PACKAGE SCHEMATIC

Refer to Figure 6.24-10 for the complete schematic of the flip-flop 20-70 parallel plate package.



NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/8W 1%
2. ALL DIODES ARE TYPE 6

FIGURE 6.24-10. FLIP-FLOP 20-70 PACKAGE SCHEMATIC

6.25 SWITCH I

GENERAL DESCRIPTION

The standard Switch I is intended for use as an active element in current-steering diode-mode logical circuitry. The switch always inverts and amplifies the incoming signal. The logical is used as an inverter.

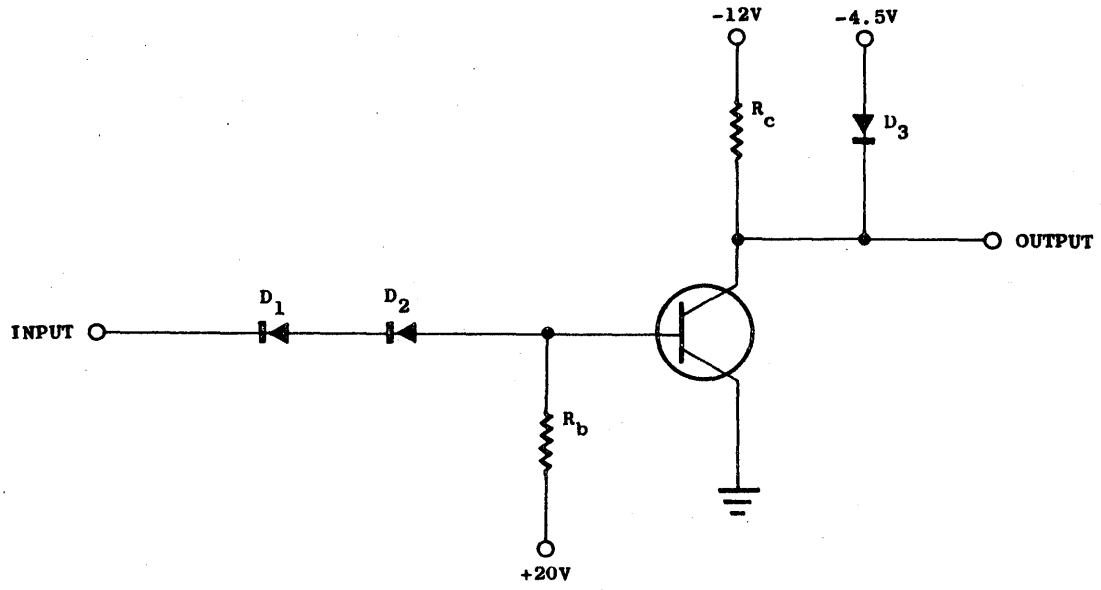


FIGURE 6.25-1. SWITCH I SCHEMATIC

COMPONENTS

The circuit consists of one transistor stage with associated components. Diodes CR1 and CR2 are silicon diodes (stabistors) with a forward drop in the range of 0.5V.

The purpose is to hold the transistor base 1V positive with respect to the input. This guarantees that the switch will be back-biased even if the input goes to -1V.

The resistor R_b is used as a pull-up resistor during the back-biasing of the transistor. It also supplies the ICBO protection and the current to remove base charge during the transistor turn-off. The transistor Q1 is the active element in the circuit. It is a PNP germanium transistor of the mesa design and provides the amplification and inversion of the signal. Diode CR3 is used to clamp the output voltage at -4.5V. This clamping action drastically reduces the switching dissipation of the transistor. Resistor R_c is the collector supply return, the value of which is determined by expected loads.

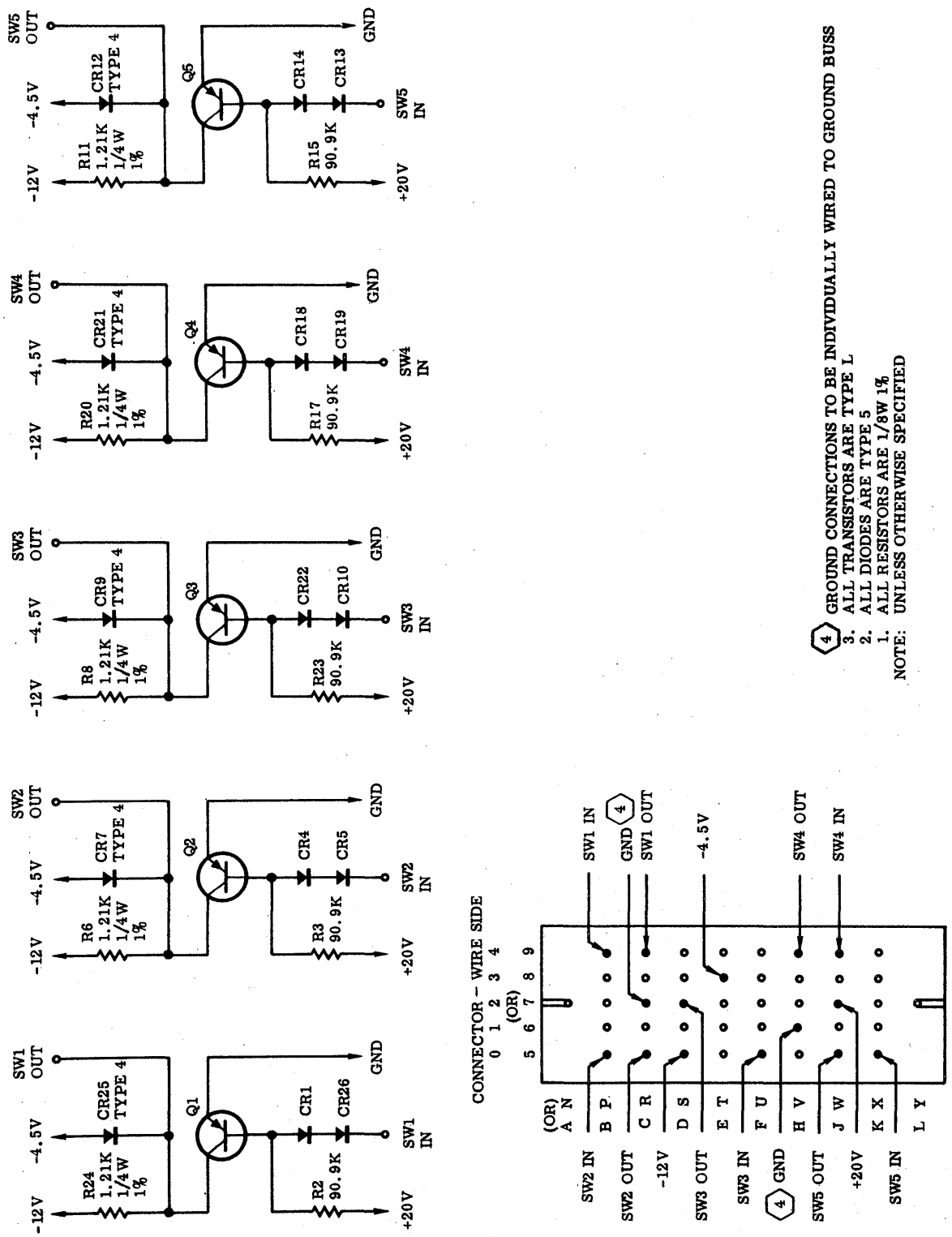
OPERATION

The following is a description of the basic operation of the circuit.

Assuming the transistor is OFF, the input signal will be more positive than -1.0V. The base of the transistor will then be positive through the action of CR1, CR2 and Rb. The transistor is back-biased and the collector voltage is damped through CR3 to -4.5V. When the input signal becomes more negative than -1.0V, the transistor becomes forward-biased and goes into the saturation region. During this state, there is an effective amplification of the input current to the collector current in the ratio of 20:1.

PACKAGE SCHEMATIC

Refer to Figure 6.25-2 for the complete schematic of the Switch I parallel plate package.



4 GROUND CONNECTIONS TO BE INDIVIDUALLY WIRED TO GROUND BUSS
3. ALL TRANSISTORS ARE TYPE L
2. ALL DIODES ARE TYPE 5
1. ALL RESISTORS ARE 1/8W 1%
NOTE: UNLESS OTHERWISE SPECIFIED

FIGURE 6.25-2. SWITCH I PACKAGE SCHEMATIC

6.26 DRIVER 50-90

GENERAL DESCRIPTION

The Driver 50-90 is a non-inverting switch amplifier to be used in current mode diode logic circuitry and for driving cables and other loads requiring currents up to 90 ma. Depending on load conditions, it can operate at switching rates in excess of 5 megacycles. In current mode diode logic, the circuit restores the true and false levels as well as amplifying.

BLOCK DIAGRAM DESCRIPTION

See Figure 6.26-1 for Driver 50-90 Block Diagram illustration.

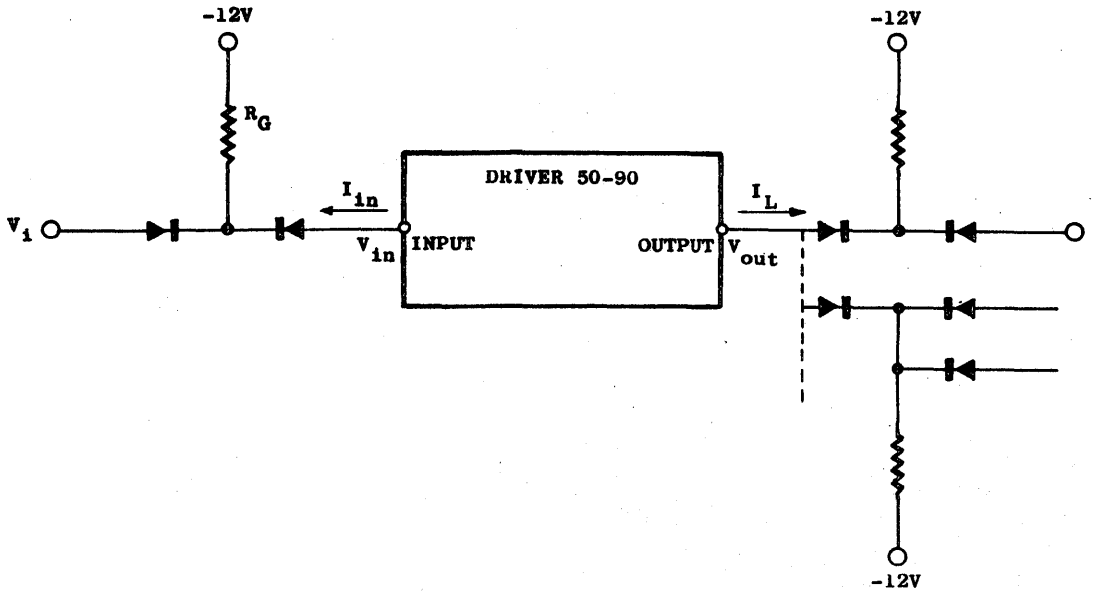


FIGURE 6.26-1. DRIVER 50-90 BLOCK DIAGRAM

A Driver has one input and one output. The output responds to input signals in one of two ways.

1. If the input signals are such as to hold the input between ground and -1.0V, then V_0 will be between ground and -0.3V and will be able to supply an I_L of up to 90 ma.

2. If the input signals can produce an I_{in} of 1 ma or more (occurring when V_i is more negative than -1.8V), then V_0 will be more negative than -4.5V provided I_L is no greater than -8.0 ma.

CIRCUIT DESCRIPTION

Refer to Figure 6.26-2 for working schematic of Driver 50-90.

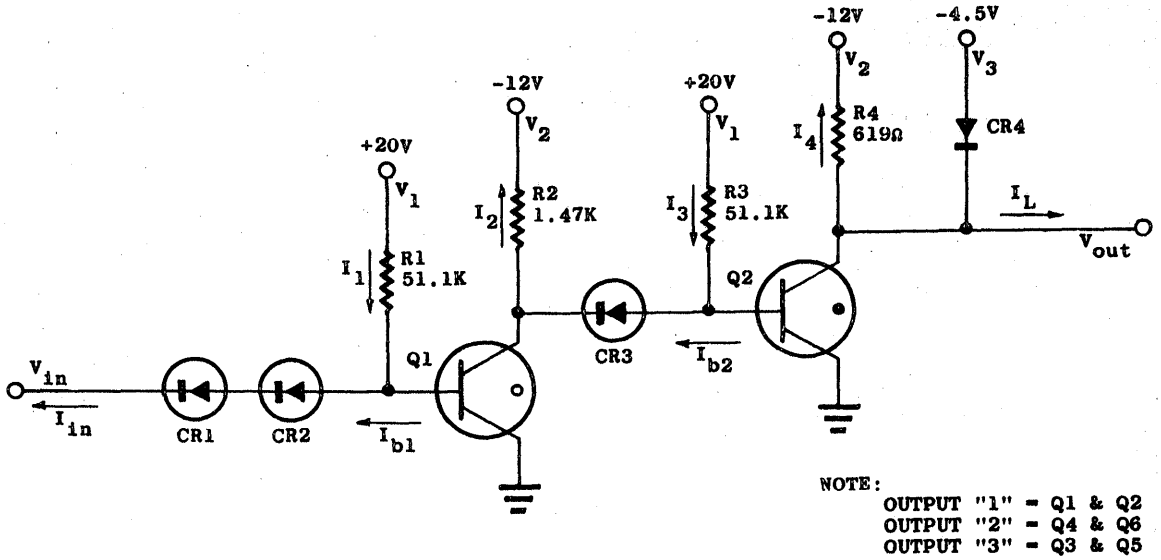


FIGURE 6.26-2. DRIVER 50-90 CIRCUIT SCHEMATIC

Driver 50-90 is basically two switches connected serially. The two states described under Block Diagram Description occur as follows:

1. When V_{in} is -1.0V or more positive, V_{b1} is at ground or above, due to the forward drop characteristics of silicon diodes CR1 and CR2. With V_{b1} at ground, Q1 is necessarily cut off. With Q1 OFF, I_2 flows through CR3. This current is much greater than I_3 so that a large I_{b2} results. I_{b2} is sufficient to hold Q2 in saturation when I_{c2} is as great as 119 ma. Since the maximum I_4 is 20 ma, I_L can be as great as 90 ma.

2. When I_{in} exceeds 1.0 ma, it also exceeds I_1 by several hundred microamps. Therefore, an I_{b1} flows, which is sufficient to drive Q1 into saturation. This brings V_{c1} to -0.3V. Thus, the base of Q2 is above ground so that Q2 is OFF. Thus, the base of Q2 is above ground so that Q2 is OFF. CR4 is forward-biased and supplies I_4 so that V_0 is slightly more negative than -4.5V.

SWITCHING

Refer to Figures 6.26-2 and 6.26-3.

When the input changes from the false conditions (V_i more positive than -1.0V) to the true condition (V_i more negative than -1.8V and I_{in} > 1.0 ma), the following sequence of events occurs in the driver.

1. I_{b1} starts from the cut off condition in which no forward current flows.

2. When I_{in} exceeds I_1, I_{b1} starts flowing.

3. Q1 turns on at a rate which depends on transistor speed and available I_{b1}.

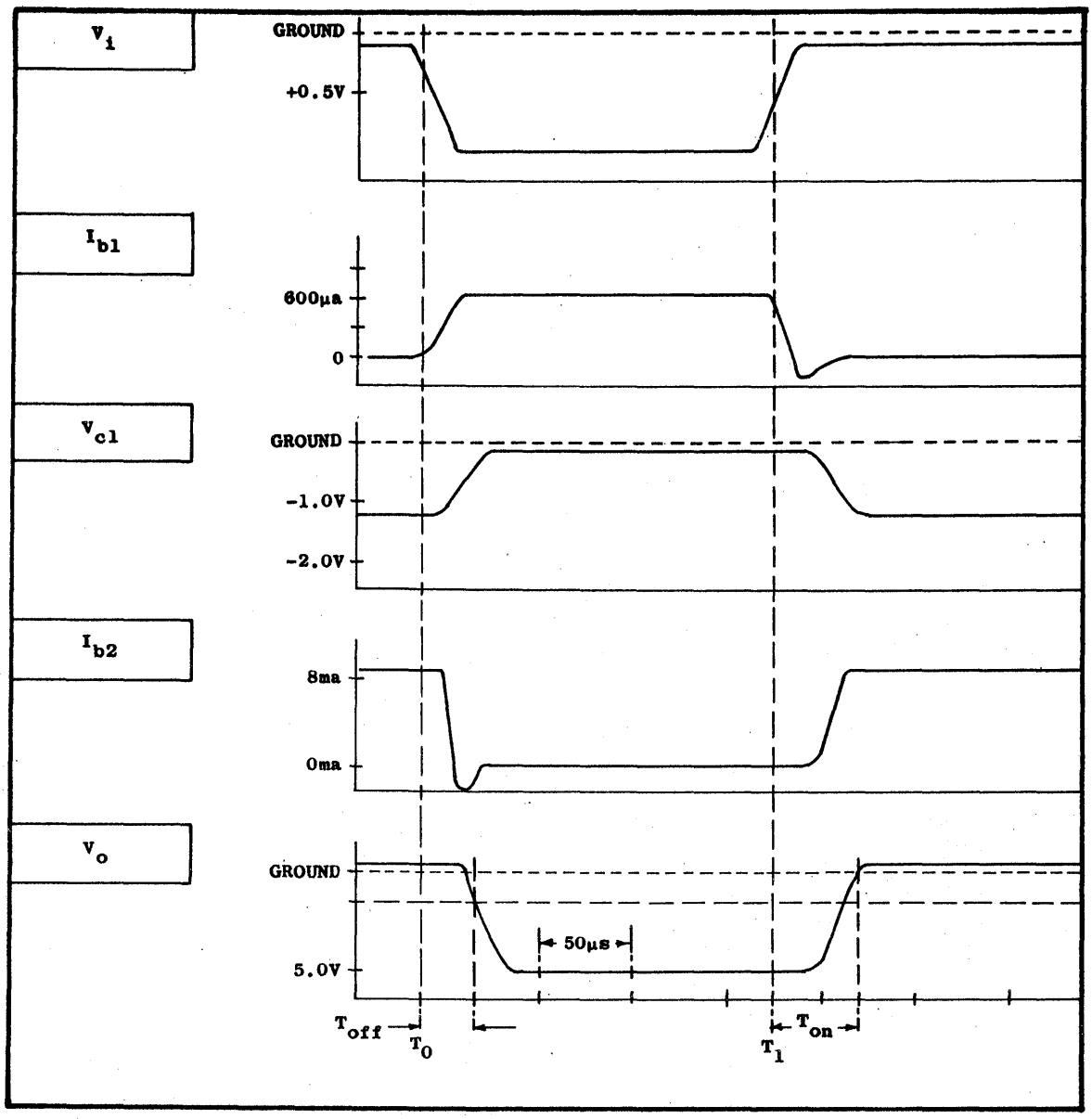


FIGURE 6.26-3. DRIVER 50-90 TYPICAL WAVEFORMS

4. V_{c1} is about -1.3V when Q1 is OFF. It is clamped at this level by the sum of the forward drop of CR3 and the base emitter diode of Q2. It is driven to -0.3V as Q1 turns ON.

5. During turn on, Q2 starts supplying I_2 so that I_{b2} is reduced. Also during this period, CR3 which is a stabistor, looks like a battery so that some reverse current may flow through it even though it is forward-biased. This reverse current and I_3 combine to sweep out the stored base charge of Q2 and turn Q2 OFF in the shortest possible time.

6. When Q2 turns OFF, V_0 falls. The rate at which V_0 falls will depend primarily on the output load conditions.

When the input goes from this true state to the false state, the reverse sequence occurs.

PACKAGE SCHEMATIC

Refer to Figure 6.26-4 for the complete schematic of the Driver 50-90 Parallel Plate Package.

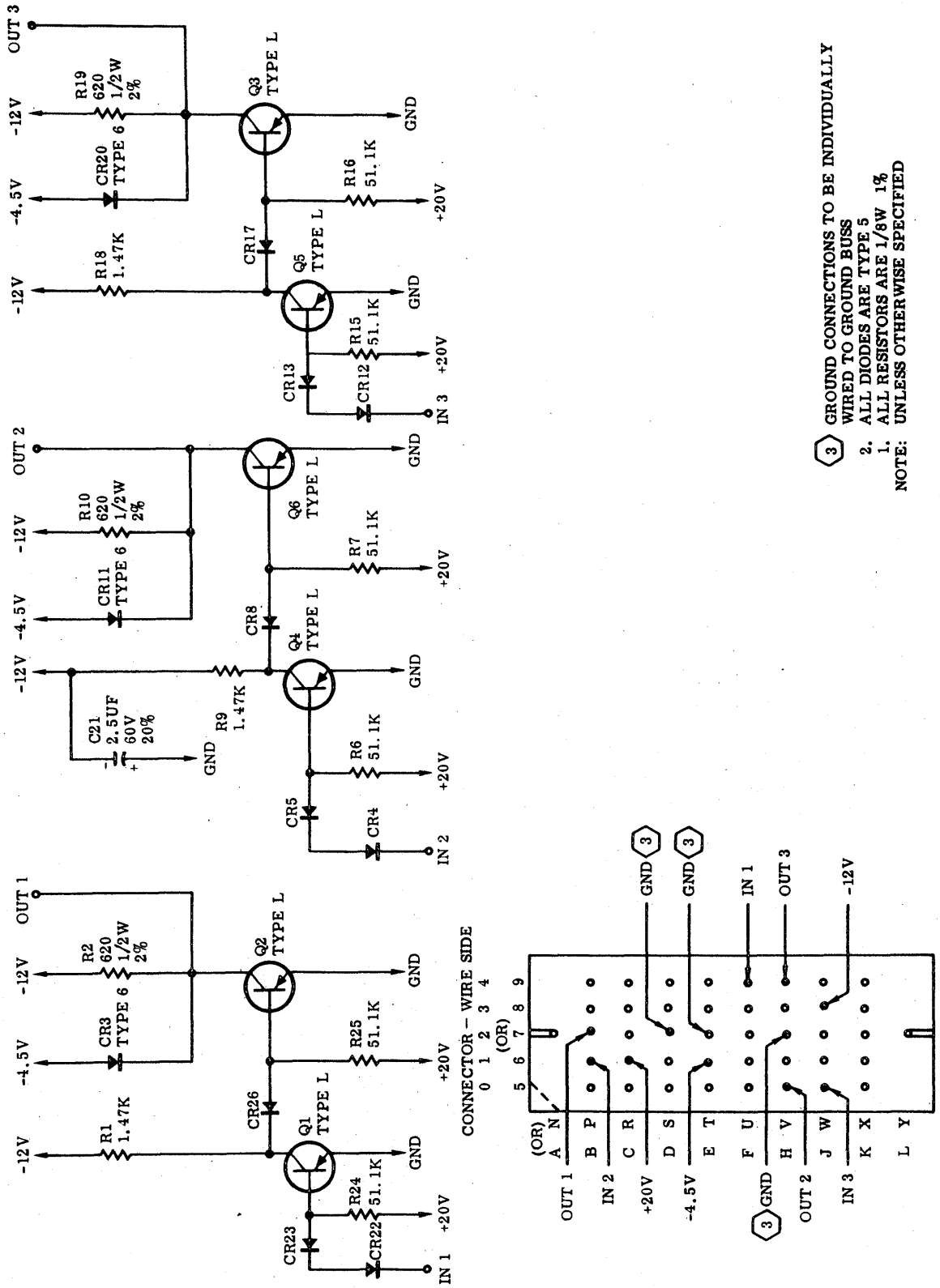


FIGURE 6.26-4. DRIVER 50-90 PACKAGE SCHEMATIC

6.27 DELAY "A"

GENERAL DESCRIPTION

The Delay "A" is a delay circuit of the holdover type to be used in current steering diode logic. The output in the quiescent state is false. When a short negative pulse (0.10 to 0.20 μs) is received, the output becomes true. With this type input, the delay time is measured from the beginning of the input pulse.

If after at least 25 percent of the delay time, a second input pulse is received, the output will continue true and will now be timed from the beginning of the second pulse. The circuit may thus be kept in the true state for any desired length of time by the repeated application of short input pulses.

After the conclusion of the last input pulse, the circuit will time out the delay and then return to the false state.

The delay time is determined by the choice of two capacitors and by the adjustment of a potentiometer.

CIRCUIT DESCRIPTION

Refer to Figure 6.27-1 for circuit schematic and to Figure 6.27-2 for Delay "A" Timing.

INITIATE OUTPUT PULSE

In the quiescent condition, Q1 is cut OFF, Q2 is conducting, and Q3 and Q4 are saturated. At this time, the potential at the input terminal is -1.2V.

When a negative pulse of greater magnitude is applied to the input terminal so that the potential lies in the range of -1.4V to -2.2V, Q1 will begin to conduct. The input voltage cannot go more negative than this because the base emitter diode of Q1 will act as a clamp.

When Q1 begins to conduct, the collector which has been resting at -6.0V will start toward its saturation voltage of about -0.3V. The collector is restrained by capacitors C12 and C14 so that approximately 6 coulombs must be removed from these capacitors before saturation is reached. The time required for this is called T_a. In general, $T_a = T_{in}$. Therefore, it is necessary to supply current to hold Q1 ON until the end of T_a. The collector current of Q1 is derived between R9, C12 and C14. That portion which flows in C14 is applied to the base of Q3 to turn Q3 OFF. When Q3 begins to turn OFF, its collector which was resting near ground, starts toward -12V. CR20 will then begin to conduct, allowing R19 to supply current to the base of Q1, thus holding Q1 ON. As soon as Q1 has become saturated, C14 receives no more current from Q1.

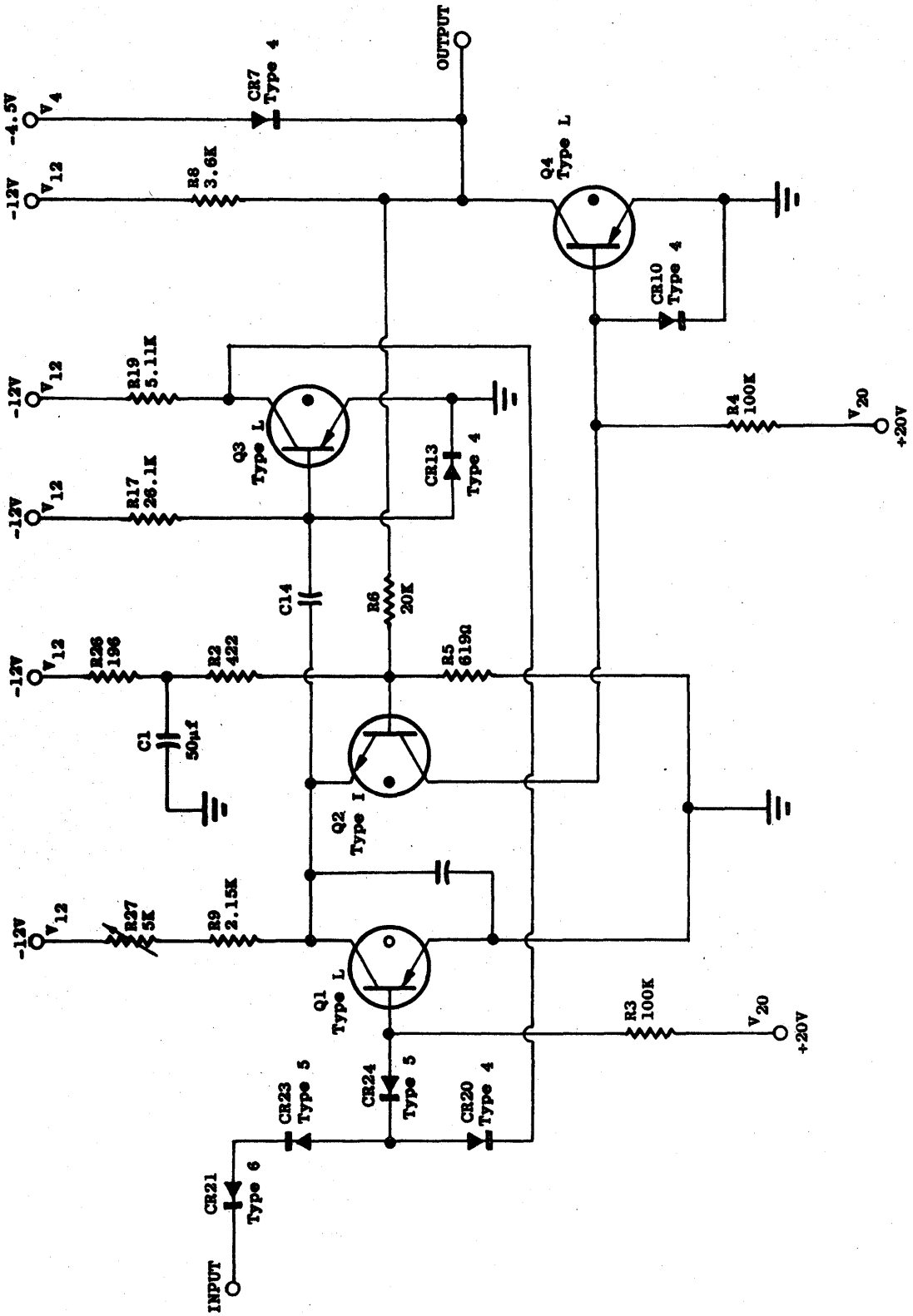


FIGURE 6.27-1. DELAY "A" CIRCUIT SCHEMATIC

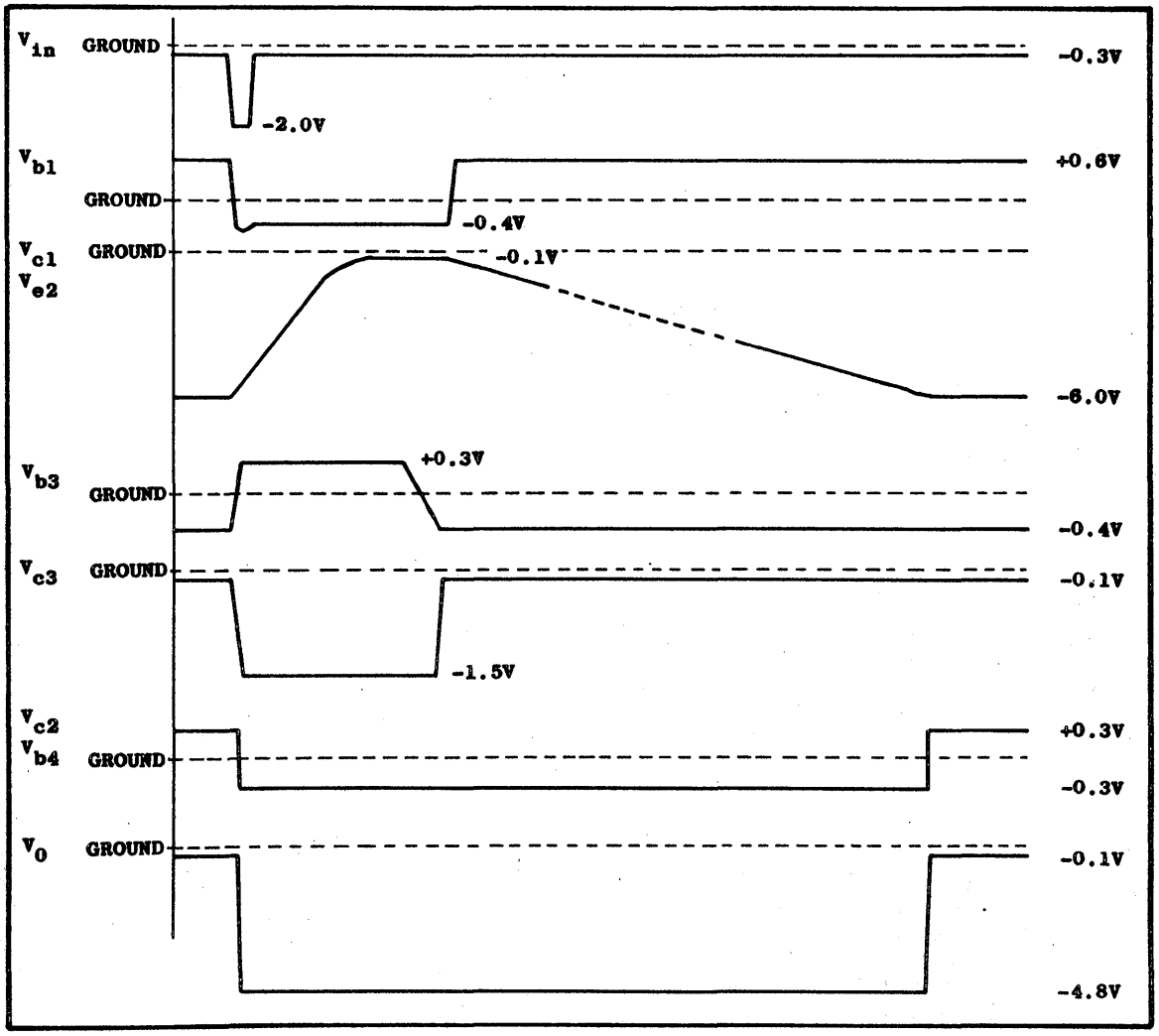


FIGURE 6.27-2. DELAY "A" TIMING

At this time, the base of Q3 will be at approximately +0.3V, being prevented from going more positive by CR13. When Q1 goes into saturation, the base of Q3 will be pulled toward -12V by R17, but will move slowly because C14 must be charged. When the base of Q3 becomes slightly negative, Q3 will begin to conduct. CR20 will then cease to conduct so that Q1 will be turned OFF. Meanwhile, as soon as the collector of Q1 has moved about 0.1V, Q2 has begun to turn OFF.

The turn OFF of Q2 removes the drive from Q4 so that it turns OFF, initiating a true output pulse

OUTPUT PULSE TERMINATION

After Q1 turns OFF, C12 and C14 begin to charge toward -12V thru R9. When the potential reaches approximately 6V, Q2 begins to turn ON. When Q2 turns ON, the collector current will begin to turn Q4 ON. When Q4 begins to turn ON, feedback through R6 will speed up the turn ON, thus terminating the output pulse.

After 20 percent of the delay time has passed, C14 will be reset and the collector of Q1 has moved far enough so that a new input pulse will re-trigger the circuit. The delay time may now be measured from the new pulse.

PACKAGE SCHEMATIC

Refer to Figure 6.27-3 for complete schematic of the Delay "A" Parallel Plate Package.

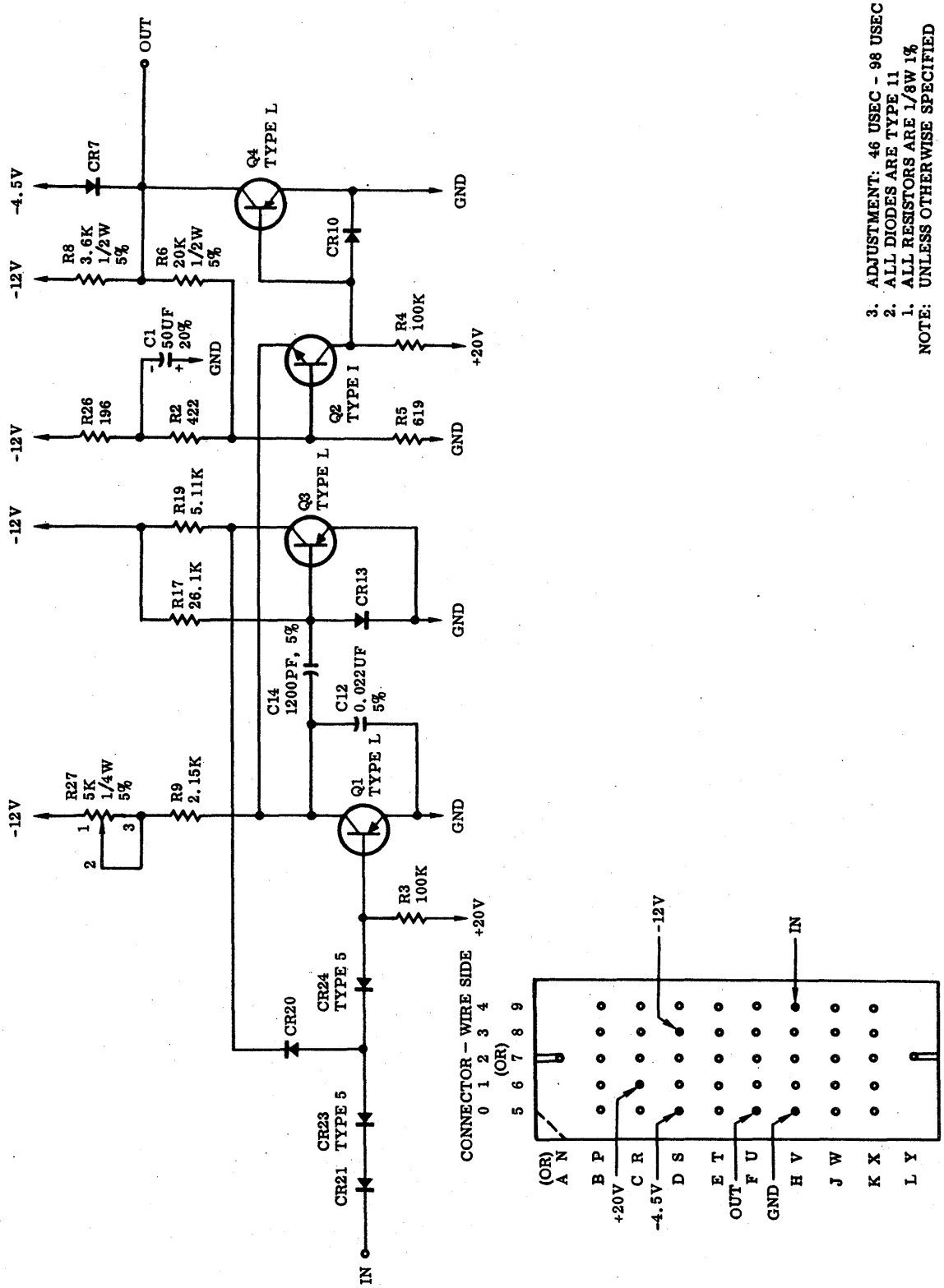


FIGURE 6.27-3. DELAY "A" PACKAGE SCHEMATIC

6.28 DELAY "C"

GENERAL DESCRIPTION

The Delay "C" is a delay circuit of the holdover type. When a negative pulse of prescribed minimum width (0.11 μs) and magnitude is received at the input, the output is caused to go negative, and will remain negative until a specified delay time after the completion of the input pulse. If, before the output pulse is completed, a new input pulse of the proper length and magnitude is received, the output will continue negative until the delay time has elapsed after the completion of the last input pulse received. There is no maximum limit on length of input pulse which can be tolerated, but the delay time does not begin until the input is completed. Delay time is determined by the choice of a capacitor and by the adjustment of a potentiometer.

CIRCUIT DESCRIPTION

Refer to Figure 6.28-1 for Delay "C" circuit schematic, and Figure 6.28-2 for Delay "C" Timing.

INITIATION OF THE OUTPUT PULSE

In the quiescent condition, Q1 is cut OFF, Q2 is conducting, and Q3 is saturated. At this time, the potential at the input terminal is -1.0V. When a negative pulse is applied to the input terminal, the potential will become more negative and lie in the range of -1.2V to -2.2V, being prevented from going more negative by the base emitter diode of Q1. Q1 begins to conduct, causing its collector which has been resting at -6.0V, to start toward its saturation voltage of approximately -0.3V. The first change in the collector voltage will be a small step due to voltage drop across R14. Since the emitter of Q2 is connected to this point, Q2 will quickly be turned OFF. The collector of Q1 will now continue toward saturation at a rate determined by C17. The input time must be suffficient (0.11 μs) to allow this process to reach completion if accurate timing is to be obtained.

When Q2 is turned OFF, the drive is removed from Q3 so that Q3 is quickly turned OFF. When Q3 is turned OFF, the output pulse is initiated.

CONCLUSION OF THE OUTPUT PULSE

At the conclusion of the input pulse, Q1 turns OFF and C17 begins to charge toward -12V through R21 and R27. When the potential reaches -6.0V, Q2 will begin to turn ON. When Q2 begins to turn ON, Q3 will also begin to conduct. As soon as the current at the collector of Q3 is sufficient to cause the collector voltage to charge, the base of Q2 will be made slightly more positive. This brings Q2 further into conduction and speeds the turn ON of Q3. When Q3 goes into conduction, the output pulse is terminated. If at any time during the above delay cycle, a new input pulse of sufficient length is received, C17 will again discharge, initiating a new delay.

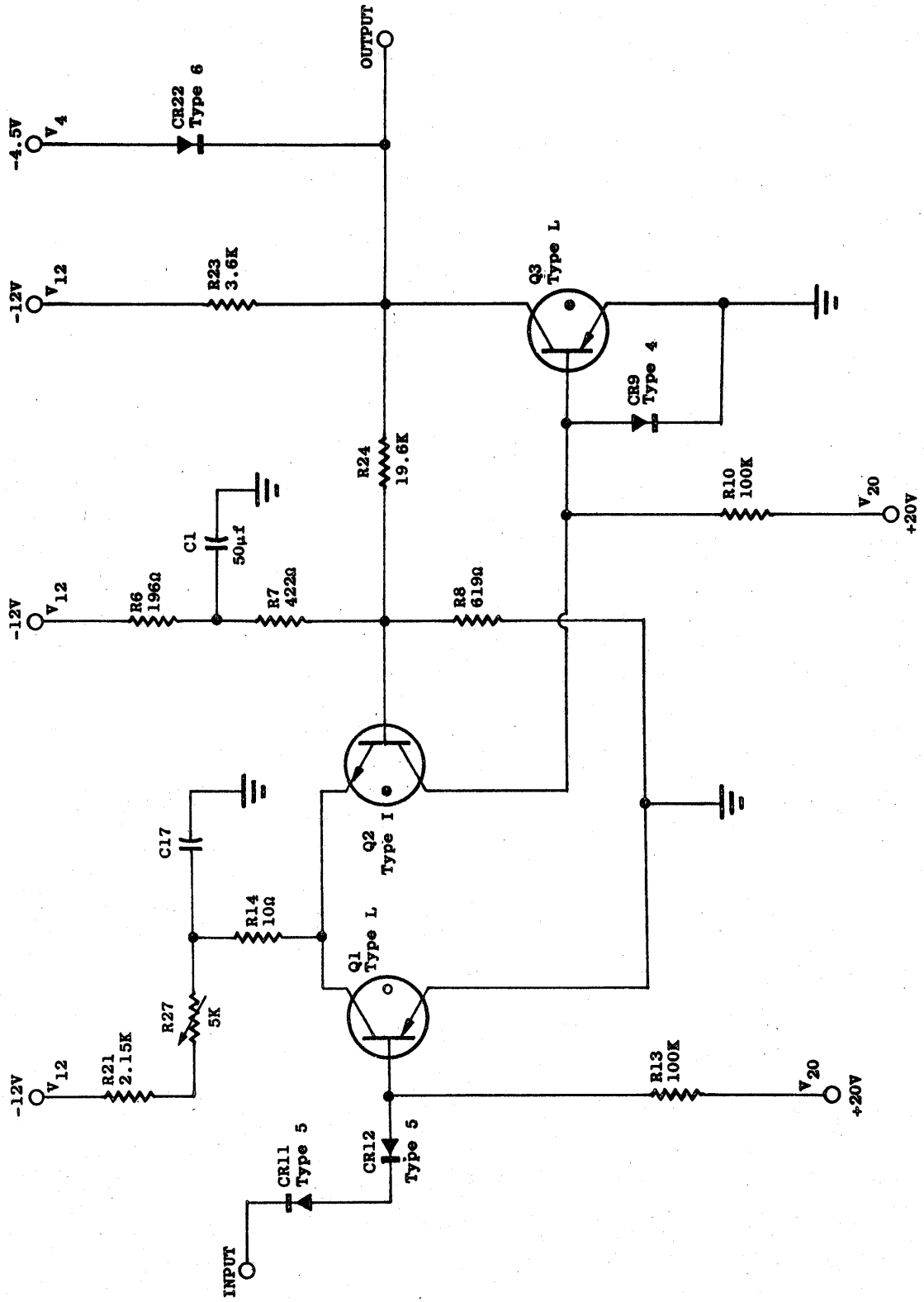


FIGURE 6.28-1. DELAY "C" CIRCUIT SCHEMATIC

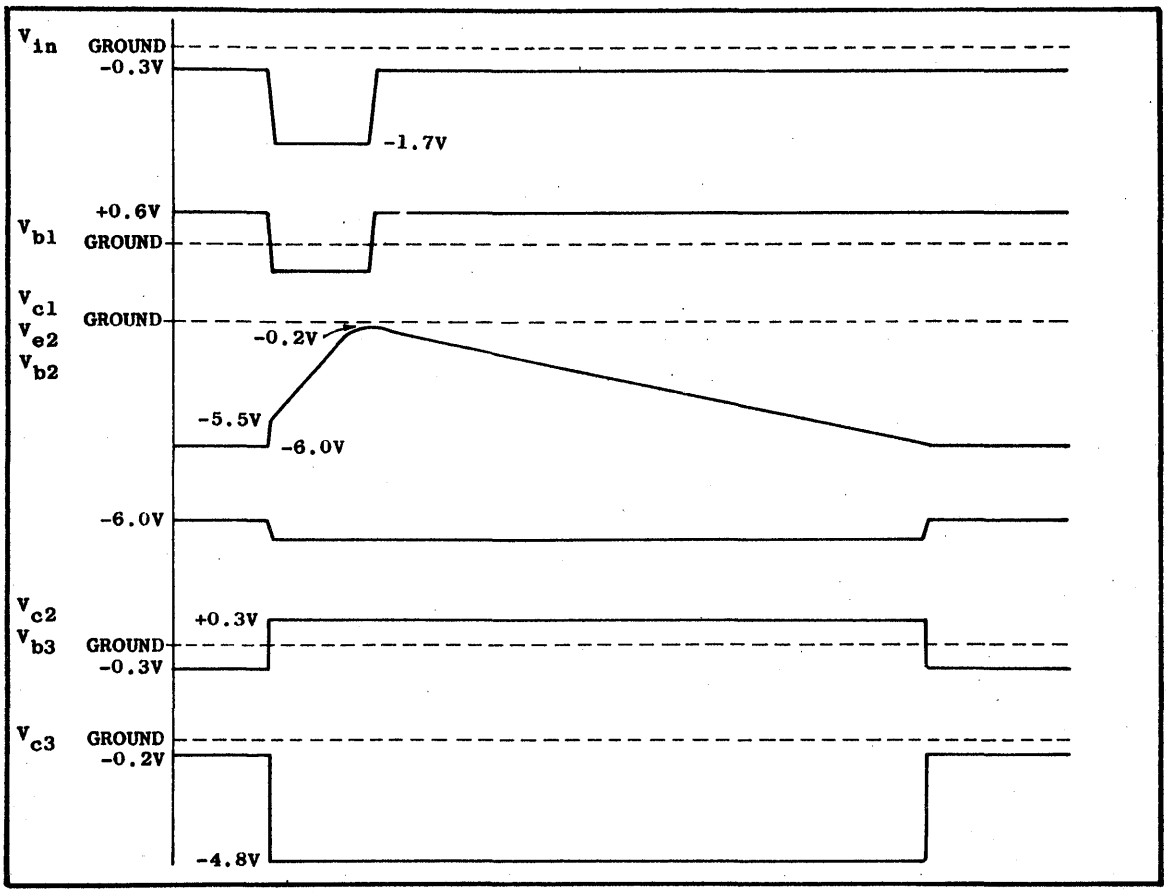
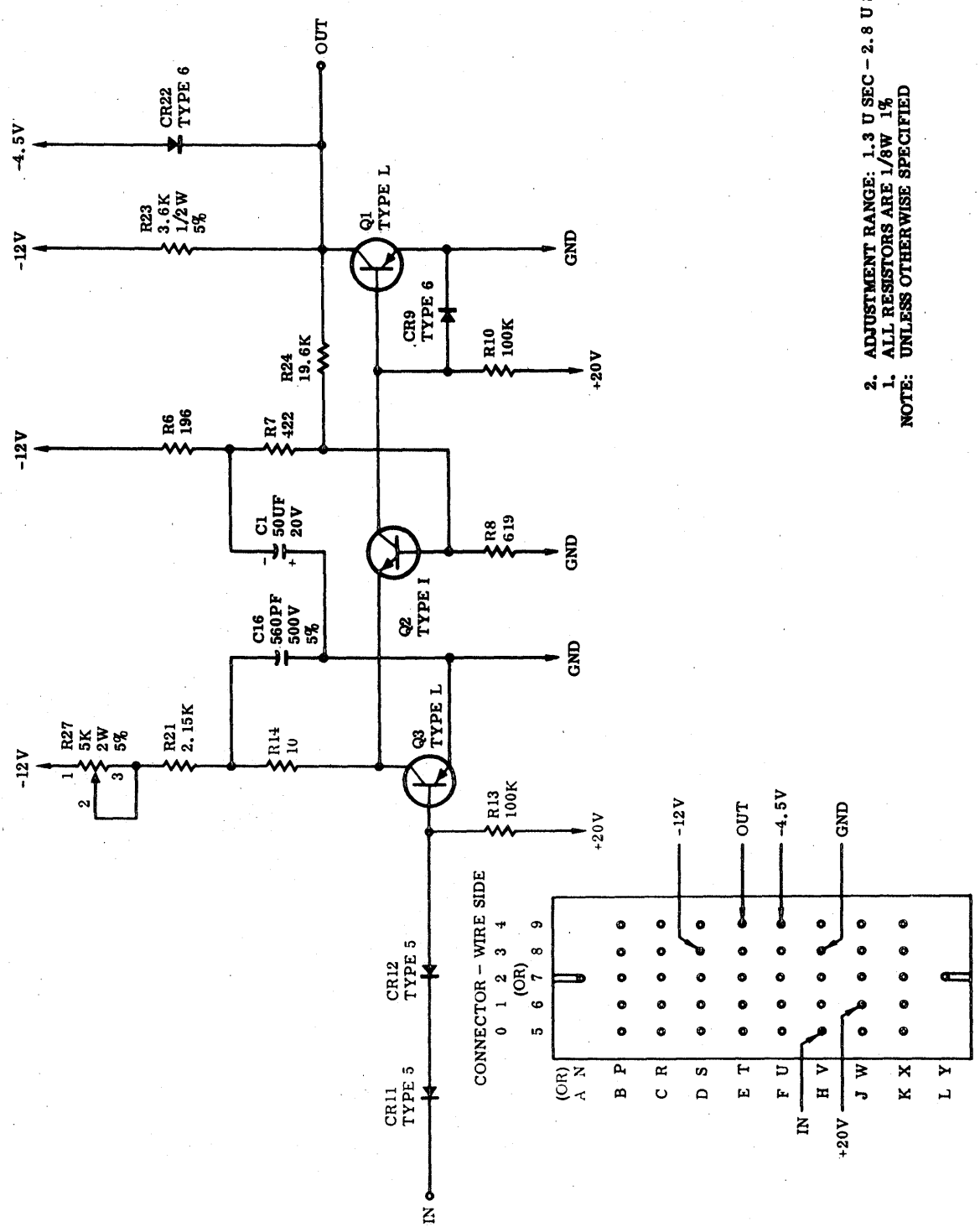


FIGURE 6.28-2. DELAY "C" TIMING

PACKAGE SCHEMATIC

Refer to Figure 6.28-3 for the complete schematic of the Delay "C" Parallel Plate Package.



2. ADJUSTMENT RANGE: 1.3 U SEC - 2.8 U SEC
1. ALL RESISTORS ARE 1/8W 1%
NOTE: UNLESS OTHERWISE SPECIFIED

FIGURE 6.28-3. DELAY "C" PACKAGE SCHEMATIC

6.29 MULTI

GENERAL DESCRIPTION

The Multi is a delay circuit of the "Multi" type which differs from most Multis in that no allowance need be made for reset time because the reset time is included in the delay.

When a negative pulse of 0.1 μs or greater width, and at least 1100 μamp magnitude is received at the input, the output is caused to go negative and will remain negative until a specified delay time after the application of the input pulse.

If a new input pulse is received before the reset portion of the delay begins, the pulse will not be accepted; the delay time will be measured from the application of the first pulse.

If an input pulse is received during reset time, the pulse will be accepted but will result in an unpredictable delay time.

If the logic allows an input to arrive during reset time, provision is made for inhibiting the input during this time by means of an external switch circuit driven by the output of the delay circuit. The length of the input pulse is not to be longer than the delay time minus the reset time in the first case, or longer than the delay time in the second.

Delay time is determined by the choice of one capacitor and by the adjustment of a potentiometer.

CIRCUIT DESCRIPTION

Refer to Figure 6.29-1 for Delay "B" Multi circuit schematic, and Figure 6.29-2 for Delay "B" Multi Timing.

INITIATION OF THE OUTPUT PULSE

In the quiescent state, Q1 is cut OFF, Q2 is conducting, and Q3 and Q4 are in saturation. At this time, the potential at the input is 0 to -1.1V. When a negative pulse equal to or greater than 400 μamp is applied to the input terminal, the potential will become more negative and lie in the range of -1.7V to -2.5V. It is prevented from going more negative by the base emitter diode Q1.

Q1 begins to conduct, causing the collector which has been resting at -6.0V, to start toward its saturation voltage of -0.3V. As soon as the collector of Q1 has moved 0.3V in the positive direction, Q2 will turn OFF because its emitter is tied to the collector of Q1. As soon as Q2 begins to turn OFF, the base of Q4 will go positive, causing Q4 to turn OFF and thus initiating the output pulse.

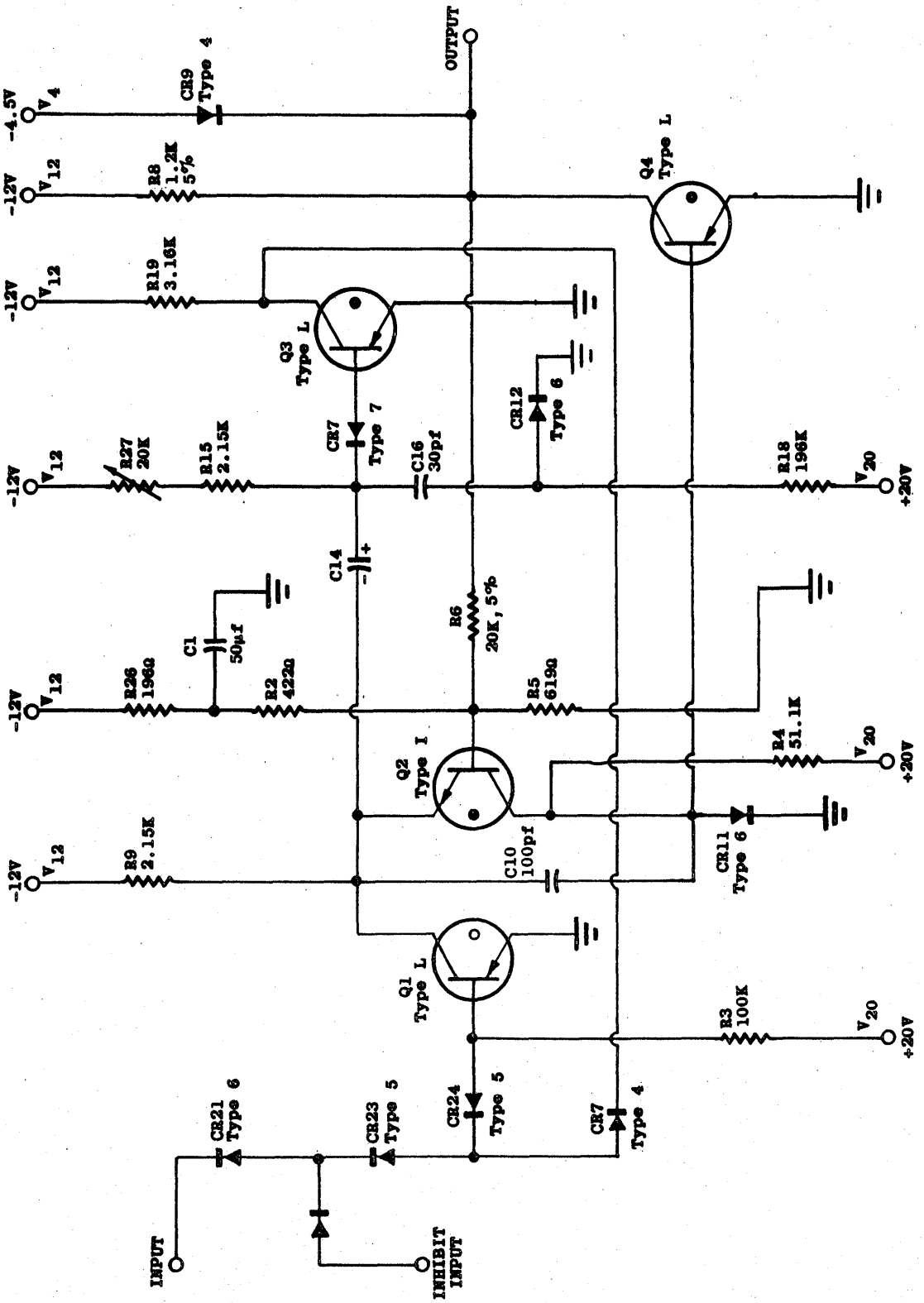


FIGURE 6.29-1. DELAY MULTI "B" CIRCUIT SCHEMATIC

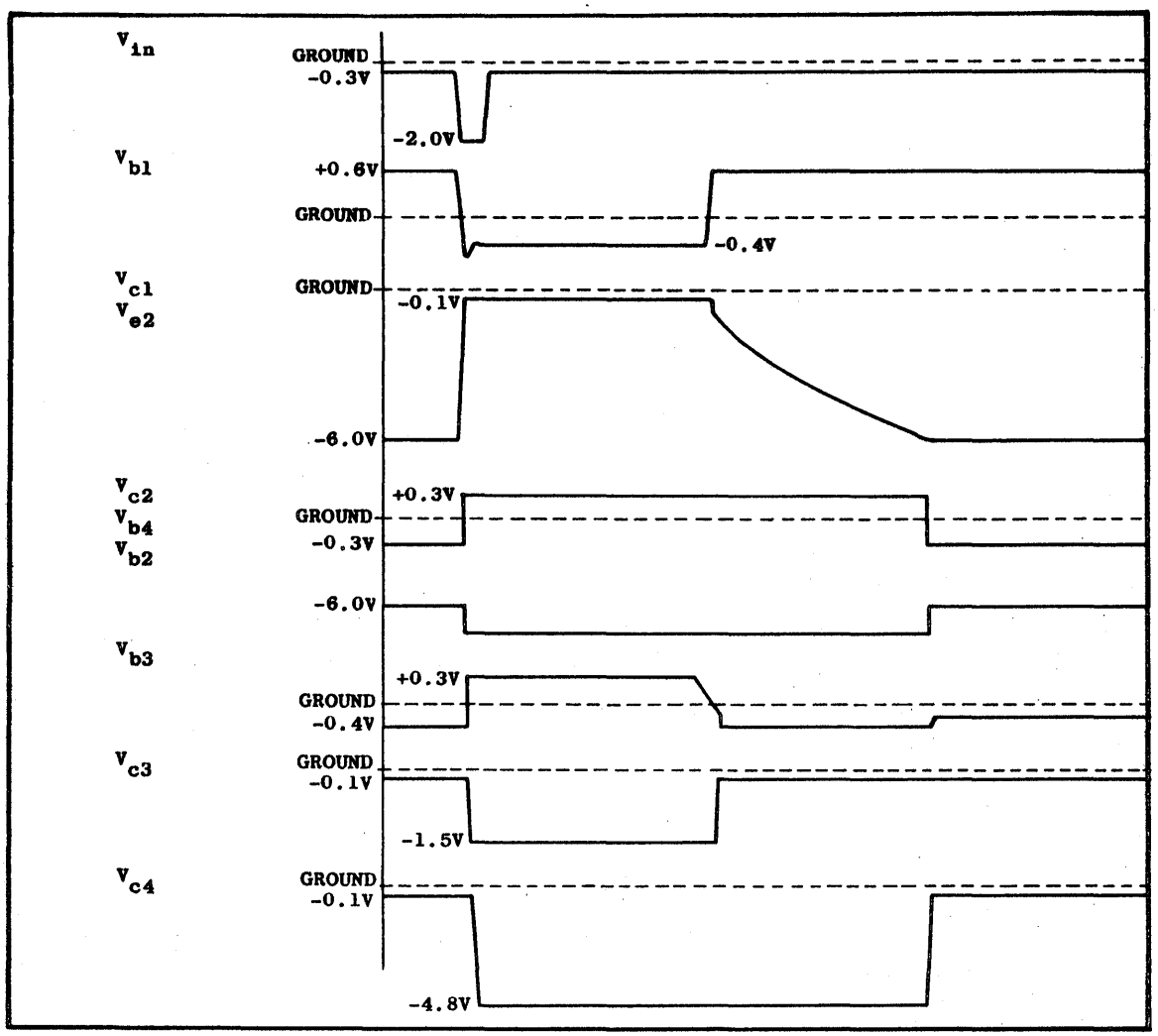


FIGURE 6.29-2. MULTI TIMING

THE DELAY HALF CYCLE

When the collector of Q1 goes toward ground, capacitor C14 cannot discharge instantaneously, so the base of Q3 is driven positive, resulting in the transistor being turned OFF.

When Q3 is turned OFF, the base of Q1 is held negative so that the collector of Q1 is brought to -0.3V and held there as long as Q3 is cut OFF.

The cathode of CR17 which is now at +6.0V, begins to move toward -12V as C14 is charged through R15 and R27. When this point begins to go negative, Q3 will begin to turn ON. When Q3 turns ON, Q1 will turn OFF (assuming that there is no input at this time).

THE RESET HALF CYCLE

When Q1 turns OFF, its collector starts toward -12V, being restrained by C14.

When the collector of Q1 reaches -6.0V, Q2 will begin to turn ON. When Q2 turns ON, Q4 will be turned ON, thus ending the output pulse.

The circuit is now ready to receive a new input and repeat the above cycle.

INHIBIT

The input is automatically inhibited during the time Q3 is OFF, but a separate inhibit input has been provided to prevent triggering during the reset time if this is desirable.

The complete inhibit circuit was not included in this package because in most cases, no pulses would be received during this time. The use of this inhibit input with an external switch is shown in Figure 6.29-3.

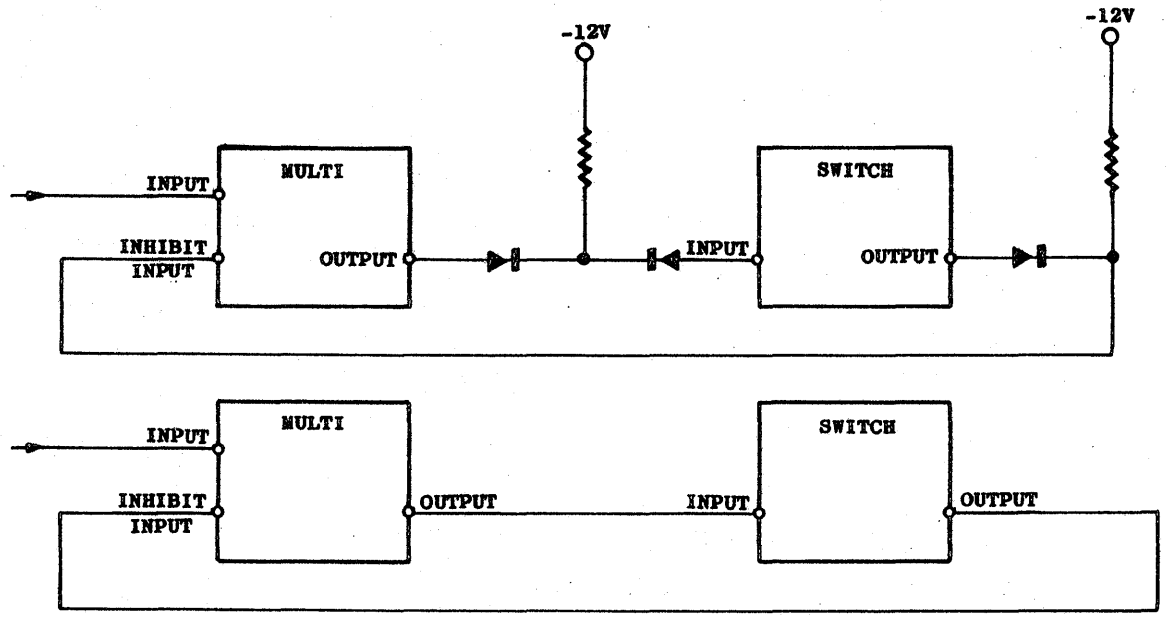


FIGURE 6.29-3. POSSIBLE CONNECTIONS FOR INHIBIT CIRCUIT

The true output from the multi circuit produces a false output from the switch, which when applied to the inhibit input (a shunt AND) prevents an input from reaching the base of Q1.

PACKAGE SCHEMATIC

Refer to Figure 6.29-4 for the complete schematic of a Multibrator Parallel Plate Package.

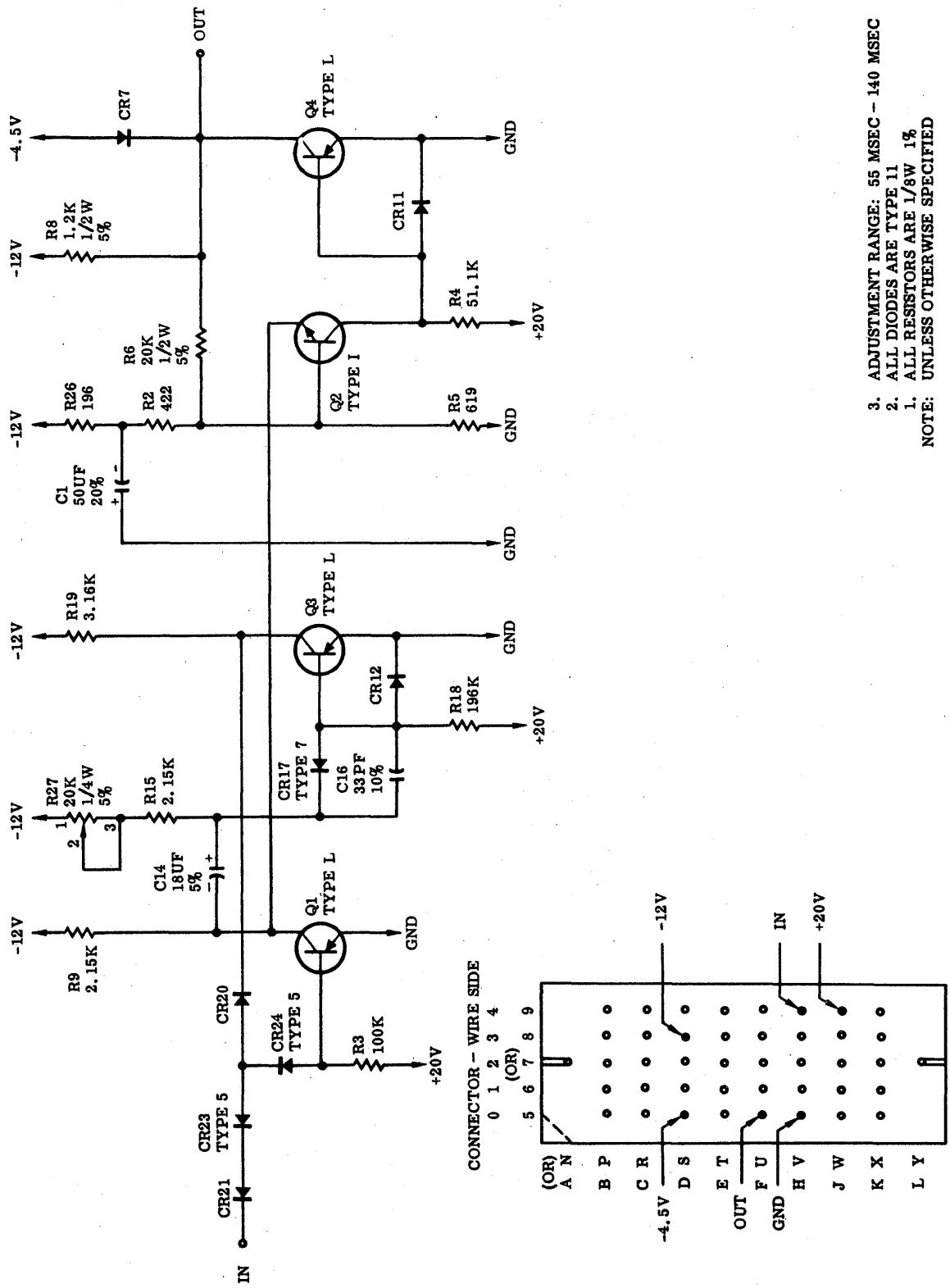


FIGURE 6.29-4. MULTIVIBRATOR PACKAGE SCHEMATIC

6.30 COMPRESSOR

GENERAL DESCRIPTION

The Compressor is a circuit which produces an output pulse of about 0.400 μs when an input pulse longer than 1 μs is received.

The output of the circuit is primarily meant to trigger a flip-flop.

BASIC CIRCUIT

Refer to Figure 6.30-1.

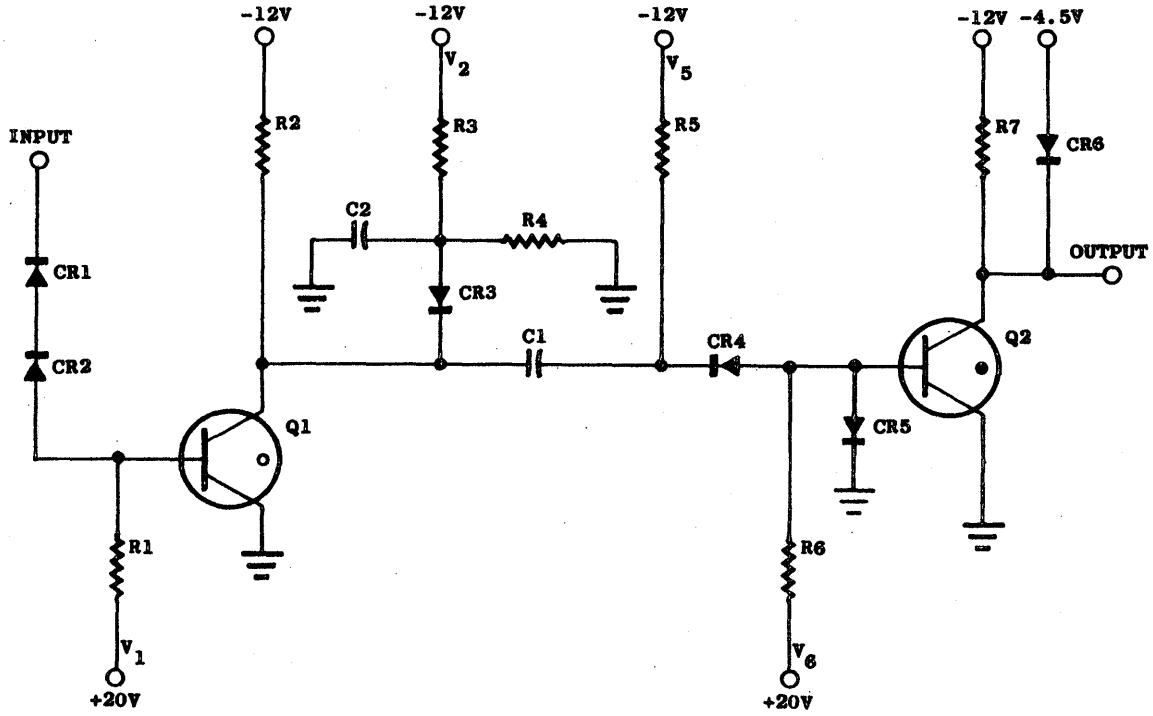


FIGURE 6.30-1. COMPRESSOR CIRCUIT SCHEMATIC

The circuit is basically a monostable multivibrator, except for the fact that no feedback is used since the input pulse is longer than the desired output pulse.

In its stable state, Q1 is OFF, and Q2 is ON. For a false input, the output is false. For a true input pulse of duration longer than 1 μs, there will be a true output pulse of approximately 0.400 μs. The input must be of a minimum length, and the output will never be longer than the input.

The width of the output pulse actually produces ranges from 0.340 μs to 0.450 μs. A reset time of 0.400 μs is required.

OPERATION

Refer to Figure 6.30-1 for Compressor circuit schematic, and to Figure 6.30-2 for Compressor waveforms.

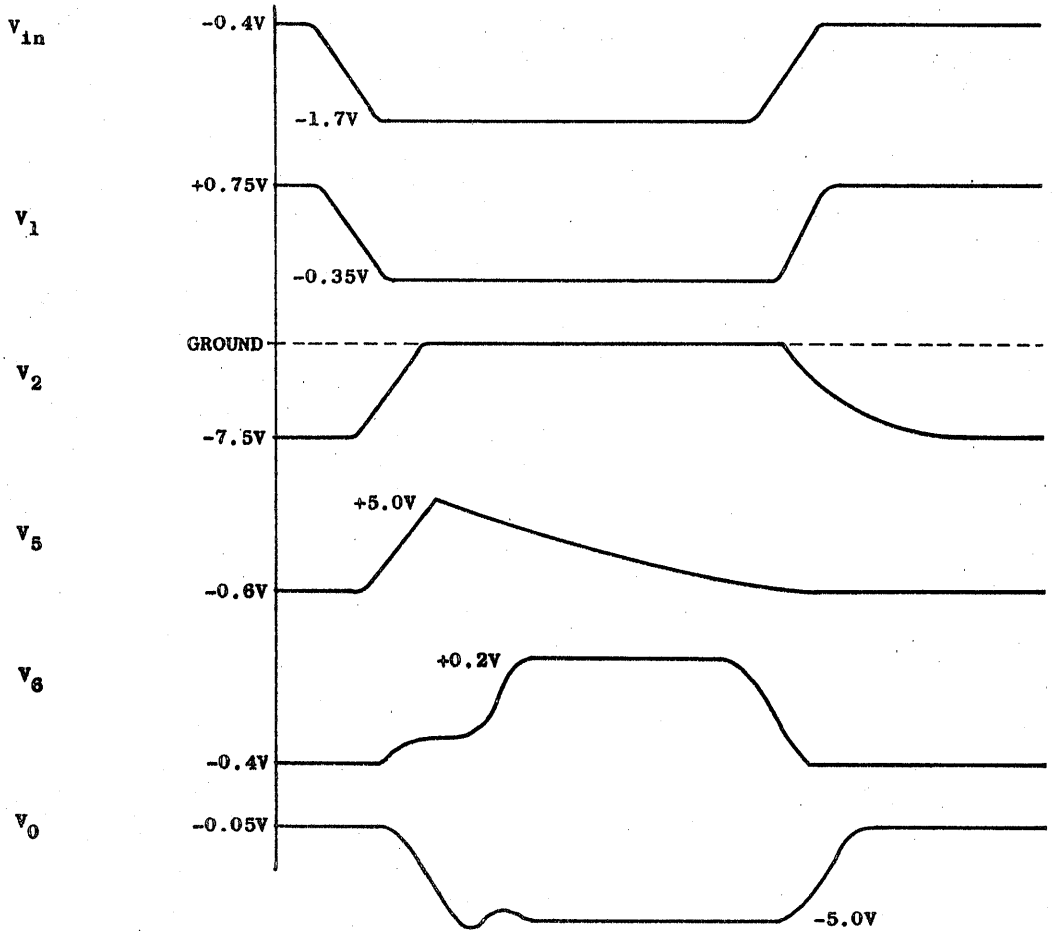


FIGURE 6.30-2. COMPRESSOR WAVEFORMS

BEGINNING OF CYCLE

In the quiescent state, Q1 is OFF and Q2 is ON. At this time, the input voltage is -0.2V to -1.0V. When a true input pulse is applied, transistor Q1 will turn ON. The potential at the input will be in the range of -1.3V to -2.0V. It will not be any more negative because of the clamping action of Q1, CR1 and CR2. As Q1 is turned ON, its collector will swing from a potential of about -7.0V to about -0.2V. V_5, normally at about -0.6V, now rises through capacitor C1 to a potential of about +5.0V.

DURATION OF OUTPUT

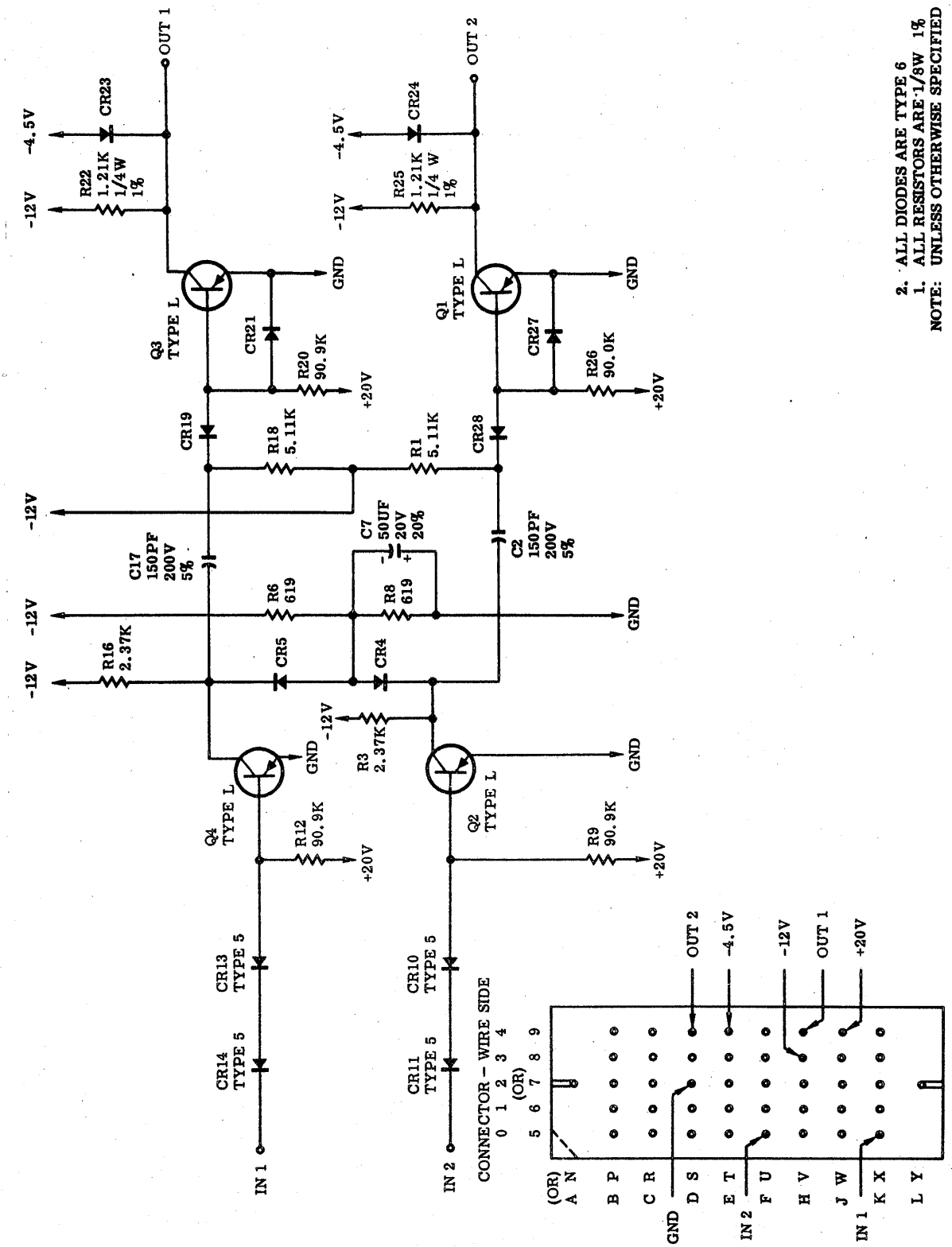
As soon as V_5 becomes more positive than -0.6V, Q2 starts turning OFF and the stored charges in CR4 and the base of Q2 just about cancel out. The time during which V_5 is greater than -0.6V is mainly determined by the RC combination of C1 and R5. The output of the circuit is true during this same time, minus the rise time, plus the fall time.

RESET

At the end of the input pulse when V_{in} reaches -1.0V in the positive direction, Q1 is turned OFF, but V_2, the voltage at the collector of Q1, cannot change instantly from about -0.2V to about -7.0V. The reset time is determined by the RC combination of R2 and C1. The minimum duration of a complete cycle is equal to the length of the input pulse plus the reset time.

PACKAGE SCHEMATIC

Refer to Figure 6.30-3 for the complete schematic of the Compressor Parallel Plate Package.



NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/8W 1%
2. ALL DIODES ARE TYPE 6

FIGURE 6.30-3. COMPRESSOR PACKAGE SCHEMATIC

6.31 PULSE SYNCHRONIZER

GENERAL DESCRIPTION

The Pulse Synchronizer is a circuit which synchronizes a pulse with a level.

There are two inputs to the circuit. One input is a negative going clock pulse of a given width and frequency, and the other is a negative going logical level whose maximum width or frequency is not specified. However, the minimum duration of the logical level must be such that it overlaps at least two clock pulses. A certain minimum reset time must be allowed to elapse between two consecutive logical levels.

The output is true only when both inputs are true and there is only one negative going output pulse for every logical level input. The output pulse starts after the clock pulse has completed and it (output pulse) brackets one and only one input clock pulse. Refer to Figure 6.31-1.

GENERAL OPERATION OF THE CIRCUIT

Since there must be only one input pulse for every time both inputs are true, the circuit consists of three stages.

1. To trigger the circuit with the trailing edge of the clock pulse when both inputs are true.

2. The second stage holds the circuit from triggering again with another clock pulse for the same logical level input.

3. There is a timing circuit which controls the width of the output followed by the third and final stage.

CIRCUIT DESCRIPTION

Refer to Figure 6.31-1.

When both the level and clock are false, transistors Q1 and Q3 are in saturation, and Q2 is cut OFF.

When the clock pulse becomes true, Q1 may be driven harder. However, when the clock pulse terminates, Q1 will be cut OFF by the stored charge in C1. If the level input is false, Q2 will remain cut OFF. However, if the level input is true when Q1 is cut OFF, Q2 will be turned ON and the positive voltage at P_1 will be coupled to the base of Q3, turning it OFF. The output pulse width is dependent upon the RC time constant of C3 and R8. This time must be more than 1 μs, but less than 2 μs. Since point P_1 is fed back to the input, when P_1 goes positive (false) Q1 will be held off and Q1 is turned ON.

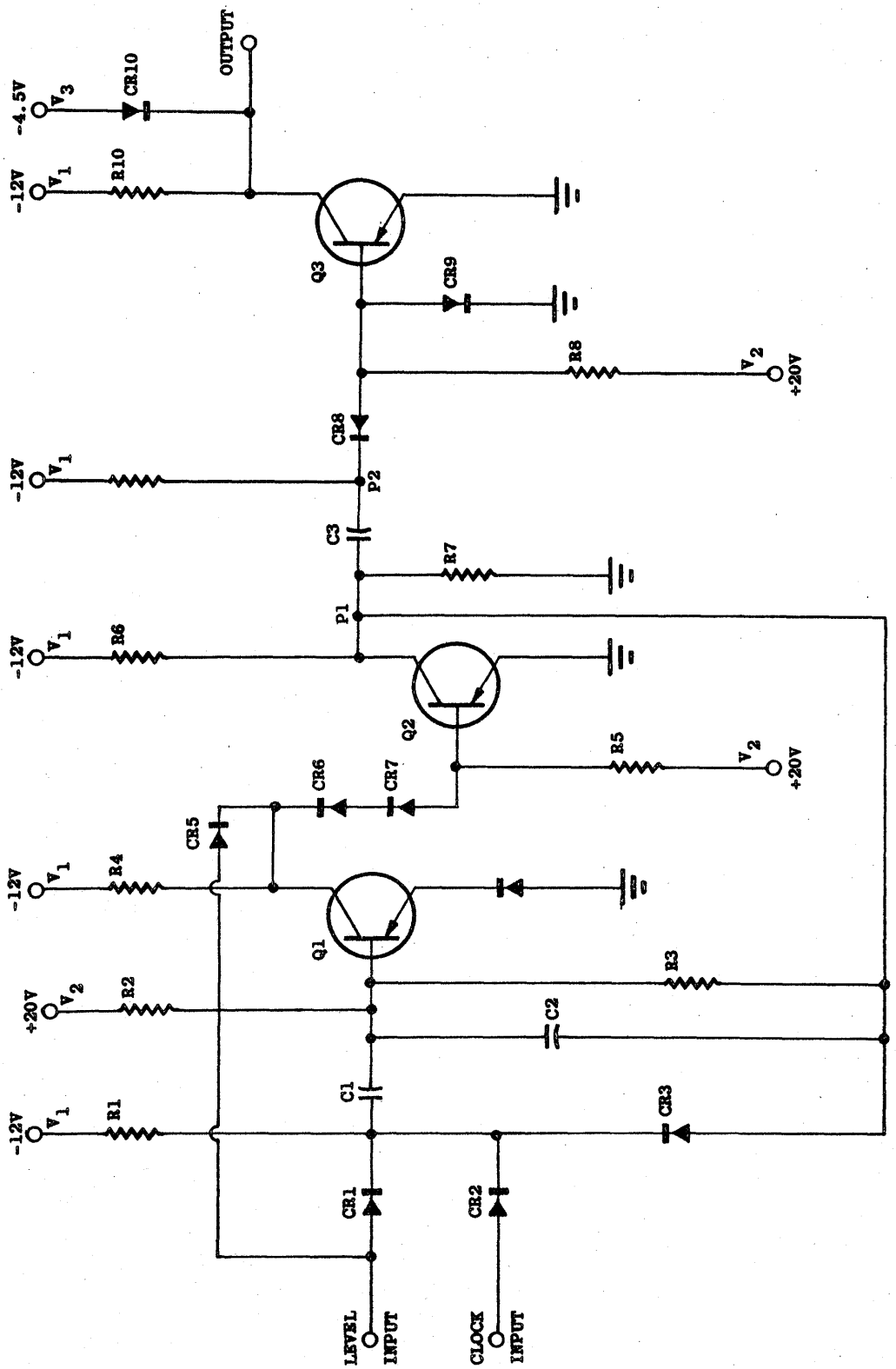


FIGURE 6.31-1. PULSE SYNCHRONIZER CIRCUIT SCHEMATIC

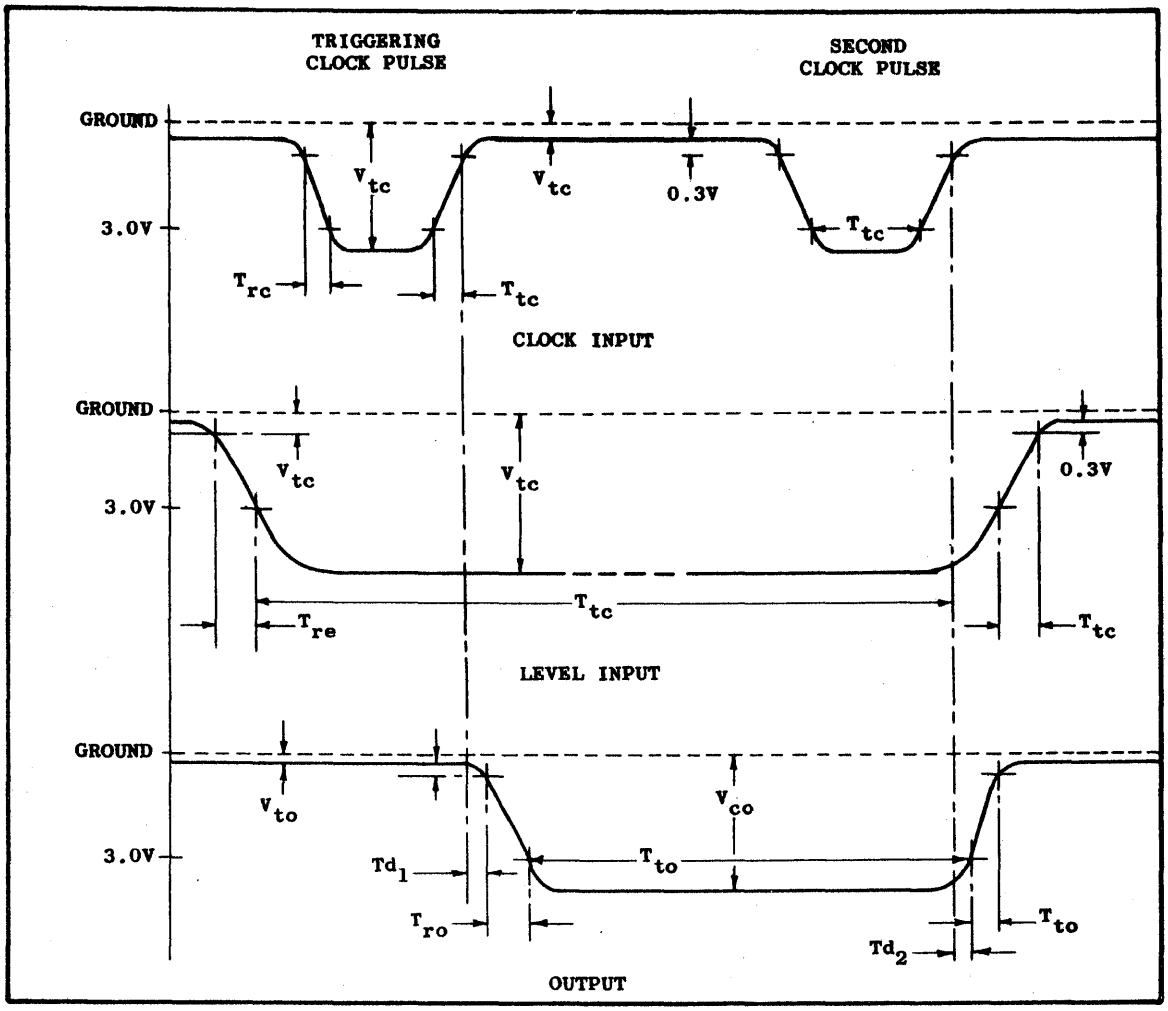


FIGURE 6.31-2. PULSE SYNCHRONIZER TIMING

PACKAGE SCHEMATIC

Refer to Figure 6.31-3 for the complete schematic fo the Synchronizer Parallel Plate Package.

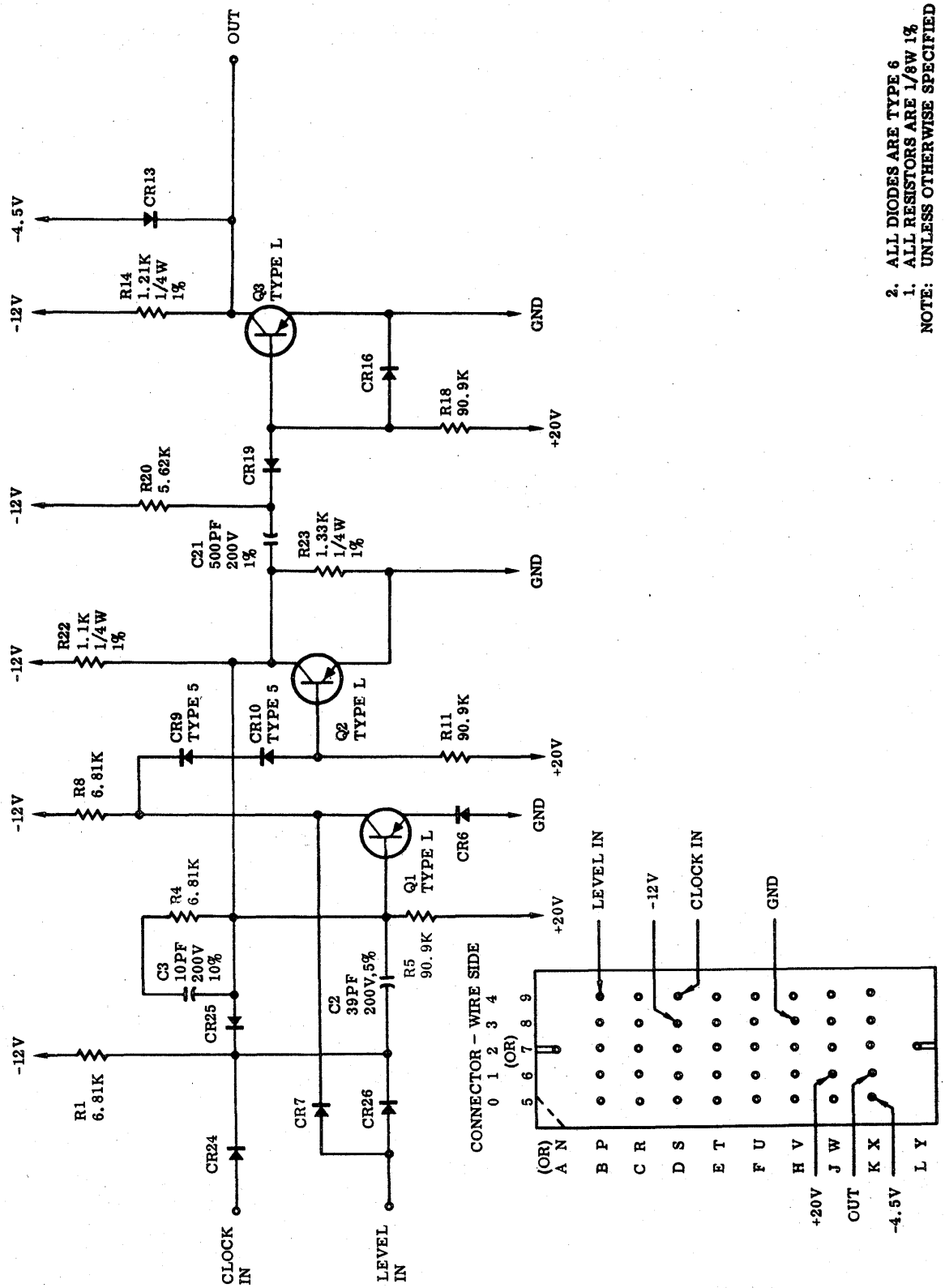


FIGURE 6.31-3. PULSE SYNCHRONIZER PACKAGE SCHEMATIC

6.32 CLOCK OSCILLATOR & SQUARING AMPLIFIER

GENERAL DESCRIPTION

The Clock Oscillator and Squaring Amplifier consists of two circuits; one which generates the 1 megacycle Master Clock sine wave signal, and one which shapes the sine waves into square wave output pulses.

The oscillator circuit is a crystal controlled oscillator with a basic frequency of 1 megacycle. The circuit is so packaged that the crystal may be shorted out of the circuit thus converting the circuit to a Variable Frequency Oscillator for maintenance purposes.

The Squaring Amplifier circuit uses the positive peak to negative peak slope of the oscillator sine wave to produce a negative output pulse having a frequency of 1 megacycle with a width of 0.43 to 0.48 μs.

CIRCUIT DESCRIPTION

Refer to Figure 6.32-1 for circuit schematic and to Figure 6.32-2 for Timing.

Transistor Q3 and Q4, crystal X37 and the tank circuit L36 and C4 make up the basic oscillator circuit. Q3 and Q4 are both biased into conduction. When power is applied to the circuit, the crystal X37 will be shocked into oscillation. The AC voltage developed across the crystal is coupled through C2 and R35 to the emitter of Q3. This voltage on the emitter results in a pulsating Q4 emitter current which develops an AC voltage across R23, which supplies positive feedback to the crystal to maintain oscillation.

Capacitor C20 and diodes CR18 and CR19 make up a gain limiter, limiting the voltage applied to the base of Q4, plus providing a more symetrical sine wave at the base of Q4.

Capacitor C2 provides DC isolation to the crystal X37.

R35 provides a means of adjusting the gain of the circuit.

Transistor Q5 and its associated circuit comprise the Squaring Amplifier circuit. Q5 is normally ON. The change from a positive to a negative peak of the sine wave applied to the base of Q4, causes Q4 to conduct more. Part of this greater collector current flows through C14, R13 and CR15, resulting in a positive potential on the base of Q5 cutting it OFF. Q5 remains cut OFF until the signal on the base of Q4 has nearly reached its peak in the negative direction, resulting in a negative pulse to be developed at the collector of Q5. This method of deriving a square wave pulse from a sine wave results in a constant width pulse of 0.43 to 0.48 μs, regardless of the amplitude of the sine wave.

The negative potential at the collector of Q5 when it is cut OFF, is applied to the bases of the two emitter followers Q2 and Q1. The emitters follow the bases providing a negative pulse of -4.5V at outputs 1 and 2.

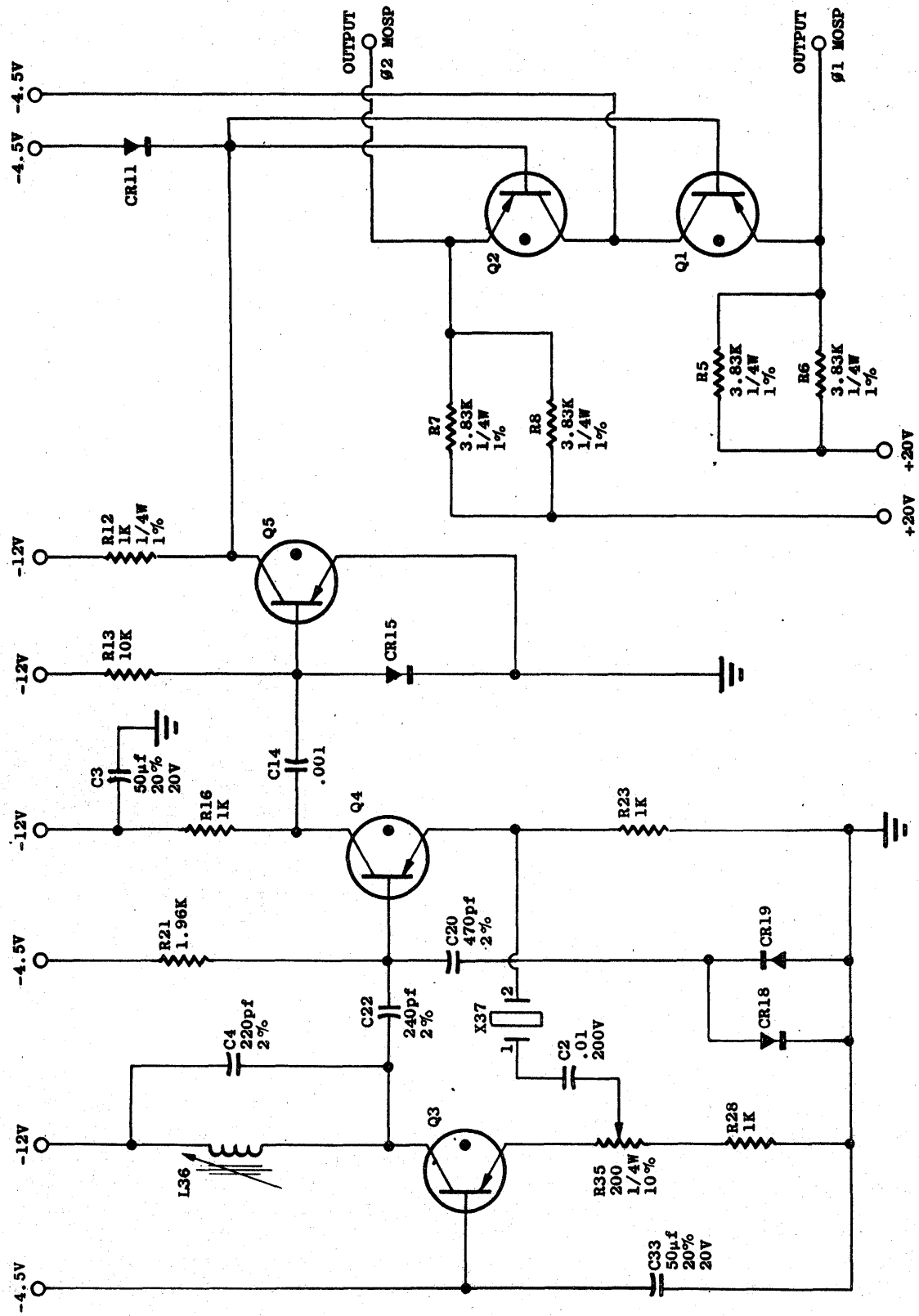


FIGURE 6.32-1. CLOCK OSCILLATORY SQUARING AMPLIFIER CIRCUIT SCHEMATIC

Output 1 is used to trigger the BO and Line Drivers and output 2 is used in the Clock Control circuitry of Central Control.

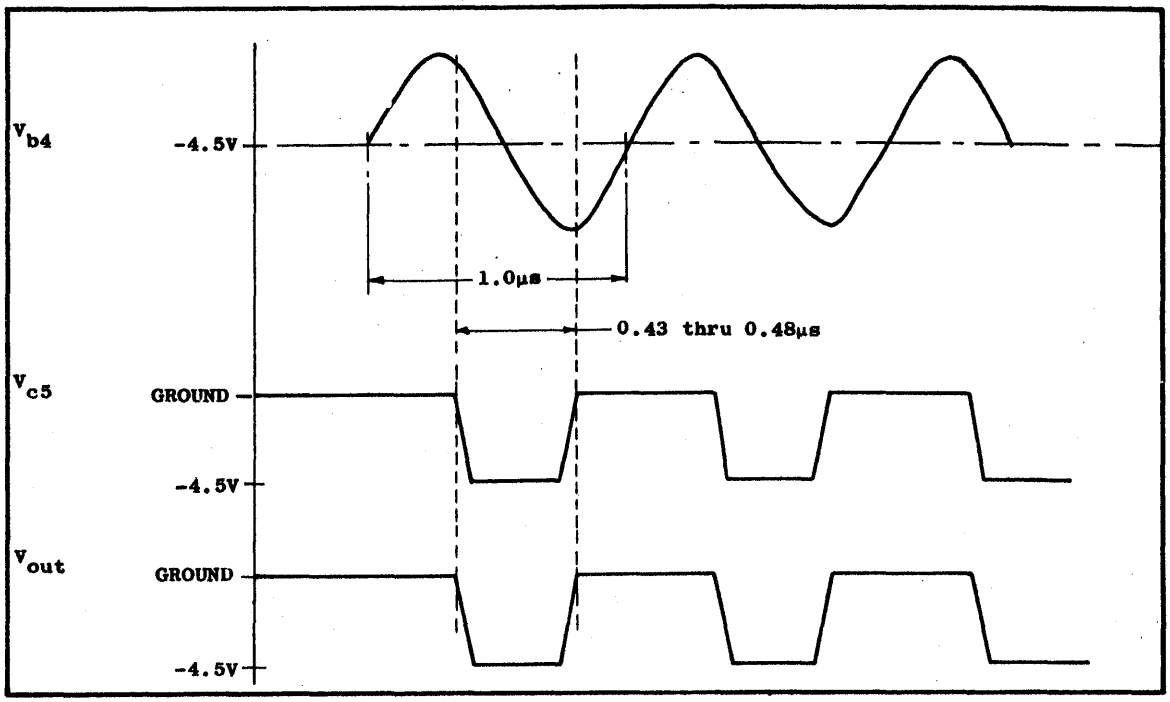


FIGURE 6.32-2. CLOCK OSCILLATOR AND SQUARING AMPLIFIER TIMING

VARIABLE FREQUENCY OSCILLATOR OPERATION

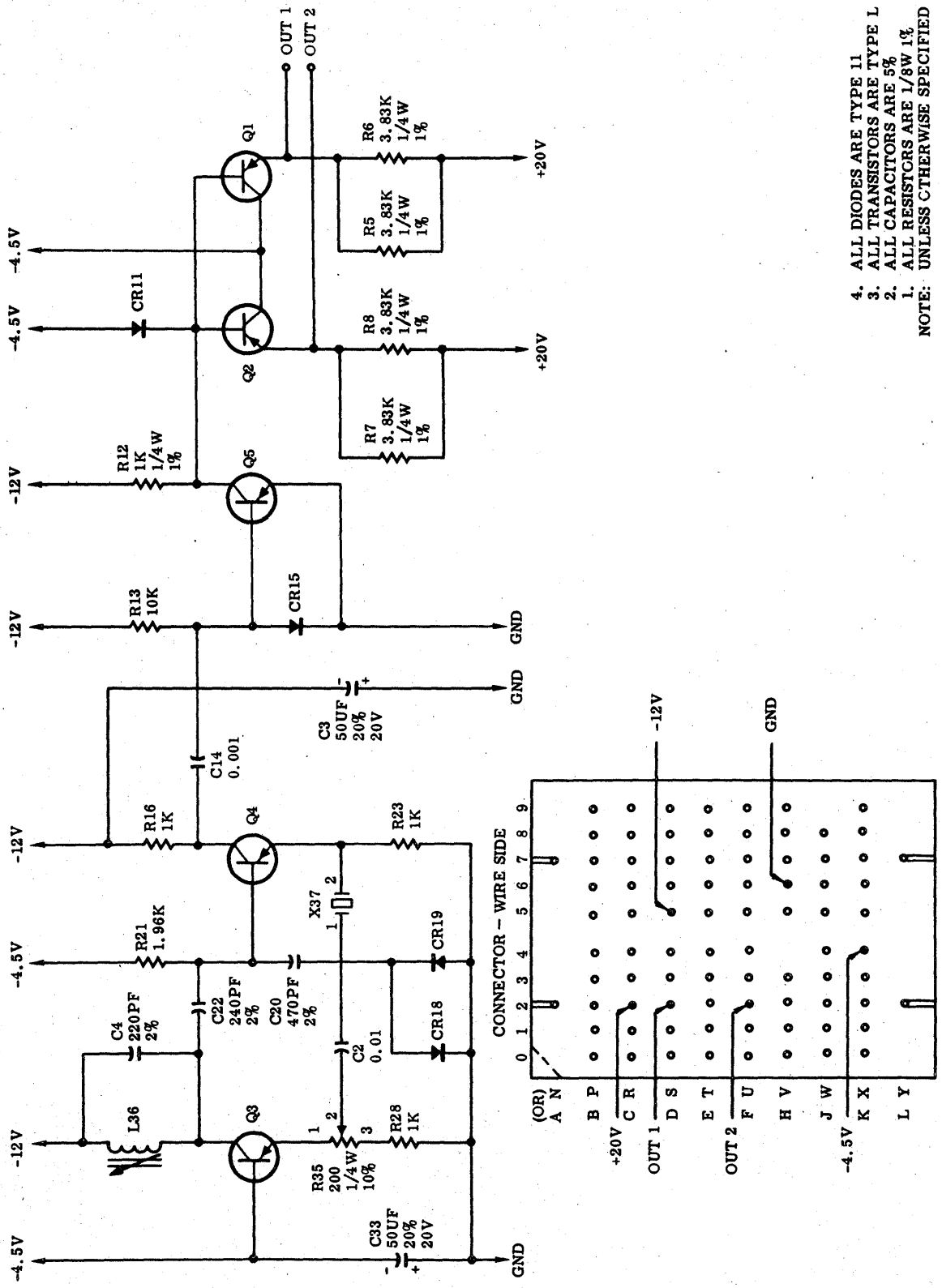
The oscillator circuit may be converted to a variable frequency oscillator for maintenance purposes by shorting out crystal X37. Without the crystal in the circuit, the oscillator is dependent upon the tuned tank circuit, L36 and C4, to determine the frequency of oscillation. Therefore, by varying the inductance L36, the circuit will oscillate over a frequency range of 400 kc from 800 kc to 1.2 megacycles.

Potentiometer R35 provides a means of adjusting the gain of the circuit. When using the circuit as a variable frequency oscillator, it may be necessary to increase the gain to obtain stable operation when tuned near the limits of the frequency range.

When returning the circuit to normal by removing the short from across X37, it is necessary to tune the tank circuit to 1 megacycle prior to removing the short.

PACKAGE SCHEMATIC

Refer to Figure 6.32-3 for the complete schematic of the Clock Oscillator and Squaring Amplifier Parallel Plate Package.



NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/8W 1%
2. ALL CAPACITORS ARE 5%
3. ALL TRANSISTORS ARE TYPE L
4. ALL DIODES ARE TYPE 11

FIGURE 6.32-3. CLOCK OSCILLATOR AND SQUARING AMPLIFIER PACKAGE SCHEMATIC

6.33 BLOCKING OSCILLATOR AND LINE DRIVER

GENERAL DESCRIPTION

The Blocking Oscillator and Line Driver is a circuit used in conjunction with the Clock Oscillator and Squaring Amplifier to produce a 1 megacycle clock pulse having a width of 0.155 μs. The Line Drivers drive the clock lines going to all units requiring these pulses.

CIRCUIT DESCRIPTION

Refer to Figures 6.33-1 and 6.33-2.

In the quiescent state, Q7, Q4 and Q1 are cut OFF. Q6, Q2, Q3, Q5 and Q8 are conducting.

The input to Q7 consists of a level (Inhibit IN) and a negative pulse from the Clock Oscillator and Squaring Amplifier (IN). The inhibit level is false until such time that the start, load or single pulse switch is depressed. When any of these three switches are depressed, a true level is applied at the Inhibit IN terminal. This level along with a negative clock pulse at the IN terminal will bias Q7 into conduction.

R23 limits the emitter current of Q7 when the input is true. The collector of Q7 in the quiescent state has a +10.0V bias applied to it due to the voltage divider R20 and R21 between ground and +20V. When A7 begins to conduct, the collector will start to go negative towards its saturation voltage, causing current to flow through C28, thus supplying base drive to Q4 to turn it ON. The turning ON of Q4 provides a current path for Q1 emitter current, resulting in turning ON Q1.

The base of Q1 is held at a constant -6.0V due to the voltage divider R1 and R34 between ground and -12V. This constant voltage on the base of Q1 results in a constant Q1 emitter current as long as Q4 and Q1 are held ON. When Q1 turns ON, a 6.0V potential is placed across the primary of the constant voltage switching transformer (T28).

Q1 collector current will begin to flow and to increase linearly through T38 inducing a voltage in the secondary and feedback windings of T38. The voltage induced in the secondary cuts OFF Q6. The voltage induced in the feedback winding continues to supply base drive to Q4 to hold it ON. When the collector current has increased to such a value that it equals the constant emitter current, the field across the primary of T38 collapses, removing base drive to Q4, cutting it OFF along with Q1, and turning Q6 ON again.

The circuit and T38 are so designed as to allow a pulse of 0.155 μs duration to be produced during the time Q4 and Q1 are ON. R37 provides a means of accurately adjusting the width of the pulse. CR2 and R3 provide a damping network across the primary of T38.

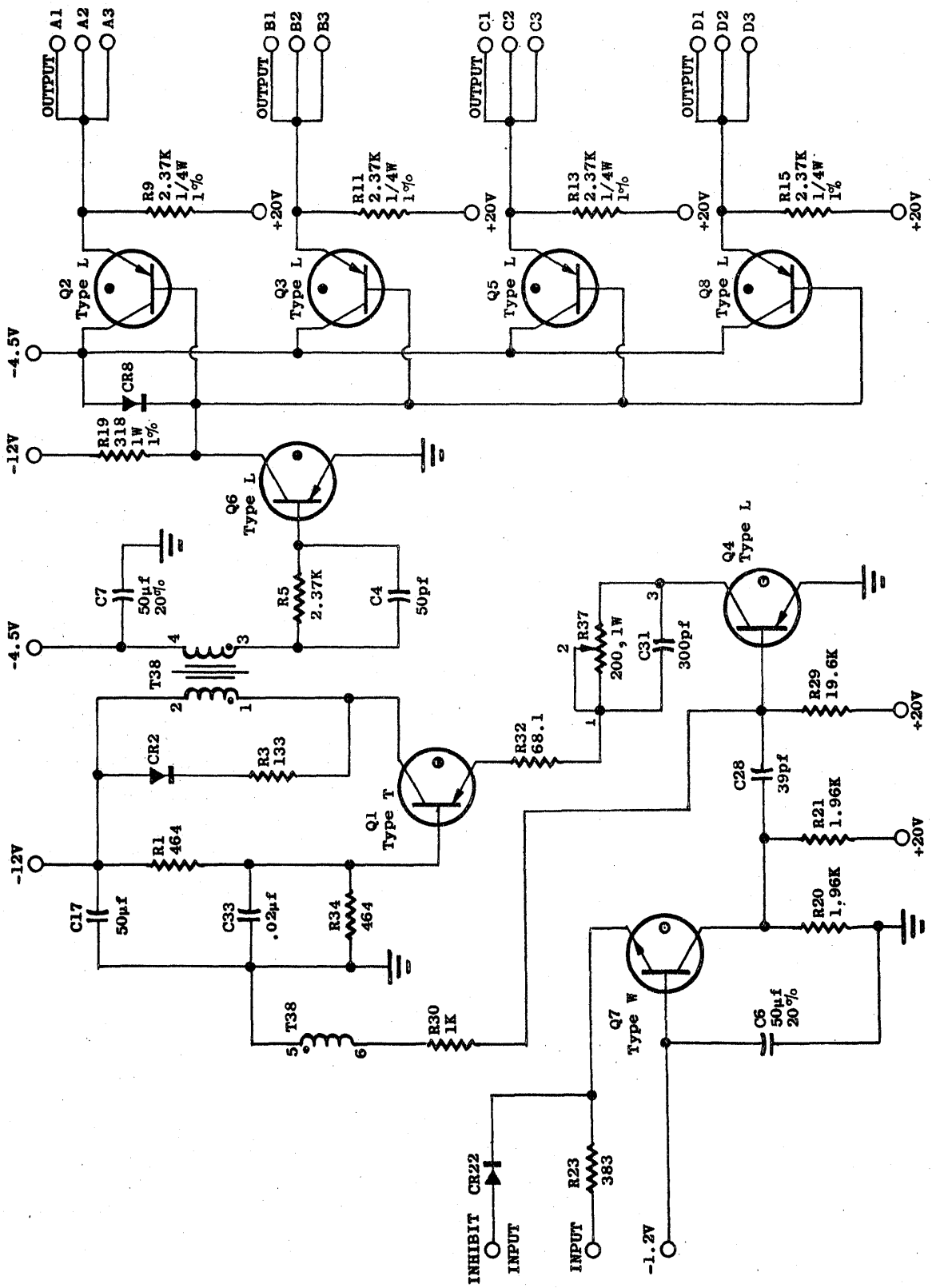


FIGURE 6.33-1. BLOCKING OSCILLATOR AND LINE DRIVER CIRCUIT

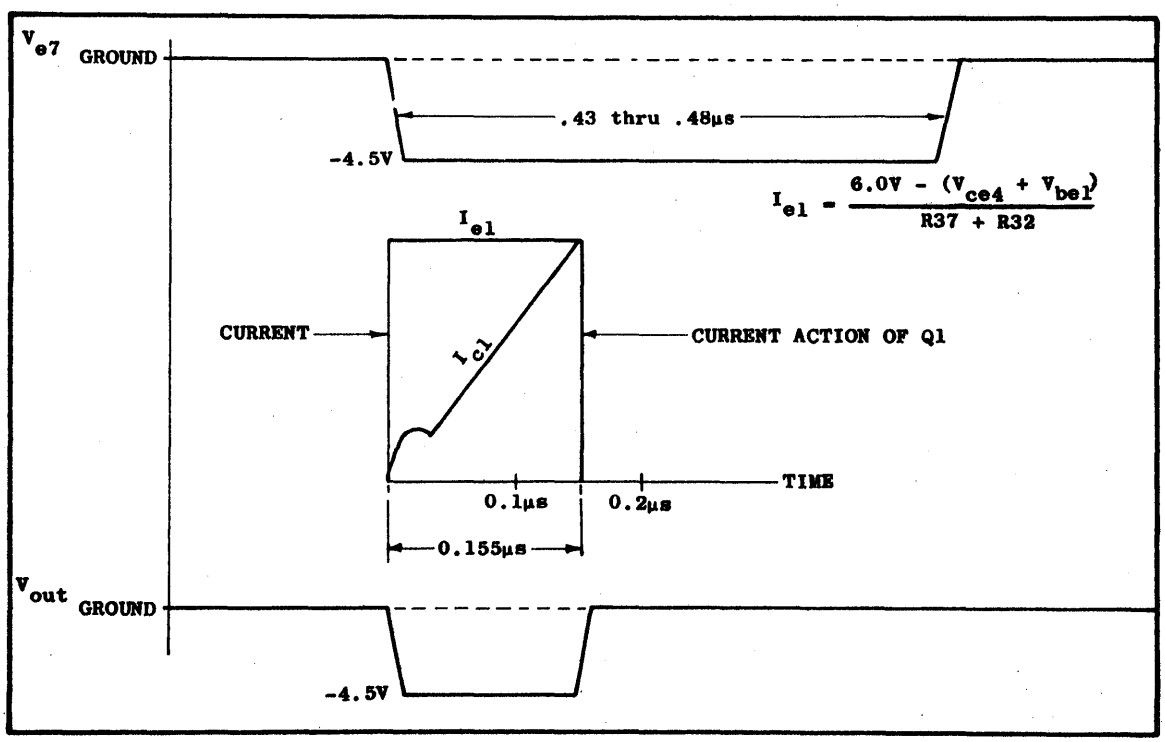


FIGURE 6.33-2. BLOCKING OSCILLATOR AND LINE DRIVER TIMING

When Q6 is cut OFF by the induced voltage in the secondary of T38, its collector starts toward its cut OFF potential of -12V. CR8, however, prevents it from reaching -12V by clamping it to -4.5V. The -4.5V potential is applied to the bases of the emitter followers Q2, Q3, Q5 and Q8. The emitters follow this potential resulting in a -4.5V pulse of 0.155 μs width to be sent out via cables to all units requiring the clock pulses from the output terminals A1 through D3.

PACKAGE SCHEMATIC

Refer to Figure 6.33-3 for the complete schematic of the Blocking Oscillator and Line Driver Parallel Plate Package.

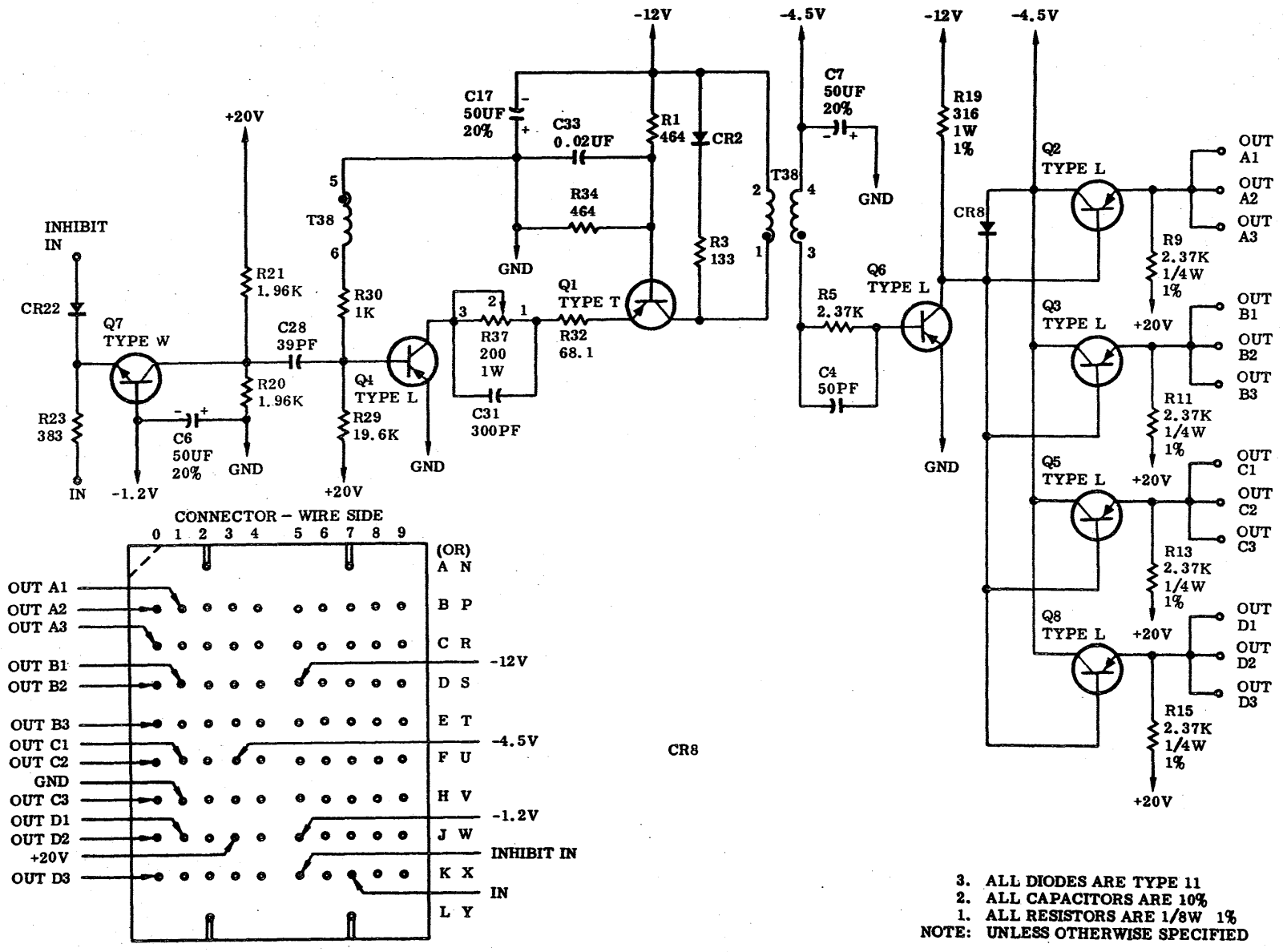


FIGURE 6.33-3. BLOCKING OSCILLATOR AND LINE DRIVER PACKAGE SCHEMATIC

6.34 DIRECT-COUPLED LOCAL CLOCK DRIVER AND VARIABLE BIAS

GENERAL DESCRIPTION

The Direct-Coupled Local Clock Driver is a circuit centrally located in each panel of each gate of every unit requiring clock pulses. Its function is to distribute the clock pulses sent via cables from the BO and Line Driver package in Central Control to the individual circuits on a panel. It also isolates the loads of these circuits from the clock cables.

CIRCUIT DESCRIPTION

Refer to Figure 6.34-1.

In the quiescent state, Q1 and Q2 are cut OFF. Q3, Q4 and Q5 are conducting.

When a negative clock pulse is applied to the input between T/P Input and T/P Ground Input, Q1 will be turned ON. R8 provides termination for this pulse.

The turn ON of Q1 results in its collector going negative towards its saturation potential, supplying base drive to Q2 turning it ON.

When Q2 turns ON, its collector starts toward its saturation potential, removing the base drive from Q3, Q4 and Q5, cutting them OFF. This action results in a -4.5V clock pulse at outputs 1 through 6 being made available to be used by the circuits within the unit.

Diodes CR35, CR30, CR39 and CR27, clamp the outputs at -4.5V.

VARIABLE BIAS

In the flip-flop circuit, the clocked inputs see the gated circuits as a load if the diodes between the clock line and the gated levels are not back biased. This would normally be the case since the gated inputs will tend to be at a lower level than the clock lines due to the drop through the cascading of gating diodes. The leakage would load the clock driver to a greater extent than necessary. Therefore, the false level from the Local Clock Driver is adjusted sufficiently negative by the variable bias input, to back bias the flip-flop gating diodes, reducing the current and loading caused by it.

This variable bias is in the range of -0.5V to -0.8V and is applied to the two paralleled bias terminals from a variable bias package. There is a variable bias package associated with each Local Clock package.

PACKAGE SCHEMATIC

Refer to Figure 6.34-2 for the complet ect-Coupled Local Driver Parallel Plate Package.

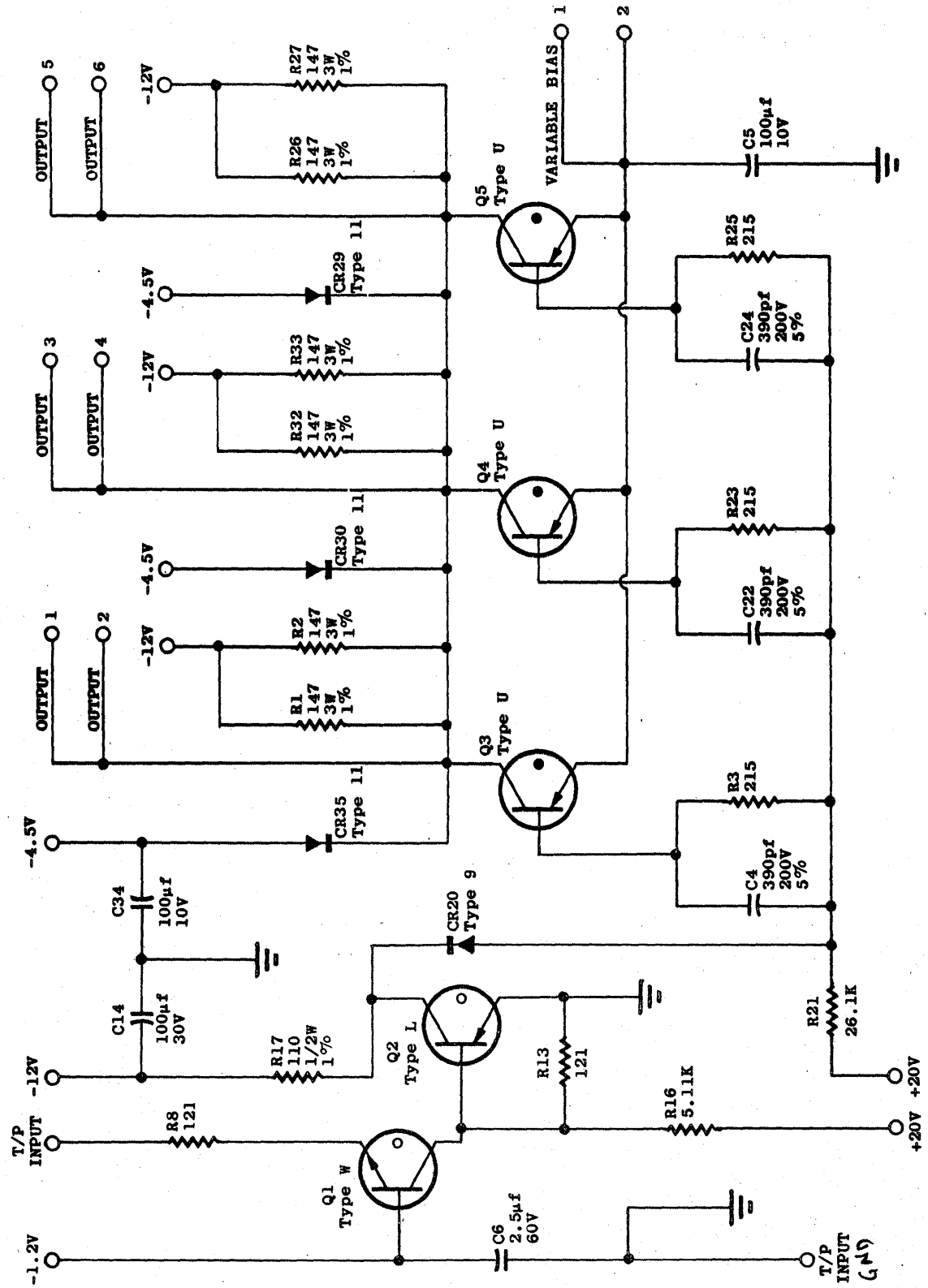


FIGURE 6.34-1. DIRECT COUPLED LOCAL CLOCK DRIVER

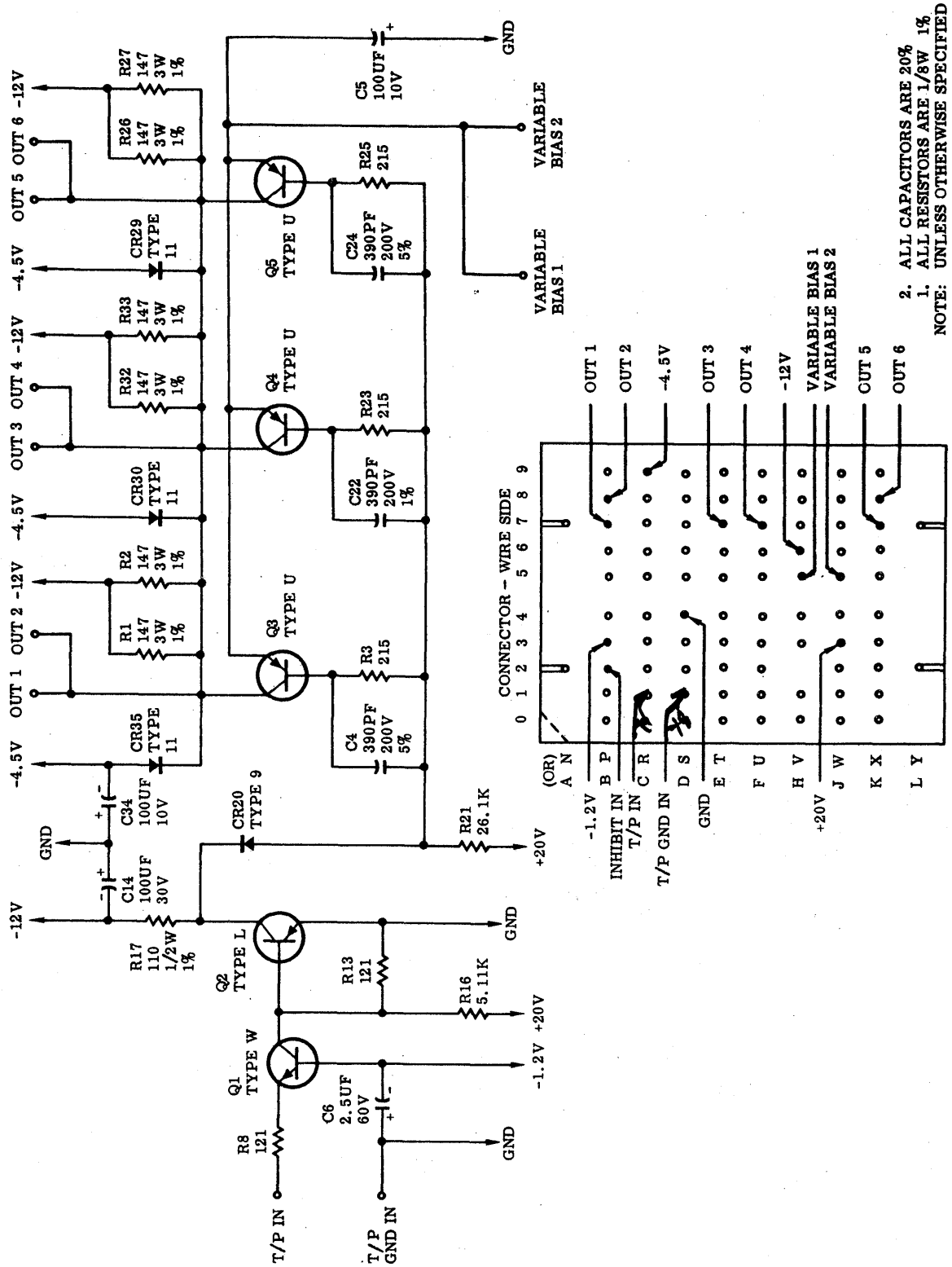


FIGURE 6.34-2. DIRECT COUPLED CLOCK DRIVER PACKAGE SCHEMATIC

6.35 DOUBLE DRIVER 90

GENERAL DESCRIPTION

The Double Driver 90 is a package specifically designed to reduce the number of driver packages required by the system as well as to reduce the number of back-plane wires.

The package consists of two identical Double Driver 90 circuits. Each has one input and two outputs. The circuit is a non-inverting switch amplifier to be used to drive cables and load requiring currents up to 90 ma.

CIRCUIT DESCRIPTION

Refer to Figures 6.35-1 and 6.35-2.

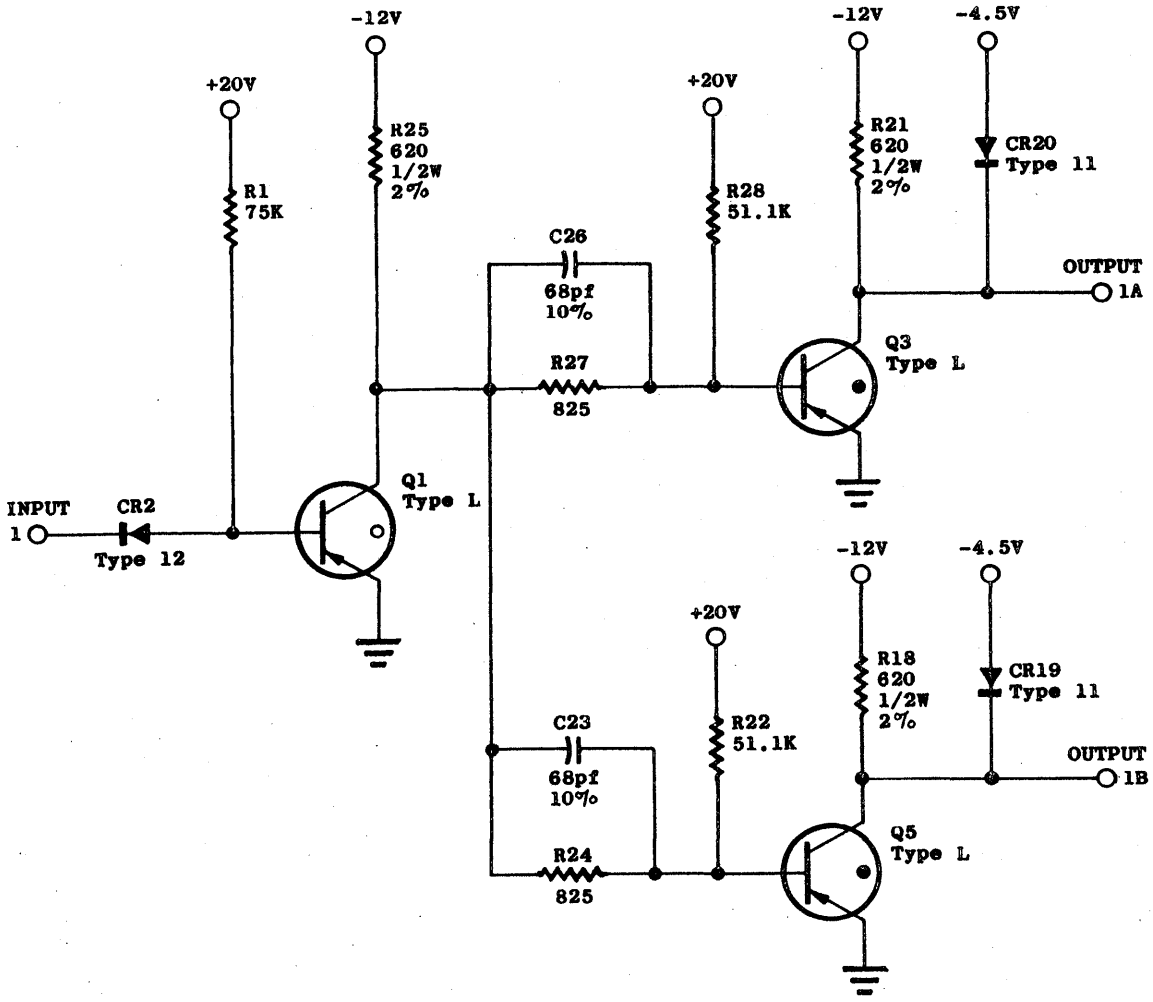


FIGURE 6.35-1. DOUBLE DRIVER 90 CIRCUIT SCHEMATIC

In the quiescent state, Q1 is cut OFF and Q3 and Q5 are in saturation.

When a negative input greater than -1.2V is applied at the input, base drive is supplied to Q1, turning it ON. When Q1 goes ON, its collector goes toward its saturation voltage, removing base drive to Q3 and Q5 cutting them OFF. The cut OFF of Q3 and Q5 results in their collectors rising toward -12V. However, the clamping diodes CR20 and CR19, clamp the rise to -4.5V resulting in an output of -4.5V at 1A and 1B.

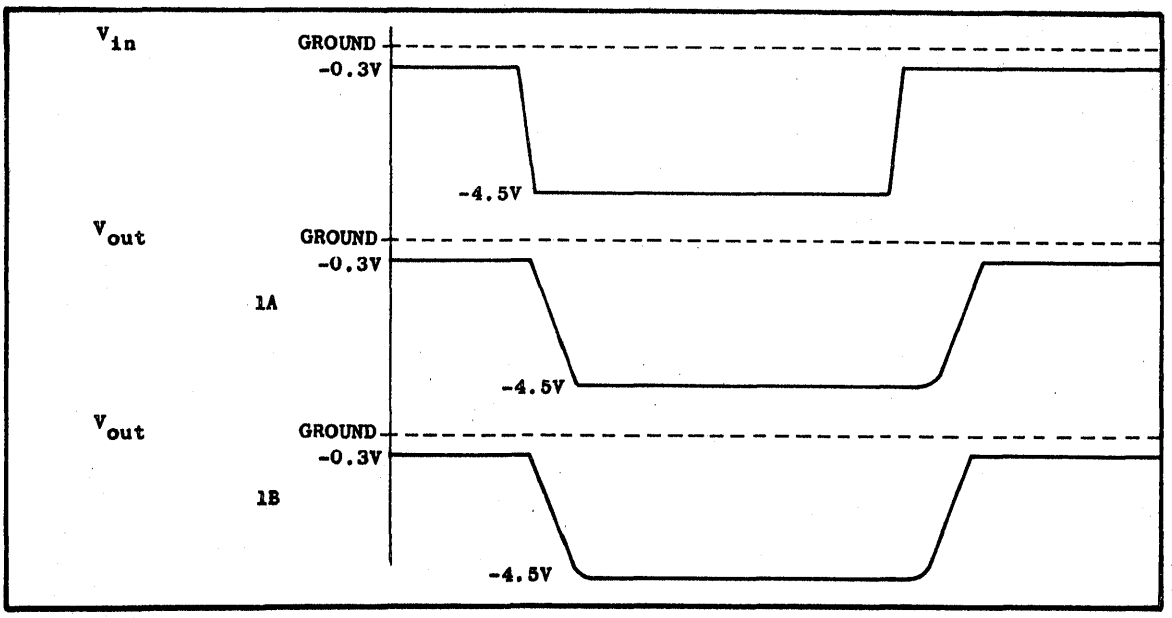


FIGURE 6.35-2. DOUBLE DRIVER 90 TIMING

SWITCHING

When the input goes from a true level to a false, the reverse action takes place.

Q1 will be turned OFF, Q3 and Q5 will be turned ON, resulting in a false level of -0.3V at output 1A and 1B.

Capacitors C26 and C23 speed up the switching time of Q3 and Q5.

Resistors R27 and R24 limit the base to emitter current of Q3 and Q5 when Q1 is cut OFF.

PACKAGE SCHEMATIC

Refer to Figure 6.35-3 for the complete schematic of the Double Driver 90 parallel Plate Package.

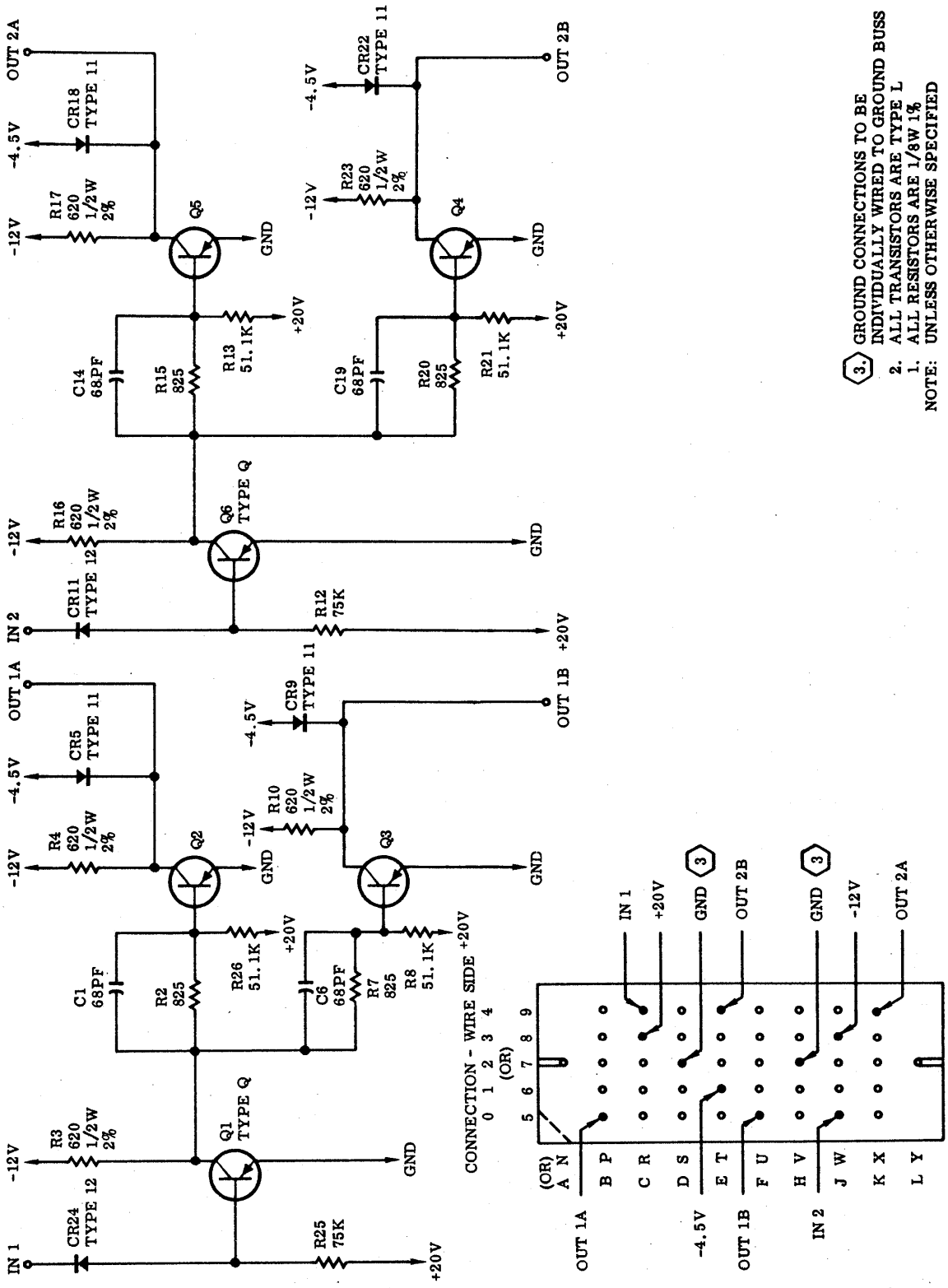


FIGURE 6.35-3. DOUBLE DRIVER 90 PACKAGE SCHEMATIC

6.36 INVERTER DRIVER 90

GENERAL DESCRIPTION

The Inverter Driver 90 is a circuit which provides two driver outputs. One non-inverted and one inverted, for one input.

The package contains two identical circuits, each having one input and two outputs. The circuits are used to drive loads and cables requiring currents up to 90 ma.

CIRCUIT DESCRIPTION

Refer to Figures 6.36-1 and 6.36-2.

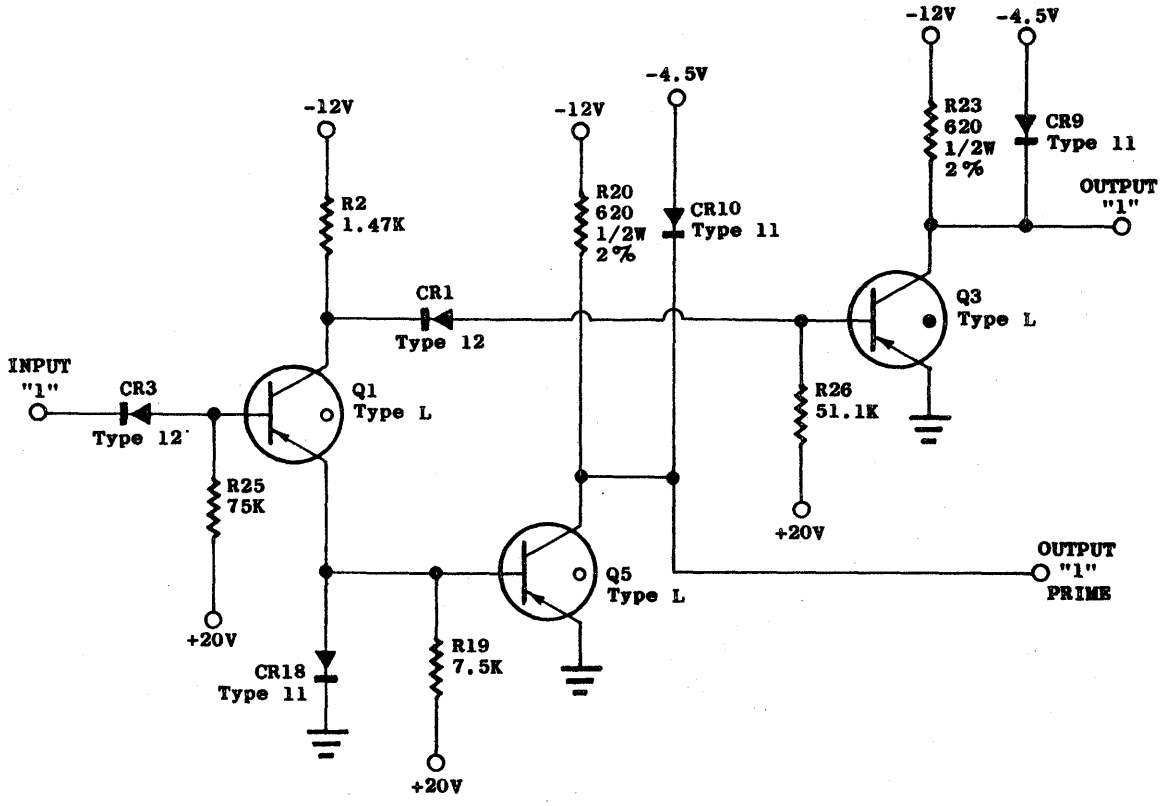


FIGURE 6.36-1. INVERTER DRIVER 90 CIRCUIT SCHEMATIC

In the quiescent state, Q1 and Q5 are cut OFF, and Q3 is in saturation.

When a true level is applied to the input, base drive will be supplied to Q1 turning it ON. When Q1 turns ON, its emitter follows the base supplying base to Q5, turning it ON.

The turn ON of Q5 results in its collector going toward its saturation potential, supplying an inverted (false in this case) output at Output 1 Prime.

The turn ON of Q1 also results in its collector going toward its saturation potential, removing base drive from Q3 turning it OFF. When Q3 goes OFF, its collector rises toward -12.0V, the clamp diode CR9 clamps the rise to -4.5V resulting in an output of -4.5V at Output 1.

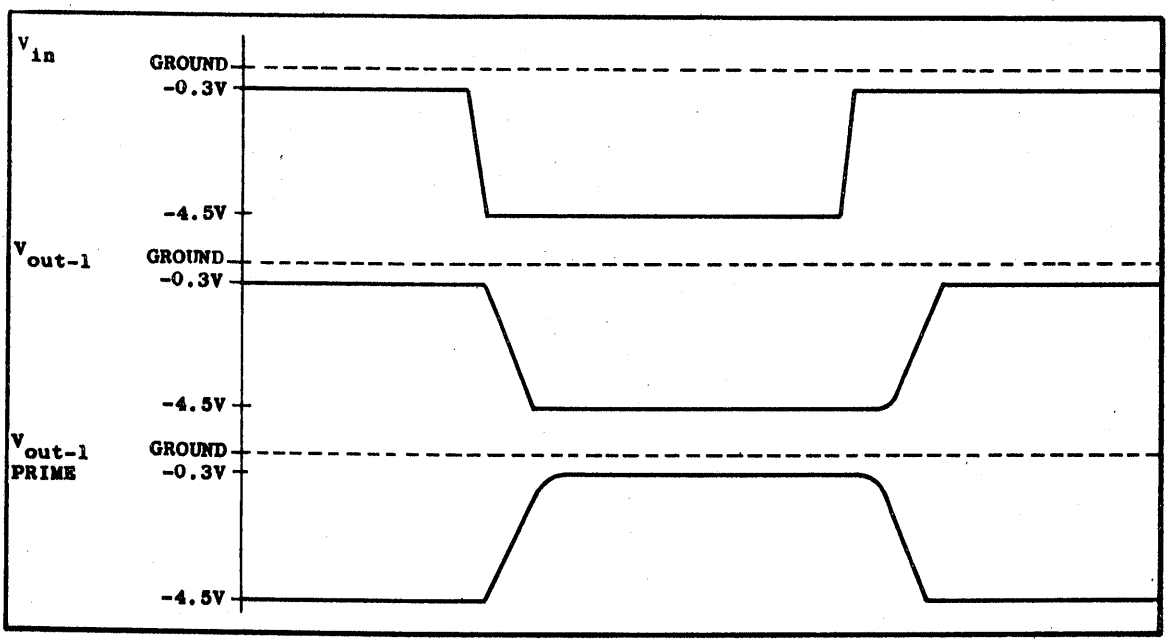


FIGURE 6.36-2. INVERTER DRIVER 90 TIMING

SWITCHING

When the input goes from a true level to a false, the reverse action takes place.

Q1 will be turned OFF, turning OFF Q5, which results in Ouput 1 Prime going true (-4.5V). The turn OFF of Q1 also results in Q3 turning ON, producing a false (-0.3V) output at Output 1.

PACKAGE SCHEMATIC

Refer to Figure 6.36-3 for the complete schematic of the Inverter Driver 90 Parallel Plate Package.

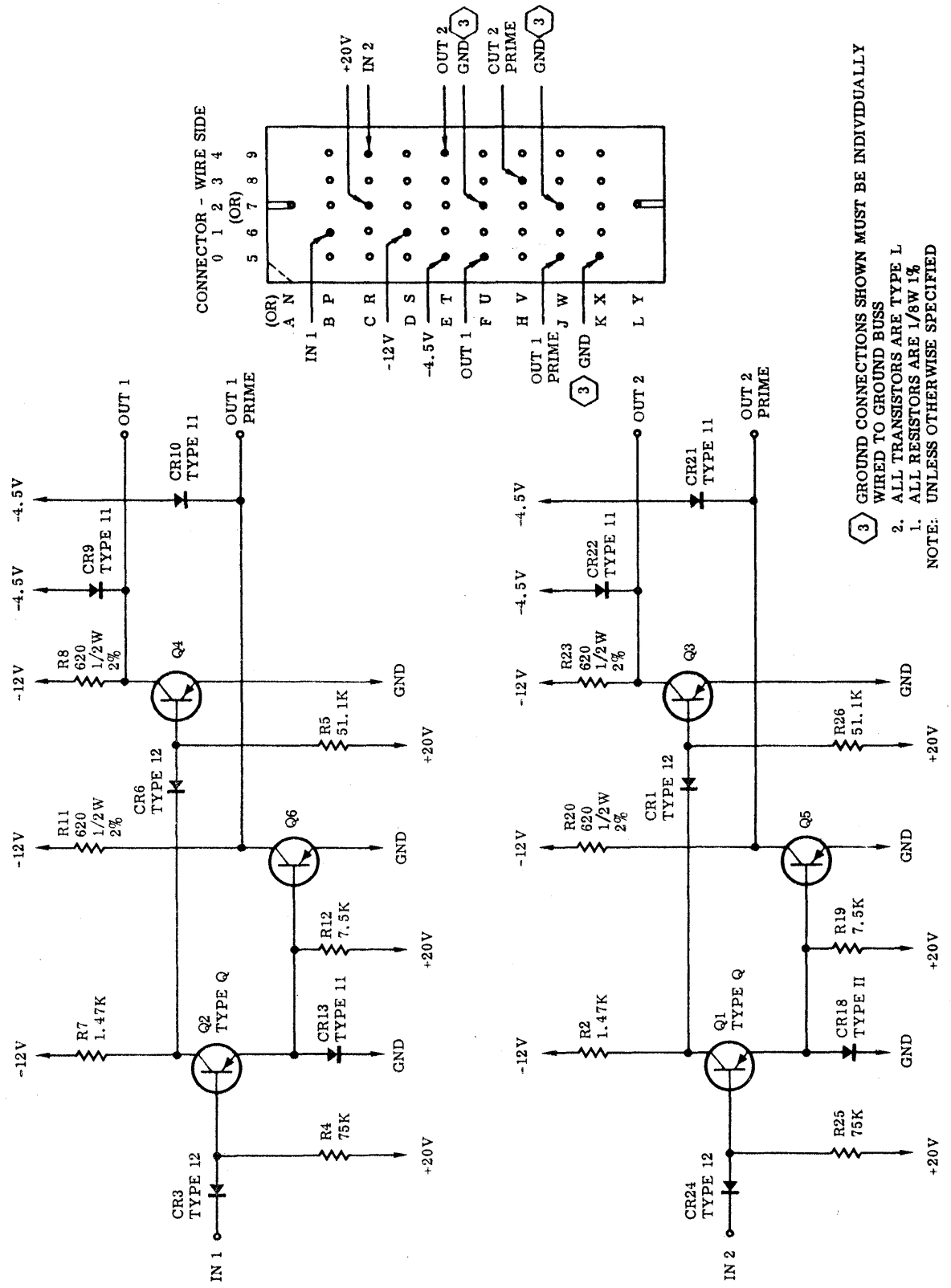


FIGURE 6.36-3. INVERTER DRIVER 90 PACKAGE SCHEMATIC

6.37 FLIP-FLOP AMPLIFIER

GENERAL DESCRIPTION

The Flip-Flop Amplifier is a package containing three circuits. Two of these circuits are double switches, having two outputs for a single input, and the third is a single switch.

The circuits are used directly with the outputs of a flip-flop, providing drive to more loads, with no time delay than is possible with the conventional switch or driver circuit.

CIRCUIT DESCRIPTION

Refer to Figures 6.37-1 and 6.37-2.

In the quiescent state, Q1 and Q3 are cut OFF.

When a negative level is applied to input 1, base drive is supplied to Q1 and Q3, turning both ON.

The collectors of Q1 and Q3 move toward their saturation potentials providing false (-0.3V) outputs at Output 1A and 1B.

Capacitors C27 and C24 speed up the switching time of Q1 and Q3.

Resistors R28 and R25 limit the base to emitter currents of Q1 and Q3 when the input is true.

The identical circuit consisting of Q4 and Q5 operates the same as the Q1 and Q3 circuit. However, normally, this circuit will have as its output the opposite state of the flip-flop. Therefore, if Input 1 is true, Input 2 will be false, and Output 2A and 2B will be true.

In the third circuit, Q2 is cut OFF in the quiescent state.

When a negative level is applied to Input 3, base drive is supplied to Q2, turning it ON. Its collector will then start toward its saturation potential, producing a false (-0.3V) output at Output 3.

PACKAGE USAGE

When the Flip-Flop Amplifier is used with a flip-flop, its inputs tie directly to the output of the flip-flop, and is the only load tied to the flip-flop.

All loads requiring an input from the flip-flop are then tied to the outputs of the Flip-Flop Amplifier.

If a Flip-Flop Amplifier is used with the flip-flops "1" output, there will also be an amplifier on the "0" output. The maximum amplifiers used with one output of a flip-flop is 5. Inputs 1, 2 and 3 are connected in parallel to one of the outputs of the flip-flop.

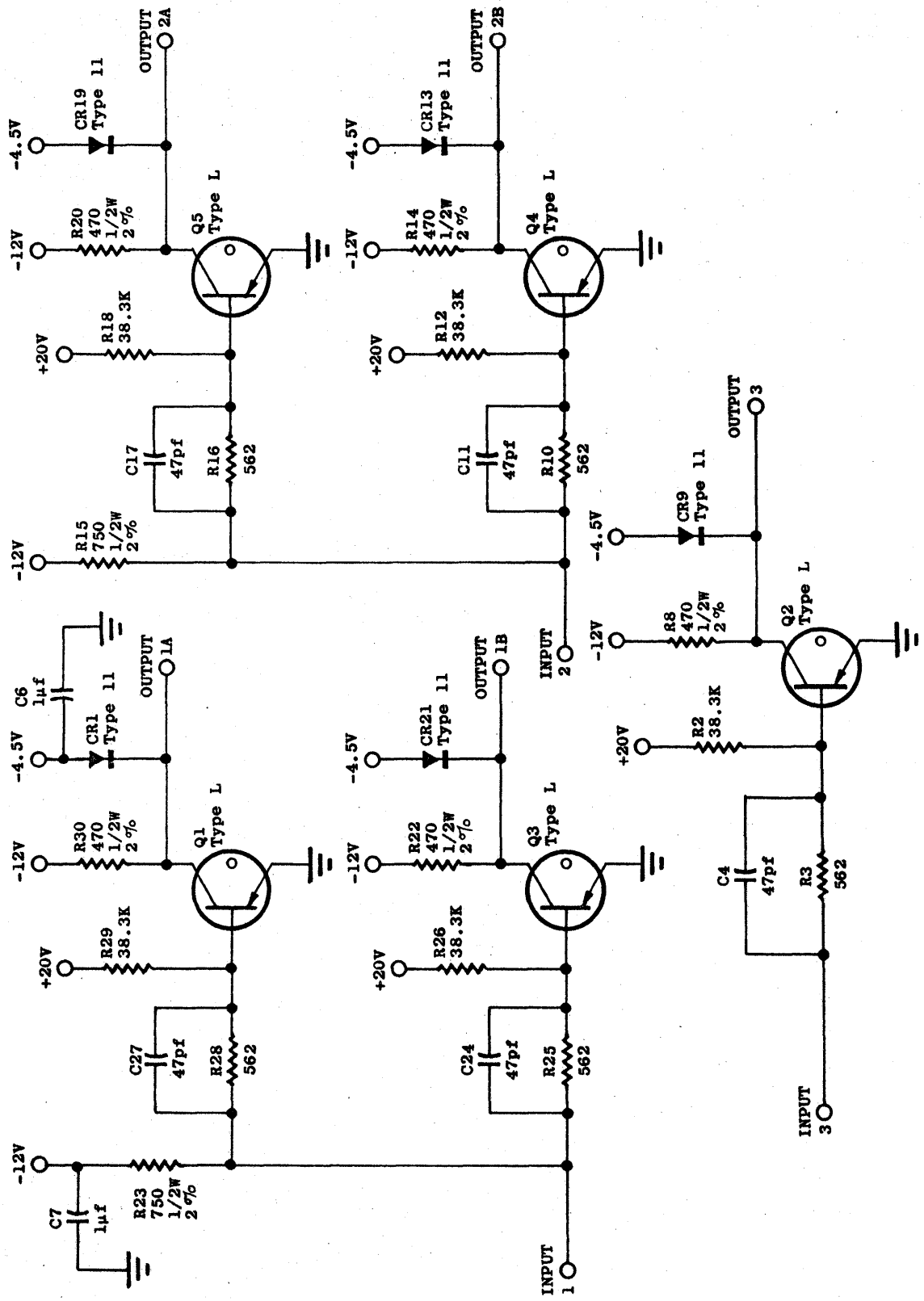


FIGURE 6.37-1. FLIP-FLOP AMPLIFIER CIRCUIT SCHEMATIC

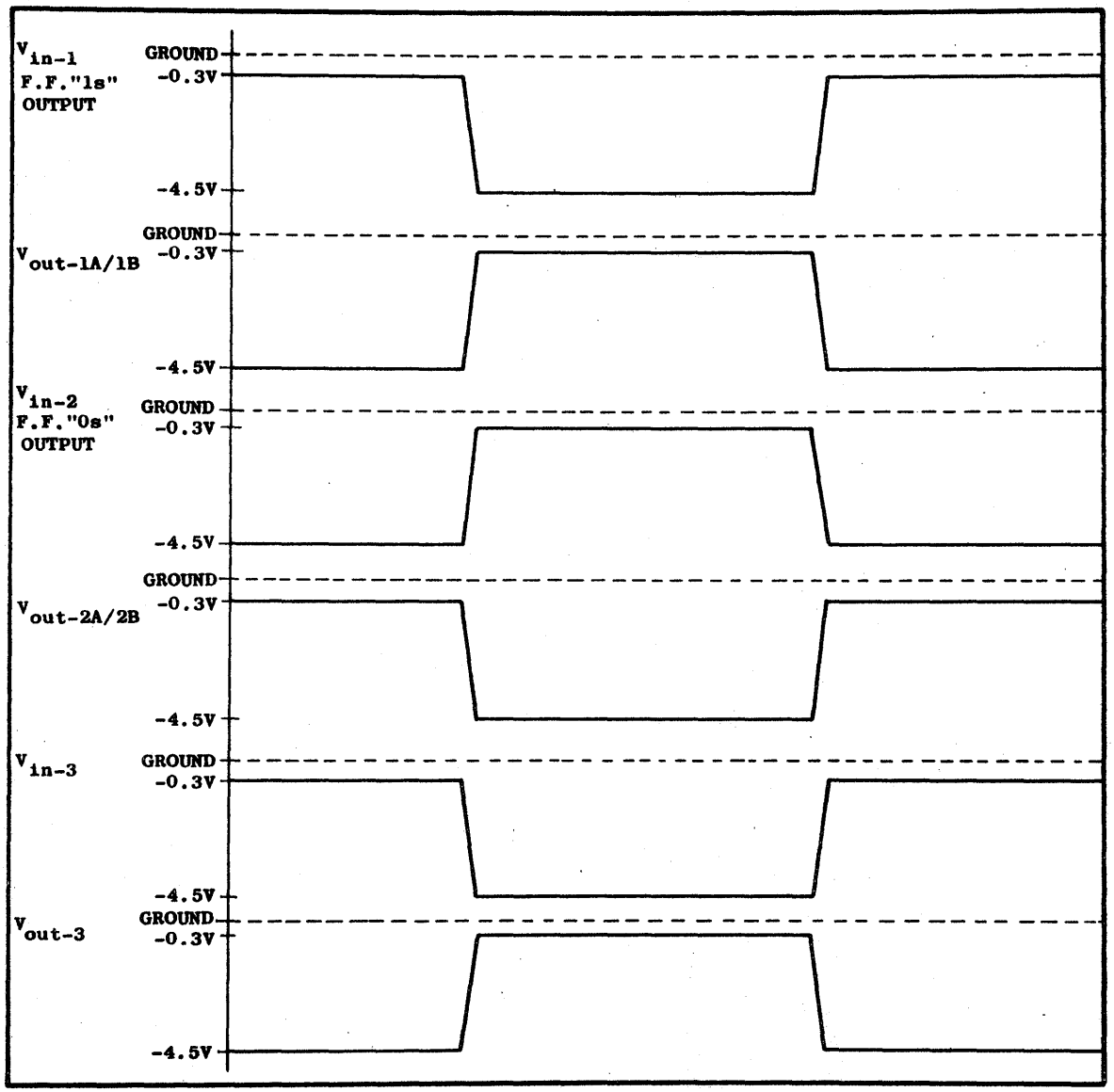


FIGURE 6.37-2. FLIP-FLOP AMPLIFIER WAVEFORMS

PACKAGE SCHEMATIC

Refer to Figure 6.37-3 for the complete schematic of the Flip-Flop Amplifier Parallel Plate Package.

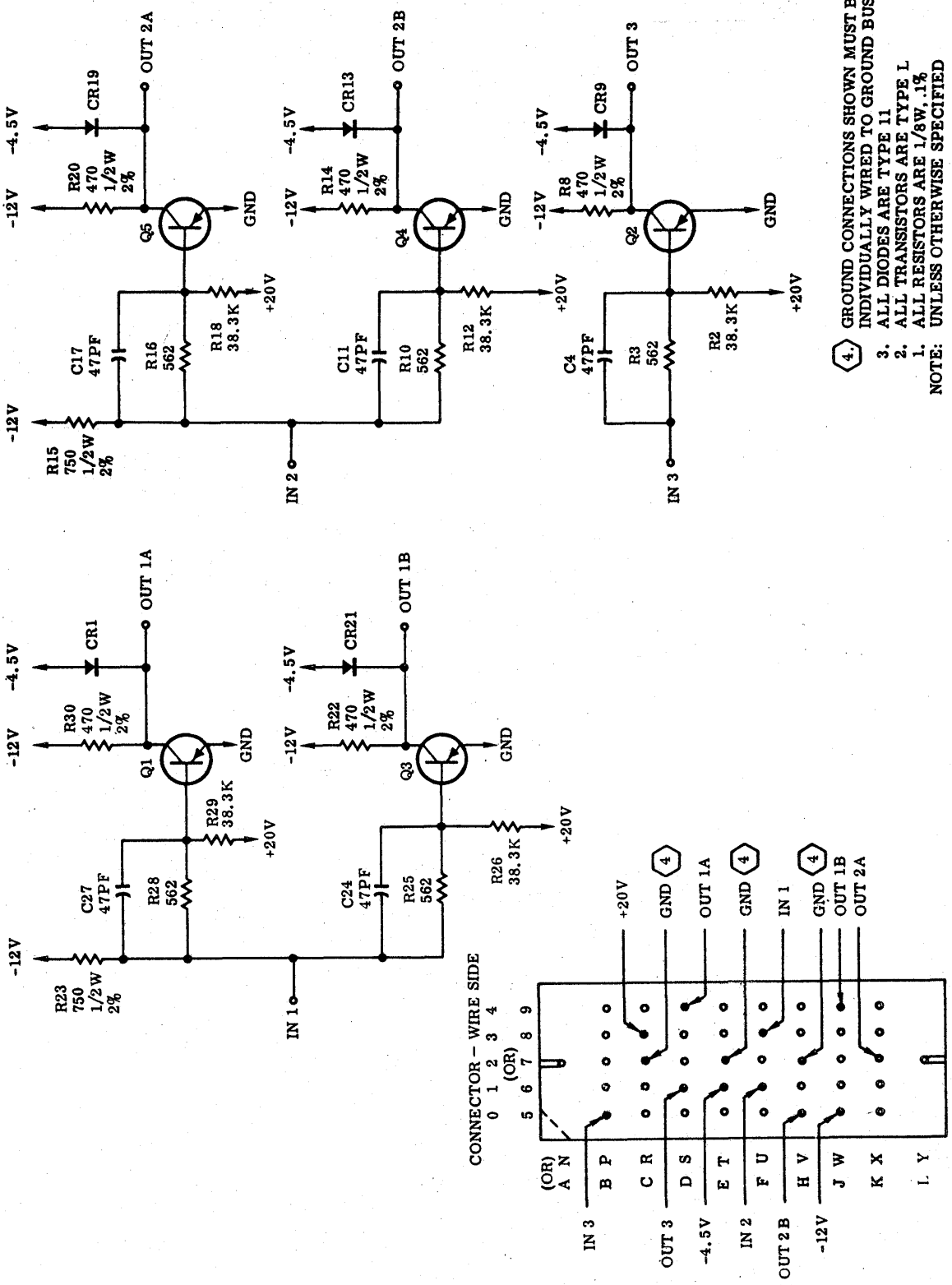


FIGURE 6.37-3. FLIP-FLOP AMPLIFIER PACKAGE SCHEMATIC

7.1 GENERAL

INTRODUCTION

The B 5000 System Power Supply provides all DC voltages required for proper operation of the system, and 115V AC for the Convenience Outlets and Fan Motor Power.

The voltages are distributed through the Display and Distribution Cabinet to the Central Processors, Central Control, Core Memories and the Input/Output Unit, which are the Main cabinets of the system, and also to the Control Console.

All power is supplied through the Distribution Panel in the D & D Unit EXCEPT -19V which comes from the Power Supply via the D & D Cabinet to the cabinets with regulator units.

The peripheral units not receiving power from the Main Supply; for example, the Drum Memories, Readers, Punches, Printer, Magnetic Tapes etc., will be dealt with separately and connected electrically for optimum phase balance according to the Pre-Installation Planning Manual.

The raw voltages of the System Supply are developed from transformers of the constant voltage type, and are used as inputs to voltage regulators, drive voltage sensing and shut-down circuits, and energize Control Relays. The raw supplies are also used directly without external regulation within the B 5000 system.

The voltage regulators (B 5000 Regulator Power Unit) develop the regulated voltages -1.2V, -4.5V and -12V. The regulator units are physically separate and each unit provides its own three (3) regulated voltages. There are six (6) of these power units in a maximum system configuration, one in each of the Main cabinets except the Display and Distribution cabinet, Drum cabinet and the Power Supply cabinet. Each of the three voltages, provided by the power unit of each cabinet, is sensed for over and under voltage within the Display and Distribution cabinet. The status is shown by indicator lights.

Excess Current is also sensed from the power unit (-12V Regulator), and indicated on the Power Maintenance Panel located in the Display and Distribution cabinet. In addition, the +20V and +100V Supplies are sensed only in the Display and Distribution cabinet and indicated on the Power Maintenance Panel.

Overheat in the cabinets, and excess current drawn from a power unit (-12V Regulator) and the other FAIL conditions provide automatic shut-down of the system Power Supply.

7.2 CLASSIFICATION OF DC SUPPLIES

Power Supplies in the Power Supply can be divided into three classes.

CLASS 1 - POWER SUPPLIES WITH FINAL REGULATION

These voltages have no means of regulation but the constant voltage transformer, which has more stringent requirements for load and line regulation. They will have heavier bleeder current. Loads on these supplies are anticipated to be fairly constant and will also represent a significant part of the maximum current. Voltages +20V, +100V, -100V and +50V belong to this class.

CLASS 2 - POWER SUPPLIES WITH DC VOLTAGE PRE-REGULATED

These are the raw DC voltages for the local transistorized regulators. Pre-regulation primarily means compensation of wide line voltage variation (-30%, +10%), and some load regulation (by the compensating winding of the constant voltage transformers). Bleeder currents on these supplies are limited from 3% to 5% of the nominal DC output circuits.

Voltages in this class are -19/12V (used also to produce -4.5V and -1.2V), and Core Memory voltages, -38/30V, +19/12V, -33/25V, and +74/60V.

CLASS 3 - POWER SUPPLIES WITH DC VOLTAGES NOT REGULATED

Only two voltages are NOT regulated. These are: neon indicator voltage -120V and auxiliary control voltage -24V.

These two voltages will follow directly the line voltage variation (this means ±10%), and will also be affected by the changes in load and temperature.

7.3 +20 VOLT ELECTRICAL SWITCH

The +20V Electrical Switch is a circuit which provides a means of controlling the +20V Power Supply. The circuit is used to insure that the +20V power is supplied to the transistor circuits prior to the negative voltages. In this way, damage to circuit components is prevented.

This circuit also provides a means of removing the negative potentials from the circuitry, prior to removal of the bias voltage when power is lost due to a power failure, or during power shutdown.

7.4 +100 VOLT ELECTRICAL SWITCH

The +100V Electrical Switch provides a means of controlling the +100V Power Supply. The switch circuit is used to insure that all other voltages are present on the system prior to the +100V. The +100V is used to develop the +20V Delayed to clear all flip-flops when power is applied.

7.5 AC CIRCUITS

AC METER

The AC Meter measures the voltage across any two legs of the input lines. It is controlled through a four position, two layer, rotary switch and provides monitoring of the three phase (3Ø) AC input.

There are four neon indicators located on the Power Supply cabinet, adjacent to the AC meter, which, when lit, indicate power on. There is one light for each of the following combinations: ØAB, ØBC, ØAC and ØAN.

AC AUXILIARY CIRCUITS

There is a group of single phase 120V circuits, derived from Neutral to Phase A. These circuits serve the following:

1. Fans

   Five on top of the cabinet, three on the power rectifier assembly. This circuit is extended to other cabinets of the Main Frame through terminals K8 - 01/02 - 03/04 in the distribution box.

2. Convenience Outlets

   The 120V AC should be checked at local convenience outlets and at terminals K8-05-06 in distribution box. This voltage is controlled by circuit breaker CB18 in AC input box.

7.6 ELAPSED TIME INDICATOR

The Elapsed Time Indicator indicates in hours, the time that power is applied to the system. The meter is located in the Power Supply cabinet.

7.7 METER CHECK SWITCH

The Meter Check Switch is a five deck rotary wafer switch located on the Power Supply Indicator Panel. The Meter Check switch is used to monitor the voltage and amperage of the DC Supplies individually.

The voltmeter is 1 milliampere movement and ranges 0-50V, 0-150V.

The ammeter is 50 millivolt movement and ranges 0-5A, 0-10A, 0-50A and 0-100A.

The Meter Check switch is used in conjunction with a voltmeter and an ammeter to select and monitor a given DC Supply.

7.8 METER CHECK CIRCUIT

This circuit provides a means by which the meters themselves can be checked. Fixed potentials are supplied such that with the rotorary switch in position V (Meter Check) the meters are examined for full deflection. The potentials are +5V and 50 milliamperes.

Refer to Section 3 for adjustment procedure.

7.9 CONTROL RELAYS

Power for the B 5000 system is controlled through the use of DC relays. There are two (2) DC contactors and seven (7) DC relays which control the distribution of DC power to the main units and the peripheral equipment. These relays provide DC power to the system in proper sequence when applying power. They also provide cycling down of DC power in the proper order when removing power or during a power failure, either within the Power Supply itself, or a power failure within one of the main units of the system except the Drum cabinet.

RELAY OPERATION

Refer to Figure 6.2-4 for schematic showing relays K11 and K12.

The following is a list of the control relays giving their use.

Relay K11

Relay K11 opens and closes the primary winding of power transformers 1 and 4.

Refer to Figure 6.2-5 for schematic showing relays K12, K13, K14, K15, K17, K18, K19 and K20.

Relay K12

K12 opens and closes the primary windings of transformers 2, 3 and 6. Relay K12 also controls the 120V AC Supply to the Cabinet Fans and the Running Time Meter.

Relay K13

K13 controls the pick and drop of K11 and K12. It is the main Power ON relay, and is controlled through the Power ON and Power OFF buttons, the overvoltage, undervoltage, excess current and overheat sensing.

Relay K14

K14 allows 150 ms delay during Power OFF to insure that the peripheral units have time to function. K14 is a slow release relay.

Relay K15

Sends Power ON and Power OFF signals to the peripheral equipment.

Realy K17

Inhibit interlock to peripheral units and -24VB to DC Indicators.

Relay K18

Remove System Power down level to Core Memory, and inhibit or enable the 1 megacycle clock.

Relay K19

Power Sensing Matrix inhibit, +20V switch control and Core Memory Power Supply delay.

Relay K20

Display and Distribution cabinet cover interlock.

7.10 VOLTAGE SENSING

The B 5000 System has facilities for sensing over and under voltage conditions for the -1.2V, -4.5V, -12V, +20V and +100V. In addition, excess current from the -12V regulator and overheat conditions are sensed. These conditions will shut down the Power Supply. The +20V and +100V are sensed in the Display and Distribution cabinet. The remainder of the voltages, excess current, and overheat conditions are sensed in Display and Distribution by cabinet.

Using this method, a visual indication can be presented. For example: the voltage that failed, over or under voltage, and the cabinet where the failure occurred. Overheat is indicated by the cabinet causing the failure. Excess current is indicated by cabinet, -12V indicator ON, and excess current indicator ON. Only the -12V regulator supply is sensed for excess current.

7.11 VOLTAGE SENSING PACKAGE

There are twenty identical voltage sensing circuits. One circuit is used for each of the three separate voltages (-1.2V, -4.5V, and -12V) in the B 5000 Regulator Power Pack. There are six power units in a maximum system. Therefore, there are eighteen voltage sensing circuits for these voltages alone. The +20V and the +100V are also sensed for undervoltage and overvoltage, requiring two additional sensing circuits, for a total of twenty. These circuit packages are located in the Display and Distribution cabinet.

The Voltage Sensing Package is a circuit providing two separate outputs, an output when an overvoltage is sensed, and an output when an undervoltage is sensed. Both outputs in normal operation (neither an overvoltage or undervoltage condition exists) have a negative output (true). With the detection of an overvoltage, output 1 becomes false. With an undervoltage detection, output 2 becomes false. At no time are both outputs simultaneously false.

7.12 VOLTAGE REFERENCE PACKAGE

The Voltage Reference Package is made up of a circuit that develops three separate voltages for use in the voltage sensing circuits. These three voltages, -9V and two separate voltages of -4.5V each, are used as reference voltages in sensing for overvoltage and undervoltage.

7.13 -12 VOLT REGULATOR

The -12V Regulator is a standard series type with the output sensed through a difference amplifier. The difference is amplified, inverted and applied to the output as a corrective signal.

The -12V Regulator provides circuitry for the detection of excess current being drawn from the supply. If excess current is drawn from the supply, the main power source is shut-down automatically through a sensing circuit.

A -12V Regulator is located in each of the major units except the Display and Distribution, Power Supply, and Drum cabinets.

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7.14 -4.5 VOLT REGULATOR

The -4.5V regulator provides regulation for the -4.5V from the source portion of the regulator. It also regulates the incoming current through the sink portion of the regulator.

The regulator, at times, supplies power to circuit loads that terminate at a voltage more negative than -4.5V. At these times, current will flow in the reverse direction or toward the positive potential, in this case the -4.5V. This negative source is flowing into the regulator through the -4.5V normal output terminal, thereby overriding the -4.5V source. With this condition existing, the incoming current must also be regulated, as it will vary the -4.5V output. This is done in the sink regulator section.

7.15 -1.2 VOLT REGULATOR

The -1.2V regulator is a series type with the output sensed through a difference amplifier. The difference is amplified and applied to the output circuit as a corrective signal.

7.16 POWER OFF CIRCUIT

This circuit is a part of power control located in D & D and Console. It is intended for emergency use and regular use when checking the Power Supply Main Unit.