

**B 9499-3 DISK PACK
ELECTRONIC CONTROLLER**

(MODEL 206)

TECHNICAL MANUAL

VOLUME 1:

**OPERATION
and
MAINTENANCE**

Burroughs 

FIELD ENGINEERING

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PREFACE

The 206 Disk Pack Electronic Controller (206 DPEC) technical manual provides installation, operation, and maintenance information to the field engineer. In addition, three standard appendices are included:

- a. Appendix A. Glossary of Terms.
- b. Appendix B. LINs.
- c. Appendix C. RINs.

SECTION 1

FUNCTION AND OPERATION

INTRODUCTION

This section contains a general description of the B 9499-3 Disk Pack Electronic Controller (206 DPEC). It includes explanations of the operation codes, result descriptor information, and miscellaneous functional requirements.

GENERAL DESCRIPTION

The 206 DPEC is a hard-wired controller that includes all the hardware for synchronizing the interfaces between the B 1700 Disk Pack Control (DPC) and the 206 Disk Pack Drive (DPD) (see figures 1-1 through 1-3).

The controller is designed for a maximum configuration of one by eight spindles of disk pack drives. All DPEC's are capable of one by eight operation with no modifications. Standard 25-wire interface (parallel) is used between the DPC (host system) and the DPEC (see figure 1-4).

The DPEC acts upon I/O instructions from the DPC, performs the operation specified by the I/O descriptor and, upon completion, generates a result descriptor containing the operation completed and any error status information.

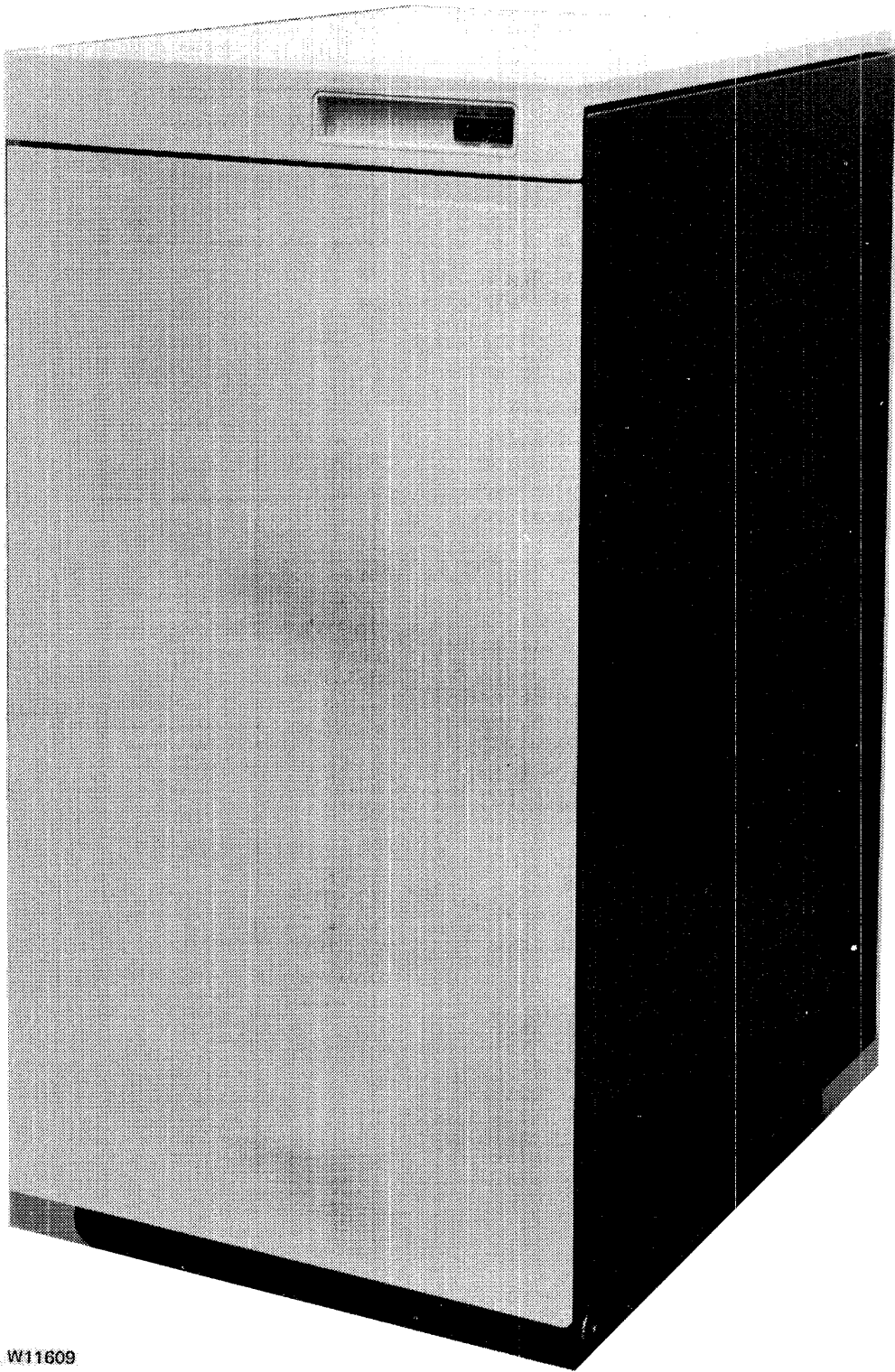
A 6-wire interface is used between the DPEC and the DPD. The interface lines consist of two bidirectional data lines (positive and negative), two clock lines (positive and negative), a controller message line, and a drive message line (refer to table 1-1).

Table 1-1. Edge Connector Wiring

Signal Description	Spindle Number	Card Edge Signal Lead	Connector Pin Ground Lead
CM	1	\$D	\$C
DATA POSITIVE	1	\$E	\$F
DATA NEGATIVE	1	\$G	\$F

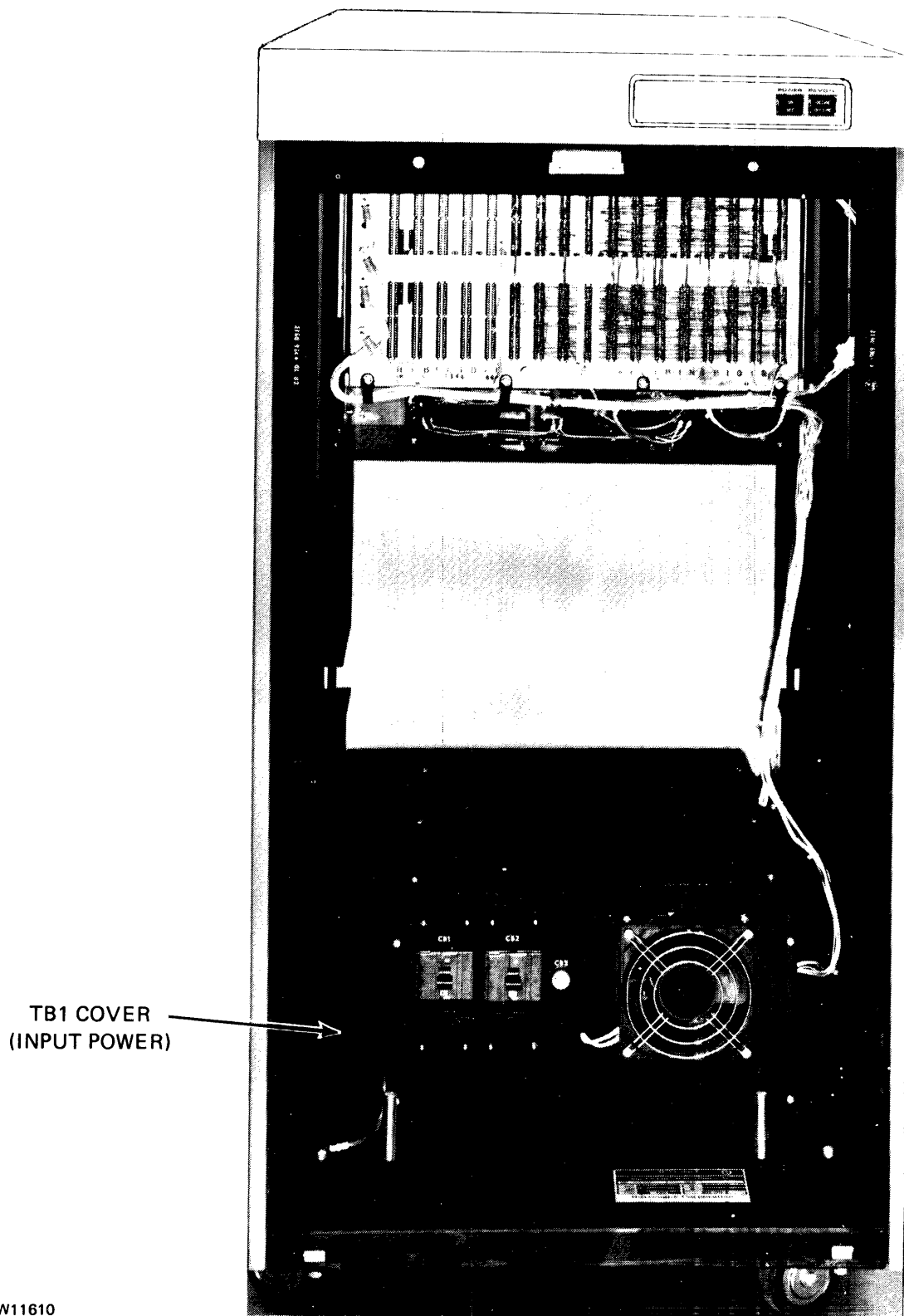
Table 1-1. Edge Connector Wiring (Cont)

Signal Description	Spindle Number	Card Edge Signal Lead	Connector Pin Ground Lead
CLOCK POSITIVE	1	\$H	\$I
CLOCK NEGATIVE	1	\$J	\$I
DM	1	\$K	\$L
DM	2	\$M	\$L
CLOCK NEGATIVE	2	\$N	\$P
CLOCK POSITIVE	2	\$Q	\$P
DATA NEGATIVE	2	\$R	\$S
DATA POSITIVE	2	\$T	\$S
CM	2	\$U	\$V
CM	3	#D	#C
DATA POSITIVE	3	#E	#F
DATA NEGATIVE	3	#G	#F
CLOCK POSITIVE	3	#H	#I
CLOCK NEGATIVE	3	#J	#I
DM	3	#K	#L
DM	4	#M	#L
CLOCK NEGATIVE	4	#N	#P
CLOCK POSITIVE	4	#Q	#P
DATA NEGATIVE	4	#R	#S
DATA POSITIVE	4	#T	#S
CM	4	#U	#V



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Figure 1-1. 206 Disk Pack Electronic Controller



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Figure 1-2. Internal Front View of 206 DPEC

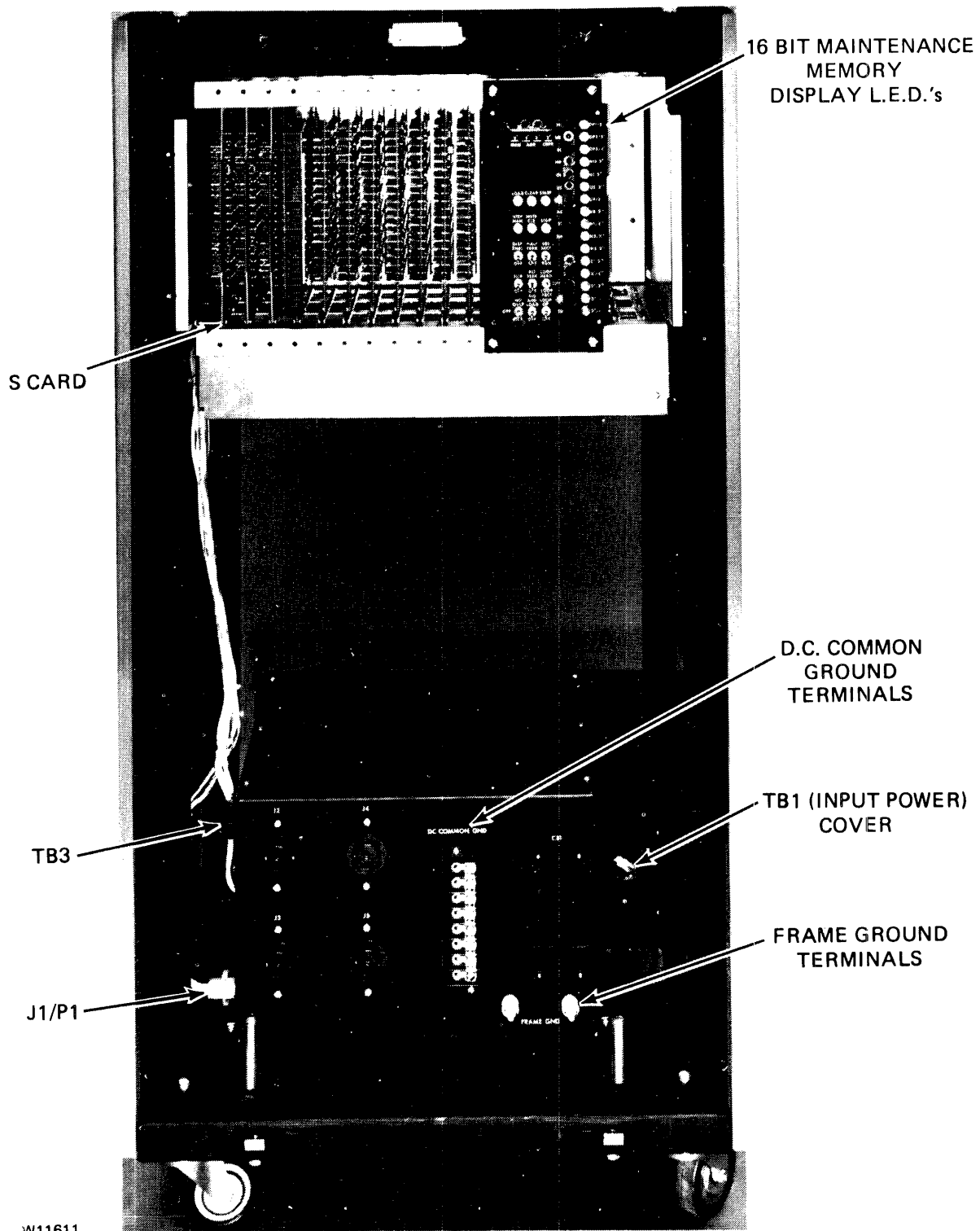
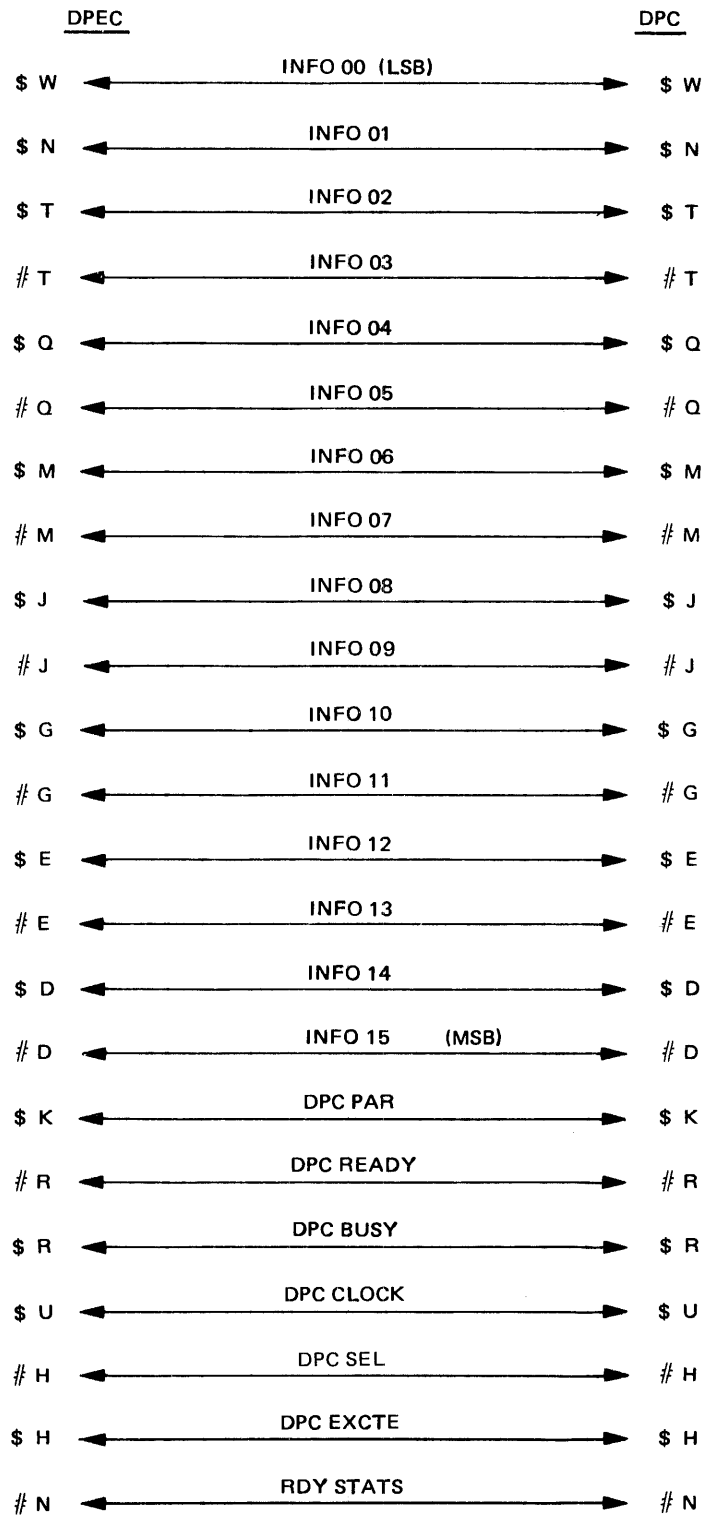


Figure 1-3. Internal Rear View of 206 DPEC



W11612 A

Figure 1-4. Interface Lines, DPEC to DPC ground.

DPEC OPERATION CODES

The following discussion provides a description of the operation codes used in the disk pack subsystem. Table 1-2 contains a list of the DPEC operation codes.

a. READ (000)

Read data from the disk pack starting at the beginning address specified by the initiate words and continue reading each full sector until the select line drops, informing the DPEC that the operation is terminated. No partial sector reads are permitted.

The DPEC will send 90 data words and two error code words to the DPC followed by the result descriptor in each sector read. The final result descriptor will be a composite of all previous sectors read.

b. READ MAINTENANCE (001) Unconditional Seek

Read all data bits from the designated sector, through the error protection code (EPC), by dead reckoning beginning at the index mark. Data integrity is not guaranteed.

c. READ EXTENDED STATUS (001 and N2 variant set)

A read maintenance operation code with the N2 variant set is used to clear a TRY DIAGNOSTICS condition. In local, the READ EXTENDED STATUS operation code is used to read the four extended result descriptor registers.

d. WRITE (010)

Write data on the disk pack starting at the beginning address specified by the initiate words and continue writing each full sector until the select line drops informing the DPEC that the operation is terminated. No partial sector writes are permitted.

The DPEC will accept 90 data words plus two dummy words. The DPEC will strip the dummy words and write the 32 check bits (Fire code) on disk. A result descriptor is sent to the DPC at the termination of the write operation.

e. INITIALIZE (011)

Write all bits according to the format shown in figure 1-5, starting after the index pulse on

the specified track (head) for the entire track of pack. Spare sectors are also initialized. One data transfer takes place between the DPC and DPEC during an initialization period. The DPEC will fill the data field and write the check bits for the pattern specified by the S variant.

If the operation is terminated by the DPC (SELECT FALSE) during an initialize, the DPEC will complete the initialize to the end of the existing full track. The result descriptor will be returned at the termination of the initialize whether the DPC or DPEC caused the termination.

f. RELOCATE (100) Specified data

One data transfer takes place between the DPC and the DPEC. The DPEC writes the actual formatted address in the designated spare sector and writes the specified data pattern on a repeating basis to fill the data field. On completion of this operation, the DPEC returns a result descriptor to the DPC.

g. RELOCATE (101) Address data

No data transfer takes place between the DPC and the DPEC. The DPEC writes the actual formatted address in the designated spare sector and writes the sync byte and address repeatedly to fill the data field. On completion of this operation, the DPEC returns a result descriptor to the DPC.

During a normal read or write operation, the DPEC will perform all necessary and required operations to read the relocated sectors and then return to the previous address plus one to ensure the continuity of data transfer.

h. VERIFY (110)

The verify operation is a normal read if the N1, N2 or N3 variants are all zeros (LOW TRUE). If the N N N variants are specified, the following applies:

NNN Variant	Read Spare Sector	Head	Sector
001	1	4	85
010	2	4	86
011	3	4	87
100	4	4	88
101	5	4	89

The test pattern for verification is keyed data: sync byte plus cylinder, head, and sector information, if the S variant is not set on the initialization. If the S variant is set, then the data is specified by the processor.

i. TEST OP (111)

The DPEC will return a result descriptor for the unit specified in the test operation.

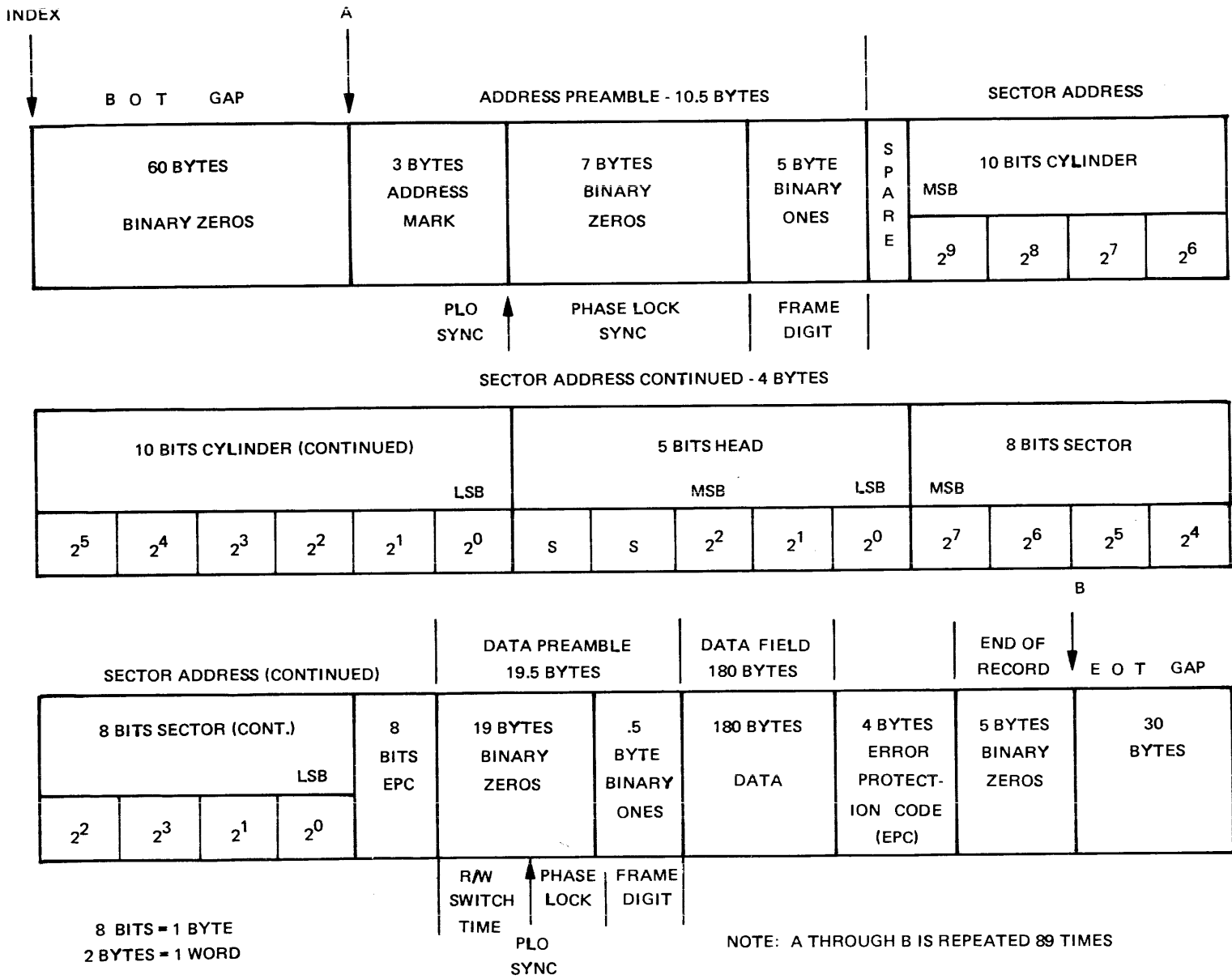
Table 1-2. DPEC 206 Operation Codes

OP1	OP2	OP3	N0	N1	N2	N3	OP DECODE
0	0	0	PLO	OF	E/L	I	READ
0	0	1	-	-	D	-	READ MAINTENANCE OR READ ERD
0	1	0	-	-	-	-	WRITE
0	1	1	-	-	S	P	INITIALIZE
1	0	0	-	N	N	N	RELOCATE 1. DATA SPECIFIED.
1	0	1	-	N	N	N	RELOCATE 2. DATA=ADDRESS FIELD.
1	1	0	-	N	N	N	VERIFY
1	1	1	-	-	C	W	TESTOP

The following are variants of the above codes.

- NNN* = (Binary 1 to 5) Spare Sector No.
- C = 1, Clear Seek Status Flip-Flops
- P = 0, Single Track. Initialize
- P = 1, Full Pack Initialize
- W = 0, Normal Test Op
- W = 1, Remote Power Down
- PLO = 1, Enable Early/Late Strobe
- PLO = 0, Disable Early/Late Strobe
- E/L = 0, Early Strobe
- E/L = 1, Late Strobe
- S = 1, Specified Data
- S = 0, Address Data
- OF = 0, Normal
- OF = 1, Offset
- D = 0, Read Maintenance
- D = 1, Read Extended Status
- I = 0, Offset Away from Spindle
- I = 1, Offset Toward Spindle

*The binary values of the N variants are N1 = 1, N2 = 2, N3 = 4.



TRACK FORMAT, 90 SECTORS/TRACK (20, 160 BYTES/TRACK), INTERLACE FORMAT

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Figure 1-5. 206 Track Format

INSTRUCTION FORMAT

Each instruction format contains three data words. The first data word consists of the operation code, "N" variants, unit designations, and the five least significant bits of the file address. The second data word consists of the 14 most significant bits of the file address and two spare bits. The third data word consists of the data information used during initialize, write, and relocate operations. Refer to table 1-3.

Table 1-3. DPEC 206 Instruction Format

INFO NN (LSB)	First Data Word	Initiate Phase
	1 OP1	9 N1
	2 OP2	10 N2
	3 OP3	11 N3
	4 NO	12 B2*0
	5 U1	13 B2*1
	6 U2	14 B2*2
	7 U4	15 B2*3
	8 U8	16 B2*4(MSB)

INFO NN (LSB)	Second Data Word	Initiate Phase
	1 B2*5	9 B2*13
	2 B2*6	10 B2*14
	3 B2*7	11 B2*15
	4 B2*8	12 B2*16
	5 B2*9	13 B2*17
	6 B2*10	14 B2*18
	7 B2*11	15 SPARE
	8 B2*12	16 SPARE (MSB)

INFO NN (LSB)	Third Data Word	Initiate Phase
	1 D Word, Bit 1	9 B Word, Bit 1
	2 D Word, Bit 2	10 B Word, Bit 2
	3 D Word, Bit 4	11 B Word, Bit 4
	4 D Word, Bit 8	12 B Word, Bit 8
	5 C Word, Bit 1	13 A Word, Bit 1
	6 C Word, Bit 2	14 A Word, Bit 2
	7 C Word, Bit 4	15 A Word, Bit 4
	8 C Word, Bit 8	16 A Word, Bit 8

NOTE

The first and second data words of the file address bits are identified as B2*0 (least significant bit) through B2*18 (most significant bit). For example, 2*3 indicates that 2 is to be raised to the third power, $2 \times 2 \times 2 = 8$.

RESULT DESCRIPTOR INFORMATION

At the completion of an operation code, a result descriptor will be returned to the DPC. (In a local mode, the result descriptor will be displayed on the maintenance plug-on package on the F card.) Table 1-4 lists the definitions of the result descriptor bits.

Table 1-4. Result Descriptor Information Lines

Bit	Description
00	Read Data Error. Indicates an error in the data field or the Fire code bytes.
01	Write Lockout. Indicates the spindle is in a Read-Only mode or the DPEC failed to send a Write Enable CM during a write operation.
02	Seek Status Flip-Flop Set. Indicates the previous seek operation has not been serviced by the DPC (conditional seek capability).
03	Spindle Not Ready. Indicates the positioner is not settled, and a seek is in progress.
04	Spindle Off Line. Indicates the spindle is in an off condition and will not accept any commands.
05	Spindle Unsafe. Indicates the spindle is unsafe for use.
06	Data Sync Code Error. Indicates the data sync character was not detected.
07	Address Parity Error, EPL Error, or Sync Code Error. Indicates one of the following: a. The address was not found. b. The read data address Error Protection Logic (EPL) code is not in agreement with the actual EPL. c. The address sync character was not detected.
08	Seek Timeout. Indicates that the DPD was unable to complete a seek within 700 milliseconds after being told to do so.
09	Drive not present. Indicates that the DPD is not present.
10	NA
11	NA
12	NA
13	NA
14	Transmission Parity Error or Illegal Command. Indicates a parity error exists between the DPC and DPEC.
15	Operation Not Completed. Try diagnostics. Indicates that an exception condition (fault) occurred in the subsystem and that the data is corrupt. A Read Extended Status command is required to clear the condition.

Extended Result Descriptor Feature

The 206 DPEC contains the ability to store up to 64 bits of extended result descriptor (ERD) information in addition to the normal 16 bits of result descriptor information. Table 1-5 contains a list of the 64 bits of ERD that are used. Refer to section 4 of this volume for details on using the ERD capability.

NOTE

The information in table 1-5 is listed in the order that will be read on the maintenance display plug-on indicator on the F card when in a LOCAL mode. (In REMOTE, the contents of each word are inverted. For example, in the E log, ERD bit 1 is cylinder 512, ERD bit 17 is sector 32, ERD bit 33 is DPEC blower failure, and ERD bit 49 is spindle address error.)

Table 1-5. 206 Extended Result Descriptor Information in a Local Mode

ERD Word 1	ERD Word 2	ERD Word 3	ERD Word 4
1 Sector 64	1 N3 Variant bit	1 Illegal Cylinder	1 Spare
2 Head 1	2 N2 Variant bit	2 Illegal Head	2 Bad DM response
3 Head 2	3 N1 Variant bit	3 CM or Offline when seeking	3 RPM less than 3420
4 Head 4	4 N0 Variant bit	4 Wr Protect and Wr Enable	4 Temp critical
5 Spare	5 Unit 2*0	5 Write data missing	5 Temp warning
6 Spare	6 Unit 2*1	6 Maintenance mode	6 DC power failure
7 Cylinder 1	7 Unit 2*2	7 Spare	7 Head select fault
8 Cylinder 2	8 OP Code 3	8 Spare	8 No write current changes
9 Cylinder 4	9 OP Code 2	9 Spare	9 Write current, no Wr gate
10 Cylinder 8	10 OP Code 1	10 Model 206 Drive	10 Spare
11 Cylinder 16	11 Sector 1	11 CM error*	11 Carriage hit end stop
12 Cylinder 32	12 Sector 2	12 Index Mark Missing	12 Off track and Wr enable
13 Cylinder 64	13 Sector 4	13 Read data not received	13 Seek incomplete
14 Cylinder 128	14 Sector 8	14 Missing Address mark	14 Offset during seek
15 Cylinder 256	15 Sector 16	15 Missing R/W clock	15 Offset during Wr enable
16 Cylinder 512	16 Sector 32	16 DPEC blower failure	16 Spindle address error

* When a CM error is detected in a local mode, the last CM message that was sent to the drive will be displayed in ERD registers three and four in the following manner:

ERD Word 3 (CM Error)		ERD Word 4 (CM error)	
1	Address information or PLO early		
2	Address information or Offset in		
3	Head or cylinder or Offset on	3	End bit
4	Address or Control message	4	Parity even (1-23)
5	Continue	5	Spare
6	Parity even (1-5)	6	Write enable
7	Address mark	7	Address information or Set maintenance mode
8	Read bit	8	Address information or Reset maintenance mode
9	Write bit	9	Address information or Spare
10	Mark Bit	10	Address information or Spare
		11	Address information or Find index
		12	Address information or Send status
		13	Address information or Re-zero
		14	Address information or Power down
		15	Address information or Power up
		16	Address information or PLO late

PHYSICAL REQUIREMENTS

Construction

The controller is constructed as a free-standing unit and is shipped with both side panels attached. The unit is designed to attach to a 206 disk pack drive unit.

Control Panel

A control panel incorporated on the indicator panel provides the following controls and indicators:

POWER: ON/OFF switch and indicator.

REMOTE: ONLINE/OFFLINE switch and indicator

Dimensions

The following are the dimensions for a 1 x 8 configuration, including front door, rear door, and side panels.

Dimensions	Inches	Cm
Height	44	112
Width, including side panels	21.5	53.5
Depth, including doors	30	76.3

Weights	Pounds	Kg
Installed Weight	220	100
Shipping Weights (not including I/O cables)		
Packaged for local shipment, polyethylene cover	225	102
Packaged for air shipment	250-260 (estimated)	113-118 (estimated)

When I/O cables are included in the shipping weight, use the following increments:

P/N	Description	Pounds	Kg
1145 7645	I/O Cable, 25 ft.	17	7.7
1147 8369	I/O Cable, 35 ft.	20	9.0
1147 8377	I/O Cable, 50 ft.	32	14.5
2105 8788	I/O Cable, 100 ft.	64	29.0

FUNCTIONAL REQUIREMENTS

Compatibility

The DPEC is compatible with the BX 387 disk pack drive controller, standard 90 sector interlaced format.

Chained I/O (DPC) Conditional Seeks

The DPEC is capable of operating with a chained I/O from the central processor unit (CPU). With chained or linked I/O, the DPEC will internally determine if a seek (positioner change) is required. If a seek is required, the DPEC performs the seek and

informs the CPU (DPC) that a specific spindle is seeking. By the use of a seek status flip-flop, once a seek has been initiated, the DPEC will not again perform a seek to that specific spindle until a read or write is received for that same cylinder. However, it will accept and perform operations on other spindles.

Error Detection

The DPEC will generate the Fire code and perform the error detection for all data transfers. (Error correction will be done by CPU.)

Operational Procedure

The front panel of the DPEC contains two push-button switches. See figures 1-1 and 1-2.

The switch on the left is the POWER ON/POWER OFF switch. Pressing the switch once causes the DPEC to be powered on and the ON portion of the switch to be illuminated. There is approximately a 30 second delay after the power ON button is pressed before the DPEC is operational.

Pressing the POWER button a second time will cause the DPEC to power off, and the OFF portion of the POWER button will become illuminated. In a similar manner, the REMOTE switch is used to place the DPEC in the ONLINE (remote) or OFFLINE (local) mode.

For system operation, the DPEC must be in the ONLINE mode and OFFLINE for local operation.

The mode of the DPEC (ONLINE or OFFLINE) will be indicated by having either the upper or lower portion of the REMOTE button illuminated. To transfer the DPEC to the opposite mode, press the REMOTE button.

SECTION 2 INSTALLATION

INTRODUCTION

This section contains the information necessary to install the B 9499-3 Disk Pack Electronics Controller (206 DPEC).

PRE-INSTALLATION REQUIREMENTS

The following paragraphs explain how the 206 disk pack drives are connected to the 206 DPEC. See figure 2-1.

Physical Site Requirements

Maintenance Clearances

Front	36 inches	90 cm
Rear	36 inches	90 cm
Sides	None	None

Floor Loading

Front Wheels	50 pounds each	(100 pounds total) 45.4 kg
Rear wheels	60 pounds each	(120 pounds total) 54.5 kg

I/O Cable Information (B 1700 to DPEC)

25 feet	1145	7645
35 feet	1147	8369
50 feet	1147	8377
100 feet	2105	8788

Drive Cable Information (DPEC to 206)

The 1 x 4 cable kit, 2781 0068, is available for use with the 206 DPEC and 206 DPD. The 1 x 4 kit consists of the following:

- One 1 x 4 signal cable.
- Two 3.0 foot dc common cables
- Two 4.5 foot dc common cables
- One 3.0 foot ac frame ground cable
- One 4.5 foot ac frame ground cable

Depending on the system configuration, the following quantities of the kit can be ordered from Group III Distribution. One kit can be ordered for a 1 x 2 configuration, one for a 1 x 4 configuration, two for a 1 x 6 configuration, and two for a 1 x 8 configuration.

Power Requirements

Input power is wired directly to the DPEC by the building electrician, through the access hole adjacent to terminal block TB1 on the left side of the power supply. Refer to section 5 of this volume for adjustments to the power supply to compensate for variations in input power.

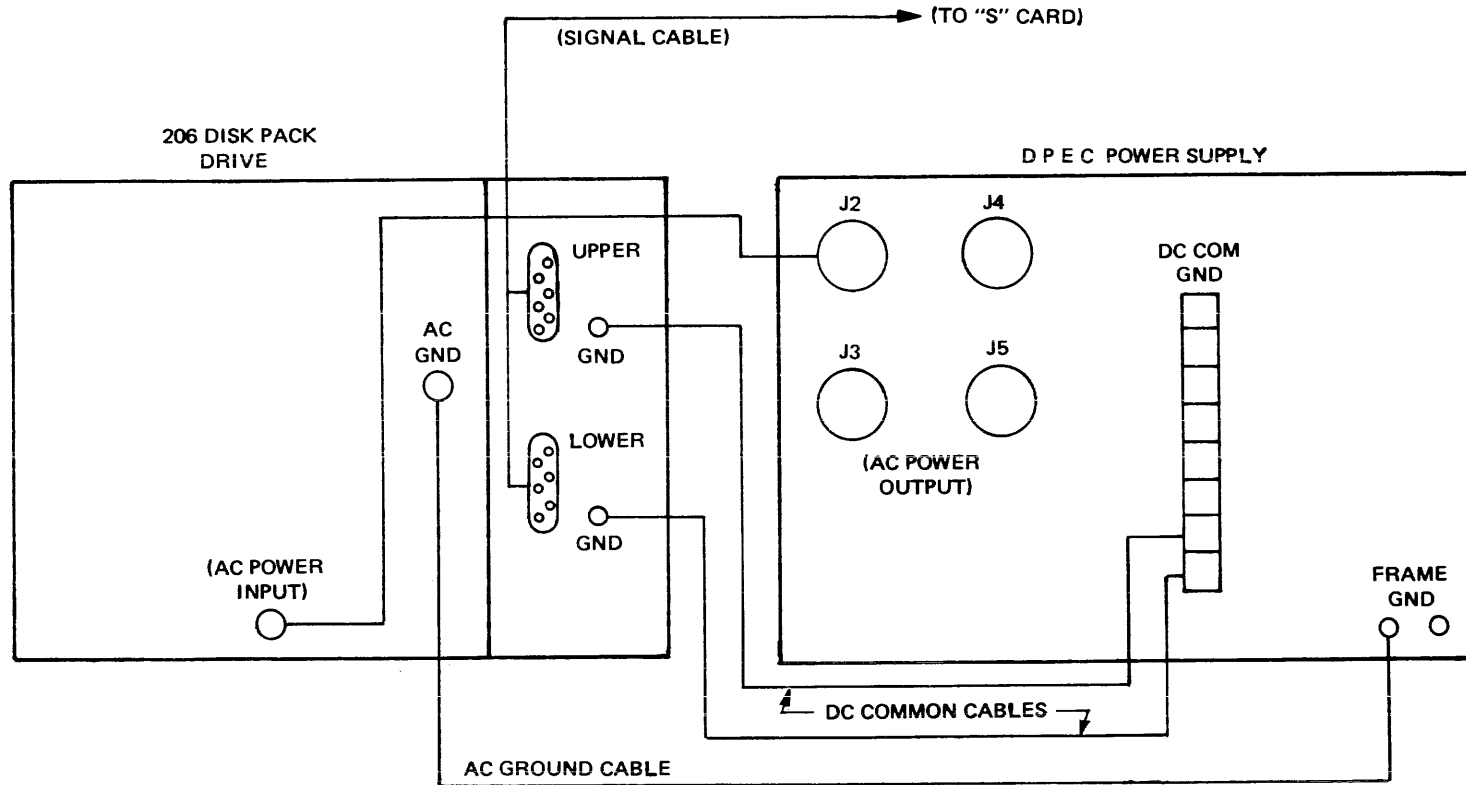
Voltage	208 to 240V +5%, -10%	
Frequency	50 ± 1 Hz or 60 ± 1 Hz	
	1 x 4	1 x 8
Power (208V three phase)	3.7 KVA	7.5 KVA
Current (208V three phase)		
Line 1	4A	12A
Line 2	8A	12A
Line 3	6A	10A
Power (240V single phase std. Int'l.)	3.7 KVA	7.5 KVA
Current (240V single phase std Int'l.)	18A	34A
Power factor	0.8	0.8
Power consumption (DPEC only)	300W	300W
Heat dissipation (DPEC only)	1024 BTU/Hr	1024 BTU/Hr
Air flow at a density of 0.075 lb/cubic foot (DPEC only)	300 CFM	300 CFM

Circuit Breaker Information

The DPEC and the power distribution subsystem in the DPEC are protected by time delay circuit breakers (20 amperes) that are rated at 1.75 times the current value of the 1 x 8 configuration, single phase, for a period of one minute.

Equipment Grounding

A separate equipment ground wire is required in addition to the neutral service connection. Additionally, a frame ground lug is also provided for connection to the DPD. To meet U.L. requirements, the building ground wire that is furnished by the input power cable must be connected directly to the DPEC frame ground lug. A jumper wire is connected between the frame ground lug and TP1-5 in the terminal box.



W11614

Figure 2-1. Cabling Diagram

A separate dc common lug is provided for connection to the DPD. The dc common wire is connected to the frame ground wire at a single point in the controller.

Drive Power Sequencing

AC power is distributed by the controller to the associated disk pack drives. Power-on and power-off of the disk pack drives are controlled by sequenced logic in the controller and disk pack drives.

The 206 DPEC will provide power-on sequencing to all attached units when the front panel RUN/STOP switch on the drive is activated. The sequencing will commence approximately 25 seconds after the DPEC is ready. Each unit will be commanded to power on at 8-second intervals. After this initial power-on sequence, all future power-on cycles will be done on the appropriate drive through use of the RUN/STOP switch.

Environment

Operating Environment

Temperature	60 to 100 degrees F (16 to 38 degrees C)
Relative humidity	10 to 90 percent

Shipment and Storage Environment

Temperature	50 to 160 degrees F (45 to 71 degrees C)
Relative humidity	up to 95 percent

Unpacking Instructions

All DPEC's shipped via air carrier will be in a packing crate. The crate consists of a pallet with cushion supports, tri-wall top, front, rear, and side cardboard panels. The DPEC is in a polyethylene bag. Edge protectors are used between the DPEC and the crate. The complete packing crate is then wrapped with two metal packing straps.

The following procedure is to be used to remove the DPEC from its packing crate.

- a. Remove the metal packing straps.
- b. Remove the crate cover.
- c. Remove the edge protectors from inside the crate.
- d. Carefully lift off the cardboard sleeve.
- e. Lift the DPEC off the shipping pallet.

WARNING

To prevent injury, at least two field engineers must assist in removing the DPEC from the pallet.

INSTALLATION PROCEDURE

Panel Removal

To remove any DPEC panel, two bolts must be loosened under the appropriate panel. Once these bolts are loose, lifting the panel approximately one-quarter inch will allow the top of the panel to be pulled away from the DPEC frame and the panel can be removed.

The maintenance plug-on packages will be located inside the DPEC beside the power supply.

An I/O cable and T & F documentation package will also be shipped with the DPEC.

AC Input Power

AC input power is wired directly to the DPEC by an electrician. A 2.5-inch by 10-inch access hole for ac input power is provided below TB1 on the left side of the power supply. Refer to the TB1 cover or the power supply schematic for details

NOTE

To meet U.L. requirements, the fifth wire (green/building ground) in the input power cable to the DPEC must not be connected to TB1-5. It must be connected to the frame ground lug on the DPEC chassis. A wire is then connected from the frame ground lug to TB1-5.

AC power for all disk pack drive units is obtained from the back of the DPEC power supply. The receptacles on the DPEC are labeled J2, J3, J4, and J5.

There are three circuit breakers on the front of the DPEC power supply: CB1, CB2, and CB3. CB1 is used to protect J2 and J3. CB2 is used to protect J4 and J5. CB3 is used to protect the DPEC power supply.

Cables

DC Common Cable

A dc common ground cable is placed between each disk pack drive spindle and the dc common ground terminal on the rear of the DPEC power supply.

AC Ground Cable

An ac ground cable is placed between the AC GND terminal on each disk pack drive ac panel and the FRAME GND terminal on the rear of the DPEC power supply.

Signal Cable

A signal cable is placed from the "S" card (in the DPEC) for up to four disk pack drive spindles. A

second signal cable connected to the "R" card is required for spindles 5 through 8.

I/O Cable

The processor I/O cable is attached to the "Q" card in the DPEC.

Drive Installation

Regardless of the configuration used, the voltage at receptacles J2, J3, J4 and J5 must be measured before inserting the disk pack drive line cords. Refer to the B 9484-5 Disk Pack Drive technical manual Volume I, form number 1084324 for the correct input voltage requirements to prevent serious damage to the drive.

SPECIAL INSTALLATION INSTRUCTIONS

See figure 2-2, DPEC power supply schematic.

Normal Three Phase Operation

The standard power that is intended for use with the 206 DPEC is three phase power that provides 208 to 240 volts (+5 percent, 10 percent) phase to phase, four or five wire. The 206 DPEC is wired for this configuration when it is shipped from the factory. Refer to the HIGH/LOW INPUT VOLTAGE adjustment in section 5 for the input voltage that exceeds 225 volts, phase to phase.

Single Phase Operation

The DPEC is capable of single phase operation if modifications are made on the DPEC power supply (see figure 2-3).

The maximum number of drawers that can be used is four. The drive units must be wired for line-to-line operation.

CAUTION

Under no circumstances may the voltage applied to FL1 (in the DPEC power supply) between lugs 1 and 3 exceed 250 volts ac.

International Installations

Only receptacles J2 and J5 on the DPEC are used. (Line to Neutral=208 to 240 volts.)

- a. Connect a jumper wire from TB1-1 to TB1-3.

- b. Connect the line lead to TB1-1.

- c. Connect the neutral lead to TB1-2.

- d. Connect the building ground lead to the frame ground screw provided.

NOTE

There is no connection to TB1-4. Do not use DPEC power receptacles J3 or J4. Do not make any modifications to the TB4 terminal strip in the DPEC power supply.

Domestic Installations

Only receptacles J2 and J5 on the DPEC are used. (Line to Line=208 to 240 volts, Line to Neutral=110 Volts.)

- a. Connect a jumper wire from TB1-1 to TB1-3.

- b. Connect line one to TB1-1.

- c. Connect line two to TB1-2.

- d. Connect the building ground lead to the frame ground screw.

CAUTION

Do not connect the neutral lead to any TB1 terminal.

NOTE

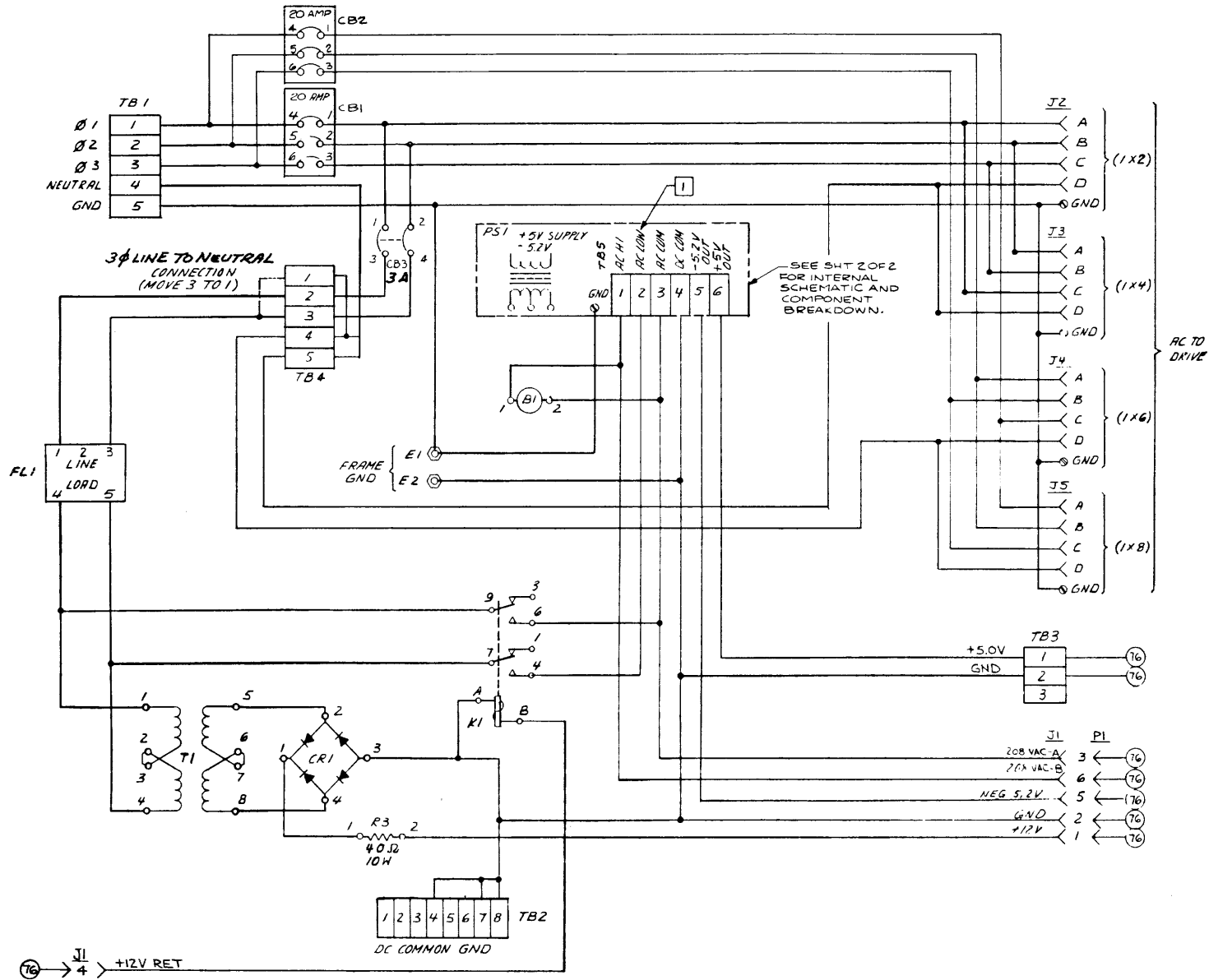
There is no connection to TB1-4. Do not use DPEC receptacles J3 or J4. Do not make any modifications to the TB4 terminal strip in the DPEC power supply.

NOTE

To meet U.L. requirements, the building ground lead in the input power cable must not be connected to TB1-5. This lead must be connected directly to the frame ground lug on the DPEC chassis. Another wire is then connected from the frame ground lug to TB1-5.

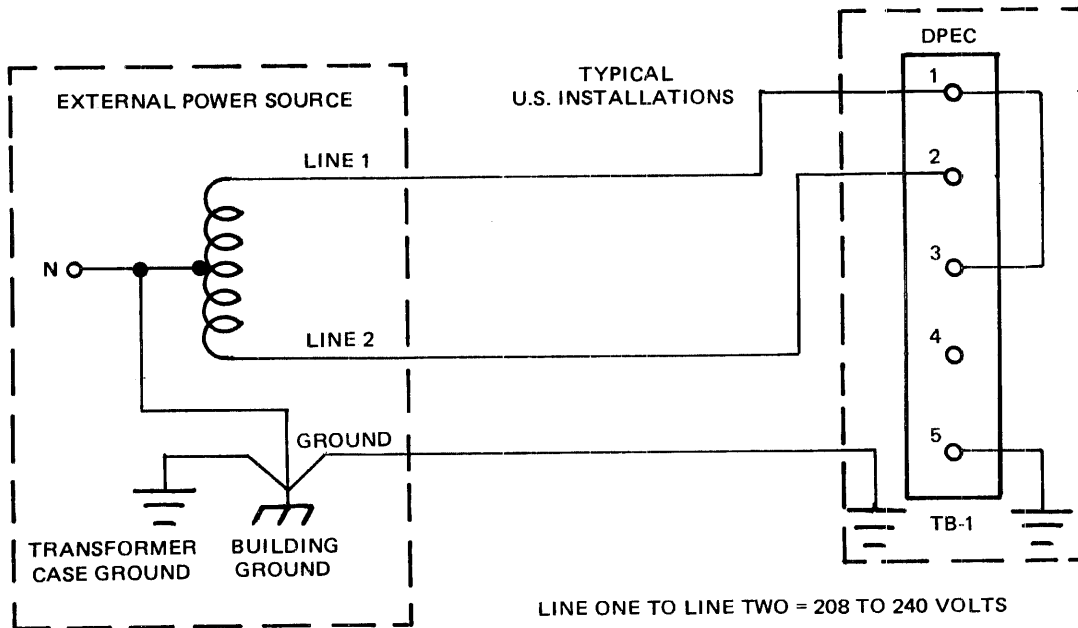
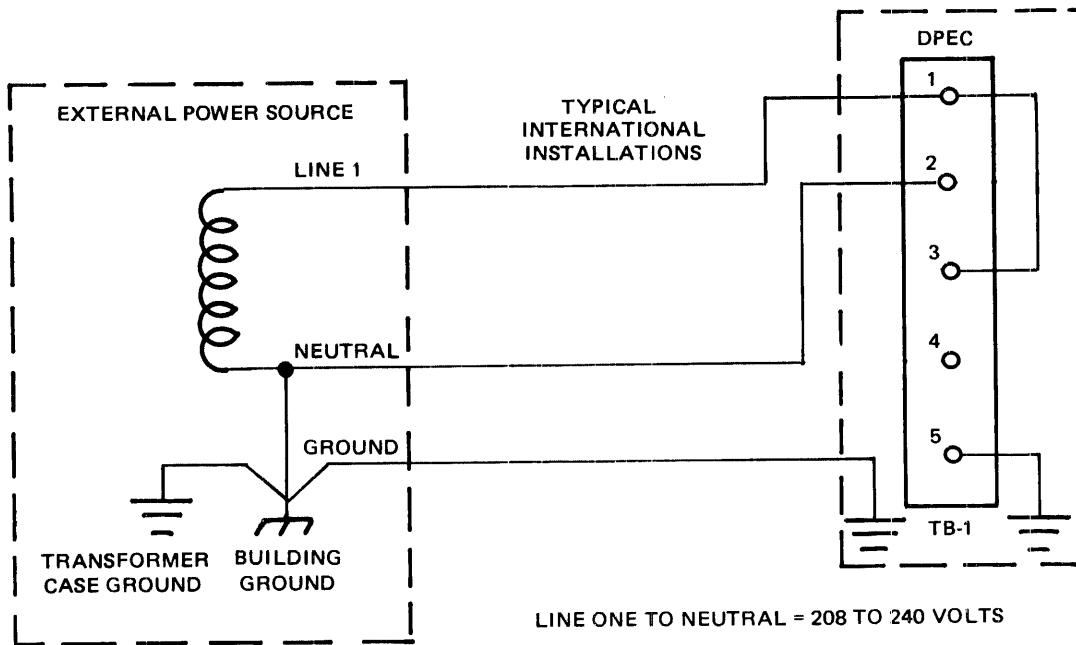
System Checkout

Revision AG (P/N CT 2211-0175) of the B 1700 disk pack subsystem test routine can be used to check out the disk pack subsystem. This revision is supplied with the DPC. Refer to section 4 for details.



W11615A

Figure 2-2. DPEC Power Supply Schematic



NOTE TO MEET U.L. REQUIREMENTS, THE GREEN (OR BUILDING GROUND) WIRE IN THE INPUT POWER CABLE TO THE DPEC MUST NOT BE CONNECTED TO THE DPEC. IT MUST BE CONNECTED DIRECTLY TO THE FRAME GROUND LUG ON THE DPEC CHASSIS. A WIRE IS THEN CONNECTED FROM THE FRAME GROUND LUG TO TB1-5.

W11616 A

Figure 2-3. Single Phase Input Power Connection

SECTION 3

DOCUMENTATION AND COMPONENTS

INFORMATION

This section contains material relating to the documentation, component location, and flow charts for the 206 DPEC.

RELATED DOCUMENTS

The following is a list of books and documents related to the operation and maintenance of the 206 DPEC.

- a. B 9499-3 Disk Pack Electronic Controller Theory of Operation, form no. 1095650.
- b. B 9484-5 206 Disk Pack Drive Function and Operation, form no. 1104189.
- c. B 9484-5 206 Disk Pack Drive Theory of Operation, form no. 1084332.
- d. B 1800/B 1700 Disk Pack Control II, form number 1098290.
- e. Test and Field Document, P/N 2161 1660.
- f. B 9499-3 DPEC Illustrated Parts Catalog, form no. 1104189.

PRINTED CIRCUIT CARDS

The printed circuit cards used in the DPEC are double sided boards into which 860 gold-plated socket terminals can be installed. Printed circuit wiring is used to distribute power and ground planes to the matrix terminals, and the socket terminals are configured to accept 14-pin or 16-pin dual in-line (DIL) integrated circuit packages. All of the integrated circuit modules, terminator resistors, decoupling capacitors, and potentiometers which comprise a card are pluggable; no solder is used to mount these components to the boards.

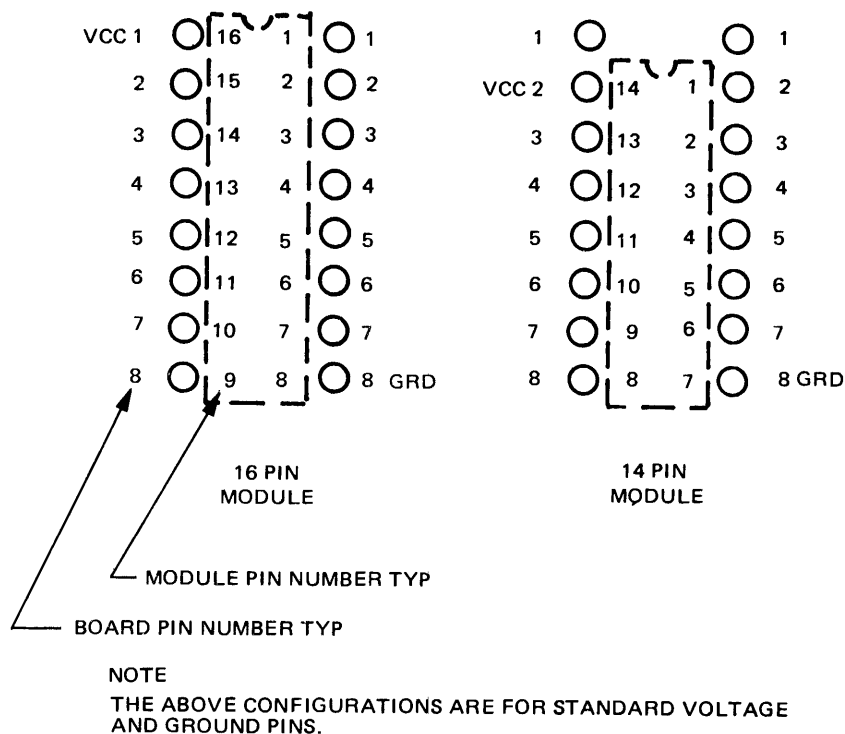
All connections on the card assembly backplane are wire wrapped. Two connections can be made on each card assembly backplane terminal.

A particular integrated circuit (IC) can be located by using the coordinate markings that appear on both sides of the cards. The IC locations will be listed on the schematics as two letters followed by a number: AB4, LM3, VW0, etc.

Figure 3-1 will be helpful in locating a particular integrated circuit leg for troubleshooting purposes.

The ground plane is the complete etching surface on the backplane or wiring side (#) of the card.

The +5.0 volts plane is the complete etching surface on the component side (\$) of the card.



W11617

3-1. Integrated Circuit Leg to Card Backplane Correlation (Backplane View)

Card Backplane Pin And Connector Pad Identification

Figure 3-2 illustrates the method used in the DPEC to locate a particular backplane pin on the card. Group row "Z" will be used to make connections to the card connector pads. All cards will have a top and a bottom section of backplane connector pads.

Cable Connector Cards

There are five cards in the DPEC that have connector pads at both ends of the card. The following discussion refers to only the cable connector ends of these cards.

Q, R, S, and P Cards

The Q, R, S, and P cards contain 40-edge connector pads, 20 pads on each side. The pads on the component side will be identified with a letter between "C" and "W" and will be preceded by a "\$" symbol. The pads on the wiring side will be preceded by a " " symbol.

All connector pad pins for both sides of the card will be located in group row 6 on the wiring or backplane side of the card. The coordinate method of pin identification is used in this row of pins. See figures 3-2 and 3-3.

F Card

The F card has a conventional card cage backplane connector pad array on both ends of the card. The maintenance control plug-on package is attached to this card. The plug-on package connector pad pins will be in group rows 6 and 7. See figure 3-2 for the coordinate designations.

Each DPEC is shipped with a set of Test and Field documents (T & F) which reflect the configuration of that particular DPEC. In some cases, a supplemental T & F document may also be included.

The following material will be found in the T & F package:

- a. DPEC block diagrams.
- b. Flow chart.
- c. Schematics for the cards and the power supply.
- d. Card assembly parts lists.
- e. Switch panel parts list.
- f. Power supply parts list and specifications.
- g. Backplane wiring list, signal name.
- h. Card wiring list.

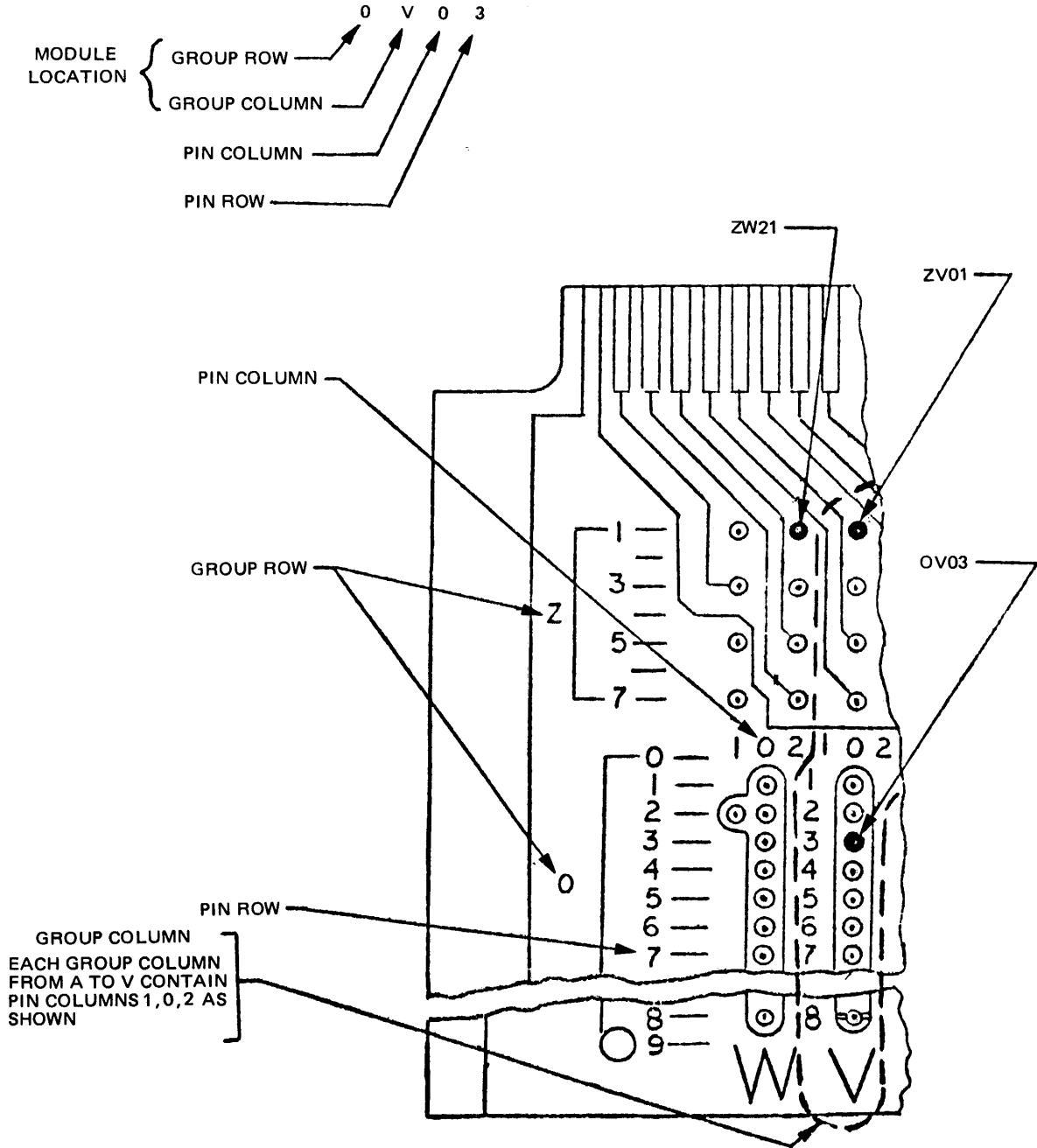
DPEC MODE DEFINITIONS

The 206 DPEC operates in 16 modes. Table 3-1 lists the basic function of each mode.

Table 3-1. Mode Functions

Mode	Function
0	Spindle spin up sequence.
1	Idle halt and initiatory OP processing.
2	Non overlap positioning routine.
3	Overlap positioning routine.
4	Op branching and disk location sync.
5	Read, write or verify address search.
6	Read, write or verify data transfer.
7	Initialize operation and index mark search routine.
8	Initialize and relocate writing operation.
9	Sector location counter sync routine.
10	Dead reckoning address search (relocate and read maintenance)
11	Write relocate flag routine.
12	Read maintenance data transfer.
13	Send ERD routine.
14	Test operation processing
15	Terminate and display result descriptor.

DESCRIPTION OF COORDINATE DESIGNATIONS
WIRING SIDE



W11618A

Figure 3-2. Card Backplane Pin Locating Scheme

DPEC FLOW CHART DESCRIPTION

The following paragraphs describe the use of the 206 DPEC detailed flow chart (see figure 3-4). The flow chart is for reference use only, refer to the flow chart in the T & F documentation package for the current revision.

The first page of the flow chart is an overall flow diagram which can be used as a guide in determining which modes can be accessed from any other mode. There is also a brief description of the operations that will take place at that particular mode.

The top half of the second page of the flow chart contains a guide to the use of the flow chart.

The abbreviations used are as follows:

Abbreviation	Meaning
HEAD	Header name
DO	Operation to be performed
MAKE	Make some particular thing happen
TEST	Condition to be tested.
GO TO	Name of header desired.
CMNT	Text of the comment
SYMBL	Symbol
EXEC TIME	Execution time
P--	Page number in schematics
YSSYM	Operation to be performed if test result is "yes."
NOSYM	Operation to be performed if test result is "no."

The actual flow chart begins on the third page. The left margin will contain the mode that the DPEC is in where the actions in that section are to take place.

There are four columns on the right side of the page. When a TEST condition is being performed, the first column will contain the mode to go to if the result of the TEST was a "yes." The second column on the right will contain the mode to go to if the result of the TEST was a "no." Other terms used during the TEST condition are NEXT, SKIP 1, AND BACK 1. NEXT indicates that the following line is to be performed, SKIP 1 indicates the next line is to

be skipped and the following line performed. BACK 1 is self explanatory.

Term names in parentheses are used to identify a term that is instrumental in the PERFORM statement preceding it.

When a DO, MAKE, or TEST statement is being performed, the third column on the right will contain the time when the statement will be performed. In some cases, the GO TO MODE statement can contain a location within a certain mode, for example, M5-4. This means that the operation will be performed at part 4 time of mode 5. It may be necessary to locate this new mode by searching the left margin on another page within the flow chart.

Unless otherwise specified, when a comment contains the phrase "GO TO MODE 'n' ", the SECTOR LOCATION COUNTER is cleared and the MAIN MODE COUNTER is set to the number indicated.

Figure 3-5 is a simplified flow chart of the 206 DPEC covering the READ, WRITE, or VERIFY operation codes. This flow chart is intended only as a quick reference. When detailed descriptions and timing information are required, refer to the detailed flow chart of figure 3-5.

Figure 3-6 is a simplified flow chart of an INITIALIZE operation. It begins at Mode 4 because there are no significant differences, prior to that mode, when compared to the READ, WRITE, or VERIFY simplified flow chart.

The following table (table 3-2) illustrates the main mode jump conditions.

The first column lists the MODE that is being entered.

Column 2 is the FINAL TERM name and the schematic where the term can be found.

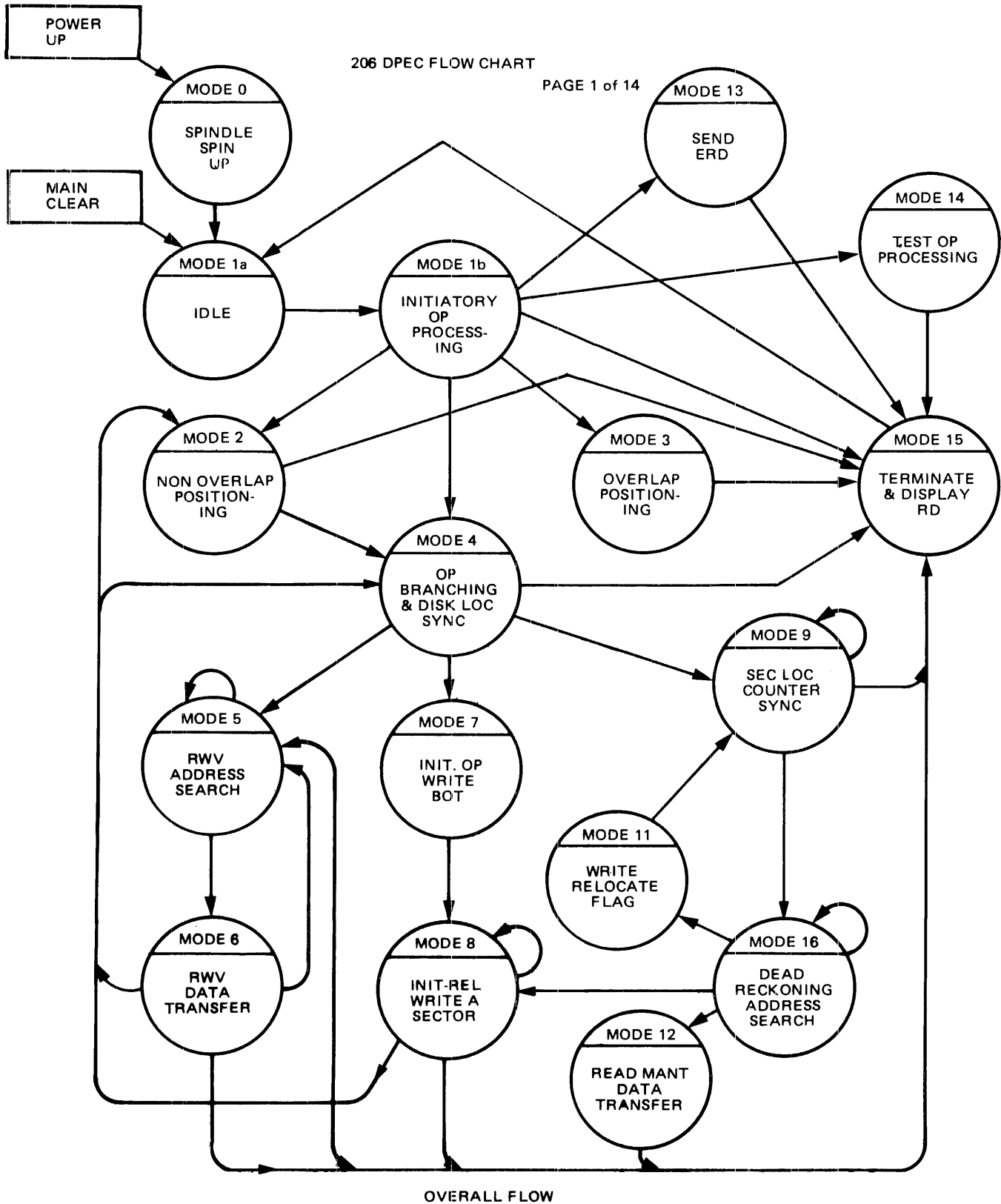
Column 3 contains the PARTIAL TERMS (default names) needed to derive the final term.

Column 4 has SUB PARTIAL TERMS, where applicable, and the page numbers.

Column 5, FROM MODE, lists the modes that the DPEC may be in prior to entering a particular mode.

Column 6 contains the conditions needed to produce the "GO TO MODE" term.

The final column, 7, contains the SOURCE PIN and PAGE DPEC to the opposite mode, press the REMOTE button. NUMBER for the PARTIAL TERM names.



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Figure 3-4. Detailed DPEC Flow Chart (Sheet 1 of 14)

```

-----
HEAD  HEADER NAME
DO    OPERATION TO BE PERFORMED      SYMBL  ---- EXEC TIME  P--
MAKE  SOME PARTICULAR THING HAPPEN  SYMBL  ---- EXEC TIME  P--
TEST  CONDITION TO BE TESTED        YSSYM  NOSYM TEST TIME  P--
GOTO  NAME OF HEADER DESIRED        SYMBL  ----
CMNT  TEXT OF THE COMMENT
-----

```

CMNT MODES 0 THRU 9 ARE NAMED MDE0 THRU MDE9;
MODES 10 THRU 15 ARE NAMED MD10 THRU MD15.
THE CONTROL SIGNALS WHICH CAUSE THESE GOTO'S ARE NAMED
GOT0MDE0 THRU GOT0MDE9 AND GOT0MD10 THRU GOT0MD15. P 46-49

CMNT SAYING "GO TO MODE N" IMPLIES (UNLESS NOTED OTHERWISE):
1. THE CLEARING OF SECTOR LOCATION COUNTER, AND
2. CAUSING MAIN MODE TO GO TO THE NUMBER MENTIONED.

HEAD >>>>>>>>>> START OF FLOW CHART <<<<<<<<<<<<

```

TEST IS AC POWER ON YET?          NEXT  SAME      P77
DO  PWR RESET _ TO ENTIRE _ DPEC  MDE0                P42
                                (PWRRESYN  P71
                                (PWRRESET)
-----

```

```

>>>>>>>>>> MDE0 MDE0 MDE0 MDE0 MDE0 MDE0 MDE0 <<<<<<<<<<<<
MDE0 HEAD SPINDLE SPIN-UP SEQUENCE - MODE 0 P50
-----

```

CMNT WE GET HERE FROM A POWER RESET ONLY -
POWER RESET LASTS ABOUT 25 SECONDS P71
CMNT MAIN MODE = 0, UNIT CNTR = 0, SEC LOC CNTR = 0
INSECLOC = HI, CLOCK = LOCAL P51

```

SPIN HEAD SPINDLE SPIN-UP SEQUENCE
TEST DRIVE THERE? (DR_THERE) W1811 P7
DO MAKE CM_SEL = HI (CM_SEL) W281 P55
CMNT SETCMSEL CLEARS DM_RCVD FF
DO MAKE SW_TO_DR = HI FOR ONE BIT TIME W281 P55
TEST HAS A DM BEEN RECEIVED? (DM_RCVD) SP_1 SP_2 W5815 P23
-----

```

```

SP_1 CMNT DRIVE PRESENT AND POWERED ON
DO SEND PWR-UP CM TO DRIVE (MDE0) CM_LOAD AT W5815 P50,62
DO START 8-SECOND TIMER (ST_8TIMR) W5815 P56
DO HALT SEC LOC COUNTER (INSECLOC=LO) W5815 P54
-----

```

CMNT SEC LOC CNTR TO STAY OFF UNTIL TIMER FINISHES

```

TEST 8-SEC TIMER FINISHED? (TMOT8SEC) NEXT SAME TMOT8SEC P37
DO FREE SEC LOC COUNTER (INSECLOC=HI) TMOT8SEC P51
-----

```

```

DO MAKE CM_SEL = LO (CM_SEL) W6815 P55
DO SWITCH TO LOCAL CLOCK (SW_LOCAL) W6815 P55
SP_2 DO INCREMENT UNIT COUNTER (INUNITCT) W6815 P57
-----

```

```

TEST UNIT CNTR BIT 2*3 ON? (UNTCT2*3) SP_3 NEXT W8815 P4
DO CLEAR SEC LOC CNTR (CLSECLOC) W8815 P52
GOTO TOP OF SPINDLE SPIN-UP SEQUENCE SPIN W8815 .
-----

```

```

SP_3 CMNT THIS IS THE END OF THE SPINDLE SPIN-UP SEQUENCE
DO CLEAR SEC LOC CNTR (CLSECLOC) W9815 P52
DO HALT SEC LOC COUNTER (INSECLOC=LO) W9815 P54
GOTO IDLE HALT, INITIATORY PROC - MODE1 MDE1 W9815 .
-----

```

Figure 3-4. Detailed DPEC Flow Chart (Sheet 2 of 14)


```

>>>>>>>> MDE4 MDE4 MDE4 MDE4 MDE4 MDE4 MDE4 <<<<<<<<<<<<
MDE4 HEAD OP BRANCHING & DISK LOC SYNC - MODE 4

  CMNT MDE4FLOP IS SET ((MDE2+MDE8)*INITIAL)+MDE6 TO REMIND US TO P56
  DO A HEADSWITCH BEFORE SEARCHING FOR INDEX OR
  DOING OP BRANCHING

  TEST IS MODE 4 FLOP SET?      (MDE4FLOP)   M4_1  M4_0                P53

M4_1 DO SEND HEAD SWITCH CM      (ENABL_WR)   CM_LOAD AT  W1811      P60,62
DO CLEAR MODE4 FLOP            (MDE4FLOP)   W9815      P56
DO CLEAR SECTOR LOC CNTR      (CLSECLC)   M4_0      W9815      P52

  CMNT AFTER EXECUTING THE ABOVE STATEMENTS,
  CONTROL IS RETURNED TO THE BEGINNING
  OF MDE4 WITH MDE4FLOP RESET.

M4_0 TEST READ,WRITE,VERIFY OPS? (RWV)      M4_0B  M4_0A                P45
M4_0A HEAD NOT RWV ROUTINE
DO CLEAR DISK LOC CNTR        (CLDSKLOC)   W0815      P54
DO START 25 MSEC TIMER        (ST25TIMR)   W0815      P54
DO SEND INDEX SEARCH CM      (INDXSrch)   CM_LOAD AT W0815      P53,62
DO HALT SEC LOC COUNTER      (INSECLOC=LO)   W0815      P54

  CMNT THE SEC LOC CNTR NOW SITS HALTED IN THE - - W180 STATE.
  CMNT WE NOW WAIT FOR EITHER THE INDEX MARK DM TO RETURN
  OR FOR THE 25 MSEC TIMER TO FINISH.

  CMNT WE ARE ASSURED THAT ADDRINDX WILL BE FALSE AT THIS TIME
  BECAUSE OF THE TWO DM'S WE RECEIVED IN MODE 1, NEITHER
  OF WHICH COULD HAVE HAD THIS BIT ON.

  TEST INDEX MARK DM BACK YET? (ADDRINDX) SKIP1 NEXT  ADRIDXUP      P24
  TEST 25 MSEC TIMER FINISHED? (TMOT25MS) MD15  BACK1  TIME_OUT      P37
  CMNT TMOT25MS SETS TRY DIAG.

  CMNT WE WILL SEE THE UP EDGE OF THE ADDRINDX LINE SOMETHING
  LIKE EIGHT (8) BIT TIMES AFTER THE BEGINNING OF THE DM.
  WE WILL J UP THE INSECLOC FF WITH THE TERM P54
  GS GTO ENC * GOTOMDE1/ WHICH WAS CAUSED BY ADDRINDX.

DO FREE SEC LOC COUNTER      (INSECLOC=HI)   ADRIDXUP      P51
TEST INITIALIZE OP          (INITIAL)   SKIP1 NEXT  ADRIDXUP      P47
DO INCREMENT DISK LOC CNTR  (INDSKLOC)   ADRIDXUP      P51

  TEST INITIALIZE OP?        (INITIAL)   MDE7  MDE9  ADRIDXUP      P47

-----
M4_0B HEAD RWV WAIT ROUTINE
DO SEND OFFSET/PLO CM      (CM#1-0)   W0815      P62
TEST IS DRIVE READY        (DR_READY)   NEXT      W9814      P24
DO HALT SEC LOC COUNTER    (INSECLOC=LO)   W9814      P54
CMNT SEC LOC CNTR NOW HALTED IN THE - - - W9815 STATE
TEST IS DRIVE READY?      (DR_READY)   NEXT  SAME  W9815      P24
DO FREE SEC LOC COUNTER    (INSECLOC=HI)   P51
GO TO MODE 5              (GOTO5FR4)   MDE5  W11814      P73
-----

```

W11620 (Sheet 5 of 14)

Figure 3-4. Detailed DPEC Flow Chart (Sheet 5 of 14)


```

M5_3 HEAD ACTUAL ADDRESS COMPARE
CMNT THE ADDRESS COMPARE IS HANDLED AUTOMATICALLY BY THE
      ADDRESS LOGIC BLOCK'S CONTROL AND THE RESULTS OF THE
      COMPARE WILL BE AVAILABLE AT W784 TIME.

DO   LOAD SEC LOC CNTR TO W584 (LDSECLOC)          STADRCMP      P38
DO   SEND GO IDLE CM          (CMGOIDLE/) CM_LOAD AT W686      P60,62
TEST HEADER ADDR = ADDR CNTR (ADDR_EQL) MDE6 M5_4 W784      P15

CMNT AS WE GO TO MODE 6 WE DO >>NOT<< CLEAR
      THE SECTOR LOCATION COUNTER.
-----

M5_4 HEAD NO COMPARE ROUTINE
CMNT THE ADDR MARK COUNTER IS USED TO KEEP TRACK OF
      HOW MANY ATTEMPTS WE HAVE MADE AT FINDING THE
      DESIRED SECTOR. IT IS CLEARED BY MODE 1 AND
      INCREMENTED AT W784 TIME IF ADDRESS COMPARE WAS
      NOT EQUAL. WHEN ADMRK127 GOES TRUE WE
      CHECK TO SEE IF WE ARE ALREADY ON HEAD 4, AND IF NOT
      WE SWITCH THERE AND CONTINUE SEARCHING
      FOR THE CORRECT ADDRESS (AMONG THE SPARES) UNTIL
      THE ADDR MARK CNTR EQUALS 255. AT THIS POINT WE
      GO TO MODE 15 AND REPORT NO ADDRESS COMPARE.

DO   INCREMENT ADDR MARK CNTR (INADMRK)           W784          P45

CMNT WE PERFORM THESE NEXT TESTS AT WORD 14 TIME TO USE
      PRODUCT TERMS IN COMMON WITH THE M1_3 ROUTINE.

TEST ADDR MARK CNTR = 255? (REVSDONE) MD15 NEXT W1480      P71
TEST IS ADDR MARK 2*7 BIT ON? (ADMRK127) NEXT MDE5 W1481   P47
TEST ARE WE ON HEAD 4 ? (ACHED2*2) MDE5 NEXT W1482        P47
DO   FORCE HEAD=4 TO CM INPUT (CMSELHD4)          W1482        P71
CMNT ADDRESS COUNTER REMAINS UNCHANGED. WE JUST WANT
      TO SEARCH THE RELOCATED AREA ON SURFACE 4 TO FIND
      THE SECTOR. THE CMSELHD4 LINE WILL BE RESET
      UPON ENTERING MDE6.

DO   SEND HEAD SW CM          (ENABL_WR) CM_LOAD AT W1483   P60,62
CMNT LOADING OF THE CM REGISTER TAKES PLACE THROUGHOUT
      THE WHOLE W1483 TIME. WE CAN THEREFORE BE SURE THAT
      THE HEAD=4 DATA IS STABILIZED FOR LOADING.

TEST ROGER DM BACK? (ROGER_DM) MDE5 MD15 W2988          P70
CMNT IN MODE 5 WE GO TO MD15 ANYTIME THE DPC
      DESELECTS US AND ENSELTRM IS TRUE.
-----

```

W11620 (Sheet 7 of 14)

Figure 3-4. Detailed DPEC Flow Chart (Sheet 7 of 14)

```

>>>>>>>> MDE6 MDE6 MDE6 MDE6 MDE6 MDE6 MDE6 <<<<<<<<<<<<
MDE6 HEAD READ-WRITE-VERIFY DATA TRANSFER - MODE 6

CMNT WE ENTER THIS MODE FROM A REAL-TIME ADDRESS COMPARE.
THE SEC LOC CNTR IS >>NOT<< CLEARED AS WE ENTER.

TEST IS THIS A WRITE OP?      (WRITE)   WRIT READ          P65
-----

READ HEAD DATA TRANSFER FOR READ AND VERIFY OPS

DO SEND READ DATA CM          (CM_R/W/) CM_LOAD AT W10B14    P61,62
CMNT THIS CM GOES ACTIVE AT THE DRIVE AT - - - - W11B12 TIME .
WHICH IS 9 WORD TIMES AFTER THE END
OF THE ADDRESS FIELD.

DO ENABLE SYNC DETECTOR      (ENSNCDET)          W1486          P57
CMNT ENSNCDET SHOULD BE RESET AT W11B15 TIME.

TEST SEEN DATA SYNC CHAR YET? (STDAXFR) SKIP2 NEXT STDAXFR    P38
TEST OVERRUN SYNC CHAR FIELD? (W2988) NEXT BACK1 W2988        P36
DO SET DATA SYNC OVERRUN FF (DTSYNCER) MD15 W2988            P56
DO CLEAR REVSDONE COUNTER W2988 P71
DO CLEAR ENSNCDET STDAXFR P57
MAKE FRMT CTRL MODE=READ DATA (FMRCDATA) STDAXFR P58

CMNT THE FORMAT CONTROL LOGIC WILL NOW HANDLE
THE DETAILS OF THE DATA FLOW.

MAKE FRMT CTRL MODE=READ FIRE (FMRDFIRE) W106B15 P58
MAKE FRMT CTRL MODE = SEND RD (FMSENDRD) W108B15 P58
DO SEND A GO IDLE CM (CMGOIDLE/) CM_LOAD AT W109B1 P60,62
CMNT FORMAT CONTROL GOES IDLE AT W109B15 AS A RESULT
OF THE PREVIOUS FMSENDRD.

GOTO RWV END TEST ROUTINE M6_1
-----

WRIT HEAD WRITE OP DATA TRANSFER ROUTINE

DO SEND A WRITE DATA CM      (CM_R/W) CM_LOAD AT W885 P61,62
MAKE FRMT CTRL MODE=WRIT ZERO (FMWRZERO) W885 P52
CMNT THE WRITE DATA CM GOES ACTIVE AT - - - W9B3 TIME. .

MAKE FRMT CTRL MODE=WRIT ONES (FMWRONES) W16B9 P58
MAKE FRMT CTRL MODE=WRIT DATA (FMWRDATA) W16B13 P58
MAKE FRMT CTRL MODE=WRIT FIRE (FMWRFIRE) W106B13 P58
CMNT FRMT CTRL GOES TO WRZERES AT W108B13 AS A RESULT
OF THE PREVIOUS WRFIRE. IF OP IS NOT INITIAL,
FRMT CTRL GOES IDLE AFTER WRITING 1 BYTE OF ZEROES.
DO SEND A GO IDLE CM (CMGOIDLE/) CM_LOAD AT W109B1 P60,62
CMNT DRIVE WILL GO IDLE AT END OF - - - W109B7 TIME. .

CMNT WHEN THE FORMAT CTRL LOGIC IS GIVEN THE
TERMINATE WRITE COMMAND, IT STAYS IN THE TERM WR
MODE FROM W105B14 THRU W106B13, THEN IN THE WRITE
FIRE MODE FROM W106B14 THRU W108B13, THEN IN THE
WRITE ZEROS MODE FROM W108B14 THRU W109B7 AT WHICH
TIME IT GOES BACK INTO THE IDLE MODE.

GOTO THE RWV END TEST ROUTINE M6_1
-----

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W11620 (Sheet 8 of 14)

Figure 3-4. Detailed DPEC Flow Chart (Sheet 8 of 14)


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>>>>>>>> MDE9 MDE9 MDE9 MDE9 MDE9 MDE9 MDE9 <<<<<<<<<<<<
MDE9 HEAD SEC LOC CNTR SYNC ROUTINE - MODE 9

CMNT IN THE RELOCATE AND READ MAINTENANCE OPS WE FIND
      THE DESIRED ADDRESS BY DEAD RECKONING (DISK LOC CNTR)
      AND MUST KNOW ONE SECTOR IN ADVANCE OF AN ADDRESS COMPARE.
      THIS IS WHY WE GIVE THE EXTRA INC DISK LOC UPON ENTERING.
      WHEN WE LOOP BACK AFTER CYL-HEAD NOT EQUAL, WE INC
      AGAIN TO MAINTAIN DISK SYNC.
P51
P15

DO SND RD ADDRMRK CM (CM_R/W/,CM ADD M/) CM_LOAD 2 W1B11 P61,62
DO START 250 USEC TIMER (ST250TMR) W1B11 P56

CMNT A ROGER DM SHOULD BE BACK BY - - - - - W3B14 TIME.
TEST IS A ROGER DM BACK? (ROGER_DM) NEXT MD15 W3B14 P70
CMNT THIS MD15 JUMP SETS TRY DIAG. (BADDRSP) P73

DO HALT SEC LOC COUNTER (INSECLOC=LO) W3B14 P54

TEST ADDR MARK DM BACK YET? (ADDRINDX) M9 1 NEXT ADRIDXUP P24
TEST 250-USEC TIMER FINISHED? (TMOT250U) NEXT BACK1 TIME_OUT P37

DC SET ADDRESS MARK ERROR FF(ADMRKER) NEXT P68
-----

M9_1 DO FREE SEC LOC COUNTER (INSECLOC=HI) TMOT250U+ADRIDXUP P51
TEST TIMEOUT 250USEC (TMOT250U) MDE9 NEXT P73
CMNT THE SEC LOC CNTR HAS BEEN HALTED IN THE W4B0 STATE.
      WE NEED TO CHECK THE TIME LAPSE FROM THE ADDR MARK DM
      TO WHEN THE ADDR SYNC CHAR IS TO ARRIVE. THE LONGEST
      THAT THIS SHOULD BE IS NINE (9) WORDS. WE WILL ALLOW
      TEN (10) WORD TIMES. WHEN WE SEE THE ADDR SYNC CHAR,
      WE WILL LOAD THE SEC LOC CNTR TO W5B4 (FROM WHEREVER
      IT WAS) AND GO TO MODE 10. IF THE COUNTER GETS TO
      W1B15, WE WILL SAY THAT WE HAVE OVERRUN THE ADDR SYNC
      CHAR FIELD.

TEST ADDR SYNC CHAR DETECTED? (STADRCMP) M9 2 NEXT STADRCMP P38
TEST PASSED ADDR SYNC FIELD? (W1B15) NEXT BACK1 W1B15 .
-----

M9_2 HEAD ACTUAL ADDRESS COMPARE

CMNT THIS COMPARE IS BETWEEN THE HEADER ADDRESS AND THE CONTENTS
      OF THE ADDRESS COUNTER JUST AS IN RWV, BUT ONLY THE
      CYLINDER AND HEAD PORTIONS OF THE COMPARE ARE USED.

CMNT THE ADDRESS COMPARE IS HANDLED AUTOMATICALLY BY THE
      ADDRESS LOGIC BLOCK'S CONTROL AND THE RESULTS OF THE
      COMPARE WILL BE AVAILABLE AT W7B4 TIME.

DO SEND GO IDLE CM (CMGOIDLE/) CM_LOAD AT W6B6 P60,62
TEST CYL AND HEAD COMPARE? (CYLHDEQL) MD10 M9_3 W11B14 P15

CMNT WE >>DO NOT<< CLEAR SEC LOC CNTR WHEN GOING TO MODE 10.
-----

M9_3 HEAD NO COMPARE ROUTINE

CMNT THE ADDR MARK COUNTER IS USED TO KEEP TRACK OF
      HOW MANY ATTEMPTS WE HAVE MADE AT FINDING THE
      CORRECT TRACK ADDRESS. IT IS CLEARED BY MODE 1 AND
      INCREMENTED AT W7B4 TIME IF ADDRESS COMPARE WAS
      NOT EQUAL. WHEN ADMRK127 GOES TRUE WE
      GO TO MODE 15 AND REPORT NO TRACK COMPARE.

DO INCREMENT ADDR MARK CNTR (INADMRK) W11B14 P45
TEST IS ADMRK127 BIT ON? (ADMRK127) NEXT MDE9 W11B14 P64
DO INDSKLOC (INDSKLOC) W11B14 P51
DO GO TO MD15 (PT3GMD15) W13B15 P48
-----

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W11620 (Sheet 11 of 14)

Figure 3-4. Detailed DPEC Flow Chart (Sheet 11 of 14)


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>>>>>>>> MD14 MD14 MD14 MD14 MD14 MD14 MD14 <<<<<<<<<<<<
MD14 HEAD TEST OP PROCESSING - MODE 14

CMNT TESTOP IS MERELY TO INFORM THE PROCESSOR OF THE
      STATUS OF THE DRIVE AND OPTIONALLY TO POWER IT DOWN
      OR TO CLEAR ALL SEEK STATUS FF'S. P55

TEST POWER DOWN REQUESTED? (N3) NEXT SKIP1 W0B14 P4
DO SEND POWER DOWN CM (MD14) CM_LOAD AT W0B14 P50,62

TEST CLEAR ALL SKSTATUS FF? (N2) NEXT SKIP1 W0B14 P4
DO CLEAR ALL SKSTATUS FF'S (CLALSKST) W0B14 P55

GOTO TERMINATE AND DISPLAY RD - MODE 15 MD15 W0B14 P49
-----
>>>>>>>> MD15 MD15 MD15 MD15 MD15 MD15 MD15 <<<<<<<<<<<<
MD15 HEAD TERMINATE AND DISPLAY RD - MODE 15

CMNT IN ALL OPS EXCEPT TESTOP AND SEND_ERD, WE MUST ASK
      THE DRIVE TO SEND THE CONTENTS OF ITS STATUS REGISTER
      SO WE CAN SEE IF IT HAS A TEMP WARNING CONDITION. P67

DO DROP READY LINE (READY) GTM10R15 P56
TEST IS THIS OP A TESTOP? (TESTOP) M15B NEXT W0B14 P67
TEST IS OP A TRANSMIT ERD? (SEND_ERD) M15B NEXT W0B14 P67
TEST DO WE NEED TO RESTORE? (NDTORSTR) M15A NEXT W0B14 P57
TEST WAS THIS A LONG DM TRM./ (LONG_DM) M15B NEXT W0B14 P73
DO SEND "SEND STATUS" CM (SEND_STS) CM_LOAD AT W0B14 P60,62

CMNT DM SHOULD BE BACK BY - - (DM_RCVD) - - - W8B14 TIME P23
GOTO . . . . . M15B W8B15 P35
-----
M15A HEAD THIS IS THE RESTORE ROUTINE
DO SND RSTR-SNDSTS CM (SEND_STS,RESTORE) CM_LD AT W0B14 P54,60,62
DO UPDATE OLD CYL MEMORY (CKADDMEM) W0B14 P62
DO HALT SEC LOC COUNTER (INSECLOC=LO) W0B14 P54
DO FREE SEC LOC CNTR (INSECLOC=HI) W0B15
DO GO TO MODE15B M15B W8B15 P35
-----
M15B HEAD DISPLAY RD AND DROP BUSY SEQUENCE

MAKE FRMT CTRL MODE = SEND RD (FMSENDRD) W8B15 P58
MAKE FRMT CTRL MODE = IDLE (FMGOIDLE) W9B15 P58

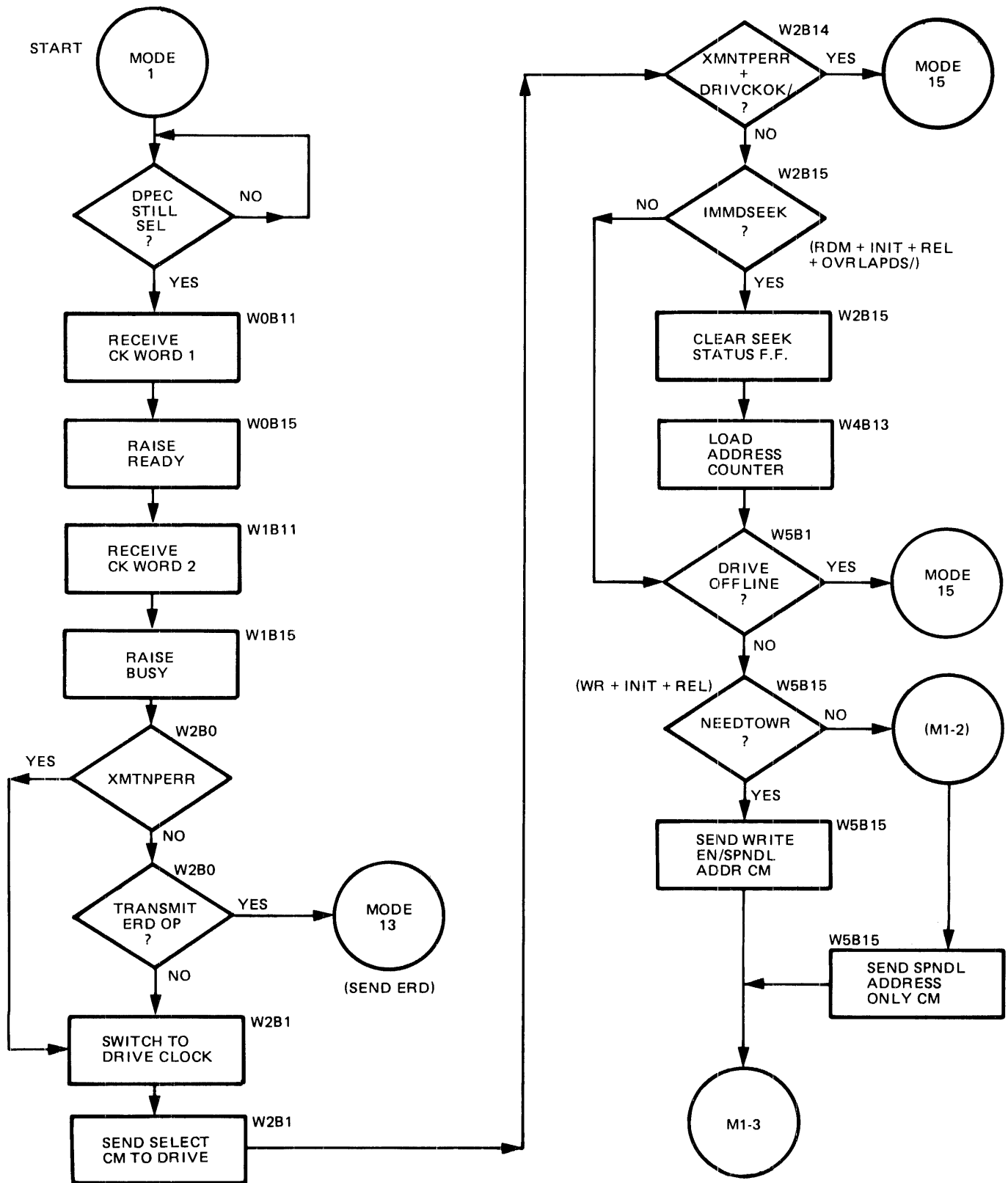
CMNT THE ACTUAL RD CK_DPC WILL BE AT . . . . W10B12-14 P66

DO DROP BUSY (KTRMBUSY) W11B14 P56
DO GO IDLE (GOTOMDE1) MDE1 W11B14 P46
-----

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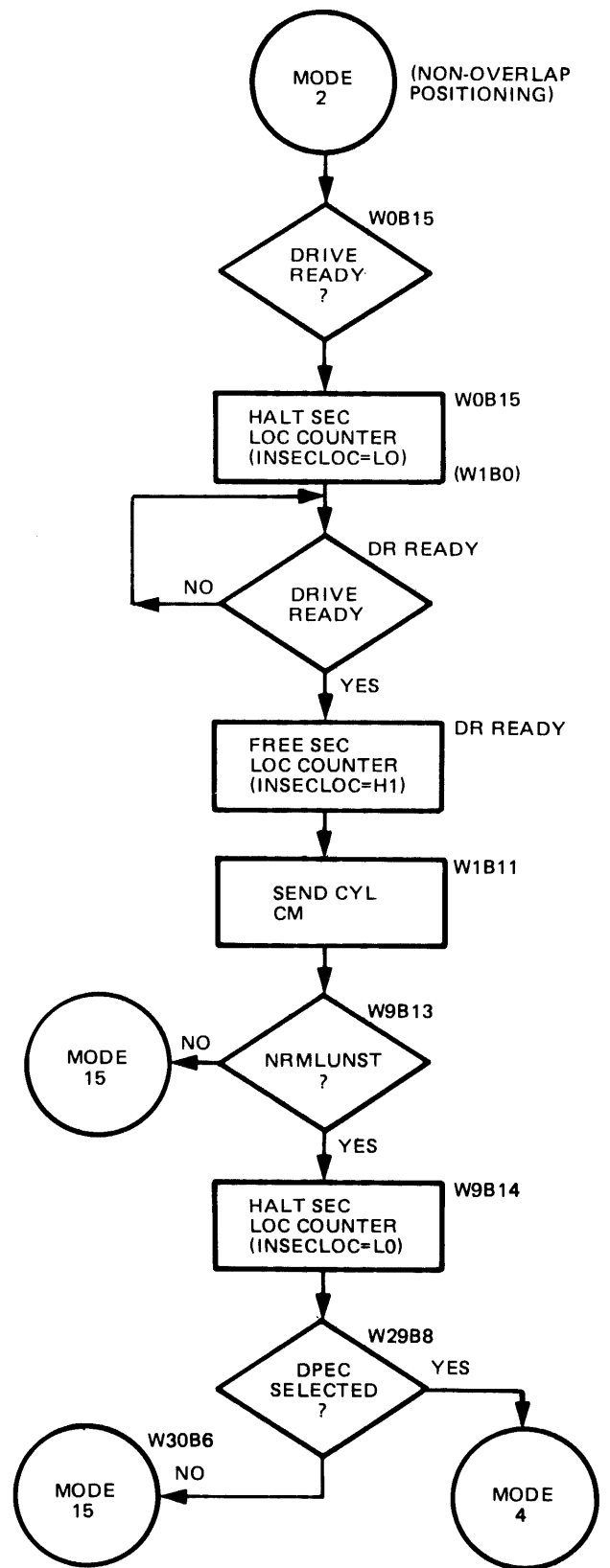
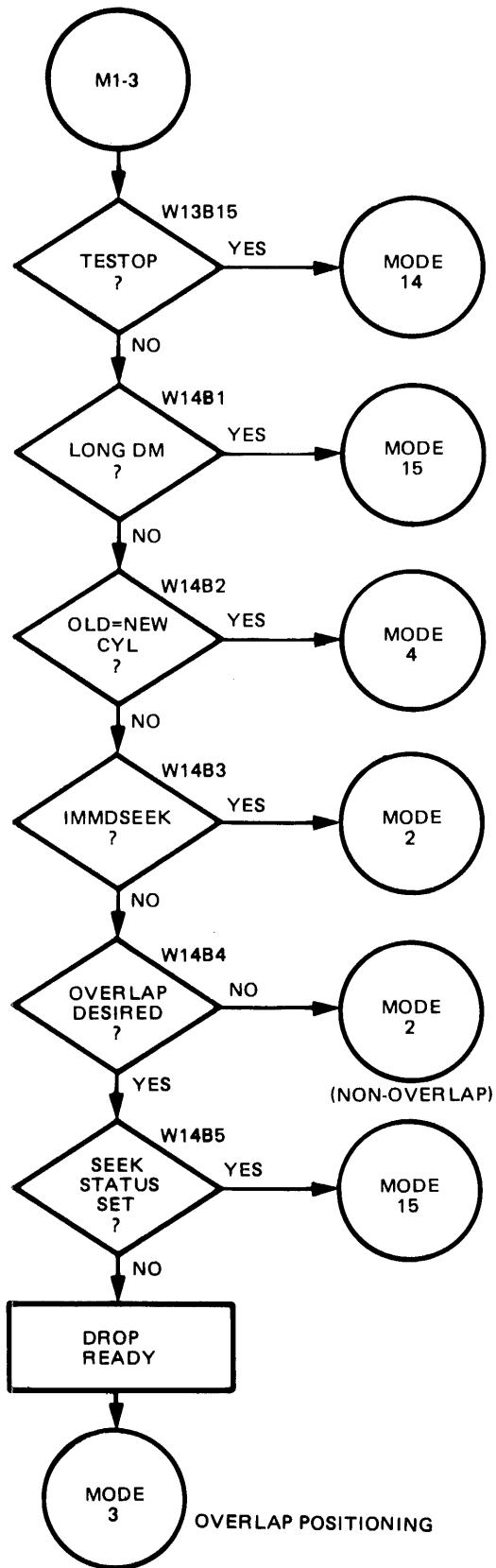
W11620 (Sheet 14 of 14)

Figure 3-4. Detailed DPEC Flow Chart (Sheet 14 of 14)



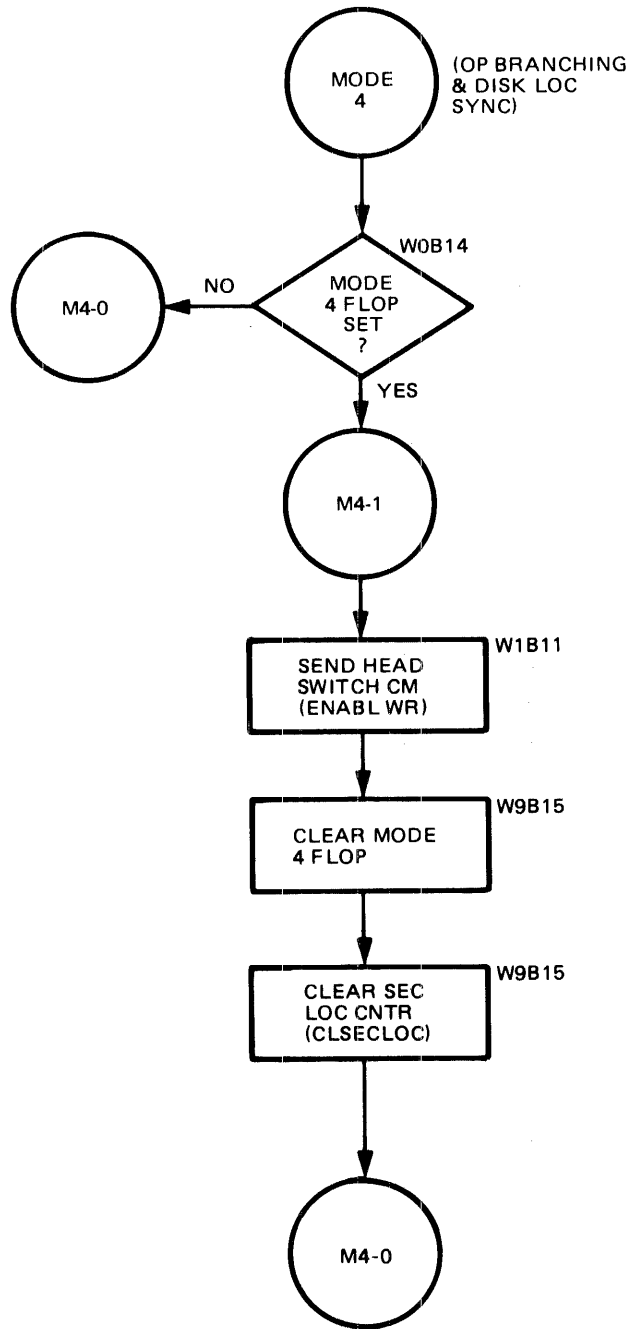
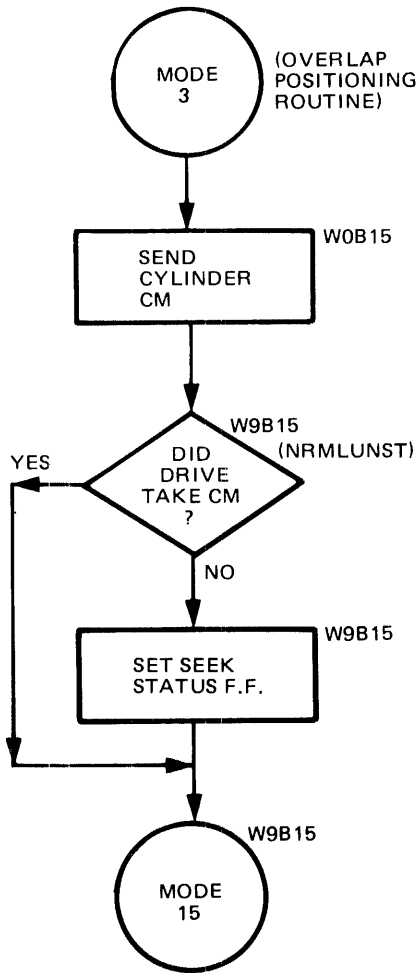
W11621 (Sheet 1 of 13)

Figure 3-5. Read and Write and Verify Operation (Sheet 1 of 13)



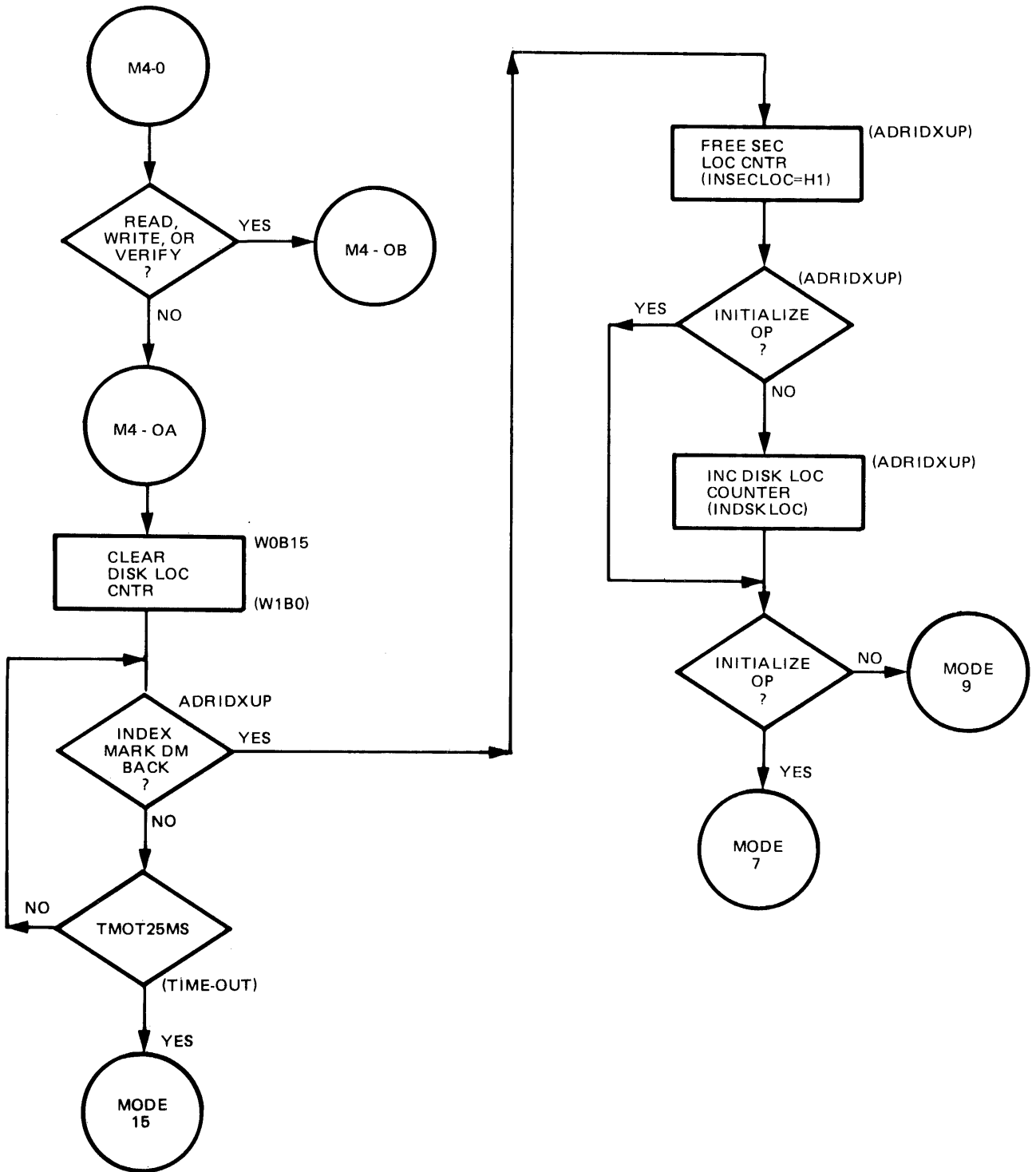
W11621 (Sheet 2 of 13) A

Figure 3-5. Read and Write and Verify Operation (Sheet 2 of 13)



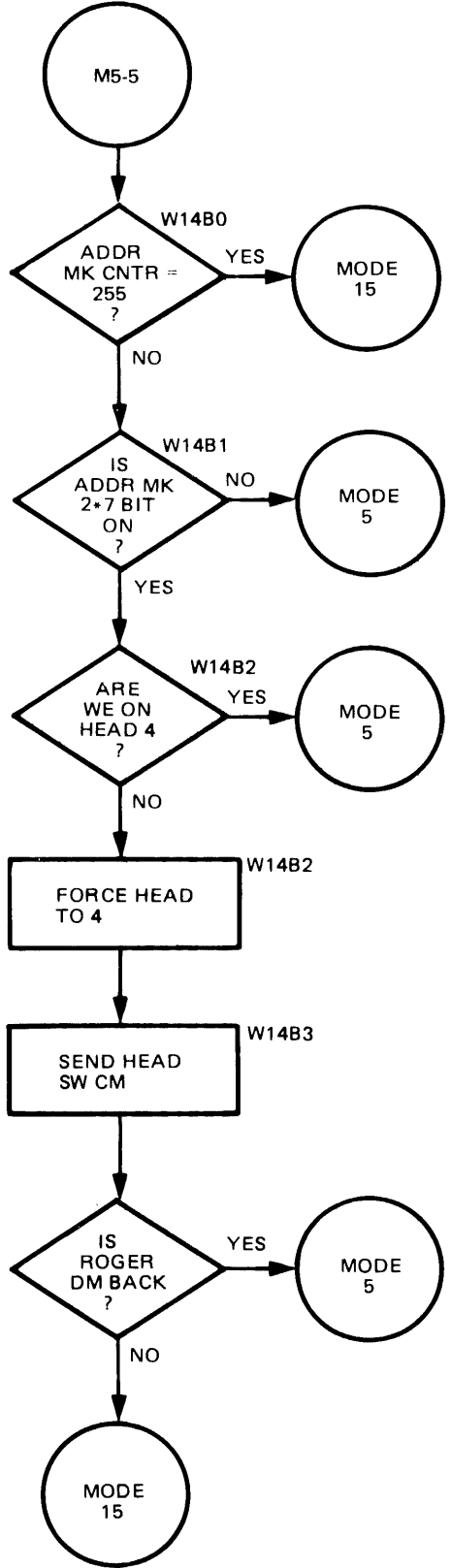
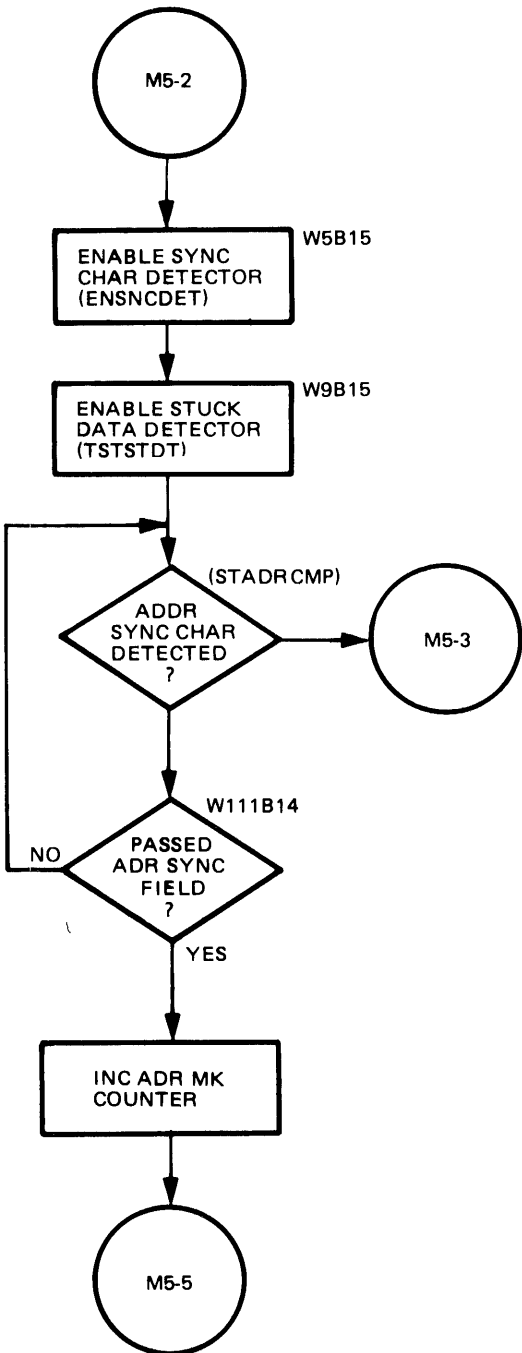
W11621 (Sheet 3 of 13)

Figure 3-5. Read and Write and Verify Operation (Sheet 3 of 13)



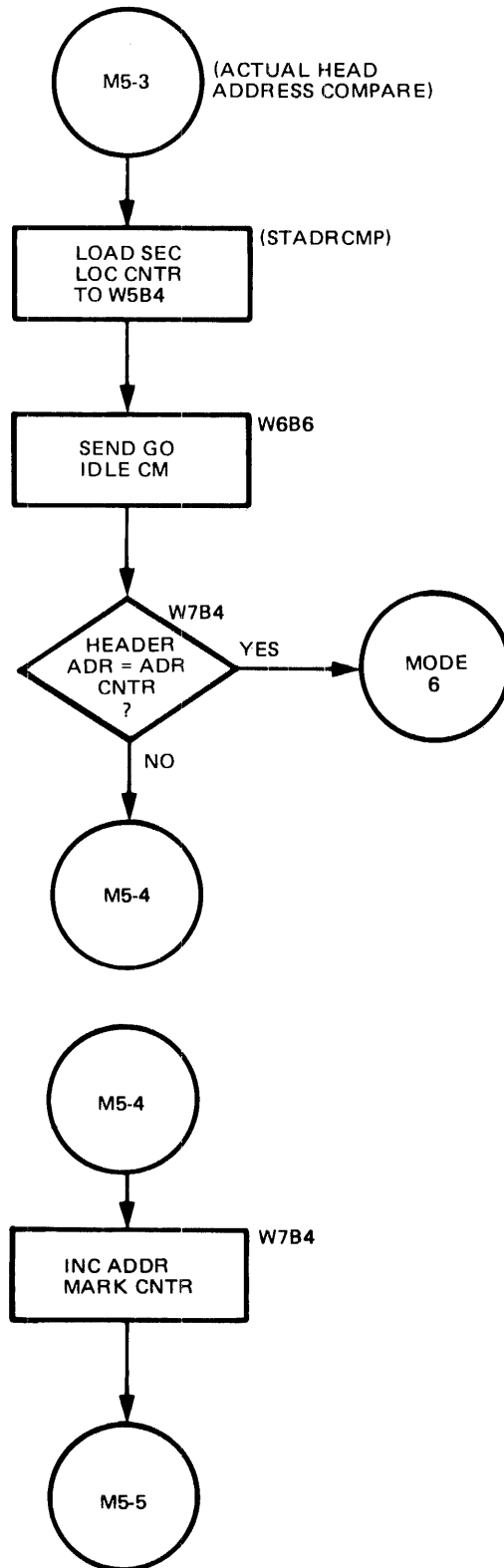
W11621 (Sheet 4 of 13) A

Figure 3-5. Read and Write and Verify Operation (Sheet 4 of 13)



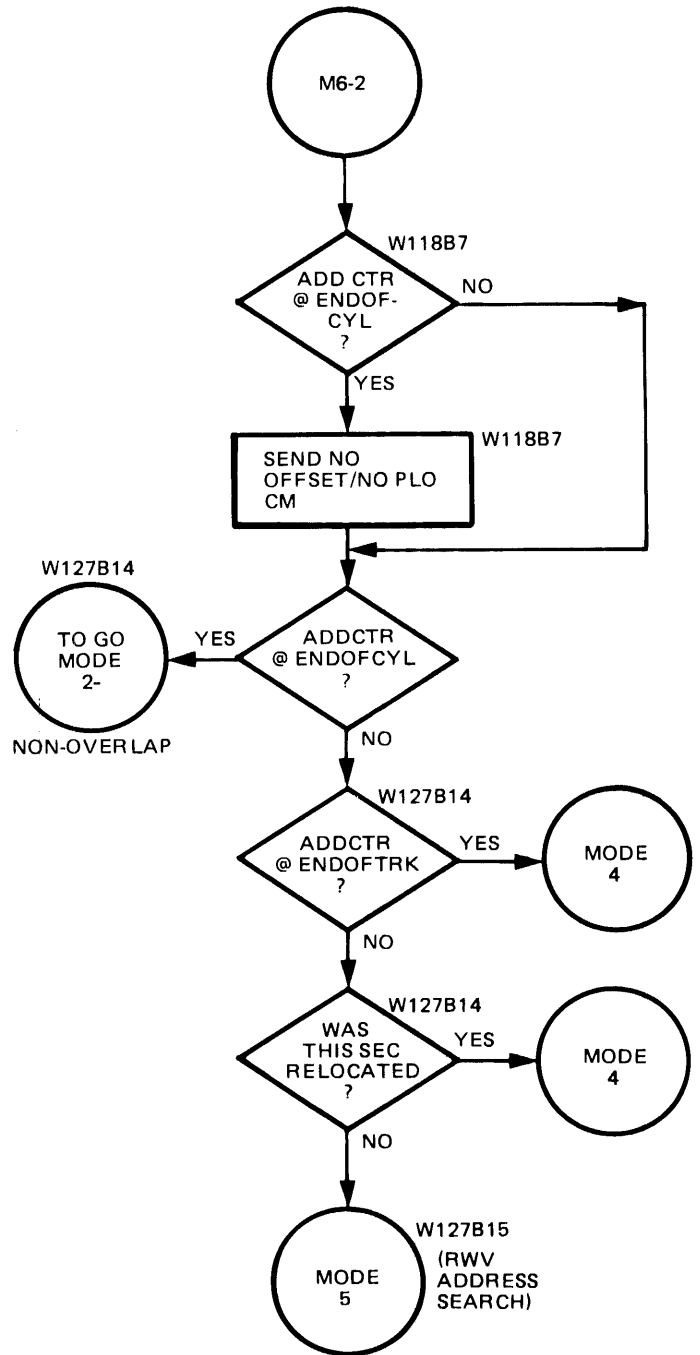
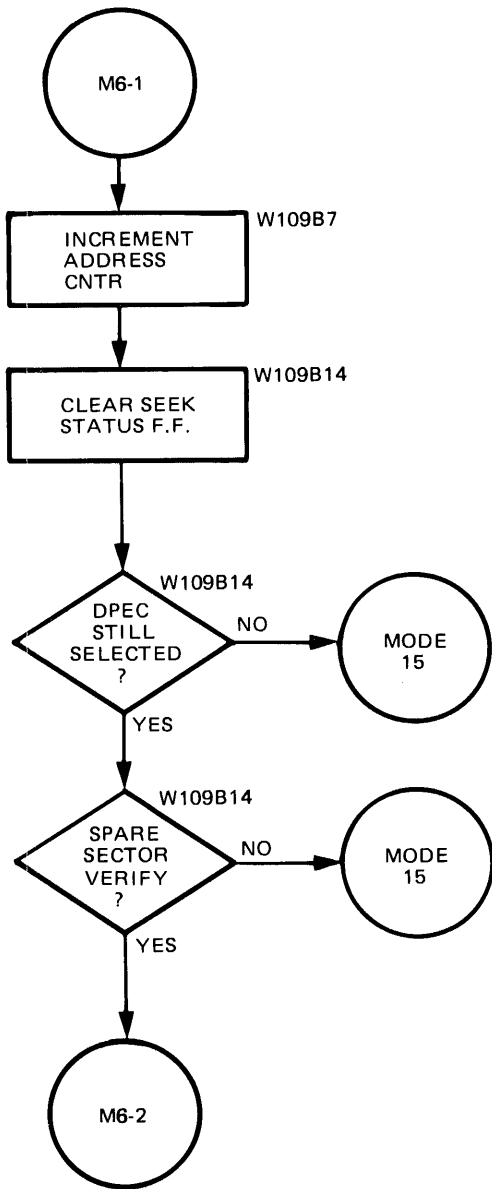
W11621 (Sheet 6 of 13)

Figure 3-5. Read and Write and Verify Operation (Sheet 6 of 13)



W11621 (Sheet 7 of 13)

Figure 3-5. Read and Write and Verify Operation (Sheet 7 of 13)



W11621 (Sheet 8 of 13)

Figure 3-5. Read and Write and Verify Operation (Sheet 8 of 13)

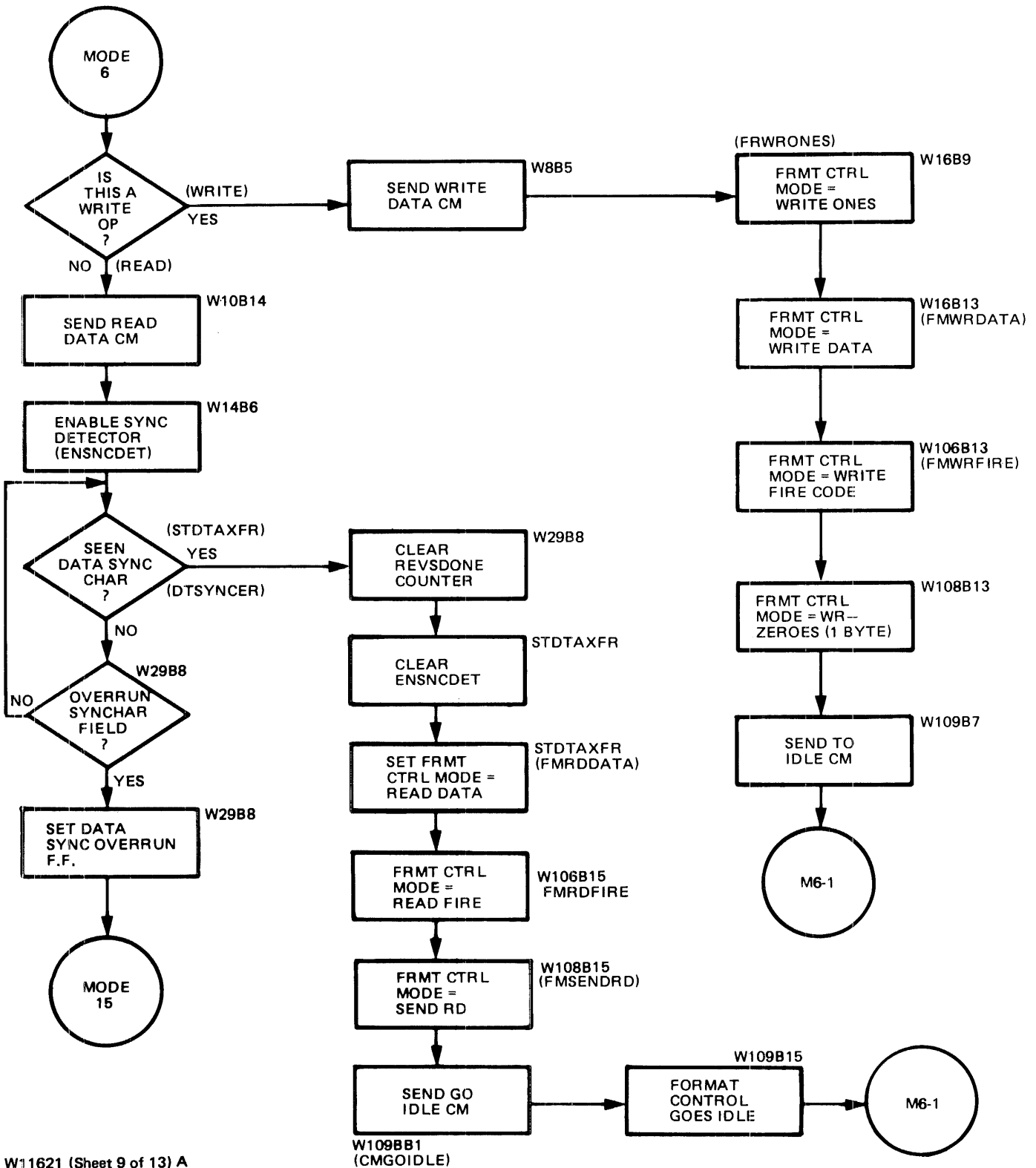
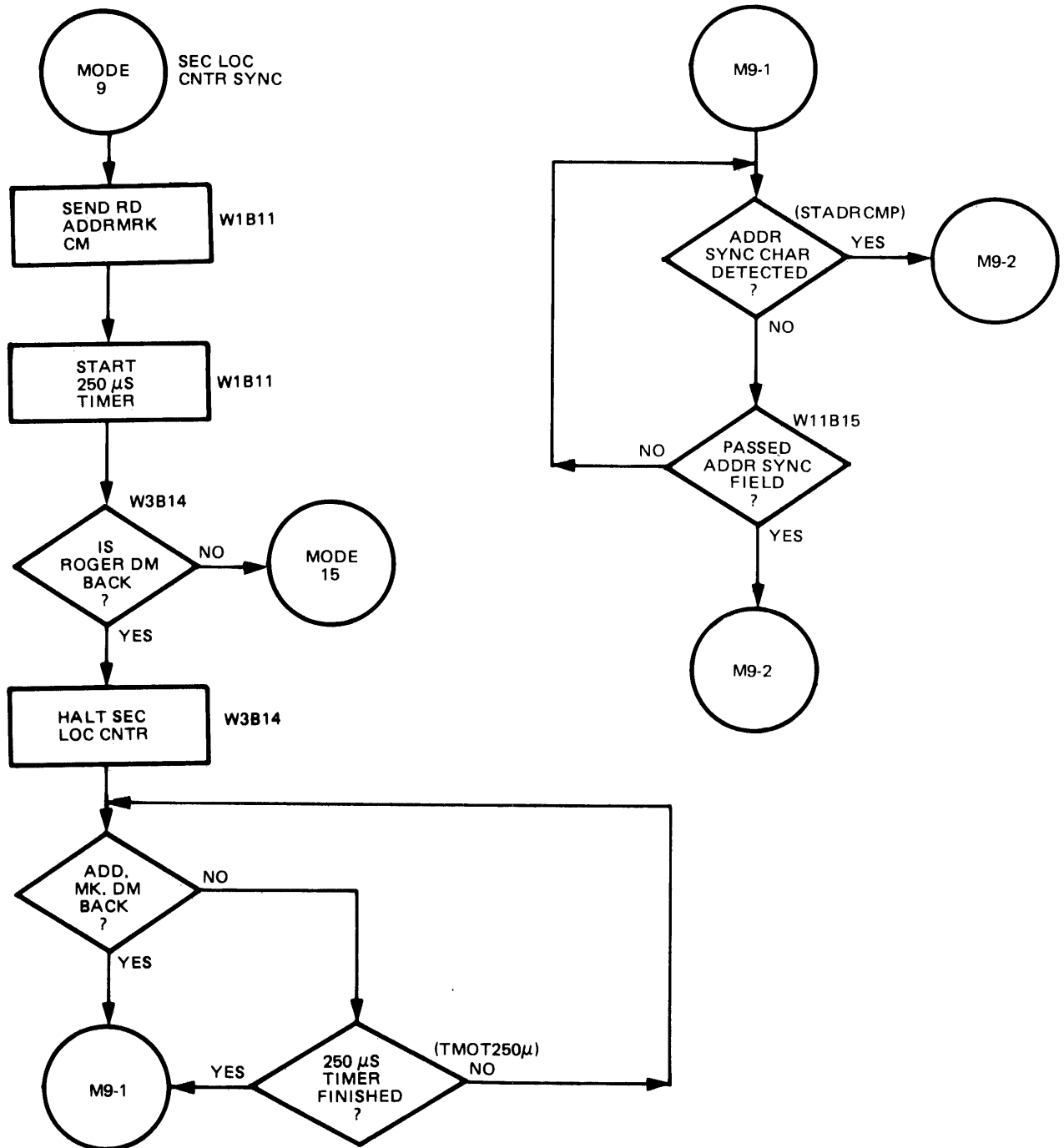
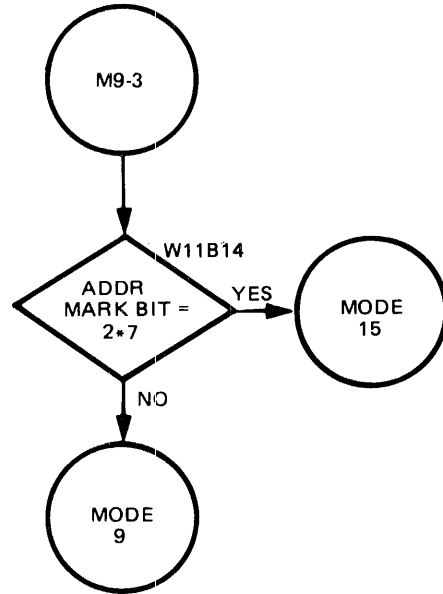
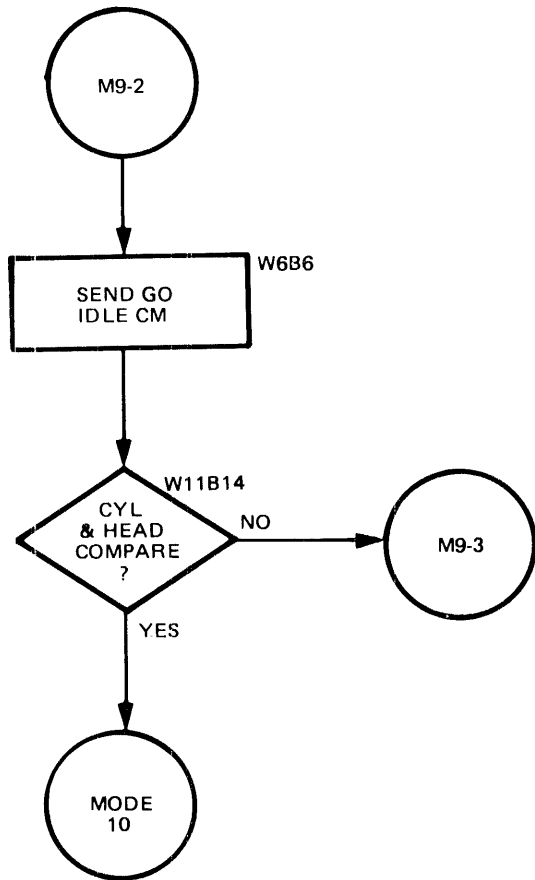


Figure 3-5. Read and Write and Verify Operation (Sheet 9 of 13)



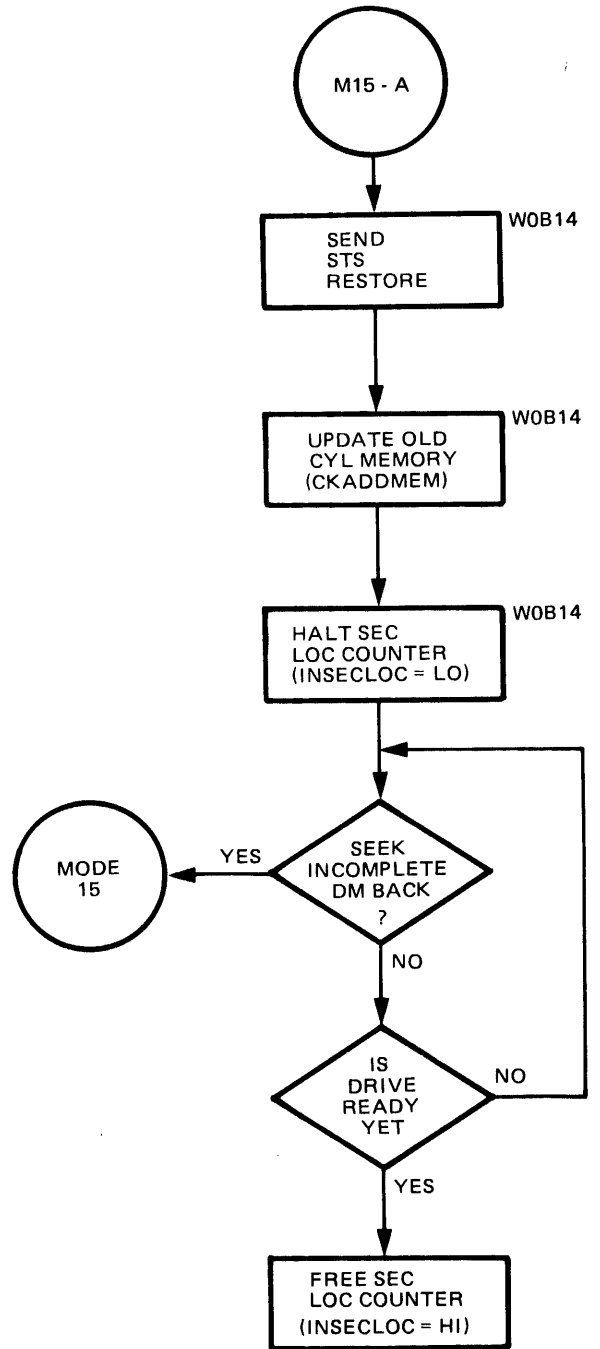
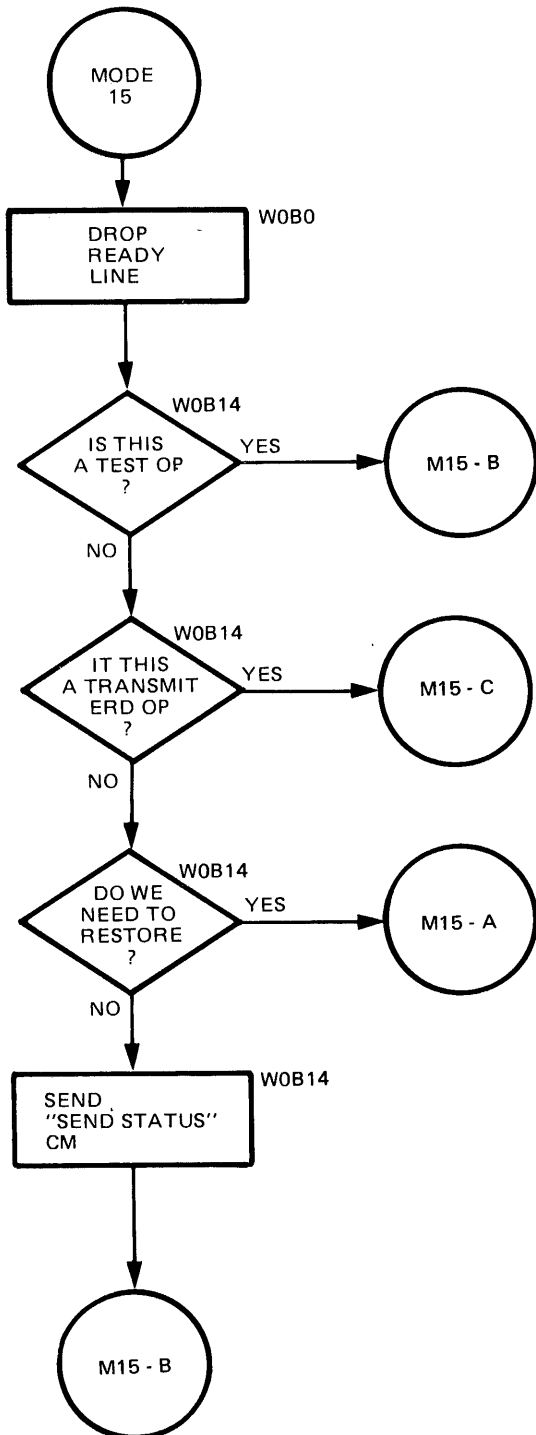
W11621 (Sheet 10 of 13)

Figure 3-5. Read and Write and Verify Operation (Sheet 10 of 13)



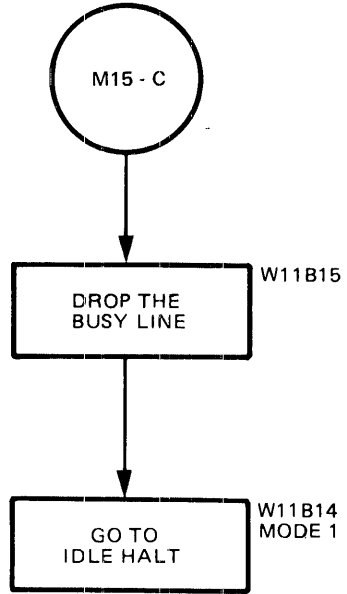
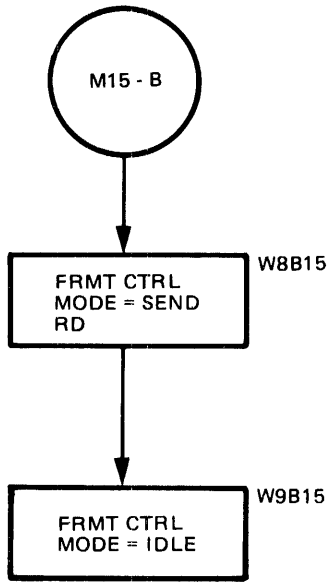
W11621 (Sheet 11 of 13)

Figure 3-5. Read and Write and Verify Operation (Sheet 11 of 13)



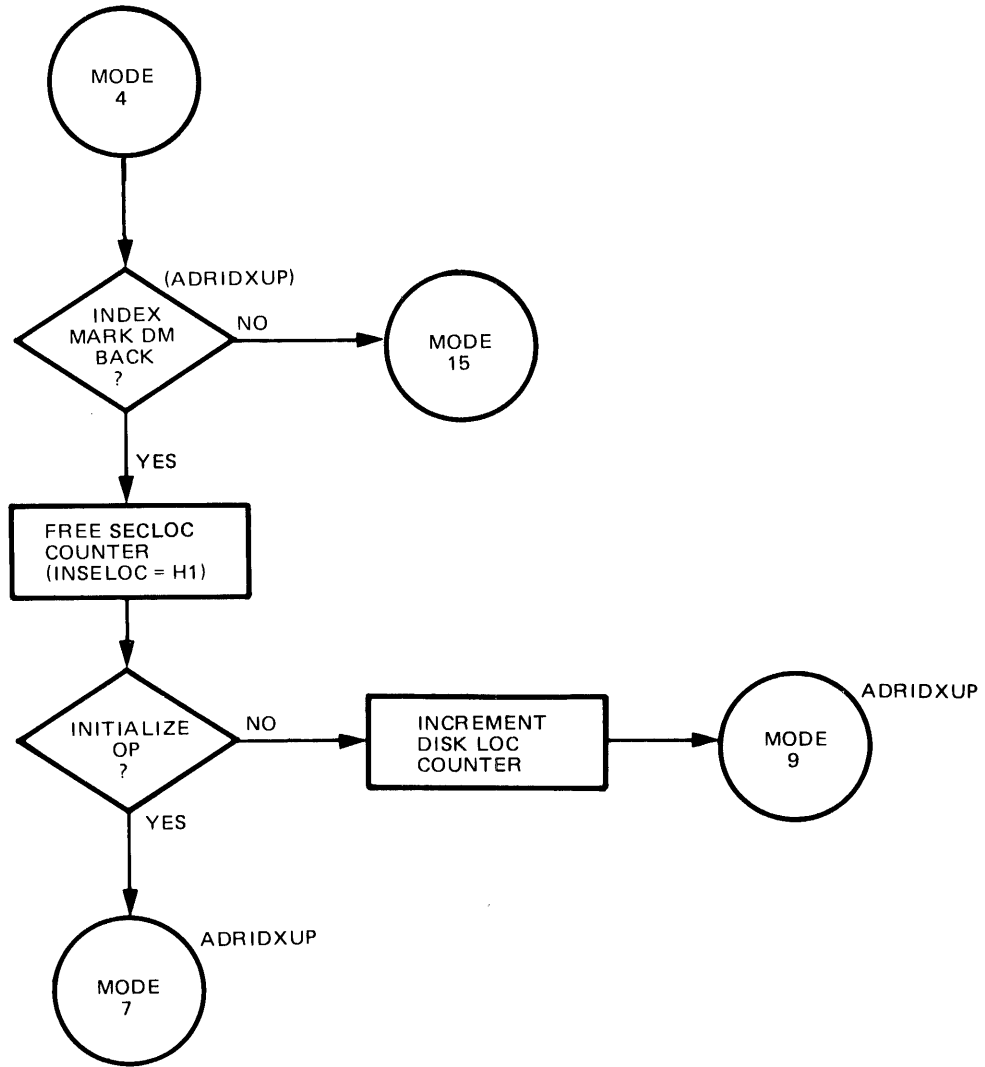
W11621 (Sheet 12 of 13) A

Figure 3-5. Read and Write and Verify Operation (Sheet 12 of 13)



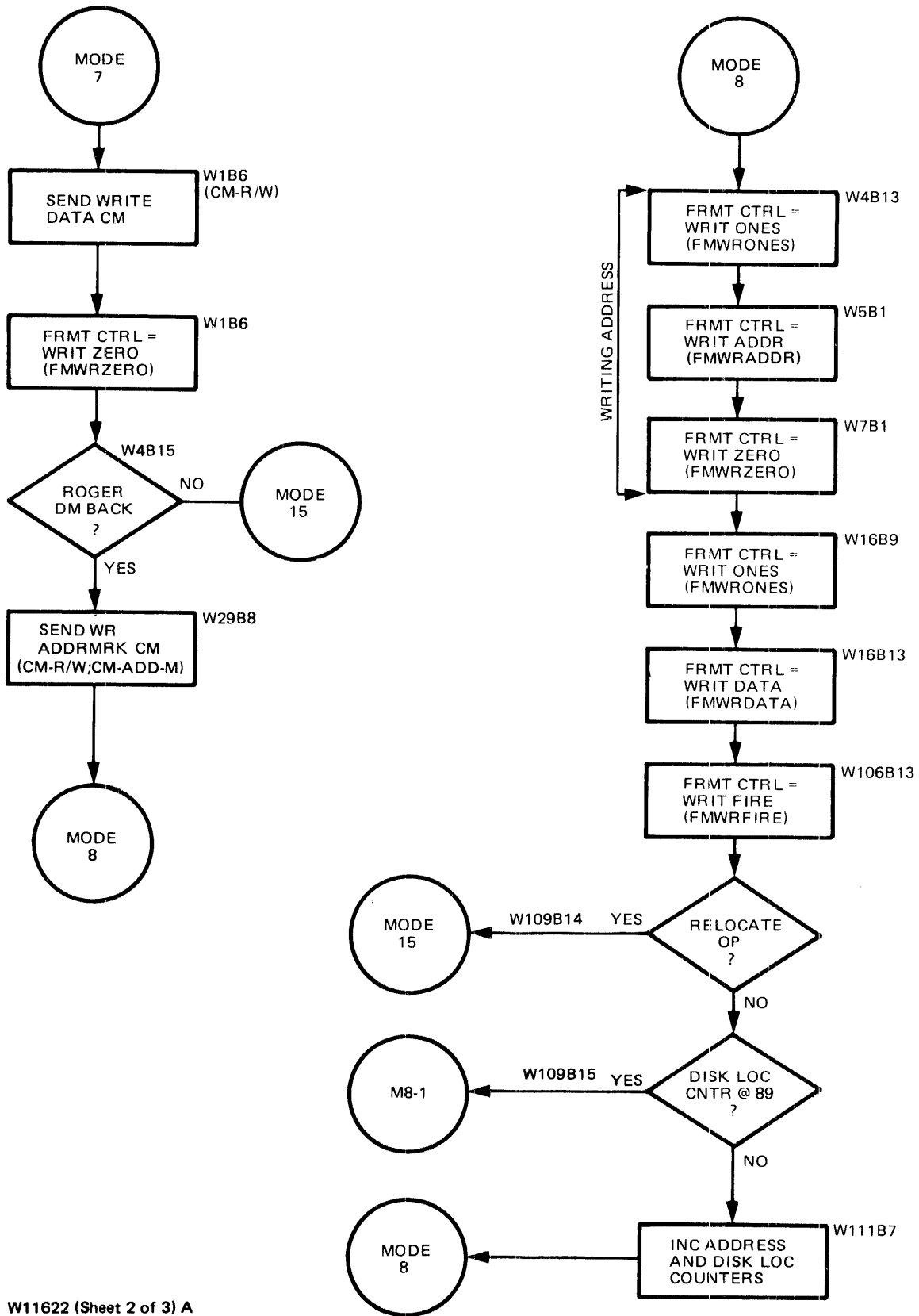
W11621 (Sheet 13 of 13) A

Figure 3-5. Read and Write and Verify Operation (Sheet 13 of 13)



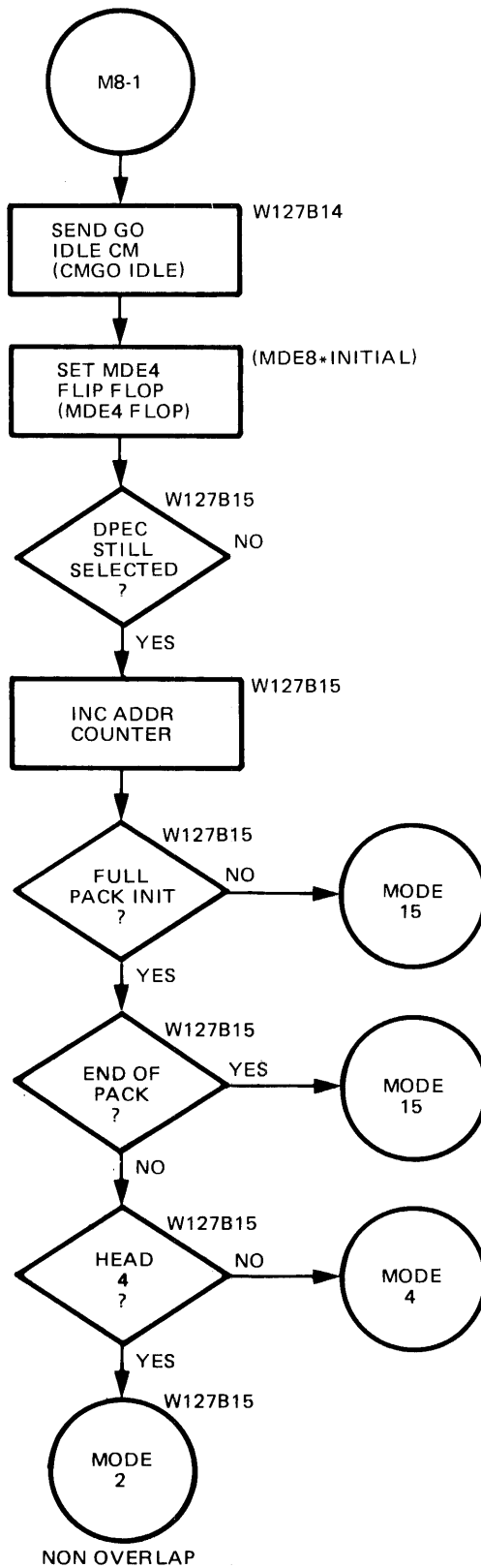
W11622 (Sheet 1 of 3) A

Figure 3-6. Initialize Operation (Sheet 1 of 3)



W11622 (Sheet 2 of 3) A

Figure 3-6. Initialize Operation (Sheet 2 of 3)



W11622 (Sheet 3 of 3)A

Figure 3-6. Initialize Operation (Sheet 3 of 3)

Table 3-2. Main Mode Jump Conditions

TO MODE	FINAL TERM	PAGE NO.	PARTIAL TERMS	PAGE NO.	SUB-PART TERMS	PAGE NO.	FROM MODE	UNDER THE FOLLOWING CONDITIONS:	SOURCE PIN	PAGE NO.
MDE0	PWR R SYNC	P42					PWR OFF	APPLICATION OF A.C. POWER - HOLDS 25 SEC.	0B07	P12
MDE1	GOTOMDE1	P46	L0A04	P46			MDE0	W9B15 } * PWR R SYNC/	0A04	P46
			L0A07	P46			MD15	W11B14 }	0A07	P46
			PBMN CLR	P42			ANY	ALL EXCEPT PWR R SYNC	0A06	P42
MDE2	GOTOMDE2	P46	L2C07	P46	LOB08	P46	MDE1	W14B3 * IMMDSSEEK	0B08	P46
					LOB05	P46	MDE1	W14B4 * NOEXCHNG/	0B05	P46
			L0R04	P46			MDE6	W127B14 * ENDOFTRK * ENDOFCYL	0B04	P46
			L1B08	P46			MDE8	W127B15 * ACHED2*2 * MDE8TERM/	1B08	P46
MDE3	GOTOMDE3	P46					MDE1	W14B6	2J04	P46
MDE4	GOTOMDE4	P46	L0D04	P46			MDE1	W14B2 * OLD=NEW	0D04	P46
			L0D07	P46			MDE2	W29B8 * SELECT	0D07	P46
			PTGT4FR6	P71			MDE6	W127B14 * FCD HD TO 4	2D04	P71
			L2W03	P46			MDE6	W127B14 * ENDOFTRK * ENDOFCYL/	2W03	P46
			L1C07	P46			MDE8	W127B15 * ACHED2*2/ * MDE8TERM/	1C07	P46
MDE5	GOTOMDE5	P47	GOTOSFR4	P73			MDE4	W11B14 * RWV * MDE4FLOP/	3P04	P73
			L0E07	P47			MDE5	W14B1 * ADMRK127/	0E07	P47
			L0F08	P47			MDE5	W14B2 * ACHED2*2	0F08	P47
			L0F05	P47			MDE5	W29B8 * ROGER DM	0F05	P47
			L1H08	P47			MDE6	W127B15	1H08	P47
MDE6	GOTOMDE6	P46					MDE5	W7B4 * ADDR EQL * ADSNCSTF * SELECT	1D08	P46
MDE7	GOTOMDE7	P47					MDE4	ADRIDXUP * INITIAL	3H04	P47
MDE8	GOTOMDE8	P47	L2K08	P47			MDE7	W30B6	2K08	P47
			L3E07	P47			MDE8	W111B7 * LOC 89/	3E07	P47
			L0G07	P47			MD10	W109B7 * FLAGWR TN * LOOPMD10	0G07	P47
MDE9	GOTOMDE9	P47	L3G07	P47			MDE4	ADRIDXUP * INITIAL/	3G07	P47
			P2INADMK	P47			MDE9	W11B14 * ADMRK127/ * (ADSNCSTF/ + CYLHDEQL/)	0H08	P47
			L1K04	P47			MD11	W104B7	1K04	P47
MD10	GOTOMD10	P48					MDE9	W11B1 * CYLHDEQL * ADSNCSTF	3C07	P48

Table 3-2. Main Mode Jump Conditions (Cont)

TO MODE	FINAL TERM	PAGE NO.	PARTIAL TERMS	PAGE NO.	SUB-PART TERMS	PAGE NO.	FROM MODE	UNDER THE FOLLOWING CONDITIONS:	SOURCE PIN	PAGE NO.
MD11	GOTOMD11	P48					MD10	W109B7 * FLAGWRTN/ * LOOPMD10/	3D08	P48
MD12	GOTOMD12	P48					MD10	W108B9 * DSKLOCEQ * RELOC/	0J07	P48
MD13	GOTOMD13	P46					MDE1	W2B0 * SEND ERD	1F08	P46
MD14	GOTOMD14	P48					MDE1	W13B15 * TESTOP	1J07	P48
MD15	GOTOMD15	P49						NOTE: THE FINAL TERM IS BLOCKED WITH (MDE0 + MD15).	3U08	P49
			L3S08	P49	L0S08	P49	MDE1	W2B14 * XMPER + TD	0S08	P49
					L1S08	P49	MDE1	W5B1 * (DR READY/ + DRONLINE/)	1S08	P49
					L0R07	P49	MDE1	W14B5 * SKSTATUS	0R07	P49
			PT8GMD15	P48	L1K08	P48	MDE2	W9B13 * NRMLUNST/	1K08	P48
					MD2W30B6	P47	MDE2	W30B6	4E07	P47
			PT4GMD15	P48			MDE3	W9B15	3R04	P48
			PT5GMD15	P72	G3N07	P72	MDE4+5	ENSELTRM * SELECT/	3N07	P72
					PT59TO15	P73	MDE5+9	(W3B14+W29B8) * ROGER DM/	2H08	P73
					PTM6TO15	P73	MDE6	W29B8 * WRITE/ * DTSNCSTF/	0S08	P73
					G3P08	P72	MDE6	W109B14 * ENDOFPAK/	3P08	P72
					PTM9TO15	P73	MDE9	W11B14 * ADMRK127	2D08	P73
					G2G04	P72	ANY	LONG DMS * W14B0 FF	2G04	P72
					NOROG DM	P72	ANY	DOWN-EDGE DETECT OF 65 MS TIMER TRIGGERED BY CM START CLEARED BY (ROGER DM + IDLE)	0K05	P72
					TIME OUT	P73	ANY	TMOT25MS	0S06	P37
			PT7GMD15	P71	L0M04	P71	MDE5	W14B0 * REVSDONE	0M04	P71
					L0M08	P71	MDE6	W109B14 * (SELECT/ + SPRVRIFY)	0M08	P71
			PT2GMD15	P48			MDE8	W109B14 * RELOC	4H08	P48
			PT1GMD15	P48			MDE8	W127B15 * LOC 89 * MDE8TERM	0K08	P48
			PT3GMD15	P48			MDE9	W13B15	1U04	P48
			L1R04	P49			MD12	W109B15	1R04	P49
			L1S05	P49			MD13	W11B14	1S05	P49
			PTCASKST	P49			MD14	W0B14	1R07	P49
			L1V07	P49			MD15	W0B15 * SEEKINCL * DM RCVD (SUPERFLUOUS TERM)	1V07	P49
			PT6GMD15	P69			ANY	SYNCHRONIZED DPEC EXC	4U08	P69

SECTION 4

MAINTENANCE

INTRODUCTION

This section explains the use of the maintenance control panel, and provides an overall maintenance guide to the 206 DPEC.

USE OF MAINTENANCE CONTROL PANEL

The maintenance control panel is used in the local mode. It can be used to perform maintenance on the disk pack drive as well as on the DPEC (see figure 4-1).

Switch Functions (Local Mode Only)

a. LOAD

Allows the contents of the 16 (vertical) data bits to be loaded into the maintenance memory location being indicated by the four (horizontal) memory address lamps. Pressing this button will load the memory and increment the memory location by 1.

b. CLEAR

1. DISP ENBL Switch ON. Clears the contents of the 16 data bits being displayed and loads zeros into that memory location. It does not affect the contents of the other 15 memory words.
2. DISP ENBL Switch Resets the maintenance memory to location 0, clears the 16 data bits, but does not affect the contents of the maintenance memory.

c. START

Initiates the instruction at one of the two maintenance memory locations.

d. STEP MEM (Step memory)

1. DISP ENBL OFF. No effect.
2. DISP ENBL ON. When the STEP MEM button is pressed (while the DPEC is in the idle state), the maintenance memory word (horizontal lamps) will be incremented, and the next memory location will be displayed in the 16 data bit registers.

e. DISP ENBL

Affects the operation of the CLEAR and

STEP MEM buttons (see previous descriptions).

f. HALT FERR

When in the ON position, allows the DPEC to halt when a Fire code error is detected.

g. SGL SECT (Single Sector)

1. LOOP OP OFF. Allows the execution of a single instruction on a single sector and terminates.
2. LOOP OP ON. Allows the continuous execution of one operation code on a single sector.

h. SLIP

Simulates the slip operation generated by the processor to interrupt the transfer of data from the DPEC to the DPC.

i. ALT SEEK

1. ALT SEEK ON, LOOP OP OFF, SGL SECT OFF

The Field Engineer can selectively initiate one maintenance memory instruction and then the other by using the START and STOP buttons. (The CLEAR button must not be used in this sequence.)

2. ALT SEEK ON, LOOP OP ON, SGL SECT ON

This mode is primarily used to alternate between two different cylinders to check servo operation. A different address is loaded at each maintenance memory instruction.

3. ALT SEEK ON, LOOP OP ON, SGL SECT OFF

This mode can be used to perform serial instructions without operator intervention. An example is to load an initialize operation code in one maintenance memory location and a read or verify operation code in the other. Pressing the START button will execute one instruction. Upon termination, the other operation code will be executed until it terminates.



W11623

Figure 4-1. Maintenance Control Panel

CAUTION

If an error occurs during a read or verify, and the HALT ERR switch is ON, the operation will terminate and the other operation code will be performed.

j. LOOP HEAD/LOOP SECT

Allows the DPEC to loop on a particular head or sector.

k. NO OVRLP (No Overlap)

Disables the overlapping seek function in the local mode.

l. NO ADD LOAD (No Address Load)

Prevents the address register from being reset to 0 when a maintenance memory instruction is re-initiated.

For example, a pack is being read in a local mode and a Fire code error is detected at cylinder 256, head 1, sector 10. Since the HALT ERR switch was on, the operation terminates. With the NO ADD LOAD switch ON, the operation can be continued from this point. If the NO ADD LOAD switch is OFF, restarting the operation will reset the address register to 0.

m. LOOP OP

Used primarily with the SGL SECT or ALT SEEK switches to continuously execute an operation.

Indicator Functions

Sixteen vertical LEDs (light-emitting diodes) are used to display the contents of one word of maintenance memory. The four horizontal memory address counter (MEM ADR CNTR) LEDs are used to identify which of the 16 words are being displayed in the vertical LEDs.

Maintenance Memory Loading

Operation codes are entered into the DPEC maintenance memory using the 16 vertical pushbuttons and the LOAD pushbutton. The memory contains 16 words of 16 bits each. Refer to section I of this manual for the operation codes, tables 1-2 and 1-3.

The 16 maintenance memory words will be used in the following manner:

Table 4-1. Maintenance Memory Loading Descriptions

Memory Address Counter	Mode	Description
0	All	Word 1 of instruction 1. OPERATION CODE, "N" variants, unit designations and the five least significant bits of the file address.
1	All	Word 2 of instruction 1. Fourteen most significant bits of the file address and two spare bits.
2	All	Word 3 of instruction 1. Data information used during initialize, write and relocate operations.
3	Read Extended Status	ERD word 1 from either instruction. Refer to table 1-5 for the contents of the register.
	Alternate Seek/Loop Op	First 16 bits of Fire code information. The most significant of the 32 bits will be displayed in the bottom LED.
4	Read Extended Status	ERD word 2 from either instruction. Refer to table 1-5 for the contents of the register.
	Alternate Seek/Loop Op	Second 16 bits of Fire code information. The least significant of the 32 bits will be displayed in the top LED.
5	Read Extended Status	ERD word 3 from either instruction. Refer to table 1-5 for the contents of the register.
6	Read Extended Status	ERD word 4 from either instruction. Refer to table 1-5 for the contents of the register.
7	All	Not used.
8	All	Word 1 of instruction 2.
9	All	Word 2 of instruction 2.
10	All	Word 3 of instruction 2.
11	Alternate Seek/Loop Op	First 16 bits of Fire code information from the second instruction. The most significant of the 32 bits of Fire code will be displayed in the bottom LED.
12	Alternate Seek/Loop Op	Last 16 bits of Fire code information from the second instruction. The least significant of the 32 bits of Fire code will be displayed in the top LED.
13	All	Not used.
14	All	Not used.
15	All	Not used.

Memory Address Counter Indicators

The memory address counter indicators on the maintenance control panel are the four horizontal lamps in the upper left of the panel. These lamps can be used to determine the state of the DPEC while in a local mode.

Memory Address 2 (2*1)	Normal running state while executing an instruction located at memory address 0, 1, and 2.
Memory Address 3, 5, 7 or 13	Halt conditions.
Memory Address 4 (2*2)	Executing the instruction at the beginning of maintenance memory while using the ALT SEEK mode.
Memory Address 10 (2*1 and 2*3)	Executing the instruction at location 8, 9, and 10 maintenance memory instruction while in the ALT SEEK mode.
Memory Address 12 (2*2 and 2*3)	Executing instruction number 2 with ALT SEEK off.

For example, if the DPEC is in an operating state, and the memory address lamp 2 is illuminated, the DPEC is in a normal running state and executing an instruction at the first operation code location.

P CARD PLUG-ON INDICATOR

Figure 4-2 illustrates the P-card plug-on indicator. This indicator will display the cylinder, head, sector, and unit being addressed (or addressed on the last operation).

The address information that is being displayed is the output of the address counter.

TROUBLESHOOTING AIDS

Several aids are available to assist the field engineer in troubleshooting DPEC problems. Depending on the particular problem and the individual field engineer's preference in troubleshooting, various methods can be used. Some of the aids available to the field engineer are listed in the following subsections.

Local Maintenance Aids

The switch control package and the indicator display package have been described earlier in this section. These aids can be used to determine whether a problem exists only in a remote mode or in both local and remote modes. The aids can also be used to perform spindle alignments when an exerciser is not available.

The following procedure can be used to seek to a particular address by loading the desired address into the first and second data words of either instruction word. Refer to table 1-4. As an example, a seek to cylinder 496, head 4 on the disk pack drive: Using the "Disk Pack Address Scheme in Hex" table (that is available from the Disk Pack Test Routine tape, PACK option), determine the hex address that corresponds to the desired cylinder and head. In this example, cylinder 496, head 4 is 035F98. This hex address is entered in LSD to MSD order.

The first word will contain the five least significant bits of the file address. The information is loaded from right to left. Using the file address 035F98, the

C Y L I N D E R	512	<input type="radio"/>
	256	<input type="radio"/>
	128	<input type="radio"/>
	64	<input type="radio"/>
	32	<input type="radio"/>
	16	<input type="radio"/>
	8	<input type="radio"/>
	4	<input type="radio"/>
	2	<input type="radio"/>
	1	<input type="radio"/>
H E A D	4	<input type="radio"/>
	2	<input type="radio"/>
	1	<input type="radio"/>
S E C T O R	64	<input type="radio"/>
	32	<input type="radio"/>
	16	<input type="radio"/>
	8	<input type="radio"/>
	4	<input type="radio"/>
	2	<input type="radio"/>
U N I T	4	<input type="radio"/>
	2	<input type="radio"/>
	1	<input type="radio"/>

W11624

Figure 4-2. P-Card Plug-on Indicator

LSD digit, 8, would be loaded into position 2*3. (2*0, 2*1 and 2*2 are blank.) See figure 4-1. The one bit from the 9 digit will be loaded into the 2*4 position.

The second word will contain the remaining 14 bits of the file address. The eight bit from the 9 digit will be loaded into the 2*7 location.

Block Diagrams

The block diagrams can be used to determine the relation between one basic DPEC circuit and another within the DPEC, with definable results. In many cases, the cause of a solid malfunction can be isolated to a specific circuit by studying the block diagrams, either the overall diagram or the individual circuit diagrams.

Flow Charts

Two flow charts are included; one is a simplified flow chart, the other a detailed flow chart. The detailed flow chart should be studied to refresh a field engineer's memory as to what functions take place during a particular mode and the details of that mode. A good starting point would be page 1 of the detailed flow chart. From this page, the field engineer can determine which modes will be accessed, and their sequence during a given operation.

B 1700 Disk Pack Subsystem Test Routine

Revision AG (P/N CT 2211 0175) of the Disk Pack Subsystem test routine can be helpful in determining the confidence of the complete disk pack subsystem. Refer to the documentation that is included with the B 1700 Disk Pack Control for operating instructions.

Extended Result Descriptor

Local

When the try diagnostics bit is set during a local operation, the contents of the ERD registers can be read in the following manner.

The Read Maintenance OP code is used with the N2 variant set to load the contents of the ERD registers into the DPEC Maintenance Memory. Once this has been done, the maintenance memory words will contain the following information:

- Word 3: First ERD word, first 16 bits
- Word 4: Second ERD word, second 16 bits
- Word 5: Third ERD word, third 16 bits
- Word 6: Fourth ERD word, fourth 16 bits

Refer to table 1-6 for the contents and sequence of each word.

Remote

Refer to the instructions included with Section 9, part 3 of the disk pack test routine (part number CT 2211 0175) included with the DPC for using the ERD option under test conditions.

Using the E Log

The following discussion can be used as a guide to using the ERD information from the E log to troubleshoot intermittent or potential problem areas.

Figure 4-3 is a copy of a typical E log using MCP II Mark VI.0.0.

Refer to the underlined area in the figure. This is the ERD information in a 16-digit format. The information can be decoded in the following manner.

Each group of four digits is the contents of one word of ERD information.

ERD Word	Contents
1	17C6
2	3C30
3	2000
4	0000 (No data)

This information must be converted to its binary equivalent:

17C6 =	(1) 0001	(7) 0111	(C) 1100	(6) 0110
3C30 =	(3) 0011	(C) 1100	(3) 0011	(0) 0000
2000 =	(2) 0010	(0) 0000	(0) 0000	(0) 0000

The binary equivalent must contain 64 bits of ERD information. The bits are numbered from 1 to 64, from left to right.

In the above example, the ERD bits that are present are: 4, 6, 7, 8, 9, 10, 14, 15, 19, 20, 21, 22, 27, 28 and 35.

Cylinder:	64, 16, 8, 4, 2 and 1 = 95
Head:	2 and 1 = 3
Sector:	8, 4, 2 and 1 = 15
Unit:	2 and 1 = 3, UNIT D
Other information:	Missing Sector Pulse

Table 4-2. 206 Extended Result Descriptor (Remote)

Bit	Description
1	Cylinder 512
2	Cylinder 256
3	Cylinder 128
4	Cylinder 64
5	Cylinder 32
6	Cylinder 16
7	Cylinder 8
8	Cylinder 4
9	Cylinder 2
10	Cylinder 1
11	Spare
12	Spare
13	Head 4
14	Head 2
15	Head 1
16	Sector 64
17	Sector 32
18	Sector 16
19	Sector 8
20	Sector 4
21	Sector 2
22	Sector 1
23	OP code 1
24	OP code 2

Table 4-2. 206 Extended Result Descriptor (Remote) (Cont)

Bit	Description
25	OP code 3
26	Unit 2*2
27	Unit 2*1
28	Unit 2*0
29	N0 variant bit
30	N1 variant bit
31	N2 variant bit
32	N3 variant bit
33	DPEC blower failure
34	Missing R/W clock
35	Missing address mark
36	Read data not received
37	No index mark
38	CM error*
39	Model 206 drive
40	Spare
41	Spare
42	Spare
43	Maintenance mode
44	Write data missing
45	Write protect and write enable
46	CM or offline when seeking
47	Illegal head
48	Illegal cylinder
49	Spindle address error
50	Offset during write enable
51	Offset during seek
52	Seek incomplete
53	Off track and write enable
54	Carriage hit end stop
55	Spare
56	Write current, no write gate
57	No write current changes
58	Head select fault
59	DC power failure
60	Temperature warning
61	Temperature critical
62	Rpm less than 3420
63	Bad DM response
64	Spare

* When a CM error is detected in a Remote mode, ERD bits 39 through 62 will contain the last CM message that was sent to the drive. The information will be displayed in the following manner.

Bit	Description
39	Mark bit
40	Write bit

Table 4-2. 206 Extended Result Descriptor (Remote) (Cont)

Bit	Description
41	Read bit
42	Address mark
43	Parity even (1-5)
44	Continue bit
45	Address or Control message
46	Head or cylinder, or Offset on
47	Address information (LSB) or Offset in
48	Address information (LSB) or PLO early
49	Address information (LSB) or PLO late
50	Address information (LSB) or Power up
51	Address information (LSB) or Power down
52	Address information (LSB) or Re-zero
53	Address information (LSB) or Send status
54	Address information (LSB) or Check index
55	Address information (LSB) or Spare
56	Address information (LSB) or Spare
57	Address information (LSB) or Reset maintenance mode
58	Address information (MSB) or Set maintenance mode
59	Write enable
60	Spare
61	Parity even (1-23)
62	End bit

LOGIC LEVELS

True

A signal level is considered a logical TRUE (ONE) if it is in the range of +2.4 to +5.0 volts. A signal level is measured at the receiving end of its line with a termination resistance of 100 ohms to ground.

False

A signal level is considered a logical FALSE (ZERO) if it is in the range of 0.0 to +0.4 volt. A signal level is measured at the receiving end of its line, with a termination resistance of 100 ohms to ground.

SECTION 5

SUBASSEMBLY MAINTENANCE ADJUSTMENTS

INTRODUCTION

This section contains the procedures needed to make the 206 DPEC adjustments.

10 MEGAHERTZ CLOCK ADJUSTMENT

The 10-megahertz clock frequency adjustment potentiometer is located on the bottom of the "N" card.

The 10 megahertz clock can be monitored at card cage backplane location ENCB. The time between clock pulse leading edges should be 0.1 microsecond. If it is not at this value, the potentiometer on the "N" card must be adjusted.

POWER SUPPLY ADJUSTMENTS

Refer to the installation section for instructions on removing DPEC panels.

The DPEC power supply chassis contains an OEM power supply subassembly.

This subassembly contains three potentiometers. To gain access to these potentiometers, the DPEC power supply cover must be removed. Two of the potentiometers (OL ADJ and VOLT ADJ) can be reached from the top of the power supply subassembly. The third potentiometer can be reached from the side of the subassembly.

NOTE

Only the VOLT ADJ potentiometer requires adjustment in the field. The other two potentiometers were adjusted at the factory and should not require further adjustment.

Overload Protection

The OL ADJ (Overload Current Adjustment) potentiometer is adjusted at the factory to limit the power supply maximum current to between 20 and 22 amperes at +5.0 volts dc.

Overvoltage Protection

The potentiometer on the side of the power supply subassembly is not labeled. It is the overvoltage adjustment potentiometer. It was adjusted at the factory to prevent the output voltage of the power supply

from exceeding approximately 6.0 volts.

+5.0 Volts Supply

Using a digital voltmeter, monitor card cage backplane pin CSAQ. The voltage at this location should be +5.0 volts dc with the DPEC in an operational mode. If this voltage is not within ± 0.1 volts, remove the power supply chassis cover and adjust the VOLT ADJ potentiometer to obtain +5.0 volts ± 0.1 volt at CSAQ.

High/Low Input Voltage Adjustment

CAUTION

Remove power from the DPEC before attempting to move any power supply terminal connections.

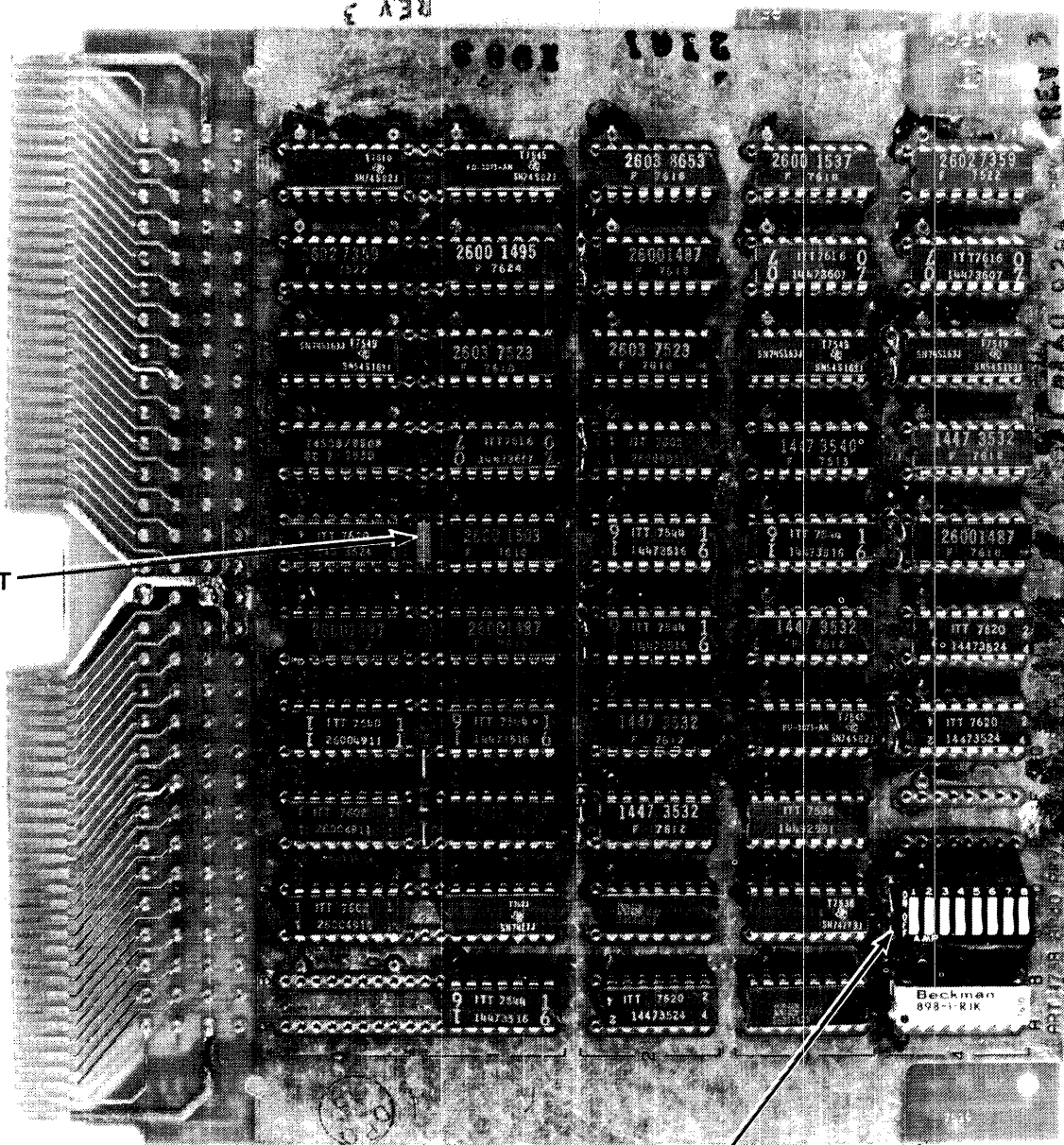
The following procedure must be used to modify the input power circuitry of the DPEC. The subassembly is wired at the factory for an input voltage of 208 to 225 volts ac. Measure the input voltage between phases 1 and 2 at TB1 in the DPEC power supply. If the voltage is greater than 225 volts, the following modification is required.

- a. Remove the DPEC power supply cover.
- b. Locate the OEM power supply subassembly terminal strip.
- c. Move the lead from the AC LOW terminal to the AC HIGH terminal.
- d. Replace the power supply cover.

DRIVE PRESENT AND FORMAT OPTION ADJUSTMENTS

The H card contains a switch package integrated circuit at location CD4. See figures 5-1 and 5-2. This integrated circuit is used to notify the system of the number of spindles that will be used. The system will then allocate memory for these spindles. For proper system operation, the switches must be set to reflect only the number of spindles on the disk pack subsystem.

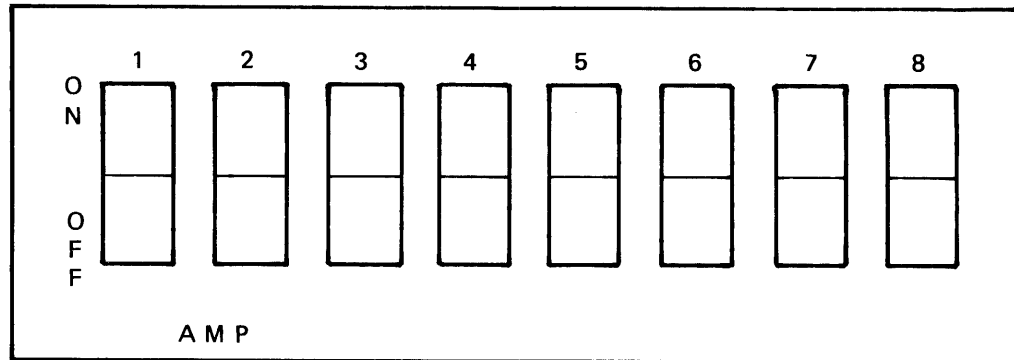
AUGHT



DRIVE PRESENT
I.C. SWITCH

W11626

Figure 5-1. H-Card



W11627

Figure 5-2. Drive Present Integrated Circuit Switch Assembly

The switches are numbered from one to eight, and the OFF and ON positions are labeled. To make the adjustment, use the following procedure:

- a. Power off the DPEC.
- b. Remove the H card.
- c. Transfer the appropriate switches to the ON position to reflect the number of spindles that will be in the system.
- d. Ensure that there is a jumper bar (AUGHT) between locations 1LOO and 1MOO. The jumper will be physically located between chip LM0 and LM1. (This jumper is necessary to enable the gated unit [GUNIT 2* n] logic. See schematic page 67 for the H card. There should be NO jumper from 1N00 to 1P00.) See figure 5-1.
- e. Replace the H card.

APPENDIX A. GLOSSARY OF TERMS

Any signal name followed by a slash (/) indicates the signal is low active.

Signal Name	Backplane Pin No.	Schematic Page No.	Description	Signal Name	Backplane Pin No.	Schematic Page No.	Description
ACCYL2*0	CPCF	9	Address counter cylinder output	ADSNCSTF	FMCL	38	Address sync start flip-flop
ACCYL2*1	CPCG	9	Address counter cylinder output	ALTGOWRZ/	EHAK	66	Alternate go write zeros
ACCYL2*2	CPCH	9	Address counter cylinder output	BADDMRSP	FGAJ	73	Bad DM response
ACCYL2*3	CPCJ	9	Address counter cylinder output	BIT-11	BMAJ	35	Bit 11
ACCYL2*4	CPCL	9	Address counter cylinder output	BIT-14/	BMAG	33	Bit 14
ACCYL2*5	CPCM	9	Address counter cylinder output	BUFDATA	FSAB	19	Buffered data
ACCYL2*6	CPCN	9	Address counter cylinder output	BUFDCM/	FSCK	20	Buffered CM
ACCYL2*7	CPCP	9	Address counter cylinder output	BUSY	EKCC	56	Busy
ACCYL2*8	EPCE	9	Address counter cylinder output	BUSY/	EKCL	56	Busy
ACCYL2*9	EPCF	9	Address counter cylinder output	CK-DPC	EHAB	66	Clock to the disk pack control (DPC)
ACHED2*0	CPCC	9	Address counter head output	CK-DPC/	EHAC	66	Clock to the disk pack control (DPC)
ACHED2*1	CPCD	9	Address counter head output	CKADDMEM/	FJAN	62	Clock address memory
ACHED2*2	CPCE	9	Address counter head output	CKINTWRD/	EKAQ	57	Clock initiate word
ACSEC2*0	BPCB	9	Address counter sector output	CKSKSTAT/	EKAL	55	Clock seek status flip-flop
ACSEC2*1	BPCC	9	Address counter sector output	CKWORD1/	CPAM	7	Clock word 1
ACSEC2*2	BPCD	9	Address counter sector output	CK10DRV	CSCK	19	10 MHz clock from the drive
ACSEC2*3	BPCE	9	Address counter sector output	CK10MHz	ENCB	32	DPEC 10 MHz clock
ACSEC2*4	BPCF	9	Address counter sector output	CK10MHz/	ENAB	32	DPEC 10 MHz clock
ACSEC2*5	BPCG	9	Address counter sector output	CK10MHz1	ENAN	32	DPEC 10 MHz clock one
ACSEC2*6	BPCH	9	Address counter sector output	CK10MHz2	FNAP	32	DPEC 10 MHz clock 2
ADDR-EQL	CRAH	15	Address equal	CK5MHz	ENAG	32	DPEC 5 MHz clock
ADDR-EQL/	CRAN	15	Address equal	CLALSKST/	FKCE	55	Clear all seek status flip-flops
ADDRINDX	ESCK	24	Address index	CLDSKLOC/	EKAD	54	Clear disk location counter
ADMRK127/	EHCC	64	127 address marks have been counted	CLFMCNTR/	FJAF	59	Clear format counter
ADRIDXUP/	CLCK	51	Sector mark or index pulse	CLSECLOC/	FLAN	52	Clear sector location counter
ADRMRKER	CHCP	68	Address mark error	CM-ADD-M/	CJAP	61	Address controller message
				CM-ENABL	FGCG	72	Controller message enable

Signal Name	Backplane Pin No.	Schematic Page No.	Description	Signal Name	Backplane Pin No.	Schematic Page No.	Description
CM-ERROR	FSCD	24	Controller message error	DATA 04	BNCG	27	DPEC internal data bus line 04
CM-ERROR/	FSCE	24	Controller message error	DATA 05	BNAG	27	DPEC internal data bus line 05
CM-LOAD/	EJAL	62	Controller message load	DATA 06	BNCH	27	DPEC internal data bus line 06
CM-R/W	EJAF	61	Controller message write	DATA 07	BNAH	27	DPEC internal data bus line 07
CM R/W/	CJCP	61	Controller message read	DATA 08	BNCN	27	DPEC internal data bus line 08
CM-SEL	CKCH	55	Controller message select	DATA 09	BNAN	27	DPEC internal data bus line 09
CM-START	FJAC	62	Controller message start	DATA 10	BNCP	27	DPEC internal data bus line 10
CM-START/	CJAD	62	Controller message start	DATA 11	BNAP	27	DPEC internal data bus line 11
CMGOIDLE/	CJCE	60	Controller message go to idle	DATA 12	CNCD	27	DPEC internal data bus line 12
CML09	EPAH	12	Controller message line 09	DATA 13	CNAD	27	DPEC internal data bus line 13
CML10	EPAJ	12	Controller message line 10	DATA 14	CNCE	27	DPEC internal data bus line 14
CML11	EPAK	12	Controller message line 11	DATA 15	CNAE	27	DPEC internal data bus line 15
CML12	EPAL	12	Controller message line 12	DM-RCVD	ESCD	23	Drive message received
CML13	FPAD	12	Controller message line 13	DMBUF	ESCM	23	Drive message buffer enable
CML14	FPAE	12	Controller message line 14	DMBUF/	ESCL	23	Drive message buffer enable
CML15	FPCL	12	Controller message line 15	CMCNTNUE	ESCF	24	Drive message continue
CML16	FPCM	12	Controller message line 16	DMFAULT	ENCD	26	Drive message fault
CMODE2*0	BJCN	60	Controller mode 2 0	DMSRCK	ESAN	23	Drive message shift register clock
CMODE2*0/	CJAF	60	Controller mode 2 0	DMSRCLR/	ESAQ	23	Drive message shift register clear
CMODE2*1	CJCD	60	Controller mode 2 1	DMSRCLRT	FNCJ	26	Drive message shift register clear
CMODE2*1/	CJCC	60	Controller mode 2 1	DMSRENB	ESCH	23	Drive message shift register enable B
CMSELHD4	FGCC	71	Controller message, select head 4	DMSTAS 7	ENAM	31	Drive message STATUS register line 7
CM2-OM11/	EJCE	62	Controller message 2 0, in mode 11	DMSTAS10	ENCM	31	Drive message STATUS register line 10
CYLHDEQL	CRAJ	15	Cylinder and head equal	DMSTAS14	ENAL	31	Drive message STATUS register line 14
DATA 00	BNCB	27	DPEC internal data bus line 00	DMSTAS16	ENAK	31	Drive message STATUS register line 16
DATA 01	BNAB	27	DPEC internal data bus line 01	DMSTAS20	ENCK	31	Drive message STATUS register line 20
DATA 02	BNCC	27	DPEC internal data bus line 02				
DATA 03	BNAC	27	DPEC internal data bus line 03				

Signal Name	Backplane Pin No.	Schematic Page No.	Description	Signal Name	Backplane Pin No.	Schematic Page No.	Description
DMSTAS21	ENCJ	31	Drive message STATUS register line 21	ENDSCXFR	EGAK	71	End of transfer
DMSTAS23	ENAH	31	Drive message STATUS register line 23	ENSNCDET	FKCG	57	Enable sync detector
DMSTAS24	ENCG	31	Drive message STATUS register line 24	EPCEQL	CRCG	15	Error protection code equal
DPC-RMOT/	FKCJ	55	DPEC is in remote	ERD-ENRD	BHCJ	66	Extended result descriptor, enable result descriptor
DPEC-EXC	FHCP	68	DPEC exception	ERDXFREN/	ENCH	25	Extended result descriptor, transfer enable
DR-READY	ESCN	24	Drive ready	ERDXMTNG	ENAE	25	Extended result descriptor transmitting
DR-READY/	FSCB	24	Drive ready	EXECUTE	BQCJ	3	Execute
DR-THERE	BPAC	7	Drive there	FAN-FAIL	FHCE	69	Fan failure
DR-THRCK/	FKCK	53	Drive there clock	FIRCDERR	EQCN	6	Fire code error
DRIVEKOK	FNAM	32	Drive okay	FIRCOMPEN	FJCF	59	Fire code compare enable
DRIVCKOK/	ENCN	32	Drive okay	FIRENCEN	FHAP	65	Fire code enable
DRNPRSNT	BHAB	67	Drive not present	FIREOUT	EQAC	6	Fire code out
DRONLINE	ESCG	24	Drive on line	FIRESHEN	CHAP	65	Fire code shift enable
DRONLINE/	ESAG	24	Drive on line	FLAGWRTN	CLCC	52	Writing relocate flag bit
DRUNSAFE	CGCL	70	Drive unsafe	FMCNTF	FHCG	64	Format control counter F
DRXMITEN	FHAM	65	Drive transmit enable	FMCNT9	FHAD	64	Format control counter equal to 9
DR4CLK	BRAD	18	Drive 4 clock.	FMIDLING	EJCN	59	Format idling
DR4DM	CRCM	18	Drive 4 drive message	FMWRONES/	FJCE	58	Format control term: write all 1's
DR4DTA	BRCB	18	Drive 4 data	FMWRZERO	FLAM	52	Format control term: write zeros
DR5CLK	FRAF	18	Drive 5 clock	GOTO5FR4/	CGAM	73	Go to mode 5 from mode 4
DR5DM	ERAE	18	DRive 5 drive message	GTM10R15/	ELAE	49	Go to mode 1 or 15
DR5DTA	FRAD	18	Drive 5 data	GTM8FR10/	CLCG	47	Go to mode 8 from mode 10
DR6CLK	BRAJ	18	Drive 6 clock	GUNIT2*0	BHCE	67	Gated unit number 1
DR6DM	CRCK	18	Drive 6 drive message	GUNIT2½1	BHCD	67	Gated unit number 2
DR6DTA	BRAG	18	Drive 6 data	GUNIT2*2	BHCC	67	Gated unit number 4
DR7CLK	FRAP	18	Drive 7 clock	HDR-ERR	FNCN	32	Header error
DR7DM	CRCN	18	Drive 7 drive message	HEAD-ERR	FGCA	70	Drive exception condition head error
DR7DTA	FRAL	18	Drive 7 data	IDLE	BKCF	55	Idle
DSKLOCEQ	ERCE	14	Disk location equal	IDLE/	CKCG	55	Idle
DTSNCSTF/	FMCN	38	Data sync start flip-flop	IDXMRKER	CGCF	70	Index mark error
DTSYN CER	FHAH	68	Data sync error	ILL-CYL	EGAN	70	Illegal cylinder
ENABL-WR	BJAM	60	Enable write	IMMDSEEK	BFCM	45	Immediate seek
ENADDRCT/	BPAB	7	Enable address counter				
CNCKDET	BKCD	56	Enable clock detector				
ENDOF CYL	CPCCK	9	End of cylinder				
ENDOFPAK/	EPCJ	9	End of pack				
ENDOFTRK	FPCE	9	End of track				

Signal Name	Backplane Pin No.	Schematic Page No.	Description	Signal Name	Backplane Pin No.	Schematic Page No.	Description
IMMDSEEK/	CFAC	45	Immediate seek	MANTRECV	BHAG	69	Maintenance received
INADDRCT	FLCD	51	Increment address counter	MDEO	ELCG	50	Mode zero
INADRMRK	BFCE	45	Increment address mark	MDEO*W1/	FKCN	57	Mode zero word 1
INDSKLOC	FLCF	51	Increment disk location counter	MDE1	ELCH	50	Mode 1
INITIAL	ELAG	47	Initialize operation	MDE4A	CKAE	54	Mode 4 A
INITIAL/	BHCQ	67	Initialize operation	MDE4FLOP	EKAF	56	Mode 4 flip-flop
INSECLOC	BKAQ	54	Increment sector location counter	MDE5A	BKCK	53	Mode 5 A
INSLWORD	EKAH	55	Increment sector location counter, word portion	MDE6	ELAF	50	Mode 6
INUNITCT	FKAK	57	Increment unit count	MDE6OR8	ELCK	50	Mode 6 or 8
JTRMINSC	FLAK	51	J flip-flop input term to increment sector counter	MDE9B	BJCD	63	Mode 9 B
KTRMBUSY/	BLAB	46	K flip-flop input term for busy flip-flop	MD11	ELCJ	52	Mode 11
LDPSREG/	CHCK	65	Load parallel-serial-parallel register	MD14	ELAB	50	Mode 14
LDRDBFFR	FHAN	65	Load read buffer	MD15A	BKCH	53	Mode 15 A
LDWRBFFR	EHCL	65	Load write buffer	MD6*NOWR	EJCQ	58	Mode 6 and no write
LOAD-AC/	BRCE	17	Load address counter	MD6*WR	CJAM	58	Mode 6 and write operation
LOC-EXEC/	FFAE	42	Local execute (in slip mode)	MEMUN2*0	FPCC	10	Memory unit zero-(Binary 1)
LOC-89/	ERAQ	13	Sector location 89	MEMUN2*1	FPCB	10	Memory unit two-(Binary 2)
LOC=ZERO	BRAE	13	Disk location counter at zero	MEMUN2*2	FPCA	10	Memory unit four-(Binary 4)
LONG-DM	FSCF	24	Long drive message	MEMWRTEN/	EPCQ	10	Memory write enable
LOOPHEAD/	FFCE	42	Maintenance switch enabled causing loop on head to be true	MNCLRRAW/	FFAH	42	Raw maintenance clear
LOOPMD10/	FKCA	56	Loop on mode 10	MNERDWD1/	FNCH	25	Maintenance extended result descriptor
LOOPSEC/	FFCD	42	Maintenance switch enabled causing loop on sector to be true	M15DSPRD	BHAH	69	Mode 15 display result descriptor
MAIN-CLR	EFCD	42	Main clear term	M4 0*RWV	BKAH	53	Mode 4, part zero and read, write or verify
MAIN-CLR/	FFCA	42	Main clear term	NEEDTOWR	BFAM	45	Need to write
MAIN-CL1/	BFAL	42	Main clear one term	NEEDTOWR/	CFAG	45	Need to write
MAINMD*0	ELAD	50	Main mode zero (2*0)	NOADDRLD/	FFCC	42	No address load
MAINMD*1	ELAC	50	Main mode 1 (2*1)	NOEXCHNG/	BHAM	67	No exchange
MAINMD*2	ELCE	50	Main mode 2 (2½2)	NRMLUNST/	FKAG	57	Normal and unsettled
MAINMD*3	ELCC	50	Main mode 3 (2*3)	NO	FQCD	4	N zero variant
				N1	FQAD	4	N one variant
				N2	FQCF	4	N two variant
				N3	FQAG	4	N three variant
				N3/	FQCG	4	N three variant
				OFFSETEN	BHCG	68	Offset enabled
				OFFSETIN	EHCJ	68	Offset toward the spindle
				OLD=NEW/	EPAG	10	New cylinder address is equal to the old cylinder address

Signal Name	Backplane Pin No.	Schematic Page No.	Description	Signal Name	Backplane Pin No.	Schematic Page No.	Description
OP1	FQCE	4	Operation code 1	READ	CHCC	67	Read operation
OP2	FQAE	4	Operation code 2	READY	EKCD	56	Ready
OP3	FQAH	4	Operation code 3	RELADDR	CHCJ	67	Relocate, address information used as data
PARERR	EQAB	3	Parity error	RELDATA	BHCL	67	Relocate, data information used as data
PBMN-CLR/	BFCE	42	Pushbutton main clear	RELOC	EFCH	45	Relocate operation
PJTRMINC	CGCD	72	Part of J flip-flop term to increment sector location counter	RELOC/	EFCC	45	Relocate operation, low true
PLO-LATE	CHAD	67	Phase lock loop term to the drive causing late strobe pulses	RELPASS2/	CFCE	45	RElocate pass 2
PLOEARLY	CHAC	67	Phase lock loop term to the drive causing early strobe pulses	REMOTE	EFCB	45	Remote
PTCASKST/	ELAH	49	Part of clock for seek status	RESDESEN	CHCH	66	Result descriptor enable
PTGT4FR6/	BGCL	71	Part of go to mode 4 from mode 6	RESDESEN/	EHAJ	66	Result descriptor enable
PTINADMK/	EGAJ	71	Part of increment address mark	RESTORE	CKAM	54	Restore
PTJTRMSD/	BGCQ	73	Part of J input flip-flop term	RESTORE/	FPAG	12	Restore, low true
PTLDSLOC/	BKAP	57	Part of load sector location counter	RESTOREN/	BHAK	67	Restore enable
PTM6TO15/	FGAE	73	Part of go to mode 15 from mode 6	REVSDONE/	EHAF	64	Revolution counter completed, Count 255
PT1CLSCL	CKAK	54	Part 1, clear sector location counter	ROGER-DM	CGAP	70	A drive message indicating no errors existed on the last CM
PT2CML0D	FKCB	56	Part 2, controller message load	RSELECT	BQCP	3	Raw select
PT4GMD15/	FLAG	48	Part 4, go to mode 15	RWV	BFAP	45	Read, write, or verify
PT5GMD15/	CGAD	72	Part 5, go to mode 15	SECHDEQL	CRCF	15	Sector and header address equal
PT6GMD15/	FHCD	69	Part 6, go to mode 15	SEEKINCL	EGAM	70	Seek incomplete
PT7GMD15/	EGAC	71	Part 7, go to mode 15	SELECT	FFCK	45	Select
PWRRESET/	FGCD	71	Power reset	SEL84ADR	CFAE	45	Select 84 adder
PWRRSYNC/	BFCF	42	Synchronized power reset	SEND-ERD	CHCF	67	Send extended result descriptor
P2INADMK/	CLCA	47	Part two of increment address mark	SEND-ERD/	CHCN	66	Send extended result descriptor
RAWDTAIN	ESCB	19	Raw data input	SEND-ST5	CJAJ	60	Send status
RD-BIT15	EHCH	68	Result descriptor bit 15	SER-HEDR	CRAG	16	Serial header
RDATA	FJCG	59	Read data	SERDTA=0	FHCL	65	Serial data equal to zero
RDBUFEN/	EHAG	66	Read buffer enable	SERDTAIN	FNCP	32	Serial data in
RDMANT	BHAL	67	Read maintenance	SERDTAOT	EQCQ	4	Serial data out
				SERMPXRO	CHAN	65	Serial multiplexer 0
				SERMPXR1	CHAG	65	Serial multiplexer 1
				SETSKSTS	BKCP	54	Set seek status
				SKSTATUS	EFCM	44	Seek status
				SPRVRFY/	CFCG	45	Spare sector verify

Signal Name	Backplane Pin No.	Schematic Page No.	Description	Signal Name	Backplane Pin No.	Schematic Page No.	Description
SRD	FJAH	59	Send result descriptor	WRADR	FJCN	59	Write address
ST-8TIMR/	FKAB	56	Start 8 second timer	WRD	FJCM	59	Write data
STADRCMP	FMCF	38	Start address compare	WRFIR	FJAM	59	Write firecode
STBLKRDY	FLCL	49	Start block ready	WRITE	CHAL	65	Write operation
STDTAXFR	EMCB	38	Start data transfer	WRITE/	CHCA	67	WRite low true
STERDOUT	FJAL	58	Start extended result descriptor output	WRLOCKOT	EGCM	70	Write lock out
STLSKTRM/	ELAK	48	Settled seek terminate	WRZ	FJAG	59	Write zeros
STROB-AD/	EHCE	68	Strobe address portion of extended result descriptor	WR1	FJCP	59	Write 1's
STUKDATA	EHCQ	68	Stuck data; No data transfer on a read	WR32HEDR	CHAH	65	Write 32 bits of header information
ST25T1MR/	BKAL	54	Start 25 millisecond timer	The terms that follow that have the WnnBnn format are WORD and BIT times. Their definitions are self explanatory and will not be listed.			
ST25OTMR/	FKCC	56	Start 250 microsecond timer	WO/	BMAD	33	
SW-LOCAL	CKAC	55	Switch to local oscillator 10 MHz clock	WOBO	BMCB	35	
SW-TO-DR	CKAH	55	Switch to 10 MHz drive clock	WOB11	BMAE	35	
TESTOP/	CHAE	67	Operation code equal to 7 (Test operation code)	WOB12	EMCF	35	
TIME-OUT/	FMAB	37	Time out, low true	WOB13	BMCD	35	
TMOT25MS	FMAA	37	Time out after 25 milliseconds (NO INDEX detected)	WOB14	BMCE	35	
TMOT25OU	FMCA	37	Time out after 250 microseconds (NO ADDRESS MARK detected)	WOB15	BMCF	35	
TMOT8SEC	FMCB	37	Time out after 8 seconds (Remote power up)	W1/	BMCC	33	
TRY-DIAG/	CNCP	25	Try diagnostics	W1B0	BMAF	35	
TSTSTKDT/	BKAK	53	Test for stuck data (no data transfer on a read)	W1B11	BMCG	35	
UNIT2*0	FQCP	4	Unit 0	W1B15	BMCH	35	
UNIT2*1	FQAP	4	Unit 2	W1B6	BMAH	35	
UNIT2*2	FQCN	4	Unit 4	W10/	CMCF	34	
UNIT2*3	FQCM	4	Unit 8	W10B14	CMCK	36	
UNIT4SEL	FSCJ	19	Select unit 4	W10B4	CMCL	36	
UNIT5SEL	FSCH	19	Select unit 5	W104B7	FMAC	36	
UNIT6SEL	FSAJ	19	Select unit 6	W106B13	EMCK	36	
UNIT7SEL	FSAH	19	Select unit 7	W106B15	EMAJ	36	
VERIFY/	BHCM	67	Verify operation	W108/	EMCC	34	
				W108B15	EMAK	36	
				W108B9	EMAH	36	
				W109/	EMAC	34	
				W109B1	EMCM	36	
				W109B14	EMAM	36	
				W109B7	EMAL	36	
				W11B14	CMCN	36	
				W110/	FMCE	34	
				W110B9	CMAE	36	
				W111B7	FMCC	36	
				W118/	CMAJ	38	
				W118B7	EMCJ	38	
				W119B15	EMCQ	36	
				W127B14	CMCJ	34	
				W127B15	CMAM	34	
				W13B15	FMCD	36	

Signal Name	Backplane Pin No.	Schematic Page No.	Description	Signal Name	Backplane Pin No.	Schematic Page No.	Description.
W14/	CMAF	34		W5B1	BMAN	35	
W14B0	CMCP	36		W5B15	BMCP	35	
W14B1	CMAL	36		W6/	BMAC	33	
W14B2	CMAK	36		W6B15	BMCQ	35	
W14B3	EMCE	36		W6B6	BMAP	35	
W14B4	EMAE	36		W61B14	CMCA	36	
W14B5	EMCG	36		W64/	CMAD	34	
W14B6	EMCH	36		W64B14	EMAG	36	
W16/	CMAF	34		W7B1	BMAQ	35	
W16B13	EMAD	36		W7B4	CMAA	35	
W16B9	EMCD	36		W8/	BMAB	34	
W2B0	BMCK	35		W8B15	CMAG	35	
W2B1	BMCL	35		W8B5	CMAC	35	
W2B14	BMAK	35		W9B13	CMCD	36	
W2B15	BMAL	35		W9B14	CMCE	36	
W29/	CMCM	34		W9B15	CMAH	36	
W29B8	EMAF	36		XMPER+TD	FGAH	70	Transmission parity error or try diagnostics
W3B14	BMCM	35					
W30B6	EMCL	36		XMTNPERR	CGCE	70	Transmission parity error
W4B13	BMAM	35					
W4B15	BMCN	35		XMENABLE	EHAH	66	Transmission enable

NOTE

The symbol “*” indicates that the number to the left of the symbol is to be raised to the power of the number to the right. For example, 2 * 3 = 8.