B 1700

SPO CONTROL

Burroughs

FIELD ENGINEERING

TECHNICAL MANUAL

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INDEX

Introduction and Operation

GENERAL DESCRIPTION

The SPO Control consists of one card located within either the I/O Base or an I/O Base Extension. The Supervisory Print Out (SPO) used with the SPO Control is the Model 33/35 Keyboard Teletypewriter. The use of the SPO provides the system with an input/output device which allows an Operator to communicate with the System.

INTERFACE

The Interface shown in Figure I-1 illustrates all control and data transfer lines between the Processor, SPO Control and SPO Device. The Interface between the Control and the Processor is via the Base Distribution Card in the I/O Base or via the Base Distribution Card and a Sub-Distribution Card (Extension) if the SPO Control is located within an I/O Base Extension. Refer to the I/O Base Technical Manual for details.

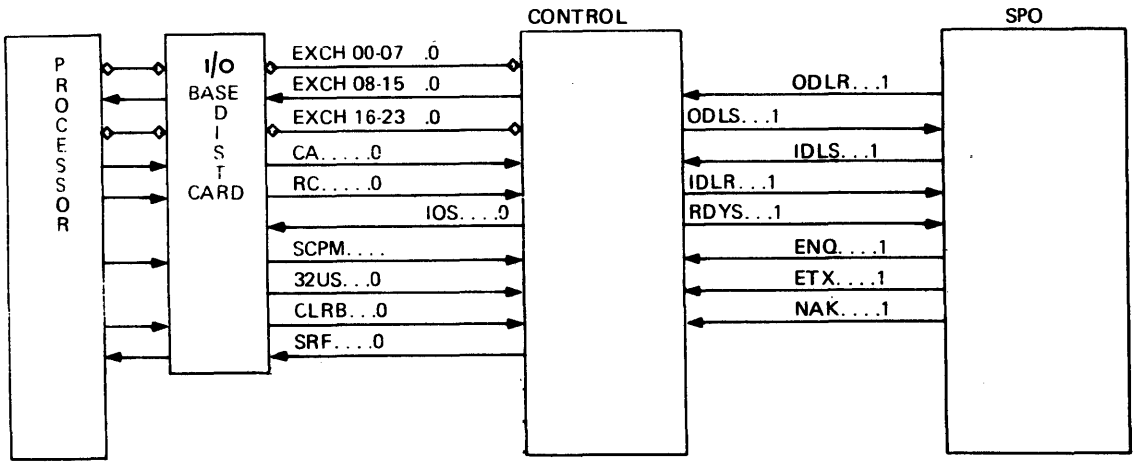


Fig. I-1

TYPE OF CODE

The SPO Device uses the U.S. Standard Code for Information Interchange (ASCII) internally. The Control provides Extended Binary Coded Decimal Interchange Code (EBCDIC) to ASCII translation when designated during write operations (Processor to SPO). The Control also provides ASCII to EBCDIC translation when designated during read operations (SPO to Processor).

DATA STORAGE

A 8 x 100 bit MOS Register provides storage of 0 to 75 characters of SPO data plus three bytes of a Reference Address.

OPERATION

The Control sends and receives bit serial data to/from the teletypewriter. The Processor sends and receives character serial data to/from the Control.

READ OPERATION

In a system environment two conditions will cause a SPO Read operation to be initiated:

1. Depression of the ENQ Key by the operator. The Processor must recognize that the ENQ has been depressed and in response, generate a read operation which turns on the ready light.
2. When the system is running under MCP Control, it is possible to execute a program which requires operators input via the SPO. A read operation is initiated by the Processor and the ready light is turned on.

USASCII X3.4-1967

Bits b_7 b_6 b_5					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4	b_3	b_2	b_1	Row / Column	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P	`	p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,		L	\	l	¦
1	1	0	1	13	CR	GS	-	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	^	n	~
1	1	1	1	15	SI	US	/	?	O	_	o	DEL

8TH BIT DESIGNATES PARITY. BITS 1 THRU 7 ARE ADDED TOGETHER, IF THE RESULT IS ODD, THE 8TH BIT IS "ON", IF THE RESULT IS EVEN THE 8TH BIT IS "OFF".

Fig. I-2

WRITE OPERATION

In a system environment the processor will initiate SPO write operation to output messages to the Operator. Write operations are completely software controlled.

TEST OPERATION

A test operation is used and initiated by the Processor (under software control) to determine the following:

1. The SPO Ready Condition
2. The Control ID (Identity)
3. Whether or not the Enquiry Key (ENQ) has been depressed.

PAUSE OPERATION

A variance of the test operation used by the programer. This operation does a test if the control and causes a pause of 9.08 milliseconds. This is used by software to allow time to service the controls last operation.

EBCDIC (REVISED)

b8 b7 b6 b5 / BITS	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
b4 b3 b2 b1 ROW / COL	0	1	2	3	4	5	6	7	8	9	10 A	11 B	12 C	13 D	14 E	15 F
0 0 0 0 0	NUL	DLE			SP	&	–						+ *	! **		0
0 0 0 1 1	SOH	DC1					/		a	j			A	J		1
0 0 1 0 2	STX	DC2		SYN					b	k	s		B	K	S	2
0 0 1 1 3	ETX	DC3							c	l	t		C	L	T	3
0 1 0 0 4									d	m	u		D	M	U	4
0 1 0 1 5	HT	NL	LF						e	n	v		E	N	V	5
0 1 1 0 6		BS	ETB						f	o	w		F	O	W	6
0 1 1 1 7	DEL		ESC	EOT					g	p	x		G	P	X	7
1 0 0 0 8		CAN							h	q	y		H	Q	Y	8
1 0 0 1 9		EM							i	r	z		I	R	Z	9
1 0 1 0 10 A					[	]		:								
1 0 1 1 11 B	VT				.	$	,	#								
1 1 0 0 12 C	FF	FS		DC4	<	*	%	@								
1 1 0 1 13 D	CR	GS	ENQ	NAK	(	)	_	'								
1 1 1 0 14 E	SO	RS	ACK		+	;	>	=								
1 1 1 1 15 F	SI	US	BEL	SUB	|		?	"					DELIM-ITER			

Fig. I-3

PERIPHERAL OPERATION

The Supervisory Printer is a Model 33/35 Teletypewriter and is used as an Input/Output device for communication between the operator and the system. Input is by means of an ASC11 coded keyboard and several switches on a separate control panel. Output is by means of a moving head printer, operating at a speed of approximately 10 characters per second.

The depression of a key on the keyboard causes code bars to position to a unique combination, which in turn, through a contact mechanism, provides a unique combination of seven data bits and one parity bit (always two). These levels are connected to a rotative contact, which, when triggered, produces a serial bit pattern output of the required frequency. In addition to the eight bits of the keyboard input, the rotative contact provides one start bit and two stop bits for each character.

During a "local" operation of the SPO, the decoded character is directed in serial bit form to a selector magnet assembly and the print mechanism is activated.

During a "remote" operation the SPO works in conjunction with the SPO I/O Control. This time the decoded character is directed first to the I/O control, which stores the character in an MOS memory (buffer). At the same time as the character is being stored, it is transmitted back to the SPO, where a print cycle is instigated and the character is printed on the SPO itself.

With the SPO in the remote mode the processor may transmit messages to it through the I/O Control, and cause them to print. Within the SPO itself the printing of processor messages is handled in an identical manner to the way its own "looped back" messages are handled.

GLOSSARY OF TERMS

REGISTERS AND COUNTERS

Command Register	Accepts all commands to all channels during CA time.
Command Variant Register	Accepts all command variants to all channels during CA time. Clears at RC time. Note that each Control must accept all commands and command variants as the TEST Service request command is sent to all channels with no particular channel number designated.
OP-Register	Accepts OP-Code when in STC = 01.
Input Register	Accepts parallel data from the exchange lines and serial data from the SPO. Accepts all Transfer Out data from the exchange lines, but enters only the appropriate data into the MOS Register during the appropriate Status Counts. When accepting serial data from the SPO, the register is in the Bit Set Mode. By using a 1 x 8 Decoder (EFAN) and the Bit Counter, each serial data bit is "latched" into the Input Register.
100 bit MOS Register	100 bits in length and 8 bits high the register requires a two phase clock drive to complete a shift right by one of the entire 100 bits. Each shift right by one requires four clock periods.
Status Counter	(STC) Keeps count of the status counts (00-23). The status count is returned to the Processor during the RC portion of all commands except the Test Service Request command.
Sequence Counter	(SC) Sequences the actual data transfers to/from SPO.
Byte Counter	(BCNT) Counts the actual number of bytes (up to eight bits) in the MOS Register.
Bit Counter	(BC) is used to count the number of serial data bits transferred to/from the SPO. During read SPO operations, the counter will count from 00 to 01 to 07 and back to 00 again. Each count from 01 thru 07 indicates one of seven data bits. During write SPO operations the counter will count from 00 to 01 and back to 00. BC01 thru BC07 indicates the transfer time of data bits.
Bit Time Counter	(BTC) counts to 284 using the 32 usec. clock. This is 9.088 msec., the length of time each data bit must be present during transfers to/from the SPO. BTC is used to increment the Bit Counter by 1 every 9.088 msec. BTC is also used for the PAUSE OP-Code.

INTERFACE (CONTROL/SPO)

ETX	End of Text, is true when the operator depresses the ETX key on the SPO keyboard. The level indicates to the Control the Operator has completed typing the message.
NAK	Negative Acknowledgement is true when the NAK key on the keyboard is depressed. It indicates the Operator has made a typing error on input. NAK true will cause the NAK and ETX flip-flops to set, therefore, the input operation is terminated. The Operator must depress the ENQ key and wait for the Ready Light to come on before another input from the SPO can be made.
ENQ	Enquiry is true when the Operator depresses the ENQ key on the keyboard. It indicates the Operator wants to type (input) a message. The operator must wait for the Ready Light to turn ON before the input message can be typed.
RDYS	RDYS when true will turn on the SPO Ready Light. It indicates the Operator can type an input message to the Processor. RDYS is the result of depressing the ENQ key. The Processor will sense the presence of ENQ via Result Descriptor returned to the Processor at the completion of an operation. The Processor then must initiate a Read OP operation via a transfer out command to the SPO Control.
ODLS	Outgoing Data Level to the SPO, is the serial data line to the SPO. The level is +11.3 volts for a Space and -8.0 volts for a mark.
ODLR	Outgoing Data Level Return is at +11.0 volts for a Space and -7.0 volts for a Mark. ODLR is also used to indicate the SPO Not Ready condition. Quiescently (in the IDLE state) ODLR is at -7.0 volts which indicates the SPO is Ready.
IDLS	Incoming Data Level from the SPO is the serial data transfer level from the SPO to the Control. The level is at +10.5 volts for a Space and -6.0 volts for a Mark.

IDLR	Incoming Data Level Return is the return line for serial data transfers from the SPO to the Control. IDLR provides concurrent typing during read SPO operations. The level is a -7.0 volts for a Mark and -12.0 volts for a Space.
CONTROL MNEMONICS	
BCNT10/.	Byte count does not equal 100.
BUFO . . . . thru BUFT	MOS buffer register outputs 0 through 7.
C A R	Buffered command active signal from the processor to I/O system and is true for one clock period. It indicates that a command is being transmitted. The exact command is defined by bit 20, 21, and 22 of exchange.
C H	Channel recognition. Channel number sent during CA time compares with SPO control channel number.
CHAF	Channel active FIF, set by CH . . . ., reset by RC1 . . . .
CHARC	CHAF . . . . *RC1 . . . .
CHAXFR	CHAF . . . . xFRIN . . 1
CLEAR	Resets all I/O controls to the initial state. Signal is transmitted each time power is applied, at test and clear operation and with console clear button.
32CP	Buffered 32us slow clock. Pulse spacing is 32 usec.
DATAFF/	Data F/F not in the reset side output of the data flip-flop, the F/F is set with.
DSCP	Buffered SCOM synchronized system clock.
ENQF	Enquiring flip-flop. Operator depresses input request button on SPO to indicate he wants to enter message.
EXCEDF	Exceed flip-flop.
ETXF	End of text flip-flop. Operator depresses end of message button when finished typing message.
EXCH00 23	Data exchange bits. These 24 bits transfer information such as command variants, address, I/O device status and/or data etc.
EX00 R/D EX07 R/D	Result descriptor levels to be sent to the processor.
EXCH07.0	I/O channel present signal is transmitted on this I/O bus at test status or test and clear status time.
FLAG1	Buffered bit 7 output of the MOS register.
IDLC	When IDLS is equal to mark (-7v), IDLC is true.
IDLS	Incoming data level serial from SPO.
IDLR	Return line for serial data from SPO.
IOS	I/O send. The function is to switch the interface circuit on the distribution card to the transmit mode.
IR0 IR7	Outputs of CTL MOS interface, become inputs of MOS register.
MOS PH1	Outputs of MOS clock driver.
MOS PH2	
NAK/	Negative acknowledgement not. Operator depresses error button to indicate he has made an error on input. Outgoing data level serial to SPO.
ODLS	Outgoing data level serial to SPO.
ODLR	Return line of data to SPO.
ORXC0 ORXC7	Output signal to the processor.
PAUSE	OP code: return service request after a Pause of 9.08 msec.
PAUSOS/	Reset side output of count flip-flop.
R C 1	Buffered response complete signal, true for one clock period. If the transfer is from processor to I/O device, RC commands the device to accept the information on the exchange. If the transfer is from I/O device to processor, RC indicates that the information has been accepted by the processor and must move the information from the exchange.
RDYF	Reset side output of RDYFF when SPO power on and remote mode.
RDYS	Ready line to SPO. Turns on ready light.
READ	OP code, read data from SPO to the processor.
SC00 05	Sequence count 00 05.

SHAFEF	Share flip flop is set by ETX and inhibits MOS shift.
SHF-1	It triggers clock generator and produces MOS register shift clock.
SHFWR	SHF--1 signal at write operation.
SHFWR/	SHF--1 signal at write not operation.
STC 00 23	Status count 00 23.
STC SUM	Comes true at STC11, STC12, STC13, STC15, STC18, STC19.
SORSDQ	Serial signals converted from the ASCII parallel.
STROBE	Enable serial to parallel conversion.
TEST	OP code
TESTER	Held high only when tested in card tester
TERM	Command variant: Terminates the flow at read or write operation.
TSR	Test service request: Command variant
TSTS	Test status: Command variant
VAR/	Variant of operation code
WRITE	OP Code: Write data from processor to SPO
XCH0 XCH7	Buffered signal from exchange
XFRIN	Command: Transfer in
XIR0 XIR7	Buffered HCXn signals true at STC7, 8, 9
XFROTA1	Command: Transfer out
XLT/	Translate not. When true translator is by-passed.
XLTBYD	CACHXF * XLTFS/

I/O DESCRIPTORS

The Supervisory Print Out (SPO) Control is capable of executing one of four I/O Descriptors (also referred to as OP-Codes). Each Descriptor is 24-bits in length with the following variables:

1. T represents the Translate Bit.
2. V represents the Variant Bit.
3. (.) represents "Blank" bits with no significance, these bits should be set to zero.
4. The three most significant bits (MSB) of the I/O Descriptor (Bits 23 thru 21) represent the OP-Code.

READ OP

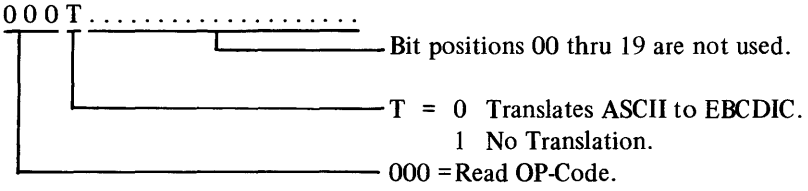


Figure II-1

The Read Op when received in the control will permit the operator to input from 0 to 75 characters from the SPO to the controls 100 x 8 MOS Buffer. As one line of print consists of 72 characters, the three additional characters provide for Line Feed, Carriage Return and End of Text. If ETX is not detected within 75 characters and a 76th key is depressed, a Flag bit is set in the Controls Input Register as well as the 76th character. Termination of a read operation will occur when either the ETX or NAK key is depressed or if a 76th key has been depressed and neither ETX nor NAK is sensed. When the 100 x 8 MOS buffer is assembled and termination of an input established, the processor must transfer the MOS buffer data from the control to the processor under software control.

WRITE-OP

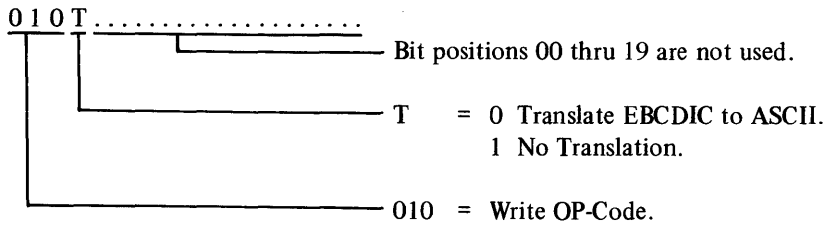


Figure II-2

The Write-Op when received in the control will cause the control to accept character serial data from the processor. Data transfers from the processor to the control are terminated when either the End of Text code is sensed, a terminate command is received or when the Controls Byte Counter is equal to 74 which indicates 75 characters hav been received. After receiving a Reference Address from the processor, the control will transmit the character data to the SPO, independent of processor intervention.

TEST-OP

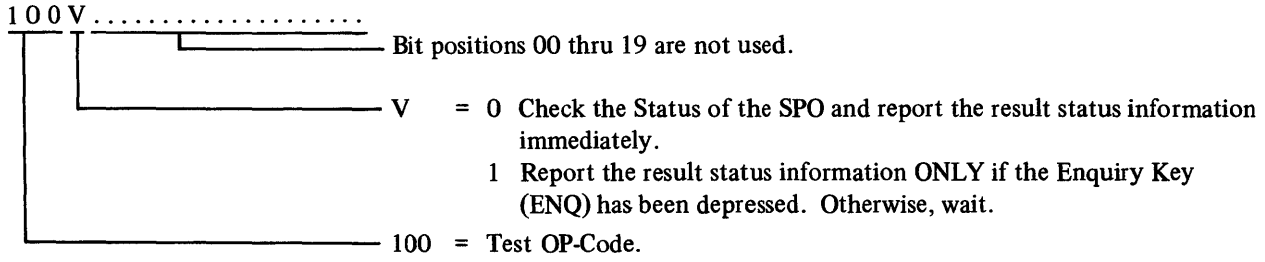


Figure II-3

The Test Op will test the SPO and Control for the following conditions:

1. Not Ready
2. Control ID
3. ENQ Key sensed. (See variant bit "V" of I/O Descriptor.)

PAUSE-OP

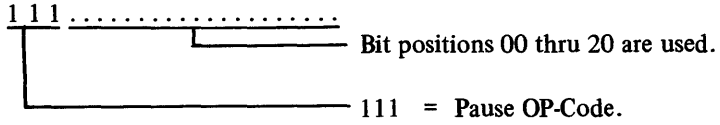
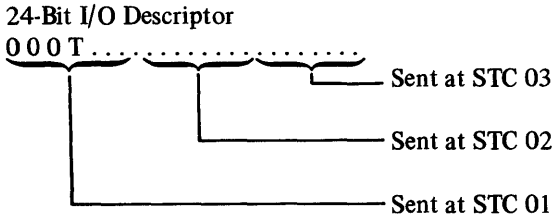


Figure II-4

The Pause OP will return a service request after a pause of nine milliseconds. The result descriptor returned must have the operation complete bit set. This OP-Code is sent to the control by the I/O Interpreter program when the next I/O descriptor is not yet available for execution. Upon completion of any pause, the next I/O descriptor is inspected by the I/O interpreter program to see if it is ready for execution.

I/O DESCRIPTOR TRANSFER TIMES

The 24 Bit I/O Descriptor is sent to the Control in three 8-Bit Bytes. First byte is sent at Status Count 01 time (STC01) the second at STC02 and the third at STC03. Only the first byte has significance. OP-Code and translate or variant Bits, if applicable, are sent with the first byte at STC01. Refer to the example of the READ OP Figure II-5.



Read OP, I/O Descriptor

Figure II-5

RESULT INFORMATION

At the completion of executing any of the four I/O Descriptors, a 24 bit result descriptor is available. The processor (under software control) must transfer the result descriptor from the Control to the Processor. The information available in the 24-bit result descriptor is as follows:

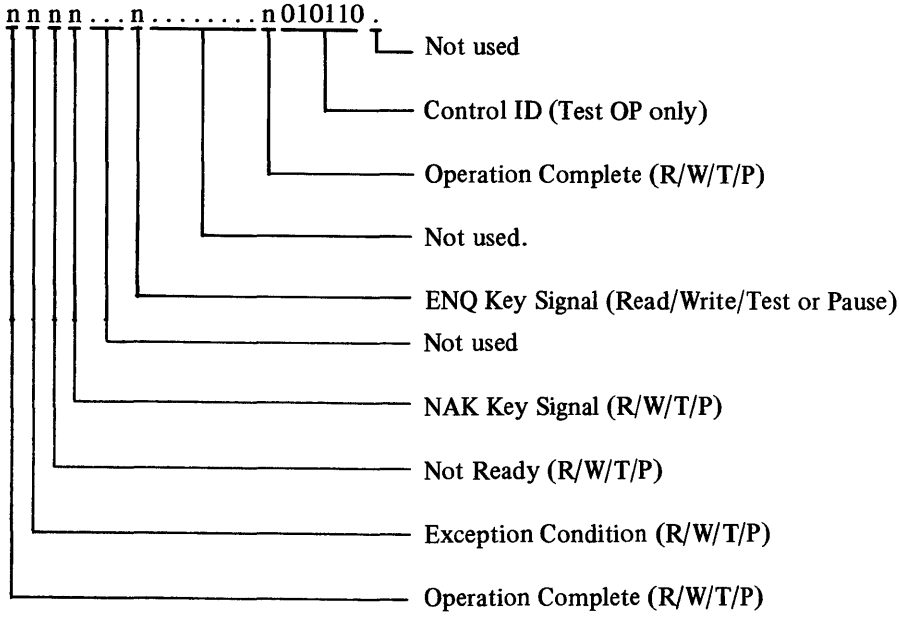


Figure II-6

RESULT DESCRIPTOR TRANSFER TIMES

The 24-bit result information available is sent to the Processor from the Control in three 8-bit Bytes. The first Byte is sent at Status Count 21 (STC21), the second at STC22 and the third at STC23. Refer to Figure II-6 which illustrates a SPO result Descriptor.

BASIC SERIAL DATA TRANSFER (SPO/CONTROL)

(Refer to Figure II-7 and Figure II-8)

READ SPO

Quiescently the Incoming Data Level from SPO (IDLS) and the Outgoing Data Level to SPO (ODLS) are at -6 volts and -8 volts respectively. Note the -12V supply is connected to the Conduction Bar the 2nd stop Bit is at the "reset" position of the brush rotator.

When a key is depressed the brush rotator connected to IDLS will make one revolution. The Start bit position is not connected to the -12V supply (IDLR) therefore the circuit is open. IDLS then goes to +10.5 Volts. The +10.5V is provided from the +12V supply within the SPO Control. Depressing the "U"-key as shown causes the ASCII code bits b1 thru b7 to be 1010101. Therefore each Data bit which is a one will allow current flow from the -12V supply through the conduction bar and to the Brush contacts within the rotator. IDLS at this time will be at -6 Volts. When the data bit is a zero, the -12V supply will not make contact with the brush rotator. IDLS at this time is at 10.5 Volts. IDLS is at -6 Volts when the Parity, 1st & 2nd stop Bit Positions are sensed. Refer to the Control's Interface level changer logic SCCIII for details.

WRITE SPO

ODLS, quiescently at -8 volts, will go to 11.3 Volts when the start bit is transferred to the SPO from the Control. With ODLS at +11.3 Volts, (Start Bit) a solenoid is released thus allowing one revolution of the selector magnet rotator. ODLS is at -8 Volts if the data bit = 1 and is at +11.3 Volts if the data bit = 0. The parity, 1st and 2nd Stop bit are each at -8 Volts ODLS provides for concurrent typing operations during Read SPO operations.

DATA TRANSFER TIMING – Refer to Figure II-8

Each of the 11 bits of serial data transferred to (from) the SPO from (to) the Control is 9.088 msec in duration. A Bit Time Counter (BTC) in the Control is counted to 284 with the 32 usec clock (284X32 usec = 9.088 msec). As effectively 11 serial data bits are transferred the total transfer time for one data or control character is therefore approx. 100 ms. (11X9.088ms = 100.776 ms)

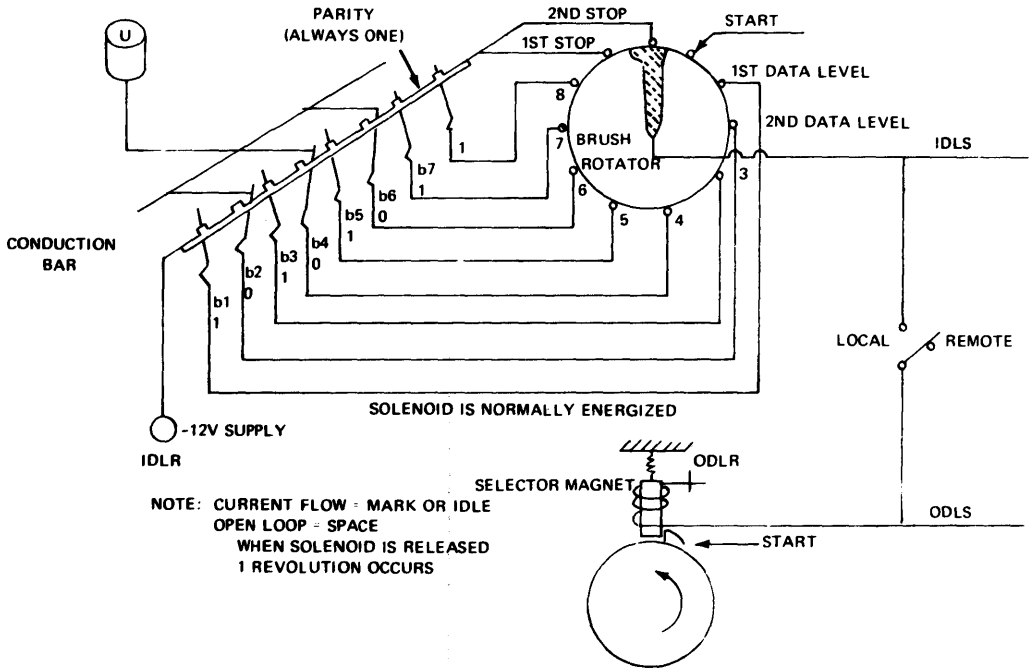


Fig. II-7 BASIC SPO/CONTROL SERIAL DATA TRANSFER

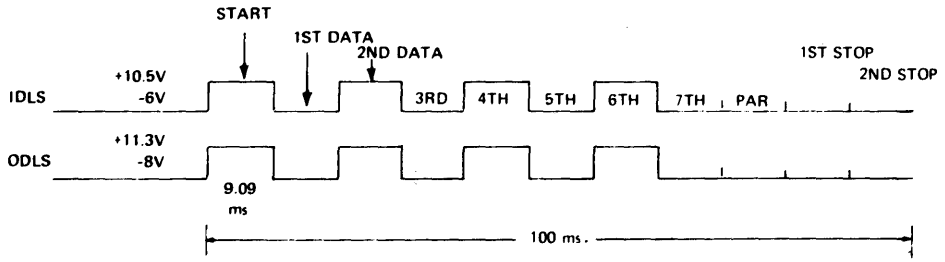


Fig. II-8 DATA TRANSFER TIMING

INPUT REGISTER
(Refer to Figure II-9)

The Input register to the 8X100 Bit MOS Shift Register consists of two 4-bit registers (RFBNs). The Input Register is in the D-Set Mode when a transfer out command is received and the command is for the SPO Control. The contents of the 24-Bit I/O Bus (8LSBs only) are set in the Input Register with the trailing edge of the next Delayed System Clock pulse.

If translation from EBCDIC to ASCII is designated then the 8LSB of the I/O Bus are gated through the translator to the Input Register.

Functional Detail

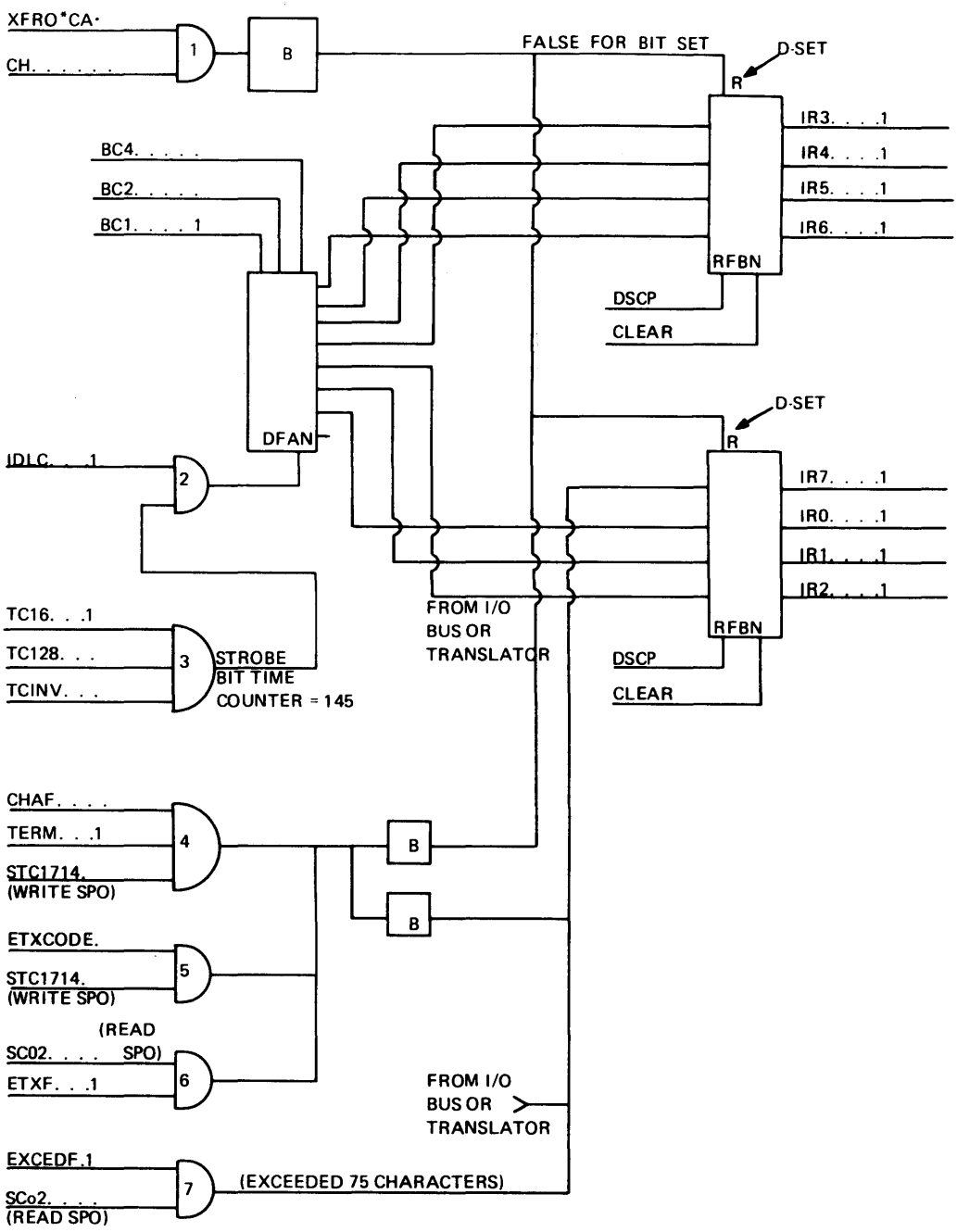


Fig. II-9 INPUT REGISTER

Gate 1's output is true when a transfer out command is received from the Processor and the Channel Number agrees with the Channel Number of the SPO Control. At this time the Input Register is in the D-Set Mode. Either untranslated or translated data is set in the Input Register at clock time.

Gate 2 gates the serial data bits from SPO to the Input Register. Incoming Data after Level Changer (IDLC . . . 1) is true for each serial bit equal to 1 (Mark).

Gate 3 provides strobing the SPO serial data bits at BTC = 144 time. The Bit Time Counter (BTC) is counted from 0 to 284 during the presence of each of the 11 serial data Bits.

Gate 4 true in addition to causing the Input Register to be in the D-Set Mode sets a 1 in the IR7 . . . . 1 bit position. This bit position is set if the operation is "Write SPO" and the terminate command is received.

Functional Detail

Gate 5 is true when the End of text code is received from the Processor on Write operations.
Gate 6 is true when either the ETX or NAK key has been depressed and a Read SPO operation is in progress.
Gate 7 is true during a Read SPO operation if the operator attempts to Key in more than 75 characters.
The significance of the 7th bit of the Input Register is when the data is shifted right in the 8 x 100 MOS Register, the 7th bit output of the MOS Register (if true) is a "Flag" to indicate the end of Data.

DATA TRANSFER (I/O BUS/CONTROL/SPO) – Refer to Figure II-10

The Block Diagram, Figure II-10 illustrates the data transfer paths to/from the Processor and the serial data transfer path to/from the SPO. The EXCH lines 00-07 are the 8 LSBs of the 24-Bit bi-directional I/O Bus. Data from the Processor on the EXCH lines 00-07 can be gated thru an EBCDIC to ASCII translator or it can by-pass the translator. The translate bit of the I/O Descriptor will designate and control the use of the translator. All data set in the 8 x 100 MOS Shift Register is first set in the Input Register. Only Character data to or from the SPO and the three 8-bit bytes of the Reference Address will enter the MOS Shift Register.

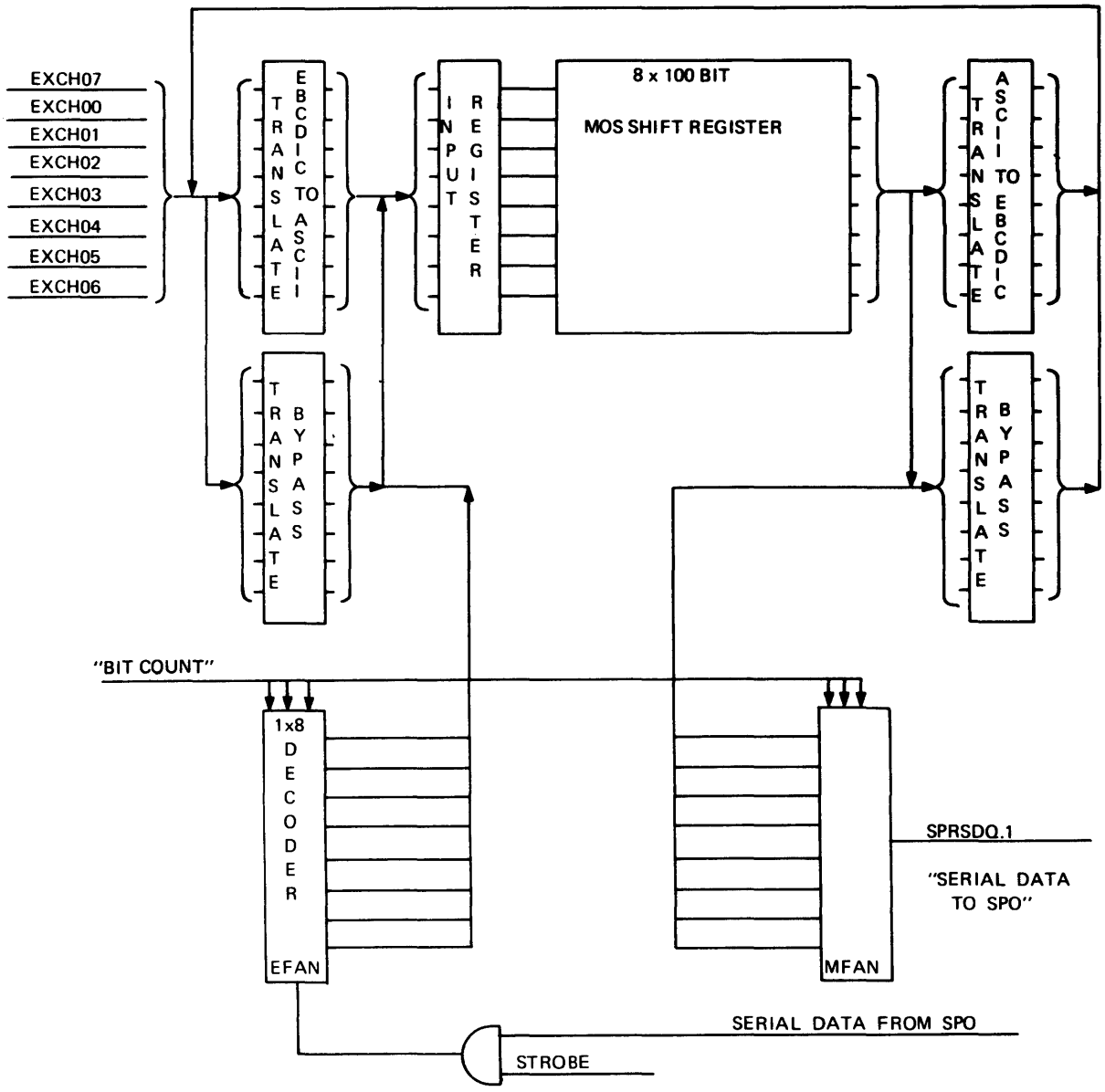


Fig. II-10 DATA TRANSFER; BLOCK DIAGRAM

ASCII to EBCDIC translation is provided at the output of the MOS Shift Register and is controlled by the translate bit of the I/O Descriptor.

When translation is designated on either a Read or Write SPO operation the three 8-Bit bytes of the Reference Address are also translated. When received from the Processor the EBCDIC to ASCII translation occurs and when sent back to the Processor the ASCII to EBCDIC translation occurs. Each of the 11 data bits to/from the SPO is present for 9.088 ms. The Bit Time Counter (BTC) is counted from 0 to 284 with the 32us clock during the time each of these bits is present. The Bit Counter (BC) is incremented by one when BTC = 284. A DFAN is used to gate each of the serial data bits 1 - 7 to the corresponding bit position of the Input Register. During serial data transfers from the SPO the Input Register is in the Bit Set Mode; therefore, as the Input Register is initially cleared before assembly each character from SPO only the 1 bits (MARK) will be set in the Register.

The Bit Counter (BC) is also used to strobe serial data to the SPO from the Output of the MOS Shift Register. A MFAN is used to compare the Bit Count with the proper data bit. If the Bit is true when the Bit Counter points to it, SPRSDQ.1 will be true. SPRSDQ.1 true will cause ODLS to go to -8 Volts.

TIMING (SERIAL DATA, INPUT/OUTPUT)

(Refer to Figure II-11)

READ OPERATION

Figure II-11 illustrates the timing of strobing the serial data bits (for one character from SPO) to the Input Register. The character illustrated is "U" whose ASCII code is 1010101 (b 1 - 7). Depressing the "U" Key will cause IDLC to go false. This starts the Bit Time Counter (BTC) and clears the Input Register. When BTC = 144 is true Strobe occurs. The Strobe which occurs when the start bit is present has no significance as the data bits are set in the Input Register when BC = 01 thru 07 is true. When BC = 07 is true and BTC = 283, the COUNT . . . Flip/Flop is reset which disables the BTC from being incremented with the 32us clock. IDLC is true when the parity and 1st and 2nd stop bit is received; however, as the strobe pulse does not occur and BC = 00 is true, the bits are not used in the control.

WRITE OPERATION

Figure II-11 illustrates the timing of gating the serial data bits (on character to SPO) from the output bit positions of the MOS Shift Register. The character illustrated is "U" whose ASCII code is 1010101 (b 1 - 7). When the write data is right justified in the MOS Shift Register, the Sub Counter (SC) is set to 05 and the BTC counter will start to count. When SC = 05 is true it forces ODL false thus the Start bit is sent to the SPO. When BTC = 284, 284CP is true and the BC counter is incremented by 1. When BC is equal to 01 thru 07 if the output bit position of the MOS Register which corresponds to the BC count is true, then SPRSDQ. is true. SPRSDQ. true causes ODL to go true thus a data bit (Mark) is sent to the SPO via ODLS. (ODLS = -6V for Mark). When the BC count is equal to 10 and 284CP is true, BC is cleared to zero.

During write operation the next character to be serially transferred to the SPO is shifted to the output position of the MOS Register when BC is set to zero. The BTC counter continues to count to 284. When BC = 0, ODL is again true which indicates the next start bit.

The last character to be serially transferred to the SPO is sensed by the "Flag" output bit position of the MOS Register (BUF7 . . . .). BUF7 . . . . when true will cause the COUNT . . . F/F to be reset at the same time the BC counter is set to zero. With COUNT . . . false, the BTC counter is disabled. The Flag Bit sensed also causes the Status Counter (STC) to be set to 18 and the Service Request F/F to be set. Note that STC18 and SRF will be true after the last character has been serially transferred to the SPO.

Functional Detail

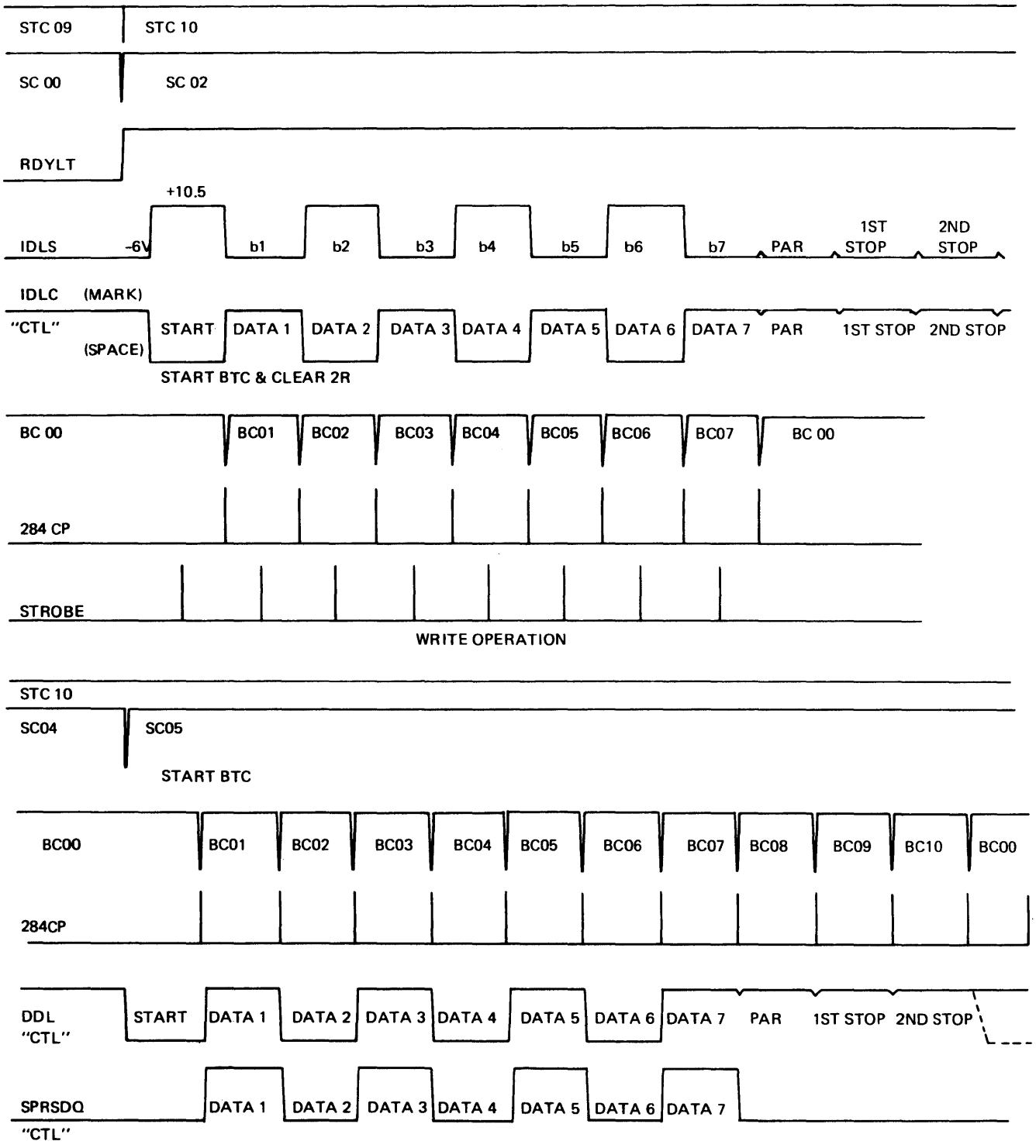


Fig. II-11

SIMPLIFIED FLOW

Each of the four OP-Codes (Read, Write, Test and Pause) when initiated within the Control logic will cause the Status Counter (STC) and the Sequence Counter (SC) to follow a definite sequence. The STC and SC's which are entered as the result of receiving the OP-Codes are shown in Figure II-12.

TEST OP		PAUSE OP					READ OP						WRITE OP			
STC	SC	STC	SC	STC	SC	Ready	STC	SC	Ready/STC	SC	STC	SC	STC	SC	Ready/STC	SC
1		1		10	06		1				Ready		1			
2		2		10	02		2				STC	SC	2			
3		3		10	03		3				10	06	3			
4		4		11			4				10	04	4			
5		5		12			5				10	05	5			
6		6		13			6						6			
7		7		15			7						14			
8		8		17			8						17			
9		9		21			9		10	00			7		10	00
10	06	10	06	22					18				8			
10	00	10	00	23					19				9			
18		10	01						20							
19		18							21							
20		19							22				18			
21		20							23				19			
22		21											20			
23		22											21			
		23											22			
													23			

Fig. II-12 GENERAL FLOW FOR OP-CODES

SIMPLIFIED FLOW OF READ OPERATION

STC01	The control in the quiescent state is at STC = 01. Assuming the SPO Control is the Channel designated, the OP-Code (Read) is gated from the EXCH bits 00 thru 07 to the OP-Register. The translate bit indicating either Translate or Translate Not is also set in the Variant Register. (Translation if indicated is from ASCII to EBCDIC).
STC02	No Action
STC03	No Action
STC04	No Action
STC05	No Action
STC06	Enable the Translator if ASCII to EBCDIC translation is to occur.
STC07	Receive the Reference Address (Byte 1) in the Input Register Shift the MOS Register right by 1 and increment the Byte Counter by 1.
STC08	Receive the Reference Address (Byte 2) in the Input Register Shift the MOS Register right by 1 and increment the Byte Counter by 1.
STC09	Receive the Reference Address (Byte 3) in the Input Register Shift the MOS Register right by 1 and increment the Byte Counter by 1. Turn ON SPO Ready Lite if SPO is Ready.

STC10 * SC00	(Only if SPO Not Ready) Upcount the Byte Counter to 100 and exit to STC18. When BCNT100 is true, Reference Address is right justified in the MOS Register. Set SRF.
STC18	(Only if SPO Not Ready) Send Reference Address Byte 1 to the Processor. Shift MOS by 1 & Increment BCNT by 1.
STC19	(Only if SPO is Not Ready) Send Reference Address Byte 2 to the Processor. Exit to STC20.
STC20	(Only if SPO is Not Ready) Send Reference Address Byte 3 to the Processor. Exit to STC21.
STC10 * 06	Check to be sure all Control Keys are clear.
STC10 * SC02	Serial character data is received from the SPO, assembled in the IR Register and shifted into the MOS Register. The Bit Counter is used to synchronize the incoming data pulses from the SPO with the Control's logic. When BC = 1 thru 7, a Strobe pulse is developed when the Bit Time Counter = 144 that strobes the serial data from SPO into the IR Register. The BCNT counter is incremented by 1 with each Shift which occurs. The operation terminates when either BCNT78 is true and a 76th Key is depressed or the ETXF flip-flop is set. Depressing either ETX or NAK sets ETXF.
STC10 * SC03	The Reference Address (Bytes 1, 2, & 3) and the SPO read data is right justified in the MOS Register. When BCNT100 is true, the MOS Register is right justified and the flow exits to STC11. SRF is set.
STC11	Send the Reference Address Byte 1 to the Processor and shift MOS right by 1. Reset the SRF flip-flop.
STC12	Send Reference Address Byte 2 to the Processor and shift MOS right by 1.
STC13	Send Reference Address Byte 3 to the Processor and shift MOS right by 1.
STC15	Send SPO Read Data to the Processor until the flag bit is sensed indicating the last character is shifted to the output of the MOS Register. This last character is sent during STC17. If instead of receiving a Transfer In command from the Processor a Terminate command is received, exit to STC21 to send the Result Descriptor. Data read from SPO and not already transferred to the Processor is not sent.
STC17	Send the last character in MOS to the Processor. The flag bit is also sent and the MOS Register is shifted right by 1. If instead of a Transfer In command, a Terminate command is received, the last character in MOS is not sent to the Processor; however, a shift right by 1 does occur. Exit in either case to STC21 to send Result Descriptor.
STC21	Send Result Descriptor (Byte 1) to the Processor.
STC22	No Action
STC23	Send Result Descriptor (Byte 3) to the Processor, exit to STC01.

SIMPLIFIED FLOW OF WRITE OPERATION

STC01	The Control in the quiescent state is at STC = 01. Assuming the SPO Control is the Channel designated, the OP-Code (Write) is gated from the EXCH bits 00 thru 07 to the OP-Register. The translate bit indicating either Translate or Translate Not is also set in the Variant Register. (Translation if indicated is from EBCDIC to ASCII).
STC02	No Action
STC03	No Action
STC04	No Action
STC05	No Action
STC06	Enable the Translator if EBCDIC to ASCII translation is to occur.
STC14	Character data is transferred from the Processor to the Control. Each character transferred in parallel to the Control is set in the Input Register and shifted in the 8 x 100 Bit MOS Shift Register. A Flag bit is set in IR7 when either the End of Text Code or the Terminate Command is received. If neither is received and the BCNT counter equals 73 and another character is received the Flow exits to STC17 to receive the last character. If the End of Text code is received the flow exits to STC17 but the last character (if received) is ignored. If the Terminate command is received the flow exits to STC07 to receive the Reference Address.
STC17	If the last character is received, the flag bit is set and the last character with the flag bit is shifted into the MOS Register. If the flag bit was set at STC14 then the Shift is disabled. Exit to STC07. If the terminate command is received, the Flag is set and shifted into the MOS Register (Bits 00-06 are zeros). If the flag was set at STC14 the shift is disabled. Exit to STC07.
STC07	Receive the Reference Address (Byte 1) in the Input Register Shift the MOS Register right by 1 and increment the Byte Counter by 1.

STC08	Receive the Reference Address (Byte 2) in the Input Register Shift the MOS Register right by 1 and increment the Byte Counter by 1.
STC09	Receive the Reference Address (Byte 3) in the Input Register. Shift the MOS Register right by 1 and Increment the Byte Counter by 1.
STC10 SC06	Check to be sure all control keys are clear.
STC10 SC00	Only if SPO is Not Ready. Set SRF and exit to STC18 after right justifying MOS Register.
STC10 SC04	Right Justify the MOS Register. When BCNT100 is true, exit to SC05 and set the COUNT flip-flop. The COUNT F/F set enables the Bit Time Counter (BTC) to count from 0 to 284 to 0 etc.
STC10 SC05	Serial Data bits are transferred to the SPO. The Bit Counter (BC) is incremented by 1 when the BTC counter = 284. For each BC count from 01 - 07 a serial data bit is transferred to the SPO. When BC = 10 and BTC = 284 is true, the next character is shifted to the output position of the MOS Register and the cycle repeats. If the last character is sensed by the Flag bit the last character is serially transferred to the SPO and upon completion (BC10 & 284CP) the Count F/F is reset thru disabling the BTC counter. BC & BTC are set to zero and the Service Request F/F is set. Exit to STC 18.
STC 18	Send Reference Address Byte 1 to the Processor. Reset SRF. Shift MOS right by 1 and Increment BCNT by 1.
STC 19	Send Reference Address Byte 2 to the Processor. Shift MOS right by 1 and Increment BCNT by 1.
STC 20	Send REference Address Byte 3 to the Processor. Shift MOS right by 1 and Increment BCNT by 1.
STC 21	Send Result Descriptor (Byte 1) to Processor.
STC 22	No Action
STC 23	Send Result Descriptor (Byte 3) to the Processor. Exit to STC 01.

SIMPLIFIED FLOW OF TEST OPERATION

STC 01	The Control in the quiescent state is at STC = 01. Assuming the SPO control is the channel designated the OP-Code (Test) is gated from the EXCH bits 00 through 07 to the OP-Register. The Variant bit indicating either Test and Wait for ENQ Key or Test and Don't Wait is also set in the Variant Register.
STC 02	No action
STC 03	No action
STC 04	No action
STC 05	No action
STC 06	No action
STC 07	Receive the Reference Address (Byte 1) in the Input Register. Shift MOS right by 1 and increment the Byte Counter (BCNT) by 1.
STC 08	Receive the Reference Address (Byte 2) in the Input Register. Shift MOS right by 1 and increment the Byte Counter (BCNT) by 1.
STC 09	Receive the Reference Address (Byte 3) in the Input Register. Shift MOS right by 1 and increment the Byte Counter (BCNT) by 1.
STC10 SC=06	Check to be sure all control keys are clear.
STC 10 SC = 00	Right justify the Reference address in the MOS Register. Exit to STC 18 and set SRF if VAR/ is true which indicates Don't Wait for the ENQ Key to be depressed. If VAR is true then "Wait" for the ENQ to be depressed.
STC 18	Send Reference Address Byte 1 to the Processor. Reset SRF. Shift MOS right by 1 and Increment BCNT by 1.
STC 19	Send Reference Address Byte 2 to the Processor. Shift MOS right by 1 and Increment BCNT by 1.
STC 20	Send Reference Address Byte 3 to the Processor. Shift MOS right by 1 and Increment BCNT by 1.
STC 21	Send Result Descriptor (Byte 1) to Processor.
STC 22	No Action
STC 23	Send Result Descriptor (Byte 3) to the Processor. Exit to STC 01.

SIMPLIFIED FLOW OF PAUSE OPERATION

STC 01	The Control in the quiescent state is at STC = 01. Assuming the SPO control is the channel designated, the OP-Code (PAUSE) is gated from the EXCH (bits 00 thru 07) to the OP-Register.

STC 02	No action
STC 03	No action
STC 04	No action
STC 05	No action
STC 06	No action
STC 07	Receive the Reference Address (Byte 1) in the Input Register. Shift MOS right by 1 and increment the Byte Counter (BCNT) by 1.
STC 08	Receive the Reference Address (Byte 2) in the Input Register. Shift MOS right by 1 and increment the Byte Counter (BCNT) by 1.
STC 09	Receive the Reference Address (Byte 3) in the Input Register. Shift MOS right by 1 and increment the Byte counter (BCNT) by 1.
STC10	SC = 06 Check to be sure all Control Keys are clear.
STC 10	SC = 00 Right justify the MOS Register. When BCNT 100 is true, set the Count F/F and exit to SC 01.
STC 10	SC = 01 With the Count F/F set at SC 00 the Bit Time Counter (BTC) is counted to 284 with each 32 usec clock pulse. When BTC = 284, the "pause" is complete and the Count F/F is reset. With the Count F/F reset, the Service Request F/F (SRF) is set and exit is to STC 18.
STC 18	Send Reference Address Byte 1 to the Processor. Reset SRF. Shift MOS right by 1 and Increment BCNT by 1.
STC 19	Send Reference Address Byte 2 to the Processor. Shift MOS right by 1 and Increment BCNT by 1.
STC 20	Send Reference Address Byte 3 to the Processor. Shift MOS right by 1 and Increment BCNT by 1.
STC 21	Send Result Descriptor (Byte 1) to Processor.
STC 22	No Action
STC 23	Send Result Descriptor (Byte 3) to the Processor. Exit to STC 01.

Functional Detail

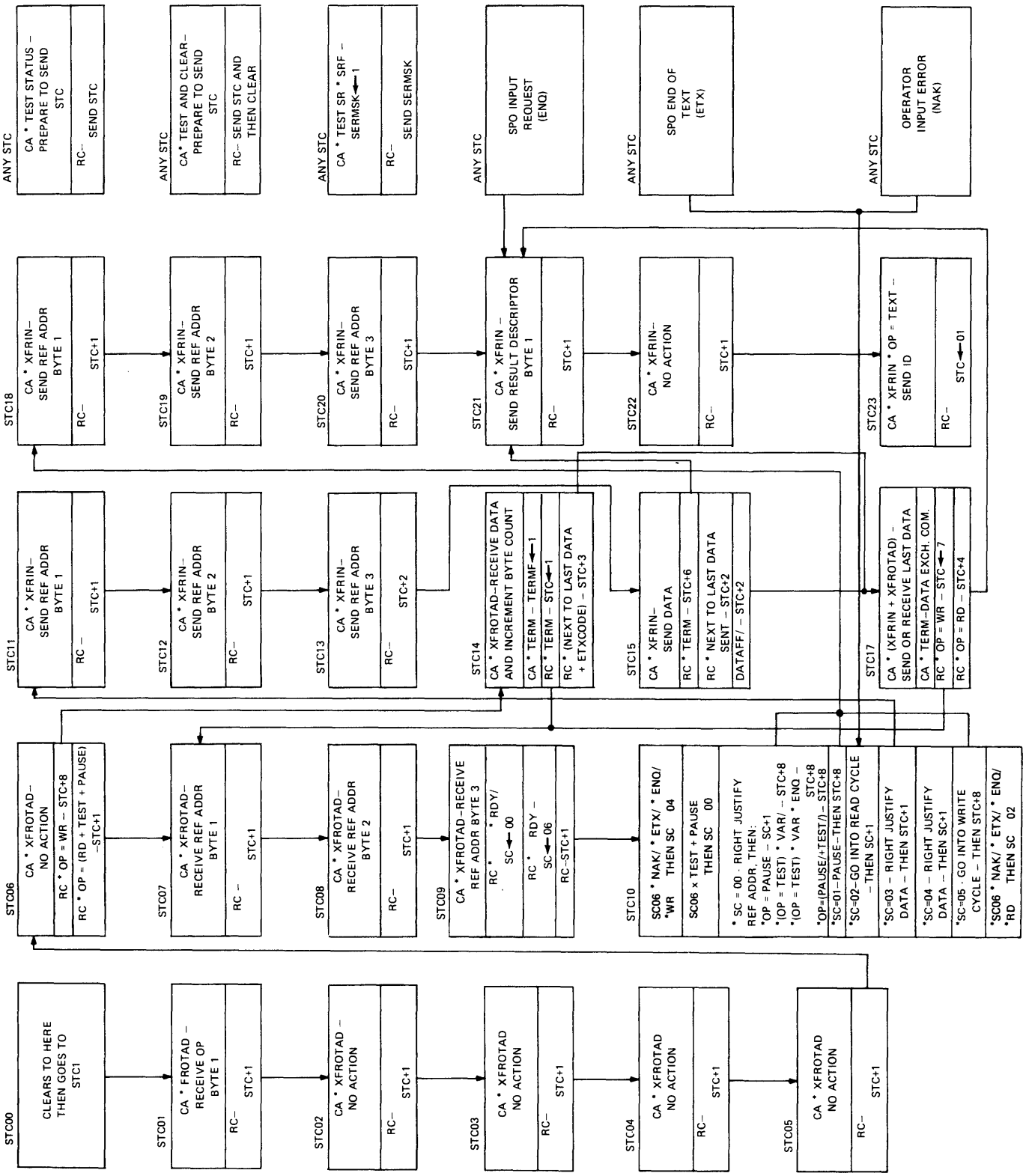


Fig. II-13 BASIC FLOW CHART

DETAILED SPO CONTROL FLOW

STC = ANY

CHAF 0	RC	Reset the Channel Active Flip-Flop.
BUF (I+1) ← BUFI BUF ← IR	SHF ← 1	During each shift sequence of the 100 bit MOS Register, shift each bit right 1 and accept the Input Registers (IR) contents. Note that the 100 bit MOS Register is 8 bit's high.
IOS	CHAF	With the Channel Active flip-flop set, I/O Send is true. IOS is sent to the Distribution Card in the I/O Base and the Subdistribution Card in a I/O Base extension if applicable to enable sending Control data on the 24 bit EXCH to the Processor via the I/O Bus. CHAF is true during the phase B portion of a two phase cycle.
EXCH ← SERMSK	TSR * SRF	If the command sent during CA time is Test Service Request and the SPO Control requires service by the Processor which is indicated by SRF, then gate the Service Req. Mask to the EXCH line (00 thru 15) which is applicable for the SPO Control.
NAKF ← 1 ETXF ← 1	NAK	If the Operator's Negative Acknowledgement Key on the Keyboard is depressed, set the NAKF flip flop and the End of Text Flip-Flop.
ETXF ← 1	ETX	Depressing the ETX Key sets the ETXF flip-flop.
ENQF ← 1	ENQ	Depressing the ENQ Key sets the ENQF flip-flop.
PH2 ← 0 P1 ← 1	SHF ← 1 * P1/ * PH1/ * P3	SHF ← 1 true indicates a shift is to occur in the 8 x 100 bit MOS Register. P1/, PH1/, & P3/ true indicates the quiescent or idle state of the Phase Counter. Setting P1 and resetting PH2 is the start of a shift sequence.
P1 ← 0	P1	Reset P1 and set PH1 when P1 is true.
PH1 ← 0 P3 ← 1	PH1	Reset PH1 and set P3 when PH1 is true.
P3 ← 0 PH2 ← 1 BCNT+1	P3	Reset P3 and set PH2 when P3 is true. This ends the shift sequence. The BYTE Counter is upcounted by 1 as the shift sequence indicates another BYTE of information has been shifted into the MOS Register.
EXCH ← STC	CHAF * TSR/	The status count of the SPO Control is gated to the EXCH lines 1 thru 20 if this is not a Test Service Request.
EXCH ← ID EXCH ← CHPL	CHAF * (TSTS + CLTS)	When the Channel Active flip-flop is set when either the command is TEST STATUS or CLEAR & TEST STATUS, gate the Channel # ID to EXCH bits 2, 3, & 5 and gate Channel present to EXCH bit 7.

Functional Detail

From STC = ANY

ODLS	SC2+5/ +(SC02*IDLC) +BC8-10 +SC05*SPRSDQ	ODLS true (-8 volts) energizes the selector magnet in the SPO Device. When the Sub-Counter is not set to either 2 or 5, ODLS remains at -8V. When the Sub-Counter is equal to 2 and IDLC is true a Read SPO operation is taking place and a MARK or data bit is present. During BC = 8 thru 10 in either a read or write operation, the parity and 1st and 2nd stop bits are either received or sent, ODLS is at -8v. During SC05 * SPRSDQ time, a write operation is indicated and a data bit or MARK is being transmitted to the SPO.
STC = 00		
STC+1		STC = 00 always goes to STC = 01
STC = 01		
BCNT←00 OPREG←EXCH	CA * CH * XFROTAD	If the command received on the EXCH bits 22 thru 20 is equal to 0 1 0, then a Transfer Out command or cycle type is present. CH indicates the channel designated to receive the command is the channel # of the SPO Control. Reset the BYTE Counter to zero and gate the OP-Code on the EXCH bits 05 thru 07 to the OP-Register.
STC+1	RC * CHAF *	When RC (Response Complete) is received, the CHAF flip-flop is set and the type of command is Transfer Out, upcount the status counter by 1.
STC = 02		
STC+1	RC * CHAF * XFROTA.1	Upcount the Status Counter by 1. No other action during STC = 02.
STC = 03		
STC+1	RC * CHAF * XFROTA	Upcount the Status Counter by 1. No Action.
STC = 04		
STC+1	RC * CHAF * XFROTA	Upcount the Status Counter by 1. No other Action.
STC = 05		
STC+1	RC * CHAF * SFROTA	Upcount the Status Counter by 1. No other Action.
STC = 06		
XLTFS←1	CA * VAR/ * (READF+WRITEF)	VAR/ true indicates the EXCH bit 04 received with the OP-Code at STC = 01 is false. EBCDIC Translation is designated. This has significance only if the OP-Code received is either Read or Write. A to E, Read; E to R, write.
STC+8	RC * CHAF * XFROTA * WRITEF	If the OP-Code is Write, then exit to STC = 14 STC = 14

Functional Detail

From STC=06

STC+1	RC * CHAF * XFROTA * WRITEF/	Exit to STC = 07 if the OP-Code is READ, TEST, or PAUSE.

STC 07

STC = 07 ← STC = 14 + STC = 17 + STC = 06

IR←EXCH	CA * CH * SFROTAD	Accept Byte 1 of the Reference Address on EXCH bits 00 thru 07. Store in IR.
STC+1 SHF←1	RC * CHAF * XFROTA	Upcount the Status Counter by one and initiate a shift right by 1 of the 8 x 100 MOS Register. This effectively shifts Byte 1 of the Reference Address into the shift Register. Refer to STCXX logic.
STC+1 SHF←1	RC * CHAF * XFROTA	Upcount the Status Counter by one and initiate a shift right by 1 of the 8 x 100 MOS Register. This effectively shifts Byte 1 of the Reference Address into the shift Register. Refer to STCXX logic.
BCNT←00	RDYF/	If the SPO is Not Ready, The Byte Counter is reset to 0 to insure the MOS Register is shifted properly. Note that this has Significance only if Write OP is true, in which case the MOS Register will already contain data. Specifically the Reference Address. If Write OP is true, entrance is made from either STC14 or STC17.

STC = 08

IR←EXCH	CA * CH * XFROTAD	Accept Reference Address Byte 2.
STC+1 SHF←1	RC * CHAF * XFROTA	Upcount the Status Counter by one and initiate a shift right by 1 of the MOS Shift Register. Bytes 1 & 2 of the Reference Address are in the left most Byte positions of the MOS Register (after the shift occurs).

STC = 09

IR←EXCH	CA * CH * XFROTA	Accept Reference Address Byte 3.
SHF←1 STC+L	RC * CHAF * XFROTA	Upcount the Status Counter by one and initiate a shift right by 1 of the MOS Register. Bytes 1, 2, and 3 are in the left most Byte positions of the MOS Register (after the shift occurs).
SC←0	STC≠10	Sequence Counter is set to zero any time the Status Count ≠ 10. Actually SC is in D-Set Mode.
SC←06	RC * CHAF * XFROTA *READF	If the SPO is Ready, set the Sequence Counter to 6.

Functional Detail

STC10*SC06	FROM STC=09	
STC = 10 * SC = 00	FROM STC=10 * SC06	(TEST, PAUSE, READ & Not Ready, or Write & Not Ready)
SHF←1	BCNT100/	STC10*SC=00 true indicates either the TEST OP, PAUSE OP, READ OP * Not Ready or the WRITE OP * Not Ready. The MOS Register is shifted right until BCNT = 100.
SHF←0	BCNT100	MOS Register is right justified, disable shift right by 1 (SHF←1).
SC+1 COUNTF←1	SC00*BCNT100* PAUSEF	If this is a Pause Op, when BCNT = 100, increment the Sequence Counter by one and set the Count Flip-Flop. With the Count F/F set, the Bit Time Counter is in the Add Mode and is incremented by 1 with each 32 μs clock pulse until equal to 284. When equal to 284, the pause is complete. The pause is approximately 9.08 ms 284 x 32 = 9076 μs or 9.08 ms.
STC+8 SRF←1	BCNT100* ((PAUSEF/+TESTF/) +TESTF*VAR/) + (TESTF*VAR*ENQF))	If the Op Code is not either TEST or Pause, exit to STC18, this indicates Read or Write Op and the SPO not ready. If the OP Code is Test and the Variant bit is not set, the results are stored immediately, exit to STC18. If the Op Code is Test and Wait (Variant bit set), then wait until the ENQ key is depressed and then exit to STC18 to store the results. The Service Request F/F is set which indicates the shift is complete and the SPO Control needs service by the Processor.
		STC = 18 →
STC=10*SC=01		"PAUSE OP Only"
COUNTF←0	BTC=284*32CP	Reset the Count F/F when the pause is complete (9.08ms).
STC+8 SRF←1	PAUSOS/	PAUSOS/ is the reset output of the COUNT Flip-Flop. Exit to STC18 and set the Service Request Flip-Flop.
		← STC = 18
STC=10*SC=02	STC=10*SC=06	"READ OP Only"
COUNTF←1 IR←0	IDLC/*32CP* PAUSOS/	IDLC/ when true indicates a key on the key board has been depressed. Although IDLC/ is true for each SPACE received during the transmission of one character from SPO, the START pulse received is the only pulse which has significance here. Note that PAUSOS/ must also be true. The Count F/F is set to start the Bit Time Counter. The BTC is used to synchronize the incoming data bits from the SPO with the Control. The Input Register is cleared as an initial clearing before receiving data from the SPO.
SC←02 LTONC←1	ETX/*ENQ/*NAK/ *READ	SC06 is entered to assure that the operator has taken his finger off the three control keys. LTONC turns on the SPO Ready Light.
SC←04	ETX/*ENQ/*NAR/ *WRITE	
SC←00	TEST + PAUSE	

Functional Detail

From STC = 10 * SC = 02

BC+1	BTC = 284	When the Bit Time Counter = 284, increment the Bit Counter by 1. The Bit Counter is used to count the start, data, parity & stop bits from the SPO. BC is initially set to zero and is incremented by 1 until equal to 10 when it is again reset to 0. This is true for Write Operations only. During Read SPO operations the Bit Counter counts only from zero to 1 when it is reset to zero.
BC←0 SHF←1 COUNTF←0	BC8CY	BC8CY indicates the Bit Counter is equal to 7, and the Bit Time Counter is equal to 284 which indicates the last data bit from SPO has been strobed into the Input Register. The BC Counter is reset to zero in preparation of the next character to be read from SPO. SHF←1 shifts the character assembled in the IR into the MOS Register and the COUNTF F/F is reset to disable increment the BTC counter with each 32cp. until the next START bit from the SPO is received.
EXCEDF←1	IDLC/*BCNT78	The EXCEDF is set if the Byte Counter is equal to 78, and another START bit is received from SPO. BCNT78 indicates 75 character from SPO are assembled in the MOS Register in addition to the 3 Bytes of the Reference Address.
IR7←FLAG	EXCEDF	Enter Flag bit in Input Register's 7 bit position if EXCEDF is true.
SC+1	BC8CY*EXCEDF	Exit to SC03 to right justify the data in the MOS Register. EXCEDF true indicates 75 characters plus the 3 Bytes of the reference address are assembled in the MOS Register. BC8CY indicates the Bit counter is at 7 with a carry, effectively this indicates the 76th key on the keyboard has been depressed.
IR←ETXCODE SHAREF←1 IR7←FLAG	ETXF * NAKF/	Set IR bits 7, 0 & 1 if ETX key has been depressed. IR bit 7 is the Flag bit. SHAREF is set to increment the SC by 1 and generate a Shift of the MOS Register.
LTONC←0	ETXF + EXCEDF	Turn off the SPO Ready Lite if either condition is true.
SHAREF←1 IR7←FLAG	ETXF	Depressing the NAK key on the keyboard sets both the NAKF and ETXF flip-flops. The flag bit is set to indicate the last character will be all zeros. SHAREF set is used to increment the SC count by 1 and shift the MOS Register right by 1.
SHAREF←0 SC+1 SHF←1	SHAREF	SHAREF true resets itself and is used to shift the MOS Register and increment the SC count by 1.
DATAF←1	IDLC/	IDLC/ indicates at least 1 character was typed.
STC=10*SC=03		"Read Op Only"
SHF←1	BCNT100/	SHF←1 remains true until the MOS Register is right justified (BCNT = 100)

From STC = 10 * SC = 03

SHF ←0 STC+1 SRF ←1	BCNT100	BCNT100 indicates the MOS Register is right justified, exit to STC11 and set the Service Request Flip-Flop. STC = 11

STC10*SC06

STC=10*SC=04		"Write OP Only"
SHF ←1	BCNT100/	SHF ←1 remains true until the Byte Counter equals 100 (MOS Register is right justified).
SHF ←0	BCNT100	Disable SHF ←1 as data in MOS Register is right justified.
SC+1 COUNTF ←1	BCNT100*32CP	Exit to SC05 to start sending data bits for each character assembled in MOS to the SPO. Bit Time Counter is started with COUNTF set.
STC=10*SC=05		"Write OP Only'
BC+1	284CP	Increment the Bit Counter with each 284cp pulse from the Bit Time Counter.
SHF ←1 BC ←0	BC10*284CP	When the Bit Counter equals 10 and the 284cp pulse from the Bit Time Counter is true, one complete character has been transferred to the SPO. The MOS Register is shifted right by 1 to place the next character to be transferred to the SPO at the output buffer position of the MOS Register. Reset the Bit Counter to sequence sending the next character to the SPO.
SRF ←1 STC+8 COUNTF ←0	BC10*284CP* FLAG1	FLAG1 indicates the End of Text Code is sensed at the output bit position of the MOS Register (Buffer 7); FLAG1 might also be true as the result of receiving the TERM command during STC14. The Service Request F/F is set and exit is made to STC18. The COUNTF F/F is reset to disable the counting of the Bit Time Counter.

STC10*SC03

STC=11		"Read Op Only"
EXCH ←BUF100	CHAF*XFRIN	Send Reference Address Byte 1 on Exchange lines 00 thru 07 to the Processor via the I/O Bus.
SHF ←1 STC+1	RC*CHAF* XFRIN	Shift Byte two of the Reference address to the output position of the MOS Register and exit to STC12.
SRF ←0	CHAF*XFRIN	Presence of the XFRIN command to the SPO Control will set the CHAF Flip-flop. The Service Request has been acknowledged by the Processor; therefore, reset SRF.
STC =12		"Read OP Only"
EXCH ←BUF100	CHAF*XFRIN	Send Reference Address Byte 2 to the Processor.
SHF ←1 STC+1	RC*CHAF* XFRIN	Shift Byte 3 of the REference Address to the output bit position of the MOS Register and exit to STC13.

From STC = 12

STC = 13

EXCH←BUF100	CHAF*XFRIN
SHF←1 STC+2	RC*CHAF* XFRIN

"Read OP Only"

Send Reference Address Byte 3 to the Processor.

Exit to STC15 to send Character data to the Processor. Shift the MOS Register right by 1 to place the first character read from SPO at the output position of the MOS Register. The data in the MOS Register is transferred to the Processor, one character at a time.

STC = 15 →

STC = 06 ←

STC = 14

IR←EXCH	CA*CH* XFROTAD
IR7←FLAG	CA*CH*ETXCODE
IR7←FLAG	CHAF*TERM
SHF←1	RC*CHAF*TERM
SHF←1	RC*CHAF* XFROTA
STC+3	RC*CHAF* XFROTA*BCNT73
STC←7	RC*CHAF*TERM
STC+3 DATAFF←1	RC*CHAF* XFROTA*IR7

"Write OP Only"

Receive the data from the Processor and set the same in the Input Register. EXCH bits 00 thru 07 will transfer one character of information.

Set the flag if the End of Text Code is received.

If the Command received is the TERM command, the flag is set to indicate there is no more data to be transferred.

Shift (zeros) and IR7 into MOS Register.

Shift data (characters) into the MOS Register.

When the Byte Counter is equal to 73, it indicates 74 characters have been transferred to the MOS Register. Exit to STC17 to receive the last (75th) character from the Processor.

STC = 17 →

If the command received is the TERM command, exit to STC07 to receive the Reference Address Byte 1.

STC = 07 →

IR7 indicates the End of Text Code has been received, exit to STC17 but ignore next character if sent.

STC = 17 →

STC = 13 ←

STC = 15

STC+2	FLAG1*FLGFF
FLGFF 1	RC * CHAF* XFRIN

"Read OP Only"

FLAG1 indicates the Flag output bit position of the MOS Register is sensed. This is Buffer 7 and indicates the MOS Register has been shifted right by 1 until this bit is sensed. This is the result of setting IR7 during the read operation at STC10*SC02. The last character read is transferred to the EXCH when PH2 is true. Exit to STC17 to transfer last character to the Processor. If FLAG1 is true because the ETX key was depressed, then the ETX Code is sent at STC17. If the NAK key was depressed, only the Flag Bit is sent. If an attempt to key in a 76th character from SPO occurred, then the 76th character key-ed is sent along with the flag bit.

STC = 17 →

From STC = 15

EXCH ← BUF100	CHAF*XFRIN	Transfer character data to the Processor until FLAG1 is true.
SHF ← 1	RC*CHAF*XFRIN	Shift next Character in MOS right by 1.
STC+6	RC*CHAF*TERM	If the command sent during CA time is TERM, then exit to STC21 and send the Result Descriptor. STC = 21 →
STC+2	DATAF/	Go to STC = 17 if no data was read from SPO at STC10. STC=17 →

STC=14 + STC=15 ← "Read or Write OP Code"

STC = 17		If the command received at this STC is TERM, then the FLAG is set in IR7.
SHF ← 1	RC*CHAF* TERM*DATAFF/	DATAFF/ true indicates a Write operation is in progress, the end of text code was not received at STC14. Entrance to STC17 in this case is because the BCNT count was 73. The flag bit in IR7 is shifted into the MOS Register. TERM indicates the TERM command. If the Operation is Write, then TERM indicates no more data will follow from the Processor. If the operation is Read, then TERM indicates that the Processor does not want any more read data from the SPO.

STC = 17		"Read OP Only"
EXCH ← BUFF100	CHAF*XFRIN	The XFRIN command will gate the last character in the MOS Register to the Processor. Refer to STC15 for details of the character data sent.
STC+4	RC*CHAF*XFRIN	If this is a XFRIN command then exit to STC 21 and send the Result Descriptor.
STC+4	RC*CHAF* TERM*WRITE/	WRITE/ indicates the operation if Read SPO, however if this command is TERM, then the last character is not sent and the flow exits to STC21 to send the Result Descriptor.

STC = 17		"Write OP Only"
IR ← EXCH IR7 ← FLAG	CA*CH*XFROTA	If this is a transfer out command, then receive the last character from the Processor. Set flag to indicate the last character.
STC ← 7	RC*CHAF* TERM*WRITE	If the command sent is TERM, then exit to STC07 to receive the Reference Address.
STC ← 7	RC*CHAF*XFROTA	If this is a transfer out command, then exit to STC07 to receive the Reference Address.

From STC = 17

SHF←1	RC*CHAF*XFROTA *DATAFF/	The flag bit set in IR7 during CA time is shifted into the MOS Register if not done at STC14. Refer to setting DATAFF at STC14.

From STC=10

STC = 18 — "ALL OP Codes except Read & Ready"

EXCH←BUF100 SRF←0	CHAF*XFRIN	Send Reference address Byte 1 to the Processor and clear Service Request.
SHF←1 STC+1	RC*CHAF*XFRIN	Shift Reference Byte 2 to the output position of the MOS Register and upcount the STC by 1.

STC = 19

EXCH←BUF100	CHAF*XFRIN	Send Reference Address Byte 2 to the Processor.
SHF←1 STC+1	RC*CHAF*XFRIN	Shift Reference Address Byte 3 to the output position of the MOS Register. Increment the STC by 1.

STC = 20

EXCH←BUF100	CHAF*XFRIN	Send Reference Address Byte 3 to the Processor.
STC+1	RC*CHAF*XFRIN	Upcount the STC by 1.

STC = 21

EXCH←R/D	CHAF*XFRIN	Send the Result Descriptor on exchange lines 00 thru 07. Refer to R/D formal for conditions indicated.
STC+1	RC* CHAF*XFRIN	Increment STC by 1.
XLTFS		Dis-enable translator chips if ON.

STC = 22

STC+1	RC*CHAF*XFRIN	Upcount the STC by 1.

STC = 23

EXCH←ID	CHAF*XFRIN*TESTF	If this is a Test OP, then send the CH # ID to the Processor on EXCH bits 2, 3, & 5.
STC←1	RC*CHAF*XFRIN	Exit to STC01, operation complete.
ENQF←0		Several Flip-Flops are reset in addition to the ENQF Flip-Flop.

Adjustments

SECTION IV

There are no adjustments for the SPO control.
Refer to I/O Base Section IV for clock adjustments.
Refer to SPO Control Section VI for determining the control channel number.

Maintenance Procedures

INTRODUCTION

The purpose of this section is to provide directions and aids in maintaining the SPO Control.

PREVENTIVE MAINTENANCE

There is no preventive maintenance for the SPO Control. Refer to teletype manual for SPO PM.

SPECIAL MAINTENANCE TOOLS REQUIRED

SPO Test Routines
B 1700 Field Card Tester
Tektronix 453A Oscilloscope or equivalent
Tripplet 630 VOM or equivalent

MAINTENANCE CONCEPT

B 1700 controls are soft controls. No offline capability is built into the control. The B 1700 Maintenance concept is centered around the use of test routines used in conjunction with the Field Card Tester. Hardware testpoints are provided for conventional troubleshooting.

TEST ROUTINES

CONFIDENCE ROUTINE

SPO confidence routine tests the following:

1. Not ready condition
2. Types all characters using EBCIDIC translation
3. Types all characters from ASCII without translation
4. Echo Test using EBCIDIC Translation
5. Echo test without translation
6. Checks Input control keys (ETX, NAK, ENO)
7. Ripple Test using EBCIDIC translation
8. Ripple test without translation

HOW TO LOAD TAPE

1. Place Processor in the MTR mode and Ready the SPO
2. Insert SPO confidence routine into the Cassette Drive
3. Clear and Depress START
4. After the cassette halts, clear and again depress START
5. After cassette halts, place the processor in the RUN mode and again depress START.

RUN INSTRUCTIONS

1. The SPO Confidence Routine Listing gives run instructions.
2. The SPO prints out special instructions as the program proceeds.

RESULTS

Refer to Test Procedures to analyze the failure.

I/O DEBUG ROUTINE

GENERAL

Figure V-1 is a breakdown of the Processor to I/O flow. The I/O Debug Routine is a basic routine that follows the path shown in the figure. This routine may be used for any I/O Control. The OP Code and control channel number have to be manually loaded. The instructions on the program listing give the FA value where these commands are placed.

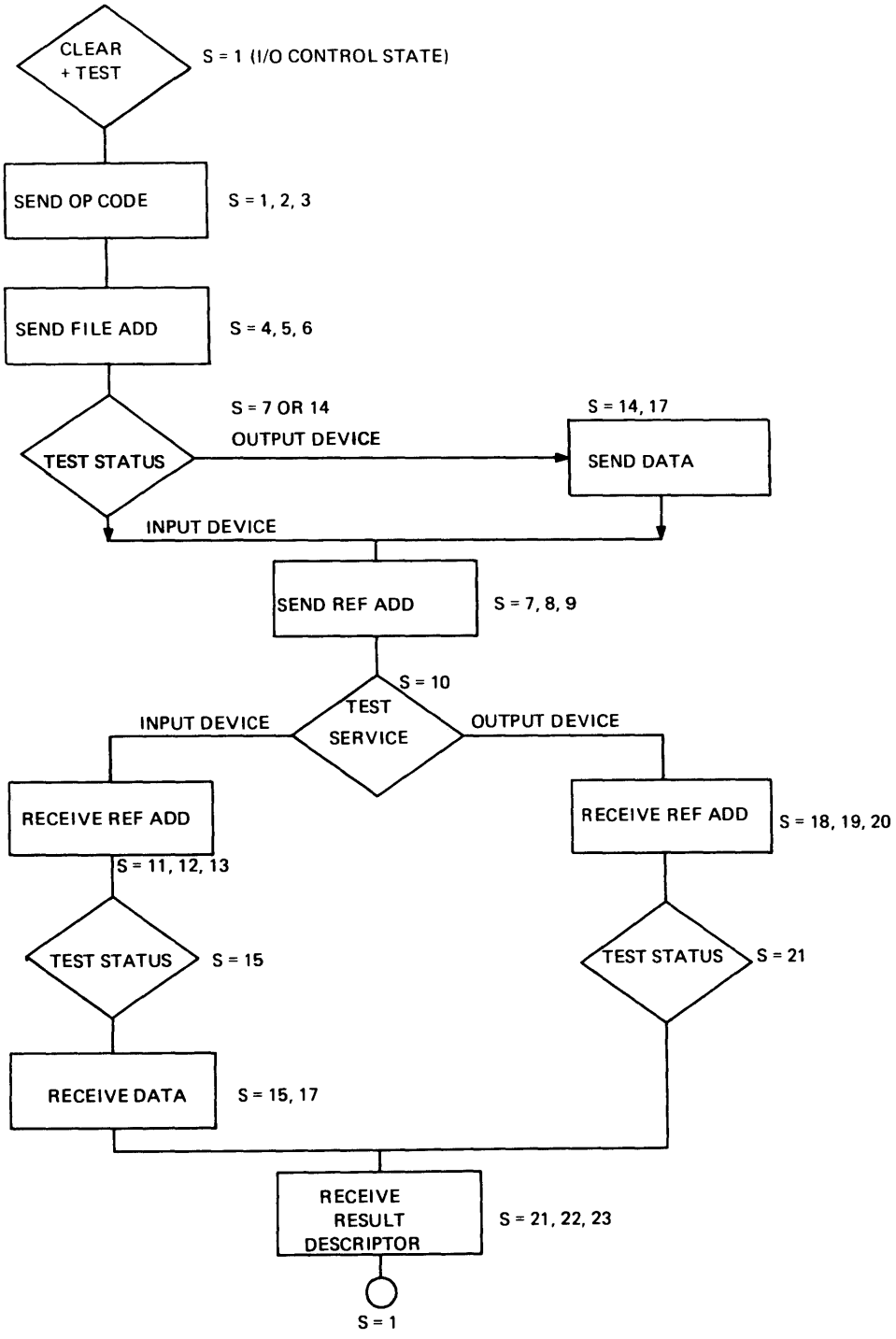


Fig. V-1 PROCESSOR TO I/O FLOW

STEPPING

By stepping this program 1 micro at a time the Field Engineer can observe Hardware testpoints and determine the internal SPO control operation.

Each time this program sends out a basic command to the I/O it will read in the status of the 24 exchange lines to the L Reg. By displaying L at the proper time the F.E. can observe what status count the control is at and what data is returned to the processor. By looking at T Reg. at the proper time the Field Engineer can observe the commands and data sent to the control.

USING HALTS

Figure V-1 shows the basic subroutines within the boxes. For example, send OP Code is a subroutine. The Debug program has no-op micros placed between subroutines and within certain routines. These allow the Field Engineer to manipulate the program to his liking. For example, a halt could be put after the 1st byte of REF ADD has been transferred to the control. The Field Engineer could then check at the storage buffer in the control for this byte of data. Another example would be placing a halt after the first result Descriptor Byte is transferred in. The L Reg could then be checked for this data.

TEST PROCEDURES

SPO Control Troubleshooting should follow these basic steps.

VISUAL CHECKS (REFER TO SPO CONTROL SECTION VI)

1. Assure that the control has been loaded into a valid one card control slot
2. Assure that SPO cabling to control is proper
3. Assure that a channel jumper chip has been installed and that no two controls have the same channel number

RUN CONFIDENCE ROUTINE

1. Before running SPO confidence routine be assured that Processor and Memory are functioning properly. If necessary run the processor and memory confidence routines.
2. Run the SPO confidence routine (Refer to paragraph on Confidence Routine)

TYPE OF FAILURES FROM THE CONFIDENCE ROUTINE

1. Routine will not run
2. Not Ready Section fails
3. EBCIDIC write fails
4. ASCII write fails
5. Read EBCIDIC fails
6. Read ASCII fails
7. Input control keys not detected
8. Ripple EBCIDIC fails
9. Ripple ASCII fails
10. Confidence test passes

DECISION

1. If confidence test passed, attempt to recreate original problem.
2. For a failure. Proceed to the Field Card Tester.
3. Test card in Field Card Tester (Refer to B 1700 Field Card Tester Manual)
4. If problem is found and repaired, rerun Confidence Routine.
5. If card checks OK in tester or the problem cannot be resolved, go to next paragraph.

USE OF I/O DEBUGGING ROUTINE

This step involves the running of an I/O Debugging Routine. For operation of the I/O Debugging Routine refer to the paragraphs describing it.

Attempt to analyze the failure of the Confidence Routine and relate it to particular circuitry of the SPO Control.

For example if the EBCIDIC write failed the translator chips located at G7 and H7 should be checked along with their associated logic.

PROCESSOR TO I/O TRANSFER PROBLEMS

With problems involving processor to I/O transfers it is best to step the processor and observe hardware testpoints along with processor registers.

SPO CONTROL TO SPO TRANSFER PROBLEMS

For SPO Control to SPO data transfer problems first check the interface testpoints. Second, observe the Serial data in respect to the strobe pulse. In a read operation the strobe should fall in the center of the bit cell as shown in Figure V-4.

HARDWARE TESTPOINTS

SPO CONTROL CARD FRONTPLANE CONNECTORS

$X
Testpoints

A	STCT1 . . 1	I	SC+1 . . . 1	S	ODL 1
B	STC+2 . . 1	J	CT1 1	T	IDLC 1
C	STC+3 . . 1	K	CT2 1	U	RDYOFF . 1
D	STC+4 . . 1	L	CT4 1	V	LTON . . . 1
E	STC+8 . . 1	M	CT8 1	W	
F	STC 1	N	CT16 . . . 1	X	SPRSDQ . 1
G	STC 02 1	P	SCCT1 . . 1	Y	EX OR 1
H	SC-04 . . . 1	Q	SCCT2 . . 1	Z	
		R	SCCT4 . . 1		

#X
Testpoints

A	XFRIN . . 1	I	CLTS . . . 1	S	ORXC6 . . 1
B	XFRDTA 1	J	TSR 1	T	ORXC7 . . 1
C	WRITE . . 1	K	TERM . . . 1	U	NAKF . . . 1
D	TEST . . . 1	L	ORXC0 . . 1	V	ETXF . . . 1
E	PAUSE . . 1	M	ORXC1 . . 1	W	ENQF . . . 1
F	READ . . . 1	N	ORXC2 . . 1	X	EXCEDF . 1
G	VAR/ . . . 1	P	ORXC3 . . 1	Y	COUNT-1 . 1
H	TSTS . . . 1	Q	ORXC4 . . 1	Z	COUNT-0 . 1
		R	ORXC5 . . 1		

$Y
Testpoints

A	BYT01 . 1	I	P3 1	S	IR0 1
B	BYT04 . 1	J	PH2 1	T	IR1 1
C	BYT08 . 1	K		U	IR2 1
D	BYT32 . 1	L		V	IR3 1
E	BYT64 . 1	M		W	IR4 1
F	SHF 11	N		X	IR5 1
G	P1 1	P		Y	IR6 1
H	PH1 . . . 1	Q		Z	IR7 1
		R			

#Y

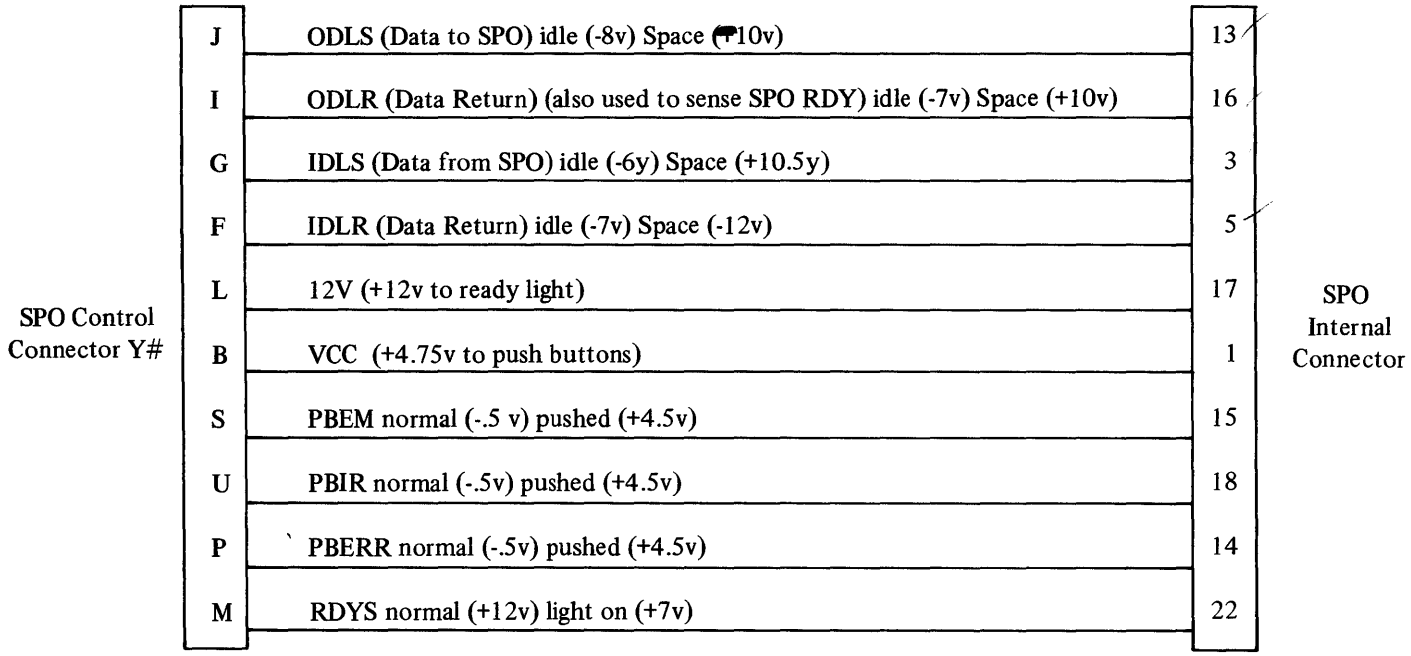
Interface Levels to SPO

A		I	ODLR . . . 1	S	ETX 1
B	4.75V . . 1	J	ODLS . . . 1	T	ETX/
C		K		U	ENQ 1
D		L	P12V 1	V	
E		M	RDYS . . . 1	W	ENQ/ 1
F	IDLR . . 1	N		X	
G	IDLS . . . 1	P	NAK 1	Y	
H		Q	NAK/ 1	Z	
		R			

Backplane

	0		A	1
	EXCH00 .0		B	EXCH01 .0
	EXCH02 .0		C	EXCH03 .0
	EXCH04 .0		D	
	EXCH05 .0		E	EXCH06 .0
	EXCH07 .0		F	EXCH08 .0
	EXCH09 .0		G	EXCH10 .0
	EXCH11 .0		H	EXCH12 .0
X Connector	EXCH13 .0		I	EXCH14 .0
	EXCH15 .0		J	
	EXCH16 .0		K	EXCH17 .0
	EXCH18 .0		L	EXCH19 .0
	EXCH20 .0		M	EXCH21 .0
	EXCH22 .0		N	EXCH23 .0
			P	
			Q	
			R	
	32VS . . .0		S	
			T	
			U	
			V	
	SCPM		W	
			X	
			Y	
	-12v 0		Z	

		A	-12v
		B	IOS 0
		C	CLRB. . .0
		D	
		E	RC 0
		F	CA 0
		G	SRF 0
		H	
Y Connector		I	
		J	
		K	
		L	+12V . . .0
		M	
		N	TESTER.0
		P	
		Q	
		R	
		S	
		T	
		U	
		V	
		W	
		X	
		Y	
		Z	



Conditions for interface measurements

1. Cable connected
2. Power on
3. SPO plugged in and in line operation
4. ODLS, ODLR, IDLS and IDLR must be observed on a scope. For this operation the SPO should be in the read mode and the lines observed while striking the space bar.
5. All other levels can be checked with a Tripplet 630 VOM.

Figure V-2

Maintenance Procedures

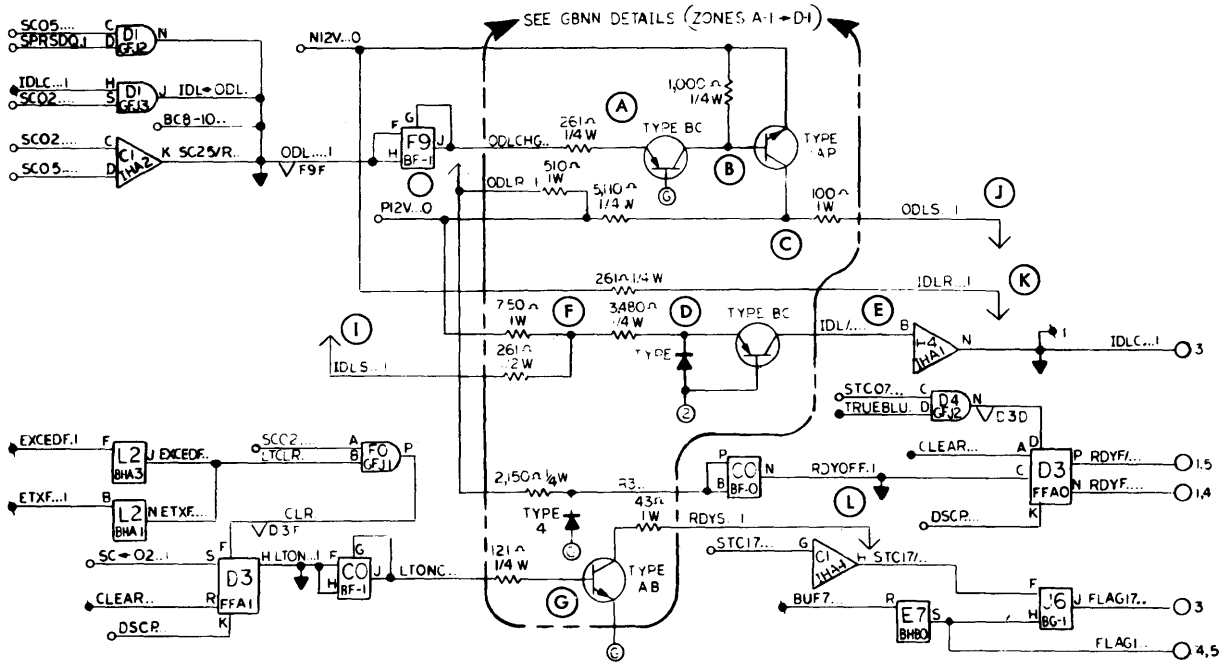


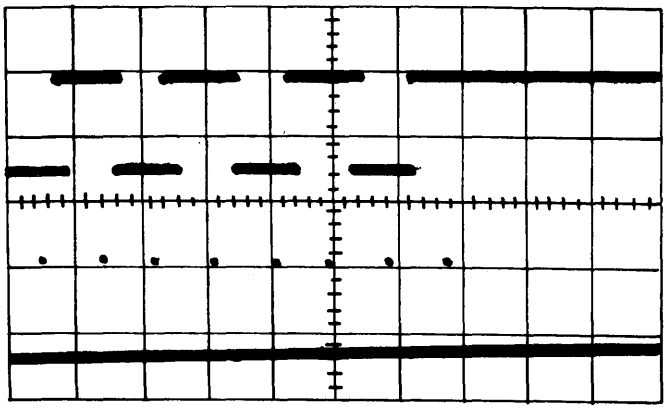
Fig. V-3 SPO INTERFACE TEST POINTS

TESTPOINT	WAVE FORM
A	+.8V / -.6V
B	-11V / -12V
C	+5V / -6V
D	5.5V / 4V
E	+1.6V / -2V
F	5.2V / 4V
G	LIGHT OFF / +.8V LIGHT ON / -.8V
H (ODLR)	+10V / -7V
I (IDLS)	+11V / -6V
J (ODLS)	+10V / -8V
K (IDLR)	-7V / -12V
L (RDYS)	+12V / LIGHT OFF / +7V LIGHT ON

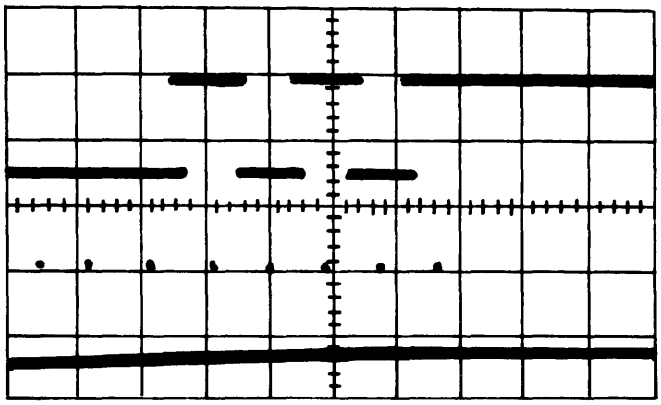
FOR MEASUREMENTS
SPO IS IN READ MODE
DEPRESS SPACE BAR

TABLE V-1

Letter U
and Strobe



Letter T
and Strobe



SPO is in read mode
Set up Scope as follows:

Top Trace Testpoint Chip D1 pin N (ODL....1)
Bottom Trace Testpoint Chip C2 pin K (STROBE..)
Sync Scope on Top Trace
2V/cm Vertical
10 milliseconds/cm horizontal

Fig. V-4

Installation Procedures

INTRODUCTION

This section provides information to install and check out a SPO Control.

LOGIC PREPARATION

The processor communicates with an I/O Control by addressing the controls unique channel number. During a service request by a control the channel is used to determine priority in the event two or more controls need service. Priority is determined by high order number first. Channel number for a particular control will vary depending on system configuration.

CHANNEL NUMBER ADJUSTMENT

Jumper chip F8 should be wired to reflect the desired SPO channel number. Refer to I/O Base Section VI for typical system control numbers and an example for wiring the jumper chip. Jumper chip K-9 is for wiring in a channel number from 8 to 15. At present only 8 channels (0-7) are used.

PHYSICAL INSTALLATION

The SPO Control Card will be mounted in the I/O Base and cabled to the I/O Adapter Panel. The SPO is located on the table top to the left or right of the console, depending upon the system configuration. The SPO is cabled to the I/O Adapter Panel.

CARD LOADING

The SPO Control is contained on one card. This card may be installed in any 1 or 2 card control slot of the I/O Base. Refer to I/O Base Section VI for definition of these control slots.

PERIPHERAL TO I/O ADAPTER PANEL CABLING

The SPO cable is routed to the rear of the table top, through the hole in the rear skin assembly. The edge connector is installed on the I/O adapter panel. The extra cable length must be coiled up and tied neatly, then placed near the adapter panel.

CONTROL TO I/O ADAPTER PANEL CABLING

Route the SPO Control Adapter cable from the frontplane connector #Y straight down to the trough at the bottom of the I/O base. From the trough drop the cable straight down and into the table assembly. Route over and up to the I/O Adapter panel. Plug the paddle board into the SPO cable edge connector. The connector is keyed and therefore can only be inserted in one way.

ELECTRICAL INSTALLATION

AC POWER

Route the SPO AC Power Card to the rear of the table top and through the hole in the rear skin assembly. Drop cable straight down and plug into standard power receptacle on the AC Power Distribution Assembly.

PERIPHERAL/CONTROL CHECKOUT

Upon completion of the SPO Installation run the SPO confidence routine and associated test routines to assure proper operation.