MEMORANDUM

THE Bendix CORPORATION

BENDIX COMPUTER DIVISION

TO: Whom It May Concern FROM: Raymond Fillingim

SUBJECT: Central Processor Manual Erratum DATE: January 24, 1963

We realize that the accompanying errata listing is rather lengthy. Also at some future date the pages incorporating errors will be reprinted. Therefore, the following method of handling these errata is suggested.

Instead of penciling in all of the corrections, you might prefer to simply mark the pages in error (being sure these marks are distinctive enough that they will not be missed in subsequent references to these pages). These marks will then remind you to refer to the accompanying list for corrections.

Ray Fillingim

Raymond Fillingim

jk
Enc.

CENTRAL PROCESSOR MANUAL, VOL. I (BER 10622) ERRATUM

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i	Section 2.3, Page Location	Reads Should Read	2-11 2-10
vi	Figure No. Column, Between 4.2-6 and 4.3-1	Add	4.2-7*
vi	Bottom of Page	Add	*4.2-7 Transfer Paths of CD Register for Bootstrap Operation 4-17
viii	Figure No. 7.1-15, Description Column, 2nd Line	Reads Should Read	Figure 12.1-13 Figure 7.1-14
x	Table No. 2.3-1, Page Location	Reads Should Read	2-12 2-11
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CHAPTERS 1 THROUGH 8

PAGE	LOCATION		CORRECTION
2-6	Line 12	Reads Should Read	. . . PE register are set to zero . . . . . PE register are ignored . . .
2-8	Operation Column of Address Preparation Commands, 7th Formula	Reads Should Read	X + (ACC) → (OA) |X + (ACC)| → (OA)
2-8	Operation Column of Address Preparation Commands, 8th Formula	Reads Should Read	-X + (ACC) → (OA) |-X + (ACC)| → (OA)
2-8	Operation Column of Add and Subtract Commands, 7th Formula	Reads Should Read	X + (ACC) → (ACC) |X + (ACC)| → (ACC)
2-8	Operation Column of Add and Subtract Commands, 8th Formula	Reads Should Read	-X + (ACC) → (ACC) |-X + (ACC)| → (ACC)
2-8	Operation Column of Add and Subtract Tests Commands, 5th Formula	Reads Should Read	-X + (ACC) > 0 |-X + (ACC)| > 0

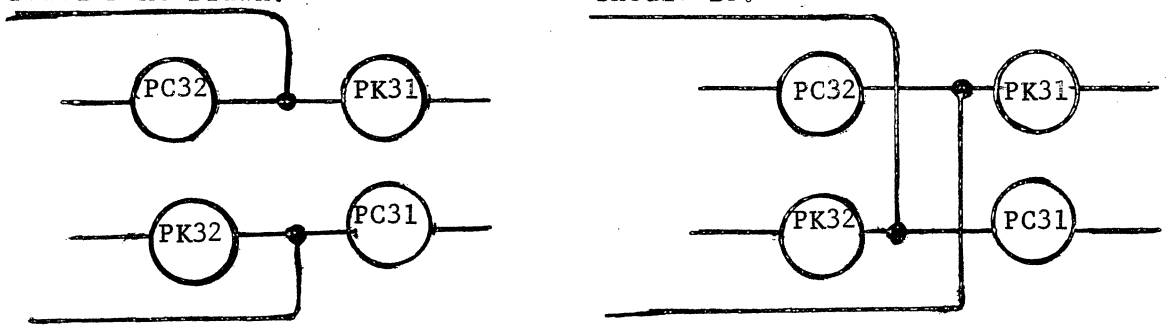
PAGE	LOCATION		CORRECTION
2-8	Operation Column of Add and Subtract Tests Commands, 8th Formula	Reads Should Read	X + (ACC) > 0 |X + (ACC)| > 0
2-8	Operation Column of Logic Tests Commands, 3rd Formula	Reads Should Read	31 X + (ACC) 0 > 0 31|X + (ACC)|0 > 0
2-8	Operation Column of Logic Tests Commands, 4th Formula	Reads Should Read	31 -X + (ACC) 0 > 0 31|-X + (ACC)|0 > 0
2-9	Note Under Register Operations, Last Line	Reads Should Read	*The CA register can be read only by an ERO or ERA opcode. *The CA register can only be used with an ERO or ERA opcode. The PE register can only be used with the LDR opcode.
2-9	Note Under Repeat Operations, Last Line	Reads Should Read	. . . for is met. . . . for is met or until the specified block length is reached.
2-10	Lines 23 and 24	Read Should Read	. . . location (1 through 63) to be operated on. . . . location (0 through 63) to be operated on.*
2-10	Bottom of Page	Add	*An I field of 00 in an Index Command specifies memory location 00000, and this location will be operated on by these commands. However, an I field of 00 as used with the general case of Operand Assembly indicates no index address is specified.
2-12	Line 6	Reads Should Read	. . . of the 63 index locations . . . . . of the 64 index locations . .
3-2	Line 8	Reads Should Read	. . . discussed in Part IV, . . . discussed in Volume II,
3-2	Line 21	Reads Should Read	. . . Chapter 12 of Part IV . . . . . . Chapter 12 of Volume II . .
4-2	Lines 1 and 2	Read Should Read	The MA register starts the memory cycle which brings the new command from memory and places it in the B At the start of a memory cycle the new command is brought from memory and placed in the B

PAGE	LOCATION		CORRECTION
4-2	Line 12	Reads	. . . register which starts the memory cycle which brings . . .
		Should Read	. . . register. The memory cycle now brings . . .
4-3	Line 16	Reads	. . . peripheral units, control . .
		Should Read	. . . peripheral units,* control. .
4-3	Bottom of Page	Add	*At the present time only the Central Processor is capable of receiving and acting upon interrupts. Therefore, with present equipment, the Central Processor will transmit interrupts to another Central Processor only.
4-6	Line 14	Reads	. . . locations 1 through 63) . .
		Should Read	. . . locations 0 through 63) . .
4-8	CD7 Column at Bottom ($\overline{9} \wedge \overline{8} \wedge \overline{6}$)	Add	1
4-8	CD Decoding $\overline{9} \wedge \overline{8} \wedge 7 \wedge \overline{6} \wedge 12 \wedge \overline{11} \wedge \overline{10}$	Reads	TIC 157
		Should Read	TLC 157
4-15	Line 1	Reads	. . . the least 2 bits . . .
		Should Read	. . . the least significant 2 bits . . .
4-31	Line 26	Reads	. . . Figure 4.3-2 it is seen . .
		Should Read	. . . Figure 4.4-2 it is seen . .
4-33	Table 4.4-2, Bit Position 3 of J Register	Reads	UWB
		Should Read	JWB
4-34	Figure 4.4-3, Immediate Right of ULA and ULB	Reads	DATA word
		Should Read	LOGIC word
4-34	Figure 4.4-3, Immediate Right of UDA and UDB	Reads	LOGIC word
		Should Read	DATA word
4-34	Figure 4.4-3, Between UWA, UWB and JWA, JWB JWC, JWD	Reads	OUTPUT INPUT Interrupt Requests
		Should Read	TRANSMIT RECEIVE Interrupt Requests
4-36	Line 12	Reads	. . . and Table 4.3-2.
		Should Read	. . . and Table 4.4-2.
4-38	Line 1	Reads	. . . is therefore forbidden.
		Should Read	. . . is therefore forbidden.*

PAGE	LOCATION		CORRECTION
4-38	Bottom of Page	Add	*A negative zero exponent in the PE register is not detected by the hardware. It therefore becomes the programmer's responsibility to avoid this condition.
4-39	Figure 4.4-6, Bottom	Reads	. . . necessary and sufficient to . . .
		Delete	. . . and sufficient . . .
5-1	Figure 5.1-1, Lower Right, Above D Register	Reads Should Read	B(L31)41D21 B(L21)41D21
5-3	Line 23	Reads	. . . double precision operation. . . .
		Should Read	. . . double precision operation.*
5-3	Bottom of Page	Add	*During index operations, the number to be stored is always shifted to zero exponent and truncated. Therefore, the EA(L21)B transfer, when used in an index operation, will always result in zeros being stored in 27B21.
5-4	Line 2	Reads Should Read	. . . operation is performed. . . . operation is performed.*
5-4	Bottom of Page	Add	*Bits 30 and 31 of the B register are reset during a store zero operation, but this is accomplished by the M(0)31B0 transfer (the M register being cleared before the transfer).
5-5	Line 11	Reads Should Read	. . . for a negative exponent, ... for a negative, non-zero exponent, . . .
5-5	Line 16	Reads Should Read	. . . overflow (when a . . . . . . underflow (when a . . .
5-5	Line 17	Reads	. . . exponent overflow condition . . .
		Should Read	. . . exponent underflow condition . . .
5-5	Line 17	Reads Should Read	. . . For a positive exponent . . . . . For a positive or zero exponent . . .

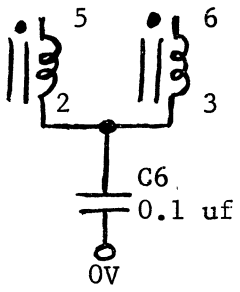
PAGE	LOCATION		CORRECTION
5-6	Table 5.1-3, Under When Used Column, 2nd Line	Reads	. . . is negative . . .
		Should Read	. . . is negative and exponent is not zero . . .
5-6	Table 5.1-3, Under When Used Column, 4th Line	Reads	. . . is plus . . .
		Should Read	. . . is plus or exponent is zero. . .
5-6	Table 5.1-4, Title Box 1st Line	Reads	. . . of Bits 31 through 27 . . .
		Should Read	. . . of Bits 31 through 21 . . .
5-6	Table 5.1-4, Last Line	Reads	. . . (PE) as exponent) . . .
		Should Read	. . . (PE) as exponent) exponent sign in single or double precision floating point numbers. (Set = minus, Reset = plus)
5-6	Table 5.1-4, Bottom	Add	26B21 All six bits reset in a single or double precision floating point number, indicates a zero exponent (EXZ).
5-7	Line 12	Reads	. . . in Part IV where. . .
		Should Read	. . . in Chapter 12 of Volume II where . . .
5-9	Line 1	Reads	. . . of an add or subtract command is . . .
		Should Read	. . . of a sum or difference operation is . . .
5-11	Line 12	Reads	. . . WS (Working Sign).
		Should Read	. . . WS (Working Sign).*
5-11	Line 14	Reads	. . . indicating subtract. WS . .
		Should Read	. . . indicating a difference. WS . . .
5-11	Bottom of Page	Add	*Provided the contents of the accumulator is being used as one of the operands.
5-15	Lines 25 and 26	Read	. . . if the subtrahend and denominator are . . .
		Should Read	. . . if one of the operands of a subtract operation and the denominator of a divide operation are . . .
5-16	Line 19	Reads	. . . that the subtrahend of a. .
		Should Read	. . . that one of the operands of a . . .

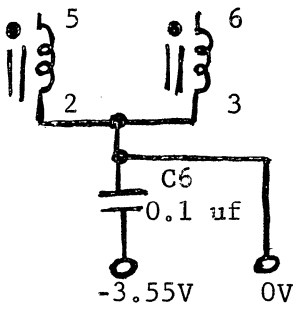
PAGE	LOCATION		CORRECTION
5-16	Line 20	Reads	. . . to the minuend. It . . .
		Should Read	. . . to the other. It . . .
5-16	Lines 22 and 23	Read	. . . that the minuend was larger than the subtrahend and the . . .
		Should Read	. . . that the smaller of the two operands was complemented and the . .
5-24	Table 5.3-2, Time Column, 2nd Line	Reads	0.048 msec.
		Should Read	0.048 μsec.
5.25	Line 5 (Leapfrog Kill Formula)	Reads	. . . ∧ . . . $(\overline{N}_{n-1} \vee \overline{D}_{n-1})$ ∧ . .
		Should Read	. . . ∧ . . . $(\overline{N}_{i-1} \vee \overline{D}_{i-1})$ ∧ . .
5-26	Figure 5.3-8, Input OR Gate to LFC Inverter 3rd Term Down	Reads	$N4 \wedge \overline{D4}$
		Should Read	$\overline{N4 \wedge D4}$
5-24	Table 5.3-2 Time Column, Last Line	Reads	or 2.006 μsec.
		Should Read	or 2.016 μsec.
5-24	Table 5.3-2, Elapsed Time Column, Last Line	Reads	2.289 μsec.
		Should Read	2.299 μsec.
5-25	Line 1	Reads	. . . are generated in Figure . . .
		Should Read	. . . are illustrated in Figure . .
5-28	Panel C, Output of Parallel Inverters Above PC16 and PK17 Inverters	Reads	26LFK13
		Should Read	26LFC13
5-28	Panel C, Output of Parallel Inverters Below PK16 and PC17 Inverters	Reads	26LFC13
		Should Read	26LFK13
5-28	Panel D As Drawn:		Should Be:



5-33	Lines 7 through 11	Delete	
5-34	Line 13	Reads	. . . sections of Part IV . . .
		Should Read	. . . sections of Volume II . . .

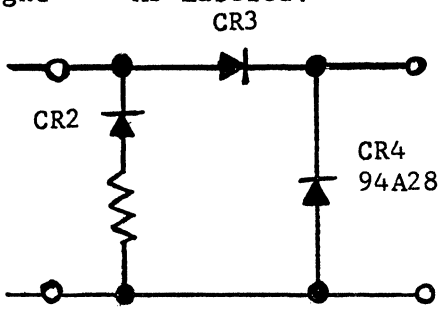
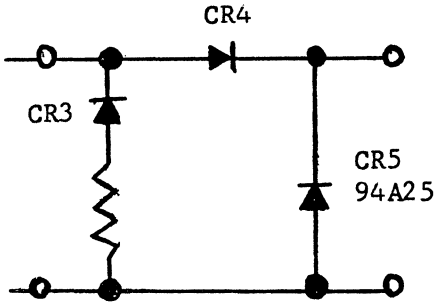
PAGE	LOCATION		CORRECTION
5-35	Line 5	Reads Should Read	. . . complement form. Certain . . . . . complement form.* Certain. .
5-35	Bottom of Page	Add	*When transferring the value of the exponent to the EP register from the B register complementing is done only if the exponent is negative and non-zero (B27 ∧ EXZ).
5-40	Table 5.4-2, (Borrow Out) Column, 2nd Number Down	Reads Should Read	0 1
6-11	Line 9	Reads Should Read	. . . or $1,000_8$, words . . . . . . or $10,000_8$, words . . .
6-13 and 6-14	Figure 6.2-2 and Figure 6.2-3, Bottom of Each	Add	NOTE: The memory addresses on this page are shown in octal and decimal.
6-19	Figure 6.3-3, Blocking Oscillator Circuit	Add	A line connecting the collector of Q5 with the collector of Q6
6-19	Figure 6.3-3, Blocking Oscillator Circuit	As Drawn:	Should Be:



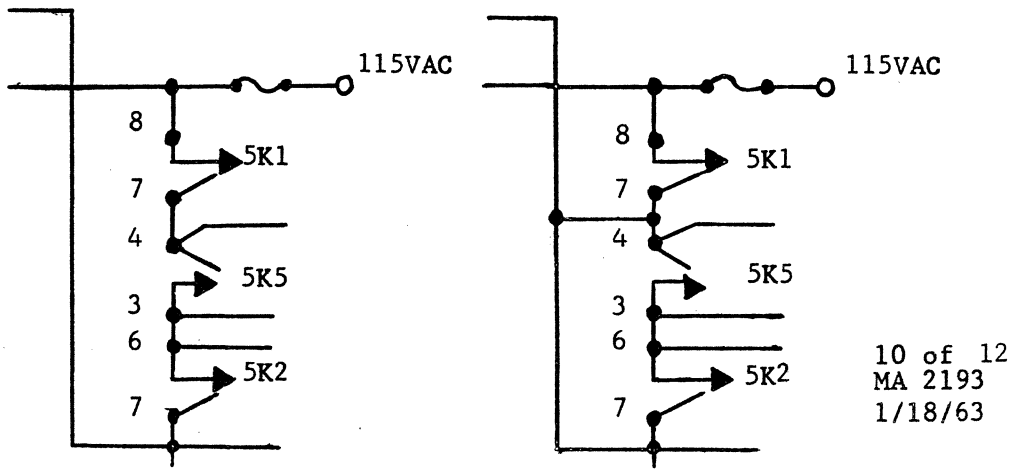


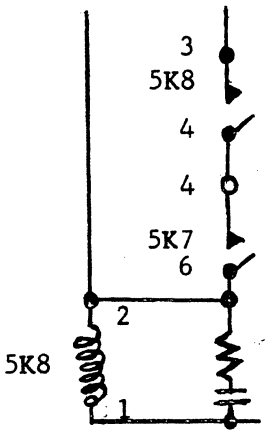
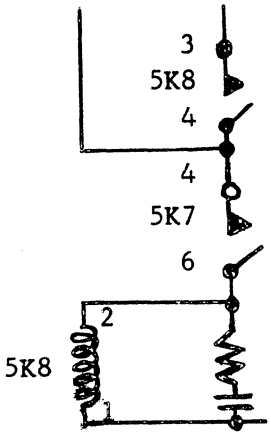
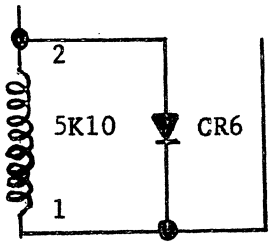
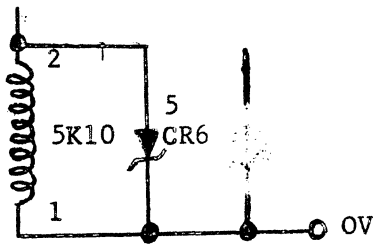
6-21	Line 12	Reads Should Read	. . . through Q5 to . . . . . . through C5 to . . .
6-24	Figure 6.3-5, Top, Center, D.C. Voltage Input	Reads Should Read	-12V +12V
6-29	Line 18	Reads Should Read	. . . available in Part III . . . . . . available in Volume II. . .
6-33	Lines 20 and 21	Delete	. . . of the read portion of a memory cycle. . .
6-38	Center of Page, Diode Immediately Below Q2	Label	CR1
6-38	Center of Page, Diode Immediately Below Q3	Label	CR2

PAGE	LOCATION		CORRECTION
6-38	Bottom, Right of Center, D. C. Voltage Input at R2	Reads Should Read	-100V -102.5V
6-38	Bottom, Left of Center, D. C. Voltage Input at R1	Add	-102.5V
6-39	Line 16	Reads Should Read	Bit 33 of . . . Bit 32 of . . .
6-39	Line 21	Reads Should Read	. . . bit 33 contains . . . . . . bit 32 contains . . .
6-39	Line 23	Reads Should Read	. . . to bit 33. Then . . . . . . to bit 32. Then . . .
6-40	Line 20	Reads Should Read	. . . to bit 33 of the . . . . . . to bit 32 of the . . .
6-40	Line 23	Reads Should Read	. . . to bit 33 is not . . . . . . to bit 32 is not . . .
6-40	Line 23	Reads Should Read	. . . into bit 33, thus . . . . . . into bit 32, thus . . .
6-50	Top, Center, Legend Box	Reads Should Read	*From DC-11 **From MM-10 ***From Central Processor or DC-11 *From MM-10 ** From Central Processor or DC-11 ***From DC-11
6-50	Center of Page, 3rd Line Receiver Down, Input	Reads Should Read	SM3 LM3
6-56	Line 3	Reads Should Read	Figure 6.6-5 has . . . Figure 6.6-4 has . . .
6-56	Line 12	Reads Should Read	. . . Figure 6.6-5 is a . . . . . . Figure 6.6-4 is a . . .
6-58	Lines 11 and 12	Delete	. . . solenoid 12K4 energized provides a hold contact for 12K5, and 12K5 keeps the D. C. voltages on.
6-58	Line 27	Reads Should Read	. . . the $12 volt . . . . . . the +12 volt . . .

PAGE	LOCATION		CORRECTION
7-9	Figure 7.1-6, D4 Package, Immediately Below M	Add	A
7-15	Table 7.1-2, V03 Package, R_L Column	Reads Should Read	7.10K 2.10K
7-15	Table 7.1-2, V13 Package, BCD No. Column	Reads Should Read	1C2312 1C2313
7-18	Figure 7.1-15, Title Box	Reads Should Read	. . . to Figure 7.1-13 . . . to Figure 7.1-14
7-22	Figure 7.2-1, Upper Right	As Labeled:  	Should Be: 
7-22	Figure 7.2-1, Center, Test Point Pin Number	Reads Should Read	J 1J
7-22	Figure 7.2-1, Lower Left CR1 Part Number	Reads Should Read	94928 94A28
7-24	Figure 7.2-2, Lower Right, Value of Capacitor Between Pins D and E	Reads Should Read	4uf 47uf
7-26	Figure 7.3-1, Top AND Gate, Lower Input Term	Reads Should Read	$\overline{SH}$ CS(
7-26	Figure 7.3-1, Bottom AND Gate, Upper Input Term	Reads Should Read	$\overline{CSC}$ SHD
7-28	Lower Right, Logic Term at Anode of CR23	Reads Should Read	$\overline{C1}$ C1
7-28	Lower Right, Junction of Anodes of CR23, 24, and 25	Add	Tie Point (⊕)
7-30	Line 12	Add	It is impossible to hand clock the G-20 through an external memory read cycle and read into the internal (Central Processor) B register.

PAGE	LOCATION		CORRECTION
7-33	Eigure 7.3-6, Center, Switch at Base of Q13	Reads Should Read	S/F S1F
7-33	Figure 7.3-6, Center, Switch at Base of Q13 Upper Contact (To R6)	Label	Fixed
7-33	Figure 7.3-6, Center, Switch at Base of Q13 Lower Contact (To R28)	Label	Variable
7-40	Figure 7.3-10, Right Center, Value of Capacitor C15	Reads Should Read	01uf .01µf
7-41	Figure 7.3-11, Lower Right, OR Gate Feeding C2 Pulse Amplifier, Lower Input Term	Reads Should Read	Man. C2 Man.
7-42	Line 8	Reads Should Read	two ten-input AND-gates which are in turn fed into two ten-input OR- two ten-input OR-gates, which are in turn fed into two ten-input AND-
7-43	Line 4	Reads Should Read	. . . Thus, it can be seen that the . . . . . . If no asynchronous events (e.g. input/output) are in process the . . .
7-43	Lines 17 and 18	Delete	. . . or completely insufficient
7-43	Line 18	Delete	. . . if this should happen, it would mean that
7-43	Lines 19 and 20	Delete	
7-55	Figure 7.4-6, Upper Left, DC Voltage Input	Add	~~-15V~~ approx. -18V
7-58	Upper Right	As Drawn:	Should Be:



PAGE	LOCATION		CORRECTION
7-58	Left, Center	As Drawn:	Should Be:
			
7-58	Right, Center, AC Voltage Input at 12L2-3	Reads Should Read	115VAC 115VAC <u>RETURN</u>
7-58	Lower Right	As Drawn:	Should Be:
			
7-59	Lines 2 and 3	Read Should Read	. . . and <u>immediately following</u> relay . . . . . . and relay . . .
7-61	Line 3	Reads Should Read	. . . SLAVE position. The . . . . . . SLAVE position*. The . . .
7-61	Line 5	Reads Should Read	. . . 5Ks, <u>5K8 and 5K9</u> are . . . . . . 5K3 <u>and 5K8</u> are . . .
7-61	Bottom of Page	Add	*Note also that since the system switch being referred to is the system switch on the Central Processor, the Central Processor must be in the SLAVE condition or ON condition before it can send a SYSTEM ON signal out over the communication line.
7-66	Figure 7.6-2, Center, Logic Input Signal	Reads Should Read	URB∧<u>TGO</u> URB∧TGO
8-31	Line 8	Reads Should Read	. . . connector pin is to . . . . . . connector pin, <u>respectively</u>, is to . . .

PAGE	LOCATION		CORRECTION
8-32	Line 6	Reads	pin is tc be . . .
		Should Read	pin, respectively, is to be . .
2-8	Immediately Below Address Preparation Commands	Add	NOTE: The accumulator is not disturbed in these opcodes.
2-8	Note, Immediately Below Address Preparation Commands	Delete	
4-10	Line 4	Reads	the ERA opcodes . . .
		Should Read	the ERO opcodes . . .
4-17	Figure 4.2-7, Center, Immediately Below and to Left of "opcode"	Reads	8
		Should Read	12
5-41	Line 23	Reads	. . . equal and positive
		Should Read	. . . equal at time of subtraction
6-34	Line 23	Reads	. . . the collector of Q2 or Q3 will . . .
		Should Read	. . . the cathode of CR1 or CR2 will . . .
6-34	Lines 24 and 25	Reads	. . . the collectors of both Q2 and Q3 are . . .
		Should Read	. . . the cathodes of both CR1 and CR2 are . . .
6-35	Line 22	Reads	(When TR and TW are . . .
		Should Read	(When $\overline{TR}$ and $\overline{TW}$ are . . .
6-41	Figure 6.5-1, Lower Right, Formula for PW	Reads	. . . B32] $\wedge$ $\overline{XPC}$
		Should Read	. . . B32] $\vee$ XPC
6-46	Line 3	Reads	. . . signals DC1 through DC5 are . . .
		Should Read	. . . signals DC0 through DC4 are . . .
6-48	Line 4	Reads	Part IV
		Should Read	Volume II
7-41	Figure 7.3-11, Upper Left Input Term of AND gate on set side of SRC F/F	Reads	C1
		Should Read	C1*
7-44	Figure 7.3-12, (C), First Line	Reads	. . . set by SSC* $\_$ $\wedge$ C1* . .
		Should Read	. . . set by SSC* $\overline{1}$ $\wedge$ C1* . .

Note: Figure 7.5-1 (Page 7-58), as corrected by this erratum serves as a valid guide to the operation of the turn-on/turn-off cycle circuitry. It should not, however, be used as a troubleshooting schematic because several of the terminal strip connections are called out wrong. A corrected drawing, suitable for trouble-shooting, will be sent out in the near future.