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ABSTRACT and CONTENTS

This document describes the functional specification for the Model 1 System Registers and the Real Time Clock. These registers are:

1) The Real Time Register (RTR)
2) The Sense Switch Register (SSR)
3) The System Control Register (SCR)
4) The System Warning Registers (SWRA, B, C, D, and E)
5) The Reset Register (RSR)
6) The Indicator Light Register (ILR)
7) The Interval Timer Register (ITR)
8) The Compute Time Register (CTR)
9) The Unique Name Generator (UNG)

The phasing of counting, loading, reading, and addressing these registers is also specified.

Revision 3 changes the address of CTR, ITR, RTR, & UNG, and adds additional definitions to the bits of RSR.

1.0 REAL TIME CLOCK SOURCE

1.1 General Description

The source frequency for the Real Time Clock Register is a very stable quartz oscillator giving a 100 kHz output signal.

1.2 Requirements

1.2.1 Stability

The Real Time Frequency Source oscillator shall have a long term stability equal to or better than $|5| \times 10^{-10}$ per 24 hours. (This corresponds to a maximum accumulated error of 2.88 seconds per year.)

1.2.2 The Real Time Clock Pulse

The Real Time Clock Pulse shall occur every 10 microseconds and shall be a single gated K3 System Clock Pulse of the Unit in which the Real Time Clock Pulse is used. In the event of the secession of the System Clock for any reason, a Real Time Clock Pulse shall be generated in lieu of the gated K3 System Clock Pulse such that, no matter in what sequence the starting and stopping of the System Clock occurs, one and only one, Real Time Clock Pulse occurs during the 10 microsecond period following the beginning of the input Real Time Timing Pulse.

1.2.3 Power Source

The Real Time Source Oscillator shall operate continuously regardless of system power failures

for a period not less than 8 hours. This implies the use of a standby floating battery source of power.

1.2.4 Available Units

The Hewlet-Packard Model 105B Oscillator meets these requirements.

2.0 THE REAL TIME REGISTER

2.1 General Description

The Real Time Register consists of 46 bits plus sign which accumulates (counts) the Real Time Clock Pulses. (46 bits will count 70,368,764,177,664 10 microsecond pulses. There are 3,162,240,000,000 10 microsecond periods in one 365 day year, thus the counter will operate for approximately 22.2 years before cycling to zero.)

2.2 Requirements

2.2.1 Size

The Real Time Register shall consist of 46 bits plus an indicator bit. The indicator bit shall be the sign bit and shall be set when a carry is propagated into the most significant half of the register.

2.2.2 Phasing of Count

All bits of the Real Time Register shall change their state in synchronism with the input Real Time Clock Pulse starting at the trailing edge. (This

removes all program restrictions on the time of reading the register.) The count shall be standard binary.

2.2.3 Carry Propagation and Read-out

A carry from the LS Half of the register into the MS half of the register shall occur normally if no reading is in progress. The sign bit is also set. If the carry occurs during or after the reading of the LS half of the register the propogation of the carry into the MS half of the register shall be delayed approximately 3 microseconds. The sign bit shall be set only when the actual propagation occurs. The sign bit shall be reset when either half of the register is read-out.

Note that the effect of this requirement is the removal of the necessity of testing the sign bit if it can be guaranteed that the reading of the two halves of the register will occur within 3 microseconds. Note also that in order to guarantee that the number read-out is always correct the LS half of the register must be read first. Should the reading of the two halves of the register be spaced more than 3 microseconds apart and a carry has occurred between the two readings the sign bit will be set and indicates that 2^{24} should be subtracted from the entire number or 1 from the MS half.

(Given that a carry has crossed the boundary, between the reading of the LS and MS half of the register, this has a 1% chance of occurrence since the Master Clock Pulse occurs 100 times more often than the Real Time Clock Pulse.)

The Real Time Register shall be readable only by the CHIO. The standard reading sequence (see paragraph 11 below) shall be used.

2.2.4 Other Outputs

a) The carry to the 2^8 and the 2^{10} position shall be made available for use by other circuits elsewhere. These are pulses every 2.56 ms and 10.24 ms.

b) An output level which indicates that the Real Time Clock Pulse is not being generated and received by the Real Time Register. This is used as a system warning signal.

2.2.5 Clear Input

All clear inputs, one for each bit of the register, shall be tied together, terminated high, and brought to a common point. This common point shall be protected from accidental grounding. This will be used to start the count at zero at a known point in time.

2.2.6 Location

The Real Time Register shall be an integral part of the CHIO.

2.2.7 Power

The Real Time Register shall be powered from the +5B (Battery) power buss. It shall operate continuously regardless of system power failures, for a minimum of 8 hours.

3.0 SENSE SWITCH REGISTER

3.1 General Description

The Sense Switch Register consists of 24 bits any one of which may be set or reset by a corresponding switch on the Master Control Panel.

3.2 Requirements

3.2.1 Size

The Sense Switch Register shall consist of 24 bits.

3.3.2 Phasing of Set or Reset

A bit of the Sense Switch Register shall sample the signal from its associated sense switch once every 10.24 ms using the 10.24 ms period pulse from the Real Time Register. This will accomplish debounce.

3.2.3 Location

The Sense Switch Register shall be an integral part of the micro scheduler.

3.2.4 Power

Normal power supply of the micro scheduler shall be used.

4.0 SYSTEM CONTROL REGISTER

4.1 General Description

The System Control Register consists of 24 bits. The least significant 22 bits may be set or reset by a corresponding switch on the Master Control Panel. The most significant bit is a sample of the System GO push button on the Master Control Panel. The next most significant bit is a flip-flop called CONTINUE which is set by GO and reset by the System STOP push button (also known as system ZM). Except for the two most significant bits this register is physically the 22 LSBs of the Sense Switch Register. The distinction between the two is determined by the call address.

4.2 Requirements

The 22 least significant bits of the System Control Register shall be the 22 least significant bits of the Sense Switch Register. The second most significant bit shall be a flip-flop which is set by the System GO push button and reset by the System STOP (system ZM) push button. The most significant bit shall be a sample of the System GO

push button.

The selection between the two MSB's of the Sense Switch Register and the two MSB's of the System Control Register shall be determined by the call address. All other requirements are the same as for the Sense Switch Register.

5.0 THE SYSTEM WARNING REGISTERS

5.1 General Description

There are five System Warning Registers, A, B, C, D and E. Each is 24 bits long. They provide a central deposit of signals which indicate some malfunction in the system, a few of which require immediate attention. The System Warning Registers are ranked in order of priority. SWRA, which has the highest priority, provides warning in case of various power supply failures which require immediate attention. In general a unit will operate reliably for no more than one millisecond after the detection of a unit power failure. SWRA also gives warning in case of Core Memory Power Supply failures. Any one Core Memory Module is immediately internally inhibited upon detection of a power failure. SWRB and SWRC provide warning in case of Core Memory parity errors. SWRD provides warning in case of parity errors detected in a micro-processor. SWRE,

which has lowest priority, provides warning in case of various other miscellaneous malfunctions, none of which will immediately cause the system to malfunction but which may eventually do so if not attended to (such things as Rack overtemperature, reserve batteries discharging, and excessive disk or drum vibration). There are a sufficient number of spare bits to enable the addition of other warning signals in appropriate priority as they may become desirable. A REQUEST STROBE #2 signal is generated which is the union of all bits in the first four registers. It causes the generation of REQUEST STROBE #2 to the Micro Scheduler if the STROBE #2 INHIBIT is off.

Where appropriate the "bits" of a register may be only the input warning levels appropriately gated onto the E Bus.

5.2 Requirements

5.2.1 Size

The System Warning Register shall consist of five registers, each of which shall be 24 bits long.

5.2.2 Warning Signal Inputs

The following bit assignment shall be followed:

A. SWRA

Bit 0: Set on the occurrence of PF. (PF indicates input AC power failure. When set it indicates approximately 1 ms of reliable operation remaining. See SCCP/S-3 .)

Bit 1: Set if the +5 "Battery" power goes out of tolerance (see reference).

Bit 2: Set on the occurrence of S1UPO' (Fast Memory UNIT POWER ON). About 1 ms of reliable operation remaining.

Bit 3: Set on the occurrence of S2UPO'. (TUIM UNIT POWER ON). 1 ms of operation remains.

Bit 4: Set on the occurrence of T1UPO' (CPU #1) 1 ms left.

Bit 5: (Future) T2UPO' (CPU #2)

Bit 6: U1UPO' (AMC)

Bit 7: (Future) U2UPO' Second Unit in Rack U.

Bit 8: (Future) U3UPO' Third Unit in Rack U.

Bit 9 : V1UPO' (MPMBM).

Bit 10: (Future) V2UPO' Second Unit in Rack V.

Bit 11: (Future) V3UPO' Third Unit in Rack V.

Bit 12: W1UPO' (CHIO)

Bit 13: W2UPO' (Micro-scheduler)

Bit 14: X1UPO' (Master Control-pilot Supplies)

Bit 15: Spare

Bit 16,17: Spare

Bit 18: Set if no Real Time Clock Pulse is generated for RTR

Bit 19: Set if no Real Time Clock is generated for ITRs/CTRs.

Bit 20: Set if any of the POWER SUPPLY READY (PSR) signals of the Core Memory Modules in Quadrant J go false.

Bit 21: Set if any of the POWER SUPPLY READY (PSR) signals of the Core Memory Modules in Quadrant K go false.

Bit 22: Set if any of the POWER SUPPLY READY (PSR) signals of the Core Memory Modules in Quadrant L go false.

Bit 23: Set if any of the POWER SUPPLY READY (PSR) signals of the Core Memory Modules in Quadrant M go false.

B. SWRB

Bit 0: Set if a parity error is detected in data read from Memory Module 1.

Bit 1: Set if a parity error is detected in data written in Memory Module 1.

Bit 2: Set if a parity error is detected in the address for Memory Module 1.

Bit 3: Set if a parity error is detected in data read from Memory Module 2.

Bit 4: Set if a parity error is detected in data written in Memory Module 2.

Bit 5: Set if a parity error is detected in the address for Memory Module 2.

Bit 6: Set if a parity error is detected in data read from Memory Module 3.

Bit 7: Set if a parity error is detected in data written in Memory Module 3.

Bit 8: Set if a parity error is detected in the address for Memory Module 3.

Bit 9: Set if a parity error is detected in data read from Memory Module 4.

Bit 10: Set if a parity error is detected in data written in Memory Module 4.

Bit 11: Set if a parity error is detected in the address for Memory Module 4.

Bit 12: Set if a parity error is detected in data read from Memory Module 5.

Bit 13: Set if a parity error is detected in data written in Memory Module 5.

Bit 14: Set if a parity error is detected in the address for Memory Module 5.

Bit 15: Set if a parity error is detected in data read from Memory Module 6.

Bit 16: Set if a parity error is detected in data written in Memory Module 6.

Bit 17: Set if a parity error is detected in the address for Memory Module 6.

Bit 18: Set if a parity error is detected in data read from Memory Module 7.

Bit 19: Set if a parity error is detected in data written in Memory Module 7.

Bit 20: Set if a parity error is detected in the address for Memory Module 7.

Bit 21: Set if a parity error is detected in data read from Memory Module 8.

Bit 22: Set if a parity error is detected in data written in Memory Module 8.

Bit 23: Set if a parity error is detected in the address for Memory Module 8.

C. SWRC

Bit 0: Set if a parity error is detected in data read from Memory Module 9.

Bit 1: Set if a parity error is detected in data written in Memory Module 9.

Bit 2: Set if a parity error is detected in the address for Memory Module 9.

Bit 3: Set if a parity error is detected in data read from Memory Module 10.

Bit 4: Set if a parity error is detected in data written in Memory Module 10.

Bit 5: Set if a parity error is detected in the address for Memory Module 10.

Bit 6: Set if a parity error is detected in data read from Memory Module 11.

Bit 7: Set if a parity error is detected in data written in Memory Module 11.

Bit 8: Set if a parity error is detected in the address for Memory Module 11.

Bit 9: Set if a parity error is detected in data read from Memory Module 12.

Bit 10: Set if a parity error is detected in data written in Memory Module 12.

Bit 11: Set if a parity error is detected in the address for Memory Module 12.

Bit 12: Set if a parity error is detected in data read from Memory Module 13.

Bit 13: Set if a parity error is detected in data written in Memory Module 13.

Bit 14: Set if a parity error is detected in the address for Memory Module 13.

Blt 15: Set if a parity error is detected in data read from Memory Module 14.

Bit 16: Set if a parity error is detected in data written in Memory Module 14.

Bit 17: Set if a parity error is detected in the address for Memory Module 14.

Bit 18: Set if a parity error is detected in data read from Memory Module 15.

Bit 19: Set if a parity error is detected in data written in Memory Module 15.

Bit 20: Set if a parity error is detected in the address for Memory Module 15.

Bit 21: Set if a parity error is detected in data read from Memory Module 16.

Bit 22: Set if a parity error is detected in data written in Memory Module 16.

Bit 23: Set if a parity error is detected in the address for Memory Module 16.

D. SWRD

Bit Ø: Set if parity error #1 is detected by CPU #1 (T1).

Bit 1: Set if parity error #2 is detected by CPU #1 (T1).

Bit 2: Set if parity error #1 is detected by CPU #2 (T2).

Bit 3: Set if parity error #2 is detected by CPU #2 (T2).

Bit 4: Set if parity error #1 is detected by AMC (U1).

Bit 5: Set if parity error #2 is detected by AMC (U1).

Bit 6: Set if parity error #1 is detected by (Future) (U2).

Bit 7: Set if parity error #2 is detected by (Future)(U2).

Bit 8: Set if parity error #1 is detected by (Future) (U3).

Bit 9: Set if parity error #2 is detected by (Future) (U3).

Bit 10: Set if parity error #1 is detected by (Future) (V2).

Bit 11: Set if parity error #2 is detected by (Future) (V2).

Bit 12: Set if parity error #1 is detected by CHIO (W1).

Bit 13: Set if parity error #2 is detected by Micro Scheduler (W2).

Bits 14 through 21: Set if Memory Modules; 1 thru 8 respectively, Unit Available Time out signal is true, i.e., a Memory Unit is not available for longer than 1 microsecond.

E. SWRE

Bit Ø: Set if the Battery in the Real Time Frequency Source is discharging (approximately eight hours of operation are possible before the battery discharges, i.e., about eight hours to repair or supply external 24 VDC).

Bit 1: Set if the storage battery is discharging. (The source for the +5 "Battery" supply.) Approximately eight hours remaining

Bit 2 through 14: Spare

Bit 15 through 23: Set if overtemperature is detected in Racks R through Z respectively.

	A	B		C
	Power	Core Memory Parity Errors		
	Imminent Sys. Failure	Incipient System Failure		
		Parity Error in:	SWRB	SWRC
Ø	PF	Data Read		
1	+5B	Data Written	Mem. Mod. 1	Mem. Mod. 9
2	FM UPO'	Address		
3	TUIM UPO'	Data Read		
4	CPU 1 UPO'	Data Written	Mem. Mod. 2	Mem. Mod. 10
5	CPU 2 UPO'	Address		
6	AMC UPO'	Data Read		
7	U2UPO'	Data Written	Mem. Mod. 3	Mem. Mod. 11
8	U3UPO'	Address		
9	MPMBM UPO'	Data Read		
1Ø	V2UPO'	Data Written	Mem. Mod. 4	Mem. Mod. 12
11	V3UPO'	Address		
12	CHIO UPO'	Data Read		
13	Micro Sch UPO'	Data Written	Mem. Mod. 5	Mem. Mod. 13
14	X1UPO (Pilot P.S. UPO')	Address		
15	Spare	Data Read		
16	Spare	Data Written	Mem. Mod. 6	Mem. Mod. 14
17	Spare	Address		
18	Failure of RTP in RTR	Data Read		
19	Failure of RTP in Sp. Reg.	Data Written	Mem. Mod. 7	Mem. Mod. 15
2Ø	Quad.J PSR	Address		
21	" K "	Data Read		
22	" L "	Data Written	Mem. Mod. 8	Mem. Mod. 16
23	" M "	Address		

	D	E
	Miscellaneous	Miscellaneous
	High Priority	Low Priority
Ø	Parity #1 CPU #1 (T1)	RTFS Battery Discharging
1	" #2 CPU #1 (T1)	12v Storage Battery Discharging
2	" #1 CPU #2 (T2)	Spare
3	" #2 CPU #2 (T2)	Spare
4	" #1 AMC (U1)	"
5	" #2 AMC (U1)	"
6	" #1 Future (U2)	"
7	" #2 " (U2)	"
8	" #1 " (U3)	"
9	" #2 " (U3)	"
1Ø	" #1 " (V2)	"
11	" #2 " (V2)	"
12	" #1 CHIO (W1)	"
13	" #2 CHIO (W1)	"
14	" #1 Micro. Sch. (W2)	"
15	" #2 Micro Sch. (W2)	R Overtemperature
16	MUATO 1	S "
17	" 2	T "
18	" 3	U "
19	" 4	V "
2Ø	" 5	W "
21	" 6	X "
22	" 7	Y "
23	" 8	Z "

5.2.3 STROBE INHIBIT

A Flip Flop called STROBE INHIBIT shall enable or disable the sending of REQUEST STROBE #2 to the Microscheduler. It is set by a '1' in bit Ø of the Reset Register and reset by a '0' in Bit Ø.

5.2.4 Outputs

The System Warning Registers shall be read by the Micro Scheduler. A REQ. STROBE #2 signal shall be generated so long as a bit is set in registers A thru D and the STROBE INHIBIT is OFF. Other read out timing shall be as specified in paragraph 11.

5.2.5 Resetting

A. SWRA and SWRE

All bits of the register shall be copies of their respective input signals.

B. SWRB, SWRC, and SWRD

All bits shall be reset when the register is read.

6.0 THE RESET REGISTER

6.1 General Description

The Reset Register is an addressable pseudo-register provided to allow programmable reset of any microprocessor and the CPU's. It also is used to enable or disable the STROBE #2 signal from the System Warning Registers to the Micro-

scheduler. In addition provision is made for the future installation of program control of the deselection of half of the core memory, a function presently done entirely manually by switches on the Master Control Panel.

Each CPU and each microprocessor (resetable Units) has a corresponding bit in the register. The output of the register is a gated POT signal to every resetable unit corresponding to a 'set' bit. This signal is one term of a local RESET signal in each resetable unit. The other terms, which are ORed together are:

1.) System Reset

A signal generated by the System STOP push button, located on the Master Control Panel and which initiates a system wide ZM cycle. (see SCCP/S-3)

2.) Local Reset

A signal generated by the LOCAL RESET push button, located on the Local Control Panel.

3.) Breakpoint

A signal generated by the debugging equipment.

The local RESET signal does the following

in a microprocessor:

1.) Clears the ROM address ('O' register and the bank flip-flop)

2.) Clears the current instruction ('I' register)

3.) Initializes the Core Memory interface by resetting SCY, FCY, MPREQ, LMRUN, STARTP

4.) Resets the state flip-flops XXB and XXC

5.) Enables RCE

Note that the System can reset itself by sending '1's' to all the resetable Units simultaneously.

6.2 Requirements

6.2.1 Bit Assignment and Meaning

When a '1' appears in the following bit position the meaning is:

Bit	Meaning
Ø	Set STROBE #2 INHIBIT for SWR. A 'O' will reset the STROBE #2 INHIBIT.
1	Cause half of the Core Memory to be deselected according to bits 2 and 3.
2	Select guadrant J and deselect quadrant K. A 'O' will select K and deselect J.

3	Select quadrant L and deselect quadrant M. A '0' will select M and deselect L.
4-12	Spare
13	Reset Fast Memory (Unit S1), If Implemented
14	Reset AMTU (" S2), If Implemented
15	Reset CPU #1 (" T1)
16	Reset CPU #2 (" T2)
17	Reset AMC (" U1)
18	Reset possible future unit U2
19	" " " " U3
20	" MPMBM (" V1), If Implemented
21	" possible " " V2
22	" CHIO (Unit W1)
23	" MSCH (" W2)

6.2.2 Input/Output

When addressed, bits 13 to 23 of the Reset Register shall gate a 200 ns signal onto those lines corresponding to a '1' in the input word from the Microscheduler. A standard ALERT/POT sequence shall be used.

6.2.3 Location and Power

The Reset Register shall be an integral part of the Microscheduler and shall use the normal +5 power bus therefrom.

7.0 THE INDICATOR LIGHT REGISTER

7.1 General Description

The Indicator Light Register has 24 bits. It is used to drive the set of 24 indicator lights on the Master Control Panel. The register

loaded by the Micro Scheduler.

7.2 Requirements

The Indicator Light Register shall be 24 bits. No special timing or power requirements exist. The register shall be an integral part of the Micro Scheduler.

8.0 THE INTERVAL TIMER REGISTER

8.1 General Description

There is an Interval Timer Register associated with each CPU. The register is continuously incremented by the Real Time Clock Pulse. The CPU loads the complement of the desired interval into the register, however, the sign bit is normally loaded with an "0" . Thus, a carry into the sign bit indicates the end of the time interval, however, the register will continue to count. The CPU may read the register at any time.

Note: if N = the number loaded into the register and n = the number read from the register, both the following relationships hold:

A. For the case where the true number is loaded into the register and the register is decremented:

1) the number of 10 microsecond periods which occur before the sign bit changes=N+1.

2) the elapsed time = $N-|n|$ if s=0

$N+|\overline{n}|$ if s=1

B. For the case where the complement of the number is loaded into the register and it is incremented:

1) the number of 10 microsecond periods remain N+1

2) the elapsed time = $N-|\overline{n}|$ if s=0

= $N+|n|$ if s=1

8.2 Requirements

8.2.1 Size

The Interval Timer Register shall consist of 24 bits.

8.2.2 Phasing

All bits of the Interval Timer Register shall change their state in synchronism with the Real Time Clock Pulse starting at the trailing edge. The counter shall increment in standard binary starting from a number loaded in. There are no program restrictions as to when data is loaded into the register or read from the register.

8.2.3 Loading Date and Readout

All bits of the Interval Timer Register shall be capable of loading data from its associated CPU and to be read by its associated CPU, according to the timing given in paragraph 11 below. A D.C. level shall be available to its associated CPU from the sign bit for branch condition detection

of overflow.

8.2.4 Power

A normal +5v power bus from the register's associated CPU shall be used.

8.2.5 Location

The register(s) shall be a part of the associated CPU.

9.0 THE COMPUTE TIME REGISTER

9.1 General Description

There is a Compute Time Register associated with each CPU. Each register is 24 bits long and is loaded by its assocaited CPU. The register is incremented by the Real Time Clock Pulses. The associated CPU may read the contents of the register, at any time.

9.2 Requirements

9.2.1 Size

The Compute Time Register shall consist of 24 bits.

9.2.2 Phasing and Direction of Count

All bits of the Compute Time Register shall change their state in synchronism with the Real Time Clock Pulse starting at the trailing edge. The counting action shall increment the register in standard binary starting from a number loaded in.

9.2.3 Other Requirements

The Loading, Readout, Power and Location requirements are the same as the Interval Timer Register.

10.0 THE UNIQUE NAME GENERATOR

10.1 General Description

The Unique Name Generator is a counter 40 flip-flops long but read as if it were 41 bits long. The least significant bit is hard wired so that CPU #1 will always read an odd number and CPU #2 will always read an even number. Each time that the register is accessed by either CPU or both, the counter is incremented by 2. The register serves to supply a unique number each time that it is read. 41 bits will provide 2,199,023,255,552 unique numbers but only half of these numbers will normally be used. In effect, then, only 2^{40} unique numbers will be used to provide 1,099,511,627,776 numbers. The time over which unique numbers can be provided versus the average access rate is as follows:

Average Access Rate	Approximate Time Duration
10 microseconds	.319 year or 110 days
100 microseconds	3.19 years
1 millisecond	31.9 years

10.2 Requirements

10.2.1 Size

The Unique Name Generator shall consist of 41 bits. The LSB shall be hard wired as a "1" to CPU #1 and as a "0" to CPU #2. The other 40 bits shall be a counting register.

10.2.2 Phasing and Speed

All 40 bits of the counting register shall change their state in synchronism with the count pulse beginning with the trailing edge. The register shall be capable of counting at the full 10 MHz rate of the Master Clock Pulse. Other timing is given in paragraph 11.

10.2.3 Readout

Each half of the register shall be read by a separate address. The LS half shall be read first, then the MS half. Provision shall be made to allow simultaneous or overlapping reading of the register by both CPU's such that each receives a unique number. CALL LS half implies increment and read LS half of UNG. CALL MS half implies read MS half of UNG.

10.2.4 Clearing

All clear inputs to the register shall be tied together, terminated high, and brought to a common

point. This point shall be protected from accidental grounding. This point is used to initialize the register at the beginning of operation.

10.2.4.1 Setting

Each preset input shall be individually tied high so that a number may be preset in case of failure/ repair/loss of power, etc.

10.2.5 Power

The special power bus, +5B (battery) shall be used to provide continuous preservation and operation in the event of system power failure or power down. Provision shall be made for continuous operation with the card removed.

10.2.6 Location

The register shall be a part of CPU1.

11.0 SYSTEM TIMING

11.1 General Description

The general scheme of reading or loading any of the registers is as follows: The address of the register to be accessed is loaded into the Z register of the accessing Unit followed by an ALERT then a PIN for a read or a POT for a load. In the case of a double length register, each half has a separate address. In the case of a load, the Z register is loaded with the data to be transferred to the register in the next cycle after loading the address. This is

fully described in Specification MPPI/S-16 .

11.2 Requirements

11.2.1 Timing for Special Registers (except UNG)

Figure 11-1 shows the timing applicable to all registers except UNG. Specification MPPI/S-16 shall prevail in case of conflict. There are two items to note concerning RTR:

1) The ALERT for reading the MS half of RTR may occur simultaneously with the PIN for reading the LS half.

2) Paragraph 2.2.3, which notes that the LSB's should be read first, must be observed if the time is to be correctly read at all times.

11.2.2 Timing for UNG

Figure 11-2 shows the timing applicable to UNG. Specification MPPI/S-16 shall prevail in case of conflict.

11.2.3 Address Coding

Seventeen unique addresses are required for the System Registers. In the Microscheduler they are:

	Z	0,15,16,17,18	19	20	21	22	23	OCTAL
Read SRWA		0	0	0	0	0	1	1
B		0	0	0	0	1	0	2
C		0	0	0	0	1	1	3
D		0	0	0	1	0	0	4
E		0	0	0	1	0	1	5
Read SSR		0	0	0	1	1	0	6
Read SCR		0	0	0	1	1	1	7
Load ILR		0	0	1	0	0	0	10
Load RSR		0	0	1	0	0	1	11

In the CHIO they are:

	Z	0	18	19	20	21	22	23	OCTAL
Read LS RTR		0	0	1	1	0	0	0	60
Read MS RTR		0	0	1	1	0	0	1	61

In the Special Register unit they are:

	Z	0	18	19	20	21	22	23	OCTAL
Read ITR		0	0	1	1	0	0	0	30
Load ITR		0	0	1	1	0	0	1	31
Read CTR		0	0	1	1	0	1	0	32
Load CTR		0	0	1	1	0	1	1	33
Read LS UNG		0	0	1	1	1	0	0	34
Read MS UNG		0	0	1	1	1	0	1	35

11.2.3.1 The address given in the previous paragraph are those presently installed in M1 phase 1. For CPU phase one, they will remain as stated. For CPU phase 1.5 and 2, the Special Register will revert back to:

	Z	0	18	19	20	21	22	23	OCTAL
Read ITR		0	1	1	0	0	0	0	60
Load ITR		0	1	1	0	0	0	0	61
Read CTR		0	1	1	0	0	0	0	62
Load CTR		0	1	1	0	0	0	0	63
Read LS UNG		0	1	1	0	0	0	0	64
Read MS UNG		0	1	1	0	0	0	0	65

In the phase 2 CHIO, the address for RTR will probably be 4B7+40 and 4B7+41. This spec will be updated when these are firm.

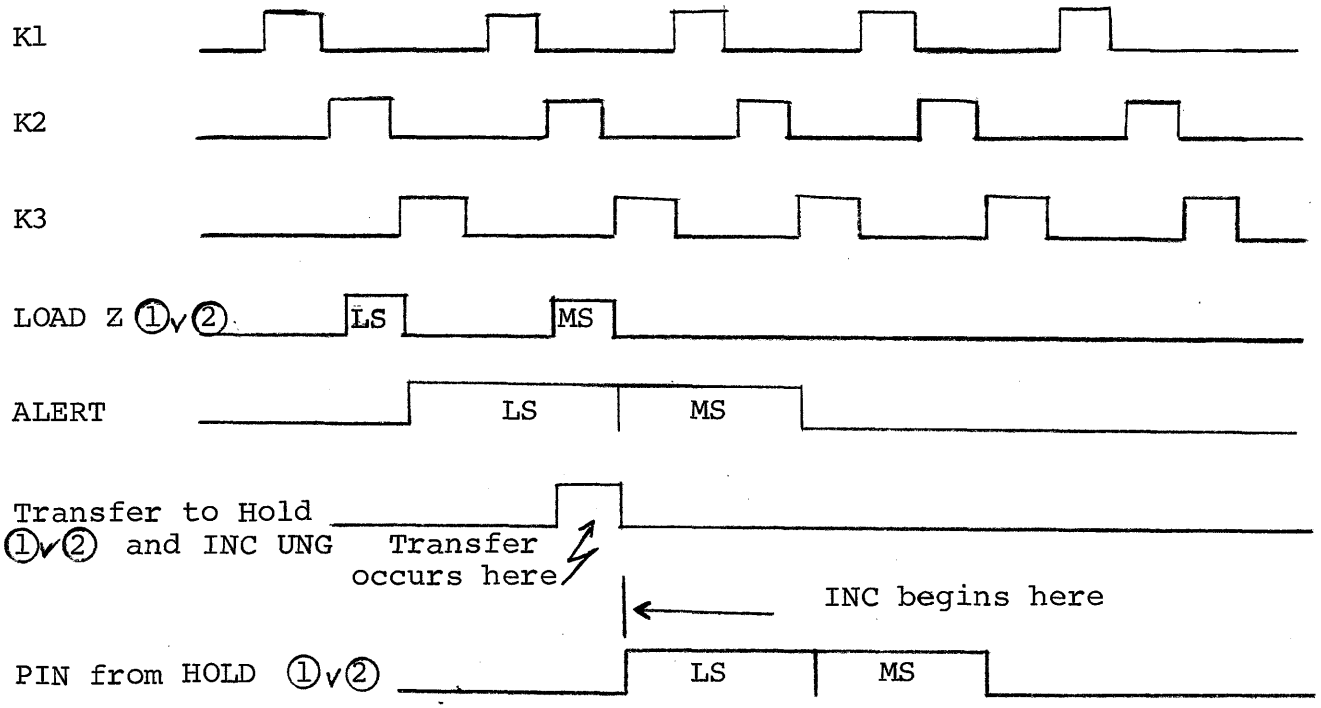
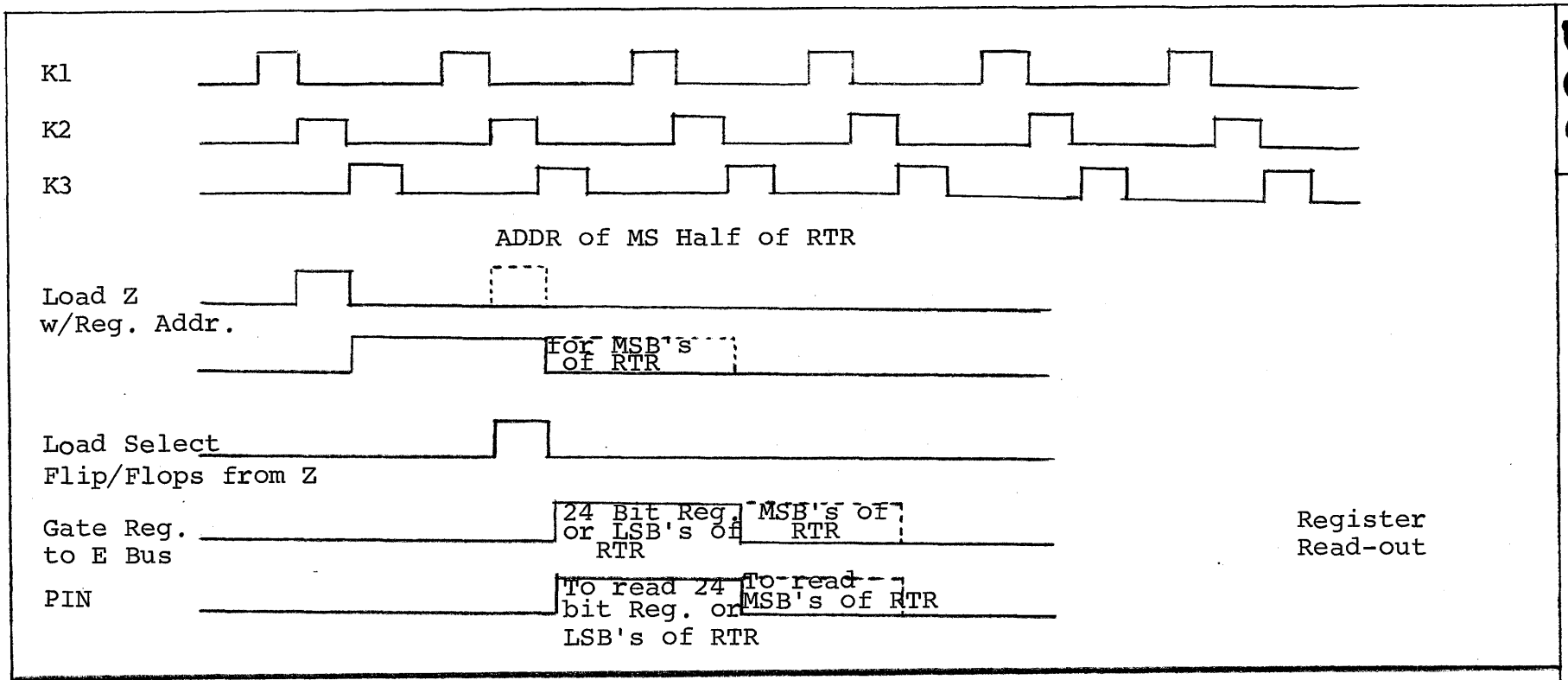


Figure 11-2
TIMING FOR UNG



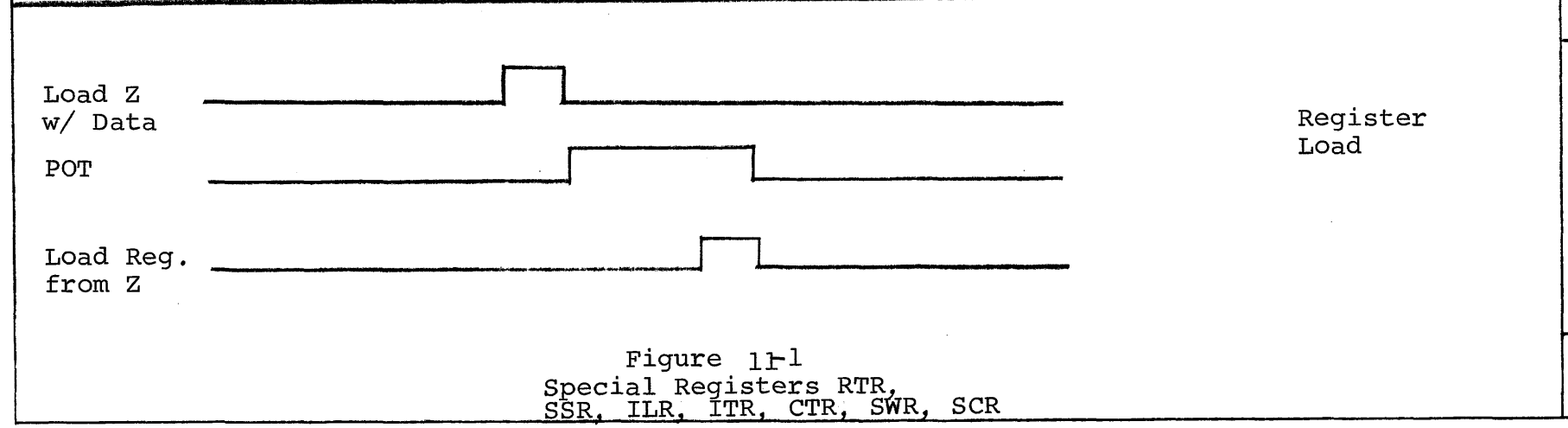


Figure 11-1
Special Registers RTR,
SSR, ILR, ITR, CTR, SWR, SCR