Peripheral Serial Buffer

PSB-Ø2 Logic Description

PSB-Ø5 Technical Reference

PSB-15 Standard Modification

PSB-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/19/75	

PSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/19/75

CHECKER

ENGINEER 751219

APP'D FOR REL 751219

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PSB LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		PSB - Ø2

SCALE	REV A	SHEET OF

PSB

SUE 4502 SERIAL I/O CONTROLLER

MAINTENANCE BULLETIN M4502

Includes Program Wiring For:

SUE 4630 TELETYPEWRITER CONTROLLER
SUE 4640 ALPHANUMERIC DISPLAY CONTROLLER

620

May 74 Rev. B

CONTENTS

LIST OF ILLUSTRATIONS

SUE 4502 SERIAL I/O CONTROLLER

MAINTENANCE BULLETIN

PSB

INTRODUCTION

This bulletin contains a logic description of the SUE 4502 Serial I/O Controller. A functional block diagram of the 4502 is shown in figure 1 and input-output timing is shown in figure 2. The functional block diagram is keyed to the logic diagrams in this bulletin by the number in the upper left-hand corner of each block. This number indicates the logic diagram sheet on which the logic, that corresponds to the block, is represented.

SUE 4502 can be programmed by jumpers to accommodate a number of serial I/O devices. With program wiring installed, SUE 4502 becomes a specific device controller that carries a model number in the 4600 series. Refer to the program wiring indicated in the parts lists near the end of this bulletin for the following device controllers:

SUE 4630 Teletypewriter Controller	PL2001002138-10
SUE 4640 Alphanumeric Display Controller	PL2001002138-11

All program plugs on the 4502 are indicated in the logic diagrams (LD2001002138 sheets 1 through 11 of 11) and can be located by referring to Circuit Card Assembly, PSB Serial Buffers, drawing number 2001002138.

DRAWINGS AND PARTS LISTS

This is a list of the drawings and parts lists included in this bulletin.

Title	Mnemonic	Drawing Number	Sheets
Serial Buffer Circuit Card	PSB	2001002138-1	1
Serial Buffer Logic Diagram	PSB	LD2001002138-1	1 thru 11
Serial Buffer Parts List	PSB	PL2001002138-1	2, 3, 4, 8
Serial Buffer Parts List	PSB	PL2001002138-10	5, 8
Serial Buffer Parts List	PSB	PL2001002138-11	6, 8

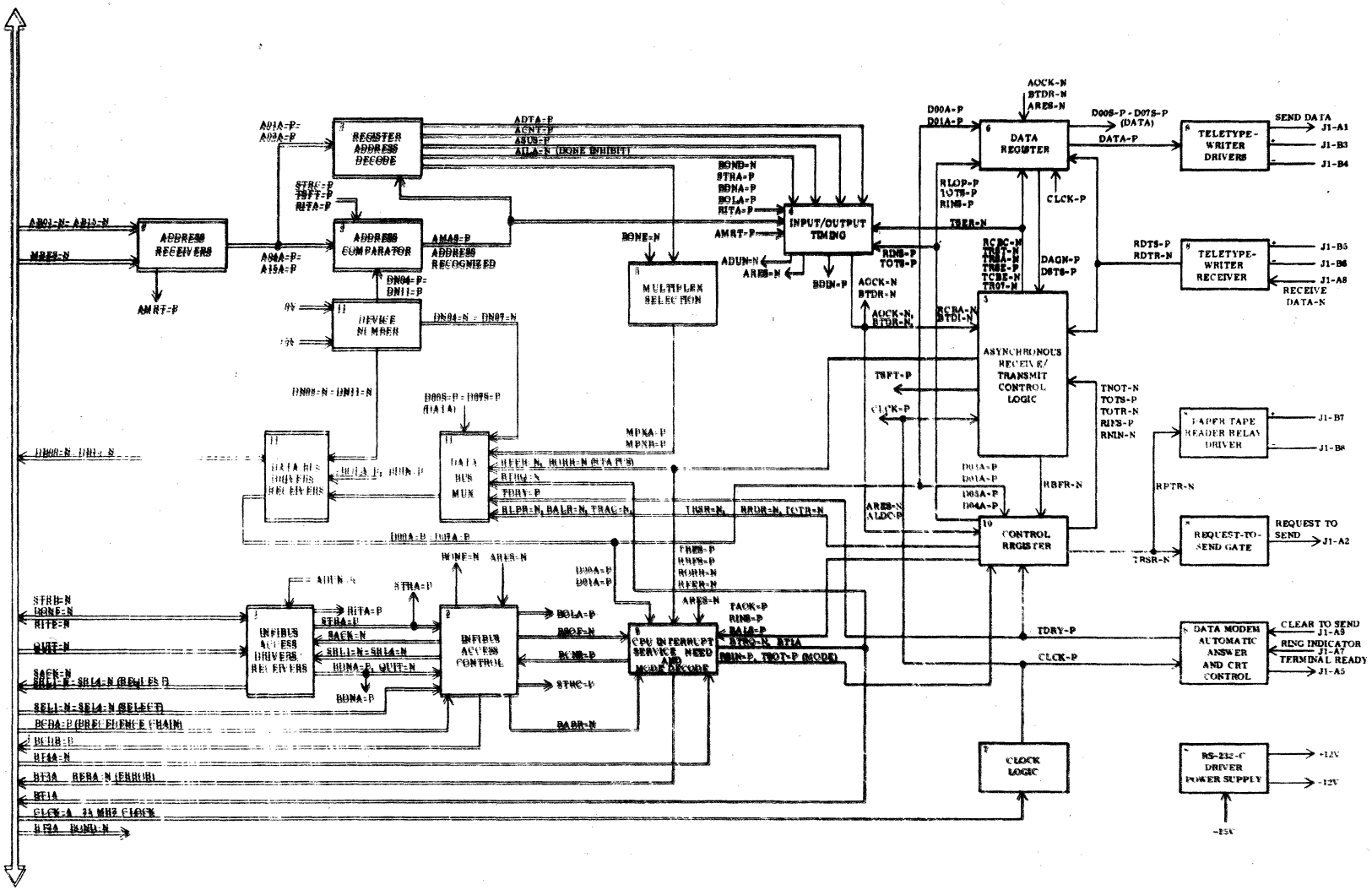


Figure 1. SUE 4502 Functional Block Diagram

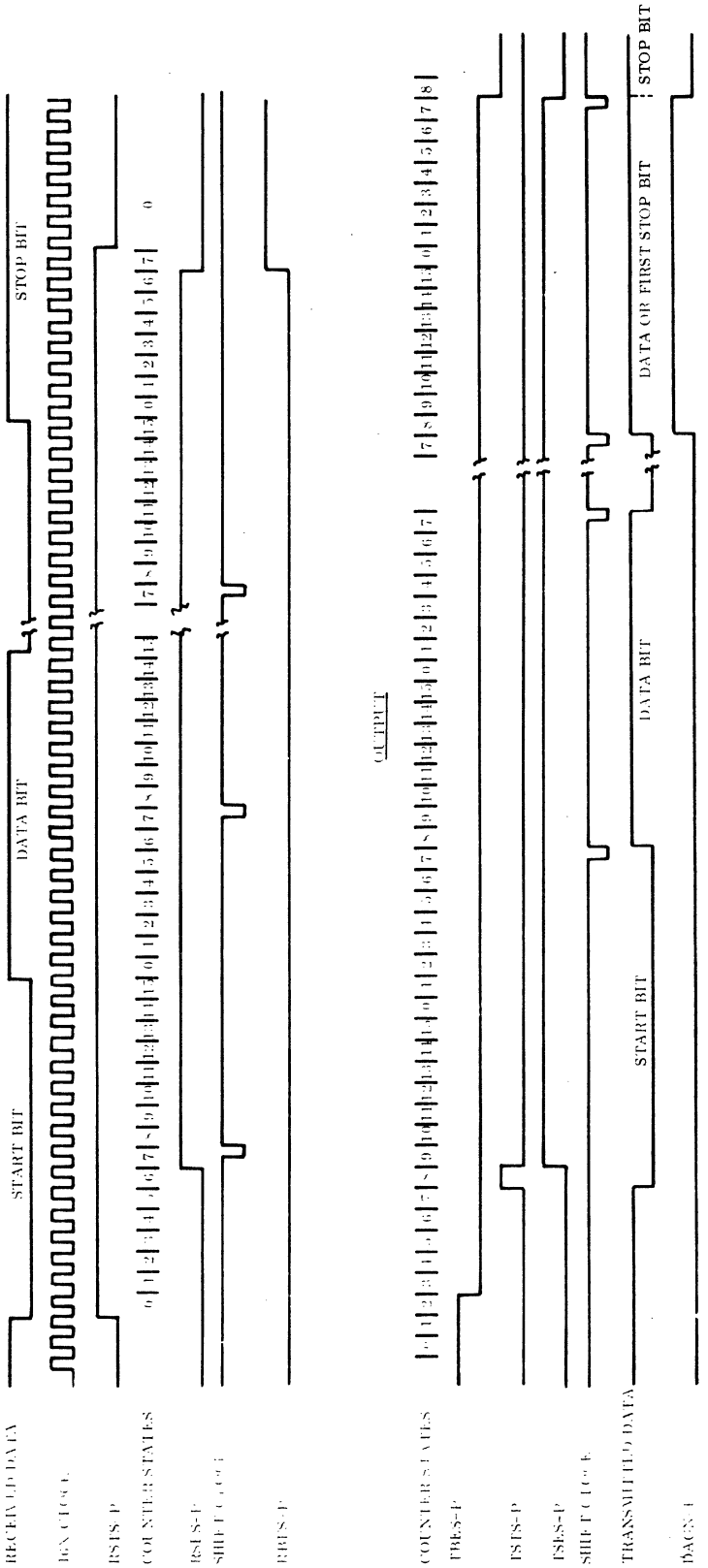
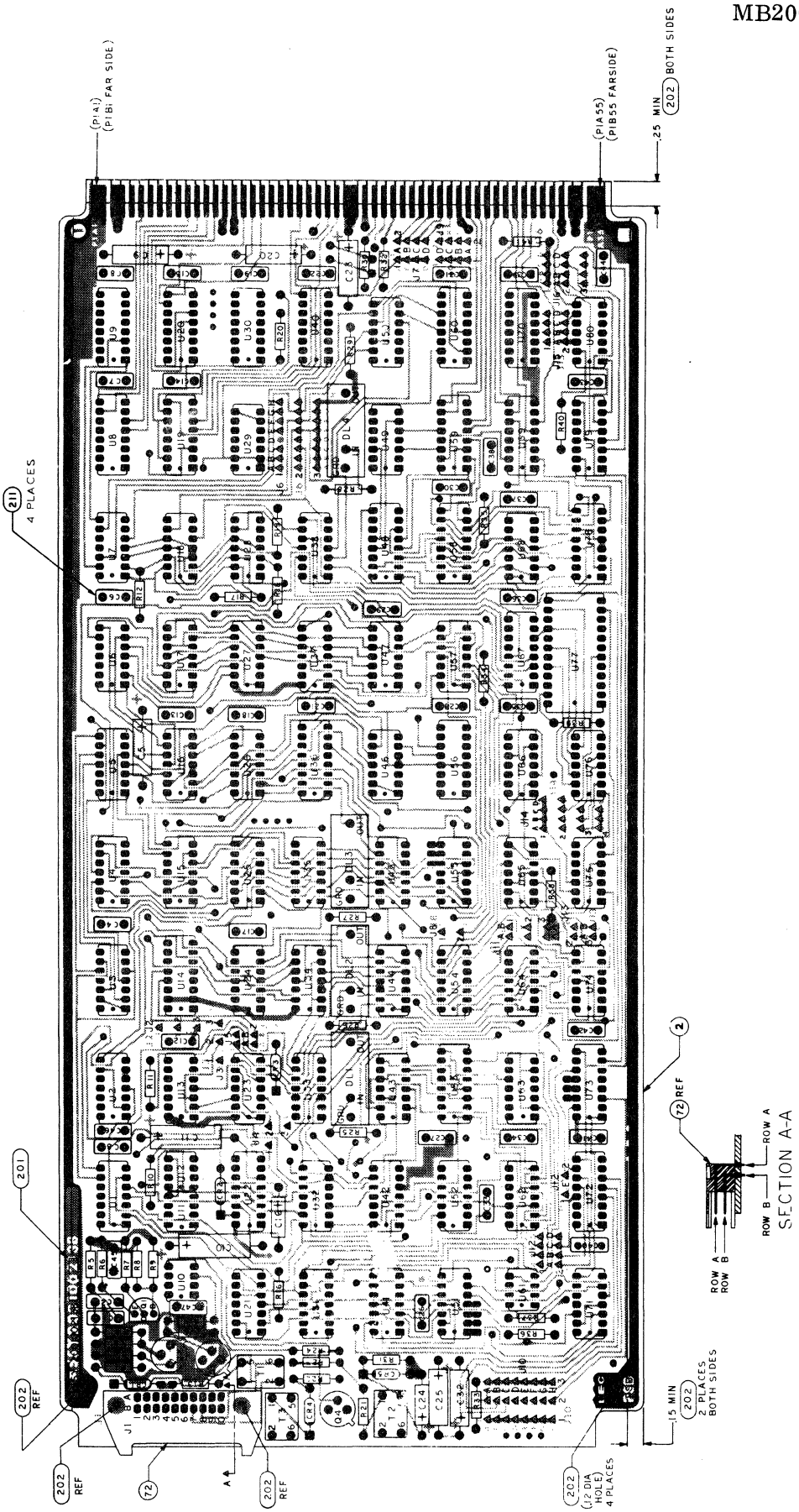


Figure 2. SUE 4502 Input/Output Timing

PSB



Serial Buffer Circuit Card (PSB)
2001002138-1, Rev. F, Sheet 1

PSB

NOTES: UNLESS OTHERWISE SPECIFIED

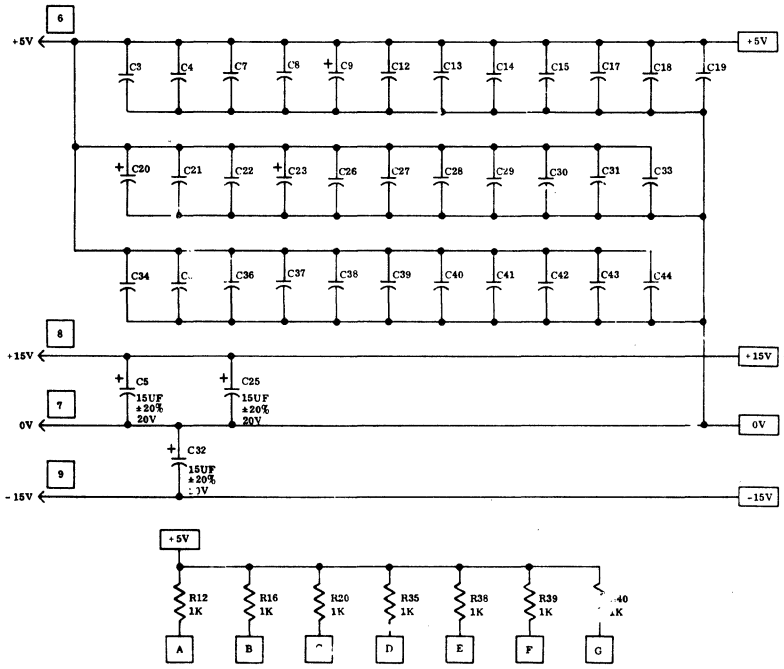
1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33UF, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED. FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 3001800200.)
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V, EXCEPT T93 PIN 5 +5V, PIN 10 0V, 8242 AND H103 PIN 4 +5V, PIN 11 0V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR PIN 7 AND 8 0V, PIN 16 +5V, P154 PIN 8 0V, PIN 15 +5V, H106 PIN 5 +5V, PIN 13 0V; (24 PIN ICP) PIN 12 0V, PIN 24 +5V.

6 +5V CONNECTOR PINS ARE: P1-A16, A28, A29, A51, B16, B28, B29, B51.

7 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J1-A10, B10.

8 +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4.

9 -15V CONNECTOR PINS ARE: P1-A52, A53, B52, B53.



ADDRESS PROGRAM PLUG

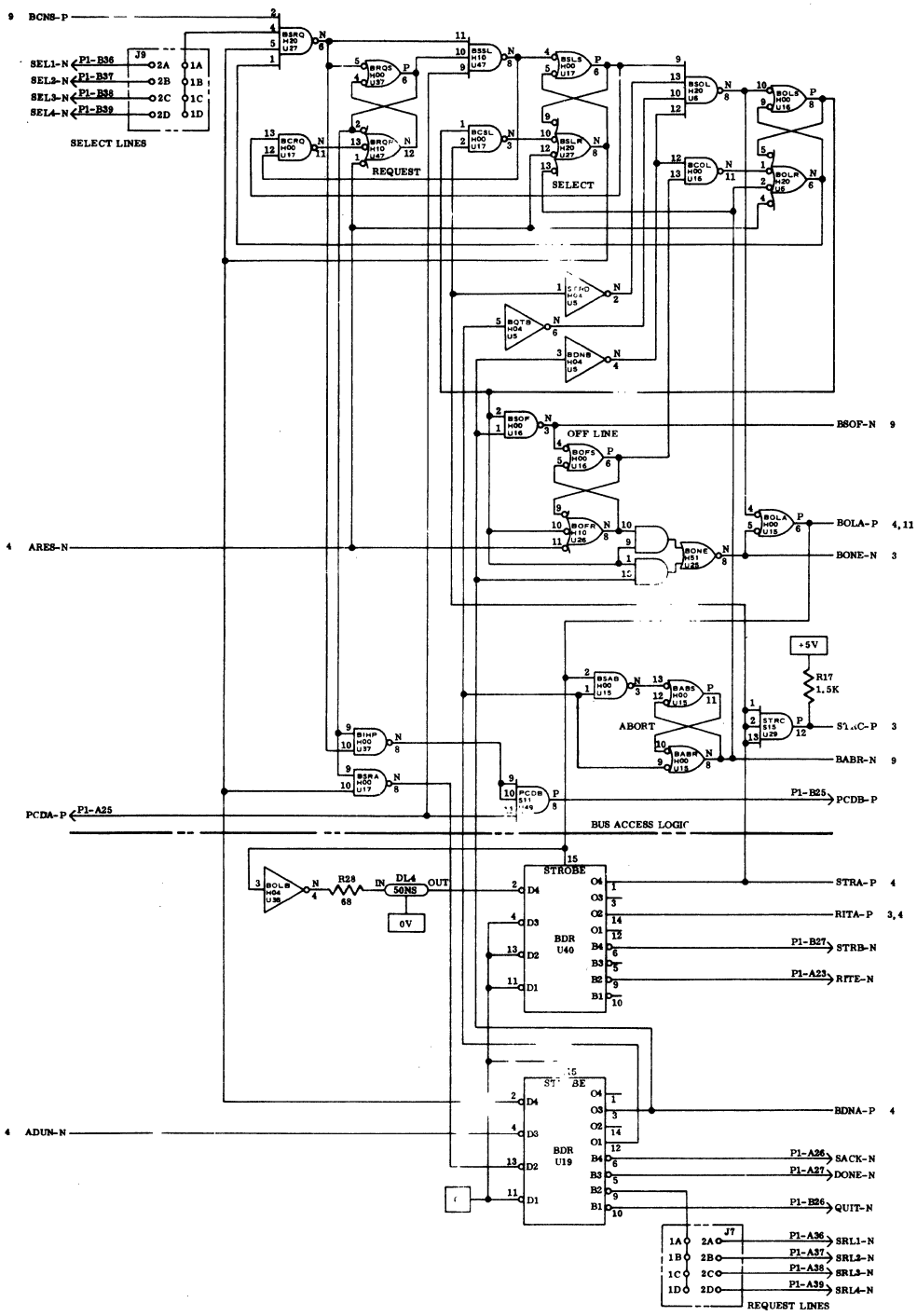
ADDRESS BIT	FROM	CONNECT TO	
		BINARY 0	BINARY 1
4	J6-2A	J6-1A	J6-3A
5	J6-2B	J6-1B	J6-3B
6	J6-2C	J6-1C	J6-3C
7	J6-2D	J6-1D	J6-3D
8	J6-2E	J6-1E	J6-3E
9	J6-2F	J6-1F	J6-3F
10	J6-2G	J6-1G	J6-3G
[illegible]	J6-2H	J6-1H	J6-3H

Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 1 of 11

BUS ACCESS LOGIC FOR CPU INTERRUPT (LD Sheet 2)

A request for a CPU interrupt is placed on line BCNS-P. If the Select line is false (high) and the Select and On-Line flip-flops are reset, the Request flip-flop (BRQ) sets, placing a service request on one of lines SRL1, 2, 3 or 4 on the INFIBUS. Program plug J7 is used to select the Request line and program plug J9 is used to implement the Select line. The Select line going true ANDed with the Precedence Chain pulse (PCDA-P) sets Select flip-flop, BSL, which generates SACK and inhibits the Precedence Chain pulse from propagating down the bus (BIHP-N). When the Strobe (STRA-P) goes false, the On-Line flip-flop (BOL) sets causing the device number to be gated on to the INFIBUS via BOLA-P and BONE-N; and Strobe STRB-N to be asserted after a 50-nanosecond delay. Receiving the Strobe (STRA-P true) resets the Select flip-flop. While the On-Line flip-flop is set, receiving a DONE sets the Off-Line flip-flop (BOF). Receipt of a QUIT at that time sets the Abort flip-flop (BAB) which resets the On-Line and Select flip-flops. The trailing edge of the DONE resets the On-Line flip-flop. Resetting the On-Line flip-flop resets the Off-Line flip-flop.

Signals BOLA-P and BONE-N are true while the On-Line flip-flop is set. The 50-nanosecond ON Strobe allows the device number to be placed on the bus and to settle out.



Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 2 of 11

ADDRESS RECOGNITION LOGIC (LD Sheet 3)

The three 8242 integrated circuit chips are implemented to match the eight programmable bits (A04A-P thru A11A-P) of the address bus. These eight bits, and bits A12A-P thru A15A-P equal to a ONE, comprise the 4502 address. DN01-P thru DN11-P are the programmable lines from plug J6 on sheet 11 that are programmed to the 4502 device number.

Delay is built into strobe circuit STRC-P (i.e. values of R19 and C6) to allow the match signal enough set-up time at the J input of flip-flop AMA before the strobe arrives at the T input. This delay assures address recognition even if the strobe and the address arrive at the BTA simultaneously.

Address bits A01A-P, A02A-P and A03A-P are decoded to address the three registers in the 4502.

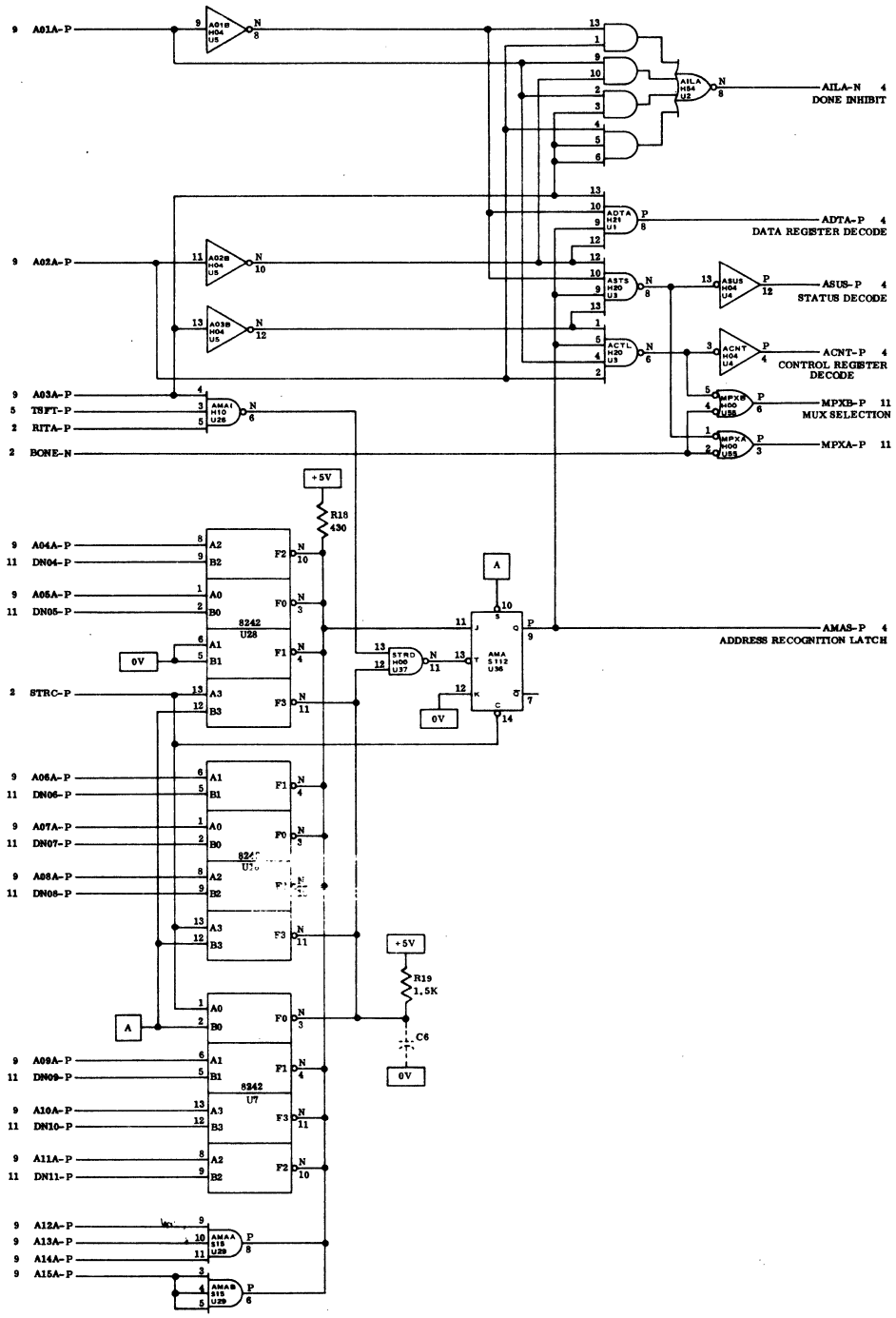
Register	AB03	AB02	AB01	Address Signal
Status	0	0	0	ASUS-P
Control	0	1	1	ACNT-P
Data	1	0	0	ADTA-P

Signal AILA-N is true (low) when any address other than one of the register addresses occurs on lines A01A-P, A02A-P, and A03A-P. AILA-N is false (high) when the address of one of the three registers is on the lines. Lines MPXA-P and MPXB-P drive the data multiplexers shown on LD sheet 11.

MPXA = Device Number + Status

MPXB = Device Number + Control

MPXB-P	MPXA-P	Register Selected
0	0	Data
0	1	Status
1	0	Control
1	1	Device Number



Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 3 of 11

READ/WRITE CYCLE TIMING (LD Sheet 4)

Address match signal AMAS-P, propagates through three 50-nanosecond delay lines, DL1, DL2, and DL3. For a write cycle, RITA-P is true and APLE-P is a 60-nanosecond pulse occurring approximately 60 nanoseconds into the cycle. If one of the three controller registers is addressed, AILA-N is high and flip-flop ADN is set which allows generation of ADUN-N, the Done pulse. The Done pulse is generated approximately 120 nanoseconds after AMAS-P goes true. The Done pulse width is a function of Delay Line DL3 and the propagation delay inherent in inverter ADNA-N.

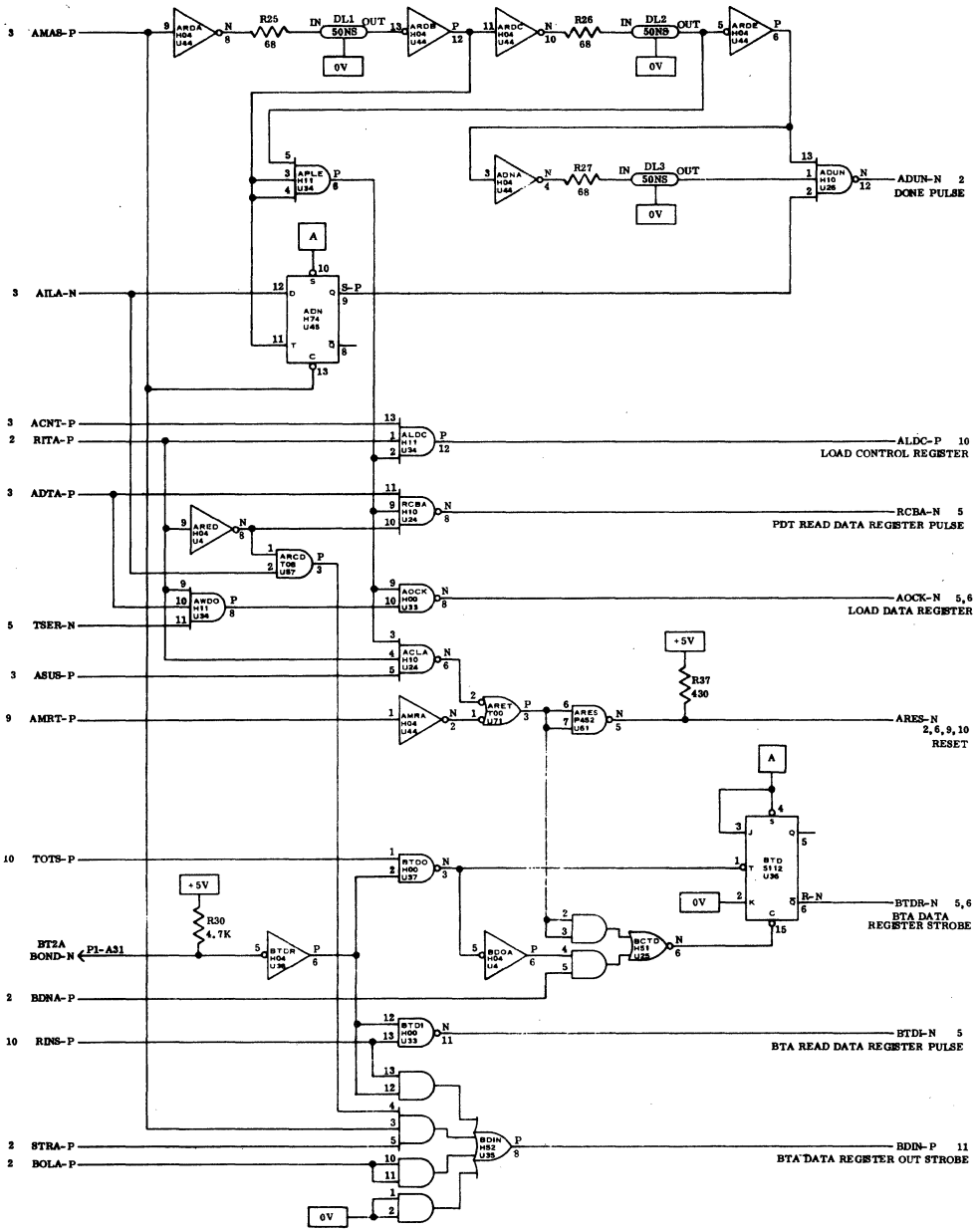
APLE-P is used to: load the control register via gate ALDC, load the data register via gate AOCK, reset the controller via gate ACLA, and clear control logic during a Read of the data register via gate RCBA.

When the 4502 is operating with a block transfer adapter (BTA), data register strobe BTDR-N goes low with receipt of BT2A-N (in the output mode), and goes high when a Done is received (BDNA-P). The low-to-high transition is the strobe. Data is taken at the leading edge of Done because it is not guaranteed valid at the receiving device on the trailing edge of Done.

BTDI-N performs the same function for BTA input operations as RCBA-N does for PDT input mode functions.

Gate BDIN-P, the data out strobe for the INFIBUS gates the device number (BOLA-P), gates data, control, or status during address recognition read cycle, and gates data during BTA input transfers.

PSB



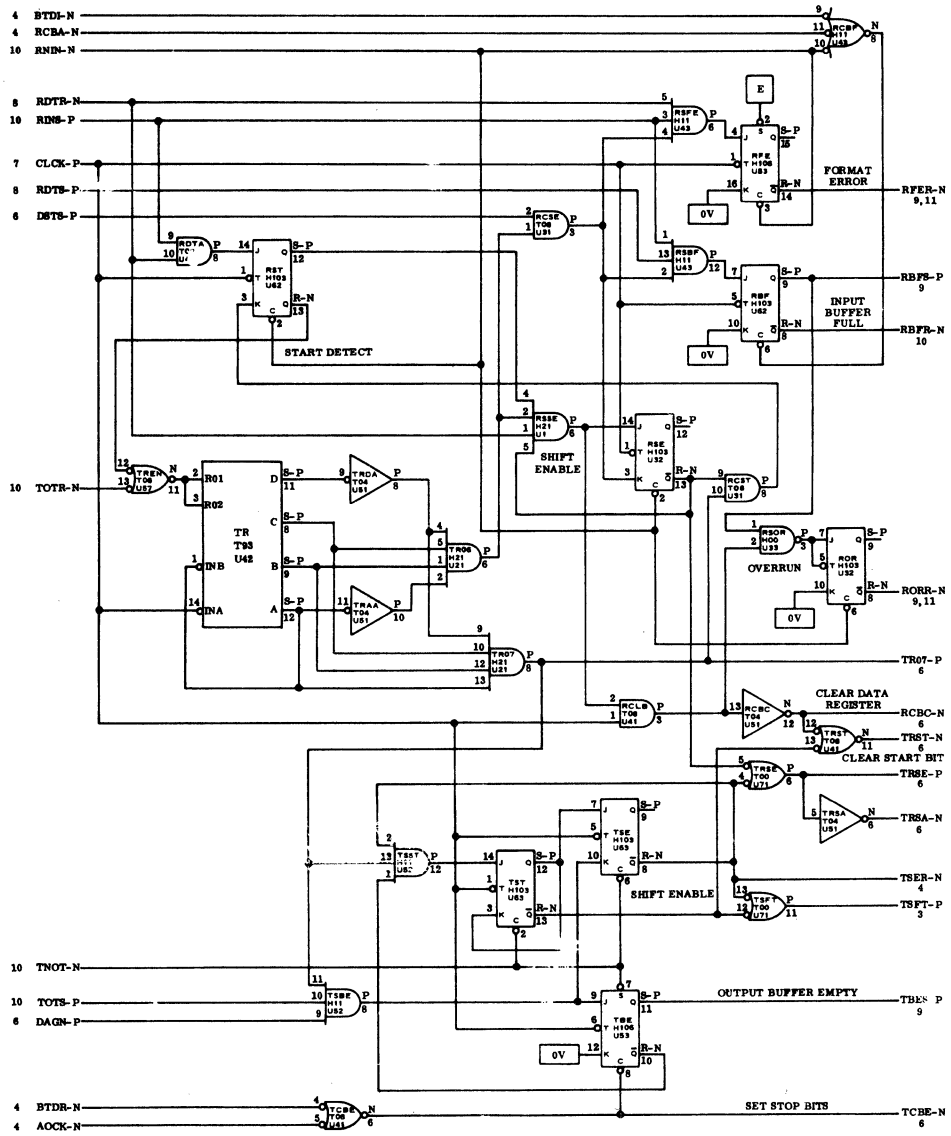
Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 4 of 11

ASYNCHRONOUS RECEIVE/TRANSMIT CONTROL LOGIC AND DATA SHIFT REGISTER (LD Sheets 5 and 6)

When the controller is in the input mode, RNIN-N is high and TNOT-N is low. Clock CLCK-P is 16 times faster than the incoming data. Data on the line is initially a ONE making RDTR-N low. Flip-flop RST sets on a ONE-to-ZERO change of the incoming data. Once set, RST enables the counter clock (TR). Seven counts later the data is checked again to be low (start bit). If still low the transition was a valid Start bit and the Shift Enable flip-flop (RSE) is set. At the end of the eighth count (State 7), data is shifted into the shift register and once every sixteen counts thereafter until the correct number of data bits is shifted into the data register. After all the data is shifted into the register, DSTS-P goes true. DSTS and State 6 reset the Shift Enable flip-flop. After RSE resets with the next clock, RST and counter reset TR permitting another start bit to be detected and a new character to be assembled. If the data coming into the controller is not a ONE (RDTR-N high) when DSTS-P is true, the Format Error flip-flop (RFE) sets. If the data coming in is a ONE (stop bit) (RDTS-P high), the Buffer Full flip-flop (RBF) sets.

The correct number of data bits received is determined as follows: When the Shift Enable flip-flop sets, the shift register is cleared (all ZEROS) via RCBC-N and the Start Bit cell DST is cleared via TRST-N. Data is inverted when received and right-shifted into the 74198 register. Since a data ZERO is shifted into the register as a ONE and the register starts out as all ZEROs, the first ONE to be detected in cell DST is the Start bit (zero data bit - first bit received of each character). The Start bit being the first bit of each character indicates that the remaining bits are data. For eight-bit data, the data shifts through all eight cells of the shift register. For five-bit data, the data shifts right through the five most significant positions of the register and from DO3S-P to the Start cell, DST. The cells not used contain ZEROs.

When the data is read out of the data register, RBF is reset via BTDI-N for a BTA master cycle, or via RCBA-N for a PDT slave cycle. If the data is not



ASYNCHRONOUS RECEIVE/TRANSMIT CONTROL LOGIC

Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 5 of 11

read out before new data starts to shift into the register, the Over-run flip-flop, ROR, sets.

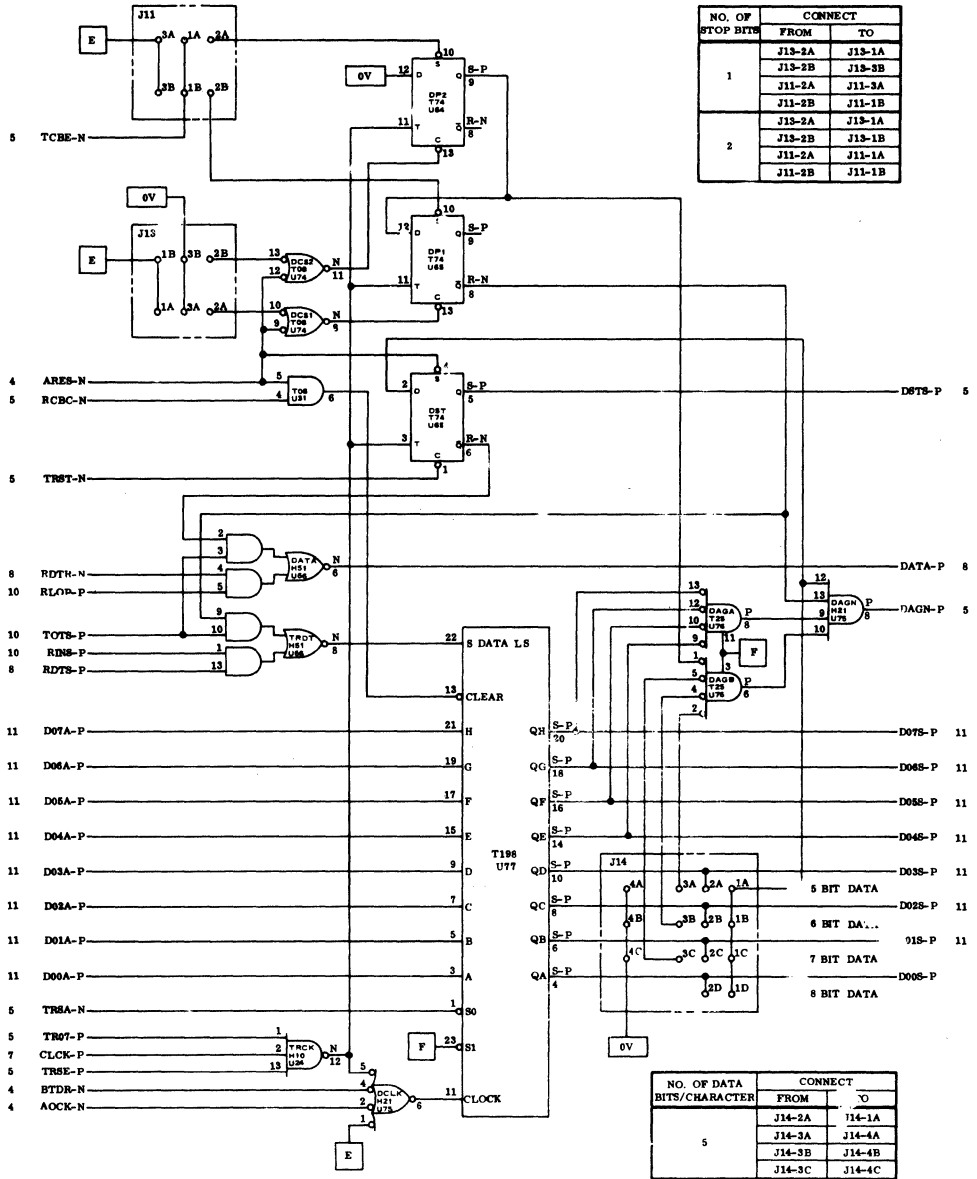
When the controller is in the output mode, initially the data buffer register is empty and the Buffer Empty flip-flop, TBE, is set to a ONE. When data is loaded into the data register via AOCK-N for a PDT slave cycle or via BTDR-N for a BTA master cycle, the Buffer Empty flip-flop is reset. The next State 7 ANDed with clock time causes flip-flop TST to set. One clock time later, flip-flop TSE, the Transmitter Shift Enable flip-flop, sets to a ONE and TST resets. TST high causes the Start bit DST to be cleared to a ZERO. Data is shifted right each counter State 7 from then on until the data register, including Stop bit cells DP1 and DP2 contain ZEROS (except for the least significant bit used which is a ONE). When this occurs, DAGN-P goes true causing the Shift Enable flip-flop to be reset as the last Stop bit is shifted into DST. TBE goes true as TSE resets indicating a request for more data.

The number of Stop bits per character is selected by program plugs J11 and J13. When the data register is loaded, pulse TCBE-N is generated setting either one or two of bits DP1 and DP2. As data is shifted right, ZEROs are shifted into DP2.

For data containing less than eight bits, the most significant bits of the data register are used. For example: five-bit data uses bits D07S, D06S, D05S, D04S, D03S but not D02, D01, D00. Data shifts through these low-order bits but also shifts out of D03S-P into DST. The decode for all ZEROs and ONE is ZEROs on DP2, DP1, D07S-D02S and a ONE in D03S-P. Program plug J14 selects the number of bits per character and connects the decode.

Gate DATA-P is the transmitted data line going to the interface drivers. Data goes out either through DST in the output mode or is looped from the receiver (RDTR-N) if Input-with-Echo is used, RLOP-P.

Signal TSFT-P inhibits the address recognition logic if a Write Data Register instruction is received while data is being transmitted.



NO. OF STOP BITS	CONNECT FROM	CONNECT TO
1	J13-2A	J13-1A
	J13-2B	J13-3B
	J11-2A	J11-3A
	J11-2B	J11-1B
2	J13-2A	J13-1A
	J13-2B	J13-1B
	J11-2A	J11-1A
	J11-2B	J11-1B

NO. OF DATA BITS/CHARACTER	CONNECT FROM	CONNECT TO
5	J14-2A	J14-1A
	J14-3A	J14-4A
	J14-3B	J14-4B
	J14-3C	J14-4C
6	J14-2A	J14-3A
	J14-2B	J14-1B
	J14-3B	J14-4B
	J14-3C	J14-4C
7	J14-2A	J14-3A
	J14-2B	J14-3B
	J14-2C	J14-1C
	J14-3C	J14-4C
8	J14-2A	J14-3A
	J14-2B	J14-3B
	J14-2C	J14-3C
	J14-2D	J14-1D

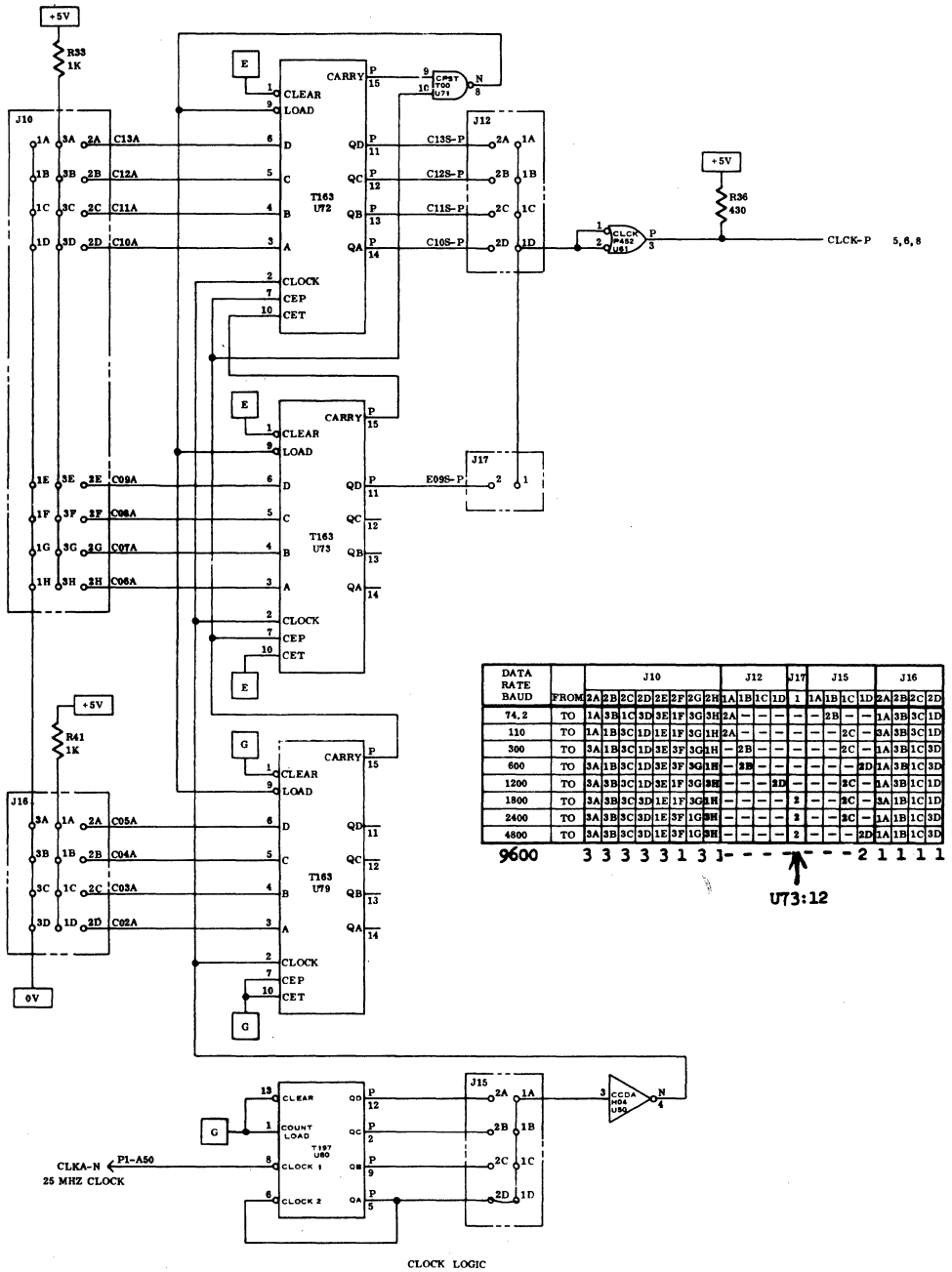
Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 6 of 11

CLOCK LOGIC (LD Sheet 7)

The four counter integrated circuits divide down the 25-megahertz clock on the INFIBUS, CLKA-N, to a frequency that is sixteen times the desired data rate. Counter T197 first divides the 25 megahertz frequency by 2, 4, 8, or 16 and this signal, CCDA-N, clocks a programmable 12-bit counter. The 12-bit counter is preset to a count and counts up to all ONEs. When it reaches the all ONEs condition, CPST-N goes true and on the next CCDA-N the counter presets. The highest order bit that changes from a ZERO to a ONE and back again, is connected to CLCK the Controller Clock Line. The preset is the two's complement of the count. For example, to get the frequency for 110 Baud, the data bit time is 9.09 milliseconds. A sixteen-times clock has a period of 0.568 milliseconds. If a divide-by-four or 160 nanosecond clock is used, then the count in decimal is $\frac{568,000}{160} = 3,551$. Converted to hexadecimal, this count $3,551_{10} = DDF_{16}$ and its two's complement is 221_{16} — the programmed preset.

The table on sheet 7 shows how to program plugs J10, J12, J15, J16, and J17 for the most popular data rates. Rates above 4800 are possible but pads located at U73 pins 12, 13, and 14 must be connected to gate CLCK.

PSB



DATA RATE BAUD	FROM	J10								J12				J17	J15				J16			
		2A	2B	2C	2D	2E	2F	2G	2H	1A	1B	1C	1D	1	1A	1B	1C	1D	2A	2B	2C	2D
74.2	TO	1A	3B	1C	3D	3E	1F	3G	3H	2A	–	–	–	–	–	2B	–	–	1A	3B	3C	1D
110	TO	1A	1B	3C	1D	1E	1F	3G	1H	2A	–	–	–	–	–	–	2C	–	3A	3B	3C	1D
300	TO	3A	1B	3C	1D	3E	3F	3G	1H	–	2B	–	–	–	–	–	2C	–	1A	3B	1C	3D
600	TO	3A	1B	3C	1D	3E	3F	3G	1H	–	2B	–	–	–	–	–	–	2D	1A	3B	1C	3D
1200	TO	3A	3B	3C	1D	3E	1F	3G	3H	–	–	–	2D	–	–	–	2C	–	1A	3B	1C	1D
1800	TO	3A	3B	3C	3D	1E	1F	3G	1H	–	–	–	–	2	–	–	2C	–	3A	1B	1C	1D
2400	TO	3A	3B	3C	3D	1E	3F	1G	3H	–	–	–	–	2	–	–	2C	–	1A	1B	1C	3D
4800	TO	3A	3B	3C	3D	1E	3F	1G	3H	–	–	–	–	2	–	–	–	2D	1A	1B	1C	3D
9600		3	3	3	3	3	1	3	1	–	–	–	–	–	–	–	–	2	1	1	1	1

U73:12

Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 7 of 11

CONTROL LOGIC (LD Sheet 8)

The data modem automatic answer logic is shown on the top one-third of LD sheet 8. Control signal, Terminal ready (J1-A5), is required to enable type 103A2 and 202C data sets to enter the data mode. The automatic call answer logic works in the following manner.

The Data Set Ring Indicator signal goes high each time the telephone circuit rings as shown in figure 1. This clears control flip-flop TRR, turns on the Terminal Ready driver signal, and starts the five-second one-shot timer TRT when the Type 804 control unit answers the call and holds ring indicator (J1-A7) low. The data set supplies a positive on indication, Clear-To-Send (J1-A9), when the carrier signal of the calling data terminal is detected. This enables gate TCTA-N to pass transmitter clock pulses through the gate to the low input of one-shot TRT. These clock pulses continually retrigger the one-shot, holding it on, thus holding the Terminal Ready signal on. Failure to receive the Clear-To-Send signal (for example number dialed by a non-data terminal user) from the data set, inhibits retriggering TRT and causes the Terminal-Ready signal to be off in approximately 5 seconds. This sets TRR that releases the Terminal-Ready holding signal, and the line disconnects after the caller hangs up. The line is also disconnected similarly at the end of a data call when the Clear-To-Send signal drops as the remote calling terminal goes on hook.

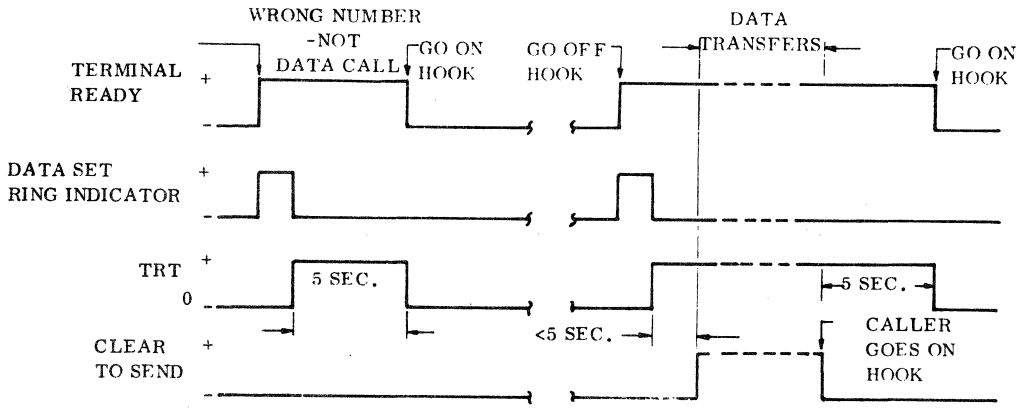


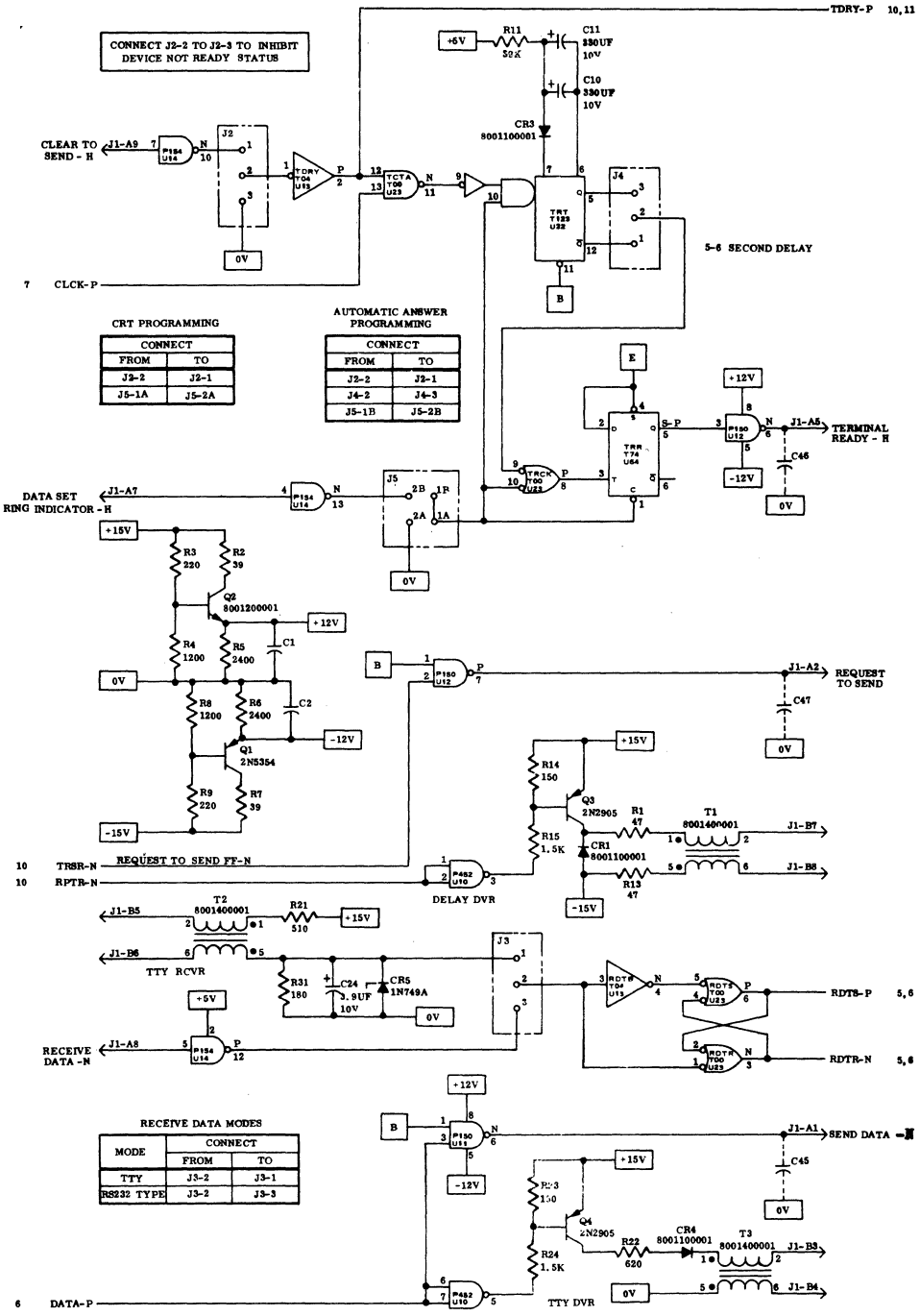
Figure 1. SUE 4502 Automatic Answer and Disconnect Timing

When used for manual call answering, hard-wired terminals, with non-dial-up 103F or 202D dedicated line communications, and CRT terminals, J5-2A is connected to J5-1A forcing the Terminal Ready signal to remain on at all times. The Clear-To-Send signal, when false, is used to inhibit initiation of a CPU interrupt in output mode and to inhibit the PDT status bit on output. In this way the 4502 can be placed in the output mode with interrupts and can wait for the computer to be called by a remote terminal. When the automatic answer sequence is complete, TDRY-P goes high, the PDT status bit goes true, and a CPU interrupt is generated. The interrupt indicates the start of the output transmission. If placed in the input mode, when the computer is called, receipt of the incoming data generates an interrupt.

RS232-C drivers (75150 integrated circuit components) require ±12 volts. The power supply shown in the center of LD sheet 8 converts ±15 volts to ±12 volts.

Shown on the bottom one-half of LD sheet 8 are the Teletypewriter (TTY) data driver, TTY paper tape reader relay driver, and the TTY data receiver. Of the three RS232-C receivers two are fail-safe receivers — Clear-To-Send and Data Set Ring Indicator. The data receiver does not use failsafe feature, therefore, it has a wide hysteresis loop.

PSB



Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 8 of 11

ADDRESS BUS DRIVERS/RECEIVERS (LD Sheet 9)

Gate BTRQ is the PDT status logic that also drives BT1A-N, the Data Transfer Request line. The gate is true when in the input mode (RINS-P) and the data register is full (RRFS-P), or when in the output mode with the device ready (TAOK-P) and the data register empty (TBES-P).

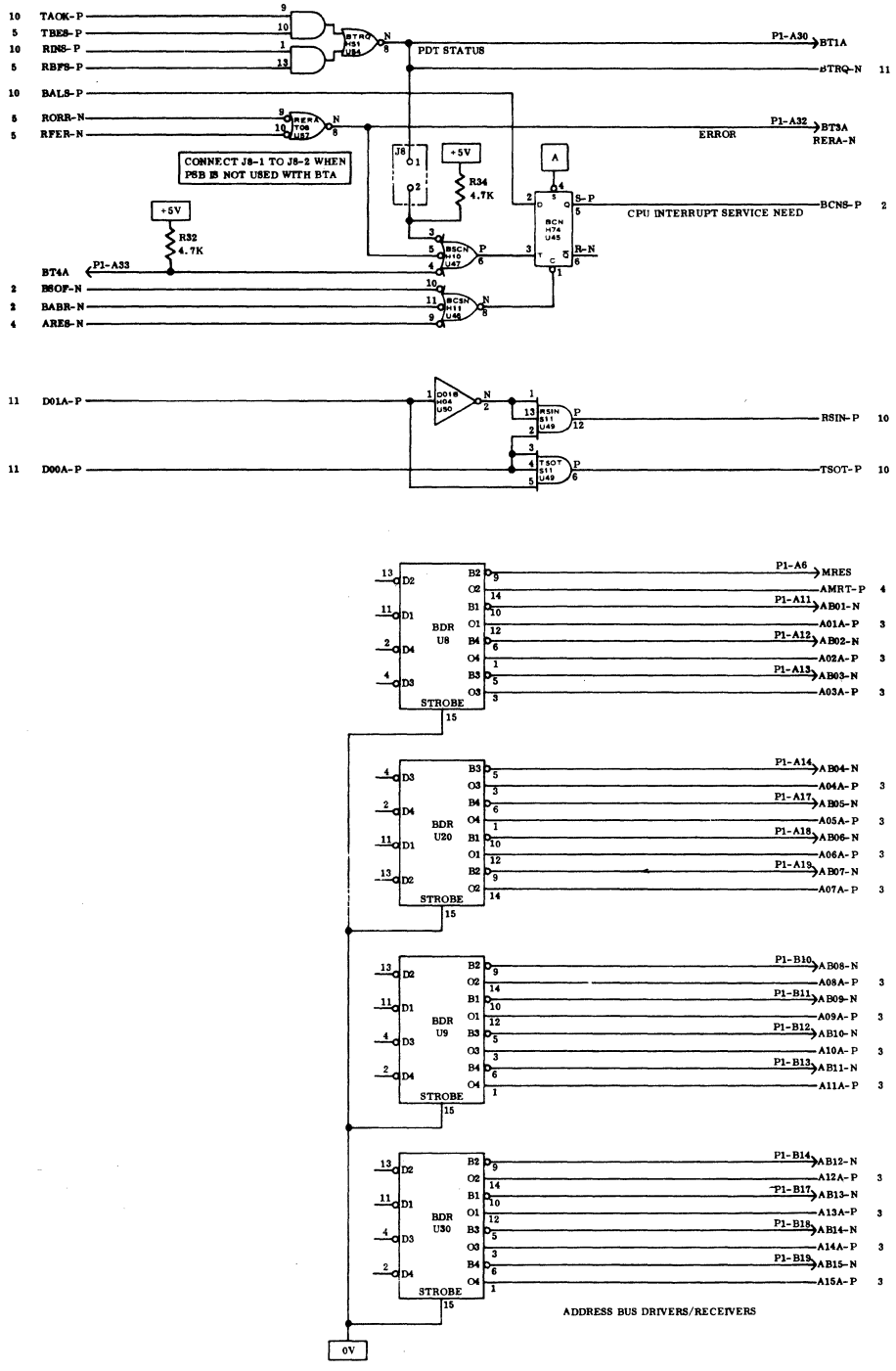
BCN is the CPU Interrupt Service Need flip-flop that initiates an interrupt when set. BCN is set by the PDT status line if jumper J8-1 is connected to J8-2 (BTA not used with 4502), by an error (RERA), or by a request from the BTA (BT4A-N). BCN is reset by an Abort condition (BABR-N), a Done is received when on line (BSOF-N), or by a reset (ARES-N).

Error line RERA-N drives BT3A-N going to the BTA. Two error conditions activate gate RERA: overrun (RORR-N) and format error (RFER-N).

RSIN-P is the input mode decode received from the INFIBUS: bit 0 = 1, bit 1 = 0. TSOT-P is the output mode decode from the INFIBUS: bit 0 = 1, bit 1 = 1.

LD sheet 9 also shows the Address Bus Receivers. AB01-N through AB15-N are the INFIBUS address lines and A01A-P through A15A-P are the receiver address lines.

PSB



Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 9 of 11

CONTROL REGISTER (LD Sheet 10)

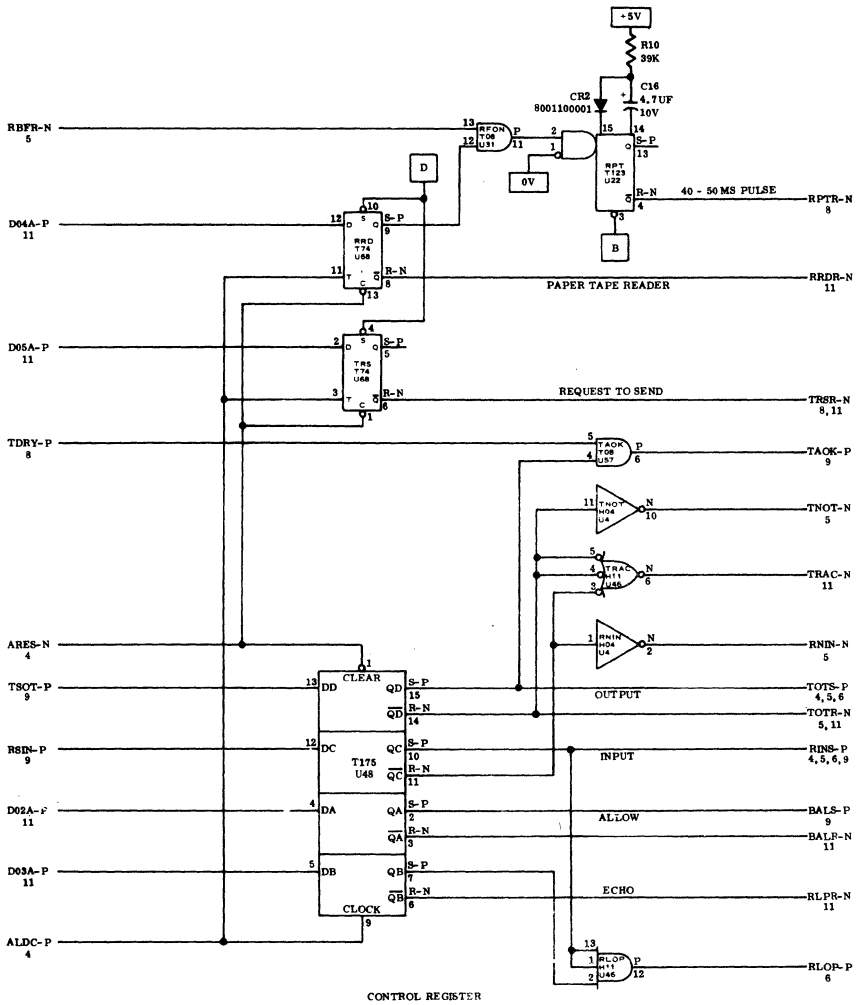
The control register is loaded during an address recognition cycle when a MOVW operation to the control register address is executed.

RLPR-N	Loop or echo bit
BALS-P/ BALR-N	Allow/inhibit interrupts
RINS-P	Input mode, receive
TOTS-P/ TOTR-N	Output mode, transmit
TRSR-N	Output of control flip-flop for driving Request-To-Send line
RRDR-N	TTY Paper Tape Reader enable

TRAC-N is the OR of the input and output mode bits that mean Not Idle.
TAOK-P = Output Device Ready. RLOP-P true for input mode and echo bit set.

Gate RFON-P, when true, triggers one-shot RPT which remains on for 40 to 50 milliseconds. This pulse turns off the relay drive circuit shown on LD sheet 8, turning off the relay in the Teletypewriter. This turns on the reader long enough to advance one frame. Emptying the data register (RBFR-N true) triggers the one-shot again advancing the tape one more frame.

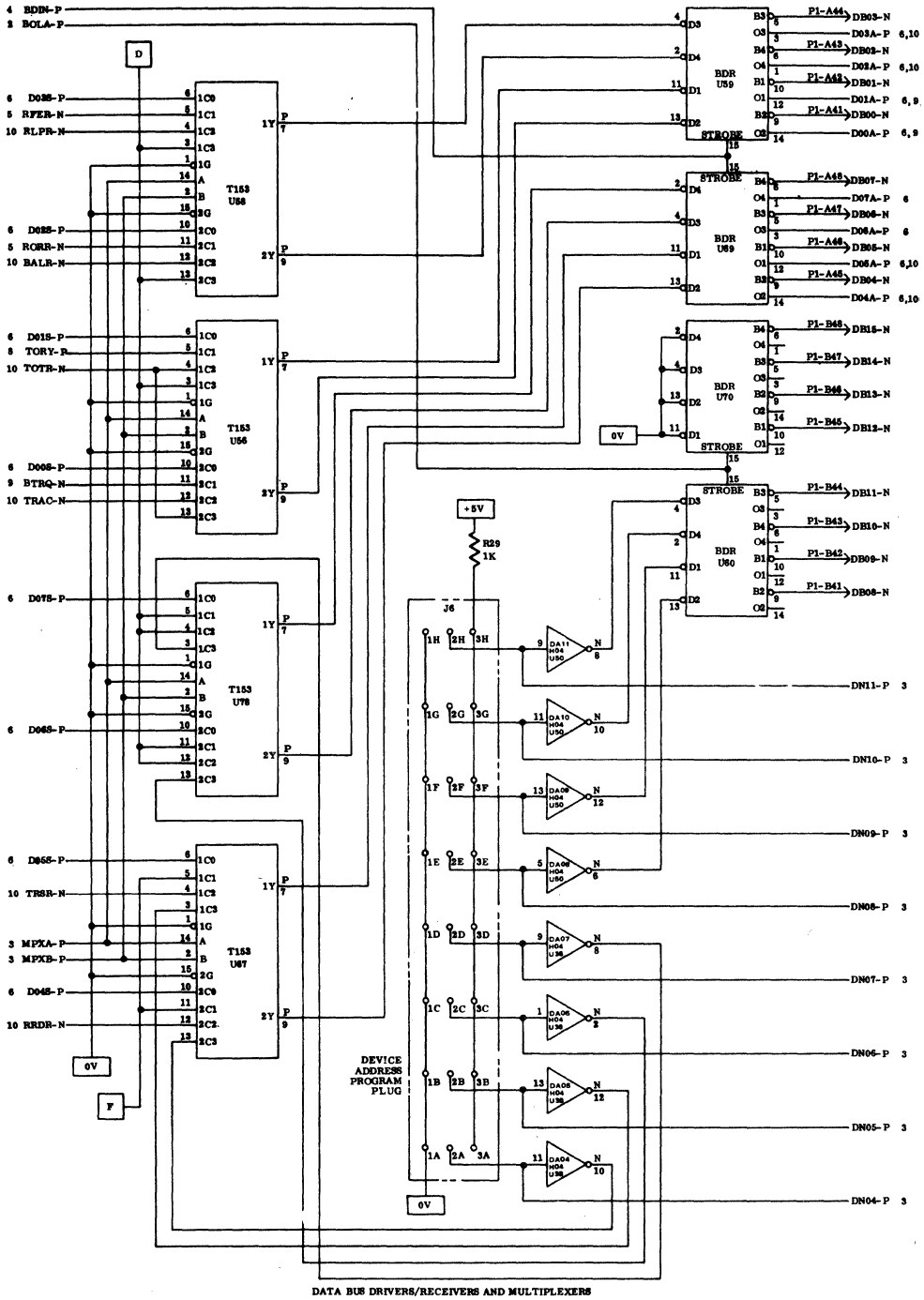
PSB



Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 10 of 11

DATA BUS DRIVERS/RECEIVERS AND MULTIPLEXERS (LD Sheet 11)

Plug J6 is the device number program plug on which the 4502 Controller device address is encoded. Bits DB00-N thru DB15-N are the INFIBUS data lines and D00A-P thru D15A-P the data lines from receivers. Components U56, U58, U67 and U78 are the data multiplexers that provide 1 to 4 selection of status, control, or data outputs to the data lines.



Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 11 of 11

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002138-1		PSB-CKT CARD ASSY		USED ON SUE 4502	1
002		001	0001		1001004752-1		PRINTED WRG BD, PSB			2
003		000								3
004		002	0001		RL07S390G		RESISTOR	MIL-R-22684/1	R2,7 .5 IS	4
005		002	0001		RL07S221G		RESISTOR	MIL-R-22684/1	R3,9 .5 IS	5
006		003	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R30,34,32 .5 IS	6
007		002	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R14,23 .5 IS	7
008		004	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R17,19,15,24 .5 IS	8
009		001	0001		RL07S621G		RESISTOR	MIL-R-22684/1	R22 .5 IS	9
010		002	0001		RL07S470G		RESISTOR	MIL-R-22684/1	R1,13 .5 IS	10
011		001	0001		RL07S511G		RESISTOR	MIL-R-22684/1	R21 .5 IS	11
012		001	0001		RL07S181G		RESISTOR	MIL-R-22684/1	R31 .5 IS	12
013		002	0001		RL07S393G		RESISTOR	MIL-R-22684/1	R11,10 .5 IS	13
014		002	0001		RL07S242G		RESISTOR	MIL-R-22684/1	R5,6 .5 IS	14
015		003	0001		RL07S431G		RESISTOR	MIL-R-22684/1	R18,37,36 .5 IS	15
016		004	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R28,25,26,27 .5 IS	16
017		010	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R41,33,29,12,16, 20,35,38,39,40 .5 IS	17
018		002	0001		RL07S122G		RESISTOR	MIL-R-22684/1	R4,8 .5 IS	18
019		000								19
020	F	002	0001		1005000041-1		TRANSIPAD		(T05)	20
021	F	033	0001		8001300101-1		CAPACITOR		C1,2,3,4,7,8,12, 13,14,15,17,18, 19,21,22,26,27, 28,29,30,31,C33 THRU C44	21
022		003	0001		8001300311-2		CAPACITOR		C9,20,23 .8 IS	22
023		001	0001		8001300308-1		CAPACITOR		C24 .65 IS	23
024		002	0001		MTP-337M010P1C	90201	CAPACITOR	MALLORY CAP. CO.	C10,11 1.00 IS	24
025		003	0001		8001300333-2		CAPACITOR		C5,25,32 .80 IS	25
026		001	0001		8001300309-2		CAPACITOR		C16 .65 IS	26
027		000	0001				CAPACITOR		C8,45,46,47 .25 IS NOTE 211	27
028		001	0001		2N5354		TRANSISTOR		Q1	28
029	E	001	0001		8001200001-1		TRANSISTOR		Q2	29
030		002	0001		2N2905		TRANSISTOR		Q3,4	30
031		000	0001							31
032	E	004	0001		8001100001-1		DIODE		CR1,2,3,4 .5 IS	32
033		001	0001		1N749A		DIODE, ZENER		CR5 .5 IS	33
034		000								34

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035	E	003	0001		8001400001-1		TRANSFORMER, PULSE		T1,2,3	35
036		000								36
037	F	135	0001		100500076 1		PIN, TERMINAL		NOTE 210	37
038	F	002	0001		8(1800072-1		ICP		U23,71 (7400)	38
039	F	002	0001		8001800076-1		ICP		U13,51 (7404)	39
040		000								40
041	F	003	0001		8001800099-1		ICP		U64,65,68 (7474)	41
042	F	001	0001		8001800110-1		ICP		U42 (7493)	42
043	F	006	0001		8001800042-1		ICP		U15,16,17,33,37,55 (74H00)	43
044	F	005	0001		8001800044-1		ICP		U4,5,38,44,50 (74H04)	44
045	F	003	0001		8001800046-1		ICP		U24,26,47 (74H10)	45
046	F	004	0001		8001800047-1		ICP		U34,43,46,52 (74H11)	46
047	F	003	0001		8001800048-1		ICP		U3,6,27 (74H20)	47
048	F	003	0001		8001800049-1		ICP		U1,21,75 (74H21)	48
049	F	003	0001		8001800054-1		ICP		U25,54,66 (74H51)	49
050	F	001	0001		8001800057-1		ICP		U2 (74H54)	50
	F	003	0001		8001800069-1		ICP		U32,62,63 (74H103)	51
052	F	001	0001		8001800070-1		ICP		U53 (74H106)	52
053		004	0001		8001803126-1		ICP		U31,41,57,74 (7408)	53
054	F	001	0001		8001803134-1		ICP		U76 (7425)	54
055		002	0001		SN 5150P	01295	ICP	TEXAS INSTR INC	U11,12	55
056	F	001	0001		8001800055-1		ICP		U35 (74H52)	56
057	F	001	0001		8001803204-1		ICP		U29 (74S15)	57
058	F	004	0001		8001803165-1		ICP		U56,58,67,78 (74153)	58
059	F	001	0001		8001803194-1		ICP		U80 (74197)	59
060	F	003	0001		8001803173-1		ICP		U72,73,79 (74163)	60
061	F	001	0001		8001803181-1		ICP		U48 (74175)	61
062	F	001	0001		8001803155-1		ICP		U22 (74123)	62
063	F	001	0001		8001803195-1		ICP		U77 (74198)	63
064	F	001	0001		8001803121-1		ICP		U45 (74H74)	64
065	F	001	0001		8001803203-1		ICP		U49 (74S11)	65
066		002	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U10,61	66
067		001	0001		SN75154N	01295	ICP	TEXAS INSTR INC	U14	67
068		003	0001		N8242A	18324	ICP	SIGNETICS	U7,18,28	68
069	F	001	0001		8001803212-1		ICP		U36 (74S112)	69
070		010	0001		8001800123-1		ICP		U8,9,19,20,30,40,59,60,69,70 (BDR)	70

PSB

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
071	F	004	0001		8001600008-1		DELAY LINE, FIXED		DL1,2,3,4 (5ONS)	71
072		001	0001		3428-1002	26066	CONNECTOR, RT ANGLE	3M CO	J1 20 CONTACT RECEPTACLE	72
073		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		73

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002138-10		PSB-CKT CARD ASSY		USED ON SUE 4630	1
002		001	0001		2001002138-1		PSB-CKT CARD ASSY			2
003	F	075	0001		9003400417-7		WIRE, INSULATED		30AWG APPROX INCH REQD	3
004		REF	0001		LD2001002138-1		LOGIC DIAGRAM, PSB			4
005		005	0001		9003400417-1		WIRE, INSULATED		30AWG APPROX INCH REQD	5

WIRE LIST

FROM	TO	FIND NO.
J13-2A	J13-1A	3
J13-2B	J13-1B	3
J11-2A	J11-1A	3
J11-2B	J11-1B	3
J14-2A	J14-3A	3
J14-2B	J14-3B	3
J14-2C	J14-3C	3
J14-2D	J14-1D	3
J10-2A	J10-1A	3
J10-2B	J10-1B	3
J10-2C	J10-3C	3
J10-2D	J10-1D	3
J10-2E	J10-1E	3
J10-2F	J10-1F	3
J10-2G	J10-3G	3
J10-2H	J10-1H	3
J12-1A	J12-2A	3
J15-1C	J15-2C	3
J16-2A	J16-3A	3
J16-2B	J16-3B	3
J16-2C	J16-3C	3
J16-2D	J16-1D	3
J3-2	J3-1	5
J2-3	J2-2	5

PSB

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002138-11		PSB-CKT CARD ASSY		USED ON SUE 4640	1
002		001	0001		2001002138-1		PSB-CKT CARD ASSY			2
003	F	075	0001		9003400417-7		WIRE, INSULATED		30AWG APPROX INCH REQD	3
004		REF	0001		LD2001002138-1		LOGIC DIAGRAM, PSB			4

WIRE LIST

FROM	TO	FIND NO.
J13-2A	J13-1A	3
J13-2B	J13-1B	3
J11-2A	J11-1A	3
J11-2B	J11-1B	3
J14-2A	J14-3A	3
J14-2B	J14-3B	3
J14-2C	J14-3C	3
J14-2D	J14-1D	3
J10-2A	J10-3A	3
J10-2B	J10-3B	3
J10-2C	J10-3C	3
J10-2D	J10-3D	3
J10-2E	J10-1E	3
J10-2F	J10-3F	3
J10-2G	J10-1G	3
J10-2H	J10-3H	3
J17-1	J17-2	3
J15-1C	J15-2C	3
J16-2A	J16-1A	3
J16-2B	J16-1B	3
J16-2C	J16-1C	3
J16-2D	J16-3D	3
J2-2	J2-1	3
J5-1A	J5-2A	3
J3-2	J3-3	3

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200	REF	0001		SPEC/DWG/STD		NOTE:			200
201	A/R	0001		LECP1049-17		MARKING (IDENTIFY).			201
202	REF	0001				AREA TO BE FREE OF SOLDER.			202
203	REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
204	REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205	REF	0001				MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
206	REF	0001				PROTRUSION (SIDE 2) .075 MAXIMUM.			206
207	REF	0001				SQUARE PAD AND/OR STRIPE DENOTES CATHODE END OF DIODE.			207
208	REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209	REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			209
210	REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			210
211	REF	0001				C6,45,46,47 AND LOCATIONS ARE RESERVED FOR FUTURE DESIGN.			211

PSB

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12-16-74	
B	ECN 0116	2-19-75	SJ/DAF
C	ECN 0257	8-19-75	JSS

PSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN SJ/DAF

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PSB TECHNICAL REF

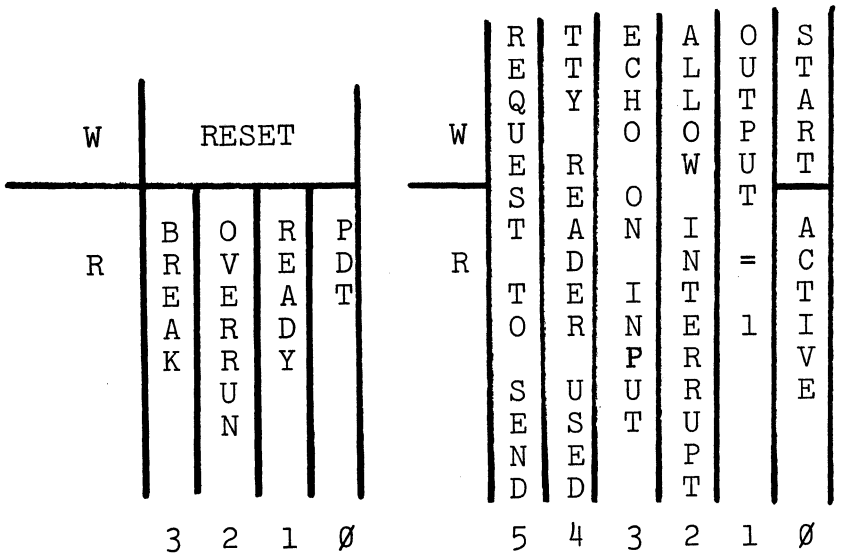
SIZE	CODE IDENT NO.	DRAWING NO.
A		PSB-05

SCALE	REV	SHEET
	C	1 OF 7

Teletype Interface

Status - address FXX0

Control - address FXX6



Switches - none

Jumpers

Address Recognition

Address Bit	From	Connect To	
		Ø	1
4	J6-2A	J6-1A	J6-3A
5	J6-2B	J6-1B	J6-3B
6	J6-2C	J6-1C	J6-3C
7	J6-2D	J6-1D	J6-3D
8	J6-2E	J6-1E	J6-3E
9	J6-2F	J6-1F	J6-3F
10	J6-2G	J6-1G	J6-3G
11	J6-2H	J6-1H	J6-3H
12*	J18-01	J6-1H	J6-3H

* if A12 mod is installed

BUS SERVICE LEVEL

Level	Connect J7 and J9	
	From	To
1	1A	2A
2	1B	2B
3	1C	2C
4	1D	2D
None	J9-1A -	J16-3A

NUMBER OF STOP BITS

Number of Stop Bits	Connect	
	From	To
ONE	J13-2A	J13-1A
	J13-2B	J13-3B
	J11-2A	J11-3A
	J11-2B	J11-1B
TWO	J13-2A	J13-1A
	J13-2B	J13-1B
	J11-2A	J11-1A
	J11-2B	J11-1B

B U S

P	Processor Bus	Remove jumper from J28-1 J18-4
I	M, I/O, or M/I Bus	Connect jumper from J28-1 J18-4

Number of Data Bits Per Character

DATA BITS	CONNECT	
	FROM	TO
FIVE	J14-2A	J14-1A
	J14-3A	J14-4A
	J14-3B	J14-4B
	J14-3C	J14-4C
SIX	J14-2A	J14-3A
	J14-2B	J14-1B
	J14-3B	J14-4B
	J14-3C	J14-4C
SEVEN	J14-2A	J14-3A
	J14-2B	J14-3B
	J14-2C	J14-1C
	J14-3C	J14-4C
EIGHT	J14-2A	J14-3A
	J14-2B	J14-3B
	J14-2C	J14-3C
	J14-2D	J14-1D

PSB

DATA RATE		J10								J12				J17	J15				J16			
BAUD	FROM	2A	2B	2C	2D	2E	2F	2G	2H	1A	1B	1C	1D	1	1A	1B	1C	1D	2A	2B	2C	2D
74.2	TO	1A	3B	1C	3D	3E	1F	3G	3H	2A	--	--	--	--	--	2B	--	--	1A	3B	3C	1D
110	TO	1A	1B	3C	1D	1E	1F	3G	1H	2A	--	--	--	--	--	--	2C	--	3A	3B	3C	1D
300	TO	3A	1B	3C	1D	3E	3F	3G	1H	--	2B	--	--	--	--	--	2C	--	1A	3B	1C	2D
600	TO	3A	1B	3C	1D	3E	3F	3G	1H	--	2B	--	--	--	--	--	--	2D	1A	3B	1C	3D
1200	TO	3A	3B	3C	1D	3E	1F	3G	3H	--	--	--	2D	--	--	--	2C	--	1A	3B	1C	1D
1800	TO	3A	3B	3C	3D	1E	1F	3G	1H	--	--	--	--	2	--	--	2C	--	3A	1B	1C	1D
2400	TO	3A	3B	3C	3D	1E	3F	1G	3H	--	--	--	--	2	--	--	2C	--	1A	1B	1C	3D
4800	TO	3A	3B	3C	3D	1E	3F	1G	3H	--	--	--	--	2	--	--	--	2D	1A	1B	1C	3D
9600	TO	3A	3B	3C	3D	3E	1F	3G	1H	--	--	--	--	*	--	--	--	2D	1A	1B	1C	1D

*J17-1 to U73:12

Data Rate

Receive Data Mode

Mode	Connect	
	From	To
TTY	J3-2	J3-1
RS232	J3-2	J3-3

Auto Answer

Connect	
From	To
J2-2	J2-1
J4-2	J4-3
J5-1B	J5-2B

CRT

Connect	
From	To
J2-2	J2-1
J5-1A	J5-2A

Data Terminal always ready

Auto answer and CRT are not well understood.

Inhibit Device Not Ready
Connect J2-2 to J2-3

BTA Not Used with PSB
Connect J8-1 to J8-2

Inhibit "Data Set Ring Indicator" into PSB, and force "Terminal Ready" out of PSB
Connect J5-1A to J5-2A

Socket		
J1	A1	SEND DATA (EIA)
	B1	
	A2	REQUEST TO SEND (EIA)
	B2	
	A3	
	B3	SEND DATA + (CURRENT LOOP)
	A4	
	B4	SEND DATA - (CURRENT LOOP)
	A5	TERMINAL READY (EIA)
	B5	RECEIVE DATA IN + (CURRENT LOOP)
	A6	
	B6	RECEIVE DATA IN - (CURRENT LOOP)
	A7	DATA SET RING INDICATOR (EIA)
	B7	PTR BUFFER FULL + (CURRENT LOOP)
	A8	RECEIVE DATA IN (EIA)
	B8	PTR BUFFER FULL - (CURRENT LOOP)
	A9	CLEAR TO SEND
	B9	
	A10	GROUND
	B10	GROUND

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	5-7-74	
B	ECN 0116	12-16-75	ST/DRF
C	ECN 0257	8/18/77	JSS/DRF
D	ECN 297	6/7/78	E.C.
E	ECN 3[illegible]	2/23/79	E.C.

PSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN ST/DRF

CHECKER

ENGINEER [illegible]

APP'D FOR REL [illegible]

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PSB MODIFICATION STND

SIZE	CODE IDENT NO.	DRAWING NO.
A		PSB-15

SCALE	REV E	SHEET 1 OF 10

PSB Assembly (Modification)

1. This applies to Lockheed PSB's (BBN #254) of all revision levels.

2. Parts needed:

BBN #	QTY	ITEM
2	4	ULB pin
3	2	14-pin socket (T.I.)
4	1	16-pin socket (T.I.)
61	1	DS8642N (BDR)
83	1	SN7474
130	1	CIT-10 TAG
181	1	6-32 X 1/4 nylon screw
206	1	SN74S15
300	1	double-sided tape (ft)

3. Install plastic tag showing board type and serial number.

4. Drill 1/8" hole centered on the "A" in "P1A1" near the upper right corner of the board, using a sharp drill bit. Check for a short between +5 and ground.

5. Cut the trace between U29:09 and U30:14 on the solder side of the board, as shown in Figure 2.

6. Cut the trace leading from U56:11 to a pad on the component side (see Figure 1). Install a wirewrap pin in the pad. This will be referred to as J47:1.

7. Carefully pull out the rightmost leg of R18 (see Figure 1). Install a wirewrap pin in the hole. This pin will be referred to as J2B:1. Wrap the lead of R18 around the base of the pin and solder it.

8. Install wirewrap pins in the leftmost and rightmost pads of the row between U20 and U30. The leftmost pin is J18:01 and the rightmost is J18:04 (see Figure 1). Also install a wire-wrap pin in pad adjacent to U73:12.

9. Place pieces of double-sided tape in the locations marked U8A, U9A, and U47A in Figure 1.

   Remove the plastic shields from the bottoms of the three I.C. sockets and bend their leads slightly outward. Mount the two 14-pin sockets in locations U8A and U47A, with notches toward the left. Mount the 16-pin socket in U9A in the same way. Be sure that the socket leads are not touching any neighboring I.C.'s.

   Install the BDR in U9A, the 74S15 in U8A, and the 7474 in U47A.

10. Cut and lift the leads at U28:05 and U28:06.

11. Make the following connections:

    a. Jumper U29:09 to U29:10 on the solder side of the board (see Figure 2).

    b. See Figure 1 for locations of the following:

(Note: Connections to U9A, U8A, and U47A should be made by hand-wrapping and soldering to the leads of the sockets. Connections to other I.C.'s should be made by soldering through the holes shared by the I.C. leads if possible. If not possible, they should be made by soldering directly to the I.C. leads. Connections to fingers should be soldered onto the part of the finger which is not gold-plated. Connections to pins should be wire-wrapped.)

PSB

U9A:07	U9A:08
U9A:15	U20:08
U9A:08	U9A:15
U9A:12	U8A:01
U9A:14	U8A:02
U9A:03	U8A:13
U9A:01	U8A:09
U8A:10	U8A:11
U8A:09	U8A:10
U8A:08	U8A:12
U9A:16	U9:16
U8A:14	U8:16
U8A:07	U19:08
U47A:05	U56:11
U47A:03	U36:09
U47A:01	U47A:04
U47A:04	U58:13
U47A:14	U47:14

U47A:07	U57:07	
U9A:05	P1:20	
U9A:06	P1:09	
U9A:10	P2:20	(route through drilled hole)
U9A:09	P2:09	(route through drilled hole)
U30:14	U28:06	(solder to lifted lead)
J18:01	U28:05	(solder to lifted lead)
J18:04	U8A:12	
J47:1	U47A:02	
J14:2A	J14:3A	
J14:2B	J14:3B	
J14:2C	J14:3C	
J14:1D	J14:2D	
J8:1	J8:2	
J2:2	J2:3	
J5:1A	J5:2A	

12. This modification allows for recognition of either 16-bit or 20-bit addresses, latches the state of the PDT bit to allow proper function if parity is used, and configures the card with proper formats and control options (8bits per character, no BTA, no device not ready, always assert terminal ready).

PSB STANDARD MODIFICATION

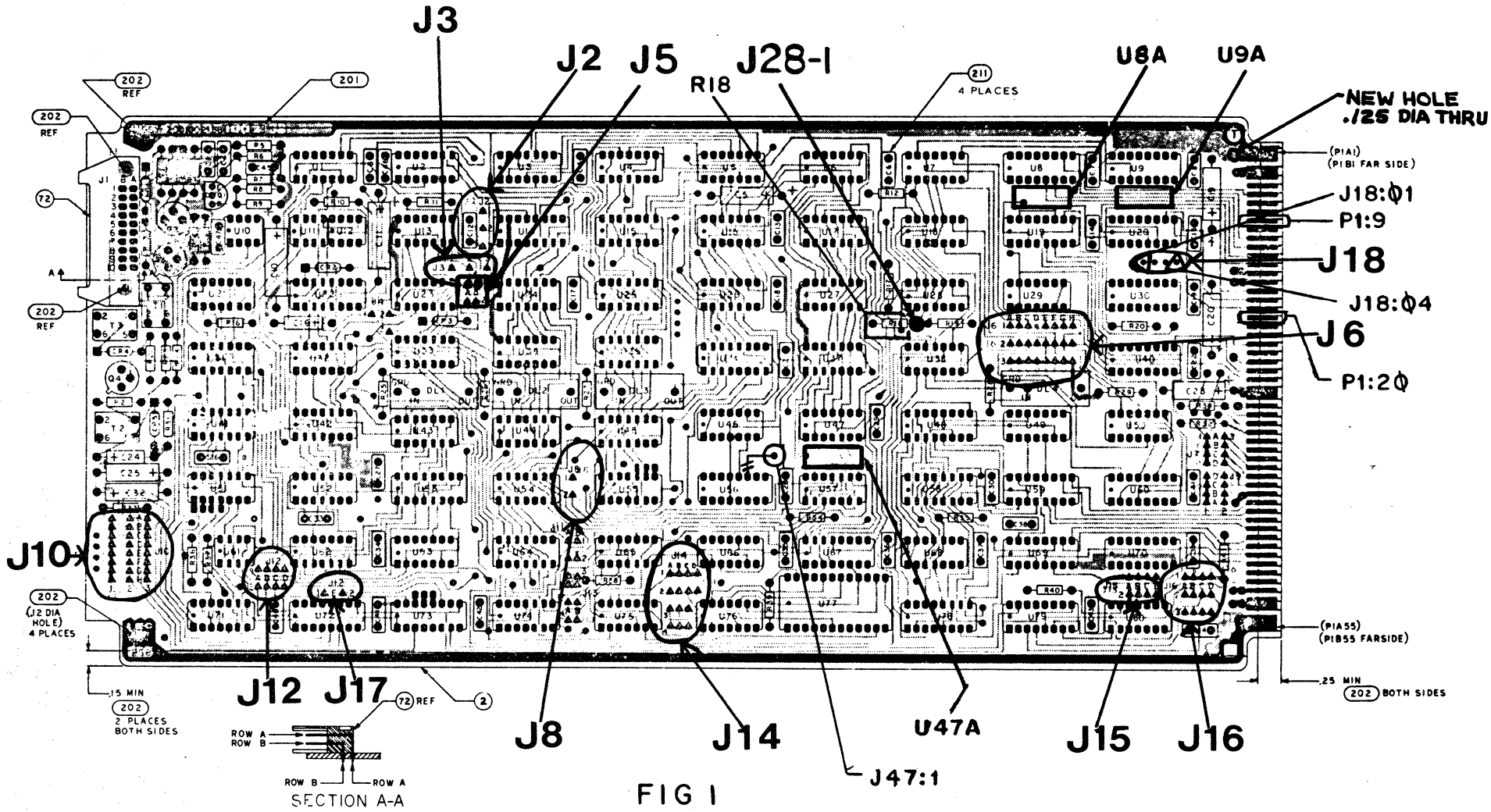


FIG 1

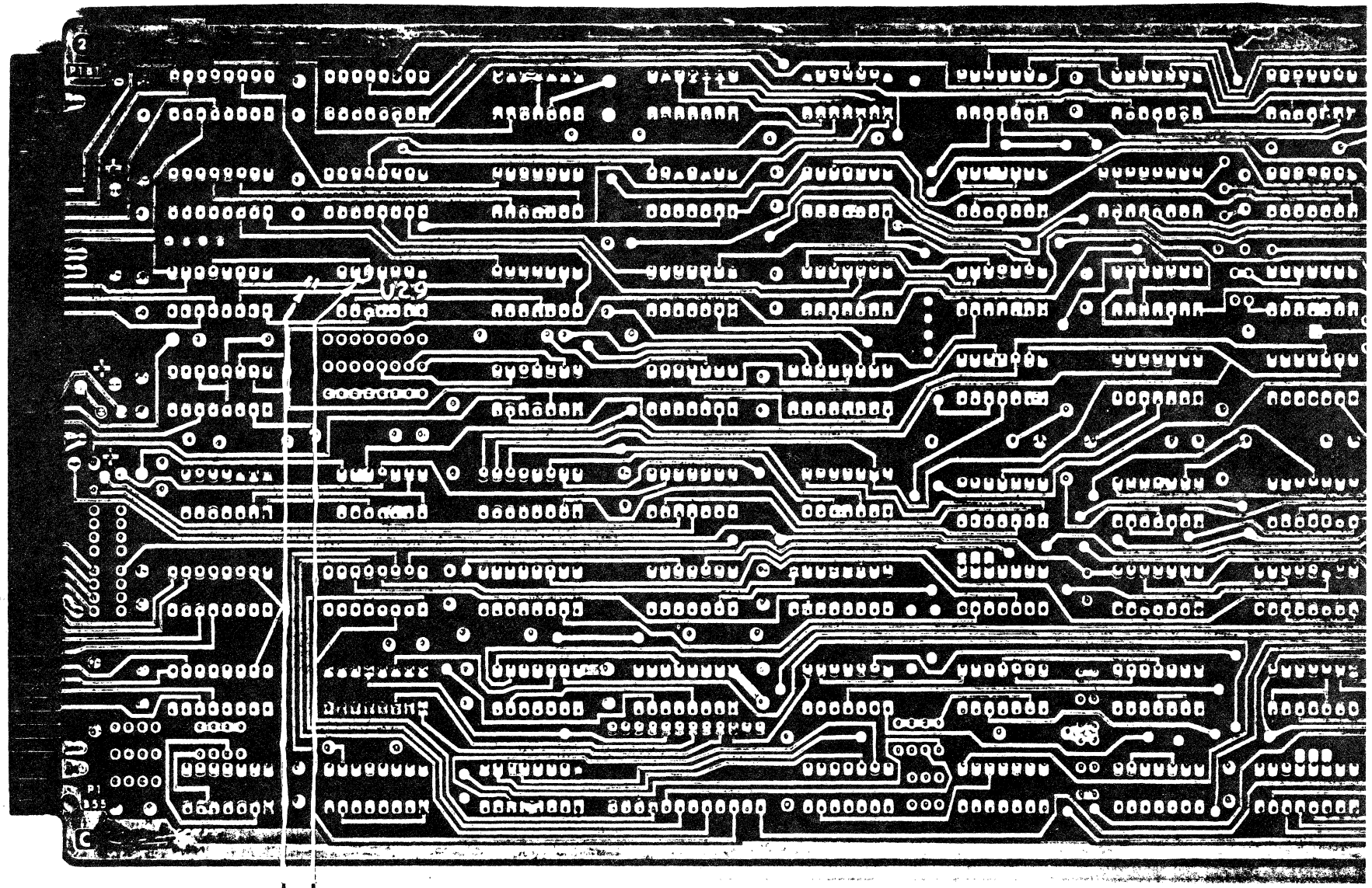
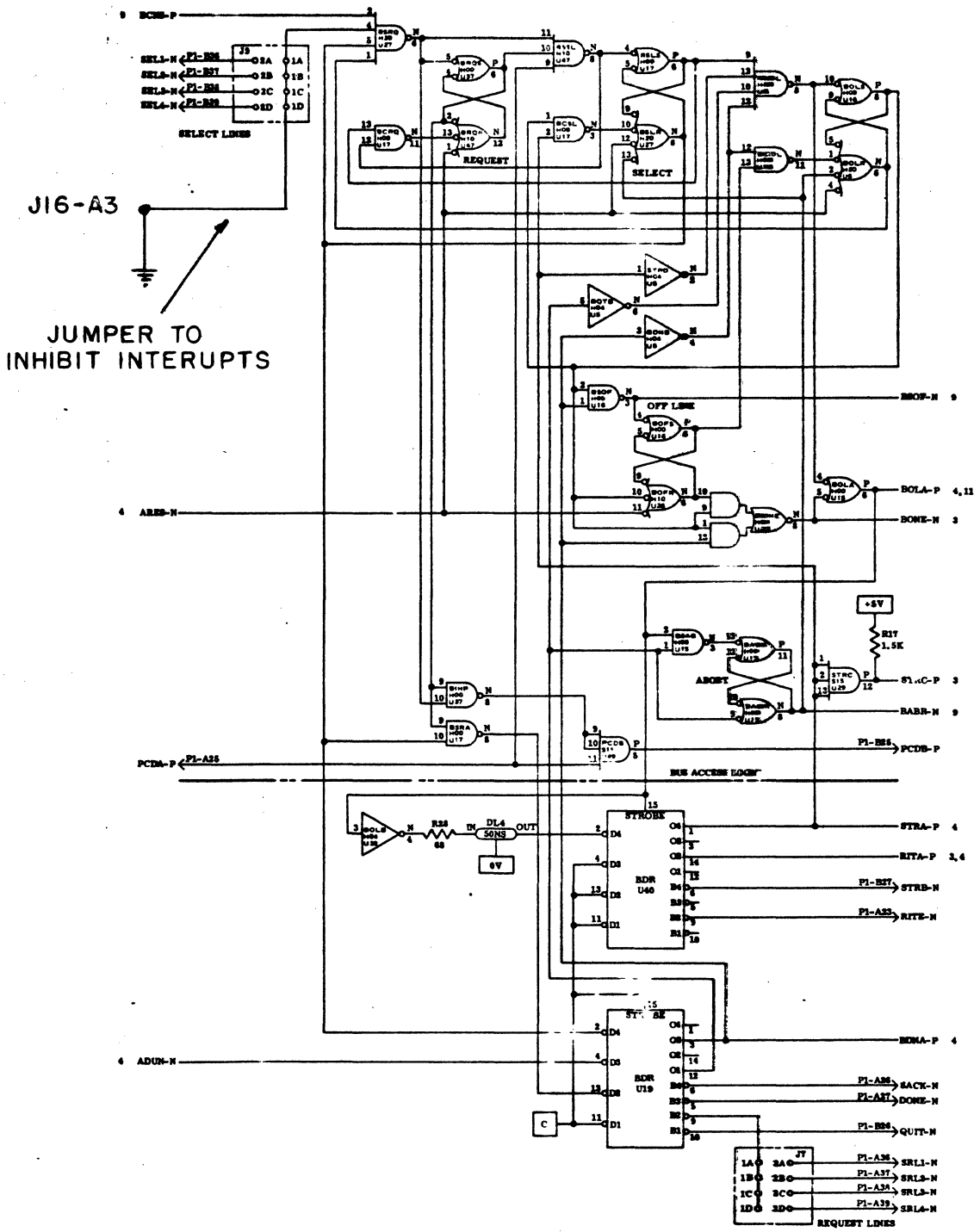
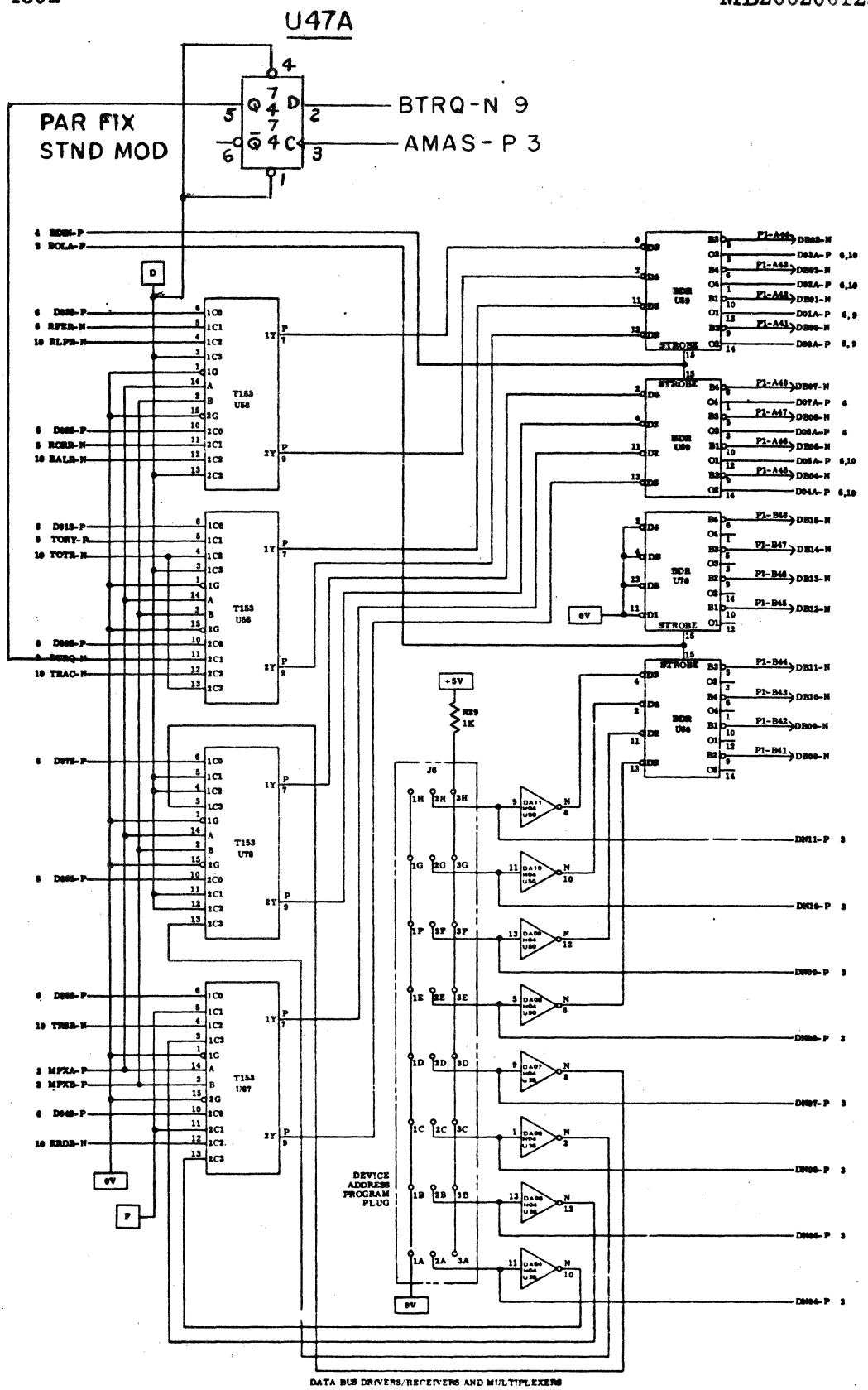


FIG 2

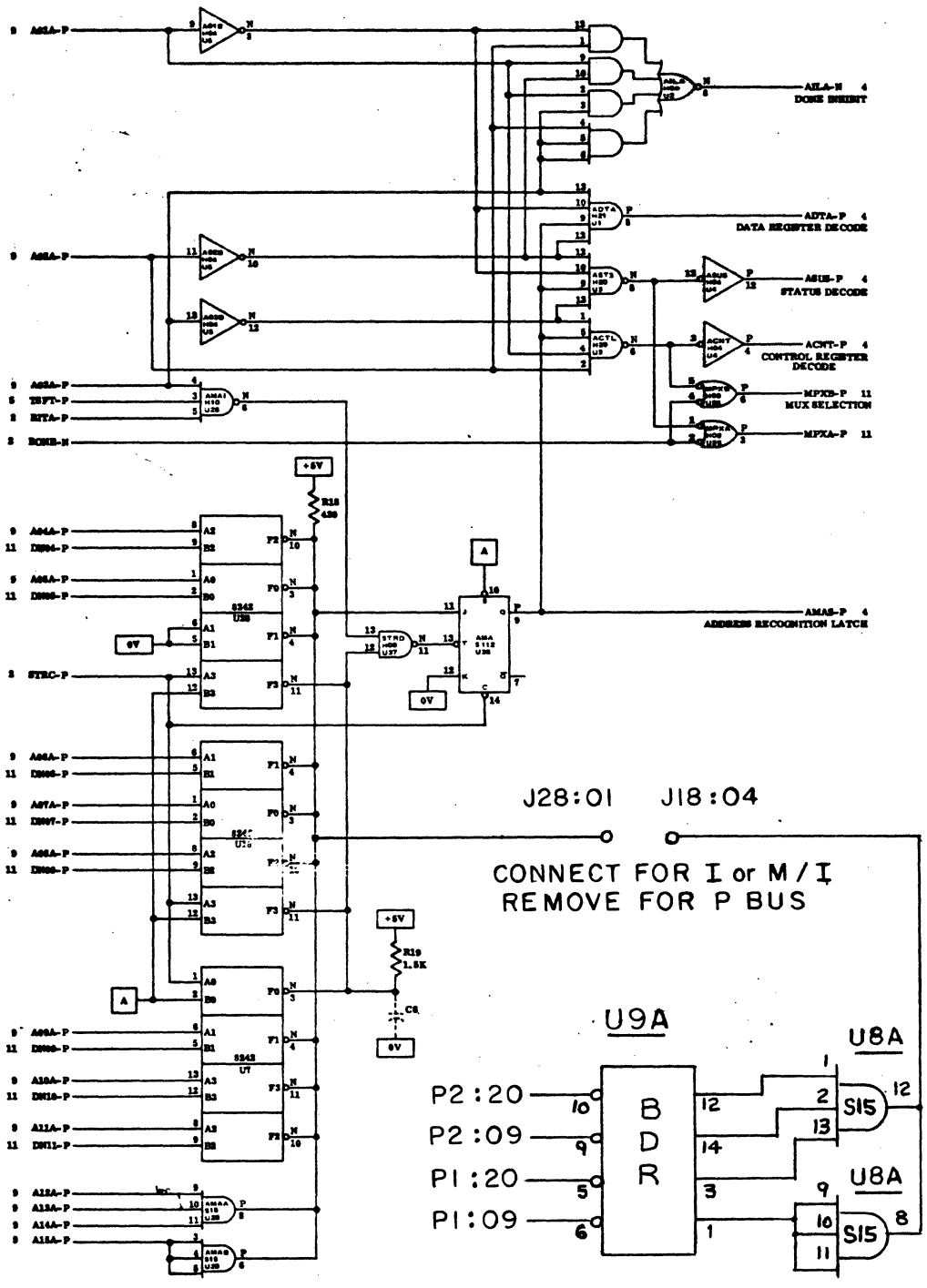


Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 2 of 11



PSB 15 rev C

Serial Buffer Logic Diagram (PSB) Sheet 9 of 10
LD2001002138-1, Rev. C, Sheet 11 of 11



Serial Buffer Logic Diagram (PSB)
LD2001002138-1, Rev. C, Sheet 3 of 11

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

PSB

SEE PSB-Ø2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER 12/5/75

APP'D FOR REL 12/5/75

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PSB SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		PSB-2Ø

SCALE	REV	SHEET 1 OF 1

Internal Power Supply

PS1-Ø2 Logic Description

PS1-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	2/17	

PS1

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN 12/19/75	
	CHECKER	DRAWING TITLE PS1 - LOGIC DESCRIPTION
	ENGINEER	
	APP'D FOR REL	SIZE A / CODE IDENT NO. / DRAWING NO. PS1 - Ø2
	APP'D (CUSTOMER)	SCALE / REV A / SHEET OF

PSI

SUE 5951 INTERNAL POWER SUPPLY

MAINTENANCE BULLETIN M5951

1445

Sept 74 Rev A

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PSI

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LIST OF ILLUSTRATIONS (continued)

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SUE 5951 INTERNAL POWER SUPPLY

MAINTENANCE BULLETIN M5951

PSI

INTRODUCTION

This bulletin contains general and detailed information about the SUE 5951 Internal Power Supply. See figures 1 and 2. The power supply mounts internally in a SUE 7910 chassis and plugs into the INFIBUS. The 5951 supplies +15 volts at 7 amperes, +5 volts at 38 amperes, and -15 volts at 3 amperes to operate up to 16 SUE circuit cards depending on computer system configuration.

DESCRIPTION

The power supply chassis is 7.0-inches wide, 14.25-inches long, 6.25-inches high, and weighs approximately 14.5 pounds. AC line power of 105-125 volts, 47-63 Hz is applied through a 31-inch, 3-conductor power cord with a straight blade power plug (NEMA 5-15P). The power supply is protected by a 10-ampere fuse (3AB-10) mounted in the front panel. A light emitting diode (LED) visible, through the POWER ON opening in the front panel, lights when ac power is applied. DC output voltages, control signals, and common ground connections are made through plug P1 attached to the rear of the power supply.

Power consumption of the 5951 at the following levels, for outputs specified, is:

AC Line	I_{in} (amperes)	P_{in} (watts)
105 v	8.6	780
115 v	8.3	800
125 v	8.0	820

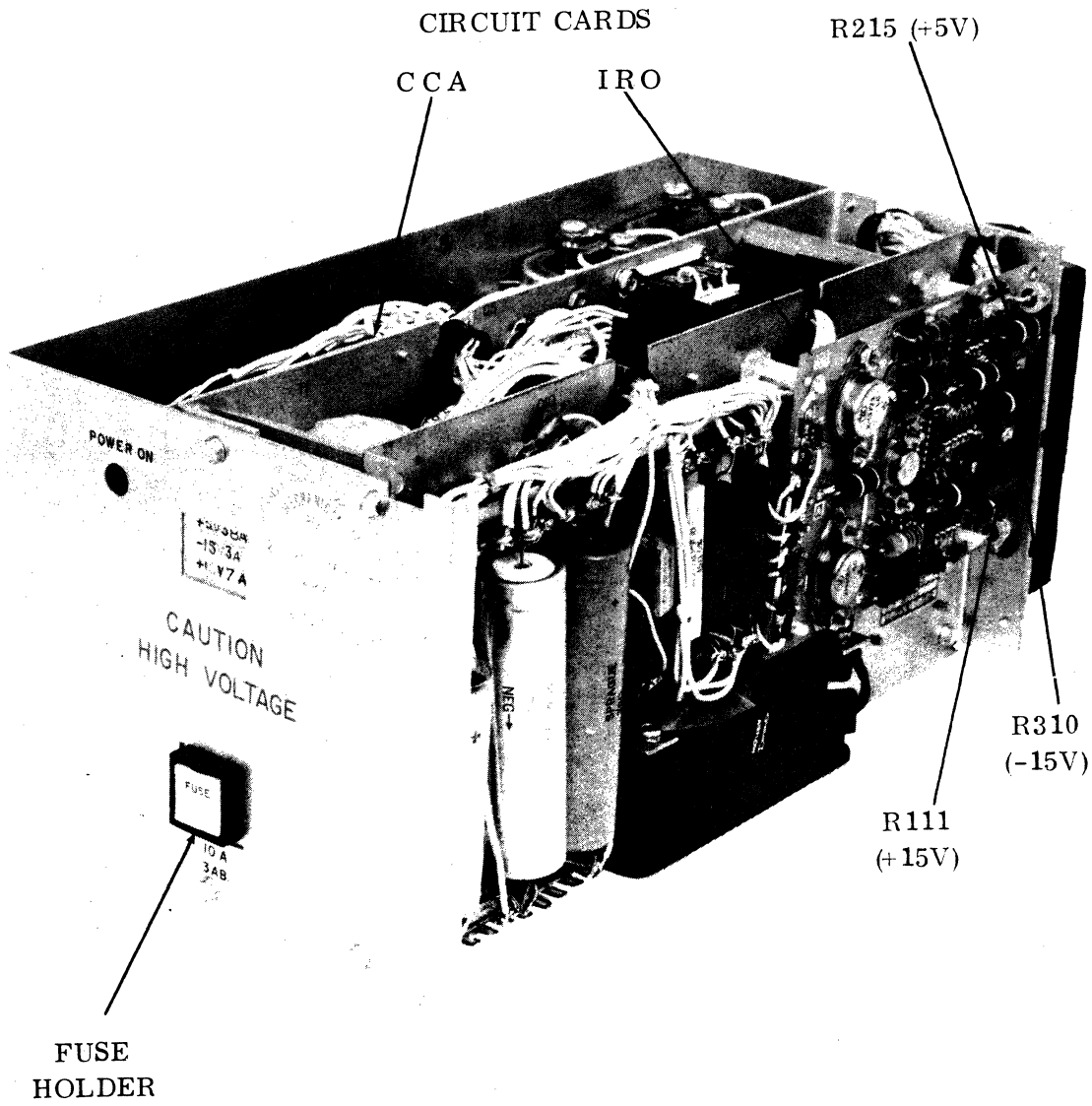

Figure 1. SUE 5951 Power Supply

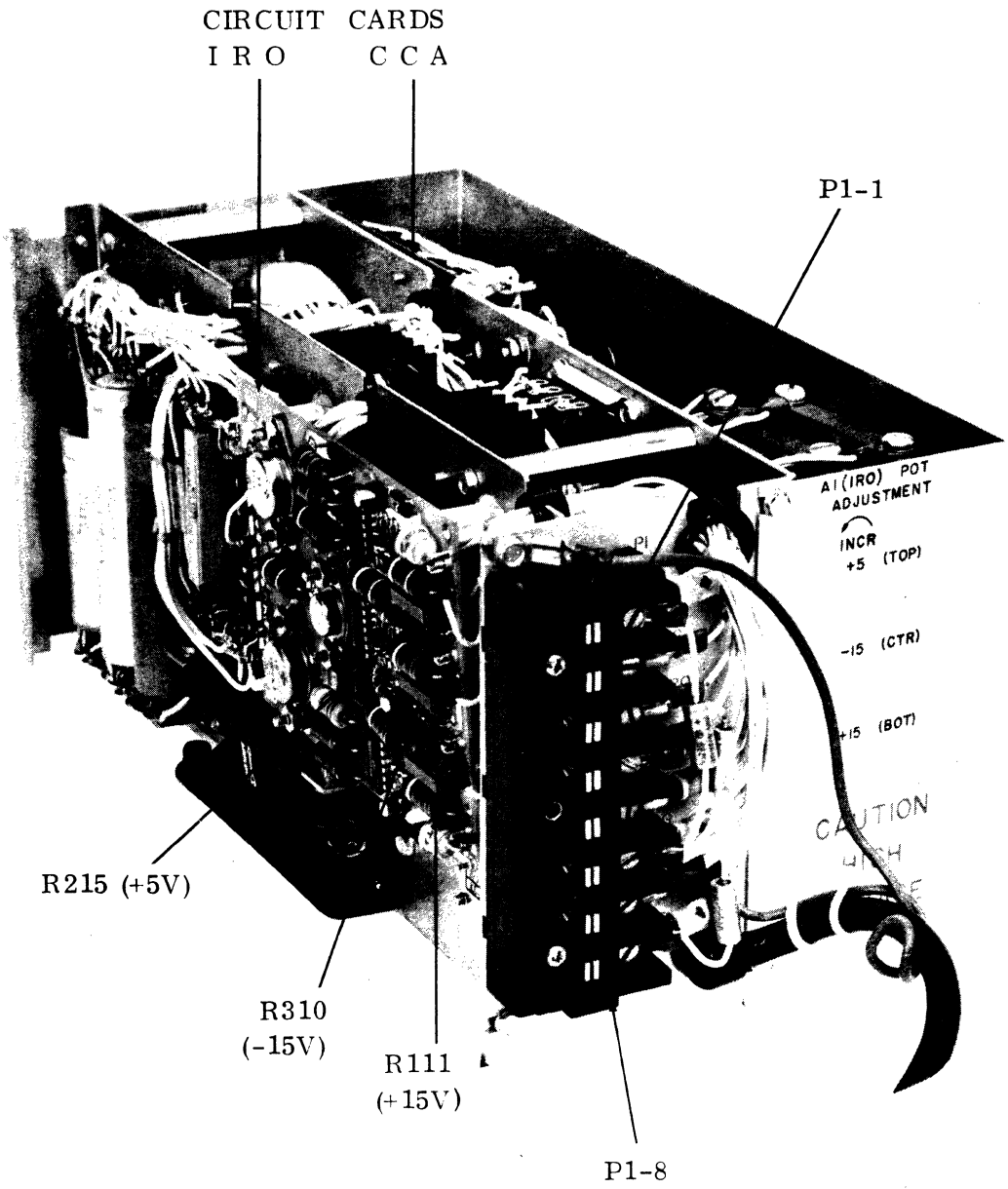

Figure 2. SUE 5951 Power Supply, Rear View

INSTALLATION

SUE 5951 is installed into the right-most position of the SUE Computer chassis from the module insertion end, so that plug P1 on the power supply engages the matching receptacle on the INFIBUS. With all power to the cabinet off, install the power supply as follows:

a. Remove the bezel, unsnap the control panel and swing the panel to the open position.

b. Slide the 5951, in upright position, into the right-most slots of the computer chassis. Route the power supply ac cord, with chassis ground wire attached, through the aperture in the lower right-hand corner of the computer chassis.

c. Apply sufficient pressure on the power supply front panel so that plug P1 engages, completely, its mating receptacle in the disconnect block on the INFIBUS. Engage and tighten the screw (6-32 x 2-1/2 inch) in the disconnect block to secure the connection. Do not over-tighten.

d. Insert the power supply ac plug into one of the receptacles on the SUE 2201, 2202 or 2205 Power Distribution Units. If a SUE Power Distribution Unit is not included in the cabinet, the ac power plug may be connected into any ac convenience outlet in the cabinet or to the 115-volt, primary ac source.

e. Connect the attached ground wire on the power supply ac cord to the dual spade, male-type ground stud mounted on the computer chassis.

f. Swing the control panel closed and replace the bezel to complete the installation.

POWER SUPPLY CIRCUITS

Circuit components are contained on the power supply chassis and on two printed circuit cards — Converter and Control Assembly (CCA) and Inverter Regulator Output (IRO). Simplified schematic and timing diagrams are shown throughout the descriptions that follow. A detailed schematic diagram (SD2003000430) is located near the end of this bulletin.

GENERAL CIRCUIT DESCRIPTION (See Figure 3)

The power supply consists of an a-c to d-c rectifying circuit that drives an inverter operating at approximately 10 KHz. Output from the inverter provides a-c power to three, functionally-independent, regulated d-c output sources

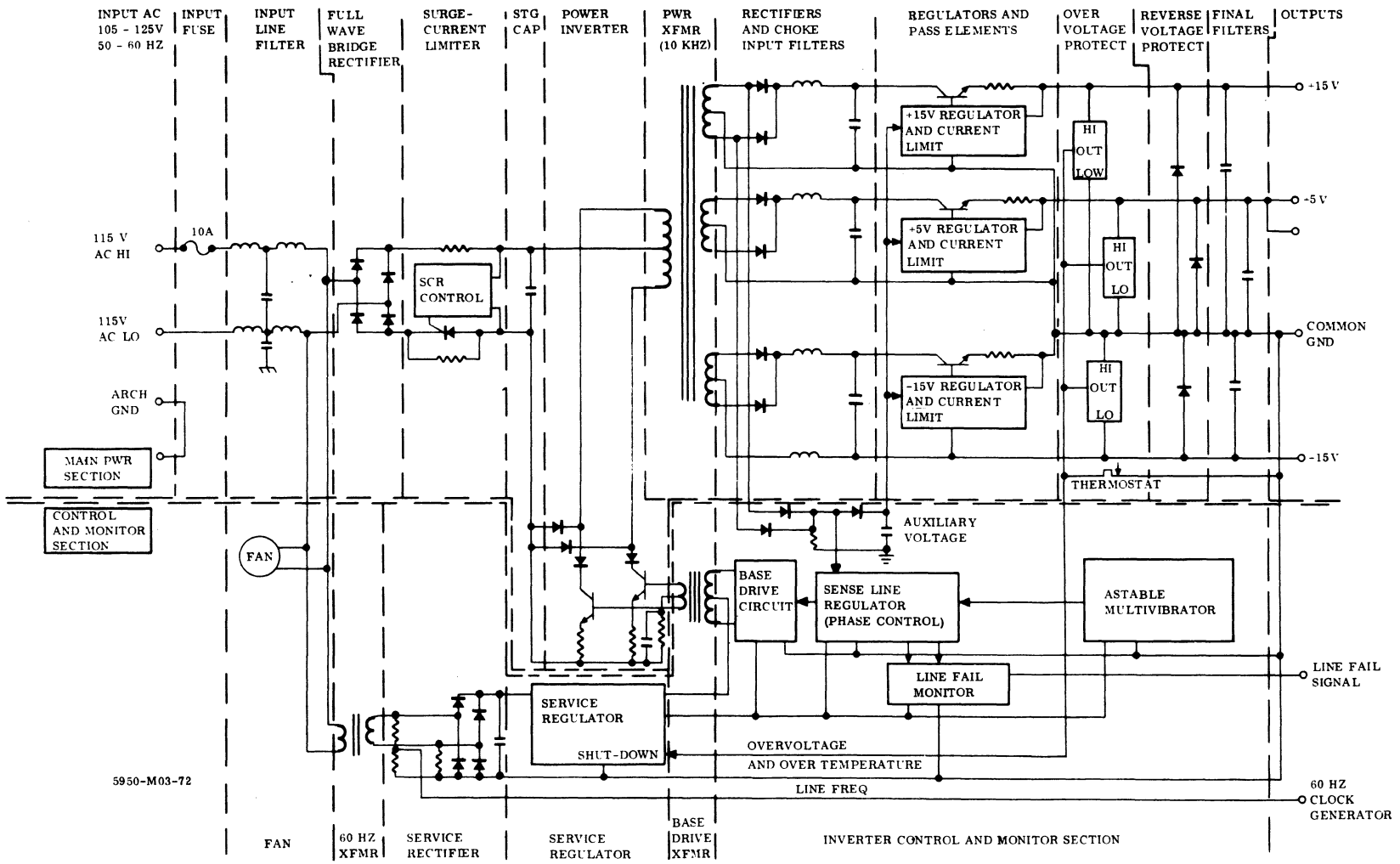

Figure 3. SUE 5951 Power Supply Block Diagram

(+15, +5 and -15 volts). Each series regulator type output circuit is composed of a pass-transistor stage and a section containing output-voltage monitoring, and a reference and feedback amplifier connected in a closed loop arrangement so that regulated output voltages are maintained over a specified load-current range. Each output is adjustable by means of a screwdriver control (figure 2).

Each of the three output circuits has overload/short-circuit current protection in the form of fold-back limiting whereby load-current is reduced to only a small fraction of the maximum value existing at the time the malfunction occurs. In addition, each output circuit contains overvoltage protection circuitry that, when energized, activates a thyristor (SCR). When the SCR is activated, an internally-used reference voltage is removed and with it the base drive to the transistor inverter stage resulting in shutdown of the power supply.

Input voltage is stepped down via an auxiliary transformer operating at 50/60 Hz line frequency. The stepped-down voltage is supplied after rectification to a coarse-regulated, fixed-output, voltage-type series regulator that produces an internally-used reference voltage.

Inverter-transformer outputs are coarse line-regulated. This is accomplished by controlling the base-drive current of the inverter transistors. e.g., an increase in line voltage results in these transistors conducting for a shorter length-of-time. Control circuitry to drive the inverter stage consists of multivibrator, line-voltage sensing, flip-flop, and inverter base-drive circuits. Integrated circuits as well as discrete components are used to perform the various functions.

A thermostat in the power supply serves a dual purpose:

1. Operating ambient temperature is monitored continuously. When excessive temperatures occur, the power supply is shut down.
2. Case temperature of most pass transistors (being critical items) is also monitored continuously. Thus, the thermostat protects power supply circuits and also protects system operation during any component malfunction.

Reverse diodes across each series regulator output prevent polarity reversal from exceeding approximately two volts.

Line failure logic pulses (PWST) and a line frequency signal (LFRQ) are generated for use by the SUE Bus Controller Unit (BCU). PWST pulses provide early warning signals for the BCU when line voltage drops below a threshold level. PWST signals cause a priority interrupt to the highest program level and direct the controller to perform a data protection sequence in ample time before DC power fails. Line frequency signal circuitry provides pulses at the a-c line frequency for use as required by the user.

PSI

DETAILED CIRCUIT DESCRIPTION

Detailed descriptions of major circuits of the power supply are contained in the following subparagraphs. Partial circuit illustrations are provided, but, where circuits are functionally identical, only one is described. Appropriate timing diagrams are also provided. Detailed circuits for the power supply are indicated in schematic diagram SD 2003000430.

INPUT LINE FILTER. - A symmetrical T-type filter (figure 4) reduces voltage spikes and noise signals generated in the power supply during the switching process in the Power Inverter stage. These voltage spikes and noise signals are reduced to an acceptable level to prevent them from entering the a-c power lines.

FULL-WAVE BRIDGE RECTIFIER. - Conventional full-wave bridge rectifier circuitry is used to convert 115-volt 60 Hz line power into an unregulated d-c voltage to power the power inverter.

SURGE-CURRENT LIMITER. - Power resistors R01 and R02 limit a-c input power surge currents into the power supply. To minimize power dissipation of resistor R02 during steady-state, a thyristor (SCR) is connected in parallel with this resistor. A resistor-capacitor type network forms a part of the thyristor gate circuit and retards the firing of Q05 until the inrush current magnitude has reached a safe value.

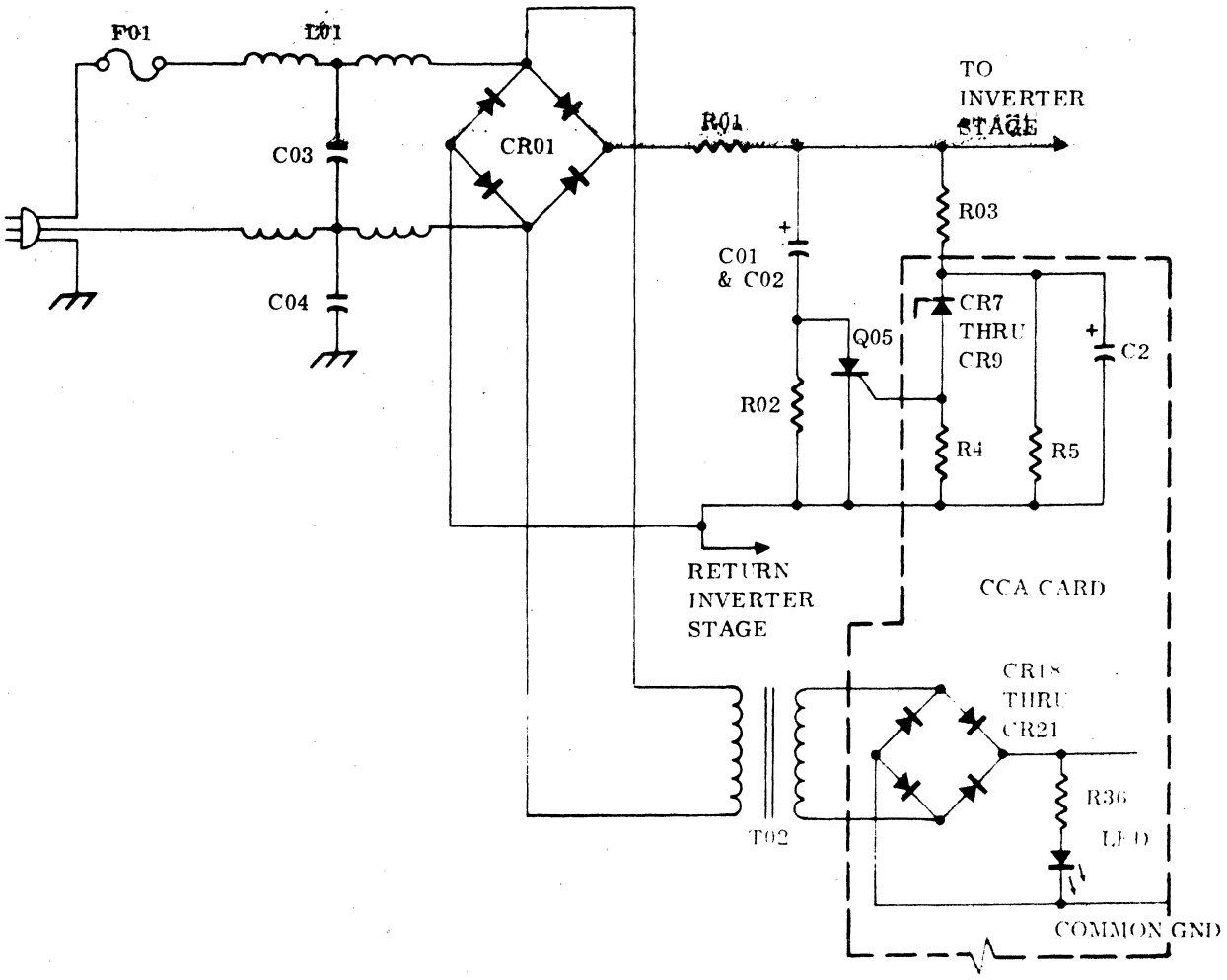

Figure 4. Power Supply Input Stage (Preceding Power Inverter)

INDICATING LIGHT. -An indicator (Light Emitting Diode) that illuminates when the supply is energized, can be observed through a hole in the cover on the front of the power supply. The LED no longer lights when a-c power is removed from the power supply.

POWER INVERTER.- The power inverter is essentially an oscillator operating in a quasi square-wave mode whereby the unregulated d-c input voltage is converted into three a-c voltages (figure 5). Square-wave generation is accomplished by transistors Q01 and Q02. and transistors Q03 and Q04. respectively. connected in parallel to accommodate input-current requirements under maximum load-current conditions. Emitter resistors R13 and R14 are equalizing resistors for these transistor pairs.

PSI

Switching action of the inverter transistors occurs in the following manner. Rectified and filtered line voltage is applied between the center tap of transformer T01 primary and the common node of resistors R13 and R14. When base current is supplied to one of the two transistor pairs, that particular pair is driven into saturation and the other pair to the cutoff state. When Q01 and Q02 are driven into saturation, the voltage at A is approximately at ground potential (figure 5). Since the voltage between A and B is the d-c input voltage. the voltage at C with respect to A is twice the input voltage because of autotransformer action of T01 thereby applying a reverse voltage across transistors Q03 and Q04. During the time interval that transistors Q01 and Q02 are conducting, input power is transferred from primary to secondary windings. Removal of base-drive current to Q01 and Q02 causes both transistors to become cutoff and since temporarily base drive has not been supplied to transistor pair Q03 and Q04, there is no transfer of input power from primary to secondary windings of transformer T01.

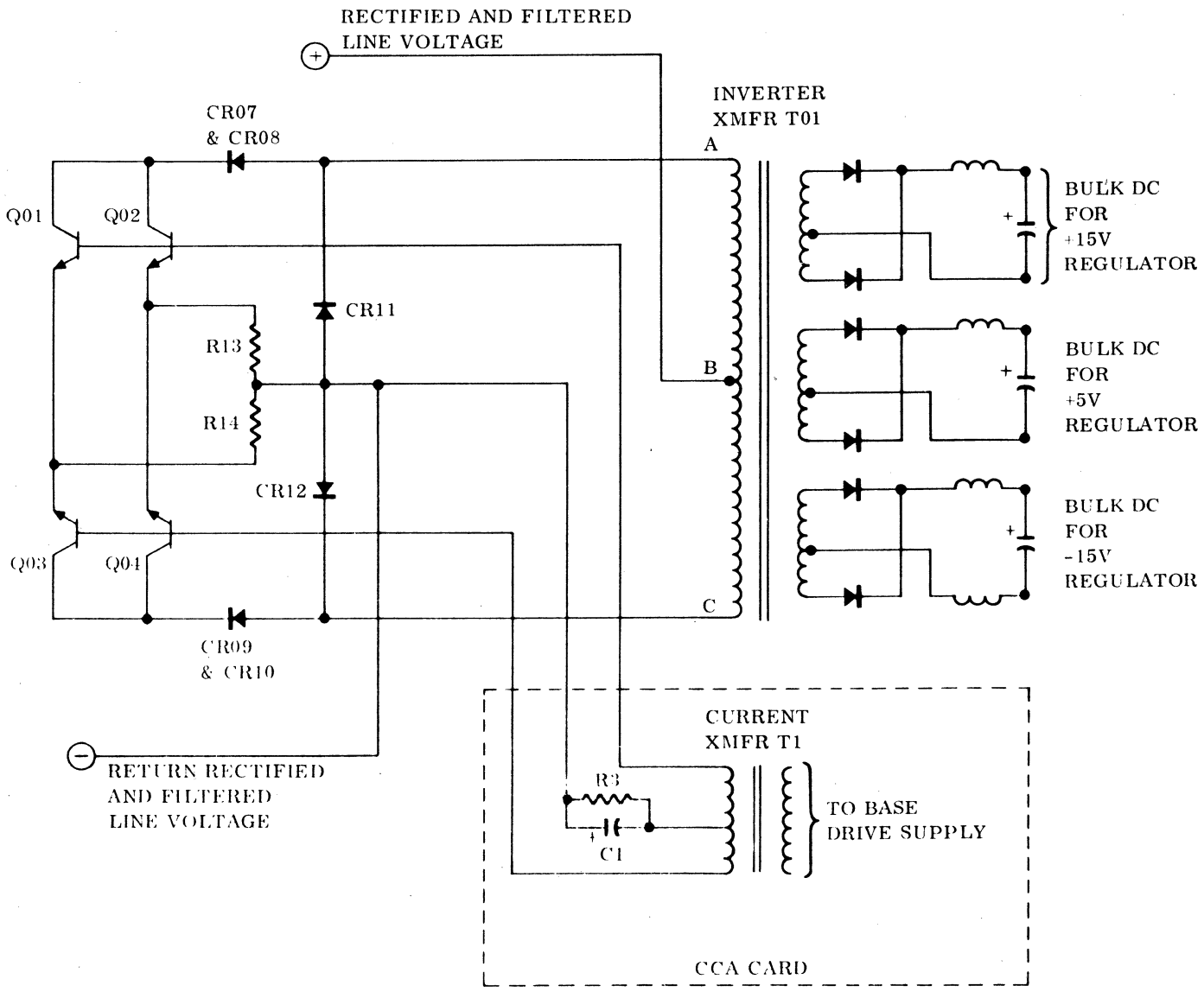

Figure 5. Power Inverter Circuit

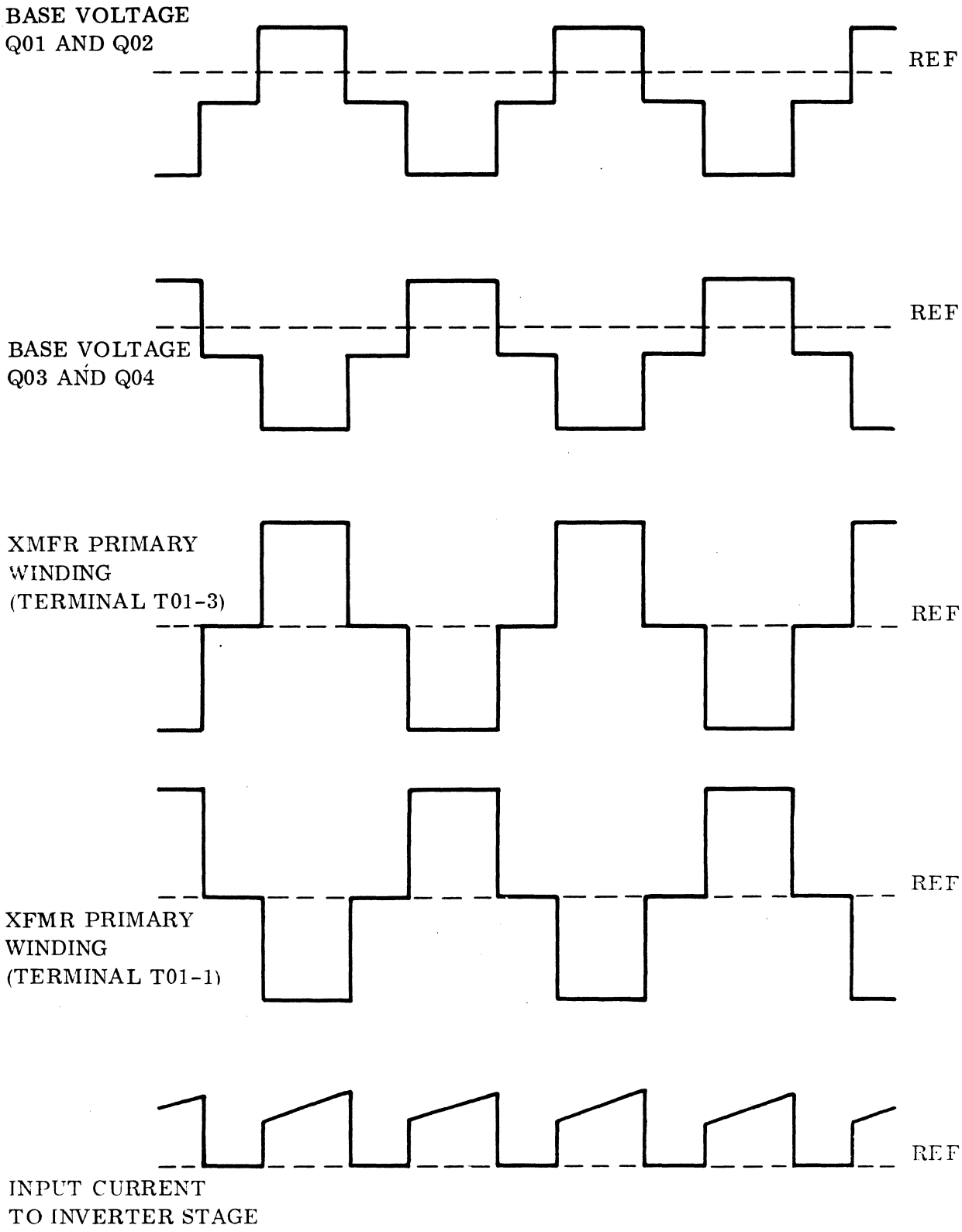

Figure 6. Power Inverter Timing

Various waveforms for the power inverter stage are shown in figure 6. These waveforms indicate that at different time intervals, a similar action occurs when transistors Q03 and Q04 receive base-drive current from current transformer T1 (on the CCA card), and consequently saturate. Again, input power is transferred from primary to secondary windings whereby transistor pair Q01 - Q02 is maintained at cutoff. A slightly negative emitter-to-base voltage applied to any transistor pair in cutoff, assures no collector-current flow through that pair. This voltage is derived from the R3 resistor and C1 capacitor combination in the base-drive circuit.

ASTABLE MULTIVIBRATOR. - Circuitry for the 20 KHz clock (50 microsecond cycle time) is shown in figure 7. Selection of the RC-timing circuits is such that transistors Q4 and Q5 are conducting successively for time intervals of 40 microseconds and 10 microseconds, respectively.

Operating voltage for this cicruit is derived from an internally-used series regulator (transistor Q9 and associated zener diode CR22).

Astable multivibrator detailed operation can be explained by examining details occurring during any one cycle. When Q5 is maintained in the conducting state as a result of current through R14, and Q4 is non-conducting as a result of a reverse bias voltage from C5, waveforms are as shown in figure 8. Capacitors C4 and C5 charge to the voltage across them. Different values for C4 and C5 cause non-equal time intervals during which these capacitors are charged or discharged. For correct operation, capacitor C4 must be fully charged before any change-of-state occurs. C4 charges through the parallel resistance of R13 and Q3. A voltage of $V_{Q3_E} - V_{Q5_E}$ is developed across C4. During this time, capacitor C5 also charges to a voltage of $V_{REF} - V_{CE_{Q5\ SAT}}$. As soon as C5 charges to a sufficient voltage to forward bias Q4, Q4 starts conducting and thereby brings the Q4 collector voltage down. This voltage drop is coupled through C5 to the base of Q4 and exponentially stops Q4 conduction. This

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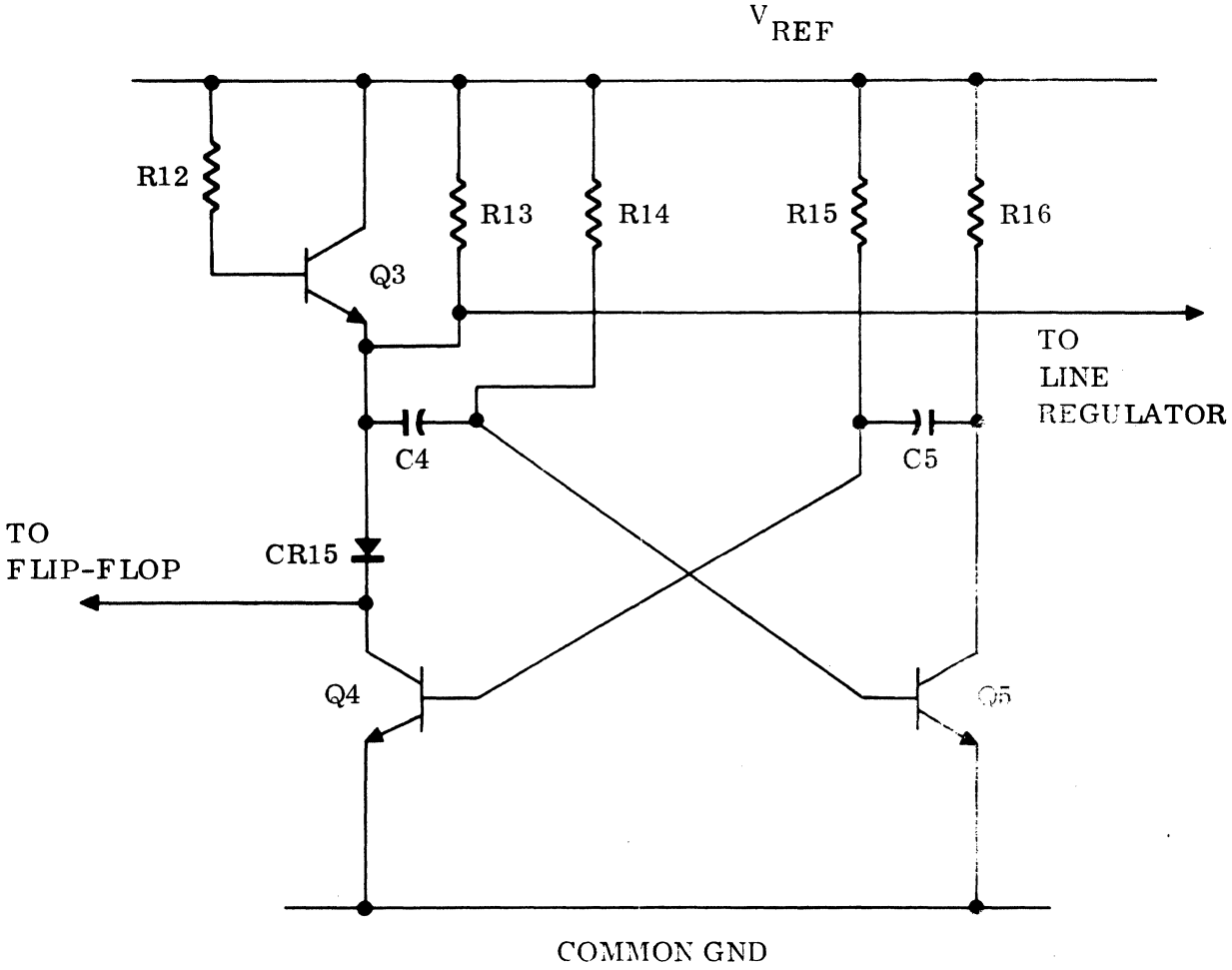

Figure 7. Astable Multivibrator (20 KHz Clock) Circuit

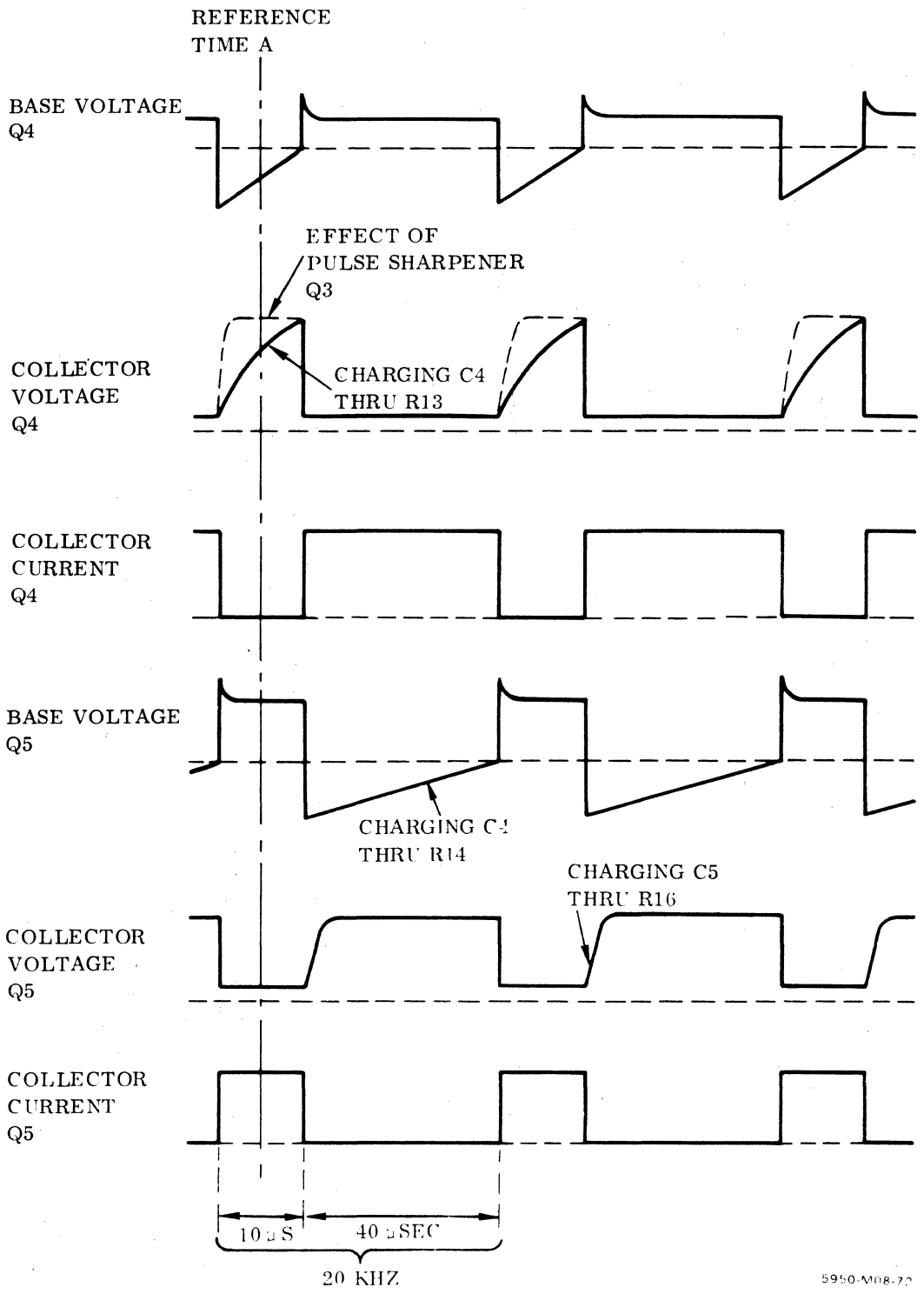

Figure 8. Astable Multivibrator Idealized Waveforms

process is regenerative and proceeds rapidly until Q4 conducts and Q5 is non-conducting. Initial conditions again exist but the states of both transistors have interchanged. Transistor Q3 has one sole function, to act as a pulse-sharpener for pulses generated at the collector of transistor Q4.

LINE REGULATOR. - Figure 9 shows the line regulator circuit which basically consists of a differential amplifier. The base of transistor Q7 is held constant and the base of transistor Q8 is connected to a voltage divider network thereby sampling a portion of one of the secondary winding voltages of the power inverter transformer.

PSI

Operation of this circuit is such that for an increase in line voltage, i.e., an increase in output voltage of the power inverter transformer, transistor Q8 drive voltage decreases while the collector current of Q7 increases. This condition alters the time constant of the R17-C6 combination and thus the rate-of-rise in voltage at the base of Q6. This result is demonstrated in figure 10 where reference time A is shifted so that a steeper slope occurs, i.e., the forward biasing of transistor Q6 base occurs at an earlier time.

FLIP-FLOP. - Signals from the astable multivibrator and from the line regulator are supplied to a J-K flip-flop (U3 in figure 11) to generate complementary pulses that are coupled via driver stages U1 and U2 to current transformer T1. Figure 10 shows in detail the waveforms at various nodes. Mixing line regulator output signals and flip-flop output signals causes the generation of two complementary trains of pulses of variable pulse width but at a constant repetition rate. An increase in line voltage causes narrower complementary pulses to be supplied to the T1 current transformer.

SERVICE REGULATOR (INTERNALLY-USED REFERENCE VOLTAGE AND VOLTAGE-TO-CONSTANT CURRENT CONVERTER). - Auxiliary transformer T02 steps down line voltage to furnish power, after rectification, to a coarse-regulated series regulator with fixed output (figure 12). One of various functions of this reference voltage is to supply a bias voltage for a

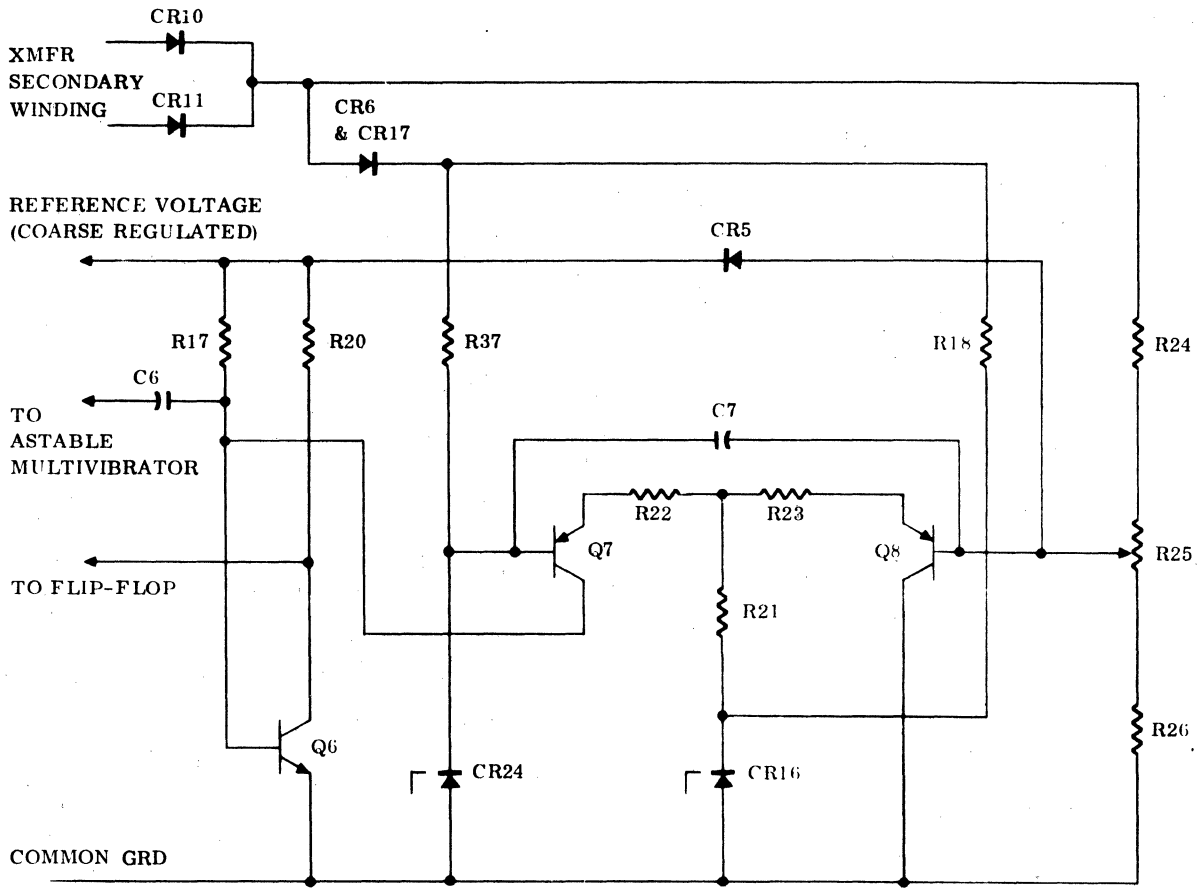

Figure 9. Line Regulator Circuit

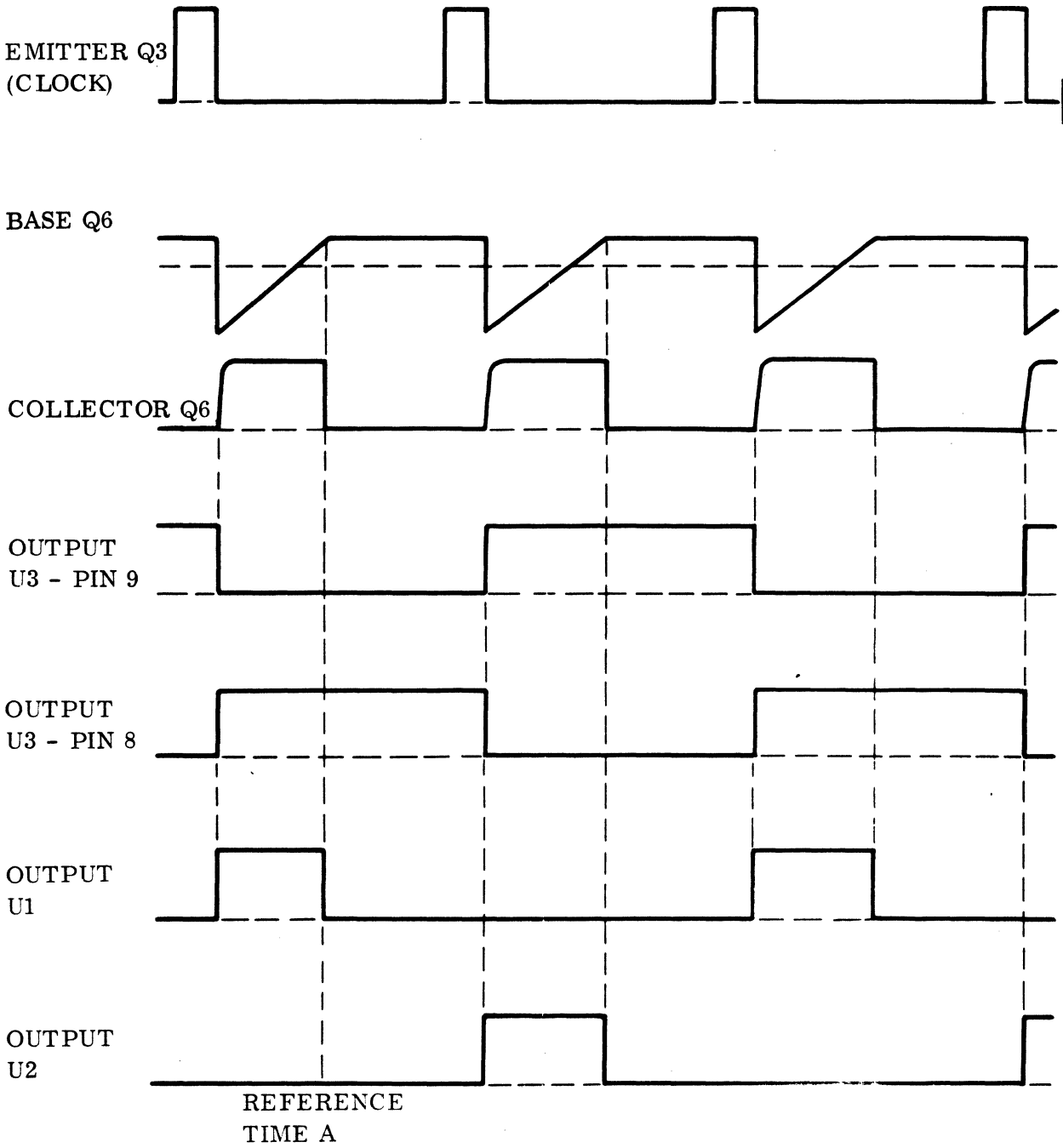

Figure 10. Line Regulator Timing Diagram, Idealized

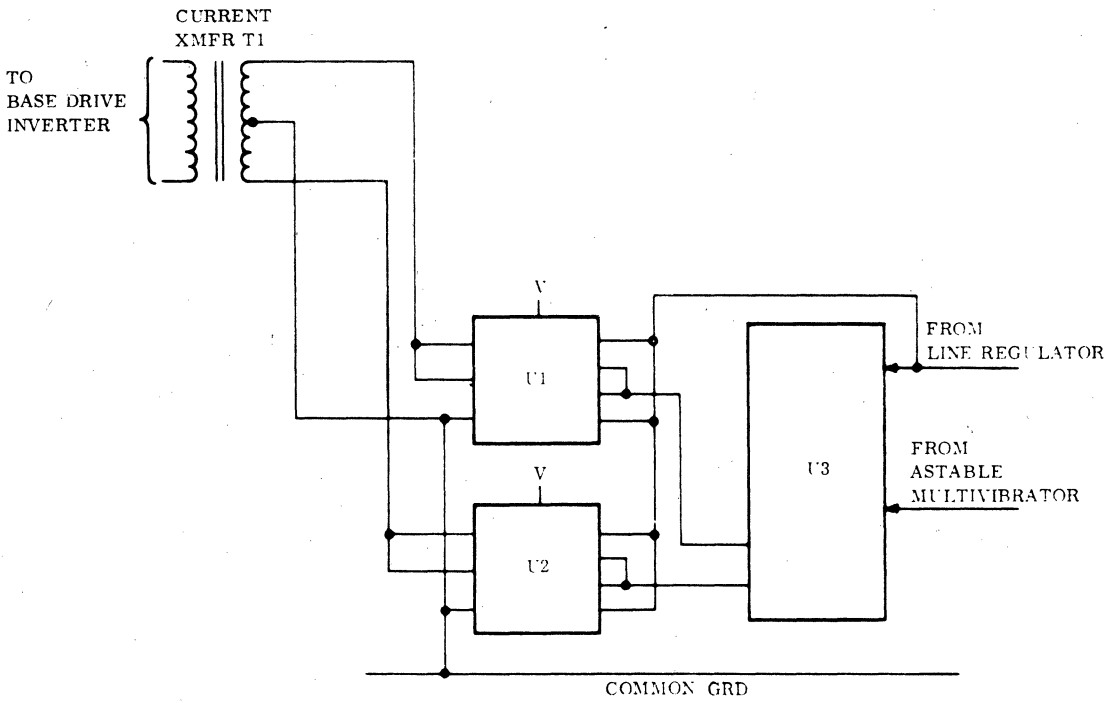

Figure 11. Power Inverter Drive Circuit

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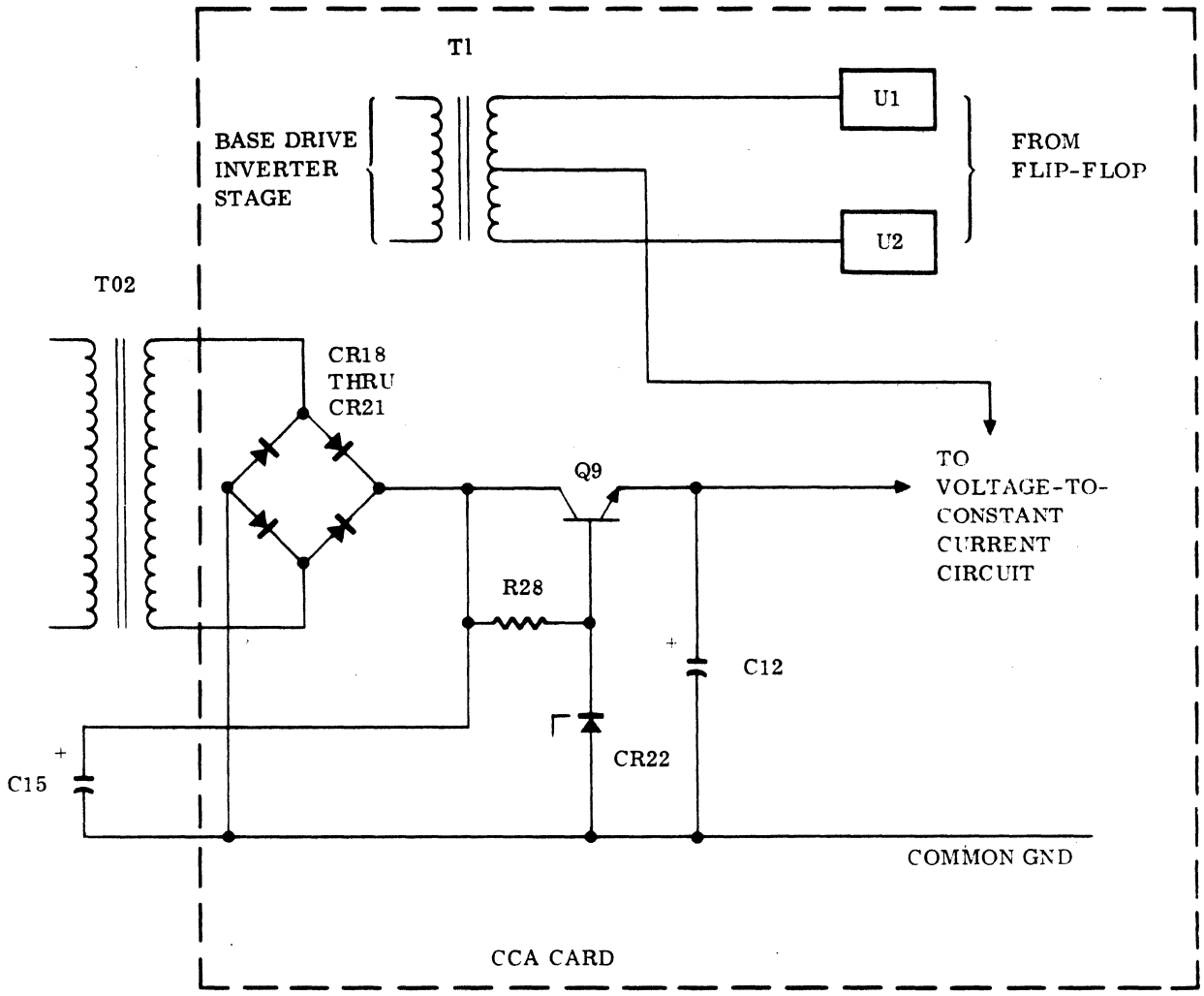

Figure 12. Service Regulator Circuit

constant-current circuit supplying base-drive current (transistors Q1 and Q2 plus associated bias networks - SD2003000430) via a center-tapped current transformer to the power inverter transistors. On-and-off timing of this constant current is controlled by driver stages U1 and U2.

RECTIFIER AND INPUT CHOKE FILTER STAGES (TO THE OUTPUT REGULATORS). - Input power to each of the three regulator circuits is obtained from separate secondary windings of the power inverter transformer. These voltages are rectified, filtered, and are line-regulated, thereby reducing the number of pass transistors required in the series-regulator circuits.

REGULATORS AND PASS ELEMENTS (OUTPUT REGULATORS). - Each series regulator consists of a power amplifier stage (one or more pass transistors with their associated Darlington circuit) and a feedback loop (figure 13). Except for voltage and current handling capacity, all regulators are functionally identical. Where, to meet current requirements, more than one pass transistor is used, all are connected in parallel. In the feedback loop, part of the output voltage is compared with a stable reference voltage by a differential amplifier. Any difference in conduction detected by this comparator circuit, because of line and load variations, causes amplifiers to react and the pass transistor(s) to vary accordingly. This condition continues until the unbalanced input to the comparator stage is restored to the original balanced state. A combination of discrete components and an integrated circuit assures stable operation throughout a fairly wide temperature range.

OVERLOAD AND SHORT-CIRCUIT PROTECTION. – An inherent feature of the integrated circuit used in each series regulator is output-stage built-in overload-and-short-circuit protection circuitry. Protection is accomplished by using foldback techniques. When load current delivered exceeds a pre-set level, base current to the pass-transistor stage is shunted away (reducing base drive) which causes the output voltage and load current to decrease (figure 14). Occurence of excessive heat dissipation in the pass transistors (the -15 volt pass

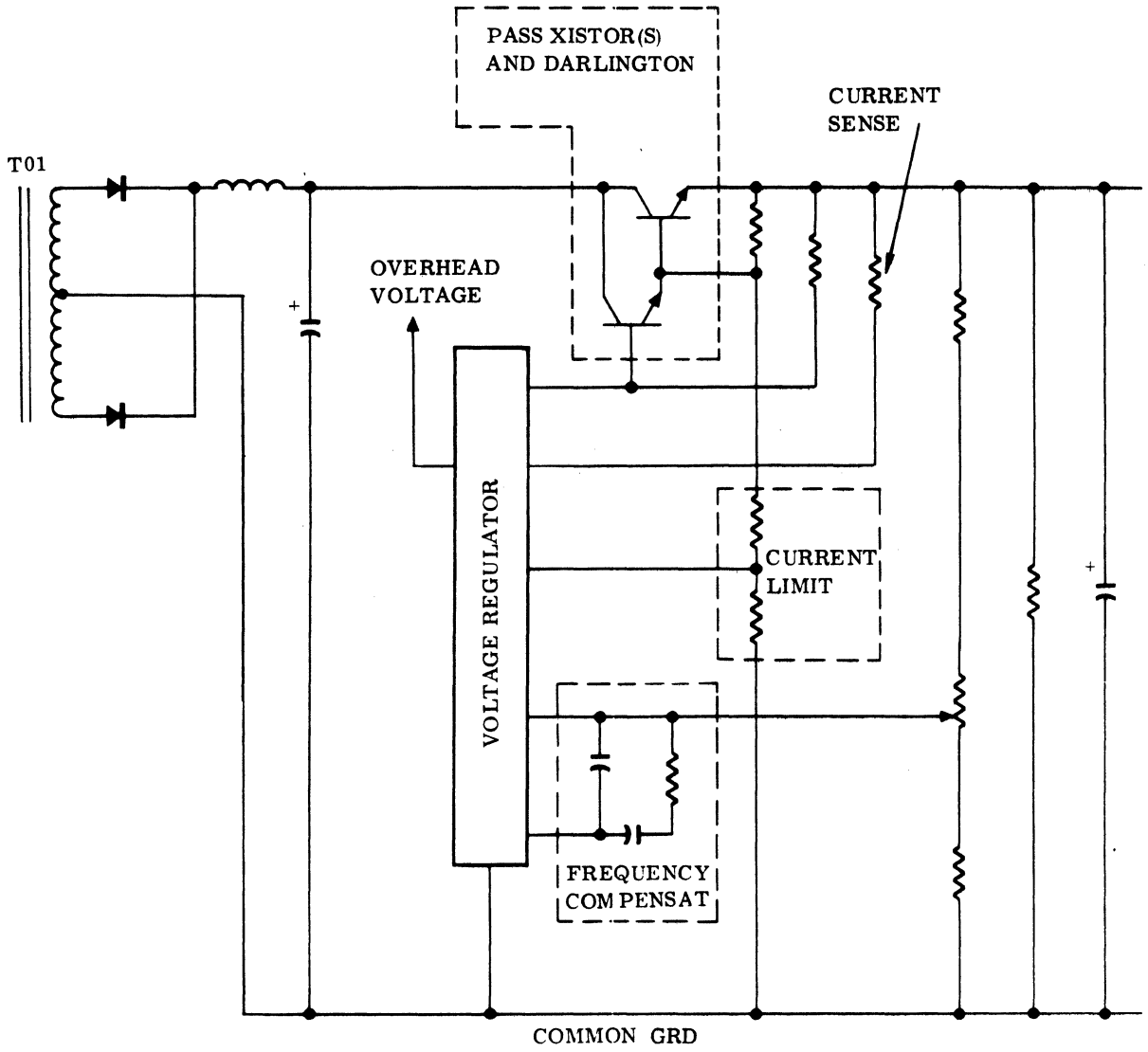

Figure 13. Regulator and Current Limiter Circuit (Typical)

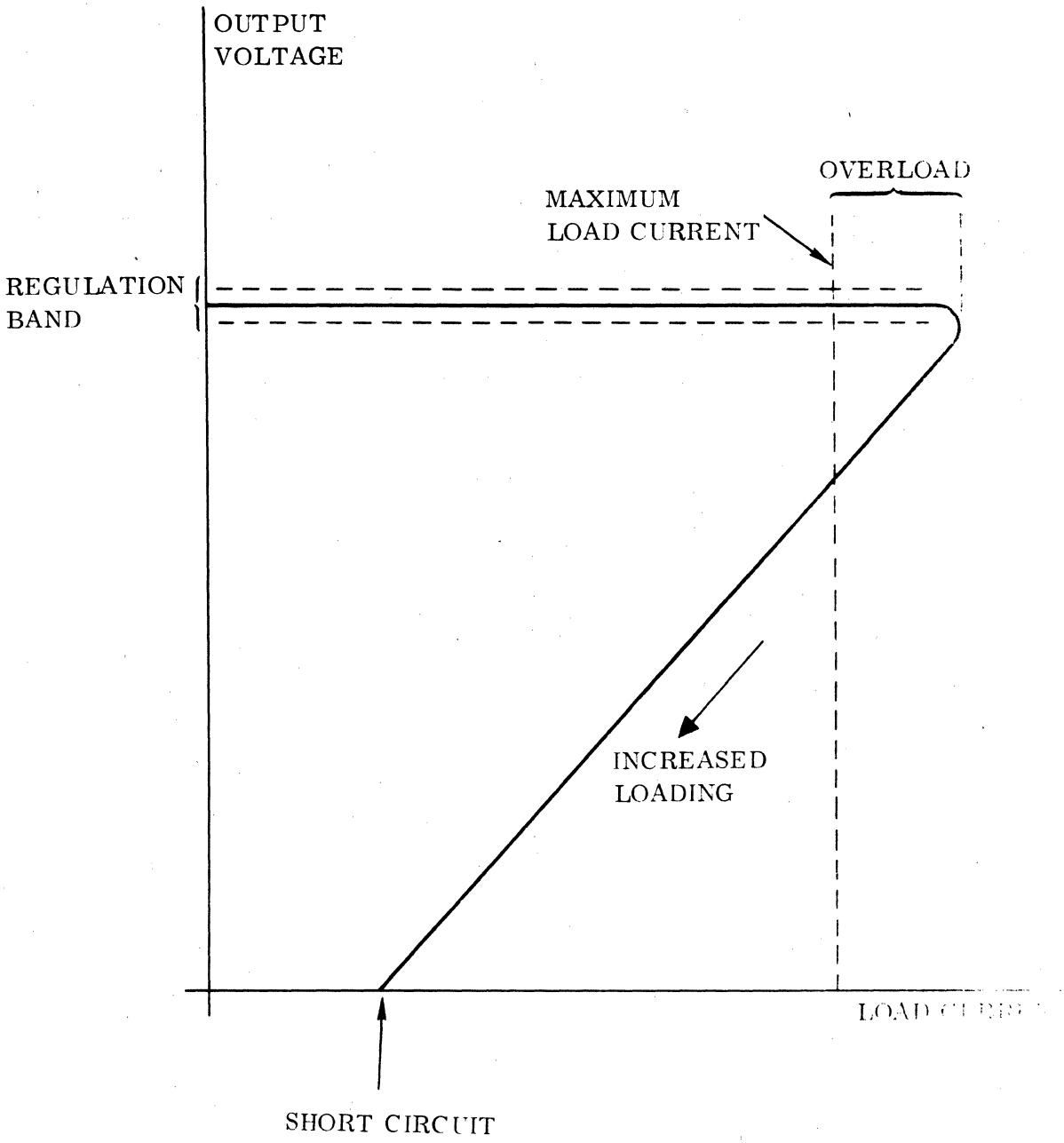

Figure 14. Overvoltage/Short-Circuit Regulator-Output-Current Plot

transistor is chassis mounted and, therefore, has adequate heatsinking) is prevented by the closure of contacts on a thermostat. Closing the thermostat contacts causes Q10 (CCA) to conduct, thereby developing a voltage across R32; this voltage rise triggers SCR Q11 (figure 15). Firing of this thyristor causes collapse of the internally-used reference voltage; base drive current to the power inverter transistors is eliminated and the power supply is shut down.

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OVERVOLTAGE PROTECTION. - Overvoltage protection exists at the output of each series regulator. This protective circuit consists of a simple threshold voltage detector in the form of one or more (output voltage sensing) zener diodes and an amplifier. When an excessive output voltage occurs, this circuit is activated and fires thyristor Q11, thereby shutting down the power supply (figure 15).

LINE FAIL DETECTION. - Line-failure detection circuitry provides a series of positive pulses to the bus controller unit when line voltage becomes less than the threshold level (figure 16). Input signals to integrated-circuit flip-flop U3 and signals from the succeeding U4 output-driver stage are illustrated in figure 16. Continued decrease in the line voltage causes collapse of all voltages in the power supply and, consequently, of this line fail signal. Any increase in line voltage above this threshold removes these line-fail pulses.

LINE FREQUENCY SIGNAL. - The line-frequency signal circuit provides one positive pulse for each full cycle of the line voltage. This is accomplished by connecting a resistor network across part of the full-wave bridge at the output of auxiliary transformer T02. Figure 17 shows this circuit and the waveform of pulses obtained.

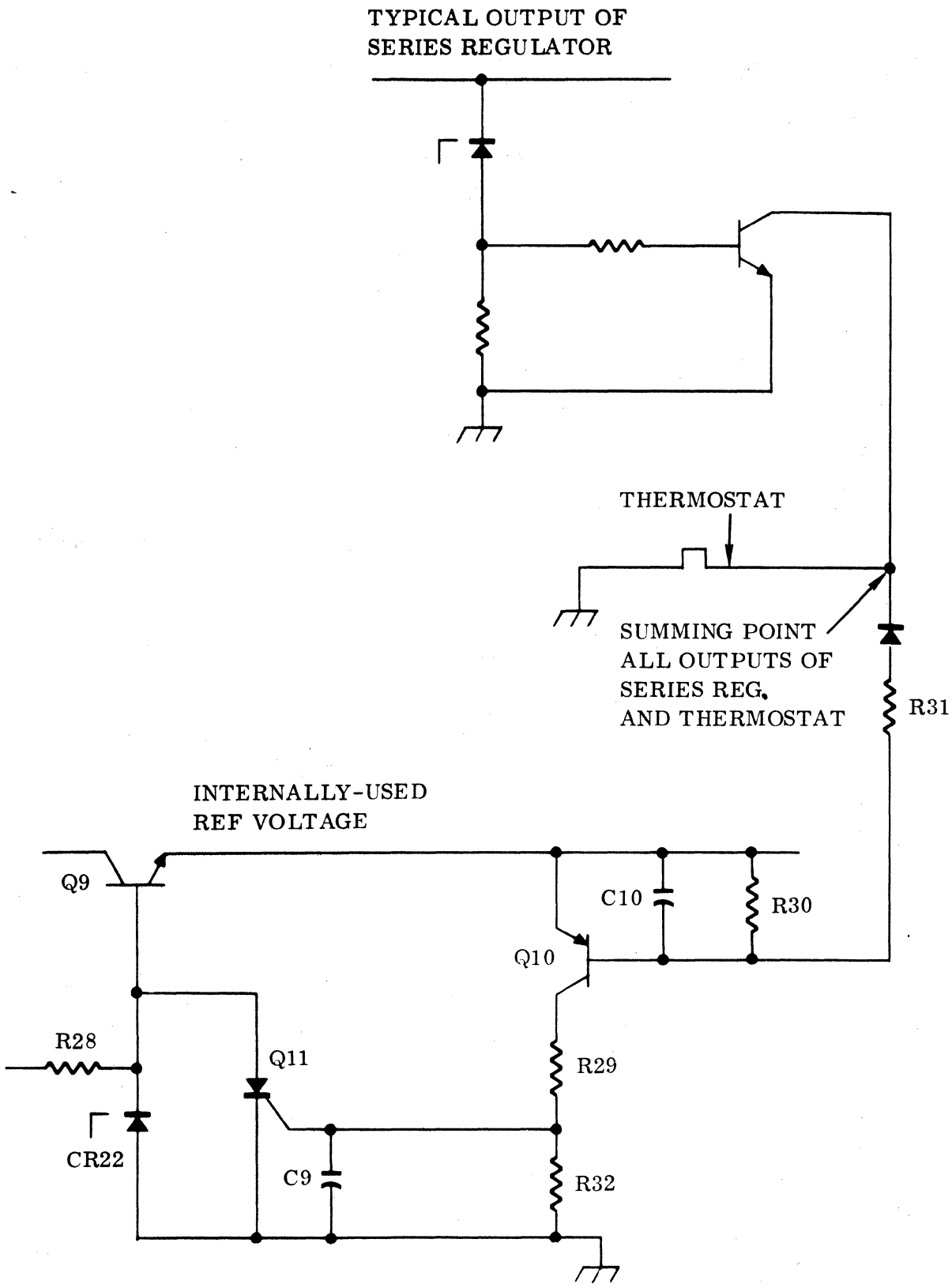

Figure 15. Overvoltage and Temperature Protection Circuit

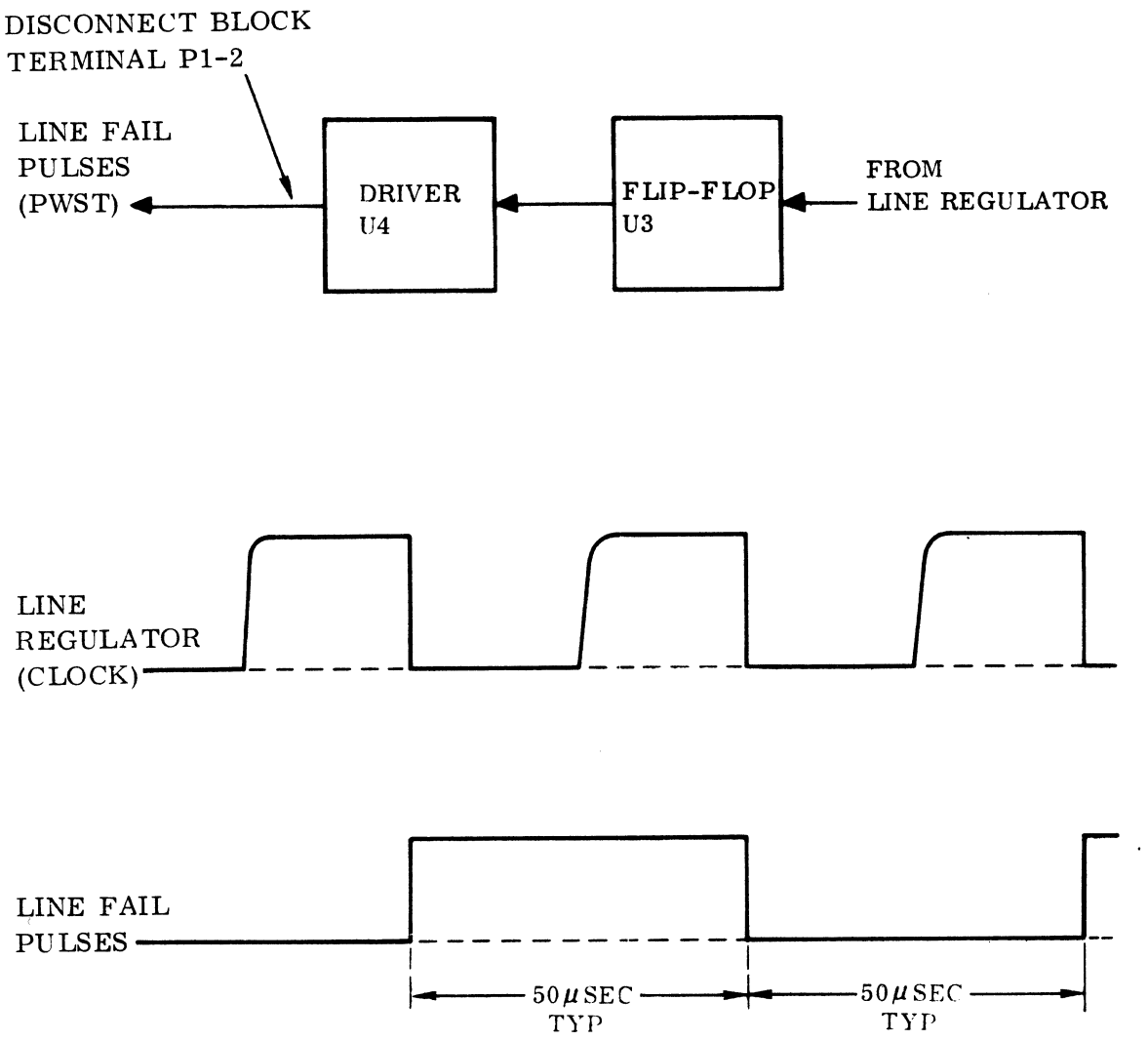

Figure 16. Line-Failure Circuit Block Diagram and Signal Waveforms

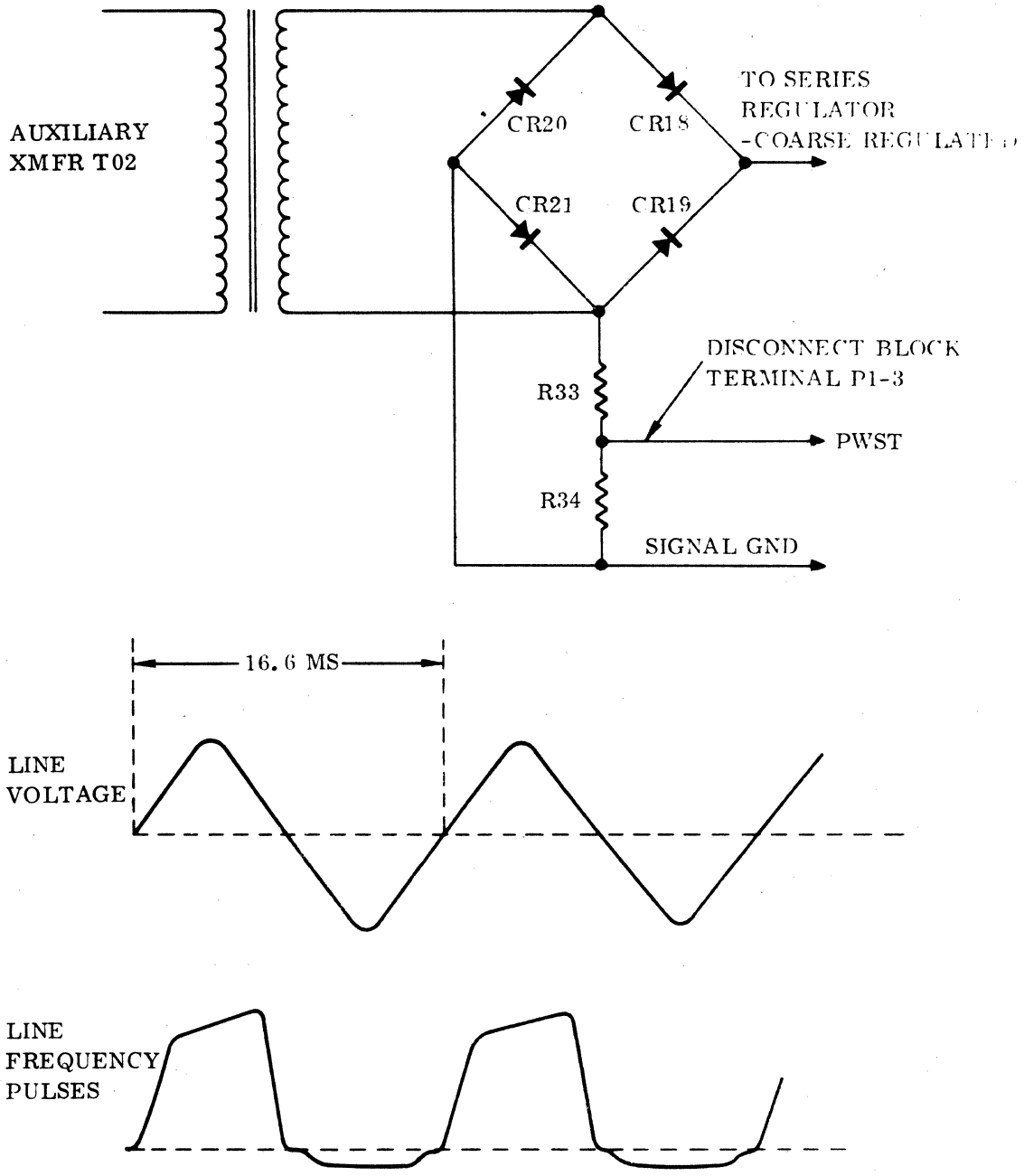

Figure 17. Line-Frequency Circuit and Signal

MAINTENANCE

GENERAL

The SUE 5951 Power Supply is designed for unattended operation without routine preventive maintenance. Thus, paragraphs following contain only corrective maintenance information, i.e., calibration and testing, trouble analysis, and repair techniques.

RECOMMENDED TEST EQUIPMENT. - Table 1 contains a list of test equipment recommended for power supply maintenance. Equivalent equipment can be used.

Table 1. Recommended Test Equipment

Equipment	Manufacturer	Model
DC Ammeter	Weston	50 amp 931
Multimeter	Simpson	270
Digital Voltmeter	Non-Linear Systems	LX-2
Variable Auto-Transformer	General Radio	W 20
Oscilloscope	Tektronix	545A
Preamplifier	Tektronix	CA
Variable Loads	Litton (Dynaload)	541900
Resistor, 1000 ohms, 1/4 W		

CALIBRATION AND TESTING

NOTE

Power supply calibration and testing must be performed normally with the power supply disconnected from the INFIBUS. Thus, unless a substitute power supply is available, the computer system must be non-operational during calibration and testing.

OVERVOLTAGE THRESHOLD TEST. - Overvoltage threshold test must precede the output voltage adjustments. Refer to table 2 and proceed as follows:

Step 1: Disconnect line cord from a-c power.

Step 2: Connect digital voltmeter test leads to appropriate output terminals per table 2.

Step 3: Assure that all outputs are unloaded.

Step 4: Connect line cord to a-c power and turn the appropriate output voltage adjustment potentiometer, per table 2, counterclockwise until the output voltage decays to a very low value and the power supply shut-down condition occurs.

Table 2. Overvoltage Threshold Check

Nominal Voltage (volts)	Test Points*	Overvoltage Threshold (volts)	Potentiometer to Set Output Voltage
-15	P1-1	+17.5 ± 0.8	R111 (IRO)
+5	P1-4	+6.1 ± 0.5	R215 (IRO)
-15	P1-8	-17.5 ± 0.8	R310 (IRO)
*NOTE: Connect voltmeter return to P1-6 (common ground).			

Step 5: Turn the output voltage adjustment potentiometer several turns clockwise.

Step 6: Disconnect and reconnect the line cord from/to the a-c power.

Step 7: Set output voltage to nominal value with output voltage adjustment potentiometer.

Step 8: Repeat steps 4 through 7 to check each overvoltage detection circuit.

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OUTPUT VOLTAGE ADJUSTMENT TO NOMINAL. - Output voltages can be adjusted under no-load conditions. Proceed as follows:

Step 1: Connect digital voltmeter test leads to the appropriate output terminals (table 2).

Step 2: Connect line cord to a-c power.

Step 3: Verify that each output voltage is per table 3; adjust appropriate potentiometer to obtain nominal output setting as required.

NOTE

In this procedure, do not exceed threshold overvoltage. If regulator output decreases suddenly during this adjustment because of an overvoltage condition, disconnect power supply from a-c power, turn applicable potentiometer slightly clockwise and attempt readjustment.

CURRENT LIMITER TEST. - Proceed as follows:

Step 1: Disconnect line cord from a-c power.

Step 2: Connect digital voltmeter test leads to appropriate output terminals (table 4).

Table 3. Output-Voltage Adjustments

Test Points*	Acceptable Voltage	Output Voltage Adjustment Potentiometer	Nominal Output Voltage
P1-1	+14.85 to +15.15 v	R111 (IRO)	+15.00 v
P1-4	+4.95 to +5.05 v	R215 (IRO)	+5.00 v
P1-8	-14.85 to -15.15 v	R310 (IRO)	-15.00 v
*NOTE: Connect voltmeter return to P1-6 (common ground).			

Step 3: Connect variable loadbank to same terminals per table 4. Set loadbank to obtain a current flow below rated output capacity for the particular regulator output under test so that less than maximum load current is drawn.

Step 4: Connect line cord to a-c power.

Table 4. Current-Limiter Check

Voltage Test Point*	Acceptable Start of Current Limiting	Nominal Voltage
P1-1	11.2 ± 0.6 amperes with short-circuit current at 1.5 ± 0.5 amperes	+15.0v
P1-4	53.0 ± 5.0 amperes with short-circuit current at 11.0 ± 4.0 amperes	+5.0v
P1-8	4.0 ± 0.5 amperes with short-circuit current at 0.6 ± 0.3 amperes	-15.0v
*NOTE: Connect voltmeter return to P1-6 (common ground)		

Step 5: Increase the variable load until current limiting occurs per table 4.

Step 6: Repeat all steps for all current limiters.

LINE FAIL PULSES TEST. - Proceed as follows:

Step 1: Disconnect line cord from a-c power.

Step 2: Connect one resistor, 1000 ohm, 1/4W, to terminals P1-2 and P1-4 of disconnect block P1. Connect oscilloscope to terminals P1-2 and P1-6 of disconnect block.

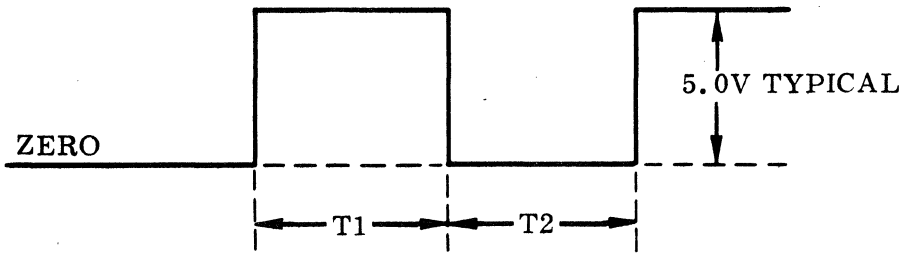
Step 3: Verify that all outputs of the power supply are unloaded.

Step 4: Connect power supply to variable autotransformer and variable autotransformer to a-c power.

Step 5: Increase autotransformer voltage until nominal a-c voltage is obtained.

Step 6: Sync oscilloscope (by connecting TRIGGER INPUT) to terminal marked TP 1 on CCA printed circuit card

Step 7: Decrease power supply input voltage until a train of pulses is observed. Verify that these pulses appear when an input voltage of 70 ± 7 volts, 60 Hz occurs and disappear above this threshold level. Verify that these pulses have the following waveform:



T1 = T2 = 46 to 58 MICROSECONDS

Alternate Method

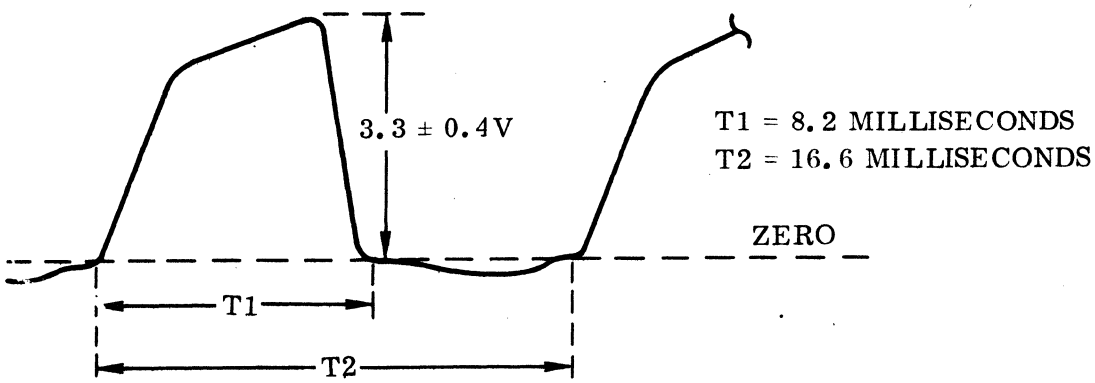
If no variable autotransformer is available, this particular test can be accomplished by disconnecting the power supply line cord from the a-c power and observing the momentary oscilloscope display of the line fail pulses.

LINE FREQUENCY SIGNAL TEST. - Proceed as follows:

Step 1: Connect line cord to a-c power.

Step 2: Connect oscilloscope input leads to terminals P1-3 and P1-6 (common ground) of disconnect block P1.

Step 3: Verify that a train of pulses occurs at the specific time intervals indicated and the following waveform is typical for each of these pulses.



TROUBLE ANALYSIS

Whenever a malfunction occurs, systematically examine the fuse, primary power lines, and external wiring before performing trouble analysis. Usually, power supply malfunctions can be traced to simple causes such as loose supply load connections or accidental short circuit between lead connections on a terminal strip.

During detailed malfunction analysis, refer to schematic diagram SD2003000430-2. Typical malfunction symptoms are listed in Power Supply Trouble Analysis Guide, table 5.

Table 5. Power Supply Trouble-Analysis Guide

Symptom	Possible Cause	Corrective Action
1. Power supply inoperative	No input power	Check for input power presence.
	Fuse F01 open	Check fuse and replace as required.
	Defective Power Inverter transistors (open)	Check and replace as required.
	Overvoltage protection SCR fired	Turn all output voltage-adjust potentiometers fully clockwise. Remove press-on terminal from pin 10 on CCA card. Find malfunctioning series regulator and isolate problem.
	Closed thermostat	Disconnect thermostat ground connection.
2. No output voltage from any regulator (0 volt)	Short circuit in any regulated power source	With a-c power off, check for shorted or open power transistors. Check integrated circuit in feedback loop. Replace any out-of-tolerance semiconductor.
	Short in primary circuit with F01 fuse open	Shorted filter capacitor. Replace input filter capacitor and check input rectifier bridge assembly.
		Shorted rectifier assembly in transformer secondary. Replace shorted rectifier assembly (check filter capacitor charging voltage).

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Table 5. Power Supply Trouble-Analysis Guide (Continued)

Symptom	Possible Cause	Corrective Action
3. Very low voltage at output of any regulator (2 volts or less)	Shorted reverse-polarity protection diode	Disconnect a-c power and check for short with ohm-meter. Replace when damaged. Check out all active components of the regulator.
4. Output voltage from any regulator is below regulation band.	Partial overload causing current limiting.	Remove partial overload
	Associated regulator circuit defective.	Analyze malfunctions of associated regulator.
5. Output voltage from any regulator above regulation band.	Improper output voltage adjustment.	Re-calibrate output voltage.
	Associated regulator circuit (IRO) defective.	Analyze malfunctions of regulator.
6. Output voltage from a regulator cannot be adjusted.	Damaged output voltage adjustment potentiometer.	Replace damaged potentiometer.
7. High ripple from any regulator output.	Output slightly overloaded and current limiter is beginning to function.	Check the current limiter setting per table 4.
		Setting of input voltage levels of series regulator circuits too low. Increase by turning potentiometer R25 on CCA card.
8. LED does not light	Inoperative	Replace damaged LED.
9. Improper line fail pulses	CCA card circuit failure	Check out circuit thoroughly and replace/ repair faults.

Table 5. Power Supply Trouble-Analysis Guide (Continued)

Symptom	Possible Cause	Corrective Action
10. Improper line frequency signal	CCA card circuit failure.	Checkout circuit thoroughly and replace/ repair faults.

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WARNING

D-C VOLTAGES TO 300 VOLTS AND A-C VOLTAGES TO 115 VOLTS ARE USED IN THE POWER SUPPLY. THESE VOLTAGES EXIST WITH HIGH CURRENT CAPABILITY AND ARE HAZARDOUS TO LIFE. BEFORE ATTEMPTING TO REMOVE OR REPLACE ANY POWER SUPPLY COMPONENT, DISCONNECT POWER SUPPLY FROM A-C POWER SOURCE.

HEAT SINKS AND CHASSIS OPERATE AT FAIRLY HIGH TEMPERATURES, RETAINING HEAT FOR SOME TIME AFTER EQUIPMENT IS TURNED OFF. ALLOW AMPLE TIME FOR COOLING AFTER THE POWER-OFF CONDITION BEFORE MAKING CONTACT WITH COMPONENTS.

REPAIR TECHNIQUES

The following techniques are recommended when making repairs.

a. When unsoldering components from a circuit board, never pry or force the part loose; unsolder the component by using the wicking process described below if no vacuum solder removal tool is available:

Step 1: Select a 3/16-inch tinned-copper braid for use as a wick; if braid is not available, select AWG No. 14 or No. 16 stranded wire with 1/2-inch of insulation removed.

Step 2: Dip the wick in liquid rosin flux.

Step 3: Place the wick onto the soldered connection and apply soldering iron to the wick.

Step 4: When sufficient amount of solder flows onto the wick and frees the component, simultaneously remove iron and wick.

b. Always use a heat sink when soldering transistors; a transistor pad with mounting feet is an effective heat sink. Pliers holding the lead being soldered also provide an excellent heat sink.

NOTE

Thermal compound should be applied when replacing some transistors and components. For a list of these components refer to note 207 on sheet 18 of parts list PL2003000430 in the Drawings and Parts Lists section following in this bulletin.

c. Broken or damaged printed circuitry can be repaired by tinning a piece of uninsulated wire first, and holding the wire in place along the damaged printed circuit; flow a little solder along the length of the wire.

CHECKING SEMICONDUCTORS AND CAPACITORS. - Disconnect line cord from a-c power source. Check any transistor with an in-circuit transistor checker. If no checker is available, transistors can be checked with an ohmmeter that has a highly-limited current capability. Observe proper polarity for PNP or NPN to avoid error in measurement. Forward transistor resistance is low but never zero; backward resistance is always higher than the forward resistance. Likewise, check forward and backward resistance of diodes with a multimeter.

Replacement of one part does not always cause elimination of a malfunction. For example, elimination of a malfunction by replacing one transistor can also

cause other transistors to fail. Replacing only one transistor and then reapplying power before checking for additional faulty components can cause damage to the replaced component.

NOTE

Leakage resistance indicated by a simple resistance check of a capacitor is not always an indication of a faulty capacitor. In most instances the capacitors are shunted with resistances, some of which have low values. Only a complete short is a true indication of a shorted capacitor. A charge-discharge test can be used to check filter capacitors.

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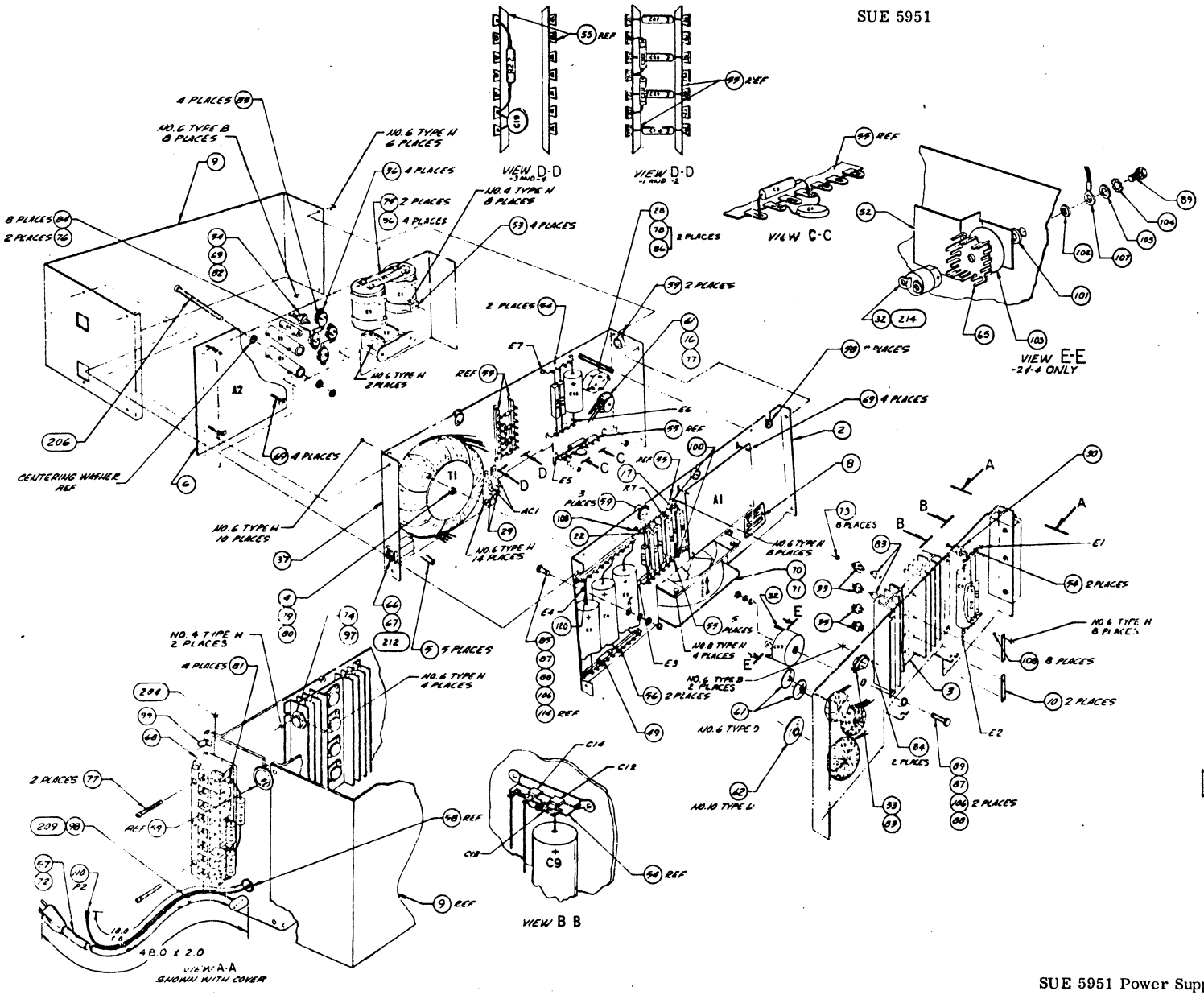
DRAWINGS AND PARTS LISTS

Following is a list of the drawings and parts lists included in this bulletin.

	Drawing Number	Sheets
Power Supply, 5951 Assembly	2003000430-2	1
Power Supply, 5951 Parts List	PL2003000430-2	6 thru 9, 18
Power Supply, 5951 Schematic Diagram	SD2003000430	1
Circuit Card Assembly, CCA	2001002156-1	1
Circuit Card Assembly, CCA Parts List	PL2001002156-1	2, 3, 6
Circuit Card Assembly, IRO	2001002157-1	1
Circuit Card Assembly, IRO Parts List	PL2001002157-1	2, 3, 8



	-2	5951	115VAC, 60HZ	+5V 38A, +1 -15V 3A (VI

SUE 5951 Power Supply Assembly
2003000430-2, Rev. G, Sheet 1

PS1

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2003000430-2		ASSEMBLY		SUE 5951	1
002		001	0001		1001004755-1		PLATE, LEFT SIDE			2
003		001	0001		1001004756-1		HEAT SINK			3
004		001	0001		1001004508-1		WASHER, RETAINING			4
005	F	005	0001		1005000793-1		STANDOFF			5
006		001	0001		2001002156-1		CCA-CKT CARD ASSY		A2 NOTE 216	6
007		001	0001		2001002157-1		IRO-CKT CARD ASSY		A1 NOTE 216	7
008		001	0001		1005000777-1		NAMEPLATE		NOTE 202	8
009		001	0001		1001004769-1		COVER			9
010		002	0001		1001004866-1		BUS BAR			10
011	E	001	0001		8001400080-1		TRANSFORMER, POWER		T1	11
012		001	0001		P6375	80089	TRANSFORMER	CHICAGO STANCOR	T2	12
013	E	001	0001		8001400082-1		REACTOR		L2	13
014	E	001	0001		8001400093-1		REACTOR		L3	14
015	E	001	0001		8001400084-1		REACTOR		L4	15
016	E	001	0001		8001400085-1		REACTOR, INPUT BALUN		L1	16
017	B	004	0001		TYPE 1700S	00213	RESISTOR	SAGE	R6 THRU R9 1700S-.050HM3PCT	17
018	B	001	0001		TYPE 2D-2	75042	RESISTOR	IRC, INC	R2 2D-2 OHM 5PCT VERT MTG KIT NOTE 206	18
019	B	001	0001		TYPE 2D-.25	75042	RESISTOR	IRC, INC	R1 2D-.25 OHM 10PCT VERT MTG KIT NOTE 206	19
020	B	001	0001		TYPE 2D-1500	75042	RESISTOR	IRC, INC	R3 2D-1500 OHM 5PCT VERT MTG KIT NOTE 206	20
021	B	001	0001		TYPE PW5-.25	75042	RESISTOR	IRC, INC	R10 PW5-.25 OHM10PCT	21
022	B	002	0001		TYPE PW10-15	75042	RESISTOR	IRC, INC	R11,12 PW10-15 OHM5PCT	22
023	B	004	0001		TYPE PW10-.18	75042	RESISTOR	IRC, INC	R4,5,13,14 PW10-.18OHM10PCT	23
024		002	0001		20AWG WHT		TUBING (TEFLON)	MIL-I-22129	APPROX FT REQD	24
025		000								25
026		002	0001		1N4004		DIODE		CR11,12	26
027		004	0001		1N4720	09423	DIODE	SCIENTIFIC CMPT	CR7 THRU CR10	27
028		001	0001		MDA962-3	04713	FULL WAVE BRIDGE	MOTOROLA	CR1	28
029		002	0001		SCPA1	14099	RECTIFIER	SEMTECH	CR2,5 NOTE 207	29
030		001	0001		40HF5	81483	DIODE	INTL RECTIFIER	CR6	30
031		000								31

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	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
032		001	0001		SCSPFIL	14099	RECTIFIER, ASSY	SEMTECH	CR3 NOTE 207	32
033		003	0001		8001200021-1		TRANSISTOR		Q6,7,10	33
034		001	0001		2N685		SCR		Q5	34
035		002	0001		2N5685	04713	TRANSISTOR	MOTOROLA	Q8,9 NOTE 207	35
036		004	0001		DTS-430	16758	TRANSISTOR	DELCO RADIO	Q1 THRU Q4	36
037		001	0001		1001004754-4		PLATE, RIGHT SIDE			37
038		000								38
039	F	003	0001		8001300101-1		CAPACITOR		C12,13,14	39
040		002	0001		71C200JB1151	99392	CAPACITOR	STM	C1,2	40
041		001	0001		DD1032	71690	CAPACITOR	CENTRALAB	C4	41
042		001	0001		ZD6A274	02980	CAPACITOR	ELPAC	C3	42
043		000								43
044		003	0001		8001300392-1		CAPACITOR		C16,17,18	44
045		001	0001		39D118G050HP4	56289	CAPACITOR	SFRAGUE	C7	45
046		002	0001		39D228G025HP4	56289	CAPACITOR	SPRAGUE	C9,15	46
047		001	0001		39D238G050JT4	56289	CAPACITOR	SPRAGUE	C5	47
048		001	0001		TCG123U015N3L3P	90201	CAPACITOR	MALLORY	C6	48
[illegible]		000	0001		TVA1175.8	56289	CAPACITOR	SPRAGUE	C6	48A
[illegible]		001	0001		8001300333-2		CAPACITOR		C8	49
050		002	0001		TE1213	56289	CAPACITOR	SPRAGUE	C10,11	50
051		000								51
052		001	0001		1001005347-1		BRACKET, RECTIFIER			52
053		004	0001		6179-2A	91506	CLIP, COMPONENT	AUGAT	(C1,C2)	53
054		004	0001		326-20-04-001	71785	TERMINAL STRIP	CINCH	TB1,2,8,9	54
055		005	0001		326-20-07-001	71785	TERMINAL STRIP	CINCH	TB3,4,7,10,11	55
056		002	0001		326-20-10-001	71785	TERMINAL STRIP	CINCH	TB5,6	56
057		001	0001		SCR11-2	28520	BUSHING	HEYMAN MFG		57
058		004	0001		OCB-500	28520	BUSHING, OPEN/CLOSE	HEYMAN MFG		58
059		003	0001		OCB-875	28520	BUSHING, OPEN/CLOSE	HEYMAN MFG		59
060		000								60
061		003	0001		100-5	08289	RETAINER, TOROID	DELBERT BLINN	(L2,L4)	61
062		001	0001		100-6	08289	RETAINER, TOROID	DELBERT BLINN	(L3)	62
063		001	0001		NY25-030	08289	INSULATOR, NYLON	DELBERT BLINN		63
064		000								64
065		001	0001		UP-TE28-CB	98978	HEAT SINK	IERC	(CR3)	65
066		001	0001		348875	75915	FUSE HOLDER	LITTELFUSE	XF1	66
067		001	0001		314010	75915	FUSE	LITTELFUSE	F1(3AB 10A 250V)	67
068		001	0001		11978-82	11873	DISCONNECT BLOCK	UNDERWRITERS SAFETY DEVICE CO	P1 (FEMALE)	68
069		008	0001		LCBS-10N	06915	SUPPORT, CIRCUIT BD	RICHCO PLASTIC		69
070		001	0001		1005000906-1		FAN		B1 (115CFM, 115VAC)	70

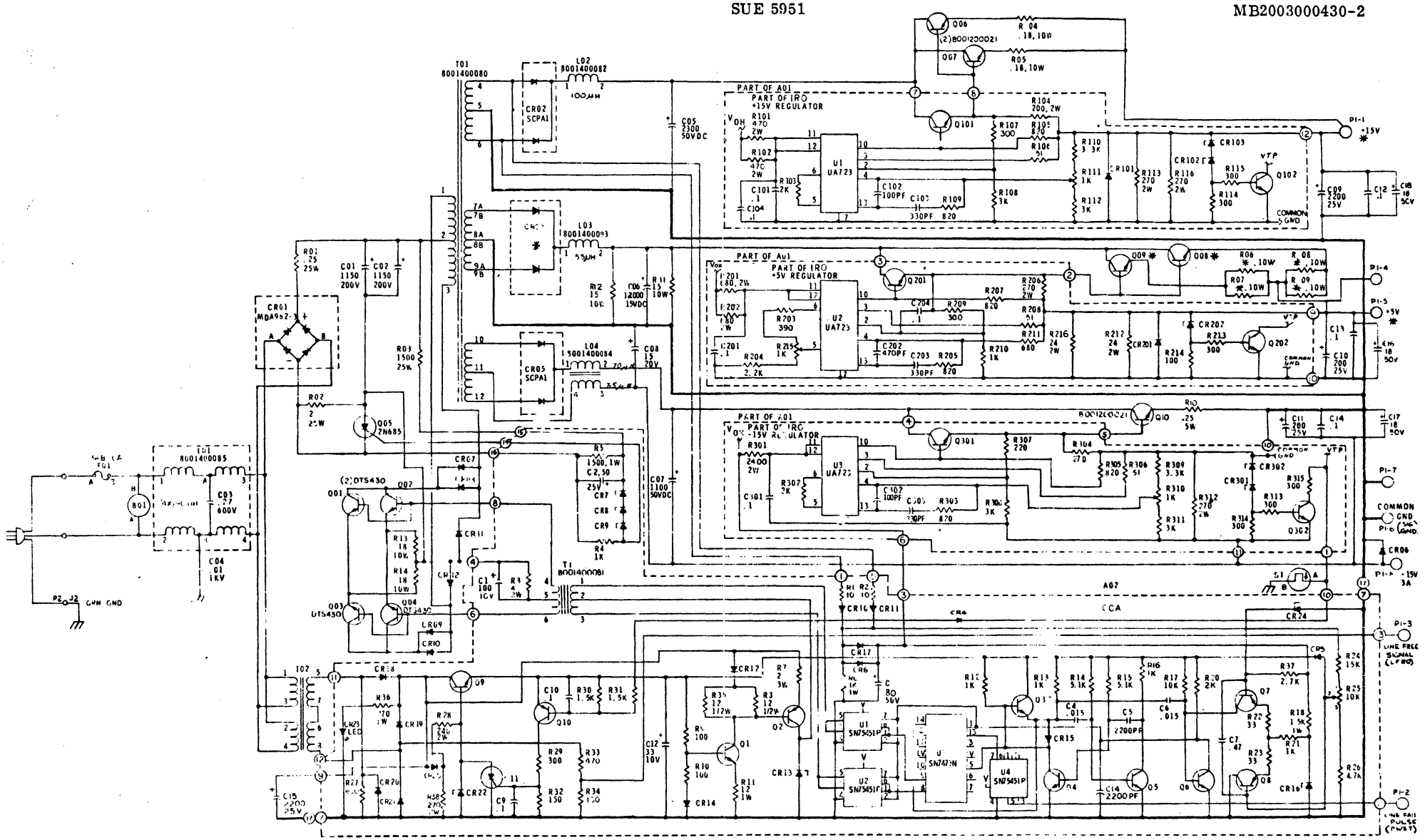
	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
071		001	0001		C-2055-015-BL	80126	LINE CORD, FAN	PACIFIC ELECTRICORD CO		71
072		001	0001		C1316-006-BL	80126	LINE CORD, AC	PACIFIC ELECTRICORD CO	6FT. 16/3	72
073	B	008	0001		TYPE 511-061800	78189	NUT, LOCK	SHAKEPROOF	511-061800-01-0251-0551	73
074	B	001	0181		TYPE 430-764	93410	THERMOSTAT	ESSEX INTL INC	S1 430-764 CL 210 DEG OPEN 195 DEG NOTE 207	74
075		002	0001		1001004866-3		BUS BAR			75
076		002	0001		1001004866-2		BUS BAR			76
077		003	0001		MS51957-35	96906	SCREW, PAN HD		6-32 X 1.25 LG	77
078	F	002	0001		9002200582-1		SCREW, PAN HD		4-40 X 1.00 LG	78
079		001	0001		MS51957-54	96906	SCREW, PAN HD		8-32 X 2.25 LG	79
080		001	0001		22NM832	15653	NUT, LOCK	KAYNAR	8-32	80
081		004	0001		1005000786-2		LUG			81
082		001	0001		60-11-4661-1662	18565	INSULATOR	CHOMERICS	(Q5)	82
083		007	0001		60-11-4305-1662	18565	INSULATOR	CHOMERICS	(Q1 THRU Q4,Q6, 7,10)	83
084		010	0001		495334-7	02735	WASHER, NYLON	RCA		84
085		001	0001		MS90725-4	96906	SCREW, CAP, HEX HD		1/4-20 X .56 LG	85
086		002	0001		MS15795-804	96906	WASHER, FLAT		NO. 4	86
087		001	0001		MS35338-44	96906	WASHER, LOCK		NO. 1/4	87
088		002	0001		MS35649-2252	96906	NUT, HEX		1/4-20	88
089		001	0001		MS90725-32	96906	SCREW, CAP, HEX HD		5/16-18 X .75 LG	89
090	F	003	0001		9003400421-18		WIRE, STRANDED		14AWG WHT APPROX FT REQD	90
091	F	030	0001		9003400421-16		WIRE, STRANDED		16AWG WHT APPROX FT REQD	91
092	F	003	0001		9003400421-15		WIRE, STRANDED		16AWG BLK APPROX FT REQD	92
093	F	030	0001		9003400421-12		WIRE, STRANDED		20AWG WHT APPROX FT REQD	93
094		003	0001		AWG18 TYPE S		WIRE, SOLID, UNINSUL	QQ-W-343	NOTE 216 APPROX FT REQD	94
095	F	003	0001		9003400419-9		WIRE, SOLID, UNINSUL		20AWG APPROX FT REQD	95
096		004	0001		MS35335-32	96906	WASHER, EXT TOOTH		NO. 10	96
097		A/R	0001		NO. 340	71984	SILICONE HT SK CMPD	DOW CORNING	NOTE 207	97
098		001	0001		MS3367-5	96906	STRAP TIEDOWN		NOTE 209	98
099	F	001	0001		1005000787-22		TERMINAL, TAB		J1	99
100		002	0001		MS15795-805	96906	WASHER, FLAT		NO. 6	100
101		001	0001		2322-N317	06540	WASHER, INSULATING	AMATOM	NO. 5/16	101
102		001	0001		2718-49550-N317	06540	WASHER, SHOULDER	AMATOM	NO. 5/16	102
103		001	0001		MM-1000-328-006	08289	WASHER, MICA	DELBERT BLINN	(CR3)	103
104		001	0001		MS35335-34	96906	WASHER, LOCK		NO. 5/16	104
105		001	0001		MS27183-12	96906	WASHER, FLAT		NO. 5/16	105
106		001	0001		MS27183-10	96906	WASHER, FLAT		NO. 1/4	106

PSI

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
107		001	0001		MS25036-109	96906	LUG, RING		14-16AWG NO.5/16 NOTE 211	107
108	B	008	0001		TYPE 2636-24850	06540	WASHER, SHOULDER	AMATOM	2636-24850-PM140	108
109	E	004	0001		10050000785-14		LUG, RING		16-24AWG NO. 10 NOTE 211 APPROX QTY REQD	109
110	E	006	0001		10050000787-3		TERMINAL RECPT		FASTON 250 16-14AWG NOTE 211 APPROX QTY REQD	110
111	E	001	0001		10050000785-20		LUG, RING		12-10AWG NO. 1/4 NOTE 211 APPROX QTY REQD	111
112		A/R	0001		2005000001-1		SUBSTITUTE KIT		FOR FIND NO. 40 (C1,2)	112
113	E	006	0001		10050000785-7		LUG, RING		22-18AWG NO. 6 NOTE 211 APPROX QTY REQD	113
114	E	004	0001		10050000785-15		LUG, RING		16-14AWG NO. 1/4 NOTE 211 APPROX QTY REQD	114
115	E	002	0001		10050000787-1		TERMINAL RECPT		FASTON 250 22-18AWG NOTE 211 APPROX QTY REQD	115
116	E	006	0001		10050000785-12		LUG, RING		14-16AWG NO. 6 NOTE 211	116
117	E	004	0001		10050000787-5		TERMINAL RECPT		FASTON 250 12-14AWG APPROX QTY REQD	117
118		A/R	0001		SN60/SN63		SOLDER	QQ-S-571	NOTE 216	118
119		002	0001		34306	00779	SPLICE	AMP, INC	16-14AWG APPROX QTY REQD	119
120		001	0001		18AWG WHT		TUBING (TEFLON)	MIL-I-22129	APPROX FT REQD	120
121		REF	0001		SD2003000430-2		SCHEMATIC DIAGRAM			121
122		REF	0001		WL2003000430-1		WIRE LIST			122
123		REF	0001		AP2003000430-2		ACCEPTANCE TEST PROC			123
124		000								124
125		000								125
126		000								126
127		000								127
128		REF	0001		DS2003000430-2		DESIGN SPECIFICATION			128

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTE:			200
201		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			201
202		A/R	0001		LECP1049-16		MARK FIND NUMBER 8 .09 HIGH CHARACTERS (TYPEWRITER MAY BE USED) AS FOLLOWS: TOP BLOCK: UNIT TITLE 2ND BLOCK: PART NUMBER 3RD BLOCK: SERIAL NUMBER 4TH BLOCK: 105-125VAC 47-63HZ			202
203		000								203
204		REF	0001				ALLOW .010 TO .040 GAP FOR CONNECTOR FLOAT ALIGNMENT.			204
205		A/R	0001		LECP1075		HARDWARE.			205
206		REF	0001				INSTALL R1,2,3 USING SCREW, CENTERING WASHER, LOCK-WASHER AND NUT FROM VERTICAL MOUNTING KIT. DISCARD UNUSED HARDWARE.			206
207		A/R	0001				MOUNT Q8 AND Q9, CR2,3,5, S1 USING THERMAL COMPOUND FIND NO. 97.			207
208		000								208
209		REF	0001				INSTALL FIND NO. 98 TO ALLOW FOR ADJUSTMENT BETWEEN FIND NO. 72 AND GREEN WIRE.			209
210										210
211		REF	0001		WL2003000430		SEE WIRE LIST FOR LOCATION.			211
→		REF	0001				INSTALL FIND NO. 110 (TERMINAL) ON FIND NO. 66 (FUSE HOLDER) PRIOR TO INSTALLING FIND NO. 67 (FUSE) INTO FUSE HOLDER.			212
213		000								213
214		REF	0001				BEND LUGS 90 DEGREES, STARTING BEND .12 FROM DIODE. CAUTION: DO NOT FRACTURE INSULATION.			214
215		A/R	0001		LECP1049-16		MARK FIND NUMBER 8 .09 HIGH CHARACTERS (TYPEWRITER MAY BE USED) AS FOLLOWS: TOP BLOCK: UNIT TITLE 2ND BLOCK: PART NUMBER 3RD BLOCK: SERIAL NUMBER 4TH BLOCK: 200-240 VAC, 47-53HZ			215
216		A/R	0001				INSTALL FIND NUMBER 93 ON FIND NUMBERS 6 AND 7 BY INSERTING IN .060 DIAMETER HOLE AND SOLDERING WITH FIND NUMBER 118.			216
217		000								217
218		REF	0001				LOCATE AND TIE ALL WIRE BUNDLES TO PREVENT CONTACT WITH HEAT SINKS AND FAN BLADES.			218

PSI



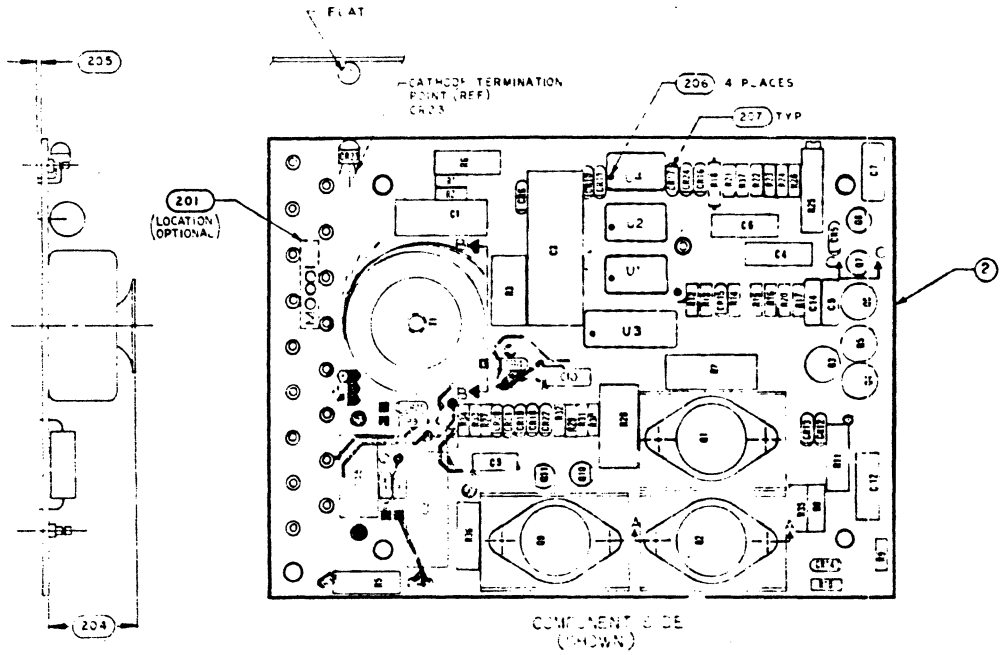
NOTES:
1. UNLESS OTHERWISE SPECIFIED
   - RESISTANCE VALUES ARE IN OHMS, 1/4W.
   - CAPACITANCE VALUES ARE IN MICROFARADS.

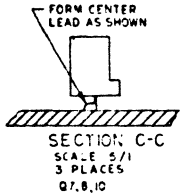
* TABLE

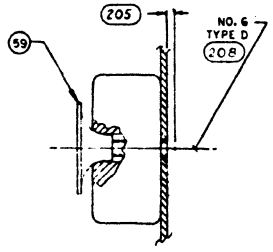
SCHEMATIC NO.	MODEL NO.	DESCRIPTION CR03				
SD2003000430-1	5950	SCPA01A	30A	10A	2N5883	.01Ω
SD2003000430-2	5951	SCSPE1L	30A	7A	2N5683	.035Ω

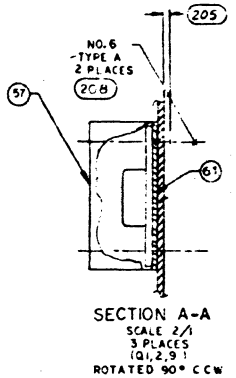
SUE 5951 Power Supply Schematic Diagram
SD2003000430 Rev. D, Sheet 1

PS1









SUE 5951 Circuit Card Assembly, CCA
2001002156 . Rev. D, Sheet 1

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	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002156-1		CCA-CKT CARD ASSY		USED ON SUE 5950,5951,5952, 5953	1
002		001	0001		1001004757-1		PRINTED WRG BD, CCA			2
003	F	001	0001		8001800098-1		ICP		U3 (7473)	3
004		003	0001		SN75451P	01295	ICP	TEXAS INSTR INC	U1,2,4	4
005		001	0001		PW2-4 OHMS	75042	RESISTOR	IRC, INC	R3 1.10 IS	5
006		001	0001		8001300314-1		CAPACITOR		C1 1.10 IS	6
007		001	0001		MTA50E25	90201	CAPACITOR	MALLORY CAP. CO	C2 1.25 IS	7
008		001	0001		MTA80F50	90201	CAPACITOR	MALLORY CAP. CO	C3 1.70 IS	8
009		001	0001		RL42S271G		RESISTOR	MIL-R-22684/4	R38 1.0 IS	9
010		002	0001		192P15392	56289	CAPACITOR	SPRAGUE ELEC	C4,6 .80 IS	10
011		001	0001		8001300311-2		CAPACITOR		C12 .80 IS	11
012		001	0001		1N5160		DIODE		CR25 .5 IS	12
013	F	002	0001		8001300017-1		CAPACITOR		C5,14 .20 IS	13
014	F	002	0001		8001300101-1		CAPACITOR		C9,10 .25 IS	14
015	F	001	0001		8001300102-1		CAPACITOR		C7 .375 IS	15
016		001	0001		1N4734		DIODE, ZENER		CR13 .5 IS	16
017	E	001	0001		8001400081-1		TRANSFORMER		T1	17
018	E	004	0001		8001200001-1		TRANSISTOR		Q3,4,5,6 (TO18)	18
019		002	0001		2N3054		TRANSISTOR		Q1,9 (TO66)	19
020		001	0001		2N4898		TRANSISTOR		Q2 (TO66)	20
021		001	0001		2N5060		SCR		Q11 (TO18)	21
022		003	0001		2N5354		TRANSISTOR		Q7,8,10 (TO18)	22
023		002	0001		S2F	14099	DIODE	SEMTECH	CR10,11 .5 IS	23
024		001	0001		1N751A		DIODE, ZENER		CR24 .5 IS	24
025		001	0001		1N752A		DIODE, ZENER		CR22 .5 IS	25
026		001	0001		1N758A		DIODE, ZENER		CR16 .5 IS	26
027		005	0001		1N4002		DIODE		CR12,18,19,20,21 .5 IS	27
028		003	0001		1N4735		DIODE, ZENER		CR7,8,9 .5 IS	28
029	E	006	0001		8001100001-1		DIODE		CR4,5,6,14,15,17 .5 IS	29
030	E	001	0001		1005000837-1		DIODE		CR23	30
031		001	0001		RL07S471G		RESISTOR	MIL-R-22684/1	R33 .5 IS	31
032		001	0001		3007P-1-103	80294	RESISTOR, POT.	BOURNS, INC	R25	32
033		001	0001		PW3-2 OHMS	75042	RESISTOR	IRC, INC	R7 1.10 IS	33
034	B	001	0001		TYPE RLS-1A	91637	RESISTOR	DALE ELEC INC	R18 .425 IS RLS-1A,1.5K OHMS 3 PERCENT, 1W	34

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	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		RL42S241G		RESISTOR	MIL-R-22684/4	R28 1.0 IS	35
036		001	0001		RL32S102G		RESISTOR	MIL-R-22684/3	R6 .8 IS	36
037		001	0001		RL32S120G		RESISTOR	MIL-R-22684/3	R11 .8 IS	37
038		001	0001		RL32S152G		RESISTOR	MIL-R-22684/3	R5 .8 IS	38
039		001	0001		RL32S271G		RESISTOR	MIL-R-22684/3	R36 .8 IS	39
040		002	0001		RL20S120G		RESISTOR	MIL-R-22684/2	R8,35 .6 IS	40
041		005	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R4,12,13,16,21 .5 IS	41
042		002	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R9,10 .5 IS	42
043		002	0001		RL07S512G		RESISTOR	MIL-R-22684/1	R14,15 .5 IS	43
044		001	0001		RL07S103G		RESISTOR	MIL-R-22684/1	R17 .5 IS	44
045		002	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R30,31 .5 IS	45
046		001	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R26 .5 IS	46
047		002	0001		RL07S330G		RESISTOR	MIL-R-22684/1	R22,23 .5 IS	47
048		001	0001		RL07S153G		RESISTOR	MIL-R-22684/1	R24 .5 IS	48
049		001	0001		RL07S621G		RESISTOR	MIL-R-22684/1	R27 .5 IS	49
050		001	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R29 .5 IS	50
051		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R32 .5 IS	51
052		001	0001		RL07S202G		RESISTOR	MIL-R-22684/1	R20 .5 IS	52
053		001	0001		RL07S272G		RESISTOR	MIL-R-22684/1	R37 .5 IS	53
054		001	0001		RL07S131G		RESISTOR	MIL-R-22684/1	R34 .5 IS	54
055		002	0001		RL07S100G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	55
056		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		56
057		003	0001		6166B-BASE	13103	HEAT SINKS	THERMALLOY CO	(TO66)	57
058		000								58
059		001	0001		100-5	08289	RETAINER, TOROID	DELBERT BLINN		59
060		REF	0001		SD2003000430-1		SCHEMATIC DIAGRAM			60
061		003	0001		DF31A	02735	INSULATOR, MICA	RCA	MAY BE FURNISHED WITH Q1,2,9	61
062		REF	0001		SD2003000430-2		SCHEMATIC DIAGRAM			62

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		REF	0001		LECP1049-17		MARKING.			201
202		REF	0001				PRINTED WIRE CIRCUITRY SHOWN IS PHYSICALLY ON COMPONENT SIDE.			202
203		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			203
204		REF	0001				COMPONENT HEIGHT .70 MAX.			204
205		REF	0001				LEAD PROTRUSION (SIDE 2) .075 MAX. HARDWARE PROTRUSION .160 MAX.			205
206		REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			206
207		REF	0001				SQUARE PAD DENOTES CATHODE END OF DIODE.			207
208		A/R	0001		LECP1075		HARDWARE.			208

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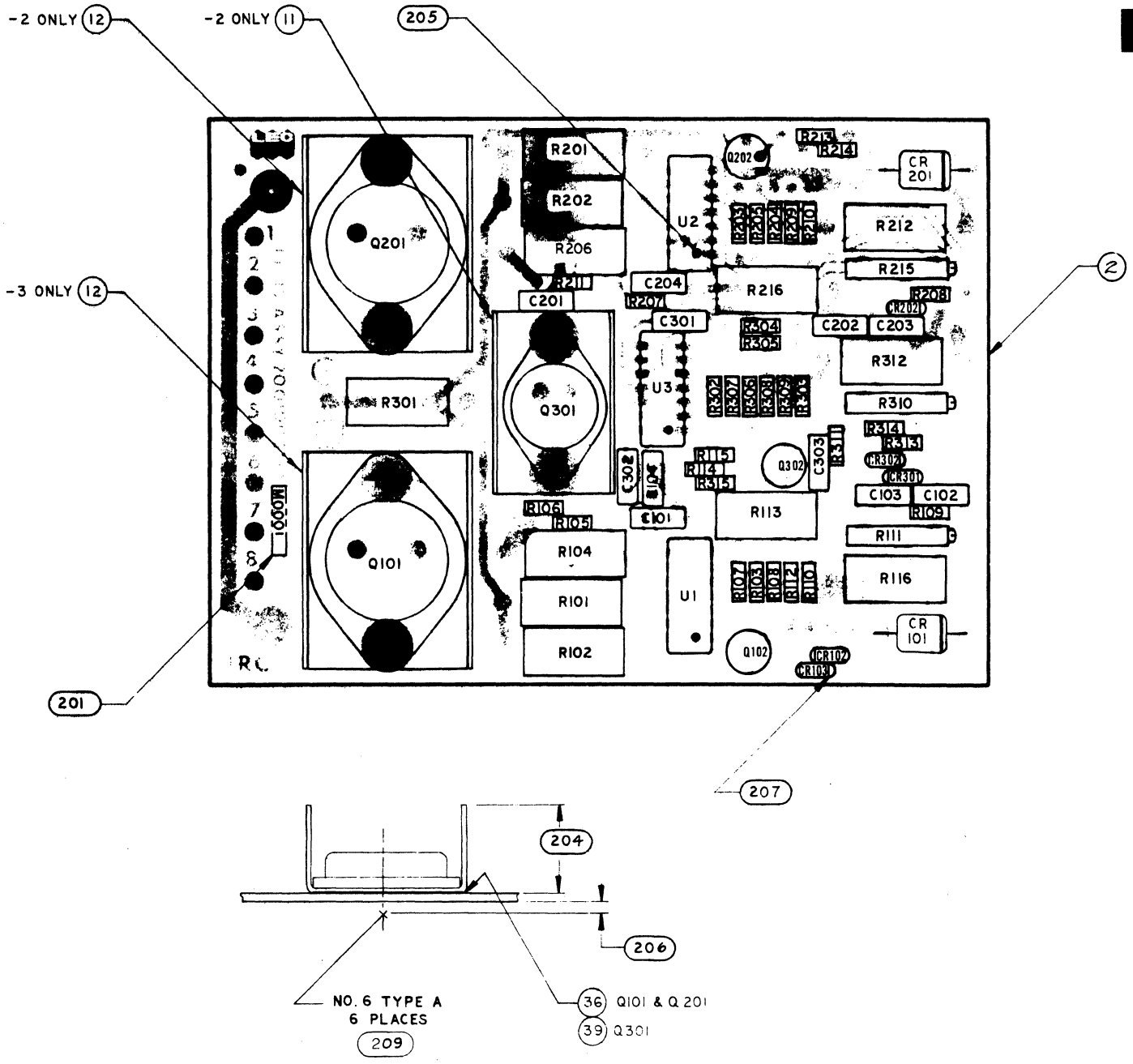

SUE 5951 Circuit Card Assembly, IRO
2001002157-1, Rev. B, Sheet 1

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002157-1		IRO-CKT CARD ASSY		USED ON SUE 5950/5951	1
002		001	0001		1001004758-2		PRINTED WRG BD, IRO			2
003		002	0001		1N4720	13327	DIODE	SOLITRON	CR101, CR201 .625 IS	3
004		002	0001		1N756A		DIODE, ZENER		CR102, CR301 .5IS	4
005		001	0001		1N752A		DIODE, ZENER		CR202 .5 IS	5
006		002	0001		1N757A		DIODE, ZENER		CR103, CR302 .5IS	6
007	E	001	0001		8001200021-1		TRANSISTOR		Q101 (TO-3)	7
008	E	003	0001		8001200001-1		TRANSISTOR		Q102, 202, 302 (TO-18)	8
009		001	0001		2N3771	04713	TRANSISTOR	MOTOROLA	Q201 (TO-3)	9
010		001	0001		2N3054		TRANSISTOR		Q301 (TO-66)	10
011		002	0001		RL42S471G		RESISTOR	MIL-R-22684/4	R101, 102 1.0 IS	11
012		001	0001		DM15F471J	72136	CAPACITOR	EL MENCO	C202 .25 IS	12
013	E	005	0001		8001300101		CAPACITOR		C201, 204, 301, 101, 104 .25 IS	13
014		002	0001		CM05FD101J03		CAPACITOR	MIL-C-5/18	C102, 302 .25 IS	14
015		003	0001		3007P-1-102	80294	RESISTOR, VARIABLE	BOURNS, INC	R111, 215, 310	15
016		003	0001		CM05FD331J03		CAPACITOR	MIL-C-5/18	C103, 203, 303 .25 IS	16
017		003	0001		U6A7723393	07263	ICP	FAIRCHILD	U1, 2, 3	17
018		002	0001		RL07S202G		RESISTOR	MIL-R-22684/1	R103, 302 .5 IS	18
019		006	0001		RL07S821G		RESISTOR	MIL-R-22684/1	R303, 305, 105, 109, 207, 205 .5IS	19
020		004	0001		RL07S302G		RESISTOR	MIL-R-22684/1	R108, 112, 308, 311 .5 IS	20
021		008	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R107, 114, 115, 209, 213, 315, 314, 315 .5 IS	21
022		002	0001		RL07S332G		RESISTOR	MIL-R-22684/1	R110, 309 .5 IS	22
023		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R210 .5 IS	23
024		001	0001		RL07S681G		RESISTOR	MIL-R-22684/1	R211 .5 IS	24
025		001	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R214 .5 IS	25
026		001	0001		RL07S271G		RESISTOR	MIL-R-22684/1	R304 .5 IS	26
027		001	0001		RL07S241G		RESISTOR	MIL-R-22684/1	R307 .5 IS	27
028		001	0001		RL07S391G		RESISTOR	MIL-R-22684/1	R203 .5 IS	28
029		001	0001		RL07S222G		RESISTOR	MIL-R-22684/1	R204 .5 IS	29
030		001	0001		RL42S201G		RESISTOR	MIL-R-22684/4	R104 1.0 IS	30
031		002	0001		RL42S681G		RESISTOR	MIL-R-22684/4	R201, 202 1.0 IS	31
032		004	0001		RL42S271G		RESISTOR	MIL-R-22684/4	R113, 116, 206, 312 1.0 IS	32

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
033		001	0001		RL42S242G		RESISTOR	MIL-R-22684/4	R301 1.0 IS	33
034		002	0001		RL42S240G		RESISTOR	MIL-R-22684/4	R212,216 1.0 IS	34
035		000								35
036		002	0001		495320	02735	INSULATOR, MICA	RCA	MAY BE FURNISHED WITH Q101 AND Q201	36
037		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		37
038		REF	0001		SD2003000430-1		SCHEMATIC DIAGRAM			38
039		001	0001		DF31A	02735	INSULATOR, MICA	RCA	MAY BE FURNISHED WITH Q301	39
040		003	0001		RL07S510G		RESISTOR	MIL-R-22684/1	R306,208,106 .5 IS	40

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	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARKING.			201
202		REF	0001				PRINTED CIRCUITRY SHOWN IS PHYSICALLY ON COMPONENT SIDE.			202
203		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATION.			203
204		REF	0001				COMPONENT HEIGHT .70 MAX.			204
205		REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			205
206		REF	0001				LEAD PROTRUSION (SIDE 2) .075 MAX. HARDWARE PROTRUSION .160 MAX.			206
207		REF	0001				SQUARE PAD AND/OR STRIPE DENOTES CATHODE END OF DIODE.			207
208		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING, FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209		A/R	0001		LECP1075		HARDWARE.			209

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

PS1

SEE PS1-02

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER

APP'D FOR REL 751206

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PS1 SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		PS1-20

SCALE	REV	SHEET 1 OF 1

External Power Supply

PS2-Ø2 Logic Description

PS2-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12/19/75	

PS2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN 12/19/75	
	CHECKER	DRAWING TITLE PS2 LOGIC DESCRIPTION
	ENGINEER	
	APP'D FOR REL	SIZE: A; CODE IDENT NO.; DRAWING NO.: PS2-Ø2
	APP'D (CUSTOMER)	SCALE; REV 1/1; SHEET OF

PS2

SUE 5952 EXTERNAL POWER SUPPLY

MAINTENANCE BULLETIN M5952

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SUE 5952 EXTERNAL POWER SUPPLY

MAINTENANCE BULLETIN M5952

INTRODUCTION

This bulletin contains general and detailed information about the SUE 5952 External Power Supply, manufactured by Lockheed Electronics Company, Inc. SUE 5952, a self-contained power conditioning system, is designed to power SUE computer system configurations containing more than 16 SUE circuit cards.

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DESCRIPTION

Two separate power supplies are contained in the 5952: LEC part numbers 2002001206 and 2002001251. See Figures 1a, 1b, 2a, and 2b. Both supplies are similar and differ only in output voltages and load currents delivered to the computer system. Type 2002001206 supplies +5 volts at 50 amperes and -15 volts at 5 amperes; type 2002001251 supplies +15 volts at 25 amperes.

Both power supplies plug into a SUE 7905 Card Guide Frame that forms the 5952 chassis. The chassis dimensions are 7-inches high, 17-inches wide and 18-inches deep. The 5952 weighs approximately 50 pounds. With a fan pack assembly attached to the bottom, the 5952 assembly is 8-3/4 inches high and weighs approximately 63 pounds.

Each of the two power supplies is protected by a 10-ampere fuse (3AB-10) mounted in each respective front panel. A Light Emitting Diode (LED), visible through the POWER ON opening in each front panel, lights when ac power is applied.

Line power of 105-125 volts, 47-63 Hz, is applied through a 15-foot, 12 AWG, Type S, 3-conductor cable containing a three-prong, right-angle plug (P4) (NEMA 5-20P). See Figure 1b. Through this cable, ac power is connected

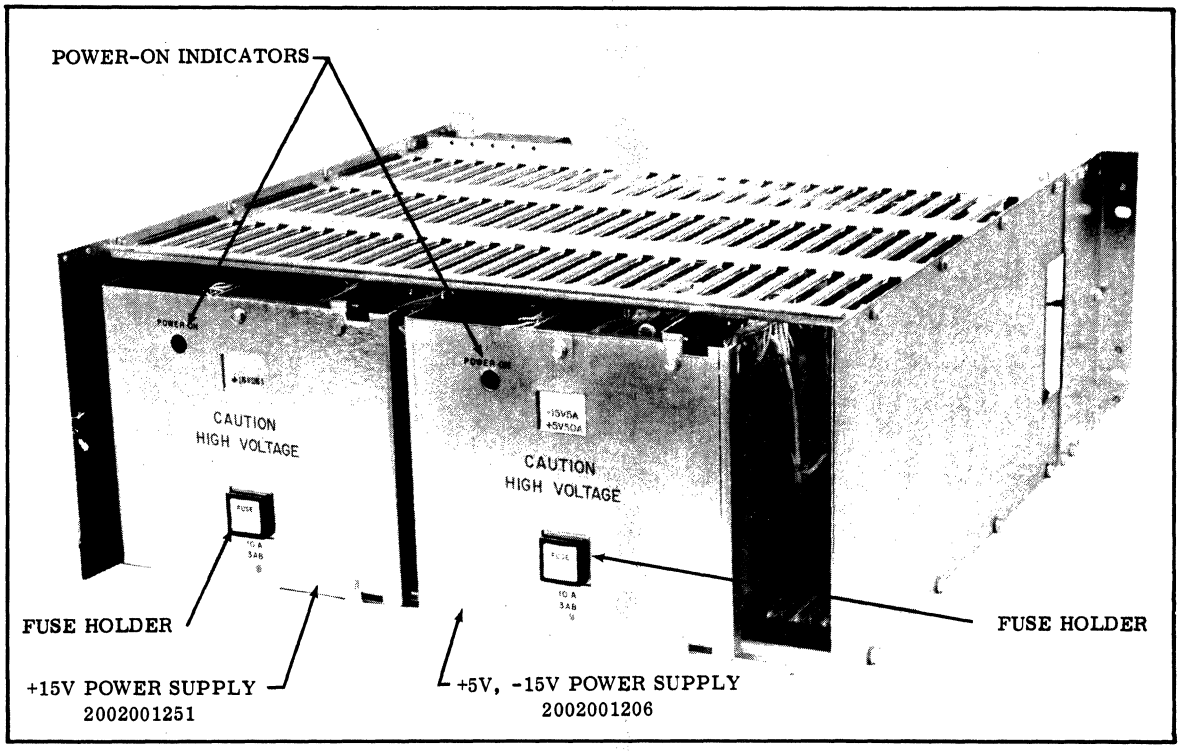


Figure 1a. SUE 5952 Power Supply, Front View

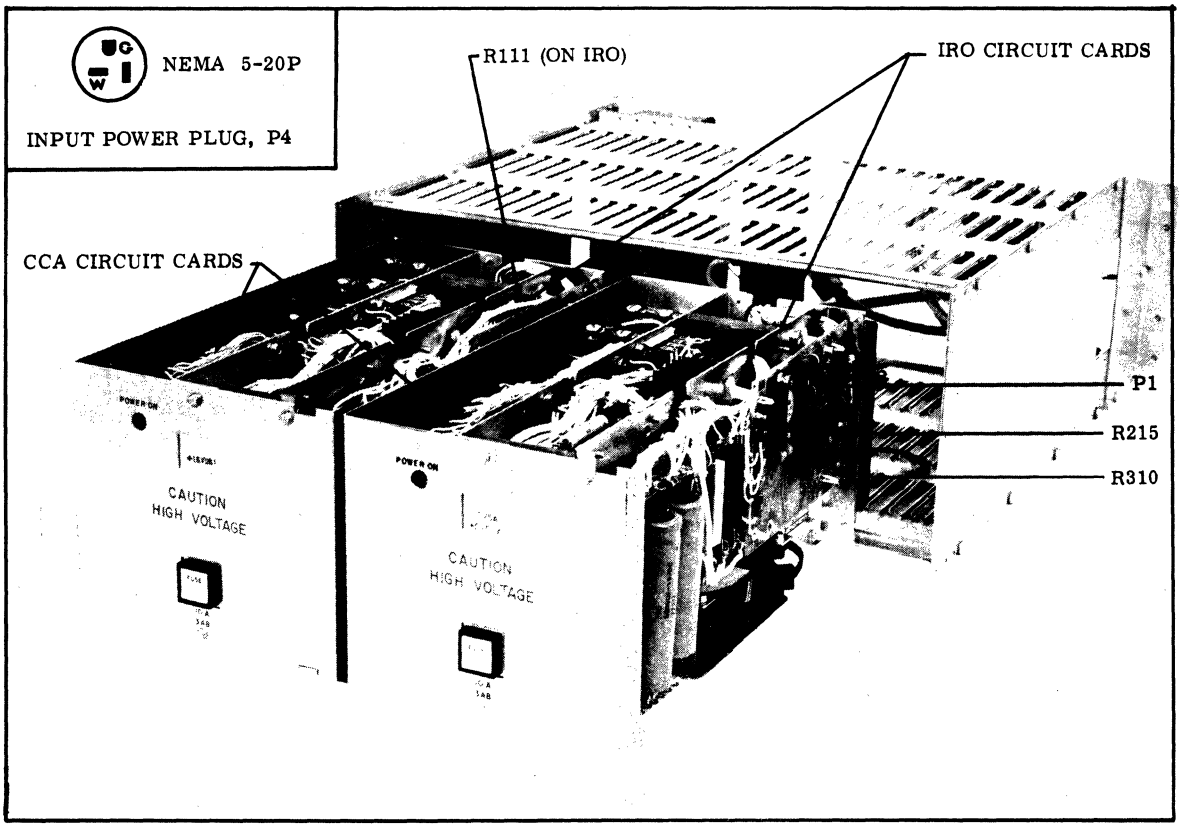


Figure 1b. SUE 5952 Power Supply With Subassemblies Removed

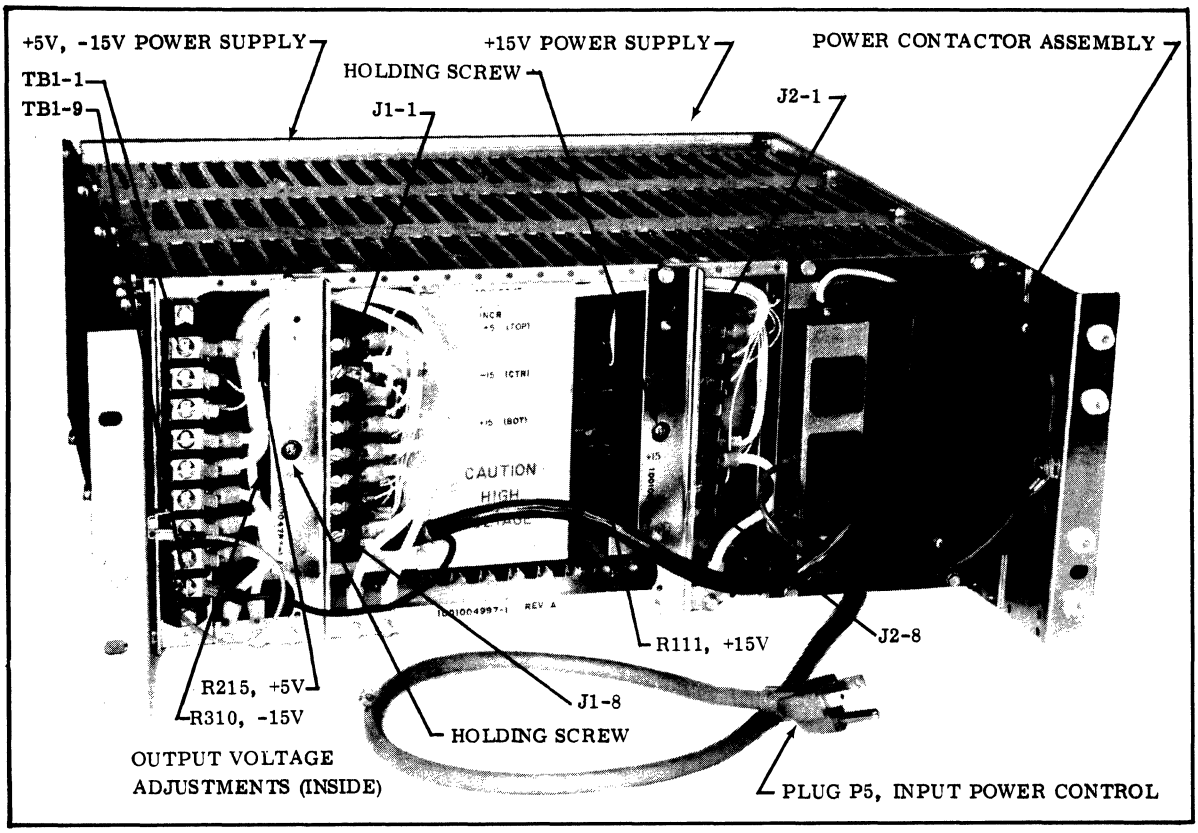


Figure 2a. SUE 5952 Power Supply, Rear View

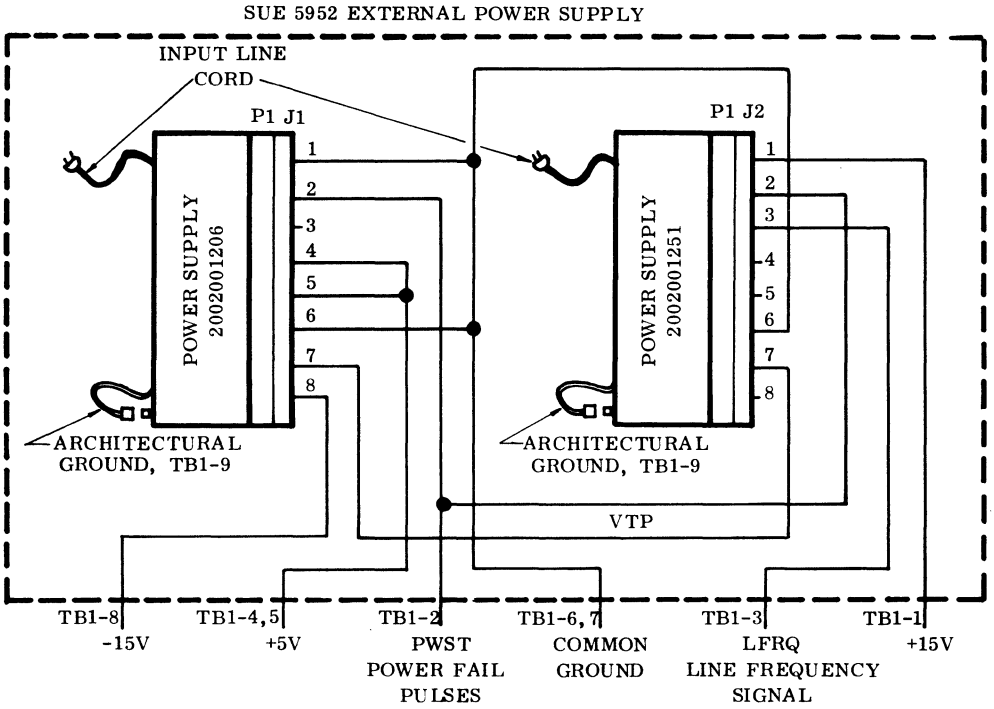


Figure 2b. Power Supply Interconnections and 5952 Outputs

to the Power Contactor Assembly attached to the rear of the 5952. The power contactor assembly contains a power control relay and three convenience ac outlets. Each power supply is plugged into one of the receptacles. The third receptacle can be used to power the fan pack. The relay in the power contactor assembly is actuated through another ac plug (P5) (Figure 2a) that can be plugged into the SUE 2201 or 2202 Keylock Power Distribution Unit so that input ac power can be turned on and off through a keylock switch.

Power consumption of the 5952 at the following levels, for outputs specified, is:

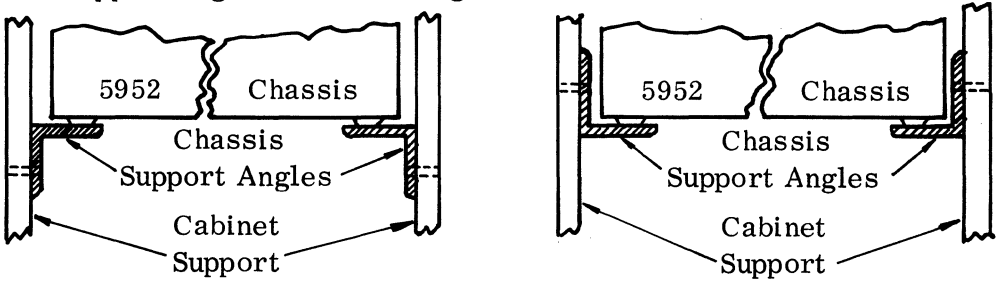
	Type 2002001206		Type 2002001251	
Ac Line	I_{in} (amperes)	P_{in} (watts)	I_{in} (amperes)	P_{in} (watts)
105v	8.6	760	8.9	820
115v	8.1	780	8.4	840
125v	7.8	800	8.2	860

INSTALLATION CONSIDERATIONS

SUE 5952 is designed for installation in a SUE cabinet or any standard 19-inch rack. A SUE 7921 Six Fan Pack Assembly, attached to the bottom of the 5952 chassis, is required for cooling. Complete with fan-pack, the 5952 rests on chassis support angles mounted inside the cabinet on the left- and right-hand sides. Normally, the power supply is placed above the computer chassis in the cabinet.

With all power to the cabinet off, install the 5952 as follows:

a. Install a SUE 7946 chassis support angle kit (LEC part number 2002001429) in the desired location in the cabinet. The kit contains two support angles and mounting hardware.



Method A Method B (Optional)

b. Place the 5952 chassis, with fan pack, onto the support angles and secure the assembly by fastening two machine screws through each mounting flange at the rear of the 5952 chassis.

c. Connect eight solderless electrical leads, supplied with the 5952, between the terminal board on the INFIBUS (computer chassis) and terminal board TB1 on the 5952 as follows:

Power Supply 5952	SUE Computer INFIBUS	Voltage or Signal
TB1-1	J3-1	+15 V
TB1-2	J3-2	PWST
TB1-3	J3-3	LFRQ
TB1-4	J3-4	+5 V
TB1-5	J3-5	+5 V
TB1-6	J3-6	Common Ground
TB1-7	J3-7	Common Ground
TB1-8	J3-8	-15 V

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d. Insert power control plug P5 (Figure 2a) into one of the receptacles in the SUE Power Distribution Unit or other switch-controlled outlet in the cabinet.

e. Assure that the respective power plugs attached to each power supply in the 5952, and the plug for the fan pack, are inserted into the Power Contactor Assembly receptacles. Also assure that the respective chassis ground wires are connected to their respective ground terminals.

REMOVAL AND REPLACEMENT OF POWER SUPPLIES

Both power supplies in the 5952 can be removed from the chassis in the following manner:

a. Disconnect the respective three-prong plug from the receptacle on the power contactor assembly.

b. Disconnect the ground lead attached to the respective line cord.

c. With a cross-head screwdriver, loosen the holding screw (Figure 2a) that secures the disconnect block assembly.

d. Gently pull on the front of the power supply to disengage the disconnect block and slide the power supply out of the 5952 chassis while guiding the line cord and ground lead through their access.

Reverse the procedures in the above steps to replace the power supplies in the 5952 chassis.

POWER SUPPLY CIRCUITS

Circuit components in each of the two power supplies are contained on the respective power supply chassis and on two printed wiring circuit cards: Converter and Control Assembly (CCA) and Inverter Regulator Output (IRO). Simplified schematic and timing diagrams are shown throughout the descriptions that follow. Detailed schematic diagrams (SD2002001206 and SD2002001251) for each power supply are located near the end of this bulletin.

GENERAL CIRCUIT DESCRIPTION (See Figures 3a and 3b)

Each power supply consists of an ac to dc rectifying circuit that drives an inverter operating at approximately 10 KHz. Output from the inverter provides ac power to three functionally-independent regulated dc output sources. Type 2002001206 delivers +5 volts at 50 amperes and -15 volts at 5 amperes. Type 2002001251 delivers +15 volts at 25 amperes. Each series-regulator type output circuit is composed of a pass-transistor stage and a section containing output-voltage monitoring, and a reference and feedback amplifier connected in a closed loop arrangement so that regulated output voltages are maintained over a specified load-current range. Each output is adjustable by a screwdriver control.

Each of the three output circuits has overload/short-circuit current protection in the form of fold-back limiting whereby, during an overload, load current is reduced to a small fraction of its maximum value. In addition, each output circuit contains overvoltage protection circuitry that activates a thyristor (SCR), when energized. When the SCR is activated, an internally-used reference voltage is removed, and with it, the base drive to the transistor inverter stage. Both power supplies are shut down as a result, because they track each other through gating.

Input voltage is stepped down via an auxiliary transformer in each supply operating at 50/60 Hz line frequency. The stepped-down voltage is supplied after rectification to a coarse-regulated, fixed-output, voltage-type series regulator that produces an internally-used reference voltage.

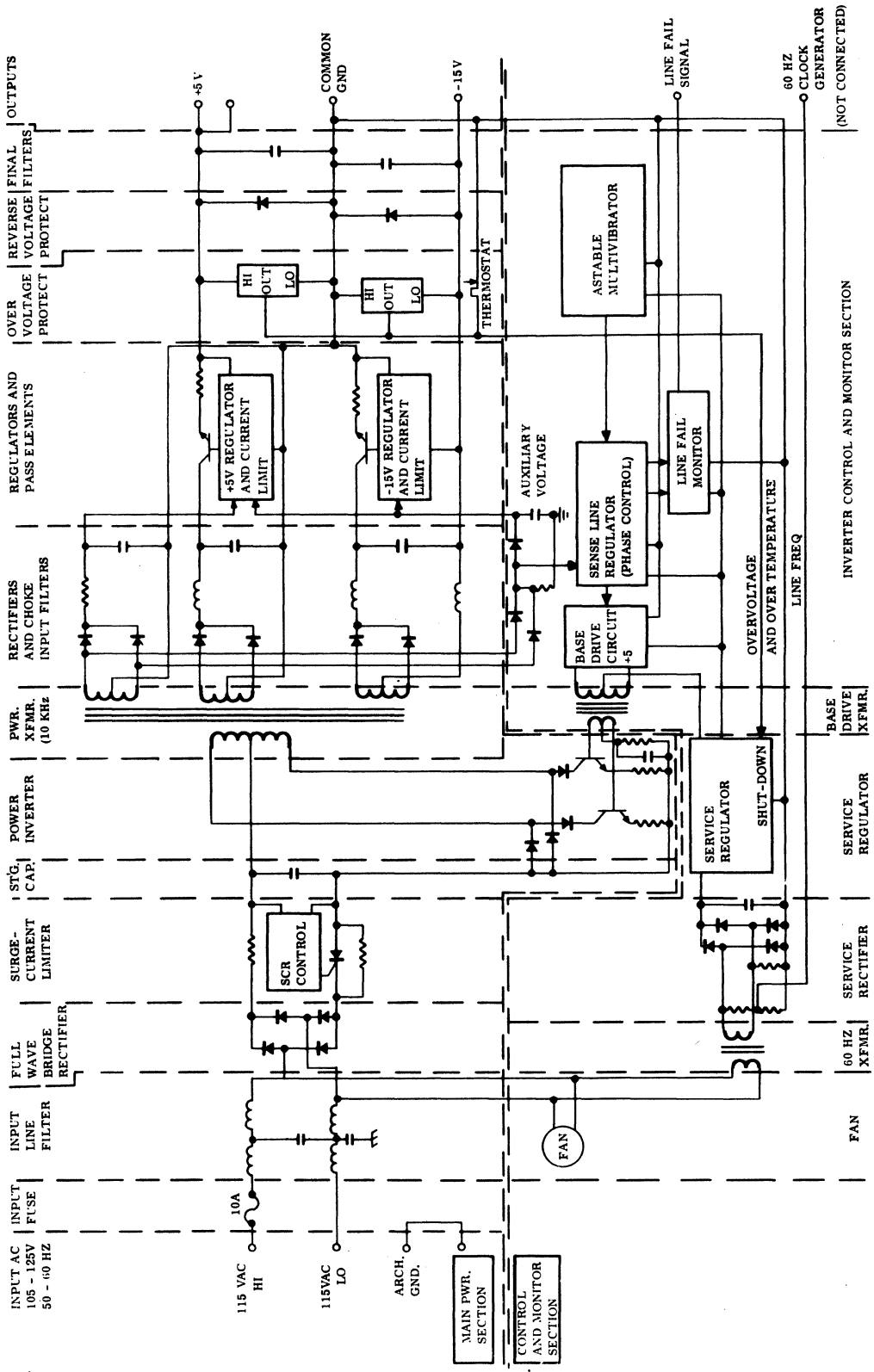

Figure 3a. Power Supply 2002001206 Functional Block Diagram

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Inverter-transformer outputs are line-regulated. Line regulation is accomplished by controlling the base-drive current of the inverter transistors, e.g., an increase in line voltage results in these transistors conducting for a shorter length-of-time. Control circuitry to drive the inverter stage consists of multivibrator, line-voltage sensing, flip-flop, and inverter base-drive circuits. Integrated circuits and discrete components are used to perform the various functions.

A thermostat in the power supply serves a dual purpose:

1. Operating ambient temperature is monitored continuously. When excessive temperatures occur, both power supplies are shut down.

2. Case temperature of most pass transistors (being critical items) is also monitored continuously. Thus, the thermostat protects power supply circuits and also protects system operation during any component malfunction.

Reverse diodes across each series regulator output prevent polarity reversal from exceeding approximately two volts.

Line failure logic pulses (PWST) and a line frequency signal (LFRQ) are generated for use by the SUE Bus Control Unit (BCU). PWST pulses provide early warning signals for the BCU if line voltage drops below a threshold level. PWST signals cause a priority interrupt to the highest program level so that a data protection sequence can be performed before dc power fails. Circuitry for signal LFRQ provides pulses at the ac line frequency as required by the user.

DETAILED CIRCUIT DESCRIPTION

Detailed descriptions of major power supply circuits are contained in the following subparagraphs. Partial circuit illustrations are provided. Where circuits are functionally identical, only one illustration is shown.

INPUT LINE FILTER. - A symmetrical T-type filter reduces voltage spikes and noise signals generated in the power supply during the switching process in the

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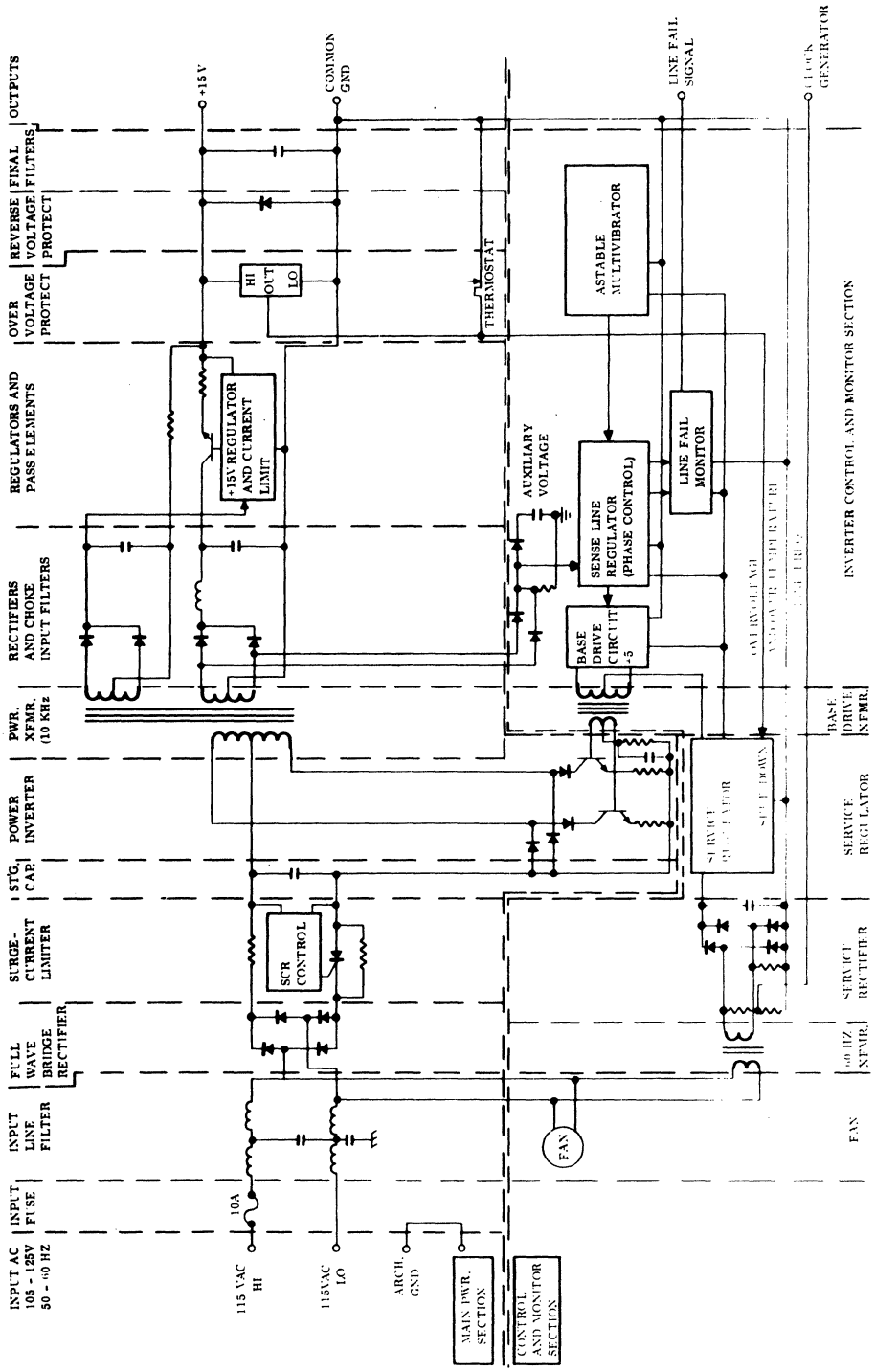

Figure 3b. Power Supply 2002001251 Functional Block Diagram

Power Inverter stage. These voltage spikes and noise signals are reduced to an acceptable level before entering the ac power lines.

FULL-WAVE BRIDGE RECTIFIER. - A conventional full-wave bridge rectifier converts 115-volt 60 Hz line power into an unregulated dc voltage which activates the power inverter.

SURGE-CURRENT LIMITER. - Power resistors R01 and R02 limit surge currents into the power supply ac input. To minimize power dissipation of resistor R02 during steady-state, a thyristor (SCR) is connected in parallel with this resistor. A resistor-capacitor type network forms a part of the thyristor gate circuit and retards firing of Q05 until the inrush current magnitude has reached a safe value. The input circuit preceding the power inverter stage is shown in Figure 4.

INDICATING LIGHT. - Light Emitting Diodes (LEDs) that illuminate when the supply is energized, can be observed through a hole in the panel on the front of each power supply. The LEDs no longer light when ac power is removed.

POWER INVERTER. - The power inverter is an oscillator operating in a quasi square-wave mode whereby the unregulated dc input voltage is converted into three ac voltages (Figures 5a and 5b). Square-wave generation is accomplished by transistor pairs Q01-Q02 and Q03-Q04 connected in parallel to accommodate input-current requirements under maximum load-current conditions. Emitter resistors R13 and R14 are equalizing resistors for these transistor pairs.

Switching action of the inverter transistors occurs in the following manner. Rectified and filtered line voltage is applied between the center tap of transformer T01 primary and the common node of resistors R13 and R14. When base current is supplied to one of the two transistor pairs, that particular pair is driven into saturation and the other pair to the cutoff state. When Q01-Q02 are driven into saturation, the voltage at A is approximately at ground potential (Figure 5). Since the voltage between A and B is the dc input voltage, the voltage

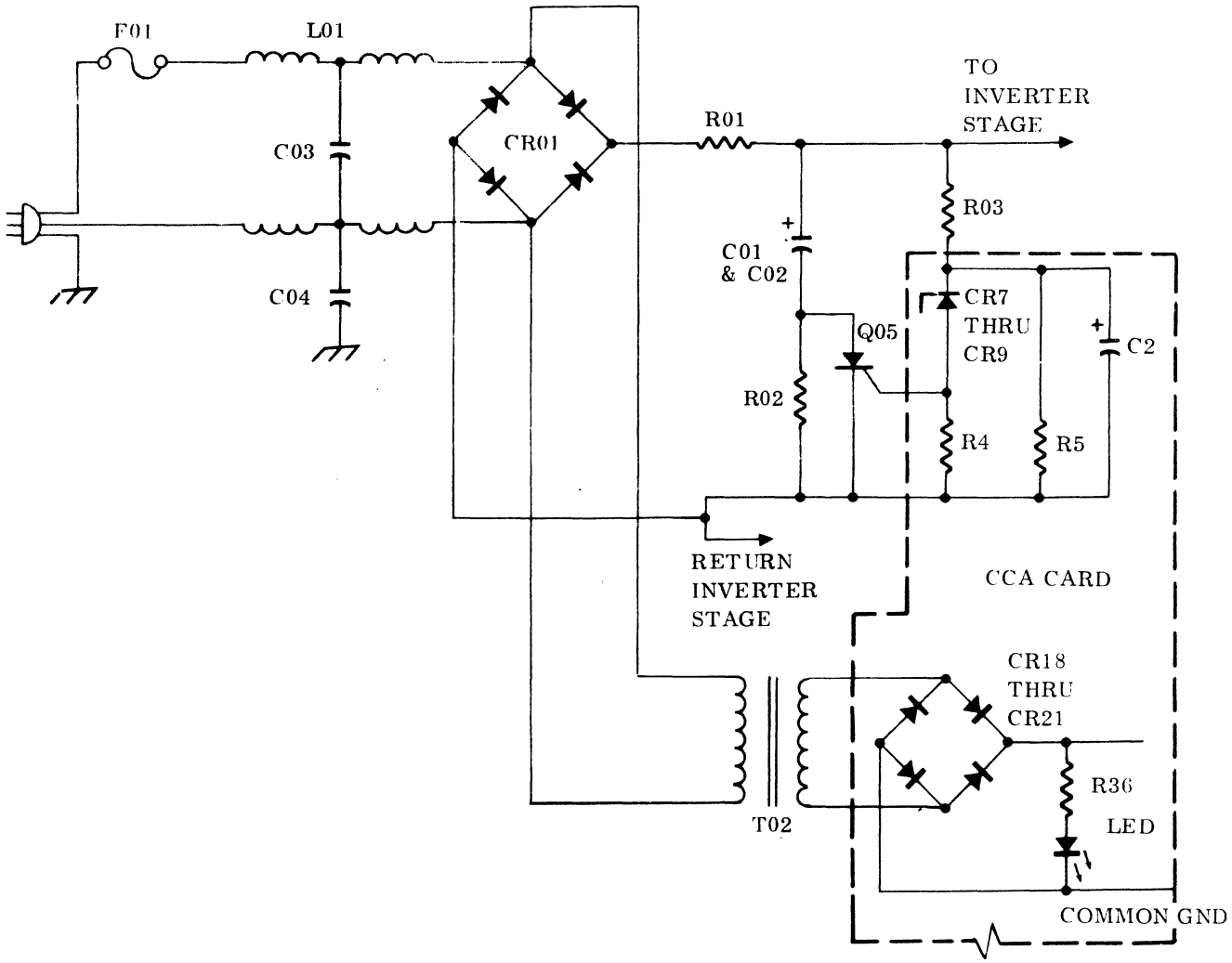

Figure 4. Power Supply Input Stage (Preceding Power Inverter)

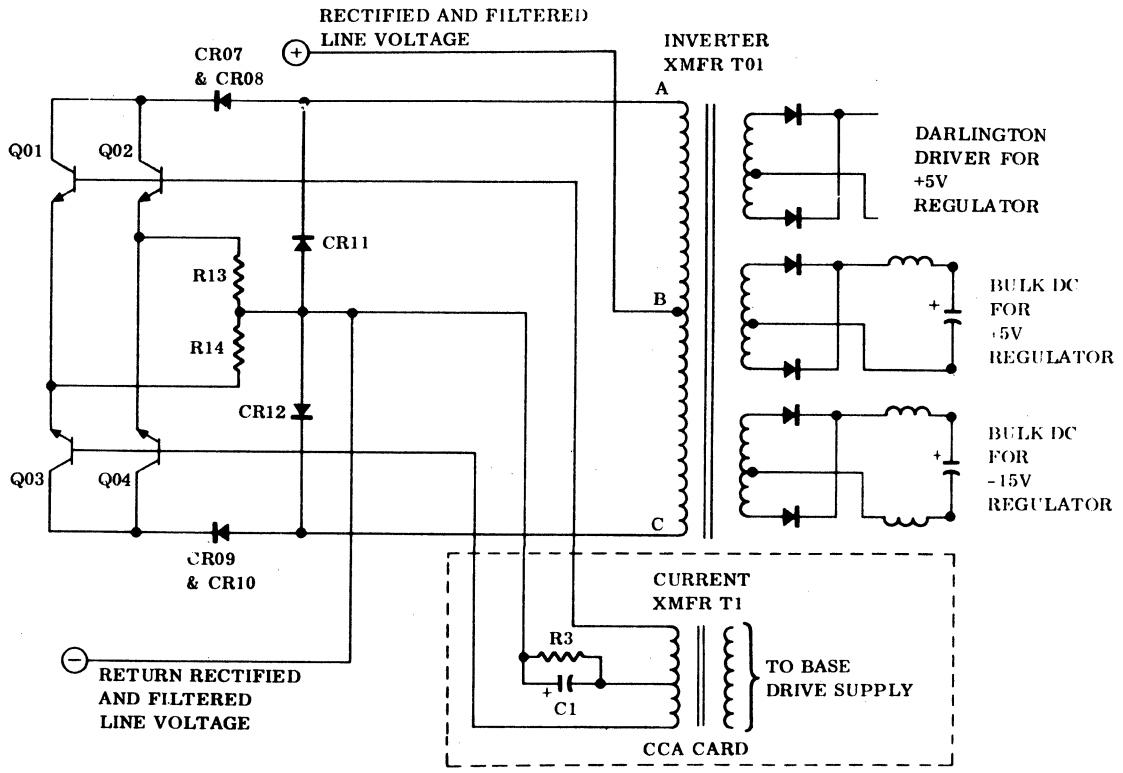

Figure 5a. Power Inverter Circuit, +5, -15V Supply

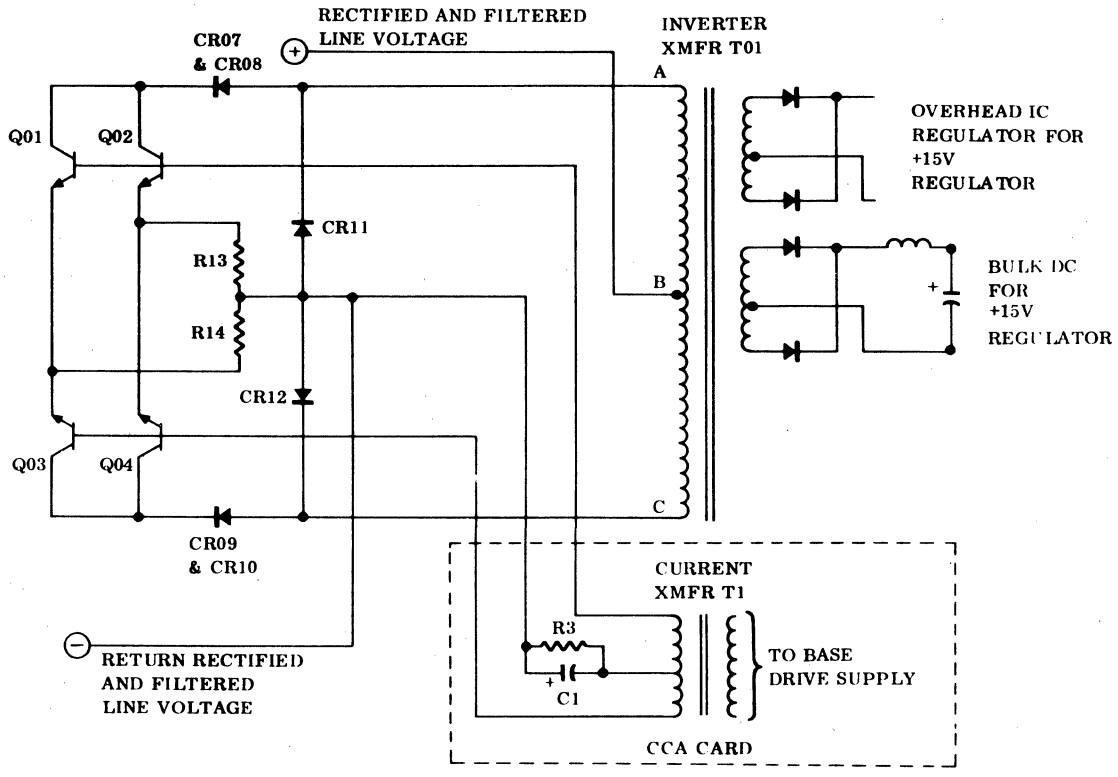

Figure 5b. Power Inverter Circuit, +15V Supply

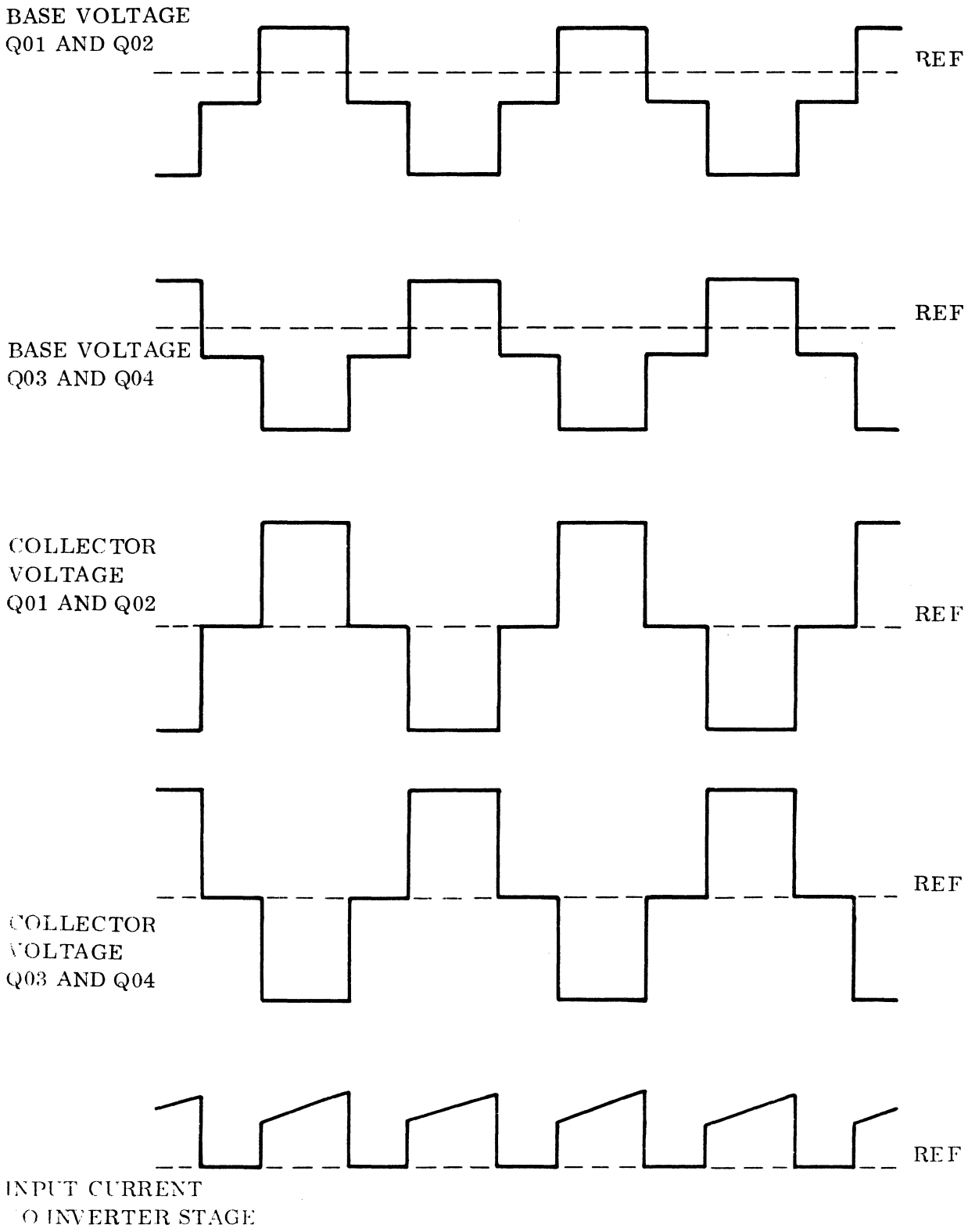

Figure 6. Power Inverter Timing

at C with respect to A is twice the input voltage because of autotransformer action of T01. A reverse voltage is applied across transistor pair Q03-Q04 as a result. While transistor pair Q01-Q02 conducts, input power is transferred from primary to secondary windings. Removal of base-drive current to Q01-Q02 causes both transistors to become cutoff and since temporarily base drive has not been supplied to transistor pair Q03-Q04, there is no transfer of input power from primary to secondary windings of transformer T01.

Various waveforms for the power inverter stage are shown in Figure 6. These waveforms indicate that at different time intervals, a similar action occurs when transistor pair Q03-Q04 receives base-drive current from current transformer T1 (on the CCA card), and consequently saturates. Again, input power is transferred from primary to secondary windings whereby transistor pair Q01-Q02 is held at cutoff. A slightly negative emitter-to-base voltage applied to any transistor pair in cutoff, assures no collector-current flow through that pair. This voltage is derived from the resistor-capacitor combination (R3-C1) in the base-drive circuit.

ASTABLE MULTIVIBRATOR. - Circuitry for the 20 KHz clock (50-microsecond cycle time) is shown in Figure 7. Selection of the R-C timing circuits is such that transistors Q4 and Q5 conduct successively for time intervals of 40 microseconds and 10 microseconds, respectively.

Operating voltage for this circuit is derived from an internally-used series regulator (transistor Q9 and associated zener diode CR22).

Astable multivibrator detailed operation can be explained by examining details occurring during any one cycle. For example, if action is stopped when Q5 is held conducting by current through R14, and Q4 is held non-conducting by a reverse bias voltage from C5, the waveforms at various points in the circuit are as shown at Reference Time A in Figure 8. Capacitors C4 and C5 charge to the voltage across them. Different values for C4 and C5 cause non-equal time intervals during which these capacitors are charged or discharged. For correct

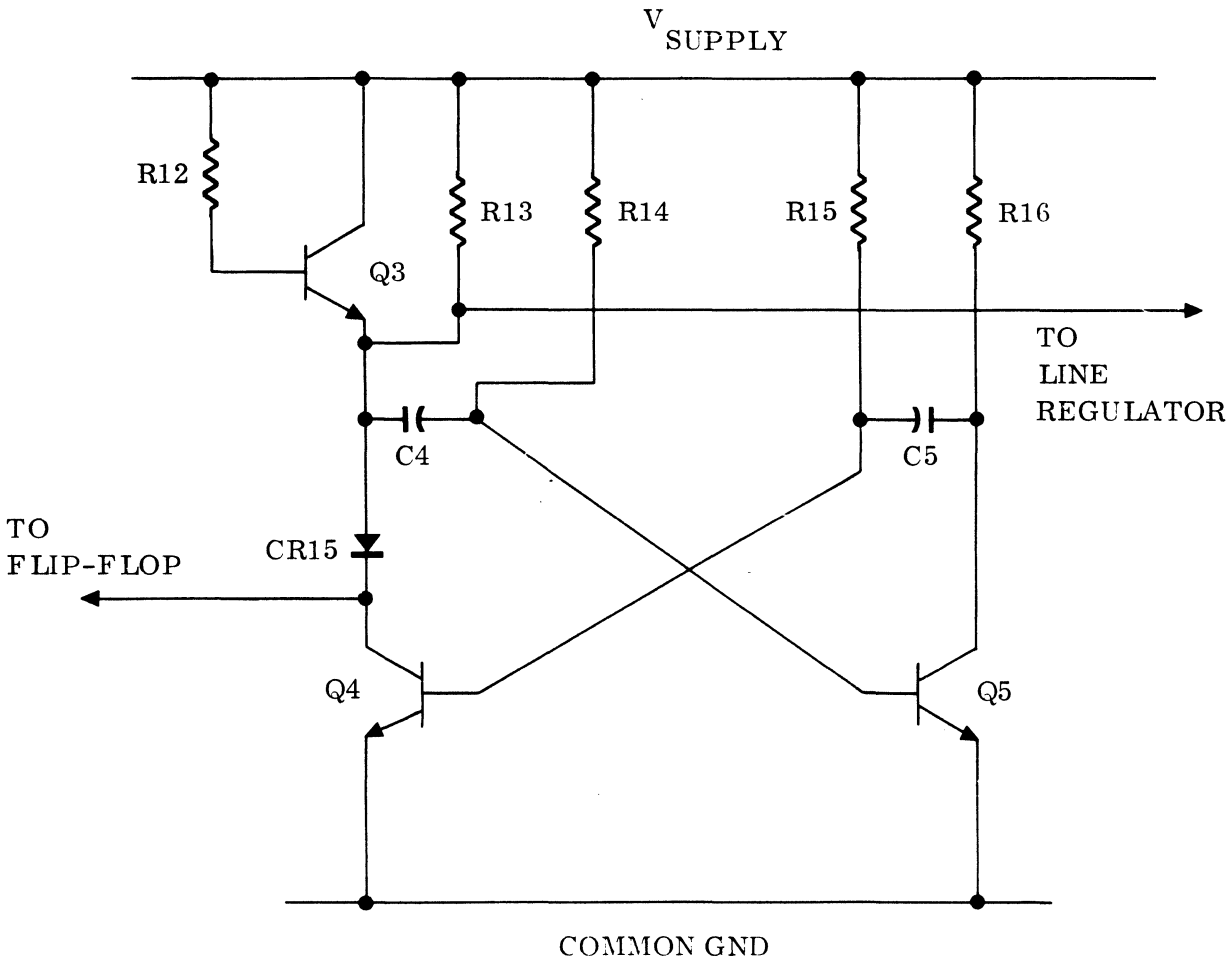

Figure 7. Astable Multivibrator (20 KHz Clock) Circuit

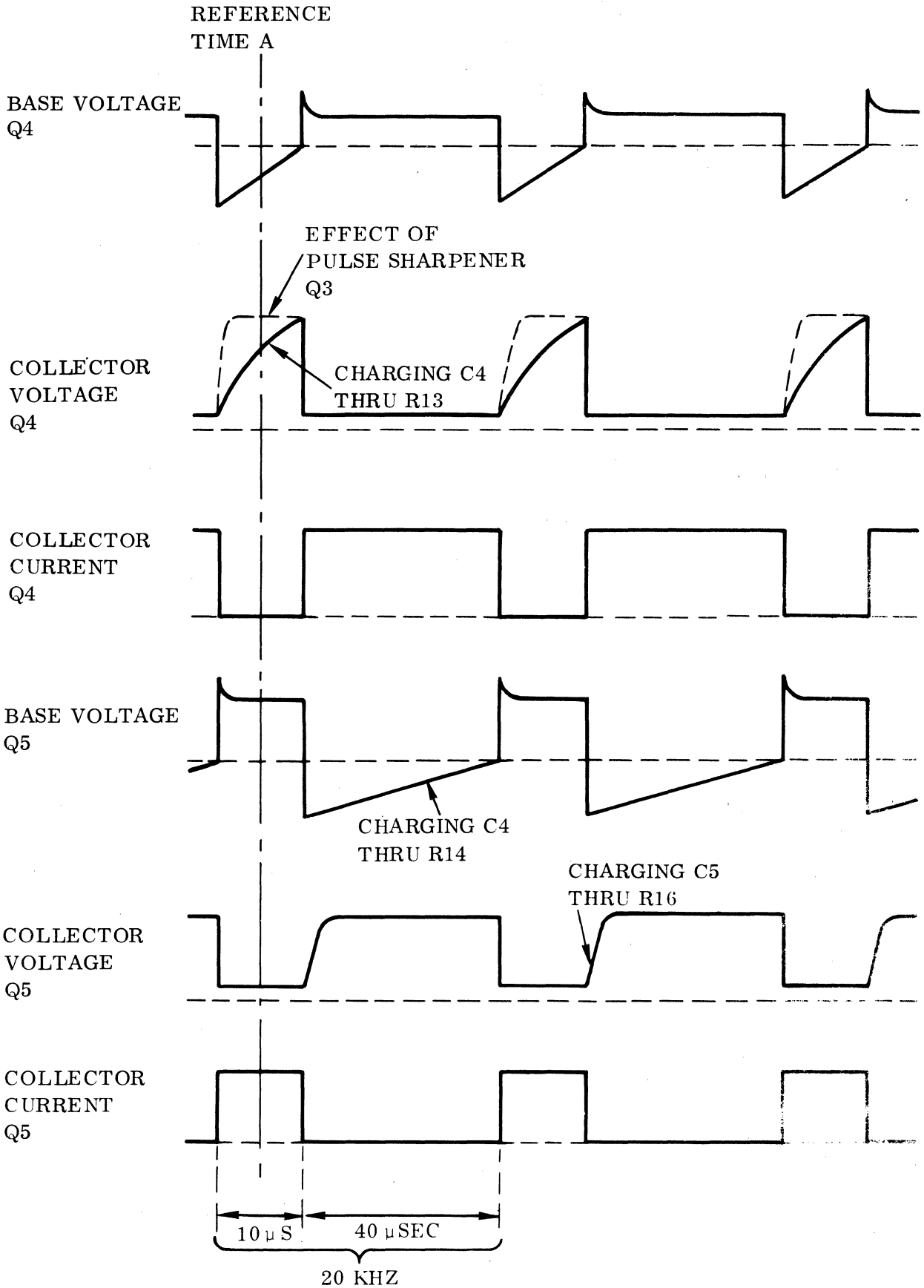

Figure 8. Astable Multivibrator Idealized Waveforms

operation, capacitor C4 must be fully charged before any change of state occurs. C4 charges through the parallel resistance of R13 and Q3. A voltage of $V_{Q3_E} - V_{Q5_E}$ is developed across C4. During this time, capacitor C5 also charges to a voltage of $V_{REF} - V_{CE_{Q5\,SAT}}$. As soon as C5 charges sufficiently to forward-bias Q4, Q4 starts conducting and thereby brings the Q4 collector voltage down. This voltage drop is coupled through C4 to Q5 and begins to stop conduction of Q5. Consequently, the collector voltage of Q5 rises, and the change is coupled through C5 to the base of Q4 aiding Q4 conduction. This process is regenerative and proceeds rapidly until Q4 conducts and Q5 is non-conducting. Initial conditions again exist but the states of both transistors have interchanged. Transistor Q3 has one function, to act as a pulse-sharpener for pulses generated at the collector of transistor Q4.

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LINE REGULATOR. - Figure 9 shows the line regulator circuit which basically consists of a differential amplifier. The base of transistor Q7 is held constant and the base of transistor Q8 is connected to a voltage divider network thereby sampling a portion of one of the secondary winding voltages of the power inverter transformer.

Operation of this circuit is such that for an increase in line voltage, (i.e., an increase in output voltage of the power inverter transformer), transistor Q8 drive voltage decreases while the collector current of Q7 increases. This condition alters the time constant of the R17-C6 combination and thus the rate of rise in voltage at the base of Q6. This result is demonstrated in Figure 10 where reference time A is shifted so that a steeper slope occurs, i.e., the forward biasing of transistor Q6 base occurs at an earlier time.

FLIP-FLOP. - Signals from the astable multivibrator and from the line regulator are supplied to a J-K flip-flop (U3 in Figure 11) to generate complementary pulses that are coupled via driver stages U1 and U2 to current transformer T1. Figure 11 shows in detail the waveforms at various nodes. Mixing line regulator output signals and flip-flop output signals causes the generation of two complementary trains of pulses of variable pulse width but at a constant

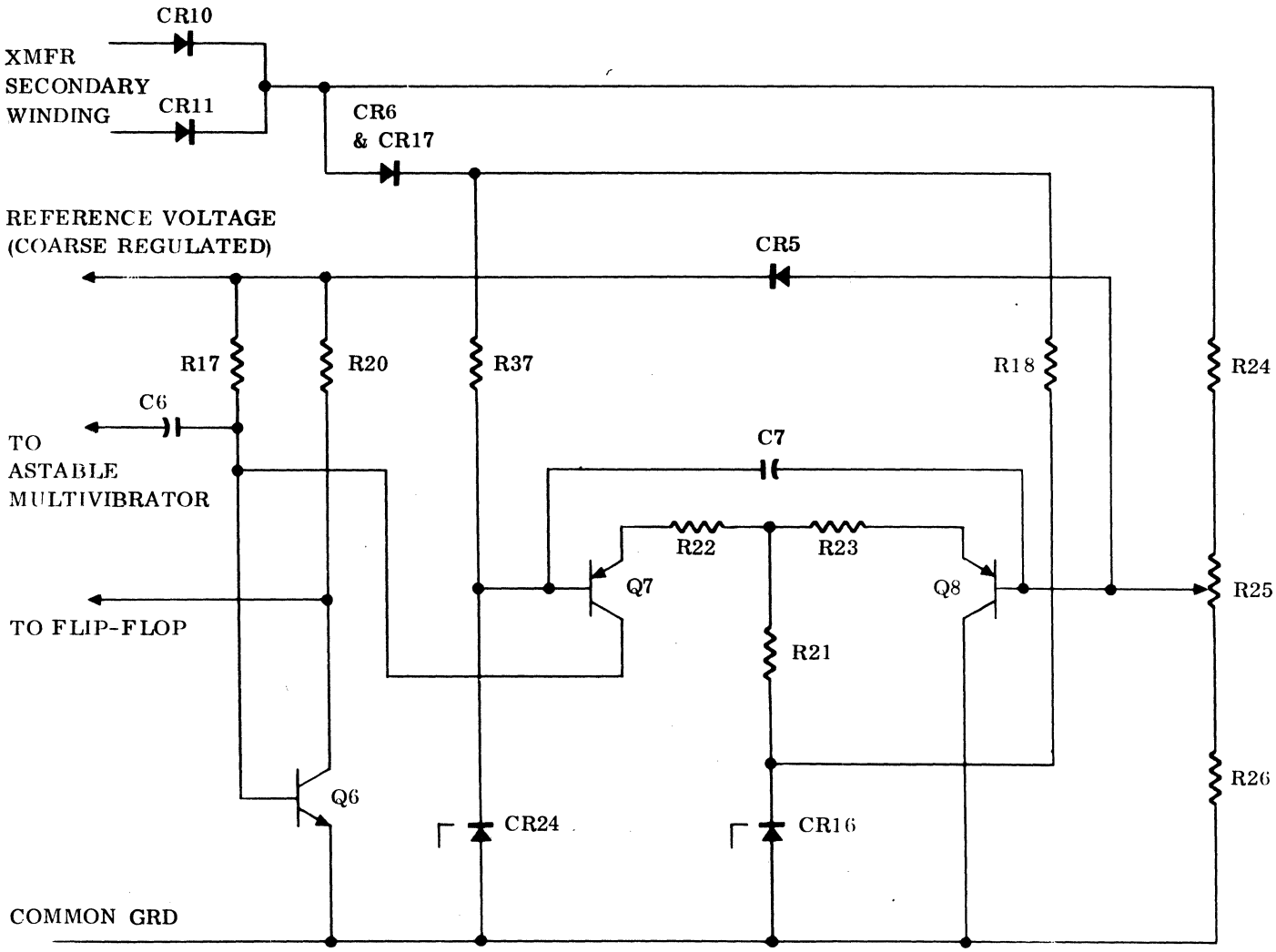

Figure 9. Line Regulator Circuit

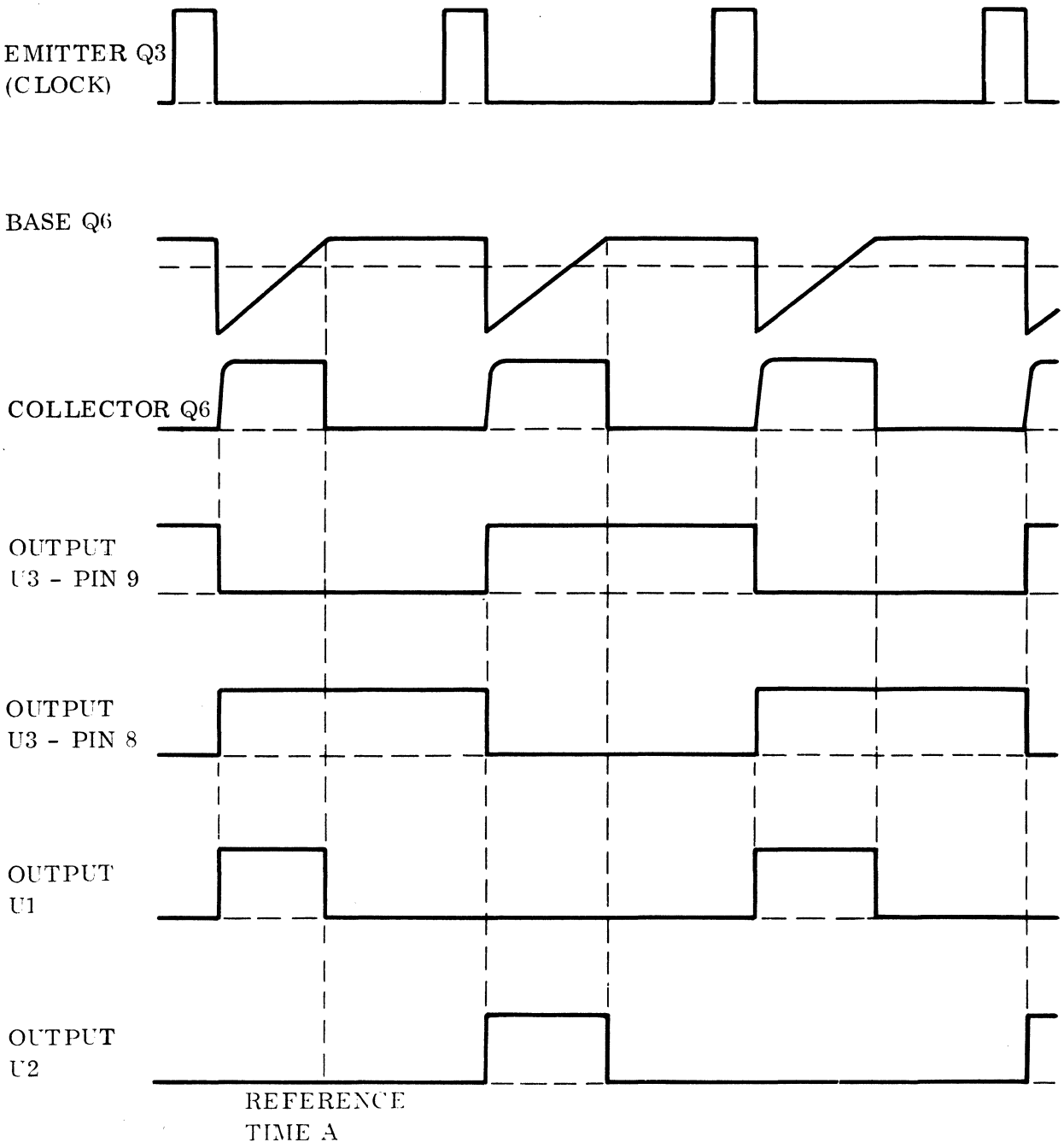

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Figure 10. Line Regulator Timing Diagram, Idealized

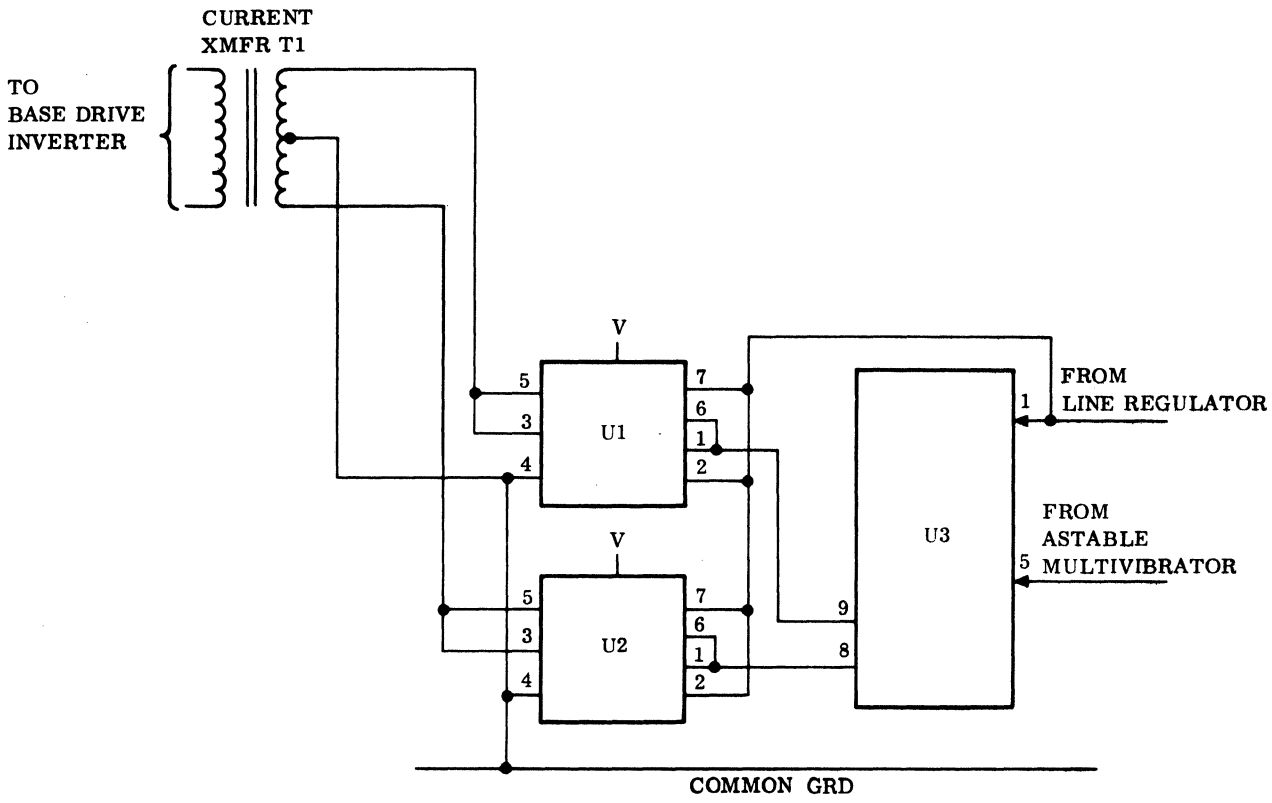

Figure 11. Power Inverter Drive Circuit

repetition rate. An increase in line voltage causes narrower complementary pulses to be supplied to the T1 current transformer.

SERVICE REGULATOR (INTERNALLY-USED REFERENCE VOLTAGE AND VOLTAGE-TO-CONSTANT-CURRENT CONVERTER). - Auxiliary transformer T02 steps down line voltage to furnish power, after rectification, to a coarse-regulated series regulator with fixed output (Figure 12). One of various functions of this reference voltage is to supply a bias voltage for a constant-current circuit supplying base-drive current (transistors Q1 and Q2 plus associated bias networks) via a center-tapped current transformer to the power inverter transistors. On-and-off timing of this constant current is controlled by driver stages U1 and U2.

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RECTIFIER AND INPUT CHOKE FILTER STAGES (TO THE OUTPUT REGULATORS). - Input power to each of the three regulator circuits is obtained from separate secondary windings of the power inverter transformer. These voltages are rectified, filtered, and are line-regulated, thereby reducing the number of pass transistors required in the series-regulator circuits.

REGULATORS AND PASS ELEMENTS (OUTPUT REGULATORS). - Each series regulator consists of a power amplifier stage (one or more pass transistors with their associated Darlington circuit) and a feedback loop (Figure 13). Except for voltage and current-handling capacity, all regulators are functionally identical. Where, to meet current requirements, more than one pass transistor is used, all are connected in parallel. In the feedback loop, part of the output voltage is compared with a stable reference voltage by a differential amplifier. Any difference in conduction detected by this comparator circuit, because of line and load variations, causes amplifiers to react and the pass transistor(s) to vary accordingly. This condition continues until the unbalanced input to the comparator stage is restored to the original balanced state. A combination of discrete components and an integrated circuit assures stable operation throughout a fairly wide temperature range.

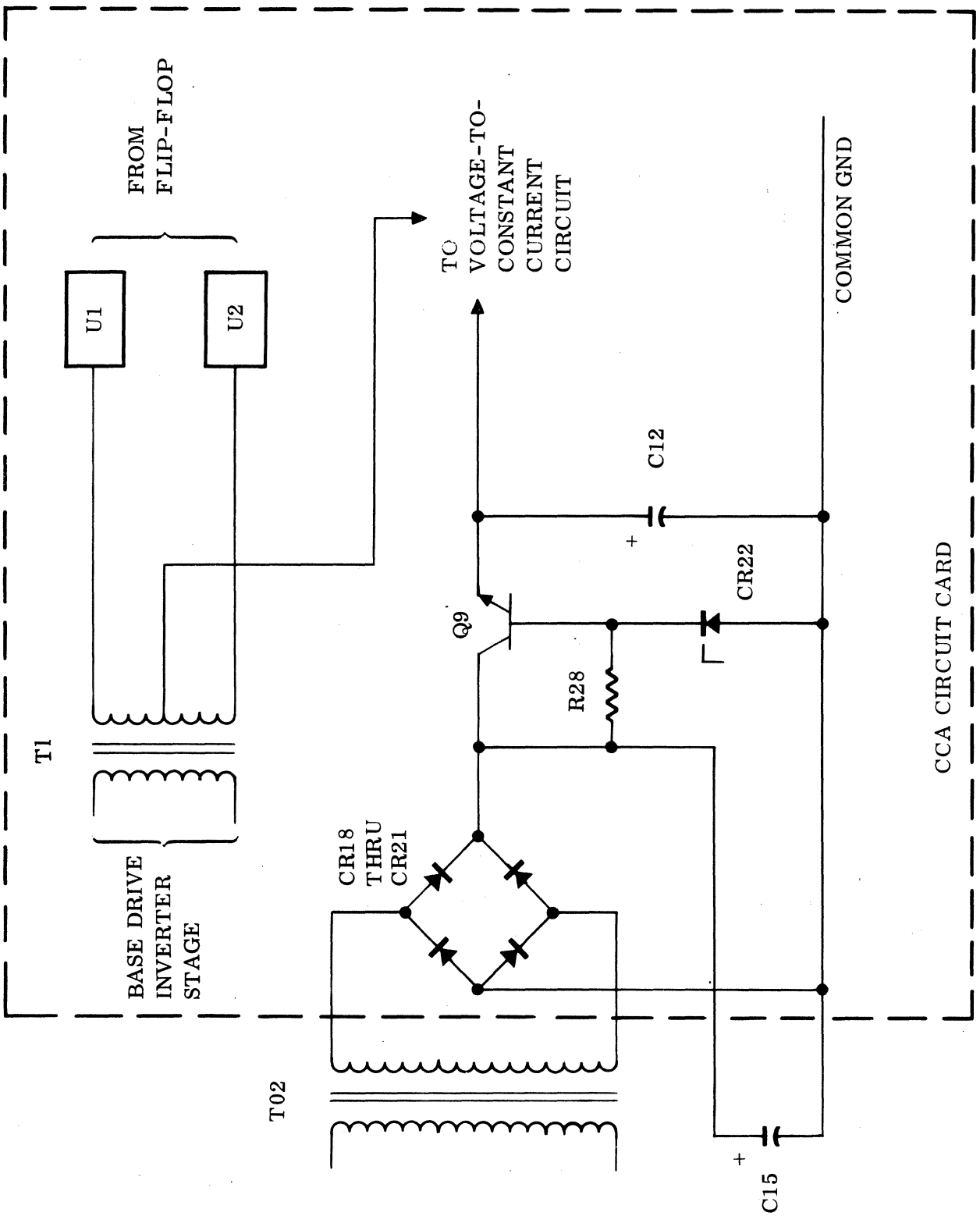

Figure 12. Service Regulator Circuit

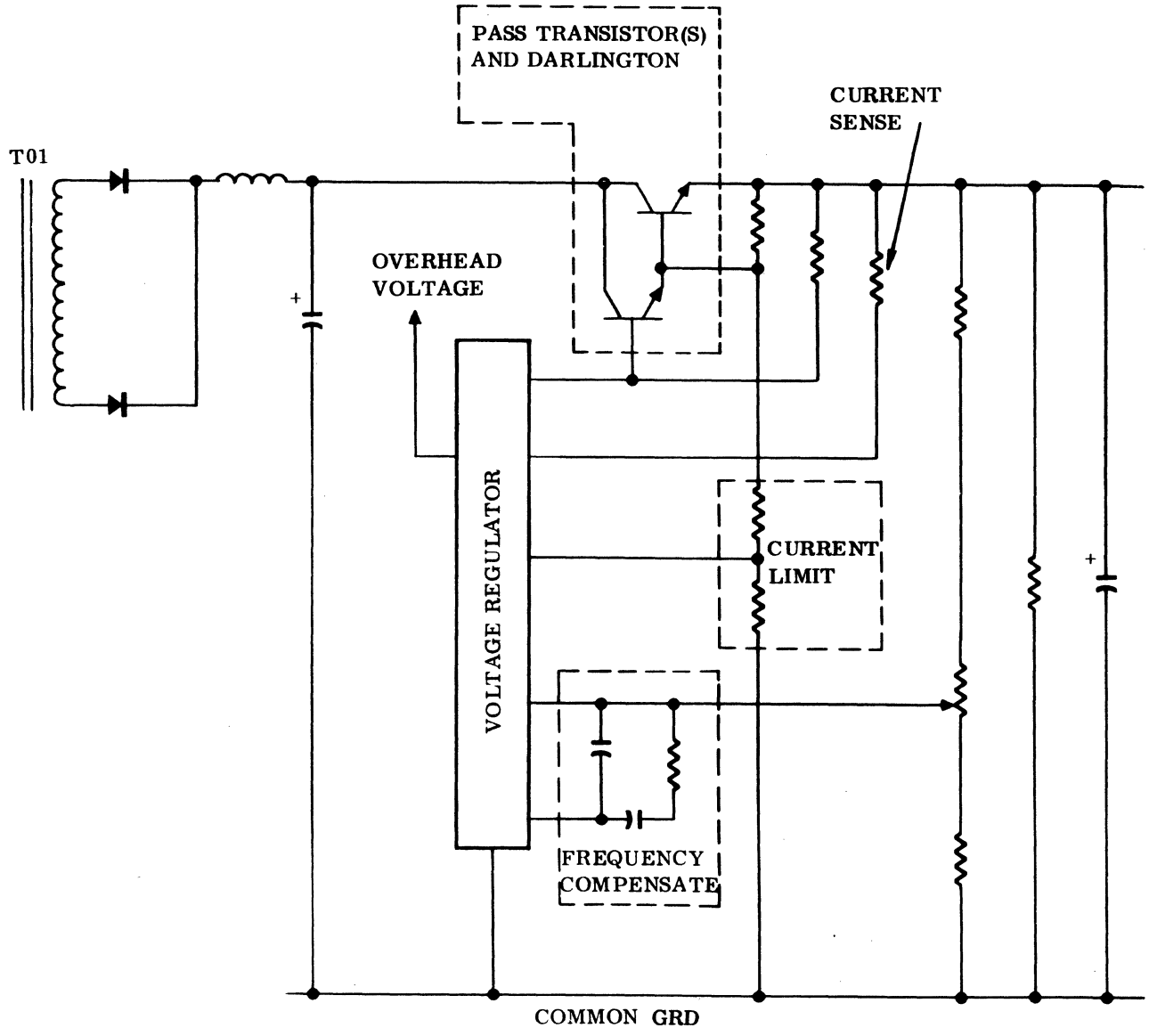

Figure 13. Regulator and Current Limiter Circuit (Typical)

OVERLOAD AND SHORT-CIRCUIT PROTECTION. - Overload and short-circuit protection for the output stage is an inherent feature built into the integrated circuit used in each series regulator. The protection is accomplished with foldback techniques. If the delivered load current exceeds a pre-set level, base current to the pass transistor stage is shunted away reducing base drive. This causes the output voltage to decrease with a simultaneous reduction in load current. See Figure 14 .

Excessive heat dissipation in the pass transistors is prevented by a thermostat. See Figure 15. When the thermostat contacts close, gate current is supplied to thyristor Q11 through transistor stage Q10. Firing of the thyristor causes the internally-used reference voltage to collapse which eliminates the base drive current supply to the inverter transistors. This action shuts down both power supplies because this sensing circuit is OR-gated in both supplies.

The -15 volt dc pass transistor in power supply 2002001206 is provided with an adequate heat sink because it is mounted on the chassis. Therefore, additional protection against excessive heat dissipation in this pass transistor is not required.

OVERVOLTAGE PROTECTION. - Overvoltage protection at the output of each series regulator consists of a simple threshold voltage detector made up of one or more (output voltage sensing) zener diodes and an amplifier. See Figure 15. Excessive output voltage activates this circuit and fires thyristor Q11, thereby shutting down their power conditioning system.

LINE FAIL DETECTION. - Line-failure detection circuitry provides a series of positive pulses to the bus controller unit when line voltage becomes less than the threshold level (Figure 16). Input signals to integrated-circuit flip-flop U3 and signals from the succeeding U4 output-driver stage are illustrated in Figure 16. Continued decrease in the line voltage causes collapse of all voltages in the power supply and, consequently, of this line fail signal. Any increase in line voltage above this threshold removes these line-fail pulses.

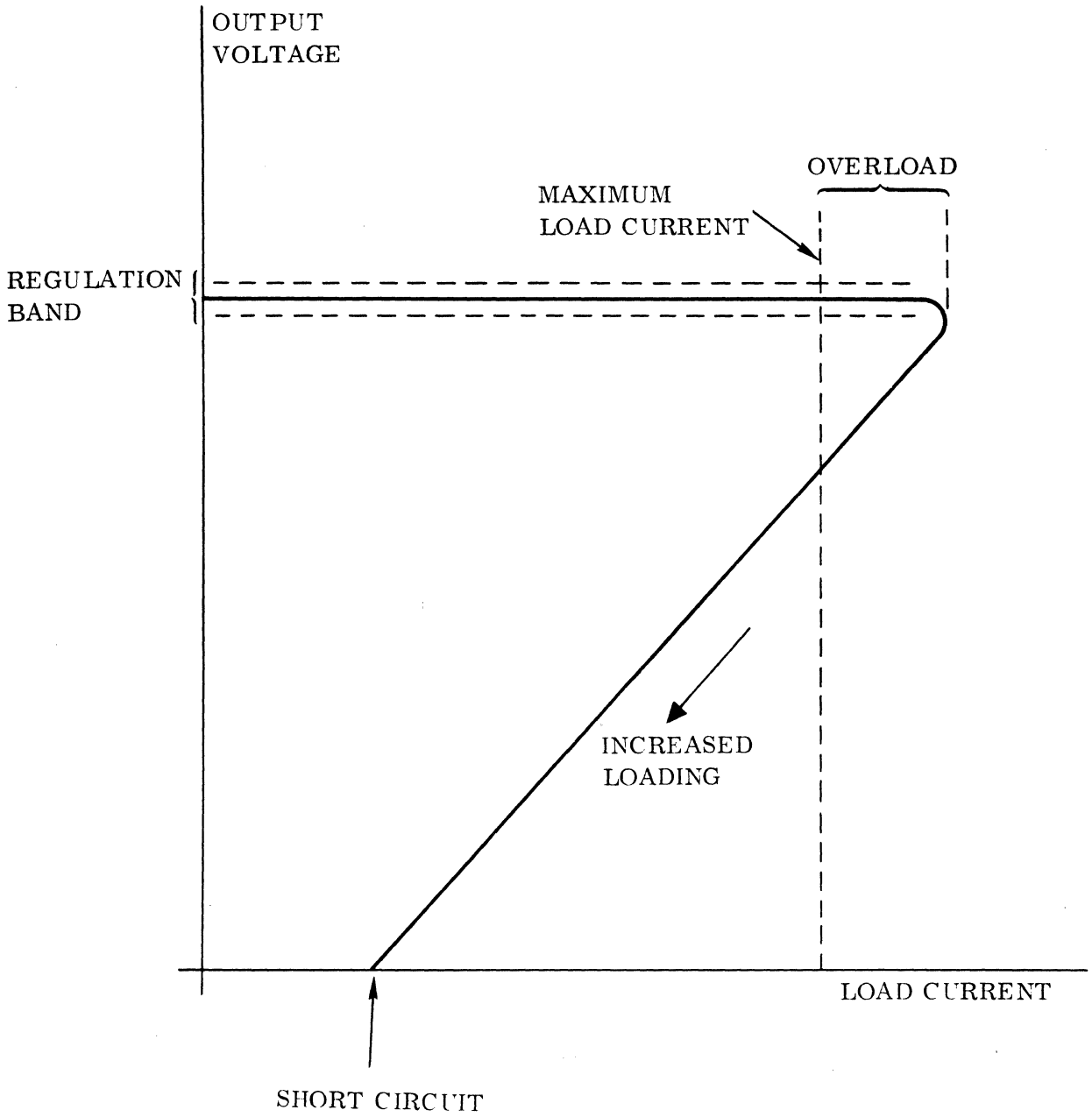

Figure 14. Overvoltage/Short-Circuit Regulator-Output-Current Plot

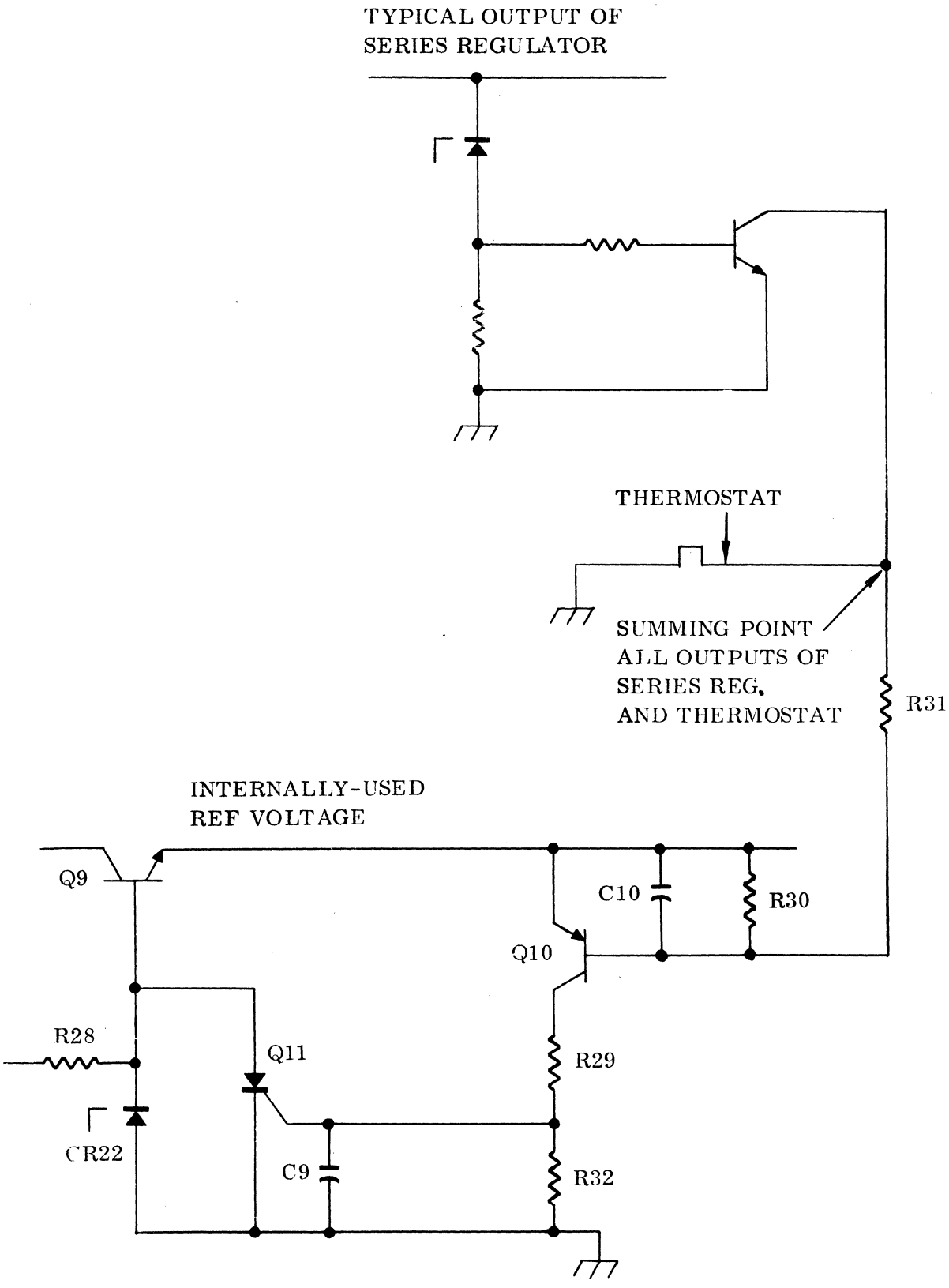

Figure 15. Overvoltage and Temperature Protection Circuit

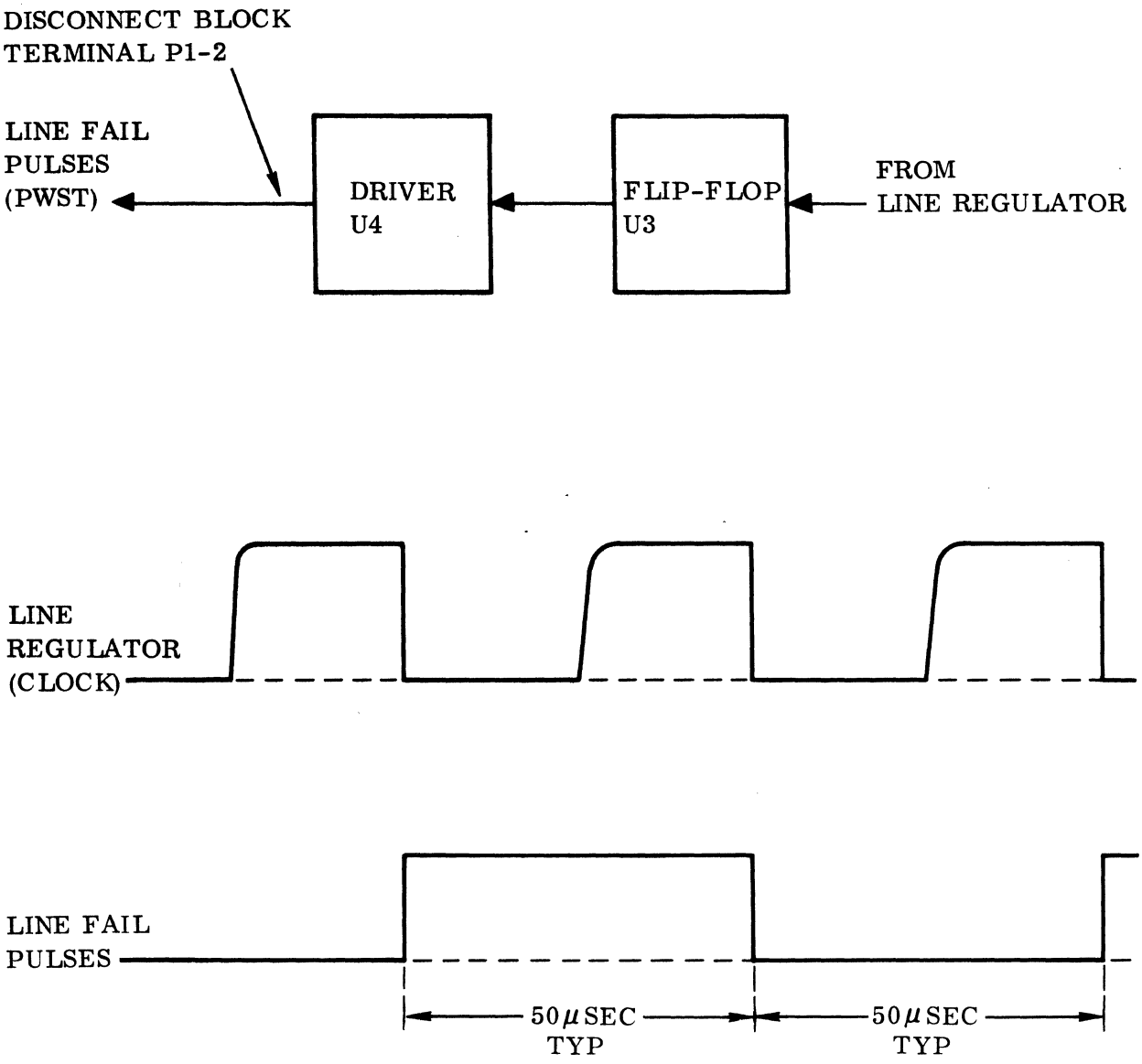

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Figure 16. Line-Failure Circuit Block Diagram and Signal Waveforms

LINE FREQUENCY SIGNAL. - The line-frequency signal circuit provides one positive pulse for each full cycle of the line voltage. This is accomplished by connecting a resistor network across part of the full-wave bridge at the output of auxiliary transformer T02. Figure 17 shows this circuit and the waveform of pulses obtained.

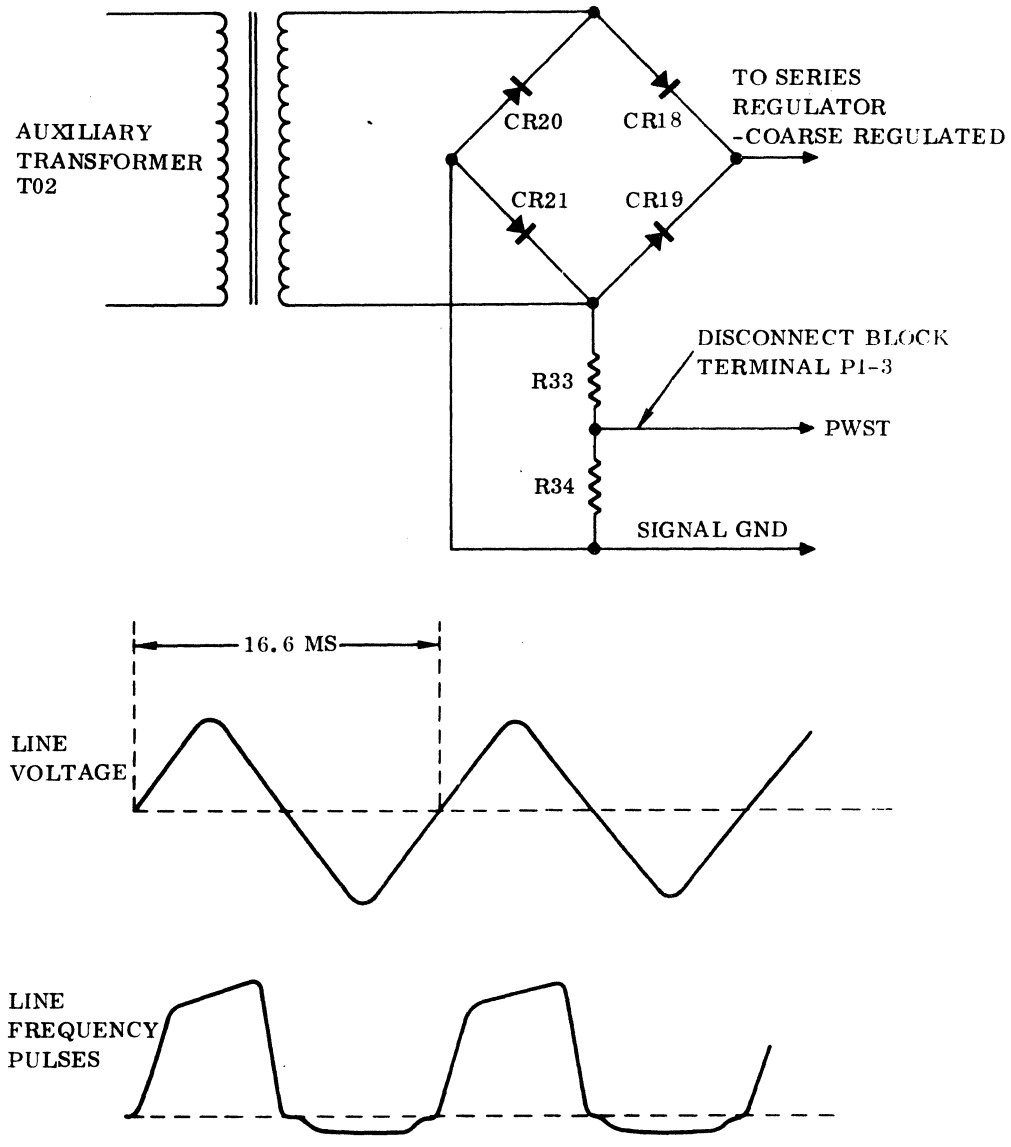

Figure 17. Line-Frequency Circuit and Signal

MAINTENANCE

GENERAL

The SUE 5952 Power Supply is designed for unattended operation without routine preventive maintenance. Thus, paragraphs following contain only corrective maintenance information, i.e., calibration and testing, trouble analysis, and repair techniques.

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RECOMMENDED TEST EQUIPMENT. - Table 1 contains a list of test equipment recommended for power supply maintenance. Equivalent equipment can be used.

Table 1. Recommended Test Equipment

Equipment	Manufacturer	Model
DC Ammeter	Weston	50 amp 931
Multimeter	Simpson	270
Digital Voltmeter	Non-Linear Systems	LX-2
Variable Auto-Transformer	General Radio	W 20
Oscilloscope	Tektronix	545A
Preamplifier	Tektronix	CA
Variable Loads	Litton (Dynaload)	541900
Resistor, 1000 ohms, 1/4 W	—	—
Zener Diode Type 1N751A	—	—

CALIBRATION AND TESTING

NOTE

Calibration and testing of each power supply must be performed normally with the power supply disconnected. Thus, unless a substitute power supply is available, the computer system must be non-operational during calibration and testing.

OVERVOLTAGE THRESHOLD TEST. - Overvoltage threshold test must precede the output voltage adjustments. Refer to Table 2 and proceed as follows:

Step 1: Disconnect line cord from ac power.

Step 2: Connect digital voltmeter test leads to appropriate output terminals per Table 2.

Step 3: Verify that all outputs are unloaded.

Step 4: Connect line cord to ac power and turn the appropriate output voltage adjustment potentiometer, per Table 2, counterclockwise until the output voltage drops suddenly to a very low value and the power supply shuts down.

Table 2. SUE 5952 Overvoltage Threshold Check

Power Supply	Nominal Output Voltage	Test Points*	Overvoltage Threshold	Output Voltage Adjustment Potentiometer
2002001206	+ 5.00V	P1-4	+ 6.2 ± 0.4V	R215 (IRO)
2002001206	-15.00V	P1-8	-17.5 ± 0.7V	R310 (IRO)
2002001251	+15.00V	P1-1	+17.5 ± 0.7V	R111 (IRO)

*NOTE: Connect voltmeter return to P1-6 (common ground).

Step 5: Turn the output voltage adjustment potentiometer several turns clockwise.

Step 6: Disconnect and reconnect the line cord from/to the ac power.

Step 7: Set output voltage to nominal value with output voltage adjustment potentiometer.

Step 8: Repeat steps 4 through 7 to check each overvoltage detection circuit.

OUTPUT VOLTAGE ADJUSTMENT TO NOMINAL. - Output voltages can be adjusted under no-load conditions. Proceed as follows:

Step 1: Connect digital voltmeter test leads to the appropriate output terminals per Table 3.

Step 2: Connect line cord to ac power.

Step 3: Verify that each output voltage is per Table 3; adjust appropriate potentiometer to obtain nominal output setting as required.

NOTE

In this procedure, do not exceed threshold overvoltage. If regulator output decreases suddenly during this adjustment because of an overvoltage condition, disconnect power supply from ac power, turn applicable potentiometer slightly clockwise and attempt readjustment.

CURRENT LIMITER TEST. - Proceed as follows:

Step 1: Disconnect line cord from ac power.

Step 2: Connect digital voltmeter test leads to appropriate output terminals per Table 4.

Table 3. SUE 5952 Output Voltage Adjustment to Nominal

Power Supply	Nominal Output Voltage	Test Points*	Acceptable Output Voltage	Output Voltage Adjustment Potentiometer
2002001206	+ 5.00V	P1-4	+ 4.95 to + 5.05V	R215 (IRO)
2002001206	-15.00V	P1-8	-14.85 to -15.15V	R310 (IRO)
2002001251	+15.00V	P1-1	+14.85 to +15.15V	R111 (IRO)
*NOTE: Connect voltmeter return to P1-6 (common ground).				

Step 3: Connect variable loadbank to same terminals per Table 4. Set loadbank to obtain a current flow below rated output capacity for the particular regulator output under test so that less than maximum load current is drawn.

Step 4: Connect line cord to ac power.

Table 4. SUE 5952 Current-Limiter Check

Power Supply	Nominal Output Voltage	Voltage Test Point*	Acceptable Start of Current Limiting
2002001206	+ 5.0V	P1-4	62.0 ± 7.0 amperes with short-circuit current at 15.0 ± 4.0 amperes
2002001206	-15.0V	P1-8	6.0 ± 0.6 amperes with short-circuit current at 0.9 ± 0.4 amperes
2002001251	+15.0V	P1-1	35.0 ± 6.0 amperes with short-circuit current at 5.0 ± 2.0 amperes
*NOTE: Connect voltmeter return to P1-6 (common ground).			

Step 5: Increase the variable load until current limiting occurs per Table 4.

Step 6: Repeat all steps for all current limiters.

LINE FAIL PULSES TEST, POWER SUPPLY 2002001206. - Proceed as follows:

Step 1: Disconnect line cord from ac power.

Step 2: Connect one resistor, 1000 ohm, 1/4W, to terminals P1-2 and P1-4 of disconnect block P1. Connect oscilloscope to terminals P1-2 and P1-6 of disconnect block.

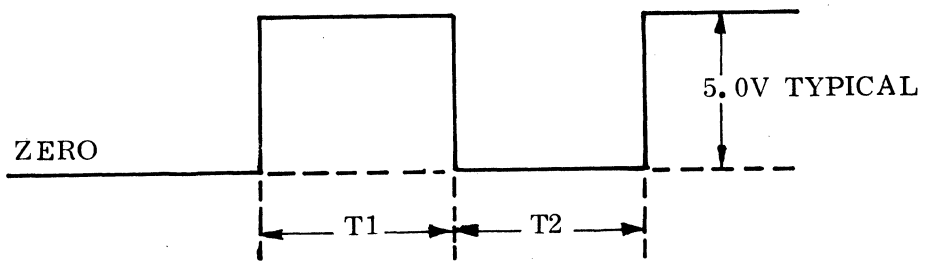
Step 3: Verify that all outputs of the power supply are unloaded.

Step 4: Connect power supply to variable autotransformer and variable autotransformer to ac power.

Step 5: Increase autotransformer voltage until nominal ac voltage is obtained.

Step 6: Sync oscilloscope by connecting TRIGGER INPUT to terminal marked TP 1 on CCA printed circuit card.

Step 7: Decrease power supply input voltage until a train of pulses is observed. Verify that these pulses appear when an input voltage of 72 ± 8 volts, 60 Hz occurs and disappear above this threshold level. Verify that these pulses have the following waveform:



T1 = T2 = 46 to 58 MICROSECONDS

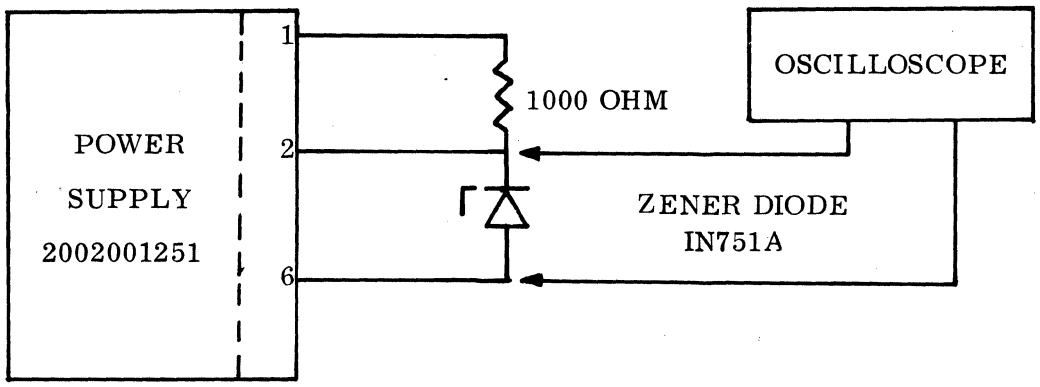
Alternate Method

If no variable autotransformer is available, this particular test can be accomplished by disconnecting the power supply line cord from ac power and observing the momentary oscilloscope display of the Line Fail pulses.

LINE FAIL PULSES TEST, POWER SUPPLY 2002001251. - Proceed as follows:

Step 1: Disconnect line cord from ac power.

Step 2: Connect one resistor, 1000 ohm, 1/4W, to terminals P1-1 and P1-2 of disconnect block P1; and connect one zener diode, type 1N751A between terminals P1-2 and P1-6 of disconnect block P1. Connect oscilloscope to terminals P1-2 and P1-6 of the disconnect block. See sketch.



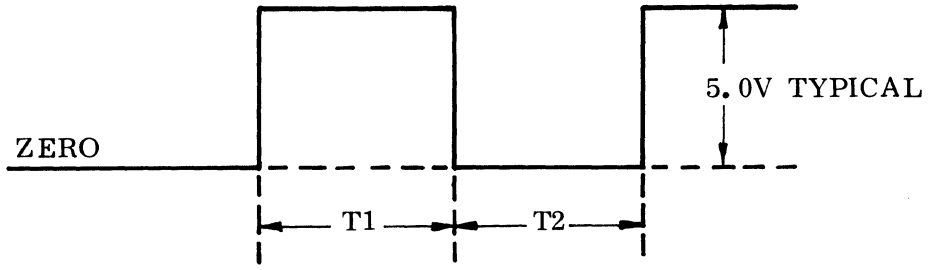
Step 3: Verify that all outputs of the power supply are unloaded.

Step 4: Connect the power supply to the variable autotransformer and connect the autotransformer to ac power. Increase the autotransformer voltage until nominal ac voltage is obtained.

Step 5: Sync oscilloscope by connecting TRIGGER INPUT to terminal marked TP 1 on CCA printed circuit card.

Step 6: Decrease power supply input voltage until a train of pulses is observed. These pulses appear when an input voltage of

72 ± 8 volts, 60 Hz and disappears above this threshold level. Verify that these pulses have the following waveform:



T1 = T2 = 46 to 58 MICROSECONDS

PS2

Alternate Method

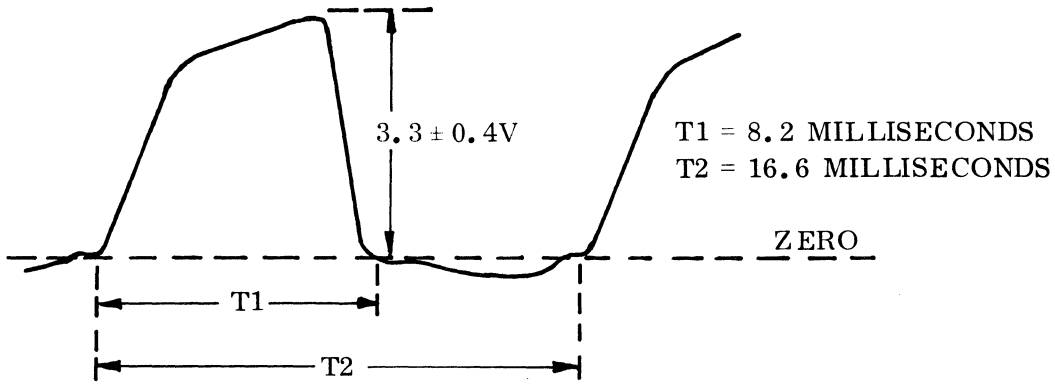
If no variable autotransformer is available, this particular test can be accomplished by disconnecting the power supply line cord from ac power and observing the momentary oscilloscope display of the Line Fail pulses.

LINE FREQUENCY SIGNAL TEST. - Proceed as follows:

Step 1: Connect line cord to ac power.

Step 2: Connect oscilloscope input leads to terminals P1-3 and P1-6 (common ground) of disconnect block P1.

Step 3: Verify that a train of pulses occurs at the specific time intervals indicated. The following waveform is typical for each of these pulses.



TROUBLE ANALYSIS

When a malfunction occurs, systematically examine the fuse, primary power lines, and external wiring before performing trouble analysis. Usually, power supply malfunctions can be traced to simple causes such as loose supply-load connections or accidental short circuit between lead connections on a terminal strip.

During detailed trouble analysis, refer to schematic diagrams SD2002001206 and SD2002001251. Typical malfunction symptoms are listed in Power Supply Trouble Analysis Guide, Table 5.

Table 5. Power Supply Trouble-Analysis Guide

Symptom	Possible Cause	Corrective Action
1. Power supply inoperative	No input power	Check for input power presence.
	Fuse F01 open	Check fuse and replace as required.
	Defective Power Inverter transistors (open)	Check and replace as required.
	Overvoltage protection SCR fired	Turn all output voltage-adjust potentiometers fully clockwise. Remove press-on terminal from pin 10 on CCA card. Find malfunctioning series regulator and isolate problem.
	Closed thermostat	Disconnect thermostat ground connection.
2. No output voltage from any regulator (0 volt)	Short circuit in any regulated power source	With ac power off, check for shorted or open power transistors. Check integrated circuit in feedback loop. Replace any out-of-tolerance semiconductor.

Table 5. Power Supply Trouble-Analysis Guide (continued)

Symptom	Possible Cause	Corrective Action
2. No output voltage from any regulator (0 volt) (continued)	Short in primary circuit with F01 fuse open	Shorted filter capacitor. Replace input filter capacitor and check input rectifier bridge assembly.
		Shorted rectifier assembly in transformer secondary. Replace shorted rectifier assembly (check filter capacitor charging voltage).
3. Very low voltage at output of any regulator (2 volts or less)	Shorted reverse-polarity protection diode	Disconnect ac power and check for short with ohmmeter. Replace when damaged. Check out all active components of the regulator.
4. Output voltage from any regulator is below regulation band.	Partial overload causing current limiting.	Remove partial overload.
	Associated regulator circuit defective.	Analyze malfunctions of associated regulator.
5. Output voltage from any regulator above regulation band.	Improper output voltage adjustment.	Re-calibrate output voltage.
	Associated regulator circuit (IRO) defective.	Analyze malfunctions of regulator.
6. Output voltage from a regulator cannot be adjusted.	Damaged output voltage adjustment potentiometer.	Replace damaged potentiometer.

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Table 5. Power Supply Trouble-Analysis Guide (continued)

Symptom	Possible Cause	Corrective Action
7. High ripple from any regulator output.	Output slightly overloaded and current limiter is beginning to function.	Check the current limiter setting per Table 4.
		Setting of input voltage levels of series regulator circuits too low. Increase by turning potentiometer R25 on CCA card.
8. LED does not light	Inoperative	Replace damaged LED.
9. Improper line fail pulses	CCA card circuit failure	Check out circuit thoroughly and correct the faults.
10. Improper line frequency signal	CCA circuit card failure.	Check out circuit thoroughly and correct the faults.

WARNING

DC VOLTAGES TO 300 VOLTS AND AC VOLTAGES TO 115 VOLTS ARE USED IN THE POWER SUPPLY. THESE VOLTAGES EXIST WITH HIGH CURRENT CAPABILITY AND ARE HAZARDOUS TO LIFE. BEFORE ATTEMPTING TO REMOVE OR REPLACE ANY POWER SUPPLY COMPONENT, DISCONNECT POWER SUPPLY FROM AC POWER SOURCE.

HEAT SINKS AND CHASSIS OPERATE AT FAIRLY HIGH TEMPERATURES, RETAINING HEAT FOR SOME TIME AFTER EQUIPMENT IS TURNED OFF. ALLOW AMPLE TIME FOR COOLING AFTER THE POWER IS OFF, BEFORE MAKING CONTACT WITH COMPONENTS.

REPAIR TECHNIQUES

The following techniques are recommended when making repairs.

a. When unsoldering components from a circuit board, never pry or force the part loose; unsolder the component by using the wicking process described below if no vacuum solder removal tool is available.

Step 1: Select a 3/16-inch tinned-copper braid for use as a wick. If braid is not available, select AWG No. 14 or No. 16 stranded wire with 1/2-inch of insulation removed.

Step 2: Dip the wick in liquid rosin flux.

Step 3: Place the wick onto the soldered connection and apply soldering iron to the wick.

Step 4: When sufficient amount of solder flows onto the wick and frees the component, simultaneously remove iron and wick.

b. Always use a heat sink when soldering transistors; a transistor pad with mounting feet is an effective heat sink. Pliers holding the lead being soldered also provide an excellent heat sink.

NOTE

Thermal compound should be applied when replacing some transistors and components. For a list of these components, refer to note 207 on sheet 10 of parts list PL2002001206 and PL2002001251 that follow in this bulletin.

c. Broken or damaged printed circuitry can be repaired by tinning a piece of uninsulated wire. Then, holding the wire in place along the damaged printed circuit, flow a little solder along the length of the wire.

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CHECKING SEMICONDUCTORS AND CAPACITORS. - Disconnect line cord from ac power source. Check any transistor with an in-circuit transistor checker. If no checker is available, transistors can be checked with an ohmmeter that has a highly-limited current capability. Observe proper polarity for PNP or NPN to avoid error in measurement. Forward transistor resistance is low but never zero; backward resistance is always higher than the forward resistance. Likewise, check forward and backward resistance of diodes with a multimeter.

Replacement of one part does not always eliminate the malfunction. For example, failure of one transistor can cause other transistors to fail. Replacing only one transistor and then reapplying power before checking for additional faulty components can cause damage to the replaced component.

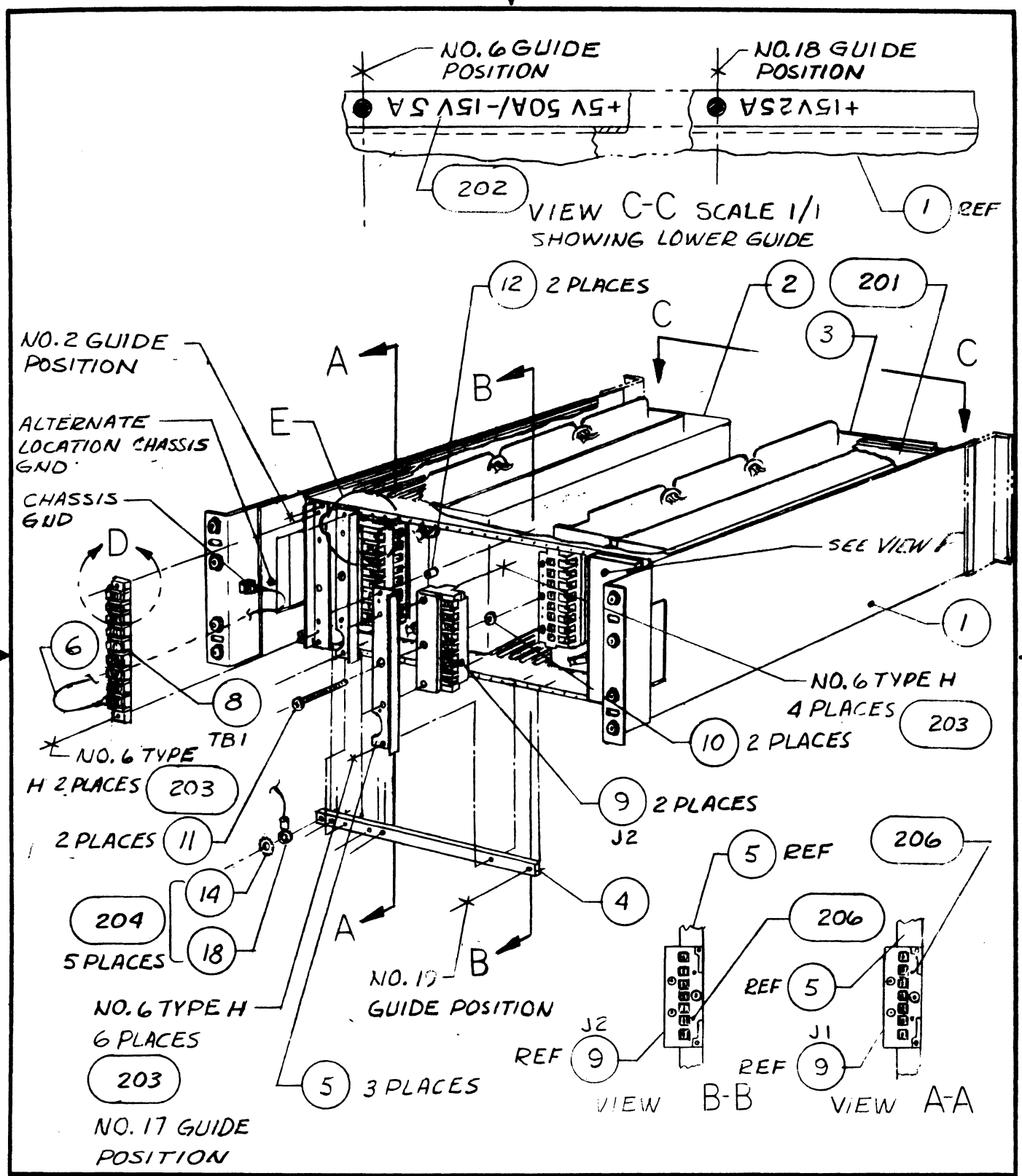
NOTE

Leakage resistance indicated by a simple resistance check of a capacitor is not always an indication of a faulty capacitor. In most instances the capacitors are shunted with resistances, some of which have low values. Only a complete short is a true indication of a shorted capacitor. A charge-discharge test is a valid method to check filter capacitors.

DRAWINGS AND PARTS LISTS

Following are the drawings and parts lists included in this bulletin.

Drawing or Parts List	Drawing Number	Sheets
Power Supply, 5952 Assembly	2003000447	2 thru 6
Power Supply, 5952 Parts List	PL2003000447-1	7, 8, 11
Power Contactor Assembly	2002001308	2, 3
Power Contactor Parts List	PL2002001308-1	4, 5
Power Supply, Dual Output +5V, -15V Schematic Diagram	SD2002001206	1
Power Supply, Dual Output, Assembly	2002001206	1
Power Supply, Dual Output, Parts List	PL2002001206-1	2 thru 5, 10
Power Supply, Single Output +15V Schematic Diagram	SD2002001251	1
Power Supply, Single Output, Assembly	2002001251	1
Power Supply, Single Output, Parts List	PL2002001251-1	2 thru 5, 10
Circuit Card Assembly, CCA	2001002156	1
Circuit Card Assembly, CCA Parts List	PL2001002156-1	2, 3, 6
Circuit Card Assembly, IRO	2001002157	1
Circuit Card Assembly, IRO Parts List +5V, -15V Supply	PL2001002157-2	4, 5
Circuit Card Assembly, IRO Parts List +15V Supply	PL2001002157-3	6, 7, 8
Assembly, Fan Pack 7921	2002001148-2	3
Assembly, Fan Pack, Parts List	PL2002001148-2	6



PS2

	SIZE	CODE IDENT NO.		REV
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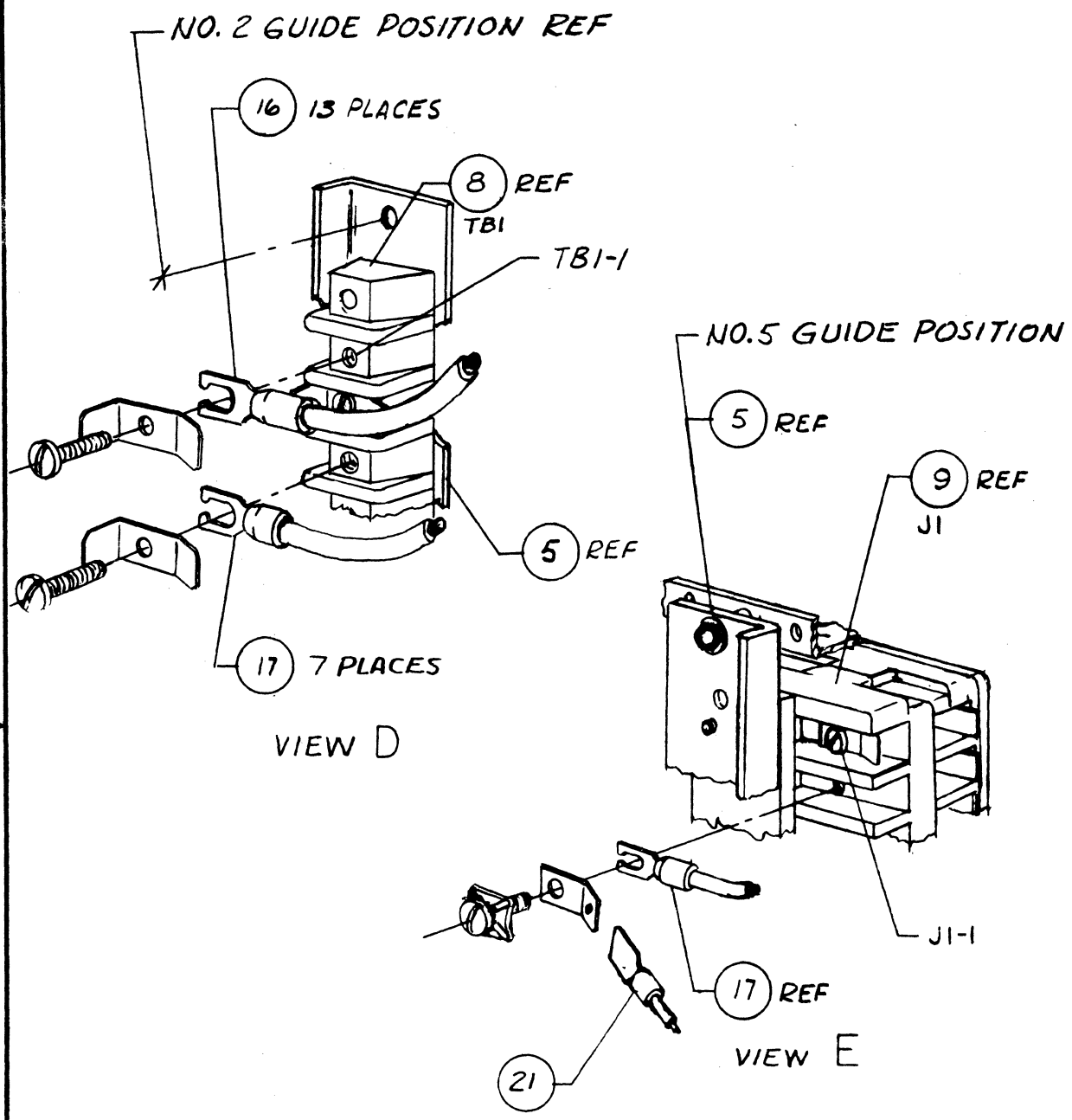
	SCALE —			SHEET 2



TYPICAL TERMINAL INSTALLATION DETAIL

	SIZE	CODE IDENT NO.		REV
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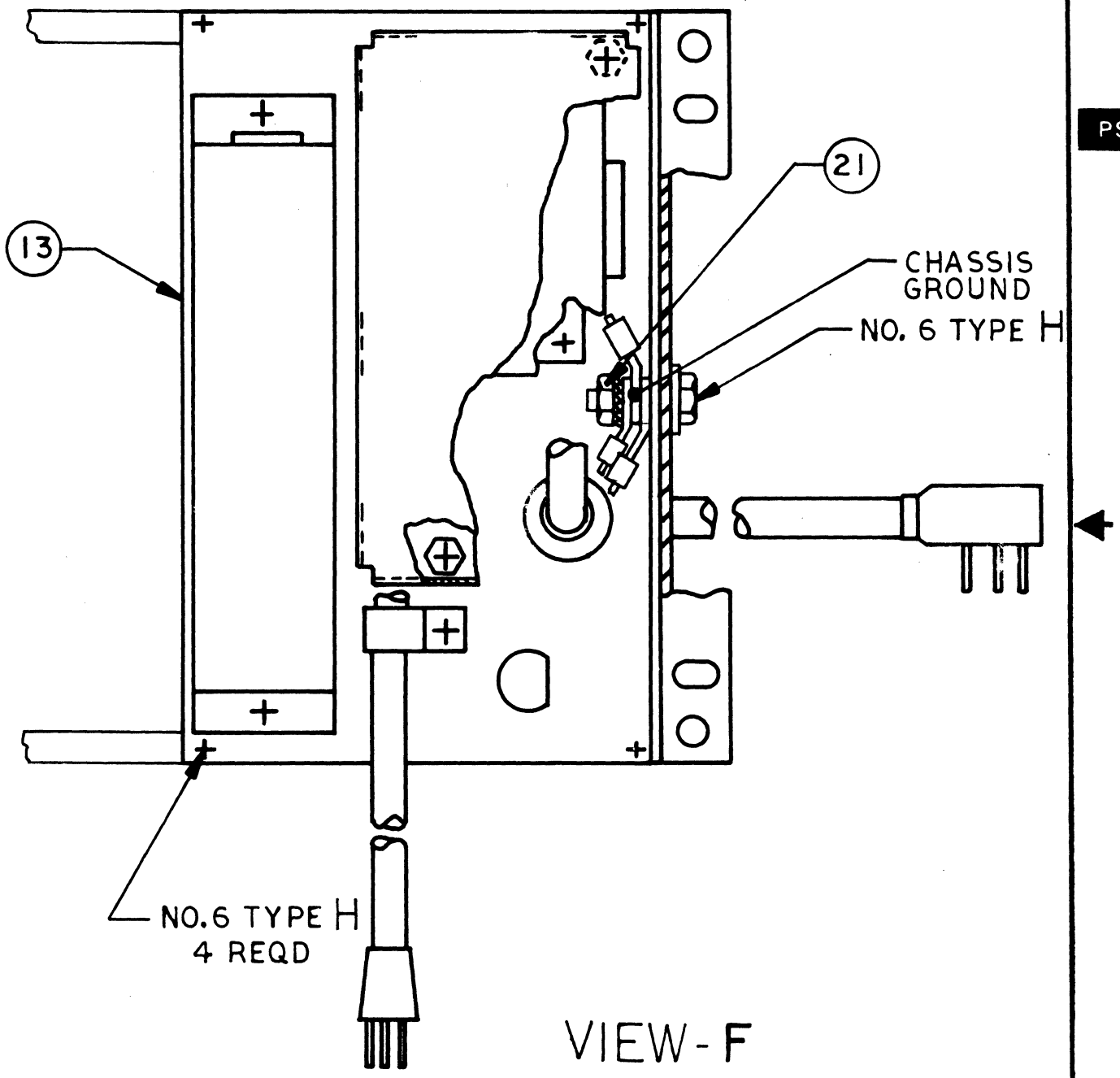
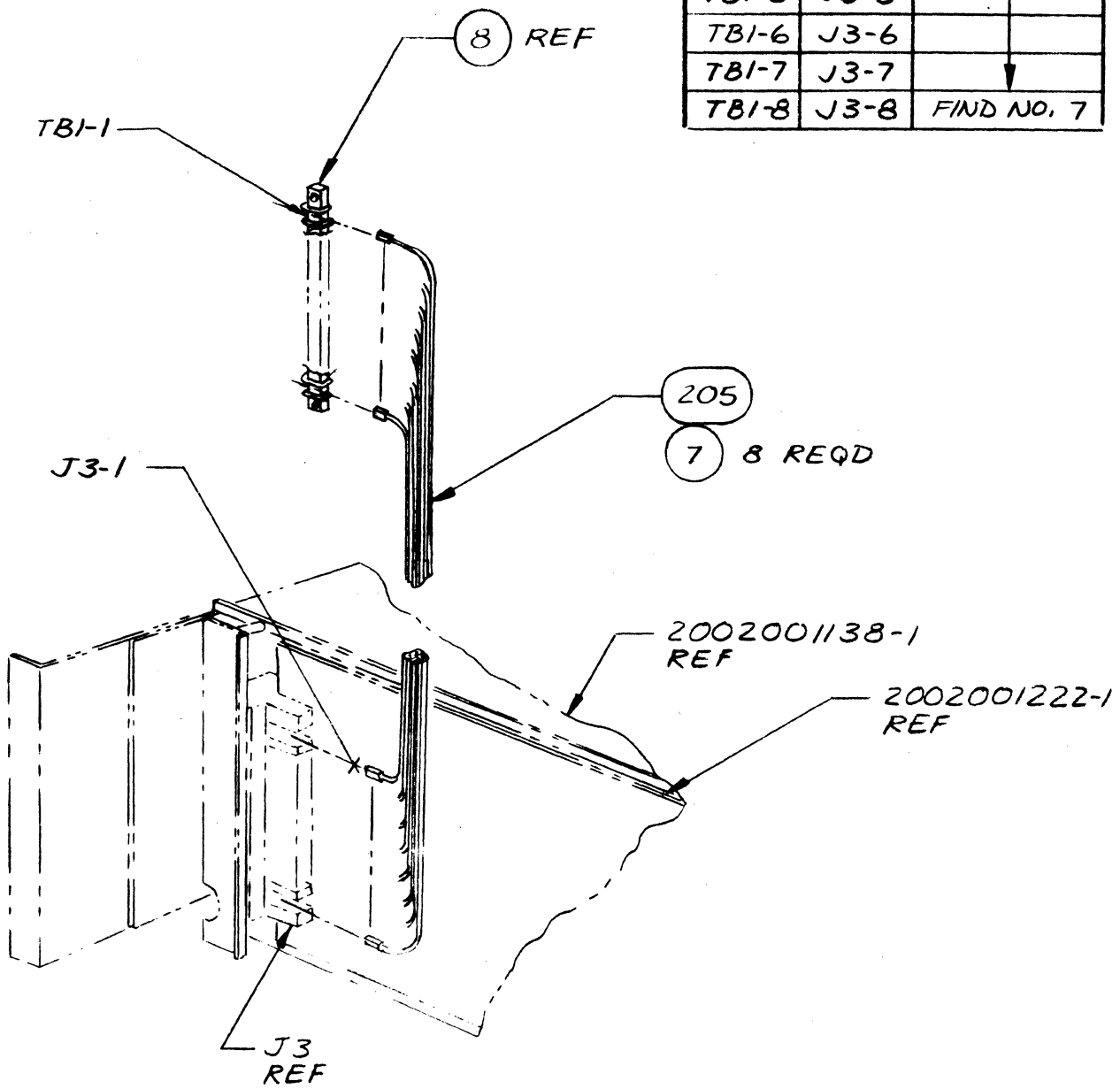
	SCALE —			SHEET 3



VIEW - F

	SIZE	CODE IDENT NO.		REV
	A	14715	2003000447	C
	SCALE ——		SHEET 4	

NEXT ASSEMBLY WIRING		
FROM	TO	USING
TB1-1	J3-1	FIND NO. 7
TB1-2	J3-2	
TB1-3	J3-3	
TB1-4	J3-4	
TB1-5	J3-5	
TB1-6	J3-6	
TB1-7	J3-7	
TB1-8	J3-8	FIND NO. 7



	SIZE	CODE IDENT NO.		REV
	A	14715	2003000447	C
	SCALE		SHEET 5	

LECW 234-1 K & E 2-70

PS2

WIRE LIST

WIRE NO. OR LINE	S	FROM	TO	LENGTH (INCHES)	REMARKS OR DESCRIPTION	COLOR	SIZE
1		TB1-1	J2-1		FIND NO. 19,16,16	WHITE	10 AWG
2		TB1-2	J1-2		FIND NO. 20,17 21	↑	20 AWG
3		TB1-3	J2-3		FIND NO. 20,17,17		20 AWG
4		TB1-4	J1-4		FIND NO. 19,16,16		10 AWG
5		TB1-5	J1-5		FIND NO. 19,16,16		↓
6		TB1-6	W1-4		FIND NO. 19,16,18,(204)		
7		TB1-7	W1-3		FIND NO. 19,16,18,(204)	↓	↓
8		TB1-8	J1-8		FINDNO. 19,16,16	WHITE	10AWG
9		TB1-9	CHAS GND		FIND NO. 6	GRN	14AWG
10		J1-1	W1-8		FIND NO. 19,16,18,(204)	WHITE	10AWG
11		J1-2	J2-2		FIND NO. 20,17,17,	↑	20 AWG
12		J1-6	W1-7		FIND NO. 19,16,18,(204)		10 AWG
13		J1-7	J2-7		FIND NO. 20,17,17	↓	20 AWG
14		J2-6	W1-19		FIND NO. 19,16,18,(204)	WHITE	10 AWG

PREPARED BY	LOCKHEED ELECTRONICS CO. DATA PRODUCTS DIVISION Los Angeles 22, Calif.	TITLE WIRE LIST
CHECKED		DWG. NO 2003000447 REV. C
APPROVED		CODE IDENT 14715 SHT 6

LECW Form 202-1

AEL

PREPARED RON RODGERS DATE 3-28-72
CHK L.A. Segura DATE 14NOV 72
ENGR [illegible] DATE [illegible]
PROJ ENGR DATE

LEC
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

A	14715	PL 20030000447-1	C
SIZE	CODE IDENT	SHEET 7	REV

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		20030000447-1		POWER SUPPLY ASSY		SUE 5952	1
002		001	0001		20020001206-1		POWER SUPPLY, DUAL		PLUS 5V 50A/ MINUS 15V 5A	2
003		001	0001		20020001251-1		POWER SUPPLY, SINGLE		PLUS 15V 25A	3
004		001	0001		10010004997-1		BUS BAR		W1	4
005		003	0001		10010004783-1		PLATE CONNECTOR MTG			5
006		001	0001		20020001207-1		LEAD, ELECT DC PWR			6
007		008	0001		20020002048-8		LEAD, ELECTRICAL		NOTE 205	7
008		001	0001		36009-3628	98410	TERMINAL BLOCK	ETC, INC	TB1	8
009		002	0001		11978-1	11873	MALE DISC BLOCK ASSY	UNDERWRITERS SAFETY DEVICE CO	J1, J2 NOTE 206	9
010		002	0001		5610-55-62	86928	WASHER, NYLON	SEASTROM		10
011	B	002	0001		TYPE 6-32		SCREW, PAN HD		6-32X2.50 CRES CROSS RECESSED	11
012		002	0001		9286-B-140-3	06540	SPACER, ROUND	AMATOM	NO.6X5/16 OD X .25 LG	12
013		001	0001		20020001308-1		POWER CONTACTOR ASSY			13

CONFORMS TO MIL-STD 100

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL	E — SOURCE CONTROL DWG	IC P — INTEGRATED CIRCUIT PKG	FOR REV RECORD SEE SHEET 1
B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO	F — SPEC CONTROL DWG	I S — INSERTION SPAN	
C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	M — DENOTES MAKE FROM	A/R — AS REQD	
	& — ALTERNATE SOURCE		

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

A	14715	PL 2003000447-1	C
SIZE	CODE IDENT	SHEET 8	REV

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
014		005	0001		MS35335-30	96906	WASHER,LK,FL EXT TH		NO. 6 NOTE 204	14
015		001	0001		2002001138-1		CARD GUIDE FRAME		SUE 7905	15
016		013	0001		C-8197-08	98410	TERMINAL,SNAP SPADE	ETC, INC	12-10AWG YELLOW	16
017		007	0001		AA-5191-08	98410	TERMINAL,SNAP SPADE	ETC, INC	22-18AWG RED	17
018	F	005	0001		1005000785-17		TERMINAL,LUG-RING		10-12AWG NO. 6 YEL	18
019		005	0001		A3065-01	90484	WIRE, STRANDED	ITT SURPRENANT	10AWG WHITE APPROX FT REQD	19
[illegible]	F	003	0001		9003400421-12		WIRE, STRANDED		20AWG WHITE APPROX FT REQD	20
021	F	001	0001		1005000787-1		TERMINAL,RECPT, TAB		22/18AWG .250TAB RED	21
[illegible]	F	001	0001		TYPE 511	78189	NUT, LOCK (6-32)	SHAKEPROOF	511-061800-00-0251-0551	22

CONFORMS TO MIL-STD-100

LECW 264 (JAN 70) K&E

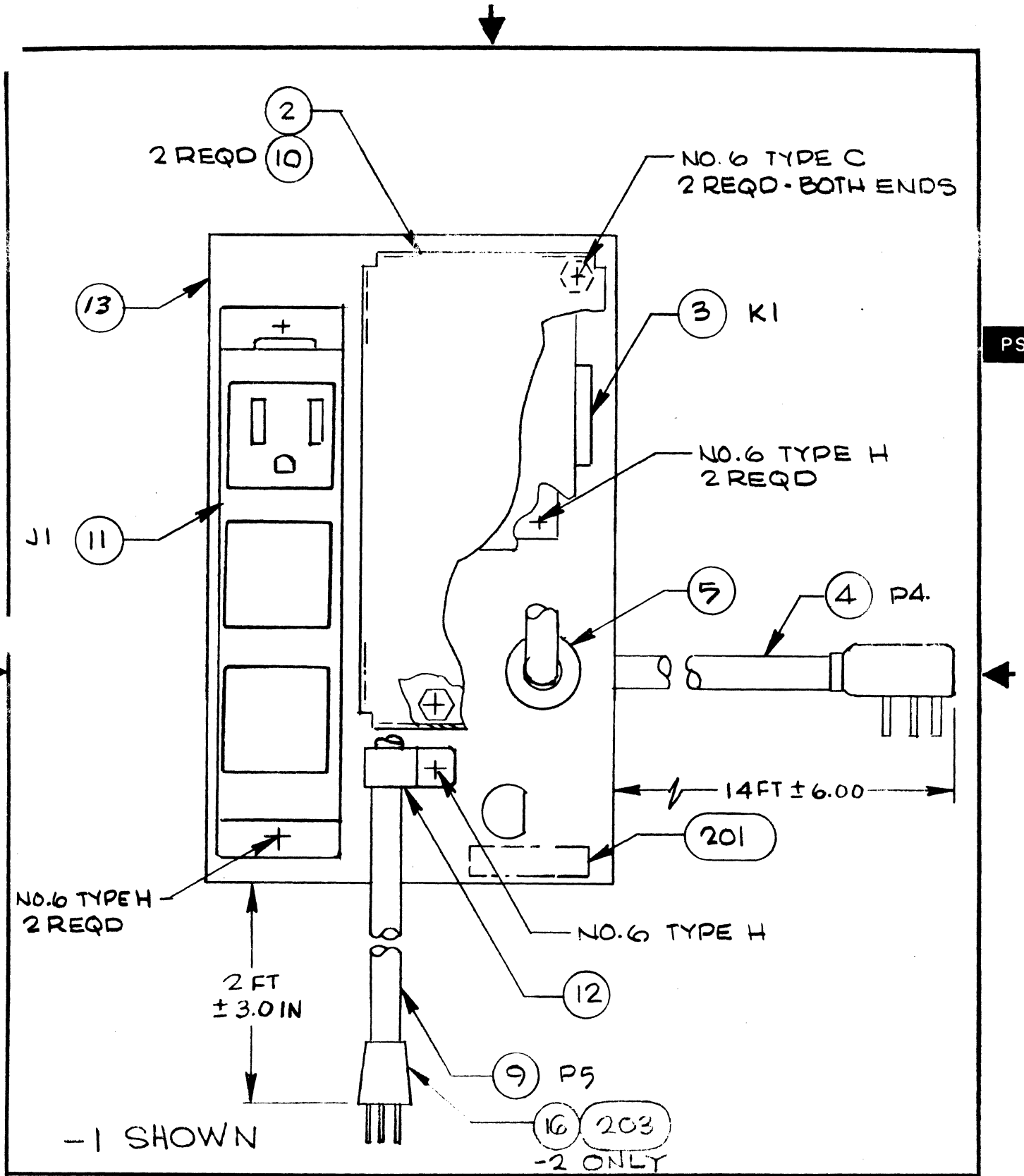
PS2

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT		REV
A	14715	PL 2003000447	C
		SHEET 11	

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-18		MARKING (IDENTIFY).			201
202		A/R	0001		LECP1049-11/12		MARKING.			202
203		A/R	0001		LECP1075		HARDWARE.			203
204		REF	0001				INSTALL PER LECP1075 NO. 6 TYPE H USING FIND NO. 14 AS SHOWN.			204
205		REF	0001				TO BE SUPPLIED AS LOOSE PARTS FOR USE ON NEXT ASSY.			205
206		REF	0001				REMOVE AND DISCARD THIS PIN.			206

CONFORMS TO MIL-STD-100



SIZE	CODE IDENT NO.		REV
A	14715	2002001308	C
SCALE NONE		SHEET 2	

-1 WIRE LIST

WIRE NO.	FROM	TO	COLOR	SIZE	FUNCTION	TERMINATION
1	J1	K1-5	BLK	14		FIND NO 7
2	J1	K1-6	WHT	14		FIND NO. 7
3	J1	GND	GRN	14		FIND NO 15
4	P4	K1-4	WHT	12		FIND NO. 14
5	P4	K1-3	BLK	12		FIND NO. 14
6	P4	GND	GRN	12		FIND NO. 14
7	P5	K1-1	BLK	18		FIND NO. 8
8	P5	K1-2	WHT	18		FIND NO. 8
9	P5	GND	GRN	18		FIND NO. 6

-2 WIRE LIST

1	J1	K1-5	BLK	16		FIND NO. 7
2	J1	K1-6	WHT	16		FIND NO. 7
3	J1	GND	GRN	16		FIND NO. 15
4	P4	K1-4	WHT	12		FIND NO. 14
5	P4	K1-3	BLK	12		FIND NO. 14
6	P4	GND	GRN	12		FIND NO. 14
7	P5	K1-1	BLK	18		FIND NO. 8
8	P5	K1-2	WHT	18		FIND NO. 8
9	P5	GND	GRN	18		FIND NO. 6

SIZE	CODE IDENT NO.		REV
A	14715	2002001308	C
		SHEET 3	

Form E

JNH

PREPARED J. BARRIO	DATE 8/10/72	LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90040	A 14715 PL 2002[illegible]1308-1 C
CHK W. Reuter	DATE 9/14/72		
ENGR W. Reuter	DATE 9/1./72		SIZE CODE IDENT SHEET 4 REV
PROJ ENGR H. Wenzel	DATE 10/4/72		

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2002001308-1		POWER CONTACTOR ASSY		USED ON SUE 5952	1
002	001	0001		1001005197-1		COVER, CONTACTOR			2
003	001	0001		75-905	80089	RELAY	RBM CONTROLS	K1	3
004	001	0001		3088	22012	POWER CABLE	WABER	12AWG TYPE S RT ANGLE NEMA 5-20P 15 FT P4	4
005	001	0001		SR-9P-1	28520	BUSHING	HEYCO		5
006	E 001	0001		1005000786-1		TERM, LUG SNAP SPADE		22-18AWG NO. 6 RED	6
007	E 002	0001		1005000786-5		TERM, LUG SNAP SPADE		22-14AWG NO. 6 BLUE	7
008	E 002	0001		1005000787-1		FASTON RECEPTACLE		22-18AWG RED	8
009	001	0001		17407	70903	CONTROL CABLE	BELDEN	18AWG TYPE SJT 8FT NEMA5-15P P5	9
[illegible]	002	[illegible]		SFSS-SS-0632-7	06540	STANDOFF	AMATOM	6-32 3/8 HEX 2.75 LG	[illegible]
011	001	0001		L18E8-3	22012	OUTLET BOX	WABER	J1	11
011&	000	0001		2002001431-1		OUTLET ASSY AC		J1	11&
012	001	0001		HP-5N	09922	CLAMP CABLE	BURNDY	NO. 6	12

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	E — SOURCE CONTROL DWG F — SPEC CONTROL DWG M — DENOTES MAKE FROM & — ALTERNATE SOURCE	IC P — INTEGRATED CIRCUIT PKG I S — INSERTION SPAN A/R — AS REQD	FOR REV RECORD SEE SHEET 1

LECW 263 (JAN 70) K&E

PS2

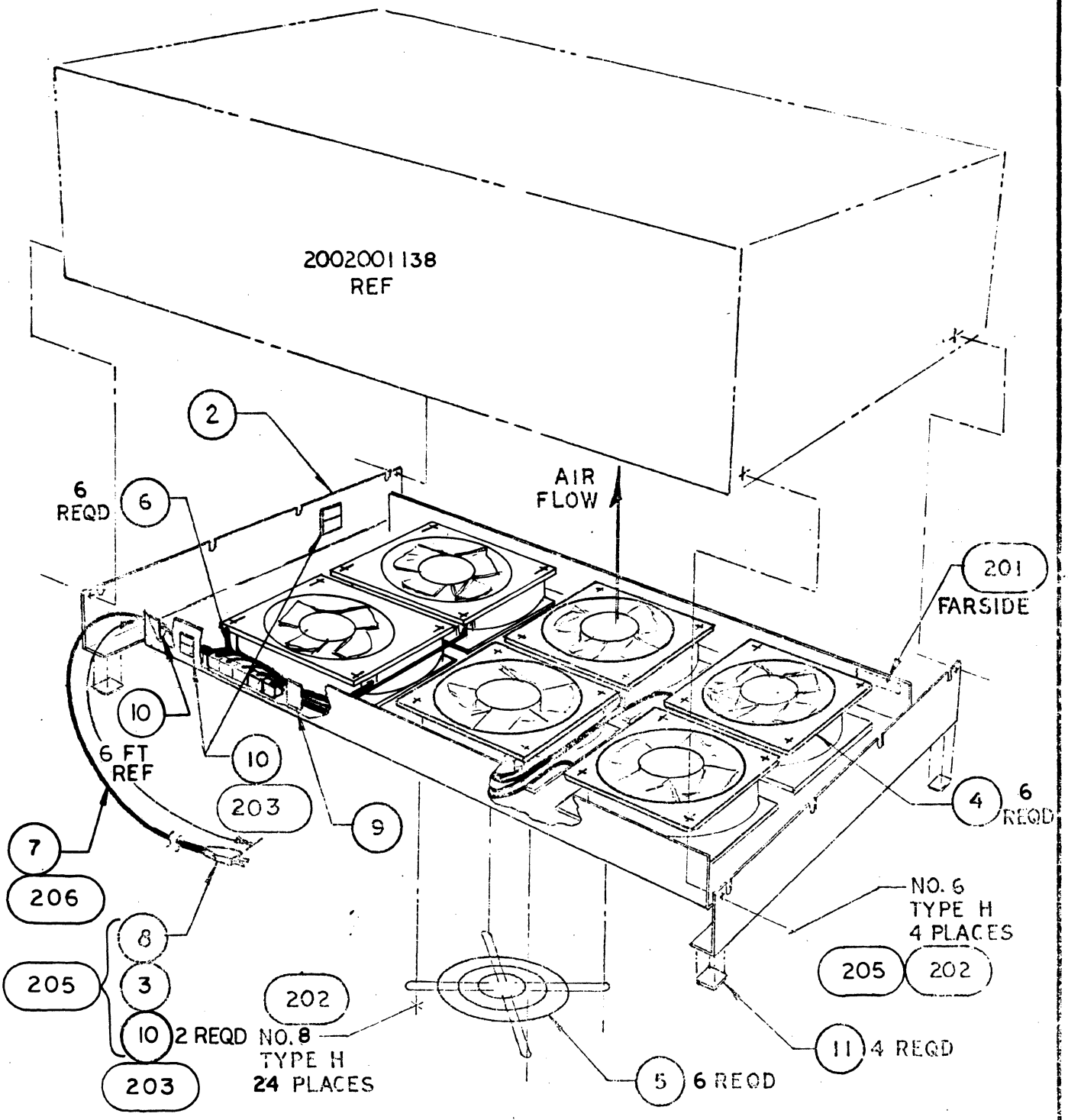
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	SHEET	REV
A	14715	PL 2002001308-1	C

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
013		001	0001		1001005039-1		PLATE, CONTACTOR MTG			13
014	E	003	0001		1005000786-8		TERM, LUG SNAP SPADE		12-10AWG YEL	14
015	E	001	0001		1005000786-4		TERM, LUG SNAP SPADE		16-14AWG BLUE	15

CONFORMS TO MIL-STD-100

-2,-3,-6 ASSEMBLY'S



SIZE	CODE IDENT NO.		REV
A	14715	20020011 48	D
SCALE ——		SHEET 3	

PS2

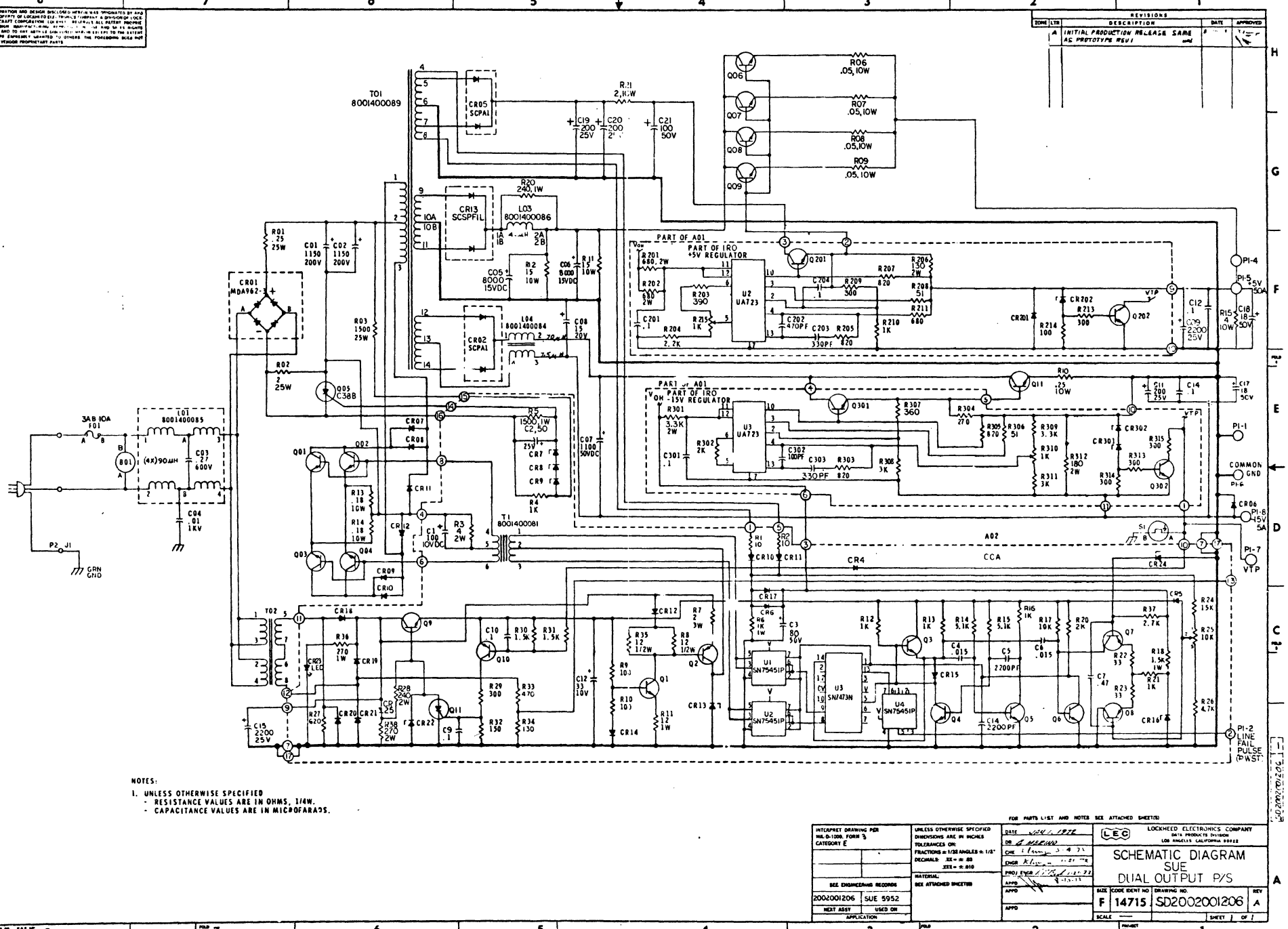
AEL

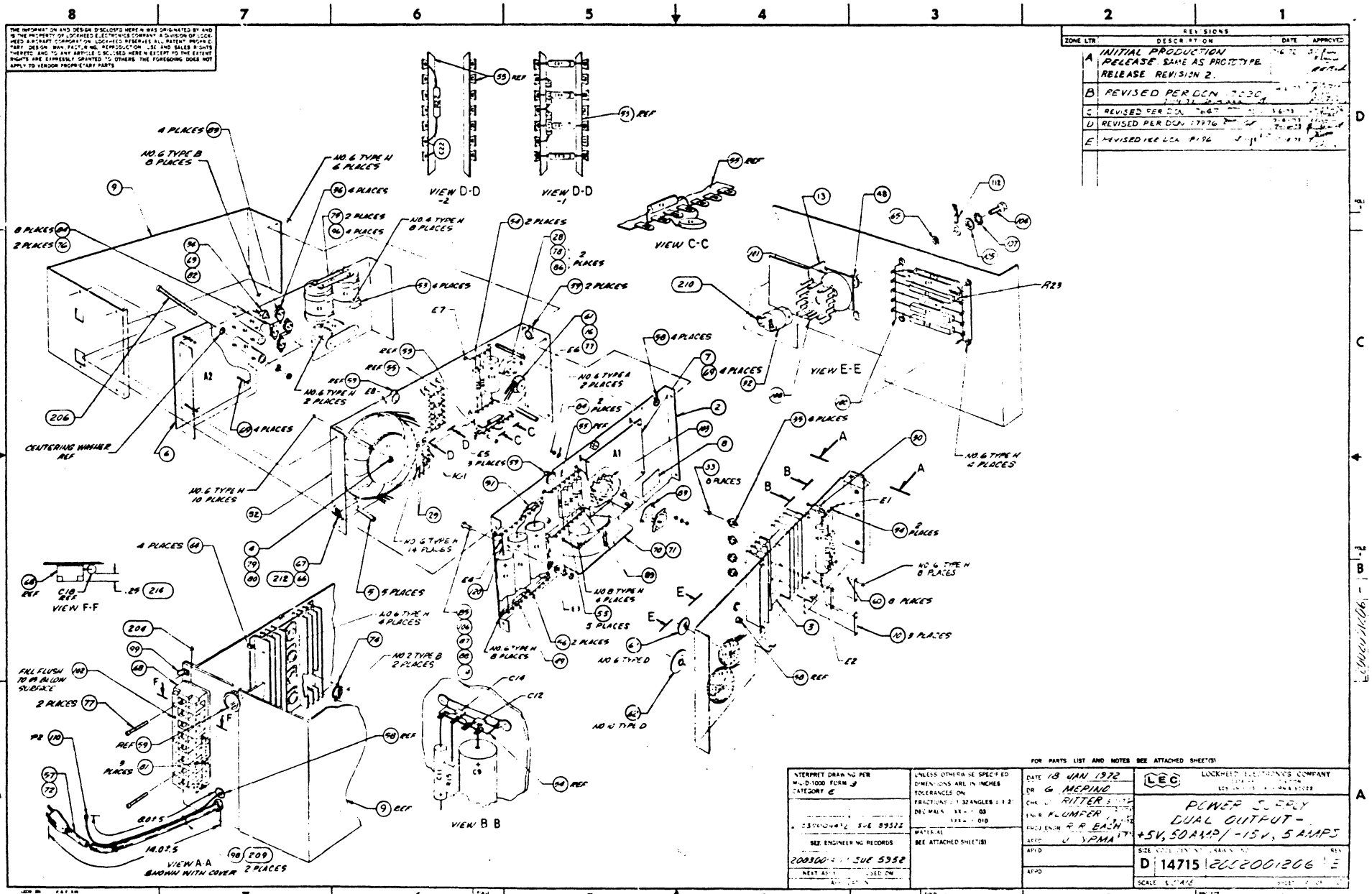
PREPARED E. MARIANO	DATE 2-22-72	LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022	A 14715 PL 2002001148-2 D
CHK J. Clifton	DATE 2-22-72		
ENGR	DATE		SIZE CODE IDENT SHEET 6 REV
PROJ ENGR	DATE		

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2002001148-2		ASSY, FAN PACK		SUE 7921	1
002	001	0001		1001004817-1		BRACKET, FAN			2
003	001	0001		MS3420-4	96906	BUSHING, CABLE			3
004	006	0001		1005000906-2		FAN, TUBE AXIAL		95 CFM, 115 VAC BLK ON YEL LABEL	4
005	006	0001		1005000905-1		GUARD, FAN			5
006	006	0001		C-2053-012-PL	80126	FAN LINE CORD	PACIFIC ELEC	MALE-FEMALE	6
007	001	0001		C-2055-006-PL	80126	FAN LINE CORD	PACIFIC ELEC	FEMALE-STRIP	7
008	001	0001		12475	73545	PLUG, ELECTRICAL	CABLE ELEC PROD	NEMA 1-15P	8
009	000	0001		380	73545	PLUG, ELECTRICAL	CABLE ELEC PROD	BULK PACK (250)	8&
009	001	0001		8511-03-00-9909	02768	CLIP, CORD-1/2	FASTEX ITW	APPROX QTY REQD	9
010	005	0001		8511-01-00-9909	02768	CLIP, CORD-1/4	FASTEX ITW	APPROX QTY REQD	10
011	004	0001		SJ-5023-BLACK	04963	PAD, POLYURETHANE	3M CO	.300 HT X.812 WD	11
012	000								12
013	000								13

CONFORMS TO MIL-STD-100A

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	E — SOURCE CONTROL DWG F — SPEC CONTROL DWG M — DENOTES MAKE FROM & — ALTERNATE SOURCE	IC P — INTEGRATED CIRCUIT PKG I S — INSERTION SPAN A/R — AS REQD	FOR REV RECORD SEE SHEET 1


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A INITIAL PRODUCTION RELEASE SAME AS PROTOTYPE REV1
T01 8001400089
T02
T1 8001400081
L01 8001400085
L03 8001400086
L04 8001400084
CR01 MDA962-3
CR02 SCPA1
CR05 SCPA1
CR13 SCSPF1L
Q01
Q02
Q03
Q04
Q05 C388
Q06
Q07
Q08
Q09
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q201
Q202
Q301
Q302
U1 SN75451P
U2 SN75451P
U3 SN7473N
U4 SN75451P
U2 UA723
U3 UA723
PART OF A01
PART OF 1R0 +5V REGULATOR
PART OF 1R0 ON -15V REGULATOR
A02
CCA
PI-1
PI-2 LINE FAIL PULSE (PWST)
PI-4
PI-5 +5V 50A
PI-6 COMMON GND
PI-7 VTP
PI-8 15V 5A
P2 J1
GRN GND
3AB 10A
NOTES:
1. UNLESS OTHERWISE SPECIFIED
- RESISTANCE VALUES ARE IN OHMS, 1/4W.
- CAPACITANCE VALUES ARE IN MICROFARADS.
FOR PARTS LIST AND NOTES SEE ATTACHED SHEET(S)
INTERPRET DRAWING PER MIL-D-1000, FORM 3, CATEGORY E
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON: FRACTIONS ± 1/32 ANGLES ± 1/2° DECIMALS .XX = ± .03 .XXX = ± .010
MATERIAL SEE ATTACHED SHEET(S)
SEE ENGINEERING RECORDS
2002001206 SUE 5952
NEXT ASSY USED ON
APPLICATION
DATE NOV. 1978
DR G. MARINO
CHK
ENGR
PROJ ENGR
APPD
APPD
APPD
LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022
SCHEMATIC DIAGRAM
SUE
DUAL OUTPUT P/S
SIZE F
CODE IDENT NO 14715
DRAWING NO SD2002001206
REV A
SCALE —
SHEET 1 OF 1
PS2


REVISIONS
ZONE LTR
DESCRIPTION
DATE
APPROVED
A INITIAL PRODUCTION RELEASE. SAME AS PROTOTYPE RELEASE REVISION 2.
B REVISED PER DCN
C REVISED PER DCN
D REVISED PER DCN 17976
E REVISED PER DCN 19196
VIEW D-D -2
VIEW D-D -1
VIEW C-C
VIEW E-E
VIEW F-F
VIEW A-A SHOWN WITH COVER
VIEW B B
4 PLACES
NO. 6 TYPE B 8 PLACES
NO. 6 TYPE N 6 PLACES
2 PLACES
NO. 6 TYPE N 8 PLACES
NO. 6 TYPE N 10 PLACES
NO. 6 TYPE N 14 PLACES
NO. 6 TYPE N 4 PLACES
NO. 6 TYPE A 9 PLACES
NO. 8 TYPE N 4 PLACES
NO. 6 TYPE N 2 PLACES
NO. 6 TYPE D
NO. 2 TYPE B 2 PLACES
NO. 4 TYPE N 2 PLACES
NO. 6 TYPE N 6 PLACES
NO. 6 TYPE N 4 PLACES
5 PLACES
9 PLACES
8 PLACES
CENTERING WASHER REF
FILL FLUSH TO 99 BELOW SURFACE
14.07.5
8.01.5
A1
A2
E1
E2
E3
E4
E5
E6
E7
E8
C9
C12
C14
C16
R29
FOR PARTS LIST AND NOTES SEE ATTACHED SHEET(S)
INTERPRET DRAWING PER MIL-D-1000 FORM 3 CATEGORY C
SEE ENGINEERING RECORDS
NEXT ASSY USED ON
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± 1/32 ANGLES ± 1/2 DECIMALS .XX ± .03 .XXX ± .010
MATERIAL SEE ATTACHED SHEET(S)
DATE 18 JAN 1972
DR G MEPINO
CHK R RITTER
ENGR R KLIMPER
PROJ ENGR R R EACH
APPD J SPMA
APPD
APPD
LOCKHEED ELECTRONICS COMPANY
PLAINFIELD, NEW JERSEY
POWER SUPPLY
DUAL OUTPUT -
+5V, 50 AMPS / -15V, 5 AMPS
SIZE D
14715
2022001206
REV E
SCALE
PS2

JNH

PREPARED R. RODGERS	DATE 1/26/72	LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022	B 14715 PL 2002001206-1 D
CHK [illegible]	DATE 3-[illegible]-72		
ENGR K Lumpp	DATE 3-7-72		SIZE CODE IDENT SHEET 2 REV
PROJ ENGR R.A. Bock	DATE 3-7-72		

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2002001206-1		POWER SUPPLY		USED ON SUE 5952	1
002		001	0001		1001004755-1		PLATE, LEFT SIDE			2
003		001	0001		1001004756-1		HEAT SINK			3
004		001	0001		1001004508-1		WASHER, RETAINING			4
005	F	005	0001		1005000793-1		STANDOFF			5
006		001	0001		2001002156-1		CCA-CKT CARD ASSY		A2 NOTE 216	6
007		001	0001		2001002157-2		IRC-CKT CARD A'		A1 NOTE 216	7
008		001	0001		1005000777-1		NAMEPLATE		NOTE 202	8
009		001	0001		1001004769-1		COVER			9
010		003	0001		1001004866-1		BUS-[illegible]			10
011	E	001	0001		8001400089-1		TRANSFORMER, P-[illegible]		T1	11
012		001	0001		P6375	80089	TRANSFORMER	CHICAGO STANCOR	T2	12
013		001	0001		1001005347-1		BRACKET, RECTIFIER			13
014	E	001	0001		8001400086-1		REACTOR		L3	14
015	E	001	0001		8001400084-1		REACTOR		L4	15
016	E	001	0001		8001400085-1		REACTOR, INPUT BALUN		L1	16
017	B	004	0001		TYPE 1700S	00213	RESISTOR	SAGE	R6 THRU R9 1700S-.050HM3PCT	17
018	B	001	0001		TYPE 2D-2	75042	RESISTOR	IRC, INC	R2 2D-2 OHM5PCT VERT MTG KIT NOTE 206	18
019	B	001	0001		TYPE 2D-.25	75042	RESISTOR	IRC, INC	R1 2D-.25 OHM10PCT VERT MTG KIT NOTE 206	19
020	B	001	0001		TYPE 2D-[illegible]	75042	RESISTOR	IRC, INC	R3 2D-1500 OHM5PCT VERT MTG KIT NOTE 206	20
021	B	001	0001		TYPE PW10-.25	75042	RESISTOR	IRC, INC	R10 PW10-.250HM10PCT	21
022	B	002	0001		TYPE PW10-15	75042	RESISTOR	IRC, INC	R11,12 PW10-15 OHM5PCT	22
023	B	002	0001		TYPE PW10-.18	75042	RESISTOR	IRC, INC	R13,14 PW10-.180HM10PCT	23
024		002	0001		20AWG WHT		TUBING (TEFLON)	MIL-1-22129	APPROX FT REQD	24
025		000								25
026		002	0001		S4M	14099	DIODE	SEMTECH	CR11,12	26
027		004	0001		1N4720	13327	DIODE	SOLITRON	CR7 THRU CR10	27
028		001	0001		MDA962-3	04713	FULL WAVE BRIDGE	MOTOROLA	CR1	28
029		002	0001		SCPA1	14099	RECTIFIER, ASSY	SEMTECH	CR2,5 NOTE 207	29
030		001	0001		40HF5	81483	DIODE	INTL RECTIFIER	CR6	30
031		000								31
032		1	0001		SCSPF1L	14099	RECTIFIER, ASSY	SEMTECH	CR13 NOTE 207	32

CONFORMS TO MIL-STD-100A

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	E — SOURCE CONTROL DWG F — SPEC CONTROL DWG M — DENOTES MAKE FROM & — ALTERNATE SOURCE	ICP — INTEGRATED CIRCUIT PKG IS — INSERTION SPAN A/R — AS REQD	FOR REV RECORD SEE SHEET 1

LECW 239 (JAN 70) K&E

PS2

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	SHEET	REV
B	14715	PL 2002001206-1	D

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
033	B	008	0001		TYPE 511-061800	78189	NUT, LOCK	SHAKEPROOF	511-061800-01-0251-0551	33
034		001	0001		C38B	09214	SCR	GENERAL ELEC	Q5 NOTE 207	34
035		005	0001		2N5885	04713	TRANSISTOR	MOTOROLA	Q6,7,8,9,11 NOTE 207	35
036		004	0001		DTS-430	16758	TRANSISTOR	DELCO RADIO	Q1 THRU Q4 NOTE 207	36
038	B	001	0001		TYPE PW10-2	75042	RESISTOR	IRC, INC	R21 PW10-2 OHM10PCT	37
039	B	001	0001		TYPE PW10-4	75042	RESISTOR	IRC, INC	R15 PW10-4 OHM10PCT	38
040	F	002	0001		8001300101-1		CAPACITOR		C12,14	39
041		002	0001		71C200JB1151	99392	CAPACITOR	STM	C1,2	40
042		001	0001		DD1032	71690	CAPACITOR	CENTRALAB	C4	41
043		001	0001		ZD6A274	02980	CAPACITOR	ELPAC	C3	42
044		001	0001		8001300314-1		CAPACITOR		C21	43
045		002	0001		8001300392-1		CAPACITOR		C17,18	44
046		001	0001		39D118G050HP4	56289	CAPACITOR	SPRAGUE	C7	45
047		002	0001		39D228G025HP4	56289	CAPACITOR	SPRAGUE	C9,15	46
048		002	0001		39D808G015JT4	56289	CAPACITOR	SPRAGUE	C5,6	47
049		001	0001		2322-N317	06540	WASHER, INSULATED	AMATOM	NO. 5/16	48
050		001	0001		8001300333-2		CAPACITOR		C8	49
051		003	0001		TE-1213	56289	CAPACITOR	SPRAGUE	C11,19,20	50
052		001	0001		RL32S241G		RESISTOR	MIL-R-22684/3	R20	51
053		001	0001		1001004754-2		PLATE, RIGHT SIDE			52
054		004	0001		6179-2A	91506	CLIP, COMPONENT	AUGAT	(C1,C2)	53
055		004	0001		326-20-04-001	71785	TERMINAL STRIP	CINCH	TB1,2,8,9	54
056		005	0001		326-20-07-001	71785	TERMINAL STRIP	CINCH	TB3,4,7,10,11	55
057		002	0001		326-20-10-001	71785	TERMINAL STRIP	CINCH	TB5,6	56
058		001	0001		SR-6P3-4	28520	BUSHING	HEYMAN MFG		57
059		004	0001		OCB-500	28520	BUSHING, OPEN/CLOSE	HEYMAN MFG		58
060		003	0001		OCB-875	28520	BUSHING, OPEN/CLOSE	HEYMAN MFG		59
061	B	008	0001		TYPE 2636-24850	06540	WASHER, SHOULDER	AMATOM	2636-24850-PH140 (Q6 THRU Q9)	60
062		002	0001		100-5	08289	RETAINER, TOROID	DELBERT BLINN	(L1,L4)	61
063		001	0001		100-6	08289	RETAINER, TOROID	DELBERT BLINN	(L3)	62
064		001	0001		NY25-030	08289	INSULATOR, NYLON	DELBERT BLINN		63
065		004	0001		304-025	98978	STANDOFF BUSHING	IERC		64
066		001	0001		2718-49550-N317	06540	WASHER, SHOULDER	AMATOM CO	NO. 5/16	65
067		001	0001		348875	75915	FUSE HOLDER	LITTELFUSE	XF1	66
068		001	0001		314010	75915	FUSE	LITTELFUSE	F1(3AB 10A 250V)	67
069		001	0001		11978-82	11873	DISCONNECT BLOCK	UNDERWRITERS SAFETY DEVICE CO	P1 (FEMALE)	68
070		008	0001		CBS-10N	06915	SUPPORT, CIRCUIT BD	PICHCO PLASTIC		69
071		001	0001		1005000906-2		FAN		B1(95CFM, 115VAC)	70

CONFORMS TO MIL-STD-100

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
072		001	0001		C-2055-015-BL	80126	LINE CORD, FAN	PACIFIC ELECTRICORD CO	(B1)	71
073		001	0001		C1316-006-BL	80126	LINE CORD, AC	PACIFIC ELECTRICORD CO	6FT, 16/3	72
074		000								73
075	B	001	0001		TYPE A-672	93410	THERMOSTAT	ESSEX INTL INC	S1 - A-672 CLOSE 190 DEG OPEN 165 DEG SEE NOTE 207	74
076		002	0001		1001004866-3		BUS BAR			75
077		002	0001		1001004866-2		BUS BAR			76
078		003	0001		MS51957-35	96906	SCREW, PAN HD		6-32 X 1.25 LG	77
079	F	002	0001		9002200582-1		SCREW, PAN HD		4-40 X 1.00 LG	78
080		001	0001		MS51957-54	96906	SCREW, PAN HD		8-32 X 2.25 LG	79
081		001	0001		22NM832	15653	NUT, LOCK	KAYNAR	8-32	80
082		003	0001		AA5191-08	98410	LUG	ETC, INC	APPROX QTY REQD	81
083		001	0001		DF6B	02735	INSULATOR, MICA	RCA	(Q5)	82
084		005	0001		495320	02735	INSULATOR, MICA	RCA	(Q1 THRU Q4,Q11)	83
085		010	0001		495334-7	02735	WASHER, NYLON	RCA	(Q1 THRU Q4,Q11)	84
086		001	0001		MS90725-4	96906	SCREW, CAP, HEX HD		1/4-20 X .56 LG	85
087		002	0001		MS15795-804	96906	WASHER, FLAT		NO. 4	86
088		001	0001		MS35338-44	96906	WASHER, LOCK		NO. 1/4	87
089		001	0001		MS35649-2252	96906	NUT, HEX		1/4-20 -	88
090		002	0001		MS15795-805	96906	WASHER, FLAT		NO. 6	89
091	F	003	0001		9003400421-18		WIRE, STRANDED		14AWG WHT APPROX FT REQD	90
092	F	030	0001		9003400421-16		WIRE, STRANDED		16AWG WHT APPROX FT REQD	91
093	F	003	0001		9003400421-15		WIRE, STRANDED		16AWG BLK APPROX FT REQD	92
094	F	030	0001		9003400421-12		WIRE, STRANDED		20AWG WHT APPROX FT REQD NOTE 216	93
095		003	0001		AWG18 TYPE S		WIRE, SOLID, UNINSUL	QQ-W-343	18AWG APPROX FT REQD	94
096	F	003	0001		9003400419-9		WIRE, SOLID, UNINSUL		20AWG APPROX FT REQD	95
097		004	0001		MS35335-32	96906	WASHER, EXT TOOTH		NO. 10	96
098		A/R	0001		NO. 340	71984	SILICONE HT SK CMPD	DOW CORNING	NOTE 207	97
099		002	0001		MS3367-5	96906	STRAP TIEDOWN		NOTE 209	98
100	E	001	0001		1005000787-22		TERMINAL, TAB		J1	99
101		002	0001		326-20-05-001	71785	TERMINAL STRIP	CINCH	TB12,13	100
102		001	0001		MW-1000-328-006	08289	WASHER, MICA	DELBERT BLINN	(CR13)	101
103		A/R	0001		K-22 BLACK	16245	CONAP EPOXY	CONAP INC		102
104		001	0001		UP1-T03-B	98978	HEAT SINK	IERC	(Q11)	103

CONFORMS TO MIL-STD-100

PS2

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	PL	REV
B	14715	2002001206-1	D

SHEET 5

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
105		001	0001		MS90725-32	96906	SCREW, CAP HEX HD		5/16-18 X .75 LG	104
106		001	0001		MS27183-12	96906	WASHER, FLAT		NO. 5/16	105
107		001	0001		MS27183-10	96906	WASHER, FLAT		NO. 1/4	106
108		001	0001		MS35335-34	96906	WASHER, LOCK		NO. 5/16	107
109		001	0001		UP-TE28-CB	98978	HEAT SINK	IERC	(CR13)	108
110	E	002	0001		1005000785-14		LUG, RING		16-24AWG NO. 10 NOTE 211 APPROX QTY REQD	109
111	E	009	0001		1005000787-3		TERMINAL RECPT		FASTON 250 16-14AWG NOTE 211 APPROX QTY REQD	110
112	E	004	0001		1005000787-5		TERMINAL RECPT		FASTON 250 12-14AWG APPROX QTY REQD	111
113		001	0001		MS25036-104	96906	LUG, RING		22-18AWG NO.5/16 NOTE 211 APPROX QTY REQD	112
114		008	0001		MS25036-102	96906	LUG, RING		22-18AWG NO. 6 NOTE 211 APPROX QTY REQD	113
115	E	004	0001		1005000785-15		LUG, RING		16-14AWG NO.1/4 NOTE 211 APPROX QTY REQD	114
116	E	008	0001		1005000787-1		TERMINAL RECPT		FASTON 250 22-18AWG NOTE 211 APPROX QTY REQD	115
117	E	004	0001		1005000785-12		LUG, RING		14-16AWG NO. 6 NOTE 211	116
118	E	002	0001		1005000785-20		LUG, RING		12-10AWG NO. 1/4 NOTE 211	117
119	E	003	0001		1005000785-10		LUG, RING		22-18AWG NO. 1/4 NOTE 211 APPROX QTY REQD	118
120		002	0001		34306	00779	SPLICE	AMP	16-14AWG APPROX QTY REQD	119
121		001	0001		18AWG WHT		TUBING (TEFLON)	MIL-I-22129	APPROX FT REQD	120
122		REF	0001		SD2002001206-1		SCHEMATIC DIAGRAM			121
123		REF	0001		WL2002001206-1		WIRE LIST			122
124		REF	0001		AP2002001206-1		ACCEPTANCE TEST PROC			123
125		REF	0001		DS2002001206-1		DESIGN SPECIFICATION			124
126		A/R	0001		SN60/SN63		SOLDER	QQ-S-571	NOTE 216	125

CONFORMS TO MIL-STD-100

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	SHEET	REV
B	14715	PL 2002001206 10	D

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			201
202		A/R	0001		LECP1049-16		MARK FIND NUMBER 8 .09 HIGH CHARACTERS (TYPEWRITER MAY BE USED) AS FOLLOWS: (-1 ONLY) TOP BLOCK: UNIT TITLE 2ND BLOCK: PART NUMBER 3RD BLOCK: SERIAL NUMBER 4TH BLOCK: 105-125 VAC, 47-63HZ			202
203		A/R	0001				REMOVE MOLDED PLUG FROM FIND NUMBER 72 AND REPLACE WITH FIND NUMBER 126.			203
204		REF	0001				ALLOW .010 TO .040 GAP FOR CONNECTOR FLOAT ALIGNMENT.			204
205		A/R	0001		LECP1075		HARDWARE.			205
206		REF	0001				INSTALL R1,2,3 USING SCREW, CENTERING WASHER, LOCKWASHER AND NUT FROM VERTICAL MOUNTING KIT. DISCARD UNUSED HARDWARE.			206
207		A/R	0001				MOUNT Q1 THRU Q9,Q11,CR2,5,13,S1 USING THERMAL COMPOUND FIND NO. 97.			207
208		000								208
209		REF	0001				INSTALL FIND NO. 98 TO ALLOW FOR ADJUSTMENT BETWEEN FIND NO. 72 AND GREEN WIRE.			209
210		REF	0001				BEND LUGS 90 DEGREES, STARTING BEND .12 FROM DIODE CAUTION: DO NOT FRACTURE INSULATION.			210
211		REF	0001		WL2002001206-1,-2		SEE WIRE LIST FOR LOCATION.			211
212		REF	0001				INSTALL FIND NO. 110 (TERMINAL) ON FIND NO. 66 (FUSE HOLDER) PRIOR TO INSTALLING FIND NO. 67 (FUSE) INTO FUSE HOLDER.			212
213		000								213
214		REF	0001				TO BE CLEAR OF ANY WIRING AND COMPONENTS.			214
215		A/R	0001		LECP1049-16		MARK FIND NUMBER 8 .09 HIGH CHARACTERS (TYPEWRITER MAY BE USED) AS FOLLOWS: (-2 ONLY) TOP BLOCK: UNIT TITLE 2ND BLOCK: PART NUMBER 3RD BLOCK: SERIAL NUMBER 4TH BLOCK: 200-240 VAC, 47-53HZ			215
216		A/R	0001				INSTALL FIND NUMBER 93 ON FIND NUMBERS 6 AND 7 BY INSERTING IN .060 DIAMETER HOLE AND SOLDERING WITH FIND NUMBER 125.			216

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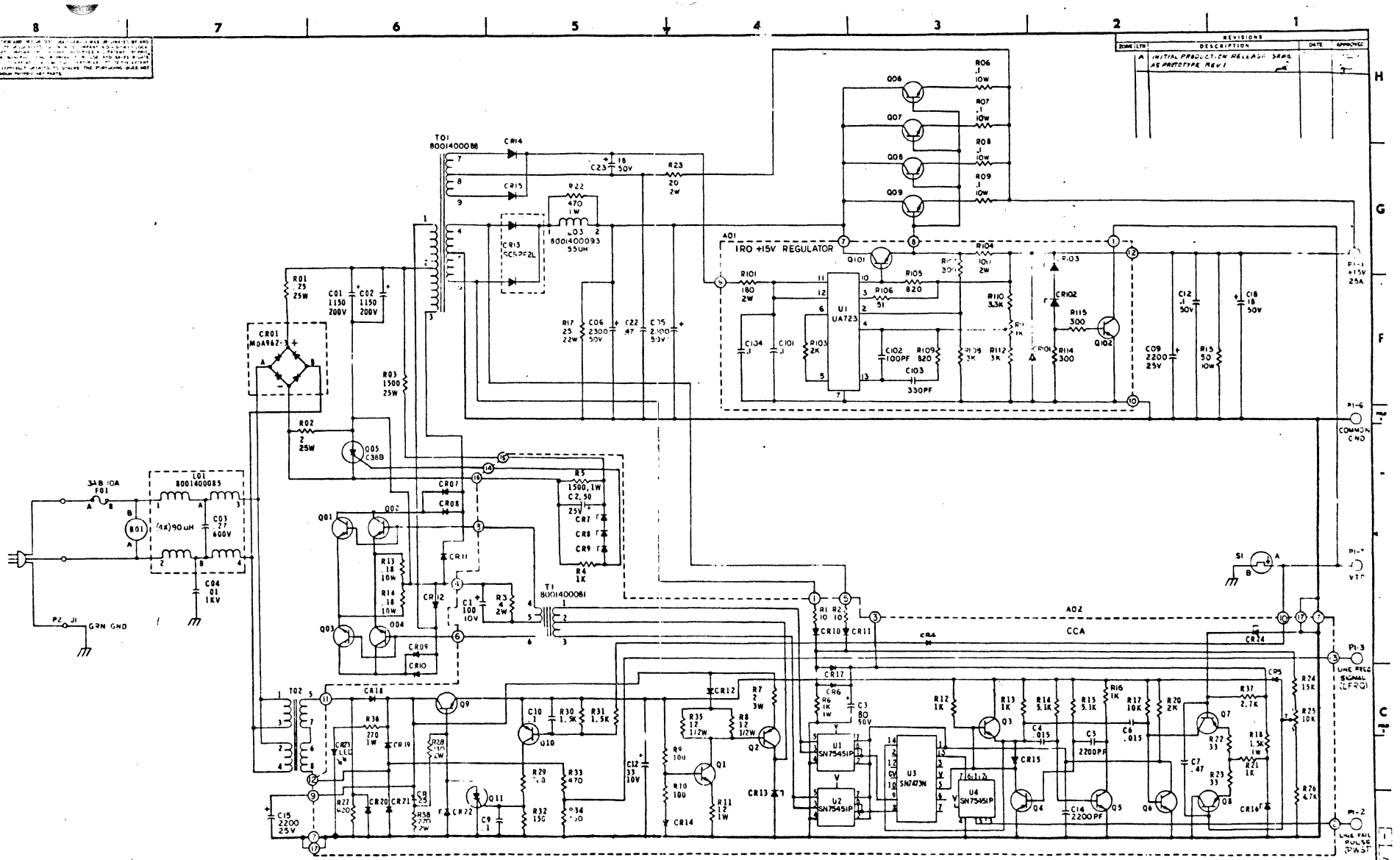
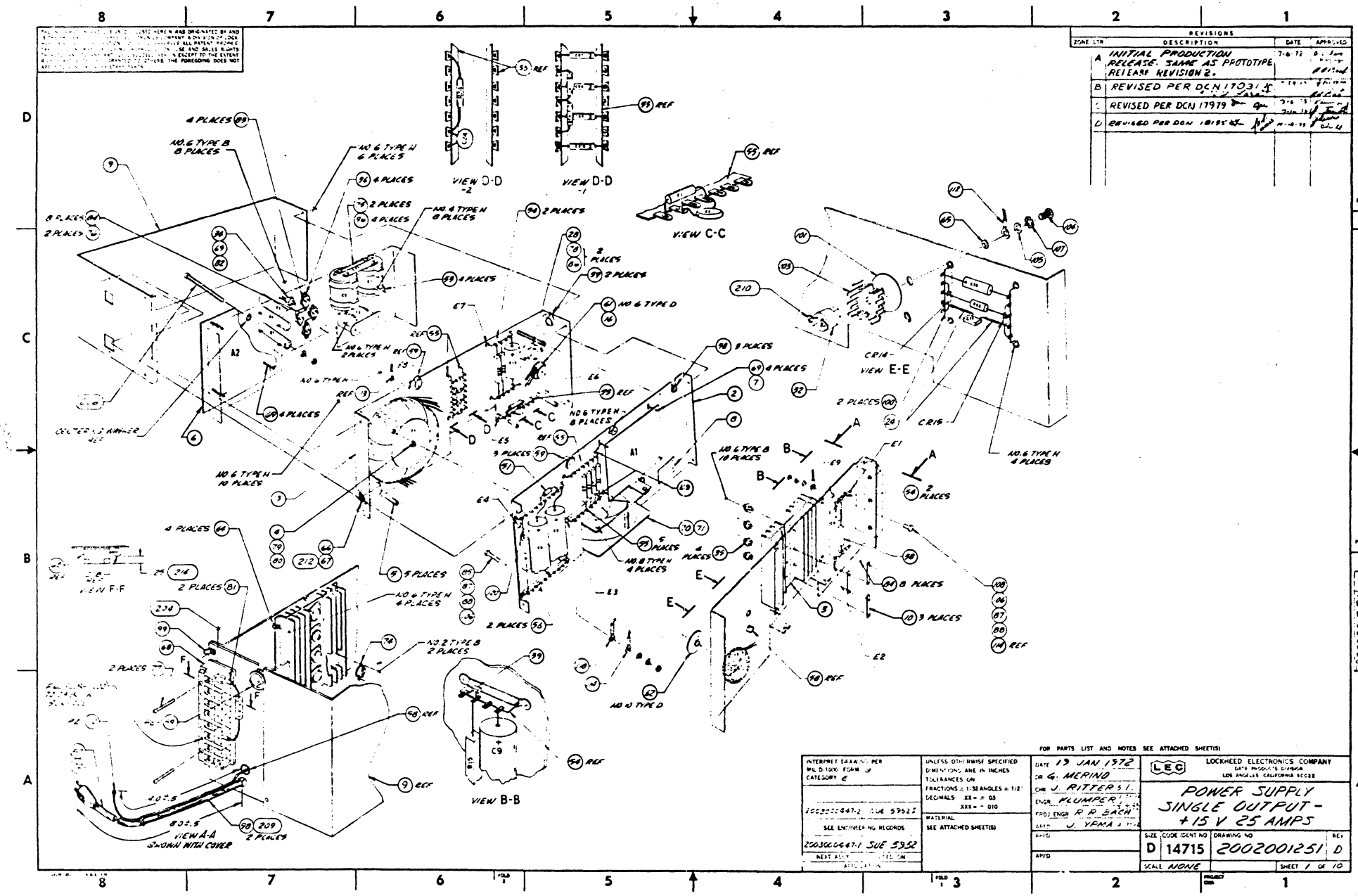
CONFORMS TO MIL-STD-100


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A INITIAL PRODUCTION RELEASE SAME AS PROTOTYPE REV 1
T01 8001400088
T02
T1 8001400081
L01 8001400085
(4x) 90 uH
CR01 MDA962-3
Q005 C38B
Q01 Q02 Q03 Q04
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11
Q101 Q102
A01 1RO +15V REGULATOR
U1 UA723
U1 SN75451P
U2 SN75451P
U3 SN7473N
U4 SN75451P
A02 CCA
P1-1 +15V 25A
P1-6 COMMON GND
P1-7 VTP
P1-3 LINE REG SIGNAL (LFRQ)
P1-2 LINE FAIL PULSE (PWST)
P2 J1 GRN GND
S1
F01 3AB 10A
R01 .25 25W
R02 2 25W
R03 1500 25W
R5 1500, 1W
C01 1150 200V
C02 1150 200V
C03 .27 600V
C04 .01 1KV
C15 2200 25V
C18 18 50V
C09 2200 25V
R15 50 10W
NOTES:
1. UNLESS OTHERWISE SPECIFIED
- RESISTANCE VALUES ARE IN OHMS, 1/4W.
- CAPACITANCE VALUES ARE IN MICROFARADS.
INTERPRET DRAWING PER MIL-D-1000, FORM 3, CATEGORY E
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± 1/32 ANGLES ± 1/2° DECIMALS .XX = ± .03 .XXX = ± .010
MATERIAL SEE ATTACHED SHEET(S)
FOR PARTS LIST AND NOTES SEE ATTACHED SHEET(S)
SEE ENGINEERING RECORDS
2003000447 SUE 5952
NEXT ASSY USED ON
APPLICATION
DATE 13 JAN 1972
DR
CHK
ENGR
PROJ ENGR
APPD
APPD
APPD
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA
SCHEMATIC DIAGRAM
SUE
SINGLE OUTPUT P/S
SIZE F
CODE IDENT NO 14715
DRAWING NO SD200200125
REV A
SCALE —
SHEET 1 OF 1

PS2


REVISIONS
ZONE LTR | DESCRIPTION | DATE | APPROVED
A INITIAL PRODUCTION RELEASE. SAME AS PROTOTYPE RELEASE REVISION 2. 7-6-72
B REVISED PER DCN 17031
C REVISED PER DCN 17979
D REVISED PER DCN 18195
VIEW D-D -2
VIEW D-D -1
VIEW C-C
VIEW E-E
VIEW F-F
VIEW B-B
VIEW A-A SHOWN WITH COVER
4 PLACES
NO. 6 TYPE B 8 PLACES
NO. 6 TYPE H 6 PLACES
NO. 6 TYPE H 8 PLACES
NO. 6 TYPE H 10 PLACES
NO. 6 TYPE D
NO. 6 TYPE H 4 PLACES
NO. 8 TYPE H 4 PLACES
NO. 2 TYPE B 2 PLACES
NO. 4 TYPE D
2 PLACES
3 PLACES
5 PLACES
8 PLACES
9 PLACES
10 PLACES
A1
A2
C9
CR14
CR15
FOR PARTS LIST AND NOTES SEE ATTACHED SHEET(S)
INTERPRET DRAWING PER MIL-D-1000 FORM 3 CATEGORY E
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± 1/32 ANGLES ± 1/2° DECIMALS .XX ± .03 .XXX ± .010
MATERIAL SEE ATTACHED SHEET(S)
SEE ENGINEERING RECORDS
NEXT ASSY
DATE 13 JAN 1972
DR G. MERINO
CHK J. RITTER
ENGR PLUMPER
PROJ ENGR R. R. BACH
APVD J. YAMA
APVD
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90028
POWER SUPPLY
SINGLE OUTPUT - +15 V 25 AMPS
SIZE D
CODE IDENT NO 14715
DRAWING NO 2002001251
REV D
SCALE NONE
SHEET 1 OF 10
2002001251

PS2

JNH

PREPARED R. RODGERS	DATE 1/26/72	LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022	B 14715 PL 2002001251-1 C
CHK [signature]	DATE 3-7-72		
ENGR [signature]	DATE 3-7-72		
PROJ ENGR [signature]	DATE 3-7-72		SIZE CODE IDENT SHEET 2 REV

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2002001251-1		ASSEMBLY		SUE 5952	1
002		001	0001		1001004755-1		PLATE, LEFT SIDE			2
003		001	0001		1001004756-1		HEAT SINK			3
004		001	0001		1001004508-1		WASHER, RETAINING			4
005	F	005	0001		1005000793-1		STANDOFF			5
006		001	0001		2001002156-1		CCA-CKT CARD ASS		A2 NOTE 216	6
007		001	0001		2001002157-3		IRO-CKT CARD ASS		A1 NOTE 216	7
008		001	0001		1005000777-1		NAMEPLATE		NOTE 202	8
009		001	0001		1001004769-1		COVER			9
010		003	0001		1001004866-1		BUS BAR			10
011	E	001	0001		8001400088		TRANSFORMER, POWER		T1	11
012		001	0001		P6375	80089	TRANSFORMER	CHICAGO STANCOR	T2	12
013		001	0001		1001004754-3		PLATE, RIGHT SIDE			13
014	E	001	0001		8001400093		REACTOR		L3	14
015		000								15
016	E	001	0001		8001400085		REACTOR, INPUT BALUN		L1	16
017	B	004	0001		TYPE PW10-.1	75042	RESISTOR	IRC, INC	R6 THRU R9 PW10-.1 OHM10PCT	17
018	B	001	0001		TYPE 2D-2	75042	RESISTOR	IRC, INC	R2 2D-2 OHM 5PCT VERT MTG KIT NOTE 206	18
019	B	001	0001		TYPE 2D-.25	75042	RESISTOR	IRC, INC	R1 2D-.25 OHM10PCT VERT MTG KIT NOTE 206	19
020	B	001	0001		TYPE 2D-1500	75042	RESISTOR	IRC, INC	R3 2D-1500 OHM5PCT VERT MTG KIT NOTE 206	20
021		000								21
022		000								22
023	B	002	0001		TYPE PW10-.18	75042	RESISTOR	IRC, INC	R13,14 PW10-.18OHM10PCT	23
024		002	0001		20AWG WHT		TUBING (TEFLON)	MIL-1-22129	APPROX FT REQD	24
025		000								25
026		002	0001		S4M	14099	DIODE	SEMTECH	CR11,12	26
027		004	0001		1N4720	13327	DIODE	SOLITRON	CR7 THRU CR10	27
028		001	0001		MDA962-3	04713	FULL WAVE BRIDGE	MOTOROLA	CR1	28
029		002	0001		S2M	14099	DIODE	SEMTECH	CR14,15	29
030		000								30
031		000								31
032		001	0001		SCSPF2L	14099	RECTIFIER, ASSY	SEMTECH	CR13 NOTE 207	32
033		000								33

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES	DEFINITIONS	REVISIONS
A -- DENOTES SEPARATE PL B -- REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO C -- INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS E -- SOURCE CONTROL DWG F -- SPEC CONTROL DWG M -- DENOTES MAKE FROM & -- ALTERNATE SOURCE	IC P -- INTEGRATED CIRCUIT PKG I S -- INSERTION SPAN A/R -- AS REQD	FOR REV RECORD SEE SHEET 1

PS2

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	SHEET	REV
B	14715	PL 2002001251-1	C

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
034		001	0001		C38B	09214	SCR	GENERAL ELEC	Q5 NOTE 207	34
035		004	0001		2N5885	04713	TRANSISTOR	MOTOROLA	Q6 THRU Q9 NOTE 207	35
036		004	0001		DTS-430	16758	TRANSISTOR	DELCO RADIO	Q1 THRU Q4 NOTE 207	36
038	B	001	0001		TYPE PW22	75042	RESISTOR	IRC, INC	R17 PW22-25 OHM1OPCT	37
039	B	001	0001		TYPE PW10-50	75042	RESISTOR	IRC, INC	R15 PW10-50 OHM10PCT	38
040	F	001	0001		8001300101		CAPACITOR		C12	39
041		002	0001		71C200JB1151	99392	CAPACITOR	STM	C1,2	40
042		001	0001		DD1032	71690	CAPACITOR	CENTRALAB	C4	41
043		001	0001		ZD6A274	02980	CAPACITOR	ELPAC	C3	42
044		002	0001		8001300392-1		CAPACITOR		C18,23	43
045	F	001	0001		8001300102		CAPACITOR		C22	44
046		000								45
047		002	0001		39D228G025HP4	56289	CAPACITOR	SPRAGUE	C9,15	46
048		002	0001		39D238G050JT4	56289	CAPACITOR	SPRAGUE	C5,6	47
049		000								48
050		000								49
051		000								50
052		001	0001		RL32S471G		RESISTOR	MIL-R-22684/3	R22	51
053		001	0001		RL42S200G		RESISTOR	MIL-R-22684/4	R23	52
054		004	0001		6179-2A	91506	CLIP, COMPONENT	AUGAT	(C1,C2)	53
055		004	0001		326-20-04-001	71785	TERMINAL STRIP	CINCH	TB1,2,8,9	54
056		005	0001		326-20-07-001	71785	TERMINAL STRIP	CINCH	TB3,4,7,10,11	55
057		002	0001		326-20-10-001	71785	TERMINAL STRIP	CINCH	TB5,6	56
058		001	0001		SR-6P3-4	28520	BUSHING	HEYMAN MFG		57
059		004	0001		OCB-500	28520	BUSHING, OPEN/CLOSE	HEYMAN MFG		58
060		003	0001		OCB-875	28520	BUSHING, OPEN/CLOSE	HEYMAN MFG		59
061		001	0001		34306	00779	SPLICE	AMP, INC	16-14AWG APPROX QTY REQD	60
062		001	0001		100-5	08289	RETAINER, TOROID	DELBERT BLINN	(L1)	61
063		001	0001		100-6	08289	RETAINER, TOROID	DELBERT BLINN	(L3)	62
064		001	0001		NY25-030	08289	INSULATOR, NYLON	DELBERT BLINN		63
065		004	0001		304-025	08928	STANDOFF BUSHING	IERC		64
066		001	0001		2718-49550-N317	06540	WASHER, SHOULDER	AMATOM CO	NO. 5/16	65
067		001	0001		348875	75915	FUSE HOLDER	LITTELFUSE	XF1	66
068		001	0001		314010	75915	FUSE	LITTELFUSE	F1(3AB 10A 250V)	67
069		001	0001		11978-2	11873	DISCONNECT BLOCK	UNDERWRITERS SAFETY DEVICE CO	P1 (FEMALE)	68
070		008	0001		CBS-10N	06915	SUPPORT, CIRCUIT BD	BI MO PLASTIC		69
071		001	0001		10050000906-2		FAN		B1(95CFM, 115VAC)	70
072		001	0001		C-2055-215-P1	80126	LINE CORD, FAN	CASE ELECTRICORD CO	(P1)	71

CONFORMS TO MIL-STD-100

LECW 240 (JAN 70) K&E

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
073		001	0001		C1316-006-BL	80126	LINE CORD, AC	PACIFIC ELECTRICORD CO	6FT, 16/3	72
074		000								73
075	B	001	0001		TYPE A-672	93410	THERMOSTAT	ESSEX INTL INC	S1 A-672 CLOSE 190 DEG OPEN 165 DEG SEE NOTE 207	74
076		002	0001		1001004866-3		BUS BAR			75
077		002	0001		1001004866-2		BUS BAR			76
078		002	0001		MS51957-35	96906	SCREW, PAN HD		6-32 X 1.25 LG	77
079	F	002	0001		9002200653		SCREW, PAN HD		4-40 X 1.25 LG	78
080		001	0001		MS51957-54	96906	SCREW, PAN HD		8-32 X 2.25 LG	79
081		001	0001		22NM832	15653	NUT, LOCK	KAYNAR	8-32	80
082		002	0001		AA5191-08	98410	LUG	ETC, INC	APPROX QTY REQD	81
083		001	0001		DF6B	02735	INSULATOR, MICA	RCA	(Q5)	82
084		004	0001		495320	02735	INSULATOR, MICA	RCA	(Q1 THRU Q4)	83
085		016	0001		495334-7	02735	WASHER, NYLON	RCA	(Q1 THRU Q4, Q6 THRU Q9)	84
086		001	0001		MS90725-5	96906	SCREW, CAP, HEX HD		1/4-20 X .62 LG	85
087		002	0001		MS15795-804	96906	WASHER, FLAT		NO. 4	86
088		002	0001		MS35338-44	96906	WASHER, LOCK		NO. 1/4	87
089		002	0001		MS35649-2252	96906	NUT, HEX		1/4-20	88
090		002	0001		MS15795-805	96906	WASHER, FLAT		NO. 6	89
091	F	003	0001		9003400421-18		WIRE, STRANDED		14AWG WHT APPROX FT REQD	90
092	F	030	0001		9003400421-16		WIRE, STRANDED		16AWG WHT APPROX FT REQD	91
093	F	003	0001		9003400421-15		WIRE, STRANDED		16AWG BLK APPROX FT REQD	92
094	F	030	0001		9003400421-12		WIRE, STRANDED		20AWG WHT APPROX FT REQD NOTE 216	93
095		003	0001		AWG18 TYPE S		WIRE, SOLID, UNINSUL	QQ-W-343	18AWG APPROX FT REQD	94
096	F	003	0001		9003400419-9		WIRE, SOLID, UNINSUL		20AWG APPROX FT REQD	95
097		004	0001		MS35335-32	96906	WASHER, EXT TOOTH		NO. 10	96
098		A/R	0001		NO.340	71984	SILICONE HT SK CMPD	DOW CORNING	NOTE 207	97
099		002	0001		MS3367-5	96906	STRAP TIEDOWN		NOTE 209	98
100	E	001	0001		1005000787-22		TERMINAL, TAB		J1	99
101		002	0001		326-20-05-001	71785	TERMINAL STRIP	CINCH	TB12,13	100
102		001	0001		MW-1000-328-006	08289	WASHER, MICA	DELBERT BLINN	(CR13)	101
103		A/R	0001		K-22 BLACK	16245	CONAP EPOXY	CONAP INC		102
104		001	0001		UP-TE28-CP	98978	HEAT SINK	IERC	(CR13)	103
105		001	0001		MS90725-32	96906	SCREW, CAP HEX HD		5/16-18 X .62 LG	104
106		001	0001		MS27183-12	96906	WASHER, FLAT		NO. 5/16	105
107		002	0001		MS27183-10	96906	WASHER, FLAT		NO. 1/4	106

PS2

CONFORMS TO MIL-STD-100

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT		REV
B	14715	PL 2002001251-1	C

SHEET 5

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
108		001	0001		MS35335-34	96906	WASHER, LOCK		NO.5/16	107
109		001	0001		MS90725-4	96906	SCREW, CAP HEX		1/4-20 X .56 LG	108
110	E	003	0001		1005000785-14		LUG		16-24AWG NO. 10 NOTE 211 APPROX QTY REQD	109
111	E	002	0001		1005000787-3		TERMINAL RECPT		FASTON 250 16-14AWG NOTE 211 APPROX QTY REQD	110
112	E	001	0001		1005000785-20		LUG, RING		12-10AWG NO. 1/4 NOTE 211 APPROX QTY REQD	111
113		001	0001		MS25036-104	96906	LUG, RING		22-18AWG NO.5/16 NOTE 211 APPROX QTY REQD	112
114		001	0001		MS25036-102	96906	LUG, RING		22-18AWG NO. 6 NOTE 211 APPROX QTY REQD	113
115	E	003	0001		1005000785-15		LUG, RING		16-14AWG NO. 1/4 NOTE 211 APPROX QTY REQD	114
116	E	002	0001		1005000787-1		TERMINAL RECPT		FASTON 250 22-18AWG NOTE 211 APPROX QTY REQD	115
117		001	0001		MS25036-109	96906	LUG, RING		16-14AWG NO.5/16 NOTE 211 APPROX QTY REQD	116
118	E	001	0001		1005000785-9		LUG, RING		22-18AWG NO. 10 NOTE 211 APPROX QTY REQD	117
119	E	001	0001		1005000785-10		LUG, RING		22-18AWG NO. 1/4 NOTE 211 APPROX QTY REQD	118
120		REF	0001		SD2002001251-1		SCHEMATIC DIAGRAM			119
121		REF	0001		WL2002001251-1		WIRE LIST			120
122		REF	0001		AP2002001251-1		ACCEPTANCE TEST PROC			121
123		REF	0001		DS2002001251-1		DESIGN SPECIFICATION			122
124		A/R	0001		SN60/SN63		SOLDER	QQ-S-571	NOTE 216	123
125	E	004	0001		1005000785-12		LUG, RING		14-16AWG NO.6 NOTE 211	124
126	E	002	0001		1005000787-5		TERMINAL RECPT		FASTON 250 14-12AWG NOTE 211	125

CONFORMS TO MIL-STD-100

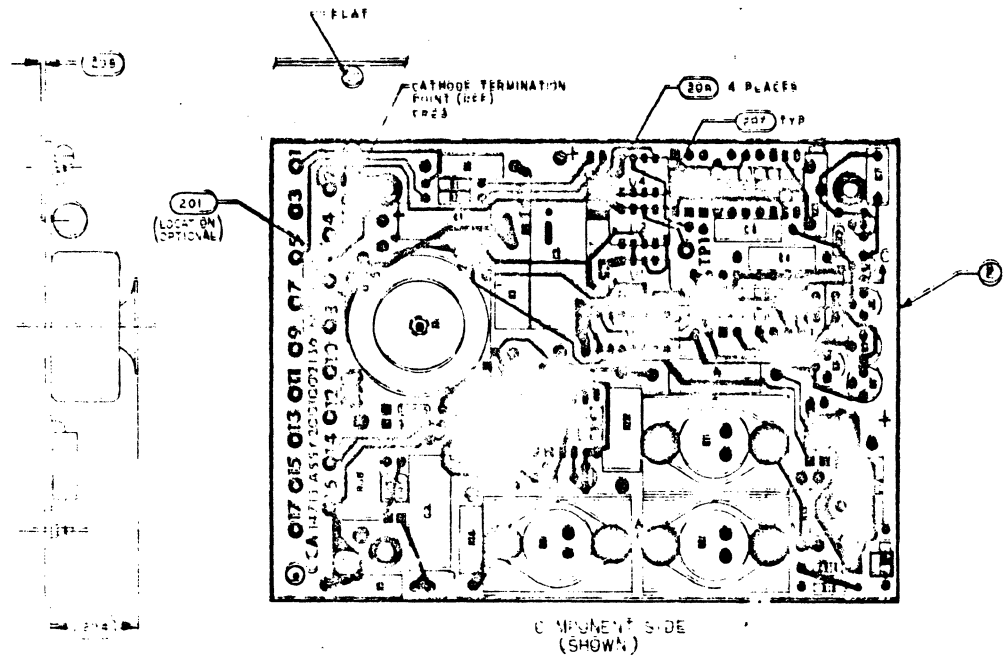
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

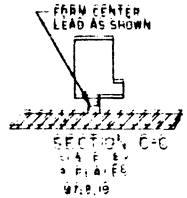
SIZE	CODE IDENT	SHEET	REV
B	14715	PL 2002001251	C
		10	

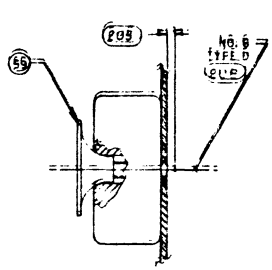
SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
	REF	0001		SPEC/DWG/STD		NOTES:			200
	REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			201
	A/R	0001		LECP1049-16		MARK FIND NUMBER 8 .09 HIGH CHARACTERS (TYPEWRITER MAY BE USED) AS FOLLOWS: TOP BLOCK: UNIT TITLE 2ND BLOCK: PART NUMBER 3RD BLOCK: SERIAL NUMBER 4TH BLOCK: 200-240 VAC, 47-63HZ			202
	A/R	0001				REMOVE MOLDED PLUG FROM FIND NUMBER 72 AND REPLACE WITH FIND NUMBER 127.			203
	REF	0001				ALLOW .010 TO .040 GAP FOR CONNECTOR FLOAT ALIGNMENT.			204
	A/R	0001		LECP1075		MOUNTING			205
	REF	0001				INSTALL RI 2 HOUSING SCREW CENTERING WASHER, LOCK-WASHER AND NUT FROM VERTICAL MOUNTING KIT. DISCARD UNUSED HARDWARE.			206
	A/R	0001				MOUNT Q1 THRU Q9, CR2,5,13,S1 USING THERMAL COMPOUND FIND NUMBER 97.			207
	000								208
	REF	0001				INSTALL FIND NUMBER 98 TO ALLOW FOR ADJUSTMENT BETWEEN FIND NUMBER 72 AND GREEN WIRE.			209
	REF	0001				BEND LUGS 90 DEGREES, STARTING .12 FROM DIODE. CAUTION DO NOT FRACTURE INSULATION.			210
	REF	0001		WL2002001251-1,-2		SEE WIRE LIST FOR LOCATION.			211
	REF	0001				INSTALL FIND NUMBER 110 (TERMINAL) ON FIND NUMBER 66 (FUSE HOLDER) PRIOR TO INSTALLING FIND NUMBER 67 (FUSE) INTO FUSE HOLDER.			212
	000								213
	REF	0001				TO BE CLEAR OF ANY WIRING AND COMPONENTS.			214
	A/R	0001		LECP1049-16		MARK FIND NUMBER 8 .09 HIGH CHARACTERS (TYPEWRITER MAY BE USED) AS FOLLOWS: TOP BLOCK: UNIT TITLE 2ND BLOCK: PART NUMBER 3RD BLOCK: SERIAL NUMBER 4TH BLOCK: 200-240 VAC, 47-53HZ			215
	A/R	0001				INSTALL FIND NUMBER 93 ON FIND NUMBERS 6 AND 7 BY INSERTING IN .060 DIAMETER HOLE AND SOLDERING WITH FIND NUMBER 123.			216

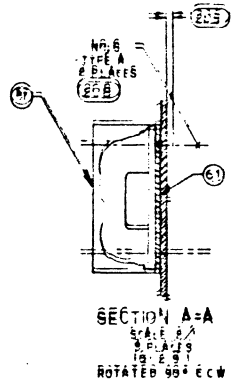
PS2

CONFORMS TO MIL-STD-100









200200251-1 SUE5952		LEE	CIRCUIT CARD ASSEMBLY CCA CONVERTER & CONTROL
200200251-1 SUE5952		SIZE D	CODE IDENT NO 14715
		DWG NO 2001002156	

PS2

MAB

PREPARED M. GLEIXNER DATE 8-30-7
CHK DATE 9-8-72
ENGR DATE
PROJ ENGR DATE 9-8-72

LEC
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

B	14715	PL 2001002156-1	D
SIZE	CODE IDENT	SHEET 2	REV

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2001002156-1		CCA-CKT CARD ASSY		USED ON SUE 5950,5951,5952, 5953	1
002	001	0001		1001004757-1		PRINTED WRG BD, CCA			2
003 F	001	0001		8001800098-1		ICP		U3 (7473)	3
004	003	0001		SN75451P	01295	ICP	TEXAS INSTR INC	U1,2,4	4
005	001	0001		PW2-4 OHMS	75042	RESISTOR	IRC, INC	R3 1.10 IS	5
006	001	0001		8001300314-1		CAPACITOR		C1 1.10 IS	6
007	001	0001		MTA50E25	90201	CAPACITOR	MALLORY CAP. CO	C2 1.25 IS	7
008	001	0001		MTA80F50	90201	CAPACITOR	MALLORY CAP. CO	C3 1.70 IS	8
009	001	0001		RL42S271G		RESISTOR	MIL-R-22684/4	R38 1.0 IS	9
010	002	0001		192P15392	56289	CAPACITOR	SPRAGUE ELEC	C4,6 .80 IS	10
011	001	0001		8001300311-2		CAPACITOR		C12 .80 IS	11
012	001	0001		1N5160		DIODE		CR25 .5 IS	12
013 F	002	0001		8001300017-1		CAPACITOR		C5,14 .20 IS	13
014 F	002	0001		8001300101-1		CAPACITOR		C9,10 .25 IS	14
015 F	001	0001		8001300102-1		CAPACITOR		C7 .375 IS	15
016	001	0001		1N4734		DIODE, ZENER		CR13 .5 IS	16
017 E	001	0001		8001400081-1		TRANSFORMER		T1	17
018 E	004	0001		8001200001-1		TRANSISTOR		Q3,4,5,6 (TO18)	18
019	002	0001		2N3054		TRANSISTOR		Q1,9 (TO66)	19
020	001	0001		2N4898		TRANSISTOR		Q2 (TO66)	20
021	001	0001		2N5060		SCR		Q11 (TO18)	21
022	003	0001		2N5354		TRANSISTOR		Q7,8,10 (TO18)	22
023	002	0001		S2F	14099	DIODE	SEMTECH	CR10,11 .5 IS	23
024	001	0001		1N751A		DIODE, ZENER		CR24 .5 IS	24
025	001	0001		1N752A		DIODE, ZENER		CR22 .5 IS	25
026	001	0001		1N758A		DIODE, ZENER		CR16 .5 IS	26
027	005	0001		1N4002		DIODE		CR12,18,19,20,21 .5 IS	27
028	003	0001		1N4735		DIODE, ZENER		CR7,8,9 .5 IS	28
029 E	006	0001		8001100001-1		DIODE		CR4,5,6,14,15,17 .5 IS	29
030 E	001	0001		1005000837-1		DIODE		CR23	30
031	001	0001		RL07S471G		RESISTOR	MIL-R-22684/1	R33 .5 IS	31
032	001	0001		3007P-1-103	80294	RESISTOR, POT.	BOURNS, INC	R35	32
033	001	0001		PW3-2 OHMS	75042	RESISTOR	IRC, INC	R7 1.10 IS	33
034 B	001	0001		TYPE RLS-1A	91637	RESISTOR	DALE ELEC INC	R18 .425 IS RLS-1A,1.5K OHMS 3 PERCENT, 1W	34

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES

A — DENOTES SEPARATE PL
B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO
C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS
E — SOURCE CONTROL DWG
F — SPEC CONTROL DWG
M — DENOTES MAKE FROM
& — ALTERNATE SOURCE

DEFINITIONS

IC P — INTEGRATED CIRCUIT PKG
I S — INSERTION SPAN
A/R — AS REQD

REVISIONS

FOR REV RECORD SEE SHEET 1

LECW 239 (JAN 70) K&E

PS2

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	PL	REV
B	14715	2001002156-1	D

SHEET 3

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
035		001	0001		RL42S241G		RESISTOR	MIL-R-22684/4	R28 1.0 IS	35
036		001	0001		RL32S102G		RESISTOR	MIL-R-22684/3	R6 .8 IS	36
037		001	0001		RL32S120G		RESISTOR	MIL-R-22684/3	R11 .8 IS	37
038		001	0001		RL32S152G		RESISTOR	MIL-R-22684/3	R5 .8 IS	38
039		001	0001		RL32S271G		RESISTOR	MIL-R-22684/3	R36 .8 IS	39
040		002	0001		RL20S120G		RESISTOR	MIL-R-22684/2	R8,35 .6 IS	40
041		005	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R4,12,13,16,21 .5 IS	41
042		002	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R9,10 .5 IS	42
043		002	0001		RL07S512G		RESISTOR	MIL-R-22684/1	R14,15 .5 IS	43
044		001	0001		RL07S103G		RESISTOR	MIL-R-22684/1	R17 .5 IS	44
045		002	0001		RL07S152G		RESISTOR	MIL-R-22684/1	R30,31 .5 IS	45
046		001	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R26 .5 IS	46
047		002	0001		RL07S330G		RESISTOR	MIL-R-22684/1	R22,23 .5 IS	47
048		001	0001		RL07S153G		RESISTOR	MIL-R-22684/1	R24 .5 IS	48
049		001	0001		RL07S621G		RESISTOR	MIL-R-22684/1	R27 .5 IS	49
050		001	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R29 .5 IS	50
051		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R32 .5 IS	51
052		001	0001		RL07S202G		RESISTOR	MIL-R-22684/1	R20 .5 IS	52
053		001	0001		RL07S272G		RESISTOR	MIL-R-22684/1	R37 .5 IS	53
054		001	0001		RL07S[illegible]1G		RESISTOR	MIL-R-22684/1	R34 .5 IS	54
055		002	0001		RL07S100G		RESISTOR	MIL-R-22684/1	R1,2 .5 IS	55
056		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		56
057		003	0001		6166R-BASE	13103	HEAT SINKS	THERMALLOY CO	(TO66)	57
058		000								58
059		001	0001		100-5	08289	RETAINER, TOROID	DELBERT BLINN		59
060		REF	0001		SD2003000430-1		SCHEMATIC DIAGRAM			60
061		003	0001		DF31A[illegible]	02735	INSULATOR, MICA	RCA	MAY BE FURNISHED WITH Q1,2,9	61
062		REF	0001		SD2003000430-2		SCHEMATIC DIAGRAM			62

CONFORMS TO MIL-STD-100

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

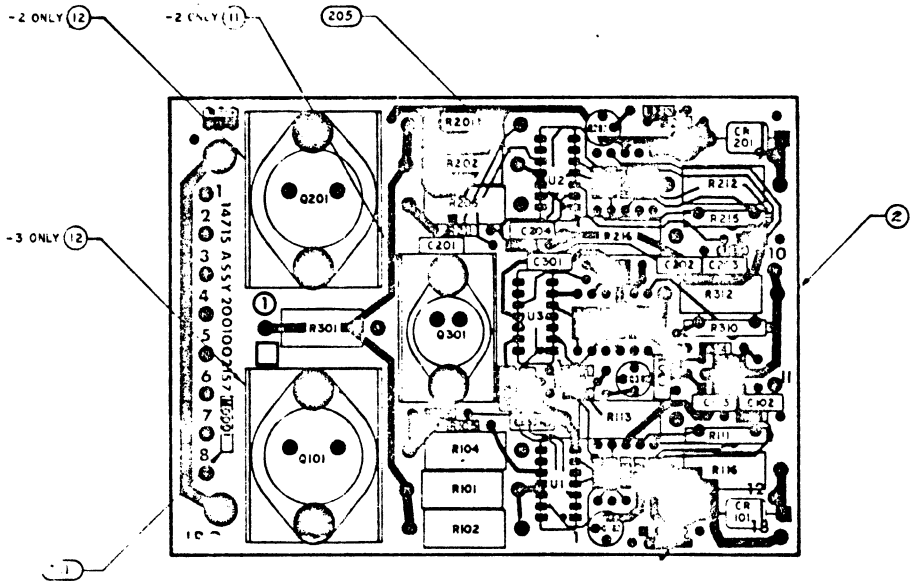
SIZE	CODE IDENT		REV
B	14715	PL 2001002156	D
		SHEET 6	

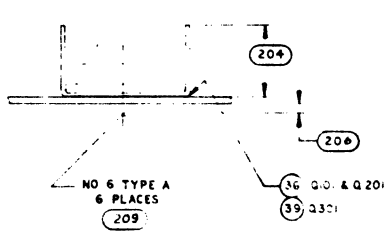
SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200	REF	0001		SPEC/DWG/STD		NOTES:			200
201	REF	0001		LECP1049-17		MARKING.			201
202	REF	0001				PRINTED WIRE CIRCUITRY SHOWN IS PHYSICALLY ON COMPONENT SIDE.			202
203	REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			203
204	REF	0001				COMPONENT HEIGHT .XXX MAX.			204
205	REF	0001				LEAD PROTRUSION (SIDE 2) .075 MAX. HARDWARE PROTRUSION .160 MAX.			205
206	REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			206
207	REF	0001				SQUARE PAD AND/OR DOT DENOTES CATHODE END OF DIODE.			207
208	A/R	0001		LECP1075		HARDWARE.			208

CONFORMS TO MIL-STD-100

LECW 240 (JAN 70) K&E

PS2





ZONE LTR	DESCRIPTION	DATE	APPROVE

FOR PARTS LIST AND NOTES SEE ATTACHED SHEETS

INTERPRET DRAWING PER MIL-STD-100 FORM 3 CATEGORY E	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS ± 1/32 ANGLES ± 1/2° DECIMALS .XX = ± .03 .XXX = ± .010	DATE 8 JUNE 71 DR C.J. Barrio CHK ENGR PROJ ENGR APPD APPD APPD	LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022
SEE ENGINEERING RECORDS SUE 5950 NEXT ASSY USED ON APPLICATION	MATERIAL SEE ATTACHED SHEET(S)		CIRCUIT CARD ASSEMBLY IRO INVERTER REGULATOR OUTPUT
			SIZE D CAGE IDENT NO 14715 DRAWING NO 2001002157 REV E
			SCALE 2/1 SHEET 1 OF 5

2001002157

PS2

MAB

PREPARED J. JEPSEN DATE 8-25-71
CHK G. Ritter DATE 3-8-72
ENGR [illegible] DATE 3-10-72
PROJ ENGR A.A. Bach DATE 3-10-72

LEC
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

B	14715	PL 2001002157-2	B
SIZE	CODE IDENT	SHEET 4	REV

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2001002157-2		IRO-CKT CARD ASSY		USED ON SUE 5952/5953	1
002	001	0001		1001004758-2		PRINTED WRG BD, IRO			2
003	001	0001		1N4720	13327	DIODE	SOLITRON	CR201 .625 IS	3
004	001	0001		1N756A		DIODE, ZENER		CR301 .5 IS	4
005	001	0001		1N752A		DIODE, ZENER		CR202 .5 IS	5
006	001	0001		1N757A		DIODE, ZENER		CR302 .5 IS	6
007	001	0001		CM05D471J03		CAPACITOR	MIL-C-5/18	C202 .25 IS	7
008 E	002	0001		8001200001-1		TRANSISTOR		Q202,302 (TO-18)	8
009	001	0001		MJ3000	04713	TRANSISTOR	MOTOROLA	Q201 (TO-3)	9
010	001	0001		2N3054		TRANSISTOR		Q301 (TO-66)	10
011	001	0001		6166B-BASE	13103	HEAT SINK	THERMALLOY	(TO-66)	11
012	001	0001		6103B-BASE	13103	HEAT SINK	THERMALLOY	(TO-3)	12
013 E	003	0001		8001300101-1		CAPACITOR		C201,204,301 .25 IS	13
014	001	0001		CM05FD101J03		CAPACITOR	MIL-C-5/18	C302 .25 IS	14
015	002	0001		3007P-1-102	80294	RESISTOR, VARIABLE	BOURNS, INC	R215,310	15
016	002	0001		CM05FD331J03		CAPACITOR	MIL-C-5/18	C203,303 .25 IS	16
017	002	0001		U6A7723393	07263	ICP	FAIRCHILD	U2,3	17
018	001	0001		RL07S202G		RESISTOR	MIL-R-22684/1	R302 .5 IS	18
019	004	0001		RL07S821G		RESISTOR	MIL-R-22684/1	R303,305,207,205 .5 IS	19
020	002	0001		RL07S302G		RESISTOR	MIL-R-22684/1	R308,311 .5 IS	20
021	005	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R209,213,313, 314,315 .5 IS	21
022	001	0001		RL07S332G		RESISTOR	MIL-R-22684/1	R309 .5 IS	22
023	001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R210 .5 IS	23
024	001	0001		RL07S681G		RESISTOR	MIL-R-22684/1	R211 .5 IS	24
025	001	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R214 .5 IS	25
026	001	0001		RL07S271G		RESISTOR	MIL-R-22684/1	R304 .5 IS	26
027	001	0001		RL07S361G		RESISTOR	MIL-R-22684/1	R307 .5 IS	27
028	001	0001		RL07S391G		RESISTOR	MIL-R-22684/1	R203 .5 IS	28
029	001	0001		RL07S222G		RESISTOR	MIL-R-22684/1	R204 .5 IS	29
030	001	0001		RL42S181G		RESISTOR	MIL-R-22684/4	R312 1.0 IS	30
031	002	0001		RL42S681G		RESISTOR	MIL-R-22684/4	R201,202 1.0 IS	31
032	001	0001		RL42S131G		RESISTOR	MIL-R-22684/4	R206 1.0 IS	32
033	001	0001		RL42S332G		RESISTOR	MIL-R-22684/4	R301 1.0 IS	33
034	002	0001		RL07S510G		RESISTOR	MIL-R-22684/1	R208,306 .5 IS	34
035	000								35

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL	E — SOURCE CONTROL DWG	IC P — INTEGRATED CIRCUIT PKG	FOR REV RECORD SEE SHEET 1
B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO	F — SPEC CONTROL DWG	I S — INSERTION SPAN	
C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	M — DENOTES MAKE FROM	A/R — AS REQD	
	& — ALTERNATE SOURCE		

LECW 239 (JAN 70) K&E

PS2

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT		REV
B	14715	PL 2001002157-2	B
		SHEET 5	

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
036	001	0001		495320	02735	INSULATOR, MICA	RCA	MAY BE FURNISHED WITH Q201	36
037	A/R	0001		SN60/SN63		SOLDER	QQ-S-571		37
038	REF	0001		SD2002001206-1		SCHEMATIC DIAGRAM			38
039	001	0001		DF31A	02735	INSULATOR, MICA	RCA	MAY BE FURNISHED WITH Q301	39

CONFORMS TO MIL-STD-100

MAB

PREPARED J. JEPSEN DATE 8-25-7	LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022	B 14715	PL 2001002157-3 B
CHK J. Ritter DATE 9-10-72			
ENGR K Lemm DATE 9-10-72		SIZE CODE IDENT	SHEET 6 REV
PROJ ENGR R.A. Back DATE 9-10-72			

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002157-3		IRO-CKT CARD ASSY		USED ON SUE 5952/5953	1
002		001	0001		1001004758-2		PRINTED WRG BD, IRO			2
003		001	0001		1N4720	13327	DIODE	SOLITRON	CR101 .625 IS	3
004		001	0001		1N756A		DIODE, ZENER		CR102 .5 IS	4
005		000								5
006		001	0001		1N757A		DIODE, ZENER		CR103 .5 IS	6
007		001	0001		2N5885	04713	TRANSISTOR	MOTOROLA	Q101 (TO-3)	7
008	E	001	0001		8001200001 -1		TRANSISTOR		Q102 (TO-18)	8
009		000								9
010		000								10
011		000								11
012		001	0001		6103R-BASE	13103	HEAT SINK	THERMALLOY	(TO-3)	12
013	E	002	0001		8001300101 -1		CAPACITOR		C101,104 .25 IS	13
014		001	0001		CM05FD101J03		CAPACITOR	MIL-C-5/18	C102 .25 IS	14
015		001	0001		3007P-1-102	80294	RESISTOR, VARIABLE	BOURNS, INC	R111	15
016		001	0001		CM05FD331J03		CAPACITOR	MIL-C-5/18	C103 .25 IS	16
017		001	0001		U6A7723393	07263	ICP	FAIRCHILD	U1	17
018		001	0001		RL07S202G		RESISTOR	MIL-R-22684/1	R103 .5 IS	18
019		002	0001		RL07S821G		RESISTOR	MIL-R-22684/1	R105,109 .5 IS	19
020		002	0001		RL07S302G		RESISTOR	MIL-R-22684/1	R108,112 .5 IS	20
021		003	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R107,114,115 .5 IS	21
022		001	0001		RL07S332G		RESISTOR	MIL-R-22684/1	R110 .5 IS	22
023		000								23
024		001	0001		RL07S510G		RESISTOR	MIL-R-22684/1	R106 .5 IS	24
025		000								25
026		000								26
027		000								27
028		000								28
029		000								29
030		001	0001		RL42S101G		RESISTOR	MIL-R-22684/4	R104 1.0 IS	30
031		001	0001		RL42S181G		RESISTOR	MIL-R-22684/4	R101 1.0 IS	31
032		000								32
033		000								33
034		000								34
035		000								35

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL	E — SOURCE CONTROL DWG	IC P — INTEGRATED CIRCUIT PKG	FOR REV RECORD SEE SHEET 1
B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO	F — SPEC CONTROL DWG	I S — INSERTION SPAN	
C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	M — DENOTES MAKE FROM	A/R — AS REQD	
	& — ALTERNATE SOURCE		

LECW 239 (JAN 70) K&E

PS2

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT		REV
B	14715	PL 2001002157-3	B
		SHEET 7	

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
036	001	0001		495320	02735	INSULATOR, MICA	RCA	MAY BE FURNISHED WITH Q101	36
037	A/R	0001		SN60/SN63		SOLDER	QQ-S-571		37
038	REF	0001		SD2002001207-1		SCHEMATIC DIAGRAM			38

CONFORMS TO MIL-STD-100

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	SHEET	REV
B	14715	PL2001002157	B

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTES:			200
201		A/R	0001		LECP1049-17		MARKING.			201
202		REF	0001				PRINTED CIRCUITRY SHOWN IS PHYSICALLY ON COMPONENT SIDE.			202
203		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATION.			203
204		REF	0001				COMPONENT HEIGHT .70 MAX.			204
205		REF	0001				SQUARE PAD AND/OR DOT DENOTES PIN 1 OF ICP.			205
206		REF	0001				LEAD PROTRUSION (SIDE 2) .075 MAX. HARDWARE PROTRUSION .160 MAX.			206
207		REF	0001				SQUARE PAD AND/OR STRIPE DENOTES CATHODE END OF DIODE.			207
208		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING, FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209		A/R	0001		LECP1075		HARDWARE.			209

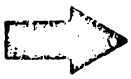
PS2

CONFORMS TO MIL-STD-100

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

PS2



SEE PS2-Ø2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/5/75 H

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

PS2 SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		PS2-2Ø

SCALE	REV	SHEET 1 OF 1

Network Reload

RLD-Ø2 Logic Description

RLD-Ø5 Technical Reference

RLD-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	REL FOR PROD	1/21/76	
B	ECN 0216	7/21/76	

RLD

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:	
DRAFTSMAN	
CHECKER	
ENGINEER	
APP'D FOR REL	
APP'D (CUSTOMER)	

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

RLD - LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		RLD-Ø2

SCALE	REV	SHEET
	B	1 OF 8

RLD LOGIC DESCRIPTION

The Modem Reload Device (RLD) is a single card module containing eight front end activators, priority arbitration, finite state machine, data registers, and bus master logic to perform the functions outlined in the RLD functional specification. This document is a detailed description of the implemented logic. In general, signals signed "+" are true when at a TTL high level, while signals signed "-" are true when at a TTL low level.

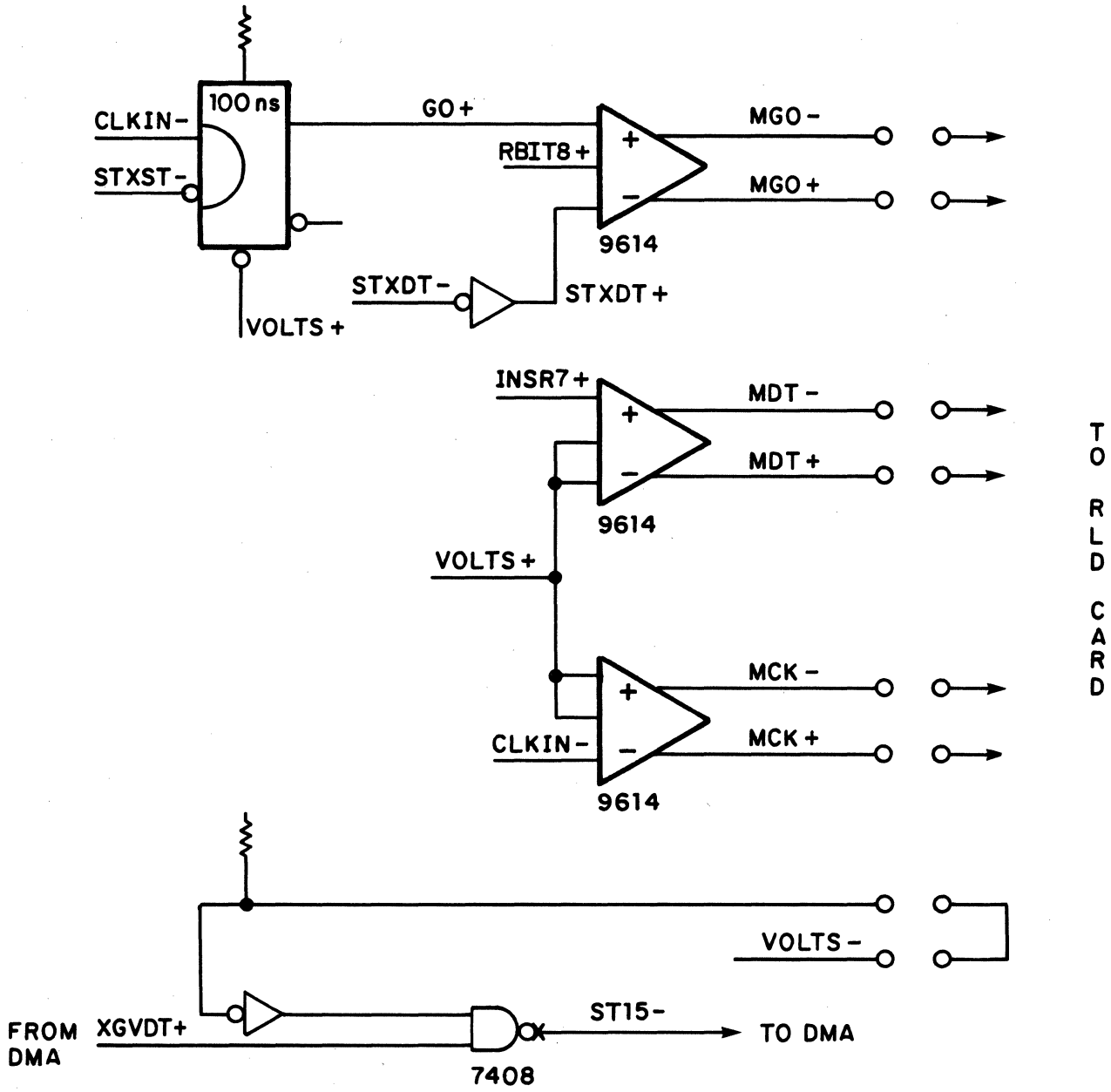
Line Activators (RLD20)

Each of the eight individual activation circuits is connected to the received data stream of its respective modem interface by three differentially driven signals. The modem clock signal (MCKXX) is the inverse of the received modem clock, while the data (MDTXX) is the received data as sampled and shifted once in the modem interface. Therefore, both signals have the same relationship as those at the input to the modem interface,* but the clock trails the received signal by half a clock cycle and the data trails by one and a half clock cycles. Note the inverted sense of MCKXX at the receiver input. The third signal (MGOXX) is a 100 ns pulse derived from the modem interface receive finite state machine to indicate the last bit of the STX framing character just prior to the start of a packet. It is legislated that for a reload packet the very next bit, the first bit of data, will be a 1 (see Figure 1).

Each of the differential signals is true when the "+" side is more positive than the "-" side. Each side is a TTL signal with typical TTL levels, but each pair is terminated in a 120 Ω resistor internal to the 9615 receiver.

The assertion of MGOXX direct sets LOOKX. On the next rising edge of MCKXX, the first data bit will be present at MDTXX. If none of the ACTXX flops are set (SELGO will be false) and the data bit is a 1 (MDTXX is true), GACTX will be true. Therefore, ACTXX will be set on the rising edge of CLKXX, and regardless of the data, LOOKX will be cleared. Now, since ACTXX is true, GACTX will be held true, preventing CLKXX from clearing

*Data changes on the falling clock edge and is sampled on the rising clock edge.



MGO+ = START OF PACKET
INSR7+ = MODEM RECEIVE DATA, HIGH = 1
CLRIN- = MODEM RECEIVE CLOCK, ↑ = DATA GOOD

Figure 1 Suggested Modem Circuit

ACTXX. The eventual occurrence of SELND (see below) will clear ACTXX and allow future activators.

Line Select and Control (RLD21)

When any of the ACTXX signals becomes true, the 9318 "GS" signal, which is an OR of the eight inputs, becomes true, and the octal number of the highest priority true input will appear at ADD00, ADD01 and ADD02. Therefore, when any input becomes activated SELGO goes true. As a result, SLDLY (200 ns) fires and on its trailing edge SELCT is set. The assertion of SELGO blocks activation of any further inputs, and the 200 ns delay allows the activators and priority tree to settle. Should a marginal timing situation develop, such that the ACTXX line is no longer true following the 200 ns delay, SELGO will be false and SELCT will not be set. When SELCT becomes true, the 74151 selectors are enabled to choose the clock and data inputs indicated by ADD01, ADD02 and ADD03 to correspond to the selected input. The remainder of the control logic is now independent of any specific modem interface input.

Two clock signals are derived from CLKGO. The first, CKCLK, follows the CLKGO pulse corresponding to the first of each pair of doubled data bits, while the other, DTCLK, follows CLKGO during the second of the pair (see Figure 2).

The 74161 state counter (see Figure 3) begins in the 0 state and SERCH is true. When SELCT comes true, CLKGO comes true, causing CKCLK to come true during the initial data bit equal to 1. Since STDTA is therefore true, INITP will be true during CKCLK, direct clearing ERRFF and CKDTA. At the same time, the rise of SELCT fires WDTOK (1 second). Since SELCT and SERCH are true, COUNT will be true.

On the fall of CKCLK, the state counter is incremented. On all odd counts, SHDTA will be true, and on all even counts, except zero when SERCH will be true, SHCKR will be true -- the data and checksum states respectively. When the counter reaches 15, CARRY comes true and the next fall of CKCLK sets the counter to 1.

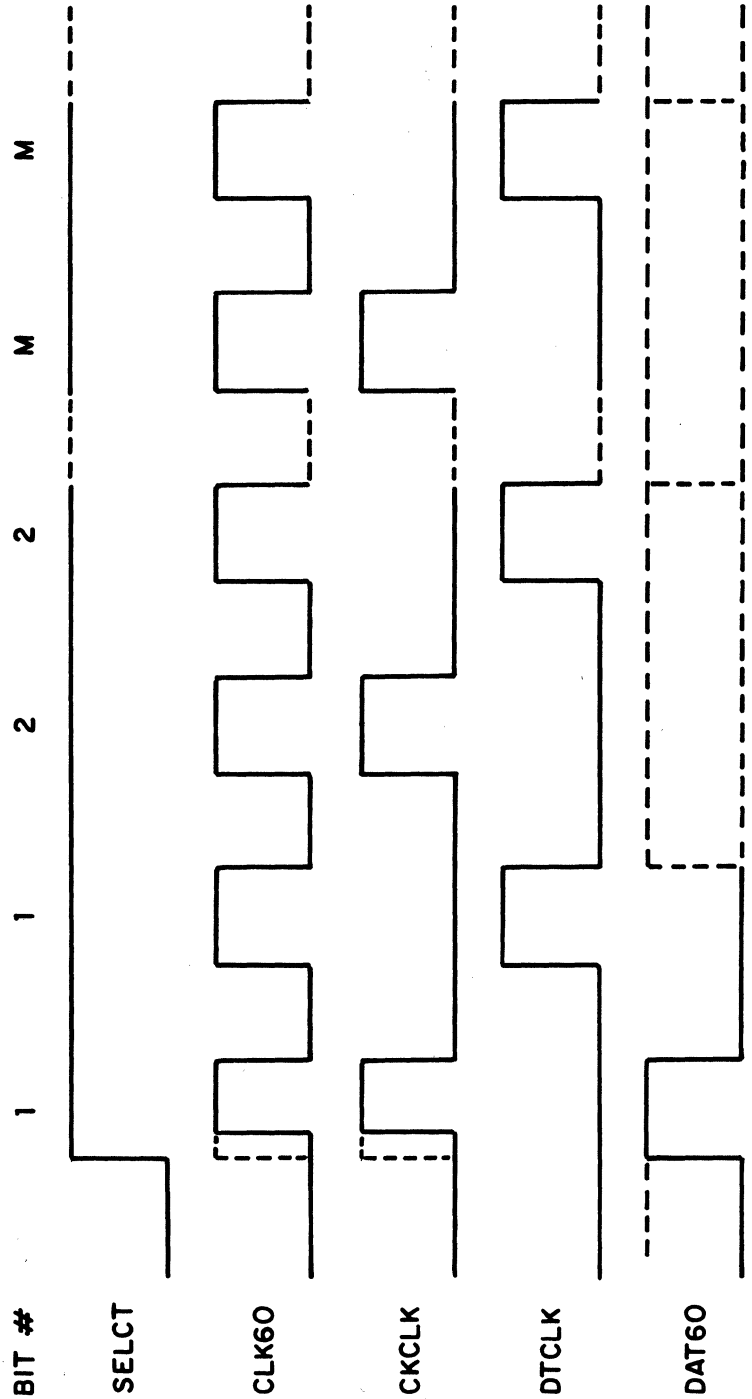
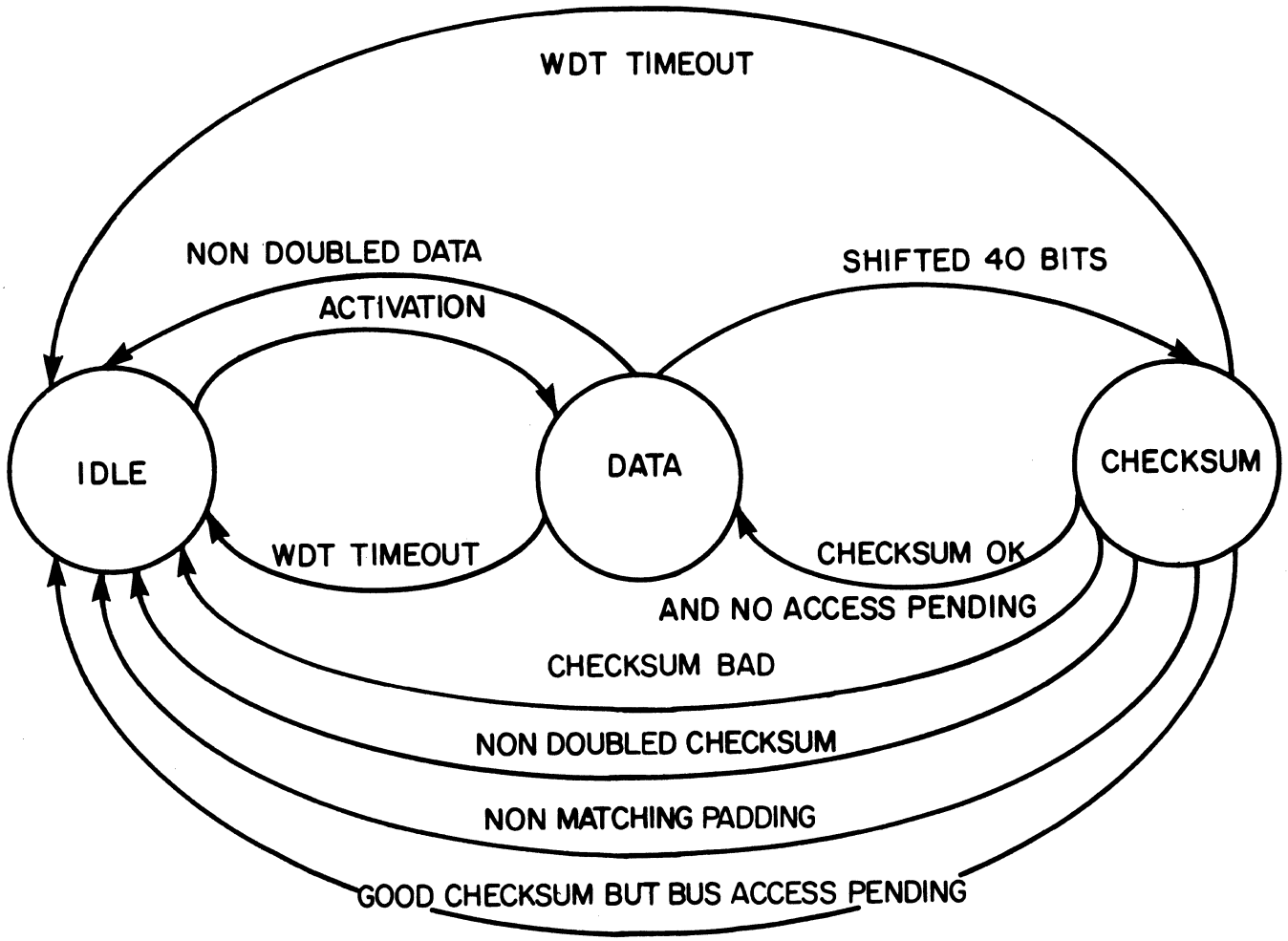


Figure 2 Clock Signals



RLD

Figure 3 RLD Finite State Machine

Reload Command Format

D	S	1	A	A	A	A	1	D	D	D	D	C	C	C	C	A			C	D	E
		A	D	D	D	D		A	A	A	A	H	H	H	H	D			H		
		D	D	D	D	D		T	T	T	T	E	E	E	E	D			E		
		D	R	R	R	R	1	A	A	A	A	C	C	C	C	R			C		
L	T	R	E	E	E	E						S	S	S	S	E	.	.	S	L	T
		E	S	S	S	S						U	U	U	U	S			U		
		S	S	S	S	S	1					M	M	M	M	S			M		
		S																			
		0	4	8	12	16		0	4	8	12	0	4	8	12	0			12		
E	X	3	7	11	15	19	1	3	7	11	15	3	7	11	15	3			15	E	X

Low order address bit is constrained to be 0.

Each time CKCLK comes true, DATGO is sampled into CKDTA. If the XOR of CKDTA and DATGO is true (the data stream was not doubled), ERRFF will be set on the leading edge of DTCLK. This is true of the 16 data bits, 20 address bits, 4 padding bits, and 16 checksum bits. However, at the conclusion of shifting the data, address and padding bits, GOSUM comes true, asserting COUNT. On the next fall of CKCLK, the state counter steps to assert SHCKR. While SHCKR is true, each falling edge of CKCLK steps a 4-bit counter after each checksum bit is shifted. Following the 15th bit, DONEX will be true, and the next falling edge of CKCLK will step the state counter back to the data state. At that point, STDAT will be true and the presence of CKCLK will assert RGCLR to clear the clock register.

There are, however, two error conditions possible while SHCKR is true, both sampled on the leading edge of DTCLK. First, if all 4 padding bits do not agree with the jumper selections on the card, BADPD will come true. Similarly, if the checksum does not agree with the data stream, FBTAP will come true, causing BADCK.

CMDAX is normally set while STDAT is true on the falling edge of DTCLK (the checksum has been received correctly). This flop requests a bus access for a properly received data and address stream. It is cleared by BENDX from the DBAL to indicate completion of the bus cycle. However, if a bus access was previously requested and has not yet been honored, CMDAX will still be true, since it is never cleared by DTCLK once it is set. The rise of CKCLK samples CMDAX into CMDAS and if the latter is still true while STDAT is true, the rise of DTCLK will set ERRFF to indicate the error.

The normal termination for a string of data and address commands is to send a DLE which contains a single data 1. This will result in setting ERRFF as described above. Any of the conditions setting ERRFF, including timeout of WDTOK, have the following result. The rise of ERRFF fires ERDLY (100 ms) which asserts SELND and RGCLR. SELND clears all activator components, resets the state counter, clears SELCT and so forth. However, CMDAX is cleared only by completion of a bus access.

Three indicators monitor reload operation. The first latches the occurrence of SELCT and stays lit until the next Master Reset. The second is driven by SELCT firing a .1 second oneshot to show when it is currently active. The third is lit by ACKLK from the DBAL firing a .1 second oneshot to indicate completed bus accesses.

Registers and Latches (RLD23)

The data, address, and padding bits are shifted into a single shift register 40 bits wide. Prior to each data and address pair, RGCLR clears this register and sets FLAGF. Subsequently, the rise of each DTCLK while SHDTA is true clocks the DATGO data stream into the shift register. The data is preceded by the initial 1 in FLAGF, which appears in the register as a zero, since the 74164 register is run with inverted data. When the initial logic high from FLAGF appears at the far end of the register, GOSUM comes true to indicate that the checksum bits are next. The contents of the register are now stable since SHDTA will go false as a result of GOSUM.

Meanwhile DATGO is applied to a CRC16 feedback check register also, since SERCH is false and shifted on the leading edge of DTCLK. During SHCKR, FBTAP is monitored in the control circuitry, a high indicating a bad checksum.

When CMDAX comes true, which will happen only after a proper checksum, the 16 data bits and 120 address bits are latched in a second buffer register. The low order address bit is forced to be zero.

Bus Access Control (RLD22)

Address and Data Bus Drivers (RLD24)

The heart of the bus access mechanism is the DBAL chip, configured to use only the A half and to clear on the trailing rather than leading edge of inputs. The command input is CMDAX.

When ONLN is true, the data and address buffers drive the data and address buses using standard BDR chips.

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION.	/	

RLD

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

RLD TECH. REF.

SIZE	CODE IDENT NO.	DRAWING NO.
A		RLD-05

SCALE	REV	SHEET
	A	1 OF 2

Status - none

Switches - none

Jumpers - padding bits

Jumper C7 as follows:

PAD BIT	3	2	1	Ø
FROM	C7-16	C7-14	C7-12	C7-10
-	to	to	to	to
Ø	C7-1	C7-3	C7-5	C7-7
1	C7-2	C7-4	C7-6	C7-8

RLD-2Ø SCHEMATICS

13	12	11	10	9	8	7	6	5	4	3	2	1	
	9615 16	9615 16	7474 14	7425 14	9318 16		7404 14	7408 14	7425 14	DRES 16 (VCC 1 390K 2 1K 3 5.1K 4 33K 5 10K 6 51K 7 100MΩ)	BDR AB16 ↓ AB19 16	BDR AB00 ↓ AB03 16	A
	9615 16	9615 16	7474 14	7425 14	7474 16		7404 14	74H40 14	74123 16	74123 16	74S74 14	BDR AB04 ↓ AB07 16	B
	9615 16	9615 16	7474 14	7474 14	74161 16	JUMPERS (16 14 15 13 12 1 2 3 4 5 6 7 8)	7402 14	7400 14	DBAL 24		BDR AB12 ↓ AB15 16	BDR AB08 ↓ AB11 16	C
	9615 16	9615 16	7474 14	7474 14	7474 16	7486 14	7400 14	7408 14			BDR MRESB QUITB RITEB 16	BDR STRBB DONEB SRLDB SACKB 16	D
J1 J2 44 10 MHz 44 50 50 51 51 51KΩ 52 52 51KΩ	9615 16	9615 16	7474 14	7410 14	74161 16		74164 14	74164 14	74164 14	74164 14	74164 14	BDR DB00 ↓ DB03 16	E
53 53 LED 54 54 LED 55 55 LED	9615 16	9615 16	7474 14	7425 14	74151 16		74164 14	74164 14	7486 14	74174 16	74174 16	BDR DB04 ↓ DB07 16	F
	74123 16	7474 14	7474 14	7425 14	74151 16		74174 16	74174 16	74174 16	74174 16	BDR DB12 ↓ DB15 16	BDR DB08 ↓ DB11 16	G

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7/31/74

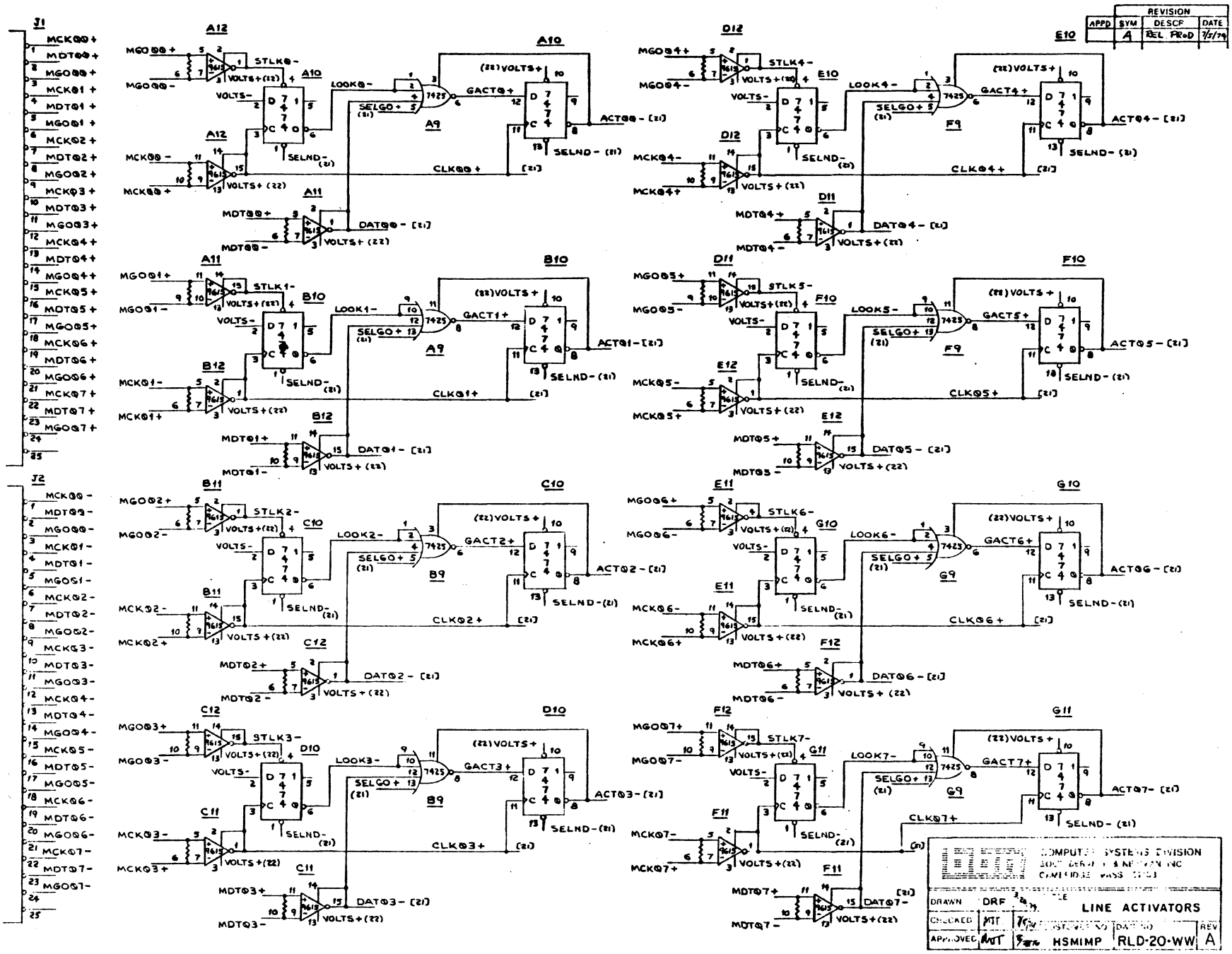
NOTES

1

TOP VIEW

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	5/13/74	TITLE INTEGRATED CIRCUIT LAYOUT
CHECKED	[illegible]	7/8/74	CUSTOMER/NO. HSMIMP
APPROVED	[illegible]	9/4/74	DWG NO. RLD-00-WW REV A

RLD


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 7/5/79
J1
J2
A12
A10
A11
A9
B10
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B9
C10
C12
C11
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LOOK2-
LOOK3-
LOOK4-
LOOK5-
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LOOK7-
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GACT2+
GACT3+
GACT4+
GACT5+
GACT6+
GACT7+
SELGO+ 5
SELGO+ 13
SELND-
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CLK01+
CLK02+
CLK03+
CLK04+
CLK05+
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CLK07+
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ACT02-
ACT03-
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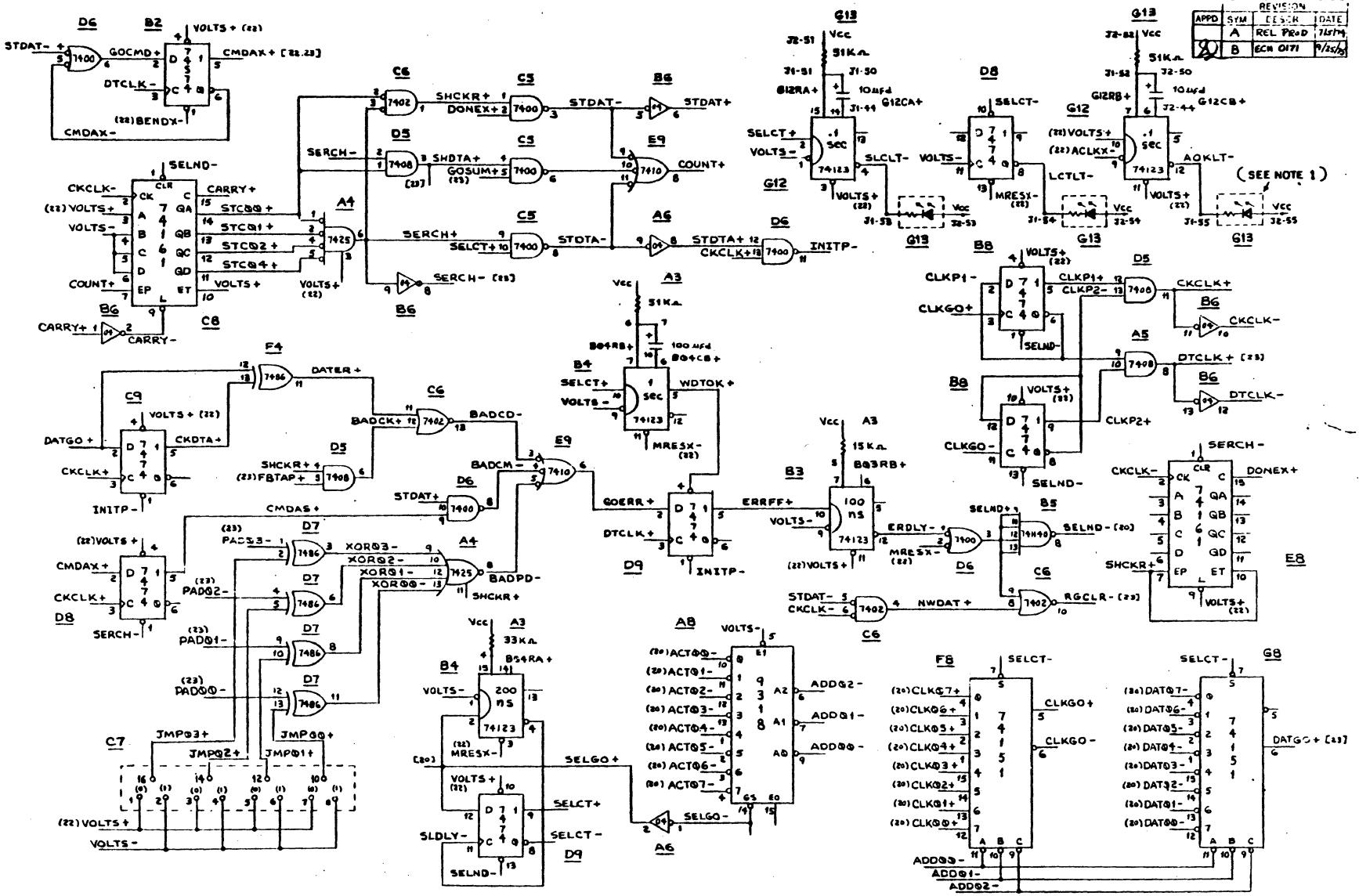
ACT07-
DAT00-
DAT01-
DAT02-
DAT03-
DAT04-
DAT05-
DAT06-
DAT07-
VOLTS+
VOLTS-
COMPUTER SYSTEMS DIVISION
DRAWN DRF
CHECKED MJT
APPROVED MJT
LINE ACTIVATORS
HSMIMP
RLD-20-WW
REV A



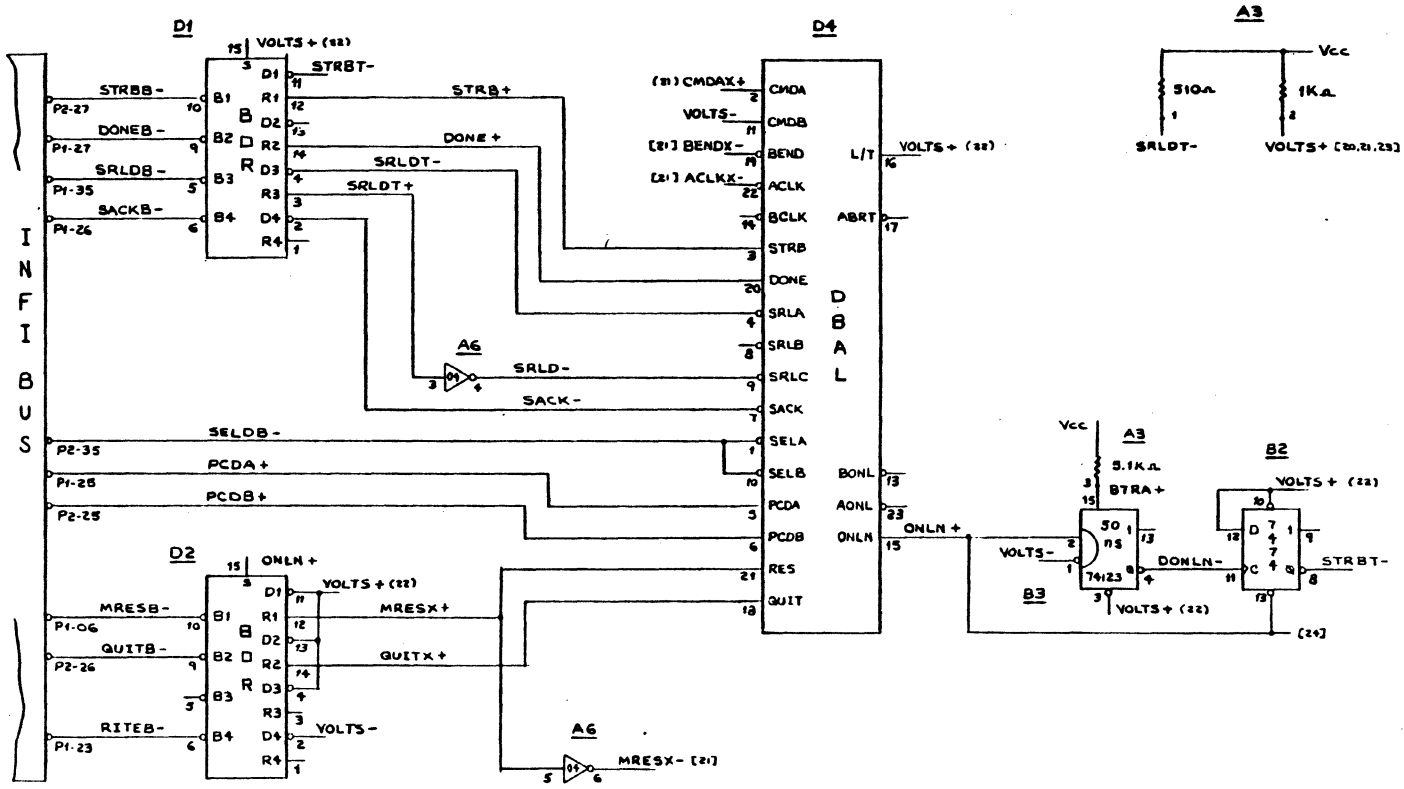
PAD BIT	3	2	1	0
FROM	C7-16	C7-14	C7-12	C7-10
—	TO	TO	TO	TO
0	C7-1	C7-3	C7-5	C7-7
1	C7-2	C7-4	C7-6	C7-8

NOTES

1- LED's (3) ARE DIALCO #555-2007

RLD

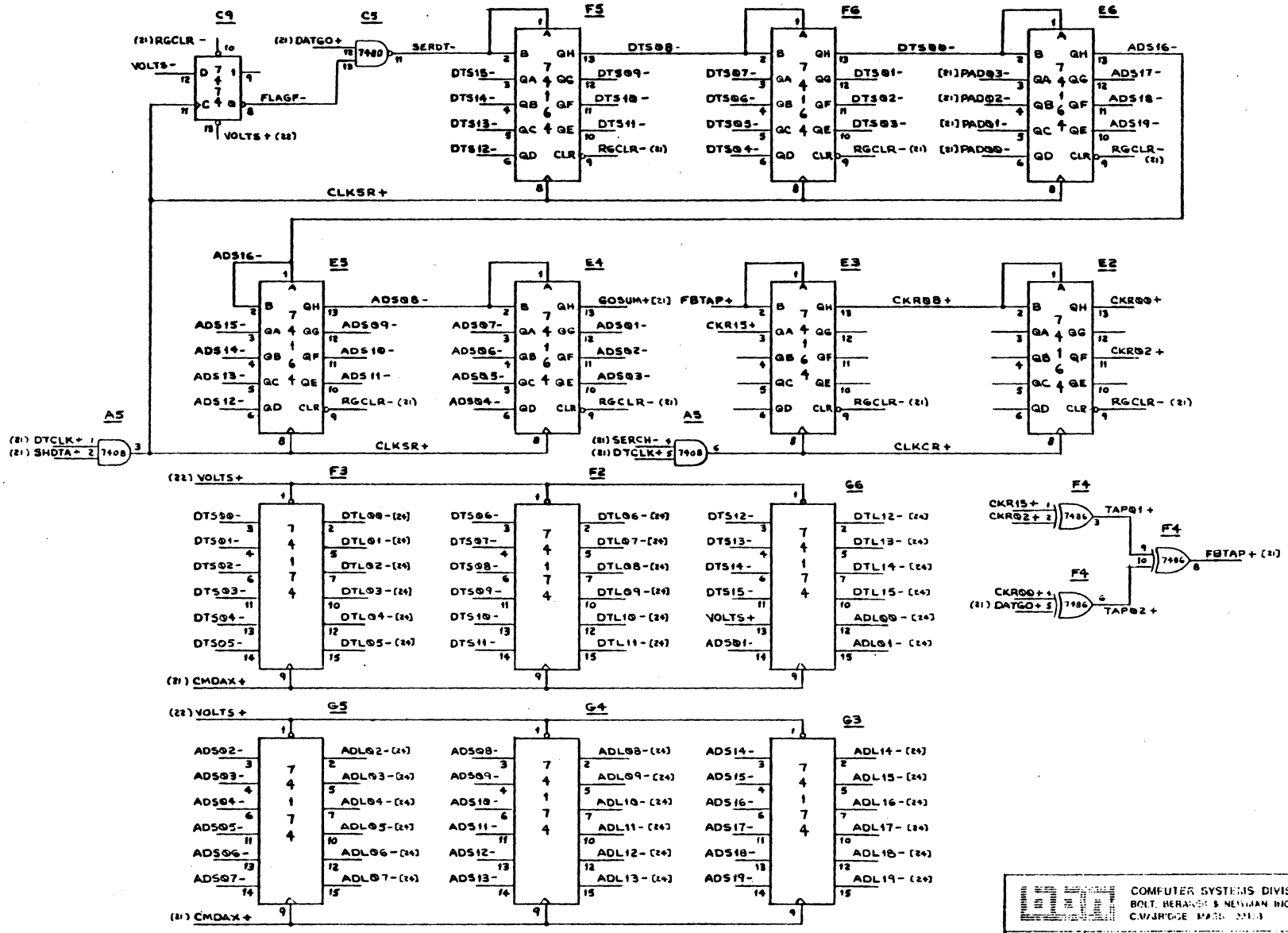
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.5.74



DRAWN	DRF	3/8/74	BUS ACCESS CONTROL
CHECKED	MJT	3/8/74	
APPROVED	MJT	3/8/74	HSMIMP RLD-22-WW A

COMPUTER SYSTEMS DIVISION
BOLT BERANEK AND NEWMAN INC
CAMBRIDGE MASS

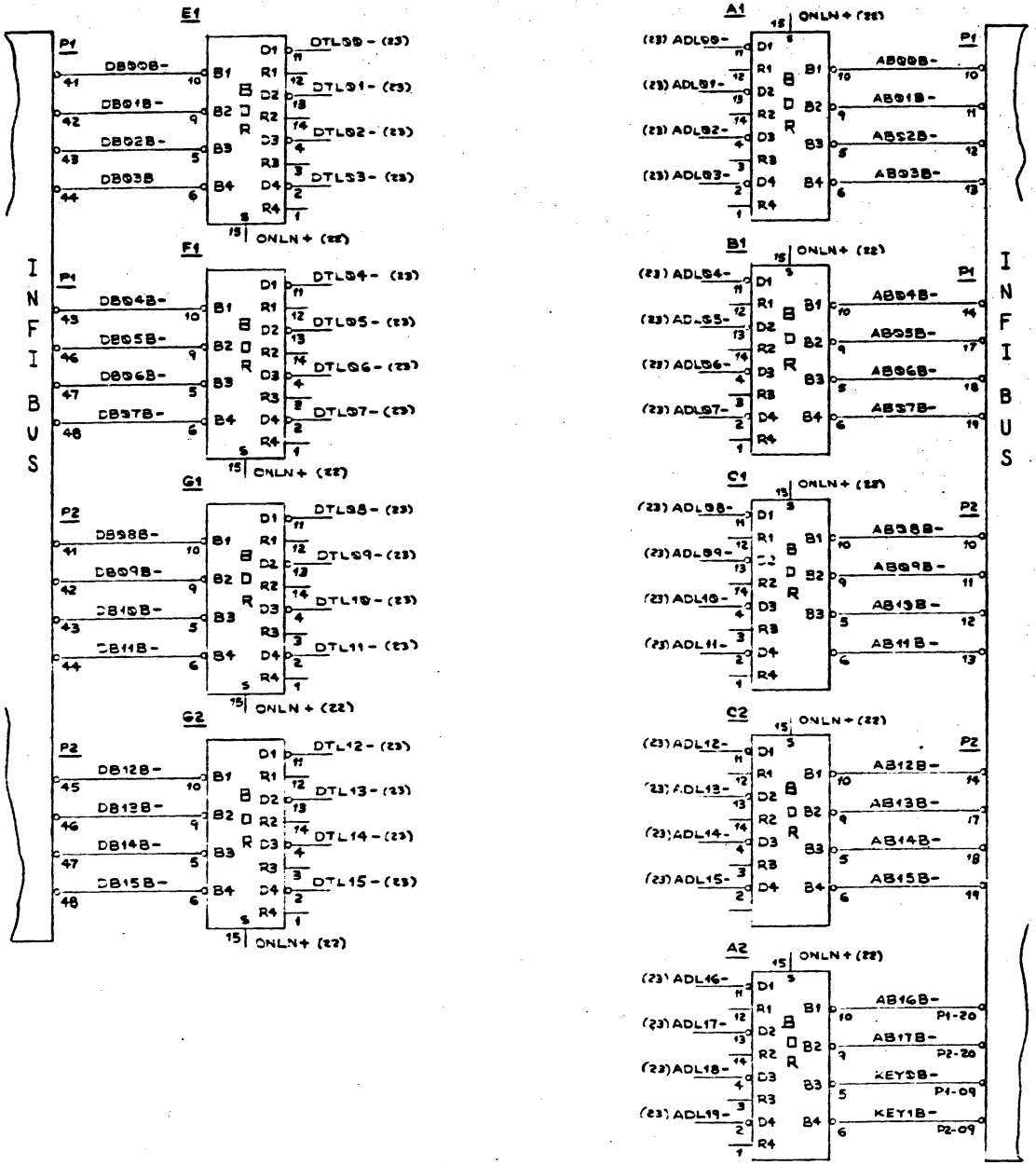
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	12.5.74



COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE MASS. 02138

DRAWN	DRF	3/19/74	TITLE: REGISTERS & DATA LATCHES
CHECKED	MT	3/19/74	SUBSYSTEM NO: HSMIMP
APPROVED	MT	3/19/74	DATA NO: RLD-23-WW
			REV: A

RLD



REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.5.76

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	3/19/76	TITLE	ADDRESS & DATA BUS DRIVERS
CHECKED	MT	7/4/76	CUSTOMER NO.	DWG NO. / REV
APPROVED	MT	7/5/76	HSMIMP	RLD-24-WW / A

Real Time Clock

RTC-Ø2 Logic Description

RTC-Ø5 Technical Reference

RTC-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE [illegible]	6-28-74	
B	ECN 0056	8-28-74	
C	ECN 0218	7-21-75	

RTC

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN [illegible]

CHECKER

ENGINEER [illegible]

APP'D FOR REL [illegible]

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

RTC LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		RTC-02

SCALE	REV	SHEET
	C	1 OF 5

RTC LOGIC DESCRIPTION

The Real Time Clock (RTC) is a single card module containing a counter, bus master logic, slave logic and readable switch registers conforming to the RTC functional specification. This document is a detailed description of the implemented logic. In general, signals signed "+" are true when at a TTL high level, signals signed "-" are true when at a TTL low level.

Clock Timing Chain (RTC23)

The 25 MHz system clock (CLKAB+) is buffered and applied to the countdown input of a BCD counter. The 2.5 MHz output pulse train from this counter CLK1D+ is sufficiently wide to drive the remainder of the divider chain. This signal is applied to the countdown input of the 74193 binary counter at D7. Underflow of the 74193 at D8 produces CLK2C- which initializes the counter at D7 to 1010 by direct load. When D7 underflows, the trailing edge of CLK1C- pulses the countdown input of D8. Because of the initialization of D7, these two counters constitute a divide by 250 network. Therefore, the output pulse train CLK2C- is the system clock divided by 2500 -- a 100 microsecond repetition rate. If TIKEN is true (see below), the trailing edge of this signal sets TIKTM which is the command input to the DBAL chip (RTC20). The trailing edge of BONL- occurring at the end of the bus cycle steps the four stage 16-bit counter, which is the actual clock register. The bus access cycle at each 100 microsecond clock tick guarantees that the clock will not be changing while it is being read. The counter step on the trailing edge of BONL- guarantees that any bus access resulting from stepping the counter (see below) will not conflict with the ticking mechanism. The BEND- signal from the BDR clears TIKTM.

A one second timeout disables the 100 microsecond clock tick accesses and therefore all clock bus activity. Any reference to the clock addresses (read or write) fires the timer when the leading edge of ME fires TIKGO, which is synchronized and applied to the data input to TIKTM. TIKEN (the synchronized TIKGO) is made false one pulse of CLK2C after either the expiration of the timeout period or a master reset (MRES direct clears TIKGO).

The 16-bit counter counts down to simplify the data network by allowing inverted sense outputs from the counter. Operation of the counter is completely straightforward with the underflow condition of each stage allowing the input pulse to that stage to increment the succeeding stage.

RTC

Clock Control (RTC20)

The heart of the bus master circuitry is the DBAL chip, which operates round robin on the device service level. To allow for setting of the data network, ONLN is delayed by 80 ns (DONLN-) before STRBT is set and STRB applied to the bus. The fall of ONLN+ clears STRBT. Control signals to and from the bus are transmitted and received in the conventional manner using BDR chips. The SRLA and SRLB open collector DBAL outputs are pulled up to 510 ohms each. TIKTM+ is applied to the B command input for each 100 microseconds tick of the clock. During the resulting cycle, the PID is addressed with zero data as described below. This has no effect except to lock the bus while the clock is incremented. Incrementing takes place on all bus cycles unless the cycle is aborted in the request portion.

Requests for the 25.6 ms and 1.6 ms PID interrupts are applied to the A command input as follows. The 1.6 ms "fast" interrupt request is set by the leading edge of CLK03 setting DOMLC. The 25.6 ms "slow" interrupt request is set by the trailing edge of CLK07 setting DORTC. This insures that these two requests are non-interfering since they will occur on opposite phases of CLK03. DORTC will be set on the trailing edge of CLK03 while DOMLC will be set on the leading edge. The OR of these two signals is applied to the A command input of the DBAL. The requests are cleared by Master Reset, a bus abort (QUIT gives ABRT- at the DBAL), or by conclusion of the service cycle (ACLK- being true). Note that aborted requests are not reinitiated. During these bus accesses, the desired level is written to the PID as described below.

When ONLN+ is true, RITE is asserted on the bus to cause the interrupt level data to be written to the PID. When the clock is addressed, the leading edge of STRB samples RITE on the bus and sets RITE- if a write operation is to take place.

Clock Address and Decoding (RTC21)

This is the circuitry involved in the clock acting as a bus slave when addressed by other devices and the address generation for bus master references to the PID.

Slave address decoding recognizes addresses of the form FXY0Z. XY is switch selectable to be E0, E8, F0, F8 (ASL11-ASL12-), and is recognized by two XOR gates, ADC3+ and ADC4+. Z is either 6, 8, A, C, or E, recognized by an AND-OR-INVERT gate.

Either address bits 1 and 2 are true (6), or bit 3 is true (8, A, C, E), giving AB123-. A multi-input NAND gate outputs ADCOM- true when clock addresses are recognized. The leading edge of STRB, propagated through two XOR gates to match the address recognition delay, clocks ADCOM- into ME if HOLD is not true. Otherwise, the trailing edge of HOLD will clock ADCOM. When ME+ is true, an access to the clock is in progress. The leading edge of ME triggers a MEPLS (80 ns) to allow data to the bus to settle. The trailing edge of MEPLS fires DONET a 50 ns pulse to drive DONE on the bus. When STRB falls as a result, ME is direct reset. On clock read references, RITE- will be high, causing DREN+ or MREAD+ to enable the data BDR's driving data to the bus.

When the clock writes to the PID, ONLN enables address FXY00 on the bus directly at the address BDR's. XY is chosen by the setting of switches PIA11- and PIA12-. When a real PID level is written, AONL- being true causes DREN+ to enable the low order BDR's. AB01P-, AB02P- and AB03P- determine which data source will be input to the low order data BDR's. AB01-, AB02-, and AB03- address the high order data bits, since these bits are only gated to the data bus lines on clock slave references. These bits constitute the 3-bit address of the 8-to-1 multiplexers driving the BDRs. Assignments are as follows, where 0 indicates a false address line.

RTC

000	1.6 ms PID
001	25.6 ms PID
010	unused
011	clock register
100	25.6 ms PID/1.6 ms PID switches
101	switch register #1
110	switch register #2
111	switch register #3

For clock slave reference AONL- will be false, and the bus address lines are applied directly to the multiplexer address inputs to direct the addressable registers to the bus. For clock master references to the PID when a level is written, AONL- is true, making AB02P- and AB03P- false. This selects one or the other PID level as follows. AB01+ is false since this is a reference to the PID, and AONL- is true, so the state of MLCGO+ determines AB01P-. If a 1.6 ms ("MLC") PID reference is requested, DOMLC+ direct sets MLCGO causing AB01P- to be false. This gives address 000 to the multiplexers and the 1.6 ms level is written to the bus. Otherwise, MLCGO- is false and AB01P- will be true, giving 001. This causes the 25.6 ms level to be

written to the bus. BEND- clears MLCGO after the bus cycle is concluded to guarantee the stability of the data during the bus cycle. The multiplexer circuitry is described below.

Clock Data (RTC22)

The data paths consist of sixteen 8-to-1 multiplexers addressed as described above, and four BDR chips connected to the bus. The multiplexers are used with both data and address senses inverted -- the former for convenience in driving the BDRs, the latter for convenience in encoding the 3-bit multiplexer address. Thus the data selected by address 000 is found on the 74151 data 7 input. As described above, the BDR drivers are enabled by the presence of DREN or MREAD. The receivers are unused.

The high order 8 bits for the two data inputs written to the PID are unused. The low order inputs are switch selected (PLF01-07, PLS01-07). The third input is unused, while the fourth comes directly from the 16-bit clock register (CLK00-15). The fifth position has PLS01-07 in the left half and PLF01-07 in the right half. The remaining three inputs are from the 16-bit switch registers (SW100-SW115, SW200-SW215, SW300-SW315). Switches are described below.

Switch Registers (RTC24)

All switches are true when closed, causing that signal line to be low. Each switch has the usual pull-up.

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	12-16-74	

RTC

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:	
DRAFTSMAN	
CHECKER	
ENGINEER	
APP'D FOR REL	
APP'D (CUSTOMER)	

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

RTC TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		RTC-05

SCALE	REV	SHEET
	A	1 OF 2

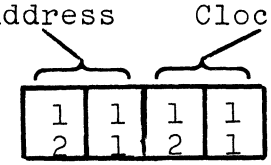
RTC - REAL TIME CLOCK BBN

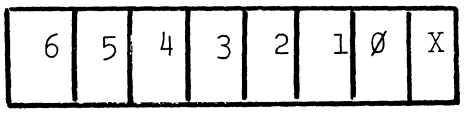
Status - address none

W
R

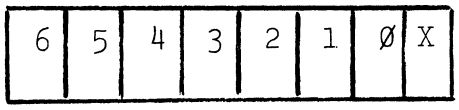
Switches

PI Address Clock Address

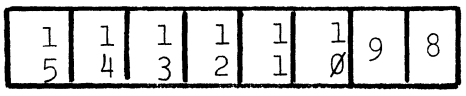


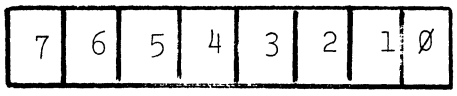


PI slow 25.6 ms

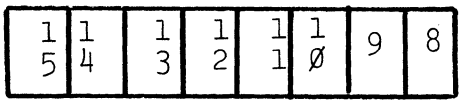


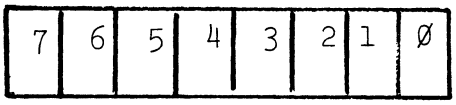
PI fast 1.6 ms



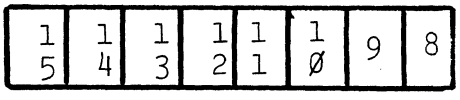


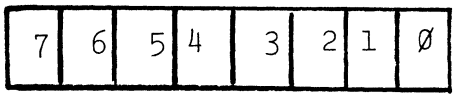
Switch #1





Switch #2



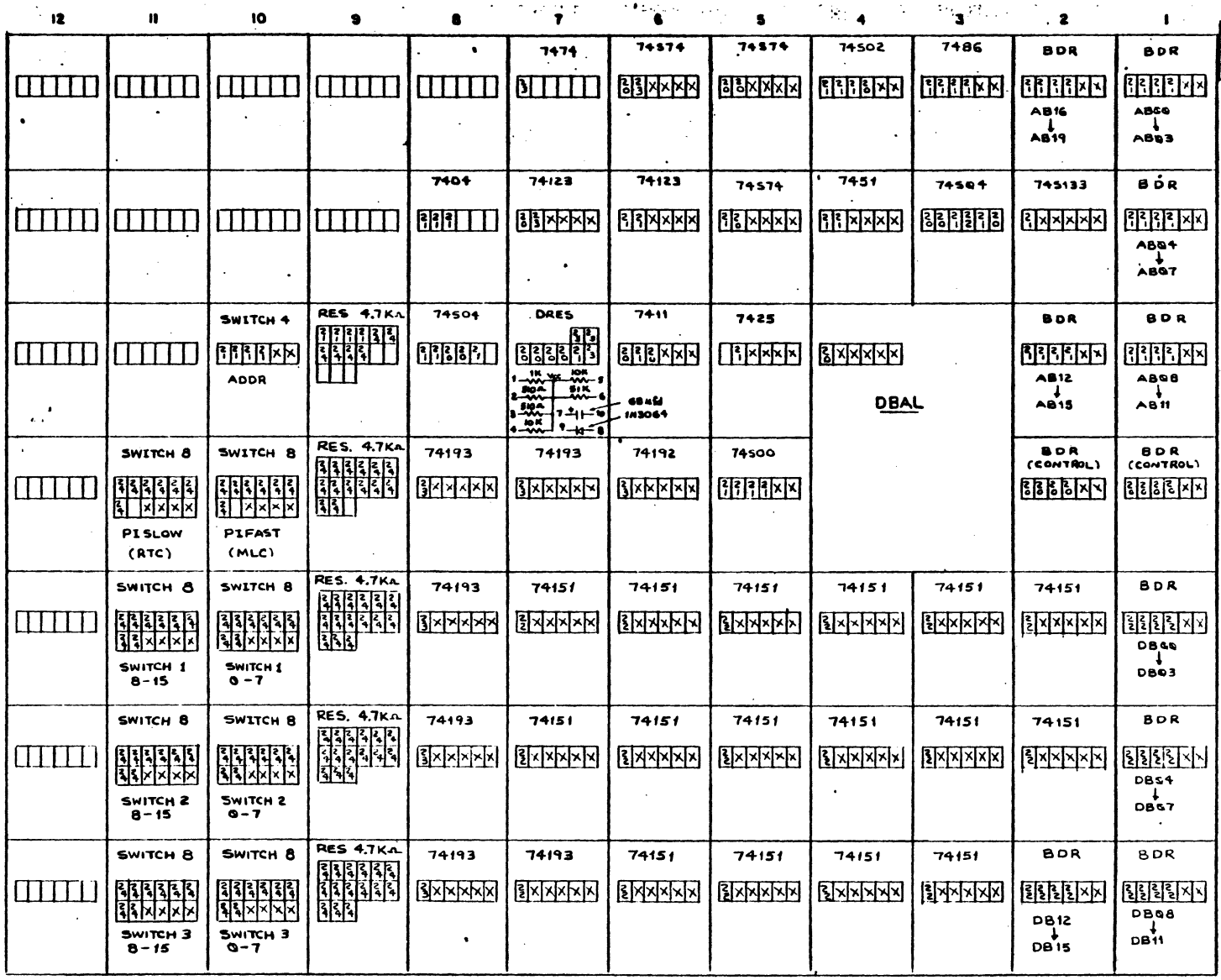


Switch #3

Jumpers - none

RTC

RTC-2Ø SCHEMATICS



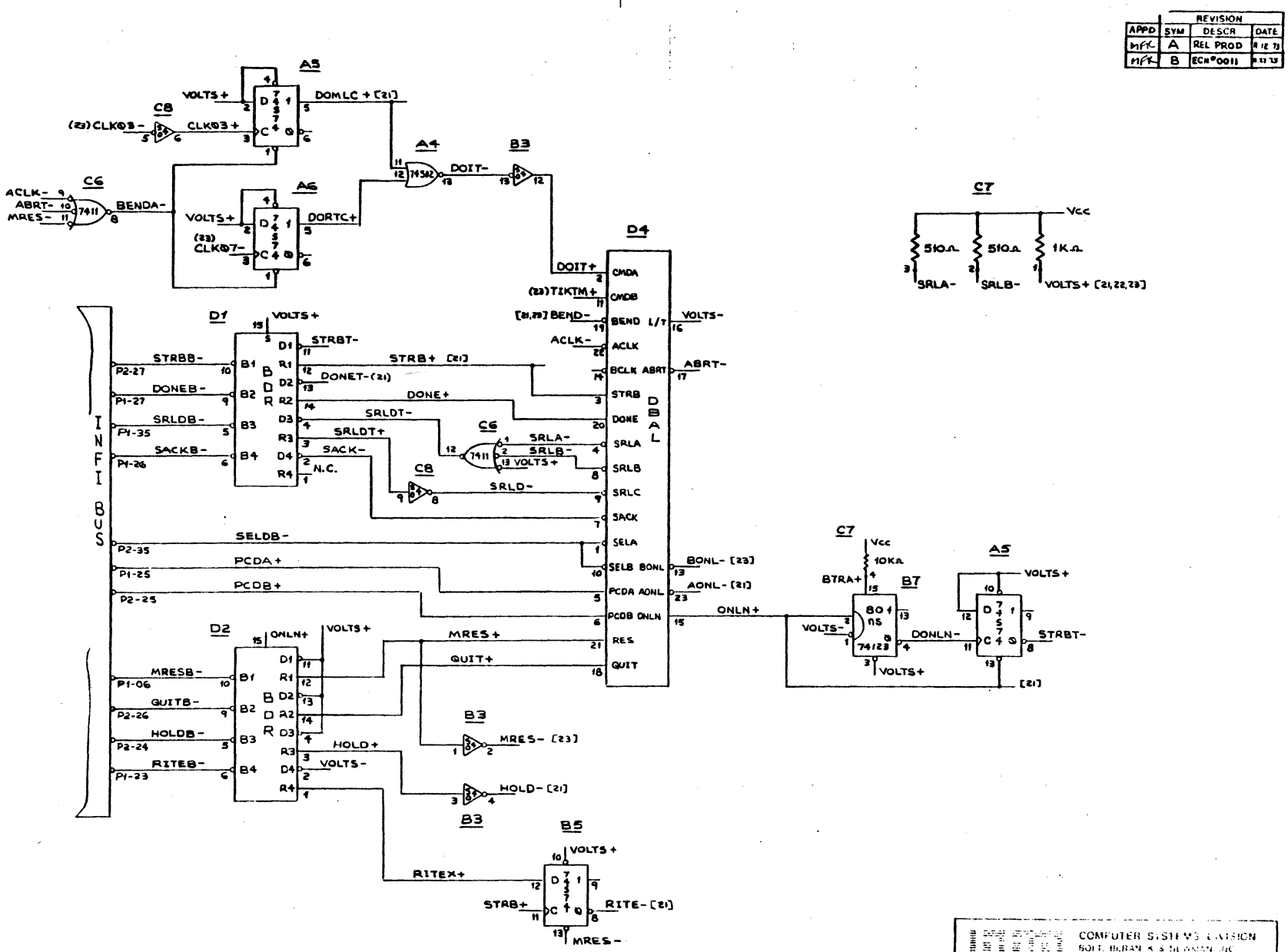
TOP VIEW

REVISION			
APPD	SYM	DESCR	DATE
MFT	A	REL PROD	4.R.73
MFG	B	ECN #0011	9.13.73
MFG	C	ECN #0151	7.11.75

NOTES:

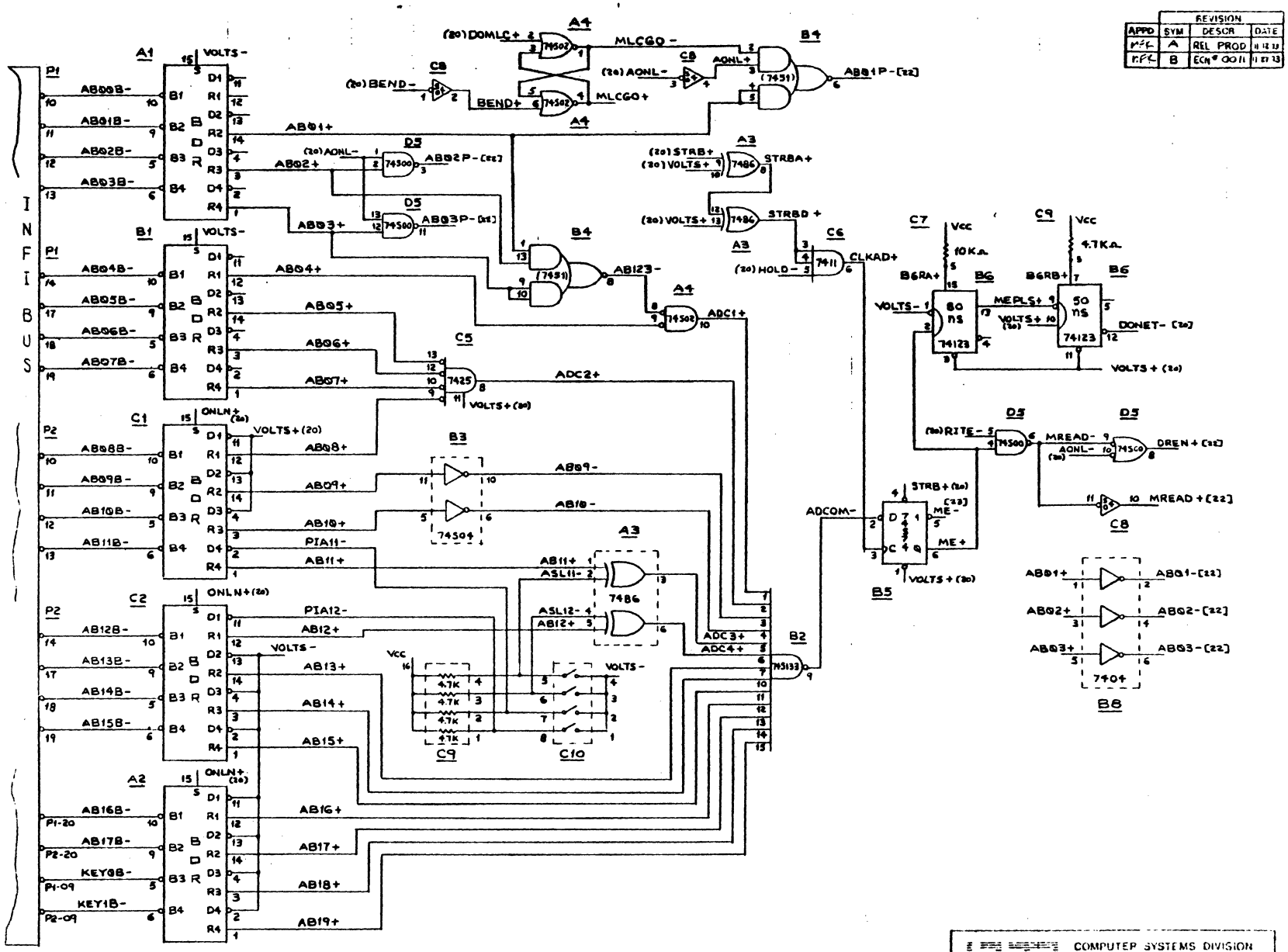
BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	DRF	5/1/73	TITLE	INTEGRATED CIRCUIT LAYOUT
CHECKED	DRF	7/6/73	CUSTOMER/NO.	DWG NO. / REV
APPROVED	MFT	8/16/73	HSMIMP	RTC-00-WW / C

RTC



DRAWN	DRF	9/19/73	CLOCK CONTROL
CHECKED	DRF	9/19/73	
APPROVED	ABT	9/27/73	HSMIMP RTC-20 WW B

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS

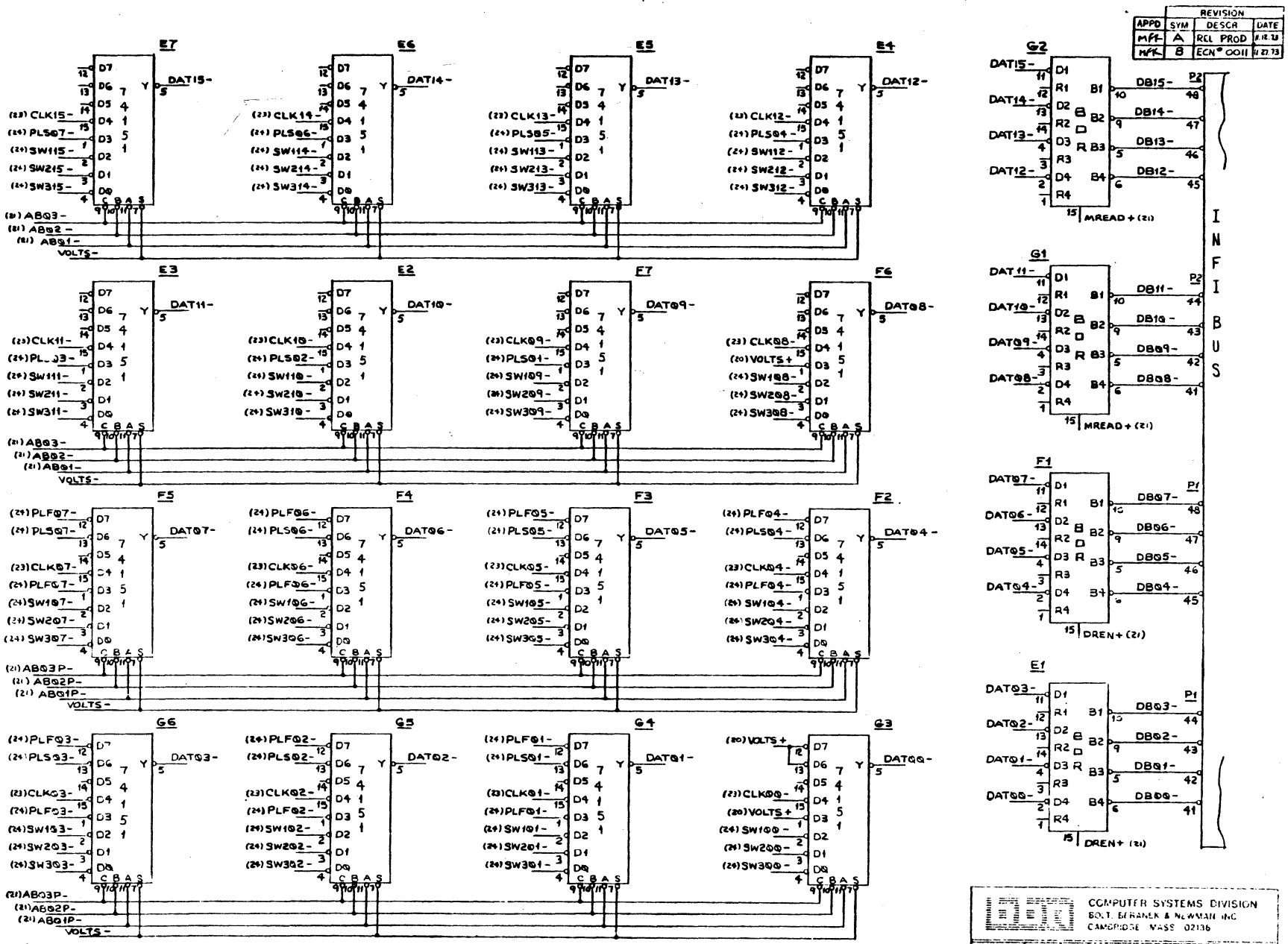


REVISION			
APPD	SYM	DESCR	DATE
MEL	A	REL PROD	11 12 73
MEL	B	ECN# 0011	11 27 73

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/8/73	TITLE: CLOCK ADDRESS & DECODE
CHECKED	DRF	11.73	CUSTOMER NO. / DWG NO.
APPROVED	MJT	6/8/74	HSMIMP / RTC-21-WW B

RTC



REVISION			
APPD	SYM	DESCR	DATE
MFT	A	RCL PROD	11.12.73
MFK	B	ECN# 0011	11.27.73

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE MASS 02136

DRAWN	DRF	12/13	TITLE: CLOCK DATA
CHECKED	DRF	12/13	
APPROVED	MJT	12/13	COVER NO: HSMIMP
			DWG NO: RTC-22-WW
			REV: B

	REVISION		
APPD	SYM	DESCR	DATE
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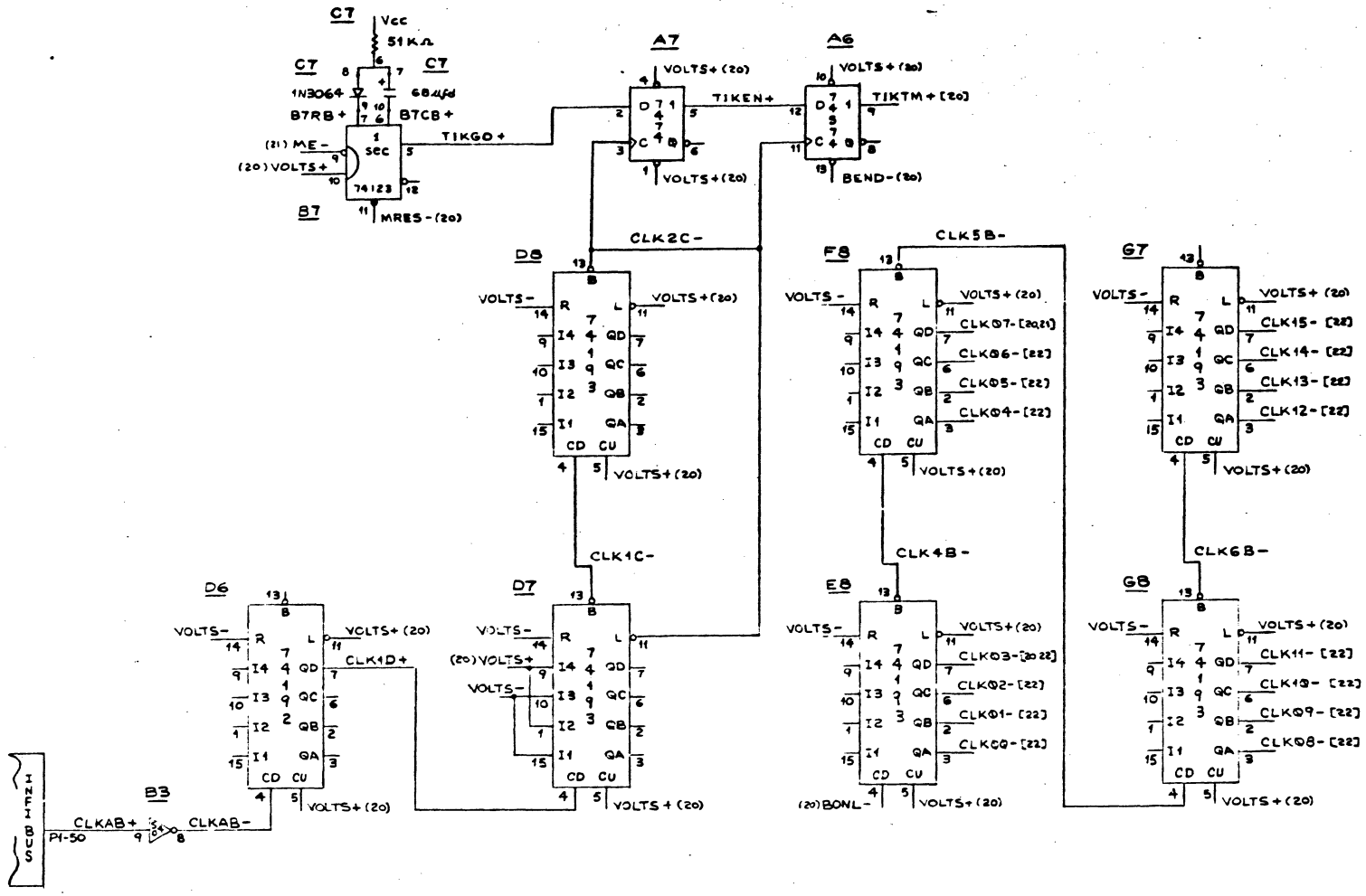
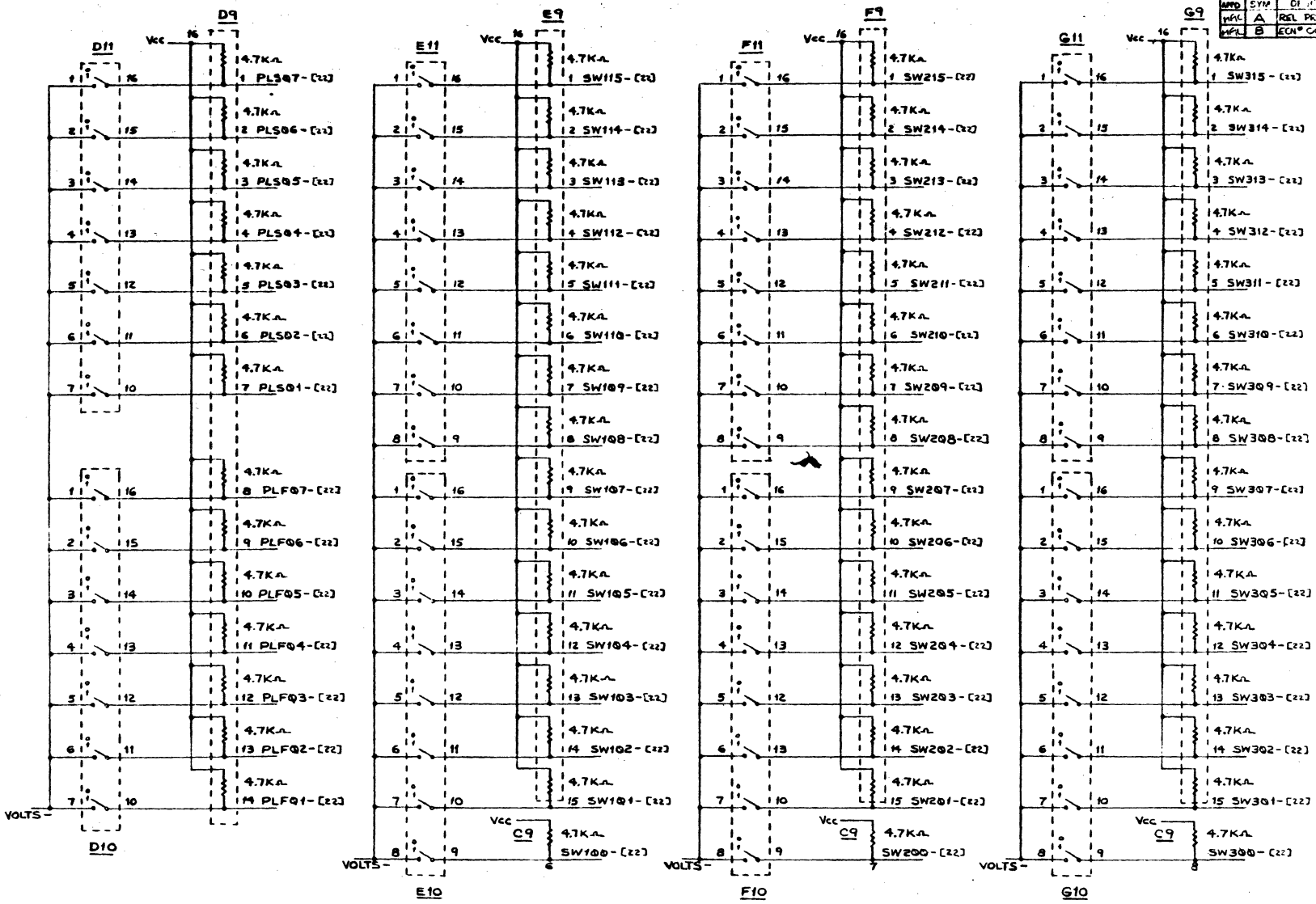
	B	ECN# 0011	11.21.73
	C	ECN# 0157	12.14.73



COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	9/20/73	TITLE: CLOCK TIMING CHAIN
CHECKED	DRF	9/20/73	
APPROVED	[illegible]	[illegible]	CUSTOMER NO.: HSMIMP; DWG NO.: RTC-23-WW; REV: C

RTC



REVISION			
APPD	SYM	DESCR	DATE
MFG	A	REL PROD	11.17.78
MFG	B	ECN# 6011	11.27.78

COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS 02138

DRAWN	DRF	8/20/78	TITLE: SWITCH REGISTERS
CHECKED	DRF	8/22/78	CUSTOMER NO: HSMIMP
APPROVED	MFT	8/24	DWG NO: RTC-24-WW
			REV: B

Sense Inhibit Drivers

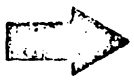
SID-Ø2 Logic Description

SID-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SID



SEE TAG-Ø2

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/72

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

SID LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		SID-Ø2

SCALE	REV	SHEET 1 OF 1

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SID

SEE TAG-02

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/9/?

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

SID SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		SID-20

SCALE	REV	SHEET 1 OF 1

Synchronous Line Interface

SLI-Ø2 Logic Description

SLI-Ø5 Technical Reference

SLI-2Ø Schematics

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	1/19/76	
B	ECN 0218	7/21/76	

SLI

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

SLI - LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		SLI-Ø2

SCALE	REV B	SHEET OF

SLI LOGIC DESCRIPTION

The reader is assumed to have read the functional specification for this card. In particular, the description of the "bit-map" Appendix A should be at hand while reading this logic description. Also, for general notes about the drawings, see Appendix B.

SLI20

Drawing 20 contains the logic for miscellaneous INFIBUS control signals. In the upper left, the discontinuous INFIBUS signals are carried from one side of the INFIBUS connector to the other. This includes the precedence pulse PCDAB+. The remaining four INFIBUS signals used actively in the card are the: Strobe, Done pulse, Master Reset, and Rite signals. These are interfaced in the BDR D1. The status of the Rite signal during a particular memory reference is held in a flip-flop whose outputs are RITE+ and RITE-. The upper portion of the drawing shows a bank of 1K resistors used to generate positive logic signals for unused logic inputs throughout the card. Additionally, there are 6 single-pole switches and their associated pull up resistors used to generate signals in the Data-Type word (DT107 down through DT206). (DT105 and DT205 are no longer used in the logic.) These perform no active logic function in the card but may be used to indicate baud rates or identify individual cards in a system.

SLI21

Drawing 21 shows the interface address decoding for this card. The logic is straightforward and conventional. At the left are 5 BDRs providing a direct interface to the INFIBUS. Their inputs are unused (tied high in early versions of the card; left floating but gated off by grounding the strobes in later versions), and their outputs are used as part of the address selection logic. The switches on the card are used to select the address to be recognized by an individual card. To the right of center is a 13-input and-gate, whose output ADCOM- indicates that the address specified on the bus matches the switch settings on the card. Its inputs include bits 16-19 ungated, and bits 4-13 as selected by switches shown at the bottom of the drawing. The 7486 and 74136 bugs are exclusive-or circuits. Note 2 on the drawing indicates that a switch closure is used to specify recognition of a 1 in the corresponding address bit. It does

this by grounding the 1 input of the exclusive-or circuit associated with it. For example, with ASL11- grounded by the lowest switch in the leftmost switch of A3, a positive gate output ABS11+ will occur when the second gate input AB11+ is high. This will occur when the associated BDR input is low, indicating assertion of AB11B- on the INFIBUS. The output of the 4 gates in C3 is a wired-and configuration going high only when bits 4-7 compare correctly.

At the bottom of the drawing, an additional de-skewing gate is used to delay the strobe pulse STRB+ by an amount equivalent to the delay in the individual data bits before triggering the flip-flop whose output is ME+. A gate is also provided to inhibit ADSTR+ from clocking the flip-flop if the bus HOLD signal is present. Note that until the address selection cycle is started, the STRB+ pulse keeps the flip-flop in the "1" state. ME+ is a synchronized address selection signal used for all subsequent address dependent functions. Below this flip-flop is a 150 ns delay whose output ultimately generates a 60 ns DONE pulse.

In the upper right corner of the drawing is an octal decoder. Its inputs are the RITE signal, the low order address bits 1 and 3, and address bit 2 anded with MEPLS+. As is noted on the drawing, the octal decoder is strobed only on selection of the Data and Control words of an SLI. Each of the two independent halves of the SLI is provided with its own write-control, read-data and write-data decoded pulses. Below the octal decoder is a single and-gate whose output DRSTR+ is used to strobe the data BDRs during a read operation.

SLI22

Drawing 22 contains the data multiplexer and BDRs used to interface with the data portion of the INFIBUS. The 4 BDRs are shown at the right of the drawing; their non-bus outputs in all cases go to other drawings. Each of their inputs comes from a flip-flop used to synchronize the data information with the INFIBUS reading cycle. The flip-flops themselves are contained on three circuits (74174 and 74175) near the upper left and in the top center of the drawing. In all three cases the strobe used to latch the data is the data-read strobe DRSTR+. Note that this is the same signal used to strobe the BDRs themselves. This does not prohibit change of the signals on the INFIBUS at the beginning of the cycle, but the 150 ns duration of DRSTR+ is sufficient to ensure stabilization of outputs by the end of the cycle, when the signals are used on the bus.

The remaining logic is part of the data multiplexer. The low order 3 bits of the address decoding are brought in at the bottom of each bug, and the data bits to be decoded are brought in at the left. The bit assignment chart will be of considerable help in understanding the origin of these signals. Bugs used for the 1-out-of-8 decoders are 74151s. Their strobe is permanently enabled (negative), and because the input signals tend to be available in their low state when true, the low output is used. As an example: Bit 7, whose output is DAT07-, appears at the left center of the drawing. In conventional use of this bug, positive inputs and positive address bits are ordinarily used. Therefore, a certain amount of mental inversion is necessary to follow the logic. If the address on the INFIBUS is all zeros for bits 1, 2, and 3, the A, B, and C inputs of the multiplexer are all high. This results in the input D7 or pin 12 being gated through to the output pin 5. Each of the multiplexer bugs is therefore shown with the input addresses ascending from 0-7. The appropriate Data-Type register bit is at the bottom and the modem 2 data bit is shown at the top.

The same situation pertains to the bottom row of 74153s. Their strobe input is permanently enabled, and the positive states of their address bits are used as inputs. Note from the bit assignment chart that no outputs should result from Data bits 0-3, unless address bit 1 is asserted. This is carried out by a negative-and (actually an "or") gate at the output of each 74153. The correct function could not be obtained by strobing the multiplexers themselves with AB01- because of the nature of the bug.

SLI

In the upper left corner, for bits 14 and 15, the 74153s are used more conventionally, since the positive states of their inputs are available. The AB01- is used as a strobe for both, and the positive states of address bits 2 and 3 are used as selection inputs. Since the four data bit inputs are available in a positive state, the output will be positive, and the 7432 is unnecessary. As with each of the other multiplexers, the unsynchronized output is brought to a flip-flop for synchronization by the data-read strobe. This step is required because of the ultimate use of SLIs in systems containing Parity (PAR) cards.

SLI23

Drawings 23 and 24 show the detailed logic specific to modem #1. 25 and 26 are identical, except that each signal name has had a "1" replaced with a "2", indicating that it is the second modem logic. Drawings 23 and 24 will be described. The lower edge connector is for the modem 1 cable.

General parts of drawing 23 are as follows: in the center of the drawing is a COM2601 LSI bug, a 40-pin USRT (Universal Synchronous Receiver Transmitter), see Appendix C. The portion having to do with received data is shown in drawing 23; the transmitter portion is shown on drawing 24. In the upper left corner of 23 are the serial inputs and clocks coming from the modem. Below them is an 8-bit shift register used for the determination of the sync character being used (ASCII or EBCDIC). Below that is logic involved in resetting the receiver portion of the USRT. In the lower center are 2 flip-flops having to do with error conditions derived from the USRT parity error and overrun. Immediately to the right of these are 3 flip-flops and 2 gates having to do with sync-character detection and a transition to data mode following sync characters. Above these are a flip-flop, two oneshots and a pair of gates involved in synchronization of Data-Ready with the INFIBUS. To the right of the USRT are 8 bits of flip-flop storage for the second rank of double buffering. One rank of parallel buffering is contained within the USRT itself.

Data enters from the modem with the characteristics shown in the waveform to the left of USRT. The data bits are sampled on the negative transition of the clock in two places. One is the USRT itself. The second is the 8-bit shift register. A previous reset signal will have set all the bits of this register to 1 and the normal condition of a synchronous modem line with no data on it is all ones. Therefore, the succeeding clock pulses will cause no change in the outputs of the 74164. When a transition to a zero occurs it will ultimately be shifted down to the bottom of this register. At that point the 1LSB1+ signal goes low, gating off further clock signals into the shift register. The register then contains 8 bits of information that begin with a 0; Ordinarily it will be a SYN character of either ASCII or EBCDIC format. The program may detect this with the status bit ST100 and therefore determine whether an ASCII or an EBCDIC terminal dialed into its associated modem. Once this has been determined, there should be no further use for the shift register. Ordinarily, if an unknown character is read from these status

bits 0-7, the program will reset the system, and again search for SYNC characters, assuming that noise was the cause of the transition to zero in the data.

The unorthodox symbol used to show the gating of shift pulses into the First-Character-Received register accurately describes the logical function taking place. Its pin 2 remains high, enabling negative transitions on pin 1 to produce positive transitions at its output and to the shift register trigger input.

Turning now to the USRT, several things begin to happen. The USRT contains a holding register, into which the program has previously deposited an 8-bit character to be searched for in the data stream as a sync character. Due to the possibility of phoneline noise generating sync characters, synchronous line protocols invariably call for multiple sync characters to be used in establishing synchronization. Logic exists to do that. When the USRT has detected that 8 bits matching the specified sync character have come into the serial input, its Sync-Character-Received pin (17) goes high. Although the program can sense this on RD114, the logic about to be described makes this unnecessary. The two flip-flops 1SYN1 and 2SYN1 have the function of determining that two or more sequential sync characters have arrived, and establish a "data mode" only at the transition to the first non-sync (data character) after two or more syncs.

SLI

Both flip-flops begin in a reset condition due to the Reset-Receiver pulse RESR1- coming from the oneshot in the lower left corner of the drawing. At this point, the USRT specification and its timing diagram, located in Appendix C, should be consulted. Note that the Sync-Character-Received signal comes up before the Received-Data-Available RDA1+ signal goes high. This sets the lower flip-flop causing the signal 1SYN1+ to go high, and enabling the upper flip-flop.

Let us now consider the case where only one sync character is received, presumably caused by noise on the modem line. To the right of these two flip-flops is a 4-input gate whose input pins 1,2, and 4 are now high (pin 2 is high because the data flip-flop has been cleared previously by the reset pulse). After the next 8 bits have been clocked into the USRT, if these 8 do not contain a sync character, the SCR signal drops, causing its inversion signal NSCR1+ to make the remaining input of the 4 input gate go high. NOIS1-, its output, now drops, feeding back into the reset oneshot, and setting the system back into a

condition where it once again searches for sync characters. (A 33 pf capacitor is provided to prevent "runting" of the NOIS1- pulse.) The positive transition in NSCR1+ does not produce data mode since the remaining input to the two input gate, signal 2SYN1+, is still in the low state.

If on the other hand a second sync character follows the first, the following will take place: the first sync character makes 1SYN1+ high, priming the D input of the 2SYN1 flip-flop. Eight bits later, the RDA1+ signal strobes that flip-flop, causing 2SYN1+ to go high, and disabling the four input gate directly below it. These will remain in this state for as long as sync characters are received. Each new sync character strobes both flip-flops into the set condition, but both are set already. The NSCR1+ signal is low because continuous sync characters are being received. Eventually a non-sync character will be shifted into the USRT and the Sync-Character-Received signal will drop, as shown in the waveform to the bottom right of the USRT symbol. This transition causes SDAT1- (the output of the 2 input gate) to drop, and sets the data-mode flip-flop DATA1+. Because 2SYN1- has been low, the 4 input gate has been disabled so that the transition to non-sync has not produced an output of the noise gate. Once data-mode has been achieved, that gate is disabled by its pin 2 so that appearance or disappearance of a sync character in the following data stream does not cause the system to self-reset. Note that until the DATA signal has gone high, the flip-flop in the upper right corner of the drawing has been cleared by reset signals and has never indicated to the program that the Receiver-Buffer-Full signal (RBFL1+) has been present. With the appearance of the data signal this flip-flop will be set anytime its clock input is triggered.

The data portion of the USRT works as follows: the 8 data lines appear on the right side of its symbol (RD1-RD8), with RD1 ordinarily being the least significant bit, but in any event being the first bit serially received. The bug contains a data output strobe which is not used and is tied high, pin 25. Upon the arrival of 8 bits, the internal serial register is transferred broadside into an internal holding register whose outputs are the RD1-8 bits. Simultaneously, the RDA1+ signal is raised, indicating that received data is available at the outputs of the USRT. This frees-up the internal shift register to continue receiving the next 8 bits without having produced an overrun condition. Logic external to the USRT is required to furnish a Received-Data-Available-Reset signal (RDAR1+) to the bug in order to indicate that its output buffer has been emptied

and new serial data may be transferred to it when received. The specifications of that pulse are 200 ns, minimum, and a 400 ns oneshot is provided, shown in the upper right corner of the drawing. Its output signals the USRT that its buffer has been transferred into the 8-bit register to the right of the USRT symbol, by the leading edge of the 400 ns pulse, RDAR1+. This transition is allowed to take place only when that external buffer has been emptied by the program as indicated by the low state of Receiver-Buffer-Full, RBFL1+. At the transition to data mode, this signal is low, and therefore the pin 1 input of the 400 ns oneshot is primed. RDA1+ goes high, triggering the oneshot and producing an immediate RDAR1+. The extreme slowness of the LSI bug prevents any possibility of a race condition. The RDA signal drops substantially after RDAR. At the trailing edge of the 400 ns pulse, the Receiver-Buffer-Full flip-flop is triggered on, since its D input is high. This signals the program that received data is available in the outputs of the 8-bit holding register. The program is presumably in a loop reading this data register, searching for a 1 in this Ready bit, bit 15. Each time it reads the data register, the 60 ns oneshot is triggered by RDAT1-. Its output however, produces no Clear-Receiver-Buffer-Full signal (CRBF1-) because the pulse is gated off by DAS15+ as long as "old" data is still in the buffer. DAS15 is the synchronized Receiver-Buffer-Full signal that is put on data bit 15 during this read. Only when RBFL has been in the 1 state, signifying new data, will DAS15+ be high, which causes a reset to the Receiver-Buffer-Full flip-flop. At that point, RBFL1+ goes low again, priming the 400 ns oneshot.

SLI

Note that due to program timing there may be a substantial delay between receiver-buffer-full and the reading-out of that 8-bit buffer. Under these conditions, the 400 ns oneshot will have its pin 2 input high from RDA1+ and be waiting for the pin 1 input to drop. In that case the data will be available at the output of the USRT and will be transferred into the second rank immediately upon program readout of the data already there. 400 ns seconds later the receiver-buffer-full flip-flop will be set once again. Thus the program has nearly two full serial byte times in which to empty the buffer before data will have been lost. The loss of data is indicated in the program by Data Bit 8, Receiver Overrun Error. The USRT produces an ROR signal for Receiver Overrun whenever it is forced to transfer data from its serial register to its output holding register prior to an emptying of that register, signaled by RDAR. This overrun causes a rising transition of ROR1+ and sets the overrun flip-flop in the bottom center of the drawing. Note that this flip-flop was

held in the reset condition until data mode had been achieved, and since data mode is disabled whenever the system is reset, the overrun flip-flop is similarly disabled.

Above the overrun flip-flop is the parity error flip-flop, which behaves in a similar manner. The program has the ability to specify whether parity checking is desired. If it is so indicated, and if a parity error has been detected, the RPE1+ signal rises setting the parity error flip-flop. It too is cleared by the reset signal indirectly through the data flip-flop. Turning to the lower left corner of the drawing, reset conditions are carried out by a oneshot specified to be 1 ms in duration or longer. The bit assignment chart shows that control bit zero is the receiver reset bit; hence data bit 0 and the write-control signal are gated together producing RRES1-. This signal, or master reset, or the previously mentioned noise signal, fires the 1.5 ms oneshot. Its output is used to reset the USRT causing it to resume searching for sync characters, sets all the bits in the First-Character-Received shift register, and provides a number of miscellaneous reset signals throughout the drawing.

SLI24

Drawing 24 contains the logic surrounding the transmit portion of the USRT bug. It also shows the modem interconnections at the left side of the drawing, the RS232-to-TTL level shifters immediately to the right of the modem connector, and the various bits of the control register in the upper right corner. In the upper portion, a 555 oscillator is provided for internal testing, and immediately below it is a 74157 bug used to bring about internal Loop-Back Mode for self-testing. To the right of the LSI bug is a holding register (a 6-bit and a 4-bit bug) and 3 gates used to decode the upper 2 of these 10 bits. The control circuitry for that is at the rightmost part of the drawing.

The input connector is shown at the left side of the drawing. With the exception of the two clock and the two data signals, all signals are mode and status bits for controlling and obtaining slow speed information from the modem. These are passed through directly to the program in the control and status words and may be used or ignored as is appropriate for the modem in use and the modem protocol specified. Their functions are described in some detail in the functional specification and in EIA Specification RS232. The interface circuits are standard

RS232 drivers and receivers, both of which invert their signals. Status and control signals are high in the ON or assertion case, and low when gated OFF. Data signals are 1 when low and 0 when high, and the transitions in data are specified to take place at the positive transition of the clock pulses. Data strobing on input therefore, is done at the negative transition of the clock pulse. The telecommunication terms "mark" and "space" refer to 1 and 0 of the data, respectively, and a modem leaves its data output in the marking or low state in the absence of data.

The 4 flip-flops in the upper right corner are cleared by master reset, and are read or cleared by the program as it writes the appropriate ones and zeros to the control register. The name of each function is written next to each flip-flop. The loop test function will be described later. The two states of control bit 7 are 7-bits-plus-parity in the ONE case, and 8-bits-and-no-parity in the ZERO case. The output of the flip-flop is connected to two of the mode bits of the USRT, as explained in its data sheet. The remaining control bits to the USRT are grounded or tied high as is appropriate for the application.

The USRT has 8 data bits into it, and a choice of 3 strobes determining where these data bits will go. As in the receive case, the USRT has a shift register connected directly to its serial output and clock, and an internal parallel holding register which is automatically transferred to this serial register after 8 bits have been shifted out. At that point a buffer empty signal from the USRT transmitter, TBMT1+, is asserted, indicating to the logic that it may load the data inputs from an external holding register, located to the right of the USRT symbol.

In addition to the data strobe, TDS1+, there are two other strobes into the bug. They provide DC sets and are independent of both the clock and the Transmitter-Buffer-Empty output signal. RSS1+ is used to specify that the 8 bits are to be placed in a holding register inside the bug, used for comparison with the incoming data stream for character synchronization, as described above in SLI23. The second, TSS1+, is analogous to it. A second holding register specifies a given sync character which will be transmitted serially on the line in the absence of data. This is equivalent to an "underflow" condition, and in those protocols which allow it, will permit the program to fall behind without losing character sync. The bit assignment chart shows that these are derived from writing data bits 8 and 9, respectively. In the

bits 8 and 9, respectively. In the absence of either of these bits, the data bits are considered to be transmitted data, and strobe TDS1+ is asserted instead. Data bits 8 and 9 are carried along with the 8 valid data bits so that there are 10 bits of storage in the external parallel register. This provides total synchronization of what otherwise would be control signals. The 2 outputs are decoded into the three possibilities by the 3 and-gates located to the right of the USRT. It is perfectly permissible to write both transmitted and received sync characters simultaneously.

The program, by polling status bit 15, can determine that the transmitter buffer is empty and it may therefore do a WRITE into the data register. When power is first applied, it takes several byte times for the system to reach stability. The transmitter portion of the SLI bug cannot be reset, so some number of random bits is transmitted. At the end of that, TBMT is asserted and the previously cleared (or program-set) contents of the holding register are transferred into the SLI bug by the 400 ns oneshot. Ordinarily, the first 2 words written by the program to the bug are the specified sync characters.

Two conditions are necessary to trigger the 400 ns oneshot and generate the strobe: the holding register must contain information, as indicated by TFUL1+; and the USRT transmitter buffer must be empty, as indicated by TBMT1+. The 400 ns pulse strobes the 3 and-gates, determining the destination of the 8 data bits, and also clears the flip-flop in the lower right corner asserting the Transmitter-Buffer-Empty signal. This flip-flop remains cleared until the program writes a new data word, at which time it is set by WDAT1+, which is derived from the address decoding on drawing 21. This strobes the INFIBUS data lines into the 10-bit holding register, and the buffer remains "full" until these bits have been transferred into the USRT.

Above the USRT symbol, is a 74157. It is a 4-bit multiplexer or half adder whose strobe is always asserted. Its function is to allow the two serial data and the two serial clock signals to be connected directly to the modem or to allow loop testing when the TEST1+ signal is present at the top of the multiplexer. When this select line is low, the modem signals are applied to the USRT. When it is high however, the USRT data signals are connected together and the two clock signals are connected to a free-running oscillator shown just above the multiplexer. This square wave runs at about 12KHz, and its

output also is made available on the interface plug pin 26, which is not used in connecting to modems. A properly connected looping plug can therefore be plugged into the edge card connector and allow testing of the drivers as if a modem were providing this clock signal. See Appendix D.

Note that the transmitted data signal to the modem is inhibited except when the modem has asserted Clear-To-Send. This is done because certain half-duplex modems become confused when their data lines are not held at mark when they are in receive mode. Without this signal, the data line would presumably continue to accept sync characters, since the transmit clock will free run even in the absence of the Clear-To-Send signal with certain modems. The looping plug suggested above connects Clear-To-Send to Request-To-Send, and the program should control the latter appropriately. If the modem in use does not provide a CTS signal, a jumper within the modem or its interconnecting cable should be provided to hold it ON.

SLI25 and SLI26

These two drawings are logically identical to drawings 23 and 24. The signal names in all cases end in "2", where in former cases they ended in "1", indicating that it is modem 2 and its logic that are involved. The loop test circuitry is independently controlled, but shares the common clock.

FIRST UNIT	XXXØ	2	4	6	
SECOND UNIT	8	A	C	E	
BIT	DEVICE TYPE (DT)	STATUS (ST)	CONTROL (CR)	DATA READ (DR)	DATA WRITE (DW)
15	Ø	TRANS BUFFER EMPTY		INPUT DATA READY	
14	Ø	SYN TRANSMITTED		SYN RECEIVED	
13	Ø				
12	Ø				
11	Ø				
10	1	CLEAR TO SEND	REQ. TO SEND		
9	Ø	CARRIER DETECT	LOOP TEST	RCVR. PARITY ERROR	STORE TRANS SYN
8	Ø	DATA SET READY	DATA TERMINAL READY	RCVR. OVERRUN ERROR	STORE RCVR SYN
7	BAUD RATE CODE		7 BIT-PLUS-PARITY MODE		
6	BAUD RATE CODE		(RESERVED FOR EVEN PARITY MODE)		
5					
4					
3					
2					
1					
Ø			RECEIVER RESET*		

8 BIT DEVICE TYPE

FIRST CHAR RCD (TEST BIT Ø FOR EVEN)

INPUT DATA BYTE

OUTPUT DATA BYTE

*CRØ WILL ALWAYS BE Ø WHEN READ

Appendix A. SLI Bit Assignments

Appendix B. General Notes About Logic Drawings

1. Logic names tend to be given in their TRUE state for positive logic, e.g., when a write cycle is taking place, RITE+ will be high and RITE- will be low.

2. VOLTS- is ground (logic-low), named this way for the convenience of the program that generates the paper tape for the automatic wirewrap machine.

3. VOLTS+ similarly is logic-high, actually a 1K resistor to Vcc, driving up to 20 loads. Since several are required, VOLT1+, VOLT3+, etc., are used, designating on which drawing most of the loads are found.

4. Signals that leave a drawing show the destination drawings as [20,22], etc. On those drawings, for example, the drawing containing the logic source is designated (21).

5. INFIBUS signals usually have names ending in B, such as RITEB-.

6. The INFIBUS connector is designated P1 on the side that Lockheed calls P1A, and P2 on Lockheed's side P1B. The "outside" edge connector is designated J1 and J2 (1 through 55) for LEC's J1A and J1B respectively.

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A Standard Microsystems Company

COM2601

Universal Synchronous Receiver/Transmitter

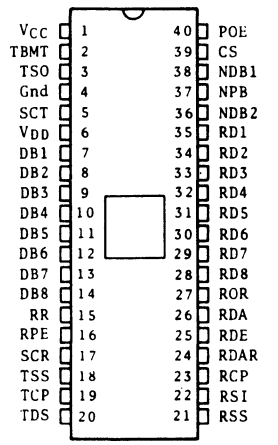
FEATURES

- **STR, BSC**—Bi-sync and interleaved bi-sync modes of operation
- **Fully Programmable**—data word length, parity mode, receiver sync character, transmitter sync character
- **Full or Half Duplex Operation**—can receive and transmit simultaneously at different baud rates
- **Fully Double Buffered**—eliminates need for precise external timing
- **Directly TTL Compatible**—no interface components required
- **Tri-State Data Outputs**—bus structure oriented
- **IBM Compatible**—internally generated SCR and SCT signals
- **High Speed Operation**—250K baud, 200ns strobes
- **Low Power**—300mW
- **Input Protected**—eliminates handling problems
- **Hermetic Dip Package**—easy board insertion

GENERAL DESCRIPTION

The Universal Synchronous Receiver/Transmitter is an MOS/LSI monolithic circuit that performs all the receiving and transmitting functions associated with synchronous (STR, BSC, Bi-sync, and interleaved bi-sync) data communications. This circuit is fabricated using SMC's P-channel low voltage oxide-nitride technology, allowing all inputs and outputs to be directly TTL compatible. The duplex mode, baud rate, data word length, parity mode, receiver sync character, and transmitter sync character are independently programmable through the use of external controls. The USR/T is fully double buffered and internally generates the sync character received and sync character transmitted signals. These programmable features provide the user with the ability to interface with all synchronous peripherals.

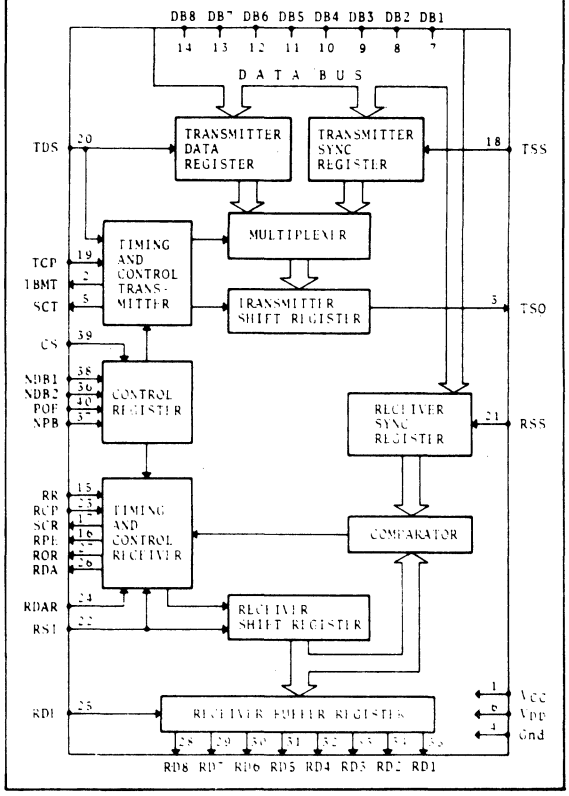
Pin Configuration



PACKAGE: 40-Pin D.I.P.

SLI

Functional Block Diagram



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, V_{CC}	+0.3 V
Negative Voltage on any Pin, V_{CC}	-25 V

* Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A=0-+70°C, V_{CC}=+5V±5%, V_{DD}=-12V±5%, unless otherwise noted)

Parameter	Min	Typ	Max	Unit	Conditions
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	V_{DD}		0.8	V	
High-level, V_{IH}	V_{CC}-1.5		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}		0.2	0.4	V	I_{OL} = 1.6mA
High-level, V_{OH}	2.4	4.0		V	I_{OH} =-100µA
INPUT CURRENT					
Low-level, I_{IL}			1.6	mA	see note 1
OUTPUT CURRENT					
Leakage, I_{LO}			-1	µA	RDE=V_{IL}, 0≤V_{OUT}≤+5V
Short circuit, I_{OS}**			10	mA	V_{OUT} = 0V
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = V_{CC}, f = 1MHz
OUTPUT CAPACITANCE					
All outputs, C_{OUT}		10	20	pf	R_{DE} = V_{IL}, f = 1MHz
POWER SUPPLY CURRENT					
I_{CC}			20	mA	All outputs = V_{OH}
I_{DD}			15	mA	
A.C. CHARACTERISTICS					T_A =+25°C
CLOCK FREQUENCY	DC		250	KHz	RCP, TCP
PULSE WIDTH					
Clock	1			µs	RCP, TCP
Receiver reset	1			µs	RR
Control strobe	200			ns	CS
Transmitter data strobe	200			ns	TDS
Transmitter sync strobe	200			ns	TSS
Receiver sync strobe	200			ns	RSS
Receiver data available reset	200			ns	RDAR
INPUT SET-UP TIME					
Data bits	0			ns	DB1-DB8
Control bits	0			ns	NPB,NDB2,NDB1,POE
INPUT HOLD TIME					
Data bits	0			ns	DB1-DB8
Control bits	0			ns	NPB,NDB2,NDB1,POE
STROBE TO OUTPUT DELAY					Load =20pf+1 TTL input
Receive data enable		180	250	ns	RDE: T_{PD1}, T_{PD0}
OUTPUT DISABLE DELAY		100	250	ns	RDE

** Not more than one output should be shorted at a time.

NOTES:

1. Under steady state condition no current flows for TTL or MOS interfacing. A switching current of 1.6 mA maximum flows during a high to low transition of the input.
2. The tri-state output has 3 states:
   1) low impedance to V_{CC}
   2) low impedance to GND
   3) high impedance OFF ≅ 10M ohms
   The OFF state is controlled by the RDE input.

DESCRIPTION OF PIN FUNCTIONS

Pin No.	Symbol	Name	Function
1	V_{CC}	Power Supply	+5 volt Supply
2	TBMT	Transmitter Buffer Empty	This output is at a high-level when the transmitter data buffer register may be loaded with new data.
3	TSO	Transmitter Serial Output	This output serially provides the entire transmitted character. This character is extracted from the transmitter data buffer register provided that a TDS pulse occurs during the presently transmitted character. If TDS is not pulsed, the next transmitted character will be extracted from the transmitter sync register.
4	GND	Ground	Ground
5	SCT	Sync Character Transmitted	This output is set high when the character loaded into the transmitted shift register is extracted from the transmitter sync register, indicating that the TDS was not pulsed during the previously transmitted character. This output is reset low when the character to be transmitted is extracted from the transmitter data buffer register. This can only occur if TDS is pulsed.
6	V_{DD}	Power Supply	-12 volt Supply
7-14	DB1-DB8	Data Bus Inputs	This 8 bit bus inputs information into the receiver sync register under control of the RSS strobe, into the transmitter sync register under control of the TSS strobe, and into the transmitter data buffer register under control of the TDS strobe. The strobes operate independently of each other. Unused bus inputs should be at a high level. The LSB should always be placed on DB1.
15	RR	Receiver Reset	This input should be pulsed to a high-level after power turn-on. This resets the RDA, SCR, ROR, and RPE outputs to a low-level. The transitior of the RR input from a high-level to a low-level sets the receiver into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the SCR output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded int the receiver buffer register.
16	RPE	Receiver Parity Error	This output is a high-level if the received character parity bit does not agree with the selected parity.

Description of Pin Functions (cont.)

Pin No.	Symbol	Name	Function
17	SCR	Sync Character Received	This output is set high each time the character loaded into the receiver buffer register is identical to the character in the receiver sync register. This output is reset low the next time the receiver buffer register is loaded with a character which is not a sync character.
18	TSS	Transmitter Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter sync register.
19	TCP	Transmitter Clock	The positive going edge of this clock shifts data out of the transmitter shift register, at a baud rate equal to the TCP clock frequency.
20	TDS	Transmitter Data Buffer Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the transmitter data buffer register.
21	RSS	Receiver Sync Strobe	A high-level input strobe loads the character on the DB1-DB8 lines into the receiver sync register.
22	RSI	Receiver Serial Input	This input accepts the serial bit input stream.
23	RCP	Receiver Clock	The negative-going edge of this clock shifts data into the receiver shift register, at a baud rate equal to the RCP clock frequency.
24	RDAR	Receiver Data Available Reset	A high-level input resets the RDA output to a low-level.
25	RDE	Received Data Enable	A high-level input enables the outputs (RD8-RD1) of the receiver buffer register
26	RDA	Receiver Data Available	This output is at a high-level when an entire character has been received and transferred into the receiver buffer register.
27	ROR	Receiver Over-Run	This output is at a high-level if the previously received character is not read (RDA not reset) before the present character is transferred into the receiver buffer register.
28-35	RD8-RD1	Receiver Data Output	These are the 8 tri-state data outputs enabled by RDE. Unused data output lines, as selected by NDB1 and NDB2, have a low level output, and received characters are right justified, i.e. the LSB always appears on the RD1 output.
36, 38	NDB2, NDB1	Number of Data	These 2 inputs are internally decoded to select either 5, 6, 7, or 8 data bits/character as per the following truth table: NDB2 NDB1 data bits/character L L 5 L H 6 H L 7 H H 8

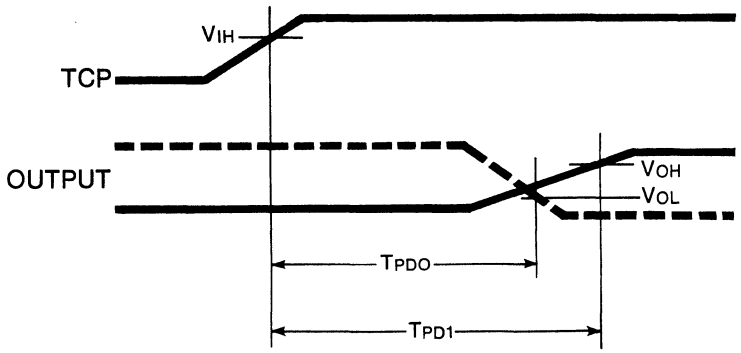
Description of Pin Functions (cont.)

Pin No.	Symbol	Name	Function
37	NPB	No Parity Bit	A high-level input eliminates the parity bit from being transmitted. In addition, it is necessary that the received character contain no parity bit. Also, the RPE output is forced to a low-level. See pin 40, POE.
39	CS	Control Strobe	A high-level input enters the control bits (NDB1, NDB2, POE, and NPB) into the control bits register. This line may be strobed or hard wired to a high-level.
40	POE	Odd/Even Parity Select	The logic level on this input, in conjunction with the NPB input, determines the parity mode for both the receiver and transmitter, as per the following table:

NPB	POE	MODE
L	L	odd parity
L	H	even parity
H	X	no parity
		X=don't care

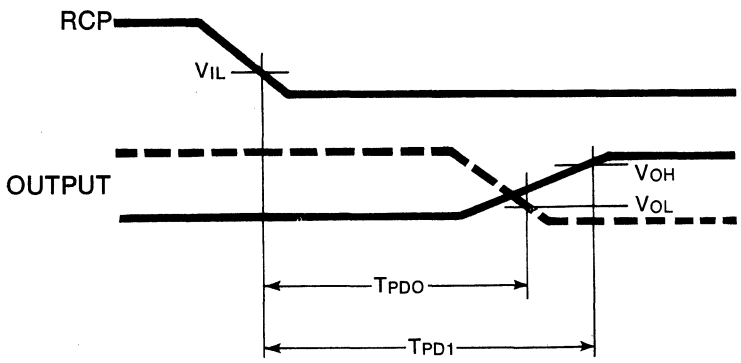
ADDITIONAL TIMING INFORMATION
(Typical Propagation Delays)

Transmitter



OUTPUT	TPDO	TPD1	UNITS
TBMT	NA	2.0	μs
SCT	1.0	1.5	μs
TSO	1.0	1.0	μs

Receiver



OUTPUT	TPDO	TPD1	UNITS
RDA	NA	1.0	μs
ROR	2.0	2.5	μs
RPE	2.0	2.5	μs
SCR	2.0	2.5	μs
RD1-RD8	2.5	2.5	μs

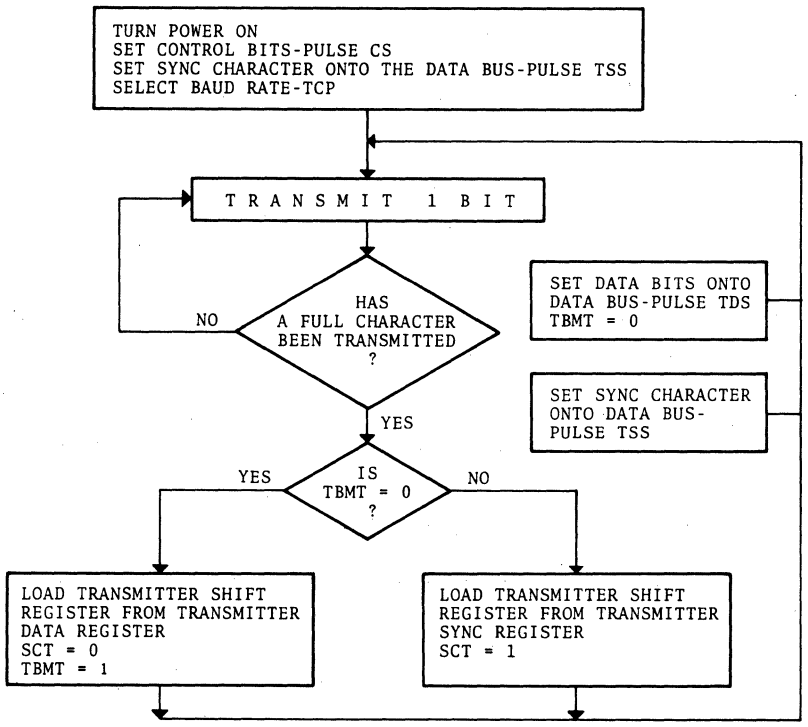
DESCRIPTION OF OPERATION - RECEIVER/TRANSMITTER

The input clock frequency for the receiver is set at the desired receiver baud rate and the desired receiver sync character (synchronous idle character) is loaded into the receiver sync register. When the Receiver Reset input transitions from a high-level to a low-level the receiver is set into the search mode (bit phase). In the search mode the serially received data bit stream is examined on a bit by bit basis until a sync character is found. A sync character is found, by definition, when the contents of the receiver sync register and the receiver shift register are identical. When this occurs the Sync Character Received output is set high. This character is then loaded into the receiver buffer register and the receiver is set into the character mode. In this mode each character received is loaded into the receiver buffer register. The receiver provides flags for Receiver Data Available, Receiver Over Run, Receiver Parity Error, and Sync Character Received. Full double buffering eliminates the need for precise external timing by allowing one full character time for received data to be read out.

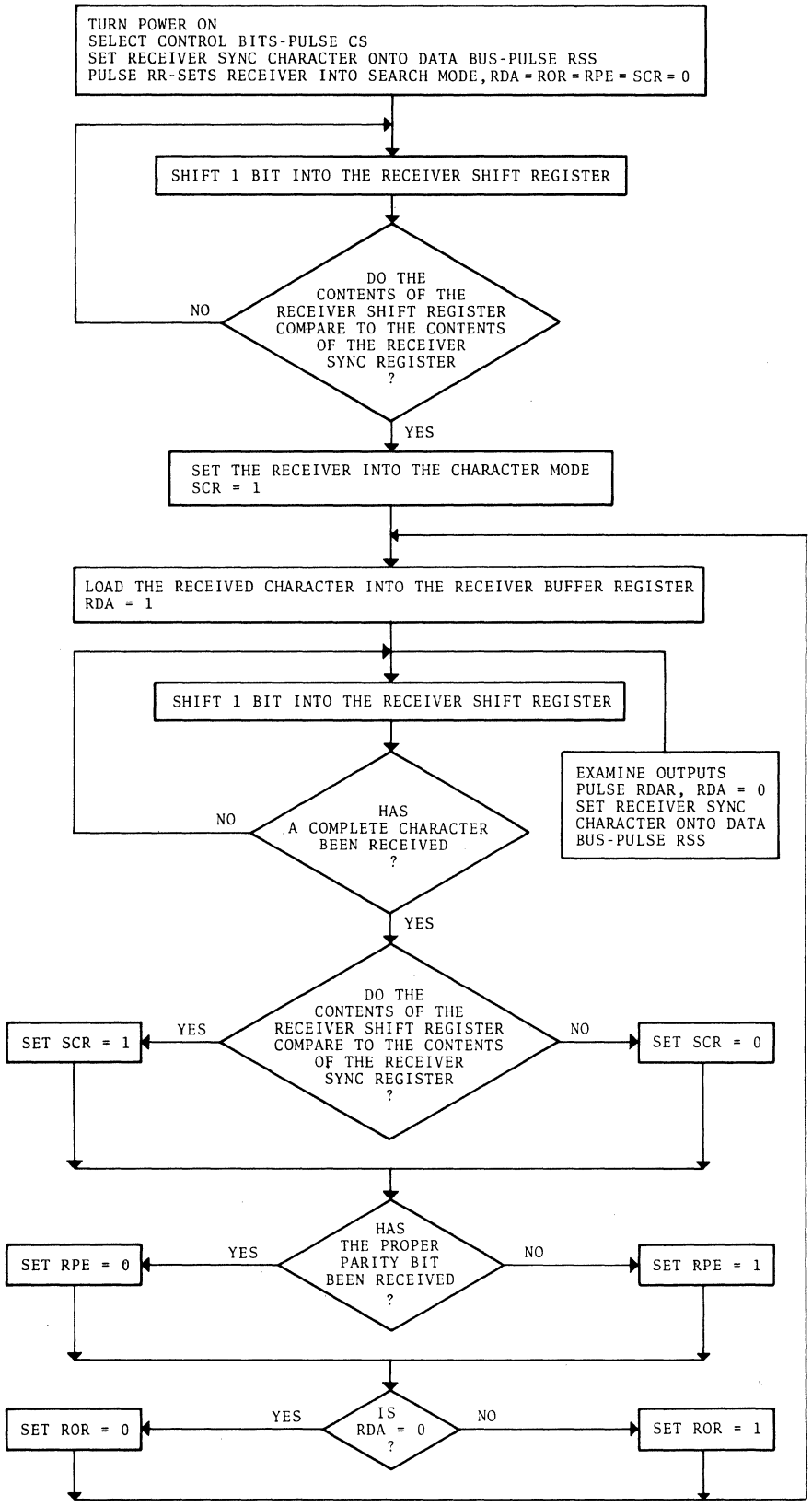
The input clock frequency for the transmitter is set at the desired baud rate and the desired transmitter sync character is loaded into the transmitter sync register. Internal logic decides if the character to be transmitted out of the transmitter shift register is extracted from the transmitter data register or the transmitter sync register. The next character transmitted is extracted from the transmitter data register provided that a Transmitter Data Strobe pulse occurs during the presently transmitted character. If the Transmitter Data Strobe is not pulsed, the next transmitted character is extracted from the transmitter sync register and the Sync Character Transmitted output is set to a high level. Full double buffering eliminates the need for precise external timing by allowing one full character time to load the next character to be transmitted.

There may be 5, 6, 7, or 8 data bits and odd/even or no parity bit. All inputs and outputs are directly TTL compatible. Tri-state data outputs levels are provided for the bus structure oriented signals. Input strobe widths of 200ns, output propagation delays of 250ns, and receiver/transmitter rates of 250K baud are achieved.

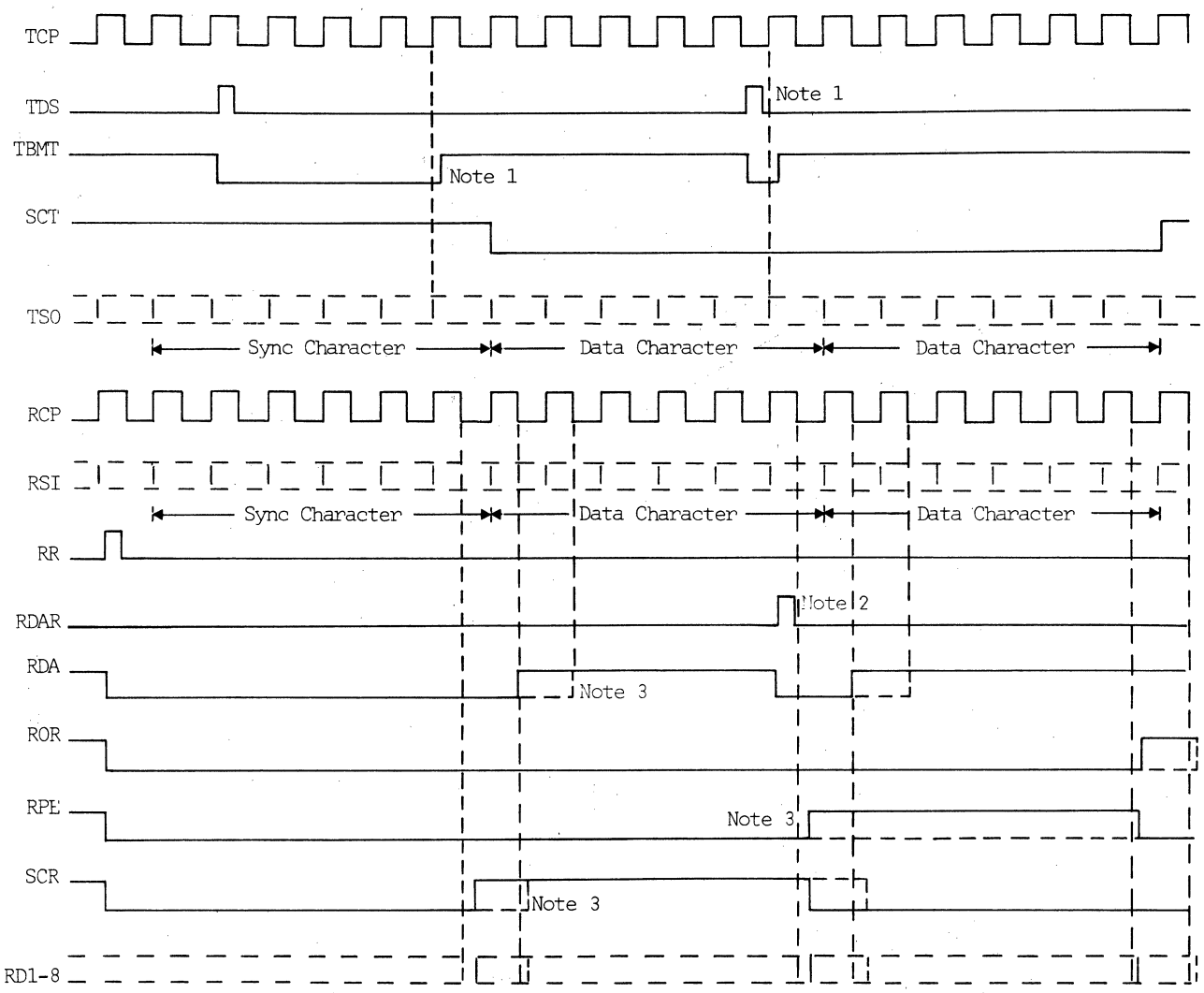
FLOW CHART - TRANSMITTER



FLOW CHART - RECEIVER



USRT TIMING DIAGRAM



NOTE 1
The transmitter shift register is loaded with the next character at the positive clock transition corresponding to the leading edge of the last bit of the current character on the TSO output. TBMT is set high approximately two microseconds after this clock transition. If it is desired that the next character be extracted from the transmitter data register the leading edge of the TDS should occur at least one microsecond prior to this clock transition.

NOTE 2
In order to avoid an ROR indication the leading edge of the RDAR pulse should occur at least one microsecond prior to the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input.

NOTE 3
The ROR, RPE, SCR and RD1-RD8 outputs are set to their correct levels approximately two microseconds after the negative clock transition corresponding to the center of the first bit after the last data bit on the RSI input. The RDA output is set high at the next negative clock transition.

The solid waveforms correspond to a control register setting of 5 data bits and a parity bit. The dashed waveforms are for a setting of 6 data bits and no parity bit.

Am2812 / Am2812A • Am2813 / Am2813A

32 x 8-Bit and 32 x 9-Bit First-in First-out Memories

Advanced Micro Devices
Complex MOS Integrated Circuits

Distinctive Characteristics

- Completely independent read and write operations
- "Half-full" flag
- Am2812 has serial or parallel input and output
- Data rates up to 1 MHz

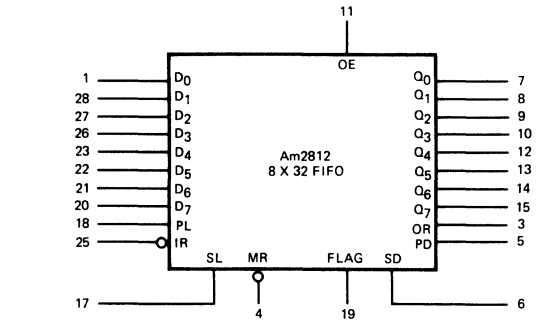
FUNCTIONAL DESCRIPTION

The Am2812 and Am2813 are 32 word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three-state outputs controlled by an output enable pin (OE). Data on the data inputs (D_i) are written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word. Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs (Q_i) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready (IR) signal indicates that the device is ready to accept data and also provides a memory full signal. Both the Am2812 and Am2813 have master reset inputs which clear all data from the device (reset to all LOWs), and a FLAG signal which goes HIGH when the memory contains more than 15 words.

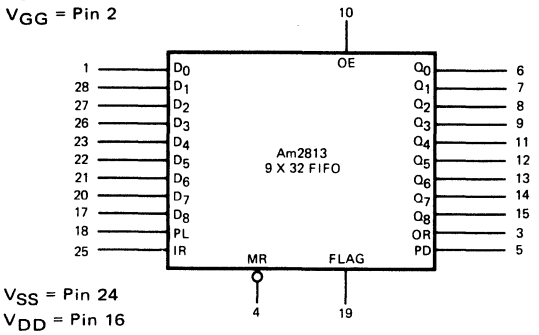
The Am2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is in reality an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the D_0 input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built-in parallel-to-serial converter, so that data can be shifted out of the Q_7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals, PL, IR, PD, and OR, are designed so that two FIFOs can be placed end to end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

LOGIC SYMBOLS



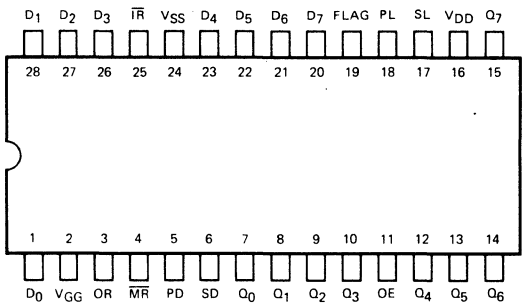
V_{SS} = Pin 24
V_{DD} = Pin 16
V_{GG} = Pin 2



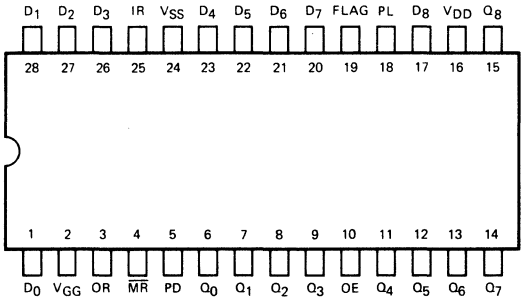
V_{SS} = Pin 24
V_{DD} = Pin 16
V_{GG} = Pin 2

CONNECTION DIAGRAMS
Top Views

Am2812



Am2813



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Frequency	Temperature Range	Am2812 Order Number	Am2813 Order Number
Hermetic DIP	500KHz	0°C to +70°C	AM2812DC	AM2813DC
Hermetic DIP	500KHz	−55°C to +125°C	AM2812DM	AM2813DM
Hermetic DIP	1MHz	0°C to +70°C	AM2812ADC	AM2813ADC
Hermetic DIP	1MHz	−55°C to +125°C	AM2812ADM	AM2813ADM

SLI

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{DD} Supply Voltage	V_{SS} −7V to V_{SS} +0.3V
V_{GG} Supply Voltage	V_{SS} −20V to V_{SS} +0.3V
DC Input Voltage	V_{SS} −10V to V_{SS} +0.3V

OPERATING RANGE

Part Number	Ambient Temperature	V_{SS}	V_{DD}	V_{GG}
Am2812DC, Am2812ADC Am2813DC, Am2813ADC	0°C to +70°C	5.0V ±5%	0V	−12V ±5%
Am2812DM, Am2812ADM Am2813DM, Am2813ADM	−55°C to +125°C	5.0V ±5%	0V	−12V ±5%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions		Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	I_{OH} = .300mA		V_{SS} −1.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 1.6mA				0.4	V
V_{IH}	Input HIGH Level			V_{SS} −1.0			V
V_{IL}	Input LOW Level					0.8	V
I_{IL}	Input Leakage Current	V_{IN} = 0V				1.0	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{SS} −1.0V		250			µA
V_{PUP}	Input Pull-up Initiation Voltage	(Note 2)	V_{SS} = MIN.			2.0	V
			V_{SS} = MAX.			2.2	V
V_{BAR}	Voltage at Peak Input Current	(Note 2)				V_{SS} −1.5	V
I_{BAR}	Maximum Input Current	(Note 2)				1.6	mA
I_{GG}	V_{GG} Current	T_A = 0°C to +70°C			14	22	mA
		T_A = −55°C to +125°C				27	
I_{DD}	V_{DD} Current	T_A = 0°C to +70°C			30	45	mA
		T_A = −55°C to +125°C				55	

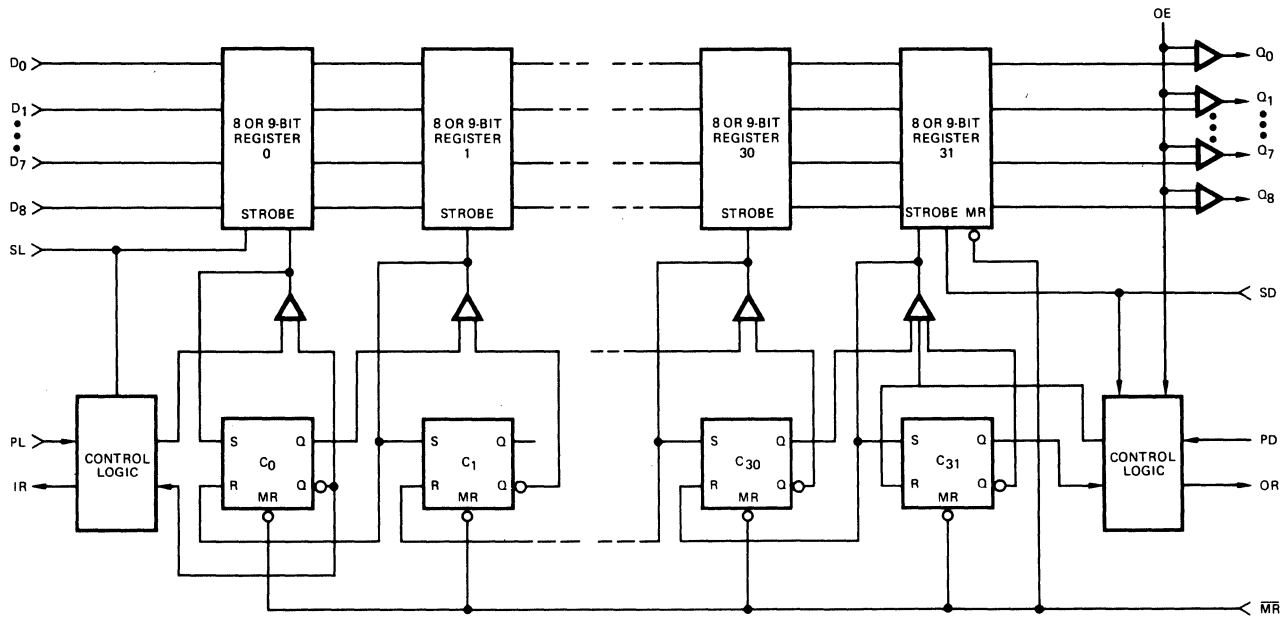
Notes: 1. Typical limits are at V_{SS} = 5.0V, V_{GG} = −12.0V, T_A = 25°C
2. Pull up circuit on Am2813 only. See graph of input V-I characteristics.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Conditions/Note	Test Conditions	Am2812 Am2813 Min.	Am2812 Am2813 Typ.	Am2812 Am2813 Max.	Am2812A Am2813A Min.	Am2812A Am2813A Typ.	Am2812A Am2813A Max.	Units
f_p	Maximum Parallel Load or Dump Frequency		0.5			1.0			MHz
t_{IR+}	Delay, PL or SL HIGH to IR In-Active		100	300	1100	80	300	450	ns
t_{IR-}	Delay, PL or SL LOW to IR Active		100	250	800	80	250	400	ns
$t_{pw}H(P)$	Minimum PL or PD HIGH Time				100			80	ns
$t_{pw}L(P)$	Minimum PL or PD LOW Time				100			80	ns
$t_{pw}H(S)$	Minimum SL or SD HIGH Time	Am2812 only			350			300	ns
$t_{pw}H(S)$	Minimum SL or SD LOW Time	Am2812 only			350			300	ns
$t_h(D)$	Data Hold Time			190	250		170	200	ns
$t_s(D)$	Data Set-Up Time	to PL			0			0	ns
		to SL			100			90	
t_{OR+}	Delay, PD or SD HIGH to OR LOW	OE HIGH	100	450	1100	100	350	520	ns
t_{OR-}	Delay, PD or SD LOW to OR HIGH	OE HIGH	100	400	850	100	300	470	ns
t_{PT}	Ripple through Time	FIFO Empty			10			8	µs
t_{DH}	Delay, OR LOW to Data Out Changing	PD = LOW	50	200		50	200		ns
t_{DA}	Delay, Data Out to OR HIGH	PD = HIGH	0	100		0	100		ns
t_{MRW}	Minimum Reset Pulse Width				400			400	ns
t_{DO}	Delay, OE LOW to Output OFF				400			400	ns
t_{EO}	Delay, OE HIGH to Output Active				400			400	ns
t_{DF}	Delay from PL or SL HIGH to Flag HIGH or PD or SD HIGH to Flag LOW			0.5	1.0		0.5	1.0	µs
CI	Input Capacitance				7			7	pF

Notes: 3. IR is active HIGH on Am2813 and active LOW on Am2812.
4. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

LOGIC BLOCK DIAGRAM



SLI

DESCRIPTION OF THE Am2812 and Am2813 FIFO OPERATION

The Am2812 and Am2813 FIFOs consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A "1" in a bit of the control register indicates that a data word is stored in the corresponding data register. A "0" in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of the control register contains a "1" and the (n+1)th bit contains a "0", then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit and clearing the n^{th} control register bit, so that the control flag moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are "empty" locations ahead of it. The fall through operation stops when the data reaches a register n with a "1" in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a LOW-to-HIGH transition on the parallel load (PL) input. A "1" is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now "busy", unable to accept more data. When PL next goes LOW, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This causes IR to go active, indicating the inputs are available for another data word.

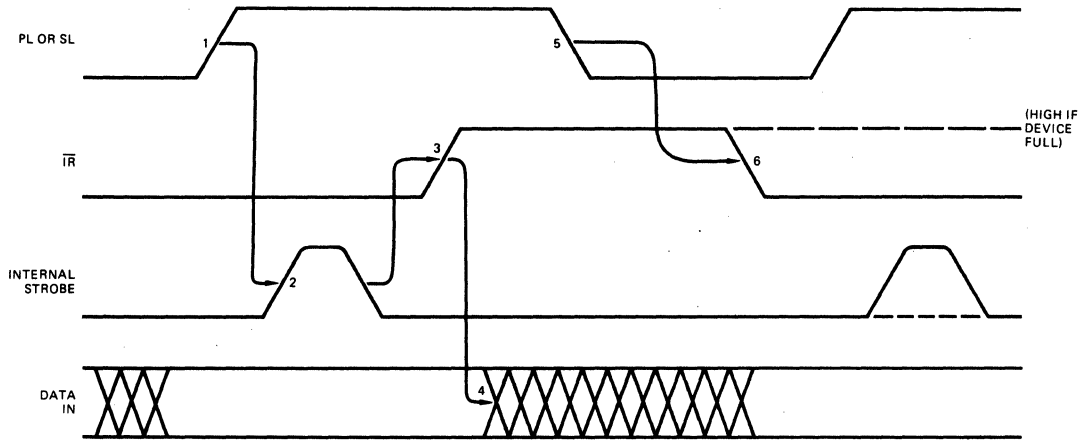
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A HIGH on OR indicates there is a "1" in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A LOW-to-HIGH transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes LOW, the "0" which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The "0" in the control register then "bubbles" back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes HIGH, OR will go LOW as before, but when PD next goes LOW, there is no data to move into the last location, so OR remains LOW until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes LOW, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFOs to operate together, as shown in the application on the last page.

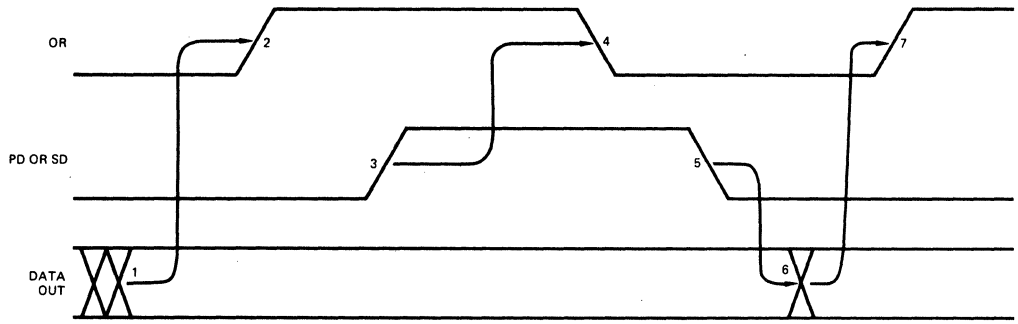
Because the input ready signal is active LOW on the Am2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two Am2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n Am2812s connected end-to-end store 31n+1 words (instead of 32n). The Am2813 stores 32n words in this configuration, because IR is active HIGH and does dump the last word written into the second device.

Am2812 TIMING DIAGRAM



Am2812 INPUT TIMING

When data is steady PL is brought HIGH (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes HIGH (3) and data may be changed (4). $\overline{IR}$ remains HIGH until PL is brought LOW (5); then $\overline{IR}$ goes LOW (6) indicating new data may be entered.



Am2812 OUTPUT TIMING

When data out is steady (1), OR goes HIGH (2). When PD goes HIGH (3), OR goes LOW (4). When PD goes LOW again (5), the output data changes (6) and OR returns HIGH (7).

The input and output timing diagrams above illustrate the sequence of control on the Am2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The Am2813 pattern is similiar, but IR is active HIGH instead of active LOW (shown in timing diagram on next page).

FLAG OUTPUT

A flag output is available on the Am2812 and Am2813 to indicate whether the FIFO is more or less than half full. The flag signal is generated by summing the "1s" in the control flip-flops, and therefore is not affected by the movement of data through the register. The flag signal goes HIGH when the 13th, 14th, 15th, or 16th word is loaded into the FIFO. It will remain HIGH until there are less than $15^{+1}/_{-2}$ words in the memory. It is always HIGH if there are more than 16 words in the FIFO.

RESET

An over-riding master reset ($\overline{MR}$) is used to clear all control register bits and set all the outputs LOW.

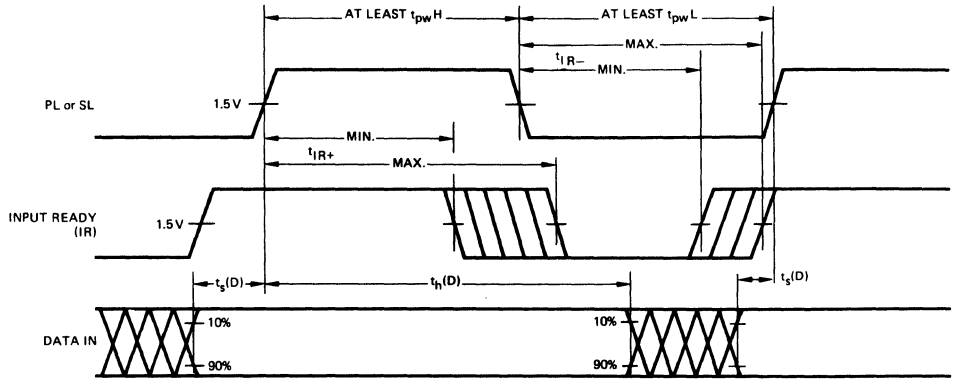
SERIAL INPUT AND OUTPUT (Am2812 ONLY)

The Am2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to D_0 input. Inputs D_1–D_7 must be grounded. The SL signal operates just like the PL input, causing IR to go HIGH and LOW as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they had been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

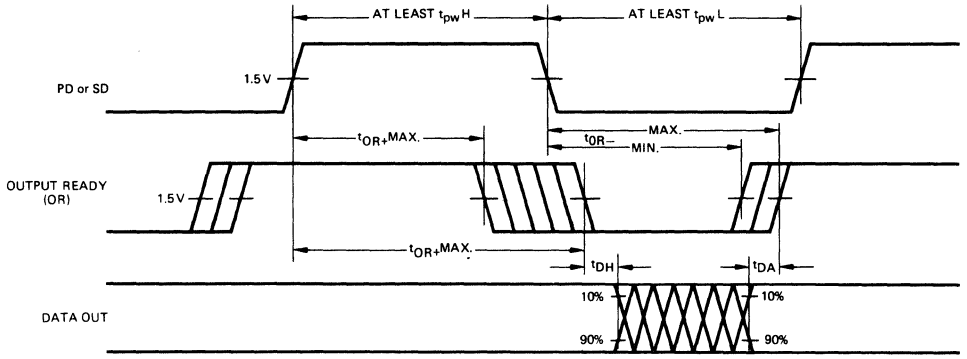
A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the O_7 output. OR moves HIGH and LOW with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and a new 8-bit word is brought to the output. OR will stay LOW if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.

TIMING DIAGRAM



Note: IR inverted on Am2812.



SLI

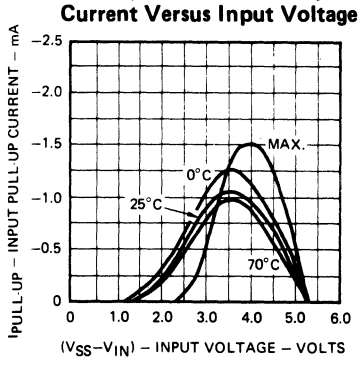
USER NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on PD, the OR signal always goes LOW before there is any change in output data and always stays LOW until after the new data has appeared on the outputs, so anytime OR is HIGH, there is good, stable data on the outputs.
3. If PD is held HIGH while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go HIGH for one internal cycle (at least t_{OR+}) and then will go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought LOW.
4. When the master reset is brought LOW, the control register and the outputs are cleared. $\overline{IR}$ goes HIGH and OR goes LOW. If PL is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and $\overline{IR}$ will return to the LOW state until PL is brought LOW. If PL is LOW when the master reset is ended, then $\overline{IR}$ will go HIGH but the data on the inputs will not enter the memory until PL goes HIGH.
5. The output enable pin inhibits dump commands while it is LOW and forces the Q outputs to a high impedance state.
6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.
7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

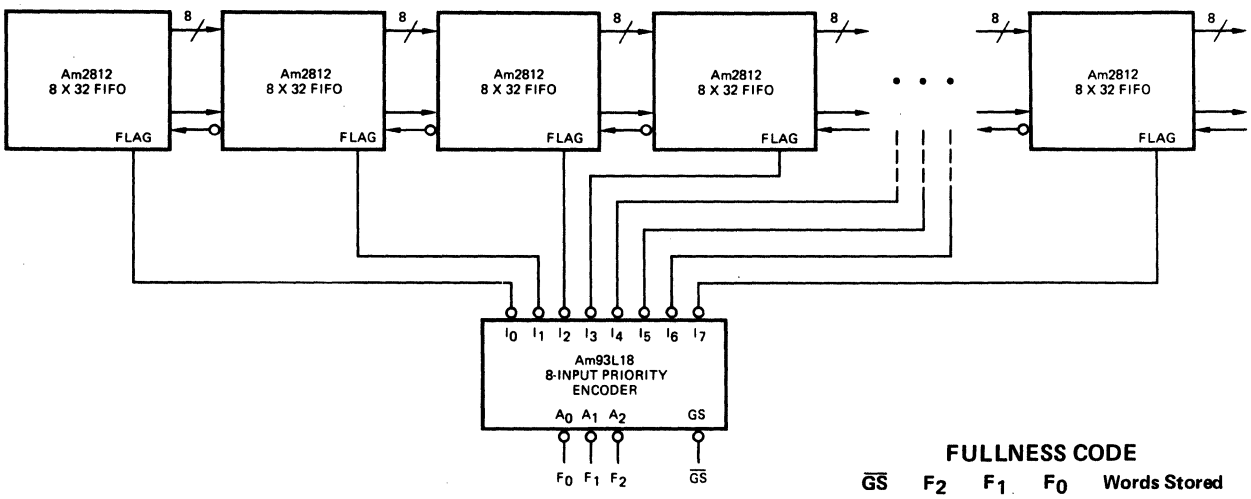
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
▨	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN

Pull-up Characteristic Input Current Versus Input Voltage



APPLICATIONS



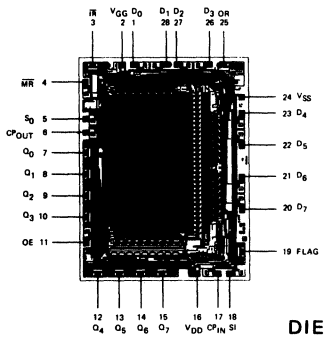
FULLNESS CODE

$\overline{GS}$	F_2	F_1	F_0	Words Stored
L	L	L	L	0 - 15
L	L	L	H	13 - 47
L	L	H	L	45 - 78
L	L	H	H	76 - 109
L	H	L	L	107 - 140
L	H	L	H	138 - 171
L	H	H	L	169 - 202
L	H	H	H	200 - 233
H	H	H	H	231 - 249

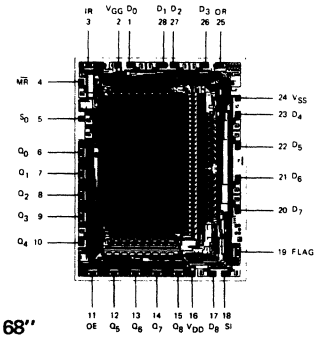
The Fullness Flags from Am2812 or Am2813 FIFOs can be encoded by an Am93L18 8-input priority encoder. The output code F_0-F_2 indicates the weight of the highest priority input which is LOW. GS is group signal; it is HIGH if all the inputs are HIGH.

Metallization and Pad Layouts

Am2812



Am2813



DIE SIZE .128" X 0.168"

ADVANCED
MICRO
DEVICES INC.
901 Thompson Place
Sunnyvale
California 94086
(408) 732-2400
TWX: 910-339-9280
TELEX: 34-6306

FAIRCHILD MOS INTEGRATED CIRCUIT 3341

GENERAL DESCRIPTION — The 3341 is a 64-word x 4-bit memory that operates in a first-in first-out (FIFO) mode. Inputs and the output are completely independent (no common clocks) making the 3341 ideal for asynchronous buffer applications.

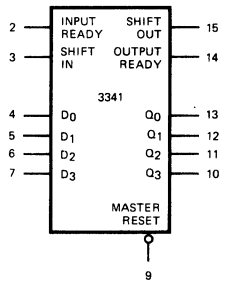
Special on chip input pull up circuits and bipolar compatible output buffers provide direct bipolar interfacing with no external components required. Control signals are provided so that both vertical and horizontal cascading may be easily achieved.

- **1 MHz SHIFT-IN SHIFT-OUT RATE**
- **DIRECT TTL/DTL INTERFACE AT INPUTS & OUTPUTS**
- **16-LEAD DUAL IN-LINE PACKAGE**
- **READILY EXPANDABLE IN EITHER DIRECTION**
- **ASYNCHRONOUS OR SYNCHRONOUS OPERATION**
- **CONVENIENT LEAD ORIENTATION FOR EASY BREADBOARDING**
- **UNIQUE TTL INPUT STAGE**

ABSOLUTE MAXIMUM RATINGS

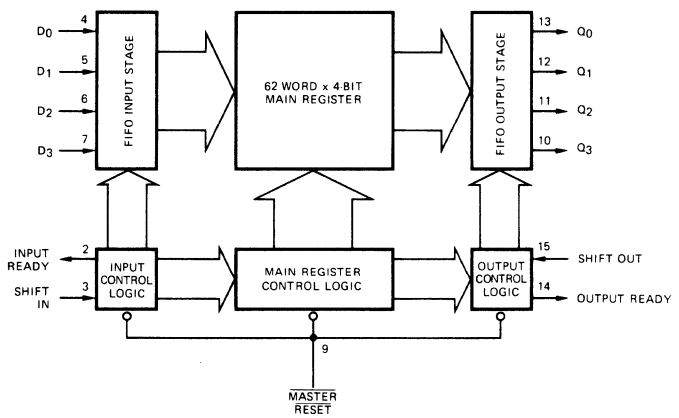
Storage Temp (T_S)	−65° C to +150° C
Operating Temp (T_A)	0° to +70° C
Voltage on all pins except outputs + V_{DD}	V_{SS} −24V to V_{SS} +0.3V
Voltage on V_{DD}	V_{SS} −7V to V_{SS} +0.3V

LOGIC SYMBOL

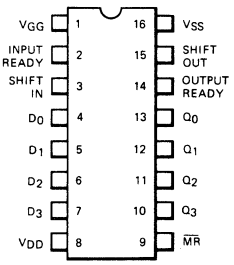


V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FUNCTIONAL DESCRIPTION:

DATA INPUT:

The four bits of data on the D_0 . . . D_3 inputs are entered into the first bit location when both Input Ready (IR) and Shift In (SI) are HIGH ($\approx V_{SS}$). This causes IR to go LOW ($\approx$GND), but data will stay locked in the first bit location until both IR and SI are brought LOW. Then data will propagate to the second bit location, provided the location is empty. When data is transferred, IR will go HIGH indicating that the device is ready to accept new data. If the memory is full, IR will stay LOW.

DATA TRANSFER:

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel, from input to the output of a previously empty device.

DATA OUTPUT:

When data has been transferred into the last cell, Output Ready (OR) goes HIGH, indicating the presence of valid data at the output pins Q_0 . . . Q_3. The transfer of data is initiated when both the Output Ready (OR) output from the device and the Shift Out (SO) input to the device are HIGH. This causes OR to go LOW; output data, however, is maintained until both OR and SO are LOW. Then the content of the adjacent (upstream) cell (provided it is full) will be transferred into the last cell, causing OR to go HIGH again. If the memory has been emptied, OR will stay LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

SPECIAL INPUT CHARACTERISTICS:

The 3341 uses a TTL compatible input pull up circuit. When going HIGH, the TTL driver must only provide 2.2V minimum which is then internally pulled up to V_{SS}.

When going LOW, the TTL driver must overcome a current barrier of $\leqslant$1.6mA at 2V. Once this is overcome, the input current drops to zero.

Unused inputs are stable in the HIGH state, but must be terminated when LOW, e.g., 1MΩ to V_{GG}.

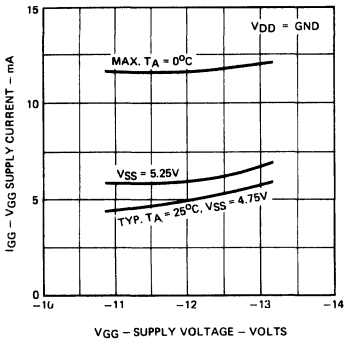
DC CHARACTERISTICS: V_{SS} = +5V $\pm$5%, V_{GG} = −12V $\pm$5%, V_{DD} = 0V, T_A = 0°C to 70°C (unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IH}	Input Voltage HIGH	V_{SS}−1.0			V	Notes 1 and 2
V_{IL}	Input Voltage LOW			0.8	V	Note 1
V_{OH}	Output Voltage HIGH	V_{SS}−1.0			V	I_{OH} = 0.3mA
V_{OL}	Output Voltage LOW			0.4	V	I_{OL} = 1.6mA
V_{PUP}	Input Pull Up Initiation Voltage			2.0	V	V_{SS} = 4.75V
V_{PUP}	Input Pull Up Initiation Voltage			2.2	V	V_{SS} = 5.25V
V_{BAR}	Peak Input Barrier Current Voltage Point			V_{SS}−1.5	V	
I_{IH}	Input Current HIGH	250			μA	Note 1, V_{IH} = V_{SS}−1.0 V
I_{LI}	Input Leakage Current			1.0	μA	Note 1, V_{IN} = 0V
I_{BAR}	Input Barrier Current			1.6	mA	Note 1
I_{GG}	V_{GG} Current		7.0	12	mA	
I_{DD}	V_{DD} Current		30	45	mA	
P_D	Power Dissipation			450	mW	

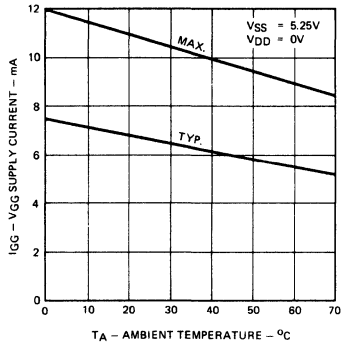
NOTES:
1. Inputs include D_0 – D_3. $\overline{\text{Master Reset}}$, Shift In, and Shift Out.
2. Internal pull up circuits are provided on all inputs to insure proper HIGH level.

ELECTRICAL CHARACTERISTICS

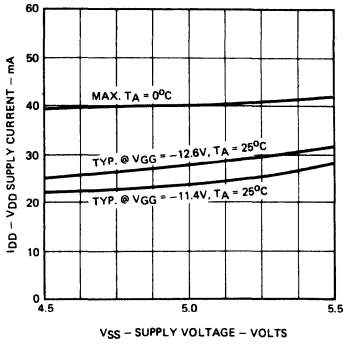
V_{GG} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



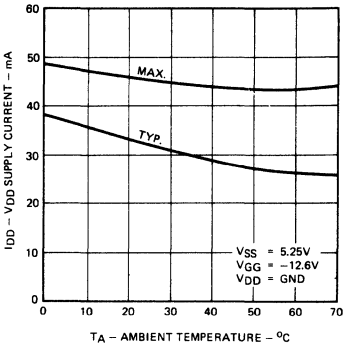
V_{GG} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



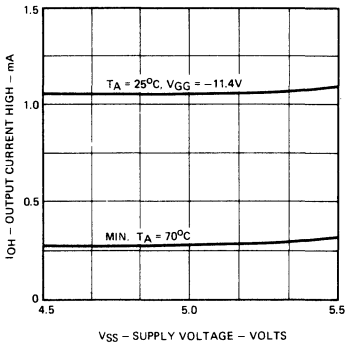
V_{DD} SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



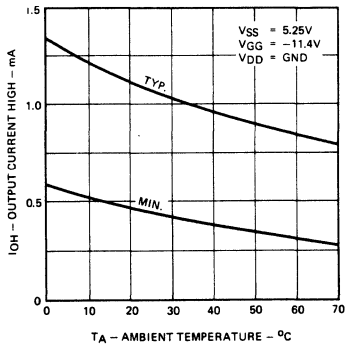
V_{DD} SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



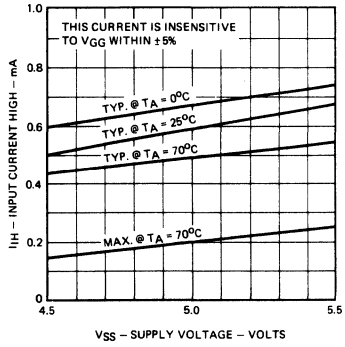
OUTPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE



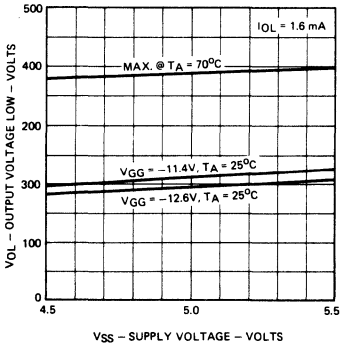
OUTPUT CURRENT HIGH VERSUS AMBIENT TEMPERATURE



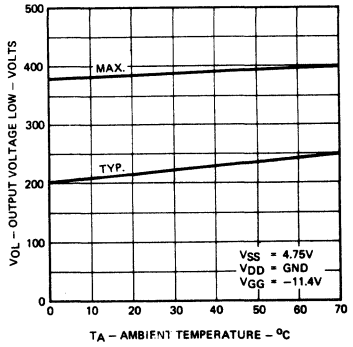
INPUT CURRENT HIGH VERSUS SUPPLY VOLTAGE



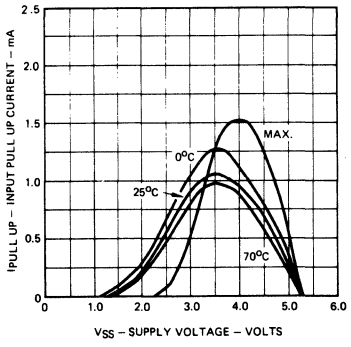
OUTPUT VOLTAGE LOW VERSUS SUPPLY CURRENT



OUTPUT VOLTAGE LOW VERSUS AMBIENT TEMPERATURE



INPUT PULL UP CURRENT VERSUS V_{SS} POWER SUPPLY CURRENT



SLI

AC CHARACTERISTICS: V_{SS} = +5V ± 5%, V_{DD} = 0V, V_{GG} = 12V ± 5%, T_A = 0°C to 70°C

SYMBOL	CHARACTERISTIC	0°C			70°C			UNITS	CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
t_{IR+}	Input Ready HIGH Time	90	200		155	300	550	ns	Fig. 1, Note 6
t_{IR-}	Input Ready LOW Time	138	250			300	550	ns	Fig. 1, Note 6
t_{0V+}	Control Overlap HIGH Time	70			100			ns	Figs. 1 and 2, Note 3
t_{0V-}	Control Overlap LOW Time	70			100			ns	Figs. 1 and 2, Note 3
t_{DSI}	Data Input Stable Time	400			400			ns	Fig. 1
t_{DD}	Data Input Delay Time	25						ns	Fig. 1, Note 5
t_{OR+}	Output Ready HIGH Time	90	200		155	300	500	ns	Fig. 2, Note 5
t_{OR-}	Output Ready LOW Time	170	300			450	850	ns	Fig. 2, Note 5
t_{PT}	Data Through-Put Time		10			10	32	μs	Note 4
t_{DH}	Data Hold Time	75						ns	Fig. 2, Note 5
t_{MRW}	Master Reset Pulse Width				400			ns	
t_{DA}	Data Output Available Time	0	30					ns	Fig. 2
C_I	Input Cap. of Data and Control Lines			7.0			7.0	pF	
C_{MR}	Input Cap. of $\overline{MR}$			15			15	pF	

NOTES:
3. Control signals include Input Ready, Shift In, Output Ready, and Shift Out.
4. This parameter defines total time from the time data is present at $D_0 - D_3$ to the time it is available at $O_0 - O_3$ with FIFO initially empty.
5. 1 TTL load +20 pF.

TIMING DIAGRAMS

INPUT TIMING

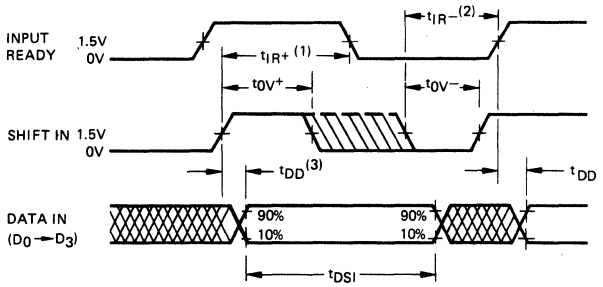


FIG. 1

Input data must remain stable during timing window t_{DSI}. Both SI and IR must be HIGH for t_{0V+}. Similarly, both SI and IR must be LOW for t_{0V-}.

NOTES:
1. t_{IR+} is referenced to the positive going edge of IR or SI, whichever occurs later.
2. t_{IR-} is referenced to the negative going edge of IR or SI, whichever occurs later.
3. t_{DD} is referenced to the positive going edge of IR or SI, whichever occurs later.
4. t_{0V+} is referenced to the positive going edge of IR or SI, whichever occurs later.
5. t_{0V-} is referenced to the negative going edge of IR or SI, whichever occurs later.
6. Data must be stable for t_{SDI} or t_{IR+}, whichever is shorter.

OUTPUT TIMING

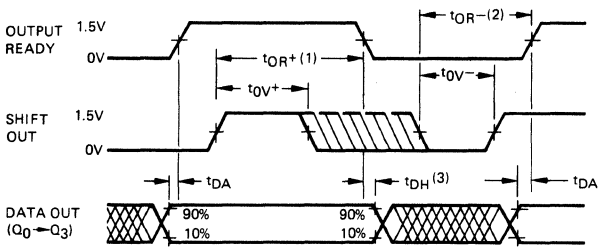


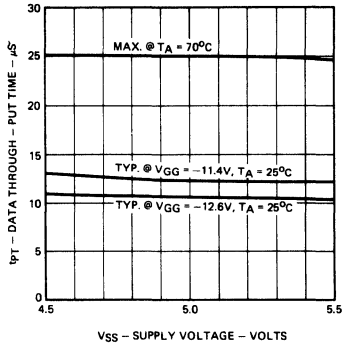
FIG. 2

Both SO and OR must be HIGH for t_{0V+}. Similarly both SO and OR must be LOW for t_{0V-}. Data will remain stable for t_{DH} after both SO and OR are LOW.

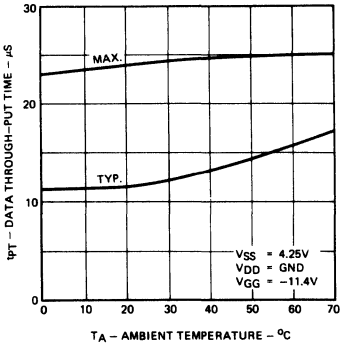
NOTES:
1. t_{OR+} is referenced to the positive going edge of OR or SO, whichever occurs later.
2. t_{OR-} is referenced to the negative going edge of OR or SO, whichever occurs later.
3. t_{DH} is referenced to the negative going edge of OR or SO, whichever occurs later.
4. t_{0V+} is referenced to the positive going edge of IR or SI, whichever occurs later.
5. t_{0V-} is referenced to the negative going edge of IR or SI, whichever occurs later.

ELECTRICAL CHARACTERISTICS

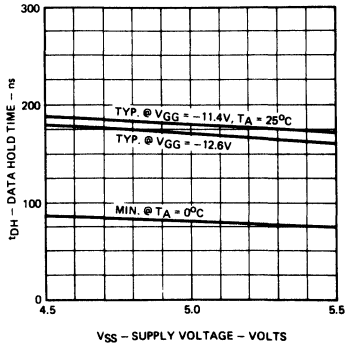
DATA THROUGH-PUT TIME VERSUS SUPPLY VOLTAGE



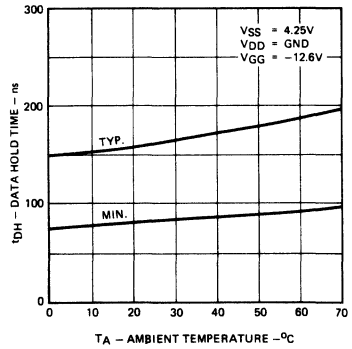
DATA THROUGH-PUT TIME VERSUS AMBIENT TEMPERATURE



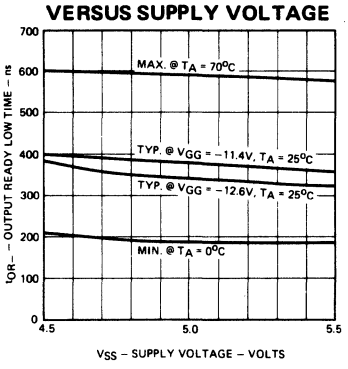
DATA HOLD TIME VERSUS SUPPLY VOLTAGE



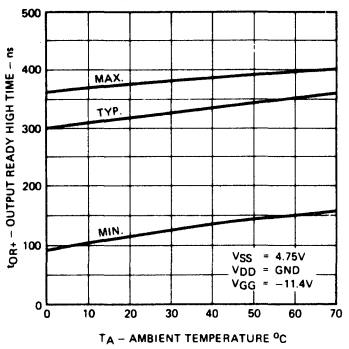
DATA HOLD TIME VERSUS AMBIENT TEMPERATURE



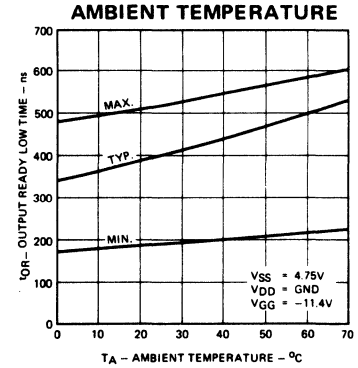
OUTPUT READY LOW TIME VERSUS SUPPLY VOLTAGE



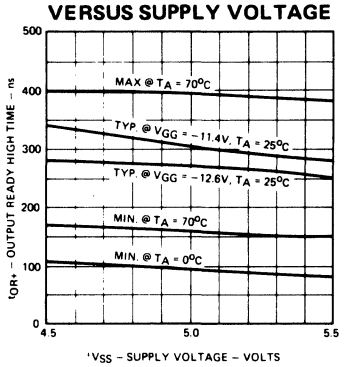
OUTPUT READY HIGH TIME VERSUS AMBIENT TEMPERATURE



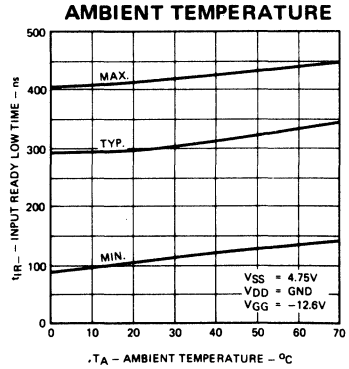
OUTPUT READY LOW TIME VERSUS AMBIENT TEMPERATURE



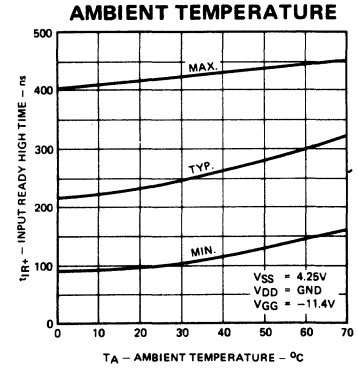
OUTPUT READY HIGH TIME VERSUS SUPPLY VOLTAGE



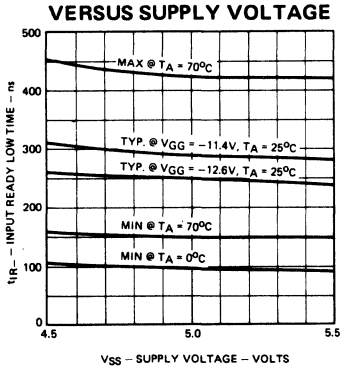
INPUT READY LOW TIME VERSUS AMBIENT TEMPERATURE



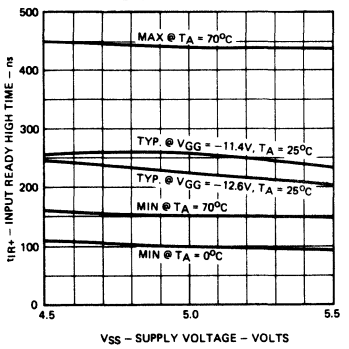
INPUT READY HIGH TIME VERSUS AMBIENT TEMPERATURE



INPUT READY LOW TIME VERSUS SUPPLY VOLTAGE

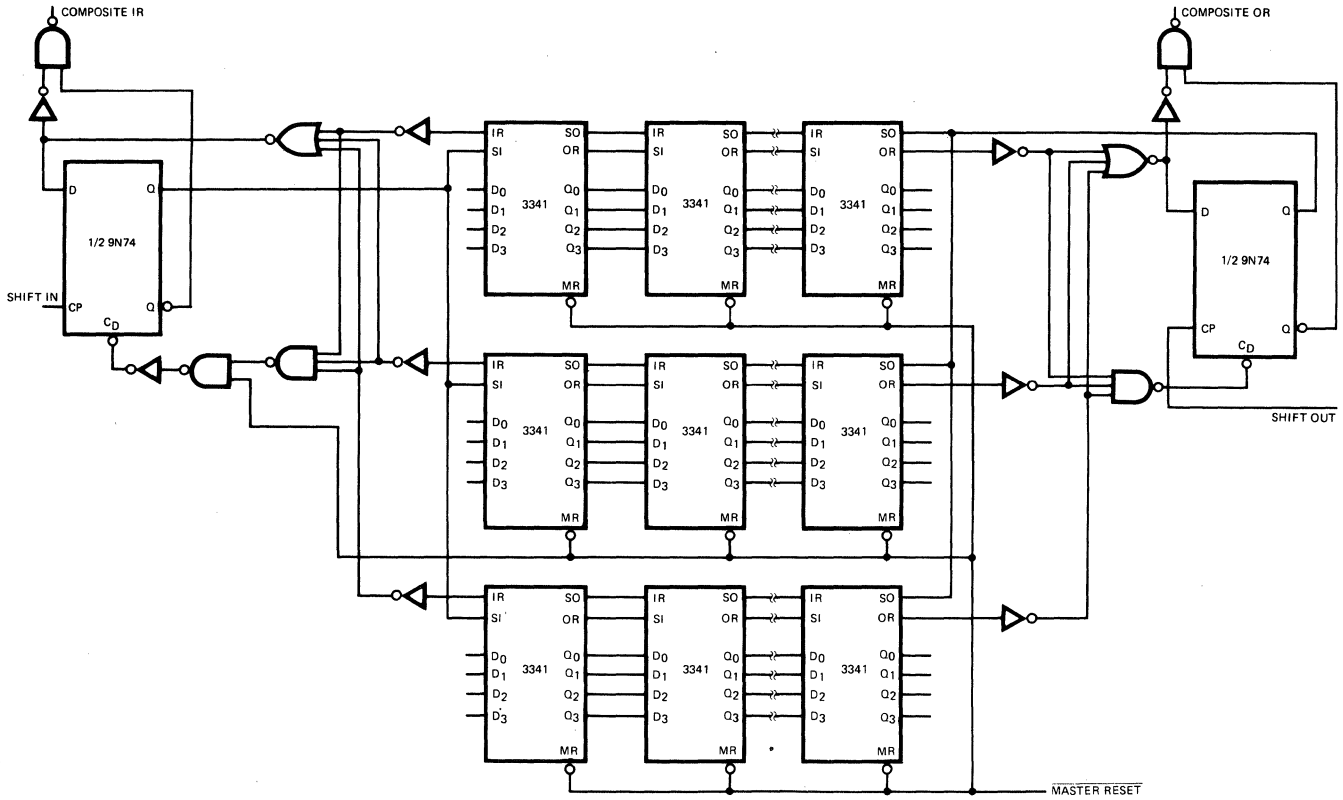


INPUT READY HIGH TIME VERSUS SUPPLY VOLTAGE



SLI

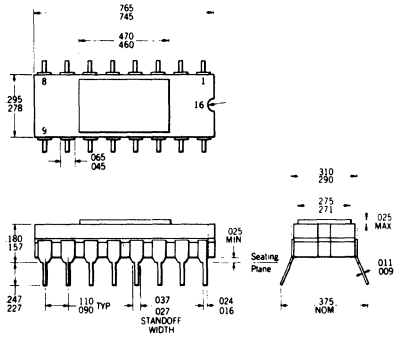
EXPANSION OF 3341 TO N-WORD BY 12-BIT FIFO



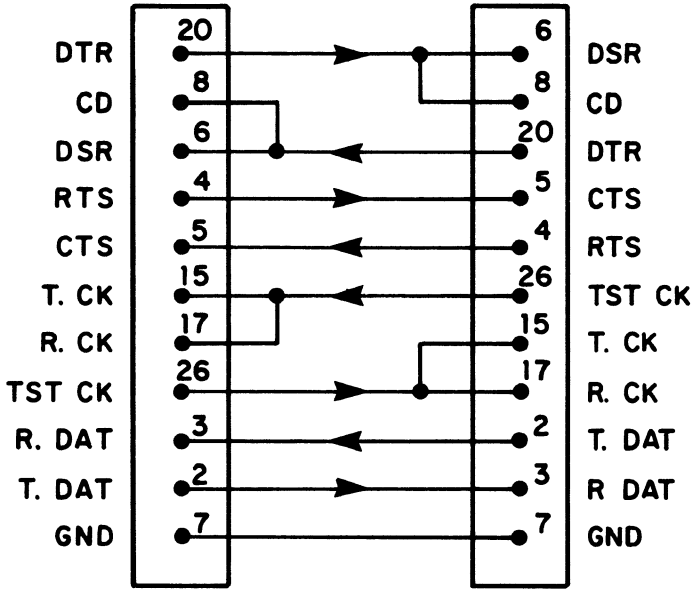
NOTE: Composite Shift In should be LOW when Master Reset goes HIGH. Input data may be changed after Composite IR goes LOW. Composite IR will not go HIGH until Composite Shift In goes LOW. When Composite IR goes HIGH FIFO's will accept new data. 3341's will operate at their highest natural speeds if these rules are followed.

PACKAGE INFORMATION

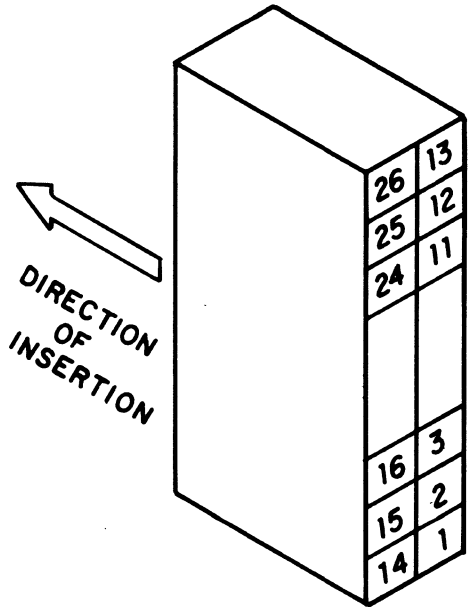
7K – 16-LEAD DUAL IN-LINE PACKAGE



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are gold-plated kovar
Lead No. 8 is internally grounded

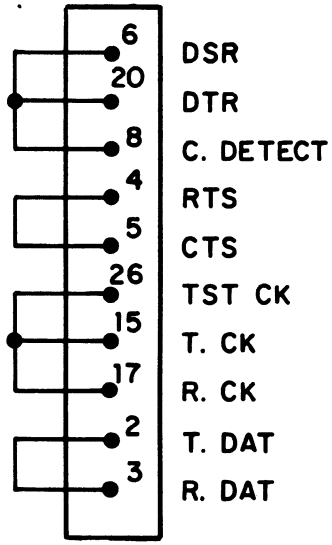


DOUBLE PLUG CONFIGURATION FOR TESTING TWO CARDS OR TWO HALVES OF SAME CARD AGAINST EACH OTHER



CONNECTOR PIN-NUMBERING

SINGLE PLUG CONFIGURATION



Appendix D. Looping Plug Configurations; BLI

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A	RELEASE FOR PROJECT #1	1/19/76	

SLI

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN BF / NRF

CHECKER

ENGINEER 1/19/76

APP'D FOR REL 1/19/76

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

SLI-TECHNICAL REFERENCE

SIZE	CODE IDENT NO.	DRAWING NO.
A		SLI-Ø5

SCALE	REV	SHEET
	A	1 OF 3

WORD AND BIT ASSIGNMENTS

FIRST UNIT	XXX0	2	4	6	
SECOND UNIT	8	A	C	E	
BIT	DEVICE TYPE (DT)	STATUS (ST)	CONTROL (CR)	DATA READ (DR)	DATA WRITE (DW)
15	0	TRANS BUFFER EMPTY		INPUT DATA READY	
14	0	SYN TRANSMITTED		SYN RECEIVED	
13	0				
12	0				
11	0				
10	1	CLEAR TO SEND	REQ. TO SEND		
9	0	CARRIER DETECT	LOOP TEST	RCVR. PARITY ERROR	STORE TRANS SYN
8	0	DATA SET READY	DATA TERMINAL READY	RCVR. OVERRUN ERROR	STORE RCVR SYN
7	BAUD RATE CODE		7 BIT-PLUS-PARITY MODE		
6	BAUD RATE CODE		(RESERVED FOR EVEN PARITY MODE)		
5					
4					
3					
2					
1					
0			RECEIVER RESET*		

8 BIT DEVICE TYPE

FIRST CHAR RCD (TEST BIT 0 FOR EVEN)

INPUT DATA BYTE

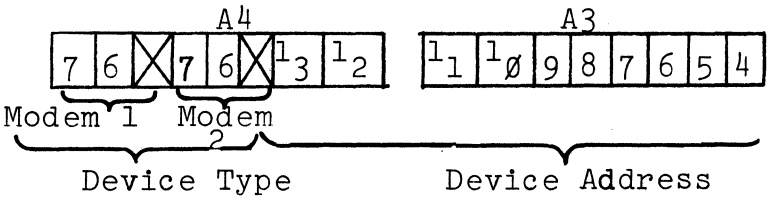
OUTPUT DATA BYTE

12/11/74

*CR0 WILL ALWAYS BE 0 WHEN READ

SLI - SYNCHRONOUS LINE INTERFACE

Switches



Bus (Address field)

1. For 20 bit Address Decoding (I-Bus) Insert BDR in A2
2. For 16 bit Adress Decoding (P-Bus) Insert Jumper-Bug in A2, connecting pins 1,2,3,12, and 13.

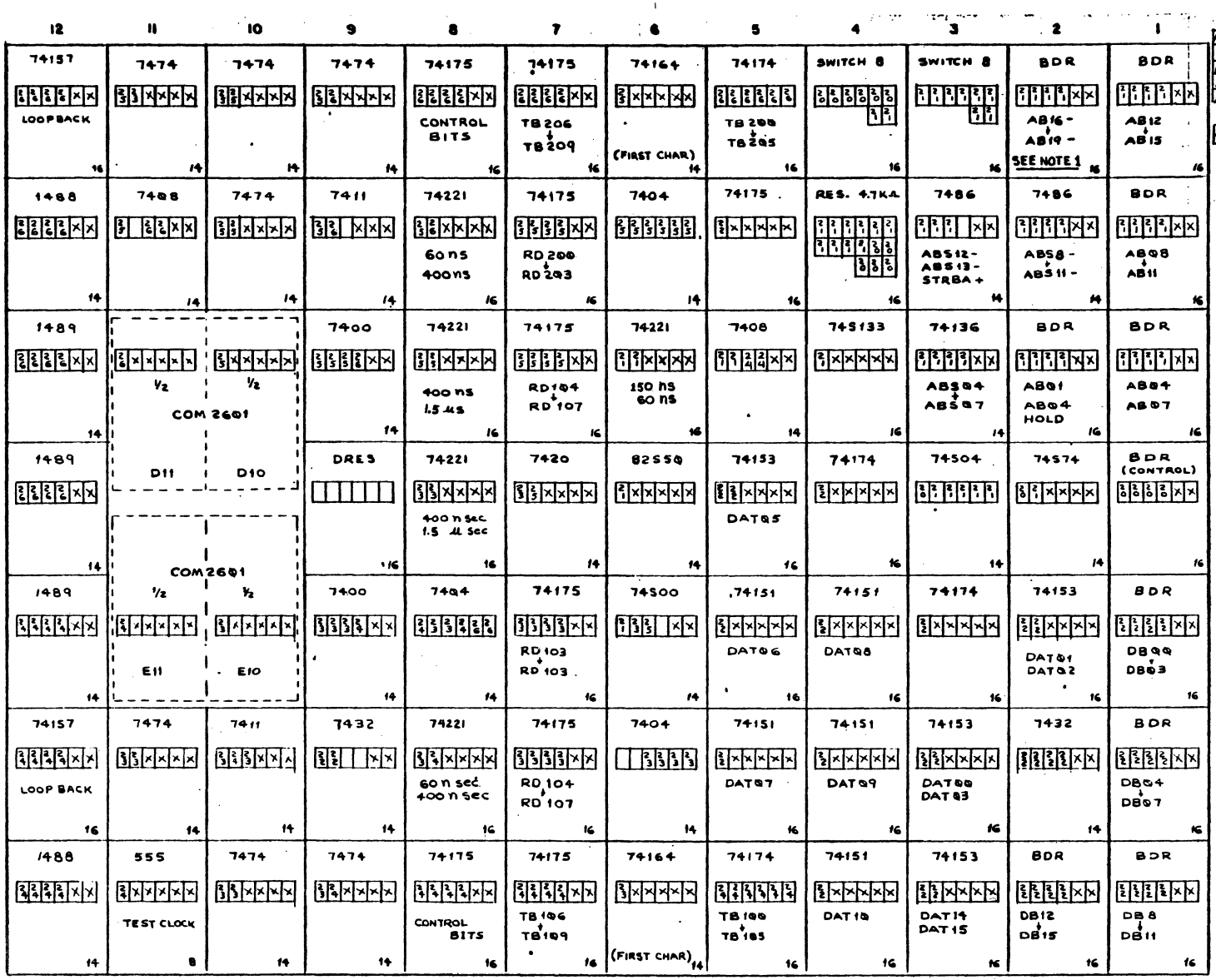
Connectors

Upper connector is for Modem #2 (D.T. Address XXX8)
Lower connector is for Modem #1 (D.T. Address XXXØ)

Jumpers

NONE

SLI-2Ø SCHEMATICS



TOP VIEW

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	4/16/73
	B	ECN# 0021	12/1/73
	C	ECN 0110	2/2/74
	D	ECN 0129	3/4/75
	E	ECN 0144	7/2/75

NOTES:

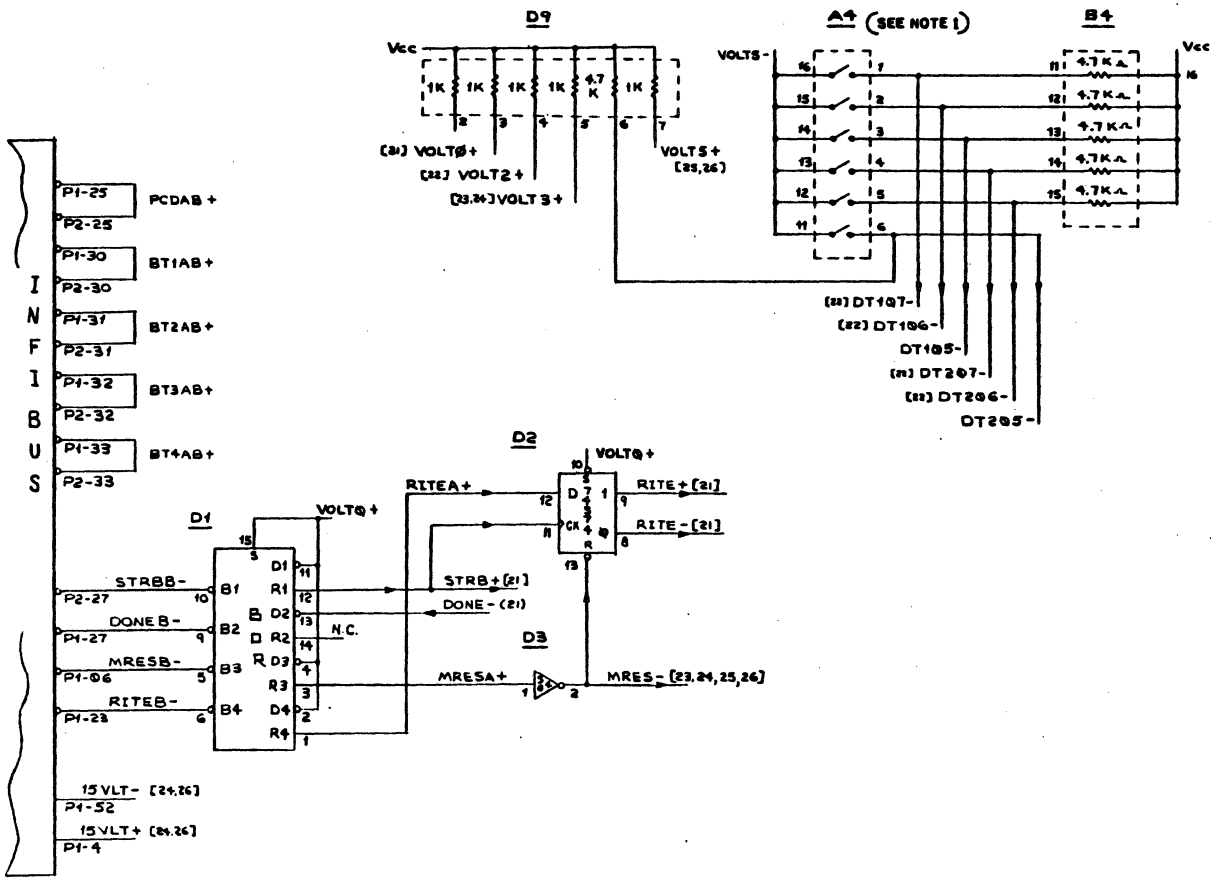
1 - IN 16 BIT ADDRESS SYSTEM (P-BUS) REPLACE A2 WITH COMPONENT-BUG, CONNECTING PINS 1, 3, 12 & 14 TO PIN 16 THROUGH A 1K RES.

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	4/16/73	TITLE	INTEGRATED CIRCUIT LAYOUT
CHECKED		4/16/73	CUSTOMER/NO. HSMIMP	DWG NO. SLI-00-WW REV E
APPROVED		3/6/75		

SLI

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	11.1.73
	B	ECN # 0021	1-30-74
	C	ECN 0110	12.2.74
	D	ECN 0143	5-26-75
	E	ECN 149	6-11-75



NOTES

1 - ON = SWITCH CLOSED POSITION = 1

COMPUTER SYSTEMS DIVISION

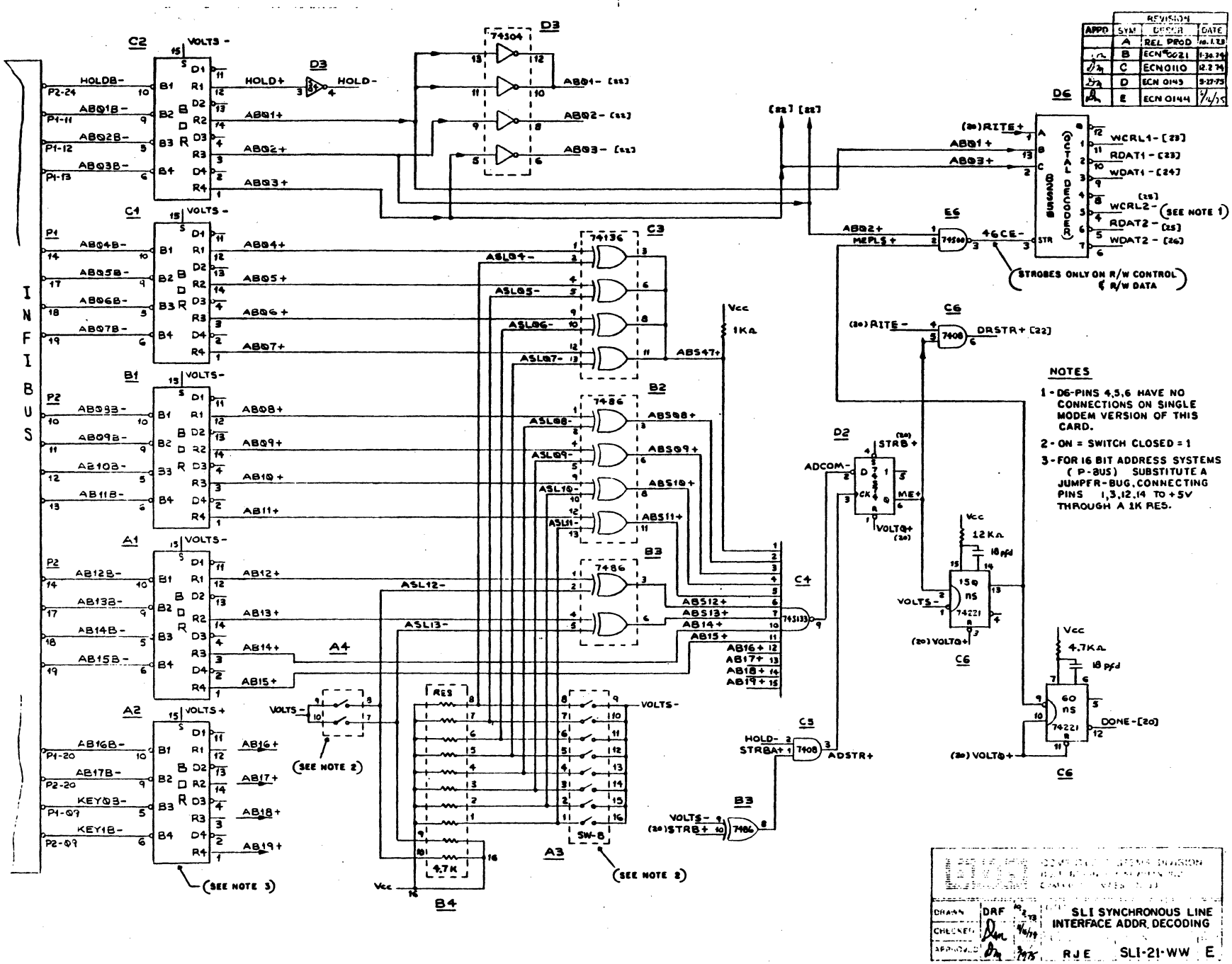
DRAWN DRF 1.13.75

CHECKED 1/16/75

APPROVED 3/4/75 RJE

SLI MISC CONTROL SIGNALS

SLI-20-WW E



APPD	SYM	DESCR	DATE
	A	REL PROD	10.1.73
	B	ECN 0221	1-24-74
	C	ECN 0110	12.2.74
	D	ECN 0143	3-27-75
	E	ECN 0144	7/4/75

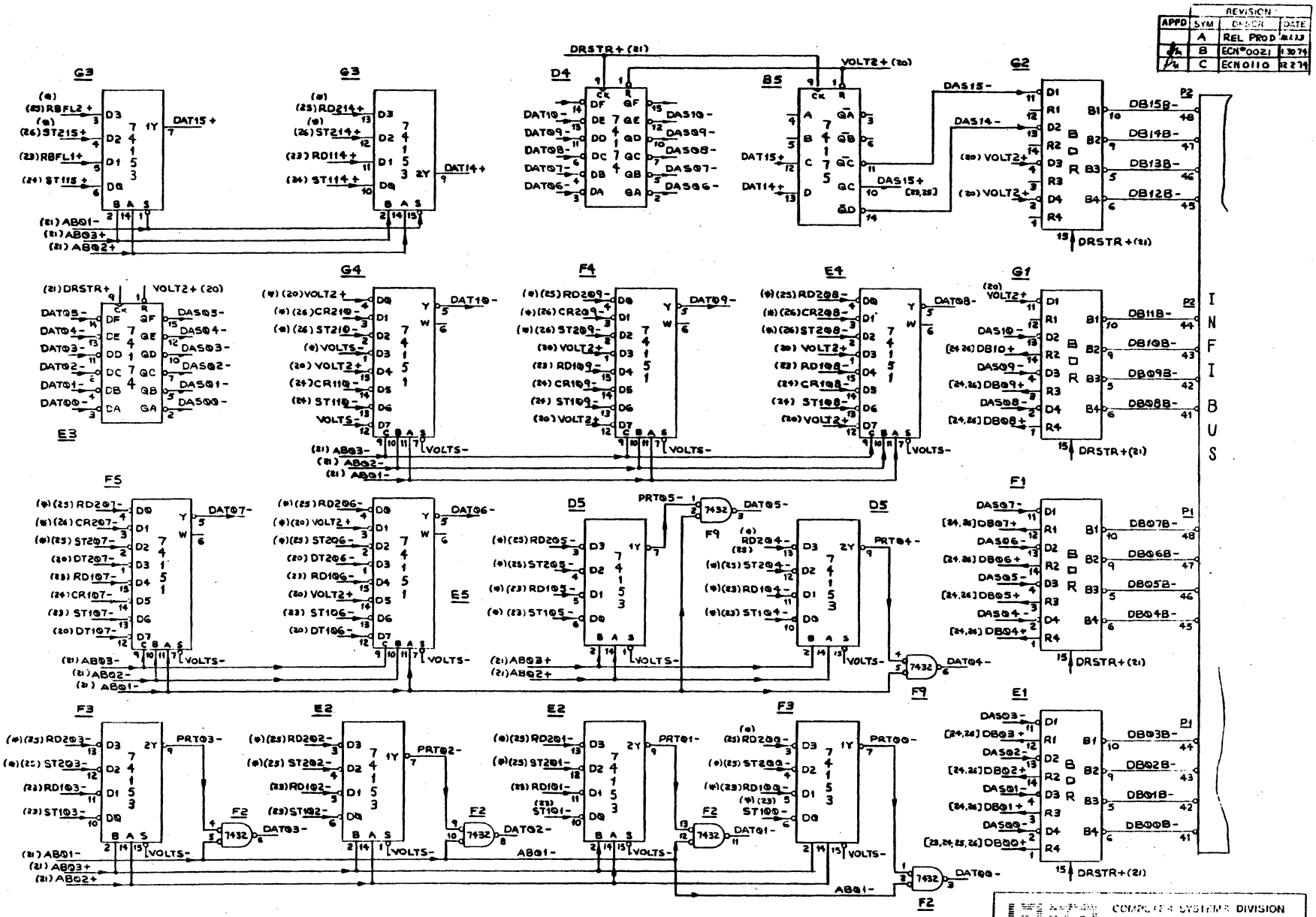
NOTES

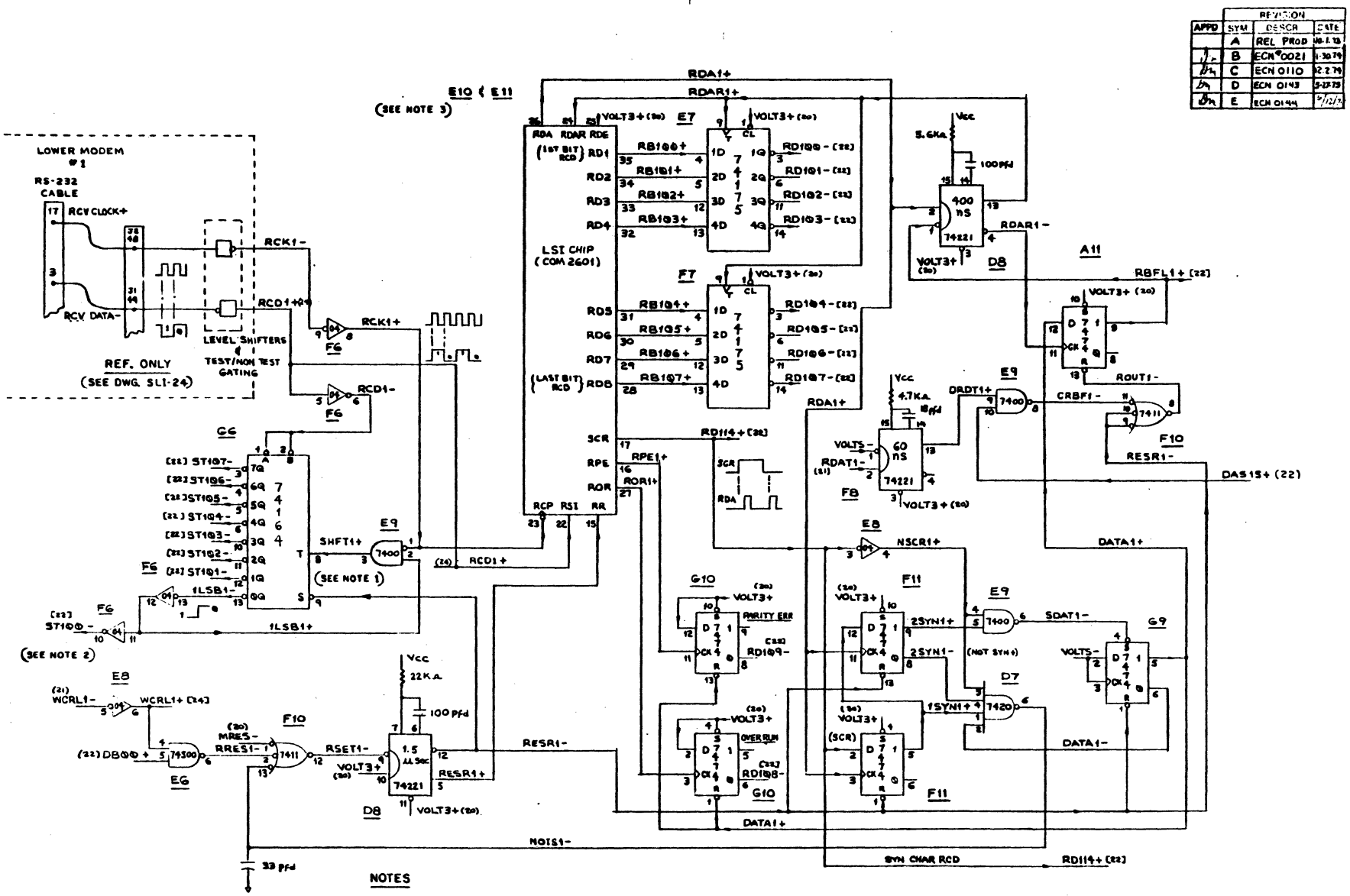
1 - D6-PINS 4,5,6 HAVE NO CONNECTIONS ON SINGLE MODEM VERSION OF THIS CARD.

2 - ON = SWITCH CLOSED = 1

3 - FOR 16 BIT ADDRESS SYSTEMS (P-BUS) SUBSTITUTE A JUMPER-BUG, CONNECTING PINS 1,3,12,14 TO +5V THROUGH A 1K RES.

DRAWN	DRF	10/2/73	SLI SYNCHRONOUS LINE INTERFACE ADDR. DECODING
CHECKED		10/10/73	
APPROVED		3/7/75	RJE SLI-21-WW E


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 8/13
B | ECN#0021 | 1 30 74
C | ECN0110 | 12 2 74
G3
G3
D4
B5
G2
G4
F4
E4
G1
E3
F5
D5
D5
F1
F3
E2
E2
F3
E1
F9
F9
F2
F2
INFIBUS
P2
P1
DRSTR+(21)
VOLT2+(20)
VOLTS-
ABS01-
ABS02+
ABS03+
NOTE 1-ALL PINS WITH A (*) HAVE NO CONNECTIONS ON SINGLE MODEM VERSION OF THIS CARD.
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC.
CAMBRIDGE, MASS.
DRAWN DRF
CHECKED
A. ROVSO
TITLE SLI DATA BDR's & MUX
CUSTOMER NO. RJE
DWG. NO. SLI-22-WW
REV C



NOTES

1 - 8 { 1 NOMENCLATURE REVERSED:
"1" INPUT FROM MODEM PRODUCES LOW OUTPUTS
PIN 9 (SET) INPUT PRODUCES LOW OUTPUTS

2 - BIT 8 DELAYED SO READING ALWAYS VALID WHEN EVEN

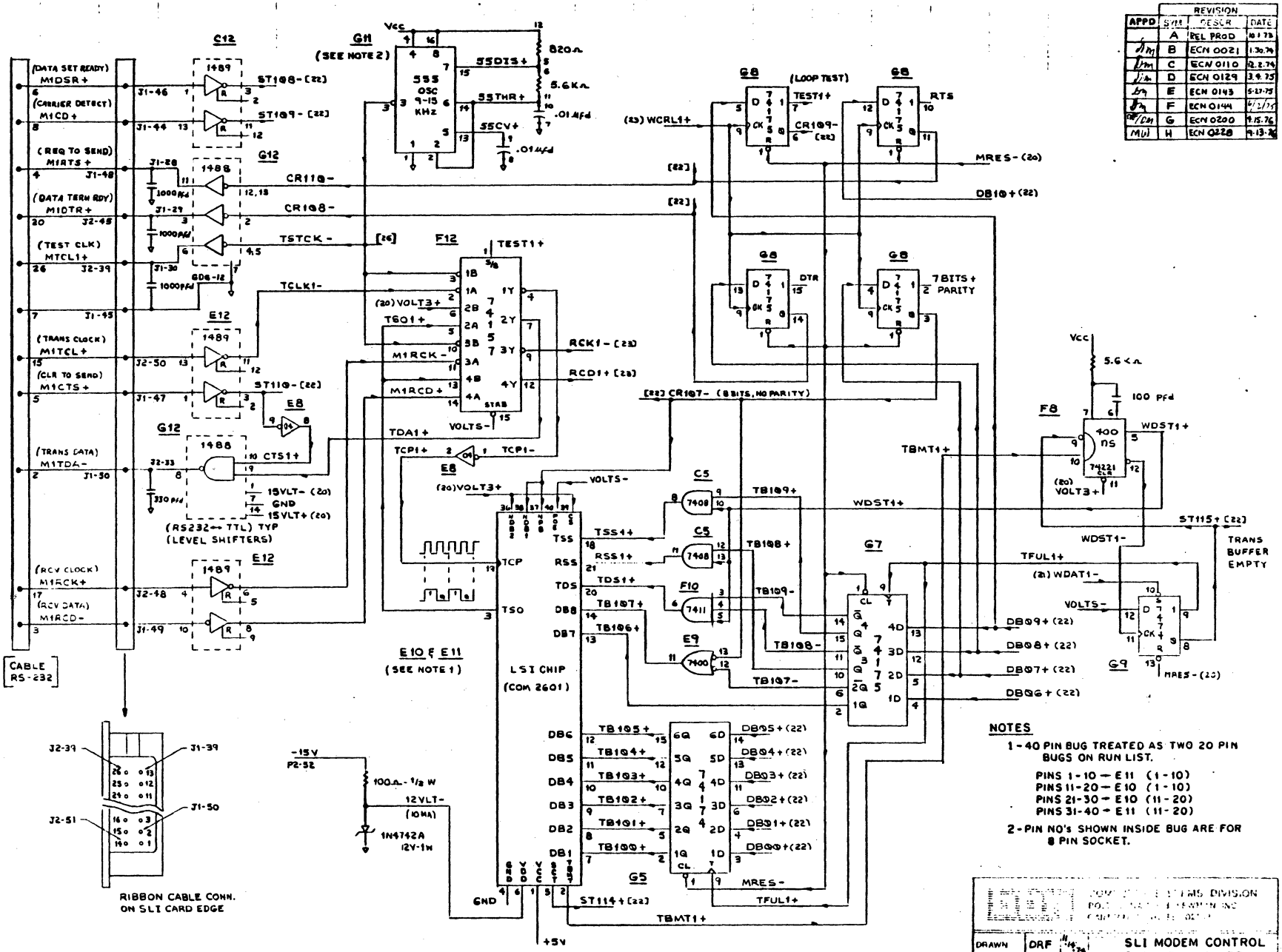
3 - 40-PIN BUG TREATED AS TWO 20-PIN BUGS ON WIRE LIST
PINS, 1-10 → E11-(1-10)
PINS, 11-20 → E10-(1-10)
PINS 21-30 → E10-(11-20)
PINS 31-40 → E11-(11-20)

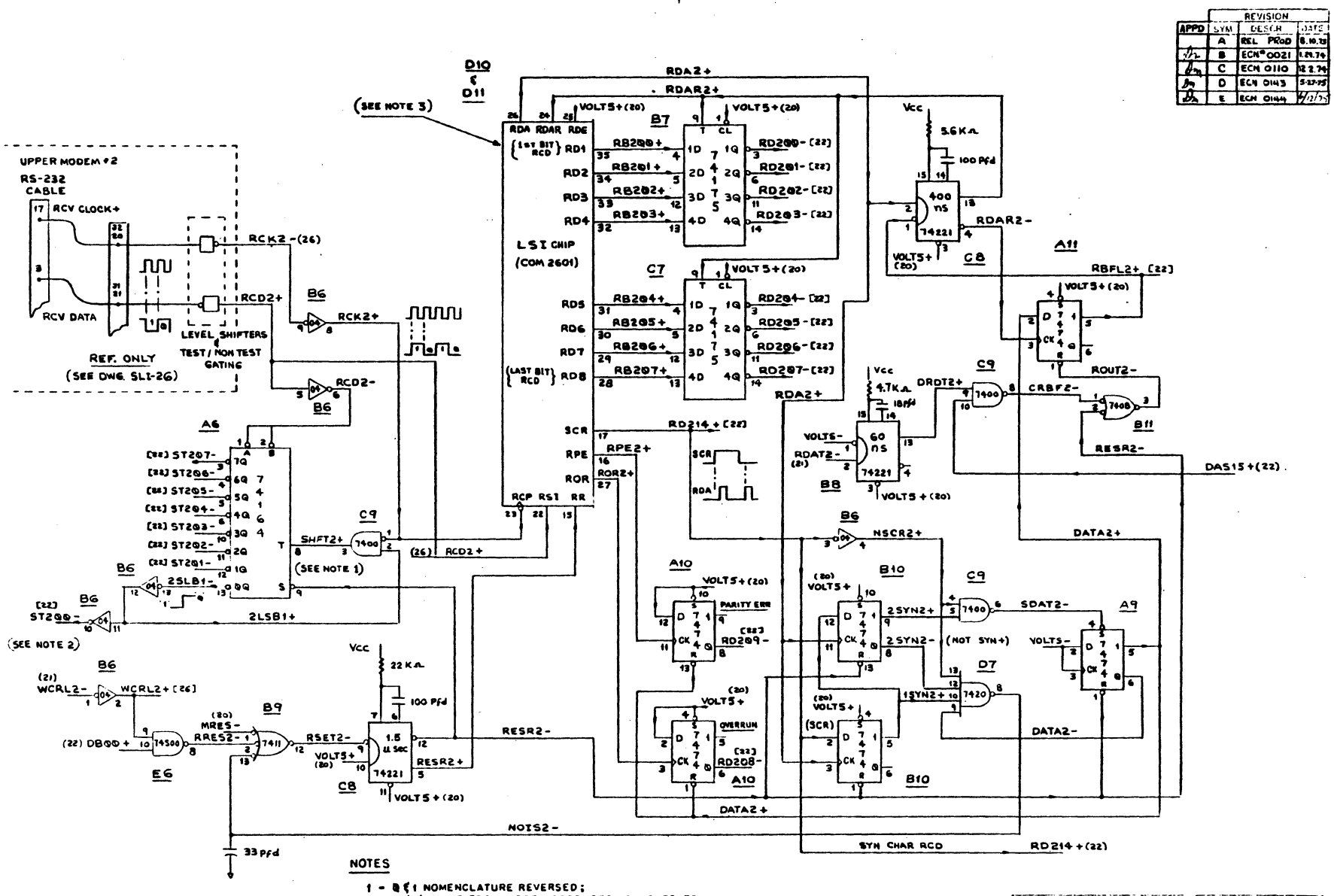
COMPUTER SYSTEMS DIVISION
FULL RANGE SYSTEMS INC
LAWRENCE, MASS.

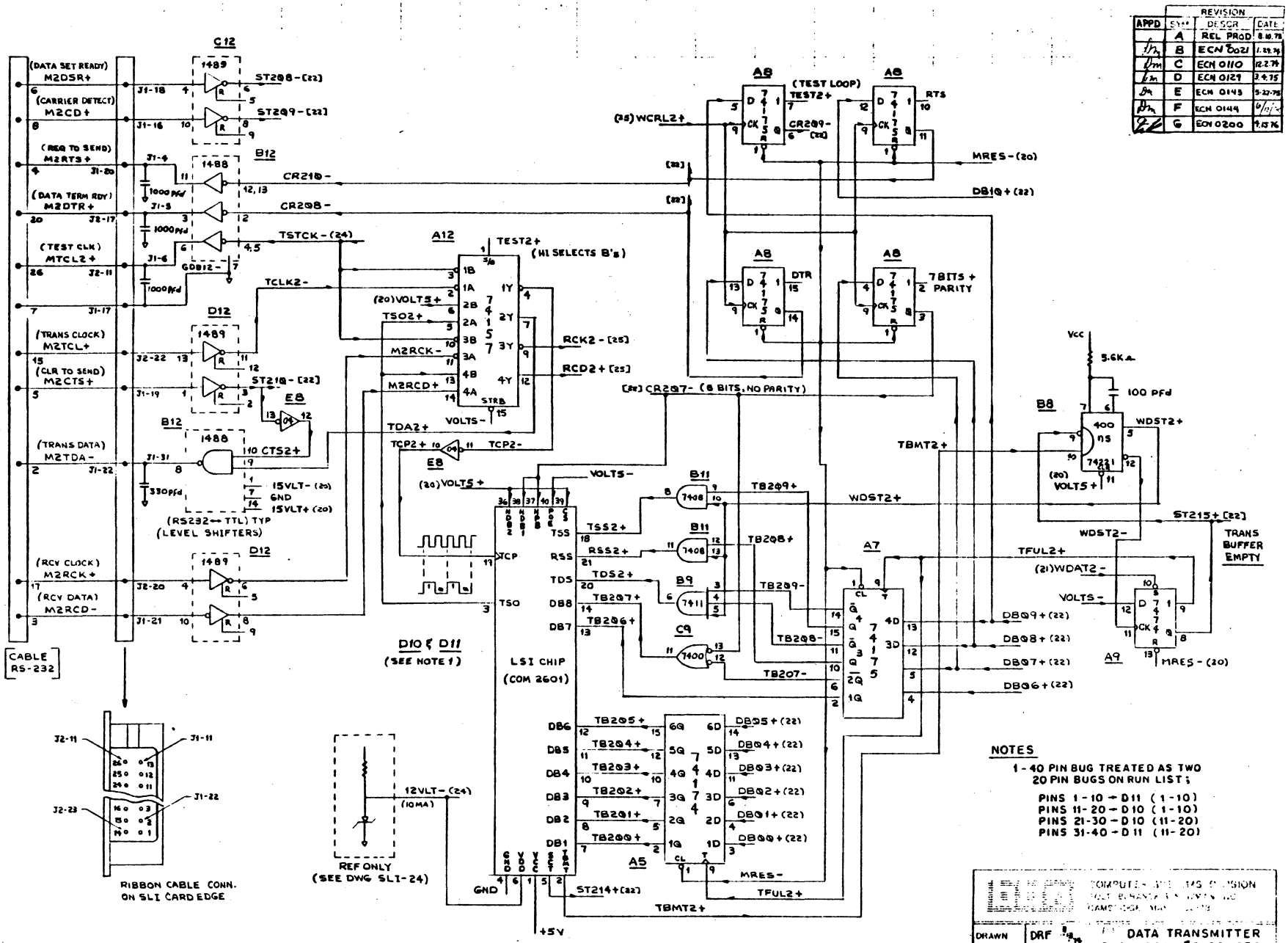
DRAWN DRF 8/73
CHECKED
APPROVED RJE

SLI DATA RECEIVER
SLI-23-WW E

SLI


REVISION
APPD SYM DESCR DATE
A REL PROD 10 1 75
B ECN 0021 1.30.76
C ECN 0110 2.2.76
D ECN 0129 3.9.76
E ECN 0143 5-27-76
F ECN 0144 6/2/76
G ECN 0200 9.15.76
H ECN 0228 9-13-76
(DATA SET READY) M1DSR+
(CARRIER DETECT) M1CD+
(REQ TO SEND) M1RTS+
(DATA TERM RDY) M1DTR+
(TEST CLK) MTCL1+
(TRANS CLOCK) M1TCL+
(CLR TO SEND) M1CTS+
(TRANS DATA) M1TDA-
(RCV CLOCK) M1RCK+
(RCV DATA) M1RCD-
CABLE RS-232
RIBBON CABLE CONN. ON SLI CARD EDGE
(RS232↔ TTL) TYP (LEVEL SHIFTERS)
LSI CHIP (COM 2601)
E10 & E11 (SEE NOTE 1)
(SEE NOTE 2)
(LOOP TEST)
NOTES
1 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST.
PINS 1-10 — E11 (1-10)
PINS 11-20 — E10 (1-10)
PINS 21-30 — E10 (11-20)
PINS 31-40 — E11 (11-20)
2 - PIN NO'S SHOWN INSIDE BUG ARE FOR 8 PIN SOCKET.
SLI MODEM CONTROL DATA TRANSMITTER
DRAWN DRF
CHECKED
APPROVED RJE
SLI-24-WW H


REVISION
APPD SYM DESCR DATE
A REL PROD 8.10.73
B ECN# 0021 1.29.74
C ECN 0110 12.2.74
D ECN 0143 5-27-75
E ECN 0144 6/25/75
UPPER MODEM #2
RS-232 CABLE
RCV CLOCK+
RCV DATA
RCK2-(26)
RCD2+
LEVEL SHIFTERS TEST/NON TEST GATING
REF. ONLY (SEE DWG. SLI-26)
RCK2+
RCD2-
D10 & D11
(SEE NOTE 3)
RDA2+
RDAR2+
LSI CHIP (COM 2601)
RDA RDAR RDE
RD1 RD2 RD3 RD4 RD5 RD6 RD7 RD8
RB200+ RB201+ RB202+ RB203+ RB204+ RB205+ RB206+ RB207+
RD200- RD201- RD202- RD203- RD204- RD205- RD206- RD207-
SCR RPE ROR RCP RSI RR
RPE2+ ROR2+ RD214+(22)
5.6K Ω 100 Pfd 400 ns 74221
4.7K Ω 18 Pfd 60 ns 74221
RBFL2+(22) ROUT2- RESR2- DAS15+(22)
DRDT2+ CRBFE- RDAT2-
NSCR2+ DATA2+
SHFT2+ (SEE NOTE 1) 2LSB1+ 2LSB1- ST200- (SEE NOTE 2)
ST207- ST206- ST205- ST204- ST203- ST202- ST201-
PARITY ERR RD209-
2SYN2+ 2SYN2- (NOT SYN+) SDAT2-
OVERRUN RD208-
SYN CHAR RCD RD214+(22)
WCRL2- WCRL2+(26)
MRES- RRES2- RSET2- RESR2+
DB00+ 22 KΩ 100 Pfd 1.5 μSec 74221
NOIS2- 33 Pfd
NOTES
1 - B{1 NOMENCLATURE REVERSED; '1' INPUT FROM MODEM PRODUCES LOW OUTPUTS PIN 9 (SET) INPUT PRODUCES LOW OUTPUTS
2 - BIT 0 DELAYED SO READING ALWAYS VALID WHEN EVEN
3 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON WIRE LIST
PINS, 1-10 → D11-(1-10)
PINS, 11-20 → D10-(1-10)
PINS, 21-30 → D10-(11-20)
PINS, 31-40 → D11-(11-20)
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE, MASS.
DRAWN DRF
CHECKED
APPROVED RJE
TITLE SLI DATA RECEIVER MODEM #2
CUSTOMER DWG. NO. SLI-25-WW
REV E
SLI



APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	8.10.73
	B	ECN 0021	1.29.74
	C	ECN 0110	12.2.74
	D	ECN 0129	3.4.75
	E	ECN 0143	5-22-75
	F	ECN 0144	6/17/75
	G	ECN 0200	1.23.76

NOTES

1 - 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST;

PINS 1 - 10 → D11 (1 - 10)
PINS 11 - 20 → D10 (1 - 10)
PINS 21 - 30 → D10 (11 - 20)
PINS 31 - 40 → D 11 (11 - 20)

COMPUTER SYSTEMS DIVISION
VOLT INSTRUMENTS INC.
SANTA CLARA, CALIFORNIA

DRAWN	DRF 8/19/74	DATA TRANSMITTER SLI MODEM 2 CONTROL
CHECKED		
APPROVED	8/26/75	RJE SLI-26-WW G

16-K Words Semiconductor Memory

SME-Ø5 Technical Reference

SME-1Ø Assembly Drawing

SME-15 Standard Modification

SME

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
		A			
		B			

SME

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

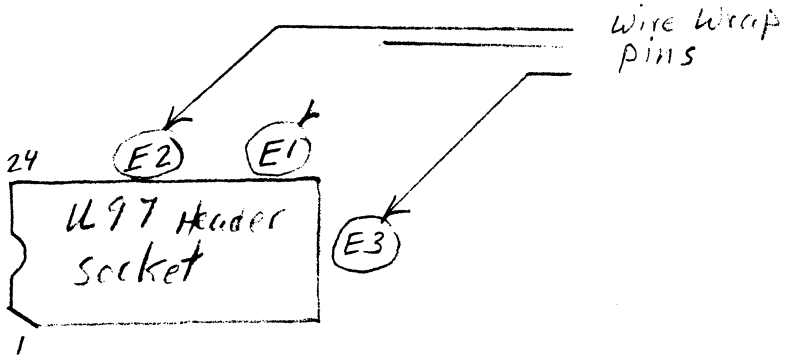
	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN	
	CHECKER	DRAWING TITLE
	ENGINEER	
	APP'D FOR REL	SIZE: A; CODE IDENT NO.; DRAWING NO.
	APP'D (CUSTOMER)	SCALE; REV; SHEET 1 OF 5

SME - 16K Semiconductor Memory LEC

Address Strapping

Address strapping is done by soldering jumpers on the header plug at U97. Headers may be supplied prewired by BBN for common addressing modes, in which case it is only necessary to plug in the correct header and insure that the three wirewraps pins, E1, E2, and E3 around U97, are correctly jumpered. (These wirewrap pins select recognition of address bit 19).

"E" ww jumpers in relation to U97 Header: Be careful to insert U97 correctly. Pin 1 is next to a 1000pf cap and faces the outboard end of the card. Addresses are specified as decimal words.



Note: For all except split-8K operation, strap U97:24 - U97:6 (in addition to other strapping required).

Since the SME recognizes 20 address bits, strappings for Key ALT (KA0, KA1, KA2, KA3) are given also. (KA will normally be strapped for either KA0 or "ignore KA").

A. Key ALT strapping (in addition to other address strapping) select one of the following:

Memory Address Range	Key ALT	U97 Header Strapping
0-128K	(KA0)	13-22, 11-21, 12-19*, E1-E3
128-256K	(KA1)	13-22, 11-21, 5-19*, E1-E3
256-348K	(KA2)	13-22, 11-21, 12-19*, E1-E2
384-512K	(KA3)	13-22, 11-21, 5-19*, E1-E2
"Ignore KA"		18-19, 19-20, 13-22, 11-21
"Ignore Keys + KA"		22-20, 21-10, 18-19, 19-20

*(Omit for 0-4K blinding as in Table C below)

B. 16K block address strapping select one of the following:

Address	Key	U97 Header Strapping
0-16K	(K0)	17-4
16-32K	(K0)	7-4
32-48K	(K1)	16-4
48-64K	(K1)	8-4
64-80K	(K2)	15-4
80-96K	(K2)	9-4
96-112K	(K3)	14-4
112-128K	(K3)	10-4

C. Memory Blinding in 0-4K rang, any 32K page

Memory Blinding	U97 Header Strapping
0-4K of 0-128K block or 256-384K block	5-2, 23-19
0-4K of 128-256K block or 384-512K block	12-2, 23-19

(plus other strapping required)

D. 31-32K Memory Blinding, any 32K page

U97-3-2

E. Split -8K Locals:

To use an SME on a processor bus as both 0-8K, Key 0, and 0-8K, Key 1 (2 separate 8K locals) strap:

SME

U97:11 - U97:22
U97:24 - U97:21
U97:13 - U97:6
U97:17 - U97:4
U97:3 - U97:20
U97:20 - U97:18
U97:18 - U97:19

(SME must have BBN std mod to allow this operation)

F. 0-8K Key 0 Only (8-16K blind)

For use on processor busses.

U97: 11-19, 20-22, 21-24, 6-24, 13-18, 17-4, (E1/E2/E3 - no jumpers).

G. 0-8K Key 1 only (8-16K blind) for use on processor busses.
U97: 11-19, 20-22, 21-24, 6-24, 2-13, 18-20, 17-4, (E1/E2/E3 - no jumpers).

Battery Backup

The IBPK (or IBPO) cable from the BPK battery pack attaches to the socket on the daughter board at the outboard end of the SME.

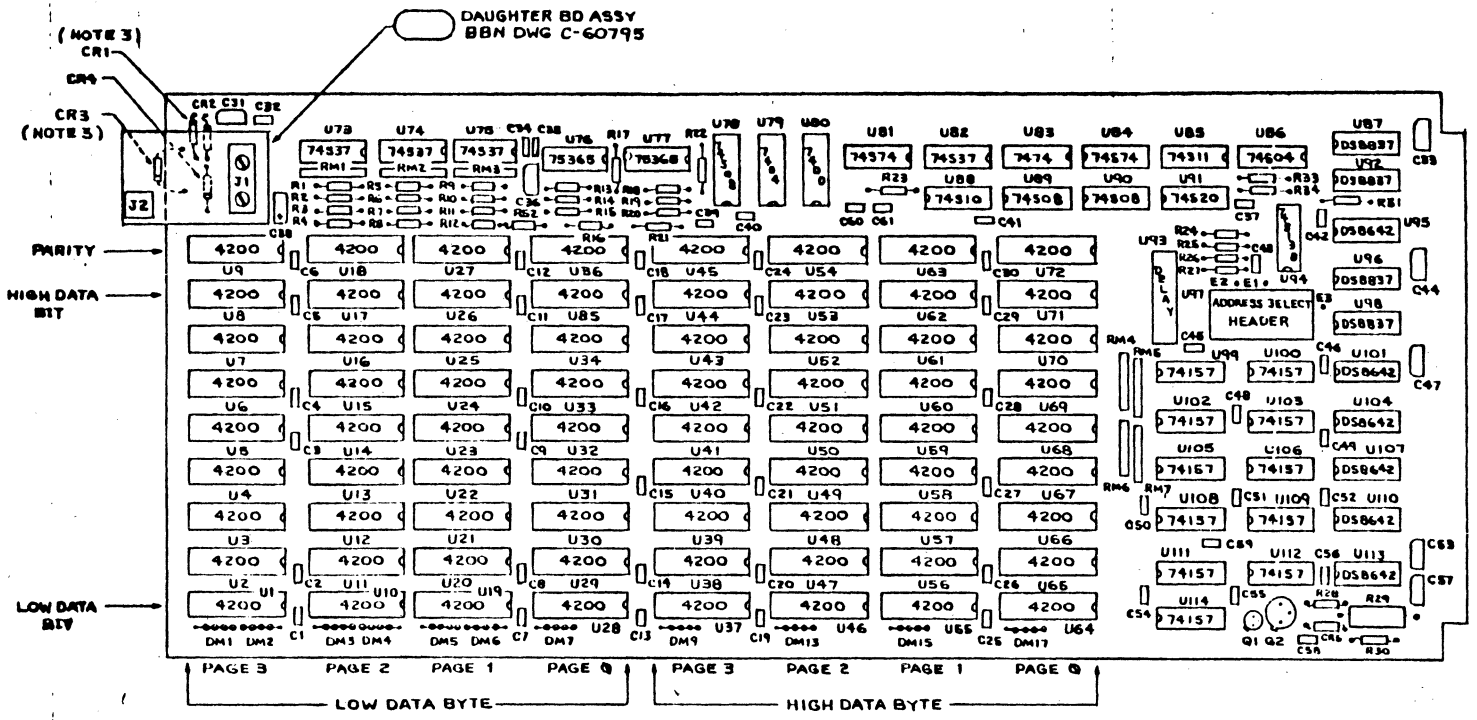
It is not necessary to have a BPK attached to run the memory, but without it the memory contents will be volatile over power fail.

It is necessary to have a daughter board installed to run the memory if the SME has had its standard modification performed (installation of the daughter board should have been done with the standard mod).

Up to 6 SME's may be attached to a single BPK (see BPK functional spec).

SME-1Ø ASSEMBLY DRAWING

REVISION			
LTR	DESCR	DATE	APPD
A	REL PROD	3.7.79	



(REPAIR, REF ONLY)

COMPONENT VALUES

	BBN P NO
C1-30,32,34,36,37,39,40-48 45,46,48-52,54,55,56,58,60 = .01 MFD CAPACITOR	427
C31,33,36,38,44,47,53,57 = 6.8 MFD CAPACITOR	
C59 = 100 PFD CAPACITOR	
C61 = .22 MFD CAPACITOR	287
R1-12,21 = 20Ω 1/4W-5% RESISTOR	
R13,14,15,17-20,22 = 10Ω	
R16 = 330Ω	673
R23-27,31,33,34 = 680Ω	956
R28 = 470Ω	1258
R30 = 182Ω	
R29 = 59.7Ω - 2W RESISTOR	
RM1-7 = 330Ω (RESISTOR MODULE)	
CR1-4 = IN4001 DIODE	654
CR5 = IN752A DIODE	
DM1-7,9,11,13,15 = IN2500 (DIODE MODULE)	
Q1 = 2N2907A TRANSISTOR	686
Q2 = 2N3725 TRANSISTOR	

(REPAIR, REF ONLY)

IC TYPES

	BBN P NO
U1-72 = 4200	
U73-75,82 = 74S37	1414
U76,77 = 75365	
U78,89,90 = 74S08	261
U79 = 7404	70
U80 = 7400	67
U81,84 = 74S74	111
U88 = 7474	83
U85 = 74S11	109
U86 = 74S04	107
U87,92,96,98 = DS8837	
U88 = 74S10	108
U91 = 74S20	110
U93 = 7714 DELAY	
U94 = 74S138	1393
U15,101,104 107,110,113 = DB642	61
U97 = ADDR SEL HEADER	
U99,100,102,103,105 106,108,109,111,112,114 = 74157	93

NOTES

1 - ▷ INDICATES PIN ORIENTATION

2 - COMMON LEAD ON DIODE MODULES (DM) & RESISTOR MODULES (RM) IS DESIGNATED PIN NO 1

3 - REMOVE DIODES (CR1 & CR3) & REMOUNT 2 NEW DIODES (IN4001) AS FOLLOWS:

A) CR1 IS TO BE MOUNTED AS CLOSE TO TOP SOLDER TERMINAL AS POSSIBLE TO ALLOW SPACE FOR MOUNTING DAUGHTER BOARD

B) CR3 IS TO BE MOUNTED FLUSH WITH SME CARD EDGE (AS SHOWN) TO ALLOW SPACE FOR MOUNTING DAUGHTER BOARD

		SIZE	
		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC CAMBRIDGE, MASS 02138	
	PLURIBUS SYS	DRAWN DRF 3/1/79	TITLE LEC 16K SEMI-CONDUCTOR MEMORY
NEXT ASSY	USED ON	CHECKED	
APPLICATION		ENG APPD	COLE ID. NO. DWG NO. SME-10 REV A

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A			
B			
C			

SME

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN	
	CHECKER	DRAWING TITLE
	ENGINEER	
	APP'D FOR REL	SIZE: A; CODE IDENT NO.; DRAWING NO.
	APP'D (CUSTOMER)	SCALE; REV A; SHEET OF

SME-15
SME STANDARD MODIFICATION

Applies to: Board PC Rev level C - G
Assy Rev level K - L

Note: Because of sensitivity of M.O.S. ICs to static discharge, all of the standard mods described should be performed at an anti-static work station or on a sheet of neutro-stat plastic if possible. SME boards should be stored in the black neutro-stat bags which they are received in.

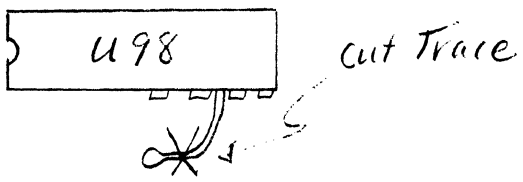
A. Attach tag at bottom hole of board. Tag and head of nylon screw should be on solder-side of board. It may be necessary to trim the component leads slightly. Write "SME" and serial # on tag.

B. Mods to board. Do all modifications. (Ref. SME-10)

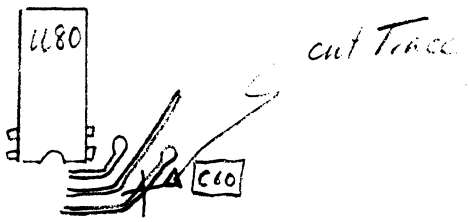
Parts required:

(1) 16 pin dip socket, BBN #221
(1) SME daughter board C-60795
(2) 2-56 X 5/8 PHMS Nylon, BBN #1704 and 2-56 nylon nuts, BBN #1705

Delete U92:14 - U97:6 side 1
(at feed through under U98)



Delete U79:11 - U91:5 at feed through (side 1) to rt of U80:1



Add U79:11 - U97:6 (S2) (solder)
secure wire with silicone or epoxy adhesive

Locate unused bug position directly above U9. This is to be called J1. J1:1 is at bottom right (nearest U18).

SME

(Note: if there is already a bug in this position, do not proceed further - call an engineer.)

Remove & Replace

Remove C38 (below CR-3) and move to position called C38 on Dwg. # SME-10 observing proper polarity.

Replace CR-3 with 1N4004 and position so body of diode extends past edge of PCB.

Replace CR-1 with 1N4004 and position bends so body of diode is as far toward top edge of board as possible.

Carefully remove all solder from holes of J1.

Lift leg of U76:16
Lift leg of U77:16
Lift leg of U76:1
Lift leg of U76:9
Lift leg of U77:1
Lift leg of U77:9

Connect U92:14 - U91:1 (solder to bug legs)
Connect U76:16 - U77:16 (solder wire to bug legs)
Connect U77:16 - J1:5 (solder to outer pad)
Connect U76:1 - U76:9 - U77:1 - U77:9 (solder wire to bug legs)
Connect U76:1 - J1:6 (solder to outer pad)
Connect U86:6 - J1:1 (solder to outer pad)
Connect J1:10 (solder to outer pad) - end of CR4 nearest U9
Connect J1:9 (solder to outer pad) - U9:1 (side 2)

Install 16 pin dip socket (BBN #221) in J1 and solder

Plug in tested daughter board and using holes in daughter board as template, carefully drill two .096" dia holes through socket and SME board.

Remove daughter board.

Clean off SME board (DO NOT DIP board in hot tank of degreaser use only vapors and spray wand).

Ring out all connections and attach daughter board with two 2-56 X 5/8 pan head screws, BBN # 1704 and two 2-56 nylon nuts, BBN #1705

Report No. 3004 Bolt Beranek and Newman Inc.

Synchronous Modem Simulator

SMS-2Ø Schematics

SMS

13	12	11	10	9	8	7	6	5	4	3	2	1	
	8T13 (NOTE 3) (NOTE 5) 16	8T13 (NOTE 3) (NOTE 5) 16		74163 16	74163 16	SWITCH-8 16	74163 16	74163 16	SWITCH-8 16	SWITCH-8 16	BDR (NOTE 1) AB16 ↓ AB19 (NOTE 5) 16	BDR AB12 ↓ AB15 16	A
	8T13 (NOTE 3) (NOTE 5) 16	DRES 16		74163 16	74163 16	RES 4.7K 16	74163 16	74163 16	RES 4.7K 16	7486 ABS12 ABS13 14	7486 ABS08 ↓ ABS11 14	BDR AB08 ↓ AB11 16	B
	8T14 (NOTE 3) (NOTE 5) 16	74157 16	7400 14	7404 14	7474 14	74S00 14	7408 14	74123 130 ns 50 ns 16	74S133 16	74136 AB$04 ↓ AB$07 14	BDR AB 01, 02, 03 HOLD 16	BDR AB04 ↓ AB07 16	C
THNG 1 (NOTE 2)	9616 (NOTE 4) (NOTE 5) 14	COM 2601 ½ (E11) ½ (E10)	THNG 1 (NOTE 2)	DRES 16	74123 14	7402 14	82S50 14	74S74 14	74S10 14	74S04 14	74S74 14	BDR CONTROL 16	D
	9616 (NOTE 4) (NOTE 5) 14		7408 14	7400 14	3341 FIFO 16	7404 14	74175 16	74175 16	74153 16	74175 16	BDR DB00 ↓ DB03 16	E	
THNG 1 (NOTE 2)		THNG 1 (NOTE 2) 16	7474 14	7411 14	74123 14	3341 FIFO 16	7400 14	74175 16	74153 16	74153 16	74175 16	BDR DB04 ↓ DB07 16	F
THNG 1 (NOTE 2)	8T16 (NOTE 4) (NOTE 5) 14	7474 14	7474 14	DRES 16	3341 FIFO 16	3341 FIFO 16	7408 14	3341 FIFO 16	74153 16	74157 16	BDR DB12 ↓ DB15 16	BDR DB08 ↓ DB11 16	G

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	5 & 75
	B	ECN 0195	2.22.76

NOTES: 1-IN 16 BIT ADDRESS SYSTEM, REPLACE A2 WITH COMPONENT-BUG CONNECTING PINS 1, 2, 3, 12 & 14
2-THNG 1 (TYP) ARE ACTUALLY ROWS OF PINS FOR STRAP OPTIONS, SEE ASSY DWG. SMS-10 FOR ACTUAL LOCATION OF PINS
3- FOR SMS-L, OMIT A11, A12, B12 AND REPLACE C12 WITH JUMPER-BUG, CONNECTING PINS 7, 8 & 9
4- FOR SMS-H, OMIT D12, E12 AND G12
5- INSTALL IC SOCKETS AT A11, A12, B12, C12, D12, E12, G12 AND A2

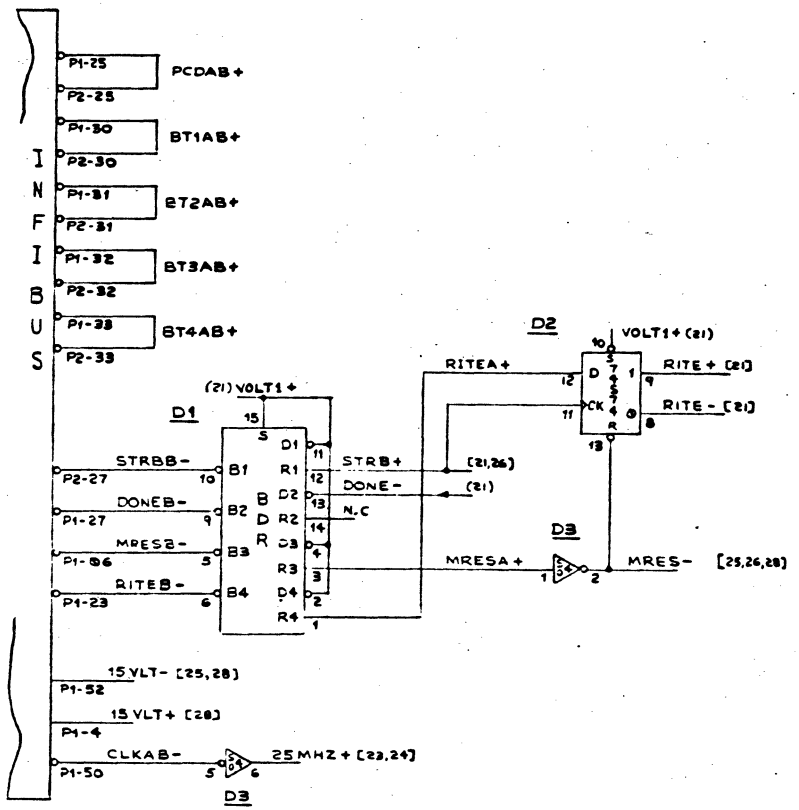
TOP VIEW

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

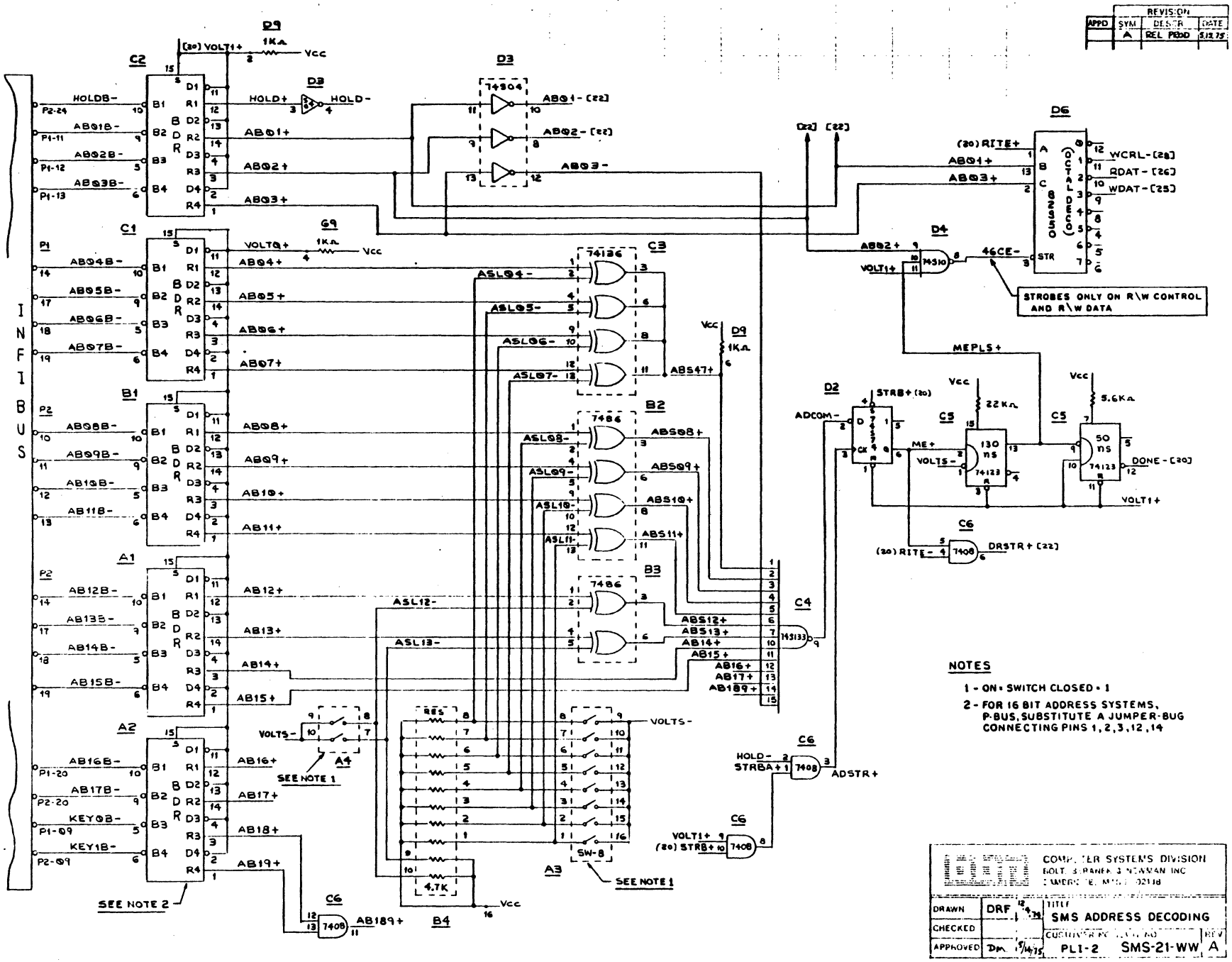
DRAWN	SET	12/19/74	TITLE	INTEGRATED CIRCUIT LAYOUT	
CHECKED	DRF	2/4/75	CUSTOMER/NO.	DWG NO.	REV
APPROVED	DM.	5/15/75	PL1-2	SMS-00-WW	B

SMS

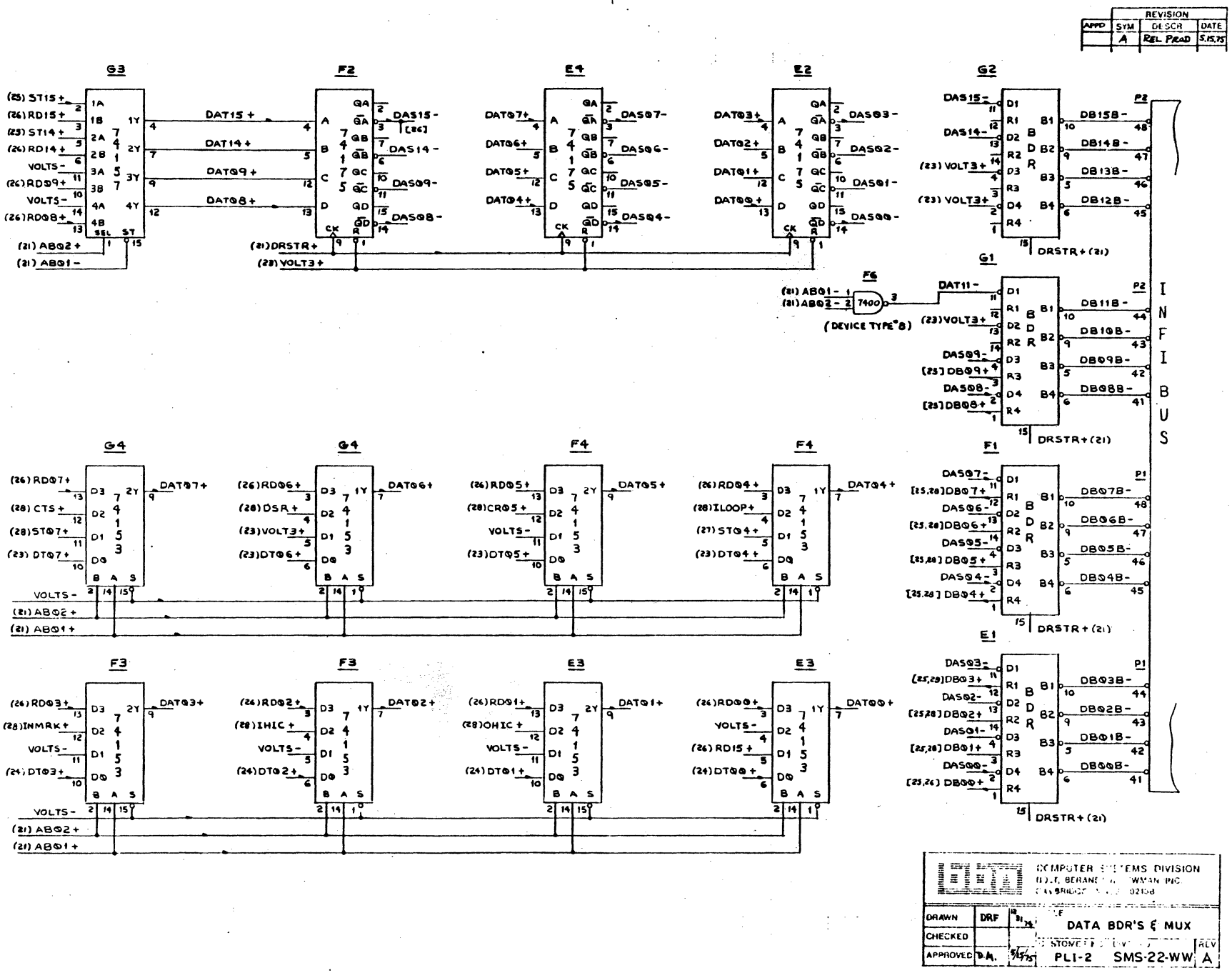
APPD	REVISION		
	SYM	DESCR	DATE
	A	REL PROD	5.15.75



COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	12-4-74	TITLE SMS MISC CONTROL SIGNALS
CHECKED			CUSTOMER NO. PLI-2 / DWG NO. SMS-20-WW / REV A
APPROVED	DM	5.15.75	


REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 5.12.75
INFIBUS
D9
1KΩ
Vcc
(20) VOLT1+
C2
HOLDB-
P2-24
HOLD+
HOLD-
D3
ABS1B-
P1-11
ABS2B-
P1-12
ABS3B-
P1-13
ABS1+
ABS2+
ABS3+
74S04
ABS1-[22]
ABS2-[22]
ABS3-
[22] [22]
D6
(20) RITE+
ABS1+
ABS3+
WCRL-[28]
RDAT-[26]
WDAT-[25]
STR
46CE-
STROBES ONLY ON R\W CONTROL AND R\W DATA
C1
P1
ABS4B-
ABS5B-
ABS6B-
ABS7B-
VOLT0+
ABS4+
ABS5+
ABS6+
ABS7+
G9
1KΩ
ASLS4-
ASLS5-
ASLS6-
ASLS7-
C3
74136
ABS47+
D4
ABS2+
VOLT1+
74S10
MEPLS+
B1
P2
ABS8B-
ABS9B-
AB10B-
AB11B-
ABS8+
ABS9+
AB10+
AB11+
B2
7486
ASLS8-
ASLS9-
ASLS10-
ASLS11-
ABS8+
ABS9+
ABS10+
ABS11+
D2
ADCOM-
STRB+(20)
ME+
VOLTS-
74123
130 ns
50 ns
DONE-[20]
VOLT1+
C5
22KΩ
5.6KΩ
A1
P2
AB12B-
AB13S-
AB14B-
AB15B-
AB12+
AB13+
AB14+
AB15+
ASL12-
ASL13-
B3
7486
ABS12+
ABS13+
AB14+
AB15+
AB16+
AB17+
AB18+
AB19+
C4
74S133
C6
(20) RITE-
7408
DRSTR+[22]
A2
AB16B-
AB17B-
KEY0B-
KEY1B-
P1-20
P2-20
P1-09
P2-09
AB16+
AB17+
AB18+
AB19+
VOLTS-
A4
SEE NOTE 1
RES
4.7K
B4
A3
SW-8
SEE NOTE 1
SEE NOTE 2
C6
7408
AB189+
HOLD-
STRBA+1
ADSTR+
VOLT1+
(20) STRB+
NOTES
1 - ON = SWITCH CLOSED = 1
2 - FOR 16 BIT ADDRESS SYSTEMS, P-BUS, SUBSTITUTE A JUMPER-BUG CONNECTING PINS 1, 2, 3, 12, 14
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC
CAMBRIDGE, MASS. 02138
DRAWN DRF
CHECKED
APPROVED DM 5/14/75
TITLE
SMS ADDRESS DECODING
DOCUMENT NO. PL1-2 SMS-21-WW REV A

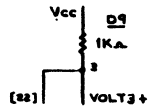
SMS

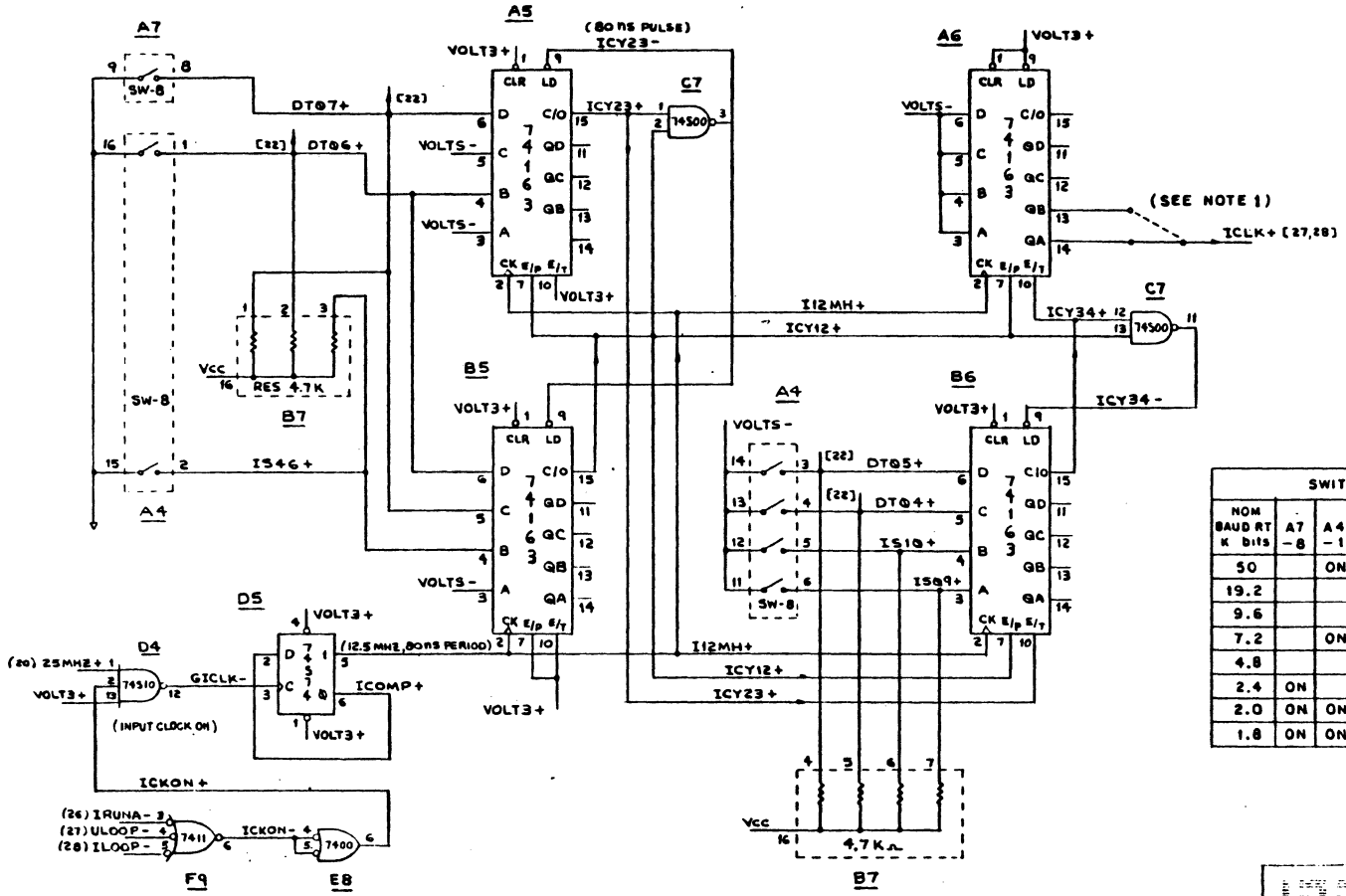

REVISION
APPD | SYM | DESCR | DATE
A | REL PROD | 5.15.75
G3
F2
E4
E2
G2
DAT15+
DAT14+
DAT09+
DAT08+
DAS15-
DAS14-
DAS09-
DAS08-
DAT07+
DAT06+
DAT05+
DAT04+
DAS07-
DAS06-
DAS05-
DAS04-
DAT03+
DAT02+
DAT01+
DAT00+
DAS03-
DAS02-
DAS01-
DAS00-
(25) ST15+
(26) RD15+
(25) ST14+
(26) RD14+
VOLTS-
(26) RD09+
VOLTS-
(26) RD08+
(21) AB02+
(21) AB01-
(21) DRSTR+
(23) VOLT3+
DRSTR+(21)
G1
F6
7400
(DEVICE TYPE "8")
(21) AB01-
(21) AB02-
DAT11-
(23) VOLT3+
DAS09-
[25] DB09+
DAS08-
[25] DB08+
DB15B-
DB14B-
DB13B-
DB12B-
DB11B-
DB10B-
DB09B-
DB08B-
P2
G4
F4
(26) RD07+
(28) CTS+
(28) STO7+
(23) DT07+
(26) RD06+
(28) DSR+
(23) VOLT3+
(23) DT06+
(26) RD05+
(28) CR05+
VOLTS-
(23) DT05+
(26) RD04+
(28) ILOOP+
(27) STO4+
(23) DT04+
DAT07+
DAT06+
DAT05+
DAT04+
VOLTS-
(21) AB02+
(21) AB01+
F1
DAS07-
[25,28] DB07+
DAS06-
[25,28] DB06+
DAS05-
[25,28] DB05+
DAS04-
[25,28] DB04+
DB07B-
DB06B-
DB05B-
DB04B-
P1
F3
E3
(26) RD03+
(28) INMRK+
VOLTS-
(24) DT03+
(26) RD02+
(28) IHIC+
VOLTS-
(24) DT02+
(26) RD01+
(28) OHIC+
VOLTS-
(24) DT01+
(26) RD00+
VOLTS-
(26) RD15+
(24) DT00+
DAT03+
DAT02+
DAT01+
DAT00+
VOLTS-
(21) AB02+
(21) AB01+
E1
DAS03-
[25,28] DB03+
DAS02-
[25,28] DB02+
DAS01-
[25,28] DB01+
DAS00-
[25,26] DB00+
DB03B-
DB02B-
DB01B-
DB00B-
INFIBUS
DRSTR+(21)
COMPUTER SYSTEMS DIVISION
DRAWN | DRF
CHECKED
APPROVED | D.M. | 5/15/75
DATA BDR'S & MUX
PLI-2 SMS-22-WW
REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	5/15/75

NOTES

1- CARD MANUFACTURED WITH ICLK+ WIRED TO A6-14, FOR BAUD RATE OF 1.2 K BITS WIRE MUST BE MOVED TO A6-13.



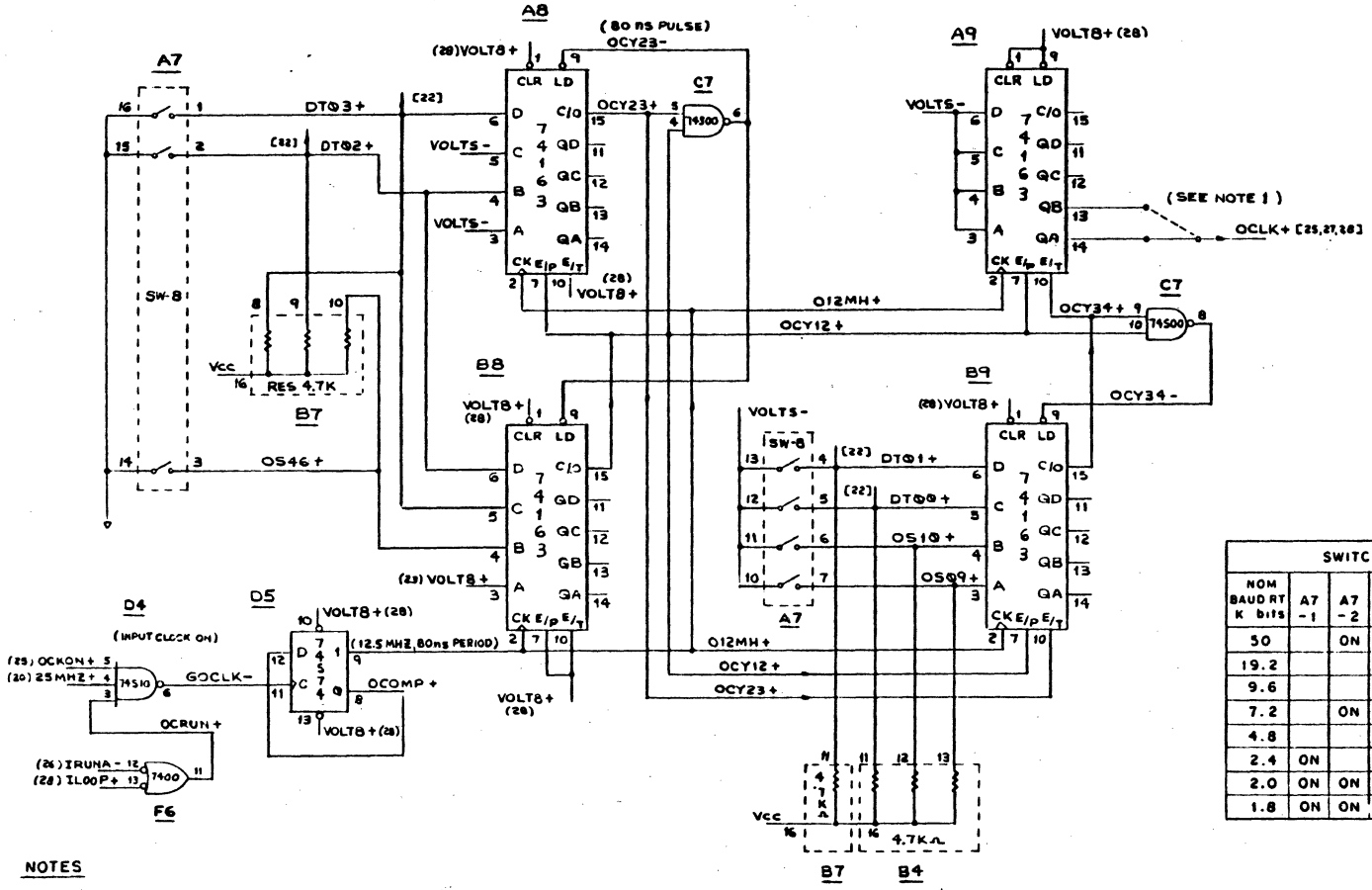


SWITCH SETTING TABLE								
NOM BAUD RT K bits	A7 -8	A4 -1	A4 -2	A4 -3	A4 -4	A4 -5	A4 -6	DATA TYPE-BITS
50		ON	ON					1011
19.2						ON	ON	1111
9.6					ON	ON	ON	1110
7.2		ON	ON		ON	ON		1010
4.8				ON	ON	ON	ON	1100
2.4	ON		ON	ON		ON	ON	0101
2.0	ON	ON		ON		ON	ON	0001
1.8	ON	ON		ON	ON		ON	0000

DRAWN	DRF	1-25	DATA INPUT CLOCK, DIVIDERS & TIMING
CHECKED			
APPROVED	JM	5/15/75	PLI-2 SMS-23-WW A

SMS

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	5.15.75



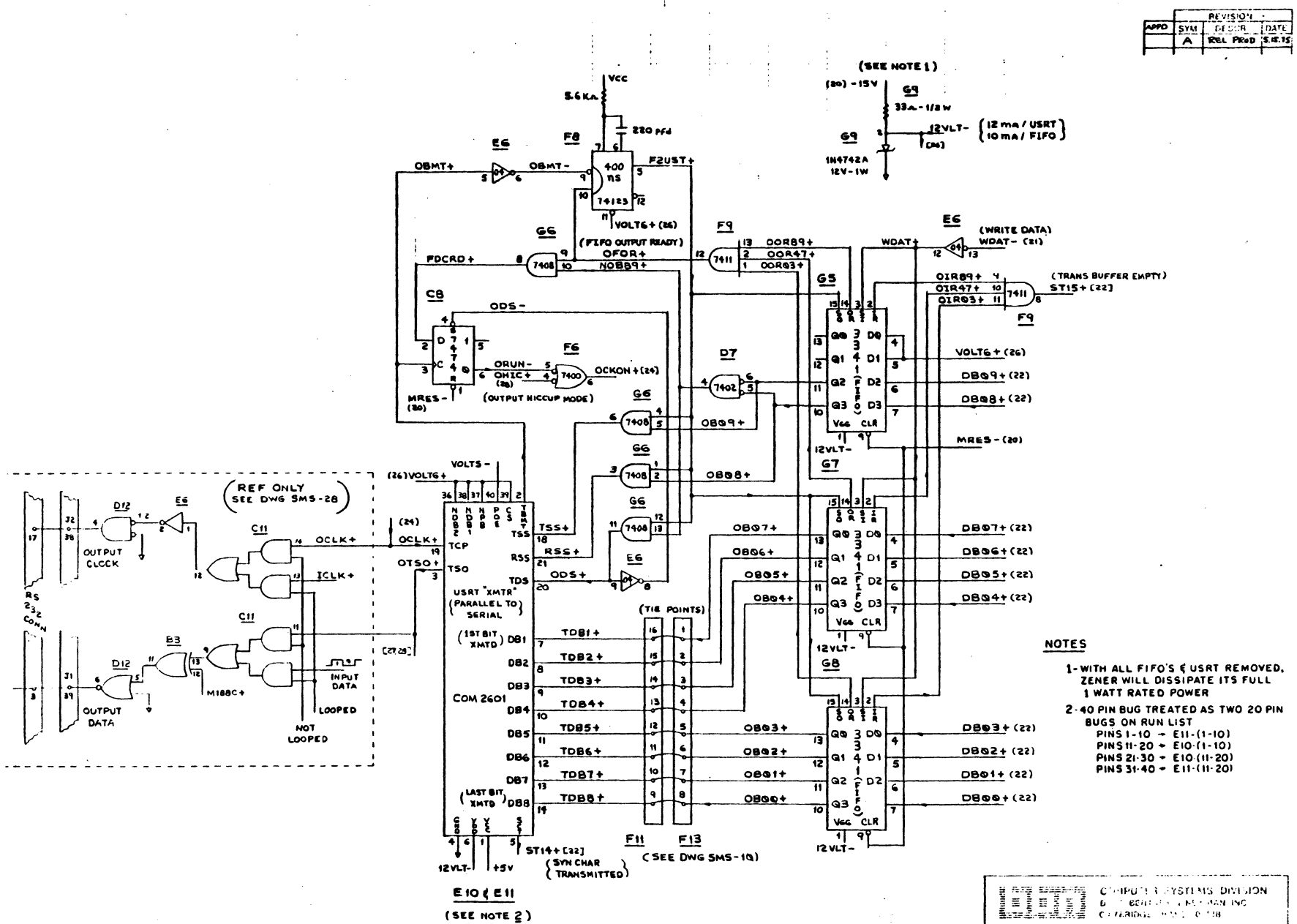
SWITCH SETTING TABLE

NOM BAUD RT K bits	A7 -1	A7 -2	A7 -3	A7 -4	A7 -5	A7 -6	A7 -7	DATA TYPE-BITS
50		ON	ON					1011
19.2						ON	ON	1111
9.6					ON	ON	ON	1110
7.2		ON	ON		ON	ON		1010
4.8				ON	ON	ON	ON	1100
2.4	ON		ON	ON		ON	ON	0101
2.0	ON	ON		ON		ON	ON	0001
1.8	ON	ON		ON	ON		ON	0000

NOTES

1 CARD MANUFACTURED WITH OCLK+ WIRED TO A9-14, FOR BAUD RATE OF 1.2K BITS, WIRE MUST BE MOVED TO PIN A9-13

DRAWN	DRF 7/75	DATA OUTPUT CLOCK, DIVIDERS & TIMING
CHECKED		
APPROVED	DM 5/5/75	PLI-2 SMS-24-WW-A



APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	5.15.75

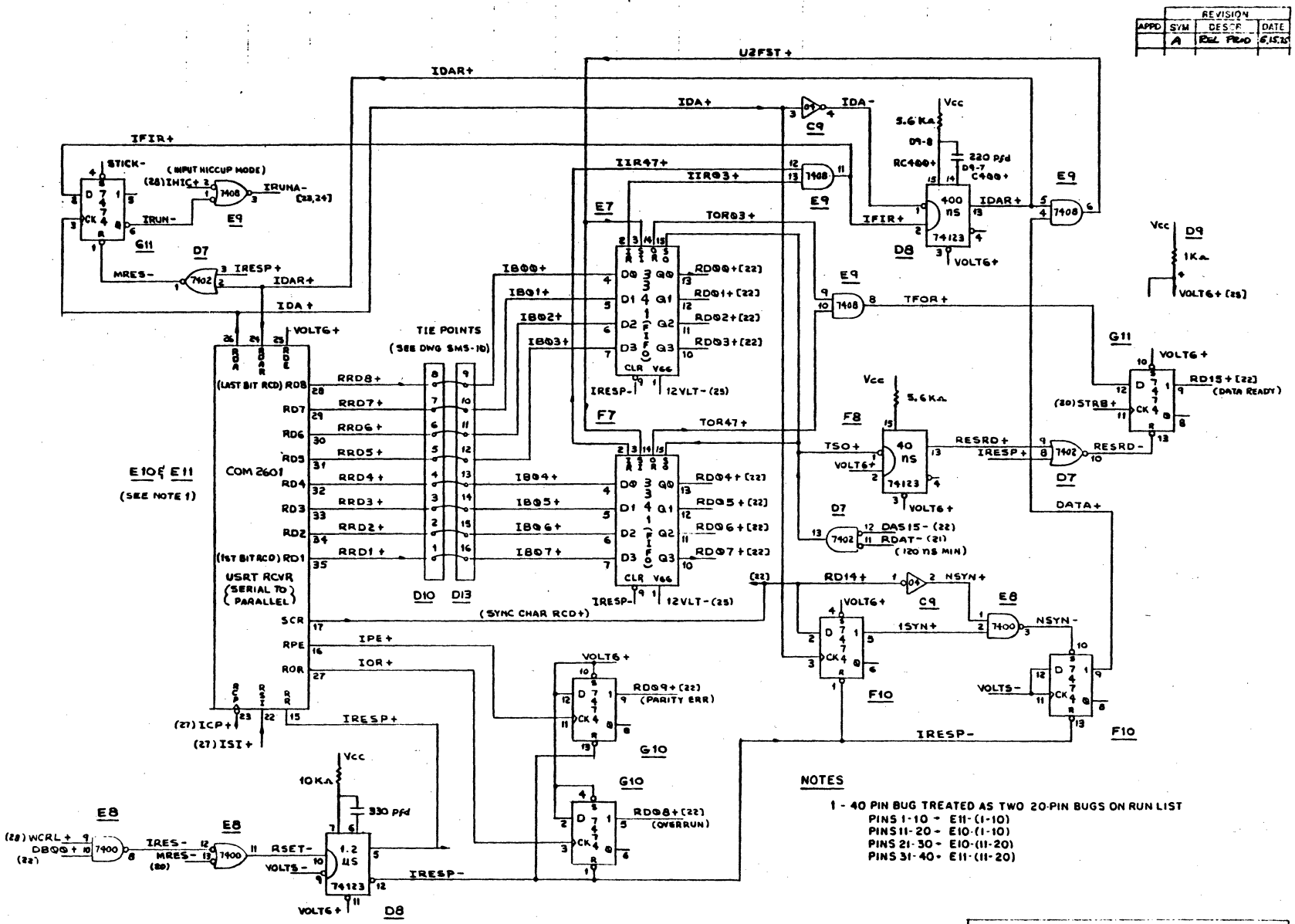
NOTES

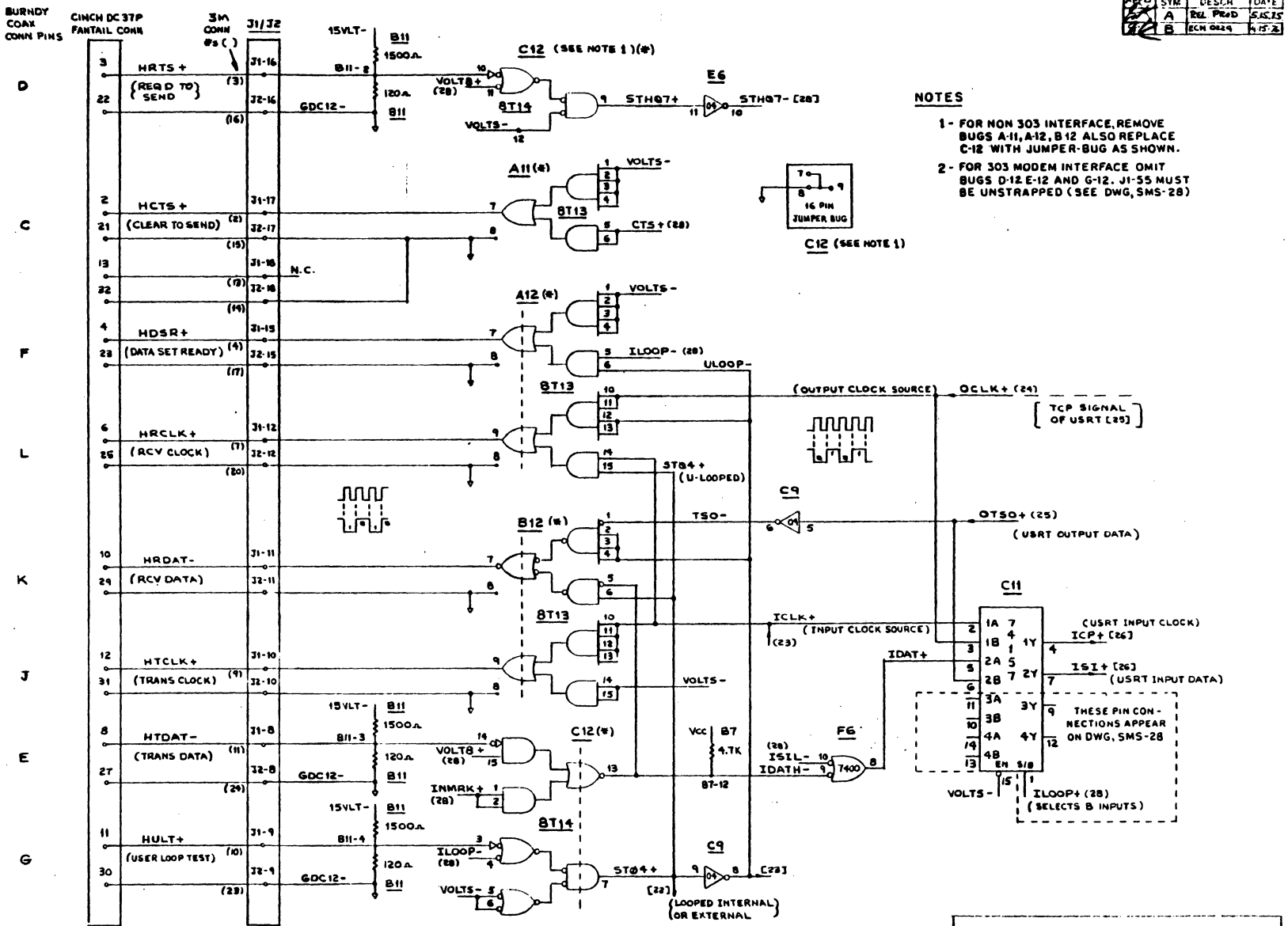
1. WITH ALL FIFO'S & USRT REMOVED, ZENER WILL DISSIPATE ITS FULL 1 WATT RATED POWER
2. 40 PIN BUG TREATED AS TWO 20 PIN BUGS ON RUN LIST
   - PINS 1-10 → E11-(1-10)
   - PINS 11-20 → E10-(1-10)
   - PINS 21-30 → E10-(11-20)
   - PINS 31-40 → E11-(11-20)

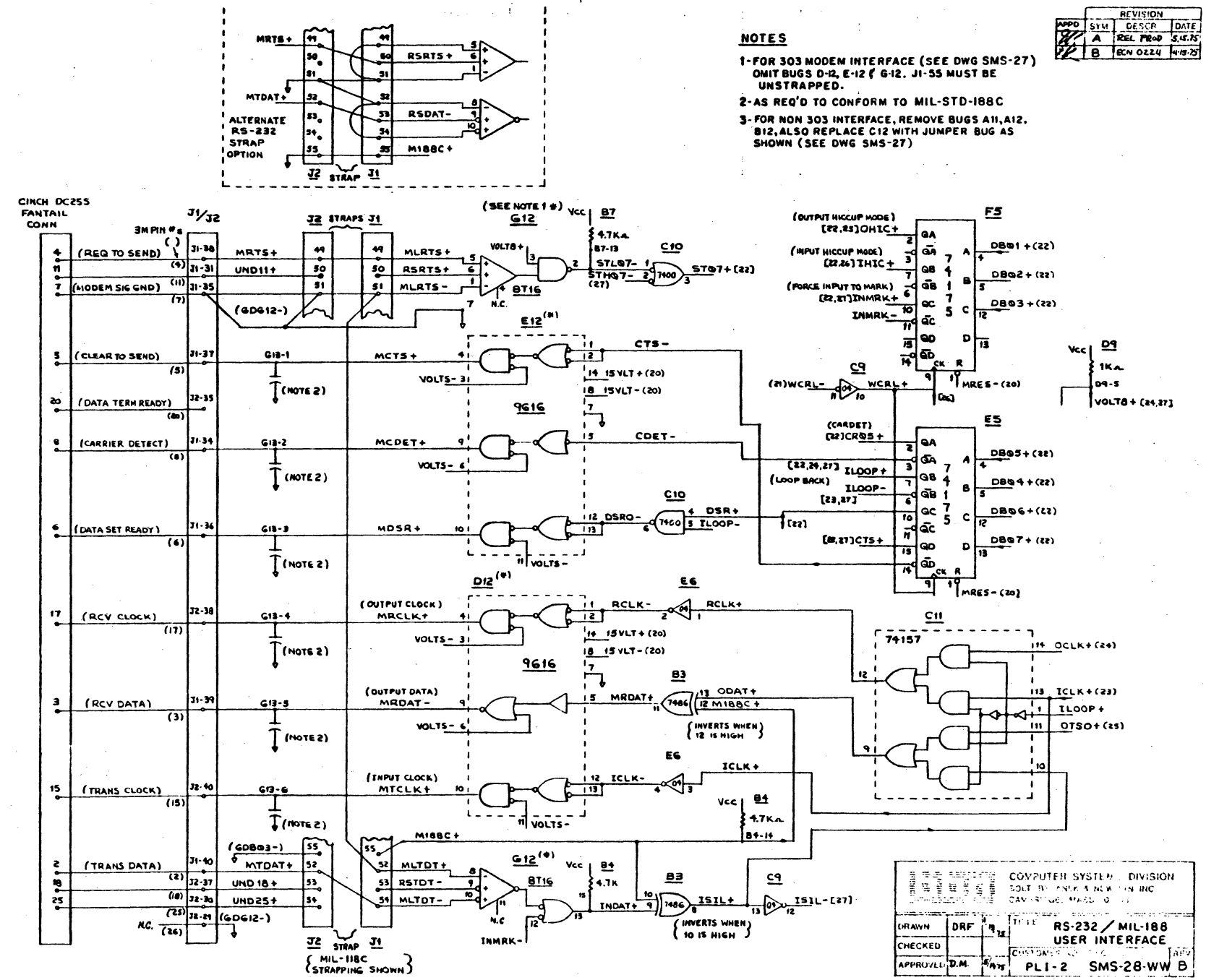
COMPUTER SYSTEMS DIVISION

DRAWN	DRF	MODEM RECEIVER USRT TRANSMITTER FIFO'S	
CHECKED		CUSTOMER NO.	DWG NO. / REV
APPROVED	DM.	PLI-2	SMS-25-WW / A

SMS


REVISION
APPD | SYM | DESCR | DATE
A | Rel Prod | 6.15.76
U2FST+
IDAR+
IDA+
IDA-
IFIR+
STICK-
(INPUT HICCUP MODE)
(28)IHIC+
IRUNA-
(23,24)
IRUN-
MRES-
IRESP+
IDAR+
IDA+
VOLT6+
TIE POINTS
(SEE DWG SMS-10)
IIR47+
IIR03+
TOR03+
IB00+
IB01+
IB02+
IB03+
IB04+
IB05+
IB06+
IB07+
RD00+[22]
RD01+[22]
RD02+[22]
RD03+[22]
RD04+[22]
RD05+[22]
RD06+[22]
RD07+[22]
IRESP-
12VLT-(25)
TOR47+
TFOR+
TSO+
RESRD+
RESRD-
DATA+
RD15+[22]
(DATA READY)
(20)STRB+
DAS15-(22)
RDAT-(21)
(120 ns MIN)
RD14+
NSYN+
1SYN+
NSYN-
VOLTS-
RD09+[22]
(PARITY ERR)
RD08+[22]
(OVERRUN)
COM 2601
USRT RCVR
(SERIAL TO PARALLEL)
(SYNC CHAR RCD+)
(LAST BIT RCD) RD8
RD7
RD6
RD5
RD4
RD3
RD2
(1ST BIT RCD) RD1
RRD8+
RRD7+
RRD6+
RRD5+
RRD4+
RRD3+
RRD2+
RRD1+
SCR
RPE
ROR
IPE+
IOR+
IRESP+
(27)ICP+
(27)ISI+
E10, E11
(SEE NOTE 1)
D10
D13
F7
F8
F10
G10
G11
E7
E8
E9
C9
D7
D8
D9
Vcc
5.6 KΩ
10 KΩ
1 KΩ
220 pfd
330 pfd
400 ns
1.2 µs
74123
7408
7400
7402
7474
RC400+
D9-8
D9-7
C400+
(28)WCRL+
DB00+
(22)
IRES-
RSET-
(80)
MRES-
NOTES
1 - 40 PIN BUG TREATED AS TWO 20-PIN BUGS ON RUN LIST
PINS 1-10 - E11-(1-10)
PINS 11-20 - E10-(1-10)
PINS 21-30 - E10-(11-20)
PINS 31-40 - E11-(11-20)
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN | DRF | 1-9-75
CHECKED
APPROVED | DM | 1/6/75
TITLE: MODEM-TRANSMITTER
USRT-RECEIVER-FIFO'S
CUSTOMER NO | REV
PLI-2 | SMS-26-WW A


BURNDY COAX CONN PINS
CINCH DC 37P FANTAIL CONN
3M CONN #s ( )
J1/J2
HRTS + (REQ'D TO SEND)
HCTS + (CLEAR TO SEND)
HDSR + (DATA SET READY)
HRCLK + (RCV CLOCK)
HRDAT - (RCV DATA)
HTCLK + (TRANS CLOCK)
HTDAT - (TRANS DATA)
HULT + (USER LOOP TEST)
N.C.
15VLT -
GDC12 -
B11
1500Ω
120Ω
C12 (SEE NOTE 1)(*)
E6
8T14
STH07 +
STH07 - [28]
VOLTS +
VOLTS -
A11 (*)
8T13
CTS + (28)
16 PIN JUMPER BUG
A12 (*)
ILOOP - (28)
ULOOP -
(OUTPUT CLOCK SOURCE)
OCLK + (24)
TCP SIGNAL OF USRT [25]
ST04 + (U-LOOPED)
B12 (*)
TSO -
C9
OTSO + (25)
(USRT OUTPUT DATA)
C11
ICLK +
(INPUT CLOCK SOURCE)
(23)
(USRT INPUT CLOCK)
ICP + [26]
ISI + [26]
(USRT INPUT DATA)
IDAT +
F6
ISIL -
IDATH -
7400
THESE PIN CONNECTIONS APPEAR ON DWG, SMS-28
ILOOP + (28)
(SELECTS B INPUTS)
INMRK + (28)
Vcc
B7
4.7K
B7-12
ST04 +
[22]
(LOOPED INTERNAL OR EXTERNAL)
NOTES
1 - FOR NON 303 INTERFACE, REMOVE BUGS A-11, A-12, B-12 ALSO REPLACE C-12 WITH JUMPER-BUG AS SHOWN.
2 - FOR 303 MODEM INTERFACE OMIT BUGS D-12 E-12 AND G-12. J1-55 MUST BE UNSTRAPPED (SEE DWG, SMS-28)
REVISION
APPD
SYM
DESCR
DATE
A
REL PROD
5/15/75
B
ECN 0829
4-15-76
COMPUTER SYSTEMS DIVISION
BOLT BERANEK & NEWMAN INC
CAMBRIDGE MASS 02138
DRAWN
DRF
CHECKED
APPROVED
D.M.
5/14/75
303 USER INTERFACE
CUSTOMER DWG NO
PL1-2
SMS-27-WW-B


MRTS+
MTDAT+
ALTERNATE RS-232 STRAP OPTION
RSRTS+
RSDAT-
M188C+
J2 STRAP J1
NOTES
1-FOR 303 MODEM INTERFACE (SEE DWG SMS-27) OMIT BUGS D-12, E-12 & G-12. J1-55 MUST BE UNSTRAPPED.
2-AS REQ'D TO CONFORM TO MIL-STD-188C
3-FOR NON 303 INTERFACE, REMOVE BUGS A11, A12, B12, ALSO REPLACE C12 WITH JUMPER BUG AS SHOWN (SEE DWG SMS-27)
REVISION
APPD SYM DESCR DATE
A REL PROD 5.15.75
B ECN 0224 6-19-75
CINCH DC25S FANTAIL CONN
3M PIN #s
J1/J2
J2 STRAPS J1
(REQ TO SEND)
(MODEM SIG GND)
MRTS+
UND11+
MLRTS+
RSRTS+
MLRTS-
(GDG12-)
(SEE NOTE 1 *)
G12
VCC
B7
4.7KΩ
VOLT8+
BT16
N.C.
C10
STL07-
STH07-
(27)
7400
ST07+ [22]
E12 (*)
(CLEAR TO SEND)
(DATA TERM READY)
(CARRIER DETECT)
(DATA SET READY)
(RCV CLOCK)
(RCV DATA)
(TRANS CLOCK)
(TRANS DATA)
G13-1
G13-2
G13-3
G13-4
G13-5
G13-6
(NOTE 2)
MCTS+
MCDET+
MDSR+
MRCLK+
MRDAT-
MTCLK+
MTDAT+
UND18+
UND25+
VOLTS- 3
VOLTS- 6
VOLTS-
15 VLT+ (20)
15 VLT- (20)
9616
CTS-
CDET-
DSRQ-
DSR+
ILOOP-
RCLK-
RCLK+
ICLK-
ICLK+
MRDAT+
ODAT+
M188C+
(INVERTS WHEN 12 IS HIGH)
(INVERTS WHEN 10 IS HIGH)
B3
B4
4.7KΩ
E6
D12 (*)
C11
74157
OCLK+ (24)
ICLK+ (23)
ILOOP+
OTSO+ (25)
F5
E5
(OUTPUT HICCUP MODE) [22,25]OHIC+
(INPUT HICCUP MODE) [22,26]IHIC+
(FORCE INPUT TO MARK) [22,27]INMRK+
INMRK-
DB01+ (22)
DB02+ (22)
DB03+ (22)
DB04+ (22)
DB05+ (22)
DB06+ (22)
DB07+ (22)
MRES- (20)
(21)WCRL-
WCRL+
C9
D9
1KΩ
D9-5
VOLT8+ [24,27]
(CARDET) [22]CRQS+
[22,24,27] ILOOP+
(LOOP BACK) ILOOP- [23,27]
[22]
[23,27]CTS+
(GDB03-)
J2 STRAP J1
(MIL-118C STRAPPING SHOWN)
N.C.
INDAT+
IS1L+
IS1L-[27]
INMRK-
COMPUTER SYSTEMS DIVISION
CAMBRIDGE, MASS.
DRAWN DRF
CHECKED
APPROVED D.M.
TITLE RS-232 / MIL-188 USER INTERFACE
CUSTOMER PLI-2
SMS-28-WW B
REV

Switch Panel Board

SWB-Ø2 Logic Description

SWB-Ø5 Technical Reference

SWB-15 Standard Modification

SWB-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SEE PBI-Ø2

SWB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER

APP'D FOR BEL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

SWB LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		SWB-Ø2

SCALE	REV	SHEET 1 OF 1

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	[redacted]	

SWB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

	CONTRACT NO:	Bolt Beranek and Newman Inc. Cambridge Massachusetts
	DRAFTSMAN [redacted]	DRAWING TITLE SWB TECHNICAL REF
	CHECKER	
	ENGINEER	
	APP'D FOR REL	SIZE A | CODE IDENT NO. | DRAWING NO. SWB-65
	APP'D (CUSTOMER)	SCALE | REV A | SHEET 1 OF 2

A

SWB - SWITCH PANEL BOARD - CONTROL PANEL Lockheed

also see PBI-Ø5, PCB-Ø5

Status - address none

Switches

Power Fail Interrupt Enable on-off

Line Frequency Interrupt Enable on-off

Power Recovery off-interrupt (in) - autoload (al)

Key Bit Select (S73)

Off: Key bits ØØ, Processor Ø
On: Key bits Ø1, Processor 1

All other switches are self-explanatory

Jumpers - none

SWB

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	2/[illegible]/72	

SWB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

SWB MODIFICATION STND

SIZE	CODE IDENT NO.	DRAWING NO.
A		SWB-15

SCALE	REV	SHEET
	A	1 OF 4

A

Card Type SWB Modification Standard

Card Function: Control Panel

Modification Description:

Add switch for selection of key bits for console references.
Add switch for continuous read/write.

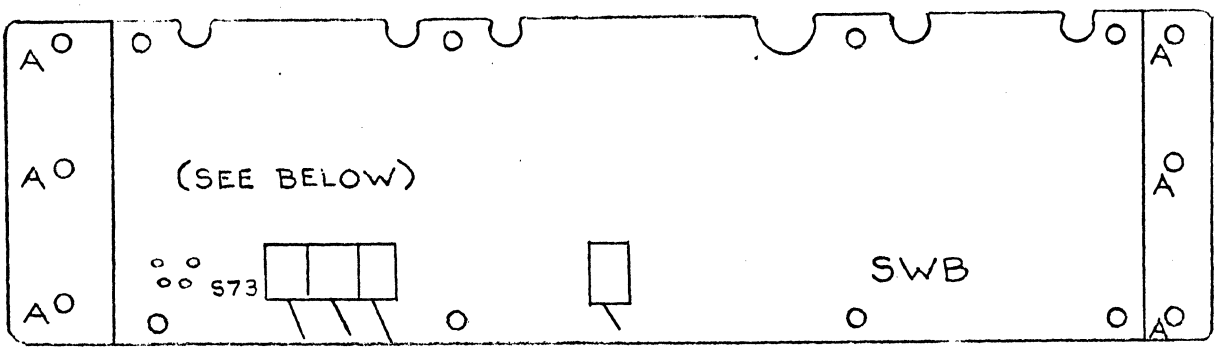
Implementation:

Install S68 and S73 as per sketch if not already present.
Modify board as described on page 2.

SWB

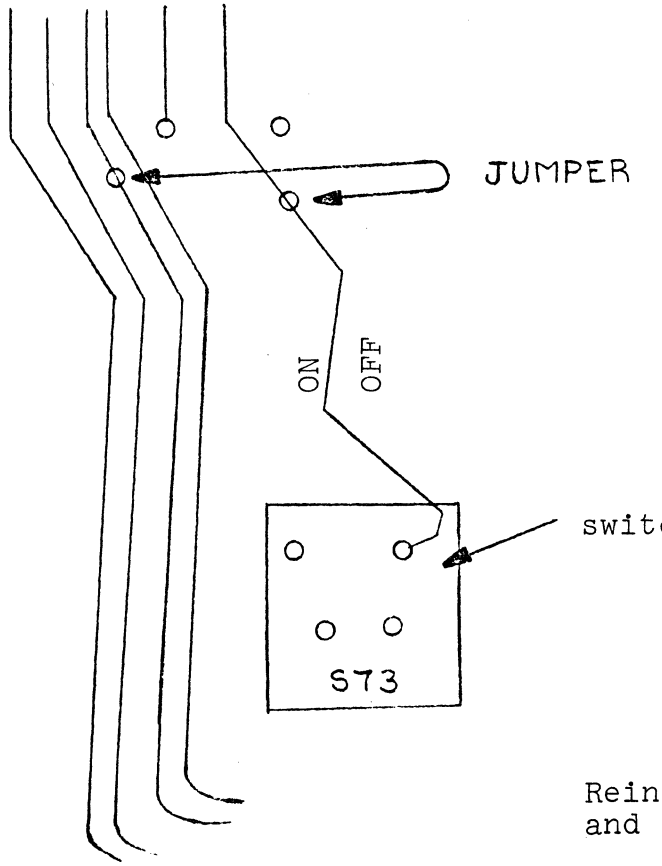
Fix to console (2) on SWB board (front panel)

Turn so that front side (with numbers, etc.) faces down.
If you see a PC board, remove 8 hex head screws from top and bottom (not the 3 on each side); otherwise, remove metal plate by removing 8 screws and spacers.
Install a red-handled switch in holes labeled S73.



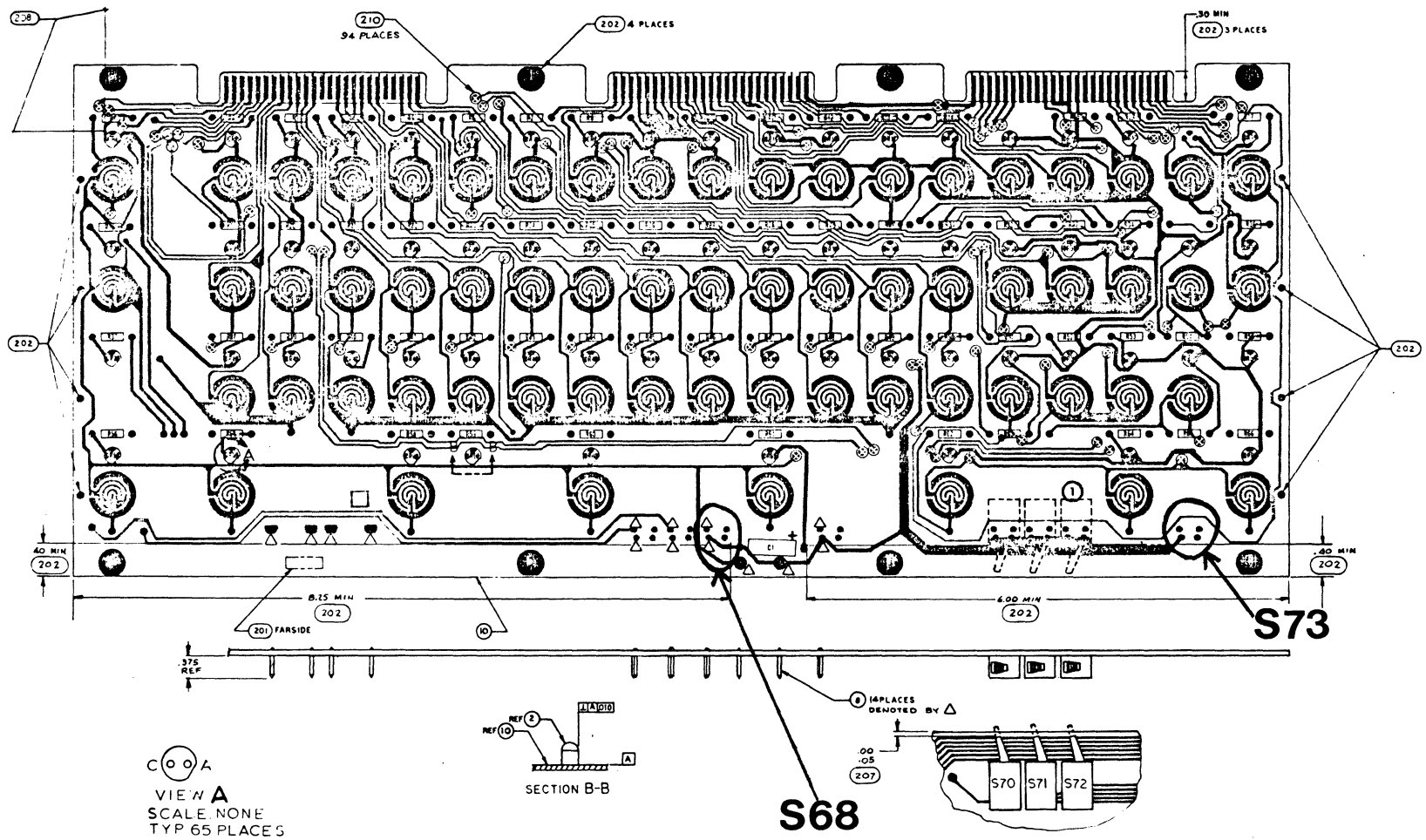
Install from side you are looking at, solder on other side, clip leads and put PC board back in place.

Jumper two traces together with insulated wire as below:



switch you just installed

Reinstall cover plate (if any) and screws.


210
94 PLACES
202 4 PLACES
.30 MIN
202 3 PLACES
208
202
202
.40 MIN
202
.40 MIN
202
8.25 MIN
202
6.00 MIN
202
201 FARSIDE
10
.375
REF
S73
8 PLACES
DENOTED BY △
.00
.05
207
S70
S71
S72
S68
C
O
O
A
VIEW A
SCALE NONE
TYP 65 PLACES
REF 2
REF 10
.010 A A
A
SECTION B-B

SWB

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SEE PBI-Ø2

SWB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN 12/8/75

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

SWB SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		SWB-2Ø

SCALE	REV	SHEET 1 OF 1

Memory Timing

TAG-Ø2 Logic Description

TAG-Ø5 Technical Reference

TAG-15 Standard Modification

TAG-2Ø Schematic

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	[redacted]	

TAG

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN [redacted] 12/19/75

CHECKER

ENGINEER [redacted]

APP'D FOR REL [redacted]

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

TAG LOGIC DESCRIPTION

SIZE	CODE IDENT NO.	DRAWING NO.
A		TAG - Ø2

SCALE	REV	SHEET OF
	A	

SUE 3310 4K MAGNETIC CORE MEMORY MODULE

MAINTENANCE BULLETIN M3310

TAG

1526

Dec 74

CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SUE 3310 4K MAGNETIC CORE MEMORY MODULE

MAINTENANCE BULLETIN

INTRODUCTION

The SUE model 3310 Magnetic Core Memory Module provides random access storage for data and programmed instructions in SUE Computer systems. The memory module is a 3-wire, 3D, coincident-current core memory for storage of up to 4096 16-bit words comprising two 8-bit bytes each. Cycle time for the model 3310 is 800 nanoseconds nominal with a read access time of 460 nanoseconds.

DESCRIPTION

A model 3310 memory module comprises three standard sized SUE printed circuit (PC) cards as follows:

- memory electronics and XY stacks (EXY),
- sense and inhibit drivers (SID),
- timing and gating (TAG).

In addition to the three basic PC cards an interconnecting module (ICM) plugs into the free edges of the three cards to interface control and data lines. The three memory PC cards plug into three consecutive INFIBUS slots in the order specified under paragraph heading Installation Considerations.

TAG

FUNCTION

Figure 1 is a general block diagram of the SUE model 3310 Magnetic Core Memory Module showing the basic data flow, key source logic terms associated with the flow (with the logic page number where these terms are defined), and the circuit boards where each function originates. A description of the functional operation of each block follows the block diagram. Three functions, timing

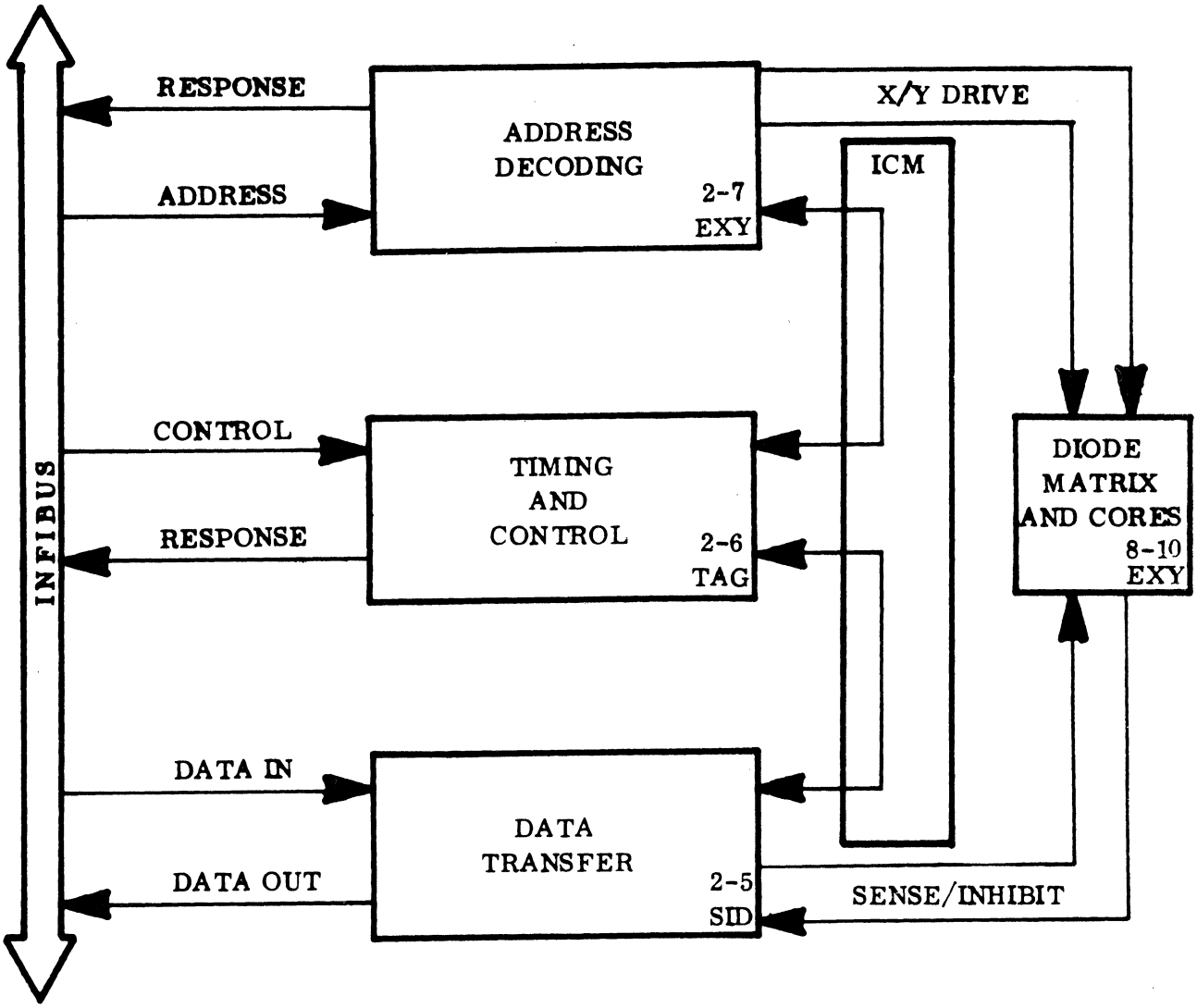


Figure 1. SUE 3310 Memory Functional Block Diagram

control, address control, and data flow control are required for core storage of data and programmed instruction in any computer system. Figure 1 identifies the three modules associated with each of these functions in a SUE Computer system. The TAG and EXY circuit cards comprise the timing and address control functions, and the SID circuit card comprises the data flow control functions.

Two types of addressing are associated with the address control function. First the memory module must be uniquely addressed and secondly each data location within the selected memory module must be uniquely identified. Module addressing is semi-permanently coded onto the TAG circuit card by jumper wires. Each core storage address (4096 data locations) within the selected module is program selectable through a matrix of 64 X coordinate wires (X-lines) and 64 Y coordinate wires (Y-lines) located on the EXY circuit card.

Data sense and inhibit control functions are located on the SID circuit card. This circuit card also comprises the data registers, gates and switches as well as line drivers and receivers for handling data to or from core storage and the INFIBUS.

TAG Circuit Card

The TAG circuit card contains the module address decoding circuits and all control logic. All timing, gating and monitoring logic of the model 3310 memory module responds to STRB-N from the processor via the INFIBUS that initiates the memory cycles whose mode of operation is determined by RITE, HCYC, BYTE and AB00 control signals.

TAG

Internal timing signals that control memory during execution of the storage cycles in the three modes of operation, i.e., Clear-Write (C/W), Read-Restore (R/R) and Read-Modify-Write (R/M/W), are generated by the TAG card delay lines. However, the effectiveness of the timing signals is at all times subject to modification by control signals from the processor.

EXY Circuit Card

The EXY circuit card contains the core storage stacks, XY diode matrix, address register and decoding logic, XY current sources, and core driver circuits.

Core Storage

The basic storage elements in the model 3310 memory module are 18 mil lithium-ferrite cores. The cores are mounted in arrays called mats; each mat contains 4096 cores arranged in a 64 x 64 matrix. These mat-arrays are mounted on both sides of a frame, nine mats to the side, arranged in 3 x 3 matrices. The frame (core stack) is then mounted on the EXY circuit card. The extra mat on each side of the frame is used for memories with parity bits (i.e. one parity bit per 8-bit byte) and is not used on the model 3310 memory module. One core in each mat is selected by 1 of 64 X-drive lines and 1 of 64 Y-drive lines during a read or write cycle.

Each mat (corresponding to a data bit) has a sense and inhibit line through all cores connected to one of 16 sense amplifiers and 1 of 16 inhibit driver circuits located on the SID circuit card.

Address Register and Decoding Circuits

Address bits 12 through 1 from the INFIBUS are stored in the storage address register and applied to decoder logic that selects 1 of 64 possible X-driver lines and 1 of 64 possible Y-driver lines in the memory stack unique for the decoded address.

SID Circuit Card

The SID circuit card contains all data transfer logic consisting of the sense amplifiers and inhibit drivers, the data register, data gates, as well as the line drivers and receivers. The data register circuits receive data from the INFIBUS during write operations, and from core during read operations. In a write operation, data coming from the INFIBUS is loaded into the data register and then written into the addressed core location during the write half of the

storage cycle. In a read operation, data that is destructively read out of a core location during the read half of the storage cycle, is loaded into the data register to be restored into the same core location by writing it back during the write half of the storage cycle.

INSTALLATION CONSIDERATIONS

The SUE model 3310 Magnetic Core Memory Module can be plugged into any three consecutive INFIBUS slots. However, in stacked, multi-chassis SUE configurations, memory modules should be plugged into the INFIBUS in locations that assure maximum air flow.

After selecting the most favorable location on the INFIBUS, code the TAG and EXY circuit cards for the address and modes of operation desired by installing jumper wires as shown in table 1. Then refer to table 2 and check that all timing and configuration jumpers are properly installed as shown in the table.

NOTE

For location of jumper terminals refer to TAG Assembly Drawing sheet 1 and EXY Assembly Drawing sheet 1.

Finally referencing the SID circuit card identification tag check that it is a 2001002155-3 configuration.

After installing and checking all jumper connections install the three memory circuit cards into three consecutive INFIBUS slots as defined earlier and interconnect the free edge of the circuit cards using the ICM.

TAG

Table 1. Model 3310 Memory Address and Mode Jumpers

	TAG Circuit Card		EXY Circuit Card	
Address Or Mode	Remove Jumpers*	Install Jumpers**	Remove Jumpers*	Install Jumpers**
ADDRESS				
0-4K	-	J2A5 to J2B5 J2A6 to J2B6 J2A7 to J2B7		
4-8K	E201-E208			
8-12K	E203-E210			
12-16K	E201-E208 and E203-E210			
16-20K	E206-E213			
20-24K	E201-E208 and E206-E213			
24-28K	E203-E210 and E206-E213			
28-32K	E201-E208, E203-E210, and E206-E213	J2A5 to J2B5 J2A6 to J2B6 J2A7 to J2B7		
GENERAL	-	E141-E142		
MODE				
INTERLOCK	J4-2 to J4-3	J4-3 to J4-1	J3-1 to J3-2	J2-1 to J2-2
OVERLAP	J4-3 to J4-1	J4-2 to J4-3		
INTERLEAVE	E202 to E209 (2nd memory only) J4-3 to J4-1	J2A4 to J2B4 J4-2 to J4-3	J2-1 to J2-2	J3-2 to J3-3
BLIND				
30-32K	J3-1 to J3-2	J2A1 to J2B1		
31-32K	-	J3-1 to J3-2 J2A1 to J2B1		

*If they exist
**If not present

Table 2. Model 3310 Memory Timing and Configuration Jumpers

TAG Circuit Card	
Jumpers Installed	Jumpers Removed
E34 to E24	J2A2 to J2B2
E35 to E9	J2A3 to J2B3
E36 to E17	J2A4 to J2B4
E47 to E87	J5-2 to J5-3
E48 to E2	
E55 to E73	
E67 to E9	
E71 to E131	
E72 to E82	
E141 to E142	
J5-1 to J5-2	
J2A5 to J2B5	
J2A6 to J2B6	
J2A7 to J2B7	
E201 to E208	
E202 to E209 (1)	
* (2)	
E204 to E211	
E205 to E212	
* (2)	
E207 to E214	

NOTES (1) Not installed on second TAG circuit card if interleaving mode.

(2) Jumpers between E203 to E210 and E206 to E213 dependent upon module address. Reference table 1 for double check.

TAG

LOGIC DESCRIPTION

Figure 2 is a detailed block diagram of the SUE 3310 Magnetic Core Memory Module that corresponds directly with the logic diagrams and their descriptions. The number in the upper left-hand corner of each block refers to the logic diagram sheet number where the corresponding logic is located. Logic descriptions and key source logic definitions are contained on the sheet preceding each logic diagram.

DRAWINGS AND PARTS LISTS

SUE 3310 memory module assembly drawings, logic diagrams, and parts lists are collected in the following pages in the order listed below.

Title	Drawing Number	Sheets
SUE 3310 Timing and Gating (TAG) Circuit Card Assembly	2001002273	1
SUE 3310 Timing and Gating (TAG) Logic Diagram	LD2001002273	1 thru 6
SUE 3310 Memory Electronics and XY Matrix (EXY) Circuit Card Assembly	2001002219-2	1
SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram	LD2001002219-2	1 thru 10
SUE 3310 Sense, Inhibit Data (SID) Circuit Card Assembly	2001002155	1
SUE 3310 Sense, Inhibit Data (SID) Logic Diagram	LD2001002155	1 thru 5
SUE 3310 Timing and Gating (TAG) Parts List	PL2001002273	3, 4, 6, 8
SUE 3310 Memory Electronics and XY Matrix (EXY) Parts List	PL2001002219-2	4 and 5
SUE 3310 Sense, Inhibit Data (SID) Parts List	PL2001002155	8 thru 10

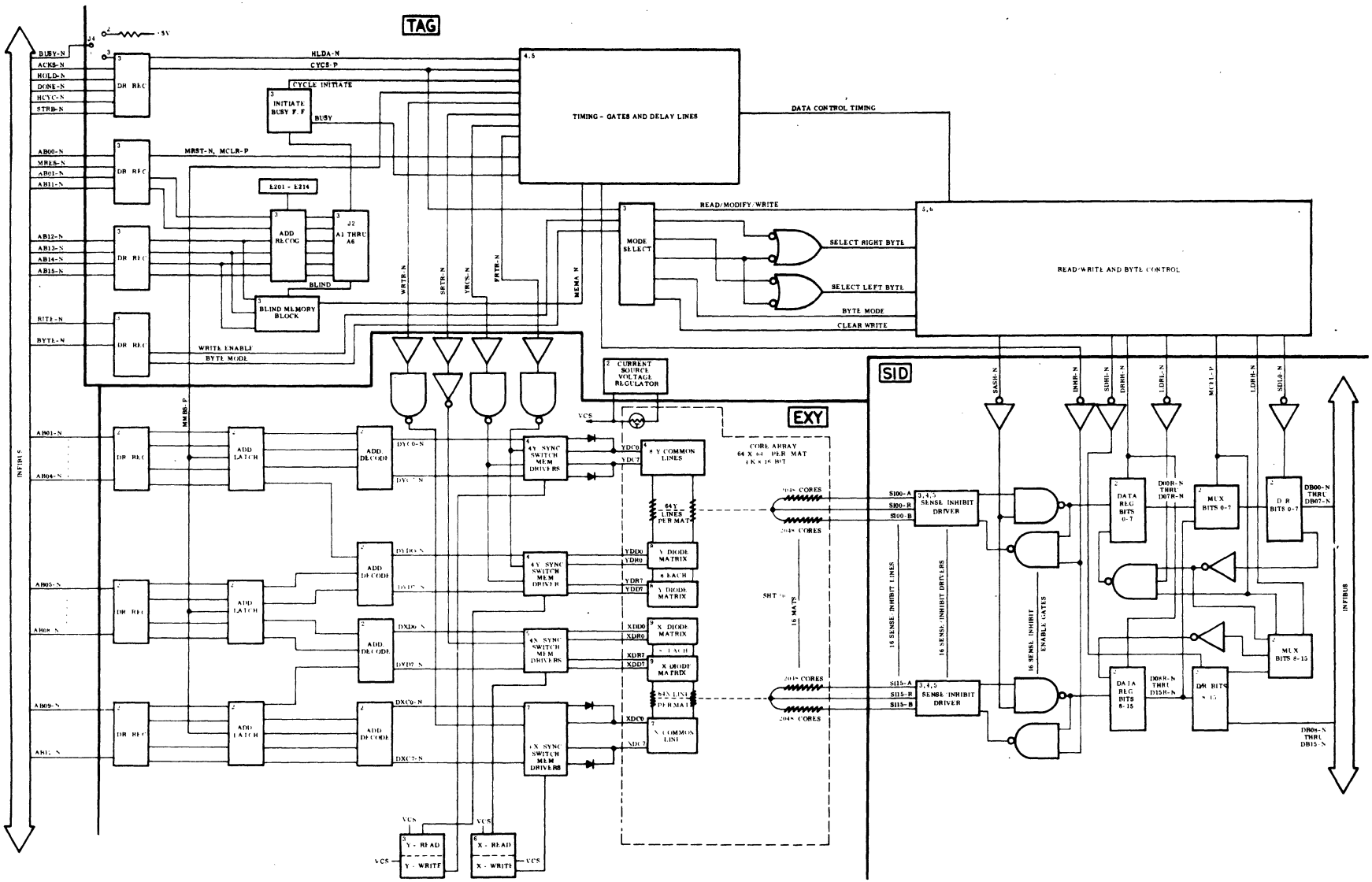
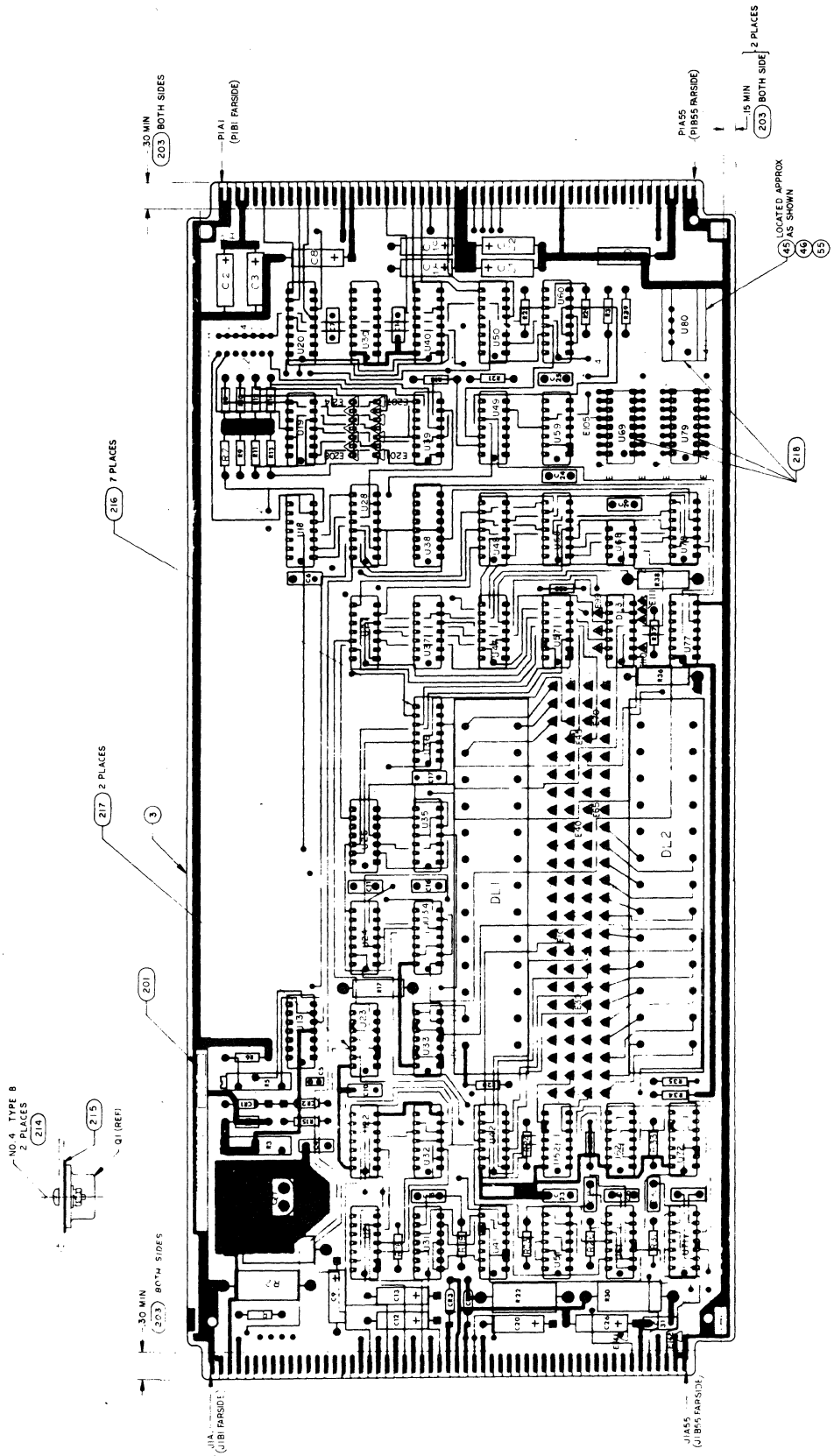


Figure 2. SUE 3310 Memory Detailed Block Diagram



SUE 3310 Timing and Gating (TAG) Circuit Card Assembly
2001002273, Rev. D, Sheet 1

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE 33UF, ±20%, 10V.
4. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATORS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST (REFERENCE LIST ON DRAWING 8001800200).
5. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V, EXCEPT U6A7723393 (U13), PIN 7 0V, PIN 12 +15V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR, PIN 7 AND 8 0V, PIN 16 +5V AND T75, PIN 12 0V, PIN 5 +5V.
6. +5V CONNECTOR PINS ARE: P1-A28, A29, A51, B28, B29, B51.
7. 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J1-A1, A2, A4, A18, A20, A22, A24, A26, A28, A30, A32, A50, A52, A55, J1-B1, B2, B4, B18, B20, B22, B24, B26, B28, B30, B32, B50, B52, B54, B55.
8. +5VA CONNECTOR PINS ARE: P1-A16, B16.
9. +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4; J1-A31.
10. -15V CONNECTOR PINS ARE: P1-A52, A53, B52, B53.
11. ALL TIMING JUMPERS FOR 2001002273-1 AND -2 CONFIGURATIONS ARE IDENTICAL EXCEPT AS SHOWN IN TABLE I.
12. ◯ DENOTES COMMON SIGNAL.

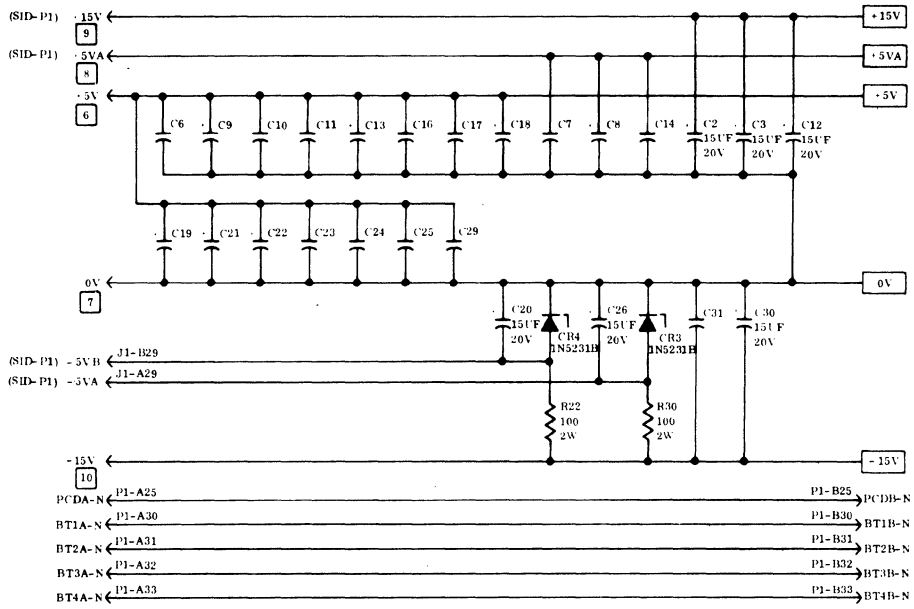


TABLE I - TIMING WIRE LIST [11]

FROM		TO (LD2001002273-1 (3312) (3212))		TO (LD2001002273-2 (3310) (3210))	
E72	SH 4	E90 (DL2-130)	SH 5	E82 (DL2-104)	SH 5
E67	3	E2 (DL1-287.5)		E9 (DL1-237.5)	
E55	5	E75 (DL2-65)		E73 (DL2-71.5)	
E47	6	E131 (DL2-0)		E87 (DL2-26)	
E71	6	E87 (DL2-26)		E131 (DL2-0)	
E34	6	E21 (DL1-162.5)		E24 (DL1-137.5)	
E45	6	E9 (DL1-262.5)		E9 (DL1-237.5)	
E36	6	E17 (DL1-200)		E17 (DL1-187.5)	
E48	4	E85 (DL2-52.5)	5	E2 (DL1-287.5)	5
E142	3	—		E141	3
J2-B7	SH 3	—		J2-A7	SH 3

+5V
R21
1K
A

TAG

SUE 3310 Timing and Gating (TAG) Logic Diagram
LD2001002273, Rev. D, Sheet 1 of 6

CURRENT SOURCE VOLTAGE REGULATOR (TAG LD Sheet 2)

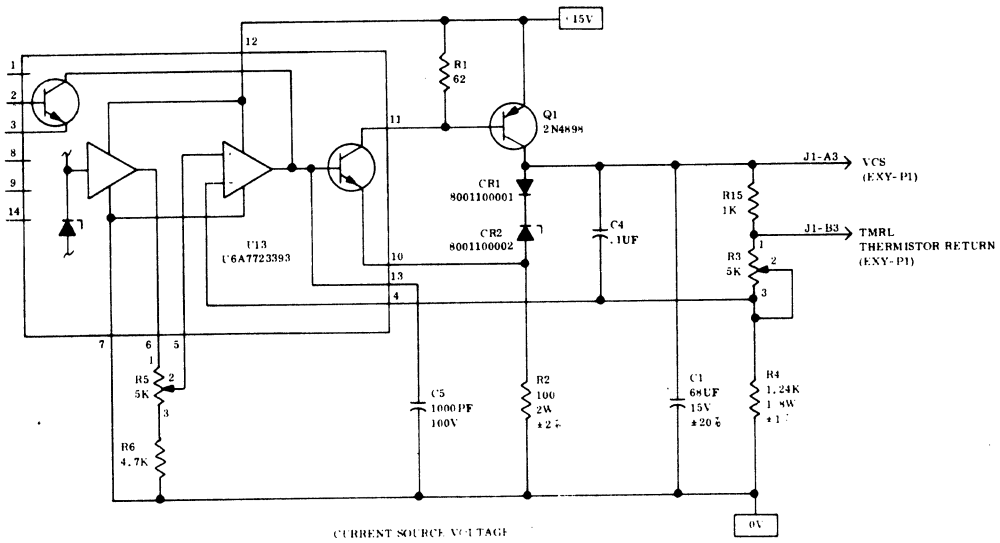
The current source voltage regulator (VCS regulator) controls a bus voltage at pin J1-A3 for the X and Y driver currents on the EXY circuit card. The X and Y driver currents are proportional to the VCS voltage which must track temperature at a rate of minus 1 volt per 25°C in order to assure proper memory operation. Regulation and temperature compensation are assured by a differential amplifier in the U13 integrated voltage regulator (on the TAG board) and a thermistor mounted to the core plane (on the EXY board).

The U13 integrated voltage regulator drives a PNP pass transistor Q1 that receives its upstream voltage from the +15 volt supply and provides the regulated VCS output voltage at J1-A3. The differential amplifier within U13 compares the voltage fed back from the output (through R3) into pin 4 to a reference voltage (controlled by R5) at pin 5. When R5 is set so that 5 volts exists at pin 5, the voltage at pin 4 is driven to 5 volts by the regulator circuit. When properly set, a 4 milliamperes divider current through the 1.24K ohm resister R4 maintains the proper value for conversion of the thermistor resistive variations into voltage changes to maintain a steady, regulated output voltage at VCS. Potentiometer R5, therefore, sets the required temperature compensation and R3 sets the center operating voltage for VCS independent of temperature compensation. For normal operation, R3 is set so that VCS is 10 volts at 25°C operating temperature of the memory stack. For test purposes, R3 can be varied to explore the operating limits of memory.

The current source voltage regulator also contains short circuit and saturation protection provided by CR1, CR2, and R15.

KEY SOURCE LOGIC DEFINITIONS

TMRL	Thermistor output return from core stack.
VCS	Regulated X and Y current driver voltage to EXY board.



TAG

SUE 3310 Timing and Gating (TAG) Logic Diagram
LD2001002273, Rev. D, Sheet 2 of 6

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MODULE SELECTION AND ADDRESS RECOGNITION (TAG, LD Sheet 3)

Memory cycle initiation for a memory bank can only occur when the memory-bank address portion of the memory address from the INFIBUS matches exactly that address patched into the TAG board by address recognition jumpers E201 through E214. By jumpering these TAG-board connections, as shown in Table II of TAG logic drawing sheet 3, each 3310 memory module is assigned a specific memory bank address of 0-4K, 4-8K, 8-12K, 12-16K, 16-20K, 20-24K, 24-28K, or 28-32K. When all jumpers are installed (i.e. E201 through E207 are jumpered to E208 through E214 respectively) the assigned memory bank address is 0-4K. When the jumper between E201 and E208 (jumper number 1) is removed, address bit 13 is always asserted so that the memory bank address is 4-8K. Asserting the 14 bit only selects a memory bank address of 8-12K and so on per table II.

Bit 1 is used for odd/even bank assignment when interleaving (see Interleaving Mode). Bits 16 and 17 are always negated (i.e. jumpers 4 and 5 are always installed).

Jumper connector J2 is used to activate the memory-bank address recognition logic (U19 and U39) to be used by the memory module (i.e. bits 14 and 15 are used for 8K modules while bits 13, 14, and 15 are used for 4K module addressing) and to enable memory blinding logic. Table II and boxed notes on TAG logic drawing sheet 3 identify the various jumper configurations for interleaving and memory blinding.

Memory Blinding

Address $F000_{16}$ through $FFFF_{16}$ are reserved on SUE systems to uniquely identify the various I/O controllers and system hardware registers that are directly addressable. This 2K word address space is larger than normally required. Therefore, SUE I/O controllers and system modules are assigned device addresses in the range $F800_{16}$ through $FFFF_{16}$, leaving $F000_{16}$ through $F7FF_{16}$ for customer use as memory space or addressing for custom modules.

Since it is possible for memory modules to recognize this 2K word address block, logic (U28) is provided on each memory module to blind the memory to these addresses. U28 is removed from 4K (3310) memory modules. Blinding logic is not provided on 4K (3310) memory modules since half of the module would be blocked from use. If blinding is desirable (on a 32K memory system), the last 8K (24-32K) of memory should be provided by an 8K (3312) memory module.

Interleave Mode

Two 3310 memory modules can be made to operate in interleave mode by adding jumpers to the TAG board. In interleave mode one memory responds to even addresses and the other responds to odd memory addresses.

Interleaving between two 3310 memories is enabled by jumpering J2-A4 to J2-B4 on both TAG boards and on the first TAG board only (closest to the processor on the INFIBUS) jumpering E202 to E209. This enables interleaving logic and assigns an even address to the first memory bank and odd address to the second memory bank respectively.

It is also necessary when initiating interleave mode to remove the jumper from J2-2 to J2-1 and install a jumper from J3-2 to J3-3 on both EXY circuit boards in the two memories. This interchanges address bits 1 and 13 to implement odd and even memory addressing of the two memory modules. In addition the two memory modules should be configured for overlap mode if interleaving is to be used.

MODULE SELECTION AND ADDRESS RECOGNITION (TAG, LD Sheet 3) (continued)

Overlap Mode

Overlap mode allows two memory modules to be operated nearly simultaneously within the same system by accepting the next cycle in one memory before the current cycle is completed in the other memory. This configuration minimizes the time required on the INFIBUS for communication between a master module and memory.

Overlapping mode is enabled by removing a jumper between J4-1 and J4-3 and adding a jumper between J4-2 and J4-3 on both memory modules. This negates HLDA-N releasing HOLD on the INFIBUS allowing the second memory module to be accessed during a memory cycle on the first memory module.

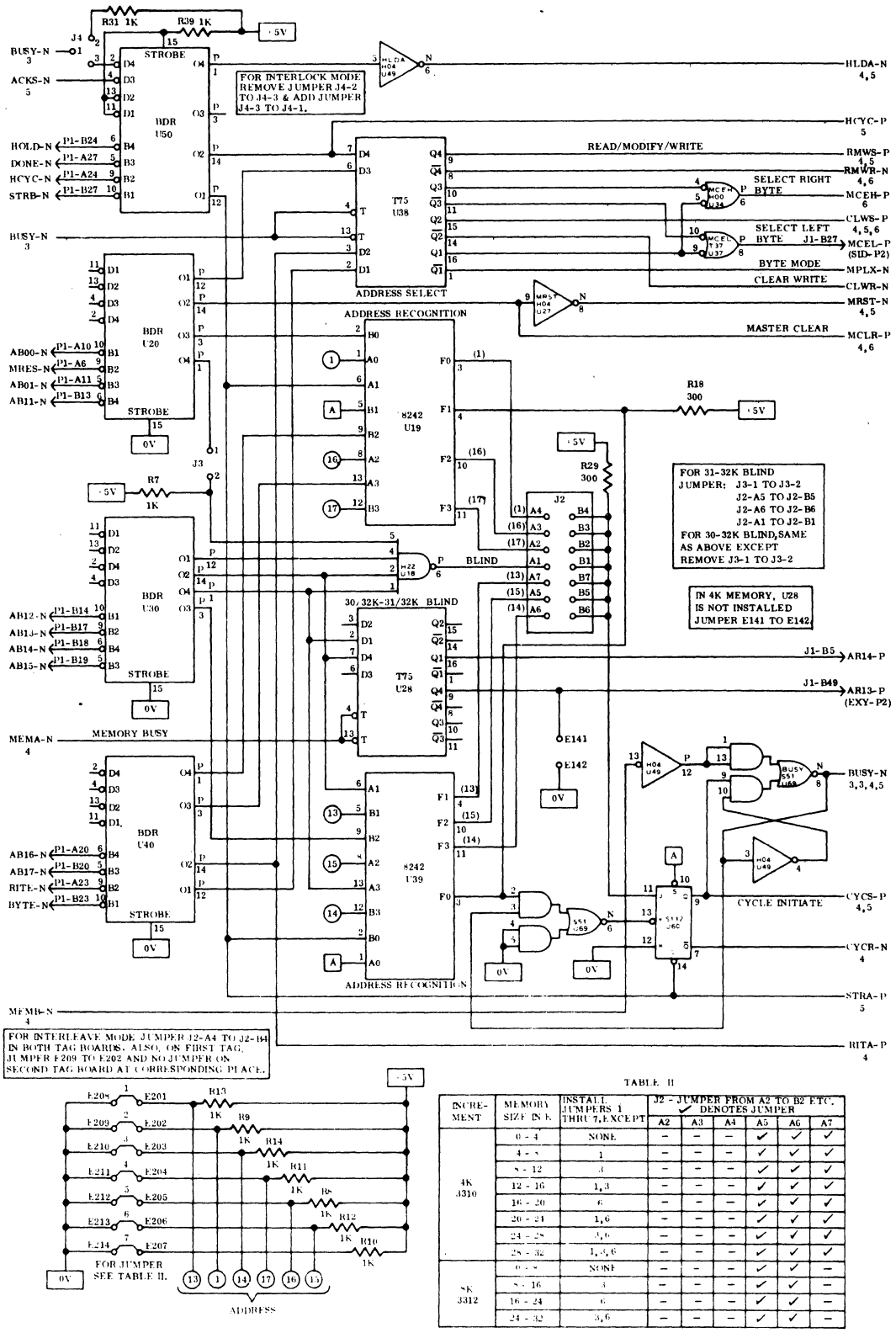
Interlock Mode

The interlock mode inhibits the overlap mode so that a new memory cycle cannot begin in any memory module until the current cycle is completed.

Interlock mode is implemented by removing a jumper from J4-2 to J4-3 and installing a jumper from J4-1 to J4-3 thereby asserting HOLD on the INFIBUS during any memory cycle.

KEY SOURCE LOGIC DEFINITIONS

AB00-N, AB01-N AB11-N thru AB15-N, AB16-N, AB17-N	Address Bit 00 through 17 Input (Negative)
AR13-N, AR14-N	Address Register Output Bit 13 and 14 (Negative)
BUSY-N	Busy Flip-Flop Output (Negative)
CLWS-P, CLWR-N	Clear Write Register Set Output (Positive) Clear Write Register Reset Output (Negative)
CYCS-P, CYCR-N	Cycle Initiate Register Set Output (Positive) Cycle Initiate Register Reset Output (Negative)
HLDA-N	Memory Disable Advanced (Negative)
HCYC-N, HCYC-P	Read Modify Write Command (Negative) Read Modify Write Command (Positive)
MCLR-P, MRST-N	Master Clear Input (Positive) Master Reset of all Control Flip-Flops (Negative)
MCEH-P, MCEL-P	Select Right Byte (Positive) Select Left Byte (Positive)
MPLX-N	Multiplex Order (Negative)
RMWS-P, RMWR-N	Read Modify Write Register Output (Positive) Read Modify Write Register Output (Negative)
STRA-P	Strobe Advanced (Positive)
RITA-P	Rite Command Advanced (Positive)



INCREMENT	MEMORY SIZE IN K	INSTALL JUMPERS 1 THRU 7, EXCEPT	J2 - JUMPER FROM A2 TO B2 ETC. ✓ DENOTES JUMPER					
			A2	A3	A4	A5	A6	A7
4K 3310	0 - 4	NONE	–	–	–	✓	✓	✓
	4 - 8	1	–	–	–	✓	✓	✓
	8 - 12	3	–	–	–	✓	✓	✓
	12 - 16	1,3	–	–	–	✓	✓	✓
	16 - 20	6	–	–	–	✓	✓	✓
	20 - 24	1,6	–	–	–	✓	✓	✓
	24 - 28	3,6	–	–	–	✓	✓	✓
	28 - 32	1,3,6	–	–	–	✓	✓	✓
8K 3312	0 - 8	NONE	–	–	–	✓	✓	–
	8 - 16	3	–	–	–	✓	✓	–
	16 - 24	6	–	–	–	✓	✓	–
	24 - 32	3,6	–	–	–	✓	✓	–

TAG

SUE 3310 Timing and Gating (TAG) Logic Diagram
LD2001002273, Rev. D, Sheet 3 of 6

READ/WRITE OPERATION CONTROL (TAG LD Sheet 4)

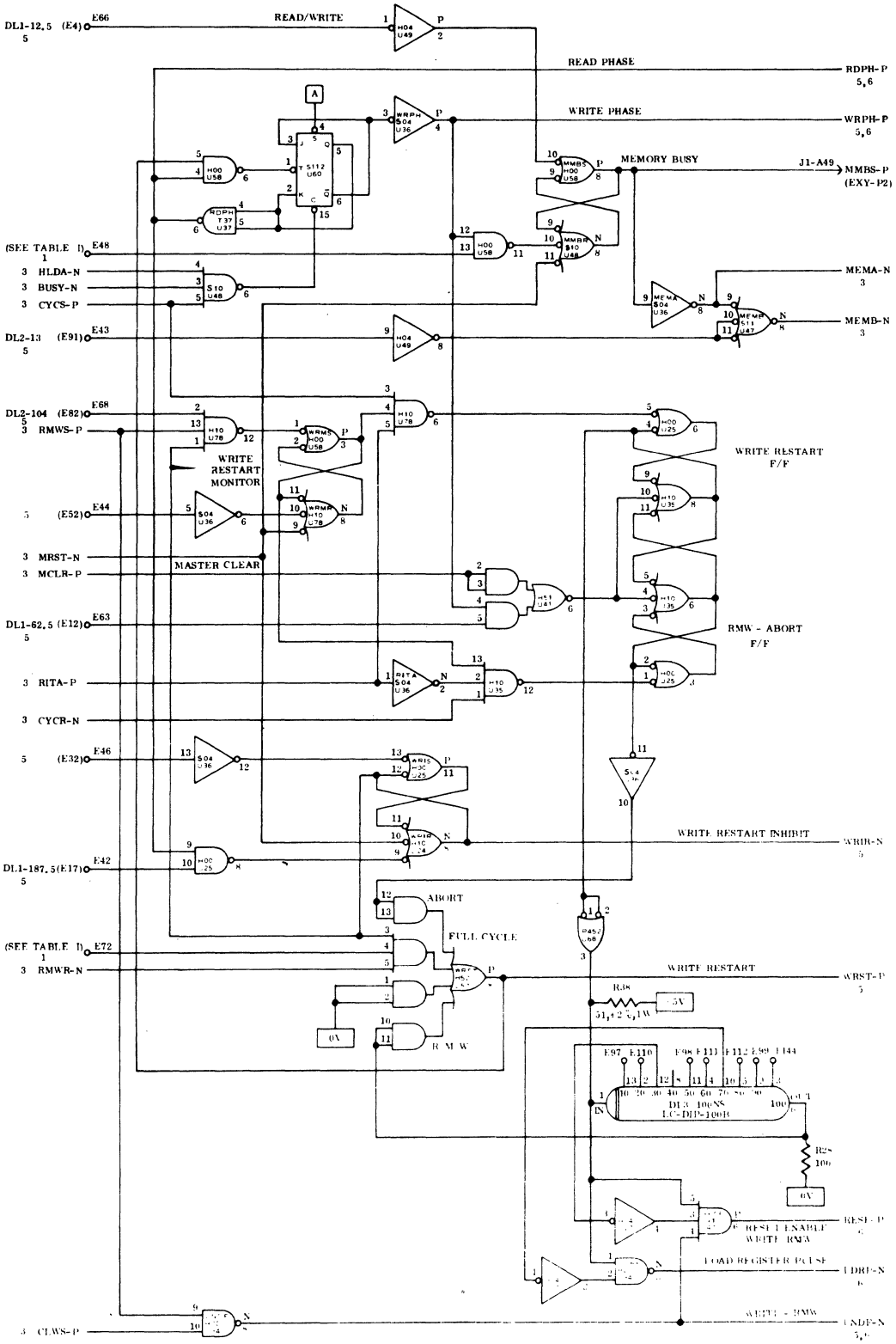
Read/Write flip-flop U60 determines whether a read or write operation is to be performed. When the flip-flop is set, its reset output brings up the Write Phase term, WRPH-P. When the flip-flop is reset, its set output brings up the Read Phase term, RDPH-P. During the write portion of the Clear/Write operation, the U60 Read/Write Phase flip-flop is reset, causing term WRPH-P to go true.

Terms MMBS-P, MEMA-N and MEMB-N, the Memory Busy indicator signals, are generated by the Memory Busy S-R latch.

Term RMWR-N false enables the Write Restart OR gate U57, via the Full Cycle AND gate, to bring up term WRST-P at DL2-130 (E90) time.

KEY SOURCE LOGIC DEFINITIONS

LDRP-N	Load Register Pulse
MEMA-N, MEMB-N, MMBS-P	Memory Busy Status Signals
RDPH-P	Read Phase Term
UNDF-N	Undefined Mode Status Signal
WRIR-N	Write Phase Restart Inhibit
WRPH-P	Write Phase Term
WRST-P	Write Restart Signal



SUE 3310 Timing and Gating (TAG) Logic Diagram
LD2001002273, Rev. D, Sheet 4 of 6

TAG

TIMING CIRCUITS (TAG LD Sheet 5)

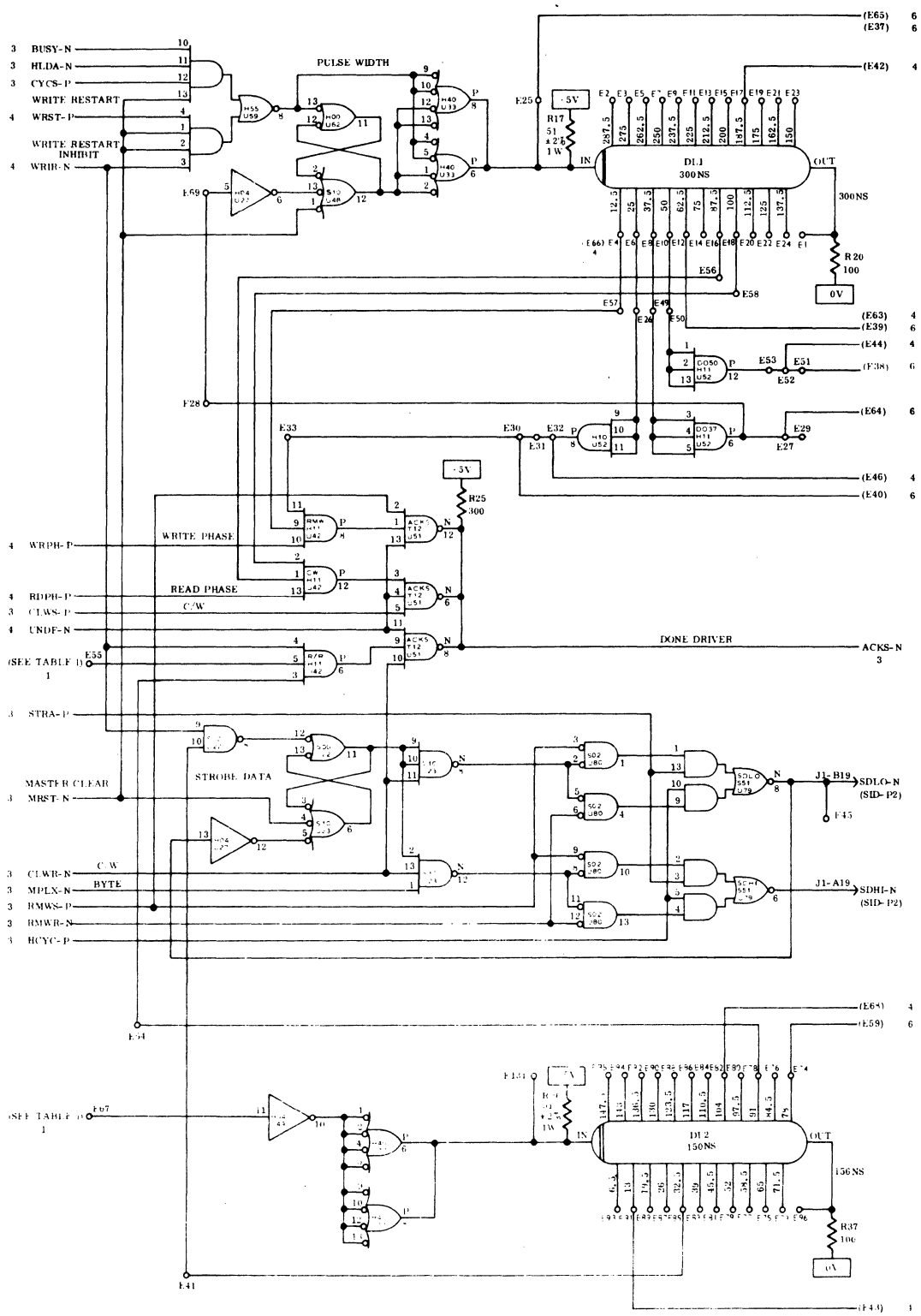
Term CYCS-P passes through delay lines DL1 and DL2. The time signals of the two delay lines are used for the precise timing of the various operational mode control circuits. The above sequence of events occurs twice for every storage cycle.

Term CLWK-N false, enables the U23 AND-gates to bring up the left and right data out strobe terms SDHI-N and SDLO-N. Term RMWR-N false, enables the U59 AND/OR-gate combination to bring up Pulse Width, and starts via OR gate U33, the timing strobe terms of delay lines DL1 and DL2.

The 237.5 nanosecond timing pulse from the DL1 delay line, term DL1-237.5 (E9), starts delay line DL2. The 104 nanosecond timing pulse from the DL2 delay line, term DL2-104 (E82), enables the Full Cycle AND-gate (TAG LD sheet 4) to bring up term WRST-P. Term WRST-P once more brings up the Pulse Width signal, which successively starts delay lines DL1 and DL2. After this second time through the DL1/DL2 timing network however, the timing pulses cease to be generated until another STRB strobe signal is received.

KEY SOURCE LOGIC DEFINITIONS

ACKS-N	Acknowledge Signal
SDHI-N	Data Out Left Byte
SDLO-N	Data Out Right Byte



SUE 3310 Timing and Gating (TAG) Logic Diagram
LD2001002273, Rev. D, Sheet 5 of 6

TAG

DATA TRANSFER CONTROL (TAG LD Sheet 6)

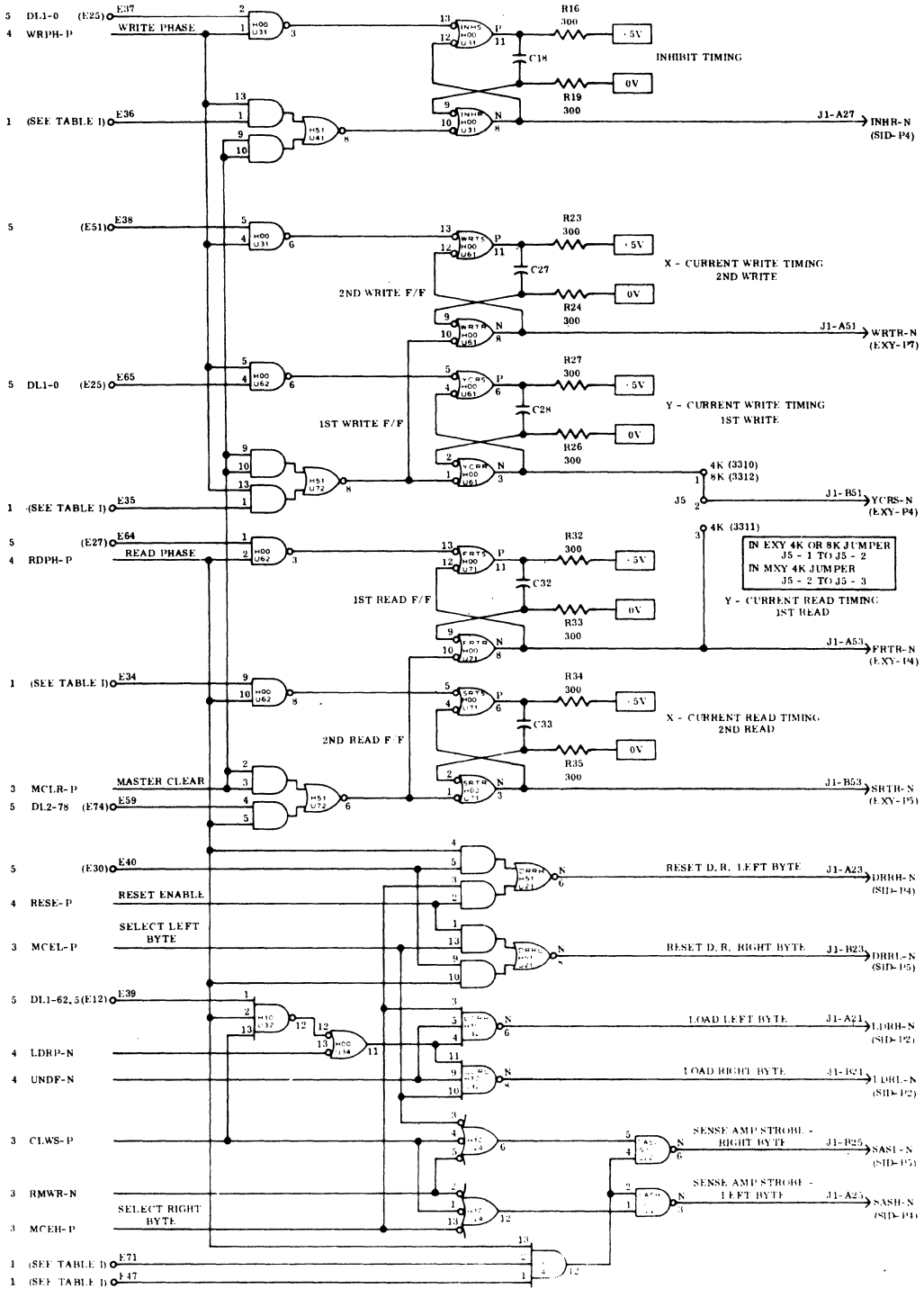
Term CLWR-P negated, enables the U22 AND-gates to bring up the left and right sense amplifier strobe terms SASH-N and SASL-N. The data out and sense amplifier strobe terms are all control signals to the EXY circuits.

Terms MCEH-P and MCEL-P asserted prevent the bringing up of the SASL-N and SASH-N sense amplifier strobe terms. Terms SASL-N and SASH-N would, if activated, enable the sense amplifiers or the SID circuit card.

Term WRPH-P sets the Inhibit Timing latch U31, asserting term INHR-N. At the same time WRPH-P sets the Y-Current Write Timing flip-flop (one half of U61) to assert YCRS-N, and 50 nanoseconds later sets the X-Current flip-flop (the other half of U61) to assert WRTR-N. The WRTR-N signal controls the X-current switches on the EXY circuit card and the YCRS-N signal controls the Y-current switches on the EXY circuit card.

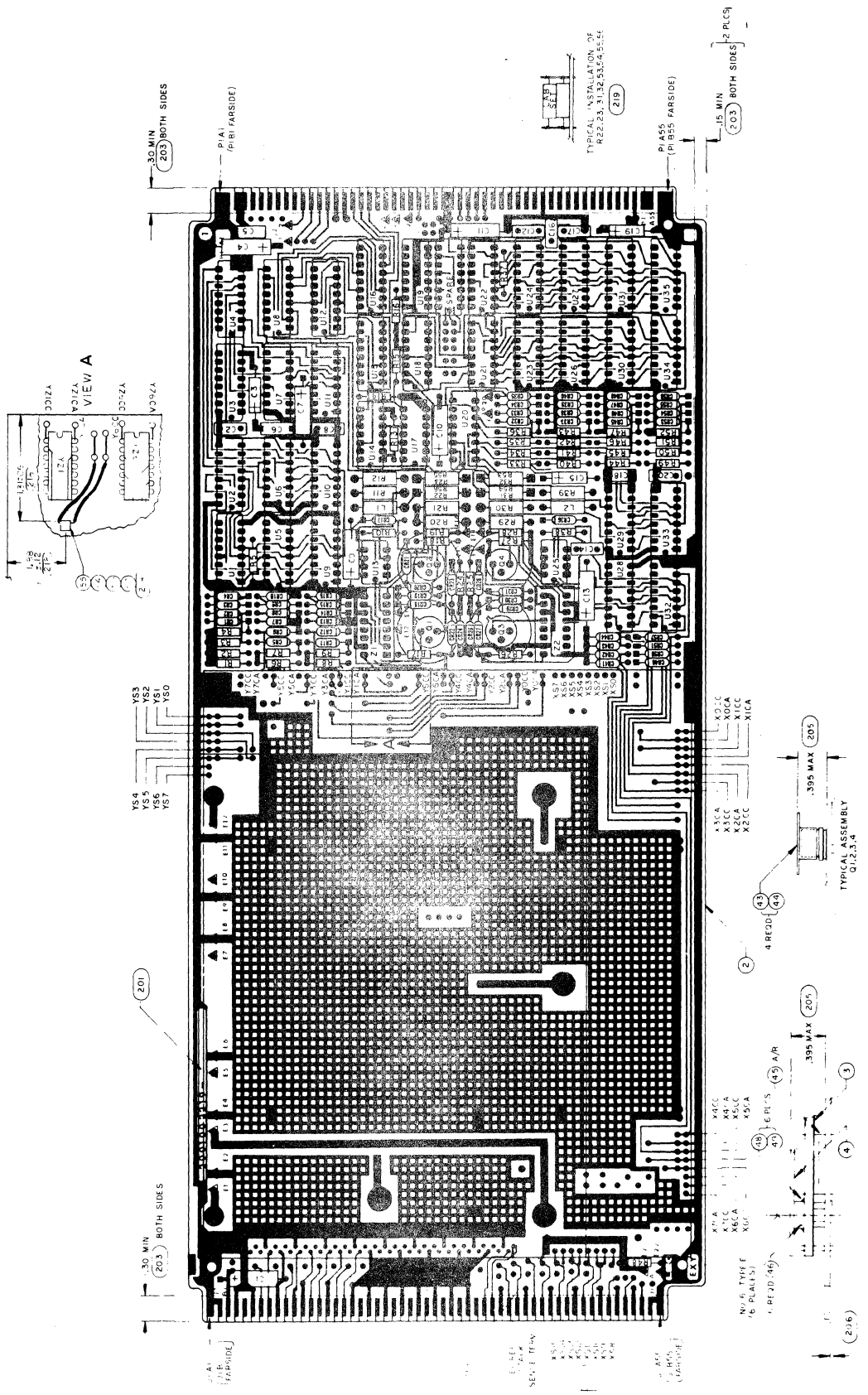
KEY SOURCE LOGIC DEFINITIONS

DRRH-N	Data Register Reset Left Byte Strobe
DRRL-N	Data Register Reset Right Byte Strobe
FRTR-N	First Read Timing Pulse
INHR-N	Inhibit Timing Pulse
LDRH-N	Load Data Register Left Byte
LDRL-N	Load Data Register Right Byte
SASH-N	Sense Amp Strobe Right Byte
SASL-N	Sense Amp Strobe Left Byte
SRTR-N	Second Read Timing Pulse
WRTR-N	Write Timing Pulse
YCRS-N	Y Common Read Only



SUE 3310 Timing and Gating (TAG) Logic Diagram
LD2001002273, Rev. D, Sheet 6 of 6

TAG



SUE 3310 Memory Electronics and XY Matrix (EXY) Circuit Card Assembly
2001002219-2, Rev. C, Sheet 1

NOTES:

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS ARE IN MICROFARADS, ±20%.
4. ALL DIODES ARE 8001100001.
5. ALL TRANSISTORS ARE 8001200016.
6. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED. FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
7. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (8 PIN ICP) PIN 4 0V, PIN 8 +5V; (14 PIN ICP) PIN 7 0V, PIN 14 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR PIN 7 AND 8 0V, PIN 16 +5V, T75 PIN 5 +5V, PIN 12 0V, P325 PIN 8 0V, PIN 9 +5V, PIN 16 +15V.

[8] +5V CONNECTOR PINS ARE: P1-A28, A29, B28, B29.

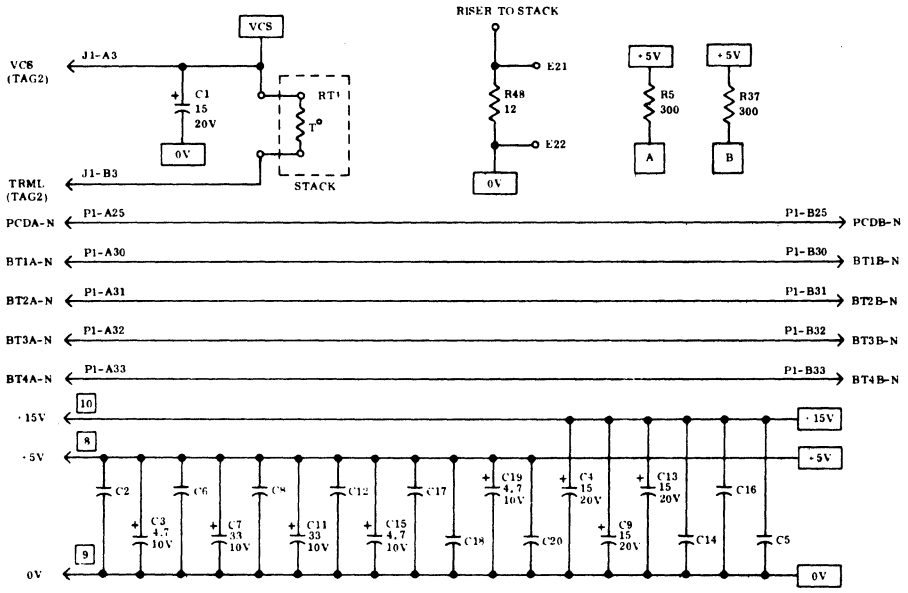
[9] 0V CONNECTOR PINS ARE: P1-A1, A2, A15, A40, A54, A55, B1, B2, B15, B40, B54, B55; J1-A1, A2, A4, A18, A20, A22, A24, A26, A28, A30, A32, A50, A52, A54, A55, B1, B2, B4, B18, B20, B22, B24, B26, B28, B30, B32, B50, B52, B54, B55.

[10] +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4.

[11] R53 IS A TRIM RESISTOR (LAB SET).

[12] R54, R55 AND R56 VALUES MAY BE CHANGED AT TEST LEVEL.

13. ◯ DENOTES COMMON SIGNAL.



TAG

SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 1 of 10

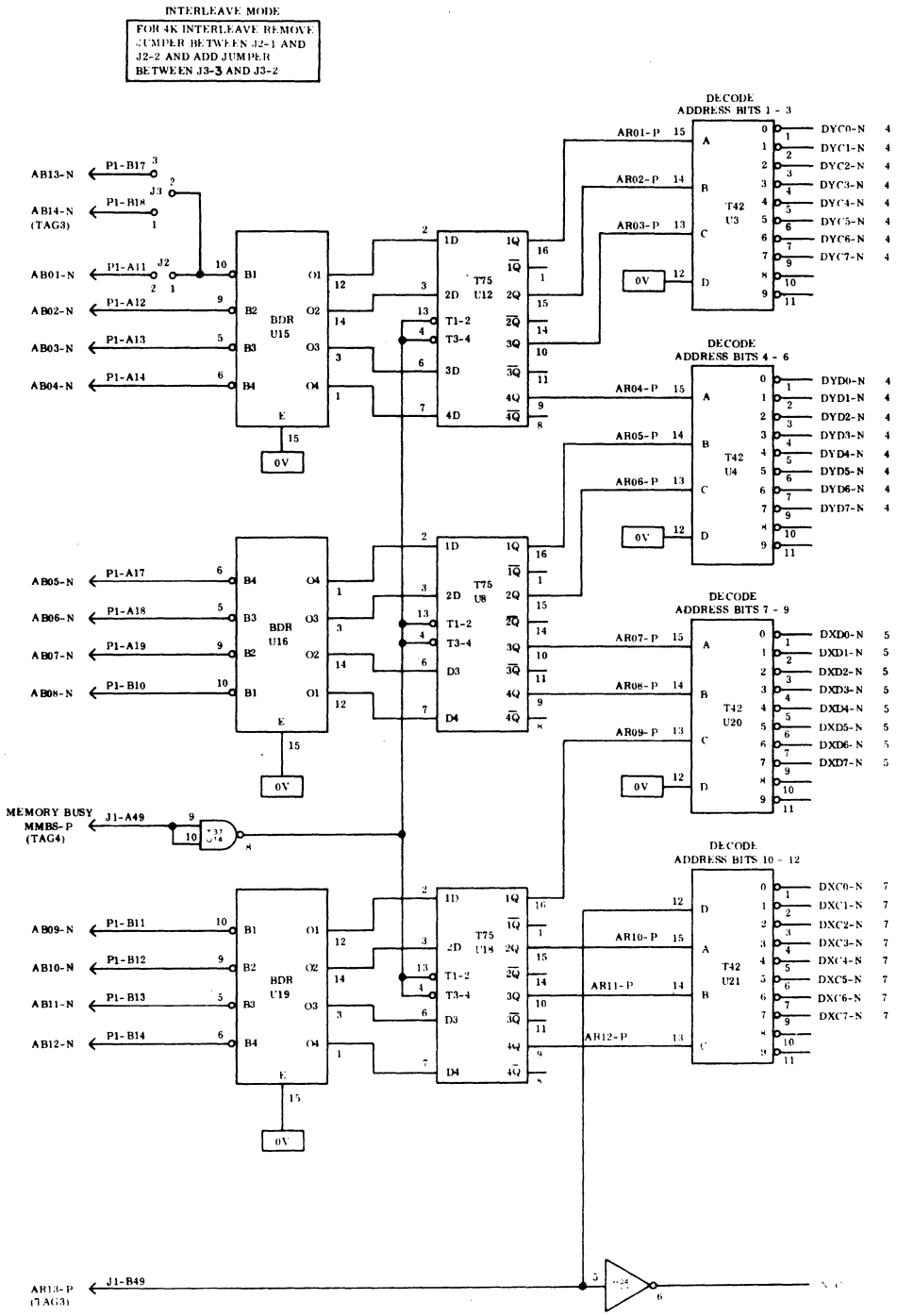
ADDRESS RECEIVERS AND X-Y LINE DECODING (EXY LD Sheet 2)

Memory address bits AB01-N through AB12-N are decoded by this logic to select the X-Y common and diode end drive lines. The address bits are received from the INFIBUS in sets of four by receiver/driver integrated circuit logic U15, U16, and U19 respectively. The receiver/driver logic inverts the memory address bits that then set or reset corresponding flip-flops in the U12, U8, and U18 (if not inhibited by memory busy MMBS-P). The flip-flops hold the memory address received from the INFIBUS until memory busy MMBS-P releases them to accept a new set of address bits from the receiver/driver logic. It is also the function of the flip-flop logic in U12, U8, and U18 to act as hexadecimal to octal converter logic (i.e. four memory address bits are converted to three address register bits). Each set of three address register bits is decoded by U3, U4, U20 and U21 to select one of eight Y-common end lines (DYC0-N through DYC7-N), Y-diode end lines (DYD0-N through DYD7-N), X-diode end lines (DXD0-N through DXD7-N), and X-common end lines (DXC0-N through DXC7-N). Each of the address decode logic integrated circuits U3, U4, U20, and U21 perform an octal to decimal conversion to select one of eight lines from three binary address bits.

The address decode circuits U3, U4, and U20 are always enabled (pin D held at 0 volts). U21 is controlled by address register bit AR13-P from the TAG circuit card that is held at 0 volts by a jumper between E141 and E142 so that U21 is enabled allowing AR10-P through AR12-P to be decoded into one of the X-common diode lines DXC0-N through DXC7-N.

KEY SOURCE LOGIC DEFINITIONS

AR01-P thru AR12-P	Memory Address register bits 01 through 12 (Positive)
DXC0-N thru DXC7-N	Decoded Line 0 through 7 for X Common end (Negative)
DXD0-N thru DXD7-N	Decoded Line 0 through 7 for X Diode end (Negative)
DYC0-N thru DYC7-N	Decoded Line 0 through 7 for Y Common end (Negative)
DYD0-N thru DYD7-N	Decoded Line 0 through 7 for Y Diode end (Negative)



SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 2 of 10

TAG

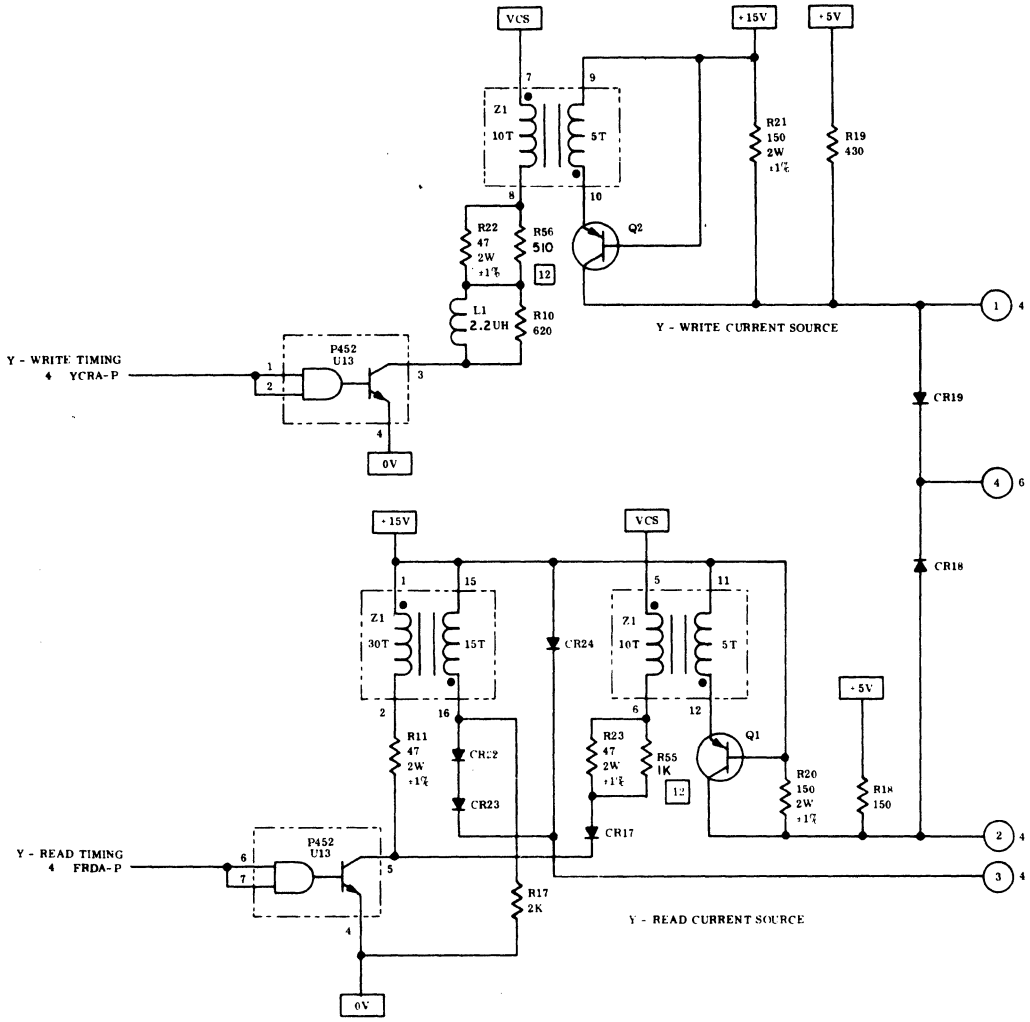
Y-READ AND WRITE CURRENT SOURCE (EXY LD Sheet 3)

At the same time that memory address decoding is performed the proper Y-read or write current source is enabled by either YCRA-P or FRDA-P into current source enabling gates in U13. The selected U13 gate draws current through the primary of the 2 to 1 ratio (10 turn to 5 turn) transformer from VCS which drives twice the current in the secondary through the current source transistor Q1 or Q2. The resultant current flow through the current source transistor is approximately 350 milliamperes. The 150-ohm pull-up resistor (R20 or R21) to +15 volts supplies another 70 milliamperes of drive current and also assures 15 volts (for the Y-write current source) can be maintained as the driving voltage regardless of the value of VCS. The current source transistor collector is a high impedance drive source that minimizes the affect of slight impedance variations among the 64 Y-drive lines.

The second 2 to 1 ratio (30 turn to 15 turn) transformer and its associated logic in the Y-read current source circuitry adds a 5-volt pulse to the 15 volts DC source voltage for the switching logic (EXY LD sheet 4). This momentary increase in the source voltage provides faster switching of the read current source to the drive lines shortening the read cycle time.

The purpose of the 430 ohm (R19) in the Y-write current source and 68 ohm (R18) in the Y-read current source circuits is to provide damping of the source current to remove some of the inherent ringing at initial turn-on of the current source drivers. The Y-write current source circuit tends to be slightly more linear and therefore requires less damping (i.e. the 430 ohm rather than 68 ohm resistor).

The collectors of the current source transistors Q1 and Q2 through CR18 and CR19 respectively are clamped to approximately 1-1/2 volts below the +15 volt DC sources to avoid saturation. The 1-1/2 volt drop is across CR20, CR21, and CR31 located in the X-read and write current source circuitry (EXY LD sheet 6).



TAG

SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 3 of 10

Y-CURRENT DRIVE SWITCHING (EXY LD Sheet 4)

Common End Line Switching

After memory address bits AB01-N through AB04-N are decoded to select one Y-drive common end line DYC0-N through DYC7-N (EXY LD sheet 2) the asserted line enables either the read or write memory drive switching gate in IC U1, U2, U5 or U9. Selection of the read or write gate is controlled by Y-write timing pulse YCRS-N and Y-read timing pulse FRTR-N both originating on the TAG circuit card. When the read or write memory drive switching gate is enabled, it turns on one memory drive transistor within that IC thereby connecting Y-read or write current source circuit to the Y-matrix common end line YDC0 through YDC7 associated with the selected current drive switching logic. There are two current flow paths associated with each Y drive common end line DYC0-N through DYC7-N (one for read cycle and one for write cycle). Current flow is discussed under a separate paragraph in this logic description.

Diode End Line Switching

After memory address bits AB05-N through AB08-N are decoded to select one Y-drive diode end line DYD0-N through DYD7-N (EXY LD sheet 2) the asserted line enables either the read or write memory drive switching gate in IN U6, U7, U10, or U11. Selection of the read or write gate is controlled by Y-write timing pulse YCRS-N and Y-read timing pulse FRTR-N both originating on the TAG circuit card. When the read or write memory drive switching gate is enabled, it turns on one memory drive transistor within that IC thereby connecting to the Y-matrix diode end line YDD0 through YDD7 or YDR0 through YDR7 associated with the selected current drive switching logic. As with the Y-drive common end lines DCY0-N through DYC7-N, there are two current flow paths associated with the Y-drive diode end lines.

Current Flow for Y-Drive Lines

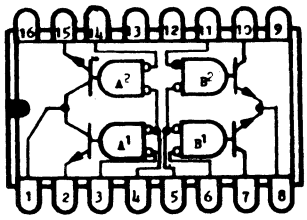
For this discussion, reference the drawing of a P325 IC, EXY LD sheets 4 and 8 and assume a read cycle followed by a unite cycle where memory address decoding logic bus selected DYD4-N and DYC2-N diode and common end lines respectively.

Y-read timing pulse FRTR-N with DYD4-N and DYC2-N respectively enables U10 memory drive switching gate A^1 and U9 memory drive switching gate B^1. This causes current to flow from the Y-read current source circuit into pin 1 of U10, through the A^1 memory drive transistor to pin 2 and out through the Y-diode end line YDD4. Current flows through the cores associated with Y-matrix line Y36 to YDC2 where it enters U9 at pin 7 and passes through the B^1 memory drive transistor to pin 8 ground thus completing the circuit.

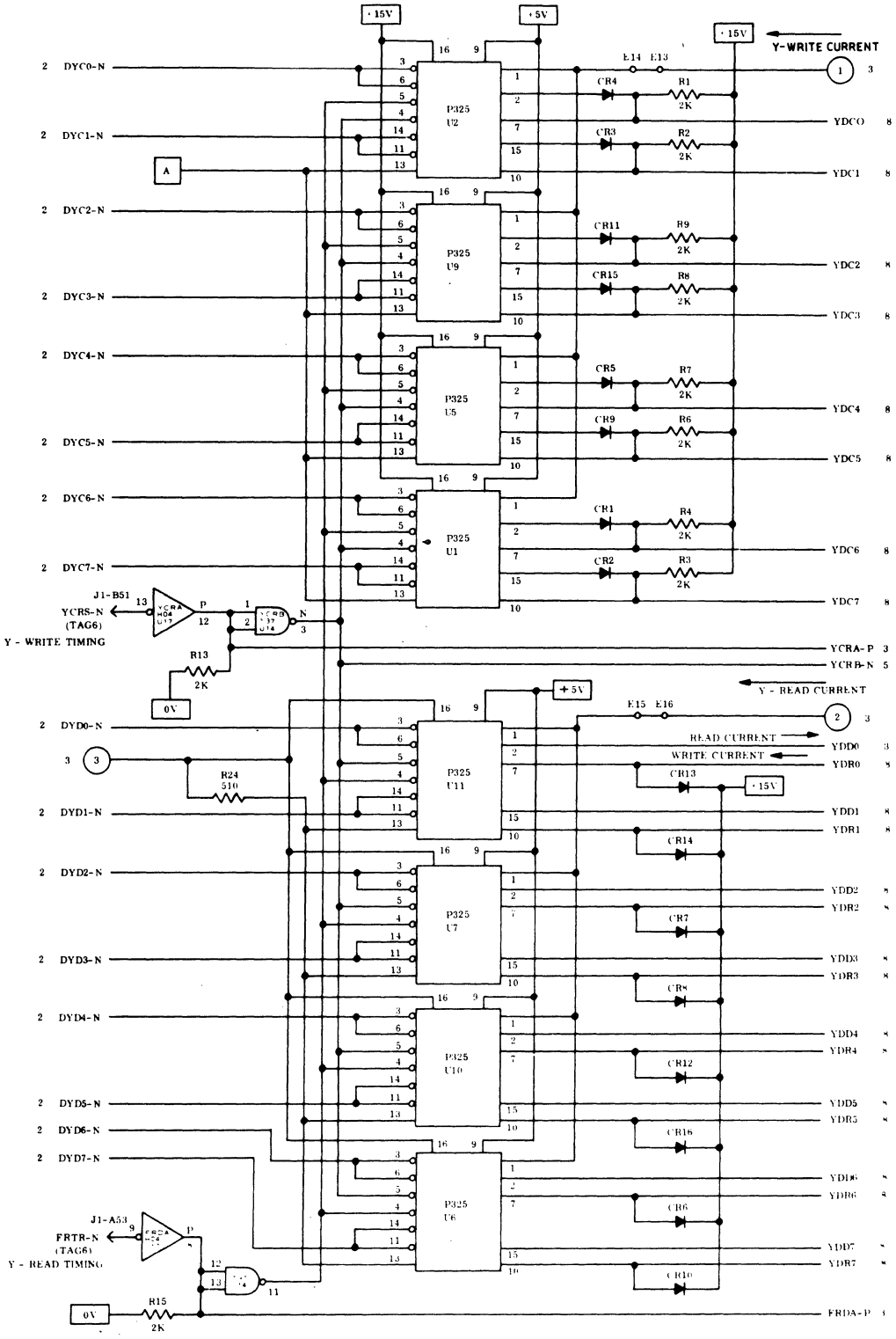
When Y-write timing pulse YCRS-N is asserted (DYD4-N and DYC2-N asserted also) U9 memory drive switching gate A^1 and U10 memory drive switching gate B^1 are enabled. This causes current to flow from the Y-write current source circuit into pin 1 of U9, through the A^1 memory drive transistor to pin 2 and through blocking diode CR11 to the YDC2 common line. Current flows through Y-matrix line Y36 and associated cores to YDR4 (the diode end return line) to pin 7 of U10 through the B^1 memory drive transistor to ground to complete the circuit. The current flow path for a write cycle is simply the reverse of that for a read cycle.

KEY SOURCE LOGIC DEFINITIONS

FRDA-P	First Read Timing Inverted (Positive)
YCRA-P	First Write Timing Inverted (Positive)
YCRB-N	First Write Timing Buffered (Negative)
YDC0 thru YDC7	Y common-end Line 0 through 7
YDD0 thru YDD7	Y Diode and Drive Line 0 through 7
YDR1 thru YDR7	Y diode end Received Line 0 through 7



P325 Integrated Circuit-Memory Drivers



SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 4 of 10

TAG

X-CURRENT DRIVE SWITCHING (EXY LD Sheet 5)

Diode-End Line Switching

After memory address bits AB05-N through AB08-N and AB09-N are decoded to select one X-drive diode end line DXD0-N through DXD7-N (EXY LD sheet 2) the asserted line enables either the read or write memory drive switching gate in IC U28, U29, U32, or U33. Selection of the read or write gate is controlled by X-write timing pulse YCRB-N and X-read timing pulse SRTR-N (delayed second pulse) both originating on the TAG circuit card. When the read or write memory drive switching gate is enabled, it turns on one memory drive transistor within that IC thereby connecting the X-read or write current source circuit to the X-matrix diode end line XDD0 through XDD7 or XDRD through XDR7 associated with the selected current drive switching logic. There are two current flow paths associated with the X-drive diode end lines, one for read and one for write.

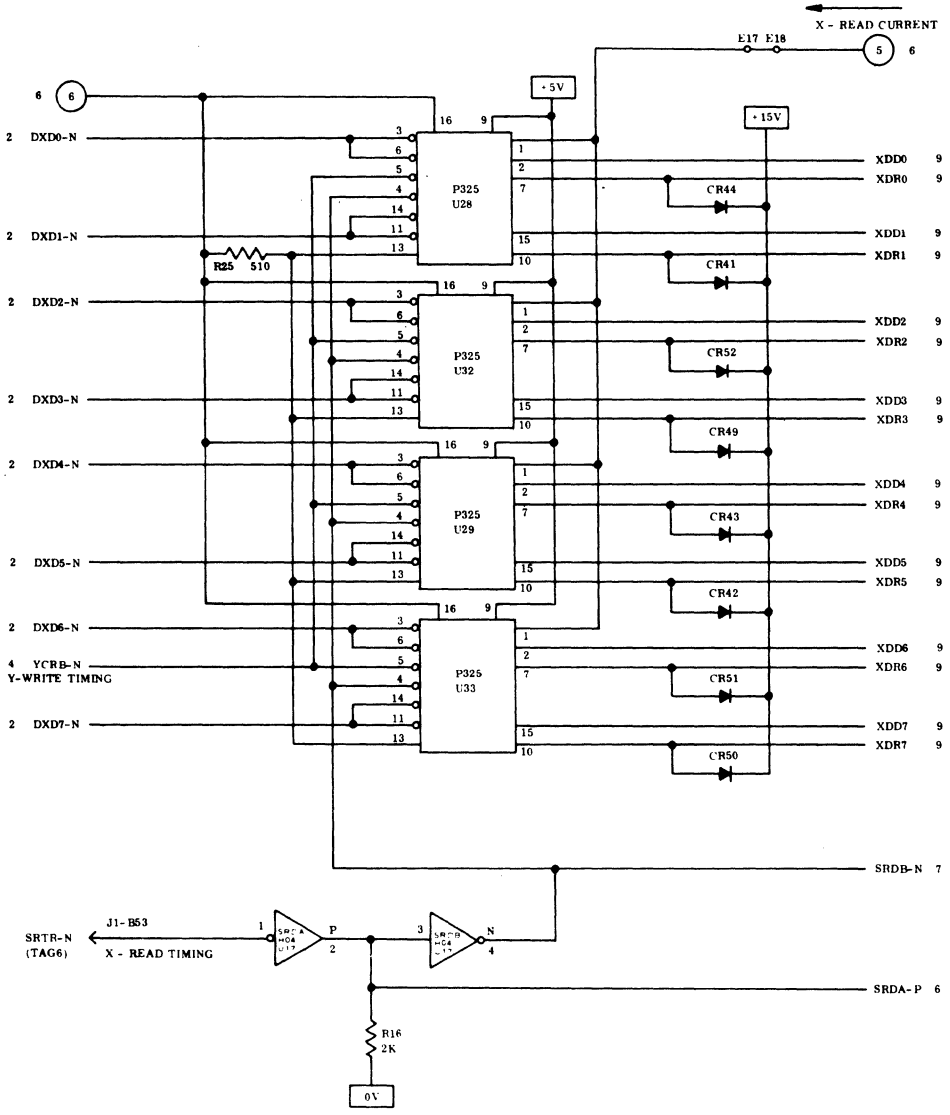
The read timing pulse is delayed (approximately 100 nanoseconds after assertion of Y-timing pulse) to assure the Y-read or write current source has settled down and there are no spurious spikes that could cross-talk with X-drive lines during core selection to address an unaddressed core. It also minimizes the initial load and resulting current surge that would be placed on VCS if both X and Y current source circuits were enabled simultaneously.

Current Flow for X-Drive Logic

Current flow for X-drive lines is discussed after the X-common line switching logic description for EXY LD sheet 7.

KEY SOURCE LOGIC DEFINITIONS

SRDA-P	Second Read Timing Inverted (Positive)
SRDB-N	Second Read Timing Buffered (Negative)
XDD0 thru XDD7	X Diode-end Drive Line 0 through 7
XDR0 thru XDR1	X Diode-end Receive Line 0 through 7



SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 5 of 10

TAG

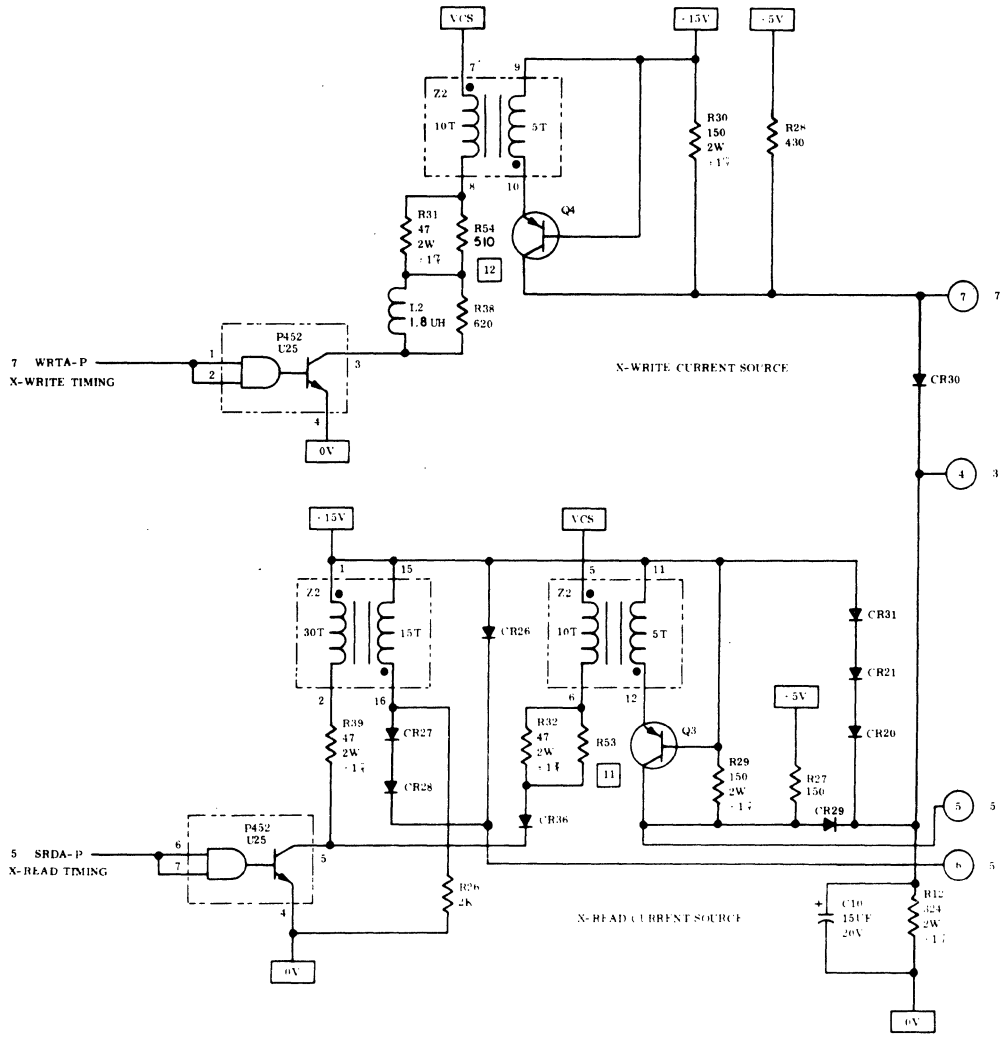
X-READ AND WRITE CURRENT SOURCE (EXY LD Sheet 6)

The X-read current source circuitry is turned on approximately 110 nanoseconds after the Y-read current source and drive line decoding logic by SRDA-P. The X-write current source circuitry is turned on by the second write timing pulse WRTA-P approximately 50 nanoseconds after the Y-write current source, X- and Y-diode end drivers, and Y-common end driver logic. This delay in both X-current source circuitry allows the direct inductance from the Y drive lines into sense lines to decay before the X current source appears to select specific cores in memory. The selected U25 current source enabling gate draws current through the primary of the 2 to 1 ratio (10 turn to 5 turn) transformer from VCS which drives twice the current in the secondary through the current source transistor Q3 or Q4. The resultant current flow through the current source transistor is approximately 350 milliamperes. The 150-ohm pull-up resistor (R29 or R30) to +15 volts supplies another 70 milliamperes of drive current and also assures 15 volts (for the X-write current source) can be maintained as the driving voltage regardless of the value of the VCS. The current source transistor collector is a high impedance drive source that minimizes the affect of slight impedance variations among the 64 X-drive lines.

The second 2 to 1 ratio (30 turn to 15 turn) transformer and its associated logic in the X-read current source circuitry adds a 5-volt pulse to the 15 volts DC source voltage for the switching logic (EXY LD sheets 5 and 7). This momentary increase in the source voltage provides faster switching of the read current source to the drive lines shortening the read cycle time.

The purpose of the 430 ohm resistor (R28) in the X-write current source and 150 ohm resistor (R27) in the X-read current source circuits is to provide damping of the source current to remove some of the inherent ringing at initial turn-on of the current source drivers. The X-write current source circuit tends to be slightly more linear and therefore requires less damping (i.e. the 430 ohm rather than 150 ohm resistor).

The collectors of the current source transistors Q3 and Q4 through CR29 and CR30 respectively are clamped to approximately 1-1/2 volts below the +15 volt DC sources to avoid saturation. The 1-1/2 volts drop is across CR20, CR21, and CR31 that provide clamping for both the X and Y current source circuitry.



SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 6 of 10

TAG

X-CURRENT DRIVE SWITCHING (EXY LD Sheet 7)

Common End Line Switching

After memory address bits AB09-N through AB12-N are decoded to select one X-drive common end line DXC0-N through DXC7-N (EXY LD sheet 2), the asserted line enables either the read or write memory drive switching gate in IC U26, U23, U30, and U34. Selection of the read or write gate is controlled by X-write timing pulse WRTR-N (delayed second pulse) and X-read timing pulse SRDB-N (delayed second pulse) both originating on the TAG circuit card. When the read or write memory drive switching gate is enabled, it turns on one memory drive transistor within that IC thereby connecting the X-read or write current source circuit to the X-matrix common end line XDC0 through XDC7 associated with the selected current drive switching logic. There are two current flow paths associated with each X-drive common end line DXC0-N through DXC7-N (one for read cycle and one for write cycle). Current flow is discussed under a separate paragraph in this logic description.

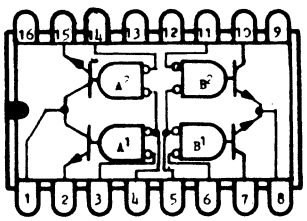
The read and write timing pulses are delayed (approximately 100 nanoseconds after assertion of Y-timing pulse) to assure the Y-read or write current source has settled down and there are no spurious spikes that could cross-talk with X-drive lines during core selection to address an unaddressed core. It also minimizes the initial load and resulting current surge that would be placed on VCS if both X and Y current source circuites were enabled simultaneously.

Current Flow for X-Drive Lines

For this discussion, reference the drawing of a P325 IC, EXY LD sheets 5, 7, and 9 and assume a read cycle followed by a write cycle where memory address decoding logic has selected DXD4-N and DXC2-N diode and common end lines respectively.

X-read timing pulses SRTR-N and SRDB-N with DXD4-N and DXC2-N respectively enables U 29 memory drive switching gate A^1 and U23 memory drive switching gate B^1. This causes current to flow from the X-read current source circuit into pin 1 of U29, through the A^1 memory drive transistor to pin 2 and out through the X-diode end line XDD4. Current flows through the cores associated with X-matrix line X66 to XDC2 where it enters U23 at pin 7 and passes through the B^1 memory drive transistor to pin 8 ground thus completing the circuit.

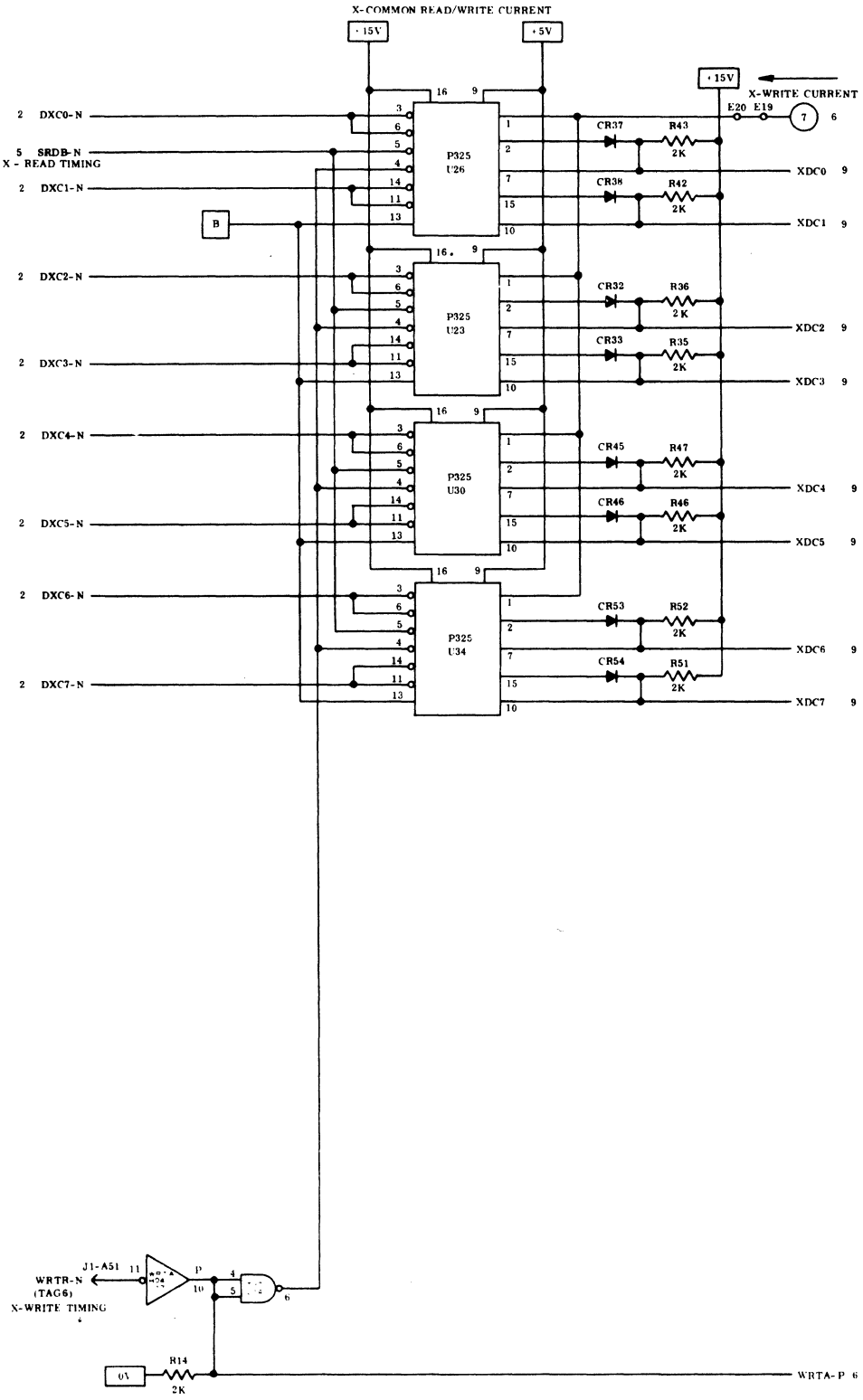
When X-write timing pulses YCRB-N and WRTR-N are asserted (DXD4-N and DXC2-N asserted also) U23 memory drive switching gate A^1 and U29 memory drive switching gate B^1 are enabled. This causes current to flow from the X-write current source circuit into pin 1 of U23 through the A^1 memory drive transistor to pin 2 and through blocking diode CR32 to the XDC2 common line. Current flows through the X-matrix line X66 and associated cores to XDR4 (the diode end return line) to pin 7 of U29 through the B^1 memory drive transistor to ground to complete the circuit. The current flow path for a write cycle is simply the reverse of that for a read cycle.



P325 Integrated Circuit-Memory Drivers

KEY SOURCE LOGIC DEFINITIONS

WRTA-P	Second Write Timing Inverted (Positive)
XDC0 thru XDC7	X Common End Line 0 through F

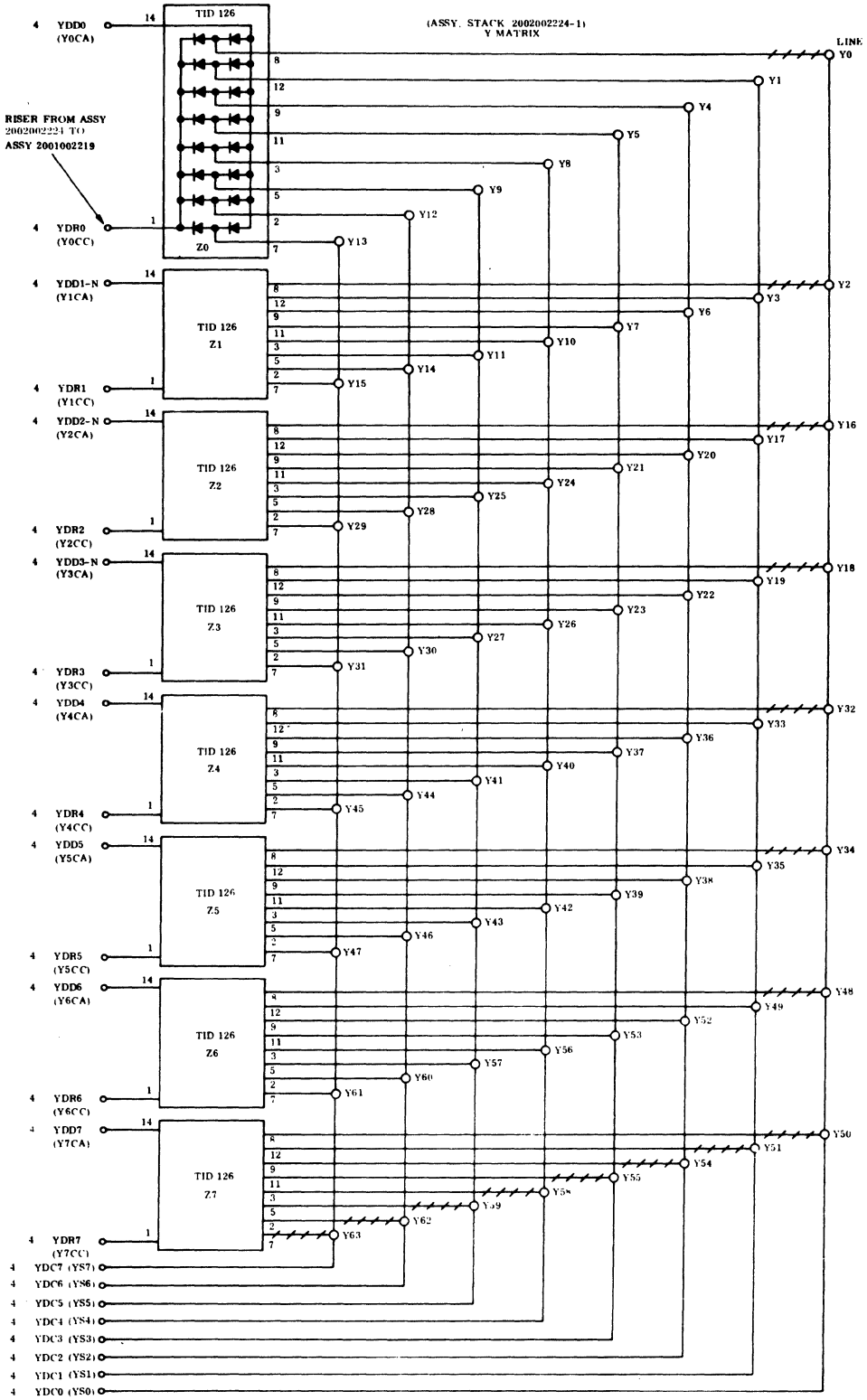


SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 7 of 10

TAG

Y-MATRIX DRIVE LINES (EXY LD Sheet 8)

The Y matrix consists of 8 diode array integrated circuits each driving 8 lines for a total of 64 Y-drive lines. Y-current drives lines YDD0 through YDD7 each drive a diode array IC (i.e. 8 Y-drive lines). The Y-common read/write logic (EXY LD sheet 4) selects one common line YDC0 through YDC8 of the 8 selected Y-drive lines so that during a read/write cycle one Y-drive line in each memory mat is selected for one unique core memory address.

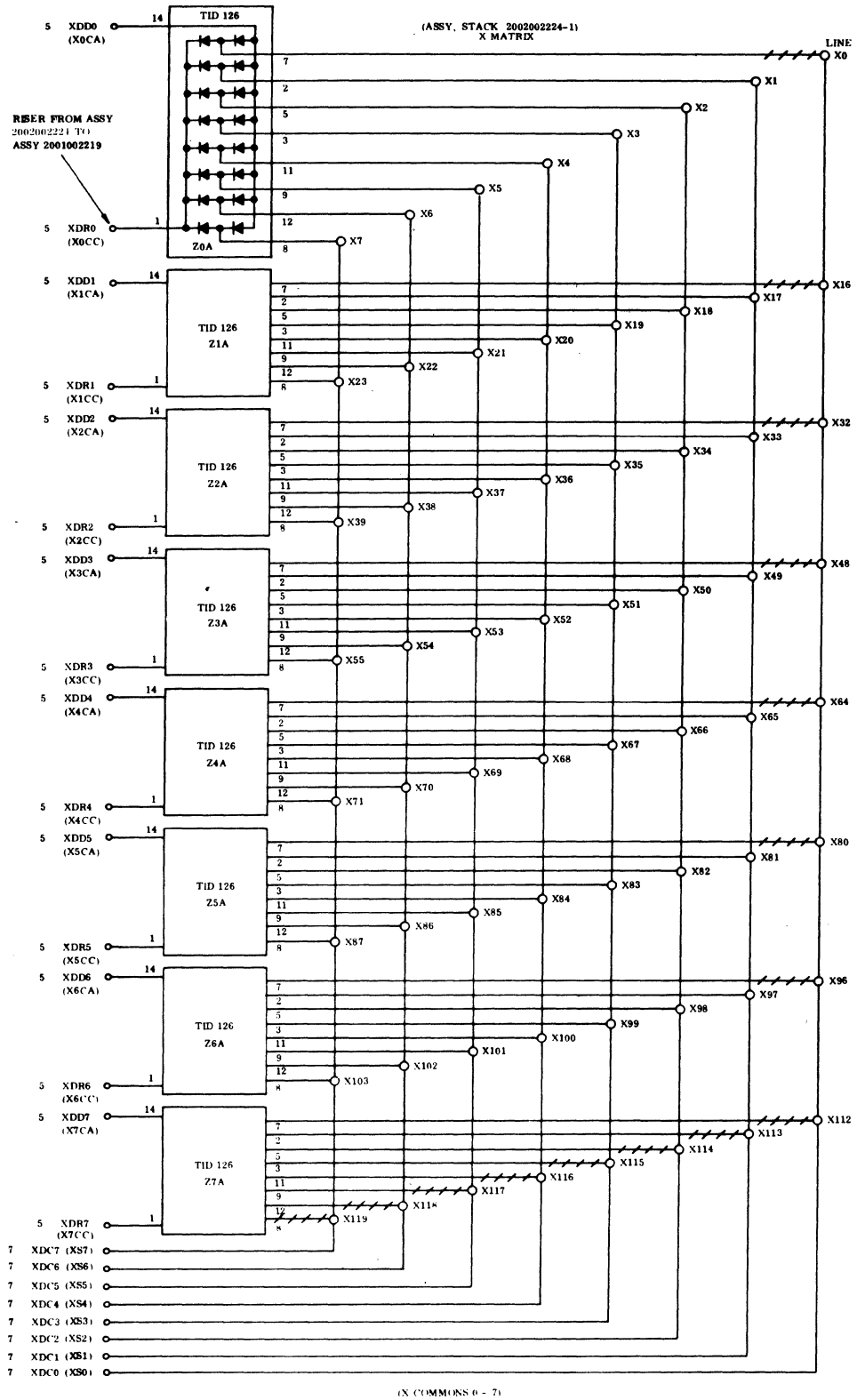


SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 8 of 10

TAG

X-MATRIX DRIVE LINES (EXY LD Sheet 9)

The X matrix consists of 8 diode array integrated circuits each driving 8 lines for a total of 64 X-drive lines. X-current drive lines XDD0 through XDD7 each drive a diode array IC (i.e. 8 X-drive lines). The X-common read/write logic (EXY LD sheet 7) selects one common line XDC0 through XDC7 of the 8 selected X-drive lines so that during a read/write cycle one X-drive line in each memory mat is selected for one unique core memory address.



SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 9 of 10

TAG

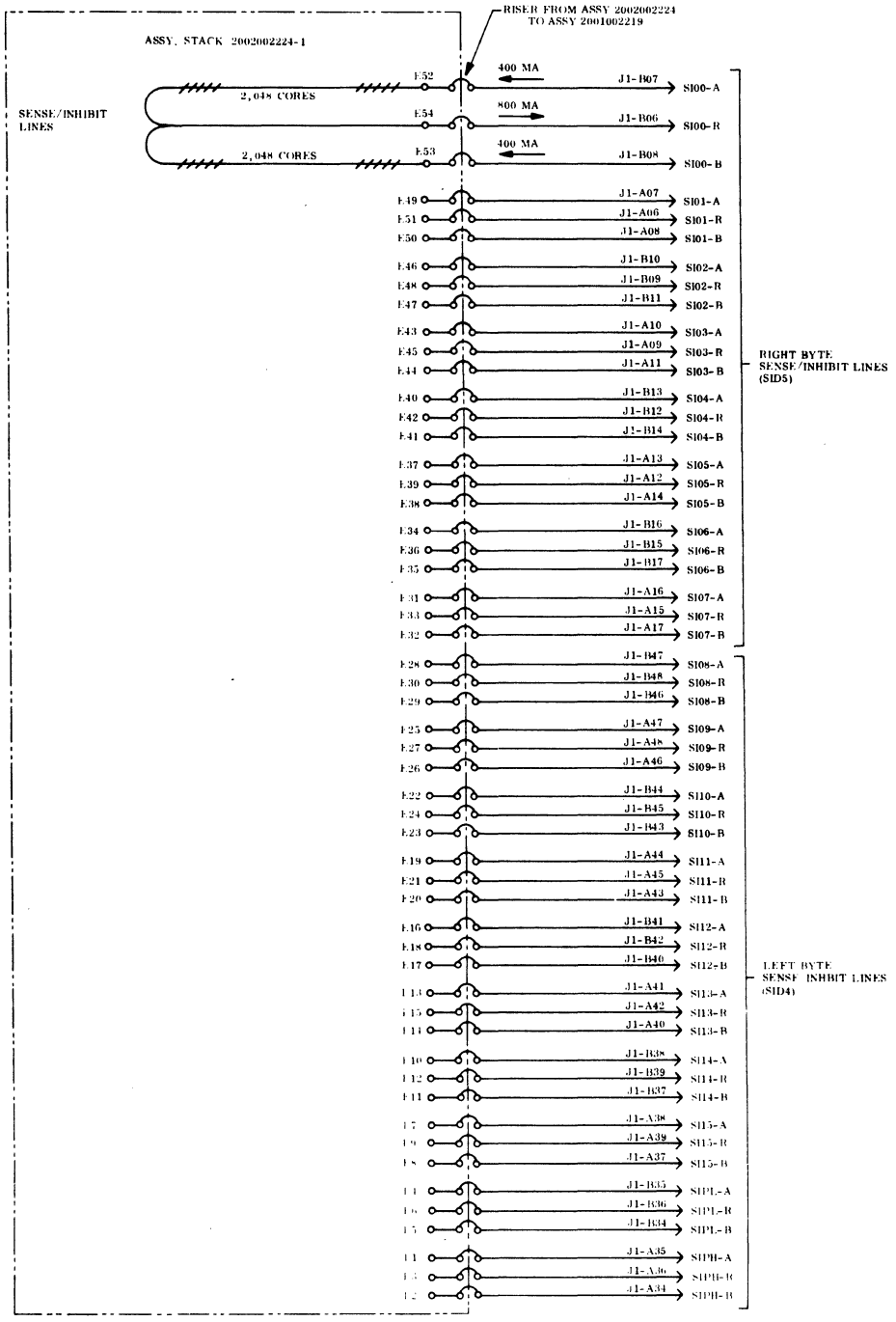
SENSE/INHIBIT LINES (EXY LD Sheet 10)

Each mat of core memory has two sense lines serially connected to form one sense that passes through each of the 4096 ferrite cores. When a core in each mat is driven to a "ZERO" during a read cycle the sense line for that mat detects an electrical impulse if the core is driven from a "ONE" state to a "ZERO" state. This induced voltage is sent to the sense amplifier where it is amplified and strobed to the data register.

The inhibit current during a write cycle can flow from both ends of the sense lines (e.g. SI00-A and SI00-B) when inhibiting driving a core to the "ONE" state if that core was in the "ZERO" state during the read cycle. The center line (e.g. SI00-R) of the sense lines are brought out for inhibit current return.

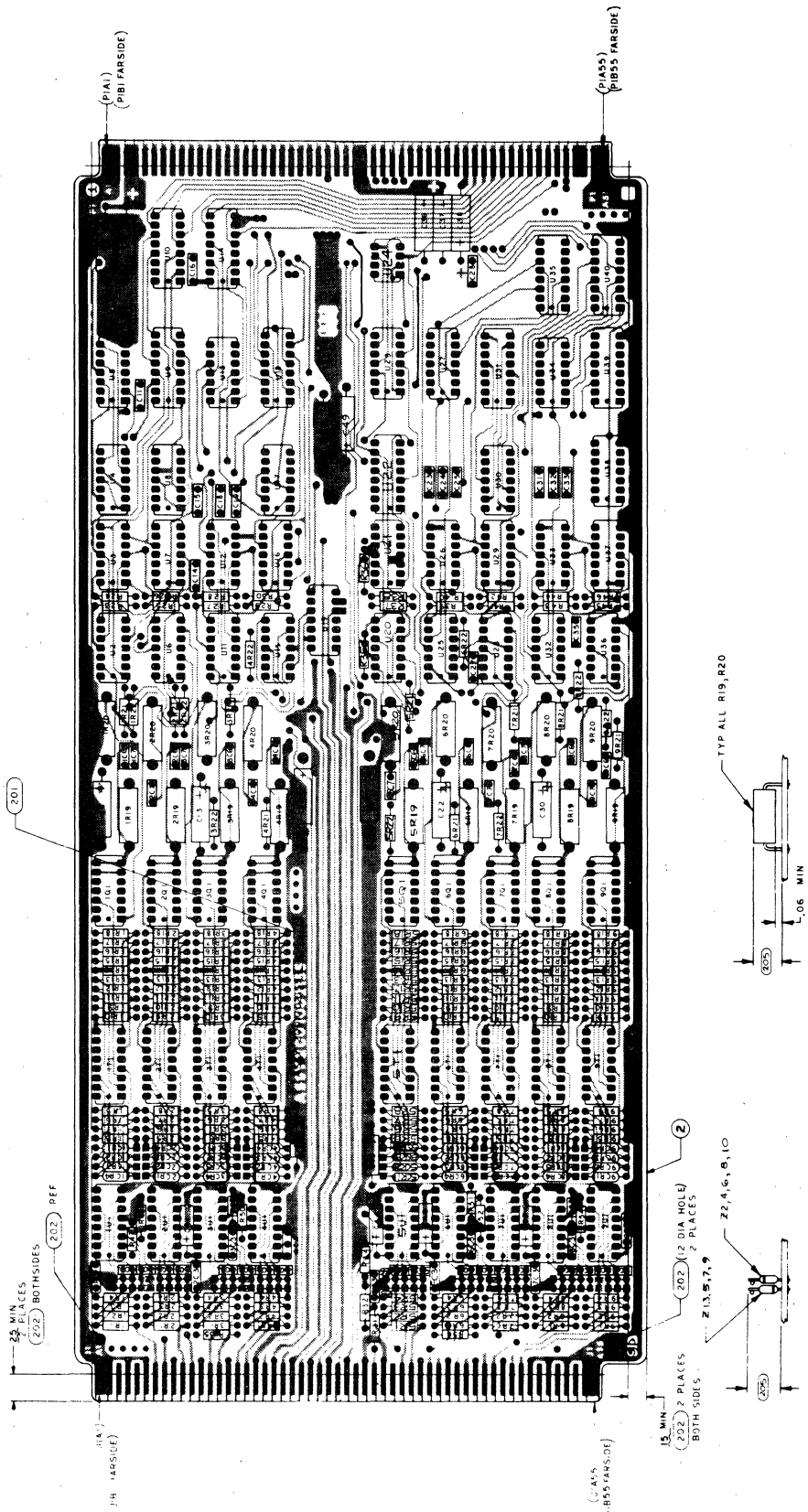
KEY SOURCE LOGIC DEFINITIONS

SI00-A thru SI15-A	Sense Inhibit A, 00 through 15
SI00-B thru SI15-B	Sense Inhibit B, 00 through 15
SI00-R thru SI15-R	Sense Inhibit Return, 00 through 15
SIPH-A, SIPH-B, SIPH-R	Sense Inhibit Parity High (A, B and Return)
SIPL-A, SIPL-B, SIPL-R	Sense Inhibit Parity Low (A, B and Return)



SUE 3310 Memory Electronics and XY Matrix (EXY) Logic Diagram
LD2001002219-2, Rev. B, Sheet 10 of 10

TAG



SUE 3310 Sense, Inhibit Data (SID) Circuit Card Assembly
2001002155, Rev. F, Sheet 1

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL NON-POLARIZED CAPACITORS ARE 0.1UF, +80%, -20%, 50V.
3. ALL POLARIZED CAPACITORS FOR +5V, -5VA, -5VB ARE 4.7UF, ±20%, 10V.
4. ALL POLARIZED CAPACITORS FOR +15V ARE 15UF, ±20%, 20V.
5. ALL DIODES ARE 8001100001.
6. ALL TRANSFORMERS ARE 8001400051.
7. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED, FOR COMPLETE PART NUMBER SEE PARTS LIST. (REFERENCE LIST ON DRAWING 8001800200.)
8. INTEGRATED CIRCUIT PACKAGE POWER PINS ARE: (14 PIN ICP) PIN 7 0V, PIN 14 +5V; (16 PIN ICP) PIN 8 0V, PIN 16 +5V, EXCEPT BDR, PIN 7 AND 8 0V, PIN 16 +5V.

9 +5V CONNECTOR PINS ARE: P1-A28, A29, B28, B29.

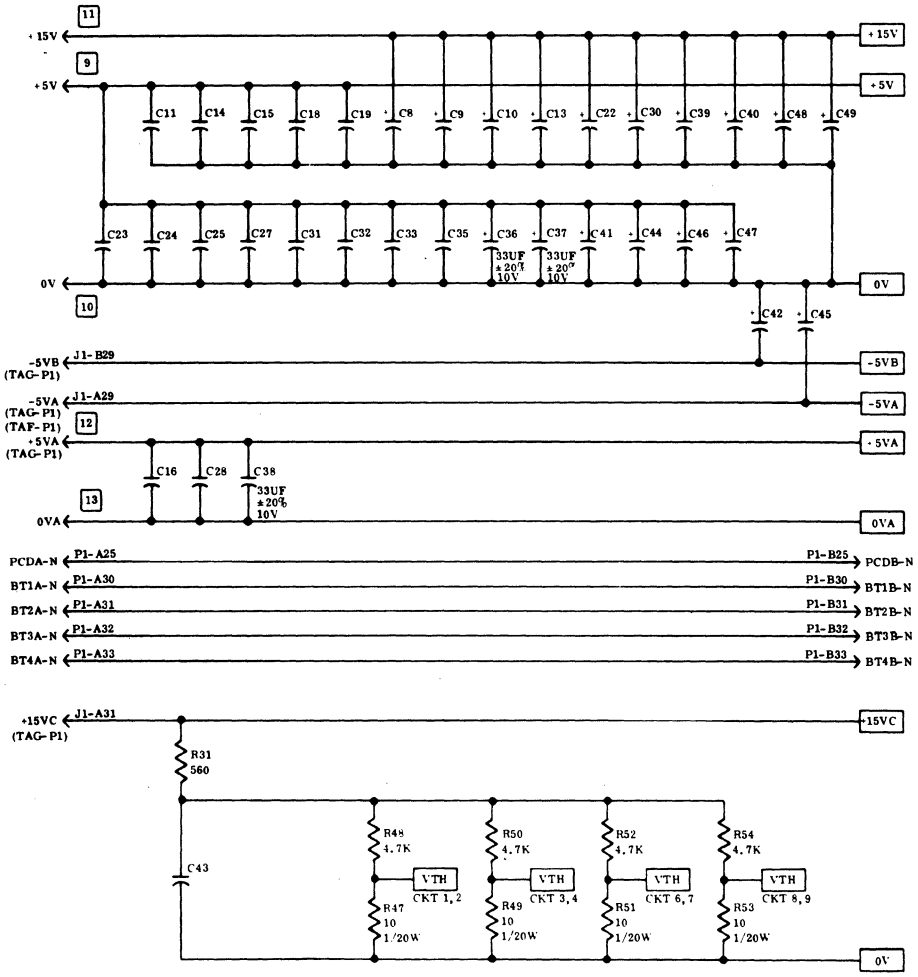
10 0V CONNECTOR PINS ARE: P1-A1, A2, A54, A55, B1, B2, B54, B55; J1-A1, A6, A9, A12, A15, A36, A39, A42, A45, A48, A54, B1, B6, B9, B12, B15, B36, B39, B42, B45, B48, B54.

11 +15V CONNECTOR PINS ARE: P1-A3, A4, B3, B4.

12 +5VA CONNECTOR PINS ARE: P1-A51, B51.

13 0VA CONNECTOR PINS ARE: P1-A40, B40.

14 LD2001002155-1, -2, AND -3 CONFIGURATION ARE IDENTICAL EXCEPT AS SHOWN ON TABLE I AND II ON SHEET 3.



SUE 3310 Sense, Inhibit Data (SID) Logic Diagram
LD2001002155, Rev. C, Sheet 1 of 5

TAG

MULTIPLEX LOGIC AND LINE DRIVERS/RECEIVERS (SID LD Sheet 2)

The multiplex circuits provide the means for data transfers in the byte mode.

During write operations in the byte mode, INFIBUS data bits DB00 through DB07 are transferred to either the left or the right byte position within the addressed word. The other byte position of the word remains unchanged.

During read operations in the byte mode, the byte located in bit positions 0 through 7 of the data word, are transmitted correspondingly over the INFIBUS. Data bits 8 through 15 are transmitted as zeros.

Operation of the multiplex units is controlled by the following control signals:

- General enabling term MCEL-P,
- Left byte data enabling term LDRH-N enables, and
- Right byte data enabling term LDRL-N.

Terms MCEL-P and LDRH-N being active simultaneously, causes transfer of the INFIBUS right byte data to corresponding data register left byte positions.

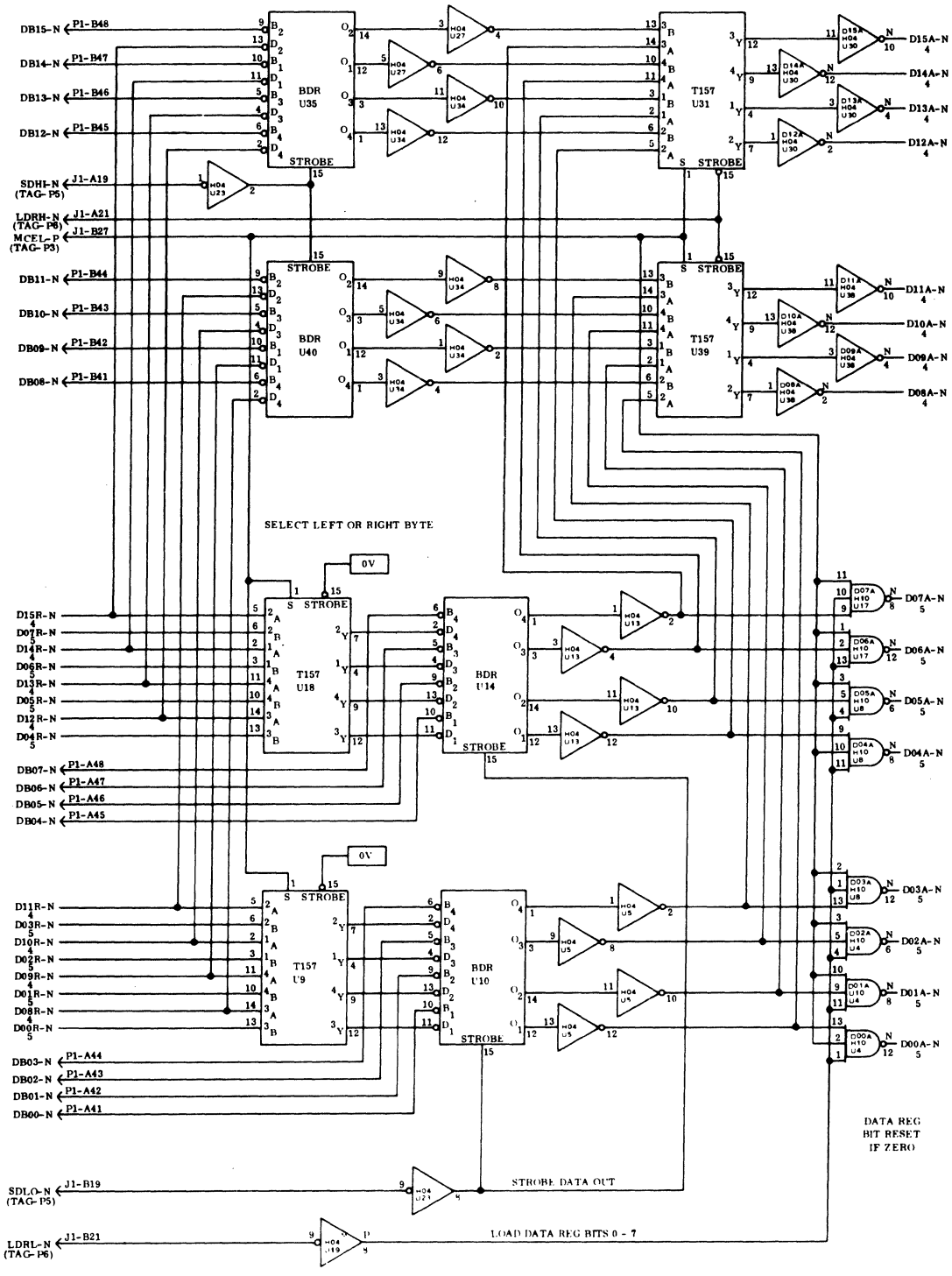
Although the multiplex capability to switch either data register byte is inherent in the circuit design, only the right byte to the left byte switching logic is implemented on the SID circuit card.

Line Drivers/Receivers

The line driver/receiver IC units U10, U14, U35 and U40, collectively receive data from the data register during read operations and from the INFIBUS during write operations. Data received from the storage data register is gated out the line drivers/receivers to the INFIBUS by terms SDHI-N and SDLO-N.

KEY LOGIC DEFINITIONS

D00A-N thru D15A-N	Data Register Bit Out
DB00-N thru DB15-N	Data Bit (INFIBUS)



SUE 3310 Sense, Inhibit Data (SID) Logic Diagram
LD2001002155, Rev. C, Sheet 2 of 5

TAG

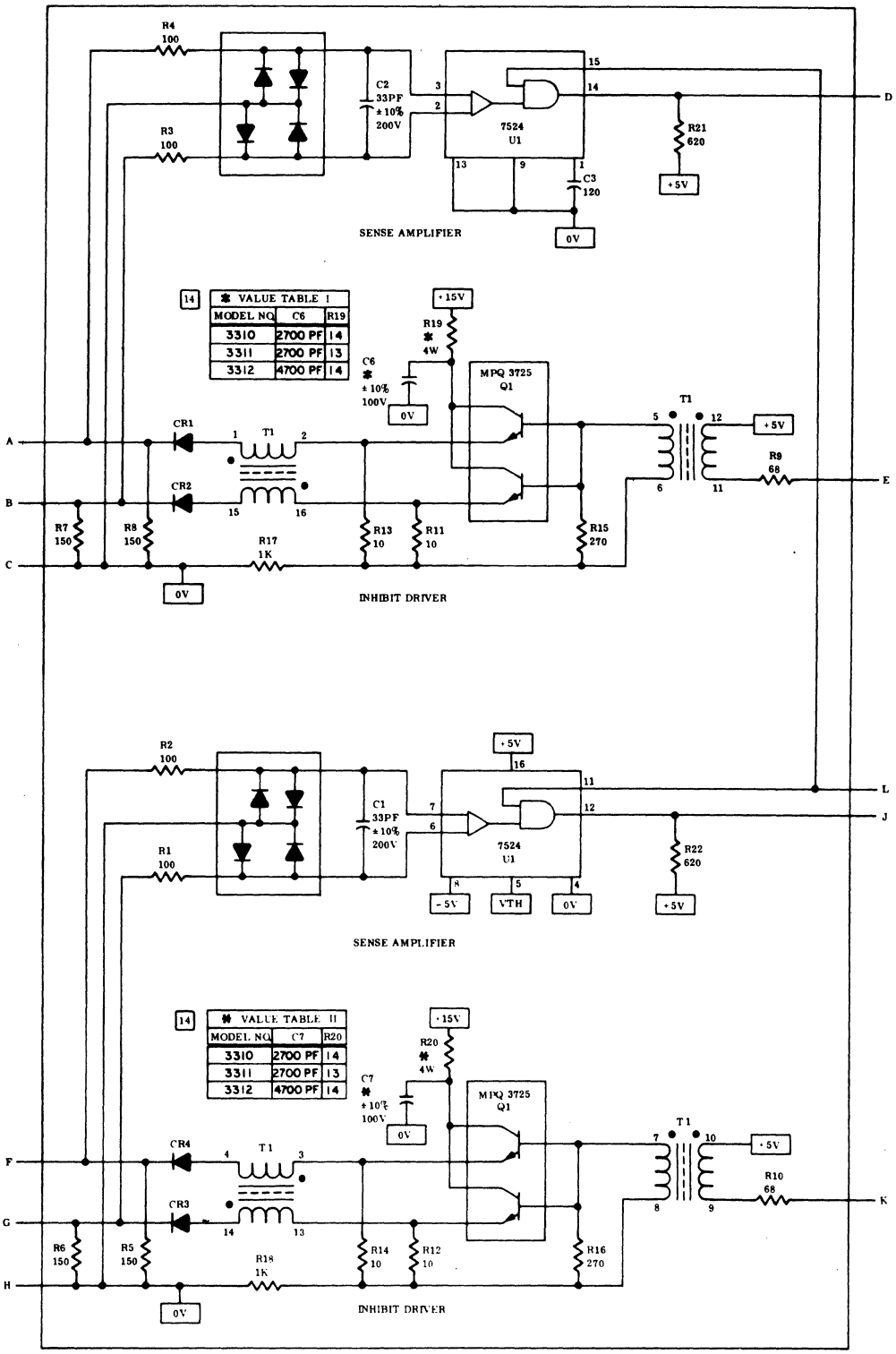
SENSE AMPLIFIER AND INHIBIT DRIVER SCHEMATIC DIAGRAM (SID LD Sheet 3)

Sense Amplifiers

Two 2048-core sense lines are serially joined together to form an 4096-core sense line (EXY LD sheet 10). The sense line from each mat in memory is connected to that sense amplifier associated with each mat (SID LD sheet 4 and 5). When the magnetic state of a ferrite core in a mat at the address specified by the address register changes from a logic one (ONE) state to a logic zero (ZERO) state, an electrical impulse is detected and amplified by the sense amplifier. Data from the sense amplifiers is strobed into the data register flip-flops by SASL-N (right byte) and SASH-N (left byte signals from the TAG circuit card). Data from the sense amplifiers is inverted by the gating logic before being entered into the data register flip-flops.

Inhibit Drivers

To preserve data during read operations, the output from each data register flip-flop is connected to an inhibit driver. Thus, 16 inhibit drivers are used to restore data-bit information read from core. When information read from memory is to be restored, each data register flip-flop with a ZERO state operates an associated inhibit driver. Complement states of data register flip-flops with ZEROs enable U6, U15, U28 and/or U36 gates when the INHR-N timing pulse from the TAG board is applied. When the U6, U15, U28 and/or U36 gates are enabled, pins E and/or K are grounded and the associates inhibit driver(s) is (are) pulsed. These inhibit drivers that are pulsed, produce a current through the corresponding sense-inhibit line that inhibits the writing of a ONE in the associated mat.



SUE 3310 Sense, Inhibit Data (SID) Logic Diagram
LD2001002155, Rev. C, Sheet 3 of 5

TAG

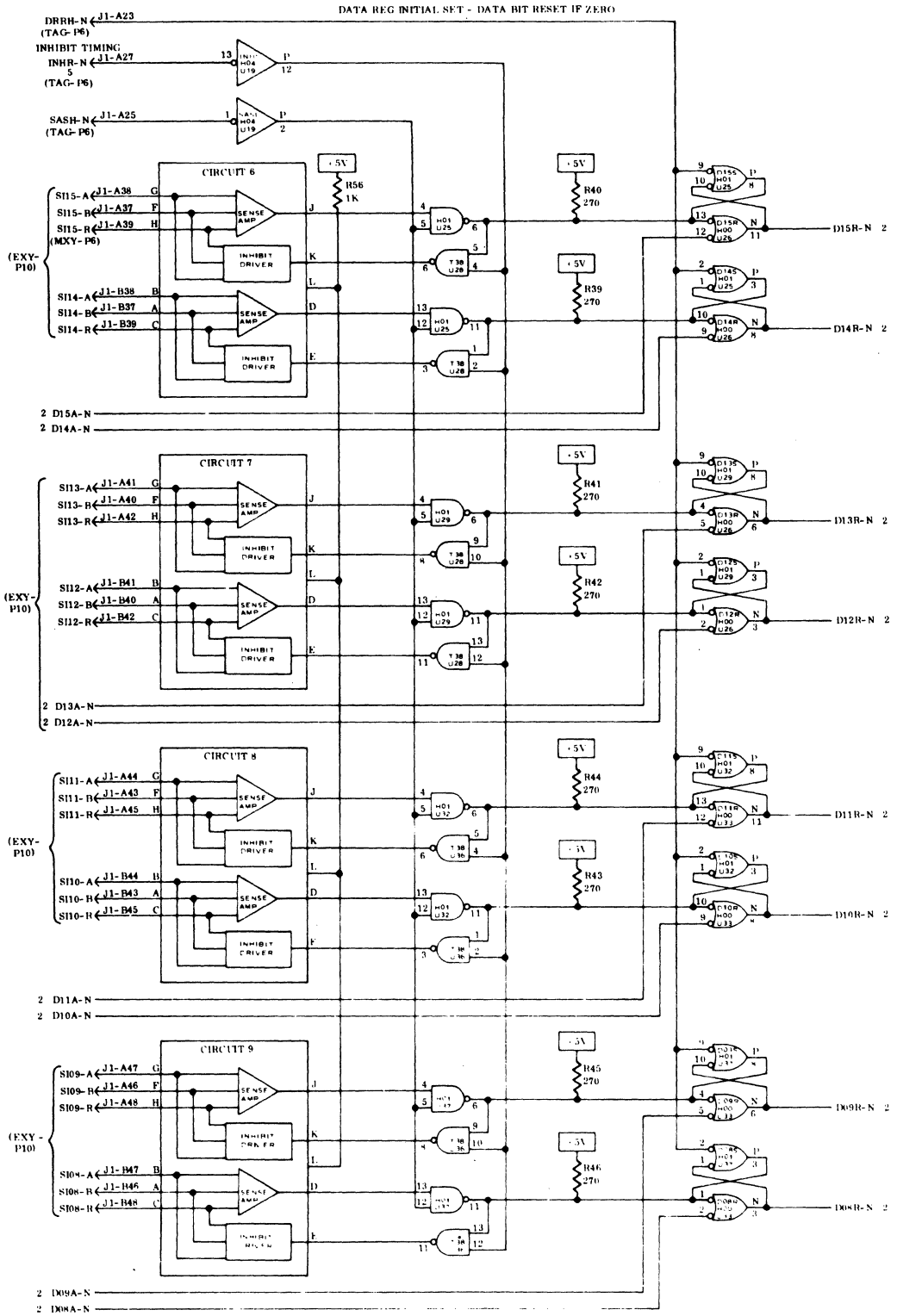
DATA REGISTER LEFT BYTE (SID LD Sheet 4)

Depending upon the mode of operation, input data to the left-byte data register flip-flops is either from the sense amplifiers or from the INFIBUS. Prior to the loading of data into the left byte data registers, DRRH-N (from the TAG circuit card) sets the left byte data register flip-flops controlling data bits D08R-N through D15R-N.

Output from the data register flip-flops to the INFIBUS is controlled by the BYTE signal from the INFIBUS. In byte mode, the left-byte can be transferred either through associated line drivers/receivers to corresponding INFIBUS lines or through multiplex circuits U9 and U18 (SID LD sheet 2) to the INFIBUS right-byte lines when enabled by MCEL-P from the TAG circuit card.

KEY SOURCE LOGIC DEFINITIONS

D08R-N thru D15R-N	Data Register Output 08 through 15
DRRH-N	Data Register Reset, Left Byte (Negative)
INHS-P	Inhibit Timing Inverted, Left Byte (Positive)
SASI-P	Sense Amplifier Strobe Inverted, Left Byte (Positive)



SUE 3310 Sense, Inhibit Data (SID) Logic Diagram
LD2001002155, Rev. C, Sheet 4 of 5

TAG

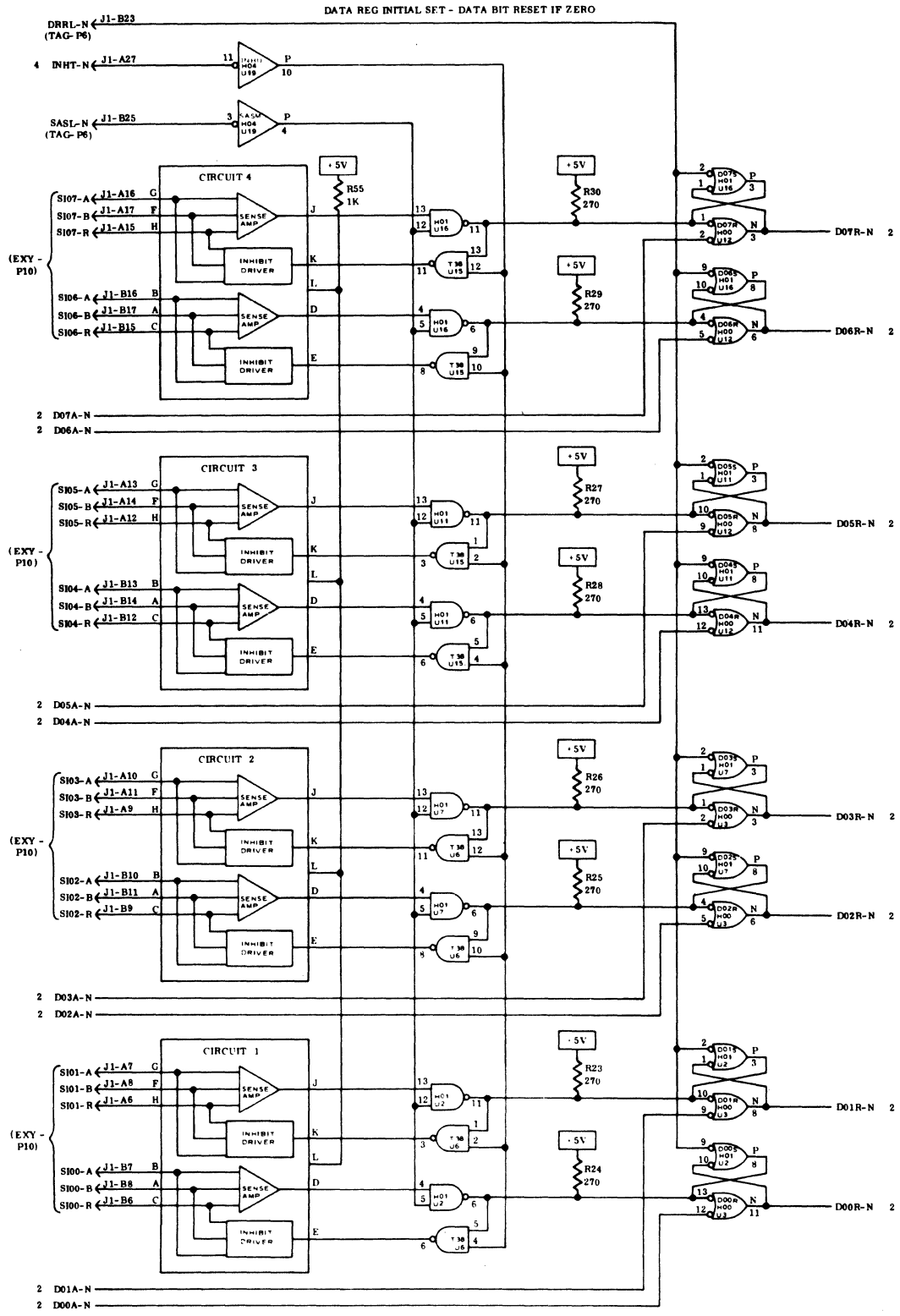
DATA REGISTER RIGHT BYTE (SID LD Sheet 5)

Depending upon the mode of operation, input data to the right-byte data register flip-flops is either from the sense amplifiers or from the INFIBUS. Prior to the loading of data into the right byte data registers, DRRL-N (from the TAG circuit card) sets the right byte data register flip-flops controlling data bits D00R-N through D07R-N.

Output from the data register flip-flops to the INFIBUS is controlled by the BYTE signal from the INFIBUS. In byte mode, the right-byte can be transferred either through associated line drivers/receivers to corresponding INFIBUS lines or through multiplex circuits U9 and U18 (SID LD sheet 2) to the INFIBUS right-byte lines when enabled by MCEL-P from the TAG circuit card.

KEY SOURCE LOGIC DEFINITIONS

D00R-N thru D07R-N	Data Register Output 00 through 07
DRRL-H	Data Register Reset, Right Byte (Negative)
INHV-P	Inhibit Timing Inverted, Right Byte (Positive)
SASM-P	Sense Amplifier Strobe Inverted, Right Byte (Positive)



SUE 3310 Sense, Inhibit Data (SID) Logic Diagram
LD2001002155, Rev. C, Sheet 5 of 5

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	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002273-0		KIT			1
002		000								2
003		000								3
004		120	0001		10050000764-1		PIN, TERMINAL		NOTE 211	4
005		001	0001		8001600001-1		DELAY LINE		DL1	5
006		001	0001		8001600004-1		DELAY LINE		DL2	6
007		001	0001		LC-DIP-100B	91615	DELAY LINE	ALLEN AVIONICS	DL3	7
008		000								8
009		000								9
010		000								10
011		001	0001		8001100001-1		DIODE		CR1 .5 IS	11
012		001	0001		8001100002-1		DIODE, ZENER		CR2 .5 IS	12
013		002	0001		1N5231B		DIODE, ZENER		CR3,4 .5 IS	13
014		000								14
015		001	0001		2N4898		TRANSISTOR		Q1 (TO-66)	15
016		000								16
017		007	0001		8001800042-1		ICP		U25,31,34,58,61, 62,71 (74H00)	17
018		003	0001		8001800044-1		ICP		U27,36,49 (74H04)	18
019		005	0001		8001800046-1		ICP		U24,32,35,48,78 (74H10)	19
020		002	0001		8001800047-1		ICP		U42,52 (74H11)	20
021		001	0001		8001803203-1		ICP		U47 (74S11)	21
022		001	0001		8001800050-1		ICP		U18 (74H22)	22
023		002	0001		8001800052-1		ICP		U33,77 (74H40)	23
024		003	0001		8001800054-1		ICP		U21,41,72 (74H51)	24
025		001	0001		8001800055-1		ICP		U57 (74H52)	25
026		000								26
027		001	0001		8001800058-1		ICP		U59 (74H55)	27
028		002	0001		8001800100-1		ICP		U28,38 (7475)	28
029		004	0001		8001800120-1		ICP		U20,30,40,50 (BDR)	29
030		001	0001		8001803198-1		ICP		U22 (74S00)	30
031		001	0001		8001803202-1		ICP		U23 (74S10)	31
032		001	0001		8001803139-1		ICP		U37 (7437)	32
033		001	0001		8001803128-1		ICP		U51 (7412)	33
034		001	0001		8001803212-1		ICP		U60 (74S112)	34
035		001	0001		U6A7723393	07263	ICP	FAIRCHILD	U13	35

TAG

SUE 3310 Timing and Gating (TAG) Parts List
PL2001002273, Rev. D, Sheet 3

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
036		002	0001		N8242A	18324	ICP	SIGNETICS	U19,39	36
037		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U68	37
038		002	0001		SN74S51N	01295	ICP	TEXAS INSTR INC	U69,79	38
039		018	0001		8001300101-1		CAPACITOR		C4,6,7,10,11,14, 15,16,17,23,24, 25,27,28,29,31, 32,33 .25 IS	39
040		001	0001		8001300015-1		CAPACITOR		C5 .1 IS	40
041		007	0001		8001300311-2		CAPACITOR		C8,9,13,18,19, 21,22 .8 IS	41
042		006	0001		8001300333-2		CAPACITOR		C2,3,12,20,26, 30 .8 IS	42
043		001	0001		8001300323-2		CAPACITOR		C1 1.1 IS	43
044		001	0001		SN74S02N	01295	ICP	TEXAS INSTR INC	U80	44
045		000								45
046		000								46
047		013	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R16,19,23,24,25, 26,27,32,33,34, 35,18,29 .5 IS	47
048		012	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R7,8,9,10,11,12, 13,14,15,21,31, 39 .5 IS	48
049		001	0001		RL07S620G		RESISTOR	MIL-R-22684/1	R1 .5 IS	49
		001	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R6 .5 IS	50
051		003	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R20,28,37 .5 IS	51
052		003	0001		RL32S510G		RESISTOR	MIL-R-22684/3	R17,36,38 .8 IS	52
053		003	0001		RL42S101G		RESISTOR	MIL-R-22684/4	R2,22,30 1.0 IS	53
054		001	0001		RN55D1241F		RESISTOR	MIL-R-10509/7	R4 .5 IS	54
055		000								55
056		002	0001		3007P-1-502	80294	RESISTOR,VARIABLE	BOURNS, INC	R3,5	56
057		002	0001		26AWG WHT		TUBING (TEFLON)	MIL-I-22129	APPROX INCH REQD	57
058		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		58
059		010	0001		90034000417-10		WIRE, SOLID		30AWG WHT APPROX FT REQD	59
060		001	0001		90034000419-4		WIRE, SOLID		28AWG APPROX FT REQD	60

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002273-2		TAG-CKT CARD ASSY		USED ON SUE 3310,3210	1
002		001	0001		2001002273-0		KIT			2
003		001	0001		1001005408-1		PRINTED WRG BD, TAG			3
004		REF	0001		LD2001002273-2		LOGIC DIAGRAM			61

TIMING WIRE LIST

FROM	TO	COLOR	FIND NO.
E91	E43	WHT	59
E82	E72	WHT	59
E28	E69	WHT	59
E9	E67	WHT	59
E32	E46	WHT	59
E17	E42	WHT	59
E12	E63	WHT	59
E82	E68	WHT	59
E52	E44	WHT	59
E16	E56	WHT	59
E18	E58	WHT	59
E31	E33	WHT	59
E4	E57	WHT	59
E78	E54	WHT	59
E73	E55	WHT	59
E85	E41	WHT	59
E87	E47	WHT	59
E131	E71	WHT	59
E12	E39	WHT	59
E30	E40	WHT	59
E27	E64	WHT	59
E24	E34	WHT	59
E74	E59	WHT	59
E25	E65	WHT	59
E51	E38	WHT	59
E9	E35	WHT	59
E25	E37	WHT	59
E17	E36	WHT	59
E4	E66	WHT	59
E2	E48	WHT	59
J4-2	J4-3	WHT	60 & 57
J5-1	J5-2	WHT	60 & 57
E141	E142	WHT	59
E10	E50	WHT	59
E6	E26	WHT	59
E8	E49	WHT	59
J2-A5	J2-B5	WHT	60
J2-A6	J2-B6	WHT	60
J2-A7	J2-B7	WHT	60
E201	E208	WHT	59
E202	E209	WHT	59
E203	E210	WHT	59
E204	E211	WHT	59
E205	E212	WHT	59
E206	E213	WHT	59
E207	E214	WHT	59

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002273-4		TAG-CKT CARD ASSY		USED ON SUE 3310,3210	1
002		001	0001		2001002273-0		KIT			2
003		001	0001		1001005140-1		PRINTED WRG BD, TAG			3
004		001	0001		AS-143-U-3	06776	SOCKET	ROBINSON NUGENT	(U80)	45
005		001	0001		NO.4416 X 3/4	26066	TAPE	3M CO	.75 X .70 LG APPROX INCH REQD	46
006		A/R	0001		RTV 3140	71984	RTV COATING	DOW CORNING		55
007		REF	0001		LD2001002273-4		LOGIC DIAGRAM			61

TIMING WIRE LIST

FROM	TO	COLOR	FIND NO.
E91	E43	WHT	59
E82	E72	WHT	59
E28	E69	WHT	59
E9	E67	WHT	59
E32	E46	WHT	59
E17	E42	WHT	59
E12	E63	WHT	59
E82	E68	WHT	59
E52	E44	WHT	59
E16	E56	WHT	59
E18	E58	WHT	59
E31	E33	WHT	59
E4	E57	WHT	59
E78	E54	WHT	59
E73	E55	WHT	
E85	E41	WHT	
E87	E47	WHT	59
E131	E71	WHT	59
E12	E39	WHT	59
E30	E40	WHT	59
E27	E64	WHT	59
E24	E34	WHT	59
E74	E59	WHT	59
E25	E65	WHT	59
E51	E38	WHT	59
E9	E35	WHT	59
E25	E37	WHT	59
E17	E36	WHT	59
E4	E66	WHT	59
E2	E48	WHT	59
J4-2	J4-3	WHT	60 & 57
J5-1	J5-2	WHT	60 & 57
E141	E142	WHT	59
E10	E50	WHT	59
E6	E26	WHT	59
E8	E49	WHT	59
J2-A5	J2-B5	WHT	60
J2-A6	J2-B6	WHT	60
J2-A7	J2-B7	WHT	60
E201	E208	WHT	59
E202	E209	WHT	59
E203	E210	WHT	59
E204	E211	WHT	59
E205	E212	WHT	59
E206	E213	WHT	59
E207	E214	WHT	59

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002219-2		EXY-CKT CARD ASSY		USED ON SUE 3310	1
002		001	0001		1001004954-5		PRINTED WRG BD, EXY			2
003		001	0001		2001002224-1		FRAME, ASSY			3
004		001	0001		1001005141-1		COVER			4
005		000								5
006	F	001	0001		8001800044-1		ICP		U17)74H04)	6
007	F	004	0001		8001800083-1		ICP		U3,4,21,20 (7442)	7
008	F	003	0001		8001800100-1		ICP		U8,12,18 (7475)	8
009		003	0001		8001800123-1		ICP		U15,16,19 (BDR)	9
010	F	001	0001		8001803139-1		ICP		U14 (7437)	10
011		016	0001		SN75325N	01295	ICP	TEXAS INSTR INC	U1,2,5,6,7,9,10, 11,23,26,28,29, 30,32,33,34	11
012		002	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U13,25	12
013		000								13
014		000								14
015	E	002	0001		8001400092-1		TRANSFORMER		Z1,2	15
016		000								16
017	E	004	0001		8001200016-1		TRANSISTOR		Q1 THRU Q4 (TO5)	17
		000								18
019	E	047	0001		8001100001-1		DIODE		CR1 THRU CR24, CR26 THRU CR33, CR36,37,38, CR41 THRU CR46, CR49 THRU CR54 .5 IS	19
020		000								20
021		000								21
022		003	0001		8001300309-2		CAPACITOR		C3,15,19 .65 IS	22
023		002	0001		8001300311-2		CAPACITOR		C7,11 .8 IS	23
024		005	0001		8001300333-2		CAPACITOR		C1,4,9,10,13 .8 IS	24
025	F	010	0001		8001300101		CAPACITOR		C2,5,6,8,12,14, 16,17,18,20 .25 IS	25
026		000								26
027		000								27
028		001	0001		RL07S120G		RESISTOR	MIL-R-22684/1	R48 .5 IS	28
029		022	0001		RL07S202G		RESISTOR	MIL-R-22684/1	R1 THRU R4, R6 THRU R9, R13 THRU R17, R26,35,36,42,43, 46,47,51,52 .5IS	29
030		002	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R5,37 .5 IS	30

TAG

SUE 3310 Memory Electronics and XY Matrix (EXY) Parts List
PL2001002219-2, Rev. C, Sheet 4

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
031		004	0001		RL07S511G		RESISTOR	MIL-R-22684/1	R24,25,54,56 .5 IS	31
032		001	0001		RL07S680G		RESISTOR	MIL-R-22684/1	R18 .5 IS	32
033	B	006	0001		TYPE BR5-47.0	07716	RESISTOR	IRC, INC	R11,22,23,31,32, 39 .6 IS BR5-47.0 OHM1PCT TC100PPM/C DEG	33
033	B	000	0001		TYPE BR4-47.0	07716	RESISTOR	IRC, INC	R11,22,23,31,32, 39 .6 IS BR4-47.0 OHM1PCT TC100PPM/C DEG	33&
034	B	004	0001		TYPE BR5-150	07716	RESISTOR	IRC, INC	R20,21,29,30 .6 IS BR5-150 OHM1PCT TC100PPM/C DEG	34
034	B	000	0001		TYPE BR4-150	07716	RESISTOR	IRC, INC	R20,21,29,30 .6 IS BR4-150 OHM1PCT TC100PPM/C DEG	34&
035	B	001	0001		TYPE BR5-324	07716	RESISTOR	IRC, INC	R12 .6 IS BR5-324 OHM1PCT TC100PPM/C DEG	35
035	B	000	0001		TYPE BR4-324	07716	RESISTOR	IRC, INC	R12 .6 IS BR4-324 OHM1PCT TC100PPM/C DEG	35&
036		001	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R55 .5 IS NOTE 219	36
037		002	0001		RL07S621G		RESISTOR	MIL-R-22684/1	R10,38 .5 IS	37
038		002	0001		RL07S431G		RESISTOR	MIL-R-22684/1	R19,28 .5 IS	38
039		001	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R27 .5 IS	39
040		001	0001		9310-20		INDUCTOR	J.W. MILLER CO COMPTON, CA	L1 .6 IS	40
041		001	0001		9310-18		INDUCTOR	J.W. MILLER CO COMPTON, CA	L2 .6 IS	41
042		006	0001		9003400419-7		WIRE, BARE		28AWG APPROX INCH REQD	42
043		004	0001		2226B	13103	HEATSINK	THERMALLOY		43
044		004	0001		10050000041-1		TRANSIPAD		TO5	44
045		006	0001		9003400419-3		WIRE, RISER		APPROX FT REQD	45
046		006	0001		10010005025-2		SPACER		5/16 DIA	46
047		008	0001		10050000764-1		PIN, TERMINAL		NOTE 217	47
048		A/R	0001		1203	71984	PRIMER	DOW CORNING		48
049		A/R	0001		RTV3145	71984	ADHESIVE	DOW CORNING		49
050		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		50
051		000								51
052		REF	0001		LD20010002219-2		LOGIC DIAGRAM			52
053		000								53
054		003	0001		26AWG WHT		SLEEVING	MIL-I-22129	APPROX INCH REQD	54
		001	0001		M70-9-506	14193	THERMISTER	CAL-R, INC	RT1 .1 IS	55
		A/R	0001		DELTA BOND	05820	ADHESIVE	WAKEFIELD ENGR	NO. 152	56
		A/R	0001		RTA	05820	HARDENER	WAKEFIELD ENGR		57

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		2001002155-3		SID-CKT CARD ASSY		USED ON SUE 3310	1
002		001	0001		1001004740-1		PRINTED WRG BD, SID			2
003		001	0001		RL07S561G		RESISTOR	MIL-R-22684/1	R31 .45 IS	3
004		032	0001		RL07S101G		RESISTOR	MIL-R-22684/1	1R1 THRU 4R1, 6R1 THRU 9R1, 1R2 THRU 4R2, 6R2 THRU 9R2, 1R3 THRU 4R3, 6R3 THRU 9R3, 1R4 THRU 4R4, 6R4 THRU 9R4 .45 IS	4
005		032	0001		RL07S151G		RESISTOR	MIL-R-22684/1	1R5 THRU 4R5, 6R5 THRU 9R5, 1R6 THRU 4R6, 6R6 THRU 9R6, 1R7 THRU 4R7, 6R7 THRU 9R7, 1R8 THRU 4R8, 6R8 THRU 9R8 .45 IS	5
006		018	0001		RL07S102G		RESISTOR	MIL-R-22684/1	1R17 THRU 4R17, 6R17 THRU 9R17, 1R18 THRU 4R18, 6R18 THRU 9R18, R55,56 .45 IS	6
007		032	0001		RL07S100G		RESISTOR	MIL-R-22684/1	1R11 THRU 4R11, 6R11 THRU 9R11, 1R12 THRU 4R12, 6R12 THRU 9R12, 1R13 THRU 4R13, 6R13 THRU 9R13, 1R14 THRU 4R14, 6R14 THRU 9R14 .45 IS	7
008		016	0001		RL07S680G		RESISTOR	MIL-R-22684/1	1R9 THRU 4R9, 6R9 THRU 9R9, 1R10 THRU 4R10, 6R10 THRU 9R10 .45 IS	8
009		032	0001		RL07S271G		RESISTOR	MIL-R-22684/1	1R15 THRU 4R15, 6R15 THRU 9R15, 1R16 THRU 4R16, 6R16 THRU 9R16, R23 THRU R30, R39 THRU R46 .45 IS	9
010		005	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R32,48,50,52,54 .45 IS	10
011		005	0001		RN50C10R0F		RESISTOR	MIL-R-55182	R34,47,49,51,53 .35 IS	11
012		000								12
013		016	0001		NLS2-14 OHM1PCT	91637	RESISTOR	DALE ELEC INC	1R19 THRU 4R19, 6R19 THRU 9R19, 1R20 THRU 4R20, 6R20 THRU 9R20 .675 IS	13
014		000	0001		SP1413	14193	RESISTOR	CAL-R, INC	1R19 THRU 4R19, 6R19 THRU 9R19, 1R20 THRU 4R20, 6R20 THRU 9R20 .675 IS	13A

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SUE 3310 Sense, Inhibit Data (SID) Parts List
PL2001002155, Rev. F, Sheet 8

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
015	016	0001		RL07S621G		RESISTOR	MIL-R-22684/1	1R21 THRU 4R21, 6R21 THRU 9R21, 1R22 THRU 4R22, 6R22 THRU 9R22 .50 IS	14
016	032	0001		8001100001-1		DIODE		1CR1 THRU 4CR1, 6CR1 THRU 9CR1, 1CR2 THRU 4CR2, 6CR2 THRU 9CR2, 1CR3 THRU 4CR3, 6CR3 THRU 9CR3, 1CR4 THRU 4CR4, 6CR4 THRU 9CR4 .45 IS	15
017	008	0001		8001400051-1		TRANSFORMER		1T1 THRU 4T1, 6T1 THRU 9T1	16
018	008	0001		MP03725	04713	TRANSISTOR	MOTOROLA	1Q1 THRU 4Q1, 6Q1 THRU 9Q1	17
019	016	0001		8001300006-1		CAPACITOR		1C1 THRU 4C1, 6C1 THRU 9C1, 1C2 THRU 4C2, 6C2 THRU 9C2 .10 IS	18
020	006	0001		8001300309-2		CAPACITOR		C42,45,41,44,46, 47 .65 IS	19
021	016	0001		8001300101-1		CAPACITOR		C11,14,15,16,18, 19,23,24,25,27, 28,31,32,33,35, 43 .25 IS	20
[illegible]	016	0001		300100Y5S272K	08514	CAPACITOR	CENTRE ENG	1C6 THRU 4C6, 6C6 THRU 9C6, 1C7 THRU 4C7, 6C7 THRU 9C7 .20 IS	21
023	000	0001		CK05BX272K		CAPACITOR	MIL-C-11015/18	1C6 THRU 4C6, 6C6 THRU 9C6, 1C7 THRU 4C7, 6C7 THRU 9C7 .20 IS	21A
024	003	0001		8001300311-2		CAPACITOR		C36,37,38 .80 IS	22
025	010	0001		8001300333-2		CAPACITOR		C8,9,10,13,22, 30,40,48,49,39 .80 IS	23
026	000								24
027	008	0001		CK05BX121K		CAPACITOR	MIL-C-11015/18	1C3 THRU 4C3, 6C3 THRU 9C3	25
028	004	0001		8001800042-1		ICP		U3,12,26,33 (74H00)	26
029	008	0001		8001800043-1		ICP		U2,7,11,16,25, 29,32,37 (74H01)	27
030	008	0001		8001800044-1		ICP		U5,13,19,23,27, 30,34,38 (74H04)	28
031	003	0001		8001800046-1		ICP		U4,8,17 (74H10)	29
032	004	0001		8001800120-1		ICP		U10,14,35,40 (BDR)	30
033	004	0001		8001803140-1		ICP		U6,15,28,36 (7438)	31
	000								32
	004	0001		8001803169-1		ICP		U9,18,31,39 (74157)	33

SUE 3310 Sense, Inhibit Data (SID) Parts List
PL2001002155, Rev. F, Sheet 9

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
036		008	0001		SN7524N	01295	ICP	TEXAS INSTR INC	1U1 THRU 4U1, 6U1 THRU 9U1	34
037		000								35
038		000								36
039		004	0001		1001005125-2		DIODE, CLUST, COM CATH		Z2,4,8,10	37
040		000								38
041		004	0001		1001005126-2		DIODE, CLUST, COM ANOD		Z1,3,7,9	39
042		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		40
043		REF	0001		LD2001002155-3		LOGIC DIAGRAM			41

TAG

SUE 3312 8K X 16 MAGNETIC CORE MEMORY

MAINTENANCE BULLETIN M3312

TAG

1296

May 1973

This bulletin contains the following documents in the order listed:

TAG

SUE 3312
10/4/72
Rev. 1

PRODUCT SPECIFICATION

Title:	PROGRAM MEMORY - CORE 8192 WORD - 875 ± 25 ns
Function:	To provide an optional program memory module for the SUE system.
Description:	The 8192 word by 16-bit (18 with parity) core memory is contained on three module boards which mount in three adjacent slots within any SUE chassis. The memory interfaces to the SUE system via the INFIBUS The address range is assigned by jumpers installed on the address module to provide comparison for address bits 1 and 13 to 17. All bits are provided with an override option. Masking of 30-32K or 31 to 32K is possible. The memory read access delay is $\leqslant$ 550 nsec. The write access delay is $\leqslant$ 280 nsec. The fastest cycle time is 875 ± 25 ns.
Split Cycle:	Read access $\leqslant$ 550 nsec; restart enabled at $\leqslant$ 550 nsec; modify time $\leqslant$ 300 nsec from fall of RITE; fastest split cycle time $\leqslant$ 1.1 μs.
Size:	Three PWB requiring 3 slots.
Weight:	4 lbs.
Power Required:	+15 volts @ 5 amps max. +5 volts @ 3.1 amps max. -15 volts @ 0.3 amps max.
Operating Temp.:	0^{o}C to 50^{o}C.

CORE MEMORY SPECIFICATION

SUE 3312

This document defines the design goals and functional operation of the NPL 3312 core memory (8K x 18).

The following lines will be recognized by the memory:

Read/Write Command 1	($\overline{\text{RITE}}$)	Mode Control
Read/Write Command 2	($\overline{\text{HCYC}}$)	Mode Control
Byte Command	($\overline{\text{BYTE}}$)	Byte or word operation
Address Line 00	($\overline{\text{AB00}}$)	Controls which byte is acted upon
Address Line 01 to 13	($\overline{\text{AB01}}$ to $\overline{\text{AB13}}$)	Addressing for drive line decode
Address Line 14 to 17	($\overline{\text{AB14}}$ to $\overline{\text{AB17}}$)	Addressing for memory select decode
Strobe	($\overline{\text{STRB}}$)	Initiates cycle in memory
Data 00 to 15	($\overline{\text{DB00}}$ to $\overline{\text{DB15}}$)	Data bus lines
Parity Bits	($\overline{\text{PBL0}}$ to $\overline{\text{PBH1}}$)	Parity Bus Lines
Operation Complete	($\overline{\text{DONE}}$)	Signal for operation complete
Memory Disable	($\overline{\text{HOLD}}$)	Disables memory cycle initiate
Memory Reset	($\overline{\text{MRES}}$)	Resets all control flip flops

TAG

CORE MEMORY SPECIFICATION

SUE 3312

The following chart indicates module control recognition:

RITE	HCYC	BYTE			
0	0	1	By Byte	Read/Restore	
0	0	0	By Word		
1	0	1	By Byte	Clear/Write	
1	0	0	By Word		
0	1	1	By Byte	Read Portion	READ MODIFY WRITE
0	1	0	By Word		
1	1	1	By Byte	Write Portion	
1	1	0	By Word		
1	1	1	By Byte	Undefined	Read/Restore w/o Data or DONE
1	1	0	By Word		

Modes of Operation:

Read/Restore: Data is read out of core, transmitted on the bus line along with DONE, and stored back in core. Cycle time = 900 nanoseconds maximum.

Clear/Write: Data is read out of core and destroyed. Data on the bus is transferred into the data register and written into core. DONE will occur 280 ns maximum into the cycle releasing the Infibus.

Read/Modify/Write: Data is read out of core, transmitted on the bus line along with DONE, and the memory cycle stops. Upon the switching of RITE from a logic "0" to a logic "1", the memory will execute the write portion of the cycle. Approximately 50 nanoseconds into the write cycle, the data register will have been cleared and the new data will be strobed in. Upon completion of the strobing, DONE will be transmitted releasing the Infibus. (300 ns max after fall of RITE).

Undefined: In the event that a memory is selected and both of the mode control lines are at logic "1", the memory will perform a Read/Restore cycle, but neither data nor DONE will be transmitted on the Infibus.

Byte Control:

Byte Command = Logic "1"

a. Address Bits 00 (AB00) = Logic "1"

All data bits handled by Data Register Bits 00 to 07 will be transmitted or received on Data Bus lines DB00 to DB07. All mode operations will be performed on Data Register Bits 00 to 07. All data handled by Data Register bits 08 to 15 will be in the Read/Restore mode and no data will appear on Data bus lines DB08 to DB15.

TAG

b. Address Bit 00 (AB00) = Logic "0"

All data bits handled by Data Register Bits 00 to 07 will be in an automatic Read/Restore mode and will not be transmitted on the Infibus. All data handled in Data Register Bits 08 to 15 will be transmitted and received on Data bus lines DB00 to DB07. All mode operations will be performed on Data Register Bits 08 to 15.

Byte Command = Logic "0"

Address Bit 00 (AB00) will be ignored and all mode operations will be performed on the entire word (Data Register Bits 00 to 15). All data will be transmitted and received on Data bus lines DB00 to DB15.

Address Recognition

Since the Address Register (AB01 to AB13) input will be active from the end of the

Address Recognition, continued

previous cycle until 65 nanoseconds after the beginning of the new cycle, the address lines must be valid by strobe time (STRB) and remain valid for at least 100 nanoseconds after strobe. Address bits AB14 to AB15 are not stored and require the same conditions as the lower order address bits.

Address Recognition of all bits is an option capability; likewise, masking of 30K-32K or 31K-32K is an option.

The Mode Control lines are strobed into the mode control register the same as the address register.

Write Restart in the R/M/W Mode

Two conditions exist during this mode. Under normal operating conditions, when the memory has reached the halt condition, the changing of the state of RITE from a logic "0" to a logic "1" will initiate the write portion of the cycle.

However, the strobe ($\overline{\text{STRB}}$) line will also be monitored. If, while the memory is in the halt condition, the strobe should change state from a logic "1" to a logic "0", the write portion of the cycle will be initiated. Since this isn't a normal operation, the memory will write into core whatever was stored in the data register during the read portion. However, there will be no DONE signal indicating the memory has completed the cycle.

HOLD-Memory Disable

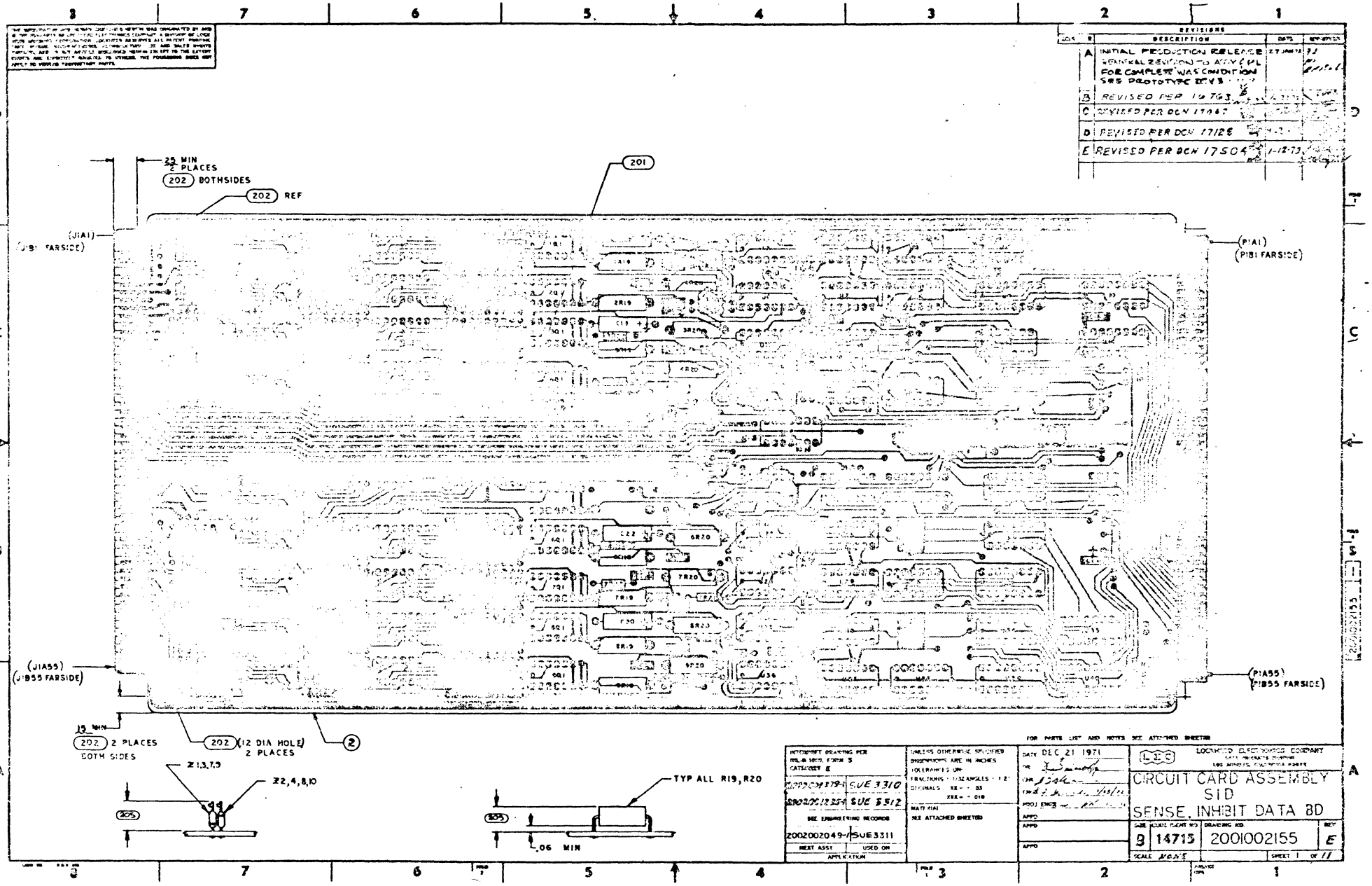
If this line is at logic "1" level at strobe time ($\overline{\text{STRB}}$) = logic "1", the memory will remain in an idle state until such time as the HOLD line returns to a logic "0". Then the memory will respond in accordance with the present State of the BUS address and STRB.

Parity Bits (PBLO and PBHI)

These bits will be handled the same as data bits and will be associated with the data bits as follows:

PBLO with Data Register Bits 00 - 07

PBHI with Data Register Bits 08 - 15


.33 MIN
2 PLACES
202 BOTHSIDES
202 REF
201
(J1A1)
(J1B1 FARSIDE)
(P1A1)
(P1B1 FARSIDE)
(J1A55)
(J1B55 FARSIDE)
(P1A55)
(P1B55 FARSIDE)
.19 MIN
202 2 PLACES
BOTH SIDES
202 (.12 DIA HOLE)
2 PLACES
2
Z1,3,7,9
Z2,4,8,10
205
TYP ALL R19, R20
.06 MIN
REVISIONS
A INITIAL PRODUCTION RELEASE
B REVISED PER 14763
C REVISED PER DCN 17067
D REVISED PER DCN 17125
E REVISED PER DCN 17504
1-12-73
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ± 1/32 ANGLES ± 1°
DECIMALS .XX ± .03
.XXX ± .010
MATERIAL
SEE ATTACHED SHEETED
FOR PARTS LIST AND NOTES SEE ATTACHED SHEETED
DATE DEC 21 1971
LOCKHEED ELECTRONICS COMPANY
LOS ANGELES, CALIFORNIA
CIRCUIT CARD ASSEMBLY
SID
SENSE, INHIBIT DATA BD
SIZE B
CODE IDENT NO 14715
DRAWING NO 2001002155
REV E
SCALE 4/1
SHEET 1 OF 11
SEE ENGINEERING RECORDS
2002002049-1 SUE 3311
NEXT ASSY
USED ON
APPLICATION

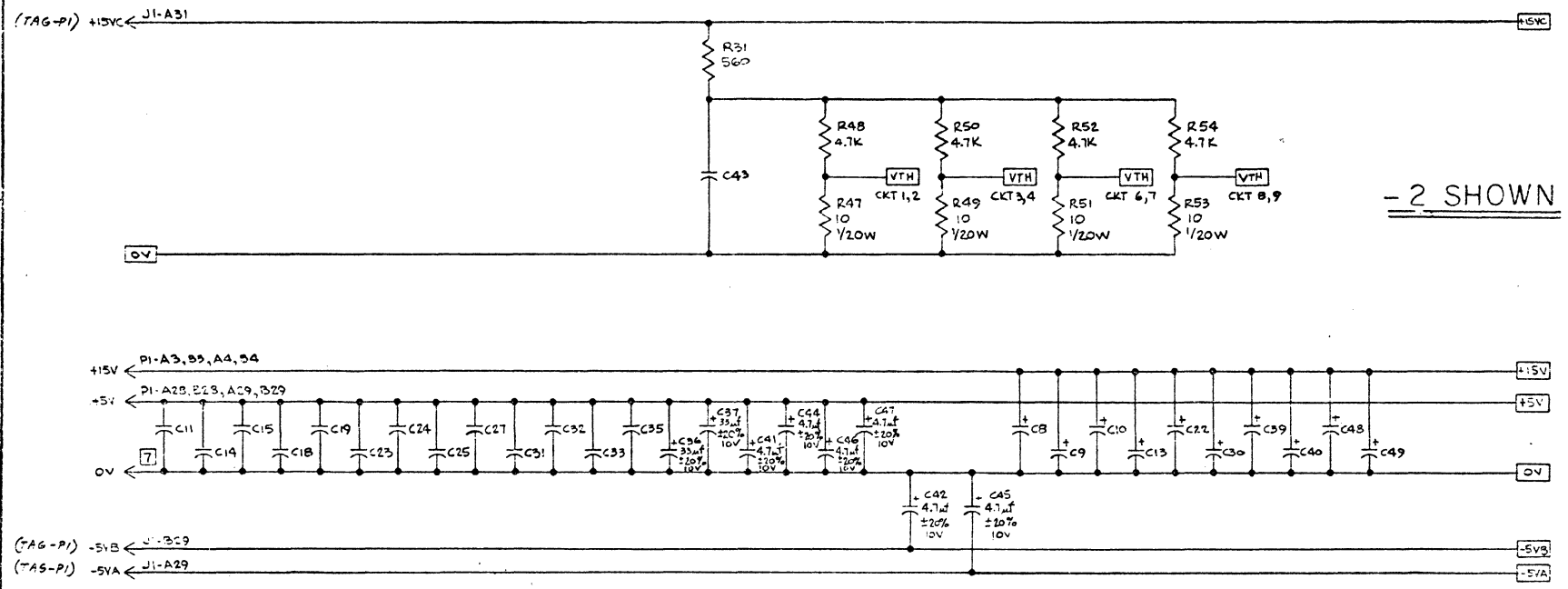
TAG

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INITIAL PRODUCTION RELEASE	12/21/72	

NOTES:

1. ALL RESISTORS ARE IN OHMS, ±2%, 1/4W.
2. ALL POLARIZED CAPACITORS ARE 15μf, ±20%, 20V.
3. ALL NON-POLARIZED CAPACITORS ARE 8001300101.
4. ALL DIODES ARE 8001100001.
5. ALL TRANSFORMERS ARE 8001400051.
6. ALL TRANSISTORS ARE MPQ3725.
7. 0V CONNECTOR PINS ARE: P1-A1, B1, A2, B2, A54, B54, A55, B55; J1-A1, B1, A6, B6, A9, B9, A12, B12, A15, B15, A36, B36, A39, B39, A42, B42, A45, B45, A48, B48, A54, B54.
8. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED. FOR COMPLETE PART NUMBERS SEE 8001800200.

PCDA-N ← P1-A25 — P1-B25 → PCDB-N
BT1A-N ← P1-A30 — P1-B30 → BT1B-N
BT2A-N ← P1-A31 — P1-B31 → BT2B-N
BT3A-N ← P1-A32 — P1-B32 → BT3B-N
BT4A-N ← P1-A33 — P1-B33 → BT4B-N



INTERPRET DRAWING PER MIL-D-1000, FORM 3, CATEGORY E

SEE ENGINEERING RECORDS

2001002155-2	SUE 3312
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ± 1/32 ANGLES ± 1/2°
DECIMALS: .XX = ± .03
.XXX = ± .010
MATERIAL:
SEE ATTACHED SHEET(S)

DATE	10-16-72
DR	Gleixner
CHK	12/21/72
ENGR	
PROJ ENGR	
APPD	12/21/72
APPD	

LOCKHEED ELECTRONICS COMPANY, INC.
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90040

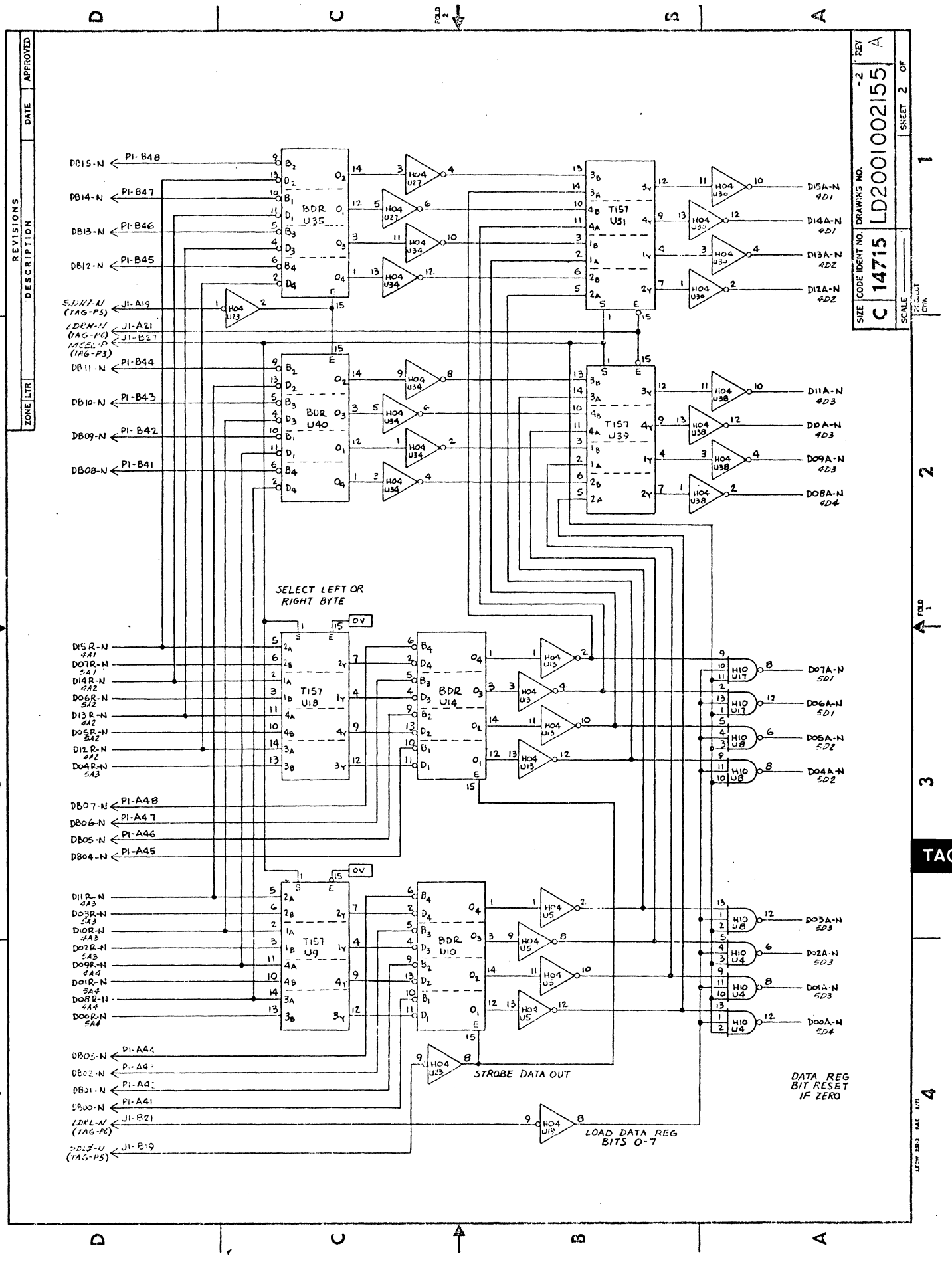
LOGIC DIAGRAM
SID
SENSE, INHIBIT DATA BOARD

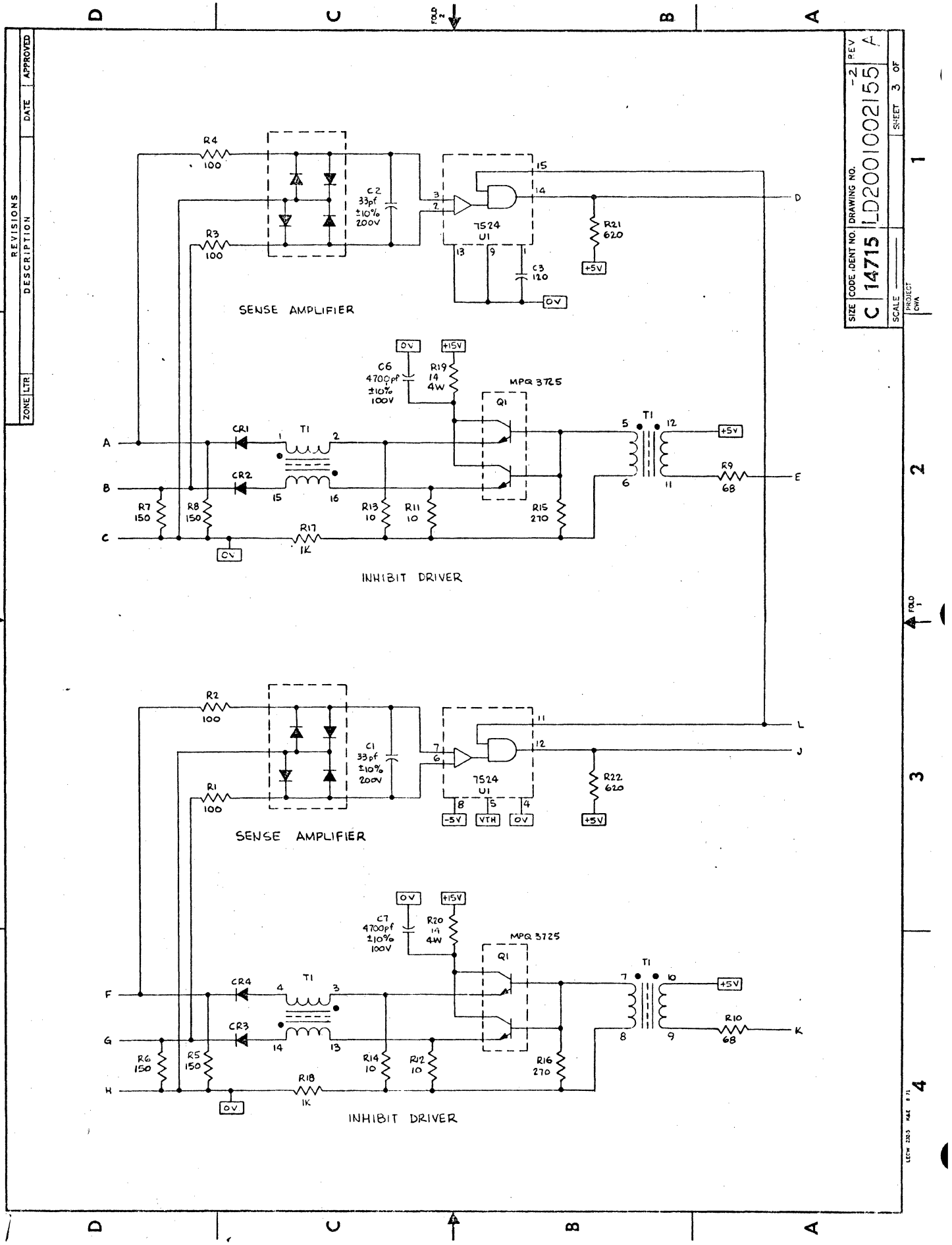
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	14715	LD2001002F-2	A

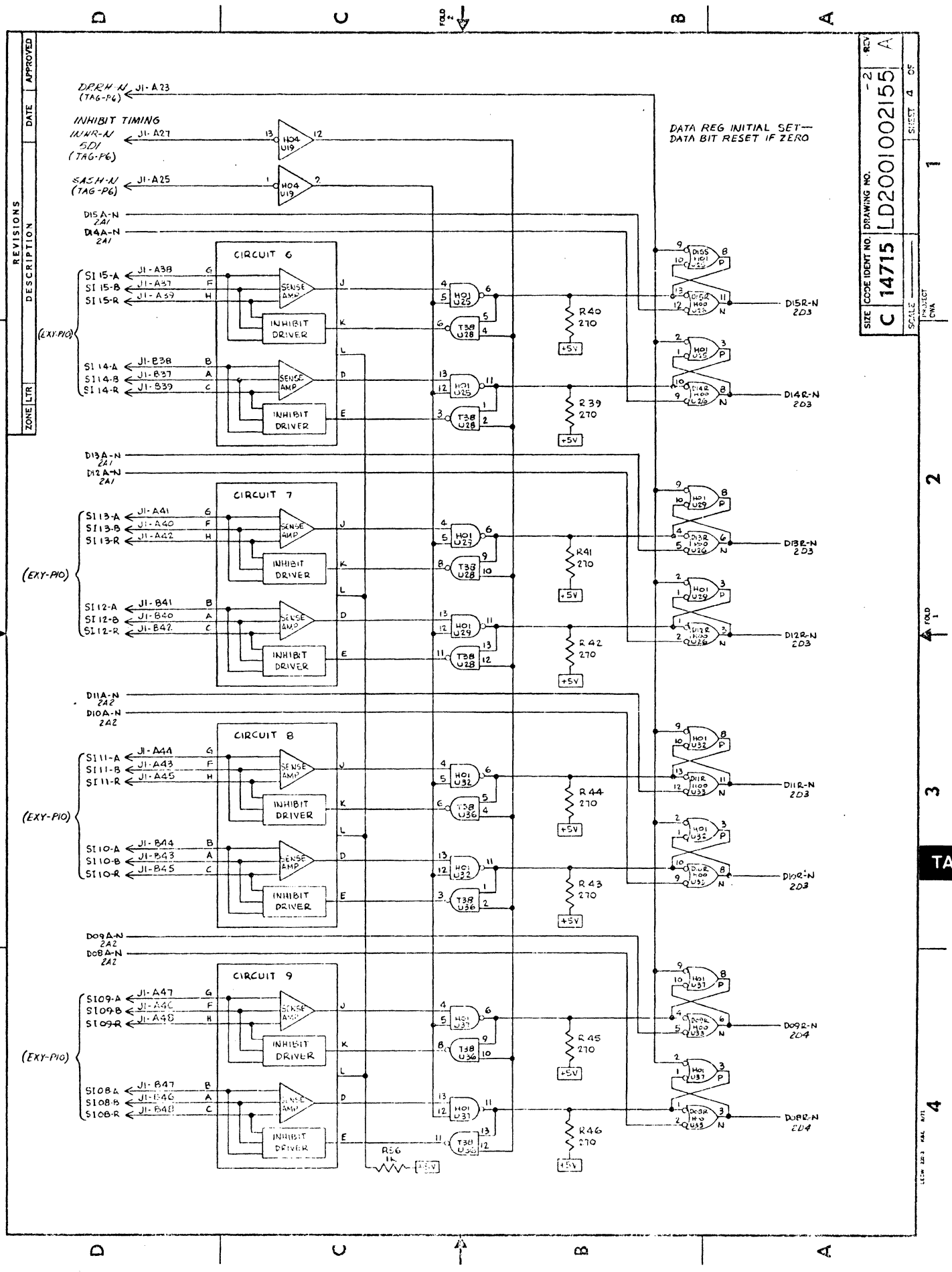
SCALE — SHEET 1 OF 5

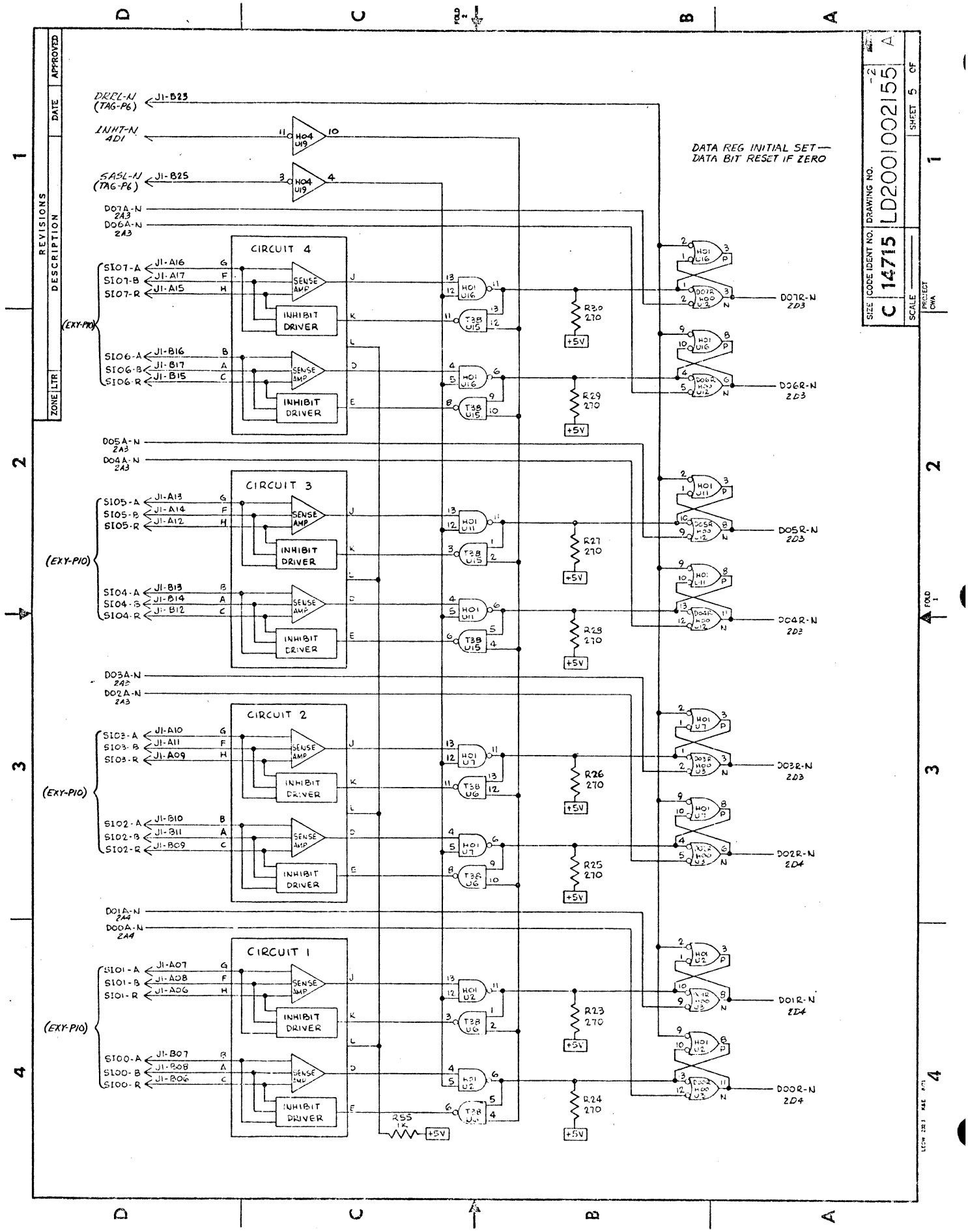
PROJECT CWA

FOLD 1 FOLD 2


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SIZE C | CODE IDENT NO. 14715 | DRAWING NO. LD2001002155-2 | REV A
SCALE | SHEET 2 OF
DB15-N PI-B48
DB14-N PI-B47
DB13-N PI-B46
DB12-N PI-B45
DB11-N PI-B44
DB10-N PI-B43
DB09-N PI-B42
DB08-N PI-B41
SDINT-N (TAG-P5) J1-A19
LDRM-N (TAG-P6) J1-A21
MCEL-P (TAG-P3) J1-B27
BDR U35
BDR U40
T157 U31
T157 U39
DI5A-N 4D1
DI4A-N 4D1
DI3A-N 4D2
DI2A-N 4D2
DI1A-N 4D3
DI0A-N 4D3
DO9A-N 4D3
DO8A-N 4D4
SELECT LEFT OR RIGHT BYTE
T157 U18
T157 U9
BDR U14
BDR U10
DI5R-N 4A1
DO7R-N 5A1
DI4R-N 4A2
DO6R-N 5A2
DI3R-N 4A2
DO5R-N 5A2
DI2R-N 4A2
DO4R-N 5A3
DI1R-N 4A3
DO3R-N 5A3
DI0R-N 4A3
DO2R-N 5A3
DO9R-N 4A4
DO1R-N 5A4
DO8R-N 4A4
DO0R-N 5A4
DB07-N PI-A48
DB06-N PI-A47
DB05-N PI-A46
DB04-N PI-A45
DB03-N PI-A44
DB02-N PI-A43
DB01-N PI-A42
DB00-N PI-A41
LDRL-N (TAG-P6) J1-B21
LDCK-N (TAG-P5) J1-B19
STROBE DATA OUT
LOAD DATA REG BITS 0-7
DATA REG BIT RESET IF ZERO
DO7A-N 5D1
DO6A-N 5D1
DO5A-N 5D2
DO4A-N 5D2
DO3A-N 5D3
DO2A-N 5D3
DO1A-N 5D3
DO0A-N 5D4
TAG


R4
100
R3
100
C2
33pf
±10%
200V
7524
U1
15
14
13
9
1
C3
120
R21
620
+5V
0V
D
SENSE AMPLIFIER
C6
4700pf
±10%
100V
R19
14
4W
+15V
MPQ 3725
Q1
T1
5
12
6
11
+5V
R9
68
E
A
B
C
CR1
CR2
1
2
15
16
R7
150
R8
150
R13
10
R11
10
R15
270
R17
1K
INHIBIT DRIVER
R2
100
R1
100
C1
33pf
±10%
200V
7
6
11
12
L
J
R22
620
-5V
VTH
8
5
4
SENSE AMPLIFIER
C7
4700pf
±10%
100V
R20
14
4W
F
G
H
CR4
CR3
4
3
14
13
R6
150
R5
150
R14
10
R12
10
R16
270
R18
1K
7
10
8
9
R10
68
K
INHIBIT DRIVER
REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
SIZE
C
CODE IDENT NO.
14715
DRAWING NO.
LD200100215 5-2
REV
A
SCALE
SHEET 3 OF
PROJECT
CMA
FOLD 2
FOLD 1


DRRH-N (TAG-P6) J1-A23
INHIBIT TIMING
INWR-N J1-A27
SDI (TAG-P6)
SASH-N (TAG-P6) J1-A25
DATA REG INITIAL SET— DATA BIT RESET IF ZERO
CIRCUIT 6
CIRCUIT 7
CIRCUIT 8
CIRCUIT 9
SENSE AMP
INHIBIT DRIVER
(EXY-PIO)
R40 270
R41 270
R42 270
R43 270
R44 270
R45 270
R46 270
R56 1K
+5V
DI5R-N ZD3
DI4R-N ZD3
DI3R-N ZD3
DI2R-N ZD3
DI1R-N ZD3
DI0R-N ZD3
D09R-N ZD4
D08R-N ZD4
REVISIONS
DESCRIPTION
DATE
APPROVED
ZONE LTR
SIZE C
CODE IDENT NO. 14715
DRAWING NO. LD2001002155 -2
REV A
SHEET 4 OF
TAG


DATA REG INITIAL SET—
DATA BIT RESET IF ZERO
CIRCUIT 4
CIRCUIT 3
CIRCUIT 2
CIRCUIT 1
SENSE AMP
INHIBIT DRIVER
(EXY-PIO)
DRCL-N (TAG-P6)
INIT-N 4D1
SASL-N (TAG-P6)
R30 270
R29 270
R27 270
R28 270
R26 270
R25 270
R23 270
R24 270
R55 1K
+5V
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SIZE C | CODE IDENT NO. 14715 | DRAWING NO. LD200100215 5 -2 A
SCALE | SHEET 5 OF
PROJECT CWA

JOB

PREPARED [illegible] DATE 9/15/7[illegible]
CHK DATE
LNGR DATE
PROJ ENGR DATE

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

B	14715	DL 2001002155-2	E
SIZE	CODE IDENT	SHEET 5	REV

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION VENDOR	MATL NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2001002155-2		SID-CKT CARD ASSY		USED ON SUE 3312	1
002	001	0001		1001004740-1		PRINTED WRG BD, SID			2
003	001	0001		RL07S561G		RESISTOR	MIL-R-22684/1	R31 .45 IS	3
004	032	0001		RL07S101G		RESISTOR	MIL-R-22684/1	1R1 THRU 4R1, 6R1 THRU 9R1, 1R2 THRU 4R2, 6R2 THRU 9R2, 1R3 THRU 4R3, 6R3 THRU 9R3, 1R4 THRU 4R4, 6R4 THRU 9R4 .45 IS	4
005	032	0001		RL07S151G		RESISTOR	MIL-R-22684/1	1R5 THRU 4R5, 6R5 THRU 9R5, 1R6 THRU 4R6, 6R6 THRU 9R6, 1R7 THRU 4R7, 6R7 THRU 9R7, 1R8 THRU 4R8, 6R8 THRU 9R8 .45 IS	5
006	018	0001		RL07S102G		RESISTOR	MIL-R-22684/1	1R17 THRU 4R17, 6R17 THRU 9R17, 1R18 THRU 4R18, 6R18 THRU 9R18, R55,56 .45 IS	6
007	032	0001		RL07S100G		RESISTOR	MIL-R-22684/1	1R11 THRU 4R11, 6R11 THRU 9R11, 1R12 THRU 4R12, 6R12 THRU 9R12, 1R13 THRU 4R13, 6R13 THRU 9R13, 1R14 THRU 4R14, 6R14 THRU 9R14 .45 IS	7
008	016	0001		RL07S680G		RESISTOR	MIL-R-22684/1	1R9 THRU 4R9, 6R9 THRU 9R9, 1R10 THRU 4R10, 6R10 THRU 9R10 .45 IS	8
009	032	0001		RL07S271G		RESISTOR	MIL-R-22684/1	1R15 THRU 4R15, 6R15 THRU 9R15, 1R16 THRU 4R16, 6R16 THRU 9R16, R23 THRU R30, R39 THRU R46 .45 IS	9
010	005	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R32,48,50,52,54 .45 IS	10
011	005	0001		RN50C10R0F		RESISTOR	MIL-R-55182	R34,47,49,51,53 .35 IS	11
012	000								12
013	016	0001		NLS-2 14 OHMS	91637	RESISTOR	DALE ELEC INC	1R19 THRU 4R19, 6R19 THRU 9R19, 1R20 THRU 4R20, 6R20 THRU 9R20 .675 IS	13
014	016	0001		RL07S621G		RESISTOR	MIL-R-22684/1	1R21 THRU 4R21, 6R21 THRU 9R21, 1R22 THRU 4R22, 6R22 THRU 9R22 .50 IS	14

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL	E — SOURCE CONTROL DWG	ICP — INTEGRATED CIRCUIT PKG	FOR REV RECORD SEE SHEET 1
B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO	F — SPEC CONTROL DWG	I.S — INSERTION SPAN	
C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	M — DENOTES MAKE FROM	A/R — AS REQD	
	& — ALTERNATE SOURCE		

LECW 234 (JAN 70) K&E

TAG

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
015	E	032	0001		8001100001-1		DIODE		1CR1 THRU 4CR1, 6CR1 THRU 9CR1, 1CR2 THRU 4CR2, 6CR2 THRU 9CR2, 1CR3 THRU 4CR3, 6CR3 THRU 9CR3, 1CR4 THRU 4CR4, 6CR4 THRU 9CR4 .45 IS	15
016	E	008	0001		8001400051-1		TRANSFORMER		1T1 THRU 4T1, 6T1 THRU 9T1	16
017		008	0001		MP03725	04713	TRANSISTOR	MOTOROLA	1Q1 THRU 4Q1, 6Q1 THRU 9Q1	17
018	F	016	0001		8001300006-1		CAPACITOR		1C1 THRU 4C1, 6C1 THRU 9C1, 1C2 THRU 4C2, 6C2 THRU 9C2 .10 IS	18
019		006	0001		M39003/01-2015		CAPACITOR	MIL-C-39003/1	C42,45,41,44,46, 47 .65 IS	19
020	F	016	0001		8001300101-1		CAPACITOR		C11,14,15,16,18, 19,23,24,25,27, 28,31,32,33,43, 35 .25 IS	20
021	F	016	0001		8001300019-1		CAPACITOR		1C6 THRU 4C6, 6C6 THRU 9C6, 1C7 THRU 4C7, 6C7 THRU 9C7 .20 IS	21
022		003	0001		M39003/01-2018		CAPACITOR	MIL-C-39003/1	C36,37,38 .80 IS	22
023		010	0001		M39003/01-2050		CAPACITOR	MIL-C-39003/1	C8,9,10,13,22, 30,40,48,49,39 .80 IS	23
024		000								24
025		008	0001		CK05BX121K		CAPACITOR	MIL-C-11015	1C3 THRU 4C3, 6C3 THRU 9C3	25
026	F	004	0001		8001800042-1		ICP		U3,12,26,33 (74H00)	26
027	F	008	0001		8001800043-1		ICP		U2,7,11,16,25, 29,32,37 (74H01)	27
028	F	008	0001		8001800044-1		ICP		U5,13,19,23,27, 30,34,38 (74H04)	28
029	F	003	0001		8001800046-1		ICP		U4,8,17 (74H10)	29
030	F	004	0001		8001800120-1		ICP		U10,14,35,40 (BDR)	30
031	F	004	0001		8001803140-1		ICP		U6,15,28,36 (7438)	31
032		000								32
033	F	004	0001		8001803169-1		ICP		U9,18,31,39 (79157)	33
034		008	0001		SN7524N	01295	ICP	TEXAS INSTR INC	1U1 THRU 4U1, 6U1 THRU 9U1	34
035		000								35
036		000								36
037		004	0001		1001005125-2		DIODE, CLUST, COM CATH		Z2,4,8,10	37
038		000								38
039		004	0001		1001005126-2		DIODE, CLUST, COM ANOD		Z1,3,7,9	39

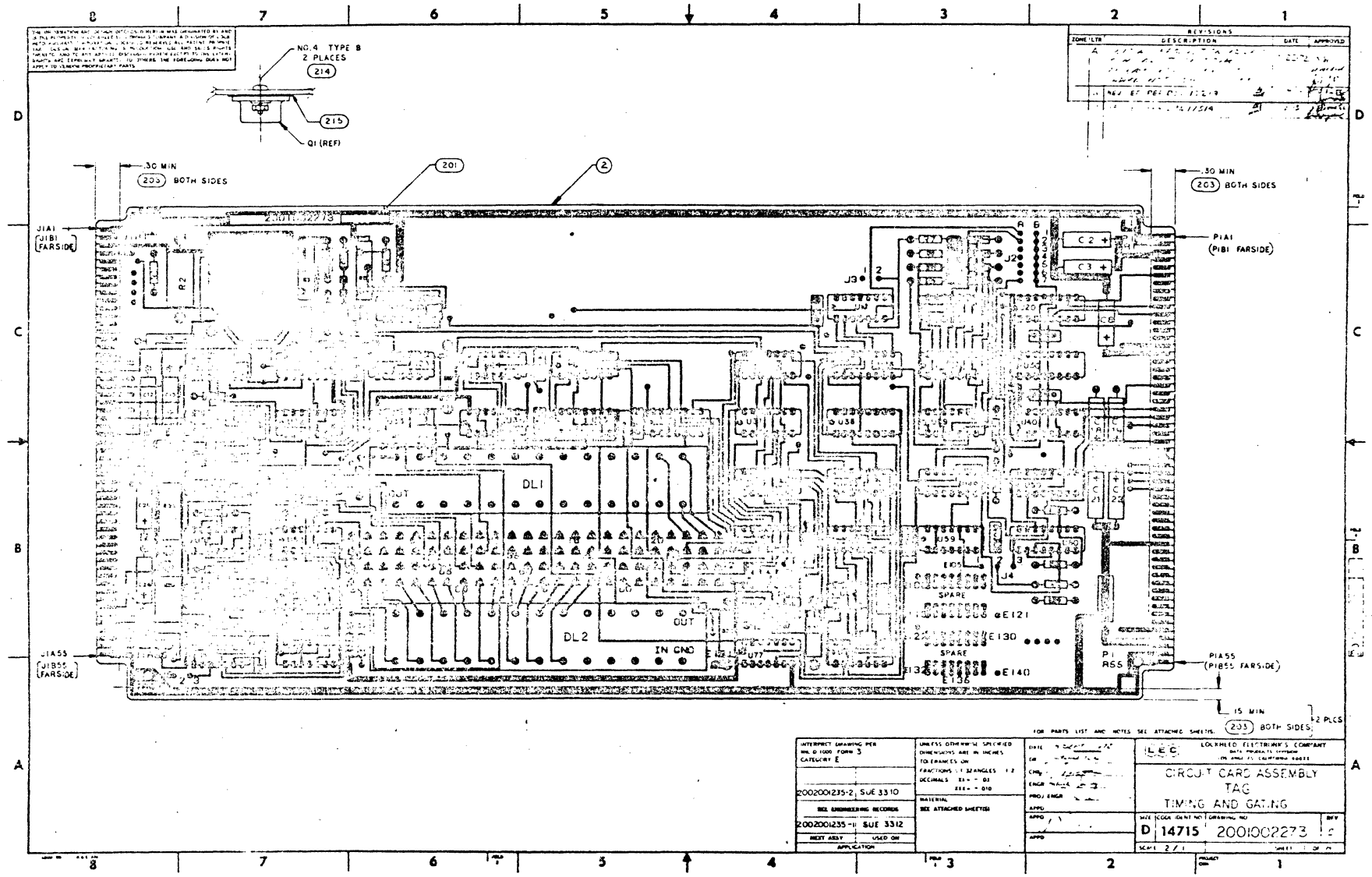
CONFORMS TO MIL-STD-100

				LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022	B	14715	PL 2001002155		F
					SIZE	CODE IDENT	SHEET 11		REV

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200		REF	0001		SPEC/DWG/STD		NOTE:			200
201		A/R	0001		LECP1049-17		MARK DASH NUMBER, REVISION LETTER AND SERIALIZE USING A FOUR DIGIT NUMBER STARTING WITH 0001 PRECEDED BY M (M0001).			201
202		REF	0001				AREA TO BE FREE OF SOLDER.			202
203		REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010/INCH IN GENERAL AREA AND .005/INCH IN CONNECTOR AREA.			203
204		REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NUMBER ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205		REF	0001				MAXIMUM COMPONENT HEIGHT (SIDE 1) .395 MAXIMUM.			205
206		REF	0001				PROTRUSION (SIDE 2) .075 MAXIMUM.			206
207		REF	0001				SQUARE PAD AND/OR STRIPE DENOTES CATHODE END OF DIODE.			207
208		REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			208
209		REF	0001				SQUARE PAD AND/OR DOT DENTOES PIN 1 OF ICP.			209

CONFORMS TO MIL-STD-100

TAG



REVISIONS			
ZONE/LTR	DESCRIPTION	DATE	APPROVED
A			

INTERPRET DRAWING PER MIL-D-1000 FORM 3
CATEGORY E

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON
FRACTIONS ± 1/2 ANGLES ± 2
DECIMALS .XX ± .03
.XXX ± .010

MATERIAL
SEE ATTACHED SHEET(S)

SEE ENGINEERING RECORDS	
2002001235-2	SUE 3310
2002001235-1	SUE 3312

NEXT ASSY	USED ON
APPLICATION	

DATE
DR
CHK
ENGR
PROJ ENGR
APPD
APPD
APPD

ILLEC. LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS SYSTEMS
PLAINFIELD, NEW JERSEY AND LOS ANGELES, CALIFORNIA 90022

CIRCUIT CARD ASSEMBLY TAG TIMING AND GATING

SIZE	CODE IDENT NO	DRAWING NO	REV
D	14715	2001002273	E

SCALE 2/1 SHEET 1 OF 1

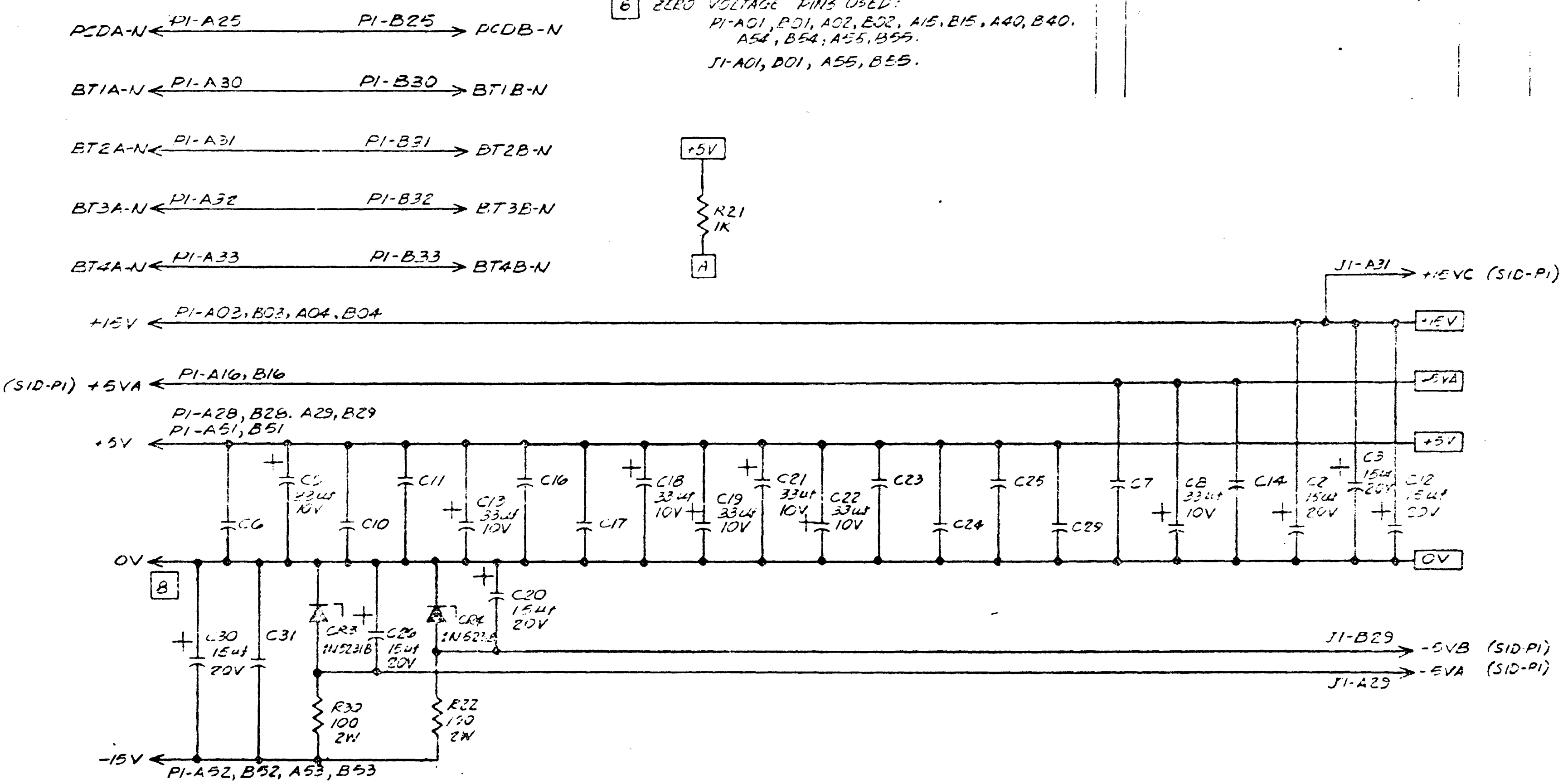
REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INITIAL PRODUCTION RELEASE, SAME AS PROTOTYPE REV C	12/20/72	
	B	REVISED PER DCN 17606	3/7/73	

NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS 1/4 W, ±2%.
2. ALL NONPOLARIZED CAPACITORS ARE .1µf, 50V, +80%-20%
3. ALL POLARIZED CAPACITORS ARE 33 µf, 10V, ±20%.
4. ▭ DENOTES COMMON VOLTAGE TO ALL CKTS.
5. ← DENOTES CONNECTOR INPUT/OUTPUT PIN NO.
6. ▭ DENOTES COMMON SIGNAL.
7. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED FOR COMPLETE PART NUMBERS SEE SCS 8002000.

[6] ZERO VOLTAGE PINS USED:
P1-A01, B01, A02, B02, A15, B15, A40, B40, A54, B54, A55, B55.
J1-A01, B01, A55, B55.



FOR PARTS LIST AND NOTES SEE ATTACHED SHEET(S)

-1 SHOWN

INTERPRET DRAWING PER MIL-D-1000, FORM 3 CATEGORY E	
SEE ENGINEERING RECORDS	
2001002273-1	SUE 3312
NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ± 1/32 ANGLES ± 1/2°
DECIMALS .XX = ± .03
.XXX = ± .010
MATERIAL:
SEE ATTACHED SHEET(S)

DATE 10-16-72
DR
CHK 10/23/72
ENGR
PROJ ENGR
APPD
APPD
APPD

LOCKHEED ELECTRONICS COMPANY, INC.
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90040

LOGIC DIAGRAM TAG TIMING AND GATING

SIZE	CODE IDENT NO	DRAWING NO.	REV
C	14715	LD2001002273	B

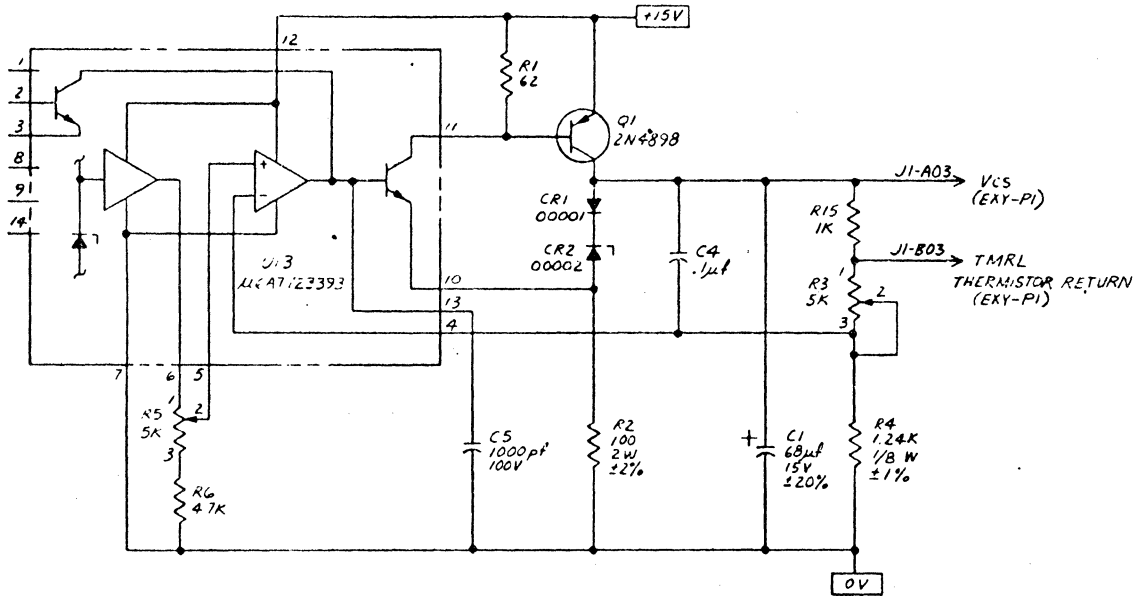
SCALE — SHEET 1 OF 5

TAG

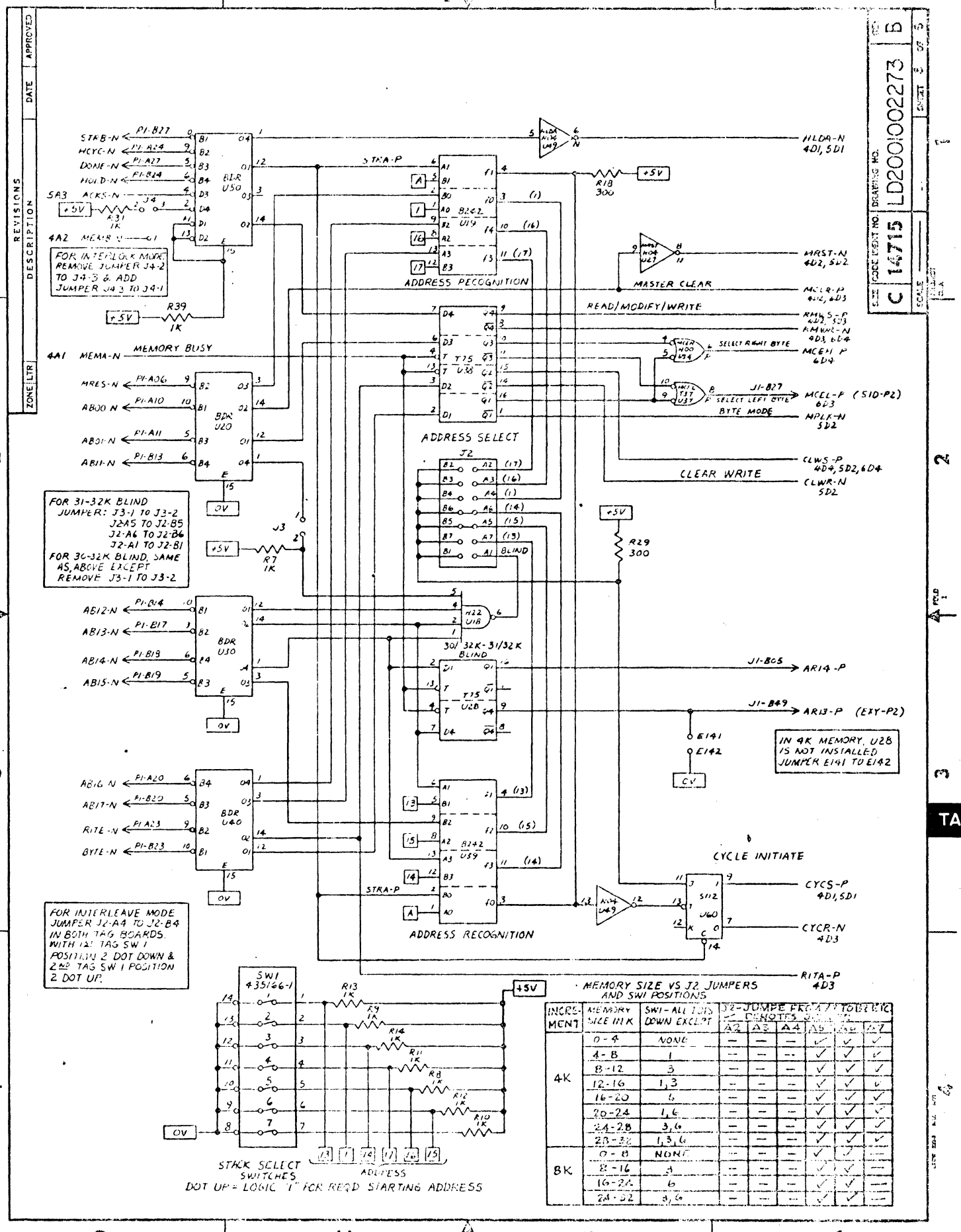
REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	14715	LD2001002273	B

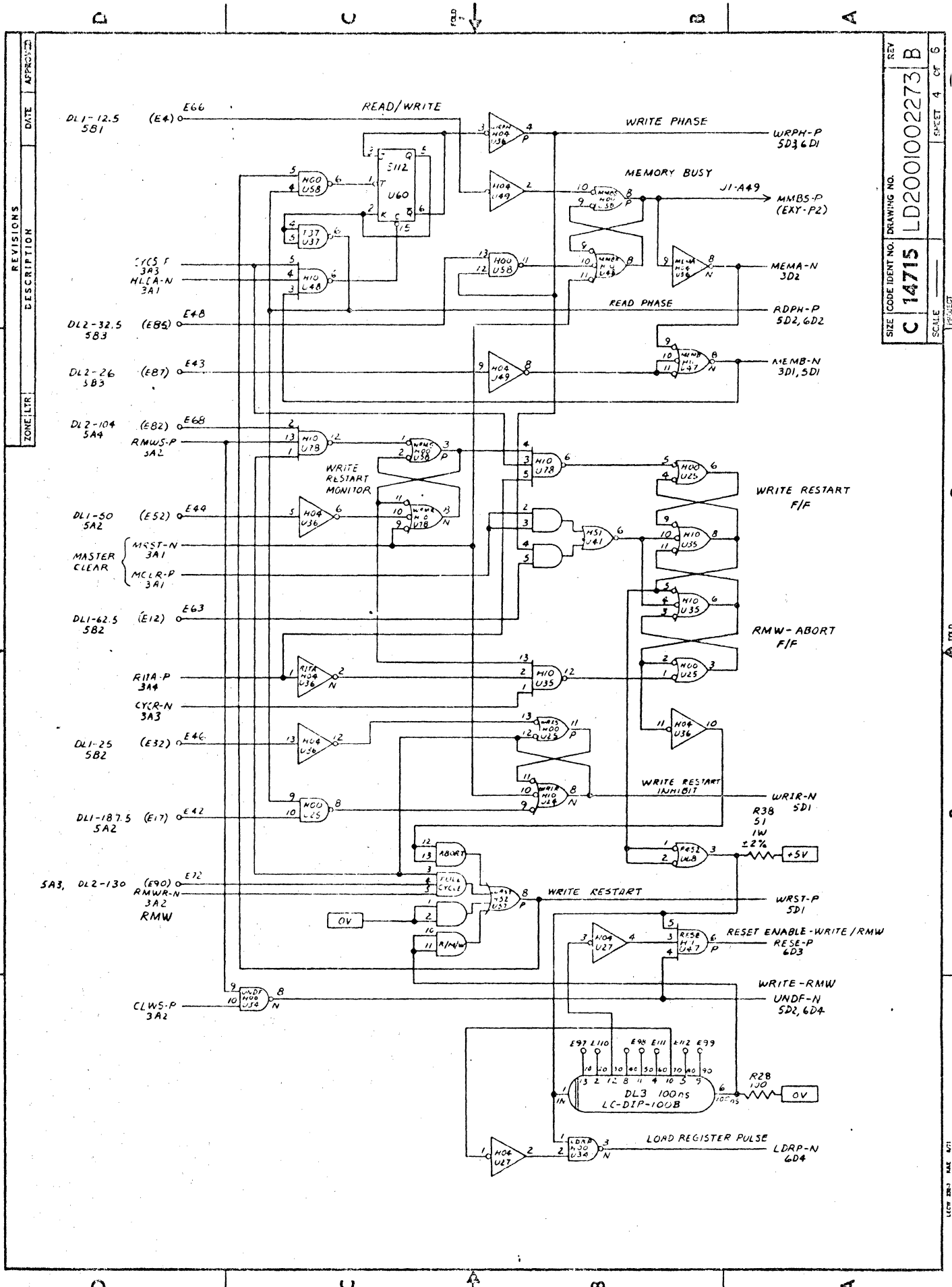
SCALE —— SHEET 2 OF 5



CURRENT SOURCE VOLTAGE REGULATOR


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
SIZE C | CODE IDENT NO. 14715 | DRAWING NO. LD200100273 | REV B | SHEET 3 OF 5
SCALE —
STAB-N
MCYC-N
DONE-N
HOLD-N
ACKS-N
MEMB-N
FOR INTERLOCK MODE REMOVE JUMPER J4-2 TO J4-3 & ADD JUMPER J4-3 TO J4-1
+5V
R39 1K
MEMORY BUSY
MEMA-N
MRES-N
ABOO-N
AB01-N
AB11-N
BDR U20
BDR U30
BDR U40
FOR 31-32K BLIND JUMPER: J3-1 TO J3-2 J2-A5 TO J2-B5 J2-A6 TO J2-B6 J2-A1 TO J2-B1
FOR 30-32K BLIND, SAME AS ABOVE EXCEPT REMOVE J3-1 TO J3-2
R7 1K
AB12-N
AB13-N
AB14-N
AB15-N
AB16-N
AB17-N
RITE-N
BYTE-N
FOR INTERLEAVE MODE JUMPER J2-A4 TO J2-B4 IN BOTH TAG BOARDS. WITH 1ST TAG SW 1 POSITION 2 DOT DOWN & 2ND TAG SW 1 POSITION 2 DOT UP.
STRA-P
ADDRESS RECOGNITION
ADDRESS SELECT
MASTER CLEAR
READ/MODIFY/WRITE
MEMORY BUSY
SELECT RIGHT BYTE
SELECT LEFT BYTE
BYTE MODE
CLEAR WRITE
30/32K-31/32K BLIND
CYCLE INITIATE
IN 4K MEMORY, U28 IS NOT INSTALLED JUMPER E141 TO E142
HLDA-N 4D1, 5D1
MRST-N 4D2, 5D2
MCLR-P 4D2, 6D3
RMWR-P 4D2, 5D3
RMWR-N 4D3, 6D4
MCEH-P 6D4
MCEL-P (5ID-P2) 6D3
MPLR-N 5D2
CLWS-P 4D4, 5D2, 6D4
CLWR-N 5D2
AR14-P
AR13-P (EXY-P2)
CYCS-P 4D1, 5D1
CYCR-N 4D3
RITA-P 4D3
R18 300
R29 300
SW1 435166-1
R13 1K
R9 1K
R14 1K
R11 1K
R8 1K
R12 1K
R10 1K
STACK SELECT SWITCHES DOT UP = LOGIC "1" FOR REQ'D STARTING ADDRESS
MEMORY SIZE VS J2 JUMPERS AND SW1 POSITIONS
INCREMENT | MEMORY SIZE IN K | SW1 - ALL TOTS DOWN EXCEPT | J2 JUMPERS FROM A7 TO B1 (✓ DENOTES JUMPER)
4K: 0-4 NONE; 4-8 1; 8-12 3; 12-16 1,3; 16-20 6; 20-24 1,6; 24-28 3,6; 28-32 1,3,6
8K: 0-8 NONE; 8-16 3; 16-24 6; 24-32 3,6

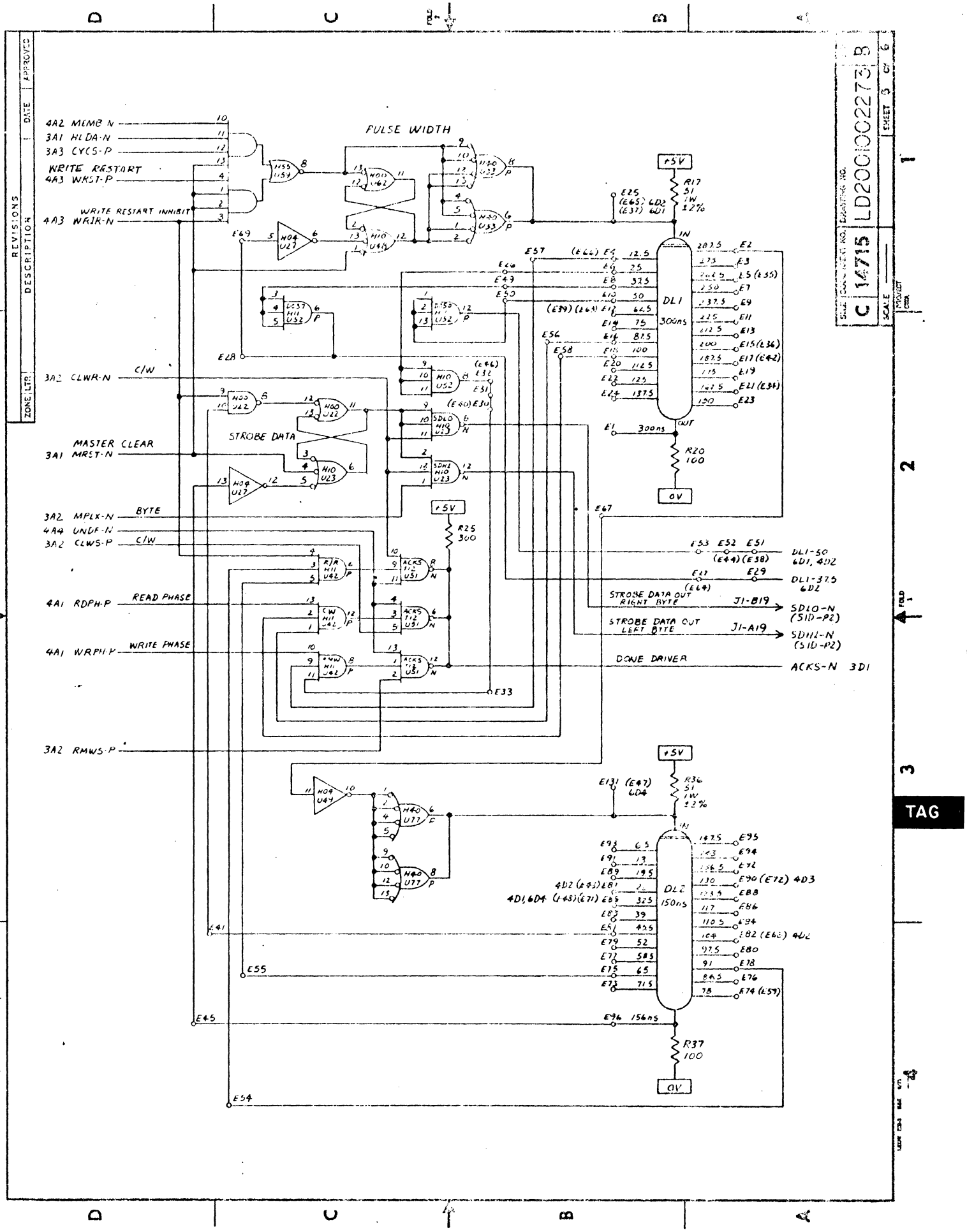
TAG

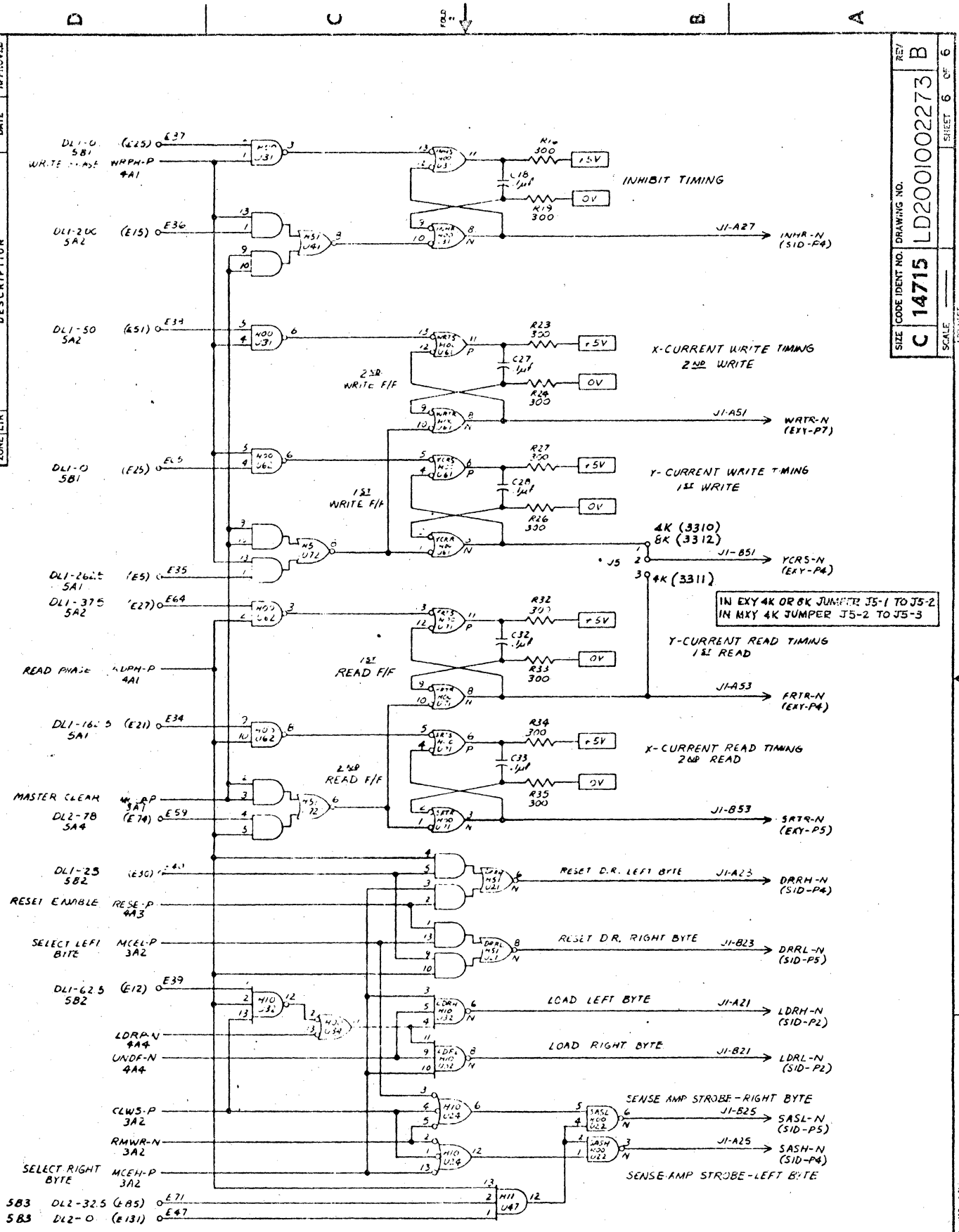


REVISIONS | ZONE | LTR | DESCRIPTION | DATE | APPROVED

SIZE	CODE IDENT NO.	DRAWING NO.	REV
C	14715	LD2001002273	B

SCALE — SHEET 4 OF 6


PULSE WIDTH
WRITE RESTART
WRITE RESTART INHIBIT
MASTER CLEAR
STROBE DATA
BYTE
READ PHASE
WRITE PHASE
C/W
4A2 MEMB N
3A1 HLDA-N
3A3 CYCS-P
4A3 WRST-P
4A3 WRIR-N
3A2 CLWR-N
3A1 MRST-N
3A2 MPLX-N
4A4 UNDF-N
3A2 CLWS-P
4A1 RDPH-P
4A1 WRPH-P
3A2 RMWS-P
+5V
R17 51 1W 1%
R20 100
R25 300
R36 51 1W 1%
R37 100
DL1
30ons
DL2
150ns
0V
IN
OUT
DLI-50 6D1, 4D2
DLI-37.5 6D2
STROBE DATA OUT RIGHT BYTE
J1-B19
SDLO-N (SID-P2)
STROBE DATA OUT LEFT BYTE
J1-A19
SDHI-N (SID-P2)
DONE DRIVER
ACKS-N 3D1
REVISIONS
ZONE/LTR
DESCRIPTION
DATE
APPROVED
C 1715
LD20C0C2273 B
SHEET 3 OF 6
SCALE
TAG


INHIBIT TIMING
X-CURRENT WRITE TIMING 2ND WRITE
Y-CURRENT WRITE TIMING 1ST WRITE
Y-CURRENT READ TIMING 1ST READ
X-CURRENT READ TIMING 2ND READ
IN EXY 4K OR 8K JUMPER J5-1 TO J5-2
IN MXY 4K JUMPER J5-2 TO J5-3
RESET D.R. LEFT BYTE
RESET D.R. RIGHT BYTE
LOAD LEFT BYTE
LOAD RIGHT BYTE
SENSE AMP STROBE-RIGHT BYTE
SENSE AMP STROBE-LEFT BYTE
INHR-N (SID-P4)
WRTR-N (EXY-P7)
YCRS-N (EXY-P4)
YRTR-N (EXY-P4)
XRTR-N (EXY-P5)
DRRH-N (SID-P4)
DRRL-N (SID-P5)
LDRH-N (SID-P2)
LDRL-N (SID-P2)
SASL-N (SID-P5)
SASH-N (SID-P4)

JNH

PREPARED E. SOUZA DATE 1/23/73
CHK [illegible] DATE 1/23/73
ENGR [illegible] DATE [illegible]
PROJ ENGR [illegible] DATE [illegible]

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

B	14715	PL 2001002273-1	C
SIZE	CODE IDENT	SHEET 2	REV

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2001002273-1		TAG-CKT CARD ASSY		USED ON SUE 3312	1
002	001	0001		1001005140-1		PRINTED WRG BD, TAG			2
003	000								3
004 F	104	0001		1005000764-1		PIN, TERMINAL		NOTE 211	4
005 F	001	0001		8001600001-1		DELAY LINE		DL1	5
006 F	001	0001		8001600004-1		DELAY LINE		DL2	6
007	001	0001		LC-DIP-100B	19615	DELAY LINE	ALLEN AVIONICS	DL3	7
008	000								8
009	001	0001		435166-1	00779	SWITCH, 7 TOGGLE	AMP, INC	SW1	9
010	000								10
011 E	001	0001		8001100001-1		DIODE		CR1 .5 IS	11
012 E	001	0001		8001100002-1		DIODE, ZENER		CR2 .5 IS	12
013	002	0001		1N52318		DIODE, ZENER		CR3,4 .5 IS	13
014	000								14
015	001	0001		2N4898		TRANSISTOR		Q1 (TO-66)	15
016	000								16
017 F	008	0001		8001800042-1		ICP		U22,25,31,34,58, 61,62,71 (74H00)	17
018 F	003	0001		8001800044-1		ICP		U27,36,49 (74H04)	18
019 F	006	0001		8001800046-1		ICP		U23,24,32,35,48, 78 (74H10)	19
020 F	003	0001		8001800047-1		ICP		U42,47,52 (74H11)	20
021	000								21
022 F	001	0001		8001800050-1		ICP		U18 (74H22)	22
023 F	002	0001		8001800052-1		ICP		U33,77 (74H40)	23
024 F	003	0001		8001800054-1		ICP		U21,41,72 (74H51)	24
025 F	001	0001		8001800055-1		ICP		U57 (74H52)	25
026	000								26
027 F	001	0001		8001800058-1		ICP		U59 (74H55)	27
028 F	002	0001		8001800100-1		ICP		U28,38 (7475)	28
029 F	004	0001		8001800120-1		ICP		U20,30,40,50 (BDR)	29
030	000								30
031	000								31
032 F	001	0001		8001803139-1		ICP		U37 (7437)	32
033 F	001	0001		8001803128-1		ICP		U51 (7412)	33
034 F	001	0001		8001803203-1		ICP		U60 (74S112)	34
035	001	0001		U6A7723393	07263	ICP	FAIRCHILD	U13	35
036	002	0001		N8242A	18324	ICP	SIGNETICS	U19,39	36

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES

A — DENOTES SEPARATE PL
B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO
C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS
E — SOURCE CONTROL DWG
F — SPEC CONTROL DWG
M — DENOTES MAKE FROM
& — ALTERNATE SOURCE

DEFINITIONS

ICP — INTEGRATED CIRCUIT PKG
IS — INSERTION SPAN
A/R — AS REQD

REVISIONS

FOR REV RECORD SEE SHEET 1

LECW 239 (JAN 70) K&E

TAG

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	PL	REV
B	14715	LD2001002273-1	C

SHEET 3

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL NOTE(S) REF DESIGNATION(S)	FIND NO.
037		001	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U68	37
038		000								38
039	F	018	0001		80013C0010I-1		CAPACITOR		C4,6,7,10,11,14, 15,16,17,23,24, 25,27,28,29,31, 32,33 .25 IS	39
040	F	001	0001		80013C0015-1		CAPACITOR		C5 .1 IS	40
041		007	0001		M39003/01-2018		CAPACITOR	MIL-C-39003/1	C8,9,13,18,19, 21,22 .8 IS	41
042		006	0001		M39003/01-2050		CAPACITOR	MIL-C-39003/1	C2,3,12,20,26, 30 .8 IS	42
043		001	0001		M39003/01-2035		CAPACITOR	MIL-C-39003/1	C1 1.1 IS	43
044		000								44
045		000								45
046		000								46
047		013	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R16,19,23,24,25, 26,27,32,33,34, 35,18,29 .5 IS	47
048		012	0001		RL07S102G		RESISTOR	MIL-R-22684/1	R7,8,9,10,11,12, 13,14,15,21,31, 39 .5 IS	48
049		001	0001		RL07S620G		RESISTOR	MIL-R-22684/1	R1 .5 IS	49
050		001	0001		RL07S472G		RESISTOR	MIL-R-22684/1	R6 .5 IS	50
051		003	0001		RL07S101G		RESISTOR	MIL-R-22684/1	R20,28,37 .5 IS	51
052		003	0001		RL32S510G		RESISTOR	MIL-R-22684/3	R17,36,38 .8 IS	52
053		003	0001		RL42S101G		RESISTOR	MIL-R-22684/4	R2,22,30 1.0 IS	53
054		001	0001		RN55D1241F		RESISTOR	MIL-R-10509/7	R4 .5 IS	54
055		000								55
056		002	0001		3007P-1-502	80294	RESISTOR,VARIABLE	BOURNS, INC	R3,5	56
057		000								57
058		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		58
059	F	010	0001		9003400417-10		WIRE, SOLID		30AWG WHT APPROX FT REQD	59
060	F	001	0001		9003400419-4		WIRE, SOLID		28AWG APPROX FT REQD	60
061		REF	0001		LD2001002273-1		LOGIC DIAGRAM			61

CONFORMS TO MIL-STD-100

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	SHEET	REV
B	14715	PL 2001002273-1	C

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL NOTE(S) REF DESIGNATION(S)	FIND NO.

WIRE LIST

FROM	TO	COLOR	FIND NO.
E87	E43	WHT	59
E90	E72	WHT	59
E28	E69	WHT	59
E2	E67	WHT	59
E32	E46	WHT	59
E17	E42	WHT	59
E12	E63	WHT	59
E82	E68	WHT	59
E52	E44	WHT	59
E16	E56	WHT	59
E18	E58	WHT	59
E31	E33	WHT	59
E4	E57	WHT	59
E78	E54	WHT	59
E75	E55	WHT	59
E81	E41	WHT	59
E96	E45	WHT	59
E131	E47	WHT	59
E85	E71	WHT	59
E12	E39	WHT	59
E30	E40	WHT	59
E27	E64	WHT	59
E21	E34	WHT	59
E74	E59	WHT	59
E25	E65	WHT	59
E51	E38	WHT	59
E5	E35	WHT	59
E25	E37	WHT	59
E15	E36	WHT	59
E4	E66	WHT	59
E85	E48	WHT	59
E6	E26	WHT	59
E8	E49	WHT	59
E10	E50	WHT	59
J2-A6	J2-B6	WHT	60
J2-A5	J2-B5	WHT	60
J4-2	J4-3	WHT	60
J5-1	J5-2	WHT	60

CONFORMS TO MIL-STD-100

TAG

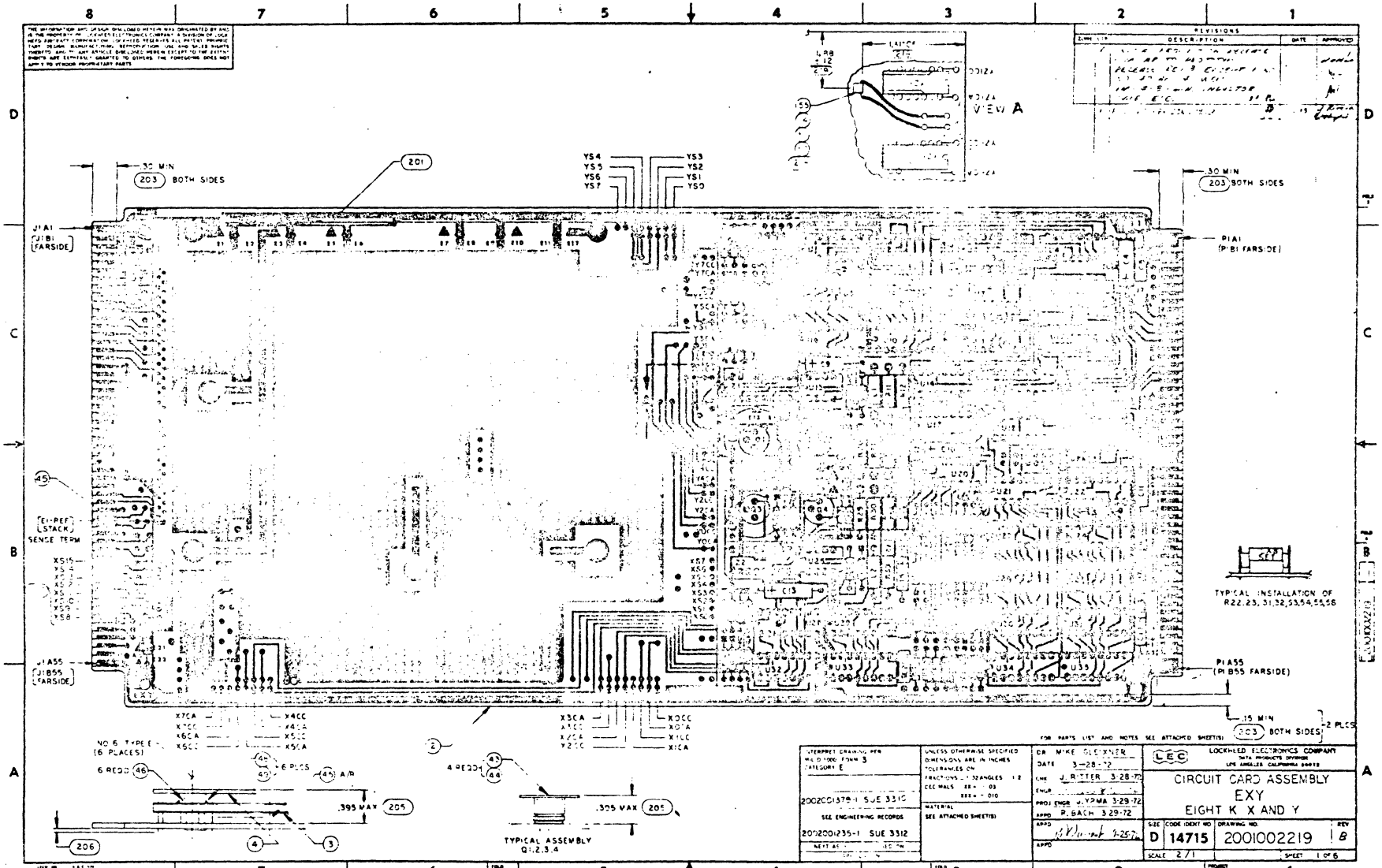
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT		REV
B	14715	PL 2001002273	C

SHEET 8

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
200	REF	0001		SPEC/DWG/STD		NOTES:			200
201	A/R	0001		LECP1049-17		MARKING (IDENTIFY).			201
202	REF	0001		LECP1080		CLEANING.			202
203	REF	0001				AREA TO BE FREE OF SOLDER.			203
204	REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205	REF	0001				COMPONENT HEIGHT.395 MAX.			205
206	REF	0001				PROTRUSION SIDE 2, .075 MAX., LEADS TO BE VISIBLE THRU SOLDER.			206
207	REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010 INCH/INCH IN GENERAL AREA AND .005 INCH/INCH IN CONNECTOR AREA.			207
208	REF	0001				SQUARE PAD DENOTES CATHODE END (STRIPE) OF DIODE, OR POSITIVE (+) END OF CAPACITOR.			208
209	REF	0001				RECTANGULAR PAD AND DOT OR SLOTTED END OF ICP DENOTES PIN 1.			209
210	REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			210
211	REF	0001				TRIANGLE SYMBOL DENOTES TERMINAL PIN LOCATION.			211
212	000								212
213	000								213
214	A/R	0001		LECP1075		HARDWARE.			214
215	A/R	0001				INSTALL MICA WASHER UNDER Q1 AS SUPPLIED WITH FIND NO. 15.			215

CONFORMS TO MIL-STD-100


REVISIONS
DESCRIPTION
DATE
APPROVED
VIEW A
30 MIN
203 BOTH SIDES
201
J1A1
(J1B1 FARSIDE)
P1A1
(P1B1 FARSIDE)
P1A55
(P1B55 FARSIDE)
J1A55
(J1B55 FARSIDE)
YS4
YS5
YS6
YS7
YS3
YS2
YS1
YS0
TYPICAL INSTALLATION OF
R22,23,31,32,53,54,55,56
.15 MIN
203 BOTH SIDES
2 PLCS
NO.6 TYPE E
(6 PLACES)
6 REQD
46
6 PLCS
45 A/B
.395 MAX
205
206
4
3
4 REQD
45
44
.305 MAX
205
TYPICAL ASSEMBLY
Q1,2,3,4
DR MIKE GLEICHER
DATE 3-28-72
LDS J. RITTER 3-28-72
ENGR
PROJ ENGR J. YAMA 3-29-72
APPD P. BACH 3-29-72
APPD
APPD
CIRCUIT CARD ASSEMBLY
EXY
EIGHT K X AND Y
LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90053
SIZE D
CODE IDENT NO 14715
DRAWING NO 2001002219
REV B
SCALE 2/1
SHEET 1 OF 6
2002001379-1 SUE 3310
2002001235-1 SUE 3312
SEE ENGINEERING RECORDS

TAG

NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS 1/4W, ±2%
2. ALL NON-POLARIZED CAPACITORS ARE 8001300101.
3. ALL DIODES ARE 8001100001.
4. ALL TRANSISTORS ARE 8001200016.
5. ▭ DENOTES COMMON VOLTAGE TO ALL CKTS.
6. ← DENOTES CONNECTOR INPUT/OUTPUT PIN NO.
7. ☐ DENOTES COMMON SIGNAL.
8. INTEGRATED CIRCUIT PACKAGE TYPE DESIGNATIONS ARE ABBREVIATED FOR COMPLETE PART NUMBERS SEE 8001B00200.

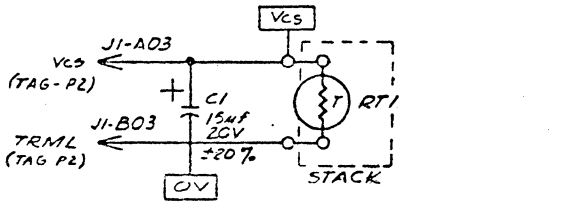
[5] R53 & R55 ARE TRIM RESISTORS (LAB SET)

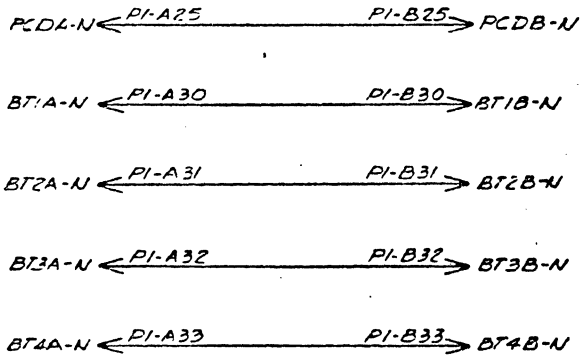
[6] R54 & R56 VALUES MAY BE CHANGED AT TEST LEVEL.

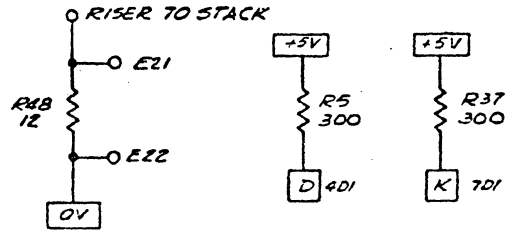
[7] ZERO VOLTAGE PINS USED:

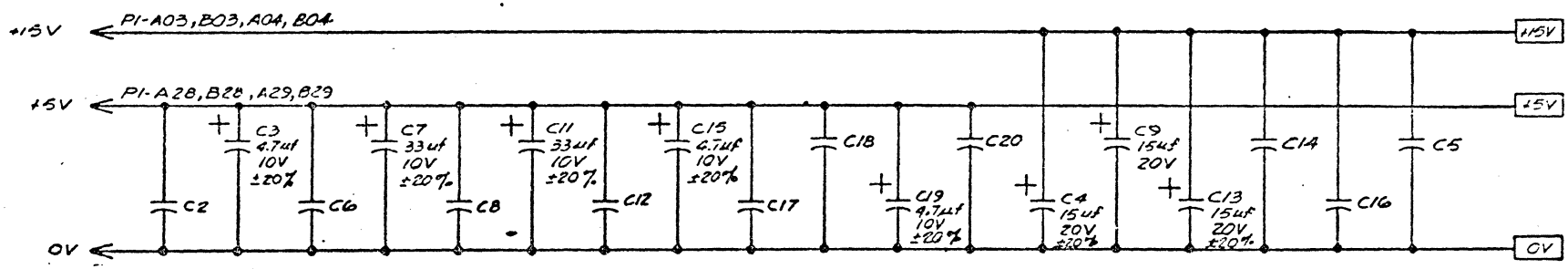
P1-A01, B01, A02, B02, A15, B15, A40, B40, A54, B54, A55, B55.

J1-A01, B01, A02, B02, A04, B04, A18, B18, A20, B20, A22, B22, A24, B24, A26, B26, A26, B26, A28, B29, A30, B30, A32, B32, A50, B50, A52, B52, A54, B54, A56, B55.



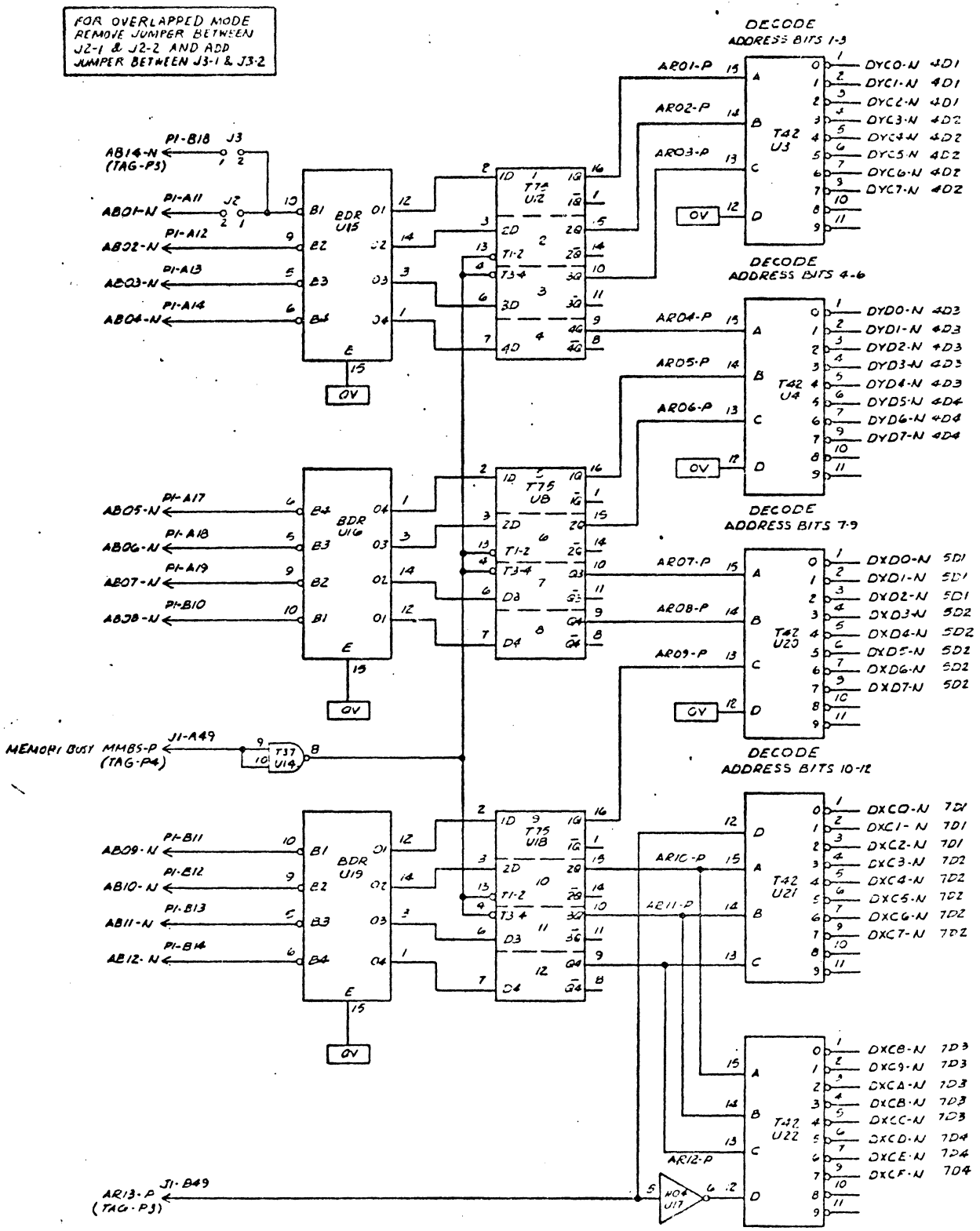


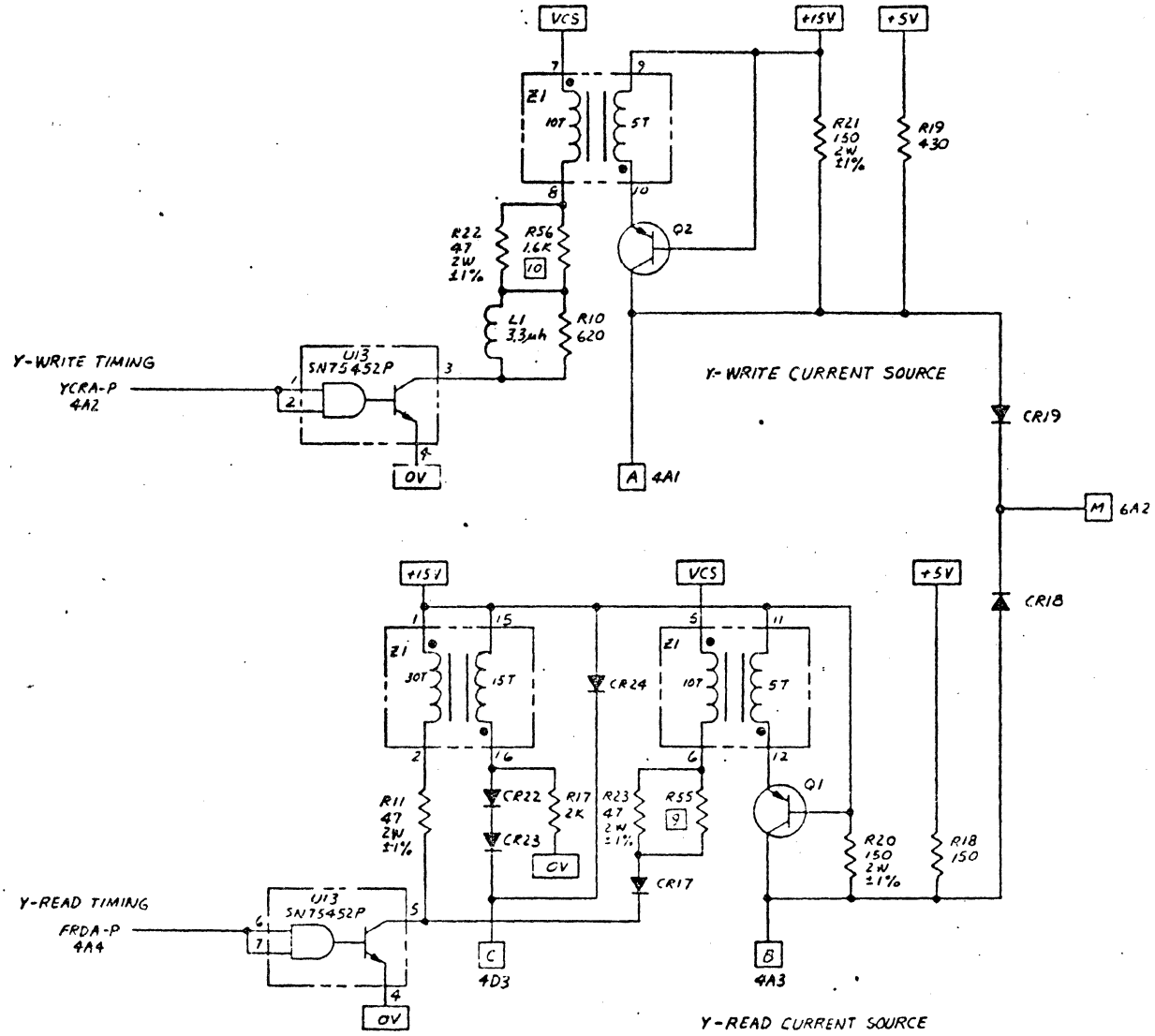


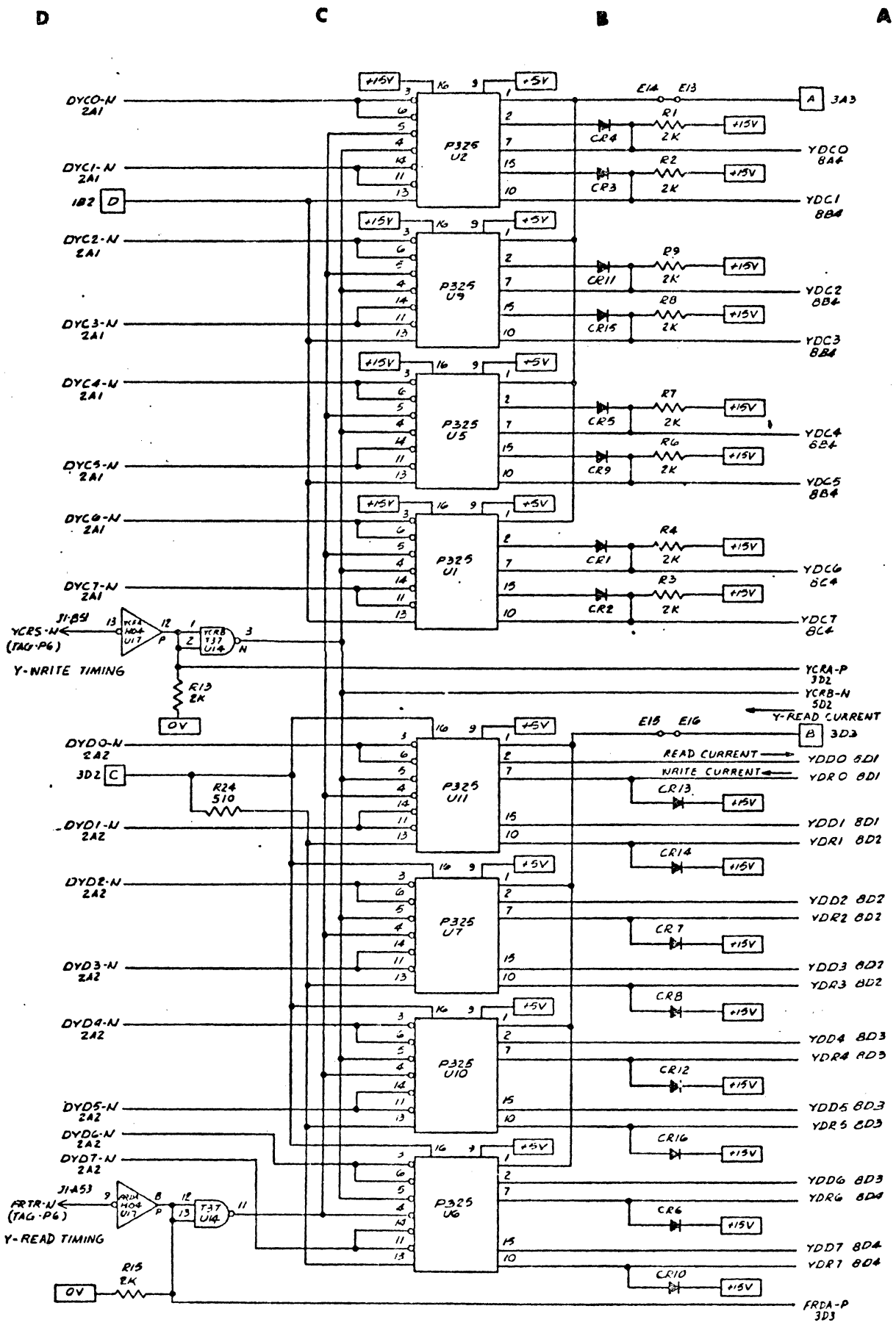


4 3 2 4

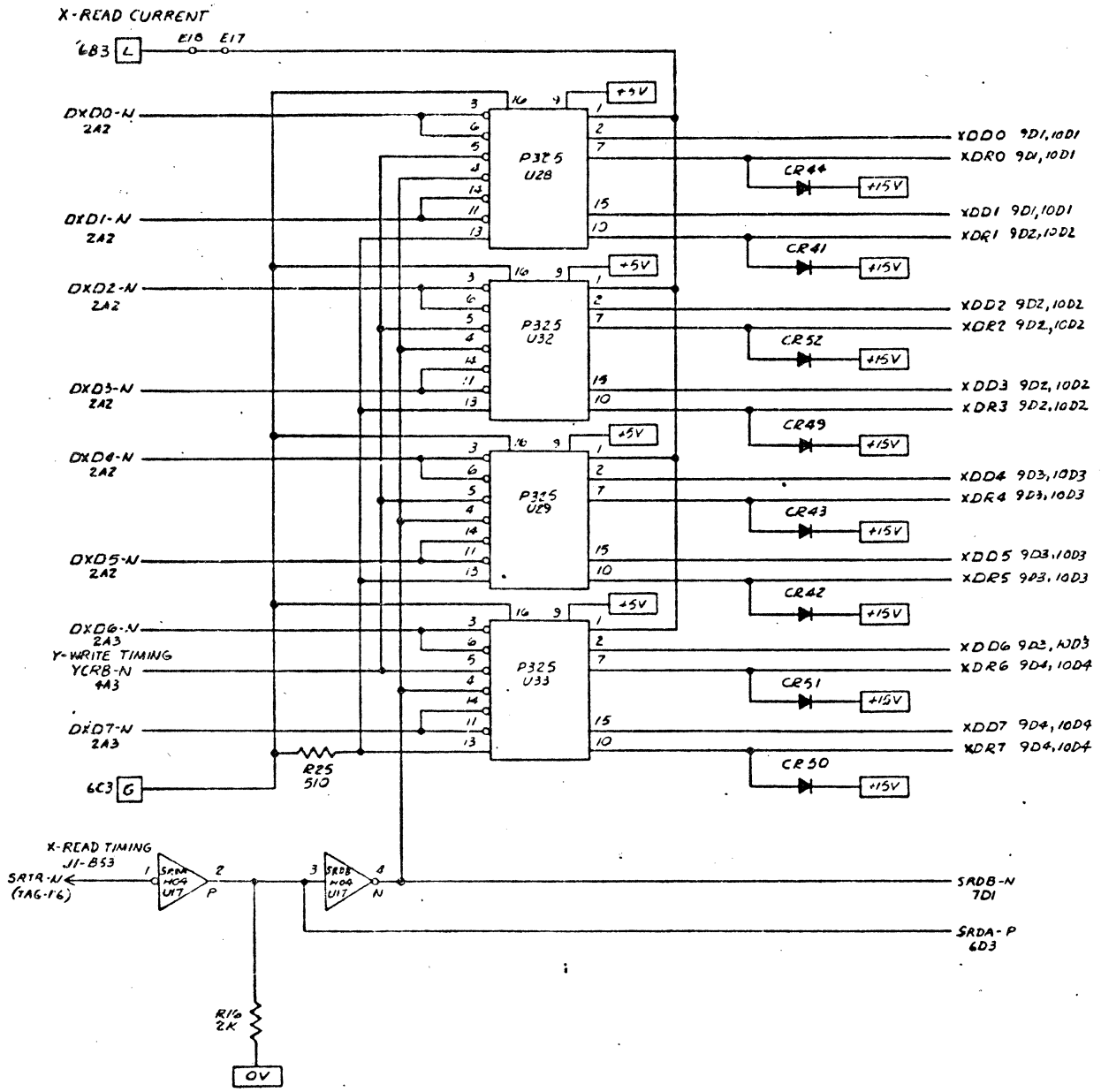
D C B A

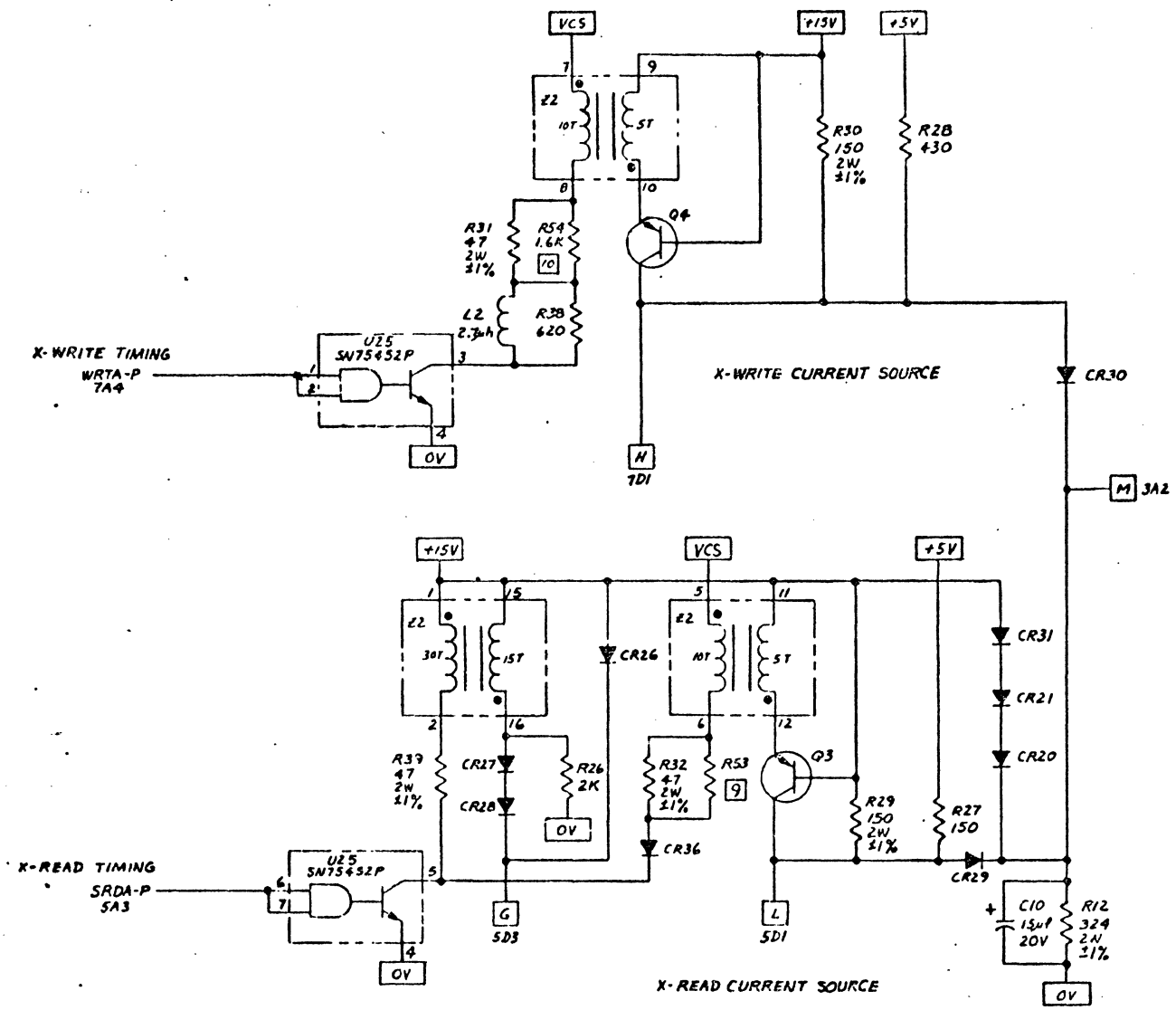

FOR OVERLAPPED MODE REMOVE JUMPER BETWEEN J2-1 & J2-2 AND ADD JUMPER BETWEEN J3-1 & J3-2
DECODE ADDRESS BITS 1-3
DECODE ADDRESS BITS 4-6
DECODE ADDRESS BITS 7-9
DECODE ADDRESS BITS 10-12
BDR U15
BDR U16
BDR U19
T74 U12
T75 U18
T75 U18
T42 U3
T42 U4
T42 U20
T42 U21
T42 U22
T37 U14
HO4 U17
AB14-N (TAG-P3)
AB01-N
AB02-N
AB03-N
AB04-N
AB05-N
AB06-N
AB07-N
AB08-N
AB09-N
AB10-N
AB11-N
AB12-N
MEMORY BUSY MMBS-P (TAG-P4)
AR13-P (TAG-P3)
AR01-P
AR02-P
AR03-P
AR04-P
AR05-P
AR06-P
AR07-P
AR08-P
AR09-P
AR10-P
AR11-P
AR12-P
DYC0-N 4D1
DYC1-N 4D1
DYC2-N 4D1
DYC3-N 4D2
DYC4-N 4D2
DYC5-N 4D2
DYC6-N 4D2
DYC7-N 4D2
DYD0-N 4D3
DYD1-N 4D3
DYD2-N 4D3
DYD3-N 4D3
DYD4-N 4D3
DYD5-N 4D4
DYD6-N 4D4
DYD7-N 4D4
DXD0-N 5D1
DXD1-N 5D1
DXD2-N 5D1
DXD3-N 5D2
DXD4-N 5D2
DXD5-N 5D2
DXD6-N 5D2
DXD7-N 5D2
DXC0-N 7D1
DXC1-N 7D1
DXC2-N 7D1
DXC3-N 7D2
DXC4-N 7D2
DXC5-N 7D2
DXC6-N 7D2
DXC7-N 7D2
DXC8-N 7D3
DXC9-N 7D3
DXCA-N 7D3
DXCB-N 7D3
DXCC-N 7D3
DXCD-N 7D4
DXCE-N 7D4
DXCF-N 7D4

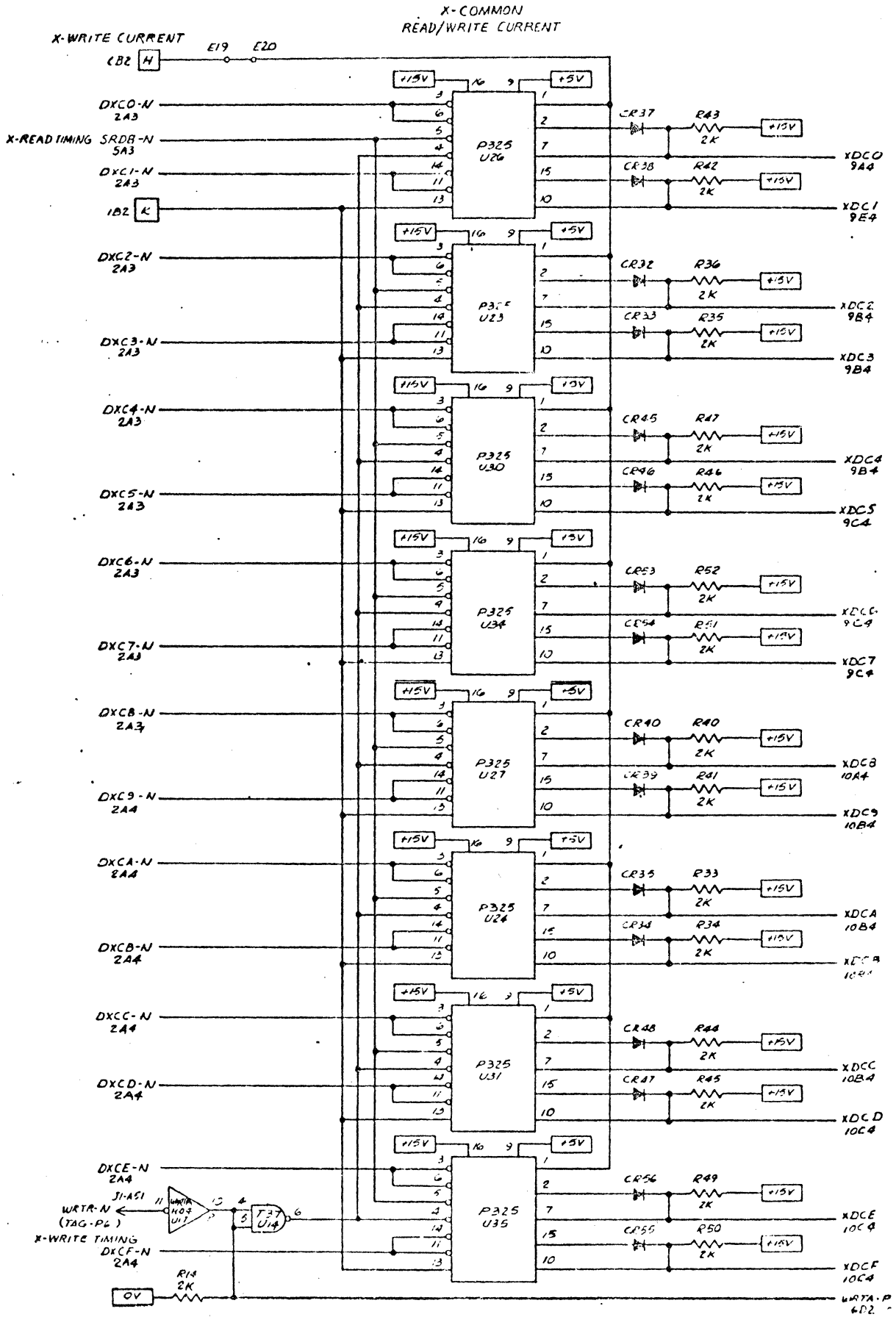

VCS
+15V
+5V
Z1
10T
5T
R21
150
2W
±1%
R19
430
R22
47
2W
±1%
R56
1.6K
10
Q2
L1
3.3μh
R10
620
Y-WRITE TIMING
YCRA-P
4A2
U13
SN75452P
OV
Y-WRITE CURRENT SOURCE
A
4A1
CR19
M
6A2
CR18
30T
15T
CR24
CR22
R17
2K
CR23
CV
R11
47
2W
±1%
R23
47
2W
±1%
R55
9
Q1
R20
150
2W
±1%
R18
150
CR17
Y-READ TIMING
FRDA-P
4A4
C
4D3
B
4A3
Y-READ CURRENT SOURCE



SUE 3312 8K Magnetic Core Memory, LD2001002219 EXY, Sheet 4 of 11 Rev. A

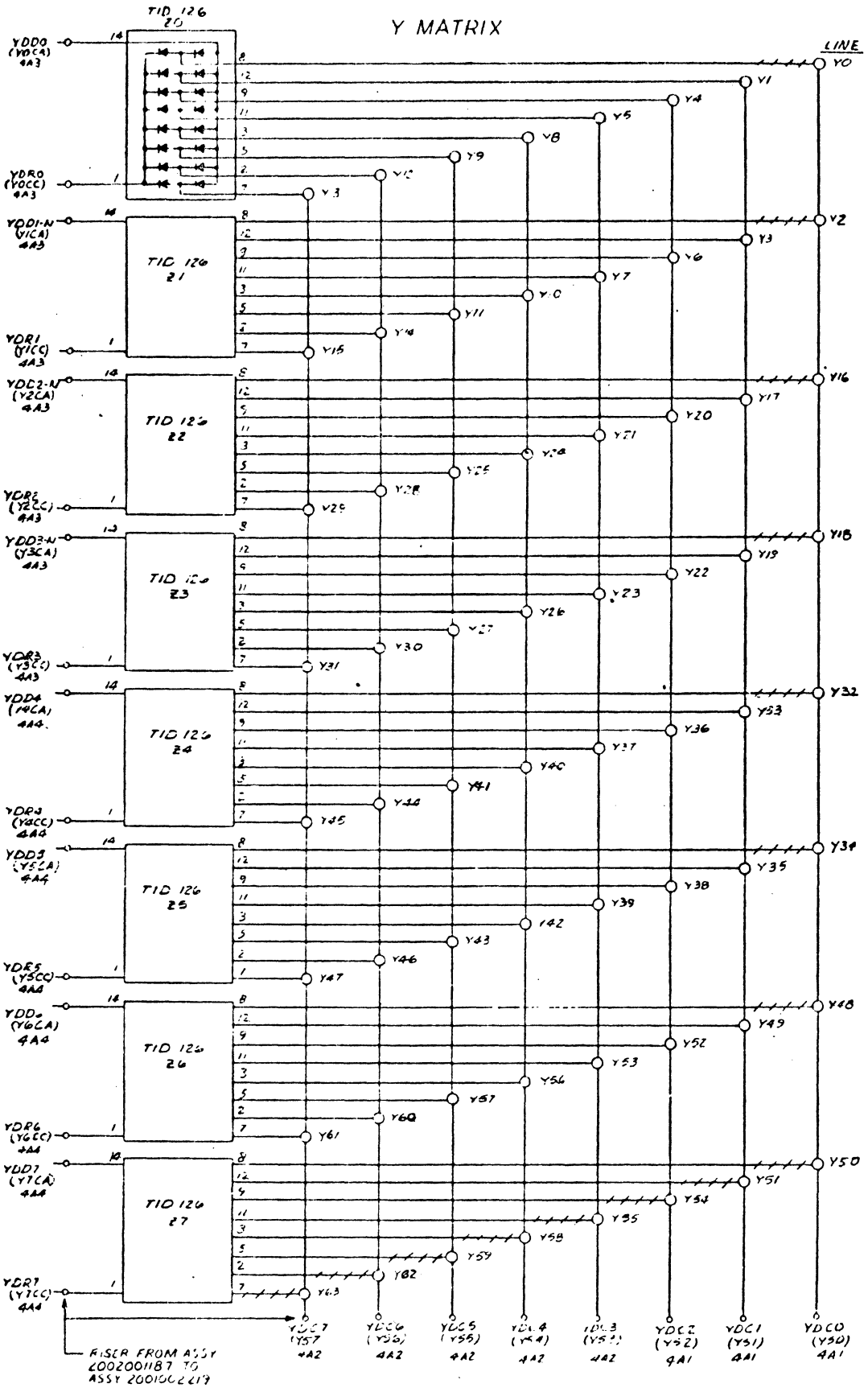

X-READ CURRENT
6B3 L
E18 E17
DXD0-N 2A2
DXD1-N 2A2
DXD2-N 2A2
DXD3-N 2A2
DXD4-N 2A2
DXD5-N 2A2
DXD6-N 2A3
Y-WRITE TIMING
YCRB-N 4A3
DXD7-N 2A3
6C3 G
R25 510
P325 U28
P325 U32
P325 U29
P325 U33
+5V
+15V
CR44
CR41
CR52
CR49
CR43
CR42
CR51
CR50
XDD0 9D1,10D1
XDR0 9D1,10D1
XDD1 9D1,10D1
XDR1 9D2,10D2
XDD2 9D2,10D2
XDR2 9D2,10D2
XDD3 9D2,10D2
XDR3 9D2,10D2
XDD4 9D3,10D3
XDR4 9D3,10D3
XDD5 9D3,10D3
XDR5 9D3,10D3
XDD6 9D3,10D3
XDR6 9D4,10D4
XDD7 9D4,10D4
XDR7 9D4,10D4
X-READ TIMING J1-B53
SRTR-N (TAG-16)
SRDA UNIT
SRDB UNIT
SRDB-N 7D1
SRDA-P 6D3
R16 2K
0V

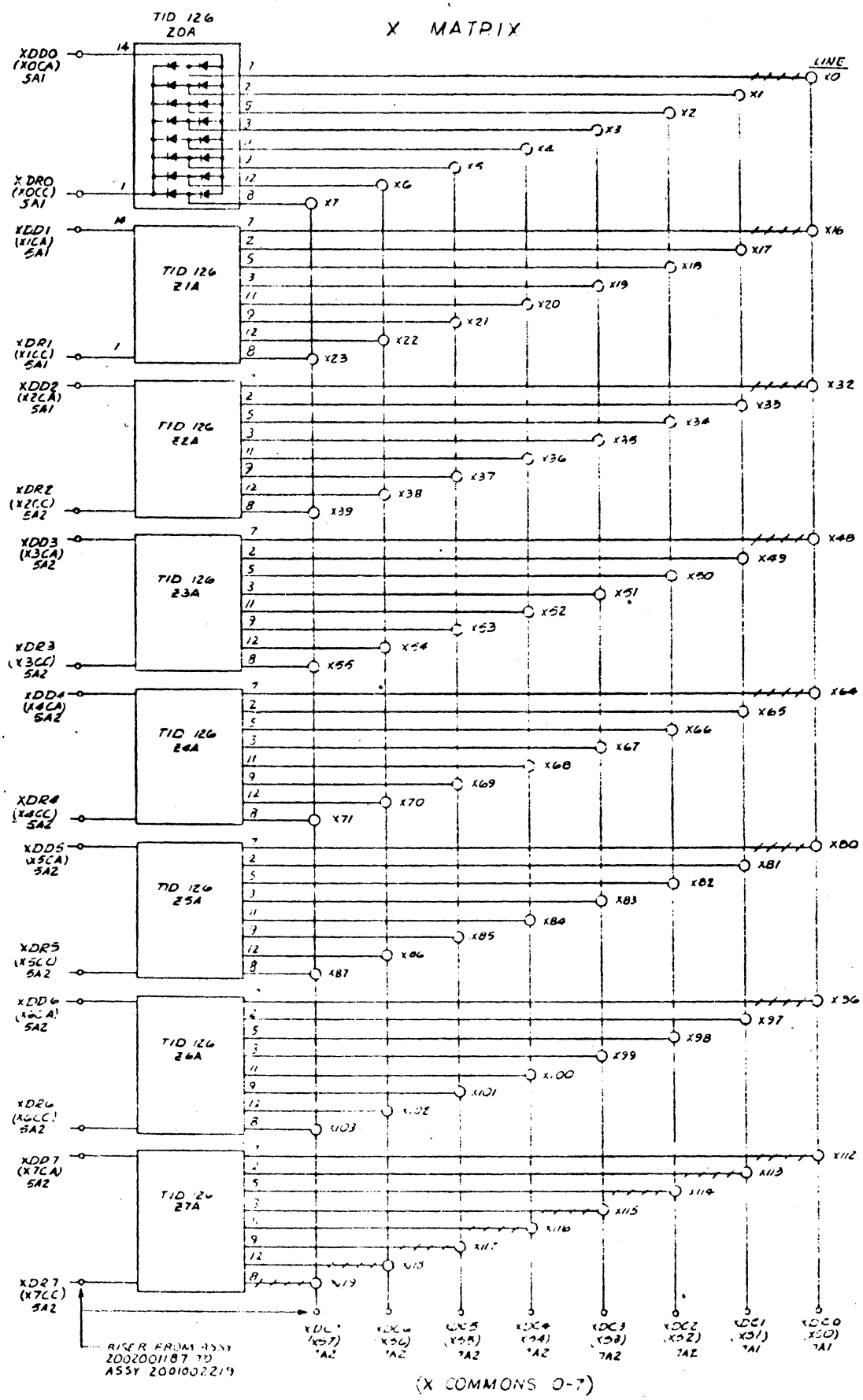

VCS
+15V
+5V
T2
10T
5T
R30
150
2W
±1%
R28
430
Q4
R31
47
2W
±1%
R54
1.6K
L2
2.7μh
R38
620
X-WRITE TIMING
WRTA-P
7A4
U15
SN75452P
OV
X-WRITE CURRENT SOURCE
CR30
M
3A2
7D1
+15V
VCS
+5V
T2
30T
15T
CR26
40T
5T
CR31
CR21
CR20
R39
47
2W
±1%
CR27
CR28
R26
2K
R32
47
2W
±1%
R53
9
Q3
R29
150
2W
±1%
R27
150
CR36
CR29
X-READ TIMING
SRDA-P
5A3
U25
SN75452P
G
5D3
L
5D1
C10
15μF
20V
R12
324
2W
±1%
X-READ CURRENT SOURCE



SUE 3312 8K Magnetic Core Memory, LD2001002219 EXY, Sheet 7 of 11 Rev. A

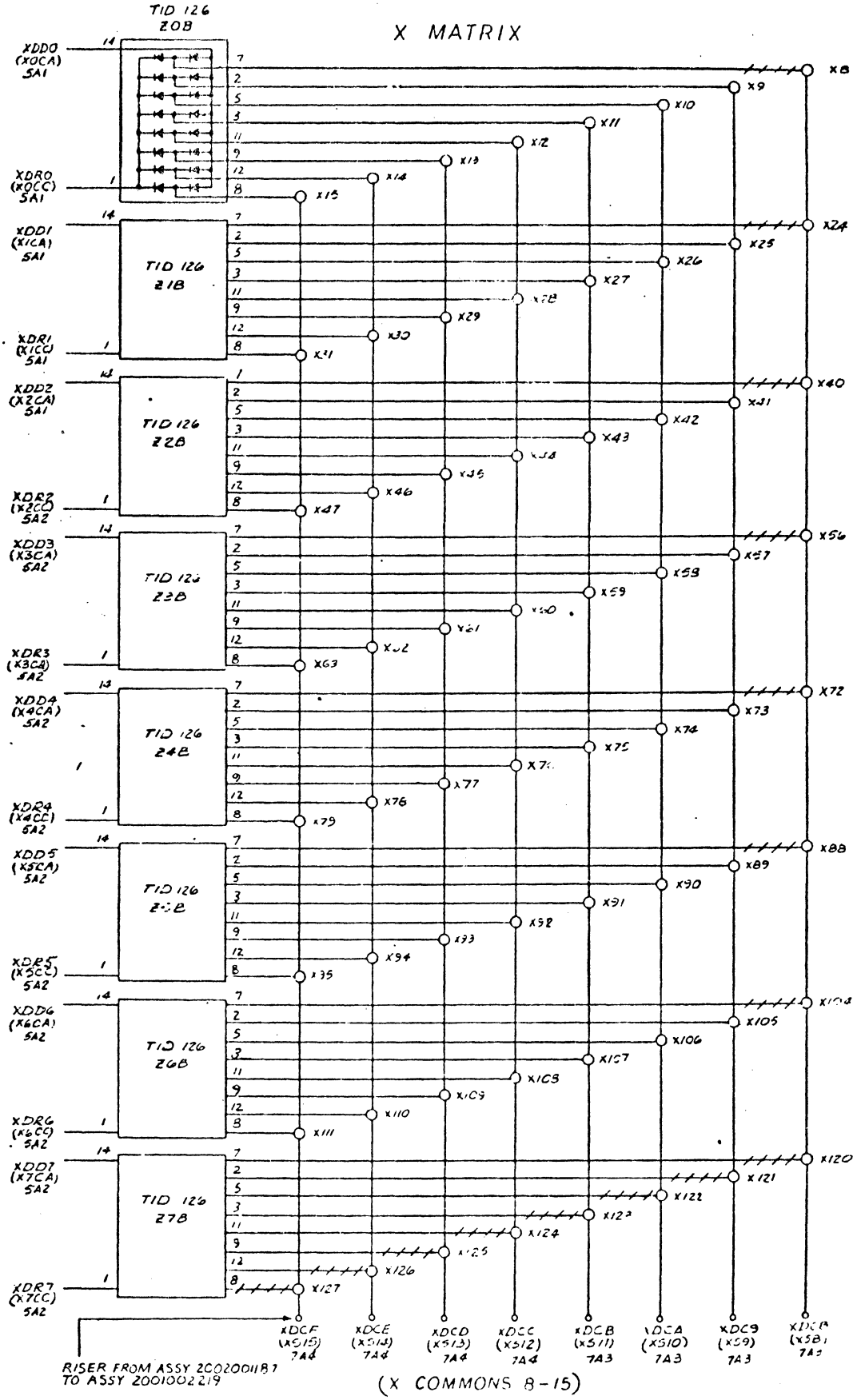
(ASSY, STACK 2001001187 3)



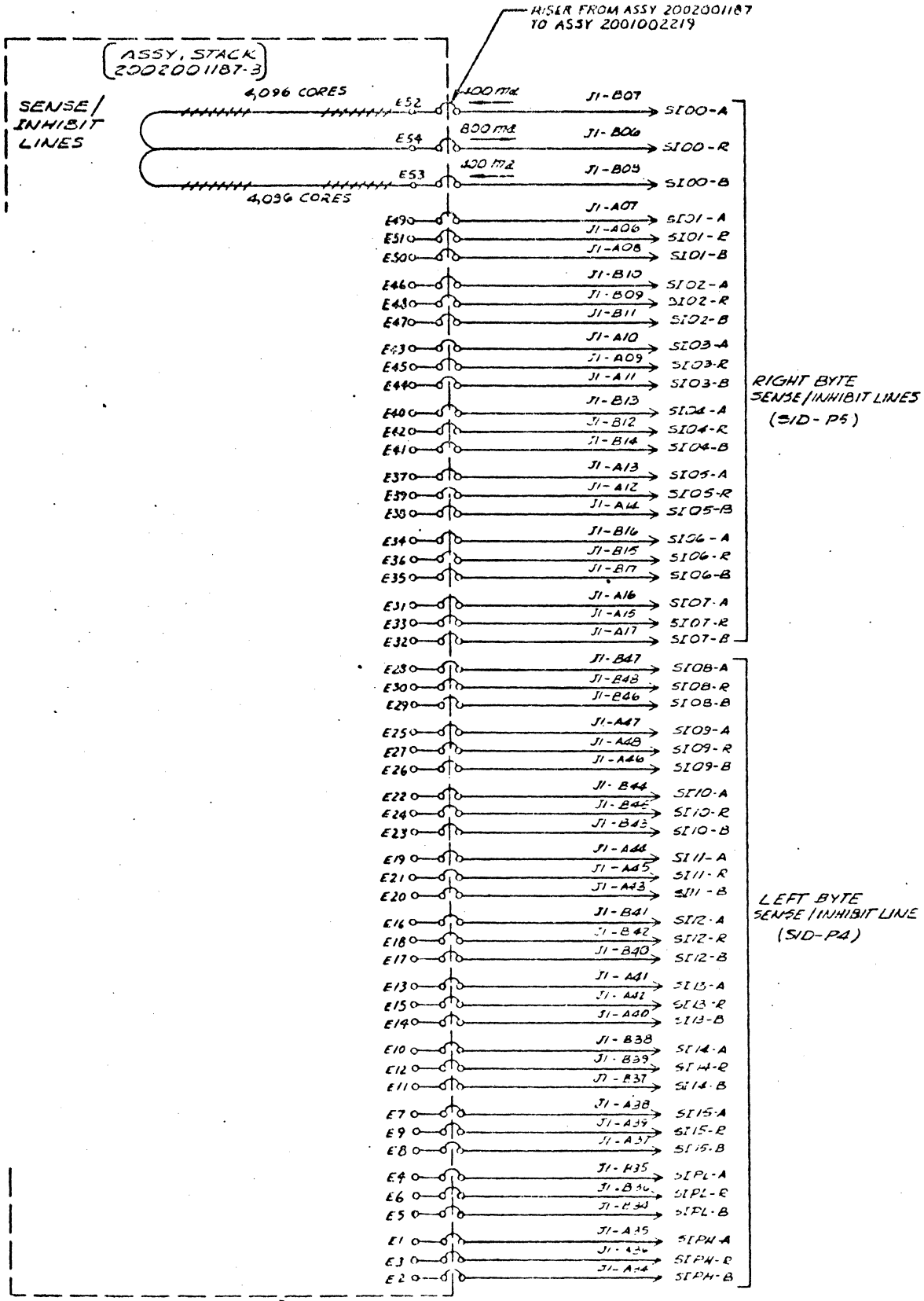


SDS 3312 8K Magnetic Core Memory, LD2001002219 EXY, Sheet 9 of 11 Rev. A

(ASSY STACK 2002001187-3)



SUE 3312 8K Magnetic Core Memory, LD2001002219 EXY, Sheet 10 of 11 Rev. A


RISER FROM ASSY 2002001187
TO ASSY 2001002219
ASSY, STACK
2002001187-3
SENSE/
INHIBIT
LINES
4,096 CORES
E52
E54
E53
4,096 CORES
400 mA
800 mA
400 mA
J1-B07
J1-B06
J1-B05
SI00-A
SI00-R
SI00-B
J1-A07
J1-A06
J1-A05
SI01-A
SI01-R
SI01-B
J1-B10
J1-B09
J1-B11
SI02-A
SI02-R
SI02-B
J1-A10
J1-A09
J1-A11
SI03-A
SI03-R
SI03-B
J1-B13
J1-B12
J1-B14
SI04-A
SI04-R
SI04-B
J1-A13
J1-A12
J1-A14
SI05-A
SI05-R
SI05-B
J1-B16
J1-B15
J1-B17
SI06-A
SI06-R
SI06-B
J1-A16
J1-A15
J1-A17
SI07-A
SI07-R
SI07-B
RIGHT BYTE
SENSE/INHIBIT LINES
(SID-P5)
J1-B47
J1-B48
J1-B46
SI08-A
SI08-R
SI08-B
J1-A47
J1-A48
J1-A46
SI09-A
SI09-R
SI09-B
J1-B44
J1-B45
J1-B43
SI10-A
SI10-R
SI10-B
J1-A44
J1-A45
J1-A43
SI11-A
SI11-R
SI11-B
J1-B41
J1-B42
J1-B40
SI12-A
SI12-R
SI12-B
J1-A41
J1-A42
J1-A40
SI13-A
SI13-R
SI13-B
J1-B38
J1-B39
J1-B37
SI14-A
SI14-R
SI14-B
J1-A38
J1-A39
J1-A37
SI15-A
SI15-R
SI15-B
J1-B35
J1-B36
J1-B34
SIPL-A
SIPL-R
SIPL-B
J1-A35
J1-A36
J1-A34
SIPH-A
SIPH-R
SIPH-B
LEFT BYTE
SENSE/INHIBIT LINE
(SID-P4)
E28
E30
E29
E25
E27
E26
E22
E24
E23
E19
E21
E20
E16
E18
E17
E13
E15
E14
E10
E12
E11
E7
E9
E8
E4
E6
E5
E1
E3
E2

JNH

PREPARED M. GLEIXNER DATE 6/28/7?
CHK [illegible] DATE [illegible]
ENGR [illegible] DATE [illegible]
PROJ ENGR [illegible] DATE [illegible]

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

B	14715	PL 20001002219-1	B
SIZE	CODE IDENT	SHEET 2	REV

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		20001002219-1		EXY-CKT CARD ASSY		USED ON SUE 3312	1
002		001	0001		1001004954-5		PRINTED WRG BD, EXY			2
003		001	0001		20020011187-3		FRAME, ASSY			3
004		001	0001		1001005141-1		COVER			4
005		000								5
006	F	001	0001		8001800044-1		ICP		U17 (74H04)	6
007	F	005	0001		8001800083-1		ICP		U3,4,21,22,20 (7442)	7
008	F	003	0001		8001800100-1		ICP		U8,12,18 (7475)	8
009	F	003	0001		8001800120-1		ICP		U15,16,19 (BDR)	9
010		001	0001		8001803139-1		ICP		U14 (7437)	10
011		020	0001		SN75325N	01295	ICP	TEXAS INSTR INC	U1,2,5,6,7,9,10, 11,23,24,26,27, 28,29,30,31,32, 33,34,35	11
012		002	0001		SN75452P	01295	ICP	TEXAS INSTR INC	U13,25	12
013		000								13
014		000								14
015	E	002	0001		8001400092-1		TRANSFORMER		Z1,2	15
016		000								16
017	E	004	0001		8001200016-1		TRANSISTOR		Q1 THRU Q4 (TO5)	17
018		000								18
019	E	055	0001		8001100001-1		DIODES		CR1 THRU CR24, CR26 THRU CR56 .5 IS	19
020		000								20
021		000								21
022		003	0001		M39003/01-2015		CAPACITOR	MIL-C-39003/1	C3,15,19 .65 IS	22
023		002	0001		M39003/01-2018		CAPACITOR	MIL-C-39003/1	C7,11 .8 IS	23
024		005	0001		M39003/01-2050		CAPACITOR	MIL-C-39003/1	C1,4,9,10,13 .8 IS	24
025	F	010	0001		8001300101-1		CAPACITOR		C2,5,6,8,12,14, 16,17,18,20 .25 IS	25
026		000								26
027		000								27
028		001	0001		RL07S120G		RESISTOR	MIL-R-22684/1	R48 .5 IS	28
029		030	0001		RL07S202G		RESISTOR	MIL-R-22684/1	R1 THRU R4, R6 THRU R9, R13 THRU R17, R26,R33 THRU R36,R40 THRU R47,R49 THRU R52 .5 IS	29
030		002	0001		RL07S301G		RESISTOR	MIL-R-22684/1	R5,37 .5 IS	30

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES

A — DENOTES SEPARATE PL
B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO
C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS
E — SOURCE CONTROL DWG
F — SPEC CONTROL DWG
M — DENOTES MADE FROM
& — ALTERNATE SOURCE

DEFINITIONS

ICP — INTEGRATED CIRCUIT PKG
I.S. — INCEPTION SPAN
A/R — AS REQD

REVISIONS

FOR REV RECORD SEE SHEET 1

LECW 239 (JAN 70) K&E

TAG

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

SIZE	CODE IDENT	PL	REV
B	14715	2001002219-1	B

SHEET 3

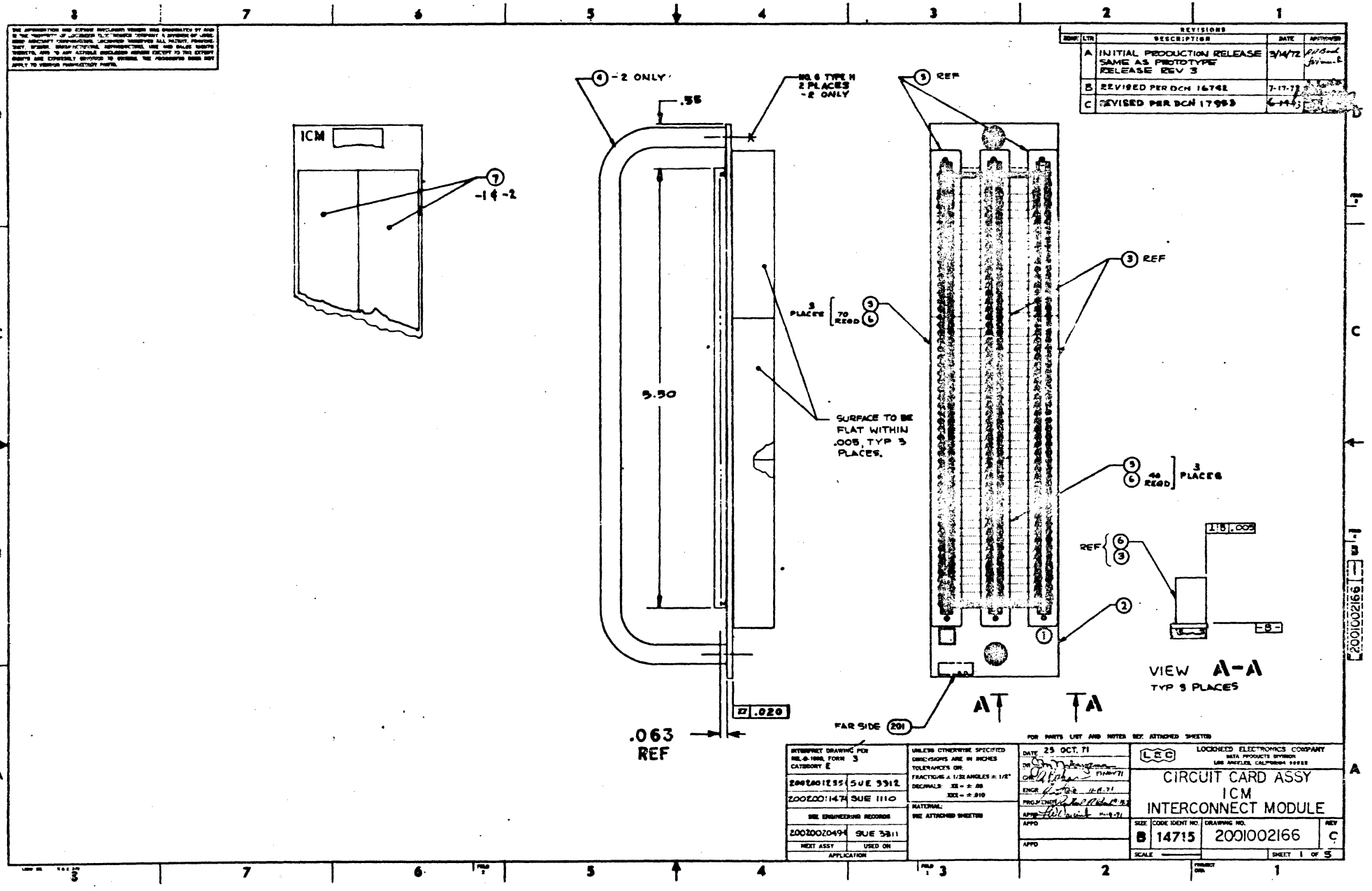
	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
031		002	0001		RL07S511G		RESISTOR	MIL-R-22684/1	R24,25 .5 IS	31
032		000								32
033	B	006	0001		TYPE BR5-47.0	07716	RESISTOR	IRC, INC	R11,22,23,31,32, 39 .6 IS BR5-47.0 OHM1PCT TC100PPM/C DEG	33
034	B	004	0001		TYPE BR5-150	07716	RESISTOR	IRC, INC	R20,21,29,30 .6 IS BR5-150 OHM1PCT TC100PPM/C DEG	34
035	B	001	0001		TYPE BR5-324	07716	RESISTOR	IRC, INC	R12 .6 IS BR5-324 OHM1PCT TC100PPM/C DEG	35
036		002	0001		RL07S162G		RESISTOR	MIL-R-22684/1	R54,56 NOTE 219	36
037		002	0001		RL07S621G		RESISTOR	MIL-R-22684/1	R10,38 .5 IS	37
038		002	0001		RL07S431G		RESISTOR	MIL-R-22684/1	R19,28 .5 IS	38
039		002	0001		RL07S151G		RESISTOR	MIL-R-22684/1	R18,27 .5 IS	39
040		001	0001		9310-24		INDUCTOR	J.W. MILLER CO COMPTON, CA	L1 .6 IS	40
041		001	0001		9310-22		INDUCTOR	J.W. MILLER CO COMPTON, CA	L2 .6 IS	41
042	F	006	0001		9003400419-7		WIRE, BARE		28AWG APPROX INCH REQD	42
043		004	0001		2226B	13103	HEATSINK	THERMALLOY		43
044	F	004	0001		1005000041-1		TRANSIPAD		TO5	44
045	F	006	0001		9003400419-3		WIRE, RISER		APPROX FT REQD	45
046		006	0001		1001085025-2		SPACER		5/16 DIA	46
047	F	008	0001		1005000764-1		PIN, TERMINAL		NOTE 217	47
048		A/R	0001		1203	71984	PRIMER	DOW CORNING		48
049		A/R	0001		3145	71984	RTV COATING	DOW CORNING		49
050		A/R	0001		SN60/SN63		SOLDER	QQ-S-571		50
051		000								51
052		REF	0001		LD2001002219-1		LOGIC DIAGRAM			52
053		000								53
054		003	0001		26AWG WHT		SLEEVING	MIL-I-22129	APPROX INCH REQD	54
055		001	0001		M70-9-506	14193	THERMISTER	CAL-R, INC	RT1 .1 IS	55
056		A/R	0001		DELTA BOND	05820	ADHESIVE	WAKEFIELD ENGR	NO. 152	56
057		A/R	0001		RTA	05820	HARDENER	WAKEFIELD ENGR		57

CONFORMS TO MIL-STD-100

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL NOTE(S) REF DESIGNATION(S)	FIND NO.
200	REF	0001		SPEC/DWG/STD		NOTES:			200
201	A/R	0001		LECP1049-17		MARKING (IDENTIFY).			201
202	REF	0001		LECP1080		CLEANING.			202
203	REF	0001				AREA TO BE FREE OF SOLDER.			203
204	REF	0001				COMPONENTS NOT CALLED OUT BY THEIR FIND NO. ON FACE OF DRAWING ARE IDENTIFIED BY THEIR REF DESIGNATIONS.			204
205	REF	0001				COMPONENT HEIGHT .395 MAX.			205
206	REF	0001				PROTRUSION SIDE 2 .075 MAX. LEADS TO BE VISIBLE THRU SOLDER.			206
207	REF	0001				TOTAL WARP AND TWIST SHALL NOT EXCEED .010 INCH/INCH IN GENERAL AREA AND .005 INCH/INCH IN CONNECTOR AREA.			207
208	REF	0001				SQUARE PAD DENOTES CATHODE END (STRIPE) OF DIODE OR POSITIVE (+) END OF CAPACITOR.			208
209	REF	0001				RECTANGULAR PAD AND DOT OR SLOTTED END OF ICP DENOTES PIN 1.			209
210	REF	0001				MAXIMUM COMPONENT CONFIGURATION DEPICTED ON FACE OF DRAWING. FOR ACTUAL USAGE SEE APPLICABLE PARTS LIST.			210
211	000								211
212	000								212
213	000								213
214	A/R	0001		LECP1075		HARDWARE.			214
215	REF	0001				THE FOLLOWING CONNECTIONS ARE TO BE MADE USING FIND NO. 42. FROM TO J2-1 J2-2 E13 E14 E15 E16 E17 E18 E19 E20			215
216	REF	0001				R53 IS A TRIM RESISTOR (LAB SET) AND MAY BE INSTALLED AT TEST LEVEL, (IF NECESSARY)			216
217	REF	0001				⊠ SYMBOL DENOTES TERMINAL PIN INSTALLATIONS.			217
218	REF	0001				PRECOAT MATING SURFACE OF FIND NO. 55 WITH FIND NO.S 56 AND 57. BOND FIND NO. 55 TO FIND NO. 3 WITH FIND NO.S 56 AND 57. INSULATE LEADS WITH FIND NO. 54 AND SOLDER TO PADS AS SHOWN.			218
219	REF	0001				R54,55 AND 56 COMPONENT VALUES MAY BE CHANGED AT TEST LEVEL.			219
220	REF	0001				FOR 2001002219-2 APPLICATION THESE RISER WIRES ARE NOT REQUIRED.			220

TAG

CONFORMS TO MIL-STD-100



REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INITIAL PRODUCTION RELEASE SAME AS PROTOTYPE RELEASE REV 3	3/14/72	
	B	REVISED PER DCN 16782	7-17-72	
	C	REVISED PER DCN 17983	6-14-73	

INTERPRET DRAWING PER MIL-D-1000, FORM 3 CATEGORY E		
2002001555	SUE 3312	
2002001474	SUE 1110	
SEE ENGINEERING RECORDS		
2002002049	SUE 3311	
NEXT ASSY	USED ON	
APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ± 1/32 ANGLES ± 1/2°
DECIMALS .XX – ± .03
.XXX – ± .010
MATERIAL:
SEE ATTACHED SHEETS

FOR PARTS LIST AND NOTES SEE ATTACHED SHEETS

DATE	25 OCT. 71	
DR		
CHK		11-9-71
ENGR		11-8-71
PROJ ENGR		
APPD		11-9-71
APPD		
APPD		

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

CIRCUIT CARD ASSY ICM INTERCONNECT MODULE

SIZE	CODE IDENT NO.	DRAWING NO.	REV
B	14715	2001002166	C
SCALE		SHEET 1 OF 5	

2001002166

PREPARED	DATE
CHK	DATE
ENGR	DATE
PROJ ENGR	DATE

LOCKHEED ELECTRONICS COMPANY
DATA PRODUCTS DIVISION
LOS ANGELES, CALIFORNIA 90022

A	14715	PL 2001002166-0	C
SIZE	CODE IDENT	SHEET 2	REV

SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001	000	0001		2001002166-0		ICM-CKT CARD ASSY		PROCUREMENT ONLY	1
002	001	0001		1001004808-1		PRINTED WRG BD, ICM			2
003	003	0001		121-7360-035	71468	INSULATOR, ECP4	ITT CANNON	70 POS (DUAL 35)	3
004	003	0001		121-7360-020	71468	INSULATOR, ECP4	ITT CANNON	40 POS (DUAL 20)	5
005	330	0001		030-7331-001	71468	CONTACT, ECP4	ITT CANNON	.094 THK BD	6

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	E — SOURCE CONTROL DWG F — SPEC CONTROL DWG M — DENOTES MAKE FROM & — ALTERNATE SOURCE	IC P — INTEGRATED CIRCUIT PKG I S — INSERTION SPAN A/R — AS REQD	FOR REV RECORD SEE SHEET 1

CONFORMS TO MIL-STD-100

LECW 263 (JAN 70) K & E

TAG

PREPARED	G. MERINO	DATE 7/20/72	LOCKHEED ELECTRONICS COMPANY DATA PRODUCTS DIVISION LOS ANGELES, CALIFORNIA 90022	A	14715	PL 20010002166-1	C
CHK	L. OHANESIAN	DATE 7/20/72					
ENGR	J. RITTER	DATE 7/21/72					
PROJ ENGR		DATE		SIZE	CODE IDENT	SHEET 3	REV

	SYM	QTY REQD	SERIAL NO. START	SERIAL NO. END	PART NUMBER	CODE IDENT	DESCRIPTION	SPECIFICATION / VENDOR	MATL/NOTE(S) REF DESIGNATION(S)	FIND NO.
001		000	0001		20010002166-1		ICM-CKT CARD ASSY		USED ON SUE 1110-1	1
002		001	0001		20010002166-0		ICM-CKT CARD ASSY			2
003		000								3
004		000								4
005		000								5
006		000								6
007		012	0001		4508 .75 WIDE	04963	FOAM TAPE	3M CO	APPROX INCH REQD	7

CONFORMS TO MIL-STD-100

SYM AND FIND NO. COLUMN CODES		DEFINITIONS	REVISIONS
A — DENOTES SEPARATE PL B — REMARKS COLUMN CONTAINS ADDITIONAL ORDERING INFO C — INFO UNAVAILABLE, TO BE ADDED BY CHG DOCUMENTS	E — SOURCE CONTROL DWG F — SPEC CONTROL DWG M — DENOTES MAKE FROM & — ALTERNATE SOURCE	IC P — INTEGRATED CIRCUIT PKG I S — INSERTION SPAN A/R — AS REQD	FOR REV RECORD SEE SHEET 1

[redacted]

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	2/[illegible]	

TAG

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN [illegible]

CHECKER

ENGINEER [illegible]

APP'D FOR REL [illegible]

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

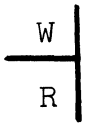
TAG TECHNICAL REF

SIZE	CODE IDENT NO.	DRAWING NO.
A		TAG-05

SCALE	REV	SHEET
	A	1 OF 3

A

Status - address none



Switches

Memory Address Select

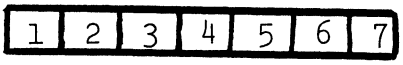
Address Range	Set These Switches						
	1	2	3	4	5	6	7
0-8K	X	X	X	X	X	X	X
0-4K	X	X	X	X	X	X	X
4-8K	-	X	X	X	X	X	X
8-16K	X	X	-	X	X	X	X
8-12K	X	X	-	X	X	X	X
12-16K	-	X	-	X	X	X	X
16-24K	X	X	X	X	X	-	X
16-20K	X	X	X	X	X	-	X
20-24K	-	X	X	X	X	-	X
24-32K	X	X	-	X	X	-	X
24-28K	X	X	-	X	X	-	X
28-32K	-	X	-	X	X	-	X
32-64K	as above			X	-	as above	
64-96K	as above			-	X	as above	
96-128K	as above			-	-	as above	

KEY Ø

KEY 1

KEY 2

KEY 3



Note: In interleave mode, set one switch #2 and reset the other switch #1.

X = set

Note: On some cards these switches will be pairs of jumper pins instead. A jumper equals a set switch.

TAG

TAG

Jumpers

Address Recognition

Address Bit	Connect	
	From	To
17	J2-A2	J2-B2
16	J2-A3	J2-B3
15	J2-A5	J2-B5
14	J2-A6	J2-B6
13	J2-A7	J2-B7
1	J2-A4	J2-B4

For 8K memory, do not connect J2-A7 to J2-B7. Connect J2-A4 to J2-B4 only for interleave mode.

Memory Core Card

Card Type	Connect	
	From	To
EXY	J5-1	J5-2
MXY	J5-2	J5-3

Note: MXY is 4K only;
EXY is 4K or 8K.

Memory Size:

For 4K memory, U28 is not installed.

Jumper E141 and E142 for 4K memory.

High Core Blind

To make 30K to 32K blind connect:

J2-A5 to J2-B5

J2-A6 to J2-B6

J2-A1 to J2-B1

To make 31K to 32K only blind, also connect:

J3-1 to J3-2

Interleave Mode - Jumper J2-A4 to J2-B4

Interlock Mode unused.

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION	2/2/76	

TAG

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL.

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

TAG MODIFICATION STND

SIZE	CODE IDENT NO.	DRAWING NO.
A		TAG-15

SCALE	REV A	SHEET 1 OF 3

Card Type TAG Modification Standard

Card Function: Memory Timing

Modification Description:

Enable later selection of key bit recognition.

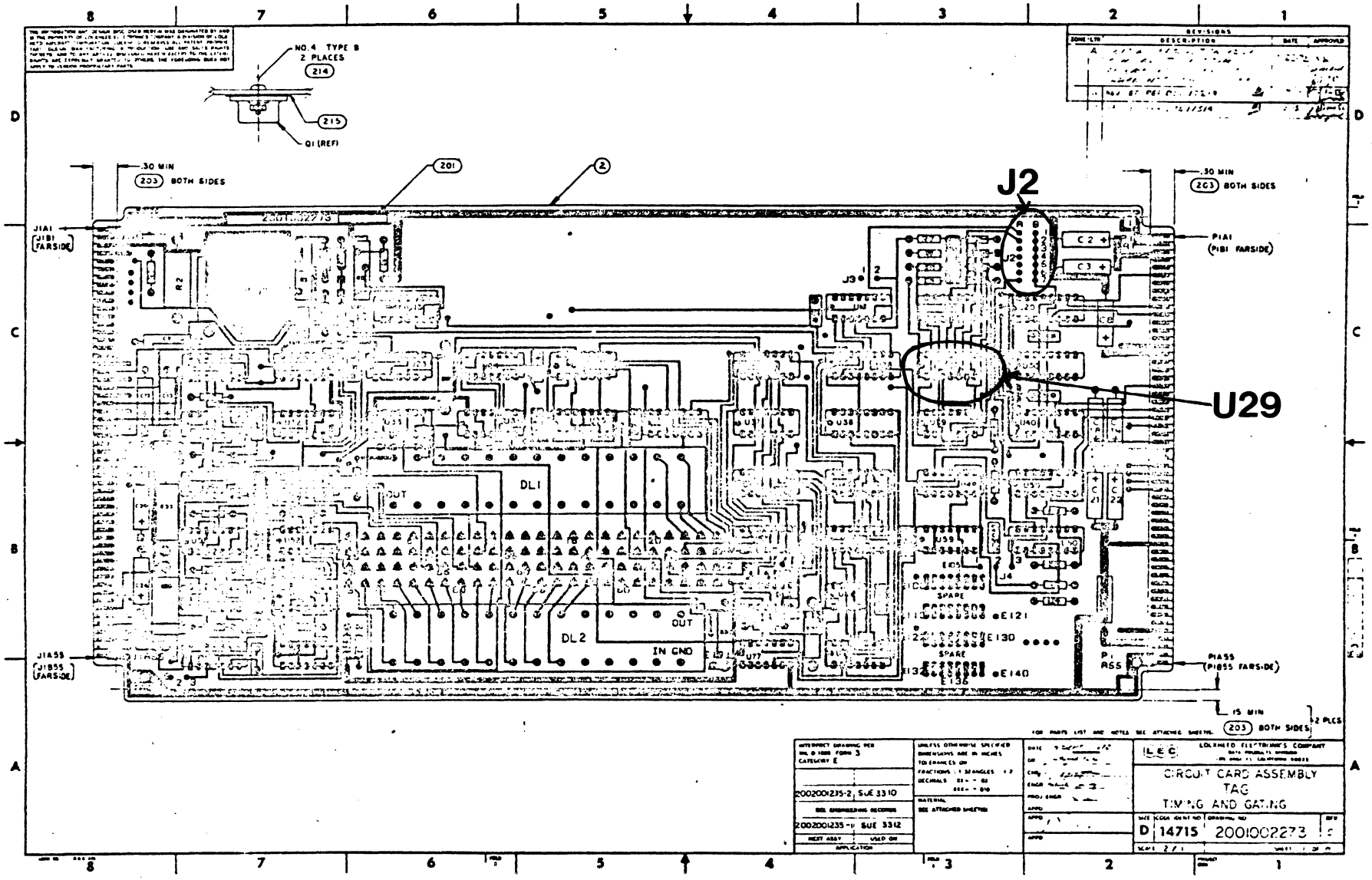
Implementation:

Insert and solder wire wrap pins at

J2: pins 2A, 2B, 3A, 3B.

See attached drawing.

TAG


J2
U29
DL1
DL2
OUT
IN GND
SPARE
CIRCUIT CARD ASSEMBLY
TAG
TIMING AND GATING
D
14715
2001002273

APPLICATION	
NEXT ASSY	USED ON

REVISION			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASE FOR PRODUCTION		

SEE TAG-Ø2

TAG

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

RECORD OF REVISION STATUS OF EACH SHEET

CONTRACT NO:

DRAFTSMAN

CHECKER

ENGINEER

APP'D FOR REL

APP'D (CUSTOMER)

Bolt Beranek and Newman Inc.
Cambridge Massachusetts

DRAWING TITLE

TAG SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.
A		TAG-2Ø

SCALE	REV	SHEET 1 OF 1

CABLES

CABLE LIST

Drawing No.	Revision
AHSA-10	A
AHSA-11	A
DBRS-10	A
DBRS-11	A
DHLD-10	F
DHLD-11	B
DHLS-10	G
DHLS-11	B
DHSD-10	E
DHSD-11	B
DHSS-10	D
DHSS-11	B
DILS-10	C
DILS-11	B
DKGB-10	A
DKGB-11	A
DKGC-10	A
DKGC-11	A
DLCF-10	A
DLCF-11	A
DLCM-10	A
DLCM-11	A
DLTF-10	A
DLTF-11	A
DLTM-10	A
DLTM-11	A

CABLE LIST Cont'd.

Drawing No.	Revision
DMLD-10	F
DMLD-11	C
DMLS-10	F
DMLS-11	C
DPSB-10	F
DPSB-11	C
DPTP-10	A
DPTP-11	A
DPTR-10	E
DPTR-11	B
DRBS-10	A
DRBS-11	A
DRSP-10	C
DRSP-11	A
DRSS-10	C
DRSS-11	A
DTTY-10	D
DTTY-11	A
FHDA-10	A
FHDA-11	A
FHSA-10	E
FHSA-11	C
FHSH-10	A
FHSH-11	A
FHSI-10	B
FHSI-11	B
FHSS-10	A
FHSS-11	A

CABLE LIST Cont'd.

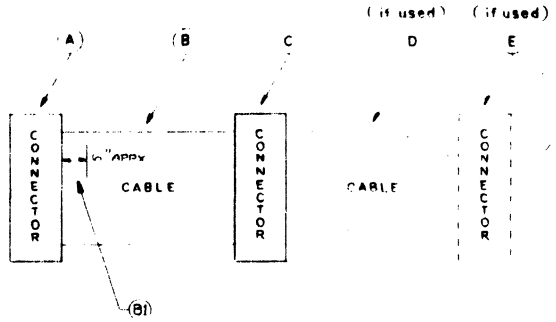
Drawing No.	Revision
FHST-10	A
FHST-11	A
FKGA-10	B
FKGA-11	B
FMHA-10	C
FMHA-11	B
FMLA-10	C
FMLA-11	A
FPTP-10	A
FPTP-11	A
FTIA-10	A
FTTY-10	B
FTTY-11	A
IAMA-10	B
IAMA-11	A
IAMC-10	B
IAMC-11	A
IBCA-10	B
IBCA-11	A
IFCA-10	A
IFCA-11	A
IILJ-10	B
IILJ-11	B
IJMP-10	B
IJMP-11	B
IPTP-10	B
IPTP-11	A
IPTR-10	C
IPTR-11	A

CABLE LIST Cont'd.

Drawing No.	Revision
IRLD-10	A
IRLD-11	A
ITTC-10	A
ITTC-11	A
ITTR-10	A
ITTR-11	A
ITTY-10	A
ITTY-11	A
PILC-10	C
PWRA-10	B
PWRA-11	A
SBRS-10	A
SBRS-11	A
SRBS-10	A
SRBS-11	A
XILC-10	A
XILC-11	A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	8 2 77

PIN NUMBERING & ASSEMBLY DETAILS



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO.
A	1	MALE CONN	CINCH	DP-37P	149
A1	1	PLASTIC BACK SHELL	AMPHENOL	17-1373	155
A2	2	DISC LATCHES	CANNON	DHW278	367
B	(*)	25 TW/PR CABLE	WOVEN CABLE	1255TC-2807 BL127N	49
C	1	FEMALE CONN	AMPHENOL	48-10R18-31S	
B1	1	TIE WRAP NAME TAG	PANDUIT	PLE1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		

DISTANT HOST ADAPTER CABLE

CABLE FUNCTION	
FROM A	FANTAIL
TO C	DISTANT HOST
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	7/25/77	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED	[illegible]	8/26/77	CUSTOMER/NO. HSMIMP; DWG NO AHSA-10; REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL FROD	8.2.77

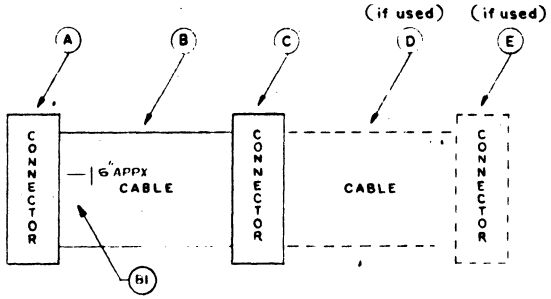
(CINCH) CONNECTOR A PIN NO.	WIRE COLOR B	(AMPHENOL) CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
9	GRN	13									
10	WHT	14									
11	YEL	12									
12	WHT	11									
13	ORN	7									
32	WHT	8									
15	RED	5									
33	WHT	6									
19	BRN	3									
37	WHT	4									
17	BLK	1									
35	WHT	2									
1	GRY	17									
20	WHT	18									
6	VIO	19									
25	WHT	20									
8	BLU	23									
27	WHT	24									
7	GRN	21									
26	WHT	22									

DISTANT HOST ADAPTER CABLE

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	7/25/77	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	[illegible]	8/4/77	CUSTOMER/NO. HSMIMP; DWG NO. AHSA-11; REV A

CABLES

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77



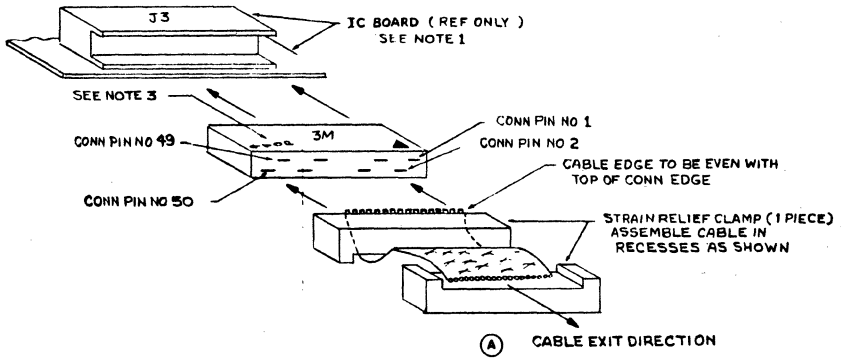
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	3M	3425-3000	442
B	(*)	25 TW-PAIR CABLE	WOVEN CABLE	T25TP2807-UL1227N	49
C	1	FEMALE CONN 25 P	CINCH	DB-25S	211
C1	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTOR'S
	NO. (SEE DWG DBRS-11) PLF ONLY
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
3	USING STAMP (SCD-0002), STAMP PAD (SCD-0003) MARK (ON PIN 50 END
	OF CONN) AS SHOWN WITH WHITE INK (SCD-0004)

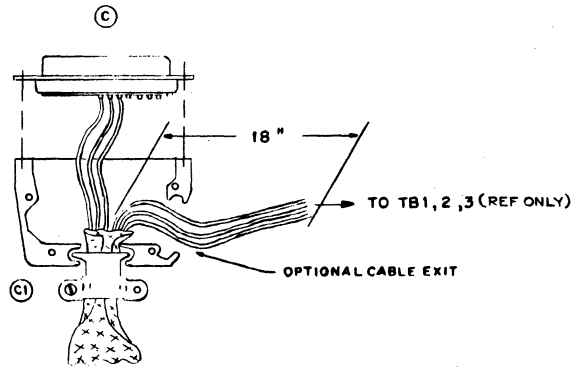
CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	4 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED



CABLE FUNCTION	
FROM A	KGB
TO C	FILTER BOX PNL
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	11/28/77	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED					
APPROVED	AEL	11/28/77	CUSTOMER/NO. HSMIMP	DWG NO. DBRS-10	REV A

APP'D	REVISION SYM	DESCR	DATE
	A	REL PROD	11.28.77

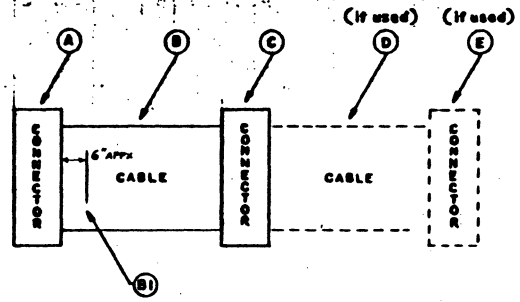
3M CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used ~~CONNECTOR E~~ TERMINALS ~~PIN NO.~~ (REF ONLY)	NOTES SIG. NAME	3M CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used ~~CONNECTOR E~~ TERMINALS ~~PIN NO.~~ (REF ONLY)	NOTES SIG NAMES
1	BROWN / WHITE	1			XFCW	31	PURPLE / WHITE			TB3-2	ISO12-
2		14			GND	32				TB3-4	ISO13-
3	RED / WHITE	2			RBW0-	33	GRAY / WHITE			TB3-6	GND-C
4		15			GND	34				TB3-8	ISO15-
5	ORANGE / WHITE	3			RBW1-	35	BLACK / WHITE			TB3-11	GND-C
6		16			GND	36				TB2-11	GND-B
7	YELLOW / WHITE	4			RBW2-	37	BROWN / WHITE			TB1-11	GND-A
8		17			GND	38				TB1-11	GND-A
9	GREEN / WHITE	5			RBW3-	39	RED / WHITE			TB3-12	ISOYY
10		18			GND	40				TB3-11	GND-C
11	BLUE / WHITE	6			RBW4-	41	ORANGE / WHITE	N.C.	DO NOT CUT SHORT	N.C.	
12		19			GND	42		N.C.		N.C.	
13	PURPLE / WHITE	7			RBW5-	43	YELLOW / WHITE	10			B2RWE+
14		20			GND	44		23			GND
15	GRAY / WHITE	8			RBW6-	45	GREEN / WHITE	11			RRFR-
16		21			GND	46		24			GND
17	BLACK / WHITE	9			RBW7-	47	BLUE / WHITE	12			RBBR-
18		22			GND	48		25			GND
19	BROWN / WHITE			TB1-2	ISO00-	49	PURPLE / WHITE			TB3-10	ISOXX
20				TB1-4	ISO01-	50				TB3-9	GND
21	RED / WHITE			TB1-6	ISO02-						
22				TB1-8	ISO03-						
23	ORANGE / WHITE			TB1-10	ISO04-						
24				TB1-12	ISO05-						
25	YELLOW / WHITE			TB2-2	ISO06-						
26				TB2-4	ISO07-						
27	GREEN / WHITE			TB2-6	ISO08-						
28				TB2-8	ISO09-						
29	BLUE / WHITE			TB2-10	ISO10-						
30				TB2-12	ISO11-						

CABLES

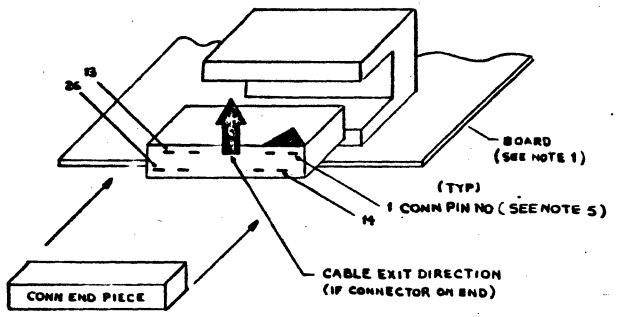
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF 12/30/76	TITLE	CABLE RUN-LIST	
CHECKED				
APPROVED	ABL 11/28/77	CUSTOMER/NO. HSMIMP	DWG NO. DBRS-11	REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7/27/76
	B	ECN 0127	11.14.77
DCF	C	ECN 0230	4.9.78
	D	ECN 0325	9.21.78
	E	ECN 0342	1.9.79
	F	ECN 0356	2.8.79



PIN NUMBERING & ASSEMBLY DETAILS



CONN Ⓐ & Ⓒ
VIEW FROM BACK
(UNASSEMBLED)

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	AMP	86905-2	47
	OR	FEMALE CONN	ANSLEY	609-3430	1687
		STRAIN RELIEF ASSY	ANSLEY	609-3431	1688
B	(*)	13PR TWIST'N'FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
C	1	FEMALE CONN	AMP	86905-2	47
	OR	FEMALE CONN	ANSLEY	609-3430	1687
		STRAIN RELIEF ASSY	ANSLEY	609-3431	1688
D	(*)	13PR TWIST'N'FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
E	1	FEMALE CONN	CINCH	DC-37S	148
E1	2	SPRING LATCH	CANNON	D110277	368
E2	1	PLASTIC BACK SHELL	AMPHENOL	17-1373	155
E3	2	4-40X1/2 PHM SCREW	LEHIGH METALS	—	336
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM-CP	366

SEE NOTE 3

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTORS,
	(3399) EX: #1 ON CONN = #13 ON BOARD.
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
3	DO NOT USE SCREWS SUPPLIED WITH THIS UNIT, INSTEAD USE E3 FOR ASSY
4	STRIP BRN/TAN PAIR OF CABLE, PRIOR TO ASSY
5	REMOVE 1ST PR BRN/TAN WIRES FROM CABLE, START CABLE AT PINS 2 & 15

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT	5 FT	ACTUALLY 1.10 FT LENGTH UNBROKEN CUT CABLE TO LENGTH IN MIDDLE OF FLAT AREA

CABLE FUNCTION	
FROM A	HLC
TO C	HLC
TO E	FANTAIL (HOST)

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	6/4/79
CHECKED	[illegible]	[illegible]
APPROVED	[illegible]	7/24/79

TITLE: CABLE ASSEMBLY DETAILS

CUSTOMER/NO.	DWG NO.	REV
HSMIMP	DHLD-10	F

REVISION			
APPD	SYM	DESCN	DATE
	A	REL PROD	9/20/78
	B	ECN 0342	1.9.79

CINCH

CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO's		CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
13 (1)	ORN/TAN	13 (1)	ORN/TAN	1	1	RFNIB+						
26 (14)		26 (14)		20	1	GND						
12 (2)	RED/TAN	12 (2)	RED/TAN	2	2	TYIMB						
25 (15)		25 (15)		21	2	GND						
11 (3)	BRN/TAN	11 (3)	BRN/TAN	3	3	LIBIT						
24 (16)		24 (16)		22	3	GND						
10 (4)	BLK/TAN	10 (4)	BLK/TAN	4	4	IMDTA						
23 (17)		23 (17)		23	4	GND						
9 (5)	WHT/TAN	9 (5)	WHT/TAN	5	5	RFNHB						
22 (18)		22 (18)		24	5	GND						
8 (6)	GRY/TAN	8 (6)	GRY/TAN	6	6	TYHBx						
21 (19)		21 (19)		25	6	GND						
7 (7)	VIO/TAN	7 (7)	VIO/TAN	7	7	LHBIT						
20 (20)		20 (20)		26	7	GND						
6 (8)	BLU/TAN	6 (8)	BLU/TAN	8	8	HSDTA						
19 (21)		19 (21)		27	8	GND						
5 (9)	GRN/TAN	5 (9)	GRN/TAN	9	9	XMTOT						
18 (22)		18 (22)		28	9	GND						
4 (10)	YEL/TAN	4 (10)	YEL/TAN	10	10	XMTXM						
17 (23)		17 (23)		29	10	GND						
3 (11)	ORN/TAN	3 (11)	ORN/TAN	11	11	HMRDY						
16 (24)		16 (24)		30	11	GND						
2 (12)	RED/TAN	2 (12)	RED/TAN	12	12	HRDYT						
15 (25)		15 (25)		31	12	GND						

NUMBERS ENGRAVED ON CONNECTOR BODY (TYP)

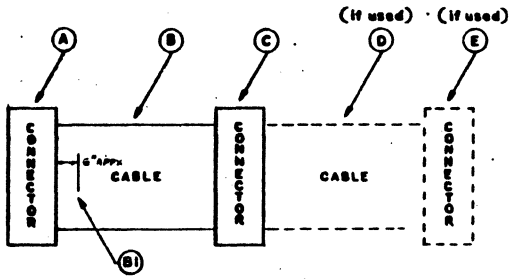
IC BOARD (TYP) PIN NO'S (REF)

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/15/78	TITLE	CABLE RUN-LIST	
CHECKED	KK	7/24/79	CUSTOMER/NO.	DWG NO.	REV
APPROVED	QK	7/24/79	HSMIMP	DHLD-11	B

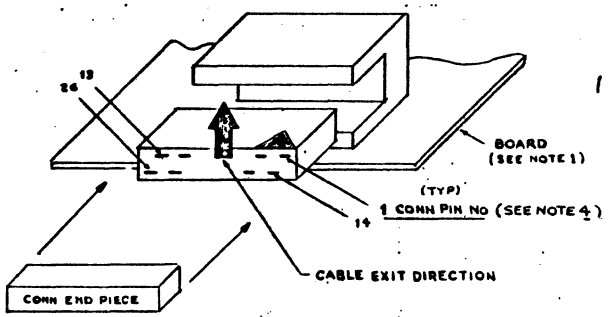
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	1.29.74
	B	ECN 0127	1.27.75
	C	ECN 0148	6.16.75
	D	ECN 0230	10.9.76
	E	ECN0325	9.21.78
	F	ECN0347	1.10.79
	G	ECN0356	2.8.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	AMP	86905-2	47
	-OR-	FEMALE CONN	ANSLEY	609-2630	1689
		STRAIN RELIEF ASSY	ANSLEY	609-2631	1690
B	(*)	13 PR TWIST'N'FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
C	1	FEMALE CONN	CINCH	DC 37S	148
C1	2	SPRING LATCH	CANNON	D-110277	368
C2	1	PLASTIC BACK SHELL	AMPHENOL	17-1373	155
C3	2	4-40 x 1/2 PHM SCREW	LEHIGH METALS	-	336
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

SEE NOTE 3

PIN NUMBERING & ASSEMBLY DETAILS



CONN (A)
VIEW FROM BACK
(UNASSEMBLED)

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTOR
	(3399) EX: #1 ON CONN = #13 ON BOARD
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
3	DO NOT USE SCREWS SUPPLIED WITH THIS UNIT. INSTEAD USE C3 FOR ASSY
4	REMOVE 1ST PR BRN/TAN WIRES FROM CABLE, START CABLE AT PINS 2 & 15

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		CUT CABLE TO LENGTH IN MIDDLE OF FLAT AREA

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	HLC1	DRAWN	DRF	2.11.74	TITLE	CABLE ASSEMBLY DETAILS
TO C	FANTAIL (HOST)	CHECKED	[illegible]	2/5/74	CUSTOMER/NO.	DWG NO. / REV
TO E		APPROVED	[illegible]	2/11/74	HSMIMP	DHLS-10 / G

APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	1.24.79
	B	ECN 0347	1.10.79

CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO'S	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
13 (1)	ORN	1			1 RFNIB+						
26 (14)	TAN	20			1 GND						
12 (2)	RED	2			2 TYIMB						
25 (15)	TAN	21			2 GND						
11 (3)	BRN	3			3 LIBIT						
24 (16)	TAN	22			3 GND						
10 (4)	BLK	4			4 IMDTA						
23 (17)	TAN	23			4 GND						
9 (5)	WHT	5			5 RFNHB						
22 (18)	TAN	24			5 GND						
8 (6)	GRY	6			6 TYHBX						
21 (19)	TAN	25			6 GND						
7 (7)	VIO	7			7 LHBIT						
20 (20)	TAN	26			7 GND						
6 (8)	BLU	8			8 HSDTA						
19 (21)	TAN	27			8 GND						
5 (9)	GRN	9			9 XMTOT						
18 (22)	TAN	28			9 GND						
4 (10)	YEL	10			10 XMTXN						
17 (23)	TAN	29			10 GND						
3 (11)	ORN	11			11 HMRDY						
16 (24)	TAN	30			11 GND						
2 (12)	RED	12			12 HRDYT						
15 (25)	TAN	31			12 GND						

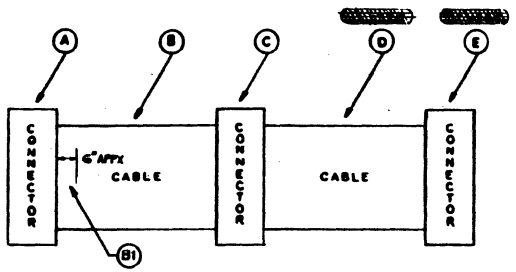
NUMBERS ENGRAVED ON CONNECTOR BODY (TYP)

IC BOARD (TYP) PIN NO'S (REF)

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	8/13/74	TITLE: CABLE RUN-LIST
CHECKED	LHK	8/14/74	CUSTOMER/NO.: HSMIMP; DWG NO.: DHLS-11; REV: B
APPROVED	D-K	8/14/74	

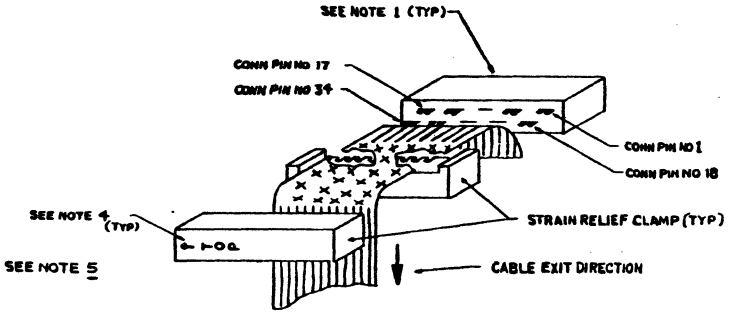
	REVISION		
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.28.77
	B	ECN 0310	2.14.78
	C	ECN 0325	4.3.78
	D	ECN 0349	6.10.79
	E	ECN 0356	7.8.79



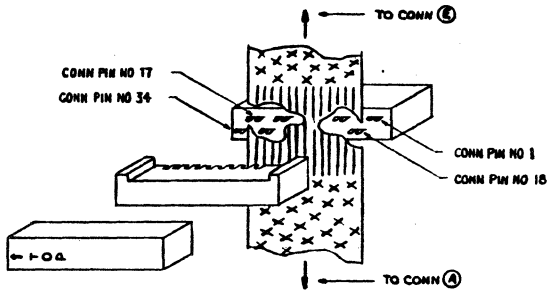
PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	CINCH	DC 375	148
A1	1	PLASTIC BACK SHELL	AMPHENOL	17-1373	155
A2	2	SPRING LATCH	CANNON	D-110277	368
A3	2	4-40X1/2 PHM SCREW	LEHIGH METALS	—	336
B	*	17PR TWIST'N'FLAT CABLE	SPECTRA-STRIP	455-248-34	1658
C	1	FEMALE CONN	AMP	86987-2	522
	OR	FEMALE CONN	ANSLEY	609-3430	1687
		STRAIN RELIEF ASSY	ANSLEY	609-3431	1688
D	(*)	17PR TWIST'N'FLAT CABLE	SPECTRA-STRIP	455-248-34	1658
E	1	FEMALE CONN	AMP	86987-2	522
	OR	FEMALE CONN	ANSLEY	609-3430	1687
		STRAIN RELIEF ASSY	ANSLEY	609-3431	1688
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM-CP	366

SEE NOTE 5



CONN (E) ONLY, VIEW FROM CABLE SIDE (UNASSEMBLED)



CONN (C) ONLY, VIEW FROM CABLE SIDE (UNASSEMBLED)

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTOR (3414)
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH IDELIBLE FELT-TIP PEN (BLK)
3	SCREWS CONNECTING AEA1 TO BE FROM 'AMP' CONNECTOR PACKAGE
4	USING STAMP (SCD-0002), STAMP PAD (SCD-0003), MARK ON END PIECE OF CONN AS SHOWN (PINS 17 & 34 END) WITH WHITE INK (SCD-0004)
5	DO NOT USE SCREWS SUPPLIED WITH THIS UNIT, INSTEAD USE A3 FOR ASSY

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT	5 FT	ACTUALLY 1 CONTINUOUS CABLE, CUT CABLE TO LENGTH IN MIDDLE OF FLAT AREA

CABLE FUNCTION	
FROM A	FANTAIL (HOST)
TO C	HST
TO E	HST

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	3/29/77	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			CUSTOMER/NO.: HSMIMP
APPROVED	[illegible]	3/31/77	DWG NO.: DHSD-10
			REV: E

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.25.77
J.J.	B	ECN 0349	1.10.79

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
9	YEL / TAN	14 (41-1)	YEL / TAN	14 (41-1)	XMTOT						
10		31 (41-2)		31 (41-2)	XMTXN						
11	ORN / TAN	13 (42-1)	ORN / TAN	13 (42-1)	HMRDY						
12		30 (42-2)		30 (42-2)	HRDYT						
13	RED / TAN	12 (43-1)	RED / TAN	12 (43-1)	RFNBV+						
32		29 (43-2)		29 (43-2)	RFNBV-						
15	BRN / TAN	11 (44-1)	BRN / TAN	11 (44-1)	TYIMV+						
33		28 (44-2)		28 (44-2)	TYIMV-						
19	BLK / TAN	10 (45-1)	BLK / TAN	10 (45-1)	IMDTV+						
37		27 (45-2)		27 (45-2)	IMDTV-						
17	WHT / TAN	9 (46-1)	WHT / TAN	9 (46-1)	LIBIV+						
35		26 (46-2)		26 (46-2)	LIBIV-						
1	GRY / TAN	8 (47-1)	GRY / TAN	8 (47-1)	RFNIB+						
20		25 (47-2)		25 (47-2)	RFNIB-						
6	VIO / TAN	7 (48-1)	VIO / TAN	7 (48-1)	TYHBX+						
25		24 (48-2)		24 (48-2)	TYHBX-						
8	BLU / TAN	6 (49-1)	BLU / TAN	6 (49-1)	HSDTA+						
27		23 (49-2)		23 (49-2)	HSDTA-						
7	GRN / TAN	5 (50-1)	GRN / TAN	5 (50-1)	LHBIT+						
26		22 (50-2)		22 (50-2)	LHBIT-						
2	YEL / TAN	4 (51-1)	YEL / TAN	4 (51-1)	TYIMB						
21		21 (51-2)		21 (51-2)	GND						
5	ORN / TAN	3 (52-1)	ORN / TAN	3 (52-1)	RFNHB						
24		20 (52-2)		20 (52-2)	GND						
4	RED / TAN	2 (53-1)	RED / TAN	2 (53-1)	IMDTA						
23		19 (53-2)		19 (53-2)	GND						
3	BRN / TAN	1 (54-1)	BRN / TAN	1 (54-1)	LIBIT						
22		18 (54-2)		18 (54-2)	GND						

NO'S ENGRAVED ON CONN BODY

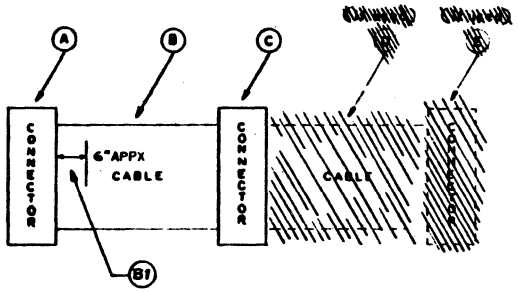
IC CARD PIN NO'S (REF)

CABLES

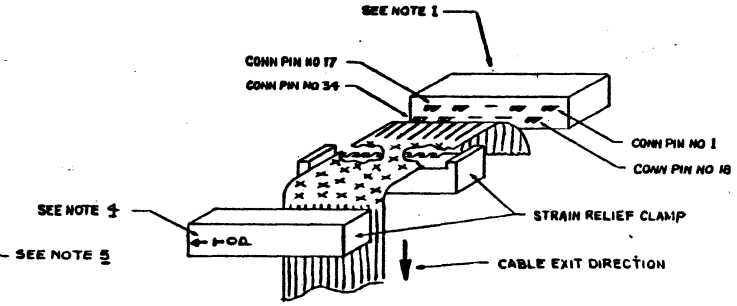
COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	S.E.T.	8.25.76	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	MAN	7/25/77	CUSTOMER/NO. HSMIMP; DWG NO. DHSD-11; REV B

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	7.25.77
	B	ECN0325	11.21.78
	C	ECN0348	1.10.79
	D	ECN0356	2.8.79



PIN NUMBERING & ASSEMBLY DETAILS



CONN (C) ONLY, VIEW FROM CABLE SIDE (UNASSEMBLED)

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	CINCH	DC-37S	148
A1	1	PLASTIC BACK SHELL	AMPHENOL	17-1373	155
A2	2	SPRING LATCH	CANNON	D-110277	368
A3	2	4-40x1/2 PHM SCREW	LEHIGH METALS	——	336
B	(*)	17 PR TWIST'N FLAT CABLE	SPECTRA-STRIP	455-248-34	1658
C	1	FEMALE CONN	AMP	86987-2	522
	OR	FEMALE CONN	ANSLEY	609-3430	1687
		STRAIN RELIEY ASSY	ANSLEY	609-3431	1688
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLFIM-CP	366

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTOR (3414)
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
3	SCREWS CONNECTING A & A1 TO BE FROM 'AMP' CONNECTOR PACKAGE
4	USING STAMP (SCD-0002), STAMP PAD (SCD-0003) MARK ON END PIECE OF CONN AS SHOWN (PINS 17 & 34 END) WITH WHITE INK (SCD-0004)
5	DO NOT USE SCREWS SUPPLIED WITH THIS UNIT, INSTEAD USE A3 FOR ASSY

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		CUT CABLE TO LENGTH IN MIDDLE OF FLAT AREA

CABLE FUNCTION	
FROM A	FANTAIL (HOST)
TO C	HST
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	4/7/77	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED					
APPROVED	MAW	7/25/77	CUSTOMER/NO. HSMIMP	DWG. NO. DHSS-10	REV D

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.25.77
	B	ECN 0348	1.10.79

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
9	YEL	14 (41-1)			XMTOT						
10	TAN	31 (41-2)			XMTXN						
11	ORN	13 (42-1)			HMRDY						
12	TAN	30 (42-2)			HRDYT						
13	RED	12 (43-1)			RFNBV+						
32	TAN	29 (43-2)			RFNBV-						
15	BRN	11 (44-1)			TYIMV+						
33	TAN	28 (44-2)			TYIMV-						
19	BLK	10 (45-1)			IMDTV+						
37	TAN	27 (45-2)			IMDTV-						
17	WHT	9 (46-1)			LIBIV+						
35	TAN	26 (46-2)			LIBIV-						
1	GRY	8 (47-1)			RFNIB+						
20	TAN	25 (47-2)			RFNIB-						
6	VIO	7 (48-1)			TYHBX+						
25	TAN	24 (48-2)			TYHBX-						
8	BLU	6 (49-1)			HSDTA+						
27	TAN	23 (49-2)			HSDTA-						
7	GRN	5 (50-1)			LHBIT+						
26	TAN	22 (50-2)			LHBIT-						
2	YEL	4 (51-1)			TYIMB						
21	TAN	21 (51-2)			GND						
5	ORN	3 (52-1)			RFNNB						
24	TAN	20 (52-2)			GND						
4	RED	2 (53-1)			IMDTA						
23	TAN	19 (53-2)			GND						
3	BRN	1 (54-1)			LIBIT						
22	TAN	18 (54-2)			GND						

NO'S ENGRAVED ON CONN BODY

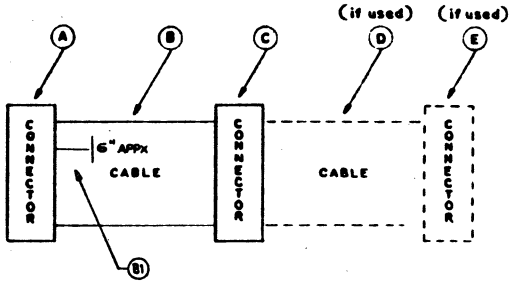
IC CARD PIN NO'S (REF)

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	4.3.77	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	(illegible)	7/25/77	CUSTOMER/NO. HSMIMP; DWG NO. DHSS-11; REV B

CABLES

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	8.18.77
	B	ECN 0344	1.9.79
	C	ECN 0356	2.8.79



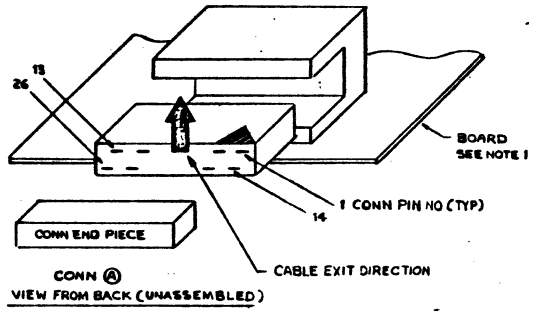
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	AMP	86905-2	47
	OR	FEMALE CONN	ANSLEY	609-2630	1689
		STRAIN RELIEF ASSY	ANSLEY	609-2631	1690
B	(*)	13PRTWIST'N'FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
C	1	FEMALE CONN	WINCHESTER ELECTRONICS	PGB-13A	1112
C1	10	CRIMP CONTACT (PIN)	WINCHESTER ELECTRONICS	100-71126S	1481
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM CONN/3399) EX: #1 (CONN) = #13 (BOARD)
2	THE WIRE WRAP PIN NUMBERING SYSTEM DIFFERS FROM CONN (PGB) (C)
	EX: #1 ON CONN (C) = #7 ON WIREWRAP PIN CONN (DYNATECH)
3	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
4	USING STAMP (SCD-0002), STAMP PAD (SCD-0003) MARK AS SHOWN
	WITH WHITE INK (SCD-0004)
5	PINS 1 & 25 TO BE MARKED AS SHOWN, WITH INDELIBLE FELT-TIP PEN (BLK)

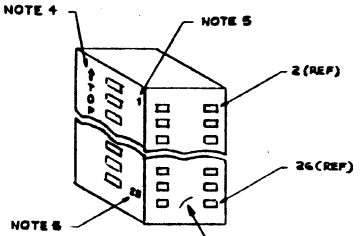
CABLE LENGTH

	TYPE	B	D	NOTES
*	-A	80"		CUT CABLE TO LENGTH IN MIDDLE OF FLAT AREA

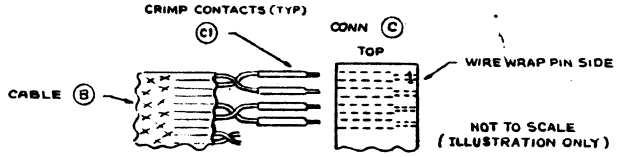
PIN NUMBERING & ASSEMBLY DETAILS



CONN (A)
VIEW FROM BACK (UNASSEMBLED)



CONN (C)



ASSEMBLY INSTRUCTIONS

1- CRIMP CONTACT PINS TO CABLE WIRES PER DWG DILS-11 USING A CRIMPING TOOL (WINCHESTER # 107-0525 or equiv)

2- INSERT PINS INTO CONN 'C' (SNAP FIT) PER DWG DILS-11

CABLE FUNCTION	
FROM A	MLR
TO C	ILC
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/4/77	TITLE	CABLE ASSEMBLY DETAILS		
CHECKED	AT	8/18/77	CUSTOMER/NO.	DWG NO.	REV	
APPROVED	AT	8/18/77	HSMIMP	DILS-10	C	

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.16.77
	B	ECN 0344	1.9.79

CONNECTOR A PIN NO.	WIRE COLOR B	WINCHESTER CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES SIG NAMES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
13 (1)	ORN	N.C.									
26 (14)	TAN	N.C.									
12 (2)	RED	N.C.									
25 (15)	TAN	N.C.									
11 (3)	BRN	1			TDATA+ (MXDLD)						
24 (16)	TAN	2			GND						
10 (4)	BLK	3			TLOOP+ (MXPLD)						
23 (17)	TAN	4			GND						
9 (5)	WHT	5			TCLK + (MXCLR)						
22 (18)	TAN	6			GND						
8 (6)	GRY	7			RDATA+ (MRDLR)						
21 (19)	TAN	8			GND						
7 (7)	VIO	9			RCLK + (MRCLR)						
20 (20)	TAN	10			GND						
6 (8)	BLU	N.C.									
19 (21)	TAN	N.C.									
5 (9)	GRN	N.C.									
18 (22)	TAN	N.C.									
4 (10)	YEL	N.C.									
17 (23)	TAN	N.C.									
3 (11)	ORN	N.C.									
16 (24)	TAN	N.C.									
2 (12)	RED	N.C.									
15 (25)	TAN	N.C.									
1 (13)	BRN										
14 (26)	TAN										

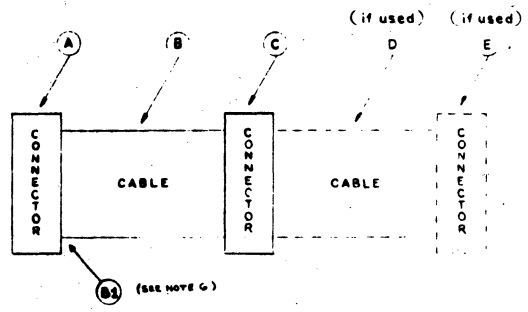
IC BOARD (TYP) PIN NO'S (REF ONLY)

NUMBERS ENGRAVED ON CONNECTOR BODY (TYP)

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	5/27/77	TITLE: CABLE RUN-LIST
CHECKED	AT	6/16/77	CUSTOMER/NO.: HSMIMP; DWG NO.: DILS-11; REV: B
APPROVED	AT	6/16/77	

REVISION			
APPD	SYM	DESCR	DATE
	A	RCL PROD	5.8.75



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN I/O CONNECTOR	CANNON	121-7326-11Ø	2Ø9
A1	20	PINS FOR 2Ø9	CANNON	Ø3Ø-7312-Ø11	21Ø
B	*	18 TW PAIR	ALPHA	1327	356
			OR BELDEN	8749	356
B1	1	NAME TAGE TIE WRAP	PANDUIT	PLF 1M CP	366
C	1	RT ANGLE CONN	CANNON/CINCH	MS 3108B-28-12S	420
C1	1	CABLE CLAMP ADAPTER	CANNON/CINCH	CA-2265-10	421

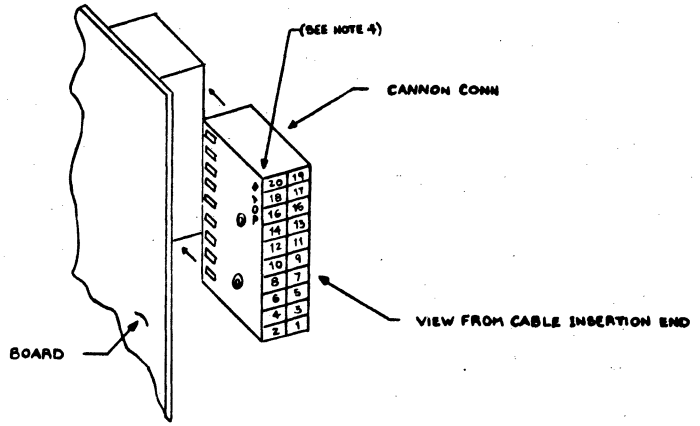
ASSEMBLY NOTES

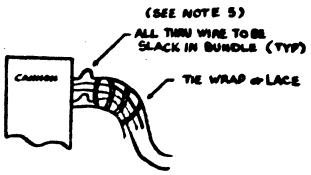
1. AT C, SLIDE CABLE CLAMP C1 OVER CABLE END BEFORE SOLDERING PINS
2. WRAP OR TAPE CABLE AT C1 TO PROVIDE STRAIN RELIEF
3. AT A CRIMP PINS A1 WITH CANNON CRIMPER # CCT-UBC
4. USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 19 END OF CONN) AS SHOWN WITH WHITE INK (SCD-0004)
5. LEAVE SLACK IN WIRE FOR STRAIN RELIEF AS SHOWN
6. CABLE TYPE & SIN TO BE MARKED ON B1 WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

TYPE	B	D	NOTES
A	5 FT		

PIN NUMBERING & ASSEMBLY DETAILS





CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	KGB CARD	DRAWN	B.E.T.	5/29/75	TITLE	CABLE ASSEMBLY DETAILS	
TO C	OPTICAL ISOLATOR CONNECTOR BOX	CHECKED					
TO E		APPROVED	D.M.	5/29/75	CUSTOMER/NO. PLI-1	DWG NO. DKGB-10	REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	5.29.75

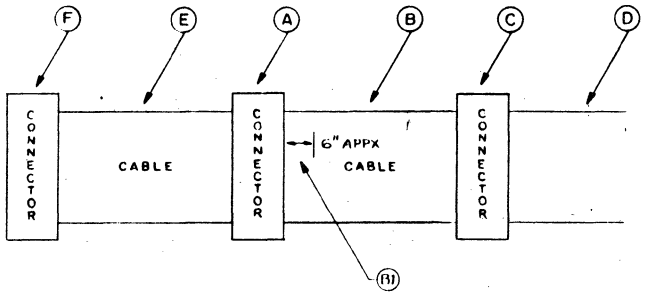
3M CONNECTOR A PIN NO.	WIRE COLOR B	MS 3108 CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1	BLK/	A									
2	/RED	B									
3	BLK/	C									
4	/WHT	D									
5	BLK/	E									
6	/GRN	F									
7	BLK/	G									
8	/BLU	H									
9	BLK/	J									
10	/BRN	K									
11	BLK/	L									
12	/YEL	M									
13	BLK/	N									
14	/ORG	P									
15	RED/	R									
16	/GRN	S									
17	RED/	T									
18	/WHT	U									
19	RED/	V									
20	/WHT	W									

OTHER WIRES NOT USED

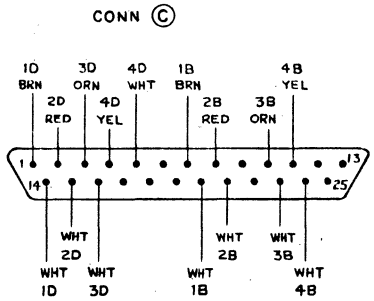
CABLES

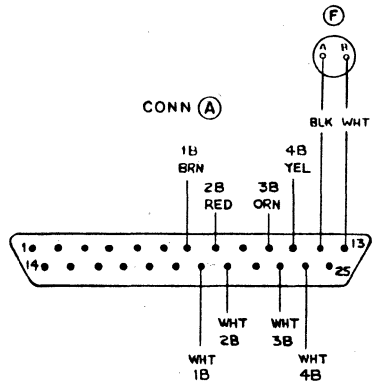
COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	S.E.T	5/30/75	TITLE	CABLE RUN-LIST
CHECKED				
APPROVED	D.M	5/30/75	CUSTOMER/NO. PLI-1	DWG NO. DKGB-11 REV A

	REVISION		
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77

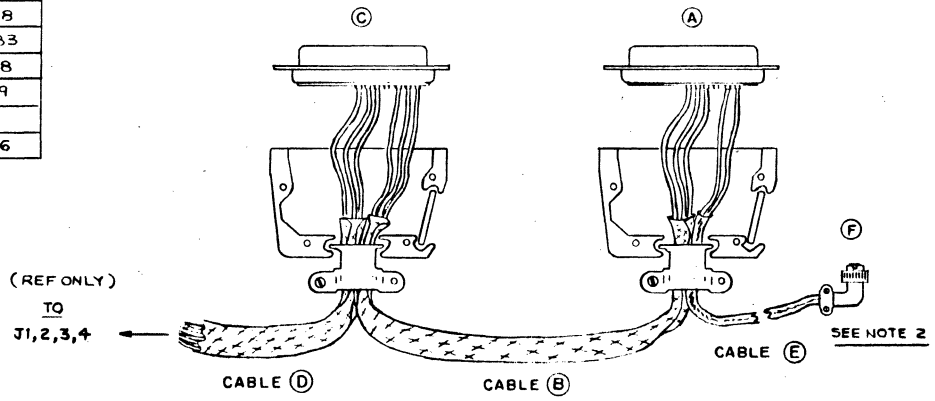


PIN NUMBERING & ASSEMBLY DETAILS





SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN, 25 PIN	CINCH	DB-25 S	211
A1	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526
A2	2	SPRING LATCH	CANNON	D-110277	368
B	*	4 TW-PAIR CABLE	WOVEN	T4TP-2807UL-1227	208
C	1	MALE CONN, 25 PIN	CINCH	DB-25P	353
C1	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526
C2	2	DISC LATCH	CANNON	D110278	367
D	*	4 TW PAIR CABLE	WOVEN	T4TP-2807UL-1227	208
E	*	2 TW-PAIR CABLE	ALPHA or BELDEN	1317 or 9744	383
F	1	RT ANGEL CONN	CANNON or CINCH	MS-3108B-125-3S	418
F1	1	CABLE CLAMP ADAPT	CANNON or CINCH	AN 3057-4	419
B1	1	NAME TAG TIE WRAP	PANDUIT	PLF 1M CP	366



ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	WRAP OR TAPE CABLE UNDER CLAMP TO PROVIDE STRAIN RELIEF,
	TAPE OR TIE BACK UNUSED TW-PAIR INSIDE SHELL OF (F)

CABLE LENGTH

	TYPE	B	D	E	
(*)	A	10"	15"	5 FT	

CABLE FUNCTION	
FROM A	BLK FANTAIL PNL (J6)
TO C	BLK FANTAIL PNL (J5)
TO F	FILTER BOX (J9)

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	11/27/77	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED	ABL	11/28/77	CUSTOMER/NO.: HSMIMP; DWG NO.: DKGC-10; REV: A

	REVISION		
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77

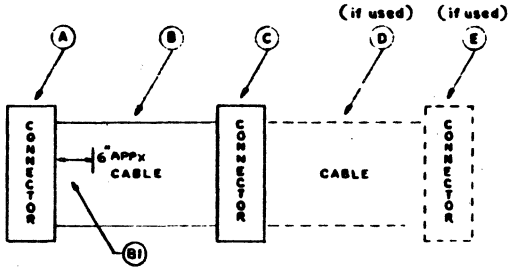
CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR F PIN NO.	NOTES (REF ONLY)	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
7	BRN	7			XLRM+						
20	WHT	20			GND						
8	RED	8			PWRON+						
21	WHT	21			GND						
10	ORN	10			KMIAR+						
23	WHT	23			GND						
11	YEL	11			KRPRP+						
24	WHT	24			GND						
		1	BRN		(J1) RCLK						
		14	WHT		GND						
		2	RED		(J2) RDATA						
		15	WHT		GND						
		3	ORN		(J3) TCLK						
		16	WHT		GND						
		4	YEL		(J4) TDATA						
		5	WHT		GND						
			E (CINCH)								
12			BLK	A	TPREP-						
13			WHT	B	GND						

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	11-27-77	TITLE	CABLE RUN-LIST
CHECKED				
APPROVED	ABL	11-28-77	CUSTOMER/NO. HSMIMP	DWG NO. DKGC-11 REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	1.28.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN CONN, FEMALE	ANSLEY	609-2030	1647
A1	1	STRAIN RELIEF CLAMP	ANSLEY	609-2031	1648
	OR	20 PIN CONN, FEMALE	AMP	86904-2	1660
B	*	20 WIRE FLAT CABLE	SPECTRA-STRIP	455-044-20	1646
C	1	25 PIN CONN, FEMALE	CINCH	DB25S	211
C1	1	PLASTIC CONN SHELL	AMP	205-781-1	1649
C2	2	FEMALE SCREW LOCK ASSY	CINCH	D20418-2	429
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM-CP	366

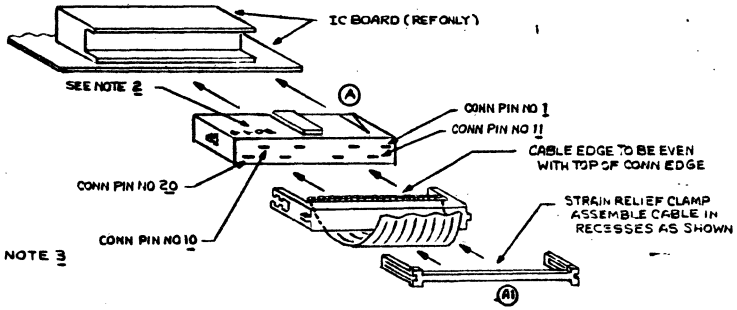
SEE NOTE 3

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	USING STAMP (SCD-0002), STAMP PAD (SCD-0003) MARK ON END PIECE OF CONN AS SHOWN (PINS 10 & 20 END) WITH WHITE INK (SCD-0004)
3	AMP CONN IS AN ALTERNATE REPLACEMENT FOR (A) & (A1) (STRAIN RELIEF CLAMP SUPPLIED WITH AMP CONN)

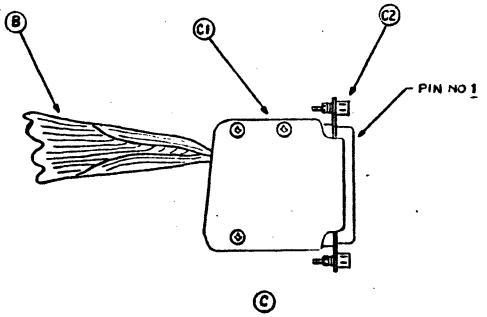
CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	3 FT		
	B	10 FT		
	C	20 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED



CABLE FUNCTION	
FROM A	ELI CARD
TO C	MODEM
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	11/78	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED			CUSTOMER/NO.	DWG NO.	REV
APPROVED	EYGC	11/79		DLCF-10	A

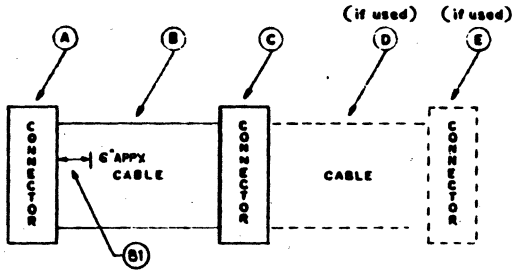
REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	1.29.79

CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1	BRN	3			LINE IN						
11	RED	N.C.									
2	ORG	4			MODCNT0						
12	YEL	20			+12V						
3	GRN	6			MODSTAT1						
13	BLU	1			PROT GND						
4	VIO	5			MODSTAT0						
14	GRY	N.C.									
5	WHT	19			MODCNT2						
15	BLK	N.C.									
6	BRN	2			LINEOUT						
16	RED	N.C.									
7	ORG	8			MODSTAT2						
17	YEL	N.C.									
8	GRN	NC									
18	BLU	N.C.									
9	VIO	14			MODCNT1						
19	GRY	N.C.									
10	WHT	12			MODSTAT3						
20	BLK	7			SIG GND						

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138				
DRAWN	DRF	1-78	TITLE	CABLE RUN-LIST
CHECKED			CUSTOMER NO.	DWG NO. DLCF-11 REV A
APPROVED	EYGC	1-31-79		

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	1.29.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN CONN, FEMALE	ANSLEY	609-2030	1647
A1	1	STRAIN RELIEF CLAMP	ANSLEY	609-2031	1648
	OR	20 PIN CONN FEMALE	AMP	86904-2	1660
B	(*)	20 WIRE FLAT CABLE	SPECTRA-STRIP	455-044-20	1646
C	1	25 PIN CONN, MALE	CINCH	DB25P	353
C1	1	PLASTIC CONN SHELL	AMP	205-718-1	1649
C2	2	JACK SCREW ASSY	CINCH	D20419-16	361
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

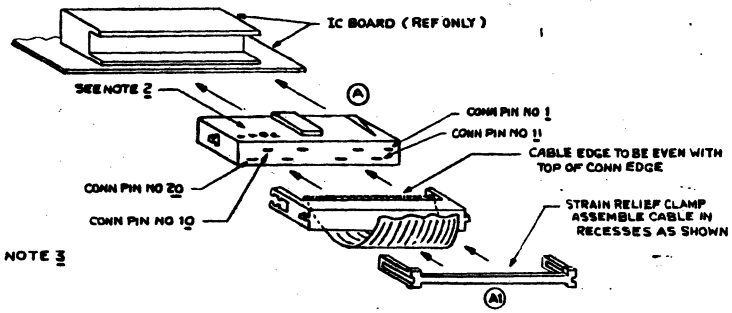
SEE NOTE 3

	ASSEMBLY NOTES
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	USING STAMP (SCD-0002), STAMP-PAD (SCD-0003), MARK ON END PIECE OF CONN AS SHOWN (PINS 10 & 20 END) WITH WHITE INK (SCD-0004)
3	AMP CONN IS AN ALTERNATE REPLACEMENT FOR (A) & (A1) (STRAIN RELIEF CLAMP IS SUPPLIED WITH AMP CONN).

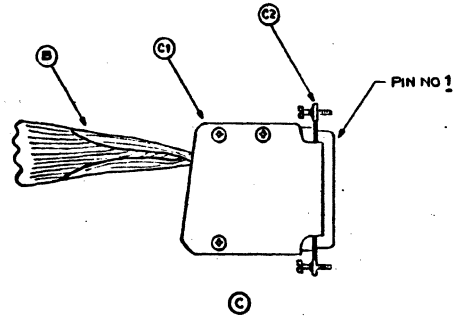
CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	3 FT		
	B	10 FT		
	C	20 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED



(C)

CABLE FUNCTION	
FROM A	ELI CARD
TO C	MODEM
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	10.13.78	TITLE: CABLE ASSEMBLY DETAILS
CHECKED	[signature]	9.14.78	CUSTOMER/NO.
APPROVED	EYGC	1.29.79	DWG NO. DLCM-10 REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	1.29.71

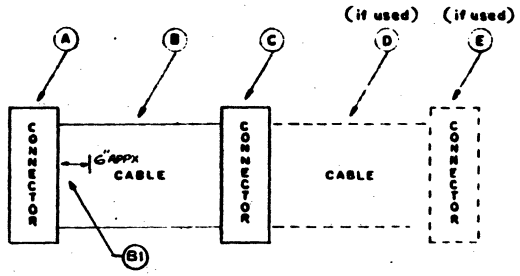
CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1	BRN	3			LINE IN						
11	RED	N.C									
2	ORG	4			MODCNTØ						
12	YEL	20			+12V						
3	GRN	6			MODSTAT1						
13	BLU	1			PROT GND						
4	VIO	5			MODSTATØ						
14	GRY	N.C.									
5	WHT	19			MODCNT2						
15	BLK	N.C.									
6	BRN	2			LINEOUT						
16	RED	N.C.									
7	ORG	8			MODSTAT2						
17	YEL	NC									
8	GRN	N.C									
18	BLU	N.C									
9	VIO	14			MODCNT1						
19	GRY	N.C									
10	WHT	12			MODSTAT3						
20	BLK	7			SIG GND						

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	12-13-70	TITLE	CABLE RUN-LIST	
CHECKED	[illegible]	1/4-71	CUSTOMER NO.	DWG NO. DLCM-11	REV A
APPROVED	EYGC	1-22-71			

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	1.29.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN CONN, FEMALE	ANSLEY	609-2030	1647
A1	1	STRAIN-RELIEF CLAMP	ANSLEY	609-2031	1648
	OR	20 PIN CONN, FEMALE	AMP	86904-2	1660
B	(*)	20 WIRE FLAT CABLE	SPECTRA-STRIP	455-044-20	1646
C	1	25 PIN CONN, FEMALE	CINCH	DB25S	211
C1	1	PLASTIC CONN SHELL	AMP	205-718-1	1649
C2	2	FEMALE SCREW LOCK ASSY	CINCH	D20418-2	429
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLFIM-CP	366

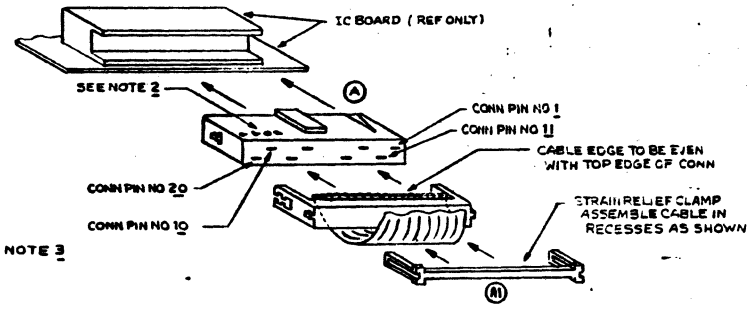
SEE NOTE 3

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	USING STAMP (SCD-0002), STAMP PAD (SCD-0003) MARK ON END PIECE OF CONN AS SHOWN (PINS 10 & 11 END) WITH WHITE INK (SCD-0004)
3	AMP CONN IS AN ALTERNATE REPLACEMENT FOR (A) & (A1) (STRAIN RELIEF CLAMP SUPPLIED WITH AMP CONN)

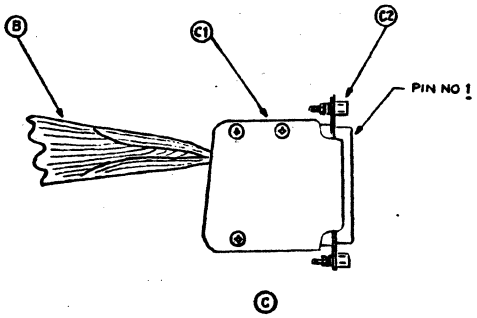
CABLE LENGTH

	TYPE	B	D	NOTES
*	A	3 FT		
	B	10 FT		
	C	20 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED



CABLE FUNCTION	
FROM A	ELI CARD
TO C	TERMINAL (RS232)
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	11.78	TITLE: CABLE ASSEMBLY DETAILS
CHECKED	[illegible]	11/29/78	
APPROVED	EYGC	11/29/78	CUSTOMER/NO.
			DWG NO. DLTF-10 REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	1.29.79

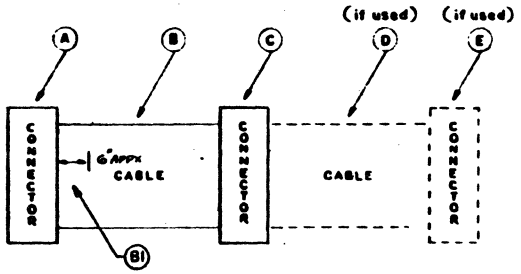
CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1	BRN	2			LINEIN						
11	RED	N.C.									
2	ORG	5			MODCNT0						
12	YEL	N.C.									
3	GRN	19			MODSTAT1						
13	BLU	1			PROT GND						
4	VIO	4			MODSTAT0						
14	GRY	N.C.									
5	WHT	6			MODCNT2						
15	BLK	N.C									
6	BRN	3			LINEOUT						
16	RED	N.C.									
7	ORG	20			MODSTAT2						
17	YEL	N.C.									
8	GRN	8			MODCNT3						
18	BLU	N.C.									
9	VIO	16			MODCNT1						
19	GRY	N.C									
10	WHT	12			MODSTAT3						
20	BLK	7			SIG GND						

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	11-1-78	TITLE: CABLE RUN-LIST
CHECKED	[illegible]	79	CUSTOMER NO. / DWG NO. DLTF-11 / REV A
APPROVED	EVGC	1-29-79	

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	1.29.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN CONN, FEMALE	ANSLEY	609-2030	1647
A1	1	STRAIN RELIEF CLAMP	ANSLEY	609-2031	1648
	OR	20 PIN CONN, FEMALE	AMP	86904-2	1660
B	*	20 WIRE FLAT CABLE	SPECTRA-STRIP	455-044-20	1646
C	1	25 PIN CONN, MALE	CINCH	DB25P	353
C1	1	PLASTIC CONN SHELL	AMP	205-718-1	1649
C2	2	JACK SCREW ASSY	CINCH	D20419-16	361
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

SEE NOTE 3

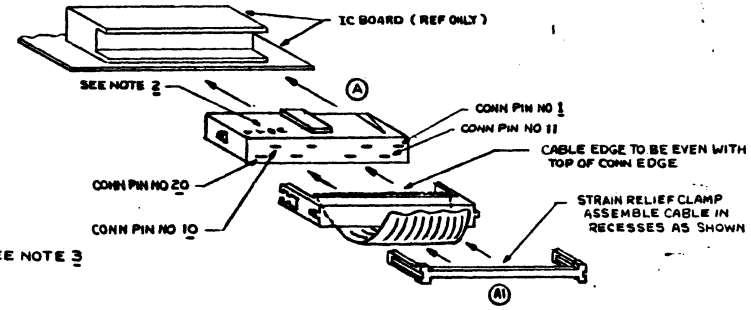
ASSEMBLY NOTES

1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	USING STAMP (SCD-0002), STAMP-PAD (SCD-0003), MARK ON END PIECE OF CONN AS SHOWN (PINS 10 & 20 END) WITH WHITE INK (SCD-0004)
3	AMP CONN IS AN ALTERNATE REPLACEMENT FOR (A) & (A1) (STRAIN RELIEF CLAMP IS SUPPLIED WITH AMP CONN)

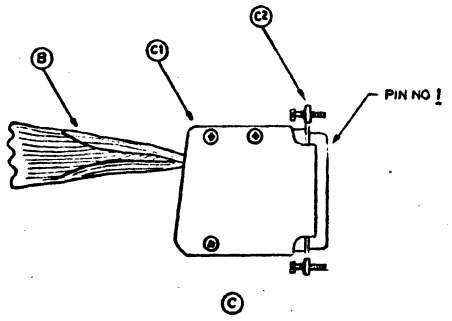
CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	3 FT		
	B	10 FT		
	C	20 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED



CABLE FUNCTION	
FROM A	ELI CARD
TO C	TERMINAL (RS232)
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	10/4/78	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED	[illegible]	5/14/79	CUSTOMER/NO.	DWG NO. DLTM-10	REV A
APPROVED	EYGC	1/29/79			

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	4.29.79

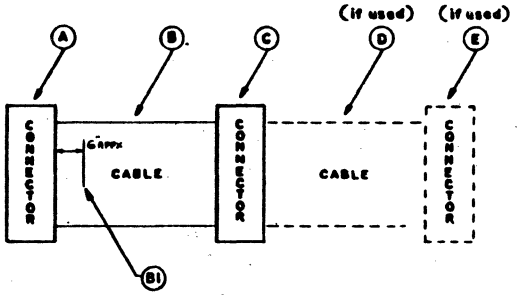
CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1	BRN	2			LINE IN						
11	RED	N.C.									
2	ORG	5			MODCNT0						
12	YEL	N.C.									
3	GRN	19			MODSTAT1						
13	BLU	1			PROT GND						
4	VIO	4			MODSTAT0						
14	GRY	N.C									
5	WHT	6			MODCNT2						
15	BLK	N.C.									
6	BRN	3			LINEOUT						
16	RED	N.C.									
7	ORG	20			MODSTAT2						
17	YEL	N.C									
8	GRN	8			MODCNT3						
18	BLU	N.C.									
9	VIO	16			MODCNT1						
19	GRY	N.C									
10	WHT	12			MODSTAT3						
20	BLK	7			SIG GND						

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	10/16/78	TITLE	CABLE RUN-LIST	
CHECKED	[illegible]	2/27	CUSTOMER/NO.	DWG NO. DLTM-11	REV A
APPROVED	EVGC	4/29/79			

	REVISION		
APPD	SYM	DESCR	DATE
	A	REL PROD	9.16.74
	B	ECN 0127	1.27.75
	C	ECN 0230	10.9.75
	D	ECN 0325	9.22.78
	E	ECN 0345	1.9.79
	F	ECN 0356	2.8.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	AMP	86905-2	47
	OR	FEMALE CONN	ANSLEY	609-2630	1689
		STRAIN RELIEF ASSY	ANSLEY	609-2631	1690
B	(*)	13PR TWIST 'N' FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
C	1	FEMALE CONN	AMP	86905-2	47
	OR	FEMALE CONN	ANSLEY	609-2630	1689
		STRAIN RELIEF ASSY	ANSLEY	609-2631	1690
D	(*)	13PR TWIST 'N' FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
E	1	MALE CONN	CINCH	DC 37P	149
E1	2	SPRING LATCH	CANNON	D-110277	368
E2	1	PLASTIC BACK SHELL	AMPHENOL	17-1373	155
E3	1	4-40 x 1/2 PHM SCREW	LEHIGH METALS	—	336
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM-CP	366

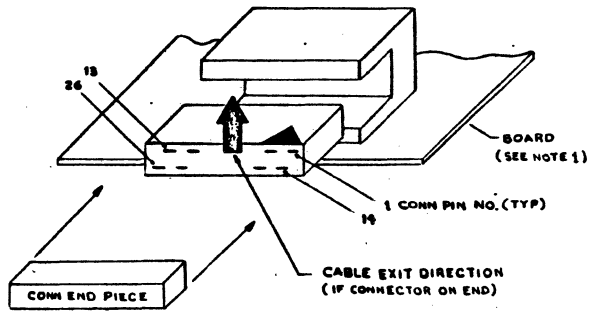
SEE NOTE 3

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTORS, (3399) EX: #1 ON CONN = #13 ON BOARD.
2	CABLE TYPE & SIZE TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
3	DO NOT USE SCREWS SUPPLIED WITH THIS UNIT, INSTEAD USE E3 FOR ASSY

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT	5 FT	ACTUAL 1, 10 FT I.G UNBROKEN, CUT CABLE TO LENGTH IN CENTER OF FLAT AREA

PIN NUMBERING & ASSEMBLY DETAILS



CONN (A) & (C)
VIEW FROM BACK
(UNASSEMBLED)

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	MLR	DRAWN	DRF	8/16/79	TITLE	CABLE ASSEMBLY DETAILS	
TO C	MLR	CHECKED					
TO E	FANTAIL (LOW SPEED MODEM)	APPROVED			CUSTOMER/NO. HSMIMP	DWG NO. DMLD-10	REV F

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.26.79
	B	ECN 0104	8.28.79
	C	ECN 0345	4.9.79

CINCH

CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO's	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
13 (1)	ORN / TAN	13 (1)	ORN / TAN	N.C.							
26 (14)		26 (14)		N.C.							
12 (2)	RED / TAN	12 (2)	RED / TAN	N.C.							
25 (15)		25 (15)		N.C.							
11 (3)	BRN / TAN	11 (3)	BRN / TAN	8	1 (SD) MXDLD						
24 (16)		24 (16)		27	1 GND						
10 (4)	BLK / TAN	10 (4)	BLK / TAN	11	2 (LT) MXPLD						
23 (17)		23 (17)		30	2 GND						
9 (5)	WHT / TAN	9 (5)	WHT / TAN	12	3 (SCT) MXCLR						
22 (18)		22 (18)		31	3 GND						
8 (6)	GRY / TAN	8 (6)	GRY / TAN	10	4 (RD) MRDLR						
21 (19)		21 (19)		29	4 GND						
7 (7)	VIO / TAN	7 (7)	VIO / TAN	6	5 (SCR) MRCLR						
20 (20)		20 (20)		25	5 GND						
6 (8)	BLU / TAN	6 (8)	BLU / TAN	N.C.							
19 (21)		19 (21)		N.C.							
5 (9)	GRN / TAN	5 (9)	GRN / TAN	N.C.							
18 (22)		18 (22)		N.C.							
4 (10)	YEL / TAN	4 (10)	YEL / TAN	N.C.							
17 (23)		17 (23)		N.C.							
3 (11)	ORN / TAN	3 (11)	ORN / TAN	N.C.							
16 (24)		16 (24)		N.C.							
2 (12)	RED / TAN	2 (12)	RED / TAN	N.C.							
15 (25)		15 (25)		N.C.							
1 (13)	BRN / TAN	1 (13)	BRN / TAN	N.C.	6						
14 (26)		14 (26)		32	6 GND						

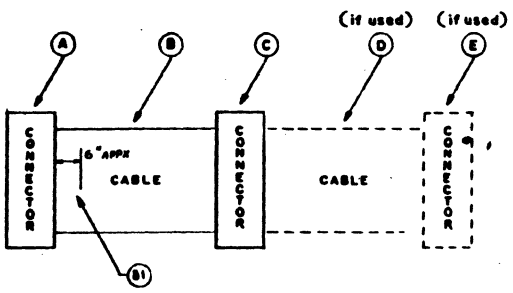
NUMBERS ENGRAVED ON CONNECTOR BODY (TYP)

IC BOARD (TYP) PIN NO'S (REF)

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	8/4/79	TITLE: CABLE RUN-LIST
CHECKED	DK	8/4/79	CUSTOMER/NO. HSMIMP
APPROVED	DK	8/4/79	DWG NO. DMLD-11 REV C

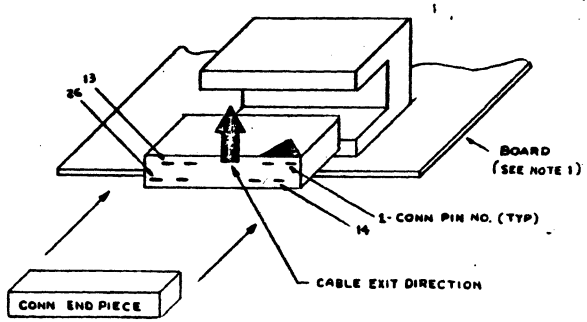
	REVISION		
APP'D	SYM	DESCR	DATE
	A	REL PROD	7.24.79
	B	ECN 0127	1.22.79
DRF	C	ECN 0230	4.9.79
	D	ECN 0325	7.22.79
	E	ECN 0343	8.9.79
	F	ECN 0356	2.8.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	AMP	86905-2	47
	OR	FEMALE CONN	ANSLEY	609-2630	1689
		STRAIN RELIEF ASSY	ANSLEY	609-2631	1690
B	(*)	13 PR TWIST 'N' FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
C	1	MALE CONN	CINCH	DC 37P	149
C1	2	SPRING LATCH	CANNON	D-110277	368
C2	1	PLASTIC BACK SHELL	AMPHENOL	17-1373	155
C3	2	4-40 x 1/2 PHM SCREW	LEHIGH METALS	—	336
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

SEE NOTE 3

PIN NUMBERING & ASSEMBLY DETAILS



CONN (A)
VIEW FROM BACK
(UNASSEMBLED)

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTOR
	(3399) EX: #1 ON CONN = #13 ON BOARD
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
3	DO NOT USE SCREWS SUPPLIED WITH THIS UNIT, INSTEAD USE C3 FOR ASSY

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		CUT CABLE TO LENGTH IN MIDDLE OF FLAT AREA

CABLE FUNCTION						
FROM A	MLR	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
TO C	FANTAIL (LOW SPEED MODEM)	DRAWN	DRF	6/15/79	TITLE: CABLE ASSEMBLY DETAILS	
TO E		CHECKED	OK	6/19/79	CUSTOMER/NO.: HSMIMP	DWG NO.: DMLS-10 REV: F
		APPROVED	OK	6/19/79		

APP		REVISION
	A	REL PROD (2.7.79)
	B	ECN0343 (4.9.79)
	C	ECN0356 (8.8.79)

CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO's	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
13 (1)	ORN	N.C.									
26 (14)	TAN	N.C.									
12 (2)	RED	N.C.									
25 (15)	TAN	N.C.									
11 (3)	BRN	8			1 (SD) MXDLD						
24 (16)	TAN	27			1 GND						
10 (4)	BLK	11			2 (LT) MXPLD						
23 (17)	TAN	30			2 GND						
9 (5)	WHT	12			3 (SCT) MXCLR						
22 (18)	TAN	31			3 GND						
8 (6)	GRY	10			4 (RD) MRDLR						
21 (19)	TAN	29			4 GND						
7 (7)	VIO	6			5 (SCR) MRCLR						
20 (20)	TAN	25			5 GND						
6 (8)	BLU	N.C.									
19 (21)	TAN	N.C.									
5 (9)	GRN	N.C.									
18 (22)	TAN	N.C.									
4 (10)	YEL	N.C.									
17 (23)	TAN	N.C.									
3 (11)	ORN	N.C.									
16 (24)	TAN	N.C.									
2 (12)	RED	N.C.									
15 (25)	TAN	N.C.									
1 (13)	BRN	N.C.			6						
14 (26)	TAN	32			6 GND						

NUMBERS ENGRAVED ON CONNECTOR BODY (TYP)

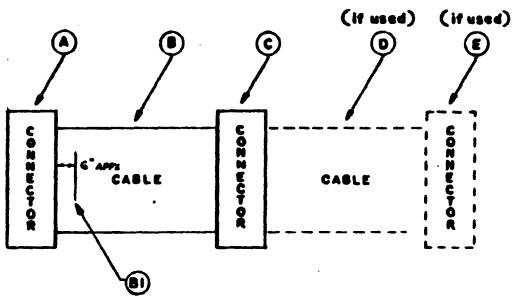
IC BOARD (TYP) PIN NO's (REF)

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/4/78	TITLE	CABLE RUN-LIST	
CHECKED	DK	7/20/79	CUSTOMER/NO.	DWG NO.	REV
APPROVED	DK	7/24/79	HSMIMP	DMLS-11	C

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	7.16.74
	B	ECN 0105	11.8.74
	C	ECN 0127	1.29.75
	D	ECN 0137	9.25.75
DRF	E	ECN 0230	10.1.76
	F	ECN 0287	4.20.78



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 COND FEMALE CONN	CANNON	121-7326-110	209
A1	20	PINS, FEMALE CONN	CANNON	030-7312-011	210
B	(*)	5 COND, 22 AWG CABLE	BELDEN	8445	212
		(OR EQUIV)			
C	1	FEMALE CONN	CINCH/CANNON	DB-25S	211
C1	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526
C2	2	SCREW-LATCH SOCKET	CINCH	D-20418-2	429
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

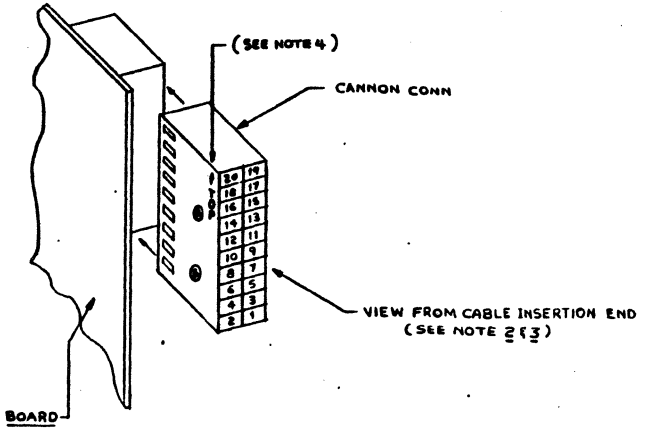
NOTE : ITEMS (A) & (A1) AVAILABLE AS KIT FROM LEC (PN 7770-1)

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT
	TIP PEN (BLK)
2	INSERT PINS IN ALL POSITIONS OF CONNECTOR
3	USE CANNON HAND-CRIMP # CCT-UBC
4	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN
	19 END OF CONN) AS SHOWN, WITH WHITE INK (SCD-0004)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	10FT		

PIN NUMBERING & ASSEMBLY DETAILS



CABLE FUNCTION	
FROM A	PSB
TO C	FANTAIL (INFOTON)
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	3/24/74
CHECKED	DK	7/16/74
APPROVED	AL	7/29/74

TITLE: CABLE ASSEMBLY DETAILS

CUSTOMER/NO.	DWG NO.	REV
HSMIMP	DPSB-10	F

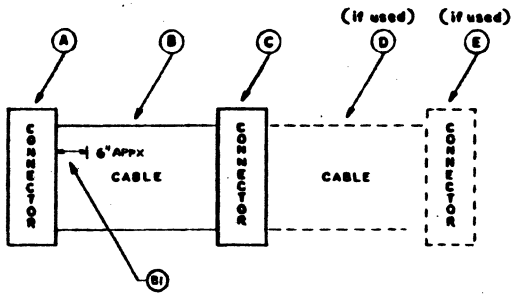
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7/24/74
	B	ECN 0105	11.18.74
	C	ECN 0127	1.29.75

CANNON CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES TERMINAL SIGNAL IDENT	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
19 (A1)	WHITE	3			BB RCV DATA						
11 (A5)	GREEN	5 } JUMPER ALL 3			CB CLEAR TO SEND	DERIVED FROM					
		8 } TO GREEN WIRE			CF CARRIER DETECT	NOTE: DATA-TERM-READY					
		6 }			CC DATA SET READY	SIGNAL ON PSB CARD					
5 (A8)	BLACK	2			BA TRANS DATA						
1 (A10)	BROWN	7			GND						
↑											
(REF ONLY)											
↓											
3 (A9)	RED	20			CD DATA TERM. READY	NOTE: TO CLEAR-TO-SEND ON PSB CARD					
↑											
CARD J1 ( )											

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
DRAWN	DRF	7/21/74	TITLE CABLE RUN-LIST		
CHECKED		7/24/74	CUSTOMER/NO.	DWG NO.	REV
APPROVED		7/24/74	HSMIMP	DPSB-11	C

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.9.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	CINCH	DC-375	148
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
B	(*)	12 LENGTHS	ALPHA/BELDEN	RG-174/U	432
B2	(*)	1" ZIPPER TUBING	ALPHA/BELDEN	ZIP-31-1 BLK/QPL	347
C	1	FEMALE CONN	CINCH	DC 375	148
C1	1	PLUG SHELL	AMPHENOL	17-1373	155
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	3 FT		

PIN NUMBERING & ASSEMBLY DETAILS

CABLE FUNCTION						
FROM A	LOCAL HOST (PLURIBUS CABLE)	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
TO C	LOCAL HOST (PLURIBUS CABLE)	DRAWN	DRF	5.18	TITLE	CABLE ASSEMBLY DETAILS
TO E		CHECKED			CUSTOMER/NO.	DWG NO. / REV
		APPROVED			HSMIMP	DPTP-10 / A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.9.79

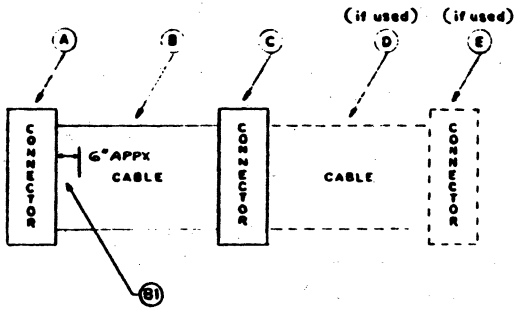
CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
12	CENTER	9									
31	SHIELD	28									
11	CENTER	10									
30	SHIELD	29									
9	CENTER	12									
28	SHIELD	31									
10	CENTER	11									
29	SHIELD	30									
4	CENTER	8									
23	SHIELD	27									
2	CENTER	6									
21	SHIELD	25									
1	CENTER	5									
20	SHIELD	24									
3	CENTER	7									
22	SHIELD	26									
8	CENTER	4									
27	SHIELD	23									
6	CENTER	2									
25	SHIELD	21									
5	CENTER	1									
24	SHIELD	20									
7	CENTER	3									
26	SHIELD	22									

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/79	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	JCH	5/15	CUSTOMER/NO. HSMIMP; DWG NO. DPTP-11; REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.26.75
	B	ECN 0137	4.25.75
	C	ECN 0230	10.1.76
	D	ECN 0350	1.11.79
	E	ECN 0356	2.8.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	40 PIN FEMALE CONN	AMP	86896-2	443
	OR	40 PIN FEMALE CONN	ANSLEY	609-4030	1685
		STRAIN RELIF ASSY	ANSLEY	609-4031	1686
B	(*)	13 PR TWIST 'N' FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
C	1	25 PIN, RS232	CANNON / CINCH	DB25S	211
C1	1	PLASIC BACK SHELL	AMPHENOL	17-1372	526
C2	2	SCREW-LATCH SOCKET	CANNON / CINCH	D-20418-39	354
C3	2"	1/2 SHRINK TUBING	ALPHA	FIT-221-1/2"	1034
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLFIM-CP	366

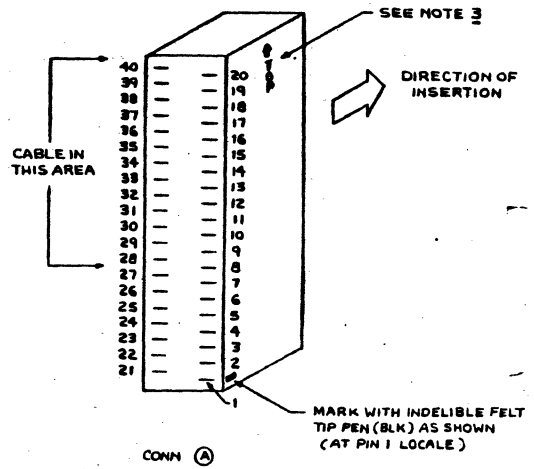
ASSEMBLY NOTES

1	USE 1/2" SHRINK TUBING (C3) AROUND CABLE (B) AT PLASTIC BACK SHELL (C1)
2	AT CONN (C) BUNDLE THE INDICATED 6 WIRES WITH A PIGTAIL TO PIN 12 AND
	BUNDLE THE INDICATED 5 WIRES WITH A PIGTAIL TO PIN 13 (SEE DPTR-11)
3	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 20 END
	OF CONN) AS SHOWN WITH WHITE INK (SCD-0004)
4	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBE FELT TIP PEN (BLK)
5	CUT CABLE TO LENGTH IN CENTER OF FLAT AREA

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		
(*)	-B	10 FT		
(*)	-C	20"		

PIN NUMBERING & ASSEMBLY DETAILS



CONN (A)

VIEW FROM CABLE SIDE, UNASSEMBLED

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	PPB	DRAWN	DRF	4.25.75	TITLE	CABLE ASSEMBLY DETAILS
TO C	FANTAIL {REMEX / RR6300}	CHECKED				
TO E		APPROVED	JM	4.28.75	CUSTOMER NO.	DWG NO. DPTR-10 REV E

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.28.78
	B	ECN 0350	1.12.79

AMP/ANSLEY CONNECTOR A PIN NO.	WIRE COLOR B	REMEX-MATE CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PR NO'S SIG NAME	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
40	TAN	N.C.			13 SPARE						
20	ORN	14			13 SYS RDY						
39	TAN	13			12 GND						
19	RED	9			12 DAT RDY						
38	TAN	13			11 GND						
18	BRN	16			11 DRV RT						
37	TAN	N.C.			10 SPARE						
17	BLK	N.C.			10 SPARE						
36	TAN	12			9 GND						
16	WHT	1			9 DAT BIT 1						
35	TAN	12			8 GND						
15	GRY	2			8 DAT BIT 2						
34	TAN	12			7 GND						
14	VIO	3			7 DAT BIT 3						
33	TAN	12			6 GND						
13	BLU	4			6 DAT BIT 4						
32	TAN	12			5 GND						
12	GRN	5			5 DAT BIT 5						
31	TAN	12			4 GND						
11	YEL	6			4 DAT BIT 6						
30	TAN	13			3 GND						
10	ORN	7			3 DAT BIT 7						
29	TAN	13			2 GND						
9	RED	8			2 DAT BIT 8						
28	TAN	N.C.			1 SPARE						
8	BRN	13			1 GND						
		10	JUMPERED		MODE SEL						
		11	TOGETHER		GND						
		15/17/25	NO CONNECTION								

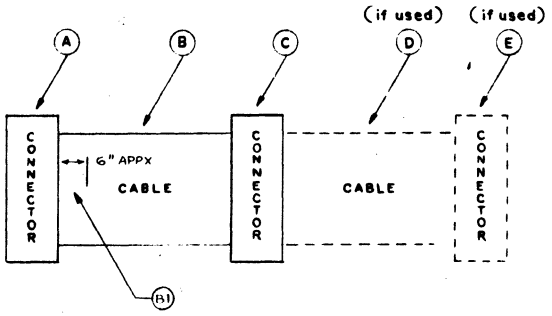
FOR WIRING SEE ASSY NOTE 2 ON CABLE ASSY DWG DPTR-10

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	SET	1/31/75	TITLE: CABLE RUN-LIST
CHECKED	DRF	2.1.75	CUSTOMER/NO. HSMIMP
APPROVED		2.20.75	DWG NO. DPTR-11 REV B

	REVISION		
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77



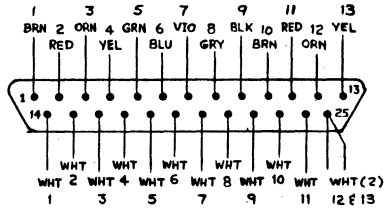
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN, 25 PIN	CINCH	DB25S	211
A1	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526
A2	2	DISC LATCHES	CANNON	D-110278	367
B	*	13 TW-PAIR CABLE	WOVEN	T13TP2807-UL1227	48
C	1	FEMALE CONN, 25 PIN	CINCH	DB25S	211
C1	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526
C2	2	DISC LATCHES	CANNON	D-110278	367
D	*	4 TW-PAIR CABLE	WOVEN	T4TP-2807UL-1227	208
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP-PEN (BLK)

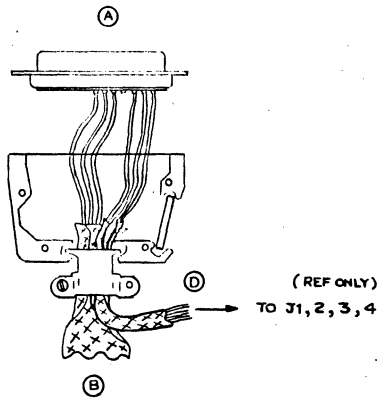
CABLE LENGTH

	TYPE	B	D	NOTES
*	A	20"	15"	

PIN NUMBERING & ASSEMBLY DETAILS



CONN (A) & (C) TW-PR WIRING SEQUENCE



CABLE FUNCTION	
FROM A	RED CONT PNL (J5)
TO C	CAPACITOR BOX (J10)
TO E	RED CONT PNL (J1,2,3,4)

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	12/7/77	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED	ABL	11/28/77	CUSTOMER/NO.: HSMIMP; DWG NO.: DRBS-10; REV: A

	REVISION		
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	RED PANEL PLI-10 NOTES (REF ONLY)	CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1			BRN/WHT		(J1) RCLK	N.C.	BRN/WHT	1			
14					GND	N.C		14			
2			RED/WHT		(J4) RDATA	N.C	RED/WHT	2			
15					GND	N.C		15			
3			ORN/WHT		(J3) TCLK	N.C.	ORN/WHT	3			
16					GND	N.C		16			
4			YEL/WHT		(J2) TDATA	N.C.	YEL/WHT	4			
17					GND	N.C.		17			
5	GRN/WHT	5			XFCW						
18		18			GND		(SEE NOTE 2)				
6	BLU/WHT	6			B2RWE-						
19		19			GND						
7	VIO/WHT	7			RRFR-						
20		20			GND						
8	GRY/WHT	8			RBBR-						
21		21			GND						
9	BLK/WHT	9			XTRA						
22		22			RBW0-						
10	BRN/WHT	10			RBW7-						
23		23			RBW6-						
11	RED/WHT	11			RBW5-						
24		24			RBW4-						
12	ORN/WHT	12			RBWW3-						
25		25			RBW2-						
13	YEL/WHT	13			RBW1-						
25	(SEE NOTE 1)	25			RBW2-						

NOTES

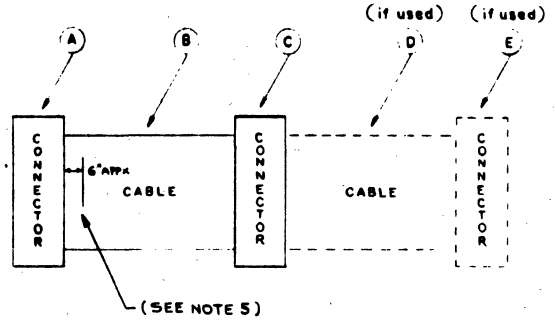
1- WHITE WIRE OF #13 PAIR (YEL/WHT) SOLDER TO PIN #25 OF CONN'S 'A' & 'C'

2- WIRE WIRES OF 'B' (13 TW-PR) TO PINS OF 'C' AS SHOWN

	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138		
DRAWN	DRF	12-7-77	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	ABI	11-28-77	CUSTOMER/NO.: HSMIMP; DWG NO.: DRBS-11; REV: A

CABLES

	REVISION		
APPD	SYM	DESCR	DATE
	A	REL HEAD	7.28.75
JM	B	ECN 0137	9.25.75
DRF	C	ECN 0230	10.1.76



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	3 M	3399 - 0000	351
B	(*)	RIBBON CABLE	3 M	3365 - 26 COND	352
C	1	MALE CONN	CANNON OR CINCH	DB 25 P	353
C1	2	SCREWLOCK SOCKET	CANNON OR CINCH	D 20418 - 39	354
C2	1	PLASTIC BACK SHELL	AMPHENOL	17 - 1372	526

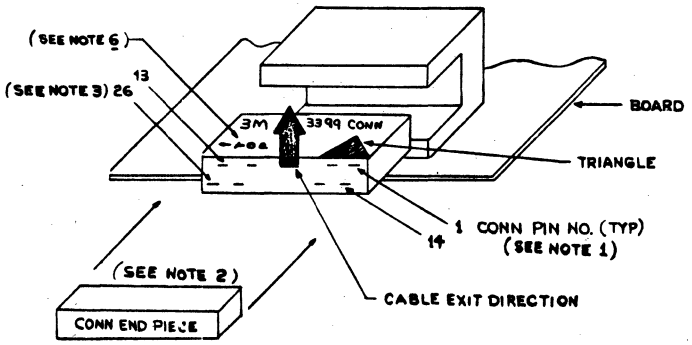
ASSEMBLY NOTES

6	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 26 END OF CONN) AS SHOWN, WITH WHITE INK (SCD-0004)
1	RED CABLE STRIPE GOES ON PIN 1 (BELOW TRIANGLE SYMBOL)
2	'LUMPY' SIDE OF CABLE GOES AGAINST CONN END PIECE
3	WIRE #26 NOT CONNECTED AT CINCH CONN - CUT & TAPE
4	ASSEMBLE USING 3M PRESS & LOCATOR PLATE NO: 3443 - 1
5	CABLE TYPE & S/N TO BE MARKED DIRECTLY ON RIBBON CABLE WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	5 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM BACK
(UNASSEMBLED)

START CABLE ASSY WITH THIS END. CABLE CANNOT BE MADE CORRECTLY IF NOTES 1 & 2 ARE NOT FOLLOWED, WHICH ONLY OCCURS AT ONE END OF THE CUT RIBBON-CABLE.

CABLE FUNCTION	
FROM A	SLI
TO C	FANTAIL
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	SET	5/1/74	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED					
APPROVED	JM	7/28/76	CUSTOMER/NO. CCP	DWG NO. DRSP-10	REV C

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	[illegible]

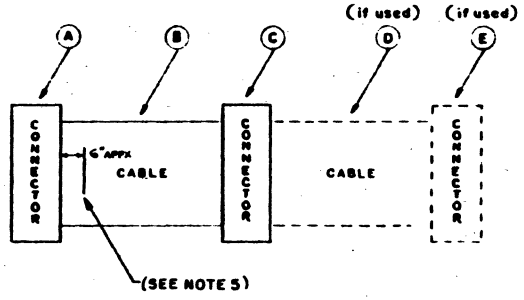
3M CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	EIA RS-232 DESIGNATION NOTES IF APPLICABLE	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
1	RED STRIPE	1			PROTECTIVE GROUND						
14	GRAY	14			SEC. TRANSMITTED DATA						
2		2			TRANSMITTED DATA						
15		15			TRANSMIT CLOCK (DCE SOURCE)						
3		3			RECEIVED DATA						
16		16			SEC. RECEIVED DATA						
4		4			REQUEST TO SEND						
17		17			RECEIVE CLOCK						
5		5			CLEAR TO SEND						
18		18			(UNASSIGNED)						
6		6			DATA SET READY						
19		19			SEC. REQUEST TO SEND						
7		7			SIGNAL GROUND						
20		20			DATA TERMINAL READY						
8		8			CARRIER DETECT						
21		21			SIGNAL QUALITY DETECTOR						
9		9			(DO NOT USE)						
22		22			RING INDICATOR						
10		10			(DO NOT USE)						
23		23			CLOCK RATE SELECTOR						
11		11			(UNASSIGNED)						
24		24			TRANSMIT CLOCK (DTE SOURCE)						
12		12			SEC. CARRIER DETECT						
25		25			(UNASSIGNED)						
13		13			SEC. CLEAR TO SEND						
26											

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	SET	12 24 79	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	[illegible]	[illegible]	CUSTOMER/NO.: HSMIMP; DWG NO.: DRSP-11; REV: A

	REVISION		
APPD	SYM	DESCR	DATE
	A	REL PROTO	2 28 75
DRF	B	ECN 0137	9.25.75
DRF	C	ECN 0230	11.1.76



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	3 M	3399 — 0000	351
B	(*)	RIBBON CABLE	3M	3365 - 26 COND	352
C	1	FEMALE CONN	CANNON / CINCH	DB25S	211
C1	2	SCREW-LATCH SOCKET	CANNON / CINCH	D20418-39	354
C2	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526

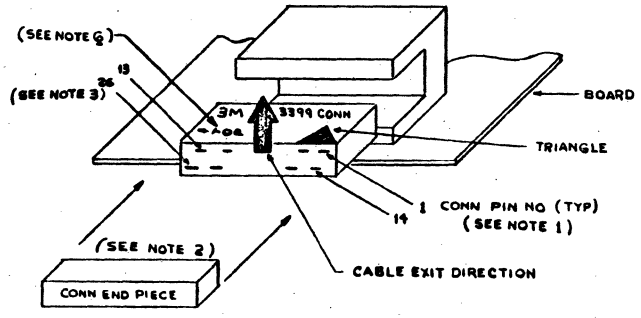
ASSEMBLY NOTES

6	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON P.N 26 END OF
	CONN) AS SHOWN, WITH WHITE INK (SCD-0004)
1	RED CABLE STRIPE GOES ON PIN 1 (BELOW TRIANGLE SYMBOL)
2	'LUMPY' SIDE OF CABLE GOES AGAINST CONN END PIECE
3	WIRE #26 NOT CONNECTED AT CINCH CONN - CUT & TAPE
4	ASSEMBLE USING 3M PRESS & LOCATOR PLATE NO: 3443-1
5	CABLE TYPE & S/N TO BE MARKED DIRECTLY ON RIBBON CABLE
	WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM BACK
(UNASSEMBLED)

START CABLE ASSY WITH THIS END.
CABLE CANNOT BE MADE CORRECTLY
IF NOTES 1 & 2 ARE NOT FOLLOWED,
WHICH ONLY OCCURS AT ONE END OF
THE CUT RIBBON CABLE.

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	SMS	DRAWN	DRF	8/75	TITLE	CABLE ASSEMBLY DETAILS	
TO C	FANTAIL	CHECKED					
TO E		APPROVED			CUSTOMER/NO. CCP	DWG NO. DRSS-10	REV C

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	[illegible]

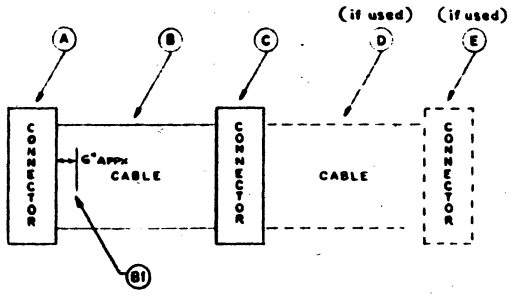
3M CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	EIA RS-232 DESIGNATION NOTES IF APPLICABLE	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
1	RED STRIPE	1			PROTECTIVE GROUND						
14	GRAY	14			SEC. TRANSMITTED DATA						
2	↓	2			TRANSMITTED DATA						
15		15			TRANSMIT CLOCK (DCE SOURCE)						
3		3			RECEIVED DATA						
16		16			SEC. RECEIVED DATA						
4		4			REQUEST TO SEND						
17		17			RECEIVE CLOCK						
5		5			CLEAR TO SEND						
18		18			(UNASSIGNED)						
6		6			DATA SET READY						
19		19			SEC. REQUEST TO SEND						
7		7			SIGNAL GROUND						
20		20			DATA TERMINAL READY						
8		8			CARRIER DETECT						
21		21			SIGNAL QUALITY DETECTOR						
9		9			(DO NOT USE)						
22		22			RING INDICATOR						
10		10			(DO NOT USE)						
23		23			CLOCK RATE SELECTOR						
11		11			(UNASSIGNED)						
24		24			TRANSMIT CLOCK (DTE SOURCE)						
12		12			SEC. CARRIER DETECT						
25		25			(UNASSIGNED)						
13		13			SEC. CLEAR TO SEND						
26	↓	NO CONNECTION (CUT & TAPE)									

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	12/12/25	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	[illegible]	[illegible]	CUSTOMER/NO.: CCP; DWG NO.: DRSS-11; REV: A

APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	2 28.75
	B	ECN 0137	4.25.75
	C	ECN 0193	7.24.75
	D	ECN 0280	10.1.76



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN I/O CONN	CANNON	121-7326-110	209
		NOTE (A) & (A1) AVAILABLE AS PKG FROM LEC		7770-1	
A1	20	CRIMP-PINS FEMALE	CANNON	030-7312-011	210
B	(*)	5 COND, 22 AWG CABLE	BELDEN	8445 (or equiv)	212
C	1	CONN, MALE	CANNON/CINCH	DB-25P	353
C1	2	SCREW-LATCH SOCKET	CANNON / CINCH	D-20418-39	354
C2	1	PLASTIC BACK SHELL	AMPHENOL	17-1372	526
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

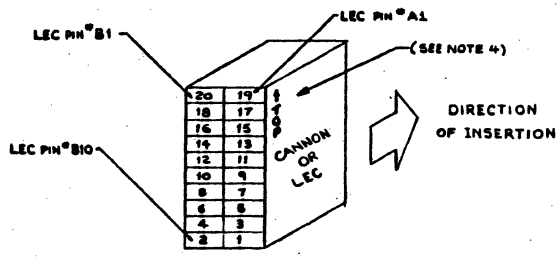
ASSEMBLY NOTES

1. CRIMP PINS (A1) WITH CANNON HAND CRIMPER # CCT-UBC
2. CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
3. AT (A) INSERT ALL 20 PINS
4. USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 19 END OF CONN) AS SHOWN, WITH WHITE INK (SCD-0004)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED (A)

CABLE FUNCTION	
CURRENT-LOOP TTY	
FROM A	PSB
TO C	FANTAIL
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	4.15	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			CUSTOMER NO.: HSMIMP; DWG NO.: DTTY-10; REV: D
APPROVED			

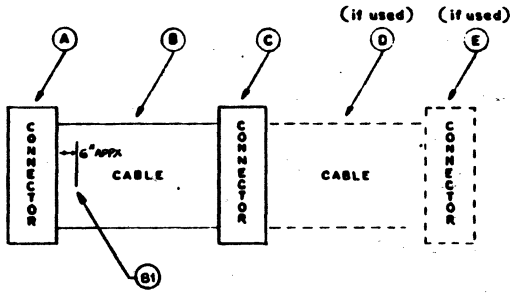
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	2 28 75

3M (20 PIN) CONNECTOR A PIN NO. 3M (LEC)	WIRE COLOR B	CINCH (25 PIN) CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
16 (B3)	WHT	16			PRINTER +						
14 (B4)	BLK	14			PRINTER -						
12 (B5)	RED	12			KEYBOARD +						
10 (B6)	GREEN	10			KEYBOARD -						
	BROWN NOT USED										
(REF ONLY)											

	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138			
DRAWN	S.E.T.	2/8/75	TITLE CABLE RUN-LIST	
CHECKED				
APPROVED		2/28/75	CUSTOMER/NO. HSMIMP	DWG NO. DTTY-11 REV A

CABLES

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.17.77



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN	CINCH	DC-37P	149
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
A2	2	DISC LATCHES	CANNON	D-110278	367
B	(*)	[RECOMMENDED] AWG-12 PR DIRECT BURIAL CABLE, REA SPEC # PE-23			
B	(**)	[RECOMMENDED] FOR RUNS UNDER 300 FT	COLUMBIA # 6059		
C	1	CONNECTOR	(SUPPLIED BY SITE)		
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A			SUPPLIED BY SITE
(**)	A	UNDER 300 FT		

PIN NUMBERING & ASSEMBLY DETAILS

CABLE FUNCTION	
FROM A	FANTAIL
TO C	HOST
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	S.E.T.	7/26/77	TITLE: CABLE ASSEMBLY DETAILS
CHECKED	DRF	8/11/77	
APPROVED	[illegible]	8/17/77	CUSTOMER/NO. HSMIMP; DWG NO. FHDA-10; REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	2.1277

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	(ALTERNATE) COLUMBIA* 6039 if used WIRE COLOR @B	if used CONNECTOR E PIN NO.	NOTES PAIR NO'S	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1			WHT / RED	SEE NOTE 1 (TYP)	1 RFNIB +	# READY FOR NEXT IMP BIT					
20					1 RFNIB -	" " " "					
15			YEL / BLK	SEE NOTE 2 (TYP)	2 TYIMV +	# THERES YOUR IMP BIT					
33					2 TYIMV -	" " " "					
17			BLU / BLK		3 LIBIV +	# LAST IMP BIT					
35					3 LIBIV -	" " "					
19			GRN / BLK		4 IMDTV+	# IMP DATA					
37					4 IMDTV-	" "					
13			WHT / BLK		5 RFNBV+	# READY FOR NEXT HOST BIT					
32					5 RFNBV-	" " " " "					
6			YEL / RED		6 TYHBX +	# THERES YOUR HOST BIT					
25					6 TYHBX -	" " " "					
7			BLU / RED		7 LHBIT +	# LAST HOST BIT					
26					7 LHBIT -	" " "					
8			GRN / RED		8 HSDTA+	# HOST DATA					
27					8 HSDTA-	" "					
9			BLK / BRN		9 XMTOT+	# IMP READY TEST					
10					9 XMTXM+	# IMP MASTER READY					
11			BRN / RED		10 HMRDY+	# HOST MASTER READY					
12					10 HRDYT+	# HOST READY TEST					
			BLK / RED	SPARE							
			BLK / ORN	SPARE							
22			SHIELDS	(SEE NOTE 3)	GND	SHIELD GROUND					

NOTES

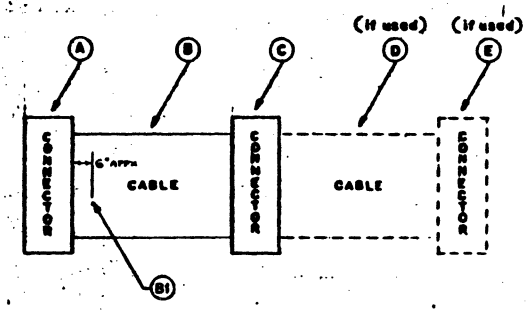
1- SIGNALS ORIGINATING AT HOST USE ONLY HALF-RED TWISTED PAIRS
2- SIGNALS ORIGINATING AT IMP USE ONLY HALF-BLK TWISTED PAIRS
3- CONNECT ALL SHIELDS TOGETHER AND WIRE TO PIN # 22

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	S.E.T.	7/6/76	TITLE	CABLE RUN-LIST
CHECKED	DRF	7/7/77	CUSTOMER/NO. HSMIMP	DWG NO. FHDA-11 REV A
APPROVED	DRF	7/7/77		

	REVISION		
APPD	SYM	DESCR	DATE
MJ	A	REL PROD	1-24-74
AK	B	ECN 0124	1-22-75
MFL	C	ECN 0147	6-16-75
AK	D	ECN 0148	6-16-75
JRF	E	ECN 0221	7-29-76



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN	CINCH	DC-37P	149
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
A2	2	DISC LATCHES	CANNON	D-110278	367
B	(*)	12 LENGTHS	ALPHA / BELDEN	RG-174/U	432
B2	(*)	1" ZIPPER TUBING	ALPHA / BELDEN	ZIP-31-1 BLK/Q.P.L.	347
C	1	CONN	(SUPPLIED BY SITE)		
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	30 FT		
	B	40 FT		
	C	60 FT		
	D	70 FT		
	E	150 FT		
	F	200 FT		
	G	100 FT		
	H	300 FT		

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	FANTAIL	DRAWN	DRF	4/16/74	TITLE	CABLE ASSEMBLY DETAILS	
TO C	HOST	CHECKED	AK	7/24/74	CUSTOMER/NO.	DWG NO.	REV
TO E		APPROVED	MFL	7/31/74	HSMIMP	FHSA-10	E

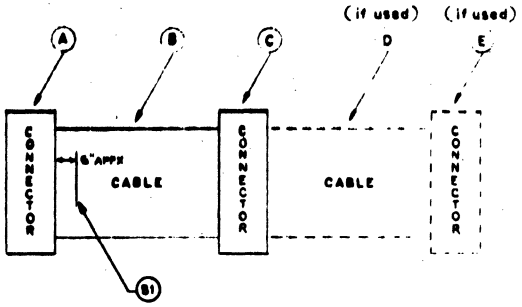
REVISION			
APP'D	SYM	DESCR	DATE
MFL	A	REL PROD	7.14.76
[illegible]	B	ECN 0112	12.9.76
MFL	C	ECN 0158	7.20.78

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO'S	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1	CENTER				1 RFNIB						
20	SHIELD				1 GND						
2	CENTER				2 TYIMB						
21	SHIELD				2 GND						
3	CENTER				3 LIBIT						
22	SHIELD				3 GND						
4	CENTER				4 IMDTA						
23	SHIELD				4 GND						
5	CENTER				5 RFNHB						
24	SHIELD				5 GND						
6	CENTER				6 TYHBX						
25	SHIELD				6 GND						
7	CENTER				7 LHBIT						
26	SHIELD				7 GND						
8	CENTER				8 HSDTA						
27	SHIELD				8 GND						
9	CENTER				9 XMTOT						
28	SHIELD				9 GND						
10	CENTER				10 XMTXM						
29	SHIELD				10 GND						
11	CENTER				11 HMRDY						
30	SHIELD				11 GND						
12	CENTER				12 HRDYT						
31	SHIELD				12 GND						

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
DRAWN	DRF	6-19-76	TITLE CABLE RUN-LIST		
CHECKED	WK	7/6/78	CUSTOMER/NO.	DWG NO.	REV
APPROVED	MFL	7/6/78	HSMIMP	FHSA-11	C

APP'D	REVISION SYM	DESCR	DATE
	A	REL PROD	4.28.78



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN	CINCH	DC-37P	149
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
A2	2	DISC LATCHES	CANNON	D-110278	367
B	(*)	12 LENGTHS	ALPHA / BELDEN	RG-174/U	432
B2	(*)	1" ZIPPER TUBING	ALPHA / BELDEN	ZIP-33-1 BLK/Q.L.P.	347
C	1	PADDLE CONN	HONEYWELL	013-625-701	446
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

	ASSEMBLY NOTES
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
*	A	30 FT		

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	FANTAIL	DRAWN	DRF	10.17.75	TITLE	CABLE ASSEMBLY DETAILS
TO C	316 IMP	CHECKED				
TO E		APPROVED	dm	10/24/75	CUSTOMER/NO. HSMIMP	DWG NO. FHSH-10 REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	10.24.75

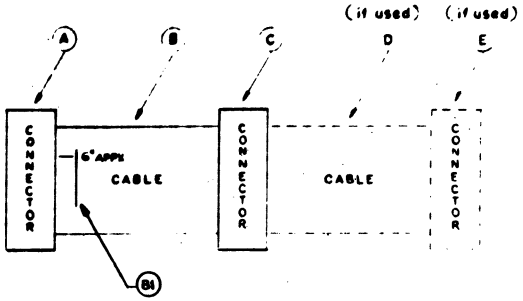
CINCH CONNECTOR A PIN NO.	WIRE COLOR B	HONEYWELL CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO's	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
1	CENTER	7			1 RFNIB						
20	SHIELD	33			1 GND						
2	CENTER	4			2 TYIMB						
21	SHIELD	33			2 GND						
3	CENTER	6			3 LIBIT						
22	SHIELD	33			3 GND						
4	CENTER	8			4 IMDTA						
23	SHIELD	33			4 GND						
5	CENTER	2			5 RFNHB						
24	SHIELD	33			5 GND						
6	CENTER	5			6 TYHBX						
25	SHIELD	33			6 GND						
7	CENTER	1			7 LHBIT						
26	SHIELD	33			7 GND						
8	CENTER	3			8 HSDTA						
27	SHIELD	33			8 GND						
9	CENTER	11			9 XMTOT						
28	SHIELD	33			9 GND						
10	CENTER	12			10 XMTXM						
29	SHIELD	33			10 GND						
11	CENTER	13			11 HMRDY						
30	SHIELD	33			11 GND						
12	CENTER	14			12 HRDYT						
31	SHIELD	33			12 GND						

ALL SHIELDS MECHANICALLY TIED TOGETHER AND TERMINATE AT PIN NO 33

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	DRF	10/17/75	TITLE CABLE RUN-LIST	
CHECKED				
APPROVED			CUSTOMER/NO. HSMIMP	DWG NO. FHSH-11 REV A

CABLES

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	12.11.73
[illegible]	B	ECN 0192	2.28.74



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN	CINCH	DC-37P	149
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
A2	2	DISC LATCHES	CANNON	D-110278	367
B	(*)	12 LENGTHS CABLE	ALPHA / BELDEN	RG-174/U	432
B2	(*)	1" ZIPPER TUBING	ALPHA / BELDEN	ZIP-33-1 BLK/GLP	347
C	1	85 PIN CONN WITH PINS	AMPHENOL	348-46E18-85P1	499
C1	1	CABLE CLAMP	AMPHENOL	348-260-18001	513
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF 1M-CP	366

ASSEMBLY NOTES
1 CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	30 FT		

CABLE FUNCTION	
FROM A	HOST (PLI) FANTAIL
TO C	516 IMP (LOCAL HOST)
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	12/11/73	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED	[illegible]	12/11/73	CUSTOMER/NO.	DWG NO.	REV
APPROVED	[illegible]	12/11/74	HSMIMP	FHSI-10	B

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	8.11.75
[illegible]	B	ECN 0198	8.28.76

37 PIN CINCH CONNECTOR A PIN NO.	WIRE COLOR B	86 PIN AMPHENOL CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	SIGNAL NAMES (REF. PLURIBUS) NOTES PAIR NO'S	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
1	CENTER	13			1 RFNIB						
20	SHIELD	14			1 GND						
2	CENTER	7			2 TYIMB						
21	SHIELD	8			2 GND						
3	CENTER	11			3 LIBIT						
22	SHIELD	12			3 GND						
4	CENTER	15			4 IMDTA						
23	SHIELD	16			4 GND						
5	CENTER	3			5 RFNHB						
24	SHIELD	4			5 GND						
6	CENTER	9			6 TYHBX						
25	SHIELD	10			6 GND						
7	CENTER	1			7 LHBIT						
26	SHIELD	2			7 GND						
8	CENTER	5			8 HSDTA						
27	SHIELD	6			8 GND						
9	CENTER	21			9 XMTOT						
28	SHIELD	22			9 GND						
10	CENTER	23			10 XMTXM						
29	SHIELD	24			10 GND						
11	CENTER	27			11 HMRDY						
30	SHIELD	28			11 GND						
12	CENTER	25			12 HRDYT						
31	SHIELD	26			12 GND						

HOST

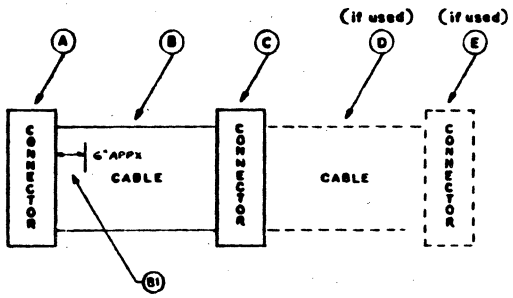
516 IMP

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/29/75	TITLE: CABLE RUN-LIST
CHECKED	[illegible]	9/9/75	CUSTOMER/NO.: HSMIMP
APPROVED	[illegible]	9/9/75	DWG NO.: FHSI-11
			REV: B

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.9.79



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN	CINCH	DC-37P	149
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
A2	2	DISC LATCHES	CANNON	D-110278	367
B	(*)	12 LENGTHS	ALPHA/BELDEN	RG-174/U	432
B2	(*)	1" ZIPPER TUBING	ALPHA/BELDEN	ZIP-31-1 BLK/Q.PL.	347
C	1	MALE CONN ASSY	AMPHENOL	48-16R18-31P	1307
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

TYPE	B	D	NOTES
A	30 FT		
B	40 FT		
C	60 FT		
D	70 FT		
E	150 FT		
F	200 FT		
G	100 FT		
H	300 FT		

CABLE FUNCTION	
FROM A	FANTAIL
TO C	HOST
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	4-28-78	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			CUSTOMER/NO.: HSMIMP
APPROVED			DWG NO.: FHSS-10
			REV: A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.9.79

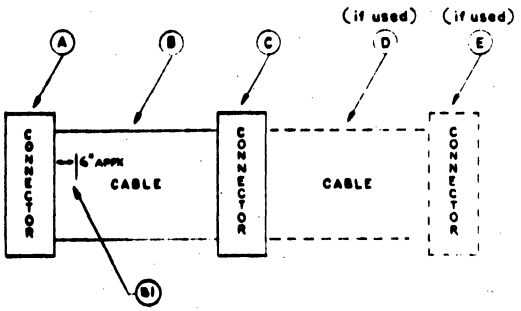
CINCH CONNECTOR A PIN NO.	WIRE COLOR B	AMPHENOL CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
1	CENTER	17									
20	SHIELD	18									
2	CENTER	5									
21	SHIELD	6									
3	CENTER	1									
22	SHIELD	2									
4	CENTER	3									
23	SHIELD	4									
5	CENTER	7									
24	SHIELD	8									
6	CENTER	19									
25	SHIELD	20									
7	CENTER	21									
26	SHIELD	22									
8	CENTER	23									
27	SHIELD	24									
9	CENTER	13									
28	SHIELD	31									
10	CENTER	14									
29	SHIELD	31									
11	CENTER	11									
30	SHIELD	31									
12	CENTER	12									
31	SHIELD	31									

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	2.9.79	TITLE: CABLE RUN-LIST
CHECKED			CUSTOMER/NO.: HSMIMP; DWG NO.: FHSS-11; REV: A
APPROVED			

CABLES

APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	6.2.76



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	CINCH	DC-37S	148
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
B	(*)	12 LENGTHS	ALPHA / BELDEN	RG-174/U	432
B2	(*)	1" ZIPPER TUBING	ALPHA / BELDEN	ZIP-33-1 BLK/Q.L.P.	347
C	1	PADDLE CONN	HONEYWELL	031-625-701	446
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	3 FT		

CONNECTOR 'A' COUPLES TO FHSA CABLES CONNECTOR 'A'

CABLE FUNCTION	
FROM A	SEE ABOVE
TO C	316 IMP
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

			TITLE		
DRAWN	DRF	8 JUL 76	CABLE ASSEMBLY DETAILS		
CHECKED			CUSTOMER/NO.	DWG NO.	REV
APPROVED	[illegible]	[illegible]	HSMIMP	FHST-10	A

REVISION			
APPD	SYM	DESCR	DATE
	A	Rel Prod	4.1.76

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	HONEYWELL CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO'S
1	CENTER	2			1 RFNIB
20	SHIELD	33			1 GND
2	CENTER	5			2 TYIMB
21	SHIELD	33			2 GND
3	CENTER	1			3 LIBIT
22	SHIELD	33			3 GND
4	CENTER	3			4 IMDTA
23	SHIELD	33			4 GND
5	CENTER	7			5 RFNHB
24	SHIELD	33			5 GND
6	CENTER	4			6 TYHBX
25	SHIELD	33			6 GND
7	CENTER	6			7 LHBIT
26	SHIELD	33			7 GND
8	CENTER	8			8 HSDTA
27	SHIELD	33			8 GND
9	CENTER	14			9 XMTOT
28	SHIELD	33			9 GND
10	CENTER	13			10 XMTXM
29	SHIELD	33			10 GND
11	CENTER	12			11 HMRDY
30	SHIELD	33			11 GND
12	CENTER	11			12 HRDYT
31	SHIELD	33			12 GND

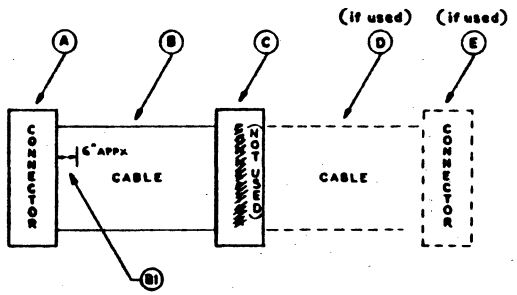
CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES

ALL SHIELDS MECHANICALLY TIED TOGETHER AND TERMINATE AT PIN NO 33

CABLES

BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			COMPUTER SYSTEMS DIVISION
DRAWN	DRF	3.5.76	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED			CUSTOMER/NO. HSMIMP; DWG NO. FHST-11; REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	5.2375
E.C.	B	ECN 243	3.2377



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	25 PIN MALE CONN	CANNON/CINCH	DB 25 P	353
A1	1	CONN HOOD	CANNON/CINCH	DB 24659	423
A2	2	JACK SCREW (M)	CANNON/CINCH	D 20419-16	361
B	(*)	FANTAIL MODEM CABLE	ALPHA	#1323 9TW PR 22 GA	219
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	WRAP OR TAPE CABLE AT (A1) IF RQ'D TO PROVIDE STRAIN RELIEF
3	TAPE OR TIE BACK UNUSED PAIRS INSIDE SHELL AT (A)
4	AT (C) DO NOT CUT BACK JACKET OR INSULATION

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	30FT		
	-B	50FT		

CABLE FUNCTION KG STATUS & CONTROL (BLACK)		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	BLACK FANTAIL	DRAWN	S.E.T.	5/21/75	TITLE	CABLE ASSEMBLY DETAILS	
TO B	KG-34 TB-4 (EXTERNAL)	CHECKED					
TO C		APPROVED	DM	5/21/75	CUSTOMER/NO. PLI-1	DWG NO. FKGA-10	REV B

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	5.11.75
DM	B	ECN 0194	8.14.75

DB 25 P CONNECTOR A PIN NO.	WIRE COLOR B	KG 34 TB4 CONNECTOR C PIN NO.	If used WIRE COLOR D	[illegible] CONNECTOR E PIN NO. SIGNAL	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
7	YELLOW	1		XLRM+							
20	BLACK	13		GND							
8	ORANGE	2		PWRON+							
21	BLACK	13		GND							
10	BROWN	11		KMIAR+							
23	BLACK	14		GND							
11	RED	9		KRPAP+							
24	BLACK	14		GND							
12	BLUE	10		TPREP+							
13	BLACK	15		TPREP-(GND)							

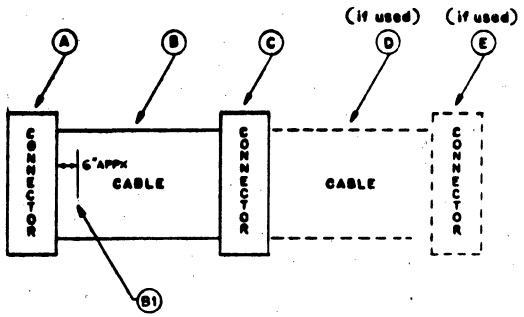
NOTE: THIS COLOR-CODE SCHEME IDENTICAL TO FMLA CABLE AND DOES NOT FOLLOW MANUFACTURES (ALPHA) STANDARD.

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	S. E. T.	5/21/75	TITLE CABLE RUN LIST LOW SPEED KG SIGNALS	
CHECKED				
APPROVED	DM	5/28/75	CUSTOMER/NO. PLI-1	DWG NO. FKGA-11 REV B

CABLES

	REVISION		
APPD	SYM	DESCR	DATE
	A	REL PROD	7/26/74
	B	ECN 0124	1/27/75
	C	ECN 0148	6/16/75



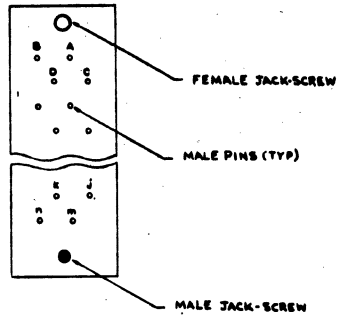
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	CINCH	DC-37S	148
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
A2	2	DISC LATCHES	CANNON	D-110278	367
B	(*)	25 TW-PR TELEPHONE CABLE			215
C	1	MALE CONN	WINCHESTER	MRAC 34P JTDH	216
C1	32	PINS	WINCHESTER	100-2516P OR	217
				100-1016P	
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	30 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM PIN END
WINCHESTER CONN.

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	FANTAIL	DRAWN	DRF	8/14/74	TITLE	CABLE ASSEMBLY DETAILS	
TO C	306 MODEM	CHECKED	DK	8/14/74			
TO E		APPROVED	DK	9/10/74	CUSTOMER/NO. HSMIMP	DWG NO. FMHA-10	REV C

REVISION			
APP'D	SYM	DESCR	DATE
	A	Rel Prod	7.31.79
KO	B	ECN 0113	10.9.79

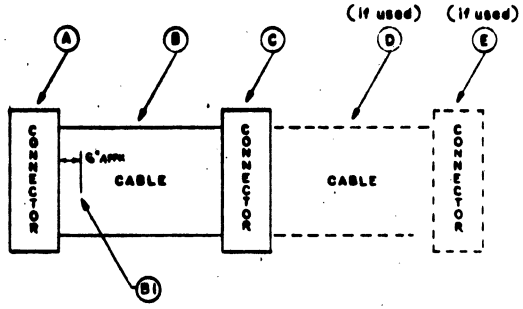
CINCH CONNECTOR A PIN NO.	WIRE COLOR B	WINCHESTER CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO's	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
1	BLUE \WHITE	V			1 SCR+						
20	WHITE\BLUE	X			1 SCR-						
2	ORANGE\WHITE	R			2 RD+						
21	WHITE\ORANGE	T			2 RD-						
3	GREEN\WHITE	Y			3 SCT+						
22	WHITE\GREEN	n (Lower case)			3 SCT-						
4	BROWN\WHITE	P			4 SD+						
23	WHITE\BROWN	S			4 SD-						
5	SLATE\WHITE	U			5 SCTE+						
24	WHITE\SLATE	W			5 SCTE-						
6	BLUE\BLACK	L			6 GND						
25	BLACK\BLUE	B			6 GND						
7	ORANGE\BLACK	C			7 RS						
26	BLACK\ORANGE	B			7 GND						
8	ORANGE\YELLOW	B			8 GND						
27	YELLOW\ORANGE	B			8 GND						
9	SLATE\YELLOW	H			9 DTR						
28	YELLOW\SLATE	B			9 GND						
10	VIOLET\BLUE	B			10 GND						
29	BLUE\VIOLET	B			10 GND						
11	VIOLET\ORANGE	K			11 LT						
30	ORANGE\VIOLET	B			11 GND						
12	VIOLET\GREEN	B			12 GND						
31	GREEN\VIOLET	B			12 GND						
13	VIOLET\SLATE	A			13 Prt GND						
32	SLATE\VIOLET	A			13 Prt GND						

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	7/11/79	TITLE: CABLE RUN-LIST
CHECKED	DK	7/11/79	CUSTOMER/NO. HSMIMP; DWG NO. FMHA-11; REV B
APPROVED	DK	7/11/79	

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.8.74
	B	ECN 0124	1.27.75
	C	ECN 0148	6.4.75



SYM	AMT	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	CINCH / CANNON	DC-375	148
A1	1	SHELL, CONN	AMPHENOL	17-1373	155
A2	2	DISC LATCH	CANNON	D-110278	367
B	(*)	9 PR-TW 22AWG CABLE	ALPHA	1323	219
C	1	FEMALE CONN	BURNDY	MD-12-MXP-7TC	213
C1	5	OUTER PINS, CONN	BURNDY	RMMX110-1	293
C2	5	INNER PINS, CONN	BURNDY	RFM22W1	292
C3	5	CRIMP COLLAR, PIN	BURNDY	YORX110-2	294
C4	5	TEFLON INNER-SLEEVE	BURNDY	RCMXB-067	295
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE
	FELT-TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	30 FT		

PIN NUMBERING & ASSEMBLY DETAILS

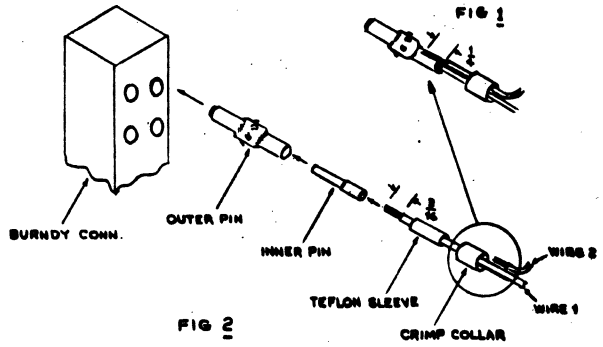


FIG 2

BURNDY CONNECTOR PIN ASSEMBLY INSTRUCTION

1 – SLIDE CRIMP COLLAR AND TEFLON-SLEEVE ONTO WIRE 1 AS SHOWN.

2 – STRIP WIRE 1 AS SHOWN, INSERT IN INNER-PIN AND CRIMP, USE BURNDY CRIMPING TOOL M8ND-HOLE MARKED 22.

3 – SLIDE TEFLON-SLEEVE UP TO INNER-PIN END, INSERT INNER-PIN INTO OUTER, UNTIL IT SNAPS LOCKED.

4 – STRIP WIRE 2 AS SHOWN, INSERT THRU CRIMP-COLLAR, PLACE STRANDS ON SHOULDER OF OUTER-PIN, AS SHOWN IN FIG 1.

5 – SLIDE CRIMP COLLAR ONTO OUTER-PIN AND CRIMP, USE BURNDY CRIMPING TOOL M8ND-HOLE MARKED 110.

6 – SLIDE ENTIRE PIN ASSY INTO PROPER HOLE OF BURNDY CONNECTOR UNTIL IT SNAPS LOCKED.

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	FANTAIL	DRAWN	DRF	6.22.74	TITLE	CABLE ASSEMBLY DETAILS
TO C	303 MODEM	CHECKED	DK	7/24/74	CUSTOMER/NO.	DWG NO. / REV
TO E		APPROVED	DK	9/24/74	HSMIMP	FMLA-10 / C

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	11/20/79

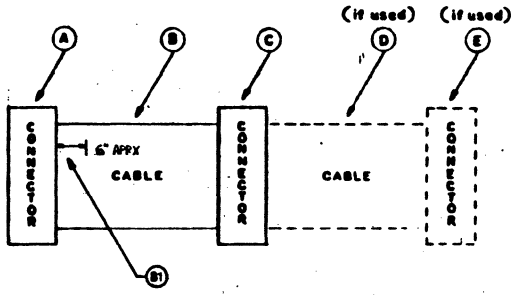
CINCH CONNECTOR A PIN NO.	WIRE COLOR B	BURNDY CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO'S	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
8	YELLOW	(#) E (INNER)			1 SD						
27	BLACK	(†) E (OUTER)			1 GND						
11	ORANGE	G (INNER)			2 LT						
30	BLACK	G (OUTER)			2 GND						
12	BROWN	J (INNER)			3 SCT						
31	BLACK	J (OUTER)			3 GND						
10	RED	K (INNER)			4 RD						
29	BLACK	K (OUTER)			4 GND						
6	BLUE	L (INNER)			5 SCR						
25	BLACK	L (OUTER)			5 GND						

= INNER PIN (TYP)
† = OUTER PIN (TYP)

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	DRF	8/22/79	TITLE	CABLE RUN-LIST
CHECKED	QK	9/4/79	CUSTOMER/NO.	DWG NO. / REV
APPROVED	QK	9/24/79	HSMIMP	FMLA-11 / A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.9.79



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN	CINCH	DC-37P	149
A1	1	PLUG SHELL	AMPHENOL	17-1373	155
B	(*)	12 LENGTHS	ALPHA/BELDEN	RG-174/U	432
B2	(*)	1" ZIPPER TUBING	ALPHA/BELDEN	ZIP-31-1 BLK/Q.P.L	347
C	1	MALE CONN	CINCH	DC-37P	149
C1	1	PLUG SHELL	AMPHENOL	17-1373	155
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF 1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	100 FT		

CABLE FUNCTION	
FROM A	LOCAL HOST (FANTAIL)
TO C	LOCAL HOST (FANTAIL)
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/8/79	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED			CUSTOMER/NO.: HSMIMP; DWG NO.: FPTP-10; REV: A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.9.79

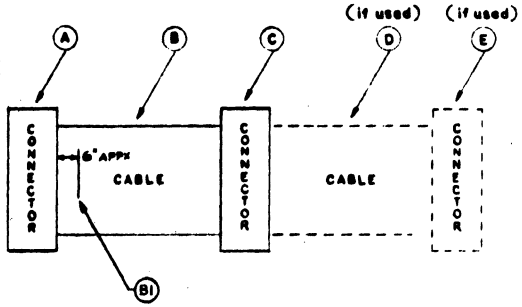
CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
12	CENTER	9									
31	SHIELD	28									
11	CENTER	10									
30	SHIELD	29									
9	CENTER	12									
28	SHIELD	31									
10	CENTER	11									
29	SHIELD	30									
4	CENTER	8									
23	SHIELD	27									
2	CENTER	6									
21	SHIELD	25									
1	CENTER	5									
20	SHIELD	24									
3	CENTER	7									
22	SHIELD	26									
8	CENTER	4									
27	SHIELD	23									
6	CENTER	2									
25	SHIELD	21									
5	CENTER	1									
24	SHIELD	20									
7	CENTER	3									
26	SHIELD	22									

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	5/5/78	TITLE	CABLE RUN-LIST
CHECKED				
APPROVED			CUSTOMER/NO. HSMIMP	DWG NO. FPTP-11 REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	2 28 75



	SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	PLUKIBUS P/N
	A					
	B	1	6 FT CABLE ASSY	TEXAS INSTRUMENT	959372-1	364
	C		(ONE FURNISHED WITH EACH T.I. SILENT 700 TERMINAL)			
(*)	C1	2	SCREW-LOCK SOCKET	CINCH/CANNON	D-20418-2	354
			(FEMALE)			
	B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

	ASSEMBLY NOTES
(*) 1	REPLACE JACKSCREW WITH JACK SOCKETS (C1) ON 25 PIN CONNECTOR
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE
	FELT TIP PEN (BLK)

CABLE LENGTH

TYPE	B	D	NOTES
-A	6FT		

CABLES

PIN NUMBERING & ASSEMBLY DETAILS

APPLICATIONS REQUIRING ONLY A 6FT CABLE (SILENT 700 TERMINAL), DO NOT REQUIRE THIS MODIFICATION.

THE CONVERSION OF THE T.I. CABLE TO A FTIA-A ALLOWS A FEIN CABLE TO BE ATTACHED, TO INCREASE THE OVER-ALL CABLE LENGTH. (THIS IS NECESSARY BECAUSE PARTS OF CONN (A) ARE NOT COMMERCIALLY AVAILABLE)

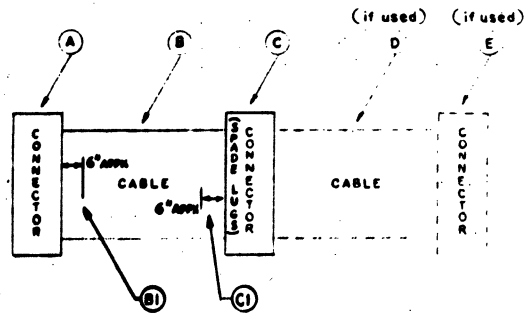
NOTE: THERE IS NO DWG FTIA-11, FOR WIRING SEE TEXAS INSTR. SERVICE MANUAL

CABLE FUNCTION	
FROM A	T.I. SILENT 700 TERM (EIA OPTION)
TO C	FANTAIL DPSB
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	SBT	2/25	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED					
APPROVED		2/27/75	CUSTOMER/NO. HSMIMP	DWG NO. FTIA-10	REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	2.28.78
	B	ECN 0193	2.26.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	25PIN RS-232 CONN (F)	CINCH / CANNON	DB-25S	211
A1	1	CONN HOOD, DB	CINCH / CANNON	DB-20962	359
A2	2	JACKSCREW (MALE)	CINCH / CANNON	D-20419-16	361
B	(*)	2 TW-PR, 22 AWG	BELDEN	9744	383
			OR ALPHA	1317	
C	4	#6 SPADE-LUG (CRIMPED)	BURNDY	BA16F8	384
			OR AMP	60199-1	
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366
C1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES

1. STRIP JACKET BACK 6" AT (C) AND CRIMP LUG ON EACH WIRE
2. CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
3. MARK ON TAG (C1) "20 MA, FULL DUPLEX" WITH INDELIBLE FELT-TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	15 FT		

PIN NUMBERING & ASSEMBLY DETAILS

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	FANTAIL (DTTY)	DRAWN	DRF	3/9/78	TITLE	CABLE ASSEMBLY DETAILS	
TO C	TELETYPE (CURRENT LOOP)	CHECKED					
TO E		APPROVED			CUSTOMER/NO. HSMIMP	DWG NO. FTTY-10	REV B

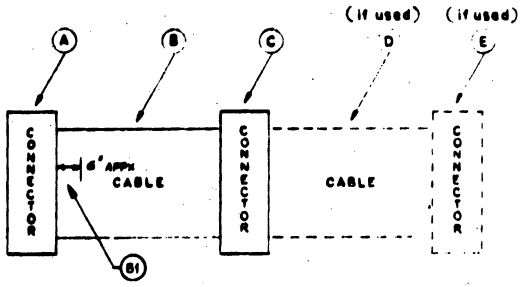
REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	2 APR 76

DB25 CONNECTOR A PIN NO.	WIRE COLOR B	SPADE LUGS CONNECTOR C PIN NO. TELETYPE T.B. TTY TERMINAL	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES (SIGNAL)	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
16	WHT	7			PRINTER +						
14	BLK	6			PRINTER -						
12	RED	4			KEYBOARD +						
10	BLK	3			KEYBOARD -						

CABLES

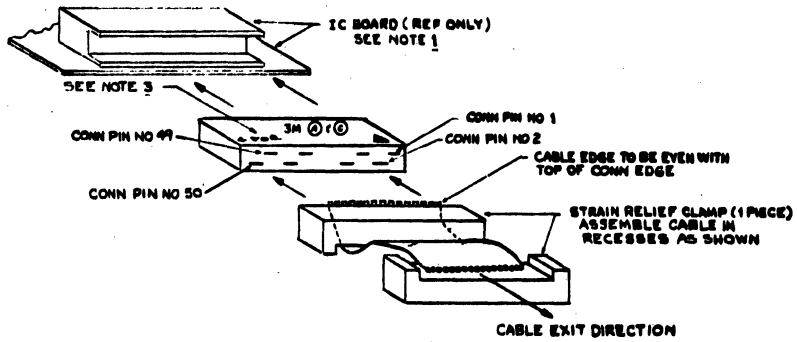
COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	S.E.T.	2 APR 76	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED		4/16/76	CUSTOMER/NO. HSMIMP; DWG NO. FTTY-11; REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	6-24-76
4-24	B	ECN 0218	7-2-76



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	3M	3425 - 3000	442
B	(*)	25 TW-PAIR CABLE	WOVEN CABLE	T25TP2807-UL1227N	49
C	1	FEMALE CONN	3M	3425 - 3000	442
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED

ASSEMBLY NOTES	
1	THE BOARD NUMBERING SYSTEM DIFFERS FROM THE CONNECTOR'S NO 3425 (SEE DWG IAMA-11) REF ONLY
2	CABLE TYPE & S/N TO BE MARKED ON B1 WITH INDELIBLE FELT-TIP PEN (BLK)
3	USING STAMP (SCD-0002), STAMP PAD (SCD-0003) MARK (ON PIN 50 END OF CONN) AS SHOWN, WITH WHITE INK (SCD-0004)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	15 FT		
	B	3FT		FOR USE BETWEEN PPB AND CARD TESTER

CABLE FUNCTION	
FROM A	AML
TO C	CLM
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	6-25	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED	[illegible]	6-24-76	CUSTOMER/NO. HSMIMP; DWG NO. IAMA-10; REV B

REVISION			
APPD	SYM	DESCR	DATE
EWH	A	REL PROD	5/24/78

3M CONNECTOR A PIN NO.	WIRE COLOR B	3M CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES	3M CONNECTOR A PIN NO.	WIRE COLOR B	3M CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
49 [3]	PURPLE	49 <1>				19 [18]	BROWN	19 <16>			
50	WHITE	50				20	WHITE	20			
47 [4]	BLUE	47 <2>				17 [19]	BLACK	17 <17>			
48	WHITE	48				18	WHITE	18			
45 [5]	GREEN	45 <3>				15 [20]	GRAY	15 <18>			
46	WHITE	46				16	WHITE	16			
43 [6]	YELLOW	43 <4>				13 [21]	PURPLE	13 <19>			
44	WHITE	44				14	WHITE	14			
41 [7]	ORANGE	41 <5>				11 [22]	BLUE	11 <20>			
42	WHITE	42				12	WHITE	12			
39 [8]	RED	39 <6>				9 [23]	GREEN	9 <21>			
40	WHITE	40				10	WHITE	10			
37 [9]	BROWN	37 <7>				7 [24]	YELLOW	7 <22>			
38	WHITE	38				8	WHITE	8			
35 [10]	BLACK	35 <8>				5 [25]	ORANGE	5 <23>			
36	WHITE	36				6	WHITE	6			
33 [11]	GRAY	33 <9>				3 [26]	RED	3 <24>			
34	WHITE	34				4	WHITE	4			
31 [12]	PURPLE	31 <10>				1 [27]	BROWN	1 <25>			
32	WHITE	32				2	WHITE	2			
29 [13]	BLUE	29 <11>									
30	WHITE	30									
27 [14]	GREEN	27 <12>									
28	WHITE	28									
25 [15]	YELLOW	25 <13>									
26	WHITE	26									
23 [16]	ORANGE	23 <14>									
24	WHITE	24									
21 [17]	RED	21 <15>									
22	WHITE	22									

AML BOARD J1 PIN NUMBERS (TYP)

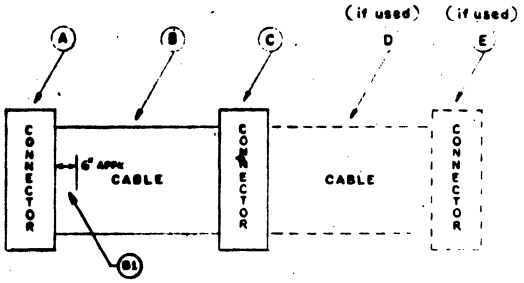
MLC CABLE TERMINATOR CARD PIN NUMBERS (TYP)

SCOTCHFLEX CONN PIN NUMBERS (TYP)

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	DRF	7/24/78	TITLE CABLE RUN-LIST	
CHECKED				
APPROVED	AJJT	8/1/78	CUSTOMER/NO. HSMIMP	DWG NO. IAMA-11 REV A

	REVISION		
APPD	SYM	DESCR	DATE
	A	REL PROD	8-21-75
LWH	B	ECN 0215	7-2-76



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	CONNECTOR PLUG, 50 PINS	3M	3417-3000	443
B	*	25 TW-PAIR CABLE	WOVEN	T25TP2807-UL1227N	49
C	1	CONNECTOR PLUG, 50 PINS	3M	3417-3000	443
B1	1	TIE-WRAP NAME	PANDUIT	PLF1M-CP	366

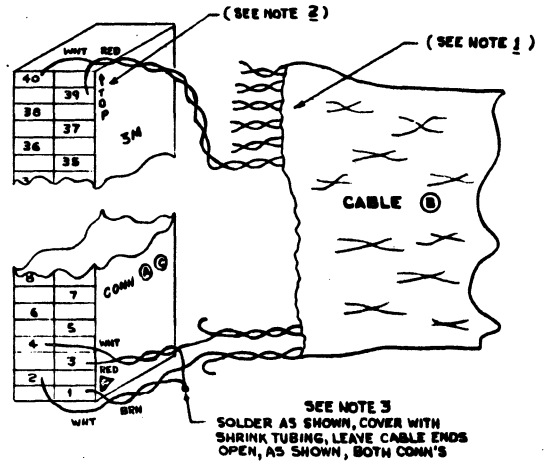
ASSEMBLY NOTES

1	CONNECT WIRES PER DWG IAMC-11, USE 1ST 20 PAIRS. (LEAVE LAST 5 PRS LOOSE AS SHOWN)
2	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 39 END OF CONN) AS SHOWN WITH WHITE INK (SCD-0004)
3	CUT WIRE SHOWN APPX 2" FROM CONN'S END AND SOLDER (LEAVE CABLE WIRES UNCONNECTED) COVER CONNECTION WITH SHRINK TUBING
4	CABLE TYPE & S/N TO BE MARKED (B1) WITH INDELIBLE FELT TIP PEN (BLK)

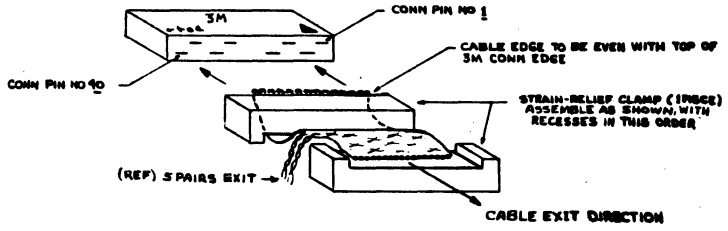
CABLE LENGTH

	TYPE	B	D	NOTES
(*)	A	15 FT.		
	B	3 FT.		FOR USE BETWEEN PPB AND CARD TESTER

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED
FOR ASSEMBLY DETAIL, SEE BELOW



CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	AML	DRAWN	DRF	9/12/75	TITLE	CABLE ASSEMBLY DETAILS	
TO C	CLM	CHECKED					
TO E		APPROVED	JT	9/14/75	CUSTOMER/NO. HSMIMP	DWG NO. IAMC-10	REV B

REVISION			
APPD	SYM	DESCR	DATE
LWH	A	REL PROD	6-24-75

3M CONNECTOR A PIN NO.	WIRE COLOR B	3M CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	3M CONNECTOR A PIN NO.	WIRE COLOR B	3M CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
39 [36]	RED	39 ⟨1⟩				9 [51]	GREEN	9 ⟨16⟩			
40	WHITE	40				10	WHITE	10			
37 [37]	BROWN	37 ⟨2⟩				7 [52]	YELLOW	7 ⟨17⟩			
38	WHITE	38				8	WHITE	8			
35 [38]	BLACK	35 ⟨3⟩				5 [53]	ORANGE	5 ⟨18⟩			
36	WHITE	36				6	WHITE	6			
33 [39]	GRAY	33 ⟨4⟩				3 [54]	RED	3 ⟨19⟩			CUT WIRES SHOWN APPX 2" FROM
34	WHITE	34				4	WHITE	4			CONN'S END AND SOLDER, LEAVE
31 [40]	PURPLE	31 ⟨5⟩				1 [55]	BROWN	1 ⟨20⟩			CABLE WIRES UNCONNECTED) COVER
32	WHITE	32				2	WHITE	2			CONNECTION WITH SHRINK TUBING
29 [41]	BLUE	29 ⟨6⟩									(SEE ASSY SKETCH DAMC-10)
30	WHITE	30									
27 [42]	GREEN	27 ⟨7⟩									
28	WHITE	28									
25 [43]	YELLOW	25 ⟨8⟩									
26	WHITE	26									
23 [44]	ORANGE	23 ⟨9⟩									
24	WHITE	24									
21 [45]	RED	21 ⟨10⟩									
22	WHITE	22									
19 [46]	BROWN	19 ⟨11⟩									
20	WHITE	20									
17 [47]	BLACK	17 ⟨12⟩									
18	WHITE	18									
15 [48]	GRAY	15 ⟨13⟩									
16	WHITE	16									
13 [49]	PURPLE	13 ⟨14⟩									
14	WHITE	14									
11 [50]	BLUE	11 ⟨15⟩									
12	WHITE	12									

SOLDER (JUMPER)

SCOTCHFLEX CONN PIN NUMBERS (TYP)

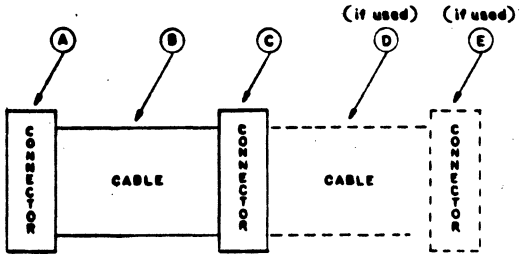
AML BOARD J1 PIN NUMBERS (TYP)

MLC CABLE TERMINATOR CARD PIN NUMBERS (TYP)

CABLES

BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	S.E.T.	7-15-75	TITLE: CABLE RUN-LIST
CHECKED	DEF	7-24-75	
APPROVED	MJT	7/21/75	CUSTOMER/NO. HSMIMP; DWG NO. IAMC-11; REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	9.24.74
	B	ECN 0124	1.22.75



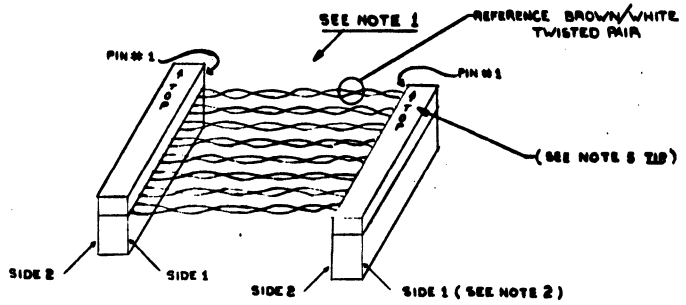
SYM	AMT	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	3M	3415-0001	53
B	(*)	25 TW PAIR CABLE	WOVEN CABLE	T25TP28O7 UL1227N	49
C	1	FEMALE CONN	3M	3415-0001	53

ASSEMBLY NOTES	
1	2 CABLES REQUIRED FOR EACH BUS COUPLER CARD (BCM, BCP & BCI)
2	CABLES MUST BE ASSEMBLED WITH CONNECTORS ORIENTATED AS SHOWN.
3	STRAIN RELIEFS INSTALLED PER SAN-12 (BOTH ENDS)
4	CABLE TYPE & S/N MARKED ON STRAIN-RELIEFS AT BOTH ENDS, WITH INDELIBLE FELT-TIP PEN (BLK).
5	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 1 END OF CONN) AS SHOWN, WITH WHITE INK (SCD-0004)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	5 FT		
(*)	-B	10 FT		
(*)	-C	15 FT		

PIN NUMBERING & ASSEMBLY DETAILS



CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	BCM OR BCP OR BCI	DRAWN	DRF	9/24/74	TITLE	CABLE ASSEMBLY DETAILS
TO C	BCM OR BCP OR BCI	CHECKED	[illegible]	9/24/74		
TO E		APPROVED	[illegible]	10/6/74	CUSTOMER/NO. HSMIMP	DWG NO. IBCA-10 REV B

REVISION			
APPD	SYM	DESCR	DATE
	A	ECL PROD	9.25.79

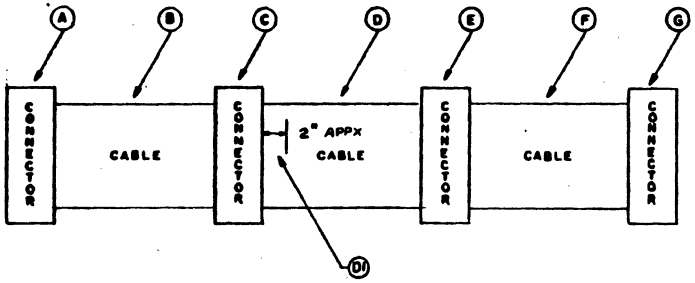
3M CONNECTOR A PIN NO.	WIRE COLOR B	3M CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO'S	3M CONNECTOR A PIN NO.	WIRE COLOR B	3M CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO'S
1	BROWN	1			1	29	BLUE	29			15
2	WHITE	2			1	30	WHITE	30			15
3	RED	3			2	31	PURPLE	31			16
4	WHITE	4			2	32	WHITE	32			16
5	ORANGE	5			3	33	GRAY	33			17
6	WHITE	6			3	34	WHITE	34			17
7	YELLOW	7			4	35	BLACK	35			18
8	WHITE	8			4	36	WHITE	36			18
9	GREEN	9			5	37	BROWN	37			19
10	WHITE	10			5	38	WHITE	38			19
11	BLUE	11			6	39	RED	39			20
12	WHITE	12			6	40	WHITE	40			20
13	PURPLE	13			7	41	ORANGE	41			21
14	WHITE	14			7	42	WHITE	42			21
15	GRAY	15			8	43	YELLOW	43			22
16	WHITE	16			8	44	WHITE	44			22
17	BLACK	17			9	45	GREEN	45			23
18	WHITE	18			9	46	WHITE	46			23
19	BROWN	19			10	47	BLUE	47			24
20	WHITE	20			10	48	WHITE	48			24
21	RED	21			11	49	PURPLE	49			25
22	WHITE	22			11	50	WHITE	50			25
23	ORANGE	23			12						
24	WHITE	24			12						
25	YELLOW	25			13						
26	WHITE	26			13						
27	GREEN	27			14						
28	WHITE	28			14						

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/29/79	TITLE	CABLE RUN-LIST
CHECKED	DK	9/5/79	CUSTOMER/NO.	DWG NO. / REV
APPROVED	DK	9/6/79	HSMIMP	1BCA-11 / A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	9.13.78



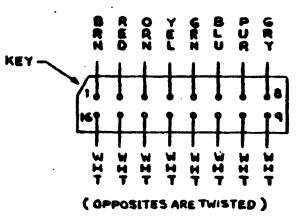
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN & CABLE ASSY	AUGAT	1P16-3T24-1	1528
B	*				
C	1	FEMALE CONN, 25 PIN	CINCH	DB25S	211
D	*	13 TW-PR CABLE	WOVEN	T13TP2807-UL1227N	48
E	1	MALE CONN, 25 PIN	CINCH	DB25P	353
F	*	13 TW-PR CABLE	WOVEN	T13TP2807-UL1227N	48
G	1	FEMALE CONN, 25 PIN	CINCH	DB25S	211
	4	TIE WRAP			793
D1	1	NAME TAG TIE WRAP	PANDUIT	PLFIM-CP	366

	ASSEMBLY NOTES
1	WIRE CONN'S (C),(E),(G) PER WIRE RUN LIST IFCA-11. FAN WIRES OUT OF CABLE (B) AND CONNECT TO CONN'S (C),(E),(G) PER WIRE RUN LIST IFCA-11
2	LEAD OUT 2 TW-PRS OF CABLE (B) (PER IFCA-11) 6" FROM CONN (C) AS SHOWN, ALSO CUT ALL UNUSED WIRES OF CABLE (B) AT CONN (C) EDGE AND TIE OFF
3	CABLE (D) & (F) EQUAL 1 CABLE. USING DAISY CHAIN WIRING METHODS, WIRE FROM (C) TO (E) TO (G) PER WIRE RUN LIST IFCA-11
4	CABLE TYPE & S/N TO BE MARKED ON (D1) WITH INDELIBLE FELT TIP PEN (BLK)

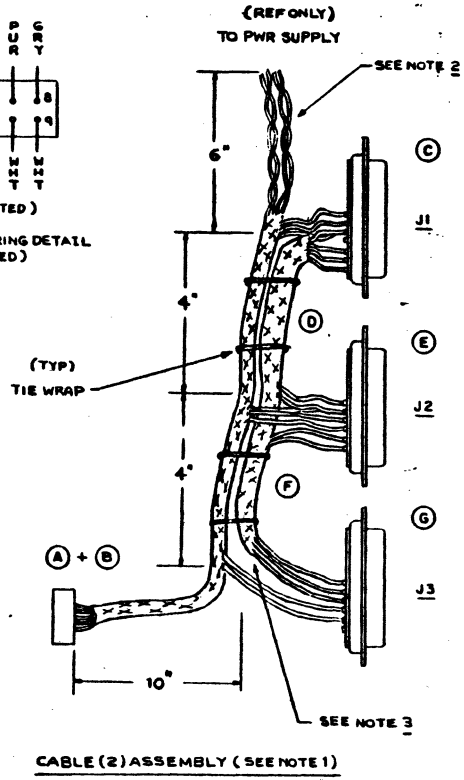
CABLE LENGTH

	TYPE	B	D	F	NOTES
(*)	A	10"	4"	4"	DEF = 1 CONTINUOUS CABLE

PIN NUMBERING & ASSEMBLY DETAILS



(A) AUGAT PLUG / CABLE WIRING DETAIL (PRE-ASSEMBLED)



CABLE (2) ASSEMBLY (SEE NOTE 1)

CABLE FUNCTION	
FROM A	FCL CARD
TO C	TFB-J1
TO E	TFB-J2
TO G	TFB-J3

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	11/16/77	TITLE: CABLE ASSEMBLY DETAILS
CHECKED	[illegible]	11/23/77	
APPROVED	[illegible]	11/30/77	CUSTOMER/NO. HSMIMP; DWG NO. IFCA-10; REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	9.13.78

(CINCH) CONNECTOR C PIN NO.	WIRE COLOR D	(CINCH) CONNECTOR E PIN NO.	WIRE COLOR F	(CINCH) CONNECTOR G PIN NO.	NOTES	(AUGAT) CONNECTOR A PIN NO.	WIRE COLOR B	(CINCH) CONNECTOR C PIN NO.	(CINCH) CONNECTOR E	(CINCH) CONNECTOR G PIN NO.	NOTES
1	YEL	1	YEL/WHT	1		1	BRN/WHT	14 (*)			
2	WHT	3		3		16				16	
3	ORN	2	ORN/WHT	N.C.		2	RED/WHT		15		
4	WHT	4		4		15					
5	RED	5	RED/WHT	5		3	ORN/WHT			2	
6	WHT	6		6		14					
7	BRN	7	BRN/WHT	7		4	YEL/WHT	17 (*)			
8	WHT	8		8		13					
9	BLK	9	BLK/WHT	9		5	GRN/WHT	3 (*)			
10	WHT	10		10		12					
11	GRY	11	GRY/WHT	11		6	BLU/WHT	7 (*)			
12	WHT	12		12		11					
13	VIO	13	VIO/WHT	13		7	PUR/WHT				PWR SUPPLY +12 V
14	WHT	16		N.C.		10					PWR SUPPLY +12 V
15	BLU	17	BLU/WHT	17		8	GRY/WHT				
16	WHT	14		14		9					PWR SUPPLY -12 V
17	GRN	NC	GRN/WHT	15							PWR SUPPLY -12 V
18	WHT	18		18							
19	YEL	19	YEL/WHT	19							
20	WHT	20		20							
21	ORN	21	ORN/WHT	21							
22	WHT	22		22							
23	RED	23	RED/WHT	23							
24	WHT	24		24							
25	BRN	25	BRN/WHT	25							
N.C.	WHT	N.C.		N.C.							

(*) - INDICATES THESE WIRES TO BE SOLDERED TO CINCH CONN PINS WITH WIRES FROM CABLE D-F

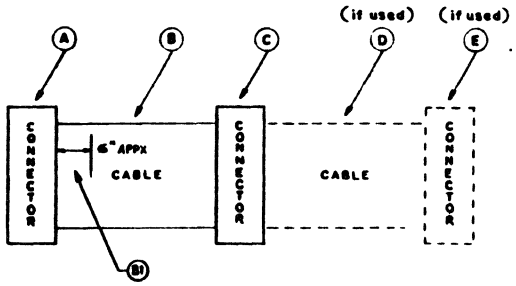
PURCHASED AUGAT CABLE

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	11/6/77	TITLE: CABLE RUN-LIST
CHECKED	JAT	9/30/78	CUSTOMER/NO.: HSMIMP
APPROVED	RK	9/30/78	DWG NO.: IFCA-11
			REV: A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	9.19.77
	B	ECN 0346	1.10.79



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE CONN	WINCHESTER ELECTRONICS	PGB-13A	
A1	10	CRIMP CONTACT (PIN)	" "	100-711265	
B	*	13PR TWIST'N'FLAT CABLE	SPECTA-STRIP	455-248-26	1659
C	1	FEMALE CONN	WINCHESTER ELECTRONICS	PGB-13A	
C1	10	CRIMP CONTACT (PIN)	" "	100-711265	
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

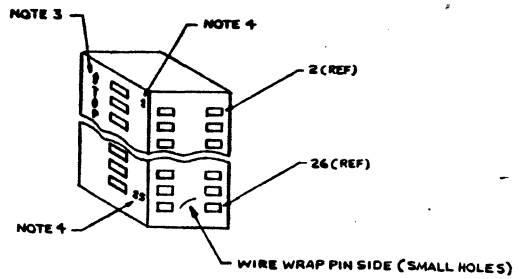
ASSEMBLY NOTES	
1	THE WIRE WRAP PIN NUMBERING DIFFERS FROM THE CONN (PGB)
	EX: #1 ON CONN (PGB) = #43 ON WIRE WRAP CONN (DYNATECH)
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
3	USING STAMP (SCD-0002), STAMP PAD (SCD-0003) MARK AS SHOWN
	WITH WHITE INK (SCD-0004)
4	PINS 1 & 25 TO BE MARKED AS SHOWN, WITH INDELIBLE FELT-TIP PEN (BLK)

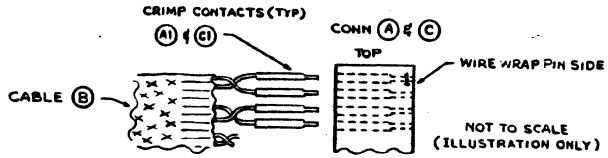
CABLE LENGTH

	TYPE	B	D	NOTES
*	A	5 FT		CUT CABLE TO LG IN CENTER OF FLAT AREA

PIN NUMBERING & ASSEMBLY DETAILS

CONN'S A & C





ASSEMBLY INSTRUCTIONS

1-CRIMP CONTACT PINS TO CABLE WIRES PER DWG IILJ-11, USING A CRIMPING TOOL (WINCHESTER # 107-0525 or equiv)

2-INSERT PINS INTO CONN'S A & C (SNAP FIT) PER DWG IILJ-11

CABLE FUNCTION	
FROM A	ILC # 1A
TO C	ILC # 1B
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	5/10/77
CHECKED	AT	9/18/77
APPROVED	AT	9/18/77

TITLE: CABLE ASSEMBLY DETAILS

CUSTOMER/NO.	DWG NO.	REV
HSMIMP	IILJ-10	B

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.19.77
JF	B	ECN0346	1.10.79

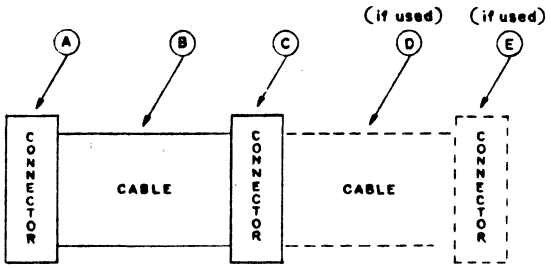
WINCHESTER CONNECTOR A PIN NO.	WIRE COLOR B	WINCHESTER CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES SIG NAMES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
N.C.	TAN	N.C									
N.C.	ORN	N.C.									
N.C.	TAN	N.C.									
N.C.	RED	N.C.									
N.C.	TAN	N.C.									
N.C.	BRN	N.C.									
N.C.	TAN	N.C.									
N.C.	BLK	N.C.									
N.C.	TAN	N.C.									
N.C.	WHT	N.C.									
N.C.	TAN	N.C.									
N.C.	GRY	N.C.									
N.C	TAN	N.C.									
N.C.	VIO	N.C.									
N.C.	TAN	N.C.									
N.C	BLU	N.C.									
17	TAN	17			RECCLK-						
18	GRN	18			RECCLK+						
19	TAN	19			RECDATA-						
20	YEL	20			RECDATA+						
21	TAN	21			TRANSCLK-						
22	ORN	22			TRANSCLK+						
23	TAN	23			TRANSLOOP+						
24	RED	24			TRANSLOOP-						
25	TAN	25			TRANSDATA+						
26	BRN	26			TRANSDATA-						

FOR PIN LOCATION ON CONN'S (TYP)
SEE DWG IILJ-10

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138				
DRAWN	JRF	5/2/77	TITLE	CABLE RUN-LIST
CHECKED	AT	8/8/77	CUSTOMER NO.	DWG NO. / REV
APPROVED	AT	8/12/77	HSMIMP	IILJ-11 / B

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	1.16.74
bk	B	ECN 0124	1.27.75



PIN NUMBERING & ASSEMBLY DETAILS

SEE NOTE 1

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	FEMALE LUG	T&B	.25 FASTON TAB	166
B	(*)	10AWG STRANDED WIRE	COLUMBIA	# 7804	218
		NEOPRENE INS. (RED	(OR EQUIV)		
C	1	FEMALE LUG	T&B	.25 FASTON TAB	166

ASSEMBLY NOTES	
1	8 WIRES REQUIRED FOR EACH POWER SUPPLY #5952

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	1.5 FT		

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	#5952 PWR. SUPPLY	DRAWN	DRF	1/24/74	TITLE	CABLE ASSEMBLY DETAILS
TO C	24 SLOT INFIBUS	CHECKED	bk	1/24/74	CUSTOMER/NO.	DWG NO. / REV
TO E		APPROVED	bk	1/24/74	HSMIMP	IJMP-10 / B

CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
TAB	RED	TAB			(*)						

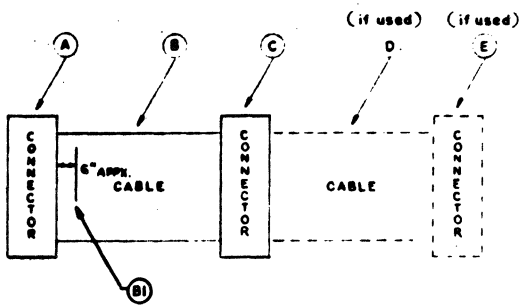
* 8 REQUIRED FOR EACH POWER SUPPLY #5952

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8/26/74	TITLE	CABLE RUN-LIST
CHECKED	CK	9/6/74	CUSTOMER/NO.	DWG NO.	REV
APPROVED	DK	9/10/74	HSMIMP	IJMP-11	A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	2.28.75
DJ	B	ECN 0188	2.28.75



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	50 PIN FEMALE CONN	CANNON	121-7326-125	372
		NOTE A & A1 AVAILABLE AS PKG FROM LEC		7770-1	
A1	50	CRIMP-PINS, FEMALE	CANNON	030-7312-011	210
B	(*)	15 TW PR CABLE	ALPHA	1327	357 or 356
			or BELDEN	8749	
C	1	25 PIN MALE CONN	CANNON / CINCH	DB-25P	353
C1	1	CONN HOOD	CANNON / CINCH	DB-20962	359
C2	2	JACKSCREW (MALE)	CANNON / CINCH	D20419-16	361
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
2	USE HEAT-SHRINK TUBING (½" DIA) AT POINT WHERE JACKET STOPS, ON BOTH ENDS
3	AT (A) ALLOW 5" UNJACKETED PAIRS FOR FLEXIBILITY, BUT LACE BUNDLE
4	INSERT ALL PINS (50), INCLUDING UNUSED PINS, IN (A)
5	CRIMP PINS WITH CANNON CCT-UBC HAND CRIMPER AT (A)
6	AT (C) BUNDLE THE INDICATED WIRES TO PIGTAILS, TO PINS 18, 23 & 25
7	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 49 END OF CONN)
	AS SHOWN, WITH WHITE INK (SCD-0004)

CABLE LENGTH

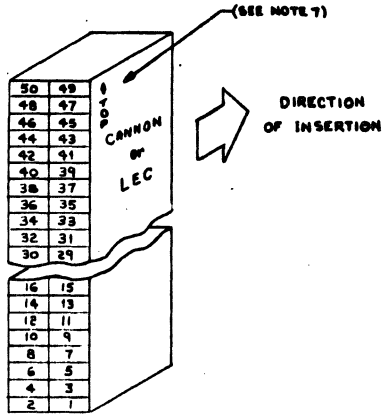
	TYPE	B	D	NOTES
(*)	-A	10 FT		
(*)	-B	5 FT		

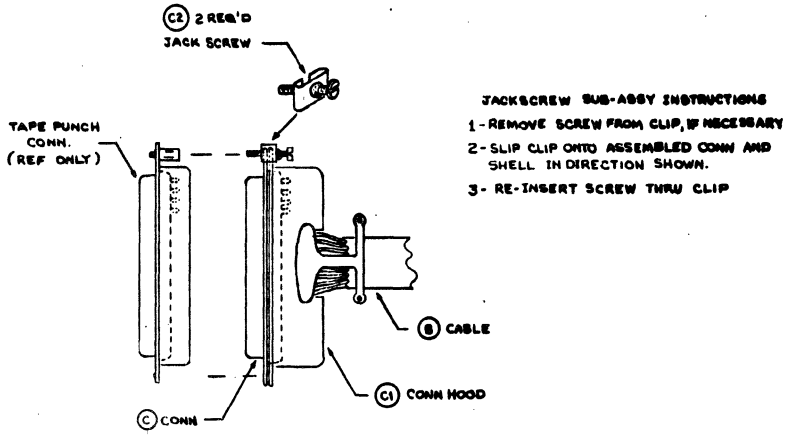
PIN NUMBERING & ASSEMBLY DETAILS

VIEW FROM CABLE SIDE, UNASSEMBLED (A)

(SEE ASSY NOTES)

LEC CANNON CONNECTORS ARE UNNUMBERED, SCHEME BELOW IS 3M CONN NUMBERING SYS. (REF ONLY)





JACKSCREW SUB-ASSY INSTRUCTIONS

1 - REMOVE SCREW FROM CLIP, IF NECESSARY

2 - SLIP CLIP ONTO ASSEMBLED CONN AND SHELL IN DIRECTION SHOWN.

3 - RE-INSERT SCREW THRU CLIP

CABLE FUNCTION	
FROM A	PPB
TO C	REMEX PAPER TAPE PUNCH
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	2.28.75	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED			CUSTOMER/NO.: CCP; DWG NO.: 1PTP-10; REV: B

REVISION			
ALL	SYM	DESCR	DATE
	A	ROLL THRU	2-15-77

50 PIN CANNON CONNECTOR A PIN NO. LEC 73-( )	WIRE COLOR B	DB25 P CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
17 (A17)	RED	1			DATA BIT 1						
18 (B17)	BLACK	18			GND						
19 (A16)	WHT	2			2						
20 (B16)	BLACK	18			GND						
21 (A15)	GREEN	3			3						
22 (B15)	BLACK	19			GND						
23 (A14)	BLUE	4			4						
24 (B14)	BLACK	18			GND						
25 (A13)	BROWN	5			5						
26 (B13)	BLACK	25			GND						
27 (A12)	YELLOW	6			6						
28 (B12)	BLACK	23			GND						
29 (A11)	ORANGE	7			7						
30 (B11)	BLACK	25			GND						
31 (A10)	GREEN	8			8						
32 (B10)	RED	25			GND						
37 (A7)	WHT	11			START PUNCH CYCLE						
38 (B7)	RED	25			GND						
45 (A3)	BLUE	12			PUNCH DATA CALL						
46 (B3)	RED	25			GND						
43 (A4)	YELLOW	20			PUNCH NOT READY						
44 (B4)	RED	25			GND						
15 (A18)	JUMPER										
16 (B18)											
UNUSED PAIRS NOT CONNECTED											

NOTES

1 - ALPHA & BELDEN USE THE SAME PAIR COLORING BUT NUMBER DIFFERENT. WIRE AS ABOVE AND IGNORE BELDEN GUIDE.

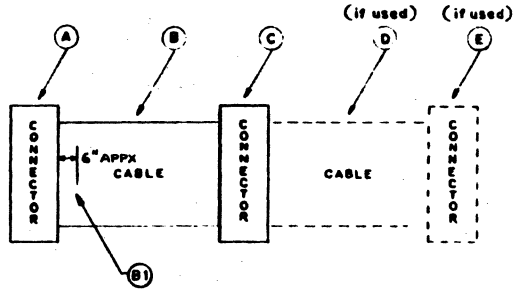
2 - WIRE ABOVE, USING ASSY NOTES ON DWG IPTP-10 AS REF. GUIDES.

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	S.E.T.	2/15/77	TITLE: CABLE RUN-LIST
CHECKED			CUSTOMER/NO.: CCP; DWG NO.: IPTP-11; REV: A
APPROVED		2/18/77	

APPD	REVISION SYM	DESCR	DATE
	A	REL PROD	2.28.75
	B	ECN 0153	7.25.75
	C	ECN 0312	7.18.78



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	40 PIN FEMALE CONN	CANNON	121-7326-120	355
		NOTE (A) & (A1) AVAILABLE AS PKG FROM LEC.		7771-1	
A1	22	CRIMP-PINS, FEMALE	CANNON	030-7312-011	210
B	(*)	15 TW PR. CABLE	ALPHA	1327	356
			or BELDEN	8749	
C	1	25 PIN RS232 TYPE (F)	CANNON / CINCH	DB-25S	211
C1	1	CONN HOOD	CANNON / CINCH	DB-20962	359
C2	2	JACKSCREW (MALE)	CANNON / CINCH	D20419-16	361
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES

1	CABLE TYPE & SIN TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	USE HEAT-SHRINK TUBING [½" DIA] AT POINT WHERE JACKET STOPS, ON BOTH ENDS
3	AT (A) ALLOW 5" ON JACKETED PAIRS FOR FLEXIBILITY, BUT LACE BUNDLE
4	CRIMP PINS WITH CANNON CCT-UBC HAND CRIMPER AT (A)
5	AT (C) BUNDLE THE INDICATED 6 WIRES WITH A PIGTAIL TO PIN 12
	AT (C) BUNDLE THE INDICATED 5 WIRES WITH A PIGTAIL TO PIN 13
6	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 39 END
	OF CONN) AS SHOWN WITH WHITE INK (SCD-0004)

CABLE LENGTH

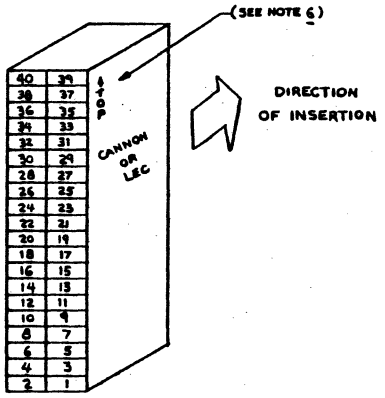
	TYPE	B	D	NOTES
(*)	-A	10 FT		
(*)	-B	5 FT		

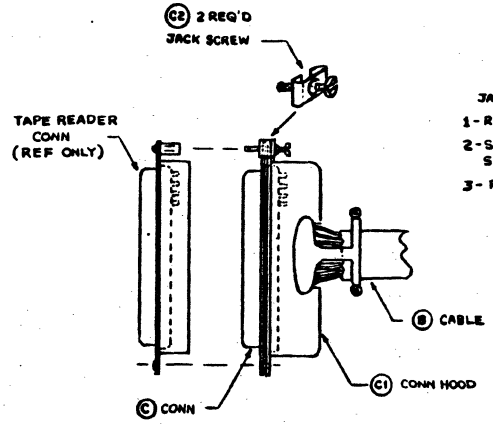
PIN NUMBERING & ASSEMBLY DETAILS

VIEW FROM CABLE SIDE, UNASSEMBLED (A)

(SEE ASSY NOTES)

LEC/CANNON CONNECTOR ARE UNUMBERED. SCHEME BELOW IS 3M CONN NUMBERING SYS. (REF ONLY)





JACKSCREW SUB-ASSY INSTRUCTIONS

1- REMOVE SCREW FROM CLIP, IF NECESSARY.

2- SLIP CLIP ONTO ASSEMBLED CONN AND SHELL IN DIRECTION SHOWN.

3- RE-INSERT SCREW THRU CLIP

CABLE FUNCTION (INTERNAL REMEX RR-6300 PTR)	
FROM A	PPB
TO C	REMEX PAPER TAPE READER
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	12 Jan 75	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED	[illegible]	7/24/75	CUSTOMER/NO. HSMIMP · DWG NO. IRTR-10 · REV C

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL TO P	

CANNON CONNECTOR A PIN NO.	WIRE COLOR B	REMEX-MATE CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR (NOTE 1)	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
39	RED	14			1 $\overline{\text{SYS READY}}$						
15	BLACK	13			1 GND						
37	WHITE	9			2 DATA READY						
38	BLACK	13			2 GND						
35	GREEN	16			3 $\overline{\text{DRIVE RIGHT}}$						
36	BLACK	13			3 GND						
31	BLUE	1			4 DATA BIT (1)						
32	BLACK	12			4 GND						
29	BROWN	2			5 DATA BIT (2)						
30	BLACK	12			5 GND						
27	YELLOW	3			6 DATA BIT (3)						
28	BLACK	12			6 GND						
25	ORANGE	4			7 DATA BIT (4)						
26	BLACK	12			7 GND						
23	GREEN	5			8 DATA BIT (5)						
24	RED	12			8 GND						
21	WHITE	6			9 DATA BIT (6)						
22	RED	12			9 GND						
19	BLUE	7			10 DATA BIT (7)						
20	RED	13			10 GND						
17	YELLOW	8			11 DATA BIT (8)						
18	RED	13			11 GND						
		10 } JUMPER			MODE SELECT						
		11 } TOGETHER			GND						
		15, 17 ⟷ 25	NO CONNECTION		—						
		(UNUSED PAIRS NOT CONNECTED)									

NOTES

1 - ALPHA & BELDEN USE THE SAME PAIR COLORING BUT NUMBER DIFFERENT. WIRE AS ABOVE AND IGNORE BELDEN GUIDE.

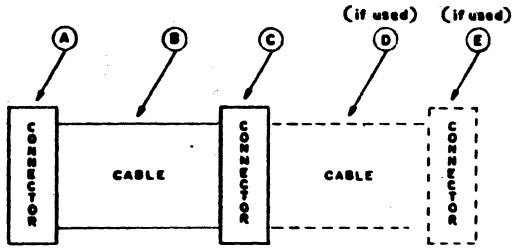
2 - WIRE ABOVE, USING ASSY NOTES ON DWG IPTR-10 AS REF. GUIDES.

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	TITLE	CABLE RUN-LIST
CHECKED			
APPROVED		CUSTOMER NO. HSMIMP	DWG NO. IPTR-11 REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL FROM	2-20-75



SYM	AMT	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	8	FEMALE CONN	3M	3416-0001 (16 PIN)	207
B	(*)	4 PR TW FLAT CABLE	WOVEN CABLE	T4TP2807 UL1227N	208
C	1	FEMALE CONN	3M	3415-0001	53
				(CARD EDGE CONN)	

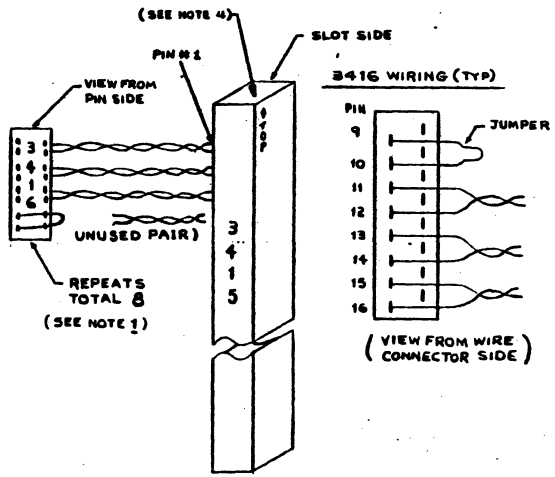
ASSEMBLY NOTES

4	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN
	1 END OF CONN) AS SHOWN, WITH WHITE INK (SCD-0004)
1	THIS CABLE ASSEMBLY IS MADE UP OF (8) 3416 CONNECTORS
	FEEDING INTO (1) 3415 CONNECTOR
2	ADD STRAIN RELIEF ON 3415 CONNECTOR PER SAN-12
3	CABLE TYPE & S/N TO BE MARKED ON STRAIN RELIEF WITH
	INDELIBLE FELT-TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	2.5 FT		8 RUNS PER CABLE

PIN NUMBERING & ASSEMBLY DETAILS



CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
FROM A	MLR/MHR (1-8)	DRAWN	DRF	3/15/75	TITLE	CABLE ASSEMBLY DETAILS	
TO C	RLD	CHECKED	MFK	2/24/75			
TO E		APPROVED	MFK	2/25/75	CUSTOMER/NO. HSMIMP	DWG NO. IRLD-10	REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	PCL PROD	2-28-75

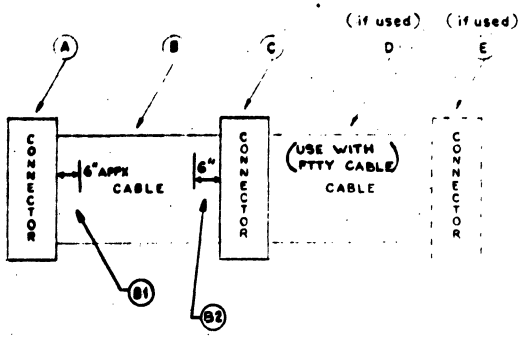
3416 CONNECTOR A PIN NO.	WIRE COLOR B	3415 CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO.	3416 CONNECTOR A PIN NO.	WIRE COLOR B	3415 CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
16	BROWN	1			1A CLK+	16	BROWN	25	1E CLK+		
15	WHITE	2			1A CLK-	15	WHITE	26	1E CLK-		
14	RED	3			2A DAT+	14	RED	27	2E DAT+		
13	WHITE	4			2A DAT-	13	WHITE	28	2E DAT-		
12	ORANGE	5			3A GO+	12	ORANGE	29	3E GO+		
11	WHITE	6			3A GO-	11	WHITE	30	3E GO-		
10	JUMPER	N.C.				10	JUMPER	N.C.			
9		N.C.				9		N.C.			
16	BROWN	7			1B CLK+	16	BROWN	31	1F CLK+		
15	WHITE	8			1B CLK-	15	WHITE	32	1F CLK-		
14	RED	9			2B DAT+	14	RED	33	2F DAT+		
13	WHITE	10			2B DAT-	13	WHITE	34	2F DAT-		
12	ORANGE	11			3B GO+	12	ORANGE	35	3F GO+		
11	WHITE	12			3B GO-	11	WHITE	36	3F GO-		
10	JUMPER	N.C.				10	JUMPER	N.C			
9		N.C.				9		N.C.			
16	BROWN	13			1C CLK+	16	BROWN	37	1G CLK+		
15	WHITE	14			1C CLK-	15	WHITE	38	1G CLK-		
14	RED	15			2C DAT+	14	RED	39	2G DAT+		
13	WHITE	16			2C DAT-	13	WHITE	40	2G DAT-		
12	ORANGE	17			3C GO+	12	ORANGE	41	3G GO+		
11	WHITE	18			3C GO-	11	WHITE	42	3G GO-		
10	JUMPER	N.C				10	JUMPER	N.C.			
9		N.C.				9		N.C.			
16	BROWN	19			1D CLK+	16	BROWN	43	1H CLK+		
15	WHITE	20			1D CLK-	15	WHITE	44	1H CLK-		
14	RED	21			2D DAT+	14	RED	45	2H DAT+		
13	WHITE	22			2D DAT-	13	WHITE	46	2H DAT-		
12	ORANGE	23			3D GO+	12	ORANGE	47	3H GO+		
11	WHITE	24			3D GO-	11	WHITE	48	3H GO-		
10	JUMPER	N.C.				10	JUMPER	N.C.			
9		N.C.				9		N.C.			

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	8-13-75	TITLE	CABLE RUN-LIST
CHECKED	MFK	2-28-75	CUSTOMER/NO. HSMIMP	DWG NO. IRLD-1 REV A
APPROVED	MFK	3-17-75		

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	4/25/75



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN I/O CONN	CANNON	121-7326-110	209
		NOTE (A) & (A1) AVAILABLE AS PKG FROM LEC		7770-1	
A1	20	CRIMP-PINS, FEMALE	CANNON	030-7312-011	210
B	(#)	5 COND, 22 AWG CABLE	BELDEN	8445 (or equiv)	212
C	1	CONN. MALE	CANNON / CINCH	DB-25 P	353
C1	2	SCREW-LATCH SOCKET	CANNON / CINCH	D-20418-2	429
C2	1	CONNECTOR HOOD	CANNON / CINCH	DB-20962	359
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF 1M-CP	366
B2	1	TIE-WRAP NAME TAG	PANDUIT	PLF 1M-CP	366

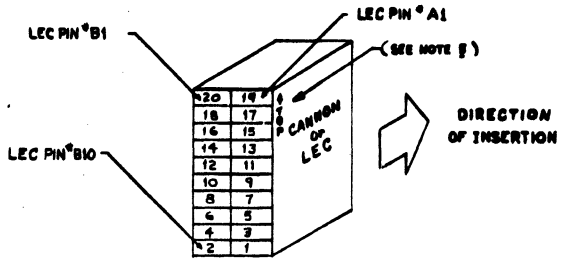
ASSEMBLY NOTES

1	CRIMP PINS (A1) WITH CANNON HAND CRIMPER # CCT-UBC
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
3	AT (A) CRIMP 4" PIECE OF WIRE ON ALL UNUSED PINS, USE MULTI TIE-WRAPS OR LACE, TO PROVIDE STRAIN RELIEF
4	WRAP OR TAPE CABLE AT (C) AS REQUIRED FOR STRAIN-RELIEF
5	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 19 END OF CONN) AS SHOWN, WITH WHITE INK (SCD-0004)
6	MARK "FULL DUPLEX, 20 MIL" ON B2 WITH BLACK FELT TIP PEN

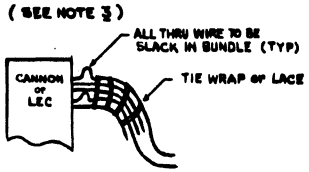
CABLE LENGTH

	TYPE	B	D	NOTES
(#)	-A	5 FT		

PIN NUMBERING & ASSEMBLY DETAILS



VIEW FROM CABLE SIDE, UNASSEMBLED (A)



CABLE FUNCTION	
CURRENT-LOOP TTY	
FROM A	PSB
TO C	FTTY CABLE WITHOUT FANTAIL
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	4/18/75	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED		4/21/75	CUSTOMER/NO.: HSMIMP; DWG NO.: ITTC-10; REV: A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	8-22-75

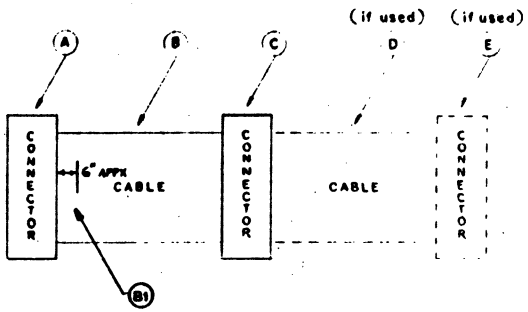
3M (20 PIN) CONNECTOR A PIN NO. 3M	PIN NO. LEC	WIRE COLOR B	CINCH (25 PIN) CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
16	B3	WHT	16			PRINTER +
14	B4	BLK	14			PRINTER -
12	B5	RED	12			KEYBOARD +
10	B6	GREEN	10			KEYBOARD -
		BROWN NOT USED				
	(REF ONLY)					

CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	DRF	8-19-75	TITLE	CABLE RUN-LIST
CHECKED				
APPROVED		8/24/75	CUSTOMER/NO. HSMIMP	DWG NO. ITTC-1 REV A

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	8-22-75



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 COND FEMALE CONN	CANNON	121-7326-110	209
A1	20	PINS, FEMALE CONN	CANNON	030-7812-011	210
B	(#)	5 COND. 22 AWG CABLE	BELDEN	8445	212
		(OR EQUIV)			
C	1	FEMALE CONN	CINCH / CANNON	DB-25S	211
C1	1	CONNECTOR HOOD	CINCH / CANNON	DB*20962	359
C2	2	SCREW-LATCH SOCKET	CINCH	D-20418-2	429
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

NOTE: ITEMS (A) & (A1) AVAILABLE AS KIT FROM LEC (PN 7770-1)

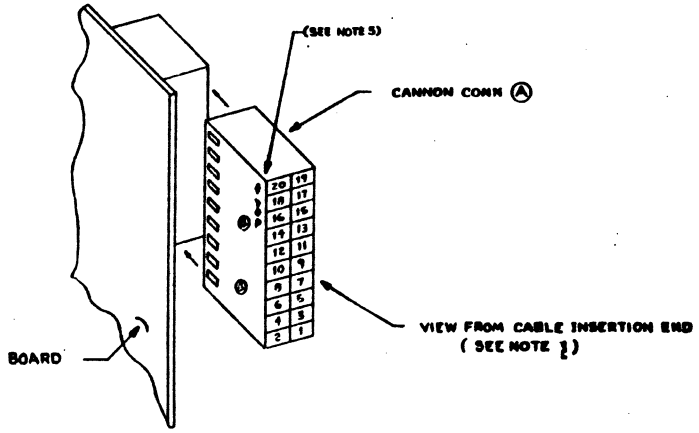
ASSEMBLY NOTES

1	CRIMP PINS (A1) WITH CANNON HAND CRIMPER # CCT-UBC
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
3	AT (A) CRIMP 4" PIECE OF WIRE ON ALL UNUSED PINS, USE MULTI TIE-WRAPS OR LACE, TO PROVIDE STRAIN RELIEF
4	WRAP OR TAPE CABLE AT (C) AS REQUIRED FOR STRAIN-RELIEF
5	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 19 END OF CONN)
	AS SHOWN, WITH WHITE INK (SCD-0004)

CABLE LENGTH

	TYPE	B	D	NOTES
(#)	-A	10 FT		

PIN NUMBERING & ASSEMBLY DETAILS



(SEE NOTE 3)

CABLE FUNCTION	
INFOTON or EIA TERMINAL	
FROM A	PSB
TO C	EIA CABLE WITHOUT FANTAIL
TO E	

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS 02138

DRAWN	DRF	8/18/75	TITLE	CABLE ASSEMBLY DETAILS	
CHECKED					
APPROVED			CUSTOMER/NO. HSMIMP	DWG NO. ITTR-10	REV A

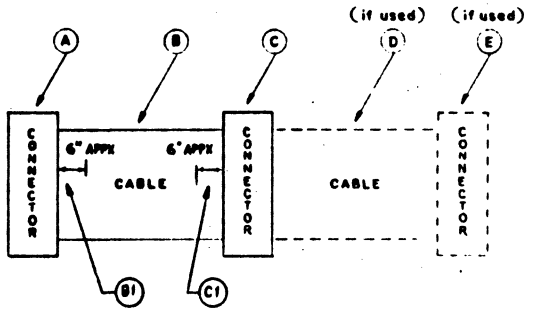
REVISION			
APPD	SYM	DESCR	DATE
JM	A	REL PROD	8-22-75

CANNON CONNECTOR A PIN NO.	WIRE COLOR B	CINCH CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES TERMINAL SIGNAL IDENT	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
19 (A1)	WHITE	3			BB RCV DATA						
11 (A5)	GREEN	5			CB CLEAR TO SEND	DERIVED FROM NOTE: DATA-TERM-READY SIGNAL ON PSB CARD					
		8 JUMPER ALL 3			CF CARRIER DETECT						
		6 TO GREEN WIRE			CC DATA SET READY						
5 (A8)	BLACK	2			BA TRANS DATA						
1 (A10)	BROWN	7			GND						
(REF ONLY)											
3 (A9)	RED	20			CD DATA TERM READY	NOTE: TO CLEAR-TO-SEND ON PSB CARD					
CARDJ1-( )											

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
DRAWN	S.E.T.	5-75	TITLE	CABLE RUN-LIST	
CHECKED					
APPROVED	[illegible]	8/1/75	CUSTOMER/NO. HSMIMP	DWG NO. ITTR-11	REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	P.M.K.



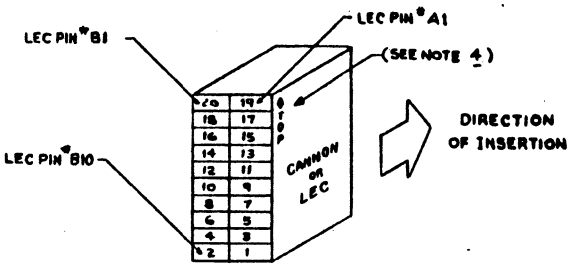
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	20 PIN I/O CONN	CANNON	121-7326-110	209
		NOTE (A) & (A1) AVAILABLE AS PKG FROM LEC		7770-1	
A1	20	CRIMP-PINS, FEMALE	CANNON	030-7312-011	210
B	(*)	5 COND, 22 AWG CABLE	BELDEN	8445 (OR EQUIV)	212
C	4	#6 SPADE LUG (CRIMP)	BURNDY OR	BA16F8	384
			AMP	60199-1	384
B1	1	TIE WRAP NAME TAG	PANDUIT	PLF1M-CP	366
C1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

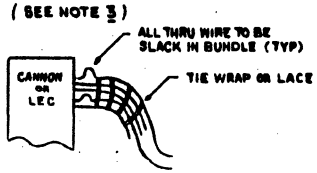
ASSEMBLY NOTES	
1	CRIMP PINS (A1) WITH CANNON HAND CRIMPER # CCT-UBC
2	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)
3	CRIMP 4" PIECE OF WIRE ON ALL UNUSED PINS, LACE TO PROVIDE STRAIN RELIEF
4	USING STAMP (SCD-0002) & STAMP PAD (SCD-0003) MARK (ON PIN 19 END OF CONN)
	AS SHOWN, WITH WHITE INK (SCD-0004)
5	MARK ON (C1) "20 MA. FULL DUPLEX" WITH INDELIBLE FELT-TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	10 FT		

PIN NUMBERING & ASSEMBLY DETAILS





VIEW FROM CABLE SIDE, UNASSEMBLED (A)

CABLE FUNCTION CURRENT LOOP TTY						
FROM A	PSB	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
TO C	CURRENT LOOP TTY	DRAWN	DRF	2/10/76	TITLE	CABLE ASSEMBLY DETAILS
TO E		CHECKED				
		APPROVED			CUSTOMER/NO. HSMIMP	DWG NO. ITTY-10 REV A

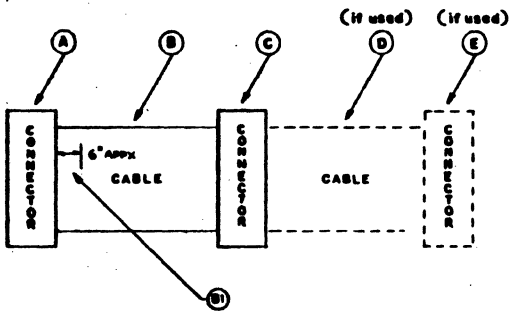
REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.8.74

CANNON 20 PIN CONNECTOR A PIN NO.	WIRE COLOR B	SPADE LUGS CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
3M (LEC)		TELETYPE T.B.#									
16 (B3)	WHITE	7			PRINTER +						
14. (B4)	BLACK	6			PRINTER -						
12 (B5)	RED	4			KEY BOARD +						
10 (B6)	GREEN	3			KEY BOARD -						
	BROWN NOT USED										
	(REF ONLY)										

CABLES

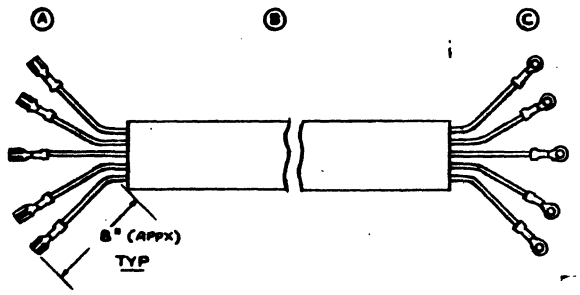
COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138			
DRAWN	DRF	2/19/74	TITLE: CABLE RUN-L ST
CHECKED			
APPROVED	[signature]	2/19/74	CUSTOMER/NO. HSMIMP; DWG NO. ITTY-11; REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	8.4.77
	B	ECN 274	1.3.78
	C	ECN 316	8.7.78



SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	5	TERMINAL LUG	T & B	RB14-250F	1048
B	*	#16 AWG, 5 COND CABLE	ALPHA	# 4105	1113
C	5	RING TERMINAL	T & B	RB14-6	924
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM-CP	366

PIN NUMBERING & ASSEMBLY DETAILS



ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)

CABLE LENGTH

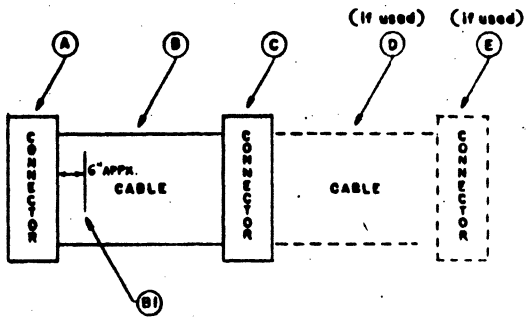
	TYPE	B	D	NOTES
(*)	A	6 FT		

NOTE: THERE IS NO DWG PILC-11

CABLE FUNCTION							
FROM A	I/O FWR BACK PLANE	COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138					
TO C	LCE LEVEL CONVERTER ENCLOSURE	DRAWN	DRF	6/8/77	TITLE	CABLE ASSEMBLY DETAILS	
TO E		CHECKED		9/12/77	CUSTOMER/NO.	DWG NO.	REV
		APPROVED		9/10/77	HSMIMP	PILC-11	C

CABLES

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	7.8.74
	B	ECN 0128	8.29.75



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO.
A	1	FEMALE CONN	HUBBELL	45235 "TWIST LOCK"	198
		(TRIANGULAR KEY SHAPE)			
B	(*)	5 WIRE, #8 AWG			201
		TYPE, SO PWR CABLE			
C	1	MALE CONN	HUBBELL	45215 "TWIST LOCK"	197
		(TRIANGULAR KEY SHAPE)			
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE
	FELT-TIP PEN (BLK

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	20 FT		

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	PDU	DRAWN	DHP	8/4/75	TITLE CABLE ASSEMBLY DETAILS	
TO C	SITE, 3PH, 30A. SERV.	CHECKER	[illegible]	8/11/75		
TO L		APPROVED	[illegible]	8/29/75	CUSTOMER/NO. HSMIMP	DWG NO. PWRA-10 REV B

REVISION			
APPD	SYM	DESCR	DATE
	A	REL PROD	11-15-76

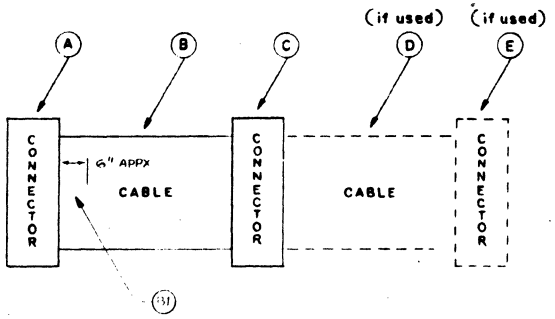
CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES PAIR NO. & SIG NAME	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
X	RED	X			G1						
Y	# ORANGE	Y			G2						
Z	# BLACK	Z			G3						
N	WHITE	N			NEUTRAL						
G (SCREW)	GREEN	G (SCREW)			PROT. GND						

PER HUBBELL CATALOG # 31 - PAGE 015

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
DRAWN	DRF	11/15/76	TITLE	CABLE RUN-LIST
CHECKED	DLK	11/17/76	CUSTOMER/NO.	DWG NO. / REV
APPROVED	DLK	11/24/76	HSMIMP	PWRA-11 / A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77



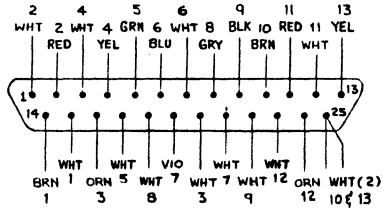
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN. 25 PIN	CINCH	DBM25P	353
A1	1	PLASTIC BACKSHELL	AMPHENOL	17-1372	526
A2	2	DISC LATCHES	CANNON	D-110278	367
B	*	13 TW-PAIR CABLE	WOVEN	T13TP2807-UL1227	48
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
*	A	3.5 FT		

PIN NUMBERING & ASSEMBLY DETAILS



CONNECTOR (A) TW-PR WIRING SEQUENCE

CABLE FUNCTION		COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS. 02138				
FROM A	RED CNT PNL (J6)	DRAWN	DRF	11/22/77	TITLE	CABLE ASSEMBLY DETAILS
TO C	FILTER PNL (TB 4,5,6)	CHECKED				
TO E		APPROVED	ABL	11/28/77	CUSTOMER/NO. HSMIMP	DWG NO. SBRS-10 REV A

APP'D	REVISION		
	SYM	DESCR	DATE
	A	PEL PROD	11.28.77

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	FILTER PANEL TERM BOARDS NOTES (REF ONLY)	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
14	BRN/WHT		ISO13		TB6-3						
15	/WHT		ISOZZ		TB6-5						
2	RED/WHT		ISO01		TB4-3						
1	/WHT		ISO00		TB4-1						
16	ORN/WHT		ISO15		TB6-7						
20	/WHT		GND		TB6-12						
4	YEL/WHT		ISO03		TB4-7						
3	/WHT		ISO02		TB4-5						
5	GRN/WHT		ISO04		TB4-9						
17	/WHT		GND		TB4-12						
6	BLU/WHT		ISO05		TB4-11						
7	/WHT		ISO06		TB5-1						
19	VIO/WHT		ISOXX		TB6-9						
21	/WHT		GND		TB6-10						
8	GRY/WHT		ISO07		TB5-3						
18	/WHT		GND		TB5-12						
9	BLK/WHT		ISO08		TB5-5						
22	/WHT		ISOYY		TB6-11						
10	BRN/WHT		ISO09		TB5-7						
25	/WHT		GND		N.C.						
11	RED/WHT		ISO10		TB5-9						
12	/WHT		ISO11		TB5-11						
24	ORN/WHT		TPREP		PREP FILTER						
23	/WHT		GND		GND LUG, PREP FILTER						
13	YEL/WHT		ISO12		TB6-1						
25	/WHT				N.C.						
(SEE NOTE 1)			↑								
			(SIG NAMES)								

NOTES

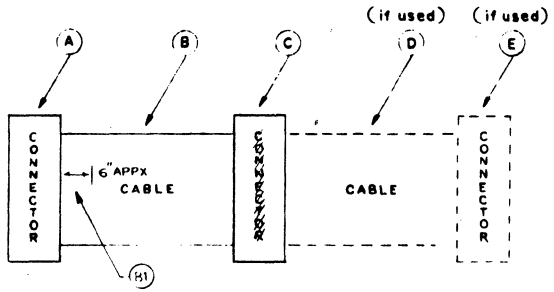
1 – WHITE WIRE OF # 13 PAIR (YEL/WHT) SOLDER TO PIN # 25 OF CONN 'A'

CABLES

COMPUTER SYSTEMS DIVISION
BOLT, BERANEK & NEWMAN INC.
CAMBRIDGE, MASS. 02138

DRAWN	DRF	12/7/77	TITLE	CABLE RUN-LIST	
CHECKED					
APPROVED	AEL	12/8/77	CUSTOMER/NO. HSMIMP	DWG NO. SBRS-11	REV A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77



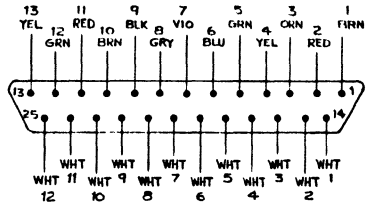
SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	MALE CONN, 25 PIN	CINCH	DB-25P	353
B	(*)	13 TW-PAIR CABLE	WOVEN CABLE	T13TP2807-UL1227N	48
B1	1	TIE-WRAP NAME TAG	PANDUIT	PLF1M-CP	366

ASSEMBLY NOTES	
1	CABLE TYPE & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT-TIP-PEN (BLK)

CABLE LENGTH

	TYPE	B	D	NOTES
*	A	2.5 FT		

PIN NUMBERING & ASSEMBLY DETAILS



CONNECTOR (A) TW-PR WIRING SEQUENCE

CABLE FUNCTION	
FROM A	FILTER BOX (J11)
TO C	CAPACITOR BOX
TO E	

COMPUTER SYSTEMS DIVISION
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DRAWN	DRF	11/27/77	TITLE: CABLE ASSEMBLY DETAILS
CHECKED			
APPROVED	ABL	11/28/77	CUSTOMER/NO.: HSMIMP; DWG NO.: SRBS-10; REV: A

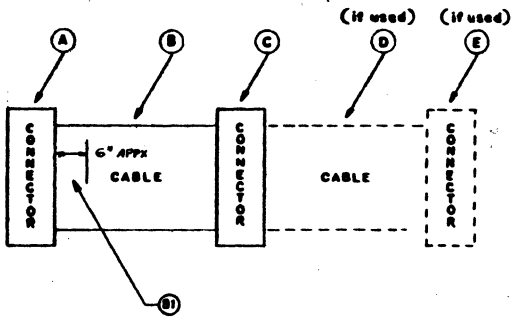
REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	11.28.77

CINCH CONNECTOR A PIN NO.	WIRE COLOR B	CAPACITOR BOX CONNECTOR D PIN NO. REF ONLY	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES SIG NAMES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	if used WIRE COLOR D	if used CONNECTOR E PIN NO.	NOTES
1	BROWN	XFCW (C12) + GND			XFCW						
14	WHITE	GND									
2	RED	C1			RBW0-						
15	WHITE	GND									
3	ORANGE	C2			RBW1-						
16	WHITE	GND									
4	YELLOW	C3			RBW2-						
17	WHITE	GND									
5	GREEN	C4			RBW3-						
18	WHITE	GND									
6	BLUE	C5			RBW4-						
19	WHITE	GND									
7	VIOLET	C6			RBW5-						
20	WHITE	GND									
8	GRAY	C7			RBW6-						
21	WHITE	GND									
9	BLACK	C8			RBW7-						
22	WHITE	GND									
10	BROWN	C9			B2RWE-						
23	WHITE	GND									
11	RED	C10			RRFR-						
24	WHITE	GND									
12	ORANGE	C11			RBBR-						
25	WHITE	GND									
13	YELLOW	N.C.									
12	WHITE	N.C.									

CABLES

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138			
DRAWN	DRF	11-22-77	TITLE: CABLE RUN-LIST
CHECKED			
APPROVED	ABL	11-28-77	CUSTOMER/NO.: HSMIMP; DWG NO.: SRBS-11; REV: A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2-4-79



PIN NUMBERING & ASSEMBLY DETAILS

SYM	AM'T	PART DESCRIPTION	MANUFACTURER	PART NUMBER	BBN NO
A	1	12 PIN ROUND CONN (MALE)	CANNON	GK12-22C-1/2	1700
B	#	13 PR TWIST'N FLAT CABLE	SPECTRA-STRIP	455-248-26	1659
C	1	12 PIN ROUND CONN (FEMALE)	CANNON	GK12-21C-1/2	1115
B1	1	TIE WRAP NAME TAG	PANDUIT	PLFIM	366
B2	as req'd	ELECTRICAL TAPE (BLK)	—	—	1056

ASSEMBLY NOTES	
1	CABLE TYP & S/N TO BE MARKED ON (B1) WITH INDELIBLE FELT TIP PEN (BLK)
2	USING TAPE (B2) TAPE BACK ALL UNUSED WIRES TO CABLE (B)
3	USING TAPE (B2) WRAP AS REQ TO PROVIDE STRAIN RELIEF

CABLE LENGTH

	TYPE	B	D	NOTES
(*)	-A	25 FT		

CABLE FUNCTION	
FROM A	EXTENDER FOR
TO C	ILC CABLES
TO E	

COMPUTER SYSTEMS DIVISION
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DRAWN	DRF	10/4/77
CHECKED		
APPROVED		

TITLE: CABLE ASSEMBLY DETAILS

CUSTOMER/NO.	DWG NO.	REV
HSMIMP	XILC-10	A

REVISION			
APP'D	SYM	DESCR	DATE
	A	REL PROD	2.1.79

CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES	CONNECTOR A PIN NO.	WIRE COLOR B	CONNECTOR C PIN NO.	If used WIRE COLOR D	If used CONNECTOR E PIN NO.	NOTES
1	TAN/BRN	1			TRANSDAT −						
2		2			TRANSDAT +						
3	TAN/RED	3			TRANSLOOP +						
4		4			TRANSLOOP −						
5	TAN/ORN	5			TRANSCLK +						
9		9			TRANSCLK −						
7	TAN/YEL	7			RECCLK +						
8		8			RECCLK −						
10	TAN/GRN	10			RECDATA +						
11		11			RECDATA −						
12	TAN/BLU	12			TP11 = GND						
6		6			TP12 = GND						

COMPUTER SYSTEMS DIVISION BOLT, BERANEK & NEWMAN INC. CAMBRIDGE, MASS 02138				
DRAWN	DRF	10/79	TITLE	CABLE RUN-LIST
CHECKED				
APPROVED		7/1/11	CUSTOMER/NO. HSMIMP	DWG NO. XILC-11 REV A

CABLES