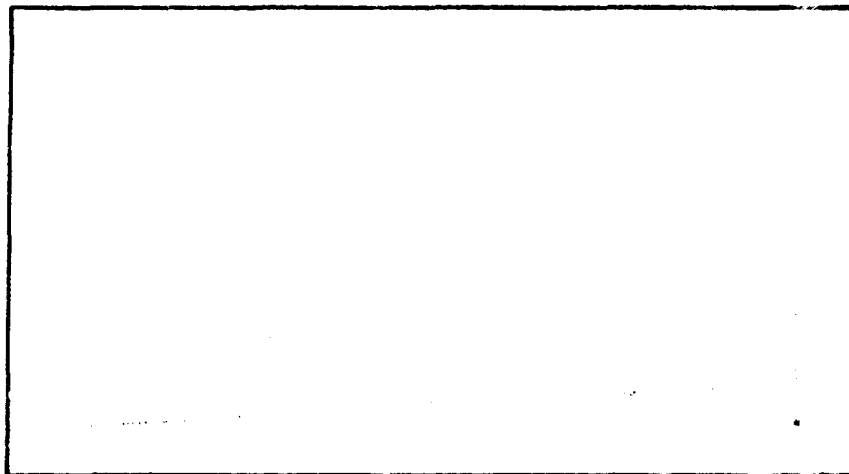


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11. ABSTRACT

The D-17B computer is a digital minicomputer that is used in the NSQ-10 Minuteman I missile guidance system. This system has been made available for reutilization by qualifying agencies. Documentation concerning the procedures for converting the computer for general purpose use is being generated by the Minuteman Computer Users' Group. This report is addressed toward part of that effort.

Before the conversion process is begun the computer may be tested to determine useability. An inexpensive forced-air cooling system will allow operation at ambient air temperatures up to 50°. Preliminary descriptions of the D-17B previously available are supplemented in this report by a description using the states of control flip-flops. This state description is useful as a study plan and a maintenance aide. Suggestions of educational applications and a data input bus are included. This thesis can provide the information necessary to convert the D-17B to a laboratory computer and it contains data for those interested in similar conversion projects.

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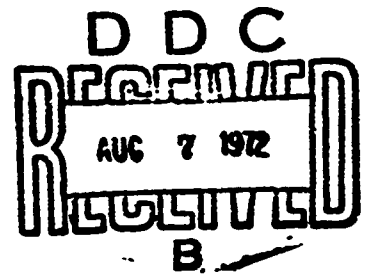
LABORATORY CONVERSION AND
STATE DESCRIPTION OF THE
D-17B COMPUTER

Thesis

GE/EL/72S-2

Douglas J. Allen

Captain USAF



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Minuteman I Computer D-17B Computer Computer Conversion Computer Description Computer Cooling						
1c						

LABORATORY CONVERSION AND
STATE DESCRIPTION OF
THE D-17B COMPUTER

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

by

Douglas J. Allen, B.S.E.E.

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Graduate Electrical Engineering

June 1972

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Preface

I have always admired those people who could ingeniously find a new use for obsolete equipment. When I was given the opportunity to be part of the effort to reuse a computer, I was delighted. This report is the result of my efforts toward the goal of providing documentation about the D-17B computer and the procedure needed to change it from a missile control computer to a laboratory computer.

I would like to thank Dr. Gary B. Lamont and Dr. Frank M. Brown for their tireless efforts in advising the Minuteman computer project. Also, I wish to express my gratitude to Mr. Robert L. Mitchell and to Mr. Dale Wells, systems engineers at Newark Air Force Station, for their technical assistance and for data that they so willingly provided. My sincere appreciation is due Mr. Robert G. Durham for technical help and the AFIT workshop for their excellent craftsmanship.

A special thank you is due my wife and family for their patience, encouragement and assistance in preparing this report.

Douglas J. Allen

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Abstract

The D-17B computer is a digital minicomputer that is used in the NSQ-10 Minuteman I missile guidance system. This system has been made available for reutilization by qualifying agencies. Documentation concerning the procedures to convert the computer for general purpose use is being generated by the Minuteman Computer Users' Group. This report is addressed toward part of that effort.

Before the conversion process is begun the computer may be tested to determine useability. An inexpensive forced-air cooling system will allow operation at ambient air temperatures up to 85°F. Fragmentary descriptions of the D-17B previously available are supplemented in this report by a description using the states of control flip-flops. This state description is useful as a study plan and a maintenance guide. Suggestions of educational applications and a data input bus are included. This thesis can provide the information necessary to convert the D-17B to a laboratory computer and it contains data for those interested in similar conversion projects.

I. Introduction

This thesis was undertaken to investigate the conversion of the Minuteman I guidance computer to a general purpose laboratory computer and to provide a state description of the computer. In order to discuss this problem in more detail, it is necessary to consider the background of this problem and some general definitions of computer classes.

Background

The modernization of the Minuteman Intercontinental Ballistic Missile Force has made it necessary for the United States Air Force to declare over 1,000 outdated inertial guidance systems unserviceable. Each of these model NS-10Q guidance systems contains a D-17B computer, power supplies, and the unclassified parts of the stable platform.

These systems are available, for only the shipping costs, to colleges and other qualifying organizations. Unfortunately, written procedures for reutilizing the system were nonexistent and only fragmentary descriptions of the machine were available. Thus, this effort met an early impasse because of the lack of documentation concerning the D-17B.

The Minuteman Computer Users' Group (MCUG) was formed by Dr. Charles Beck at Tulane University for the purpose of consolidating the efforts of potential users of the D-17B. It is intended that the members of this cooperative may share the results of their research and overcome the initial reutilization problems (Ref 7:ii). The Air Force Institute of Technology (AFIT) is a member of the MCUG and it is hoped that this report will be used as part of that effort.

AFIT obtained two NS-10Q Minuteman I guidance systems in June 1971. Since that time, four thesis projects have been undertaken as part of an overall plan to convert a D-17B computer from one of these NS-10Q systems into a useful laboratory computer. One of these projects (Ref 8) developed a control console for the computer. Another project (Ref 13) developed an input/output interface, and a third effort (Ref 9) produced a software simulation for the D-17B. The fourth thesis project is the subject of this report and its purpose and plan of development will be explained in the following paragraph.

Definitions and Problem Analysis

In order to accurately describe the unmodified D-17B computer and the planned modifications, it is necessary to define a general-purpose and special-purpose computer. A general-purpose computer is a computer designed to solve a wide variety of problems. In contrast, a special-purpose computer is designed to solve a specific problem or a restricted class of problems (Ref 4:202). The D-17B computer can be considered to be equally worthy of either title. It was constructed along the

lines of a general-purpose computer, but when used as part of the Minuteman System it functions as a special-purpose machine.

Essentially then, the problem involves changing a special-purpose computer to a general-purpose computer. The extent and type of modifications depend upon the following assumptions.

Assumptions Computers similar to the D-17B are commercially available for less than \$10,000. It can be assumed that future users of the D-17B will require minimal conversion expenditures; otherwise, it would be advantageous to purchase a new machine. It is also necessary to assume that the computer and associated power supplies would be used in their present physical package, which is a right circular cylinder, 29 inches in diameter and 20 inches high. These dimensions could be reduced by repackaging the computer, but the cost of such a modification would be prohibitive.

It is assumed that the modified computer will be operated in a laboratory where the temperature of the room can be controlled within the range of 65-85°F. This assumption provides a standard for designing a new cooling system for the computer.

Subproblems Since the computer was cooled in its original configuration by special equipment associated with the Minuteman Missile, a new cooling system must be designed. This design will be under strict economic limitations and should be as simple as possible.

In order to operate the D-17B computer, the user must know how the machine functions. A major subproblem of this thesis will be to describe the computer in several ways so that each user may choose a description that best suits his application.

A third subproblem will be to develop procedures that will allow future users to determine the operational status of their particular D-17B. These procedures are desirable since they give the user the assurance of knowing that the computer will operate, prior to beginning the conversion process.

Presentation of Problem Solutions

Chapter II of this report presents five different types of descriptions of the D-17B: A physical description, a functional description, a description of the word format, state descriptions and mode description. Chapter III discusses the initial preparation, checkout, and a cooling system for the computer, and is written for the technician who is faced with installing the D-17B in the laboratory. Chapter IV briefly discusses some applications of the D-17B, and Chapter V presents conclusions and recommendations for future investigation.

II. Descriptions of D-17B Computer

In this portion of the report the D-17B computer will be described from five basic points of view. These descriptions range from a general overview to a specific analysis. First, a basic physical description will be presented; second, the computer will be described in terms of five functional sections; third, the word format and information necessary for programming will be briefly discussed; fourth, register transfer will be described using state diagram techniques; and, finally, some alternate descriptive techniques will be covered. General specifications of the computer are listed in Table I.

Physical Description

Size and Composition. The D-17B computer occupies one-half of a right polygonal-cylindrical shell. This twelve-sided cylinder is 20 inches high, has a maximum radius of 29 inches and the shell is 6 inches in depth. A power-supply for the complete NS-10Q guidance system is contained in the remainder of the shell. A stable platform, the third major item of the NS-10Q, occupies the cavity formed by the computer and power supplies.

The computer alone weighs 62 pounds and is composed of 76 printed circuits and a rotating disk memory (Ref 11:16).

Power Requirements. If the associated power supply is used with the D-17B, it is necessary to provide 28 VDC, 19-25 amps from an external source. The computer may be operated without the accompanying power supply; however, it is necessary to supply fourteen separate DC voltages as well as 1200 and 400 hz alternating current supplies. These secondary power specifications are listed in Table II. Power consumption for the computer alone is approximately 350 watts (Ref 11:16).

Functional Description

The D-17B may be divided into five basic functional parts: the Control Unit, Arithmetic Unit, Memory, Input, and Output. This division is shown in Figure 1 (Ref 11:TR24).

Basic Components and Terminology of the D-17B. Each functional section of the D-17B is composed of basic components or building blocks that are common to several parts of the computer. These components must be described and common terminology must be defined in order to adequately describe the functional parts of the computer.

The term bit will be used as a shortened form of binary digit. Thus, a bit of information may be stored in a two-state device such as a flip-flop. An extension of this notion leads to an ordered set of binary cells, such as flip-flops, and this ordered set is called a register (Ref 4:15).

TABLE I

General Specifications of D-17B Computer

TYPE	Serial, synchronous
NUMBER SYSTEM	Binary, fixed point, sign plus 2's complement
LOGIC LEVELS	False-0 volts: True -10 volts (Negative logic)
DATA WORD LENGTH	24 bits 11 bits - (split word)
INSTRUCTION WORD LENGTH	24 bits
NUMBER OF INSTRUCTIONS	39
EXECUTION TIME	Varies with each instruction type Add 78.125 micro sec multiply 1015.625 micro sec.
CLOCK FREQUENCY	345.6 khz
ADDRESSING	Direct Addressing Two-address and 3-address instructions
MEMORY	Ferrous-oxide-coated disk 2,727 word (24 bits) capacity 78.125 micro sec. cycle time
INPUT/ OUTPUT	48 Digital lines (output) 28 Digital lines (input) 12 Analog lines 3 pulse lines

Information adapted from Ref 2:23

TABLE II

D-17E Computer DC Power Supplies, Voltages, and Tolerances

Voltage Volts	Tolerance	Ripple MV P-P	Current MA	Location Plug	Pin
-35	4%	10.0	100 \pm 20%	J2(31) ^a	23
-25	2%	10.0	428 \pm 20%	J2(31)	14
-10	2%	10.0	3410 \pm 20%	J2(31)	20
-5	0.25%	10.0	160 \pm 20%	J2(50)	9
-5	2%	10.0	1380 \pm 20%	J2(31)	24
-3	2%	10.0	520 \pm 20%	J2(31)	18
-2.5	0.25%	5.0		P301	9,11
-1.0	2%	10.0	500 \pm 10%	J2(31)	13
+2	2%	10.0	1855 \pm 20%	J7	25
+2.5	0.25%	5.0		P301	20,22
+5	0.25%	10.0	75 \pm 20%	J2(50)	20
+6	2%	10.0	185 \pm 10%	J2(50)	22
+10	2%	10.0	1060 \pm 20% -10%	J2(50)	16
+15	2%	10.0	1600 \pm 20%	J2(50)	9
+25	2%	10.0	650 \pm 20%	J2(50)	17
+35	2%	10.0	870 \pm 20%	J2(50)	19

a. Number in parenthesis indicates the number of pins in the plug.

Adapted from Ref 3:99, 16:3-7, 7:6.

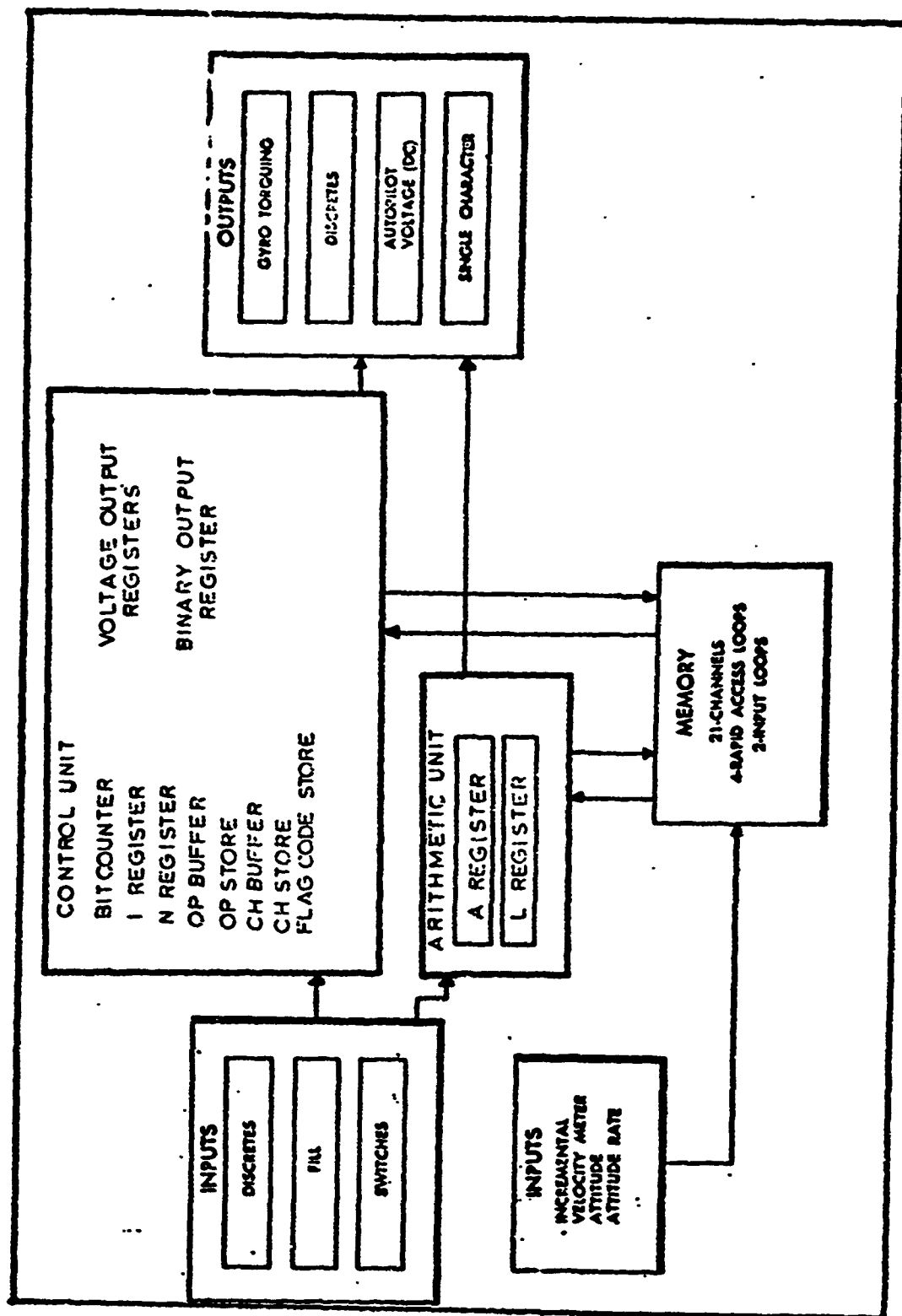


Fig. 1. Functional Block Diagram of Minuteman Computer (From Ref 11: TR24).

The term word is used for a group of digits that represent a basic unit of information to the computer (Ref 6:3). A word, then, is the information that may be stored in a register. In the D-17B, the information carrying part of a word is 24 bits in length with three additional bits used for timing as shown in Fig. 2.

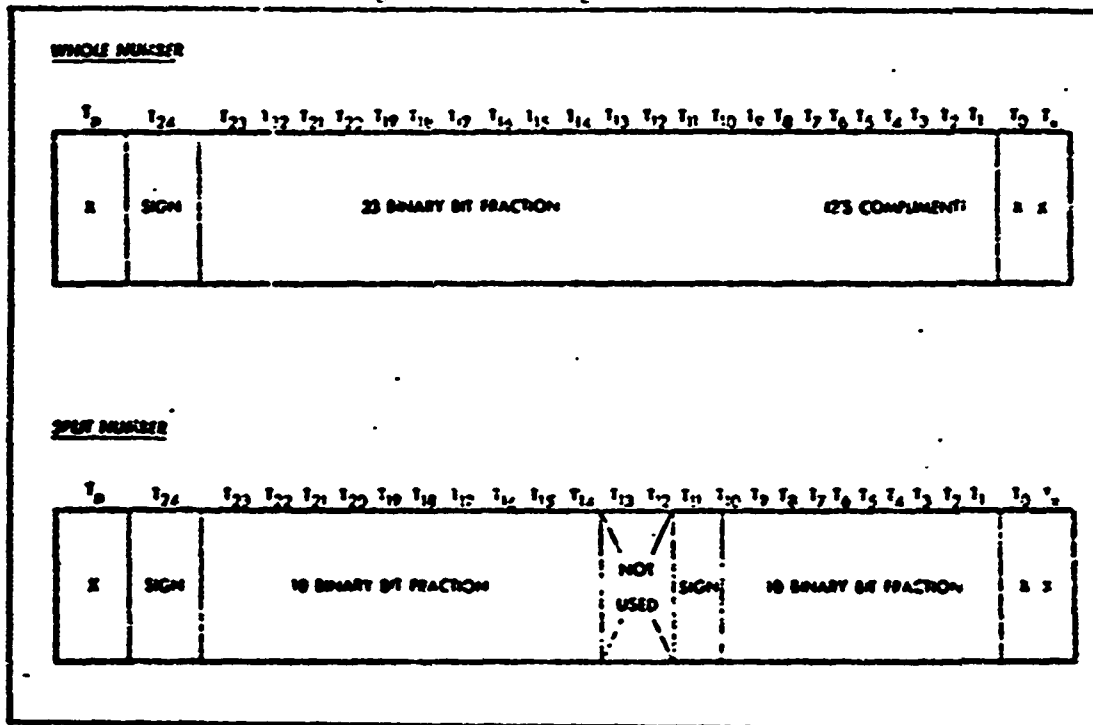


Fig. 2. D-17B Word Formats (From Ref 2:16).

A word may be divided into two parts to represent two different numbers. In the D-17B computer this process is called split-word operation. During split-word operation the term right half-word applies to bits 0 through bit 11 and left half-word applies to bits 14 through 24, as shown in Fig. 2.

A loop is a register composed of flip-flops and bits that are stored on the magnetic disk memory. As the memory disk turns, the information is read into a read flip-flop and written back onto the memory disk by a write flip-flop, as depicted in Fig. 3.

Since loops are special serial registers, both terms loop and register will be used to refer to loops in the description of this computer.

The term word-time is derived from the length of time required to circulate an entire word in a one-word loop. A word time may be further divided into "bit times" since a bit is one-twenty-seventh of a word.

The bits in a word may be coded to form an instruction for the computer. Different parts of the word may be decoded to indicate specific information such as the "address" or memory location to the next instruction. A part of the instruction which is allocated for such a special purpose is called

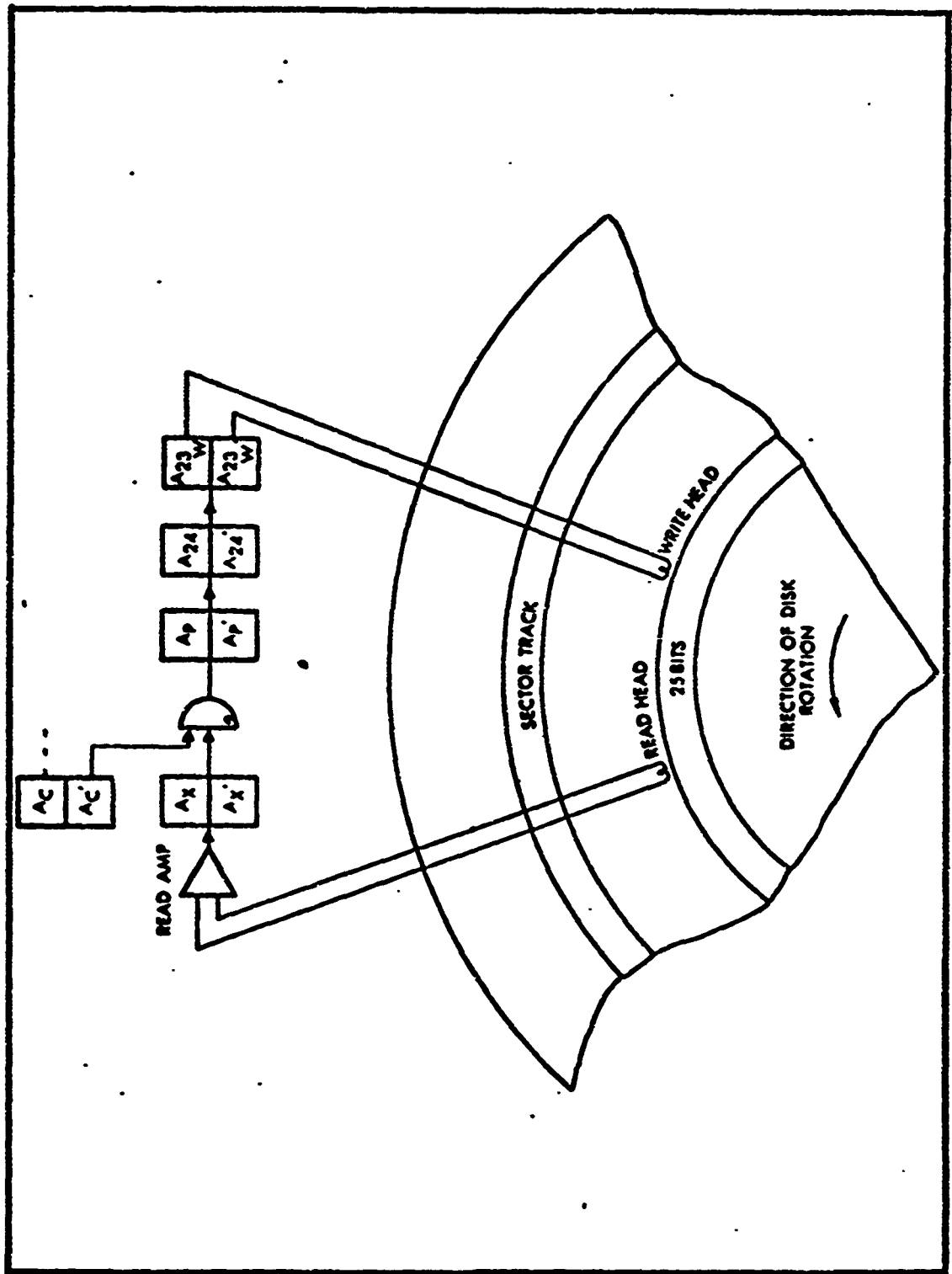


Fig 3 Typical D-17 B Recirculating Register (From Ref 2:14)

a field. Fields are also commonly used to indicate what operation is to be performed (Op Code) or what addresses of numbers are to be used in the operation (operand). This leads to a method of classifying instruction words - by the number of addresses in the instruction (Ref 10:452).

Control Unit. The primary function of the Control Unit is to interpret machine instructions and direct the execution of these instructions. Therefore, the Instruction Register (I) is one of the major components in the Control Unit (Ref 11:16).

The I-loop or Instruction Register is composed of one delay flip-flop, I_p , and a read and a write flip-flop, I_x and I_{24} respectively. Twenty-four other bits of this one word register are written on the disk memory. New information may be entered into the I loop when the control flip-flop I_c is "one" set; otherwise, the information circulates from the magnetic disk through the I flip-flop and is re-written on the disk in a continuous loop.

The I register receives the computer instruction from the memory and holds that instruction for part of the instruction interpretation. Prior to execution, the instruction is read into various buffer registers and the I register is free to receive the next instruction to be executed (Ref 11:16).

The Operation Buffer Register is used to store the instruction operation code prior to execution (see State Description c2). This register consists of flip-flops $I_p, O_{b3}, O_{b2}, O_{b1}$. During the last word time of execution, the next instruction is serially loaded into the Operation Buffer Register, then parallel-loaded into the Operation Code Storage Register. Flip-flops, O_4, O_3, O_2, O_1 , form the Operation Code Storage Register which serves primarily to hold the op code during execution (see Word Format for an explanation of the Op Code) (Ref 11:27).

Storage of the operand information is accomplished in a similar manner by the Channel Buffer Register and the Channel Storage Register. During the Instruction Read operation, the operand channel information is fed into the Channel Buffer Register, flip flops C_{b5} through C_{b1} . When the operand sector is found (see memory for discussing sectors), the operand channel is parallel-loaded into the Channel Storage Register, flip-flops C_5 through C_1 . This register then holds the operand channel information during execution of the instruction. Some operations do not require an operand and the Channel Storage flip-flops may be used as additional hardware to execute the instruction. An example of this application is the Character Output operation: four bits of the Accumulator are shifted into the Channel Storage Register to be output to the character output lines (Ref 2:TR-72).

Flag Storing is a special operation, and it is explained in the word format description. In this operation the previous contents of the Accumulator are stored in a channel specified by the instruction. A code for that channel number is loaded into the Flag Code Buffer Register, S_{b3}, S_{b2}, S_{b1} , when the instruction is read. At the first bit time of execution the Flag Code Buffer Register is

parallel-loaded into the Flag Code Storage Register (Ref 11:TR45). A set of diagrams showing the codes that may be loaded into these registers is displayed in Fig. 4.

When an operand is read from memory it is loaded into a register of the Control Unit called the Number Register. The Number Register or N-loop consists of three flip-flops, N_p , N_{24} , N_x , and twenty-four bits of memory. The three flip-flops N_p , N_{24} , and N_x are used for delay, writing on the memory disk, and reading, respectively, and a fourth flip-flop, N_c , controls the entry of new information into the N-loop (Ref 11:31).

There are four Output Control registers which are a part of the control unit. The composition of these registers will be discussed here, but their functional task will be discussed in the Output functional description. The Discrete Output Register is contained in the Control Unit. It consists of five flip-flops, D_5 through D_1 , which, together with a Discrete Output Matrix, control the twenty-eight Discrete Outputs. Digital-to-analog conversion control flip-flops form three registers of eight flip-flops each. The registers are designated V_{1i} , V_{2i} , and V_{3i} , $i = 1, \dots, 8$. The Binary Output Control Register consists of three flip-flops: G_3 , G_2 , G_1 .

Timing control of the D-17B is achieved using a bit counter that is controlled by the sector track of memory (see "Memory" for a discussion of the sector track). The bit counter is a set of flip-flops that are used to distinguish bit times of the serial operations of the computer. These flip-flops are designated B_1 , B_2 , B_3 , B_4 , B_5 , B_6 . T_p , T_x , T_o , T_p , T_x , and T_o are timing flip-flops that are "one" set only at the beginning and ending of words (the use of these flip-flops is apparent in the Word Format discussion). B_1 is used to distinguish between odd and even bit times and B_2 is "one" set and "zero" set at alternating two-word time periods. B_3 is "one" set only during the right and left split-word bit times. B_4 and B_5 are counting flip-flops that support the other flip-flops of the bit counter. B_6 is "zero" set during the first half of the word time and "one" set during the second half (Ref 11:25). The relationship between the B_1 flip-flop and the word times is shown in Fig. 5.

These are the major components of the Control Unit. Interaction of this function and the following functional units will be discussed in the State Description of the D-17B.

Arithmetic Unit. As its name implies, the purpose of the Arithmetic Unit is to perform the calculations as directed by the Control Unit. Each of these Arithmetic operations is explained in the State Description. This unit consists of two one-word registers, the Accumulator and the Lower Accumulator. (Ref 11:17)

The Accumulator holds the results of all arithmetic functions and is an output register for the voltage, binary, and character output operations (Ref 11:17). In addition to 23 bits on the magnetic disk, it is composed of two delay flip-flops, A_p and A_{24} , a write flip-flop, A_{23} , and A_x , a read flip-flop.

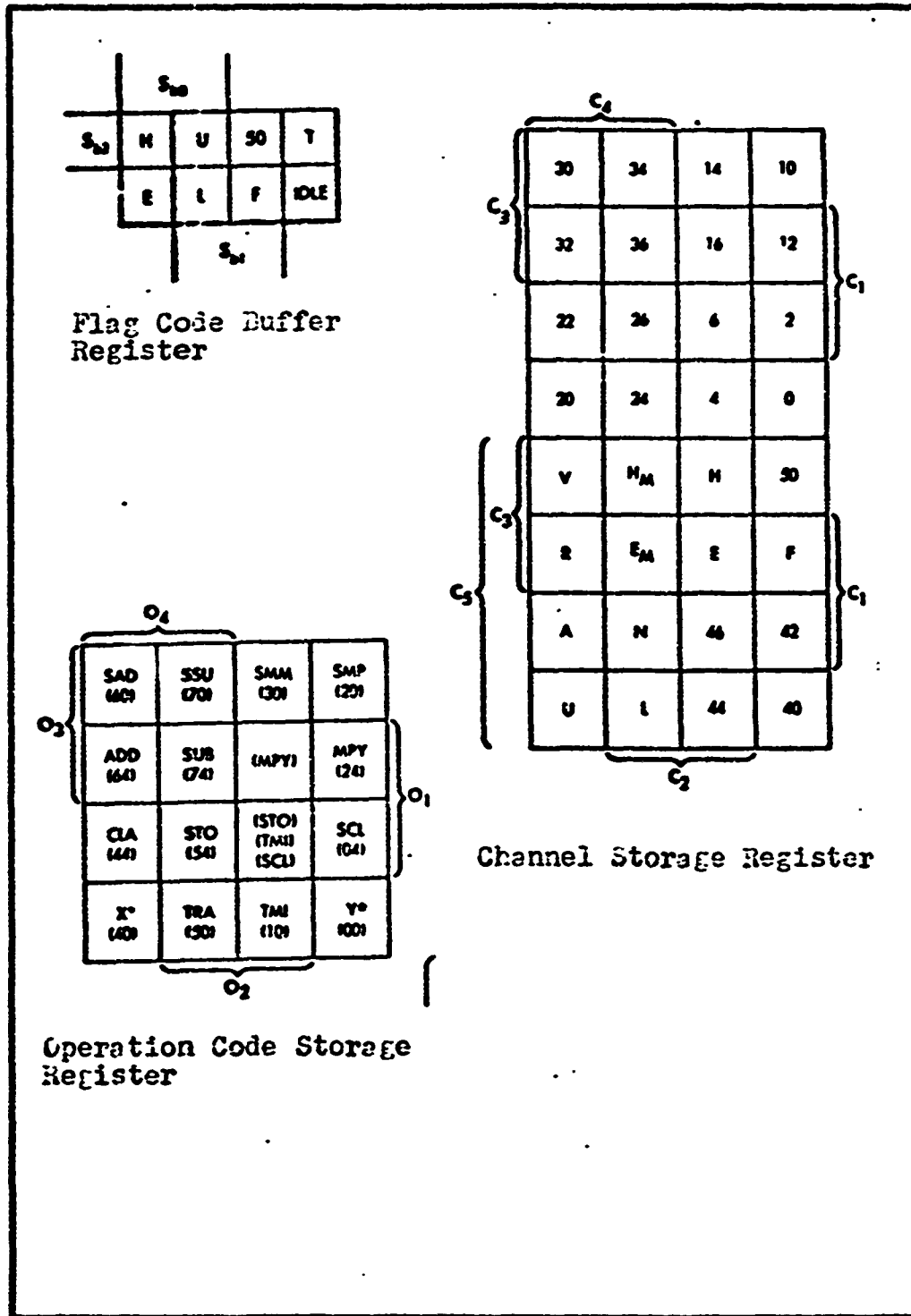


Fig. 4. Veitch Diagram for Storage Register Codes (From Ref 2:42, 43, 45).

When the control flip-flop, A_c is "zero" set, the A loop is allowed to circulate and new information may be serially loaded into the Accumulator when A_c is "one" set (Ref 11:30).

The Lower Accumulator, L-loop, is used for rapid access storage, character inputs, and logical operations. It consists of two delay flip-flops, L_x and L_p , one write flip-flop, L_{24} , a read flip-flop, L_0 , and twenty-three bits on the magnetic disk (Ref 11:31).

Memory. Memory in the D-17B is a rotating magnetic disk. Information is transferred to the magnetic disk by stationary read and write heads. This information remains on the disk until new data is recorded. Therefore, this information is in non-volatile storage; that is, the information remains stored even when power is removed from the computer. However, the loops may be considered as volatile storage, because the flip-flops that are part of the loop will be activated in a random state when power is returned to the computer (Ref 11:17).

In order to define specific locations in memory, the disk is divided into 128 radial divisions (sectors) and 21 concentric tracks (channels) as shown in Fig. 6. The sectors are numbered octally from 00 to 177 and channels are numbered in an even octal progression, 00,02, ..., 50. (Channels are numbered evenly because the least significant digit of the octal number used for channel addressing is part of the sector address). The sector numbers are recorded on the memory in a special sector track, S; however, these sectors are numbered one sector out of phase for timing purposes in the computer. Each channel and sector number designate 27 bits (one word) of memory. Twenty of the channels are called "cold storage channels" because the write heads on these channels may be deactivated (Ref 11:17).

In addition to the part of memory defined by the sector and channel divisions there are ten recirculating loops, which are used in input, arithmetic, and rapid storage operations. The A, L, N, and I loops function as part of the Arithmetic and Control Units. Rapid access storage is provided by the U-loop, which is a one-word register consisting of a read flip-flop, U_p , and a write flip-flop, U_x , and twenty-five bits stored on the memory disk.

The F loop, a four-word rapid access storage register, is comprised of F_p , a write flip-flop, F_x , a read flip-flop, and 106 bits on the memory disk. Two other four-word loops, V and R, are used as input loops. The V loop contains a V_p and V_x flip-flop and the R loop uses a R_p and R_x flip-flop for write and read functions respectively.

Rapid access storage of eight words is provided by the E loop which is composed of a read flip-flop, E_x , a write flip-flop, E_p , and 214 bits on the rotating disk. A read amplifier, E_{mx} , is provided at the midpoint of this register to allow rapid access to the E loop contents. The H loop is a 16-word

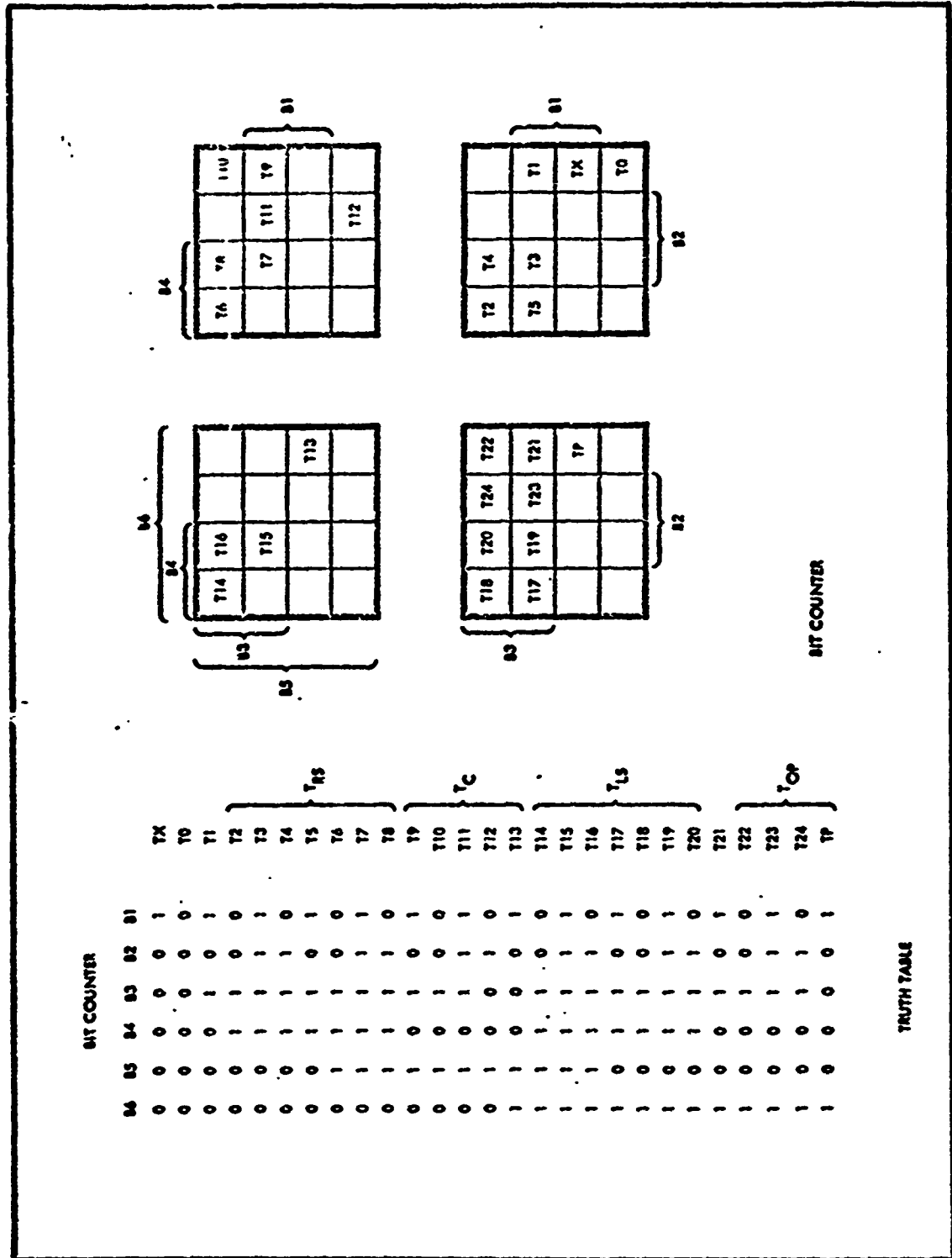


Fig. 5 D-17B Bit Counter (From 11:TR22)

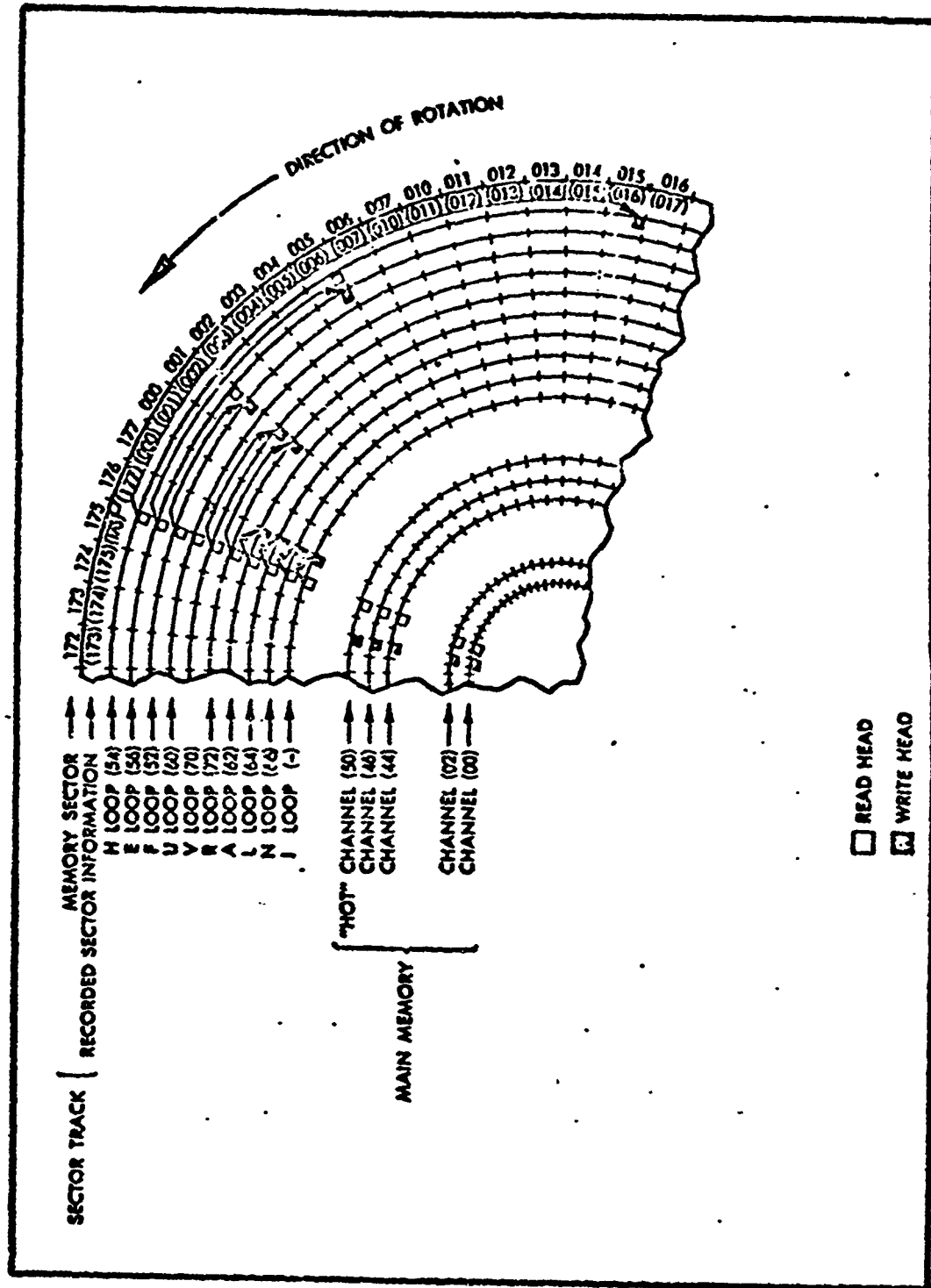


Fig. 6 D-17B Memory Layout (From Ref 2:11)

rapid access storage register. Like the other loops, the H_p and H_x flip-flops are used for writing and reading from the memory disk. An intermediate read amplifier, H_{mx} , is provided at the midpoint of this register to allow rapid access reading (Ref 11:34).

Inputs. In this report, inputs to the D-17B will be discussed in two general classes: control input signals, and data inputs. Control input signals are those signals which would be generated by a control panel or input device to cause the computer to enter a particular state or to accept data. Data inputs are defined as character input signals and discrete input signals. Both classes of inputs, associated common symbols, and plug connections are listed in Table III. In the following discussion of both control and data inputs, voltage ranges and general specifications are given; however, these ranges have not been completely tested on the computer at AFIT. It is known from experiments that these ranges are conservative and that successful operation has been achieved outside the listed ranges. These input voltage levels are adjusted by input circuits in the computer to obtain the level required for machine operation. The adjusted signal is signified by adding a (*) to the standard symbol, thus an adjusted fill signal would be F_{sc}^* .

Discrete Disable, D_{dc} , is a control input signal which deactivates the discrete output signals. The "true" or "1" level is +10v with a worst-case current of 2.2 amps. Typical load is 135 milliamps. False level is -25v with 4.0 microamp load (Ref 1:69).

The control signal Enable Write, E_{wc} , controls the write flip-flops in the memory "cold storage" channels (00-46). "True" for E_{wc} is +35 to +39v into a 120 ohm resistance connected to -30v into a 1 meg ohm impedance (Ref 1:68).

Initiate load or Fill signal, F_{sc} , allows the computer to leave the Manual Halt states and enter the Wait state. "True" or "1" for this signal is -16 to -30v into a 8.2k ohms resistance connected to +25v. The "false" level is +6 to +30v into a resistance of 1 meg ohm.

The Mechanical Reader Input Signal, I_m , is not used in the control console at AFIT. It may be used as one of several commands to enter the Wait state (see State Description). I_m has the same specification as the Fill signal.

The Halt prime or Run, K'_{hc} , input signal allows the computer to enter the compute states. "True" for this signal is -16 to -30v into a 4.1 k ohm resistance connected to 25v and the "false" level is +6 to +30v into 1 meg ohms (Ref 1:63).

K'_k and K'_{kr} are both used as symbols for the halt or run prime signal. It is used to cause the computer to enter the non-compute states. Signal specifications are the same as K'_{hc} (Ref 1:63).

Single-step Prime Input is used to cause the computer to execute only one instruction. Two symbols appear in the literature for this signal, K'_{sc} and K'_{sk} . "False" level is +2 to +30v and "true" is -3 to -30v (Ref 1:67).

TABLE III
D-17B Computer Input Locations

Input Name	Input Symbol	Plug and Pin Number
Disable Discrete	D _{dc}	J1(100) ^a -23
Enable Write	E _{wc}	J1(100) -93
Initiate Load or Fill Signal	F _{sc}	J8-24
Gyro Bottom	I _{bc}	J10-22
Mechanical Input	I _{mc}	J8-17
Character Inputs	I _{1c} I _{2c} I _{3c} I _{4c} I _{5c}	J7-1 J7-2 J7-3 J7-4 J7-5
Halt Prime	K _{hc}	J7-17
Run Prime	K _{kr}	J8-16
Master Reset	M _{rc}	J1(100) -90
Sprocket Timing	T _c	J8-38
Sprocket Timing Prime	T _c	J7-6
Discrete Inputs	X1C X2C X3C X4C X5C X6C X7C X8C X9C X10C X11C X12C X13C X14C X15C X16C X17C X18C X19C	J1(100) -96 J1(100) -97 J1(100) -98 J1(100) -99 J9-7 J10-25 J9-2 J9-3 J9-4 J9-5 J10-19 J3(100) -63 J10-20 J3(100) -48 J3(100) -18 J3(100) -65 J3(100) -66 J10-21 J9-10

TABLE III (cont)

Input Name	Input Symbol	Plug and Pin Number
Discrete Inputs (cont)	Y1C	J10 -1
	Y2C	J10 -2
	Y3C	J10 -3
	Y4C	J10 -4
	Y5C	J1(100) -95
	Y6C	J1(100) -94
	Y7C	J3(100) -76
	Y8C	J9-11
	Y9C	J9-12
	Y10C	J9-13
	Y11C	J9-14
	Y12C	J9-15
	Y13C	J9-16
	Y14C	J9-17
	Y15C	J9-44
	Y16C	J9-45
	Y17C	J9-46
	Y18C	J9-9
	Y19C	J3(100) -29
	Y20C	J3(100) -28
	Y21C	J3(100) -17
	Y22C	J3(100) -16
	Y23C	J3(100) -6
	Y24C	J3(100) -5

a. Number in parenthesis indicates total number of pins in plug. Information obtained from Ref 5: Fig. 3 and through experiments with D-17B computer.

Master Reset, M_{rc} , is used to set the control flip-flop to a specified set of settings. Signal specifications are similar to the Fill signal specifications.

The Sprocket Timing input signal, T_c , is an input which causes the computer to accept data from the character input lines. "True" level is -3 to -30v and "false" is +20 to +30v. The inverse signal is T'_c , however, T'_c has the same signal specifications; true is -3 to -30v and false is +20 to +30v.

Input signals listed in the above paragraphs are control inputs. Next, the data inputs will be specified. Character input lines, I_{1c} to I_{5c} provide input codes for both command and numeric data. These codes are listed in Table IV. Signal specifications for the Character Inputs are the same as the Fill signal (Ref 1:42).

Discrete inputs $X_{1c} - X_{19c}$ and $Y_{1c} - Y_{24}$ are two sets of on-off type signals which may be loaded directly into the Accumulator under program control. A special discrete signal input I_{bc} is available and may be reset under program control. In the original configuration, this signal was used to indicate a gyro malfunction. Signal level requirements for these signals are the same as the Fill signal (Ref 2:46).

Outputs. Four types of output signals will be considered under this functional heading: single character, binary, analog voltage, discrete outputs. Voltage limits and load limits are listed with each of the outputs; however, these limits were extracted from Ref 1:40-59 and were not tested as part of this report. Pin connections for these outputs are listed in Table V and Table VI.

Single characters may be output on output lines S_{c1} through S_{c4} . Under program control the four most significant bits of the Accumulator may be shifted to the lines for a period up to 31 word-times as dictated by the program instruction. During the above period a timing signal is supplied on output line S_{ct} and even parity is indicated on line S_{c5} . "True" level for the signals is -23.7v through a 1 k ohm resistor and maximum load is 50 milliamps. "False" level is +10.8v through 2 k ohm resistance for loads up to 1.4 milliamps and +25v through a 12 k ohm resistance for loads above 1.4 milliamps. Maximum current from the circuit should be 4 milliamps.

Binary Incremental Outputs were used in controlling the navigational gyros. These outputs are changed by the Binary Output instructions which cause one of three flip-flops to be set according to the sign of the Accumulator. When the BOA instruction is executed, the G_1 flip-flop is "one" set if the Accumulator is negative and "zero" set if the Accumulator is positive. Output line G_{11} is "true" if G_1 is "one" set and line G_{10} is "true" if G_1 is "zero" set. Similarly, the BOB instruction controls outputs G_{20} and G_{21} and the BOC instruction controls the G_{30} and G_{31} output lines. "True" for these outputs is -10v through a 470 ohm resistance requiring load currents less than 15 milliamps.

TABLE IV

Character Input Codes for D-17B

Input	Line Codes					T _c
	I ₁	I ₂	I ₃	I ₄	I ₅	
Number 0	0	0	0	0	1	1
1	1	0	0	0	0	1
2	0	1	0	0	0	1
3	1	1	0	0	1	1
4	0	0	1	0	0	1
5	1	0	1	0	1	1
6	0	1	1	0	1	1
7	1	1	1	0	0	1
Command Halt	0	0	0	1	0	1
Location	1	0	0	1	1	1
Fill	0	1	0	1	1	1
Verify	1	1	0	1	0	1
Compute	0	0	1	1	1	1
Enter	1	0	1	1	0	1
Clear	0	1	1	1	0	1
Delete	1	1	1	1	1	1

(Information from Ref 2:37)

TABLE V

D-17B Computer Output Pin Connections

Output	Symbols	Pin Connections
Character Outputs	SC ₁₀	J6-19
	SC ₂₀	J6-20
	SC ₃₀	J6-21
	SC ₄₀	J6-22
	SC ₅₀	J6-23
	SC ₆₀	J6-24
Binary Incremental Outputs	G ₁₀	J10-12
	G ₁₁	J10-13
	G ₂₀	J10-14
	G ₂₁	J10-15
	G ₃₀	J10-16
	G ₃₁	J10-17
Discrete Outputs	D01	J10-5
	D02	J10-6
	D03	J10-7
	D04	J10-8
	D08	J3(100) -8A.
	D09	J3(100) -9
	D10	J10-31
	D11	J3(100) -64
	D12	J6-3
	D13	J3(100) -89
	D14	J6-5
	D15	J10-30
	D16	J3(100) -100
	D17	J10-29
	D18	J9-25
	D19	J9-26
	D20	J9-23
	D21	J10-32
	D22	J9-28
	D23	J9-29
	D24	J3(100) -74
	D25	J9-30
	D26	J9-31
	D27	J9-32
	D28	J9-33
	D29	J9-34
	D30	J9-35
	D31	J9-36

A-Number in parenthesis indicates total number of pins in plug. Information obtained from Ref 5: Fig 3 and through experimentation with D-17B computer.

TABLE VI

D-17B Computer Digital-to-Analog Voltage Output Locations

Phase Register Settings	Voltage Output Symbol	Associated Output Instruction	Pin Connection
$P_3 P_2 P_1$	No Voltage Output		
$P_3 P_2 P_1$	VO_{10}	VOA	J10-9
	VO_{20}	VOB	J10-10
	VO_{30}	VOC	J10-11
$P_3 P_2 P_1$ or $P_3 P_2 P_1$	VO_{11}	VOA	J3(100) ^a -21
	VO_{21}	VOB	J3(100) - 10
	VO_{31}	VOC	J3(100) -19
$P_3 P_2 P_1$ or $P_3 P_2 P_1$	VO_{12}	VOA	J3(100) -46
	VO_{22}	VOB	J3(100) -59
	VO_{32}	VOC	J3(100) -52
$P_3 P_2 P_1$ or $P_3 P_2 P_1$	VO_{13}	VOA	J3(100) -7
	VO_{23}	VOB	J3(100) -98
	VO_{33}	VOC	J3(100) -87

a. Number in parenthesis indicates the total number of pins in the plug. Information obtained from Ref 11:TR70.

"False" voltage level is -1.0v through 470 ohms with load currents less than 30 milliamps.

Three separate digital to analog converters are available in the computer output networks. Voltage values are proportional to the split word contents of the Accumulator. The VOA instruction causes the most significant bits of the split word in A to be transferred to the Voltage Output Register number 1. Flip-flops in this register direct plus and minus 5v to eight different points in a resistor network to produce an output voltage between $\pm 20v$. If bit 1_4 is a "1", the right half of the Accumulator will be used for output, otherwise the left half-word will be used to specify the voltage flip-flop settings. Similarly, the VOB and VOC instructions control output register V_{2i} and V_{3i} ($i=1, \dots, 8$). The three voltage outputs may be directed to any one of four sets of output terminals depending on the Phase Register Contents. The setting P_3, P_2, P_1 inhibits all voltage outputs; other Phase Register settings and pin locations are shown in Table VI. Symbols for the outputs are VO_{ij} where i is either 1, 2, or 3 corresponding to the VOA, VOB, and VOC instructions respectively. The second subscript, j , refers to one of the four Phase Register settings (Ref 11:TR70). All of the outputs vary between 20v at a maximum load of 4 milliamps.

Twenty-eight discrete output lines are available and may be turned on and off under program control. Discrete line DO_4 is the only line that may be "on" while another discrete output is on. If DO_4 is on and $DO_1, DO_2,$ or $DO_3,$ is turned, it will remain on. In all other cases, if any discrete output is "on" and another discrete line is activated by program control, the first discrete line will be turned "off" (Ref 9:TR8). The on or "true" voltage level for these outputs is -23.7v through a 1 k ohm resistor with a maximum load of 30 milliamps. "False" is indicated by +10.8v into a 2 k ohm resistance for loads up to 1.4 milliamps and +25v for loads greater than 1.4 milliamps; however, the load must be less than 4 milliamps.

Computer Word Formats

In this description the word formats of the D-17B will be examined; however, no effort will be made to explain the details necessary for programming. This task has to be accomplished in the Minuteman Computer Users' Group Report MCUG-4-71 (Ref 6).

All words in the D-17B consist of 27 bits, although three bits are used for timing. The remaining 24 bits may be presented in three basically different formats: whole number, split number, and instruction. These formats are shown in Fig. 7, for reference in the following discussions.

Whole Number Format. (Ref 3:24,25) All 24 bits of one word may be used to store one number in the whole number format. The number is in 2's complement form and the twenty-fourth bit position is the sign bit. Bits $T_p, T_q,$ and T_x are the timing bits.

Split Number Format. (Ref 3:24,25) Similarly, two numbers may be stored in one word

of twenty-four bits. Bits T_{24} through T_{14} form the left half-word and Bits T_{11} through T_1 form the right half-word. T_{24} and T_{11} are the respective half-word sign bits and bit positions T_{13} and T_{12} are not used.

Instruction Format. (Ref 3:26-28) Instructions take on two basic forms in the D-17B depending upon the contents of bit position T_{20} . This bit position is the "Flag bit" and is a signal or flag to indicate that the instruction is a flag-store instruction. A flag-store instruction will cause the computer to store the contents of the Accumulator in the loop indicated by a code in T_{19} , T_{18} , and T_{17} bit positions of the instruction. First it is necessary to describe the unflagged instruction in order to consider the flagged instruction in more detail.

An unflagged instruction contains five fields: the op code, flag (always 0), next instruction sector, operand channel, and operand sector. This format is commonly called both a one and one-half address and a two address instruction. Either name would seem to be correct since two address are actually present; however, only one-half of one address is explicitly shown. These fields are shown in Fig. 7 and will be given specific symbols in the following sections.

The flagged instruction may be considered a three address instruction since three addresses are actually present. The six programmable fields of the format are: op code, flag (always 1), flag storage location, sector of next instruction, operand channel, and operand sector. One should note that since the address of the next instruction is shortened to four bits in this format, the instruction must be within 16 sectors of this instruction on the memory disk.

State Description of the D-17B

Operation of the D-17B may be described by considering the various configurations that the control flip-flops enter when the machine is executing a program. Thus, a state of the machine is defined by a particular configuration of the control flip-flops. States may be represented on a diagram which depicts the various paths that the machine may cycle through during program execution. This state diagram may be used in conjunction with a description of the information exchange between registers to completely describe the machine operation. The procedure used to formulate this description was essentially to reverse the process of computer design as described by Chu (Ref 10). Any number of different state descriptions may result, depending upon the set of two state elements (flip-flops) that are chosen as control elements of the machine. The control elements used in this particular description were picked by trial and error using the following criteria:

- 1) The states of the machine should be closely parallel to the existing descriptions of the computer.

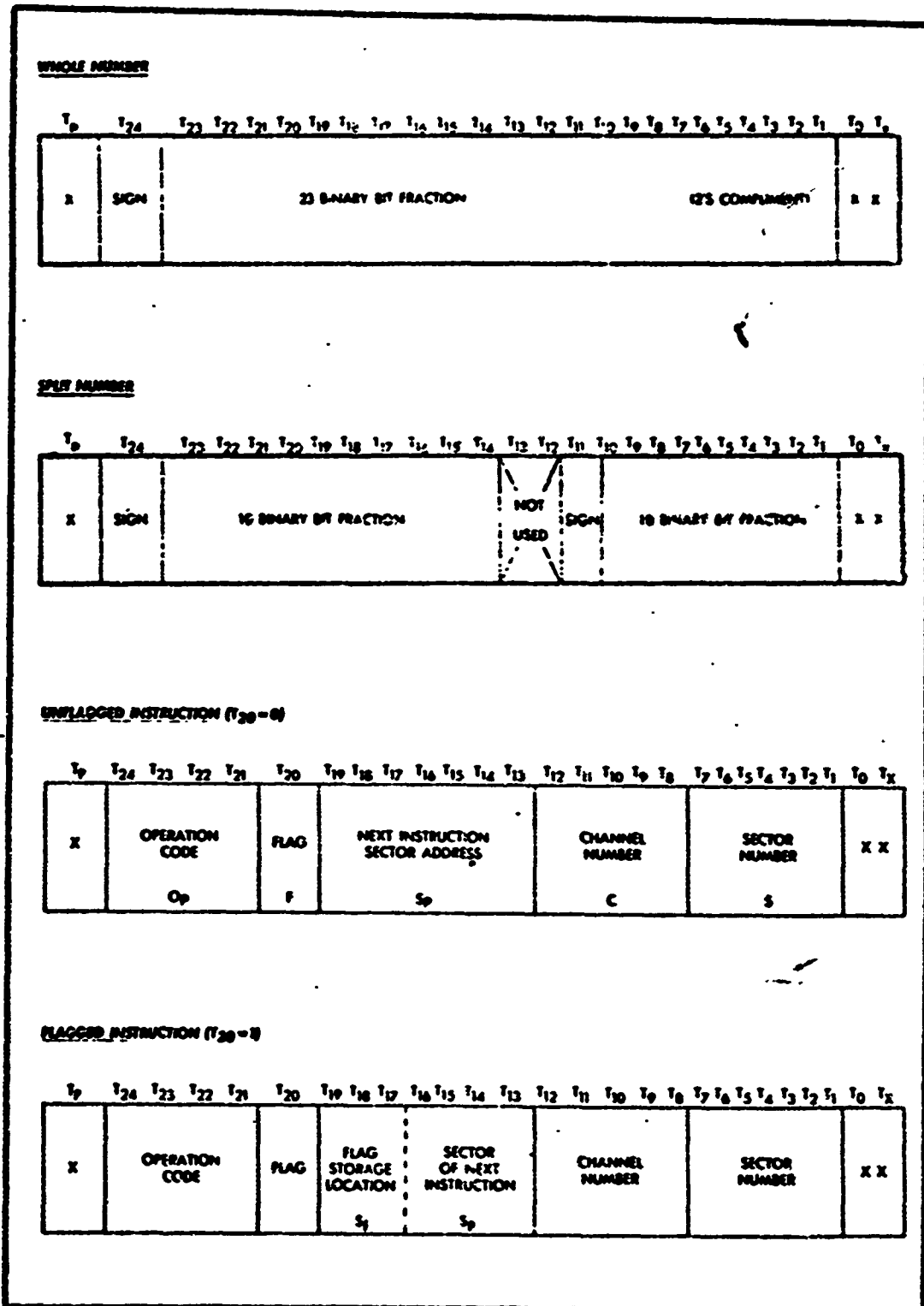


Fig. 7 D-17B Computer Word Format (From Ref 2:16,17)

- 2) The overall state description should be as simple as possible, yet there should be a sufficient number of states to describe all the machine operations.

State Descriptions have the advantage of being a visual description, hence, they are easily understood and are capable of displaying large amounts of information in a concise form. Even more important, the state diagram provides a systematic approach for describing how the computer functions.

Register Transfer Notation. In order to conveniently describe information transfer between registers during each state it is necessary to adopt a type of shorthand convention to condense the description. The symbols used in this notation are listed in Table VI and are an adaptation of the system used by Chu (Ref 10:378).

State Diagram. In this report the states of the computer have been broken into two major classes or modes, Compute (K) and Non-Compute (K'). This division was selected to allow the reader to easily correlate the state description with descriptions already published. The states in these classes are represented by nodes (circles) and are numbered with an identifying number. Configurations of the major control flip-flops which cause transition between states are listed beside the transition path on the diagram. Associated with each state diagram is a table which lists the states by number and name and the information transfer which occurs during that state. The Non-Compute states are displayed in Figs. 8 and 9 and Table VIII lists the associated register transfer notation. Compute states are shown in Fig. 10, 11, 12, and Table IX lists the register transfer notation. Table X is a list of boolean equations associated with the register transfer statements in Tables VIII and IX.

Assumption. For the purpose of this description, it is assumed that there is a control panel associated with the computer which supplies the input signals listed in Table V (Ref 8 and Ref 13). These inputs are changed to the voltage level required for use inside the computer. After this voltage transformation is completed, the signal is renamed and given a * designation. The "starred" signals are in a direct logical relationship with their generating signal: for example, when T_c is a logical "1," T_c^* is also a logical "1".

Non Compute States. (Ref 11:56 and 15:1.1-2.15)

Power on Random State. When power is applied to the D-17B, the controlling flip-flops will become activated in a random state. Depressing the "MASTER RESET" switch causes the computer to enter a Prepare to Operate state where initialization is begun (See Fig. 8).

Prepare to Operate (n1). In this state the phase register is initialized to an idle mode. F_c is turned off to prevent the computer from entering a special state called fine countdown. The Discrete output control register is initialized to prevent random discrete outputs and various other flip-flop are

TABLE VII

Register Transfer Notation Used in the State Description of the D-17B Computer

Symbol	Description of Symbol
()	Parentheses denote contents of a register.
[]	Square brackets denote a portion of a register.
o[]	A lower case o indicates the operand address part of the instruction.
c[]	A lower case c indicates the channel of the operand address.
s[]	A lower case s indicates the sector portion of the operand address.
op[]	Lower case op indicates operation code portion of an instruction.
f[]	Lower case f indicates the flag field of an instruction.
sp[]	Lower case sp indicates next instruction sector portion of an instruction.
sf[]	Lower case sf indicates the flag storage location of a flag store instruction.
l[]	Lower case l designates the left half-word of a register.
r[]	Lower case r designates the right half-word of a register.
M(P) M(c,s)	These symbols indicate a word location of memory designated by P or by channel c and sector s.
(M(c,s))	This symbol designates the contents of the above memory word location.
⇒	Double arrow indicates the transfer of one register (or part of a register) to another register.
+	This symbol means arithmetic addition.
-	This symbol means arithmetic subtraction.
x	This symbol means the multiplication operation.
:	A colon following a Boolean statement indicates that when the Boolean statement is true the subsequent operations occur.
→	A single arrow denotes the sequence of operations from one state to another.
₁ D ₂	This symbol indicates that the two state device (flip-flop) D ₂ is "one" set. "Zero" setting is expressed with a preceding zero subscript.

TABLE VII (cont)

Definition of Symbol

This symbol indicates the exclusive or operation.

This symbol indicates the logical and operation.

Symbol

+

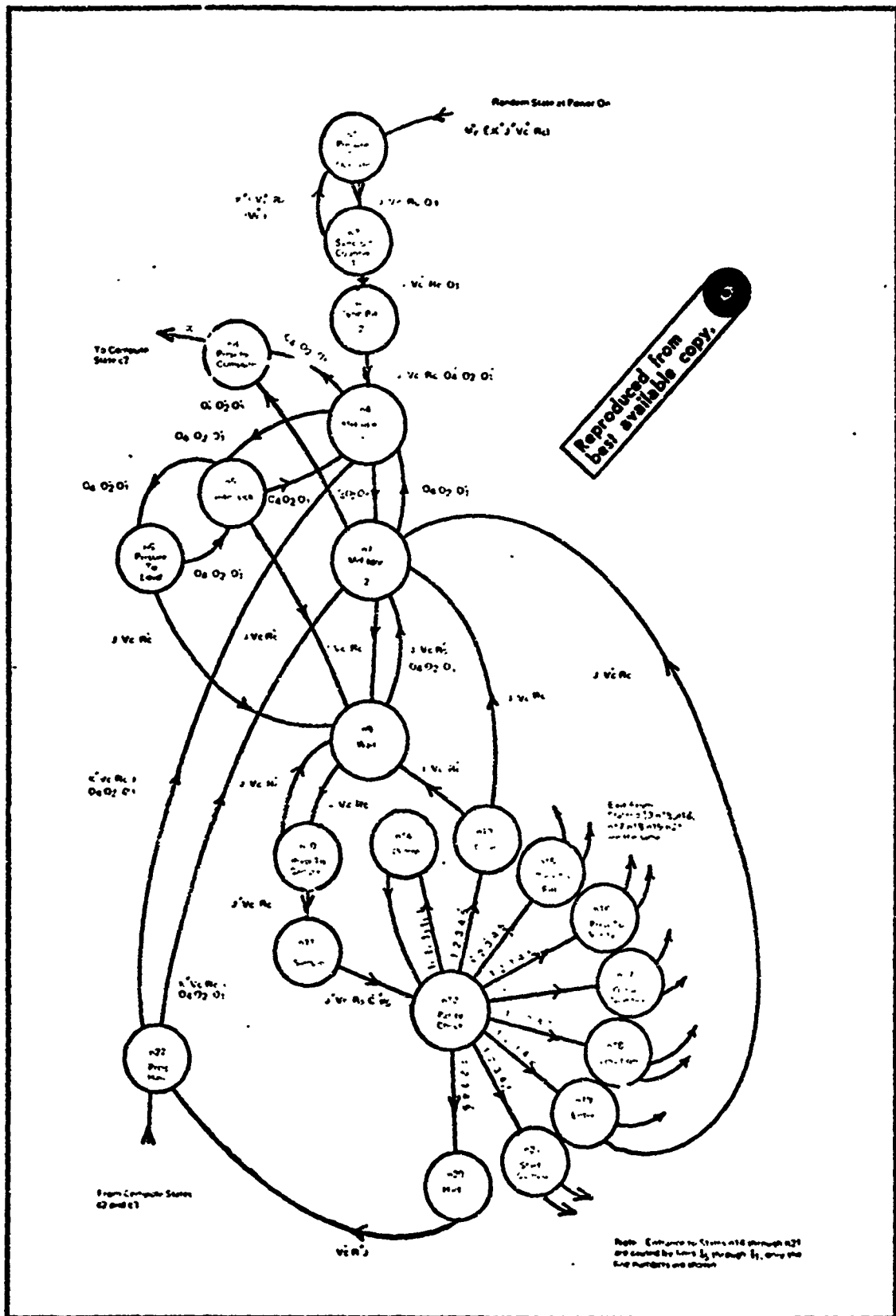


Fig.8 D-17B Noncompute States

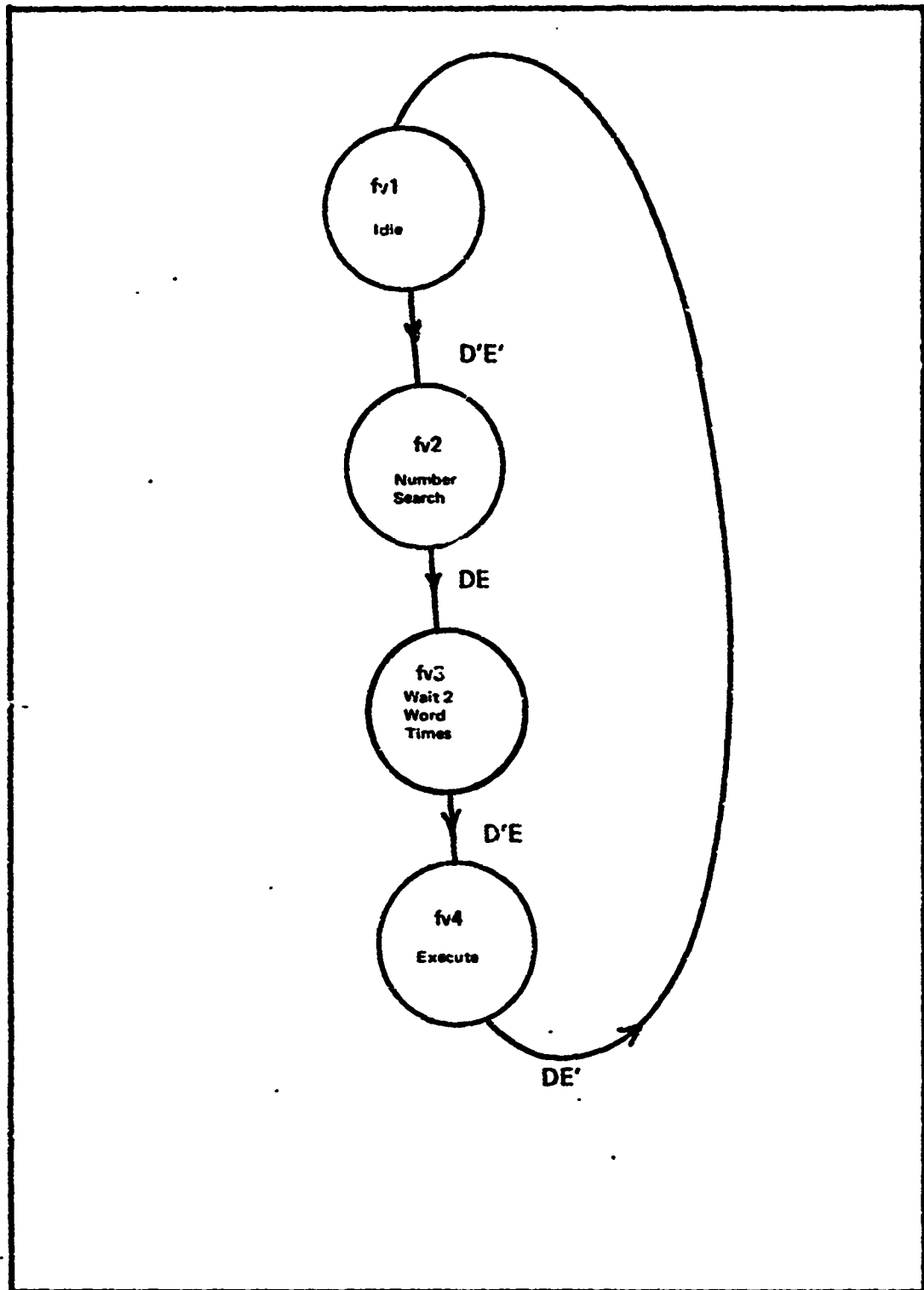


Fig. 9 Non compute Fill-Verify States

TABLE VIII

Register Transfer Equations of the Non Compute States of the D-17B Computer.

Note : This table may be used with Table X, the number in parenthesis to the right of the register transfer equation designates the associated equation in Table X.

State	State Name:	Information Transfer	
	Random State Master Reset M_r	$M_r : 0 \Rightarrow K, J, V_c$ $1 \Rightarrow R_c$	
n1	Prepare to Operate	$0 \Rightarrow P, F_c, D_i, Q, S_{b2}, E,$ O_4, O_1 $1 \Rightarrow S_{b3}, D, O_2$ $n1 T_p : 1 \Rightarrow J$ $n1 \rightarrow n2$	
n2	Sync Bit Counter 1	$n2 \ 1O_1 : 1 \Rightarrow O_1$ $n2 \rightarrow n3$	(1)
n3	Sync Bit Counter 2	$n3 \ 0O_1 : 0 \Rightarrow O_1$ $n3 \ 0R_c : 0 \Rightarrow R_c$ $0 \Rightarrow I_i \quad i = 1, 2, \dots, 21, 21$ $1 \Rightarrow I_{22}, I_{24}$ $n3 \rightarrow n4$	(2) (3)
n4	Manual Halt Idle 1	$n4 \ 1O_4 : 1 \Rightarrow O_4$ $n4 \rightarrow n5$ $n4 \ 1O_1 : 1 \Rightarrow O_1$ $n4 \rightarrow n7$ $n4 \ 0O_2 : 1 \Rightarrow O_2$ $n4 \rightarrow n8$	(4) (1) (5)
n5	Manual Halt Interlock	$n5 \ 0O_4 : 0 \Rightarrow O_4$ $n5 \rightarrow n4$ $n5 \ 0O_1 : 0 \Rightarrow O_1$ $n5 \rightarrow n7$ $n5 \ 0O_2 : 0 \Rightarrow O_2$ $n5 \rightarrow n8$ $n5 \ 1V_c : 1 \Rightarrow V_c$ $n5 \rightarrow n9$	(6)(7) (1) (8) (9)
n6	Manual Halt Prepare to Load	$n6 \ 1O_2 : 1 \Rightarrow O_2$ $n6 \rightarrow n5$ $n6 \ 1V_c : 1 \Rightarrow V_c$ $n6 \rightarrow n9$	(10) (11)
n7	Manual Halt Idle 2	$n7 \ 0O_1 : 1 \Rightarrow O_1$ $n7 \rightarrow n4$	(2)

TABLE VIII (CONT)

State	State Name	Information Transfer	
		$n7 \text{ }_1S_{b2} : 1 \Rightarrow S_{b2}$	(12)
		$n7 \text{ }_0O_2 : 0 \Rightarrow O_2$ $n7 \rightarrow n8$	(5)
		$n7 \text{ }_1V_c : 1 \Rightarrow V_c$ $n7 \rightarrow n9$	(13)
n8	Manual Hal: Prepare to Compute	$n8 \text{ } T_x : 0 \Rightarrow J$	(14)
		$n8 \text{ }_1D : 1 \Rightarrow D$	(15)
		$n8 \text{ }_1K : 1 \Rightarrow K$ $n8 \rightarrow c2$	
n9	Wait	$n9 \text{ }_1R_c : 1 \Rightarrow R_c$ $n9 \rightarrow n10$	(16)
		$n9 \text{ }_0V_c : 0 \Rightarrow V_c$ $n9 \rightarrow n8$	(17)
n10	Prepare to Sample	$n10 \text{ }_0R_c : 0 \Rightarrow R_c$ $n10 \rightarrow n9$	(18)
		$n10 \text{ }_0J : 0 \Rightarrow J$ $n10 \rightarrow n11$	(19)
n11	Sample	$n11 \text{ }_0S_{b3} : 0 \Rightarrow S_{b3}$	(20)
		$I_i^* \Rightarrow C_{pi} \quad i = 1, \dots, 4$	
		$I_3^* \Rightarrow S_{b3}$	
		$n11 \text{ }_0R_c : 0 \Rightarrow R_c$ $n11 \rightarrow n12$	(18)
n12	Parity Check	$n12 \text{ } C_{p1} : S_{b3}^* \Rightarrow S_{b3}$	
		$n12 \text{ } T_{20} : 1 \Rightarrow O_4$	
		$n12 \text{ } O_4 : C_{pi} \Rightarrow C_{pi-1} \quad i = 2,3,4$ $C_{pi} = C_{p4}$	
		$n12 \text{ } T_{24} : 0 \Rightarrow O_4$	
		$n12 \text{ }_1C_{p5} : 1 \Rightarrow C_{p5}$ $n12 \rightarrow n13$	(21)
n13	Process Code Clear	$n13 \text{ }_1L_c : 1 \Rightarrow L_c$ $0 \Rightarrow L_i \quad i = 1, \dots, 24$	(22)
		$n13 \text{ }_0L_c : 0 \Rightarrow L_c$	(23)
		$n13 \text{ }_1J : 1 \Rightarrow J$ $n13 \rightarrow n9$	(24)
		$n13 \text{ }_1O_2 : 1 \Rightarrow O_2$	(25)
		$n13 \text{ }_0V_c : 0 \Rightarrow V_c$ $n13 \rightarrow n7$	(26)
n14	Delete	No Action	

TABLE VI(KCONT)

State	State Name	Information Transfer	
n15	Prepare to Fill	$n15 \quad {}_0O_3 : 0 \Rightarrow O_3$	(27)
		$n15 \quad {}_1J : 1 \Rightarrow J$	(24)
		$n15 \rightarrow n9$	
n15		$n15 \quad {}_1O_2 : 1 \Rightarrow O_2$	(25)
		$n15 \quad {}_0V_c : 0 \Rightarrow V_c$	(26)
		$n15 \rightarrow n7$	
n16	Prepare to Verify	$n16 \quad {}_1O_3 : 1 \Rightarrow O_3$	(52)
		$n16 \quad {}_1J : 1 \Rightarrow J$	(24)
		$n16 \rightarrow n19$	
		$n16 \quad {}_1O_2 : 1 \Rightarrow O_2$	(25)
n16		$n16 \quad {}_0V_c : 0 \Rightarrow V_c$	(26)
		$n16 \rightarrow n7$	
		$n17 \quad {}_1L_c : 1 \Rightarrow L_c$	(22)
		$n17 \quad {}_1O_4 : 1 \Rightarrow O_4$	(28)
n17	Octal Numbers	$C_{pi} \Rightarrow L_p$	
		$L_p \Rightarrow L_{24}$	
		$L_o \Rightarrow L_x$	
		$L_x \Rightarrow C_{p3}$	
		$C_{pi} \Rightarrow C_{pi-1} \quad i = 2,3$	
		$n17 \quad {}_0L_c : 0 \Rightarrow L_c$	(23)
		$n17 \quad {}_1J : 1 \Rightarrow J$	(24)
		$n17 \rightarrow n9$	
		$n17 \quad {}_1O_2 : 1 \Rightarrow O_2$	(25)
		$n17 \quad {}_0V_c : 0 \Rightarrow V_c$	(26)
n17		$n17 \rightarrow n7$	
		$n18 \quad {}_1L_c : 1 \Rightarrow L_c$	(53)
		$(L) \Rightarrow 1$	
n18	Location	$n18 \quad T_p : 0 \Rightarrow L_c$	
		$n18 \quad {}_1J : 1 \Rightarrow J$	(24)
		$n18 \rightarrow n19$	
n18		$n18 \quad {}_1O_2 \quad {}_0V_c : 1 \Rightarrow O_2 \quad 0 \Rightarrow V_c$	(25)(26)
		$n18 \rightarrow n7$	
n19 fv1	Enter Fill-Verify Idle	$n19 \quad {}_1A_c : 1 \Rightarrow A_c$	(34)
		$(L) \Rightarrow A$	
		$n19 \quad {}_1J : 1 \Rightarrow J$	(24)
		$n19 \rightarrow n9$	
n19		$n19 \quad {}_1O_2 \quad {}_0V_c : 1 \Rightarrow O_2 \quad 0 \Rightarrow V_c$	(25)(26)
		$n19 \rightarrow n7$	
fv1		$fv1 \quad {}_0D : 0 \Rightarrow D$	(35)
		$fv1 \rightarrow fv2$	
fv2	Fill-Verify Search	$fv2 \quad {}_1O_{b3} : S + l_i \Rightarrow O_{b3}$	(36)
		$i = 2, \dots, 7$	

TABLE VIII(CONT)

State	State Name	Information Transfer	
		$(I_i) \Rightarrow C_{bi-7}$	$i = 8, \dots, 12$
		$fv2 \quad {}_1D \quad {}_1E : 1 \Rightarrow D \quad 1 \Rightarrow E$	$fv2 \rightarrow fv3$
fv3	Fill-Verify Wait 2 Word times	$(C_b) \Rightarrow C$ $(M \langle C \rangle) \Rightarrow N$ $fv3 \quad {}_oD : O \Rightarrow D$	(39) $fv3 \rightarrow fv4$
fv4	Fill-Verify Execute	$fv4 \quad {}_1I_p : 1 \Rightarrow I_p$	(41)
		$(s [1] + 1) \Rightarrow s [1]$	(40)
		$fv4 \quad {}_oI_p : O \Rightarrow I_p$	(Fill only)
		$(A) \Rightarrow M \langle o [1] \rangle$	(42)(43)
		$fv4 \quad {}_oE \quad {}_1D : O \Rightarrow E, 1 \Rightarrow D$	$fv4 \quad fv1$
		$fv4 \quad {}_1S_{b2} : 1 \Rightarrow S_{b2}$	(44)
		$O \Rightarrow V_c$ $n19 \rightarrow n10$	
n20	Halt	$n20 \quad {}_oV_c : O \Rightarrow V_c$	(29) $n20 \rightarrow n21$
n21	Start Compute	$n21 \quad {}_1O_2 \quad {}_oV_c : 1 \Rightarrow O_2, O \Rightarrow V_c$	(25)(30) $n21 \rightarrow n4 \rightarrow$
n22	Program Halt	$n22 \quad {}_1D \quad {}_oE : 1 \Rightarrow D, O \Rightarrow E$	(14)(31) $fv4 \rightarrow fv1$
		$n22 \quad {}_1O_2 \quad {}_oO_4 \quad {}_1J : 1 \Rightarrow O_2$	(25)
		$O \Rightarrow O_4$	(32)
		$1 \Rightarrow J$	(33)
		$n22 \rightarrow n7 \text{ or } n4$	

Information used to construct this table was taken from Ref 7: 55-67 and Ref 14: 1.1 - 2.15.

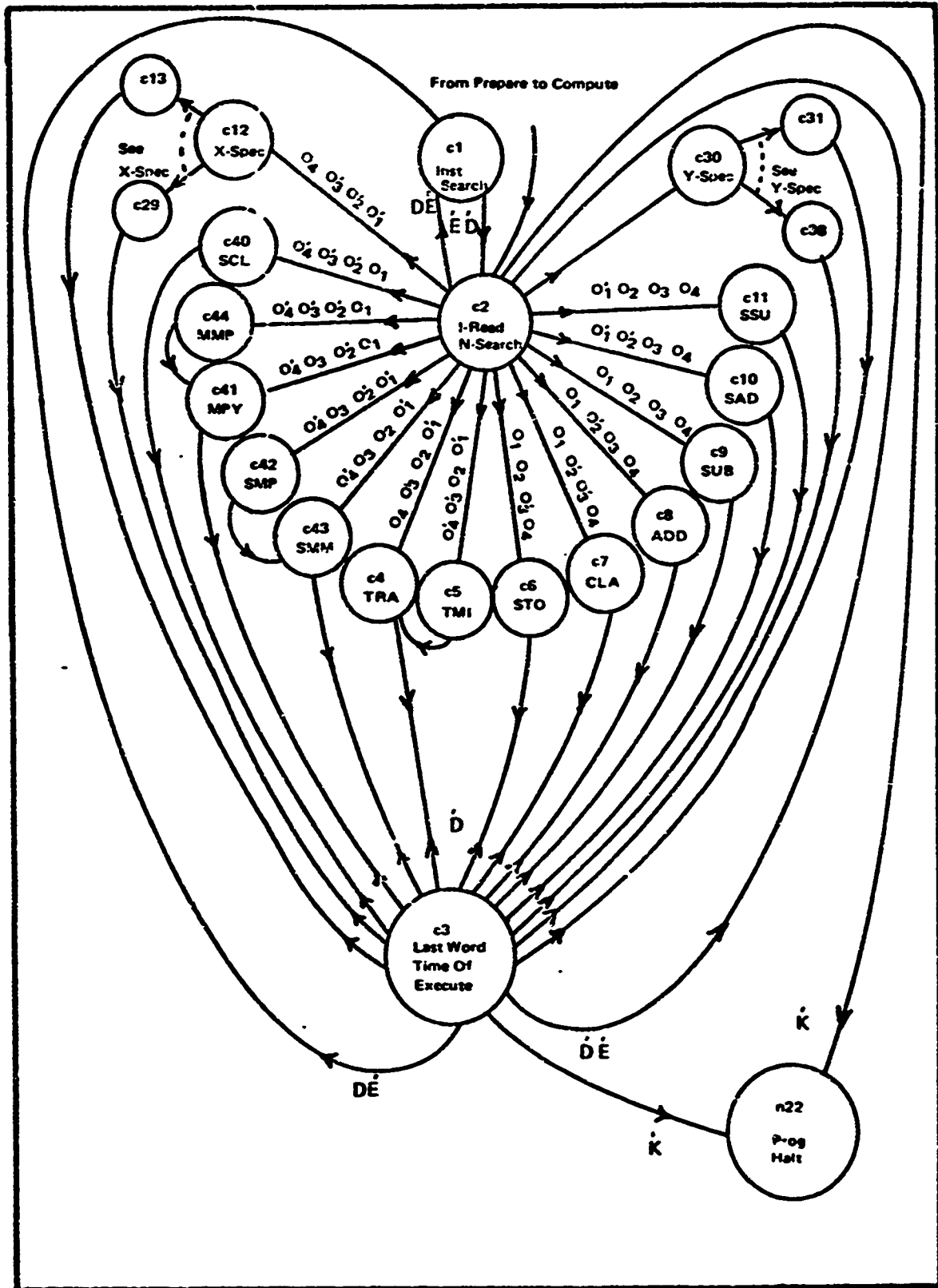


Fig. 100-178 Compute States

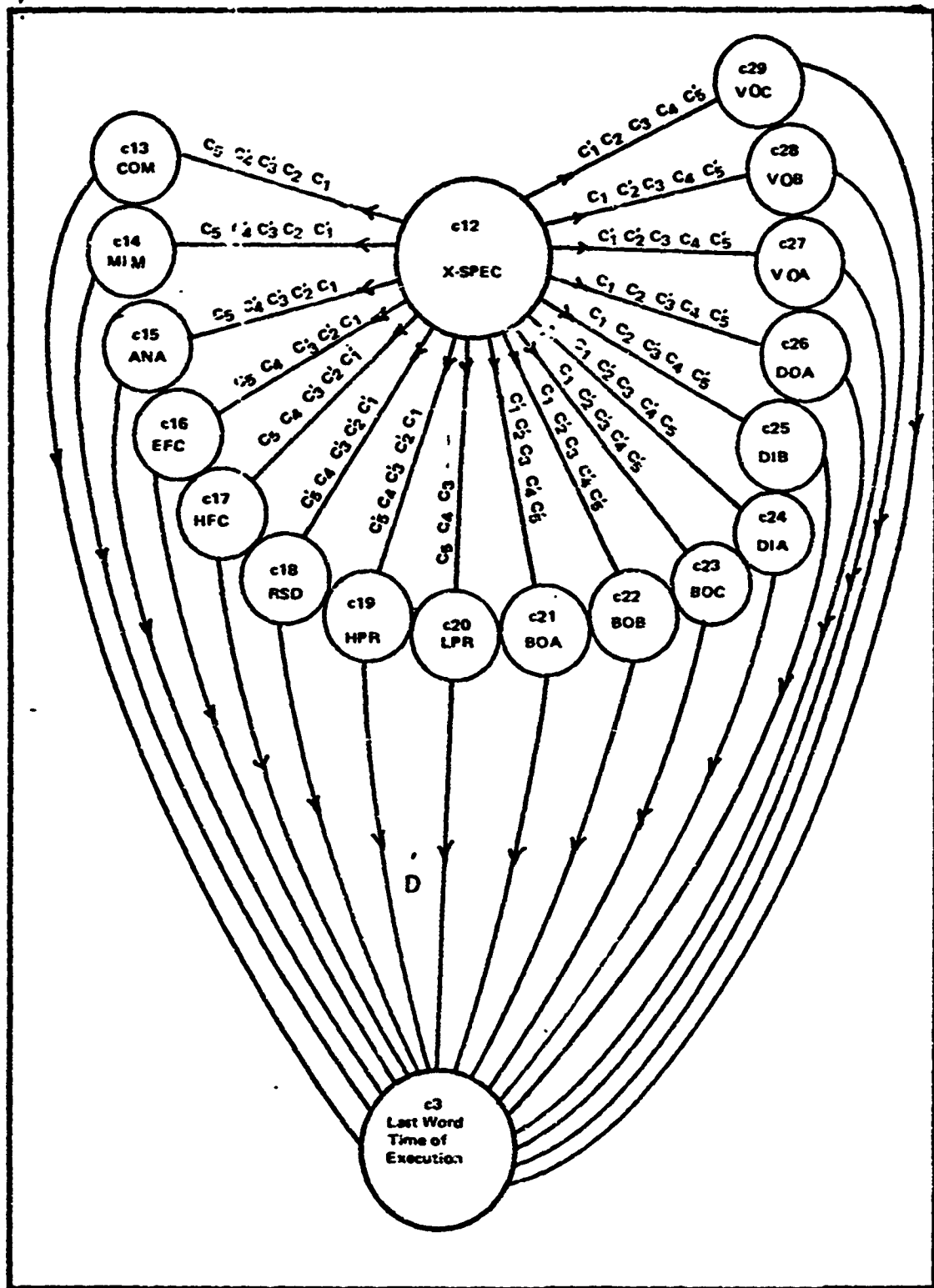


Fig. 11 X-Special Compute States

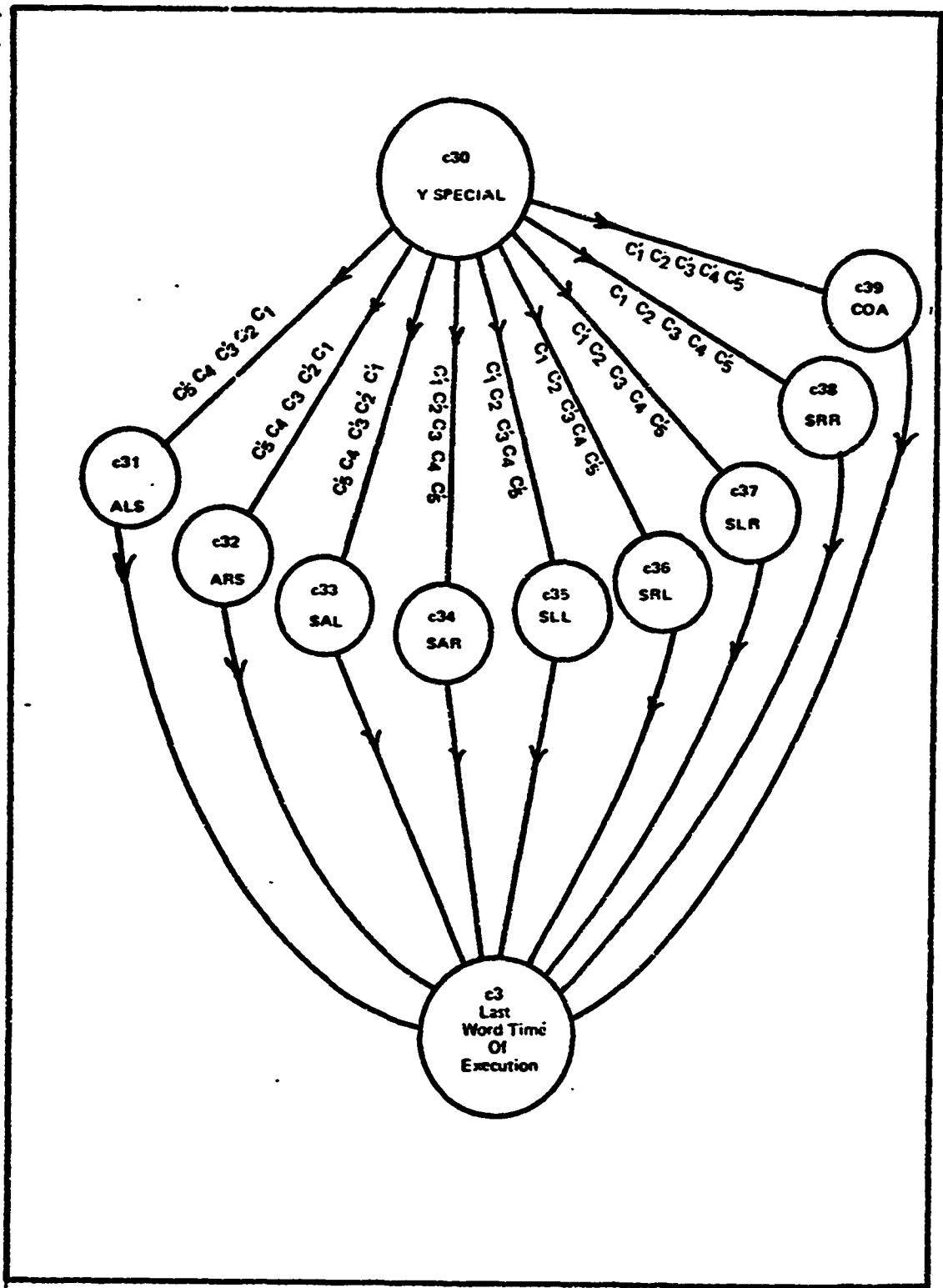


Fig. 12 Y Special Compute States

TABLE IX

Register Transfer Equations for the Compute States of the D-17B Computer.

Note: This table may be used with Table X, the number in parenthesis to the right of the register transfer equation designates the associated equation in Table X

State	State Name	Information Transfer
c1	Compute Instruction Search	$T_i(I_p \oplus S) : 1 \Rightarrow O_{b3} \quad i = 14, \dots, 20$
		$T_i O_{b3} : 1 \Rightarrow O_{b2} \quad i = 4, 17, 18, 24$
		$T_i O_{b3} : 1 \Rightarrow O_{b1} \quad i = 5, 18, 23, 21$
		$T_i O_{b3} : 1 \Rightarrow I_d \quad i = 16, 17$
		$T_{22} O_{b1} : 1 \Rightarrow I_d$
		$c1 T_o I_d : 0 \Rightarrow D$ $c1 \rightarrow c2$
c2	Instruction Read - Number Search	$T_i(I_p \oplus S) : 1 \Rightarrow O_{b3} \quad i = 2, \dots, 8$
		$T_4 O_{b3} : 1 \Rightarrow O_{b2}$
		$T_5 O_{b3} : 1 \Rightarrow O_{b1}$
		$T_6 O_{b3} : 1 \Rightarrow S_{b1}$
		$c2 T_{13} O_{bi} : 1 \Rightarrow N_d \quad i = 1, 2, 3$
		$c2 I_d T_o : 1 \Rightarrow I_c$ $(M(C_p)) = 1$
		$T_p : 0 \Rightarrow I_c$ $(I_{24}) \Rightarrow I_p$
		$(I_j) \Rightarrow O_{bi-20} \quad i = 21, 22, 23$
		$(I_j) \Rightarrow C_{bi-7} \quad i = 8, \dots, 12$
		$c2 I_{20} : 1 \Rightarrow S_{b1}$ $I_1 \Rightarrow S_{b1} \quad i = 17, 18, 19$
		$N_d T_p : c2 \rightarrow c1 \quad i = 4, \dots, 10, 12, 30, 40, \dots, 44$
		$A_{24} T_x : c2 \rightarrow c1$
		$c2 I_c K_r^* : 0 \Rightarrow K$ $c2 \rightarrow n22$

TABLE D(CONT)

State	State Name	Information Transfer
		$c2 O_4 O_3 O_2 O_1 T_x A_{24} : 0 \Rightarrow D$ $c2 \rightarrow c1$
c3	Last Word Time of Execution	$c3 T_p K_T^* : 0 \Rightarrow K$ $c41 \rightarrow n22$
c4	Unconditional Transfer	$c4 N_d^* T_x : 0 \Rightarrow I_d, 0 \Rightarrow D$ $c4 \rightarrow c3$ $c3 T_o : (C_{bi}) \Rightarrow C_{pi} \quad i = 1, 2, \dots, 5$
c5	Conditional Transfer	$c5 T_x A_{24} : 1 \Rightarrow O_4$ $c5 \rightarrow c4$
c6	Store	$c6 {}_1S_1 {}_1S_2 T_x : 1 \Rightarrow S_1, 1 \Rightarrow S_2$ (45) (46) $c6 \rightarrow c3$ $(A) \Rightarrow M (c [1], s [1] - 2)$ $c6 E_{wc} : c6 \rightarrow c3$ $(A) \Rightarrow M (c [1], s [1] - 2)$ $c6 T_x C_{b5} C_{b4} C_{b3} C_{b2} C_{b1} : 1 \Rightarrow V_c$ $c6 \rightarrow c3$ $(A)_i + V_{ki} \Rightarrow V_i \quad i = 1, \dots, 24$
c7	Clear and Add	$c7 T_x : 1 \Rightarrow N_c$ $1 \Rightarrow A_c$ $c7 \rightarrow c3$ $(M (o [1])) \Rightarrow A$
c8	Add	$c8 T_x : 0 \Rightarrow A_k$ $c8 \rightarrow c3$ $(M (o [1])) + (A) \Rightarrow A$
c9	Subtract	$c9 T_x : 0 \Rightarrow A_k$ $c9 \rightarrow c3$ $(A) - (M (o [1])) \Rightarrow A$
c10	Split Add	$c10 T_x : 0 \Rightarrow A_k$ $c10 \rightarrow c3$ $c3 {}_1A_c : 1 \Rightarrow A_c$ (47) $(A)_i + (M (o [1])) \Rightarrow A_i$ $i = 1, 2, \dots, 11, 14, 15, \dots, 24$ $c3 O_1 T_{12} : 0 \Rightarrow A_c$ $(A)_i \Rightarrow A_i \quad i = 12, 13$ $c3 T_p : 0 \Rightarrow A_c$

TABLE IX(CONT)

State	State Name	Information Transfer
c11	Split Subtract	$c11 T_x : 0 \Rightarrow A_k$ $c11 \rightarrow c3$ $c3 \text{ } {}_1A_c : 1 \Rightarrow A_c \quad (47)$ $(A_i) \cdot (M(o[1])) \Rightarrow A_i \quad i = 1, 2, \dots, 11, 14, 15, \dots, 24$ $c3 \text{ } {}_0T_{12} : 0 \Rightarrow A_c$ $(A_i) \Rightarrow A_i \quad i = 12, 13$ $c3 T_p : 0 \Rightarrow A_c$
c12	X Special	No Action
c13	Complement	$c13 T_x : c13 \rightarrow c3$ $c3 \text{ } {}_1A_c : 1 \rightarrow A_c \quad (48)$ $c3 \text{ } {}_2A_c : A_x \rightarrow A_p$ $2\text{'s Complement of } (A) \Rightarrow A$
c14	Minus Magnitude	$c14 \text{ } {}_{24}A' T_x : 1 \Rightarrow C_{b1}$ $c14 \text{ } {}_{b1}C T_0 : 1 \Rightarrow C_1$ $c14 - c13$
c15	Logical And To Accumulator	$c15 T_x : c15 \rightarrow c3$ $c3, \text{ } {}_pA : A_i \cdot L_i \rightarrow A_i$ $i = 1, \dots, 24 \quad (49)$
c16	Enter Fine Countdown	$c16 : 1 \Rightarrow F_c$
c17	Halt Fine Countdown	$c17 : 0 \Rightarrow F_c$
c18	Reset Detector	$c18 : 0 \Rightarrow D_r$
c19	Halt and Proceed	$c19 T_x : c19 \rightarrow c3$ $c3 \text{ } {}_0K : 0 \Rightarrow K \quad (50)$ $c3 \rightarrow n22$
c20	Load Phase Register	$c20 T_x : c20 \rightarrow c3$ $c3 : C_2 \Rightarrow P_2$ $C_1 \Rightarrow P_1$ $I_5 \Rightarrow P_3$
c21	Binary Output I	$c21 G_1 : (A_i) + 1 \Rightarrow A_i \quad i = 17, \dots, 24$ $c21 G'_1 : (A_i) - 1 \Rightarrow A_i \quad i = 17, \dots, 24$ $(A_{24}) \Rightarrow G_1$

TABLE IX(CONT)

State	State Name	Information Transfer
c22	Binary Output 2	$c22 G_2 : (A_i) + 1 \Rightarrow A_i \quad i = 17, \dots, 24$ $c22 G_2' : (A_i) - 1 \Rightarrow A_i \quad i = 17, \dots, 24$ $(A_{24}) \Rightarrow G_2$
c23	Binary Output 3	$c23 G_3 : (A_i) + 1 \Rightarrow A_i \quad i = 17, \dots, 24$ $c23 G_3' : (A_i) - 1 \Rightarrow A_i \quad i = 17, \dots, 24$ $A_{24} \Rightarrow G_3$
c24	Discrete Input A	$c24 T_x : 0 \Rightarrow A_p$ $c24 \rightarrow c3$ $X_i^* \Rightarrow A_i \quad i = 1, \dots, 19$ $D_r \Rightarrow A_{20}$ $F_c \Rightarrow A_{21}$ $P_3 \Rightarrow A_{22}$ $P_1 \Rightarrow A_{23}$ $P_2 \Rightarrow A_{24}$
c25	Discrete Input B	$c25 T_x : 0 \Rightarrow A_p$ $c25 \rightarrow c3$ $Y_i^* \Rightarrow A_i \quad i = 1, \dots, 24$
c26	Discrete Output A	$c26 T_x : c26 \rightarrow c3$ $(I_j) \Rightarrow D_i \quad i = 1, \dots, 5$
c27	Voltage Output A	$c27 T_x : 0 \Rightarrow A_k$ $c27 \rightarrow c3$ $A_i \Rightarrow V_{1j} \quad \begin{matrix} I_4 : i = 1, \dots, 8 \\ I_4' : i = 17, \dots, 24 \\ j = 1, \dots, 8 \end{matrix}$
c28	Voltage Output B	$c28 T_x : 0 \Rightarrow A_k$ $c28 \rightarrow c3$ $A_i \Rightarrow V_{2j} \quad \begin{matrix} I_4 : i = 1, \dots, 8 \\ I_4' : i = 17, \dots, 24 \\ j = 1, \dots, 8 \end{matrix}$
c29	Voltage Output C	$c29 T_x : 0 \Rightarrow A_k$ $c29 \rightarrow c3$ $A_i \Rightarrow V_{3j} \quad \begin{matrix} I_4 : i = 1, \dots, 8 \\ I_4' : i = 17, \dots, 24 \\ j = 1, \dots, 8 \end{matrix}$
c30	Y Special	No Action

TABLE IX (CONT)

State	State Name	Information Transfer
c31	Accumulator Left Shift	$c31 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c31 (C_b) \text{ } 1 : A_i \Rightarrow A_i + 1 \quad 0 \Rightarrow A_0$ $(C_b) - 1 \Rightarrow C_b$ $c31 \text{ }_0D : c31 \rightarrow c3$ $c3 (C_b) = 1 : (A_i) \Rightarrow A_i + 1 \quad i = 1, \dots, 23$ $0 \Rightarrow A_1$ <p style="text-align: right;">(51)</p>
c32	Accumulator Right Shift	$c32 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c32 (C_b) \text{ } 1 : A_i \Rightarrow A_{i-1} \quad i = 2, \dots, 24$ $A_{24} \Rightarrow A_{24}$ $(C_b) - 1 \Rightarrow C_b$ $c32 \text{ }_0D : c32 \rightarrow c3$ <p style="text-align: right;">(51)</p> $c3 (C_b) = 1 : A_i \Rightarrow A_{i-1} \quad i = 2, \dots, 24$ $A_{24} \Rightarrow A_{24}$
c33	Split Accumulator Left Shift	$c33 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c33 (C_b) \text{ } 1 : A_i \Rightarrow A_{i+1} \quad i = 1, \dots, 10, 14, \dots, 23$ $0 \Rightarrow A_1, A_{14}$ $(C_b) - 1 \Rightarrow C_b$ $c33 \text{ }_0D : c33 \rightarrow c3$ <p style="text-align: right;">(51)</p> $c3 (C_b) = 1 : (A_i) \Rightarrow A_{i+1} \quad i = 1, \dots, 10, 14, \dots, 23$ $0 \Rightarrow A_1, A_{14}$
c34	Split Accumulator Right Shift	$c34 : I_i \Rightarrow C_{b3} \quad i = 1, \dots, 5$ $c34 (C_b) \text{ } 1 : A_i \Rightarrow A_{i-1} \quad i = 2, \dots, 11, 15, \dots, 24$ $A_{11} \Rightarrow A_{11}$ $A_{24} \Rightarrow A_{24}$ $(C_b) - 1 \Rightarrow C_b$ $c34 \text{ }_0D : c34 \rightarrow c3$ <p style="text-align: right;">(51)</p> $c3 (C_b) = 1 : (A_i) \Rightarrow A_{i-1} \quad i = 2, \dots, 11, 15, \dots, 24$ $A_{11} \Rightarrow A_{11}$ $A_{24} \Rightarrow A_{24}$
c35	Split Left Word Left Shift	$c35 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c35 (C_b) \text{ } 1 : (A_i) \Rightarrow A_{i+1} \quad i = 14, \dots, 23$ $0 \Rightarrow A_{14}$ $c35 \text{ }_0D : c35 \rightarrow c3$ <p style="text-align: right;">(51)</p> $c3 (C_b) = 1 : (A_i) \Rightarrow A_{i+1} \quad i = 14, \dots, 23$ $0 \Rightarrow A_{14}$
c36	Split Right	$c36 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c36 (C_b) \text{ } 1 : (A_i) \Rightarrow A_{i+1} \quad i = 1, \dots, 10$

TABLE IX (CONT)

State	State Name	Information Transfer
	Word Left Shift	$0 \Rightarrow A_1$ $c36 \text{ } {}_0D : c36 \rightarrow c3$ $c3 (C_b) = 1 : (A_i) \Rightarrow A_{i+1} \quad i = 1, \dots, 10$ $0 \Rightarrow A_1$
c37	Split Left Word Right Shift	$c37 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c37 (C_b) \rangle 1 : (A_i) \Rightarrow A_{i-1} \quad i = 15, \dots, 24$ $A_{24} \Rightarrow A_{24}$ $c37 \text{ } {}_0D : c37 \rightarrow c3$ $c3 (C_b) = 1 : (A_i) \Rightarrow A_{i+1} \quad i = 15, \dots, 24$ $A_{24} \Rightarrow A_{24} \quad (51)$
c38	Split Right Word Right Shift	$c38 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c38 (C_b) \rangle 1 : A_i \Rightarrow A_{i-1} \quad i = 2, \dots, 11$ $A_{11} \Rightarrow A_{11}$ $c38 \text{ } {}_0D : c38 \rightarrow c3$ $c3 (C_b) = 1 : (A_i) \Rightarrow A_{i-1} \quad i = 2, \dots, 11$ $A_{11} \Rightarrow A_{11} \quad (51)$
c39	Single Character Output	$c39 : I_i \Rightarrow C_{bi} \quad i = 1, \dots, 5$ $c39 (C_b) \rangle 1 : (A_i) = C_{i-20} \quad i = 21, \dots, 24$ $c39 (C_{bi}) = 1 : J' \Rightarrow J \quad i = 1, \dots, 4$ $c39 \text{ } {}_0D : c39 \rightarrow c3 \quad (51)$
c40	Split Compare and Limit	$c40 : A_{11} \Rightarrow C_{b4} A_{24} \Rightarrow J$ $(M \langle o[1] \rangle) \Rightarrow N$ $c40 \text{ } r [(A)] \rangle r [(N)] : 1 \Rightarrow C_{b3}$ $c40 \text{ } l [(A)] \rangle l [(N)] : 1 = C_{b1}$ $c40 \text{ } {}_0D : c40 \rightarrow c3$ $c3 C_{b3} C_{b4} : r [(N)] \Rightarrow r [A]$ $c3 C_{b3} C_{b4} : 2\text{'s complement of}$ $r [(N)] \Rightarrow [A]$ $c3 C_{b1} J' : 1 [(N)] \Rightarrow 1 [A]$ $c3 C_{b1} J : 2\text{'s complement of } 1 [(N)] \Rightarrow [A]$
c41	Multiply	$c41 : (A) \Rightarrow L$ $(M \langle o[1] \rangle) \Rightarrow N$ $(L) \times (N) \Rightarrow A$ $c41 \text{ } {}_0D : c41 \rightarrow c3 \quad (51)$

TABLE IX (CONT)

State	State Name	Information Transfer
c42	Split Multiply	$c42 : (l [A]) = r [L]$ $(r [A]) \Rightarrow l [L]$ $(M (o [i])) \Rightarrow N$ $(l [L]) \times (r [N]) \Rightarrow r [A]$ $(r [L]) \times (l [N]) \Rightarrow l [A]$ $c42_{oD} : c42 \rightarrow c3$
c43	Split Multiply Modified	$c43 : (C_{bi}) + (P_i) \Rightarrow C_{bi} \quad i = 1,2,3$ $l ([A]) \Rightarrow n [L]$ $r ([A]) \Rightarrow [L]$ $(M (C_{p,s} [i])) \Rightarrow N$ $(l [L]) \times (r [N]) \Rightarrow l [A]$ $c43_{oD} : c43 \rightarrow c3$

(S1)

(S1)

Information for this table was obtained from Ref 7: 37-54 and Ref 14: 5.1 -- 6.13

TABLE X

Logic Equations Used in a State Description of the D-17B Computer.

Equation Number	Equation
(1)	$1O_1 = K' V_c' J O_1' S B_6 B_3' B_5'$
(2)	$0O_1 = K' V_c' O_4' O_1 S B_6 B_3' B_5'$
(3)	$0R_c = K' V_c' R_c J S B_6 B_3' B_5' O_1$
(4)	$1O_4 = K' V_c' R_c' J O_1 O_2 S T_{24}$
(5)	$0O_2 = K' V_c' R_c' J T_{24} O_4' S_{b2}' K_h'$
(6)	$0O_4 = K' V_c' R_c J O_2 T_0 I_m$
(7)	$0O_4 = K' V_c' R_c' J O_2' T_0 S_{b2} K_h'$
(8)	$0O_2 = K' V_c' R_c' J T_{24} O_4 O_2 O_1$
(9)	$1V_c = K' V_c' R_c' J T_x O_1 O_2 F_s'$
(10)	$1O_2 = K' V_c' R_c' J O_4' O_2' T'$
(11)	$1V_c = K' V_c' R_c' J T_x O_4' O_2'$
(12)	$1S_{b2} = K' V_c' R_c' J S_{b3}'$
(13)	$1V_c = K' V_c' R_c' J T_x O_1 O_2 F_s'$
(14)	$1D = K' V_c' J B_3'$
(15)	$1K = K' V_c' R_c' J D' T_{13}$
(16)	$1R_c = K' V_c' J T^* T_{11}$
(17)	$0V_c = K' V_c' J R_c' S_{b2} T_x$
(18)	$0R_c = K' V_c' T^* T_{13}$
(19)	$0J = K' V_c' R_c T_{23}$
(20)	$0S_{b3} = K' J V_c' R_c O_4$
(21)	$1C_{p5} = K' V_c' B_6'$
(22)	$1L_c = K' J' V_c' R_c' C_{p5} C_{p4} C_{p3} C_{p2} C_{p1} T_0$
(23)	$0L_c = K' T_{24}$
(24)	$1J = K' V_c' R_c' T_p C_{p5}$

TABLE X (CONT)

Equation Number	Equation
(25)	${}_1O_2 = K' J'$
(26)	${}_0V_c = K' V_c R'_c J C_{p5} S'_{b3} T_p$
(27)	${}_0O_3 = K' J' V_c R'_c C_{p5} C_{p4} C_{p3} C_{p2} C'_{p1} T_p$
(28)	${}_0O_4 = K' V_c R'_c J C_{p5} C_{p4} T_0$
(29)	${}_0V_c = K' J' V_c R'_c C_{p5} C_{p4} C'_{p3} C'_{p2} C'_{p1} T_{.13}$
(30)	${}_0V_c = K' J R'_c V_c C_{p5} C_{p4} C_{p3} C'_{p2} C'_{p1} T_p$
(31)	${}_0E = K' V'_c$
(32)	${}_0O_4 = K' J' T_{24}$
(33)	${}_1J = K' V'_c R'_c K'_T T_p$
(34)	${}_1A_c = K' J V_c R'_c C_{p5} C_{p4} C_{p3} C'_{p2} C'_{p1} T_0$
(35)	${}_0D = K' J V_c R'_c C_{p5} C_{p4} C_{p3} C'_{p2} C'_{p1} T_p$
(36)	${}_1O_{b3} = B_4 (I'_p S' + I_p S')$
(37)	${}_1D = N'_d D' T_p$
(38)	${}_1E = E' N'_d D' T_p$
(39)	${}_0D = K' E N_d D T_p$
(40)	${}_0I_p = A_k I_x I'_c K' T_{px}$
(41)	${}_1I_p = A_k I'_x I'_c K' T_{px}$
(42)	${}_1D = E D' T_p K' V_c$
(43)	${}_0E = E D' T_p K'$
(44)	${}_1S_{b2} = E D' T_{pxo} A_x N'_x K' O_3$
(45)	${}_1S_1 = O'_3 O_2 O_1 E Q' C_{b5} C'_{b4} C_{b3} C'_{b2} T_x$
(46)	${}_1S_2 = O'_3 O_2 O_1 E O' C_{b5} C'_{b4} C_{b3} C'_{b1} T_x$
(47)	${}_1A_c = K E O_4 O'_3 O'_2 O_1 B_3$
(48)	${}_1A_c = K E O_4 O'_3 O'_2 O_1 E C_5 C_4 C_3 C_2 C_1 A_x T_p T_x T_0$
(49)	${}_1A_p = K O_4 O'_3 O'_2 O_1 E' C_5 C_4 C_3 C_2 C_1 T_x A'_x L_x$

TABLE X (CONT)

Equation Number	Equation
(50)	${}_0K = K E O_4 O_3 O_2 O_1 C_5 C_4 C_3 C_2 C_1 T_p$
(51)	${}_0D = K E C_{b5} C_{b4} C_{b3} C_{b2} N_d T_x$
(52)	${}_1O_3 = K' J' V_c R_c C_{p5} C_{p4} C_{p3} C_{p2} C_{p1} T_p$
(53)	${}_1I_c = C_{p5} C_{p4} C_{p3} C_{p2} C_{p1} T_0$

Information Used to Construct this Table was obtained from Ref 14: 1.1 - 2.15, 5.1 - 6.13 and Ref 19: 5-44 - 5-162.

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initialized to start the synchronization of the bit counter with the sector track. Control flip-flop O_2 and J are "one" set to allow transition to the Sync Bit Counter 1 state.

Sync Bit Counter 1 (n2). This state is the second state during which synchronization of the Bit Counter and the Sector Track is accomplished. As shown on the state diagram, a transient master reset signal (less than one memory revolution in duration) will cause the machine to recycle through the Prepare to Compute State. The O_1 flip-flop is "one" set allowing entry into the next state, Sync Bit Counter 2.

Sync Bit Counter 2 (n3). In this state the instruction register is loaded with an unconditional jump instruction to channel 0, sector 0. This instruction will be the first instruction executed unless a new instruction is loaded prior to the computer entering the compute mode.

After complete synchronization of the bit counter and the sector track, the R_c and O_1 flip-flops are "zero" set allowing transition to the Manual Halt-Idle 1 state.

Manual Halt-Idle 1 (n4). This state acts as a decision point for state transition. Three separate situations will cause the computer to enter the Manual Halt-Interlock state. If the previous state were n3 or n7, then state n4 was entered at a bit time corresponding to T_x of sector number 0; thus, the O_4 flip-flop will be "one" set prior to the occurrence of any other state-determining transition.

A third situation, which could cause transition from n4 to n5, arises when the computer control switch is placed into "Halt" or "Single Step" during a compute operation. State n4 will be entered from Program Halt and transition will occur to state n5 or n7 depending on the O_1 flip-flop state will be determined by the instruction that was being executed when the compute switch was placed in the Halt or Single Step. State n7 may be the next state entered if the previous state were n5. In this case, n4 was entered at a bit time corresponding to T_1 of sector 177, thus allowing the O_1 flip-flop to be "one" set according to equation (1) Table X.

State n8, Prepare to Compute, will be entered if the "Compute" switch is not in a "Halt" position and S_{b2} is "zero" set. S_{b2} is a flip-flop that is "one" set as the result of a verify or parity error.

Manual Halt-Interlock (n5). If there is no Mechanical Reader Input Signal (I_m^*) present or if a "Halt" command is present from the "Compute" Switch or if a Sprocket timing Interlock signal (T^*) is present with no Fill Signal, the computer will cycle between states n6 and n5. Similarly, a cycle will exist through n7, n4, and n5 if a Mechanical Reader Input signal is present with no Fill signal (F^*). "Wait" state, n9, will be entered if a Fill signal is present. Thus Manual Halt-Interlock, n5, acts as an interlock for the state transition process of the computer.

Manual Halt-Prepare to Load (n6). Prepare to Load state is entered if a device such as a photo reader is used for loading. From this state, transition will be back to n5 if a Sprocket Timing Interlock Signal (T^*) is present or to the Wait state, n9, if no T^* signal is present.

Manual Halt-Idle 2 (n7). The Manual Halt - Idle 2 state serves as a timing delay. From this state the computer will enter n6 if the compute switch is in the "Halt" position and/or a Parity Error has occurred. If no parity or verify errors have occurred, the next state will be n8, the Prepare to Compute State. In the event that a Fill signal (F_x^*) occurs, the next state will be n9.

Prepare to Compute (n8). In the Prepare to Compute State initialization of several flip-flops is accomplished in preparation for entry in the Number Search State of Compute. J must be "one" set allowing the D flip-flop to be "one" set. Then when agreement is reached between sector track and the Number Register, K is "one" set.

Wait (n9). Flip-flops are initialized to receive the Input Load code in the Wait State. The computer will cycle between this state, n9, and Prepare to Sample, n10, until the Sprocket Timing Interlock signal, T^* , has reached steady state. If a verify error occurs the Idle 2 state will be reentered.

Prepare to Sample (n10). The primary purpose of the Prepare to Sample state, n10, is to allow the Sprocket Timing Interlock signal to reach steady state as described above. When this occurs, the computer will remain in the Prepare to Sample state until bit time T_{23} occurs and will then transition to the Sample state, n11.

Sample (n11). During the Sample state the computer will load the information on Input Lines I_1^* through I_5^* . Note that flip-flops C_{p1} through C_{p4} were "zero" set in state n9 and will be "one" set only by an I^* input. At bit time T_{13} the computer will enter the Parity Check state.

Parity Check (n12). Flip-flops S_{b3} will toggle on C_{pi} as C_{p1} through C_{p4} complete a circular shift. This circulation will occur on each bit time when the O_4 flip-flop is "one" set. In order to insure circulation for only five bits times the O_4 flip-flop is "one" set on bit time T_{20} and "zero" set on bit T_{24} . "One" setting the C_{p5} flip-flop will allow a change to one of the Process Code states depending upon the contents of the Input Lines.

Clear (n13). The clear load code causes the Lower Accumulator, L, to be filled with zeroes. "One" setting the L_c flip-flop allows new information to be read into L starting with bit time T_0 . Then the C_{p1} flip-flop is copied into the L_p flip-flop at bit times T_1 through T_{24} . At T_{24} the L_p flip-flop is "zero" set preventing new information from being read into the L-loop. If a parity error is indicated by a S'_{b3} at bit time T_p , the next mode will be n9; however, if no parity error occurs, the computer will go to state n7, the Wait State.

Delete (n15). When the input lines are all "ones" no action is taken by the computer. This

command can be used as a space in input tape. Five "zeroes" are not used as a Delete command because the S_{b3} flip-flop would indicate a parity error.

Prepare to Fill (n 15). The Prepare to Fill State is a preparation state for filling the memory. After the Fill command is processed, the succeeding Load codes will be loaded into memory until "Halt" or "Start Compute" commands are processed. In the event a parity error occurs, the next state will be n7; if no parity error occurs, n9 will be next.

Prepare to Verify. The Prepare to Verify State, n16, is analogous to the Prepare to Fill State. Once the computer cycles through this state (caused by processing a load code $I_5 I_4 I_3 I_2 I_1$) the succeeding load codes will be compared with the contents of memory as specified by the instruction Register. This actual operation will be executed as the result of an Enter command and will therefore be described as part of the Enter state. Exit from this Prepare to Verify is similar to that of the Prepare to Fill state.

Octal Numbers (n17). In this state the octal numbers received from the input lines will be stored in the L register. Any number of octal codes may be loaded, but only eight sets of octal digits may be stored in the Lower Accumulator at one time. Octal Numbers that are shifted out of L are lost. Exit from this state is similar to those of the other Process Code states.

Location (n18). In this state, n18, the contents of the L register is transferred to the instruction register. This information will contain the memory location, channel and sector number, that will be used to start Fill and Verify operations.

The I_c flip-flop is "one" set at bit time T_0 allowing new information to be written in the L register, then it is "zero" set at bit time $T_{2,4}$ after L is transferred to I.

Enter (n19). In this state, n17, the contents of the lower accumulator will be loaded first into the accumulator, then into memory if a Prepare to Fill state had initiated a fill operation. The contents of the Accumulator and memory will be compared if a verify operation had been initiated by the machine when cycling through the Prepare to Verify state. The location of memory involved in the above operation is specified by the Instruction Register. If a parity error is detected, transition will be from n19 to n7, otherwise an error-free operation will allow the computer to go from the Enter state to the Wait state.

At this point it is necessary to define a set of four states that the computer cycles through during a Fill or Verify operation. (A Fill or Verify operation results after the computer has successfully cycled through the Prepare to Fill or Prepare to Verify states and will continue until the Halt or Start compute state is reached.) These four states are called Fill-Verify Idle, fv1; Fill-Verify Number Search, fv2; Fill-Verify Wait 2 Word Times, fv3; and Fill-Verify Execute, fv4. The computer cycles

through these states simultaneously as it passes through the Enter state. A state diagram of this four-state operation is depicted in Fig. 9. These states will be discussed in conjunction with the Enter state, since they occur simultaneously beginning in the Enter state. The action taken by the computer will vary with the part of memory that is to be filled or verified, thus it is necessary to consider not only the Enter state and the four-state cycle described above, but also the part of the memory involved in this operation.

Fill-Verify Idle (fv1). During the Fill-Verify Idle state the Lower Accumulator is copied into the accumulator. "Zero" setting the D flip-flop causes transition to fv2, the Number Search State. This transition occurs simultaneously with a transition from n19 to n9 states.

Fill-Verify Number Search (fv2). During this state agreement is established between the Sector Track and the operand sector part of the I register. This comparison is made by the O_{b2} flip-flop during bit times T_2 through T_7 . The operand channel part of the I register is copied into the C_p register and channel agreement is established. The D and E flip-flops are "one" set to cause transition to the Wait Two Word Times State.

Fill-Verify Wait Two Word Times (fv3). During the Wait Two Word Times state the Channel Buffer is copied into the Channel Register. The Number Register copies the contents of memory as specified by the Channel Register. "Zero" setting the D flip-flop causes transition to the Fill-Verify Execute State.

Fill-Verify Execute (fv4). For both Fill and Verify operations the operand sector part of the I register will be augmented by one in this state. For Fill operations the contents of the Accumulator will be transferred to a memory location as specified by the Operand Address part of the I register. After the Fill operation, transition is made to the Fill-Verify Idle State. Verify operations are different in two ways. First, the contents of the Accumulator and the Number Register are compared. If agreement occurs, S_{b2} flip-flop will remain "zero" set and the next state will be fv1. Disagreement is indicated by S_{b2} "one" setting and the next state will be a Manual Halt state.

Halt (n20). When the "Halt" code is processed the Halt state will be entered and the V_c flip-flop will be "zero" set causing a transition to the Program Halt state.

Start Compute (n21). The Start Compute command, when entered on the Input lines, will cause the computer to enter the Manual Halt Idle 1 State before transitioning to the Prepare to Compute and Compute States. If a parity error occurred while processing the code, the computer will not transition from the Manual Halt states.

Program Halt (n22). Four separate conditions may cause the computer to enter n22, the Program Halt state: (1) If a "Halt" load code is successfully processed, the computer will enter n7 before returning to Manual Halt Idle states. (2) A halt instruction may be executed in the compute states. (3) If the Compute Switch is not in the "Run" position when a new instruction is found the computer will return to Program Halt state from the "Last Word Time State" of compute. (4) If during the Number Search state of compute the "Compute Switch" is not in "Run" and an instruction search is required to locate a new instruction the computer will enter n22. In all cases the computer prepares to enter one of the Manual Halt Idle states during the Program Halt state. The actual Idle state entered depends upon the state of the O_1 flip-flop which was set by the instruction being executed when state n22 was entered.

If state n22 were entered as the result of processing a Halt command during a fill or verify operation, the D and E flip-flops would be set to cause the computer to simultaneously enter the Idle state of the Fill-Verify operation.

Compute States. Ref (11:25) and (15:5.1 - 6.13)

The Compute States of the D-17B are controlled by seven major control flip-flops. The K flip-flop, when "one" set, indicates that the computer is in one of the "compute" states. The various states of compute are then controlled by the D and E flip-flop. When the E flip-flop is "one" set an instruction is being executed. The D flip-flop, when "one" set, indicates that an instruction search is in progress and when "zero" set indicates instruction read and/or operand search is in progress. The four flip-flops of the Operand Storage Register, O_4 through O_1 , determine the instruction that will be executed.

Instruction Search (c1). The Instruction Search State as defined in this report will be the state indicated by the flip-flop settings K D E'. It is not necessary for this state to occur with the execution of every instruction.

If a program is optimally coded, a new instruction can be read into the I register during the execution of the present instruction. In this case, the instruction search operation was performed as a result of the forethought of the programmer. Similarly, the Instruction Read-Number Search State may also be avoided by astute programming. In this case the computer would cycle between the two states of Execute without actually performing an instruction or operand search.

Instruction agreement occurs when the memory location addressed by "next instruction" part of I is in a position to be read by the computer. Monitoring for this condition is performed by the buffer flip-flops O_{b1} and O_{b2} . These two flip-flops are monitored by the I_d flip-flop which controls the D flip-flop. When the D flip-flop becomes "zero" set, transition to state c2 occurs.

Instruction Read-Number Search (c2). Instruction Read-Number Search state, c2, is a dual function state defined by DE flip-flop conditions. Like the Instruction Search State, this state may not necessarily be realized with the execution of every instruction. One-half of the dual function of the state may be exercised. For example, the next instruction may be found and read during the Execution State and the computer may cycle to state c3 for the Number Search function alone.

For number agreement the information in I_p at bit times $T_2 - T_8$ must agree with the Sector track, S. Since the loops are effectively separate channels of 4, 8, 16 word length more than one flip-flop is needed to check agreement for all channel lengths. Flip-flop O_{b2} monitors for agreement for the 4 word loops, O_{b1} monitors for 8 word loops, S_{b1} for 16 word loops and O_{b3} monitors for the full channel length, 128 words. The N_d flip-flop is the primary number agreement monitor and is changed by the above number agreement flip-flops at bit time T_{13} .

Instruction Read is accomplished by setting the desired memory channel into the C_{p5} through C_{p1} flip-flops. When the I_d flip-flop indicates Instruction agreement, the I_c flip-flop is "one" set allowing the new instruction to be read into the I register. Bits $I_{24}-I_{21}$ are read into the Operand Buffer Register, and $I_{12}-I_8$ are read into the channel buffer register. If the instruction is a flag-store instruction ($I_{20} = 1$) the flag channel information, I_{19} , I_{18} , and I_{17} is read into the Flag Code Buffer Register. If the instruction is not a flag store instruction, the Flag Code Buffer Register is loaded with "zeros."

From this state, c2, transition will be to one of the instruction execution states or to c1 in the case of the transfer on minus instruction with a positive accumulator (see state c4 description). If the Compute Switch is not in the "Run" position when the I_c flip-flop is "one" set to read a new instruction, the computer will go to Non Compute Program Halt, n22.

Last Word Time of Execute (c3). The Last Word Time of Execution, c3, will be discussed in conjunction with the execution of each of the instruction states since during this state the operation started in each of the instruction states is completed. For all one-word-time instructions ($O_4 = 1$), the instruction defining state is entered for the first bit time of execution and then the computer transitions to c3 to complete the operation.

This state acts as a decision point for the computer to exit the Compute Mode. If the Compute Switch is not in the "Run" position and a new instruction is found, the computer will go to state n22, Non Compute Program Halt.

Unconditional Transfer (c4). The word format of the D-17B makes no provision for specifying the channel of the next instruction. Thus, there must be a command to change channels of operation. The Unconditional Transfer is a "jump" instruction that is used for this purpose. In this "jump"

instruction the sector of next instruction field is ignored and the complete operand address serves as the address of the next instruction. The new channel address is contained in the Operand channel portion of the transfer instruction. This information was shifted to the program channel buffer register during the instruction search operation. At bit time T_0 the program Channel Buffer Register is parallel loaded into the Program Channel Register.

Instruction agreement is controlled by the number agreement flip-flop which determines the sector of the new instruction from bits I_7 through I_1 of the present instruction.

Conditional Transfer (c5). The decision for the Conditional Transfer operation is made in state c2. If bit A_{24} is zero, the accumulator is positive and the computer returns to state c1 to search for the instruction as indicated by $sp [1]$. A "1" in bit position A_{24} indicates that the accumulator contains a negative number and the computer goes to state c3 and selects the new instruction as indicated by $o [1]$.

Store Accumulator (c6). The Store state must be considered for four different situations; storing in channel 50, storing in channels 00-46, storing in the loops, and flag storing.

Storing in channel 50 or "hot storage writing" is initiated by setting the S_i flip-flop to the channel 50 store code, then the Accumulator is copied directly into channel 50 and in a sector two octal numbers less than the sector of $s [1]$. This two-sector difference is accounted for by the fact that the write heads are separated from the read heads by two sectors.

In order to store information in channels 00-46 an EWC signal must be present, enable write switch must be on. For selecting channels 00-46 the computer utilizes a separate selector switch for each channel. This selection is accomplished using the contents of Channel Storage Register. The Accumulator is then stored in the memory address specified by the $op [1]$ minus two sector positions.

Storing in the E, F, H loops is similar to storing in channel 50 except the S_i flip-flops are set by the contents of the channel buffer register.

Storing in the V and R loops may be accomplished if the computer is not in Fine Countdown mode (F_c1) (See state c17). In this case the contents of A is added to the incremental input at the time of execution.

A special case results when the T_{20} bit of any instruction is "1". This "flag", "1" in T_{20} , is used to execute two operations with one instruction. The contents of the Accumulator will be stored in the channel indicated by the contents of bits $I_{19} - I_{17}$. This means that the sector of next instruction field of the instruction being executed is limited to the four bits $I_{16} - I_{13}$ and the next instruction must be within the next 16 sectors. Flag storing is accomplished in the following steps: The Flag store buffer register S_b is loaded with the contents of $I_{19} - I_{17}$ during state c2. During the

execution of the instruction the Flag Store Buffer register is parallel-loaded into the flag store register. This information is used to select the proper write heads for writing the Accumulator contents into memory.

Clear and Add (c7). State c7 initiates the clear and add operation, in which the contents of memory as specified by the operand address is transferred to the Accumulator. In state c7 the N_c flip-flop is "one" set allowing the selected contents of memory to be read into the Number register. In state c3 the operation is completed, the selected contents of memory is read into the accumulator.

Add (c8). State c8 initiates the add operation in which the memory contents as specified by operand address is added to the accumulator. The sum is then stored in the accumulator.

Subtract (c9). Subtraction is accomplished by the hardware as addition in the D-17B; however, the carry operation of addition is converted to a borrow operation by a "one" in the O_2 flip-flop.

Split Add (c10). During the split add operation the split word contents of the accumulator is added to the corresponding parts of memory and the sum is stored in the split word portions of the accumulator. At bit times T_{12} and T_{13} the A_c flip-flop is "zero" set allowing the contents of A_{12} and A_{13} to remain unchanged.

Split Subtract (c11). The split subtract operation is similar to the split add operation, except that the split word contents of memory location specified by $o[1]$ is subtracted from the contents of the Accumulator.

X Special (c12). No action is performed in the X special state. It serves only as a decision point for the computer to enter a special set of states that require one word time to complete and do not require access to the computer memory. The Channel Storage Register contents are used to select the X Special State that will be entered from c12. In this special operation the channel storage register serves as an auxiliary operation-code storage register. Since all the S special operations are one word time instructions, the specific X special state serves to define the operation and much of the actual operation is performed in state c3.

Complement (c13). The complement operation causes the 2's complement of the Accumulator to be read into the accumulator. The accumulator is circulated and the A_c flip-flop is "one" set by the first "one" in the Accumulator. All succeeding bits of the accumulator are complemented.

Minus Magnitude (c14). When the computer enters the Minus Magnitude state, c14, the sign of the Accumulator is tested. If the Accumulator is negative no action is taken; if the Accumulator is positive the C_{b1} flip-flop is "one" set and copied into the C_1 flip-flop, thus generating a complement instruction.

Logical And to Accumulator (c15). Entering state c15 causes the corresponding bits of the Accumulator and Lower Accumulator to be logically "anded".

Enter Fine Countdown (c16). Entering the Fine Countdown causes the F_c flip-flop to be "one" set. This places the computer into a parallel operation called Fine Countdown. During Fine Countdown the V and U loops form a digital integrator. This operation will continue until the Halt Fine Countdown State is entered.

Halt Fine Countdown (c17). Entering the Halt Fine Countdown state, c17, causes the Fine Countdown flip-flop, F_c , to be "zero" set.

Reset Detector (c18). When the Reset Detector state is entered, the D_r flip-flop is "zero" set. The D_r flip-flop is "one" set by I_8^* .

Halt and Proceed (c19). Entering state c19, Halt and Proceed causes the computer to enter state c3 and then state n22, Program Halt.

Load Phase Register (c20). The Load Phase Register special instruction causes C_2 to be loaded into P_2 and C_1 is copied into P_2 . P_3 copies the I_x flip-flop at bit times T_1 through T_5 . State c20 is defined by three of the C flip-flops, C_5, C_4, C_3 ; the remaining two C flip-flops may be either "one" or "zero" set. The actual purpose in setting the Phase Register will be discussed in conjunction with states c27.

Binary Output (c21, c22, c23). Binary Incremental Output States may be discussed simultaneously. These states differ only in the sense that state c21 involves output flip-flop G_1 , c22 involves G_2 , and c23 involves G_3 . Only the first state, c21, will be discussed because the discussion is directly applicable to all three states by substituting the proper G_i flip-flop in state c2i, where $i = 1, 2, \text{ or } 3$.

In state c21 the state of the G_1 flip-flop is checked, if G_1 equals "1" the first eight bits of A is treated as a word and +1 is added to that word. If G_1 equals "0" a 1 is subtracted from the word formed by the first eight bits of A. After one of the above operations is accomplished the G_1 flip-flop copies the sign bit of A.

Discrete Inputs (c24, c25). In both discrete input operations a set of twenty-four discrete input lines and flip-flops are sampled and read into the A register. For a Discrete Input A, DIA, operation the discrete input lines X_1 through X_{19} and flip-flops D_r, F_c, P_3, P_1, P_2 replace bits A_1 through A_{24} respectively.

During the operation initiated by state c25, DIB the discrete lines Y_1 through Y_{24} replace bits A_1 through A_{24} respectively. The actual information transfer described in these states takes place in state c3; however, the states c24 and c25 serve to define the operation to be performed in state c3.

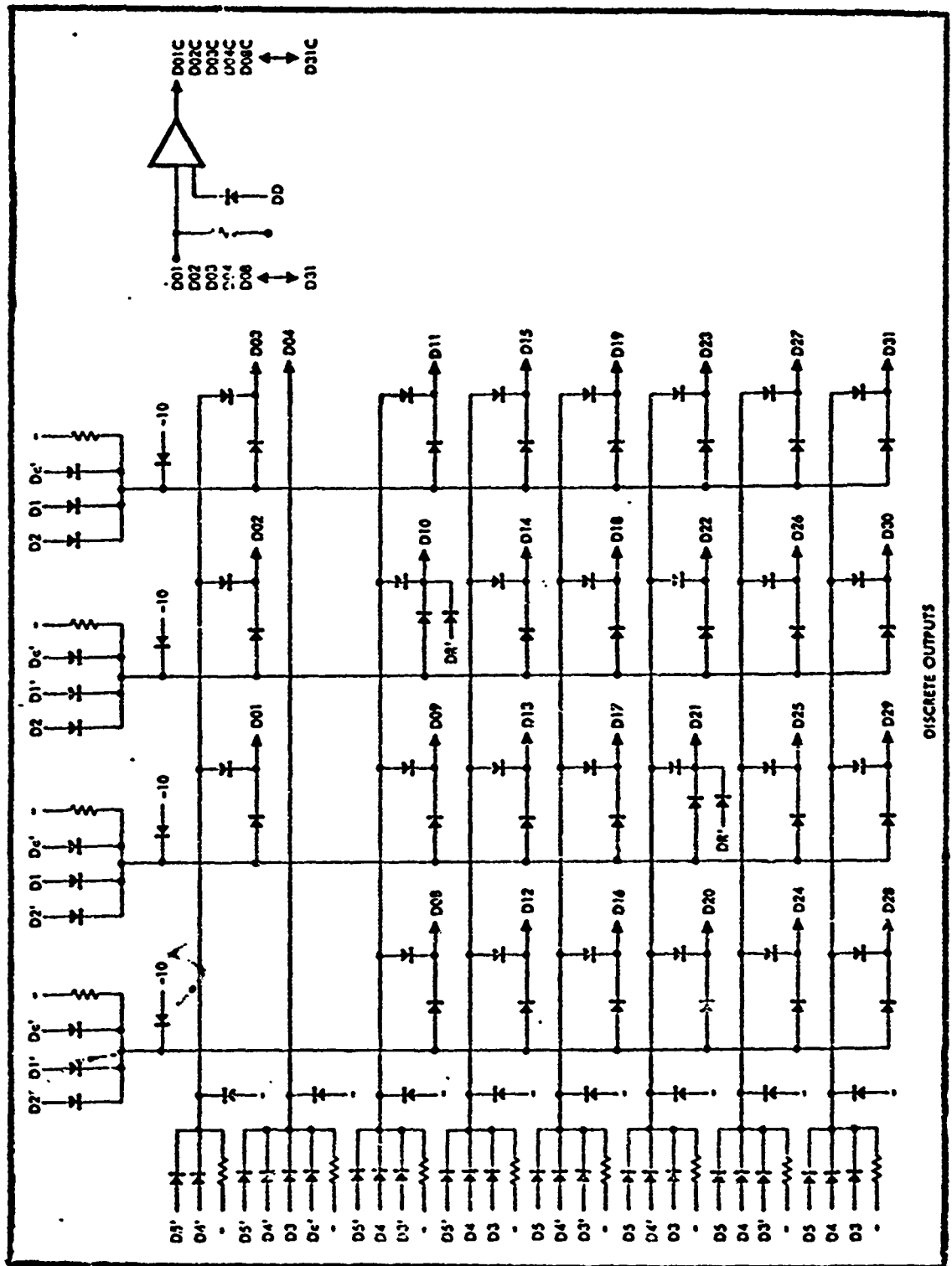


Fig. 13 D-17B Discrete Outputs (From Ref 11:TR48)

Discrete Outputs (c16). The operation initiated by state c2, Discrete Output A, causes the bits I_1 through I_5 to be loaded into the Discrete Output Register, D_1 through D_5 . Thus, the discrete output lines may be changed as depicted in Figure 13.

Voltage Output (c27, c28, c29). The Voltage Output States are identical in concept. The function of these states varies only in the physical location of the output voltage.

Three Voltage Output Registers are loaded with the split word contents of A. If I_4 is "1" the right half of A is loaded and if I_4 is "0" the left half of A is loaded.

The states c27, c28, c29 determine which set of Voltage-Output flip-flop, $V_{i1}-V_{i8}$, ($i=1, \text{ or } 2, \text{ or } 3$) will be loaded from A. If c27, VOA, is entered $V_{11}-V_{28}$ to be loaded; and c29, VOC, causes $V_{31}-V_{38}$ to be loaded with the proper half-word of A.

The Phase Register also affects the output location of each voltage line. The setting of the Phase Register is necessary to direct the voltage outputs as shown in Table VI.

Y Special State (c30). The Y Special State, c30, serves only as a decision point for entering specific states c31 through c38. Operations initiated by the Y Special State do not require access to Memory; however, they do require more than one word time to complete.

Accumulator Left Shift (c31). A left shift operation is accomplished in the D-17B by adding an extra flip-flop, A_k , to the A loop for the number of word times equal to the number of shifts required. The number of shifts is specified by I_1 through I_5 . This number is loaded into the Channel Buffer Register and counted down at each word time.

Accumulator Right Shift (c32). State c32 initiates a right shift of the Accumulator. To accomplish this operation the A_p flip-flop is removed from the recirculation loop of the Accumulator. The number of right shifts required is indicated by I_1 through I_5 and the A_p flip-flop remains out of the A loop for that number of word times. If the Accumulator is positive, zeroes are filled into the vacated bits; however, if the Accumulator contains a negative number, 1's replace the bit positions vacated by the right shift.

Split Accumulator Left and Split Accumulator Right Shift (c33, c34). The discussion of states c31 and c32 are directly applicable to the states c33 and c34 respectively. In the split-shift states the left and right half-words of the Accumulator are shifted the same number of bit positions but are treated as separate words.

Split Left Word Left Shift (c35). State c35 initiates an operation which causes the left half-word of the Accumulator to be shifted left by the number of bit positions specified in I_1 through I_5 . The discussion of state c31 is applicable to this state, except that bits A_{14} through A_{24} only are affected.

Split Right Word Left Shift (c36). Bits A_1 through A_{10} only are affected by the Split Right Word Left Shift operation. As implied by the state name, the right half-word of the A register is shifted left.

Split Left Word Right Shift (c37). State c37 initiates a right shift of the left half-word of the Accumulator. As in all right shift operations, if the half-word were positive, the bits vacated by the shifting are filled with zeroes and if the half word were negative, 1's are filled into the vacated bit positions.

Split Right Word Right Shift (c38). State c37 initiates a right shift of the right half-word of the Accumulator. The discussion of c37 is directly applicable to this state except the right half-word is shifted.

Single Character Output (c39). The operation initiated by state c39 shifts the four most significant bits out of the Accumulator and presents them to the four character output lines. A fifth character output-line is used as a parity line. This information is presented on the character output lines for the number of word times specified in $s[1]$.

The Single Character Output operation is accomplished in the following manner. The sector portion of the instruction operand is shifted into the Operand Channel Buffer Register. Each word time this register is decreased by one, thus it is used to terminate the operation after the end of $(s[1]) + 1$ word times.

During the first word time of the Single Character Output Operation the circulation loop of the Accumulator is extended to include four flip-flop's of the Operand Channel Buffer Register: C_1, C_2, C_3, C_4 . This causes the four most significant bits of the Accumulator to be left shifted into these C flip-flops. Parity is indicated by the J flip-flop by "zero" setting it at the beginning of the operation and allowing it to toggle as each "1" is shifted into the flip-flop.

The parity (J), and output (C_4, C_3, C_2, C_1) is presented on the output lines S_{C5} through S_{C1} respectively with the occurrence of each S_{CT} timing pulse.

Split Compare and Limit (c40). State c40 initiates the Split Compare and Limit Operation in which the split-word contents of the Accumulator is compared with the corresponding bits of a word in memory. The memory word is specified in the operand of the SCL instruction. If the contents of the memory word is greater than that of A, no changes are made. If the split word portion of A is positive and greater than the corresponding part of the memory word, the split memory word replaces the split-word of A.

If the quantity in memory is less than the corresponding part of A and that half-word of A is negative, the two's complement of the memory half-word replaces the Accumulator half word.

Multiply (c41). The Multiply Operation is initiated by state c41. The operation causes the contents of the Accumulator to be moved to the Lower Accumulator and the product of the Accumulator

and memory contents specified by the MPY operand is placed in the Accumulator.

Split Multiply (c42). State c42 initiates the Split Multiply Operation. This operation is similar to the Multiply operation except the left half-word of A goes into the right half-word of L. The split words of the Accumulator and the memory word specified by O I are multiplied and stored in the respective split words of the Accumulator.

Split Multiply Modified (c43). Split Multiply Modified is an operation which causes the three least significant bits of the Channel Buffer Register to be replaced by the "exclusive or" of those bits and the contents of the Phase register. The operation then proceeds as a Split Multiply operation. Split Multiply Modified commands allow the computer program to vary the effective operand channel address depending upon the Phase register contents.

Multiply Modified (c44). State c44 initiates the Multiply Modified operation which causes the three least significant bits of the Channel Buffer Register to be changed by an "exclusive or" operation with the Phase Register. After the above modification a multiply operation is accomplished as described in state c41. It is noteworthy that this operation does not change the original multiply instruction in memory.

State Description Summary.

In the above state description of the D-17B the various configurations of control flip-flops were used to define states of the computer. These state definitions are not unique and many other sets of flip-flop combinations may be used to describe the machine operation. For example a state description might be formed using only the K, D, and E flip-flops. The states described in this report were chosen because they could be given names that correlate with other published information about the D-17B. Hopefully, this type of description will be an aid not only in understanding the operations of the machine, but also in maintaining it. For example, the "state" of an inoperable machine may be determined by checking the status of the control flip-flops. Once the state is identified, the malfunctioning circuit may become apparent by considering which flip-flop is preventing normal state transition.

Other Techniques of Describing the D-17B

One description of the D-17B that was used in the original documentation describes the machine in terms of modes of operation (Ref 11:25-27, T12, TR15; Ref 16: 5-172 - 5-184). The term mode could be defined as the type of operation that the computer may perform. The machine then has two basic modes, "compute" and "non-compute". Compute operations are related to the actual performance of an instruction and the non-compute mode involves operations such as synchronization and reading instructions. These modes are further subdivided by the states of the D and E flip-flops (Ref 11:25).

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The state description in the previous section was patterned using this subdivision of modes (submodes). Veitch Diagrams. These submodes may be conveniently represented on a veitch diagram as shown in Figs. 14 and 15. This type of representation has the advantage of being compact; however, it does lack the facility for presenting the detail that is possible using a state description and the associated register transfer equations.

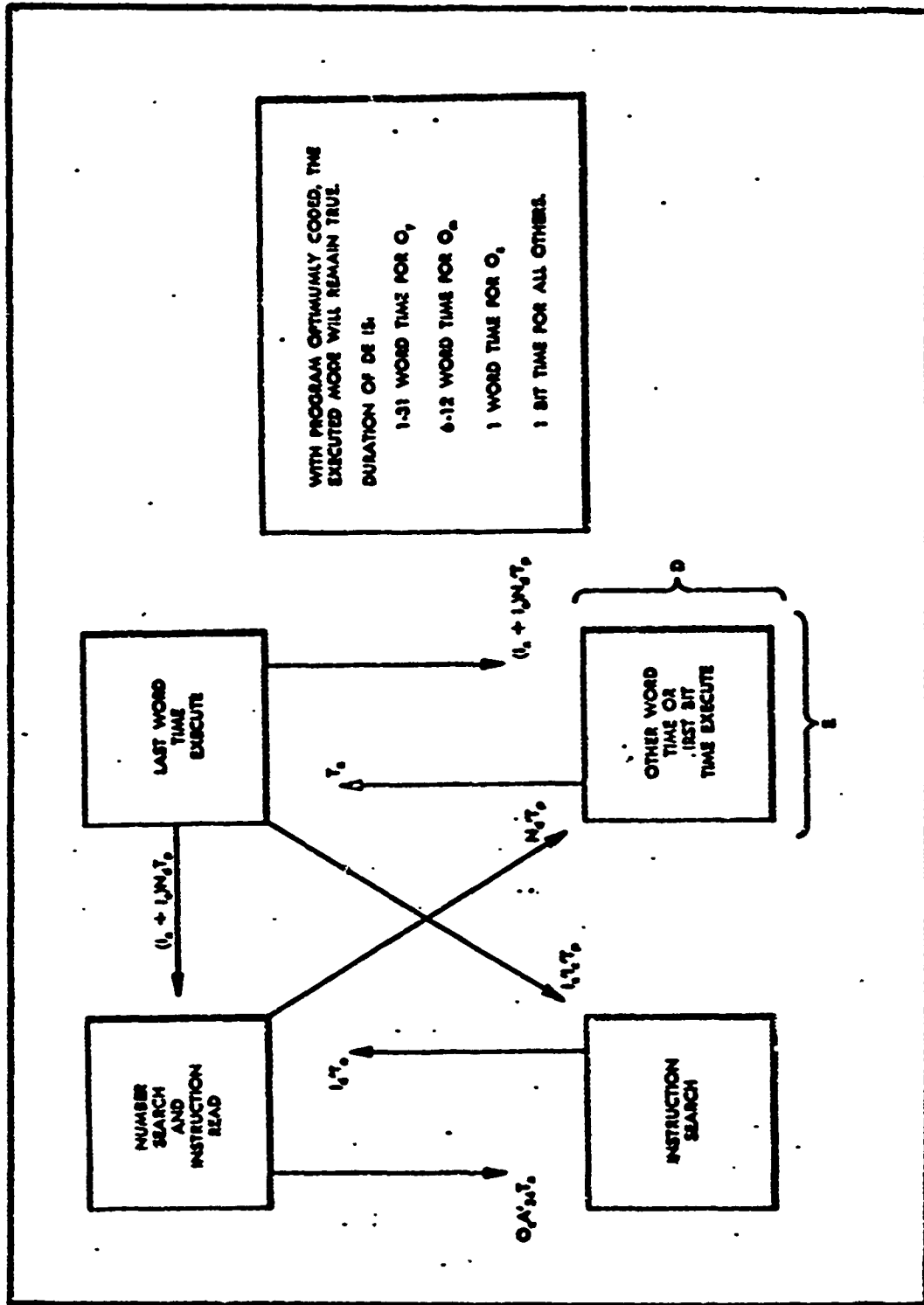


Fig. 14 Veitch Diagram of Compute Mode (From 2:41).

III. INITIAL PREPARATION OF D-17B COMPUTER

One remarkable specification of the D-17B computer system is a predicted 5.5 years mean time between failure (Ref 7: Table 1). This reliability estimation applies to a packaged control assembly that functioned in a controlled environment. Since many of the protective features of the designed missile environment have been removed, an unpackaged D-17B computer is easily damaged. To prevent damaging the system a well-planned installation procedure should be used.

This part of the report describes a process that could be used to unpack the computer and to determine if it is operable. The process can be divided into three phases: 1) preparation for power on, 2) initial power on, and 3) fabrication of a cooling system.

Preparation for Power On

The D-17B can be uncrated and prepared for the initial power-on checks in four to six days; however, since the system is easily damaged it is not recommended that this step be hastily completed (Ref 7:3).

The tools required for this procedure are: a 7/16 inch socket and ratchet drive, a 5/16-inch 12-point socket, an 18-inch speed handle socket drive, an Ampex no. 212-8 screwdriver bit, and electrical insulating tape.

Uncrating. The D-17B computer is shipped in a wooden crate. The top and all four sides of this crate should be removed, allowing access to the truncated cone-shaped computer housing. This black missile section is fastened to the base of the computer by eighteen 7/16-inch hex bolts. A 100-pin umbilical connector may be attached to the side of the missile section. The umbilical connector is 8 inches in diameter and is easily located. It should be disconnected from the missile section first to prevent stressing the wires that attach it to the computer. The 7/16-inch bolts should be removed and stored. When the last bolts are removed from the missile section, the D-17 will drop approximately one-half inch onto the bottom of the shipping crate. This will allow the missile section to be lifted free of the computer. The missile section could be used as a stand for the computer, as will be discussed later. Therefore, it should not be discarded.

Free Lead Wire Insulation. Once the missile section has been removed the computer and power supply sections may be observed. At this time it is advantageous to note that the cables and wire bundles that interconnect the different sections of the computer are easily broken and should be twisted or handled as little as possible.

In order to secure the cables that are on the underside of the circular mounting-frame the computer should be placed between two tables in such a way that the circular mounting-frame partially rests on

each table but does not rest on one of the wire bundles. In this position the nine loose wires that were initially part of the missile battery system may be insulated and tied to the mounting frame.

The top of the computer is covered with a white dome (coolie hat) that has a four-inch circular hole in its center. This dome was used in the original system to hold a blower fan. This dome should be removed and the loose leads to the original blower motor should be insulated. Do not discard the dome, as it may be used as part of the new cooling system.

Defining a Locating System. From a top view the D-17B computer system may be described as a rectangular polygon with twelve sides, as shown in Figure 16. One half of this polygon consists of power supplies and the other half is the actual D-17B computer hardware. These two halves may be distinguished by the following features: the panels covering the power supplies are held in place by bolts with heads that are the shape of a 5/16"-12 point socket, panels covering the computer hardware are attached with screws that have Phillips-type heads (the screws are not true Phillips heads; they are best removed with an Ampex no. 212-8 screwdriver bit). In order to locate each section of the computer, the sections of the computer hardware side will be identified by a number from 1-6 in clockwise fashion. Similarly, the power supply half will be identified by the numbers 7-12 in clockwise fashion.

Using this system, the memory is located at the intersection of sections 1 and 2, and the 100-pin umbilical connector is at the intersection of sections 9 and 10.

Memory Desiccant. The clearances between moving parts of the D-17B memory are in the order of a few microns. To prevent moisture contamination, the memory has been equipped with a desiccating filter that is used when it is operated in the open atmosphere (originally the computer system operated in an inert gas atmosphere). This filter is a plastic circular cylinder approximately three-fourths inch in diameter and three inches long that screws into the front memory cover. The end of the filter may be covered with a plastic cap which should be removed during operation of the memory.

If the indicator paper strip inside the filter is pink, the filter should be replaced or the desiccant may be dried in an oven and re-used. If the filter is removed to dry the desiccant, the filter port in the memory should be taped to lessen the chances of moisture contamination.

Removal of Inertial Reference Platform. The missile guidance gyros were removed when the system was declassified. The remaining parts of the inertial reference platform may be removed, thus allowing full access to the inside of the toroid formed by the D-17B computer and power supply sections. The gyro assembly is electrically connected to the computer through three plugs, J-19, J-20, J-21, that are on the bottom of section 2 (section positions are described in the above paragraph). The plugs should be disconnected.

Viewing the inside of the computer from the top, one may observe three concentric rings of screws

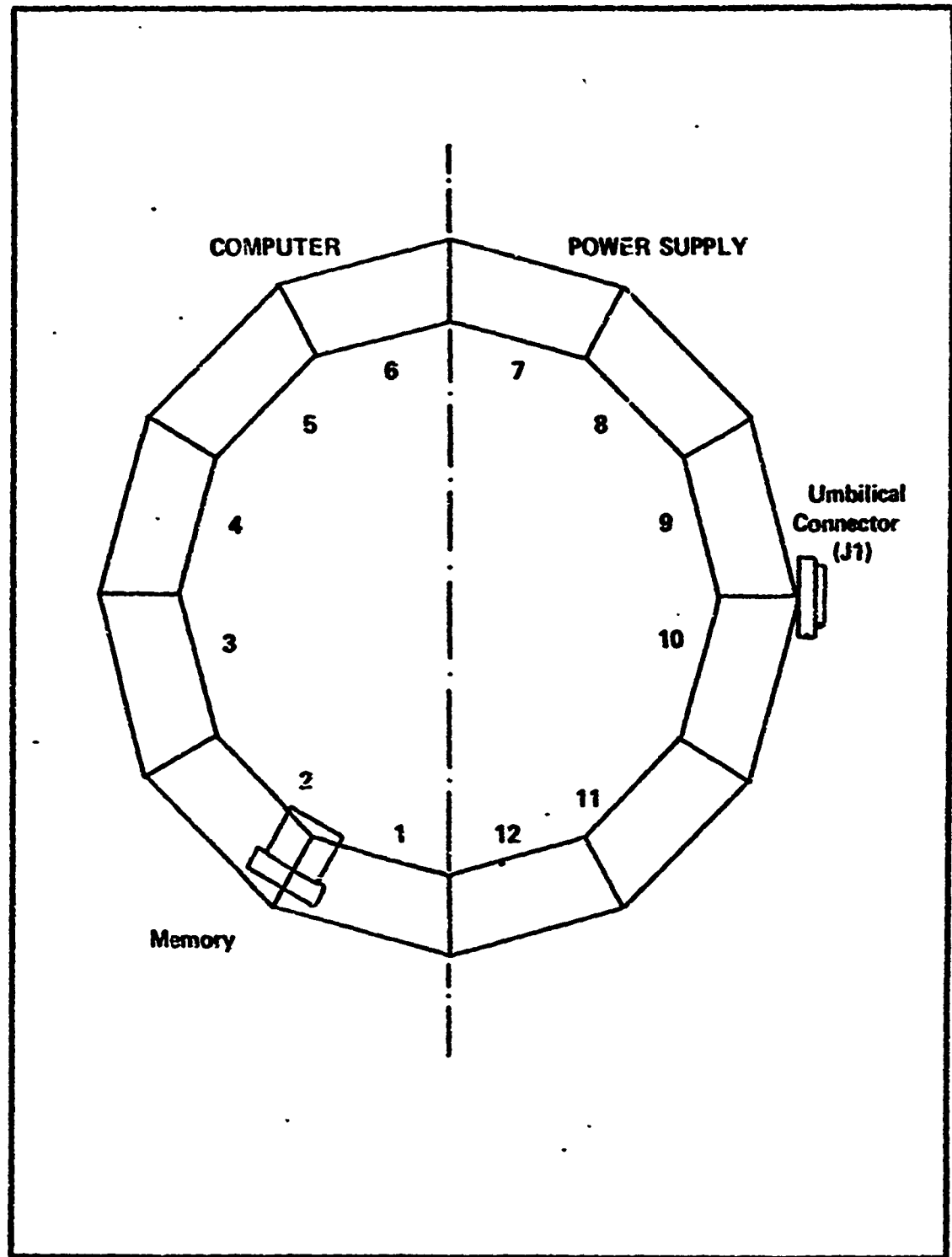


Fig. 16 Location system used in check out procedures for the D-1 B Computer.

on the computer base. The two outside rings attach a copper-colored heat exchanger to the computer base. The inside ring consists of eighteen screws that attach the inertial reference platform to the computer. These screws are slotted for an Ampex no. 212-8 screwdriver bit (if this tool is not available a Phillips screwdriver may be modified to fit the head). Remove the screws holding the inertial reference platform. Care should be taken to preclude damage to the inside of the computer when these screws are removed. Now the inertial reference platform may be lifted free of the computer base.

Once the inertial reference platform has been removed from the computer, the inside of the computer should be inspected for loose wires or foreign objects that may cause a short-circuit on the exposed circuit-board terminals.

Preparation of External Plug Connectors. It is advantageous at this point in the preparation process to disconnect and secure the external plugs that will be used for input/output and checkout of the computer. These plugs are J1, J2, J3, and J4. Plug J1 is the 100-pin umbilical connector located between sections 9 and 10. In the original system, computer failure was occasionally caused by twisting the wire bundle that is connected to plug J1; therefore, this plug should be secured with a sturdy bracket to the computer mounting base and the computer sides.

Plugs J2 and J4 are circular, approximately one inch in diameter, and are located at the intersection of sections 7 and 8. These plugs are mounted to the frame of the computer base facing downward. To facilitate access to the plug pins, the plugs may be detached from the base and carefully lifted free of the mounting holes.

Plug J3 is a 2.5 inch by 4 inch rectangular plug located on the underside of the computer frame. J3 may be easily located since the wire bundle connecting it to the computer wiring harness is formed directly below the main 100-pin umbilical connector, J1. The wire bundle associated with J3 should be tied to the underside of the computer so that the computer frame does not rest on the wires. J3 should be securely mounted for easy access (one possibility is suggested in the following section).

Conversion of Missile Section to a Computer Stand. The truncated cone-shaped missile section which originally housed the D-17B may be converted to a computer stand. This method offers the advantage of a hollow stand which will allow access to the underside of the computer base. Also plug J3 may be securely mounted in the inch hole in the side of the converted stand.

If the computer housing is to be used as a stand, turn it upside down (small end down). The holes around the larger end of the proposed stand must be reamed in a manner such that the 7/16-inch bolts may be inserted from the outside at a 10 degree downward angle from the horizontal. The computer may then be positioned in the stand and the 7/16 inch hex bolts that were stored during the uncrating process may be used to secure the computer to the new stand.

Initial Power on Checks

Power may be applied to the computer at this point in the conversion procedure to determine if the memory motor and power supplies are operable.

External Power Supply. Since an internal power supply is part of the navigational system, it is necessary only to supply 28 VDC from an external source to operate the D-17B. This source should be regulated and capable of supplying a 25 amp surge current and 19-20 amps continuously.

Power terminals for the computer are located on the computer mounting frame at section 12. The terminals are numbered E1, E2, E3, and E4 from left to right; thus, E1 is the nearest terminal to the computer memory.

Connect the power supply positive terminal to terminal E2 on the computer mounting frame and connect the negative terminal to E3 (Ref 2:4). (Use connecting wire capable of carrying 25 amps).

Initial Power Application. Power application to the computer system without cooling should be limited to short periods of two minutes or less. In all cases, once power has been turned off, it should remain off for at least 40 seconds. This procedure is recommended to insure that the memory disk has stopped turning prior to reapplication of power. If the disk is turning when power is applied, permanent damage may result (Ref 16:5-70).

The input current to the computer system should be monitored at least during the initial power check. This initial power check provides the opportunity to check the 28 v, 400 hz, 3-phase power supply which drives the memory motor. A convenient test point for the 400 hz supply is the fan leads on the upper part of the D-17B. These leads are easily located, since they are attached to the inner side of the computer at the intersection of sections 11 and 12. Figure 17 shows the wave form of one phase of this three-phase supply on an oscilloscope.

The other secondary direct current power supplies may be checked at this time. The test point locations, voltages, and tolerances are listed in Table II. To avoid damaging the system it is recommended that a meter with a high input impedance, such as an oscilloscope, be used to check these supplies.

When power is applied, the input current should rise quickly to 22-25 amps, then drop to 17-19 amps within five seconds. The hum of the 400 hz power supply should be audible and the sound of the memory motor starting may be heard. If the input current does not drop below 20 amps within five to ten seconds, the memory motor may not be turning. In this case, the windings of the memory motor will be drawing starting value current. If the memory is not turning and the 28 v, 400 hz power supply is operating, power should be removed from the system immediately. It is not recommended that any internal repairs be attempted to a memory without consulting qualified technicians.

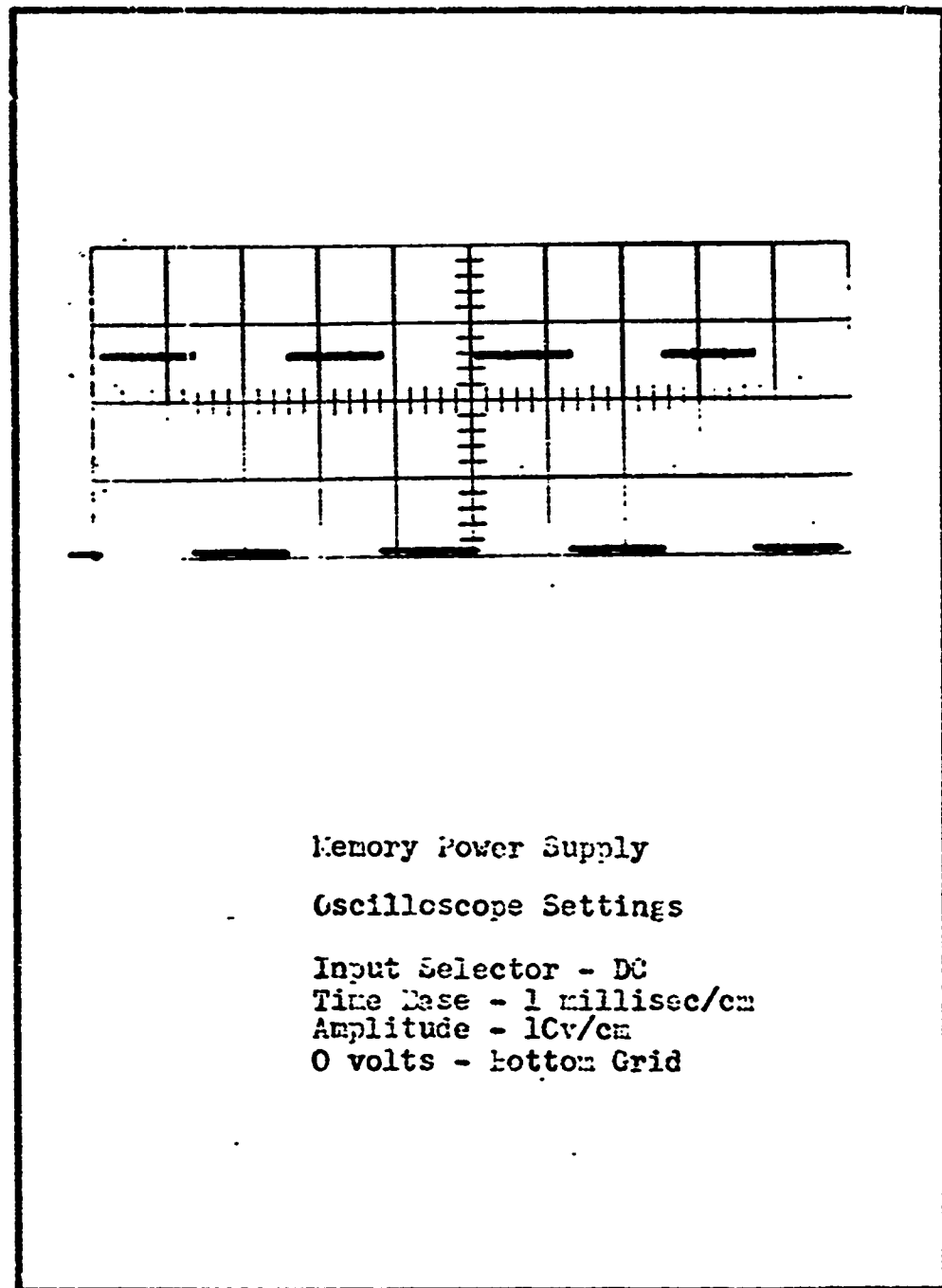


Fig. 17. D-17B Memory Power Supply Waveform.

Some memory repair and modification procedures are being prepared by the Minuteman Computer Users' Group. These procedures have not been tested on the computer at AFIT.

Preparation of Cooling System

The navigational system in the Minuteman missile was cooled using a closed circulating air system to cool most of the logic networks, power supplies and memory. A liquid coolant was circulated through the power supply and memory heat sinks and through the circular heat-exchanger on top of the supporting base. Therefore, the liquid coolant served two purposes: it removed heat energy from the enclosed navigational system and it partially cooled the memory and power supplies.

An exclusively air-cooled system is economically advantageous for utilizing the D-17B in the laboratory. The cooling system described in this report requires some minor modifications of the computer supporting base; however, it is constructed utilizing inexpensive fans and will allow continuous computer operation with ambient air temperatures of up to 85°F. (see Fig. 18). A 2 1/2-inch hole saw is the only special equipment used to modify the computer base.

Cooling System General Description. The cooling scheme of this system is to force ambient air through the computer from the top and from the lower side panel covering the memory (sections 1 and 2). Air forced into these two points will exhaust at the bottom of the computer and power supply. The computer base restricts the exhausting air flow, thus, holes must be cut in the base under the sections which require more cooling air.

Modification of Computer Base. Sections 2, 1, 12, and 11 contain the memory and power supplies and require more cooling than the other sections. Exhaust ports should be cut under these sections using the procedures described below.

There are seven main supporting beams on the computer base between the left side of section 2 and the right side of section 11. For descriptive purposes in this topic only, these seven supporting beams will be designated with the letters A through G. Thus, beam A is at the intersection of sections 2 and 3 and beam G is at the intersection of sections 10 and 11, as shown in Fig. 19.

Using a 2 1/2-inch hole saw, cut holes in the side of the computer mounting frame between beams A and B, B and C, C and D (see Fig. 19). These three holes are in the side of the mounting frame directly in front of the memory. Continuously vacuum the filings from this cutting process to prevent them from shorting the electrical components.

From the underside, cut two holes 2 1/2-inches in diameter between each beam A through G. Thus, there will be twelve holes in the bottom of the mounting base: two holes radially aligned between each of the seven beams. Under sections 11 and 12 there is a magnesium supporting brace which may

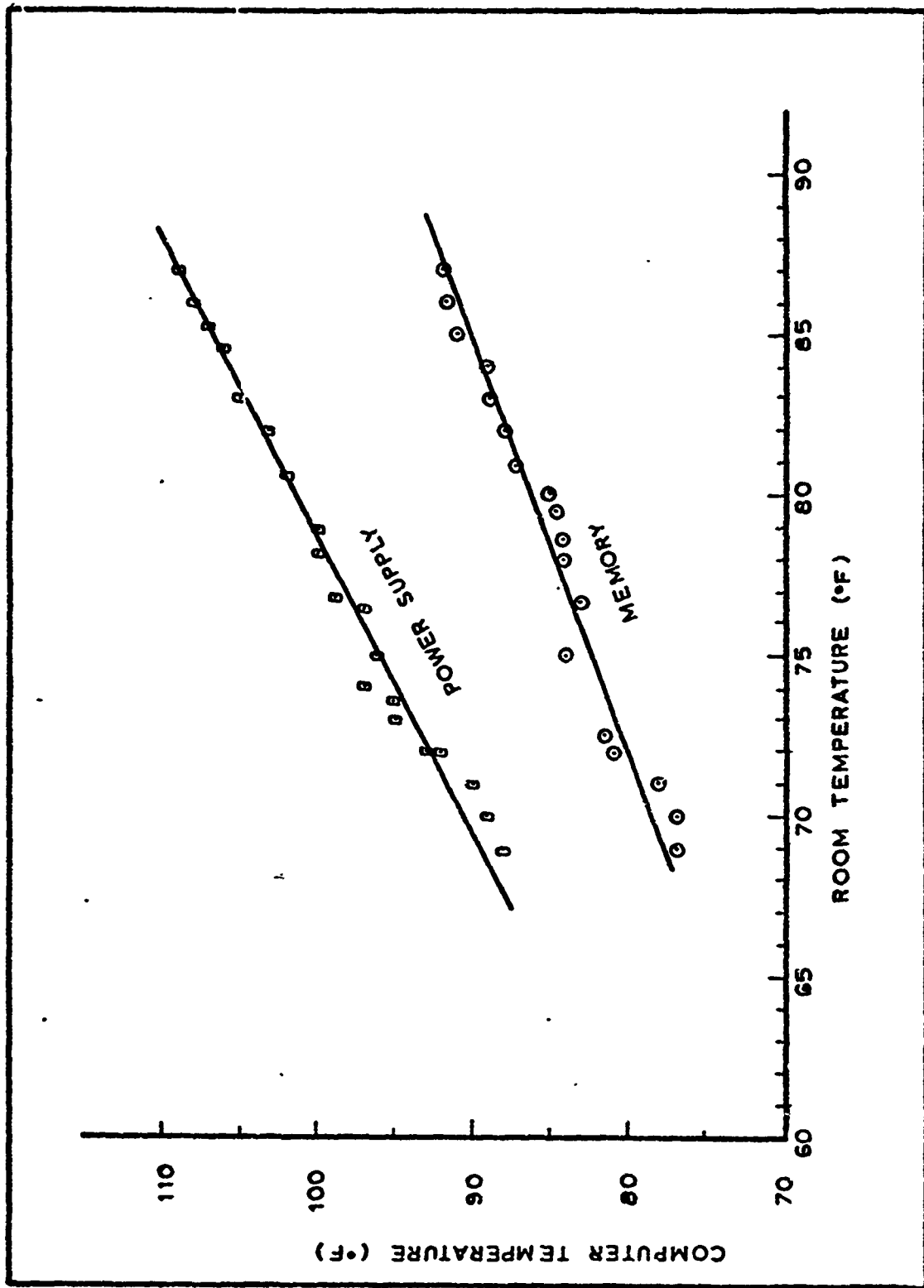


Fig. 18 D-17B Computer temperature vs. Ambient Air Temperature.

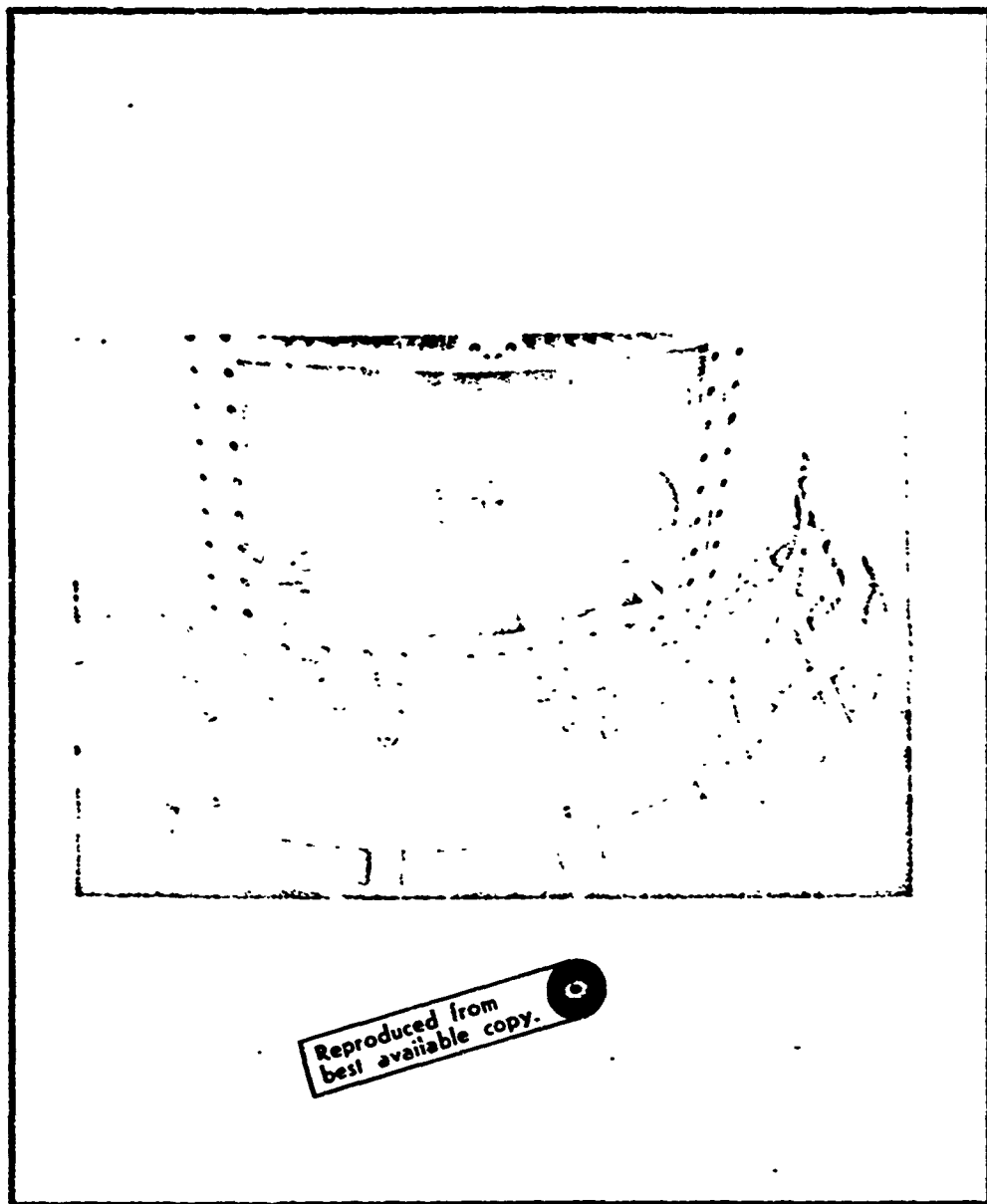


Fig. 19. Air Exhaust Modifications on D-17B
Computer Supporting Frame.

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hinder the hole cutting process. This brace may be pulled free of the computer base using vice-grip pliers.

Memory-blowers. The side panel covering sections 1 and 2 is divided into two parts. The top half covers the memory read and write amplifiers and the bottom half covers the memory. The densely packed components in the read and write amplifier section prevent sufficient cooling air from reaching the memory from the top of the computer. To alleviate the problem the bottom half of the side panel should be replaced with a metal cover and a blower should be installed on each side of the memory. These fans should have an output of at least 35 cubic feet per minute at zero inches of water static pressure. Since the memory is the single critical part of the D-17B, it was decided to use two fans for added protection and to prevent dead air flow spots on the memory cooling fins.

Main Blower Fan. A manifold was used to direct cooling air into each section of the D-17B when maintenance was performed on the original system. The use of a manifold was abandoned in this project because manifolds are expensive to construct and require fans capable of high output pressure. A system which allowed the use of a standard fan which is normally used to cool electronic equipment racks was chosen.

To implement this system it is necessary to cover the top of the computer without covering the inlets to sections that house the electrical components. The white dome (coolie hat) which initially covered the computer top may be used for this purpose. Cover the 3 3/4-inch hole on this dome and place it upside-down (concave side up) on the computer top. Using this arrangement, the dome sits in the cavity formed by the computer and power supply and prevents air from flowing into this cavity.

The next step is to construct a collar to fit around the outside of the twelve-sided polygon formed by the computer and power supply sections. This collar should be at least 6 inches high and may be secured to the computer system using the screws that attach the top of the panels which cover each of the computer sections as shown in Fig. 20.

The final step is to construct a top cover for the computer system that will support the top blower fan. A number of different fans may be used. The fan shown in Fig. 20 is a fan that was originally used to cool an electronic equipment rack. Publications from the Minuteman Computer Users' Group have suggested the use of two 6-inch fans in this top (Ref 12:20). A system of this type, as shown in Fig. 21, was found to be preferable because of the lower noise level. The fans that are used should be capable of an output of at least 350 cubic feet per minute at 0 inches backpressure.

The temperature data and specifications provided in this report came from two separate computer systems and the cooling characteristics were nearly identical. However, since there is a possibility that other cooling systems may be constructed differently than the one described or the cooling characteristics

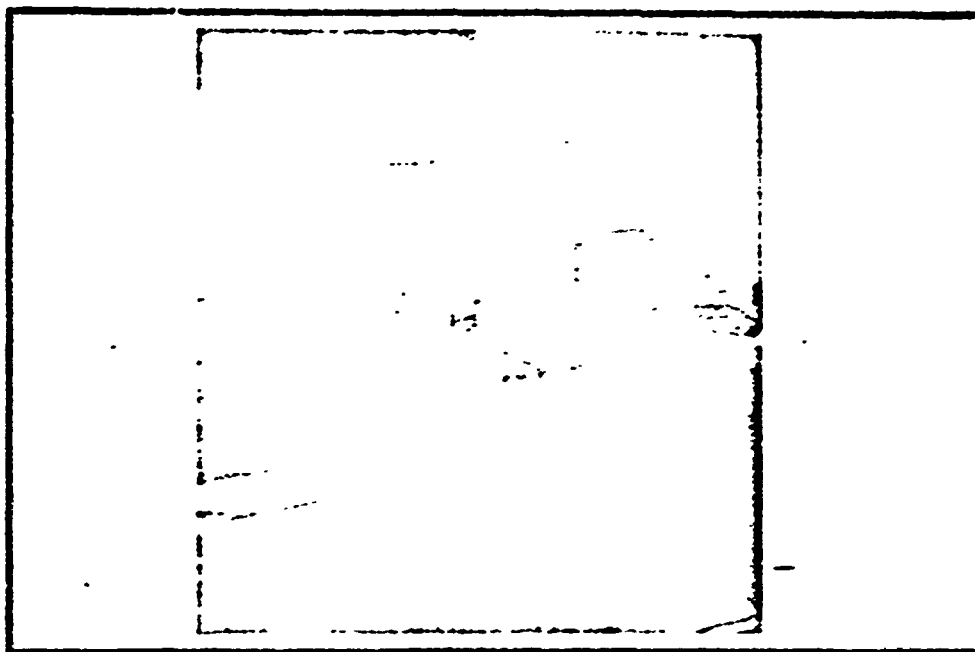


Fig. 20. D-173 Cooling System Using Electronic Equipment Rack Blower.

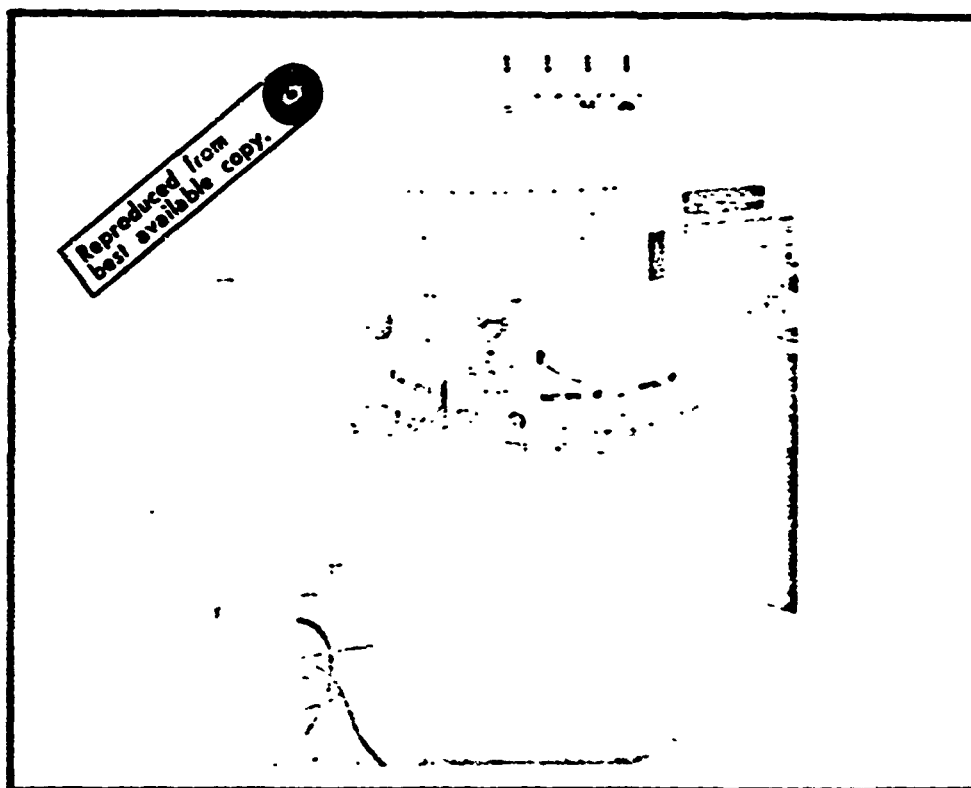


Fig. 21. D-173 Cooling System Using Two 6-inch Fans.

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of different computers may vary, it is recommended that the memory and power supply temperatures be monitored. A temperature sensing device which may be used for this purpose is shown in Appendix II. This circuit also includes a scheme for monitoring the external 28 VDC power supply.

The memory test point is the side cooling fins and the power supply test point is the heat sink associated with power transistor Q1 on power supply board A-19. This heat sink is located in the center of section 12.

Computer Checkout

Once power has been applied to the D-17B and a cooling system has been developed, checks may be made to determine the status of the logic networks. The checks that are described in this section are divided into two parts: first, tests that require no control panel are discussed; then, a more extended check which requires control and data entry capability is considered. Construction of a control panel and input output devices is covered in AFIT theses GE/EE/72-3 and GE/EE/72; that effort will not be duplicated in this report.

Waveshapes shown in this section were photographed from an operable computer using an oscilloscope with a shielded input cable. An isolation transformer should be used in the oscilloscope power cable to prevent accidentally shorting the D-17B circuits through the ground lead of the scope.

Test point locations are included in Appendix B and are listed alphabetically by functional designation. For example, the system clock is listed under the function "clock" and one suitable test point is plug J3, pin 47.

Tests Using No Control Panel.

When power is applied to the computer the controlling flip-flops will be activated in a random state (a more complete discussion of states is given in "State Description") and the logic networks are not synchronized with the rotating disk memory. Even though the machine is operating in this undefined state, some indication of its operational status may be determined.

System Clock Waveforms. The system clock may be observed as shown in Fig. 22. The existence of the clock signal indicates that the memory is turning and that information can be read from it. If the clock frequency is 345.6 kHz the memory is turning at the required 6000 revolutions per min.

The clock pulse should have the following specification: True level is $-10.7 \pm 1v$; false level measured on the flat portion of the waveform is $-1.8 \pm 0.4v$. At a -3 volt level the pulse width should be 0.52 ± 0.07 micro-seconds and the overshoot above the 0 volt level should be less than 0.1 micro-seconds wide and less than 1.9v (Ref 16:5-11, 5-12).

Tests Using a Control Panel. More conclusions about the computer's operational status may be made after a control panel has been constructed. A master reset signal, M_r , causes the computer to

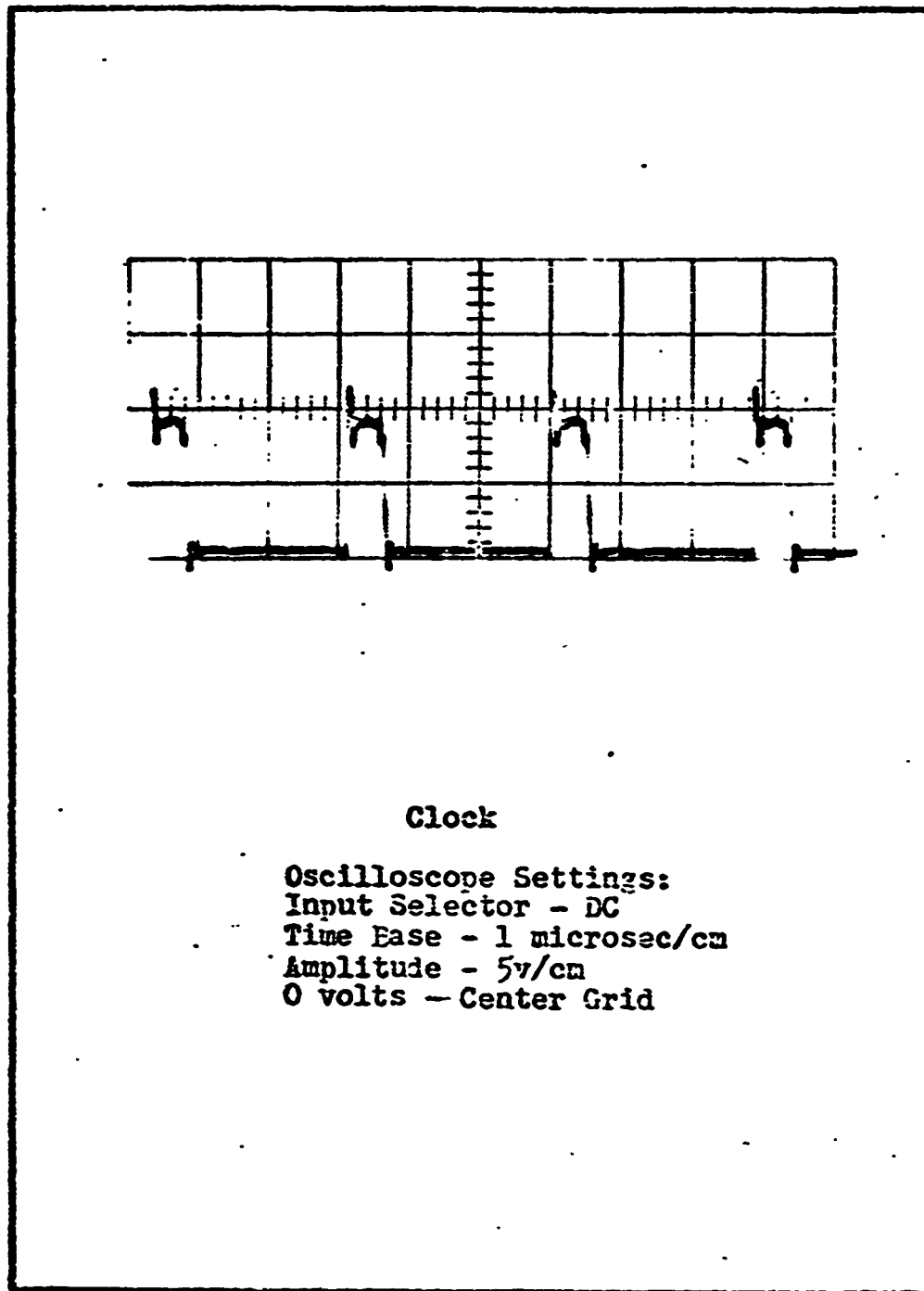


Fig. 22. D-17B System Clock Waveform.

enter a defined state and synchronization of the computer timing circuits and the rotating memory occurs. (A more detailed explanation of this action is covered in the State Description of the machine).

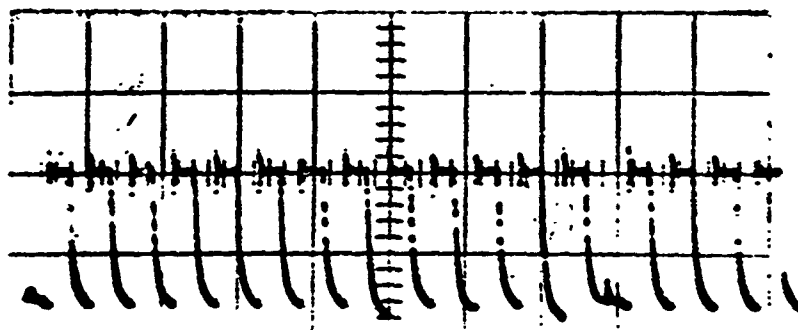
Bit Counter Waveforms. Proper response from the Bit Counter flip-flops, B_1 through B_6 , indicates that synchronization between the rotating disk memory and the bit counter circuits has occurred. These responses are shown in Fig. 5, and output waveforms for B_1 and B_6 are shown in Fig. 23 and Fig. 24. "True" level of the signals is -8 to -10 volts and "false" is 0 volts. Since B_6 is "false" or 0 volts during the first half of the 78.12 microsecond word time, it may be used as an external synchronizing pulse for the oscilloscope to establish a time reference for observing the other waveforms.

Timing Flip-flop Waveforms. The states of the bit counter flip-flops determine the states of the timing flip-flops, T_0 , T_X , and T_p . The output waveforms of these flip-flops are similar; therefore, only T_p is shown in Fig. 25. Note that the "true" level, -10v, occurs every 78.12 microseconds (one word time).

Loop Waveforms. The contents of the loops may be observed by monitoring one flip-flop in the loop. For example, the L register is shown in Fig. 26. This figure was obtained by monitoring the L_X flip-flop and shows a "true" pulse for bit position L_X , L_1 , and L_4 . Using this procedure, the contents of any register may be displayed and further testing of the machine is limited only by the capability of the control console to enter commands in the computer.

Summary

Care should be exercised when uncrating and testing the D-17B computer. Since a power supply is part of the NSQ-10 navigational system, only a 28 VDC external power source is needed to operate the computer. Some preliminary tests may be made without a cooling system to insure that the computer is operable. An inexpensive forced-air cooling system may be constructed from common laboratory cooling fans. After a cooling system is constructed, more detailed testing may be conducted by observing the signal waveshape of the clock, accumulator, and timing pulses.

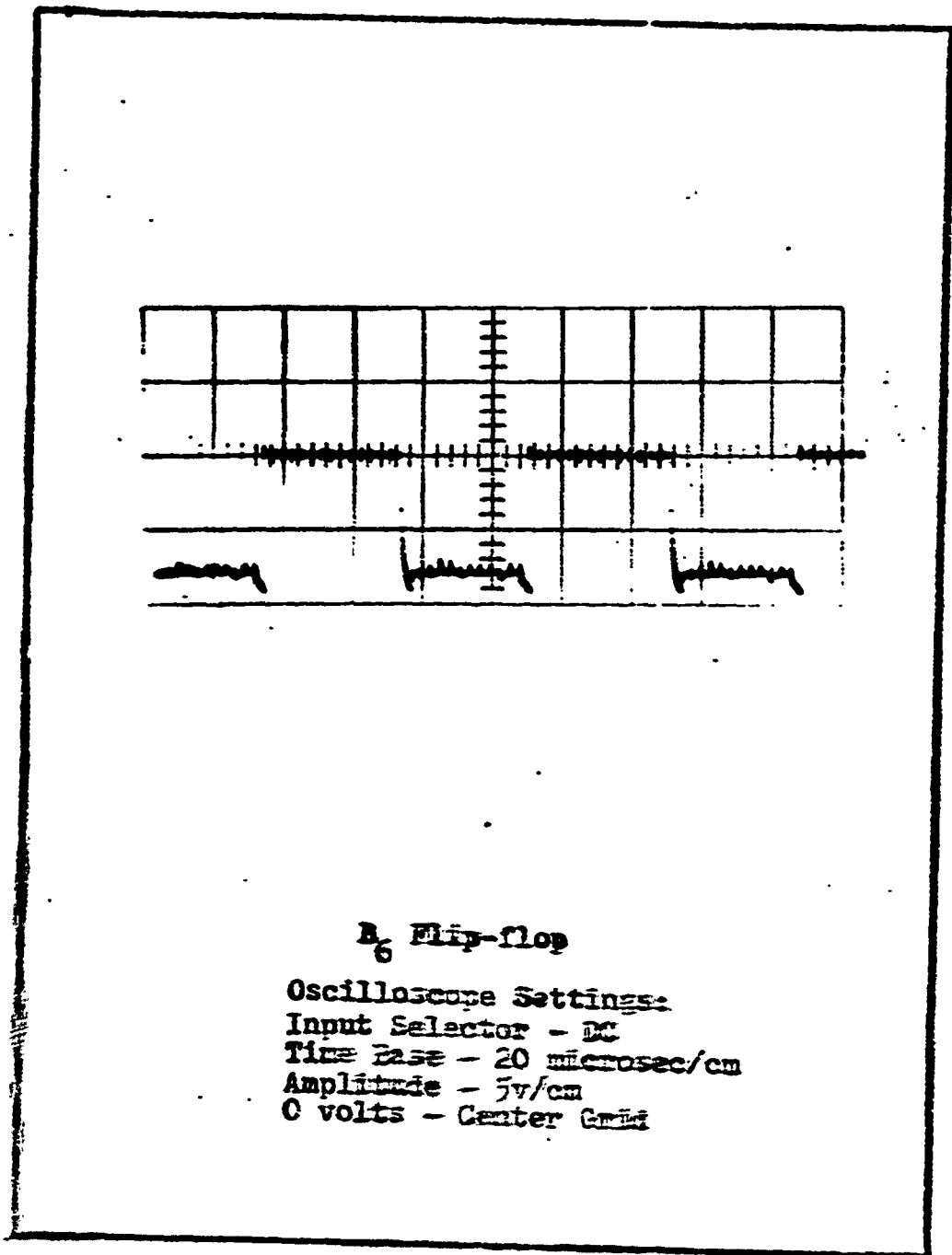


B_1 Flip-Flop

Oscilloscope Settings:
Input Selector - DC
Time Base - 10 microsec
Amplitude - 5v/cm
0 volts - Center Grid

Fig. 23. D-17B Bit Counter, B_1 , Waveform.

(0)



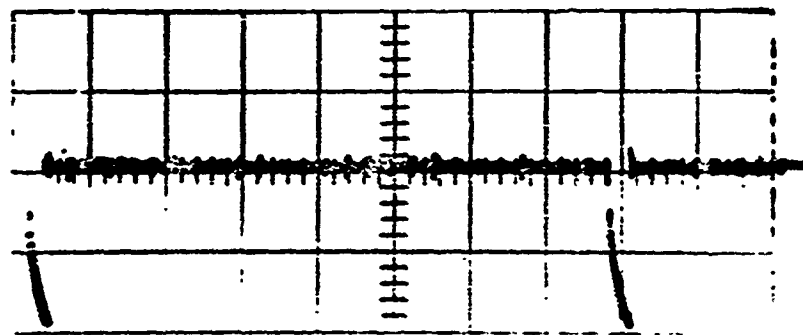
B₆ Flip-flop

Oscilloscope Settings:
Input Selector - DC
Time Base - 20 microsec/cm
Amplitude - 5v/cm
0 volts - Center Grid

Fig. 24. D-173 Bit Counter, B₆ Waveform.

(0)

(0)



Timing Pulse T_p

Oscilloscope Settings:
Input Selector - DC
Time Base - 10 microsec/cm
Amplitude - .5v/cm
0 volts - center grid

Fig. 25. D-17B Timing Pulse, T_p , Waveform.

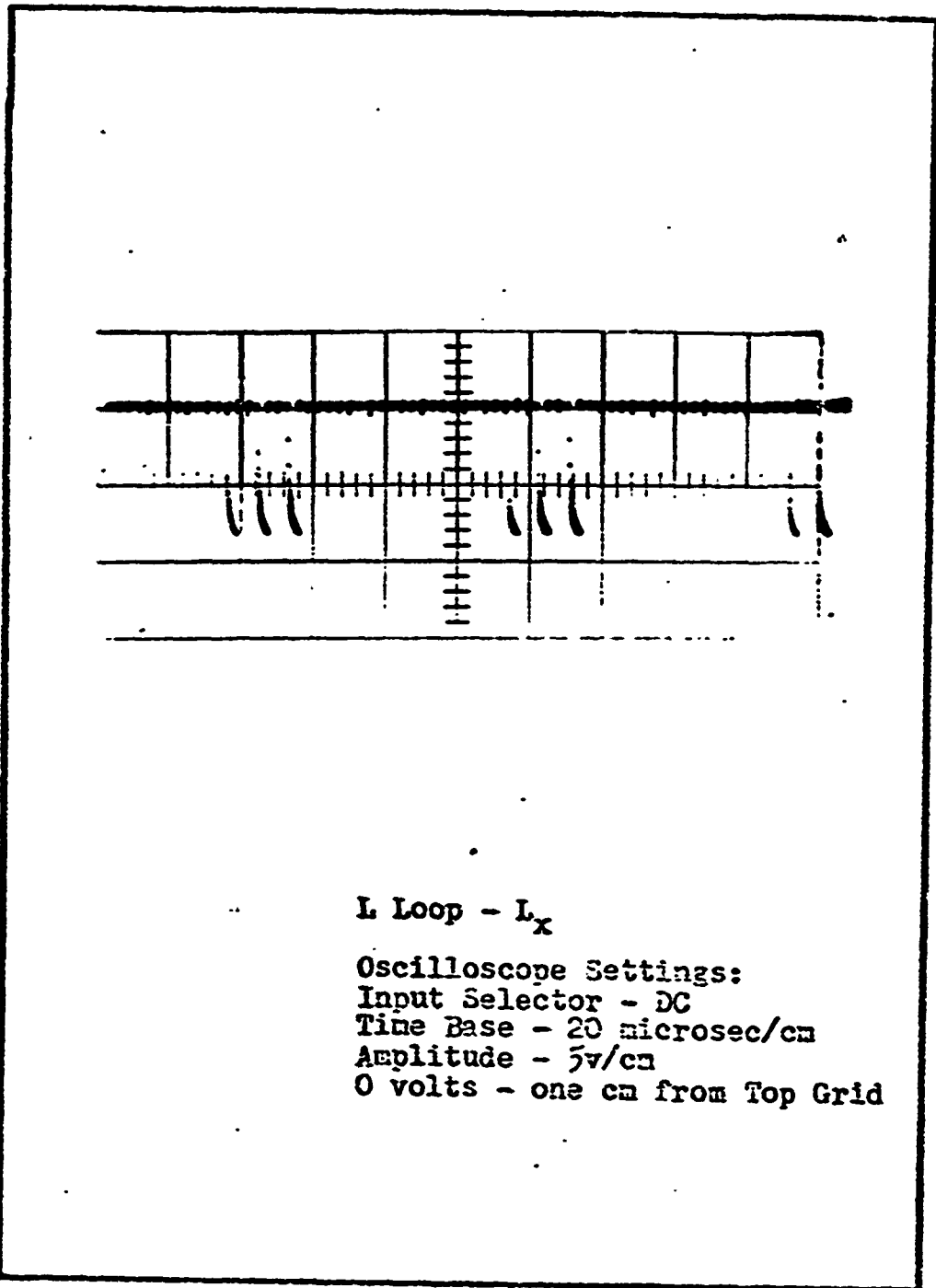


Fig. 26. L_x Flip-flop Output Waveform.

IV. Applications of the D-17B Computer

Applications for any minicomputer are widely varied and determined in detail by the specific user. The D-17B computer applications are presently limited by the size of the memory, speed of execution and lack of software programs. These undesirable features are offset by the fact that the computer is inexpensive, has built-in digital-to-analog converters, and two sets of discrete input lines. Thus, the D-17B is best suited for fixed tasks (and not general purpose computing) where its capabilities can be used to full advantage (Ref 6.35).

In this section some general applications will be presented. These techniques will provide a starting point for more specific applications by future users of the computer.

General Purpose Input Bus System

The discrete inputs may be used to input data from a peripheral bus system. A conceptual block diagram of such a system is shown in Fig. 27. This system uses the discrete Y inputs to input data bits directly into the Accumulator under program control. Obviously, the system could easily be extended to as many as 24 input data bits. An X discrete input is used as a flag line to indicate peripheral ready status and discreted output lines are used to control the peripherals.

Educational Uses of the D-17B

A control panel such as the system described in Ref 8 converts the D-17B into an excellent "hands on" educational computer. This system allows the student to observe the states of computer registers and information transfers between the registers. The contents of memory may be displayed with this system and machine language programming may be taught without the "turn-around time" obstacles that are involved with larger data processing systems.

The input bus system described above may be used as an educational tool by allowing the students to breadboard peripherals and input data to exercise software programs.

Laboratory Uses of the D-17B

In the laboratory, an analog-to-digital converter is a useful input device. One suggested approach for this addition is to use the A/D converters as one of the peripherals of the data bus system described above (Ref 13). This suggestion has merit since the A/D converter could be disconnected easily from the computer for temporary use with other laboratory projects.

Once the ability to input analog data has been achieved, many applications as a laboratory control system become apparent. Even without analog input capability the system may be used as an open-loop control system. Analog inputs present one convenient way to use the D-17B in a closed-loop control system. As a closed-loop digital control system, the D-17B can be employed in processes such as numerical

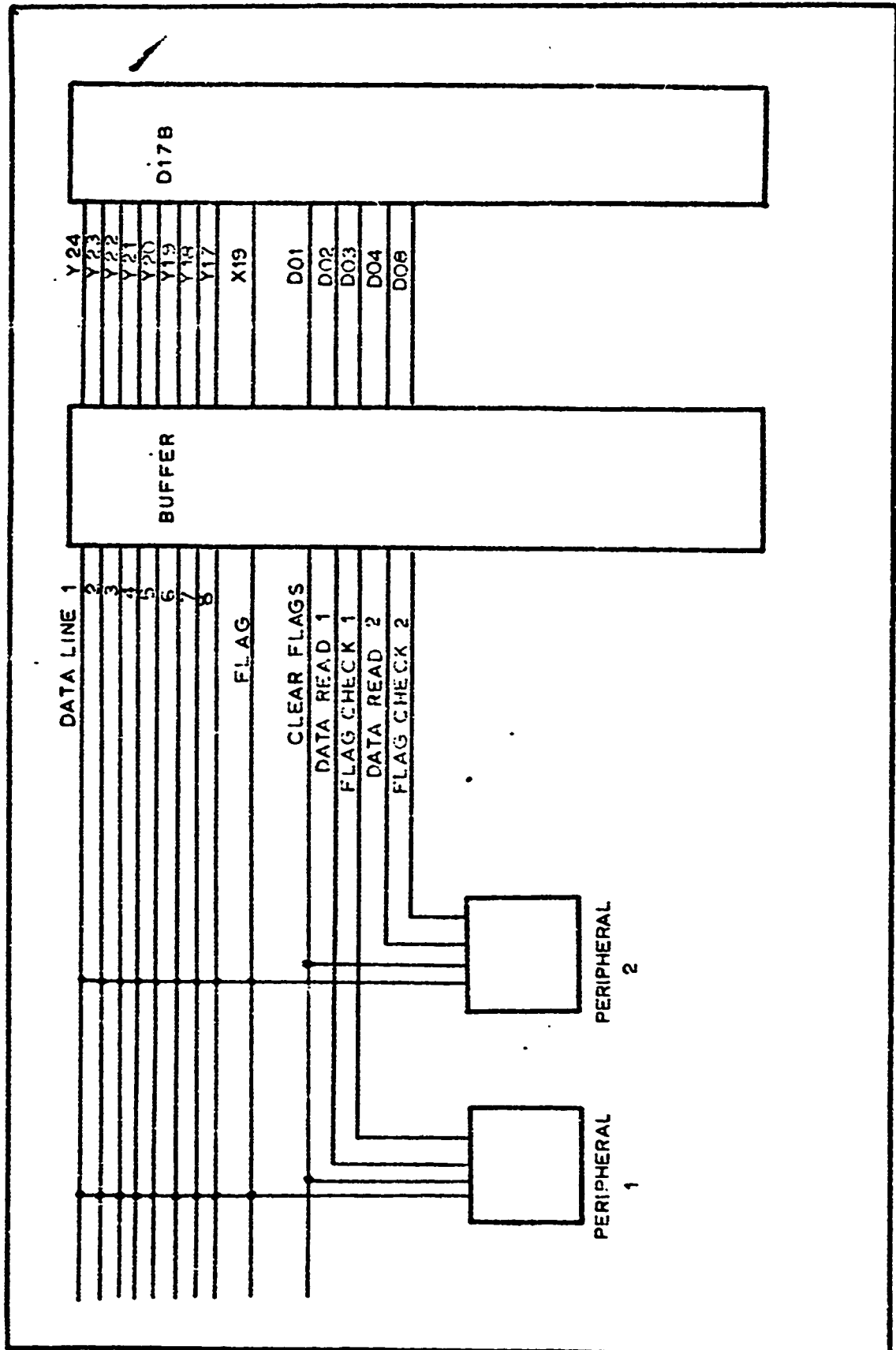


Fig. 27 D-17B Input Bus Block Diagram (Adapted from Ref 13 : III-1).

control, process monitoring, and electronic component testing (Ref 3:40). Certainly these applications are limited by the speed of the D-17B input operation (approximately 78 micro seconds). However, one must consider that the system proposed in Ref 8 allows for the simultaneous input of two 12-bit A/D converters of three 8-bit converters.

Data Collection Capabilities of the D-17B

Several D-17B computers may be used with peripherals such as an A/D converter to perform dedicated tasks such as data collection. Used in this way the limitations of the D-17B may be circumvented for the following reasons:

- 1) a system of several computers has an advantage for data collection in remote locations since a failure of one system would not result in a total loss (Ref 7:36).
- 2) Since the D-17B would be performing a dedicated task such as collecting a single type of data, its effective computing speed would be comparable to a more general purpose machine. That is, much of the speed of faster general purpose machines is lost in "housekeeping" tasks and the D-17B instruction repertory is suited for this type of operation (Ref 7:36). As an example, the D-17B can collect new data and store the previous data input with a single flag store operation. Also the character output instruction is ideal for unpacking data since four bits of the accumulator can be output with one instruction (Ref 7:36).
- 3) Using several computers helps overcome the small memory limitations of the D-17B.
- 4) Such a system would be inexpensive because A/D converters that are compatible with the D-17B computing speed are available for less than fifty dollars (Ref 13).

Summary

The D-17B is capable of a wide variety of applications. The user must apply the computer as a dedicated machine to make up for its relatively slow speed, small memory, and present lack of hardware. These limitations are offset because the system is inexpensive, dependable, and has an instruction set which is designed for special applications. (Ref 7:35).

The number of applications can be greatly enhanced by adding a general purpose input bus to the computer. This bus system used in conjunction with inexpensive A/D converters tailors the D-17B for uses in educational, laboratory, and data collection applications.

Conclusions and Recommendations

The D-17B computer is a sturdy, reliable minicomputer; however, it can be damaged as the result of an improper installation. Since the computer and a power supply are attached to a rigid base, it is recommended that the system be reconfigured as little as possible. If the associated navigational system power supply is utilized, only a 28vDC power supply is needed for D-17B operation. An inexpensive forced-air cooling system can be constructed that is suitable for operation at ambient temperatures up to 85°F. During the course of this study it was found that this cooling system plan requires only minor modifications to the computer base and is the best approach for cooling the computer at normal room temperatures.

Documentation concerning the software and applications represents a task for future endeavors. This report provides a state description of the machine that should be useful for maintenance as well as a systematic approach for studying the machine. Other documentation is being provided by the Minuteman Computer Users' Group (Ref:5,6,7,12).

A complete buffered interface system would greatly aid efforts toward future applications of the computer. If the system clock, bit counter flips and all discrete lines were buffered and made available on a patch panel, experiments with other hardware devices could more easily be carried out.

Some of these experiments might entail connecting the D-17B to a TR-48 analog computer for a "mini-hybrid-computer" operation. Initial experiments along this line could suggest using the D-17B analog outputs to generate a programmed function waveform.

Any number of proposals might be suggested; however, they would simply be a reiteration of minicomputer application that are available on commercial machines. From the experience of this project it would seem that a complete buffered interface would be the key to all these applications within the bounds of the speed restriction and memory capacity of the D-17B.

Bibliography

1. Autonetics. EM2817. Anaheim, California: Autonetics, Division of North American Rockwell, Inc.
2. Autonetics. Minuteman D-17 Computer Training Data. Anaheim, California: Autonetics, Division of North American Rockwell, Inc. 8 June 1970.
3. Autonetics. Part I Preliminary Maintenance Manual of the Minuteman D-17A Computer and Associated Test Equipment. P.O. Memo 71. Anaheim, California: Autonetics, Division of North American Rockwell, Inc., January 1960.
4. Bartee, Thomas C. ; Lebrow, Irving L.; and Reed, Irving S. Theory and Design of Digital Machines. New York: McGraw Hill Inc., 1962.
5. Beck, C.H. Minuteman Computer Users' Group D-17B Computer Documentation, MCUG-4-71. New Orleans, Louisiana: Tulane University, April 1971.
6. Beck, C.H. Minuteman Computer Users' Group D-17B Computer Documentation, D-17B Computer Programming Manual, Report MCUG-4-71. New Orleans, Louisiana: Tulane University, September 1971.
7. Beck, C.H. Proceedings of the Second Meeting of the Minuteman Computer Users' Group. Systems Laboratory Report No. TSL-3-71. New Orleans, Louisiana: Tulane University 16 Nov 1970.
8. Brady, R.C. and Husky, C.D. Design and Fabrication of a Control Console for the Minuteman I D-17B Computer. GE/EE/72-3. Unpublished Thesis. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March 1972.
9. Chatterton, B. Software Simulation of the D-17B Minuteman Computer. GE/EE/72-7. Unpublished Thesis. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March 1972.
10. Chu, Yaohan. Digital Computer Design Fundamentals. New York: McGraw Hill Inc., 1962.
11. Hansen, D.D. and Watkins, K.R. A Rigorous Logical Study-With Lab-of the D-17 Digital Computer. ACC-31170P-33 Anaheim, California: Computer and Data Systems Dept. of Autonetics Division of North American Rockwell Inc., 30 April 1962.
12. Minuteman Computer Users' Group. Proceedings of the Third Meeting of the Minuteman Computer Users' Group. Report MCUG-3-71. New Orleans, Louisiana: Tulane University, 19-20 July 1971.
13. Schaff, Robert M.; Chatterton, B.; and Allen, Douglas J. Design of Minuteman Computer Peripheral Interface. Unpublished Report. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March 1972.
14. Schaff, Robert M. Development of Input/Output Interface for the D-17B Computer. GE/EE/72-21. Unpublished Thesis. Wright-Patterson Air Force Base, Ohio: Air Force Institute of Technology, March 1972.
15. Shoryer, L.O. D-17A Computer Manual. Anaheim, California: Autonetics, Division of North American Rockwell, Inc., 1 Jul 1960.

16. USAF Technical Order. Technical Manual Overhaul and Repair General Purpose Computer (Model D-17B), T.O. 11G2-10-5-3-5. Los Angeles, California: Air Force Keir Lithographic, 24 November 1964.
17. USAF Technical Order. Technical Manual Overhaul Digital Computer Magnetic Memory, T.O. 11G2-10-5-3-6. 10 June 1964.

Appendix A

List of Terms and Abbreviations

- A_k** : Carry, borrow and misc. flip-flop.
A_p : "A" register extra delay flip-flop.
A_x : "A" register read flip-flop.
A₂₄ : "A" register delay flip-flop.
A_{23w} : "A" register write flip-flop.
B₆, B₅, B₄, B₃, B₂, B₁ : Bit time counter flip-flops.
C_{b5}, C_{b4}, C_{b3}, C_{b2}, C_{b1} : Operand channel buffer register and word time counter flip-flops.
C_{p5}, C_{p4}, C_{p3}, C_{p2}, C_{p1} : Program channel register.
C₅, C₄, C₃, C₂, C₁ : Operand channel storage register and auxiliary operation-code storage register.
D-17B : Designation of the computer used for guidance in the Minuteman I missile.
D_c : Shift control for "Discrete Output" register.
D_{dc} : Discrete disable signal from a control panel to control the discrete outputs.
D_f : Gyro malfunction indicator flip-flop.
D₅, D₄, D₃, D₂, D₁ : "Discrete Output" register.
D : Control flip-flop.
E : Control flip-flop.
E_{inx} : "E" loop intermediate read flip-flop.
E_x : "E" loop end read flip-flop.
E_p : "E" loop write flip-flop.
E_{wc} : Enable write signal - from a control panel - enables "cold storage" write heads in memory.
F_c : Fine-countdown-mode indicator flip-flop.
F_p : "F" loop write flip-flop.
F_s : Also F_{xc} in some writings - signal from a control panel that directs the computer to enter the prepare to fill state.
F_x : "F" loop read flip-flop.
G₃, G₂, G₁ : Binary Outputs flip-flops.
H_p : "H" loop write flip-flop.
H_{inx} : "H" loop intermediate read flip-flop.
H_x : "H" loop end read flip-flop.
I_c : "I" register interrupt control flip-flop.

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- I_d : "Instruction Search" sector disagreement indicator flip-flop.
- I_i : Also I_{ic} , the i th signal input to the computer from an external source for character input.
 $i = 1, \dots, 5$.
- I_{mc} : Symbol for a mechanical input signal to the computer, command to enter the Wait State.
- I_p : "I" register extra delay flip-flop.
- I_x : "I" register read flip-flop.
- I_{24w} : "I" register write flip-flop.
- J : Control flip-flop.
- K : Control flip-flop.
- K'_{hc} : Halt not or run signal from a control console - directs the computer to enter the compute states.
- K'_{kr} : Run not or halt signal from a control console - directs the computer to enter the Non-Compute states.
- L_c : "L" register interrupt control flip-flops.
- L_C : "L" register delay flip-flop.
- L_p : "L" register extra delay flip-flop.
- L_x : "L" register read flip-flop.
- L_{24w} : "L" register write flip-flop.
- M_{px} : Memory output buffer flip-flop.
- M'_{rc} : Also M_r - master reset signal from a control console, initiates the computer to the Prepare to Operate state.
- N_c : "N" register interrupt control flip-flop.
- N_d : "Number Search" sector disagreement flip-flop.
- N_p : "N" register extra delay flip-flop.
- N_x : "N" register read flip-flop.
- N_{24w} : "N" register write flip-flop.
- O_{b3}, O_{b2}, O_{b1} : Operation-Code-Buffer register.
- O_4, O_3, O_2, O_1 : Operation-code-storage register.
- P_3, P_2, P_1 : Phase register.
- Q : Special timing flip-flop
- R_c : "R" loop interrupt control and mode control flip-flop.
- R_p : "R" loop write flip-flop.
- R_x : "R" loop read flip-flop.
- S : Information read from the sector track of the D-17B computer memory.
- S_{b3}, S_{b2}, S_{b1} : "Flag-Code" buffer register.

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S_3, S_2, S_1 : "Flag-Code" storage register.

T_c : Sprocket timing signal; used to direct the computer to accept character inputs.

T_i : Bit times of the computer, $i = 1, \dots, 24$.

T_0 : "To Time" indicator flip-flop.

T_p : " T_p Time" indicator flip-flop.

T_x : " T_x Time" indicator flip-flop.

U_p : "U" loop write flip-flop.

U_x : "U" loop read flip-flop.

V_c : "V" loop interrupt control and state control flip-flop.

V_p : "V" loop write flip-flop.

V_x : "V" loop read flip-flop.

$V_{38}, V_{37}, \dots, V_{31}$: Voltage output register number 3.

$V_{28}, V_{27}, \dots, V_{21}$: Voltage output register number 2.

$V_{18}, V_{17}, \dots, V_{11}$: Voltage output register number 1.

$0A_1$: Symbolizes that the flip-flop named A_1 is set to a logical "zero" condition or "zero set".

$1A_1$: Symbolizes that the flip-flop named A_1 is set to a logical "one" condition or "one set".

A_1^* : The star or asterisk indicates an external signal to the computer that has been changed in voltage level but has the same logical meaning as the symbol with no asterisk.

A' : Prime is used to indicate a logical "not" when A is a logical 1, A' is a logical 0.

Flip-flop names and some definitions in this list were taken from Ref 1:110-114.

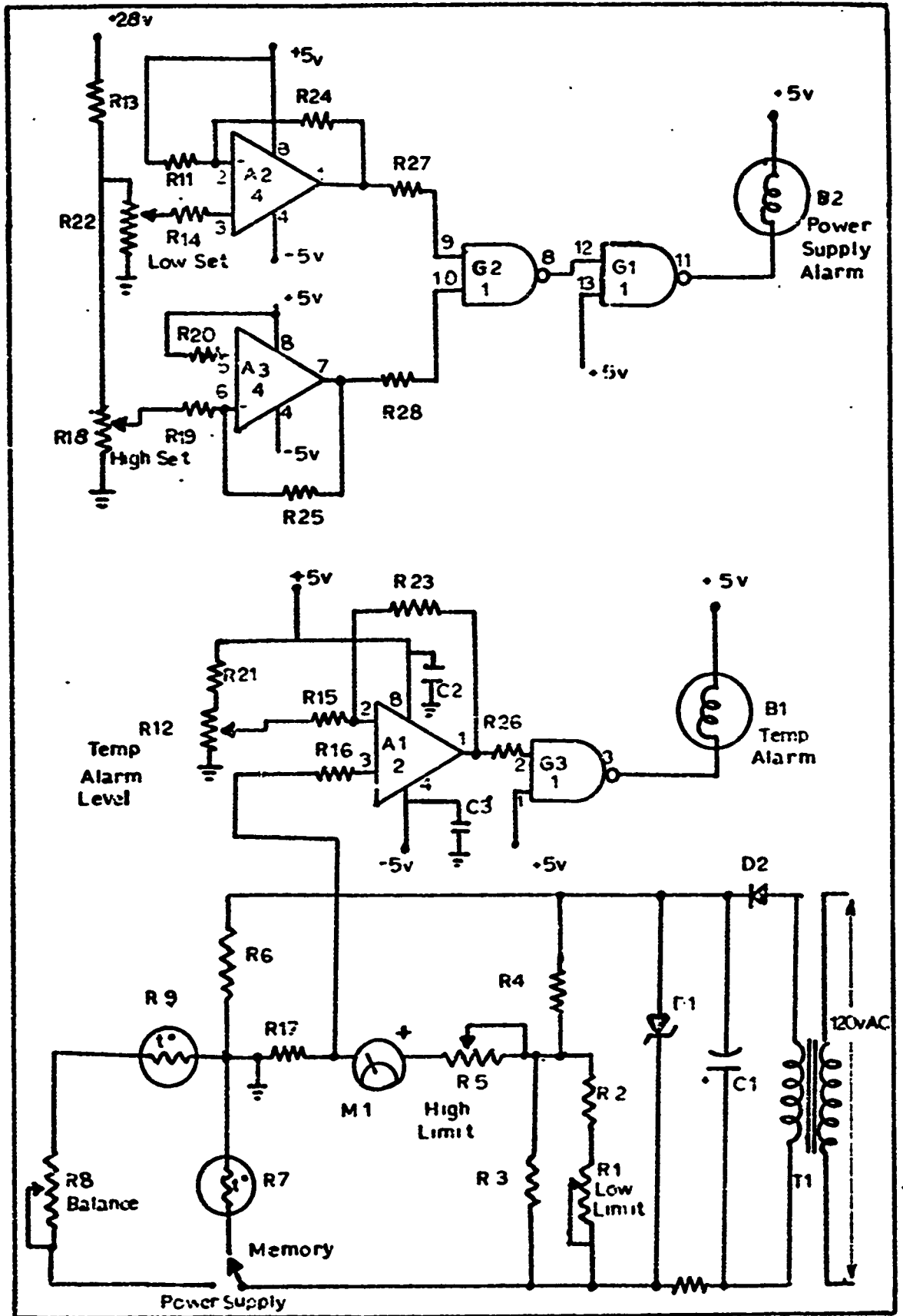


Fig. 28 Temperature Sensing equipment

Appendix B

Construction and Calibration of Temperature Sensing Equipment

The temperature sensing device shown here is a modification of a circuit from Popular Electronics magazine, October 1969. In addition, two alarm circuits have been added; one is used to monitor the 28v power supply output and the other alarm is used to monitor the computer temperature. A wiring diagram is provided in Fig. 28 and a parts list is provided on page 9:

Calibration

Temperature. The temperature sensing unit may be calibrated by using the following procedures:

- (1) Adjust the Balance potentiometer, R8, until the temperature readings are the same when the Selector switch, S1, is in either the "Memory" or "Power Supply" position.
- (2) Adjust the "Low Temp" potentiometer R1 until the present room temperature is indicated on the meter, M1.
- (3) Place the Sensor, R7, in a high temperature reference oven. (For calibration accurate to within one degree F, hold the sensor in your hand and use body temperature as the reference.
- (4) With switch S1 in the "Memory" position, adjust the "High Temp" potentiometer, R5, until the high reference temperature is indicated on M1.
- (5) Repeat steps (2) and (4) several times until the correct temperatures are indicated on the meter, M1, without adjustment.

Temperature Alarm. The temperature alarm light may be adjusted to come on at any point using the following procedures:

- (1) Switch the selector switch, S1, to the "Power Supply" position. The temperature should indicate the present room temperature. Note this reading and then adjust the low setting potentiometer, R1, until the desired temperature limit is indicated on the meter, M1.
- (2) If the temperature alarm light is on, adjust the "Temperature Limit" potentiometer R12 until the temperature alarm light just goes out.
- (3) If the temperature alarm light is off, adjust R12 until it just comes on.
- (4) Adjust R1 until the present room temperature that was noted in step (1) is indicated on the temperature meter, M1.

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Computer Power Alarm. The power supply alarm can be adjusted to detect an overvoltage of 28.1 volts and an undervoltage of 27.9 volts. Calibration of the power supply alarm circuit is accomplished as follows:

- (1) Adjust the undervoltage potentiometer, R22, (Low Set) for maximum voltage on the center tap. (clockwise).
- (2) Adjust the overvoltage potentiometer, R18, (High Set) for minimum voltage on the center tap (counter clockwise). At this time, the Power Supply alarm light, B2, should be off.
- (3) Adjust R22 until the Power Supply Alarm light just comes on, then back off the potentiometer until the light just goes out.
- (4) Repeat step (3) for R18.

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Parts List for Temperature Sensing Network

A1, A2, A3	-	SN72558, operational amplifier
B1, B2	-	6v, 40 milliamp bulb
C1	-	400u farad, 15v electrolytic capacitor
C2, C3	-	10u farad, 15v capacitor
D1	-	1N4735, 6.2v, 1-watt zener diode
D2	-	1N4001 diode
G1, G2, G3	-	S7400 quad-dual input nand gates
M1	-	0-1 milliamp meter, 50 ohm max resistance (a 100 ohm meter may be used by removing R-17 and hooking the input to A1 on the plus side of M1)
R1	-	1,000 ohm potentiometer
R2	-	150 ohm, 1/2 watt resistor
R3	-	100 ohm, 1/2 watt resistor
R4, R6	-	470 ohm, 1/2 watt resistor
R5	-	500 ohm potentiometer
R7, R9	-	100 ohm, 10% Sensistor
R8	-	50 ohm potentiometer
R10	-	100 ohm, 1/2 watt resistor
R11, R14, R15, R16, R19, R20	-	10 k ohm, 1/4 watt resistor
R12	-	200 ohm potentiometer
R13	-	15 k ohm, 1/2 watt resistor
R17	-	47 ohm, 1/2 watt resistor
R17, R22	-	10 k ohm potentiometer
R21	-	4700 ohm, 1/2 watt resistor
R23, R24, R25	-	10 meg ohm, 1/4 watt resistor
R26, R27, R28	-	3900 ohm, 1/4 watt resistor
S1	-	Single pull single throw switch
T1	-	Filament transformer, 6.3 volt secondary

Appendix C

Wiring list for the D-17B computer (From Ref 16:3-5 to 3-41)

From Receptacle and Terminal No	To Receptacle and Terminal No	Function
20211-1	20211-1	CL-1
20211-2	20211-2	CL-2
20211-3	20211-3	CL-3
20211-4	20211-4	CL-4
20211-5	20211-5	CL-5
20211-6	20211-6	CL-6
20211-7	20211-7	CL-7
20211-8	20211-8	CL-8
20211-9	20211-9	CL-9
20211-10	20211-10	CL-10
20211-11	20211-11	CL-11
20211-12	20211-12	CL-12
20211-13	20211-13	CL-13
20211-14	20211-14	CL-14
20211-15	20211-15	CL-15
20211-16	20211-16	CL-16
20211-17	20211-17	CL-17
20211-18	20211-18	CL-18
20211-19	20211-19	CL-19
20211-20	20211-20	CL-20
20211-21	20211-21	CL-21
20211-22	20211-22	CL-22
20211-23	20211-23	CL-23
20211-24	20211-24	CL-24
20211-25	20211-25	CL-25
20211-26	20211-26	CL-26
20211-27	20211-27	CL-27
20211-28	20211-28	CL-28
20211-29	20211-29	CL-29
20211-30	20211-30	CL-30
20211-31	20211-31	CL-31
20211-32	20211-32	CL-32
20211-33	20211-33	CL-33
20211-34	20211-34	CL-34
20211-35	20211-35	CL-35
20211-36	20211-36	CL-36
20211-37	20211-37	CL-37
20211-38	20211-38	CL-38
20211-39	20211-39	CL-39
20211-40	20211-40	CL-40
20211-41	20211-41	CL-41
20211-42	20211-42	CL-42
20211-43	20211-43	CL-43
20211-44	20211-44	CL-44
20211-45	20211-45	CL-45
20211-46	20211-46	CL-46
20211-47	20211-47	CL-47
20211-48	20211-48	CL-48
20211-49	20211-49	CL-49
20211-50	20211-50	CL-50

From Receptacle and Terminal No	To Receptacle and Terminal No	Function
20212-1	20212-1	CL-1
20212-2	20212-2	CL-2
20212-3	20212-3	CL-3
20212-4	20212-4	CL-4
20212-5	20212-5	CL-5
20212-6	20212-6	CL-6
20212-7	20212-7	CL-7
20212-8	20212-8	CL-8
20212-9	20212-9	CL-9
20212-10	20212-10	CL-10
20212-11	20212-11	CL-11
20212-12	20212-12	CL-12
20212-13	20212-13	CL-13
20212-14	20212-14	CL-14
20212-15	20212-15	CL-15
20212-16	20212-16	CL-16
20212-17	20212-17	CL-17
20212-18	20212-18	CL-18
20212-19	20212-19	CL-19
20212-20	20212-20	CL-20
20212-21	20212-21	CL-21
20212-22	20212-22	CL-22
20212-23	20212-23	CL-23
20212-24	20212-24	CL-24
20212-25	20212-25	CL-25
20212-26	20212-26	CL-26
20212-27	20212-27	CL-27
20212-28	20212-28	CL-28
20212-29	20212-29	CL-29
20212-30	20212-30	CL-30
20212-31	20212-31	CL-31
20212-32	20212-32	CL-32
20212-33	20212-33	CL-33
20212-34	20212-34	CL-34
20212-35	20212-35	CL-35
20212-36	20212-36	CL-36
20212-37	20212-37	CL-37
20212-38	20212-38	CL-38
20212-39	20212-39	CL-39
20212-40	20212-40	CL-40
20212-41	20212-41	CL-41
20212-42	20212-42	CL-42
20212-43	20212-43	CL-43
20212-44	20212-44	CL-44
20212-45	20212-45	CL-45
20212-46	20212-46	CL-46
20212-47	20212-47	CL-47
20212-48	20212-48	CL-48
20212-49	20212-49	CL-49
20212-50	20212-50	CL-50

From Receptacle and Terminal No	To Receptacle and Terminal No	Function
20213-1	20213-1	CL-1
20213-2	20213-2	CL-2
20213-3	20213-3	CL-3
20213-4	20213-4	CL-4
20213-5	20213-5	CL-5
20213-6	20213-6	CL-6
20213-7	20213-7	CL-7
20213-8	20213-8	CL-8
20213-9	20213-9	CL-9
20213-10	20213-10	CL-10
20213-11	20213-11	CL-11
20213-12	20213-12	CL-12
20213-13	20213-13	CL-13
20213-14	20213-14	CL-14
20213-15	20213-15	CL-15
20213-16	20213-16	CL-16
20213-17	20213-17	CL-17
20213-18	20213-18	CL-18
20213-19	20213-19	CL-19
20213-20	20213-20	CL-20
20213-21	20213-21	CL-21
20213-22	20213-22	CL-22
20213-23	20213-23	CL-23
20213-24	20213-24	CL-24
20213-25	20213-25	CL-25
20213-26	20213-26	CL-26
20213-27	20213-27	CL-27
20213-28	20213-28	CL-28
20213-29	20213-29	CL-29
20213-30	20213-30	CL-30
20213-31	20213-31	CL-31
20213-32	20213-32	CL-32
20213-33	20213-33	CL-33
20213-34	20213-34	CL-34
20213-35	20213-35	CL-35
20213-36	20213-36	CL-36
20213-37	20213-37	CL-37
20213-38	20213-38	CL-38
20213-39	20213-39	CL-39
20213-40	20213-40	CL-40
20213-41	20213-41	CL-41
20213-42	20213-42	CL-42
20213-43	20213-43	CL-43
20213-44	20213-44	CL-44
20213-45	20213-45	CL-45
20213-46	20213-46	CL-46
20213-47	20213-47	CL-47
20213-48	20213-48	CL-48
20213-49	20213-49	CL-49
20213-50	20213-50	CL-50

From Receptacle and Terminal No	To Receptacle and Terminal No	Function
20214-1	20214-1	CL-1
20214-2	20214-2	CL-2
20214-3	20214-3	CL-3
20214-4	20214-4	CL-4
20214-5	20214-5	CL-5
20214-6	20214-6	CL-6
20214-7	20214-7	CL-7
20214-8	20214-8	CL-8
20214-9	20214-9	CL-9
20214-10	20214-10	CL-10
20214-11	20214-11	CL-11
20214-12	20214-12	CL-12
20214-13	20214-13	CL-13
20214-14	20214-14	CL-14
20214-15	20214-15	CL-15
20214-16	20214-16	CL-16
20214-17	20214-17	CL-17
20214-18	20214-18	CL-18
20214-19	20214-19	CL-19
20214-20	20214-20	CL-20
20214-21	20214-21	CL-21
20214-22	20214-22	CL-22
20214-23	20214-23	CL-23
20214-24	20214-24	CL-24
20214-25	20214-25	CL-25
20214-26	20214-26	CL-26
20214-27	20214-27	CL-27
20214-28	20214-28	CL-28
20214-29	20214-29	CL-29
20214-30	20214-30	CL-30
20214-31	20214-31	CL-31
20214-32	20214-32	CL-32
20214-33	20214-33	CL-33
20214-34	20214-34	CL-34
20214-35	20214-35	CL-35
20214-36	20214-36	CL-36
20214-37	20214-37	CL-37
20214-38	20214-38	CL-38
20214-39	20214-39	CL-39
20214-40	20214-40	CL-40
20214-41	20214-41	CL-41
20214-42	20214-42	CL-42
20214-43	20214-43	CL-43
20214-44	20214-44	CL-44
20214-45	20214-45	CL-45
20214-46	20214-46	CL-46
20214-47	20214-47	CL-47
20214-48	20214-48	CL-48
20214-49	20214-49	CL-49
20214-50	20214-50	CL-50

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From Receipts and Terminal No.	To Receipts and Terminal No.	Function
12200	12200	122
12201	12201	122
12202	12202	122
12203	12203	122
12204	12204	122
12205	12205	122
12206	12206	122
12207	12207	122
12208	12208	122
12209	12209	122
12210	12210	122
12211	12211	122
12212	12212	122
12213	12213	122
12214	12214	122
12215	12215	122
12216	12216	122
12217	12217	122
12218	12218	122
12219	12219	122
12220	12220	122
12221	12221	122
12222	12222	122
12223	12223	122
12224	12224	122
12225	12225	122
12226	12226	122
12227	12227	122
12228	12228	122
12229	12229	122
12230	12230	122
12231	12231	122
12232	12232	122
12233	12233	122
12234	12234	122
12235	12235	122
12236	12236	122
12237	12237	122
12238	12238	122
12239	12239	122
12240	12240	122
12241	12241	122
12242	12242	122
12243	12243	122
12244	12244	122
12245	12245	122
12246	12246	122
12247	12247	122
12248	12248	122
12249	12249	122
12250	12250	122
12251	12251	122
12252	12252	122
12253	12253	122
12254	12254	122
12255	12255	122
12256	12256	122
12257	12257	122
12258	12258	122
12259	12259	122
12260	12260	122
12261	12261	122
12262	12262	122
12263	12263	122
12264	12264	122
12265	12265	122
12266	12266	122
12267	12267	122
12268	12268	122
12269	12269	122
12270	12270	122
12271	12271	122
12272	12272	122
12273	12273	122
12274	12274	122
12275	12275	122
12276	12276	122
12277	12277	122
12278	12278	122
12279	12279	122
12280	12280	122
12281	12281	122
12282	12282	122
12283	12283	122
12284	12284	122
12285	12285	122
12286	12286	122
12287	12287	122
12288	12288	122
12289	12289	122
12290	12290	122
12291	12291	122
12292	12292	122
12293	12293	122
12294	12294	122
12295	12295	122
12296	12296	122
12297	12297	122
12298	12298	122
12299	12299	122
12300	12300	122

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
12301	12301	122
12302	12302	122
12303	12303	122
12304	12304	122
12305	12305	122
12306	12306	122
12307	12307	122
12308	12308	122
12309	12309	122
12310	12310	122
12311	12311	122
12312	12312	122
12313	12313	122
12314	12314	122
12315	12315	122
12316	12316	122
12317	12317	122
12318	12318	122
12319	12319	122
12320	12320	122
12321	12321	122
12322	12322	122
12323	12323	122
12324	12324	122
12325	12325	122
12326	12326	122
12327	12327	122
12328	12328	122
12329	12329	122
12330	12330	122
12331	12331	122
12332	12332	122
12333	12333	122
12334	12334	122
12335	12335	122
12336	12336	122
12337	12337	122
12338	12338	122
12339	12339	122
12340	12340	122
12341	12341	122
12342	12342	122
12343	12343	122
12344	12344	122
12345	12345	122
12346	12346	122
12347	12347	122
12348	12348	122
12349	12349	122
12350	12350	122
12351	12351	122
12352	12352	122
12353	12353	122
12354	12354	122
12355	12355	122
12356	12356	122
12357	12357	122
12358	12358	122
12359	12359	122
12360	12360	122
12361	12361	122
12362	12362	122
12363	12363	122
12364	12364	122
12365	12365	122
12366	12366	122
12367	12367	122
12368	12368	122
12369	12369	122
12370	12370	122
12371	12371	122
12372	12372	122
12373	12373	122
12374	12374	122
12375	12375	122
12376	12376	122
12377	12377	122
12378	12378	122
12379	12379	122
12380	12380	122
12381	12381	122
12382	12382	122
12383	12383	122
12384	12384	122
12385	12385	122
12386	12386	122
12387	12387	122
12388	12388	122
12389	12389	122
12390	12390	122
12391	12391	122
12392	12392	122
12393	12393	122
12394	12394	122
12395	12395	122
12396	12396	122
12397	12397	122
12398	12398	122
12399	12399	122
12400	12400	122

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
12401	12401	122
12402	12402	122
12403	12403	122
12404	12404	122
12405	12405	122
12406	12406	122
12407	12407	122
12408	12408	122
12409	12409	122
12410	12410	122
12411	12411	122
12412	12412	122
12413	12413	122
12414	12414	122
12415	12415	122
12416	12416	122
12417	12417	122
12418	12418	122
12419	12419	122
12420	12420	122
12421	12421	122
12422	12422	122
12423	12423	122
12424	12424	122
12425	12425	122
12426	12426	122
12427	12427	122
12428	12428	122
12429	12429	122
12430	12430	122
12431	12431	122
12432	12432	122
12433	12433	122
12434	12434	122
12435	12435	122
12436	12436	122
12437	12437	122
12438	12438	122
12439	12439	122
12440	12440	122
12441	12441	122
12442	12442	122
12443	12443	122
12444	12444	122
12445	12445	122
12446	12446	122
12447	12447	122
12448	12448	122
12449	12449	122
12450	12450	122
12451	12451	122
12452	12452	122
12453	12453	122
12454	12454	122
12455	12455	122
12456	12456	122
12457	12457	122
12458	12458	122
12459	12459	122
12460	12460	122
12461	12461	122
12462	12462	122
12463	12463	122
12464	12464	122
12465	12465	122
12466	12466	122
12467	12467	122
12468	12468	122
12469	12469	122
12470	12470	122
12471	12471	122
12472	12472	122
12473	12473	122
12474	12474	122
12475	12475	122
12476	12476	122
12477	12477	122
12478	12478	122
12479	12479	122
12480	12480	122
12481	12481	122
12482	12482	122
12483	12483	122
12484	12484	122
12485	12485	122
12486	12486	122
12487	12487	122
12488	12488	122
12489	12489	122
12490	12490	122
12491	12491	122
12492	12492	122
12493	12493	122
12494	12494	122
12495	12495	122
12496	12496	122
12497	12497	122
12498	12498	122
12499	12499	122
12500	12500	122

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
12501	12501	122
12502	12502	122
12503	12503	122
12504	12504	122
12505	12505	122
12506	12506	122
12507	12507	122
12508	12508	122
12509	12509	122
12510	12510	122
12511	12511	122
12512	12512	122
12513	12513	122
12514	12514	122
12515	12515	122
12516	12516	122
12517	12517	122
12518	12518	122
12519	12519	122
12520	12520	122
12521	12521	122
12522	12522	122
12523	12523	122
12524	12524	122
12525	12525	122
12526	12526	122
12527	12527	122
12528	12528	122
12529	12529	122
12530	12530	122
12531	12531	122
12532	12532	122
12533	12533	122
12534	12534	122
12535	12535	122
12536	12536	122
12537	12537	122
12538	12538	122
12539	12539	122
12540	12540	122
12541	12541	122
12542	12542	122
12543	12543	122
12544	12544	122
12545	12545	122
12546	12546	122
12547	12547	122
12548	12548	122
12549	12549	122
12550	12550	122
12551	12551	122
12552	12552	122
12553	12553	122
12554	12554	122
12555	12555	122
12556	12556	122
12557	12557	122
12558	12558	122
12559	12559	122
12560	12560	122
12561	12561	122
12562	12562	122
12563	12563	122
12564		

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
20703	20715	141
20715	20745	141
20745	20759	142
20759	20761	142
20761	20791	143
20791	20797	143
20797	20801	144
20801	20803	144
20803	20805	145
20805	20807	145
20807	20809	146
20809	20811	146
20811	20813	147
20813	20815	147
20815	20817	148
20817	20819	148
20819	20821	149
20821	20823	149
20823	20825	150
20825	20827	150
20827	20829	151
20829	20831	151
20831	20833	152
20833	20835	152
20835	20837	153
20837	20839	153
20839	20841	154
20841	20843	154
20843	20845	155
20845	20847	155
20847	20849	156
20849	20851	156
20851	20853	157
20853	20855	157
20855	20857	158
20857	20859	158
20859	20861	159
20861	20863	159
20863	20865	160
20865	20867	160
20867	20869	161
20869	20871	161
20871	20873	162
20873	20875	162
20875	20877	163
20877	20879	163
20879	20881	164
20881	20883	164
20883	20885	165
20885	20887	165
20887	20889	166
20889	20891	166
20891	20893	167
20893	20895	167
20895	20897	168
20897	20899	168
20899	20901	169
20901	20903	169
20903	20905	170
20905	20907	170
20907	20909	171
20909	20911	171
20911	20913	172
20913	20915	172
20915	20917	173
20917	20919	173
20919	20921	174
20921	20923	174
20923	20925	175
20925	20927	175
20927	20929	176
20929	20931	176
20931	20933	177
20933	20935	177
20935	20937	178
20937	20939	178
20939	20941	179
20941	20943	179
20943	20945	180
20945	20947	180
20947	20949	181
20949	20951	181
20951	20953	182
20953	20955	182
20955	20957	183
20957	20959	183
20959	20961	184
20961	20963	184
20963	20965	185
20965	20967	185
20967	20969	186
20969	20971	186
20971	20973	187
20973	20975	187
20975	20977	188
20977	20979	188
20979	20981	189
20981	20983	189
20983	20985	190
20985	20987	190
20987	20989	191
20989	20991	191
20991	20993	192
20993	20995	192
20995	20997	193
20997	20999	193

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
20999	21001	194
21001	21003	194
21003	21005	195
21005	21007	195
21007	21009	196
21009	21011	196
21011	21013	197
21013	21015	197
21015	21017	198
21017	21019	198
21019	21021	199
21021	21023	199
21023	21025	200
21025	21027	200
21027	21029	201
21029	21031	201
21031	21033	202
21033	21035	202
21035	21037	203
21037	21039	203
21039	21041	204
21041	21043	204
21043	21045	205
21045	21047	205
21047	21049	206
21049	21051	206
21051	21053	207
21053	21055	207
21055	21057	208
21057	21059	208
21059	21061	209
21061	21063	209
21063	21065	210
21065	21067	210
21067	21069	211
21069	21071	211
21071	21073	212
21073	21075	212
21075	21077	213
21077	21079	213
21079	21081	214
21081	21083	214
21083	21085	215
21085	21087	215
21087	21089	216
21089	21091	216
21091	21093	217
21093	21095	217
21095	21097	218
21097	21099	218
21099	21101	219
21101	21103	219
21103	21105	220
21105	21107	220
21107	21109	221
21109	21111	221
21111	21113	222
21113	21115	222
21115	21117	223
21117	21119	223
21119	21121	224
21121	21123	224
21123	21125	225
21125	21127	225
21127	21129	226
21129	21131	226
21131	21133	227
21133	21135	227
21135	21137	228
21137	21139	228
21139	21141	229
21141	21143	229
21143	21145	230
21145	21147	230
21147	21149	231
21149	21151	231
21151	21153	232
21153	21155	232
21155	21157	233
21157	21159	233
21159	21161	234
21161	21163	234
21163	21165	235
21165	21167	235
21167	21169	236
21169	21171	236
21171	21173	237
21173	21175	237
21175	21177	238
21177	21179	238
21179	21181	239
21181	21183	239
21183	21185	240
21185	21187	240
21187	21189	241
21189	21191	241
21191	21193	242
21193	21195	242
21195	21197	243
21197	21199	243

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
21199	21201	244
21201	21203	244
21203	21205	245
21205	21207	245
21207	21209	246
21209	21211	246
21211	21213	247
21213	21215	247
21215	21217	248
21217	21219	248
21219	21221	249
21221	21223	249
21223	21225	250
21225	21227	250
21227	21229	251
21229	21231	251
21231	21233	252
21233	21235	252
21235	21237	253
21237	21239	253
21239	21241	254
21241	21243	254
21243	21245	255
21245	21247	255
21247	21249	256
21249	21251	256
21251	21253	257
21253	21255	257
21255	21257	258
21257	21259	258
21259	21261	259
21261	21263	259
21263	21265	260
21265	21267	260
21267	21269	261
21269	21271	261
21271	21273	262
21273	21275	262
21275	21277	263
21277	21279	263
21279	21281	264
21281	21283	264
21283	21285	265
21285	21287	265
21287	21289	266
21289	21291	266
21291	21293	267
21293	21295	267
21295	21297	268
21297	21299	268
21299	21301	269
21301	21303	269
21303	21305	270
21305	21307	270
21307	21309	271
21309	21311	271
21311	21313	272
21313	21315	272
21315	21317	273
21317	21319	273
21319	21321	274
21321	21323	274
21323	21325	275
21325	21327	275
21327	21329	276
21329	21331	276
21331	21333	277
21333	21335	277
21335	21337	278
21337	21339	278
21339	21341	279
21341	21343	279
21343	21345	280
21345	21347	280
21347	21349	281
21349	21351	281
21351	21353	282
21353	21355	282
21355	21357	283
21357	21359	283
21359	21361	284
21361	21363	284
21363	21365	285
21365	21367	285
21367	21369	286
21369	21371	286
21371	21373	287
21373	21375	287
21375	21377	288
21377	21379	288
21379	21381	289
21381	21383	289
21383	21385	290
21385	21387	290
21387	21389	291
21389	21391	291
21391	21393	292
21393	21395	292
21395	21397	293
21397	21399	293

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
21399	21401	294
21401	21403	294
21403	21405	295
21405	21407	295
21407	21409	296
21409	21411	296
21411	21413	297
21413	21415	297
21415	21417	298
21417	21419	298
21419	21421	299
21421	21423	299
21423	21425	300
21425	21427	300
21427	21429	301
21429	21431	301
21431	21433	302
21433	21435	302
21435	21437	303
21437	21439	303
21439	21441	304
21441	21443	304
21443	21445	305
21445	21447	305
21447	21449	306
21449	21451	306
21451	21453	307
21453	21455	307
21455	21457	308
21457	21459	308
21459	21461	309
21461	21463	309
21463	21465	310
21465	21467	310
21467	21469	311
21469	21471	311
21471	21473	312
21473	21475	312
21475	21477	313
21477	21479	313
21479	21481	314
21481	21483	314
21483	21485	315
21485	21487	315
21487	21489	316
21489	21491	316
21491	21493	317
21493	21495	317
21495	21497	318
21497	21499	318
21499	21501	319
21501	21503	319
21503	21505	320
21505	21507	320
21507	21509	321
21509	21511	321
21511	21513	322
21513	21515	322
21515		

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
31-27	3030-18	V22
31-28	3040-20	V22
31-29	3040-24	V22
31-30	3040-28	V22
31-31	3040-32	V22
31-32	3040-36	V22
31-33	3040-40	V22
31-34	3040-44	V22
31-35	3040-48	V22
31-36	3040-52	V22
31-37	3040-56	V22
31-38	3040-60	V22
31-39	3040-64	V22
31-40	3040-68	V22
31-41	3040-72	V22
31-42	3040-76	V22
31-43	3040-80	V22
31-44	3040-84	V22
31-45	3040-88	V22
31-46	3040-92	V22
31-47	3040-96	V22
31-48	3040-100	V22
31-49	3040-104	V22
31-50	3040-108	V22
31-51	3040-112	V22
31-52	3040-116	V22
31-53	3040-120	V22
31-54	3040-124	V22
31-55	3040-128	V22
31-56	3040-132	V22
31-57	3040-136	V22
31-58	3040-140	V22
31-59	3040-144	V22
31-60	3040-148	V22
31-61	3040-152	V22
31-62	3040-156	V22
31-63	3040-160	V22
31-64	3040-164	V22
31-65	3040-168	V22
31-66	3040-172	V22
31-67	3040-176	V22
31-68	3040-180	V22
31-69	3040-184	V22
31-70	3040-188	V22
31-71	3040-192	V22
31-72	3040-196	V22
31-73	3040-200	V22
31-74	3040-204	V22
31-75	3040-208	V22
31-76	3040-212	V22
31-77	3040-216	V22
31-78	3040-220	V22
31-79	3040-224	V22
31-80	3040-228	V22
31-81	3040-232	V22
31-82	3040-236	V22
31-83	3040-240	V22
31-84	3040-244	V22
31-85	3040-248	V22
31-86	3040-252	V22
31-87	3040-256	V22
31-88	3040-260	V22
31-89	3040-264	V22
31-90	3040-268	V22
31-91	3040-272	V22
31-92	3040-276	V22
31-93	3040-280	V22
31-94	3040-284	V22
31-95	3040-288	V22
31-96	3040-292	V22
31-97	3040-296	V22
31-98	3040-300	V22
31-99	3040-304	V22
31-100	3040-308	V22
31-101	3040-312	V22
31-102	3040-316	V22
31-103	3040-320	V22
31-104	3040-324	V22
31-105	3040-328	V22
31-106	3040-332	V22
31-107	3040-336	V22
31-108	3040-340	V22
31-109	3040-344	V22
31-110	3040-348	V22
31-111	3040-352	V22
31-112	3040-356	V22
31-113	3040-360	V22
31-114	3040-364	V22
31-115	3040-368	V22
31-116	3040-372	V22
31-117	3040-376	V22
31-118	3040-380	V22
31-119	3040-384	V22
31-120	3040-388	V22
31-121	3040-392	V22
31-122	3040-396	V22
31-123	3040-400	V22
31-124	3040-404	V22
31-125	3040-408	V22
31-126	3040-412	V22
31-127	3040-416	V22
31-128	3040-420	V22
31-129	3040-424	V22
31-130	3040-428	V22
31-131	3040-432	V22
31-132	3040-436	V22
31-133	3040-440	V22
31-134	3040-444	V22
31-135	3040-448	V22
31-136	3040-452	V22
31-137	3040-456	V22
31-138	3040-460	V22
31-139	3040-464	V22
31-140	3040-468	V22
31-141	3040-472	V22
31-142	3040-476	V22
31-143	3040-480	V22
31-144	3040-484	V22
31-145	3040-488	V22
31-146	3040-492	V22
31-147	3040-496	V22
31-148	3040-500	V22
31-149	3040-504	V22
31-150	3040-508	V22
31-151	3040-512	V22
31-152	3040-516	V22
31-153	3040-520	V22
31-154	3040-524	V22
31-155	3040-528	V22
31-156	3040-532	V22
31-157	3040-536	V22
31-158	3040-540	V22
31-159	3040-544	V22
31-160	3040-548	V22
31-161	3040-552	V22
31-162	3040-556	V22
31-163	3040-560	V22
31-164	3040-564	V22
31-165	3040-568	V22
31-166	3040-572	V22
31-167	3040-576	V22
31-168	3040-580	V22
31-169	3040-584	V22
31-170	3040-588	V22
31-171	3040-592	V22
31-172	3040-596	V22
31-173	3040-600	V22
31-174	3040-604	V22
31-175	3040-608	V22
31-176	3040-612	V22
31-177	3040-616	V22
31-178	3040-620	V22
31-179	3040-624	V22
31-180	3040-628	V22
31-181	3040-632	V22
31-182	3040-636	V22
31-183	3040-640	V22
31-184	3040-644	V22
31-185	3040-648	V22
31-186	3040-652	V22
31-187	3040-656	V22
31-188	3040-660	V22
31-189	3040-664	V22
31-190	3040-668	V22
31-191	3040-672	V22
31-192	3040-676	V22
31-193	3040-680	V22
31-194	3040-684	V22
31-195	3040-688	V22
31-196	3040-692	V22
31-197	3040-696	V22
31-198	3040-700	V22
31-199	3040-704	V22
31-200	3040-708	V22

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
31-201	3040-712	V22
31-202	3040-716	V22
31-203	3040-720	V22
31-204	3040-724	V22
31-205	3040-728	V22
31-206	3040-732	V22
31-207	3040-736	V22
31-208	3040-740	V22
31-209	3040-744	V22
31-210	3040-748	V22
31-211	3040-752	V22
31-212	3040-756	V22
31-213	3040-760	V22
31-214	3040-764	V22
31-215	3040-768	V22
31-216	3040-772	V22
31-217	3040-776	V22
31-218	3040-780	V22
31-219	3040-784	V22
31-220	3040-788	V22
31-221	3040-792	V22
31-222	3040-796	V22
31-223	3040-800	V22
31-224	3040-804	V22
31-225	3040-808	V22
31-226	3040-812	V22
31-227	3040-816	V22
31-228	3040-820	V22
31-229	3040-824	V22
31-230	3040-828	V22
31-231	3040-832	V22
31-232	3040-836	V22
31-233	3040-840	V22
31-234	3040-844	V22
31-235	3040-848	V22
31-236	3040-852	V22
31-237	3040-856	V22
31-238	3040-860	V22
31-239	3040-864	V22
31-240	3040-868	V22
31-241	3040-872	V22
31-242	3040-876	V22
31-243	3040-880	V22
31-244	3040-884	V22
31-245	3040-888	V22
31-246	3040-892	V22
31-247	3040-896	V22
31-248	3040-900	V22
31-249	3040-904	V22
31-250	3040-908	V22
31-251	3040-912	V22
31-252	3040-916	V22
31-253	3040-920	V22
31-254	3040-924	V22
31-255	3040-928	V22
31-256	3040-932	V22
31-257	3040-936	V22
31-258	3040-940	V22
31-259	3040-944	V22
31-260	3040-948	V22
31-261	3040-952	V22
31-262	3040-956	V22
31-263	3040-960	V22
31-264	3040-964	V22
31-265	3040-968	V22
31-266	3040-972	V22
31-267	3040-976	V22
31-268	3040-980	V22
31-269	3040-984	V22
31-270	3040-988	V22
31-271	3040-992	V22
31-272	3040-996	V22
31-273	3040-1000	V22
31-274	3040-1004	V22
31-275	3040-1008	V22
31-276	3040-1012	V22
31-277	3040-1016	V22
31-278	3040-1020	V22
31-279	3040-1024	V22
31-280	3040-1028	V22
31-281	3040-1032	V22
31-282	3040-1036	V22
31-283	3040-1040	V22
31-284	3040-1044	V22
31-285	3040-1048	V22
31-286	3040-1052	V22
31-287	3040-1056	V22
31-288	3040-1060	V22
31-289	3040-1064	V22
31-290	3040-1068	V22
31-291	3040-1072	V22
31-292	3040-1076	V22
31-293	3040-1080	V22
31-294	3040-1084	V22
31-295	3040-1088	V22
31-296	3040-1092	V22
31-297	3040-1096	V22
31-298	3040-1100	V22
31-299	3040-1104	V22
31-300	3040-1108	V22

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
31-301	3040-1112	V22
31-302	3040-1116	V22
31-303	3040-1120	V22
31-304	3040-1124	V22
31-305	3040-1128	V22
31-306	3040-1132	V22
31-307	3040-1136	V22
31-308	3040-1140	V22
31-309	3040-1144	V22
31-310	3040-1148	V22
31-311	3040-1152	V22
31-312	3040-1156	V22
31-313	3040-1160	V22
31-314	3040-1164	V22
31-315	3040-1168	V22
31-316	3040-1172	V22
31-317	3040-1176	V22
31-318	3040-1180	V22
31-319	3040-1184	V22
31-320	3040-1188	V22
31-321	3040-1192	V22
31-322	3040-1196	V22
31-323	3040-1200	V22
31-324	3040-1204	V22
31-325	3040-1208	V22
31-326	3040-1212	V22
31-327	3040-1216	V22
31-328	3040-1220	V22
31-329	3040-1224	V22
31-330	3040-1228	V22
31-331	3040-1232	V22
31-332	3040-1236	V22
31-333	3040-1240	V22
31-334	3040-1244	V22
31-335	3040-1248	V22
31-336	3040-1252	V22
31-337	3040-1256	V22
31-338	3040-1260	V22
31-339	3040-1264	V22
31-340	3040-1268	V22
31-341	3040-1272	V22
31-342	3040-1276	V22
31-343	3040-1280	V22
31-344	3040-1284	V22
31-345	3040-1288	V22
31-346	3040-1292	V22
31-347	3040-1296	V22
31-348	3040-1300	V22
31-349	3040-1304	V22
31-350	3040-1308	V22
31-351	3040-1312	V22
31-352	3040-1316	V22
31-353	3040-1320	V22
31-354	3040-1324	V22
31-355	3040-1328	V22
31-356	3040-1332	V22
31-357	3040-1336	V22
31-358	3040-1340	V22
31-359	3040-1344	V22
31-360	3040-1348	V22

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
31		

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
25-31	2610-5	2040E
2610-2	2610-5	2040E
2610-7	2610-8	2040E
2610-8	2610-9	2040E
2610-9	2610-10	2040E
2610-10	2610-11	2040E
2610-11	2610-12	2040E

From Receipts and Terminal No.	To Receipts and Terminal No.	Function
2610-9	2610-8	2040E
2610-8	2610-7	2040E
2610-7	2610-6	2040E
2610-6	2610-5	2040E
2610-5	2610-4	2040E

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From Receipts and Terminal No.	To Receipts and Terminal No.	Function
2610-7	2610-6	1911
2610-6	2610-5	1912
2610-5	2610-4	1913
2610-4	2610-3	1914
2610-3	2610-2	1915
2610-2	2610-1	1916
2610-1	2610-0	1917
2610-0	2609-9	1918
2609-9	2609-8	1919
2609-8	2609-7	1920
2609-7	2609-6	1921
2609-6	2609-5	1922
2609-5	2609-4	1923
2609-4	2609-3	1924
2609-3	2609-2	1925
2609-2	2609-1	1926
2609-1	2609-0	1927
2609-0	2608-9	1928
2608-9	2608-8	1929
2608-8	2608-7	1930
2608-7	2608-6	1931
2608-6	2608-5	1932
2608-5	2608-4	1933
2608-4	2608-3	1934
2608-3	2608-2	1935
2608-2	2608-1	1936
2608-1	2608-0	1937
2608-0	2607-9	1938
2607-9	2607-8	1939
2607-8	2607-7	1940
2607-7	2607-6	1941
2607-6	2607-5	1942
2607-5	2607-4	1943
2607-4	2607-3	1944
2607-3	2607-2	1945
2607-2	2607-1	1946
2607-1	2607-0	1947
2607-0	2606-9	1948
2606-9	2606-8	1949
2606-8	2606-7	1950
2606-7	2606-6	1951
2606-6	2606-5	1952
2606-5	2606-4	1953
2606-4	2606-3	1954
2606-3	2606-2	1955
2606-2	2606-1	1956
2606-1	2606-0	1957
2606-0	2605-9	1958
2605-9	2605-8	1959
2605-8	2605-7	1960
2605-7	2605-6	1961
2605-6	2605-5	1962
2605-5	2605-4	1963
2605-4	2605-3	1964
2605-3	2605-2	1965
2605-2	2605-1	1966
2605-1	2605-0	1967
2605-0	2604-9	1968
2604-9	2604-8	1969
2604-8	2604-7	1970
2604-7	2604-6	1971
2604-6	2604-5	1972
2604-5	2604-4	1973
2604-4	2604-3	1974
2604-3	2604-2	1975
2604-2	2604-1	1976
2604-1	2604-0	1977
2604-0	2603-9	1978
2603-9	2603-8	1979
2603-8	2603-7	1980
2603-7	2603-6	1981
2603-6	2603-5	1982
2603-5	2603-4	1983
2603-4	2603-3	1984
2603-3	2603-2	1985
2603-2	2603-1	1986
2603-1	2603-0	1987
2603-0	2602-9	1988
2602-9	2602-8	1989
2602-8	2602-7	1990
2602-7	2602-6	1991
2602-6	2602-5	1992
2602-5	2602-4	1993
2602-4	2602-3	1994
2602-3	2602-2	1995
2602-2	2602-1	1996
2602-1	2602-0	1997
2602-0	2601-9	1998
2601-9	2601-8	1999
2601-8	2601-7	2000
2601-7	2601-6	2001
2601-6	2601-5	2002
2601-5	2601-4	2003
2601-4	2601-3	2004
2601-3	2601-2	2005
2601-2	2601-1	2006
2601-1	2601-0	2007
2601-0	2600-9	2008
2600-9	2600-8	2009
2600-8	2600-7	2010
2600-7	2600-6	2011
2600-6	2600-5	2012
2600-5	2600-4	2013
2600-4	2600-3	2014
2600-3	2600-2	2015
2600-2	2600-1	2016
2600-1	2600-0	2017
2600-0	2599-9	2018
2599-9	2599-8	2019
2599-8	2599-7	2020
2599-7	2599-6	2021
2599-6	2599-5	2022
2599-5	2599-4	2023
2599-4	2599-3	2024
2599-3	2599-2	2025
2599-2	2599-1	2026
2599-1	2599-0	2027
2599-0	2598-9	2028
2598-9	2598-8	2029
2598-8	2598-7	2030
2598-7	2598-6	2031
2598-6	2598-5	2032
2598-5	2598-4	2033
2598-4	2598-3	2034
2598-3	2598-2	2035
2598-2	2598-1	2036
2598-1	2598-0	2037
2598-0	2597-9	2038
2597-9	2597-8	2039
2597-8	2597-7	2040
2597-7	2597-6	2041
2597-6	2597-5	2042
2597-5	2597-4	2043
2597-4	2597-3	2044
2597-3	2597-2	2045
2597-2	2597-1	2046
2597-1	2597-0	2047
2597-0	2596-9	2048
2596-9	2596-8	2049
2596-8	2596-7	2050
2596-7	2596-6	2051
2596-6	2596-5	2052
2596-5	2596-4	2053
2596-4	2596-3	2054
2596-3	2596-2	2055
2596-2	2596-1	2056
2596-1	2596-0	2057
2596-0	2595-9	2058
2595-9	2595-8	2059
2595-8	2595-7	2060
2595-7	2595-6	2061
2595-6	2595-5	2062
2595-5	2595-4	2063
2595-4	2595-3	2064
2595-3	2595-2	2065
2595-2	2595-1	2066
2595-1	2595-0	2067
2595-0	2594-9	2068
2594-9	2594-8	2069
2594-8	2594-7	2070
2594-7	2594-6	2071
2594-6	2594-5	2072
2594-5	2594-4	2073
2594-4	2594-3	2074
2594-3	2594-2	2075
2594-2	2594-1	2076
2594-1	2594-0	2077
2594-0	2593-9	2078
2593-9	2593-8	2079
2593-8	2593-7	2080
2593-7	2593-6	2081
2593-6	2593-5	2082
2593-5	2593-4	2083
2593-4	2593-3	2084
2593-3	2593-2	2085
2593-2	2593-1	2086
2593-1	2593-0	2087
2593-0	2592-9	2088
2592-9	2592-8	2089
2592-8	2592-7	2090
2592-7	2592-6	2091
2592-6	2592-5	2092
2592-5	2592-4	2093
2592-4	2592-3	2094
2592-3	2592-2	2095
2592-2	2592-1	2096
2592-1	2592-0	2097
2592-0	2591-9	2098
2591-9	2591-8	2099
2591-8	2591-7	2100
2591-7	2591-6	2101
2591-6	2591-5	2102
2591-5	2591-4	2103
2591-4	2591-3	2104
2591-3	2591-2	2105
2591-2	2591-1	2106
2591-1	2591-0	2107
2591-0	2590-9	2108
2590-9	2590-8	2109
2590-8	2590-7	2110
2590-7	2590-6	2111
2590-6	2590-5	2112
2590-5	2590-4	2113
2590-4	2590-3	2114
2590-3	2590-2	2115
2590-2	2590-1	2116
2590-1	2590-0	2117
2590-0	2589-9	2118
2589-9	2589-8	2119
2589-8	2589-7	2120
2589-7	2589-6	2121
2589-6	2589-5	2122
2589-5	2589-4	2123
2589-4	2589-3	2124
2589-3	2589-2	2125
2589-2	2589-1	2126
2589-1	2589-0	2127
2589-0	2588-9	2128
2588-9	2588-8	2129
2588-8	2588-7	2130
2588-7	2588-6	2131
2588-6	2588-5	2132
2588-5	2588-4	2133
2588-4	2588-3	2134
2588-3	2588-2	2135
2588-2	2588-1	2136
2588-1	2588-0	2137
2588-0	2587-9	2138
2587-9	2587-8	2139
2587-8	2587-7	2140
2587-7	2587-6	2141
2587-6	2587-5	2142
2587-5	2587-4	2143
2587-4	2587-3	2144
2587-3	2587-2	2145
2587-2	2587-1	2146
2587-1	2587-0	2147
2587-0	2586-9	2148
2586-9	2586-8	2149
2586-8	2586-7	2150
2586-7	2586-6	2151
2586-6	2586-5	2152
2586-5	2586-4	2153
2586-4	2586-3	2154
2586-3	2586-2	2155
2586-2	2586-1	2156
2586-1	2586-0	2157
2586-0	2585-9	2158
2585-9	2585-8	2159
2585-8	2585-7	2160
2585-7	2585-6	2161
2585-6	2585-5	2162
2585-5	2585-4	2163
2585-4	2585-3	2164
2585-3	2585-2	2165
2585-2	2585-1	2166
2585-1	2585-0	2167
2585-0	2584-9	2168
2584-9	2584-8	2169
2584-8	2584-7	2170
2584-7	2584-6	2171
2584-6	2584-5	2172
2584-5	2584-4	2173
2584-4	2584-3	2174
2584-3	2584-2	2175
2584-2	2584-1	2176
2584-1	2584-0	2177
2584-0	2583-9	2178
2583-9	2583-8	2179
2583-8	2583-7	2180
2583-7	2583-6	2181
2583-6	2583-5	2182
2583-5	2583-4	2183
2583-4	2583-3	2184
2583-3	2583-2	2185
2583-2	2583-1	2186
2583-1	2583-0	2187
2583-0	2582-9	2188
2582-9	2582-8	2189
2582-8	2582-7	2190
2582-7	2582-6	2191
2582-6	2582-5	2192
2582-5	2582-4	2193
2582-4	2582-3	2194
2582-3	2582-2	2195
2582-2	2582-1	2196
2582-1	2582-0	2197
2582-0	2581-9	2198
2581-9	2581-8	2199
2581-8	2581-7	2200
2581-7	2581-6	2201
2581-6	2581-5	2202
2581-5	2581-4	2203
2581-4	2581-3	2204
2581-3	2581-2	2205
2581-2	2581-1	2206
2581-1	2581-0	2207
2581-0	2580-9	2208
2580-9	2580-8	2209
2580-8	2580-7	2210
2580-7	2580-6	2211
2580-6	2580-5	2212
2580-5	2580-4	2213
2580-4	2580-3	2214
2580-3	2580-2	2215
2580-2	2580-1	2216
2580-1	2580-0	2217
2580-0	2579-9	2218
2579-9	2579-8	2219
2579-8	2579-7	2220
2579-7	2579-6	2221
2579-6	2579-5	2222
2579-5	2579-4	2223
2579-4	2579-3	2224
2579-3	2579-2	2225
2579-2	2579-1	2226
2579-1	2579-0	2227
2579-0	2578-9	2228
2578-9	2578-8	2229
2578-8	2578-7	2230
2578-7	2578-6	2231
2578		

VITA

Douglas J. Allen was born on 21 June 1941 in Brandenburg, Kentucky. He graduated from high school in Brandenburg in 1959. He attended the University of Cincinnati until 1961 as a student in chemical engineering. In 1961 he joined the United States Air Force and received a commission and navigational flying rating through the Aviation Cadet program. He served in the Strategic Air Command as a B-52 Electronic Warfare Officer until 1968. He attended the Air Force Institute of Technology and received the degree of Bachelor of Science in Electrical Engineering in 1971.

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