AUTOMATIC ELECTRONIC SYSTEMS

JOHN J. WRIGHT
MARKETING REPRESENTATIVE

5455 RUE PARE, MONTREAL 309, CANADA
TEL. (514) 735-6581

September 21st, 1972

Lawrence Lvmr. Lab
P.O. Box 808 L-404
Livermore, Ca. 94550
U.S.A.

Attn.: R.E. Anderson - Phys. Chem.

Dear Sir:

This letter is a response to your request for further information on our AES-8Ø Microprocessor. The material you requested is enclosed.

The processor has been designed for dedicated task processing in a variety of applications - data acquisition, process control, front ends, peripheral control, etc. If, at any time, we can be of further assistance in your application please do not hesitate to call or write.

For your convenience, we have enclosed a pre-addressed reply form. At your convenience, we would appreciate your response on this form.

Thank you for your interest in A.E.S.

Yours very truly,

AUTOMATIC ELECTRONIC SYSTEMS

J. J. Wright
Marketing Representative

JJW:jo

Encl.

Automatic Electronic Systems Inc.

The AES-80 Microprocessor

A Fourth dimension in data acquisition processing and communication

1 Hardware

2 Controllers

3 Minicomputers

4 The AES-80 Microprocessor

There used to be three

There were three ways to design a digital data product or system, that is, until the AES-80 Microprocessor.

1) The traditional approach required dedicated hardware — a time consuming exercise involving long lead times for prototyping. Just when you have your product developed a customer with different requirements sends you back to redesign and modify. Often you end up with a proliferation of products, none with enough volume for reasonable manufacturing costs. Why build hardware if a make/buy analysis favours the AES-80 over your own design?

2) A recent approach uses a controller for logical functions. Typically, controllers have limitations: they are slow — with a limited instruction set and inadequate input/output capability. If you have not found a suitable controller, why not look at our Microprocessor?

3) In more complex applications, a minicomputer is a frequent choice for your dedicated processing application — often a case of overkill (and overexpenditure). A mini is a general purpose digital computer and its capabilities are not required in many applications. Furthermore minicomputer instructions do not always result in an optimum approach to a given problem and input/output is relatively complex. Finally, when you add up the cost for a minicomputer plus memory plus interface options, you have a pretty expensive item. Until the AES-80, however, you had no viable alternatives. Why buy a mini when a micro will do?

Go fourth

with the AES-80 Microprocessor, a byte oriented processor at a fraction of the cost of a mini. It is designed for the OEM or sophisticated user in dedicated processing applications. The AES-80 is part of a family of Modular System Units (MSU's) designed for data acquisition, processing and communication. Serial I/O, analog I/O, communication, control, and special purpose modules are designed for "daisy chaining" with the microprocessor MSU to satisfy specific applications.

Why the AES-80?

Using the AES-80, your design cycle is reduced to writing a software program and debugging it on our easy-to-use Program Development and Control Console. We then convert this program to a permanent Read Only Memory (ROM) and supply the completed microprocessor with memory and input/output MSU's ready for installation. Alternatively, our Programming Service is available for the software phase.

You eliminate that costly design and prototyping cycle and get to your market while others are still in the design phase. In short, the AES-80 can make you money.

The AES-80 features exceptionally fast processing-240 nanoseconds full cycle time with bipolar memory. The instruction set of 92 micro-instructions allows great flexibility for solving application problems efficiently. The input/output capability is exceptional with the serial I/O bus capable of a transfer rate of over 100,000 (8-bit) characters per second to or from the microprocessor. Parallel I/O peripherals share the high speed parallel bus with the data memory and communicate at internal processor speeds.

Naturally there is the cost element. Using the AES-80 optimizes the tradeoff between hardware and software: the microprocessor is extremely competitive with standard hardware design and when you compare our prices to those of a minicomputer, well, there is no contest. If the AES-80 will do the job then it will definitely save dollars and that's the name of the game, isn't it?

Features

- 240 nanosecond full cycle time with bipolar memories.
- serial transfer up to 100,000 8-bit characters/second.
- high speed parallel I/O.
- capability of intermixing memory types in both data and instruction memories (bipolar, MOS, ROM, etc.).
- add-on I/O capability with standard MSU's.
- direct accessing to 1K of data memory and 2K of instruction memory.
- easy to use Program Development and Control Console, which supports a teletype or high speed tape reader. No other computing facilities required.
- expandable to 4K ROM and 4K RAM with additional memory accessible on an indirect basis.
- comprehensive set of 92 micro instructions.
- complete software support includes a cross assembler, minicomputer emulator, a self assembler and standard system development routines.
- multiprocessor configuration facilitated with relinquish bus command.

Applications

1 - OEM
2 - End user
3 - Research

- bread boards
- data communication
- process control
- terminals
- machine tool control
- remote concentration
- educational systems
- custom designs
- CRT controllers
- processing
- peripheral control
- switching
- front end preprocessing
- instrument systems
- automated testing
- airline reservations
- point of sale concentration
- simulators
- medical systems
- contour plotting
- spectrum analysers
- batch terminals
- sequence controllers
- line concentrators
- monitors
- lane counters

- **Cut your design time**
- **Eliminate bread boards**
- **Tradeoff software and hardware optimally**
- **Replace minicomputers in dedicated processing applications**
- **Reduce engineering in custom designs**

Architecture

The AES microprocessor is a bus organized machine designed around a data transfer concept. An 8-bit three-state processor bus is used as the main highway for data traffic between registers and the data memory. The source and destination of data travelling along the processor bus is under complete microprogram control. The basic microprocessor elements are shown in the block diagram.

Memory

A data memory word is 8 bits — chosen for its applicability in data communications. To reduce memory costs a 12-bit instruction word is used, a length which is extremely efficient yet allows single word literal instructions.

Commands from the read-only instruction memory control all aspects of the microprocessor operation and are executed in a single machine clock cycle. The 12-bit data from the ROM output bus is fed to an instruction decoder, the output of which determines the logic functions to be performed within the processor during the machine cycle. The ROM data bus also goes to the inputs of various registers within the microprocessor so that, depending upon the particular instruction decoded, literal data can be outputted directy from ROM.

Data is both read out of and written into data memory via the high speed 8-bit three-state processor bus.

Intermixing

A unique feature of the AES-80 microprocessor is the ability to intermix types of memories in both Data and Instruction Memories. Memory modules of 256 words each (8-bit data memory or 12-bit instruction memory) of many types may be intermixed.

- Bipolar ROM or RAM
- MOS ROM or RAM
- Core RAM
- Capacitive ROM
- Special purpose memories

Memory module selection depends on your requirements for processing speed, power failure protection, and program length. Depending on your volume requirements memories are chosen to minimize set up and unit costs. Intermixing provides flexibility for the solution of many application problems.

Arithmetic Logic Unit (ALU)

The arithmetic logic unit operates on two 8-bit variables the processor bus and its own output buffer accumulator. The ALU is capable of performing up to 16 logic operations on its two input variables and a variety of arithmetic operations, the most important being add and subtract. The mode of the ALU is selected by the ALU command register which is set by executing a single ALU literal instruction.

Registers-

P-Register: The 12-bit P (Program Counter) register indicates the address of the next instruction to be fetched out of instruction memory.

A-Register: The 12-bit A (Data Memory Address) register holds the address of the data memory cell being read from or written into.

LA-Register: The 8-bit LA (ALU Command) register is similar to the L-Register in that an 8 bit literal from ROM is loaded into it during an ALU literal instruction. The output of the LA-Register selects the operating mode of the ALU.

B-Register: The 8-bit (ALU Output Buffer) register is the ALU accumulator in which all results of the arithmetic and logical operations are stored.

U-Register: The U (Universal) register is an 8-bit parallel in, parallel out, serial in or serial out register. It is primarily used as the serial I/O buffer register.

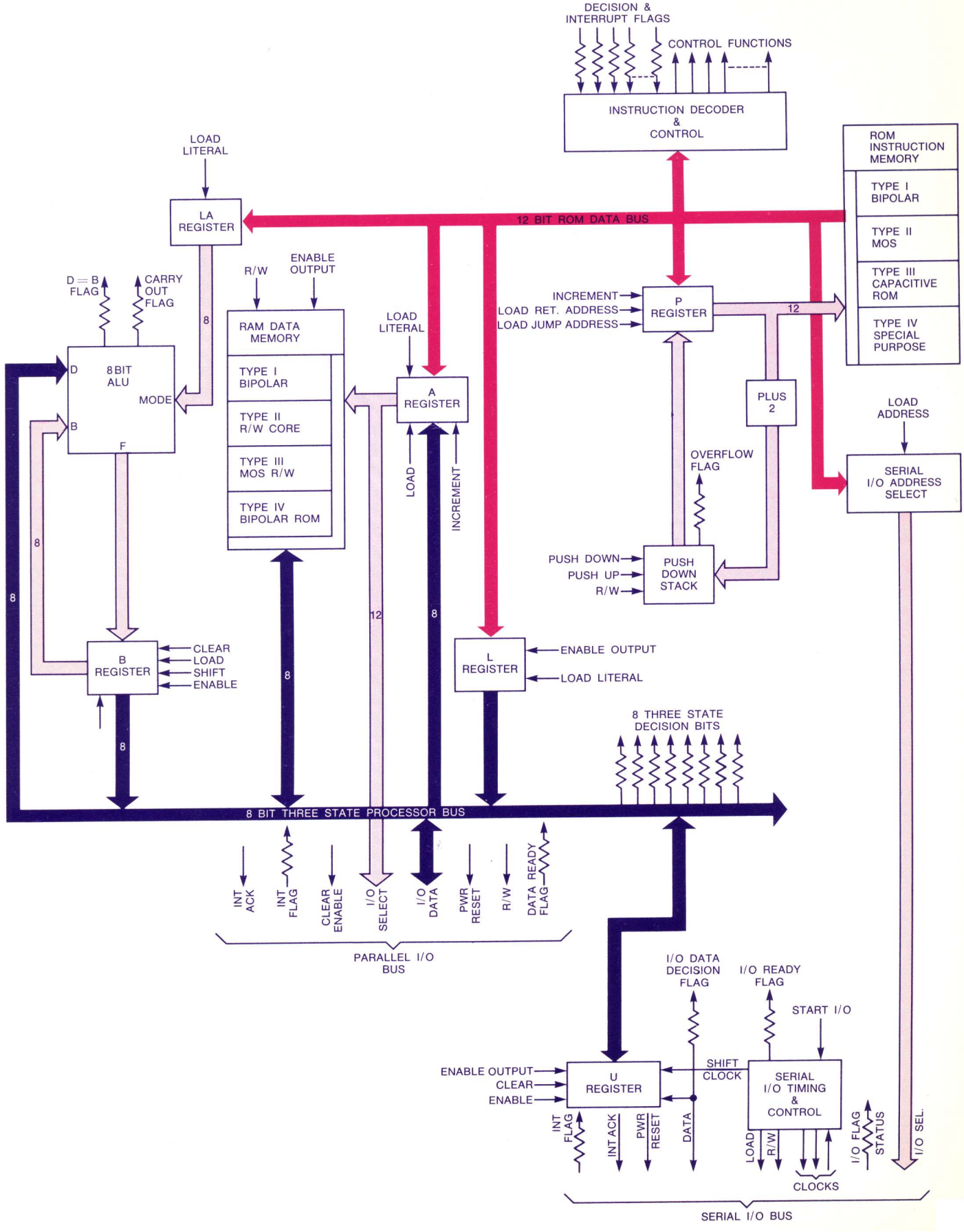
Push Down Stack

The AES microprocessor has an automatic push down stack for routine linkage. With this feature subroutines are written with a minimum of instruction time overhead.

Input / Output

The AES microprocessor serial I/O interface provides the necessary timing and control to communicate with both low and high speed peripheral devices. This I/O bus is used to transfer 8-bit serial characters at rates up to one character every 9.12 microseconds. When a start I/O instruction is executed, the clocking and transfer of I/O data then becomes automatic, with the microprocessor free to execute other instructions during the I/O interval. In addition to the serial I/O, a high speed parallel I/O capability is available. This is normally used as a means of providing fast hardware processor options such as multiply/divide or sine/cosine, etc. This bus is also used as a means of accessing a large data base such as a disc or magnetic tape unit where maximum data throughput is necessary.

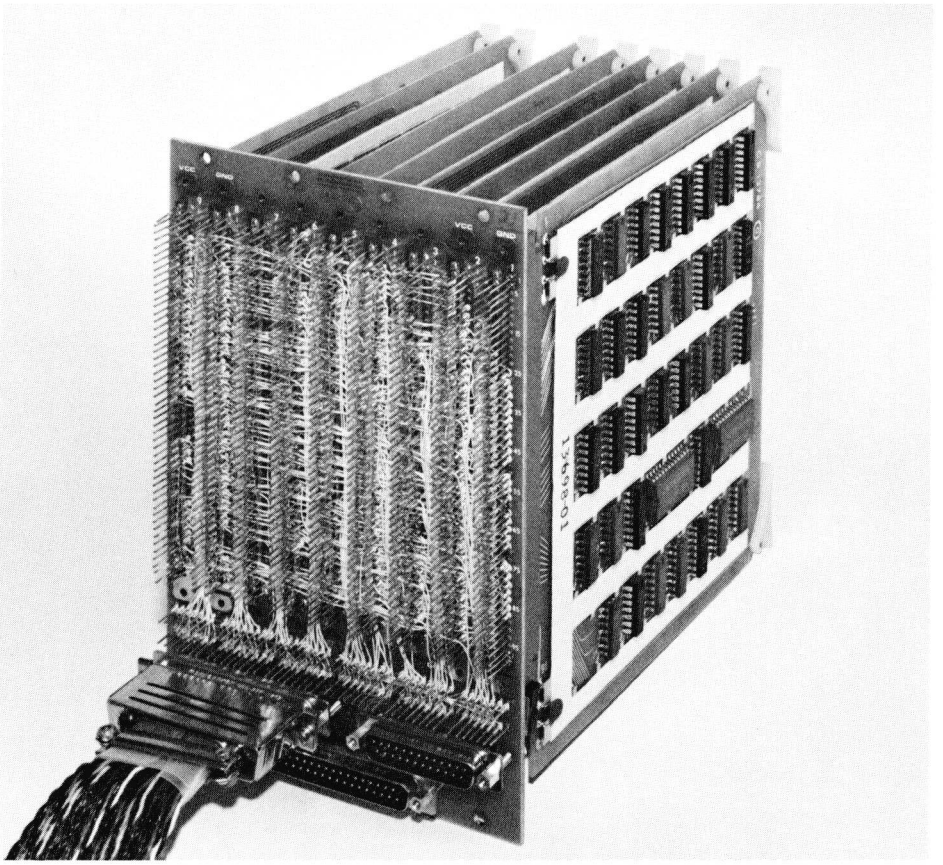
The AES-80 MICROPROCESSOR



Physical Configuration

The basic microprocessor MSU consists of a wire wrap mother board with nine connectors for insertable printed circuit boards. The microprocessor boards consist of 3 logic cards, one ROM card, and one RAM card. Four additional connector slots are available on the mother board. The first of these is reserved for an interface board for communication with the Program Development and Control Console used for program development and checkout.
One position is reserved for serial input/output control which comes in two versions — equipped with three-state inputs and outputs or differential line drivers and receivers. This card increases the load capability on the I/O bus. The remaining two slots may be filled by two parallel I/O interface cards or one interface card and one parallel I/O buffer expander.

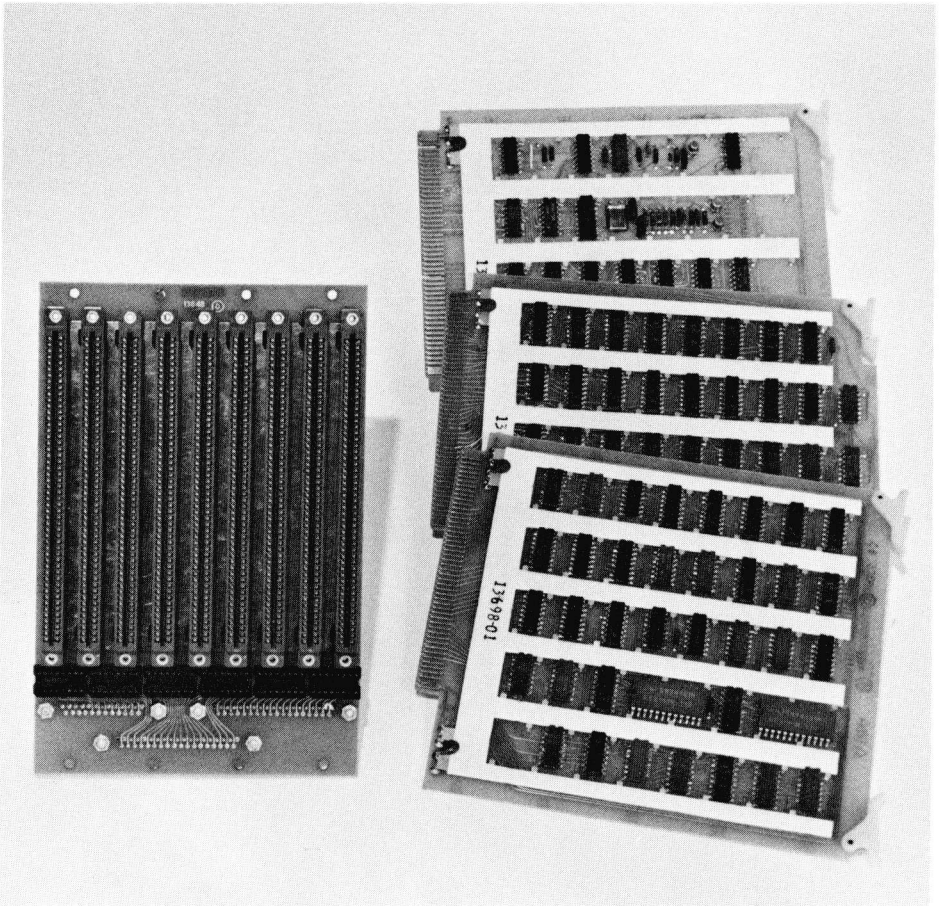
MSU back planes contain three standard connectors — a differential serial I/O connector and 2 parallel I/O connectors. MSU's may be "daisy chained" at distances up to 1000 feet.



Microprocessor Modular System Unit (MSU)

OEM Configurations

The AES-80 is available in packages specifically designed to the mechanical requirements of an OEM user.



MSU backplane with timing and control cards

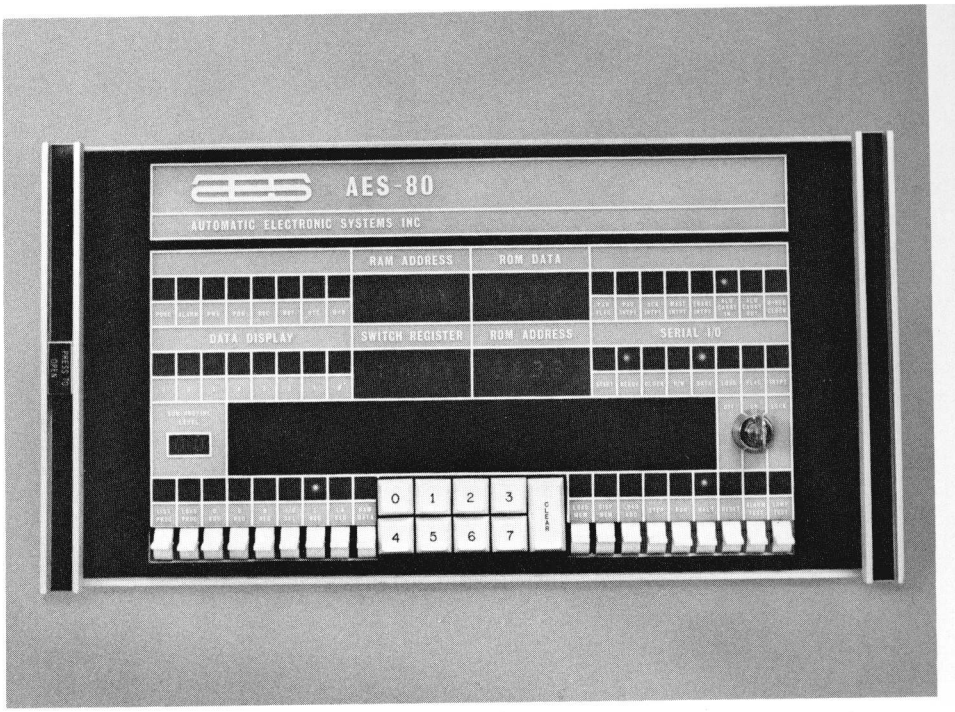
Support

Program Development and Control Console (PDCC)

A unique Program Development and Control Console is available for either program preparation and debugging prior to the "burning in" of a ROM or for passively monitoring an external microprocessor. The configuration used for program development is a microprocessor without ROM but including the interface card for the P.D.C.C. A second interface card is inserted in the Read Only Memory slot of the microprocessor and also connected to the P.D.C.C. Within the P.D.C.C. a high speed random access bipolar memory simulates the permanent ROM. Its contents, however, are alterable by loading instructions into it via the switch registers on the console, an ASR teletype, or a punched paper tape reader. The front panel of the P.D.C.C. contains a complete set of indicators, displays, switches, and controls for program development, including controls for program listing and tape loading.

When used to monitor a microprocessor installed in a larger system, the P.D.C.C. is primarily a passive display; active control is limited to halt, reset, single step and set command address. The microprogram is limited to fixed instruction in ROM unless read/ write memory is intermixed in the Instruction Memory.

A configuration of the P.D.C.C. which provides a convenient packaging arrangement for program development is one in which the microprocessor cards themselves are inserted in the P.D.C.C. The combined console is ideal for software development or for prototyping.



Program Development and Control Console (PDCC)

Software

A cross assembler is available for software development which allows programming the AES-80 in symbolic language. This cross assembler is itself written in Fortran II or assembler language. Input can be from paper tape, punched card, magnetic tape, or disc. Output consists of an object program on paper tape, a comprehensive listing, and diagnostics. The Fortran version can be executed on any computer with 8K of core and a Fortran compiler; the assembler version is designed for one of the more popular minicomputers with 4K of memory.

A self assembler is available for execution on the Program Development and Control Chassis equipped with a 4K x 16-bit external memory. This configuration permits complete program development in assembler language. No other computer facilities are required.

Once a program is debugged a Truth Table generator is used to generate a truth table for every block of 256 words of ROM permitting easy manufacture of the permanent ROM.

AES-80 Specifications

Characteristics

- general purpose, 8 bit, byte oriented, programmable digital microprocessor
- serial I/O — up to 1 character every 9.12 microseconds
- parallel I/O — on data memory bus at internal processor speeds.
- physically and functionally expandable with Modular System Units

Memory

- 8 bit data memory, 12 bit instruction memory
- either memory available with 1 to 16 256 word modules intermixed from the following types:
  1 - Bipolar read/write — 240 nsec cycle time
  2 - Random Access read/write Core — 1 microsecond cycle time
  3 - MOS random access read/write memory—2 microsecond cycle time
  4 - Bipolar Read Only Memory — 240 nsec cycle time
  5 - Capacitive Read Only Memory — 240 nsec cycle time
  6 - Special purpose
  7 - Other

Serial I/O

- 8 address lines, 1 read/write line, 1 load strobe line, 3 I/O clock lines,
  1 flag status line, 1 interrupt flag,
  1 IAK line, 1 serial data line, and
  1 power on pulse line.
- automatic I/O of 8 bit data stream
- serial I/O can address 256 devices

Parallel I/O

12 address line, 8 I/O data lines,
1 write strobe, 1 read enable,
1 interrupt flag, 1 device ready flag,
1 interrupt line and 1 power on pulse line.

Instruction Set

ALU mode instructions	20
Data bus instructions	4
RAM address instructions	3
Accumulator instructions	4
Register instructions	6
Branch instructions	23
I/O instructions	16
Other instructions	16
TOTAL	92

Environment

0 to 70° C

Dimensions

- MSU backplane 5.25 x 8.5 inches
- Insertable PC boards 7.5 x 7.5 inches
- PDCC 19″W x 8.75H x 17″D

Power

9 amps maximum at 5 VDC for complete microprocessor with 1K x 8 Bipolar RAM and 1K x 12 Bipolar ROM.

Automatic Electronic Systems Inc.
5455 Pare Street
Montreal 309, P. Quebec, Canada
(514) 735-6581

AES Data Inc.
P.O. Box 143
St. Albans, Vermont 05478
(802) 524-3660

Printed in Canada

AUTOMATIC ELECTRONIC SYSTEMS INC

AES 8Ø STANDARD PRICE LIST

CODE	DESCRIPTION	PREREQUISITE COLUMN	PRICE
	This list gives prices for the AES-8Ø Microprocessor system, FOB St. Albans, Vermont. Prices are quoted for unit quantity purchase before OEM volume discounts. Prices are subject to revision without notice. The prices are a condensation of equipment available; the factory should be consulted for options and equipment needed that are not listed.		
	AES-8Ø MICROPROCESSOR		
8Ø-Ø1	Basic microprocessor including prewired backplane with 9 PC Board & 3 I/O connectors, and 3 timing and control PC Boards.	-	950.00
	INSTRUCTION MEMORY		
8Ø-1Ø-1	Bipolar ROM (256 x 12 bits) field programmable, 24Ø nanosecond cycle time, PC Board mounted.	8Ø-Ø1	350.00
	One time charge/program for above.		150.00
8Ø-1Ø-2	Bipolar ROM (512 x 12 bits) field programmable, 24Ø nanosecond cycle time, PC Board mounted.	8Ø-Ø1	640.00
	One time charge/program		300.00
8Ø-1Ø-3	Bipolar ROM (768 x 12 bits) field programmable, 24Ø nanosecond cycle time, PC Board mounted.	8Ø-Ø1	920.00
	One time charge/program		450.00

AUTOMATIC ELECTRONIC SYSTEMS INC

AES 8Ø STANDARD PRICE LIST

CODE	DESCRIPTION	PREREQUISITE COLUMN	PRICE
	INSTRUCTION MEMORY		
8Ø-1Ø-4	Bipolar ROM (1Ø24 x 12 bits) field programmable, 24Ø nanosecond cycle time, PC Board mounted.	8Ø-Ø1	1,210.00
	One time charge/program		600.00
8Ø-11-1	Capacitive ROM (1Ø24 x 12 bits), 24Ø nanosec cycle time.	8Ø-Ø1	585.00
	Masking charge/program		195.00
	Revisions of data mask (each board)		40.00
8Ø-11-2	Capacitive ROM (2Ø48 x 12 bits) 24Ø nanosec cycle time.	8Ø-Ø1	680.00
	Masking charge/program		350.00
	Revision of data mask (each board)	8Ø-Ø1	80.00
	DATA MEMORY		
8Ø-2Ø-1	Bipolar Random Access Memory (256 x 8 bits), 24Ø nanosecond cycle time.	8Ø-Ø1	255.00
8Ø-2Ø-2	Bipolar Random Access Memory (512 x 8 bits), 24Ø nanosecond cycle time.	8Ø-Ø1	445.00
8Ø-2Ø-3	Bipolar Random Access Memory (768 x 8 bits), 24Ø nanosecond cycle time.	8Ø-Ø1	640.00
8Ø-2Ø-4	Bipolar Random Access Memory (1Ø24 x 8 bits), 24Ø nanosecond cycle time.	8Ø-Ø1	830.00
8Ø-21-1	MOS Random Access Memory (1Ø24 x 8 bits), 1 microsecond cycle time.	8Ø-Ø1	415.00

AUTOMATIC ELECTRONIC SYSTEMS INC

AES 8Ø STANDARD PRICE LIST

CODE	DESCRIPTION	PREREQUISITE COLUMN	PRICE
	DATA MEMORY		
8Ø-22-1	Core Memory Random Access memory, (1Ø24 x 8 bits), 1 micro-second cycle time.	8Ø-Ø1	880.00
	DIGITAL INPUT/OUTPUT		
8Ø-Ø2	Digital I/O Modular System Unit including prewired backplane and differential bus interface card with capacity for 8 I/O boards.	8Ø-Ø1	550.00
8Ø-Ø2-1	16 input board with transient protection filters, optoelectronic isolation and signal conditioning.	8Ø-Ø2	280.00
8Ø-Ø2-2	16 output board including opto-electronic isolation, over-voltage protection and 2ØØ milliamp source and sink capability.	8Ø-Ø2	280.00
8Ø-Ø2-3	8input/8output board including opto-electronic isolation on all points.	8Ø-Ø2	280.00
	COMMUNICATION		
8Ø-Ø2-4	Modem I/O with RS232 interface for control of 1 low speed modem.	8Ø-Ø2	200.00
8Ø-Ø2-5	Low speed modem card, Ø-18ØØ baud, asynchronous.	8Ø-Ø2-4	595.00
	ANALOG INPUT/OUTPUT		
8Ø-Ø3	Multiplexed high level analog input modular system unit including prewired backplane and bus interface board with capacity for 2 A/D subsystems.	8Ø-Ø1	550.00
8Ø-Ø3-1	A/D converter with dual slope integration, 1 board per subsystem.	8Ø-Ø3	590.00

AUTOMATIC ELECTRONIC SYSTEMS INC

AES 8Ø STANDARD PRICE LIST

CODE	DESCRIPTION	PREREQUISITE COLUMN	PRICE
	ANALOG INPUT/OUTPUT		
8Ø-Ø3-2	A/D timing and control, 1 board per subsystem.	8Ø-Ø3-1	200.00
8Ø-Ø3-3	A/D multiplexer, 16 channel differential, solid state, 1 or 2 boards per subsystem.	8Ø-Ø3-1 8Ø-Ø3-2	390.00
	MSU CHASSIS		
8Ø-Ø4	19" chassis to accept 3 modular system units with power supply.	8Ø-Ø1	825.00
	PROGRAM DEVELOPMENT AND CONTROL		
8Ø-3Ø	Console for system monitoring including display panel, power supply and maintenance logic.		2,540.00
8Ø-31	Program development console including the above 8Ø-3Ø system plus logic and a 512 x 12 bit ROM simulator.		3,990.00
8Ø-32	Program development console including the above 8Ø-31 system plus an internal microprocessor with self assembly capability, 2K x 12 ROM simulator, 1K x 8 data memory.		8,700.00
8Ø-31-1	Additional ROM simulator memory 512 x 12 bits.	8Ø-31	670.00
8Ø-31	Additional 4K x 16 MOS memory.	8Ø-32	2,000.00
	TELEPRINTERS		
8Ø-4Ø	33 ASR teletype machine, 1Ø char/sec, with paper tape reader and punch.	8Ø-Ø2 8Ø-3Ø	1,500.00
8Ø-41	Teletype modification kit	-	175.00

AUTOMATIC ELECTRONIC SYSTEMS INC

AES 8Ø STANDARD PRICE LIST

CODE	DESCRIPTION	PREREQUISITE COLUMN	PRICE
	TELEPRINTERS		
8Ø-42	33 Teletype and/or high speed paper tape reader interface.	8Ø-4Ø	225.00
8Ø-43	RS 232 C teleprinter and/or high speed paper tape reader interface.	-	225.00
8Ø-44	High speed paper tape reader assembly, 75 char. per second.	-	495.00

AES-80 Microprocessor OEM Discount Provisions

DISCOUNT TERMS

AES products not subject to discount are normally indicated on AES' price list and include: spare parts, software and peripheral equipment not manufactured by AES.

The price of each discountable product type, under these terms, is computed on a non-accumulative basis as purchase orders are received. The placement of additional orders does not reduce the price of previously received orders.

Deliveries will only be scheduled upon receipt of a duly executed Purchase Order or release from Buyer. Any addition to a given configuration shall be on a separate order and may result in a delay in the scheduled delivery date.

DISCOUNT SCHEDULE

NO. of Units		Discount %
1		10
2		15
3 - 5		19
6 - 9		23
10 - 14		26
15 - 19		29
20 - 29		31
30 - 49		34
50 - 74		36
75 - 99		37
100 - 149		38
150 - 199		39
200 - 499		40
500 - 999		45
1000 OR +		50

DISCOUNT FORFEITURE

Discounts under this agreement will be forfeited by the Buyer with respect to equipment for which payment is not received by AES within thirty (30) days after delivery.

Automatic Electronic Systems Inc.
5455 Pare Street
Montreal 309, P. Quebec, Canada
(514) 735-6581

AES Data Inc.
P.O. Box 143
St. Albans, Vermont 05478
(802) 524-3660

AES 80

DATA MEMORY REFERENCE INSTRUCTIONS

A=### 2000 TO 3777

01.	.AD	DRE	SS.

AL=D	FE 0605
AH=D	FF 0606
A=A+1	F: 0672
M=D	FL 0614

INSTRUCTION MEMORY REFERENCE INSTRUCTIONS

2ND WORD FORMAT

1..	.AD	DRE	SS.

JUMPS

JMP	B@ 0200
JSR	F0 0660

RET (NO ADDR.) FN 0616

CONDITIONAL JUMPS

TEST	JIS	JIC
ALM	BA 0201	@A 0001
IOR	BB 0202	@B 0002
BR7	BC 0203	@C 0003
CRY	BD 0204	@D 0004
D=B	BE 0205	@E 0005
RTC	BF 0206	@F 0006
IOD	BG 0207	@G 0007
RBF	BP 0220	@P 0020
SIN	BQ 0221	@Q 0021
SFL	BR 0222	@R 0022
PIN	BS 0223	@S 0023
PFL	BT 0224	@T 0024
INT	BU 0225	@U 0025
PWR	BV 0226	@V 0026
PDS	BW 0227	@W 0027

DATA BUS BIT TEST

JIS, DB# 0210 TO 0217

000	010	001	...

JIC, DB# 0010 TO 0017

000	000	001	...

PAGE CHANGE

PG=0	DT 0424
PG=1	FT 0624

A.L.U. INSTRUCTIONS

LOADING

F=D	L@ 1400
F=D'	LP 1420
F=B	LZ 1432
F=B'	LU 1425
F=-1	LC 1403
F=0	LS 1423

LOGIC #=OR .=AND ↑=XOR

F=D#B	LA 1401
F=D#B'	LB 1402
F=D'#B	LX 1430
F=D'#B'	LT 1424
F=D.B	L[1433
F=D.B'	LW 1427
F=D'.B	LR 1422
F=D'.B'	LQ 1421
F=D↑B	LV 1426
F=D↑B'	LY 1431

ARITHMETIC

F=D+D	LL 1414
F=D+B	LI 1411
F=D+D+1	L, 1454
F=D+B+1	L) 1451
F=D+1	L 1440
F=D-B	L& 1446
F=D-B-1	LF 1406
F=D-1	LO 1417

COMBINED

F=D#B+D	LM 1415
F=D#B'+D	LN 1416
F=D#B+1	L! 1441
F=D#B'+1	L" 1442
F=D#B+D+1	L- 1455
F=D#B'+D+1	L. 1456
F=D.B+D	LH 1410
F=D.B'+D	LD 1404
F=D.B+D+1	L(1450
F=D.B'+D+1	L$ 1444
F=D.B-1	LK 1413
F=D.B'-1	LG 1407
F=D#B+D.B'	LE 1405
F=D#B'+D.B	LJ 1412
F=D#B+D.B'+1	L% 1445
F=D#B'+D.B+1	L* 1452

SHIFT-ROTATE

F=BSL	LL 1414
F=BRL	ML 1514
EBR	N@ 1600

B-REGISTER INSTRUCTIONS

B=0	FH 0610
B=F B=BRR	F! 0611
B=FH	FJ 0612
B=FL	FK 0613

DATA BUS INSTRUCTIONS

D=L	F@ 0600
D=M	FA 0601
D=U	FB 0602
D=B	FC 0603

L & U REGISTERS INSTRUCTIONS

L=### 1000 TO 1377

001	0..	...	...

U=0	FG 0607
U=U#D	FD 0604

I/O INSTRUCTIONS

SERIAL I/O

CLK=0	DU 0425
CLK=1	FU 0625
LD=0	DV 0426
LD=1	FV 0626
R/W=R	DW 0427
R/W=W	FW 0627

CHL=## 07000 0737

000	111	0..	...

RG=# 06300 0637

000	110	011	...

RG=B	FM 0615
SIO	F0 0617

INTERRUPT

IAK=0	DR 0422
IAK=1	FR 0622
DIN	DQ 0421
EIN	FQ 0621
RBC	FP 0620
EBC	DP 0420
RST	F8 0670

HALT

HLT=## 0640 TO 0657

000	110	1..	...

NO OPERATION

NOP	@@ 0000