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RECOMP II

Autonetics Division

North American Aviation, Inc.

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SUMMARY REPORT: RECOMP II

.1 AVAILABILITY

RECOMP II is a small scientific computer system that was manufactured from 1958 to 1963 by the Autonetics Division of North American Aviation, Inc. Autonetics announced the discontinuance of manufacture of the RECOMP line of computers on April 24, 1963. A total of approximately 120 RECOMP II computers were manufactured.

Autonetics states that a limited number of used RECOMP II systems are currently available for either lease or purchase. Prices for used RECOMP II's will be quoted upon request to prospective customers. Autonetics is continuing to provide maintenance and "limited software support" for installed RECOMP systems.

.2 HARDWARE

RECOMP II is a fully-transistorized desk-size computer designed primarily for low-volume scientific applications. Paper tape is the basic input-output medium, but a card reader/punch, up to four slow magnetic tape units, and a digital plotter can be added if desired. Despite the close hardware similarity between the RECOMP II and the later RECOMP III (page 162:011.100), there is no direct program compatibility between the two systems.

RECOMP II's 40-bit word size — unusually long for computers in this class — provides about 12 decimal digits of precision. Each word can contain two instructions or one fixed-point operand. Floating-point numbers are represented by pairs of words.

All internal storage is provided by a single magnetic disc. The disc contains 70 tracks served by fixed read and write heads. Sixty-four tracks form the 4,080-word Main Memory, two "recirculating" tracks form a 16-word Fast Memory, and the remaining four tracks are used for special registers. The disc revolves at about 3,500 rpm, so the average access time to Main Memory is about 8.5 milliseconds. Each 8-word Fast Memory track has two read heads and one write head; maximum Fast Memory access times are 1.1 milliseconds for reading and 2.2 milliseconds for writing. A special instruction permits eight-word data transfers between Main Memory and Fast Memory. No parity checking is performed upon transfers to or from the disc.

The Central Processor operates in the binary mode on either fixed-point or floating-point operands. The instruction structure is one-address, but because the 20-bit instructions are accessed from the disc in pairs, a pseudo one-plus-one addressing scheme (in which the second instruction of each pair is an unconditional transfer to the next instruction pair) can be used to increase execution speeds by minimizing disc rotational delays.

The instruction repertoire is well-designed for most scientific computations. It includes a full complement of arithmetic operations — including square root — in both fixed-point and floating-point modes. There are, however, no facilities for indexing or indirect addressing. Instructions in typical programs are executed at the rate of about 50 to 200 per second.

Decimal-to-binary conversion for input data is automatic, but binary-to-decimal conversion for output operations requires a special subroutine which is rather slow. Some 40 basic subroutines have been provided to handle a variety of four-, five-, and six-bit input-output codes, but the output operations are awkward.

Simultaneous operations cannot be performed in RECOMP II systems; the Central Processor is interlocked during all input-output operations.

The standard input-output devices are a 400-character-per-second paper tape reader, a 20-character-per-second paper tape punch, and a 10-character-per-second typewriter, all of which are supplied with the basic RECOMP II system. The basic tape reader and punch use 5-channel tape and the Baudot code, so no parity checking can be performed, although echo checking is used to verify the punching operation. The console typewriter is a modified IBM unit that can be used for both keyboard input and printed output. A convenient desk-top Console Unit provides a digital display of data in selected registers or storage locations.

Other peripheral equipment that can be used with RECOMP II systems includes: a Facitape Console containing a 600-character-per-second paper tape reader and a 150-character-per-second paper tape punch; a Connector unit that permits an IBM 24 or 26 Card Punch to be used for low-speed card input and/or output; a digital X-Y plotter; and up to four low-speed magnetic tape units. Peak data transfer rate for the magnetic tape units is 1,850 characters per second, and Autonetics considers them to be more useful for auxiliary storage than for conventional input-output purposes. The Facitape paper tape units can accommodate tape

.2 HARDWARE (Contd.)

with 5, 6, 7, or 8 channels; they provide higher speeds and more flexibility than the basic Autonetics paper tape units.

.3 SOFTWARE

A fairly wide range of software facilities is available, a large proportion of which has been prepared by individual RECOMP II users. An interpretive system, RAFT IV, provides a simple machine-oriented language for limited engineering applications; the structure of the language is quite similar to the type of instructions given to operators of desk calculators, so RAFT IV is well-suited for open-shop operations. SCOPAC is an algebraic compiler language that is closely related to FORTRAN, but SCOPAC lacks FORMAT and library facilities, holds all variables in floating-point form, and cannot handle arrays of more than two dimensions. Several other compilers and assemblers have been developed for the RECOMP II, but they are less widely used than RAFT IV and SCOPAC.

The RECOMP II program library contains routines for various engineering and mathematical applications using both fixed-point and floating-point arithmetic.

Despite the various software programming systems available to RECOMP II users, machine-language programming is common because the computer is relatively straightforward and easy to program. Autonetics estimates that 80 percent of all user programs are written in machine language. RECOMP II's simplicity and ease of programming make it suitable for use as a training device to teach digital computer principles and programming.

PRICE DATA: RECOMP II

The rental and purchase prices shown below were those in effect for new RECOMP II equipment while it was in production. Autonetics states that current prices for used RECOMP II equipment will be quoted upon request to prospective customers.

The monthly maintenance charges shown below are those currently in effect; they cover a preventative maintenance program plus all parts and labor necessary to maintain the equipment in good operating condition. As an alternate plan, Autonetics will supply maintenance service on a call-to-call basis for a fixed price per day, plus parts and transportation.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR	D4A-AB	RECOMP II Standard System	2,495	550	95,000
	D4G-AB	RECOMP II Magnetic Tape System	2,795	550	99,850
		Either system includes 4,080-word Main Memory, 16-word Fast Memory, Central Console and Display, Console Typewriter, 400-cps Paper Tape Reader, and 20-cps Paper Tape Punch.			
STORAGE		Included in basic system, above.			
INPUT-OUTPUT	AFPC	Facitape Console, including 600-cps Paper Tape Reader and 150-cps Paper Tape Punch	500	100	16,950
	D4K	Connector for IBM 24 or 26 Card Punch (for card input/output)	150	30	4,250
	M906II	Magnetic Tape Unit	625	125	25,000
	D4H	X-Y Digital Plotter	220	45	5,450
	-	Consolette (required for above I/O devices)	50 per unit connected	10	3,800
	225	Versatape II (off-line 10-key paper tape preparation unit)	100	20	2,500
	266	Computeriter	100	20	2,600

RECOMP III

Autonetics Division

North American Aviation, Inc.

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SUMMARY REPORT: RECOMP III

.1 AVAILABILITY

RECOMP III is a small scientific computer system that was manufactured from 1961 to 1963 by the Autonetics Division of North American Aviation, Inc. Autonetics announced the discontinuance of manufacture of the RECOMP line of computers on April 24, 1963. A total of approximately 60 RECOMP III computers were manufactured.

Autonetics states that a limited number of used RECOMP III systems are currently available for either lease or purchase. Prices for used RECOMP III's will be quoted upon request to prospective customers. Autonetics is continuing to provide maintenance and "limited software support" for installed RECOMP systems.

.2 HARDWARE

RECOMP III is a fully-transistorized desk-size computer designed for low-volume scientific applications. The basic input-output device is a 10-character-per-second Flexowriter, although faster paper tape input-output equipment is available. Despite the fact that RECOMP III was designed as an "economy model" of the earlier RECOMP II (page 161:011.100), there is no direct program compatibility between the two RECOMP systems because of significant differences in their instruction repertoires and data formats.

RECOMP III's 40-bit word size — unusually long for computers in this class — provides about 12 decimal digits of precision for fixed-point operands. Floating-point numbers are represented by an 8-bit exponent, a 31-bit fraction, and a sign bit. Each RECOMP III word can contain two 20-bit instructions or one fixed-point or floating-point operand (whereas RECOMP II uses two words to hold each floating-point operand).

All internal storage is provided by a single magnetic disc. The disc contains 70 tracks served by fixed read and write heads. Sixty-four tracks form the 4,080-word Main Memory, two "recirculating" tracks form a 16-word Fast Memory, and the remaining four tracks are used for special registers. The disc revolves at about 3,500 rpm, so the average access time is about 8.5 milliseconds to Main Memory and 1.1 milliseconds to Fast Memory. A special instruction permits eight-word data transfers between Main Memory and Fast Memory. No parity checking is performed upon transfers to or from the disc.

The Central Processor operates upon fixed-point binary operands. Floating-point arithmetic is a hardware option; if the optional feature is not installed, its facilities can be simulated (at a considerable reduction in speed) by a standard software package. The instruction structure is one-address, but because the 20-bit instructions are accessed from the disc in pairs, a pseudo one-plus-one addressing scheme (in which the second instruction of each pair is an unconditional transfer to the next instruction pair) can be used to increase speeds by minimizing disc rotational delays.

The RECOMP II instruction repertoire is well-designedfor most scientific computations, although it lacks some of RECOMP II's convenient but costly facilities such as built-in square root and decimal-to-binary conversion. One index register is available, but it can be referenced only by the second instruction of each instruction pair. Instructions in typical programs are executed at the rate of about 50 to 200 per second.

All editing and radix conversion operands must be programmed, and standard subroutines are available to facilitate them. Any code of 5 to 8 bits can be used for input and output operations, but every data character is handled as though it contained eight data bits; characters are packed five to a 40-bit word.

There are no facilities for simultaneous input-output operations, and only a limited amount of overlapping of Flexowriter and Central Processor operations is possible.

The standard RECOMP III input-output device is a Friden Flexowriter, which is an electric typewriter with an integrated paper tape reader and punch. The Flexowriter provides keyboard or paper tape input and printed or punched output, all at a rated speed of 10 characters per second. Paper tape with 5, 6, 7, or 8 channels can be used. The Flexowriter's low speed and uncertain reliability make the basic RECOMP III configuration suitable only for applications whose ratios of input-output to computational volume are very low.
The standard Flexowriter can be augmented by faster Facitape paper tape input-output units. The Facitape reader has a rated speed of 600 characters per second and a maximum effective speed of 285 characters per second when used with a RECOMP III. The Facitape

.2 HARDWARE (Contd.)

punch, rated at 150 characters per second, achieves a maximum speed of about 90 characters per second in RECOMP III systems. The Facitape reader can be used as an independent unit, or the reader and punch can be combined in a Facitape Console.

Also available for use with RECOMP III systems are a digital X-Y plotter and a Connector unit that permits an IBM 24 or 26 Card Punch to be used for low-speed (20 columns per second maximum) card input and/or output.

.3 SOFTWARE

RECOMP III is a relatively straightforward, easy-to-program computer, so many user programs are written in machine language. The RECOMP III program library contains an assortment of input-output control routines and mathematical functions to simplify machine-language programming.

An interpretive system called RIP-3000 permits the RECOMP III to be programmed as if it were an even more convenient — but slower — pseudo-computer with built-in floating-point arithmetic, radix conversions, and mathematical functions. RIP-3000 provides a convenient coding language, but the instructions are executed interpretively at a rate of only about 12 instructions per second.

Also available for the RECOMP III are a FORTRAN II compiler and NUCOM, a numerical control compiler that generates control tapes for a variety of machine tools.

PRICE DATA: RECOMP III

The rental and purchase prices shown below were those in effect for new RECOMP III equipment while it was in production. Autonetics states that current prices for used RECOMP III equipment will be quoted upon request to prospective customers.

The monthly maintenance charges shown below are those currently in effect; they cover a preventative maintenance program plus all parts and labor necessary to maintain the equipment in good operating condition. As an alternate plan, Autonetics will supply maintenance service on a call-to-call basis for a fixed price per day, plus parts and transportation.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR		RECOMP III Computer, including: 4,080-word Main Memory, 16-word Fast Memory, Console, and Flexowriter	1,495	425.00	65,000
		Floating-Point Arithmetic (optional)		41.66	
STORAGE		Included in basic system, above			
INPUT-OUTPUT		Facitape Paper Tape Reader	125	25.00	4,750
		Facitape Console, including 600-cps Paper Tape Reader and 150-cps Paper Tape Punch	500	100.00	16,950
		Connector for IBM 24 or 26 Card Punch (for card input/output)	75	30.00	2,625
		X-Y Digital Plotter	195	45.00	4,950
		Flexowriter for remote operation (inquiry station)	260	50.00	5,650
		One additional input plug (for optional or special devices; 3 max.)	25	5.00	750
		One additional output plug (3 max.)	25	5.00	750

BURROUGHS B 200 SERIES

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CONTENTS

INTRODUCTION

.1 SUMMARY

The B 100/200/300 Series designates a group of three similar, small-to-medium-scale, business-oriented computer systems manufactured by Burroughs Corporation. The original entry in the Series was the B 200 line of computer systems, first delivered in October 1962. The B 200 Series provided 4,800 characters of core storage and a memory cycle time of 10 microseconds. Peripheral device flexibility was limited to punched card, line printer, MICR document, magnetic-striped ledger card, and magnetic tape input-output units. Buffered card reading, punching, and line printing were offered as standard features.

Fourteen months later the B 200 Series was significantly improved: memory cycle time was reduced to 6 microseconds; the instruction repertoire was increased from 37 to 49; 4,800 additional characters of core storage were offered; and paper tape, disk file, and data communications peripheral facilities were added. The upgraded systems were designated as "level threes", such as the B 263 and B 283 computer systems, and the original 10-microsecond systems were reduced in price and presented to the market as the economy B 100 Series. Previously-announced peripheral devices, such as the card reader, MICR sorter-reader, and line printer, were offered in new models with lower speeds and prices to meet the needs of the low-priced B 100 Series market.

The next major announcement by Burroughs occurred in May 1964, when the B 370 System for banking applications was released. The B 370 System included a 16-pocket MICR Sorter-Reader and up to 3 high-speed multiple tape listers. The first stirrings of a revamped marketing policy were perceptible when the B 370 central processor was offered with modular control and instruction features; the power and flexibility of the central processor could be tailored in price and performance to individual customer requirements.

In February 1965, more peripheral devices were announced — high-speed models such as a 1,400-card-per-minute reader and a 1,040-line-per-minute printer. Concurrently, further design improvements were incorporated into the B 200 "level three" central processor, and the B 300 Series was officially born. Emphasizing modularity, the B 300 Series was publicized to include under one title all possible system configurations, including the archetype B 370 system. The capability to add 9,600 more characters of core storage, for a Series maximum of 19,200 characters, became possible, and several new and powerful instruction options were unveiled. The memory cycle time of 6 microseconds, however, was not further improved in the new processor.

Thus, today's B 100/200/300 Series offers a wide range of peripheral devices that can be connected, with few restrictions, to two basic central processors with cycle times of 10 or 6 microseconds and with core storage capacities of 4,800, 9,600, or 19,200 characters. Monthly rental rates can vary from $2,500 for a B 100 Series card system to $20,000 for a B 300 Series system with extensive random access disk file and data communications capabilities. A wide variety of proven software is available to facilitate the programming of business applications. (The limited core storage and lack of floating-point arithmetic make the B 100/200/300 Series systems unsuitable for most scientific applications.)

In this Introduction, several significant topics are discussed, as listed below. The true scope of the B 100/200/300 Series can be best understood if each area of discussion is read. However, the topics that follow can be read separately if desired.

.2 CENTRAL PROCESSORS

The B 100/200/300 Series offers two basic central processors, with memory cycle times of 10 and 6 microseconds. All B 100 central processors have the slower cycle time, and all B 300's have the faster time. The B 200 central processor can be ordered with either cycle time. B 100 Series core storage capacity is limited to 4,800 characters, but the capacity of the 6-microsecond B 200/300 processors can be increased to 9,600 or 19,200 characters.

Each B 100/200/300 Series central processor is a character-oriented unit containing core storage facilities, an arithmetic and control unit, two input buffers, one output buffer, and an integrated console. Each instruction has a fixed length of 12 characters and is divided into an operation code, two variant characters, and three 3-character addresses. Operand lengths can vary from 1 to 12 characters and are specified in the individual instructions; no "word marks" are required in the data fields. Instructions in typical routines are executed at the rate of about 1,800 per second in the B 200/300 6-microsecond central processor.

The instruction list includes a full complement of decimal arithmetic and comparison operations as well as automatic editing facilities. Multiply and divide instructions are standard. There are no index registers and no indirect addressing facilities, but all B 200/300 central processors include an address modification instruction to increment individual operand addresses. Among the instructions recently added to the Series with the advent of the B 300 central processor are Transfer and Translate, Unit Interrogate, Transfer and Branch, Data Compress and Expand, and Binary Card Read and Punch.

All B 100/200/300 Series input-output operations are buffered except those involving magnetic tape, the ledger-card processor, and the disk file. Instruction execution by the central processor is inhibited for the duration of the latter three types of operations, with the exception of magnetic tape rewinding. Card reading and punching, paper tape reading and punching, printing, MICR sorter-reader input, and data communications operations can proceed in parallel with each other and with internal processing.

Computer system designations within the B 100 and B 200 Series are determined by the class of input-output controllers that must be added to the central processor in order to satisfy configuration requirements. For example, punched card configurations without magnetic tape or MICR facilities utilize B 160, B 260, or B 263 systems; MICR/magnetic tape operations demand B 170, B 270, or B 273 systems; and if magnetic tape is desired without MICR capabilities, then a B 180, B 280, or B 283 system is required. The MICR and ledger-card processing Visible Record Computer (VRC) is controlled by a B 250 or B 251 central processor.

The B 300 central processor is a single model designed to function with any available peripheral unit, provided that the appropriate, separately-priced input-output control module is added either at the time of manufacture or in the field.

.3 PERIPHERAL UNITS

The principal peripheral units available with the B 100/200/300 Series are listed in Table I along with their chief characteristics. A complete list of peripheral devices, indicating model numbers and performance data, is provided in the Price Data section of this report, page 201:221.101. The configuration possibilities for the B 100 Series are limited to one card reader, one card punch, one MICR sorter-reader, one line printer or multiple tape lister, and up to four magnetic tape units. The B 250/251 central processors are the only ones capable of controlling the B 401 Ledger Processor. The B 200 Series 10-microsecond central processor permits the connection of two card readers or one card reader with one sorter-reader, one card punch, two line printers or multiple tape listers, and up to six magnetic tape units. The B 200 Series 6-microsecond central processor offers the additional capability of controlling one paper tape reader and punch, up to 50 Disk File storage modules, and up to 15 data communications terminal units. The still more comprehensive B 300 Series central processor can control all these peripheral devices, plus an additional 6-tape multiple tape lister.

Burroughs card readers offer speeds between 200 and 1,400 cards per minute. The line printers can operate at peak speeds ranging from 475 to 1,040 lines per minute. Top printing speed for the multiple tape listers is 1,600 numeric lines per minute on each of up to three listing tapes.

(Contd.)

TABLE I: PRINCIPAL B 100/200/300 SERIES PERIPHERAL UNITS

Peripheral Type	Model No.	Name	Characteristics
Punched Card Equipment	B 122 B 123 B 124 B 129 B 303 B 304	Card Reader Card Reader Card Reader Card Reader Card Punch Card Punch	Reads 200 cpm. Reads 475 cpm. Reads 800 cpm. Reads 1,400 cpm. Punches 100 cpm. Punches 300 cpm; has Stacker Select option.
Punched Paper Tape Equipment	B 141 B 341	Paper Tape Reader Paper Tape Punch	Reads 5, 6, 7, or 8 level tape at 500 or 1,000 char/sec. Punches 5, 6, 7, or 8 level tape at 100 char/sec.
Printers	B 320 B 321 B 329 B 326 B 332	Line Printer Line Printer Line Printer Multiple Tape Lister Multiple Tape Lister	Prints 475 lpm. Prints 700 lpm. Prints 1,040 lpm. Prints 1,200 numeric lpm. Prints 1,600 numeric lpm.
MICR Equipment	B 107 B 116	Sorter-Reader Sorter-Reader	Reads 1,200 documents/min; sorts to 13 pockets. Reads 1,560 documents/min; sorts to 16 pockets.
Magnetic Tape Units	B 421 B 422 B 423 B 424 B 425	Magnetic Tape Unit Magnetic Tape Unit Magnetic Tape Unit Magnetic Tape Unit Magnetic Tape Unit	Transfers data at 18 or 50KC. Transfers data at 24 or 66KC. Transfers Data at 24KC. Transfers Data at 66KC. Transfers data at 18, 50, or 72KC.
Random Access Storage	B 450 B 475	Disk File Basic Control Disk File Storage Module	Controls 9.6 to 480 million characters. Stores 9.6 million characters; 20 msec average access time.

.3 PERIPHERAL UNITS (Contd.)

The Burroughs magnetic tape units provide a range of transfer rates from 18,000 to 72,000 characters per second and packing densities of 200, 556, and 800 rows per inch. Data is recorded on 0.5-inch, 7-track magnetic tape, providing compatibility with the tape units used in IBM 1400 and 7000 Series systems. All magnetic tape operations (except rewinding) require the use of the central processor throughout the entire operation, so there is no read/compute, write/compute, or read/write simultaneity.

The Burroughs Disk File System is a modular storage system that combines high on-line storage capacity (up to 480 million characters) with rapid random access (20 milliseconds average). The rapid accessing is made possible by the use of a fixed read-write head serving each data track, which completely eliminates head-positioning delays and provides relatively high reliability. Peak data transfer rate is 100,000 characters per second. Prices are competitive with those of other currently-available mass storage systems whose average access times are 5 to 10 times as high.

An array of data communications devices can be attached to any B 200/300 Series central processor. Up to four such processors can share the same communications network, which can consist of up to fifteen terminal units of varying capacities. The B 481 Teletype Terminal Unit provides buffered interfacing for up to 399 remote teletype stations, the B 483 Typewriter Terminal Unit can control up to 8 typewriter inquiry stations, and the B 484 Terminal Unit regulates the use of up to 8 stations of the Dial TWX network. Burroughs has recently announced another terminal unit, the B 486 Central Terminal, to channel transmissions between the central processor and up to 96 remote Teller Consoles in its On-Line Banking System. All of the terminal units are buffered and can simultaneously accept inquiries from as many remote devices as their individual buffer sizes will accommodate. Buffer sizes are specified at the time of manufacture. An operating system to control the operations of a data communications network has been announced, with delivery expected in June, 1965.

.4 SOFTWARE

A wide variety of proven software is available for the B 100/200/300 Series. Most of the existing software is designed to be used with 4,800 characters of central processor core storage. As a result of this severe storage limitation, the software is characteristically simple and straightforward, and makes extensive use of multiple passes and phases.

The most important programs provided include a basic and an advanced symbolic assembler, a Compact COBOL compiler, tape and Disk File sorts, and report generators. A translator program is also provided to convert IBM 1401 SPS source-language programs into Burroughs symbolic assembly-language programs.

Burroughs has announced a full COBOL compiler for B 200/300 Disk File systems, with delivery expected by July, 1965. A Tape/Disk Operating System is anticipated for delivery in June, 1965.

Programs currently supplied by Burroughs include:

- Compact COBOL Compiler: Provides that group of language facilities that comprise the Compact COBOL subset of COBOL-61; designed for use with 4 magnetic tape units and 4,800 characters of core storage.
- Basic Assembler: A straightforward card or tape assembly program that provides one-for-one conversions from source code to machine language. There are no provisions for use of a program library, and only two macro instructions are permitted. The coding form makes use of coding-form page and line numbers for symbolic references. All elements of every instruction must be specified in every statement.
- Advanced Assembler I: An improved assembly program designed for use on B 200/300 Series magnetic tape systems. A system library can be utilized to call utility routines, diagnostics, error routines, and other subroutines that the user inserts himself. Seven macro instructions are provided, including tape and disk instructions that call forth and set linkages to their required error routines. Symbolic names and reusable program points can reference both data and instructions. Operand sizes, once described in the Data Division, need not be specified again in individual instructions.
- Sort Generator I: Generates magnetic tape sort programs within five minutes. Sort programs can be generated that utilize from 3 to 6 tape units. The object sort program operates within 4,800 characters of core storage.
- Generalized Three-Tape Sort: A multi-phase sort program modified according to the user's parameter cards; designed for use with 9,600 characters of core storage and three magnetic tape units.
- Disk File Sort Generator III: Generates object sort programs that utilize a Disk File for intermediate storage. Tag sorting is possible, enabling most sorts to be completed significantly sooner than would be the case with record sorting. Source and result files can be contained on either magnetic tape or Disk File.
- Report Generator I: Generates specially-tailored programs that process input from punched cards, magnetic tape, or Disk File and produce reports on either punched cards or line printer.
- Utility Routines: A variety of programs designed to handle data transcription, diagnostic, and file-maintenance operations using minimal equipment configurations.
- Demand Deposit Accounting Programs: A series of standard financial programs designed for use with the Visible Record Computer (B 250 or B 251) exclusively.
- Demand Deposit/Proof and Transit Financial Application Package: A series of programs written for banks that have 4 magnetic tape units and 4,800 characters of core storage. Complete documentation is included with the package.

(Contd.)

.4 SOFTWARE (Contd.)

- Installment Loan Financial Application Package: A group of programs that process MICR loan payments. All master file information is maintained on magnetic tape. Four tape units and 4,800 characters of core storage are required.

- Bond Analysis and Accounting Package: A series of programs that provide bond portfolio management with detailed analyses and evaluations of current and proposed bonds. A B 200/300 Series central processor is required for use of this program, as well as a card reader and line printer.

- On-Line Teller System: A thoroughly documented systems approach to on-line banking operations is provided; a complete operating system is not yet available.

- Flow Chart Generator: A program that generates detailed logic charts from Basic or Advanced Assembly Language source programs. The programmers' remarks, as punched into the source card, are printed in the symbol generated for each source statement. Three magnetic tapes are required to use the generator, in addition to a B 200/300 6-microsecond central processor with 4,800 positions of core storage.

.5 COMPATIBILITY WITH COMPETITIVE EQUIPMENT

Certain hardware options available with the improved B 200 and B 300 central processors provide some degree of input-output compatibility with other commercially-oriented computer systems. Binary card reading and punching are available, as well as the reading and punching of Bull and ICT card codes. Magnetic tapes can be read and written using any 6-bit binary code. Direct compatibility is possible between the Burroughs tape units and the IBM 729 and 7330 tape units.

The B 100/200/300 Series instruction code is not directly compatible with that of any other computer system. Burroughs has developed a program translator to convert IBM 1401 SPS source code into a source code acceptable to Burroughs assemblers, but the SPS Translator is too limited in scope to serve as a really productive tool in most conversion operations. Hardware dissimilarities that could not be circumvented within the 4,800 characters used by the SPS Translator program limit the candidates for effective translation to small and relatively basic IBM 1401 card and tape programs. Even so, some manual changes will usually be required before the translated program can be assembled and run.

.6 COMPATIBILITY WITHIN THE B 100/200/300 SERIES

The standard inclusion of many additional instructions in the B 200/300 6-microsecond central processor has made downward compatibility with the slower B 200 and B 100 Series systems almost impossible unless the use of these additional features is deliberately restricted. However, upward compatibility throughout the line is completely feasible. The great majority of the available peripheral devices can be used with any central processor in the Series, although in some cases a special input-output control module is a prerequisite.

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of location	Size	Purpose or use
Character:	6 bits + parity bit	alphamerics.
Block:	group of characters	magnetic tape record.
Input buffers:	80 characters (sorter-reader, 84 char)	store input for cards, paper tape, or sorter-reader.
Output buffer:	80 characters	store output for cards or paper tape.
Print buffer:	120 characters*	store output for printer.
Lister buffer:	44 characters	store output for lister.

.2 DATA FORMATS

Type of information	Representation
Letter:	1 character.
Numeral:	1 character.
Special symbol:	1 character.
Operand:	1 to 12 characters, as specified in instruction.
Instruction:	12 characters.
Block on tape:	any number of characters greater than 6.
Arithmetic operand:	1 to 12 characters.
Data for mask:	1 to 12 characters.
Edit mask:	1 to 24 characters.
Ledger stripe:	1 to 80 characters.
Line of print for Record Processor:	160 characters.
One MICR document:	84 characters in core storage.
Internal block for transfer:	1 to 132 characters.

* 132 characters for B 325 and B 329 printers.

SYSTEM CONFIGURATION

The following table shows the number of peripheral devices of each available type that can be connected to each of the central processor models in the B 100/200/300 Series. The next six pages show the components and prices of Burroughs systems in representative standard configurations, arranged in accordance with the specifications on page 4:030.120 of the Users' Guide.

TABLE OF PERMISSIBLE CONFIGURATIONS

PERIPHERAL UNITS	CENTRAL PROCESSOR MODEL										
	B 160	B 170	B 180	VRC	B 260	B 270	B 280	B 263	B 273	B 283	B 300
B 122 Card Reader	1	1	1	1	2	2	2	2	2	2	2
B 123 Card Reader	1	1	1	1	2	2	2	2	2	2	2
B 124 Card Reader	1†	1†	1†	1	2	2	2	2	2	2	2
B 129 Card Reader	0	0	0	0	0	0	0	2	2	2	2
B 141 Paper Tape Reader	0	0	0	0	0	0	0	2*	2*	2*	2*
B 102 Sorter-Reader	0	1†	0	1	0	1	0	1*	1	1*	1*
B 103 Sorter-Reader	0	1†	0	0	0	1	0	1*	1	1*	1*
B 104 Sorter-Reader	0	1†	0	0	0	1	0	1*	1	1*	1*
B 106 Sorter-Reader	0	1	0	1	0	1	0	1*	1	1*	1*
B 107 Sorter-Reader	0	1	0	0	0	1	0	1*	1	1*	1*
B 116 Sorter-Reader	0	0	0	0	0	1	0	1*	1	1*	1*
Note: Any combination of one sorter-reader and up to two paper tape and punched card readers, to a maximum of two units, can be connected to the two input buffers provided.											
B 303 Card Punch	1	1	1	1	1	1	1	1	1	1	1
B 304 Card Punch	1	1	1	1	1	1	1	1	1	1	1
B 341 Paper Tape Punch	0	0	0	0	0	0	0	1*	1*	1*	1*
Note: Either the B 303, B 304, or B 341 punch unit can be attached to the one output buffer provided.											
B 320 Line Printer	1	1	1	1	2	2	2	2	2	2	2
B 321 Line Printer	1†	1†	1†	1	2	2	2	2	2	2	2
B 325 Line Printer	0	0	0	0	0	0	0	2	2	2	2
B 328 Line Printer	0	0	0	1	2	2	2	2	2	2	2
B 329 Line Printer	0	0	0	0	0	0	0	2	2	2	2
B 322 Multiple Tape Lister	0	1†	0	1	2	2	2	2	2	2	2
B 323 Multiple Tape Lister	0	0	0	1	2	2	2	2	2	2	2
B 326 Multiple Tape Lister	1	1	1	1	2	2	2	2	2	2	2
B 332 Master Multiple Tape Lister	0	0	0	0	0	0	0	0	0	0	1
B 333 Slave Multiple Tape Lister	0	0	0	0	0	0	0	0	0	0	2
Note: Printers and Listers, which contain their own buffers, cannot operate on-line in combination with each other.											

† Adapter required for use with B 100 Series.
* Appropriate input-output control module required.

(Table continued overleaf)

TABLE OF PERMISSIBLE CONFIGURATIONS (Contd.)

PERIPHERAL UNITS	CENTRAL PROCESSOR MODEL										
	B 160	B 170	B 180	VRC	B 260	B 270	B 280	B 263	B 273	B 283	B 300
B 421 Magnetic Tape Unit	0	0	0	0	0	6	6	6*	6	6	6*
B 422 Magnetic Tape Unit	0	0	0	0	0	0	0	6*	6	6	6*
B 423 Magnetic Tape Unit	0	4	4	0	0	6	6	6*	6	6	6*
B 424 Magnetic Tape Unit	0	0	0	0	0	0	0	6*	6	6	6*
B 425 Magnetic Tape Unit	0	0	0	0	0	0	0	0	0	0	6*
Note: B 421 Tape Units cannot be used in combination with B 422 or B 423 tape units. All other combinations are permissible.											
B 401 Ledger Processor and Printer	0	0	0	1	0	0	0	0	0	0	0
B 495 Supervisory Printer	0	0	0	0	0	0	0	1*	1*	1*	1*
B 450 Basic Disk File/Data Communication Control	0	0	0	0	0	0	0	1	1	1	1
B 247 Disk File Control	0	0	0	0	0	0	0	1	1	1	1
B 451 Disk File Expanded Control	0	0	0	0	0	0	0	2	2	2	2
B 471 Disk File Electronics Unit	0	0	0	0	0	0	0	10	10	10	10
B 475 Disk File Storage Module	0	0	0	0	0	0	0	50	50	50	50
B 248 Data Communication Control	0	0	0	0	0	0	0	4	4	4	4
B 481 Teletype Terminal	0	0	0	0	0	0	0	15	15	15	15
B 483 Typewriter Terminal	0	0	0	0	0	0	0	15	15	15	15
B 484 Dial TWX Terminal	0	0	0	0	0	0	0	15	15	15	15
B 486 Central Terminal	0	0	0	0	0	0	0	0	0	0	15
Note: All 4 terminal units contain their own input-output buffers; up to 15 terminal units in any combination can be attached to a B 248 Data Communication Control.											
<u>Central Processor Optional Features</u>											
Sense Switches	0	0	0	0	0	0	0	0	0	0	6
Card Reader Early Release	0	0	0	0	0	0	0	1	1	1	1
Printer-Lister Selector Switch	0	1	0	0	0	1	0	1	1	1	1
Card Reader Busy Branch	0	0	0	0	1	1	1	1#	1#	1#	1#
132-Print Position Capability	0	0	0	0	0	0	0	1	1	1	1#

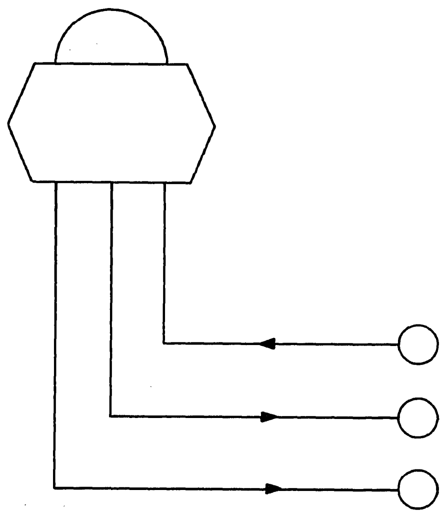
† Adapter required for use with B 100 Series.
* Appropriate input-output control module required.
\# Standard feature.

(Contd.)

AUERBACH

.1 TYPICAL CARD SYSTEM; CONFIGURATION I

Deviations from Standard Configurations: . . . . no index registers.
card reader is 20% slower.
card punch is 33% faster.

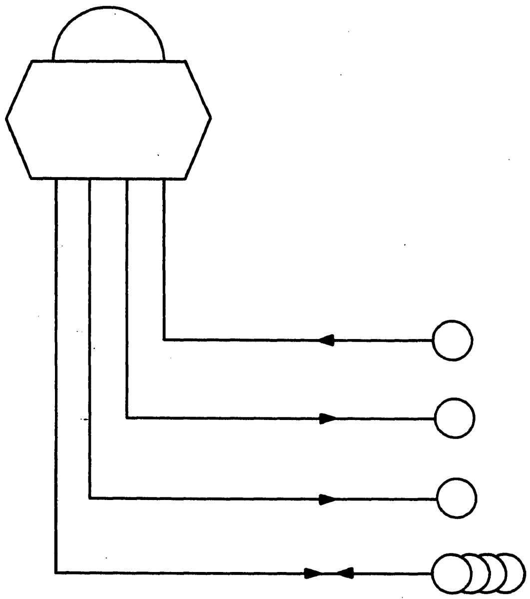


Equipment	Rental
Core Storage: 9,600 char.	$ 550
B 263 Central Processor and Console	1,600
Card Reader: 800 cards/min.	400
Card Punch: 300 cards/min.	650
Line Printer: 1040 lines/min.	1,325
TOTAL RENTAL:	$4,525

Note: A typical card system that uses slower peripheral devices (200-cpm reader, 100-cpm punch, and 475-lpm printer) and the B 100 Series 10-microsecond central processor (with only 4,800 positions of core storage) rents for $2,510 per month.

.2 4-TAPE BUSINESS SYSTEM; CONFIGURATION II

Deviations from Standard Configuration: . . . . magnetic tape is 60% faster.



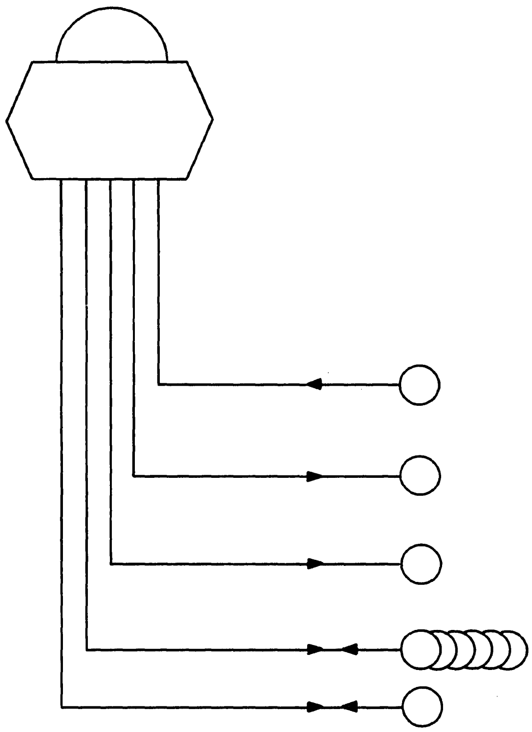
Equipment	Rental
Core Storage: 9,600 char.	$ 550
B 283 Central Processor and Console (tape and disk file capabilities are included)	1,785
Card Reader: 475 cards/min.	320
Card Punch: 100 cards/min.	450
Line Printer: 475 lines/min.	810
Magnetic Tape Units (4): 24,000 char/sec.	1,980
TOTAL RENTAL:	$5,895

Note: If this same configuration is used with a B 100 Series 10-microsecond central processor (providing only 4,800 positions of core storage), the monthly rental is $4,590.

(Contd.)

.3 6-TAPE BUSINESS SYSTEM; CONFIGURATION III

Deviations from Standard Configuration: . . . . no index registers.
console typewriter input is included.
magnetic tape is up to 67% faster.

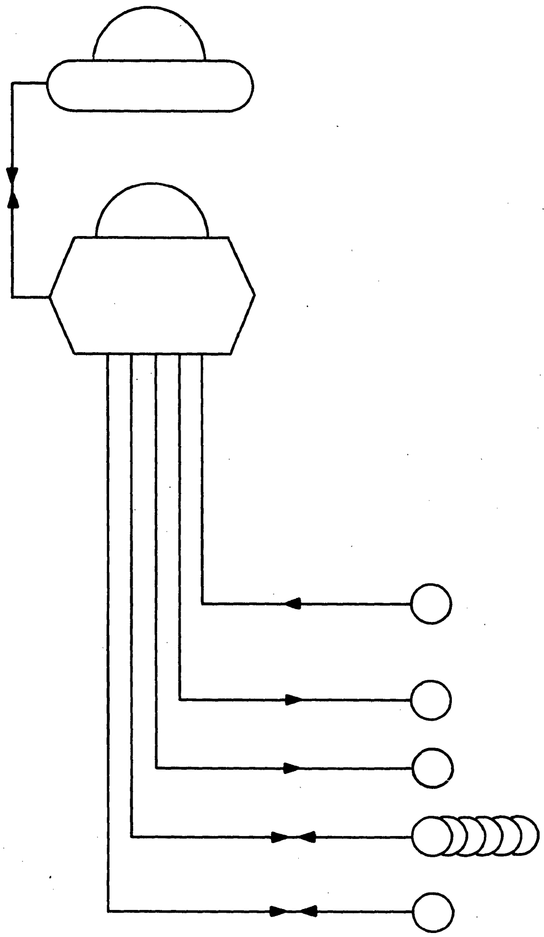


Equipment	Rental
Core Storage: 19,200 char.	$ 875
B 283 Central Processor and Console (tape and disc file capabilities are included)	1,785
Card Reader: 475 cards/min.	320
Card Punch: 100 cards/min.	450
Line Printer: 475 lines/min.	810
Magnetic Tape Units (6): 18,000 or 50,000 char/sec.	4,200
Supervisory Printer	400
TOTAL RENTAL:	$8,840

Note: A similar configuration connected to the B 300 Series Central Processor and using high-speed peripheral devices rents for $10,070 per month. This price includes a 1400-cpm card reader, 300-cpm card punch, 1040-lpm line printer, and six 72 KC magnetic tape units with a recording density of 800 bpi.

.4 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V

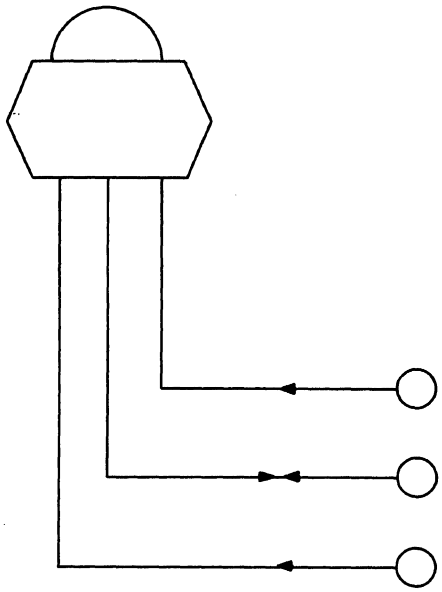
Deviations from Standard Configuration: . . . . magnetic tape is up to 67% faster.
no index registers.
console typewriter input is included.



Equipment	Rental
Disk File Storage Unit: 9,600,000 char.	$1,700
Disk File Storage Module: 9,600,000 char.	990
Disk File Control Unit and Adapter	730
Core Storage: 19,200 char.	875
B 283 Central Processor and Console (tape and disc file capabilities are included)	1,785
Card Reader: 475 cards/min.	320
Card Punch: 100 cards/min.	450
Line Printer: 475 lines/min.	810
Magnetic Tape Units (6): 18,000 or 50,000 char/sec.	4,200
Supervisory Printer	400
TOTAL RENTAL:	$12,260

(Contd.)

.5 SPECIAL CONFIGURATION FOR UNIT RECORD HANDLING



Core Storage: 4,800 char.

VRC Central Processor and Console

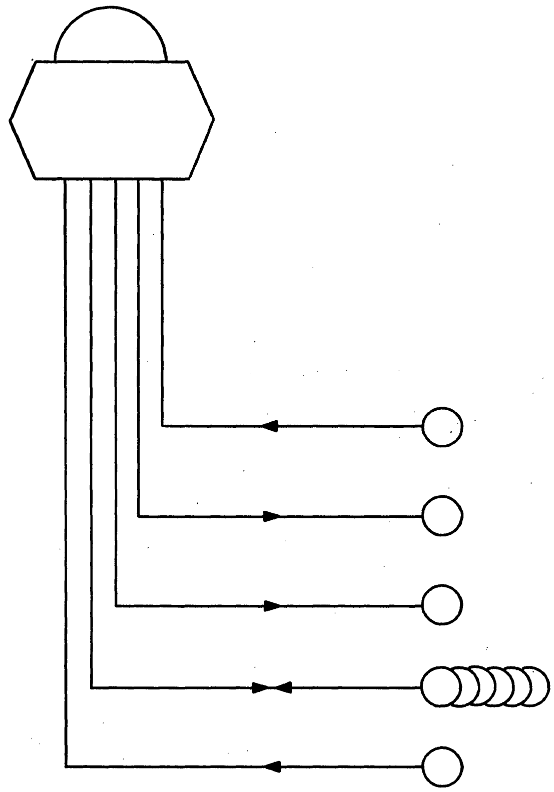
Card Reader: 200 cards/min.

Record Processor

B 102 MICR Sorter-Reader:
1,565 items/min.

TOTAL RENTAL: $4,400 per month (special VRC System package).

.6 SPECIAL CONFIGURATION FOR PROOF-TRANSIT OPERATIONS



Equipment	Rental
Core Storage: 4,800 char. (included in price of Processor)	
B 270 10-microsecond Central Processor and Console (tape and MICR capabilities included).	$ 1,650
Card Reader: 200 cards/min.	220
Card Punch: 100 cards/min.	450
Multiple Tape Lister: 1,565 lines/min.	1,600
Magnetic Tape Units (6): 18,000 or 50,000 char/sec.	4,200
B 103 MICR Sorter-Reader without endorser: 1,565 items/min.	2,000
TOTAL RENTAL:	$10,120

INTERNAL STORAGE: CORE STORAGE

.1 GENERAL

.11 Identity: . . . . Magnetic Core Storage. Part of B 100/200/300 Series Central Processors.

.12 Basic Use: . . . . working storage.

.13 Description

Magnetic core storage for the B 100/200/300 Series is available in storage capacities of 4,800, 9,600, and 19,200 alphameric characters. Each character position is individually addressable and consists of seven bits, six for data and one for odd parity. Every system in the series can function with the basic 4,800 positions of core storage, but the addition of successive modules of 4,800 and 9,600 characters is possible only in the B 263, B 273, B 283, and B 300 Systems. Memory cycle time is either ten microseconds (B 100, VRC, B 260, B 270, B 280) or six microseconds (B 263, B 273, B 283, B 300), providing potential transfer rates of 100,000 or 166,000 characters per second, respectively.

Storage positions are referenced by three-character addresses. The most significant character designates one of 40 sections within a 4,800-character block of storage, the mid-order character of the address specifies one of ten fields within the section, and the least significant character indicates the character position (1-12) within the data field. Zone bits over the ten's position of the address reference one of the four possible 4,800-character logical blocks.

.14 Availability: . . . . . . immediate for B 100, VRC, 260, 270, 280.
6 months for B 263, 273, 283.
6 to 8 months for B 300.

.15 First Delivery: . . . . September 1961 for B 200 Series.
January 1963 for 9,600 characters of storage.
April 1964 for B 100 Series.
May 1965 for B 300 and 19,200 characters of storage.

.16 Reserved Storage: . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . magnetic core.

.23 Storage Phenomenon: direction of magnetization.

.24 Recording Permanence

.241 Data erasable by program: . . . . yes.
.242 Data regenerated constantly: . . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . no.
.245 Storage changeable: . . no.

.28 Access Technique: . . coincident current.

.29 Potential Transfer Rates

.292 Peak Data Rates —
Unit of data: . . . . . character.
Cycle rate: . . . . . see Table I.
Conversion factor: . 7 bits per character.
Data rate: . . . . see Table I.

TABLE I: B 100/200/300 SERIES CORE STORAGE CHARACTERISTICS

Processor Model	B 100, VRC, B 260, B 270, B 280	B 263, B 273, B 283, B 300
Potential cycle and data rate, char/sec	100,000	166,000
Available capacities, characters	4,800	4,800, 9,600 19,200
Uniform access and cycle time, microseconds	10	6
Effective transfer rate, char/sec	48,000	80,000

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum Storage
Characters:	4,800	19,200
Instructions:	400	1,600
Modules:	1	3

.32 Rules for Combining Modules: . . . . . . see Table I for available capacities.

.4 CONTROLLER: . . . no separate controller.

.5 ACCESS TIMING

.53 Access Time Parameters and Variations

.531 For data unit of 1 character: . . . . . . see Table I.

.6 CHANGEABLE STORAGE: . . . . . . none.

.7 STORAGE PERFORMANCE

.72 Transfer Load Size: . 1 to 132 characters.

.73 Effective Transfer Rate: . . . . see Table I.

.8 ERROR, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	none.	
Receipt of data:	none.	
Dispatch of data:	send parity bit.	
Invalid character:	all valid.	
Recovery of data:	parity check	stop computer; alarm.
Recording of data:	record parity bit.	

INTERNAL STORAGE: DISK FILE SYSTEM

.1 GENERAL

.11 Identity: . . . . B 450 Disk File and Data Communication Basic Control.
B 247 Disk File Control Unit.
B 451 Disk File Expanded Control Unit.
B 471 Disk File Electronics Unit.
B 475 Disk File Storage Module.

.12 Basic Use: . . . . auxiliary storage.

.13 Description

The Burroughs Disk File System is a large-capacity random access storage facility available for use with the B 263, B 273, B 283, and B 300 systems. The Disk File features a fast average access time of 20 milliseconds, high-density recording, high reliability through elimination of movable access arms, and capabilities for shared usage by multiple processors.

The B 450 Disk File and Data Communications Basic Control serves as an interface between up to two processors and the Disk File System (a maximum of four processors can access the same mass storage). Each B 471 Disk File Electronics Unit can have 1 to 5 four-disk modules, each containing 9.6 million* character locations. From 1 to 10 Electronics Units can be connected to the B 247 Disk File Control Unit. The maximum storage capacity per system, therefore, is 480 million alphameric characters. Multiple processors and/or more than five B 475 storage modules are controlled by the B 451 Disk File Expanded Control Unit. Table I shows the potential Disk File System sizes with the corresponding configuration demands.

The following is a breakdown of the storage capacities of the Disk System components:

- Segment - can be 96, 240, or 480 characters in size, as specified during manufacture.
- Data track - can store 24,000 alphameric characters (250, 100, or 50 segments, depending on segment size).
- Disc face - has 50 data tracks (2 faces per disc).
- Module - has 4 vertically-mounted discs, on one horizontal shaft.
- Electronics Unit - can contain 1 to 5 modules.
- Control Unit - can control 1 to 10 Electronics Units.
- Disc System - can have one control unit per processor.

Each physical track has a fixed read-write head. Since positioning time is eliminated, access time is a function of the rotation time. The time for the rotation of a disc record is 40 milliseconds, so access to each record will take from 0 to 40 milliseconds, or an average of 20 milliseconds. One case where the average access time is greater than 20 milliseconds is updating a record. This takes two references (to read the original record and then rewrite the updated version), but the

*Module capacity can be increased to 14.4 million packed decimal digits through use of the B 300 optional Data Compress instruction (see Instruction List, Section 201:121).

TABLE I: CONFIGURATION REQUIREMENTS FOR DISK FILE SYSTEMS

B 475 Disk File Storage Modules (9.6 million char/module)	Number of Processors			
	1 Processor	2 Processors	3 Processors	4 Processors
1 to 5 Modules	1A, 1B, 1D	1A, 2B, 1C, 1D	2A, 3B, 1C, 1D	2A, 4B, 1C, 1D
6 to 25 Modules	1A, 1B, 1C, 2-5D	1A, 2B, 1C, 2-5D	2A, 3B, 1C, 2-5D	2A, 4B, 1C, 2-5D
26 to 50 Modules	1A, 1B, 2C, 6-10D	1A, 2B, 2C, 6-10D	2A, 3B, 2C, 6-10D	2A, 4B, 2C, 6-10D

Key to TABLE I:

A - B 450 Disk File and Data Communications Basic Control.
B - B 247 Disk File Control Unit.
C - B 451 Disk File Expanded Control Unit.
D - B 471 Disk File Electronics Unit.

.13 Description (Contd.)

second reference is not a random reference and will often cost almost a full revolution (40 milliseconds). Thus, the average reference time for file maintenance applications will be about 30 milliseconds.

Average data transfer rate is 100,000 characters per second. Data transfers are executed as eight-character words which are assembled in the controller. Up to 10 segments can be transferred by one instruction (a maximum of 4,800 characters).

The method of addressing the Disk File Control Unit is by a 7-character address. One character designates the storage unit and six characters designate the segment address. Segment addresses are assigned starting at some point on the initial disc surface of the first module and continuing in direct sequential order. There is a positive check on the address itself. No timing synchronization between different modules is possible; this prevents attempts to optimize programming by minimizing disc latency.

A "multiple character check" is produced in the control circuitry and recorded with each 48-bit data word. These codes are always checked automatically upon reading data from the disc; they can also be examined by a programmed read-back operation after recording. The checking procedure does not compare the original data with the recorded data but merely regenerates and examines the check code associated with the recorded data.

Burroughs Corporation does not appear to rely heavily on this programmed read-after-write check, pointing out the reliability of head-per-track switching. They also point out the cost in time of such checking (it can reduce effective speeds by two-thirds), and instead recommend a simultaneous tape write-out of the data.

Disk File programming is facilitated by a compact and comprehensive set of three basic instructions: Read, Record, and Interrogate. The Interrogate instruction checks the conditions of controller readiness, data transfer error, and Disk File address validity.

When multiple processors access the same Electronics Unit, one processor is serviced while the others wait. Consecutive references to the same record are possible and must be regulated according to individual installation requirements.

A number of physical precautions are taken to safeguard the information on the discs.

- The head design is such that if the heads approach the disc too closely, a fail-safe technique moves the heads away and switches the unit off.
- Each individual disc has its own manual lockout circuits which can prevent it from being written upon, while allowing reference to be made to its contents.
- The heads are embedded in a soft material so that the disc will not be damaged if contact is made with the disc.

.15 First Delivery: . . . . third quarter of 1964.

.16 Reserved Storage: . . none (but write lockout) switches are provided for each individual disc).

.2 PHYSICAL FORM

.21 Storage Medium: . . . multiple magnetic discs.

.22 Physical Dimensions

.222 Disc
Diameter: . . . . . . 26.5 inches.
Thickness or length: 0.125 inch.
Number on shaft: . . 4 (shaft is horizontal).

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . no.
.245 Storage changeable: . no.

.25 Data Volume per Band of 1 Track

Words: . . . . variable.
Characters: . . . . 24,000.
Digits: . . . . 24,000.
Instructions: . . . . 2,000.
Segments: . . . . . . 50, 100, or 250.

.26 Bands per Physical Unit: . . . . 50 per disc surface.

.27 Interleaving Levels: . 1.

.28 Access Techniques

.281 Recording method: . . every track on each disc surface has an individual fixed head.
.283 Type of access—
Description of stage: wait for selected segment for reading or recording.
Possible starting stage: . . . . uniform.

.29 Potential Transfer Rates

.291 Peak bit rates—
Cycling rates: . . . 1,500 rpm.
Bit rate per track: . 700,000 bits/sec/track.
.292 Peak data rates—
Unit of data: . . . . character.
Conversion factor: . 7 bits per character.
Gain factor: . . . . . 1 track/band.
Data rate: . . . . . . 100,000 char/sec.

(Contd.)

.3 DATA CAPACITY

.31 Module and System Sizes

(See Table Below.)

.32 Rules for Combining Modules: . . . . . . 1 to 10 Disk File Electronics Units may be connected to the control unit; one 4-disc module is included in each Electron ics Unit; up to 4 additional modules can be connected to an Electronics Unit.

.4 CONTROLLER

.41 Identity: . . . . B 247 Disk File Control Unit.

.42 Connection to System

.421 On-line: . . . . 4, one per processor.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . . 1 to 10 Electronics Units.
.432 Restrictions: . . . . . refer to Table I.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 10 segments (each can be 96, 240, or 480 characters in size).
.442 Input-output area: . . core storage.
.443 Input-output area access: . . . . . . each character.
.444 Input-output area lockout: . . . . . . none.
.445 Synchronization: . . . programmed.
.446 Synchronizing aids: . test busy; branch on not ready.
.447 Table control: . . . . none.
.448 Testable conditions: . Busy Controller, Recording Lock, Recovery Error, Transfer Error.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks: . . one read-write head per track.
.512 Stack Movement: . . . none.
.513 Stacks that can access any particular location: . . . 1.
.514 Accessible locations:
By single stack: . . 24,000 chars. (50, 100, or 250 segments).
By all stacks: . . . 9,600,000 per module.

.52 Simultaneous Operations: . . . . only one disc file operation at a time is permitted.

.53 Access Time Parameters and Variations

.532 Variation in access time —

Stage	Variation	Average
Positioning:	0	0.
Latency (rotational delay):	0 to 40 msec.	20 msec.
Total:	0 to 40 msec.	20 msec.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 AUXILIARY STORAGE PERFORMANCE

.72 Transfer Load Size

With core storage: 1 to 10 segments; number of segments is selected by program.

.73 Effective Transfer Rate

With core storage: 62,000 char/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	error indicator set, operation terminated
Receipt of data:	parity check on addresses	indicator set, operation terminated, no data transferred.
Recording of data:	optional programmed readback	set indicator.
Recovery of data:	error check code	set indicator.
Dispatch of data:	parity bit included. Not ready check	branch.
Timing conflicts:	interrogate command	branch on busy, error, or write interlock.
Reference to locked area:	check	indicator set, operation terminated.

.31 Module and System Sizes

	Minimum Storage			Maximum Storage
Identity:		B 475 Disk File Storage Module	B 471 Disk File Electronics Unit	B 450 Disk File Sub-System.
Disks:	0	4	20	200
Characters:	0	9,600,000	48,000,000	480,000,000.
Instructions:	0	800,000	4,000,000	40,000,000.
Modules:	0	1	5 (max.)	50 (max.)

CENTRAL PROCESSOR: B 100/200 (10-MICROSECOND CYCLE TIME)

.1 GENERAL

.11 Identity: . . . . Central Processor (identified by system): B 260, B 270, B 280, VRC, B 160, B 170, and B 180.

.12 Description

The B 200 Series Central Processor, first produced by Burroughs in 1961, still forms the basis of the entire B 100/200/300 Series of computer systems. It functions in its original form in the VRC, the entire B 100 Series, and the B 260, B 270, and B 280 systems. The improved and enlarged version, currently available in the B 263, B 273, B 283, and B 300 systems, is treated on page 201:052.100.

The Basic B 200 Series Processor is a three-address, character-oriented processor containing core storage facilities, an arithmetic and control unit, input-output buffer areas, and an integrated console. The arithmetic and logical capabilities of the various B 200 Series Processors are essentially the same; they differ, however, in the configurations of peripheral equipment and optional features that can be attached, as shown in the System Configuration chart (page 201:031.001). The B 100 Processor is offered with somewhat less peripheral flexibility than the B 200, but at a substantially reduced price (see the Price Data section, page 201:221.101).

Core storage capacity in the original line of B 200 Processors is fixed at 4,800 alphameric characters. Each character position is individually addressable. The core storage cycle time is 10 microseconds both for instructions and data. Instructions have a fixed length of 12 characters each, whereas data fields can be of variable length.

Due largely to the three-address command structure, the instruction repertoire contains good decimal arithmetic, comparison, and editing capabilities. The lengths of the operands can vary from 1 to 12 characters and are specified in the instructions themselves. An address modification instruction, available in all systems except the B 100 Series and the VRC, can increment one 3-character address. Index registers and indirect addressing, however, are not provided in any of the B 100/200/300 Series processors. Another shortcoming, with regard to real-time operations, is the lack of automatic interrupt facilities. However, the capability to test all peripherals for busy status is optional with the B 300 Processor; see Paragraph 201:052.12.

The B 100 Series Processor, economy version of the original B 200 Line, restricts the control of input-output devices to one card reader (minus a busy-test option), one printer (700 lines per minute maximum), and six B 423 Magnetic Tape Units (24,000 characters per second data transfer rate). Standard card punches and MICR sorter-readers can also be connected according to the configuration rules on page 201:031.001.

.13 Availability: . . . . immediate.

.14 First Delivery: . . . . . July, 1962.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point — Add-subtract:	automatic	decimal	1 to 12 digits.
	Multiply — Short:	none.		
	Long:	automatic	decimal	1 to 12 digits.
	Divide — No remainder:	none.		
	Remainder:	automatic	decimal	1 to 12 digits.

.212 Floating point: . . . . . none.
.213 Boolean:. . . . . none.
.214 Comparison —

	Provision	Size
Numbers:	automatic (sign ignored)	1 to 12 digits.
Absolute:	automatic	1 to 12 digits.
Letters:	automatic	1 to 12 char.
Mixed:	automatic	1 to 12 char.
Zone:	automatic	1 to 12 char.
Collating sequence:	specials, A to I, specials, J to R, specials, S to Z, 0 to 9.	

.215 Code translation: . . . . none.
.216 Radix conversion: . . . none.

.217 Edit format

	Provision	Comment	Size
Alter size:	none.		
Suppress zero:	automatic	use b char	
Round off:	none.		
Insert point:	automatic.		
Insert commas:	automatic.		
Insert dollar:	automatic.		
Insert spaces:	none	only replace leading zeros	
Insert special char:	automatic	1 char in LSD of mask inserted if sign of field is negative	12 char field max. 24 char mask max.
Replace by special char:	automatic	leading zeros replaced by any desired char placed in mask (except $..)	
Float dollar:	none.		
Protection:	automatic	1 of the replacement possibilities.	

Notes: 1. Special character insertion ends at decimal point.
2. Character in mask between point and LSD may be used for addressable storage.

.218 Table lookup: . . . . . . none.

.22 Special Cases of Operands

.221 Negative numbers: . . . absolute value with sign in zone bits.
.222 Zero: . . . . positive except in some multiply or divide results; treated as equal in branch tests.
.223 Operand size determination: . . . . . counter, set by instructions.

.23 Instruction Formats

.231 Instruction structure: . 12 characters.
.232 Instruction layout:

Part:	O	M	N	AAA	BBB	CCC
Size (char):	1	1	1	3	3	3

.233 Instruction parts —

Name	Purpose
O:	operation code.
M, N:	field length, variations, or device control.
AAA, BBB, CCC: .	operand address or jump location.

.234 Basic address structure: . . . . 3 + 0.
.235 Literals: . . . . none.
.236 Directly addressed operands: . . . . 1 to 12 characters; from anywhere in core storage.
.237 Address indexing: . . . none.
.238 Indirect addressing: . . none.
.239 Stepping: . . . . none.

.24 Special Processor Storage: . . . . 2 80-character input buffer areas.
1 80-character output buffer area.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: sequential.

.32 Look-Ahead: . . . . none.

.33 Interruption: . . . . none.

.34 Multiprogramming: . . none.

.35 Multi-sequencing: . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
Add-subtract: . . . . . 40 + 130 D, where D is operand length in digits.
Multiply: . . . . $30 + 60D + 210D^2$.
Divide: . . . . $600D^2 - 110D - 470$.
.413 Additional allowance for re-complementing: 10D
.414 Control —
Compare: . . . . 40 + 100C, where C is operand length in characters.
Branch (on sign): . . . 70.
.416 Edit: . . . . 120 + 120M + 80N; where M = operand length and N = number of inserts ($), (.), (,).
.417 Convert: . . . . none.

.418 Shift: . . . . none.

.42 Processor Performance in Microseconds

.421 For random addresses —
c = a + b: . . . . 40 + 130D.
b = a + b: . . . . 40 + 130D.
Sum N items: . . . . . (40 + 130D) N.
c = ab: . . . . $70 + 190D + 210D^2$.
c = a/b: . . . . $600D^2 + 20D - 470$.
.422 For arrays of data —
$c_i = a_i + b_j$: . . . . 750 + 260D.
$b_j = a_i + b_j$: . . . . 620 + 260D.
Sum N items: . . . . . . (490 + 260D)N.
$c = c + a_ib_j$: . . . . $650 + 320D + 210D^2$.
.423 Branch based on comparison —
Numeric data: . . . . 720 + 200C.
Alphabetic data: . . . 720 + 200C.

(Contd.)

.424 Switching —
Unchecked: . . . . 410.
Checked: . . . . 760.
List search: . . . . . . 450 + 100N.

.425 Format control, per character —
Unpack: . . . . 31.
Compose: . . . . 65.

.426 Table look-up, per comparison —
For a match: . . . . . 240 + 100C.
For least or greatest: . . . . . . 520 + 100C.
For interpolation point: . . . . 240 + 100C.

.427 Bit indicators —
Set bit in separate location: . . . . 120.
Test bit in separate location: . . . . 140.
Test AND for B bits: 170B.
Test OR for B bits: . 30 + 134B.

.428 Moving: . . . . 40 + 80C for VRC system.
100 + 20C for B 260, B 270, and B 280 systems.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	none.	
Zero divisor:	check	quotient set to zero.
Invalid data:	check	halt, alarm.
Invalid operation:	none.	
Arithmetic error:	none.	
Invalid address:	none.	
Receipt of data:	parity check	halt, alarm.
Dispatch of data:	none.	
Divisor and dividend same length:	check	halt, alarm
Improper significant digits in dividing:	check	quotient set to zero.
Processing of data:	parity check	halt, alarm.

CENTRAL PROCESSOR: B 200/300 (6-MICROSECOND CYCLE TIME)

.1 GENERAL

.11 Identity: . . . . Central Processor (identified by system): B 263, B 273, B 283, and B 300.

.12 Description

The B 200/300 Central Processor offers higher internal speed and more core storage than the original B 200 Processor described on page 201:051.100. The upgraded model, featuring a core storage cycle time of six microseconds, is used in the B 263, B 273, B 283, and B 300 Series systems. Core storage capacity can be increased from the series base of 4,800 alphameric characters to either 9,600 or 19,200 characters.

The internal design and functional capabilities of the B 100/200 Central Processor are repeated in the more comprehensive B 200/300 Series Processor. Provisions have been added to control a random access Disk File System, data communications network paper tape reader and punch, supervisory printer, high-speed card reader (1,400 cpm), and high-speed magnetic tape units (66 KC). Features optionally available for this line of processors include a combination Transfer and Branch instruction, selective stacking with the B 304 Card Punch, 132-print-position control with the B 325 and B 329 Line Printers, and a Card Reader Early Release device. The latter option frees the Processor immediately after the 80th card column is read into the buffer area.

Increasing the level of B 200 Central Processor design one step further, Burroughs has developed the B 300 Processor. This is a single processor model designed to serve the entire B 300 Series. The unique concept introduced in the B 300 Processor is the use of optional Input-Output Control Modules for each peripheral unit connected (card reader, punch, and line printer are the only exceptions). In effect, every B 300 Central Processor will be custom-designed according to individual installation requirements.

Similarly, optional Processor Command Modules can be added whenever certain instructions are desired. The Command Modules, available for the B 300 Processor exclusively, can control the following instructions:

- Transfer and Translate: Permits translation of any 6-bit code to any other code of up to 12 bits. This is accomplished through the use of translation tables, which utilize from 92 to 184 characters of core storage.
- Unit Interrogate: Tests the status of all peripheral devices and initiates further program control upon detection of not-readiness, busy status, or error condition. The line printers are regarded as not busy when spacing or skipping; hence, the processor must wait for paper motion to cease.
- Data Compress: Packs three numeric digits into the space normally occupied by two alphameric characters. The Data Expand instruction (included in this Command Module) performs the converse function. Through the use of the Data Compress command, the storage capacity of both magnetic tape reels and Disk Files can be increased by up to 50%, assuming all-numeric data.
- Binary Card Read: Reads the contents of a punched card and stores in memory the 160-character binary card image. This instruction permits reading any card code (including pure column binary), with the necessary translation being performed by the stored program.
- Binary Card Punch: Punches binary card images from core storage. (Neither Binary Read nor Binary Punch are buffered operations.)
- B 300 Lister Command: Controls the B 322 and B 333 Multiple Tape Listers; provides the ability to select up to 18 listing tapes and to print simultaneously on any 3 selected tapes. Page 201:082.100 describes the operation of the various Burroughs Multiple Tape Listers.
- Six externally-controlled Sense Switches are also available with the B 300 Central Processor. The Sense Switches can be tested by means of the Unit Interrogate Command.

Two improved peripheral devices can operate only with the B 300 Central Processor: the B 332/333 Multiple Tape Lister (1,565 lines per minute), and the B 425 Magnetic Tape Unit. The B 425 provides data transfer rates of 18,000, 50,000 or 72,000 characters per second.

All B 300 optional features, including memory modules, Input-Output Control Modules, and Processor Command Modules, can be installed in the field. As a result, the expansion of B 300 Series systems can be accomplished easily as installation demands increase.

.14 First Delivery: . . . . . January 1964 for B 263, 273, 283.
May 1965 for B 300.

.13 Availability: . . . . 6 to 8 months for B 300.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add-subtract:	automatic	decimal	1 to 12 digits.
	Multiply —			
	Short:	none.		
	Long:	automatic	decimal	1 to 12 digits.
	Divide —			
	No remainder:	none.		
	Remainder:	automatic	decimal	1 to 12 digits.

(Contd.)

.212 Floating point: . . . . none.
.213 Boolean: . . . . none.
.214 Comparison —

	Provision	Size
Numbers:	automatic (sign ignored).	1 to 12 digits.
Absolute:	automatic	1 to 12 digits.
Letters:	automatic	1 to 12 char.
Mixed:	automatic	1 to 12 char.
Zone:	automatic	1 to 12 char.
Bit:	automatic	1 bit.
Collating sequence:	specials, A to I, specials, J to R, specials, S to Z. 0 to 9.	

.215 Code translation (B 300 only) —
Provision: . . . . automatic (using optional command and code table constructed by programmer).
From: . . . . any 6-bit code.
To: . . . . any code from 6 to 12 bits.
Size: . . . . 1 to 120 characters.
.216 Radix conversion: . . . none.
.217 Edit format —

	Provision	Comment	Size
Alter size:	none.		12 char field max. (Alter size through Insert spaces)
Suppress zero:	automatic	use b char	
Round off:	none.		
Insert point:	automatic.		
Insert commas:	automatic.		
Insert dollar:	automatic.		
Insert spaces:	automatic	use alphameric mask.	
Insert special char:	automatic	1 char in LSD of mask inserted if sign of field is negative; also any char. inserted with alphameric mask.	24 char mask max. (Insert special char through Protection)
Replaced by special char.	automatic	leading zeros replaced by any desired char placed in mask (except $..)	
Float dollar:	none.		
Protection:	automatic	1 of the replacement possibilities.	

Note: 1. Special character insertion ends at decimal point.
2. Character is mask between point and LSD may be used for addressable storage.

.218 Table lookup: . . . . . . none.

.22 Special Cases of Operands

.221 Negative numbers: . . . absolute value with sign in zone bits.
.222 Zero: . . . . positive except in some multiply or divide results; treated as equal in branch tests.
.223 Operand size determination: . . . . . counter, set by instructions.

.23 Instruction Formats

.231 Instruction structure: . 12 characters.
.232 Instruction layout:

Part:	O	M	N	AAA	BBB	CCC
Size (char):	1	1	1	3	3	3

.233 Instruction parts —

Name	Purpose
O:	operation code.
M, N:	field length, variations, or device control.
AAA, BBB, CCC: .	operand address or jump location.

.234 Basic address structure: . . . . 3 + 0.
.235 Literals: . . . . none.
.236 Directly addressed operands: . . . . 1 to 12 characters; from anywhere in core storage.
.237 Address indexing: . . . none.
.238 Indirect addressing: . . none.
.239 Stepping: . . . . none.

.24 Special Processor Storage: . . . . 2 80-character input buffer areas.
1 80-character output buffer area.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: sequential.

.32 Look-Ahead: . . . . none.

.33 Interruption: . . . . none.

.34 Multiprogramming: . . none.

.35 Multi-sequencing: . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
Add-subtract: . . . . . $24 + 78D$.
Multiply: . . . . $18 + 36D + 126D^2$.
Divide: . . . . $360D^2-66D-262$.

.413 Additional allowance for re-complementing: . . . . 6D.

.414 Control
- Compare: . . . . 24 + 60C.
- Branch (on sign): . . . 42.

.416 Edit: . . . . 72 + 72M + 48N; M = operand length and N = number of inserts ($), (.), (,).

.417 Convert: . . . . none.

.418 Shift: . . . . none.

.42 Processor Performance in Microseconds

.421 For random addresses —
- c = a + b: . . . . 24 + 78D.
- b = a + b: . . . . 24 + 78D.
- Sum N items: . . . . . (24 + 78D)N.
- c = ab: . . . . $42 + 114D + 126D^2$.
- c = a/b: . . . . $360D^2 + 12D - 258$.

.422 For arrays of data —
- $c_i = a_i + b_j$: . . . . . . 450 + 156D.
- $b_j = a_i + b_j$: . . . . . . 372 + 156D.
- Sum N items: . . . . . 372 + 156D.
- $c = c + a_i b_j$: . . . . . . $390 + 192D + 126D^2$.

.423 Branch based on comparison —
- Numeric data: . . . . 432 + 120C.
- Alphabetic data: . . . 432 + 120C.

.424 Switching —
- Unchecked: . . . . 246.
- Checked: . . . . 456.
- List search: . . . . . . 270 + 60N.

.425 Format control, per character —
- Unpack: . . . . 19.
- Compose: . . . . 39.

.426 Table look-up, per comparison —
- For a match: . . . . . 144 + 60C.
- For least or greatest: . . . . . . 312 + 60C.
- For interpolation point: . . . . 144 + 60C.

.427 Bit indicators —
- Set bit in separate location: . . . . 72.
- Test bit in separate location: . . . . 84.
- Test AND for B bits: . . . . 102B.
- Test OR for B bits: . 18 + 84B.

.428 Moving: . . . . 60 + 12C.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	none.	
Zero divisor:	check	quotient set to zero.
Invalid data:	check	halt, alarm.
Invalid operation:	none.	
Arithmetic error:	none.	
Invalid address:	none.	
Receipt of data:	parity check	halt, alarm.
Dispatch of data:	none.	
Divisor and dividend same length:	check	halt, alarm.
Inproper significant digits in dividing:	check	quotient set to zero.
Processing of data:	parity check	halt, alarm.

CONSOLE

.1 GENERAL

.11 Identity: . . . . Console Panel: a sub-unit of Processor.
Processor Console is built into end of Central Processor cabinet and consists of sloping panel and horizontal work space.

.12 Associated Units: . . . B 495 Supervisory Printer (described below).

.13 Description

The Console contains the control and visible indicators used in the operation and maintenance of the computer. It includes facilities for display of device operation, display and manual entry of binary-coded data, and single-instruction operation.

The B 495 Supervisory Printer, with an output rate of 10 characters per second, can be used with the B 200/300 6-microsecond Central Processors only. It is unbuffered and uses the Burroughs Common Language (BCL) character set. Appropriate commands have been added for programmed control of the Supervisory Printer, which uses a modified electric typewriter as an input-output device. Print format is 10 characters per inch horizontally, and six lines per inch vertically.

The Printer accepts continuous fanfold paper 8.5 inches in width (9.875 inches including sprocket hole tracks). No provision is made for automatic indexing to a specific location on a pre-printed form. Two carbons can be printed. Left and right hand margins cannot be pre-set by the operator. The left hand margin is set at one inch. Maximum length for a printed line is 72 characters. Carriage return is caused by:

- pressing carriage return key,
- printing of the 72nd character,
- a left pointing arrow (←) in the output data (in memory as 01 1111), or
- pressing the end-of-input key during input.

.2 CONTROLS

.21 Power

Name	Form	Comment
Power on:	indicating switch	controls power to Processor and all system components.
Power off:	switch	
Emergency off:	pull switch.	

.22 Connections: . . . . none.

.23 Stops and Restarts

Name	Form	Comment
Halt:	indicating switch	system halts after all operations in progress have been completed.
Continue:	indicating switch	starts system after halt, or stop with error conditions removed.

.24 Stepping

Name	Form	Comment
Single Instruction:	switch	instruction stored at displayed address is executed.

.25 Resets

Name	Form	Comment
Clear:	switch	clears all indicators and registers.
Bit Reset:	switch	allows clearing of any selected bits which are displayed.

.26 Loading

Name	Form	Comment
Load:	switch	causes reading and sequential storage of deck of cards (may be used with paper tape in B 200/300 Series 6-microsecond central processors).

.27 Program Branching

Name	Form	Comment
Sense Switches	toggle switches (6)	Testable by program to control branching (optional with B 300 Series).

.3 DISPLAY

.31 Alarms

Name	Form	Comment
Disk File/Data Communications:	static lamp	error, or Disk File control busy or not ready. System halts.
Tape:	static lamp	error or not ready in magnetic tape. System halts.
Printer:	static lamp	error or not ready in printer. System halts.
Punch:	static lamp	error or not ready in punch. System halts.
Reader 1:*	static lamp	error or not ready in reader. System halts.
Reader 2/ Sorter:*	static lamp	error or not ready in reader/ sorter. System halts.
Central Processor:	static lamp	parity error in Central Processor. System halts.

* These alarms are labeled Card 1 and 2 on VRC Console.

.32 Conditions: . . . . none.

.33 Control Registers

Name	Form	Comment
Instruction:	binary coded indicating push-buttons	display of instruction to be executed.
Instruction address:	binary coded indicating push-buttons	display starting location of instruction to be executed.

.34 Storage

Name	Form	Comment
Memory Display:	binary coded indicating push-buttons	display 1 character.
Memory Address:	binary coded indicating push-buttons	display address of displayed character.
Read Memory:	switch	char in Memory Address location displayed in Memory Display.
Increase Address and Read Memory:	switch	Memory Address increased by one and char at that location displayed in Memory Display.

.4 ENTRY OF DATA

.41 Into Control Registers

Name	Form	Comment
Instruction address:	binary coded indicating push-buttons	depress display buttons to set up address.

.42 Into Storage

Name	Form	Comment
Memory Display:	binary coded indicating push-buttons	depress display push-buttons to set up character.
Write Memory:	switch	Memory Display char stored in Memory Address location.

.5 CONVENIENCES

.51 Communication:. . . . . no facilities.

.52 Clock: . . . . optional.

.53 Desk Space: . . . . approximately 10 by 28 inches, situated below console panel, at a height of approximately 40 inches from floor.

.54 View: . . . . standing; height of Central Processor is 55 inches.

INPUT-OUTPUT: B 122 CARD READER

.1 GENERAL

.11 Identity: . . . . B 122 Card Reader.

.12 Description

The B 122 Card Reader reads 80-column punched cards of standard or post-card thickness at a maximum rate of 200 cards per minute. Reading is performed by 13 photoelectric cells (one for timing), serially by column and parallel by bit. The time required to read each card, normally 300 milliseconds, is increased by 15 milliseconds when the reader is used intermittently rather than at its peak rate. The B 122 Card Reader automatically translates Hollerith code into Burroughs Common Language (BCL) code before transferring the information to the buffer area of the central processor.

The B 100/200/300 Series Central Processor contains two 80-character input buffers which can accommodate one or two B 122 Card Readers per system. A Read instruction transfers the contents of the buffer, containing the data read from the previous card, to core storage within 3.2 milliseconds; then the next card is read, refilling the buffer. The buffer-refilling operation proceeds independently of the central processor. Buffered card reading permits the peak speed of 200 cards per minute to be maintained if processing time per card does not exceed 296.8 milliseconds.

Cards are fed by a pinch roller device on demand from the central processor. The input hopper has a capacity of 500 cards and can be refilled while cards are being read. The single stacker provided also holds 500 cards, but it cannot be emptied while the unit is in operation.

When the B 122 Card Reader is connected to a B 200/300 Series Central Processor, its status can be tested by the Read instruction. If the reader is not available, program control is transferred, enabling the processor to perform alternative functions before attempting another Read operation.

The validity of each character being read is checked before it is sent to the buffer, provided that the Validity On indicator-switch is set. Reader operational failure causes a system interlock and displays a Read Check indicator. Failure to feed a card or a feeder jam (maximum of two cards involved) also causes an interlock and illuminates a Feed Check indicator. After all cards in the hopper have been read, the central processor will halt on the next Card Read instruction. If the operator then depresses the End of File button on the Reader, a program branch will occur.

Unlike the Burroughs card readers described on page 201:072.100, there are no optional features available for the B 122 Card Reader. First delivery of the B 122 occurred late in 1961. It is currently available immediately.

INPUT-OUTPUT: B 123/124/129 CARD READERS

.1 GENERAL

.11 Identity: . . . . B 123 Card Reader.
B 124 Card Reader.
B 129 Card Reader.

.12 Description

The Burroughs B 123, B 124, and B 129 Card Readers provide punched card reading speeds of 475, 800, and 1400 cards per minute, respectively. Except for this considerable difference in rated speeds, the three readers are essentially the same. The only significant restriction upon connecting any one or two of these readers to any central processor in the B 100/200/300 Series is that the B 129 Card Reader can be used with the B 200/300 six-microsecond Central Processor only. If a Burroughs MICR Sorter-Reader is part of the system, utilizing one of the two input buffers of the central processor, then only one card reader can be connected. The B 122 200-card-per-minute Card Reader described in the preceding report section can be paired with a B 123, B 124, or B 129 model.

The B 123, B 124, and B 129 Card Readers can read standard or post-card thickness punched cards of 51, 60, 66, or 80 columns. The standard types of scored cards are acceptable when the stubs are removed. An immediate-access clutch provides demand feeding of the cards. Photoelectric reading by column initiates the automatic transfer of data from the card to a code translator, en route to the central processor's buffer. (The Binary Card Read option enables cards to be read without any code translation.) A Read instruction transfers the contents of the buffer, containing the data read from the previous card, to core storage within 3.2 milliseconds; then the next card is read, refilling the buffer. During the buffer refilling operation, the processor is free for computation; but without the Early Release optional processor modification described below, the processor must wait for the full card cycle to be completed before performing any magnetic tape, data communication, or Disk File operations. Comparative timings for the B 123, B 124, and B 129 Card Readers are shown in the table below.

Times in Milliseconds	Card Reader Model		
	B 123 475 cpm	B 124 800 cpm	B 129 1400 cpm
Read cycle time, per card:	126	75	42.8
Buffer unloading time:	3.2	3.2	3.2
Processor delay before tape, Disk File, and data communications operations:	122.8	71.8	39.6
Processor delay before above operations using Card Read Early Release option:	55.8	55.8	39.3

Contributing to an increased compatibility with equipment and input media in the field are several optional card reader features. The options listed below are applicable to the B 123, B 124, and B 129 Card Readers only:

- Bull Code Compatibility: A special version of the Card Reader can read and translate 80-column cards punched with a modified Bull T-8 code.
- ICT Code Compatibility: Another specially-manufactured version of the card reader provides for both ICT code and Bull code compatibility, but not during the same run. With a manual switch, the operator can select the mode of operation desired.
- Post Money Order Modification: Allows the reading of 51-column punched cards using round holes that occupy the space of two standard-size rectangular holes.
- Binary Card Read Command: A B 300 Central Processor option that allows the reading of any card code. The 12-bit binary image of each card column code is stored directly in core storage, in two consecutive character positions. Binary card reading is an unbuffered operation.
- Card Read Early Release: Allows the release of the central processor immediately following the reading of the 80th card column. The resultant time savings for magnetic tape, Disk File, and data communication operations are indicated in the table at left.
- Card Read Busy Test: Provides the ability to test the card reader's status. If the reader is busy, program control is transferred to another alternative routine. This feature is not applicable if the card reader is connected to a B 100 Series Central Processor.

Cards are fed by a belt-drive mechanism past the stack of 13 photoelectric read cells (one for timing) and transported to the single stacker. Both the hopper and the stacker have capacities of 2,400 cards and can be filled and emptied while the card reader is in operation. Should a jam occur in the card transport device, the unit will halt with a maximum of two cards jammed.

The validity of each character being read is checked before it is sent to the buffer, provided that the Validity On indicator-switch is set. Card reader operational failure causes a system interlock and displays a Read Check indicator. Failure to feed a card after two attempts (the second try is automatic) will cause a system interlock and illuminate a Feed Check indicator.

The availability of the B 123, B 124, and B 129 Card Readers is from three to four months. First deliveries of the prototype B 124 Card Readers occurred during the last quarter of 1963.

INPUT-OUTPUT: CARD PUNCHES

.1 GENERAL

.11 Identity: . . . . B 303 Card Punch.
B 304 Card Punch.

.12 Description

The B 303 and B 304 Card Punches operate at maximum rates of 100 and 300 cards per minute, respectively; either can function with any central processor in the B 100/200/300 Series. Standard or postcard thickness 80-column cards can be punched (but not both thicknesses during the same run). Pre-scribed and/or pre-punched cards can also be punched if the post-punch checking device is inactivated by the operator. Formatting of the punched card is controlled exclusively by the stored program.

Cards are punched by a single row of 80 punch dies, one row at a time. When a card punch instruction is initiated, data in core storage is loaded into the central processor's 80-character output buffer. A row of information is then transferred to the punch unit's self-contained 80-bit row buffer and punched. During the time required to punch each row, the central processor is free for processing. Throughout the punching cycle the output buffer in the central processor is interlocked against any other potentially destructive accesses.

A checking operation is performed at the punch station to insure that 80 data bits are received for each row and that 12 rows are punched in each card. In addition, a post-punch sensing station compares the card just punched to the image in the buffer to insure accuracy. Detection of a punching error causes a central processor halt when the next punch instruction is initated. Processor halts also occur upon detection of abnormal conditions such as empty hopper, full stacker, card jam, or improper card registration.

Translation from Burrough's internal code to Hollerith punched card code is automatically performed within the punch unit itself. By adding a Bull Code and/or ICT Code compatibility module to a B 200/300 6-microsecond central processor, the standard punch units are rendered capable of punching these special card codes as well as the standard card code.

Another option, available only with the B 300 Series central processor, is the capability to punch cards in the binary mode. A binary card image of the contents of 160 core memory positions is punched, with the contents of single character positions stored in the upper and lower six positions of every card column. Binary card punching is an unbuffered operation.

From hopper to stacker, cards are transported by positive-action pinch rollers. Hopper and stacker capacities of the B 303 Card Punch are 800 cards each. The B 304 Card Punch is equipped with three stackers: primary, auxiliary, and error. The primary stacker can hold 3,000 cards, the same capacity as the unit's hopper. Error cards are segregated in the error stacker, holding 750 cards. The 850-card auxiliary stacker is normally used as an alternative to the primary stacker, controlled by a switch on the control panel, but selective auxiliary stacking under control of the program can be obtained as an option with B 200/300 Central Processors.

Significant timing considerations and a comparison of the B 303 and B 304 Card Punches are provided in Table I.

TABLE I: B303/B304 CARD PUNCH TIMING FACTORS

Model	B 303	B 304
Rated speed	100 cpm	300 cpm
Total card cycle time in synchronous mode, msec	600	200
Overhead in asynchronous mode, msec	50	200
Total buffer load time per card, msec	14.74	14.74
Processing time available to maintain synchronous operation, msec	585.26	185.26
Maximum punching rate if available processing time is exceeded (cards/min.)	92.3	150
Central Processor delay if magnetic tape, Disk file, or data communication operations follow a punch instruction, msec	539.26	154.46

INPUT-OUTPUT: B 141 PAPER TAPE READER

.1 GENERAL

.11 Identity: . . . . B 141 Paper Tape Reader.

.12 Description

This unit reads data from punched paper tape into core storage at a speed of 500 or 1,000 characters per second. Either one or two B 141 Paper Tape Readers can be used with all B 200/300 Series six-microsecond central processors. The unit makes use of the same input buffers as the card readers. The B 141 can accommodate 5, 6, 7, or 8 level tape, as selected by the operator. Standard tape code is the BCL paper tape code (see Data Code Table No. 5).

Two optional features are available: an Input Code Translator and a Reader Selector Switch. The translator allows automatic translation of any code (5, 6, 7, or 8 level) to one of the 64 Burroughs Common Language (BCL) characters used by the central processor. The manual selector switch permits selection of the paper tape reader or card reader.

Reading speed is 500 or 1,000 characters per second. Fanfold tape, whether in strips or in reels, and metalized Mylar tape must be read at 500 characters per second. Other punched tape may be read at either speed. Start and stop times are 5 and 20 milliseconds, respectively. The reader stops on the stop character or between characters at both high and low speeds.

A minimum of four feet of tape leader is required with reels, and at least one foot is needed for strip reading. Tape widths of 0.675, 0.875, or 1 inch can be handled. Reel diameters of either 5.5 or 7 inches can be accommodated. Beginning and end-of-tape indicators are sensed by means of adhesive conductive strips on the tape being read.

The operator can select different paper tape channels by use of a plugboard which is supplied as part of the B 141 Reader. A code punched in all channels (whether 6, 7, or 8 level tape) is considered a delete code and is not transferred to the Processor when operating without a translator.

Reading can be performed in a buffered or unbuffered mode. Maximum use of the buffered mode is realized if the data is arranged in 80-character blocks. Paper Tape Space Forward, Space Backward, and Rewind instructions are provided. Upon detection of an information parity error, the reading is completed and a branch is taken to a subroutine.

The following switches and indicators are provided:

Function	Form	Comment
Local:	switch (and light)	reader not ready for instruction.
Remote:	switch (and light)	reader is ready for instruction.
Stop:	switch	stops reader (Local mode).
Forward:	switch	moves tape forward to next control code or end-of-tape marker (Local mode).
Rewind:	switch	moves tape in reverse until beginning-of-tape marker is reached and then stops (Local plus Reel modes).
Strip-Reel:	switch	selects Reel or Strip input.
Control Code:	3 sets of switches	provides manual selection of three different control codes, any combination of which can be used; each set has OFF (ignore), STORE AND STOP, DELETE AND STOP, and DELETE AND CONTINUE positions.
High-Low:	switch	selects high or low tape speed.
Parity On-Off:	switch	determines whether parity checking will take place.
Teletype On-Off:	switch	provides for the use of teletype tape as input.
Load Reader:	switch	allows loading of tape (Local mode).
Ready:	switch	starts motors, etc. (Local mode).
Backspace:	switch	tape moves in reverse to next control code or beginning-of-tape marker (Local mode).
Unit Selected:	switch (and light)	indicates when the B 141 is selected by operator. Interchanges card reader with B 141.
Parity check:	light	indicates a parity error has occurred.
No Tape:	automatic switch	if in Reel mode and no tape is loaded (or tape breaks), the reel motors are shut off.
Guide Selection:	switch	adjusts tape guiding mechanisms to the width of the tape.

.13 Availability: . . . . 3 to 4 months.

.14 First Delivery: . . . . . September, 1963.

INPUT-OUTPUT: B 341 PAPER TAPE PUNCH

.1 GENERAL

.11 Identity: . . . . B 341 Paper Tape Punch.

.12 Description

The B 341 Paper Tape Punch punches data from core storage onto paper tape at a speed of 100 characters per second. One paper tape punch can be used with all B 200/300 Series six-microsecond central processors. The B 341 is capable of punching 5, 6, 7, or 8 level tape. Standard code is the BCL paper tape code (see Data Code Table No. 5).

Two optional features are available: an Output Code Translator and a Punch Selector Switch. The translator allows translation of Burroughs Common Language (BCL) code to any 5, 6, 7, or 8 level code, for up to 64 different characters. The manual selector switch provides interchangeability between the paper tape punch and the card punch.

The punch is capable of punching paper or plastic tape in widths of 0.675, 0.875, and 1 inch. Maximum reel diameter is eight inches, and it is not necessary to have a take-up reel. An end-of-tape indication is produced whenever 35 feet (or less) of tape is left on the supply reel. The operator can select different paper tape channels by use of a plugboard which is supplied as part of the B 341 Punch.

The following switches and indicators are provided:

Function	Form	Comment
Tape Feed:	switch	tape is fed with all holes punched.
Local:	switch and light	punch is not ready for an instruction.
Remote:	switch and light	punch is ready for an instruction.
Control Code:	4-position switch	determine action by punch when a control code is detected: OFF (ignore), PUNCH AND STOP, DELETE AND STOP, and DELETE AND CONTINUE.
Level Designation:	switch	selects number of channels and width of paper tape.
Unit Selected:	switch and light	indicates paper tape punch is on-line. Selects card punch or B 341.
Low Tape:	light	35 feet of tape or less remains on supply reel.

.13 Availability: . . . . . . 3 to 4 months.

.14 First Delivery: . . . . . January, 1964.

INPUT-OUTPUT: B 320/321/325 LINE PRINTERS

.1 GENERAL

.11 Identity: . . . . B 320 Line Printer.
B 321 Line Printer.
B 325 Line Printer.

.12 Description

The B 321 Line Printer prints at the maximum rate of 700 single-spaced alphameric lines per minute. When average line spacing occurs at one-inch intervals, the speed is reduced to about 540 lines per minute. Sixty-four characters (10 numeric, 26 alphabetic, and 28 special symbols) can be printed in a line of 120 print positions. The comprehensive character set is listed in the Data Code Table on page 201:141.100.

The B 320 Line Printer is a slower version of the B 321 and is offered at a substantially reduced price. This slower model operates at a peak speed of 475 lines per minute. The B 325 Line Printer increases the printing flexibility by providing 132 print positions. Except for these differences in speed and print-block size, respectively, the B 320 and B 325 Line Printers are functionally identical with the B 321 model. Therefore, in the description that follows, reference is made only to the characteristics and capabilities of the B 321.

The B 321 Line Printer contains its own 120-character buffer, as well as the necessary control equipment. At the peak speed of 700 lines per minute, the total print-cycle time is 85.7 milliseconds. Of this time, only 1.3 milliseconds is consumed in loading the buffer. As soon as the buffer is loaded, printing commences and the central processor is free for other processing.

Line advance can occur before or after printing and can be specified as 0, 1, or 2 lines. Skipping, before or after printing, is controlled by a 12-channel punched tape loop and can occur at a rate of 25 to 40 inches per second.

Printing is performed on continuous card or paper forms. Forms width can extend from 5 to 20 inches; the maximum length is 22 inches per form. Output format spacing is 10 characters per inch horizontally and 6 or 8 lines per inch vertically.

As many as five carbons plus the original form will function properly in the printers. The forms are loaded in the cabinet beneath the printing mechanism and are transported through the unit by means of pin-fed tractors to the self-maintaining stacker. A Paper-Exhausted indicator/switch and several broken-paper detectors provide error-condition indications and serve to interlock the central processor.

Line formatting, spacing, and skipping are under control of the stored program. When a print instruction is initiated, 120 alphameric characters from anywhere in core storage are loaded into the printer's buffer. As soon as the buffer is full, the central processor is freed and the printing cycle begins. The translation from Burroughs Common Language (BCL) internal code to the 64-character print set is performed automatically. The actual printing is accomplished by hammer strokes against a continuously-rotating engraved drum. Once the drum has made a complete revolution, every character will have been printed, and the paper motion can begin. The next printing cycle cannot begin until all paper motion has ceased.

A number of functional controls are provided to enable the operator to adjust for variances in the size of the forms and the number of interleaved carbons. The operator can also adjust the horizontal and vertical alignment of the forms and the print quality of individual print positions.

Error checks are made for proper character parity in the buffer, for drum rotation synchronization, and for the presence of paper. Errors are signalled by a control panel indicator and result in a halt of the system. Error conditions and unoperational status can be tested by the Unit Interrogate command, which is optional in the B 200/300 Series central processors. Printer timing conflicts result in an interlock of the printer until execution of the print instruction is possible.

The differences between the B 320, B 321, and B 325 Line Printers, with regard to both capabilities and configuration requirements, are indicated in Table I. A noteworthy feature, the Dual Printer Control, is optional for any central processor in the Series except the B 100 Series models and the VRC. With this feature two line printers, utilizing the print buffering to full advantage, can theoretically operate simultaneously and at their rated speeds.

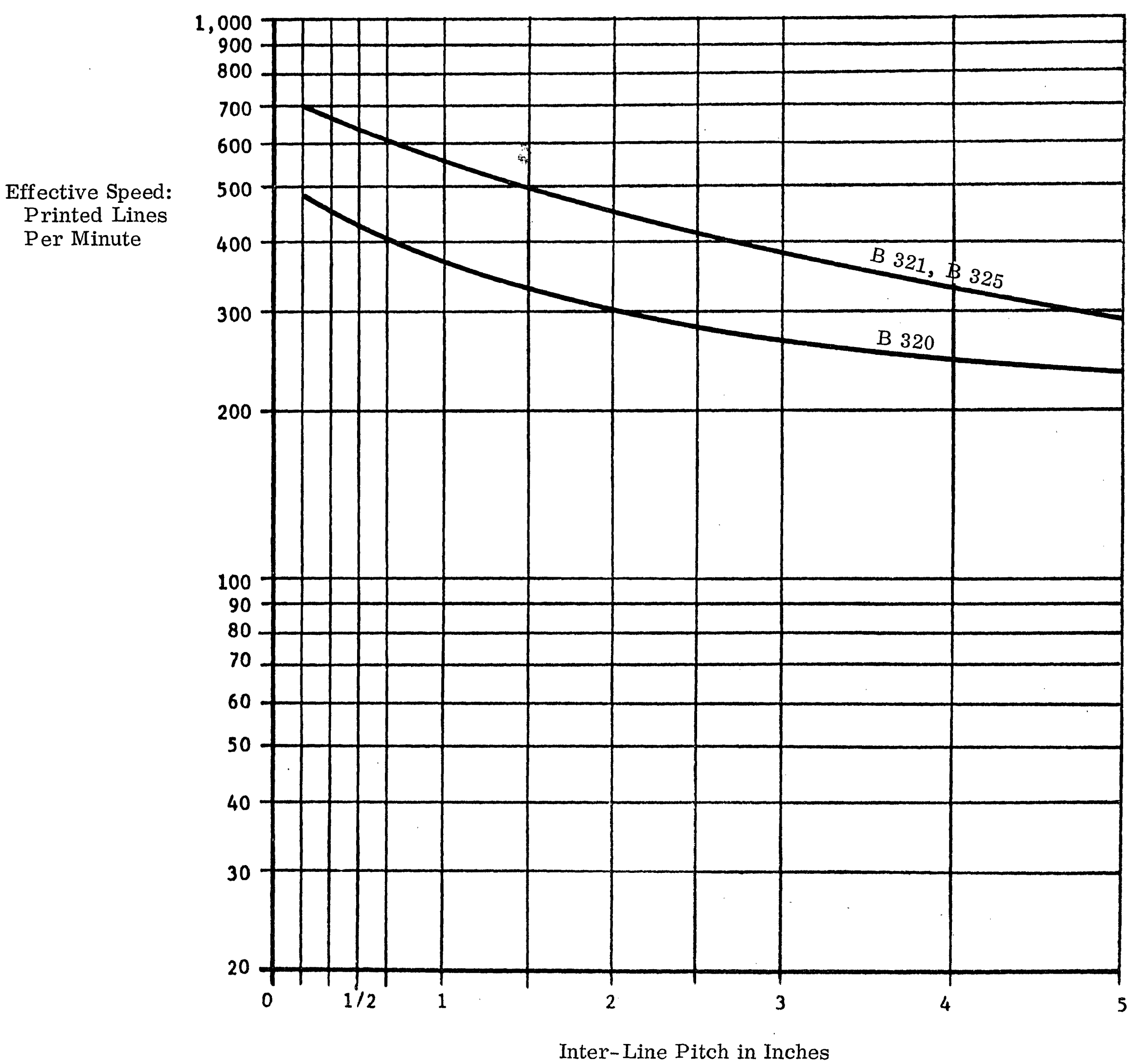
The graph on the following page illustrates the effective speeds of the three Line Printers under various spacing conditions.

(Contd.)

TABLE I: LINE PRINTER CHARACTERISTICS

Line Printer Model	B 320	B 321	B 325
Maximum speed (lines per minute)	475	700	700
Number of print positions	120	120	132
B 100/200/300 Series availability	All models	All, with adapter for B 100 Series	B 200/300 Series 6-μsec Processor

Effective Speed:
B 320, B 321, and B 325 Line Printers



INPUT-OUTPUT: B 328/329 LINE PRINTERS

.1 GENERAL

.11 Identity: . . . . B 328 Line Printer.
B 329 Line Printer.

.12 Description

The B 328 and B 329 Line Printers operate at a maximum rate of 1,040 lines per minute at single spacing when the characters to be printed are limited to those in a continuous 37-character segment of the print drum. The peak rate can also be maintained while printing and triple-spacing if a 16-character "numeric and edit" set is used. As larger character sets are used, the operational speeds are reduced, as shown in Table I below. When the entire 64-character set is utilized, the single-spaced speed will not fall below 734 lines per minute.

The only differences between the B 328 and B 329 Line Printers are in the number of print positions provided per line and in the configuration requirements for each model. The B 328 has 120 positions on a line and can be connected to any B 100/200/300 Series central processor except the B 100 line. The B 329 has 132 print positions and can function only with the B 200/300 Series six-microsecond central processor.

Burroughs' standard 64-character drum printer set has been statistically analyzed and regrouped on the drum according to frequency of use. The 37 most frequently used characters (10 numeric, 26 alphabetic, and the period) are arranged in consecutive locations around the drum. The revised drum arrangement and a "quick cancel" memory result in the improved performance of the B 328 Line Printer over the 700-line-per-minute B 321 model.

Printing occurs after the central processor loads the printer's buffer with 120 or 132 characters from core storage. The processor is free for additional operations as soon as the buffer is loaded (within 1.3 milliseconds). As each character in the buffer is printed, its buffer position is set to a blank. Immediately upon detection of a completely blank buffer, paper motion begins. (A minimum of 16 characters on the drum must pass the printing mechanism before paper advancing can begin.) The start of paper motion is therefore not contingent on the completion of a full drum revolution.

The operational speeds of the printers are governed by the rotational speed of the print drum and the paper advance speeds. The rotational speed is 1,040 rpm, or one revolution every 57.7 milliseconds. The printing or bypassing of each character on the drum requires 0.9 millisecond. To advance the form a single space requires 24 milliseconds for the first space and 7 milliseconds for each additional space. Therefore, to maintain printing speeds of 1,040 lines per minute, the total printing and spacing time must not exceed 57.7 milliseconds. On this basis, up to 37 consecutive alphameric characters can be printed and single spacing can occur during a single drum revolution. The chart below indicates effective speeds as character sets and spacing demands are varied.

Standard features of the B 328 and B 329 Line Printers include a ribbon-tracking device to sense and control ribbon mistracking, and duplicate controls and indicators on the rear of the cabinets to assist the operator. Except for these added features, the B 328 and B 329 Line Printers have the same physical characteristics, forms controls, and error-checking devices as the B 320, B 321, and B 325 printers described in the previous report section, page 201:081.100.

The first deliveries of the B 328 and B 329 1,040-line-per-minute printers are scheduled for June, 1965. Availability has been set at eight months.

TABLE I: EFFECTIVE SPEEDS OF B 328 AND B 329 LINE PRINTERS

Lines Advanced per Line Printed	Printed Lines per Minute Using Various Consecutive Character Sets		
	16 Characters	37 Characters	64 Characters
1	1040	1040	734
2	1040	692	677
3	1040	692	626
4	692	624	584
5	624	560	546

INPUT-OUTPUT: MULTIPLE TAPE LISTERS

.1 GENERAL

.11 Identity: . . . . B 322 Multiple Tape Lister.
B 323 Multiple Tape Lister.
B 326 Multiple Tape Lister.
B 332 Multiple Tape Lister.
B 333 Multiple Tape Lister.

.12 Description

The Burroughs Multiple Tape Listers provide high-speed master and detail listings of MICR documents as they are read by a MICR Sorter-Reader. From 6 to 18 individually-controlled listing tapes can be controlled by a single central processor, enabling the contents of each Sorter-Reader pocket to be listed on a separate tape. In addition, master and difference tapes can be printed without interrupting the flow of MICR documents. Up to three listing tapes can be printed upon simultaneously, at speeds up to 1,600 lines per minute for each tape. All the tapes can be skipped 2.5 inches or slewed 10 inches simultaneously, if desired. From one to three Multiple Tape Listers can be connected to a B 100/200/300 Series Central Processor. Each lister unit controls six paper tapes.

Printing is performed on 2.5-inch-wide, single or two-ply adding machine forms. Print lines can extend to 22 print positions on each tape, with a horizontal spacing of 10 positions per inch and vertical spacing of 6 lines per inch. Each lister unit contains an engraved print drum composed of six 22-column segments mounted on a horizontal shaft. Printing occurs when hammer strokes drive the paper forms against the symbols on the revolving drum. The drum's character set can range from a numeric-and-special-symbol 24-character set to a 40-character set with full numeric and alphabetic printing capability.

Each configuration of one, two, or three Multiple Tape Listers includes a 44-character buffer and a self-contained set of controlling devices. The buffer is interlocked from the time it is loaded by the central processor until printing is completed and paper motion begins. An attempt to gain access to the buffer during the print cycle will cause the central processor to be delayed until the print cycle is completed.

The central processor loads the buffer in 0.7 millisecond. Immediately after the brief buffer-loading operation, the central processor is released for further operations. Contents of the first 22 positions of the buffer are then printed on one listing tape, and positions 23 to 44 are simultaneously printed on another. Individual tape and lister unit designations are controlled by the stored program. The two sections of the buffer can contain the same or different information.

Single spacing of the tapes after printing is performed automatically. The tapes can also be individually spaced, skipped, or slewed at any time. Skipping a tape 2.5 inches after printing interlocks the print mechanism for 100 milliseconds, but it should be noted that multiple tape listing operations will normally be single-spaced.

The paper listing tapes are 2.5 inches wide and are provided in rolls or in fan-fold form in lengths up to 1,000 feet. The paper advance operations are controlled by pressure rollers that direct the tapes to stackers at the rear of the cabinets. Stacker capacity for each tape is 1,000 feet. Forty-five minutes of consecutive printing on a single tape could be accomplished before exhausting the paper supply and halting the system.

The Print on Lister command provides for branching to alternative routines when a print error occurs. However, this capability is present only when the listers are used with the B 200/300 Series 6-microsecond central processor. This level of central processor also has the optional capability to test the operational status of the listers and to continue processing if they are found to be unavailable.

Duplicate control panels are located at the front and rear of the lister cabinets. Any or all listing tapes can be manually skipped by a paper-advance switch. Also, since two listers can be used alternatively with up to two Burroughs Line Printers on the same system, a manual Printer/Lister Selector switch can be provided.

A print check indicator will be illuminated if data is received in the buffer with improper parity or if the buffer and drum-revolution timings are out of synchronization. If branching upon error indicators has not been specified by the program, the central processor will halt on the next instruction that references the lister.

The individual characteristics and capabilities of Burroughs' five Multiple Tape Lister models are described below.

.121 B 322 Multiple Tape Lister

The B 322 Lister prints 22-position lines at speeds up to 1,600 lines per minute. It has a 24-character print set consisting of 10 numeric, 10 alphabetic (B, C, D, L, M, R, S, T, X, and Y), and 4 editing characters. The alphabetic set is designed to provide indicative symbols for most banking operations. One or two 6-tape B 322 Listers can be attached to any central processor in the B 100/200/300 Series. Optional features are available to allow the simultaneous skipping or slewing of all listing tapes (either 6 or 12), or of all but the master tape. First delivery of the B 322 Lister occurred during the second quarter of 1962.

.122 B 323 Multiple Tape Lister

The 323 Lister prints at a maximum speed of 1,600 lines per minute, provided that a 16-character set of 10 numeric and 6 special symbols is used exclusively. The noteworthy feature of the B 323 Lister is the expansion of the character set to 40 characters. Full alphabetic printing capability is thereby offered, although at a greatly reduced rate of speed. The lister will print at 600 single-spaced lines per minute in the alphameric mode, as opposed to the 1,600 line-per-minute rate in the special 16-character numeric mode. One or two B 323 Listers can be connected to any B 200 or B 300 Series Central Processor. Simultaneous tape skipping is a standard feature, but simultaneous tape slewing is optional. First delivery of this version of the Multiple Tape Lister occurred in January, 1964.

.123 B 326 Multiple Tape Lister

The B 326 Lister differs from the B 322 model described in Paragraph .121 above only in its printing speed. The B 326 prints at a maximum rate of 1,250 lines per minute. It was designed to operate efficiently with the B 106 and B 107 1,200-document-per-minute Sorter-Readers.

.124 B 332 and B 333 Multiple Tape Listers

The B 332 18-tape Multiple Tape Lister subsystem is formed by combining a B 332 Master Lister with two B 333 Slave Lister sections with six listing tapes each. The 44-character buffer and controlling devices are contained within the B 332 unit. Single-spaced printing speeds range from 800 alphameric to 1,600 numeric lines per minute. Up to three listing tapes can be printed upon simultaneously. The characters in buffer positions 1 to 22 can be printed on both the master tape and a selected detail tape. The second section of the buffer can be loaded with information unrelated to the document-processing operation. This information can be printed concurrently on a selected third tape.

The provision to print on 18 individually-controlled tapes provides functional compatibility with B 116 16-pocket MICR Sorter-Reader. Full tape skipping and slewing flexibility is offered as standard equipment. One B 332 Lister and 0, 1, or 2 B 333 Slave Listers are available only for use with the B 300 Series Central Processor; they cannot be used with older B 100/200 Series systems. The availability of these units is quoted as 6 to 8 months.

INPUT-OUTPUT: MAGNETIC TAPE UNITS

.1 GENERAL

.11 Identity: . . . . B 421 Magnetic Tape Unit.
B 422 Magnetic Tape Unit.
B 423 Magnetic Tape Unit.
B 424 Magnetic Tape Unit.
B 425 Magnetic Tape Unit.

.12 Description

The Burroughs Magnetic Tape Units provide a range of transfer rates from 18,000 to 72,000 characters per second and packing densities of 200, 556, and 800 characters per inch. Alphameric characters in binary-coded decimal form are stored on 0.5-inch Mylar-based tape on reels 10.5 inches in diameter. The reel capacity is 2,400 feet, allowing a maximum of 22.1 million characters per reel at the 800 characters-per-inch density. Magnetic tape operations are not buffered, and, with the exception of tape rewinding and stopping, they require the use of the central processor throughout.

Each central processor in the B 100/200/300 Series can control up to six magnetic tape units. Operational problems with any one tape unit will not affect the performance of the others. Reading and recording operations are performed only in the forward direction. The tape reading operation transfers data from tape to core storage until a 0.75-inch interblock gap is sensed. A special end-of-information mark is stored in memory following the last character transferred. The recording operation transfers information from core storage and records it on tape until the end-of-information mark in storage is sensed. The tape must come to a complete stop after either of these operations before any other tape operation can be initiated by the central processor.

Data is recorded in variable-length blocks. The size of the blocks can extend from seven characters to the limit of core storage. At a block size of 1,000 characters, the 200, 556, and 800-bit-per-inch tape units can store 4,900, 11,100, and 13,800 blocks, respectively, on a 2,400-foot reel of tape. Given the same 1,000-character blocks, the effective data transfer rates of the 18KC and 72KC tape units will be 14,400 and 41,800 characters per second, respectively. Relative speeds and capacities of the five Burroughs tape unit models are listed in Table I. A graph is also provided (page 201:091.801) to demonstrate the variation in effective speed of each model as the size of the data blocks increases.

In addition to the provisions for tape reading and recording, the capability is provided to backspace the tape until an interblock gap is sensed, and to erase the tape forward until a group mark is encountered in core storage. The time required to set the tape in motion in a backward direction is 11.2 milliseconds. By comparison, the start time for a tape read operation will be from 5.0 to 6.8 milliseconds. Start-stop overhead timings are also supplied in Table I.

Binary tape reading and recording capabilities are provided when any of the tape unit models are used with a B 200/300 Series 6-microsecond

TABLE I: CHARACTERISTICS OF BURROUGHS MAGNETIC TAPE UNITS

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, char per sec	Interblock Gap Lengths			Efficiency, % (3)		Demand on Core Storage, %	Rewind Speed, inches per sec
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks		
B 421	90	200 556	18,000 50,000	0.75	13.8	248 690	27.7 13.0	80.5 60.0	100	320
B 422	120	200 556	24,000 66,000	0.75	11.0	264 726	26.2 12.1	75.0 59.0	100	320
B 423	120	200	24,000	0.75	10.0	240	26.2	75.0	100	320
B 424	83	800	66,000	0.75	10.0	660	13.1	60.2	100	320
B 425	90	200 556 800	18,000 50,000 72,000	0.75	10.0	180 500 720	27.7 13.0 12.2	80.5 60.0 58.1	100	320

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.
(2) Effective number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.

.12 Description (Contd.)

central processor. Any binary-coded decimal code can thereby be read and stored in memory, where a programmed code translation can be effected if desired. The binary recording operation is terminated when every character in memory from the point of origin to the upper end of core storage has been recorded, in a single tape block.

The tape units used in the B 100/200/300 Series are fully compatible with those of the Burroughs B 5500 system. Compatibility is also achieved with the IBM 729 and 7330 tape units using binary-coded-decimal coding at 200, 556, or 800 rows per inch. The ability to read tape in the binary mode adds still further possibilities in the area of tape compatibility.

When reading or recording, tape is pulled from a vacuum-column buffer by a moving capstan and pinch-roller assembly and passed under a dual-gap read/write head. Tape speed past the head varies from 83 to 120 inches per second according to the tape unit model (see Table I). The read section of the head follows the write section by 0.15 inches to allow for immediate read-after-write checking. Tape is then drawn into another vacuum column preceding the take-up reel to minimize tape damage and breakage.

Data on tape is arranged in seven-bit rows, six bits for information and one for even-parity checking. The number of rows per block is limited only by the size of the available core storage. When recording information in the binary mode, the parity scheme is odd, consistent with that of core storage.

In addition to the data-transfer validation provided by the read-after-write check, several other checks are provided. Row parity is checked during both reading and recording. A longitudinal check character for each block is developed during recording and checked during subsequent readings. Data transfer errors of any kind cause an immediate program branch to a corrective routine. Program branching will also occur when a reflective tape marker is sensed at the end of a tape reel during recording, and when a special final-block character is recognized during reading.

Reel loading is facilitated by a latch-leader device affixed to every reel. The leader is latched to a section of tape permanently attached to the take-up transport, and a Load button is pushed. Tape positioning for proper operation is then performed automatically. Density-switching and high-speed rewinding (320 inches per second) can also be controlled at the tape unit's control panel.

The differentiating characteristics between the five models of Burroughs magnetic tape units are described in the paragraphs that follow and in the associated chart and graph.

.121 B 421 Magnetic Tape Unit

The B 421 provides peak data transfer rates of 18,000 or 50,000 characters per second at packing densities of 200 or 556 rows per inch. It can be connected to any model B 200 or B 300 Series Central Processor, but cannot be combined with any other tape unit model except the B 425. First delivery occurred during the third quarter of 1962.

.122 B 422 Magnetic Tape Unit

The densities of the B 422 Tape Unit are the same as those of the B 421 model, but its peak data transfer rate has been increased to 24,000 or 66,000 characters per second. The B 422 Tape Unit can be connected to the B 200/300 Series 6-microsecond Central Processor only. It can function in combination with both the B 423 and B 424 models. The B 422 unit has been available since January, 1964.

.123 B 423 Magnetic Tape Unit

The B 423 Tape Unit is basically the same as the B 422, except that it lacks the high speed and high density options. Its peak data transfer rate is 24,000 characters per second. Tape start time in the B 423 has been reduced to 5.0 milliseconds, as compared with 6.8 milliseconds for the B 422 model. The B 423 can be connected to any central processor in the B 100/200/300 Series and can be used in combination with the B 422 and B 424 models. First delivery was made in February, 1964.

.124 B 424 Magnetic Tape Unit

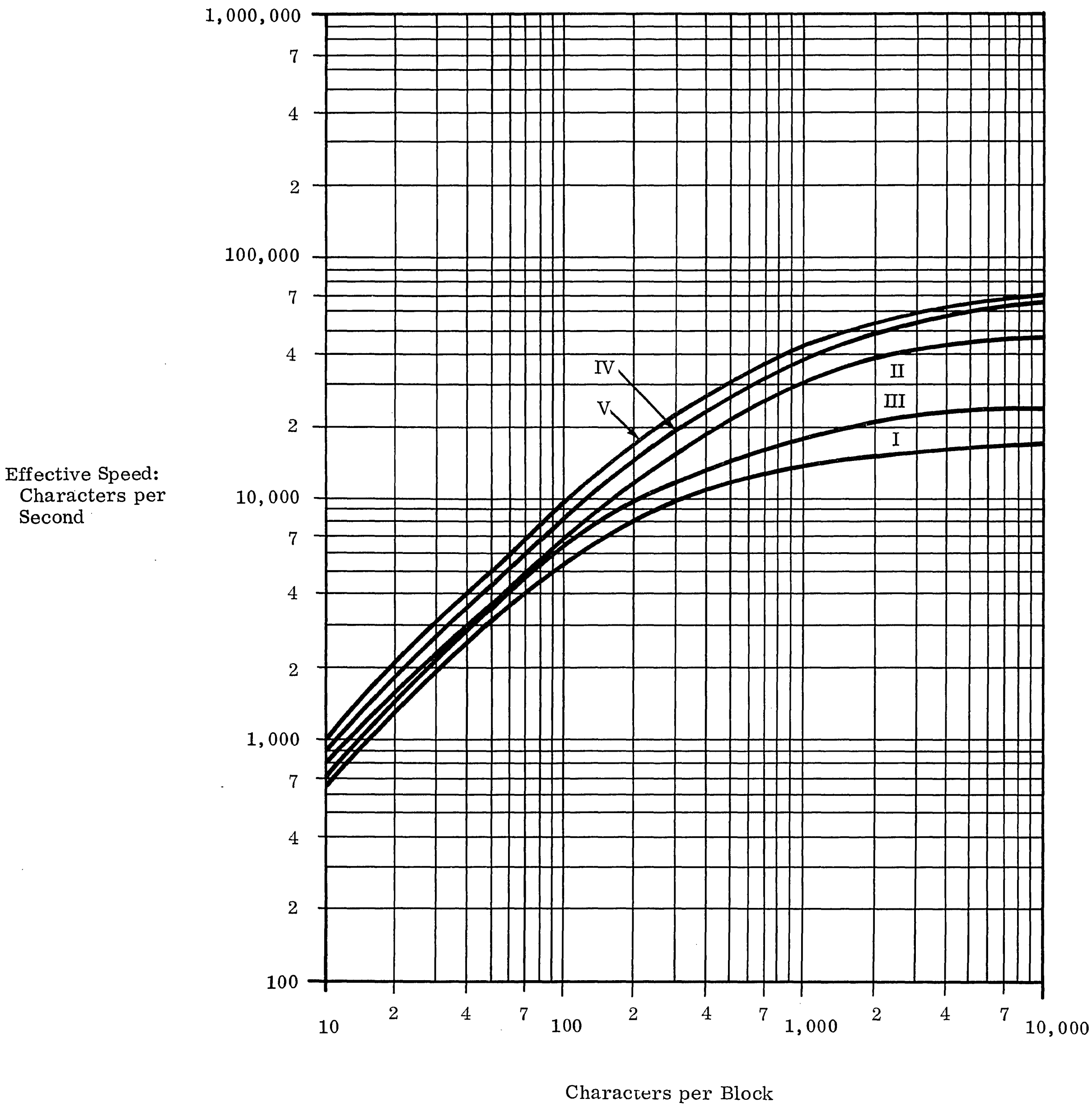
The increased packing density of 800 rows per inch was introduced to the Burroughs line of tape units when the B 424 model was delivered in May, 1965. Its peak data transfer rate is a non-variable 66,000 characters per second at a tape speed of 83 inches per second. Up to six B 424 Tape Units can be used with any B 200/300 Series 6-microsecond Central Processor, but the B 424 cannot be used in the same system with any other Burroughs tape unit except the B 422.

.125 B 425 Magnetic Tape Unit

With the announcement of its B 300 Series in February, 1965, Burroughs introduced the B 425 Tape Unit. This unit provides packing densities of 200, 556, and 800 rows per inch, and a tape speed of 90 inches per second. Thus, in a single unit, full compatibility has been achieved with all of the IBM 7330 and 729 tape units. The B 425 Tape Unit can be connected to the B 300 Series Central Processor only. Its use requires a special processor control module.

(Contd.)

Effective Speeds: Burroughs Magnetic Tape Units



LEGEND

I. Models B 421 and B 425 at 200 char/inch.
II. Models B 421 and B 425 at 556 char/inch.
III. Models B 422 and B 423 at 200 char/inch.
IV. Model B 422 at 556 char/inch.
V. Model B 425 at 800 char/inch.

INPUT-OUTPUT: B 401 RECORD PROCESSOR

.1 GENERAL

.11 Identity: . . . . B 401 Record Processor.

.12 Description

The B 401 Record Processor and Console provides the VRC System (Page 201:031.500) with the capability for automatic handling, reading, and updating of unit records. Ledger cards, such as those used in banking and inventory applications, are accepted as direct computer input for processing and updating, providing visual account histories on the records.

By means of a programmed cycle of read, process, print, and update, ledgers can be handled at 45 per minute at 100 percent account activity, printing one line of new information on each ledger. Inactive accounts are passed by at 180 per minute.

On a magnetic stripe on the reverse side of each ledger, information is stored about the account status and the position of the most recent line of printing. This information (maximum of 80 characters) is read as the ledger is moved from a "ready" station past a magnetic read head. The VRC Central Processor determines whether the ledger should be stopped at the print area of the Record Processor, or ejected as inactive, on the basis of other data read into the Central Processor (from an MICR Sorter-Reader, for example).

If the account is to be updated, new balance information is calculated and printed on the ledger. As the ledger is ejected, new information is recorded on the magnetic stripe on the reverse side of the ledger. A check head reads the information just recorded for comparison with the information in core storage.

The print station may also contain one or two continuous forms (side by side), which can be printed upon separately or together with ledgers. Presence of a ledger will mask some of the form printing area. If forms printing is desired in this case, it can be done after the ledger is ejected. Printing is done with automatic single spacing at a maximum speed of 214 lines per minute while printing on one ledger, or on forms. Printing format is 160 positions per line and six lines per inch. Four of the print positions are blocked by ribbon guides, leaving 156 positions available for actual printing. Since the ribbon guides are movable, a print instruction transfers 160 characters per line. Instructions are available for spacing the forms and ledger one line without printing. The two forms and the ledger can be moved in any combination in this instruction. Printing is accomplished with a 12-character set on each type bar, containing only the 0-9 and 2 special symbols.

The Console of the B 401 provides for manual operation of the Record Processor. The Console contains a 12-column numeric keyboard and a set of special character keys. These keys can be read by the VRC Central Processor, under program control. Ledger cards are fed from one of three hoppers: main, auxiliary, and a single-card hopper. Two stackers can be selected: primary or auxiliary. All hopper and stacker selection is under program control.

An Optical Reader (optional) aids in comparison of account numbers during balance transfer operations.

.14 First Delivery: . . . . . 3rd qtr. 1961.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . ledgers: pinch rollers.
forms: sprocket drive.

.22 Sensing and Recording Systems

.221 Recording system: . . . printed characters: type bars.
magnetic characters: magnetic head.

.222 Sensing system: . . . . magnetic head for magnetic characters.
optional Optical Reader for special digits at auxiliary read station.

.23 Multiple Copies

.231 Maximum number: . . . forms: 1 + 2 carbons.
ledgers: none.

.24 Arrangement of Heads

Use of station: . . . . . reading ledger magnetic stripe.
Stacks: . . . . 1.
Heads/stack: . . . . 1.
Method of use: . . . . . . ledger passes head.
Use of station: . . . . . . writing onto ledger magnetic stripe.
Stacks: . . . . 1.
Heads/stack: . . . . 1.
Method of use: . . . . . . ledger passes head.
Use of station: . . . . . . checking data recorded on magnetic stripe.
Stacks: . . . . 1.
Heads/stack: . . . . 1.
Method of use: . . . . . . ledger passes head.

(Contd.)

.24 Arrangement of Heads (Contd.)

Use of station:...... printing on ledger or forms.
Stacks:........... 1.
Heads/stack:....... 160.
Method of use:...... one line at a time.
Use of station:...... reading special binary characters on ledger.
Stacks:........... 1.
Heads/stack:....... 1.
Method of use:...... optical; ledger passes head.

.25 Range of Symbols

Numerals: .... 10 0-9.
Letters:.......... 5 see below.*
Special:.......... 9 see below.*
Alternatives: ...... upon special request.
FORTRAN set: ..... no.
Req. COBOL set: ... no.
Total: .... 12 at one time on any type bar.

* Special symbols and letters:........ one type bar contains numerals 0-9 plus 1 of the groups of 2 characters shown:

LS	and	R	RT	and	CM
X	and	Y	-	and	,
.	and	,	A	and	D
OD	and	SC	DM	and	SC
.	and	Y			

.3 EXTERNAL STORAGE

.31 Form of Storage

		Unit Record Cards	Journal Forms
.311	Medium:	ledger cards with magnetic stripe on rear side	paper, fanfold, multiset.
.312	Phenomenon:	printing on front side; magnetization on rear side	printing by type bars.

.32 Positional Arrangement

		Unit Record Cards	Journal Forms
.321	Serial by:	printing: 1 row of 140 char max at 6 rows/in magnetic char: serial by 80 char.	1 row of 160 char at 6 rows/in.
.322	Parallel by:	140 col max at 10 col/in	160 col at 10 col/in.
.324	Track use:	all for data	all for data.
.325	Row use:	all for data	all for data.

.33 Coding:.......... as in Data Code Table No. 4.

.34 Format Compatibility: none.

.35 Physical Dimensions

.351 Overall width:...... Ledger: allowable width 6.5, 7, 8, 9, 10, 11, 12, 13, or 14 inches.
Forms: 3.25 to 18 inches by vernier.
Combined width of both forms used may not exceed 18 inches, including the space between them. Minimum space is 0.375 inch.

.352 Length
Ledger:......... 11 inches.
Forms:......... 3.5, 5.5, 7, or 11 inches.

.353 Maximum margins

	Ledgers	Forms
Left:	0 inch	1 inch.
Right:	0 inch	1 inch.
Top:	2 inches	0.5 inch.
Bottom:	1 inch	0.5 inch.

.4 CONTROLLER:..... built into central processor.

.42 Connection to System

.421 On-line:.......... one B 401 Record Processor, in VRC System only.
.422 Off-line:.......... none.

.44 Data Transfer Control

.441 Size of load
Printer:......... 160 char.
Magnetic stripe: ... 80 char. max.
.442 Input-output areas: .. core storage.
.443 Input-output area access: .... each character.
.444 Input-output area lockout: .... none.
.445 Table control:...... none.
.446 Synchronization: .... automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

		Printer	Magnetic Stripe
.511	Size of block:	160 char	up to 80 char.
.512	Block demarcation		
	Input:	none	end-of file symbol.
	Output:	counter	group mark (≢) in core storage.

.52 Input-Output Operations

		Printer	Magnetic Stripe
.521	Input:	none	up to 80 char specified by ≢.
.522	Output:	160 char specified by counter	up to 80 char marked by group mark in core storage ≢.
.523	Stepping:	single space	none.
.524	Skipping:	to start of next form	none.
.525	Marking:	none	none.
.526	Searching:	none	none.

.53 Code Translation: . . . automatic.

.54 Format Control: . . . . by program.

.55 Control Operations

Select hopper: . . . . . . yes.
Select stacker: . . . . . yes.
Select format: . . . . . . no.

.56 Testable Conditions: . . none.

.6 PERFORMANCE

.61 Conditions

I: . . . . passing inactive account.
II: . . . . reading active accounts; printing one line per ledger.
III: . . . . single-space printing.

.62 Speeds

.621 Nominal or peak speed: . . . . I; 180 ledgers/min.
II; 44 ledgers/min.
III; 214 lines per min.

.622 Important parameters
Read ledger: . . . . . . 282 msec.
Read data entry keyboard: . . . . 1.23 sec.
Processing time on Condition II: . . . . . 31 msec.
Line advance time when printing consecutive lines: . . . . 35 msec.
Align ledger: . . . . . . 189 to 345 msec depending on line on ledger.
Write on magnetic stripe and eject ledger: . . . . 630 to 474 msec depending on starting line on ledger.
Print one line on ledger: . . . . 250 msec.

.623 Overhead: . . . . none; feeding rate depends on program. However, if printing successive lines on same ledger, print cycle goes from 281 msec to 316 msec if processing time exceeds 31 msec.

.624 Effective speeds: . . . . II; 214/(3.82 + N) ledgers/min. N = No. lines printed/ledger.
66 msec available processing time/line printed.

.63 Demands on System

Component	Condition	msec per ledger	or	Percentage
Processor:	I	282		84.
Processor:	II	1,084 av.		80.
Processor:	III	250		89.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method	Comment
Form width	tractor	by operator.
Form depth	cam	by operator.

.72 Other Controls

Function	Form	Comment
Data entry:	keyboard	for entry of data.
Form and record movement:	switches	manual positioning.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Forms:	stack of 6 inches.
Ledgers:	
Primary hopper:	1,000 ledgers.
Auxiliary hopper:	500 ledgers.
Manual feeder:	1 record.
Primary stacker:	1,000 ledgers.
Auxiliary stacker:	150 ledgers.

.732 Replenishment time: . . 1 to 2 minutes; unit needs to be stopped.

.733 Adjustment time: . . . . 1 to 5 minutes.

.734 Optimum reloading period: . . . . ledgers; 22 minutes if printing on each ledger.
forms; 76 minutes if printing at maximum speed on 300 3-part sets 11 inches long.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	post-record read	halt; ledger ejected; alarm. *
Reading	check	stop computer; alarm; records sent to auxiliary stacker; B 401 console alarm. *
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	none.	
Nearly exhausted forms:	check	alarm.
Imperfect medium:	none.	
Timing conflicts:	interlock	wait.
Two documents fed:	check	stop computer, alarm; records sent to auxiliary stacker; B 401 console alarm. *
Missing information:	check	program branch.
Stacker full:	check	halt and alarm.
Hopper empty:	check	halt on read instruction.
End of form when printing:	check	program branch.
Record out of alignment:	check	halt; alarm, record ejected. Program continues in sequence when Continue button on B 401 console is depressed.
Print error:	check	spacing suppressed; halt, alarm. *
Ledger missed:	check	halt; alarm; ledger ejected.

* Program branch when Continue button on B 401 console depressed.

INPUT-OUTPUT: MICR SORTER-READERS

.1 GENERAL

.11 Identity: . . . . B 101 Sorter-Reader.
B 102 Sorter-Reader.
B 103 Sorter-Reader.
B 104 Sorter-Reader.
B 106 Sorter-Reader.
B 107 Sorter-Reader.
B 116 Sorter-Reader.

.12 Description

The Burroughs Sorter-Readers are designed to read magnetically-encoded documents at speeds up to 1,560 documents per minute and to sort these items into one of 13 or 16 different pockets. The Sorter-Readers can serve as high-speed input devices to any of the B 100/200/300 Series banking systems, or as off-line, general-purpose MICR document sorters. On-line reading speeds are matched by the printing speeds of the Burroughs Multiple Tape Listers (see Section 201:083), providing integrated systems for most banking operations.

Documents are fed into the Sorter-Reader from a hopper holding up to 3,000 documents of intermixed sizes. Two belts separate and feed items at a speed of 150 inches per second. The documents are accelerated to 400 inches per second and aligned for passage past the read head. The encoded characters are reinforced by a magnetic charge and then read serially from right to left. If the characters are defectively encoded or improperly formatted, or if the documents do not meet specification sizes, the item is directed to a reject pocket. After the items are read, they pass an optional endorsing station, where the individual bank's endorsement can be printed on each document without reducing the Sorter-Reader's rate of speed. In place of the endorsing station, a standby station can be provided to allow for the feeding and reading of individual documents in a demand mode under control of the central processor.

After the magnetically-encoded information is read into the second of the central processor's input buffers and then transferred to core storage (within two milliseconds), the stored program determines the document's proper pocket selection and transfers this information back to the Sorter-Reader. A specific blade is then activated and the document enters the proper blade-transport, where it is sped by belts to its selected pocket. The capacity of each standard-sized pocket is 800 items, and both the pockets and the input hopper can be emptied and replenished while the Sorter-Reader is in high-speed operation.

The Sorter-Reader has the ability to read 14 magnetic characters printed in Font E-13B, the standard adopted by the American Bankers' Association. Included in the character set are the numerals 0 through 9 and four special symbols: amount, on us, transit, and dash. Up to 59 characters can be encoded on each document, according to strict ABA formatting rules. The characters are spaced automatically in core storage into seven 12-character fields.

The Sorter-Reader has been designed to handle paper documents ranging in thickness from 0.0040 to 0.0075 inch. Document size tolerances vary if the items are not uniform in size:

	Uniform Size	Intermixed Sizes
Length:	5.75 to 9.5 inches	5.9375 to 9.0625 inches
Width:	2.5 to 4.25 inches	2.6875 to 4.0625 inches

The Sorter-Readers can operate on-line in one of two modes: demand and flow. When a document is read in demand mode, it will remain in the standby station indefinitely until a pocket-select instruction routes it to its pocket. A maximum rate of 400 items per minute can be achieved in this mode. Flow mode operation establishes continuous feeding of documents at the full speed of the Sorter-Reader. In order to maintain this flow, each read instruction must be followed by a pocket-select instruction within approximately 10 milliseconds. After pocket selection, approximately 10 milliseconds of additional processing time remain before the next read instruction must be initiated. If these timing restrictions are exceeded by the stored program, the items in transport will be rejected and the system will halt.

In the flow mode, the reading operation can be buffered or unbuffered. From 14.4 to 19.4 milliseconds are required to read the document and transfer the data either to the buffer or directly to core storage. Buffered reading permits this time to be utilized for processing. Buffer unloading requires only two milliseconds of the central processor's time, but this time occurs during the critical period before pocket selection. The advantage of unbuffered reading lies in the extra two milliseconds of processing time available before the pocket-select instruction must be given.

Sorting speeds are determined by the length of the documents being read. The peak speed of 1,560 items per minute can be maintained only when processing a batch of items with a uniform length of 5.75 inches. Speeds for longer documents can be conveniently estimated by multiplying the feeding speed of 150 inches per second times 60, and dividing by the average length of the documents being processed. Thus, for 9-inch documents, sorting proceeds at 1,000 documents per minute. (This relationship is not valid for the B 106 and B 107 models, which have a peak speed of only 1,200 documents per minute.)

In order that each document can be read and sorted properly, proper spacing between documents must be maintained. Improper spacing is detected by strategically-located beams of light, causing the potentially erroneous documents to be routed to the reject pocket. Document feeding is stopped for 300 milliseconds for the rejecting process,

.12 Description (Contd.)

after which it resumes automatically. Such rejects will also occur if the documents fail to meet size specifications. During continuous or flow-mode operations, as well as during off-line sorting, the documents must be within 7.75 and 10.0 inches from each other in order to maintain Sorter-Reader speed and insure accuracy of data transmission.

An optical sensing device, the Batch Ticket Detector, automatically halts the flow of items at the conclusion of a controlled batch of documents. Summary operations can then be as lengthy as desired. This sensing device is located just beyond the mouth of the feeder, preventing the feeding of any document from the following batch before the transport can be halted. Another type of feed halt can occur if feeding is unsuccessful after 180 milliseconds. After halts of this type, a Start Flow instruction cannot be subsequently initiated for 300 milliseconds.

When MICR documents are read, the pulse sensed from each character is transferred to the Sorter-Reader's character recognition device for testing of density and validity of encoding. If the character is not recognized as one of the 14 valid symbols, a binary 15 is transferred to memory in place of the unrecognizable character. Then, at the conclusion of the read instruction, an automatic program branch is taken if an error character (the binary 15) is discovered in the core storage input area. A similar program branch will occur if the first character read is not the Amount symbol. Corrective routines will usually reject the faulty item and resume the document flow.

Document jams are detected in each of the two principal areas of the Sorter-Reader: the feed, align, and read areas; and the sorting area. If a jam is detected in the first area, the transport mechanism halts immediately, preventing the feeding of any additional documents. The documents traveling to their selected pockets will continue their course. Should a jam occur in the sorting area, the feeder is also halted immediately, but all items that have passed the read head will attempt to continue to their selected pockets.

When any pocket reaches 75% of its capacity (approximately 600 documents), a warning indicator above the pocket is illuminated. If the warning is ignored and the pocket becomes full, the feeding mechanism ceases operations and a full-pocket indicator is displayed on the control panel of the Sorter-Reader. Displays also indicate: the specific area in the Sorter-Reader where an item jam has occurred; the current mode of operation (on-line or off-line); the activation of the endorser; the inability to feed an item; and empty hopper conditions. Start, stop, and end-of-job controls are provided on the control panel, as well as along the length of the Sorter-Reader, to increase the operator's efficiency.

The Sorter-Reader can be operated off-line for general MICR document sorting. Field and digit selection for sorting is accomplished by push-buttons on the control panel, which function in conjunction with a plugboard. Override code detection is available to allow for two-way segregation of high-volume items. In addition, a zero-kill feature segregates items that need no further sorting because they contain non-significant zeroes in all fields that remain to be sorted. In the off-line mode of operation, all timing synchronization is controlled by the Sorter-Reader itself.

The various models of the Burroughs Sorter-Readers function in basically the same manner as described above. Individual differences in performance and configuration requirements are described in the paragraphs that follow.

.121 B 101 and B 102 Sorter-Readers

The B 101 Sorter-Reader operates in an off-line mode only, and can sort items into 13 pockets at a maximum speed of 1,560 documents per minute. The B 102 model has the ability to perform the same functions in an on-line mode as well. A standby station is provided to enable documents to be processed singly if desired. The B 102 is designed for operation with the B 251 (VRC) central processor.

.122 B 103 and B 104 Sorter-Readers

The B 103 Sorter-Reader is also capable of speeds up to 1,560 documents per minute over a 13-pocket selection area, but it adds the provision for an endorsing station instead of the standby station. As a result, the flow mode is the only possible mode of operation. The B 103 model is available with every B 100/200/300 Series Central Processor. A special Start-Stop Bar is optionally available with this model, providing the operator with immediate access to the controls along the entire extent of the pocket-select area. The B 104 is the same model as the B 103, except that no endorser can be attached.

.123 B 106 and B 107 Sorter-Readers

The Burroughs 13-pocket Sorter-Reader is offered with a slower peak rate of 1,200 documents per minute as the B 106 and B 107 models. Originally designed for use with the economy B 100 Series of central processors, the B 106 and B 107 are currently available for use with any level of central processor in B 100/200/300 Series. The B 106 Sorter-Reader is provided with an item standby station in place of the B 107's endorsing station.

.124 B 116 Sorter-Reader

The B 116 model represents an enlarged version of the Sorter-Readers listed above. Three more distribution pockets have been added, thereby reducing the number of passes required to complete many sorting operations. The 16-pocket Sorter-Reader also operates at a peak speed of 1,560 documents per minute while printing endorsements on the reverse side of every item. The 16th pocket has a capacity of 2,000 items, as compared with the standard 800-item capacity. When the number of documents in any pocket reaches a programmed tally point, an indicator can be lit above that pocket and the system halted. Special features include the full-length Start/Stop Bar and a power-driven transport area cover. The B 116 Sorter-Reader is designed for use with the B 300 Series Central Processor when a 16-Pocket Control Module is attached. It is also currently available with every level of central processor in the B 100/200/300 Series except the B 100 line; the 16-Pocket Control Module must be added to the central processor in every case.

INPUT-OUTPUT: DATA COMMUNICATIONS SYSTEM

.1 GENERAL

.11 Identity: . . . . B 450 Disk File and Data Communications Basic Control.
B 248 Data Communications Control Unit.
B 481 Teletype Terminal Unit.
B 483 Typewriter Terminal Unit.
B 493 Typewriter Inquiry Station.
B 484 Dial TWX Terminal.
B 486 Central Terminal.

.12 Description

The Burroughs B 450 Disk File and Data Communications Basic Control Unit houses the B 247 Disk File Control (Section 201:042) and the B 248 Data Communications Control. It is available for use with the B 200/300 Series 6-microsecond central processor only.

The B 248 Data Communications Control Unit provides the interface between the Central Processor and 1 to 15 terminal units which are capable of handling a variety of inquiry traffic requirements. Up to four B 248 Control Units can be attached to a system — one for every on-line central processor. The B 248 can be located up to 50 feet from the Processor, and is under control of the Processor only while loading or unloading a terminal unit buffer. The nominal data transfer rate between a terminal unit buffer and the Processor core storage is 30,000 characters per second.

The principal functions performed by the B 248 Data Communications Control are:

- Selection and connection of from 1 to 15 Teletype, Typewriter, Dial TWX, or Central Telephone Terminal units, in any combination.
- Determination of "ready" status of any of the attached terminal units within 20 microseconds.
- Generation of a Processor "interrupt" signal when a selected terminal unit is ready to supply input data or receive output data from the Processor.
- Translation between Burroughs Common Language (BCL) code and Baudot 5-level or ASCII 8-level code.

The B 481 Teletype Terminal Unit is a Teletype Model 28 Sequential Selector with selective calling features, which provides the interface between the B 248 and a network of teletype stations. The B 481 provides buffer storage and performs serial-to-parallel (input) and parallel-to-serial (output) conversions of the teletype character codes. From 1 to 399 teletype stations can be serviced by a single terminal unit, allowing a total of 5,985 teletype stations in the network if only teletype terminals are used. Each B 481 can service only one teletype station at a time. The B 481 has a buffer storage capacity of either 120 or 240 characters; access time is 20 microseconds. A character control device provides for the insertion and deletion of special teletype control characters and station disconnect signals. An optional Teletype Page Printer can be included as part of the B 481 Terminal Unit and used to monitor all messages on the network.

The B 483 Typewriter Terminal Unit provides facilities for connecting from 1 to 8 Typewriter Inquiry Stations to the communications system. The unit contains an input buffer which is capable of storing simultaneous inputs of 60 characters from each of 8 inquiry stations. An input scanning device accepts data as it becomes available (a character at a time) from any of the 8 stations, and directs it to the proper portion of the buffer. An interrupt and latch facility holds the input buffer to a station while data is transferred through the B 248 Data Communications Control to the Central Processor.

The input buffer is also utilized as an output buffer, and stores reply messages from the Processor under control of timing signals generated in the terminal unit. Output buffer readout to the Typewriter Inquiry Station is also under control of the terminal unit.

The B 493 Typewriter Inquiry Station utilizes a Teletype Send-Receive Paper Printer set. It communicates with the B 483 Terminal Unit via a multiple-conductor cable which can be up to 1 mile long, and it can be used for input and output of alphameric data at up to 10 characters per second.

The B 484 Dial TWX Terminal Unit provides the facilities required to use stations of the Dial TWX network as inquiry and transmission devices. The B 484 unit contains 480 positions of input-output buffering that can accept messages from up to eight stations of the Dial TWX network simultaneously. The buffer size can be segmented into groups of 60, 120, 240, or 480 positions, depending on the number of channels to be utilized — 8, 4, 2, or 1. A Model 103A Data-Phone subset must be used as an interface between each channel and the TWX network. Normal telephone dialing procedures are followed in establishing contact between one of

.12 Description (Contd.)

the eight channels and each Terminal Unit. If it is not desired to provide each channel with its own number, a sequential calling device is available from the telephone company. This device connects the caller to the next available input-output channel, rather than directing him to a specific path. With this arrangement, the caller will receive a busy signal only if all of the buffered channels are unavailable.

After a connection between a TWX station and the B 484 Terminal Unit has been established, the operator types an input message on the Dial TWX station keyboard, using a Model 33 or 35 Teletypewriter unit. The message is transmitted and loaded into the Terminal Unit's buffer as it is keyed in. After the message has been processed, the Terminal Unit sends the central processor's response to the awaiting channel. Until the station has received the "disconnect code," it can continue to communicate with the processing center. The B 484 Terminal Unit can accept messages larger than the buffer size established for each channel, but only one such message can be accepted at any one time. All input-output messages controlled by the Dial TWX Terminal Unit can be monitored by connecting a B 493 Typewriter Inquiry Station to the Terminal Unit. When the monitor station is disconnected, the typewriter can be used in its normal manner.

The B 486 Central Terminal Unit serves as an interface between the central processor and up to 96 Burroughs On-line Teller Consoles. Each branch of a bank can communicate with the main office through its Teller Consoles and normal telephone lines. Up to eight Teller Consoles can be controlled by a Remote Terminal Unit. The Remote Terminal Unit in each office monitors the input-output status of all local Teller Consoles, converts and checks information being transmitted to and from the processing center, and initiates all message and reply transmission. A Model 202D Data-Phone subset is required in each office for every Remote Terminal Unit used, to convert that unit's signals into a form acceptable for telephone-line transmission. A central office bridge, available from the telephone company, can connect up to nine lines from several different offices into one transmission channel in order to maximize the use of the six communication channels available in each Central Terminal Unit.

The Central Terminal Unit at the processing center controls six communications input-output channels. Each channel can control up to 16 Teller Consoles, providing a maximum of 96 Consoles for each Central Terminal Unit. If the input messages have been sent via Data-Phone subsets, they must be reconverted to signals acceptable to the Central Terminal Unit by Data-Phone subsets at the processing center. The Central Terminal Unit accepts and stores messages until the central processor is ready to process them. Replies can be sent back to the originating Teller Console through the Central Terminal Unit according to a channel-queueing discipline established by the B 248 Data Communications Control Unit.

Burroughs estimates that the average transaction time for its On-line Teller System is 8 seconds. To achieve and maintain that rate requires that no more than 1,000 transactions per channel, or 62 per Teller Console, be processed every hour.

The B 200/300 Operating System I has been announced for use with the On-line Teller System. Program library calls and operator interrupts can be controlled by the Operating System, but no provisions have been included for the automatic control of all input-output demands on the central processor.

First delivery of Burroughs data communications equipment occurred in November, 1964. The On-line Teller System was first installed during the second quarter of 1965.

SIMULTANEOUS OPERATIONS

Buffer storage facilities are the same for each of the B 100/200/300 Series Systems. These facilities include two input buffers and one output buffer in the central processor, as well as local buffers in the printer, tape lister, and data communications terminal units. The assignment of the processor buffers is as follows:

- Input Buffer 1 — card reader or paper tape reader.
- Input Buffer 2 — card reader, paper tape reader or MICR sorter-reader.
- Output Buffer — card punch or paper tape punch.

The use of the various buffers permits several input-output operations to take place simultaneously while internal processing proceeds unhindered (except during the short periods required to load and unload the buffers). For example, as many as nine input-output units can be operating during computation (two card readers, one card punch, three tape listers, and up to three data communications devices).

The maximum number of peripheral units that can be connected to each of the central processors is listed on Page 201:031.011. Two line printers can be used (with all but the VRC System) if a special dual-printer module is added to one of the printers. Two tape listers can be used as alternatives to the line printers, but a combination of one printer and one lister is not allowed. Both printing and paper advance operations can occur on the line printer(s) or tape lister(s), in parallel with other operations.

The B 401 Record Processor is used only in the VRC System, and its data transfer operations are not buffered. However, forms and ledger card movements can occur independently. In a similar manner, magnetic tape read and write operations cannot occur in parallel with any other operation, but up to six simultaneous tape rewind operations are permitted.

Disk File read and write operations are not overlapped, so the processor is locked out for an average of 20 milliseconds rotational delay plus the full data transfer time (at 100,000 characters per second) for each read or write instruction. The processor can, however, be released during programmed read-backs to check for Disk File recording errors.

Multiple data communications operations can occur in parallel with other operations because of buffer facilities in the following units:

- B 481 Teletype Terminal Unit — one buffer of 120 or 240 characters capacity.
- B 483 Typewriter Terminal Unit — eight 60-character input-output buffers.
- B 484 Dial TWX Terminal Unit — eight 60-character input-output buffers.
- B 486 Central Terminal Unit — twelve 86-character input-output buffers.

To summarize, the following operations are mutually exclusive; i.e., only one operation from this group can be performed at a time:

- Internal processing.
- Magnetic tape reading or writing.
- Disk File reading, writing, or rotational delay.
- B 401 Record Processor data transfer operations.

INSTRUCTION LIST

These instructions are common to all B 100/200/300 Series systems.

INSTRUCTION						OPERATION
Op.	M	N	A	B	C	
						Arithmetic
1	M	N	A	B	C	A + B → C, B, or A. M, N specify length of operands.
2	M	N	A	B	C	A - B → C, B, or A. M, N specify length of operands.
3	M	N	A	B	C	A x B → C. M, N specify length of operands.
4	M	N	A	B	C	A ÷ B → C. M, N specify length of operands.
						Logic
5	0	N	A	B	C	Compare A to B alphameric, branch to C if equal. N specifies field length.
5	1	N	A	B	C	Compare A to B, zone bits only, branch to C if equal. N specifies field length.
5	2	N	A	B	C	Compare A to B, numeric, branch to C if equal. N specifies field length.
5	4	N	A	B	C	Compare A to B alphameric, branch to C if unequal. N specifies field length.
5	5	N	A	B	C	Compare A to B, zone bits only, branch to C if unequal. N specifies field length.
5	6	N	A	B	C	Compare A to B, numeric, branch to C if unequal. N specifies field length.
6	0		A	B	C	Jump to A, B, or C depending on low, equal, or high comparison indicators.
6	1		A			Jump to A.
b						No operation; proceed to next instruction in sequence.
9	M	N				Halt after all operations in progress have been executed. Opcode, M, N displayed on console.
						Data Transfer
7	M	N	A		C	Transfer M fields, N char starting at A to C.
8	M	N	A	B	C	Transfer M char starting at A to C thru mask starting at B.
						Input-Output; Punch Cards
#		N		B	C	Transfer contents of card buffer specified by N to storage starting at C and read 1 card to buffer or go to B if End of File.
@			A			Transfer 80 char from storage starting at A to punch buffer and punch 1 card.
						Input-Output; Printer and Lister
A	M	N	A	B		Transfer 120 char to print buffer for printer (or 44 char for lister) starting at A. Print 1 line with spacing specified by M or skipping specified by N. For lister, M specifies lister and N specifies tape number. B specifies branch address if end of page (printer) or out of paper (lister).
B	M	N		B		Space or skip without printing on printer or lister, specified by M and N. B specifies branch address if end of page (printer) or out of paper (lister).
						Input-Output; Sorter-Reader
#		4	A	B	C	Transfer all fields from Sorter-Reader document to core storage starting at C, in flow mode. A, B are branch addresses.

INSTRUCTION						OPERATION
Op.	M	N	A	B	C	
#		5	A	B	C	Transfer char thru transit field only from Sorter-Reader document to core storage at C, in flow mode. A, B are branch addresses.
#		6	A	B		Transfer all fields from Sorter-Reader document to buffer, in flow mode. A, B are branch addresses.
C	0	N				Pocket select in Sorter-Reader. Pocket set by N.
C	2	N				Demand feed and pocket select in Sorter-Reader. Pocket set by N.
C	4	N				Stop flow mode in Sorter-Reader; select pocket set by N.
C	6	N				Start flow mode in Sorter-Reader; select pocket set by N.
C	8					Increase batch counter by 1 (B 103 and B 116 only).
C	7	N				Start buffered flow and pocket select. Pocket set by N.
						Input-Output; Magnetic Tape
D	1	N	A	B	C	Read one block forward on unit N to storage starting at C. A, B are branch addresses.
D	2	N	A	B	C	Write one block on unit N from storage starting at A. B, C are branch addresses.
D	3	N	A	B		Erase one block on unit N from storage starting at A. B is branch address.
D	4	N				Backspace one block on unit N.
D	5	N				Rewind unit N.

.2 These instructions, and instruction modifications, are common to all systems except VRC.

INSTRUCTION						OPERATION
Op.	M	N	A	B	C	
						Input-Output; Paper Tape
E	M		A	B	C	Transfer 80 characters from storage starting at A to output buffer and punch paper tape. B, C are branch addresses. Punching instructions are indicated by M.
F	M	N	A	B	C	Transfer characters (buffered or unbuffered) from paper tape unit N into C. A, B, are branch addresses. M indicates buffered or not.
F	4	N		B		Space paper tape forward on unit N to next control code. B is branch on End-of-Tape address.
F	&	N			C	Space paper tape backward on unit N to next control code. C is branch on Beginning-of-Tape address.
F	8	N		B	C	Rewind paper tape on unit N. B, C are branch addresses.
						Address Modification
J			A	B		Modify one 3-character address, specified by B, by the quantity stored in A.
						Data Transfer
P	M	N	A		C	Transfer zone bits of characters from A to C. M selects number of words; N selects number of characters.
						Logic
9	M	N	A			Halt after all operations in progress have been executed. Opcode, M, N, and A are displayed on console. If the 2 bit of the M variant is on, a branch to the address specified by A occurs after the system is restarted. B 103 or B 116 Sorter-Reader pocket indicators are lit as specified by N.

(Contd.)

.3 These instructions pertain only to the VRC System.

INSTRUCTION						OPERATION			
Op.	M	N	A	B	C				
						Input-Output; Record Processor			
G	M	N			C	Select hopper and read magnetic stripe on record into core storage starting at C. N selects feed or feed and read where applicable.			
						M operation	N function	A	B
	1	N	A	B	C	primary feed	as above	branch address	stripe read control
	2	N	A	B	C	manual feed	as above	branch address	stripe read control
	3	N	A	B	C	auxiliary feed	as above	branch address	stripe read control
	4				C	optical reader	N/A	N/A	N/A
	5	N			C	R. P. keyboard	select lamp	N/A	N/A
G	8	0	A		C	Eject record to primary stacker, write on stripe from storage starting at A. C is branch address.			
G	9	1				Eject record to auxiliary stacker without writing.			
H	0	N	A	B	C	Print and single space on record and/or forms from storage, starting at A. Spacing controlled by N as shown below. B, C are branch addresses.			
H	1	N	A	B	C	Print and single space on forms only from storage, starting at A. Spacing controlled by N as shown below. B, C are branch addresses.			
						N	Spacing		
						0	Spacing suppressed.		
						1	Form A only.		
						2	Form B only.		
						3	Forms A and B.		
						4	Record only.		
						5	Form A and record.		
						6	Form B and record.		
						7	Forms A and B and record.		
I	1					Restore Forms A and B.			
I	2	N		B		Single-space record and/or forms without printing. B is branch address. Spacing controlled by N as in table below.			
						N	Spacing		
						0	Spacing suppressed.		
						1	Form A only.		
						2	Form B only.		
						3	Forms A and B.		
						4	Record only.		
						5	Form A and record.		
						6	Form B and record.		
						7	Forms A and B and record.		
I	4		A			Align record to line specified by information in core storage starting at A.			

.4 These instructions, and instruction modifications, are available in the B 200/300 Series 6-microsecond central processor.

INSTRUCTION						OPERATION
Op.	M	N	A	B	C	
						Date Transfer
8	M	N	A	B	C	Transfer M characters starting at A to C, thru mask starting at B. N = 0: standard mask (fiscal). N = 1: inverted mask (fiscal). N = 2: alphameric mask.
						Input-Output; Punched Cards
#	M	N		B	C	Transfer contents of card buffer specified by N to storage starting at C and read 1 card to buffer, or go to B if End-of-File. M = halt or branch on Not Ready condition.
@	M		A			Transfer 80 characters from storage starting at A to punch buffer and punch 1 card. M = BCL, Bull, or ICT code designation.
						Input-Output; Lister
A	M	N	A	B	C	Transfer 44 char to buffer from memory starting at A. Print 1 line on lister specified by M and tape specified by N. B specifies branch address on out-of-paper. C specifies a print-error branch.
						Input-Output; Supervisory Printer
Q	1		A			Print on supervisory printer starting at A. Continue until group mark is encountered.
Q	2			B	C	Read from supervisory printer into storage locations starting at C. B is branch address upon end of input message.
						Input-Output; Magnetic Tape
D	8	N	A	B	C	Write one record on unit N starting at A and continuing to end of storage. B and C are branch addresses.
D	9	N	A	B	C	Read one binary record on unit N into storage beginning at C. A and B are branch addresses.
D	10	N	A	B	C	Write one binary record on unit N starting at A and continuing to end of storage. B and C are branch addresses.
						Input-Output; Disk File
K	O	N	A	B	C	Write N segments on disk file starting at A from processor storage locations starting at B. C is branch on "Not Ready" address.
K	2	N	A	B	C	Read N segments from disk file starting at A into storage starting at B. C is branch on "Not Ready" address.
K	4	N	A		C	Transfer the addressing word at A to disk file control, release the central processor, and read N segments for read errors.
K	8		A	B	C	Interrogate disk file and branch on "Busy," error, "Write Lockout," or invalid address.
						Input-Output; Data Communications
L	1	N	A	B	C	Interrogate inquiry ready on unit N. A, C, are branch addresses. B is store address on terminal unit.
L	2	N		B	C	Transfer contents of terminal unit N buffer to processor storage starting at C. B is branch address.
L	4	N	A	B		Transfer to terminal unit N buffer data from processor storage starting at A. B is branch address.

(Contd.)

.5 These instructions, except those marked with asterisks, are available in the B 300 Series central processors only. Asterisks denote those instructions that can also be obtained on the B 200 Series 6-microsecond central processor through field or factory modifications.

	INSTRUCTION						OPERATION
	Op.	M	N	A	B	C	
							Input-Output; Punch Cards
	#	M	N	A	B	C	Transfer contents of card buffer specified by N to storage starting at C, and one card to buffer if M is 0 or 1. Go to B if End-of-File, and go to A if reader is busy or not ready when M is 1. A 2 in M reads the binary card image into storage starting at A.
	U		N	A			Transfer 160 characters from storage starting at A and punch the binary image in one card.
*	@	M	N	A			Transfer 80 characters from storage starting at A to punch buffer and punch one card. M designates punching in BCL, BULL, or ICT code. N determines stacker selection with B 304.
							Input-Output; Lister
	A	M	N	A	B	C	Transfer 44 characters to buffer from memory starting at A. Print chars 1-22 on master lister and tape designated by M; print chars 23-44 on lister and tape designated by N. B specifies branch address on out-of-paper. C specifies a print-error branch.
	B	M	N		B		Space, skip, or slew master lister, as specified by M, and any designated non-master lister and tape as specified by N.
							Input-Output; Sorter-Reader
*	C	M	N				Pocket select in sorter. Pockets 1-16 are selected by N. M determines starting, stopping, or maintaining demand or flow mode of sorter operation.
							Data Transfer
	R	M	N	A		C	Transfer M fields and N characters from storage starting at A, translate the characters to any 6- or 12-bit code, and store the result starting at C.
*	7	M	N	A	B	C	Transfer M fields and N characters from memory starting at A to memory starting at C, and go to location specified by B if a "B" bit is over M.
*	P	M	N	A	B	C	Transfer zone bits of characters from memory starting at A to memory starting at C, and go to location specified by B if a "B" bit is over M. M and N specify the size of the transfer.
	M			A	B	C	Compress a field of numeric data starting at the memory location specified by A and store the packed data starting at the address specified by C. The size of the field to be compressed is expressed by B.
	N			A	B	C	Expand a field of numeric data compressed in storage beginning at the address specified by A and store the expanded digits starting at the address specified by C. The size of the expanded record is specified by B.
							Unit Interrogate
	T	M	N	A	B	C	Interrogate the input-output unit designated by M and N, and go to memory location specified by A, B, or C if the unit is busy, not ready, or in an error state, respectively.

CODING FORMS: ASSEMBLY LANGUAGES

.1 BASIC ASSEMBLY LANGUAGE (B 100/200/300 Series Systems)

Op	M	N	A ADDRESS	B ADDRESS	C ADDRESS	PAGE	REF	CONSTANTS	REMARKS		LINE	*
0	1	2	3	6	9							
			PG R I	PG R I	PG R I			SIZE 0 1 2 3 4 5 6 7 8 9 T E				
7 8 9	10 11	12 13	14 15 16 17	18 19 20 21	22 23 24 25	26 27	28	29 30 31 32 33 34 35 36 37 38 39 40 41 42 43	44 50 56 62 68 71	74	78 79 80	
											0 1	A
											0 2	B
											0 3	C
											0 4	D
											0 5	E
											0 6	F
											0 7	G
											0 8	H
											0 9	J
											1 0	K
											1 1	L
											1 2	M

.2 ADVANCED ASSEMBLY LANGUAGE (B 200/300 Series Systems)

LINE NO.	I	SYMBOLIC LABEL	OP CODE	VARIANT M	VARIANT N	A ADDRESS TAG	±	ENT.	CHAR.	B ADDRESS TAG	±	ENT.	CHAR.	C ADDRESS TAG	±	ENT.	CHAR.	REMARKS
4 5	6	7 8 9 10 11 12	13 14 15 16	17 18	19 20	21 22 23 24 25 26	27	28 29	30 31 32	33 34 35 36 37 38	39	40 41	42 43 44	45 46 47 48 49 50	51	52 53	54 55 56	57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
0 1																		
0 2																		
0 3																		
0 4																		
0 5																		
0 6																		
0 7																		
0 8																		
0 9																		
1 0																		
1 1																		
1 2																		

DATA CODE: INTERNAL, PRINTER, LISTER, SORTER-READER, DISK FILE

.1 USE OF CODE: . . . . Internal, Printer, Lister, Sorter Reader, Disk File.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits + odd parity bit.

.22 Character Structure

.221 More significant pattern: . . . . 2 bits; 16, 32.

.222 Less significant pattern: . . . . 4 bits; 1, 2, 4, 8.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	0	+[2] 0	-[3] 0	BLANK
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
10	#[4]	.	$	,
11	@[5]	[	*	%
12	?	&	-	≠
13	:[6]	(	)	=
14	>[7]	<	;	]
15	≥	‡[1]	≤	"

Notes:
1. Group mark in storage; printed as ←.
2. Printed as +.
3. Printed as x.
4. Code for MICR amount symbol.
5. Code for MICR transit number symbol.
6. Code for MICR on us symbol.
7. Code for MICR dash symbol.

DATA CODE: ALPHAMERIC CARD

.1 USE OF CODE: . . . . . Alphameric Card Code.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 1 column.

.23 Character Codes

UNDERPUNCH	OVERPUNCH			
	None	12	11	0
None		&	-	
12				
11				
0	O	+	x	
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
8-2				≠
8-3	#	.	$	,
8-4	@	[	*	%
8-5	:	(	)	=
8-6	>	<	;	]
8-7	≥	←	≤	"

DATA CODE: MAGNETIC TAPE

.1 USE OF CODE: . . . . . Magnetic Tape.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 6 bits + even parity bit.

.22 Character Structure

.221 More significant pattern: . . . . 2 bits; 16, 32.

.222 Less significant pattern: . . . . 4 bits; 1, 2, 4, 8.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	?	Blank	-	&
1	1	/	J	A
2	2	S	K	B
3	3	T	L	C
4	4	U	M	D
5	5	V	N	E
6	6	W	O	F
7	7	X	P	G
8	8	Y	Q	H
9	9	Z	R	I
10	0	≠	CR	+
11	#	,	$	.
12	@	%	*	[
13	:	=	)	(
14	>	]	;	<
15	‡[1]	"	≤	Note 2

Notes: 1. Tape mark.
2. Group mark in core storage.

DATA CODE: RECORD PROCESSOR

.1 USE OF CODE: . . . . . B 401 Record Processor.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 4 bits + even parity bit.

.22 Character Structure

.221 More significant pattern: . . . . none.

.222 Less significant pattern: . . . . 4 bits; 1, 2, 4, 8.

.23 Character Codes

PATTERN	SYMBOL
0	0
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	.
11	)

DATA CODE: PAPER TAPE

.1 USE OF CODE: . . . . . B 141 Paper Tape Reader and B 341 Paper Tape Punch.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 6 data tracks + 1 odd parity track + 1 track for end-of-line symbol.

.22 Character Structure

.221 More significant pattern: . . . . 2 zone bits; X = 32, 0 = 16.

.222 Less significant pattern: . . . . 4 numeric bits; 8, 4, 2, 1.

.23 Character Codes

Less Significant Pattern	More Significant Pattern			
	0	16	32	48
0	BLANK	0	–	&
1	1	/	J	A
2	2	S	K	B
3	3	T	L	C
4	4	U	M	D
5	5	V	N	E
6	6	W	O	F
7	7	X	P	G
8	8	Y	Q	H
9	9	Z	R	I
10	:	≠	x[2]	+
11	#	,	$	.
12	@	%	*	[
13	?[3]	=	)	(
14	>	]	;	<
15	≥	"	≤	Note 1

Notes:
1. Tape feed code.
2. Multiplication sign.
3. Invalid code (as punched).

DATA CODE: COLLATING SEQUENCE

.1 USE OF CODE . . . . internal collating sequence.

.2 STRUCTURE OF CODE

In ascending sequence:

blank
.
[
(
<
ǂ (group mark)
&
$
*
)
;
≤
-
/
,
%
=
]
"
#
@
:
>
≥, ≣ (tape mark)
+0
A
B
C
D
E
F
G
H
I
-0
J
K
L
M
N
O
P
Q
R
/
S
T
U
V
W
X
Y
Z
0
1
2
3
4
5
6
7
8
9
? (invalid code)

PROBLEM ORIENTED FACILITIES

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . none.

.12 Simulation by Other Computers

By Burroughs B 220

Reference: . . . . Burroughs Corporation.
Date available: . . . . . January, 1961.
Description:

A general computer simulation of the B 200 Series equipment, including the Multiple Tape Listers, Sorter-Readers, and Record Processor, by using combinations of B 220 printers and magnetic tapes. Designed primarily to enable early B 200 Series users to test their programs on the earlier B 220 system, this simulator is no longer in use.

.13 Data Sorting and Merging

Sort Generator I

Reference: . . . . URS-035.
Record size: . . . . 600 characters max.
Block size: . . . . 800 character max.
Key size: . . . . 23 characters max.
File size: . . . . one reel.
Number of tapes: . . . . 3 to 6.
Date available: . . . . . May, 1963.
Description:

Auto-load routines for magnetic tape sorting are produced and are claimed to be about 95% efficient. The generator can be run on either a card or tape system. It is a one-pass generator, and less than 5 minutes are required to generate a sort program. Operating instructions and complete documentation are printed, and a Restart Program is produced.

Generalized Three-Tape Sort

Reference: . . . . URS-043.
Record size: . . . . 1,200 characters max.
Block size: . . . . 1,200 characters max.
Key size: . . . . 47 characters max.
File size: . . . . one reel.
Number of tapes: . . . . three.
Date available: . . . . . April, 1964.
Description:

Two specification cards containing the input-output parameters and sorting requirements are loaded with the object sort program. After about one minute of initialization operation, during which the best sorting techniques for the tape block length are selected, the multi-phase sort begins. Specification card editing is provided, but no provision is included for restarts once the actual sort has begun. With this program it is possible to sort 20,000 80-character records with a sort key of 20 characters, blocked 10 records in and 14 out, using three 50KC tape units, within 34 minutes. In order to use this program, a B 200/300 6-microsecond central processor with 9,600 characters of core storage is required, in addition to three magnetic tape units and a line printer (any models).

Disk File Sort Generator III

Reference: . . . . URS-053.
Record size: . . . . 1,200 characters max.
Block size: . . . . 1,920 characters max.
Key size: . . . . 60 characters max.
File size: . . . . dependent on number of Disk File modules available.
Input form: . . . . magnetic tape or Disk File.
Output form: . . . . magnetic tape or Disk File.
Date available: . . . . . January, 1965.
Description:

Sort Generator III is designed to produce auto-load object sort programs that utilize a Burroughs Disk File for intermediate storage. Generation requires about six minutes and can be performed on a B 200/300 central processor with either 4,800 or 9,600 characters of core storage. In addition, at least one module of Disk File storage (9.6 million characters) is required. The generated object program accepts records from either magnetic tape or Disk File and sorts them in about half the time required for tape sorts, according to the manufacturer.

Two types of sort programs can be generated: record sorts or tag sorts. Tag sorting eliminates the need to process the entire data record during each sort phase by generating a short control record that corresponds to each data record, and then sorting the control records. During the final phase of the sort operation, the full records are drawn in sequence from input area storage and written on tape or another area in the Disk File. One module of Disk File storage provides enough intermediate storage to sort up to 84,000 80-character records.

Disk File Chained Records Sort

Reference: . . . . URS-048.
Date available: . . . . . January, 1965.
Description:

The Chained Records Sort program is designed to relocate Disk File records within a chain based on the activity of each record. At the conclusion of the sort, the Home location of each chain of records will contain the most active record; successive records in the chain will be arranged in the order of descending activity. Processing chained records arranged according to degree of activity will reduce the number of accesses required to find each record.

.13 Data Sorting and Merging (Contd.)

The Chained Records Sort program sorts each chain of records within either 4,800 or 9,600 characters of B 200/300 core storage. Magnetic tape units are not required. The user must insert his own randomizing formula into the program in order to direct the discovery of successive Home addresses prior to each chain sort.

.14 Report Writing

Revised Report Generator I

Reference: . . . . URS-022, Tech. Bulletin 170R.
Date available: . . . . . April, 1962.
Description:

This routine generates specially-tailored object programs that process input data from either punched cards or magnetic tape to produce reports on either punched cards or the on-line printer. The only required peripheral devices are a card reader, card punch, and printer; an optional magnetic tape version, however, reduces report program generation time to about 2.5 minutes. An 80-card auto-load object program deck is produced by the one-pass generator. Facilities are provided for controlling the printed format, for simulating listing and tabulation of up to seven running totals, and for maintaining up to four levels of totals. Each report produced by a generated object program includes a printed description of itself.

Report Generator IA performs functions similar to those of Report Generator I, except that the generated program is produced in symbolic assembly language in order to facilitate any necessary program patching. An additional pass for assembly is therefore required in order to produce the machine-language object program.

.15 Data Transcription

Data Conversion Program

Reference: . . . . URS-027.
Date available: . . . . . March, 1963.
Description:

This program allows data to be converted, in image form, from one medium to another. Conversions which can be performed include card, paper tape, or magnetic tape input to any combination of card, paper tape, printer, and/or magnetic tape output. Any one of 45 possible conversion operations may be selected.

Disk File Utility Programs

Reference: . . . . URS-047.
Date available: . . . . . January, 1965.
Description:

The following programs are provided:

- Reset Disk File — clears and resets specified areas to any preselected character.
- Card-to-Disk — writes the contents of punched cards onto specified areas of the Disk File, using indirect addressing.
- Disk-to-Card — punches the contents of specified areas of the Disk File.
- Tape-to-Disk — writes the contents of magnetic tape records onto specified areas of the Disk File. Direct addressing is used.
- Disk-to-Tape — writes the contents of specified areas of the Disk File onto magnetic tape.
- Disk-to-Printer – prints the contents of specified areas of disk storage.
- Disk-to-Disk — transfers information from one section of Disk File storage to another.

.16 File Maintenance

Magnetic Tape Copy/Verify

Reference: . . . . URS-031.
Date available: . . . . . January, 1963.
Description:

The Magnetic Tape Copy/Verify Program provides a means of reproducing and/or verifying magnetic tape files. Reproduction is performed on a record image basis. Up to five control totals can be accumulated for each file being copied, in addition to a record count. The program will process either multiple-reel files or multiple-file reels. In the case of multiple-file reels, the files to be processed are selected by the user. Magnetic tape files can also be processed for establishing or verifying control totals without copying.

Disk File Record Maintenance System

Reference: . . . . URS-049.
Date available: . . . . . February, 1965.
Description:

Three routines are provided for Disk File maintenance:

- Record Load Routine — loads records onto the Disk File from punched cards.
- Record Change Routine — changes selected portions of specified records. Input must be punched card, and random addressing is used.
- Delete Record Routine — provides for deleting a specified record from the Disk File. Direct addressing is used.

(Contd.)

.17 Other

Library of Demand Deposit Accounting Programs

Reference: . . . . FAS-001 through -13.
Date available: . . . . . October, 1962.
Description:

This is a library of standard financial programs to assist in the preparation and installation of the Visible Record Computer (VRC) System. These programs are based on the MICR concept and direct item input. They are:

FAS-002; MICR Conversion: . . . . prepares customer ledger cards from magnetic ink characters encoded on documents prepared by the Burroughs P 703 Amount and Account Number Printer.

FAS-003; Preliminary Proof: . . . . performs the first sort and proving pass for documents that affect the demand deposit ledger.

FAS-004; Secondary Proof: . . . . further proves all demand deposit documents and sorts them by ledger control.

FAS-005; Sequence Check and Stop Pay Control: . . . . assures that documents have been sorted according to ascending account number (and stated sequence).

FAS-006; Daily Account Updating: . . . . posts the daily activity to the demand deposit ledger (may be last program used).

FAS-007; Daily Reversal and Correction: . . . .
a) Daily reversal and correction — posts documents on a daily basis;
b) File maintenance — used on a weekly basis to adjust stored data on ledger card magnetic strips.

FAS-008; Balance Transfer and Analysis: . . . . processes the customer ledger cards for the last time during the accounting period.

FAS-009; Balance Transfer and Analysis Correction: . . . . selectively processes customer ledger cards not processed in the preceding program.

FAS-010; Analysis History: . . . . provides hard copy record of analysis data.

FAS-011; Management Report: . . . . . .
a) New and Closed Accounts — Significant Balance Changes — Large Transactions Report — use documents and ledger cards as input.
b) Daily Consolidated Control Report - uses ledger proof cards to obtain daily settlement figures.
c) Monthly Consolidated Income Report — run after Balance Transfer to provide analysis data in report form.

FAS-012; Trial Balance: . . . . provides a listing by account balance and number of all ledger cards in the ledger control.

FAS-013; Ledger Card Preparation: . . uses punched cards which are punched directly from formats of the ledger cards to be prepared.

Demand Deposit/Proof and Transit Financial Application Package

Reference: . . . . Technical Bulletin 200-22017.
Date available: . . . . . August, 1964.
Description:

The Financial Application Package provides a set of 23 programs designed to process MICR documents and their associated records from the proof and distribution of all items entering a banking institution to the updating of customer accounts. The package includes full documentation for each program. The programs are written in the Basic Assembly Language, and are designed for use with any B 100/200/300 Series tape-oriented central processor and 4 magnetic tape units of any model. A MICR sorter-reader, card reader, and line printer (any available models) are also required. The package includes the following programs:

Counter Proof: . . . . . converts all deposit information to magnetic tape; segregates outgoing transit work; develops cash-in and cash-out totals for up to 15 branches or tellers.

Transit: . . . . lists, segregates, and totals outgoing transit work.

Preliminary Proof: . . proves, lists, and totals all checks drawn on the bank; writes all valid items onto magnetic tape.

.17 Other (Contd.)

Credit Tape Sort; Debit Tape Sort: . . . . sort the credit item magnetic tape created in Counter Proof and the debit item tape created in Preliminary Proof.

Correct Credit Tape: . performs a preliminary file maintenance on the sorted credit item tape.

Daily Transaction Merge:. . . . . merges the sorted credit and debit tapes; develops control totals for audit trail purposes.

Transaction Journal: . produces a printed listing of all items on the merged input tape; balances to control totals; lists separately any large transactions.

Stop Pay/List Post: . . lists any items that have possible stop payment orders against them; produces a list of individual items to be posted to high activity accounts.

Update: . . . . posts items from transaction tape to proper accounts on the tape master file; prints a complete trial balance report.

Reversal and Correction: . . . . corrects the master account file if necessary; reverses payment of items that are to be returned.

Service Charge Analysis: . . . . analyzes each type of account according to service charge rules; produces a tape to serve as an input to preparation of customers' statements.

Merge Month-to-Date Transaction Tape: . . merges items on daily transaction tape with month-to-date items; writes all transactions for a cycled group of accounts on tape for monthly statement printing.

Statement Preparation: prepares completely addressed customer statements with service charges applied.

Report Programs — Daily Referral Journal; New and Closed Accounts; Significant Balance Changes; Overdrafts; Unposted Transactions: . . . . produce 5 management reports from an exception item/account tape developed as an output to Update.

File Maintenance Programs — Name and Address; Master File:. . . . . . provide capability of keeping both magnetic tape files up to date.

Conversion Programs — Name and Address File; Master File: . . . . . . convert account and name/address information from punched cards to magnetic tape for use in this programming system.

Installment Loan Financial Application Package

Reference: . . . . FAS-015 Application Bulletin.
Date available: . . . . . May, 1965.
Description:

The Installment Loan Package provides 9 documented programs that process loan payments through a MICR sorter-reader and apply them to the master file on magnetic tape. The package requires four magnetic tape units, a line printer, and any B 100/200/300 Series central processor, in addition to the sorter-reader. The programs included in the package are listed as follows:

Preliminary Proof: . . converts information from MICR loan payments to magnetic tape; separates items by type of account; prints a transaction journal with control totals.

Daily File Maintenance:accepts any new loan accounts; processes all changes to loan master file on magnetic tape.

Update: . . . . processes daily transaction tape and master file tape, applying all loan payments; prints a Daily Reference Journal; prepares an exception item/account output tape.

Exception Report: . . . produces daily printed reports of zero balances, unposted payments, and payments over 15 days delinquent; other-than-daily reports include delinquent loans, new loans exceeding $5,000, weekly dealers' and weekly past due reports.

Dealer Earnings or Employee Loan Report: . . . . lists all bank employee loans and their status; lists the four high-volume dealers and shows earnings of each.

Loan Classification or Dealer Loan Report:. lists all loans according to 10 classifications, showing totals and delinquencies; categorizes loans by dealer, showing totals and delinquencies.

(Contd.)

.17 Other (Contd.)

Customer Interest
Report: . . . . prepares a form for each customer indicating his yearly loan interest paid for tax purposes.
Loan History Report: . provides a monthly picture of the loan's history, including accrual information.
Loan Conversion:. . . . converts initial loan account information on punched cards to magnetic tape; develops conversion totals for balancing.

Management Science Series

Reference: . . . . MSS-044, MSS-005, and MSS-006.
Date available: . . . . . January, 1965.
Descriptions:

Loan Payment Schedular Program —

The Loan Payment Schedular Program develops a month-by-month schedule for any monthly-payment loan, showing the portions of each payment that are applied to interest and principal. The term of payment or the payment itself can be fixed: the program calculates whichever quantity is not specified. The Loan Payment Schedular Program functions with any B 200/300 6-microsecond central processor and any model card reader and line printer.

Bank Customer Service Model —

This 3-phase program simulates the interaction between banking customers and specified facilities of the bank. Banking equipment configurations, both on-line and off-line, and tellers' schedules can be evaluated in terms of total customer service offered. By means of this program, proposed operations changes can be evaluated with respect to resulting customer service before any changes are actually put into effect.

The user of this program must provide as input the total number of customers expected for the day, the number and length of the periods in the day, and the distribution of the various customer transaction types. The user must also specify the number of tellers' windows available and the amount of time a typical customer demands in order to be completely serviced.

The printed output shows simulated customers' movements through the bank, indicates waiting times and processing times, and lists the number of various types of customers serviced and the cumulative time for each type. In addition to the line printer required to produce this report, the computer system configuration required to run the program includes any B 100/200/300 Series tape-oriented central processor, two magnetic tape units, and a card reader (any model).

Bond Analysis and Accounting Program Package —

The Bond Accounting Package provides four programs capable of analyzing a bond portfolio file on punched cards and producing reports designed to assist the portfolio management in the evaluation of proposed and existing bond earnings. Program 1 projects the cash flow of future interest and maturity payments resulting from an existing bond portfolio. Program 2 calculates the effective rate of interest for bonds being considered for purchase. Amortization schedules for premiums or discounts of purchased bonds are developed by Program 3. The final program in the package computes various accounting entries for user-specified accounting periods for the entire bond portfolio. The Bond Analysis Package can operate with any B 200/300 6-microsecond central processor that has a card reader and line printer as peripheral devices.

On-Line Teller System

Reference: . . . . Burroughs Corp.
Date available: . . . . . January, 1965.
Description:

The On-Line Teller System is basically a special configuration of on-line and off-line banking-oriented hardware designed to permit direct communications between tellers located in branch offices and a centrally-located data processing center. Burroughs has prepared good documentation on the overall On-Line Teller System, and has designed an input-output controller program to regulate all messages and replies to and from the processing center. The data communications equipment that functions as the data link between Burroughs Teller Consoles and the B 200/300 central processor is described in detail in Report Section 201:103.

B 200/300 Flow Chart Generator

Reference: . . . . Burroughs Corp.
Date available: . . . . . June, 1965.
Description:

The Flow Chart Generator produces detailed logic flow charts, using standard symbols, for programs coded in either the Basic or Advanced Assembly Languages. The program provides numbered exit connectors with flow chart page numbers for ease of program logic tracing. The remarks portion of each symbolic source statement appears within the statement's charted symbol, justified and hyphenated as required. The symbol also contains the mnemonic operation code for the statement represented by the symbol. Charting proceeds horizontally on the printed output and includes all program segment headings and symbolic labels or references. Multiple-branch program switches are clearly charted. Any invalid or nonexistent exit points are checked and indicated as being in error.

In order to use the Flow Chart Generator, an input tape must first be created during a Basic or Advanced Assembly operation. Equipment configuration requirements include a B 200/300 Series 6-microsecond central processor, three magnetic tape units, one card reader, and one line printer, in any available models.

PROCESS ORIENTED LANGUAGE: COMPACT COBOL

.1 GENERAL

.11 Identity: . . . . B 200 Compact COBOL.

.12 Origin: . . . . Burroughs Corporation.

.13 Reference: . . . . Compact COBOL for Burroughs B 270/B280 Series Systems, Utility Routine Series URS-052.

.14 Description

Compact COBOL is a subset of COBOL-61 that is designed primarily for use in small-scale computers. The standard language specifications for Compact COBOL used in this section are those published in the American Standards Association's X3.4 COBOL Information Bulletin #5 in October, 1964. (It should be noted that Compact COBOL has not been adopted as an American standard to date.) B 200 Compact COBOL incorporates most of the features of Compact COBOL listed in the ASA document. Some features of COBOL-61 which are not provided in the specifications for the Compact version have been included in B 200 Compact COBOL. These are listed below in the paragraphs headed "Restrictions" and "Extensions."

The B 200 Compact COBOL Translator requires a B 273, B 283, or B 300 Central Processor with 4,800 positions of core storage, a card reader, a printer, and four magnetic tape units. A description of the translator can be found in Section 201:183.

.141 Availability

Language specifications: . . . . Burroughs B 200 Compact COBOL Programmed Instruction Course: June, 1964.
Compiler: . . . . November, 1964.

.142 Restrictions of B 200 Compact COBOL with Respect to ASA X3.4 CIB #5

(1) Limits are placed upon the number of data-names and procedure-names used in a program.

(2) The decimal point in numeric literals cannot be at the left end of a number.

(3) There are no SPECIAL-NAMES or I-O-CONTROL paragraphs in the Environment Division.

(4) The MULTIPLE REEL clause of the FILE-CONTROL entry is not permitted.

(5) The VALUE OF clause of the File Description entry is restricted to the use of non-numeric literals.

(6) The ADD and SUBTRACT verbs permit only two quantities to be added or subtracted. The words TO or GIVING must be used with these verbs.

(7) The words TO or GIVING must be used with the verbs MULTIPLY and DIVIDE.

(8) The DISPLAY and ACCEPT verbs cannot be used.

(9) The REEL option for the CLOSE verb is not allowed.

.143 Extensions of B 200 Compact COBOL with respect to ASA X3.4 CIB #5

(1) Data-names and procedure-names do not need to have an alphabetic as the first character.

(2) Section-names are allowed.

(3) The following figurative constants are allowed: ZEROS, ZEROES, SPACE, TAPE-MARK, and GROUP-MARK.

(4) The SOURCE-COMPUTER and OBJECT-COMPUTER paragraphs of the Environment Division can have the MEMORY SIZE clause and can indicate the number of CARD READERS, LINE-PRINTERS, etc.

(5) Indentation is allowed in the Record Description entry of the Data Division.

(6) In Record Descriptions, the SIZE, SIGNED, and CLASS clauses are permitted.

(7) The phrase OTHERWISE (ELSE) is permitted in conditional statements.

(8) The phases EQUALS and EXCEEDS are permitted in relation tests.

(9) The EXAMINE verb with the REPLACING ALL option is provided.

(10) Option 2 of the PERFORM verb (TIMES) is allowed.

(11) An AT END OF REEL clause is added to the WRITE verb.

(12) The symbol ; (semicolon) and the word THEN can be used as separators.

(13) The word CHANNEL is reserved for spacing on the line printer.

PROCESS ORIENTED LANGUAGE: DISK FILE COBOL

.1 GENERAL

.11 Identity: . . . . B 200 Disk File COBOL.

.12 Origin: . . . . E. Saumets Associates (under contract to Burroughs Corp.)

.13 Reference: . . . . "Burroughs B 200 Disk File COBOL Compiler Description" (preliminary information).

.14 Description

The B 200 Disk File COBOL Compiler will accept most of the language facilities of Required COBOL-61 and a number of the facilities of Elective COBOL-61. This new compiler is designed to take advantage of the fast-access, high-capacity storage provided by the Burroughs Disk File during both compilation and (when desired) object program execution. Equipment requirements for compilation are a B 200/300 6-microsecond central processor with 9,600 positions of core storage, one module of Disk File storage, one magnetic tape unit, a card reader, and a printer. A card punch is also required if object program decks are to be produced on punched cards. Burroughs expects the compiler to use a total of 12 Disk File data tracks of 24,000 characters each.

Although no detailed definition of the B 200 Disk File COBOL language is available to date, present indications are that it will include all of Required COBOL-61 except for the minor deficiencies listed in Paragraph .142 below. Approximately ten of the elements of Elective COBOL-61 will be implemented, including the COMPUTE, ENTER, and USE verbs, the ADVANCING option of the WRITE verb, compound conditional statements, the I-O-CONTROL paragraph, and segmentation of the object program.

The most significant extensions to the COBOL-61 language in B 200 Disk File COBOL are those provided to facilitate Disk File processing. A special File Description entry (type MD) permits the programmer to specify FILE-LIMITS, ACCESS MODE (SEQUENTIAL or RANDOM), and ACTUAL KEY, in addition to most of the entries in the type FD File Description entry used for files stored on sequential media. The OPEN verb can specify that a file will be used for both input and output. In the READ and WRITE verbs, a branch to any imperative statement can be executed upon detection of an invalid key.

Sequential access to Disk File records will be provided automatically by the compiler. The programmer is responsible for file organization and layout, and for any indirect addressing techniques he chooses to use. The Disk File records can be divided into header and trailer records, which can be physically separated from one another. No file may extend over more than one Disk File Storage Unit consisting of one B 472 and up to four additional B 475 modules (a maximum of 48 million characters).

Compilations can be performed in any of three modes: Compile and Go, Compile Deferred, and Compile Stack. Compilation speeds of about 75 source-program cards per minute are anticipated by the manufacturer on typical, "well-balanced" source programs. Burroughs expects the compiler to detect and flag all syntax errors in the Data and Procedure Divisions during the first compilation attempt unless a sentence contains more than one error; in this case only the first error encountered will be flagged during each compilation attempt. Error diagnostics will be interspersed among the lines of source coding in the source program listing.

Data and procedure names can be up to 30 characters in length; in the absence of qualification, only the first 23 characters will be scanned to determine uniqueness. When data and procedure names average seven characters or less in length, it will be possible to store up to 600 unique names in the symbolic dictionaries. There are no limitations upon the total number of referenced data names nor on the number of Procedure Division literals. A maximum of 24 files can be described in any one source program. A standard label-handling technique is provided.

.141 Availability

Language: . . . . July, 1965.
Compiler: . . . . July, 1965.

.142 Deficiencies with Respect to Required COBOL-61

- The SYNCHRONIZED and FLOAT DOLLAR SIGN clauses of the Record Description entry are not permitted.
- No more than three nested levels are permitted in the OCCURS clause of the Record Description entry.
- Only simple conditions can be specified in the UNTIL options of the PERFORM verb.

.143 Extensions to COBOL-61

- Features added to facilitate the use of mass storage include a special MD File Description entry and special options for the READ, WRITE, OPEN, CLOSE, and USE verbs; see the Description above.
- A WRITE verb option permits branching to any imperative statement at the end of a page or reel of the output file medium.

MACHINE ORIENTED LANGUAGE: BASIC ASSEMBLY LANGUAGE

.1 GENERAL

.11 Identity: . . . . B 100/200/300 Series Basic Assembly Language.

.12 Origin: . . . . Burroughs Corp.

.13 Reference: . . . . . . Manual URS-041.

.14 Description

This is a straightforward symbolic assembly language usable on any B 100/200/300 Series system that includes a card (or punched tape) reader and punch. Magnetic tape can be utilized when available to speed up the translation process and reduce card handling. The only unusual language features are those which are necessitated by the machine address digit radices of 12, 10, and 40. A special macro operation is provided to step an address by a chosen value. Pseudo-instructions are provided to control the allocation of storage.

The B 200 Series Basic Assembly Language offers less flexibility in label naming than most symbolic assembly systems. A two-character "page" field (used to assign coding sheet page numbers) and a one-character "reference symbol" together make up the three-character symbolic address of an instruction and/or data field.

.15 Publication Date: . . . August, 1961.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . refer to Assembly Language Coding Specimen, Page 201:131.100.

.22 Legend

IDENT NO.: . . . . . . 6 alphameric character program identification number.
OP: . . . . 3 alphabetic character mnemonic operation code.
M: . . . . 2 alphameric character operation code variant.
N: . . . . 2 alphameric character operation code variant.
A, B, C ADDRESS:. . operand addresses, in 3 parts.
PAGE: . . . . 2 alphameric character coding sheet.
REF: . . . . optional 1 alphameric character line label.
SIZE: . . . . 3 digits; number of characters in a constant.
CONSTANTS: . . . . . 12 alphameric characters, for literals or data areas.
REMARKS: . . . . coder's remarks.
Columns 72-77: . . . . reserved for translator use.
LINE: . . . . 3 digit input sequence number for lines of coding.

.23 Corrections: . . . . . . use inserts in the LINE numbers and manual replacement.

.24 Special Conventions

.241 Compound addresses: none.
.242 Multi-addresses: . . . one per column; usually three addresses per line.
.243 Literals: . . . . * in first column of Address field plus literal in Constants field.
.244 Special coded addresses: . . . . bb*J is "This address plus 12" (b denotes blank).
- in first column of an Address field indicates address of next instruction is to be inserted.
.245 Other —
Axxx: . . . . address of xxx.
xxxJ: . . . . address xxx+12.
xxxK: . . . . address xxx+24.
xxxL: . . . . address xxx+36.
Mxxx: . . . . actual data to appear in machine coding.

.3 LABELS

.31 General

.311 Maximum number of labels —
Procedures: . . . . . 1,800.
Constants: . . . . . . 200.
Items: . . . . 1,800.
.312 Common label formation rule: . . . . yes.
.313 Reserved labels: . . . yes.
.314 Other restrictions: . see .315.
.315 Designators —
Address value: . . . initial letter A.
Absolute value: . . . initial letter M.
Literal: . . . . * in col 14 and 18.

.32 Universal Labels

.321 Labels for procedures —
Existence: . . . . . . mandatory.
Formation rule: . . address of first statement.
.322 Labels for library routines: . . . . yes.
.323 Labels for constants: address.
.324 Labels for files: . . . none.

.325 Labels for records: . . none.
.326 Labels for variables:. address.

.33 Local Labels: . . . . . none.

.4 DATA

.41 Constants

.411 Maximum size constants: . . . . . . 12 characters.
.412 Maximum size literals: . . . . 12 characters.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence: . . . . . . yes.
Number: . . . . 30 (VRC), 37 (B 260, B 270, B 280). 49 (B 263, B 273, B 283), or 58 (B 300).
Example: . . . . ADD.
Comment: . . . . . . all 3 characters in size.
.512 Absolute: . . . . none.

.52 Macro-Codes

.521 Number available —
Addressing: . . . . . 2.
.522 Examples —
Simple: . . . . LNK.
.523 New macros: . . . . . none.

.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control —
Allocation counter:. . pseudo.
Label adjustment:. . none.
Annotation: . . . . . . REMARKS columns

.542 Allocation counter —
Set to absolute: . . . SLC.
Set to label: . . . . . OVR.
Step forward: . . . . ALC.
Step backward: . . . SLC.
Reserve area: . . . . CST.

.543 Label adjustment —
Set labels equal:. . no.
Set absolute value: no.
Clear label table: . no.
.544 Annotation —
Comment phrase: . special columns. HDG pseudo.
Title phrase: . . . . special box.
.545 Other —
End of program:. . END.

.6 SPECIAL ROUTINES AVAILABLE: . . . see Section 201:151.

.7 LIBRARY FACILITIES: . . . none.

.8 MACRO AND PSEUDO TABLES

.81 Macros

Code	Description
LNK:	sets linkage for subroutines.
AAR:	steps an address value (by creating a linkage to a closed, 30-instruction address modification subroutine).

.82 Pseudos

Code	Description
SLC:	set allocation counter to absolute value.
ALC:	step allocation counter forward.
END:	end assembly.
OVR:	sets allocation counter to any value (absolute or symbolic) and assembles balance of first 4,800 characters in auto-load form with literals.
SAD:	permits M and N columns to be used together for a symbolic address.
HDG:	allows identification or explanatory remarks.
CST:	defines I/O areas, working storage, constants, and masks.
IGM:	inserts a group mark character in core storage.

MACHINE ORIENTED LANGUAGE: ADVANCED ASSEMBLY LANGUAGE

.1 GENERAL

.11 Identity: . . . . Advanced Assembler I.

.12 Origin: . . . . Burroughs Corp.

.13 Reference: Manual URS-044.

.14 Description

Advanced Assembler I is an expanded version of the Burroughs Basic Assembler (see page 201:171.100). The principal features of this new assembly language include the capability to use up to 10,000 six-character name labels and the provision for use of a comprehensive and expandable library of program subroutines. The limited label-naming facilities of the Basic Assembly Language have been further improved in the new version by the inclusion of up to 10,000 program point labels to complement the use of symbolic name labels. A fixed field-length coding form, similar to the IBM Symbolic Programming System (SPS) coding form, has been retained. Operand lengths need not be specified in every instruction. The size of the operand is specified once, in the Data Division section of the program. All subsequent references to the operand will then have the correct size inserted by the translator.

The Advanced Assembler I translator requires a B 200/300 6-microsecond Central Processor and 3 magnetic tape units, in addition to a card reader, line printer, and card punch, in any models. If Disk File storage is available, only one magnetic tape unit is required for use in conjunction with one Disk File storage module. Programs written in the Basic Assembly Language can also be assembled by the Advanced Assembler I in order to utilize the increased capabilities of the improved translator. See Section 201:182 for further details about the Advanced Assembler I translator.

The major improvements of the Advanced Assembler I over the B 200 Basic Assembler can be summarized as follows:

- Either Basic Assembler or Advanced Assembler I is acceptable as symbolic-language input.
- Up to 10,000 six-character symbolic name labels and 10,000 program point labels can be utilized.
- Up to 100 program point labels of the same character are permitted within a program segment.
- Up to 20 library subroutine call entries are permitted within a program segment.
- Furnished library subroutines include input-output error procedures and their linkages, as well as a debugging package of dumps, snapshots, and tracers.
- Automatic field-length definition is provided to facilitate the coding of all arithmetic, compare, data transfer, and editing commands.
- Symbolic address incrementing by up to 999 characters is provided, in addition to entry incrementing and decrementing by up to 99 entries.
- Symbol tables or cross-reference listings of labels can be provided if desired.

.15 Publication Date: . . . . May, 1964.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . refer to Assembly Language Coding Form, page 201:131.100.

.22 Legend:

Page: . . . . 3-alphameric-character coding form sequence number.

Line: . . . . 3-alphameric-character entry sequence number; units position is used for insertions.

Symbolic Label: . . . . 6-alphameric-character field or instruction name; or a decimal point and a reusable alphabetic character program point marker.

Op. Code: . . . . 4-alphameric-character mnemonic operation code.

Variant: . . . . 4-numeric-digit operation code modifier; for many commands it is separated into 2-digit M and N Variant modifiers.

A, B, C address: . . . . operand addresses, in 3 parts.

Tag: . . . . 6-alphameric-character operand base address, in the form of labels, ± program points, self-addressing, machine language, or literals. Literals cannot be used in the calling string of library subroutines.

.22 Legend (Contd.)

ENT: . . . . 1-character-sign and 2-numeric-digit Tag address entry-modifier. Entry modifications cannot be used with machine language coding or literals.
Char: . . . . 3-alphameric-character increment factor added to the net address formed by the Tag and Entry modifier.
Remarks: . . . . 24-alphameric-character field for coder's comments.

.23 Corrections

.231 Insertions: . . . . use units position of line field as insert number and manually insert card.

.24 Special Conventions

.241 Compound addresses: . Tab ± entry-modifier + character increment = address.
.242 Multi-address: . . . . . one per column, three per entry.
.243 Literals: . . . . from 1 to 6 characters in arithmetic, compare, and transfer commands.
.244 Special coded addresses: . . . . ± alphabetic character indicates next instruction labeled with same character.
.245 Others —
*xxxxx: . . . . address of instruction in which it appears.
@xxx: . . . . actual data can be entered in machine language.
#xxxxxx: . . . . literals.

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . 10,000 universal and 10,000 local labels.
.312 Common label formation rule: . . . . . . yes.
.313 Reserved labels: . . . . none.
.314 Other restrictions: . . . see next entry.
.315 Designators —
Symbolic name: . . . . initial character must be alphabetic.
Program point: . . . . initial character must be a decimal point, followed by an alphabetic character.
.316 Synonyms permitted: . any symbolic name can be equated to any other prior name.

.32 Universal Labels

.321 Labels for procedures —
Existence: . . . . mandatory if referenced by other instructions.
Formation rule —
First character: . . . alphabetic.
Other: . . . . any alphameric characters.
Number of characters: . . . . 1 to 6.
.322 Labels for library routines: . . . . none.
.323 Labels for constants: . same as Procedures.
.324 Labels for files: . . . . none.
.325 Labels for records: . . same as Procedures.
.326 Labels for variables: . same as Procedures.

.33 Local Labels

.331 Region: . . . . local to the closest point of reference.
.332 Labels for procedures —
Existence: . . . . mandatory if referenced by other instructions.
Region: . . . . local to the closest point of reference.
Formation rule —
First character: . . . decimal point.
Last character: . . . alphabetic character.
Number of characters: . . . . two.
.333 Labels for library routines: . . . . none.
.334 Labels for constants: . same as Procedures.
.335 Labels for files: . . . . none.
.336 Labels for records: . . same as Procedures.
.337 Labels for variables: . same as Procedures.

.4 DATA

.41 Constants

.411 Maximum size constants —
Numeric: . . . . 60 characters.
Alphabetic: . . . . 60 characters.
Alphameric: . . . . . . 60 characters.
.412 Maximum size literals —
Numeric: . . . . 12 characters.
Alphabetic: . . . . 12 characters.
Alphameric: . . . . . . 12 characters.

.42 Working Areas

.421 Data layout —
Implied by use: . . . . no.
Specified by program: . . . . yes.
.422 Data type: . . . . not required.
.423 Redefinition: . . . . yes; EQU pseudo operation.

.43 Input-Output Areas

.431 Data layout: . . . . explicit layout.
.432 Data type: . . . . not required.
.433 Copy layout: . . . . no provision.

(Contd.)

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence: . . . . yes; mandatory.
Number: . . . . 58.
Example: . . . . CRD.
Comment: . . . . all are 3 characters in size.
.512 Absolute: . . . . none.

.52 Macro-Codes

.521 Number available —
Input-output: . . . . . . 5.
Arithmetic: . . . . . . none.
Math functions: . . . . none.
Error control: . . . . . contained within input output macros.
Restarts: . . . . none.
Program control: . . 2.
.522 Examples: . . . . see Paragraph .81
.523 New macros: . . . . inserted into library in separate run.
.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control —
Allocation counter: . . pseudo operations.
Label adjustment: . . pseudo operations.
Annotation: . . . . coder's comments.
.542 Allocation counter —
Set to absolute: . . . . SLC, OVR pseudos.
Set to label: . . . . . . OVR pseudo.
Step forward: . . . . . ALC pseudo.
Step backward: . . . . . SLC pseudo.
Reserve area: . . . . . CST, RSV, pseudos.
.543 Label adjustment —
Set labels equal: . . . . EQU pseudo.
Set absolute value: . . EQU pseudo.
Clear label table: . . . none.
.544 Annotation —
Comment phrase: . . . HDG pseudo.
Title phrase: . . . . . . HEAD card.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: . . none.

.62 Special Functions: none.

.63 Overlay Control

.631 Facilities: . . . . OVR macro sets allocation counter to any value, absolute or symbolic, and assembles balance of first auto-load program deck to end of memory.
.632 Method of call: . . . . . OVR macro.

.64 Data Editing

.641 Radix conversion: . . . none.
.642 Code translation: . . . . not required due to hardware code translation capability.
.643 Format control: . . . . not required due to hardware editing capabilities.

.65 Input-Output Control

.651 File labels: . . . . none.
.652 Reel labels: . . . . none.
.653 Blocking: . . . . none.
.654 Error control: . . . . . input-output operations.
.655 Method of call: . . . . . . macros.

.66 Sorting: . . . . no routines that can be embedded in a program.

.67 Diagnostics

.671 Dumps: . . . . specified section of core storage is printed at object time by means of DUMP pseudo. DBUG control card removal negates all diagnostic pseudos.
.672 Tracers: . . . . traces all instructions following TRAC pseudo up to the address specified in the B address, in TRAC. DBUG pseudo is required for use of tracers.
.673 Snapshots: . . . . SNAP pseudo prints at object program time the symbolic name, machine address, and 120 characters starting with the address specified in the SNAP pseudo. Up to 9 addresses can be controlled by the SNAP and DBUG pseudos.

.7 LIBRARY FACILITIES

.71 Identity: . . . . Advanced Assembler I System Library

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.
.723 Private: . . . . private facilities can be added to master library.

.73 Storage Form: . . . . . tape (supplied on cards for transcription to tape).

.74 Varieties of Contents: . macro instructions and their linkages, input-output error routines, and subroutines for debugging.

.75 Mechanism

.751 Insertion of new item: . special library assembly run.
.752 Language of new item: . Advanced Assembler I.
.753 Method of call: . . . . . CALL pseudo with routine name in A address of entry, or any macro entry.

.76 Insertion in Program

.761 Open routines exist: . . yes; user-defined macros.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: . . . . no.
.764 Closed routines appear once: . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros

Macros	Description
MTR:	sets linkage to and calls in the magnetic tape read error routine; generates tape read instruction.
MTW:	sets linkage to and calls in the magnetic tape write error routine; generates tape write instruction.
DRD:	sets linkage to and calls in disk read error routine; generates disk read and interrogate commands.
DWR:	sets linkage to and calls in disk write error routine; generates disk write and interrogate commands.
DWC:	functions the same as DWR except that a disk check command and its linkage are also generated.
LNK:	creates the necessary two-instruction linkage to and from a routine and branches to the routine.
SET:	functions the same as LNK except that no branch is taken.

.82 Pseudos

Code	Description
SLC:	sets location counter to a specified absolute or symbolic value.
ALC:	sets location counter ahead by a specified number of fields and characters.
EQU:	symbolic name in label field is given the same absolute value as another specified name or machine value.
CST:	loads a constant field up to 60 characters in length; if more than 60 characters are specified, the balance will be reserved with blanks.

.82 Pseudos (Contd.)

Code	Description
RSV:	reserves a specified number of characters in storage.
HDG:	generates coder's remarks on output listing.
OVR:	sets location counter to any value, absolute or symbolic, and causes overlaid routines to follow the main object program deck.
SAD2:	generates a two-character machine address constant for each symbolic address specified.
SAD3:	generates a three-character machine address constant for each symbolic address specified.
LORG:	specifies that all literals following LORG be packed in an area of memory subsequent to the current setting of the location counter to prevent destruction by overlays.
GPMK:	generates a one-position group mark character.
TPMK:	generates a two-position constant consisting of end-of-tape and group marks.
CALL:	calls in a specified library routine for assembly at end of program.
SUBR:	functions the same as CALL, but also functions within overlays.
TEMP:	inserts a temporary routine into the library for use in the program being assembled only.
END:	terminates every temporary library routine and every program.
FINI:	terminates any given number of consecutive assembly operations.
DBUG:	controls use of all DUMP, TRAC, and SNAP pseudo operations.
DUMP:	prints at object program time the contents of a specified section of core storage.
TRAC:	selectively traces specified program areas at object program time.
SNAP:	prints symbolic name, machine address, and 120 characters of address specified.

PROGRAM TRANSLATOR: BASIC ASSEMBLER

.1 GENERAL

.11 Identity: . . . . B 100/200/300 Series Basic Assembler.

.12 Description

This translator can be run on any B 100/200/300 Series configuration with a card or paper tape reader and punch. Listings can be provided if a printer is available. The translator can take advantage of any magnetic tapes available on the translating computer to speed up the translation process and reduce card handling.

Translation requires three passes and is limited in speed by the output equipment: a punch or magnetic tape unit.

.13 Originator: . . . . Burroughs Corp.

.14 Maintainer: . . . . . . Burroughs Corp.

.15 Availability: . . . . . . March, 1961.

.2 INPUT

.21 Language

.211 Name: . . . . Burroughs Basic Assembly Language, described in Section 201:171.
.212 Exemptions: . . . . . . none.

.22 Form

.221 Input media: . . . . . . punched cards or paper tape.
.222 Obligatory ordering: . in line sequence order.

.23 Size Limitations: . . . limited by hardware; maximum of 1,800 labels and 200 constants.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . Basic Assembly Language.
.312 Language style: . . . machine code.
.313 Output media: . . . . . auto-load card deck or tape; printer listing.

.32 Conventions: . . . . . none.

.33 Documentation

Subject	Provision
Source program . . .	listing.
Object program: . . .	listing.
Storage map:	implied.
Language errors: . .	listing.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Label table pass: . . . check op. codes, etc.
Translate pass: . . . . assign addresses.
Auto-load deck output: final output.

.42 Optional Modes

.421 Translate: . . . . yes.
.422 Translate and run: . . no.
.423 Check only: . . . . no.
.424 Patching: . . . . no.
.425 Updating: . . . . no.

.43 Special Features: . . . none.

.44 Bulk Translating: . . . yes.

.45 Program Diagnostics: none.

.46 Translator Library: . none.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . . none.
.512 Space required for each input-output file: . . as coded.
.513 Approximate expansion of procedures: . . . unity.

.52 Translation Time

.521 Normal translating: . usually output limited.
5 minutes maximum on cards; 300 cards/minute.
3 minutes maximum on tape; 700 instructions/minute.

.53 Optimizing Data: . . . none.

.54 Object Program Performance: . . . unaffected; i.e., same as hand coding.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . . 1 card or paper tape reader.
1 card or paper tape punch.
1 central processor.

.612 Larger configuration advantages: . . . . . . use printer for program listing.
use magnetic tape to speed up run and avoid card handling.

.62 Target Computer

.621 Minimum configuration: . . . . 1 card or paper tape reader and 1 output device.

.622 Usable extra facilities: all.

.7 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries:	check	listing.
Duplicate names:	check	listing.
Improper format:	check	listing.
Target computer overflow:	check	listing.

.8 ALTERNATIVE TRANSLATORS: . . . Advanced Assembler I translates either Basic Assembly language or Advanced Assembly language programs.

PROGRAM TRANSLATOR: ADVANCED ASSEMBLER I

.1 GENERAL

.11 Identity: . . . . Advanced Assembler I.

.12 Description

The Advanced Assembler I translator is a multiphase tape or disk oriented program designed to translate relatively large source programs (including up to 10,000 symbolic labels) within 4,800 characters of core storage. The minimum requirements for the translation process include a B 200/300 6-microsecond Central Processor and either three magnetic tape units or one tape unit and one module of Disk File storage. The translator can accommodate programs written in either the Basic or Advanced Assembly Language and contained in card image form on either cards, paper tape, magnetic tape, or disk storage. A program listing and the machine-language autoload output are produced as desired on cards, printer, paper tape, and/or magnetic tape.

The translator program itself is contained on magnetic tape. During the translation process, a minimum of 11 functionally-distinct phases are called in and performed. Resultant translation times fall between 75 and 150 entries per minute, depending upon the speed of the output equipment and the number of output options elected. All translator phase loadings and modifications are self-performed and require no monitor.

The Advanced Assembler I translator provides subroutine library facilities, automatic operand length definition, complete language error checking, entry and character adjustments to symbolic addresses, and cross-referenced symbol tables.

The output program listing consists of the machine-language instruction and its location in core storage, the source coding, error messages derived from invalid or defective coding, all generated instructions and routines, and the location of each entry in the auto-load card deck.

.13 Originator: . . . . Burroughs Corp.

.14 Maintainer: . . . . Burroughs Corp.

.15 Availability: . . . . October, 1964.

.2 INPUT

.21 Language

.211 Name: . . . . Advanced Assembly or Basic Assembly Language.

.212 Exemptions: . . . . none.

.22 Form

.221 Input media: . . . . card images on cards, paper tape, magnetic tape, or disk file.

.222 Obligatory ordering: . . must be in correct sequence according to coding sheet page and line numbers.

.223 Obligatory grouping: . . none.

.23 Size Limitations

.231 Maximum number of source statements: . . unlimited.

.232 Maximum size of source statements: . . 80 characters.

.233 Maximum number of named data items: . . 10,000.

.234 Maximum number of program point labels: 10,000.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . . . Burroughs Common Language.

.312 Language style: . . . . . machine language.

.313 Output media: . . . . . . punched cards, paper tape, or magnetic tape.

.32 Conventions

.321 Standard inclusions: . . input-output error routines.

.322 Compatible with: . . . . Advanced Assembler Program Library.

.33 Documentation

Subject	Provision
Source program:	listing.
Object program:	listing.
Storage map:	implied.
Restart point list:	none.
Language errors:	messages on listing.
Label table:	listing with cross-referencing.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Phase 1: . . . . edits parameter card; calls in appropriate input-output routines.

Phase 2: . . . . translates source language, assigns operation codes, and adds temporary library routines.

Phase 3: . . . . calls in any necessary library routines; checks validity of operation codes and library routines.

Phase 4: . . . . checks M and N variants; assigns machine-language equivalents.

.41 Phases and Passes (Contd.)

Phase 5: . . . . constructs literal table; packs literals into unused addresses of instructions.

Phase 6: . . . . writes labels and program points to tape; assigns machine addresses to instructions and constants.

Phase 7: . . . . transfers addresses called for from library calling strings to library routine skeletons.

Phase 8: . . . . assigns addresses to symbolic labels, flagging duplicate or unused labels.

Phase 9: . . . . builds entry increment table; modifies machine-language addresses by entry increments.

Phase 10: . . . . assembles final machine-language instruction; performs any necessary character incrementation.

Phase 11: . . . . generates object-coded auto-load output; formats source code for listings.

Phase 12: . . . . produces symbolic listing on specified output media; develops label cross-reference list.

Phase 13: . . . . sorts label table; calls in and modifies Phase 12 for outputting of edited lable table or cross-reference list.

.42 Optional Mode

.421 Translate: . . . . yes.
.422 Translate and run: . . . no.
.423 Check only: . . . . no.
.424 Patching: . . . . no.
.425 Updating: . . . . no.

.43 Special Features

.431 Alter to check only: . . no.
.432 Fast unoptimized translate: . . . . no.
.433 Short translate on restricted program: . Phases 12 and 13 can be skipped if symbolic output is not desired.

.44 Bulk Translating: . . . yes, but only when source programs are on punched cards.

.45 Program Diagnostics

.451 Tracers: . . . . can be integrated into object program; removal of DBUG source card causes diagnostics to be ignored during subsequent assemblies.
.452 Snapshots: . . . . same as in .451, above.
.453 Dumps: . . . . same as in .451, above.

.46 Translator Library: . . see Paragraph 201:172.7.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . . . none.
.512 Space required for each input-output file: . . . . same as block length.
.513 Approximate expansion of procedures: . . . . . one to one, exclusive of macros.

.52 Translation Time

.521 Normal translating: . . 0.013S minutes, reading source cards at 800 cpm and punching auto-load deck at 300 cpm, where S is number of statements in source program.
.522 Checking only: . . . . . . none.
.523 Unoptimized translating: . . . . none.

.53 Optimizing Data: . . . . none.

.54 Object Program Performance: . . . . . unaffected by translation; i.e., same as hand coding.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: B 200/300 6-microsecond Central Processor with 4,800 positions of core storage.
3 magnetic tape units (any model).
1 card reader (any model).
1 card punch (B 303 or B 304).

.612 Larger configuration advantages: . . . . additional core storage can reduce number of translator passes per phase by handling more labels per pass; any model line printer provides variety of output documentation.

.62 Target Computer

.621 Minimum configuration: . . . . no limitations.
.622 Usable extra facilities: . . . . everything except B 401 Record Processor with VRC systems.

.7 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries:	check	noted in listing.
Duplicate names:	check	noted in listing.
Improper format:	check	noted in listing.
Incomplete entries:	check	noted in listing.
Target computer overflow:	check	noted in listing.
Inconsistent program:	none.	
Undefined names:	check	noted in listing.
Parameter card errors:	check	noted in listing; source deck is bypassed.

.8 ALTERNATIVE TRANSLATORS: . . . none available (but see also the Basic Assembler, Section 201:181).

PROGRAM TRANSLATOR: COMPACT COBOL

.1 GENERAL

.11 Identity: . . . . B 200 Compact COBOL.

.12 Description

The B 200 Compact COBOL Translator converts source programs written in the B 200 Compact COBOL language (as described in Section 201:161) into machine code. Compilation proceeds at the rate of approximately 50 source cards per minute.

Minimum configuration requirements for the translator are a B 273, B 283, or B 300 Central Processor with 4,800 positions of core storage, a card reader, a line printer, and 4 magnetic tape units. Additional core storage and a card punch can be utilized when available. Object programs can be run on any B 263, B 273, B 283, or B 300 Series system equipped with the appropriate peripheral devices. B 200 Compact COBOL does not provide for the use of MICR sorter-readers, Disk Files, data communications devices, paper tape equipment, or listers.

The B 200 Compact COBOL Translator provides debugging aids, printer listings, and diagnostic printouts. The programming manual (Burroughs publication URS-052) lists various methods for optimizing compilation times and/or object program efficiencies for all COBOL divisions and each B 200 Compact COBOL verb.

.13 Originator: . . . . E. Saumets Associates.

.14 Maintainer: . . . . Burroughs Corp.

.15 Availability: . . . . November, 1964.

.2 INPUT

.21 Language

.211 Name: . . . . B 200 Compact COBOL; see Section 201:161.
.212 Exemptions: . . . . none.

.22 Form

.221 Input media: . . . . punched cards.
.222 Obligatory ordering: . . Identification Division
Environment Division
Data Division
Procedure Division
.223 Obligatory grouping: . . by division, section, paragraph.

.23 Size Limitations

.231 Maximum number of source statements: . . limited by size of target computer's core storage.
.232 Maximum size source statements: . . . . limited to use of one verb and one to three operands per statement.
.233 Maximum number of data names: . . . . . . 190.
.234 Others —
Maximum number of object code instructions: . . . . . 2,800.
Procedure names: . . 40.
Elements in an array: 119.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . . . B 200 Series machine language.
.312 Language style: . . . . . machine code.
.313 Output media: . . . . . . magnetic tape or punched cards.

.33 Documentation

Subject	Provision
Source program:	listing.
Object program:	listing (optional).
Storage map:	listing (optional).
Restart point list: . . .	none.
Language errors:	listing.
Object program-source program cross-reference table:	listing.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Phase 1: . . . . reads source program, edits, performs lexical checks, lists source program, and stores it on tape.
Phase 2: . . . . reduces symbols and processes labels.
Phase 3: . . . . reduces data-names, prescans Pictures, performs label definition look-up.
Phase 4: . . . . analyzes symbols and processes Picture items.
Phase 5: . . . . processes Data Division, Procedure Division syntax, memory allocation, and mask interpretation; replaces data items with sets of properties.

.41 Phases and Passes (Contd.)

Phase 6: . . . . generates literals, operand calls, descriptor calls, and subroutine calls.

Phase 7: . . . . processes value literals, assembles object program, optimizes masks, writes loader, trace, and value literals on object tape, optimizes space occupied by literals, prints diagnostic messages.

.42 Optional Model

.421 Translate: . . . . yes.
.422 Translate and run: . . . yes.
.423 Check only: . . . . no.
.424 Patching: . . . . no.
.425 Updating: . . . . no.

.43 Special Features

.431 Alter to check only: . . no.
.432 Fast unoptimized translate: . . . . no.
.433 Short translate on restricted program: . no.

.44 Bulk Translating: . . . yes.

.45 Program Diagnostics

.451 Tracers: . . . . object time routine, included with object program.
.452 Snapshots: . . . . File Status Table can be printed at object time.
.453 Dumps: . . . . routines available at compile or object time.

.46 Translator Library: . . none.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . . . none.
.512 Space required for each input-output file: . . . . as specified in Data Division of source program.
.513 Approximate expansion of procedures: . . . . . 3 to 1.

.52 Translation Time: . . . approximately 50 source cards/minute.

.53 Optimizing Data: . . . . a list of ways in which the programmer can optimize both compile time and execution time is provided in the manual.

.54 Object Program Performance: . . . . . uses approximately 30% more core storage than good hand coding requires, but execution times are about the same, according to the manufacturer.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: B 273, B 283, or B 300 Central Processor with 4,800 positions of core storage.
B 122, 123, or 124 Card Reader.
B 320 or 321 Line Printer.
Four B 421, 422, or 423 Magnetic Tape Units.

.61 Larger configuration advantages: . . . . 4,800 additional core positions permit compilation of larger programs with a maximum of 400 data names.
B 303 or 304 Card Punch provides punched card output of object program.

.62 Target Computer

.621 Minimum configuration: any B 263, B 273, B 283, or B 300 Series System.

.622 Usable extra facilities: . . . . all except MICR sorter-reader, Disk File, data communications devices, paper tape, and listers.

.7 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Missing entries:	check	halt and/or diagnostic message.
Unsequenced entries:	none.	
Duplicate names:	check	diagnostic message.
Improper format:	check	diagnostic message.
Incomplete entries:	check	halt and/or diagnostic message.
Target computer overflow:	check	precautionary message.
Inconsistent program:	check	halt and/or diagnostic message.
Limitations on data and procedure names exceeded:	check	halt and diagnostic message.

.8 ALTERNATIVE TRANSLATORS: none.

PROGRAM TRANSLATOR: 1401 SPS TRANSLATOR

.1 GENERAL

.11 Identity: . . . . Burroughs B 200/300 Series Symbolic Program Translator.

.12 Description

The Burroughs Symbolic Program Translator (SPS Translator) converts IBM 1401/1460 SPS programs into Burroughs Assembly Language. The scope of the Translator is limited to translating Symbolic Programming System source code (see Section 401:171 of the IBM 1401 report) in single load format. Condensed SPS or Autocoder source programs cannot be translated.

The minimum configuration requirements for the translating computer are a B 200/300 6-microsecond Central Processor with 4,800 characters of core storage, three magnetic tape units of any model, and any model card reader, card punch, and line printer.

The complete translation process consists of three distinct phases: translation from SPS to Burroughs assembly language; post-translation patching of the assembly language coding as directed by notes on the translation listing; and assembly of the intermediate assembly-language program into Burroughs machine language. If any non-standard features or programming techniques have been utilized in the 1401 source program, direct translation of these program areas is impossible. Disk file instructions also require extensive hand translation and modification during the post-translation edit phase of the translation process.

The Burroughs SPS Translator can be expected to perform efficiently when it is applied to the task of translating card-oriented SPS programs of modest size. No 1401 source program larger than 8,000 characters should be considered for translation and operation on a 9,600-character B 200/300 Central Processor, because the eventually-produced object program consumes between 30% and 60% more core storage than the source program. Object program running times for translated card programs will nearly always be faster than on the 1401, and can be up to four times faster. The improvement is due partially to efficient use of the Burroughs three-address instruction format, but primarily to the completely buffered card input-output devices and printers in the Burroughs system.

Translation times average about 5 minutes for 4,000 characters of IBM 1401 program volume. If the Translator has been applied within the scope of its design, the post-translation edit phase can usually be completed within an hour. Another five to ten minutes is then required to assemble the patched intermediate-language program into the auto-load object program deck.

The principal capabilities of the SPS Translator can be summarized as follows:

- Up to 35 IBM 1401 machine-language or mnemonic operation codes can be translated.
- Decimal machine-language operand addresses are permissible, but only when they reference the fixed card read, punch, and print input-output areas.
- Other decimal machine-language addresses can be used if defined and labeled by a special Define entry prior to translation.
- Address modifications are performed correctly.
- Up to six 1401 Sense Switches are simulated by means of six reserved character positions of core storage.
- Definition of constants and equation of symbolic labels are performed correctly.
- Tape read/write error routines and printer page-overflow simulation routines are automatically generated.
- Compare and Branch instructions, chained data transfers, and other sequences of 1401 instructions are replaced by single instructions wherever possible.

The standard card and tape 1401 SPS instructions are classified by the SPS Translator into four different categories:

(1) The 27 instructions that are directly and accurately translated.

(2) The translated instructions that require modification as noted on the translation listing.

(3) The instructions utilized by the Translator but not actually translated because they are of no use to the object program (e.g., Set Word Mark).

(4) The group of 1401 instructions associated with special programming or hardware features that cannot be directly translated and will require special attention.

In a typical 1401 card processing program, approximately 60% of the instructions will normally fall into category (1), 38% into categories (2) and (3), and 2% into category (4).

.12 Description (Contd.)

The principal IBM 1401 capabilities that cannot be handled by the SPS Translator include:

- Index registers.
- Store Address Register instructions.
- Paper tape devices.
- Disk file devices.
- Any other non-standard features or devices.
- Operation code modifications by arithmetic quantities.

Instructions to read and write magnetic tape can be directly translated. Therefore, the SPS Translator can be effectively utilized to produce functional object programs from tape-oriented source programs of up to 6,000 characters in volume, provided they use primarily standard IBM 1401 programming techniques and features.

.13 Originator: . . . . Burroughs Corporation.

.14 Maintainer: . . . . Burroughs Corporation.

.15 Availability: . . . . January, 1964.

.2 INPUT

.21 Language

.211 Name: . . . . IBM 1401 Symbolic Programming System (SPS).
.212 Exemption: . . . . statements associated with all non-standard programming features and peripheral devices, and with 1401 capabilities not handled by the SPS Translator (see list above).

.22 Form

.221 Input media: . . . . IBM 1401 SPS single load format program deck (or card images of the same type on magnetic tape).
.222 Obligatory ordering: . . none.
.223 Obligatory grouping: . . none.

.23 Size Limitations: . . . . target computer must provide 30% to 60% more core storage than the amount utilized in the original 1401 target computer.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . . . Burroughs Modified Basic Assembly Language is the intermediate result of the translation process; final object program is in Burroughs machine code.

.313 Output media: . . . . . . punched card decks or card images on magnetic tape.

.32 Conventions

.321 Standard inclusions: . . magnetic tape read/write error routines and linkages are automatically generated; printer page-overflow routine is automatically simulated.

.33 Documentation

Subject	Provisions
Source program: / Object program:	analyzed listing of both source program and symbolic intermediate program; listing of object program is produced after assembly.
Storage map:	implied on assembly listing.
Restart point list: . . .	none.
Language errors:	any unrecognized 1401 operation codes are noted on the translation listing; decimal machine-language operand addresses referring to other than the fixed input-output areas are also noted as untranslated.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Pass 1: . . . . loads translator program on tape; writes 1401 SPS source deck on tape.
Pass 2: . . . . determines size of all named fields (instructions or data); writes all named fields on a label tape.
Pass 3: . . . . compares A and B operand addresses to label table; creates symbolic labels for input-output areas; flags (for listing purposes) invalid operand addresses.
Pass 4: . . . . constructs a table of all word marks used; affects operand lengths as necessary.
Pass 5: . . . . translates SPS operation codes; constructs entire B 200/300 symbolic instruction.
Pass 6: . . . . optimizes use of symbolic instructions by combining chained, compare, and editing instructions whenever possible.
Pass 7: . . . . generates standard subroutines according to input-output requirements.

(Contd.)

.42 Optional Mode: . . . . . none provided.

.43 Special Features

.431 Alter to check only: . . no.
.432 Fast unoptimized translate: . . . . no.
.433 Short translate on restricted program: . no.

.44 Bulk Translating: . . . after initial loading of translator card deck on tape, SPS programs can be bulk-translated without reloading the translator.

.45 Program Diagnostics: . . none directly; the translation listing records the original and intermediate instructions, the data constants, and notes to aid post-translation editing.

.46 Translator Library: . . none provided.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space: uses 30% to 60% more core storage than the SPS source program; tailoring of the intermediate symbolic program by the programmer can improve this performance considerably.

.512 Space required for each input-output file: . . . . same as coded in source program.
.513 Approximate expansion of procedures: . 1 to 1 (high core storage demands are caused primarily by B 200/300 Series 12-character fixed instruction length).

.52 Translation Time

.521 Normal translating: . . 0.0125S minutes, where S is number of source program statements.
.522 Checking only: . . . . . . none provided.
.523 Unoptimized translating: . . . . none provided.

.53 Optimizing Data: . . . . when possible, translator combines chained Move instructions, Compare and Branch instructions, carriage tape control, and editing operations into single instructions.

.54 Object Program Performance: . . . . execution speed will generally range from 1 to 4 times as fast as that of original 1401 program, depending upon type of program and speeds of peripheral devices.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . . B 200/300 6-microsecond Central Processor with 4,800 positions of core storage; 3 magnetic tape units of any model; and 1 line printer and card punch of any available models.
.612 Larger configuration advantages: . . . . additional core storage allows translation of larger 1401 programs and use of larger magnetic tape input-output blocks.

.62 Target Computer

.621 Minimum configuration: . . . . any B 100/200/300 Series system with sufficient input-output equipment to make it logically equivalent to the original 1401 system.
.622 Usable extra facilities: . . . . all except paper tape, MICR readers, Disk File, and data communications equipment.

.7 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries:	none.	
Duplicate names:	none.	
Improper format:	check	noted on listing.
Incomplete entries:	none.	
Target computer overflow:	check	noted on listing.
Inconsistent program:	none.	
Invalid operation codes:	check	noted on listing.

OPERATING ENVIRONMENT: GENERAL

.1 GENERAL

.11 Identity: . . . . individual Burroughs service routines, as identified below.

.12 Description

Three groups of routines are provided to assist in general computer operation: input-output control, dumps, and magnetic tape editing.

A straightforward input-output control subroutine is used to attempt several rereads for handling magnetic tape errors. In addition, a magnetic tape edit routine is provided to test for tape flaws.

A variety of dumps are available to print and/or punch the contents of core storage. They may be used as subroutines. There is also a set of trace routines.

.2 PROGRAM LOADING

.21 Source of Programs: . punched cards, punched tape, magnetic tape, or Disk File.

.22 Library Subroutines: . no special provisions.

.23 Loading Sequence: . . . as loaded by operator.

.3 HARDWARE ALLOCATION: . . . . . as incorporated in user's program.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: . as incorporated in user's program.

.42 Multiprogramming: . . . a pre-determined set of small independent routines can be run in an intermingled mode, each able to stop and start independently; see Section 201:192.

.43 Multi-sequencing: . . . none.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Loading input error:	check	stop.
In-out error - single:	check	reread magnetic tape, or stop.
In-out error - persistent:	check	stop.
Overflow:	none.	
Invalid instruction:	none.	
Program conflicts:	not possible.	

.45 Restarts: . . . . as incorporated in user's program.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

Trace routines are available for all B 100/200/300 Series Systems. Each Trace routine is capable of printing or punching the following information for specified instructions: the instruction's location, the instruction itself, comparison indicators, and the contents of two areas of core storage before and after execution. Core storage requirements range from 729 to 823 characters, depending upon the processor model.

.52 Post Mortem

A number of standard dump routines are available to punch and/or print the contents of specified areas of core storage. Printed output can be produced either in full, 120-character lines or as five annotated, 12-character fields per line. Punched-card output can be in either auto-load format or in un-numbered cards. Core storage requirements range from 42 to 384 characters, depending upon the function or pair of functions to be performed.

.6 OPERATOR CONTROL: . . . . as incorporated in user's program.

.7 LOGGING: . . . . manual.

.8 PERFORMANCE

.84 Program Loading Time: . . . . maximum of 6 seconds, using B 124 Card Reader, to load 4,800-character core storage.

OPERATING ENVIRONMENT: MULTIPROCESSING

.1 GENERAL

.11 Identity: . . . . B 200/300 Series Multiple Program Productivity Advisor.
B 200/300 Series Program Schedular.

.12 Description

"Multiprocessing" in B 200/300 Series systems is implemented by two closely related routines: the Multiple Program Productivity Advisor and the Program Schedular.

- Productivity Advisor:

  This program has been designed primarily to serve as an aid in determining the most efficient manner of using the Program Schedular in a given situation. The Productivity Advisor accepts basic data regarding the programs to be run simultaneously and produces a series of tables displaying the productivity which would be realized for each possible combination of priority ratios. Depending upon the particular jobs under consideration, the productivity tables show this information in terms of lines per minute, cards per minute, or records per minute. By reviewing the productivity figures for various ratio combinations and considering the volumes associated with each job, the user can select the ratio that will most efficiently accomplish his purposes. He may then use this information as input to the Program Schedular.

- Program Schedular:

  In many applications of B 200/300 Series systems, the cycle time of the input-output units exceeds the internal processing time, so that a surplus of computing capability is available. The Program Schedular permits users to package multiple programs for processing at the same time, thereby maximizing the use of the central processor. During this packaging operation, a specially-conditioned executive routine, a fully documented program listing, and an auto-load object program deck are prepared. Up to five programs can be packaged together for subsequent multiple processing. Since each program functions independently of all other programs, runs may be combined, started, or stopped whenever the user desires.

Up to five independent and unrelated programs can be run simultaneously. Since all programs mustbe stored in core storage at the same time, the size of each program is severely limited. When the maximum core storage available for B 200/300 Series processors (19,200 characters) is utilized, the Program Schedular concept becomes somewhat more practical than when smaller memory sizes are considered. This multiprocessing approach is designed for programs that are input-output limited and written in a cyclic manner. Because the number of input-output units available per computer system is severely restricted, and because magnetic tape operations are unbuffered, an efficient five-program mix is difficult to achieve in practice. Small data transcription programs appear to be best suited for effective multiprocessing with the Program Schedular.

When it becomes necessary to add, delete, or modify any of the programs being run together, the Program Schedular must be used to prepare a new multi-program package.

.13 Availability: . . . . June, 1963 (date released for general use).

.14 Originator: . . . . Burroughs Corp.

.15 Maintainer: . . . . Burroughs Corp.

.16 First Use: . . . . demonstrated in January, 1963.

.2 PROGRAM LOADING

.21 Source Programs

.211 Programs from on-line libraries: . . . . . none.
.212 Independent programs: up to 5 programs are input to the Program Schedular.
.213 Data: . . . . must be supplied as called for by each of the programs being run together.
.214 Master routines: . . . . executive routine (3 instructions); one routine per program is created by the Program Schedular and included in the multi-program deck.

.22 Library Subroutines: . none.

.23 Loading Sequence: . . . all programs to be run together (maximum of 5) are contained in the multi-program deck. The complete deck is loaded in one operation.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Segmentation: . . . . . . no provisions.

.312 Occupation of working storage: . . . . assigned in scheduling phase of the Program Schedular. Programs must be loaded in relocatable form.

.32 Input-Output Units

.321 Initial assignment: . . . by program.
.322 Alternation: . . . . as indicated by user.
.323 Reassignment: . . . . . by scheduling phase of the Program Schedular (to increase simultaneity).

.4 RUNNING SUPERVISION

.41 Simultaneous Working: implemented in sequencing of programs by Program Schedular. Reassignment of input-output units is also made wherever decided.

.42 Multiprogramming: . . maximum of five programs. Each program is assigned a priority number and status (active or inactive) by the programmer. During actual operation the operator can change the priority or status of a run.

.43 Multi-sequencing: . . . none.

.44 Errors, Checks, and Action: . . . . the following checks for errors are made during the editing phase of the Program Schedular routine. No checks are made during object program execution time.

Error	Check or Interlock	Action
Loading input error:	none.	
Allocation impossible:	check	print message.
Storage overflow:	check	print message and halt.
In-out error — single:	check	either restart or continue, depending on circumstances.
Invalid instructions:	check	print message.
Program conflicts:	check	print message.
Arithmetic overflow:	none.	
Invalid operation:	check	print message.
Improper format:	check	print message.
Invalid address:	check	print message.

.45 Restarts: . . . . none.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . none.
.512 Snapshots: . . . . none.
.52 Post Mortem: . . . . . . none.

.6 OPERATOR CONTROL: . . . . . . as incorporated into user's individual routines.

.7 LOGGING: . . . . as incorporated into user's individual routines.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . . central processor plus those input and output devices required by individual programs.

.812 Usable extra facilities: . . . . larger core storage.
1 or 2 card readers.
card punch.
1 or 2 line printers.
magnetic tape (1 to 6 units).
1 or 2 paper tape readers.
paper tape punch.

.813 Reserved equipment: . all of core storage is available; "executive routine" consists of only 3 instructions per program.

.82 System Overhead

.822 Reloading frequency: for each new set of routines to be run, the Multiple Program Productivity Advisor and Program Schedular routines must be run, and the resulting program deck loaded.
For a multi-program deck, that is already prepared, reloading must take place each time a routine in the deck is to be run.

.83 Program Space Available: . . . . all of core storage except for "executive routine" requirements of 3 instructions per program.

.84 Program Loading Time: . . . . maximum of 6 seconds, using B 124 Card Reader, to load 4,800-character core storage.

.85 Program Performance: . . . . . generally as predicted by the Productivity Advisor (Paragraph .12), unless central processor time becomes the limiting factor for a particular combination of programs.

OPERATING ENVIRONMENT: TAPE/DISK OPERATING SYSTEM

.1 GENERAL

.11 Identity: . . . . B 200 Tape/Disk Operating System.

.12 Description

The B 200 Tape/Disk Operating System is a Control System designed to operate with magnetic tape or Disk File subsystems. One of four executive routines contained within the Operating System is in core storage at all times. The four executive routines are:

- Tape Executive Routine - controls all processing and program segmentation by calling in control routines, utility programs, system functions, user programs, and overlays from a magnetic tape source.
- Disk File Executive Routine - controls all processing and program segmentation by accessing a Disk File to bring in control routines, utility programs, system functions, user programs, and overlays.
- Multiprocessing Control - controls all user programs of a relatively-addressed nature by means of a cycle-time clocking scheme designed to make effective use of peripheral equipment. Core memory is allocated according to a predetermined priority code and memory-availability scheme. Multiprocessing Control is provided for use with Disk File systems only.
- Program Debugging Control - provides formatted output of memory dumps, trace points, control state running, and file dumps as directed by specification cards. Program Debugging Control is available for use with either magnetic tape or Disk File Systems.

.13 Availability

Tape Executive Routine: June, 1965.
Disk File Executive Routine: . . . . June, 1965.
Multiprocessing Control: July, 1965.
Program Debugging Control: . . . . July, 1965.

.14 Originator: . . . . . . Burroughs Corp.

.15 Maintainer: . . . . . . Burroughs Corp.

.16 First Use: . . . . Bankers Data Processing, Boston, Mass. July, 1965.

.2 PROGRAM LOADING

.21 Source of Programs: . all programs of a checked-out nature can be added to a Program Add Tape. The Permanent User Program Library, including all error routines and special situation subroutines, can be maintained on either the Program Add tape or on the Disk File. Programs can contain absolute or relative addresses and input-output unit numbers.

.211 Programs from on-line libraries . . . . Disk File or magnetic tape.
.212 Independent programs: . . . . can be called in from punched cards, paper tape, or disk file.
.213 Data: . . . . as required by users' programs.
.214 Master routines: . . . either the Tape Executive or Disk File Executive Routine is loaded into 480 character positions of core storage by means of a Tape Start or Disk Start Card. Any executive routine can then call in any other executive routine.

.22 Library Subroutines: . called in from User Program Library, Operating System Library, or as loaded from some peripheral source.

.23 Loading Sequence: . . sequential loading of programs as provided by operator on User Program Library tape or on card reader. The system operator can interrupt this sequence by calling in specific programs through the Supervisory Printer. Stored programs can also call in other predetermined programs.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . . programs are assembled in a single-instruction format adaptable to relative addressing and relative unit assignment by the Executive Routine.

.312 Occupation of working storage: . . . . once programs are allocated to a portion of core storage, they are not disturbed except by operator request. If the interruption calls for a high priority program change, the original program is stored on tape or disk in a "saved" state.

32 Input-Output Units

.321 Initial assignment: . . performed by the Multiprocessing Control based upon program need and available equipment.
.322 Alternation: . . . . . . not provided.
.323 Reassignment: . . . . . provided by re-calling the Program with input-output configuration specified differently.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: the programs in the mix will be allocated their required input and output units as available at load time by a system test of the configuration available and the priority rating assignment. The degree of simultaneous working of input-output units depends exclusively on the amount of skill with which the source program was written.

.42 Multiprogramming: . . the number of programs in the mix is arbitrarily set at a maximum of three, with five more permitted in a call-in stack. The normal program processing cycle-time, stored as a notation with the program call record, determines the individual program time allotment. A call for change of priority can alter, suspend, or replace programs that are currently in process or still in the program stack.

.43 Multi-sequencing: . . . not provided.

.44 Errors, Checks, and Action (See table below.)

.45 Restarts: . . . . handled by the executive routine when possible, or by user-written utility or maintenance programs.

.451 Establishing restart points: . . . . dependent upon individual user programs.

.452 Restarting process: . automatic system recovery brings the End-of-Job Function into memory. Individual user programs must provide for restarts if required.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Loading input error:	system check	message to the operator.
Allocation impossible:	system check	delay processing of the program until allocation becomes possible.
Input-output errors:	system and I/O equipment checks	all errors detected during control state initiate automatic retries where possible.
Storage overflow:	user program check	system assumes a program added to the User Library is tested and does not exceed available core storage.
Invalid instructions	hardware	hardware can allow execution of some properly-formatted invalid instructions; in some cases the hardware will cause an alarm and stop when an invalid instruction is detected.
Improper format:	none.	
Invalid address:	none.	
Reference to forbidden area:	none.	

(Contd.)

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . Program Debugging Control executive routine allows trace points to be set by memory location, instruction type, control points, or change of control points.

.512 Snapshots: . . . . specifications are entered as each program is loaded. Dumps of any nature can be called in under Program Debugging Control. Under any executive routine's control, a dump can be executed by operator interrupt.

.52 Post Mortem: . . . . . printer or tape dumps, as well as storage dumps, can be executed by means of an operator function call.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . typed message on the Supervisory Printer.

.612 Action required by operator: . . . . typed message.

.613 Reporting progress of run: . . . . typed message.

.62 Operator's Decisions: keyboard entry.

.63 Operator's Signals:

.631 Inquiry: . . . . keyboard entry.

.632 Change of normal progress: . . . . keyboard, card, or paper tape entry to alter priorities or specified input-output configurations.

.7 LOGGING

.71 Operator Signals: . . . typed record of keyboard entry.

.72 Operator Decisions: . typed record of keyboard entry.

.73 Run Progress: . . . . . typed messages.

.74 Errors: . . . . typed messages.

.75 Running Times: . . . . typed messages indicate end-of-job conditions. Operator can then type any desired supplements.

.76 Multiprogramming Status: . . . . keyboard inquiry of program status results in a report on the Supervisory Printer of status of current program and those remaining in the call-in stack.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . .
B 273 or B 283 Central Processor with 9,600 characters of core storage.
B 495 Supervisory Printer.
Card or paper tape reader (any model).
Line printer (any model).
3 magnetic tape units, or 2 magnetic tape units and 1 Disk File (any model tape units).

.812 Usable extra facilities: . . . . any available keyboard card, paper tape, and magnetic tape devices will increase the number and variety of programs permitted in the "multiprocessing" mix.

.813 Reserved Equipment: 1 magnetic tape unit or a user-designated portion of Disk File storage, the size of which will be determined by the size of the User's Permanent Program Library and desired Disk File Controls, and 480 characters of core storage.

.82 System Overhead

.821 Loading time: . . . . . programs and Operating System controls are transferred from magnetic tape to core storage at up to 66KC in binary mode, and from Disk File to core storage at 100KC.

.83 Program Space Available: . . . . all but 480 characters of core storage, and all available Disk File storage except the portion that is reserved according to the number of functions included within the Disk File Control.

.84 Program Loading Time

From cards: . . . . . . 200, 475, 800, or 1400 cards per minute, depending upon card reader model.

From magnetic tape:. varies with tape unit speed and position of user program on the tape.

From Disk File:. . . . 100 KC transfer rate.

.85 Program Performance: . . . . during each program cycle, less than 1 millisecond will be required for control purposes in most cases; if a specific system function is called for, Multiprocessing Control is not available.

SYSTEM PERFORMANCE

Generalized File Processing (201:201.100)

These are a series of typical commercial data processing applications that involve the processing of a detail file against a master file. The detail file contains data used to update the master file by inserting new records, deleting old records, and recording changes to records in the file. A printed record of each transaction is produced. This type of processing occurs, for example, in a payroll routine in which the master file is the payroll file, the detail file contains the data from the periodic time sheets, and the output is largely in the form of paychecks.

The Standard File Problems are fully described in the Users' Guide, Section 4:200.11, and the Standard Configurations used as a basis for measuring the performance of B 100/200/300 Series Systems are shown in Section 201:031 of this report. The master files in Standard Configuration I are on punched cards; in Configurations II and III, the master files are on magnetic tape. All configurations use the card reader for input of the detail file and the printer for output of the report file.

In Standard File Problems A, B, C, and D, the controlling factor for Configuration I is card punching time. For Configurations II and III, the sum of central processor computational time and tape time (which cannot be overlapped) is the controlling factor under most conditions; at high activity ratios, however, the total processing time is controlled by the printer speed.

Sorting (201:201.200)

Times are presented for sorting 80-character records on magnetic tape. These times are estimated both by the standard procedures described in the Users' Guide, Section 4:200.21, and for routines produced by the manufacturer's Tape Sort Generator I.

WORKSHEET DATA TABLE 1									
	ITEM		CONFIGURATION						REFERENCE
			I		II		III		
1 Input-Output Times	Char/block	(File 1)	80		1,080		1,080		4:200.112
	Records/block	K (File 1)	0.5		10		10		
	msec/block	File 1 = File 2	75 (File 1); 200 (File 2)		55.0		35.4		
		File 3	75		126		126		
		File 4	111		158		158		
	msec/switch	File 1 = File 2	0		0		0		
		File 3	0		0		0		
		File 4	0		0		0		
	msec penalty	File 1 = File 2	1.0 (File 1); 1.2 (File 2)		50.0		28.3		
		File 3	1.0		1.0		1.0		
		File 4	0.8		0.8		0.8		
2 Central Processor Times	msec/block	a_1	2.7		2.7		2.7		4:200.1132
	msec/record	a_2	3.1		3.1		3.1		
	msec/detail	b6							
	msec/work	b5 + b9	38.8		38.8		38.8		
	msec/report	b7 + b8							
3 Standard File Problem A F = 1.0	msec/block for C.P. and dominant column.		C.P.	Punch	C.P.	Printer	C.P.	Printer	4:200.114
		a_1	2.7		2.7		2.7		
		a_2 K	1.6		31.0		31.0		
		a_3 K	19.4		388.0		388.0		
		File 1: Master In	1.0		50.0		28.3		
		File 2: Master Out	1.2	200	50.0		28.3		
		File 3: Details	0.5		10.0		10.0		
		File 4: Reports	0.4		8.0	1,580	8.0	1,580	
		Total	26.8	200	539.7	1,580	496.3	1,580	
4 Standard File Problem A Space	Unit of measure	(character)							4:200.1151
		Std. routines	232		520		520		
		Fixed	100		100		100		
		3 (Blocks 1 to 23)	360		360		360		
		6 (Block 24 to 48)	2,808		2,808		2,808		
		Files	520		2,360		2,360		
		Working	0		108		108		
		Total	4,020		6,256		6,256		

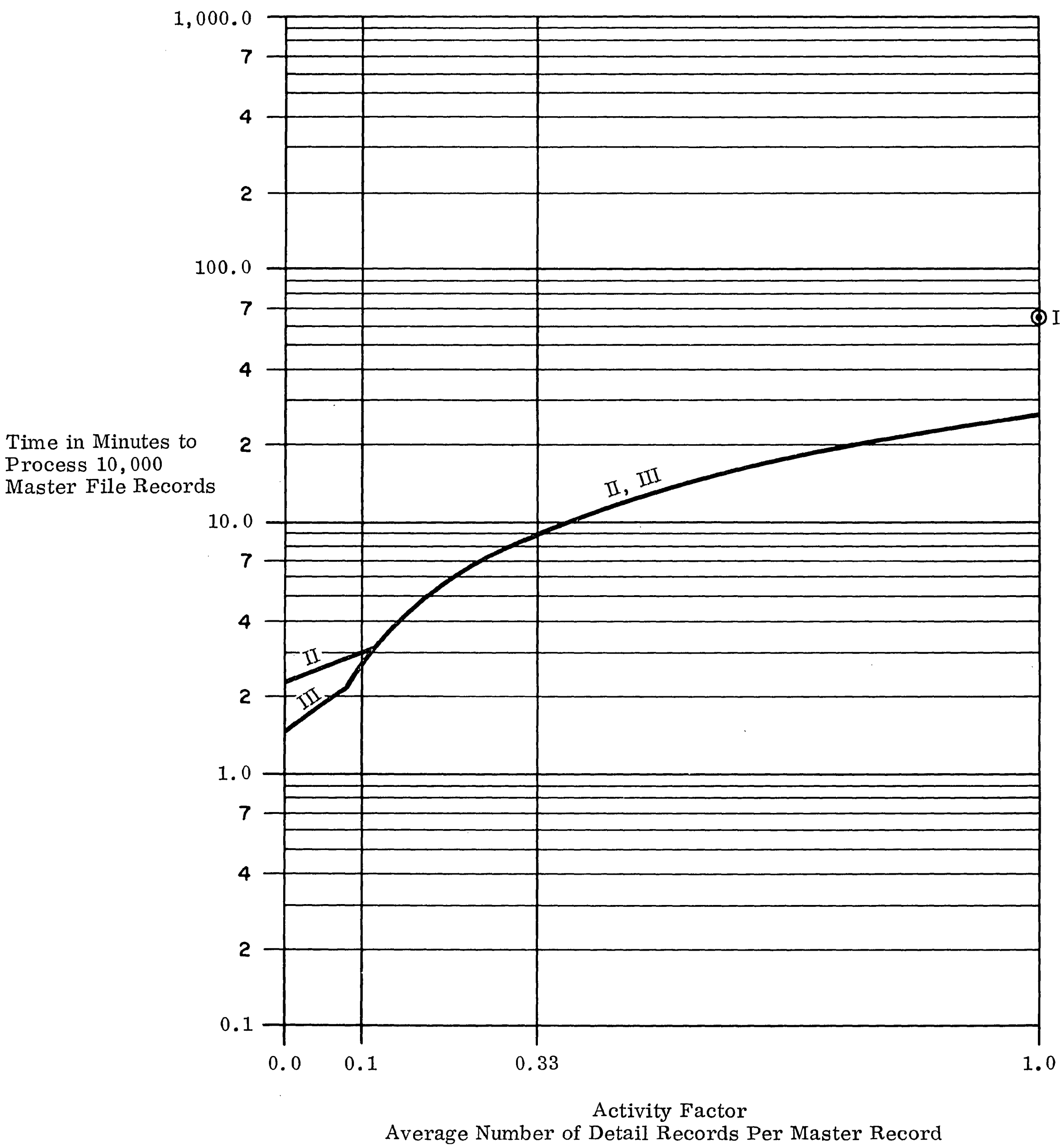
(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes—
Master file: . . . . . . 108 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.112 Computation: . . . . standard.
.113 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.
.114 Graph: . . . . see graph below.
.115 Storage space required—
Configuration I: . . . . 4,020 characters.
Configuration II: . . . . 6,256 characters.
Configuration III: . . . 6,256 characters.

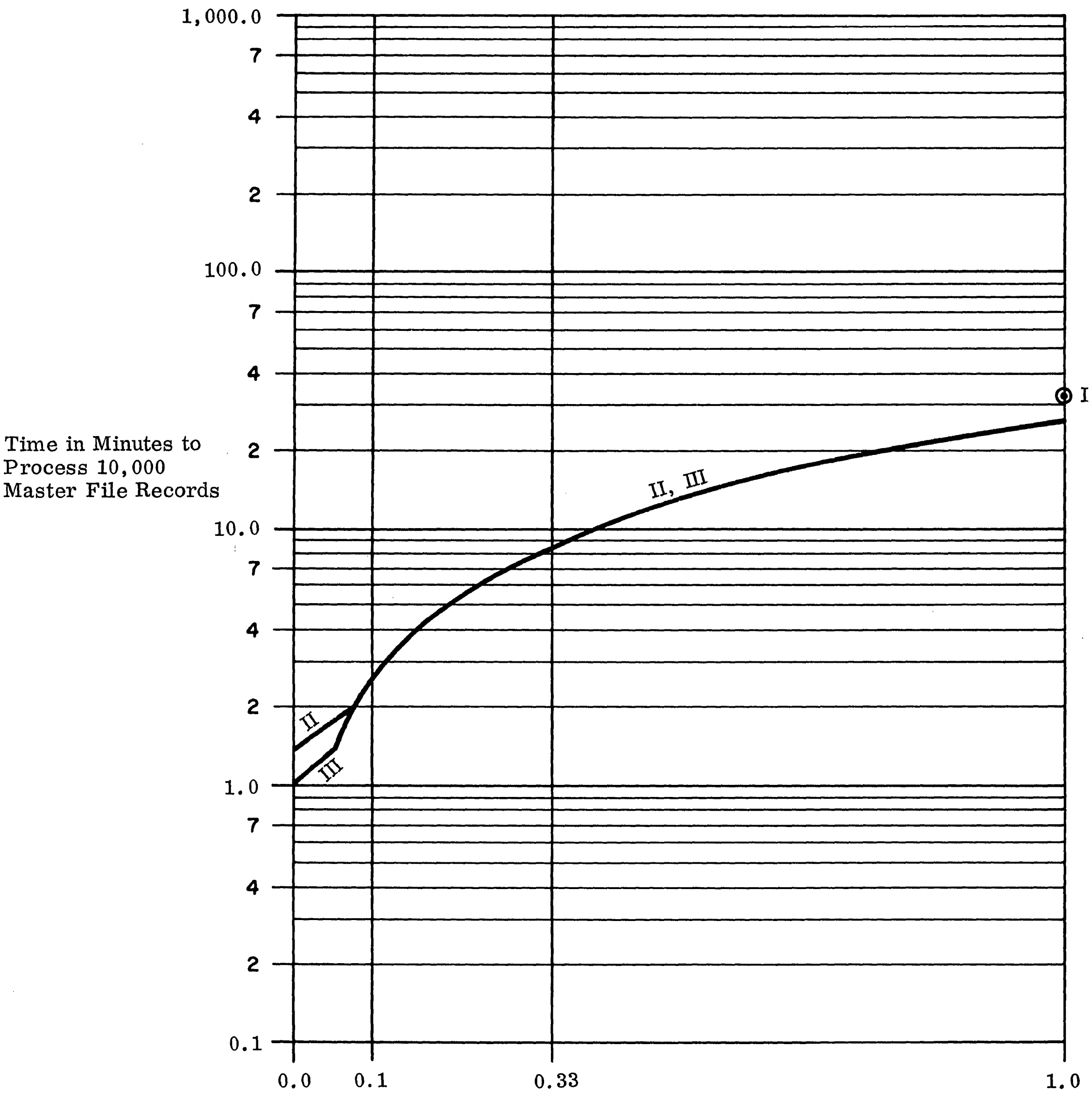


(Roman numerals denote standard System Configurations.)

.12 Standard File Problem B

.121 Record Sizes —
Master file: . . . . . . 54 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.122 Computation: . . . . standard.
.123 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

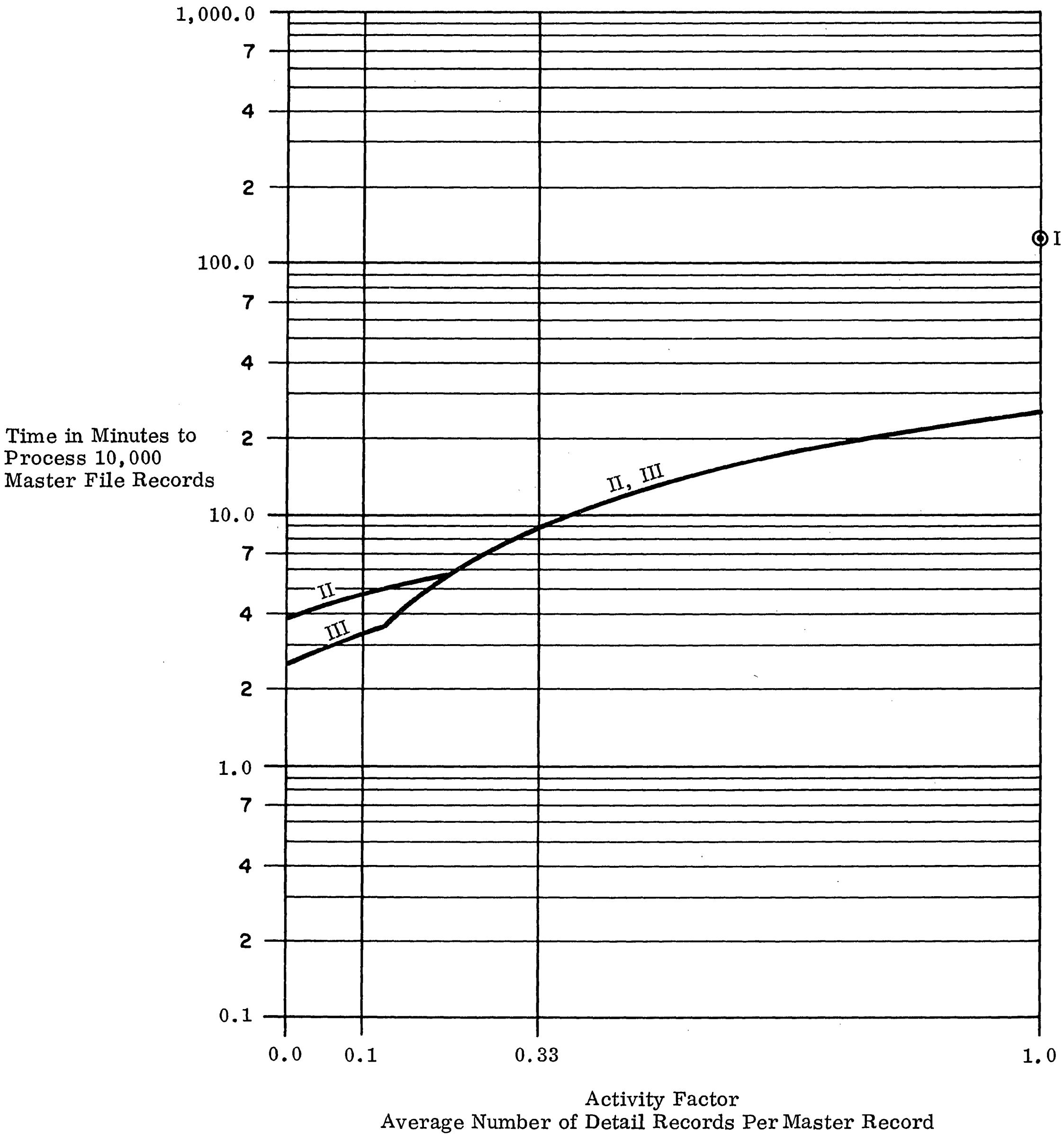
(Roman numerals denote standard System Configurations.)

(Contd.)

.13 Standard File Problem C

.131 Record Sizes —
Master file: . . . . . . 216 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.132 Computation: . . . . standard.
.133 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . see graph below.

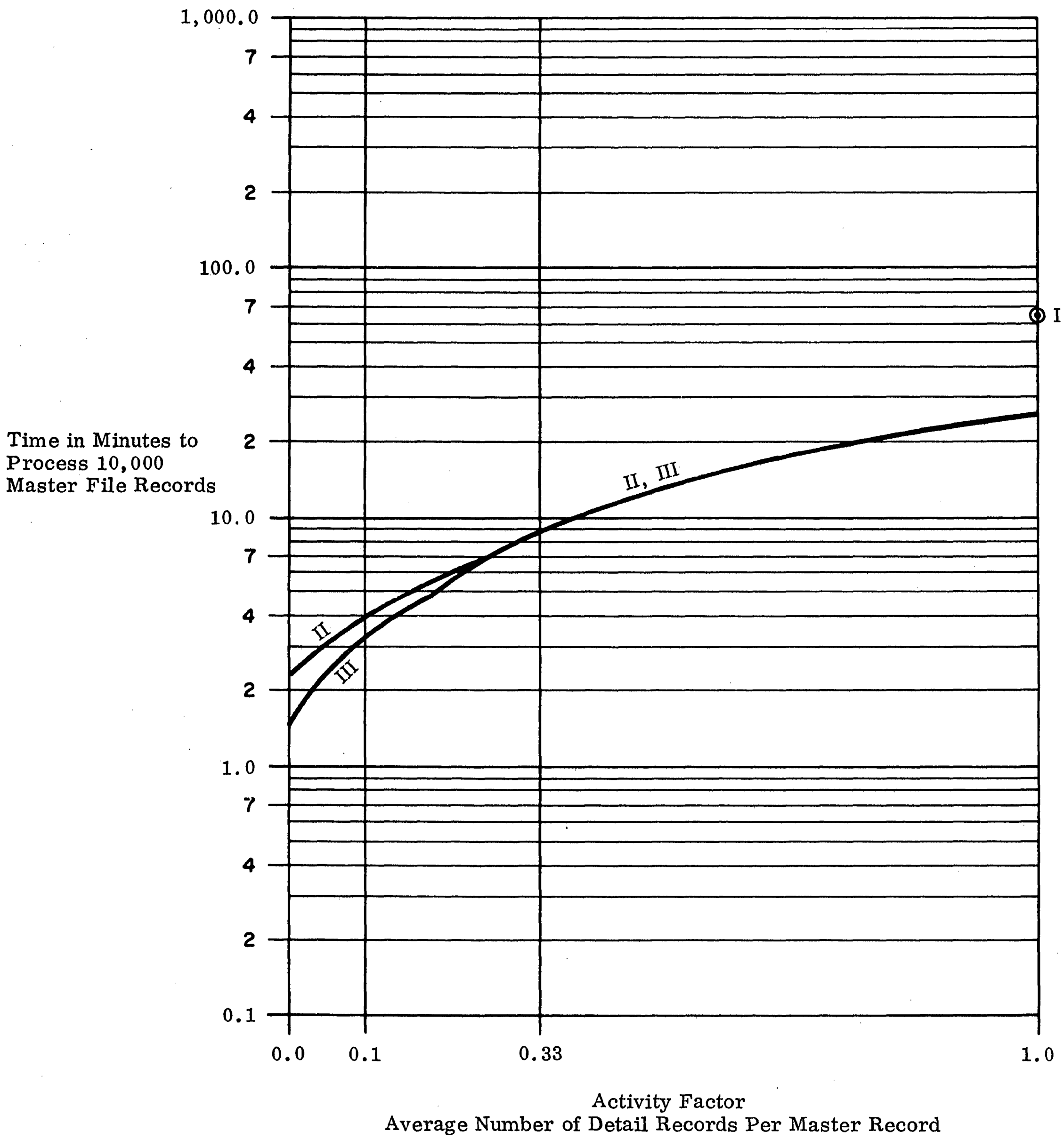


(Roman numerals denote standard System Configurations.)

.14 Standard File Problem D

.141 Record Sizes —
Master file: . . . . . . 108 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.142 Computation: . . . . trebled.
.143 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

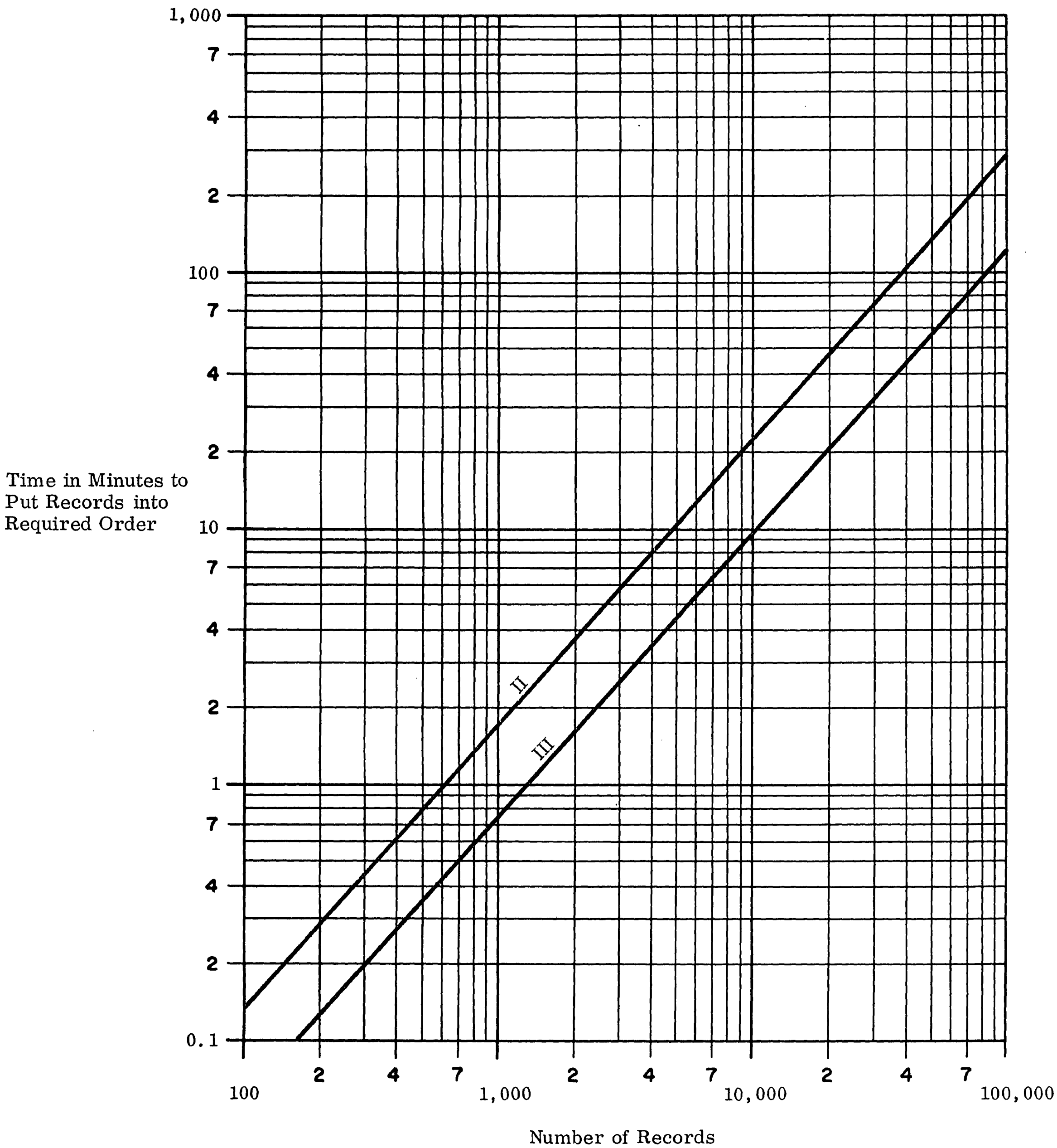
(Contd.)

AUERBACH

.2 SORTING

.21 Standard Problem Estimate

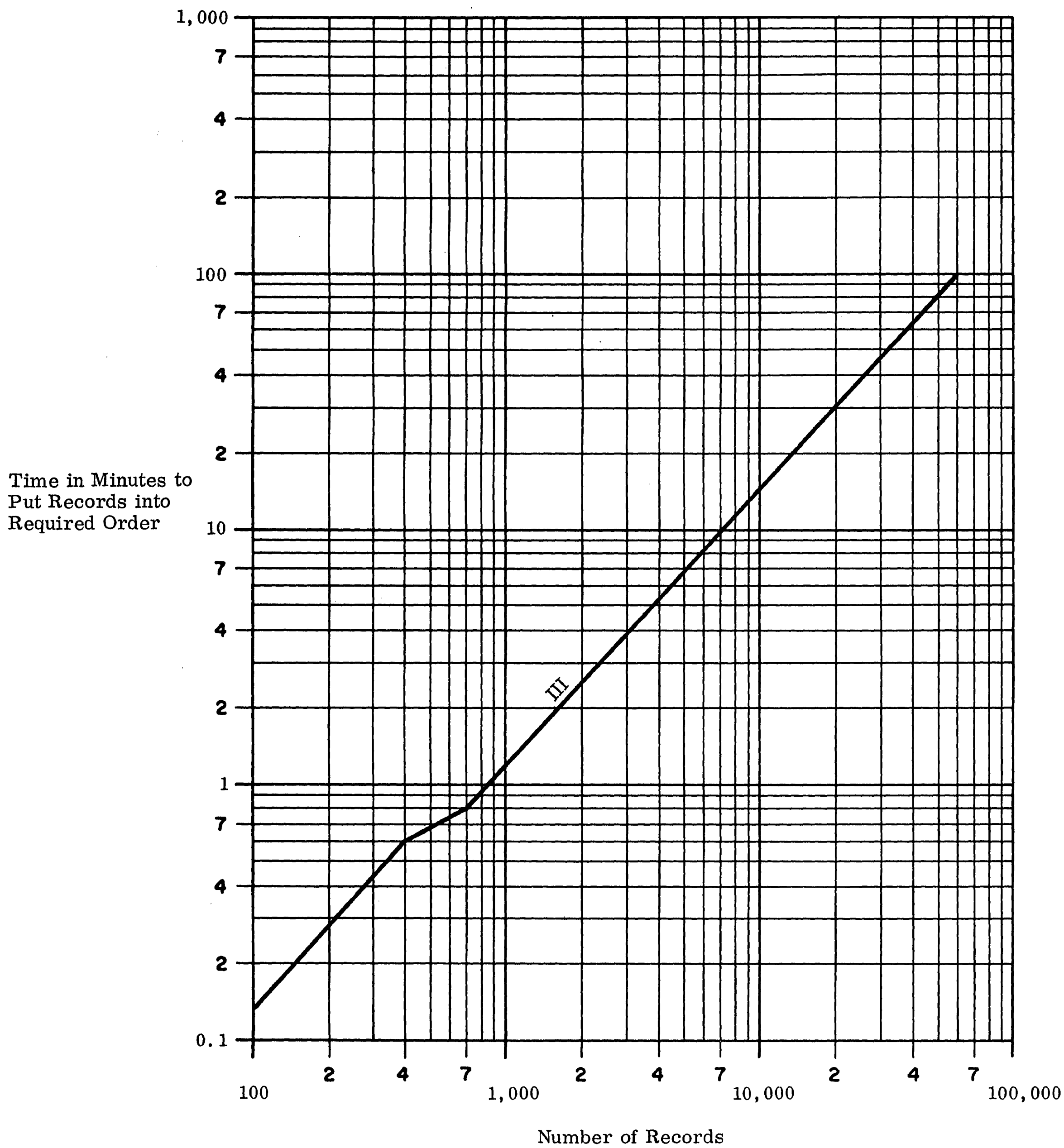
.211 Record size: . . . . 80 characters.
.212 Key size: . . . . 8 characters.
.213 Timing basis: . . . . . . as in Paragraph 4:200.213, using 2-way merge for Standard Configuration II and 3-way merge for Configuration III.
.214 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

.22 Tape Sort Generator

.221 Record size: . . . . 80 characters.
.222 Key size: . . . . 8 characters.
.223 Timing basis: . . . . . . times supplied by Burroughs Corporation.
.224 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

PHYSICAL CHARACTERISTICS

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
Central Processor (all models)	29	66	55	1,200	0.7	2,000
B 122 Card Reader	29	17	41	102	0.20	700
Card Reader (all other models)	48	29	50	920	1.3	3,000
B 303 Card Punch	44	28	53	655	1.4	4,000
B 304 Card Punch	73	27	47	1,283	2.2	5,500
Line Printer (all models)	74	29	55	1,738	2.3 idle 3.5 printing	4,480
B 333 Multiple Tape Lister	40	29	55	800	1.7	1,740
Multiple Tape Lister (all other models)	74	29	55	1,750	2.3 idle 3.5 printing	4,480
Magnetic Tape Unit (all models)	29	28	74	900	2.05/ 3.35	7,200
B 116 Sorter-Reader	180	35	58	3,800	9.6	24,000
Sorter-Reader (all other models)	144	35	58	3,580	8.0	22,000
Paper Tape Reader	30	24	60	437	0.91	3,100
Paper Tape Punch	30	24	60	426	0.59	1,500
Supervisory Printer	22	22	50	200	0.3	negligible
Record Processor	63	116	65	2,800	4.5	12,000
Teletype Terminal	24	38	42	500	0.23	800
Typewriter Terminal	24	38	42	500	0.23	800
Typewriter Inquiry Station	18	20	40	60	0.26	800
Dial TWX Terminal	24	38	42	500	0.23	800
Central Terminal	24	44	43	525	0.4	1,000
Basic Disk File/Data Communication Control Unit	32	46	73	1,000	1.5	5,000
Disk File Storage Module	22	46	53	3,800	1.46	3,800
Disk File Electronics Unit	45	46	53	450	1.1	4,100

General Requirements

Temperature: . . . . between 66° and 80°F.
Relative humidity: . . . . between 30% and 65%.
Power:. . . . . 115/230-volt, 1-phase, 60-cycle, 3-wire; or 120/208-volt, 1-phase, 60-cycle, 3-wire.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	*	Monthly Rental $	Monthly Maintenance $**	Purchase $
CENTRAL PROCESSORS	B 160	Card Processor		1,030	105.00	67,500
	B 170	MICR/Tape Processor		1,340	110.00	74,250
	B 180	Tape Processor		1,195	105.00	71,325
	B 250	MICR/Ledger Processor		1,650	110.00	56,100
	B 251	VRC System (includes B 102, B 122, and B 104)		4,400	1,175.00	175,000
	B 260	Card Processor		1,500	105.00	67,500
	B 270	MICR/Tape Processor		1,650	115.00	74,250
	B 280	Tape Processor		1,585	110.00	71,325
	B 263	Card Processor		1,600	110.00	72,000
	B 273	MICR/Tape/Disk File Processor		1,850	125.00	83,250
	B 275	MICR Processor		1,665	115.00	74,925
	B 283	Tape/Disk File Processor		1,785	115.00	80,325
	B 300	Basic Processor		1,645	110.00	74,025
		(Note: Each Central Processor includes 4,800 character positions of core storage.)				
CORE STORAGE MODULES		Additional 4,800 characters	450	550	20.00	24,750
		Additional 9,600 characters	450	325	10.00	14,625
CENTRAL PROCESSOR OPTIONAL COMMANDS		Transfer and Branch	50	25	—	1,250
		16-Pocket Sorter-Reader Control	50	30	—	1,350
		Selective Stacking (B 304 Card Punch only)	50	15	—	675
		(Note: above options are available with B 200/300 6-μsec Processors.)				
		Transfer and Translate	50	25	—	1,125
		Unit Interrogate	50	65	—	3,325
		Data Compress and Expand	50	50	—	2,250
		Binary Card Read/Punch	50	100	—	4,500
		B 332 Lister Control	50	25	—	1,125
		(Note: above commands are available with B 300 Processor only.)				
CENTRAL PROCESSOR OPTIONAL FEATURES		132-Printer-Position Capability	250	40	—	1,800
		Card Reader Busy Branch	95	45	—	1,800
		Printer/Lister Selector	85	40	5.00	1,610
		Card Reader Early Release	50	15	—	675
		66KC Magnetic Tape Control	50	50	5.00	2,250
		72KC Magnetic Tape Control	50	50	5.00	2,250
		Sense Switches	50	15	5.00	675

* One-time charge applicable when certain units are added to an existing system installation.
** Maintenance charges are slightly higher in rural areas.

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	*	Monthly Rental $	Monthly Maintenance $**	Purchase $
CENTRAL PROCESSOR OPTIONAL FEATURES (Continued)		(Note: see System Configuration chart, page 201:031.001, for feature applicability.)				
INPUT-OUTPUT CONTROL MODULES		MICR Sorter-Reader	85	65	10.00	2,925
		Paper Tape	85	120	10.00	5,400
		MICR Sorter/Paper Tape	130	185	10.00	8,325
		Supervisory Printer	50	15	—	675
		Magnetic Tape	85	155	10.00	6,975
		Disk File	130	15	—	675
		Data Communications	50	15	—	675
		(Note: B 300 Series requires one module for each class of input-output device used; B 200 Series requires the modules only for extra input-output devices attached in the field.)				
INPUT-OUTPUT		MICR Sorter-Readers				
	B 101	13-Pocket Non-System (1560 dpm)		1,890	465.00	85,050
	B 102	13-Pocket With Standby (1560 dpm)		2,000	500.00	90,000
	B 103	13-Pocket With Endorser Capability (1560 dpm)		2,000	500.00	90,000
	B 104	13-Pocket Without Standby (1560 dpm)		1,900	500.00	85,500
	B 106	13-Pocket With Standby (1200 dpm)		1,800	500.00	90,000
	B 107	13-Pocket With Endorser (1200 dpm)		2,000	550.00	99,000
	B 116	16-Pocket With Endorser Capability (1560 dpm)		2,300	615.00	103,500
		Endorser (B 103 and B 116 only)	1,080	200	50.00	9,000
		Readers and Punches				
	B 122	Card Reader (200 cpm)		220	40.00	9,900
	B 123	Card Reader (475 cpm)		320	70.00	18,000
	B 124	Card Reader (800 cpm)		400	75.00	18,000
	B 129	Card Reader (1,400 cpm)		600	115.00	27,000
		Postal Money Order Option	145	20	—	800
	B 303	Card Punch (100 cpm)		450	65.00	20,250
	B 304	Card Punch (300 cpm)		650	115.00	29,250
	B 141	Paper Tape Reader (500-1000 char/sec)		400	70.00	18,000
		Input Code Translator	50	180	10.00	8,100
		Card Reader/Paper Tape Reader Selector Switch	50	15	—	675
	B 341	Paper Tape Punch (100 char/sec)		190	40.00	8,550
		Output Code Translator	50	170	10.00	7,650
		Card Punch/Paper Tape Punch Selector Switch	50	15	—	675

* One-time charge applicable when certain units are added to an existing system installation.
** Maintenance charges are slightly higher in rural areas.

(Contd.)

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	*	Monthly Rental $	Monthly Maintenance $**	Purchase $
INPUT-OUTPUT (Continued)		Printers and Listers				
	B 320	Line Printer (475 lpm; 120 p.p.)		810	170.00	54,000
	B 321	Line Printer (700 lpm; 120 p.p.)		1,200	175.00	54,000
	B 325	Line Printer (700 lpm; 132 p.p.)		1,275	185.00	57,375
	B 328	Line Printer (1040 lpm; 120 p.p.)		1,325	195.00	59,600
	B 329	Line Printer (1040 lpm; 132 p.p.)		1,400	205.00	63,000
		Dual Printer Control	85	200	10.00	9,000
	B 322	Multiple Tape Lister (1600 lpm) —				
		First		1,600	290.00	72,000
		Additional		1,200	245.00	72,000
	B 323	Multiple Tape Lister (1600 lpm) —				
		First		1,700	310.00	76,500
		Additional		1,300	260.00	76,500
	B 326	Multiple Tape Lister (1250 lpm)		1,290	290.00	72,000
	B 332	Master Multiple Tape Lister (1600 lpm)		1,800	325.00	81,000
	B 333	Slave Multiple Tape Lister (1600 lpm)		750	200.00	33,750
		Simultaneous Tape Skipping (B 322 only)	240	10	—	400
		Magnetic Tape Units				
	B 421	Magnetic Tape Unit (18/50KC at 90 ips)		700	145.00	31,500
	B 422	Magnetic Tape Unit (24/66KC at 120 ips)		800	155.00	36,000
	B 423	Magnetic Tape Unit (24KC at 120 ips)		495	145.00	31,500
	B 424	Magnetic Tape Unit (66KC at 83 ips)		850	165.00	38,250
	B 425	Magnetic Tape Unit (18/50/72KC at 90 ips)		850	165.00	38,250
		Typewriter				
	B 495	Supervisory Printer		300	35.00	13,500
		Record Processor				
	B 401	Ledger Processor and Printer		1,150	540.00	63,100
		Optical Reader	50	83	25.00	3,475
		Data Communications				
	B 481	Teletype Terminal -				
		120-char buffer		460	55.00	20,700
		240-char buffer		480	55.00	21,600
	B 483	Typewriter Terminal		660	75.00	29,700
	B 493	Typewriter Inquiry Station		55	10.00	2,475
	B 484	Dial TWX Terminal		700	80.00	31,500
	B 486	Central Terminal		1,095	100.00	49,275
AUXILIARY STORAGE		Disk File				
	B 471	Electronics Unit		710	80.00	31,950
	B 475	Storage Module		990	115.00	44,550

* One-time charge applicable when certain units are added to an existing system installation.
** Maintenance charges are slightly higher in rural areas.

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	*	Monthly Rental $	Monthly Maintenance $**	Purchase $
CONTROL-LERS	B 450	Basic Disk File/Data Communication Control		330	40.00	14,900
	B 247	Disk File Control		400	45.00	18,000
	B 248	Data Communication Control		340	45.00	15,300
	B 451	Disk File Expanded Control		200	25.00	9,000
B 100 SERIES ADAPTERS		B 160 Adapter to use B 124		235	—	—
		B 170 Adapter to use B 124		150	—	—
		B 180 Adapter to use B 124		195	—	—
		B 160 Adapter to use B 321		235	—	—
		B 170 Adapter to use B 321		150	—	—
		B 180 Adapter to use B 321		195	—	—
		B 170 Adapter to use B 102, B 103, and B 104		150	—	—
		B 170 Adapter to use B 322		150	—	—

* One-time charge applicable when certain units are added to an existing system installation.
** Maintenance charges are slightly higher in rural areas.

BURROUGHS B 5500

Burroughs Corporation

AUERBACH

STANDARD EDP REPORTS

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CONTENTS

INTRODUCTION

.1 SUMMARY

The Burroughs B 5500 Information Processing System is a medium-scale computer system that is suitable for both scientific and commercial data processing. Flexibility in the choice of system configurations results in monthly rentals that range from $16,700 to $160,000. Typical B 5500 systems, however, fall within the $20,000 to $35,000 rental range.

The B 5500 system is an upgraded, improved version of the highly unconventional and imaginative B 5000 system, which was first delivered in March, 1963. Burroughs announced the B 5500 in October, 1964, as a replacement for all B 5000 systems in the field at that time, and dropped the B 5000, as such, from its product line. In most cases, field modifications permitted on-site conversion of the installed B 5000's to B 5500's.

Changes in hardware have centered principally on the central processor. The processor read access time has been reduced from 6 to 4 microseconds, the execution time of many instructions has been improved, and several new and powerful operators have been added to the repertoire. Software changes included a reworked version of the Drum Master Control Program — designed to take full advantage of the expanded instruction list — and a new Master Control Program that is oriented toward the use of Burroughs' high-performance Disk File. In addition, the COBOL and ALGOL compilers were refurbished to provide improved compilation times and greater efficiency in the generation of machine-language instructions.

It should be noted that the B 5500 is basically a more efficient and, therefore, more productive version of the B 5000; but the B 5500 system retains all the design characteristics that made the B 5000 appear so unconventional when it was announced in 1961. Primary emphasis is still placed on the exclusive use of process-oriented languages (ALGOL, COBOL, and FORTRAN) for coding all user programs. Because of this emphasis, Burroughs has developed hardware and software that is oriented toward fast and efficient compilation, with the hope that no user will feel the need for any machine-oriented languages. The B 5500 also features the capability that has come to be called multiprogramming — the ability to execute more than one independent program concurrently on the same computer system. Both the B 5500's hardware and its Master Control Program (MCP) have been designed specifically to facilitate the support of efficient multiprogramming. Benefitting from several years of experience in this area, Burroughs does not hesitate to market the B 5500 primarily on the basis of its ability to process more than one program simultaneously, leading in most cases to increased job throughput.

Some of the unusual hardware facilities that have been incorporated to help achieve the B 5500's design objectives can be summarized as follows:

- Automatic temporary storage for operands and subroutine parameters is provided by a "stack", which operates on the "last-in, first-out" principle.
- Internal operations can be performed in either the Word Mode, upon 48-bit binary operands, or in the Character Mode, upon strings of 6-bit alphameric characters.
- A common representation is used for integers and floating-point numbers.
- Recursive use of subroutines is largely automatic and unrestricted.
- All machine-language addressing is relative and/or indirect, facilitating program segmentation and relocation.
- The same two registers are used for both indexing and arithmetic operations; no index registers of the usual type are provided.

.1 SUMMARY (Contd.)

- There is effective (but not infallible) storage protection against coding errors, invalid data, and inter-program interference.
- Comprehensive interrupt facilities are provided to detect and service special conditions arising anywhere in the system.
- Each of up to 8 core storage modules can accept or transmit data independently of the other core modules and of the processor.
- Magnetic drums and/or disc files provide rapid-access auxiliary storage for the operating system, compilers, program segments, and data arrays.
- All input-output operations are controlled by independent Input/Output Channels; up to four channels can be connected, and any channel can reference any one of up to 39 peripheral devices in a system.
- A second, virtually independent central processor can be added to any B 5500 system; the two processors share all storage and input-output facilities.

.2 CENTRAL PROCESSOR

The B 5281 Processor of the B 5500 Information Processing System is the control center of a unique arrangement of memory and input-output control units, arithmetic units, and interrupt networks. All internal operations can be performed in either the Word Mode, using 48-bit binary words as operands, or in the Character Mode, using variable-length alphameric fields packed eight characters to the word. In the Word Mode, the central processor can perform fixed-point or floating-point arithmetic operations upon single or double word-length binary operands. A variety of logical and comparison operations is also provided in this mode. The Character Mode is designed mainly for data manipulation operations such as editing and scanning. Many processor functions, including addition, subtraction, branching, and table lookups, can be performed in either mode.

A program word consists of four 12-bit "syllables", and each syllable can specify an operation, a relative address, or a literal to be placed in the stack. The Program Reference Table is a relocatable table containing single data items and 48-bit "descriptors," which are used for supplementary control and indirect addressing of data arrays, input-output areas, and program segments. The "stack" consists of the two arithmetic registers (A and B) in the central processor and a relocatable area of core storage; it provides automatic temporary storage of the "last-in, first-out" type for a list of operands and control words. In a multiprogramming environment, each program has its own stack and its own Program Reference Table. Whenever an interrupt occurs during the execution of one program, the contents of the A and B registers and all necessary control information are automatically pushed down into the appropriate stack in core storage; then the Processor transfers control to the Master Control Program, which initiates the processing of the next available program.

Operands in the Word Mode are considered to be 48-bit binary words. The integer part of an operand is represented by 39 bits plus sign, and the octal exponent by 6 bits plus sign. Since the fixed-point part of a B 5500 floating-point number is represented as an integer rather than a fraction, fixed-point and floating-point operands can be intermixed without conversions.

The comprehensive interrupt system informs the Processor when any of 40 possible special conditions arises anywhere in the system. All interrupt conditions are sampled continuously and processed on a priority basis, so that a high-priority interrupt condition (such as a storage parity error) can interrupt the servicing of a lower-priority interrupt condition (such as a free Input/Output Channel).

The Processor of the B 5500 system initiates all peripheral input-output operations by sending a descriptor to a free I/O Channel. The processor is then free to perform its operations independently of the peripheral operation. Up to four "floating" Input/Output Channels can be connected to the B 5500 system, and each Channel can transfer data between core storage and any of the connected input-output devices. Up to four input-output data transfer operations can be performed simultaneously, one per installed I/O Channel, since each I/O Channel functions independently of the others.

(Contd.)

.2 CENTRAL PROCESSOR (Contd.)

The B 5500's Processor includes many improvements to the original B 5000 Processor design. Processor read access time — the total time required to transfer a word of information from core memory to the Processor or an I/O Channel — has been reduced from 6 to 4 microseconds. Syllable overlap techniques have been improved, stack manipulation operations have been accelerated, and 19 new operators have been added. The primary objective in the inclusion of these and other improvements in the B 5500's Processor has been to enable the compilers to generate more efficient object programs and to permit the Master Control Program to perform its program-segment switching and multi-programming control routines more quickly and more effectively.

.3 INTERNAL STORAGE

From three to eight B 460 or B 461 Memory Modules of core storage can be connected to a B 5500 system. Each Memory Module contains 4,096 words, providing a maximum system capacity of 32,768 words, or 262,144 6-bit characters. Each word location consists of 48 data bits and one parity bit and can hold one binary data item (in floating-point or integer form), eight alphameric characters, or one program word. The B 460 Memory Module has a memory cycle time of 6 microseconds, as compared with the newer B 461's 4-microsecond cycle time. The B 460 and B 461 are functionally identical, but they cannot be intermixed in the same B 5500 system.

Each core storage module contains its own addressing and read/write circuitry. Operating in conjunction with a switching network called the Memory Exchange, the Memory Modules can transmit data independently of the central processor. Both the Processor and the I/O Channels can communicate with the Memory Modules, but always through the Memory Exchange. Using the maximum B 5500 complement of two Processors and four I/O Channels, six different Memory Modules can be accessed simultaneously. However, only one processor or I/O Channel can access any one Memory Module during any one memory cycle.

The B 430 Magnetic Storage Drum provides an 8.3-millisecond average access time to 32,768 words of auxiliary storage. Up to 1,023 consecutive words can be transferred at the rate of 15,360 words per second. Two Storage Drums can be connected to a B 5500 system. Customers who choose to have their B 5500 system controlled by the Drum Master Control Program (see Section 203:191) must have at least one Storage Drum on-line for MCP and system program residence; two Storage Drums are required for Drum MCP-oriented installations that wish to use COBOL. Use of the Storage Drum provides the MCP with rapid access to program segments, subroutines, and blocks of data.

Burroughs' head-per-track Disk Files can also be utilized as auxiliary storage with the B 5500 system. The Disk File system is a modular on-line storage system that provides storage capacities of up to 960 million characters in modules of 9.6 million characters. Any randomly-addressed block of characters can be accessed within a maximum of 40 milliseconds, and the average access time is only 20 milliseconds. Transfer of information between the Disk File system and the Input/Output Channels proceeds at an average of 100,000 characters per second. From 1 to 1,890 48-bit words of information can be read or written by a single instruction. If two B 5470 Control Units are connected to a B 5500 system, two simultaneous Disk File accesses are possible. Disk File accessing can also proceed simultaneously with computation and up to three additional input-output operations.

In addition to providing the standard random processing capabilities, the use of Disk File storage with the B 5500 system permits the storage of on-line program libraries. The Disk File-oriented MCP (see Section 203:192) is thereby enabled to gain rapid access to all scheduled programs, a fact which adds to the efficiency of the B 5500's multi-programming capability.

.4 INPUT-OUTPUT EQUIPMENT

Most of the input-output equipment offered for use with the B 5500 computer system is conventional in design and performance. Table I lists all of the current peripheral devices (other than the auxiliary storage units described in the preceding paragraphs), together with their principal characteristics. A B 5500 system can include a maximum of two card readers, one card punch, two line printers, three paper tape units (readers or punches), 16 magnetic tape units, and 15 data communications terminal units.

Four different types of data communications terminal units are offered by Burroughs for use with the B 5500 system. The B 481 Teletype Terminal Unit provides buffered interfacing for up to 399 remote Teletype stations; the B 483 Typewriter Terminal Unit can

TABLE I: B 5500 INPUT-OUTPUT DEVICES

Type of Device	Model No.	Name	Characteristics
Punched Card Equipment	B 122 B 123 B 124 B 129 B 303 B 304	Card Reader Card Reader Card Reader Card Reader Card Punch Card Punch	Reads 200 cpm. Reads 475 cpm. Reads 800 cpm. Reads 1,400 cpm. Punches 100 cpm. Punches 300 cpm.
Punched Paper Tape Equipment	B 141	Paper Tape Reader	Reads 5, 6, 7, or 8-level tape at 500 or 1,000 char/sec.
	B 341	Paper Tape Punch	Punches 5, 6, 7, or 8-level tape at 100 char/sec.
Printers	B 320 B 321 B 325 B 328 B 329	Line Printer Line Printer Line Printer Line Printer Line Printer	Prints 475 lpm; 120 print positions. Prints 700 lpm; 120 print positions. Prints 700 lpm; 132 print positions. Prints 1,040 lpm; 120 print positions. Prints 1,040 lpm; 132 print positions.
Magnetic Tape Units	B 422 B 423 B 424 B 425	Magnetic Tape Unit Magnetic Tape Unit Magnetic Tape Unit Magnetic Tape Unit	Transfers data at 24 or 66KC. Transfers data at 24KC. Transfers data at 66KC. Transfers data at 18, 50, or 72KC.
Data Communications Devices	B 5480	Data Communications Control Unit	Transfers data between Processor and Terminal Units at 30KC.
	B 481	Teletype Terminal Unit	Controls up to 399 remote Teletype stations.
	B 483	Typewriter Terminal Unit	Controls up to 8 typewriter inquiry stations.
	B 484	Dial TWX Terminal Unit	Controls up to 8 Dial TWX stations.
	B 487	Data Transmission Terminal Unit	Provides buffering and interfacing for wide variety of remote devices.

.4 INPUT-OUTPUT EQUIPMENT (Contd.)

control up to 8 typewriter inquiry stations; and the B 484 Dial TWX Terminal regulates the use of up to 8 stations of the Dial TWX network. The B 487 Data Transmission Terminal Unit, unlike the other Burroughs terminal units, is general in purpose, permitting a B 5500 system to communicate with a varied mix of data transmission devices without the use of additional terminal units. Most remote devices that can use the low-speed and voice-grade lines of the telephone companies can be connected to a B 487, and ultimately to a B 5500, via Burroughs line adapters. All four models of Burroughs' terminal units are buffered and can simultaneously accept inquiries from as many remote devices as their individual buffer sizes will accommodate. Buffer sizes are specified at the time of manufacture.

.5 SOFTWARE

.51 Compilers

Users of the B 5500 Information Processing System normally do all of their programming in the ALGOL, COBOL, or FORTRAN languages. Two additional languages, OSIL and ESPOL, are available for special-purpose programming. OSIL, or Operating Systems Implementation Language, is a symbolic assembly language that was developed for writing Burroughs' Drum Master Control Program. ESPOL, or Executive System Problem Oriented Language, is a modified version of the ALGOL language that was designed to facilitate the writing of the Disk File Master Control Program.

Extended ALGOL for the B 5500 includes virtually all of the facilities of ALGOL 60 and a number of useful machine-dependent extensions that enable the programmer to take advantage of the hardware capabilities of the B 5500. Some of these extensions include device-oriented input-output constructs, partial-word and double-precision arithmetic operations, B 5500 Character Mode statements, and constructs to control the operations of Burroughs data communications terminal units. The ALGOL compiler delivers translation speeds that range between 600 and 800 source-program cards per minute, or up

(Contd.)

.51 Compilers (Contd.)

to 2500 magnetic tape card images per minute. More than 100 standard mathematical functions are included in the ALGOL library of subroutines.

COBOL-61 Extended for the B 5500 is a comprehensive version of the Department of Defense's COBOL-61 Extended language. All of Required COBOL-61 has been implemented, as well as most of the Elective features of COBOL-61. Two of the three principal extensions of COBOL-61 Extended — the SORT verb and the Mass Storage language facilities — have also been implemented. (Tape or Disk File sorting on the B 5500 system, using Burroughs-supplied software, is possible only through the use of the COBOL SORT verb and the Sort Generator within the COBOL compiler.) The Mass Storage facilities provide the programmer with direct control over both sequential and random processing of records on the Disk File. COBOL language facilities are also provided to permit the effective use of Burroughs' various types of data communications terminal units. Translation speeds of up to 800 source-program cards per minute have been achieved with the COBOL compiler, and the practicality of programming and debugging exclusively in COBOL has been effectively demonstrated through more than two years of successful user experience.

FORTRAN IV for the B 5500 includes virtually all of the language features proposed by the X.3.4.3 FORTRAN group of the American Standards Association. In comparison to this standard, B 5500 FORTRAN lacks only the provisions to handle double-precision and complex variable items. Burroughs has designed its FORTRAN language to duplicate, wherever possible, the facilities of the IBM 7090/7094 FORTRAN IV language in order to facilitate conversions of scientific and engineering installations to the B 5500. Burroughs' FORTRAN translator (called FORGOL 4) converts FORTRAN IV source statements into Extended ALGOL for eventual compilation by the ALGOL compiler. No FORTRAN language facilities have been implemented to date by Burroughs to provide direct control of Disk File storage or remote terminal devices.

Almost all program debugging on the B 5500 system is done at the source language level. MONITOR and DUMP statements are provided in the ALGOL and COBOL languages to produce tracers, dumps, and snapshots as requested by the programmer.

.52 Master Control Program (MCP)

The Master Control Program, or MCP, is a comprehensive operating system that controls the scheduling, loading, and execution of every program that is run on a B 5500 system. By means of close integration with the hardware interrupt facilities of the B 5500 system, the MCP controls multiprogramming, or the simultaneous processing of two or more independent program segments.

To use multiprogramming effectively with the B 5500 system, the only prerequisites are that the programs be written in small, logical segments, and that sufficient input-output equipment be available to service the needs of the multiple program segments. The MCP continually analyzes the list of scheduled jobs and decides, on its own, when and to what degree multiprogramming is possible. The sole criterion used by the MCP in making this decision is the continuous use of as many as possible of the processing and input-output facilities of the B 5500 system.

Other functions performed by the MCP include automatic handling of most error conditions, monitoring and control of communications between the system and the operator, complete logging of processing and input-output times for each program processed, and maintenance of the system and problem program libraries.

Two versions of the Master Control Program are offered for use with the B 5500 system: the Drum MCP and the more recent Disk File MCP, both designated according to the system device on which the MCP and its control routines reside. The Drum MCP is slightly less flexible than the Disk MCP in that the Drum MCP lacks the facilities to control Disk File and data communications operations. In addition, the Drum MCP gathers its scheduled programs on a Program Collection Tape and scans this tape to access programs that are appropriate for inclusion in a multiprogramming mix at any given time. By contrast, the Disk File MCP has direct access to any object program stored in the on-line program library. This advantage can lead to significant improvements in multiprogramming performance under control of the Disk File MCP. It should be noted that the storage of frequently-accessed program segments on the magnetic drum will be advantageous even when the Disk File MCP is used, due to the drum's faster average access time of 8.3 milliseconds.

Both versions of the MCP require the permanent use of the first 1,600 words of core storage for basic control routines; other portions of the MCP are called into core storage from drum or disc storage as required. Burroughs estimates that the MCP's control functions consume between 2 and 10 per cent of the system's total processing time in typical applications; yet the improvements in throughput gained by means of MCP-controlled multiprogramming can far overshadow the small MCP overhead time.

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	48 data bits plus 1 parity bit.	basic addressable unit; holds a data item, 8 characters, or 4 syllables.
Row:	6 data bits plus 1 parity bit.	magnetic tape; holds 1 character or 1/8 of a binary word.
Line:	120 or 132 characters	Line Printer reports.
Column:	12 positions	punched cards.
Block:	1 to N characters	magnetic tape, and Disk File in alphanumeric mode.
Block:	1 to 1,023 words	magnetic tape and Disk File in binary mode.

.2 DATA FORMATS

Type of Information	Representation
Instruction	four 12-bit "syllables" per word; each can be an operator, literal, operand call, or descriptor call.
Descriptor	1 word; used for indirect addressing and supplementary control.
Integer number	1 word: 39 data bits + sign.
Floating-point number	1 word: 39 bits + sign for integer part, 6 bits + sign for exponent.
Character	6 bits (internal), 1 row (tape), or 1 column (cards).
Card image	4 card columns per word; 20 consecutive words per card.

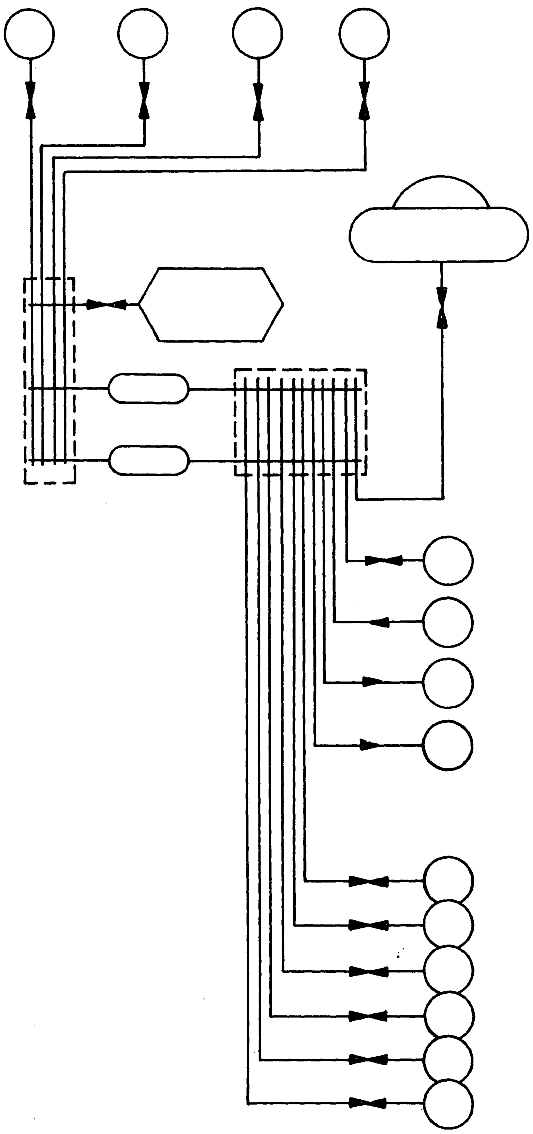
SYSTEM CONFIGURATION

The upper and lower limits of on-line system configuration for the B 5500 are summarized in the following table.

Model No.	Unit	Min. No.	Max. No.	Notes
B 5280	Processor A	1	1	
B 5281	Processor B	0	1	
B 460	Memory Module (4,096 48-bit words, 6 μsec cycle time)	3	8	B 460 and B 461 modules cannot be intermixed in one system; COBOL requires a minimum of 4 memory modules.
B 461	Memory Module (4,096 48-bit words, 4 μsec cycle time)	3	8	
B 430	Storage Drum (32,768 words)	0	2	No B 430 Storage Drum is required if Disk File storage is available.
B 5283	Input/Output Channel	1	4	Up to 32 input/output devices can be supported.
B 422	Magnetic Tape Unit (24-66KC)	1	16	From 1 to 16 tape units per system can be supported; B 422 and B 423 units cannot be intermixed; B 422 and B 424 can be intermixed if B 422 operates at 120 ips.
B 423	Magnetic Tape Unit (24KC)	1	16	
B 424	Magnetic Tape Unit (66 KC)	1	16	
B 320	Line Printer (475 lpm, 120 char)	1	2	Either 1 or 2 line printers per system can be supported; B 325 and B 329 models require use of a special adapter.
B 321	Line Printer (700 lpm, 120 char)	1	2	
B 325	Line Printer (700 lpm, 132 char)	1	2	
B 328	Line Printer (1,040 lpm, 120 char)	1	2	
B 329	Line Printer (1,040 lpm, 132 char)	1	2	
B 122	Card Reader (200 cpm)	1	2	Either 1 or 2 card readers can be supported per system.
B 123	Card Reader (475 cpm)	1	2	
B 124	Card Reader (800 cpm)	1	2	
B 129	Card Reader (1,400 cpm)	1	2	
B 303	Card Punch (100 cpm)	0	1	
B 304	Card Punch (300 cpm)	0	1	
B 141	Paper Tape Reader (500-1,000 cps)	0	2	Up to 3 paper tape units can be supported per system.
B 341	Paper Tape Punch (100 cps)	0	2	
B 450	Disk File/Data Communications Basic Control	0	1	Up to 960 million characters of Disk File storage can be supported, in modules (B 475) of 9.6 million characters.
B 451	Disk File Expanded Control	0	4	
B 5470	Disk File Control Unit	0	2	
B 471	Disk File Electronics Unit	0	20	
B 475	Disk File Storage Module	0	100	
B 5480	Data Communication Control Unit	0	2	Up to 15 terminal units can be supported per system.
B 481	Teletype Terminal Unit	0	15	
B 483	Typewriter Terminal Unit	0	15	
B 484	Dial TWX Terminal Unit	0	15	
B 493	Typewriter Inquiry Station	0	120	
—	Supervisory Printer and Keyboard	1	1	

.1 6-TAPE BUSINESS SYSTEM; CONFIGURATION III

Deviations From Standard Configuration: . . . . . Disk File storage is used by Master Control Program.
Core storage capacity is 10 times larger than standard.
Card Reader is 60% faster.
Line printer is 40% faster.
Magnetic tape units are 20% slower.



Equipment	Rental
4 B 461 Memory Modules: 16,384 words total (4 μsec cycle time)	$ 5,800
Disk File storage (9.6 million characters) and controllers	2,620
Processor	7,400
2 Input/Output Channels	2,500
Supervisory Printer & Keyboard	*
B 124 Card Reader: 800 cards/min.	400
B 303 Card Punch: 100 cards/min.	450
B 321 Line Printer: 700 lines/min.	1,200
6 B 423 Magnetic Tape Units: 24,000 char/sec.	2,970
Total:	$23,340

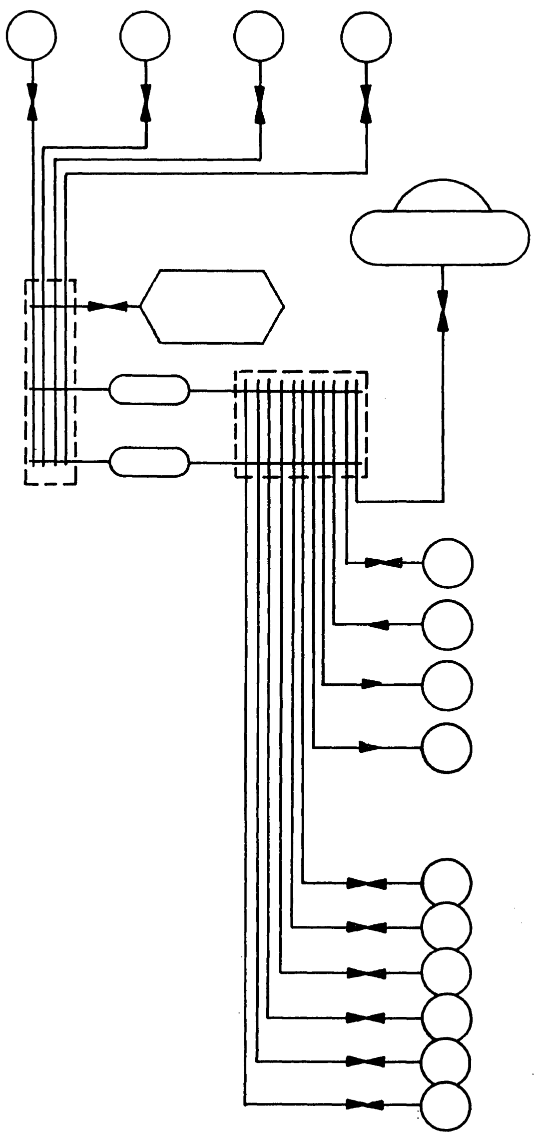
* Included in Processor rental.

Note: This system also meets all requirements for Standard Configuration VI, the 6-Tape Business/Scientific System.

(Contd.)

.2 6-TAPE AUXILIARY STORAGE SYSTEM: CONFIGURATION V

Deviations from Standard Configurations: . . . One Disk File Storage Module (9.6 million chars.) is used by Master Control Program.
Core storage capacity is 10 times larger than standard.
Card Reader is 60% faster.
Line printer is 40% faster.
Magnetic tape units are 20% slower.

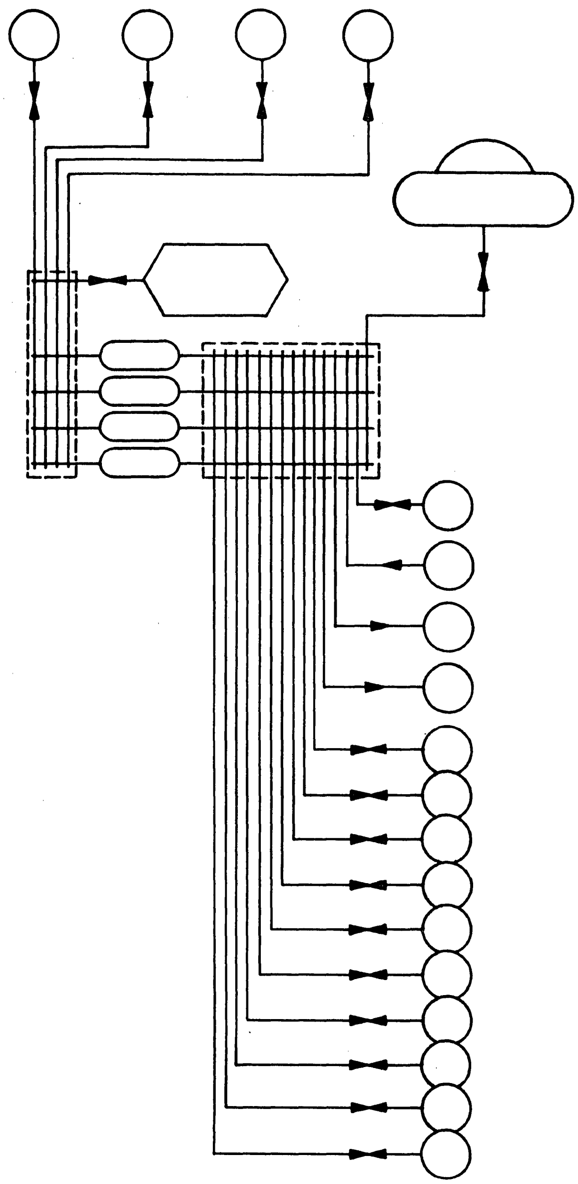


Equipment	Rental
4 B 461 Memory Modules: 16,384 words total (4 μsec cycle time)	$ 5,800
Disk File controllers	920
3 Disk File Storage Modules (28.8 million characters)	3,610
Processor	7,400
2 Input/Output Channels	2,500
Supervisory Printer & Keyboard	*
B 124 Card Reader: 800 cards/min.	400
B 303 Card Punch: 100 cards/min.	450
B 321 Line Printer: 700 lines/min.	1,200
6 B 423 Magnetic Tape Units: 24,000 char/sec.	2,970
Total	$25,250

* Included in Processor rental.

.3 INTEGRATED 10-TAPE GENERAL SYSTEM; CONFIGURATION VIIA

Deviations from Standard Configuration: . . Core storage is 82% larger than standard.
Disk File storage is used by Master Control Program.
Card reader is 60% faster.
Printer is twice as fast as standard.



Equipment	Rental
B 461 Memory Modules: 16,384 words total (4 μsec cycle time)	$ 5,800
Disk File storage (9.6 million characters) and controllers	2,620
Processor	7,400
4 Input/Output Channels	5,000
Supervisory Printer & Keyboard	*
B 124 Card Reader: 800 cards/min.	400
B 303 Card Punch: 100 cards/min.	450
B 328 Line Printer: 1,040 lines/min.	1,325
10 B 422 Magnetic Tape Units: 24,000 or 66,600 char/sec.	8,000
Total	$30,995

* Included in Processor rental.

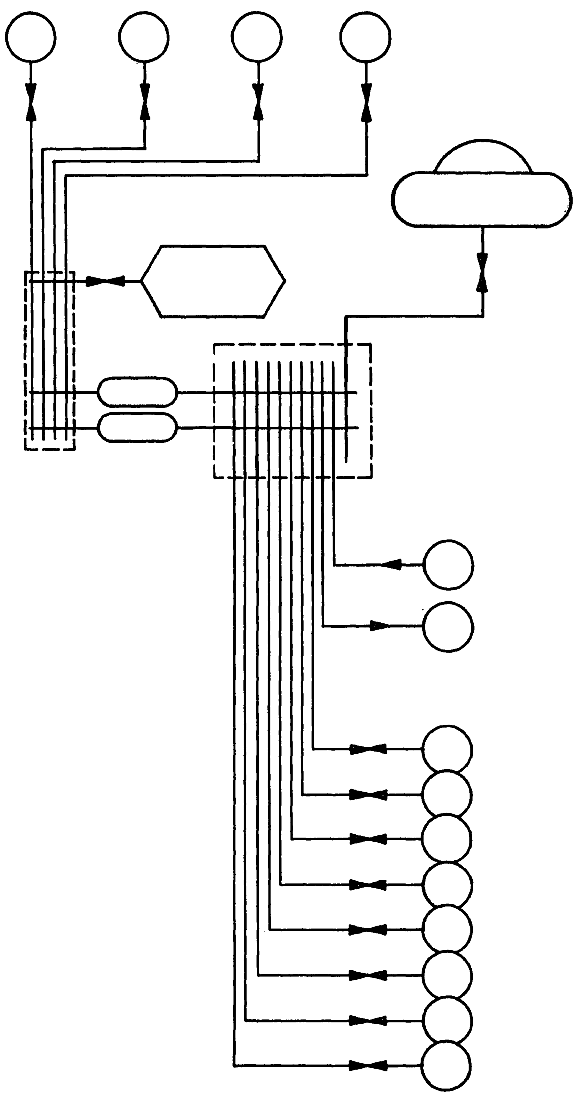
(Contd.)

.4 PAIRED 10-TAPE GENERAL SYSTEM; CONFIGURATION VIIB

Deviations from Standard Configuration

On-line: . . . . Core storage is more than twice as large as standard.
Disk File storage is used by Master Control Program.
Card reader is twice as fast as standard.

Off-line: . . . . Magnetic tape units are 25% slower.
Multiply-Divide hardware is standard.
Card reader, punch, and printer are buffered.
No console typewriter is available with B 180 processor.

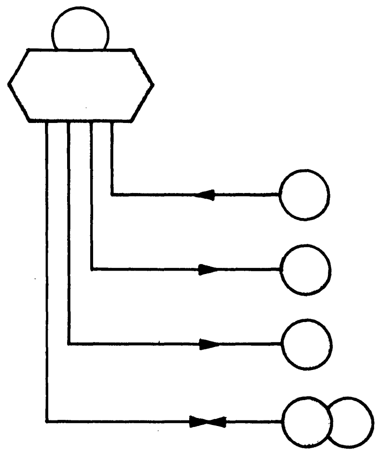


Equipment	Rental
4 B 461 Memory Modules: 16,384 words total (4 μsec cycle time)	$ 5,800
Disk File storage (9.6 million characters) and controllers	2,620
Processor	7,400
2 Input/Output Channels	2,500
Supervisory Printer & Keyboard	*
B 122 Card Reader: 200 cards/min.	220
8 B 422 Magnetic Tape Units: 24,000 or 66,000 char/sec.	6,400
Total:	$24,940
Total, including off-line equipment (next page):	$28,705

* Included in Processor rental.

.4 CONFIGURATION VIIB (Contd.)

Off-Line Equipment (Burroughs B 180)



Equipment	Rental
Core Storage: 4,800 characters; B 180 Processor (10 μsec cycle time)	$1,195
B 123 Card Reader: 475 cards/min.	320
B 303 Card Punch: 100 cards/min.	450
B 320 Line Printer: 475 lines/min.	810
2 B 423 Magnetic Tape Units: 24,000 char/sec.	990
	3,765

INTERNAL STORAGE: B 460/461 MEMORY MODULES

.1 GENERAL

.11 Identity: . . . . B 460 Memory Module (6-μsec cycle).
B 461 Memory Module (4-μsec cycle).

.12 Basic Use: . . . . working storage.

.13 Description

Working storage for B 5500 systems is provided by either B 460 or B 461 Memory Modules. The B 460 has a memory cycle time of 6 microseconds, as opposed to the newer B 461's 4-microsecond cycle time. Except for this difference in memory cycle time, the B 460 and B 461 Memory Modules are functionally identical. However, they cannot be intermixed in the same B 5500 system.

Each B 460 or B 461 Memory Module provides 4,096 48-bit words of coincident-current magnetic core memory. A minimum of three and a maximum of eight memory modules can be utilized with each B 5500 computer system, providing core storage capacities ranging from 12,288 to 32,768 words. If the COBOL language is to be used in a B 5500 installation, the minimum core storage requirement is four memory modules (16,384 words).

Each individual memory module contains its own addressing and read-write circuitry. Operating in conjunction with a switching network called the Memory Exchange, a section of the B 5500 Central Control Unit, the memory modules can transmit data independently of the central processor. The effective memory read access time of the B 460 Memory Module is 3 microseconds per word; that of the B 461 Memory Module is 2 microseconds per word (or 250 nanoseconds per 6-bit character). Both the Processor and the Input/Output Channels can communicate with the memory modules, but always through the Memory Exchange. When the maximum complement of two Processors and four Input/Output Channels is connected to a B 5500 system, up to six different memory modules can be accessed simultaneously. However, only one Processor or I/O Channel can access the same memory module at the same time.

The address of each word of available core storage is formed by means of a 15-bit binary field. The first three bits of the address field designate the memory module to be accessed, and the remaining twelve bits refer directly to the specific address within the 4,096 possible addresses of the designated memory module. The selection of the designated memory module is performed by the Memory Exchange network, but the memory module itself independently locates the addressed location within its core storage. This method of memory access contributes to the B 5500's ability to communicate with up to six memory modules simultaneously.

Each of the 4,096 word locations in a memory module holds 48 data bits and one parity bit. Therefore each location can store one single-precision fixed-point or floating-point data item, eight alphameric characters, one 4-syllable program word, or one Program or Data Descriptor. Each memory module also contains a 12-bit Memory Address register, which holds the address of the location currently being accessed, and a 49-bit Information Buffer register, which receives each word to be stored and transmits each word that is read from storage.

A parity bit is generated when a word is stored and checked when it is read out of storage. Checks are also made for invalid storage addresses and for references to segments not currently in core storage. Any of these error conditions will cause an interrupt and a transfer of control to the Master Control Program.

Burroughs anticipates that the use of the 4-microsecond B 461 Memory Module, rather than the 6-microsecond B 460, will improve B 5500 processing times by as much as 25%.

.14 Availability: . . . . immediate for B 460 and B 461.

.15 First Delivery: . . . . . April 1963 for B 460.
April 1965 for B 461.

.16 Reserved Storage: . . . 1600 words in 1 module are reserved for most frequently-used portion of Master Control Program and are not normally available as working storage. Attempts to access this area in the Normal State cause invalid address interrupts.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic cores.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.27 Interleaving Levels: . . no interleaving.

.28 Access Techniques

.281 Recording method: . . . coincident current.
.282 Reading method: . . . . sense wire.
.283 Type of access: . . . . . uniform; read-out followed by rewrite.

.29 Potential Transfer Rates

.292 Peak data rates —
Cycling rate: . . . . . . 166,667 cps for B 460. 250,000 cps for B 461.
Unit of data: . . . . . . word.
Conversion factor: . . 48 data bits per word.
Data rate: . . . . 166,667 words/sec for B 460. 250,000 words/sec for B 461.
Compound data rate: . when 2 Processors and 4 I/O Channels each access a separate Memory Module, the B 460 transfers up to 1,000,000 words/sec and the B 461 transfers up to 1,500,000 words/sec.

.3 DATA CAPACITY

.31 Module and System Size

	Minimum Storage	Maximum Storage
Identity:	B 460 or B 461	B 460 or B 461
Modules:	3	8
Words:	12,288	32,768
Characters:	98,304	262,144
Syllables:	49,152	131,072

.32 Rules for Combining Modules: . . . . 3 to 8 Memory Modules per system; B 460 and B 461 cannot be intermixed.

.4 CONTROLLER

.41 Identity: . . . . Central Control Unit, model B 5220 (part of B 5280 Processor).

.42 Connection to System

.421 On-line: . . . . 1 Central Control Unit.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . 3 to 8 Memory Modules.
.432 Restrictions: . . . . none.

.5 ACCESS TIMING

.51 Arrangement of Heads: . . . . 1 access device per module.

.52 Simultaneous Operations: . . . . each module operates independently; maximum number of simultaneous accesses is N, where N is either the number of Memory Modules or the total number of Processors and I/O Channels, whichever is smaller.

.53 Access Time Parameters and Variations

.531 For uniform access —
Access time: . . . . . . 3 μsec for B 460. 2 μsec for B 461.
Cycle time: . . . . 6 μsec for B 460. 4 μsec for B 461.
For data unit of: . . . 1 word of 48 data bits and 1 parity bit.

.7 PERFORMANCE

.72 Transfer Load Size

With self: . . . . 1 to 63 words.
With storage drum: . . . . 1 to 1,023 words.
With Disk File: . . . . . 1 to 1,890 words.

.73 Effective Transfer Rate

With self (via Processor): . . . . . . 44,168 words/sec for B 460; 55,555 words/sec for B 461.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	interrupt.
Receipt of data:	parity check	interrupt.
Recording of data:	record parity bit.	
Recovery of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	
Timing conflicts:	check	form access request queue according to priority.
Physical record missing:	presence check	interrupt.

INTERNAL STORAGE: B 430 MAGNETIC DRUM

.1 GENERAL

.11 Identity: . . . . B 430 Magnetic Drum Memory.

.12 Basic Use: . . . . auxiliary storage.

.13 Description

The B 430 Magnetic Drum Memory (or simply, Storage Drum) is an auxiliary storage device that provides rapid access to program segments, subroutines, and blocks of data. Up to two Storage Drums can be connected to a B 5500 system. Each drum provides 32,768 word locations of storage, arranged in 64 bands of 512 words each. At least one Storage Drum is required with each B 5500 system that is controlled by the Drum Master Control Program (MCP). Business-oriented installations using COBOL require two Storage Drums when operating in the Drum MCP environment. However, if the newer Disk File MCP is alternatively selected as the B 5500's operating system, then a Storage Drum is not essential to the B 5500 configuration.

Each of the B 430 Storage Drum's 64 bands consists of 6 tracks that are read and recorded in parallel. Each word location contains eight 6-bit data rows and one 6-bit parity row. The 512 words in each band are recorded in the form of 2 interleaved groups of 256 words each. Therefore, any location can be accessed within one drum revolution, but two revolutions are required to transfer a full band. Drum speed is 3,600 revolutions per minute, so the average access time is 8.3 milliseconds. Peak data transfer rate is 15,360 words or 122,880 characters per second.

The B 430 is considered an input-output device, and, as such, all data transfers are performed through the Input/Output Channels. Drum read or write operations are initiated when the Processor sends an Input or Output Descriptor from the A register to an idle Input/Output Channel. The descriptor specifies the number of consecutive words (from 1 to 1,023) to be transferred between a Storage Drum and a Memory Module, and the drum and core address of the first word to be transferred. Reading or writing can start at any drum address.

When a drum read or write operation is completed, the Input/Output Channel sets an interrupt bit and places an External Result Descriptor in a fixed storage location. If any of the following error conditions has occurred, it is indicated by a specific bit in the result descriptor: incorrect parity, reference to a locked area, not ready, malfunction, busy, or drum storage overflow.

Protection against overwriting sections of the Storage Drum is provided by four manual switches, each capable of locking out attempted write operations within a 4,096-word block. Drum read or write operations are not directly provided in the available B 5500 programming languages, such as COBOL, ALGOL, and FORTRAN. Instead, the Master Control Program controls the use of the Storage Drum for storing and retrieving frequently-used blocks of data and program segments. In addition, when the drum version of the MCP is used, the COBOL, ALGOL, and/or FORTRAN compilers, as well as the MCP itself, are resident on Storage Drum 1. Consequently, this Storage Drum is unavailable for use by the MCP as auxiliary storage.

.14 Availability: . . . . immediate.

.15 First Delivery: . . . . . April, 1963.

.16 Reserved Storage

.161 Hardware: . . . . 4 manual lockout switches per Storage Drum protect 4,096-word blocks of storage.

.162 Software: . . . . the Drum MCP and its compilers reserve exclusive use of one Storage Drum.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic drum.

.22 Physical Dimensions

.222 Drum —
Diameter:. . . . . 8 inches.
Length: . . . . 22 inches.
Number on shaft: . . . 1.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 6 Tracks

Words:. . . . . 512.
Characters: . . . . 4,096.
Syllables: . . . . 2,048.

.26 Bands per Physical Unit: . . . . 64.

.27 Interleaving Levels: . . 2.

.28 Access Techniques

.281 Recording method: . . . fixed heads.
.283 Type of access: . . . . . wait for specified sector to pass under read/write heads.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rate: . . . . . . 3,600 rpm.
Track/head speed: . . . . 1,510 inches/sec.
Bits/inch/track: . . . 183 (average).
Bit rate per track: . . . . 276,480 bits/sec/track.
.292 Peak data rates —
Unit of data: . . . . . . word.
Conversion factor: . . . . 48 data and 6 parity bits per word.
Gain factor: . . . . . . 6 tracks per band.
Loss factor: . . . . . . 2 interleaving levels.
Data rate: . . . . 15,360 words/sec.
Compound data rate: . . . . 30,720 words/sec (2 drums).

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum Storage
Identity:	B 430	B 430
Drums:	1	2
Words:	32,768	65,536
Characters:	262,144	524,288
Syllables:	131,072	262,144

.32 Rules for Combining Modules: . . . . 0 to 2 Storage Drums per system.

.4 CONTROLLER

.41 Identity: . . . . Input/Output Channel, Model B 5283.

.42 Connection to System

.421 On-line: . . . . 1 to 4 channels.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per system: . . . . 0 to 2 drums; either drum can use any available channel; switching is performed automatically.
.432 Restrictions: . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . 1 to 1,023 words.
.442 Input-output area: . . . core storage.
.443 Input-output area access: . . . . each word.
.444 Input-output area lockout: . . . . yes; program reference to a descriptor of an input-output area being filled or emptied causes an interrupt.
.445 Synchronization: . . . . automatic.
.447 Table control: . . . . . . none.
.448 Testable conditions: . . parity error; reference to locked area; busy unit; not ready; core storage overflow.

.5 ACCESS TIMING

Stage	Variation, μsec	Example, μsec
Switch bands:	0 or 25	25
Wait for specified sector:	0 to 16,667	8,333
Read or write:	65 to 66,500*	16,700
	65 to 83,192	25,058

.52 Simultaneous Operations: . . . . maximum of 1 read or write operation per drum; two drums can be accessed simultaneously.

.53 Access Time Parameters and Variations

.6 CHANGEABLE STORAGE: . . . . no.

.7 PERFORMANCE

.72 Transfer Load Size

With Memory Modules: . . . . 1, to 1,023 words.

.73 Effective Transfer Rate

With Memory Modules: . . . . 15,360 words/sec or 122,880 char/sec.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	set bit indicator.
Invalid code:	all codes valid.	
Receipt of data:	parity check.	
Recording of data:	record parity bits.	
Recovery of data:	parity check	set bit indicator.
Dispatch of data:	send paritybit.	
Timing conflicts:	"busy" check	set bit indicator.
Reference to locked area:	check	set bit indicator.
Descriptor parity:	check	set bit indicator.

Note: All "bit indicators" are set in the External Result Descriptor that is returned to core storage at the end of each input-output operation.

* 65 μsec per word transferred.

INTERNAL STORAGE: DISK FILE SYSTEM

.1 GENERAL

.11 Identity: . . . . B 450 Disk File/Data Communications Basic Control Unit.
B 5470 Disk File Control Unit.
B 451 Disk File Expanded Control.
B 471 Disk File Electronics Unit.
B 475 Disk File Storage Module.

.12 Basic Use: . . . . random-access auxiliary storage.

.13 Description

The Burroughs B 5500 Disk File System is a large-capacity random-access storage facility that provides the capability to store up to 960 million 6-bit characters and to access any selected block of characters within an average of 20 milliseconds. The high data capacity and fast access time of the Disk File System result largely from high-density recording and a fixed read/write head for every data track. Electronic switching between tracks in place of movable access arms contributes to the improved speed and reliability of the B 5500 Disk File System.

The B 450 Disk File/Data Communications Basic Control Unit serves as an interface between the B 5500 and up to two B 5470 Disk File Control Units or B 5480 Data Communication Control Units. The B 5470 Disk File Control Unit is the control center for the B 5500 Disk File System; it regulates the transfer of 48-bit words of data to and from the Input/Output Channels. Since the B 5500 system can accommodate two independently-operating B 5470's, two simultaneous Disk File accesses are possible. Disk File access can also proceed simultaneously with computation and with three additional input-output operations.

Each B 5470 Disk File Control Unit contains the control and checking circuitry to support up to 480 million characters of data. The B 5470 controls from one to ten B 471 Disk File Electronics Units, and each Electronics Unit contains the circuitry to control from one to five B 475 Disk Storage Modules. Each Storage Module contains four magnetic discs that together provide storage for up to 9.6 million characters of data, the smallest available unit of Disk File storage. The B 451 Disk File Expanded Control is required when on-line Disk File storage exceeds 48 million characters. Up to four B 451's can be required, one for each additional block of 240 million storage locations that is included in the Disk File system. Table I shows the potential B 5500 Disk File System sizes and the configuration requirements for each size.

TABLE I: SELECTED DISK FILE SYSTEM SIZES AND CONFIGURATION REQUIREMENTS

Size in Millions of Characters	Disk File System Components				
	B 475	B 471	B 451	B 5470	B 450
9.6	1	1	0	1	1
48	5	1	0	1	1
96	10	2	1	1	1
240	25	5	1	1	1
480	50	10	2	1	1
960	100	20	4	2	1

The following is a breakdown of the storage capacities of the Disk File system components:

- Segment — contains 240 6-bit characters or 30 48-bit words; it is the smallest addressable area of Disk File storage.
- Data Track — contains up to 24,000 characters, divided into 100 segments.
- Disc Face — contains 50 data tracks. (Both disc faces are used for data storage.)
- Storage Module — includes 4 vertically-mounted discs on one horizontal shaft. Each Storage Module contains 9.6 million character locations.
- Electronics Unit — controls 1 to 5 Storage Modules.
- Control Unit — controls 1 to 10 Electronics Units, providing from 48 to 480 million character locations of disc storage.
- Basic Control — Supports the B 5500 system maximum of two Control Units.

The magnetic discs rotate at 1500 rpm, and since no repositioning of the read/write heads is required, the maximum access time to any data record is 40 milliseconds (one disc revolution) and the average is 20 milliseconds. One situation in which the average access time is greater than 20 milliseconds is that of updating a record in a non-sequential file. This operation requires two accesses (to read the original record and then rewrite the updated version); but the second access is not a random reference and will often cost almost a full revolution (40 milliseconds). Thus, the average access time for file maintenance operations will be about 30 milliseconds. No timing synchronization between different Storage Modules is possible; this prevents attempts to optimize programming by minimizing disc latency.

Transfer of information between the Disk File system and the Input/Output Channels proceeds at an average rate of 100,000 characters per second. Data transfers are executed as 8-character, 48-bit

.13 Description (Contd.)

words that are assembled in the B 5470 Control Unit. From 1 to 1,890 words (63 segments) of information can be read or written by a single instruction.

Disk File segments are addressed through the B 5470 Control Unit by means of a 7-character address. The first character designates the Storage Module to be accessed, and the remaining six characters designate the segment address. Segment addresses are assigned starting at some point on the first disc surface of a Storage Module and continuing in direct sequential order through the 40,000 segments of the module. The validity of each Disk File Address is checked by the Control Unit prior to any transfer of data. Detection of an invalid address terminates execution of the Disk File instruction and sets a specific error indicator in the appropriate I/O Result Descriptor.

A "check character" is generated in the B 5470 Control Unit and recorded with each 48-bit data word. This check-character code is automatically regenerated and compared with the code read from the disc during every read operation or during a special Disk File Check operation. If the check-character comparison is unequal, a special error bit is set in the Disk File Result Descriptor.

Burroughs Corporation does not emphasize the use of the programmed read-after-write check for two reasons: first, the readback-and-check operation can triple the time normally required to write a segment of data; and second, the reliability of the head-per-track Data File design is allegedly high enough to render such a checking operation unnecessary. Instead, Burroughs recommends, in some situations, a simultaneous tape write-out of the data recorded on the Disk File.

A number of physical precautions are taken to safeguard the information on the discs:

- The head design is such that if the heads approach the discs too closely, a fail-safe technique moves the heads away and switches the unit off.
- The heads are embedded in a soft material so that the discs will not be damaged if the heads come into contact with the discs.
- Each individual disc has its own manual lockout circuits which can prevent it from being written upon, while allowing reference to its contents.

Programming of the Disk File system with the B 5500 is made possible by special language constructs provided in the ALGOL and COBOL compilers. (Report Sections 203:161 and 203:162 describe these language facilities.) The Disk File Master Control Program makes use of the Disk File's high storage capacity for storing all its control programs and language compilers, as well as all the programs in the installation's library. The Disk File's relatively fast access time permits the MCP to make all programs and on-line data blocks available quickly for use by the problem program.

.14 Availability: . . . . immediate.

.15 First Delivery: . . . . . 3rd quarter of 1964.

.16 Reserved Storage: . . . the Disk File MCP reserves use of 1,000 segments of Storage Module 1; a manual lockout switch can prevent access to each disc.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . multiple magnetic discs.

.22 Physical Dimensions

.222 Disc —
Diameter: . . . . 26.5 inches.
Thickness or length: . 0.125 inch.
Number on shaft: . . . 4 (shaft is horizontal).

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 1 Track

Words: . . . . 3,000.
Characters: . . . . 24,000.
Digits: . . . . 24,000.
Instructions: . . . . 12,000.
Segments: . . . . 100.

.26 Bands per Physical Unit: . . . . 50 per disc surface.

.27 Interleaving Levels: . . 1.

.28 Access Techniques

.281 Recording method: . . . every track on each disc surface has an individual, fixed head.
.283 Type of access: . . . . . wait for selected segment for reading or recording; no repositioning of access mechanisms is involved.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 1,500 rpm.
Bit rate per track: . . 700,000 bits/sec/track.
.292 Peak data rates —
Unit of data: . . . . . . word.
Conversion factor: . . 48 bits plus parity bit.
Gain factor: . . . . . . 1 track/band.
Data rate: . . . . 12,500 words or 100,000 characters per second.

(Contd.)

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage			Maximum Storage
Identity:	-	B 475 Disk File Storage Module	B 471 Disk File Electronics Unit	B 450 Disk File Basic Control
Discs:	0	4	20	400
Words:	0	1,200,000	6,000,000	120,000,000
Characters:	0	9,600,000	48,000,000	960,000,000
Instructions:	0	4,800,000	24,000,000	480,000,000
Modules:	0	1	5 (max.)	100 (max.)

.32 Rules for Combining Modules: . . . . 1 or 2 Control Units can be used per B 5500; 1 to 10 Electronics Units can be connected to each Control Unit; 1 to 5 Storage Modules can be connected to each Electronic Unit.

.4 CONTROLLER

.41 Identity: . . . . B 5470 Disk File Control Unit.

.42 Connection to System

.421 On-line: . . . . 1 or 2 B 5470's.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . 1 to 10 Electronics Units.
.432 Restrictions: . . . . refer to Table I.

.44 Data Transfer Control

.441 Size of load: . . . . 1 to 63 240-character segments, or 1 to 1,023 words.
.442 Input-output area: . . . core storage.
.443 Input-output area access: . . . . each character.
.444 Input-output area lockout: . . . . none.
.445 Synchronization: . . . . automatic.
.446 Synchronizing aids: . . none.
.447 Table control: . . . . . . none.
.448 Testable conditions: . . busy controller; recording lock; recovery error; transfer error; address error.

.5 ACCESS TIMING

.51 Arrangement of Heads: one read-write head per track.

.52 Simultaneous Operations: . . . . only one Disk File operation at a time per B 5470 Control Unit can be performed.

.53 Access Time Parameters and Variations

Stage	Variation	Average
Positioning:	0	0.
Latency (rotational delay):	0 to 40 msec.	20 msec.
Total:	0 to 40 msec.	20 msec.

.6 CHANGEABLE STORAGE: . . . . none.

.7 AUXILIARY STORAGE PERFORMANCE

.72 Transfer Load Size

With core storage: . . . 1 to 63 segments; number of segments is selected by program.

.73 Effective Transfer Rate

With core storage: . . . 80,000 char/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	error indicator set, operation terminated.
Receipt of data:	parity check on addresses	indicator set, operation terminated, no data transferred.
Recording of data:	optional programmed readback	set indicator.
Recovery of data:	regenerate and compare check character	set indicator.
Dispatch of data:	parity bit included; not-ready check	branch.
Timing conflicts:	interrogate command	branch on busy, error, or write interlock.
Reference to locked area:	check	indicator set, operation terminated.

CENTRAL PROCESSOR

.1 GENERAL

.11 Identity: . . . . B 5280 Basic System —
B 5220 Central Control;
B 5281 Processor;
B 5282 I/O Subsystem;
B 5290 Display and Distribution;
B 5370 Power Supply.

.12 Description

.121 Summary

The B 5281 Processor of the B 5500 Information Processing System represents an upgraded, improved version of the central processor originally supplied with the Burroughs B 5000 systems. Production of the older processors has ceased, and all processors in the field have been modified to include the improved performance features of the B 5281 Processor. All existing B 5000 systems have thus been transformed into B 5500's. Paragraph .129 below enumerates several changes that have been incorporated into the design of the original central processors.

One or two functionally independent Processors can be included in a B 5500 system. Access to instructions and data in the B 460 or B 461 Memory Modules is accomplished through the Memory Exchange of the Central Control — a general switching network. All information transfers between the Processor and Memory Modules are made in units of 48-bit words.

Internal operations can be performed in either the Word Mode, using 48-bit binary words as operands, or in the Character Mode, using variable-length alphameric fields packed eight characters to the word. In the Word Mode, a common representation is used for floating-point and integer numbers, so conversion routines are not required. Complete arithmetic facilities for single and double-length operands are provided in the Word Mode. The Character Mode is designed mainly for data manipulation operations such as editing and scanning.

Instructions are 12-bit "syllables," packed four per program word. Each syllable specifies an operation, a relative address, or a 10-bit literal. Processor fetch overlap is provided to mask the access to successive instruction syllables and words with the execution of the current syllable. "Descriptors" are 48-bit words used for indirect addressing and supplementary control; they, along with single operands, are stored in a relocatable core storage area called the Program Reference Table. The "stack" consists of two Processor registers and a reserved area of core storage, and provides temporary storage for an ordered list of operands and control words.

.122 States, Levels, and Modes

The Processor will at all times operate in either the Normal or Control State, in either the Program or Subprogram Level, and in either the Word or Character Mode.

Operation is in the Normal State except when a bit is set in the Interrupt Register to indicate that a special condition has arisen in the system. Then the Processor enters the Control State to deal with the interruption. Certain operations can be performed only in the Control State; these are listed in the Instruction List, Section 203:121.

The Program Level is the level in which a user's main program operates. Whenever the program calls upon a subroutine, the Processor switches automatically to the Subprogram Level. In the Program Level, direct reference can be made only to the top operand in the stack and to the Program Reference Table. The Subprogram Level permits direct reference to other stack locations, enabling the stack to be used for subroutine parameters and working storage. In both levels, reference can be made to elements of data arrays in core storage through the use of Descriptors (see Paragraph .123).

Subroutines can be nested, and a subroutine can call itself recursively. The level of nesting is limited only by the capacity of the stack. Before entering a subroutine, the original contents of the stack are marked, and all necessary parameters are loaded onto the top of the stack. Then a reference to the subroutine's Program Descriptor in the PRT causes placement of a return control word in the stack, effects entrance to the Subprogram Level, and transfers control to the first location of the subroutine addressed by the descriptor.

In the Word Mode, operands are considered to be 48-bit binary words. A parallel binary adder is used for arithmetic and comparison operations. The integer part is represented by 39 bits plus sign, and the octal exponent by 6 bits plus sign. Since the fixed-point part of a floating-point number is an integer rather than a fraction, fixed and floating-point operands can be intermixed without conversion, and numbers ranging from 10^{-46} to 10^{+69} can be represented.

Each program word consists of four 12-bit "syllables," and in the Word Mode each syllable can specify an operation to be performed, a 10-bit literal, or the address (relative to the start of the Program Reference Table) of an operand or descriptor. These functions are described in more detail in the Instruction List, Section 203:121.

In the Character Mode, each data word consists of eight 6-bit alphameric characters. All operations

.122 States, Levels, and Modes (Contd.)

are performed serially by character, and fields of up to 63 characters can be handled in a single operation. Although decimal addition and subtraction operators are included, the Character Mode is intended primarily for editing, scanning, comparison, and general data manipulation. Each Character Mode program syllable consists of a 6-bit repeat field and a 6-bit operation code. Functions of the Character Mode operators are described in the Instruction List, Section 202:121.

.123 Descriptors

A descriptor is a 48-bit word used for indirect addressing and/or for supplementing the program syllables in controlling the Processor's internal functions. A Program Descriptor specifies the size (up to 1,023 words) and current locations in both core and auxiliary storage of a program segment. A Data Descriptor specifies the base address of a data array or input-output area; this address can be indexed to locate a specific item in the array. If the address formed by indexing a Data Descriptor exceeds the array size limit (up to 1,023 words) specified in the descriptor, an interrupt occurs. This is a fairly effective means of automatic storage protection against coding errors and invalid data. Data Descriptors are also used to initiate all input-output operations. The general layouts of both Program and Data Descriptors are shown in Paragraphs .232 and .233 of this report section.

.124 Program Reference Tables (PRT)

The PRT is a relocatable core storage area of up to 1,023 words. One PRT is required for each program that is running simultaneously in a B 5500 system, including the Master Control Program. The PRT is used primarily for storage of Program and Data Descriptors, but it may also contain single operands such as counts and index values. The R register contains the base address of the PRT for the program being executed. The program syllables contain no direct addresses, but only 10-bit relative addresses which are added to the contents of the R register to access descriptors or operands anywhere in the PRT. The facts that the PRT is relocatable and that only relative addresses are used in program segments assure complete program relocatability and facilitate operation of the Master Control Program.

.125 Stacks

The stack is a list of operands and control words which are stored temporarily in the sequence in which they are to be processed. Physically, the stack consists of the Processor's A and B (arithmetic) registers and an area of core storage addressed by the S register. The stack operates on the "last in, first out" principle. An operand fetched by a program is placed in the A register; the previous contents of the A register (if any) are pushed down into the B register; and the previous contents of the B register (if any) are automatically transferred to the storage location addressed by the S register.

Push-up operations are automatically performed when an operator requires information from the stack; the process is the reverse of the push-down procedure just described. The address in the S register is automatically incremented by one before each push-down operation and decremented by one after each push-up. Each push-down operation requires 3 microseconds and each push-up requires 5 microseconds. The A and B registers have flip-flops which indicate the presence or absence of information, and push-ups and push-downs are performed only when necessary. The automatic temporary storage provided by the stack can significantly reduce the number of explicit fetch and store operations required in a program.

When multiprogramming is performed in a B 5500, each program has its own stack. Whenever an interrupt occurs, the contents of the A and B registers and all necessary control information are automatically pushed down into the appropriate stack in core storage before the Processor enters the Control State. The Master Control Program allocates storage to each stack, as well as to the Program Reference Table, program segments, data arrays, and input-output areas of each program. If the capacity of any program's stack is exceeded, an interrupt occurs, and the Master Control Program causes an error message to be printed and terminates the job.

.126 Interrupts

A comprehensive interrupt system is provided to inform the Processor when special conditions arise anywhere in the system. The occurrence of any one of 40 interrupt conditions causes a specific bit to be set in the Interrupt Register. Depending upon the nature of the interrupt condition, execution of the current program syllable may be completed or terminated immediately. Then the A and B registers and all necessary control information are pushed into the stack, the address of the associated interrupt handling routine is placed in the Interrupt Address Register, the Processor enters the Control State, and control is transferred to the Master Control Program for initiation of the required action.

All interrupt conditions are sampled continuously by the hardware and processed on a priority basis, so a high-priority interrupt condition (such as a storage parity error) can interrupt the servicing of a lower-priority interrupt condition (such as a free Input/Output Channel). For a detailed description of the interrupt facilities, see Paragraph .33 of this report section.

.127 Dual Processors

When two Processors are included in a B 5500 system, true multiprocessing is possible. The two Processors share the same Memory Modules, Input/Output Channels, and peripheral devices, but each Processor contains all the control and arithmetic facilities and operating registers required for independent program execution. Furthermore, through use of the interrupt facilities and the Master Control Program, each of the two Processors can effectively control multiprogramming operations. It is important to note, however, that only Processor 1 can operate in the Control State. Consequently, if an interrupt occurs in Processor 2,

(Contd.)

.127 Dual Processor (Contd.)

Processor 1 is forced to halt its processing in order to handle Processor 2's interrupt. By contrast, Processor 2 will be unaffected by interrupt conditions occurring in Processor 1. Either Processor Module (A or B) can be logical Processor 1, depending upon the setting of a Console switch.

.128 Performance

The performance of the B 5500 Processor is summarized in Paragraphs .41 and .42 of this section. Average times for the basic instructions are listed in Paragraph .41, and times to perform the standard central processor tasks are listed in Paragraph .42. In general, times for arithmetic, logical, and switching operations are based on use of the Word Mode with one-word operands, while times for format control are based on the Character Mode. Where either the Word or Character Mode can be used effectively, as in table lookups, both times are listed. There are usually numerous ways of coding a given task for the B 5500, and timing of internal operations is complex. The times listed here are for coding similar to that produced by the Extended ALGOL translator.

.129 Processor Improvements

The Processor used in B 5500 systems includes many improvements to the original B 5000 Processor design. Processor read access time — the total time required to transfer a word of information from memory to the Processor or to an Input/Output Channel — has been reduced from 6 to 4 microseconds. Syllable and word fetch-overlap techniques have been improved, and the execution times of the most frequently-used operators have been reduced. For example, the execution time of the logical AND and logical OR operators has been reduced from 17 to 3 microseconds. In addition, stack adjustment times have been improved, permitting push-down operations to be performed in 3 microseconds instead of 4, and push-up operations to be performed in 5 microseconds instead of 8.

Nineteen new operators have been added to the instruction repertoire to speed up Master Control Program functions such as automatic storage allocation and program segment overlay control. Time-consuming algorithms formerly required to switch from Word Mode to Character Mode have been completely eliminated. It is now possible to embed Character Mode coding directly in-line with Word Mode coding. All of these improvements in the Processor's logic design have been added to enable the compilers to generate more efficient object programs and to permit the Master Control Program to perform its program-segment switching and multiprogramming control routines more quickly and more effectively.

.13 Availability: . . . . immediate.

.14 First Delivery: . . . . . April 1963 for B 5000 Processor.
December 1964 for B 5500 Processor.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add-subtract			
	Word Mode:	automatic	binary	39 or 78 bits and sign.
	Character Mode:	automatic	decimal	1 to 63 digits.
	Multiply			
	Short:	automatic	binary	39 or 78 bits and sign.
	Long:	none.		
	Divide			
	No remainder:	automatic*		39 or 78 bits and sign.
	Remainder:	none*		
.212	Floating point —			
	Add-subtract:	automatic	binary	39 or 78 bits for fraction; 6 bits for exponent.
	Multiply:	automatic		
	Divide:	automatic		
.213	Boolean —			
	AND:	automatic	binary	47 bits.
	Inclusive OR:	automatic		
	Equivalence:	automatic		
	Negate:	automatic		
.214	Comparison —			
	Numbers:	automatic		1 full or partial word, or 1 to 63 characters.
	Absolute:	none.		
	Letters:	automatic		
	Mixed:	automatic		
	Collating sequence:	see Data Code Table, Section 203:141.		

* Either quotient or remainder can be retained, but not both; single-length division is rounded.

		Provision	From	To	Size
.215	Code translation:	none.			
.216	Radix conversion:	automatic	decimal	binary	1 to 8 dec. digits.
		automatic	binary	decimal	1 word.

.217 Edit format: . . . . no automatic facilities; editing is accomplished by strings of program syllables in the Character Mode.

.218 Table lookup: . . . . . . the Link List Lookup operator compares the contents of the A register to a linked list of data; a ≥ condition sets the A register to the address of the "found" data item.

.219 Others: . . . . see Instruction List, Section 203:121.

.22 Special Cases of Operands

.221 Negative numbers —

Word Mode: . . . . . . absolute value with sign bit of 1.

Character Mode: . . . absolute value, with zone bit of low-order character used as sign.

.222 Zero: . . . . +0 and -0; no difference in arithmetic or comparisons.

.223 Operand size determination:. . . . . fixed at 1 or 2 words in Word Mode; variable from 1 to 63 characters (specified by repeat field) in Character Mode.

.23 Instruction Formats

.231 Instruction structure: . four 12-bit syllables per word.

.232 Instruction layout —

Word Mode Syllable:

Name	Op. code or data	Syllable type
Size (bits)	10	2

Character Mode Syllable:

Name	Repeat field	Op. code
Size (bits)	6	6

.233 Instruction parts —

Name	Purpose
Syllable type:	denotes whether a Word Mode syllable is an operator, literal, Operand Call, or Descriptor Call.
Op. code or data (Word Mode):	(1) specifies operation to be performed upon data in A and/or B register; or (2) specifies a 10-bit literal value to be placed in A register; or (3) specifies the address (when modified by contents of R register) of an operand or descriptor to be placed in the A register and examined.
Op. code (Character Mode): .	specifies operation to be performed.
Repeat field:	specifies number of times (up to 63) the operation shall be repeated; or a 6-bit literal character.

.2331 Descriptor parts —

Name	Purpose
Flag:	denotes type of word: descriptor or operand.
I/D:	denotes type of descriptor.
Presence:	denotes whether program segment or data is in core storage.
Mode:	denotes Word or Character Mode syllable.
Parameter:	indicates that parameters are required for the program segment.
Size:	number of words in segment, array, or input-output load.
Drum or disc address:	drum or disc location of segment.
Core address: . .	core location of first word of a segment, array, or input-output area.
Unit:	input-output device designation.
Control:	detailed specifications for input or output operation, error indications or drum address.

Program Descriptor:

Name	Flag	I/D	Presence	Mode	Parameter	Size	Disc/Drum address	Core address
Size (bits)	1	2	1	1	1	10	15	15

Data and Input-Output Descriptors:

Name	Flag	I/D	Presence	Unit	Size	Control	Core address
Size (bits)	1	1	1	5	10	15	15

(Contd.)

.234 Basic address structure: one 10-bit address per Operand Call and Descriptor Call syllable; no address is specified in an Operator syllable.

.235 Literals —

	Word Mode	Character Mode
Arithmetic:	10 bits	none.
Comparisons and tests:	10 bits	1 character.
Incrementing modifiers:	10 bits	none.

.236 Directly addressed operands —
Internal storage type: core.
Minimum size: 1 word.
Maximum size: 63 words.
Volume accessible: 1,024 words.
Increased address capacity: 32,786 words, using indexing and/or indirect addressing as described in following entries.

.237 Address indexing —
.2371 Number of methods: 3.
.2372 Names: R-register indexing (occurs whenever a program syllable is an Operand Call or Descriptor Call).
B-register indexing (occurs only when the word brought to the A register by R-register indexing is found to be a Data Descriptor for an array, or when the "index" operator is executed).
R/F-register indexing (occurs when a "store" operator is given and the A register contains an operand.
.2373 Indexing rules —
R-register indexing: add the 10 high-order bits of the Operand Call or Descriptor Call syllable to the contents of the R register and store the resulting address in the M register; bring the word found at this address to the A register.
B-register indexing: add the 10 low-order bits of the B register's contents to the 15 low-order bits of the Data Descriptor in the A register.
R/F-Register indexing: add the 10 low-order bits of the operand in the A register to the contents of the R register (if in Program Level) or the F register (if in Subprogram Level); store contents of B register at the resulting address.
.2374 Index specification: none required; see .2372 above.
.2375 Number of potential indexers: 3: R, B, and F registers.
.2376 Addresses which can be indexed —

Type of Address	Application
Descriptors and operands in Program Reference Table, using R-register indexing:	facilitates relocation of programs.
Data items in arrays, using B-register indexing:	specifies particular element of an array whose base address is in the Data Descriptor.
Temporary storage areas for subroutines, using F register indexing:	facilitates dynamic storage allocation and recursion.

.2377 Cumulative indexing: when an Operand Call syllable references a Data Descriptor, R and B-register indexing occur successively.
.2378 Combined index and step: no.

.238 Indirect addressing —
.2381 Recursive: no.
.2382 Designation: occurs automatically whenever an Operand Call syllable references a Data Descriptor: contents of the location specified by the descriptor, indexed by contents of the B register, are brought into the A register.
.2384 Indexing with indirect addressing: B-register indexing occurs after indirect addressing; see .2382 above.

.239 Stepping: R register, in Character Mode only.
.2391 Specification of increment: in repeat field of the "increase tally" syllable.
.2392 Increment sign: always positive.
.2393 Size of increment: 0 to 63.
.2394 End value: no direct test available.
.2395 Combined step and test: no.

.24 Special Processor Storage

Register Name	Size in Bits	Word Mode Usage	Character Mode Usage
P	48	holds program word being processed	same as Word Mode.
C	15	sequence counter; contains address of next program word	same as Word Mode.
T	12	holds program syllable being executed	same as Word Mode.

.24 Special Processor Storage (Contd.)

Register Name	Size in Bits	Word Mode Usage	Character Mode Usage
L	2	denotes position in word in P of the syllable in T; overflows into C	same as Word Mode.
A	48*	arithmetic register; top location in stack	source register for data to be edited.
M	15	address of storage location associated with A register	same as Word Mode.
G	3	generally not used	addresses a character within the A register; overflows into M.
H	3	generally not used	addresses a bit within the character addressed by G.
B	48*	arithmetic register; second location in stack	destination register for edited data.
S	15	address of storage location associated with B register	same as Word Mode.
K	3	generally not used	addresses a character within the B register; overflows into S.
V	3	generally not used	addresses a bit within the character addressed by K.
F	15	contains stack location where subroutine return point is stored	same as Word Mode.
R	9	contains base location of Program Reference Table	tally register for counting.
X	39	extension of A or B register	contains a loop control word.

* A and B registers have associated one-bit flip-flops to indicate the presence or absence of data.

Note: There are other Processor registers which serve specific logical functions; only the registers directly associated with Word and Character Mode operations are listed here.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . . 1.

.312 Arrangement: . . . . . . 1 sequence counter per Processor (C register).

.313 Precedence rule: . . . . when 2 Processors are used, they operate independently.

.314 Special sub-sequence counters —

Name	Purpose
L register:	specifies which syllable of word in P register is being executed; overflows into C register.
G, H registers: . . .	locate individual character and bit of word in A register.
K, V registers: . . .	locate individual character and bit of word in B register.

.315 Sequence control step size: . . . . 1 word for C register; 1 syllable for L register.

.316 Accessibility to routines: . . . . contents of C and L registers can be stored and reloaded by instructions.

.317 Permanent or optional modifier: . . no.

.32 Look-ahead: . . . . fetch of next syllable and program word is accomplished during execution of current syllable.

.33 Interruption

.331 Possible causes —

I/O units: . . . . unit free, error, malfunction, end of file, write lockout.

I/O controllers: . . . . channel free.

Storage access: . . . . drum or disc write lockout, parity error, malfunction, stack overflow, invalid address, flag bit (end of a data array), presence (reference to information not in core storage).

Processor errors: . . integer overflow, exponent overflow, exponent underflow, division by zero, invalid index.

Other: . . . . time interval, keyboard request, Processor B busy, program release (I/O area free to receive or transfer data), continuity bit (designating multiple I/O areas).

.332 Control by routine: . . . none; all possible interrupts are sampled continuously and simultaneously, and they are processed according to a fixed priority list.

.333 Operator control: . . . . none; see .332 above.

.334 Interruption conditions: . . . . none; see .332 above.

.335 Interruption process —

Disabling interruption: . . . . automatic; Processor enters Control State, and further interruptions set Interrupt Register bits which remain set until interrogated.

Registers saved: . . . B register, A register (Word Mode only), and specially-formed control words containing the settings of registers M, R, C, F, K, V, G, L, and S; all are pushed into the stack.

Destination: . . . . . . enter Control State and transfer to fixed location.

(Contd.)

.336 Control methods —
Determine cause: . . . "interrogate Interrupt Register" instruction transfers control to location corresponding to the interrupt bit that is set.
Enable interruption: . automatic when control is returned to Normal State.

.34 Multiprogramming

.341 Method of control: . . . interruption and/or two separate Processors; usually controlled by Master Control Program (MCP).
.342 Maximum number of programs: . . . . limited by hardware and program requirements.
.343 Precedence rules: . . . assigned priorities.
.344 Program protection —
Storage: . . . . storage areas are assigned by Master Control Program. There is no positive protection, but an interrupt occurs if a data address formed by indexing exceeds the area assigned the array by the Data Descriptor, or if a referenced program segment or data array is not present in core storage.
I/O units: . . . . assigned by Master Control Program; no positive protection.
Maximum separate sets: . . . . limited by system configuration.

.35 Multisequencing: . . . . possible when two Processors are used, but the facility is not incorporated into the Master Control Program.

.36 Multiprocessing: . . . . maximum of 2 independent Processors per system.

.4 PROCESSOR SPEEDS*

.41 Instruction Times in Microseconds

.411 Fixed-point (average)

	Single length	Double length
Add-subtract —		
Word Mode:	1	15
Character Mode:	13 + 4D	—
Multiply:	32	133
Divide:	36	159

.412 Floating-point (average)

	Single length	Double length
Add-subtract:	4	24
Multiply:	32	133
Divide:	36	159

* All B 5500 Processor timings in this report assume the use of B 461 4-microsecond Memory Modules, currently the standard memory units with B 5500 systems.
C = operand length in characters.
D = operand length in decimal digits.

.413 Additional allowance for —
Recomplementing: . . 2.
Indexing: . . . . see Paragraph .419.
Loading of registers: see Paragraph .419.
.414 Control:
Word Mode —
Compare: . . . . . . 2.
Branch: . . . . 5.
Character Mode —
Compare: . . . . 10+3C.
Branch: . . . . 9 to 20.
.415 Counter control (Character Mode) —
Step: . . . . 2 to 62.
Test: . . . . 2 to 10.
.416 Edit: . . . . no automatic facilities.
.417 Convert —
Decimal to binary: . . 37 + 2D.
Binary to decimal: . . 43+2D.
.418 Shift: . . . . no automatic facilities.
.419 Others:
Fetching an operand —
Single value from PRT: . . . . 5.
Single value, using descriptor: . . . . . 10.
Array element, using descriptor: . 11 minimum.

Storing an operand —
Single value into PRT: . . . . 3.
Single value, using descriptor: . . . . . 3.
Array element, using descriptor: . 13 minimum.

Fetching a program word: . . . . 4.
Note: fetch time is completely overlapped if execution time of last syllable in preceding word exceeds 4 μsec.

Fetching a program syllable: . . . . 0.

Stack adjustment —
Push-down: . . . . . . 3.
Push-up: . . . . 5.

.42 Processor Performance in Microseconds

.421 For typical tasks

	Fixed point	Floating point
All operands and results in core storage —		
c = a + b:	17	17
b = a + b:	17	17
Sum N items, per item:	7	7
c = ab:	44	44
c = a/b:	76	76
All operands and results in optimum stack locations —		
c = a + b: . . .	2	2
b = a + b:	2	2
Sum N items, per item:	7	7
c + ab:	30	30
c = a/b:	61	61

.422 For arrays of data

	Fixed point	Floating point
$c_i = a_i + b_j$:	85	85
$b_j = a_i + b_j$:	85	85
Sum N items, per item:	56	56
$c = c + a_i b_j$:	112	112

.423 Branch based on comparison (Word Mode) —
- Numberic data: . . . 114.
- Alphabetic data:. . . 114.

.424 Switching (Word Mode) –
- Unchecked: . . . . 39.
- Checked: . . . . 66.
- List search: . . . . . . 16 + 50N.

.425 Format control, per character:
- Unpack —
  - Mathematical: . . . . 18.
  - Commercial:. . . . . 9.
- Compose —
  - Mathematical: . . . . 23.
  - Commercial:. . . . . 37.

.426 Table lookup, per comparison:
- Word Mode —
  - For a match:. . . . . 50.
  - For least or greatest: . . . . . . 56.
  - For interpolation point:. . . . . 44.
- Character Mode —
  - For a match: . . . . 46 + 4C.
  - For least or greatest: . . . . . . 50 + 4C.
  - For interpolation point:. . . . . 46 + 4C.

.427 Bit indicators:
- Word Mode —
  - Set bit in separate location:. . . . . . . 7.
  - Set bit in pattern:. . 17.
  - Test bit in separate location:. . . . . . . 14.
  - Test bit in pattern:. 21.
  - Test AND for B bits: . . . . 27.
  - Test OR for B bits:. 27.

.428 Moving, for N words:
- Word Mode —
  - Using programmed loop: . . . . 7 + 50N.
  - Using straight-line coding:. . . . . 10N.
- Character Mode —
  - Within same Memory Module: 24 + 4N.
  - Between two Memory Modules: . . . . . 24 + 4N.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Exponent overflow:	check	interrupt.
Exponent underflow:	check	interrupt.
Integer overflow:	check	interrupt.
Zero divisor	check	interrupt.
Invalid operation:	programmed check	error routine.
Arithmetic error:	none.	
Invalid address:	check	interrupt.
Receipt of data:	parity check	interrupt.
Dispatch of data:	send parity bit.	
Invalid index:	check	interrupt.
Stack overflow:	check	interrupt.

Note: "Interrupt" indicates that the Processor sets a specific bit in the Interrupt Register and enters the Control State; the Master Control Program then deals with the error condition (see Paragraph 203:191.44).

CONSOLE

.1 GENERAL

.11 Identity: . . . . B 5310 Console.

.12 Associated Units: . . . . Supervisory Printer and Keyboard.
Distribution and Display Panel.

.13 Description

The Console of the B 5500 Information Processing System consists of a simple, elongated L-shaped desk containing a row of basic controls and indicators along a narrow ridge at the rear of the desk. On the short end of the L is the Supervisory Printer and Keyboard, a modified electric typewriter used for direct communication between the operator and the B 5500's Master Control Program (MCP); Paragraph .6 describes the characteristics of this unit.

Simplicity in system operation has clearly been a goal in the design of the B 5500. The few controls on the Console reflect this purpose. However, on-line program debugging and tracing are made impractical, if not impossible, by the lack of register displays and of direct methods for data insertion. Power on-off and loading operations are the only control facilities provided at the Console.

The normally-covered cabinet that houses the Display and Distribution Panel provides binary displays of all processor and Input-Output Channel registers in the form of button-lamps that can also be used for entry of data. Buttons are also provided to clear all or selected registers. The Display and Distribution Panel is normally used only for system maintenance purposes, although its use is in no way restricted to this purpose.

The System Control section of the B 5500 is an internal synchronization and switching network that also contains the master clock, a 1/60-of-a-second interval timer, and an interrupt system. The interval timer is used continuously by the Master Control Program in its compilation of logging and accounting information for eventual printing on the Supervisory Printer and Keyboard.

.2 CONTROLS

.21 Power

Name	Form	Comment
Power On:	button	initiates power-on cycle for all units.
Power Off:	button	initiates power-off cycle for all units.

.22 Connections: . . . . . . none.

.23 Stops and Restarts

Name	Form	Comment
Halt:	button	places Processor(s) in an idle condition; they can be restarted only by a subsequent load operation.

.24 Stepping: . . . . none.

.25 Resets: . . . . none.

.26 Loading

Name	Form	Comment
Load:	button	loads a program (usually the MCP) into core storage, beginning at location 00016, and begins processing it.
Card Load Select:	2-way button	selects Card Reader or Disk File/Drum Storage as input device for load operations.

.27 Sense Switches: . . . . . none.

.3 DISPLAY

.31 Alarms

Name	Form	Condition Indicated
Memory Check:	red lamp	storage parity error.

.32 Conditions

Name	Form	Condition Indicated
Power On:	green lamp	power on.
Halt:	redlamp	Processor(s) in idle condition.
Card Load Select:	yellow lamp	Card Reader selected for load operation.
Not Ready:	white lamp	one or more units not available for normal use.
A Normal:	yellow lamp	Processor A in normal state.
A Control:	yellow lamp	Processor A in control state.
B Normal:	yellow lamp	Processor B in normal state.
B Control:	yellow lamp	Processor B in control state.

.33 Control Registers: . . . no display provided at Console.

.34 Storage: . . . . no display provided.

.4 ENTRY OF DATA: . . . no Console provision; Supervisory Printer keyboard can be used under program control.

.5 CONVENIENCE

.51 Communication: . . . . . none.

.52 Clock: . . . . none (interval timer provides no visual display of time).

.53 Desk Space: . . . . Console provides ample work space at desk-top height.

.54 View: . . . . operator seated at Console has unobstructed view in all directions.

.6 INPUT-OUTPUT UNIT

.61 Identity: . . . . Supervisory Printer and Keyboard.

.62 Description

The Supervisory Printer and Keyboard is a modified single-case Smith-Corona Marchant electric typewriter. It is used for two-way communication between the operator and the B 5500 system. The operator can use the keyboard to type inquiries and instructions to the Master Control Program. Under control of the Master Control Program, in turn, the printer can type instructions to the Operator and answers to his inquiries. An Input-Output Channel is used for information flow to and from the Supervisory Printer. Data transmission is serial by character.

Since the Supervisory Printer functions as an input-output device, under direct control of an Input-Output Channel, processing is not halted during the printer's operations.

The Supervisory Printer prints one character at a time at a spacing of ten characters per inch horizontally and three or six lines per inch vertically. Continuous fanfold sprocket-punched stationery is used; its width may be up to 12 inches.

The keyboard contains the standard B 5500 set of 63 characters. The following controls are located on the keyboard.

Name	Form	Comment
Local:	key	disconnects unit from system and unlocks keyboard for normal typing.
Remote:	key	locks keyboard until Ready light is on.
Input Request:	key	sets Keyboard Request interrupt bit in the B 5500.
End of Input:	key	transfers a group mark to storage as the last character of a message.
Error:	key	transfers a group mark with incorrect parity, signifying that a typing error was made.
Ready:	lamp	indicates that messages can be entered via the keyboard.

.63 Performance

Input: . . . . limited by manual typing speed.
Output: . . . . 10 characters per second.

INPUT-OUTPUT: B 122 CARD READER

.1 GENERAL

.11 Identity: . . . . B 122 Card Reader.

.12 Description

The B 122 Card Reader reads 80-column punched cards of standard or postcard thickness at a maximum rate of 200 cards per minute. Reading is performed by 13 photoelectric cells (one for timing), serially by column and parallel by bit. The time required to read each card, normally 300 milliseconds, is increased by 15 milliseconds when the reader is used intermittently rather than at its peak rate.

The B 122 Card Reader automatically translates Hollerith code into Burroughs Common Language (BCL) code before transferring the information to the Input/Output Channel control. The I/O Channel acts as an input buffer and allows computation to proceed independently of the card read operation. The Input/Output Channel being used is dedicated to the card read operation until the last card column has been read. A maximum of two card readers, in any combination of models (see Report Section 202:072 for additional card readers), can be connected to a B 5500 through up to four "floating" Input/Output Channels.

The card read operation is initiated when the B 5500 Processor sends a Card Read Input/Output Descriptor from its A register to the D register of the I/O control unit. The control unit selects an idle I/O channel and initiates the card read command. Single cards are read either in alphameric mode (and then decoded by the card reader into 6-bit alphameric characters) or in the column binary mode. Groups of eight 6-bit characters, or four 12-bit binary card column representations, are assembled into a 48-bit B 5500 word in the W register of the control unit, and then transferred to a Descriptor-specified address in core storage.

After the 80th card column has been read and the last input word has been transferred to core storage, a Result Descriptor is constructed that indicates the results of the card read operation by means of various bit settings. End-of-file, busy-status, and not-ready conditions, as well as invalid-character and read-check errors, are indicated in the Result Descriptor for subsequent testing by the Master Control Program. The input storage address contained in the I/O Descriptor is checked for validity and proper parity, and error-condition bits are set in the Result Descriptor when necessary. Card jams and full-stacker conditions also set testable error indicators.

Input data transfers from the I/O control unit to the Memory Module consume only 40 microseconds (or 80 microseconds in binary mode) per card, and in no way inhibit the concurrent performance of the Processor. The sole function of the Processor in a card read operation is to issue an Initiate Input-Output command, thereby causing the Descriptor contained in its A register to be transferred to the I/O control unit. The Processor then proceeds independently until a bit is set in the External Interrupt Register, which interrupts the Processor and indicates that the card read operation has been terminated. Interrupt bits are also set if another Data or I/O Descriptor references an area of memory currently being filled by the card read operation.

Cards are fed by a pinch-roller mechanism on demand from the I/O control unit. The input hopper has a capacity of 500 cards and can be refilled while cards are being read. The single stacker provided also holds 500 cards, but it cannot be emptied while the unit is in operation. Stacker select options are not available.

Unlike the Burroughs card readers described on page 203:072.100, there are no optional features available for the B 122 Card Reader. First delivery of the B 122 occurred late in 1961. It is currently available for immediate delivery.

INPUT-OUTPUT: B 123/124/129 CARD READERS

.1 GENERAL

.11 Identity: . . . . B 123 Card Reader.
B 124 Card Reader.
B 129 Card Reader.

.12 Description

The Burroughs B 123, B 124, and B 129 Card Readers provide punched card reading speeds of 475, 800, and 1400 cards per minute, respectively. Except for this considerable difference in rated speeds, the three readers are essentially the same. Any of these readers, and the B 122 Card Reader described in the previous report section, can be paired in any combination for use with a B 5500 system; the maximum number of card readers per system is two.

The B 123, B 124, and B 129 Card Readers can read standard or postcard thickness punched cards of 51, 60, 66, or 80 columns. The standard types of scored cards are acceptable when the stubs are removed. An immediate-access clutch provides demand feeding of the cards. Photoelectric reading by column initiates the automatic transfer of data from the card to a code translator within the card reader, en route to the input/output control unit. (No code translation occurs when the reader is operating in the alternative binary mode.)

One of up to four "floating" Input/Output Channels is selected for the card read operation by the I/O control unit. The channel that is selected remains dedicated to the card read process until the last card column has been read. However, the Processor is entirely free throughout the reading operation, and the Memory Module to which input data is transferred is accessed for a total of only 40 microseconds (80 microseconds in binary mode) during the entire card read cycle.

The card read operation is initiated when the B 5500 Processor sends a Card Read Input-Output Descriptor from its A register to the D register of the I/O control unit. The control unit selects an idle I/O Channel and initiates the card read command. Single cards are read either in the alphameric or column binary mode. Groups of eight 6-bit characters, or four 12-bit binary card column representations, are assembled into a 48-bit B 5500 word in the W register of the control unit, and then transferred to a Descriptor-specified address in core storage.

After the 80th card column has been read and the last input word has been transferred to core storage, a Result Descriptor is constructed that indicates the results of the card read operation by means of various bit settings. End-of-file, busy status, and not-ready conditions, as well as invalid character and read-check errors, are indicated in the Result Descriptor for subsequent testing by the Master Control Program. The input storage address contained in the I/O Descriptor is checked for validity and proper parity, and error condition bits are set in the Result Descriptor when necessary. Card jams and full-stacker conditions also set testable error indicators.

The sole function of the Processor in a card read operation is to issue an Initiate Input-Output command, therby causing the Descriptor contained in its A register to be transferred to the I/O control unit. The Processor then proceeds independently until a bit is set in the External Interrupt Register, indicating that the card read operation has been terminated. Interrupt bits are also set if another Data or I/O Descriptor references an area of memory currently being filled by the card read operation.

Since the B 123, B 124, and B 129 Card Readers make use of immediate-access clutching, and since the read operations proceed independently of the Processor, the rated speeds of 475, 800, and 1400 cards per minute will always be achieved, provided that successive Initiate I/O instructions are issued within the readers' read cycle times. The read cycle times for the B 123, B 124, and B 129 Card Readers are 126, 75, and 42.8 milliseconds, respectively.

Cards are fed by a belt-drive mechanism past the stack of 13 photoelectric read cells (one for timing) and transported to the single stacker. Both the hopper and the stacker have capacities of 2,400 cards and can be filled and emptied while the card reader is in operation. Should a jam occur in the card transport device, the unit will halt with a maximum of two cards jammed, and a bit will be set in the Result Descriptor. An empty hopper condition sets the not-ready bit and, in the B 129 Card Reader, turns off the unit's card transport mechanism.

The availability of the B 123, B 124 and B 129 Card Readers is from three to four months. First deliveries of the prototype B 124 Card Reader occurred during the last quarter of 1963.

INPUT-OUTPUT: B 303/304 CARD PUNCHES

.1 GENERAL

.11 Identity: . . . . B 303 Card Punch.
B 304 Card Punch.

.12 Description

The B 303 and B 304 Card Punches operate at maximum rates of 100 and 300 cards per minute, respectively. Only one card punch can be connected to a B 5500 system. Standard or postcard thickness 80-column cards can be punched (but not both thicknesses during the same run). Pre-scribed and/or pre-punched cards can also be punched if the post-punch checking device is inactivated by the operator. Formatting of the punched card is controlled exclusively by the stored program.

Cards are punched by a single row of 80 die punches, one row at a time. An 80-bit, one-row buffer in the punch unit is used to compare the row just punched with the input row in the buffer. Cards can be punched in alphameric or binary mode. In the alphameric mode, the punch unit translates the BCD character codes from the B 5500 into standard Hollerith card code. In the binary mode, data is punched exactly as it appears when transferred from the I/O Channel.

The card punch operation is initiated when the Processor sends a Card Punch I/O Descriptor to the I/O control unit. From that point on, the Processor is entirely disassociated from the punching operation and is free to continue processing. The I/O control unit receives the address of the output data in the B 5500's Memory Module and selects the highest-priority free I/O Channel. The I/O control unit then accesses the designated Memory Module and fetches a 48-bit data word for temporary storage in the I/O Channel's one-word buffer (W register). This word contains either eight 6-bit alphameric characters or four 12-bit binary data representations. The data word is then sent to the card punch, one character at a time, and assembled for punching. Ten accesses to the Memory Module (20 in binary mode) are required before the card can be punched. The Memory Module being accessed is tied up for a total of either 40 or 80 microseconds for each card punch cycle. The I/O Channel is completely dedicated to the punching process once it senses the Initiate I/O instruction. When the card punch cycle has been completed, a specific bit is set in the External Interrupt Register.

After each card has been punched, an I/O Result Descriptor is constructed with bit settings that indicate the results of the punching operation. Improper or invalid punches set the punch error indicator, and data-transfer parity errors set a specific indicator. The "not-ready" bit is set for any of the following conditions: empty hopper, feed check, full stackers, punch die not in place, and power off. The address of the output data in the Memory Module is checked for validity and proper parity. If the punch unit is found to be currently assigned to another I/O Channel, a "busy" bit is set in the Result Descriptor. The External Interrupt Register is examined continuously by the Master Control Program. When it finds that an input-output operation has ended, the MCP examines the I/O Result Descriptor to determine whether or not further action is required.

From the punch unit's hopper to stacker, cards are transported by positive-action pinch rollers. Hopper and stacker capacities of the B 303 Card Punch are 800 cards each. The B 304 Card Punch is equipped with three stackers: primary, auxiliary, and error. The primary stacker can hold 3,000 cards, the same capacity as the unit's hopper. Error cards are segregated in the error stacker, holding 750 cards. The 850-card auxiliary stacker is normally used as an alternative to the primary stacker, controlled by a switch on the control panel.

Significant timing considerations and a comparison of the B 303 and B 304 Card Punches are provided in Table I.

TABLE I: B 303/B 304 CARD PUNCH TIMING FACTORS

Model:	B 303	B 304
Rated speed	100 cpm	300 cpm
Total card cycle time in synchronous mode	600 msec	200 msec
Overhead in asynchronous mode	50 msec	200 msec
Maximum punching rate in asynchronous mode	92.3 cpm	150 cpm

STANDARD EDP REPORTS

INPUT-OUTPUT: B 141 PAPER TAPE READER

.1 GENERAL

.11 Identity: . . . . B 141 Paper Tape Reader.
B 5410 Paper Tape Adapter.
B 142 Input Code Translator.

.12 Description

The B 141 Paper Tape Reader reads data from punched paper or metalized Mylar tape at speeds of either 500 or 1,000 characters per second. Up to two B 141's can be connected to a B 5500 system via the B 5410 Paper Tape Adapter. A maximum of three paper tape readers and punches (see Section 202:075) can be connected, in combination, to one system. The B 141 Paper Tape Reader can accommodate 5, 6, 7, or 8-level tape, as selected by the operator. The standard tape code is the 8-level Burroughs Common Language (BCL) paper tape code (see Data Code Table, Section 203:141).

The optional B 142 Input Code Translator allows automatic translation of any code (5, 6, 7, or 8-level) to any one of the 64 six-bit BCL characters. If the B 142 is not used, programmed translation will be required unless the tape is punched in the 8-level BCL code.

The operator can enable different paper tape channels to be read by use of a plugboard which is supplied as part of the B 141 Reader. A code punched in all channels (whether 6, 7, or 8-level tape) is considered a delete code and is not transferred to the Processor when operating without a translator.

Reading speed is 500 or 1,000 characters per second. Reading is entirely buffered, since it is performed by the Input/Output Channel control, independently of the B 5500 Processor. Fanfold tape, whether in strips or in reels, and metalized Mylar tape must be read at 500 characters per second; other punched tape can be read at either speed. Start and stop times are 5 and 20 milliseconds, respectively. The reader can stop on the stop character or between characters at both high and low speeds.

A minimum of four feet of tape leader is required when reels are used, and at least one foot is needed for strip reading. Tape widths of 0.675, 0.875, or 1.000 inch can be handled interchangeably. Reel diameters of either 5.5 or 7 inches can be accommodated. Beginning- and end-of-tape indicators are sensed by means of adhesive opaque strips on the tape being read. If the tape breaks, the tape reel motors are shut down automatically.

In addition to its use as an on-line input device to the B 5500 system, the B 141 Paper Tape Reader can be used off-line to check punched tape for parity errors. The B 141 will stop when improper parity is detected.

The Processor initiates the read operation by transferring a Paper Tape Input Descriptor from its A register to the I/O control unit by means of an Initiate I/O instruction. The processor is subsequently entirely free of the input operation. The Input Descriptor contains information such as the reader unit designation, the number of 48-bit words that are to be read, the input address in a Memory Module, and the type of paper tape reader operation to be performed: read, space, or rewind.

The I/O control unit then selects the highest-priority free I/O Channel and activates the reader. Input data is transferred to the I/O Channel control's W register and assembled into 48-bit words. When the W register is full, the designated Memory Module is accessed and the data word is transferred. The Memory Module is occupied for 4 microseconds for each word transferred. The maximum number of input words that can be transferred to core storage in one read operation is 1,023.

When the read operation is terminated, a specific indicator bit is set in the External Interrupt Register, and an I/O Result Descriptor is constructed. The Result Descriptor indicates, with bit settings, the results of the just-completed read operation. These bits are then tested by the Master Control Program to determine whether any further action is necessary. If the B 141 Paper Tape Reader was discovered to be not-ready or busy, specific indicator bits are set. Likewise, if the I/O Descriptor's address has improper parity when transferred from core storage to the I/O control unit, or if data parity errors have occurred in the transfer of data from the reader to the I/O control unit, other bit indicators are set.

.13 Availability: . . . . 3 to 4 months.

.14 First Delivery: . . . . . September, 1963.

INPUT-OUTPUT: B 341 PAPER TAPE PUNCH

.1 GENERAL

.11 Identity: . . . . B 341 Paper Tape Punch.
B 5410 Paper Tape Adapter.
B 342 Output Code Translator.

.12 Description

The B 341 is basically a Teletype paper tape punch that is capable of punching data from a B 5500 Memory Module at a "minimum" speed of 100 characters per second, spaced 10 characters per inch. The B 341 can punch either 5, 6, 7, or 8-level tape, according to operator selection. The standard code punched is the 8-level Burroughs Common Language (BCL) paper tape code. Up to two B 341's can be connected to a B 5500 system via the B 5410 Paper Tape Adapter. A maximum of three paper tape punches and readers can be connected, in combination, to one system.

The optional B 342 Output Code Translator allows automatic translation of the 64 six-bit BCL characters that can be sent from the Memory Module to the punch into any 5, 6, 7, or 8-level paper tape code. If the Code Translator is not installed, the 6-bit BCL characters from core storage are punched in the 8-level BCL paper tape code (see Data Code Table, Section 203:141).

The level of paper tape punching is operator-selectable. The choice between 5, 6, 7, or 8-level punching is made possible through the use of a plugboard that is supplied as part of the B 341 Punch.

The B 341 is capable of punching data into several forms of tape, such as oiled or dry paper tape, laminated fiber tape, and metalized or laminated Mylar tape. Tape widths can be either 0.675, 0.875, or 1.000 inch. The size of the supply reel can range up to 8 inches in diameter, and the take-up reel can be either 5.5 or 7 inches in diameter. Take-up reels are not required during the punching process. When the tape supply reel has 35 feet or less remaining on it, an end-of-tape signal is produced to alert the Processor.

The B 5500 Processor initiates the punch operation by transferring a Paper Tape Write Output Descriptor from its A register to the I/O control unit by means of an Initiate I/O instruction. The Processor is free during the remainder of the completely-buffered punching operation. The Output Descriptor contains information such as punch unit designation, starting address of the output data in a Memory Module, indication to perform a tape feed operation only (punching all holes), specification of binary or alphameric punching, and an output word counter. If punching is specified as binary, the word counter limits the punching operation to from 1 to 1,023 48-bit words of output data. In the alphameric punching mode, the word counter specifies the maximum number of words that can be punched, but allows for earlier termination of punching if an end-of-file character is recognized.

The I/O control unit selects one of the four possible "floating" I/O Channels and initiates the transfer of data from the designated Memory Module to the B 341 Punch. Data is transferred in 48-bit words. Each memory access occupies the Memory Module for four microseconds. The I/O Channel is dedicated to the punching process for the duration of the output operation, but the associated Memory Module can be accessed by the Processor(s) and other I/O Channels during the tape punching operation.

When the punch operation is terminated, a specific indicator bit is set in the External Interrupt Register and an I/O Result Descriptor is constructed. The Result Descriptor indicates, with bit settings, the results of the just-completed punch operation. These bits are then tested by the Master Control Program to determine whether any further action is necessary. If the B 341 Paper Tape Punch was discovered to be not-ready or busy, or if the physical end-of-tape marker has been sensed, specific indicator bits are set. Likewise, if the I/O Descriptor's address has improper parity when transferred from core storage to the I/O control unit, or if data parity errors have occurred in the transfer of data from the I/O control unit to the punch unit, other bit indicators are set.

INPUT-OUTPUT: B 320/321/325 LINE PRINTERS

.1 GENERAL

.11 Identity: .... B 320 Line Printer.
B 321 Line Printer.
B 325 Line Printer.

.12 Description

The B 321 Line Printer prints at a maximum rate of 700 single-spaced or 650 double-spaced alphameric lines per minute. When average line spacing occurs at one-inch intervals, the speed is reduced to about 540 lines per minute. Sixty-four characters (10 numeric, 26 alphabetic, and 28 special symbols) can be printed in a line of 120 print positions. The B 5500's line printer character set is listed in the Data Code Table on page 203.141.100.

The B 320 Line Printer is a slower version of the B 321 and is offered at a substantially reduced price; this slower model operates at a peak speed of 475 lines per minute. The B 325 Line Printer increases the printing flexibility by providing 132 print positions. Except for these differences in speed and print-block size, respectively, the B 320 and B 325 Line Printers are functionally identical with the B 321 model. Therefore, in the description that follows, reference is made only to the characteristics and capabilities of the B 321.

Up to two line printers can be connected to a B 5500 system. The B 320 and B 321 can be paired in any system, but the 132-print-position B 325 cannot be used in the same system with either the B 320 or B 321. Since the printing operation is completely buffered, two line printers can operate simultaneously and at their rated speeds. Information is transferred from core storage to the B 321 Printer through an I/O Channel in the form of fifteen 48-bit (8-character) words per line. The printer stores this information consecutively in its 120-character buffer. As soon as the buffer is full, the I/O channel is released and the printing cycle begins. Printing, spacing, and skipping operations proceed independently of the I/O Channel once the buffer is full and the paper motion signals are received.

The B 321's total print cycle time is 85.7 milliseconds. Of this time, only 3 milliseconds is consumed in loading the buffer by the I/O Channel. The B 5500 Memory Module containing the output data is occupied for a total of 60 microseconds, the time required to access 15 consecutive words of data. The Processor is entirely free of the printing operation once it has sent the Line Printer Output Descriptor to the I/O control unit.

Spacing and skipping operations are specified in the Output Descriptor, and can be performed in conjunction with printing or independently. Spacing can be specified as 0, 1, or 2 lines, and skipping can be regulated by a 12-channel punched tape loop. Paper advance can occur at a rate of 25 to 40 inches per second.

Printing is performed on continuous card or paper forms. Forms width can extend from 5 to 20 inches; the maximum length is 22 inches per form. Output format spacing is 10 characters per inch horizontally and 6 or 8 lines per inch vertically.

As many as five carbons plus the original form will function properly in the printers. The forms are loaded in the cabinet beneath the printing mechanism and are transported through the unit by means of pin-fed tractors to the self-maintaining stacker. A Paper-Exhausted indicator/switch and several broken-paper detectors interlock the printer when required in order to provent runaway printing without forms.

The format of the printed line is under control of the problem program or the Master Control Program's Output Writer. The code translation from Burroughs Common Language (BCL) internal code to the 64-character print set is performed automatically. The actual printing is accomplished by hammer strokes against a continuously-rotating engraved drum. Once the drum has made a complete revolution, every character will have been printed, and the paper motion can begin. Each line spaced after printing consumes 5.95 milliseconds. The graph on the next page illustrates the maximum printing speeds of the B 320, B 321, and B 325 Line Printers at varying line spacings.

A number of functional controls are provided to enable the operator to adjust for variances in the size of the forms and the number of interleaved carbons. The operator can also adjust the horizontal and vertical alignment of the forms and the print quality of individual print positions.

Error checks are made for proper character parity in the buffer, for drum rotation synchronization, and for the presence of paper. Errors are signalled by a control-panel indicator and result in a halt of the printer. Error conditions set individual bits in the printer's Result Descriptor, which is returned to core storage at the conclusion of the printing operation.

As soon as the printer's buffer has been loaded, an interrupt bit is set to inform the Master Control Program that the I/O Channel is free. Another interrupt bit is set when the actual printing and spacing operation is complete. At that time, the MCP tests the Result Descriptor to determine such conditions as end-of-paper, parity errors in data transfer, unit non-readiness, busy status, and improper drum synchronization. The MCP then initiates whatever corrective action might be necessary.

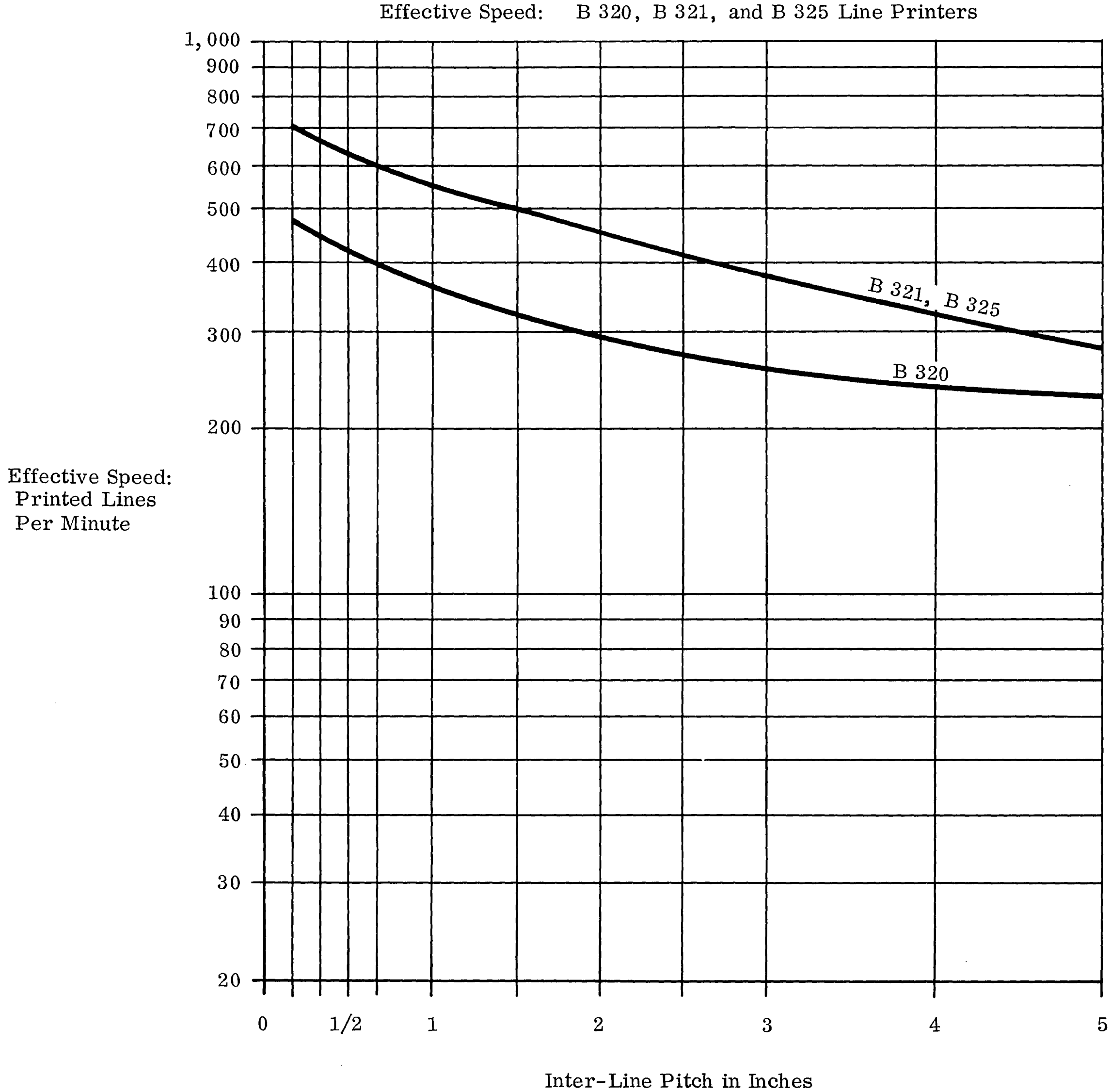
The chart and graph on the next page show comparative performance figures for the B 320, B 321, and B 325 Line Printers.

(Contd.)

TABLE I: LINE PRINTER CHARACTERISTICS

Line Printer Model	B 320	B 321	B 325
Maximum speed (lines per minute)	475	700	700
Number of print positions	120	120	132

Effective Speed: B 320, B 321, and B 325 Line Printers



INPUT-OUTPUT: B 328/329 LINE PRINTERS

.1 GENERAL

.11 Identity: . . . . B 328 Line Printer.
B 329 Line Printer.

.12 Description

The B 328 and B 329 Line Printers operate at a maximum rate of 1,040 lines per minute at single spacing when the characters to be printed are limited to those in a continuous 37-character segment of the print drum. The peak rate can also be maintained while printing and triple-spacing if a 16-character "numeric and edit" set is used. As larger character sets are used, the operational speeds are reduced, as shown in Table I below. When the entire 64-character set is utilized, the single-spaced speed will not fall below 734 lines per minute.

The only difference between the B 328 and B 329 Line Printers is the number of print positions available for each line. The B 328 provides 120 print positions, and the B 329 provides 132 print positions. Up to two line printers can be connected to a B 5500 system, but the B 328 and B 329 cannot be paired in the same system. The B 320 and B 321 Printers (described in the previous report section) can be intermixed with the B 328, and the B 325 Printer (also described in the previous section) can be paired with the B 329.

Burroughs' standard 64-character drum printer set has been statistically analyzed and regrouped on the drum according to frequency of use. The 37 most frequently-used characters (10 numeric, 26 alphabetic, and the period) are arranged in consecutive locations around the drum. The revised drum arrangement and a "quick cancel" memory result in the improved performance of the B 328 Line Printer over the 700-line-per-minute B 321 model.

The printing process is initiated when the Processor sends a Line Printer Output Descriptor to the I/O control unit. The Processor is then completely free for further processing. A free I/O Channel is selected by the I/O control unit and 15 consecutive words of output data are transferred from a designated Memory Module to a 120-character buffer (132 characters in the B 329) within the printer itself. The Memory Module is occupied for a total of 60 microseconds in accessing the data. As soon as the buffer has been filled (a process that consumes about three milliseconds), printing begins and the I/O channel is released.

As each character in the buffer is printed, its buffer position is set to a blank. Immediately upon detection of a completely blank buffer, paper motion begins. (A minimum of 16 characters on the drum must pass the printing mechanism before paper advancing can begin.) The start of paper motion is therefore not contingent on the completion of a full drum revolution.

The operational speeds of the printers are governed by the rotational speed of the print drum and the paper advance speeds. The rotational speed is 1,040 rpm, or one revolution every 57.7 milliseconds. The printing or bypassing of each character on the drum requires 0.9 millisecond. To advance the form a single space requires 24 milliseconds for the first space and 7 milliseconds for each additional space. Therefore, to maintain printing speeds of 1,040 lines per minute, the total printing and spacing time must not exceed 57.7 milliseconds. On this basis, up to 37 consecutive alphameric characters can be printed and single spacing can occur during a single drum revolution. Table I indicates effective speeds as character sets and spacing demands are varied.

Spacing and skipping operations are specified in the Output Descriptor, and can be performed in conjunction with printing or independently. Spacing can be specified as 0, 1, or 2 lines, and skipping can be regulated by a 12-channel punched tape loop. Each line spaced after printing requires 7 milliseconds. Paper advance can occur at a rate of 24 inches per second.

Standard features of the B 328 and B 329 Line Printers include a ribbon-tracking device to sense and control ribbon mistracking, and duplicate controls and indicators on the rear of the cabinets to assist the operator. Except for these added features, the B 328 and B 329 Line Printers have the same physical characteristics, program requirements, forms controls, and error-checking devices as the B 320, B 321, and B 325 printers described in the previous report section, page 203:081.100.

The first deliveries of the B 328 and B 329 1,040-line-per-minute printers were made in June, 1965. Availability is eight months.

TABLE I: EFFECTIVE SPEEDS OF B 328 and B 329 LINE PRINTERS

Lines Advanced per Line Printed	Printed Lines per Minute Using Various Consecutive Character Sets		
	10 Characters	37 Characters	64 Characters
1	1040	1040	734
2	1040	780	680
3	1040	715	625
4	1040	660	584
5	700	610	546
6	648	572	510
12	446	409	380
18	340	318	300
30	230	220	211

INPUT-OUTPUT: MAGNETIC TAPE UNITS

.1 GENERAL

.11 Identity: . . . . B 422 Magnetic Tape Unit.
B 423 Magnetic Tape Unit.
B 424 Magnetic Tape Unit.
B 425 Magnetic Tape Unit.

.12 Description

The magnetic tape units available for use with the B 5500 provide data transfer rates ranging from 18,000 to 72,000 characters per second and packing densities of 200, 556, or 800 rows per inch. Each row can consist of one 6-bit character or two octal digits, depending upon whether the recording was performed in alphameric or binary mode. In addition to the six data bits per row, a seventh channel is provided for a parity bit. Data is recorded on 0.5-inch Mylar-based tape on reels 10.5 inches in diameter. The reel capacity is 2,400 feet, allowing a maximum of 22.1 million alphameric characters per reel when recording at the 800 characters-per-inch density.

Tape reading can be performed in either a forward or backward direction, and all tape operations, including read, write, forward and backward space, erase, and rewind, are carried out independently of the B 5500 Processor. Up to four magnetic tape operations can be performed simultaneously, since each operation is controlled by an independently functioning, "floating" I/O Channel, four of which can be used in a B 5500 system. A maximum of 16 magnetic tape units can be connected to a B 5500.

The B 422, B 423, and B 424 Magnetic Tape Units are functionally identical, but they differ among themselves in several performance categories. The B 425 Magnetic Tape Unit, also similar to the other models, features "drive holdover," which improves its performance by preventing tape movement from stopping when a read or write command is initiated within 2 to 3 milliseconds after completion of the prior tape command. Table I illustrates the differentiating characteristics between the four tape unit models, and the associated graph demonstrates the resulting variances in performance. Only the B 422 and B 424 Magnetic Tape Units can be intermixed on the same B 5500 system.

Tape operations are initiated when the Processor sends a Magnetic Tape I/O Descriptor to the I/O control unit. At that point the Processor is free to continue with its processing task. The I/O control unit then selects a free I/O Channel and begins the transfer of data between a tape unit and a B 5500 Memory Module. The selected I/O Channel remains fully occupied for the duration of the tape operation.

The I/O Descriptor specifies the tape operation to be performed and all other necessary parameters such as unit designation, input or output Memory Module address, alphameric or binary reading or recording mode, direction of read, and data word count when required. When recording in the alphameric mode, BCL-coded 6-bit characters are written from core storage until a special group-mark character is encountered. Thus, the size of core storage is the only limiting factor on the tape record length when recording in the alphameric mode. Binary recording is terminated when a specified number of 48-bit words (eight tape rows per word) have been written. The maximum number of binary words that can be written in or read from each block is 1,023. Binary tape reading is also terminated by satisfying the word count. Alphameric reading is terminated either by satisfying the word count or by sensing the 0.75-inch interblock gap on tape, whichever is encountered first.

After the tape operation has been completed, a special I/O-complete bit is set in the External Interrupt Register, and an I/O Result Descriptor is constructed and sent to core storage. The Result Descriptor indicates if the assigned tape

TABLE I: CHARACTERISTICS OF BURROUGHS MAGNETIC TAPE UNITS

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, char per sec	Interblock Gap Lengths			Efficiency, % (3)		Demand on Core Storage, %	Rewind Speed, inches per sec
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks		
B 422	120	200 556	24,000 66,000	0.75	8.7	209 574	32.3 14.8	63.5 64.4	1.2 3.3	320
B 423	120	200	24,000	0.75	8.7	209	32.3	63.5	1.2	320
B 424	83	800	66,000	0.75	8.7	574	14.8	64.4	3.3	320
B 425	90	200 556 800	18,000 50,000 72,000	0.75	6.25	113 313 450	46.9 24.2 18.0	89.8 76.1 68.9	0.9 2.5 3.6	320

(1) Published time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks; the interblock gap time for the B 425 assumes the use of the "drive holdover" feature.
(2) Effective number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.

.12 Description (Contd.)

unit was not ready or busy, if an end-of-file or physical end-of-tape marker was sensed, or if data transfer parity errors occurred. The Master Control Program tests the bit settings of the Result Descriptor and initiates any corrective action that may be required.

When reading or recording, tape is pulled from a vacuum-column buffer by a moving capstan and pinch-roller assembly, and passed under a dual-gap read/write head. Tape speed past the head is 120 inches per second in the B 422 and B 423, 83 inches per second in the B 424, and 90 inches per second in the B 425. The read section of the head follows the write section by 0.15 inches to allow for immediate read-after-write checking. Tape is then drawn into another vacuum column preceding the take-up reel to guard against tape damage and breakage.

According to published specifications, the transport mechanism provides tape start times of 4.5 milliseconds and stop times of 4.2 milliseconds, although there are indications that these published times are somewhat faster than the times actually achieved in installed transports. By means of its "drive holdover" Feature, Burroughs states that the B 425 is capable of writing consecutive records with a total interblock overhead time of 6.25 milliseconds.

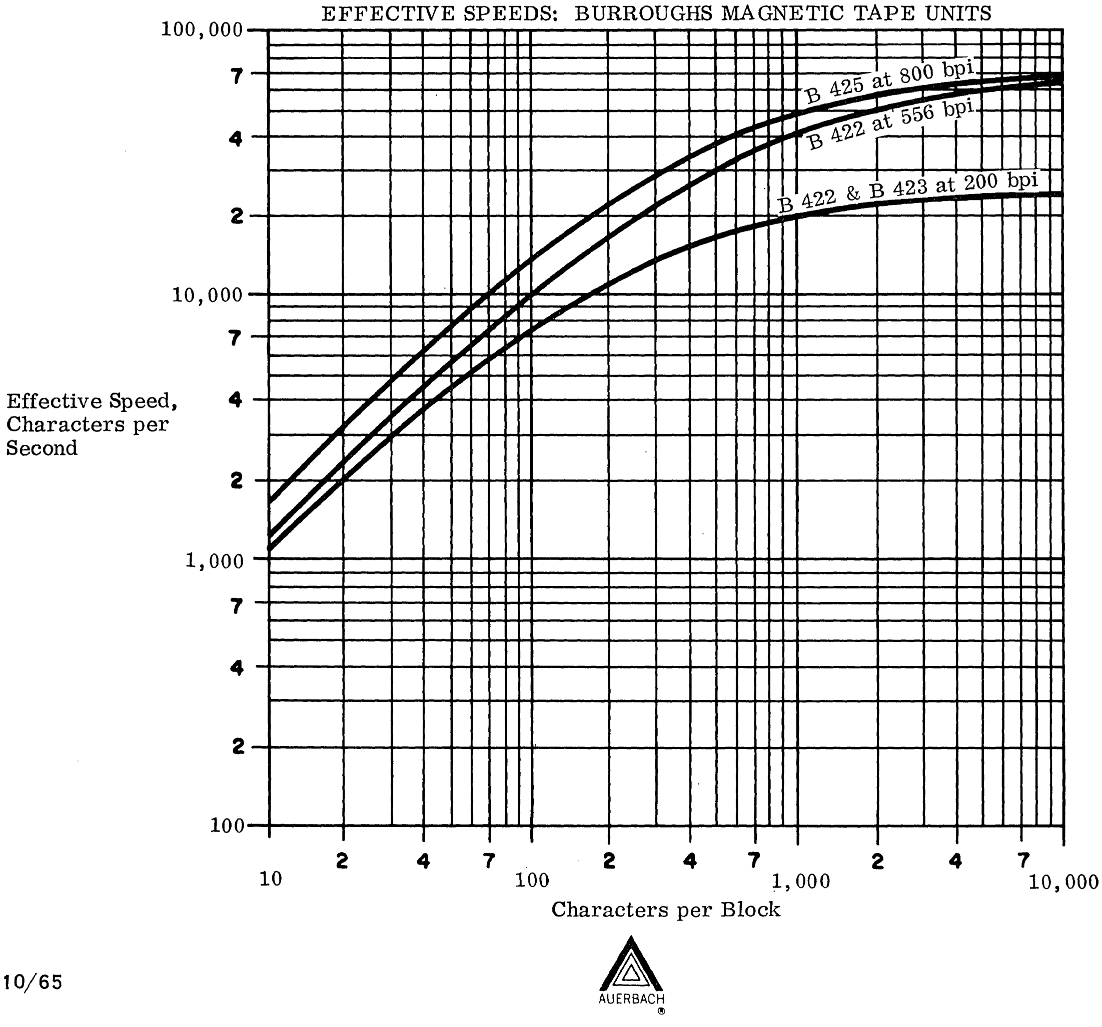
In addition to the data-transfer validation provided by the read-after-write check, several other checks are provided. Row parity is checked during both reading and recording. A longitudinal check character for each block is developed during recording and checked during subsequent readings. Data transfer errors of any kind cause specific bits to be set in the I/O result descriptor.

The B 422, B 423, B 424, and B 425 Magnetic Tape Units are fully compatible with the tape units used with the Burroughs B 100/200/300 Series. Computer systems of this smaller Burroughs series can thus be readily used as satellites to the larger B 5500 systems. Compatibility is also achieved with the IBM 729 and 7330 tape units, and with the newer IBM 2400 Series tape units equipped with the 7-Track Compatibility feature.

Reel loading is facilitated by a latch-leader device affixed to every reel. The leader is latched to a section of tape that is permanently attached to the take-up transport, and a Load button is pushed. Tape positioning for proper operation is then performed automatically. Density-switching and high-speed rewinding (320 inches per second) can also be controlled at the tape unit's control panel.

.14 First Delivery: . . . . . January 1964 for B 422.
February 1964 for B 423.
May 1965 for B 424.
Unspecified for B 425.

EFFECTIVE SPEEDS: BURROUGHS MAGNETIC TAPE UNITS



INPUT-OUTPUT: DATA COMMUNICATIONS SYSTEM

.1 GENERAL

.11 Identity: . . . .
B 450 Disk File and Data Communication Basic Control.
B 5480 Data Communication Control Unit.
B 481 Teletype Terminal Unit.
B 483 Typewriter Terminal Unit.
B 493 Typewriter Inquiry Station.
B 484 Dial TWX Terminal Unit.
B 487 Data Transmission Terminal Unit.

.12 Description

The Burroughs B 450 Disk File and Data Communication Basic Control Unit consists of a standard B 5500 cabinet module housing the power supply and circuitry to control up to two B 5480 Data Communication Control Units. Each B 5480 Control Unit provides the interface between a B 5500 I/O Channel and up to 15 data communications terminals of several varieties. The B 5480 can be located up to 50 feet from the I/O control unit; it operates independently of the I/O control unit except when loading or unloading the buffers of its associated terminal units to or from the I/O Channel.

The principal function of the B 5480 Data Communication Control Unit (DCCU) is to scan its terminal units to determine their input and output readiness, and to alert the processor of these conditions by sending interrupt signals to the I/O control unit. The B 5480 DCCU also provides automatic code translation facilities between Burroughs Common Language (BCL) and Baudot codes.

The B 5480 DCCU's scanner can recognize that any terminal unit is in one of four possible states: busy, input-ready, output-ready, or not-ready. The B 5480 cannot communicate with a "busy" terminal; instead it sets a "terminal busy" interrupt bit in an I/O Result Descriptor that is sent to core storage. The Master Control Program tests all Result Descriptors and initiates whatever action is appropriate. When a terminal unit has received a complete message from an inquiry station, the B 5480 recognizes the terminal as input-ready and selects a free I/O Channel for transfer of the inquiry to core storage. The terminal unit is in the output-ready state when it has emptied the contents of its buffer to an inquiry station and still has not detected an end-of-reply (group mark) character. In this case the B 5480 latches its scanner to the output-ready terminal until the full response is transmitted. If the I/O control unit attempts to send a response to a terminal unit that is in the not-ready state, the B 5480 notes the condition and sets an indicator bit in the I/O Result Descriptor. The maximum time required for the B 5480's scanner to examine the status of all its terminal units is 220 microseconds.

The nominal data transfer rate through the B 5480 DCCU is 30,000 six-bit characters per second. Transfers are serial by character and parallel by bit.

The paragraphs that follow describe the several types of terminal units and inquiry stations that can be connected to a single B 5480 Data Communication Control Unit. Up to 15 of these terminal units, in any combination, can operate under control of each B 5480, and two B 5480's can be connected to a B 5500 system.

.121 B 481 Teletype Terminal Unit

The B 481 Teletype Terminal Unit is a Teletype Model 28 Sequential Selector with selective calling features, which provides the interface between the B 5480 DCCU and a network of Teletype stations. A maximum cable length of 50 feet is permitted between the B 481 Teletype Terminal Units and the B 5480 DCCU. The B 481 provides buffer storage and performs serial-to-parallel (input) and parallel-to-serial (output) conversions of the Teletype character codes. From 1 to 400 Teletype stations can be serviced by a single terminal unit, allowing a total of 6,000 Teletype stations in the network if only Teletype Terminals are used. Each B 481 can service only one Teletype station at a time. The B 481 has a buffer storage capacity of either 120 or 240 6-bit characters; buffer access time is 20 microseconds. A character control device provides for the insertion and deletion of special Teletype control characters and station disconnect signals. An optional Teletype Page Printer can be included as part of the B 481 Terminal Unit and used to monitor all messages on the network.

.122 B 483 Typewriter Terminal Unit

The B 483 Typewriter Terminal Unit provides facilities for connecting from 1 to 8 Typewriter Inquiry Stations to the communications system. The unit contains an input buffer which is capable of storing simultaneous inputs of 30 characters from each of 8 typewriter inquiry stations. An input scanning device accepts data as it becomes available (a character at a time) from any of the 8 stations, and directs it to the proper portion of the buffer. When an end-of-input character is recognized, an interrupt and latch facility holds the input buffer to the station while data is transferred through the B 5480 Data Communication Control Unit to the I/O Channel and to core storage.

A 240-character output buffer is also provided in the B 483 Typewriter Terminal Unit. This buffer

.122 B 483 Typewriter Terminal Unit (Contd.)

is used to store reply messages from the I/O control unit while the terminal is latched to a Typewriter Inquiry Station. The terminal unit remains latched to its receiving station until the end-of-reply character from core storage is recognized. Output buffer read-out to the Typewriter Inquiry Station is under the independent control of the B 483 Typewriter Terminal Unit.

.123 B 493 Typewriter Inquiry Station

The B 493 Typewriter Inquiry Station utilizes a Teletype Send-Receive Page Printer set. It communicates with the B 483 Terminal Unit via a multiple-conductor cable which can be up to 1 mile long, and it can be used for input and output of alphameric data at up to 10 six-bit characters per second. Up to 8 Typewriter Inquiry Stations can be connected to each B 483 Terminal Unit.

.124 B 484 Dial TWX Terminal Unit

The B 484 Dial TWX Terminal Unit provides the facilities required to use stations of the Dial TWX network as inquiry and transmission devices. The B 484 unit contains 480 character positions of input-output buffering that can accept messages from up to eight stations of the Dial TWX network simultaneously. The buffer size can be segmented into groups of 60, 120, 240, or 480 positions, depending on the number of channels to be utilized — 8, 4, 2, or 1. A Bell System Model 103A Data-Phone subset must be used as an interface between each channel and the TWX network. Normal telephone dialing procedures are followed in establishing contact between one of the eight channels and each Terminal Unit.

After a connection between a TWX station and the B 484 Terminal Unit has been established, the operator types an input message on the Dial TWX station keyboard, using a Model 33 or 35 Teletypewriter unit. The message is transmitted and loaded into the Terminal Unit's buffer as it is keyed in. The message is then sent to the B 5480 Data Communication Control Unit, and from there to the I/O control unit at the rate of 30,000 six-bit characters per second. After the message has been processed, the Terminal Unit sends the processor's response to the awaiting channel. Until the station has received the "disconnect code," it can continue to communicate with the processing center. The B 484 Terminal Unit can accept messages larger than the buffer size established for each channel, but only one such message can be accepted at any one time. All input-output messages controlled by the Dial TWX Terminal Unit can be monitored by connecting a B 493 Typewriter Inquiry Station to the Terminal Unit. When the monitor station is disconnected, the typewriter can be used in its normal manner.

.125 B 487 Data Transmission Terminal Unit

The B 487 Data Transmission Terminal Unit (DTTU) was announced by Burroughs in August, 1965. The B 487, unlike the previously-available Burroughs terminal units, is general in purpose. Various remote input-output devices can be interfaced to it by means of up to 16 line (or channel) adapters. Therefore, a single B 487 DTTU can provide a B 5500 system with a mix of data transmission services without the use of additional terminal units.

Most remote devices that can use the low-speed and voice-grade lines of the telephone companies (with data transmission speeds up to 2,400 bits per second) can be connected to the B 487, and ultimately to the B 5500, via Burroughs' line adapters.

The B 487 DTTU contains buffer units to control the flow of data between the remote devices and the B 5500 I/O control unit. The total capacity of the B 487's buffer is 448 characters, providing a minimum (and basic) buffer size of 28 characters for each of the 16 possible transmission channels. The 448-character buffer can be divided into from 1 to 16 smaller-sized buffers in increments of 28 characters. Since each of the 16 possible buffers is individually addressable by means of the B 5500's I/O and Result Descriptors, up to 16 messages can be stored or transmitted simultaneously by each B 487. A maximum of 15 B 487 terminal units can be connected to a B 5500 system.

Automatic code translation can be provided for the B 487 DTTU by using the B 249 Data Transmission Control Unit in place of the B 5480 DCCU. The B 249 includes the facilities to translate into Burroughs' 6-bit BCL internal code input data in 5-level Baudot, 6-level ASCII, or 8-level ASCII codes. Similar code translations on output data can also be performed automatically.

The B 249 Data Transmission Control Unit is required, in place of the B 5480 DCCU, when automatic code translation is desired, when multiple B 487 DTTU's are connected to one B 5500 system, and/or when any of the previously-described Burroughs terminal units are intermixed with a B 487 in the same B 5500 system. However, the B 249 can provide individual buffer addressability only for the B 487 DTTU. The B 249 Control Unit provides the interfacing to accommodate up to 15 B 487 Data Transmission Terminal Units, or any combination of B 487's and the other Burroughs terminal units (described above) to a maximum of 15.

The B 452 Disk File/Data Transmission Terminal Unit must be used in conjunction with the B 487; each B 452 supplies the power and cabinet space for up to two B 487 DTTU's.

With the addition of the B 487 Data Transmission Terminal Unit to its line of data communications equipment, Burroughs now offers B 5500 users the equipment needed to operate the computer system from a remote site, to perform message switching, to perform medium-speed batch data transmission, to compile programs from a remote location, and to service simple inquiries.

First delivery of Burroughs' data communications equipment for the B 5500 occurred in November, 1964.

SIMULTANEOUS OPERATIONS

The Burroughs B 5500 Information Processing system can concurrently execute:

- One or two machine instructions (one per Processor); and
- Up to four input-output operations, one for each available B 5283 I/O Channel.

Because each of the core storage Memory Modules has its own independent addressing and read/write circuitry, simultaneous memory accesses are possible. The maximum number of truly simultaneous accesses to core memory in a fully-expanded B 5500 system is six: one access by each of the two Processors and one access by each of the four I/O Channels. Six interleaved (not simultaneous) accesses to the same Memory Module are also permitted, although no more than two of these accesses can result from magnetic tape operations.

The B 5500 Processor initiates all peripheral input-output operations by sending a 48-bit I/O Descriptor to the I/O control unit. Normally the Processor is then free to perform its operations, unaffecting and unaffected by the concurrent peripheral operations. The Processor's performance is delayed only when it accesses a Memory Module that is already being simultaneously accessed by another Processor or I/O Channel. Since data is transferred to and from the Memory Modules one word at a time, and since the memory cycle time per word is either four or six microseconds (for the B 461 and B 460 Modules, respectively), the Processor will normally be delayed only a minimal amount of time while awaiting access to a "busy" Memory Module.

Each I/O Channel is totally dedicated to its assigned input-output task once it has been selected by the I/O control unit. The line printers and data communications terminals have their own internal buffers, and therefore the I/O Channels are released immediately after loading or emptying these buffers. Up to four input-output operations can be performed simultaneously, one per installed I/O Channel, since each I/O Channel functions independently of the others.

Input-output data transfers utilize the accessed Memory Module only during each 48-bit, single-word transfer; the memory access time per word is either four or six microseconds, depending on whether the B 461 or B 460 Memory Modules are used. The number of memory accesses required for each input-output operation, or, alternatively, the time required for memory accesses as a percentage of the total time for the I/O operation, is specified in the report sections describing the individual B 5500 peripheral units.

INSTRUCTION LIST

.1 WORD MODE

Each Word Mode syllable is 12 bits long and may be one of the following four types, as designated by the two low-order bits.

.11 Literal (bit code 00)

The ten high-order bits are placed in A as a positive integer.

.12 Operand Call (bit code 10)

The ten high order-bits are added to (R); the word at this address is brought to A. Then:

- If (A) is an operand, no further action occurs.
- If (A) is a Data Descriptor whose size field is zero, bring the word at the descriptor address to A.
- If (A) is a Data Descriptor whose size field is non-zero, add the ten low-order bits of (B) to the descriptor address, and bring the word at this address to A.
- If (A) is a Program Descriptor, enter the addressed subroutine.

.13 Descriptor Call (bit code 11)

The ten high-order bits are added to (R); the word at this address is brought to A. Then:

- If (A) is an operand, construct a descriptor of that operand and place it in A.
- If (A) is a Data Descriptor whose size field is zero, no further action occurs.
- If (A) is a Data Descriptor whose size field is non-zero, add the ten low-order bits of (B) to the descriptor address.
- If (A) is a Program Descriptor, enter the addressed subroutine.

.14 Operators (bit code 01)

OPERATOR	OPERATION
	Arithmetic
ADD	(B) + (A) ⟶ B
SUB	(B) - (A) ⟶ B
MUL	(B) x (A) ⟶ B
DIV	(B) ÷ (A) ⟶ B; quotient is normalized and rounded.
IDV	Normalize (A) and (B); then (B) ÷ (A) ⟶ B
RDV	Normalize (A) and (B); divide (B) by (A); store remainder in B.
DLA	(S3 & S4) + (A & B) ⟶ A & B; i.e., double length add.
DLS	(S3 & S4) - (A & B) ⟶ A & B
DLM	(S3 & S4) x (A & B) ⟶ A & B
DLD	(S3 & S4) ÷ (A & B) ⟶ A & B
	Logic
LND	AND: If 1 appears in corresponding bit position of both A and B, retain the 1 in B; otherwise place a 0 in B. Mark A empty.
LOR	OR: If 1 appears in corresponding bit positions of either A or B, place a 1 in B; otherwise place a 0 in B. Mark A empty.
LQV	EQUIVALENCE: If corresponding bits of A and B are equal, place a 1 in B; otherwise place a 0 in B. Mark A empty.
LNG	NEGATE: Change all zeros to ones and all ones to zeros in Register A, except flag bit is unaltered.
GTR	If (B) > (A), 1 ⟶ B; otherwise 0 ⟶ B.
LSS	If (B) < (A), 1 ⟶ B; otherwise 0 ⟶ B.
LEQ	If (B) ≤ (A), 1 ⟶ B; otherwise 0 ⟶ B.
EQL	If (B) = (A), 1 ⟶ B; otherwise 0 ⟶ B.
NEQ	If (B) ≠ (A), 1 ⟶ B; otherwise 0 ⟶ B.
GEQ	If (B) ≥ (A), 1 ⟶ B; otherwise 0 ⟶ B.

(Contd.)

.14 Word Mode Operators (Contd.)

OPERATOR	OPERATION
	Logic (Contd.)
nnFCE	Compare nn bits of (A) to nn bits of (B); If equal, 1⟶A; otherwise 0⟶A.
nnFCL	Compare nn bits of (A) to nn bits of (B); If (B) < (A), 1⟶A; otherwise 0⟶A.
nnTFB	Copy nn bits from A to B.
nnDIA	nn⟶G & H unless nn = 0.
nnDIB	nn⟶K & V unless nn = 0.
MDS	Set flag bit of (A) to 1, making (A) a descriptor.
MOP	Set flag bit of (A) to 0, making (A) an operand.
TOP	If flag bit of (A) is 0, 1⟶A; otherwise 0⟶A.
SSN	Set sign of (A) to 1.
SSP	Set sign of (A) to 0.
CHS	Change sign of (A).
FBS	Search for word with flag bit on (i.e., descriptor) beginning at address in A. Place in A the address of first descriptor found.
LLL	Compare a field in (A) to a list of words beginning at the address in B, placing each list word in (B) for the test. When (A) is ≤ (B), place the address of the word in B into A.
	Data Transfers
XCH	Exchange (A) and (B).
DUP	Adjust stack until A is empty and B is full; duplicate (B) in A.
DEL	Delete the top word of stack; i.e., (A).
SSF	If two low-order bits of (A) are zeros, store (F) in B; if they are ones, store (B) in S; if only the low-order bit is zero, set subprogram switch and store (B) in F; if only the low-order bit is one, store (S) in B.
	In the following store operators, if A contains a descriptor, (B) is stored in the address it specifies. If A contains an operand, (B) is stored at the address formed by modifying (A) by (R) or (F).
SND	Store (B); mark A empty, but retain (B).
STD	Store (B); mark A and B empty.
ISN	Convert (B) to an integer and store; mark A empty, but retain (B).
ISD	Convert (B) to an integer and store; mark A and B empty.
CND	If low-order bit of (A) is 1, proceed as in ISN, above; otherwise proceed as in SND, above.
CID	If low-order bit of (A) is 1, proceed as in ISD, above; otherwise proceed as in STD, above.
1sISO	Store a G- and H-specified field from (A), with a length of 1s, in the low order bits of A, and set rest of (A) to zero.
CTC	Store the 15 low-order bits of (A) in the 15 low-order bits of (B).
CTF	Store the 15 low-order bits of (A) in bits 16 through 30 of (B).
FTC	Store bits 16 through 30 of (A) in the 15 low-order bits of (B).
FTF	Store bits 16 through 30 of (A) in bits 16 through 30 of (B).

.14 Word Mode Operators (Contd.)

OPERATOR	OPERATION
	Branching
	In all branching operations, if (A) is an operand it specifies number of syllables to be jumped. If (A) is a descriptor, it specifies destination address.
BFW	Branch forward unconditionally.
BBW	Branch backward unconditionally.
BFC	Branch forward unless low-order bit of (B) is 1 (set by compare operations).
BBC	Branch backward unless low-order bit of (B) is 1 (set by compare operations).
CFD	If a G- and H-specified field of (B) is not zero, mark B empty, and proceed as in BFW, above.
CFN	If G- and H-specified field of (B) is not zero, proceed as in BFW, above.
CBD	If a G- and H-specified field of (B) is not zero, mark B empty, and proceed as in BBW, above.
CBN	If a G- and H-specified field of (B) is not zero, proceed as in BBW, above.
	Subroutine Operators
MKS	MARK STACK: Push down (A) and (B) into stack. Construct Mark Stack control word containing (F) and (R), store it in stack, and copy its stack address into F.
XIT	EXIT: (A subroutine return in the Word Mode) Reset contents of C, L, G, H, K, V, R, and F from the Return and Mark Stack control words. Mark A and B empty.
RTN	RETURN: (A subroutine return in the Character Mode) Adjust stack until A is full and B is empty. Reset contents of C, L, G, H, K, V, R, and F from the Return and Mark Stack control words.
BRT	BRANCH RETURN: If presence bit is 1, set S and C from (A); restore R and F from Mark Stack control word; mark A and B empty.
CMN	ENTER CHARACTER MODE IN-LINE: Push (A) and (B) into stack. Construct Return control word containing (C) and (L), store it in stack, and copy its stack address into F. Store the word below the Return control word in S, and set sub-program and Character-Mode switches.
	Miscellaneous Operators
PRL	PROGRAM RELEASE
COC	CONSTRUCT OPERAND CALL
CDC	CONSTRUCT DESCRIPTOR CALL
COM	COMMUNICATION: Store (A) in a specific location and set communication bit in Interrupt register.
LOD	LOAD OPERATOR
INX	INDEX: Add 15 low-order bits of (B) to (A).
TUS	Store in A a peripheral unit's status word, and set a bit indicating each unit's readiness or non-readiness.
TIO	Store in A an integer indicating the lowest-numbered currently-available I/O Channel. Store a zero if all Channels are busy.
	Control State Operators
	Note: The following operators may be used only when the Processor is in the Control State as a result of an interrupt. All the preceding Normal State operators may also be used in the Control State.
HP2	Cause Processor 2 to store its registers in the stack and halt.
IIO	Store (A) in a specific location; send an Initiate I/O signal to Central Control for selection of an I/O Channel.
IP1	Set Processor 1's registers from fixed storage location and exit from Control State.
IP2	Store (A) in a specific location and activate Processor 2.
ITI	Interrogate the Interrupt Register; if any interrupt bit is on, transfer control to the corresponding storage location.
RTR	Timer setting ⟶ A.
IOR	I/O RELEASE: Set presence bit to 1 in location formed by modifying (A) by (R) or (F).

(Contd.)

.2 CHARACTER MODE

Each Character Mode syllable is a 12-bit operator consisting of a 6-bit repeat field and a 6-bit operation code. The following operators are available.

OPERATOR		OPERATION
REPEAT	OP. CODE	
		Arithmetic
		Note: Zone bits are ignored; T/F toggle →1 if field overflow occurs.
nn	FAD	(DC) + (SC)→DC, for nn successive chars.
nn	FSV	(DC) - (SC)→ DC, for nn successive chars.
		Logic
r	TLS	If (SC) < r, T/F toggle→ 1.
r	TEQ	If (SC) = r, T/F toggle →1.
r	TNE	If (SC) ≠ r, T/F toggle →1.
r	TGR	If (SC) > r, T/F toggle →1.
r	TEL	If (SC) ≤ r, T/F toggle →1.
r	TEG	If (SC) ≥ r, T/F toggle →1.
b	BIT	If (SB) = b, T/F toggle →1.
nn	CEQ	If (SC) = (DC), for nn chars, T/F toggle →1.
nn	CNE	If (SC) ≠ (DC), for nn chars, T/F toggle →1.
nn	CGR	If (SC) > (DC), for nn chars, T/F toggle→ 1.
nn	CEL	If (SC) ≤ (DC), for nn chars, T/F toggle →1.
nn	CLS	If (SC) < (DC), for nn chars, T/F toggle →1.
nn	CEG	If (SC) ≥ (DC), for nn chars, T/F toggle →1.
		Data Transfer
nn	TRW	(SW)→ DW, for nn successive words.
nn	TRP	(PC)→ DC, for nn successive characters.
nn	TRS	(SC) →DC, for nn successive characters.
nn	TRN	Same as TRS, but transfer numeric bits only.
nn	TRZ	Same as TRS, but transfer zone bits only.
—	TBN	Replace with blanks all characters in a field specified by S and K that are equal to or less than zeros. Terminate operation when a greater-than-zero character is encountered.
		Skip Operators
nn	SFS	Skip forward over nn source characters.
nn	SRS	Skip backward over nn source characters.
nn	SFD	Skip forward over nn destination characters.
nn	SRD	Skip backward over nn destination characters.
nn	BSS	Skip nn successive source bits.
nn	BSD	Skip nn successive destination bits.
		Address Operators
—	SSA	Set source address: next 3 source chars →M & G; O→H.
—	SDA	Set destination address: next 3 destination chars →S & K; O→V.
—	SES	Set source address from a word in stack.
—	SED	Set destination address from a word in stack.
—	TSA	Store source address in stack.
—	TDA	Store destination address in stack.
—	SCA	Store control address (contents of C & L) in stack.

.2 CHARACTER MODE (Contd.)

OPERATOR		OPERATION
REPEAT	OP. CODE	
		Jump Operators
nn	JFW	Jump forward nn syllables.
nn	JRV	Jump backward nn syllables.
nn	JFC	Jump forward nn syllables unless T/F toggle = 1.
nn	JRC	Jump backward nn syllables unless T/F toggle = 1.
nn	BNS	Execute the following loop nn times.
—	ENS	Identifies end of a program loop.
nn	JNS	Jump forward nn syllables to a syllable following end of loop (ENS), do not count around loop.
nn	JNC	If T/F toggle = 0, proceed as in JNS.
		Conversion Operators
nn	OCV	Convert 1 octal word in source string to nn decimal digits (8 max.) in destination string.
nn	ICV	Convert nn decimal digits (8 max.) in source string to 1-word octal integer in destination string.
		Miscellaneous Operators
nn	SEC	Set R (tally register) to nn.
nn	INC	Increment (R) by nn; ignore overflow.
nn	STC	Store (R) in stack at location (F + nn).
nn	BIS	Set nn successive bits in destination string to 1.
nn	BIR	Set nn successive bits in destination string to zero.
nn	CRF	Use the 6 low-order bits of (F + nn) as repeat field for next syllable.
—	EXC	Exit from Character Mode and re-enter Word Mode, resetting Registers C, L, G, H, K, V, S, F, and R from control words in the stack.
—	CMX	EXIT CHARACTER MODE IN-LINE (same as EXC, above, except that Registers C and L are not set).

.3 INSTRUCTION LIST NOMENCLATURE

A: . . . . A register; top location in stack.
B: . . . . B register; second location in stack.
b: . . . . a bit used as a literal in repeat field of a Character Mode syllable.
C: . . . . C register.
DC: . . . . next character in the destination string.
DW: . . . . next word in the destination string.
F: . . . . F register.
G: . . . . G register.
H: . . . . H register.
K: . . . . K register.
L: . . . . L register.
1: . . . . number of characters (included in operator syllable).
M: . . . . M register.
nn: . . . . a 6-bit literal.
PC: . . . . next character in the program segment.
R: . . . . R register.
r: . . . . a character used as a literal.
S: . . . . S register.
s: . . . . number of bits to shift a result (included in operator syllable).
SC: . . . . next character in the source string.
SW: . . . . next word in the source string.
S3:, S4: . . . . the third and fourth locations in the stack (core storage locations addressed by the S register).
T/F: . . . . True/False toggle.
V: . . . . V register.
( ): . . . . the contents of a register or location.

Note: The functions of all Processor registers are described in Paragraph 203:051.24.

DATA CODE TABLE

The B 5500 Information Processing System can manipulate data internally either in 48-bit binary words or in 6-bit BCD characters. Input-output operations can utilize three basic coding systems: binary, 6-bit Burroughs Common Language, and the standard Hollerith card code. Card readers and punches can accept data in Hollerith or binary code. The magnetic drum storage unit reads and records only in the binary mode. The supervisory printer and line printers accept and print data only in BCL code, but the magnetic tape units and Disk File can utilize binary-coded information as well as BCL. Burroughs Common Language code is also the standard input-output data code for the paper tape devices and data communications equipment, although a paper tape code translator permits use of any 5, 6, 7, or 8-level code in read and punch operations, and the 5-level Baudot code can be used with Teletype terminal units.

The table of data codes below consolidates in one chart the several types of internal and external codes used in the B 5500 system.

Collating Sequence: Low (top of the table) to High (bottom of the table)

CHAR.	INTERNAL CODE			BCL CODE		CARD CODE	
	BA	8421	OCTAL CODE	BA	8421	ZONE	NUM.
Blank	11	0000	60	01	0000	-	-
.	01	1010	32	11	1011	12	8 - 3
[	01	1011	33	11	1100	12	8 - 4
(	01	1101	35	11	1101	12	8 - 5
<	01	1110	36	11	1110	12	8 - 6
←	01	1111	37	11	1111	12	8 - 7
&	01	1100	34	11	0000	12	-
$	10	1010	52	10	1011	11	8 - 3
*	10	1011	53	10	1100	11	8 - 4
)	10	1101	55	10	1101	11	8 - 5
;	10	1110	56	10	1110	11	8 - 6
≤	10	1111	57	10	1111	11	8 - 7
-	10	1100	54	10	0000	11	-
/	11	0001	61	01	0001	0	1
,	11	1010	72	01	1011	0	8 - 3
%	11	1011	73	01	1100	0	8 - 4
=	11	1101	75	01	1101	0	8 - 5
]	11	1110	76	01	1110	0	8 - 6
"	11	1111	77	01	1111	0	8 - 7
#	00	1010	12	00	1011	-	8 - 3
@	00	1011	13	00	1100	-	8 - 4
:	00	1101	15	00	1101	-	8 - 5
>	00	1110	16	00	1110	-	8 - 6
≥	00	1111	17	00	1111	-	8 - 7
+	01	0000	20	11	1010	12	0
A	01	0001	21	11	0001	12	1
B	01	0010	22	11	0010	12	2
C	01	0011	23	11	0011	12	3
D	01	0100	24	11	0100	12	4
E	01	0101	25	11	0101	12	5
F	01	0110	26	11	0110	12	6
G	01	0111	27	11	0111	12	7

CHAR.	INTERNAL CODE			BCL CODE		CARD CODE	
	BA	8421	OCTAL CODE	BA	8421	ZONE	NUM.
H	01	1000	30	11	1000	12	8
I	01	1001	31	11	1001	12	9
×	10	0000	40	10	1010	11	0
J	10	0001	41	10	0001	11	1
K	10	0010	42	10	0010	11	2
L	10	0011	43	10	0011	11	3
M	10	0100	44	10	0100	11	4
N	10	0101	45	10	0101	11	5
O	10	0110	46	10	0110	11	6
P	10	0111	47	10	0111	11	7
Q	10	1000	50	10	1000	11	8
R	10	1001	51	10	1001	11	9
≠	11	1100	74	01	1010	0	8 - 2
S	11	0010	62	01	0010	0	2
T	11	0011	63	01	0011	0	3
U	11	0100	64	01	0100	0	4
V	11	0101	65	01	0101	0	5
W	11	0110	66	01	0110	0	6
X	11	0111	67	01	0111	0	7
Y	11	1000	70	01	1000	0	8
Z	11	1001	71	01	1001	0	9
0	00	0000	00	00	1010	-	0
1	00	0001	01	00	0001	-	1
2	00	0010	02	00	0010	-	2
3	00	0011	03	00	0011	-	3
4	00	0100	04	00	0100	-	4
5	00	0101	05	00	0101	-	5
6	00	0110	06	00	0110	-	6
7	00	0111	07	00	0111	-	7
8	00	1000	10	00	1000	-	8
9	00	1001	11	00	1001	-	9
?	00	1100	14	00	0000	ALL OTHER CARD CODES	

Table reproduced from Burroughs B 5500 Information Processing Systems Reference Manual, Appendix A, p. A-1.

PROBLEM ORIENTED FACILITIES

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . . none.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

B 5500 Tape Sort Generator

Reference:	Sorting on the B 5500 Using COBOL-61 Extended, Burroughs Publication 1021334.
Record size:	from 1 to 512 eight-character words.
Block size:	from 1 to 1,023 words.
Key size:	up to 25 fields within each key, with a maximum of 63 characters per field.
File size:	any number of input reels that can be accommodated before any of the available scratch tapes is filled.
Number of tapes: . .	from 3 to 8.
Date available:	April 1963.

Description:

The B 5500 Tape Sort Generator is an integral part of the COBOL Compiler, described in Report Sections 203:162 (COBOL language) and 203:182 (COBOL translator). The generator is activated by the SORT verb, an elective feature of COBOL-61 Extended. File and record descriptions are entered in the source program's Data Division section, and the maximum amount of core storage to be used for sorting is specified in the Environment Division.

The Tape Sort Generator sorts input records from magnetic tape in ascending or descending sequence according to key information contained in up to 25 fields of each record. Only fixed-length records can be sorted, and the record length must be a multiple of eight characters (one B 5500 word). From three to eight magnetic tapes can be used for intermediate storage during the sorting operation, and the sorted output records are written on magnetic tape. The generator uses a "vector sort" technique during the internal sort or "stringing" phase, and a polyphase Fibonacci merge during the output phase.

A simple sort of all records results when the SORT statement with the USING File Name Option is specified in the Procedures Division. However, the INPUT PROCEDURE and OUTPUT PROCEDURE can be utilized to enable the programmer to manipulate the records both before and after the actual sorting operation. The RELEASE verb can be used within the INPUT PROCEDURE to specify only selected records to be sorted. Each SORT statement is self-initializing and can therefore be re-executed as desired. In addition, any number of SORT statements can be used within a single COBOL program.

An example of the speed of the Tape Sort Generator is offered by Burroughs. A sort of 50,000 100-character records, blocked at 10 records per block and using a 10-character sort key, will take 12 minutes and 50 seconds on a single-processor B 5500 that has two I/O Channels, 32K words of core storage, and six available 66KC magnetic tape units.

B 5500 Disk Sort Generator

Reference:	preliminary information.
Record size:	from 1 to 1,023 eight-character words.
Block size:	from 1 to 1,023 eight-character words.
Key size:	up to 25 fields within each key, with a maximum of 63 characters per field.
File size:	limited only by the amount of available intermediate storage (disc and tape).
Number of discs: . .	any number that can contain between 1.1 and 2.2 times the amount of data in the input file.
Number of tapes: . . .	two.
Date available:	November, 1965.

Description:

B 5500 users with available Disk File storage can utilize the more recent Disk Sort Generator. The Disk Sort is also an integral part of the B 5500's COBOL compiler, and is activated by the SORT verb in the same manner as the Tape Sort Generator.

Functionally, the Disk Sort program attempts to make exclusive use of Disk File storage. However, if the amount of available disc storage is exhausted before the sort or "stringing" phase is complete, the Disk Sort program will use magnetic tapes as overflow storage units. All the strings are then merged, and the sorted output file is written on any available output device. In order to ensure that the Sort program will function in a disc-only mode, disc storage must be made available in an amount at least 2.2 times the size of the input file. The Disk Sort program will function with any B 5500 system capable of performing COBOL compilations.

Sort times for the B 5500 Disk Sort program have not been made available to date.

.14 Report Writing: . . . . none.

.15 Data Transcription

The only transcription routines announced to date are integral parts of the Master Control Program. The card-to-tape routine can be used to keep the card reader(s) operating at maximum speed by transcribing input data from cards to magnetic tape, and then reading it from the tape when the program is ready to utilize the data. If the operator indicates that no tape unit is available for the transcription, data is transcribed instead from cards to the Storage Drum or Disk File.

The tape-to-printer routine is used when the number of simultaneously-running programs requiring printer output exceeds the number of Line Printers in the system. Data to be printed is written on magnetic tape. A job number identifies each file, so the output from several programs can be written on the same tape reel. When a printer becomes available, the Master Control Program transcribes the accumulated output data from tape to printer.

Data transcriptions can also be performed off-line on the I/O-compatible Burroughs B 100/200/300 computer systems.

.16 File Maintenance: . . none.

.17 Others . . . .

Scientific Library Procedures

Reference: . . . . "Partial List of Scientific Library Procedures for the Burroughs B 5500."
Date available: . . . . immediate.
Description:

The document referenced above lists 99 mathematical and scientific routines that will be provided for the B 5500 by the manufacturer. These routines range in scope from "Tangent" to "Non-linear Multiple Regression." The major categories, and the number of routines falling into each, are as follows:

Trigonometric functions:	7.
Hyperbolic functions:	3.
Exponential and logarithmic functions:	4.
Root functions: . . .	3.
Polynomials, differential equations, and special functions: .	37.
Integration:	8.
Interpolation and approximation: . .	6.
Matrix algebra and determinants: . . .	6.
Linear programming:	3.
Statistics:	7.
Data correlation: . .	4.

Execution times and storage requirements for some of the standard functions and matrix algebra routines are listed below.

Single-Precision Functions	Time, msec	Size, words
Square root:	0.96	28
Exponential:	0.96 to 1.13	32
Logarithm:	0.66 to 1.19	29
Size:	0.83 to 1.28	38
Cosine:	0.88 to 1.33	40
Arcsine:	2.44 to 2.58	64
Tangent:	1.33 to 1.70	52
Arctangent:	1.20 to 1.71	59

Double-Precision Functions	Time, msec
Square root:	1.55
Exponential:	10.50 to 12.47
Logarithm:	6.22 to 13.06
Sine:	9.15 to 14.12
Cosine:	9.62 to 14.59
Arcsine:	26.84 to 28.37
Tangent:	14.64 to 18.66
Arctangent:	13.16 to 18.75

Matrix Algebra	Time, msec
Addition or subtraction of M x N matrices:	0.180NM + 0.070N + 0.082
Multiplication of 50 x 50 matrices:	33,440.
Inversion —	
For symmetric matrices:	$4N^3/22$
For non-symmetric matrices:	$(N + 1)^3$ x 0.181.
Transposition:	0.163NM + 0.080N + 0.093.

Note: Accuracy is at least 11 significant decimal digits for single-precision functions and 23 for double-precision functions.

PROCESS ORIENTED LANGUAGE: ALGOL

.1 GENERAL

.11 Identity: . . . . Extended ALGOL.

.12 Origin: . . . . Burroughs Corporation.

.13 References: . . . . Burroughs B 5500 Extended ALGOL Reference Manual.
Burroughs B 5500 Stream Procedure Reference Manual.
Burroughs B 5500 Extended ALGOL Input-Output Reference Manual.

.14 Description

ALGOL is a computation-oriented programming language designed primarily for scientific and engineering applications. Extended ALGOL for the B 5500 includes virtually all of the facilities of ALGOL 60 and a number of machine-dependent extensions to take advantage of the capabilities of the B 5500. Among the extensions to ALGOL 60 are:

- Input-output constructs to permit effective utilization of all peripheral devices, including the Disk File.
- Standard file label-checking facilities.
- Input-output buffer control.
- Data formatting and editing facilities.
- B 5500 Character Mode operations.
- Partial-word and double-precision arithmetic operations.
- Ability to insert specialized corrective routines for arithmetic error-condition interrupts.
- Source language debugging facilities.
- Constructs to assist in multisequencing control.
- Data communications inquiry statements.

The input-output facilities are patterned after those of FORTRAN, in that the standard forms of the READ and WRITE statements control the input or output of one logical record. Special forms of these verbs, however, can be used to control multiple data records. The READ and WRITE statements normally must reference a FILE declaration, a FORMAT declaration, and a LIST declaration. The FILE declaration specifies the name of the file, the size and number of buffer areas to be allocated, the class of output medium desired, and magnetic tape label and blocking information. The FORMAT declaration concisely describes the editing and conversions to be performed upon each item of input or output data. The LIST declaration specifies the list of variables whose values comprise the input or output record; alternatively, the list can be included in the READ or WRITE statement itself.

When a READ statement is encountered at execution time, the contents of one input buffer are selected according to the specified FILE declaration, edited according to the FORMAT declaration, and stored according to the LIST. Then the Processor is freed to execute succeeding program statements while the buffer area is refilled from the appropriate input device. When more than one buffer area is declared for a file, they are sequenced on a first-in first-out basis. The RELEASE statement fills an input buffer or empties an output buffer with no editing or internal transfers; it is used mainly in conjunction with user-coded editing operations in the Character Mode.

Two additional READ and WRITE constructs have recently been added to Extended ALGOL: an Edit and Move READ and an Edit and Move WRITE. When these versions of READ and WRITE are used, I/O files and buffer areas do not need to be explicitly designated. With the Edit and Move options, data is edited according to format information within the READ/WRITE statement and is assigned to program variables designated in a supplied list.

Extended ALGOL permits utilization of the B 5500's Character Mode operations through implementation of STREAM PROCEDURE declarations. This facility is described in detail in Paragraph .43 of this report section.

Extended ALGOL for the B 5500 also provides language facilities to read and write data records on Burroughs Disk Files. In the Disk File declaration statement, many parameters can be entered to furnish the ALGOL Compiler with detailed information concerning the manner in which the input-output file shall be controlled. The file can be reserved for exclusive use by the current program. The file can also be designated as a temporary or permanent member of the system. The record access technique can be specified as SERIAL, RANDOM, or UPDATE, and the number and size of input-output buffers can be designated. The data record specifications include the blocking considerations and the record size.

The SERIAL access technique is specified when records are to be read or written in a sequential order. The RANDOM technique is used when the primary objective is either to read and write records in random order, or to update records in a random order. The UPDATE technique is used only when the primary programming goal is to update records in a sequential manner.

.14 Description (Contd.)

Disk File I/O statements include specialized versions of READ and WRITE that require specification of the relative address of the file's record that is to be read or written. The FORMAT and LIST declarations are used exactly as in other input-output operations — to edit and store the record after input or just prior to output. The READ SEEK statement can be used with RANDOM files to find a relatively-addressed record and to store it in a buffer area in anticipation of a subsequent READ or WRITE statement. The relative address of the current record within the file (i.e., the "record pointer") is adjusted a specified number of times by the SPACE statement. The REWIND statement causes the record pointer to be reset to the address of the first record in the file. After a temporary file has served its purpose in the program, it will be automatically deleted from the system unless the LOCK statement is issued to change the file's status to permanent.

An example of a brief Extended ALGOL source program and its generated object code is presented in Table I.

The restrictions and extensions of B 5500 Extended ALGOL relative to the ALGOL 60 Reference Language are summarized below. The language specifications for ALGOL 60 were published in the Communications of the ACM, Volume 3, No. 5, May, 1960.

.141 Restrictions Relative to ALGOL 60

(1) Due to limitations of the B 5500 character set (64 characters), lower-case letters are not permitted and different symbols are substituted for ten ALGOL operations (see Paragraph .411).

(2) Unsigned integers may be used as statement labels.

(3) Every statement label must be declared in a LABEL declaration at the head of the innermost block in which it appears.

(4) A procedure or switch must be declared before it can be referenced in a program. (The FORWARD reference declaration makes it possible to handle cases in which, for example, procedure A calls procedure B, which in turn calls procedure A.)

(5) There are 56 reserved words which can never be used as names.

.142 Extensions Relative to ALGOL 60

(1) Complete input-output facilities are provided (see Description above).

(2) STREAM PROCEDURE declarations permit explicit use of the B 5500 Character Mode for operations on "strings" of alphameric characters.

(3) Data items may be of type ALPHA (i.e., a set of up to 6 alphameric characters), in addition to the types REAL, INTEGER, and BOOLEAN.

TABLE I: EXTENDED ALGOL SOURCE AND OBJECT PROGRAM

SOURCE PROGRAM

```
   INTEGER I;
   INTEGER ARRAY A, B, C, D, E, F, G, H [0:100];
   FOR I ← 1 STEP 1 UNTIL 100 DO

BEGIN

   A [I] ← B [I]  + C [I];
   D [I] ← E [I]  + F [I]  + G [I];
   H [I] ← A [I]  x D [I]

END;
```

OBJECT PROGRAM (Symbolic listing; not produced by the Compiler)

LITC 1	DESC D
LITC 3	OPDC I
BFW	OPDC E
OPDC I	OPDC I
LITC 1	OPDC F
ADD	ADD
LITC I	OPDC I
ISN	OPDC G
LITC 144	ADD
LEQ	XCH
LITC 40	ISD
BFC	OPDC I
OPDC I	DESC H
DESC A	OPDC I
OPDC I	OPDC A
OPDC B	OPDC I
OPDC I	OPDC D
OPDC C	MUL
ADD	XCH
XCH	ISD
ISD	LITC 51
OPDC I	BBW

NOTES

DESC A = Descriptor Call for descriptor of the array A.
OPDC I = Operand Call for the operand I.
LITC 40 = Literal Call for the value octal 40 (decimal 32).
Operator syllables are defined in the Instruction List, 203:121.14.

(4) The functions TIME, REAL, and BOOLEAN are provided in addition to the nine functions recommended in the ALGOL 60 report (see Paragraph .411).

(5) The arithmetic operator MOD facilitates operations on moduli; e.g., P MOD 8 is 3 when P is 19.

(6) Parial Word Designators allow operations on specified portions of the word designated by any simple or subscripted variable, function designator, or arithmetic expression enclosed in parentheses; e.g., X. [3:6] specifies use of 6 bits, beginning with bit 3, of the current bit representation of X.

(Contd.)

.142 Extension Relative to ALGOL 60 (Contd.)

(7) The DEFINE declaration causes an identifier to be replaced by its definition wherever it occurs within the block that contains the declaration.

(8) The FILL statement fills one row of an array with a list of specified values.

(9) The MONITOR and DUMP declarations perform useful diagnostic functions, as described in Paragraph 202:181.45.

(10) An additional form of the FOR loop control statement is provided: FOR V ← AE1 STEP AE2 WHILE BE DO. . ., where AE1 and AE2 are arithmetic expressions and BE is a Boolean (true-false) expression.

(11) Two additional iterative statements are provided: DO S UNTIL BE, in which the statement S is repeated until the Boolean expression BE becomes true; and WHILE BE DO S, in which the iteration ceases when the Boolean expression BE becomes false.

(12) A Concatenate expression provides the facility to link together selected bits of named variables to form a concatenated, integer result. The ampersand (&) is used as the Concatenate operator.

(13) A generalized ZIP statement causes all information enclosed by ZIP and END to be recognized by the MCP as Control Card or Program Parameter Card information.

(14) A WAIT statement suspends processing of one program or program segment until a specified condition exists in a designated word location in core storage.

(15) A WHEN statement provides the means to suspend the processing of a program or program segment for a specified number of seconds.

(16) Data communications terminals can be called upon to enter input data by means of a FILL WITH INQUIRY statement. A special form of the WRITE statement is available to send responses to designate terminal units.

(17) Specialized versions of the READ and WRITE statements are available to utilize directly the B 5500's Console Printer-Keyboard.

(18) Specialized versions of the READ and WRITE statements, as well as the new READ SEEK, SPACE, REWIND, and LOCK statements, are provided to control data files stored on Disk File storage.

.15 Publication Date: . . . . November, 1962 (preliminary specifications). December, 1964 (current language manuals).

.2 PROGRAM STRUCTURE

.21 Divisions: . . . . programs are not separated into divisions.

.22 Procedure Entities

Statement: . . . . an imperative description of procedural steps.
a sequence of words; basic statements are separated by semicolons.
Declaration: . . . . defines the characteristics of and assigns identifiers to one or more entities; e.g., variables, arrays, files, switches.
Compound statement: . any number of basic statements, delimited by BEGIN and END.
Block: . . . . any number of declarations, followed by any number of basic statements, compound statements, or blocks, delimited by BEGIN and END.
Program: . . . . a block or compound statement.
Procedure declaration: PROCEDURE, procedure name, formal parameter list, followed by a statement, compound statement, or block.
Procedures may be subroutines or functions and may be called recursively.

.23 Data Entities

File: . . . . a group of related records; e.g., a tape, a deck of cards.
Record: . . . . a group of items transferred by a single input or output statement.
Block: . . . . the data held in a section of external storage.
Array: . . . . a multidimensional arrangement of similar, subscripted items.
Item: . . . . an INTEGER variable or constant.
a REAL (floating point) variable or constant.
a BOOLEAN variable or constant.
an ALPHA item.
String: . . . . a group of alphameric characters delimited by quotes (").

.24 Names

.241 Simple name formation —
Alphabet: . . . . A to Z, 0 to 9.
Size: . . . . 1 to 63 characters.
Avoid key words: . . . yes; 56 reserved words.
Formation rule: . . . . must begin with a letter, and cannot contain spaces or special characters.

.242 Designators —
Procedures: . . . . . . none; LABEL and PROCEDURE declarations must be used to define the type of entity associated with each identifier.

.242 Designators (Contd.)

Data: . . . . none; type, ARRAY, FILE, and SWITCH declarations must be used.
Equipment: . . . . no unit designators in Extended ALGOL; I/O files are specified by label names recognized by the Master Control Program.
Comments: . . . . delimiters COMMENT and ";" or a sequence of characters following END.
Translator control: . none.

.25 Structure of Data Names

.251 Qualified names: . . . . none.
.252 Subscripts —
Number per item: . . unlimited.
Class may be —
Any numeric variable: . . . . . yes.
Literal: . . . . yes.
Expression: . . . . yes.
Form may be —
Signed: . . . . yes.
Truncated fraction: . . . . no.
Rounded fraction: . yes.
.255 Synonyms —
Preset: . . . . by DEFINE.
Dynamically set: . . . no.

.26 Number of Names

.261 All entities: . . . . practically unlimited.
.264 Equipment: . . . . limited by system configuration; equipment is assigned by Master Control Program at run time.

.27 Region of Meaning of Names

.271 Universal names: . . . . none.
.272 Local names: . . . . . . all identifiers are local to the block in which they are declared.
.273 Non-local names —
Designator: . . . . all identifiers not declared in a block are non-local to that block. A non-local identifier has the same meaning as it has in the region within which the current block is nested.
Restrictions: . . . . . . none.

Note: The value of a variable is lost after exit from the block in which it is declared unless it is declared as OWN.

.3 DATA DESCRIPTION

.31 Methods of Direct Data Description

.311 Concise item picture: . yes; FORMAT declarations; e.g., FORMAT IN F3 (A6, X2, 416, 2E9.2, F6.1).
.312 List by kind: . . . . yes; type declarations; e.g., INTEGER I, J, K.
.313 Qualify by adjective: . . no.
.314 Qualify by phrase: . . . no.
.315 Qualify by code: . . . . . no.
.316 Hierarchy by list: . . . no.
.317 Level by indenting: . . . no.
.318 Level by coding: . . . . no.

.32 Files and Reels: . . . . standard B 5500 Label Record is used at beginning and end of all files and reels. File-control portion is 80 characters long and has fixed format.

.33 Records and Blocks

.331 Variable record size: . dynamic.
.332 Variable block size: . . fixed for cards and printer; preset variable for tape.
.333 Record size range: . . . 1 to N blocks.
.334 Block size range —
Punched cards: . . . . 80 columns.
Printer: . . . . 120 or 132 characters.
Magnetic tape: . . . . . 1 to 1,023 words (1 to 4,096 in Read Only mode).
.335 Choice of record size: input-output LIST declarations.
.336 Choice of block size: . FILE declarations or within tape labels.
.337 Sequence control: . . . . 1 or more logical records per READ or WRITE statement.
.338 In-out error control: . automatic, by MCP.
.339 Blocking control: . . . . FILE declaration or tape label.

.34 Data Items

.341 Designation of class: . type declarations.
.342 Possible classes —
Integer: . . . . yes; INTEGER.
Fixed point: . . . . . . no.
Floating point: . . . . . yes; REAL.
Double precision floating: . . . . yes; DOUBLE statement.
Logical: . . . . yes; BOOLEAN.
Alphameric: . . . . . . yes; ALPHA.
Complex: . . . . no.
.343 Choice of external radix: . . . . yes.
.344 Possible external radices —
Decimal: . . . . yes.
Binary: . . . . yes (not for card or printer output).
.345 Internal justification: . automatic right justification for integer, logical, and alpha items.
.346 Choice of external code: . . . . FORMAT declarations.
.347 Possible external codes —
Punched cards: . . . . Hollerith as in Data Code Table or (input only) column binary.
Magnetic tape: . . . . . alphameric as in Data Code Table (203:141.100) or binary.
.348 Internal item size —
Variable size: . . . . . fixed, except strings are preset variable.

(Contd.)

.348 Internal item size (Contd.)

Designation: . . . . . . none, except strings are delimited by quotes (").
Range —
Integer: . . . . 1 word; 39 bits + sign.
Floating point numeric —
Single precision (REAL): . . . . . 1 word; 39 bits + sign for integer part; 6 bits + sign for exponent.
Double precision (DOUBLE): . . . 2 words; 78 bits + sign for integer part; 6 bits + sign for exponent.
Logical (BOOLEAN): 1 word.
Alphameric (ALPHA): . . . . . . 1 word; 6 characters max.
String (in Stream Procedures): . . . . 1 to 63 characters.

Note: Partial Word Designators permit operations on specified portions of the 48-bit word assigned to each variable; e.g., X. [3:6] specifies 6 bits, beginning with bit 3, of X. Also, the Concatenate operator (&) permits linking of specified portions of 48-bit words.

.349 Sign provision: . . . . . optional.

.35 Data Values

.351 Constants:
Possible sizes —
Integer: . . . . 0 to 2^{39}.
Fixed point: . . . . none.
Floating point: . . . 7.8×10^{-56} to 4.3×10^{68}.
Alphameric: . . . . 1 to 6 characters.
Subscriptable: . . . . . yes.
Sign provision: . . . . optional.

.352 Literals: . . . . same as constants, except alphameric literals of up to 63 characters can be used in output FORMAT declarations and in Stream Procedures.

.353 Figuratives: . . . . none.

.354 Conditional variables: . Boolean conditions (true-false) only.

.36 Special Description Facilities

.361 Duplicate format: . . . . by multiple references to a single FORMAT declaration.

.362 Re-definition: . . . . . . none.

.363 Table description —
Subscription: . . . . . . mandatory.
Multi-subscripts: . . . unlimited number.
Level of item: . . . . . variables.

.364 Other subscriptible entities: . . . . none.

.4 OPERATION REPERTOIRE

.41 Formulae

.411 Operator list —

Arithmetic
+ . . . . add (can be unary).
- . . . . subtract (can be unary).
x . . . . multiply.

Arithmetic (Contd.)
/ . . . . divide.
DIV . . . . integer divide; result is truncated.
* . . . . exponentiate.
MOD . . . . modulus.
← . . . . assignment; value of right hand side is assigned to left hand side.
& . . . . concatenate.

Functions
ABS (E) . . . . absolute value of E.
SIGN (E) . . . . produces + 1 if E > 0, 0 if E = 0, or -1 if E < 0.
SQRT (E) . . . . square root of E.
SIN (E) . . . . sine of E.
COS (E) . . . . cosine of E.
ARCTAN (E) . . . . . . arctangent of E.
LN (E) . . . . natural log of E.
EXP (E) . . . . exponential of E.
ENTIER (E) . . . . . . converts type REAL to type INTEGER with truncation.
REAL (E) . . . . permits arithmetic on type BOOLEAN quantities.
BOOLEAN (E) . . . . . permits Boolean operations on arithmetic quantities.
TIME (E) . . . . provides access to an internal clock.

Relational
< . . . . is less than.
≤ . . . . is less than or equal to.
= . . . . is equal to.
≥ . . . . is greater than or equal to.
> . . . . is greater than.
≠ . . . . is not equal to.

Logical
NOT . . . . negation.
AND . . . . logical product.
OR . . . . logical sum.
IMP . . . . implication.
EQV . . . . logical equivalence.

Note: All logical operations are performed on the entire 48-bit word.

.412 Operands allowed —
Classes: . . . . integer or real for arithmetic operators (except DIV and MOD); integer or real for standard functions (results are always real); Boolean for logical operators.
Mixed scaling: . . . . . yes.
Mixed classes: . . . . yes; types integer and real can be mixed in arithmetic expressions, subject to certain restrictions.
Mixed radices: . . . . no.
Literals: . . . . yes.

.413 Statement structure:
Parentheses —
a - b - c means: . . (a - b) - c.
a + b x c means: . . a + (b x c).
a/b/c means: . . . . (a/b)/c.
a^{b^c} means: . . . . . . $(a^b)^c$.
Size limit: . . . . 4,092 generated B 5500 syllables.
Multi-results: . . . . . yes; e.g., A← B← C← X + Y.

.414 Rounding of results: . . automatic when variable on left side of ← operator is type INTEGER.

.415 Special cases —

x = -x: . . . . X ← -X.
x = x + 1: . . . . X ← X + 1.
x = 4.7y: . . . . X ← 4.7 x Y.
x = 5 x 10^7 + y^2: . . . X ← 5 @ 7 + Y * 2.
x = y integer part: . . X ← ENTIER (Y).

.416 Typical examples: . . . X ← (-B + SQRT (B x B -4 x A x C)) / (2 x A).

.42 Operations on Arrays: by own ALGOL coding.

.43 Other Computation

STREAM PROCEDURE declarations permit use of the B 5500 Character Mode for operations on "strings" of alphameric characters. Stream Procedures can be used to facilitate editing, packing and unpacking, and scanning operations. Their overall structure is similar to that of standard ALGOL procedures; but since all ALGOL statements cause the B 5500 to operate in the Word Mode, they cannot be used within a Stream Procedure. Stream statements, in turn, cause operation in the Character Mode and can be used only within Stream Procedure declarations.

The basic function of a Stream Procedure is to operate upon a string of characters from a "source area" and to transfer the edited string to a "destination area." The source index (SI) contains the address of the word, character, and bit currently being processed. The destination index (DI) contains the address of the location where the processed data will be stored.

Stream Statement Types

- Stream address statement: Sets, increments, or stores source or destination index value; e.g., SI ← LOC D sets source index to stack location of stream variable D.

- Destination string statement: Transfers information to destination string from source string or a literal. From 1 to 63 words, characters, or the zone or numeric bit portions of characters can be transferred; octal-to-decimal or decimal-tc-octal conversions can be performed on numeric data in 1-word units; or the source characters can be added to or subtracted from the corresponding destination characters. Examples:

  DS ← 15 CHR transfers next 15 characters from source string to destination string.
  DS ← 6 OCT converts next 6 decimal digits in source string to an octal word in destination string.
  DS ← 7 LIT "HEADING" places the 7-character literal "HEADING" in destination string.

- Stream GO TO statement: transfers control to a labelled statement within the stream block; e.g., GO TO START.

- Skip bit statement: skips the specified number of bits in the source or destination string; e.g., SKIP 5 SB.

- Stream tally statement: Sets, increments, or stores contents of the counter register TALLY, whose value is modulo 64; e.g., TALLY ← TALLY + ALPHA.

- Stream release statement: Causes one buffer of an input file to be filled with new data or the contents of one buffer of an output file to be sent to an output device; e.g., RELEASE (FILEA).

- Conditional stream statement: Compares source string with destination string or a literal; tests value of a source bit; tests true-false toggle setting, or tests whether a source character is a letter or digit. If tested condition is false, the stream statement following THEN is ignored; e.g., IF SC = "-" THEN GO TO NEG transfers control to NEG if the source character is a minus sign.

- Stream nest statement: Controls the execution of a loop formed from stream statements; e.g., 10 (IF SC = "E" THEN JUMP OUT; SI ← SI + 1; TALLY ← TALLY + 1) increments both source index and TALLY by 1 ten consecutive times unless a source character "E" is found, in which case control is transferred to next statement after the right parenthesis.

.44 Data Movement and Format

.441 Data copy example: . . Y ← X.
.442 Levels possible: . . . . items only.
.443 Multiple results: . . . . yes; e.g., X ← Y ← Z.
.444 Missing operands: . . . not possible.

.445 Size of operands —

Exact match: . . . . . . implied, except in input-output editing and Stream Procedures.
Alignment rule —
Numbers: . . . . right justified or normalized.
Alpha: . . . . right justified.
Filler rule —
Numbers: . . . . zeros.
Alpha: . . . . zeros.
Truncating rule —
Numbers: . . . . truncate at left.
Alpha: . . . . truncate at left.
Variable size destination: . . . . . no.

.446 Editing possible —

Change class: . . . . . yes.
Change radix: . . . . . yes.
Insert editing symbols —
Actual point: . . . . . automatic.
Suppress zeros: . . . automatic.
Insert: . . . . sign, point.
Float: . . . . - sign only.

.447 Special moves: . . . . . in Stream Procedures: transfer 1 to 63 characters or words from source string to destination string; see Paragraph .43.

.448 Code translation: . . . . performed automatically as necessary.

.449 Character manipulation: . . . . . in Stream Procedures; see Paragraph .43.

(Contd.)

.45 File Manipulation

Open: . . . . automatic, by first reference to a file.
Close: . . . . automatic when exit is made from block in which the FILE declaration or CLOSE statement appears. For magnetic tape files the following options are available: rewind for further program use; rewind and lock; rewind and release to system; or do not rewind.
Advance to next record: READ, WRITE, SPACE, or RELEASE.
Step back a record: . . SPACE or READ REVERSE.
Set restart point: . . . . none.
Restart: . . . . none.
Start new reel: . . . . . automatic, by MCP.
Start new block: . . . . . automatic.
Search on key: . . . . . . none.
Rewind: . . . . see "Close," above.
Unload: . . . . none.

Note: READ REVERSE specifies that a magnetic tape file shall be read backward.

.46 Operating Communication

.461 Log of progress: . . . . typed messages, controlled by MCP.
.462 Messages to operator: typed messages.
.463 Offer options: . . . . . . typed messages.
.464 Accept option: . . . . . . keyboard entries.

.47 Object Program Errors

Error	Discovery	Special Actions
Overflow:	hardware interrupt	permit programmer-specified action; if none, type message and terminate program.
In-out:	hardware interrupt	(same as above)
Invalid data:	hardware check	type message.

.5 PROCEDURE SEQUENCE CONTROL

.51 Jumps

.511 Destinations allowed: . any named statement within current block, or beginning of any named block.
.512 Unconditional jump: . . GO TO N.
.513 Switch: . . . . SWITCH S ← N, P, Q; GO TO S [I].
.514 Setting a switch: . . . . I ← 2.
.515 Switch on data: . . . . . as above.

.52 Conditional Procedures

.521 Designators —
Condition: . . . . IF.
Procedure: . . . . THEN.
.522 Simple conditions —
Expression vs. expression: . . . . . . yes.
Expression vs. variable: . . . . yes.
Expression vs. literal: . . . . yes.
Expression vs. figurative: . . . . . . no.
Expression vs. condition: . . . . no.
Variable vs. variable: . . . . yes.
Variable vs. literal: . yes.
Variable vs. figurative: . . . . no.
Variable vs. condition: . . . . no.
Conditional value: . . no.
.523 Conditional relations —
Equal: . . . . =
Greater than: . . . . . >
Less than: . . . . <
Greater than or equal: . . . . ≥
Less than or equal: . ≤
.524 Variable conditions: . . true/false implied.
.525 Compound conditions —
IF x AND y: . . . . . . IF X AND Y THEN. . .
IF x OR y: . . . . IF X OR Y THEN . . .
IF x DO a AND y DO b: . . . . IF X THEN A ← A + 1; IF Y THEN B ← B + 1.
IF x DO a OR y DO b: . . . . IF X THEN A ← A + 1 ELSE IF Y THEN B ← B + 1.
.526 Alternative designator: ELSE (optional).
.527 Condition on alternative: . . . . unrestricted.
.528 Typical examples: . . . IF A > B THEN A ← A + 1 ELSE IF C = D THEN GO TO N ELSE GO TO ERROR.
IF X AND Y THEN FOR I ← 1 STEP 1 UNTIL 20 DO A [I] ← B [I] + C.

.53 Subroutines

.531 Designation —
Single statement: . . . same as set.
Set of statements —
First: . . . . PROCEDURE P (where P is name of subroutine).
Last: . . . . END.
.532 Possible subroutines: . block, compound statement, or basic statement.
.533 Use in-line in program: no.
.534 Mechanism —
Cue with parameters: P (X, Y + Z, 25).
Number of parameters: . . . . . 128.
Cue without parameter: . . . . . . P.
Formal return: . . . . implied after last procedure before END delimiter.
Alternative return: . . GO TO implied formal return or to explicit statement outside of subroutine.
.535 Names —
Parameter call by value: . . . . yes, if listed in VALUE declaration.

.535 Names (Contd.)
Parameter call by
name: . . . . yes, if not listed in VALUE declaration.
Non-local names: . . . yes, implied by no local definition.
Local names: . . . . . yes.
Preserved local
variables: . . . . only those declared OWN.
.536 Nesting limit: . . . . . . limited only by stack size, which is variable.
.537 Automatic recursion
allowed: . . . . yes.

.54 Function Definition by Procedure

.541 Designation —
Single statement: . . . same as set.
Set of statements —
First: . . . . Type PROCEDURE F (where F is function name and Type is REAL, INTEGER, BOOLEAN, or ALPHA).
Last: . . . . END.

.542 Level of procedure: . . block, compound statement, or basic statement.
.543 Mechanism —
Cue: . . . . function name in expression, followed by parameter list; e.g., X←Y + F (A, B + C).
Formal return: . . . . implied after last procedure before END delimiter.

.544 Names —
Parameter call by
value: . . . . yes.
Parameter call by
name: . . . . yes.
Non-local names: . . . yes.
Local names: . . . . . yes.
Preserved local
variables: . . . . only those declared OWN.

Note: Variable having same name as function must appear on left side of an assignment statement within the function procedure body.

.55 Operand Definition by Procedure

.551 Designation: . . . . same as .541.
.552 Level of procedure: . . same as .542.
.553 Mechanism: . . . . same as .543, but no parameters are used.
.554 Names —
Non-local names: . . . yes.
Local names: . . . . . yes.
Preserved local
variables: . . . . only those declared OWN.

.56 Loop Control

.561 Designation of loop: . . simple statement immediately following the FOR clause, or compound statement delimited by BEGIN and END.
.562 Control by count: . . . . no.
.563 Control by step —
Example: . . . . FOR V ← 2 STEP 1 UNTIL N DO . . . .
Parameter: . . . . arithmetic expression.
Step: . . . . arithmetic expression.
Criteria: . . . . until greater than end value when step is positive, less when negative.
Multiple parameters: yes.
.564 Control by condition —
Example: . . . . FOR V←3 x V WHILE A > B DO. . .
Combined with step: . optional; e.g., FOR V ← 1 STEP 1 WHILE A > O DO. . .
.565 Control by list: . . . . . FOR V ← 1, 5, 6 STEP 2 UNTIL 20, 25 DO. . .
.566 Nesting limit: . . . . . . none.
.567 Jump out allowed: . . . yes.
.568 Control variable
exit status: . . . . available while in loop and after jump out via GO TO; not available after FOR list has been satisfied.

.6 EXTENSION OF THE LANGUAGE: . . . . . . none, except by user-coded ALGOL or Stream Procedures.

.7 LIBRARY FACILITIES

.71 Identity: . . . . B 5500 Program Library.

.72 Kinds of Libraries

.721 Fixed master: . . . . . . no.
.722 Expandable master: . . yes.
.723 Private: . . . . yes.

.73 Storage Form: . . . . . . magnetic tape (punched cards in non-tape systems).

.74 Varieties of Contents: . compiled programs in machine code.
procedures (subroutines) in source language.

.75 Mechanism

.751 Insertion of new item: . by MCP, using control cards.
.752 Language of new item: ALGOL, COBOL, or machine code.
.753 Method of call: . . . . . procedures called by use of their names in source program.

.76 Type of Routine

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is
variable: . . . . no.

(Contd.)

.8 TRANSLATOR CONTROL

.81 Transfer to Another Language: . . . . Stream Procedures, described in Paragraph .43, permit use of the B 5500 Character Mode for operations on "strings" of alphameric characters.

.82 Optimizing Information Statements

.821 Process usage statements: . . . . none.
.822 Data usage statements: none.

.83 Translator Environment: . . . . . none.

.84 Target Computer Environment: . . . . . none.

.85 Program Documentation Control: . . . . compile with or without source program listing.

.9 TARGET COMPUTER ALLOCATION CONTROL

.91 Choice of Storage Level: . . . . none.

.92 Address Allocation: . . none.

.93 Arrangement of Items in Words in Unpacked Form: . . . . . standard for numeric.

.94 Assignment of Input-Output Devices: . . . . none; performed by MCP.

.95 Input-Output Areas: . . size (in words) and number of buffer areas for each file are specified in FILE declaration or in the input tape label.

PROCESS ORIENTED LANGUAGE: COBOL

.1 GENERAL

.11 Identity: . . . . COBOL-61 Extended.

.12 Origin: . . . . Burroughs Corporation.

.13 Reference: . . . . COBOL Reference Manual for the Burroughs B 5500.

.14 Description

COBOL-61 Extended for the Burroughs B 5500 is a comprehensive version of the Department of Defense's COBOL-61 Extended language. All of Required COBOL-61 has been implemented, as well as most of the elective features of COBOL-61. Two of the three principal extensions of COBOL-61 Extended — the SORT verb and the Mass Storage features — have been implemented in varying degrees of completeness, and Burroughs has also included several other useful extensions to permit the direct use of data communications terminal units. The Report Writer facility of COBOL-61 Extended has not been implemented. The extensions of B 5500 COBOL-61 with respect to Required COBOL-61 are listed in Paragraph .142, and the COBOL-61 elective features implemented are listed in Paragraph .143.

The Mass Storage language extensions of B 5500 COBOL are designed to permit efficient use of the Burroughs Disk File system while programming in the COBOL language. The constructs provided in B 5500 COBOL represent a subset of the Mass Storage language accepted by the CODASYL Maintenance Committee. The principal area of Mass Storage language facilities not implemented in B 5500 COBOL is that of asynchronous or "out-of-line" processing. However, provisions are included in the language to permit overlapping of record accessing and normal processing.

Data record accessing can be specified as RANDOM or SEQUENTIAL in the special Mass Storage (MD) File Section of the Data Division. The sequential access mode can utilize multiple buffer areas as specified in the ASSIGN nn ALTERNATE AREAS clause of the Environment Division's SELECT statement. Within the Mass Storage File Description section, it is possible to specify the size of the data blocks and records, the type of file label records, the file's SAVE-FACTOR, the symbolic or actual record address key, the size of the file, and the limits of the portion of the file that can be accessed during the execution of this program.

Based on this information, the COBOL compiler and the Disk File Master Control Program make provisions to read and record data records in one of two modes, called Technique-A and Technique-P. Technique-A calls for a fixed number of fixed-length records within a data block. If a block does not utilize all of the character positions of the 240-character Disk File segment, the unused character positions are wasted. Technique-A can support either the Random or Sequential access methods. Technique-P — not implemented to date — packs records consecutively onto the Disk File, without regard to whether the beginning or end of a record coincides with the beginning or end of a Disk File segment. Variable-length records can be used with this data-organization technique, but can be accessed only in the sequential mode. Fixed-length records can also be used with Technique-P, and can be accessed in either the sequential or random mode.

The Mass Storage procedural statements provide special versions of READ, WRITE, OPEN, and CLOSE to provide input-output routines specifically designed for the Burroughs Disk File. The WITH LOCK option of the OPEN and CLOSE statements permits the program to have exclusive use of named files unless overruled by operator intervention. The CLOSE statement can also specify that specific files be PURGED from the system after their current use is terminated. The INVALID KEY clause of the READ and WRITE statements permits control to be transferred if an actual key address is recognized as being beyond the preset limits of the program. The verb SEEK enables a record search to begin without delaying the direct-line processing. Two special versions of the MOVE statement and the USE FOR KEY CONVERSION statement provide flexible facilities to control programmer-supplied key conversion algorithms.

In May, 1965, Burroughs announced its implementation of several new COBOL constructs to permit the B 5500's data communications terminal units to be controlled directly by COBOL programmers. The ACCEPT DATA statement makes input messages entered thru a data communications network available to the program. If no message is in the specified terminal unit's input buffer, the Master Control Program suspends processing until a message is available. The WRITE...ON... construct provides the facility to output computer responses to specified terminal units. Normal COBOL constructs, such as OPEN OUTPUT and CLOSE, are also used with data communications devices.

Several additional language facilities have been added that will increase programming flexibility in data communications environments. The MOVE END statement moves the end-of-message character (←) to its desired location when formulating computer responses. The WHEN and UNTIL statements suspend processing of the current program segment, either for a specified number of seconds (WHEN), or until a specified condition is satisfied (UNTIL). The ASSIGN TO MEMORY

(Contd.)

.14 Description (Contd.)

declaration with the Data Division reserves, for the named data array, a permanent residence in the system's storage in preparation for later transmission to another computer or to a remote data communications device. All data communications output files are also identified in the Environment Division by means of a new ASSIGN TO DATA construct.

COBOL for the B 5500 also includes a complete implementation of the SORT extension to COBOL-61. Both the Basic and Extended SORT facilities are provided, enabling any number of SORT statements to appear within the Procedure Division of a program. The amount of core storage and the number of magnetic tape or disc units to be used for the sorting operation can be specified in the Environment Division. The file to be sorted is specified in a separate File Description (SD) section within the Data Division, where the approximate file size and record characteristics are entered. The SORT verb itself contains several options that permit specifying either ascending or descending sorting sequence, and whether a simple sort or a programmer-monitored sort should take place. The INPUT PROCEDURE option enables the programmer to edit records before sorting and to present only selected records to the sort operation by means of the RELEASE clause. Similarly, the OUTPUT PROCEDURE option of the SORT verb allows the programmer to access each sorted record through use of the RETURN clause.

.141 Availability

Language: . . . . March 1963 and May 1965.
Compiler: . . . . April 1963.

.142 Deficiencies of B 5500 COBOL-61 With Respect to Required COBOL-61

No deficiencies are known to exist.

.143 Extensions of B 5500 COBOL-61 With Respect to Required COBOL-61

(1) The verbs SORT, MERGE, RELEASE, and RETURN.

(2) Various Mass Storage statements, including the SEEK verb, control sequential or random processing on Disk Files.

(3) Various data communications device constructs, such as ACCEPT DATA, WRITE ON, and MOVE END.

(4) The following relational symbols:

$=$ . . . . equal to.
$>$ . . . . greater than.
$<$ . . . . less than.
$\geq$ . . . . equal to or greater than.
$\leq$ . . . . equal to or less than.
$\neq$ . . . . unequal to.

(5) The source language debugging aids MONITOR and DUMP.

(6) The CORRESPONDING option of the ADD and SUBTRACT verbs.

(7) The intrinsic functions: ABS, ARCTAN, COS, EXP, LN, SIGN, SIN, and SQRT.

(8) The ability to refer to a data item either by its name or by an arbitrary synonym.

(9) The use of arithmetic expressions as subscripts.

(10) The use of a virtually unlimited number of subscripts.

(11) The ability to use abbreviations for certain terms in the Data Division, such as CMP for Computational, PT for Point Location, and PC for PICTURE.

(12) The ZIP function for communicating with other COBOL or ALGOL programs.

(13) The RERUN statement for program restarts.

(14) Formulae are permitted in the GO TO... DEPENDING ON statement, and in the FROM and BY clauses of the VARYING option of the PERFORM verb.

(15) I/O Channel specification is permitted in the WRITE statement.

(16) Unlimited AFTER clauses within the PERFORM statement.

(17) The WHEN and UNTIL statements to suspend processing.

(18) The sequence of procedures associated with a PERFORM statement may overlap or intersect the sequence associated with another PERFORM statement, even if either sequence includes the PERFORM statement associated with the other sequence.

.144 COBOL-61 Electives Implemented in B 5500 COBOL (see 4:161.3)

Key No.	Elective	Comments
	Characters and Words	
1	Formula characters	+, -, *, /, **, =, ( ).
2	Relationship characters	=, <, >.
3	Semicolon	always ignored.
6	Figurative constants	HIGH-VALUE(S); LOW-VALUE(S).
7	PREPARED FOR Computer-Name	labels data descriptions applicable to several computers.
	File Description Clauses	
8	Block-size	allows a range to be specified.
9	FILE CONTAINS	indicates approximate file size.
11	SEQUENCED-ON	gives a list of keys to be sequence-checked.
12	HASHED	hash total checking can be specified.
	Record Description Clauses/Options	
13	Table-length	allows variable-length tables and arrays.
16	RANGE IS	gives value range of item or character.
17	RENAMES	permits overlapping of variable items.
18	SIGN IS	allows sign of data item to be named.
19	Item-length	allows variable-length items to be specified in SIZE clause (see also 16).
20	Conditional-range	allows a conditional-value to be a range.
	Verbs	
22	COMPUTE	algebraic formulae.
25	INCLUDE	calls library routines.
26	USE	amplifies I/O error and labeling routines.
	Verb Options	
27	LOCK	locks rewound tapes and files on disc storage.
28	MOVE CORRESPONDING	moves and edits matching records.
29	OPEN REVERSED	allows reading tapes backwards.
30	ADVANCING paper	gives specific paper advance.
32	Formulas	algebraic formulae, as used in COMPUTE verb.
33	Operand-size	up to 18 digits.
34	Relationships	IS UNEQUAL TO, EQUALS, and EXCEEDS.
35	Tests	IF { } IS NOT ZERO.
36	Conditionals	implied objects with implied subjects.
37	Compound conditions	ANDs or ORs.
38	Complex conditionals	additional conditions following OTHERWISE and ELSE.
39	ON SIZE ERROR	provides extension of error routines.
	Environment Division	
41	OBJECT-COMPUTER	allows selective use of previous descriptions; MEMORY SIZE clause is used only by the SORT generator; size is determined automatically by MCP.
46	I/O Control	allows programmer control; SAME AREA clause not implemented.
	Identification Division	
47	DATE	gives compilation date.
	Special Features	
48	LIBRARY	allows calls of library routines.

(Contd.)

.145 COBOL-61 Electives Not Implemented (see 4:161.3)

Key No.	Elective	Comments
	Characters and Words	
4	Long literals	more than 120 characters.
5	Figurative constants	UPPER-BOUND(S); LOWER-BOUND(S).
	File Description Clauses	
10	Label formats	allows new or library formats.
	Record Description Clauses/Options	
14	Item-length	allows length specification in PICTURE clause (see also 19).
15	Bit usage	allows items to be specified in binary.
21	Label-handling	provides free handling of labels.
	Verbs	
23	DEFINE	constructs new verbs and statements.
24	ENTER	changes to another language.
	Verb Options	
31	STOP	non-alphabetic display provision; B 5500 always has an alphabetic display device on-line.
	Environment Division	
40	SOURCE-COMPUTER	allows selective use of previous description.
42	SPECIAL NAMES	specifies switches for ACCEPT, WRITE, and DISPLAY verbs; B 5500 has no sense switches.
43	File Description	can be taken from library.
44	PRIORITY is	allows priorities to be given for multi-programming; B 5500 priorities are provided by control cards and altered as required by the MCP.
45	I/O Control	can be taken from library.
	Special Features	
49	SEGMENTATION	allows assignment of segment priorities by programmer; B 5500 segmentation is handled by MCP.

PROCESS ORIENTED LANGUAGE: FORTRAN IV

.1 GENERAL

.11 Identity: . . . . B 5500 FORTRAN IV.

.12 Origin: . . . . Burroughs Corporation.

.13 Reference: . . . . Preliminary Edition of FORTRAN IV for Burroughs B 5500.

.14 Description:

FORTRAN IV for the Burroughs B 5500 Information Processing System is a virtually complete implementation of the FORTRAN programming language as proposed by the X.3.4.3 FORTRAN Group of the American Standards Association, and as published in Communications of the ACM, October, 1964. (This proposed standard version of the FORTRAN language corresponds to what is commonly known as FORTRAN IV.) In comparison to this standard, B 5500 FORTRAN lacks the provisions to handle double-precision and complex variable items. All other FORTRAN IV language facilities have been included.

FORTRAN IV for the B 5500 is designed to duplicate, wherever possible, the facilities of the IBM 7090/7094 FORTRAN IV language to facilitate conversions of scientific and engineering installations to the B 5500. Burroughs has developed a translator program called FORGOL 4 (see Section 203:183.100) that converts FORTRAN IV programs into Extended ALGOL; Burroughs' time-proved ALGOL compiler then completes the translation/compilation operation.

A general description of the IBM 7090/7094 FORTRAN IV language is presented in Section 408:162. The restrictions and extensions of B 5500 FORTRAN IV relative to the IBM version are listed in Paragraphs .142 and .143, respectively, of this report section.

A potential area of difficulty in the use of B 5500 FORTRAN IV lies in the fact that FORTRAN does not require the programmer to arrange the source program in logical segments. Yet the ALGOL compiler that ultimately produces the object program deck attempts to break up the program into segments containing a maximum of 1,023 48-bit words. Therefore, unless the FORTRAN program can be divided into segments containing no more than 1,023 words of object coding — either naturally or by design — the compiler will generate an error message for oversized segments. The program will then have to be modified, either at the FORTRAN source program level or at the intermediate Extended ALGOL level.

Burroughs has not implemented any FORTRAN language facilities to permit direct use of its Disk File storage units, although the Disk File Master Control Program (MCP) can make the Disk File facilities available in an indirect manner. Similarly, there has been no implementation of FORTRAN language constructs to make use of the several varieties of B 5500 data communications devices.

.141 Availability

Language specifications: . . . . December, 1964.
Translator (FORGOL 4): . . . . October, 1964.

.142 Restrictions of B 5500 FORTRAN IV Relative to IBM 7090/7094 FORTRAN IV

(1) The TYPE specification for constants and variables does not include the DOUBLE PRECISION or COMPLEX options.

(2) All intrinsic functions concerned with double-precision or complex variables have been excluded.

.143 Extension of B 5500 FORTRAN IV Relative to IBM 7090/7094 FORTRAN IV

(1) Integer constants can range to 2^{39-1} as compared to 2^{35-1} in 7090/7094 FORTRAN IV; real (floating-point) constants can range from 10^{-46} to 10^{+69} as compared to the 10^{-38} to 10^{+38} range of 7090/7094 FORTRAN IV.

(2) The B 5500's relational symbols can be used as desired in place of the standard FORTRAN relational operators, as follows:

$>$ for .GT.
$\geq$ for .GE.
$<$ for .LT.
$\leq$ for .LE.
$\neq$ for .NE.
$=$ for .EQ.

(3) The logical quantities .TRUE. and .FALSE. can be represented by the letters T and F in DATA statements.

(4) The numeric value of statement labels can range to 99,999 instead of the standard 32,768.

(5) The Logical IF statement can include both another IF statement and a DO statement.

(6) Source language debugging facilities are provided through use of the MONITOR and DUMP statements.

PROGRAM TRANSLATOR: EXTENDED ALGOL

.1 GENERAL

.11 Identity: . . . . Extended ALGOL Compiler.

.12 Description

The Extended ALGOL Compiler is a single-pass routine that translates source programs written in the Extended ALGOL language (see Section 203:161) into B 5500 object programs in segmented, relocatable machine-language form. The Compiler occupies about 10,000 locations on Storage Drum 1 or 10 tracks of the Disk File, and is called into core storage by the Master Control Program when a header card indicates that an ALGOL source program is to be compiled and added to the program library, or checked for syntactic errors without compilation.

The ALGOL compiler delivers translation speeds ranging between 600 and 800 source program cards (or up to 2500 magnetic tape card images) per minute. Object program efficiencies of 90 to 95 percent relative to the best hand coding have been achieved, according to Burroughs.

The combination of fast translation and high object program efficiency was the primary goal in the design of the B 5500 hardware and the Master Control Program. Among the factors that contribute to the efficiency of the B 5500 ALGOL compiler are the following:

- Recursive use of procedures is implemented at the hardware level. (The ALGOL Compiler itself consists of about 90 procedures, each of which can use any other procedure, including itself.)
- Fixed-point and floating-point numbers are represented in the same form, so conversions and checks for mixed arithmetic are unnecessary.
- Any Input/Output Channel can reference any peripheral device.
- The B 5500 Character Mode facilitates editing, scanning, and radix conversions, while the Word Mode permits efficient arithmetic and logical operations.
- Automatic temporary storage for intermediate results and subroutine parameters is provided by the stack.
- Overlays of program segments and data arrays are handled automatically by the Processor and the MCP.
- Storage protection for data arrays and program segments is provided by the hardware.
- The same registers are used for indexing and arithmetic operations.
- Floating-point numbers can be automatically converted to integers during indexing and storing operations.
- Literals between and 0 and +1,023 can be incorporated directly into the program stream.
- Comprehensive hardware facilities are provided for detection and servicing of interrupt conditions.

Segmentation of the object program is performed by the compiler. Each ALGOL block becomes a separate program segment that is referenced by a Descriptor in the Program Reference Table. The Descriptor specifies the current drum or disk and core addresses of the segment and indicates whether or not it is currently loaded in core storage. No segment may exceed 1,023 words in length, so very long source language blocks may have to be divided into sub-blocks by the programmer. The use of short blocks is recommended for efficiency in storage allocation and in multiprogramming situations. The main restriction on overall object program size is the Program Reference Table, which is limited to 1,023 entries. The ALGOL Compiler itself requires about 650 PRT entries.

The compiler has access to the procedures, or subroutines, which are stored on the Program Library Tape in ALGOL source-language form. When a procedure is required, it is called from the library and translated along with the source program. This system facilitates multiprogramming and makes possible a listing of the complete source program, including all procedures; it also means that a single frequently-used procedure may require multiple storage areas (one area for each program being run at the same time which uses the procedure).

Input-output editing and format control operations are carried out by standard routines. Intrinsic functions are called in at object time, except for ABS, SIGN, and ENTIER, which are inserted in-line at compile time. No instructions are generated for REAL and BOOLEAN; they are temporary declarations to prevent error messages at compile time.

.12 Description (Contd.)

Diagnostics can be incorporated into the object program by the source-language declarations MONITOR and DUMP, which are described in Paragraphs .451 and .452. The printouts produced by these declarations facilitate source-language debugging. This facility, together with the high translation speeds of the B 5500, makes it practical to do all debugging in the ALGOL language and retranslate the whole program at each stage of the debugging process.

.13 Originator: . . . . . . Burroughs Corporation.

.14 Maintainer: . . . . . . Burroughs Corporation.

.15 Availability: . . . . . April, 1963.

.2 INPUT

.21 Language

.211 Name: . . . . Extended ALGOL for the Burroughs B 5500, Section 203:161.
.212 Exemptions: . . . . . none.

.22 Form

.221 Input media: . . . . . punched cards or magnetic tape.

.222 Obligatory ordering: . . . . . . header card first, then source deck in logical sequence; all declarations for a block must appear at the head of the block, and procedures and switches must be declared before they can be used (unless a FORWARD reference is used).

.23 Size Limitations

.231 Maximum number of source statements: . . . . limited by target computer storage.

.232 Maximum size source statements: . . . . 4,092 generated B 5500 syllables per ALGOL block.

.233 Maximum number of data items: . . . . . practically unlimited.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . B 5500 machine code.
.312 Language style: . . . fully relocatable.
.313 Output media: . . . . magnetic tape or disc storage.

.32 Conventions

.321 Standard inclusions: none

.322 Compatible with: . . Master Control Program

.33 Documentation

Subject	Provision
Source program: . .	optional listing.
Object program:. . .	optional listing.
Storage map:	none.
Restart point list:. .	none.
Language errors: . .	listing.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes: one-pass translator.

.42 Optional Modes

.421 Translate: . . . . . . yes.
.422 Translate and run: . yes.
.423 Check only: . . . . . . yes.
.424 Patching: . . . . no.
.425 Translate and add to library: . . . . . yes.

.43 Special Features

.431 Alter to check only: no.
.432 Fast unoptimized translate: . . . . . . no.
.433 Short translate on restricted program: . . . . no.

.44 Bulk Translating: . . yes.

.45 Program Diagnostics

.451 Tracers: . . . . MONITOR declarations cause the identifier and current value of each listed variable to be written on the designated file each time it is used as a "left-hand part" in an assignment statement. Listed switch identifiers, label identifiers, and procedure identifiers used as function designators are also written each time they are encountered in the object program.
.452 Snapshots: . . . . . . DUMP declarations cause specified data to be written on a designated file whenever a labelled statement has been executed a specified number of times. The output may include: variable identifiers with their current values, array identifiers with current values of all their elements, and statement labels with tallies of the number of times they have been executed.

(Contd.)

.453 Dumps: .... not incorporated in source programs.

.46 Translator Library

.461 Identity: .... B 5500 Program Library.
.462 User restriction: .. general.
.463 Form —
Storage medium: . magnetic tape or disc file.
Organization: ... multi-file tape and disc libraries.
.464 Contents —
Routines: ...... yes; closed procedures in source language.
Functions: ..... yes.
Data descriptions: no.
Compiled programs: .... yes, in relocatable machine code.
.465 Librarianship —
Insertion: ...... by MCP, using control cards.
Amendment: .... by MCP, using control cards.
Call procedure: .. use of name in source program.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead —

Name	Space
Master Control Program:	1,600 core locations. 15,000 drum locations. 1,000 Disk File segments.
Read-Write routine:	included in MCP on drum or disc storage.
File Control routine:	included in MCP on drum or disc storage.

.512 Space required for each input-output file: .... number and size of buffer areas for each file are specified in FILE declarations.
.513 Approximate expansion of procedures: .... varies widely; the following examples show number of program syllables generated by specific ALGOL statements.

Statement	Program syllables
FOR I ←STEP 1 UNTIL 100 DO:	14.
J ← J + 2:	5.
C [I] ← A [I] + B [J]:	9.

.52 Translation Time

.521 Normal translating:. approx. 600 to 800 source-program cards per minute (up to 2,500 source-program card images per minute when I/O is via magnetic tape).
.522 Checking only: .... same as above times.
.53 Optimizing Data: .. no explicit data.
manufacturer recommends coding in long statements (to reduce number of unnecessary storage accesses) and short blocks (to facilitate segmentation).
allocation of target computer storage and input-output devices is performed by the MCP.
.54 Object Program Performance: ... according to Burroughs, typical object program efficiency is 90 to 95% relative to best hand coding for both time and space.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: .... any B 5500 system; see System Configuration, Section 203:031.
.612 Larger configuration advantages: ..... magnetic tape and/or disc storage input, output, and handling of the program library.

.62 Target Computer

.621 Minimum configuration: .... any B 5500 system.
.622 Usable extra facilities: ...... all; allocated automatically by the MCP.

.7 ERRORS, CHECKS, AND ACTION: ... checks provided will catch nearly all syntactic errors.

.8 ALTERNATIVE TRANSLATORS: . none.

PROGRAM TRANSLATOR: EXTENDED COBOL

.1 GENERAL

.11 Identity: . . . . Extended COBOL Compiler.

.12 Description

The Extended COBOL Compiler translates source programs written in the COBOL language described in Section 203:162 into B 5500 machine-language object programs in a single pass. The Compiler occupies about 30,000 locations on the Storage Drums or about 1145 30-word segments on the Disk File, and is called into core storage by the Master Control Program whenever a header card indicates that a COBOL source program is to be compiled. The header card precedes the source deck and also indicates whether the program shall be compiled and run immediately, compiled and added to the program library, or checked for syntactic errors without compilation. The MCP treats the COBOL Compiler much like any other production program, and other programs can be compiled and/or executed concurrently with the COBOL compilation.

Translation speeds of up to 800 source program cards per minute have been achieved, as well as object program efficiencies of 90 to 95 percent relative to the best hand coding. Some of the factors that contribute to the translation speed and efficiency are listed in Paragraph 203:181.12. COBOL object programs use both the Word and Character Modes, automatically entering the mode that is generally most efficient for each type of operation.

Segmentation of the object program is performed by the compiler. Each paragraph of the Procedure Division becomes a separate program segment that is referenced by a Descriptor in the Program Reference Table. The Descriptor specifies the current drum/disc and core addresses of the segment and indicates whether or not it is currently loaded in core storage.

Since no program segment may exceed 1,023 words in length, very long source language paragraphs may have to be divided into sub-sections by the programmer. The use of relatively short paragraphs is recommended for efficiency in storage allocation and multiprogramming. The main restriction on object program size is the Program Reference Table; it is limited to 1,023 entries, which should be entirely adequate for most purposes. The compiler has access to the procedures, or subroutines, which are stored on the Program Library Tape in COBOL source-language form. Required procedures are called from the library and translated along with the source program.

Source-language debugging is facilitated by the COBOL extensions MONITOR and DUMP, described in Paragraph .45 of this report section.

.13 Originator: . . . . Burroughs Corporation.

.14 Maintainer: . . . . Burroughs Corporation.

.15 Availability: . . . . . . September, 1963.

.2 INPUT

.21 Language

.211 Name: . . . . COBOL 61 for the Burroughs B 5500, Section 203:162.

.212 Exemptions: . . . . . . none.

.22 Form

.221 Input media: . . . . . . punched cards and/or magnetic tape.

.222 Obligatory ordering: . . . . . . Header Card.
Identification Division.
Environment Division.
Data Division.
Procedure Division.

.223 Obligatory grouping: . . . . by division and section.

.23 Size Limitations

.231 Maximum number of source statements: . limited by target computer disc or drum storage.

.232 Maximum size source statements: . 4,092 generated B 5500 syllables per COBOL paragraph.

.233 Maximum number of data items: . . . . practically unlimited.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . . B 5500 machine code.
.312 Language style: . . . . fully relocatable.
.313 Output media: . . . . . magnetic tape or disc storage.

.32 Conventions: . . . . . . compatible with MCP.

.33 Documentation

Subject	Provision
Source program:	optional listing.
Object program:	optional listing.
Storage map:	none.
Restart point list:	listing.
Language errors:	listing.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes: . . one-pass translator.

.42 Optional Modes: . . . . translate only, translate and run, translate and add to library, or check only.

.44 Bulk Translating: . . . . yes.

(Contd.)

.45 Program Diagnostics

.451 Tracers: . . . . MONITOR declarations in the source program cause the identifier and current value of each listed item to be written on the designated file each time the value changes. The "current value" of a procedure name is the number of times the name has been encountered.

.452 Snapshots: . . . . DUMP declarations in the source program cause the identifier and current value of each listed item to be written on the designated file whenever a specified procedure name has been encountered a specified number of times.

.453 Dumps: . . . . not incorporated in source programs; MCP dumps any specified program on tape or printer upon keyboard request.

.46 Translator Library

.461 Identity: . . . . B 5500 Program Library.

.462 User restriction: . . . . general.

.463 Storage medium: . . . . magnetic tape or disc file.

.464 Contents: . . . . open and closed procedures, functions, data and environment descriptions.

.465 Librarianship —

Insertion: . . . . by MCP, using control cards.

Amendment: . . . . . . by MCP, using control cards.

Call procedure: . . . . use of name after PERFORM, INCLUDE, or USE verb in source program.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead —

Name	Space
Master Control Program:	1,600 core locations. 15,000 drum locations. 1,000 Disk File segments.
Read-Write routine:	included in MCP on drum or disc storage.
File Control routine:	included in MCP on drum or disc storage.

.512 Space required for each input-output file: . . . . controlled by user: RESERVE n ALTERNATE AREAS.

.513 Approximate expansion of procedures: . . . . approx. 12 syllables per source-program card.

.52 Translation Time

.521 Normal translating: . approx. 0.00125S minutes, where S is number of source program cards.

.522 Checking only: . . . . . same as above times.

.53 Optimizing Data: . . . alternate input-output areas can be assigned to files.
coding in short paragraphs facilitates segmentation and multiprogramming.
use of COMPUTE rather than ADD, MULTIPLY, etc., can reduce number of storage accesses.
allocation of target computer storage and input-output devices is performed by the MCP.

.54 Object Program Performance: . . . . Burroughs states that efficiencies of 90 to 95% relative to best hand coding for both time and space are being achieved.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . . any legal B 5500 system that has at least 4 Memory Modules; see System Configuration, Section 203:031.

.612 Larger configuration advantages: . . . . magnetic tape and disc file facilitate input, output, and handling of the program library.
larger core store speeds compilation and execution of large programs.

.62 Target Computer

.621 Minimum configuration: . . . . any B 5500 system.

.622 Usable extra facilities: . . . . . . all; allocated automatically by the MCP.

.7 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Missing entries:	check (labels only)	printed message.
Unsequenced entries:	check	printed message.
Duplicate names:	check	printed message.
Improper format:	check	printed message.
Incomplete entries:	check	printed message.
Target computer overflow:	interrupt	printed message.

.8 ALTERNATIVE TRANSLATORS: . . none.

PROGRAM TRANSLATOR: FORTRAN TRANSLATOR (FORGOL 4)

.1 GENERAL

.11 Identity: . . . . FORGOL 4.

.12 Description

Programs that have been written either in B 5500 FORTRAN IV or in IBM 7090/7094 FORTRAN IV can be translated into the Extended ALGOL language by means of Burroughs' FORTRAN translator program, FORGOL 4. The Extended ALGOL program that is generated by FORGOL 4 must be passed through the Extended ALGOL Compiler (see Section 203:181) in order to produce an executable program. The minimum machine requirements necessary to use FORGOL 4 include one B 5280 Processor, three B 460 or B 461 Memory Modules (12,288 words), one B 430 Magnetic Drum (or one B 475 Disk File storage module), one Input/Output Channel, two B 400 series magnetic tape units, and one card reader and printer of any model.

FORGOL 4 is called from the B 5500 system library by the Master Control Program. Control cards are inserted in the card input stream at the beginning and end of the FORTRAN source program, and the MCP-controlled translation begins. Control cards can specify either a halt after the translation process (for the possible insertion of ALGOL language patches), or consecutive translate and compile operations. The MCP can then effect immediate execution of the object program without any operator intervention. Bulk translations can also be indicated by control cards.

Part of the output of the FORGOL 4 translator consists of a listing of the intermediate program in the ALGOL language and diagnostic error messages. Complete FORTRAN IV syntactical checking is made, and any errors and/or inconsistencies are indicated in place on the printed output. Program patches can be entered either in the intermediate ALGOL-language program deck or in the original FORTRAN IV source program in preparation for retranslation.

A variety of FORGOL 4 output options can be specified in the START control card that is placed just before the FORTRAN program deck. The translation listing can be suppressed, if desired, and the ALGOL-language intermediate program can be punched in cards or written on magnetic tape.

Burroughs estimates that FORGOL 4 translates approximately 180 source cards per minute.

.13 Originator: . . . . Burroughs Corporation.

.14 Maintainer: . . . . Burroughs Corporation.

.15 Availability: . . . . . . October, 1964.

OPERATING ENVIRONMENT: MAGNETIC DRUM MASTER CONTROL PROGRAM

.1 GENERAL

.11 Identity . . . . Magnetic Drum Master Control Program (MD MCP).

.12 Description

.121 Major Functions

Two comprehensive operating systems are now available to the users of the Burroughs B 5500 Information Processing System: the Magnetic Drum Master Control Program (described in this report section) and the Disk File Master Control Program (described in Section 203:193). Either Master Control Program (MCP) is an essential element in every B 5500 system — all compilers, problem programs, and service routines can be executed only under direct control of the MCP.

The Magnetic Drum MCP provides powerful control routines to regulate and service the execution of programs for the B 5500, but it lacks the facilities to support the use of Burroughs' Disk File System and data communications terminal units. The more-recently-developed Disk File MCP includes several refinements to the original MCP's control routines, as well as complete Disk File and data communications capabilities. Several advantages in overall system performance also accrue to users of the Disk File MCP.

The Drum MCP performs the following major functions:

- Scheduling and loading of programs.
- Control of programs being processed.
- Control of multiprogramming.
- Effective utilization of all system components.
- Automatic handling of most errors.
- Communication between operator and system.
- Logging of system operations.
- Maintenance of the program library.

.122 Hardware Requirements

The entire Drum MCP is contained on Storage Drum 1. It occupies approximately 15,000 locations and is protected by manual write lock-out switches. The remainder of Storage Drum 1 may be used to hold the ALGOL, COBOL, and FORTRAN translators. It also serves as an auxiliary store for use by the MCP for program and data storage; the drum is not explicitly usable by the programmer. The first 1,600 locations in core storage are reserved for the operating portions of the MCP; other portions are called into core storage as required. One magnetic tape unit is normally reserved for the Program Collection Tape, and scheduling changes will be facilitated if a second tape unit is available to hold the installation's Program Library Tape.

.123 Multiprogramming

Multiprogramming, or the ability to execute two or more programs simultaneously, is one of the principal features of the B 5500 system. This feature is made possible by a unique central processor design (see Section 203:051) and by the control functions of the Master Control Program. To use multiprogramming effectively with the B 5500, the only prerequisites are that the programs be written in small, logical segments and that sufficient input-output equipment be available to service the needs of multiple programs. The MCP continually analyzes the list of scheduled jobs and decides when and to what degree multiprogramming is possible. The sole criterion used in making this decision is the effective utilization of all the processing and input-output facilities of the B 5500 system.

The number of programs that can be loaded and run at the same time naturally depends upon the system configuration and the size and complexity of the programs. The size of the Program Reference Table (PRT) is fixed for each program and cannot exceed 1,023 words. Stack sizes are set by each installation according to the average size of its programs. The MCP sets the size of the stack at 512 words if the user does not specify any desired stack size. Programs are segmented by the ALGOL and COBOL translators, and no segment can exceed 1,023 words in length. Processing of the next program in sequence is initiated as soon as the MCP determines that sufficient storage space and input-output units are available.

In typical B 5500 commercial and scientific applications, the Drum MCP consumes between 2 and 10 percent of the Processor's time. Despite this "overhead" penalty, the multiprogramming facilities controlled by the Drum MCP increase the total job throughput capacity of the system by ensuring efficient utilization of the major hardware components.

.124 Job Scheduling

The scheduling function of the MCP permits initial scheduling of a series of jobs and later introduction of new jobs or changes in the processing sequence. A "header card" is required for each program to be processed or compiled; it identifies the program and states whether it is to be compiled or called from the Program Library Tape. (If the program is to be compiled, its header card is fol-

.124 Job Scheduling (Contd.)

lowed by the source deck.) The header cards permit the creation in core storage of the MCP Job Reference Table, which lists all scheduled programs. Programs are listed and processed in the order of assigned priorities; if no priorities are assigned, they are listed in the sequence in which their control cards were read. To change the processing sequence or add a new job, the operator can, at any time, initiate a keyboard interrupt and enter the necessary control information through the keyboard or card reader.

Source programs to be compiled and library programs to be run are gathered from the input job stream and/or the Program Library Tape and arranged in processing sequence on the Program Collection Tape; this tape is also used to record log information and compiled object programs. Meanwhile the MCP Job Reference Table is expanded to include, for each program: the amount of core and drum storage required, the number and type of input-output units required, and the estimated processing time.

As each program segment is readied for running, the MCP allocates the necessary storage space and input-output devices. An idle input or output unit of the appropriate type is assigned to each file, and a record is maintained in the I/O Assignment Table. The program is transferred from the Program Collection Tape to the Storage Drum. Then core storage areas of the proper size are set aside for the stack and the Program Reference Table. The Program Reference Table and the first program segments are loaded from the drum, and execution begins. All scheduled programs are handled in a similar manner as soon as the prior program has been completed. No operator intervention is required during these operations.

.125 Overlay Control

When a transfer of control is attempted to a program segment not present in core storage, an interrupt occurs. The required segment is then loaded from the drum and overlaid into an appropriately-sized core storage area. The rules for overlaying of program segments are as follows:

(1) The program segment currently in process cannot be overlaid; all others can be.

(2) Segments of the lowest-priority program currently in core storage are overlaid first.

(3) If data segments are overlaid, the MCP first copies the segment to a reserved section of the drum so that no variable data will be lost as a result of the overlay.

Overlaid program segments never need to be "rolled out" to the drum prior to being overlaid. Programs are compiled into address-independent "pure procedures" that are never modified during the programs' execution. Therefore, for every program segment in core storage, a duplicate version exists on the magnetic drum.

Average access time to data stored on the drum is 8.5 milliseconds, after which the data is transferred at 15,360 words per second.

.126 Interrupt Control

Entrance to the MCP is always initiated by an interrupt, which indicates to the Processor that one of 40 specific conditions has arisen in the system as a result of action by the program, hardware, or operator. After the contents of the A and B registers and all necessary control registers have been stored in the stack, the Processor enters the Control State, and the MCP deals with the interrupt condition. An average of about one millisecond is required to service each interrupt condition. The comprehensive hardware interrupt facilities of the B 5500 are described in the Central Processor section, Paragraph 203:051.33.

.127 Input-Output Package

The B 5500 Input-Output Package is considered an integral part of the MCP and is used with ALGOL, FORTRAN, and COBOL programs. It consists of two basic sections:

- The File Control routine occupies about 500 locations on the drum and is called into core storage as required. It writes and verifies file and reel labels, handles multi-reel files and multi-file reels, and controls restarts.

- The Read-Write routine occupies 440 locations on the drum and is called into core storage as required. It handles blocking, unblocking, and input-output errors.

By means of its Input-Output Package, the Master Control Program assumes the responsibility for locating I/O files, providing buffers and controlling their use, and performing all actual record accessing. The object program need only specify the type of input-output control desired for a specific file and the routines to put data records to use once they are located in the buffer areas.

.13 Availability: . . . . . . original Drum MCP — April, 1963.
revised Drum MCP — October, 1965.

.14 Originator: . . . . . . Burroughs Corporation.

.15 Maintainer: . . . . . . Burroughs Corporation.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries . . . . . . Program Library Tape contains all checked-out procedures and programs.
Program Collection Tape (created by MCP) contains programs in sequence of processing, as well as log information and compiled object programs.

.212 Independent programs . . . . punched cards or magnetic tape.

.213 Data: . . . . any available type of input device, as specified in program.

(Contd.)

.214 Master routines: . . . MCP is permanently stored in 15,000 locations of Storage Drum 1; operating portion is loaded into first 1,600 locations of core storage when Program Load button is pressed, and other portions are called into core storage as required.

.22 Library Subroutines: . . from Program Library Tape.

.23 Loading Sequence: . . . set up by a header card for each job to be processed, which supplies information for the MCP Job Reference Table in core storage. Programs are loaded in same sequence as their control cards were read unless priorities are used. New jobs can be introduced or priorities altered at any time by "priority change" control cards or keyboard entries.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . object programs are automatically segmented by the ALGOL and COBOL compilers.

.312 Occupation of working storage: . . . . program segments are called from drum to core storage and overlaid by other program segments or data areas as required, under control of the MCP.

.32 Input-Output Units

.321 Initial assignment: . . performed automatically by MCP.

.322 Alternation: . . . . . . handled by File Control routine, according to source language specifications.

.323 Reassignment: . . . . . message to operator permits manual reassignment when a breakdown occurs.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: . . . . each input-output operation is automatically assigned by hardware to any idle Input/Output Channel. When two processors are used, each can operate independently, except that Processor 1 services all interrupt conditions.

.42 Multiprogramming: . . number of independent programs that can run together is limited only by hardware considerations; precedence is sequence in which job header cards were read unless priorities are used.

.43 Multisequencing: . . . no facility.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Allocation impossible:	MCP check	delay processing of this program.
I/O error — Single card:	hardware checks	message; suspend program.
Tape:	hardware checks	read or rewrite.
I/O error — persistent:	hardware checks	check for programmer-specified action; if none, type message and terminate program.
Loading input error:	same as I/O error.	
Storage parity:	interrupt	type message and terminate program.
Arithmetic overflow:	interrupt	type message and terminate program.
Underflow:	interrupt	set answer to zero and continue program.
Invalid operation:	ignored in Character Mode; hardware check in Word Mode	type message and dump program.
Stack overflow:	Interrupt	type message and terminate program.
Invalid address:	Interrupt	type message and terminate program
Reference to forbidden area:	invalid index interrupt	type message and terminate program.

.45 Restarts: . . . . handled by the Breakout and Restart routines, integral parts of the MCP.

.451 Establishing restart points: . . . . specified by COBOL's RERUN clause and ALGOL's BREAK statement, at end

.451 Establishing restart points (Contd.) of every reel or every N records. Core storage is dumped and a record is made of tape file positions on either the output or on a separate rerun tape.

.452 Restarting process: . keyboard entry by operator initiates automatic restart when all tapes files are on proper units.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . specified by MONITOR declarations in ALGOL, COBOL, or FORTRAN source programs.

.512 Snapshots: . . . . specified by DUMP declarations in source programs.

.52 Post Mortem: . . . . . typed message identifies source-language statement in which error occurred.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . type message on Supervisory Printer.

.612 Action required by operator: . . . . typed message.

.613 Reporting progress of run: . . . . typed message.

.62 Operator's Decisions: . . . . keyboard entries.

.63 Operator's Signals

.631 Inquiry: keyboard entries.

.632 Change of normal progress: . . . . "priority change" entries and program termination via keyboard or control cards.

.7 LOGGING

.71 Operator Signals: . . . typed record of keyboard entries.

.72 Operator Decisions: . typed record of keyboard entries.

.73 Run Progress: . . . . . typed messages.

.74 Errors: . . . . typed messages.

.75 Running Times: . . . . typed messages.

.76 Multiprogramming Status: . . . . typed message in response to keyboard inquiry.

Note: The Operations Log, produced on a line printer or card punch upon keyboard request, lists, for each program run since the last log printout: program ID, Processor time, and input-output time and number of errors for each file. The same information is printed for each program immediately upon its termination.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . any legal B 5500 system that has at least one B 430 Magnetic Drum connected (see System Configuration, Section 203:031). Disc-oriented systems can use the Disc File MCP, described in the following report section, 203:192.

.812 Usable extra facilities: . . . . all; control cards or keyboard entries are used to inform the MCP whenever there is a change in the number or type of available peripheral units.

.813 Reserved equipment: . . . . one magnetic tape unit (for Program Collection Tape), 1,600 core storage locations, and Storage Drum 1 (for MCP, compilers, and system utility routines).

.82 System Overhead

.821 Loading time: . . . . . drum-to-core transfers: 8.5 msec average access time, plus 0.065 msec per word transferred.

.822 Reloading frequency: . . . . operating portion always occupies 1,600 core storage locations; other portions are automatically called from drum when needed, then overwritten.

.83 Program Space Available: . . . . . . all but 1,600 positions of core storage, and all of Magnetic Drum 2 (when used).

.84 Program Loading Time: . . . . depends upon speed of the input device.

.85 Program Performance: . . . . MCP overhead is estimated by the manufacturer to be 2 to 10% of total processing time; it will vary considerably with hardware availability and with the number and complexity of programs being run at the same time. An average of about 1 msec is required to service each interrupt condition.

OPERATING ENVIRONMENT: DISK FILE MASTER CONTROL PROGRAM

.1 GENERAL

.11 Identity: . . . . Disk File Master Control Program (DF MCP).

.12 Description

.121 Major Functions

In addition to the Magnetic Drum Master Control Program described in the previous report section (203:191), Burroughs offers another completely integrated operating system for use with the B 5500 system. The Disk File Master Control Program, available since December, 1964, provides B 5500 users with all of the control routines, compilers, and service facilities offered with the Drum MCP; improvements in the design of the total Disk File MCP system result in generally better performances from these programs and the problem programs executed under their supervision. The Disk File MCP also includes provisions to control Disk File and data communications input-output operations.

Like the Drum MCP, the Disk File MCP performs the following major functions:

- Scheduling and loading of programs.
- Control of programs being processed.
- Control of multiprogramming.
- Effective utilization of all system components.
- Automatic handling of most errors.
- Communication between operator and system.
- Logging of system operations.
- Maintenance of the program libraries.

.122 Hardware Requirements

The first 15,000 240-character Disk File segments are reserved as "System Disk," containing the full Disk File MCP and its associated tables, the Disk Directory of all files stored on the Disk, the list of available storage addresses, and the area permanently assigned for use as system overlay storage. The remaining 25,000 segments of the first 9.6-million-character Disk File storage module are called "User Disk," housing the ALGOL and COBOL compilers, the FORTRAN translator, the specialized ESPOL compiler (see Paragraph .128), all MCP utility routines (including Printer Backup and System Logging routines), and as many of the user's data files and library programs as the available disc storage space can hold.

The first 1,600 words of core storage are reserved for the permanent supervisory portion of the Disk File MCP. All other portions of the MCP are called into core storage only as required. Once the Disk File MCP and its associated programs have been loaded from the supplied System Tape, the use of magnetic tape units is not required, although the availability of at least two tape units is advantageous to the system. The Magnetic Drum MCP's Program Collection Tape, used in the scheduling operation to gather today's problem programs, is not required when using the Disk File MCP; the same function can be performed entirely on the Disk File without physically moving the scheduled programs from their on-line libraries.

Despite the fact that operation of the Disk File MCP does not require the use of the B 430 Magnetic Drum Storage Unit, Burroughs recommends its inclusion in B 5500 Disk File MCP system configurations in order to optimize the performance of the MCP and its controlled programs. The drum's average access time of 8.3 milliseconds, significantly faster than the Disk File's 20-millisecond average access time, makes the drum more efficient in the storage and control of frequently-accessed program or data segments. When the B 5500 system configuration includes the maximum complement of internal storage devices, the hierarchy of storage breaks down as follows: 262,144 characters (32,768 B 5500 words) of 4-microsecond core storage, 262,144 characters of 8.5-millisecond drum storage, and 960,000,000 characters of 20-millisecond disc storage.

.123 Multiprogramming

Multiprogramming, or the ability to execute two or more programs simultaneously, is one of the principal features of the B 5500 system. This feature is made possible by a unique central processor design (see Section 203:051) and by the control functions of the Disk File Master Control Program. To use multiprogramming effectively with the B 5500, the only prerequisites are that the programs be written in small, logical segments and that sufficient input-output equipment be available to service the needs of multiple programs. The MCP continually analyzes the list of scheduled jobs and decides when and to what degree multiprogramming is possible. The sole criterion used in making this decision is the effective utilization of all the processing and input-output facilities of the B 5500 system.

The number of programs that can be loaded and run at the same time naturally depends upon the system configuration and the size and complexity of the programs. The size of the Program Reference Table (PRT) is fixed for each program and

.123 Multiprogramming (Contd.)

cannot exceed 1,023 words. Stack sizes can be set by each installation, according to the average size of its programs. If the stack size is not specified, the MCP automatically sets it at 512 words. Programs are segmented by ALGOL and COBOL translators, and no segment can exceed 1,023 words in length. Processing of the next program in sequence is initiated as soon as the MCP determines that sufficient storage space and input-output units are available.

In typical B 5500 commercial and scientific applications, the Disk File MCP consumes between 2 and 10 percent of the Processor's time. Despite this "overhead" penalty, the multiprogramming facilities controlled by the Disk File MCP increase the total job throughput capacity of the system by ensuring efficient utilization of the major hardware components.

.124 Job Scheduling

The Disk File MCP constructs an MCP Job Reference Table or "schedule sheet" at the beginning of each processing period; this consists of a list of all the jobs to be performed and any necessary program parameter information. The operator enters this information into the system by means of control cards and program parameter cards, constructed in free-field format. Unlike the control cards used with the Drum MCP, the Disk File MCP's control cards specify their purpose by means of word descriptions such as COMPILE, EXECUTE, LOAD, DUMP, REMOVE, etc. The Disk File MCP also provides a procedure that enables card deck information — including control cards, program source decks, and other input data — to be stored in the Disk File and to be subsequently accessed from the "simulated card reader." Operational errors should be diminished by taking advantage of this feature.

Included in the control information for each program can be a priority number, used to guide the MCP in its control of sequential program execution. However, if at any time during the processing sequence the operator wishes to change the priority of a scheduled program or to add a new program to the schedule, he can do so by initiating a keyboard interrupt and entering the required information through the B 5500's console keyboard or card reader.

Before execution of the scheduled programs begins, the Disk File Master Control Program inserts into its Job Reference Table for each program: the address of the program in disc storage; the amount of core, drum, and disc storage required for execution; the number and type of input-output units required; and the estimated processing time.

In the initialization of each program segment, the Disk File MCP allocates the necessary storage space and input-output devices. An idle input or output unit of the appropriate type is assigned to each file, and a record is maintained in the I/O Assignment Table. Then core storage areas of the proper size are set aside for the stack and the Program Reference Table.

The Program Reference Table and the first program segment are loaded from the Disk File, and execution begins. All scheduled programs are handled in a similar manner as soon as the prior program has been completed. No operator intervention is required during these operations.

.125 Overlay Control

When a transfer of control is attempted to a program segment not present in core storage, an interrupt occurs. The required segment is then loaded from the Disk File and overlaid into an appropriately-sized core storage area. The rules for overlaying of program segments are as follows:

(1) The program segment currently in process cannot be overlaid; all others can be.

(2) If data segments are overlaid, the MCP first copies the segments to a reserved section of the Disk File so that no variable data will be lost as a result of the overlay.

Overlaid program segments never need to be "rolled out" to disc storage prior to being overlaid. Programs are compiled into address-independent "pure procedures" that are never modified during the program's execution. Therefore, for every program segment in core storage, a duplicate version exists on the Disk File.

.126 Interrupt Control

Entrance to the MCP is always initiated by an interrupt, which indicates to the Processor that one of 40 specific conditions has arisen in the system as a result of action by the program, hardware, or operator. After the contents of the A and B registers and all necessary control registers have been stored in the stack, the Processor enters the Control State and the MCP deals with the interrupt condition. An average of about one millisecond is required to service each interrupt condition. The comprehensive hardware interrupt facilities of the B 5500 are described in the Central Processor section, Paragraph 203:051.33.

.127 Input-Output Package

The B 5500 Input-Output Package is considered an integral part of the MCP and is used with ALGOL, FORTRAN, and COBOL programs. It consists of two basic sections:

- The File Control routine occupies about 500 locations on the Disk File and is called into core storage as required. It writes and verifies file and reel labels, handles multi-reel files and multi-file reels, and controls restarts.

- The Read-Write routine occupies about 450 locations on the Disk File and is called into core storage as required. It handles blocking, unblocking, and input-output errors.

By means of its Input-Output Package, the Master Control Program assumes the responsibility for locating the I/O files, providing buffers and controlling their use, and performing all actual record

(Contd.)

.127 Input-Output Package (Contd.)

accessing. The object program need only specify the type of input-output control desired for a specific file, and the routines to put data records to use once they are located in the buffer areas.

The Input-Output Package of the Disk File MCP permits use of the Disk File as an I/O unit by the problem programs and compilers. The record access methods can be specified as sequential, random, or update. Reading, writing, checking, blocking, and unblocking are all performed by the MCP. The control of multiple input-output buffers is also provided automatically by the Disk File MCP.

Four different types of data communications terminal units can be connected to B 5500 systems (see Section 203:101), and the Disk File MCP provides the necessary routines to control their use. The operations that can be controlled include standard inquiry-response transmission, batch data transmission, message switching, and remote operation of the central processor.

.128 Drum MCP versus Disk File MCP

The Disk File MCP can provide significant throughput improvements over the Drum MCP (described in Section 203:191). Consider the following items:

- Burroughs estimates that the time to execute certain programs can be reduced by as much as 30% when the Disk MCP controls the execution and when Disk File storage is available for use by the problem program.

- Efficient multiprogramming of several program segments is facilitated by the MCP's fast access to the program library on the Disk File as soon as it is discovered that another scheduled segment can be run at a given time. There is no need to search through a Program Collection Tape to locate the desired program segment.

- Routines are provided with the Disk File MCP to create and maintain source and object programs on disc storage. The object programs are stored in a form ready for execution and can be called into core storage immediately as requested.

- Job control cards and program parameter cards can be written on disc storage as a "schedule deck," eliminating the need for the operator to load these cards each day through the card reader.

- The Disk File MCP is written and supplied in a language called ESPOL — Executive System Problem Oriented Language. ESPOL is a modified version of Extended ALGOL that is designed to facilitate the solution of executive system problems. The user familiar with the ALGOL language can readily modify the source-language Disk File MCP. An ESPOL compiler is provided with every B 5500 Disk File MCP system.

.13 Availability: . . . . December, 1964. (February, 1965, with data communications facilities.)

.14 Originator: . . . . Burroughs Corporation.

.15 Maintainer: . . . . Burroughs Corporation.

.2 PROGRAM LOADING

.21 Source of Program

.211 Programs from on-line libraries: . . . source and object programs are stored on magnetic tape or Disk File.

.212 Independent programs: . . . . punched cards or magnetic tape.

.213 Data: . . . . any available input device, as specified in the program.

.214 Master routines: . . . . the MCP is permanently stored in the first 1,000 segments of Disk File Storage Module 1; the operating portion of the MCP is loaded into the first 1,600 words of core storage when the Program Load button is pushed; the other portions of the MCP are called into core storage as required.

.22 Library Subroutines: . . . . . . stored in the object program library on magnetic tape or Disk File.

.23 Loading Sequence: . . . determined either by the sequence of the control cards in the input job stream, or by priorities specified in the control cards. New jobs can be introduced or priorities altered at any time by "priority change" control cards or keyboard entries.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . object programs are automatically segmented by the ALGOL and COBOL compilers.

.312 Occupation of working storage: . . . program segments are called from disc to core storage and overlaid by other program segments or data areas as required, under control of the MCP.

.32 Input-Output Units

.321 Initial assignment: . . . performed automatically by MCP.

.322 Alternation: . . . . handled by File Control routine, according to source language specifications.

.323 Reassignment: . . . . . message to operator permits manual reassignment when a breakdown occurs.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: . . . . each input-output operation is automatically assigned by hardware to any idle Input/Output Channel. When two processors are used, each can operate independently, except that Processor 1 services all interrupt conditions.

.42 Multiprogramming: . . . number of independent programs that can be run together is limited only by hardware considerations; precedence is sequence in which job header cards were read unless priorities are used.

.43 Multisequencing: . . . . no facilities.

.44 Errors, Checks, and Action: . . . . . . same as for Drum MCP; see Paragraph 203:191.44.

.45 Restarts: . . . . same as for Drum MCP; see Paragraph 203:191.45.

.5 PROGRAM DIAGNOSTICS: . . . . same as for Drum MCP; see Paragraph 203:191.5.

.6 OPERATOR CONTROL: . . . . same as for Drum MCP; see Paragraph 203:191.6.

.7 LOGGING: . . . . same as for Drum MCP; see Paragraph 203:191.7.

Note: The operations Log, produced on the line printer upon keyboard request, lists, for each program run since the last log printout: program ID, control card information, today's date, time of day for starting and stopping, Processor time, input-output time, number of errors for each file, the name of each I/O file, its unit number, and the length of time the file was open.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . any legal B 5500 system that has at least one B 475 Disk File Storage Module connected (see System Configuration, Section 203:031).

.812 Usable extra facilities: . . . . all; control cards or keyboard entries are used to inform the MCP whenever there is a change in the number or type of available peripheral units.

.813 Reserved equipment: . . . . 1,600 words of core storage and 1,000 segments of Disk File Storage Module 1.

.82 System Overhead

.821 Loading time: . . . . . . disc-to-core transfers: 20 msec average access time plus 0.08 msec per word.
drum-to-core transfers: 8.3 msec average access time plus 0.065 msec per word.

.822 Reloading frequency: . . . . operating portion always occupies 1,600 core storage locations; other portions are automatically called from disc or drum storage when needed, then overwritten.

.83 Program Space Available: . . . . all but 1,600 positions of core storage.

.84 Program Loading Time: . . . . depends upon speed of the input device.

.85 Program Performance: . . . . MCP overhead is estimated by the manufacturer to be 2 to 10% of total processing time; it will vary considerably with hardware availability and with the number and complexity of programs being run at the same time. An average of about 1 msec is required to service each interrupt condition.

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (203:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application, one of the most typical of commercial data processing jobs, is fully described in Section 4:200.1 of the Users' Guide.

Because the B 5500 can process several independent programs at the same time through multiprogramming, the amount of central processor time required by each program is highly significant. The difference between the total elapsed time for a particular run and the amount of central processor time required for that run represents processor time that is potentially available to other programs. Whether or not this processor time can be efficiently utilized depends upon the system configuration and the over-all problem mix.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master-file records is shown by solid lines. For Configuration VIIB, where all four input-output files are on magnetic tape, total times for both unblocked and blocked records in the detail and report files are shown by means of solid and dashed lines, respectively. Central processor time is essentially the same for all configurations, and is shown by the broken line marked "CP" on each graph. No addition has been made to the processor time to cover the requirements of the Master Control Program (MCP). As indicated in Paragraph 203:191.85, the manufacturer expects the MCP to require, on the average, 2 to 10 percent of the total processor time.

Worksheet Data Table I (page 203:201.002) shows that the printer is the controlling factor on total time required over most of the detail activity range for integrated Configurations III, V, and VIIA. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a small fraction of the total processing time. In these cases, multiprogramming of other jobs that have limited input-output requirements, such as scientific tasks, can be effectively accomplished. In other cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, the processing run with all files on magnetic tape, and a tape-to-printer transcription of the report file. The curves for paired Configuration VIIB show the time required for the all-tape processing run in this case. The card-to-tape and tape-to-printer transcriptions will run at card reader and printer-limited speeds, and their demands on the processor will be small.

The file processing problems have been coded and timed, insofar as current knowledge permits, in the style of the object programs produced by the B 5500 COBOL Compiler. Just as in the COBOL Compiler, we have used the binary Word Mode for all operations except the EXAMINE verb and most MOVE options, where the Character Mode is used. To minimize unpacking and radix conversions, all items whose USAGE is described as COMPUTATIONAL in a COBOL source program are stored in binary form, one item per B 5500 word, by the COBOL compiler. Items whose USAGE is DISPLAY are stored in a packed alphameric format, eight characters per word. It was assumed that most COBOL programs would routinely describe as COMPUTATIONAL all of the items in the master file upon which arithmetic will be performed; this assumption resulted in a master-file record length of 18 words, or 144 characters, and a significant increase in magnetic tape time over the time for packed records.

SORTING (230:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A according to the method explained in the Users' Guide, Paragraph 4:200.213. Times for both two-way and three-way merges are shown in Graph 203:201.214. The sorting times shown are for the specified 80-character record; the likely expansion to a larger record size through the assignment of each COMPUTATIONAL item to a full word by the COBOL Compiler should be kept in mind when considering sorting times.

Sorting (203:201.2) (Contd.)

The B 5500 Tape or Disk File Sort Generator is an integral part of the COBOL Compiler and is described in Paragraph 203:151.13. No timing formula is available, and the timing tables published by the manufacturer for 80-character records apply only to a file of 100,000 records. The times for smaller file sizes in Graph 203:201.224 are estimates. Sorting via the B 5500 Sort Generator is faster than the times produced by the standard estimate. This comparatively higher speed is due to efficient use of the large internal store and to the polyphase merge technique used by the manufacturer's generated routines.

MATRIX INVERSION (203:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplication ($c = c + a_ib_j$) in single-precision floating-point (see Paragraph 203:051.422). The processor time required for a matrix inversion can be spread over a much longer total elapsed time when the inversion is run simultaneously with other programs that utilize the available input-output equipment.

WORKSHEET DATA TABLE 1

	ITEM		CONFIGURATION: III		V		VIIA		VII B (blocked)		VII B (unblocked)		REFERENCE
1 Input-Output Times	Char/block	(File 1)	1,008		1,008		1,008		1,008		1,008		4:200.112
	Records/block	K (File 1)	7		7		7		7		7		
	msec/block	File 1 = File 2	50.5		50.5		23.8		23.8		23.8		
		File 3	75.		75.		75.		20.5**		9.9		
		File 4	111.		111.		92.5		26.8		10.5		
	msec/switch	File 1 = File 2											
		File 3											
		File 4											
	msec penalty*	File 1 = File 2	0.76/19.1		0.76/19.1		0.76/19.1		0.76/19.1		0.76/19.1		
		File 3	0.06/72		0.06/72		0.06/72		0.60/16.0		0.06/5.2		
		File 4	0.09/3		0.09/3		0.09/3		0.90/22.0		0.09/5.8		
2 Central Processor Times	msec/block	a_1	0.16		0.16		0.16		0.16		0.16		4:200.1132
	msec/record	a_2	0.54		0.54		0.54		0.54		0.54		
	msec/detail	b_6	0.29		0.29		0.34		0.34		0.29		
	msec/work	$b_5 + b_9$	1.06		1.06		1.06		1.06		1.06		
	msec/report	$b_7 + b_8$	2.29		2.29		2.29		2.34		2.29		
3 Standard Problem A F = 1.0	msec/block for C.P. and dominant column.	a_1	C.P.	Printer	C.P.	Printer	C.P.	Printer	C.P.	I/O Ch.	C.P.	Tape	4:200.114
		a_1	0.16		0.16		0.16		0.16		0.16		
		a_2K	2.78		3.78		3.78		3.78		3.78		
		a_3K	25.53		25.53		25.53		25.53		25.53		
		File 1: Master In	0.51		0.51		0.51		0.51		0.51		
		File 2: Master Out	0.51		0.51		0.51		0.51	19.1	0.51		
		File 3: Details	0.28		0.28		0.28		0.28		0.51		
		File 4: Reports	0.42	777.0	0.42	777.0	0.42	647.5	0.42	15.4	0.42	73.5	
		Total	31.19	777.0	31.19	777.0	31.19	647.5	31.19	34.5	31.19	73.5	
4 Standard Problem A Space	Unit of measure	(words)											4:200.1151
		Std. routines	200		200		200		200		200		
		Fixed	1,600		1,600		1,600		1,600		1,600		
		3(Blocks 1 to 23)	72		72		72		72		72		
		6(Blocks 24 to 48)	450		450		450		480		450		
		Files	554		554		554		1,004		554		
		Working	80		80		80		80		80		
		Total	2,956		2,956		2,956		3,436		2,956		
5 Standard Mathematical Problem A	Fixed/Floating point		Floating point		Floating point		Floating point		Floating point				4:200.413
	Unit name	input	B 124 Card Reader		B124 Card Reader		B 124 Card Reader		B422 Mag. Tape				
		output	B321 Line Printer		B321 Card Reader		B328 Line Printer		B422 Mag. Tape				
	Size of record	input	80 characters		80 characters		80 characters		80 characters				
		output	120 characters		120 characters		120 characters		100 characters				
	msec/block	input T_1	75		75		75		9.9				
		output T_2	86		86		57		10.2				
	msec penalty	input T_3	0.06		0.06		0.06		0.06				
		output T_4	0.09		0.09		0.09		0.08				
	msec/record	T_5	1.66		1.66		1.66		1.66				
	msec/5 loops	T_6	3.24		3.24		3.24		3.24				
	msec/report	T_7	2.55		2.55		2.55		2.55				

* Demand on Processor and I/O Channel are shown to left and right of slash, respectively.
** Ten records per block in Files 3 and 4.

(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

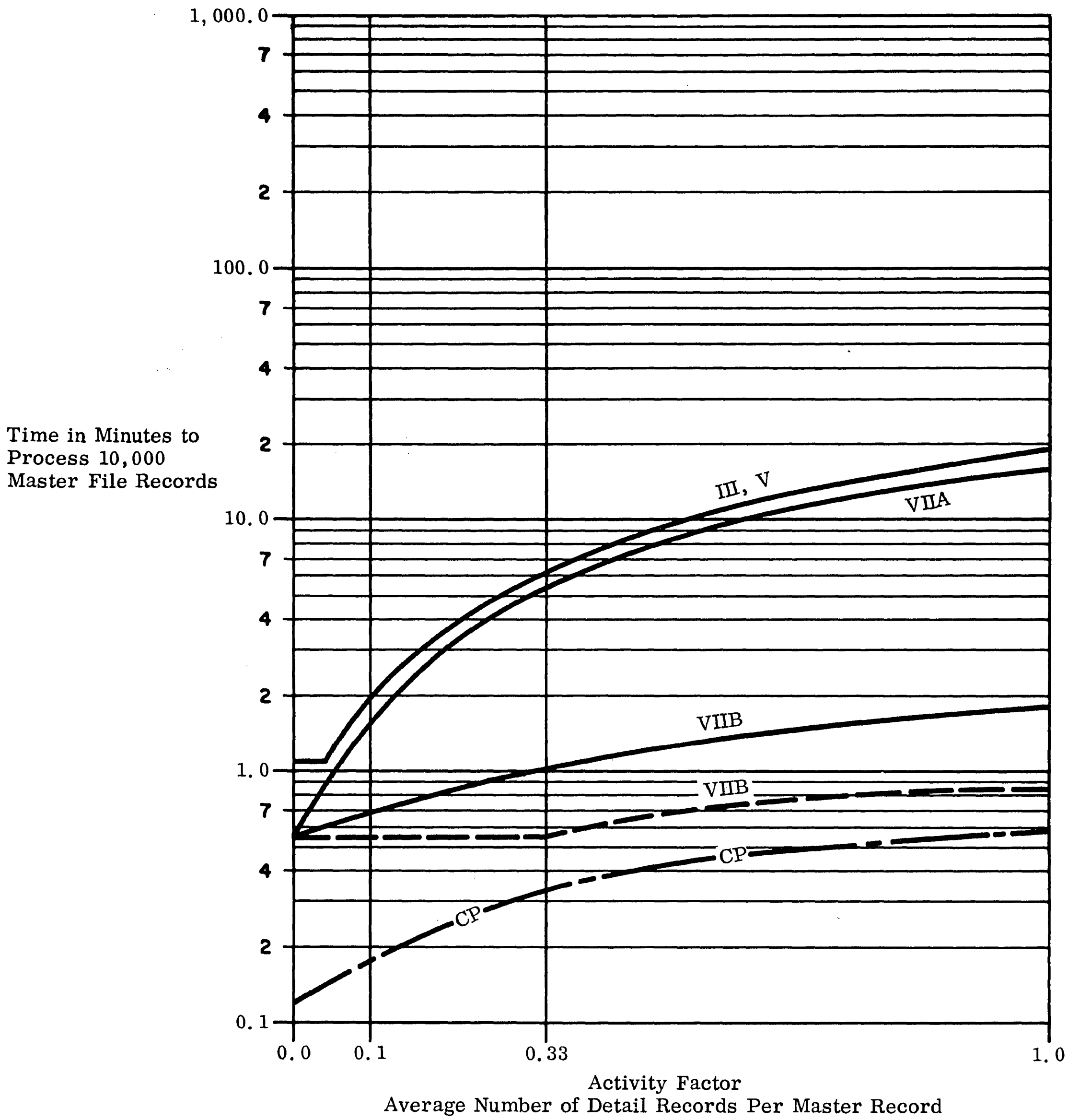
.111 Record sizes —
Master file: . . . . . . 108 data characters, arranged in 18 B 5500 words.
Detail file: . . . . 1 card.
Report file:. . . . . . . 1 line.

.112 Computation:. . . . . . . standard.

.113 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . see graph below.

.115 Storage space required —
Configuration III: . . . 2,956 words.
Configuration V: . . . 2,956 words.
Configuration VIIA: 2,956 words.
Configuration VIIB —
Unblocked files 3 & 4: . . . . 2,956 words.
Blocked files 3 & 4: . . . . 3,436 words.



(Roman numerals denote standard System Configurations.)

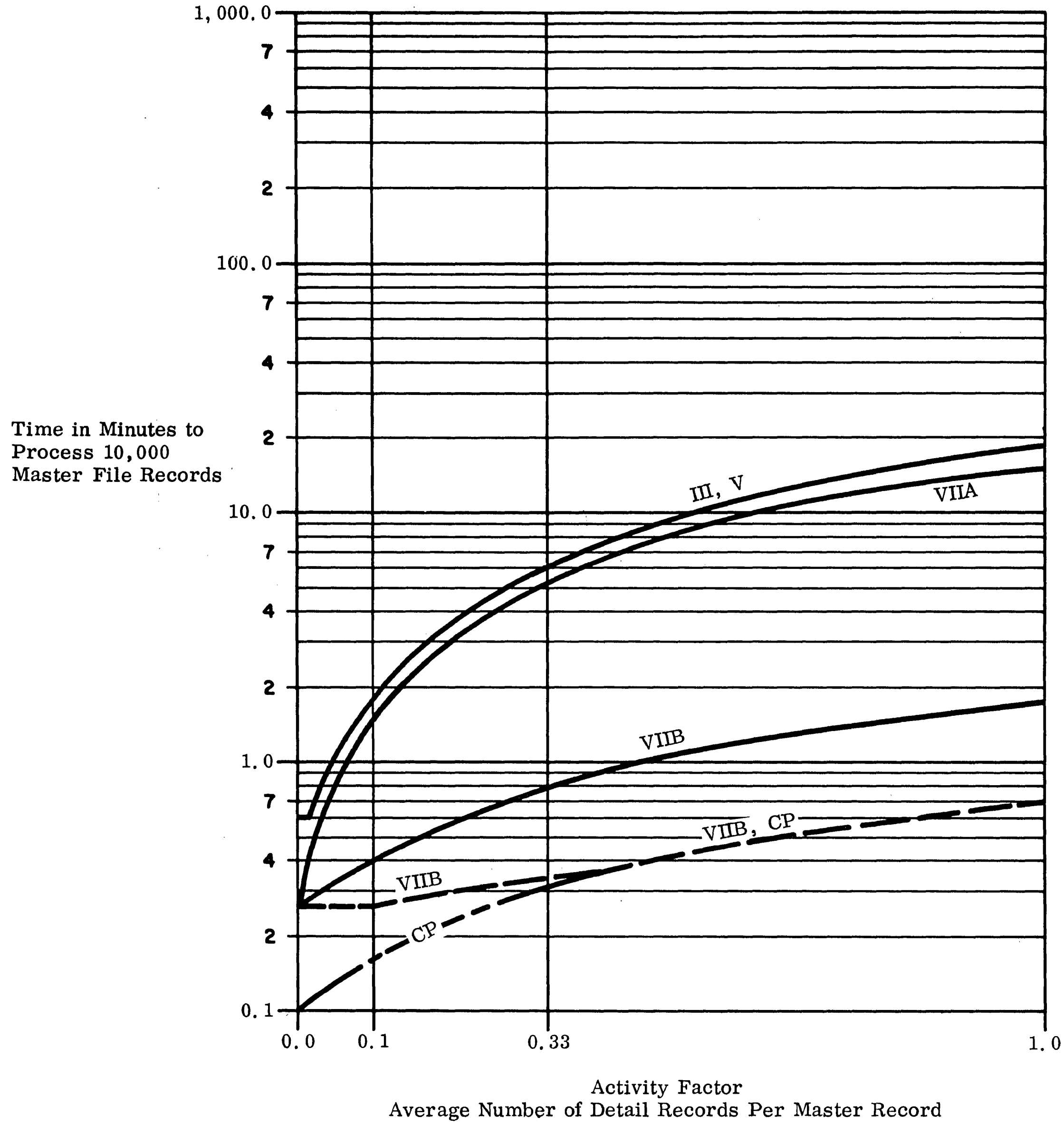
LEGEND

Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
CP Central Processor time (all configurations)

.12 Standard File Problem B

.121 Record sizes —
Master file: . . . . . . 54 data characters, arranged in 9 B 5500 words.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.122 Computation: . . . . standard.
.123 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

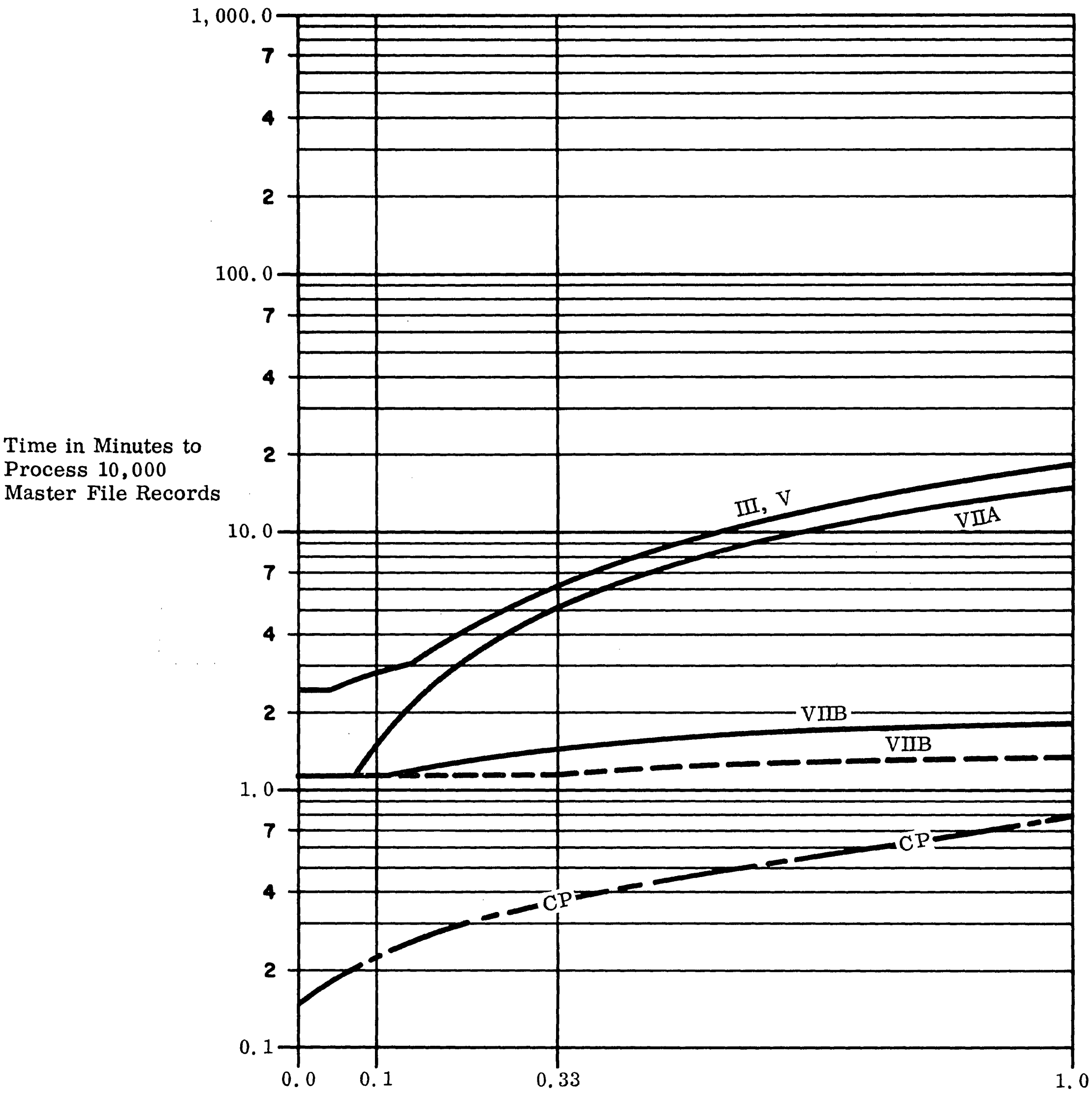
LEGEND
Elapsed time; unblocked Files 3 & 4
Elapsed time; blocked Files 3 & 4
Central Processor time (all configurations)

(Contd.)

.13 Standard File Problem C

.131 Record sizes —
Master file: . . . . . . 216 data characters, arranged in 36 B 5500 words.
Detail file: . . . . 1 card.
Report file:. . . . . . . 1 line.

.132 Computation:. . . . . . . standard.
.133 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote standard System Configurations.)

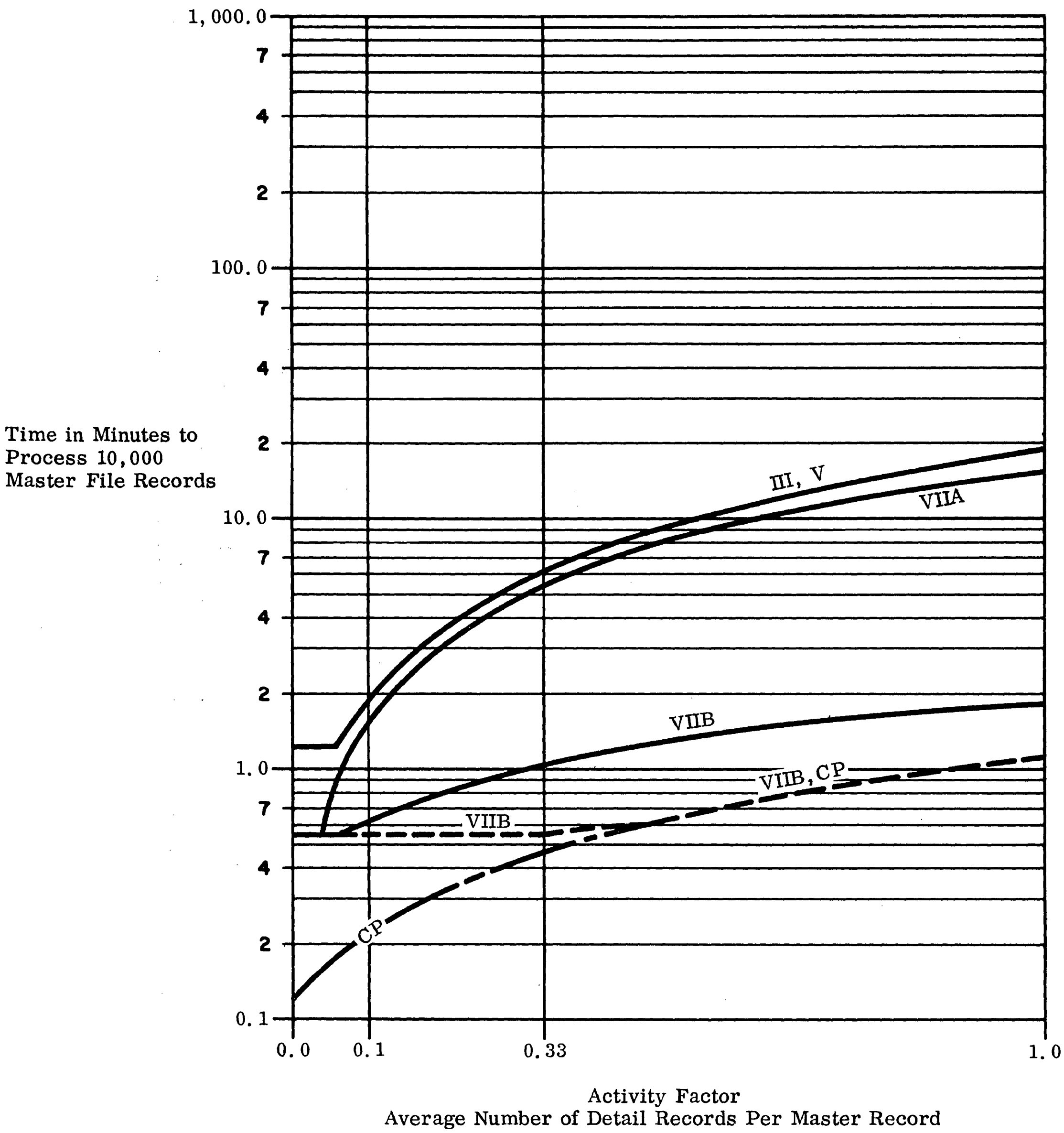
LEGEND

———————	Elapsed time; unblocked Files 3 & 4
— — — — — —	Elapsed time; blocked Files 3 & 4
——CP——-——	Central Processor time (all configurations)

.14 Standard File Problem D

.141 Record sizes
Master file: . . . . . . 108 data characters, arranged in 18 B 5500 words.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.142 Computation: . . . . trebled.
.143 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.144 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

LEGEND
——— Elapsed time; unblocked Files 3 & 4
— — — Elapsed time; blocked Files 3 & 4
——CP—— Central Processor time (all configurations)

(Contd.)

.2 SORTING

.21 Standard Problem Estimates

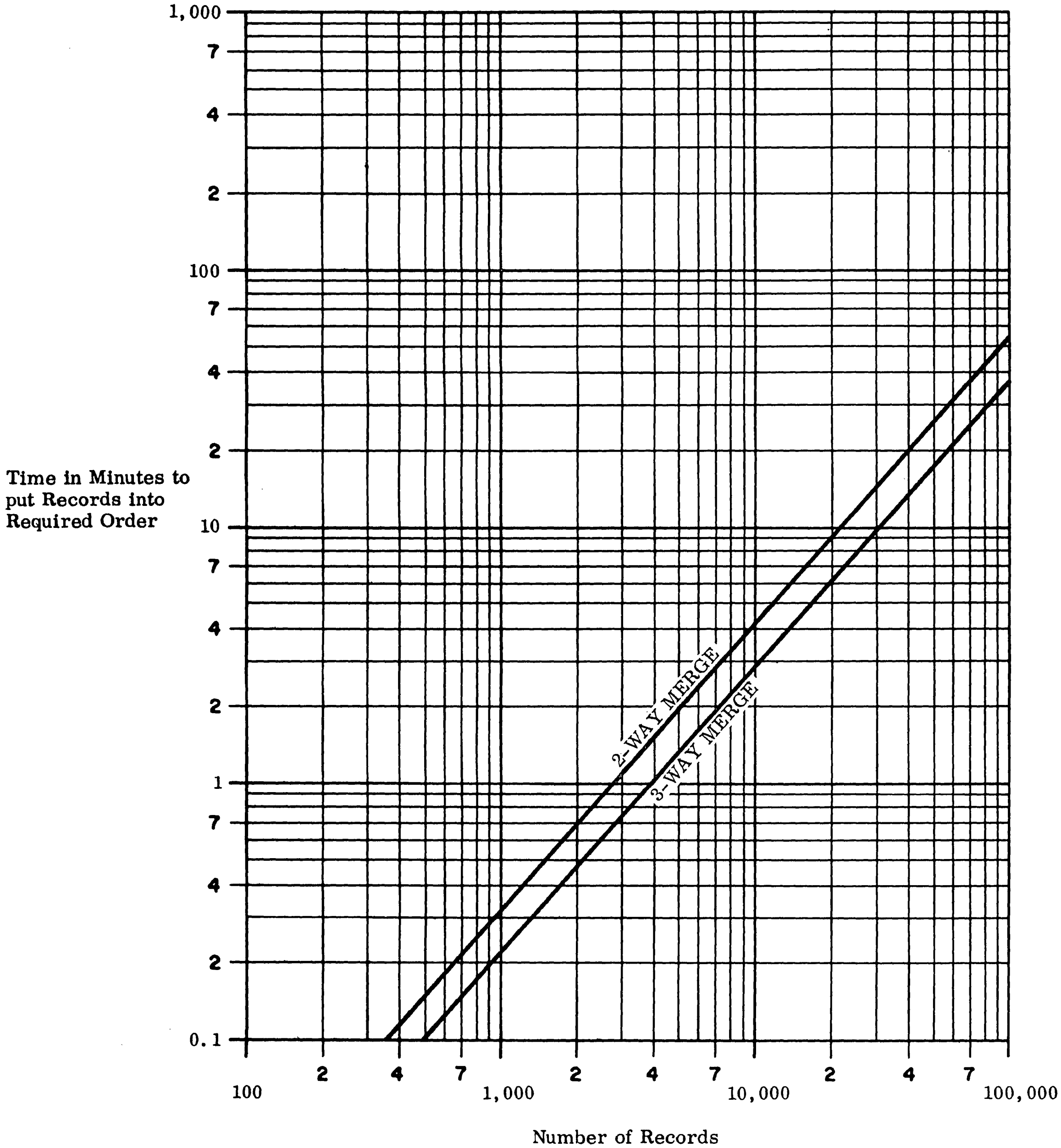
.211 Record size: . . . . 80 characters.

.212 Key size: . . . . 8 characters.

.213 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

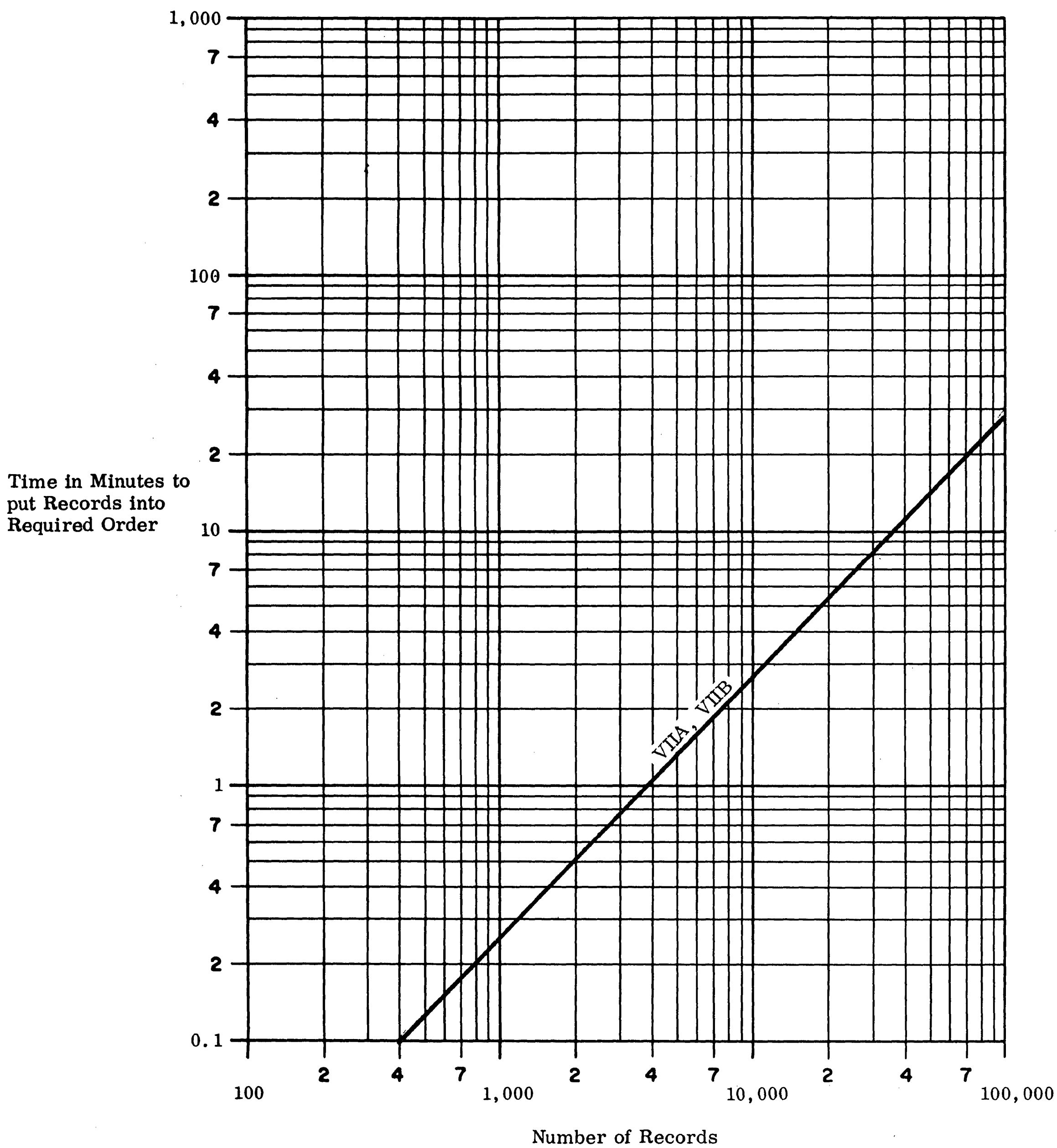
.214 Graph: . . . . see graph below.

CONFIGURATIONS VIIA AND VIIB



.22 B 5500 Tape Sort Generator Times

.221 Record size: . . . . 80 characters.
.222 Key size: . . . . 8 characters.
.223 Timing basis: . . . . . . Sorting on the B 5500, Burroughs publication 1021334.
.224 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

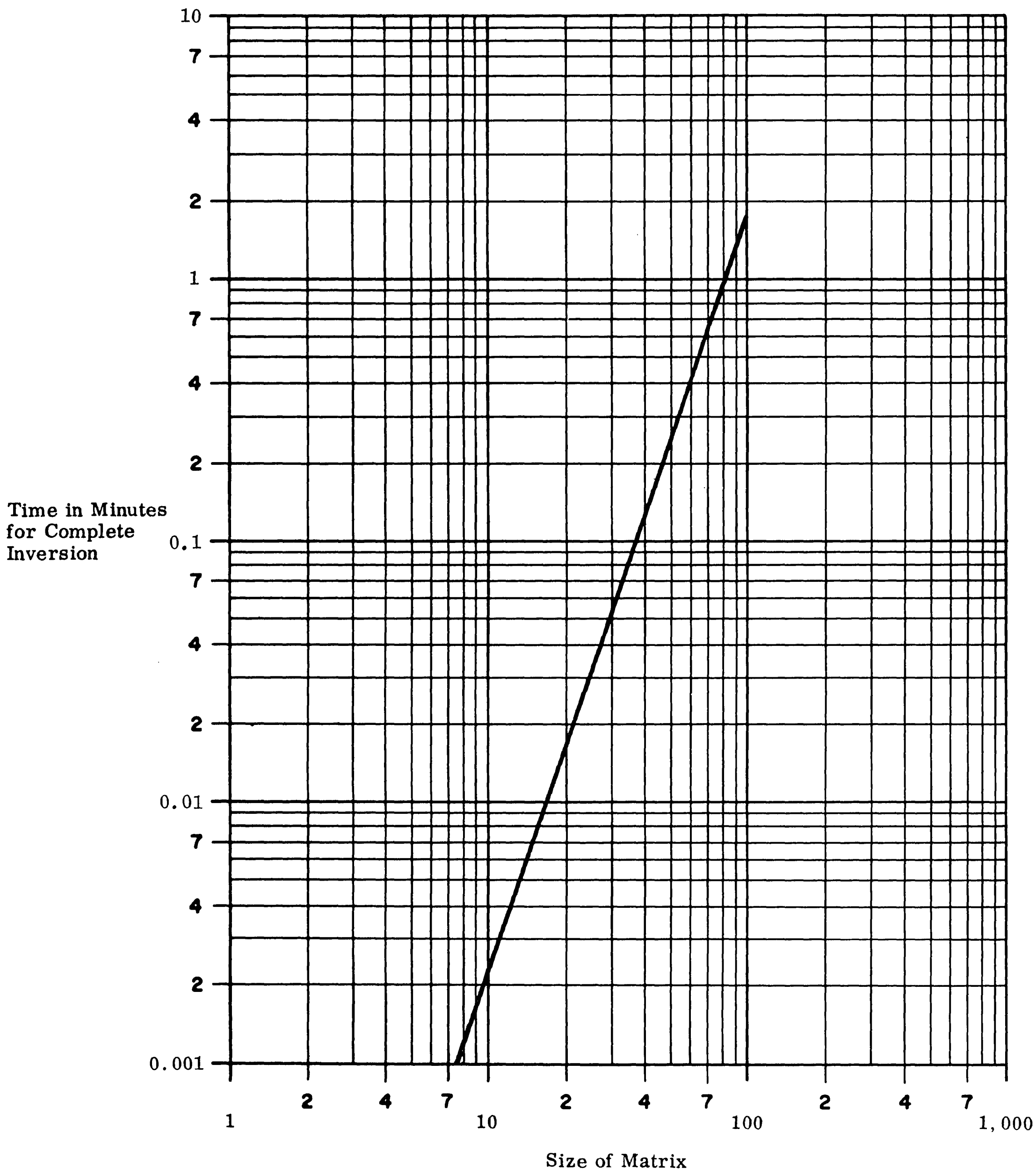
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . see graph below, which applies to all configurations.

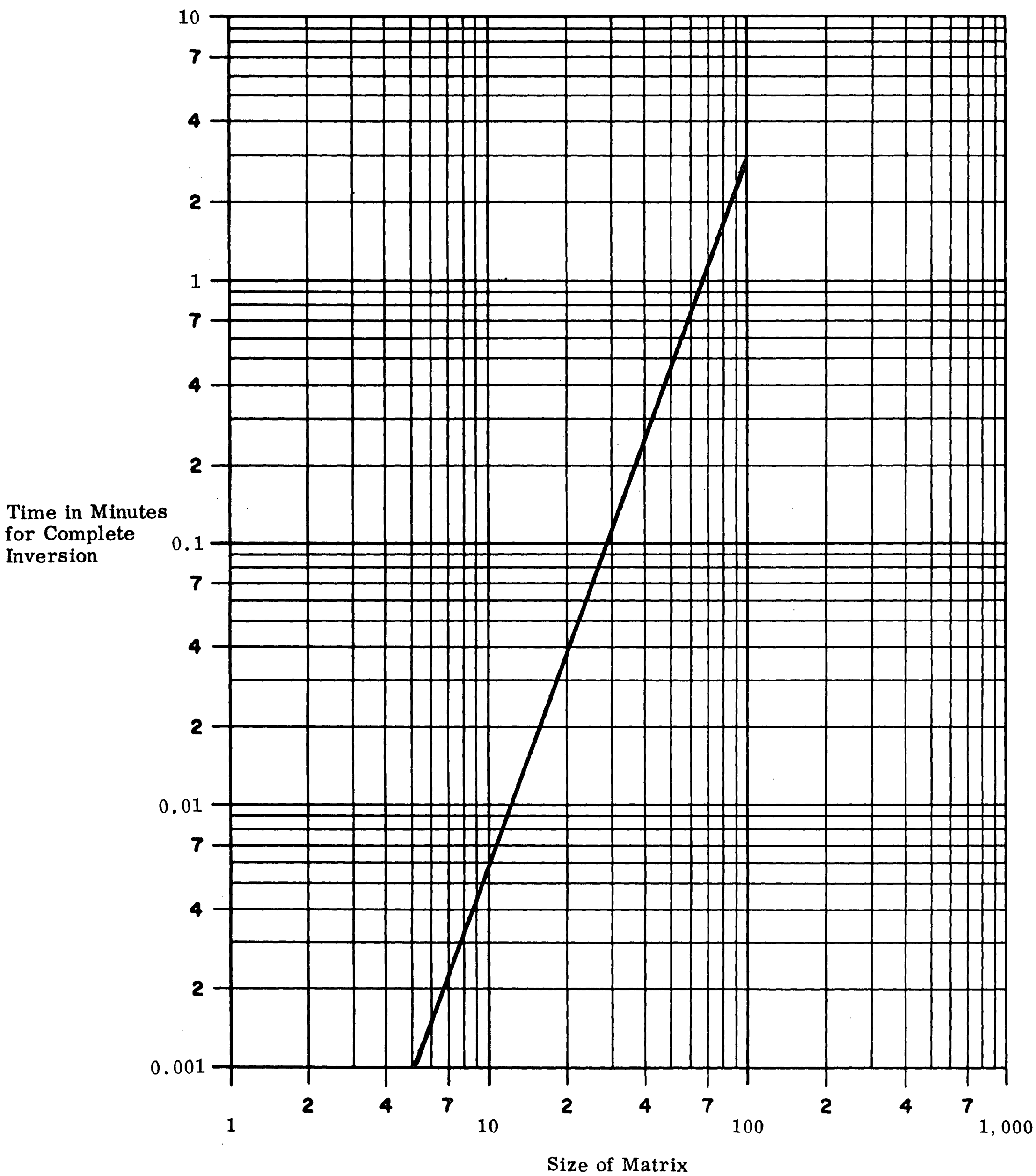


.32 <u>Manufacturer's Routine Times</u>

.321 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.322 Timing basis: . . . . . . estimates by manufacturer for Scientific Library Procedure for inversion of non-symmetric matrices.

.323 Graph: . . . . see graph below, which applies to all configurations.



(Contd.)

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.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates

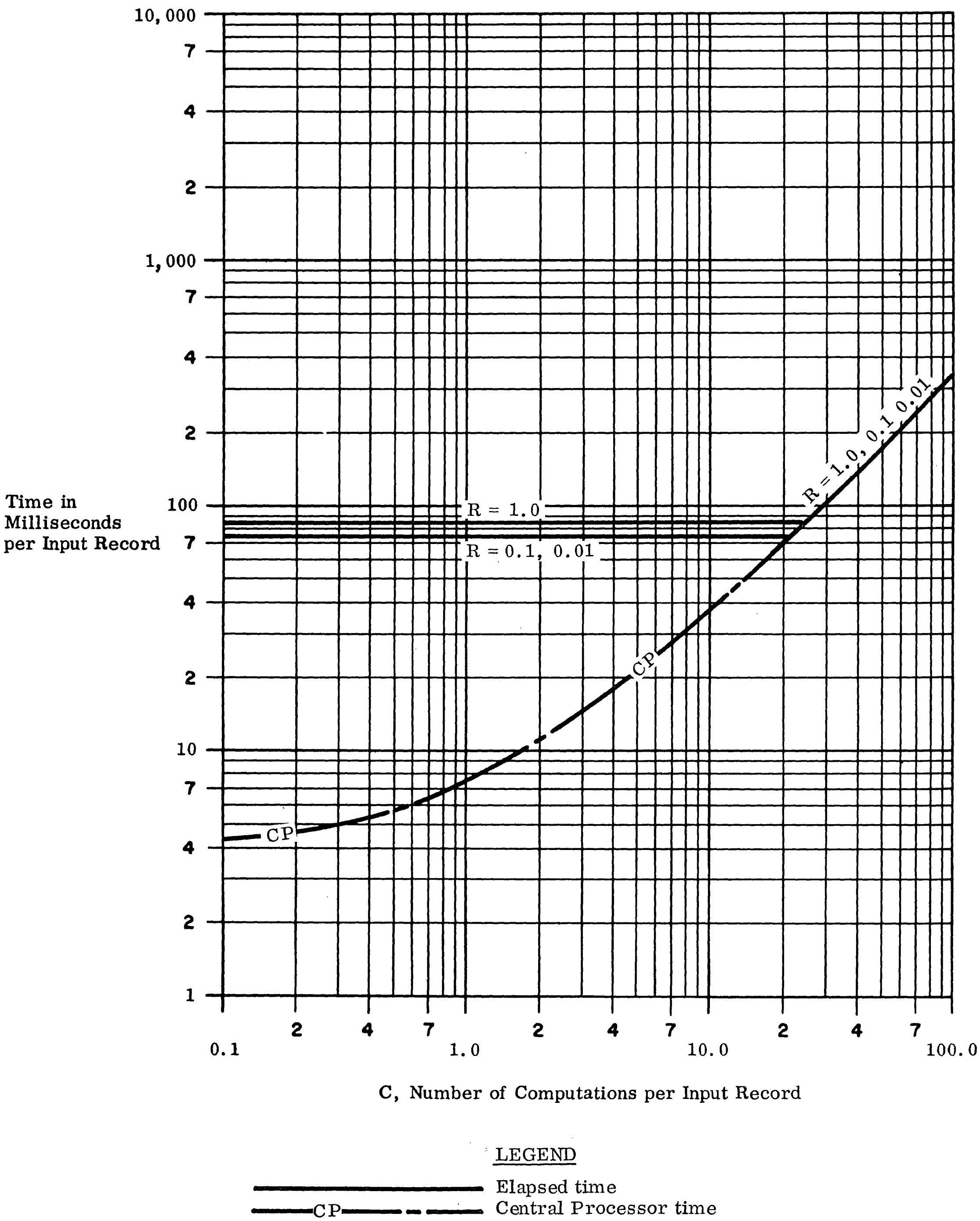
.411 Record sizes: . . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

.412 Computation:. . . . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.413 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

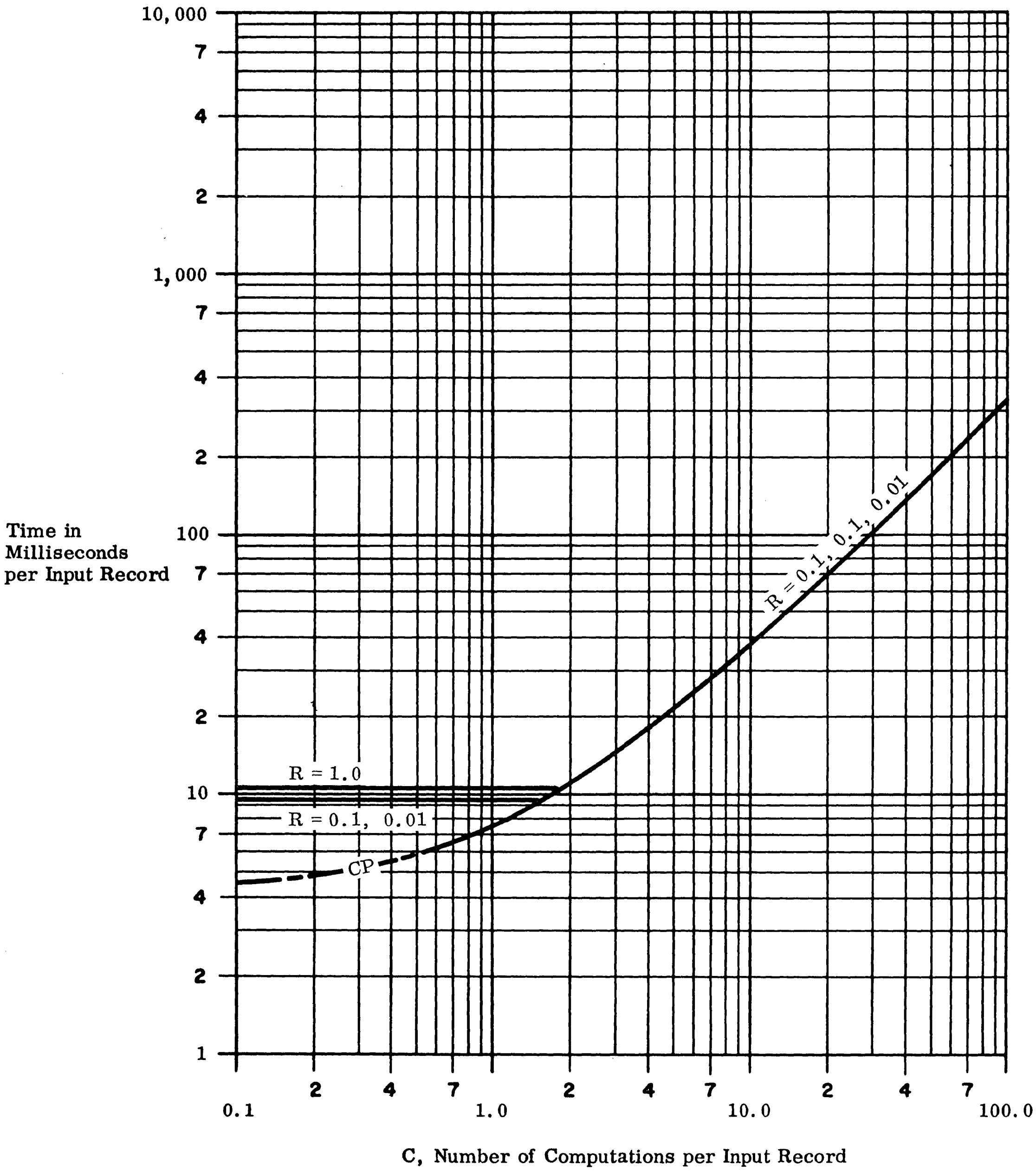
.414 Graph: . . . . Configurations III, V, and VIIA; punched card input, line printer output.

CONFIGURATIONS III, V, AND VIIA



.415 Graph: . . . . see graph below, for Configuration VIIB only; magnetic tape input and output.

CONFIGURATION VIIB



LEGEND

———— Elapsed time

——CP—— — —— Central Processor time

PHYSICAL CHARACTERISTICS

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
B 5281 Processor	45	32	74	1,000	1.8	6,800
B 5282 I/O Subsystem	45	32	74	1,000	1.5	5,400
B 5220 Central Control	45	32	74	1,000	2.0	7,400
B 5290 Display and Distribution	45	32	74	1,000	1.1	4,000
B 5370 Power Supply	45	32	74	1,000	3.8	13,000
B 5310 Console	72	24	29	250	2.4	900
B 460/461 Memory Module	45	32	74	1,000	5.4	18,500
B 430 Drum Subsystem	45	32	74	1,300	1.8	5,000
B 450 Basic Disk File/ Data Communications Control Cabinet	45	32	74	1,000	1.5	5,000
B 471 Disk File Electronics Unit	45	46	53	450	1.1	4,100
B 475 Disk File Storage Module	22	46	53	3,800	1.4	3,800
B 122 Card Reader	29	17	41	102	0.20	700
B 123/124/129 Card Readers	48	29	50	920	1.3	3,000
B 303 Card Punch	44	28	53	655	1.4	4,000
B 304 Card Punch	73	27	47	1,283	2.2	5,500
Line Printers (all models)	74	29	55	1,738	2.3 (idle) 3.5 (printing)	4,480
Magnetic Tape Units (all models)	29	28	74	900	2.0 to 3.3	7,200
B 141 Paper Tape Reader	30	24	60	437	0.91	3,100
B 341 Paper Tape Punch	30	24	60	426	0.59	1,500
B 481 Teletype Terminal	24	38	42	500	0.23	800
B 483 Typewriter Terminal	24	38	42	500	0.23	800
B 493 Typewriter Inquiry Station	18	20	40	60	0.26	800
B 484 Dial TWX Terminal	24	38	42	500	0.23	800
B 487 Data Transmission Terminal Unit	?	?	?	?	?	?

General Requirements

Temperature: . . . . between 60° and 100°F.
Relative humidity: . . . . . . between 10% and 90%.
Power: . . . . 120-volt, 1-phase, 60-cycle, 3-wire.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	One-Time Charge*	Monthly Rental $	Monthly Maintenance** $	Purchase $
PROCESSING AND CONTROL UNITS	B 5280	Central Processor System, including: B 5220 Central Control B 5281 Processor B 5282 I/O Subsystem (without I/O Channels) B 5290 Display and Distribution B 5310 Console B 5370 Power Supply		7,400	265.00	307,100
	B 5281	Central Processor (an optional second Processor)		4,500	120.00	186,750
	B 5283	I/O Channel (maximum of 4)		1,250	65.00	51,875
MAIN AND AUXILIARY STORAGE	B 460	Memory Module (6 μsec core, 4,096 words)		1,250	55.00	51,875
	B 461	Memory Module (4 μsec core, 4,096 words)		1,450	60.00	60,175
	B 430	Magnetic Storage Drum (32,768 words)		1,700	65.00	70,550
	B 5470	Disk File Control		590	65.00	26,550
	B 450	Basic Disk File/Data Communications Cabinet		255	40.00	11,475
	B 451	Disk File Expanded Control		200	25.00	9,000
	B 452	Basic Disk File/Data Transmission Terminal Unit Cabinet		255	40.00	11,475
	B 471	Disk File Electronics Unit		710	80.00	31,950
	B 475	Disk File Storage Module (9.6 million char)		990	115.00	44,550
INPUT-OUTPUT		Readers, Punches, Printers				
	B 122	Card Reader (200 cpm)		220	40.00	9,900
	B 123	Card Reader (475 cpm)		320	70.00	18,000
	B 124	Card Reader (800 cpm)		400	75.00	18,000
	B 129	Card Reader (1,400 cpm)		600	115.00	27,000
	B 303	Card Punch (100 cpm)		450	65.00	20,250
	B 304	Card Punch (300 cpm)		650	115.00	29,250
	B 141	Paper Tape Reader (500-1,000 char/sec)		400	70.00	18,000
	920	Input Code Translator		180	10.00	8,100
	B 341	Paper Tape Punch		190	40.00	8,550
	930	Output Code Translator		170	10.00	7,650
	B 320	Line Printer (475 lpm; 120 pos.)		810	170.00	54,000
	B 321	Line Printer (700 lpm; 120 pos.)		1,200	175.00	54,000
	B 325	Line Printer (700 lpm; 132 pos.)		1,275	185.00	57,375
	B 328	Line Printer (1,040 lpm;120 pos.)		1,325	195.00	59,600
	B 329	Line Printer (1,040 lpm; 132 pos.)		1,400	205.00	63,000
	871	132 Print Position Capability, per I/O Channel	$105.00	100	20.00	4,000

* One-time charge is applicable when certain features are added to an existing installation.
** Maintenance charges are slightly higher in rural areas.

CLASS	IDENTITY OF UNIT		PRICES			
	No.	Name	One-Time Charge*	Monthly Rental $	Monthly Maintenance** $	Purchase $
INPUT-OUTPUT (Continued)		Magnetic Tape Units				
	B 422	Magnetic Tape Unit (24/66 KC at 120 ips)		800	155.00	36,000
	B 423	Magnetic Tape Unit (24 KC at 120 ips)		495	145.00	31,500
	B 424	Magnetic Tape Unit (66 KC at 83 ips)		850	165.00	38,250
	B 425	Magnetic Tape Unit (18/50/72 KC at 90 ips)		850	165.00	38,250
	872	Extended Magnetic Tape Capability, per I/O Channel (provides three-transfer-rate capability, beginning of tape, end of tape, and blank tape sensing)	$500.00	100	20.00	4,500
		Data Communications Devices				
	B 5480	Data Communications Control		460	55.00	20,700
	B 249	Data Transmission Control Unit		295	45.00	13,275
	B 481	Teletype Terminal Unit:				
		120-Character Buffer		460	55.00	20,700
		240-Character Buffer		480	55.00	21,600
	B 483	Typewriter Terminal Unit		660	75.00	29,700
	B 493	Typewriter Inquiry Station		55	10.00	2,475
	B 484	Dial TWX Terminal Unit		700	80.00	31,500
	B 487	Data Transmission Terminal Unit		495	95.00	22,275
	873	B 487 Capability, per I/O Channel	$50.00	100	20.00	4,500
	980	Dial TWX/Typewriter Adapter	$50.00	40	5.00	1,800
	981	Teletype Adapter	$50.00	60	10.00	2,700
	982	Dataspeed Type 2 Adapter	$50.00	45	10.00	2,025
	983	801A Auxiliary Data Set Adapter	$50.00	35	5.00	1,575
	984	UNIVAC 1004 Adapter	$50.00	170	30.00	7,650
	985	IBM 1050 Adapter	$50.00	85	15.00	3,825

* One-time charge is applicable when certain features are added to an existing installation.
** Maintenance charges are slightly higher in rural areas.

BURROUGHS 500 SYSTEMS

Burroughs Corporation

STANDARD EDP REPORTS

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ADVANCE REPORT: BURROUGHS B 2500 AND B 3500

.01 INTRODUCTION

Burroughs Corporation announced two new small-to-medium-scale computer systems, the B 2500 and B 3500, on March 29, 1966. The two new systems are billed as the newest members of the "Burroughs 500 systems" computer family. The only previously-introduced members of this family are the B 5500 and the B 8500. There will, however, be no direct program compatibility between the two new systems and either the B 5500 or the B 8500.

The Burroughs B 5500 (Report 203:) is a medium-scale computer of highly unusual design; it has been in use for some time and has demonstrated the practicality of multiprogrammed operation and of programming and debugging exclusively in higher-level languages (ALGOL, COBOL, and FORTRAN). The B 8500 is an ultra-large-scale computer, announced last summer, with extensive capabilities for modular expansion, multiprocessing, and multiprogramming. The B 2500 and B 3500 are considerably more conventional in design (i.e., more like most of the other computer systems currently on the market) than the B 5500 or B 8500, although the designers of the two new systems have borrowed certain important concepts from the larger Burroughs systems. These concepts include operation under an integrated Master Control Program, emphasis upon multiprogrammed operation, and use of a "stack" to store subroutine parameters.

The Burroughs 500 Systems computer family is due for further expansion during the next few months, probably through the announcement of a small-scale system to compete with IBM's System/360 Model 20 and a large-scale system to fill the gap between the B 5500 and the B 8500. With these additions, Burroughs' computer line should approach the IBM System/360 line in range and suitability for varied applications.

The B 2500 and B 3500 systems are fully program-compatible with one another. The only significant differences between the two systems are in internal speed (the B 3500 is twice as fast), maximum number of I/O channels (6 for the B 2500 and 20 for the B 3500), and maximum core memory capacity (60,000 bytes for the B 2500 and 500,000 bytes for the B 3500). Compatibility with the second-generation Burroughs B 200/300 Series and IBM 1401/1440/1460 systems will be achieved through optional emulators. Although the B 2500 and B 3500 use the

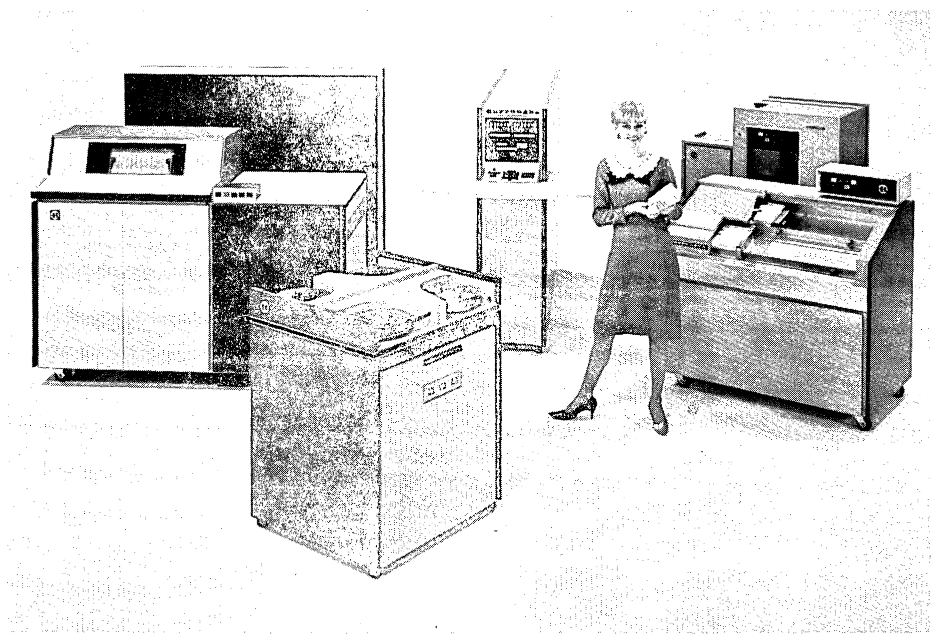

Figure 1. A small B 2500 tape system. A 4-drive Magnetic Tape Cluster is in the foreground.

.01 INTRODUCTION (Contd.)

same data structure and codes as the IBM System/360, there will be no program compatibility between the two lines.

The new Burroughs systems are definitely "third-generation" in their use of monolithic integrated circuits and a read-only memory. The read-only memory in the processor holds microprograms which initiate and control all processor operations, thereby reducing the amount of wired logic that must be built into the processor and facilitating the emulation of dissimilar computers.

A fairly wide variety of peripheral equipment is offered, though most of it is quite conventional and similar to Burroughs' second-generation peripheral equipment. The only distinctively new peripheral devices are the Magnetic Tape Cluster, which is a compact, economical unit containing up to four tape drives, and the Systems Memory, a low-priced, fast-access disc unit designed to hold the Master Control Program and other software facilities. New single-line and multi-line communications controls provide flexible facilities for data communications and real-time applications. Burroughs continues to stress the speed and reliability of its head-per-track Disk Files.

Software support is divided into two levels, Basic and Advanced. Each level is designed for use with a separate operating system. An assembler, sort generator, and report generator are provided at each level. COBOL and FORTRAN compilers, however, are offered only at the Advanced level, and no ALGOL compiler has been promised. At the Basic level — intended for small configurations — the Basic Control Program controls simple stacked-job processing and straightforward I/O operations. Systems equipped with disc storage and at least 20,000 bytes of core memory will usually use the Advanced software. At this level the Master Control Program schedules and controls multiprogrammed operations and performs many other functions usually found only in the operating systems for much larger computers.

First deliveries of B 2500 systems (and the Basic Control Program) are scheduled for January 1967. Deliveries of B 3500 systems (and the Master Control Program) will begin in May 1967. The COBOL compiler is scheduled for delivery in July 1967. Burroughs states that typical lease prices will range from $4,195 per month for a small B 2500 tape system to $20,720 per month for a large B 3500 system with 100 million bytes of disc storage and 8 tape units.

.02 DATA STRUCTURE

The B 2500 and B 3500 systems provide facilities for convenient handling of variable-length fields composed of either 8-bit bytes or 4-bit digits. Core memory is addressable by digit position. The basic unit of data, however, is the "word," which consists of 16 data bits plus one parity bit and is the amount of information that can be read from or written into core memory during each cycle. A word can hold either two 8-bit bytes or four 4-bit digits.

Data represented in the 4-bit format can be either signed (with a 4-bit sign digit preceding the most significant numeric digit of the field) or unsigned. Data in the 8-bit format is always unsigned, but all-numeric fields represented in the 8-bit mode can be used as operands in fixed-point arithmetic operations without the need (as in the IBM System/360) for prior conversion to the 4-bit digit mode. Data may be represented internally in either of two codes, EBCDIC or ASCII, as discussed in Paragraph .14.

Floating-point numbers can have variable-length mantissas of up to 100 digits. Every floating-point number consists of: one digit that specifies the sign of the exponent, two decimal digits that specify the exponent's value, one digit that specifies the sign of the mantissa, and from 1 to 100 decimal digits that specify the mantissa's value. The mantissa always represents a whole number (rather than a fraction as in most computers), with the decimal point assumed to the right of the last digit.

Instructions can consist of one, two, three, or four 6-digit "syllables" or of a single 8-digit syllable. See Paragraph .051 for a detailed description of the instruction format.

.03 SYSTEM CONFIGURATION

The B 2500 "central system" consists of a 2501 Central Processor and one combined input/output and memory cabinet. Core memory capacity can range from 10,000 to 60,000 bytes in 10,000-byte increments. Four I/O channels (two type A and two type B) are included in the basic system; a maximum of two additional channels (one type A and one type B) can be installed.

The B 3500 "central system" consists of a 3501 Central Processor, one or two input/output cabinets, and from one to six memory cabinets. Core memory capacity can range from 10,000 to 500,000 bytes in 18 different sizes (see Price Data, Section 210:221).

(Contd.)

.03 SYSTEM CONFIGURATION (Contd.)

Six I/O channels (three type A and three type B) are included in the basic system; a maximum of 14 additional channels (seven type A and seven type B) can be installed.

Optional features available for both central processors include the B 200/B 300 Emulator, the IBM 1401/1440/1460 Emulator, floating-point arithmetic, and a desk-level console.

The operations of all peripheral devices are controlled by I/O control units. One I/O control can be connected to each B 2500 or B 3500 I/O channel, and each type of peripheral device requires a different I/O control. Most of the I/O controls (card reader, punch, printer, paper tape, etc.) can accommodate only one peripheral unit each, but the controls for magnetic tape and disc storage devices can accommodate multiple units, as explained in the descriptions of these devices. Further flexibility in the control of magnetic tape and disc operations is provided by a series of Exchange units, which permit a group of tape or disc units to communicate with the central processor via either of two or more I/O control units and the associated I/O channels.

The two types of I/O channels differ in their modes of communication with the processor and, therefore, in the data rates they can accommodate. Type A channels transfer only one character at a time to or from core memory and are limited to handling the following low-speed peripheral devices: card readers or punches, paper tape readers or punches, buffered line printers, listers, MICR sorter/readers, on-line banking subsystems, or the console printer. Type B channels transfer two characters in parallel to or from core memory and can handle the following types of peripheral devices: magnetic tape units, Disc Files, Systems Memory, unbuffered printers, and data communications controls. Through the use of "type B" controls, type B channels can alternatively be used for low-speed peripheral devices.

To indicate the range and general makeup of practical system configurations, the components and features required for three of our Standard Configurations (as defined in Section 4:030 of the Users' Guide) are listed below, along with their one-shift monthly rentals.

.031 4-Tape Business System; Configuration II (B 2500)

Equipment	Rental
1 - 2501 Central Processor with Console and 4 I/O Channels	$1,195
1 - 2001 Memory Module (10,000 bytes)	450
1 - 9381-4 4-Station 36KB Magnetic Tape Cluster	1,300
1 - 2381-1 36KB Tape Cluster I/O Control	200
1 - 9240 Printer (700 lpm)	800
1 - 2241 Printer I Output Control	75
1 - 9111 Card Reader (800 lpm)	325
1 - 2110 Card Reader Input Control	50
1 - 9210 Card Punch (100 cpm)	350
1 - 2210 Card Punch Output Control	50
Total Rental:	$4,795

.032 6-Tape Auxiliary Storage System; Configuration V (B 3500)

Equipment	Rental
1 - 3501 Central Processor with Console and 6 I/O Channels	$1,695
1 - 3002 Memory Module (20,000 bytes)	1,000
1 - 9371 Disk File Electronics Unit	650
2 - 9372 Disk File Modules (20 million bytes total)	1,650
1 - 3373 Disk File I/O Control	250
2 - 9381-3 3-Station 36KB Magnetic Tape Clusters	2,200
1 - 3381 36KB Tape Cluster I/O Control	235
1 - 9240 Printer (700 lpm)	800
1 - 3241 Printer I Output Control	75
1 - 9111 Card Reader (800 lpm)	325
1 - 3110 Card Reader Input Control	50
1 - 9210 Card Punch (100 cpm)	350
1 - 3210 Card Punch Output Control	50
1 - 9340 Console Printer and Keyboard	55
1 - 3340 Console Printer I/O Control	100
Total Rental:	$9,485

.033 10-Tape General-Purpose System; Configuration VIIA (B 3500)

Equipment	Rental
1 - 3501 Central Processor with Console and 6 I/O Channels	$1,695
1 - 3510 Additional Type A I/O Channel	35
1 - 3012 Memory Module (120,000 bytes)	4,500
1 - 9370-1 Systems Memory (1 million bytes)*	375
1 - 3371 Systems Memory I/O Control*	150
10 - 9392 72KB Free-Standing Magnetic Tape Units	5,750
2 - 3393-1 Magnetic Tape I/O Controls	750
1 - 3491 Magnetic Tape Exchange (2 x 10)	250
1 - 9240 Printer (700 lpm)	800
1 - 3240 Printer I Output Control	75
1 - 9111 Card Reader (800 lpm)	325
1 - 3110 Card Reader Input Control	50
1 - 9210 Card Punch (100 cpm)	350
1 - 3210 Card Punch Output Control	50
1 - 9340 Console Printer and Keyboard	55
1 - 3340 Console Printer I/O Control	100
1 - 3530 Floating-Point Arithmetic Feature	100
Total Rental:	$15,410

* Included to provide the disc storage needed for Master Control Program use.

.04 INTERNAL STORAGE

.041 Core Memory

Core memory cycle times are two microseconds in the B 2500 and one microsecond in the B 3500. Read access times are 700 nanoseconds and 350 nanoseconds, respectively. Both processors access one word, consisting of 16 data bits plus one parity bit, per cycle. Because core memory is addressable by digit position and each word can hold four digits, all word addresses are modulo-4. Whenever a specific digit or byte position is addressed, the entire word in which it is located is accessed. Data can be transferred to or from core memory by either the central processor or any of the I/O control units.

B 2500 core memory capacities can range from 10,000 to 60,000 bytes in increments of 10,000 bytes (i.e., 5,000 words). B 3500 memory capacities can range from 10,000 to 500,000 bytes in 18 different sizes; see the Price Data section (210:221) for the available capacities and the associated model numbers.

The first 1,200 digit positions of core memory are reserved for use by certain processor instructions, the interrupt system, the I/O control units, and the Master Control Program (when used). In addition, the first 64 digit positions of the core area assigned to each program are usually reserved to hold that program's index registers and other specific information.

To prevent accidental over-writing of one program by another during multiprogrammed operation, each core memory address is checked to ensure that it lies between the boundaries established by the base register and the limit register (see Paragraph .053). If not, the program is interrupted and control is transferred to the Master Control Program.

.042 Address Memory

The B 2500 and B 3500 Central Processors contain an Address Memory unit with a 100-nanosecond cycle time. Address Memory is an array of from 24 to 120 word locations, expandable in increments of 12 words. Each word is six 4-bit digits in length — long enough to hold the absolute address of any core memory location. Address Memory's purposes are to reduce the number of core memory accesses required and to perform a number of functions that usually require separate processor registers. The first eight words are used by the processor, and two words are assigned to each installed I/O channel. The I/O channel words contain the initial and final core memory addresses for the I/O operation in progress on the associated channel; these words are used by the I/O control units to determine the core memory locations where output data is to be accessed or input data stored.

.043 Systems Memory

Burroughs' 9370 Systems Memory is a new, single-disc storage unit designed to provide, at a fairly low cost, the random-access storage required to hold the systems software and the user's program library. As in Burroughs' larger Disk Files, one read/write head serves each track, so no access-arm movement is required. Average access time is 17 milliseconds, and the peak data transfer rate is 291,000 bytes per second.

(Contd.)

.043 Systems Memory (Contd.)

Two models of Systems Memory are offered. Model 9370-1 uses only one face of the disc and has a capacity of 1,000,000 bytes; Model 9370-2 uses both disc faces and holds 2,000,000 bytes. There are 100 data tracks per disc face. Each track is divided into 100 segments, and each segment holds 100 bytes (or 200 digits) of information. A longitudinal parity character is recorded at the end of each segment. Systems Memory is connected to a B 2500 or B 3500 Processor by means of a Systems Memory I/O Control. Two Systems Memory units can be connected to a single I/O Control by adding a Systems Memory Exchange.

.044 Disk File Subsystem

The 9371/9372 Disk File Subsystem is similar to the Burroughs Disk Files that have been in use for nearly two years with B 200/300 Series and B 5500 systems (see Report Sections 201:042 and 203:043). The use of a fixed read/write head for every data track provides fast access times (20 milliseconds average) and high reliability. Average data transfer rate is 200,000 bytes per second. The Disk File Subsystem is compatible with the 9370 Systems Memory in segment size (100 bytes) and addressing structure, so either unit can be used to hold the systems software and program library.

Each 9372 Disk File Module contains four non-removable discs and holds 10 million bytes. From one to five 9372 Modules can be connected to a 9371 Disk File Electronics Unit, providing up to 50 million bytes of storage. Disk File Exchanges (usable only in B 3500 systems) permit up to ten 9371 Electronics Units and the associated Disk File Modules to be connected to from one to four Disk File I/O Controls. The available Exchanges are designated 1 x 5, 2 x 5, and 4 x 10; the first number is the maximum number of Controls and the second is the maximum number of Electronics Units that can be interconnected. Since each I/O Control is connected to a separate channel, the 2 x 5 and 4 x 10 Exchanges, in effect, provide "floating" I/O channels and two-way or four-way simultaneity for Disk File operations.

.05 CENTRAL PROCESSORS

The central processors used in B 2500 and B 3500 systems are functionally identical and completely program-compatible; they differ only in internal speeds. The processor contains the arithmetic unit, logic controls, and interrupt facilities for a B 2500 or B 3500 system. No facilities for multiple-processor configurations have been announced to date.

.051 Instruction Formats

There are two basic types of instructions: I/O instructions (called "descriptors" and discussed in Paragraph .11) and processor instructions. Processor instructions may be one, two, three, or four 6-digit "syllables" in length and may contain — respectively — zero, one, two, or three core memory addresses. (Branch instructions are eight digits in length, and therefore constitute an exception to the normal instruction format.)

The first two 4-bit digits of a processor instruction designate the operation code and initiate execution of the appropriate string of microprograms stored in the system's Read-Only Memory, a resistive-type memory with a 100-nanosecond access time. These microprograms fetch the remainder of the instruction and perform the specified operation.

In most instructions, the third, fourth, fifth, and sixth digits of the first syllable specify the lengths of the A and B operands, which can range from 1 to 100 digits or bytes, or up to 10,000 words (depending upon the operation).

In multi-syllable instructions, the second, third, and fourth syllables (when present) specify the A-field, B-field, and C-field addresses, respectively. The first digit of each address syllable specifies: (1) which, if any, of three index registers shall be used in forming the machine address, and (2) the format of the data field. Each program has its own complement of three 8-digit index registers, which are held in reserved locations in core memory. There are four format possibilities: signed 4-bit, unsigned 4-bit, unsigned 8-bit, or indirect address (which means that the data field's address, rather than the data field itself, will be found in the memory location specified by the address syllable). The remaining five digits of each address syllable specify the data field address itself.

In many instructions, the second syllable may contain a literal operand rather than the A-field address. Literal operands are limited to a maximum length of three bytes (or six digits).

.051 Instruction Formats (Contd.)

All addresses in processor instructions are "base-relative." This means that each program is written as if it started in the first location of core memory. At execution time, each address is automatically incremented by the contents of a three-digit, modulo-1000 base register to form an absolute address (which can be further modified by indexing if desired). The base-relative addressing technique facilitates program relocation and segmentation; it also permits up to 1 million digits (500,000 bytes) of core memory to be addressed although the instruction addresses are only five digits long.

.052 Processing Facilities

The instruction repertoire includes efficient facilities for arithmetic, data movement, comparison, and editing of variable-length decimal and alphanumeric data fields. No binary arithmetic facilities are available, although logical AND, inclusive OR, and exclusive OR instructions are provided. Fixed-point decimal arithmetic instructions include three-address addition, subtraction, multiplication, and division, as well as two-address addition and subtraction. The optional Floating-Point feature provides three-address instructions to add, subtract, multiply, and divide floating-point operands with 2-digit exponents and mantissas varying from 1 to 100 digits in length. Representative execution times are shown in Table I.

A novel feature of the new Burroughs processors is their ability to combine numeric operands in the 4-bit and 8-bit data formats in a single operation, without prior transformation. The programmer can specify the format in which the results of such mixed-format operations shall be expressed: signed 4-bit, unsigned 4-bit, or 8-bit.

A group of Scan instructions facilitates the coding of search operations by enabling the programmer, by means of a single instruction, to search a string of up to 100 characters for the presence (or absence) of a specified character or group of characters. A Translate instruction effects translations from any 4-bit or 8-bit code to any 8-bit code through the use of a table in core memory. The Edit instruction moves up to 100 characters or digits from a source field to a destination field under the control of a string of "micro-operators" in core memory, which can specify that any character shall be inserted, suppressed, or floated under a variety of conditions. This flexible instruction permits normal dollar-and-cent punctuation and either floating dollar sign or check protection to be accomplished in a single operation.

Two special instructions, Enter and Exit, facilitate entry to and exit from subroutines, especially when the subroutines are used in nested or recursive fashion. The Enter instruction causes return control information and subroutine parameters to be moved into the "stack," which is a core memory area that has been reserved by the programmer. If another subroutine is entered prior to exit from the first subroutine, additional return control information and parameters will be moved into the stack, causing the previously-stored parameters to be "pushed down" deeper into the stack. Thus, subroutines can be nested or used recursively to any level up to the capacity of the stack.

.053 Operational States

The central processor always operates in one of two states: the Normal State, in which user programs are executed, or the Control State, in which the functions of the MCP or BCP operating systems are performed. Several "privileged" instructions can be executed only in the Control State. These instructions permit the MCP or BCP to initiate I/O operations and to control the program mix by setting and clearing registers and flip-flops.

TABLE I: REPRESENTATIVE EXECUTION TIMES, IN MICROSECONDS

Task	Fixed Point (signed 5-digit operands)		Floating Point (5-digit mantissas)	
	B 2500	B 3500	B 2500	B 3500
c = a + b	75	37.5	102	51
b = a + b	66	33	—	—
c = a x b	416	208	462	231
c = a/b	1810	905	1860	930
Move a to b	54	27	—	—
Compare a to b	60	30	—	—

(Contd.)

.053 Operational States (Contd.)

A powerful interrupt system causes the processor to enter the Control State and branch to the MCP or BCP whenever any of the following conditions occurs: completion of an I/O operation, memory parity error, memory address error, invalid instruction (including attempted execution of a privileged instruction in the Normal State), instruction time out (failure to complete the execution of an instruction within a preset time limit), and clock interrupt. Memory address errors can result from the formation of an address beyond the bounds established by the base and limit register settings, a non-decimal digit in an address, or a "non-synchronized" address (i.e., an address that is not modulo-2 or modulo-4 when a particular instruction or data format requires such an address). A clock interrupt occurs when the processor's six-digit timer, which is incremented once each millisecond, reaches a programmer-specified control value.

Memory protection — an essential feature for successful multiprogramming — is provided by the hardware, using the base and limit registers and the interrupt system. When the MCP initiates execution of a program, it sets the base register to the program's initial core memory location. The limit register's setting is made equal to the base register setting plus the total core memory requirement for the program. Before data is fetched, all machine addresses are checked against the base and limit register settings. An out-of-bounds address causes an interrupt and a transfer of control to the MCP, which suspends execution of the offending program.

.06 CONSOLE

The operator's console for both the B 2500 and B 3500 systems is mounted on the front of the central processor cabinet, above a shelf that serves as a small worktable. The console consists of a sloping control panel and a vertical display panel. The display panel features two six-digit Nixie tube displays that can be used, under console control, to display instruction syllables, addresses, and the contents of selected memory locations and registers.

The 9340 Console Printer and Keyboard is an optional Teletype Model 33 or Model 35 Keyboard Send/Receive set that uses one type A I/O channel and provides keyboard input and printed output at a maximum speed of 10 characters per second. The 9340 is required for operation under the Master Control Program.

.07 INPUT-OUTPUT; PUNCHED CARDS AND PUNCHED TAPE

Burroughs offers three card readers, two card punches, a paper tape reader, and a paper tape punch for use with B 2500 and B 3500 systems. Except for certain difference in codes, all of the new units are similar to previous Burroughs peripheral units used with B 100/200/300 Series and B 5500 systems, as described in Report Sections 201:071 thru 201:075.

.071 Card Readers

The 9110 Card Reader is a compact unit that reads standard 80-column cards photoelectrically, in column-by-column fashion, at a peak speed of 200 cards per minute. An immediate-access clutch permits the reading of an 80-column card to be completed within a maximum of 350 milliseconds after a "start feed" signal is received. The input hopper and output stacker have a capacity of 450 cards each.

The 9111 Card Reader uses an immediate-access clutch, a belt drive mechanism, and 13 photoelectric read cells (one for timing) to read cards of 51, 60, 66, or 80 columns at a peak rate of 800 cards per minute. The input hopper and output stacker can each hold up to 2400 cards and can be loaded and unloaded while the reader is operating. Optional features permit 40-column Treasury Checks or the round holes in Postal Money Orders to be read.

The 9112 Card Reader has a peak reading rate of 1400 cards per minute. Its appearance and physical characteristics are the same as those of the 9111 Card Reader described above.

All three card readers can read either the EBCDIC or the generally similar BCL (Burroughs Common Language) card code and translate it automatically to EBCDIC internal code. Binary card images can be read and stored in memory without conversion; the contents of each card column are stored in the six low-order bit positions of two consecutive bytes.

.072 Card Punches

The 9210 Card Punch can punch standard 80-column cards at a peak rate of 100 cards per minute. Cards are punched one row at a time by a single row of 80 die punches. Punching accuracy is checked by the hole-count method. The input hopper and output stacker can each hold up to 800 cards and can be loaded and unloaded while the punch is operating.

.072 Card Punches (Contd.)

The 9211 Card Punch punches 80-column cards, in row-by-row fashion, at a peak rate of 300 cards per minute. Punching accuracy is checked by the hole-count method. The input hopper can hold up to 3500 cards. There are three stackers: a 3000-card primary stacker, a program-selectable 850-card auxiliary stacker, and a 750-card error stacker.

Both card punches can perform automatic translations from the EBCDIC internal code to EBCDIC card code. Alternatively, binary cards can be punched; the contents of the six low-order bit positions of two consecutive bytes of core memory are accessed and punched into each card column. A standard feature in the Card Punch Control permits automatic translation from EBCDIC internal code to the 64-character BCL (Burroughs Common Language) code, or optionally to the BULL or ICT card code.

.073 9120 Paper Tape Reader

The 9120 can read punched tape with 5, 6, 7, or 8 code levels at a peak speed of either 500 or 1,000 characters per second. Rated start and stop times are 5 and 20 milliseconds, respectively, and the reader can stop between consecutive characters. A standard plugboard permits the bit configurations read from tape to be interchanged and/or inverted. Automatic translation from either 5-level Baudot or 6-level BCL tape code to EBCDIC internal code is standard. For other punched tape codes, users can either add the optional 9926 Input Code Translator, which provides flexible code conversions under plugboard control, or read the tape codes directly and use programmed translation.

.074 9220 Paper Tape Punch

The 9220 can punch 5-, 6-, 7-, or 8-level tape at a peak speed of 100 characters per second. A standard plugboard permits the bit configurations from core memory to be interchanged and/or inverted prior to punching. Automatic translation from EBCDIC internal code to either 5-level Baudot or 6-level BCL tape code is standard. For other punched tape codes, either programmed translation or the optional 9928 Output Code Translator can be employed.

.08 INPUT-OUTPUT; PRINTERS

.081 Line Printers

Four line printers of the conventional drum type are available for use with B 2500 and B 3500 systems. Users can choose a buffered printer with a peak speed (at single spacing) of either 700 or 1040 lines per minute, or an unbuffered model with a peak speed of either 815 or 1040 lines per minute. Table II lists the peak printing speeds and skipping speeds of the four models.

All four printers have 120 print positions, with 12 additional positions available through use of the 9941 option. All models use the 64-character Burroughs Common Language character set. (Other character sets are available on a special-order basis.) Forms can be from 5 to 20 inches in width and can have a maximum length of 22 inches (when printing at 6 lines per inch) or 16.5 inches (at 8 lines per inch). Vertical format control is provided by a 12-level carriage control tape loop.

TABLE II: LINE PRINTER SPEEDS

Model No.	Peak Printing Speed, lines/minute	Skipping Speed, inches/second	Buffer
9240	700	25 to 40	Yes
9241	1040	25 to 40	Yes
9242	815	25 (75 with option)	No
9243	1040	25 (75 with option)	No

.082 9244 Tape Lister

The Burroughs Tape Lister is designed primarily to provide high-speed printed listings of MICR documents as they are read by a MICR Sorter-Reader. From 6 to 18 listing tapes can be individually advanced and printed upon, enabling the contents of each Sorter-Reader pocket to be listed on a separate tape. The six-tape 9244-1 master unit can be used alone, or one or two six-tape 9244-2 slave units can be connected to it.

The peak printing rate of 1565 lines per minute can be maintained when printing is restricted to a 16-character set (the digits 0-9 and six special symbols). When the full, alphanumeric

(Contd.)

.082 9244 Tape Lister (Contd.)

set of 40 characters is used, the rated speed is 600 lines per minute. Printing is performed on 2.5-inch-wide, single-ply or two-ply adding machine tapes. Print lines can extend to 22 print positions on each tape. The 9244-1 unit contains a 44-character buffer. The contents of buffer positions 1 through 22 are simultaneously printed on the master tape and on a selected detail tape. In addition, when operating in the "multiprocessing" mode, the contents of buffer positions 23 through 44 can be simultaneously printed on a third tape.

.09 INPUT-OUTPUT; MAGNETIC TAPE

.091 Magnetic Tape Cluster

The most novel peripheral units announced for use with B 2500 and B 3500 systems are the 9381 and 9382 Magnetic Tape Clusters, which provide two, three, or four tape drives in a single compact unit (33 inches wide, 30 inches deep, and 42 inches high). Reading and/or writing can be performed simultaneously on any two of the tape drives in a cluster if two Tape Controls and a 2 x 8 Exchange are employed. Each tape drive has its own drive mechanism, but the read/write electronics and power supply are shared. The feed reel and take-up reel for each drive are mounted on concentric vertical shafts, with the feed reel above the take-up reel. Tape is driven by a capstan roller and pinch rollers. Normal tape speed is 45 inches per second, and rewind speed is 90 inches per second. Tape can be read in either the forward or reverse direction.

The standard recording medium for the Magnetic Tape Clusters is 9-track, 1/2-inch-wide tape which is compatible with the IBM System/360 9-track tape units. Each unit can read and record at any two of the following three densities: 200, 800, or 1600 rows per inch. The associated peak data transfer rates are 9,000, 36,000 or 72,000 bytes per second, respectively. A single Tape Control can handle up to 8 tape drives of either the 36KB or 72KB transfer rate, but not both.

Optionally, individual tape drives can be field-modified to use 7-track tape which is compatible with earlier Burroughs and IBM systems. Seven-track and nine-track drives can be intermixed in the same Tape Cluster, although the two types must be served by separate controls. In the 7-track mode, the available densities are 200, 556, and 800 rows per inch, and the associated data transfer rates are 9,000, 25,000 and 36,000 characters per second.

.092 Free-Standing Magnetic Tape Units

Burroughs also offers four different free-standing tape units for B 2500 and B 3500 systems. Their recording densities and speeds are summarized in Table III. Two of these units use 7-track tape and are similar to earlier Burroughs units, as described in Report Section 201:091. The other two units use 9-track tape at recording densities of either 800 or 1600 rows per inch to achieve compatibility with the IBM System/360. All four models can read tape in either the forward or reverse direction at 90 inches per second; rewind speed averages 300 inches per second.

Up to ten free-standing tape units (all of the same type) can be connected to each Tape Control. Read/write simultaneity within a single group of tape units can be achieved (in B 3500 systems only) through use of a second Tape Control and a 2 x 10 Magnetic Tape Exchange unit.

TABLE III: FREE-STANDING MAGNETIC TAPE UNITS

Model No.	Recording Densities, rows/inch	Peak Data Transfer Rates
9390	200/556	18/50 KC/sec
9391	200/556/800	18/50/72 KC/sec
9392	200/800	18/72 KB/sec
9393	200/1600	18/144 KB/sec

.10 INPUT-OUTPUT; OTHER

.101 MICR Sorter-Reader

Burroughs, a leader in banking applications and in the design of MICR equipment, offers three MICR Sorter-Readers for use with the B 2500 and B 3500 systems. All are closely related to the MICR units used with B 100/200/300 Series systems and described in detail in Report Section 201:102. The maximum speed of all three units is 1565 items per minute. Model 9130 is an off-line unit that reads MICR-encoded documents and sorts them into 13 pockets. Models 9131 and 9132 are both designed for on-line use and are completely buffered; Model 9131 has 13 pockets and Model 9132 has 16 pockets.

.102 Data Communications Controls

Data communications equipment can be connected to a B 2500 or B 3500 system through individual Line Adapters and either Single-Line Controls or Multi-Line Controls. Eleven different Line Adapters permit communications with a variety of terminal equipment and common-carrier services; see the Price Data section, 210:221, for the function of each adapter. All adapters operate in the half-duplex mode.

The Single-Line Control coordinates the transmission of data between a single communications line equipped with an appropriate Line Adapter and a single B 2500 or B 3500 I/O channel (type B). The Single-Line Control is designed for limited data communications needs; if more than three lines must be controlled, it will be more economical to use one Multi-Line Control.

The Multi-Line Control uses two type B I/O channels and can control simultaneous transmissions over up to 36 communications lines, each equipped with an appropriate Line Adapter. One 40-bit word of scratchpad memory holds control information and data associated with each of the 36 subchannels. Only one Multi-Line Control can be connected to a B 2500 or B 3500 system.

.11 SIMULTANEOUS OPERATIONS

One data transfer operation on each installed B 2500 or B 3500 I/O channel can occur simultaneously with internal processing. All I/O operations, once initiated by the central processor, are executed independently of the processor under the direction of an I/O control unit. Requests for access to core memory by the processor and the various I/O channels are granted by priority logic; the processor always has the lowest priority.

Please refer to Paragraph .03 for the minimum and maximum number of type A and type B channels a system can include, the peripheral devices each type of channel can service, and other system configuration parameters.

Address Memory (Paragraph .042) is used to hold the core memory addresses associated with the I/O operation taking place on each channel. Therefore, only one core memory cycle (two microseconds in the B 2500, one microsecond in the B 3500) is required for each unit of I/O data transferred to or from core memory. Type A channels transfer one character at a time to or from memory, while type B channels transfer two characters in parallel.

I/O operations can be initiated only when the central processor is operating in the control state, and their execution will usually be directed by the Master Control Program. The processor initiates an I/O operation by sending an "I/O descriptor" to the appropriate control unit. I/O descriptors vary from one to four 6-digit syllables in length, and the core addresses they contain are absolute rather than base-relative. The processor then proceeds independently while the control unit directs the I/O operation. Upon completion, the control unit initiates a processor interrupt and sends a 16-bit "result descriptor" to a reserved location in core memory. The result descriptor informs the processor of any abnormal conditions or errors that have occurred.

.13 COMPATIBILITY

Burroughs, like IBM and RCA, has chosen the emulation approach for achieving program compatibility with certain second-generation computer systems. Emulation is a combined hardware/software technique that enables one computer to execute, without prior translation, machine-language programs written for a dissimilar computer.

An emulator for either the B 200/300 Series or the IBM 1401/1440/1460 systems (but not both) can be added, as an optional feature, to the central processor of either a B 2500 or B 3500 system. The emulator features consist of additional read-only memory containing microprograms that will trigger the appropriate hardware logic circuits to simulate the functions of most of the instructions in the original computer's repertoire. The read-only memory is complemented by a set of software subroutines that will simulate the original computer's I/O operations.

Burroughs has not yet defined the exact components and features of the B 200/300 Series and IBM 1401/1440/1460 computer systems that its emulators will or will not be able to handle. (Both of these second-generation computer lines offered such a wide variety of peripheral equipment that it is highly unlikely that Burroughs will deem it practical to emulate all of it.) Neither has Burroughs released any quantitative estimate to date of the performance it expects to achieve when executing programs in the emulation mode.

.14 DATA CODES

Like the IBM System/360, the new Burroughs systems can use either the 8-bit Extended BCD Interchange Code or an 8-bit extension of the 7-bit ASCII code. A mode flip-flop, resettable

(Contd.)

.14 DATA CODES (Contd.)

by the program, specifies whether the processor is to operate in the EBCDIC or ASCII mode. In the 4-bit mode, numeric digits are represented in a 4-bit subset of either the EBCDIC or ASCII code, depending upon the setting of the mode flip-flop.

A Translate instruction uses a table in core memory to accomplish efficient translations from any 4-bit or 8-bit code to any 8-bit code.

A hardware translator provides automatic translations between the EBCDIC internal code and the 6-bit BCL (Burroughs Common Language) code that can be used by the punched card, paper tape, and 7-track magnetic tape I/O devices. The 6-bit BCD code used by the IBM 1400 Series computers is, in turn, a subset of the BCL code. Thus, the hardware translator facilitates achieving code compatibility with earlier Burroughs and IBM equipment.

.15 SOFTWARE

Burroughs offers B 2500 and B 3500 users a choice of two levels of software support: a Basic package for small-scale configurations and an Advanced package for larger systems. Only the Advanced package permits use of the Master Control Program, the COBOL and FORTRAN compilers, and the multiprogrammed operational mode that Burroughs bills as principal features of the B 2500 and B 3500 systems. The facilities offered at each of the two software levels are summarized in the following paragraphs.

.151 Basic Software Package

The Basic package is designed for use with minimum-size B 2500 or B 3500 systems; it does not require a Disk File or Systems Memory unit or a Console Printer. The main component of the package is the Basic Control Program. Also included are an assembler, report generator, sort generator, and utility program generator. No compiler is provided at this level.

Basic Control Program (BCP)

The BCP is a group of interrelated loading and I/O routines that reside permanently in core memory. Burroughs states that the BCP routines and associated tables will require about 2,000 byte positions of memory. The BCP's principal functions are:

- To load and initiate execution of user programs in sequential fashion.
- To initiate all I/O operations requested by user programs.
- To service the interrupts that result upon completion of I/O operations.
- To transfer control to error-handling routines in the user program when errors or abnormal conditions are detected. (These error-handling routines can be extracted from the I/O library when the user program is assembled.)
- To receive control when a user program completes its run, and to load and initiate the next program.
- To assist in program debugging by means of trace and dump routines.

The BCP will accept any user program generated by the facilities of the Basic software package. In fact, the BCP's presence is required for execution of any program generated by this package. The BCP can be used with any legitimate B 2500 or B 3500 system configuration.

Basic Assembler

The Basic Assembler is a straightforward, tape-oriented symbolic assembly system that allows the programmer to utilize all the hardware facilities of B 2500 and B 3500 systems. Its use requires a processor with at least 10,000 bytes of core memory, two magnetic tape units, a card reader or paper tape reader for input, a line printer for the listing, and a card punch, paper tape punch, or a third magnetic tape unit for object-program output.

The assembly process is essentially a one-for-one translation in which symbolic instructions, coded in a fixed format, are converted into machine language instructions. Input-output operations — such as reading, writing, opening and closing of files, and generation and checking of labels — are coded by means of eight macro-instructions that generate linkages to the appropriate BCP I/O routines. I/O buffering, blocking, and unblocking operations, however, must be coded by the user. A group of pseudo-instructions is provided to control the assembly process. Segmentation of programs can be specified in the Basic Assembler language, but the actual overlaying of segments at object time must be coded by the user.

.151 Basic Software Package (Contd.)

Problem Oriented Facilities

The Basic Sort Generator accepts parametric input and produces tape sort programs in Basic Assembler language. Internal sorting is performed by the vector replacement selection technique, and a backward-read polyphase merge technique is used. From three to eight magnetic tape units can be used. Records or blocks can be up to 1000 characters long. Sort keys can be up to 100 characters long and located in up to 10 different areas of the record. Input and output records may be blocked. Multiple-reel input is allowed, and restart capabilities are provided.

The Basic Report Generator accepts problem-oriented specifications and generates programs, in Basic Assembler language, to produce the specified reports. Input to the object programs may be from punched cards or magnetic tape; output may be printed or on punched cards. Up to four levels of totals are permitted, and up to fifteen 12-position accumulators are available at each level.

The Basic Utility Program Generator accepts parametric input and generates programs to perform a variety of media conversion functions.

.152 Advanced Software Package

The Advanced package is designed for use with B 2500 or B 3500 systems that have at least 20,000 bytes of core memory, a Systems Memory unit or Disk File, and a Console Typewriter/Keyboard. Its principal component is the Master Control Program. Also included are an assembler, COBOL compiler, FORTRAN compiler, report generator, sort generator, and utility program generator.

Master Control Program (MCP)

The MCP is an integrated operating system that monitors and controls all operations of a B 2500 or B 3500 system. The MCP consists of a group of interrelated routines that will permanently occupy approximately 10,000 bytes of core memory plus 70,000 bytes of disc storage. The principal functions of the MCP are:

- To schedule the execution of user programs, in a multiprogramming environment, on the basis of their priorities and memory requirements.
- To load programs into core memory from cards, paper tape, magnetic tape, or disc storage.
- To allocate core memory and relocate user programs as necessary to achieve efficient utilization of the available memory.
- To schedule and initiate all I/O operations, using tables that indicate the status of each I/O device and the priority of each I/O request awaiting processing.
- To handle all error conditions that arise, usually by first retrying the operation and then either initiating a user-supplied error routine or aborting the program.
- To handle all communications between the system and the operator.
- To maintain a detailed log of all system operations.
- To maintain libraries, on disc storage, of user programs and systems software.
- To control compilations or assemblies, and either insert the resulting object programs into a library or execute them immediately.
- To control program segmentation by loading individual segments of a program upon request.
- To perform file control operations such as blocking, unblocking, label generation, and label checking.

The MCP will accept any user program generated by the facilities of the Advanced software package. In fact, the MCP's presence is required for execution of any program generated by this package.

(Contd.)

.152 Advanced Software Package (Contd.)

For B 2500 and B 3500 systems that use the MCP, Burroughs is placing a greater emphasis upon multiprogrammed operation than has the manufacturer of any previous small-to-medium-scale computer system. Multiprogramming (which Burroughs calls "multiprocessing") can increase a computer system's throughput by increasing the effective utilization of the processor, core memory, and all peripheral devices; and Burroughs has already demonstrated the practical value of multiprogramming in its B 5500 system, which uses a functionally similar Master Control Program and has been in service for more than two years.

Advanced Assembler

The Advanced Assembler is a disc-oriented symbolic assembly system that provides all the facilities of the Basic Assembler plus a few refinements. These refinements include:

- Facilities to operate under control of the MCP and to establish the necessary linkages with it.
- File declarations that specify, for each logical file, its label format, recording mode, buffer areas, retention period, blocking factor, etc.
- Macro-instructions to open and close files, initiate I/O operations, block and unblock logical records, seek disc records, position printer forms, etc.
- An unlimited number of symbolic labels.

The Advanced and Basic Assemblers use the same mnemonic operation codes for machine instructions and the same fixed-format coding sheet. The differences in their techniques for handling I/O operations, however, preclude direct compatibility, in either source-language or object form, between programs coded in the Advanced and Basic Assembler languages.

Burroughs states that the Advanced Assembler will use only 10,000 bytes of core memory (in addition to the 10,000 bytes required by the MCP). Thus, the Advanced Assembler can be used by systems with as little as 20,000 bytes of core memory.

Compilers

COBOL and FORTRAN compilers will be provided for use with any MCP-equipped B 2500 or B 3500 system. No detailed specifications of either the COBOL or FORTRAN language facilities to be implemented have been released to date, but Burroughs promises that both its COBOL and its FORTRAN will be compatible with the proposed A.S.A. standard versions of the two programming languages. Burroughs further states that it will be practical to run COBOL or FORTRAN compilations simultaneously with each other and with a mix of production jobs.

Problem Oriented Facilities

An Advanced Sort Generator, an Advanced Report Generator, and an Advanced Utility Program Generator will be provided. The input specifications and functional capabilities of these generators will be similar to those of their counterparts in the Basic software package. The essential difference is that the Advanced versions will generate programs in the Advanced Assembler language for execution under control of the MCP.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance* $	Purchase $
B 2500 CENTRAL SYSTEM		Central Processor			
	2501	Central Processor with 2 Type A I/O Channels, 2 Type B I/O Channels, and Standard Operator Console	$ 1,195	$ 125	$ 57,360
		Memory Modules			
	2001	10,000 Bytes Core Memory	450	20	21,600
	2002	20,000 Bytes Core Memory	900	25	43,200
	2003	30,000 Bytes Core Memory	1,325	30	63,600
	2004	40,000 Bytes Core Memory	1,725	40	82,800
	2005	50,000 Bytes Core Memory	2,100	45	100,800
	2006	60,000 Bytes Core Memory	2,450	50	117,600
		Processor Options			
	2510	Type A I/O Channel	25	5	1,200
	2511	Type B I/O Channel	50	10	2,400
	2520	Emulator for B 200/B 300	300	90	14,400
	2521	Emulator for 1401/1440/1460	300	90	14,400
	2530	Floating Point	50	7	2,400
	2540	Desk-Level Console	25	0	1,200
		Input Controls			
	2110	Card Reader	50	8	2,400
	2111	Card Reader (Type B)	50	8	2,400
	2120	Paper Tape Reader	50	8	2,400
	2130	MICR Sorter-Reader	100	12	4,800
	2131	MICR Sorter-Reader (Type B)	100	12	4,800
		Output Controls			
	2210	Card Punch	50	8	2,400
	2220	Paper Tape Punch	50	8	2,400
	2240	Printer I	75	8	3,600
	2241	Printer I (Type B)	75	8	3,600
	2243	Printer II	75	12	3,600
	2244	Lister	75	8	3,600
		Input/Output Controls			
	2340	Console Printer	75	10	3,600
	2350-1	Terminal Control for 2350-2 CTU	175	15	8,400
	2350-2	Central Terminal Unit	1,095	100	52,560
	2351	Single-Line Communications Control	125	14	6,000
	2371	Systems Memory	150	12	7,200
	2373	Disk File	200	12	9,600
	2381-1	36KB Cluster (9-Ch. — 800 bpi)	200	12	9,600
	2381-2	72KB Cluster (9-Ch. — 1600 bpi)	350	12	16,800
	2391-1	50KC (7-Ch. — 200/556 bpi)	275	12	13,200
	2391-3	72KC (7-Ch. — 200/556/800 bpi)	300	12	14,400
	2393-1	72KB (9-Ch. — 800 bpi)	325	12	15,600
	2393-2	144 (9-Ch. — 1600 bpi)	450	12	21,600
		Exchanges			
	2470	Systems Memory (1 x 2)	55	10	2,640
	2480	7-Channel Cluster (2 x 8)	175	10	8,400
	2481	9-Channel Cluster (2 x 8)	200	10	9,600
		Adapters for Controls			
	2610	BCL-BCL Code Translator for 2210 Card Punch	15	6	720
	2650	CTU Adapter for 2350-1	35	6	1,680
	2680	Convert 2381-1 to 7-Ch. Control	50	12	2,400
	2681	200 bpi Adapter for 2381-1	25	6	1,200
	2691	200 bpi Adapter for 2393-1	25	6	1,200

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance* $	Purchase $
B 2500 CENTRAL SYSTEM (Contd.)		Line Adapters for 2351 Single-Line Control			
	2651	Typewriter Inquiry Station	30	6	1,440
	2652-1	TWX/Remote Typewriter	30	6	1,440
	2652-2	TWX/Remote Typewriter with Automatic Dial Out	45	12	2,160
	2653-1	B 2500/B 3500	50	6	2,400
	2653-2	B 2500/B 3500 w/ADO	65	12	3,120
	2654	U1004	85	6	4,080
	2655-1	IBM 1050	60	6	2,880
	2655-2	IBM 1050 w/ADO	75	12	3,600
	2657	Model 35 on 8A1 Selective Calling Service	30	6	1,440
	2658-1	Digitronics D507 & D509	30	6	1,440
	2658-2	Digitronics D507 & D509 w/ADO	45	12	2,160
B 3500 CENTRAL SYSTEM		Central Processor			
	3501	Central Processor with 3 Type A I/O Channels, 3 Type B I/O Channels, and Standard Operator Console	1,695	168	81,360
		Memory Modules			
	3001	10,000 Bytes Core Memory	500	24	24,000
	3002	20,000 Bytes Core Memory	1,000	30	48,000
	3003	30,000 Bytes Core Memory	1,475	36	70,800
	3004	40,000 Bytes Core Memory	1,925	48	92,400
	3005	50,000 Bytes Core Memory	2,325	54	111,600
	3006	60,000 Bytes Core Memory	2,700	60	129,600
	3007	70,000 Bytes Core Memory	3,050	72	146,400
	3008	80,000 Bytes Core Memory	3,375	78	162,000
	3009	90,000 Bytes Core Memory	3,675	84	176,400
	3012	120,000 Bytes Core Memory	4,500	108	216,000
	3015	150,000 Bytes Core Memory	5,250	132	252,000
	3018	180,000 Bytes Core Memory	6,000	168	288,000
	3021	210,000 Bytes Core Memory	6,750	204	324,000
	3024	240,000 Bytes Core Memory	7,500	240	360,000
	3030	300,000 Bytes Core Memory	9,000	312	432,000
	3036	360,000 Bytes Core Memory	10,800	384	518,400
	3045	450,000 Bytes Core Memory	13,500	492	648,000
	3050	500,000 Bytes Core Memory	15,000	528	720,000
		Processor Options			
	3510	Type A I/O Channel	35	6	1,680
	3511	Type B I/O Channel	65	12	3,120
	3520	Emulator for B 200/B 300	300	108	14,400
	3521	Emulator for 1401/1440/1460	300	108	14,400
	3530	Floating Point	100	8	4,800
	3540	Desk-Level Console	25	0	1,200
		Input Controls			
	3110	Card Reader	50	10	2,400
	3111	Card Reader (Type B)	50	10	2,400
	3120	Paper Tape Reader	50	10	2,400
	3130	MICR Sorter-Reader	100	14	4,800
	3131	MICR Sorter-Reader (Type B)	100	14	4,800
		Output Controls			
	3210	Card Punch	50	10	2,400
	3220	Paper Tape Punch	50	10	2,400
	3240	Printer I	75	10	3,600
	3241	Printer I (Type B)	75	10	3,600
	3243	Printer II	75	14	3,600
	3244	Lister	75	10	3,600
		Input/Output Controls			
	3340	Console Printer	100	12	4,800
	3350-1	Terminal Control for 3350-2 CTU	175	18	8,400
	3350-2	Central Terminal Unit	1,095	120	52,560
	3351	Single-Line Communications Control	125	17	6,000
	3353	Multi-Line Communications Control	400	36	19,200
	3371	Systems Memory	150	14	7,200
	3373	Disk File	250	14	12,000
	3381-1	36KB Cluster (9-Ch. — 800 bpi)	235	14	11,280
	3381-2	72KB Cluster (9-Ch. — 1600 bpi)	395	14	18,960
	3391-1	50KC (7-Ch. — 200/556 bpi)	275	14	13,200
	3391-3	72KC (7-Ch. — 200/556/800 bpi)	300	14	14,400
	3393-1	72KB (9-Ch. — 800 bpi)	375	14	18,000
	3393-2	144KB (9-Ch. — 1600 bpi)	475	14	22,800

(Contd.)

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance* $	Purchase $
B 3500 CENTRAL SYSTEM (Contd.)		Exchanges			
	3470	Systems Memory (1 x 2)	$ 85	$ 12	$ 4,080
	3471-1	Disk File (1 x 5)	175	12	8,400
	3471-2	Disk File (2 x 5)	250	12	12,000
	3471-4	Disk File (4 x 10)	400	12	19,200
	3480	7-Channel Cluster (2 x 8)	175	12	8,400
	3481	9-Channel Cluster (2 x 8)	200	12	9,600
	3490	7-Ch. Mag. Tape I (2 x 10)	250	12	12,000
	3491	7- or 9-Ch. Mag. Tape II (2 x 10)	250	12	12,000
		Control Adapters			
	3610	BCL-BCL Code Translator for 3210 Card Punch	15	6	720
	3650-1	CTU Adapter for 3350-1 (first)	35	6	1,680
	3650-2	Additional CTU Adapter for 3350-1 (9 max.)	30	6	1,440
	3680	Convert 3381-1 to 7-Ch. Control	50	12	2,400
	3681	200 bpi Adapter for 3381-1	25	6	1,200
	3691	200 bpi Adapter for 3393-1	25	6	1,200
		Line Adapters for 3351 and 3353 Controls			
	3651	Typewriter Inquiry Station	30	6	1,440
	3652-1	TWX/Remote Typewriter	30	6	1,440
	3652-2	TWX/Remote Typewriter with Automatic Dial Out	45	12	2,160
	3653-1	B 2500/B 3500	50	6	2,400
	3653-2	B 2500/B 3500 w/ADO	65	12	3,120
	3654	U1004	85	6	4,100
	3655-1	IBM 1050	60	6	2,880
	3655-2	IBM 1050 w/ADO	75	12	3,600
	3657	Model 35 on 8A1 Selective Calling Service	30	6	1,440
	3658-1	Digitronics D507 and D509	30	6	1,440
	3658-2	Digitronics D507 and D509 w/ADO	45	12	2,160
INPUT DEVICES		Card Readers			
	9110	200 CPM Reader	175	48	8,400
	9111	800 CPM Reader	325	100	16,250
	9112	1400 CPM Reader	450	151	21,600
	9918	Postal Money Order Feature	20	6	1,000
	9919	40-Column Read Switch	0	0	0
		Paper Tape Reader			
	9120	500-1000 CPS Reader	300	84	16,000
	9926	Input Code Translator	145	12	6,960
		MICR Sorter-Readers			
	9130	13-Pkt. Non-System (1565 DPM)	1,890	600	90,720
	9131	13-Pkt. w/o Endorser (1565 DPM)	1,900	600	91,200
	9132	16-Pkt. w/o Endorser (1565 DPM)	2,200	738	105,600
	9932	Endorser (9131 & 9132 only)	200	60	9,600
	9933	Extended Sort Control (9130 & 9131 only)	50	18	2,400
	9934	Start/Stop Bar (9130 & 9131 only)	5	0	240
	9935	Special Field Ending	10	0	480
	9936	Override Code	10	0	480
	9937	Validity Checking	10	0	480
	9938	Reverse Override	10	0	480
	9939	Non-Resettable Counter	0	0	0
OUTPUT DEVICES		Card Punches			
	9210	100 CPM Punch	350	78	18,425
	9211	300 CPM Punch	515	210	25,750
		Paper Tape Punch			
	9220	100 CPS Punch	260	78	15,300
	9928	Output Code Translator	130	12	6,850
		Printers			
	9240	700 LPM, 120 P.P.	800	210	45,000
	9241	1040 LPM (37 Char.), 120 P.P.	900	220	50,500
	9242	815 LPM, 120 P.P.	850	216	48,000
	9243	1040 LPM (46 Char.), 120 P.P.	950	240	53,500
	9940	High Speed Slew (9242 & 9243 only)	60	24	3,000
	9941	Additional 12 Print Positions	40	12	2,000
	9947	Dual Printer Control (9240 & 9241 only)	200	12	9,600
	9949	Powered Forms Stacker	15	6	750
		Listers			
	9244-1	1565 LPM Master A/N Lister	1,350	390	67,500
	9244-2	1565 LPM Slave A/N Lister (2 max.)	650	240	32,500

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance* $	Purchase $
INPUT-OUTPUT DEVICES		Typewriter			
	9340	Console Printer and Keyboard	$ 55	$ 14	$ 2,640
		Data Communication Remote Devices			
	9350	Typewriter Inquiry Station	55	12	2,640
		Disk File Devices			
	9370-1	Systems Memory — 1 million bytes	375	96	18,000
	9370-2	Systems Memory — 2 million bytes	450	108	21,600
	9371	Disk File Electronics Unit	650	96	31,200
	9372-1	10 million bytes (1 Module)	850	145	44,000
	9372-2	20 million bytes (2 Modules)	1,650	258	85,800
	9372-3	30 million bytes (3 Modules)	2,400	378	124,800
	9372-4	40 million bytes (4 Modules)	3,100	498	161,200
	9372-5	50 million bytes (5 Modules)	3,775	618	196,300
	9372-6	Additional 10-million-byte Increments	675	120	35,100
		Magnetic Tape Units			
	9381-2	2-Station 36KB Cluster (9-Ch. — 800 bpi)	900	220	43,200
	9381-3	3-Station 36KB Cluster (9-Ch. — 800 bpi)	1,100	276	52,800
	9381-4	4-Station 36KB Cluster (9-Ch. — 800 bpi)	1,300	312	62,400
	9382-2	2-Station 72KB Cluster (9-Ch. — 1600 bpi)	1,100	270	52,800
	9382-3	3-Station 72KB Cluster (9-Ch. — 1600 bpi)	1,400	312	67,200
	9382-4	4-Station 72KB Cluster (9-Ch. — 1600 bpi)	1,700	354	81,600
	9390	18/50KC (7-Ch. — 200/556 bpi)	480	174	23,000
	9391	18/50/72KC (7-Ch. — 200/556/800 bpi)	575	198	27,600
	9392	72KB (9-Ch. — 800 bpi)	575	198	27,600
	9393	144KB (9-Ch. — 1600 bpi)	650	210	31,200
	9989	9/25/36KC 7-Ch. Station Adapter for 9381 & 9382	50	12	2,400

* "Metro" maintenance rates, roughly 20% lower than the indicated basic rates, are available in certain localities for maintenance of purchased equipment.

CDC 1604

Control Data Corporation

STANDARD EDP REPORTS

AUERBACH ®

AUERBACH INFO, INC.

PRINTED IN U. S. A.

CDC 1604

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SUMMARY REPORT: CONTROL DATA 1604

.1 AVAILABILITY

The Control Data 1604 is a medium-to-large-scale data processing system that is primarily oriented toward scientific and engineering applications which require extensive computation and a fairly large amount of internal storage. The 1604 was Control Data's first general-purpose digital computer system. Introduced as a solid-state contender for the phase of the computer market that was then dominated by the IBM 704, the 1604 was initially delivered in January 1960, two months after the IBM 7090.

Manufacture of the 1604 was phased out during 1962, when it was superseded by an improved model designated the 1604-A. The 1604-A features a more powerful interrupt system and the ability to handle higher input-output data rates with lower central processor delays. These refinements are described in Section 243:011 of the CDC 1604-A report.

A total of approximately sixty 1604 and 1604-A systems were manufactured before production facilities were shifted over to Control Data's newer 3000 Series systems in 1964. Used 1604 and 1604-A systems can be purchased or rented from Control Data Corporation, and Control Data assures prospective users that it will continue to provide full hardware maintenance and software support services. No inventory of used 1604 systems is maintained; they are offered on an "as available" basis, and a turnaround time of about three months is required to refurbish each returned system.

.2 HARDWARE

A Control Data 1604 system can contain 8,192, 16,384, or 32,768 word locations of core storage. Each 48-bit word can hold a fixed-point or floating-point number, a binary data pattern, or two 24-bit instructions. The core storage is divided into two banks, each with independent access facilities and a 6.4-microsecond cycle time. The resulting capability to overlap core storage accesses leads to an effective cycle time of approximately 4.8 microseconds. No parity checking is performed on data transferred to or from core storage.

The 1604 Central Processor operates in the binary mode on 48-bit operands in either fixed-point or floating-point form. Floating-point data values are represented by an 11-bit exponent and a 36-bit-plus-sign fraction. A useful repertoire of arithmetic, logical, branching, storage search, and data transfer operations is provided, but there are no direct facilities for radix conversion, format control, or multi-word data transfers. Instructions are executed at the rate of about 50,000 per second in typical scientific applications.

Each instruction consists of 24 bits: a 6-bit operation code, a 3-bit index designator, and a 15-bit address portion. The index designator can specify either indexing, using one of six index registers, or indirect addressing, which may be recursive. The address portion can specify an operand address in core storage, a literal operand, or a shift count.

The fact that each 48-bit word holds a pair of instructions causes some programming complications which necessitate careful "housekeeping" when coding in assembly language. All transfers of control (jumps) must be to the first instruction of a pair, and certain instructions behave differently depending upon which half of a word they occupy.

An interrupt system permits interruption of the program when an input-output controller becomes ready, when an arithmetic overflow occurs, or when the real-time clock overflows. The programmer can specify which controllers and channels shall be allowed to generate interrupt signals; but when an interrupt occurs, programmed testing is required to identify the specific condition that caused it. The 1604's unsophisticated interrupt system and lack of facilities for inter-program protection make it unsuitable for multiprogrammed operation.

The 1604 contains three pairs of buffered data channels for conventional input-output operations. Each pair consists of one input channel and one output channel. Logically, up to eight controllers can be connected to each pair of channels, and some of the controllers can, in turn, accommodate up to eight I/O devices. Power supply considerations, however, impose lower practical limits on certain configuration combinations. A seventh data channel, which is unbuffered and requires continuous Central Processor control, is intended primarily for computer-to-computer communications.

.2 HARDWARE (Contd.)

Up to three input and three output operations can occur simultaneously provided that none of them has a peak speed of over 30,000 characters per second. Each one-word data transfer between core storage and a peripheral device requires about 14.8 microseconds of Central Processor time, and the 1604's I/O control method imposes severe restrictions upon the number of high-speed I/O operations that can take place simultaneously. For example, two 62,500-character-per-second magnetic tape units can be serviced simultaneously only if no other I/O operation is attempted on any of the other channels while the two tape units are operating.

The principal peripheral devices used with Control Data 1604 systems are as follows:

- A 350-character-per-second paper tape reader and a 110-character-per-second paper tape punch, both of which are mounted in the 1604 console desk along with a console typewriter.
- 1607 Magnetic Tape Subsystem, consisting of a Synchronizer Control Unit and up to four Ampex tape units in a single cabinet. Peak speed is 30,000 characters per second, using IBM 729-compatible tape recorded at 200 rows per inch in either BCD or binary mode.
- 1609 Card Reader/Punch, a Control Data adaptation of the IBM 521 Punching Unit, which can read and/or punch up to 100 cards per minute.
- 1617 Card Reader, which reads 80-column cards column by column at 250 cards per minute.
- 1612 Line Printer, a Control Data adaptation of an Anelex Series 4-1000 printer rated at either 1,000 or (for improved print quality) 667 lines per minute.
- 1608 Control Unit, which controls up to eight IBM 729 II or 729 IV Magnetic Tape Units at data transfer rates of 15,000 to 62,500 characters per second.
- 1610-A Control Unit for one 100-cpm IBM 532 Card Punch and/or one IBM 88 Collator used as a card reader at 650 cpm (one feed) or 1,300 cpm (both feeds).

Controllers for other IBM card readers, punches, printers, and magnetic tape units were formerly offered for the 1604, and provisions can probably be made for connecting some of the more recent Control Data peripheral devices used in CDC 1604-A systems (Report 243:).

.3 SOFTWARE

Although Control Data Corporation did not originally offer software support for its computers, it soon decided to do so, and for the past five years it has been seriously engaged in providing standard software. An impressive variety of programming systems, applications programs, and subroutines developed by both Control Data and 1604 users is now available. The software facilities that are properly documented and in general use are supplied through a well-organized, CDC-supported users' group called CO-OP.

Software facilities currently available for the 1604 and 1604-A include the CO-OP Monitor, the CODAP-1 Assembler, three FORTRAN compilers, a COBOL compiler, an ALGOL compiler, a JOVIAL compiler, a sort/merge routine, a PERT routine, a linear programming package, and many mathematical and scientific routines.

The CO-OP Monitor is an operating system that provides run-to-run supervision and conveniently integrates program translation, debugging, and execution functions. CODAP-1 is the basic symbolic assembly language for the 1604. The three versions of FORTRAN that have been implemented for the 1604 are FORTRAN-60, a compiler designed for the rapid compile-and-execute operation using a restricted version of the FORTRAN II language; FORTRAN-62, which compiles more efficient object programs and can incorporate independently-compiled subprograms; and FORTRAN-63, which offers most of the language facilities of FORTRAN IV.

PRICE DATA: CONTROL DATA 1604

The following prices are the list purchase, single-shift rental, and single-shift maintenance prices currently in effect for Control Data 1604 equipment. In general, they are the same as the prices that were in effect while the 1604 system was in production. It is likely that this equipment can now be obtained at lower prices.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR	1604	Central Processor with:			
		8,192 words of core storage	22,500	1,775	750,000
		16,384 words of core storage	25,000	1,970	830,000
		32,768 words of core storage	30,100	2,360	990,000
		Price includes console, paper tape reader and punch, typewriter, and motor/generator			
STORAGE		Included in Central Processor price			
INPUT-OUTPUT	1607	Magnetic Tape Subsystem (Synchronizer plus 4 tape units)	5,050	750	145,000
	1608	Control Unit for up to 8 IBM 729 II or 729 IV Magnetic Tape Units	2,050	100	70,000
	1609	Card Reader/Punch	1,175	190	47,000
	1610-A	Control Unit for IBM 523 Card Punch and/or IBM 88 Collator	1,500	180	57,000
	1612	Line Printer	1,840	400	73,500
	1617	Card Reader	580	155	22,500

CDC 160

Control Data Corporation

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CDC 160

Control Data Corporation

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SUMMARY REPORT: CONTROL DATA 160

.1 AVAILABILITY

The Control Data 160 is a desk-size, solid-state computer designed primarily for small-scale scientific applications. Because a 160 system can include magnetic tape units, line printers, and punched card equipment, it is also suitable for use with larger computers as an off-line data transcription system or as a directly-connected satellite computer.

Initial deliveries of Control Data 160 systems were made in May 1960. Deliveries of the Control Data 160-A, a more powerful and more expensive version of the 160, began in July 1961. The 160-A features larger core storage capacities and a buffered input-output channel; it is fully described in Computer System Report 244. Programs written for a 160 system can be executed on a similarly-equipped 160-A, but modifications will be required if the user wishes to take advantage of the 160-A's increased storage capacity and simultaneity. Programs written for a 160-A system cannot, in general, be executed on a 160 without modification.

A total of more than 400 Control Data 160 and 160-A computers were manufactured. Both the 160 and 160-A are no longer in production, but used systems can be purchased or rented from Control Data Corporation on an "as available" basis. Control Data assures prospective users that it will continue to provide full hardware maintenance and software support services.

Two other computer systems whose design is closely patterned after that of the 160 are currently being produced by Control Data. The 160-G, initially delivered in March 1964, offers larger and faster core storage (from 8K to 131K words with a 1.5-microsecond cycle time) and a larger word size (14 bits), but it can be operated in a compatibility mode that enables it to execute 160-A programs without alteration. The 8090 Control Computer uses a central processor that is program-compatible with the 160-A, but the 8090 is designed primarily for communications and control applications. The 8090 is the central component of several message-switching systems installed by Control Data.

.2 HARDWARE

The basic Control Data 160 system consists of the desk-size central processor, 4,096 twelve-bit words of core storage, and a built-in 350-character-per-second paper tape reader and 110-character-per-second paper tape punch. Core storage cycle time is 6.4 microseconds, and no expansion of the basic 4,096-word capacity is possible. (A 160-A system can have from 8,192 to 32,768 words.) No parity checking is performed on data transferred to or from core storage.

The short word length of 12 bits (11 data bits plus sign bit) provides a precision of only 3.3 decimal digits and leads to numerous programming complexities. Arithmetic of double, triple, or quadruple precision will need to be performed to obtain the precision required for many scientific applications. The single-address instructions are one or two words in length, and there are seven different addressing modes. In general, instructions that reference operands in core storage are two words long, but a single word can hold an instruction that references a location within 64 locations of the present setting of the instruction counter. Limited facilities are provided for indexing (using a single index register) and for indirect addressing (non-recursive).

The 160 has an instruction repertoire of 97 instructions, most of which are variations of a few basic instructions. The basic arithmetic mode is fixed-point binary on single-word operands. There are add-to-storage and Boolean instructions, but no standard facilities are provided for multiplication, division, direct comparisons, radix conversions, or floating-point arithmetic. In the basic 160 system, these functions are usually performed by standard subroutines. The optional 168-1 Auxiliary Arithmetic Unit provides automatic facilities for double-precision addition and subtraction and for single-precision multiplication and division, all in fixed-point mode. The 168-2 Auxiliary Arithmetic Unit speeds the execution of floating-point arithmetic operations.

Although the basic 11-bit add time is only 19.2 microseconds, double-precision addition takes 225 microseconds using subroutines and 145 microseconds using the 168-1 Arithmetic Unit. Floating-point add times are about 4,000 microseconds using subroutines and 1,000 microseconds using the 168-2 Arithmetic Unit.

.2 HARDWARE (Contd.)

Simultaneous operations cannot be performed in Control Data 160 systems; the central processor is interlocked during all input-output operations. There is no interrupt system.

The principal input-output devices used with Control Data 160 systems are the built-in tape reader and punch and the following optional units:

- An on-line typewriter, which provides the typewriter input-output facilities that are lacking in the basic 160 system.
- A card reader, rated at either 250 or 1,200 cards per minute.
- A card punch, rated at either 100 or 200 cards per minute; the slower model is an IBM 523.
- A line printer with a rated speed of either 150 or 1,000 lines per minute.
- Up to four magnetic tape units. Either the 163 Magnetic Tape Subsystem or the newer 603 Magnetic Tape Units can be connected. Both use IBM 729-compatible tape in either BCD or binary mode. The 163 subsystem consists of one to four tape handlers and a control unit; its peak speed is 30,000 characters per second at a recording density of 200 rows per inch. The 603 has peak speeds of 15,000 or 41,667 characters per second at recording densities of 200 and 556 rows per inch, respectively.

A 160 computer can be connected on-line to a larger Control Data 1604, 1604-A, or 3000 Series computer. Data can be transferred between the coupled systems by direct core-to-core transfers or by way of shared magnetic tape units.

.3 SOFTWARE

Because of the Control Data 160's short word length and machine-language programming complexity, the software available for the system is of particular importance. A useful assortment of programming systems and subroutines, developed by Control Data and by 160 users, is now available, although many significant programs that have been developed for the 160-A cannot be run on 160 systems. The software facilities that are properly documented and in general use are supplied through a well-organized, CDC-supported users' group called SWAP.

OSAS is the basic symbolic assembly system for the 160 and 160-A. It provides no facilities for macro-instructions, but library subroutines can be assembled along with the user's source programs. Only about 250 symbolic labels can be accommodated by the OSAS translator for the 160. The translator is available in different versions for systems that use paper tape, magnetic tape, or punched card input-output.

A compiler is available for 160 FORTRAN, a restricted but useful version of the FORTRAN II language. The restrictions are imposed mainly by the hardware limitations of the 160 itself. Fixed-point arithmetic is limited to single precision (11 bits), while each floating-point variable occupies three words of core storage. Mixed-mode arithmetic is permitted. Object programs compiled by 160 FORTRAN are executed interpretively.

INTERFOR is a floating-point interpretive system for the 160. Its repertoire of 22 instructions is a subset of the larger Control Data 1604's machine-language instruction repertoire; thus, INTERFOR makes it easy for 1604 programmers to write programs that can be executed interpretively on a 160. Each floating-point data value occupies four words of 160 storage. Standard INTERFOR subroutines handle input, output, and mathematical functions. INTERFOR programs can be written directly in octal format, or they can be written in a more convenient symbolic format and assembled by FLAP, a special-purpose assembler.

Among the library subroutines available for the 160 are routines to perform single-precision multiplication and division, multiple-precision fixed-point arithmetic, decimal arithmetic, floating-point arithmetic, mathematical functions, radix conversions, matrix inversion, and data transcriptions (card-to-tape and tape-to-printer).

PRICE DATA: CONTROL DATA 160

The following prices are the list purchase, single-shift rental, and single-shift maintenance prices currently in effect for Control Data 160 equipment. In general, they are the same as the prices that were in effect while the 160 system was in production. It is likely that this equipment can now be obtained at lower prices.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR	160	Computer, including 4,096 words of core storage and paper tape reader and punch	1,500	200	60,000
	168-1	Auxiliary Arithmetic Unit (fixed point)	390	125	11,700
	168-2	Auxiliary Arithmetic Unit (floating point)	450	130	13,500
STORAGE		Included in basic Computer, above			
INPUT-OUTPUT	161	On-Line Input-Output Typewriter	262	95	10,500
	167-1	Card Reader (250 cpm)	400	140	15,700
	405	Card Reader (1200 cpm)	400	65	22,500
	177	Card Reader Controller (for 405)	100	10	4,800
	415	Card Punch (200 cpm)	295	60	18,150
	523	IBM Card Punch (100 cpm)	121	?	5,100
	170	Card Punch Controller (for 415 or 523)	335	55	13,700
	166-1	Line Printer (150 lpm)	595	275	25,000
	1612	Line Printer (1000 lpm)	1,840	400	73,500
	603	Magnetic Tape Unit	550	120	24,000
	162-1	Tape Synchronizer (for 1 to 4 603's)	500	105	20,000
		Magnetic Tape Subsystem:			
	163-1	One tape handler and control	970	235	38,800
	163-2	Two tape handlers and control	1,482	400	59,300
	163-3	Three tape handlers and control	1,994	565	79,800
	163-4	Four tape handlers and control	2,506	730	100,300
	165-1	Incremental Plotter	210	80	7,000

CONTENTS

CONTENTS (Contd.)

INTRODUCTION

§ 011.

The CDC 1604-A is a medium- to large-scale data processing system. It is primarily oriented towards scientific, simulation, or control applications in which extensive computation and a large, rapid-access store are required. Because punched tape and card handling speeds are relatively low, the 1604-A is most effective as a magnetic tape oriented system when input-output volumes are high. Facilities have been incorporated to enable direct connection of CDC 160 and 1604-A systems via a magnetic tape controller.

The 1604-A replaces the discontinued 1604. The differences between them are listed at the end of this Introduction. Only one of the differences, the interrupt facilities, requires alterations to programs but a "1604 Compatibility" switch is incorporated which forces a 1604-A to operate 1604 programs correctly.

The 1604-A has a core store of 8,192, 16,384 or 32,768 words. The store is divided into two banks with independent access facilities, giving an effective cycle time of approximately 4.8 microseconds. Each 48-bit word can hold a fixed or floating point number, a binary data pattern, or two instructions. Input and output data can be in a variety of codes and formats; e.g., one 6-bit character per word, binary images in 40-bit patterns, or 8 BCD 6-bit characters in a word.

The central processor operates in binary on fixed and floating point operands. A large variety of computation operations are available, but none for radix conversion or format control. Both indexing and indirect addressing features are incorporated. Approximately 50,000 or 100,000 instructions can be executed per second in floating point or fixed point mode, respectively.

An interrupt feature is provided which enables a master routine to control input-output transfers and overlapping. It is seldom practical, however, to multi-run independent programs. Individual, flexible control of interruptions is provided by selecting each condition which is to be allowed to interrupt.

The computer contains three pairs of channels for conventional input-output operations. Each pair contains one input and one output buffer. Therefore, up to three input and three output transfers can be occurring simultaneously. There are presently no limitations on the number of simultaneous input-output transfers at high tape speeds. An additional input-output channel, which is unbuffered, is available for special transfers; e.g., to another computer.

Up to eight controllers and/or units can be connected to each pair of buffered channels. Controllers may have several units attached to them; the arrangements are flexible and vary for individual devices.

The input-output units used in the 1604-A system include:

- CDC Card Reader
- CDC Punched Paper Tape Reader
- CDC Line Printer
- CDC Magnetic Tape System
- IBM Card Readers and Punches
- IBM Line Printers
- IBM/Soroban Typewriter

No special software has yet been developed for the CDC 1604-A. However, the programs used on the CDC 1604 are available. A number of programming systems including FORTRAN compilers have been developed by CDC and by 1604 users. The languages and

INTRODUCTION–Contd.

§ 011.

routines that are properly documented and in general use are supplied through CO-OP, the CDC 1604 and 1604-A Users' Group, which is supported by CDC. The 48-bit word length is naturally used in these compilers, which therefore produces routines that have greater precision than ones running on machines with shorter word-lengths.

There are two versions of the machine code assembler, one for independent programs and the other for programs to fit into the CO-OP Monitor System. The monitor system is a run-to-run supervisor providing a useful integration of translation, debugging, and running facilities.

The current contents of the CO-OP library are not all mutually consistent, due mainly to the independent development of individual installations. However, some general compatibility within the CO-OP Monitor System may be developing.

With the exception of 1604 JOVIAL, which is covered in the CDC 1604 Report, all software developed for the CDC 1604 or 1604-A systems is physically located in this Report.

Differences Between The CDC 1604 And The CDC 1604-A

- The 1604-A can use its input-output channels without restrictions, provided that no one unit is operating at greater than 125,000 characters per second. The corresponding 1604 limit is 30,000 characters per second.
- The 1604-A causes central processor delay of 3.2 microseconds per word transmitted between the core store and the input-output units. The corresponding 1604 delay was 14.8 microseconds.
- The 1604-A interrupts jump to nine different locations, depending on the source of the interrupt condition. The CDC 1604 interrupts jump to a common location.
- The 1604-A can temporarily inhibit interrupt requests from being recognized in ordinary programs. The 1604 is forced either to allow interrupts to take place or to prevent them altogether, except while the interrupt routine is being processed.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	48 bits	basic addressable unit; contains data item or two instructions.
Character:	6 bits	magnetic tape, typewriter, paper tape units.
Line:	up to 120 chars	printer unit.
Block:	1 to N words	magnetic tapes.

.2 DATA FORMATS

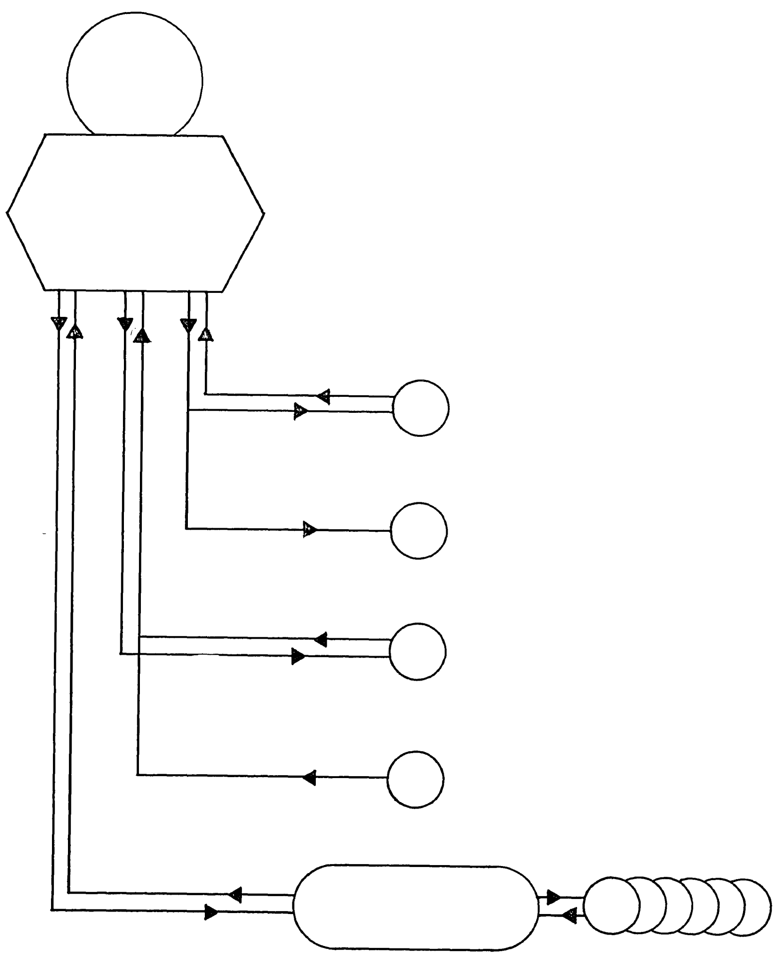
Type of Information	Representation
Binary:	48 bits in a word.
Instruction:	2 instructions/word.
Fixed point:	47 bits plus 1 sign bit.
Floating point:	36 bits plus sign bit for fixed point part; 11 bits for exponent; excess 2000_8 if positive, excess 1777_8 if negative.
Card row:	2 40-bit groups, stored in the lower 40 bits of successive 48-bit word locations.
Card image:	12 card rows (24 40-bit words).

SYSTEM CONFIGURATION

§ 031.

.1 INTEGRATED 6-TAPE BUSINESS/SCIENTIFIC SYSTEM (CONFIGURATION VI A)

Deviations from Standard Configuration: . . . . 1 additional magnetic tape transfer while computing.
faster printing (1,000 instead of 500 lines/min).
slower card reading (250 instead of 500 cards/min).
3 additional input/output transfers while computing.
3 extra index registers.
paper tape input-output.



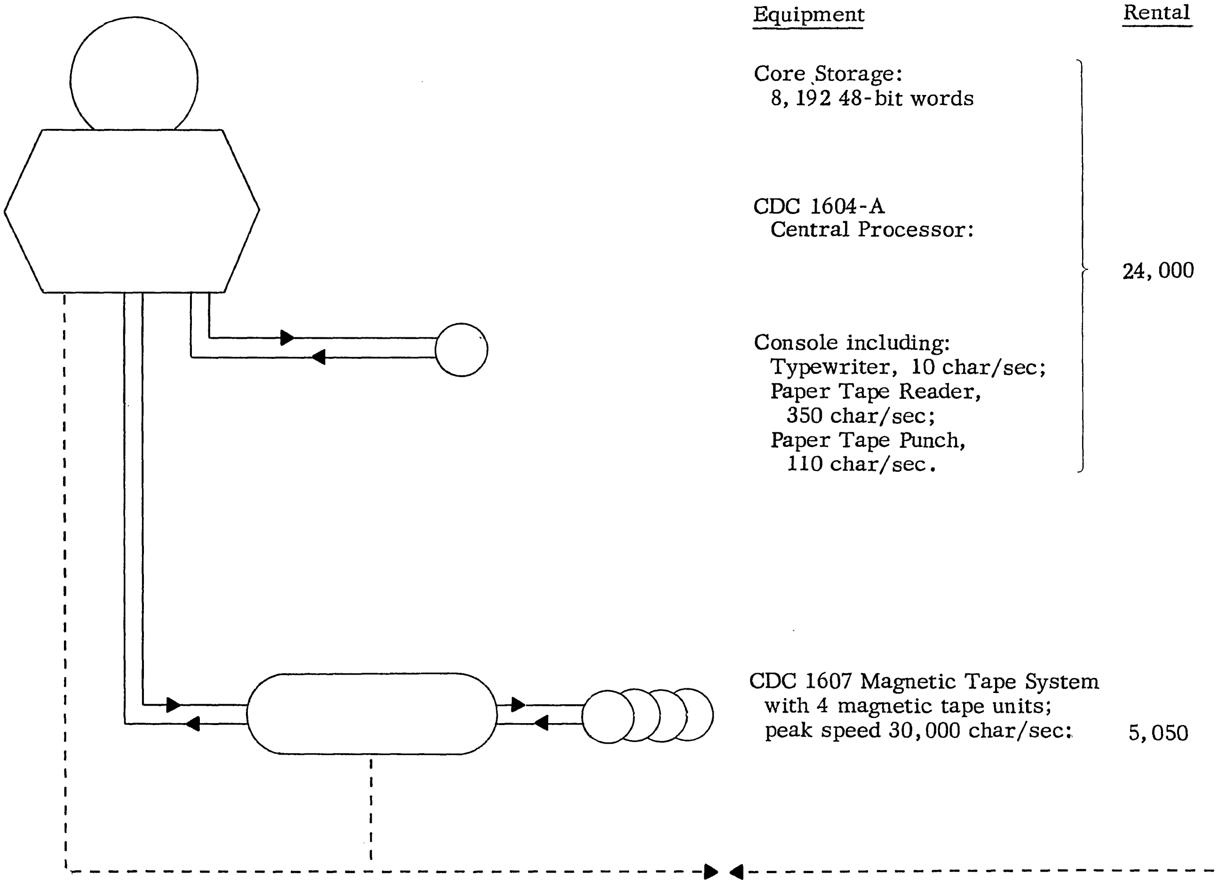
Equipment	Rental
Core Storage: 8,192 48-bit words.	
CDC 1604-A Central Processor:	24,000
Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	
CDC 1612 Printer: 1,000 lines/minute	1,840
CDC 1609 Card Reader/Punch: 100 cards/minute.	1,175
CDC 1617 Card Reader: 250 cards/minute	580
CDC 1615 Magnetic Tape System with 6 CDC 606 Magnetic Tape Units; peak speed 83,400 char/sec:	6,930
TOTAL	$34,525

§ 031.

.2 PAIRED 6-TAPE BUSINESS/SCIENTIFIC SYSTEM (CONFIGURATION VI B)

Main Computer

Deviations from Standard Configuration: . . . . direct connection to auxiliary computer.
1 additional magnetic tape transfer while computing.
1 additional input/output transfer while computing.
3 extra index registers.



To Auxiliary Computer

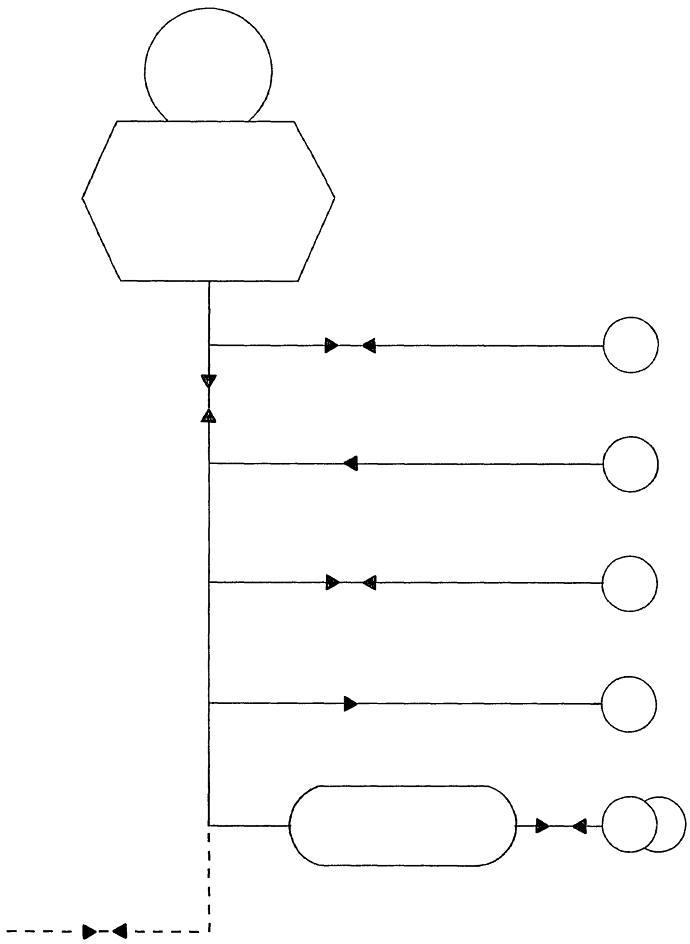
Equipment	Rental
Core Storage: 8,192 48-bit words; CDC 1604-A Central Processor; Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	24,000
CDC 1607 Magnetic Tape System with 4 magnetic tape units; peak speed 30,000 char/sec:	5,050
Total	$29,050

TOTAL, including both computers: $35,107

§ 031.

Auxiliary Computer

Deviations from Standard Configurations: . . . . direct connection to main computer or its magnetic tape unit.
6,800 12-bit words extra storage.
faster printing (1,000 instead of 500 cards/min.)
slower card-reading (250 instead of 500 cards/min.)
multiply/divide included.
typewriter output.
paper tape input and output.



To Main Computer

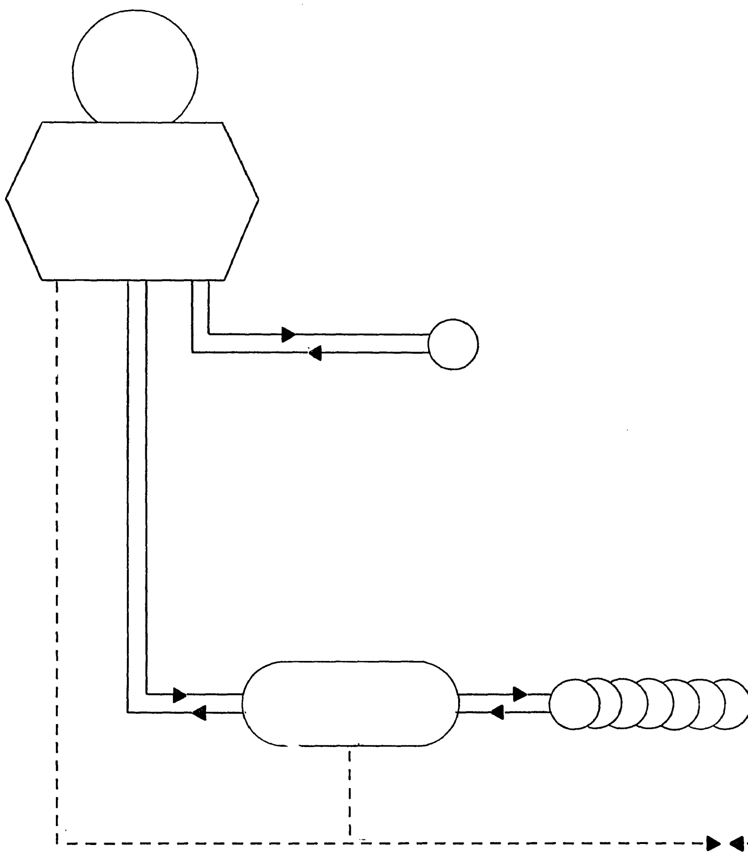
Equipment	Rental
Core Storage: 8,192 12-bit words	
CDC 160 Computer Central Processor:	1,500
Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	
CDC 167 Card Reader: 250 cards/minute	400
CDC 1609 Card Read/Punch Unit: 100 cards/minute	1,175
CDC 1612 Line Printer: 1000 lines/minute	1,500
CDC 163-2 Magnetic Tape Unit with 2 tape units; peak speed 30,000 char/sec:	1,482
Total	$6,057

§ 031.

.3 PAIRED 10-TAPE GENERAL SYSTEM (CONFIGURATION VII B)

Main Computer

Deviations from Standard Configuration: . . . . direct connection to auxiliary computer. tape units 40 percent faster.



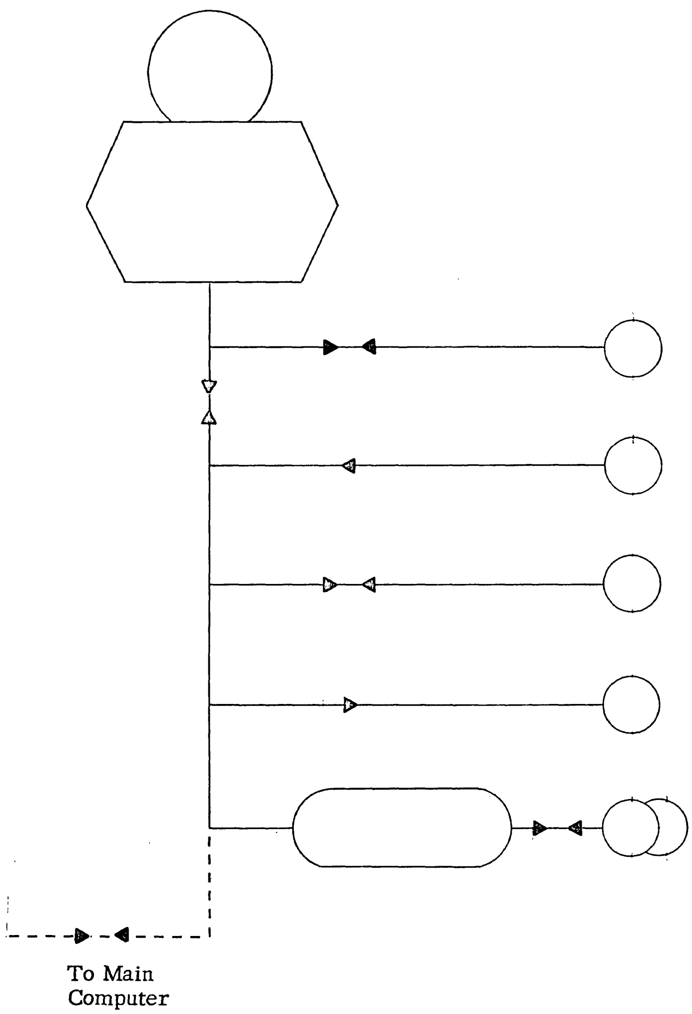
Equipment	Rental
Core Storage: 8, 192 48-bit words CDC 1604-A Central Processor: Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	24, 000
CDC 1615 Magnetic Tape System, with 8 CDC 606 tape units; peak speed 83, 400 char/sec:	1, 980 6, 600
TOTAL	$32, 580

TOTAL, including both computers: $38, 637

§ 031.

Auxiliary Computer

Deviations from Standard Configurations: . . . . direct connection to main computer or its magnetic tape unit.
6,800 12-bit words extra storage.
faster printing (1,000 instead of 500 lines/min.)
slower card reading (250 instead of 500 cards/min.)
multiply/divide included.
typewriter output.
paper tape input and output.



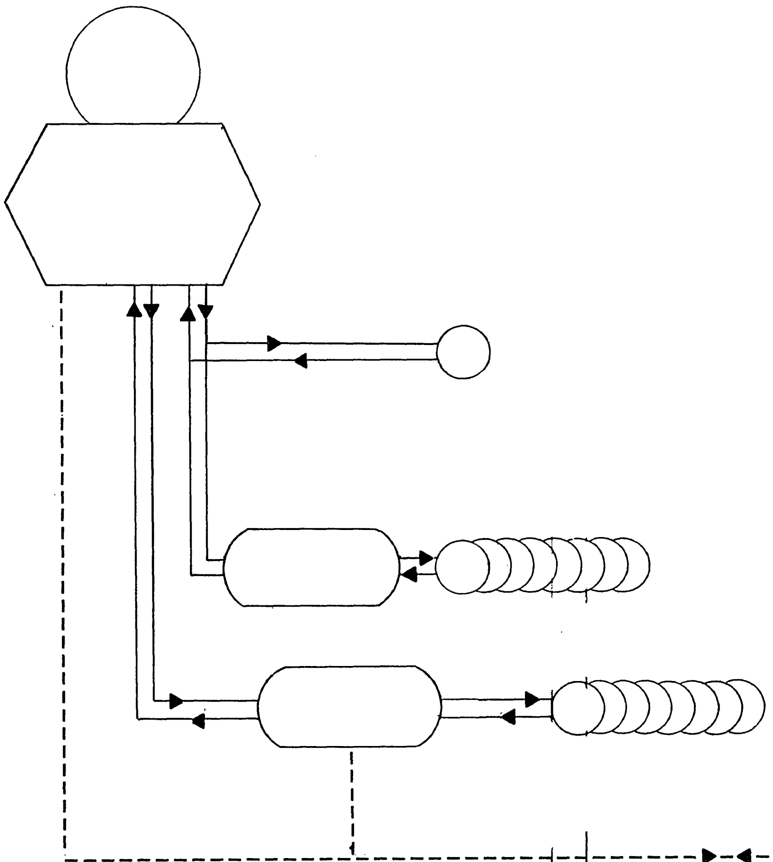
Equipment	Rental
Core Storage: 8,192 12-bit words CDC 160 Central Processor: Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	1,500
CDC 167 Card Reader: 250 cards/minute	400
CDC 1609 Card Read/Punch Unit: 100 cards/minute	1,175
CDC 1612 Line Printer: 1000 lines/minute	1,500
CDC 163-2 Magnetic Tape Unit with 2 tape units: peak speed 30,000 char/sec:	1,482
Total	$6,057

§ 031.

.4 PAIRED 20-TAPE GENERAL SYSTEM (CONFIGURATION VIII B)

Main Computer

Deviations from Standard Configuration: . . . . direct connection to auxiliary computer 4,000 48-bit words extra storage. tape units 30 percent slower.

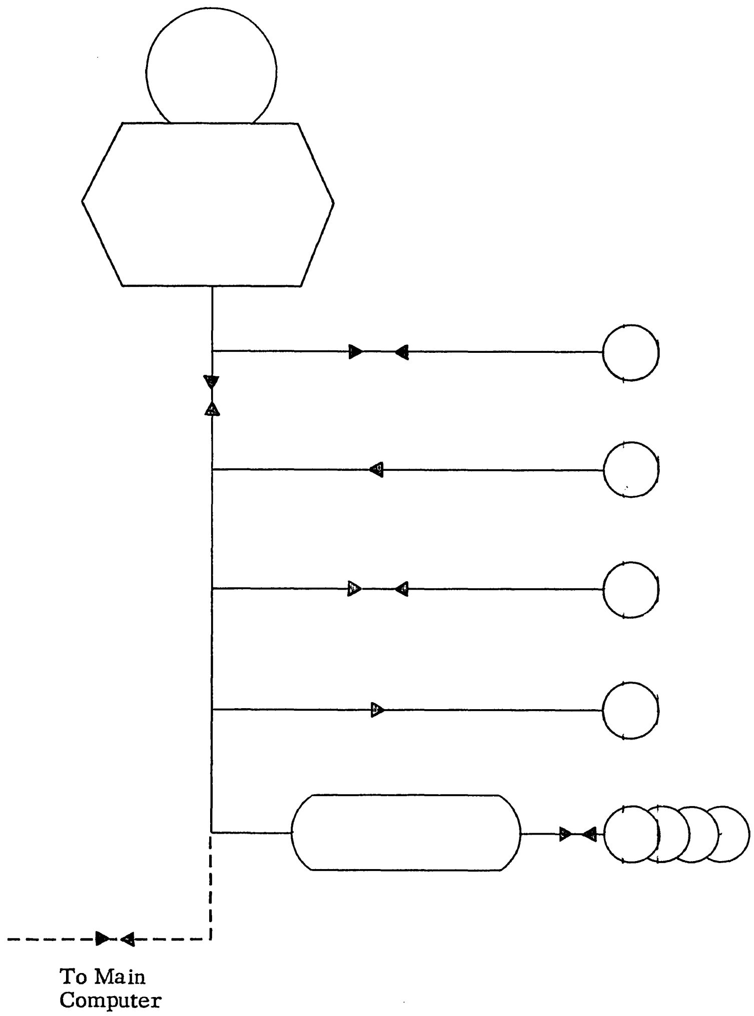


Equipment	Rental
Core Storage: 16,384 48-bit words; CDC 1604-A Central Processor:; Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	$26,500
2 CDC 1615 Magnetic Tape Systems, each with 8 CDC 606 tape units; peak speed 83,600 char/sec:	3,960 13,200
TOTAL	$43,660
TOTAL, including both computers:	$54,265

§ 031.

Auxiliary Computer

Deviations from Standard Configurations: . . . . direct connection to main computer or its magnetic tape unit.
6,800 12-bit words extra storage.
faster printing (1,000 instead of 500 lines/min.)
slower card-reading (250 instead of 500 cards/min.)
multiply/divide included.
typewriter output.
paper tape input and output.



Equipment	Rental
Core Storage: 8,192 12-bit words CDC 160-A Central Processor: Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 Char/sec; Paper Tape Punch, 110 char/sec.	$2,250
CDC 167 Card Reader: 250 cards/minute	400
CDC 1609 Card Read/Punch Unit: 100 cards/minute	1,175
CDC 1612 Line Printer: 1000 lines/minute	1,500
CDC 1615 Magnetic Tape System with 4 tape units; peak speed 82,300 char/sec:	1,980 3,300
Total	$10,605

INTERNAL STORAGE: CORE STORAGE

§ 041.

.1 GENERAL

.11 Identity: . . . . Core Storage.

.12 Basic Use: . . . . . . working storage.

.13 Description

Core Storage is housed in the central processor cabinet and has a capacity for 8,192; 16,384; or 32,768 bit words. The storage section is divided into two independent stores or "word banks"; each store has equal capacity and a storage cycle of 6.4 microseconds. Both stores operate independently, thus permitting overlapping of access operations. One store corresponds to odd addresses, the other to even addresses, and an overall average apparent cycle time of 4.8 microseconds is usually obtained by instructions. Input-output accesses probably average 3.2 microseconds. One access can provide one 48-bit number, a pair of 24-bit instructions, or a 15-bit address part of an instruction. No facilities are provided for core-to-core block transfers.

A check on the store is provided by maintaining a tolerance on the size of output pulses.

.14 Availability: . . . . . . 4 months.

.15 First Delivery: . . . . 1962.

.16 Reserved Storage

Purpose	Number of locations	Locks
Buffer control words:	6	none.
Interrupt return and entry:	9	none.
Real-time clock:	1	none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . magnetic cores.

.22 Physical Dimensions

.221 Magnetic core type storage
Core diameter: . . . 0.080 inch.
Core bore: . . . . . 0.050 inch.
Array size: . . . . . 128 bits by 128 bits.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . no.
.244 Data permanent: . . . no.
.245 Storage changeable: . . no.

.27 Interleaving Levels: . . . . . . there are two stores; one is referenced by odd addresses, the other by even addresses.

.28 Access Techniques

.281 Recording method: . . coincident current.
.282 Reading method: . . . sense wire.
.283 Type of access: . . . readout followed by rewrite.

.29 Potential Transfer Rates

.292 Peak data rates
Cycling rates: . . . . up to 156,000 cps per bank.
Unit of data: . . . . one 48-bit word.
Gain factor: . . . . use of two interleaved stores.
Data rate: . . . . . 156,000 words/sec per bank.
Compound data rate: . . . . 312,000 words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

Words: . . . . 32,768.
Instructions: . . . . . 65,536.

.4 CONTROLLER: . . . no separate controller.

.5 ACCESS TIMING

.51 Arrangement of Heads: the store is divided into two halves with independent access facilities.

.52 Simultaneous Operations: . . . . accesses to each half are asynchronous and independent of each other.

.53 Access Time Parameters and Variations

.531 For one half of store
Access time: . . . . . 2.2 μ sec.
Rewrite time: . . . . 4.2 μ sec.
Cycle time: . . . . 6.4 μ sec.
For data unit of: . . . 1 word.
2 instructions.

.532 Variation in cycle time
For alternate accesses to each half: 3.2 μ sec.
For random accesses: 4.8 μ sec avg., quoted by CDC.
see discussion in introduction.
For worst case: . . . 6.4 μ sec.

§ 041.

.6 CHANGEABLE STORAGE: . . . . none.

.7 STORAGE PERFORMANCE

.71 Data Transfer

Pair of storage unit possibilities
With self: . . . . yes.

.72 Transfer Load Size

With self: . . . . one 48-bit word or one 15-bit instruction address part.

.73 Effective Transfer Rate

With self
Using programmed loop: . . . . 46,400 words/sec.
Using straight-line coding: . . . . . . 69,444 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Receipt of data:	none.	
Recording of data:	none.	
Recovery of data:	tolerance on pulse size	stop, lamp.
Memory fault:	stage-sequencing	stop, lamp.
Invalid address:	not possible.	

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . central processor. CDC 1604-A.

.12 Description

The 1604-A is a single-address, fixed word length, binary processor. The main arithmetic and control circuitry, core storage, I/O channels, and console controls are all housed in the processor cabinet.

Arithmetic operations are performed in binary on 48-bit words. The operations are performed in a parallel mode. Each word can contain a pair of 24-bit single address instructions. An instruction's address may be indexed or used as an indirect address. Three index bit positions are provided in each instruction to select one of six index registers. However, one value of the index bits specifies an indirect address, and indirect addressing may be recursive.

Operations are provided in both fixed and floating point. Fixed length operands are 48 bits in size while floating point operands consist of an 11-bit characteristic and sign plus 36-bit fixed point part. Both integral and fractional fixed point multiplication and division are provided.

A variety of indexing, logical, masking, and storage-searching operations are provided. They are oriented toward scientific calculations or simulation. There are no code conversion, data editing, or bulk moving facilities. The six index registers and the indirect addressing facility allow modification of operand addresses. No equivalent modification of transfer addresses is possible; if a transfer of control is required, based on the contents of an index register (such as after a table search instruction), from three to six instructions are involved. These instructions can be written in many ways and the programmer must spend time deciding which is the best under the circumstances.

There are two main accumulator registers, labeled A and Q. A number of instructions applying to register A have exact parallel instructions applying to register Q. There is, in the normal 1604-A, no instruction which transfers data from A to Q or vice-versa.

Increased processor speeds are achieved by the use of two storage banks. These banks may be accessed alternately with savings in access timing due to both

.12 Description (Contd.)

overlapped accesses and to the selection of pairs of instructions. Most instruction execution times average 7.2 microseconds.

Because of the overlapped stores, execution times for individual instructions and sequences of instructions may vary up to 25 percent above and below the average. It is possible, however, to take advantage of the timing variations by careful planning. All times in this report are based upon averages; i.e., random placement of instructions and operands.

Since each word holds a pair of instructions which cannot be addressed separately, all transfers of sequence must go to the upper instruction of a pair. A number of other programming complications arise from this packing of instructions because of the housekeeping required (even with assembly systems) in keeping track of the position of various instructions and because some instructions (such as jumps) behave differently, depending upon which position they are stored in.

Input-output operations can be either buffered or unbuffered under control of the processor (see Section :111).

A real-time clock is provided which operates by adding 1 sixty times a second to a word which is brought to the accumulator. By initializing the clock at a large value, it can cause interruption when it overflows.

Interrupts on the CDC 1604-A are caused by either an arithmetic fault condition or an I/O channel condition.

There are five arithmetic fault conditions; each has to be set to interrupt separately. Each I/O channel has its own particular location to which it interrupts, thereby reducing the time spent in the interrupt routines. Should an interrupt occur during an I/O routine, it will be held until the end of the first interrupt routine. Masking the interrupts can be done by the program.

The central processor shares access to the core storage with the buffer control. Thus, if immediately after a division order has been started, an input buffer wishes to transfer a word into core storage, the transfer will only be held up until the divisor has been obtained from core store (a maximum of 6.4 microseconds) and thus, the transfer and the division will take place simultaneously.

§ 051.

.12 Description (Contd.)

There are two different sets of facilities by which input-output units may be controlled by program: (1) instructions which sense the status of an input-output device, and (2) interrupt signals. A mixture of the two may also be used. Masks and conditions set by the programmer decide which events are allowed to interrupt a program. When sensing, it is necessary to test for overflows, input-output ready, or input-output errors. When interrupting, reliance is made on special master routines to deal with general cases. Interruption can be used to control input-output operations and simultaneity, but there are significant overheads in such operations.

It is not generally practical to use the interrupt technique for multi-running of several programs because there is not inter-program protection. However, it is possible to run one main program and one or two peripheral programs if programming conventions are firmly established, and if the full use of certain channels is allocated to the peripheral program(s).

.13 Availability: . . . . . . 2 to 4 months.

.14 First Delivery: . . . . 1962.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point			
	Add-subtract:	automatic	binary	1 word
	Multiply			
	Short	none.		
	Long, integral:	automatic	binary	2 words.
	Long, fractional:	automatic	binary	2 words.
	Divide			
	No remainder:	none.		
	Remainder, integral:	automatic	binary	2 words.
	Remainder, fractional:	automatic	binary	2 words.
.212	Floating point			
	Add-Subtract:	automatic	binary	36 & 11 bits (1 word).
	Multiply:	automatic	binary	36 & 11 bits (1 word).
	Divide:	automatic	binary	36 & 11 bits (1 word).
.213	Boolean			
	AND:	automatic		1 word.
	Inclusive OR:	automatic	binary	1 word.
	Other logical and mask-type operations:	automatic		1 word.

.214 Comparison: . . . . . . yes.
.215 Code translation: . . . none.
.216 Radix conversion: . . . none.
.217 Edit format: . . . . . . none.
.218 Table look-up

	Provision	Comment	Size
Equality:	automatic	with and without mask	32, 768 words max.
Greater than:	automatic	with and without mask	32, 768 words max.
Greatest:	none.		
Least:	none.		

.22 Special Cases of Operands

.221 Negative numbers: . . . 1's complement.
.222 Zero: . . . . positive zero and negative zero. They are equal in arithmetic, but in index registers the sequence of steps is ... -2, -1, -0, +0, +1, ...
.223 Operand size determination: . . . . fixed.

.23 Instruction Formats

.231 Instruction structure: . one half-word (24 bits).
.232 Instruction layout:

Part	OP	ID	A
Size (bits)	6	3	15

.233 Instruction parts

Name	Purpose
Op, Operation Code:	specifies any of 62 operations.
ID, Index Designator:	specifies one of 6 index registers, or indirect addressing mode, or a transfer condition.
A, Base Execution Address:	specifies address of operand, an operand, or a shift count.

.234 Basic address structure: 1 + 0.
.235 Literals
Arithmetic: . . . . . . 15-bit address.
Incrementing modifiers: . . . . . 15-bit address.
.236 Directly addressed operands
.2361 Internal storage
Type: . . . . core.
Size: . . . . 15 or 48 bits.
Volume accessible: . all storage.
.2362 Increased address capacity: . . . . . . none.
.237 Address indexing
.2371 Number of methods: . 1.
.2373 Indexing rule: . . . . . addition modulo store size.
.2374 Index specification: . . 3 bit positions within the instruction to be modified.
.2375 Number of potential indexers: . 6.
.2376 Addresses which can be indexed: . . . . . operand addresses in arithmetic, logical, load, and store instructions.

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.2377 Cumulative indexing: . . none.

.2378 Combined index and step: . . . . . . none.

.238 Indirect addressing

.2381 Recursive: . . . . . . yes.

.2382 Designation: . . . . . "7" configuration of the index designator character of the instruction. The new address and index register is that of the lower instruction in the designated word.

.2383 Control: . . . . the last address in the recursive sequence specifies a direct address; i.e., other than a "7" index designator in the lower instruction of the word.

.2384 Indexing with indirect addressing: . . . . . only the last address in the indirect address chain may be modified by indexing.

.239 Stepping

.2391 Specification of increment: . . . . . stepping instructions.

.2392 Increment sign: . . . minus, plus.

.2393 Size of increment: . . minus unity, plus unity, or plus 15-bit literal in stepping instruction (but note stepping sequence is ... -2, -1, -0, +0, +1, +2, ...).

.2394 End value: . . . . . . zero, equality.

.2395 Combined step and test: . . . . yes.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size	Program usage
Q Register	1	48 bits	auxiliary arithmetic & logic.
Index Registers:	6	15 bits	address modification.
Program Register:	1	15 bits	jumps.
Buffer Control Words:	6	48 bits	control of I/O operations.
Master Mask Interrupt Register (MMIR):	1	1 bit	masking of interrupts.

.242

Category of storage	Total number locations	Physical form	Access time, μ sec
Q Register	1	flip-flops	0.2
Index Registers	6	flip-flops	0.2
Program Register:	1	flip-flops	0.2
Buffer Control Words:	6	core & flip-flop	0.2, when used by I/O logic. 4.8, when referenced by program.
MMIR	1	flip-flop	0.2

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . 1.

.315 Sequence control step size: . . . . 1 word; i.e., moves by instruction pairs.

.316 Accessibility to routines: . . . . yes, by means of a "Return Jump" instruction.

.317 Permanent or optional modifier: . . . . no.

.32 Look-Ahead: . . . . . . none.

.33 Interruption

.331 Possible causes

Input-Output Units	Conditions
Console typewriter:	carriage return.
Paper tape reader: .	end of tape.
Paper tape punch: . .	none.
IBM 88 Collator: .	when free.
IBM 407 Printer: .	when free.
IBM 523 Card reader:	when free.
IBM 533 Card reader:	when free.
IBM 533 Card punch:	when free.
CDC 1612 Printer:	when free.
CDC 606 Mag. Tape Units:	when tape free; when error occurs.
CDC 1617 Card reader:	none.

No interrupt on unit break-down is available. If a malfunction occurs in a unit causing it to become unavailable no interrupt will notify the main program.

Processor Errors: . . . arithmetic overflow.
exponent overflow.
exponent underflow.
shift.
divide.

Other: . . . . real-time clock overflow.

332 Control by routine: . . use of Master Mask Interrupt Register.

333 Operator control: . . . none.

334 Interruption conditions

I/O Interrupts: . . . . unit selected to interrupt. Channel allocated to unit. Unit signals condition (see Table in .331). Interruption not inhibited by MMIR. Neither arithmetic nor I/O interrupt routine in operation.

Arithmetic Interrupts: condition selected to interrupt. Interruption not inhibited by MMIR. Arithmetic or I/O interrupt not in operation.

.335 Interruption process Instruction Sequence:
(a) The current program is interrupted.
(b) Interrupt lockout is applied in order to prohibit any further interrupt signals from interrupting the 1604-A when it is executing an interrupt routine.
(c) The address of the next instruction of the interrupted program is stored.

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.335 Interruption process

Instruction Sequence: (Contd.)

(d) The 1604-A jumps to an interrupt location in the memory. This interrupt location depends on the source of the interrupt signal.

(e) The 1604-A performs the stored routine beginning at the interrupt location.

(f) After completing the interrupt routine, the 1604-A turns off the interrupt signal, clears the interrupt lock-out, and continues with the next instruction of the interrupted program.

Registers saved: . . . . under program control only.

Destination: . . . . . . arithmetic interruptions go to 00007.
I/O interruptions go to 00010-000017, depending on channel number.

.336 Control methods

Determine cause: . . sense instructions written in own coding.

Enable interruption: . return after interrupt routine resets the interrupt lock-out. Moderate capability for one or more peripheral programs as well as one major program.

.34 Multi-running

.341 Method of control: . . . use of channel interrupts, with resulting lock-out of major and other peripheral programs.

.342 Maximum number of programs: . . . . . . depends on number of channels available.

.343 Precedence rules: . . . peripheral programs have priority over main program. Peripheral program in use locks out other peripheral programs.

.344 Automatic program protection: . . . . . . none.

.35 Multi-sequencing: . . . none.

.4 PROCESSOR SPEEDS

Conditions: . . . . all timings based on random addresses.

.41 Instruction Times in μ secs

.411 Fixed point

Add-subtract: . . . . 7.2.
Multiply: . . . . 25.2 + 0.8n.
Divide: . . . . 65.2.
n = number of ones in multiplier.

.412 Floating point

Add-subtract: . . . . 18.8 average.
Multiply: . . . . 36.0 average.
Divide: . . . . 56.0 average.

.413 Additional allowance for

Indexing: . . . . none.
Indirect addressing: . . . . . 4.8 average, per indirect reference.

.414 Control

Branch: . . . . 7.2.

.415 Counter control

Step: . . . . 3.0.
Step down and test zero: . . . . . . 7.2.
Step up and test equal: . . . . . 7.2.

.418 Shift: . . . . 2.8+0.4B.
B = number of bits shifted.

.42 Processor Performance in μ secs

.421 For random addresses

	Fixed point	Floating point
c = a + b:	21.6	33.2.
b = a + b:	20.4	33.2.
Sum N items:	7.2	18.8.
c = ab:	39.6 to 77.2	50.4.
c = a/b:	82.6	70.4.

.422 For arrays of data

	Fixed point	Floating point
$c_i = a_i + b_j$:	29.0	40.6.
$b_j = a_i + b_j$:	27.6	40.6.
Sum N items:	11.6	23.2.
$c = c + a_i b_j$:	53 to 91.4	76.6.

.423 Branch based on comparison

Numeric data: . . . . 50.4.
Alphabetic data: . . . none.

.424 Switching

Unchecked: . . . . . . 28.8.
Checked: . . . . 53.6.
List search: . . . . . 43.5 + 3.6N.

.425 Format control per character (including BCD-binary conversion)

Unpacking: . . . . . . 80 (***).
Packing: . . . . 240 (***).

.426 Table look-up per comparison:

For a match: . . . . . 3.6.
For greatest: . . . . . 3.6 (or 21.8 whenever new "greatest" is found).
For least: . . . . . . 26.0 (or 39.2 whenever new "least" is found).
For interpolation point: . . . . 3.6.

.427 Bit indicators

Set bit in separate location: 14.4
Set bit in pattern: . . 21.6.
Test bit in separate location: . . . . . . 8.8.
Test bit in pattern: . . 21.6.
Test AND for B bits: . 28.8.
Test OR for B bits: . . 21.6.

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.428 Moving: . . . . 69,444 48-bit words/sec. with straight line coding. 46,400 48-bit words/sec. with looped coding.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	check	set overflow indicator, with optional interrupt.
Underflow:	check	sets overflow indicator with optional interrupt.

.5 ERRORS, CHECKS AND ACTION (Contd.)

Error	Check or Interlock	Action
Zero division:	causes overflow.	
Shift fault:	check	sets overflow indicator with optional interrupt.
Invalid data:	none.	
Invalid operation:	used as fault indicator	halts computer.
Arithmetic error:	none.	
Invalid address:	none	modulo size of store.
Receipt of data:	tolerance check on pulse size	halts computer & lights lamp.
Dispatch of data:	none.	

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . . . Console.

.12 Associated Units: . . CDC 350 Paper Tape Reader. Teletype BRPE Paper Tape Punch. Soroban-modified IBM Typewriter.

.13 Description

The Console control panel is mounted vertically at desk-top level at the apex of a V-shaped desk. Mounted on the desk at the operator's left is a typewriter. At the extreme right of the operator, mounted in the desk, are the paper tape punch and reader. The desk provides the operator with adequate work area and a generally clear view of peripheral units. The console panel displays the full complement of operational registers both for display of computer status and for communication with and control of the computer program. A number of alarms are displayed visibly by lamps and accoustically by means of a loudspeaker with a volume control. The console typewriter may be selected to enable the operator to interrupt the computer for operator-to-computer communication. All console equipment communicates with the computer via a single pair of buffered input-output channels.

.2 CONTROLS

.21 Power

Name	Form	Comment
Power-On:	green button	applies AC and DC power to computer.
Power-Off:	red button	removes DC and AC power from computer.

.22 Connections: . . . . none.

.23 Stops and Restarts

Name	Form	Comment
Start-Step:	lever-switch	start (up position): selects high-speed mode. step (down position): selects step mode.
Breakpoint:	five 8-position switches	provide for selection of any storage location as a breakpoint address.
Selective Stops 1, 2, 3:	three lever switches	provide manual conditions for stopping the computer on a selective stop instruction.

.24 Stepping

Name	Form	Comment
Start-Step:	momentary lever switch	step (down position): selects step mode. A single instruction is executed each time switch is pressed down. start (up position): selects high-speed mode for program execution.

.25 Resets

Name	Form	Comment
Clear:	momentary lever switch	down position: resets all operational registers and most flip-flops in the computer. up position: resets external equipment.
Clear:	1 pushbutton for each console register	clears register.

.26 Loading: . . . . . . Auto Load Button initiates loading from magnetic tape; otherwise a manual 15-step procedure is required.

.27 Sense Switches

Name	Form	Comment
Selective Jumps 1, 2, 3:	three lever switches	provide manual setting of conditions for selective jump instruction.

.28 Special

Name	Form	Comment
Volume Control:	knob	controls volume of signal from loudspeaker.
Storage Test:	two lever switches	margin: used for maintenance purposes only. mode: used in conjunction with Start-Step Mode switch, to disable advancing to next instruction or to examine storage contents without executing instructions.

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.3 DISPLAY

.31 Alarms

Name	Form	Condition Indicated
Divide fault:	lamp	improper divide instruction executed.
Shift fault:	lamp	excessive shift, greater than 127 bits.
Overflow:	lamp	addition or subtraction overflow.
Exponent fault:	lamp	exponent exceeds 210.
Odd Storage fault:	lamp	fault in sequence chain of odd storage unit.
Even Storage fault:	lamp	fault in sequence chain of even storage unit.
Interrupt Request:	lamp	interrupt request signal is being received by interrupt circuit.
Punch Out of Tape:	lamp	punch tape reel is nearly empty.

.32 Conditions

Name	Form	Condition Indicated
Interrupt Disable:	lamp	computer is in interrupt routine.
Channels 1-6 Active:	6 lamps	indicates the current status of the 6 I/0 channels (active or inactive).
Paper Tape Reader Ready:	lamp	indicates that paper tape is at load point (ready for an input buffer) or input buffer paper tape is in progress.
Deep End:	lamp	failure to complete operation.
Lower Instruction:	lamp	lower instruction is in progress.
Sweep:	3 lamps	indicates computer is in Sweep Mode (instructions read but not executed).

.33 Control Registers

Name	Form	Comment
P Register:	5 octal lamp modules	octal display of sequence counter contents.
Execution Address:	5 octal lamp modules	octal display of operand address.
Function Code:	3 octal lamp modules	octal display of instruction function code.
6 Index Registers:	5 octal lamp modules for each register	octal display of contents of index registers.
A Register (left and right):	16 octal lamp modules	octal display of contents of the accumulator.
Q Register (left and right):	16 octal lamp modules	octal display of contents of the Q register.

.34 Storage: . . . . . . contents of operational registers only are displayed in octal form when computer is stopped; no display when computer is running.

.4 ENTRY OF DATA

.41 Into Control Registers: bit switches permit direct data entry into all operational registers: P Register, Instruction Register (function code and execution address), 6 Index Registers, A Register, and Q Register.

.42 Into Storage: . . . . load control registers with data and store instruction and actuate Start-Step lever: up for high-speed mode, down position for step mode.

.5 CONVENIENCES

.51 Communication: . . . loudspeaker with volume controls.

.52 Clock: . . . . none.

.53 Desk Space: . . . . ample work space is provided on the console desk.

.54 View: . . . . console display is just below eye level of seated operator. View is generally unimpeded.

.6 INPUT-OUTPUT UNIT

.61 Typewriter, Soroban-modified IBM

.62 Description

The typewriter may be used as a keyboard input device or as an output device for producing printed copy. All of the typewriter characters and functions are represented by unique combinations of six bits. The typewriter may be selected to interrupt on each carriage return on input; this may be used to enable the operator to communicate with the computer program.

.63 Performance: . . . . peak speed is 10 char/sec.

INPUT-OUTPUT: GENERAL

§ 070.

There are six buffered input-output channels on the CDC 1604-A arranged in three pairs of one input and one output channel each. The buffering on each channel consists of one 48-bit word that is filled from, or loaded into, a core storage location whenever necessary.

A buffer control word for each channel specifies the address of the next core storage location to be used and a "terminal address," which is greater by one than the address of the last location to be filled or read out of core storage. After each one-word data transfer between the buffer and core storage, the address in the buffer control word is automatically incremented by one and compared with the terminal address. If the two addresses are equal, the data transmission is halted; otherwise, the buffer control word is replaced in storage and the transmission continues.

The buffer control words are only partially held in core storage; 30 of the 48-bits being stored in flip flops which allow fast (0.2 microsecond) access during input-output transfers. This arrangement reduces the cost of input-output transfers from 14.8 microseconds in the 1604 per word to 3.2 microseconds in the 1604-A.

Computation in the central processor can proceed during this period, provided no access to the same core bank is required. There is no lock-out protection for the buffer control word; the addresses it contains may be modified as the programmer desires. This allows "clever" programming, which may or may not be worthwhile depending upon the circumstances.

There is a special I/O type of interrupt, which is distinguished from arithmetic interrupts. During this interrupt the program jumps to location 000N, where N is the channel number from which the interrupt came. A return jump is also stored in the same location. Further interrupts can be locked out but not lost.

The cause of the interrupt depends upon the particular hardware unit which is "selected" on the I/O channel. Some units have no interrupt causes, some have one, and one unit has two. It is not possible by use of interrupts to become aware that an input-output unit has become inoperative during a run. These occurrences can be detected by special programming techniques initiated by the regular overflow of the real-time clock.

A separate non-buffered I/O channel is available as well as the six buffered channels. This is channel 7, a bi-directional channel which can receive or transmit data at a rate of up to one word every 3.2 microseconds. This channel is used for connection to other computers, or to data links.

Although only the units presently listed by Control Data Corporation are covered in this report, those that were used on the CDC 1604 (see Report 241:) could also be used if desired.

INPUT-OUTPUT: PAPER TAPE READER

§ 071.

.1 GENERAL

.11 Identity: . . . . Paper Tape Reader. CDC 350.

.12 Description

The 350 Paper Tape Reader is a photoelectric reader mounted in the 1604 console desk. Tape may be made of paper, parchment, Mylar or Mylar-aluminum laminate. Reading can be performed on either strips or loops of tape. The reader operates at a rate of up to 350 characters per second, and can accept 7- or 8-level tapes of standard widths.

Two reading modes are available, chosen by a switch on the console:

- In the ASSEMBLY mode, 7-track paper tape is used, and one 48-bit computer word is formed from the six lower tracks of 8 rows. The seventh track contains a single punch which denotes the end of a computer word; error checking is available if this is not correctly placed every eight characters.
- In the CHARACTER mode, any width of tape is allowable, but in practice eight-level tape is normally used. Each character is loaded into core storage separately, one character per word.

The reading head employs transparent windows which channel light to the photo cells. This provides a smooth reading surface and has no holes which could accumulate dust and cause reading errors. Checking is provided for an end-of-tape condition, but there is no automatic parity check on reading.

.13 Availability: . . . . . 2 to 4 months.

.14 First Delivery: . . . . 1960.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller friction.
.212 Reservoirs: . . . . . none.
.213 Feed drive: . . . . . motor.

.22 Sensing and Recording Systems

.221 Recording system: . . none.
.222 Sensing system: . . . photoelectric.

.24 Arrangement of Heads

Use of station: . . . . reading.
Stacks: . . . . 1.
Heads/stack: . . . . . 8.
Method of use: . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . paper tape; tape made of parchment, Mylar or Mylar-aluminum laminate.
.312 Phenomenon: . . . . . fully punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . . . 1 to N rows at 10 rows per inch.
.322 Parallel by: . . . . . 7 or 8 tracks at standard spacing.
.324 Track use
Data: . . . . 6 in the Assembly Mode; 8 in the Character Mode.
Redundancy check: . . 0.
Timing: . . . . . . 1 (sprocket hole).
Control signals: . . . 1 word marker in the Assembly Mode.
Unused: . . . . . . none.
Total: . . . . 7 plus sprocket hole in Assembly Mode. 8 plus sprocket in Character Mode.
.325 Row use: . . . . . . all for data; no inter-block gap required.

.33 Coding: . . . . matched to Data Code Table No. 6.

.34 Format Compatibility: . all devices using standard 7- or 8-track punched tape.

.35 Physical Dimensions

.351 Overall width: . . . . 0.875 inch for 7-track tape. 1 inch for 8-track tape.
.352 Length: . . . . 1,000 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . built into Console.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . N rows, 1 row per word (Character Mode). N rows, 8 rows per word (Assembly Mode).

§ 071.

.442 Input-output area: . . . core storage.
.443 Input-output area access: . . . . . . each word of core storage.
.444 Input-output area lockout: . . . . . . none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . 8 to 8N rows in Assembly Mode to form N words in core storage.
1 to N rows in Character Mode.
.512 Block demarcation Input: . . . . count in instruction.

.52 Input-Output Operations

.521 Input
Assembly Mode: . . . N words forward.
Character Mode: . . N characters forward, filling each word with zeros and the character read in.
.523 Stepping: . . . . none.
.524 Skipping: . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . none.

.55 Control Operations

Disable: . . . . no.
Request interrupt: . . yes.
Select format: . . . . no; selection of Assembly or Character Mode is performed manually.

.56 Testable Conditions

Disabled: . . . . . . no.
Busy device: . . . . . yes.
End-of-tape: . . . . . yes.
Operational Mode: . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 350 char/sec.
.622 Important parameters:
Density: . . . . 10 char/inch.
Speed: . . . . 35 inches/sec.
Start time: . . . . . 3 m.sec to full speed.
Stop time: . . . . . 1 m.sec.
.623 Overhead: . . . . . . none.
.624 Effective speeds: . . . 350N/ (N + 1) char/sec, for N rows/block.

.63 Demands on System

Component	n.sec per word	or	Percentage
Processor:	0.004		0.02

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . number of tracks.
Method: . . . . tape width guide.
Comment: . . . . . . set for 5, 7, or 8 level tape.

.72 Other Controls

Function: . . . . . . mode selector.
Form: . . . . switch.
Comment: . . . . . . selects Character Mode or Assembly Mode.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Reel:	1,000 feet.

.732 Replenishment time: . 0.5 to 1.0 minute; unit needs to be stopped.
.733 Adjustment time: . . . 1.0 minute including replenishment.
.734 Optimum reloading period: . . . . 6 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	none.	
Invalid code:	not possible.	
Exhausted medium:	none.	
Nearly exhausted medium:	end-of-tape indicator.	set indicator.
Format error:	check.	suspends input; sets indicator.
Hardware failure:	none.	
Timing conflicts:	none.	

INPUT-OUTPUT: PAPER TAPE PUNCH

§ 072.

.1 GENERAL

.11 Identity: . . . . Paper Tape Punch. Teletype BRPE Punch.

.12 Description:

The Paper Tape Punch is mounted on a hinged rack at the rear of the right wing of the console desk. Punched tape is fed out of a slot in the compartment door. The punch can be programmed to punch one character at a time or to punch continuously. The punch operates at 110 characters per second and punches six, seven, or eight levels as required.

ASSEMBLY or CHARACTER punching modes are available, chosen by program:

- In the ASSEMBLY Mode, 7-track paper tape is used, and 8 rows are formed from one 48-bit computer word. Six tracks are used for data, and the seventh track is only used for one control punch in the last row of each word.

- In the CHARACTER Mode, the lower six or eight bits of a computer word are punched, depending on the width of tape in the punch. Each separate row is transmitted from a separate computer word.

.13 Availability: . . . . . 2 to 4 months.

.14 First Delivery: . . . 1960.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket drive.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . die punch.
.222 Sensing system: . . . none.

.23 Multiple Copies: . . . none.

.24 Arrangement of Heads

Use of station: . . . . punching.
Stacks: . . . . 1.
Heads/stack: . . . . . 8 plus sprocket punch.
Method of use: . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . . paper tape.
.312 Phenomenon: . . . . . fully punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . . . 1 to N rows at 10 rows/inch.
.322 Parallel by: . . . . . 7 tracks in Assembly Mode. 6 or 8 tracks in Character Mode.
.324 Track use
Data: . . . . 6 or 8.
Redundancy check: . 0.
Timing: . . . . . . 1 (sprocket hole).
Control signals: . . . 1 word marker in Assembly Mode.
Unused: . . . . . . 0.
Total: . . . . 7 plus sprocket hole in Assembly Mode. 6 or 8 plus sprocket hole in Character Mode.
.325 Row use: . . . . all for data.

.33 Coding: . . . . matched to Data Code Table No. 6.

.34 Format Compatibility: . all devices using standard 6-, 7-, or 8-track paper tape.

.35 Physical Dimensions

.351 Overall width: . . . . 0.875 inch for 6- or 7-track tape. 1 inch for 8-track tape.
.352 Length: . . . . up to 1,000 feet per roll.

.4 CONTROLLER

.41 Identity: . . . . built into console.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: . . . . . . 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N characters.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . . each word of core storage.
.444 Input-output area lockout: . . . . . . none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

§ 072.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 8 to 8N rows in the Assembly Mode.
1 row in the Character Mode.
.512 Block demarcation: . . count in instruction.

.52 Input-Output Operations

.522 Output: . . . . punch 8N rows forward in Assembly Mode.
punch least significant character of N words in storage in Character Mode.
.523 Stepping: . . . . none.
.524 Skipping: . . . . none.
.525 Marking: . . . . none.
.526 Searching: . . . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . none.

.55 Control Operations

Disable: . . . . no.
Request interrupt: . . no.
Select format: . . . . select Assembly or Character Mode.
Select code: . . . . . . no.

.56 Testable Conditions

Disabled: . . . . no.
Busy device and not out of tape: . . . . . . yes.
Nearly exhausted: . . yes.
End of medium marks: no.

.6 PERFORMANCE

.61 Conditions:

I: . . . . Assembly Mode.
II: . . . . Character Mode.

.62 Speeds

.621 Nominal or peak speed: . . . . 110 char/sec.
.622 Important parameters
Tape speed: . . . . 11 inches/sec.
Packing density: . . . 10 char/inch.
.623 Overhead: . . . . none.
.624 Effective speeds: . . . 110 char/sec. if less than 250 μsec elapse between completion of punching one char and initiation of next output operation.

.63 Demands on System

Component	Condition	m. sec per word	or	Percentage
Processor:	I	0.0005		0.005
	II	0.004		0.04

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method
Number of tracks: . . .	Tape width guide.

.72 Other Controls

Function: . . . . tape feed.
Form: . . . . lever.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Reel:	1,000 feet.

.732 Replenishment time: . . . . 2.0 to 3.0 minutes; punch needs to be stopped.
.733 Adjustment time: . . . 3.0 to 4.0 minutes.
.734 Optimum reloading period: . . . . 18.2 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Output block size:	not possible.	
Invalid code:	not possible.	
Exhausted medium:	yes	set indicator.
Timing conflicts:	none.	

INPUT-OUTPUT: CDC 1617 CARD READER

§ 074.

.1 GENERAL

.11 Identity: . . . . Card Reader. CDC 1617.

.12 Description

The CDC 1617 Card Reader reads 80 column cards photoelectrically at a maximum rate of 250 cards a minute. An infinite clutch is used so that the effective reading rate is reduced smoothly to match other limitations. This contrasts with single point clutches where the speeds decrease in steps with some losses in efficiency. There is only one read station, and verification of the reading is a responsibility of the program.

Reading is accomplished column by column, and automatic translation from Hollerith coding is available under program control. Each column (12 bits if not translated, or 6 bits if translated) is loaded into the less significant end of contiguous computer words.

No Interrupt facilities are provided by the unit.

.13 Availability: . . . . . . 2 to 4 months.

.14 First Delivery: . . . . September, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch rollers.
.212 Reservoirs: . . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . none.
.222 Sensing system: . . . . photoelectric.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . reading.
Stacks: . . . . 1.
Heads/stack: . . . . . . 12.
Method of use: . . . . . 1 column at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . standard 80-column cards.
.312 Phenomenon: . . . . . . rectangular holes.

.32 Positional Arrangement

.321 Serial by: . . . . 12 rows at standard spacing.
.322 Parallel by: . . . . . . 80 columns at standard spacing.
.324 Track use: . . . . all for data.
.325 Row use: . . . . all for data.

.33 Coding: . . . . column binary. Hollerith (see Data Code Table Nos. 4 and 5 for external and internal representation).

.34 Format Compatibility: . all devices using standard 80-column cards.

.35 Physical Dimensions: . standard 80-column cards.

.4 CONTROLLER

.41 Identity: . . . . this function is performed by the central processor.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: 3 max.
.432 Restrictions: . . . . . . only one CDC 1617 per input channel.

.44 Data Transfer Control

.441 Size of load: . . . . . . 1 to N cards, N limited by store size.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . each word (equivalent to each card column).
.444 Input-output area lockout: . . . . no lockout available.
.445 Table control: . . . . . no formal facilities, but can be programmed dynamically using own coding.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 to N cards.
.512 Block demarcation: . . filling of area defined by buffer control words (counters).

.52 Input-Output Operations

.521 Input: . . . . 1 to N cards forward.
.522 Output: . . . . none.
.523 Stepping: . . . . none.
.524 Skipping: . . . . none.

§ 074.

.525 Marking: . . . . none.
.526 Searching: . . . . none.

.53 Code Translation: . . . Hollerith translation available optionally, (see Data Code Table Nos. 4 and 5).

.54 Format Control: . . . . none.

.55 Control Operations

Request interrupt: . . . no.
Offset card: . . . . . . only one hopper.
Select stacker: . . . . . only one stacker.
Select code: . . . . . . column binary or Hollerith.

.56 Testable Conditions

Disabled: . . . . yes.
Busy device: . . . . . . yes.
Output lock: . . . . . . no lock available.
Nearly exhausted: . . . no.
Hopper empty: . . . . . yes.
Stacker full: . . . . . . yes.
Feed failure: . . . . . . yes.
Amplifier failure: . . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . none.

.62 Speeds

.621 Nominal or peak speed: 250 cards/min.
.622 Important parameters: none.
.623 Overhead: . . . . none; the unit is asynchronous, reading rate is controlled by the program.
.624 Effective speed: . . . . 250 cards/min.

.63 Demands on System

Component: . . . . . . central processor.
M. sec per card: . . . . 0.256.
or
Percentage: . . . . . . 0.1.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . . . none.

.72 Other Controls: . . . . none.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	500 cards.
Stacker:	500 cards.

.732 Replenishment time: . . 0.25 to 0.50 mins. unit does not need to be stopped.
.734 Optimum reloading period: . . . . 2 mins.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	none.	
Input area overflow:	check	length error turned on.
Invalid code:	none.	
Exhausted medium:	check	sets special indicator.
Imperfect medium:	check	sets special indicator.
Timing conflicts:	not possible.	
Amplifier failure:	check	sets special indicator.

INPUT-OUTPUT: CDC 1612 PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . High Speed Printer CDC 1612 Unit.

.12 Description

The 1612 High Speed Printer consists of an Anelex Series 4-1000 model printer mounted on top of a 1612 Printer Control Unit. The printer system is designed for use as a peripheral unit for the 1604-A and other CDC computers. It prints the computer data output on fan-fold forms at a nominal maximum rate of 1,000 lines per minute. An alternative maximum rate of 667 lines per minute is possible and may be selected by actuating a single switch in the printer control unit. This 667 line rate is effected by reducing the speed of the print drum and, as a result, produces printing with improved vertical registration. One print line consists of a maximum of 120 character positions; each position can print from a 64 character set. Maximum print rates are achieved when use is limited to the 48-character FORTRAN subset of the total character set and a maximum of two line feeds following each print line, otherwise speeds are reduced by a factor of two.

Printing is accomplished by an "on-the-fly" technique. Paper and inked ribbons pass between a rotating print cylinder and a row of hammers. Timing is coordinated to strike each hammer when the appropriate character appears beneath it.

Characters to be printed are stored, in BCD form, one character to a computer word. They are assigned starting at the left-hand margin, and a maximum of 120 characters are transmitted for one line. Processor overhead is proportionately reduced if less than 120 characters are used. Paper advance follows printing, and line spacing is provided automatically by means of a pre-punched tape in the printer. Eight channels on the tape, selected by programmed instructions, control the vertical formats.

The computer is occupied only during the time required to make storage references for each character to be printed; a maximum of 120 references for each line of print. The printer occupies the data transfer channel to which it is connected only for the time required to transfer the print character data and the time for control signal communication. While paper is being advanced, the channel is free to service some other device that may also be connected to it.

.13 Availability . . . . . 2 to 4 months.

.14 First Delivery . . . . 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket drive push and pull.
.212 Reservoirs . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . on-the-fly hammer stroke against engraved drum.

.23 Multiple Copies

.231 Maximum number
Interleaved carbon: . 5.
Card stock: . . . . . 1.
.233 Types of master
Multilith: . . . . . . yes.
Xerox: . . . . yes.
Spirit . . . . yes.

.24 Arrangement of Heads

Use of station: . . . . printing.
Stacks: . . . . 1.
Heads/stack: . . . . . 120.
Method of use: . . . . prints one line at a time.

.25 Range of Symbols

Numerals:	10	0 to 9.
Letters:	26	A to Z.
Special:	28	see below.
Alternatives:	upon request.	
FORTRAN set:	yes, see below.	
Req'd COBOL set: . . .	no.	
Total:	64	

See Data Code Table No. 1.

Special characters in FORTRAN set	Additional characters in full set
. period	≤ less than or equal
- minus	≥ greater than or equal
+ plus	< less than
= equal	> greater than
(open parenthesis	∧ and
) close parenthesis	∨ or
/ slant	¬ not
* asterisk	↱ arrow right
, comma	↑ arrow up
≠ not equal	↓ arrow down
$ dollar	≡ identity
: colon	% percent
blank	[open bracket
	] close bracket
	; semicolon

Note: For business applications ~ % $ replace ∧ ∨ ¬

§ 081.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . continuous fanfold sprocket-punched stationery.
.312 Phenomenon: . . . . . printing of engraved chars.

.32 Positional Arrangement

.321 Serial by: . . . . . . one line at 6 lines/inch.
.322 Parallel by: . . . . . 120 columns at 10 chars/inch.
.323 Bands: . . . . 1.
.324 Track use: . . . . . . all for data.
.325 Row use: . . . . . . all for data.

.33 Coding: . . . . as in Data Code Table No. 1.

.34 Format Compatibility: . . . . none.

.35 Physical Dimensions

.351 Overall width: . . . . 4 to 19 inches.
.352 Length: . . . . up to a 17 inch form.
.353 Maximum margins
Left: . . . . 3.5 inches.
Right: . . . . 3.5 inches.

.4 CONTROLLER

.41 Identity: . . . . Print Control Unit.

.42 Connection to System

.421 On-line: . . . . 24.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 120 characters.
.442 Input-output areas: . . core storage; 1 char per word, in 6 low-order bit positions.
.443 Input-output area access: . . . . . . each word.
.444 Input-output area lockout: . . . . . . none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . one line of 120 characters.
.512 Block demarcation
Output: . . . . address limits in instruction.

.52 Input-Output Operations

.521 Input: . . . . none.
.522 Output: . . . . print one line.
.523 Stepping: . . . . print and step 0, 1 or 2 lines.
step 1 or 2 lines.
.524 Skipping: . . . . . . 8 levels of skipping are possible.
skipping is controlled by a tape loop.
.525 Marking: . . . . . . none.

.53 Code Translation: . . automatic translation from internal BCD code as in Data Code Table No. 1.

.54 Format Control: . . . none.

.55 Control Operations

Disable: . . . . no.
Request interrupt: . . yes.
Select format: . . . . no.
Select code: . . . . . no.

.56 Testable Conditions

Printer ready: . . . . provided power is on, 1604 is selected, paper is not in motion, and printer is not out of paper.
Printer not ready: . . if power is off, or 1604 is not selected, or paper is in motion, or printer is out of paper.

.6 PERFORMANCE

.61 Conditions

I A: . . . . restricted FORTRAN set, print drum 1,000 rpm.
I B: . . . . restricted FORTRAN set, print drum 667 rpm.
II A: . . . . full character set, print drum 1,000 rpm.
II B: . . . . full character set, print drum 667 rpm.

.62 Speeds

.621 Nominal or peak speeds
I A: . . . . 1,000 lines/min.
II A: . . . . 500 lines/min.
I B: . . . . 667 lines/min.
II B: . . . . 333 lines/min.
.622 Important parameters
Paper speed: . . . . 25 inches/sec., max.
9,000 lines/min., max.
Line length: . . . . 120 columns.
Line spacing: . . . . 6 lines/inch.
Character spacing: . 10 chars/inch.
Drum cycle, I A & II A: 60 m. sec.
Drum cycle, I B & II B: 90 m. sec.
623 Overhead: . . . . . . single clutch point.

§ 081.

.624 Effective speeds

I A:	1,000/ (1+ [(N + 6)/9]) lines/min.
II A:	1,000/(2+ [N/9]) lines/min.
I B:	667/ (1+ [(N + 6)/9]) lines/min.
II B:	677/ (2+ [N/9]) lines/min.
N:	interline spacing in lines. Note: [x] means "integer part of x."

These are shown graphically at end of the section.

.63 Demands on System

Component	Condition	m.sec per line	or	Percentage
Processor:	I A	0.384		0.6
	II A	0.384		0.3
	I B	0.384		0.4
	II B	0.384		0.2

This is based on a full line of 120 characters. It would be proportionately less for shorter lines measured from the left margin. The time taken in setting the data in storage is not taken into account.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method	Comment
Character phasing:	knob	performs fine adjustments of print quality to correspond to motor speed selection.
Penetration control:	knob	adjusts hammer mounting plate print cylinder gap to accomodate different thicknesses of paper.
Form positioning:	knob	adjusts line of print on form.
Paper tension:	knob	adjusts paper tension.

.71 Adjustments (Contd.)

Adjustment	Method	Comment
Top of form:	button	moves to top of form under control of format channel 8.
Single line feed:	button	advances paper.
Paper tractor adjustment:	adjustable form tractor	provides horizontal positioning for paper widths of 4 to 19 inches.

.72 Other Controls

Function	Form	Comment
Motor Speed:	switch	selects print drum speed of either 1,000 or 667 rpm.
Printer Ready:	combination button-lamp	indicates that printer is "ready."
160/1604 Selector Switch:	switch	selects the correct inputs for 1604-A or 160 computer.

.73 Loading and Unloading

.731 Volumes handled: . . . paper stack 12 to 14 inches high.

.732 Replenishment time: . 1 min. printer must be stopped.

.733 Adjustment time: . . . 1 to 3 mins.

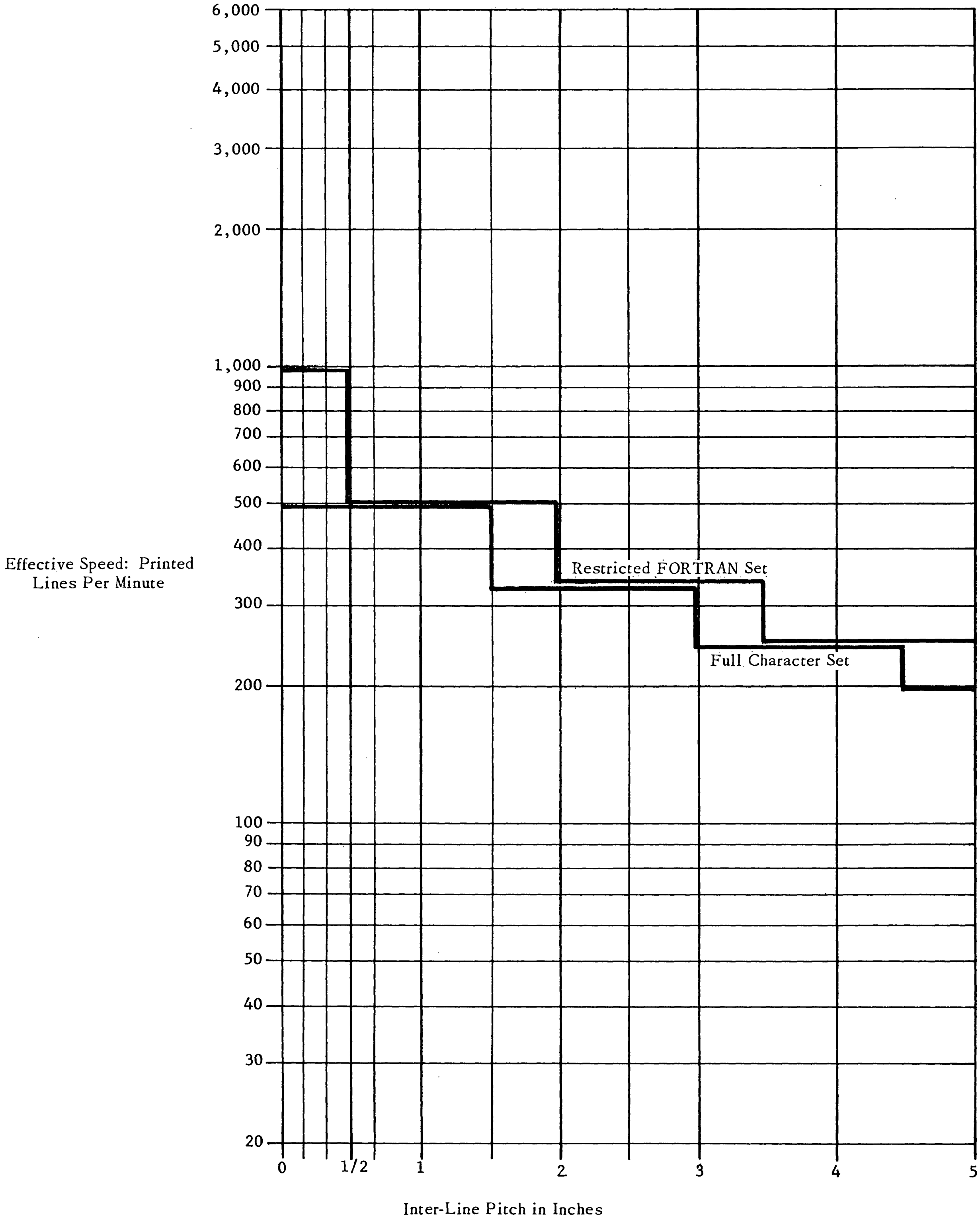
.734 Optimum reloading period: . . . . . 34 mins.
Basis: using 1,000 17-inch 2-part forms, printing full character set, 1 line every inch.

.8 ERRORS, CHECKS AND ACTION:

Error	Check or Interlock	Action
Recording:	none.	
Output block size:	none.	
Invalid code:	all codes valid.	
Exhausted medium:	micro-switch check	stop printer.
Imperfect medium:	micro-switch check	stop printer.

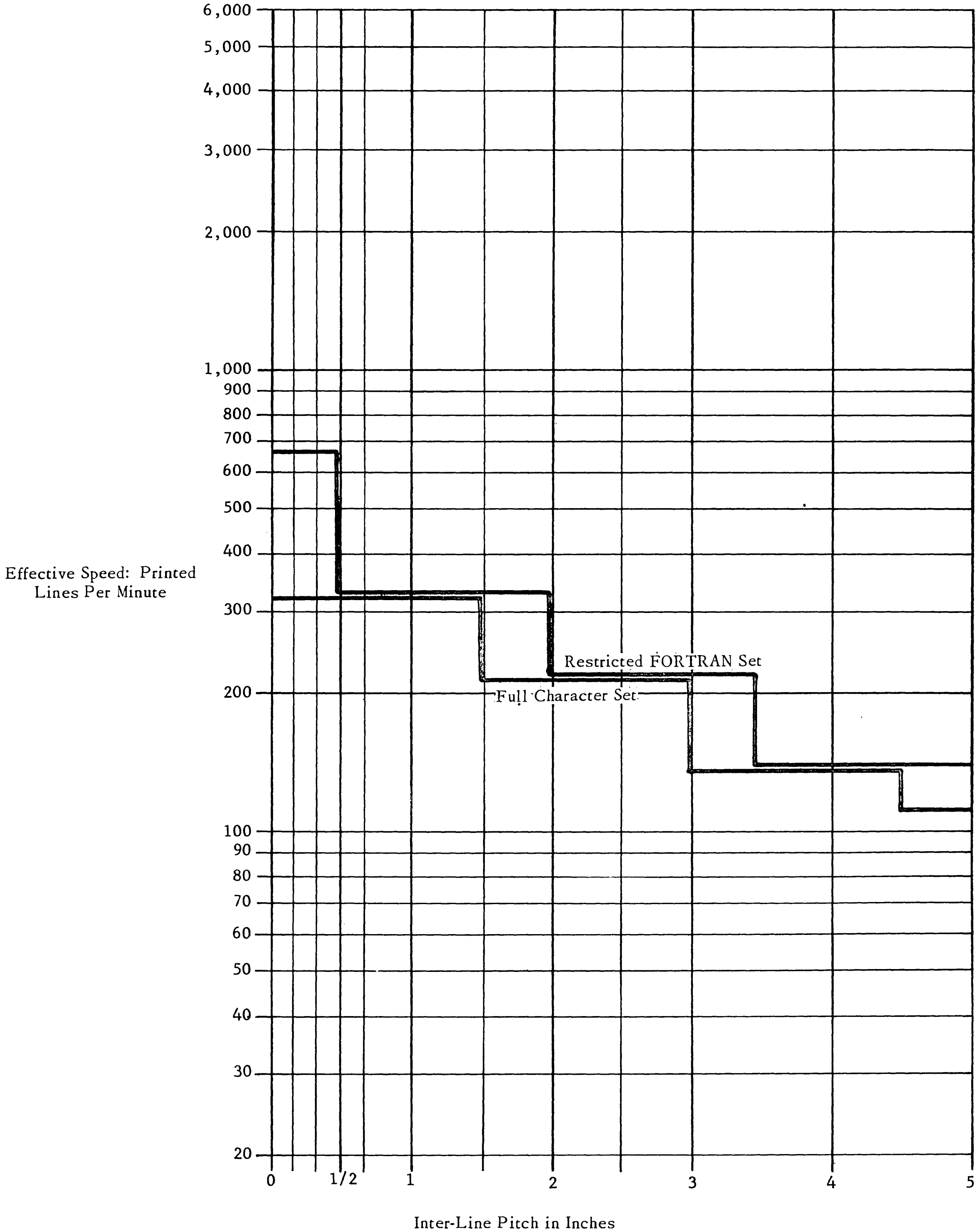
EFFECTIVE SPEED
CDC 1612 PRINTER

Condition: Print cylinder revolving at 1,000 r.p.m.



EFFECTIVE SPEED
CDC 1612 PRINTER

Condition: Print cylinder revolving at 667 r.p.m.



INPUT-OUTPUT: CDC 606 MAGNETIC TAPE UNIT

§ 091.

.1 GENERAL

.11 Identity: . . . . Magnetic Tape Unit. CDC 606.

.12 Description

The CDC 606 Magnetic Tape Unit provides the following facilities under program control.

While writing:
(1) Packing density either 200 or 556 rows per inch.
(2) Binary or BCD coding.
(3) Interrupt on either next error, or when ready.
(4) Skip bad spot.
(5) Write end-of-file mark.
(6) Rewind with or without interlock.

While reading:
(1) Binary or BCD coding.
(2) Read one file, or one record.
(3) Skip one file or one record, forward or backward.
(4) Interrupt on either next error or when ready.
(5) Rewind with or without interlock.

At any time, individual sense instructions can be used to test for the following conditions:
(1) Parity Error.
(2) Length Error.
(3) End-of-tape mark sensed.
(4) Tape positioned at Load Point.
(5) Interrupt requested on unit.
(6) Unit available.
(7) Certain types of program error have occurred and have been suppressed (e.g., read selection while writing is in progress).

The CDC 606 Magnetic Tape Unit, controlled by the CDC 1615 Control Unit, forms a magnetic tape system which can be attached to one or two computers. If attached to two computers, such as a CDC 1604-A and a CDC 160-A, control can be switched manually or by program from one computer to the other.

The 606 has a peak data rate of 83,400 characters per second. At this peak speed, one 606 requires 3.3 percent of the 1604-A running time. Any 1615 Control Unit can operate on two channels simultaneously and if three controllers are present, the maximum of six tape units can operate simultaneously at this peak speed. The total load on the central processor is 20 percent, and the character rate is 500,400. No restrictions in the number (up to six) of I/O units operating simultaneously are necessary, provided no faster I/O unit is attached. This is one of the major differences between the CDC 1604 and CDC 1604-A.

.12 Description (Contd.)

The tapes are completely compatible with IBM 729 written tapes having densities of either 200 or 556 characters per inch. Both CDC and IBM tape units are similar except that the CDC uses pneumatic capstans instead of pinch rollers. Reading and writing can only be done in a forward direction; searching for EOT, and rewinding can be done in either direction. The maximum rewind time of a 2,400 foot tape is 80 seconds.

Data is stored in the computer in multiples of eight characters; i.e., sets of full words. If a block being read from tape does not fill an exact number of words, the least significant end of the last word is filled with zeroes before being put into the core storage. If this occurs, a length error is recorded, and program examination of the Buffer Control Word can determine the cause. However, it is not possible to determine how many zeroes have been incorporated in the record. The adding of zeros will never occur when tapes written on the CDC 1604 or CDC 1604-A are being used, but may occur when tapes written on other machines (including the CDC 160 and 160-A) are used.

.13 Availability: . . . . . . 2 to 4 months.

.14 First Delivery: . . . . August, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pneumatic capstan.
.212 Reservoirs
Number: . . . . 2.
Form: . . . . vacuum.
Capacity: . . . . each about 7 feet.
.213 Feed drive: . . . . . . motor.
.214 Take-up drive: . . . . . motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.
.222 Sensing system: . . . . magnetic head.
.223 Common system: . . . two heads.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . 1.

Use of station: . . . . . recording.
Distance: . . . . 0.4375 inches.
Stacks: . . . . 1.
Heads/stack: . . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . sensing.
Distance: . . . . 0.3 inch.
Stacks: . . . . 1.
Heads/stack: . . . . . . 7.
Method of use: . . . . . 1 row at a time.

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.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . plastic tape with magnetizable surface.
.312 Phenomenon: . . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . 1 to N rows at 200 or 556 rows/inch.
.322 Parallel by: . . . . . . 7 tracks.
.324 Track use
Data: . . . . 6.
Redundancy check: . . 1.
Timing: . . . . 0 (self clocking).
Control signals: . . . 0.
Unused: . . . . 0.
Total: . . . . 7.
.325 Row use
Data: . . . . 1 to N.
Redundancy check: . . 1.
Timing: . . . . 0.
Control signals: . . . 0 (record and segment marks are optional).
Unused: . . . . 0.
Cap: . . . . 0.75 inch inter-block gap. 6.0 inch end-of-file mark.

.33 Coding: . . . . BCD mode; one tape row per character as in Data Code Table No. 3, even parity.

.34 Format Compatibility: . IBM BCD and binary codes at 200 and 556 rows per inch.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.50 inches.
.352 Length: . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . Control Unit 1615.

.42 Connection to System

.421 On-line: . . . . 6.
.422 Off-line: . . . . can be switched manually or by program between main and satellite computers.

.43 Connection to Device: . up to 8 per 1615.

.44 Data Transfer Control

.441 Size of load: . . . . . . 1 to N words, limited by available core storage.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . each word.
.444 Input-output area lockout: . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 to N words, limited by available core storage; 8 rows per word.
.512 Block demarcation
Input: . . . . gap on tape or cut-off specified in buffer control word.
Output: . . . . cut-off specified in buffer control word.

.52 Input-Output Operations

.521 Input: . . . . 1 block or file forward, with cut-off available at N words; zeros fill in the last word.
.522 Output: . . . . 1 block forward of N words.
.523 Stepping: . . . . none.
.524 Skipping: . . . . 1 block or file forward. 1 block or file backward. erase 3.5 inches forward (to skip defective tape areas).
.525 Marking: . . . . end-of-file mark, preceded by an automatic six-inch gap, followed by a longitudinal parity character and the regular interblock gap.
.526 Searching: . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . . none.

.55 Control Operations

Disable: . . . . only by unload.
Request interrupt: . . . yes, either for error or when free.
Select format: . . . . . no.
Select code: . . . . . . yes, binary mode or BCD mode.
Rewind: . . . . yes.
Unload: . . . . yes.

.56 Testable Conditions

Disabled: . . . . no.
Busy device: . . . . . . yes.
Output lock: . . . . . . yes.
Nearly exhausted: . . . yes, end-of-tape mark indicates a minimum of 8 feet remaining (approx. 20,000 chars).
Busy controller: . . . . no.
End of medium marks: end-of-tape mark (reflective spot). load point.
Ready to read: . . . . . yes.
Ready to write: . . . . yes.
Error condition: . . . . parity or length error separately.
Interrupt condition: . . whether selected to interrupt.

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.6 PERFORMANCE

.61 Conditions

I: . . . . high density (556 char/inch).
II: . . . . low density (200 char/inch).

.62 Speeds

Condition	I	II
.621 Nominal or peak speeds:	83,400	30,000.
.622 Important parameters Name		
Density:	556 char/inch	200 char/inch.
Start or stop time: .	max 4 m. sec	max 4 m. sec.
Full rewind time: . .	1.3 min.	1.3 min.
Interblock gap: . . .	0.75 inch	0.75 inch.
.623 Overhead:	max 8 m. sec/block	max 8 m. sec/block.
.624 Effective speed, characters/sec: . . .	83,400N/(N+698) (See Graph)	30,000N/(N+240).

.63 Demands on System

Component	Condition	m. sec per word	or	Percentage
Processor:	I	.0032		3.3.
Processor:	II	.0032		1.2.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . . recording density.
Method: . . . . switch.
Comment: . . . . selects high or low density, but is overridden by program changes.

.72 Other Controls

Function	Form	Comment
Unit Number Selector:	dial	select 1 of 8 addresses.
File protection ring:	plastic ring affixed to tape reel	absence of ring inhibits tape writing.
Load Point:	button	lowers tape into reservoirs and winds tape forward to load point.
Unload:	button	removes tape from reservoirs and raises upper portion of head assembly.

.73 Loading and Unloading

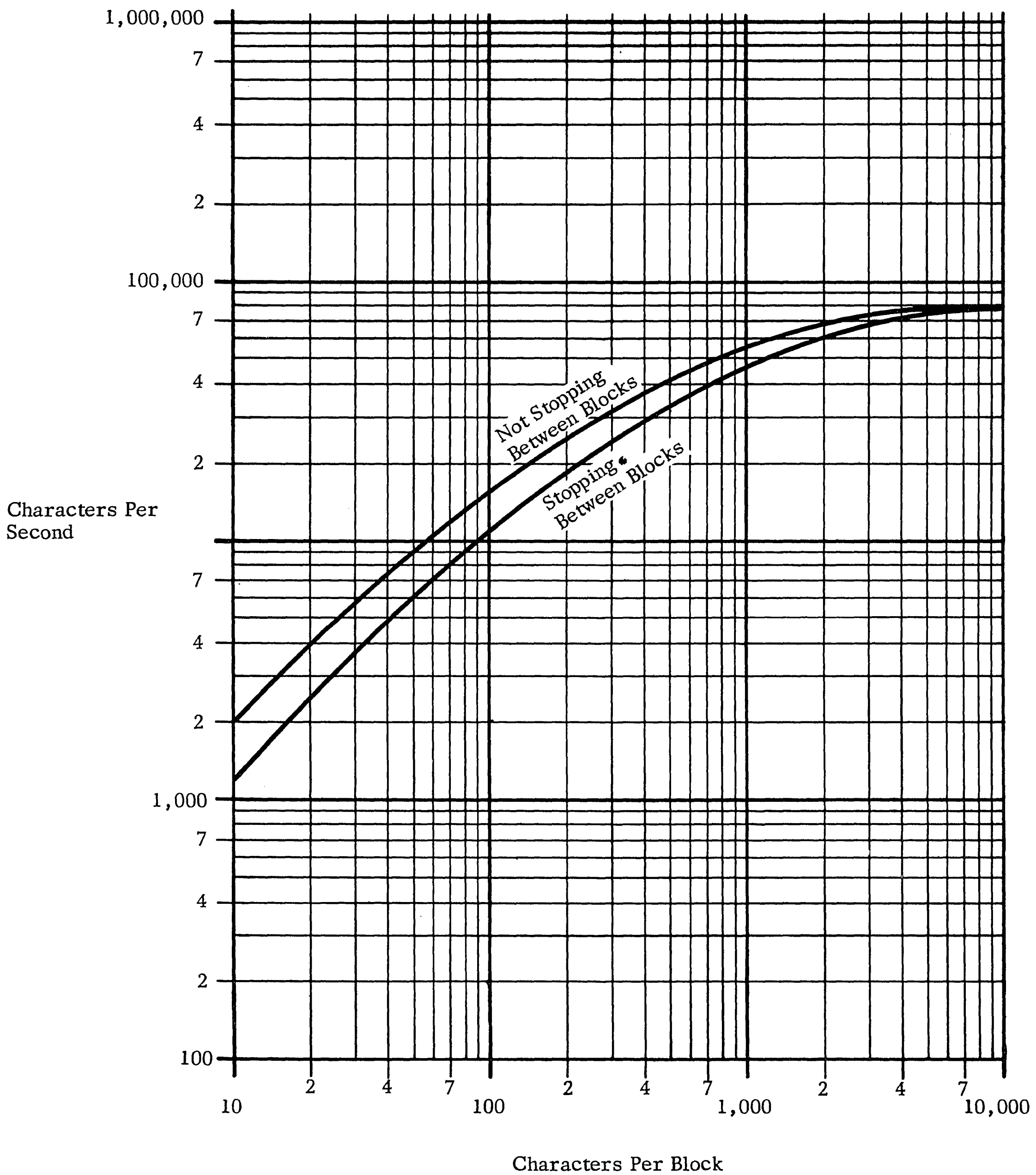
.731 Volumes handled
Storage: . . . . reel.
Capacity: . . . . 2,400 feet; for 1,000 char blocks, 5,000,000 at 200 char/inch; 11,300,000 chars at 556 char/inch.
.732 Replenishment time: . . 1.0 to 1.5 minutes.
.734 Optimum reloading period: . . . . 4 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read after write with lateral parity check	indicator, alarm and program sense.
Reading:	lateral and longitudinal parity checks	indicator, alarm and program sense.
Input area overflow:	check	stop transfer, set counter.
Output block size:	present.	
Invalid code:	all codes valid	stalls computer.
Exhausted medium:	reflective spot on tape	programmed sense.
Imperfect medium:	none.	
Timing conflicts:	none.	
Parity error:	check	programmed sense.

§ 091.

EFFECTIVE SPEED
CDC 606



INPUT-OUTPUT: 1610-A CONTROL UNIT

§ 101.

.1 GENERAL

.11 Identity: . . . . Control Unit. 1610-A.

.12 Description

The CDC 1610-A Control Unit contains independent input and output connections which can link a group of IBM peripheral units to either the CDC 1604, 1604-A, 160, or 160-A computers. In the case where a 1604 or 1604-A is operating in conjunction with a CDC 160 or 160-A, the CDC 1610-A and its associated units can be switched manually, but not by program, from one computer to the other.

The CDC works in row binary; that is, it treats a card as containing twelve 80-bit words. Cards punched in column binary or Binary Coded Decimal require programmed conversion.

In the input mode the 1610 can operate one:

- IBM 88 High Speed Collator, used as a card reader; either one or both independent card feeds at 650 cards per minute individually or 1, 300 cards per minute jointly; or one feed with a second read station at 650 cards per minute.
- IBM 533 Card Read Punch, used as a card reader at 200 cards per minute.

.12 Description (Contd.)

In the output mode it can operate one:

- IBM 533 Card Read Punch, used as a card punch at 100 cards per minute.
- IBM 407 Accounting Machine, used as a line printer at 150 lines per minute.
- IBM 523 Gang Summary Punch, used as a card punch at 100 cards per minute.

The printer, either punch and either card reader can be physically connected at one time, and each may be separately addressed. The IBM 88 and 407 units may be used in their normal off-line manner. No gang or summary punch is available with either the 523 or 533. On-line control of the 88, 407 and 523 by the computer requires modification of the control panels so that each unit is wired in the CALCULATE ON state (the 533 is wired directly and has no provision for control panel modifications).

All data transfers correspond to a card image. Each 80-bit row of a card corresponds to the least significant 40-bit patterns of two computer words. The information on a card, therefore, is stored in 24 core storage locations (as opposed to 10 words when BCD format is used).

All external function code instructions relevant to the 1604-A computer are listed in Section :121.

.13 Availability: . . . . . 2 months.

.14 First Delivery: . . . . 1961.

SIMULTANEOUS OPERATIONS

§ 111.

.1 SPECIAL UNITS

.11 Identity: . . . . incorporated in central processor.

.12 Description

A 1604-A computer contains seven input-output channels. Six of these channels are arranged in pairs of one for input and one for output. These three pairs are used for the input-output devices and are fully buffered. The seventh channel is not buffered and requires central processor control.

Logically, up to eight controllers can be connected to each pair of channels, and up to eight devices can be connected to some controllers; however, power supply considerations impose lower practical limits on many combinations.

Each channel operates independently during data transfers between an input-output device and a block of locations in the store.

Magnetic tape rewind and paper advance are independent operations.

The CDC 1604-A has an Auxiliary Sequence Control which controls single word transfers betweeen core storage and the buffered input-output channels. This, unlike the CDC 1604, is independent of the instruction sequence. Provided no unit with a transfer rate of greater than 125,000 characters per second is attached, there are no limitations to the simultaneity of the input-output units; that is, the CDC 1604-A can simultaneously compute, input from three channels, and output to three channels.

.2 CONFIGURATION CONDITIONS: . . . . . none.

.3 CLASSES OF OPERATIONS

Class	Members
A:	internal processing.
B:	transmit output data to any one device connected with channels 2, 4, 6.
C:	transmit input data from any one device connected with channels 1, 3, 5.
D:	transmit output data on channel 7.
E:	transmit input data on channel 7.
F:	paper advance. magnetic tape rewind.

.4 RULES

a + d + e = at most 1.
b = at most 3.
c = at most 3.
f = at most N.

N = number of appropriate devices attached.

INSTRUCTION LIST

§ 121.

INSTRUCTION†				OPERATION
OP	Index Designator	Addr.	Octal Code	
				Arithmetic
ADD	b	m	14------	(A) + (M) ⟶ A
SUB	b	m	15------	(A) - (M) ⟶ A
MUI	b	m	24------	(A) x (M) ⟶ QA; least significant portion in A
DVI	b	m	25------	(QA) ÷ (M) ⟶ A; remainder ⟶ Q; Sign of Q must be preset to the sign of A
MUF	b	m	26------	(A) x (M) ⟶ AQ; least significant portion in Q.
DVF	b	m	27------	(AQ) ÷ (M) ⟶ A; remainder ⟶ Q; if A is zero, it must be preset to the sign of Q
RAD	b	m	70------	(M) + (A) ⟶ A ⟶ M
RSB	b	m	71------	(M) - (A) ⟶ A ⟶ M
RAO	b	m	72------	(M) + 1 ⟶ A ⟶ M
RSO	b	m	73------	(M) - 1 ⟶ A ⟶ M
INA	b	y	11------	Y + (A) ⟶ A, Y is a 14-bit plus sign literal in the y field of the instruction
INI	b	y	51------	Y + (B^b) ⟶ B^b; if the b designator has a zero value then this instruction becomes a pass, or do nothing
ENA	b	y	10------	Y ⟶ (A)
ENQ	b	y	04------	Y ⟶ (Q)
ENI	b	y	50------	Y ⟶ (B^b)
				Floating Point Arithmetic
FAD	b	m	30------	(A) + (M) ⟶ A rounded; rounding residue ⟶ Q
FSB	b	m	31------	(A) - (M) ⟶ A rounded; rounding residue ⟶ Q
FMU	b	m	32------	(A) x (M) ⟶ A rounded; rounding residue ⟶ Q
FDV	b	m	33------	(A) ÷ (M) ⟶ A rounded; rounding residue ⟶ Q
SCA	b	k	34------	A left until $(A_{47}) \neq (A_{46})$ or K = 0 Reduce K by one per shift; $K_{final} \longrightarrow B^b$
SCQ	b	k	35------	AQ left until $(A_{47}) \neq (A_{46})$ or K = O Reduce K by one per shift; $K_{final} \longrightarrow B^b; O \leq K \leq 77777_8$
				Logic
SST	b	m	40------	Set (A_n) = 1 for (M_n) = 1
SCL	b	m	41------	Clear (A_n) to zero for (M_n) = 1
SCM	b	m	42------	Complement (A_n) for (M_n) = 1
SSU	b	m	43------	$(M_n) \longrightarrow A_n$ for (Q_n) = 1
LDL	b	m	44------	Logical product of (Q) and (M) ⟶ A
ADL	b	m	45------	(A) + [logical product of (Q) and (M)] ⟶ A
SBL	b	m	46------	(A) - [logical product of (Q) and (M)] ⟶ A
STL	b	m	47------	Logical product of (A) and (Q) ⟶ M
				Logic Shift
ARS	b	k	01------	Shift (A) right K binary places; sign bit is extended to the right.
QRS	b	k	02------	Shift (Q) right K binary places; sign bit is extended to the right.
LRS	b	k	03------	Shift (AQ) right K binary places; sign bit of A is extended to the right, lowest order bits of A shift into highest order bits of Q.
ALS	b	k	05------	Circular shift (A) left K binary places.
QLS	b	k	06------	Circular shift (Q) left K binary places.
LLS	b	k	07------	Circular shift (AQ) left K binary places.

† For definition of symbols used, see Instruction List Nomenclature at end of Instruction Listing.

INSTRUCTION LIST–Contd.

§121.

INSTRUCTION †				OPERATION
OP	Index Designator	Addr.	Octal Code	
				Data Transfers
LDA	b	m	12------	(M)⟶ A
LAC	b	m	13------	Complement of (M)⟶ A
LDQ	b	m	16------	(M)⟶ Q
LQC	b	m	17------	Complement of (M)⟶ Q
STA	b	m	20------	(A)⟶ M
STQ	b	m	21------	(Q)⟶ M
LIU	b	m	52------	(M_{38-24})⟶B^b; the upper address of file M replaces the contents of the indicated index register.
LIL	b	m	53------	(M_{14-0})⟶ B^b; the lower address field of M replaces the contents of the indicated index register.
SIU	b	m	56------	(B^b)⟶ M_{38-24}; store the contents of the designated index register into the upper address field of M.
SIL	b	m	57------	(B^b)⟶M_{14-0}; store the contents of the designated index register into the lower address field of M.
SAU	b	m	60------	(A_{00-14})⟶M_{38-24}
SAL	b	m	61------	(A_{00-14})⟶M_{00-14}
				Branching - no indexing
AJP	j	m	220-----	Jump to M if (A) = 0 i.e., positive or negative zero.
AJP	j	m	221-----	Jump to M if (A) ≠ 0.
AJP	j	m	222-----	Jump to M if (A) is positive.
AJP	j	m	223-----	Jump to M if (A) is negative.
AJP	j	m	224-----	Return Jump to M if (A) = 0.
AJP	j	m	225-----	Return Jump to M if (A) ≠ 0.
AJP	j	m	226-----	Return Jump to M if (A) is positive.
AJP	j	m	227-----	Return Jump to M if (A) is negative.
QJP	j	m	230-----	Jump to M if (Q) = 0.
QJP	j	m	231-----	Jump to M if (Q) ≠ 0.
QJP	j	m	232-----	Jump to M if (Q) is positive.
QJP	j	m	233-----	Jump to M if (Q) is negative.
QJP	j	m	234-----	Ruturn Jump to M if (Q) = 0.
QJP	j	m	235-----	Return Jump to M if (Q) ≠ 0.
QJP	j	m	236-----	Return Jump to M if (Q) is positive.
QJP	j	m	237-----	Return Jump to M if (Q) is negative.
SLJ	j	m	750-----	Jump to M unconditionally.
SLJ	j	m	751-----	Jump to M if lever key 1 is set; lever keys are on the console.
SLJ	j	m	752-----	Jump to M if lever key 2 is set.
SLJ	j	m	753-----	Jump to M if lever key 3 is set.
SLJ	j	m	754-----	Return Jump to M: unconditionally.
SLJ	j	m	755-----	Return Jump to M if lever key 1 is set.
SLJ	j	m	756-----	Return Jump to M if lever key 2 is set.
SLJ	j	m	757-----	Return Jump to M if lever key 3 is set.
SLS	j	m	760-----	Stop Unconditionally
SLS	j	m	761-----	Stop if Stop Key 1 is set } and { if the Console Run-Stop Key is
SLS	j	m	762-----	Stop if Stop Key 2 is set } and { in the step condition; otherwise,
SLS	j	m	763-----	Stop if Stop Key 3 is set } and { Jump to M.
SLS	j	m	764-----	Stop Unconditionally
SLS	j	m	765-----	Stop if Stop Key 1 is set } and { if the Console Run-Stop Key is
SLS	j	m	766-----	Stop if Stop Key 2 is set } and { in the step condition; otherwise,
SLS	j	m	767-----	Stop if Stop Key 3 is set } and { Return Jump to M.

† For definition of symbols used, see Instruction List Nomenclature at end of Instruction Listing.

INSTRUCTION LIST–Contd.

§ 121.

INSTRUCTION †				OPERATION
OP	Index Designator	Addr.	Octal Code	
				Branching on Index
ISK	b	y	54------	if (B^b) = Y; Clear B^b and Exit to the Upper Instruction of the next storage word. if $(B^b) \neq$ Y; $(B^b) + 1 \longrightarrow B^b$ and Half Exit, advance to the lower instruction. if no Index Register is indicated (b = 0 or 7) then a Half Exit is taken. ISK is normally restricted to the upper instruction.
IJP	b	m	55------	if $(B^b) \neq 0$; $(B^b) - 1 \longrightarrow B^b$, Jump to M. if $(B^b) = 0$; Continue.
				Branching on Storage
SSK	b	m	36------	if (M) is negative; Full Exit. if (M) is positive; Half Exit.
SSH	b	m	37------	Shift (M) circularly left one bit, then if $(M_{00}) = 1$; Full Exit if $(M_{00}) = 0$; Half Exit.
				Branching on Storage Search
				In the following instructions if b = 0, only the word at storage location M is searched. if b = 7, indirect addressing is used to obtain the execution address and the b designator. if $(B^b) = 0$, no search is made. Search (B^b) words starting with the last address M + (B^b) -1; reduce (B^b) by one, continue search until condition specified is met or search is exhausted.
ESQ	b	m	64------	If $(M + (B^b) - 1) = (A)$, Full Exit. If search is exhausted, Half Exit. Positive zero and negative zero are recognized as the same quantity.
THS	b	m	65------	If $(M + (B^b) - 1) > (A)$, Full Exit. If search is exhausted, Half Exit. Positive zero is greater than negative zero.
MEQ	b	m	66------	If the logical product of (Q) and $(M + (B^b) - 1) = (A)$, Full Exit. If search is exhausted, Half Exit.
MTH	b	m	67------	If the logical product of (Q) and $(M + (B^b) - 1) > (A)$, Half Exit.
				Input-Output
INT	b	m	62------	Transfer (B^b) words from an external equipment into memory, beginning at the last address, M + (B^b) - 1.
OUT	b	m	63------	Transfer to an external equipment (B^b) words from memory beginning at the last address, M + (B^b) - 1.
				External Functions
				See Instruction List Appendix for the large variety of operations provided. They are specified by considering "m" as three parts: Channel -- one octal digit Equip. No -- one octal digit Operation -- three octal digits and the Index Designator as: Select/Sense -- one octal digit

† For definition of symbols used, see Instruction List Nomenclature, at end of Instruction Listing.

INSTRUCTION LIST NOMENCLATURE

Symbol	Definition
A:	Accumulator.
b:	Index Designator.
B^b:	designated index register.
j:	condition designator for jump and stop instructions.
k:	unmodified count.
K:	modified count; $K = k + (B^b)$.
m:	unmodified operand address.
M:	modified operand address; $M = m + (B^b)$.
y:	unmodified operand.
Y:	modified operand; $Y = y + (B^b)$.
( ):	contents of a register or storage location.

INSTRUCTION LIST APPENDIX

§ 121 EXTERNAL FUNCTIONS

INSTRUCTION OP EXF	Index Select/Sense	Address Channel	Equip. No.	Sub-Operation	OPERATION
74	0 or 7	1 to 6	0 to 7	000 to 777	
	INTERRUPTS AND REAL TIME CLOCK				SELECT INTERNAL
74	0	0	0	0C0	Interrupt on Channel C inactive.
74	0	0	0	0C1	Remove Interrupt Selection on Channel C.
74	0	C	0	000	Clear all Channel C Selection C = channel = 1 - 6.
74	0	0	0	100	Interrupt on Arithmetic Faults.
74	0	0	0	101	Remove Interrupt on Arithmetic Faults.
74	0	0	1	000	Start Real-Time Clock.
74	0	0	2	000	Stop Real-Time Clock.
74	0	0	0	070	Clear Arithmetic Faults.
					SENSE INTERNAL
74	7	0	0	0C0	Exit on Channel C active.
74	7	0	0	0C1	Exit on Channel C inactive C = channel = 1 - 6.
74	7	0	0	1A0	Exit on Arithmetic Fault A.
74	7	0	0	1A1	Exit on no Arithmetic Fault A. A = 1: Divide = 2: Shift = 3: Overflow = 4: Exponent
	CONSOLE EQUIPMENT				SELECT (Using Console Equipment)
					Input
74	0	1	1	140	Select Typewriter for Input, and Interrupt on Carriage Return.
74	0	1	1	100	Select Typewriter for Input, and No Interrupt on Carriage Return.
74	0	1	1	200	Select Paper Tape Reader, and No Interrupt on End of Tape.
74	0	1	1	210	Select Paper Tape Reader, and Set End of Tape Indicator.
74	0	1	1	220	Select Paper Tape Reader, and Interrupt on End of Tape.
					Output
74	0	2	1	100	Select Typewriter for Output, Assembly Mode.
74	0	2	1	110	Select Typewriter for Output, Character Mode.
74	0	2	1	200	Select Paper Tape Punch, Assembly Mode.
74	0	2	1	210	Select Paper Tape Punch, Character Mode.
74	0	2	1	240	Turn Paper Tape Punch Motor Off.
					SENSE (Using Console Equipment)
					Input
74	7	1	1	200	Exit on Paper Tape Reader, End of Tape.
74	7	1	1	201	Exit on Paper Tape Reader, No End of Tape.
74	7	1	1	210	Exit on Paper Tape Reader in Assembly Mode.
74	7	1	1	211	Exit on Paper Tape Reader in Character Mode.
74	7	1	1	140	Exit on Typewriter in Lower Case.
74	7	1	1	141	Exit on Typewriter in Upper Case.
74	7	1	1	100	Exit on Carriage Return from Typewriter.
74	7	1	1	101	Exit on No Carriage Return from Typewriter.
					Output
74	7	2	1	200	Exit on Paper Tape Punch Out of Tape.
74	7	2	1	201	Exit on Paper Tape Punch Not Out of Tape.

§ 121.

INSTRUCTION LIST APPENDIX–Contd.

INSTRUCTION					OPERATION
OP	Index	Address			
EXF	Select/Sense	Channel	Equip. No.	Sub-Operation	
74	0 or 7	1 to 6	0 to 7	000 to 777	
CDC 1610-A CARD CONTROL UNIT					SELECT (Using CDC 1610-A Control Unit)
					Input
74	0	1	4	001	Select Primary Read Station.
74	0	1	4	002	Select Secondary Read Station.
74	0	1	4	003	Select Primary and Secondary Read Stations.
74	0	1	4	005	Select Primary Read Station and Interrupt.
74	0	1	4	006	Select Secondary Read Station and Interrupt.
74	0	1	4	007	Select Primary and Secondary Read Stations and Interrupt.
					Output
74	0	2	4	001	Select Printer.
74	0	2	4	002	Select Punch.
74	0	2	4	005	Select Printer and Interrupt.
74	0	2	4	006	Select Punch and Interrupt.
					SENSE (Using CDC 1610-A Control Unit)
					Input
74	7	1	4	002	Exit on Reader Ready.
74	7	1	4	003	Exit on Reader Not Ready.
74	7	1	4	004	Exit on 1604 Selected.
74	7	1	4	005	Exit on 1604 Not Selected.
					Output
74	7	2	4	002	Exit on Printer Ready.
74	7	2	4	003	Exit on Printer Not Ready.
74	7	2	4	004	Exit on Punch Ready.
74	7	2	4	005	Exit on Punch Not Ready.
74	7	2	4	010	Exit on 1604 Selected.
74	7	2	4	011	Exit on 1604 Not Selected.
CDC 1612 PRINTER					SELECT (Using CDC 1612 Printer).
					Output Only
74	0	2	6	000	Select Printer.
74	0	2	6	001	Single Space the Printer.
74	0	2	6	002	Double Space the Printer.
74	0	2	6	003	Select Format Channel 7.
74	0	2	6	004	Select Format Channel 8.
74	0	2	6	010	Clear Monitor Channels 1 - 6.
74	0	2	6	01N	Select Monitor Channel N: N = 1 - 6.
					SENSE (Using CDC 1612 Printer)
					Output Only
74	7	2	6	000	Exit on Printer Ready.
74	7	2	6	001	Exit on Printer Not Ready.

INSTRUCTION LIST APPENDIX—Contd.

§ 121.

INSTRUCTION					OPERATION
OP	Index	Address			
EXF	Select/Sense	Channel	Equip. No.	Sub-Operation	
74	0 or 7	1 to 6	0 to 7	000 to 777	
CDC 1615 MAGNETIC TAPE CONTROL UNIT					
					Output
74	0	C	2	0N1	Select Tape N to Write Binary.
74	0	C	2	0N2	Select Tape $\overline{N}$ to Write Coded.
74	0	C	2	001	Prepare Selected Tape to Write Binary.
74	0	C	2	002	Prepare Selected Tape to Write Coded.
74	0	C	2	003	Write End-Of-File Mark on Selected Tape.
74	0	C	2	004	Select Interrupt When Write Tape Next Ready.
74	0	C	2	005	Rewind Selected Write Tape.
74	0	C	2	006	Backspace Selected Write Tape.
74	0	C	2	007	Rewind-Unload Selected Write Tape.
74	0	C	2	400	Clear Interrupt Selections on Write Tape.
74	0	C	2	401	Set Low Density on Selected Write Tape.
74	0	C	2	402	Set High Density on Selected Write Tape.
74	0	C	2	403	Skip Bad Spot on Selected Write Tape.
74	0	C	2	404	Select Interrupt on Next Error.
					SENSE
74	7	C	2	000	Exit on Ready to Write.
74	7	C	2	001	Exit on Not Ready to Write.
74	7	C	2	002	Exit on Write Reply Parity Error.
74	7	C	2	003	Exit on No Write Reply Parity Error.
74	7	C	2	004	Exit on Write Reply Length Error.
74	7	C	2	005	Exit on No Write Reply Length Error.
74	7	C	2	006	Exit on End-of-Tape Marker.
74	7	C	2	007	Exit on Not End-of-Tape Marker.
74	7	C	2	400	Exit on Ready to Select.
74	7	C	2	401	Exit on Not Ready to Select.
74	7	C	2	402	Exit on Load Point.
74	7	C	2	403	Exit on Not Load Point.
74	7	C	2	404	Exit on Interrupt on Write Tape.
74	7	C	2	405	Exit on No Interrupt on Write Tape.
74	7	C	2	406	Exit on Write Program Error.
74	7	C	2	407	Exit on No Write Program Error.
					Input
74	0	C	2	0N1	Select Tape N to Read Binary One Record.
74	0	C	2	0N2	Select Tape $\overline{N}$ to Read Coded One Record.
74	0	C	2	2N1	Select Tape $\overline{N}$ to Read Binary One File.
74	0	C	2	2N2	Select Tape $\overline{N}$ to Read Coded One File.
74	0	C	2	001	Prepare Selected Tape to Read Binary One Record.
74	0	C	2	002	Prepare Selected Tape to Read Coded One Record.
74	0	C	2	201	Prepare Selected Tape to Read Binary One File.
74	0	C	2	202	Prepare Selected Tape to Read Coded One File.
74	0	C	2	003	Move Selected Read Tape Forward One Record.
74	0	C	2	203	Search File Mark Forward.
74	0	C	2	004	Select Interrupt When Read Tape Next Ready.
74	0	C	2	005	Rewind Selected Read Tape.
74	0	C	2	006	Backspace Selected Read Tape.
74	0	C	2	206	Search File Mark Backward.
74	0	C	2	007	Rewind-Unload Selected Read Tape.
74	0	C	2	400	Clear Interrupt Selections on Read Tape.
74	0	C	2	401	Set Low Density on Selected Read Tape.
74	0	C	2	402	Set High Density on Selected Read Tape.
74	0	C	2	404	Select Interrupt on Next Error.

INSTRUCTION LIST APPENDIX—Contd.

§ 121.

INSTRUCTION					OPERATION
OP	Index	Address			
EXF	Select/Sense	Channel	Equip. No.	Sub-Operation	
74	0 or 7	1 to 6	0 to 7	000 to 777	
					SENSE
74	7	C	2	000	Exit on Ready to Read.
74	7	C	2	001	Exit on Not Ready to Read.
74	7	C	2	002	Exit on Read Parity Error.
74	7	C	2	003	Exit on No Read Parity Error.
74	7	C	2	004	Exit on Read Length Error.
74	7	C	2	005	Exit on No Read Length Error.
74	7	C	2	006	Exit on End of-File Mark.
74	7	C	2	007	Exit on Not End-of-File Mark.
74	7	C	2	400	Exit on Ready To Select.
74	7	C	2	401	Exit on Not Ready To Select.
74	7	C	2	402	Exit on Load Point.
74	7	C	2	403	Exit on Not Load Point.
74	7	C	2	404	Exit on Interrupt on Read Tape.
74	7	C	2	405	Exit on No Interrupt on Read Tape.
74	7	C	2	406	Exit on Read Program Error.
74	7	C	2	407	Exit on No Read Program Error.
		CDC 1617 CARD READER			SELECT
74	0	C	4	000	Channel Clear.
74	0	C	4	001	Read continuously (Free Run).
74	0	C	4	002	Read Single Cycle.
74	0	C	4	005	Read continuously and Translate.
74	0	C	4	006	Read Single Cycle and Translate.
					SENSE
74	7	C	4	002	Exit if Ready.
74	7	C	4	003	Exit if Not Ready.
74	7	C	4	004	Exit on Reader Normal.
74	7	C	4	005	Exit on Reader Not Normal.
74	7	C	4	010	Exit on Input Hopper Empty.
74	7	C	4	011	Exit on Input Hopper Not Empty.
74	7	C	4	020	Exit on Stacker Full.
74	7	C	4	021	Exit on Stacker Not Full.
74	7	C	4	040	Exit on Amplifier Failure.
74	7	C	4	041	Exit on No Amplifier Failure.
74	7	C	4	100	Exit on Feed Failure.
74	7	C	4	101	Exit on No Feed Failure.

CODING SPECIMEN: MACHINE CODE

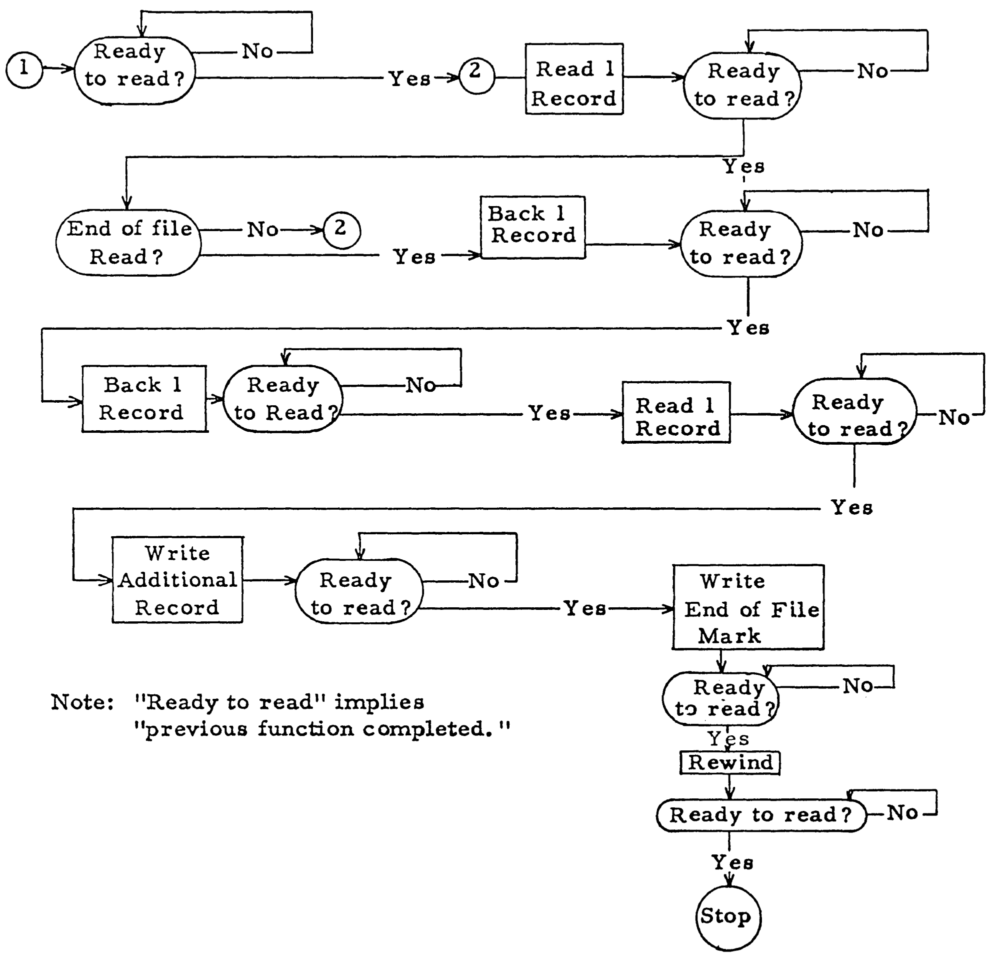
§ 131.

.1 PROBLEM

This program adds one record to the end of magnetic tape 1. It is assumed the end of data on tape is marked by an end-of-file mark. The program advances the tape past the end of file mark, backs up two records, advances one record and then writes the additional record from memory 60000-60177, and then writes a new end-of-file mark.

The reason for backing up two after reading end-of-file, then advancing by one, is so that writing shall follow a forward movement. If writing follows a back-up, especially over an end-of-file mark, the spacing between records will not be constant.

.2 FLOW CHART



Note: "Ready to read" implies "previous function completed."

§ 131.

.3 CODING

(50000) =	EXF	7	32010	Is mag. tape 1 ready to read?
	SLJ	0	50000	If not ready, wait.
(50001) =	ENI	6	Temp + 1	Set B^6 to temp. address 1
	SIL	6	00003	Store term address in lower (0003)
(50002) =	EXF	0	32010	Select Mag. Tape 1 to read
	EXF	3	Temp	Read one word to memory - tape moves one block.
(50003) =	EXF	7	32010	Sense if ready to read again
	SLJ	0	50003	If not ready, wait.
(50004) =	EXF	7	32012	Sense if end-of-file read
	SLJ	0	50001	If not end-of-file - read again.
(50005) =	EXF	0	32011	Move back one record
	Pass			
(50006) =	EXF	7	32010	Sense, if ready to read
	SLJ	0	50006	If not ready, wait.
(50007) =	EXF	0	32011	Move back one record.
	Pass			
(50010) =	EXF	7	32011	Sense, if ready to read
	SLJ	0	50010	If not ready, wait.
(50011) =	ENI	6	Temp + 1	Set B^6 to Term Address
	SIL	6	00003	Store term. add. in 00003.
(50012) =	EXF	0	32010	Select mag. tape 1
	EXF	3	Temp	Activate read
(50013) =	EXF	7	42012	Sense end-of-file on tape 1
	SLJ	0	50013	If not ready, wait.
(50014) =	ENI	6	Rec+200	Set B^6 to term address
	SIL	6	00004	Enter term. add. in 00004.
(50015) =	EXF	0	42010	Select Write
	EXF	4	Rec	Write activate
(50016) =	EXF	7	42012	Sense end of write indicator
	SLJ	0	50016	If not ready, wait.
(50017) =	EXF	0	42016	Write end-of-file mark on tape
	Pass			
(50020) =	EXF	7	42012	Skip if ready
	SLJ	0	50020	Wait
(50021) =	EXF	0	32015	Rewind
	Pass			
(50022) =	EXF	7	32010	Sense end of rewind
	SLJ	0	50022	Wait
(50023) =	SLS	0	50000	Stop
	0		0	

Reprinted from CDC 1604 Programming Training Manual, pp. G-1 through G-3.

§ 132. CODING SPECIMEN: CODAP

.1 CODING SHEET

1604 ASSEMBLY CODING FORM

PROGRAM CODAP CODING SPECIMEN

ROUTINE

NAME

PAGE NO.

DATE

H	LOCN	OPN	B	OPERAND OR M-TERM	REMARKS
		ØRG		100B	BEGINNING ADDRESS DESIGNATOR
	RØUT	ENI	1	10B	ENTER INDEX 1 WITH 10 (OCTAL)
		ENA	0	0	CLEAR A
+	A	ADD	1	C	ADD (C + B') → A
		IJP	1	A	LOOP 9 TIMES
		SLS	0	RØUT	STOP UNCONDITIONALLY; JUMP TO 100.
	C	BSS		9	RESERVE 9 LOCATIONS FOR OPERANDS
		END			END
		ABSOLUTE CODING FOR SAME ROUTINE			
	100	50	1	00010	
		10	0	00000	
	101	14	1	00103	
		55	1	00101	
	102	76	0	00100	
	103			OPERANDS	
	...				

CDC 193

CODING SPECIMEN: FORTRAN-60

§ 133.

.1 CODING SPECIMEN

```
        PROGRAM TEST
        DIMENSION A(20000),B(20000)
        COMMON A,B
        EQUIVALENCE (A,B)
        I=5
        END
TEST, 0, 24, 47041

AAA - 00000,  BAA - 00002,  IAA - 00006,  KAA - 00006,  PAA - 00010
RAA - 00010,  TAA - 00020,  VAA - 00020

WAB = 30736,  WAA = 30736

, PROGRAM PREAMBLE

AAA00   750 00000 500 00000
AAA01   571 RAA01 501 00000

, MAIN PROGRAM

RAA00   120 KAA01 610 RAA07 \
RAA01   531 RAA07 500 00000  |  MAP Language
RAA02   561 RAA01 531 RAA01  |
RAA03   750 AAA00 000 00000 /

, CONSTANTS

KAA00   000 00000 000 47040
KAA01   000 00000 000 00005

, ASSIGNED VARIABLES

, REASSIGNED VARIABLES

, NORMAL VARIABLES

, ARRAYS

WAA00   000 00000 000 00000   A
WAB00   000 00000 000 00000   B

,,
        END
```

CODING SPECIMEN: FORTRAN-62

§ 134.

.1 CODING SPECIMEN

```
START MONITOR RUN.
BEGIN JOB 006      08/31/62
COOP,AAA9-001,SWANSON,     ,3,1000,3,PROGRAM FILETAPE REEL 608.
FORTRAN,1,1,56.
                 PROGRAM FILTAPE
                 DIMENSION JJ(100)
                 DO 20 I=1,100
                 JJ(I)=I
              20 CONTINUE
                 IU=0
              30 IL=IU+1
                 IU=IL+9
                 WRITE OUTPUT TAPE 14,920,(JJ(I),I=IL,IU)
                 END FILE 14
                 IF(IU-100)30,40,40
              40 CONTINUE
                 CALL QUITS
             920 FORMAT((O20))
                    END         FILTAPE
```

```
                                          IDENT        FILTAPE
RANGE                 FWA   -   LWA+1
                      00000     00214
ENTRY POINTS
                      00000   FILTAPE
EXTERNAL SYMBOLS
                      00001      GOUT
                      00002     ERROR
                      00003    INGOUT
                      00004   ENDGOUT
                      00005     WREOF
                      00006     QUITS
                      00000+              ENTRY        FILTAPE
     00000+   75   0  77777   FILTAPE    SLJ      0   **
              50   0  00000
     00001+   50   1  00000   +          ENI      1   0

              11   0  00001              INA      0   1
     00010+   20   0  00212+             STA      0   IL
              12   0  00212+             LDA      0   IL
     00011+   11   0  00011              INA      0   9
              20   0  00210+             STA      0   IU
                                         I/O          14
     00012+   10   0  00041+  +          ENA      0   =14
              04   0  00040+             ENQ      0   F.920
     00013+   75   4 X00003   +          RTJ          INGOUT
              50   0  00000
     00014+   75   4 X00002   +          RTJ          ERROR
              50   0  00000
     00015+   53   2  00212+  +          LIL      2   IL
              51   2  77776              INI      2   -1
     00016+   10   2  00001   (00A)      ENA      2   +1
              20   0  00207+             STA      0   I
     00017+   15   0  00210+             SUB      0   IU
              11   0  77776              INA      0   -1
     00020+   22   2  00026+             AJP      P   (00B)+1
              50   0  00000
     00021+   10   2  00043+  (00)       ENA      2   JJ
              61   0  00023+             SAL          C(1)+1
     00022+   75   4 X00001   C(1)       RTJ      0   GOUT
              50   0  00000
     00023+   00   0  00042+  +          ZRO      0   =0
              00   0  77777              ZRO      0   **
     00024+   75   4 X00002   +          RTJ          ERROR
              50   0  00000
```

```
     00025+   51   2  00001   (00B)      INI      2   1
              75   0  00016+             SLJ      0   (00A)
     00026+   75   4 X00004   +          RTJ          ENDGOUT
              50   0  00000
     00027+   75   4 X00002   +          RTJ          ERROR
              50   0  00000
     00030+   10   0  00041+  +          ENA      0   =14
              75   4 X00005              RTJ      0   WREOF
     00031+   75   4 X00002   +          RTJ          ERROR
              50   0  00000
     00032+   12   0  00210+  +          LDA      0   IU
              11   0  77633              INA      0   -100
     00033+   22   0  00035+             AJP      Z   (40)
              22   3  00007+             AJP      M   (30)
     00034+   75   0  00035+             SLJ          (40)
              50   0  00000

     00043+                   JJ         BSS          100
     00207+                   I          BSS          1
     00210+                   IU         BSS          1
     00211+                   K(1)       BSS          1
     00212+                   IL         BSS          1
     00213+                   T(2)       BSS          1
     00001                               LIB          GOUT
     00002                               LIB          ERROR
     00003                               LIB          INGOUT
     00004                               LIB          ENDGOUT
     00005                               LIB          WREOF
     00006                               LIB          QUITS
                  00000                  END          FILTAPE
NO DOUBLY DEFINED
NO UNDEFINED SYMBOLS
NULLS                  (20)          (00)        K(1)

     0 MINUTES, 21 SECONDS.
END JOB 006.
```

DATA CODE TABLE NO. 1

§ 141.

.1 USE OF CODE: . . . . CDC 1612 Printer, internal.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . 3 bits: 4, 2 and 1.

.222 Less significant pattern: . . . . 3 bits: 4, 2 and 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0	:	8	Blank	Y	-	Q	+	H
1	1	9	/	Z	J	R	A	I
2	2	∅	S	]	K	%	B	<
3	3	=	T	,	L	$	C	.
4	4	≠	U	(	M	*	D	)
5	5	≤	V	→	N	↑	E	≥
6	6	'	W	≡	O	↓	F	?
7	7	[	X	~	P	>	G	;

NOTE: Characters ~ , %, and $ appear for business application and are replaced respectively by ∧ , ∨ , and ¬ for scientific application.

DATA CODE TABLE NO. 2

§ 142.

.1 USE OF CODE: . . . . Input-Output Typewriter.

.2 STRUCTURE OF CODE

.21 Character Size: . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . . . 3 bits: 4, 2 and 1.

.222 Less significant pattern: . . . . . . 3 bits: 4, 2 and 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN															
	UPPER CASE								LOWER CASE							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0			E	A	,	:	&	@			e	a	,	;	7	2
1	T	L	Z	W		Tab	Back Space		t	l	z	w		Tab	Back Space	
2	÷	R	D	J	.	–	$	¢	=	r	d	j	.	-	4	6
3	O	G	B	½					o	g	b	8				
4	Space	I	S	U	?	"	#	*	Space	i	s	u	/	'	3	1
5	H	P	Y	Q	CR				h	p	y	q	cr			
6	N	C	F	K	°	)	%		n	c	f	k	+	ϕ	5	
7	M	V	X	(	Upper Case	Lower Case			m	v	x	9	Upper Case	Lower Case		

DATA CODE TABLE NO. 3

§ 143.

.1 USE OF CODE: . . . . magnetic tape BCD internal.

.2 STRUCTURE CODE

.21 Character Size: . . . 6 bits.

.22 Character Structure

.221 More signficant pattern: . . . . 3 bits: 4, 2 and 1.

.222 Less significant pattern: . . . . 3 bits: 4, 2 and 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0		8	(blank)	Y	-	Q	&	H
1	1	9	/	Z	J	R	A	I
2	2	Ø	S	record mark	K	0 (minus)	B	0 (plus)
3	3	#	T	,	L	$	C	. (period)
4	4	@	U	%	M	*	D	⌑
5	5		V		N		E	
6	6		W		O		F	
7	7	tape mark	X		P		G	group mark

DATA CODE TABLE NO. 4

§ 144.

.1 USE OF CODE: . . . punched card BCD input-output, internal

.2 STRUCTURE OF CODE

.21 Character Size: . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . . . 3 bits: 4, 2 and 1.

.222 Less significant pattern: . . . . . . 3 bits: 4, 2 and 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0		8	BLANK	Y	–	Q	+	H
1	1	9	/	Z	J	R	A	I
2	2	ϕ	S	⊐	K	%	B	<
3	3	=	T	,	L	$	C	.
4	4	≠	U	(	M	*	D	)
5	5	≤	V	→	N	↑	E	≥
6	6	|	W	≡	O	↓	F	?
7	7	⊏	X	∼	P	>	G	;

DATA CODE TABLE NO. 5

§145.

.1 USE OF CODE: . . . . punched card BCD input-output, external.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . . 1 column.

.23 Character Codes

UNDERPUNCH	OVERPUNCH			
	None	12	11	0
None		+	–	
12				
11				
0	0			
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
8-2		<	%	]
8-3	=	.	$	,
8-4	≠	)	*	(
8-5	≤	≥	↑	→
8-6	|	?	↓	≡
8-7	[	;	>	~

DATA CODE TABLE NO. 6

§ 146.

.1 USE OF CODE: . . . . Flexowriter.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . . . 3 bits: 4, 2, and 1.

.222 Less significant pattern: . . . . . . 3 bits: 4, 2, and 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN															
	UPPER CASE								LOWER CASE							
	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	Tape Feed		E	A		:	7	2	Tape Feed		e	a		;	7	2
1	T	L	Z	W		Tab	Back Space		t	l	z	w		Tab	Back Space	
2	Color Shift	R	D	J	=	-	4	6	Color Shift	r	d	j	.	-	4	6
3	O	G	B	8	Stop				o	g	b	8	Stop			
4	Space	I	S	U	'	(	3	1	Space	i	s	u	/	)	3	1
5	H	P	Y	Q	CR				h	p	y	q	CR			
6	N	C	F	K	+	0	5		n	c	f	k	,	0	5	
7	M	V	X	9	UC	LC		Delete	m	v	x	9	UC	LC		Delete

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers

IBM 650
Reference: . . . . . . 02 NBSB.
Date available: . . . . 1961.
Description
The routine simulates an IBM 650 computer containing a 2,000 word drum, index registers and floating point. The simulator operates on a CDC 1604 with an IBM 407, 088 and 523 unit.

CDC 1604-A: . . . . . . by a switch on 1604-A console.

.12 Simulation by Other Computers

CDC 160-A: . . . . . . INTERFOR system simulates 20 of the 62 operations, and includes other facilities.

.13 Data Sorting and Merging

Reference: . . . . M 4 CODA KSM.
Record size: . . . . . . 80 or 120 characters.
Block size: . . . . 1 record per block.
Key size: . . . . any number of keys of any length.
File size: . . . . any number of tape reels.
Number of tapes: . . . 4 upwards.
Date available: . . . . . 1961.
Description
The routine provides data editing facilities and operates only on BCD data. No other sorting routines are listed in the July, 1962 CO-OP Index.

.14 Report Writing: . . . . none.

.15 Data Transcription

Convert Symbolic Magnetic-Tape-to-Paper-Tape
Reference: . . . . . . M 2 CODA MAGPT.
Date available: . . . . 1961.
Description
Converts 80 or 120 character BCD magnetic tape to Flexowriter tape.
Performance limited by Flexowriter output.

.16 File Maintenance: . . . only routines for specific installations are available.

.17 Other

Arithmetic Functions

	TIME (μ. sec.)		
	+	-	x
Double Precision, Floating Point	500	500	1000
Complex Numbers, Floating Point	173.6	173.6	353.6

Mathematical Functions (Representative cases, all floating point)

	TIME (μ sec)	SPACE	ERROR (Max)
Sine	964	68	2.1×10^{-11}
Cos	964	68	2.1×10^{-11}
Tan	1129	53	2.4×10^{-11}
Arc Sine	1610	115	8.7×10^{-11}
Arc Cos	1085		8.7×10^{-11}
Arc Tan	985	71	8.7×10^{-11}
Exponential	540	32	8.7×10^{-11}
Natural log	677	45	8.7×10^{-11}

Polynomial Evaluation

	TIME (μ sec)	SPACE
Hermite	130 + 165 (N-1)	24
Laguerre	130 + 238 (N-1)	24
Legendre	123 + 247 (N-1)	25

Other
Hypergeometric Functions Space: 2,491 locations, timing unknown.

.2 PROBLEM ORIENTED LANGUAGES

PERT: . . . . RIP.
Linear Programming Package: . . . . RIP.

PROCESS ORIENTED LANGUAGE: FORTRAN-60

§ 162.

.1 GENERAL

.11 Identity: . . . . FORTRAN-60.

.12 Origin: . . . . Computer Division, Control Data Corporation.

.13 Reference: . . . . Control Data Publications 087A and 027A.

.14 Description

FORTRAN-60 for the 1604 is a restricted version of the FORTRAN II language as implemented for the IBM 709/7090. Two newer, more powerful versions of the FORTRAN language are available for the 1604. FORTRAN-62 has been released, and the FORTRAN-63 translator is in field test status. The FORTRAN-60 system, however, is still in use; it provides faster compiling speeds in the compile-and-execute mode and permits intermixed FORTRAN and symbolic statements. Furthermore, certain language incompatibilities (summarized in Section :163.14) necessitate manual conversions before programs coded in FORTRAN-60 can be compiled by the newer CDC FORTRAN systems.

A curious feature of FORTRAN-60 is the permanent assignment of the six machine index registers to the specific integer variables named I, J, K, L, M, and N. Routines using these six variables as subscripts and loop indices can, therefore, be compiled and executed rapidly, whereas severe inefficiencies will result if any other integer variables are used as subscripts or loop indices. The names I, J, K, L, M, and N may not be assigned to subscripted variables.

Other restrictions and extensions of the FORTRAN-60 language relative to IBM 709/7090 FORTRAN II are summarized below.

Restrictions:

(1) Double precision and complex arithmetic are not permitted.

(2) It is not possible to test for arithmetic errors; IF ACCUMULATOR OVERFLOW, IF QUOTIENT OVERFLOW, and IF DIVIDE CHECK result in unconditional branches to the second statement listed.

(3) The 1604 has only three sense switches. If more are required, a SWITCH routine is used to set or clear pseudo switches in six core storage locations.

(4) The following statements have not been implemented: FREQUENCY, END FILE, READ DRUM, WRITE DRUM.

14 Description (Contd.)

Restrictions (Contd.)

(5) All allocation statements (DIMENSION, EQUIVALENCE, and COMMON) must precede the first executable statement in a source program.

(6) The CHAIN feature, which facilitates segmentation of programs too large to fit into core storage, has not been implemented.

(7) Independently-compiled subprograms cannot be linked together at execution time.

Extensions:

(1) Names may be up to eight characters in length.

(2) The following number ranges can be handled:

Floating point: .	10^{-308} to 10^{+308}.
Integers:	-2^{47} to $+2^{47}$ (except 16,383 is maximum value for variables I, J, K, L, M, and N, which are stored in index registers).
Boolean:	16 octal digits (48 bits).

(3) No parenthesized statement number list is required in an assigned GO TO statement.

.15 Publication Date: . . . . November, 1960.

.2 PROGRAM STRUCTURE

.21 Divisions: . . . . one division, composed of the following types of statements.

Procedure statements: . algebraic formulae.
comparisons and jumps.
input and output.

Data statements: . . . . FORMAT: describes the layout, size, scaling, and code of input-output data.
EQUIVALENCE: used to cause two variables to have a common location or to specify synonyms.
COMMON: used to cause a name to be common to more than one segment rather than local to each.
DIMENSION: describes the elements in each dimension of an array or set of arrays.

§ 162.

.22 Procedure Entities

Program:	subroutines and functions.
Subroutine:	statements.
Function:	statements.
Statement:	characters; blanks are ignored.

.23 Data Entities

Arrays:	all variables.
Item:	floating point variable or constant.
	integer variable or constant.
	Boolean variable or constant.
	Hollerith item.
	alphameric item.
Hollerith item:	alphameric item that can only be used for output.
Alphameric:	alphameric item that can only be input during a run; it can be used for output, or as a format statement.

.24 Names

.241 Simple name formation

Alphabet:	A to Z, 0 to 9.
Size:	1 to 8 char.
Avoid key words:	no.
Formation rule:	first char must be letter.
	do not use final F if name is more than 3 char long.

.242 Designators

Procedures	
Statement label:	unsigned integer.
Function label:	same as variable being defined.
Subroutine label:	no designator.
Data	
Integer variables:	initial I, J, K, L, M, N.
Floating point variables:	any other initial letter.
Equipment	
Card:	implied by verbs READ, PUNCH.
Magnetic tape:	use key word TAPE.
Printer:	implied by verb PRINT.
Index registers:	variable names I, J, K, L, M, N.
Comments:	C in col. 1 of statement.
Translator control:	key words EQUIVALENCE, COMMON.

.25 Structure of Data Names

.251 Qualified names:	none.
.252 Subscripts	
Number per item:	0 to 3.
Applicable to:	all variables.
Class may be	
Special index variable:	no.
Any variable:	only integers.
Literal:	yes.
Expression:	any integer expression.

.252 Subscripts (Contd.)

Form may be	
Integer only:	yes.
Signed:	no.
Truncated fraction:	no.
Rounded fraction:	no.

.253 Synonyms

Preset:	EQUIVALENCE statement causes sharing of storage locations.
Dynamically set:	no.

.26 Number of Names

.261 All entities:	no practical limit.
.262 Procedures	
Numbered statements:	all inter-related; no practical limits.
Subroutines:	all inter-related; no practical limits.
Functions:	all inter-related; no practical limits.
Others:	all inter-related; no practical limits.
.263 Data	
Files:	no limit.
Record formats:	no practical limit.
Items:	no practical limit.
.264 Equipment	
Tape units:	48.
Card readers:	1.
Card punches:	1.
Printers:	1.

.27 Region of Meaning of Names: all names are local to the program, subroutine, or function in which they are defined unless specified in a COMMON statement.

.3 DATA DESCRIPTION FACILITIES

.31 Methods of Direct Data Description

.311 Concise item picture:	FORMAT statement only.
.312 List by kind:	no.
.313 Qualify by adjective:	no.
.314 Qualify by phrase:	no.
.315 Qualify by code:	yes, first letter of name.
.316 Hierarchy by list:	no.
.317 Level by indenting:	no.
.318 Level by coding:	no.
.319 Others	
Array size:	DIMENSION (4, 7).
Four-digit integer:	FORMAT (I4).
Four-digit integers, 5:	FORMAT (5I4).
Floating point items:	FORMAT (F8.3, E10.4) for +999.999 and +.0000E+9

.32 Files and Reels: own coding.

.33 Records and Blocks

.331 Variable record size:	dynamic.
.332 Variable block size:	fixed.
.333 Record size range:	1 to N blocks.

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.334 Block size

READ TAPE, WRITE TAPE:	54 words (binary format).
READ INPUT TAPE, WRITE OUTPUT TAPE:	120 characters (BCD format).
READ, PUNCH:	80 columns.
PRINT:	120 characters.

.335	Choice of record size:	READ, WRITE statement.
.336	Choice of block size:	fixed for each input-output statement type.
.337	Sequence control:	own coding.
.338	In-out error control:	automatic.
.339	Blocking control:	none; 1 or more full blocks per logical record.

.34 Data Items

.341	Designation of class:	by name.
.342	Possible classes	
	Integer:	yes.
	Fixed point:	no.
	Floating point:	yes.
	Logical:	yes.
	Alphameric:	yes.
.343	Choice of external radix:	FORMAT statement.
.344	Possible external radices	
	Decimal:	yes.
	Octal:	yes.
.345	Internal justification:	alpha automatic left justified. integers automatic right justified.
.346	Choice of external code:	FORMAT statement and READ, WRITE statement.
.347	Possible external codes	
	Decimal:	yes.
	Octal:	yes.
	Hollerith:	yes.
	Alphameric:	yes.
.348	Internal item size	
	Variable size:	fixed.
	Designation:	none.
	Range	
	Fixed point numeric:	fixed, 1 word.
	Floating point numeric:	fixed, 1 word.
	Alphameric:	fixed, 1 word of up to 8 characters.
.349	Sign provision:	optional.

.35 Data Values

.351	Constants	
	Possible sizes	
	Integer:	$\pm 2^{47}$.
	Fixed point:	none.
	Floating point:	10^{-308} to 10^{+308}.
	Alphameric:	120 characters.
	Boolean:	16 octal digits.
	Subscriptable:	yes.
	Sign provision:	optional.
.352	Literals:	same as constants.
.353	Figuratives:	own coding; e.g., TEN = 10.0.
.354	Conditional variables:	computed GO TO.

.36 Special Description Facilities

.361	Duplicate format:	by multiple references to a single FORMAT statement.
.362	Re-definition:	COMMON statement. EQUIVALENCE statement.
.363	Table description	
	Subscription:	mandatory, in DIMENSION statement.
	Multi-subscripts:	1 to 3.
	Level of item:	variables.
.364	Other subscriptable entities:	tape units.

.4 OPERATION REPERTOIRE

.41 Formulae

.411 Operator List

+:	addition, also unary.
-:	subtraction, also unary.
*:	multiplication.
/:	division.
**:	exponentiation.
=:	is set equal to.
ABSF ( )‡:	absolute value.
INTF ( )‡:	entire.
MODF (A, B)‡:	remainder A ÷ B.
MAXOF (A, ...)‡:	max value; fixed argument.
MAX1F (A, ...)‡:	max value; floating argument.
MINOF (A, ...)‡:	min value; fixed argument.
MIN1F (A, ...)‡:	min value; floating argument.
DIMF (A, B)‡:	diminish A by B.
SIGNF (A, B)‡:	transfer sign of A to B.
FLOATF ( ):	float an integer.
XFIXF ( ):	fix a floating point variable.
LOGF ( ):	natural log.
LOG10F ( ):	common log.
SINF ( ):	sine.
ASINF ( ):	arc sine.
COSF ( ):	cosine.
ACOSF ( ):	arc cosine.
EXPF ( ):	exponential.
SQRTF ( ):	square root.
ATANF ( ):	arctangent.
TANHF ( ):	hyperbolic tangent.
SINH ( ):	hyperbolic sine.
COSH ( ):	hyperbolic cosine.

‡ denotes function may have prefix X to denote fixed point result.

.412	Operands allowed	
	Classes:	numeric only.
	Mixed scaling:	yes.
	Mixed classes:	only in exponentiation and functions.
	Mixed radices:	no.
	Literals:	yes.
.413	Statement structure	
	Parentheses	
	a - b - c means:	(a-b) - c.
	a + b x c means:	a + (b x c).
	a ÷ b ÷ c means:	(a ÷ b) ÷ c.
	a^{b^c} means:	illegal; parentheses must be used
	Size limit:	660 char.
	Multi-results:	no.

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.414	Rounding of results:	truncation of integers at each step in expression.	
.415	Special cases	Fixed	Floating
	x = -x:	K = -K	X = -X.
	x = x + 1:	K = K + 1	X = X + 1.
	x = 4.7 y:	K = 47*K/10	X = 4.7 * Y.
	$x = 5x10^7 + y^2$:	50000000+ L**2	X = 5. E7 + Y**2.
	x = |y|:	K = XABSF(L)	X = ABSF(Y).
	x = entire (3.5):	K = XINTF(L)	X = INTF(Y).
.416	Typical examples:	X = (-B + SQRTF(B*B-4. 0 *A*C))/(2. 0*A).	

.42 Operations on Arrays

.421 Matrix operations: . . . none.
.422 Logical operations
Sizes of operands: . . 48 bits.
AND: . . . . *
Inclusive OR: . . . . . +
Exclusive OR: . . . . none.
NOT: . . . . -
Designation: . . . . . B in col. 1 of each Boolean statement.
.423 Scanning: . . . . none.

.43 Other Computation: . . symbolic machine instructions may be inserted in a FORTRAN source program.

.44 Data Movement and Format

.441 Data copy example: . . Y = X.
.442 Levels possible: . . . . items.
.443 Multiple results: . . . . none.
.444 Missing operands: . . . not possible.
.445 Size of operands
Exact match: . . . . . implied, except for alpha or input-output.
Alignment rule
Numbers: . . . . . . right justified or normalized.
Alpha: . . . . left justified.
Filler rule
Numbers: . . . . . . zeros.
Alpha: . . . . blanks.
Truncating rule
Numbers: . . . . . . truncate at left.
Alpha: . . . . truncate at right.
Variable size destination: . . . . no.

.446 Editing possible
Change class: . . . . yes.
Change radix: . . . . yes.
Insert editing symbols
Actual point: . . . . automatic.
Suppress zeroes: . . automatic.
Insert: . . . . automatic point.
Float: . . . . - sign only.
.448 Special moves: . . . . . none.
.449 Character manipulation: none.

.45 File Manipulation

Open: . . . . own coding.
Close: . . . . own coding.
Advance to next record: READ, WRITE, PUNCH, PRINT.

.45 File Manipulation (Contd.)

Step back a record: . . BACKSPACE.
Set restart point: . . . none.
Restart: . . . . none.
Start new reel: . . . . . own coding.
Start new block: . . . . implied in each input-output statement.
Search on key: . . . . . none.
Rewind: . . . . REWIND.
Unload: . . . . none.

.46 Operating Communication

.461 Log of progress: . . . . PRINT uses on-line printer.
.462 Messages to operator: . same as log (error messages are automatically typed on console typewriter).
.463 Offer options: . . . . . PAUSE and type decimal integer.
PRINT message and PAUSE.
.464 Accept option: . . . . . IF SENSE SWITCH n.

.47 Object Program Errors

Error	Discovery	Special Actions
Overflow:	none.	
In-out:	automatic	?
Invalid data:	format checks	typed messages.

.5 PROCEDURE SEQUENCE CONTROL

.51 Jumps

.511 Destinations allowed: . statement.
.512 Unconditional jump: . . GO TO N.
.513 Switch: . . . . GO TO M, or GO TO M, (35, 47, 18).
.514 Setting a switch: . . . . ASSIGN 35 TO M.
.515 Switch on data: . . . . . GO TO (35, 47, 18) I.

.52 Conditional Procedures

.521 Designators
Condition: . . . . . . IF.
Procedure: . . . . . . implied.
.522 Simple conditions: . . . expression or variable versus zero.
.523 Conditional relations: . IF (A) n1, n2, n3: If value of expression A is less than, equal to, or greater than zero, respectively, go to statement n1, n2, or n3.
.524 Variable conditions: . . expression always against zero.
.525 Compound conditionals: no.
.528 Typical examples: . . . IF (X**2.0 - 3.0) 29, 37, 18; go to 29, 37, or 18 if x^2-3 is respectively less than, equal to, or greater than zero.

.53 Subroutines

.531 Designation
Single statement: . . . not possible.
Set of statements
First: . . . . SUBROUTINE.
Last: . . . . END.

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.532 Possible subroutines: . any number of statements.
.533 Use in-line in program: no.
.534 Mechanism
Cue with parameters: CALL XXX (X, Y, Z).
Number of parameters: . . . . maximum of 64.
Cue without parameters: . . . . CALL XXX.
Formal return: . . . . RETURN at least once.
Alternative return: . . none.
.535 Names
Parameter call by value: . . . . none.
Parameter call by name: . . . . yes.
Non-local names: . . use COMMON.
Local names: . . . . . all.
Preserved own variables: . . . . . . all.
.536 Nesting limit: . . . . . no limit.
.537 Automatic recursion allowed: . . . . no.

.54 Function Definition by Procedure

.541 Designation
Single statement: . . . same as set.
Set of statements
First: . . . . FUNCTION.
Last: . . . . END.

.542 Level of procedure: . . any number of statements.
.543 Mechanism
Cue: . . . . by name in expression.
Formal return: . . . . RETURN.
.544 Names
Parameter call by value: . . . . none.
Parameter call by name: . . . . yes.
Non-local names: . . use COMMON.
Local names: . . . . . all.
Preserved own variables: . . . . . . all.

.55 Operand Definition by Procedure: . . . . . . none.

.56 Loop Control

.561 Designation of loop
Single procedure: . . none.
First and last procedures: . . . . . current place to named end; e.g., DO 173 I = 1, N, 2.
.562 Control by count: . . . none.
.563 Control by step
Parameter
Special index: . . . . no.
Any variable: . . . . integer only.
Step: . . . . positive integers.
Criteria: . . . . greater than.
Multiple parameters: no.
.564 Control by condition: . no.
.565 Control by list: . . . . no.
.566 Nesting limit: . . . . . no limit.
.567 Jump out allowed: . . . yes.
.568 Control variable exit status: . . . . available.

.6 EXTENSION OF THE LANGUAGE: . . . . . can write new function in library.

.7 LIBRARY FACILITIES

.71 Identity: . . . . FORTRAN-60 Reference Library.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.

.73 Storage Form: . . . . . magnetic tape; 54-word blocks in "tag binary" format.

.74 Varieties of Contents: . subroutines.
functions.
service routines.

.75 Mechanism

.751 Insertion of new item: . separate run, using FORTLIB or MAPTLIB Compiler.
.752 Language of new item: . FORTRAN or MAP, a regional assembly language specific to FORTRAN-60.
.753 Method of call: . . . . . named in procedures.

.76 Types of Routines

.761 Open routines exist: . . no.
.762 Closed routines exist: . yes.
.763 Open-closed is variable: no.

.8 TRANSLATOR CONTROL

.81 Transfer to Another Language: . . . . . . strings of symbolic machine instructions, separated by commas, can be inserted in the source program.

.82 Optimizing Information Statements

.821 Process usage statements: . . . . . . none.
.822 Data usage statements: COMMON.
EQUIVALENCE.

.83 Translator Environment: . . . . . no.

.84 Target Computer Environment: . . . . . no.

.85 Program Documentation Control: . . . . no.

.9 TARGET COMPUTER ALLOCATION CONTROL

.91 Choice of Storage Level: no.

.92 Address Allocation: . . none.

.93 Arrangement of Items in Words in Unpacked Form: . . . . standard for numerics.

.94 Assignment of Input-Output Devices: . . . specified in input-output statements.

.95 Input-Output Areas: . . automatic.

PROCESS ORIENTED LANGUAGE: FORTRAN-62

§ 163.

.1 GENERAL

.11 Identity: . . . . FORTRAN-62.

.12 Origin: . . . . Computer Division, Control Data Corporation.

.13 Reference: . . . . Control Data Publications No. 506 and PSB-ASO6621.

.14 Description

The main advantages of the FORTRAN-62 system over FORTRAN-60 are the more efficient object programs it produces and its ability to link subroutines compiled independently. Language extensions include buffered input-output, division of the COMMON data area into named blocks, and more flexible subscripting. As in FORTRAN-60, there are no facilities for complex or double precision arithmetic or for the detection of arithmetic errors.

The incompatibilities between the FORTRAN-60 and FORTRAN-62 languages that must be considered in source program conversions can be summarized as follows:

(1) FORTRAN-62 treats Hollerith constants or literals as floating point mode and identifies them by floating point variable names; FORTRAN-60 treats them as fixed point mode.

(2) FORTRAN-62 allows symbolic coding (in CODAP-1) to appear only as a subroutine; FORTRAN-60 permits intermixed symbolic and FORTRAN statements or symbolic subroutines.

(3) There are certain differences in the naming conventions for functions.

(4) The COMMON and EQUIVALENCE statements are implemented differently; this can lead to differences in the correspondence of shared variables between two or more subprograms.

(5) FORTRAN-62 treats all integer variables as modulo $2^{47}-1$; in FORTRAN-60, the variables named I through N are treated as modulo 16,383 because they are stored in the index registers.

(6) There are differences in implementation of the E conversion in the FORMAT statement.

(7) There are minor implementation differences in the END, STOP, PAUSE, and SENSE SWITCH statements.

(8) Differences in the required source program order may necessitate some shuffling of the source cards.

.14 Description (Contd.)

(9) FORTRAN-62 places certain restrictions on names to avoid conflicts with the library program names.

(10) The different operating systems require the control cards for FORTRAN-62 to be totally different from those for the FORTRAN-60 system.

(11) The FORTRAN-60 service routine library is not available to the FORTRAN-62 system; other service routines are available in the CO-OP Monitor.

In FORTRAN-62, magnetic tape input and/or output can be overlapped with internal computation by the use of BUFFER IN and BUFFER OUT statements. Each BUFFER statement causes one block of data to be read into or written from sequential core storage locations, in either binary or BCD format. ENCODE and DECODE statements facilitate the internal packing, unpacking, and format control of buffered input and output data. ENCODE (i, n, v) L causes the variables in list L to be converted according to FORMAT statement n and stored in array v as a unit record i characters long ready for output; DECODE (i, n, v) L performs the complementary function of unpacking input data. The statement IF (UNIT, i) permits checking of a buffered input-output operation for completion, end-of-file condition, and parity error; it should always appear before any statement referencing a variable involved in a buffered transfer.

When the standard FORTRAN input-output statements are executed, the central processor is occupied throughout the operation with format conversions, so no simultaneity is possible. The buffered input-output facility of FORTRAN-62 permits the programmer to take advantage of most of the hardware facilities for simultaneous operations, and it can significantly decrease the execution time for routines where the ratio of input-output to computation is high.

Translation and execution of programs written in the FORTRAN-62 language are controlled by the CO-OP Monitor System.

Restrictions and extensions of the FORTRAN-62 language relative to IBM 709/7090 FORTRAN II are summarized below. Extensions (4) through (9) represent the main improvements over CDC's FORTRAN-60 language.

Restrictions:

(1) Double precision and complex arithmetic are not permitted.

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.14 Description (Contd.)

Restrictions (Contd.)

(2) It is not possible to test for arithmetic overflow; IF ACCUMULATOR OVERFLOW, IF QUOTIENT OVERFLOW, and IF DIVIDE CHECK result in unconditional branches to the second statement listed.

(3) IF SENSE SWITCH and IF SENSE LIGHT test the status of specific core storage locations. The monitor system must be used to alter the settings of the pseudo sense switches.

(4) The following statements have not been implemented: FREQUENCY, READ DRUM, WRITE DRUM.

(5) All allocation statements (DIMENSION, COMMON, and EQUIVALENCE) must precede the first executable statement in a source program.

(6) The CHAIN feature, which facilitates segmentation of programs too large to fit into core storage, has not been implemented. (The CO-OP Monitor, however, includes an overlay system that can be used by programs in any source language.)

(7) Symbolic coding can be incorporated only in the form of separate subroutines called by the FORTRAN program.

Extensions:

(1) Names may be up to 8 characters in length.

(2) The following number ranges can be handled:

Floating point: . .	10^{-308} to 10^{+308}
Integer:	-2^{47} to $+2^{47}$
Boolean:	16 octal digits (48 bits).

(3) No parenthesized statement number list is required in an assigned GO TO statement.

(4) Subscripts may be integer constants, integer variables, integer functions, or any fixed point arithmetic expressions.

(5) BUFFER IN and BUFFER OUT initiate the buffered reading or writing of one block on magnetic tape from sequential core storage locations, beginning and ending with specified variables.

(6) The statements IF (UNIT), IF (EOF), and IF (IOCHECK) permit tests for completion of buffered input-output operations, for end-of-file conditions, and for parity errors.

(7) ENCODE and DECODE control code or radix conversions and packing into and unpacking from sequential locations of a list of variables (usually those involved in a buffered input or output operation).

(8) The statements READ and WRITE may designate any available input or output device.

.14 Description (Contd.)

Extensions (Contd.)

(9) The COMMON data storage area can be divided into numbered or labeled blocks; this facilitates the transfer of information between subprograms.

.15 Publication Date: . . . . June, 1962.

.2 PROGRAM STRUCTURE

.21 Divisions: . . . . one division, composed of the following types of statements.

Procedure statements: . . algebraic formulae.
comparisons and jumps.
input and output.

Data statements: . . . . FORMAT: describes the layout, size, scaling, and code of input-output data.
EQUIVALENCE: used to cause two variables to have a common location or to specify synonyms.
COMMON: used to cause a name to be common to more than one segment rather than local to each.
DIMENSION: describes the elements in each dimension of an array or set of arrays.
EXTERNAL: declares the following identifiers to be function names.

.22 Procedure Entities

Program:	subroutines and functions.
Subroutine:	statements.
Function:	statements.
Statement:	characters; blanks are ignored.

.23 Data Entities

Arrays:	all variables.
Item:	integer variable or constant. floating point variable or constant. Boolean variable or constant. Hollerith item. alphameric item.
Hollerith item:	alphameric item that can only be used for output.
Alphameric:	alphameric item that can only be input during a run; it can be used for output, or as a format statement.

.24 Names

.241 Simple name formation

Alphabet:	A to Z, 0 to 9.
Size:	1 to 8 char.
Avoid key words: . . .	no.
Formation rule: . . .	first char must be letter. do not use final F if name is more than 3 char long.

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.242 Designators

Procedures

Statement label: . . .	unsigned integer.
Function label: . . .	same as variable being defined.
Subroutine label: . .	none.

Data

Integer variables: .	initial I, J, K, L, M, N.
Floating point variables:	any other initial letter.

Equipment

Card:	implied by verbs READ, PUNCH.
Magnetic tape: . . .	use key word TAPE, or READ, WRITE.
Printer:	implied by verb PRINT.
Comments:	C in col. 1 of statement.
Translator control: .	key words EQUIVALENCE, COMMON.

.25 Structure of Data Names

.251 Qualified names: . . . . none.

.252 Subscripts

Number per item: . .	0 to 3.
Applicable to:	all variables.
Class may be	
Special index variable:	no.
Any variable:	only integers.
Literal:	yes; only integers.
Expression:	any integer expression or function.
Form may be	
Integer only:	yes.
Signed:	no.
Truncated fraction: .	no.
Rounded fraction: . .	no.

.253 Synonyms

Preset:	EQUIVALENCE statement causes sharing of storage locations.
Dynamically set: . . .	no.

.26 Number of Names

.261 All entities no practical limit.

.262 Procedures

Numbered statements:	all inter-related; no practical limit.
Subroutines:	
Functions:	
Others:	

.263 Data

Files:	no limit.
Record formats: . . .	no practical limit.
Items:	no practical limit.

.264 Equipment

Tape units:	total of 64 units.
Card readers:	
Card punches:	
Printers:	

.27 Region of Meaning of Names: . . . . all names are local to the program, subroutine, or function in which they are defined unless specified explicitly or by block name in COMMON statement.

.3 DATA DESCRIPTION FACILITIES

.31 Methods of Direct Data Description

.311	Concise item picture: .	FORMAT statement only.
.312	List by kind:	no.
.313	Qualify by adjective: . .	no.
.314	Qualify by phrase: . . .	no.
.315	Qualify by code:	first letter of name.
.316	Hierarchy by list: . . .	no.
.317	Level by indenting: . .	no.
.318	Level by coding:	no.
.319	Others	
	Array size:	DIMENSION (4, 7).
	Four-digit integer: . .	FORMAT (I4).
	Four-digit integers, 5:	FORMAT (5I4).
	Floating point items: .	FORMAT (F8.3, E10.4)for +999.999 and +.0000E+99.

.32 Files and Reels: . . . . own coding.

.33 Records and Blocks

.331	Variable record size: .	dynamic.
.332	Variable block size: . .	fixed (preset variable for buffered input-output).
.333	Record size range: . .	1 to N blocks.
.334	Block size	
	READ TAPE, WRITE TAPE:	128 words (binary format).
	READ INPUT TAPE, WRITE OUTPUT TAPE:	120 characters (BCD format).
	READ, PUNCH: . . .	80 columns.
	PRINT:	120 characters.
	BUFFER IN, BUFFER OUT:	variable.
.335	Choice of record size: .	READ, WRITE statement.
.336	Choice of block size: .	fixed for each non-buffered input-output statement type; BUFFER statements specify names of first and last variables in block.
.337	Sequence control: . . .	own coding.
.338	In-out error control: .	own coding, using IF clauses.
.339	Blocking control:	none; 1 or more full blocks per logical record.

.34 Data Items

.341	Designation of class: .	by name.
.342	Possible classes	
	Integer:	yes.
	Fixed point:	no.
	Floating point:	yes.
	Logical:	yes.
	Alphameric:	yes.
.343	Choice of external radix:	FORMAT statement.
.344	Possible external radices	
	Decimal:	yes.
	Octal:	yes.
.345	Internal justification: .	alpha automatic left justified. integers automatic right justified.
.346	Choice of external code:	FORMAT statement and READ, WRITE statement.

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.347 Possible external codes
- Decimal: yes.
- Octal: yes.
- Hollerith: yes.
- Alphameric: yes.

.348 Internal item size
- Variable size: fixed.
- Designation: none.
- Range
  - Fixed point numeric: fixed, 1 word.
  - Floating point numeric: fixed, 1 word.
  - Alphameric: fixed, 1 word of up to 8 characters.

.349 Sign provision: optional.

.35 Data Values

.351 Constants
- Possible sizes
  - Integer: 2^{47}.
  - Fixed point: none.
  - Floating point: 10^{-308} to 10^{+308}.
  - Alphameric: 120 characters.
  - Boolean: 16 octal digits.
- Subscriptable: yes.
- Sign provision: optional.

.352 Literals: same as constants.
.353 Figuratives: own coding; e.g., TEN = 10.0.
.354 Conditional variables: computed GO TO.

.36 Special Description Facilities

.361 Duplicate format: by multiple references to a single FORMAT statement.
.362 Re-definition: COMMON statement. EQUIVALENCE statement.
.363 Table description
- Subscription: mandatory, in DIMENSION statement.
- Multi-subscripts: 1 to 3.
- Level of item: variables.

.364 Other subscriptable entities: input-output units.

.4 OPERATION REPERTOIRE

.41 Formulae

.411 Operator List

+:	addition, also unary.
-:	subtraction, also unary.
*:	multiplication.
/:	division.
**:	exponentiation.
=:	is set equal to.
ABSF ( )‡:	absolute value.
INTF ( )‡:	entire.
MODF (A, B)‡:	remainder A ÷ B.
MAXOF (A, ...)‡:	max value; fixed argument.
MAX1F (A, ...)‡:	max value; floating argument.
MINOF (A, ...)‡:	min value; fixed argument.
MIN1F (A, ...)‡:	min value; floating argument.
DIMF (A, B)‡:	diminish A by B.
SIGNF (A, B)‡:	transfer sign of A to B.

.411 Operator list (Contd.)

FLOATF ( ):	float an integer.
XFIXF ( ):	fix floating point variable.
LOGF ( ):	natural log.
SINF ( ):	sine.
ASINF ( ):	arc sine.
COSF ( ):	cosine.
ACOSF ( ):	arc cosine.
EXPF ( ):	exponential.
SQRTF ( ):	square root.
ATANF ( ):	arctangent.
TANHF ( ):	hyperbolic tangent.
RANIF ( ):	produce random number (even distribution).
RNDEVF ( ):	produce random number (Gauss distribution).

‡ denotes function may have prefix X to denote fixed point result.

.412 Operands allowed
- Classes: numeric only.
- Mixed scaling: yes.
- Mixed classes: only in exponentiation and functions.
- Mixed radices: no.
- Literals: yes.

.413 Statement structure
- Parentheses
  - a - b - c means: (a-b) - c.
  - a + b x c means: a + (b x c).
  - a ÷ b ÷ c means: (a ÷ b) ÷ c.
  - a^{b^c} means: illegal; parentheses must be used.
- Size limit: 660 char.
- Multi-results: no.

.414 Rounding of results: truncation of integers at each step in expression.

.415 Special cases

	Fixed	Floating
x = -x:	K = -K	X = -X.
x = x + 1:	K = K + 1	X = X + 1.
x = 4.7 y:	K = 47*K/10	X = 4.7 * Y.
$x = 5x10^7 + y^2$:	50000000+L**2	X = 5.E7+Y**2.
x = |y|:	K = XABSF(L)	X = ABSF(Y).
x = entire (3.5):	K = XINTF(L)	X = INTF(Y).

.416 Typical examples: X = (-B+SQRTF(B*B-4.0 *A*C))/(2.0*A).

.42 Operations on Arrays

.421 Matrix operations: none.
.422 Logical operations
- Sizes of operands: 48 bits.
- AND: *
- Inclusive OR: +
- Exclusive OR: none.
- NOT: -
- Designation: B in col. 1 of each Boolean statement.

.423 Scanning: none.

.43 Other Computation: subprograms in FORTRAN, COBOL, or symbolic languages may reference one another.

.44 Data Movement and Format

.441 Data copy example: Y = X.
.442 Levels possible: items.

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.443 Multiple results: . . . . none.
.444 Missing operands: . . . not possible.
.445 Size of operands
Exact match: . . . . . implied, except for alpha or input-output.
Alignment rule
Numbers: . . . . . . right justified or normalized.
Alpha: . . . . left justified.
Filler rule
Numbers: . . . . . . zeros.
Alpha: . . . . blanks.
Truncating rule
Numbers: . . . . . . truncate at left.
Alpha: . . . . truncate at right.
Variable size destination: . . . . no.
.446 Editing possible
Change class: . . . . yes.
Change radix: . . . . yes.
Insert editing symbols
Actual point: . . . . automatic.
Suppress zeroes: . . automatic.
Insert: . . . . automatic point.
Float: . . . . - sign only.
.448 Special moves: . . . . . none.
.449 Character manipulation: none.

.45 File Manipulation

Open: . . . . own coding.
Close: . . . . own coding.
Advance to next record: READ, WRITE, PUNCH, PRINT, BUFFER.
Step back a record: . . BACKSPACE.
Set restart point: . . . none.
Restart: . . . . none.
Start new reel: . . . . . own coding.
Start new block: . . . . implied in each input-output statement.
Search on key: . . . . . none.
Rewind: . . . . REWIND.
Unload: . . . . none.

.46 Operating Communication

.461 Log of progress: . . . . PRINT uses on-line printer.
.462 Messages to operator: . same as log (error messages are automatically typed on console typewriter).
.463 Offer options: . . . . . PAUSE and type decimal integer.
PRINT message and PAUSE.
.464 Accept option: . . . . . IF SENSE SWITCH n.

.47 Object Program Errors

Error	Discovery	Special Actions
Overflow:	none.	
In-out:	IF (IO CHECK)	own coding.
Invalid data:	format checks	typed messages.
I/O device busy:	IF (UNIT)	own coding.

.5 PROCEDURE SEQUENCE CONTROL

.51 Jumps

.511 Destinations allowed: . statement.
.512 Unconditional jump: . . GO TO N.
.513 Switch: . . . . GO TO M, or GO TO M, (35, 47, 18).
.514 Setting a switch: . . . . ASSIGN 35 TO M.
.515 Switch on data: . . . . . GO TO (35, 47, 18) I.

.52 Conditional Procedures

.521 Designators
Condition: . . . . . . IF.
Procedure: . . . . . . implied.
.522 Simple conditions: . . . expression or variable versus zero.
.523 Conditional relations: . IF (A) n1, n2, n3: If value of expression A is less than, equal to, or greater than zero, respectively, go to statement n1, n2, or n3.
.524 Variable conditions: . . expression always against zero.
.525 Compound conditionals: no.
.528 Typical examples: . . . IF (X**2.0 - 3.0) 29, 37, 18; go to 29, 37, or 18 if x^2-3 is respectively less than, equal to, or greater than zero.

.53 Subroutines

.531 Designation
Single statement: . . . not possible.
Set of statements
First: . . . . SUBROUTINE.
Last: . . . . END.
.532 Possible subroutines: . any number of statements.
.533 Use in-line in program: no.
.534 Mechanism
Cue with parameters: CALL XXX (X, Y, Z).
Number of parameters: . . . . maximum of 64.
Cue without parameters: . . . . CALL XXX.
Formal return: . . . . RETURN at least once.
Alternative return: . . none.
.535 Names
Parameter call by value: . . . . none.
Parameter call by name: . . . . yes.
Non-local names: . . use COMMON.
Local names: . . . . . all.
Preserved own variables: . . . . . . all.
.536 Nesting limit: . . . . . no limit.
.537 Automatic recursion allowed: . . . . no.

.54 Function Definition by Procedure

.541 Designation
Single statement: . . . same as set.
Set of statements
First: . . . . FUNCTION.
Last: . . . . END.
.542 Level of procedure: . . any number of statements.
.543 Mechanism
Cue: . . . . by name in expression.
Formal return: . . . . RETURN.

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.544 Names
- Parameter call by value: . . . . none.
- Parameter call by name: . . . . yes.
- Non-local names: . . use COMMON.
- Local names: . . . . . all.
- Preserved own variables: . . . . . . all.

.55 Operand Definition by Procedure: . . . . . . none.

.56 Loop Control

.561 Designation of loop
- Single procedure: . . none.
- First and last procedures: . . . . . current place to named end; e.g., DO 173 I = 1, N, 2.

.562 Control by count: . . . none.

.563 Control by step
- Parameter
  - Special index: . . . . no.
  - Any variable: . . . . integer only.
- Step: . . . . positive integers.
- Criteria: . . . . greater than.
- Multiple parameters: no.

.564 Control by condition: . no.

.565 Control by list: . . . . no.

.566 Nesting limit: . . . . . no limit.

.567 Jump out allowed: . . . yes.

.568 Control variable exit status: . . . . available.

.6 EXTENSION OF THE LANGUAGE: . . . . . can write new function in library.

.7 LIBRARY FACILITIES

.71 Identity: . . . . CO-OP Monitor Library.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.

.722 Expandable master: . . yes.

.73 Storage Form: . . . . . magnetic tape; variable length blocks in relocatable binary format.

.74 Varieties of Contents: . subroutines. functions. service routines.

.75 Mechanism

.751 Insertion of new item: . separate run, using FORTLIB Compiler.

.752 Language of new item: . FORTRAN, CODAP 1, or COBOL.

.753 Method of call: . . . . . named in procedures.

.76 Types of Routines

.761 Open routines exist: . . no.

.762 Closed routines exist: . yes.

.763 Open-closed is variable: no.

.8 TRANSLATOR CONTROL

.81 Transfer to Another Language: . . . . . . only by calling a subroutine written in that language.

.82 Optimizing Information Statements

.821 Process usage statements: . . . . . . none.

.822 Data usage statements: COMMON. EQUIVALENCE.

.83 Translator Environment: . . . . . no.

.84 Target Computer Environment: . . . . . no.

.85 Program Documentation Control: . . . . no.

.9 TARGET COMPUTER ALLOCATION CONTROL

.91 Choice of Storage Level: no.

.92 Address Allocation: . . none.

.93 Arrangement of Items in Words in Unpacked Form: . . . . standard for numerics.

.94 Assignment of Input-Output Devices: . . . specified in input-output statements; re-assignable at load time.

.95 Input-Output Areas: . . automatic (ENCODE and DECODE permit packing into and unpacking from named input-output areas for buffered operations).

PROCESS ORIENTED LANGUAGE: FORTRAN-63

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.1 GENERAL

.11 Identity: . . . . FORTRAN-63.

.12 Origin: . . . . Computer Division, Control Data Corporation.

.13 Reference: . . . . . . FORTRAN-63 General Information Manual (Preliminary).

.14 Description

FORTRAN-63 contains all the facilities of its predecessor, FORTRAN-62, and a number of valuable extensions. It will be implemented for both the 1604 and the more powerful CDC 3600 computer system. FORTRAN-63 has most of the capabilities of IBM 7090/7094 FORTRAN as contained in the IBJOB Processor ("FORTRAN IV"), but will not be directly compatible with it.

The most significant improvement over CDC FORTRAN-62 is the provision for eight distinct modes of arithmetic. Single and double precision floating point, integer, complex, and logical arithmetic are standard; the remaining three types are "arbitrary" in mode and execution. No changes in the compiler are required when a new type of arithmetic is inserted. The user specifies the variables involved in a TYPE declaration and inserts library routines which execute the cues generated by the compiler. Each library routine for a non-standard type of arithmetic contains 12 arithmetic sections and two input-output sections; each section implements a particular instruction type.

FORTRAN-63 is a part of the CO-OP Monitor System, which controls translation of source programs and execution of object programs.

Restrictions and extensions of the FORTRAN-63 language relative to IBM 709/7090 FORTRAN II are summarized below. Extensions (10) through (18) also summarize the improvements over CDC's FORTRAN-62 language.

Restrictions:

(1) The following statements have not been implemented: FREQUENCY, READ DRUM, WRITE DRUM.

(2) IF ACCUMULATOR OVERFLOW and IF QUOTIENT OVERFLOW result in unconditional branches to the second statement listed; but see Extension (16).

(3) Six sense switches and 48 sense lights are simulated by programmed binary flip-flops; alteration of the switch settings is a Monitor function.

.14 Description (Contd.)

Restrictions (Contd.)

(4) The following declarative statements (if used) must procede the first executable statement in a source program: PROGRAM, SUBROUTINE, FUNCTION, DIMENSION, COMMON, EQUIVALENCE.

(5) The CHAIN feature, which facilitates segmentation of programs too large to fit into core storage, has not been implemented. (The CO-OP Monitor, however includes an overlay system that can be used by programs in any source language.)

(6) Symbolic coding can be incorporated only in the form of separate subroutines called by the FORTRAN program.

Extensions:

(1) Names may be up to 8 characters in length.

(2) The following number ranges can be handled:
- Floating point: . . . 10^{-308} to 10^{+308}
- Integer: . . . . -2^{47} to $+ 2^{47}$
- Boolean: . . . . 16 octal digits (48 bits).

(3) No parenthesized statement number list is required in an assigned GO TO statement.

(4) Subscripts may be integer or floating point constants, variables, functions, or expressions.

(5) BUFFER IN and BUFFER OUT initiate the buffered reading or writing of one block on magnetic tape from sequential core storage locations, beginning and ending with specified variables.

(6) The statements IF (UNIT), IF (EOF), and IF (IOCHECK) permit tests for completion of buffered input-output operations, for end-of-file conditions, and for parity errors.

(7) ENCODE and DECODE control code or radix conversions and packing into or unpacking from sequential locations of a list of variables (usually those involved in a buffered input or output operation).

(8) The statements READ and WRITE may designate any available input or output device.

(9) The COMMON data storage area can be divided into numbered or labeled blocks; this facilitates the transfer of information between subprograms.

(10) Data values can be assigned at load time to variables in labeled COMMON storage by means of the DATA statement.

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.14 Description (Contd.)

Extensions (Contd.)

(11) Arithmetic and input-output may be performed in any of eight modes: integer, real (single precision floating point), double precision floating point, complex, logical (Boolean), and three "arbitrary modes" (see text above).

(12) TYPE declarations (e.g., TYPE LOGICAL A, B, C) are used to designate the modes of lists of variables. Variables that do not appear in TYPE statements are considered type integer if their names begin with I, J, K, L, M, or N; otherwise, they are type real.

(13) Mixed arithmetic is permitted. The mode of an expression is the same as the highest order TYPE of operand in it. The order of types, from lowest to highest, is integer, real, double, complex. Mode conversions are performed as necessary.

(14) The following symbols may be used in arithmetic/conditional statements:

.EQ. :	equal.
.NE. :	not equal.
.GT. :	greater than.
.GE. :	greater than or equal to.
.LT. :	less than.
.LE. :	less than or equal to.
.AND. :	logical and.
.OR. :	logical or.
.NOT. :	not.

(15) Conditional statements may be of the type IF (e) n1, n2; where e is a simple or compound logical expression. A branch to statement n1 is executed if e is true, or to n2 if e is false.

(16) IF OVERFLOW FAULT and IF EXPONENT FAULT test the status of the corresponding indicators and branch accordingly.

(17) $ can be used as a statement separator, permitting more than one source statement to be written on a line.

(18) Non-subscripted variables can be used as array dimensions; e.g., DIMENSION A (J, K).

.15 Publication Date: . . . July, 1962 (preliminary specifications; translator is currently in field test status).

.2 PROGRAM STRUCTURE

.21 Divisions: . . . . . . one division, composed of the following types of statements.

Procedure statements:	algebraic formulae.
	comparisons and jumps.
	input and output.
Data statements:	FORMAT: describes the layout, size, scaling, and code of input-output data.
	EQUIVALENCE: used to cause two variables to have a common location or to specify synonyms.
	COMMON: used to cause a name to be common to more than one segment rather than local to each.
	DIMENSION: describes the elements in each dimension of an array or set of arrays.
	TYPE: specifies mode of a list of variables; INTEGER, REAL, DOUBLE, COMPLEX, LOGICAL.
	DATA: assigns constant values to variables at load time.
	EXTERNAL: declares the following identifiers to be function names.

.22 Procedure Entities

Program:	subroutines and functions.
Subroutine:	statements.
Function:	statements.
Statement:	characters; blanks are ignored.

.23 Data Entities

Arrays:	all variables.
Item:	integer variable or constant.
	floating point variable or constant.
	double precision floating variable or constant.
	complex variable or constant.
	Boolean variable or constant.
	Hollerith item.
	alphameric item.
Hollerith item:	alphameric item that can only be used for output.
Alphameric:	alphameric item that can only be input during a run; it can be used for output, or as a format statement.

.24 Names

.241 Simple name formation

Alphabet:	A to Z, 0 to 9
Size:	1 to 8 char.
Avoid key words:	no.
Formation rule:	first char must be letter.

.242 Designators

Procedures

Statement label:	unsigned integer.
Function label:	same as variable being defined.
Subroutine label:	no designator.

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.242 Designators (Contd.)

Data (if not specified in a TYPE statement)
- Integer variables: . . . . . . initial I, J, K, L. M, N.
- Floating point variables: . . . any other initial letter.

Equipment
- Card: . . . . . . implied by verbs READ, PUNCH.
- Magnetic tape: . . use key word TAPE; or READ, WRITE.
- Printer: . . . . . implied by verb PRINT.

Comments:. . . . . C in col. 1 of statement.

Translator control: . . . . . . key words EQUIVALENCE, COMMON, TYPE.

.25 Structure of Data Names

.251 Qualified names: . . none.

.252 Subscripts
- Number per item: . 0 to 3.
- Applicable to: . . . all variables.
- Class may be
  - Special index variable: . . . . . . no.
  - Any variable: . . . yes.
  - Literal: . . . . . yes; except Hollerith.
  - Expression: . . . yes.
- Form may be
  - Integer only: . . . . yes.
  - Signed: . . . . . . yes.
  - Truncated fraction: . . . . . . yes.
  - Rounded fraction: . . . . . . no.

.253 Synonyms
- Preset: . . . . . . EQUIVALENCE statement causes sharing of storage locations.
- Dynamically set: . . no.

.26 Number of Names

.261 All entities: . . . . . all inter-related; no practical limits.

.262 Procedures
- Numbered statements: . . . . . .
- Subroutines: . . . .
- Functions: . . . . .
- Others: . . . .

} all inter-related; no practical limits.

.263 Data
- Files: . . . . . . no limit.
- Record formats: . . no practical limit.
- Items: . . . . . . no practical limit.

.264 Equipment
- Tape units: . . . .
- Card readers: . . .
- Card punches: . . .
- Printers: . . . . .

} total of 64 units.

.27 Region of Meaning of Names: . . . . . . all names are local to the program, subroutine, or function in which they are defined unless specified explicitly or by block name in COMMON statement.

.3 DATA DESCRIPTION FACILITIES

.31 Methods of Direct Data Description

.311 Concise item picture: . . . . FORMAT statement only.

.312 List by kind: . . . . yes; TYPE declarations.

.313 Qualify by adjective: . . . . no.

.314 Qualify by phrase . . no.

.315 Qualify by code: . . . first letter of name if not listed by TYPE.

.316 Hierarchy by list: . . no.

.317 Level by indenting: . . no.

.318 Level by coding: . . . no.

.319 Others
- Array size: . . . . DIMENSION (4, 7).
- Four-digit integer: . . . . . . FORMAT (I4).
- Four-digit integers, 5: . . . . . FORMAT (5I4).
- Floating point items: . . . . . . FORMAT (F8.3, E10.4) for +999.999 and +.0000E+99.

.32 Files and Reels: . . . own coding.

.33 Records and Blocks

.331 Variable record size: . . . . dynamic.

.332 Variable block size: . . . . fixed (preset variable for buffered input-output).

.333 Record size range: . . 1 to N blocks.

.334 Block size
- READ TAPE, WRITE TAPE: . . . . 128 words (binary format).
- READ INPUT TAPE, WRITE OUTPUT TAPE: . . . . 120 characters (BCD format).
- READ, PUNCH:. . . . 80 columns.
- PRINT: . . . . 120 characters.
- BUFFER IN, BUFFER OUT: . . . . variable.

.335 Choice of record size: . . . . READ, WRITE statement.

.336 Choice of block size: . . . . fixed for each non-buffered input-output statement type; BUFFER statements specify names of first and last variables in block.

.337 Sequence control: . . . own coding.

.338 In-out error control: . . . . own coding, using IF clauses.

.339 Blocking control: . . . none; 1 or more full blocks per logical record.

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.34 Data Items

.341 Designation of class: . . . . by name or TYPE declaration.

.342 Possible classes
- Integer: . . . . yes.
- Fixed point: . . . . . no.
- Floating point: . . . . yes.
- Logical: . . . . yes.
- Double precision: . . . . yes.
- Complex: . . . . yes.
- Alphameric: . . . . . yes.

.343 Choice of external radix: . . . . FORMAT statement.

.344 Possible external radicies
- Decimal: . . . . . . yes.
- Octal: . . . . yes.

.345 Internal justification: . . . . alpha automatic left justified. integers automatic right justified.

.346 Choice of external code: . . . . FORMAT statement and READ, WRITE statement.

.347 Possible external codes
- Decimal:. . . . . . . yes.
- Octal: . . . . yes.
- Hollerith: . . . . . . yes.
- Alphameric: . . . . . yes.

.348 Internal item size
- Variable size: . . . . fixed.
- Designation: . . . . . none.
- Range
  - Fixed point numeric: . . . . . fixed, 1 word.
  - Floating point numeric: . . . . . fixed, 1 or 2 words.
  - Complex: . . . . . fixed, 2 words.
  - Logical
    - Subscripted: . . . fixed, 1 bit.
    - Non-subscripted:. . fixed, 1 word.
  - Alphameric: . . . . fixed, 1 word of up to 8 characters.

.349 Sign provision: . . . . optional.

.35 Data Values

.351 Constants
- Possible sizes
  - Integer: . . . . . . $\pm 2^{47}$
  - Fixed point: . . . . none.
  - Floating point: . . . 10^{-308} to 10^{+308}.
  - Alphameric: . . . . 120 characters.
  - Logical: . . . . . . 16 octal digits.
- Subscriptable: . . . . yes.
- Sign provision: . . . . optional.

.352 Literals: . . . . same as constants.

.353 Figuratives:. . . . . . own coding; e.g., TEN = 10.0.

.354 Conditional variables: . . . . computed GO TO.

.36 Special Description Facilities

.361 Duplicate format: . . . by multiple references to a single FORMAT statement.

.362 Re-definition: . . . . . COMMON statement. EQUIVALENCE statement.

.363 Table description.
- Subscription: . . . . . mandatory, in DIMENSION statement.
- Multi-subscripts: . . . 1 to 3.
- Level of item: . . . . variables.

.364 Other subscriptable entities: . . . . input-output units.

.4 OPERATION REPERTOIRE

.41 Formulae

.411 Operator List

- +: . . . . addition, also unary.
- -: . . . . subtraction, also unary.
- *: . . . . multiplication.
- /: . . . . division.
- **: . . . . exponentiation.
- =: . . . . is set equal to.
- ABSF ( ) ‡: . . . . . . absolute value.
- INTF ( ) ‡: . . . . . . entire.
- MODF (A, B) ‡: . . . . remainder A ÷ B.
- MAXOF (A, ...) ‡: . . . max value; fixed argument.
- MAXIF (A, ...) ‡: . . . max value; floating argument.
- MINOF (A, ...) ‡: . . . min value; fixed argument.
- MIN1F (A, ...) ‡: . . . min value; floating argument.
- DIMF (A, B) ‡: . . . . diminish A by B.
- SIGNF (A, B) ‡: . . . . transfer sign of A to B.
- FLOATF ( ): . . . . . float an integer.
- XFIXF ( ): . . . . . fix a floating point variable.
- LOGF ( ): . . . . . . natural log.
- SINF ( ): . . . . sine.
- ASINF ( ): . . . . . . arc sine.
- COSF ( ): . . . . . . cosine.
- ACOSF ( ): . . . . . . arc cosine.
- EXPF ( ): . . . . . . exponential.
- SQRTF ( ): . . . . . . square root.
- ATANF ( ):. . . . . . arctangent.
- TANHF ( ): . . . . . hyperbolic tangent.
- RANIF ( ): . . . . . . produce random number (even distribution)
- RNDEVF ( ): . . . . . produce random number (Gauss distribution).

‡ denotes function may have prefix X to denote fixed point result.

.412 Operands allowed
- Classes: . . . . any of eight.
- Mixed scaling: . . . . yes.
- Mixed classes: . . . . yes.
- Mixed radices: . . . . yes.
- Literals:. . . . . . . yes.

.413 Statement structure
- Parentheses
  - a - b - c means:. . . (a-b) - c.
  - a + b x c means: . . a + (b x c).
  - a ÷ b ÷ c means: . . (a ÷ b) ÷ c.
  - a^{b^c} means: illegal; parentheses must be used.
- Size limit: . . . . . . 660 char.
- Multi-results: . . . . no.

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.414 Rounding of results: . . . truncation of integers at each step in expression.

.415 Special cases

	Fixed	Floating
x = -x:	K = -K	X = -X.
x = x + 1: . . .	K = K + 1	X = X + 1.
x = 4.7 y: . . .	K = 47*K/10	X = 4.7 * Y.
$x = 5x10^7+y^2$:	50000000+L**2	X = 5.E7+Y**2.
x = |y|:	K = XABSF(L)	X = ABSF(Y).
x = entire (3.5):	K = XINTF(L)	X = INTF(Y).

.416 Typical examples: . . . X = (-B + SQRTF(B*B-4.0 *A*C))/(2.0*A).

.42 Operations on Arrays

.421 Matrix operations: . . . none.
.422 Logical operations
Sizes of operands: . . 48 bits (1 bit if subscripted).
AND: . . . . .AND.
Inclusive OR: . . . . . .OR.
Exclusive OR: . . . . none.
NOT: . . . . .NOT.
Designation: . . . . . TYPE LOGICAL.
.423 Scanning: . . . . none.

.43 Other Computation: . . subprograms in symbolic or COBOL language may reference or be referenced by FORTRAN subprograms.

.44 Data Movement and Format

.441 Data copy example: . . Y = X.
.442 Levels possible: . . . . items.
.443 Multiple results: . . . . none.
.444 Missing operands: . . . not possible.
.445 Size of operands
Exact match: . . . . . implied, except for alpha or input-output.
Alignment rule
Numbers: . . . . . . right justified or normalized.
Alpha: . . . . left justified.
Filler rule
Numbers: . . . . . . zeros.
Alpha: . . . . blanks.
Truncating rule
Numbers: . . . . . . truncate at left.
Alpha: . . . . truncate at right.
Variable size destination: . . . . no.
.446 Editing possible
Change class: . . . . yes.
Change radix: . . . . yes.
Insert editing symbols
Actual point: . . . . automatic.
Suppress zeroes: . . automatic.
Insert: . . . . automatic point.
Float: . . . . - sign only.
.448 Special moves: . . . . . none.
.449 Character manipulation: none.

.45 File Manipulation

Open: . . . . own coding.
Close: . . . . own coding.
Advance to next record: READ, WRITE, PUNCH, PRINT, BUFFER.
Step back a record: . . BACKSPACE.
Set restart point: . . . none.

.45 File Manipulation (Contd.)

Restart: . . . . none.
Start new reel: . . . . . own coding.
Start new block: . . . . implied in each input-output statement.
Search on key: . . . . . none.
Rewind: . . . . REWIND.
Unload: . . . . none.

.46 Operating Communication

.461 Log of progress: . . . . PRINT uses on-line printer.
.462 Messages to operator: . same as log (error messages are automatically typed on console typewriter).
.463 Offer options: . . . . . PAUSE and type decimal integer.
PRINT message and PAUSE.
.464 Accept option: . . . . . IF SENSE SWITCH n.

.47 Object Program Errors

Error	Discovery	Special Actions
Overflow:	IF clauses	own coding.
In-out:	IF (IO check)	own coding.
Invalid data:	format checks	typed messages.
I/O device busy:	IF (UNIT)	own coding.

.5 PROCEDURE SEQUENCE CONTROL

.51 Jumps

.511 Destinations allowed: . statement.
.512 Unconditional jump: . . GO TO N.
.513 Switch: . . . . GO TO M, or GO TO M, (35, 47, 18).
.514 Setting a switch: . . . . ASSIGN 35 TO M.
.515 Switch on data: . . . . . GO TO (35, 47, 18), I.

.52 Conditional Procedures

.521 Designators
Condition: . . . . . . IF.
Procedure: . . . . . . implied.
.522 Simple conditions: . . . expression or variable versus zero.
.523 Conditional relations
Equal: . . . . .EQ., =.
Not equal: . . . . . . .NE.
Greater than: . . . . . .GT.
Less than: . . . . . . .LT.
Greater than or equal: .GE.
Less than or equal: . . .LT.
.524 Variable conditions: . . true or false for logical expressions.
less than, equal to, or greater than zero for arithmetic expressions.
.525 Compound Conditionals
IF x AND y: . . . . . yes.
IF x OR y: . . . . . . yes.
IF x DO a AND y DO b: no.
IF x DO a OR y DO b: no.
.526 Alternative designator: branch to second named statement if logical expression is false.
.527 Condition on alternative: no.

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.528 Typical examples: . . . IF (X**2.0-3.0) 29, 37, 18; go to 29, 37 or 18 if X^2-3 is respectively less than, equal to, or greater than zero.
IF (((A*B).GT.C).AND.(D.EQ.E)) 7, 12; go to 7 if the expression is true and to 12 if false.

.53 Subroutines

.531 Designation
- Single statement: . . . not possible.
- Set of statements
  - First: . . . . SUBROUTINE.
  - Last: . . . . END.

.532 Possible subroutines: . any number of statements.
.533 Use in-line in program: no.
.534 Mechanism
- Cue with parameters: CALL XXX (X, Y, Z).
- Number of parameters: . . . . maximum of 64.
- Cue without parameters: . . . . CALL XXX.
- Formal return: . . . . RETURN at least once.
- Alternative return: . . none.

.535 Names
- Parameter call by value: . . . . none.
- Parameter call by name: . . . . yes.
- Non-local names: . . use COMMON.
- Local names: . . . . . all.
- Preserved own variables: . . . . . . all.

.536 Nesting limit: . . . . . no limit.
.537 Automatic recursion allowed: . . . . no.

.54 Function Definition by Procedure

.541 Designation
- Single statement: . . . same as set.
- Set of statements
  - First: . . . . FUNCTION.
  - Last: . . . . END.

.542 Level of procedure: . . any number of statements.
.543 Mechanism
- Cue: . . . . by name in expression.
- Formal return: . . . . RETURN.

.544 Names
- Parameter call by value: . . . . none.
- Parameter call by name: . . . . yes.
- Non-local names: . . use COMMON.
- Local names: . . . . . all.
- Preserved own variables: . . . . . . all.

.55 Operand Definition by Procedure: . . . . none.

.56 Loop Control

.561 Designation of loop
- Single procedure: . . none.
- First and last procedures: . . . . . current place to named end; e.g., DO 173 I = 1, N, 2.

.562 Control by count: . . . none.
.563 Control by step
- Parameter
  - Special index: . . . . no.
  - Any variable: . . . . integer only.
- Step: . . . . positive integers.
- Criteria: . . . . greater than.
- Multiple parameters: no.

.564 Control by condition: . no.
.565 Control by list: . . . . no.
.566 Nesting limit: . . . . . 127.
.567 Jump out allowed: . . . yes.
.568 Control variable exit status: . . . . available.

.6 EXTENSION OF THE LANGUAGE: . . . . . can write new function in library.

.7 LIBRARY FACILITIES

.71 Identity: . . . . CO-OP Monitor Library.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.

.73 Storage Form: . . . . . magnetic tape; variable length blocks in relocatable binary format.

.74 Varieties of Contents: . subroutines.
functions.
service routines.

.75 Mechanism

.751 Insertion of new item: . separate run.
.752 Language of new item: . FORTRAN, CODAP 1, or COBOL.
.753 Method of call: . . . . . named in procedures.

.76 Types of Routines

.761 Open routines exist: . . no.
.762 Closed routines exist: . yes.
.763 Open-closed is variable: no.

.8 TRANSLATOR CONTROL

.81 Transfer to Another Language: . . . . . . only by calling a subroutine written in that language.

.82 Optimizing Information Statements

.821 Process usage statements: . . . . . . none.
.822 Data usage statements: COMMON.
EQUIVALENCE.

.83 Translator Environment: . . . . . no.

.84 Target Computer Environment: . . . . . no.

.85 Program Documentation Control: . . . . . . no.

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.9 TARGET COMPUTER ALLOCATION CONTROL

.91 Choice of Storage Level: no.

.92 Address Allocation: . . none.

.93 Arrangement of Items in Words in Unpacked Form: . . . . standard for numerics.

.94 Assignment of Input-Output Devices: . . . specified in input-output statements; re-assignable at load time.

.95 Input-Output Areas: . . automatic (ENCODE and DECODE permit packing into and unpacking from named input-output areas for buffered input-output operations).

PROCESS ORIENTED LANGUAGE: COBOL

§ 165

.1 GENERAL

.11 Identity: . . . . 1604 COBOL.

.12 Origin: . . . . CODASYL committee; implemented by Control Data Corporation.

.13 Reference: . . . . . STM 07-09 September, 1962.

.14 Introduction

The CDC implementation of COBOL 1961 is scheduled to become available at the start of 1963; however, preliminary information is now available. It is stated that it will include all of Required COBOL 61, the electives defined below, and the SORT provision of Extended COBOL 61. Compilation will take place under the supervision of the CO-OP Monitor, and, therefore, a programmer is able to mix COBOL languages with FORTRAN 62, or CODAP 1 assembly language within the same program. The actual choice of I/O units does not take place until object time in this system and, therefore, the RECORDING MODE IS clause of the file description is meaningless. This choice also requires that the operating instructions be written in terms of the CO-OP Monitor names for I/O units, such as "Standard Input Medium," instead of "Tape No. 7."

In addition to the SORT and ENTER functions, the most important electives that provide new procedural facilities are:

#16: RANGE IS...clause, which allows a condition name to be associated with one or more values or ranges of value.

#26: USE verb, which allows standard, library or own COBOL coding procedures to be implemented when file or reel labels are being processed, or when input-output errors have been detected. A separate section allows the items in a label block to be named and described.

#33: Fourteen decimal digits are used in arithmetic.

There are three other features, which simplify the writing of programs rather than adding to the available facilities:

#1: COMPUTE, which allows the use of +, -, *, /, **, =, in formulae.

#28: MOVE CORRESPONDING, which simplifies the movement of relevant portions of one data area to another, and performs any necessary editing.

#25: INCLUDE verb, which allows procedure paragraphs to be extracted from a library at compilation time.

.14 Introduction (Contd.)

Deficiencies: . . . . . none in prospect.

Electives:

These are listed below by reference to the keys under which they are discussed in the Users' Guide (4:161).

NO	TITLE	COMMENT
#1	Further characters	+, -, *, /, **, =.
#2	Further characters	= only; not > or <
#4	Long literals	Up to 225 characters
#5	Figurative Constants	UPPER-BOUND(S); LOWER BOUND(S).
#6	Figurative Constants	HIGH-VALUE(S); LOW VALUE(S).
#8	Variable Length Blocks	
#9	FILE CONTAINS	
#13	Table Size	Allows table and array sizes to be set at object time.
#16	RANGE IS	
#20	VALUE option	see description above.
#21	Labels	see description above.
#22	COMPUTE	see description above.
#24	ENTER	see description above.
#25	INCLUDE	see description above.
#26	USE	see description above.
#27	LOCK	
#28	MOVE CORRESPONDING	see description above.
#32	Formulas	
#33	Operand size	see description above.
#34	Specific relationship	IS UNEQUAL TO, EQUALS, EXCEEDS
#35	IF...NOT ZERO	
#36	Implied subjects	
#37	ANDS or ORS	
#39	Labels and Errors	
#43	File Description Library	
#45	I/O Procedures Library	
#47	DATE - COMPILED	

Extensions

The SORT facility allows the sorting of a file on a number of keys. Each record in the file can be processed before and/or after the sorting process.

PROCESS ORIENTED LANGUAGE: CXA

§ 166.

.1 GENERAL

.11 Identity: . . . . . . CXA
Control Data EXtended Algol.

.12 Description

The CXA language has not been fully released, but preliminary information is available. Control Data Corporation expects to release the CXA translator in January, 1963.

CXA is stated to be based on ALGOL 58 and is to include BALGOL as a subset. As CXA is designed to run under the control of the CO-OP Monitor, however, the BALGOL External Statement, which allows the use of machine language, has not been implemented. The CXA translator is being produced by a Compiler Generating System. This system uses one set of tables to describe the source language and other tables to describe the object language to produce a compiler. It is, therefore, possible by modifying the tables and re-running the CGS to produce a modified version of the CXA compiler for a modified language, thereby giving a user some freedom to select his own ALGOL dialect if he wishes to do so.

MACHINE ORIENTED LANGUAGE: CODAP-1

§ 172.

.1 GENERAL

.11 Identity: . . . . CODAP-1.

.12 Description

CODAP-1 is an outgrowth of CODAP, which is the assembly routine that has been available for the CDC 1604 since 1960. The assembly language performs two roles; first, it allows a programmer to write machine instructions and constants in a convenient form, and second, it provides a systematic means of using any library, monitor, or subprogram as desired.

Labelling is unusually free, requiring one letter with an option of being followed by up to seven further alphameric characters for all labels, except one type of data area which uses an all numeric label.

There are two types of data areas; both called "COMMON" areas. These are differentiated in the language by having alphameric (called "Labelled COMMON") or numeric (called "Numeric COMMON") labels, and in use by being able, or not able, to preset the contents of the areas at load time only if "Labelled COMMON" is used.

Communication with other independently written routines is arranged by the EXTernal Symbol linkage and LIBrary pseudo-ops. These operations provide for a label to be common to more than one routine and also control the library call and the setting of parameter values in the LIBrary routines. The actual linkage is created at loading time.

.2 LANGUAGE FORMAT

.21 Diagram

LOCN	OPN	B	M	REMARKS	
8	6	2	21	40	size in card columns

.22 Legend

LOCN: . . . . unique label allowing cross-referencing within or outside the subprogram.

OPN: . . . . (a) Machine code, in absolute or numeric form.
(b) Pseudo-op codes, which produce parameters used by a supervisor routine, controlling storage allocation, linkage with other programs, and input assignments.

.22 Legend (Contd.)

B: . . . . designates an index register, a jump key, a stop key, or a subinstruction; can be written in absolute or mnemonic form.

M: . . . . (a) for machine code instructions, an address, in absolute or relative form, or a literal constant.
(b) for pseudo-ops a series of parameters extending into remarks column.

.23 Corrections: . . . . . no special facilities.

.24 Special Conventions

.241 Compound addresses: . . . . . e.g., SYMBOL + 5.
.242 Multi-addresses: . . . none.
.243 Literals:. . . . . . . up to 40 char, any code.
.244 Special coded addresses: . . . . . * means this address.
** means - 0.
.245 Other
Radix definition: . . OCT, DEC, BCD, FLX pseudo codes preceeding the literals and constants.

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . no practical limit.
.312 Common label formation rule: . . . . . 1 to 8 alphamerics including certain special characters with no embedded blanks. First character must be non-numeric.
.313 Reserved labels: . . . none.
.315 Designators: . . . . . none.
.316 Synonyms: . . . . . yes, via EQUivalence pseudo-op.

.32 Universal Labels: . . none, but individual labels can be made local to several independent subprograms, being called an External Table Entry to each subprogram.

.33 Local Labels

.331 Labels for procedures
Existence: . . . . . optional.
Formation rule
First character: . . non-numeric character.
Others: . . . . . any non-blank character.
Number of characters: . . . . . 1 to 8.

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.332 Labels for library routines: . . . . . . same as for procedures.
.333 Labels for constants: . . . . . . same as for procedures, or as an element of an array within a numbered COMMON statement.
.334 Labels for files: . . . none.
.335 Labels for records: . . none.
.336 Labels for variables: . . . . same as for procedures.
.337 Labels for other subprograms: . . . . . same as for procedures.
.338 Others
Labels for blocks containing preset data
Existence: . . . . optional.
Formation rule: . . 1 to 8 alphabetics, "Labeled Common Blocks."
Labels for reserved blocks for working storage
Existence: . . . . optional.
Formation rule: . . 8 numeric or blank characters, an all blank label is acceptable, "Numbered Common Blocks."
Labels for arrays:. . same as for procedures.

.4 DATA

.41 Constants

.411 Maximum size constants

Machine Form	External Language
Integer:	14 decimal digits plus sign. 16 octal digits plus sign.
Fixed numeric: . .	not allowed.
Floating numeric: .	14 digits with a decimal or binary exponent of up to 3 digits, plus sign.
Alphameric, BCD, Flexowriter or Teletype coding: . . .	64 characters.

.412 Maximum size literals
Integer
Decimal: . . . . . 32,767.
Octal: . . . . . . 77,777.
Fixed numeric: . . . none.
Floating numeric: . . none.
Alphameric: . . . . 64 characters.

.42 Working Areas

.421 Data layout
Implied by use: . . . no.
Specified in program: . . . . . . BLOCK and COMMON statements.
.422 Data type: . . . . . . implied by use.
.423 Redefinition: . . . . . use of BLOCK statements.

.43 Input-Output Areas: . . specified in program.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
Existence: . . . . . optional with absolutes.
Number: . . . . . . 64 basic with 8 true alternatives.
Example: . . . . . FDV; Floating Divide.
Comment: . . . . . where one op code has more than one type of operation, specified by "B," different mnemonics may be used for the common code.
.512 Absolute
Existence: . . . . . optional with mnemonic.
Number: . . . . . 64 (only 62 used).
Example: . . . . . 45 for Add Logical.

.52 Macro-Codes: . . . . none, nor any facilities for programmer insertion.

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control
Allocation counter: . various pseudo-op.
Label adjustment: . . various pseudo-op.
Annotation: . . . . . REMark pseudo-op.
.542 Allocation counter
Set to absolute: . . . yes. (ORG pseudo-op; absolute or predefined entry in location).
Set to label: . . . . yes.
Set relative to label: . . . . . . yes.
Step forward: . . . . implied by set relative to label.
Step backward: . . . implied.
Reserve area: . . . yes.
.543 Label adjustment
Set labels equal: . . yes.
Set label relative: . . . . yes.
Set absolute value:. . yes.
Clear label table: . . not within single subprogram; yes, by dividing into separate subprograms.
.544 Annotation
Comment phrase: . . yes.
Title phrase: . . . . no.
.545 Other
Allocation mode: . . absolute or relocatable.

.55 Facilities Omitted: none.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: none.

.62 Special Functions

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.621 Facilities: . . . . . . none, any could be added in installation library.

.622 Method of call: . . . . LIBrary pseudo-op.

.63 Overlay Control: . . . none, but reserved space, called COMMON, can be redefined for each subprogram.

.64 Data Editing

.641 Radix conversion: . . . decimal-to-binary for initial constants.

Code translation: . . . alphabetic-to-BCD, Flexowriter and Teletype.

.642 Format control: . . . none.

.65 Input-Output Control: . . . . own program, with I/O pseudo-op check on I/O units involved.

.66 Sorting: . . . . none.

.67 Diagnostics: . . . . . none in CODAP 1 system, up to 10 snapshots and various dumps incorporated in CO-OP Monitor.

.7 LIBRARY FACILITIES

.71 Identity: . . . . installation library.

.72 Kinds of Libraries

.721 Fixed master: . . . . no.

.722 Expandable master: . . yes.

.73 Storage Form: . . . . magnetic tape.

.74 Varieties of Contents: . . . . as determined by installation.

.75 Mechanism

.751 Insertion of new item: . . . . via CO-OP Monitor.

.752 Language of new item: . . . . CODAP 1, or FORTRAN-62.

.753 Method of call: . . . . LIB code identifies routine. EXT identifies entry point. Manual lists special calls.

.76 Insertion in Program

.761 Open routines exist: . . ?

.762 Closed routines exist: . . . . yes.

.763 Open-closed is optional: . . . . ?

.764 Closed routines appear once: . . . . yes.

.8 INSTRUCTION CODE REPERTOIRE

.81 Macros: . . . . none.

.82 Pseudos

Code	Description
BCD:	Binary Coded Decimal.
BES:	Reserve Block, End with Symbol.
BLOCK:	Identify Data Region.
BSS:	Reserve Block, Starting with Symbol.
COMMON:	Identify COMMON arrays.
DEC:	Decimal Constant.
EJECT:	Eject Line Printer Page.
END:	Physical End of Subprogram.
ENTRY:	Entry Point Symbol.
EQU:	Equivalence.
EXT:	External Symbol.
FINIS:	Physical End of Source Program.
FLX:	Flexowriter Code.
IDENT:	Identifier.
I/O:	Input/Output Assignements.
LIB:	Identify Library Routine.
OCT:	Octal Value.
ORG:	Origin Address.
ORGE:	Origin Address Relocatable.
REM:	Remarks Only.
SPACES:	Space Listing.
TEL:	Teletype Codes.

.84 Direct: . . . . see Section 243:121.100.

PROGRAM TRANSLATOR: CODAP-1

§ 182.

.1 GENERAL

.11 Identity: . . . . CODAP-1.

.12 Description:

The CODAP-1 Translator produces output in either relocatable or absolute binary coding. The output is always on magnetic tape. The input may be either punched cards, paper tape, or magnetic tape in card format. This translator will also assemble CODAP source language programs provided that certain restrictions (described below) are observed.

The translator produces a listing of language errors and of the volume of storage required for the subprogram. An optional listing on tape or on-line printer of both the source and object programs is available.

CODAP-1 is particularly designed to produce Relocatable Binary Output suitable for the CO-OP Monitor. The translator is stored on the CODAP Monitor tape as a subsidiary control system. It can be used as part of the CO-OP Monitor facilities as a "Translate and Run" assembler.

The relationship between the CODAP-1 and CODAP translators is summarized below.

If any of the following are desired, use CODAP-1:

Relocatable Binary Output.
Compatibility with CO-OP Monitor.
Pseudo-ops. BLOCK, COMMON, ENTRY, EXT.

If any of the following are desired, use CODAP:

Compatibility with AUTOMONITOR.
Pseudo-ops. WST, RST.

.13 Originator: . . . . . . Control Data Corporation.

.14 Maintainer: . . . . . . Control Data Corporation.

.15 Availability: . . . . . presently available in 1604 version.

.2 INPUT

.21 Language

.211 Name: . . . . CODAP-1.

.22 Form

.221 Input media: . . . . . . magnetic tape.
punched card.
punched paper tape.

.222 Obligatory ordering: . . . . none.

.223 Obligatory grouping: . . . . BLOCK, defining data area, is immediately followed by associated COMMON defining arrays.

.23 Size Limitations

.231 Maximum number of source statements: . . no practical limit.

.232 Maximum size source statements: . . . . . 80 columns.

.233 Maximum number of data items: . . . . . no practical limit.

.234 Other

Maximum number of Symbols: . . . . . . 4,096, with 4,096 Equivalent names.

Maximum number of Block Common Names: . . . . 62, with 62 Equivalent names.

Maximum number of Named Entry Points: 100, with 100 Equivalent names.

Maximum number of Pseudo-operation Names: . . . . 31.

Maximum number of Machine Operation Names: . . . . 64.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . absolute or relocatable binary.

.312 Language style: . . . binary coding suitable for CO-OP Monitor.

.313 Output media: . . . . magnetic tape.

.32 Conventions

.321 Standard inclusions: . . . . none.

.322 Compatible with: . . . CO-OP Monitor.

.33 Documentation

Subject	Provision
Source program:	listing 2 (optional).
Object program:	listing 2 (optional).
Storage map:	top and bottom limits only (listing 1).
Restart point list:	none.
Language errors:	listing 2 (mandatory).
Entry points to subroutines:	listing 1.
External symbols used in subroutines:	listing 1.

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.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Pass 1: . . . . stores the input; if necessary uses a scratch tape.
Pass 2: . . . . a) produces IDC coding from program Identity card, and BLOCK and COMMON sequences.
b) produces a binary program tape.
c) optionally produces the Entry Point Symbol Table, and the Linkage Address Table for use by the CO-OP Monitor loader.
d) produces a transfer address to initiate the routine.

.42 Optional Mode

.421 Translate: . . . . yes.
.422 Translate and run: . . yes.
.423 Check only: . . . . . . yes.
.424 Patching: . . . . no.
.425 Up-dating: . . . . no.

.43 Special Features

.431 Alter to check only: . . . . no.
.432 Fast unoptimized translate: . . . . no.
.433 Short translate on restricted program: . . . . no.

.44 Bulk Translating: . . . . yes under CO-OP Monitor facilities; otherwise none.

.45 Program Diagnostics

.451 Tracers: . . . . none.
.452 Snapshots: . . . . up to 10 in CO-OP Monitor.
.453 Dumps: . . . . yes, automatically or under operator's control in CO-OP Monitor.

.46 Translator Library: . . none.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . none, but see CO-OP Monitor
.512 Space required for each input-output file: . . . implied in program.
.513 Approximate expansion of procedures: . 1 to 1.

.52 Translation Time

Conditions

I : . . . . using IBM 088 Card Reader at 650 cards/min input and CDC 1607 Tape output.
II : . . . . using CDC 1607 Tape input and output.
III: . . . . using CDC 606 Tape input and output.

.521 Normal Translating
I : . . . . 500 cards/min (*).
? + 0.002S mins (*).
II : . . . . 2000 cards/min (*).
? + 0.005S min (*).
III: . . . . ?

(*) Manufacturer's estimate considered to be reliable but not final.

.53 Optimizing Data: . . . none.

.54 Object Program Performance: . . . . . . unaffected.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . . CDC 1604 or 1604-A with 32K core store and 4 magnetic tapes.
.612 Larger configuration advantages: . . . none.

.62 Target Computer

.621 Minimum configuration: . . . . CDC 1604 computer with one input device.
.622 Usable extra facilities: . . . . all available facilities.

.7 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries	none.	
Duplicate names:	check	listed on output.
Improper format:	check	listed on output.
Incomplete entries:	check	listed on output.
Target computer overflow:	checked at load time.	
Inconsistent program:	none.	

.8 ALTERNATIVE TRANSLATORS

Computer: . . . . CDC 1604.
Identity: . . . . CODAP.
Date: . . . . 1960.
Comment: . . . . ancestor of CODAP-1 that is not compatible with CO-OP Monitor, has slightly different pseudo-ops.

PROGRAM TRANSLATOR: ADVANCE REPORT

§ 183.

.1 GENERAL

.11 Identity: . . . . 1604/1604-A COBOL.

.12 Description

The 1604/1604-A COBOL is scheduled to become available in December, 1962, and to compile COBOL statements at a rate of 450 cards per minute. It will require a 32K CDC 1604 or 1604-A as a translating computer, and will use between two and five tape units. An on-line printer, card reader, punch may each be substituted for one of the tape units.

Currently, no details of advisable styling are available.

Available listings will be:

- Error Messages.
- Reference listing of the source program.
- Optional Data Map (see illustration).
- Optional Listing of Object Program.
- Optional Relocatable binary card deck.

Modes of operation are:

- Compilation only.
- Compile and execute.
- Compile only selected portion of a program.

This last facility is designed to allow fast error correction in source language. This is practical because no scratch tape is used during the compilation.

The translator is divided into two phases: Phase I, which operates on the Identification, Environment, and Data Division; and Phase II, which operates on the Procedure Division. Only one pass through the source tape is required, and the speed, quoted above, of 450 cards per minute is applicable for a five tape system, with listing of the object program suppressed.

The following description of the two phases is taken from CDC's memorandum dated September 12, 1962.

Phase I

During this phase, the source statements of the Identification, Environment, and Data Division are read. As they are read:

a. A reference listing of the statements is generated (if requested).

.12 Description (Cont'd)

b. The statements are checked for format, conflicting or illegal descriptions, and incomplete or duplicate definitions. As errors are detected, diagnostics are generated following the source statement or group of source statements that are in error.

c. The File Environment and Reference Tables are partially created. The File Environment Table contains the descriptions of internal and external files. The Reference Table lists all data descriptions required to create the symbol table for Phase II processing.

If certain critical errors have been detected during Phase I, processing is terminated. Otherwise, the two tables are finalized. This consists of:

a. Additional checking and diagnostic generation.

b. Assigning of relocatable addresses to the data items.

c. Preparation of constants.

d. Generation of a map of memory allocated to the data items.

After this final processing, the Reference Table is complete enough to serve as a symbol table for Phase II processing.

The File Environment Table will have information added during Phase II processing. It will become a part of the object program to serve as a directory for the handling of files.

During finalization of the tables, critical errors may be detected. These errors will not stop the processing, but will prevent execution of the program.

Phase II

The statements of the Procedure Division are read. As the statements of each paragraph are read:

a. The statements are checked for format, legal wording, completeness, and continuity. As errors are detected, diagnostics are generated following the source statement or group of statements in error.

b. Data items referenced by the statements are looked up in the Reference Table and an object code generated to perform the action. Checks for correct use of data items are performed as the object code is generated.

c. As each paragraph is completed, it is formed into a closed subroutine. It is then output in one or all of the forms:

§ 183.

.12 Description (Contd.)

1. An object code listing.

2. A relocatable binary card deck.

3. A subroutine on the load-and-go unit for execution.

d. Information is added to the File Environment Table to complete it.

e. The logical flow of the program is catalogued in the Sequence Table.

The entire Procedure Division is processed even though errors have been detected. Detection of a critical error will cause suppression of card decks, load-and-go tape, and program execution.

OPTIONAL DATA MAP

WORKING STORAGE

LEVEL NO.	NAME OF DATA ENTRY	CHARPOS R	P	LOC	SIZE	CLASS	USAGE	SYNCH	JUST	BLNK IF 0	POINT LOC	OCCURS	DEP ON	EDIT
01	RECEIVER	0	0	00044	285	NUM								
02	B100	0	0	00044	1	NUM	FX DEC		R					
02	B101	0	1	00044	1	NUM	FX DEC				5L			
02	B102	0	2	00044	1	NUM	FX DEC				13L			
02	B103	0	3	00044	1	NUM	FX DEC				21L			
02	B104	0	4	00044	1	NUM	FX DEC				50L			
02	B105	0	5	00044	5	NUM	FX DEC		R					
02	B106	0	2	00045	5	NUM	FX DEC				5L			

PROGRAM TRANSLATOR: FORTRAN-60

§ 184.

.1 GENERAL

.11 Identity: FORTRAN-60

.12 Description

The FORTRAN-60 Translator is a load-and-go type which solves most of its allocation problems by calling the six index registers by the fixed-point variables I through N. These registers are called whether or not a programmer actually uses them. It can be seen, therefore, that programs written to take advantage of this feature will run very much faster than ones written without such planning.

In general, given well-designed programs, comparisons to good hand-coding show a 20 per cent increase in time usage and a doubling of space requirements (see Paragraph .54).

An interesting feature is the comparative lack of size limitations (see Paragraph .234).

FORTRAN-60 runs under its own monitor and is not presently available to operate under CO-OP Monitor control. A systematic translation of FORTRAN-60 programs to FORTRAN-62 is under way and is being coordinated by the CO-OP Users Group. At present it is not possible to forecast whether or not FORTRAN-62 and FORTRAN-63 will entirely supersede FORTRAN-60.

.13 Originator: . . . . . Control Data Corporation.

.14 Maintainer: . . . . Control Data Corporation.

.15 Availability: . . . . 1959.

.2 INPUT

.21 Language

.211 Name: . . . . FORTRAN-60.
.212 Exemptions: . . . . none.

.22 Form

.221 Input media: . . . . punched cards or magnetic tape.
.222 Obligatory ordering: . all statements must be in correct sequence.
.223 Obligatory grouping: . none.

.23 Size Limitations

A number of tables are prepared during compilation. While none of these tables have a fixed size (they are push-down type tables), the sum of their entries must not exceed 16,000 locations. The main tables are listed below; alongside is given the number of locations each entry uses.

Table	Locations/Entry
Address Assignment Table: Storage of location symbols from the generated code: .	2
Equivalence Table: Information from equivalence statements: . . .	2
Constants Table: Storage of constants used by object program:	1
Assigned Variables: Variables which have been assigned locations:	2
Format Numbers: Format Statement Numbers:	1
DO-Exits: Statement number at end of range of a DO:	1
Statement Numbers: Statement numbers assigned locations:	2
Common Variables: Names appearing in COMMON statements:	1
Arrays: Names appearing in DIMENSION statements: . . .	1

.3 OUTPUT

.31 Object Program: . . . none necessarily. An intermediate assembly (MAP) listing can be output; but frequently this is converted to machine language and left in storage at the end of compilation. See paragraph .32.

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.32 Conventions

.321 Standard inclusions: . . FORTLIB Compiler. run on "FORTLIB Compiler". This adds a FORTRAN program, presently in storage, onto a library tape.

.33 Documentation

Subject	Provision
Source program: . .	optional (Listing 1).
Object program: . .	MAP listing (Listing 2).
Storage map: . . .	none.
Restart point list: .	no.
Language errors: . .	error printouts placed on tape; errors in FORMAT statements noted at object time.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Statements are read in, decoded, and the appropriate code generated in an intermediate language called MAP. The statement may then be listed (Listing 1). After all statements have been read, passes are made over the MAP language to satisfy all conditions. The MAP may then be output as a listing (Listing 2). It is converted to machine language and stored ready for execution.

It is possible and normal for small enough programs to be compiled in a manner such that the MAP is stored in memory and converted to running code without restoring to intermediate tape passes.

.42 Optional Mode

.421 Translate: . . . . . yes.
.422 Translate and run: . . yes.
.423 Check only: . . . . . yes.
.424 Patching: . . . . . . no.
.425 Updating: . . . . . . no.

.43 Special Features

.431 Alter to check only: . yes.
.432 Fast unoptimized translate: . . . . . not applicable.
.433 Short translate on restricted program: . no.

.44 Bulk Translating: . . no.

.45 Program Diagnostics: . . . . none.

.46 Translator Library

.461 Identity: . . . . . . reference library.
.462 User restriction: . . general.

.463 Form
Storage medium: . . magnetic tape.
Organization: . . . grouped by:
Compiler and compiler subprograms.
Mathematical subprograms.
Service programs.

.464 Contents
Routines: . . . . . closed.
Functions: . . . . yes.
Data Descriptions: . no.

.465 Librarianship
Insertion: . . . . systems run.
Amendment: . . . . systems run.
Call Procedure: . . name followed by parameters. Some can be used in procedural statements (such as LOGF), others are called by service and debugging programs.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead
Name: . . . . . . resident package.
Space: . . . . . . 2,054 words.

.513 Approximate expansion of procedures: . . averages approx. 5 or 6 instructions per FORTRAN statement (**).

.52 Translation Time

Condition I: . . . . . CDC 1607 Tape input, no output.
Condition II: . . . . CDC 1607 Tape input and output.

.521 Normal Translating:
I: . . . . $0.16 + 0.0023$ S min.
II: . . . . $0.16 + 0.0025$ S min.
(where S is the number of elementary statements.)

.54 Object Program Performance

Type	Time	Space
Elementary algebra:	increased by 20%	doubled.
Complex formulae:	increased by 20%	doubled.
Deep nesting:	increased by 20%	doubled.
Heavy branching:	increased by 20%	doubled.
Complex subscripts:	increased by 50%	doubled.
Data editing:	unaffected	unaffected.
Overlapping operations:	not possible.	

(**) Analyst's estimate, provided as a guide only.

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.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . CDC 1604 with at least 2 tape units.

.612 Larger configuration advantages: . . . . additional tape units save tape handling time and on-line card and printer time.

.62 Target computer

.621 Minimum configuration: . . . CDC 1604.

.622 Usable extra facilities: . . . . paper tape.
CDC 1605 card units and printer.
CDC 1607 tape units.
CDC 1610 card units and printer.
CDC 1612 printer.

.7 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Missing entries:	check	halt compilation before running.
Unsequenced entries:	check	halt compilation before running.
Duplicate names:	check	halt compilation before running.
Improper format:	check	halt compilation before running.
Incomplete entries:	check	halt compilation before running.
Target computer overflow:	check	halt compilation before running.
Inconsistent program:	equivalence check	halt compilation before running.
Size limitations exceeded:	check	halt compilation before running.

.8 ALTERNATIVE TRANSLATORS

Computer	Identity	Date
CDC 1604	FORTRAN 62	1962
CDC 1604	FORTRAN 63	1963

PROGRAM TRANSLATOR: FORTRAN-62

§ 185.

.1 GENERAL

.11 Identity: . . . . FORTRAN-62.

.12 Description

FORTRAN-62 operates under the CO-OP Monitor, and translates programs or portions of programs into relocatable binary code suitable for use in the CO-OP Monitor system. In this system, each separate subprogram is an independent entity, without the restriction that the subprograms which are compiled, or which are executed together, need be written in the same language. CODAP 1, the CDC 1604 Assembly Program, is the only other language besides FORTRAN-62 presently available. However, COBOL and FORTRAN 63 will be available shortly.

Under CO-OP Monitor techniques, compile or load-and-go techniques are possible, although this is no part of the translator. Object program diagnostic features are also handled in this way. The integration of subprograms, or routines to be performed at object time, does not require them either to be available at compilation, or to be manually integrated before running. All such librarianship is done automatically by the CO-OP loader at object time, with the translator merely generating the necessary parameters.

By comparison with FORTRAN-60, the translation process for FORTRAN 62 is approximately 20 per cent quicker. The object program performance is not much different than that of the FORTRAN-60: 20 per cent more time and twice as much space as hand-coded routines. However, the recommended style is very different. In FORTRAN-62, I, J, K, L, M, N are ordinary fixed point variables, in no way different from any others. Index Registers are reserved to control DO-loops, so that the recommended style is to use DO-loops, and not to nest them deeper than five at any one point. Subscripts are evaluated each time they are used; therefore, it is also desirable to avoid unnecessary multiple subscripts.

.13 Originator: . . . . . . Control Data Corporation.

.14 Maintainer: . . . . . . Control Data Corporation.

.15 Availability: . . . . . currently in field test.

.2 INPUT

.21 Language

.211 Name: . . . . FORTRAN-62.
.212 Exemptions: . . . . . none.

.22 Form

.221 Input media: . . . . . magnetic tape; paper tape; cards.

.23 Size Limitations

.232 Maximum size source statements: . . . . . 100 variables and constants.
.234 Others
No. of nested parentheses: . . . . . . 39.
No. of nested DO statements: . . . 20.
Dimensioned variables: . . . . . . 300.

.3 OUTPUT

.31 Object Program

.311 Language name: . . . relocatable binary.
.312 Language style: . . . relative machine code.
.313 Output media: . . . . magnetic tape, or cards.

.32 Conventions

.321 Standard inclusions: . . Master Control System.
.322 Compatible with: . . . CO-OP Monitor.

.33 Documentation

Subject	Provision
Source program: . .	Listing 1.
Object program: . . .	Listing 3.
Storage map:	Listing 2 (partially; only external symbols mapped).
Restart point list: . .	no.
Language errors: . .	Listing 3, and at object time.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Each statement is processed as it is input; machine language object programming is produced and stored, while the source program is listed along with any error checks. At the end of the compilation, the program, still in storage, is available for optional punch out or listing.

.42 Optional Mode

.421 Translate: . . . . . yes.
.422 Translate and run: . . yes.
.423 Check only: . . . . . yes.
.424 Patching: . . . . . . no.
.425 Updating: . . . . . . subroutines can be assembled separately.

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.43 Special Features

.431 Alter to check only: . . automatic on error.
.432 Fast unoptimized translate: . . . . . no.
.433 Short translate on restricted program: . . . . . . no.

.44 Bulk Translating: . . . yes, via CO-OP Monitor.

.45 Program Diagnostics: . see CO-OP Monitor, Operating Environment.

.46 Translator Library

.461 Identity: . . . . Library Tape.
.462 User restriction: . . . none.
.463 Form
Storage medium: . . magnetic tape.
Organization: . . . . as loaded.
.464 Contents
Routines: . . . . . . closed only.
Data Descriptions: . . . . no.
Subprograms: . . . . yes, (can have been in CODAP, COBOL, or FORTRAN).
.465 Librarianship
Insertion: . . . . . LIBEDIT routine.
Amendment: . . . . LIBEDIT routine.
Call Procedure: . . . CALL, or use as a function, causes calling sequence to be formed, which in turn initiates the relocatable loader of the CO-OP Monitor system to locate and load the actual routines from tape at object time.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead
Name: . . . . CO-OP Monitor.

.52 Translation Time

.521 Normal translating: . . 0.1 + 0.002 S min, where S is the number of statements; includes card input, source and object program listings, and binary tape output.

.53 Optimizing Data

Index Registers: . . . the control variables of the first 5 DO loops in any nest are allocated to index registers.

.54 Object Program Performance

Type	Time	Space
Elementary algebra	increased by approx 20%	doubled.
Complex formulae	increased by approx 20%	doubled.
Deep nesting	increased by approx 20%	doubled.
Heavy branching	increased by approx 20%	doubled.
Complex subscripts	doubled	doubled.
Data editing	unaffected	unaffected.
Overlapping operations	unaffected, if programmer checks translator methods	unaffected

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . . CDC 1604 with 4 tape units.
.612 Larger configuration advantages: . . . . none.

.62 Target Computer

.621 Minimum configuration: . . . . CDC 1604 with 2 tape units.
.622 Usable extra facilities: . . . . CDC 1604-A central processor.
CDC 1605 card equipment.
CDC 1607 tape units.
CDC 1608 tape units.
CDC 1610 card equipment.
CDC 1612 printer.
CDC 606 tape unit.
CDC 1617 card reader.

.8 ALTERNATIVE TRANSLATORS

Computer	Identity	Date
CDC 1604	FORTRAN 60	1959
CDC 1604	FORTRAN 63	1963

PROGRAM TRANSLATOR: FORTRAN-63

§ 186.

.1 GENERAL

.11 Identity: . . . . FORTRAN-63.
Publication No. 514.

.12 Description

The FORTRAN-63 translator operates on both the CDC 1604 and 1604-A computers, and provides a tape output for use under the CO-OP Monitor System.

No limit on the various storage tables is imposed by the translator. A single push-down type of storage allocation is used, and if the entire area allocated to table storage in core memory is actually filled, then a scratch tape is used to hold the overflow. This technique allows freedom from counting the entries of particular tables and gives good utilization of storage during the compilation.

Analyses are made during compilation to determine:

1. The flow throughout each DO loop.
2. Any possible simplification of each arithmetic expression by the removal of common subexpressions.
3. Whether subscript modification is dependent on input data at object time. (If so, a small generator program is operated at object time to determine modification methods.)

During the running of a FORTRAN-63 program, some 3,000 locations are taken up by the CO-OP Monitor, FORTRAN-63, resident programs, etc. The FORMAT statements are used interpretively, being processed each time an input or output occurs. Beyond this and the subscript modification mentioned above, no translation occurs at object time.

An interesting change in the translating technique is the treatment of multisubscripts. Instead of these subscripts being computed each time they are used (which may involve two multiplications and an addition), the basic value of each subscript combination is stored and modified each time an alteration to one of its components is made. This modification only involves one multiplication or one addition, and is thus considerably shorter than the time involved in any one evaluation of a single subscript. The overall effect of this depends on the number of times a subscript value is used, as opposed to the number of times its value changes whether or not it is actually used. In straightforward, lightly branched, comparatively short subprograms there will almost always be a gain in using this subscripting method. In other cases the gain is more problematical, and losses are possible (see Paragraph .533).

.12 Description (Contd.)

The FORTRAN-63 program is designed to run under control of the CO-OP Monitor and automatic buffering on card and printer output is provided by the system.

.13 Originator: . . . . . . Control Data Corporation.

.14 Maintainer: . . . . . . Control Data Corporation.

.15 Availability: . . . . . . January, 1963 for CDC 1604.
April, 1963 for CDC 3600.

.2 INPUT

.21 Language

.211 Name: . . . . FORTRAN-63.
.212 Exemptions: . . . . . none.

.22 Form

.221 Input media: . . . . . magnetic tape, cards, paper tape.

.23 Size Limitations

.231 Maximum number of source statements: . . no limit (A scratch tape is used if necessary.)
.232 Maximum size source statements: . . . . . 660 characters.
.233 Maximum number of data items: . . . . . no limit (A scratch tape is used if necessary.)
.234 Others

The following tables are contained in storage. The total amount of storage allocated to tables must be used up prior to the use of a scratch tape to augment this space. However there is no limit as to how much space any table or group of tables may take, provided there is room in internal storage.

1. Declared Identifier List. An entry is made for each unique identifier appearing in a TYP2, COMMON, SUBROUTINE, FUNCTION, EQUIVALENCE, or DATA statement. Associated with the entry are the definition and properties associated with the identifier, e.g., its mode, size, dimensionality, etc.
2. Index Variable List. An entry is made for each unique identifier appearing in a standard index function (given below).

§ 186.

.234 Others (Contd.)

3. Index Function List. An entry is made for each unique index function, in the form:

   $i * \Delta i + j * \Delta j + k * \Delta k$, where i, j, k are the subscript variables associated with an array indentifier and Δi, Δj, Δk are the corresponding multipliers.

4. List of Constant Values. An entry is made for each unique number (converted to a common base) appearing in the source code.

5. Arithmetic Statement Function List. An entry is made for each identifier used to define an arithmetic statement function.

6. Local Identifier List. An entry is made for each identifier not appearing in the declared identifier list.

7. String List. This is an internal representation of the source statement.

8. Assembly List. An entry is made for each (assembly language) order generated.

.3 OUTPUT

.31 Object Program

.312 Language style: . . . . machine code.
.313 Output media: . . . . magnetic tape, or cards.

.32 Conventions

.321 Standard inclusions: . . . . CO-OP Monitor Library.
.322 Compatible with: . . . CO-OP Monitor.

.33 Documentation: . . . details not yet available.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Statements are compiled into a symbolic assembly language, a statement at a time, until a DO statement is encountered. Following this, and until the right bound of the DO is encountered, a global analysis involving the flow, use of index registers, depth of nesting, etc., is performed. The processing into assembly orders then continues. Finally, an assembly into relocatable binary format is performed.

.42 Optional Mode

.421 Translate: . . . . . . yes.
.422 Translate and run: . . via CO-OP monitor.
.423 Check only: . . . . . yes.
.424 Patching: . . . . . . any one subprogram can be recompiled separately.
.425 Up-dating: . . . . . . no.

.43 Special Features

.431 Alter to check only: . . . . no.
.432 Fast unoptimized translate: . . . . . . no.
.433 Short translate on restricted program: . . . . no.

.44 Bulk Translating: . . . yes, using CO-OP Monitor.

.45 Program Diagnostics: . . . . introduced in CO-OP Monitor. These are controlled in CODAP 1 Assembly Language.

.46 Translator Library

.461 Identity: . . . . CO-OP Monitor Library.
.462 User restriction: . . . general.

.463 Form
Storage medium: . . . magnetic tape.
Organization: . . . . as loaded.

.464 Contents
Routines: . . . . . . closed.
Functions: . . . . . yes.
Data Descriptions: . . . . no.
Subprograms: . . . . yes.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead

Name	Space
CO-OP Monitor:	2,000 words.
FORTRAN 63 Resident	40 words.

.512 Space required for each input-output file: . . 70 words (BCD)
500 words (Binary files).
300 words (mixed BCD and binary).

.513 Approximate expansion of procedure: . . ?

.52 Translation Time: . . . details not yet available.

.53 Optimizing Data

.531 Explicit: . . . . BUFFER IN, BUFFER OUT statements.

.532 Implicit:
DO loops should be used to give the advantage of I.R. modification.
No more than 5 DO loops should be nested.
Mixed mode expressions within a main loop should be examined for possible simplification.

.533 Automatic

- Common subexpressions are removed from any single expression and only evaluated once.
- Subscripting is done by reference to a special entry for each unique subscript, irrespective of how many times it appears in the program. When any variable used in any subscript is changed, each entry is conditionally updated.
- Three output buffers, one for each channel, are maintained in storage for use with card or printer equipment.

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.54 Object Program Performance

Type	Time	Space
Elementary algebra:	unaffected	unaffected.
Complex formulae	increased	increased.
Deep nesting		
Based on constants:	unaffected	unaffected.
Based on variables:	doubled	doubled.
Heavy branching:	increased	increased.
Complex subscripts		
With use of style rules:	unaffected	unaffected.
Written directly:	doubled (**)	doubled. (**).
Data editing:	unaffected	unaffected.
Overlapping operations		
With magnetic tapes:	BUFFER IN, OUT can be used to obtain unaffected performance	unaffected.
With card input	unaffected	unaffected.
With card or printer output:	one buffer per channel available.	unaffected.

(**) Analyst's estimate, provided as a guide only.

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . . CDC 1604 Computer.
1 tape.
1 input and 1 output medium.

.612 Larger configuration advantages: . . . . larger programs can be translated.

.62 Target Computer

.621 Minimum configuration: . . . . CDC 1604 Computer.

.622 Usable extra facilities: . . . . . magnetic tapes, (1607, 1608, or 606).
cards via CDC 1605, 1610, 1617 or1609.
CDC 1612.

.7 ERRORS, CHECKS AND ACTION: . . . . information not yet available.

.8 ALTERNATIVE TRANSLATORS

Computer	Identity	Date
CDC 1604	FORTRAN 60	1959.
CDC 1604	FORTRAN 62	1962.

OPERATING ENVIRONMENT: MACHINE CODE

§191.

.1 GENERAL

.11 Identity: . . . . CO-OP Index, July, 1962. (program numbers are quoted in the body of the text.)

.12 Description:

There are two operating systems available with the CDC 1604-A: the Three Phase Automonitor, and the CO-OP Monitor. Apart from these a number of un-integrated routines exist, which provide an operating environment for a user not wishing to use the other systems. The advantage of such an approach is the ability to use the repertoire of routines in the library, many of which are not compatible with the monitors without modifications.

.13 Availability: . . . . . via CO-OP Users Group.

.14 Originator: . . . . . issued by CO-OP.

.15 Maintainer: . . . . . CO-OP Users Group.

.16 First Use: . . . . . . 1960 onwards.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . . magnetic tape.

.212 Independent programs: . . . . magnetic tape. paper tape.

.22 Library subroutines: . only with specific systems (see Operating Environments, CO-OP Monitor and Three Phase Automonitor).

.23 Loading Sequence: . . . manual sequencing of card decks, paper tapes or magnetic tapes.

.3 HARDWARE ALLOCATION: as incorporated in user's program.

.4 RUNNING SUPERVISION: as incorporated in user's program.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . available for every, or each specifically quoted instruction, address, or jump. Output on magnetic tape or paper tape. CO-OP Program 134 or 103.

.512 Snapshots: . . . . . . see above (.511).

.52 Post Mortem: . . . . dumps onto magnetic tape or CDC 1612 printer in various formats, including "restorable," "listable," "card image," "binary," "octal," or "decimal." CO-OP Programs 049, 071, 066, 109, 136, 024, 025.

.6 OPERATOR CONTROL: . . . . as incorporated in user's program.

.7 LOGGING: . . . . . . as incorporated in user's program.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . any CDC 1604-A.

.812 Usable extra facilities: . . . . all.

.813 Reserved equipment: . . . . (a) CO-OP loader uses 659 location.
(b) traces use 666 locations plus "director."
(c) restorable dump uses 55 locations.
(d) other dumps use from 151 to 853 locations.

.82 System Overhead: . . none.

.83 Program Space Available: . . . . . variable, see .813 above.

.84 Program Loading Time: . . . . using CO-OP loader from magnetic tape approximately 60 + 0.0002 (I + 2D) seconds; where I is the number of instructions, D is the number of data items. (* *)

.85 Program Performance: . . . . negligible overhead.

OPERATING ENVIRONMENT: CO-OP MONITOR

§ 192.

.1 GENERAL

.11 Identity: . . . . CO-OP Monitor.

.12 Description

The CO-OP Monitor is a system for run-to-run control of programs on a 1604. Multi-running of programs is not possible. The monitor works with any configuration of I/O equipment and can operate at several levels. The highest level (level 1) is the Master Control System (MCS). The next level (level 2) is usually the CO-OP Control System (CCS). At level 3 there are the production programs, or program translators. Routines that are to be run in the system must be prepared with the special control linkage routines to communicate with the MCS, and must have control data available for CCS (instead of direct instructions) for such tasks as input-output, interruptions, and loading. The programs produced by CODAP-1 (see Section :172) conform to these requirements. The system operates under the control of special control cards, occasionally supplemented by the operator's use of the typewriter. Programs can be accepted from input devices, or can be requested from a library tape.

The MCS is a run-to-run supervisor which can transfer control to one "level 2" program after another. Usually the "level 2" programs are control routines that arrange smooth intra-run flow. They control abnormal run terminations and provide a flexible means of conditional load-and-go or translate-and-run procedures. In addition, they provide an automatic procedure for pre-loading tapes and internal storage.

The MCS provides a systematic allocation of input-output units and also of storage by an allocator/loader which sets linkages between independently prepared routines.

The MCS provides an automatic termination of runs that exceed their time limit or output volume limit by a fixed tolerance. At each termination, the CCS provides alternative degrees of post-mortem dumps and an optional preset entrance to a short, limited termination routine provided by the user.

The MCS controls all interrupts, but parameters specifying the type of interrupts and the routines required after an interrupt must still be incorporated in each program. The MCS provides for the housekeeping of requesting interrupts and of determining which interrupt has occurred.

.12 Description (Contd.)

The MCS contains a set of routines to control input-output transfers. They include tests for logical consistency of control linkage requests (e.g., that rewind operations apply only to magnetic tape units and not to other I/O devices) and translation between data codes (e.g., data prepared in column-binary for a device requiring row-binary) but no radix conversion. The programmer must provide for hardware error control. A large variety of routines are included to cover the various input-output formats. Simultaneous operations are still program dependent.

In addition to the dumps at termination of a program, CCS provides snapshots specified by control cards that are inserted at load time. The CCS can also provide an index of allocated storage locations so that absolute dumps can be interpreted by the programmer.

The system requires: a standard input device for control cards, and sometimes data and programs; a standard output device to record dumps and snapshots; a typewriter for short coded messages to the operator; and an accounting output device for longer messages to the operator and entries to a log. The accounting device is usually the paper tape punch. There is also a library tape which contains operational routines and subroutines, including CODAP-1, FORTRAN-62, and later COBOL and CXA (Control Data Extended Algol).

The overall operating efficiency of the CO-OP Monitor System is difficult to assess.

Running intra-run overheads are strongly dependent on the style of the level 3 program. The overheads are probably low relative to hand coding except for the input-output transfer and code translation control routines. The intra-run overheads are also likely to be low compared to manual operation, unless considerable tape searching is necessary.

.13 Availability: . . . . . . in CDC 1604 version.

.14 Originator: . . . . Control Data Corp. assisted by a CO-OP subcommittee.

.15 Maintainer: . . . . . . Control Data Corporation.

.16 First Use: . . . . July, 1962.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . loaded from magnetic tape files as called for in table used by relocatable loader.

§ 192.

.212 Independent programs: from magnetic tapes in card format.
from paper tape in card format.
from cards in card format.
from magnetic tape in binary relocatable format.

.213 Data: . . . . via any input device, under the control of I/O routines incorporated in the MCS, whenever called from individual program.

.214 Master routines: . . . . the Master Control Routine is called in from magnetic tape by a button on the Console. Further subsidiary master routines are called in by the Job Sequencer using the MCS control record.

.22 Library Subroutines: . loaded from on-line magnetic tape library.

.23 Loading Sequence: . . . normally each job is processed as loaded. The operator can also initiate by instructions to:
(a) Abandon present job and start on next job.
(b) Re-start this job.
(c) Start job XXX.
During processing, operator can instruct termination of CO-OP Monitor run either (1) at end of present job, (2) at end of present job, or (3) at end of job XXX.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . not necessary.

.312 Occupation of working storage: . . . determined by relocatable binary loader on basis of RANGE (first and last words) statement for each subprogram; and requirement of MCS.

.32 Input-Output Units

.321 Initial assignment: . . . assigned for each job based on Available Equipment Table.

.322 Alteration: . . . . not available.

.323 Reassignment: . . . . . by operator typed into Available Equipment Table.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: . controlled by standard routines incorporated in MCS.

.42 Multi-programming: . . not presently available.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Loading input error:	program check	record fact on log and on "communication to operator medium."
Allocation impossible:	program check	proceed to next job.
In-out error - single:	program check	not specified.
In-out error - persistent:	program check	not specified.
Storage overflow:	not possible.	
Invalid instructions:	not possible.	
Program conflicts:	some I/O checks.	depends on routine.
Arithmetic overflow:	hardware/program check.	determined by interrupt routine being used.
Underflow:	hardware program check.	
Invalid operation:	no check.	
Improper format:	program check.	
Invalid address:	no check.	
Reference to forbidden area:	no check.	

.45 Restarts

.451 Establishing restart points: . . . . no special provision, can use:
(a) automatic, set, and dump on abnormal exit from program.
(b) own coding initiating dump at programmer selected interval.

.452 Restarting process: . . (a) use of dump as new program.
(b) manual intervention by operator to recover control in case of total system failure.

§ 192.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . none.
.512 Snapshots: . . . . up to 10 snapshots in any one program.

.52 Post Mortem: . . . . . dumps taken automatically in case of abnormal exit from routine. Dump formats range from record of console conditions to full dumps in various formats.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . output via typewriter and/or loud speaker.
.612 Action required by operator: . . . . listed in Operator's Manual, if standard.
as required by programmer, if own coding message.
.613 Reporting progress of run: . . . . end of job and time, placed on "comment to operator" medium and "accounting medium."

.62 Operator's Decisions: . via keyboard, in accordance with action described in Operator's Manual or by previous type out.

.63 Operator's Signals

.631 Inquiry: . . . . carriage return on typewriter with standard message following. This can only produce the Available Equipment Table.
.632 Change of normal progress: . . . . amendment of Available Equipment Table, or instructions to ignore some or all jobs still awaiting processing.

.7 LOGGING

.71 Operator Signals: . . . listed on typewriter and "comment from operator" medium.

.72 Operator Decisions: . . listed on typewriter and "comment from operator" medium.

.73 Run Progress: . . . . . listed on typewriter and "accounting medium."

.74 Errors: . . . . listed on typewriter and "comment to operator medium."

.75 Running Times: . . . . listed on typewriter and "accounting medium."

.76 Multi-running Status: . not applicable.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: 4 tape CDC 1604 system.
.812 Usable extra facilities: all except reserved Jump Keys.
.813 Reserved equipment: ? words.
all Jump Keys.
option to mask out arithmetic errors not available.

.82 System Overhead: . . . ?

.83 Program Space Available: . . . . . . ?

.84 Program Loading Time: ?

.85 Program Performance: ?

OPERATING ENVIRONMENT: THREE PHASE AUTOMONITOR

§ 193.

.1 GENERAL

.11 Identity: . . . . Three Phase AUTOMONITOR System.

.12 Description

.121 General

AUTOMONITOR differs from the CO-OP Monitor by its inability to provide for mixed, production and assembly runs, or for a choice of subsidiary control systems.

There is no compatibility between the outputs produced by AUTOMONITOR and those required by the CO-OP Monitor.

The following commentary is a rewrite of the official description.

The Three Phase AUTOMONITOR is a programming system for the 1604 computer. It provides for the batched assembly and the execution of programs prepared in symbolic assembly language. A simple, but flexible, system of buffered input-output is incorporated.

The execution of batched jobs is handled in three phases: Phase one in which the stacked input for all jobs is translated into a binary input tape; phase two in which each job is executed sequentially using the binary input tape and producing a binary output tape; and phase three in which the binary output tape is translated into a BCD listable tape.

Batched assemblies may also be handled by the system. The assembly routine used is the CODAP assembly program. The system handles assembly and execution runs separately and does not permit intermixing.

The system is maintained on a library tape that contains the system's six main routines and all associated subroutines. The first file on this tape is reserved for the six routines which are described briefly as follows (paragraphs .122 to .127):

.122 SUPERVISOR

The SUPERVISOR, first routine on the AUTOMONITOR library tape, distinguishes between assembly or execution runs and brings the correct processing routine into memory. SUPERVISOR also will respond to certain key settings and call in the Library Edit routine to prepare a new library tape, or it can initiate an execution restart procedure.

.123 LIBRARY EDIT ROUTINE

The LIBRARY EDIT ROUTINE is used to prepare, copy, or update the library tape used in the AUTOMONITOR system.

.124 SYMBOLIC ASSEMBLY ROUTINE

The SYMBOLIC ASSEMBLY ROUTINE (CODAP) converts the programmer's symbolic notation into machine language and binary coded decimal (BCD), and prepares two magnetic tapes. The machine language tape can be used to produce either binary or octal cards and the BCD tape is used to provide off-line symbolic assembly listings. The performance times are similar to those listed under CODAP-1.

.125 INPUT TRANSLATOR

The INPUT TRANSLATOR (INTRAN), phase one, receives an input card image on a tape. This tape is prepared off-line and contains all the jobs to be run in one batch. INTRAN reads this tape, performs all needed conversions, and writes a binary tape (referred to as binary input tape) of uniform record length. This binary input tape contains the information together with flags denoting the type and amount of information. All jobs in the batch are processed by INTRAN before control is turned over to the next phase. INTRAN is only loaded once per batch processing.

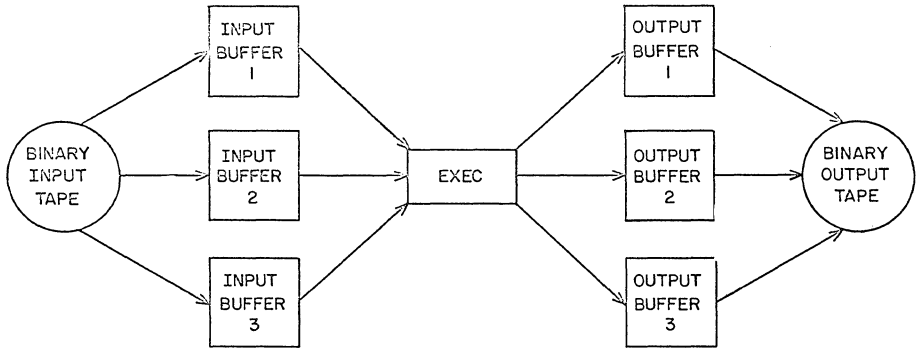
.126 EXECUTION COORDINATOR

The EXECUTION COORDINATOR (EXEC), phase two, receives control from INTRAN and uses as input the binary input tape prepared by INTRAN. EXEC loads a program into memory and turns control over to it. If input of data is required during execution, the programmer uses a calling sequence to obtain data from the binary input tape through EXEC. It is also possible, by use of the input calling sequence, to overlay a program in core. In this case, the programmer would furnish a transfer address. Three types of output are available to the programmer during the execution phase: core dumps, general purpose output, and custom output (output according to FORTRAN-type format statements).

All input and output during the execution phase is on an interrupt basis. EXEC sets up parts of the store as input and output buffers (three of each). Each internal input buffer is filled from the binary input tape as soon as all the information previously contained in that buffer has been processed by EXEC. When the programmer calls for output, EXEC writes the output in pure binary into one of the internal buffers, adding flags which describe the amount of output and the type of conversion and format. When a buffer has been filled, EXEC writes the information contained therein as one record on a binary tape (here called binary output tape).

§ 193.

.126 EXECUTION COORDINATOR (Contd.)



Since the program being executed has control of the computer during execution, it is not inconceivable that a part or all of EXEC may be destroyed. If this occurs, an execution restart procedure is available.

.127 OUTPUT TRANSLATOR

The OUTPUT TRANSLATOR (OUTRAN) phase three, receives control after the last program of a batch has been executed. OUTRAN reads the binary output tape prepared by EXEC and performs the necessary conversions. The type of conversion is terminated by the flags which are furnished with the data. A BCD listable tape is prepared for off-line listing with identifying information accompanying each job.

.128 Equipment

Certain programming conventions such as reserving the stop instructions and interrupts must be followed when using the AUTOMONITOR. Most external function instructions, particularly those involving tapes, are reserved for the use of the AUTOMONITOR. The AUTOMONITOR uses all the tapes on one 1607 and also monopolizes the 1607 input and output channels.

.128 Equipment (Contd.)

However, if more than one 1607 is available, it may be used by the programmer through a special set of calling sequences.

The minimum equipment configuration necessary for the AUTOMONITOR is as follows:

On-line - Control Data Corporation 1604 Computer and 4 1607 or 606 Tape Units. (More may be used.)

Off-line - Card reader, card punch, and line printer. Card-to-tape, tape-to-printer, and tape-to-punch capability.

.13 Availability: . . . . . . presently available in 1604 version.

.14 Originator: . . . . Control Data Corporation.

.15 Maintainer: . . . . . . Control Data Corporation.

.16 First Use: . . . . April, 1961.

SYSTEM PERFORMANCE

§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes
- Master file: . . . . . 108 characters.
- Detail file: . . . . . . 1 card.
- Report file: . . . . . . 1 line.

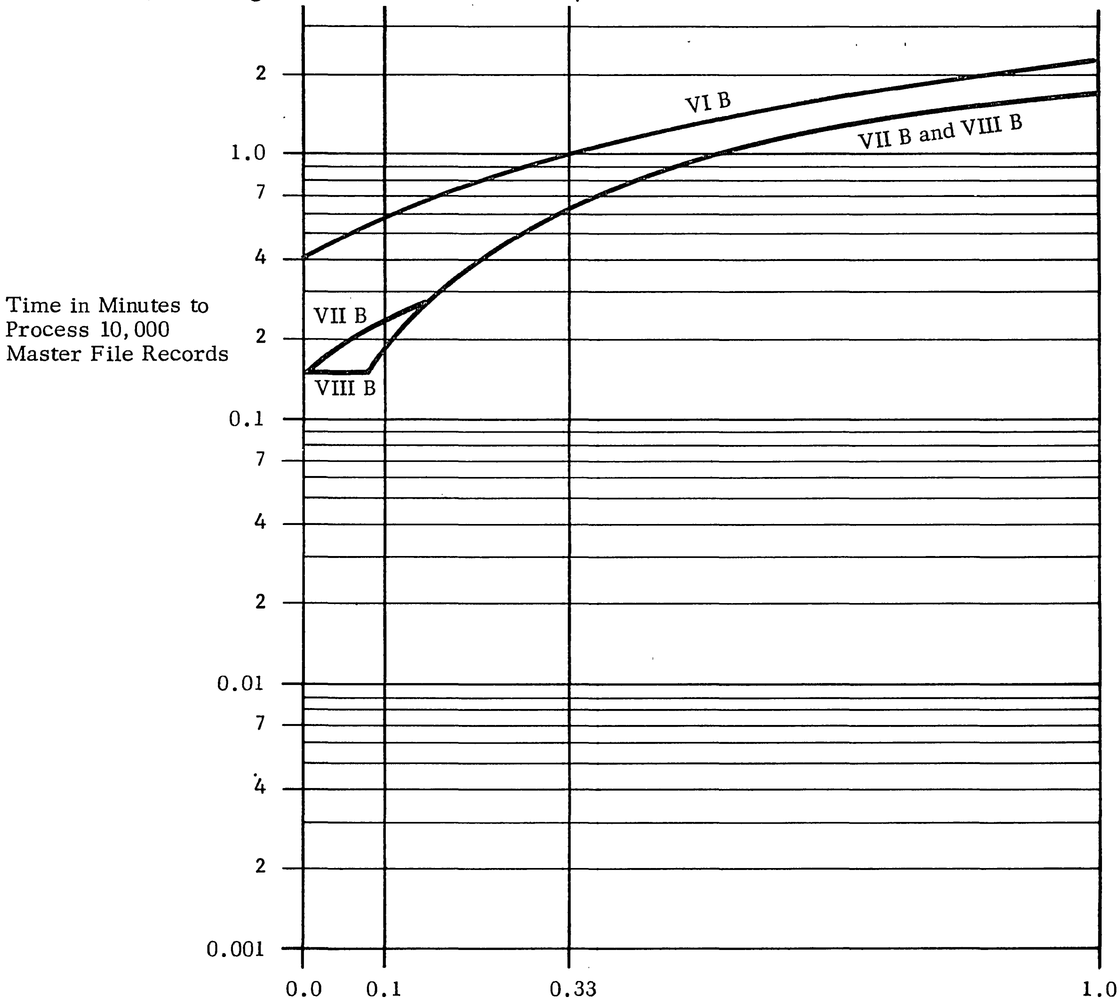
.112 Computation: . . . . . . standard.

.113 Timing basis: . . . . . using estimating procedure outlined in Users Guide, 4:200.113

A straightforward approach was made to the problem with input and output areas being kept separate. This facilitates handling insertions and deletions to the files and means that all records have to be physically moved from one area to another in storage. In other problems with different requirements and a low activity, such moving might be costly. It would then be possible to use dynamic control of the buffer control words, together with cycle storage allocation, in order to avoid such moving.

.114 Graph: . . . . see graph below.

.115 Storage space required
- Configuration VI.B: . 8,000 words.
- Configuration VII.B: . 8,000 words.
- Configuration VIII.B: . 8,000 words.



Activity Factor
Average Number of Detail Records Per Master Record
Roman Numerals denote Standard Configurations

§ 201.

.12 Standard File Problem B

.121 Record sizes

Master file: . . . . . 54 characters.
Detail file: . . . . . . 1 card.
Report file: . . . . . . 1 line.

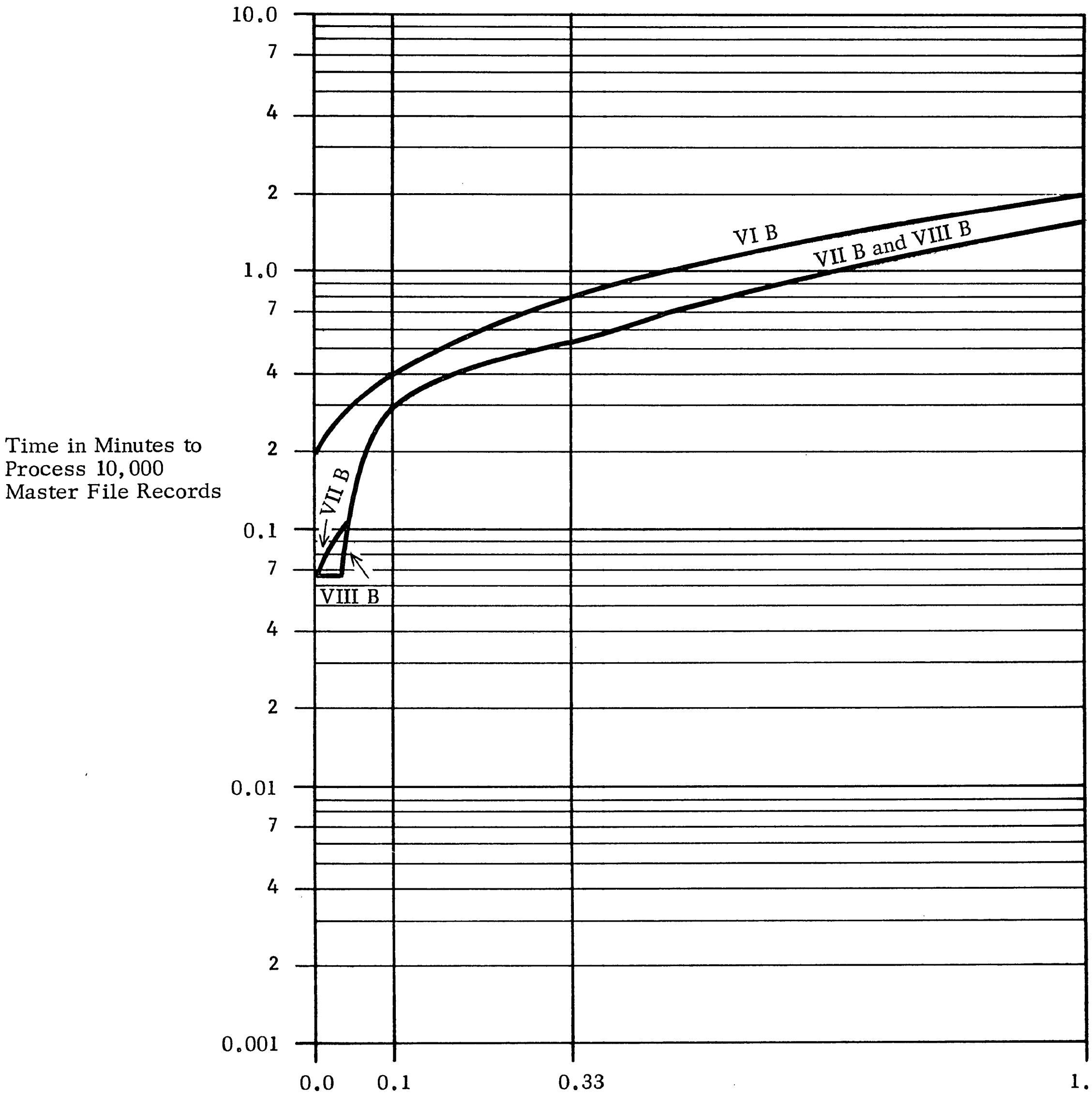
.122 Computation: . . . . . . standard.

.123 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.

.123 Timing basis (cont'd)

A straightforward approach was made to the problem with input and output areas being kept separate. This facilitates handling insertions and deletions to the files and means that all records have to be physically moved from one area to another in storage. In other problems with different requirements and a low activity, such moving might be costly. It would then be possible to use dynamic control of the buffer control words, together with cycle storage allocation, in order to avoid such moving.

.124 Graph: . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

Roman Numerals denote Standard Configurations

§ 201.

.13 Standard File Problem C

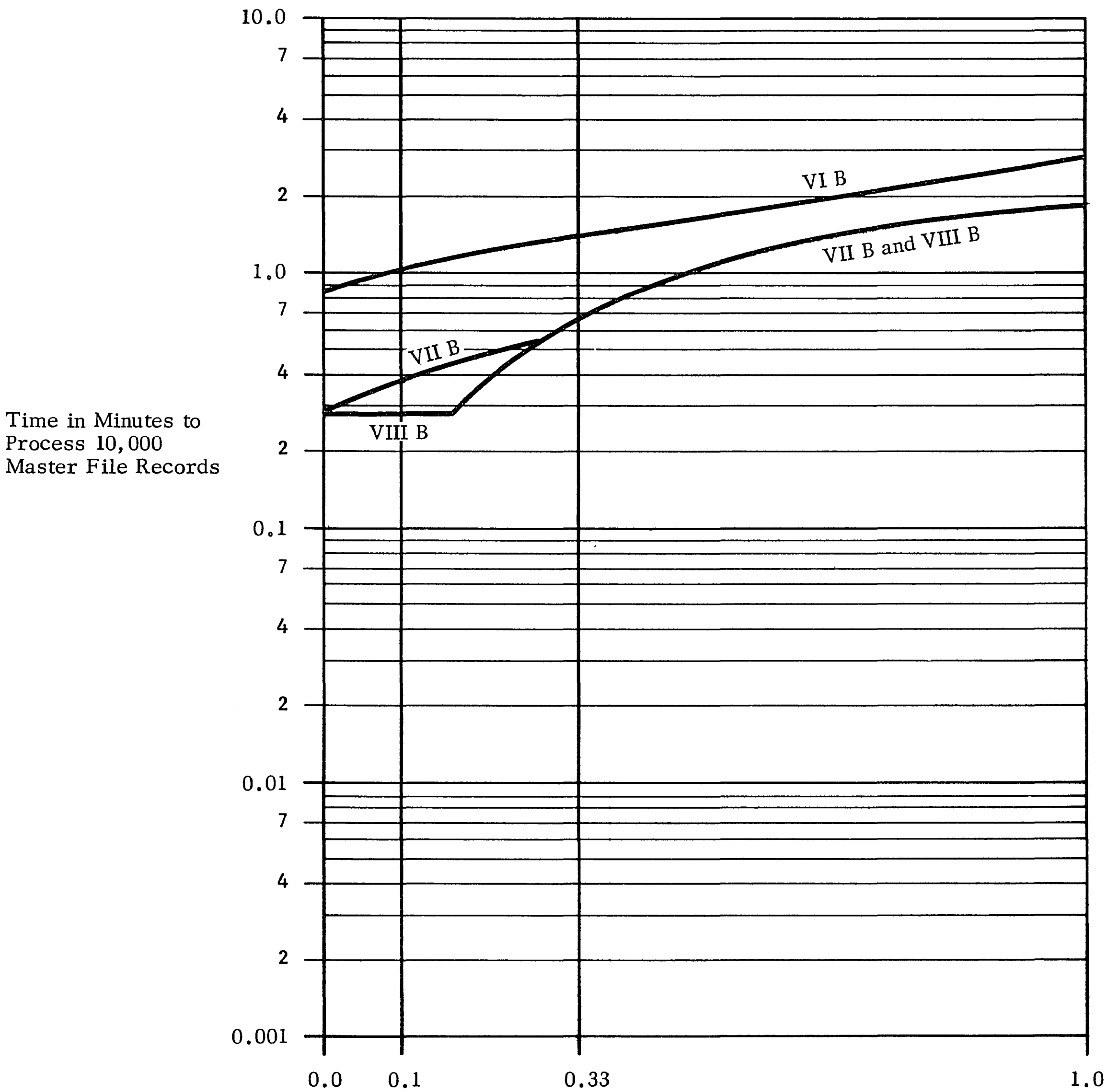
.131 Record sizes
Master file: . . . . . 216 characters.
Detail file: . . . . . . 1 card.
Report file: . . . . . . 1 line.
.132 Computation: . . . . . . standard.
.133 Timing basis: . . . . . using estimated procedure outlined in Users' Guide, 4:200.13.

A straightforward approach was made to the problem with input and output areas being kept separate.

.133 Timing basis (cont'd)

This facilitates handling insertions and deletions to the files and means that all records have to be physically moved from one area to another in storage. In other problems with different requirements and a low activity, such moving might be costly. It would then be possible to use dynamic control of the buffer control words, together with cycle storage allocation, in order to avoid such moving.

.134 Graph: . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

Roman Numerals denote Standard Configurations

§ 201.

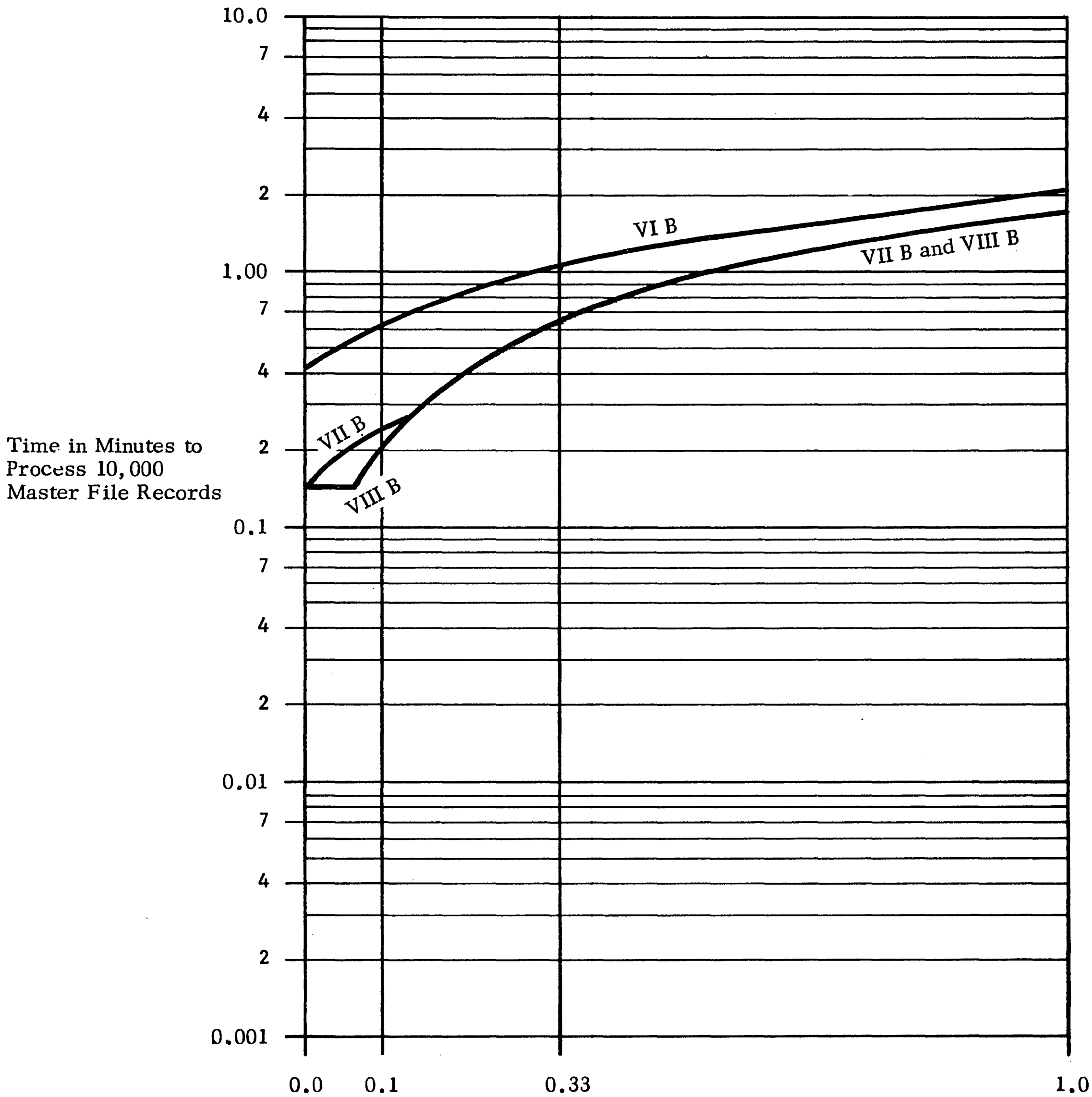
.14 Standard File Problem D

141 Record sizes
- Master file: . . . . . 108 characters.
- Detail file: . . . . . . 1 card.
- Report file: . . . . . . 1 line.

.142 Computation: . . . . . . trebled.

.143 Timing basis: . . . . . using estimated procedure outlined in Users' Guide, 4:200.13.

.144 Graph: . . . . see graph below.



Activity Factor
Average Number of Detail Records Per Master Record

Roman Numerals denote Standard Configurations

§ 201.

.2 SORTING

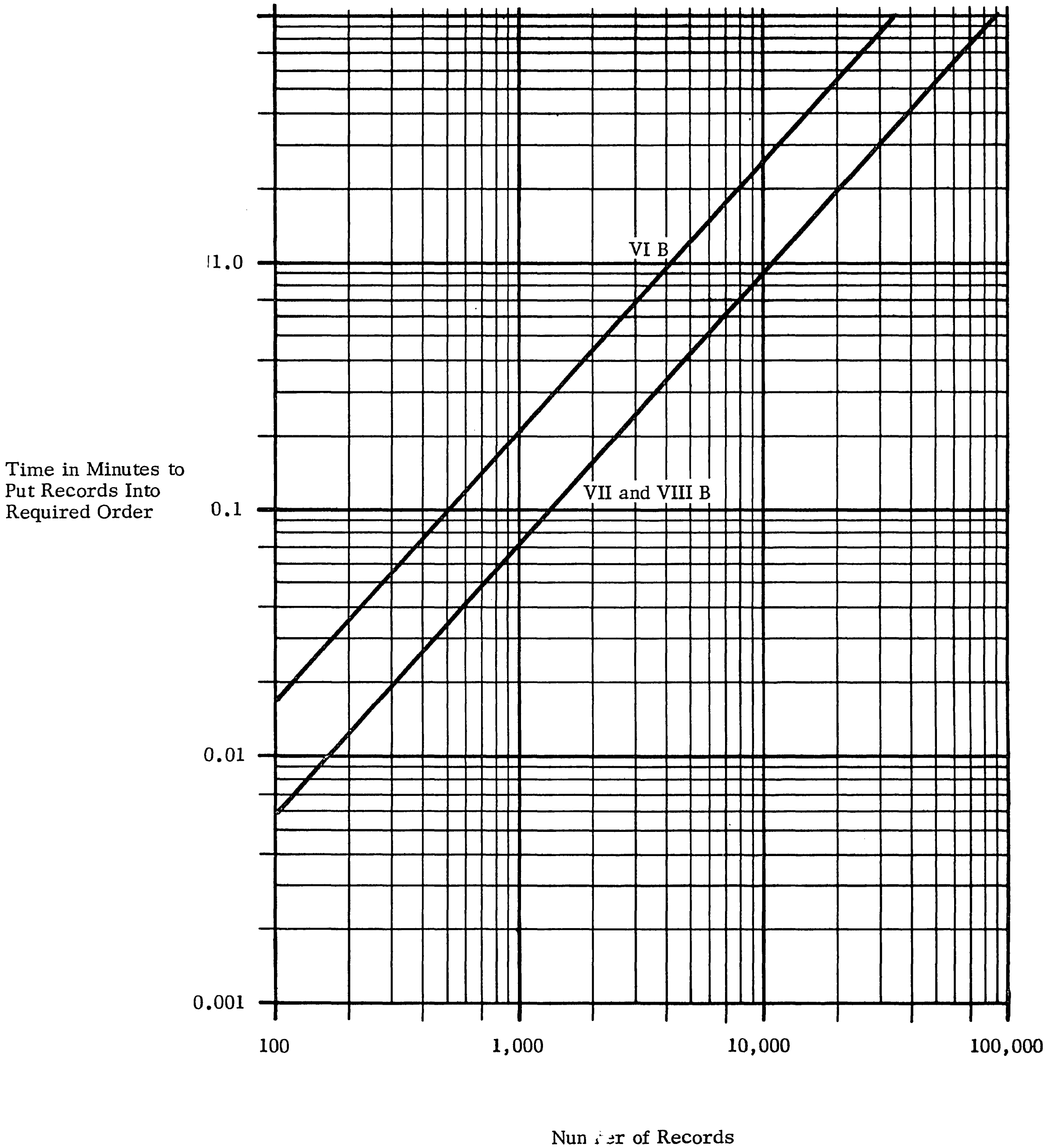
.21 Standard Problem Estimates

.211 Record size: . . . . . . 80 characters.

.212 Key size: . . . . 8 characters.

.213 Timing basis: . . . . . using estimated procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . see graph below.



Roman Numerals denote Standard Configurations

§ 201.

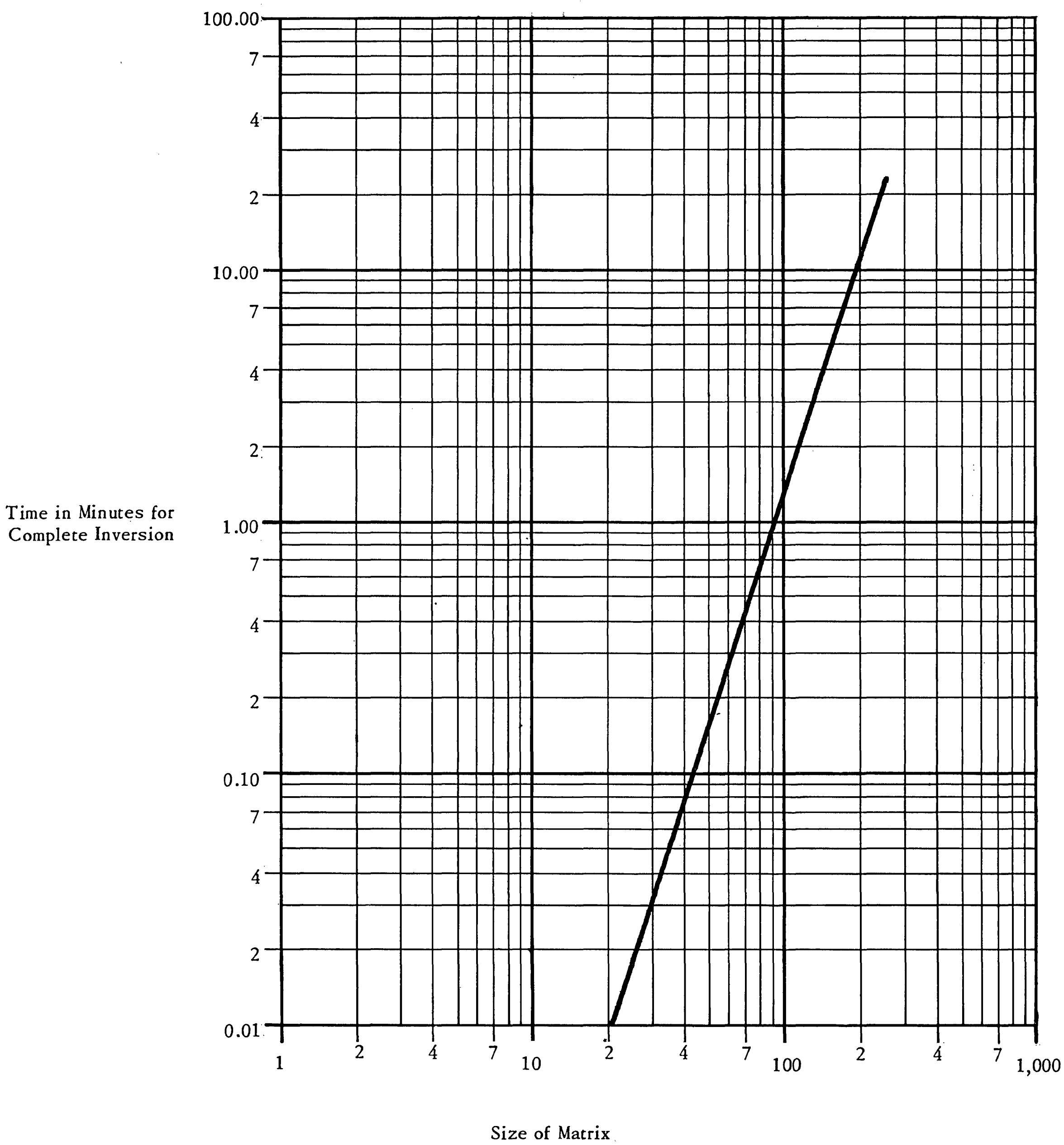
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic Parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . see graph below.



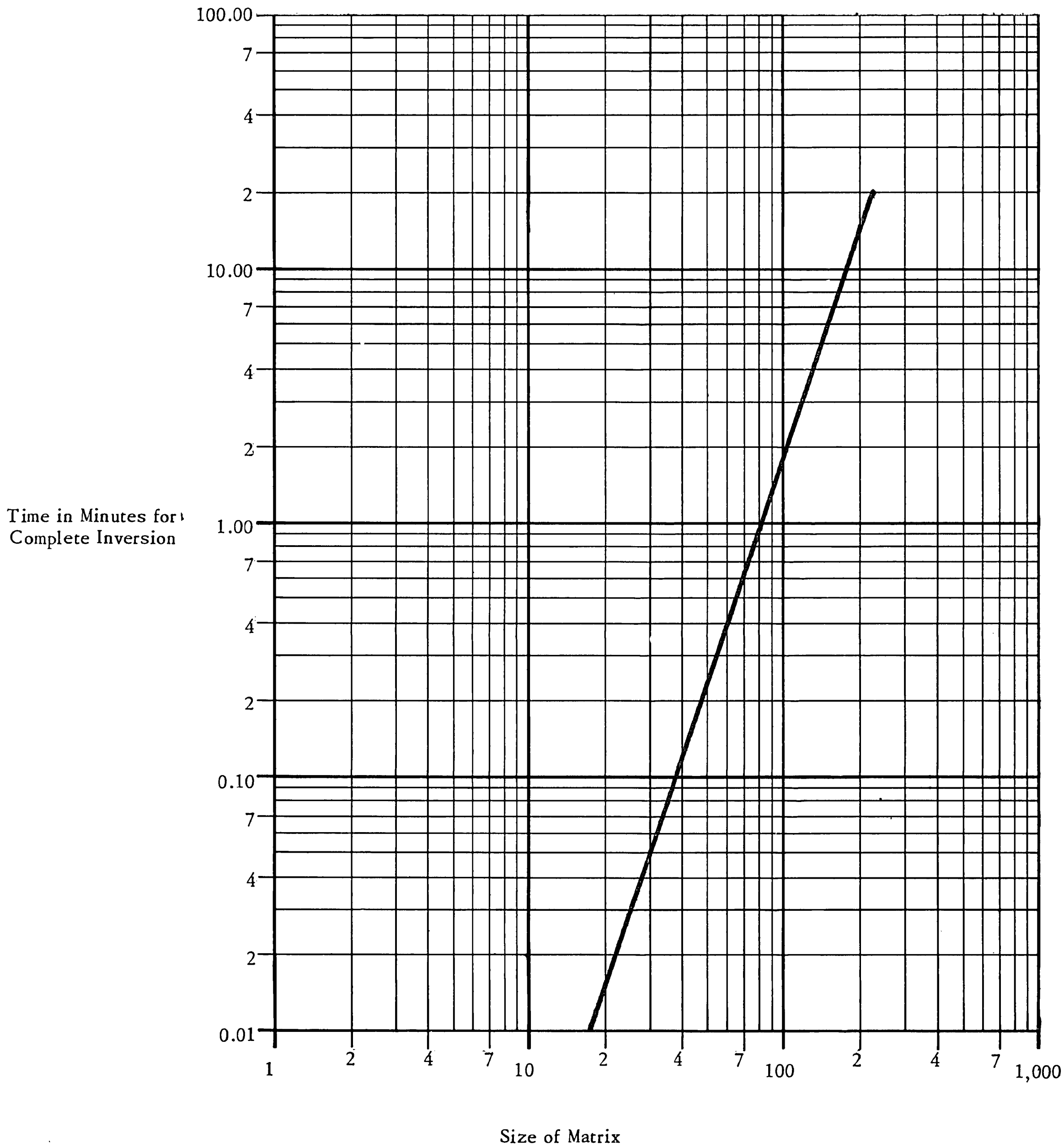
§ 201.

.32 F1 LMSD MATIN Times

.321 Basic Parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.322 Timing Basis: . . . . CO-OP Library. Times shown are times for one iteration.

.323 Graph: . . . . see graph below.



§ 201.

.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

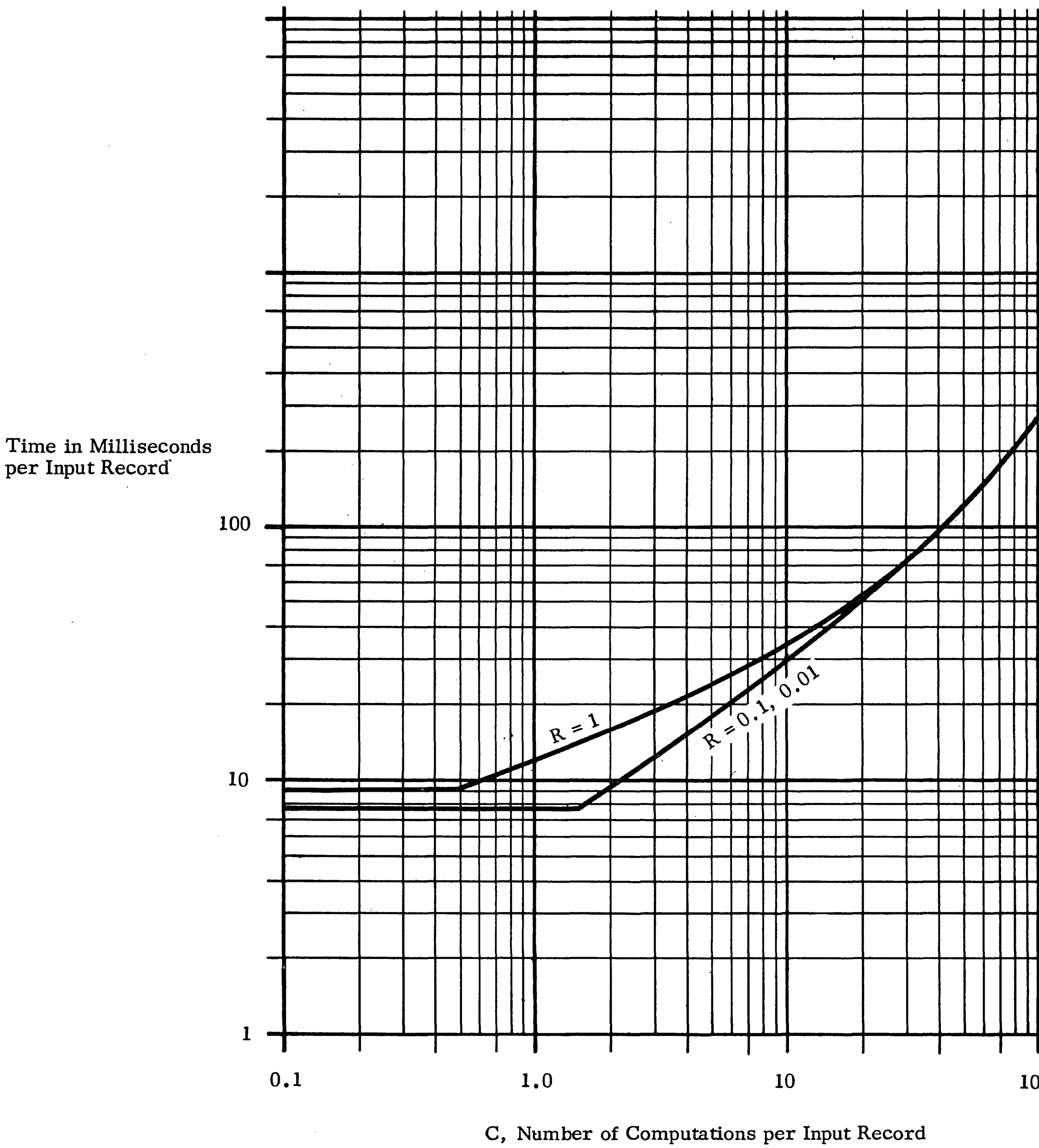
.412 Computation: . . . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.413 Timing basis: . . . . . using estimating procedure outlined in Users' Guide 4:200.413.

.414 Graph: . . . . Configuration VI B; paper tape input, typewriter output, floating point machine coding.

Configuration VI B; Single Length (11 digit precision); Floating point.

R = Number of Output Records per Input Record

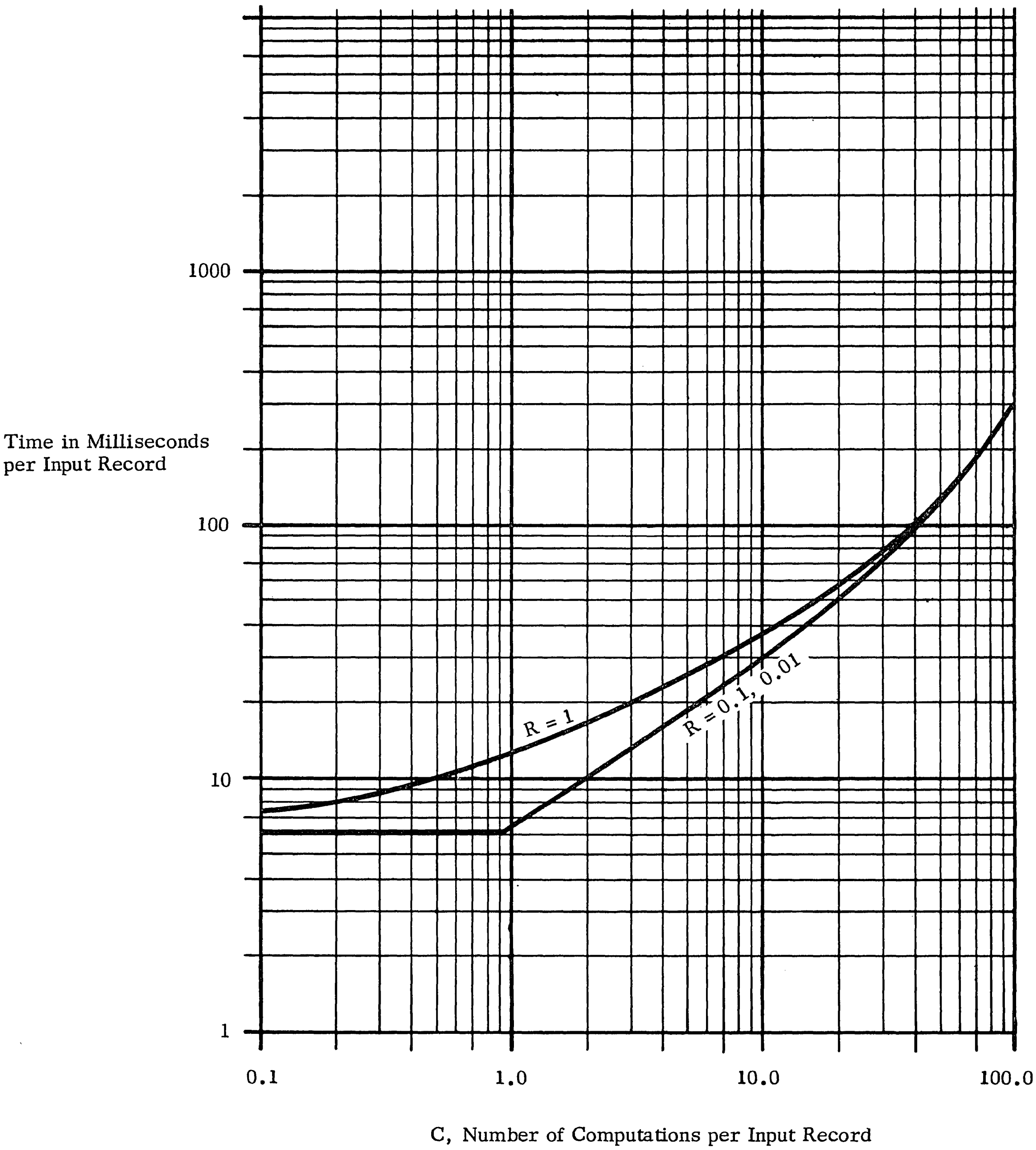


§ 201.

.415 Graph: . . . . Configuration VII B; paper tape input, typewriter output, floating point machine coding.

Configuration VII B; Single Length (11 digit precision); Floating point.

R = Number of Output Records per Input Record

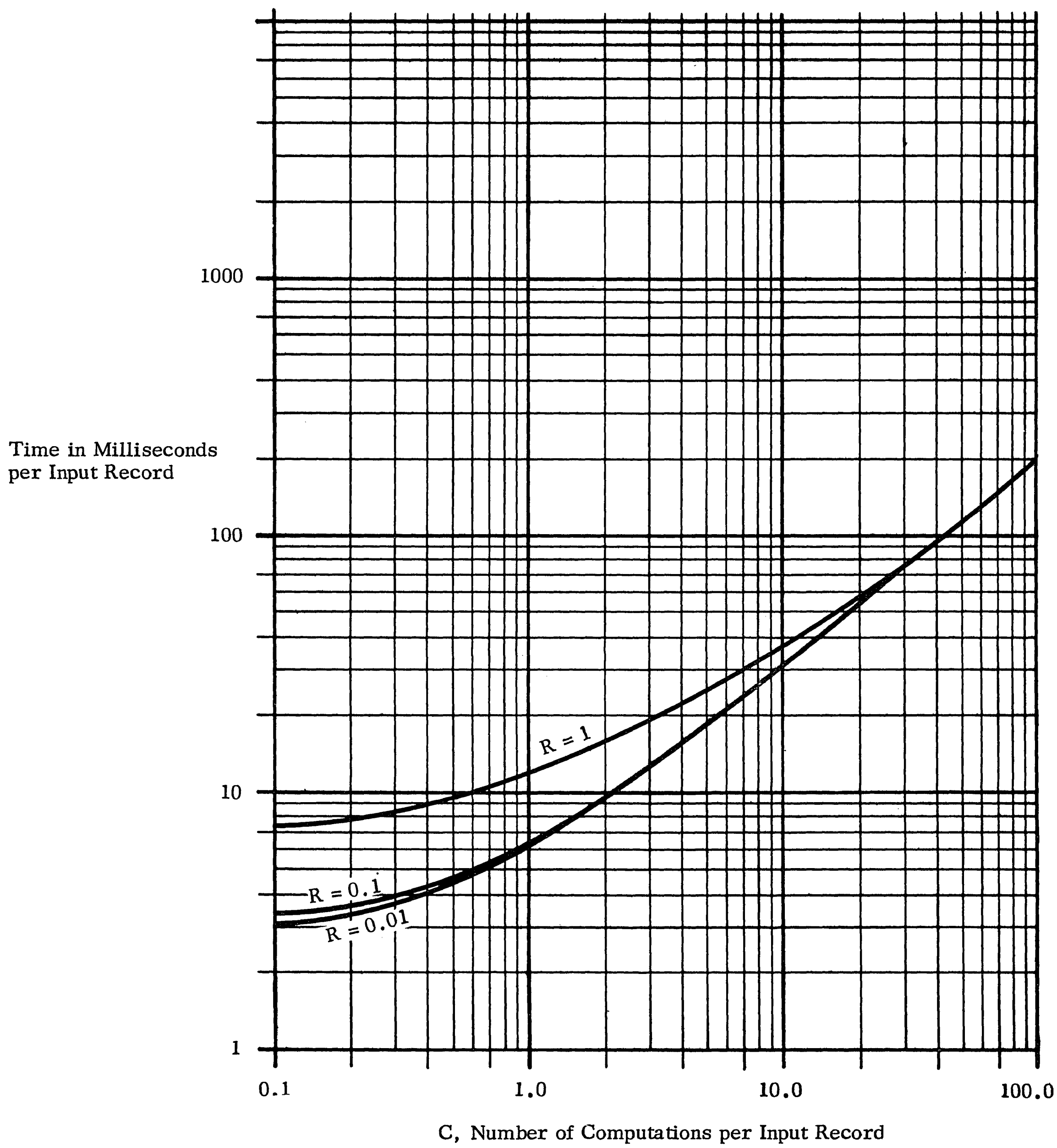


§ 201.

.416 Graph: . . . . Configuration VIII B; paper tape input, typewriter output, floating point machine coding.

Configuration VIII B; Single Length (11 digit precision); Floating point.

R = Number of Output Records per Input Record



§ 201.

.5 GENERALIZED STATISTICAL PROCESSING

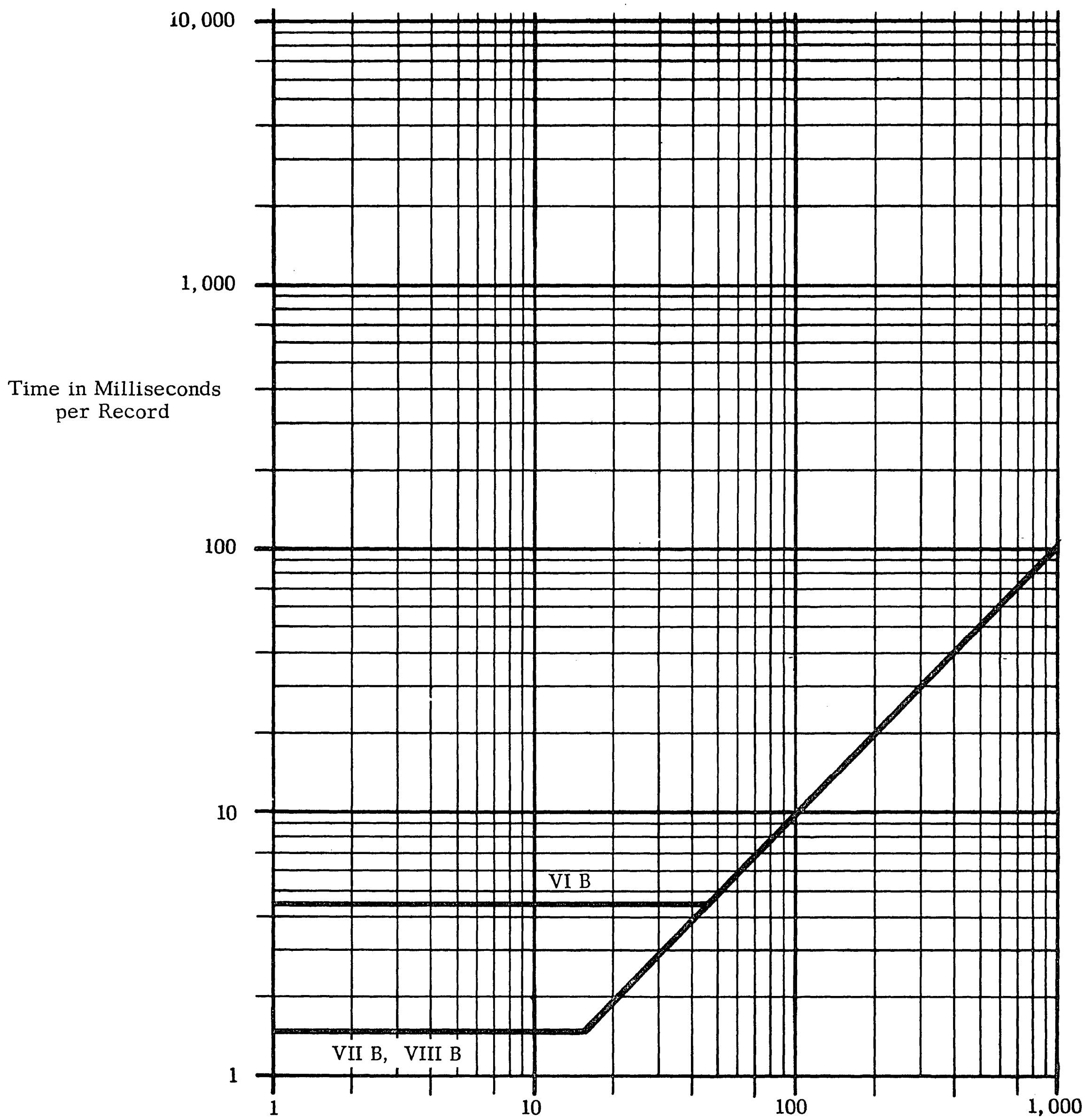
.51 Standard Statistical Problem A Estimates

.511 Record size: . . . . . . thirty 2-digit integral numbers.

.512 Computation: . . . . . . augment T elements in cross-tabulation tables.

.513 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.513.

.514 Graph: . . . . see below.



T, no of Augmented Elements

Roman Numerals denote Standard Configurations

CDC 1604-A
PHYSICAL CHARACTERISTICS

CDC 1604-A PHYSICAL CHARACTERISTICS

<table>
<tr><td rowspan="2">IDENTITY</td><td colspan="2">Unit Name</td><td colspan="2">Central Computer and Console</td><td colspan="2">Adapter</td><td colspan="2">Magnetic Tape Control Unit</td><td colspan="2">Control Unit</td><td colspan="2">Card Unit</td><td colspan="2">Control Unit</td><td>Printer</td></tr>
<tr><td colspan="2">Model Number</td><td colspan="2">CDC 1604</td><td colspan="2">CDC 1605</td><td colspan="2">CDC 1607</td><td colspan="2">CDC 1608</td><td colspan="2">CDC 1609</td><td colspan="2">CDC 1610</td><td>CDC 1612</td></tr>
<tr><td rowspan="3">PHYSICAL</td><td colspan="2">Height × Width × Depth, in.</td><td colspan="2">68 × 28 × 89</td><td colspan="2">43 × 20 × 48</td><td colspan="2">68 × 28 × 68</td><td colspan="2">43 × 20 × 48</td><td colspan="2">51 × 40 × 26</td><td colspan="2">43 × 20 × 48</td><td>56 × 72 × 31</td></tr>
<tr><td colspan="2">Weight, lbs.</td><td colspan="2">3,450</td><td colspan="2">575</td><td colspan="2">2,500</td><td colspan="2">650</td><td colspan="2">755</td><td colspan="2">600</td><td>890</td></tr>
<tr><td colspan="2">Maximum Cable Lengths</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td>---</td></tr>
<tr><td rowspan="7">ATMOSPHERE</td><td rowspan="2">Storage Ranges</td><td>Temperature, °F.</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td>---</td></tr>
<tr><td>Humidity, %</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td>---</td></tr>
<tr><td rowspan="2">Working Ranges</td><td>Temperature, °F.</td><td colspan="13">Computer room temperature should not exceed 70°F.</td></tr>
<tr><td>Humidity, %</td><td colspan="13">Computer room humidity should be 40 to 50%.</td></tr>
<tr><td colspan="2">Heat Dissipated, BTU/hr.</td><td colspan="2">26,400</td><td colspan="2">4,000</td><td colspan="2">30,000</td><td colspan="2">4,000</td><td colspan="2">5,680</td><td colspan="2">4,000</td><td>6,400</td></tr>
<tr><td colspan="2">Air Flow, cfm.</td><td colspan="2">3,000</td><td colspan="2">800</td><td colspan="2">3,000</td><td colspan="2">800</td><td colspan="2">800</td><td colspan="2">800</td><td>---</td></tr>
<tr><td colspan="2">Internal Filters</td><td colspan="2">Yes</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td colspan="2">---</td><td>---</td></tr>
<tr><td rowspan="6">ELECTRICAL</td><td rowspan="2">Voltage</td><td>Nominal</td><td>208</td><td>208</td><td>208</td><td>208</td><td>208</td><td>208</td><td>208</td><td>208</td><td>208</td><td>208</td><td>208</td><td>115</td><td>117</td></tr>
<tr><td>Tolerance</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>---</td></tr>
<tr><td rowspan="2">Cycles</td><td>Nominal</td><td>400</td><td>60</td><td>400</td><td>60</td><td>400</td><td>60</td><td>400</td><td>60</td><td>400</td><td>60</td><td>400</td><td>60</td><td>60</td></tr>
<tr><td>Tolerance</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>--</td><td>---</td></tr>
<tr><td colspan="2">Phases</td><td>3</td><td>3</td><td>3</td><td>3</td><td>3</td><td>3</td><td>3</td><td>3</td><td>3</td><td>3</td><td>3</td><td>1</td><td>1</td></tr>
<tr><td colspan="2">Load KVA</td><td>8.0</td><td>1.2</td><td>2.0</td><td>0.9</td><td>2.0</td><td>2.4</td><td>2.0</td><td>0.9</td><td>2.0</td><td>0.9</td><td>2.0</td><td>0.9</td><td>1.9</td></tr>
<tr><td>NOTES</td><td colspan="2">Where two types of power are shown for a unit, both are required.</td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td><td colspan="2"></td><td></td></tr>
</table>

CDC 1604-A PHYSICAL CHARACTERISTICS—Contd.

IDENTITY	Unit Name		Card Reader	Magnetic Tape Unit					
	Model Number		CDC 1617	CDC 606					
PHYSICAL	Height × Width × Depth, in.		41 × 30 × 19	72 × 28 × 33					
	Weight, lbs.		210	800					
	Maximum Cable Lengths		---	---					
ATMOS-PHERE	Storage Ranges	Temperature, °F.	---	---					
		Humidity, %	---	---					
	Working Ranges	Temperature, °F.	---	---					
		Humidity, %	---	---					
	Heat Dissipated, BTU/hr.		708	---					
	Air Flow, cfm.		100	---					
	Internal Filters		---	---					
ELEC-TRICAL	Voltage	Nominal	115	115					
		Tolerance %	5	5					
	Cycles	Nominal	60	60					
		Tolerance %	---	---					
	Phases and Lines		---	---					
	Load KVA		0.21	3.0					
NOTES									

PRICE DATA

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
Central Processor	1604-A	Basic Computer with:			
		8,192 words of core storage	24,000	Maintenance contracts are individually negotiated	790,000
		16,384 words of core storage	26,500		870,000
		32,768 words of core storage	31,600		1,030,000
		Price includes following features:			
		Fixed and floating point arithmetic			
		Indirect addressing			
		Console			
		Motor-generator			
		Paper tape reader and punch			
		Typewriter			
Storage		Included in Basic Computer			
Input-Output	1609	Card Reader and Punch	1,175		47,000
	1617	Card Reader	580		22,500
	1612	Line Printer	1,840		73,700
	606	Magnetic Tape Unit	825		36,000
	1615	Magnetic Tape Control Unit	1,980		66,000

CDC 160-A

Control Data Corporation

STANDARD EDP REPORTS

AUERBACH INFO, INC.

PRINTED IN U. S. A.

CDC 160-A

Control Data Corporation

STANDARD EDP REPORTS

AUERBACH INFO, INC.

PRINTED IN U. S. A.

CONTENTS

INA = Information not available

CONTENTS (Contd.)

INTRODUCTION

§ 011.

The CDC 160-A system, essentially a CDC 160 with larger core storage and a single buffered input-output channel, is a solid-state desk-size computer oriented toward scientific applications which can also be used for off-line data transcription and as a satellite to larger systems. The basic system consists of the processor and Normal input-output channel, 8,192 words of core storage with Buffer channel, and a fast paper tape reader and punch. Data transcriptions are effected by standard card-to-tape and tape-to-printer conversion subroutines, by SIMO (simultaneous card-to-tape and tape-to-printer), and by PPPP (a peripheral processing package which can perform four tape-to-printer operations and a card-to-tape operation simultaneously). The basic system rents for $2,250 per month.

Core storage is supplied in from one to four modules, with each module containing two banks of 4,096 words. Cycle time for the core storage is 6.4 microseconds, and addition of a word in storage to the accumulator requires 19.2 microseconds. Because the 12-bit address word can address only 4,096 locations, the 160-A requires a bank-control register to permit addressing of the entire core storage.

Core storage can be expanded by addition of a Model 169 Auxiliary Memory Unit, which has a maximum capacity of 24,576 words. The Model 169 provides an additional buffered channel, usable only with the core store of the Model 169. Use of this channel permits an additional independent input or output transfer of data. An interrupt system is also provided with the processor; however, use of this feature in an integrated system is not emphasized in the manufacturer's literature.

The processor performs single-address instructions sequentially on 12-bit words (11 bits plus sign bit) giving a significance of 3.3 decimal digits. Alphameric input and output is stored internally as one or two 6-bit BCD characters per computer word, and radix conversion on four- and six-bit decimal digits is performed by subroutines. Instructions are one or two words. Programming for the 160 series computers is complicated by the short computer word length. Instructions that reference operands in general storage must be two words long.

The buffered channel supplied with the basic 160-A handles one input or output block transfer at a time. The basic 160-A therefore can perform computation or an input or output transfer on the Normal channel, while simultaneously transferring a block of data on the Buffer channel.

Two card readers are available for the 160-A. The Model 167-2 reads 250 cards per minute, and the IBM 088 Collator, which is connected through the 1610-A Input-Output Control, reads 650 cards per minute. Two card punches are also available: the IBM 523, which operates under control of a Model 170 Card Punch Controller, and the IBM 533, which operates under control of a 1610-A Control. Both can punch 100 cards per minute. The fast paper tape reader and punch, which can be used only by the Normal channel, operate at 350 and 110 rows per second, respectively. Control Data offers two printers, the Model 166-2 buffered line printer, which prints either alphameric or numeric data at a rate of 150 lines per minute, and the 1612 Line Printer, which prints 500 alphameric and 1,000 numeric lines per minute. Two magnetic tape drives are available, the 603 Tape Units with 15,000 or 41,667 character per second transfer rates, and the 606 Tape Units with 30,000 or 83,333 character per second transfer rates. The older 163 and 164 Tape Units are no longer being manufactured.

The 160-A has an instruction repertoire of 134 instructions, most of which are variations of several basic instructions. These variations provide restricted relative or indirect modes of addressing. Floating point and multiple precision fixed point operations are

INTRODUCTION (Contd.)

§ 011.

performed by subroutines or optional hardware units. The central processor performs no parity checking on internal word transfers or on data transferred to and from peripheral devices. Longitudinal and transverse parity is checked by the magnetic tape units, and the processor must test for parity errors.

Problem oriented facilities include subroutines for multiple precision arithmetic and data transcriptions, as well as sorting, matrix inversion, and a number of industrial design and statistical programs.

The 160-A assembly language translator, OSAS-A, is the 160-A version of the 160 OSAS and offers a larger symbol table than OSAS. No macro instructions can be included, but library subroutines can be assembled with the source statements.

Two floating point interpretive systems, SICOM and INTERFOR, are available for the 160-A. Both systems use four 160-A words to hold each data item and two storage words to hold each instruction. SICOM offers a large instruction repertoire, flexible input-output facilities, alphameric data handling capabilities, and a built-in trace mode. INTERFOR has a repertoire of only 22 instructions, most of which correspond directly to a limited group of machine language instructions in the large-scale CDC 1604 and 1604-A computers. The main feature of the INTERFOR system is an assembly routine that makes it possible to code source programs in a convenient symbolic language; SICOM programs must be written in absolute numeric code. This INTERFOR feature permits 1604/1604-A floating point routines to be run on the 160-A if they include only the mnemonics accepted by the assembler.

160 FORTRAN-A, a version of 160 FORTRAN modified to operate on the 160-A, is currently available and can be used on systems with only punched tape input-output equipment. An improved system called 160-A FORTRAN is now in field test status. It will require at least two magnetic tape units for compilation. Both systems use restricted versions of the FORTRAN II language. The only significant FORTRAN II facilities not included in 160-A FORTRAN are the FUNCTION statement and double precision and complex variables. Both systems permit the use of Boolean statements and mixed arithmetic. Object programs produced by both FORTRAN systems are executed interpretively. Compile-and-run operation is possible with 160-A FORTRAN.

AUTOCOMM is a COBOL-like programming system designed for pseudo-English coding of commercial data processing applications. An AUTOCOMM source program consists of a Data Section, which describes the files and items to be processed, and a Procedure Section, which describes the operations to be performed. The operation repertoire includes decimal arithmetic, multi-word transfers, alphabetic and numeric comparisons, format conversions, and editing. AUTOCOMM object programs consist largely of return jumps to a library of standard macro routines that implement the source statements. AUTOCOMM should be somewhat simpler to learn and use than the COBOL language, but its facilities are considerably more limited than those of COBOL.

SWAP, the 160/160-A users' group, publishes an updated list of routines and has defined the minimum SWAP computer as the basic paper tape system with basic core storage and no typewriter.

Control Data offers program-controlled satellite operation of the 1604 or 1604-A system and the 160 or 160-A system. Either processor can transfer data to or from common magnetic tape units via a tape controller, or can set up a direct communication path between the systems by using the read and write data registers of the controller. These connections are set up under control of a program which can also test the status of the controller. The 1607 Tape Control with Ampex Tape Units was available earlier. At present, the 1615 Tape Control, which uses CDC 606 Tape Units, is offered for satellite operation. The satellite system is more a capability than an actual system; no manuals exist for the 1615 Satellite system, and no such system has been installed.

The 160 and 160-A processors can transfer data to and from peripheral equipment of the new CDC 3600 computer, using the CDC 3681 Data Channel Converter. In addition, the CDC 160-A can operate with the 3681 Converter and CDC 3600 Computer in a satellite mode. Further information must be obtained from the manufacturer.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word in storage:	12 bits	basic storage location.
Row on punched tape:	5 to 8 bits (tracks)	BCD or binary character on punched tape.
Row on magnetic tape:	6 bits + parity bit	BCD or binary character on punched tape.
Column on card:	12 rows	1 Hollerith character or 1 binary word.

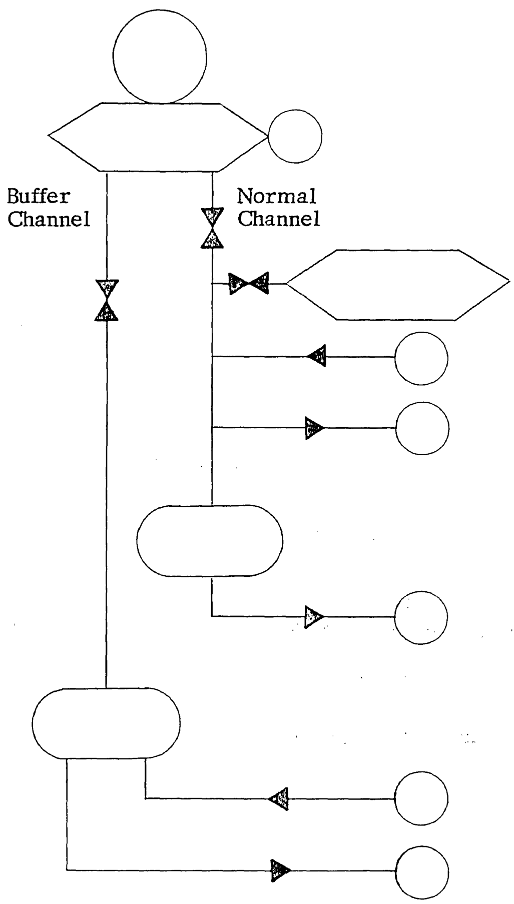
.2 INFORMATION FORMATS

Type of Information	Representation
Numeral:	1 BCD digit on external medium.
Octal digit:	3 binary bits.
Number:	1 word of 11 bits plus sign bit.
Instruction:	1 or 2 words.
Block:	group of words in core storage between 2 specified addresses.
	group of words on external medium.

§ 031. SYSTEM CONFIGURATION

.1 CARD SYSTEM; CONFIGURATION I

Deviations From Standard Configuration: . . . . paper tape equipment supplied with processor.
core storage higher by 4,000 words.
card reader slower by 35%.
card punch slower by 50%.
printer slower by 50%.
no indexing.



Equipment	Rental
Basic Core Storage: 8,192 words	---------
Processor and Console	$ 2,250
168-1 Arithmetic Unit	390
Paper Tape Reader: 350 rows/sec.	---------
Paper Tape Punch: 110 rows/sec.	---------
1612 Printer Control 1612 Printer: 500 lines/minute	1,840
1610-A Card Reader-Punch Control	1,500
IBM 088 Collator: 650 cards/minute	---------
IBM 523 Card Punch: 100 cards/minute	---------

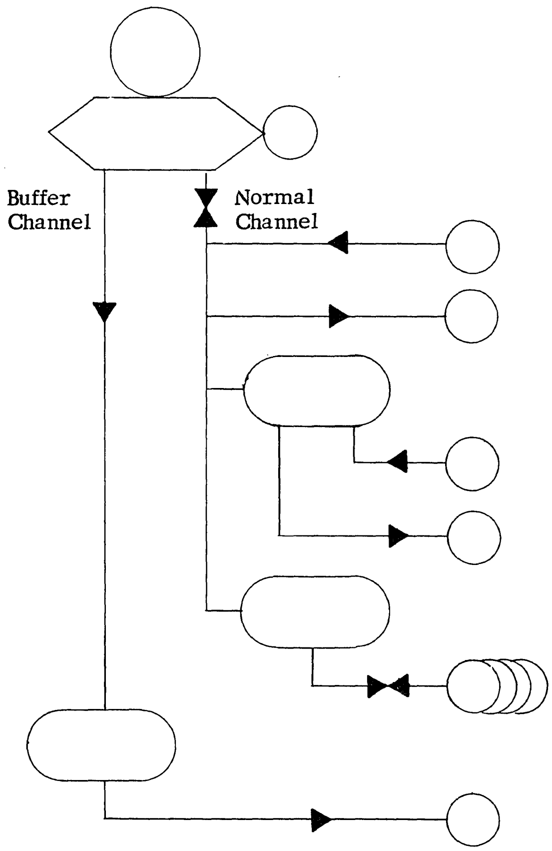
Optional Features Included: . . . . Multiple-Divide.

Rental: . . . . $5,980 per month plus IBM equipment.

§ 031.

.2 4-TAPE BUSINESS SYSTEM; CONFIGURATION II

Deviations From Standard Configuration: . . . . paper tape equipment supplied with processor.
core storage higher by 4,000 words.
card reader 30% faster.
1 extra input-output channel.
magnetic tape 27,000 char/sec faster.



Equipment	Rental
Basic Core Storage: 8,192 words	---------
Processor and Console:	$ 2,250
Paper Tape Reader: 350 rows/sec.	---------
Paper Tape Punch: 110 rows/sec.	---------
1610-A Card Reader-Punch Control	1,500
IBM 088 Collator: 650 cards/minute	---------
IBM 523 Card Punch: 100 cards/minute	---------
162-1 Magnetic Tape Control	500
603 Magnetic Tape Units (4): 15,000 or 41,700 char/sec.	2,200
1612 Printer Control; 1612 Printer: 500 lines/minute	1,840

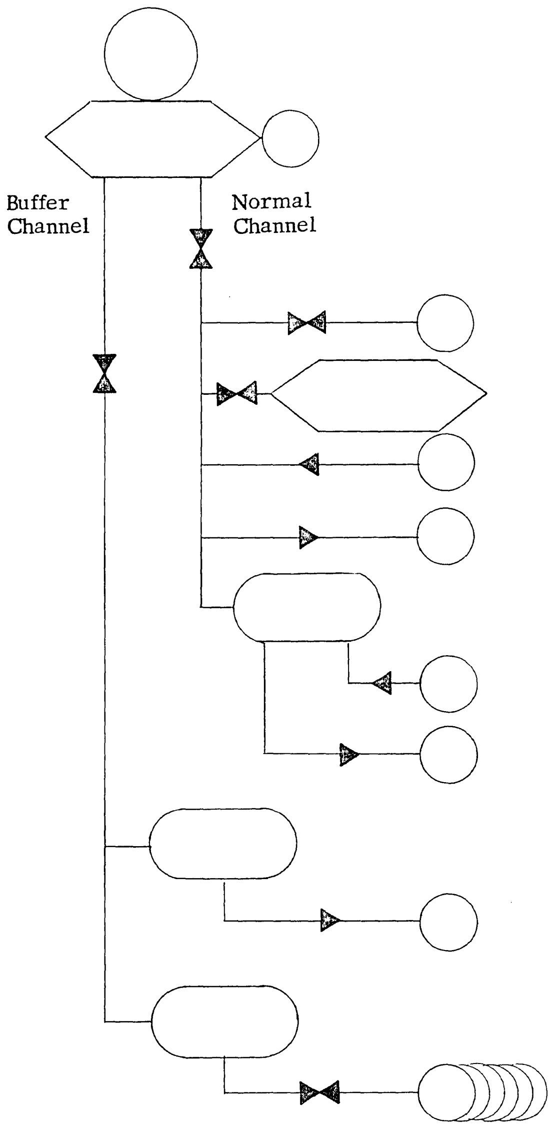
Optional Features Included: . . . . none.

Rental: . . . . $8,290 per month plus IBM equipment.

§ 031.

.3 6-TAPE BUSINESS SYSTEM; CONFIGURATION III

Deviations from Standard Configuration: . . paper tape equipment supplied with processor.
card reader 30% faster.
magnetic tape 40% faster.
no indexing.
only 1 simultaneous transfer while computing, rather than 2.



Equipment	Rental
Basic Core Storage: 8,192 words	---------
Processor and Console	$ 2,250
161 Typewriter	262
168-1 Arithmetic Unit	390
Paper Tape Reader: 350 rows/sec.	---------
Paper Tape Punch: 110 rows/sec.	---------
1610-A Card Reader-Punch Control	1,500
IBM 088 Collator: 650 cards/minute	---------
IBM 523 Card Punch: 100 cards/minute	---------
1612 Printer Control 1612 Printer: 500 lines/minute	1,840
162-1 Magnetic Tape Control	500
603 Magnetic Tape Units (6): 15,000 or 41,700 char/sec.	3,300

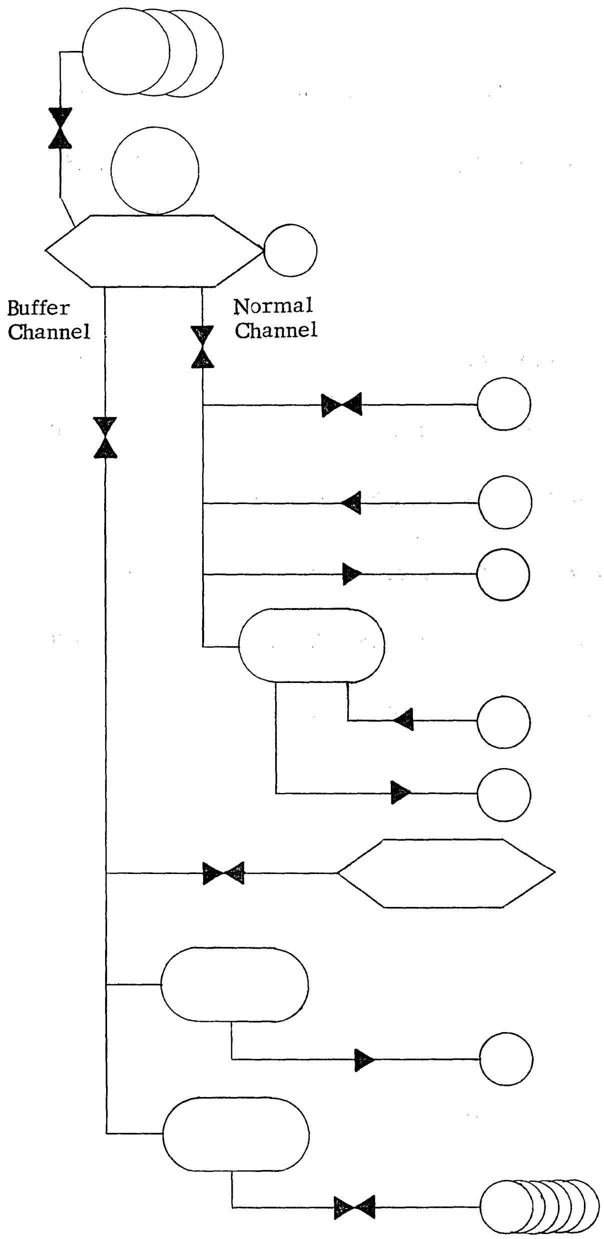
Optional Features Included: . . . . Multiply-Divide.
161 Typewriter.

Rental: . . . . $10,042 per month plus IBM equipment.

§ 031

.4 6-TAPE BUSINESS/SCIENTIFIC SYSTEM; CONFIGURATION VI

Deviations from Standard Configuration: . . . . paper tape equipment supplied with processor.
card reader 30% faster.
magnetic tape 40% faster.
no indexing.
only one simultaneous transfer while computing, rather than 2. Additional buffered channel supplied in 169 Auxiliary Memory Unit may be used for an additional simultaneous data transfer.
fixed point multiply-divide by subroutine.



Equipment	Rental
169 Auxiliary Memory Unit: 3 modules of 8,192 words each of core storage.	$ 2,750
Basic Core Storage: 8,192 words	---------
Processor and Console	2,250
161 Typewriter	262
Paper Tape Reader: 350 rows/sec.	---------
Paper Tape Punch: 110 rows/sec.	---------
1610-A Card Reader-Punch Control	1,500
IBM 088 Collator: 650 cards/minute	---------
IBM 523 Card Punch: 100 cards/minute	---------
168-2 Arithmetic Unit	450
1612 Printer Control 1612 Printer: 500 lines/minute	1,840
162-1 Magnetic Tape Control	500
603 Magnetic Tape Units (6): 15,000 or 41,700 char/sec.	3,300

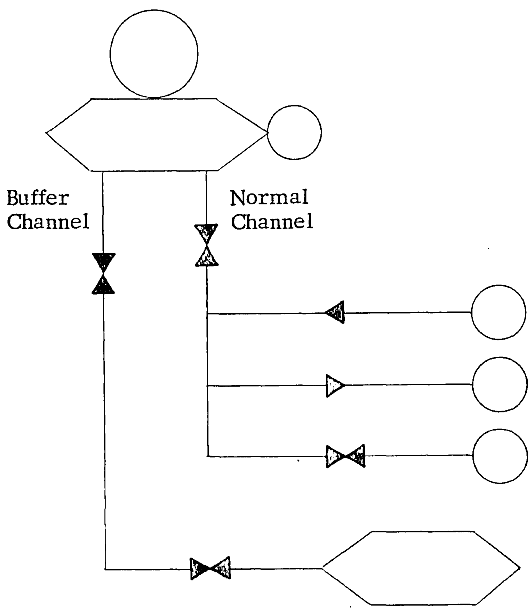
Optional Features Included: . . . . 3 modules of core storage.
168-2 Arithmetic Unit
161 Typewriter.

Rental: . . . . $12,852 per month plus IBM equipment.

§ 031.

.5 DESK SIZE SCIENTIFIC SYSTEM; CONFIGURATION IX

Deviations from Standard Configuration: . . . . core storage smaller by 1,300 words.
paper tape input faster by 340 rows/sec.
paper tape output faster by 100 rows/sec.



Equipment	Rental
Basic Core Storage: 8,192 words	---------
Processor and Console	$ 2,250
Paper Tape Reader: 350 rows/sec.	---------
Paper Tape Punch: 110 rows/sec.	---------
161 Typewriter	262
168-1 Arithmetic Unit (fixed point)	390

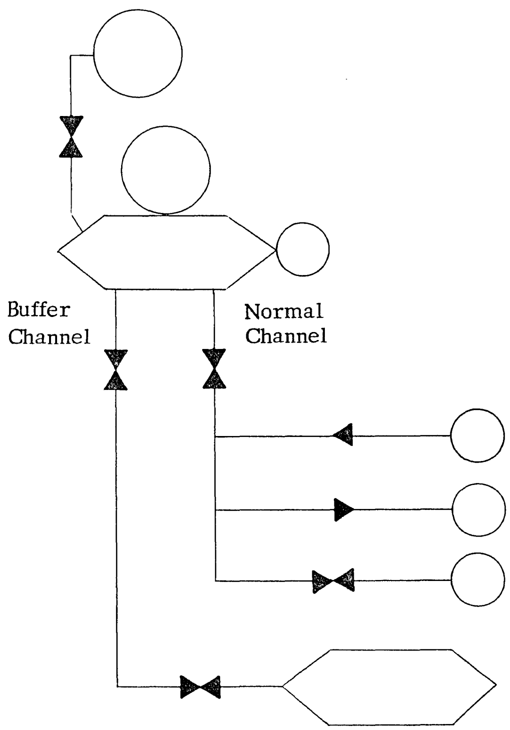
Optional Features Included: . . . . 161 Typewriter.

Rental: . . . . $2,902 per month.

§ 031.

.6 PUNCHED TAPE/CARD SCIENTIFIC SYSTEM; CONFIGURATION X

Deviations from Standard Configuration: . . . . core storage smaller by 2,280 words.
paper tape input faster by 75%.
only 1 simultaneous transfer while computing, rather than 2. Additional buffered channel supplied in 169 Auxiliary Memory Unit may be used for an additional simultaneous data transfer.
no indexing.
fixed point multiply-divide by subroutine.



Equipment	Rental
169 Auxiliary Memory Unit: 1 module of 8,192 words of core storage	$ 1,250
Basic Core Storage: 8,192 words	---------
Processor and Console	2,250
Paper Tape Reader: 350 rows/sec.	---------
Paper Tape Punch: 110 rows/sec.	---------
161 Typewriter	262
168-2 Arithmetic Unit	450

Optional Features Included: . . . . 1 module of core storage.
161 Typewriter.
168-2 Arithmetic Unit

Rental: . . . . $4,212 per month.

INTERNAL STORAGE: CORE STORAGE

§ 041.

.1 GENERAL

.11 Identity: . . . . basic core storage; part of 160-A Processor. 169 Auxiliary Memory Unit.

.12 Basic Use: . . . . . . working storage.

.13 Description

The basic storage capacity of the 160-A Processor is 8,192 12-bit words, which is twice the capacity of the 160 Processor. This capacity may be increased to a total of 32,768 words by the addition of one, two, or three modules of 8,192 words each, using the Model 169 Auxiliary Memory Unit. Each group (module) of 8,192 words is considered as containing two banks of 4,096 words. The Model 169 includes a buffered input-output channel which permits an input-output transfer to overlap computation. The manufacturer states that this feature permits two 160-A processors to share core storage.

The read-restore cycle time is 6.4 microseconds per word. Each word stores one character from an input device, or one 12-bit binary number, including its sign. No parity bit is included. One or two words are required to hold an instruction, as the processor has both one-word and two-word instructions.

Words are not directly addressable within the normal addressing scheme permitted by the 12-bit word (4 octal digits). The processor contains four storage bank control registers, each of which can store an octal digit used for selecting one of the eight storage banks. Instructions and operands use the digit in one of the four registers for bank selection, and addressing in any of seven modes is done within the selected bank. Instructions are available to load bank selection digits into the four storage control registers.

No areas of storage are reserved, although locations 0070_8 to 0077_8 in each bank are used by programming convention for temporary storage as counters, etc., and locations 0000_8 to 0067_8 in each bank are reserved in a similar manner for indirect addressing direct addresses.

.14 Availability: . . . . . 4 months.

.15 First Delivery: . . . . 1961, basic storage. 1962, 169 unit.

.16 Reserved Storage: . . 56 words per bank held by convention for indirect addressing (0000_8 to 0067_8). 8 words per bank held by convention for temporary storage (0070_8 to 0077_8).

.2 PHYSICAL FORM

.21 Storage Medium: . . . magnetic core.

.22 Physical Dimensions

.221 Magnetic core storage
Core diameter: . . . 0.050 inch o.d. 0.030 inch i.d.
Array size: . . . . . 64 bits by 64 bits by 12 bits.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . yes.
.244 Data permanent: . . . no.
.245 Storage changeable: . . no.

.28 Access Techniques

.281 Recording method: . . coincident current.
.282 Reading method: . . . same as recording.
.283 Type of access: . . . . uniform.

.29 Potential Transfer Rates

.291 Peak data rates
Cycling rates: . . . . 156,250 cycles/sec.
Unit of data: . . . . . word.
Conversion factor: . . 12 bits/word.
Data rate: . . . . . 312,500 char/sec. 468,750 digits/sec. 1,875,000 bits/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage			Maximum Storage
Identity:	basic storage plus 169-1	basic storage plus 169-1	basic storage plus 169-2	basic storage plus 169-3.
Words:	8,192	16,384	24,576	32,768.
Characters:	16,384	32,768	49,152	65,536.
Instructions:	6,000, approx.	12,000, approx.	18,000, approx.	24,000, approx.
Banks:	2	4	6	8.
Digits:	24,576	49,152	73,728	98,304.
Modules:	1	2	3	4.

.32 Rules for Combining Modules: . . . . . . any one of the above columns may be selected.

§ 041.

.4 CONTROLLER: . . . no separate controller.

.5 ACCESS TIMING

.51 Arrangement of Heads: 1 access device.

.52 Simultaneous Operations: . . . . . using Model 169 Auxiliary Memory Unit. A block of data from a storage bank of the Model 169 can be transferred to an external device via buffer register of the 169 at the same time as the 160-A and the remainder of the storage modules of the 169 operate normally.

.53 Access Time Parameters and Variations

.531 For uniform access
Access time: . . . . 6.4μ sec.
Cycle time: . . . . . 6.4μ sec.
For data unit of: . . . 1 word of 12 bits.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.71 Data Transfer

Pair of storage unit possibilities
With self: . . . . . by programming.

.72 Transfer Load Size

With self via Accumulator: . . . . 1 word.

.73 Effective Transfer Rate

With self: . . . . . . 22,300 words/sec, using straight-line coding.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid Address:	non-existent bank check	halt; alarm.
Invalid code:	all valid.	
Receipt of data:	none.	
Recording of data:	none.	
Recovery of data:	none.	
Dispatch of data:	none.	
Timing conflicts:	interlock, wait.	
Timing error in equipment:	interlock in 169	halt, alarm.

AUXILIARY STORAGE: 8951 MAGNETIC DRUM

§ 042.

.1 GENERAL

.11 Identity: . . . . Magnetic Drum.
Model 8951.

.12 Basic Use: . . . . . . auxiliary storage.

.13 Description

The 8951 Magnetic Drum is a new drum storage unit which stores 32,864 words and has a transfer rate of 32,000 words per second. No further information on the unit is available.

.14 Availability: . . . . . 4 to 6 months.

.15 First Delivery: . . . . first quarter 1963.

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . . . 160-A Processor.

.12 Description

The basic 160-A Processor operates at the same speeds as the 160 Processor, but has a larger basic core storage, a buffered input-output channel, an interrupt system, and additional instructions. The 160-A also provides for additional core storage and the facility to connect an arithmetic unit which speeds up floating point calculations.

The 160-A Processor is capable of relatively high processing speeds, but handles operands of only 11 data bits plus a sign bit. The instruction repertoire contains few basic instructions, but almost every instruction has eight possible addressing modes, with the result that programming to realize the full capabilities of the processor is complex. Instructions are performed in the single-address mode and consist of one or two words. The 11-bit data word provides a precision of only 3.3 decimal digits. Double or greater precision arithmetic, if used, must be supplied by subroutines or through use of the optional 168-1 Arithmetic Unit. Floating point operations are performed by subroutines, or by subroutines and the optional 168-2 Arithmetic Unit. Single precision arithmetic operands in the 160-A are treated as 11 bits plus a sign bit. A single precision add-to-accumulator operation requires three storage cycles of 6.4 microseconds each. Words in storage contain no parity bits, and parity is not checked automatically on input or output.

The instruction repertoire includes add-to-storage and Boolean commands, but lacks compare and radix conversion instructions. Three sense switches and three selective stop switches are provided. Automatic multiply and divide are not provided as standard; however, the Model 168-1 Arithmetic Unit is available for double precision add-subtract operations, and for single or double precision multiply and divide operations (see Section 244:052). Double precision add or subtract requires 145 microseconds using the 168-1 Arithmetic Unit; performing the add or subtract operations by subroutine requires 225 or 300 microseconds, respectively.

Indexing and indirect addressing are two of the eight addressing modes under which an instruction may operate. The usual single-address instruction, which calls for an operand anywhere in core storage, requires two successive computer words, and is found as one of the addressing modes. The modes are distinguished by the instruction operation codes, and are applicable to most instruction types. These eight addressing modes, and their operand locations, are summarized in the table which follows. The Relative mode is counted as two modes.

.12 Description (Contd.)

CDC 160-A ADDRESSING MODES

Address Mode	Instruction Length (Words)	Operand Location †
No-	1	E ‡
Direct-	1	(E)
Indirect-	1	Contents of (E)
Relative-	1	P ± E ǂ
Constant-	2	P + 1
Memory-	2	(P + 1)
Specific-	1	7777_8

† E is 2-octal-digit field in instruction.
‡ ( ) means "contents of."
ǂ P is value of instruction counter.

Literals can be provided by the No Address and Constant Address modes of instructions. In the No Address mode, the E field of the instruction is used as the operand (two octal digits), and in the Constant Address mode the word following the instruction word is used as the operand (four octal digits).

The storage bank to be referenced is specified through one of four bank control registers. Designated as the direct, indirect, relative, and buffer bank control registers, these registers correspond to three of the instruction address modes and to Buffer channel data transfers. All instructions are obtained using the relative bank control. Operands are found in banks corresponding to the addressing modes: full details are in the manufacturer's 160-A Computer Programming Manual.

The additional instructions in the 160-A not present on the 160 provide the following: additional internal shifting; a return jump; selective stops and selective jumps; a conditional jump, depending on the status of the Buffer channel; control for the storage bank control registers and the Buffer channel control registers; clear of interrupt lockout; and several other miscellaneous functions.

The interrupt system contains four separate interrupt channels: one for the operator, one which occurs at the end of every buffered data transfer, and two for external equipment. Occurrence of an interrupt causes automatic program transfer to one of four fixed locations, one location for each interrupt channel. All further interrupts are locked out until cleared by the program.

The 160-A has two types of input-output commands: external function commands and data transfer commands. These commands are similar to the input-output commands of the 1604/1604-A computers. The external function commands select devices and specify the operation to the device. The data trans-

§ 051.

.12 Description (Contd.)

fer commands specify the block of data to be transferred, and initiate the transfer. In addition, the external function command can request the external device to present its status, for interpretation by the central processor.

The recommended general procedure for an input-output operation is as follows: status request, status test, select unit, initiate data transfer; then status request and status test after the operation is finished. Status checking is recommended to avoid indefinite delays in case a unit is not capable of being operated (for example, power to the unit may be off). If power to a unit is off, its status can still be determined. The paper tape reader and punch are built into the processor and have no status codes.

Peripheral devices can be connected to either the Buffer channel or the Normal channel. Exceptions are the paper tape reader and punch, which are always connected to the Normal channel. The other devices can easily be changed from one channel to the other. A peripheral unit connected to the Normal Channel can transfer data over the Normal channel only, but a unit connected to the Buffer channel can transfer data over either channel, depending on the input-output command used. A peripheral device connected to the Buffer channel and transferring data via the Normal channel prevents use of the Buffer channel during the transfer. Simultaneous operations are effected by initiating a transfer on the Buffer channel, then either executing instructions in the processor or transferring data via the Normal channel.

Programming the 160-A system is necessarily complex because of the short computer word length. One immediate consequence of the short word is that instructions which reference arbitrary core locations are two words long. A second consequence is that a computer word cannot specify the complete address of a core storage location, and the contents of a bank control register must be used implicitly to select one of eight available core banks.

When an instruction references a location through relative addressing (plus or minus 63 locations of the program counter) or through indirect addressing (using 64 standard locations per bank) it requires only 1 word. These instructions are easy and convenient to use within short loops. However, when using symbolic locations, it is easy to exceed the 63-word limit by mistake (or when patching), thereby causing errors.

The disadvantages of this multi-mode programming are:

- Non-uniform instruction forms
- The attendant changes in thinking while programming
- Potential for making mistakes
- The requirement for changing bank control register contents.

Since the addresses are 12-bit numbers, address modification can be difficult. The address is treated by the arithmetic unit as an 11-bit number with a range of ±2,047 rather than an absolute address with a maximum value of 4,095.

.13 Availability: . . . . . 4 months.

.14 First Delivery: . . . 1961.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point			
	Add-subtract:	automatic	binary	11 bits + sign bit.
	Multiply			
	Short:	subroutine	binary	22 bits.
	Long:	subroutine	binary or decimal	depends on routine.
		optional 168-1	binary	11 or 22 bits.
	Divide			
	No remainder:	subroutine	binary	22 bits.
	Remainder:	subroutine	binary or decimal	depends on routine.
		optional 168-1	binary	11 or 22 bits.
.212	Floating point:	binary operations using either subroutines or subroutines and optional 168.2.		
.213	Boolean			
	AND:	automatic	binary	12 bits.
	Inclusive OR:	none.		
	Exclusive OR: (same as Selective Complement instruction)	automatic	bianry	12 bits.

.214 Comparison: . . . . . none.
.215 Code translation: . . . subroutine.
.216 Radix conversion: . . . subroutine.
.217 Edit format: . . . . . no edit facilities.
.218 Table look-up: . . . . none.
.219 Others
Add and replace operand with sum: . automatic.
Replace operand with operand + binary one: . . . . automatic.

.22 Special Cases of Operands

.221 Negative numbers: . . "1" in most significant bit position (one's complement).
.222 Zero: . . . . + or -; either usable in arithmetic. Must be + zero for branch on zero.
.223 Operand size determination: . . . . . fixed at 11 bits + sign bit (12 bits one's complement).

.23 Instruction Formats

.231 Instruction structure: 1 or 2 words.
.232 Instruction layout
.2321 1-word instruction:

Part	Function Code (F)	Execution Address (E)
Size (bits)	6	6

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.2322 2-word instruction:
Word 1

Part	Function Code (F)	Execution Address (E)
Size (Bits)	6	6 (all zeros)

Word 2

Part	Address or Operand (G)
Size (bits)	12

.233 Instruction parts

Name	Purpose
Function code (F): . .	operation code.
Execution address (E): . . .	specifies absolute address, or increment to present program counter contents (max value of 77 octal), or 6-bit value.
Address or Operand(G):	absolute address, or 12-bit value.

.234 Basic address structure: single address.
.235 Literals
Arithmetic: . . . . . 1 word.
Comparisons and tests: . . . . . . none.
.236 Directly addressed operands:. . . . . . operands are 1 word long. The structure of the instruction permits addressing of only 4,096 words directly; a bank control register is used to select which 1 of the 8 possible banks of 4,096 words is to be used. Basic storage contains 2 banks. The Model 169 Auxiliary Unit adds 2, 4, or 6 more banks.
.2361 Internal storage type: . . . . . . core storage.
Minimum size: . . . 8,192 words.
Maximum size: . . . 8,192 words.
Valume accessible: . 8,192 using bank control register; but note that sequential states of address counter skip an address at two different counts. These are usable by setting counter.
.237 Address indexing: . . . none as such; see .2373.
.2371 Number of methods: 1.
.2373 Indexing rule: . . . effective operand address is formed by incrementing or decrementing contents of instruction counter by "E" value in instruction. Maximum value of "E" is decimal 63.
.2374 Index specification: . operation code.
.2375 Number of potential indexers: . . . . . 1.
.2376 Addresses which can be indexed: . . . . no restrictions.
.2377 Cumulative indexing: not possible.
.2378 Combined index and step: . . . . not possible.
.238 Indirect addressing: none as such; see .2382.
.2381 Recursive: . . . . . no.
.2382 Designation: . . . . operation code specifies indirect addressing mode; "E" value in instruction specifies one of 64 indirect addresses, located in addresses 0000 to 0077 (octal).
.2384 Indexing with indirect addressing: . . . . not possible.
.239 Stepping: . . . . . . none.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size in bits	Program usage
Instruction counter (P):	1	12	stores location of present insruction.
Accumulator (A):	1	12	arithmetic accumulator register.

.242

Category of storage	Total number locations	Physical form	Access time, μsec	Cycle time, μsec
P:	1 word	flip-flops	6.4	6.4
A:	1 word	flip-flops	6.4	6.4

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: . . . . single address.

.311 Number of sequence control facilities: . . . . . 1.
.314 Special sub-sequence counters: . . . . . none.
.315 Sequence control step size: . . . . 1 instruction (1 or 2 words).
.316 Accessibility to routines: . . . . . . yes.
.317 Permanent or optional modifier: . . . . . . none.

.32 Look-Ahead: . . . . . none.

.33 Interruption

.331 Possible causes
Standard: . . . . . operator pressing any combination of a Selective Stop and a Selective Jump switch (interrupt line #10).
termination of every Buffer channel data transfer (interrupt line #20).
Special: . . . . . . any input-output device or controller which can generate an interrupt signal (interrupt lines #30 and 40).
.332 Program control
Individual control: none.
Method
The 4 interrupt lines are serviced on a priority basis, with #10 first and #40 last. Whenever an interrupt takes place, or whenever an external function instruction is executed, all further interrupts are locked out until the lockout is cleared under program control by a Clear Interrupt Lockout instruction. Thus, if each interrupt routine has a CIL instruction, all active interrupts will be serviced. Any interrupt line which becomes

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332 Program control (Contd.)
Method (Contd.)
active remains active until it is accepted, or until a console master clear is performed. This master clear removes interrupt lockout.
Restriction: . . . . none; see description of operation under Method above.

.333 Operator control: . . . operator can clear pending interrupts but cannot prevent them from becoming active again.

.334 Interruption conditions: none.

.335 Interruption process
Disabling interruption: further interruptions on other lines are locked out and saved.
Registers saved: . . . contents of program counter saved in one of four locations depending on which interrupt line is activated. Accumulator saved only if interrupt routine does so.
Destination: . . . . program control transferred to one of four locations depending on which interrupt line is activated. Transfer back depends on the interrupt routine.

.336 Control methods
Determine cause: . . one interrupt routine for each interrupt line (#10, 20, 30, and 40.).
Enable interruption: . . . interruption re-enabled when CIL instruction executed.

.34 Multi-Running: . . . . as programmed using the interrupt facilities.

.35 Multi-sequencing: . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in μsec

.411 Fixed point
Single precision (11 bits)
Add-subtract: . . . . 19.2.
Multiply: . . . . . . 650, by subroutine.
Divide: . . . . 2,000, by subroutine.
Double precision using 168-1 Arithmetic Unit
Add-subtract: . . . . 145.
Multiply: . . . . . . 250.
Divide: . . . . 295 to 365.
Double precision using subroutines
Add: . . . . 225.
Subtract: . . . . . . 300.
Multiply: . . . . . . 5,000 to 10,000.
Divide: . . . . 10,000.

.412 Floating point

		By subroutines and 168-2 Arithmetic Units
Add-subtract:	4,000	1,000 (**).
Multiply:	14,000	1,500 (**).
Divide:	19,000	1,500 (**).

.413 Additional allowance for
Indexing: . . . . no indexing.
Indirect addressing: . 0.
Re-complementing: . 0.

.414 Control
Compare: . . . . no compare.
Branch: . . . . 6.4, short jump. 12.8, unlimited.
Compare and branch: 25.6 or 32.

.415 Counter control: . . . . no counters.

.416 Edit: . . . . no edit instruction.

.417 Convert: . . . . no convert instruction.

.418 Shift: . . . . 6.4 μsec for 1 to 6 bits; circular.

.42 Processor Performance in μsec

Conditions

I: . . . . fixed point, single precision.
II: . . . . fixed point, programmed double precision.
III: . . . . floating point using subroutines; 8 decimal digits.
IV: . . . . floating point using 168-2 Arithmetic Unit.

.421 For random addresses

	I	II	III	IV
c = a + b:	64	480	4,350	1,000.
b = a + b:	45	480	4,350	1,000.
Sum N items:	19	314	4,120	1,000.
c = ab:	2,000 †	7,700 av.	14,200	1,500.
c = a/b:	2,000 †	10,200	19,200	1,500.

† programmed.

.422 For arrays of data

	I	II	III	IV
$c_i = a_i + b_j$:	192	698	4,640	1,290.
$b_j = a_i + b_j$:	147	698	4,580	1,240.
Sum N items:	115	390	4,430	1,080.
$c = c + a_i b_j$:	2,000 †	8,420	18,700	2,740.

† programmed.

.423 Branch based on comparison
Numeric data: . . . . 154 (1 word of 4 octal digits).
Alphabetic data: . . . not applicable.

.424 Switching
Unchecked: . . . . . . 154.
Checked: . . . . 256.
List search: . . . . . 45 + 128N.

.425 Format control per character
Unpack
Scientific
Binary: . . . . . . 0.
BCD input to double precision fixed point: . . . . . . 251.
BCD input to floating point: . . 1,125 (***).
Compose
Scientific
Binary: . . . . . . 14, for moving.
BCD from double precision fixed point: . . . . . . 4,345.
BCD from floating point: . . . . . . 13,040 (***).

(***) Estimate by editorial staff (see 1:010.400).

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.426 Table look-up per comparison
- For a match: . . . . . 115.
- For least or greatest: 160.
- For interpolation point: . . . . 109.

.427 Bit indicators
- Set bit in pattern: . . 58.
- Test bit in pattern:. . 26.
- Test AND for B bits: . 45.
- Test OR for B bits:. . 26.

.428 Moving: . . . . 45 per word.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	none.	
Zero divisor:	none.	
Invalid operation:	none.	
Invalid data:	none.	
Arithmetic error:	none.	
Invalid address:	check on non-existent bank	?
Receipt of data:	none.	
Dispatch of data:	none.	
Timing fault:	interlock	?
Interrupt lockout:	?	?
Output unit not selected properly:	interlock	alarm.
Input unit not selected properly:	interlock	alarm.

CENTRAL PROCESSOR: ARITHMETIC UNIT

§ 052.

.1 GENERAL

.11 Identity: . . . . Fixed Point Arithmetic Unit. 168-1.

.12 Description

The 168-1 Arithmetic Unit performs double precision fixed point add and subtract operations for the 160 and 160-A Processors; it also performs fixed point single or double precision multiply and divide operations. The Processor addresses the Arithmetic Unit and transfers the 11-bit binary number (plus sign) operands to it. After the calculation has been completed within the Arithmetic unit the Processor program initiates transfer of the results to the Processor. During the computation, both the 160 and 160-A Processors have some free time to execute other program steps. Paragraph .411 summarizes these times. The free times include loading and unloading the operands from core storage to the Arithmetic Unit and back to core storage.

The 160 and 160-A Processors can interrogate the Arithmetic Unit to determine its status, to help the program run efficiently. The status responses possible are: Unit Ready, Add/Subtract Overflow, Divide Fault, Unload Not Completed, and Busy Computing. The 168-1 Arithmetic Unit does not contain an Accumulator, and hence operations on strings of operands are not possible without reloading.

.13 Availability:. . . . . . 4 months.

.14 First Delivery: . . . . 1962.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point			
	Add-subtract:	automatic	binary	22 bits.
	Multiply			
	Short:	none.		
	Long:	automatic	binary	11 or 22 bits.
	Divide			
	No remainder:	none.		
	Remainder:	automatic	binary	22 or 44 bits.

.212 Floating point: . . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in μsec

.411 Fixed point †
- Add-subtract
  - Double precision (22 bits): . . . . . 145.
- Multiply
  - Single precision (11 x 11 bits): . . . 120.
  - Double precision (22 x 22 bits): . . . 250.
- Divide
  - Single precision (22 ÷ 11 bits): . . . 145 to 180.
  - Double precision (44 ÷ 22 bits): . . . 295 to 365.

Note: 160/160-A Processor has some free time available for its own processing, during operation of the 168-1, as follows:

- Add-subtract: . . . . . 5 μsec.
- Single precision multiply: . . . . . . 38 μsec.
- Double precision multiply: . . . . . . 71 μsec.
- Single precision divide: . . . . 39 to 74 μsec.
- Double precision divide: . . . . 72 to 142 μ sec.

† Times given include loading and unloading times of the 168-1 Arithmetic Unit.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	check	‡
Zero divisor:	check	‡
Quotient too large:	check	‡
Arithmetic error:	timing check	alarm on 168-1, halt (?).
Receipt of data:	none.	
Dispatch of data:	none.	

‡ Signal available for sensing by 160/160-A Processor.

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . Console; built into 160-A Processor.

.12 Associated Units: . . none.

.13 Description

The Console is a small sloping panel located toward the rear of the desk-size work area on the top of the Computer unit. The paper tape reader is on the right-hand end of the work area. The Console displays the register and storage contents in octal form using the Arabic numerals 0 through 7. In addition, the status indicator panel displays computer conditions using alphabetic symbols (SEL, IN, OUT, etc.).

The Program, Accumulator, and Storage Registers have their contents displayed, and each of the three displays permits entry of binary data into the registers. The other registers of interest in the 160-A may also be displayed (BER, BFR, bank controls, etc.). The A and Z Register display groups, and the status indicator panel, have colored background lamps for further status indications. Displays light only when the computer is halted.

.2 CONTROLS

.21 Power

Name	Form	Function
On:	blue button	turns system power on.
Off:	red button	turns system power off.
Punch On:	button	control power to respective units.
Punch Off:	button	control power to respective units.
Reader On:	button	control power to respective units.
Reader Off:	button	control power to respective units.

.22 Connections: . . . . . none.

.23 Stops and Restarts

Name: . . . . RUN-STEP.
Form: . . . . 3-position switch.
Function: . . . . RUN starts program. Center halts program. STEP executes 1 storage cycle of instruction each time switch moved from center to STEP.

.24 Stepping

Name: . . . . RUN-STEP.
Form: . . . . 3-position switch.
Function: . . . . see .23 above.

.25 Resets

Name	Form	Function
LOAD-CLEAR:	3-position switch	central is neutral. CLEAR is momentary; clears registers and master controls. LOAD sets condition for Load Mode paper tapes to be read properly.
Clear:	3 push buttons on register displays	clear P, A, or Z Register contents.
Clear:	1 push button next to bank selection entry buttons	clears selected bank control.

.26 Loading

Name: . . . . LOAD-CLEAR.
Form: . . . . 3-position switch.
Function: . . . . sets Load Mode on paper tape input; see .25 above.

.27 Sense Switches

Name	Form	Function
Selective Jump; 4, 2, 1:	3 two-position switches	control jump conditions.
Selective Stop; 4, 2, 1:	3 two-position switches	control stop conditions.

.28 Special

Name: . . . . Margin
Form: . . . . 3-position switch.
Function: . . . . set marginal conditions for test of computer; Hi-Lo. Normally on center; not an operator control.

.3 DISPLAY

.31 Alarms

Name	Form	Function
no name:	red background to A Register display	indicates computer timing fault.
no name:	red background to P Register display group	indicates reference to non-existent storage bank.

.32 Conditions

Name	Form	Function
none:	green background to status indicator	computer in RUN status.
none:	red background to status indicator	STOP or STEP status. Appears when HLT or ERR instruction executed, RUN switch removed from RUN position, or selective stop is executed.

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.32 Conditions (Contd.)

Name	Form	Function
none:	blue background to A Register display group	indicates interrupt lockout.
none:	blue background to Z Register display	shows instruction is in Z Register rather than data.
none:	red background to Z Register group	punch low on tape.
ERR:	alphabetic symbols	computer halted on ERR instruction.
SEL:	alphabetic symbols	computer transmitting selection code.
OUT:	alphabetic symbols	output operation proceeding or being initiated; normal channel.
IN	alphabetic symbols	input operation proceeding or being initiated; normal channel.
IBA:	alphabetic symbols	buffer channel input operation proceeding.
OBA:	alphabetic symbols	buffer channel output operation proceeding.
A, B, C, or D:	alphabetic symbols	shows next instruction cycle.
REL, IND, DIR, or BFR:	alphabetic symbols	in status display; shows which storage bank control is to be used on next storage reference.
0 to 7:	numeric symbol	in status display; shows contents of displayed bank control.

.33 Control Registers

Name	Form	Function
P Register group		
F code:	2 octal digits in Arabic form	current op code; P selector switch up.
P register:	4 octal digits in Arabic form	contents of program counter; P selector switch in center.
S register:	4 octal digits in Arabic form	address of word to be transferred to or from storage; P selector switch down.
A Register group		
BFR register:	4 octal digits in Arabic form	BFR contents; A selector switch up.
A register:	4 octal digits in Arabic form	contents of A register; A selector switch in center.
A' register:	4 octal digits in Arabic form	results of last add operation; A selector switch down.
Z Register group		
BER:	4 octal digits in Arabic form	address of last word transferred on buffer channel; Z selector switch up.
Z register:	4 octal digits in Arabic form	contents of Z register; Z selector switch in center.
BXR:	4 octal digits in Arabic form	indicates terminating address of buffer operation; Z selector switch down.

.34 Storage: . . . . in Z register display. To observe contents of a storage location, set ENTER-SWEEP switch on SWEEP. Set relative bank control to bank desired. Set core storage location into P register via buttons and press RUN-STEP switch to STEP. Z will display one word of core storage as in .33 above.

.4 ENTRY OF DATA

.41 Into Control Registers

Into storage bank controls: . . . . . . use button to select 1 of 4 controls and enter binary data to select bank, using buttons provided.

Into P Register: . . . . press binary-coded buttons below P display to enter data. Press RUN-STEP switch.

Into A Register: . . . set ENTER-SWEEP switch to ENTER. Press binary-coded buttons below A display. Press RUN-STEP switch.

.42 Into Storage: . . . . . into storage via Z and A Registers. Set ENTER-SWEEP switch to ENTER. Set relative bank control using buttons provided. Press binary coded buttons below Z display. Press RUN-STEP switch. Data goes to Z, A, and storage location specified by setting of relative bank control and setting of P.

.5 CONVENIENCES

.51 Communications: . . . none.

.52 Clock: . . . . none.

.53 Desk Space: . . . . . desk height work area 62 in. by 30 in., less small amount for console panel and paper tape reader.

.54 View: . . . . unobstructed in all directions by seated operator.

.6 INPUT-OUTPUT UNIT: none at console. Optional Model 161 Input/Output typewriter has own cabinet near console. Typewriter can output at approximately 10 char/sec.

INPUT-OUTPUT: PAPER TAPE READER

§ 071.

.1 GENERAL

.11 Identity: . . . . Paper Tape Reader. 350.

.12 Description

The 350 Paper Tape Reader is a photoelectric reader mounted on the 160 Console desk that always operates on the Normal Channel in the 160-A Processor. The reading head employs transparent windows which direct light to the photo cells. This construction provides a smooth reading surface that has no holes which can accumulate dust to cause reading errors.

The reader operates at a rate of 350 rows per second when reading blocks of data, and accepts five-, six-, seven, or eight-track paper tapes of standard widths. Reading can be performed on either strips or loops of tape. The tape can be made of paper, parchment, Mylar, or Mylar-aluminate laminate. Slightly-oiled black paper tape is recommended for use on the paper tape punch.

Under program control, the reader can input either one row, or an entire block of data. The end of the block is defined by the instruction and is specified as the final core storage location desired. These programmed inputs are known as the NORMAL mode of input, and one row is placed in the least significant bits of one 12-bit word. The LOAD mode, or automatic load input mode, causes input of two 6-bit rows per core storage 12-bit word, and is halted when a unique control code is read from the tape.

There is no automatic parity check on reading.

.13 Availability: . . . . . . 4 months.

.14 First Delivery: . . . . 1960.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pinch roller friction.
.212 Reservoirs: . . . . . . none.
.213 Feed drive: . . . . . . motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . none.
.222 Sensing system: . . . . silicon photoelectric cells.

.24 Arrangement of Heads

Use of station: . . . . . reading.
Stacks: . . . . 1.
Heads/stack: . . . . . . 8.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . paper tape; tape made of parchment, Mylar or Mylar-aluminum laminate. Lightly-oiled black tape is recommended for the punch.
.312 Phenomenon: . . . . . . fully punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . 1 to N rows at 10 rows per inch.
.322 Parallel by: . . . . . . 5, 6, 7, or 8 tracks at standard spacing.
.324 Track use

Track use	Load Mode	Normal Mode
Data:	6	5, 7, or 8.
Redundancy check:	0	0.
Timing:	1 sprocket	1 sprocket.
Control signals:	1, in alternate rows	0.
Unused:	depends on width	0.
Total:	7	5, 7, or 8 plus sprocket.

.325 Row use: . . . . all for data; no inter-block gap required.

.33 Coding: . . . . matched; see Data Code Table No. 3.

.34 Format Compatibility: . all devices using standard 5- to 8-track punched tape.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.6875 inch for 5-track tape. 0.875 inch for 7-track tape. 1 inch for 8-track tape.
.352 Length: . . . . 1,000 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . built into Console.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . . none.

§ 071.

.44 Data Transfer Control

.441 Size of load: . . . . . . 1 to N rows, 1 row per word (NORMAL Mode). 2 to N rows, 2 rows per word (LOAD Mode).
.442 Input-output area: . . . core storage.
.443 Input-output area access: . . . . each word of core storage.
.444 Input-output area lockout: . . . . yes; serial operation.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 row, or 1 to N rows.
.512 Block demarcation
Input: . . . . address specifications in instruction (NORMAL Mode).

.52 Input-Output Operations

.521 Input
LOAD Mode: . . . . . N rows forward, terminated by missing control punch.
NORMAL Mode: . . . 1 row (INA instruction). 1 to N rows (INP instruction), terminated by final address specification in instruction.
.523 Stepping: . . . . none.
.524 Skipping: . . . . none.
.526 Searching: . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . . none.

.55 Control Operations: . . none.

.56 Testable Conditions: . . none.

.6 PERFORMANCE

.61 Conditions: . . . . none.

.62 Speeds

.621 Nominal or peak speed: 350 rows/sec.
.622 Important parameters
Density: . . . . 10 char/inch.
Speed: . . . . 35 inches/sec.
Start time: . . . . . . 3 msec to next row.
Stop time: . . . . . . 1 msec; stops before next row.
Selecting device: . . . 0.032 msec.
.623 Overhead: . . . . start time.
.624 Effective speeds: . . . 350 rows/sec if less than 0.25 msec elapse between completion of reading one block and initiation of next input operation.

.63 Demands on System

Component: . . . . . . processor.
Msec/row: . . . . 2.9.
Percentage: . . . . . . 100 (on 160 or on Normal channel of 160-A).

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . . number of tracks.
Method: . . . . tape width guide.
Comment: . . . . set for 5, 7, or 8 level tape.

.72 Other Controls

Function: . . . . mode selector.
Form: . . . . LOAD-CLEAR key on Console.
Comment: . . . . selects LOAD mode or NORMAL Mode.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Reel:	1,000 feet.

.732 Replenishment time: . . 0.5 to 1.0 minute; unit needs to be stopped.
.733 Adjustment time: . . . 1.0 minute including replenishment.
.734 Optimum reloading period: . . . . 6 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock
Reading:	none.
Invalid code:	all valid.
Exhausted medium:	none.
Transmitting data:	none.

INPUT-OUTPUT: PAPER TAPE PUNCH

§ 072.

.1 GENERAL

.11 Identity: . . . . Paper Tape Punch. Teletype BRPE-11 Punch.

.12 Description

The Paper Tape Punch is a standard BRPE-11 unit mounted on a hinged rack at the rear of the right wing of the console desk. Punched tape is fed out of a slot in the compartment door.

The Punch operates at a rate of 110 rows per second and punches five-, six-, seven-, or eight-track widths as required. The punch can be programmed to punch either one character at a time or a block at a time. It is always connected to the Normal channel in the 160-A Processor.

Black, lightly-oiled tape is recommended for the punch. No parity check is made on data transmitted to the punch, nor is any recording check made.

.13 Availability: . . . . . 4 months.

.14 First Delivery: . . . . 1960.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket drive.
.212 Reservoirs:. . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . die punch.
.222 Sensing system: . . . . none.

.23 Multiple Copies: . . . none.

.24 Arrangement of Heads

Use of station: . . . . punching
Stacks: . . . . 1.
Heads/stack: . . . . . 8 plus sprocket punch.
Method of use: . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . paper tape.
.312 Phenomenon: . . . . . fully punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . . . 1 to N rows at 10 rows/inch.
.322 Parallel by: . . . . . . 5, 6, 7, or 8 tracks.
.324 Track use
Data: . . . . 5, 6, 7, or 8.
Redundancy check: . . 0.
Timing: . . . . 1 (sprocket hole).
Control signals: . . . punch in alternate rows, when punching a LOAD tape.
Unused: . . . . depends on tape width.
Total:. . . . . 5 to 8.
.325 Row use: . . . . all for data.

.33 Coding:. . . . . matched as in Data Code Tables No. 3 and 4.

.34 Format Compatibility: all devices using standard 5, 7, or 8-track paper tape.

.35 Physical Dimensions

.351 Overall width:. . . . . 0.6875 inch for 5-track tape. 0.875 inch for 6- or 7-track tape.
.352 Length:. . . . . up to 1,000 feet per roll.

.4 CONTROLLER

.41 Identity: . . . . built into console.

.42 Connection to System

.421 On-line: . . . . 1 (on Normal channel in 160-A).
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N rows; 5 to 8 bits of each word per row.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . each word of core storage.
.444 Input-output area lockout: . . . . in 160 only.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 row or 1 to N rows normally. 2 to N rows in punching LOAD tape.
.512 Block demarcation: . . address specifications in instruction.

§ 072.

.52 Input-Output Operations

.522 Output: . . . . punch 1 block forward.
.523 Stepping: . . . . none.
.524 Skipping: . . . . none.
.525 Marking: . . . . none.
.526 Searching: . . . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . . none.

.55 Control Operations: . . none.

.56 Testable Conditions: . . none.

.6 PERFORMANCE

.61 Conditions: . . . . . . none.

.62 Speeds

.621 Nominal or peak speed: 110 rows/sec.
.622 Important parameters
Tape speed: . . . . . 11 inches/sec.
Packing density: . . . 10 rows/inch.
Start time: . . . . . ?
Stop time: . . . . . . ?
Time to select device: 0.032 msec.
.623 Overhead: . . . . . . start time.
.624 Effective speeds: . . . 110 rows/sec if less than 9 msec elapsed between completion of punching one block and initiation of next output operation.

.63 Demands on System

Component: . . . . . . processor.
Msec/row: . . . . . . 9.1.
Percentage: . . . . . . 100 (on 160, or Normal channel of 160-A).

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . . number of tracks.
Method: . . . . tape width guide.
Comment: . . . . . . set for 5-, 7,- or 8-track tape.

.72 Other Controls

Function: . . . . tape feed.
Form: . . . . lever.

.73 Loading and Unloading

Storage: . . . . reel.
Capacity: . . . . 1,000 feet.

.732 Replenishment time: . . 2.0 to 3.0 minutes; punch needs to be stopped.

.733 Adjustment time: . . . 3.0 to 4.0 minutes.
.734 Optimum reloading period: . . . . 18.2 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock
Recording:	none.
Output block size:	not possible.
Invalid code:	not possible.
Exhausted medium:	none.
Receipt of data:	none.

INPUT-OUTPUT: 167 CARD READER

§ 073.

.1 GENERAL

.11 Identity: . . . . 167 Card Reader, Model 1.
167-1.

167 Card Reader, Model 2.
167-2.

.12 Description

The CDC 167 Card Reader reads 80-column cards by means of a photoelectric sensing head, at a maximum rate of 250 cards per minute. The reading mechanism is a Burroughs 200 card per minute mechanism, modified by Control Data to run at 250 cards per minute and enclosed in a Control Data cabinet. An infinite-tooth clutch is used so that the effective reading rate is smoothly reduced to match any system limiting factors. Because there is only one reading station, verification of the reading is a responsibility of the program. However, an automatic check of the reading amplifiers is performed for every card read. Failure of the check provides a testable signal to the processor.

Reading is accomplished serially, column-by-column, starting at column number one. Each column is transmitted to the processor as one 12-bit word. With the 167 Model 1, the reader selection External Function code initiates either a single card read or a free-run read. The Model 2 automatically translates each column from Hollerith to BCD code, and packs a pair of BCD characters into each computer word. The automatic translation may be overridden for reading binary cards in the Model 2. A command is available to stop the card reader. Only one stacker (which can hold 500 cards) is available.

The data input command can specify a block of core storage for input data, in which case data from each card column is placed automatically in sequential locations until the block is full. Alternatively, there can be a single-word transfer command for each word to be transferred. Synchronization of the data transfer is automatic, but the computer program timing must be watched so that the data is not lost by delayed execution of a data transfer command. The program can test for this potential condition (Program Error Status Code). Data from each card column is available at intervals of 1.88 milliseconds.

This reader is a relatively new unit and is offered as an economical reader that is slower than the 1610-A Control Unit with an IBM 088 Reader, which operates at 650 cards per minute. The reading mechanism is the same as that in the CDC 1617 Card Reader (refer to Report 243:074, CDC 1604-A); however, the 1617 has the facility of being manually switchable between two different computers. For example, the two systems may be the 1604/1604-A and the 160/160-A.

.13 Availability: . . . . . 4 months.

.14 First Delivery: . . . . 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . pinch rollers.
.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . none.
.222 Sensing system: . . . photoelectric.

.23 Multiple Copies: . . . none.

.24 Arrangement of Heads

Use of station: . . . . reading.
Stacks: . . . . 1.
Heads/stack: . . . . . 12.
Method of use: . . . . 1 column at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . . standard 80-column punched cards.
.312 Phenomenon: . . . . . rectangular punched holes.

.32 Positional Arrangement

.321 Serial by: . . . . . . 80 columns at standard spacing.
.322 Parallel by: . . . . . 12 rows at standard spacing.
.324 Track use: . . . . . all for data.
.325 Row use: . . . . . . all for data.

.33 Coding

	167-1	167-2
External:	column binary	Hollerith.
Internal:	card image; 1 column per word	2 BCD char per word.

.34 Format Compatibility: all devices using standard 80-column cards.

.35 Physical Dimensions: standard 80-column cards.

.4 CONTROLLER

.41 Identity: . . . . no separate controller; functions under control of processor.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . none.

§ 073.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 column (1 word input command). 1 to N cards (free run).
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . . 1 word.
.444 Input-output area lockout: . . . . . . in 160 in block input mode.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic, block mode. by program, 1-word mode.
.447 Synchronizing aids: . . status codes in reader.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . 1 card of 1 to 80 columns. 1 to N cards.
.512 Block demarcation: . . area defined by instruction addresses.

.52 Input-Output Operations

.521 Input: . . . . feed 1 card, or free run; then input 1 block.
.522 Output: . . . . none.
.523 Stepping: . . . . . . none.
.524 Skipping: . . . . . . none.
.525 Marking: . . . . . . none.
.526 Searching: . . . . . none.

.53 Code Translation: . . matched codes.

.54 Format Control: . . . none.

.55 Control Operations

Disable: . . . . no.
Request interrupt: . . no.
Offset card: . . . . . no.
Select stacker: . . . . no.
Select format: . . . . no.
Select code: . . . . . no.

.56 Testable Conditions

Disabled: . . . . yes.
Busy device: . . . . . no.
Output lock: . . . . . no.
Nearly exhausted: . . . no.
Hopper empty: . . . . yes.
Stacker full: . . . . . yes.
Ready: . . . . yes.
Feed failure: . . . . . yes.
Request for data too late: . . . . yes.
Read amplifier failure: . . . . yes.

.6 PERFORMANCE

.61 Conditions: . . . . . . see Paragraph .63.

.62 Speeds

.621 Nominal or peak speed: 250 cards/minute.
.622 Important parameters
Card cycle time: . . 240 msec.
Time till first column read: . . . . . . 70 msec.
Time between columns: . . . . . 1.88 msec.
.623 Overhead: . . . . . . none; infinite tooth clutch.
.624 Effective speeds: . . . 250 cards/minute. This can be obtained even following a single Card Read if reader is re-selected within 4 msec after column #80 is read.

.63 Demands on System

Component: . . . . . 160 processor.
Condition: . . . . . . N words per input command.
Msec per card: . . . . 240.
Percentage: . . . . . 100.

Component: . . . . . 160 processor, or 160-A processor using Normal channel.
Condition: . . . . . . 1 word per input command.
Msec per column: . . . 0.38.
Percentage: . . . . . 20.2.

Component: . . . . . 160-A processor using Buffer channel.
Condition: . . . . . . N words per input command.
Msec per column: . . . 0.02, approx.
Percentage: . . . . . 1.1.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . none.

.72 Other Controls

Function: . . . . . . disable row 12 "0" check.
Form: . . . . illuminated switch.
Comment: . . . . . . used when reading cut-corner cards.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	500 cards.
Stacker:	500 cards.

.732 Replenishment time: . 0.2 min. Device does not need to be stopped.
.733 Adjustment time: . . . no adjustments required.
.734 Optimum reloading period: . . . . 2.0 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Reading:	check or read amplifiers	generate status code.
Input area overflow:	none.	
Invalid code:	all codes valid.	
Exhausted medium:	check	generate status code.
Imperfect medium:	none.	
Timing conflicts:	check on program timing	generate status code.
Card not fed:	check	generate status code.
Motor power off:	interlock	generate status code.
Amplifier failure, feed failure, or program timing error:	check	generate disconnect code.

INPUT-OUTPUT: 170 CARD PUNCH

§ 074.

.1 GENERAL

.11 Identity: . . . . . . 170 Card Punch.

.12 Description

The CDC 170 Card Punch is a unit which combines an adapter and an IBM 523 Summary Punch. The 170 can connect to the 160/160-A, the 1604/1604-A or the 924/924-A Processors.

.12 Description (Contd.)

The IBM 523 Summary Punch can operate at 100 cards per minute at maximum speed.

.13 Availability: . . . . . 4 months.

.14 First Delivery: . . . . 1960.

INPUT-OUTPUT: CDC 1612 PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . . . High Speed Printer. CDC 1612 Unit.

.12 Description

The 1612 High Speed Printer consists of an Anelex Series 4-1000 model printer mounted on top of a 1612 Printer Control Unit. The printer system, which is designed for use as a peripheral unit for the 160 and 1604 series CDC computers, prints the computer data output on fan-fold forms at a nominal maximum rate of 1,000 lines per minute. An alternative rate of 667 lines per minute is possible and may be selected by actuating a single switch in the printer control unit. This 667 line rate is effected by reducing the speed of the print drum and, as a result, produces printing with improved vertical registration.

One print line consists of a maximum of 120 character positions; each position can print from a 64-character set. Maximum print rates are achieved when use is limited to the 48-character FORTRAN subset of the total character set and a maximum of two line feeds following each print line, otherwise speeds are reduced by a factor of two.

One to 120 words are sent to the print buffer before printing. Printing is accomplished by the usual "on-the-fly" technique. Automatic single-space paper advance follows printing, and line skipping is provided by means of a prepunched tape in the printer. Eight channels on the tape, selected by programmed instructions, control the vertical formats.

.13 Availability: . . . . . 2 to 4 months.

.14 First Delivery: . . . . 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket drive push and pull.

.212 Reservoirs: . . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . on-the-fly hammer stroke against engraved drum.

.23 Multiple Copies

.231 Maximum Number
Interleaved carbon: 5.
Card stock: . . . . 1.

.233 Types of master
Multilith: . . . . . . yes.
Spirit: . . . . yes.
Pressure sensitive: . yes.
Heat transfer: . . . . yes.

.24 Arrangement of Heads

Use of station: . . . . printing.
Stacks: . . . . 1.
Heads/stack: . . . . . 120.
Method of use: . . . . prints one line at a time.

.25 Range of Symbols

Numerals . . . . . . 10, 0 to 9.
Letters: . . . . 26, A to Z.
Special: . . . . 28, see below.
Alternatives: . . . . . upon request.
FORTRAN set: . . . . yes, see below.
Req'd COBOL set: . . . no.
Total: . . . . 64.

See Data Code Table No. 2.

Special characters in FORTRAN set	Additional characters in full set
. period	≤ less than or equal
- minus	≥ greater than or equal
+ plus	< less than
= equal	> greater than
(open parenthesis	∧ and
) close parenthesis	∨ or
/ slant	¬ not
* asterisk	→ arrow right
, comma	↑ arrow up
≠ not equal	↓ arrow down
$ dollar	≡ identity
: colon	% percent
blank	[open bracket
	] close bracket
	; semicolon

Note: For business applications ⌐ % $ replace ∧ ∨ ¬

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . continuous fanfold sprocket-punched stationery.

.312 Phenomenon: . . . . printing of engraved chars.

.32 Positional Arrangement

.321 Serial by: . . . . . . 1 line at 6 lines/inch.
.322 Parallel by: . . . . . 120 columns at 10 chars/inch.
.323 Bands: . . . . 1.
.324 Track use: . . . . . . all for data.
.325 Row use: . . . . . . all for data.

§ 081.

.33 Coding: . . . . as in Data Code Table No. 2.

.34 Format Compatibility: none.

.35 Physical Dimensions

.351 Overall width: . . . . 4 to 19 inches.
.352 Length: . . . . up to a 17-inch form.
.353 Maximum margins
Left: . . . . 3.5 inches.
Right: . . . . 3.5 inches.

.4 CONTROLLER

.41 Identity: . . . . Print Control Unit.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to 120 words.
.442 Input-output areas: . . core storage; 1 char per word, in 6 low-order bit positions.
.443 Input-output area access: . . . . . . each word.
.444 Input-output area lockout: . . . . . . yes, in 160.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 line of up to 120 characters.
.512 Block demarcation
Output: . . . . address limits in instruction.

.52 Input-Output Operations

.521 Input: . . . . status code.
.522 Output: . . . . print 1 line.
.523 Stepping: . . . . Step 0, 1, or 2 lines.
.524 Skipping: . . . . 8 format channels for skipping are available, controlled by a tape loop.
.525 Marking: . . . . none.

.53 Code Translation: . . . automatic.

.54 Format Control: . . . control of skipping using paper tape loop.

.55 Control Operations

Disable: . . . . yes.
Request interrupt: . . yes.
Select format: . . . . as in skipping.
Select code: . . . . . no.

.56 Testable Conditions

Printer ready: . . . . provided power is on, paper is not in motion, and printer is not out of paper.

.6 PERFORMANCE

.61 Conditions

I A: . . . . FORTRAN set, print drum 1,000 rpm.
I B: . . . . FORTRAN set, print drum 667 rpm.
II A: . . . . full character set, print drum 1,000 rpm.
II B: . . . . full character set, print drum 667 rpm.

.62 Speeds

.621 Nominal or peak speeds
I A: . . . . 1,000 lines/min.
II A: . . . . 500 lines/min.
I B: . . . . 667 lines/min.
II B: . . . . 333 lines/min.
.622 Important parameters
Paper speed: . . . . 25 inches/sec., max 9,000 lines/min., max.
Line length: . . . . . 120 columns.
Line spacing: . . . . 6 lines/inch.
Character spacing: . 10 chars/inch.
Drum cycle, I A & II A: . . . . 60 msec.
Drum cycle, I B & II B: . . . . 90 msec.
.623 Overhead: . . . . . . single clutch point.
.624 Effective speeds
I A: . . . . 1,000/ (1+ [(N+6)/9]) lines/min.
II A: . . . . 1,000/ (2+[N/9]) lines/min.
I B: . . . . 667/ (1+[(N+6)/9]) lines/min.
II B: . . . . 677/ (2+[N/9]) lines/min.
N: . . . . interline spacing in lines.
Note: [x] means "integer part of x."
These are shown graphically at end of the section.

.63 Demands on System: . 1 to 2 msec. per line.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method	Comment
Character phasing:	knob	performs fine adjustments of print quality to correspond to motor speed selection.
Penetration control:	knob	adjusts hammer mounting plate print cylinder gap to accommodate different thickness of paper.
Form positioning:	knob	adjusts line of print on form.
Paper tension:	knob	adjusts paper tension.
Top of form:	button	moves to top of form under control of format channel 8.
Single line feed:	button	advances paper.
Paper tractor adjustment:	adjustable form tractor	provides horizontal positioning for paper widths of 4 to 19 inches.

§ 081.

.72 Other Controls

Function	Form	Comment
Motor Speed:	switch	selects print drum speed of either 1,000 or 667 rpm.
Printer Ready:	combination button-lamp	indicates that printer is "ready."
160/1604 Selector Switch:	switch	selects the correct inputs for 1604-A or 160 computer.

.73 Loading and Unloading

.731 Volumes handled: . . . paper stack 12 to 14 inches high.

.732 Replenishment time: 1 min. printer must be stopped.

.733 Adjustment time: . . . 1 to 3 minutes.

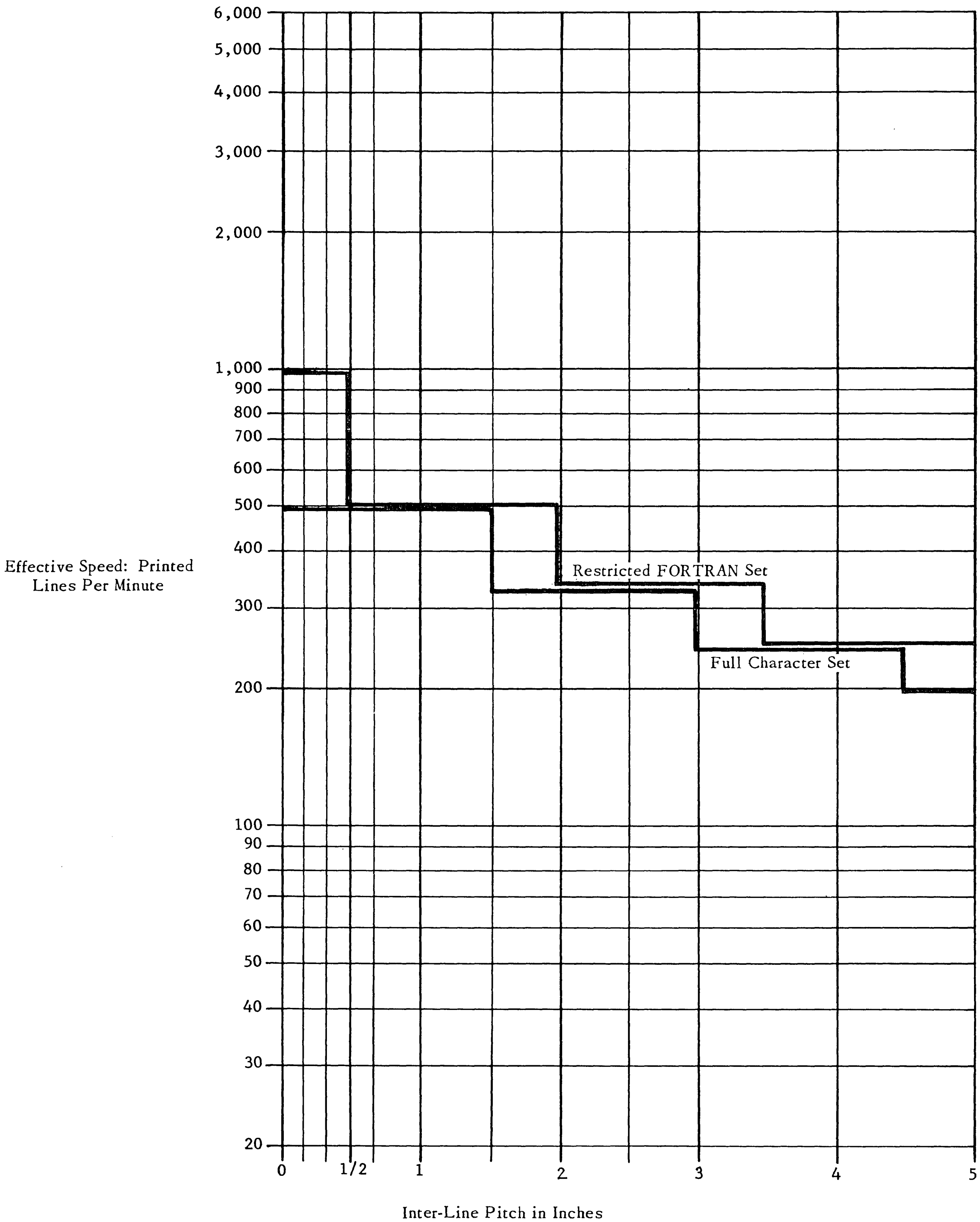
.734 Optimum reloading period: . . . . . . 34 minutes.
Basis: using 1,000 17-inch 2-part forms, printing full character set, 1 line every inch.

.8 ERRORS, CHECKS AND ACTION:

Error	Check or Interlock	Action
Recording:	none.	
Output block size:	none.	
Invalid code:	all codes valid.	
Exhausted medium:	micro-switch check	stop printer.
Imperfect medium:	micro-switch check	stop printer.

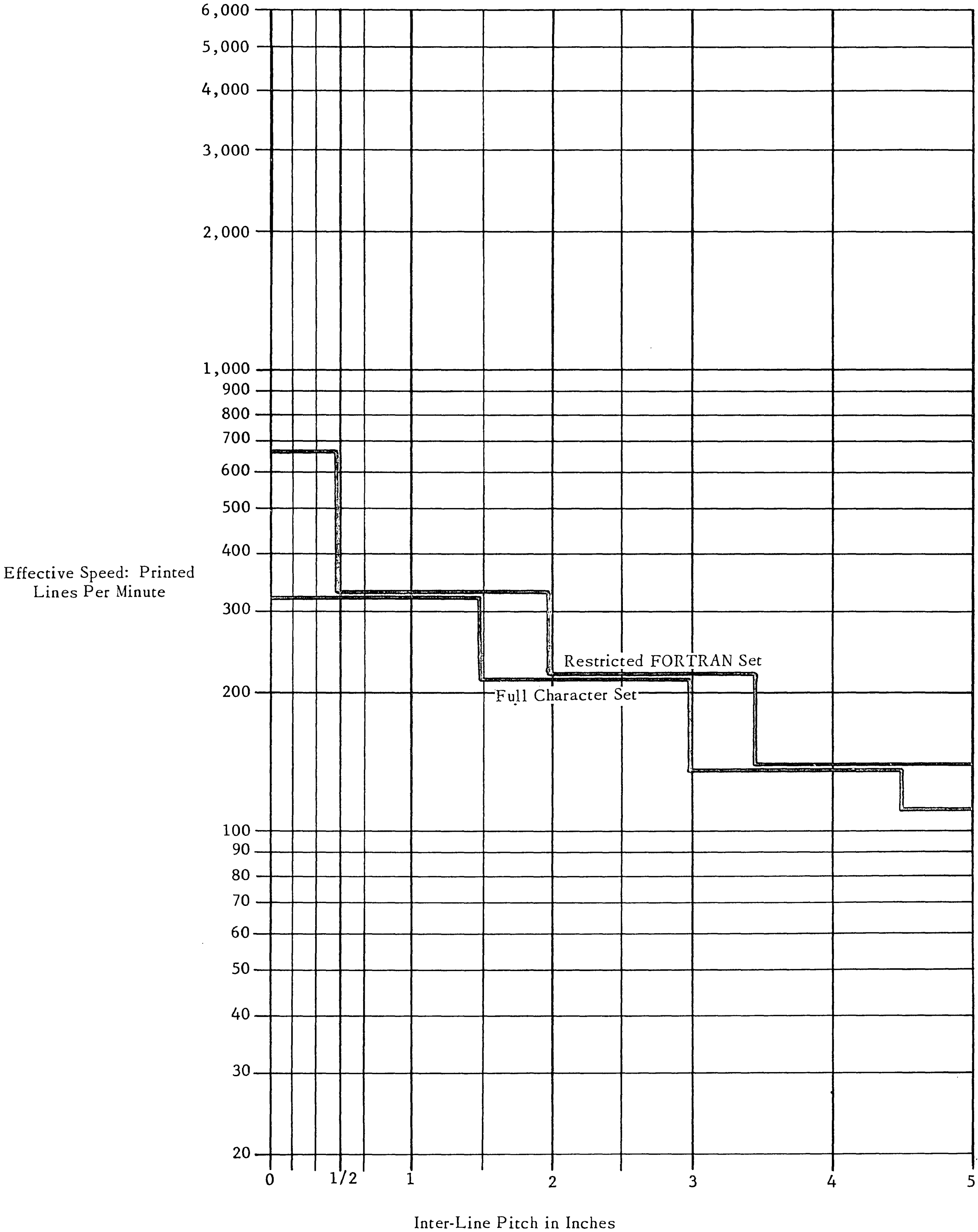
EFFECTIVE SPEED
CDC 1612 PRINTER

Condition: Print cylinder revolving at 1,000 r.p.m.



EFFECTIVE SPEED
CDC 1612 PRINTER

Condition: Print cylinder revolving at 667 r.p.m.



INPUT-OUTPUT: 166 PRINTER, MODEL 2

§ 082.

.1 GENERAL

.11 Identity: . . . . . . 166 Line Printer. Model 2.

.12 Description:

The 166 Model 2 Printer is a buffered version of the 166 Model 1 Printer. The Model 2 is now the standard printer for the CDC 160-A system. The faster 1612 Printer System can be used where faster printing is required. Data for a full line of print is transferred to the 166-2 Printer, and the processor is free to continue in its program.

The 166 Printer is a relatively new printer offered for use with the 160 and 160-A Computers. It prints alphameric data from a 64-character set in a 120-column line. The peak speed is just under 150 lines per minute when printing the entire character set. Two other print drums are easily interchangeable with this one; a 46- and a 16-character model. The 46-character set drum has the numeric field engraved twice around the circumference, and a peak numeric printing speed of 300 lines per minute is obtainable. Another variation of the print drum contains four repeated 16-character fields around the drum, and offers a peak printing speed of 600 lines per minute. The printer is made by Holley Computer Products Company.

.13 Availability: . . . . . 4 months.

.14 First Delivery: . . . . 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . sprocket drive; paper punched both sides.

.212 Reservoirs: . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . . on-the-fly hammer stroke against interchangeable engraved drum of 120 print locations.

.222 Sensing system: . . . none.

.23 Multiple Copies

.231 Maximum number
Interleaved carbon: . 1- to 6-part forms.

.233 Types of master
Multilith: . . . . . . yes.
Spirit: . . . . yes.
Pressure sensitive: . yes.
Heat transfer: . . . . yes.

.24 Arrangement of Heads

Use of station: . . . . printing.
Stacks: . . . . 1.
Heads/stack: . . . . . 120.
Method of use: . . . . one line at a time.

.25 Range of Symbols

Drum A (standard supplied)

Numerals:	10	0 to 9.
Letters:	26	A to Z.
Special:	28	see Data Code Table No. 2
Alternatives:		3 for business or scientific.
FORTRAN set: . . .		yes.
Basic COBOL set: . .		yes.
Total:	64.	

Drum B

Numerals:	10	0 to 9.
Letters:	26	A to Z.
Special:	10	. - + = ( ) / * , blank
Alternatives:		none.
FORTRAN set: . . .		yes.
Basic COBOL set: . .		no.
Total:	46.	

Drum C

Numerals:	10	0 to 9.
Letters:	none.	
Special:	6.	. - , + $ *
Alternatives:		none.
FORTRAN set: . . .		no.
Basic COBOL set: . .		no.
Total:	16, in 4 fields around drum.	

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . . continuous fanfold sprocket punched stationery, or roll paper.

.312 Phenomenon: . . . . . printing.

.32 Positional Arrangement

.321 Serial by: . . . . . . line of print at 6 lines per inch.

.322 Parallel by: . . . . . 120 print positions at 10 per inch.

.324 Track use
Data: . . . . 120 max.

.325 Row use: . . . . . . all for data.

§ 082.

.33 Coding: . . . . as in Data Code Table No. 2.

.34 Format Compatibility: none.

.35 Physical Dimensions

.351 Overall width: . . . . 12 in. to 22 in. by ? in. increments.
.352 Length: . . . . . . no limit except storage.
.353 Maximum margins: . . no restrictions; forms can be moved to print any 12-inch portion of 17 inch wide paper.

.4 CONTROLLER

.41 Identity: . . . . no separate controller; part of printer.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line:

Use	Associated equipment
Tape-to-printer: . .	603 or 163 Tape Unit.
Card reader-to-printer:	167 Card Reader.

.43 Connection to Device

.431 Devices per controller: 1.
.432 Restrictions: . . . . none.

.44 Data Transfer Control

.441 Size of load: first 60 or 62 words output from computer in 1 output operation (120 BCD char).
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . . each word.
.444 Input-output area lockout: none.
.445 Table control: . . . . none.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 60 or 62 words.
.512 Block demarcation
Output: . . . . . . addresses in instruction.

.52 Input-Output Operations

.521 Input: . . . . none.
.522 Output: . . . . output 1 block.
.523 Stepping: . . . . . . none.
.524 Skipping: . . . . . . 8-channel format tape.
.525 Marking: . . . . . . none.
.526 Searching: . . . . . . none.

.53 Code Translation: . . automatic.

.54 Format Control: . . . only as programmed.

.55 Control Operations

Disable: . . . . no.
Select format: . . . . no.
Select code: . . . . . no.
Other: . . . . select synchronous or asynchronous printing.
Status request: . . . . yes.

.56 Testable Conditions

Disabled: . . . . . . no.
Busy device: . . . . . see ready.
Output lock: . . . . . no.
Nearly exhausted: . . . no.
Hopper empty: . . . . yes.
Stacker full: . . . . . no.
Ready: . . . . yes.
Paper moving: . . . . yes.
Drum stationary: . . . yes.
Switched off-line: . . . yes.

.6 PERFORMANCE

.61 Conditions

I: . . . . 64-char drum.
II: . . . . 46-char drum.
III: . . . . 16-char drum.
IV: . . . . asynchronous.
V: . . . . synchronous.

.62 Speeds

.621 Nominal or peak speed
I: . . . . 150 lines/minute, if 4 successive char on drum ignored and used for advancing paper.
II, numeric: . . . . . 300 lines/minute.
II, alphameric: . . 150 lines/minute.
III (numeric only): . . 600 lines/minute.
.622 Important parameters
Skipping speed: . . . 5800 lines/ minute (9.67 msec/line).
Paper advance time
Single space: . . . 25 msec.
Double space: . . . 35 msec.
Drum speed: . . . . 150 rev/minute (400 msec/rev).
Time to fill buffer: . . 1 to 2 msec.
.623 Overhead: . . . . . . single-point clutch (synchronous print). infinite-point clutch (asynchronous print).
.624 Effective speeds, lines per minute.
I, IV: . . . . 142.
I, V: . . . . 150.

II, IV, alphameric: . 150.
II, IV, numeric: . . . 300.
II, V, alphameric: . . asynchronous only.
II, V, numeric: . . . asynchronous only.

III, IV: . . . . 480.
III, V: . . . . 600.

See graph at end of section.

.63 Demands on System: . 1 msec per line.

§ 082.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment	Method	Comment
Horizontal alignment:	operator	coarse and fine tractor adjustments.
Change char code disc:	operator	requires less than 1 minute.
Replace print drums:	operator	requires less than 1 minute.
Change ribbon:	operator	requires less than 2 minutes.

.72 Other Controls

Function	Form	Comment
Select off-line output:	switch	selects tape-to-printer.
Initiate off-line operation:	switch	off-line.
Step:	switch	1 line of off-line printing.
Backspace:	switch	backspace tape, off-line.

.73 Loading and Unloading

.731 Volumes handled

Storage	Capacity
Hopper:	? sets of 6-part forms.
Stacker:	? sets of 6-part forms.

.732 Replenishment time: . . 2 to 4 minutes. printer needs to be stopped, but not computer.

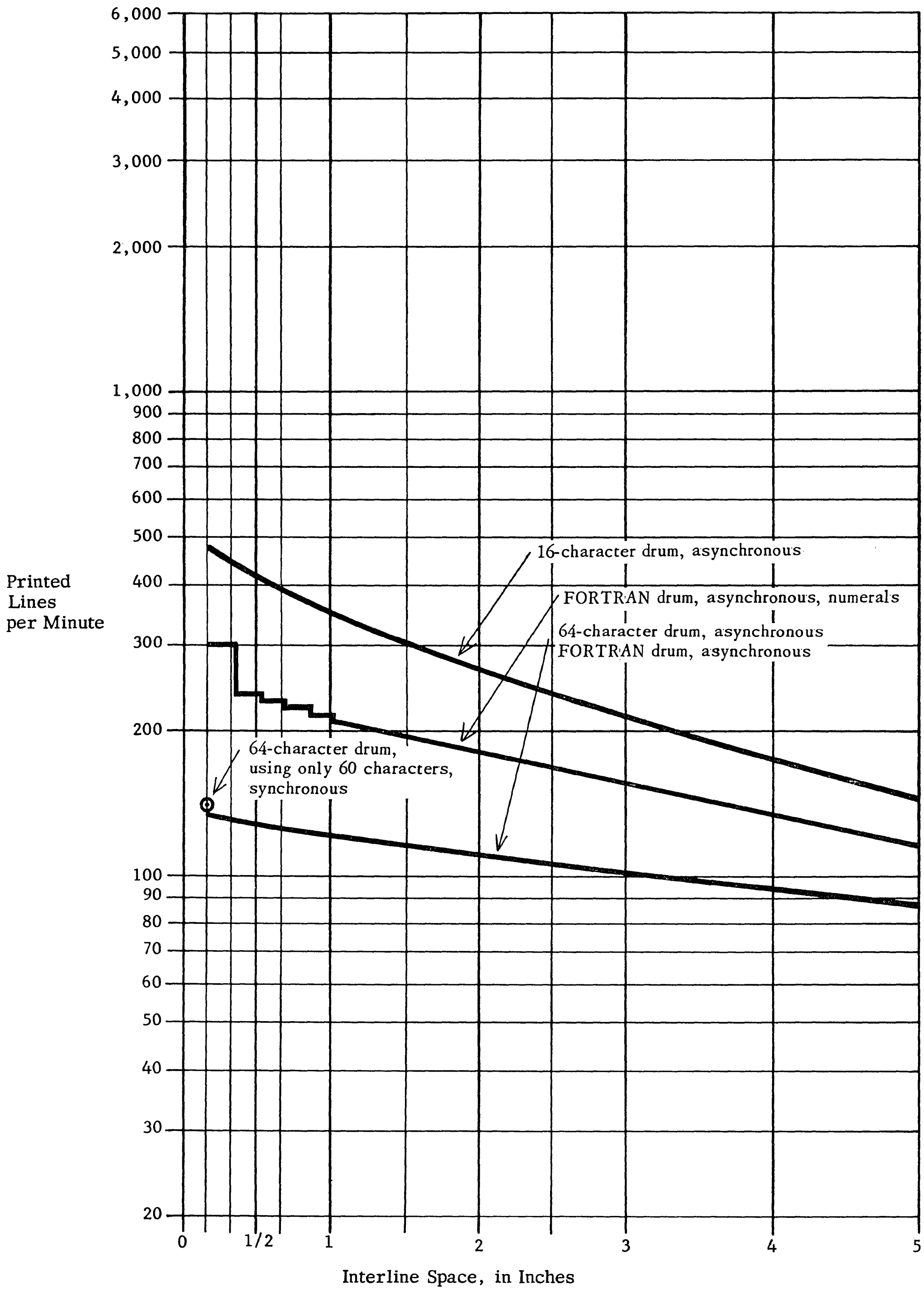
.733 Adjustment time: . . . 5 to 10 minutes.

.734 Optimum reloading period: . . . . 300 minutes. Basis: 750 single-spaced pages at 150 lines per minute.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	none.	
Output block size:	none.	
Invalid code:	none.	
Exhausted medium:	interlock	halt, program sense.
Imperfect medium:	none.	
Timing conflicts:	interlock	wait.

EFFECTIVE SPEED
CDC 166-2 PRINTER



INPUT-OUTPUT: CDC 603 MAGNETIC TAPE UNIT

§ 091.

.1 GENERAL

.11 Identity: . . . . Magnetic Tape Unit. 603.

.12 Description

The CDC Magnetic Tape Unit, which uses pneumatic capstan drive, is a new addition to the 160-A system and provides a replacement for the 163 and 164 Magnetic Tape system units. Tapes of the 163 and 164 units are recorded at low density (200 rows per inch) and can be read with the 603 unit set (by manual switch) at low density. Tape speed is 75 inches per second, resulting in data rates of 15,000 and 41,667 rows per second for recording densities of 200 and 556 rows per inch, respectively. Tapes recorded on the 603 are compatible with the IBM 729 magnetic tape units, which can operate at the above densities (IBM 729 Models II, IV, V, and VI). The 603 used a read-after-write check. Transverse and longitudinal parity are checked at the controller, and a parity error condition can be checked by the processor.

The Model 603 Tape Unit is physically identical to the CDC Model 606 Tape Unit, but has a tape speed of 75 inches per second, which provides a data rate half that of the 606. Tapes recorded by either model are compatible with the other. Detailed information about program control of the 603 is not yet available.

The 162-1 controller normally has four tape units connected to it; up to eight can be connected on special order. A feature of the 162-1 is that one tape unit can be used for tape-to-printer transcription at the same time the other tape units are available for on-line use. Alternatively, a card-to-tape transcription may proceed (using the 162-1 controller), but this operation prevents the use of the other tape units.

The 160/160-A previously used the 163 or 164 Magnetic Tape Systems, which produced IBM-compatible tape at 200 bits per inch only. A number of 160/160-A systems will still use these tape systems. CDC systems also used the Model 1608 Control Unit and IBM 729 II or IV Tape Units; this controller is now supplied only if available.

.13 Availability: . . . . . . 4 to 6 months.

.14 First Delivery: . . . . early 1963.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pneumatic capstan.

.212 Reservoirs
- Number: . . . . 2.
- Form: . . . . vacuum.
- Capacity: . . . . each about 7 feet.

.213 Feed drive: . . . . . . motor.

.214 Take-up drive: . . . . . motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.

.222 Sensing system: . . . . magnetic head.

.223 Common system: . . . two heads.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

- Use of station: . . . . . erase.
- Stacks: . . . . 1.

- Use of station: . . . . . recording.
- Distance: . . . . 0.4375 inch from erase head.
- Stacks: . . . . 1.
- Heads/stack: . . . . . . 7.
- Method of use: . . . . . 1 row at a time.

- Use of station: . . . . . sensing.
- Distance: . . . . 0.3 inch from recording head.
- Stacks: . . . . 1.
- Heads/stack: . . . . . . 7.
- Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . plastic tape with magnetizable surface.

.312 Phenomenon: . . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . 1 to N rows at 200 or 556 rows/inch.

.322 Parallel by: . . . . . . 7 tracks.

.324 Track use
- Data: . . . . 6.
- Redundancy check: . . 1.
- Timing: . . . . 0 (self-clocking).
- Control signals: . . . 0.
- Unused: . . . . 0.
- Total: . . . . 7.

.325 Row use
- Data: . . . . 1 to N.
- Redundancy check: . . 1.
- Timing: . . . . 0.
- Control signals: . . . 0 (record and segment marks are optional).
- Unused: . . . . 0.
- Cap: . . . . 0.75-inch inter-block gap. 6.0-inch end-of-file mark.

§ 091.

.33 Coding: . . . . BCD mode; one tape row per character as in Data Code Table No. 3, even parity.

.34 Format Compatibility: . IBM BCD and binary codes at 200 and 556 rows per inch.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.50 inch.
.352 Length: . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . Control Unit 162-1.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line: . . . . one of the tape units can operate in an off-line mode with the printer while the other tapes are used on-line. A tape unit can be used in a card-to-tape off-line conversion, but this prevents use of the other tapes connected on-line to the 162-1.

.43 Connection to Device: . up to 4 per 162-1; up to 8 by special order.

.44 Data Transfer Control

.441 Size of load: . . . . . . 1 to N words, limited by available core storage.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . each word.
.444 Input-output area lockout: . . . . yes, in 160.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 to N words, limited by available core storage; 1 or 2 rows per word, selected by program.
.512 Block demarcation
Input: . . . . gap on tape or cut-off specified in instruction address.
Output: . . . . cut-off specified in instruction address.

.52 Input-Output Operations

.521 Input: . . . . 1 block forward.
.522 Output: . . . . 1 block forward.
.523 Stepping: . . . . backspace 1 record.
.524 Skipping: . . . . forward or backward to end-of-file mark.
.525 Marking: . . . . end-of-file mark, preceded by an automatic six-inch gap, followed by a longitudinal parity character and the regular interblock gap.
.526 Searching: . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . . none.

.55 Control Operations

Disable: . . . . by rewind and unload.
Request interrupt: . . . no.
Select format: . . . . . write 1 or 2 rows per word.
Select code: . . . . . . odd/even parity.
Rewind: . . . . yes.
Unload: . . . . yes.
Request status: . . . . yes.

.56 Testable Conditions

Disabled: . . . . yes.
Output lock: . . . . . . no.
Nearly exhausted: . . . no.
Busy controller: . . . . ?
End-of-file mark: . . . yes.
End-of-medium marks: yes.
Odd or even parity selected: . . . . yes.
Transverse or longitudinal parity error: . yes.

.6 PERFORMANCE

.61 Conditions

I: . . . . high density (556 char/in.).
II: . . . . low density (200 char/in.).
III: . . . . unit on Buffer channel.
IV: . . . . unit on Normal channel.

.62 Speeds

	Condition	I	II
.621	Nominal or peak speeds:	41,667	15,000.
.622	Important parameters		
	Name		
	Tape speed:	75 ips	75 ips.
	Density:	556 char/in.	200 char/in.
	Start or stop time:	4 to 8 msec (*)	4 to 8 msec (*)
	Full rewind time:	1.3 min.	1.3 min.
	Interblock gap:	0.75 in.	0.75 in.
.623	Overhead:	16 msec/block (***)	16 msec/block (***)
.624	Effective speed, characters/sec:	41,667N(N+698)	15,000N/(N+240).

(See Graph)
(*) Estimate. See 1:010.400.
(***) Estimate. See 1:010.400.

§ 091.

.63 Demands on System

Component	Condition	msec per char	or Percentage
160 Processor:	I	0.024	100.
160 Processor:	II	0.0667	100.
160-A Core Storage:	I, III	0.0192	80.
160-A Core Storage:	II, III	0.0192	29.
160-A Processor:	I or II; IV	0.024 or 0.0667	100.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . . recording density.
Method: . . . . switch.
Comment: . . . . select high or low density.

.72 Other Controls

Function	Form	Comment
Unit Number Selector:	dial	digit 1 to 4.
File protection ring:	plastic ring affixed to tape reel	absence of ring inhibits tape writing.
Load Point:	button	lowers tape into reservoirs and winds tape forward to load point.
Unload:	button	removes tape from reservoirs and raises upper portion of head assembly.

.73 Loading and Unloading

.731 Volumes handled
Storage: . . . . reel.
Capacity: . . . . 2,400 feet.
5,000,000 char for 1,000 char blocks at low density.
11,300,000 char for 1,000 char blocks at high density.

.732 Replenishment time: . . 1.0 to 1.5 minutes.

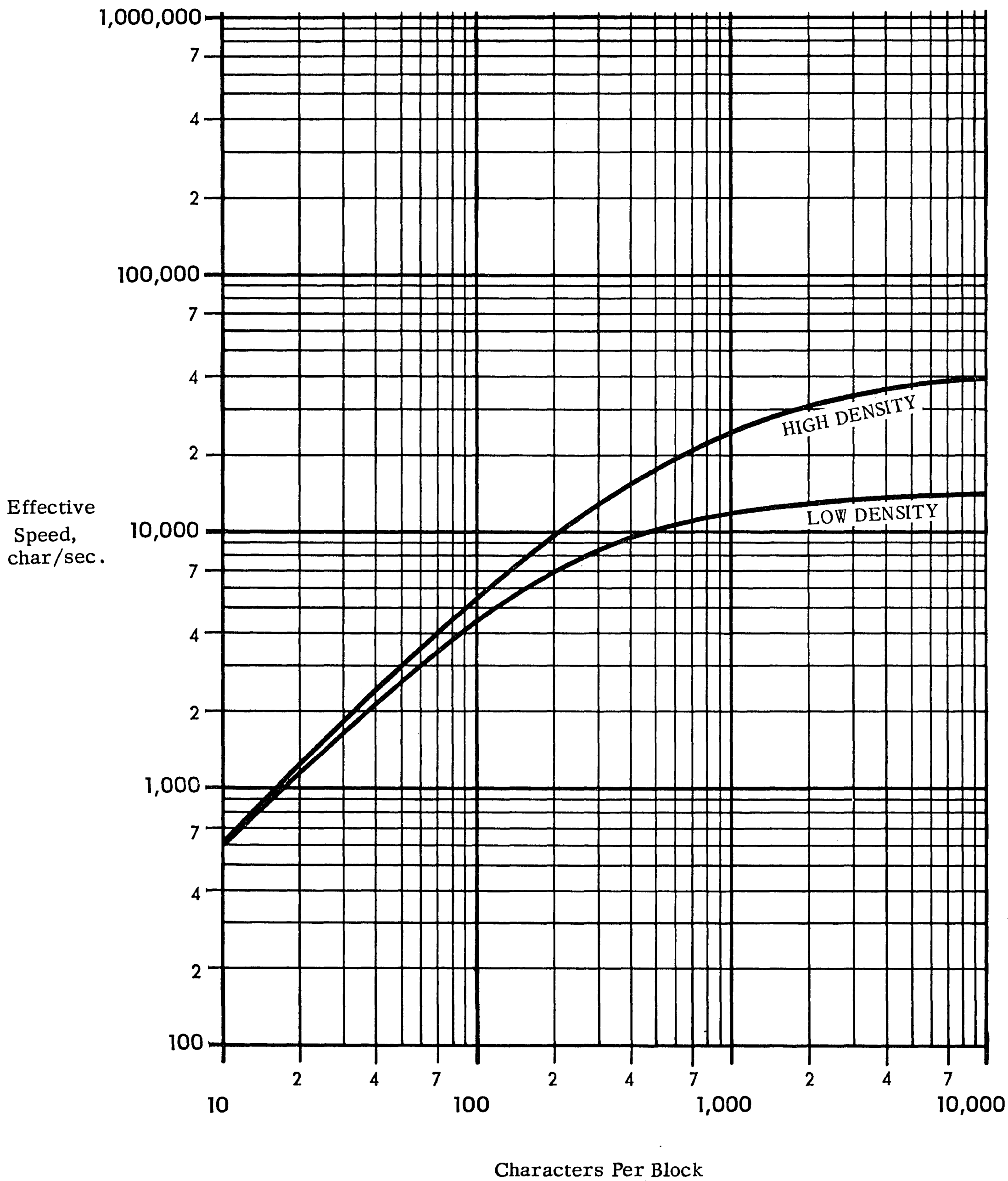
.734 Optimum reloading period: . . . . 4 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read after write	program source.
Reading:	lateral and longitudinal parity checks.	program source.
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	?	?
Exhausted medium:	interlock	program source.
Imperfect medium:	recording check.	
Timing conflicts:	?	?
Parity error:	check in controller	program source.
Transmitting data:	include parity bits.	

§ 091.

EFFECTIVE SPEED
CDC 603 MAGNETIC TAPE UNIT



INPUT-OUTPUT: CDC 606 MAGNETIC TAPE UNIT

§ 092.

.1 GENERAL

.11 Identity: . . . . Magnetic Tape Unit. CDC 606.

.12 Description

The CDC 606 Magnetic Tape Unit, which uses pneumatic capstan drive, is a new addition to the 160/160-A system and provides a replacement for the 163 and 164 Magnetic Tape system units. Tapes of the 163 and 164 units are recorded at low density (200 rows per inch), and can be read with the 606 unit set at low density. Data rates of the 606 are 30,000 and 83,400 characters per second for recording densities of 200 and 556 rows per inch, respectively. Tapes recorded on the 606 are compatible with the IBM 729 magnetic tape units, which can operate at the above densities (IBM 729 Models II, IV, V, and VI). The 606 uses a read-after-write check. Transverse and longitudinal parity are checked at the controller, and a parity error condition can be checked by the processor. Reading and writing can be performed only in a forward direction; searching for EOT, end of record, file mark; and rewinding can be performed in either direction. The maximum rewind time for a 2,400-foot tape is 80 seconds.

The Model 606 Tape Unit is physically identical to the CDC Model 603 Tape Unit, but has a tape speed of 150 inches per second, which provides a data rate twice that of the 603. Tapes recorded by either model are compatible with the other.

Data is transferred as either one or two characters per computer word, and selection is under program control. High density recording is not allowed with one character per word format, as the data rate would be high enough (one word every 12 microseconds) to cause loss of data. During high density operation (one word every 24 microseconds), when running properly, this tape transfer should be the only transfer occurring in the system, to avoid loss of data. A tape transfer using the Auxiliary Memory Unit (Model 169) is independent and usable for a simultaneous transfer if the computer does not use the 169 storage during the transfer.

The 162-2 controller normally has eight tape units connected to it. A feature of the 162-2 is that one tape unit can be used for tape-to-printer transcription at the same time the other tape units are available for on-line use. However, a card-to-tape transcription using the 162-2 controller prevents the use of the other tape units.

The CDC 606 Magnetic Tape Unit, when controlled by the CDC 1615 Control Unit, forms a magnetic tape system which can be connected to one or two computers. If connected to two computers, such as a CDC 1604-A and a CDC 160-A, control can be switched from one computer to the other either manually or by program.

The 160/160-A Computer previously used the 163 or 164 Magnetic Tape Systems, which produced IBM-compatible tape at 200 bits per inch only. A number of 160/160-A systems will still use these tape systems. CDC 160/160-A systems also used the Model 1608 Control Unit and IBM 729 II or IV Tape Units; however, this controller is now supplied only if available.

.13 Availability: . . . . . . 2 to 4 months.

.14 First Delivery: . . . . August, 1962.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pneumatic capstan.
.212 Reservoirs
Number: . . . . 2.
Form: . . . . vacuum.
Capacity: . . . . each about 7 feet.
.213 Feed drive: . . . . . . motor.
.214 Take-up drive: . . . . . motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.
.222 Sensing system: . . . . magnetic head.
.223 Common system: . . . two heads.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . 1.

Use of station: . . . . . recording.
Distance: . . . . 0.4375 inch from erase head.
Stacks: . . . . 1.
Heads/stack: . . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . sensing.
Distance: . . . . 0.3 inch from record head.
Stacks: . . . . 1.
Heads/stack: . . . . . . 7.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . plastic tape with magnetizable surface.

§ 092.

.312 Phenomenon: . . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . 1 to N rows at 200 or 556 rows/inch.
.322 Parallel by: . . . . . . 7 tracks.
.324 Track use
- Data: . . . . 6.
- Redundancy check: . . 1.
- Timing: . . . . 0 (self clocking).
- Control signals: . . . 0.
- Unused: . . . . 0.
- Total: . . . . 7.

.325 Row use
- Data: . . . . 1 to N.
- Redundancy check: . . 1.
- Timing: . . . . 0.
- Control signals: . . . 0 (record and segment marks are optional).
- Unused: . . . . 0.
- Gap: . . . . 0.75-inch inter-block gap. 6.0-inch end-of-file mark.

.33 Coding: . . . . as in Data Code Table No. 3 for BCD mode. also binary mode.

.34 Format Compatibility: . IBM BCD and binary codes at 200 and 556 rows per inch.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.50 inch.
.352 Length: . . . . 2,400 feet per reel.

.4 CONTROLLER

.41 Identity: . . . . 162-2 Control Unit, used only with 160/160-A. Also 1615 Control Unit can be used, usually for CDC 1604-A. 1615 can be switched manually or by program between 1604-A and 160/160-A computers.

.421 On-line: . . . . 1.
.422 Off-line: . . . . none.

.43 Connection to Device: . up to 8 per 162-2 or 1615. 1 tape unit using the 162-2 can be operating in a tape to printer mode while the 7 others are available to the computer.

.44 Data Transfer Control

.441 Size of load: . . . . . . 1 to N words, limited by available core storage.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . each word.
.444 Input-output area lockout: . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 to N words, limited by available core storage; 1 or 2 tape char per word, selected by program.
.512 Block demarcation
- Input: . . . . gap on tape or instruction address.
- Output: . . . . instruction address.

.52 Input-Output Operations

.521 Input: . . . . 1 block forward, with cut-off available at N words.
.522 Output: . . . . 1 block forward of N words.
.523 Stepping: . . . . 1 block forward. 1 block backward. erase 3.5 inches forward (to skip defective tape areas).
.524 Skipping: . . . . to end of file mark in either direction.
.525 Marking: . . . . end-of-file mark, preceded by an automatic 6-inch gap, followed by a longitudinal parity character and the regular interblock gap.
.526 Searching: . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . . none.

.55 Control Operations

- Disable: . . . . by rewind and unload.
- Request interrupt: . . . no.
- Select format: . . . . . write 1 or 2 rows per word.
- Select code: . . . . . . odd/even parity.
- Rewind: . . . . yes.
- Unload: . . . . yes.
- Request status: . . . . yes.

.56 Testable Conditions

- Disabled: . . . . yes.
- Output lock: . . . . . . no.
- Nearly exhausted: . . . no.
- Busy controller: . . . . ?
- End-of-file mark: . . . yes.
- End-of-medium mark: . yes.
- Odd or even parity selected: . . . . yes.
- Transverse or longitudinal parity error: . . yes.

.6 PERFORMANCE

.61 Conditions

- I: . . . . high density; 556 char/inch.
- II: . . . . low density; 200 char/inch.
- III: . . . . 1 char per computer word.
- IV: . . . . 2 char per computer word.

§ 092.

.62 Speeds

.621 Nominal or peak speeds

High density: . . . . . 83,400 char per second.
Low density: . . . . . 30,000 char per second.

.622 Important parameters

	High density	Low density
Density:	556 char/in.	200 char/in.
Time between char: .	12 μs, avg.	33 μs, avg.
Tape speed:	150 in/sec	150 in/sec.
Start time; msec: . .	3.0	3.0.
Stop time; msec: . . .	2.7	2.7.
Time from tape select till start recording; msec:	3.3	3.3.
Time from tape select till start reading; msec:	5.3	5.3.
Full rewind time: . .	1.3 minutes	1.3 minutes.
Interblock gap:	0.75 inch	0.75 inch.

.623 Overhead: . . . . 8 msec/block 8 msec/block.

.624 Effective speed, char/sec

High density: . . . . . 83,400N/(N + 698).
Low density: . . . . . 30,000N/(N + 240).
(see graph at end of this section)

.63 Demands on System

Component	Condition	Msec per block	Percentage
160 Processor:	I	4.0 + 0.012C	100.
	II	4.0 + 0.033C	100.
160-A Core Storage:	I, III	not an allowable condition.	
	I, IV	0.010C, max.	83, max.
	II, III	0.020C, max.	60, max.
	II, IV	0.010C, max.	30, max.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . . recording density.
Method: . . . . switch.
Comment: . . . . selects high or low density, but can be overridden by program changes.

.72 Other Controls

Function	Form	Comment
Unit Number Selector:	dial	select 1 of 8 addresses.
File protection ring:	plastic ring affixed to tape reel	absence of ring inhibits tape writing.
Load Point:	button	lowers tape into reservoirs and winds tape forward to load point.
Unload:	button	removes tape from reservoirs.

.73 Loading and Unloading

.731 Volumes handled

Storage: . . . . reel.
Capacity: . . . . 2,400 feet; for 1,000 char blocks, 5,000,000 at 200 char/inch; 11,300,000 chars at 556 char/inch.

.732 Replenishment time: . . 1.0 to 1.5 minutes.

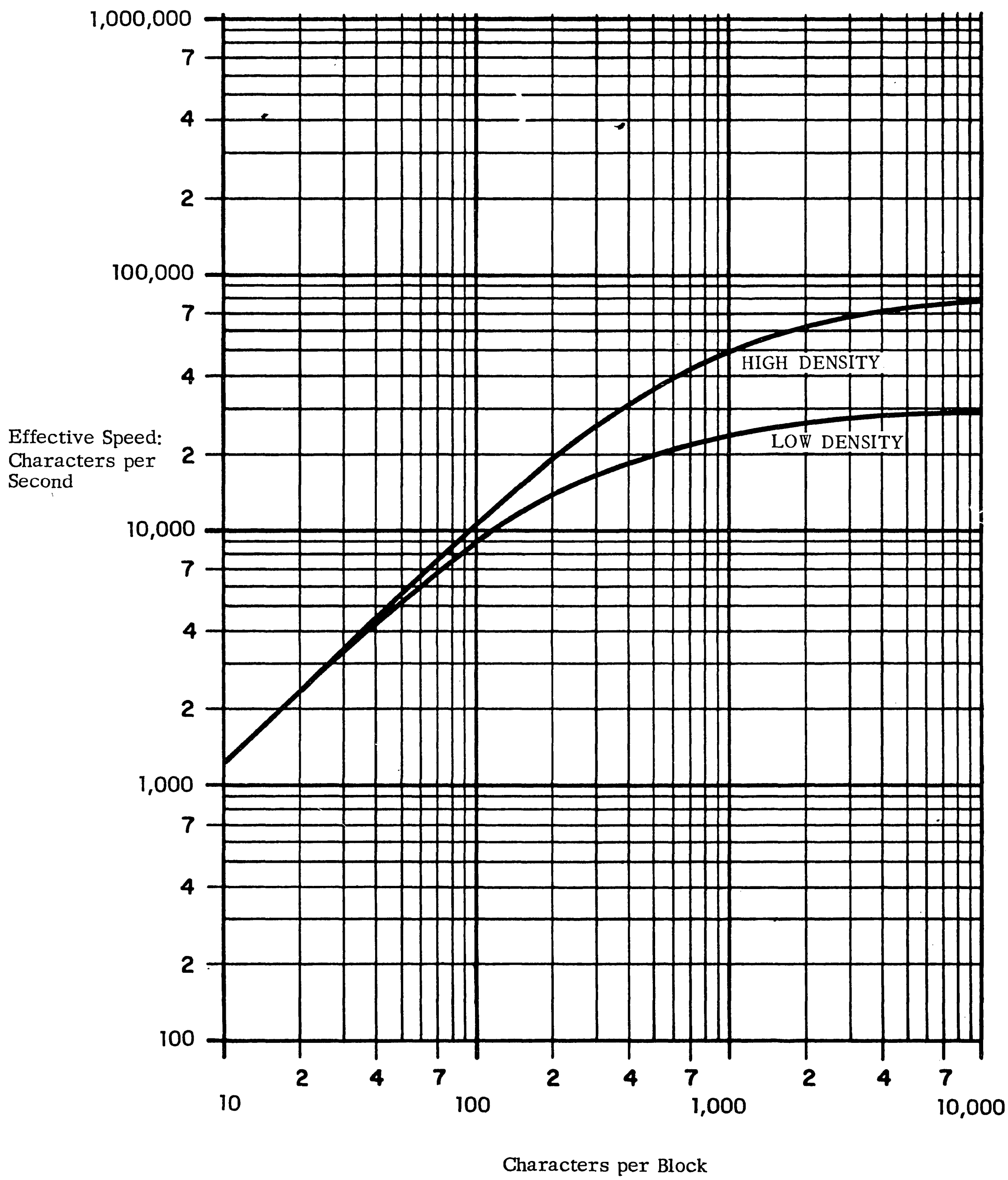
.734 Optimum reloading period: . . . . 4 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read after write with lateral parity check	indicator, alarm and program sense.
Reading:	lateral and longitudinal parity checks	indicator, alarm and program sense.
Input area overflow:	none.	
Output block size:	none.	
Invalid code:	all codes accepted.	
Exhausted medium:	reflective spot on tape	halts tape; programmed sense.
Imperfect medium:	none.	
Timing conflict:	none.	
Parity error:	check in controller available to program	depends on program.

§ 092.

EFFECTIVE SPEED
CDC 606 MAGNETIC TAPE UNIT



INPUT-OUTPUT: 161 TYPEWRITER

§ 101.

.1 GENERAL

.11 Identity: . . . . Typewriter.
161.

.12 Description

The 161 Typewriter is a modified IBM electric typewriter which is mounted on a stand, separate from the processor. Upper and lower case shift codes are provided, and both cases can be printed. The typewriter is not usable off-line, but can be connected to either the Normal or the Buffer channel of the 160-A.

The 161 either types output data or receives input data, performing both operations under program control. Input provides by-product hard copy. Input is terminated by carriage return, manual keying by the operator, or upon filling a specified core storage area. Output carriage returns must be programmed.

Several status conditions of the typewriter may be sensed (see Paragraph .56). No parity checking is performed on data transfers, and invalid codes are not detected.

.13 Availability: . . . . . 4 months.

.14 First Delivery: . . . . 1960.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . friction drive.
.212 Reservoirs: . . . . none.

.22 Sensing and Recording Systems

.221 Recording system: . . engraved hammers.
.222 Sensing system: . . . typewriter keyboard for manual input.
.223 Common system: . . . no.

.23 Multiple Copies

.231 Maximum number
Interleaved carbon: . . depends on stationery.
.233 Types of master
Multilith: . . . . yes.
Spirit: . . . . yes.

.24 Arrangement of Heads

Use of station: . . . . printing.
Stacks: . . . . 1.
Heads/stack: . . . . . 1.
Method of use: . . . . 1 character at a time.

Use of station: . . . . keyboard input.
Stacks: . . . . 1.
Heads/stack: . . . . . 44 keys.
Method of use: . . . . 1 character at a time.

.25 Range of Symbols

Numerals: . . . . . . 10 0 - 9.
Letters: . . . . 52 A - Z (U.C. & L.C.).
Special: . . . . 26.
Alternatives: . . . . none.
FORTRAN set: . . . . yes.
Req. COBOL set: . . . no.
Total: . . . . 88, plus 6 control codes not used as data.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . . . continuous fanfold stationery.
.312 Phenomenon: . . . . . printing.

.32 Positional Arrangement

.321 Serial by: . . . . . . character at 10 per inch.
.324 Track use
Data: . . . . 85 print positions.
.325 Row use: . . . . . . all for data.

.33 Coding: . . . . as in Data Code Table No. 5.

.34 Format Compatibility: . . . . none.

.35 Physical Dimensions

.351 Overall width: . . . . 8.5 inches.
.352 Length: . . . . no limit.
.353 Maximum margins: . . no limits.

.4 CONTROLLER

.41 Identity: . . . . part of 160/160-A Processor.

.42 Connection to System

.421 On-line: . . . . 1.
.422 Off-line: . . . . not usable off-line.

.43 Connection to Device

.431 Devices per controller: . . . . . . 2.
.432 Restrictions: . . . . none.

.44 Data Transfer Control

.441 Size of load: . . . . . under program control; no limit.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . . . each word.
.444 Input-output area lockout: . . . . . . yes, in 160.

§ 101.

.445 Table control: . . . . no.
.446 Synchronization: . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . same as load size; see .441 above.

.512 Block demarcation: . . . . address set by instruction.

.52 Input-Output Operations

.521 Input: . . . . input 1 block into core storage.
.522 Output: . . . . output 1 block from core storage.
.523 Stepping: . . . . . . step 1 or 2 lines at end of printed line; set by operator.
.524 Skipping: . . . . . . none.
.525 Marking: . . . . . . none.
.526 Searching: . . . . . . none.

.53 Code Translation: . . automatic.

.54 Format Control: . . . set by program.

.55 Control Operations: . . none.

.56 Testable Conditions: . . . . typewriter ready.
typewriter power off.
typewriter not in computer status.
input character ready.
character being typed.

.6 PERFORMANCE

.61 Conditions: . . . . . none.

.62 Speeds

.621 Nominal or peak speed: . . . . 10 char/sec for output; manual typing speed for input.

.624 Effective speeds: . . same as peak speeds, less allowance for carriage returns.

.63 Demands on System

Component: . . . . . processor.
Msec/char: . . . . . 100, approx.
Percentage
160 Processor: . . . 100.
160-A Processor: . . 100, on Normal channel.
0.01, on Buffer channel.

.7 EXTERNAL FACILITIES

.71 Adjustments: . . . . typical typewriter adjustments.

.72 Other Controls

Function	Form	Comment
Places unit under computer control	switch	includes momentary Clear position.
Provides termination signal after input operation	switch	terminates in 3 ways: after next carriage return. immediately. only as programmed (by storage address).

.73 Loading and Unloading

.731 Volumes handled: . . . depends on feed facilities.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Parity:	none.	
Reading:	none.	
Input area overflow:	check on last word address	?
Output block size:	any size possible.	
Invalid code:	none.	
Exhausted medium:	none.	
Imperfect medium:	none.	
Timing conflict:	interlock	wait.
Dispatch of data:	attach parity bit.	

INPUT-OUTPUT: 1610-A CONTROL UNIT

§ 102.

.1 GENERAL

.11 Identity: . . . . Control Unit. 1610-A.

.12 Description

The CDC 1610-A Control Unit can connect a group of IBM peripheral units to either the CDC 1604, 1604-A, 160, or 160-A computers. In the case where a 1604 or 1604-A is operating in conjunction with a CDC 160 or 160-A, the CDC 1610-A and its associated units can be switched manually, but not by program, from one computer to the other.

In the input mode the 1610-A can operate either one of the following:

- IBM 088 High Speed Collator, used as a card reader. Either one or both independent card feeds can each operate at 650 cards per minute; or one feed utilizing a second read station can operate at 650 cards per minute. The latter is the usual mode of operation.
- IBM 533 Card Read Punch, used as a card reader at 200 cards per minute.

.12 Description (Contd.)

In the output mode it can operate any one of the following:

- IBM 533 Card Read Punch, used as a card punch at 100 cards per minute.
- IBM 407 Accounting Machine, used as a line printer at 150 lines per minute.
- IBM 523 Gang Summary Punch, used as a card punch at 100 cards per minute.

The printer, either punch, and either card reader can be physically connected at one time, and each may be separately addressed. The IBM 088 and 407 units may be used in their normal off-line manner. No gang or summary punching is available with either the 523 or 533. On-line control of the 088, 407 and 523 by the computer requires modification of the control panels so that each unit is wired in the CALCULATE ON state (the 533 is wired directly and has no provision for control panel modifications).

.13 Availability: . . . . . . 2 months.

.14 First Delivery: . . . . . 1961.

SIMULTANEOUS OPERATIONS

§ 111.

.1 SPECIAL UNITS

.11 Identity: . . . . 168 Arithmetic Unit, Model 1 (fixed point).
168 Arithmetic Unit, Model 2.
169 Auxilary Memory Unit with its own buffer channel.

.12 Description

The basic 160-A system is capable of simultaneous operations, using the Buffer channel for a data transfer and the processor for either program execution or data transfer on the Normal channel. The Buffer operation must be initiated before the processor can proceed.

The 166-2 Buffered Line Printer provides simultaneous printing facilities. The 168-1 and 168-2 Arithmetic Units provide independent computation facilities. Very little free time is available with the 168-1 except during multiply-divide operations. Virtually no time is available for processing when using the 168-2 Arithmetic Unit, because the processor is processing exponent values while the Model 168-2 unit is doing arithmetic.

A completely independent channel exists for transferring a block of data using the 169 Auxiliary Memory Unit (core storage).

.2 CONFIGURATION CONDITIONS

I: . . . . without 169 Auxiliary Memory Unit.
II: . . . . with 169 Auxiliary Memory Unit.

.3 CLASSES OF OPERATIONS

A: . . . . input or output on Normal Channel (cards, magnetic tape, paper tape).
B: . . . . input or output on buffered channel (cards, magnetic tape).
C: . . . . print a line.
Pl: . . . . compute, or compute while doing floating point operations using subroutines and 168.2.
P2: . . . . process fixed point operands in 168-1.

.4 RULES

(Note that the time required to do one p2 operation is much shorter than input-output times.)

Condition I

a + b + c + pl + p2	= at most 4.
a + pl	= 1.
b	= at most 1.
c	= at most 1.
p2	= at most 1.

Condition II

a + b + c + pl + p2	= at most 5.
a + pl	= 1.
b	= at most 2.
c	= at most 1.
p2	= at most 1.

INSTRUCTION LIST

INSTRUCTION				OPERATION
F	E	G	Mnemonic Opcode	
				Arithmetic
01	12		MUT	10 (A) ⟶ A.
01	13		MUH	100 (A) ⟶ A.
06	ee		ADN	(A) + E ⟶ A.
30	ee		ADD	(A) + (E) ⟶ A.
31	00	YYYY	ADM	(A) + (m) ⟶ A. m = YYYY.
31	ee		ADI	(A) + ((E)) ⟶ A.
32	00	XXXX	ADC	(A) + G ⟶ A.
32	ee		ADF	(A) + (P + E) ⟶ A. P = present contents of instruction counter.
33	00		ADS	(A) + ((0)7777) ⟶ A.
33	ee		ADB	(A) + (P - E) ⟶ A.
07	ee		SBN	(A) - E ⟶ A.
34	ee		SBD	(A) - (E) ⟶ A.
35	00	YYYY	SBM	(A) - (m) ⟶ A.
35	ee		SBI	(A) - ((E)) ⟶ A.
36	00	XXXX	SBC	(A) - G ⟶ A.
36	ee		SBF	(A) - (P + E) ⟶ A.
37	00		SBS	(A) - ((0)7777) ⟶ A.
37	ee		SBB	(A) - (P - E) ⟶ A.
50	ee		RAD	(A) + (E) ⟶ A; then (A) ⟶ E.
51	00	YYYY	RAM	(A) + (m) ⟶ A; then (A) ⟶ m.
51	ee		RAI	(A) + ((E)) ⟶ A; then (A) ⟶ (E).
52	00	XXXX	RAC	(A) + G ⟶ A; then (A) ⟶ G.
52	ee		RAF	(A) + (P + E) ⟶ A; then (A) ⟶ P + E.
53	00		RAS	(A) + ((0)7777) ⟶ A; then (A) ⟶ (0)7777.
53	ee		RAB	(A) + (P - E) ⟶ A; then (A) ⟶ P - E.
54	ee		AOD	(E) + 1 ⟶ A; then (A) ⟶ E.
55	00	YYYY	AOM	(m) + 1 ⟶ A; then (A) ⟶ m.
55	ee		AOI	((E)) + 1 ⟶ A; then (A) ⟶ (E).
56	00	XXXX	AOC	G + 1 ⟶ A; then (A) ⟶ G.
56	ee		AOF	(P + E) + 1 ⟶ A; then (A) ⟶ P + E.
57	00		AOS	((0)7777) + 1 ⟶ A; then (A) ⟶ (0)7777
57	ee		AOB	(P - E) + 1 ⟶ A; then (A) ⟶ P - E.
				Logic
02	ee		LPN	(A) "LOGICAL AND" E ⟶ A.
10	ee		LPD	(A) "LOGICAL AND" (E) ⟶ A.
11	00	YYYY	LPM	(A) "LOGICAL AND" (m) ⟶ A.
11	ee		LPI	(A) "LOGICAL AND" ((E)) ⟶ A.
12	00	XXXX	LPC	(A) "LOGICAL AND" G ⟶ A.
12	ee		LPF	(A) "LOGICAL AND" (P + E) ⟶ A.
13	00		LPS	(A) "LOGICAL AND" ((0)7777) ⟶ A.
13	ee		LPB	(A) "LOGICAL AND" (P - E) ⟶ A.
03	ee		SCN	(A) "EXCLUSIVE OR" E ⟶ A.
14	ee		SCD	(A) "EXCLUSIVE OR" (E) ⟶ A.
15	00	YYYY	SCM	(A) "EXCLUSIVE OR" (m) ⟶ A.
15	ee		SCI	(A) "EXCLUSIVE OR" ((E)) ⟶ A.
16	00	XXXX	SCC	(A) "EXCLUSIVE OR" G ⟶ A.
16	ee		SCF	(A) "EXCLUSIVE OR" (P + E) ⟶ A.
17	00		SCS	(A) "EXCLUSIVE OR" ((0)7777) ⟶ A.
17	ee		SCB	(A) "EXCLUSIVE OR" (P - E) ⟶ A.
60	ee		ZJF	(P) + E ⟶ P if (A) = 0000; otherwise continue.

§ 121. INSTRUCTION LIST (Contd.)

INSTRUCTION				OPERATION
F	E	G	Mnemonic Opcode	
				Logic (Contd.)
61	ee		NZF	(P) + E → P if (A) ≠ 0000; otherwise continue.
62	ee		PJF	(P) + E → P if (A) > 0; otherwise continue.
63	ee		NJF	(P) + E → P if (A) < 0; otherwise continue.
64	ee		ZJB	(P) - E → P if (A) = 0000; otherwise continue.
65	ee		NZB	(P) - E → P if (A) ≠ 0000; otherwise continue.
66	ee		PJB	(P) - E → P if (A) > 0; otherwise continue.
67	ee		NJB	(P) - E → P if (A) < 0; otherwise continue.
70	ee		JPI	(E) → P.
71	00	YYYY	JPR	(P) + 2 → (r)m. M + 1 → P.
71	ee		JFI	((P) + E) → P.
				Data Transfers
01	01		PTA	(P) → A.
04	ee		LDN	E → A.
20	ee		LDD	(E) → A.
21	00	YYYY	LDM	(m) → A.
21	ee		LDI	((E)) → A.
22	00	XXXX	LDC	G → A.
22	ee		LDF	(P + E) → A.
23	00		LDS	((0)7777) → A.
23	ee		LDB	(P - E) → A.
05	ee		LCN	$\overline{E}$ → A. ($\overline{E}$ = 1's complement of the operand.)
24	ee		LCD	$\overline{(E)}$ → A.
25	00	YYYY	LCM	$\overline{(m)}$ → A.
25	ee		LCI	$\overline{((E))}$ → A.
26	00	XXXX	LCC	$\overline{G}$ → A.
26	ee		LCF	$\overline{(P + E)}$ → A.
27	00		LCS	$\overline{((0)7777)}$ → A.
27	ee		LCB	$\overline{(P - E)}$ → A.
40	ee		STD	(A) → E.
41	00	YYYY	STM	(A) → m.
41	ee		STI	(A) → (E).
42	00	XXXX	STC	(A) → G.
42	ee		STF	(A) → P + E.
43	00		STS	(A) → (0)7777.
43	ee		STB	(A) → P - E.
01	00	YYYY	BLS	Set an area of core storage to value present in Accumulator.
01	05	YYYY	ATE	Transfer contents of Accumulator to Buffer Entrance Register (BER).
01	06	YYYY	ATX	Transfer contents of Accumulator to Buffer Exit Register (BXR).
01	07		ETA	Transfer contents of BER to Accumulator.
01	30		CTA	Transfer contents of the 4 bank controls to Accumulator.
01	5e		STP	Store contents of Program Counter (P) to location (d)005e.
01	6e		STE	Transfer contents of BER to location (d)006e, and transfer contents of Accumulator to BER.
76	ee		HWI	Transfer E portion of contents of Accumulator to E portion of word in indirect bank whose address is at (d)00ee.
				Shifting
01	02		LS1	Circular shift (A) left 1 bit position.
01	03		LS2	Circular shift (A) left 2 bit positions.
01	10		LS3	Circular shift (A) left 3 bit positions.
01	11		LS6	Circular shift (A) left 6 bit positions.
01	14		RS1	Circular shift (A) right 1 bit position.
01	15		RS2	Circular shift (A) right 2 bit positions.
44	ee		SRD	(E) → A; left circular shift 1 position; (A) → E.
45	00	YYYY	SRM	(m) → A; left circular shift 1 position; (A) → m.
45	ee		SRI	((E)) → A; left circular shift 1 position; (A) → (E).

§ 121.

INSTRUCTION LIST (Contd.)

INSTRUCTION				OPERATION
F	E	G	Mnemonic Opcode	
				Shifting (Contd.)
47	00		SRS	((0)7777) → A; left circular shift 1 position; (A) → (0)7777.
46	00	XXXX	SRC	Operand → A; left circular shift 1 position; (A) → G.
46	ee		SRF	Operand → A; left circular shift 1 position; (A) → P + E.
47	ee		SRB	Operand → A; left circular shift 1 position; (A) → P - E.
				Input-Output
01	04		CBC	Stop buffer data transfer. Generate "no buffer complete" interrupt.
01	20		CIL	Clear the interrupt lockout.
72	00	YYYY	IBI	Initiates buffer channel input-output operation. Generate interrupt 20 when buffer operation complete. Go to YYYY if buffer is busy.
73	00	YYYY	IBO	Buffer output operation. See IBI.
72	ee	YYYY	INP	Normal channel input operation. Block of data transferred to indirect bank.
73	ee	YYYY	OUT	Normal channel output operation. Block of data transferred from indirect bank.
74	ee		OTN	Output one word (00ee) to selected device using normal channel.
76	00		INA	Input 1 word to Accumulator from selected device, using normal channel.
76	77		OTA	Output 1 word from Accumulator to selected device, using normal channel.
75	00	XXXX	EXC	Transmit External Function (XXXX) to external devices to select and instruct device.
75	ee		EXF	Transmit External Function to external device. Function is found ee locations forward of instruction.
				Miscellaneous
00	0e		NOP	Proceed to next instruction.
00	00		ERR	Computer stops; console ERR alarm; use RUN switch to continue.
77	00		HLT	Computer stops; console alarm; use RUN switch to continue.
77	77		HLT	Same as 7700.
77	0e		SLS	Stop if e sense switch is set.
77	e0	YYYY	SLJ	Jump to YYYY if e jump switch is set.
77	ee	YYYY	SJS	Test e jump switch and then e sense switch.
00	1e		SRJ	Set relative bank control to e and jump to address present in Accumulator.
00	2e		SIC	Set indirect bank control to e.
00	3e		IRJ	Set indirect and relative bank controls to e and jump to address present in Accumulator.
00	4e		SDC	Set direct bank control.
00	5e		DRJ	Set direct and relative bank controls to e and jump to address present in Accumulator.
00	6e		SID	Set indirect and direct bank controls to e.
00	7e		ACJ	Set direct, indirect, and relative bank controls to e and jump to address present in Accumulator.
01	4e		SBU	Set buffer bank control to e.

CODING SPECIMEN: OSAS/OSAS-A

§ 131.

.1 CODING SPECIMEN: Portion of a paper tape correction routine.

PROGRAM ____________ PAGE ____________
ROUTINE ____________

CONTROL DATA CORPORATION

OSAP CODING FORM

PAPER TAPE CORRECTION ROUTINE

PAGE NO. 2
DATE
PROGRAMMER

2 LOCATION	10 OP	15 ADDRESS	23 ADDITIVE	31 COMMENTS
	LDD	ASAVE		
	STI	TEMO		
	JFI	1		
		SET		
TANDP	EXC	4104		SELECT PUNCH
	AOD	NCNT		PUT CR IN OUTPUT
	ADD	SETUP		
	STD	TEMO		
	LDD	ASAVE		
	STI	TEMO		
	AOD	TEMO		TERM AD OF BLOCH
	STF	TAPO		
	OUT	UP		
TAPO				
	NZF	2		
UP		OUTPUT		
	LDN			
	STD	NCNT		
	ZJB	SET		RETURN
SLTYP	EXC	4240		
	INA			STATUS
	ZJF	3		
	ERR			
	NZB	SLTYP		
	EXC	4220		SELECT TYPEWRITER IF OK
OFLG	LDN			
	STD	SFLAG		
INP	INA			TYPE IN CORRECTION
	STD	ASAVE		
	LDD	SFLAG		AND CONVERT TO FLEX
	NZF	CHECK		
	LDD	ASAVE		

FORM 138e — REPLACES 138a&b Use shaded columns only if first symbol character is + or -, or for 4 character OP code

.2 CODING SHEET

PROGRAM ______________ PAGE ______

ROUTINE ______________

CONTROL DATA CORPORATION

OSAP CODING FORM

PAGE NO. ____________
DATE ____________
PROGRAMMER ____________

2 LOCATION	10 OP	15 ADDRESS	23 ADDITIVE	31 COMMENTS

FORM 138e — REPLACES 138a&b Use shaded columns only if first symbol character is + or -, or for 4 character OP code

CODING SPECIMEN: FORTRAN-A

§ 132.

.1 CODING SPECIMEN

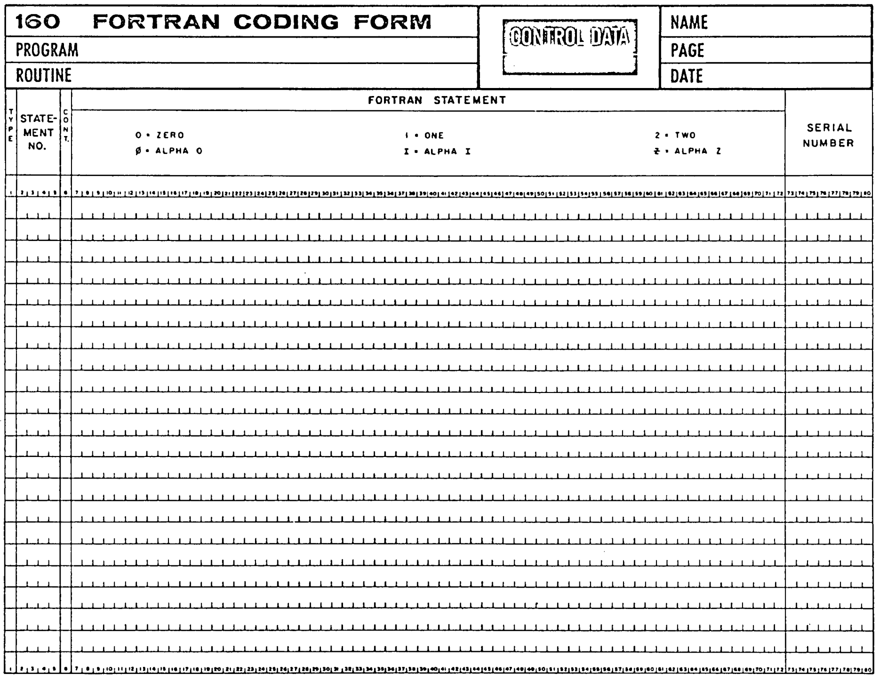
```
100  FORMAT (I4/(F5.1,F11.8))
101  FORMAT (F12.3/2F12.3/2F12.3/F12.3)
102  FORMAT (3F12.3)
     DIMENSION X(10),Z(10)
     READ100, N, (X(I),Z(I), I=1,N)
     READ101, TN2, CHI1,CHI2,A,B,ZO
     XBAR=0
     ZBAR=0
     DO 1 I=1,N
     XBAR=XBAR+X(I)/N
1    ZBAR=ZBAR+Z(I)/N
C    ESTIMATE REGRESSION COEFFICIENTS AND
     VARIANCE
     BETA=0
     ALPHA=0
     TEMP=0
     DO 2 I=1,N
     BETA=(X(I)-XBAR)'(Z(I)-ZBAR)+BETA
2    TEMP=TEMP+(Z(I)-ZBAR)''2
     BETA=BETA/TEMP
     ALPHA=XBAR-BETA'ZBAR
     VAR=0
     DO 3 I=1,N
3    VAR=VAR+(X(I)-ALPHA-BETA'Z(I))''2/N
     PUNCH102, ALPHA, BETA, VAR
C    CONFIDENCE INTERVAL FOR ALPHA
     TEMP=0
     TEMP1=0
     DO 4 I=1,N
     TEMP=TEMP+Z(I)''2
4    TEMP1=TEMP1+(X(I)-ALPHA-BETA'Z(I))''2
     TEMP1=TEMP1'TEMP
     TEMP=0
     DO 5 I=1,N
5    TEMP=TEMP+N'(N-2)'(Z(I)-ZBAR)''2
     TEMP=SQRTF(TEMP/TEMP1)
     TEMP2=(TN2+ALPHA'TEMP)/TEMP
     TEMP1=(-TN2+ALPHA'TEMP)/TEMP
     PUNCH102, TEMP1, TEMP2
```

.1 CODING SPECIMEN (Contd.)

```
C    CONFIDENCE INTERVAL FOR BETA
     TEMP1=0
     TEMP2=0
     DO 6 I=1,N
     TEMP1=TEMP1+(X(I)-ALPHA-BETA'Z(I))''2
6    TEMP2=TEMP2+(N-2)'(Z(I)-ZBAR)''2
     TEMP=SQRTF(TEMP1/TEMP2)
     TEMP1=(-TN2+BETA'TEMP)/TEMP
     TEMP2=(TN2+BETA'TEMP)/TEMP
     PUNCH102, TEMP1,TEMP2
C    CONFIDENCE INTERVAL FOR VAR
     TEMP1=(N'VAR)/CHI2
     TEMP2=(N'VAR)/CHI1
     PUNCH102,TEMP1,TEMP2
     TEMP=0
C    COMPUTE F FOR ALPHA=A AND BETA=B
     DO 7 I=1,N
7    TEMP=TEMP+(Z(I)''2)'(BETA-B)
     TEMP1=(N'(ALPHA-A)+2'N'ZBAR'(ALPHA-A)'
    1(BETA-B)+TEMP)/(N'VAR)
     PUNCH102, TEMP1
C    PREDICTION INTERVAL FOR X CORRESPONDING TO Z
     TEMP=0
     DO 8 I=1,N
8    TEMP=TEMP+(Z(I)-ZBAR)''2
     TEMP=TN2'VAR'SQRTF((N/(N-2))'((N+1)/N
    1+(ZO-ZBAR)''2/TEMP))
     TEMP1=ALPHA+BETA'ZO-TEMP
     TEMP2=ALPHA+BETA'ZO+TEMP
     PUNCH102, TEMP1, TEMP2
     STOP 7707
     END
     END
```

§ 132.

.2 CODING SHEET


160 FORTRAN CODING FORM

CONTROL DATA

NAME

PROGRAM

PAGE

ROUTINE

DATE

TYPE | STATE-MENT NO. | CONT. | FORTRAN STATEMENT | SERIAL NUMBER

0 = ZERO   I = ONE   2 = TWO

Ø = ALPHA O   I = ALPHA I   Ƶ = ALPHA Z

FORM 252-A

CODING SPECIMEN: INTERFOR

§ 134.

.1 CODING SPECIMEN - INTERFOR

A. IDENTIFICATION

TITLE: INTERFOR Subroutine - Sine Cosine

B. PURPOSE

Given X, compute the Sin X or Cos X (where X is in radians)

This is a relocatable program on Flexowriter tape with entry address of Sin X at 0000/ and Cos X at 0045/. Basic entry address is at 0033/. Accuracy is within 1 or 2 in the ninth decimal place.

```
         INTERFOR-2              SIN X   COS X


0000     75007777   entrance to sin x subroutine
         32000032/

         20000016/
         30000015/
             .
             .
             .
             .
         20000017/
         50000000

         12000014/
         75400033/    entrance to basic to evaluate series

         32000016/
         75000051/   go to check  limit of one

         00400017/
         00000025/

         00410000
         00000000
             .
             .
             .
             .
         77752427
         31403333

         7500 7777
         51000041/        exit to basic language

         2056 4067
         0404 4056
         2016 4220
         2014 4214

         0400 4014
         4015 4016

         2200 4011
         4012 7001

         3200 7777        LOOP
         5000 0000

         3060 7777        TABLE
         51000033/        exit to basic language
```

§ 134.

.1 CODING SPECIMEN - INTERFOR (Contd.)

```
      .
      .
      .
2056 0701
4056 6205

2067 4056
2341 7057

2202 7057
0040/0000

75007777        cos x entrance
30000050/

75400000/
00000000
      .
      .
      .
1300 0022/
7500 0000/
;;;;;
```

.2 CODING SPECIMEN - INTERFOR FLAP SYMBOLIC INPUT

The following example demonstrates how a sequence of instructions in a symbolic program appears on the listable output. The coding represents a routine that uses programmable input/output subroutines.

EXAMPLE:

Symbolic Input

Loc	Op	B	M
	ORG		2000
START	ENI	1	0
LOAD	SLJ	4	1224
,	STA	1	BLOCK
,	ISK	1	9D
	SLJ	0	LOAD
	SLS	0	OUT
BLOCK	EQU		3000
OUT	ENI	1	0
DUMP	LDA	1	BLOCK
	SLJ	4	1236
	ISK	1	4D
	SLJ	0	DUMP
	SLS	0	START
	END		START

CODING SPECIMEN: SICOM

§ 135.

.1 CODING SPECIMEN

Develop a subroutine to obtain Y with a given X where

$$Y = \frac{X + A}{X^2 - B}, \quad A = 3.1416, \quad B = 8.765,$$

and X is stored in location 0050 within the main program.

MAIN PROGRAM

LOC	CODE	NOTES
0000	0220050	Load X
0001	0700200	Jump to SR at 0200
0002	040Y000	Print Y

SUBROUTINE

LOC	CODE	NOTES
0200	0000008	Set Non-Trace
0201	0000006	Set Relative Mode
0202	0300010	Add X + A
0203	0770013	Store X + A
0204	0310008	Subtract X - A (to restore X)
0205	025Y000	Multiply $X \cdot X = X^2$
0206	0310008	Subtract X^2 - B
0207	0230009	Inverse Divide, $Y = \frac{X + A}{X^2 - B}$ (Y in A. R.)
0208	0000007	Set Absolute Mode
0209	0000009	Reset Trace
0210	0000070	Return to 0002
0212 =	3.1416	
0214 =	8.765	
0216 =	Storage of X + A	

CODING SPECIMEN: AUTOCOMM

§ 136.

.1 <u>CODING SPECIMEN</u>

AUTOCOMM CODING FORM — CONTROL DATA CORPORATION — DATE ______ PAGE NO. 1 — PROGRAM ______ — PROGRAMMER ______

NAME (2–8)	LEVEL (10–13)	PROCEDURE STATEMENT: LENGTH (15–21) / DESIGNATOR (23–29)	COMMENTS (31–72)
	REM		PERSØNNEL FILE UPDATE
		SET INDEX1 TØ "0".	
		RDCRD STØRE, IF ERRØR GØ TØ STØP1, IF END ØF FILE CARD -	
		GØ TØ EØJ.	
LØAD		READ MASTER, IF ERRØR GØ TØ STØP2, IF END ØF FILE SENSED -	
		GØ TØ EØF.	
CØMP		CØMPARE SERV1 TØ SERVNØ(1), IF LØW GØ TØ STØP3, IF EQUAL -	
		GØ TØ UPDATE, IF HIGH GØ TØ NEXT.	
NEXT		INCREASE INDEX1 BY "30", IF "150" GØ TØ ØUT.	
		GØ TØ CØMP.	
ØUT		SET INDEX1 TØ "0".	
		WRITE ØUTMST, IF ERRØR GØ TØ STØP4, IF END ØF TAPE-	
		SENSED GØ TØ EØT.	
		GØ TØ LØAD.	
UPDATE		MØVE RNK TØ RANK(1).	
		MØVE GRAD1 TØ GRADE(1).	
		ZRØADD PAYMØN TØ MØNPAY(1), IF ERRØR GØ TØ STØP5.	
		MØVE MØS1 TØ MØS(1).	
		MØVE NAME(1) TØ NAME1.	
		MØVE RANK(1) TØ RANK1.	
		MØVE PICT1 TØ PAY1.	
		MØVE PICT2 TØ SERNØ.	
		MØVE MØS(1) TØ MØS2.	
		EDIT SERV2(1) TØ SERNØ.	
		EDIT MØNPAY(1) TØ PAY1.	

Ø = ALPHA O O = ZERO – = MINUS ‐ = HYPHEN FORM 383

AUTOCOMM CODING FORM — CONTROL DATA CORPORATION — DATE ______ PAGE NO. 2 — PROGRAM ______ — PROGRAMMER ______

NAME (2–8)	LEVEL (10–13)	PROCEDURE STATEMENT: LENGTH (15–21) / DESIGNATOR (23–29)	COMMENTS (31–72)
		PRINT ØUTPUT.	
		RDCRD STØRE, IF ERRØR GØ TØ STØP1, IF END CARD GØ TØ EØJ.	
		GØ TØ NEXT.	
EØJ		READ MASTER, STØP6, EØF.	
		WRITE ØUTMST, STØP7, EØT.	
		GØ TØ EØJ.	
EØF		LØCK MASTER.	
		MARK ØUTMST.	
EØT		LØCK ØUTMST.	
	HLT		END ØF JØB
STØP1	HLT		CARD READ ERRØR
STØP2	HLT		READ MASTER ERRØR
STØP3	HLT		WRØNG SEQUENCE
STØP4	HLT		WRITE ERRØR ØUTMST (CØPY)
STØP5	HLT		ARITH ERRØR ZRØADD
STØP6	HLT		READ ERRØR (FINAL CØPY)
STØP7	HLT		WRITE ERRØR (FINAL CØPY)
	DATA	01	
STØRE	F1	80	CARD FILE FØR UPDATE
SERV1	02	8	CØLUMNS 1-8
	02	2	
RNK	02	6	CØLUMNS 11-16
	02	4	
GRAD1	02	2	CØLUMNS 21-22
	02	8	

Ø = ALPHA O O = ZERO – = MINUS ‐ = HYPHEN FORM 383

§ 136.

.1 CODING SPECIMEN (Contd.)

AUTOCOMM CODING FORM — CONTROL DATA CORPORATION — DATE — PROGRAM — PROGRAMMER — PAGE NO. 3

NAME	LEVEL	LENGTH	DESIGNATOR	COMMENTS
PAYMØN	02	6	P2	CØLUMNS 31-36
	02	4		
MØS1	02	6		CØLUMNS 41-46
MASTER	F1	300	1	PERSØNNEL FILE RECØRD-5 FILES, 60 CHAR.
NAME	02	30		
LAST	03	10		
FIRST	03	10		
MIDDLE	03	10		
RANK	02	6		
SERVNØ	02	8		SERVICE NUMBER
PREFIX	03	2		
BØDY	03	4		
SUFFIX	03	2		
MØS	02	6		JØB CØDE
PAYCØDE	02	8		
GRADE	03	2		
MØNPAY	03	6	P2	
	RDFN	MASTER		
ØUTMST	F1	300	2	ASSIGN TAPE HANDLER 2 FØR RECØRD ØUTPUT
	RDFN	SERVNØ		
SERV2	02	8	P0	REDEFINE SERVNØ AS NUMERIC
	DATA			
ØUTPUT	F1	120	1	PRINTER ØUTPUT, CHANNEL 1
NAME1	02	30		
	02	6		

Ø = ALPHA O   O = ZERO   – = MINUS   " = HYPHEN   FORM 383

AUTOCOMM CODING FORM — CONTROL DATA CORPORATION — DATE — PROGRAM — PROGRAMMER — PAGE NO. 4

NAME	LEVEL	LENGTH	DESIGNATOR	COMMENTS
RANK1	02	6		
	02	6		
SERNØ	02	12		
	02	6		
PAY1	02	10		
	02	6		
MØS2	02	6		
	RDFN	ØUTPUT		FILL PRINTER ØUTPUT AREA WITH BLANKS
	77	40		
	77	40		
	77	40		
	DATA			
PICT1	77	10		99999$.999
PICT2	77	12		999/9999/999
	END			

Ø = ALPHA O   O = ZERO   – = MINUS   " = HYPHEN   FORM 383

.2 CODING SHEET

AUTOCOMM CODING FORM

CONTROL DATA CORPORATION

DATE ______ PAGE NO. ______
PROGRAM ______
PROGRAMMER ______

NAME		PROCEDURE STATEMENT			
	LEVEL	LENGTH		DESIGNATOR	COMMENTS
2 8	10 13	15 21		23 29	31 72

FORM 383

Ø = ALPHA O   O = ZERO   – = MINUS   " = HYPHEN

DATA CODE TABLE NO. 1

§ 141.

.1 USE OF CODE: . . . card input-output.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 1 column per character.

.23 Character Codes

UNDERPUNCH	OVERPUNCH			
	None	12	11	0
None	BLANK	+	- (MINUS)	
12				
11				
0	0			
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
8-2				
8-3	=	.	$	,
8-4	— (DASH)	)	*	(
8-5				
8-6				
8-7				

DATA CODE TABLE NO. 2

§ 142.

.1 USE OF CODE: . . . printer.

.2 STRUCTURE OF CODE

.21 Character Size: . . . 2 octal digits (6 bits) per character.

.22 Character Structure

.221 More significant pattern: . . . . . 1 octal digit (0 to 7).

.222 Less significant pattern: . . . . . 1 octal digit (0 to 7).

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0	:	8	BLANK	Y	-	Q	+	H
1	1	9	/	Z	J	R	A	I
2	2	0	S	⊐	K	NOTE 2	B	<
3	3	=	T	,	L	NOTE 3	C	.
4	4	≠	U	(	M	*	D	)
5	5	≤	V	→	N	↑	E	≥
6	6	'	W	≡	O	↓	F	?
7	7	⊏	X	NOTE 1	P	>	G	;

Notes: 1 ∧ or ~
2 v or %
3 ⌉ or $

DATA CODE TABLE NO. 3

§ 143.

.1 USE OF CODE: . . . BCD representation.

.2 STRUCTURE OF CODE

.21 Character Size: . . . 2 octal digits (6 bits) per character.

.22 Character Structure

.221 More significant pattern: . . . . . . 1 octal digit (0 to 7).

.222 Less significant pattern: . . . . . . 1 octal digit (0 to 7).

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0		8	BLANK	Y	- (MINUS)	Q	+	H
1	1	9	/	Z	J	R	A	I
2	2	0	S		K	- (MINUS)	B	+
3	3	=	T	,	L	$	C	.
4	4	— (DASH)	U	(	M	*	D	)
5	5		V		N		E	
6	6		W		O		F	
7	7		X		P		G	

DATA CODE TABLE NO. 4

§ 144.

.1 USE OF CODE: . . . binary representation.

.2 STRUCTURE OF CODE

.21 Character Size: . . . 2 octal digits (6 bits) per character.

.22 Character Structure

.221 More significant pattern: . . . . . . 1 octal digit (0 to 7).

.222 Less significant pattern: . . . . . . 1 octal digit (0 to 7).

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0	0	8	+	H	- (MINUS)	Q	BLANK	Y
1	1	9	A	I	J	R	/	Z
2	2		B		K		S	
3	3	=	C	.	L	$	T	,
4	4	— (DASH)	D	)	M	*	U	(
5	5		E		N		V	
6	6		F		O		W	
7	7		G		P		X	

DATA CODE TABLE NO. 5

§ 145.

.1 USE OF CODE: . . . Typewriter input-output.

.2 STRUCTURE OF CODE

.21 Character Size: . . . 2 octal digits (6 bits) per character.

.22 Character Structure

.221 More significant pattern: . . . . . . 1 octal digit (0 to 7).

.222 Less significant pattern: . . . . . . 1 octal digit (0 to 7).

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0			e E	a A	, ,	; :	7 &	2 @
1	t T	1 L	z Z	w W		TAB	BS	
2	= ÷	r R	d D	j J	. .	- _	4 $	6 ¢
3	o O	g G	b B	8 ½				
4	SPACE	i I	s S	u U	/ ?	' "	3 #	1 *
5	h H	p P	y Y	q Q	CR			
6	n N	c C	f F	k K	+ °	0)	5 %	
7	m M	v V	x X	9 (	UC	LC		

Note: Both upper and lower case symbols shown in each box.

DATA CODE TABLE NO. 6

§ 146.

.1 USE OF CODE: . . . . printer collating sequence.

.2 STRUCTURE OF CODE

In ascending sequence

:	Blank	-	+
1	/	J	A
2	S	K	B
3	T	L	C
4	U	M	D
5	V	N	E
6	W	O	F
7	X	P	G
8	Y	Q	H
9	Z	R	I
0	⊐	% or V	<
=	,	$ or 7	.
≠	(	*	)
≤	→	↑	≥
!	≡	↓	?
⊏	~ or ∧.	>	;

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers

The 160-A INTERFOR assembler and interpreter subroutines permit the use of floating point instructions for the CDC 1604/1604-A computers (see Sections 244:173 and 244:184).

The National Cash Register NCR 310 computer, made by Control Data Corporation, is a CDC 160 with some instructions omitted. No known efforts are being made by 160 users to simulate the 310.

The CDC 160 can be simulated in most cases. Times are the same as on the 160. Halt codes must be checked for proper format, and all bank controls are set to zero before running.

.12 Simulation by Other Computers: . . . . . none.

.13 Data Sorting and Merging

Sort 3X

Reference: . . . . . SWAP listing, program H2.01.
Record size: . . . . 1 item; variable length, up to 984 char including key.
Block size:. . . . . . 1 record.
Key size: . . . . . . 1 to 10 variable length fields.
File size: . . . . . . 1 tape reel. Number of characters depends on record size; for example, 125,000 80-char records at 556 char/inch, and 56,500 80-char records at 200 char/inch.
Number of tapes: . . 4, using #162, 163, or 164 tape systems.
Date available:. . . . November, 1962.
Description
Sort 3X sorts one reel of tape using a two-way merge technique, with internal sorting performed on blocked records. Intermediate tape records are blocked in 1,000 character blocks. Time to sort 20,000 80-character records, with a 16-character key, on a 30 KC tape, is 89 minutes (manufacturer's example). The program was written for the 160, and makes no use of buffering in the 160-A.

.14 Report Writing: . . . . none.

.15 Data Transcription

.151 General
A number of data transcription routines are presently available which use both the older peripheral equipment found on the 160/160-A systems and the newer 167 Card Reader and 166-1 Printer. The older equipment referred to is the 1610 Controller for IBM card equipment, the 1612 line printer, the 163, 164, and 1607 magnetic tape systems, and the 1609 card read and punch unit. No routines exist specifically for the new 162 magnetic tape system using 603 or 606 tape units or the new buffered line printer, Model 166-2. However, the 603 tape unit set at low density can operate correctly in place of a 163 tape unit.

Card-to-tape transcriptions proceed at reading speeds of 650 cards per minute using the 1610-A controller and the IBM 088 Collator, or at 250 cards per minute using the 167 Card Reader.

.152 SIMO
Reference: . . . . . SWAP listing, program AD2.02.
Date available: . . . presently available.
Description
This program permits two concurrent data transcriptions: card-to-tape and tape-to-printer. The printer is the 1612 Printer, the tape units are the older Model 163 tape units which run at 30 KC, and the card reader is the IBM 088 Collator and 1610-A controller. The 160-A which is required contains basic storage (8,192 words).

An independent card-to-tape operation proceeds at 250 cards per minute (reader speed). An independent print operation proceeds at 1,000 lines per minute (maximum 48-character-set speed). If both operations proceed concurrently, a 5 to 10 per cent loss in peak speeds results on each program.

Card data can be Hollerith or column binary. Output records on tape consist of 80 BCD characters or 160 six-bit binary images, plus optional control characters. The optional characters are used to store information about the type of card image of the present record and the next record on tape. In any case, binary cards may be intermixed with BCD cards.

.153 Peripheral Processing Package (PPP)
Reference: . . . . . SWAP listing, program AD2.01, and CDC Manual, Publication 517, July 1962.
Date available:. . . . presently available.
Description
The Peripheral Processing Package contains all input and output subroutines, which are in the 160-A at one time. A control subroutine can use any one of these as specified by the setting of jump control switches on the console.

§ 151.

.153 Peripheral Processing Package (PPP) (Contd.)
Description (Contd.)

When one transcription is complete (for example, card-to-tape), the operator resets jump control switches and the next transcription specified starts immediately. Usable units are the older 163 and 1607 magnetic tape systems (30 KC tapes), the fast 1612 Printer (1,000 lines per minute with 48-character set), and the 1610-A adapter for the IBM 088 Collator and 523 card punch (reads 650 cards per minute; punches 100 cards per minute).

The manufacturer has demonstrated a newer version of a peripheral processing package; see next paragraph.

.154 Peripheral Processing Package (PPPP)
Reference: . . . . . publication BR-9.
Date available: . . . routine demonstrated in October, 1962.
Description
One to four tape-to-printer operations occur concurrently, each at 1,000 lines per minute (48-character printer set), as well as a single card-to-tape operation (using the 250-card-per-minute Model 167-2 reader, and Model 603 tape units). With auxiliary core storage, it is possible to perform two card-to-tape or tape-to-card operations and up to eight printing operations.

.16 File Maintenance

Paper Tape Edit

Reference: . . . . . program A2.01A in SWAP listing.
Date available: . . . presently available.
Description: . . . . . permits replacements, insertions, and deletions of source statements prepared for the OSAS machine oriented language translator, or for FLAP, an input to the INTERFOR interpreter.

OSAS-A Master Paper Tape Edit

Reference: . . . . . program AA2.02 in SWAP listing.
Date available: . . . presently available.
Description: . . . . . permits additions or deletions to I/O subroutines of OASA-A Master Paper Tape. Also permits duplicating the tape.

.17 Other

.171 Floating point arithmetic: . . . . . see Central Processor, Section 244:051.412 for floating point times.

.172 Floating point functions

Function	Time µ sec Subroutine	Time µ sec 168-2 floating point option	Storage, words Subroutine	Storage, words 168-2 floating point option
Arc sin:	200,000		60	
Arc cosine:	200,000	?	60	?
Exponential (2 exp x, 10 exp x, e exp x):	?	?	29	?
Square root:	100,000	3,200	21	?
Log to base 2:	?	?	478	?
Trigonometric series expansions:	?	?	98	?

.173 Radix conversion
Binary to 4-bit decimal: . . . . . . 4,300 µsec per decimal digit.
Decimal to binary: . . approximately 230 + 198N µsec, where N = no. decimal digits to be converted. Result is double precision (2 words); 6.6 decimal digit precision.
General Binary-to-BCD and BCD to Binary Conversion: . SWAP program listing AH1.04. Accepts FORTRAN-like statements and performs internal conversions. Numeric conversions are in decimal or octal and operate on 1 computer word. The A, X, and H statements are provided. Program requires 1,075 locations.

.174 Binary arithmetic
Single precision divide: . . . . . . 23-bit fraction ÷ 11-bit fraction, giving rounded 11-bit fraction. Time is 2,000 µsec.
Integer divide: . . . 23-bit integer ÷ 11-bit integer, giving 12-bit quotient with 11-bit remainder. Time is 2,000 µsec.
Multiple precision package: . . . . . . N-binary-word precision subroutine. Add, subtract, multiply, divide, and shifting provided. No timing given. Storage required is 720 + 1.5N words, where N = no. of words of precision.
Double precision arithmetic: . . . 2-word binary add, subtract, multiply, divide provided. Times are found in Central Processor (244:051.411).
Single precision fractional square root: . . . . timing is 2,250 µsec per iteration; max time is 25,000 µsec.
9-bit quick multiply: . product of 2 words formed as 1 word, accurate to 10 bits. Time is 595 to 660 µsec.

§ 151.

.174 Binary arithmetic (Contd.)

9-bit quick sine: . . . obtains sine of an angle which is less than 90 degrees. Accurate to 9 bits. Time is approximately 3,000 μsec.

.175 Matrix inversion: . . . Program II.06; written in 160 FORTRAN-A. Finds inverse of square matrix in 160 or 160-A. Size of subroutines is 487 words, and it inverts up to a 17 x 17 matrix in the 160, and a 33 x 33 matrix in the 160-A (8,192 word store). See graph in System Performance (244:201.32).

.176 Decimal Computations Programming System (BCK)

Description

The BCK program package, B2.00, provides a control routine and a number of arithmetic and logical subroutines for handling decimal numbers. Numbers up to 12 decimal digits can be processed; and the subroutines are called by alphabetic mnemonics. The OSAS assembler and the BCK subroutine are used to execute the source program interpretively. BCK occupies 550 words of core storage. The operations possible using BCK are:

ADD	MOVE	BCDBCK
SUB	GOTO (unconditional transfer)	(BCD to BCK conversion)
MPY	RECODE	BCKBCD
DIVIDE	(translate by table	(BCK TO BCD
COMPAR	look-up)	conversion)

.177 Equation Solver: . . . SWAP program listing AJ1.01. Program will solve 30 linear equations with 30 unknowns. Derived matrix can be output.

.178 Other: . . . . plot routines using the 165 plotter.
Linear Program I.
7 statistical programs.
8 Civil Engineering design programs.
Prime Factor Extractor.
NIM.

.2 PROBLEM ORIENTED LANGUAGES: . . . . none.

PROCESS ORIENTED LANGUAGE: 160 FORTRAN-A

§ 161.

.1 GENERAL

.11 Identity: . . . . CDC 160 FORTRAN-A.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . OPERATING PROCEDURES for 160 FORTRAN-A, Publication PSB-BF01 (Revised), Sept., 1962.

160 FORTRAN/REFERENCE MANUAL, Publication 503, April, 1962.

.14 Description

160 FORTRAN-A is a slightly revised version of the CDC 160 FORTRAN language and is provided as an interim language for the 160-A computer until 160-A FORTRAN is released. Section 244:162 describes the 160-A FORTRAN language; Section 242:161 describes the 160 FORTRAN language; and Section 242:182 describes the 160 FORTRAN translator. Refer to Section 242:182 for the translator applicable to 160 FORTRAN-A. Only the main features of 160 FORTRAN-A and the differences between it and 160 FORTRAN are described in this section.

160 FORTRAN-A uses the same language as 160 FORTRAN. Both are versions of IBM 709/7090 FORTRAN II, described in Section 408:161. However, the source program for the 160-A may be placed on punched cards, instead of only on punched tape as required in 160 FORTRAN. The compiler and the interpreter are read from punched tapes as before. Two additional compiler error checks are provided, one for duplicate label and one for statement out of order. See Section 242:182 for a description of the 160 FORTRAN Translator.

Subroutines are brought in using CALL statements, and names are formed using the same rules as in IBM 7090 FORTRAN. Constants and integer variables have a maximum size of only 2,047, and are represented as 1 computer word. Floating point variables are represented by three computer words and fall within the range of $\pm 10^{31}$. Boolean operations are permitted, and mixed mode arithmetic (floating and fixed point in the same statement) is provided as an extension to IBM FORTRAN. The larger storage of the 160-A (8,192 words compared to the basic 4,096 word storage of the 160 computer) permits longer source programs to be used. A larger matrix can be held in the 160-A. The maximum size matrix which can be inverted by the I1.06 Matrix Inversion program in the SWAP user's listing is 33 by 33; in the 160 computer the maximum size is 17 by 17. Inversion time for a 30 by 30 matrix is estimated to be 20 minutes.

Refer to the 160 FORTRAN Translator section (242:182) for a description of translation.

PROCESS ORIENTED LANGUAGE: 160-A FORTRAN

§ 162.

.1 GENERAL

.11 Identity: . . . . 160-A FORTRAN.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . 160-A FORTRAN/GENERAL INFORMATION MANUAL, Publication 505, no date.

160-A FORTRAN/ REFERENCE MANUAL, Publication 513, March, 1963.

.14 Description

CDC 160-A FORTRAN is a more complete version of the IBM 709/7090 FORTRAN II language than CDC 160 FORTRAN. The 160-A FORTRAN language was announced late in 1962, and is not yet fully implemented and documented (March, 1963). The references listed in Paragraph .13 contain a description of the language and the translator.

Section 244:162 describes the 160-A FORTRAN language; Section 242:161 describes the 160 FORTRAN language; and Section 242:182 describes the 160 FORTRAN translator. Only the main features of 160-A FORTRAN and the differences between it and 160 FORTRAN are described in this section. Changes to 160 FORTRAN are listed listed below:

a. The COMMON statement is permitted, and is used to link variables in subroutines and main programs. Programs and subprograms which are to be run together must be compiled together.

.14 Description (Contd.)

b. All 709/7090 FORTRAN statements are permitted except READ DRUM and WRITE DRUM. The 160 INPUT and OUTPUT statements are no longer used.

c. Fixed point constants and variables can be as large as 4, 194, 303 (two computer words), and statement numbers can be as large as 99, 999.

Subroutines are brought in using CALL statements, and names are formed using the same rules as in IBM FORTRAN. The number of subroutines is restricted only by available core storage. Floating point variables are represented by three computer words and fall within the range of $\pm 10^{31}$. Boolean operations are permitted, and mixed mode arithmetic (both fixed and floating point operands in one expression) is provided as an extension to IBM 7090 FORTRAN.

For other details of the 160-A FORTRAN, refer to the 160 FORTRAN description referenced above.

With respect to IBM 709/7090 FORTRAN II, FUNCTION and FREQUENCY statements are not permitted. Complex arithmetic, an addition to the 7090 FORTRAN, is not permitted in 160-A FORTRAN.

Object programs are executed interpretively, as before, and compile-and-run operation is possible with 160-A FORTRAN.

PROCESS ORIENTED LANGUAGE: AUTOCOMM

§ 163.

.1 GENERAL

.11 Identity: . . . . AUTOCOMM.

.12 Origin: . . . . Control Data Corp., Minneapolis, Minn.

.13 Reference: . . . . . . AUTOCOMM/GENERAL INFORMATION, CDC Publication No. 524, November, 1962.
AUTOCOMM/REFERENCE MANUAL, CDC Publication No. 519, March, 1963.

.14 Description

AUTOCOMM is a pseudo English language programming system designed for commercial data processing problems. This language can utilize any of the standard 160-A input-output devices, and its operation repertoire includes decimal arithmetic, multiword transfers, alphabetic and numeric comparisons, format conversions, and editing. Seven pseudo index registers can be set, incremented, and tested by procedural statements.

The AUTOCOMM system consists of a source language translator and a library of macro subroutines that are called by the source language statements. AUTOCOMM source programs are translated into OSAS-A (the 160-A assembly language) and then into machine language object programs. OSAS-A symbolic statements can be used in the Procedure Section of AUTOCOMM programs. The library of macro subroutines is stored on magnetic tape in OSAS-A language. Additional subroutines can easily be added by the user.

Every AUTOCOMM program is divided into a Data Section and a Procedure Section. The Data Section describes the files and items to be processed. Up to nine levels of data items are permitted. Each data statement specifies the name of an item or file, its level number, and its size in characters. For numeric items, the decimal point location can also be specified. Names cannot be more than six characters in length. Special data statements can be used to define alphameric constants of up to 42 characters, signed numeric constants of up to 12 digits, and working storage areas.

Internal data representation is in standard six-bit BCD code, with two characters per 160-A word. Special provisions allow the processing of files recorded with only one character per word. A redefine pseudo operation, RDFN, permits the assignment of more than one file to the same storage area.

The Procedure Section contains the AUTOCOMM procedural statements and any OSAS-A symbolic coding that may be required. Each statement may be named and can specify only one AUTOCOMM operation, along with its associated error and conditional clauses, if any. Most AUTOCOMM statements result in the generation of a return jump to a subroutine in the object program, but others result in the in-line generation of a block of machine coding.

All AUTOCOMM arithmetic statements have the following general form, which is quite similar to that of COBOL:

ADD data-name-1 TO data-name-2, IF ERROR GO TO procedure-name.

Operands may be up to 12 digits long; literals may not be specified as operands; and the original value of "data-name-2" is always replaced by the result of the operation.

The EDIT verb can be used to suppress leading zeros or to insert dollar signs, asterisks, commas, periods, and slashes into numeric data to be listed. The transmitting field contains the all-numeric data item. The receiving field contains a COBOL-like "picture" (specified as an alphameric constant in the Data Section) that indicates the desired output format. The picture is destroyed by the EDIT operation (i.e., it is replaced by the edited numeric item).

The COMPARE verb transfers control to one of three procedural statements, depending upon the result of a comparison of two alphameric items. TEST determines whether a specified numeric field is negative, zero, or positive, and transfers control accordingly. AUTOCOMM includes a complete set of input-output statements, but no provision has been made for the blocking and unblocking of records on magnetic tape files.

AUTOCOMM should be useful for the same type of commercial batched-processing applications as COBOL, should be somewhat easier than COBOL to learn and use, but is considerably more limited than COBOL in the facilities it offers.

.15 Translator Availability: ?

MACHINE ORIENTED LANGUAGE: OSAS/OSAS-A

§ 171.

.1 GENERAL

.11 Identity: . . . . 160 Assembly System. OSAS.
160-A Assembly System. OSAS -A.

.12 Origin: . . . . Control Data Corporation.

.13 Reference

OSAS: . . . . CDC Publication 501.
OSAS-A: . . . . CDC Publication 507A.

.14 Description

OSAS and OSAS-A provide simple, straightforward assembly systems for the 160 and 160-A Computers. The system accepts mnemonic or numeric operation codes for all the computer operation codes, and several pseudo operation codes. Synonyms can be defined, but no macro instructions are provided. Both the 160 and 160-A systems provide relocatable binary output as object programs. Both systems will accept library routines for assembly with the object program. These routines must follow the source program during assembly.

Under operator control, a given symbol table can be entered into the system to link individually assembled programs or segments of programs. Symbols consist of one to six alphameric characters. The OSAS symbol table has a maximum usable symbol table size of approximately 250 symbols, and can be considerably smaller depending on the media selected for input, intermediate and final output, and the list output.

The OSAS-A system has a symbol table size of approximately 1,000 symbols in the basic 160-A system using 8,192 words of core storage. To use more storage of the 160-A system, the assembler must be modified.

Pseudo operations provide for control of two separate allocation counters; one for lower core (locations 00 to 77 octal) and the other for the remainder of core storage. Constants and alphamerics may be entered as data in the comments field of a statement under pseudo operation control. From 32 to 50 characters are allowable depending on the input medium used.

.15 Publication Date

OSAS: . . . . March, 1962.
OSAS-A: . . . . . . Revised November, 1962.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . . . see coding diagram in Section :131.

.22 Legend

Location: . . . . . . name for statement location.
Operation Code: . . . operation code or pseudo-operation code.
Address: . . . . . . operand address or data for pseudo-operation.
Additive: . . . . . . increment or decrement for address.
Comments: . . . . . comments by programmer; also constants.

.23 Corrections: . . . . . no convention or requirements.

.24 Special Conventions

.241 Compound addresses: address + contents of additive field.
.242 Multi-addresses: . . . none.
.243 Literals: . . . . . . permissible for address and additive fields; followed by D.
.244 Special coded addresses: . . . . . none.

.3 LABELS

.31 General

.311 Maximum number of labels
Procedures
OSAS: . . . . . . 340 or fewer, depending on length of I/0 subroutines specified for use by assembler.
OSAS-A: . . . . . 1,000 - 2C, where C = no. of constants labeled.
Constants
OSAS: . . . . . . included with labels for procedures.
OSAS-A: . . . . . 1,000-P, where P = no. of procedures labeled.
Files: . . . . same as Procedures.
Record: . . . . . . same as Procedures.
Items: . . . . same as Procedures.
.312 Common label formation rule: . . . . . . yes.
.313 Reserved labels: . . . none.
.314 Other restrictions: . . none.
.315 Designators
Decimal address: decimal number followed by D.
.316 Synonyms permitted: yes; EQU pseudo.

§ 171.

.32 Universal Labels

.321 Labels for procedures
Existence: . . . . . optional.
Formation rule
First character: . . alphameric.
Last character: . . alphameric.
Others: . . . . alphameric.
Number of characters: . . . 6 max.
.322 Labels for library routines: . . . . . . same as Procedures.
.323 Labels for constants: same as Procedures.
.326 Labels for variables: . . . . . same as Procedures.

.33 Local Labels: . . . . none.

.4 DATA

.41 Constants

.411 Maximum size constants

Machine form	External form
Integer	
Decimal:	none.
Octal:	4 octal digits.
Binary:	4 octal digits.
BCD:	alphameric.
Fixed numeric: . .	none.
Floating numeric:	none.
Alphabetic:	none.
Alphameric:	none.

.412 Maximum size literals: . . . . . . literals are used only in addresses.

.42 Working Areas

.421 Data layout: . . . . . specified in program.
.422 Data type: . . . . . . not required.
.423 Redefinition: . . . . . none.

.43 Input-Output Areas

.431 Data layout: . . . . . specified in program.
.432 Data type: . . . . . . not required.
.433 Copy layout: . . . . . none.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
Existence: . . . . . optional.
Number
OSAS: . . . . . . 97.
OSAS-A: . . . . . 134.
Example: . . . . . . ADM.
Comment: . . . . . add memory.
.512 Absolute
Existence: . . . . . optional.
Number
OSAS: . . . . . . 97.
OSAS-A: . . . . . 134.
Example: . . . . . . 3100.
Comment: . . . . . add memory.

.52 Macro-Codes: . . . . none.

.53 Interludes: . . . . . none.

.54 Translator Control

.541 Method of control
Allocation counter: . pseudo-ops.
Label adjustment: . . pseudo-ops.
Annotation: . . . . . see paragraph .544.
.542 Allocation counter
Set to absolute: . . . ORG, PRG, CON pseudos.
Set to label: . . . . EQU pseudo.
Step forward: . . . . BLR, BSS pseudos.
Step backward: . . . none.
Reserve area: . . . . none.
.543 Label adjustment
Set labels equal: . . EQU pseudo.
Set absolute value: EQU pseudo.
Clear label table: . . not possible.
.544 Annotation
Comment phrase: . . 32 char (card input). 50 char (tape input).
Title phrase: . . . . no special title phrase.

.6 SPECIAL ROUTINES AVAILABLE: . . . . see Sections :151, Problem Oriented Facilities, and :191, Operating Environment.

.7 LIBRARY FACILITIES

.71 Identity: . . . . no on-line library accessible; subroutines may be added for assembly following source statements.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . none.

.82 Pseudos

Code	Description
ORG:	sets location counter at beginning of assembly.
PRG:	sets location counter during assembly.
CON:	sets location for lower core storage during assembly.
BLR:	advances location counter, by a maximum of 64 (decimal) locations.
BSS:	same as BLR.
WAI:	stop assembly until operator re-start.
END:	terminates input on first pass; can specify program branch location.
EQU:	sets symbol equal to specified value.
REM:	permits statement of only remarks.
BNKX (160-A only):	specifies a particular core storage bank to loader.
SUPA:	suppress listable output.
SUPB:	suppress binary output. (normal assembly output).
BCD:	causes a contiguous string of characters in comments field to be assembled; 2 BCD char per computer word.

§ 171.

.82 Pseudos (Contd.)

Code	Description
BCDR:	as BCD except 1 per word.
FLX:	causes a contiguous string of characters in comments field to be assembled; 2 Flexowriter char per word.
FLXR:	as FLX except 1 per word.

.83 Interpretive: . . . . . none.

.84 Direct: . . . . all machine operation codes, described in Section :121, Instruction List.

MACHINE ORIENTED LANGUAGE: SICOM

§ 172.

.1 GENERAL

.11 Identity: . . . . SICOM Interpretive System.

.12 Origin: . . . . Scientific Computers, Inc., Minneapolis, Minn.

.13 Reference: . . . . SICOM Reference Manual, CDC Publication No. 515.

.14 Description

SICOM is an interpretive system that simulates on the binary CDC 160-A a slower pseudo computer with decimal addressing, floating point decimal arithmetic, 16 two-dimensional index registers, and a repertoire of 133 one-address instructions. Programs can be coded in the SICOM language or translated into SICOM from the INTERCOM 1000 interpretive language for the Bendix G-15. The INTERCOM-to-SICOM translators are described in Section 244:184. Operation and performance of the SICOM interpreter are covered in Section 244:192.

All computations except index register operations are done in the floating point mode. Each data item occupies four 160-A words, or two SICOM locations, and consists of sign, 10 decimal digit mantissa, and exponent.

Each instruction occupies two 160-A words, or one SICOM location, and consists of seven digits: one digit to specify an index register, two digits to specify the operation code, and four digits to specify the operand address. The use of numeric rather than mnemonic operation codes, which is quite common among interpretive languages, tends to increase the time required to learn and code in the system. In 160-A systems with the maximum 32,768 words of core storage, the SICOM addresses u000 through x999 are assigned to the top two banks; otherwise all SICOM addressing is decimal.

The 16 SICOM index registers are designated 0 through 9 and u through z. Each index register is divided into two sections, i and j, and each section consists of a base, a difference (or increment), and a limit. Instructions are provided to set any part of any register to a literal value, to increment or decrement either base by its associated difference and then compare the resulting base with the limit, to clear all index registers, and to transfer data between index registers and the accumulator. The contents of both the i base and the j base of the specified index register are added to the instruction address to form the effective operand address. This double indexing can greatly facilitate the processing of two-dimensional arrays.

.14 Description (Contd.)

Many SICOM instructions offer a choice of relative or absolute addressing. When the relative mode is selected (by an instruction), the instruction address is interpreted as being relative to the location of the instruction; e.g., the address 0025 would refer to a location 25 SICOM locations forward from the instruction that contained it. Use of the relative mode is essential in subroutines that must be relocatable; no means of relocating routines that use absolute addresses is provided in the SICOM system.

SICOM offers the choice of a variety of input-output media, including punched tape, punched cards, magnetic tape, typewriter, printer, and plotter. Numeric data can be in floating or fixed point decimal format. Alphameric data can be input, stored, compared, merged, and output - an unusual and valuable capability in an interpretive system.

The SICOM instruction repertoire includes such useful facilities as inverse divide and reverse subtract. Integer operands up to 9,999 in magnitude can be specified as literals in the address portion of arithmetic instructions. The common mathematical functions such as square root and log, which are built into the instruction repertoire of many interpreters, require transfers to standard subroutines in the SICOM system. User-coded subroutines in either SICOM or 160-A machine language can be added to the SICOM subroutine library.

.15 Publication Date: . . . . November, 1962 (Preliminary manual dated June, 1962).

.2 LANGUAGE FORMAT

.21 Diagram

LOC	K	OP	ADDR	NOTES

.22 Legend

LOC: . . . . specifies location of the instruction, using a 4-decimal-digit address; not punched on program tape.

K: . . . . specifies one of 16 index registers numbered 0-9 and u-x.

OP: . . . . specifies the operation to be performed, using 2 decimal digits. (In some cases K and ADDR also help to define the operation.)

ADDR: . . . . specifies an absolute address or an address relative to the command being executed, using 4 decimal digits; or specifies a 4-digit literal.

§ 172.

.22 Legend (Contd.)

NOTES: . . . . used for coding sheet documentation only.

.23 Corrections: . . . . . . no special provisions.

.24 Special Conventions

.241 Compound addresses: . none.
.242 Multi-addresses: . . . none.
.243 Literals: . . . . in certain operation codes, contents of the ADDR field are interpreted as a 4-digit literal operand.
.244 Special coded addresses: . . . . . . none; but in relative addressing mode (entered by special instruction) all addresses are relative to location of command being executed.

.3 LABELS: . . . . none; all operands are identified by their pseudo addresses in 4-digit decimal form. (Core storage banks 6 and 7, when installed are assigned addresses u000 through v999 and w000 through x999, respectively.)

.4 DATA

.41 Constants

.411 Maximum size constants

Machine form	External form
Integer:	none.
Fixed numeric:	none.
Floating numeric	
Decimal:	1 to 8 decimal digits; with point, minus sign, and e (for exponent) as required.
Octal:	not used.
Binary:	not used.
Alphameric:	any length; stored as 8 characters per block of 2 consecutive SICOM locations.

.412 Maximum size literals

Machine form	External form
Integer:	4 decimal digits; for index register operations only.
Fixed numeric:	none.
Floating numeric	
Decimal:	4 decimal digit integer.
Octal:	not used.
Binary:	not used.
Alphameric:	none.

.42 Working Areas

.421 Data layout: . . . . . . absolute addresses are used.
.422 Data type: . . . . implied by instruction; floating numeric or alphameric.

.43 Input-Output Areas

.431 Data layout: . . . . . . absolute addresses are used.
.432 Data type: . . . . implied by instruction: floating numeric or alphameric.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic: . . . . not permitted.
.512 Absolute
Existence: . . . . . . mandatory.
Number: . . . . 60.
Example: . . . . 30 means "add".
Comment: . . . . . . K and ADDR portions are used to specify variations of the 00 and 01 operation codes. See Paragraph .83 for complete instruction list.

.52 Macro-Codes: . . . . . none.

.53 Interludes: . . . . none.

.54 Translator Control: . . see Section 244:192.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: . . none.

.62 Special Functions

.621 Facilities: . . . . square root, log, exponential, sine, cosine, and arctangent are provided as standard SICOM subroutines.
.622 Method of call: . . . . . load into SICOM storage before use and enter via operation code 70.

.63 Overlay Control: . . . . none.

.64 Data Editing: . . . . . . performed automatically by the SICOM input and output instructions.

.65 Input-Output Control

.651 File labels: . . . . . . SICOM instructions are provided to write and search for magnetic tape file numbers.
.652 Reel labels: . . . . . . none.
.653 Blocking: . . . . by own SICOM coding.
.654 Error control: . . . . . automatic, by SICOM magnetic tape read and write instructions.

.66 Sorting: . . . . none.

.67 Diagnostics

.671 Dumps: . . . . no special routines; dumps can be readily coded in SICOM.
.672 Tracers: . . . . optional trace mode is an integral feature of SICOM; see Section 244:192.
.673 Snapshots: . . . . none.

§ 172.

.7 LIBRARY FACILITIES

.71 Identity: . . . . SICOM subroutine libraries.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.
.723 Private: . . . . yes.

.73 Storage Form: . . . . . punched tape.

.74 Varieties of Contents: . standard SICOM subroutines (square root, log, exponential, sine, cosine, arctangent), plus user-developed routines.

.75 Mechanism

.751 Insertion of new item: . add to subroutine master tape.
.752 Language of new item: . SICOM or 160-A machine language.
.753 Method of call: . . . . . load required routines at execution time.

.76 Insertion in Program: . each library routine is inserted once, as a closed subroutine. All addresses within a routine must be relative rather than absolute so the routine can be relocated.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . none.

.82 Pseudos: . . . . none.

.83 Interpretive

K	OP	ADDR	Operation
K	02	Y	Set i base.
K	03	Y	Set i difference.
K	04	Y	Set i limit.
*K	05	Y	Decrement i base.
*K	06	Y	Increment i base.
K	12	Y	Set j base.
K	13	Y	Set j difference.
K	14	Y	Set j limit.
*K	15	Y	Decrement j base.
*K	16	Y	Increment j base.
*K	20	Y	Load absolute value.
*K	21	Y	Load negative.
*K	22	Y	Load.
*K	23	Y	Inverse divide.
*K	24	Y	Divide.
*K	25	Y	Multiply.
*K	26	Y	Interchange.
*K	27	Y	Extract.
*K	30	Y	Add.
*K	31	Y	Subtract.
*K	32	Y	Add absolute value.
*K	33	Y	Reverse subtract.
*K	34	Y	Replace add.
*K	35	Y	Compare numeric.

.83 Interpretive (Contd.)

K	OP	ADDR	Operation
K	36	Y	Output floating point and tab.
K	37	Y	Output floating point and cr.
K	40	Y	Output fixed point and tab.
K	41	Y	Output fixed point and cr.
K	42	Y	Set fixed point output format.
K	43	Y	Output carriage returns and tabs.
K	44	Y	Output tabulating number.
K	45	Y	Output a command from memory.
K	46	Y	Write file number on Magnetic Tape.
K	47	Y	Search magnetic tape for File Number.
K	50	Y	Group Input.
K	51	Y	Single Input.
K	52	Y	Read Octal Tape.
K	53	Y	Alphanumeric Output.
K	54	Y	Load A.N.R.
*K	55	Y	Compare A.N.R.
*K	56	Y	Merge into A.N.R.
*K	57	Y	Extract A.N.R.
*K	60	Y	Jump if accumulator is Zero.
*K	61	Y	Jump if accumulator is Non-Zero.
*K	62	Y	Jump if accumulator is Positive.
*K	63	Y	Jump if accumulator is Negative.
*K	64	Y	Jump unconditionally.
*K	65	Y	Jump unconditionally.
*K	66	Y	Jump unconditionally.
K	67	Y	Jump unconditionally.
K	70	Y	Jump unconditionally.
*K	71	Y	Selective Jump one.
*K	72	Y	Selective Jump two.
*K	73	Y	Selective Jump one and two.
*K	74	Y	Jump to machine language Subroutines.
K	75	Y	Jump back relative.
*K	76	Y	A.N.R. to storage.
*K	77	Y	Accumulator to storage.
		00	No operation.
		01	Selective Stop 1.
		02	Selective Stop 2.
		03	Stop display 3.
		AD04	Stop display 4.
		05	Halt and gate input.
		06	Select relative mode.
		07	Select absolute mode.
		08	Select non-trace mode.
		09	Reset trade mode.
		10	Clear index registers.
		11	Select Flexowriter input.
		12	Select Flexowriter output.
		13	Select Typewriter input.
		14	Select Typewriter output.
		D16	Select printer.
		17	Select tape to printer.
K	00	0D18	Select magnetic tape drive.
		AD19	Backspace AD records.
K	00	0020	Write on magnetic tape.
K	00	0021	Read magnetic tape.
K	00	AD22	Index to accumulator.
K	00	AD23	Accumulator to index.
K	00	0024	Block copy.
K	00	0025	Block clear.
K	00	0027	Punch octal tape.
K	00	0028	Punch special tape.
		29	Read special tape.
		60	Return to Mark 60.
		61	Return to Mark 61.

§ 172.

.83 Interpretive (Contd.)

K	OP	ADDR	Operation
		62	Return to Mark 62.
		63	Return to Mark 63.
		64	Return to Mark 64.
		65	Return to Mark 65.
		66	Return to Mark 66.
		67	Return to Mark 67.
		70	Return to Mark 70 (S. R. Exit)
		71	Return to Mark 71.
		72	Return to Mark 72.
		73	Return to Mark 73.
		75	Output last location.
		D78	Set floating point output format.
		79	Punch stop, check and leader.
1	01	Y	Load positive constant.
2	01	Y	Load negative constant.
3	01	Y	Divide into constant.
4	01	Y	Divide by constant.
5	01	Y	Multiply by constant.

.83 Interpretive (Contd.)

K	OP	ADDR	Operation
6	01	Y	Add constant.
7	01	Y	Subtract constant.
8	01	Y	Subtract from constant.
9	01	Y	Shift accumulator.
X	01	Y	Start automatic computation.
Y	01	Y	Set address for start trace.
Z	01	Y	Set address for stop trace.

Where A. N. R. is the alphameric data register.
K is any SICOM index register.
Y is any SICOM storage location.
* denotes the address can be relative as well as absolute.

.84 Direct Codes: . . . . . none in SICOM; 160-A machine language subroutines can be entered using SICOM operation code 74.

MACHINE ORIENTED LANGUAGE: INTERFOR

§ 173.

.1 GENERAL

.11 Identity: . . . . INTERFOR.

.12 Origin: . . . . Control Data Corp. and Mr. Gordon Stanley, General Motors Corporation.

.13 Reference: . . . . INTERFOR Reference Manual, CDC Publication No. 512, September, 1962.

.14 Description

INTERFOR is an interpretive system that facilitates the coding of scientific and engineering problems by simulating on the 160-A a slower pseudo computer with a repertoire of 22 single-address instructions, including floating point arithmetic on operands consisting of a 33-bit signed binary fraction and a 10-bit signed binary exponent. The word size and instruction repertoire are largely compatible with the more powerful CDC 1604 and 1604-A.

Each INTERFOR storage location occupies four words of 160-A core storage and is assigned a four-digit octal address. An INTERFOR location can hold one data item or a pair of instructions. Each instruction consists of eight octal digits: two digits to specify the operation code; one digit to specify which (if any) of the six INTERFOR index registers shall be used to modify the operand address; one digit to specify a breakpoint halt, depending upon console switch settings; and four digits to specify either the base operand address or the operand itself.

INTERFOR programs can be coded directly in the octal format described above, or they can be written in symbolic form and assembled by FLAP, the INTERFOR assembly program. FLAP permits the use of three-character mnemonic operation codes, labels of up to eight characters, comments, and decimal constants. Input to FLAP can be on punched tape or cards. The binary object program is punched on tape, and a listable output showing both the symbolic and translated instructions can be punched on tape or listed by the 166 Printer. FLAP normally requires two passes for an assembly. If the available storage capacity is exceeded, a third pass is required. Symbol table capacity is approximately 500 labels. FLOADER is a special load routine for the binary program tapes produced by FLAP assemblies.

The INTERFOR interpretive system fits into storage bank 0 and leaves 337 INTERFOR locations, which are usually assigned to the external system subroutines such as square root, exponential, and sine-cosine. Banks 1, 2, and 3 (when installed) each provide 1,024 locations of INTERFOR storage which can hold the user's program and data. Bank switching is handled automatically by the interpreter. Core storage banks 4 through 7 cannot be addressed in the INTERFOR system.

The INTERFOR repertoire includes instructions to load or store a particular element of a matrix stored in columnar form. The starting location of the matrix and the row and column number of the desired element are specified in the instruction. The "equality search" and "threshold search" instructions search a list of operands in sequential locations and transfer control when an operand equal to or greater than the value in the accumulator is found. A conventional set of instructions is provided to load, increment, and test the six index registers.

Input and output operations in INTERFOR programs are handled by return jumps to standard subroutines rather than by direct operation codes. Data may be read in via the 167 Card Reader, the paper tape reader, or the typewriter. Each input subroutine converts one floating point data item from decimal to binary form and leaves the result in the accumulator. Data output may be via the paper tape punch, typewriter, or 166 Printer. Each output subroutine converts the data item in the accumulator to decimal form and outputs the item, followed by a tab or carriage return. No provision is made for magnetic tape input-output. The standard INTERFOR external subroutines are: arc tangent, sine, cosine, arc cosine, arc sine, power series expansion, exponential, square root, log, and plot. CDC 160-A machine language coding can be incorporated into INTERFOR programs by exiting from and re-entering the interpretive system via special instructions.

Execution times for INTERFOR programs are not available from the manufacturer. When an error is encountered, the interpreter halts, and the operator can initiate the type-out or punch-out of an error message consisting of an error code, the instruction word that caused the error, and its INTERFOR location.

The main advantages INTERFOR has over the SICOM interpretive system described in Sections 202:172 and 202:192 are the convenience of symbolic coding and the similarity of INTERFOR to machine language programming for the CDC 1604 and 1604-A. SICOM, on the other hand, offers a larger instruction repertoire, magnetic tape operations, alphameric data handling capabilities, and a trace mode.

.8 OPERATION CODES

.81 Macros: . . . . none.

§ 173.

.82 Pseudos (FLAP Assembly Routine)

REM:	identifies comments.
EQU:	assigns the value of an expression to a label.
ORG:	defines starting address of a block of INTERFOR instructions.
DEC:	identifies a decimal constant to be converted to binary form at load time.
BSS:	reserves a block of storage locations.
OCT:	identifies a signed octal constant.
END:	indicates end of symbolic program.

.83 Interpretive

Octal Code	FLAP Code	Operation
12	LDA	Load.
13	LAC	Load complement.
20	STA	Store.
22	AJP	Conditional jump.
30	FAD	Floating add.
31	FSB	Floating subtract.
32	FMU	Floating multiply.
33	FDV	Floating divide.
36	SSK	Storage skip.
50	ENI	Enter index.
51	INI	Increment index.
52	LIU	Load index, upper.
53	LIL	Load index, lower.
54	ISK	Index skip.
56	SIU	Store index, upper.
57	SIL	Store index, lower.
64	EQS	Equality search.
65	THS	Threshold search.
75	SLJ	Unconditional jump.
76	SLS	Unconditional stop.
34	MEL	Matrix element load.
35	MES	Matrix element store.

PROGRAM TRANSLATOR: OSAS/OSAS-A

§ 181.

.1 GENERAL

.11 Identity: . . . . One Sixty Assembly System. OSAS.

One Sixty-A Assembly System. OSAS-A.

.12 Description

OSAS and OSAS-A are two-pass translators. The version of the translator to be used in a given assembly can be a previously used translator which suits the job at hand, or can be specifically set up for the occasion. The master version exists on punched tape, and includes all input-output media subroutines which may be used during the translation. An input parameter entered into the processor specifies the media for the four input-output transfers which occur during assembly. These transfers provide for reading the source program , writing and reading back the intermediate output, and writing the object program and output to be listed. Only those subroutines which are required remain in storage along with the translator. Obtaining the desired form of the translator is considered Phase I of the assembly.

Phase II assembles the program. Pass I reads symbolic input from punched tape, magnetic tape, or cards. Intermediate output from Pass I can be recorded on paper tape of magnetic tape, and is read back in as the input for Pass II. Pass II generates assembled binary coding and a BCD-coded output list. Output to be listed can be recorded on paper or magnetic tape, or directly on a line printer. Assembled instructions are contained in groups of up to 71 words, in binary card column format.

The machine language output includes word count, starting address, and relocation instructions. This output can optionally include a checksum. If the object program output is on paper tape, this image is placed in six-bit characters, and the record is only as long as required. The card image, if placed on magnetic tape, is a fixed length of 160 BCD characters.

In the 160, the input-output subroutines are placed in the symbol table, which has room for 340 symbols; the maximum useful size is approximately 250 symbols because the symbol table area holds the input-output subroutines. In the 160-A the symbol table size is approximately 1,000 symbols.

A third pass will be required if both the list output and the assembled output are put on punched tape. Note that the assembler cannot produce a list directly by means of the 161 Typewriter, but can list on-line by means of the line printer.

.13 Originator: . . . . . . Control Data Corporation.

.14 Maintainer: . . . . . Control Data Corporation.

.15 Availability: . . . . . OSAS; March, 1963.
OSAS-A; November, 1962.

.2 INPUT

.21 Language

.211 Name: . . . . OSAS, OSAS-A.
.212 Exemptions: . . . . . none.

.22 Form

.221 Input media: . . . . . paper tape.
punched cards.
magnetic tape.
.222 Obligatory ordering: none.
.223 Obligatory grouping: none.

.23 Size Limitations

.231 Maximum number of source statements: no limit; programs can be segmented. Maximum number in core storage at one time is approximately 300.
.232 Maximum size source statements: . . . . . 79 char.
.233 Maximum number of data items: . . . . . depends on space available in symbol table (see Description).

.3 OUTPUT

.31 Object Program

.311 Language name: . . . relocatable binary machine code.
.312 Language style: . . . . up to 71 machine words, with word count, optional checksum, starting address for the words, and a code to indicate which words may be relocated. This format applies to 1 card, 1 block of 160 BCD char on mag tape, or to paper tape, except that paper tape record may be shorter according to word count.
.313 Output media: . . . . paper tape, punched cards, or magnetic tape.

.32 Conventions

.312 Standard inclusions: . . bank control card (OSAS-A), and transfer address card.

§181.

.33 Documentation

Subject	Provision
Source program:	optional; may print, or may prepare tape or cards, or suppress output altogether.
Object program:	optional; see source program entry above.
Storage map:	none.
Restart point list:	none.
Language errors:	using listable output.

.4 TRANSLATING PROCEDURE

.41 Phases and Passes

Phase I: . . . . specify input-output media. Read in assembly program; set it up for job at hand. Optional output of this version of assembler for future use.

Phase II

Pass I: . . . . read symbolic input.
store condensed version of each statement in core storage as intermediate output of assembler.
translate op codes.
form symbol table.
generate binary intermediate output if core storage area is too small.

Pass II: . . . . . . scan intermediate output and generate binary object program.
output listable and assembled programs.

Pass III: . . . . . . optional; used to output listable object program on paper tape.

.42 Optional Mode

.421 Translate: . . . . . . yes.
.422 Translate and run: . . no.
.423 Check only: . . . . . no.
.424 Patching: . . . . . . no; reassemble.
.425 Updating: . . . . . . no. Source program paper tape can be updated in a separate run using program A 2.01 A, Paper Tape Edit.

.43 Special Features

.431 Alter to check only: no.
.432 Fast unoptimized translate: . . . . . no.
.433 Short translate on restricted program: no.

.44 Bulk Translating: . . . yes.

.45 Program Diagnostics: by incorporating separate routines.

.46 Translator Library

.461 Identity: . . . . . . none for direct access; add any routines desired following source program.

.5 TRANSLATOR PERFORMANCE

.51 Object Program Space

.511 Fixed overhead: . . . . none.
.512 Space required for each input-output file: . . as coded.
.513 Approximate expansion of procedures: . . . 1 complete instruction per elementary statement.

.52 Translation Time

.521 Normal translating: . . approximately 75 msec per statement using low-density magnetic tape. In a card or paper tape system, speed is limited by these input-output devices.

.53 Optimizing Data: . . . none.

.54 Object Program Performance: . . . . . essentially as good as hand coding (***).

.6 COMPUTER CONFIGURATIONS

.61 Translating Computer

.611 Minimum configuration: . . . basic 160 (4,096 words of storage) or 160-A (8,192 words of storage) with paper tape input-output.
.612 Larger configuration advantages: . . . . card, mag tape input-output for faster speed. Using mag tape on either computer for storing intermediate output, pass II is initiated automatically.
160-A may have additional storage added for larger symbol table.

.62 Target Computer

.621 Minimum configuration: . . . punched tape systems as above.
.622 Usable extra facilities: card, magnetic tape input-output.
larger core storage.

(***) Estimate by editorial staff. See 1:010:400

§181.

.7 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Missing entries:	none.	
Unsequenced entries:	none.	
Duplicate names:	check	error flag in listing.
Improper format:	none.	
Incomplete entries:	check for undefined symbols	error flag in listing.
Target computer overflow:	none.	
Inconsistent program:	none.	
Direct address mode assigned too large an address:	check	range error flag in listable output.
Relative address mode has modifier out of range:	check	range error flag in listable output, and E field of instruction cleared to zero.
Illegal op code:	check	error flag in listing.
Illegal character:	check	error flag in listing.
E field of instruction out of range:	check	error flag in listing.
Location out of range using lower core counter (CON):	check	error flag in listing.

.8 ALTERNATIVE TRANSLATORS: none.

PROGRAM TRANSLATOR: 160-A FORTRAN

§ 182.

.1 GENERAL

.11 Identity: . . . . CDC 160-A FORTRAN.

.12 Description

Summary

The 160-A FORTRAN compiler produces a pseudo object language in core storage which is ready to be executed under control of an interpreter routine, also stored in core storage. The compiler equipment required is a basic 160-A computer (8,192 words of storage), two magnetic tape units, and an input unit for the source program (which can be on punched tape, cards, or magnetic tape.) It is possible to substitute the CDC 167 card reader and punched tape for the two magnetic tape units.

The COMMON statement can provide data linkages between programs and subprograms. However, in order to be used together, the programs and subprograms must be compiled together.

Forty-seven types of error codes can be indicated via listable output during compilation. If an error occurs, compilation continues but no object code is created.

Operation of the Translator

Compilation is accomplished in two passes. Pass I reads the translator program from one of the magnetic tape units, reads the source statements, makes records of names, subroutines, etc., and produces an intermediate output on the second magnetic tape unit. Intermediate processing follows based on information extracted from the source program. This processing includes generating coding for indexing, and computing storage space required for interpretive and library routines. Pass II loads the intermediate program into core storage and produces the pseudo object language. Unassigned memory references are completed, library routines are inserted, and the interpretive routine is loaded from the first magnetic tape unit.

At this point the program in core storage can either be executed or be written out for later use.

Optional Compiler Outputs

a. Memory map.

b. Reloadable object program, in pesudo object language.

Size Limitations

The interpretive routine, library functions, table for allocation of variable addresses, and input-output subroutines must all be in core storage at execution

.12 Description (Contd.)

time. Approximately 4,000 words of storage are required, including provision for format control and Boolean operations; but not including the table of addresses of variables. Each floating point variable requires three words of storage, and each fixed point constant or variable requires two.

These fixed storage requirements are not as severe for the 160-A computer as for the 160. The largest matrix which can be inverted in the basic 160-A (8,192 words of core storage) is 33 by 33, and this matrix requires approximately 3,300 words of storage. The inversion routine requires approximately 500 words of storage.

The 169 Auxiliary Memory Unit provides up to 24,576 additional words of core storage.

Compiling Time

The only available compiling times are those for compiling the matrix inversion routine, which has 66 statements. The program contains 11 DO statements. These times (supplied by the manufacturer) are 37 seconds for a magnetic tape system and 5 minutes (estimated) for a card/paper tape system. The object program is in core storage ready for interpretive execution. Model 163 magnetic tape units (30 KC) and the Model 167 card reader (250 cards per minute) were used.

The manufacturer claims an average compiling speed of 125 statements per minute for 160-A FORTRAN.

Timing of Execution of Pseudo Object Program

Interpretive execution times of object programs are available for matrix inversion and for basic operations. The subroutine for matrix inversion inverts a 10 by 10 matrix in 53 seconds, and a 20 by 20 matrix in 7 minutes. The estimate for a 30 by 30 matrix using 160-A FORTRAN was not given, but it is probably close to the time estimated for 160 FORTRAN-A (20 minutes).

Timing of basic operations, executed interpretively, is listed below in comparison with timing of subroutines by themselves.

	160-A FORTRAN Interpretation	Subroutine Alone
DO loop control:	1.4 msec.	
Fixed point add:	4.5 msec	0.02 msec.
Floating point add (subroutine):	7.4 msec.	4 msec.
Floating point multiply (subroutine):	18 msec.	14 msec.
Floating point divide (subroutine):	26 msec.	19 msec.

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.12 Description (Contd.)

Timing of Execution of Pseudo Object Program (Contd.)

	160-A FORTRAN Interpretation	Subroutine Alone
Natural log function:	150 msec.	200 msec.
Exponential function:	180 msec.	380 msec.
Exponentiation:	270 msec.	71 msec.
Sine function:	167 msec.	123 msec.
Square root:	100 msec.	90 msec.
Single subscripted floating add C(I) = C(I) + C(I + 1):	15 msec.	
Double subscripted floating add A(I, J) = A(I, J) + A(I, J + 1):	32 msec.	
Triple subscripted floating add B(I, J, K) = B(I, J, K) + B(I, J, K + 1):	80 msec.	

.12 Description (Contd.)

Library

Eight standard functions are supplied for use by the program. Other functions may be written as subroutines and compiled with the source program. The number of subroutines is unrestricted, except by the core storage available. The limit is seven in 160 FORTRAN-A. A system tape editing routine is available which can add routines to the library itself.

Computer Configurations

Unlike 160 FORTRAN, which is limited to punched tape for compiling and execution, 160-A FORTRAN permits the use of the following magnetic tape, card, line printer, and punched tape equipment:

CDC 163 or 1607 Magnetic Tape Unit (30 KC)
CDC 167 Card Reader (250 cards/minute)
IBM 088 Collator (650 cards/minute)
CDC 170 Card Punch (100 cards/minute)
CDC 1612 Line Printer (1,000 lines per minute, numeric)
CDC 166-2 Line Printer (150 lines per minute).

PROGRAM TRANSLATOR: INTERCOM

§ 183.

.1 GENERAL

.11 Identity: . . . . Double Precision INTERCOM Translator.
Single Precision INTERCOM Translator.

.12 Description

These routines translate programs coded in the popular INTERCOM interpretive language for the Bendix G-15 computer into the SICOM interpretive language for the CDC 160-A. The SICOM language and interpretive system are described in Sections 244:172 and 244:192 respectively.

Two versions of the translator have been developed to accommodate programs written in either single or double precision INTERCOM 1000. The single precision version can also translate programs coded in INTERCOM 500X.

An INTERCOM source program tape must be punched from the original coding sheets on a Flexowriter with 160-A coding; G-15 program tapes cannot be directly used. Output from the one-pass translators is a program tape in SICOM language. Ambiguities which may arise in the translation are preceded by a "c" on the output tape, denoting a need for analysis of the INTERCOM program and correction of the SICOM object program. All data tapes must be manually repunched because INTERCOM uses an "excess 50" exponent notation while SICOM uses straight powers of 10; e.g., 48.123 in INTERCOM is .123e-2 in SICOM.

A general one-to-one correspondence exists between INTERCOM and SICOM instructions, but use of certain INTERCOM commands and facilities necessitates the inclusion of closed SICOM subroutines to perform the corresponding functions. The translator automatically includes the following SICOM subroutines wherever their G-15 counterparts are called for: square root, log-exponential, sin-cos, arctan, magnetic tape.

.13 Originator: . . . . Scientific Computers, Inc., Minneapolis, Minn.

.14 Maintainer: . . . . . . Control Data Corp., Minneapolis, Minn.

.15 Availability: . . . . . . November, 1962.

OPERATING ENVIRONMENT: GENERAL

§ 191.

.1 GENERAL

.11 Identity: . . . . no integrated supervisor available.

.12 Description

No integrated supervisor is available for the 160/160-A systems.

Library subroutines are loaded at translation time under operator control.

.13 Availability: . . . . . . library routines described are available now.

.14 Originator: . . . . Control Data Corporation and members of SWAP Users' Group.

.15 Maintainer: . . . . . . Control Data Corporation and SWAP.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . none.

.212 Independent programs: on punched tape, cards, or magnetic tape.

.214 Master routines: . . . . punched tape, cards, or magnetic tape.

.22 Library Subroutines: . by operator selection; loaded at translation time.

.23 Loading Sequence: . . . manually controlled.

.3 HARDWARE ALLOCATION: . . . . fixed.

.4 RUNNING SUPERVISION: . . . . console alarms (display of halt locations).

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . TRACK; SWAP program listing G1.01. This routine provides a record on punched tape of initial and terminal addresses of all conditional branch instructions of a 160 program. TRACK is not used with the 160-A computer because of conflicting storage allocation conventions. Storage required is 358 words. Average program running speed is 75 instructions per second. TRACK is called in by operator as needed.

.512 Snapshots: . . . . none.

.52 Post Mortem: . . . . . several separate routines are provided to dump core storage to magnetic tape, paper tape, typewriter, or 1612 printer. Printed output is in octal form.

.6 OPERATOR CONTROL: as incorporated in user's program. Error halts indicate address at console.

.7 LOGGING: . . . . as incorporated in user's program.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: computer with minimum core storage, paper tape reader, and punch. This is also the minimum SWAP computer.

.812 Usable extra facilities: punched cards, magnetic tape.

.813 Reserved equipment: . none.

.82 System Overhead

.821 Loading time: . . . . . (all times approximate)
OSAS, OSAS-A - 45 sec.
160 FORTRAN and 160 FORTRAN-A - 70 sec in 3 parts.
AUTOCOMM - 45 sec.
INTERFOR - 20 sec.
160-A FORTRAN - 5 sec in 2 parts (magnetic tape).

.822 Reloading frequency: . only FORTRAN must be reloaded.

.83 Program Space Available: . . . . . . OSAS-OSAS-A, all of core.
160 FORTRAN, 2,240 for object code and data.
160 FORTRAN-A, 1,560 for object code, 4,000 for data.
160-A FORTRAN, 5,000 for object code and data on minimum machine. Up to 29,000 available using 169 Auxiliary Memory Unit (core storage).

§ 191.

.83 Program Space Available (Contd.): . . AUTOCOMM, 4,000 for program, 4,000 to 28,000 for data.
INTERFOR, 1,712 INTERFOR words (1 INTERFOR word = 4, 160-A words) for data and program on minimum machine. Up to 3,760 INTERFOR words are available.

.84 Program Loading Time: ?

OPERATING ENVIRONMENT: SICOM

§ 192.

.1 GENERAL

.11 Identity: . . . . SICOM Interpretive System.

.12 Description

This routine interprets and executes programs written in the SICOM language, described in Section 244:172. SICOM programs can be run on a minimum CDC 160-A system (8K core store, paper tape reader, and punch), but operation is much simpler if a 161 Typewriter is available. All standard 160-A input-output devices can be utilized.

The interpretive routine occupies all 4,096 locations of core storage bank 0 and the top 96 locations of bank 1. The remaining 4,000 words of bank 1 are available to hold the user's program, subroutines, and data. Each decimally addressed SICOM pseudo location occupies two 160-A words, so the minimum 160-A provides 2,000 SICOM locations. Each instruction requires one SICOM location and each data item requires two locations. Each additional 4,096-word bank of core storage increases the number of available SICOM locations by 2,000; a 32K 160-A would have 14,000 SICOM locations, with addresses u000 through x999 assigned to the top 4,000 locations.

SICOM programs are normally prepared and stored on punched tape. Because there are no parity checks on punched tape operations, the system includes input and output tape verification operations. Verification involves rereading the tape and comparing two check sums. Library subroutines must be added to the program tape or loaded separately each time the program is run. Programs can be relocated in core storage only if all addressing is in the relative mode. The relative mode is therefore standard for general-purpose subroutines, but its use in complex programs is very inconvenient because the relative address of a particular data item varies with the location of the instruction referencing it.

SICOM has a convenient built-in trace mode that facilitates program testing and debugging by printing. when desired, each SICOM instruction, its location, and the contents of the pseudo arithmetic register after execution of the instruction.

Execution times for SICOM instructions are not available from the manufacturer.

.13 Availability: . . . . . . November, 1962.

.14 Originator: . . . . Scientific Computers, Inc., Minneapolis, Minn.

.15 Maintainer: . . . . . . Control Data Corp., Minneapolis, Minn.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . none.
.212 Independent programs: punched tape.
.213 Data: . . . . punched tape, punched cards magnetic tape or typewriter
.214 Master routines: . . . . punched tape.

.22 Library subroutines: . punched tape.

.23 Loading Sequence: . . . manually controlled.

.24 Interpreter Input

.241 Language
Name: . . . . SICOM.
Exemptions: . . . . . none.
.242 Form: . . . . punched tape.

.3 HARDWARE ALLOCATION

.31 Storage: . . . . programs can be relocated only if all addresses are relative rather than absolute.

.32 Input-Output Units: . . selected by instructions.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: none.

.42 Multi-programming: . . none.

.43 Multi-sequencing: . . . none.

.44 Errors, Checks and Action

Error	Check or Interlock	Action
Loading input error:	reread, using "verify input tape" instruction.	error stop if check sums do not agree.
Allocation impossible:	none.	
In-out error - single:	parity check	try again.
In-out error - persistent:	parity check	transfer to user-coded error routine.
Storage overflow:	none.	
Invalid index value:	check	stop; display error code.
Arithmetic overflow:	check	stop; display error code.
Underflow:	none.	
Invalid operation:	check	stop; display error code.
Improper format:	checks	stop; display error code.
Invalid address:	check	stop; display error code.

.45 Restarts: . . . . no provisions.

§ 192.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . trace mode can be entered and emerged from upon execution of instructions in specific locations selected by the "start trace" and "stop trace" instructions. Jump switch 4 inhibits all tracing. When tracing, the following information is output on the specified device after execution of each SICOM instruction: the location of the instruction, the instruction itself, and the contents of the pseudo arithmetic register (A.R.).

.512 Snapshots: . . . . none.

.52 Post Mortem: . . . . . none.

.6 OPERATOR CONTROL

.61 Signals to Operator: . . console displays (4 octal digits) or programmed typeouts.

.62 Operator Decisions: . . keyboard data entry or Selective Jump switch settings.

.7 LOGGING: . . . . as incorporated in user's program.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: Minimum 160-A (8,192 words of core storage, punched tape reader and punch).

.812 Usable extra facilities: 161 Typewriter (recommended for ease of system operation), 167 Card Reader, 166 Line Printer, 163 Magnetic Tape Unit, 165 Plotter. 603 and 606 Magnetic Tape Units will be available in the future.

.813 Reserved equipment: . 4,192 core storage locations.

.82 System Overhead

.821 Loading time: . . . . . ?

.822 Reloading frequency: . SICOM master routine can be kept in working storage.

.83 Program Space Available: . . . . . . $I + 2D \leq 2{,}000(B - 1)$, where I is number of instructions, D is number of data items, and B is number of 4,096-word core storage banks.

.84 Program Loading Time: ?

.85 Program Performance: ?

NOTES ON SYSTEM PERFORMANCE

§ 201.

.1 GENERALIZED FILE PROCESSING

Because CDC 160 applications have been on scientific problems, generalized file processing problems A, B, C, and D have not been timed. The 160 is used for off-line card-to-tape and tape-to-printer transcriptions, and these proceed at maximum card and printer speeds.

.2 SORTING

Sort routine Sort 3X is described in Problem Oriented Facilities, Section 244:151.13.

.3 MATRIX INVERSION

The standard estimate of the Users' Guide, which is based on the time for floating point cumulative multiplication, was used. Configuration IX uses floating point subroutines and Configuration X uses the 168-2 Floating Point Arithmetic Unit. CDC's standard routine for floating point subroutine matrix inversion is also timed.

.4 GENERALIZED MATHEMATICAL PROCESSING

Both double precision fixed point coding using the 168-1 Fixed Point Arithmetic Unit and floating point subroutines are timed for Configuration IX, with output via the typewriter. Configuration X is timed using subroutines and the 168-2 Floating Point Arithmetic Unit, with output via the paper tape punch. Input to both systems is via the paper tape reader.

.5 GENERALIZED STATISTICAL PROCESSING

Fixed point machine coding is used. Input is read by the paper tape reader; therefore, time for both configurations is the same.

CDC 160-A
SYSTEM PERFORMANCE

CDC 160-A SYSTEM PERFORMANCE

WORKSHEET DATA TABLE 2

Worksheet	Item			Configuration IX	IX	IX, X	X	Reference
5	Fixed/Floating point			Fixed	Floating		Floating	
	Unit name	input		Paper Tape Reader	Paper Tape Reader		Paper Tape Reader	
		output		161 Typewriter	161 Typewriter		Paper Tape Punch	
	Size of record	input		80 digits	120 digits		120 digits	
		output		80 digits	120 digits		130 digits	
Standard Mathematical Problem A	m. sec/block	input	T1	228	343		343	4:200.413
		output	T2	12,000	18,000		1,180	
	m. sec penalty	input	T3	228	343		343	
		output	T4	12,000	18,000		1,180	
	m. sec/record		T5	26	90 (***)		90 (***)	
	m. sec/5 loops		T6	60	665		90	
	m. sec/report		T7	155	618 (***)		618 (***)	
7	Unit name					Paper Tape Reader		
	Size of block					60 digits		
	Records/block		B			1		
Standard Statistical Problem A	m. sec/block		T1			171		4:200.512
	m. sec penalty		T3			171		
	C. P.	m. sec/block	T5			0.220		
		m. sec/record	T6			---		
		m. sec/table	T7			0.667		

(***) Estimate. See 1:010.4.

SYSTEM PERFORMANCE

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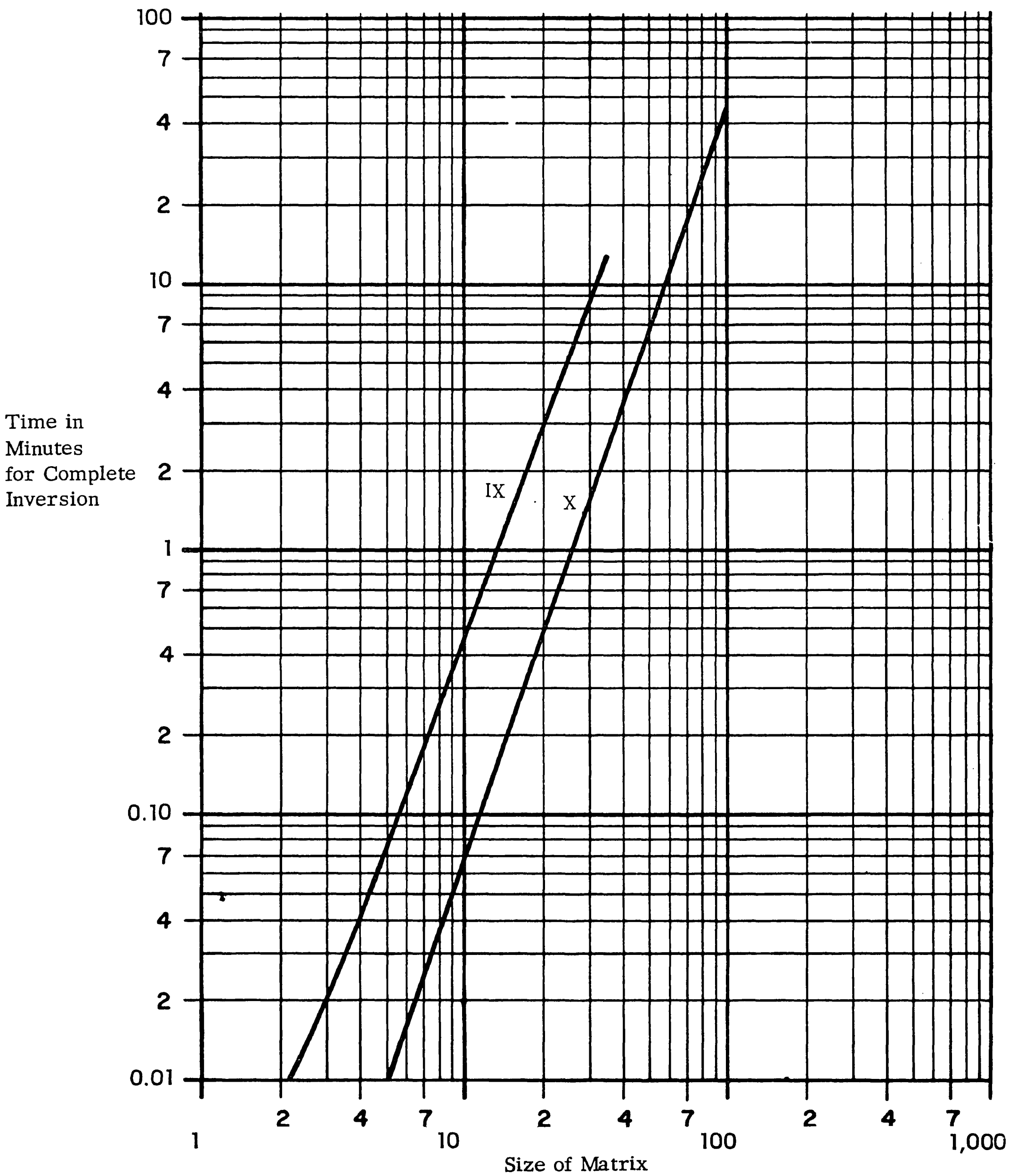
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic Parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing Basis: . . . . . using estimated procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . see graph below.



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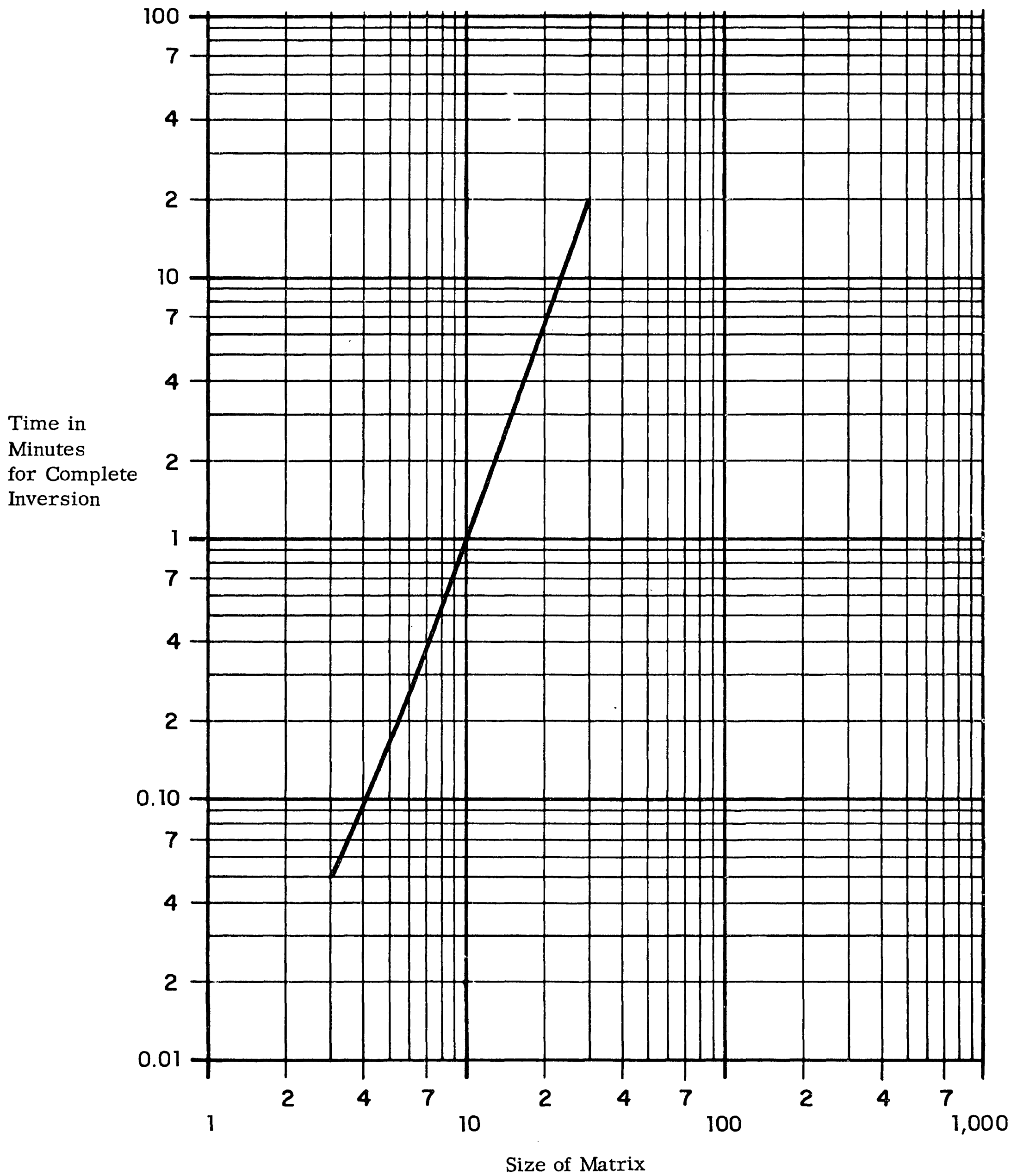
.32 I1.06 Routine

.321 Basic Parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.322 Timing Basis: . . . . . subroutine from SWAP listing.

.323 Graph: . . . . see graph below.



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.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

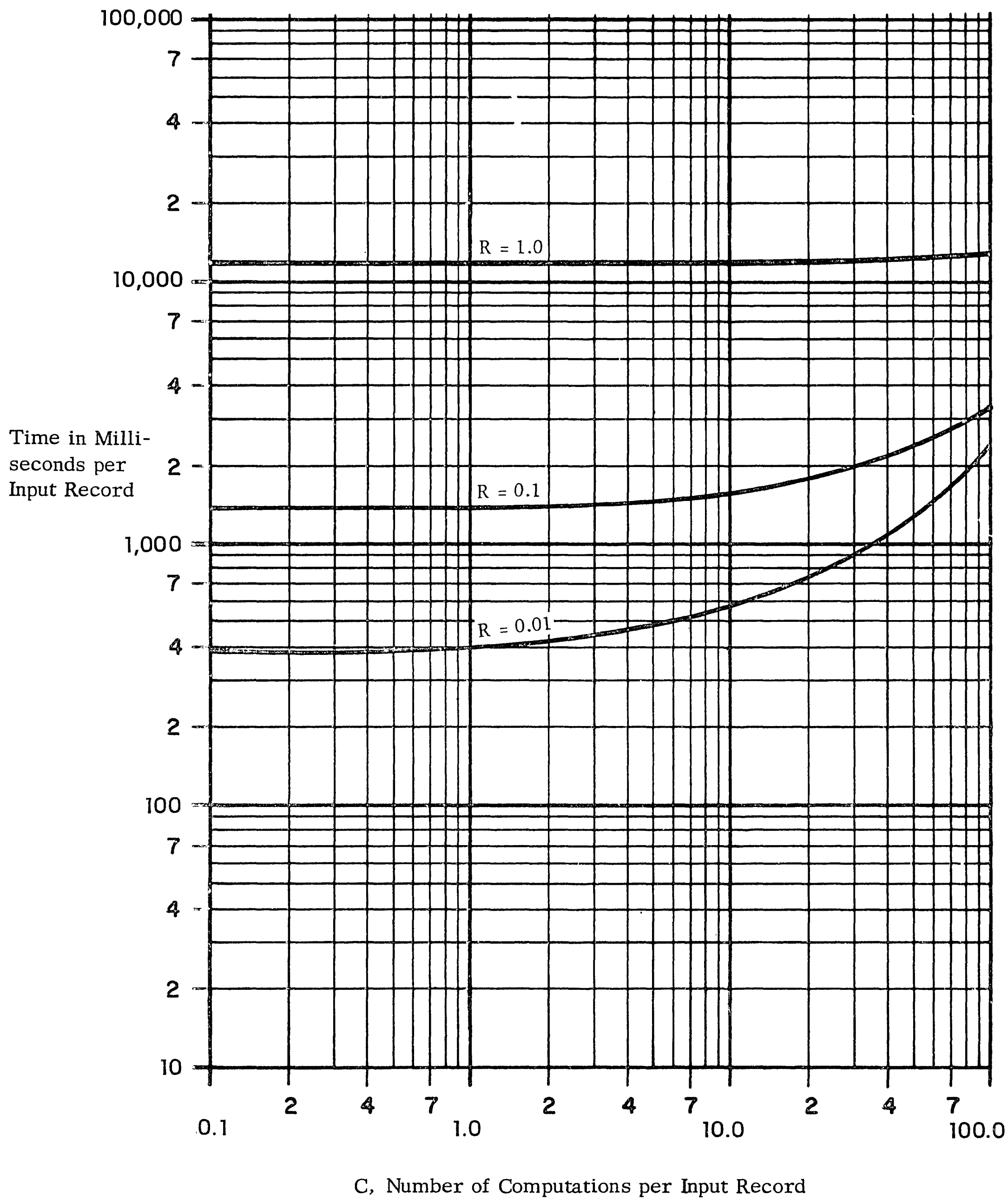
.412 Computation: . . . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.413 Timing basis:. . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . see graph below.

CONFIGURATION IX; DOUBLE LENGTH(6.6 DIGIT PRECISION); FIXED POINT

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



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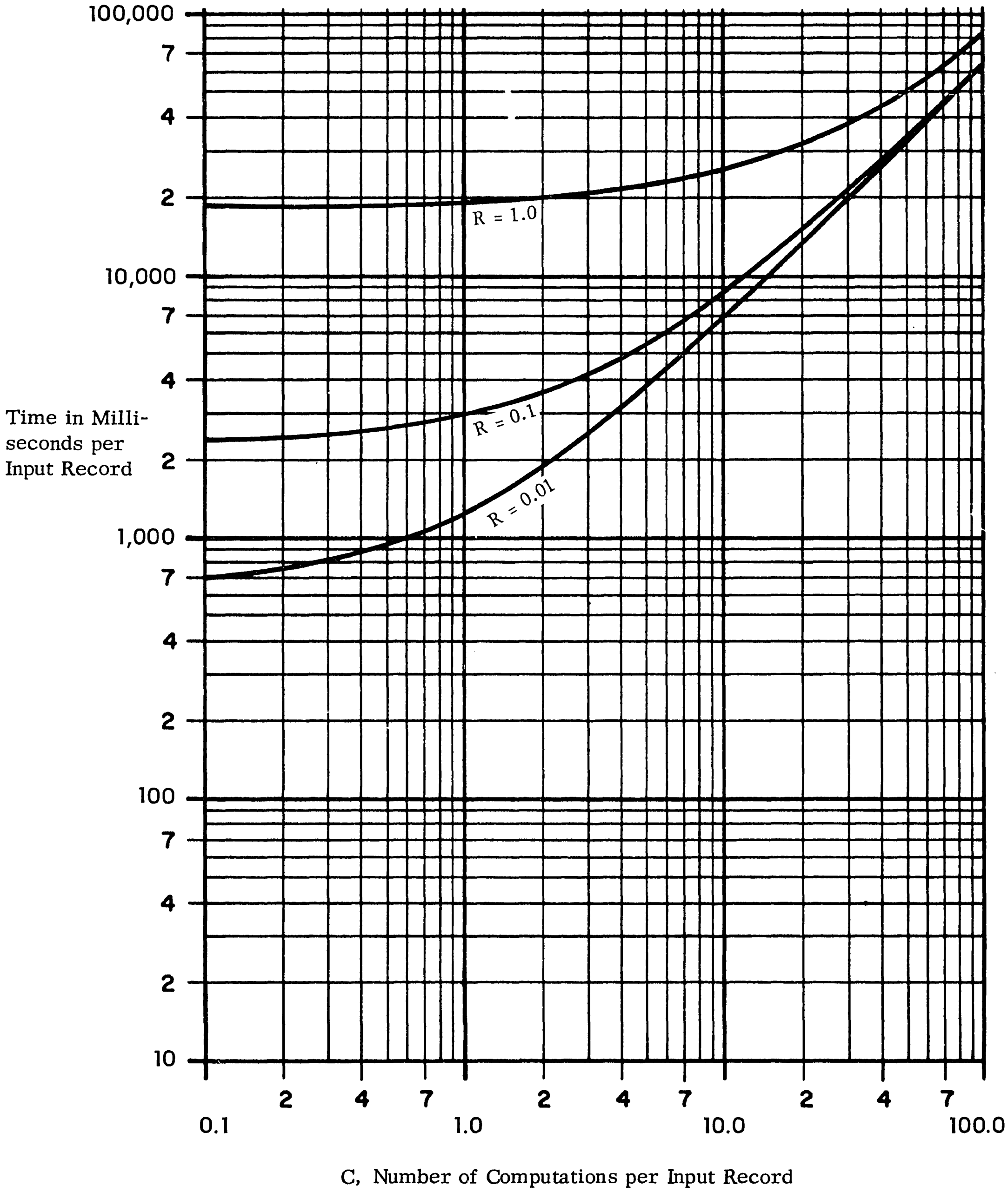
.415 Graph: . . . . see graph below.

CONFIGURATION IX; SINGLE LENGTH (8 & 2 DIGIT PRECISION); FLOATING POINT

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



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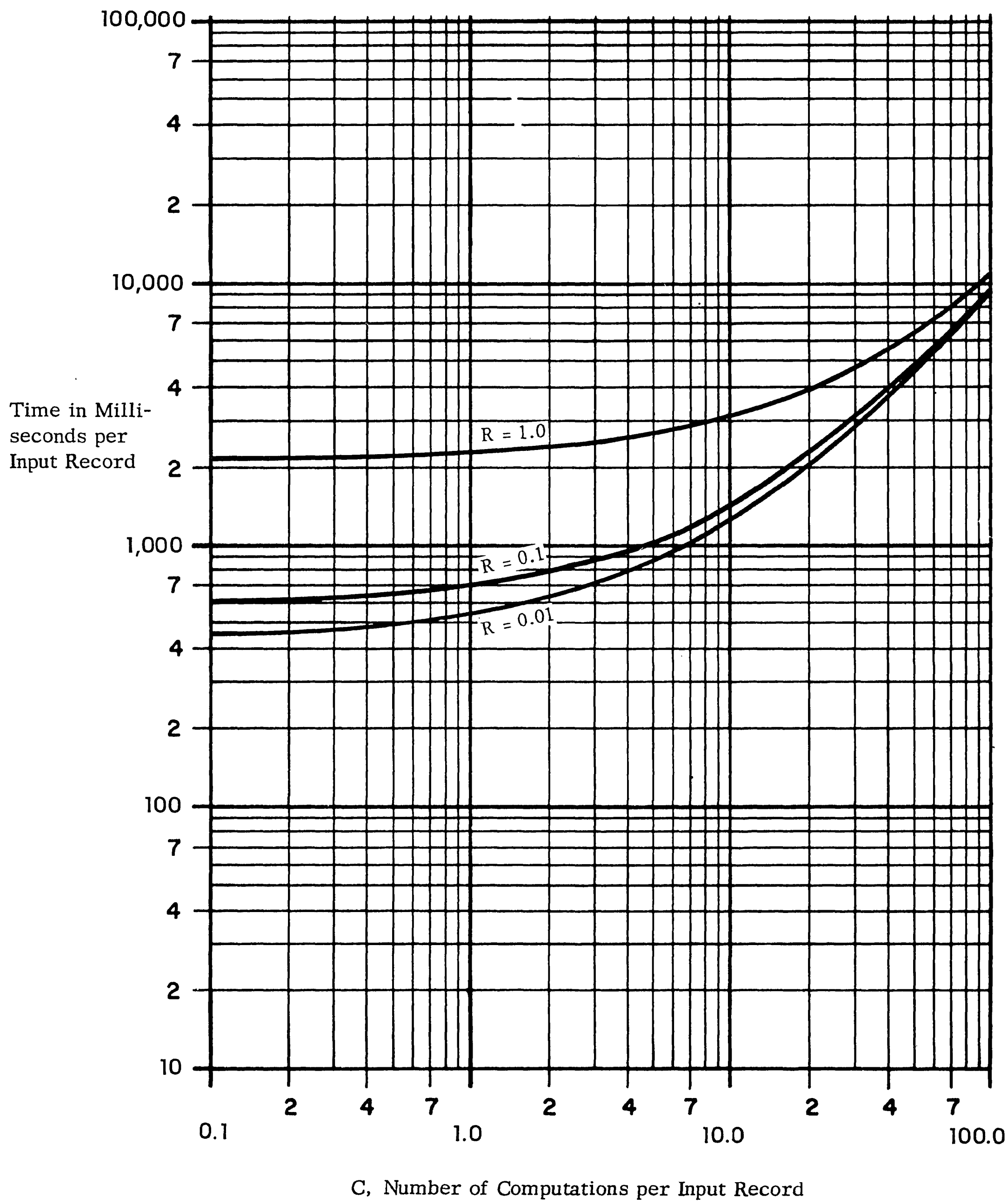
.416 Graph: . . . . see graph below.

CONFIGURATION X; SINGLE LENGTH (8 & 2 DIGIT PRECISION); FLOATING POINT

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



§ 201.

.5 GENERALIZED STATISTICAL PROCESSING

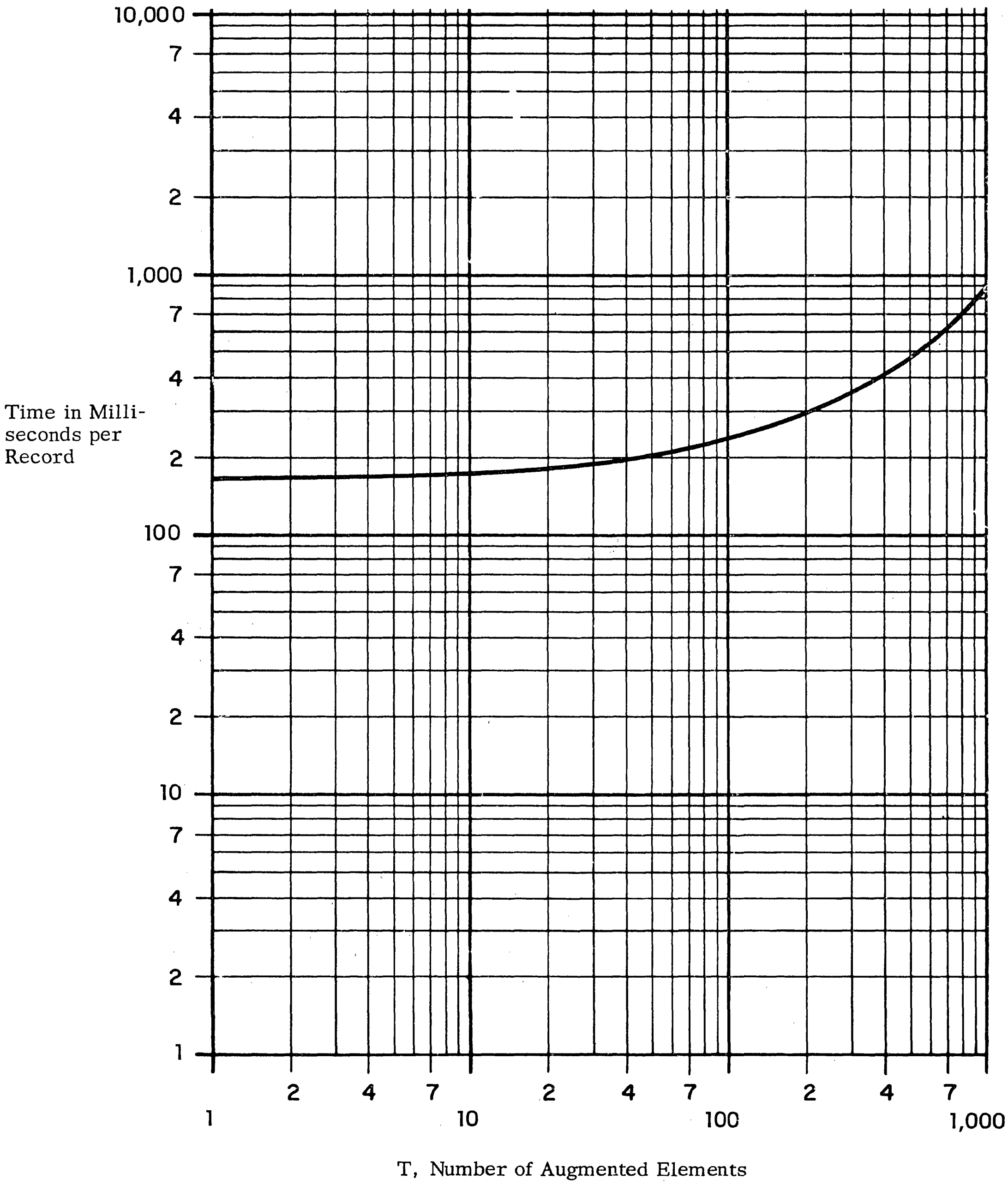
.51 Standard Statistical Problem A Estimates

.511 Record size: . . . . . . thirty 2-digit integral numbers.

.512 Computation: . . . . . augment T elements in cross-tabulation tables.

.513 Timing basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.513.

.514 Graph: . . . . see graph below.



CDC 160-A
PHYSICAL CHARACTERISTICS

CDC 160-A PHYSICAL CHARACTERISTICS

		Processor	Paper Tape Reader	Paper Tape Punch	Fixed Point Arithmetic Unit	Fixed Point Arithmetic Unit	Auxiliary Memory Unit			Card Reader
IDENTITY	Unit Name	Processor	Paper Tape Reader	Paper Tape Punch	Fixed Point Arithmetic Unit	Fixed Point Arithmetic Unit	Auxiliary Memory Unit			Card Reader
IDENTITY	Model Number	160-A	350	BRPE-11	168-1	168-2	169-1	169-2	169-3	167
PHYSICAL	Height × Width × Depth, in.	36 × 62 × 30	10 × 12 × 9		29 × 18 × 30	29 × 18 × 30	43 × 48 × 20			30 × 19 × 41
PHYSICAL	Weight, lbs.	810	25		290	340	600 to 800			210
PHYSICAL	Maximum Cable Lengths	75 data 100 power	Part of 160	Part of 160						
ATMOSPHERE	Storage Ranges — Temperature, °F.									
ATMOSPHERE	Storage Ranges — Humidity, %									
ATMOSPHERE	Working Ranges — Temperature, °F.	80 max			80 max	80 max	80 max			80 max
ATMOSPHERE	Working Ranges — Humidity, %	40 - 60			40 - 60	40 - 60	40 - 60			40 - 60
ATMOSPHERE	Heat Dissipated, BTU/hr.	7,860			2,900	4,200	4,700	5,600	6,500	630
ATMOSPHERE	Air Flow, cfm.									
ATMOSPHERE	Internal Filters	Yes	No		Yes	Yes	Yes			No
ELECTRICAL	Voltage — Nominal	115	115		115	115	115			115
ELECTRICAL	Voltage — Tolerance	10%					10%			10%
ELECTRICAL	Cycles — Nominal	60	60		60	60	60			60
ELECTRICAL	Cycles — Tolerance	3								
ELECTRICAL	Phases	1			1	1	1			1
ELECTRICAL	Load KVA	1.8	0.1		0.9		1.4	1.6	2.1	0.2
NOTES										

CDC 160-A PHYSICAL CHARACTERISTICS (Contd.)

			Card Punch Adapter	Line Printer	Typewriter	Incremental Plotter	Line Printer	Magnetic Tape Unit	Tape Unit Controller	Magnetic Tape Unit	Tape Unit Controller	Card Reader Punch Control		Card Read/ Punch		Magnetic Tape Unit	Magnetic Tape Unit
IDENTITY	Unit Name		Card Punch Adapter	Line Printer	Typewriter	Incremental Plotter	Line Printer	Magnetic Tape Unit	Tape Unit Controller	Magnetic Tape Unit	Tape Unit Controller	Card Reader Punch Control		Card Read/ Punch		Magnetic Tape Unit	Magnetic Tape Unit
IDENTITY	Model Number		170	166-2	161	165	1612	603	162-1	606	162-2	1610-A		1609		163	164
PHYSICAL	Height × Width × Depth, in.		29 × 18 × 30	41 × 35 × 19	38 × 30 × 30	47 × 18 × 14	56 × 72 × 31	72 × 28 × 33	29 × 18 × 30	72 × 28 × 33	29 × 18 × 30	43 × 20 × 48		51 × 40 × 26		68 × 27 × 28	68 × 27 × 28
PHYSICAL	Weight, lbs.		240	850	350	190	890	800	290	800	340	600		775		690	690
PHYSICAL	Maximum Cable Lengths																
ATMOSPHERE	Storage Ranges	Temperature, °F.															
ATMOSPHERE	Storage Ranges	Humidity, %															
ATMOSPHERE	Working Ranges	Temperature, °F.	80 max	80 max			70 max	80 max	80 max	80 max	80 max	70 max		70 max			
ATMOSPHERE	Working Ranges	Humidity, %	40 - 60	40 - 60			40 - 60	40 - 60	40 - 60	40 - 60	40 - 60	40 - 60		40 - 60			
ATMOSPHERE	Heat Dissipated, BTU/hr.		2,750	7,500	2,300	500	6,400	10,000	2,400		4,200	4,000		5,680		9,500 1st unit 6,500 each add'l	5,500 1st unit 2,500 each add'l
ATMOSPHERE	Air Flow, cfm.											800		800			
ATMOSPHERE	Internal Filters		Yes	Yes	Yes	No			Yes		Yes	Yes		Yes		Yes	Yes
ELECTRICAL	Voltage	Nominal	115	115	115	120	115	115	115	115	115	208	115	208	208	115	115
ELECTRICAL	Voltage	Tolerance	10%					5%	10%	5%							
ELECTRICAL	Cycles	Nominal	60	60	60	60	60	60	60	60	60	400	60	400	60	60	60
ELECTRICAL	Cycles	Tolerance	3														
ELECTRICAL	Phases		1	1	1	1	1	1	1	1	1	3	1	3	3	1	1
ELECTRICAL	Load KVA		0.8	0.8	0.8	0.15	1.9	3.0	0.7	3.0		2.0	0.9	2.0	0.9	2.5	1.4
NOTES																	

PRICE DATA

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
Central Processor	160-A	Computer, including 8,192 words of core storage Buffer channel Paper tape reader and punch	2,250	225	90,000
	168-1	Auxiliary Arithmetic Unit (fixed point)	390	125	15,500
	168-2	Auxiliary Arithmetic Unit	450	130	18,750
Storage		Auxiliary Core Storage			
	169-1	1 module of 8,192 words	1,250	100	50,000
	169-2	1 module of 16,384 words	2,000	150	80,000
	169-3	1 module of 24,576 words	2,750	200	110,000
Input-Output	161	On-Line Input-Output Typewriter	262	140	10,500
	167-1	Card Reader	400	140	15,700
	167-2	Card Reader (Hollerith-to-BCD conversion)	460	150	18,100
	170	Card Punch Controller	335	90	13,700
	166-2	Buffered Line Printer	690	325	30,000
	1612	Line Printer	1,840	400	73,500
	1610-A	Card Reader, Punch, Printer Control	1,500	190	57,000
	603	Magnetic Tape Unit	550	120	24,000
	162-1	Tape Synchronizer for 603 M.T.U.	500	105	20,000
	606	Magnetic Tape Unit	825	140	36,000
	162-2	Tape Synchronizer for 606 M.T.U.	700	115	28,000
	163	Magnetic Tape System, including Control Unit and			
		1 Tape Unit (163-1)	970	235	38,800
		2 Tape Units (163-2)	1,482	400	59,300
		3 Tape Units (163-3)	1,994	565	79,800
		4 Tape Units (163-4)	2,506	730	100,300
	165-2	Incremental Plotter	285	130	9,000

CDC 3200

Control Data Corporation

AUERBACH

STANDARD EDP REPORTS

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CDC 3200

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CONTENTS

INTRODUCTION

§ 011.

The Control Data 3200 is a scientific computer system with large-scale performance capability and a medium-scale price tag. Its large-scale processing ability is derived from up to 32,768 24-bit words of core storage with a cycle time of only 1.25 microseconds, a 0.5-microsecond control register file, an interrupt system, and up to eight input-output data channels. (For comparative purposes, the processing capacity of the 3200 is somewhere between that of the older IBM 7044 and 7094, but with a monthly rental of about $18,000 as compared to $37,000 for the 7044 and $66,000 for the 7094.*)

First delivered in May 1964 (just after the announcement of the IBM System/360 computer systems), the Control Data 3200 has since had its competitive position improved by recent price reductions, by a considerable improvement in the speeds of its decimal arithmetic operations, by the announcement of the program-compatible CDC 3100 and 3300 systems, and by the provision of IBM System/360-compatible magnetic tape units.

For scientific processing, the performance of the CDC 3215 General Processor approximately equals the performance of the Model 60 processor of the IBM System/360. The comparative shortcomings of the Control Data system (no radix conversions, only three index registers, and a short word length) are roughly balanced by its comparative assets (eight available data channels, fast memory search operations, block operations** in parallel with both computation and I/O, and no restrictions on the type of peripherals which can be connected). Financially, the performance comparison between the two systems seems to favor Control Data, with a 10-tape 3200 system renting for $18,010 per month versus the $36,395 needed to obtain a comparable System/360.

The lower cost of the Control Data 3200 system is due mainly to reductions in the cost of the central processor and associated control equipment. Central processor cost is less than 20% of the total cost of a typical 3200 installation, as opposed to more than 40% of the total for a typical IBM 7044 or 7094 installation. This points up rather vividly the present trend toward reduced internal processing costs, while the input-output equipment remains relatively expensive. From an economic viewpoint, the 3200 processor is especially attractive for use in multi-computer applications. A Control Data 3200 system using two processors can, for example, provide the processing capability of an IBM 7094 installation at about half the cost.

The Control Data 3200 system is machine-code compatible only with the CDC 3100 and 3300 systems. It has, in addition, some compatibility through common programming languages with the Control Data 3400, 3600, and 3800 computer systems.

Hardware

The 3200 system offers a choice of four different processors which differ primarily in the volume and type of data they can handle most efficiently. The comparative features of the available processors are as follows:

- 3204 Basic Processor — contains arithmetic and control logic to perform 24-bit fixed-point arithmetic, 48-bit fixed-point addition and subtraction, Boolean, word-handling, and decision-making operations. An equivalent processor, with slower core storage modules and reduced I/O throughput capabilities, is available in the Control Data 3100 computer system (Computer System Report No. 254).

- 3205 Scientific Processor — has the capabilities of the Basic Processor, but can also handle 48-bit floating-point arithmetic, as well as 48-bit fixed-point multiplication and division.

- 3210 Data Processor — has the capabilities of the Basic Processor, plus the ability to handle 6-bit binary-coded decimal characters. This includes add and subtract (but not multiply and divide) operations on decimal fields up to 12 characters in length.

---

* Rates based on comparable 10-tape configurations.
** Block operations include memory searches and mass transfer operations.

§ 011.

- 3215 General Processor — an expanded unit that includes all the facilities of the 3204, 3205, and 3210. An equivalent processor, with faster core storage units and a few additional instructions to assist in multiprogramming, is available in the Control Data 3300 computer system (Computer System Report No. 255).

Each of the four models is essentially a single-address, fixed word-length, binary processor. The additional capabilities of the 3205, 3210, and 3215 are implemented by extra hardware packages which enable "scientific" and "BCD" type operations to be performed automatically. However, all commands in the 3200 instruction repertoire can be executed (either by hardware or software) on any processor model. The Basic Processor, for example, is not capable of directly processing instructions that require the floating-point or BCD packages. Instead, these instructions (called "trapped" instructions) are automatically detected and their functions are simulated by subroutines. To the user then, every 3200 can appear as a system with all of the facilities of a binary machine plus some of those of a decimal character-oriented one. This capability is certainly an advantage, but it may also be a disadvantage if improperly utilized. The ability to use programs from other installations without regard to the processor model for which the program was written is certainly desirable. On the other hand, a practice of running programs which were not designed for the actual processor may result in unnecessarily long execution times, due to inadvertent overuse of the subroutines that simulate the instructions which cannot be directly processed.

Instruction execution times are fast: fixed-point 24-bit addition requires only 2.5 microseconds, while a floating-point multiplication with two storage references takes 19 microseconds. In the optional BCD mode, two 12-character operands can be added in 12 microseconds. No facilities for direct multiplication or division of BCD fields are available. It appears that the BCD operations will be useful for auxiliary processing of alphabetic and decimal data, but not particularly suitable for major commercial applications.

An "off-line" search facility allows consecutive locations in core storage to be searched while the main program continues unhindered. The usefulness of this facility is limited by the fact that, unless the program has been carefully designed, core storage may already be "saturated" by the other demands of the processor and peripheral devices. Future developments in this area could, however, be of great value in information storage and retrieval applications.

An unusual "power-off" interrupt feature automatically transfers control to a fixed location in the event of power failure within the 3200 system. A special routine then prepares the system for an orderly shutdown so that no data will be lost. The whole operation takes 30 milliseconds; 16 milliseconds to detect the power failure and 14 milliseconds to process the interrupt.

The Control Data 3200 system can be equipped with up to eight input-output data channels, enabling the system to compute while simultaneously performing up to eight read-write operations which use any eight peripheral devices in the system. Use of the available buffered peripheral units, which require little data channel time, can allow the number of concurrently operating peripherals to increase to well beyond the number of data channels in a system.

Computation is normally delayed by input-output operations while the data being transferred is accessed or stored away in core storage. This delay, which amounts to one core storage cycle per word transferred, can sometimes be avoided by using different core storage modules for computational and input-output purposes. However, while it is possible to avoid delaying computation, it is not possible to increase the total system throughput above 666,667 words (2,666,667 characters) per second.

Many of the input-output controllers supplied with Control Data 3200 computer systems have two or more data channel connections. Such controllers can be used to switch peripheral units between two computer systems. The use of more than one central processor in an installation is comparatively frequent in Control Data 3000 Series installations, as both peripheral units and storage modules can easily be switched under program control.

Significant recent announcements by Control Data have included the IBM System/360-compatible magnetic tape units mentioned above, the 2,000,000-character-per-second transfer rate of the Model 861 and 862 Drum Storage Units, and the provision of controllers for IBM 1311 and 2311 Disk Storage Drives. The present peripheral units available with the 3200 computer system (and with all Control Data 3000 Series computer systems) include:

- Model 828 and 838 Disk Files —
  Capacity: 33 or 66 million characters
  Access time: 187 milliseconds average

§ 011.

- IBM 1311 and 2311 Disk Storage Drives —
  Capacity: 3 or 9.7 million characters
  Access time: 170 milliseconds average
- Model 3235 Drum Storage —
  Capacity: 0.5 million characters
  Access time: 17 milliseconds average
  Data transfer rate: 167,000 characters per second
- Model 861 and 862 Drum Storage —
  Capacity: 4.2 or 2.1 million characters
  Access time: 17 or 8.6 milliseconds average
  Data transfer rate: up to 2,000,000 characters per second
- Punched card equipment —
  Maximum reader speed: 1,200 cards per minute
  Maximum punch speed: 250 cards per minute
- Paper tape equipment —
  Maximum reader speed: 1,000 frames per second
  Maximum punch speed: 110 frames per second
- Line printing equipment —
  CDC 501: 1,000 lines per minute
  CDC 505: 500 lines per minute
  CDC 3152: 150 lines per minute
  IBM 1403 Model 2: 600 lines per minute
  IBM 1403 Model 3: 1,100 lines per minute
- 7-track and 9-track magnetic tape units —
  Maximum 7-track speed: 120,000 six-bit characters per second
  Maximum 9-track speed: 90,000 eight-bit characters per second

Software

The major assembly language for the Control Data 3100, 3200, and 3300 computer systems is called 3200 COMPASS. It bears only a general resemblance to the COMPASS language used for the Control Data 3600, and programs written in the two assembly languages are not interchangeable. The 3200 COMPASS assembler requires 8,192 words of core storage and 5 input-output devices, including at least 2 magnetic tape units during the assembly process. The output of the assembler is machine-language coding suitable for use with the SCOPE Operating System. (A reduced form of the 3200 COMPASS assembler, with no macro facilities, is available for Control Data 3100 computer systems which have only 4,096 words of core storage.)

The standard mathematical compiler is 3200 FORTRAN. This compiler uses a FORTRAN IV style language which is not simply an exact copy of some other language, but rather an independently-designed scientific programming language that offers a number of performance-improving features. In this respect it appears that Control Data is continuing a policy established in its FORTRAN-63 compiler for the CDC 1604: that of constructively re-evaluating the "standard" language before implementation. This policy gives promise of continued improvements in FORTRAN.

Programs written in FORTRAN can be compiled on any Control Data 3100, 3200, or 3300 computer system that has at least 8,192 words of core storage, 3 magnetic tape units, and 2 other input-output devices. The 3200 FORTRAN compiler was released to customers in November 1964. A Basic FORTRAN II system is available for smaller configurations.

COBOL language processing is provided for the Control Data 3100, 3200, and 3300 computer systems by the 3200 COBOL compiler. The language includes almost all of Required COBOL-61, and the compiler requires a 4,096-word system with 3 tape units and 2 other input-output devices for compilation. Release of 3200 COBOL to customer is scheduled for March 1965.

The SCOPE Operating System helps to assemble programs and to provide input-output services as required. It uses between 700 and 1,500 core storage locations to hold the resident program during operation; the exact amount depends upon the number and type of input-output routines required by a particular program. At present 3200 SCOPE is oriented toward magnetic tape processing, but a random access enhancement, specifically designed to service the IBM 1311 and 2311 Disk Storage Drives, is expected to be released in Spring 1965.

Other program packages under development include a Report Generator (scheduled for June 1965), a Linear Programming Package (June 1965), and a PERT Package (March 1965).

In summary, the Control Data 3200 is a fast, modestly-priced system that fully upholds Control Data's position in the market as a producer of powerful scientific computers at attractive prices. The 3200 is also significant in pointing up the growing financial imbalanc between the cost of internal processing and that of peripheral equipment.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	24 bits	basic addressable unit (data or instruction).
Character:	6 bits	addressable data unit.
Block:	1 to N characters or 1 to N words	Search, Move, and Input-output instructions.

.2 INFORMATION FORMAT

Type of Information	Representation
Operand:	24- or 48-bit fixed point word. 48-bit floating point word (optional). 6-bit character. 4-bit BCD character (optional).
Instruction:	1 or 2 words.
Field:	1 to 13 BCD characters.

SYSTEM CONFIGURATION

§ 031.

GENERAL

Every Control Data 3200 computer system includes the following units:

- A 3204, 3205, 3210, or 3215 Central Processor.
- A 1.25-microsecond Core Storage Unit ranging from 8,192 to 32,768 words (32,768 to 131,072 characters) in capacity.
- A desk console with detachable keyboard and adjacent I/O typewriter console.
- A Power Converter and Control Unit.

Two 3206 Data Channels are included in the basic system. Up to six more can be added, so that a fully-extended Control Data 3200 computer system will have eight data channels. Eight peripheral units or controllers can be connected to each data channel.

The data channels used in all of the Control Data 3000 Series computers present a common interface with peripheral units. As a result of this, any of the 3000 Series peripheral units described in this report can be connected through a 3206 Data Channel to a Control Data 3200 computer. Details of the loadings these units place on a Control Data 3200 computer system are described in the Simultaneous Operations section of this report, starting on page 245:111.100.

Some peripheral units or controllers can be connected to more than one data channel. This facility may be used either to allow two concurrent data transmissions to take place, or to allow the peripheral unit to be switched between two computer systems. A bank of magnetic tape units connected to a dual-channel controller is a case where multiple data transmissions would be the normal reason for having the two data channels; while a printer connected to two different computer systems by way of a dual-channel controller could be used by either system, as the situation in the computer room demands.

The core storage modules can similarly be connected to, and accessed by, two computers. Each 8,192-word module is independent and permits dual access by a second processor or special device.

SELECTION OF REPRESENTATIVE CONFIGURATIONS

The Control Data 3200 computer system is shown in the following Standard System Configurations, as defined in the Users' Guide, page 4:030.100:

- Configuration V; 6-Tape Auxiliary Storage Configuration.
- Configuration VI; 6-Tape Business/Scientific Configuration.
- Configuration VIIA; 10-Tape General Integrated Configuration.
- Configuration VIIB; 10-Tape General Paired Configuration, using a Control Data 160 Computer System as the satellite system.

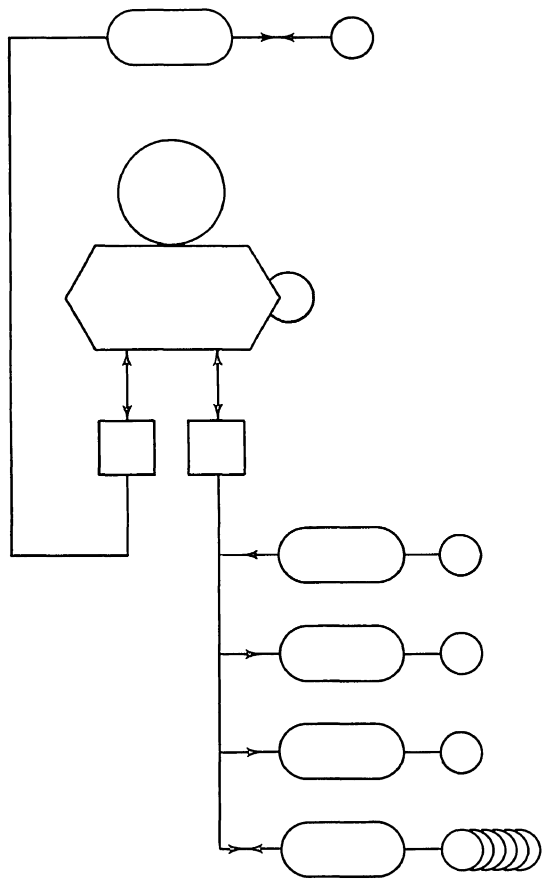
AN ADDITIONAL ILLUSTRATED CONFIGURATION

In addition to the Standard System Configurations illustrated in this section, an additional 8-tape configuration is shown (page 245:031.500), which allows for the switching of peripheral units and for the joint use of core storage by two independent computer systems.

§ 031.

.1 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V

Deviations from Standard Configuration: . . . . auxiliary storage capacity is 65% larger.
card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 40% faster.

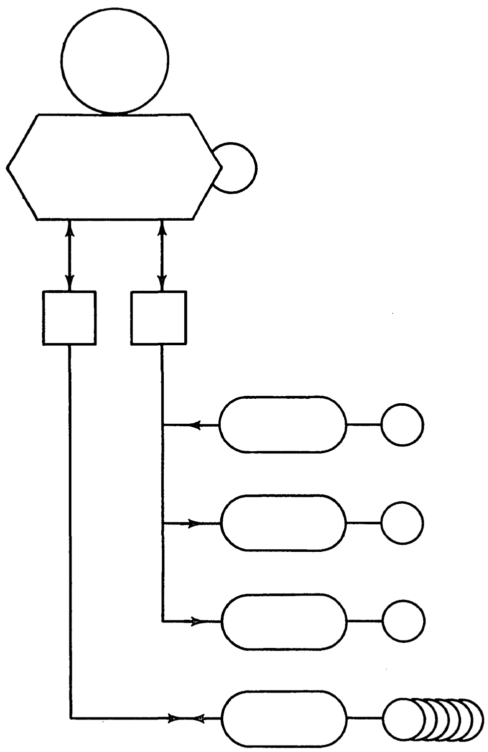


Equipment	Rental
828 Disk File (33 million char)	$ 2,400
3432 Controller	1,050
8,192 words of Core Storage	
3204 Basic Processor	
Console with Monitor Typewriter	4,300
3206 Data Channels (2)	
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3245 Controller	330
505 Line Printer (500 lpm)	635
3256 Line Printer Controller	515
603 41.7KC Magnetic Tape Units (6)	3,300
3229 Controller	600
TOTAL RENTAL:	$13,925

§ 031.

.2 6-TAPE BUSINESS/SCIENTIFIC SYSTEM; CONFIGURATION VI

Deviations from Standard Configuration: . . . . card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 40% faster.



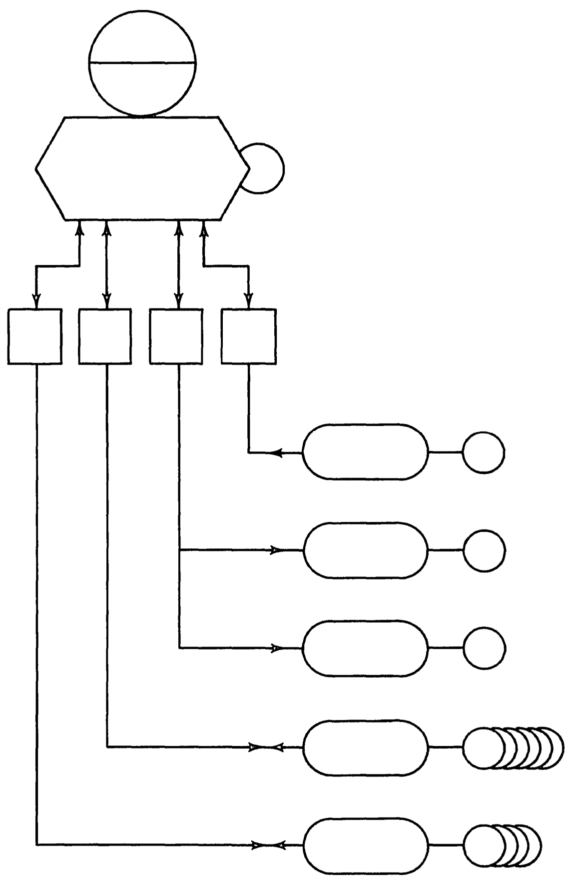
Equipment	Rental
16,384 words of Core Storage	$ 1,250*
3215 General Processor Console with Monitor Typewriter 3206 Data Channels (2)	5,150
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Line Printer	515
603 41.7KC Magnetic Tape Units (6)	3,300
3229 Controller	600
TOTAL RENTAL:	$12,695

* Price shown is for the additional 8,192 words over and above the basic core storage included in the General Processor rental.

§ 031.

.3 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . core storage is 33% larger.
3 less index registers are provided.
card reader is 140% faster.
card punch is 150% faster.



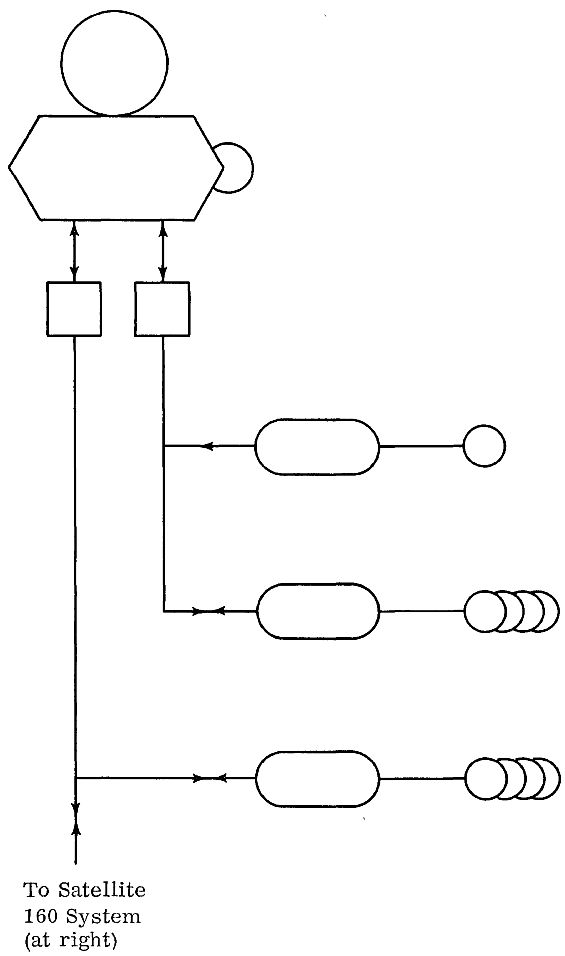
Equipment	Rental
32,768 words of Core Storage	$ 3,500*
3215 General Processor Console with Monitor Typewriter	5,150*
3206 Data Channels (4)	240*
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
604 60KC Magnetic Tape Units (6)	3,600
3229 Controller	600
604 60KC Magnetic Tape Units (4)	2,400
3228 Controller	425
TOTAL RENTAL:	$18,310

* The rental for the 3215 General Processor includes the charges for the first 8,192 words of core storage and for the first two 3206 Data Channels.

§ 031.

.4 10-TAPE GENERAL SYSTEM (PAIRED); CONFIGURATION VIIB*

Deviations from Standard Configuration: . . . . 3 less index registers.
direct connection to satellite system.
card reader is 1100% faster.



Equipment	Rental
16,384 words of Core Storage	$ 1,250**
3215 General Processor Console with Monitor Typewriter 3206 Data Channels (2)	5,150**
405 Card Reader (1,200 cpm) 3248 Controller	400 100
604 60KC Magnetic Tape Units (4) 3228 Controller	2,400 425
604 60KC Magnetic Tape Units (4) 3228 Controller	2,400 425
TOTAL ON-LINE EQUIPMENT:	$12,550
TOTAL SATELLITE EQUIPMENT:	$ 5,165
TOTAL RENTAL:	$17,715

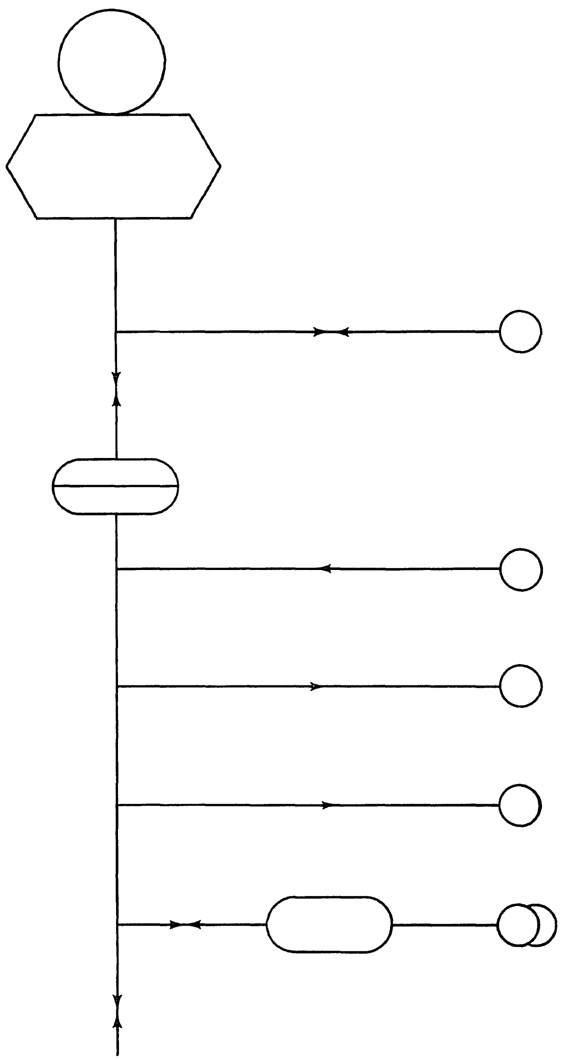
* This configuration can be rearranged in several ways: e.g., see "Typical 8-Tape System" on page 245:031.500.

* The rental for the 3215 General Processor includes the charges for the first 8,192 words of core storage and for the first two 3206 Data Channels.

§ 031.

SATELLITE EQUIPMENT (CDC 160)

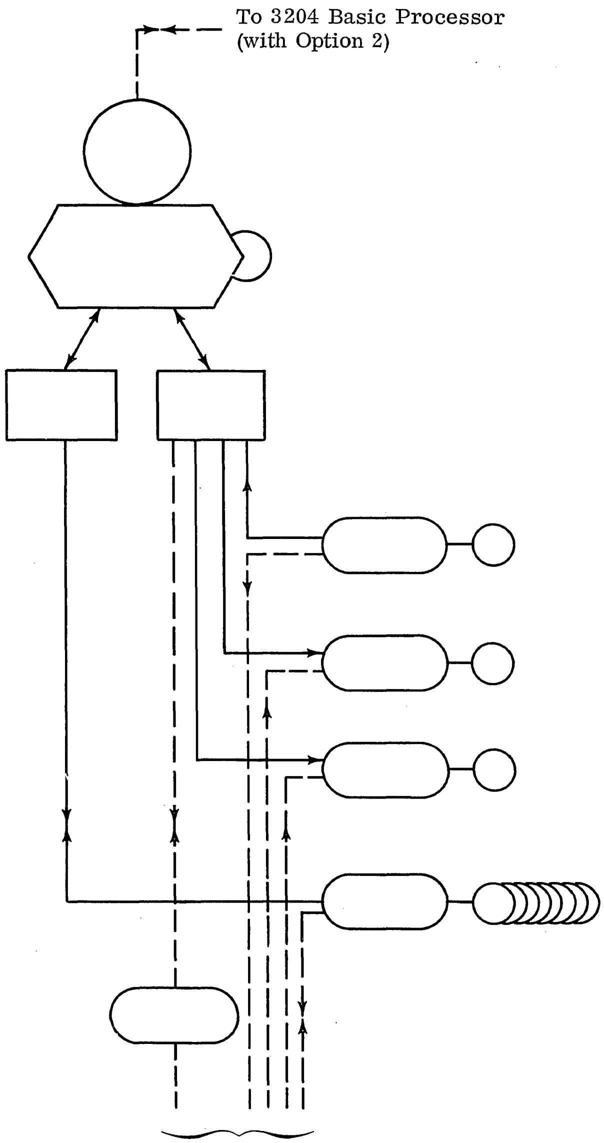
Deviations from Standard Configuration: . . . . direct connection to main system.
core storage is 100% larger.
multiply/divide is included.
paper tape equipment is included.
card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 30% slower.



Equipment	Rental
4,096 words of Core Storage 160 Processor Console with Monitor Typewriter Paper Tape Reader (350 cps) Paper Tape Punch (110 cps)	$ 1,500
3681 Data Channel Converter	275
3682 Satellite Coupler	175
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
601 21KC Magnetic Tape Units (2)	500
3127 Controller	320
TOTAL SATELLITE EQUIPMENT:	$ 5,165

§ 031.

.5 TYPICAL 8-TAPE SYSTEM



Equipment	Rental
16,384 words of Core Storage	$ 1,250*
3215 General Processor Console with Monitor Typewriter 3206 Data Channels (2)	5,150*
405 Card Reader (1,200 cpm) 3649 Controller	400
415 Card Punch (250 cpm)	295
3644 Controller	675
501 Line Printer (1,000 lpm)	865
3659 Controller	700
604 60KC Magnetic Tapes (8)	4,800
3423 Controller	1,600
3682 Satellite Coupler	175
TOTAL ON-LINE EQUIPMENT:	$16,235
SATELLITE EQUIPMENT - 160 SYSTEM:	1,775
TOTAL RENTAL:	$18,010
TOTAL ON-LINE EQUIPMENT:	$16,235
SATELLITE EQUIPMENT - 3200 SYSTEM:	3,050
TOTAL RENTAL:	$19,285

* The rental for the 3215 General Processor includes the charges for the first 8,192 words of core storage and for the first two 3206 Data Channels.

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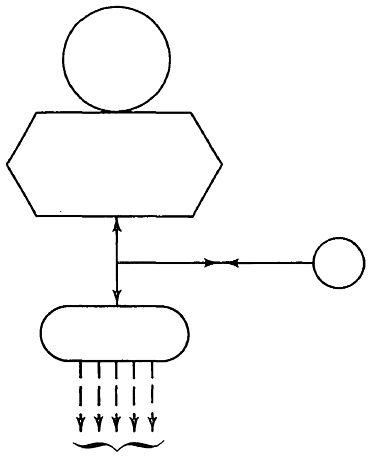
SATELLITE EQUIPMENT

OPTION 1 (CDC 160)

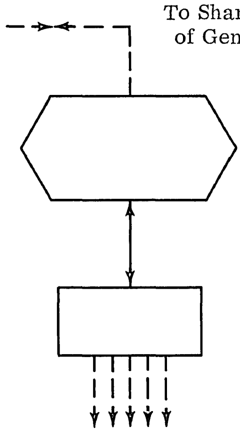


To Controllers
on facing page

Equipment	Rental
Core Storage: 4,096 words 160 Processor Console including Paper Tape Reader/Punch and Typewriter	$ 1,500
3681 Data Channel Converter	275
TOTAL SATELLITE EQUIPMENT:	$ 1,775

OPTION 2 (CDC 3200)

To Shared Core Storage
of General System



To Controllers
on facing page

Equipment	Rental
3204 Basic Processor Console with Monitor Typewriter 3206 Standard Data Channel	$ 4,300
TOTAL SATELLITE EQUIPMENT:	$ 4,300
Less allowance for 32,768 characters of core storage included in 3204 Basic Processor:	$ 1,250
EFFECTIVE TOTAL FOR SATELLITE EQUIPMENT:	$ 3,050

INTERNAL STORAGE: CORE STORAGE

§ 041.

.1 GENERAL

.11 Identity: . . . . 3203 Storage Module (16K).
3209 Storage Module (8K).

.12 Basic Use: . . . . working storage.

13 Description

A Control Data 3200 computer system can have 8,192, 16,384, or 32,768 24-bit word locations of core storage. The cycle time is 1.25 microseconds per word, and the access time is 0.75 microseconds. The core storage units use a basic 8,192-word module, and overlapped accesses are possible when more than one module is present. Overlapping is used principally to minimize the load placed on the central processor by input-output operations. Minimum loading occurs when the data used for computational purposes is contained in one module while the input-output areas are in a different module. As there is some common circuitry used both by the input-output transfers and by the central processor, it is not possible to eliminate completely the loading on the central processor, but even under worst-case conditions it can be reduced by over 75%.

All of core storage is available to the programmer, with no areas reserved for control functions, index registers, arithmetic operands, or other system requirements. By convention, however, the uppermost 32 words are reserved for the Autoload and Autodump routines, which can be initiated from the console.

Each physical storage word consists of 28 bits: 24 data bits plus 4 parity bits. The 24 data bits are functionally broken down into four 6-bit characters, and one of the parity bits is associated with each separate character. Addressing of core storage can be either by word or by character, using 15 bits or 17 bits per address, respectively.

The 3209 Storage Module contains 8,192 words of storage and is the basic module mentioned above. The 3203 Storage Module is functionally equivalent to two 3209 Storage Modules, having 16,384 words of storage arranged in two independent banks, each with its own read/write control.

A Control Data 3200 computer system can have one 3209 Storage Module, or either one or two

.13 Description (Contd.)

3203 Storage Modules. It is not possible to have one 3209 and one 3203 Module in a single computer system.

.14 Availability: . . . . 4 months.

.15 First Delivery: . . . . . May, 1964.

.16 Reserved Storage: . . . the uppermost 32 locations are, by convention, reserved for the Autoload and Autodump routines.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic cores.

.23 Storage Phenomenon: . . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no (safeguarded by power-off interrupt).
.244 Data permanent: . . . . . no.
.245 Storage changeable: . . no.

.27 Interleaving Levels: . . no interleaving as such; however, 3203 Storage Modules provide asynchronous operation with overlapped module access.

.28 Access Techniques: . . . coincident current.

.29 Potential Transfer Rates

.292 Peak data rates —
Cycling rates: . . . . . 800,000 cps.
Unit of data: . . . . . . word or character.
Gain factor: . . . . . two banks can be overlapped.
Loss factor: . . . . . both program and input-output have common use of some circuitry.
Data rate: . . . . 800,000 words (or characters)/sec/module.
Compound data rate: . 1,333,000 words (or characters)/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage		Maximum Storage
Identity:	3209 Storage Module	3203 Storage Module	2 3203 Storage Modules.
Modules:	1	1	2.
Words:	8,192	16,384	32,768.
Characters:	32,768	65,536	131,072.
Instructions:	8,192	16,384	32,768.

§ 041.

.32 Rules for Combining Modules: . . . . one 3209, or one or two 3203's (no combinations are allowed).

.4 CONTROLLER: . . . . . no separate controller required.

.5 ACCESS TIMING

.51 Arrangement of Heads: 1 read/write control for the 3209; 2 read/write controls for each 3203.

.52 Simultaneous Operations: . . . . accesses to each half (8,192 words or 32,768 characters) of the 3203, or to each one of 2 3203's, are asynchronous and independent of each other.

.53 Access Time Parameters

Access time: . . . . 0.75 μsec.
Cycle time: . . . . 1.25 μsec.
For data unit of: . . . . 1 word or 1 character.

.6 CHANGEABLE STORAGE: . . . . none.

.7 STORAGE PERFORMANCE

.72 Transfer Load Size

With self: . . . . 1 to 128 characters, one character at a time.
1 to 32 words, four characters (i.e., one word) at a time.

.73 Effective Transfer Rate

With self: . . . . 250,000 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	none	high-order bits are truncated.
Invalid code:	not possible.	
Receipt of data:	generate parity bit.	
Recording of data:	record parity pit.	
Recovery of data:	parity check	halt operation; console light.
Dispatch of data:	send parity bit.	
Timing conflicts:	interlock until cleared.	

INTERNAL STORAGE: 828 AND 838 DISK FILES

§ 042.

.1 GENERAL

.11 Identity: . . . . 828 Disk File.
838 Disk File.

.12 Basic Use: . . . . . . auxiliary storage.

.13 Description

The Model 828 and 838 Disk File Subsystems provide from 33 million to 264 million characters of random access storage, any part of which can be accessed within 365 milliseconds. The average access time is approximately 250 milliseconds and is made up of the positioning time, during which the access arms are positioned over the appropriate disc tracks, and a latency time while the discs revolve under the read/write heads and the required record comes into position.

An independently-positionable access arm serves each disc; this is the most significant difference between the Control Data Disk Files and most of the other currently-available disc storage units, which use a comb-like access mechanism in which all of the arms move in unison. The "cylinder" mode of disc file organization, which is currently being emphasized by IBM and other manufacturers, therefore does not apply to the Model 828 and 838 units.

From one to four Disk Files, each with a capacity of either 33 million (Model 828) or 66 million (Model 838) characters, can be included in a subsystem. Each Disk File unit can handle two concurrent operations - which may be reading, writing, searching, or positioning - but the whole subsystem is limited to one or two concurrent operations which involve data transmission. Whether the subsystem limit is one or two data transmission operations depends on whether a single-channel or a dual-channel controller is being used; both types are available.

Operations which require data transmissions are reading, writing, and searching for data. Searching for address positions and positioning of the access arms can proceed without supervision from the central computer once they have been initiated.

Reading and writing operations can handle records of any size, and data transmission takes place at either 68,000 or 110,000 characters per second, depending on whether the record is in the Inner Zone or the Outer Zone. Inner Zone records, which amount to one-third of the data capacity of the files, are transmitted at 68,000 characters per second and place a load on the computer system's core storage of 17,000 memory cycles per second - or 2.1% of a core storage module's maximum capacity in the case of the Control Data 3200 computer system. Outer Zone records, with their faster transmission rate, make a proportionately higher demand on the core

.13 Description (Contd.)

storage module; this amounts to 27,500 memory cycles per second, or 3.4% of a Control Data 3200 core storage module's maximum capacity.

Data searching operations make the same demands on the core storage as the reading or writing operations. In a Data Search operation, data in the files can be searched and tested for equal or greater-than conditions, using information supplied by the program for the necessary comparisons. Data searching continues until either the search is successful or the area specified as the search area has been exhausted. At the end of a search, either because the search has been successful or because no space remains to be searched, an interrupt request is sent by the Disk File to the central processor, and a flag is set showing the result of the operation.

Address searching, in contrast to data searching, makes no demands on the core storage modules during its operation, nor does it require a data channel to be reserved for its use. After an address search has been initiated, it uses no processor facilities until the address position comes under the read/write heads. At this time an interrupt request is signalled, and the address search function is concluded. The address search facility minimizes the use of the data channels by making their use unnecessary when the desired record position on the discs is still some distance away from the read/write heads. A read or write instruction is preceded by an address search, calculated to initiate an interrupt in sufficient time to allow the original read or write instruction to be given just before the desired record itself comes under the read/write heads. The rotational delay on both the Model 828 and the Model 838 units ranges from zero to 52 milliseconds, so there is a considerable advantage to be gained by reducing the time a data channel is engaged but not operating from this average rotational delay of 26 milliseconds to the time taken to recognize and service the interrupt - about half a millisecond in most cases.

The data on the Disk Files can be safeguarded by means of manual Write-Lock controls which prevent portions of the files from being overwritten. Accuracy of recording and reading back is checked by recording and checking parity bits with each character, and, at the programmer's discretion, by using the Write Check instruction. This instruction reads the data back after it has been written and compares it with the contents of the core storage locations where it was supposed to have come from. In addition, a checkword is recorded with each 256-character segment. This checkword is recomputed from the bits actually in the segment whenever readout occurs and checked with the version that was recorded when the data was originally written onto the disc.

§ 042.

.13 Description (Contd.)

The Model 828 and 838 Disk Files themselves are manufactured by Data Products Corporation for Control Data Corporation. Model 828 uses 16 discs per unit and has a capacity of 33,000,000 characters, while Model 838 uses 32 discs per unit and has a capacity of 66,000,000 characters.

.14 Availability: . . . . 4 months.

.15 First Delivery: . . . Nov. 1964 (Model 828). Apr. 1965 (Model 838).

.16 Reserved Storage

Purpose	Number of Locations
Clocking:	4 tracks on top disc, with special fixed heads.
Spares:	3 tracks per disc surface.
Address:	19 bits at the start of each 256-char. block.

.2 PHYSICAL FORM

.21 Storage Medium: . . multiple magnetic discs.

.22 Physical Dimensions: 16 or 32 31-inch diameter discs per unit.

.23 Storage Phenomenon: magnetization.

.24 Recording Permanence: . . . data once recorded can be read back at any time until overwritten by program. Turning off the electrical power leaves the data intact. The discs cannot be removed from the units.

.25 Data Volume per Band of 1 Track

Each disc-face is divided into two zones, an outer zone and an inner zone. Two-thirds of the data is stored in the outer zones, which have a greater capacity per track. Details of track capacity in each zone are:

	Inner Zone	Outer Zone
Words:	768	1,280
Characters:	3,072	5,120
Digits:	3,072	5,120
Instructions:	768	1,280
256-char. blocks:	12	20

.26 Tracks per Disc-Face: . . . . 256.

.27 Interleaving Levels:. no interleaving is used.

.28 Access Techniques

An individual, multiple-head positioning arm is used for each disc. This arm must be repositioned whenever a new track is selected. After repositioning (where necessary) has been completed, a delay follows until the start of the selected block comes under

.28 Access Techniques (Contd.)

the read/write heads, at which stage data transfer begins.

.29 Potential Transfer Rates

.291 Peak bit rates -

Cycling rate . . . . . 1,200 rpm.
Bit rate per track:
Inner zone tracks . 350,000 bits/sec.
Outer zone tracks . 590,000 bits/sec.

.292 Peak data rates -

Unit of data: . . . . . 6-bit character.
Data rate:
Inner zone tracks . 68,000 char/sec.
Outer zone tracks . 110,000 char/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

There are two modules available: Model 828, which has the same data capacity as the minimum subsystem, shown below; and Model 838, which has exactly twice the data capacity of the Model 828.

	Minimum Subsystem	Maximum Subsystem
Number of units:	1 Model 828	4 Model 838's
Words:	8,500,000	68,000,000
Characters:	33,000,000	264,000,000
Instructions:	8,500,000	68,000,000
Blocks:	131,200	1,049,600

.4 CONTROLLER

.41 Identity

Single-channel controller: . . . . Model 3432 Disk File Controller.
Dual-channel controllers: . . . Models 3632 through 3635 Disk File Controllers.

.42 Connection to System: from 1 to 64 Disk File Subsystems can be connected to a single computer system, depending on the availability of data channels.
Any dual-channel subsystem can be connected to two different computer systems if required.
No off-line connections are used.

.43 Connection to Device: 1, 2, 3, or 4 Disk File units can be connected to a subsystem, depending on the controller model.

.44 Data Transfer Control

.441 Size of load: . . . . . 1 to N 256-character blocks, limited by computer system core storage size.
.442 Input-output area: . . core storage.
.443 Input-output area access: . . . . each word or character.

§ 042.

.444 Input-output area lockout: . . . . . . manual switches on the units prevent data from being overwritten.

.446 Synchronization: . . . automatic; however an interrupt upon a specific address position passing under the heads allows data channel usage to be optimized.

.448 Testable conditions: . Ready, Busy, Access Unavailable, On Track, Write Lockout, Lost Data, Search Satisfied, Ready and Not Busy Interrupt requested, End of Operation Interrupt requested, Abnormal End of Operation Interrupt requested, Checkword Error detected.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks -
- Stacks per file: . . 128.
- Stacks per yoke: . . 8.
- Yokes per file: . . . 16 (one for each disc).

.512 Stack movement: . . . horizontal only.

.513 Stacks that can access any particular location: . . . . 1.

.514 Accessible locations -
- By single stack:
  - With no movement: 12 or 20 blocks.
  - With all movement: 768 or 1,280 blocks.
- By all stacks:
  - With no movement: 1/64th of the unit's storage capacity.

.52 Simultaneous Operations: . . . . one or two reading, writing, or data search operations per subsystem, plus up to two positioning operations and one address search per file unit.

.53 Access Time Parameters and Variations

.523 Variation in access time -

Stage	Variation (msec)	Average (msec)
Turn on positioning arm motor:	0 or 11	10.
Move head to selected track:	0 to 250	145.
Confirm track address:	52	52.
Wait for selected block:	0 to 52	26.
Transfer 1 block: .	2.6 or 4.3	3.
Total:	54.6 to 369.3	236.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With core storage: . . 1 to N blocks.

.73 Effective Transfer Rate

Variable, depending on record size and positioning requirements.

Peak Transfer Rate for Inner Zone records is 68,000 characters per second, and for Outer Zone records is 110,000 characters per second.

For random accesses with various record sizes, see the graph on page 245:042.900.

.74 Demands on System

Component	Condition	msec per word	Percentage of data transfer time
3200 Core Storage Module:	Inner Zone record	0.00125	2.1%
3200 Core Storage Module:	Outer Zone record	0.00125	3.4%

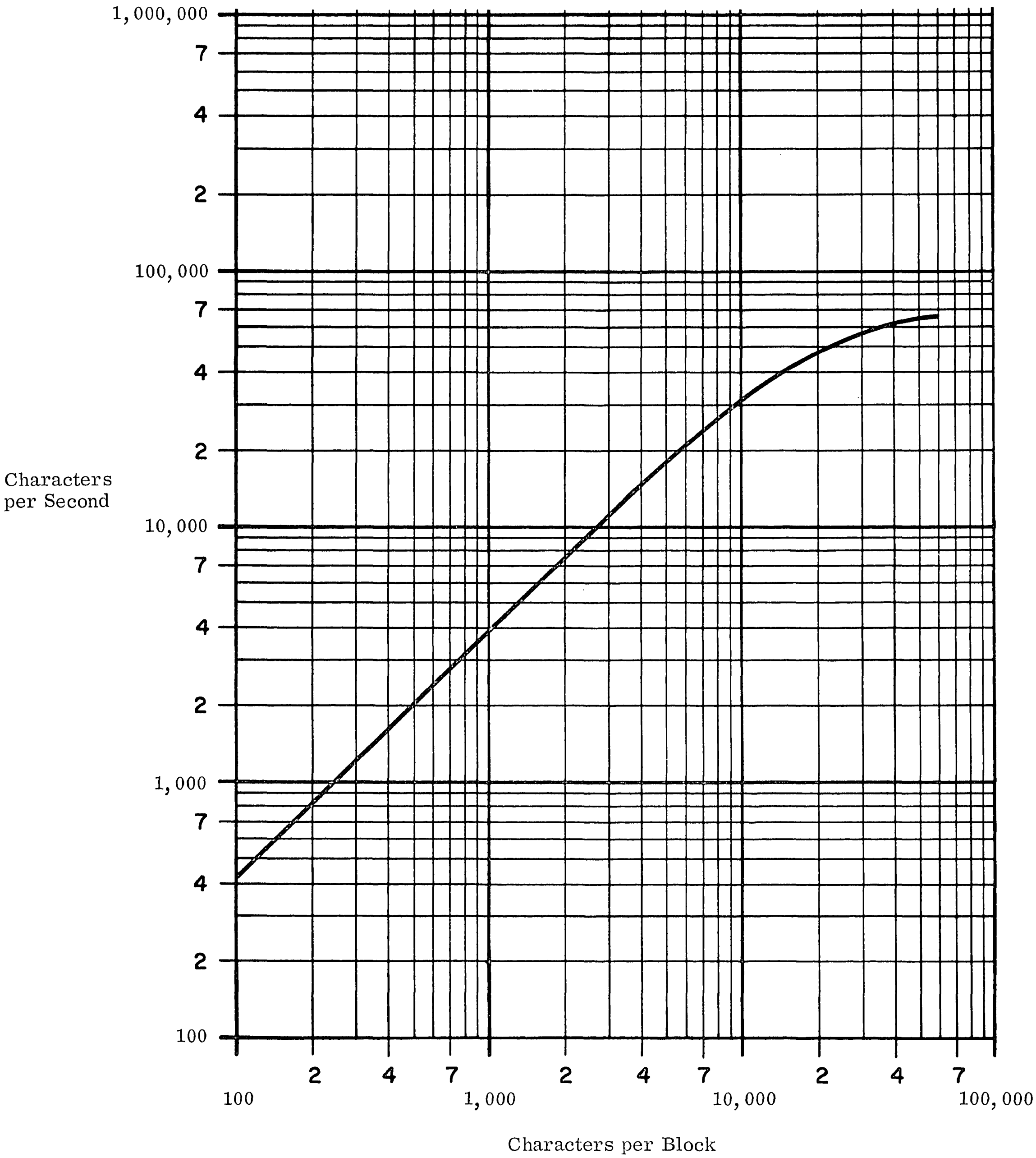
.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	not possible.	
Invalid code:	check	interrupt.
Receipt of data:	12-bit cyclic code check word per block	interrupt.
Recording of data:	generate 12-bit check word.	
Recovery of data:	none.	
Dispatch of data:	none.	
Timing conflicts:	none.	
Physical record missing:	check	interrupt.
Reference to locked area:	check	interrupt.
Wrong block selected:	address comparison	interrupt.

§ 042.

EFFECTIVE SPEED: 828 AND 838 DISK FILES

Based on random accessing and varying record sizes



INTERNAL STORAGE: IBM 1311 AND 2311 DISK STORAGE DRIVES

§ 043.

.1 GENERAL

.11 Identity: . . . . IBM 1311 Disk Storage Drive.
CDC 3231 Disk Pack Controller.

IBM 2311 Disk Storage Drive.
CDC 3233 Disk Pack Controller.

.12 Basic Use: . . . . . . auxiliary storage; for random or sequential access.

.13 Description

Control Data Corporation has two Disk Pack Controllers available which connect the IBM 1311 and 2311 Disk Storage Drives to the CDC 3200 computer system. Each controller can service up to eight Disk Drives, and the controller is in turn connected to one CDC data channel. No dual-channel controllers have been announced to date for these units.

The two IBM Disk Storage Drives are briefly described in Table I below; the 1311 and 2311 are more completely covered on page 414:042.100 of the IBM 1440 Computer System Report and page 420:044.100 of the IBM System/360 Computer System Report, respectively. The Track Record, Direct Seek, Scan Disk, and Seek Overlap optional features are expected to be normally used when the IBM equipment is connected to CDC computer systems.

Disk Packs written on IBM 1311 or 2311 Disk Storage Drives connected to a Control Data computer system can be read back only on an equivalent type of drive which is connected to the same or another Control Data computer. It is not possible, for

.13 Description (Contd.)

instance, to write a Disk Pack on an IBM computer system and then read it on a Control Data computer system; nor is it possible to write a Disk Pack on a 1311 Disk Storage Drive and read it on a 2311 Drive.

Data transfer operations include Read, Write, Write with Check Read, Masked Search, and Magnitude Search operations. The data records on the discs can be physically arranged either in sectors or in tracks; in either case the amount of data transferred or searched by a single instruction is limited only by the size of the computer system's core storage.

Interrupts can be set by the program to provide for separate interrupts when the Disk Drive becomes available, when an operation has been completed normally (e.g., when a search has been completed successfully or when a Write and Check operation has been completed without any recording error being discovered), or when for some reason the operation has been completed in an abnormal manner. The abnormal ending condition is signalled by means of indicator flags, which can be tested by the program. The four indicator flags associated with the Disk Storage Drives show the units' available or busy status, whether a search was successful, and whether Write Check or Address Error conditions have occurred.

The IBM 1311 Disk Storage Drive operates at a peak transmission rate of 77,000 characters per second, which places a loading on the Control Data 3200 core storage units of 2.4% of the total throughput capacity of a single module. The equivalent loading for an IBM 2311, which operates at 204,000 six-bit characters per second, is 6.4% of the capacity of a module.

TABLE I: COMPARISON OF IBM 1311 AND 2311 DISK STORAGE DRIVES AS USED IN THE CONTROL DATA 3200 COMPUTER SYSTEM

Model:	1311 Disk Storage Drive	2311 Disk Storage Drive
Storage capacity of 1 Disk Pack:	2.0 million characters (20 sectors per track) 2.98 million characters (1 record per track)	9.7 million characters (1 record per track)
Discs per pack:	6	6
Recording surfaces per pack:	10	10
Tracks per disc surface:	100	200
Data rate:	77,000 char/sec.	204,000 char/sec.
Rotation time:	40 msec	25 msec
Average positioning time:	150 or 250 msec	85 msec
Maximum storage capacity:	16 to 24 million characters per control unit	77.3 million characters per control unit

INTERNAL STORAGE: 3235 DRUM STORAGE UNIT

§ 044.

.1 GENERAL

.11 Identity: . . . . 3235 Drum Storage Unit.

.12 Basic Use: . . . . . . auxiliary storage.

.13 Description

Preliminary information indicates that the Control Data 3235 Drum Storage Unit provides for random access to 524,788 characters with a maximum access time of 34 milliseconds. The characters are recorded serially at a track density of 560 bits per inch, and data transmission takes place at 167,000 six-bit characters per second.

The record size used with the 3235 Drum Storage Unit can vary from one character up to the size of the core storage of the associated computer system. The effective transfer rate will depend upon the record size and the amount of rotational latency involved. Assuming an average latency of 17 milliseconds, the effective data transfer rate for a record of C characters will be:

$$\frac{167,000\ C}{C + 2840} \text{ characters per second.}$$

The load on the core storage modules during the data transfer operation will be, for CDC 3200 computer systems, 1.25 microseconds per 4-character word, which amounts to about 5% of the total data transmission time.

No separate controllers are used with the Model 3235 Drum Storage Unit; it is connected directly to a single data channel. A theoretical maximum of 64 Drum Storage Units can be connected to a Control Data 3200 computer system.

.14 Availability: . . . . . . 9 months.

.15 First Delivery: . . . October 1965.

INTERNAL STORAGE: 861 AND 862 DRUM STORAGE UNITS

§ 045.

.1 GENERAL

.11 Identity: . . . . 861 Drum Storage Unit.
862 Drum Storage Unit.
3416 Standard Input/Output Channel, Augmented.
3806 Standard Bi-directional Data Channel, Augmented.

.12 Basic Use: . . . . . auxiliary storage and inter-computer communication.

.13 Description

The Control Data 861 and 862 Drum Storage units provide very high data transmission rates - up to two million characters per second - and moderately fast access times. The choice between the two units will be based on whether doubled data capacity or halved access time is more valuable to a particular installation; the Model 861 Drum Storage Unit has a data capacity of 4, 186, 304 6-bit characters and a maximum access time of 34.4 milliseconds, while the Model 862 has half the data capacity - 2, 093, 152 6-bit characters - but can access them twice as fast - its maximum access time is only 17.2 milliseconds.

The physical characteristics of the Model 861 Drum are summarized, along with its performance characteristics, in Table I below. This table also shows the performance characteristics of the Model 862, but not its physical data, which have not yet been announced by Control Data Corporation.

The outstanding characteristic of both these units is the high data transfer rate which can be obtained. This has been achieved by recording and reading a data band of 13 tracks in parallel and using a track recording density of 560 bits per inch. The 13 physical bits consist of 12 data bits and an associated parity bit. Each data band contains approximately 64, 000 data characters in addition to system storage requirements.

The highest possible data transfer rate, 2, 000, 000 characters per second, is conditional upon every bit in the tracks being read sequentially. As an alternative, manual switches on each Drum Storage Unit can be set so that only every second, third, fourth, eighth, sixteenth or thirty-second bit is read. This technique is called "interlacing" and allows slower transfer rates to be used where advisable. As a result of the interlacing facility, these drum units can be connected to computer systems which would be unable to accept the highest available data transfer rates.

In selecting which of the interlace factors should be used, an installation must consider the slowest computer which will be connected to the Drum Storage Unit concerned, and also the peak loading which

.13 Description (Contd.)

will normally occur as a result of the simultaneous operation of other peripheral units connected to the system and the Drum Storage Unit(s). However, it is not always necessary to consider and allow for the absolute worst-case condition, provided that such a condition is not frequent, as the drum is simply allowed to revolve again if it is unable to store away a 12-bit image safely. Such an action, which reduces the transfer rate to two 6-bit characters per drum revolution, will seriously delay the data transmission which is then occurring, but this may well be more desirable than increasing the interlace factor and so permanently reducing the transmission rate from the Drum Storage Unit.

As the interlace factor is variable, the load placed on the core storage modules during data transmission also varies. With the Control Data 3200 core storage modules, where the loading is 1.25 microseconds per word transmitted, the total loading is 62.5/I percent of a core storage module's maximum capacity where I is the interlace factor in use. Under normal conditions, Control Data expects that an interlace factor of 2 will most commonly be used*, which gives a peak data transmission rate of 1, 000, 000 characters per second and uses 31% of the maximum throughput capacity of a 3200 core storage module.

Single- and dual-channel controllers are available for controlling up to eight 861 and 862 Drum Storage Units. The single-channel controllers can handle only a single data transmission at a time, while the dual-channel controllers allow two simultaneous data transmissions to take place, one on each data channel. It is not necessary that both the data channels of a dual-channel controller be connected to the same computer system; an interconnection between computers can be achieved by connecting them to different systems. Any Control Data 3000 series computer, or a Control Data 160-A computer, can be used in conjunction with either Model 861 or 862 Drum Storage Units.

In some cases, where the frequency of data arriving from the Drum Storage Units is greater than the frequency with which it can be stored in the core storage of the computer system concerned, special buffered data channels (called "Augmented" channels by Control Data) can be used. These channels have two words of storage which are used for temporary assembling and storage of data, instead of the single word which is held in the standard data channels. An Augmented channel would be needed, for example, if a Control Data 3200 Computer system, with its 1.25 microsecond memory, were attempting to use a Drum Storage Unit with an interlace factor of 1. Here, while only 62% of the core storage cycles

* An interlace factor of 2 is assumed in the associated software systems.

§ 045.

.13 Description (Contd.)

would suffice to store the output of a Drum Storage Unit, it would be necessary to clear the storage buffer of a standard channel within 1.00 microsecond in order to maintain the maximum data transmission rate. This would not be possible because the cycle time is greater than 1.00 microsecond. In an Augmented (buffered) channel it is only necessary to empty a specific buffer within three microseconds after receipt of the final characters, and this could easily be accomplished with the CDC 3200's 1.25-microsecond core storage cycle time.

.13 Description (Contd.)

The Control Data 861 and 862 Drum Storage Units are manufactured by Control Data Corporation.

.14 Availability: . . . . . 9 months.

.15 First Delivery:

861 Drum Storage Unit . . . . April 1965.
862 Drum Storage Unit . . . . August 1965.

TABLE I: FEATURES OF THE MODEL 861 AND 862 DRUM STORAGE UNITS

Model:	861	862
Capacity:		
6-bit characters	4,186,304	2,093,152
24-bit words	1,046,561	523,288
Access Time:		
Minimum (msec)	0.0	0.0
Maximum (msec)	34.4	17.2
Transfer Rate (Peak)	2,000,000 char/sec	2,000,000 char/sec
Transfer Load Size:		
Minimum (char)	1	1
Maximum (char)	full core store	full core store
Number of Tracks	832	832
Track Capacity (bits)	32,000 approx.	16,000 approx.
Track Density (bits/inch)	560	560
Error Checks:		
Recording	Parity bits recorded	Parity bits recorded
Reading	Parity checked	Parity checked
Drum Diameter	18 inches	?

CENTRAL PROCESSORS

§ 051.

.1 GENERAL

.11 Identity: . . . . 3204 Basic Processor.
3205 Scientific Processor.
3210 Data Processor.
3215 General Processor.

.12 Description

The CDC 3200 System offers a choice of four different processors which differ primarily in the volume and type of data they can handle most efficiently. The comparative features of each of the available processors are as follows:

- 3204 Basic Processor — contains arithmetic and control logic to perform 24-bit fixed-point arithmetic, 48-bit fixed-point addition and subtraction, Boolean, word handling, and decision-making operations.
- 3205 Scientific Processor — has the capability of the Basic Processor, but can also handle 48-bit floating-point arithmetic, as well as 48-bit fixed-point multiplication and division.
- 3210 Data Processor — has the capability of the Basic Processor, plus the ability to handle 6-bit decimal characters. This ability includes add and subtract (but not multiply and divide) operations on decimal fields up to 12 characters in length.
- 3215 General Processor — an expanded unit that includes all the facilities of the 3204, 3205, and 3210.

Each of the four models is essentially a single-address, fixed word-length, binary processor. The additional capabilities of the 3205, 3210, and 3215 are implemented by extra hardware packages which enable "scientific" and "BCD" type operations to be performed automatically. However, all commands in the 3200 instruction repertoire can be executed (either by hardware or software) on any processor model. The Basic Processor, for example, is not capable of directly processing instructions that require the floating-point or BCD packages. Instead, these instructions (called "trapped" instructions) are automatically detected and their functions are simulated by subroutines. To the user, then, every 3200 can appear as a system with all of the facilities of a binary machine plus some of those of a decimal character-oriented one. This capability is certainly an advantage, but may also be a disadvantage if improperly utilized. The ability to use programs from other installations, regardless of which processor model the programs were written for, is highly desirable. On the other hand, a practice of running programs which are not designed for the actual processor may result in unnecessarily long execution times, due to inadvertent overuse of the subroutines that simulate the instructions which cannot be directly processed.

.12 Description (Contd.)

Word length of core storage locations is 28 bits (24 data bits plus 4 parity bits). One location can contain an instruction, a 24-bit fixed-point binary data word, one half of a 48-bit fixed- or floating-point data word, or an alphanumeric word consisting of four 6-bit BCD characters. An instruction word normally consists of a 6-bit operation (or function) code, an addressing mode bit (indirect or direct), a 2-bit index register designator, and a 15-bit core storage address field. In some cases the indirect addressing flag, index register designation, and address bits are used for other purposes such as operand values, shift counts, and extensions of the function code or address field. Only three index registers are provided, and their use is pre-empted by various instructions. To some extent this limits the programmer in his use of automatic address modification techniques.

Instruction execution times are fast: fixed-point 24-bit addition requires only 2.5 microseconds, while a floating-point multiplication with two storage references takes from 14 to 18 microseconds. In the BCD mode, two 12-character operands can be added in 11.5 microseconds. These times, which are a great improvement over the initial specifications, are still slower than the equivalent binary operations, but they are certainly fast enough for normal editing operations.

A fast-access 64-word Register File, incorporated as part of each of the processors, has a cycle time of 0.5 microsecond. Although the programmer has access to all registers in the file, certain registers are reserved for specific purposes such as address storage during "block" operations. Other portions of the file can be used freely as temporary storage.

The "block" operations use special processor controls and are of three types: Search, Move, and Input-Output. After one of these operations has been activated, the processor can return to its main program and continue until an interrupt is generated or the program senses completion of the block operation. Each of these operations requires three instruction words, which contain the starting and ending addresses (or source and destination addresses for a Move command) for the operation and a "reject" instruction. The reject instruction is used if the block controls or the addressed input-output data channel happens to be busy. All three types of block operations are carried out on a character-by-character basis. The input-output instructions, which can also specify a word-by-word transfer, are described in more detail under Simultaneous Operations (Section 245:111).

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.12 Description (Contd.)

The 3200 has a program interrupt system which permits interruption when any of the following conditions occur: arithmetic faults (overflow, divisor too small, exponent too large), completion of a block operation (search, move, or input-output), manual switch operation (console key), an interrupt request from any of the eight peripheral positions on each data channel, or a real-time interrupt controlled by the Real-Time Clock. When an interrupt condition is recognized, the current instruction address is stored along with a number that indicates the specific interrupt condition, and program control is transferred to a fixed location. The programmer, however, can choose to honor or ignore any particular interrupt condition by setting appropriate bits in an Interrupt Mask register. In addition, several instructions are available for sensing and clearing interrupts independently, and for either enabling or disabling the entire interrupt system.

A special power failure interrupt automatically (and unequivocally) transfers control to a fixed location (location 00010) in the event power fails within the 3200 system. A special routine then prepares the system for an orderly shutdown so that no data will be lost. The whole operation takes a maximum of 30 milliseconds; 16 milliseconds for detection, and 14 milliseconds for processing the interrupt.

.13 First Delivery: . . . . . May, 1964.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add-subtract:	automatic	binary	24 bits.
		automatic	binary	48 bits.
		automatic (2)	decimal	1 through 12 BCD chars.
	Multiply —			
	Short:	none.		
	Long:	automatic	binary	24 bits.
		automatic (1)	binary	48 bits.
		subroutine	decimal	variable.
	Divide —			
	No remainder:	none.		
	Remainder:	automatic	binary	24 bits.
		automatic (1)	binary	48 bits.
		subroutine	decimal	variable.
.212	Floating point —			
	Add-subtract:	automatic (1)	binary	36 & 11 bits.
	Multiply:	automatic (1)	binary	36 & 11 bits.
	Divide:	automatic (1)	binary	36 & 11 bits.
.213	Boolean —			
	AND:	automatic	binary	24 bits.
	Inclusive OR:	none.		
	Exclusive OR:	automatic	binary	24 bits.
.214	Comparison —			
	Numbers:	automatic.		
	Absolute:	none.		
	Letters:	automatic.		
	Mixed:	6-bit characters.		
	Collating sequence:	0-9, A-Z, with special characters and unassigned symbols in various places; see Page 245:141.100.		

(1) These operations are possible only with 3205 Scientific and 3215 General Processors.

(2) This operation is possible only with 3210 Data and 3215 General Processors.

§ 051.

.215 Code translation:

Code translation from external BCD to internal BCD is automatic when magnetic tapes recorded in BCD format are being used.

Details of other code translations needed, and the timings of the subroutines used to accomplish the translations, are shown in Table I.

.216 Radix conversion:

Radix conversion between BCD and binary forms is performed by standard subroutines. The timings of these subroutines are listed in Table I.

.217 Edit format: . . . . own coding; the character-by-character search for equality or inequality appears to be the only instruction specifically oriented toward this task.

.218 Table look-up —

Operation	Provision	Size	Comment
Equality:	automatic	by word	entries may be spaced every 1, 2, 3, 4, 5, 6, 7, or 8 words. Masked operands are allowed.
Greater than:	automatic	by word	
Greatest:	none.		
Least:	none.		
.219 Others — Character Search:	automatic	character-by-character	the search is made off-line, using the block transfer facilities; single character equality or inequality can be searched for.

TABLE I: CONVERSION TIMES FOR STANDARD SUBROUTINES

Original Operand		Microseconds Required For Conversion To:				
Type	Magnitude	Internal BCD (1)	Fixed Point Binary (2)	Floating Point Binary (3)	Column BCD (4)	Row BCD (5)
Internal BCD	$< 10^7$	—	13/digit	13/digit + 18/operand	5,000/card	30,000/card
Internal BCD	$\geq 10^7$	—	23/digit	23/digit + 18/operand	5,000/card	30,000/card
Fixed Point Binary	$< 10^7$	22/digit	—	18/operand	22/digit + 5,000/card	22/digit + 30,000/card
Fixed Point Binary	$\geq 10^7$	44/digit	—	18/operand	22/digit + 5,000/card	44/digit + 30,000/card
Floating Point Binary	$<10^7$	22/digit + 28/operand	28/operand	—	22/digit + 28/operand + 5,000/card	22/digit + 28/operand + 30,000/card
Floating Point Binary	$\geq 10^7$	44/digit + 28/operand	28/operand	—	44/digit + 28/operand + 5,000/card	22/digit + 28/operand + 30,000/card

(1) Internal BCD is used in decimal arithmetic, for card reader input and for printer output.
(2) Fixed Point Binary is used for 24 or 48-bit binary arithmetic.
(3) Floating Point Binary is used for all floating point operations.
(4) Column BCD is used for output via buffered card punch equipment.
(5) Row BCD is used for output via unbuffered card punch equipment.

Note: "digit" refers to decimal digits in all of the above times.

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.22 Special Cases of Operands

.221 Negative numbers: . . . one's complement.
.222 Zero: . . . . positive zero and negative zero.
.223 Operand size determination: . . . . normally 24 bits; 48 bits available in double precision and floating point instructions, and variable length of 1-12 decimal digits in BCD operations.

.23 Instruction Formats

.231 Instruction structure: . basically 1-address.
.232 Instruction layout

Part:	f	a	b	m
Size (bits):	6	1	2	15

.233 Instruction parts

Name	Purpose
f:	function code.
a:	indirect addressing flag.
b:	index register designation.
m:	operand address.

Note: In many cases the indirect addressing flag and the index register designation are used for other purposes. These cases include:

- when literals are used instead of operand addresses;
- when Search or Move operations are involved;
- when the operand address is a register;
- when selective jumps based on console keys are involved.

In most BCD character operations, indirect addressing is not available, and only one specific index register can be used with a particular instruction.

Register file addresses cannot be indexed or indirectly addressed.

.234 Basic address structure: . . . . 1 + 0.
.235 Literals —
Arithmetic: . . . . . . no facility.
Comparisons and tests: . . . . literals can be compared with index register counts and accumulator contents only; maximum size is 262, 145.
Incrementing modifiers: . . . . . . only in the Block Search operation.

.236 Directly addressed operands — Internal storage
type: . . . . core storage.
Minimum size: . . . . 1 character.
Maximum size: . . . . 1 or 2 words.
Volume accessible: . all.
.237 Address indexing
.2371 Number of methods: . two.
.2372 Names: . . . . normal indexing. specific indexing.
.2373 Indexing rule (normal indexing): . . . . addition of contents of one of the 3 index registers to the address in one's complement mode.
.2373 Indexing rule (specific indexing): . . . . same as normal indexing except that a specified index register is always used with the particular instruction.
.2374 Index specification: . bits 15 and 16, or bit 17, of instruction word.
.2375 Number of potential indexers: . . . . 3.
.2376 Addresses which can be indexed: . . . . . . operand addresses in arithmetic, logical, load, and store instructions, and some jump instructions. BCD operations (which index by character, not by word) can only be modified within 8, 192 words.
.2377 Cumulative indexing: . no.
.2378 Combined index and step: . . . . no.
.238 Indirect addressing
.2381 Recursive: . . . . yes.
.2382 Designation: . . . . . . single bit in appropriate instructions and in each indirect operand address.
.2383 Control: . . . . the last address in the recursive sequence is the first address reached which has no indirect addressing flag.
.2384 Indexing with indirect addressing: . index modification always takes place first. All levels of a recursive indirect address sequence may be indexed.
.239 Stepping
.2391 Specification of increment: . . . . . . within instruction.
.2392 Increment sign: . . . . + or -.
.2394 End value: . . . . positive zero; tests are also available for comparison with literals.
.2395 Combined step and test: . . . . yes, for ± 1 increments only.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size in bits	Program usage
Registers:	3	24	arithmetic and instructions.
Registers:	4	15	address handling.
Registers:	57	24	I/O control, clock, temporary storage, etc.

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.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: sequential.

.32 Look-Ahead: none.

.33 Interruption

.331 Possible causes —

In-out units: the state of any specific device connected to one of the eight I/O controllers can initiate an interrupt. Conditions which can cause interrupts vary for different types of I/O devices, but usually include normal end of an operation, abnormal end, and inability to respond to an instruction.

In-out controllers: the failure of an I/O controller to accept or reject a Connect or Function instruction.

Processor errors: arithmetic overflow.
divide fault (division by too small a number; not simply by zero).
exponent overflow (> $2^{10}-1$).
BCD fault (irregular characters).

Other: power failure.
real-time clock.
search-move interrupt.

.332 Control by routine: interrupts may be masked by the program. In addition, they are automatically inhibited (except for the Power Failure Interrupt) by the entry into any interrupt routine, and a special instruction must be used to re-enable the preselected interrupts after each interrupt.

.333 Operator control: none, except that he always may originate a manual interrupt, or use the six Sense switches to set the mask.

.334 Interruption conditions:
(1) an interrupt condition must arise.
(2) it must not be inhibited either permanently or during the processing of an interrupt routine.
(3) the priority scanner must have reached the priority level of the interrupt condition.

.335 Interruption process —

Disabling interruption: operating instruction proceeds to an orderly halt.

Registers saved: program address register only.
A nine-bit interrupt identification code is placed in a fixed location.
fixed location.

Destination: 00003 or 00010.

.336 Control methods —

Determine cause: own coding.

Enable interruption: own coding.

.34 Multiprogramming: no special provisions.

.35 Multi-Sequencing: the block operations (search for character equality/inequality, move characters, input-output instructions) can proceed in parallel with and independently of the main program, once initiated.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

		Binary (24 bits)	BCD (12 char)
.411	Fixed point —		
	Add-subtract:	2.5	11.5
	Multiply:	7.8 to 11	not available.
	Divide:	11.25	not available.
.412	Floating point —		
	Add-subtract:	10 to 12.	
	Add-subtract (subroutine):	150.	
	Multiply:	14 to 18.	
	Multiply (subroutine):	240.	
	Divide:	20.	
	Divide (subroutine):	425.	
.413	Additional allowance for —		
	Indexing:	0.375	
	Indirect addressing:	1.25	
	Re-complementing:	0.0	
.414	Control —		
	Compare:	1.9	
	Branch:	1.25	
	Compare and branch:	1.9	
.415	Counter control —		
	Step:	1.25	
	Step and test:	1.9	
	Test:	1.9	
.416	Edit:	not available.	
.417	Convert:	see Table I.	
.418	Shift:	1.25 to 3.75	

.42 Processor Performance in Microseconds

.421 For random addresses —

	Fixed Point (24 bits)	BCD (12 char)	Floating Point (48 bits)
c = a + b:	7.5	27.5	18.5
b = a + b:	6.25	27.5	18.5
Sum N items:	2.5N	11.5N	11.0N
c = ab:	14.4	not available	23.5
c = a/b:	17.5	not available	27.5

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.422 For arrays of data —

	Fixed Point (24 bits)	BCD (12 char)	Floating Point (48 bits)
$c_i = a_i + b_j$:	11.79	35.16	22.79
$b_j = a_i + b_j$:	10.16	37.28	22.79
Sum N items:	4.78N	13.78N	13.28N
$c = c + a_i b_j$:	20.81	not available	38.41

.423 Branch based on comparison —
Numeric data: 15.46
Alphabetic data 15.46

.424 Switching —
Unchecked: 5.38
Checked: 9.18
List search: . . . . 14.58 + 4.2N

.425 Format control, per character —
Unpack: . . . . 120.
Compose: . . . . 120.

.426 Table look-up, per N comparisons —
For a match: . . . . 4.2 + 4.2N
For least or greatest: 4.2 + 4.2N
For interpolation point: . . . . 4.2 + 4.2N

.427 Bit indicators —
Set bit in pattern: . . . 7.5
Test bit in pattern: . . 5.65

.428 Moving, per N words: . 3.3 + 3.9N (250,000 24-bit words/sec).

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	check	specific bit is set; optionally, interrupt occurs (interrupt system is deactivated, instruction address is stored, and a forced jump is made to a specific location for each case).
Underflow:	check	(same as above)
Divisor too small:	check	(same as above)
Shift faults:	check	(same as above)
Invalid instructions:	check	(same as above)
Abnormal end of an I/O operation:	check	(same as above)
Storage reference:	parity check	optional halt; console light.
Receipt of data:	parity check	optional halt; console light.
Internal reject:	parity check	optional halt; console light.
Dispatch of data:	parity bits are included, but not checked	none.

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . 3201 Desk Console.

.12 Associated Unit: . . Input-Output Typewriter is included with the 3201.

.13 Description

The 3201 Desk Console is standard equipment in all Control Data 3200 computer systems. It includes a movable input keyboard, which can either be operated at the console or removed and carried to a suitable nearby location. An input-output typewriter is also incorporated in the console design. Both the keyboard and the typewriter have direct access to the computational module, and do not use the regular data channels.

Octal or decimal displays are used to display the contents of the seven operational registers. The operator sitting at the console has a good view of these displays, and of the equipment itself (see photograph).

The "external" status indicators display the existing condition of the input-output channels, while six columns of "internal" condition indicators provide the following information:

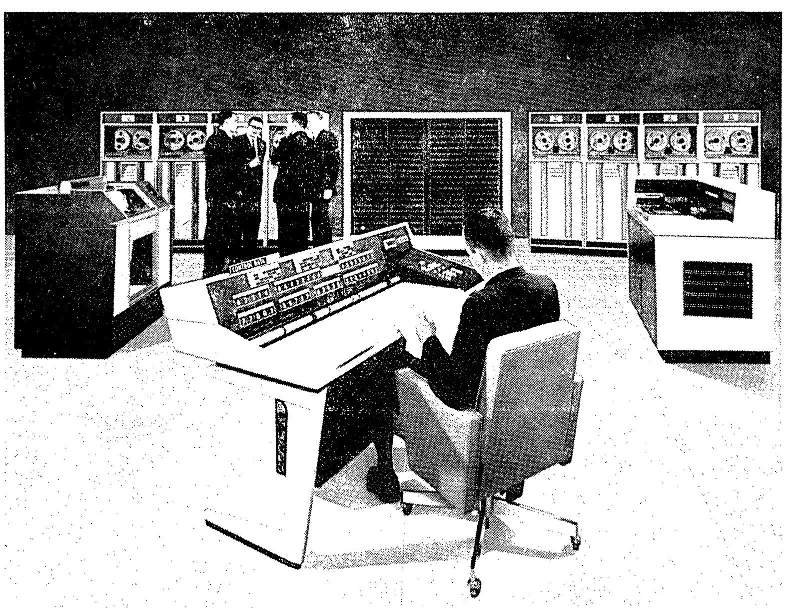
- Storage Active — for addressing purposes, the four possible 8,192-word sections of storage are designated by digits 0-3. Whenever one of these storage sections becomes active, the corresponding indicator light is lit.

.13 Description (Contd.)

- Conditions — a Standby light indicates that the main power switch is on, but that individual supplies are still off; an Interrupt Disabled light is on whenever the interrupt system is disabled by the program.
- Cycle — four cycles are represented: Read Next Instruction, Read Address, Read Operand, and Store Operand. These indicators are lit whenever the cycles are in progress.
- Faults — these lights represent four arithmetic faults: Arithmetic Overflow, Divide, Exponent Overflow, and Decimal (BCD).
- Temperature Warning and Temperature High — up to four cabinet sections are represented.

The console switches are divided into two groups — those used for normal operations of the system and those used primarily for maintenance purposes. Operational switches are included on the main console and on an entry keyboard. The keyboard replaces the Set and Clear pushbuttons that are found on most Control Data computers for the manual entry of information.

The main console switches provide for such operating controls as breakpoint/run mode selection, automatic load/dump initiation for a designated device, selective jump instruction keys, manual interrupt, and master clear buttons. The keyboard switches provide for start and stop controls, register display control, and the manual entry of information into core storage or a designated register.



INPUT–OUTPUT: 405 CARD READER

§ 071.

.1 GENERAL

.11 Identity: . . . . CDC 405 Card Reader.
CDC 3248 Card Reader Controller.
CDC 3447 Card Reader Controller.
CDC 3649 Card Reader Controller.

.12 Description

The Control Data 405 Card Reader is a fast, asynchronous photoelectric reader that operates at 1,200 cards per minute when reading full 80-column cards, and at up to 1,600 cards per minute with 51-column stub cards. The input hopper can hold 4,000 cards. Two output stackers are provided: one main stacker which can hold 4,000 cards, and a reject stacker which can hold 240 cards. The cards are turned individually as they are being read so that the card deck in the output stacker is in exactly the same order as it was before being read.

The card read operation proceeds serially, column-by-column. Two separate photoelectric read stations read each column, and the two readings are checked within the card reader before the column image is forwarded to the card reader controller. Conversion from Hollerith to BCD code is normally executed automatically on all cards which do not have positions 5 and 7 punched in column 1. The conversion can, however, be inhibited by program where desirable.

There are three different Card Reader Controllers. The controllers differ in their buffering provisions and in the number of data channels which can be connected to each controller. The available controller models and their characteristics are:

Model 3248: unbuffered, one data channel connection.
Model 3447: full-card buffer, one data channel connection.
Model 3649: full-card buffer, two data channel connections.

The Card Punch Controllers intervene between the computer system and the card reader itself. The program facilities available with the Control Data 405 Card Reader do not differ significantly when different controllers are used, except that where the controller can be physically connected to two data channels, it is possible to switch one card reader between two computer systems by connecting the two channels to different systems.

.12 Description (Contd.)

A single card read instruction defines an area in core storage which is to be filled with data read by the card reader. As many cards as are necessary to fill this area are read in under the supervision of a card reader controller, without further program intervention being necessary.

Interruptions can be set to occur when the card reader becomes available, when a card read operation is successfully completed, or when for some reason a card read operation ends without being successfully completed. The program can inhibit any or all of these three separate and distinct interrupt conditions.

In addition to the interrupt system, status indicators show: whether the unit is currently able to respond to an instruction; which interrupt conditions are presently activated; whether the card presently being read is a binary card; whether a card jam, empty input hopper, or full output hopper condition is present; whether a card read error has been noted; and whether the operator has set a switch on the reader indicating that the last card of the card file being read is physically in the card reader.

Each card reader must have its own individual card reader controller, so the number of card readers which can be connected to a computer system is related to the number of data channels and the number of selectable positions on each data channel. The theoretical maximum number of card readers that can be connected to a Control Data 3200 computer system is 64.

The load on the core storage, for the Control Data 3200 computer system operating in the word mode, is 25 microseconds per card for Hollerith coding and 50 microseconds per card for column binary cards. This loading amounts to 3% of the total throughput capacity of a single 3200 core storage module when Hollerith cards are being read at 1,200 cards per minute. Use of the column binary mode doubles the loading to 6% of a core storage unit's capacity, and use of character-mode reading (where each character read is placed into a separate word) quadruples the loading to a maximum value of 12%. Any code conversions subsequently required to convert BCD operands into binary operands for computational purposes impose an additional effective load on the central processor.

The 405 Card Reader is manufactured by Control Data Corportion.

.13 Availability: . . . . 4 months.

.14 First Delivery: . . . . . 1963.

INPUT–OUTPUT: CARD PUNCHES

§ 072.

.1 GENERAL

.11 Identity: . . . . CDC 415 Card Punch.
IBM 523 Card Punch.
IBM 544 Card Punch.
3245 Card Punch Controller.
3445 Card Punch Controller.
3644 Card Punch Controller.

.12 Description

A Control Data 415 Card Punch can be connected to any Control Data 3000 computer system through a Card Punch Controller. The punch operates at 250 cards per minute and uses a row-by-row punching technique. The punched data is then read at a post-punch read station, which counts the number of holes in the card. Subsequent to the post-punch read station, a card can be offset in the output stacker so that the operator can take any necessary action to remove mispunched cards from the card files.

IBM 523 or 544 Card Punches can be used in place of the Control Data 415 Card Punch. These IBM card punches operate at 100 and 250 cards per minute, respectively, and are functionally equivalent to the Control Data 415 except that they have no provision for offsetting mispunched cards.

There are three different Card Punch Controllers, any one of which can control one card punch unit. The controllers differ in their buffering provisions and in the number of data channels which can be connected. The available controller models and their major characteristics are as follows:

Model 3245:	unbuffered	one data channel connection.
Model 3446:	full-card buffer	one data channel connection.
Model 3644:	full-card buffer	two data channel connections.

The Card Punch Controllers intervene between the computer system and the card punch itself. The available program facilities differ depending on which controller is used. The differences in program facilities are:

- Error checking: Where the controller does not have a full-card buffer, the hole count reported by the post-punch read station cannot be used because no equivalent hole-count of the card image exists; therefore, no comparison between the two counts can be made.
- Card Punch Coding: Where the controller does not contain a full-card buffer, the computer must provide the data in exactly the form in which it is to be punched.

.12 Description (Contd.)

Where the controller does contain a full-card buffer, the data can be supplied in BCD column-by-column format and automatically "turned around" in the buffer and converted to the row-by-row format required by the card punch without any program supervision. At the same time, automatic conversion from internal BCD to Hollerith coding can occur if desired.

- Switching Between Computer Systems: Where the controller can be physically connected to two data channels, it is possible to switch the card punch unit from one computer system to the other by connecting the two data channels to different computer systems and using either channel as required. Special instructions are available to reserve the punch for one system at a time, to allow for controlled operation.

A single card punch instruction defines an area in core storage whose contents are to be punched out. As many cards as are needed to accommodate all of the data in the designated area will be punched in response to the instruction.

Interruptions can be set to occur when the card punch becomes available, when an operation is successfully completed, or when for some reason an operation ends without being successfully completed. The program can inhibit any or all of these three separate and distinct interrupt conditions.

In addition to the interrupt system, status indicators show whether the unit is currently able to respond to an instruction, what interrupt conditions are presently activated, and whether there has been a failure to feed a card.

Each card punch must have its own individual controller, so the number of card punches that can be connected to a computer system is related to the number of data channels and the number of selectable positions on each data channel.

The load on the core storage for the Control Data 3200 computer system is only 25 microseconds per punched card, which at the rated speed of 250 cards per minute is negligible. However, the data to be punched must often be prepared in BCD coding, and then (where an unbuffered controller is used) massaged into row-by-row form, so the actual load on the computer system imposed by card punch operations may be considerably higher.

The 415 Card Punch is manufactured by Control Data Corporation.

.13 Availability: . . . . 4 months.

.14 First Delivery: . . . . . December 1964.

INPUT–OUTPUT: PAPER TAPE READER/PUNCHES

§ 073.

.1 GENERAL

.11 Identity: . . . . 3691 Paper Tape Reader/Punch.
3694 Paper Tape Reader/Punch.

.12 Description

.121 3691 Paper Tape Reader/Punch

The 3691 Paper Tape Reader/Punch is a free-standing unit, which in its normal version is 36 inches high, 28 inches deep, and nearly 48 inches wide. A "ruggedized" version, built to withstand adverse physical conditions, has different dimensions, which are summarized in the Physical Characteristics section of this Computer System Report, on page 245:211.100.

The 3691 contains logically separate reading and punching sub-units and a single data channel connection for their joint use. The single data channel connection makes it impossible to run the reader and the punch concurrently. Spooling facilities are not provided.

The Paper Tape Reader operates at a peak speed of 350 characters per second, in the forward direction only. A Control Data Model 350 photoelectric reader is currently being used.

The Paper Tape Punch is suppled by the National Cash Register Company, and operates at a rated speed of 110 characters per second.

Five, seven, or eight-level paper tape can be used by either unit; a manual switch selection and tape width adjustment are required when a different type of paper tape is mounted. There are no provisions for automatically checking the parity of the characters on the paper tape itself, and any required checking or preparation of parity-checked characters must be handled by the program. Each tape character can be read into, or punched from, a separate computer word location, or alternatively a number of characters can be packed into a single word. In the packed format, a 24-bit computer word stores either four 5-bit characters or two 7-bit or 8-bit characters. Conversion to or from the appropriate internal code must be accomplished by programming.

Interruptions are controlled by the program and can occur when the unit becomes available, when an operation ends successfully, or when for some reason an operation ends without being successfully completed.

In addition to the interrupt system, status indicators show whether the unit is ready to respond to an instruction, which of the three interrupt conditions are currently activated, whether the punch tape supply is low, and whether the punch or the reader unit were last connected to the data channel.

The load on the core storage will depend upon the operating speed of the unit, and on whether one character per word or the packed format is being used. In no case with the Control Data 3200 computer system will the loading exceed 0.05% of a single core storage module's throughput capacity.

.122 3694 Paper Tape Reader/Punch

The 3694 Paper Tape Reader/Punch is a free-standing unit, about 60 inches high, 24 inches deep, and 42 inches wide. A large proportion of the total space is taken up by the spooling facilities which are a feature of this unit. Two separate data channels can be connected to the self-contained control mechanism within the 3694 Paper Tape Reader/Punch, so that concurrent paper tape reading and punching can take place.

The Paper Tape Reader operates at a peak speed of 1,000 characters per second, using standard paper or plastic tape with fully-punched holes. Reading operates photoelectrically, in either the forward or reverse direction. Control Data is currently using a Digitronics Corporation paper tape reader for this unit.

The Paper Tape Punch is supplied by the National Cash Register Corporation, and operates at a rated speed of 110 characters per second.

Five, seven or eight-level paper tape can be used by either unit; a manual switch selection and tape width adjustment are necessary when a different type of paper tape is mounted. Character parity can be optionally used on both reading and punching, under program control. Each tape character can be read into, or punched from, a separate computer word location, or alternatively a packed format can be used. In the packed format, a 24-bit computer word stores either four 5-bit characters or two 7-bit or 8-bit characters. Conversion to or from the appropriate internal code must be accomplished by programming.

Interruptions can be controlled by the program and can occur when the unit becomes available, when an operation ends successfully, or when for some reason an operation ends without being successfully completed.

.13 Availability: . . . . 6 months.

.14 First Delivery

3691 Paper Tape Reader/Punch: . . . . . 1963.
3694 Paper Tape Reader/Punch: . . . . . July, 1964.

INPUT-OUTPUT: 3152 LINE PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . 3152 Line Printer.

.12 Description

The Control Data 3152 Line Printer operates at up to 150 single-spaced alphanumeric lines per minute. It contains its own control unit, which is connected to a single data channel, and a 120-character line buffer. The 3152 is a drum printer, normally using a 63-character drum, although alternative drums are available. The drum revolution time is 400 milliseconds, and an infinite clutch is used so that asynchronous printing is possible. Paper control is handled either by the program directly, or by a combination of the program and a 6-level format tape. Skipping over non-printed areas takes place at approximately 100 line-spaces per second. The effective speed of the 3152 Printer, including allowances for paper advance, is summarized in Table 1.

Program facilities include printing with single or double spacing, page ejection, and automatic advancing to the last line of a page. In conjunction with the 132-position, 6-level format loop which is mounted by the operator before printing starts, the program can instruct the paper to be positioned at the line position corresponding to the next punched hole in the specified channel of the format tape. All paper-positioning instructions can take place either before or after printing, as the program directs.

.12 Description (Contd.)

Interrupts can be set to occur when the printer becomes available, when an operation is successfully completed, or when for some reason an operation ends without being successfully completed. The program can inhibit any or all of these three interrupt conditions.

In addition to the interrupt system, status indicators show whether the printer is ready to respond to an instruction, which of the three interrupt conditions are currently activated, whether the paper supply is exhausted, or whether the printed form is positioned at the last line of the page.

The load imposed on the core storage by the print operation amounts, in the Control Data 3200 computer system, to only 37.5 microseconds per printed line, which is negligible even at the top speed of 150 lines per minute. The data to be printed must be supplied in 6-bit BCD code, packed four characters per word. Preparing the data in this form may require many programmed code conversion operations. These operations will usually form the greater part of the system overhead incurred through a printing operation.

The 3152 Printer is manufactured by Control Data Corporation.

.13 Availability: . . . . 4 months.

.14 First Delivery: . . . . . June, 1963.

TABLE I: EFFECTIVE SPEED OF THE CDC 3152 PRINTER

Lines Advanced per Line Printed	Printed Lines per Minute Using AUERBACH Standard Character Set*
1	150
2	150
3	150
4	150
5	150
6 (1 inch)	150
12 (2 inches)	118
18 (3 inches)	108
24 (4 inches)	100
30 (5 inches)	90

* 0-9, A-Z, minus, comma, period, dollar sign.

INPUT–OUTPUT: IBM 1403 PRINTER

§ 082.

.1 GENERAL

.11 Identity: . . . . IBM 1403 Printer, Models 2 and 3.
CDC Line Printer Controller, Model 3258.

.12 Description

Either Model 2 or Model 3 of the IBM 1403 Printer can be connected to a Control Data 3000 Series computer system by means of a Model 3258 Line Printer Controller. A separate controller is required for each printer which is to be connected to the computer system. Theoretically, up to 64 printers could be connected to a single Control Data 3200 computer system by connecting 8 printers to each of the 8 possible data channels.

The IBM 1403 Model 2 operates at a peak speed of 600 lines per minute and uses a horizontal-chain printing mechanism. The 1403 Model 2 is described in detail in the IBM 1401 Computer System Report, on page 401:081.100. The newer Model 3 can operate at 1,100 alphanumeric lines per minute, using a train of type slugs which move through a horizontal channel. The 1403 Model 3 is described in detail in the IBM 1410 Computer System Report, on page 402:082.100.

.12 Description (Contd.)

Interrupts can be set to occur when the printer becomes available, when an operation is successfully completed, or when for some reason an operation is ended without being successfully completed. The program can inhibit any or all of these three separate and distinct interrupt conditions.

In addition to the interrupt system, status indicators show whether the printer is available to respond to an instruction, what interrupt conditions are presently in operation, or whether the paper supply is exhausted.

The load imposed on the core storage by a printing operation on the Control Data 3200 computer system is only 41.25 microseconds per printed line, which is negligible. However, the data to be printed must be in 6-bit BCD code and must be packed, four characters per word, into an output area. Preparing the data in this form may involve many programmed code conversion operations. These operations, rather than the transferring of data into the printer controller buffer, will form the greater part of the system overhead incurred through a printing operation.

.13 Availability: . . . . ?

.14 First Delivery: . . . . . Oct. 1964.

INPUT–OUTPUT: 501 AND 505 LINE PRINTERS

§ 083.

.1 GENERAL

.11 Identity: . . . . 501 Line Printer.
505 Line Printer.

3256 Line Printer Controller.
3659 Line Printer Controller.

.12 Description

The Control Data 501 and 505 Line Printers operate at up to 1,000 and 500 single-spaced alphanumeric lines per minute, respectively. Except for their operating speeds, the two units are functionally identical. Each printer contains its own 136-character line buffer and can be connected to the computer system through either the single-channel 3256 Line Printer Controller or the dual-channel 3659 Line Printer Controller. The major advantage of the dual-channel control is that the two channels can be connected to different computer systems, making it possible to switch the printer from one computer system to another.

Physically, the printer is enclosed in a four-foot-high cabinet, similar to those used for peripheral control equipment. The cabinet has semi-translucent front panels, through which the operator can observe the printing operation. The use of the cabinet reduces the noise level during printing.

Both the 501 and the 505 are drum printers, and both normally employ a 63-character drum, although alternative drums are available. The drum revolution time is 60 milliseconds on the 501 and 120 milliseconds on the 505; an asynchronous clutch is used so that printing of a line can be initiated at any time.

Paper control is handled by the program, either directly or in conjunction with the 6-level format tape. Skipping over non-printed areas takes place at 150 line-spaces per second. The effective speeds of both printers, including allowances for paper advance, are summarized in Table I.

Program facilities include printing with single or double spacing, page ejection, and an automatic advance to the last line of a page. In conjunction with the 132-position, 6-level format loop which is mounted by the operator before printing starts, the program can instruct the paper to be positioned at the line position corresponding to the next hole punched in the specified channel of the format tape. All paper-positioning instructions can take place either before or after printing, as the program directs.

Interrupts can be set to occur when the printer becomes available, when an operation is successfully completed, or when for some reason an operation ends without being successfully completed. The program can inhibit any or all of these three separate and distinct interrupt conditions.

In addition to the interrupt system, status indicators show whether the printer is available to respond to an instruction, which of the three interrupt conditions are currently activated, whether the paper supply is exhausted or the paper torn, or whether the printed form is currently positioned at the last line of the page.

Each printer must have its own controller, so the number of printers which can be connected to a computer system is related to the number of data channels and the number of selectable positions on each data channel. There can be 8 data channels on a CDC 3200 computer system and each channel has 8 selectable positions, so the theoretical maximum numbers of printers per system is 64.

The load on the core storage amounts, in the Control Data 3200 computer system, to only 42.5 microseconds per printed line, which is negligible even at the top speed of 1,000 printed lines per minute. However, the data to be printed must be in 6-bit BCD code and must be packed, four characters per word, into an output area. Preparing the data in this form may involve many programmed code conversion operations. These operations will usually form the greater part of the system overhead incurred through a printing operation.

The 505 and 501 Printers are manufactured by Control Data Corporation.

.13 Availability: . . . . . 4 months.

.14 First Delivery

501 Printer: . . . . . June 1964.
505 Printer: . . . . . Spring 1965.

§ 083.

TABLE I: EFFECTIVE SPEEDS OF CDC 501 AND 505 PRINTERS

	Printed Lines per Minute Using AUERBACH Standard Character Set*	
Lines Advanced per Line Printed	501 Printer	505 Printer
1	1,000	500
2	750	500
3	714	500
4	667	400
5	600	375
6 (1 inch)	571	375
12 (2 inches)	416	300
18 (3 inches)	333	250
24 (4 inches)	267	215
30 (5 inches)	227	187

* 0-9, A-Z, minus, comma, period, dollar sign.

INPUT-OUTPUT: 7-TRACK MAGNETIC TAPE UNITS

§ 091.

.1 GENERAL

.11 Identity: . . . . Control Data 601 through 607 Magnetic Tape Units, and associated Magnetic Tape Controllers.

.12 Description

The Control Data 600 Series of magnetic tape units includes both 7-track and 9-track equipment. The 7-track tape units use one parity bit and six data bits in each tape row. These units, which are compatible with the IBM 729 Magnetic Tape Units and other equivalent units, are described in this section and summarized in Table I. The 9-track units, which use eight data bits and one parity bit in each tape row and are compatible with the IBM 2400 Series magnetic tape units used in the IBM System/360, are described in the next section of this Computer System Report, on page 245:092.100. Compatibility between the two groups of units is limited to their mutual use of one-half-inch magnetic tape reels as a recording medium, and to the possible modification of 9-track units so that they can read or write 7-track magnetic tape instead of (not as well as) 9-track magnetic tape.

The peak data transfer rates of the 7-track magnetic tape units vary from 20,850 to 120,000 characters per second, depending upon which specific unit is in use. The loading on the Control Data 3200 core storage modules during data transmission is one memory cycle (1.25 microseconds) per 24 data bits, and amounts to between 0.6% and 3.7% of the total

.12 Description (Contd.)

throughput capacity of a single core storage module, depending directly on the data transfer rate.

The effective data transfer rates are controlled by the time taken to pass over the inter-block gap and the length of each physical tape block. All Control Data 7-track magnetic tape units use the IBM-compatible three-quarter-inch inter-block gaps, so that their performance when the tape speed is low and short blocks are in use is not as high as that of other magnetic tape units which have otherwise identical specifications but which are able to use shorter inter-block gaps (e.g., the Honeywell 204B Series).

The Control Data Magnetic Tape Unit Controllers can control a maximum of from 4 to 16 tape units each, depending on which model is selected (see Table II). All the tape units connected to a particular controller must be 7-track units with the same physical tape speed.

Each controller can handle as many simultaneous data transmissions as it has data channels connected to it. Models are available with one, two, three, or four possible data channel connections. Where there are multiple data channels connected to a single magnetic tape controller, it is not necessary that each data channel be connected to the same Control Data 3000 series computer system. Where there are two computers at a single site, it is common practice to connect a single tape controller to both computer systems. This allows both computers to use any of the magnetic tape units connected to the controller, and eliminates the necessity for special switching devices.

TABLE I: CHARACTERISTICS OF THE CDC 7-TRACK MAGNETIC TAPE UNITS

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, char per sec	Interblock Gap Lengths			Efficiency, %(3)		Demand on Core Storage, % (4)	Rewind Speed, inches per sec
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks		
601	37.5	556 200	20,850	0.75 0.75	20.0 20.0	417 150	19% 40%	71% 87%	0.6% 0.2%	200
603	75.0	556 200	41,700	0.75 0.75	10.0 10.0	417 150	19% 40%	71% 87%	1.3% 0.5%	350
604	75.0	800 556 200	60,000	0.75 0.75 0.75	10.0 10.0 10.0	600 417 150	14% 19% 40%	62% 71% 87%	1.9% 1.3% 0.5%	350
606	150.0	556 200	83,400	0.75 0.75	5.0 5.0	417 150	19% 40%	71% 87%	2.6% 0.9%	350
607	150.0	800 556 200	120,000	0.75 0.75 0.75	5.0 5.0 5.0	600 417 150	14% 19% 40%	62% 71% 87%	3.7% 2.6% 0.9%	350

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.
(2) Number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.
(4) Percentage of total available CDC 3200 core storage cycles used to service magnetic tape units during data transmissions.

§ 091.

.12 Description (Contd.)

The 7-track magnetic tape units can use pure binary or BCD formats and can read backward as well as forward. Writing must always operate in the forward direction. Searching backward or forward to find a file mark, and rewinding with or without automatic unloading of the tape reel, can be handled by the magnetic tape subsystem independently of the computer once the operation has been initiated.

Program interruptions can be initiated under three separate conditions: when a tape unit becomes available, when an operation ends normally (i.e., successfully), and when something has prevented an operation from being successfully completed. The program can select which types of interruption it will allow a specific controller to initiate. Different controllers, or different data channels connected to the same controller, can be concurrently using different sets of interrupt conditions. There are 11 status codes which can be tested by the program. These status codes must be used to identify the cause of an interrupt, but they are also available for use whenever required. They indicate whether a tape unit is available or not; whether the tape is positioned at a file mark, at the load point, or at the physical end of the tape; what density is currently being used, whether writing is permitted, and whether data has been lost through timing conflicts or is of dubious value because of the known occurrence of a transverse or longitudinal parity error.

Because of the wide capability range of both the magnetic tape units themselves and the associated controllers, the comparative prices of the different components are particularly important. These are listed in the Price Data section of this Computer System Report, which starts on page 245:221.101.

.13 Availability: . . . . . 6 months.

.14 First Delivery

Model 601 . . . . . . January 1965.
Model 603 . . . . . . March 1963.
Model 604 . . . . . . May 1964.
Model 606 . . . . . . August 1962.
Model 607 . . . . . . May 1964.

.2 PHYSICAL FORM

Each tape drive is a single unit. The drive past the read, write, and erase heads uses pneumatic capstans. The magnetic tape passes through vacuum reservoirs immediately before and after passing under the heads themselves. The vacuum reservoirs are vertical and can hold about seven feet of tape except on the tape units which operate at 37.5 inches per second; on these units the reservoirs are placed horizontally and have a capacity of about three feet of tape.

There are three heads, the erase head followed by the write head and the read head. The gaps between the heads are 0.4375 inches between the erase and write heads, and 0.3 inches between the write and read heads.

.3 EXTERNAL STORAGE

The Control Data 600 Series magnetic tape units use one-half-inch plastic tape. Normally 2,400-foot reels are used, but some installations are successfully using 3,600-foot reels with these tape units.

The coding used is exactly the same as that used with the IBM 729 Magnetic Tape Units.

.4 CONTROLLERS

All tape units must be connected to a controller. The wide range of available controllers is shown in Table II.

.5 PROGRAM FACILITIES AVAILABLE

The tape units can read a single block in the forward or reverse direction, or write a block in the forward direction only. The size of the block is determined by the amount of storage specified as the input or output area in the instruction, and is limited only by the amount of core storage available. An end-of-file mark can be written and is preceded by a 6-inch gap. Search operations to find the end-of-file mark can be conducted in either direction. A special instruction is available to erase 6 inches of tape, in order to skip over a bad spot on the tape.

TABLE II: CONTROLLERS FOR CDC 7-TRACK MAGNETIC TAPE UNITS

Controller Model	No. of Channels	Max. No. of Tapes	Acceptable Tape Unit Models*
3127	1	4	601
3228	1	4	604 or 607
3229	1	8	604 or 607
3421	2	4	604 or 607
3422	2	6	604 or 607
3423	2	8	604 or 607
3622	2	16	606 or 607
3625	3	8	606 or 607
3626	3	16	606 or 607
3623	4	8	606 or 607
3624	4	16	606 or 607

* Tape units with different tape transport speeds must not be connected to the same magnetic tape controller.

§ 091.

.5 PROGRAM FACILITIES AVAILABLE (Contd.)

The program can select either binary or BCD codes, and can request interrupts to occur when a tape unit becomes available, when an operation is completed normally, or when an operation is completed in some abnormal manner.

The current status of a tape unit can be tested at any time. Special status indicators show: whether the unit is available or not; whether the tape is positioned at a file mark, at the load point, or whether it is approaching the physical end of the tape; what density is currently being used; and whether the tape reel presently mounted can be written on. Error status indicators show whether any data has been lost through timing conflicts or whether any parity errors have been found.

.6 PERFORMANCE

The major performance characteristics of the Control Data 600 Series of magnetic tape units (7-track) are summarized in Table I. The effective speed of any particular tape unit at any particular block size can be calculated by using the formula "Effective speed = Peak speed x Block length in chars/(Block length + Interblock gap length in chars)." The required values are included in Table I. Alternatively, the effective speeds can be read from the graphs at the end of this section.

.7 EXTERNAL FACILITIES

The unit number is displayed on a dial at the top of the unit. There are ten positions, eight of which are marked 1 through 8 and two marked "stand-by."

.7 EXTERNAL FACILITIES (Contd.)

Single button controls are used to bring the mounted tape to the load point and to prepare a tape reel for dismounting. Loading and unloading a reel of tape takes approximately one minute, and the tape unit must be stopped while this is done.

The peak frequency of reloading is directly related to the tape transport speed, and is once every 13, 6.5, or 3.25 minutes for units with tape speeds of 37.5, 75, and 150 inches per second, respectively.

.8 ERRORS, CHECKS AND ACTION

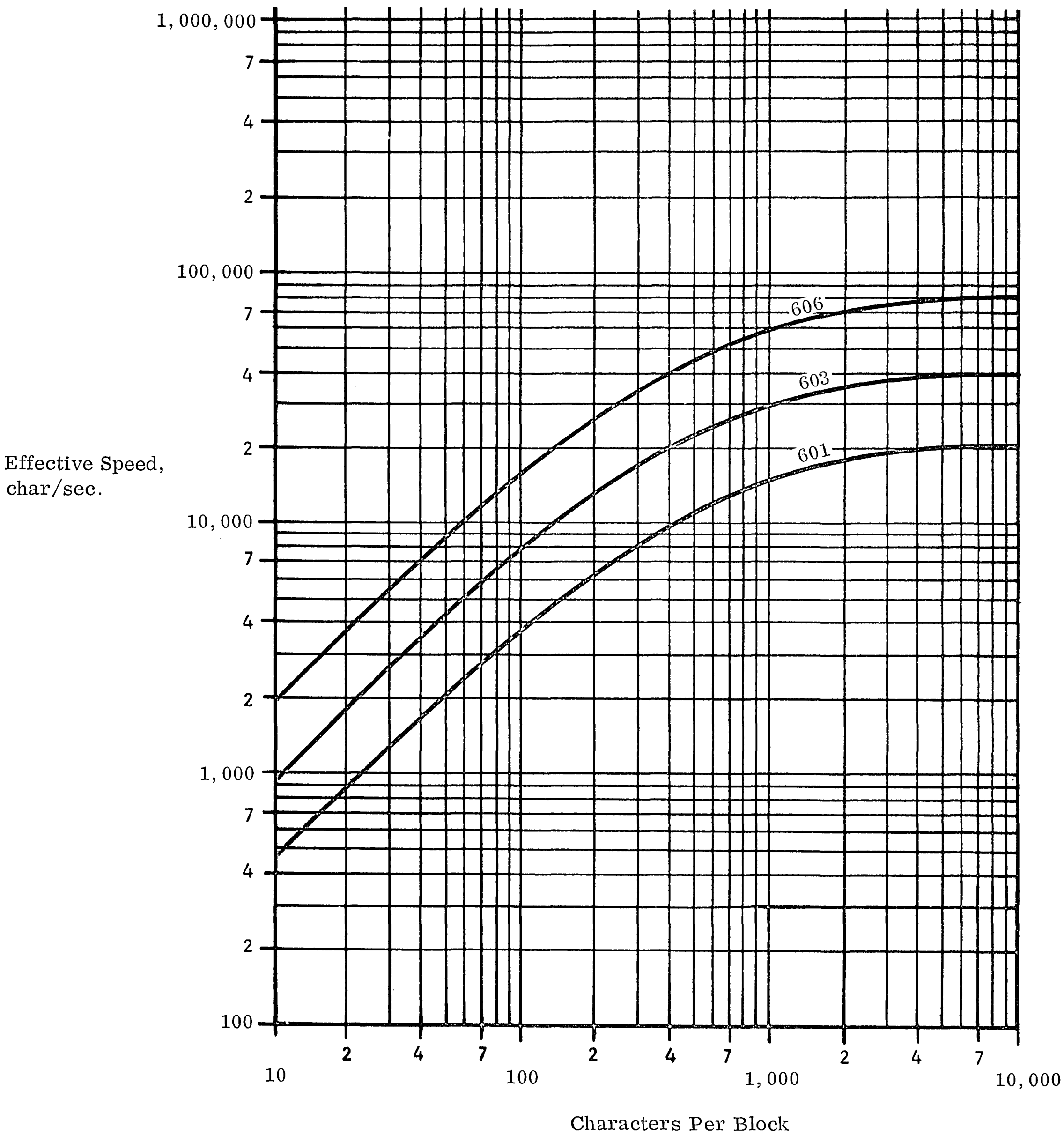
Errors which result in the failure of parity checks cause an indicator to be set and (at the option of the programmer) an interrupt. Such errors may be noted either during the automatic read-back operation, which occurs while writing is in progress, or during normal reading. Two parity checks are made, one on each 6-bit data character transferred and one on the longitudinal parity character at the end of each physical tape block.

Errors which arise from timing conflicts and which lead to a loss of data are similarly handled, by setting an indicator and providing for an optional interrupt.

Checks are made for the approaching end of the tape, and for a match between the actual length of an incoming tape block and the input area set aside to receive the block. Interrupt and indicator actions are available to notify the program of the result of these checks. No explicit check is made upon the adequacy of the plastic tape itself; reliance is placed upon the parity checks on the data recorded on the tape.

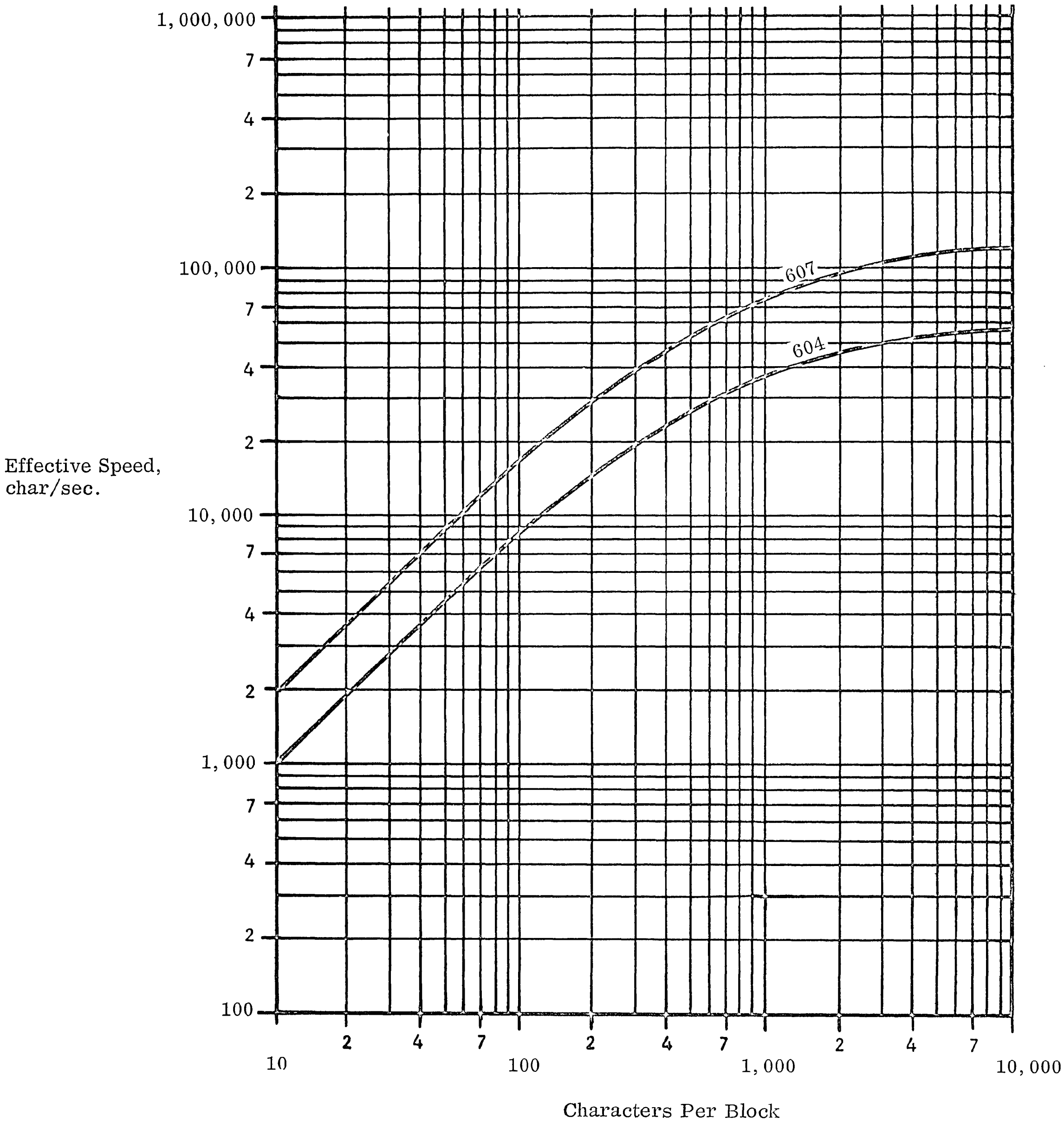
§ 091.

EFFECTIVE SPEED: CDC 601, 603 AND 606 MAGNETIC TAPE UNITS
(Recording density: 556 char/inch)



§ 091.

EFFECTIVE SPEED: CDC 604 AND 607 MAGNETIC TAPE UNITS
(Recording density: 800 char/inch)



INPUT–OUTPUT: 9–TRACK MAGNETIC TAPE UNITS

§ 092.

.1 GENERAL

.11 Identity: . . . . Control Data Magnetic Tape Units, Models 692, 694, 696, and associated controllers.

.12 Description

Control Data has announced a series of 9-track magnetic tape units which are to be compatible with the new IBM 2400 Series tape units. The IBM 2400 Series units are described in the IBM System/360 Computer System Report, on page 420:091.100; their major innovations are the use of eight data bits and one parity bit in each tape row, and the addition of a cyclic (or diagonal) check character to each tape block.

The peak speeds of the Control Data 692, 694, and 696 tape units are 30,000, 60,000, and 90,000 eight-bit bytes per second, respectively. These speeds are functionally equivalent to 40,000, 80,000, and 120,000 six-bit characters per second, respectively, unless the data is recorded in the 8-bit Extended BCD or 4-bit packed decimal codes used in the IBM System/360.

Models 3825, 3826, and 3827 controllers have been announced for the 692, 694, and 696 tape units. The ratio of data channel connections to magnetic tape unit connections is unusually high, one data channel being provided for every two magnetic tape units which can be connected. Preliminary indications are that it will be possible to connect any of the three 9-track tape unit models to any of the three controller models. The number of magnetic tape units and data channels that can be connected to each controller model are as follows:

Controller Model:	3825	3826	3827
Magnetic Tape Units:	4	6	8
Data Channels:	2	3	4

Delivery dates of the 692, 694, and 696 magnetic tape units have not been specifically announced by Control Data, but first deliveries are expected to take place as soon as IBM delivers its 2400 Series tape units.

INPUT–OUTPUT: SATELLITE COUPLER

§ 101.

.1 GENERAL

.11 Identity: . . . . 3682 Satellite Coupler.
3681 Data Channel Converter.

.12 Description

The 3682 Satellite Coupler is used to allow a computer system to communicate directly with another, physically adjacent system. The basic technique involved is that an input-output channel is used, and request and control signals from computer system A to computer system B are received in the same way as the equivalent status signals from any input-output unit. When the appropriate signals have passed, an input-output instruction will transfer data directly from one computer to the other computer memory at a speed limited only by the memory cycle timing of the slower computer.

This arrangement will usually be used to connect a large computer to a smaller one. Three examples of such connections are illustrated below. The Control Data 3400 could utilize a Satellite Coupler to connect:

- A 3200 to a smaller system (Control Data 160-A or 3100);

.12 Description (Contd.)

- Two 3200 systems together;
- A 3200 system to a larger system (Control Data 3600 or 6600);
- Several like or unlike systems, to form a "ring" of interconnected computer systems. (System "A" could be connected to system "B" and "Z"; system "B" to system "C" and "A", etc.).

The programming systems required for the control of all but the simplest cases of these multi-computer configurations may well be complex. In general, their design is the responsibility of the installation itself, since at the present time it is unusual to find two installations with the same needs.

If one of the interconnected computer systems is the Control Data 160-A, a 3681 Data Channel Converter is required in addition to the 3682. The differentiation between the 3681 and 3682 is that the 3681 simulates the appropriate 3000 series data channel, while the 3682 (which is made up of two identical elements acting as buffers between the two systems) buffers and controls the data transmissions themselves.

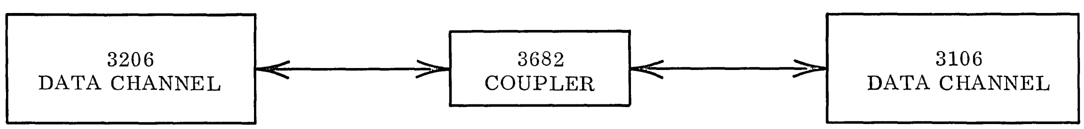


Fig. 1: Coupling of a Control Data 3200 system to a 3100 system.

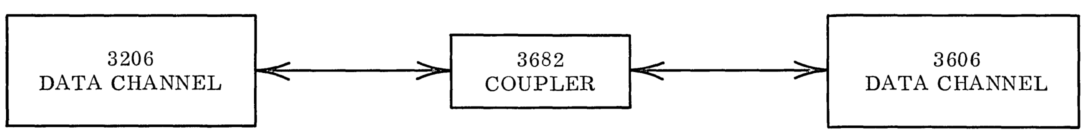


Fig. 2: Coupling of a Control Data 3200 system to a 3600 system.

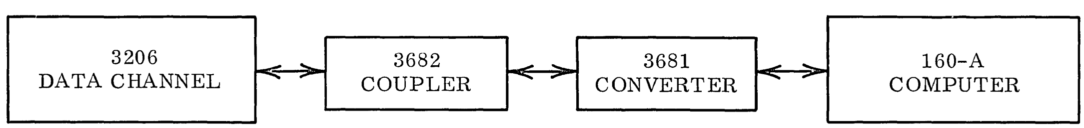


Fig. 3: Coupling of a Control Data 3200 system to a 160-A system.

INPUT-OUTPUT: 3293 INCREMENTAL PLOTTER

§ 102.

.1 GENERAL

.11 Identity: . . . . Control Data 3293 Incremental Plotter.
Calcomp Digital Incremental Plotters, Models 563, 564, 565, and 566.

.12 Description

The Control Data 3293 Incremental Plotter incorporates any one of the Models 563 through 566 Digital Incremental Plotters manufactured by California Computer Products, Inc. These plotters vary in speed (from 12,000 to 18,000 steps per minute), in step size (0.01 or 0.005 inch), and in chart width (from 12 to 31 inches). The details of each specific model are shown in Table I. (For general information about the characteristics and applications of digital plotters, see the Special Report on page 23:070.100.)

The Calcomp plotters are two-axis recorders for plotting one variable against another. Each plotter consists of a ballpoint pen mounted on a carriage and a bidirectional recording drum. Output words from the computer direct pen carriage movement and drum rotation as well as the movement of the pen against or away from the recording surface.

The pen carriage moves in the X axis (horizontally), and the drum moves in the Y axis (vertically). The two movements are independent, so that it is possible to instruct movements in both directions to take place at the same time, resulting in slant movements.

Interrupts can be set to occur when the plotter becomes available, when an operation is successfully completed, or when for some reason an operation is ended although not successfully completed. The program can inhibit any or all of these three separate interrupt conditions.

In addition to the interrupt system, six indicators are used to record the present status of the plotter. These indicators show which of the three interrupt conditions are active, whether the plotter is busy, or whether some manual adjustment is in progress. The possible manual processes include high-speed vertical and horizontal paper movement for initially setting the paper and the pen in the proper relative positions.

TABLE I: CHARACTERISTICS OF CALCOMP PLOTTERS USED WITH CDC 3293

Calcomp Model No.	Model 563	Model 564	Model 565	Model 566
Chart width, inches	31.0	31.0	12.0	12.0
Plotting width, inches	29.5	29.5	11.0	11.0
Chart length, feet	120.0	120.0	120.0	120.0
Step size, inches	0.01	0.005	0.01	0.005
Steps per minute	12,000	18,000	18,000	18,000
Milliseconds per pen movement	90.0	90.0	90.0	90.0

SIMULTANEOUS OPERATIONS

§ 111.

1. GENERAL

The Control Data 3200 system allows for the connection of up to eight input-output data channels. Each data channel is serviced by a bi-directional, 12-bit parallel interface unit called the 3206 Standard Communication Channel†. Up to eight different peripheral equipment controllers can be connected to one 3206. These facilities make it possible for up to eight input-output operations on any of 64 different controllers to proceed simultaneously with computation.

A choice of single- and dual-channel controllers is available for the card and printer equipment. Full line buffers are included with each of the printer controllers, but card buffers are optional depending upon the choice of card reader or card punch controller. The magnetic tape units, paper tape units, and typewriter simply have 12-bit interfaces.

Magnetic tape controllers can be selected from among 8 different units that provide from 1 to 4 channel accesses, and which are capable of controlling from 1 to 16 tape transports. Thus, if enough data channels are available, from one to four tapes on each controller can be operational in any combination, in addition to non-magnetic-tape peripherals and the processor.

The so-called "block" operations (Search and Move) can also occur in parallel with the main computational process, once they have been initiated. The Search instruction initiates a search through a block of character storage addresses looking for equality or inequality with a character contained in the instruction word. The Move order is used to move a block of n characters from one area of storage to another. It should be noted, however, that no real advantage results from this feature if the program requires access to the same storage module as that involved in the block operation. As a result, careful program design is required to realize the potential benefits of these overlapped internal operations.

The input-output operations are of two types: character-block transfers and word-block transfers. Character operations permit either 6 or 12 bits to be transferred in parallel between core storage and the peripheral channel, while word operations allow 24-bit transfers. Each input-output transfer is initiated after a series of instructions which connect the desired channel, test for "busy" or other status conditions in the input-output equipment, and select the desired function. The input-output transfer instruction (a two-word instruction) is then issued to start the transfer.

† A 24-bit interface unit (the 3207 Special Comunication Channel) can be used in place of two 3206 units.

.1 GENERAL (Contd.)

After the starting and ending addresses for the transfer are stored in reserved locations of the processor's fast register file, the main program is released from further control of the input-output operation. For each transfer, the Communication Channel issues a data transfer request to both the input-output equipment and the priority controls of the register file. The character or word address is then delivered from the register file to the core storage address control, and the data transfer is made between storage and the data channel. The starting address is incremented and the entire transfer sequence repeated until the operation is complete, as evidenced by the starting address becoming equal to the ending address. An automatic interrupt can be specified to notify the program immediately upon completion of the transfer.

Each four-character word transferred uses one core memory cycle (1.25 microseconds) during its accession or storage, and a further three Register File cycles (0.5 microseconds) are used to control the transfer operation. During these operations the central processor is unable to gain access to the core storage module involved, or to the Register File, so computation is delayed. The probable delaying effect which input-output operations will have on processing can be calculated using the core storage utilization figures which are listed for all the standard peripheral units in Table I. Where two or more core storage modules are incorporated into a single computer system, it may be possible to reduce such processor delays by overlapping storage references.

.2 RULES

The following processes can take place simultaneously:

- One computation; plus
- One "block" operation (Search or Move); plus
- A console key-in operation; plus
- As many buffered input-output operations* as there are buffers (up to about 50); plus
- As many non-buffered input-output operations** as there are data channels (a maximum of 8 channels); plus

* The present printers are always buffered; card equipment is optionally buffered.

** Paper tape, magnetic tape, and random access drum and disk operations are non-buffered; the number of such operations may also be restricted by the manner in which the controllers are connected to the data channels.

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.2 RULES (Contd.)

- As many "non-supervised" peripheral operations*** as there are appropriate units.

*** Magnetic tape rewinding, backspace operations, and searching for file marks, disk arm positioning and address search operations are typical "non-supervised" peripheral operations.

.2 RULES (Contd.)

The number of concurrent input-output operations may also be limited by maximum throughput capacity of the computer system, which is 2,666,666 characters per second.

TABLE I: SIMULTANEOUS OPERATIONS

DEVICE	Cycle Time, msec.	Start Time			Data Transmission			Stop Time		
		Time, msec.	Core Use	Channel Use	Time, msec.	Core Use	Channel Use	Time, msec.	Core Use	Channel Use
828, 838 Disk Files	---	250 av	0.0	1 msec	Var	2.1 or 3.4%	Yes	0.0	---	---
1311 Disk Storage Drive	---	170 or 270 av	0.0	1 msec	Var	2.4%	Yes	0.0	---	---
2311 Disk Storage Drive	---	97.5 av	0.0	1 msec	Var	6.4%	Yes	0.0	---	---
3235 Drum Storage	34.4	17.2 av	0.0	1 msec	Var	5.0%	Yes	0.0	---	---
861 Drum Storage	34.4	17.2 av	0.0	?	Var	(62/I)%	Yes	0.0	---	---
862 Drum Storage	17.2	8.6 av	0.0	?	Var	(62/I)%	Yes	0.0	---	---
405 Card Reader 1,200 cpm, unbuffered	50.0	18.0	0.0	Yes	32.0	3.0%	Yes	0.0	---	---
405 Card Reader 1,200 cpm, buffered	50.0	42.0	0.0	Yes	8.0	12.5%	Yes	0.0	---	---
415 Card Punch 250 cpm, unbuffered	240.0	48.0	0.0	Yes	190.0	1.1%	Yes	2.0	0.0	No
415 Card Punch 250 cpm, buffered	240.0	48.0	4.4%	2.2 msec	190.0	0.0%	No	2.0	0.0	No
523 Card Punch 100 cpm, unbuffered	600.0	84.0	0.0	Yes	514.0	0.4%	Yes	2.0	0.0	No
523 Card Punch 100 cpm, buffered	600.0	84.0	2.8%	2.2 msec	514.0	0.0%	No	2.0	0.0	No
544 Card Punch 250 cpm, unbuffered	240.0	48.0	0.0	Yes	190.0	1.1%	Yes	2.0	0.0	No
544 Card Punch 250 cpm, buffered	240.0	48.0	4.4%	2.2 msec	190.0	0.0%	No	2.0	0.0	No
3691 Paper Tape Reader 350 cps	2.9	? ?	0.0	Yes	2.9	<0.05	Yes	2.0	0.0	No
3691 Paper Tape Punch 110 cps	9.0	?	0.0	Yes	9.0	<0.02	Yes	3.0	0.0	No
3694 Paper Tape Reader 1,000 cps	1.0	?	0.0	Yes	1.0	<0.2%	Yes	0.8	0.0	No
3694 Paper Tape Punch 110 cps	9.0	?	0.0	Yes	9.0	<0.02%	Yes	3.0	0.0	No
3152 Line Printer 150 lpm	400 + 9.7LS	0	---	---	375	<0.01%	0.1msec	25 + 9.7LS	0.0	No
1403 Model 2 Printer 600 lpm	100 + 5LS	0	---	---	80	<0.1%	0.1msec	20 + 5LS	0.0	No
1403 Model 3 Printer 1,100 lpm	55 + 5LS	0	---	---	35	<0.2%	0.1msec	20 + 5LS	0.0	No
501 Printer 1,000 lpm	60 + 6.7LS	0	---	---	45	<0.1%	0.1msec	13 + 6.7LS	0.0	No
505 Printer 500 lpm	120 + 6.7LS	0	---	---	105	<0.05%	0.1 msec	13 + 6.7LS	0.0	No
601 Magnetic Tape Unit 20.8 KC	---	3.0	0.0	Yes	Var	0.6	Yes	3.0	0.0	No
603 Magnetic Tape Unit 41.7 KC	---	2.75	0.0	Yes	Var	1.3%	Yes	2.25	0.0	No
604 Magnetic Tape Unit 60.0 KC	---	2.75	0.0	Yes	Var	1.9	Yes	2.25	0.0	No
606 Magnetic Tape Unit 83.4 KC	---	2.75	0.0	Yes	Var	2.6	Yes	1.75	0.0	No
607 Magnetic Tape Unit 120 KC	---	2.75	0.0	Yes	Var	3.75%	Yes	1.75	0.0	No
692 Magnetic Tape Unit 30 KC	---	?	0.0	Yes	Var	1.25%	Yes	?	0.0	No
694 Magnetic Tape Unit	---	?	0.0	Yes	Var	2.5%	Yes	?	0.0	No
696 Magnetic Tape Unit	---	?	0.0	Yes	Var	3.75%	Yes	?	0.0	No
3692 Program Controlled Input-Output Typewriter	67	0	---	---	Var	<0.001	Yes	0	---	---
3293 Incremental Plotter	3.3 or 5.0	100	0.0	No	No	<0.05	No	100	0.0	No

av Average time — see main report section on this device for details.
b For the word mode; if character mode is used, the core usage should be quadrupled.
I Interlace factor (can be 1, 2, 4, 8, 16, or 32).
LS Number of lines skipped between successive printed lines
Var. Data transmission time varies with record length.

INSTRUCTION LIST

§ 121.

.1 FORMAT

The instruction format in the 3200 is varied in that, generally, internal instructions require one word of storage, while input/output instructions consist of two words. Figure 1 presents the format of an internal instruction:

23 … 18	17	16 … 15	14 … 0
f	d	b	m, y, k, or unused

Figure 1. Format of Internal Instructions

- **f:** Operation Code — 6 bits: specifies the operation to be performed.
- **d:** Auxiliary Operation Code — 1 bit: its function varies depending upon the type of instruction being executed. It is used to denote such operations as indirect addressing, variations in shift instructions, and in some cases, combines with f to form a 7 bit code.
- **b:** Index Designator — 2 bits: specifies one of three index registers, the contents of which are used to modify the execution address portion of instructions.
- **m,y,k:** Execution Address — 15 bits: specifies the address of an operand (m), an operand (Y), or a shift count (k).

Usually input/output instructions consist of two words in the format shown in Figure 2.

23 … 18	17	16 … 0
f	d	n

23 … 21	20 … 18	17	16 … 0
x	t	e	m

Figure 2. Format of Input/Output Instructions.

- **f:** Operation Code — 6 bits: specifies the type of I/O to be performed.
- **d:** Interrupt Designator — 1 bit: specifies whether or not interrupt is to occur upon completion of the operation.
- **x:** Communication Channel Designator — 3 bits: specifies which of the eight possible channels is to be used.
- **t:** Format Definer — 3 bits: is subdivided into g, h, and i.
  - **g:** Choice of BCD conversion or no conversion
  - **h:** Choice of storing in a forward or backward direction
  - **i:** Choice of 12 to 24 bit assembly or no assembly
- **e:** Mode — 1 bit: specifies input (output) to (from) storage or the accumulator.
- **m:** Beginning Address — 17 bits: specifies the source (destination) of the first word of a data block.
- **n:** Terminal Address — 17 bits: specifies the source (destination) + 1 of the last word of a data block. If backward storage is being used, n is the source (destination) — 1 and is smaller than m.

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§ 121.

2. INSTRUCTION LIST

FUNCTION	MNEMONIC	CODE
STOP AND JUMPS		
Unconditional Halt	HLT	00 0 m
Selective Jump	SJX, X = 1-6	00 j m, j = 1-6
Return Jump	RTJ	00 7 m
Unconditional Jump	UJP	01 d b m
Index Jump, Incremental	IJI	02 o b m
Index Jump, Decremental	IJD	02 l b m
Compare A with Zero, Jump	AZJ	03 o b m
Compare A with Q, Jump	AQJ	03 l b m
Compare (within limits test)	CPR	52 d b m
SKIPS		
Skip if A = y	ASE	04 6 y
Skip if Q = y	QSE	04 7 y
Skip if Index = y	ISE	04 (1-3) y
Skip if A = y	ASG	05 6 y
Skip if Q = y	QSG	05 7 y
Skip if Index = y	ISG	05 (1-3) y
Index Skip, Incremental	ISI	10 0 b y
Index Skip, Decremental	ISD	10 l b y
Storage Shift	SSH	10 00 m
24-BIT FIXED POINT ARITHMETIC		
Load A	LDA	20 d b m
Load Complement A	LCA	24 d b m
Load Q	LDQ	21 d b m
Load Index	LDI	54 d b m
Store A	STA	40 d b m
Store Q	STQ	41 d b m
Store Index	STI	47 d b m
Store Word Address	SWA	44 d b m
Shift A	SHA	12 o b k
Shift Q	SHQ	12 l b k
Enter R*	ENR	14 d b y
Increase R*	INR	15 d b y
Inter-Register Transfer	IRT	53 d
Add to A	ADA	30 d b m
Replace Add	RAD	34 d b m
Subtract from A	SBA	31 d b m
Multiply A	MUA	50 d b m
Divide A	DVA	51 d b m
48-BIT FIXED POINT ARITHMETIC		
Load AQ	LDAQ	25 d b m
Load Complement AQ	LCAQ	26 d b m
Store AQ	STAQ	45 d b m
Shift AQ	SHAQ	13 o b k
Scale AQ	SCAQ	13 l b k
E (lower) to Q	ELQ	55 1
E (upper) to A	EUA	55 2
E to AQ	EAQ	55 3
Q to E (lower)	QEL	55 5
A to E (upper)	AEU	55 6
AQ to E	AQE	55 7
Add to AQ	ADAQ	32 d b m
Subtract from AQ	SBAQ	33 d b m
Multiply AQ	MUAQ	56 d b m
Divide AQ	DVAQ	57 d b m

FUNCTION	MNEMONIC	CODE
48-BIT FLOATING POINT		
Add to AQ	DFAD	60 d b m
Subtract from AQ	DFSB	61 d b m
Multiply AQ	DFMU	62 d b m
Divide AQ	DFDV	63 d b m
LOGICAL		
Logical Product, A/y	ANA	17 6 y
Logical Product, Q/y	ANQ	17 7 y
Logical Product, Index/y	ANI	17 (1-3) y
Exclusive Or, A/y	XOA	16 6 y
Exclusive Or, Index/y	XOI	16 (1-3) y
Load A Logical	LDL	27 d b m
Selectively Set A	SSA	35 d b m
Selectively Complement A	SCA	36 d b m
Logical Product, A/m	LPA	37 d b m
CHARACTER		
Character Address to A	ECHA	11 d y
Load A, Character	LACH	22 d m
Load Q, Character	LQCH	23 d m
Store A, Character	SACH	42 d m
Store Q, Character	SQCH	43 d m
Store Character Address from A	SCHA	46 d b m
DECIMAL ARITHMETIC		
Load E	LDE	64 d m
Store E	STE	65 d m
Add to E	ADE	66 d m
Subtract from E	SBE	67 d m
Shift E	SFE	70 d b k
Jump if E = o	EZJ	70 4 m
Jump if E<o	ELT	70 5 m
Jump, E overflow	EOJ	70 6 m
Set Character Count to y	SET	70 7 y
SEARCH, MOVE, I/O		
Masked Equality Search	MEQ	06 d b y
Masked Threshold Search	MTH	07 d b y
Character Equality Search	SRCE	71 (e = o)
Character Inequality Search	SRCN	71 (e = l)
Move Data	MOVE	72
Input Character Block	INPC	73 (e = o)
Input Character to A	INAC	73 (e = l)
Input Word Block	INPW	74 (e = o)
Input Word to A	INAW	74 (e = l)
Output Character Block	OUTC	75 (e = o)
Output Character from A	OTAC	75 (e = l)
Output Word Block	OUTW	76 (e = o)
Output Word from A	OTAW	76 (e = l)
I/O CONTROL AND INTERRUPT SENSE		
Connect Select		77 0
Function Select		77 1
Sense External		77 2
Sense Internal		77 3
Sense Interrupt		77 4
Pause		77 5
Copy Status		77 6
Stop		77 7

*R designates one of the arithmetic registers as determined by d and b.

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DATA CODE TABLE

§ 141.

Character	Internal BCD*	Tape and Printer BCD*	Card
0	00	12	0
1	01	01	1
2	02	02	2
3	03	03	3
4	04	04	4
5	05	05	5
6	06	06	6
7	07	07	7
8	10	10	8
9	11	11	9
A	21	61	12-1
B	22	62	12-2
C	23	63	12-3
D	24	64	12-4
E	25	65	12-5
F	26	66	12-6
G	27	67	12-7
H	30	70	12-8
I	31	71	12-9
J	41	41	11-1
K	42	42	11-2
L	43	43	11-3
M	44	44	11-4
N	45	45	11-5
O	46	46	11-6

Character	Internal BCD*	Tape and Printer BCD*	Card
P	47	47	11-7
Q	50	50	11-8
R	51	51	11-9
S	62	22	0-2
T	63	23	0-3
U	64	24	0-4
V	65	25	0-5
W	66	26	0-6
X	67	27	0-7
Y	70	30	0-8
Z	71	31	0-9
=	13	13	3-8
- (dash)	14	14	4-8
+	20	60	12
+0	32	72	12-0
.	33	73	12-3-8
)	34	74	12-4-8
- (minus)	40	40	11
-0	52	52	11-0
$	53	53	11-3-8
*	54	54	11-4-8
(space)	60	20	blank
/	61	21	0-1
,	73	33	0-3-8
(	74	34	0-4-8

* Octal representation of 6-bit BCD codes is shown.

PROBLEM ORIENTED FACILITIES

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers: . . . . none.

.12 Simulation by Other Computers: . . . . none.

.13 Data Sorting and Merging

Generalized SORT/MERGE program

Reference: . . . . SORT/MERGE General Information Manual.
Record size: . . . . . . 17 to 1,000 characters.
Block size: . . . . 17 to 1,000 characters.
Key size: . . . . up to 1,000 characters, in not more than 10 keys.
File size: . . . . limited during processing to one reel-full.
Number of tape units: . . . . 4 through 16.

The Generalized SORT/MERGE Program is an unusually flexible sorting program. From the user's point of view, perhaps the most important feature is that it permits the use of more than one collating sequence. Four standard sequences are available:

- Standard BCD (Basically A thru Z, 0 thru 9)
- Optional BCD (Basically 0-9, A thru Z)
- Absolute binary magnitude
- Signed value (one's complement form, i.e., -2, -1, -0, +0, 1, 2).

However, any arbitrary collating sequence can also be used. More than one collating sequence can be used in a single program; for example, the sort on key A can be handled in standard BCD, while key B is being sorted according to absolute binary magnitude. Each collating sequence can also be defined as either "Ascending" or "Descending."

SORT/MERGE contains several programming exits to modification routines where the user may:

- Edit acceptable records
- Reject records
- Check non-standard labels
- Modify non-standard labels
- Generate messages for the operator
- Terminate the sort process.

.13 Data Sorting and Merging (Contd.)

These previously-assembled routines written by the user are in relocatable binary form on the standard input unit and are indicated by control cards.

Input and output tapes may contain standard or non-standard header and trailer labels. Standard and non-standard output header labels may be specified on control cards. SORT/MERGE checks standard header and trailer labels. Non-standard header and trailer labels may be checked or changed by user routines at programming exits.

For recovery protection, an optional restart dump is written at the end of the last output tape after the internal sort and each intermediate merge pass. Record control messages are written to the operator at the end of the internal sort, the intermediate merge passes, and the final merge.

SORT/MERGE contains an internal sort phase and a merge phase. The method for the internal sort is the tournament replacement technique. Successive records are read from the unordered sort input file into core storage. The sort keys of the records are compared and the selected record is written on tape as part of a "string." Strings are ordered subsets of all the records in a file. A new record is read and the comparison cycle is repeated until all the records in the file have been ordered and written on tapes in sequenced strings for use as input to the merge phase. By employing a variable rather than a fixed area for the tournament, the internal sort phase makes maximum use of available core storage.

The intermediate merge phase performs successive merge operations on the strings to form a single file of sequenced records. It orders the records from two or more strings, according to the sort keys, to form a larger ordered string. Merging is repeated, creating longer strings, until all of the data is collected into one string per available tape. A final merge places all original data into one sequenced output file. Other presorted files may be included as input to the final merge. All available tapes are used to reduce the number of passes required.

One of four merging methods is specified by a control card parameter:

- Normal balanced merge with forward reading
- Normal balanced merge with backward reading
- Polyphase merge with forward reading
- Polyphase merge with backward reading.

§ 151.

.13 Data Sorting and Merging (Contd.)

In a normal balanced merge, half of the tapes are used as input to the merge and half as output during each merge pass. Tapes are rewound and the output tapes from one pass become input for the next. During each pass, the total number of strings decreases by half the total number of tapes. During a polyphase merge using T magnetic tape units, a continuous T-1 way merge is performed until the tape with the least number of strings is depleted. The merge continues merging additional strings from tapes not yet depleted with strings from the tape just created onto the newly depleted tape.

SORT/MERGE can utilize equipment configurations within the following range:

	Minimum	Maximum
Core storage:	8,192 words	32,768 words
Data channels:	2 channels	8 channels
Tape control unit:	1 read/write control	4 read/write controls
Tape units:	4 units	16 units.

.14 Report Writing: . . . . . none.

.15 Data Transcription: . . none as such; however, the use of READ and WRITE macros in the assembly language, which transfer control to the input-output routines for the specific devices which are presently connected, allow an almost equivalent facility.

.16 File Maintenance: . . . none.

.17 Other

Data Processing Package

This is a group of macro-instructions that facilitate BCD processing, together with a group of I/O routines that allow simplified programming of I/O operations. These I/O routines provide optional buffering, and automatic facilities such as multi-reel files, translation to appropriate codes, and use of logical I/O units.

PROCESS ORIENTED LANGUAGE: COBOL

§ 161.

.1 GENERAL

.11 Identity: . . . . COBOL for CDC 3200.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . not yet available.

.14 Description

Control Data originally announced a COMPACT COBOL compiler for the 3200 system, but has since decided to produce a compiler which will accept all of Required COBOL-61 except the following five language facilities:

(1) ALL "any literal."

(2) COPY functions in any of the divisions.

.14 Description (Contd.)

(3) Nested and Compound Conditionals.

(4) The EXAMINE function.

(5) UNTIL and VARYING options of the PERFORM verb.

Control Data's position is that the COPY and EXAMINE functions are not widely used, that the Nested and Compound Conditionals can always be replaced by a rephrased input, and that the "ALL any literal" is fairly trivial. This appears to be very reasonable, and certainly preferable to providing only the much-restricted COMPACT COBOL.

The compiler is due in early 1965. No details on the translator are available to date.

PROCESS ORIENTED LANGUAGE: 3200 FORTRAN

§ 162.

.1 GENERAL

.11 Identity: . . . . 3200 FORTRAN.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . General Information Manual, Pub. No. 552.

.14 Description

3200 FORTRAN is a FORTRAN IV-style language which is not an exact copy of some other language, but rather an independently designed language that offers a choice of performance-improving features. In this respect it appears that Control Data is continuing a policy established in its FORTRAN 63 compiler for the 1604 system; that of re-evaluating the FORTRAN language before implementation. This policy gives promise of continued improvements in FORTRAN, but complicates the compatibility problem, as explained below.

As an example of this improvement policy, consider the matter of type declarations. In FORTRAN IV a variable can be declared as being of type INTEGER, REAL*, DOUBLE PRECISION, COMPLEX, or BOOLEAN; in 3200 FORTRAN, the type can be INTEGER, REAL, CHARACTER, or "OTHER," where the programmer can supply the necessary data for one "OTHER" declaration in any program segment. As a result, there will be very few occasions when a programmer will not be able to get the FORTRAN IV facilities he needs; (he would have to need a combination of variable types, such as DOUBLE PRECISION and BOOLEAN, or COMPLEX and BOOLEAN, both within a single segment). This feature also provides a new standard facility (CHARACTER), plus the possibility of automatically incorporating other ones.

The 3200 system is basically a 24-bit word machine, but its floating point representation (simulated if not in the hardware) uses two words and has 36-bit precision. The integer range in 3200 FORTRAN is up to seven decimal digits (i.e., single word representation is used), which makes integer arithmetic a much more powerful capability than it is when the range is restricted to four decimal digits as in other versions of FORTRAN IV. Naturally, any computation that can be handled in the integer mode will proceed much faster than in the floating point mode.

The question of compatibility between 3200 FORTRAN and other versions of FORTRAN becomes complex because of Control Data's continued

* "REAL" is the FORTRAN IV term for "floating point."

.14 Description (Contd.)

FORTRAN redevelopment program. In general, a close desk check will be required before any system change can be made, in either direction. Tables I and II at the end of this section (which are based on Control Data documentation) point up the relationships of 3200 FORTRAN to FORTRAN II, FORTRAN IV, and FORTRAN-62 (for the purpose of moving into 3200 FORTRAN), and of 3200 FORTRAN to 3400 FORTRAN and 3600 FORTRAN (for the purpose of moving out of 3200 FORTRAN into these languages). (It should be noted that, from Control Data's point of view, these are the most anticipated and most desirable types of moves.)

3200 FORTRAN programs can be compiled on a Control Data 3200 system containing 8,192 core storage locations and at least five input-output devices. A FORTRAN II compiler will also be available for smaller 3200 systems (4,096 word locations and two input-output devices) and will be usable on larger systems if desired.

Technical information on 3200 FORTRAN indicates that extensive use is made of library routines for mathematical statements, sense statements, arithmetic fault checks, and data transmission sensing. (In other languages these appear as source program statements — the difference is a trivial one.) Multiple replacement statements (A_n = . . . = A_2 = A_1 = Expression, which causes all the variables A_1 through A_n to be set equal to the expression) and logical operations involving magnitude and equality relationships ("greater than," "AND" etc.) are available. The FORMAT instructions allow for single-precision floating point format, with or without exponent; a choice of integer, octal, or alphanumeric characters; line spacing; Hollerith heading and labelling; and "new record" facilities. Input-output operations can be buffered, and both labeled and blank COMMON storage are available. This is not surprising, as this now-standard feature of FORTRAN IV was popularized, if not originated, by Control Data in previous FORTRAN compilers.

The following lists represent a tabulated comparison of 3200 FORTRAN with IBM 7090/7094 FORTRAN IV, as described in Section 408:162.

Restrictions upon 3200 FORTRAN

(1) The following statements are not implemented:

ASSIGN i TO n
BLOCK DATA
COMPLEX a, b, . . .
DOUBLE PRECISION a, b . . .
GO TO n, (n_1, n_2, . . ., n_m)

§ 162.

.14 Description (Contd.)

*PRINT n, List
*PUNCH n, List
*READ n, List

(2) Because 3200 FORTRAN does not directly provide for complex and double precision arithmetic, the corresponding functions are not provided in the standard package. However, they may be available in the installation library. In addition, the following functions are not currently available.

AINT (A): . . . . . truncate.
INT (A): . . . . . . truncate.
AMOD (A, B): . . remainder A ÷ B.
MOD (A, B): . . . remainder A ÷ B.
AMAX0 (A, B, ...): . . maximum value.
AMAX1 (A, B, ...): . . maximum value.
MAX0 (A, B, ...): . . maximum value.
MAX1 (A, B, ...): . . maximum value.
AMIN0 (A, B, ...): . . minimum value.
AMIN1 (A, B, ...): . . minimum value.
MIN0 (A, B, ...): . . minimum value.
DIM (A, B): . . . diminish A by A or B, whichever is smaller.
IDIM (A, B): . . . diminish A by A or B, whichever is smaller.
ALOG10 (A): . . . real common logarithm.
TANH (A): . . . . real hyperbolic tangent.

(3) Hollerith constants cannot exceed four characters in size. Integer constants must be less than or equal to 2^{23}.

(4) FORMAT specifications of the R and A types can specify a maximum of 8 real or 4 integer characters; O-type FORMAT specifications may not exceed 16 real or 8 integer characters.

Extensions of 3200 FORTRAN

(1) Names may be up to 8 characters in length.

(2) Floating point constants can range from 10^{-308} to 10^{+308}; Boolean constants can be up to 8 octal digits (24 bits).

(3) BUFFER IN and BUFFER OUT initiate the buffered reading or writing of one block on magnetic tape from sequential core storage locations, beginning and ending with specified variables.

* READ and WRITE statements, addressed to logical input-output units, will have the appropriate coding inserted automatically by the monitor system.

.14 Description (Contd.)

Extensions of 3200 FORTRAN (Contd.)

(4) Library functions and subroutines EXFLTF(J) - EXFLT(J), EOFCKF(I) — EOFCK(I, J), IOCHKK(I) — IOCHK(I, J), UNITSTF(I) — UNITST(I, J) permit tests for exponent faults, for end-of-file conditions, for parity errors, and for the status of buffered input-output operations.

(5) ENCODE and DECODE statements control code or radix conversions and packing into or unpacking from sequential locations of a list of variables (usually those involved in a buffered input or output operation).

(6) The statements READ and WRITE may designate any logical input or output device.

(7) The COMMON statement can allocate one labeled common block (DATA) per program; this facilitates the transfer of information between subprograms.

(8) Conditional statements may be of the type IF (e) nl, n2; where e is a logical expression. A branch to statement nl is executed if e is true, or to n2 if e is false. FORTRAN IV has the expression IF (e) nl; no branch is taken if e is false.

(9) Multiple replacement statements (e.g., A = B = C = D) store the value of the expression on the right in each of the variables appearing on the left, with type conversion if necessary.

(10) Four type declarations can be used to specify the mode of the associated variables. The mode of arithmetic used to evaluate an expression is determined by the highest-order type of variable appearing in it. The order is:

TYPE OTHER (one "other" type per subprogram)
REAL
INTEGER
CHARACTER.

(11) The ENTRY statement designates an entry point other than the first executable statement in a subprogram. The PROGRAM statement is the first statement in the main program.

(12) Masking operations are available through use of 3200 FORTRAN library routines. They include AND, OR, NOT, and EOR (exclusive OR).

LANGUAGE COMPATIBILITY

The 3200 FORTRAN language contains most of the features of FORTRAN-62, FORTRAN-63, and 3600 FORTRAN for the Control Data 1604 System, as well as 3400 FORTRAN for the Control Data 3400 system.

Tables I and II show some of the program facilities that might require modification if a FORTRAN program designed for a different system were to be compiled by 3200 FORTRAN.

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TABLE I — Moving Into 3200 FORTRAN

From	Original Program Facility	3200 FORTRAN Modifications
FORTRAN II	DOUBLE and COMPLEX arithmetic	Not implemented.
	External routines	Identified by EXTERNAL statements; character F not required.
	Arithmetic checks	Available as library routines.
	Boolean statements	Masking arithmetic is available through library functions.
	EQUIVALENCE statements	Cannot reorder COMMON assignments.
	FORMAT statements and E-conversion	Repeat from last unquantified open parentheses; 6 positions for sign, exponent, and E in E-Conversion.
	Hollerith constants	Treated in integer mode.
	Integers	Treated mod $2^{47} - 1$.
FORTRAN IV	Logical constants	.TRUE. is represented by 1 and .FALSE. is represented by 0.
	Data statements	The form DATA i_1/value list/, i_2/value list/, . . . must be changed to DATA (i_1 = value list), (i_2 = value list).
FORTRAN 62	Boolean statements	Masking arithmetic is handled through library functions: NOT(A), AND(A, B), OR(A, B), EOR(A, B).
	FORMAT statements, E-conversion	6 positions for sign, exponent, and E.
	Arithmetic checks	Fault checks are available as library routines.
	Hollerith constants	Treated in integer mode.

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TABLE II — Moving Out of 3200 FORTRAN

To	3200 FORTRAN Facility	Required Modifications
3400 FORTRAN	Computed GO TO statement	The path determinant must be represented as an integer variable, not an expression.
	Type declarations	The CHARACTER type is not directly implemented.
	Library subroutines	Masking arithmetic, sense statements, arithmetic fault checks, and data transmission sensing are source language statements rather than library routines.
36000 FORTRAN	Multiple replacement statement	The expression may be arithmetic, logical or masking.
	Library subroutines	Masking arithmetic, sense statements, arithmetic fault checks, and data transmission sensing are source language statements rather than library routines.
	Logical and relational expressions	The expressions may be nested and the replacement identifier must be type LOGICAL.
	TYPE declarations	The CHARACTER type is not directly implemented.
	Equivalencing	Both INTEGER and REAL variables occupy one 48-bit word per element, and equivalencing within COMMON blocks is allowed as long as the origin of the block is not changed.
	Computed GO TO	The path determinant must be represented as an integer variable, not an expression.
FORTRAN IV	See preceding lists of restrictions and extensions of 3200 FORTRAN relative to IBM 7090/7094 FORTRAN IV.	

PROCESS ORIENTED LANGUAGE: BASIC FORTRAN II

§ 163.

.1 GENERAL

.11 Identity: . . . . Basic FORTRAN II for CDC 3200.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . not yet available.

.14 Description

Preliminary information on Basic FORTRAN II for the CDC 3200 shows that the FORTRAN II language has been modernized to remove some of the input-output restrictions, and to allow FORTRAN IV style TYPE declarations (which release the programmer from having to adhere to certain naming conventions for variables according to whether they are floating point or integer).

Otherwise, this is a restricted form of the FORTRAN II language. FORTRAN II for the IBM 7090 is described in detail in Section 408:161, and only the differences from IBM 7090 FORTRAN II will be considered here.

The major restriction is probably the inability to scale floating point variables on input or output. Other restrictions and extensions relative to IBM 7090 FORTRAN II are listed below.

No details are currently available regarding the Basic FORTRAN II translator.

.14 Description (Contd.)

Restrictions

- The following IBM 7090 FORTRAN II statements are not available:
  FREQUENCY
  IF DIVIDE CHECK
  IF QUOTIENT OVERFLOW
  READ DRUM
  SENSE LIGHT
  WRITE DRUM.
- The following IBM 7090 FORTRAN II facilities are not available:
  Double precision arithmetic
  Complex arithmetic
  Scaling of input or output variables.
- A maximum of four continuation cards per statement are permitted.

Extensions

- TYPE Declarations (REAL, INTEGER; REAL takes priority in mixed mode expressions).
- Line spacing, and heading and labeling facilities in FORMAT statements.
- Ability to utilize multiple card readers, card punches, printers, paper tape readers, and paper tape punches.
- Integers up to 7 decimal digits.
- Mixed mode expressions are allowed.

MACHINE ORIENTED LANGUAGE: 3200 COMPASS

§ 171.

.1 GENERAL

.11 Identity: . . . . 3200 COMPASS.

.12 Origin: . . . . Control Data Corp.

.13 Reference: . . . . General Information Manual, Pub. No. 550.

.14 Description

3200 COMPASS is the principal symbolic assembly language for the Control Data 3200 system. It provides for both user-defined and system macro instructions, and is capable of handling communications between different program segments, with library subroutines, and with the 3200 SCOPE operating system. It also has the ability to reserve storage areas common to several program segments which can be preset with data.

Programs written in the COMPASS language are grouped into segments which can be assembled independently. This arrangement simplifies debugging, provides more working area, and permits a coding job to be spread among several programmers. Facilities for specifying and handling literals are present, and compound addresses can legally appear in any address field except where one or more of the elements of a compound address is an external symbol.

The 3200 COMPASS assembly program converts programs written in 3200 COMPASS source language into a form suitable for execution under the 3200 SCOPE operating system. The source program can be contained on punched cards, or it can be in the form of BCD card images on magnetic or paper tape. The output from the assembler includes an assembly listing and a relocatable binary object program on punched cards or magnetic tape.

The minimum configuration for 3200 COMPASS assembly is 8,192 core storage locations, input unit, scratch magnetic tape unit, listing output unit, and object program output unit (which can be the same as the listing output unit). A subset of COMPASS will be available for systems with less than 8,192 storage locations.

The assembly listing contains the source program instructions and the corresponding octal machine instructions. Relative addresses are assigned to each subprogram since absolute addresses are not assigned until the program is loaded by the monitor loader. Error codes can also appear on the assembly listing. These include codes for illegal characters or expressions in address fields, duplicate symbols, illegal operation codes, relocation errors, and undefined symbols.

.15 Publication Date: . . . October, 1963 (Preliminary Description).

.2 LANGUAGE FORMAT

.21 Diagram: . . . . same as for 3600 COMPASS; see Page 247:171.100.

.22 Legend

Location: . . . . symbols identifying the address of an instruction or data item.

Operation code: . . . . instruction codes with modifiers or pseudo instructions. Instruction codes may include MACRO names as defined by a user.

Address: . . . . word or character address, operand, index register, character, channel or input-output or interrupt code.

.23 Corrections: . . . . . . incorrect lines crossed out; additions and alterations inserted in proper sequence; corrections can be made to the object program using Octal Correction Cards under 3200 SCOPE.

.24 Special Conventions

.241 Compound addresses: can appear in any address field; symbolic names, octal or decimal constants, literals, and special characters can be joined by the operators + and -, limited only by the space available on the card; integers referring to characters may not be suffixed by a C.

.242 Multi-addresses: . . . only in unusual circumstances (macro calls, I/O operations etc.).

.243 Literals as part of operand addresses: yes.

.244 Special coded addresses: . . . . . . * — inserts relocatable address of that instruction in the address field.
** — causes each bit in the operand to be set to one.

§ 171.

.3 LABELS

.31 General

.311	Maximum number of labels:	symbol table is limited by the core storage available. In the 8,192-word configuration, about 900 symbols can be stored for any one program. Three word locations are used per symbol. The actual number may vary depending on the variations in storage available to the assembler under differing input-output configurations.
.312	Common label formation rule:	yes.
.313	Reserved labels:	none.
.314	Other restrictions:	none.
.315	Designators:	none.
.316	Synonyms permitted:	yes; via EQUivalence pseudo-op.

.32 Universal Labels

.321	Labels for procedures	
	Existence:	mandatory if referenced by more than one subprogram. Note: ENTRY pseudo defines internal universal symbols. EXT pseudo defines external symbols.
	Formation rule	
	First character:	alphabetic.
	Other:	alphabetic, numeric, or period.
	Number of characters:	1 to 8; embedded blanks are ignored.
.322	Labels for library routines:	same as Procedures.
.323	Labels for constants:	same as Procedures.
.324	Labels for files:	not applicable.
.325	Labels for records:	not applicable.
.326	Labels for variables:	same as Procedures.
.327	Labels for other subprograms:	same as Procedures.

.33 Local Labels

.331	Region:	local to a subprogram.
.332	Labels for procedures	
	Existence:	mandatory if referenced within the subprogram.
	Formation rule	
	First character:	alphabetic.
	Others:	alphabetic or numeric.
	Number of characters:	1 to 8; embedded blanks are ignored.
.333	Labels for library routines:	by definition, labels for library routines are universal (see Paragraph .322).
.334	Labels for constants:	same as Procedures.
.335	Labels for files:	not applicable.
.336	Labels for records:	not applicable.
.337	Labels for variables:	same as Procedures.

.4 DATA

.41 Constants

.411	Maximum size constants:	56 alphameric characters. 14 decimal digits (two-word constant). 7 decimal digits (one-word constant). 8 octal digits.
.412	Maximum size literals:	up to 8 characters, 16 octal digits, or 14 decimal digits.
.413	Constants per line:	number of constants written per line is limited by the size of the constants.

.42 Working Areas

.421	Data layout	
	Implied by use:	no.
	Specified in program:	BSS and COMMON statements.
.422	Data type:	implied by use.
.423	Redefinition:	possible through the use of ORGR statement.

.43 Input-Output Areas: specified in program.

.5 PROCEDURES

.51 Direct Operation Codes

.511	Mnemonic	
	Existence:	mandatory.
	Number:	128 plus 11 modifiers.
	Example:	SHA = shift A.
.512	Absolute:	octal machine codes can be used.

.52 Macro-Codes

.521	Number available	
	Input-output:	11.
	Arithmetic (BCD):	2.
	Math functions:	none.
	Error control:	none.
	Restarts:	none.
	Editing:	1.
	Compare:	1.
	Move:	1.
.522	Example:	MOVE (A-ADDRESS, X-LENGTH, B-ADDRESS, Y-LENGTH): Move field which starts at address A and is X characters in length to the field which starts at address B and is Y characters in length.
.523	New macros:	MACRO pseudo permits a section of coding written by programmer to be treated as a macro when referenced.

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.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control
- Allocation counter: none (absolute addresses are assigned by SCOPE).
- Label adjustment: . pseudo operation.
- Annotation: . . . . . . pseudo operation.

.542 Allocation counter
- Set to absolute: . . . not applicable.
- Set to label: . . . . . ORGR pseudo.
- Step forward: . . . . BSS pseudo.
- Step backward: . . . ORGR pseudo.
- Reserve area: . . . . BSS, COMMON, DATA pseudos.

.543 Label adjustment
- Set labels equal: . . EQU pseudo.
- Set absolute value: . EQU pseudo.
- Clear label table: . . no.

.544 Annotation
- Comment phrase: . . REM pseudo (* in column 1 defines remainder of card to be comments).
- Title phrase: . . . . . IDENT pseudo.

.545 Other
- Labels referenced by segments: . . . . ENTRY, EXT pseudo.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic

.611 Facilities: . . . . BCD fixed-point multiplication and division (multi-precision).

.612 Method of call: . . . . macros.

.62 Special Functions: . . none.

.63 Overlay Control: . . . handled by SCOPE operating system.

.64 Data Editing

.641 Radix conversion: . . decimal-to-binary for initial constants.
- Code translation: . . . none.

.642 Format control
- Zero suppression: . yes.
- Size control: . . . . . yes.
- Sign control: . . . . . yes.
- Special characters: yes, via COBOL picture facility.

.643 Method of call: . . . . macro instruction.

.65 Input-Output Control

.651 File labels: . . . .
.652 Reel labels: . . . . . .
.653 Blocking: . . . .
.654 Error control: . . . . .
(.651–.654: will be handled by 3200 Peripheral Equipment Package.)

.655 Method of call: . . . . macro instruction.

.67 Diagnostics: . . . . . . none can be written into the program.

.7 LIBRARY FACILITIES: . . . . . none; library routines and macros are inserted at object program time by 3200 SCOPE.

.8 MACRO AND PSEUDO TABLES

.81 Macros

Code	Description
TRANSMIT:	moves any string of up to 4,095 characters from one place in storage to another.
COMPARE:	compares any string of up to 4,095 characters to any other string and indicates the result as lower, equal, or greater.
EDIT:	moves a numeric field to a receiving field with report editing.
MULTIPLY:	multiplies one numeric BCD field by another and stores the result in a third field.
DIVIDE:	divides one BCD numeric field by another and stores the result in a third field.

Input/Output Control System Macros

READ:	read n words.
WRITE:	write n words.
READB:	read n words backward.
BKSP:	backspace one record.
SEFF:	space forward one file.
SEFB:	space backward one file.
WEOF:	write end of file.
ERASE:	erase 6 inches of tape.
REWIND:	rewind to load point.
UNLOAD:	rewind and unload.
STATUS:	return unit status to A and Q register.

.82 Pseudos

Code	Description
IDENT:	names the subprogram.
END:	marks the end of every subprogram.
FINIS:	terminates an assembly program.
EQU:	assigns the result of an expression to a symbol.
EQU,C:	identifies the label as a character address whose value appears in the address field of the coding line.
ENTRY:	defines location symbols which are referenced in other subprograms.
EXT:	defines external symbols (symbols used by a subprogram which are defined in another subprogram).
SPACE:	controls line spacing on an assembly listing.

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.82 Pseudos (Contd.)

Code	Description
EJECT:	causes printer to skip to the top of the next page of the assembly listing.
REM:	inserts program comments in listing.
NOLIST:	causes assembler to discontinue listing.
LIST:	causes assembler to resume listing the program.
MACRO:	defines the start of a sequence of instructions to be inserted in the source program whenever the location symbol of MACRO appears in an operation field.
ENDM:	defines the end of a macro sequence.
NAME:	used to reference macros.
BSS:	reserves a storage area.
BSS,C:	reserves a storage area counted by character locations.
COMMON:	reserves a storage area within a common region in storage.
DATA:	reserves common areas which may be preset with data.

.82 Pseudos (Contd.)

Code	Description
PRG:	marks the end of a sequence of instructions to be loaded into a DATA area.
OCT:	inserts octal constants into consecutive machine words.
DECD:	converts decimal constants into equivalent 48-bit binary values and stores them in consecutive groups of 2 words.
DEC:	inserts 24-bit decimal integer constants in consecutive words.
BCD:	inserts binary-coded decimal characters into consecutive words.
BCD, C:	places specified BCD characters in consecutive locations.
VFD:	assigns data in continuous strings of bits rather than in word units.
IFZ: IFN: IFT: IFF:	control of assembly subject to parameter values.
ORGR:	sets relocatable location counter from value of address field.
LIBM:	names system macros to be called from the library by this program.

MACHINE ORIENTED LANGUAGE: BASIC ASSEMBLER

§ 172.

.1 GENERAL

.11 Identity: . . . . BASIC Assembler.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . not available to date.

.14 Description

The BASIC Assembler is designed for use with the small-scale (4,096-word storage) 3212 Control Computer and as few as two input-output devices. The 3212 system, which is the lowest in the 3200 price range, is primarily aimed at process control but can be used wherever a small configuration is desirable. The BASIC Assembler is a straightforward symbolic assembly system that provides no facilities for the use of macro instructions or literals.

The BASIC Assembler program converts programs written in BASIC Assembler source language into a form suitable for loading by the Basic Loader or the SCOPE Operating System. Source program input can come from any input device capable of reading cards or card images. The output can similarly be in any device capable of representing an 80-column binary card image.

The minimum configuration for the BASIC Assembler is 4,096 locations of storage, input unit, listing output unit, and object program output unit. The list unit and the object program output unit can both be represented by the same output device.

The assembly listing contains the source program instructions and the corresponding octal machine instructions. Relative addresses are assigned to each subprogram since absolute addresses are not assigned until the program is loaded. Error codes can also appear on the assembly listing. These include codes for illegal characters or expressions in address fields, duplicate symbols, illegal operation codes, and undefined symbols.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . same as for 3600 COMPASS; see Page 247:171.100.

.22 Legend

Location: . . . . symbol(s) identifying the address of an instruction or data item.
Operation code: . . . . . instruction codes with modifiers or pseudo instructions.

.22 Legend (Contd.)

Address: . . . . word or character address, operand, index register, character, channel or input-output or interrupt code.
Comments: . . . . comments to be included on the assembly listing.
Sequence Number: . . . sequence number or identification.

.23 Corrections: . . . . incorrect lines crossed out; additions and alterations inserted in proper sequence.

.24 Special Conventions

.241 Compound addresses: . . can appear in any address field; tags, symbolic names, octal or decimal constants, and special characters may be joined by the operators + and -.
.242 Multi-addresses: . . . . none (some hardware operations require two addresses, e.g. INPW).
.244 Special coded addresses: . . . . literals are not available.
* - inserts address of that instruction in the address field.
** - causes each bit in the operand to be set to one.

.3 LABELS

.31 General

.311 Maximum number of labels
Procedures: . . . . . . the symbol table is limited by the storage available. In the 4,096-word configuration, about 900 symbols can be stored for any one program. One or two locations are used per symbol. The actual total number can vary depending upon the variations in storage available to the assembler under differing input-output configurations.
.312 Common label formation rule: . . . . yes.
.313 Reserved labels: . . . . none.
.314 Other restrictions: . . . none.
.315 Designators: . . . . none.
.316 Synonyms permitted: . . yes; via EQUivalence pseudo-op.

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.33 Local Labels

.331 Region: . . . . local to a subprogram.
.332 Labels for procedures
Existence:. . . . . mandatory if referenced within the subprogram.
Formation rule
First character: . . alphabetic.
Others:. . . . . alphabetic or numeric.
Number of characters: . . . . 1 to 8; embedded blanks are ignored.
.333 Labels for library routines:. . . . . not applicable.
.334 Labels for constants: . same as Procedures.
.335 Labels for files: . . . . not applicable.
.336 Labels for records: . . not applicable.
.337 Labels for variables: . same as Procedures.

.4 DATA

.41 Constants

.411 Maximum size constants:. . . . . 14 decimal, 8 octal, or 56 alphameric characters.
.412 Maximum size literals: . . . . no literals permitted.
.413 Number of constants: . number of constants written per line is limited by the size of the constants.

.42 Working Areas

.421 Data layout
Implied by use: . . . . no.
Specified in program: BSS statements.
.422 Data type:. . . . . implied by use.
.423 Redefinition: . . . . possible through the use of ORGR statement.

.43 Input-Output Areas: . . specified in program.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
Existence: . . . . mandatory.
Number:. . . . . 128 plus 11 modifiers.
Example: . . . . SHA = shift A.
.512 Absolute: . . . . octal machine codes may be used.

.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control
Allocation counter: . . none (absolute addresses are assigned by BASIC Loader).
Label adjustment: . . pseudo operation.
Annotation: . . . . pseudo operation.

.542 Allocation counter
Set to absolute: . . . . ORGR pseudo.
Set to label: . . . . . . ORGR pseudo affects the relocatable location counter; can be stepped forward or reverse and can specify either a constant or label.
Step forward: . . . . . BSS pseudo.
Step backward:. . . . . ORGR pseudo.
Reserve area: . . . . . BSS, BSSC pseudos.
.543 Label adjustment
Set labels equal: . . . EQU pseudo.
Set absolute value: . . none.
Clear label table:. . . no.
.544 Annotation
Comment phrase: . . . REM pseudo; Comments can also follow the blank column following the address field or an * in column 1.
Title phrase:. . . . . . IDENT pseudo.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic:. . . double-length integer arithmetic and floating point arithmetic can be used by the system.

.62 Special Functions: . . . none.

.63 Overlay Control: . . . . none.

.64 Data Editing

.641 Radix conversion:. . . . constants can be converted from decimal to binary, controlled by pseudo-operations.
.642 Code translation: . . . . none.
Format control: . . . . . none.

.65 Input-Output Control: . . none.

.66 Sorting: . . . . none.

.67 Diagnostics: . . . . none.

.7 LIBRARY FACILITIES: . . . . . . none.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . none.

.82 Pseudos

Code	Description
IDENT:	names the subprogram.
EQU:	assigns the result of an expression to a symbol.
EQU, C:	identifies the label as a character address whose value appears in the address field of the coding line.

§ 172.

.82 Pseudos (Contd.)

Code	Description
ORGR:	set relocatable location counter from value of address field.
OCT:	inserts octal constants into consecutive machine words.
DECD:	converts decimal constants into equivalent 48-bit binary values and stores them in consecutive groups of 2 words.
DEC:	inserts 24-bit decimal integer constants into consecutive words.
BCD:	inserts binary-coded decimal characters into consecutive words.

.82 Pseudos (Contd.)

Code	Description
BCD, C:	places specified BCD characters in consecutive character locations.
END:	specifies end of source program.
SPACE:	controls line spacing on an assembly listing.
EJECT:	causes printer to skip to the top of the next page of the assembly listing.
REM:	inserts program comments in listing.
NOLIST:	causes assembler to discontinue listing.
LIST:	causes assembler to resume listing the program.
BSS:	reserves a storage area.
BSS, C:	reserves a storage area counted by character locations.

OPERATING ENVIRONMENT: 3200 SCOPE

§ 191.

.1 GENERAL

.11 Identity: . . . . 3200 SCOPE.

.12 Description

3200 SCOPE is an operating system that allows a group of programs to be run sequentially — one at a time — on a Control Data 3200 computer.

During the running of a program, the operating system occupies the lower portion of core storage, the actual amount of storage utilized depending on the routines called in. Normally SCOPE's demands on central processor time will be negligible.

3200 SCOPE requires a 3-tape system with at least 8,192 core storage locations, and is the only operating system currently available for the Control Data 3200. The three basic languages (3200 FORTRAN, 3200 COBOL, and 3200 COMPASS) all use SCOPE during both the testing and production stages.

.12 Description (Contd.)

Like all operating systems, 3200 SCOPE provides a number of services to the various people involved. Some of these services naturally restrict the freedom of those involved by predetermining methods of operation which may or may not be the best ones possible under the existing circumstances. Other services involve giving up areas of storage, the use of specific peripherals, etc., and to this extent it can be said that they may have a "cost" involved.

In the following tables the facilities provided by 3200 SCOPE are listed as looked at from various points of view — those of the FORTRAN or COBOL programmer, the assembly language programmer, the user (i. e., the person who uses a "canned" program he may not have written), the computer room operator, and the data processing manager. All these individuals have different points of view, but all have a vital interest in maximizing the overall effectiveness of the computer system.

For the COBOL & FORTRAN PROGRAMMER	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
During Writing:	Dump facility in FORTRAN language. Snapshot and Trace facilities in assembly language (191.5).	Debug facilities in source language (:191.5).	Storage space is needed for these facilities.
During Testing:	Standard Recovery Dump option.		

For the ASSEMBLY LANGUAGE PROGRAMMER	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
During Writing:	Input-output routines and radix conversions (:191.2). Segmentation control system (:191.3)		Standard routines must be used.
During Testing:	Snapshot and Trace facilities (:191.5). Automatic dumps on abnormal operation (:191.4).	Restart Procedure (:191.45)	

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For the USER	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
During Normal Running:	Allocation of peripherals (:191.3)	Automatic servo swap facilities or print-outs (:191.32).	Standard I/O routines and radix conversion routines must be used.
		Time-shared operation (:191.4).	Restricted simultaneity for some peripherals
	Overlay facilities (:191.3).	Automatic segmentation (:191.3).	Segments must be predefined.
During & After Abnornal Running:	Automatic dump procedure (4 types) (:191.45).	Setting up of restart points.	
		Automatic restart facilities.	
		Standard interrupt processing routines (SCOPE simply directs the interrupt to a programmer-provided routine) (:191.4).	

For the COMPUTER ROOM OPERATOR	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
	Standard procedures for input/output unit allocation.	Type-outs for loading and unloading tape.	
	Run-to-run supervision.	Re-run ability (:191.4).	
	Amendment of running order (:191.6).		

For the DATA PROCESSING MANAGER	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
	Accounting records (:191.7).	Time sharing (:191.4).	

.14 Originator: . . . . Control Data Corp.

.15 Maintainer: . . . . Control Data Corp.

.16 First Use: . . . . 1964.

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . the SCOPE library tapes (which can be created as desired) can contain any collection of translators, subroutines and other data or programs. These may be incorporated at load time or during a run.

.212 Independent programs: loaded from card reader or tape unit with a control card.

.213 Data: . . . . any available type of input device, as specified in the program. (The data for a program is frequently loaded immediately behind the program itself.)

.214 Master routines: . . . . the SCOPE routines are held on all library tapes, together with bootstrap routines to bring them into memory.

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.22 Library Subroutines: . . can be called at load time or during a run from a library tape.

.23 Loading Sequence: . . . control card; subroutines for this run in any order (these are stored on a magnetic tape unit if necessary); data for this run if desired; further runs; ending with an End of Job control card.
Normally jobs are loaded and executed sequentially as physically placed on the input unit; however, the operator has emergency facilities to override this sequence.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . object programs, written as subprograms, can be divided into overlays defined by the programmer, and moved as needed into memory.

.312 Occupation of working storage: . . . . all addresses are relocated during loading. Once loaded, no further change is made.

.32 Input-Output Units

.321 Initial assignment: . . . performed by SCOPE using equipment availability table and logical unit definition.

.322 Alternation: . . . . automatic, by SCOPE.

.323 Reassignment: . . . . . . manual alteration of equipment availability table, followed by SCOPE operation.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: a table of waiting I/O operations is held, and when a channel becomes available, the operation that has been waiting longest is initiated.

.42 Multi-Programming: . . no provision.

.43 Multi-Sequencing: . . . . no provision.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Allocation impossible:	check by loader	flagged during loading.
In-out error — single:	check by input/ output control	?
In-out error — persistent:	check by input/ output control	?
Invalid instructions:	check	transfer to specific programmer coding.
Underflow:	check	transfer to specific programmer coding.
Invalid operation:	check	transfer to specific programmer coding.
Improper format:	check by loader	?
Invalid address:	check	transfer to specific coding.
Reference to forbidden area:	check	transfer to specific programmer coding.

.45 Restarts

.451 Establishing restart points: . . . . recovery dumps are written when a job is abandoned. No facility is available to automatically set up restart points ahead of time.

.452 Restart process: . . . . own coding.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . TRACE is a SCOPE control statement which permits a program area to be recorded on the output device each time it is executed, or when it is executed the Nth time. A dump of a memory area can also be provided.

.512 Snapshots: . . . . SNAP is a SCOPE control statement which operates like TRACE but only applies to a single core location.

.52 Post Mortem: . . . . a recovery dump can be written.

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.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . own coding.

.612 Action required by operator: . . . . print-out on Accounting Medium.

.613 Reporting progress of run: . . . . print-out on Accounting Medium (normally console typewriter).

.62 Operator's Decisions: . console typewriter.

.63 Operator's Signals

.631 Inquiry: . . . . manual interrupt button on console.

.632 Change of normal progress: . . . . SCOPE statements via console typewriter.

.7 LOGGING

.71 Operator Signals: . . . . console typewriter.

.72 Operator Decisions: . . console typewriter.

.73 Run Progress: . . . . . . console typewriter.

.74 Errors:. . . . . ?

.75 Running Times: . . . . . console typewriter.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . 1 processor module.
1 3201 console with typewriter.
1 3209 storage module (8,192 words).
1 3602 communication module.
2 3206 bidirectional data channels.
1 magnetic tape control.
3 magnetic tape units.

.812 Usable extra facilities: . . . . additional storage, tapes, and I/O equipment.

.813 Reserved equipment: . . the System Units (see below) are not available to the programmer except for the specified purposes. However, it is not necessary to use or assign all system Units, and more than one System Unit function can be allocated to a single physical unit.
System Units include the following:
Standard Input,
Standard Output,
Standard Punch,
SCOPE Libraries,
System Scratch Record.

.82 System Overhead

.821 Loading time: . . . . . . under 1 minute.

.822 Reloading frequency: . . only if the SCOPE Resident routine has been overwritten. Normally this is not done.

.83 Program Space Available: . . . . storage requirements for the resident 3200 SCOPE routines are not available to date.

.84 Program Loading Time: . . . . under 1 minute.

.85 Program Performance: essentially unaffected during normal production runs, since SCOPE merely directs run-to-run changeovers.

SYSTEM PERFORMANCE

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GENERALIZED FILE PROCESSING (245:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master file records is shown by solid lines. For Configuration VIIB, where all four input-output files are on magnetic tape, total times for cases using both unblocked and blocked records in the detail and report files are shown by means of solid and dashed lines, respectively. Central processor time is essentially the same for all configurations, and becomes the controlling factor only in Configuration VIIB under the following conditions: blocked records in the detail and report files, a high activity factor, and either a trebled computational load (Standard File Problem D) or a short master-file record length (Standard File Problem B).

Worksheet Data Table 1 (page 245:201.011) shows that the printer is the controlling factor on total time required over most of the detail activity range for the integrated Configuration VI. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a small fraction of the total processing time. In most of the cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, the processing run with all files on magnetic tape, and a tape-to-card transcription of the report file. The curves for paired Configuration VIIB show the time required for the all-tape main processing run in this case and point out that the computer is tape bound. The card-to-tape and tape-to-printer transactions will run at card reader and printer-limited speeds, and their demands on the processor will be small.

The master file record format is a mixture of alphameric BCD and pure binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. (Even so, most of the central processor time is devoted to editing and radix conversion operations, using programmed, nonstandard subroutines.) An optimized degree of packing led to a record length of 20 words (the equivalent of 80 6-bit characters).

SORTING (245:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A according to the method explained in the User's Guide, Paragraph 4:200.213, using a three-way merge.

MATRIX INVERSION (245:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplications ($c = c + a_i b_j$) in 36-bit precision floating point (see Paragraph 245:051.422).

GENERALIZED MATHEMATICAL PROCESSING (245:201.4)

This problem measures over-all system performance on a simple mathematical application that involves widely varying ratios of input-to-computation-to-output volume, as described in Section 4:200.4 of the Users' Guide. As in the File Processing problem, the total elapsed time is shown by the solid lines in Graph 245:201.400.

All computations are performed in single precision floating point. In Configuration VI, input is via the on-line card reader and output is via the on-line printer. If card-to-tape and tape-to-printer transcriptions are carried out in separate runs, the time required for the all-tape main processing run can be read from the curves for paired Configuration VIIB.

GENERALIZED STATISTICAL PROCESSING (245:201.5)

This problem measures overall system performance on a common statistical application: the development of cross-tabulation tables, as in the analysis of the results of a survey. The problem is defined in Section 4:200.5 of the Users' Guide, and the performance of the Control Data 3200 is shown in Graph 245:201.500.

WORKSHEET DATA TABLE 1

	Item		VI C.P.	VI I/O	VII B (Unblocked Files 3 & 4) C.P.	VII B (Unblocked Files 3 & 4) I/O	VII B (Blocked Files 3 & 4) C.P.	VII B (Blocked Files 3 & 4) I/O	Reference
1 Standard File Problem A Input-Output Times	Char/block	(File 1)	960		960		960		4:200.112
	Records/block	K (File 1)	12		12		12		
	msec/block	File 1 = File 2	34		26		26		
		File 3	50		11.5		26*		
		File 4	160		12.0		38*		
	msec/switch	File 1 = File 2							
		File 3							
		File 4							
	msec penalty	File 1 = File 2	0.24		0.24		0.24		
		File 3	0.03		0.03		0.03		
		File 4	0.04		0.04		0.04		
2 Central Processor Times	msec/block	a_1	1.00		1.00		1.00		4:200.1132
	msec/record	a_2	0.26		0.26		0.26		
	msec/detail	b_6	1.46		1.46		1.46		
	msec/work	b5 + b9	0.19		0.19		0.19		
	msec/report	b7 + b8	1.78		1.78		1.78		
3 Standard File Problem A F = 1.0	msec/block for C.P. and dominant column.		C.P.	I/O	C.P.	I/O	C.P.	I/O	4:200.114
		a_1	1.00		1.00		1.00		
		a_2K	3.12		3.12		3.12		
		a_3K	41.50		41.50		41.50		
		File 1 Master In	0.24		0.24	26	0.24	26	
		File 2 Master Out	0.24		0.24		0.24		
		File 3 Details	0.24		0.24		0.24		
		File 4 Reports	0.36	1,920	0.36	144	0.36	38	
		Total	46.70	1,920	46.70	170	46.70	64	
4 Standard File Problem A Space	Unit of measure	(24-bit word)							4:200.1151
		Std. routines	600		600		600		
		Fixed	2,000		2,000		2,000		
		3 (Blocks 1 to 23)	600		600		600		
		6 (Blocks 24 to 48)	1,000		1,000		1,000		
		Files	2,000		2,000		2,000		
		Working	600		600		600		
		Total	6,800		6,800		6,800		

* 12 records per block.

WORKSHEET DATA TABLE 2

	Item			Configuration VI	Configuration VIIB	Reference
5 Standard Mathematical Problem A	Fixed/Floating point			Floating	Floating	4:200.413
	Unit name		input	Card Reader	604 Tape	
			output	Line Printer	604 Tape	
	Size of record		input	1 card	80 char	
			output	1 line	120 char	
	msec/block		input T_1	50	11.3	
			output T_2	120	12.0	
	msec penalty		input T_3	0.02	0.02	
			output T_4	0.03	0.03	
	msec/record		T_5	5.0	5.0	
	msec/5 loops		T_6	2.6	2.6	
	msec/report		T_7	3.0	3.0	
7 Standard Statistical Problem A	Unit name			603 Tape	604 Tape	4:200.512
	Size of block			960 char	960 char	
	Records/block		B	15	15	
	msec/block		T_1	34.0	26.0	
	msec penalty		T_3	0.24	0.24	
	C.P.	msec/block	T_5	0.01	0.01	
		msec/record	T_6	0.01	0.01	
		msec/table	T_7	0.04	0.04	

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.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

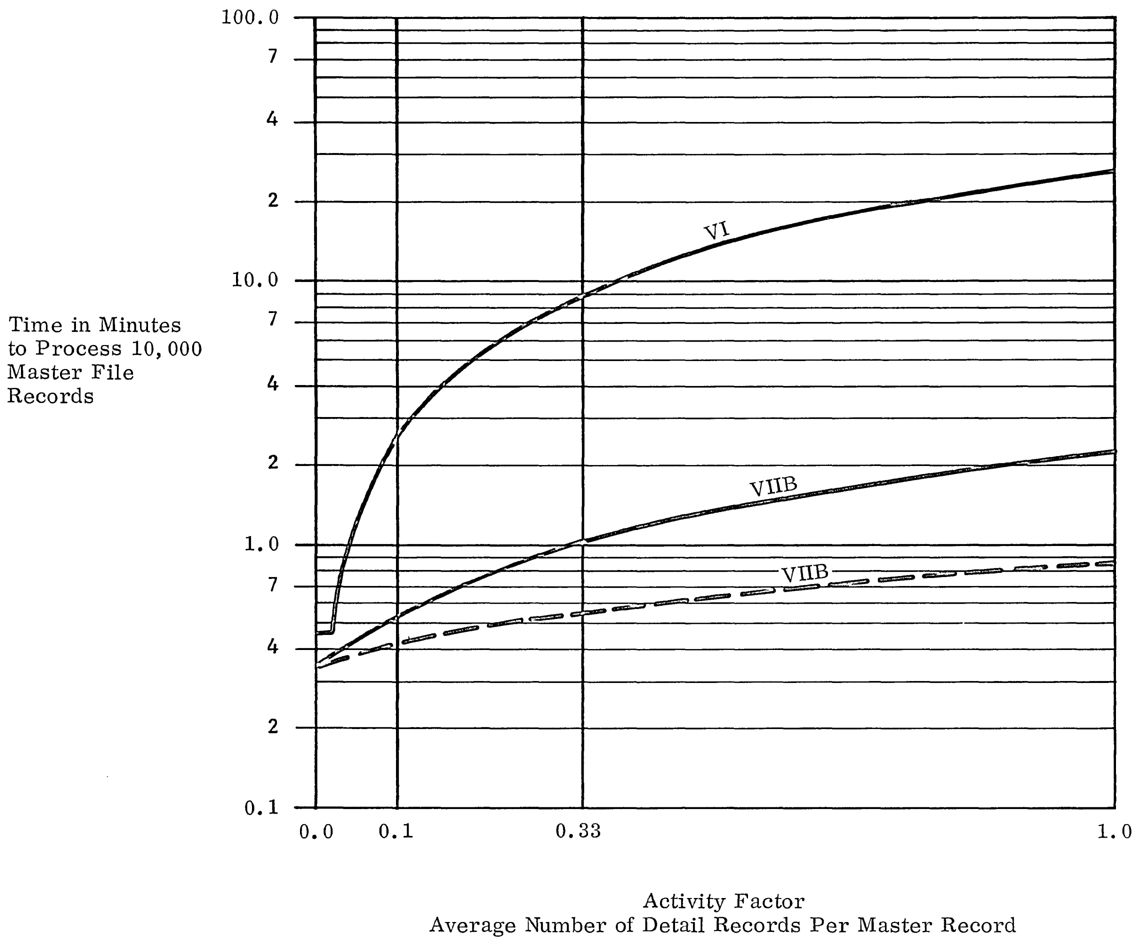
.111 Record sizes
Master file: . . . . . 108 characters (packed into 20 CDC 3200 words).
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.112 Computation: . . . . . standard.

.113 Timing basis: . . . . using estimating procedure outlines in Users' Guide, 4:200.113

.114 Graph: . . . . see graph below.

.115 Storage space required
Configuration VI: . . 6,800 words.
Configuration VII B (Unblocked Files 3 & 4): . . . . . . 6,800 words.
Configuration VII B (Blocked Files 3 & 4): . . . . . . 6,800 words.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 245:031.

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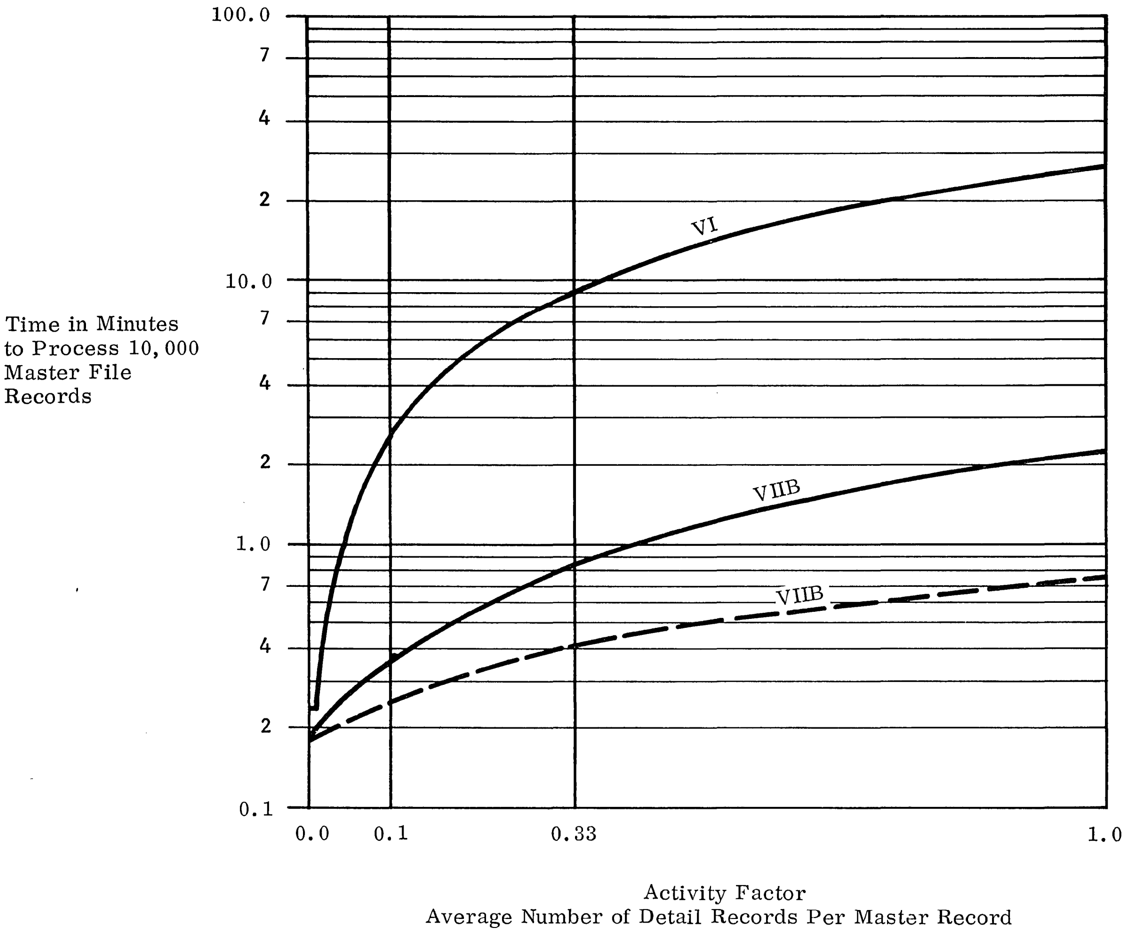
.12 Standard File Problem B

.121 Record sizes

Master file: . . . . . 54 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing Basis: . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . see graph below.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 245:031.

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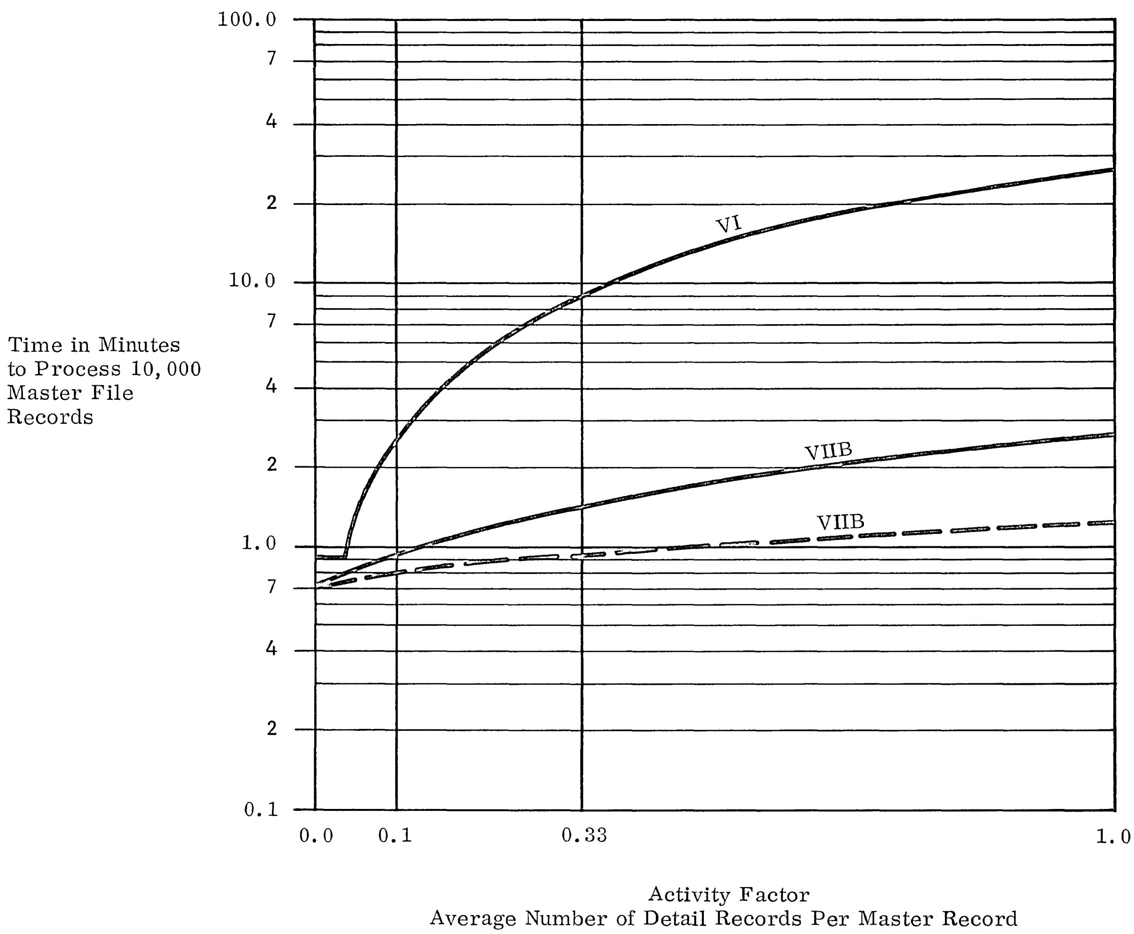
.13 Standard File Problem C

.131 Record sizes
Master file: . . . . . 216 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.132 Computation: . . . . . standard

.133 Timing Basis: . . . . using estimating procedure outlined in Users' Guide, 4:200.13

.134 Graph:



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 245:031.

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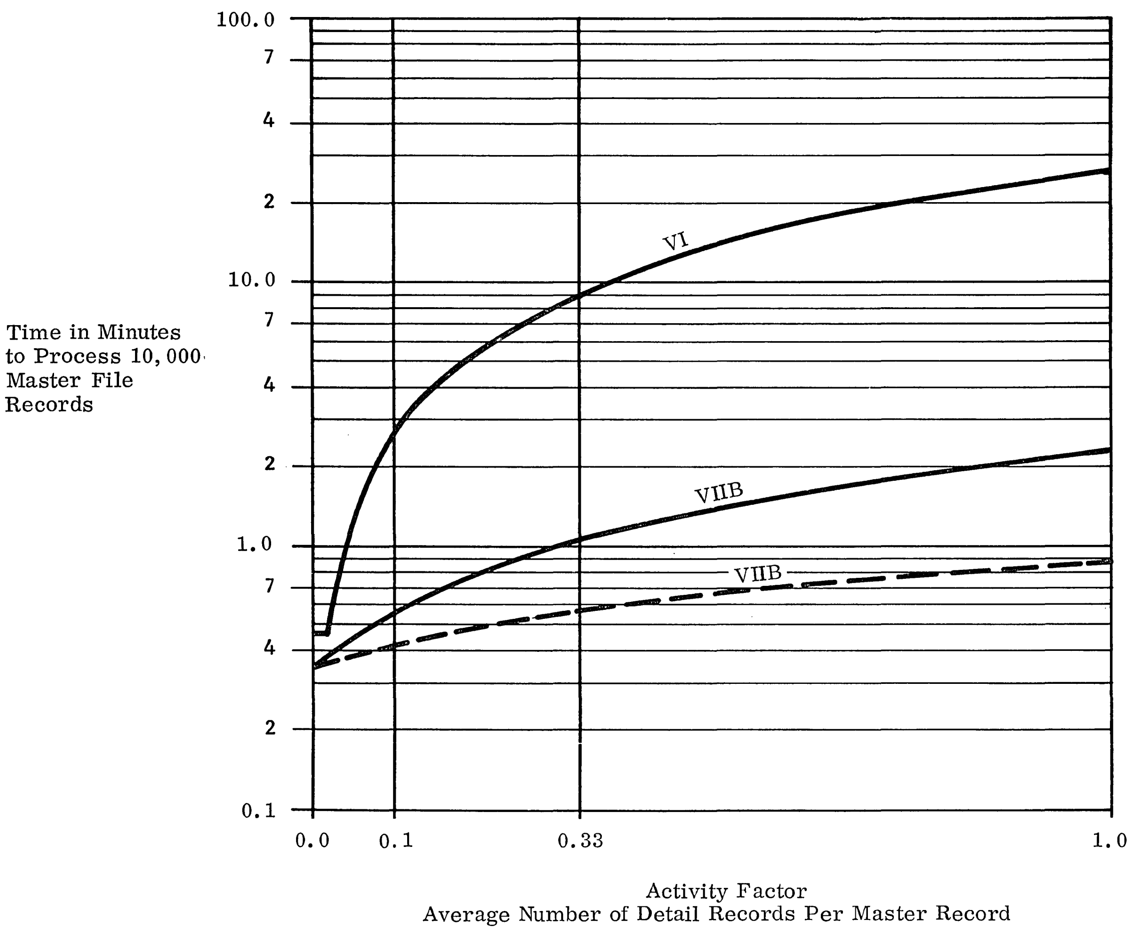
.14 Standard File Problem D

.141 Record sizes
Master file: . . . . . 108 characters.
Detail file: . . . . . 1 card.
Report file: . . . . . 1 line.

.142 Computation: . . . . . trebled.
.143 Timing Basis: . . . . using estimating procedure outlined in Users' Guide, 4:200.14.
.144 Graph: . . . . see graph below.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 245:031.

§ 201.

.2 SORTING

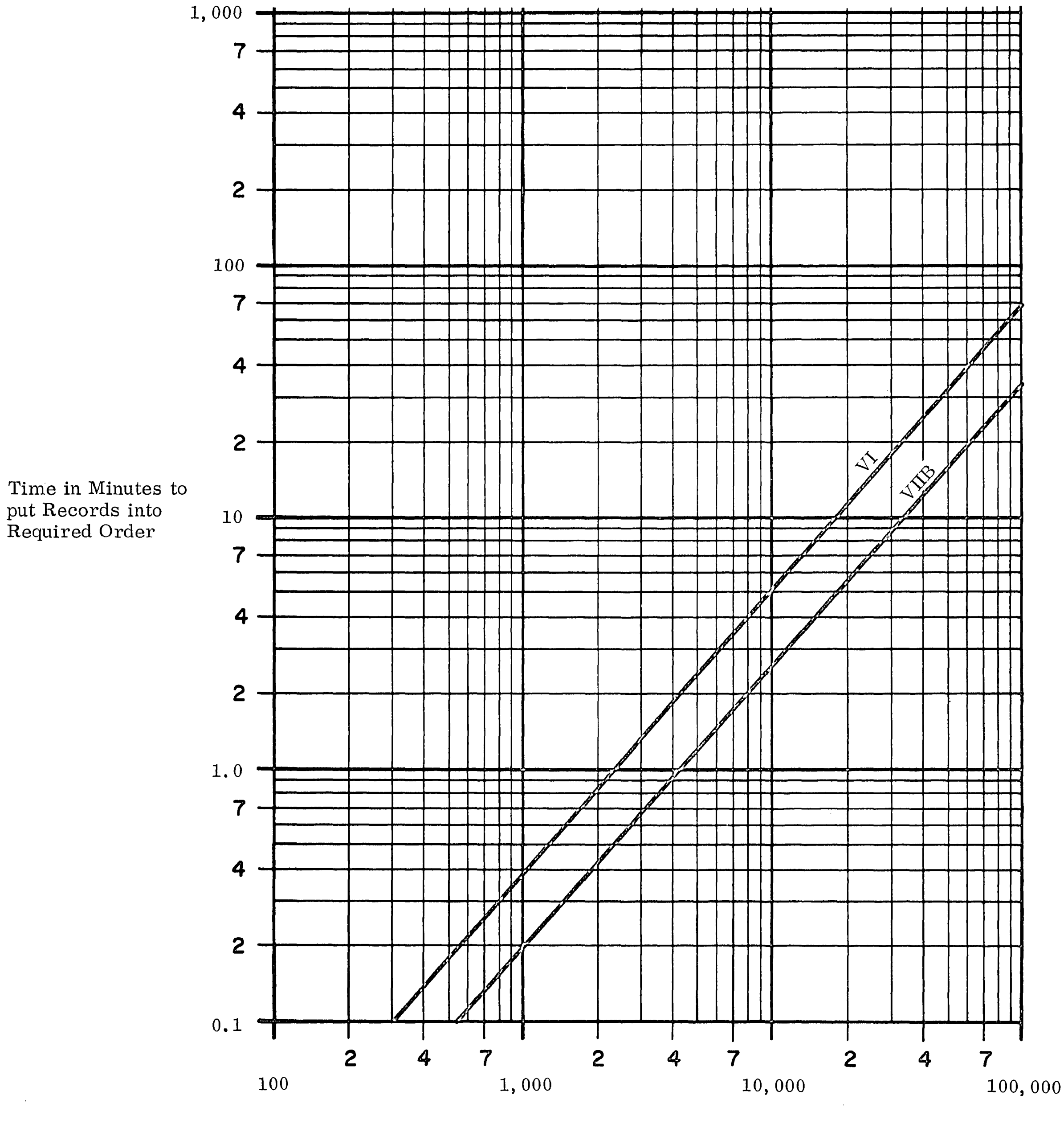
.21 Standard Problem Estimates

.211 Record size: . . . . . 80 characters.

.212 Key size: . . . . 8 characters.

.213 Timing basis: . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . see graph below.



NOTE: Roman numerals denote standard system configurations shown in Section 245:031.

§ 201.

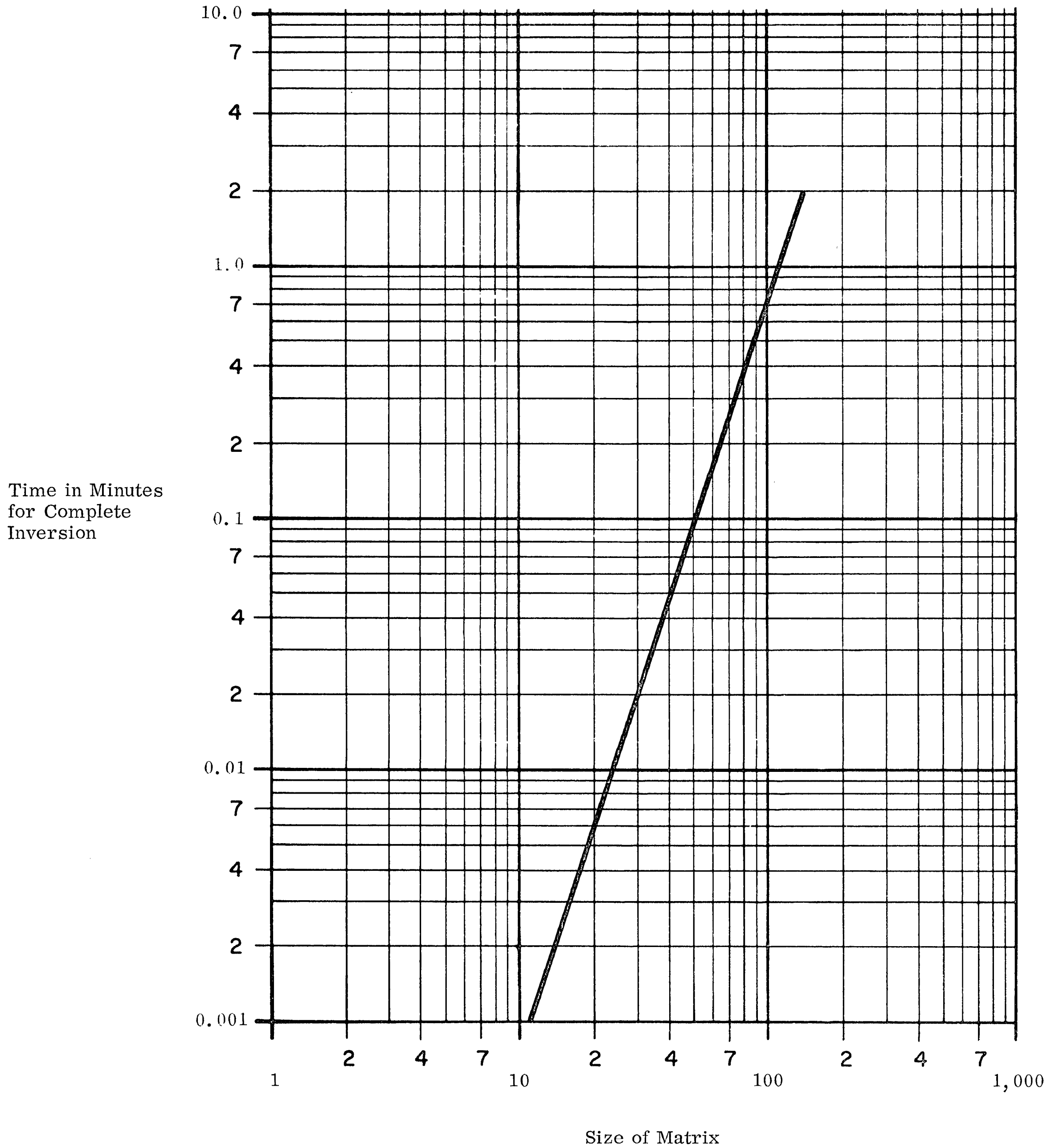
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . see graph below.



§ 201

.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

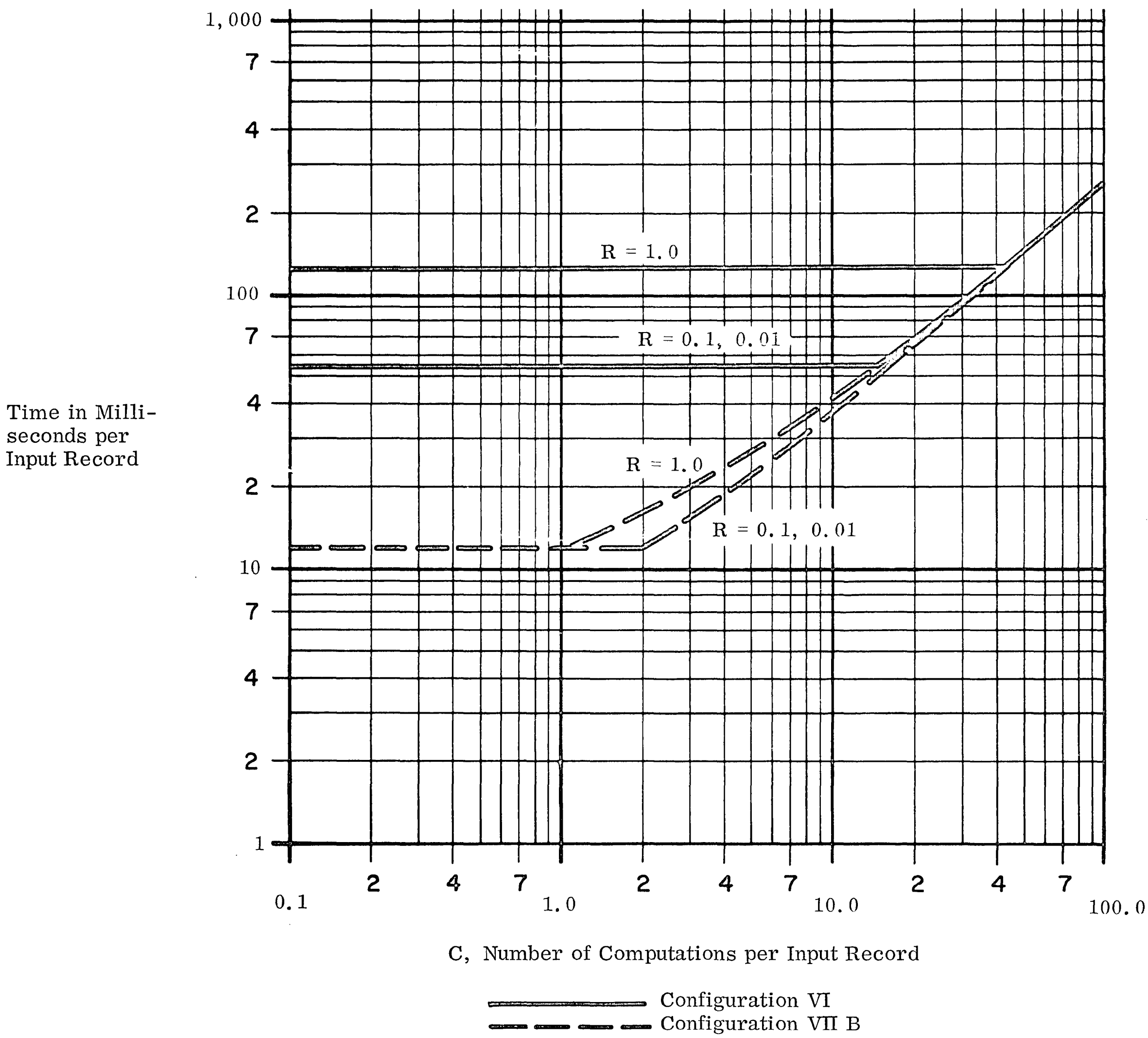
.412 Computation: . . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.413 Timing basis: . . . . using estimating procedure outlined in Users' Guide 4:200.413.

.414 Graph: . . . . see graph below.

FLOATING POINT, 36-BIT PRECISION

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



§ 201.

.5 GENERALIZED STATISTICAL PROCESSING

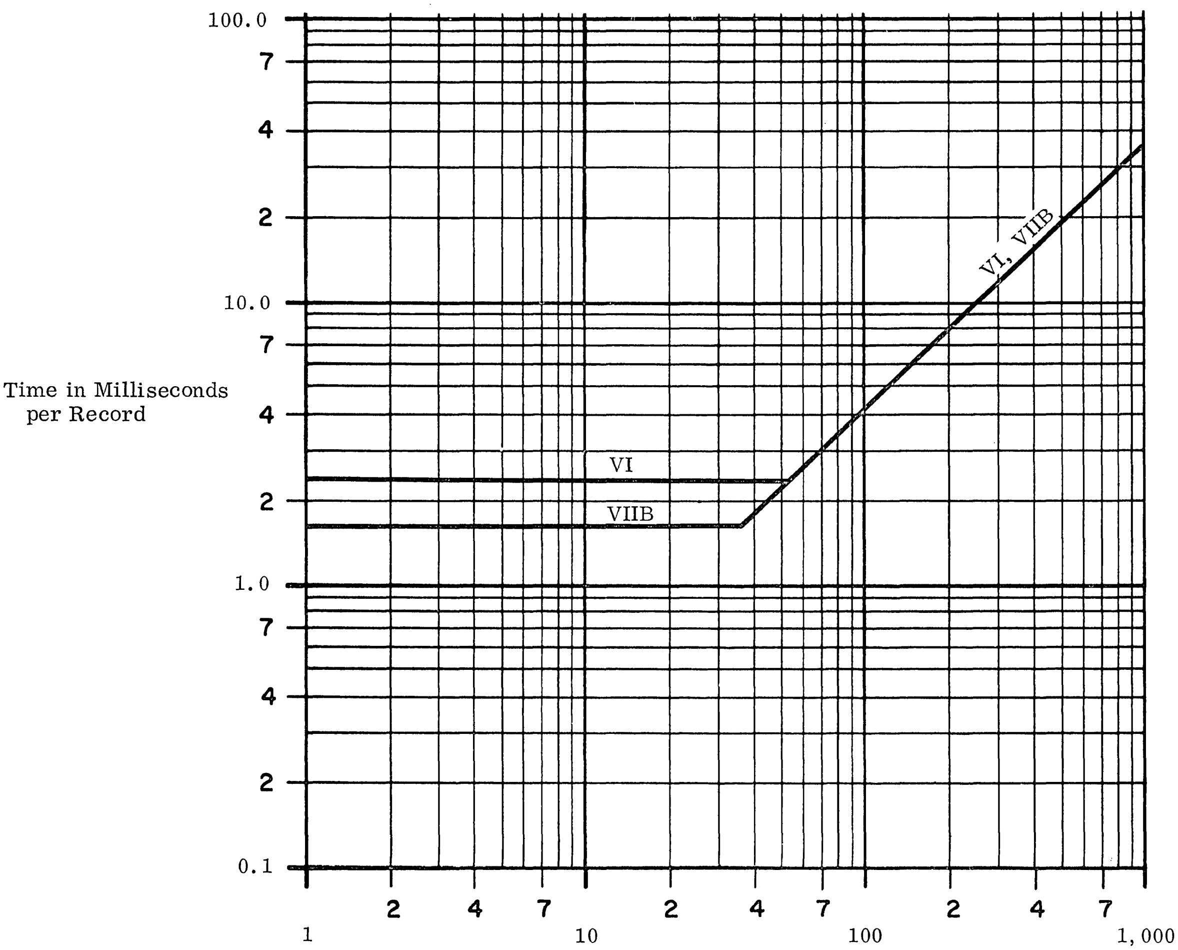
.51 Standard Statistical Problem A Estimates

.511 Record size: . . . . . . thirty 2-digit integral numbers.

.512 Computation: . . . . . augment T elements in cross-tabulation tables.

.513 Timing basis: . . . . . using estimating procedures outlined in Users' Guide, 4:200.513.

.514 Graph: . . . . see below.



T, Number of Augmented Elements

Roman numerals denote standard configurations.

PHYSICAL CHARACTERISTICS

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Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
3200 Desk Console	56.5	28.5	43.5	367	0.20	650
3200 Console I/O Typewriter	46.0	28.0	35.0	344	0.50	1,400
3204 Basic Processor *	83.8	20.1	75.0	2,000	10.8	18,500
3205 Scientific Processor	83.8	20.1	75.0	2,000	9.4	16,000
3210 Data Processor	83.8	20.1	75.0	2,000	9.6	16,400
3215 General Processor	83.8	20.1	75.0	2,000	10.0	17,000
3203 16K Storage Module	Note 1	Note 1	Note 1	80	2.40	8,200
3206 Standard Communication Channel	Note 1	Note 1	Note 1	15	0.08	76
3207 Special Communication Channel	Note 1	Note 1	Note 1	15	0.15	126
3209 8K Storage Module	Note 1	Note 1	Note 1	140	1.20	4,100
3248 Card Reader Controller	Contained in 405 Card Reader			--	--	--
3256 Line Printer Controller	46.0	20.5	56.9	?	?	?
3258 Line Printer Controller	46.0	20.5	56.9	?	?	?
3293 Incremental Plotter	30.5	27.2	42.0	288	< 0.1	785
3421 Magnetic Tape Controller	43.4	20.1	75.0	?	?	?
3422 Magnetic Tape Controller	43.4	20.1	75.0	?	?	?
3423 Magnetic Tape Controller	43.4	20.1	75.0	?	?	?
3432 Disk File Controller	88.1	27.0	75.0	1,900	3.3	11,000
3446 Card Punch Controller	46.0	20.5	56.9	?	?	?
3447 Card Reader Controller	Contained in 405 Card Reader			--	--	--
3622 through 3626 Magnetic Tape Controllers	93.5	27.0	75.0	1,850	2.2 to 3.25	7,500 to 11,000

* The Basic Processor includes 2 3206's and an 8K 3209 Storage Module in the Central Cabinet.

Note 1: One or more Auxiliary Cabinets, 40.4" wide, 20.1" deep, and 75" high, are used as necessary for these units. A single cabinet can contain 16K words of core storage plus four 3206 Channels; or 8K core storage, two 3206 Channels, and a 3228 or a 3229 Magnetic Tape Controller.

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Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
3632 Disk File Controller	88.1	27.0	75.0	1,900	3.3	11,000
3633 Disk File Controller	88.1	27.0	75.0	1,900	3.3	11,000
3634 Disk File Controller	88.1	27.00	75.00	1,900	3.3	11,000
3635 Disk File Controller	88.1	27.0	75.0	1,900	3.3	11,000
3644 Card Punch Controller	42.0	20.5	56.9	687	0.2	
3649 Card Reader Controller	Contained in 405 Card Reader			--	--	--
3659 Line Printer Controller	42.0	20.5	56.9	?	?	?
3681 Data Channel Converter	22.9	20.5	56.9	?	?	?
3682 Satellite Coupler	22.9	20.5	56.9	?	?	?
3691 Paper Tape Punch	40.0	24.0	39.3	400	0.59	2,000
3692 Paper						
3691 Paper Tape Reader/ Punch	40.0	24.0	39.3	400	0.59	2,000
3692 Program-Controlled I/O Typewriter	46.0	28.0	35.0	300	0.46	1,400
3694 Paper Tape Reader/ Punch	43.5	24.0	64.0	900	1.84	3,000
405 Card Reader	57.0	33.0	46.0	1,020	4.0	8,730
501 High Speed Line Printer	42.5	26.5	51.1	1,280	--	5,200
601 Magnetic Tape Unit	28.0	33.0	72.0	1,200	3.0	11,000
603 Magnetic Tape Unit	28.0	33.0	72.0	1,200	3.0	11,000
606 Magnetic Tape Unit	28.0	33.0	72.0	1,200	3.0	11,000
607 Magnetic Tape Unit	28.0	33.0	72.0	1,200	3.0	11,000
828 Disk File	68.2	35.2	63.5	2,575	3.6	13,650
838 Disk File	68.2	35.2	63.5	2,575	3.6	13,650

General Requirements

Temperature: . . . 62 to 78° F.
Relative humidity: . 35 to 60%.
Power: . . . . 50 or 60 cycle systems are available; 115-volt, 1-phase (30 amps) and 208-volt, 3-phase (20 amps) supplies are required.

PRICE DATA

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSORS	3204	BASIC PROCESSOR: two communication channels, 8,192 words (or 32,768 characters) of magnetic core storage, desk display console, entry keyboard, chair, on-line I/O typewriter, and control for referencing up to one additional 3209, one additional 3203, and six additional 3206 channels.	4,300	275.00	205,000
	3205	SCIENTIFIC PROCESSOR: 48-bit floating point arithmetic, 48-bit fixed point multiply and divide. Includes control, arithmetic, input-output and storage functions of the 3204 Processor.	5,000	300.00	240,000
	3210	DATA PROCESSOR: includes all operations of 3204 Processor, and features variable length (up to 13 decimal digit) BCD arithmetic.	5,050	305.00	243,000
	3215	GENERAL PROCESSOR: includes all features of the 3204 Basic, 3205 Scientific, and 3210 Data Processors.	5,150	310.00	250,000
DATA CHANNELS	3206	COMMUNICATION CHANNEL: bi-directional, buffered, 12-bit data exchange. Permits attachment of one to eight 3100, 3200, 3400 or 3600 peripheral controllers to a 3200 system.	120	35.00	5,000
	3207	COMMUNICATION CHANNEL: bi-directional, buffered, 24-bit data exchange.	200	50.00	8,500
INTERNAL STORAGE	3209	STORAGE MODULE: 8,192 words of magnetic core storage. One read/write control, accessible from two computers or special devices.	1,250	135.00	60,000
	3203	STORAGE MODULE: 16,384 words of magnetic core storage. Includes two independent 8,192-word modules, each with one read/write control accessible from two computers or special devices.	2,250	185.00	105,000

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CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
RANDOM ACCESS STORAGE	861	DRUM STORAGE: contains 4,194,304 characters of storage with 17 millisecond average access time and up to 2 million character per second transfer rate.	1,850	400.00	80,000
	862	DRUM STORAGE: contains 2,097,152 characters of storage with 8.6 millisecond average access and up to 2 million character per second transfer rate.	1,740	380.00	75,000
	3235	DRUM STORAGE: 524,288 characters of storage, 17 milliseconds average access, 167kc transfer rate.	1,150	240.00	49,000
	828	DISK FILE: 33 million character capacity, 83kc average character transfer rate, 195 millisecond average access time.	2,400	410.00	92,000
	838	DISK FILE: 66 million character capacity, 83kc average character transfer rate, 195 millisecond average access time.	3,600	580.00	155,000
INPUT-OUTPUT	405	CARD READER: 1200 cpm (80 col.), 1600 cpm (51 col.), photoelectric.	400	65.00	22,500
	415	CARD PUNCH: 250 cpm (80 col.).	295	60.00	18,150
	3691	PAPER TAPE READER PUNCH: 350 character per second reader and 110 character per second punch.	310	125.00	12,000
	3694	PAPER TAPE READER PUNCH: 1,000 character per second reader and 110 character per second punch.	645	255.00	27,400
	501	HIGH-SPEED LINE PRINTER: 1000 lines per minute, 64 characters, 136 columns.	865	240.00	42,000
	505	HIGH-SPEED LINE PRINTER: 500 lines per minute, 64 characters, 136 columns.	635	?	25,500
	3152	LINE PRINTER: 150 lines per minute, 64 characters, 120 columns, full line buffer, controller electronics.	625	280.00	29,000
	601	MAGNETIC TAPE TRANSPORT: 37.5 ips, 200 and 556 bpi, 7.5 and 20.8kc.	250	100.00	11,000
	603	MAGNETIC TAPE TRANSPORT: 75 inches per second, 200 and 556 bpi, 15 and 41.7kc.	550	120.00	24,000

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Cont.)	604	MAGNETIC TAPE TRANSPORT: 75 inches per second, 200, 556 and 800 bpi; 15, 41.7 and 60kc. Read forward and reverse.	600	130.00	26,000
	606	MAGNETIC TAPE TRANSPORT: 150 inches per second, 200 and 556 bpi; 30 and 83.3kc.	825	140.00	36,000
	607	MAGNETIC TAPE TRANSPORT: 150 inches per second, 200, 556, and 800 bpi; 30, 83.3 and 120kc. Read forward and reverse.	875	150.00	41,700
	692	MAGNETIC TAPE TRANSPORT: 9-track, 37.5 inches per second, 800 bpi, 30 kc, read forward and reverse.	300	100.00	14,000
	694	MAGNETIC TAPE TRANSPORT: 9-track, 75 inches per second, 800 bpi, 60kc, read forward and reverse.	445	115.00	21,400
	696	MAGNETIC TAPE TRANSPORT: 9-track, 112.5 inches per second, 800 bpi, 90kc, read forward and reverse.	600	135.00	28,400
	3293	INCREMENTAL PLOTTER: 300 steps per second, .01 inch per step, 11 inch width.	285	85.00	9,000
	3692	PROGRAM-CONTROLLED I/O TYPEWRITER:	280	70.00	11,000
	3681	DATA CHANNEL CONVERTER: for 160/160-A; permits 160/160-A to use 3600 peripheral equipment.	275	20.00	10,800
	3682	SATELLITE COUPLER: permits direct connection between any two standard 12-bit bi-directional channels, or Data Channel Converters.	175	25.00	9,500
COMMUNICATION EQUIPMENT	3276	COMMUNICATIONS TERMINAL CONTROLLER: Controls up to sixteen 311 or 313 Data Set Adapters, up to eight 314 Data Set Adapters, up to sixteen 321 Teletypewriter Terminals, up to thirty-two 323 Teletypewriter Terminals, or a combination of these. Operates from one standard channel.	250	55.00	12,500
	3277	COMMUNICATIONS SUPERVISOR: permits operator supervision and monitoring of communication network; includes real-time clock.	400	45.00	20,000

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
COMMUNI-CATIONS EQUIPMENT (Contd.)	3278	COMMUNICATIONS SUPERVISOR: permits operator supervision and monitoring of communications network; permits transfer of control from one computer to another; includes real-time clock.	1,000	105.00	50,000
	311	DATA SET ADAPTER: permits direct connection between 3276 and Bell 201 or 212 Data-Phone.	85	20.00	4,250
	312	DATA SET ADAPTER: permits direct connection between 3276 and Bell 201 or 212 Data-Set with 801 Automatic Dialer.	135	30.00	6,750
	313	DATA SET ADAPTER: permits direct connection between 3276 and Bell 103 Data-Set.	70	15.00	3,500
	314	DATA SET ADAPTER: permits direct connection between 3276 and Bell 103 Data-Set with 801 Automatic Dialers.	120	25.00	6,000
	321	TELETYPEWRITER TERMINAL: permits connection between 3276 and a 60, 75, or 100 word per minute full duplex teletype line.	40	10.00	2,000
	323	TELETYPEWRITER TERMINAL: permits direct connection between 3276 and a 60, 75, or 100 word per minute simplex teletype line.	25	5.00	1,250
RANDOM ACCESS CONTROL-LERS	3436	DRUM STORAGE CONTROLLER: for up to eight model 861 or 862 Drums, operated from one standard channel.	1,000	130.00	42,000
	3637	DRUM STORAGE CONTROLLER: for up to eight model 861 or 862 Drums, operated from two standard channels.	1,100	135.00	46,000
	3231	DISK PACK CONTROLLER: permits direct connection of one to five IBM 1311 Disk Storage Drives.	475	50.00	19,000
	3233	DISK PACK CONTROLLER: permits direct connection of one to eight IBM 2311 Disk Storage Drives.	625	78.00	26,200
	3432	DISK FILE CONTROLLER: for one 828 or 838 Disk File.	1,050	130.00	48,000
	3632	DISK FILE CONTROLLER: provides two independent reading, writing, or positioning controls for one 828 or 838 Disk File.	1,700	215.00	77,000

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
RANDOM ACCESS CONTROL-LERS (Contd.)	3633	DISK FILE CONTROLLER: provides two independent reading, writing, or positioning controls for two 828 or 838 Disk Files.	1,900	240.00	87,000
	3634	DISK FILE CONTROLLER: provides two independent reading, writing, or positioning controls for three 828 or 838 Disk Files.	2,100	265.00	97,000
	3635	DISK FILE CONTROLLER: provides two independent reading, writing, or positioning controls for four 828 or 838 Disk Files.	2,300	290.00	107,000
INPUT-OUTPUT CONTROL-LERS	3245	CARD PUNCH CONTROLLER: for 415 or IBM 523 Card Punch; one channel; unbuffered.	330	45.00	14,000
	3248	CARD READER CONTROLLER: for 405 Card Reader; one channel; unbuffered.	100	35.00	4,800
	3446	CARD PUNCH CONTROLLER: for 415 or IBM 523 Card Punch; one channel; full card buffer.	450	65.00	22,000
	3447	CARD READER CONTROLLER: for 405 Card Reader; one channel; full card buffer.	225	55.00	11,250
	3644	CARD PUNCH CONTROLLER: for 415 or IBM 523 Card Punch; two channels; full card buffer.	675	50.00	32,500
	3649	CARD READER CONTROLLER: for 405 Card Reader; two channels; full card buffer.	325	40.00	16,200
	3659	LINE PRINTER CONTROLLER: for 501 Printer; two standard channels or Data Channel Converters.	700	85.00	38,500
	3256	LINE PRINTER CONTROLLER: for 501 Printer; one channel.	515	60.00	22,000
	3258	LINE PRINTER CONTROLLER: for IBM 1403 Printer, model 2 or 3; one channel.	900	110.00	40,000
	3127	MAGNETIC TAPE CONTROLLER: for 1 to 4 model 601 Tape Transports; one channel.	320	55.00	14,000
	3228	MAGNETIC TAPE CONTROLLER: for 1 to 4 model 604 or 607 Tape Transports; one channel.	425	65.00	20,000
	3229	MAGNETIC TAPE CONTROLLER: for 1 to 8 model 604 to 607 Magnetic Tape Transports; one channel.	600	75.00	24,000
	3421	MAGNETIC TAPE CONTROLLER: two channels; 1 to 4 model 604 or 607 Tape Transports.	950	135.00	45,000
	3422	MAGNETIC TAPE CONTROLLER: two channels; 1 to 6 model 604 or 607 Tape Transports.	1,450	160.00	71,000

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT CONTROL-LERS (Contd.)	3423	MAGNETIC TAPE CONTROLLER: two channels; 1 to 8 model 604 or 607 Tape Transports.	1,950	205.00	96,000
	3622	MAGNETIC TAPE CONTROLLER: 1 to 16 model 606 or 607 Tape Transports; two channels.	2,800	305.00	135,000
	3623	MAGNETIC TAPE CONTROLLER: 1 to 8 model 606 or 607 Tape Transports; four channels.	2,900	290.00	140,000
	3624	MAGNETIC TAPE CONTROLLER: 1 to 16 model 606 or 607 Tape Transports; four channels.	3,900	380.00	185,000
	3625	MAGNETIC TAPE CONTROLLER: 1 to 8 model 606 or 607 Tape Transports; three channels.	2,450	250.00	120,000
	3626	MAGNETIC TAPE CONTROLLER: 1 to 16 model 606 or 607 Tape Transports; three channels.	3,300	340.00	160,000
	3825	MAGNETIC TAPE CONTROLLER: 1 to 4 model 692, 694, or 696 Tape Transports; two channels.	800	130.00	38,000
	3826	MAGNETIC TAPE CONTROLLER: 1 to 6 model 692, 694, or 696 Tape Transports; three channels.	1,100	145.00	52,000
	3827	MAGNETIC TAPE CONTROLLER: 1 to 8 model 692, 694, or 696 Tape Transports; four channels.	1,400	160.00	66,000

CDC 3400

Control Data Corporation

STANDARD EDP REPORTS

AUERBACH

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PRINTED IN U. S. A.

CDC 3400

Control Data Corporation

STANDARD EDP REPORTS

AUERBACH INFO, INC.

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CONTENTS

INA = Information Not Available

INTRODUCTION

§ 011.

The Control Data 3400 is a medium to large scale data processing system that is primarily oriented toward scientific, simulation, or control applications that require extensive computations and a large amount of fast-access storage. First customer deliveries are scheduled for November, 1964. The 3400 will usually be used as a magnetic tape oriented system. Multicomputer facilities make it possible to connect other Control Data computer systems on-line to a 3400 system.

The standard arithmetic mode is fixed point binary, using 48-bit words. A single-precision floating point hardware package is optional at extra cost, and will be required for efficient performance in most scientific applications. Without the hardware package, floating point instructions are "trapped", causing jumps to subroutines which simulate the effects of the absent machine instructions.

The Control Data 3400 should not be regarded simply as a system whose capabilities fill a gap between the Control Data 3200 and 3600 systems. Although both its price and basic processing speeds are about two-thirds as high as those of the Control Data 3600, the 3400 is limited to four input-output data channels and lacks such 3600 features as the D (flag) register and the powerful block transfer, list search, and byte manipulation instructions. The absence of these advanced processing facilities will curtail the relative efficiency of the 3400 in complex real-time systems, information retrieval, and other list-processing applications. For conventional high-speed scientific processing of the FORTRAN style, however, these advanced processing facilities of the 3600 are not normally used, and their absence from the 3400's instruction repertoire will not seriously affect its productivity. In such circumstances, the Control Data 3400 can be regarded as being nearly as good as the 3600 — at a considerably lower price.

Hardware

The 3400 central processor includes a core storage module with a capacity of 16,384 51-bit words (48 data bits and 3 parity bits) as part of the basic system. The optional 3409 Core Storage Module doubles the total core storage capacity to 32,768 words. Core storage cycle time is 1.5 microseconds. Except for a few special-purpose instructions, the 3400 processor maintains upward program compatibility with the larger Control Data 3600 processor; i.e., it will be possible to run most 3400 programs on a 3600 system with little or no alteration — the converse will not be true because of the 3600's unique advanced processing facilities.

Arithmetic operations are performed in parallel on 48-bit words. A word can contain a pair of 24-bit single-address instructions or one 48-bit input-output instruction. The operand addresses of most instructions can be indexed or indirectly addressed. Three bits are provided in the instruction for selecting one of six index registers; one of the values formed by these three bits signifies indirect addressing.

Included in the instruction repertoire are a family of Augment instructions that are used to modify the second instruction of the instruction word pairs in which they appear. This is a powerful facility which can be used, for example, to provide double indexing capabilities for most 24-bit instructions, or to direct which one of a number of modifications to a standard instruction should be used.

The 3400 has an interrupt system in which individual interrupt conditions can be honored or ignored, as the program warrants. An interrupt condition is executed by transferring control to a fixed location, recording a return address, and initiating an interrupt routine lock-out that remains in effect until a return jump is executed. The programmer must include his own routines to identify and handle each internal and peripheral interrupt condition.

The Control Data 3400 system can be equipped with up to four input-output data channels, enabling the system to compute while simultaneously performing up to four read-write operations which use any four peripheral devices in the system. A wide range of both old and new peripheral equipment is available for use with the 3400 system.

§ 011. **INTRODUCTION (Contd.)**

Two models of magnetic tape units and a variety of tape controllers are being offered The 604 and 607 Magnetic Tape Units are new additions to the Control Data line which provide a recording density of 800 characters per inch, a data transfer rate of 120,000 characters per second, and the ability to read backward. The 604 and 607 are compatible with each other, with the older Control Data 603 and 606 Tape Units, and with the IBM 729 and 7330 Tape Units.

The same Disk File subsystem that was announced recently for the Control Data 3600 system will be available for the 3400. This equipment consists of a Disk File Controller and from one to four Model 828 Disk Files, manufactured by Data Products Corporation. Each Disk File has a capacity of 33 million 6-bit characters. Each Disk File Controller includes two read-write controls which permit simultaneous access to one or two Disk Files, allowing any combination of two of the three functions of reading, writing, or positioning to occur simultaneously.

Three different printers have been announced — two "old" and one new. The improved older units operate at peak speeds of 300 and 1,000 single-spaced alphanumeric lines per minute. The new unit, built by Control Data's Peripheral Equipment Division in Minneapolis, is also rated at 1,000 lines per minute but extends the line width from 120 to 136 printing positions. New CDC-built card equipment is also available: the 405 Card Reader (1,200 cards per minute) and 415 Card Punch (250 cards per minute). Still offered, however, is an adapted version of the IBM 523 Card Punch (100 cards per minute).

Other announced peripheral units include a combination paper tape reader-punch that reads tape at 350 characters per second and punches at 110 characters per second; a program-controlled input-output typewriter which is an adaptation of the IBM 731 Selectric typewriter; and an incremental plotter that can make up to three hundred 0.01-inch steps per second.

Software

COMPASS is Control Data Corporation's symbolic assembly system for the 3400. The assembler is basically a one-to-one translator, but it includes a generous sprinkling of useful macro instructions.

The 3400 FORTRAN language allows problems of a mathematical or scientific nature to be expressed in algebraic notation. The language is a dialect of FORTRAN IV. 3400 FORTRAN is compatible with other FORTRAN languages in different degrees, and conversions will involve desk checking of varying intensities. The 3400 FORTRAN compiler and its object programs run under the control of the 3400 SCOPE operating system.

The 3400 COBOL language is the commercial and business oriented compiler counterpart of 3400 FORTRAN. The 3400 COBOL compiler and the object programs it generates run under the control of the 3400 SCOPE operating system.

SCOPE is the operating system under which programs coded in 3400 COMPASS, FORTRAN, and COBOL will generally be compiled and run. This permits the mixing of subprograms coded in different languages and provides greater flexibility. The SCOPE system controls all input-output units. It provides macros, subroutine library facilities, and job batching with elementary diagnostic facilities incorporated. SCOPE includes no announced provisions for multi-running, so unless the 3400 user elects to develop his own operating system, he will generally be able to execute only one job at a time, at least until there are some new developments in this area.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	48 data bits + 3 parity bits	basic addressable unit; contains data item or two instructions.
Character:	6 bits	internal BCD code.
Block:	1 to N words	magnetic tape.

.2 INFORMATION FORMATS

Type of Information	Representation
Operands:	48-bit fixed-point word. 48-bit floating-point word.
Instructions:	24 or 48 bits. 24-bit instructions are packed two per 48-bit word.
Fixed-point numbers:	47 data bits plus 1 sign bit (one's complement notation).
Floating-point numbers (single precision): . .	36 bits plus sign for fixed-point part; 10 bits plus sign for exponent.

SYSTEM CONFIGURATION

§ 031.

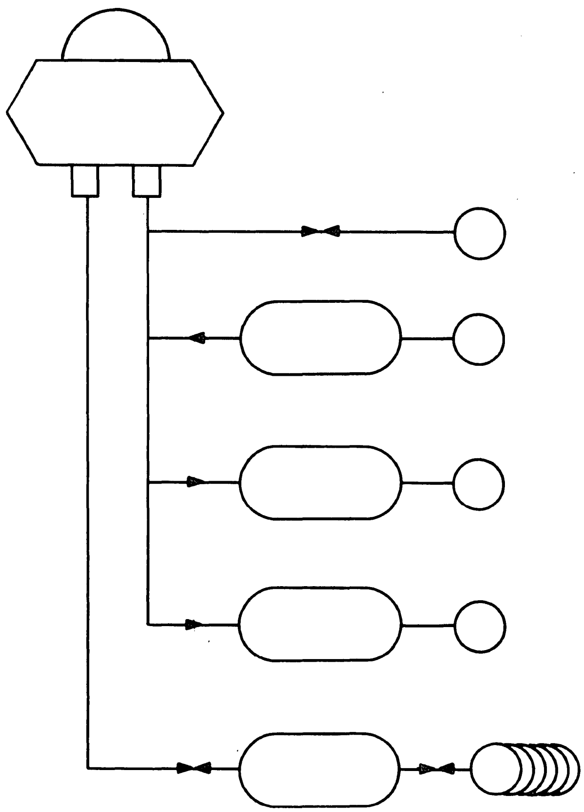
The CDC 3400 system is organized along the following basic lines:

- The central processor includes 16,384 48-bit words of core storage, which can be expanded to twice this size. An optional floating point hardware package is also available.
- Up to four bi-directional data channels can be connected to the central processor so that from one to four input-output operations can proceed in parallel.
- A combination of up to eight peripheral units, controllers, and adapters can be connected to any one channel. A controller can control one or more units, depending on the design of the specific peripheral equipment.
- Adapters to connect the data channel with satellite computers, data transmission devices, etc., can also be connected.

§ 031.

.1 6-TAPE BUSINESS/SCIENTIFIC SYSTEM; CONFIGURATION VI

Deviations from Standard Configuration: . . . . . 3 more index registers and console typewriter are included.
card reader is 140% faster.
line printer is 100% faster.
magnetic tape is 100% faster.
core storage is 100% larger.

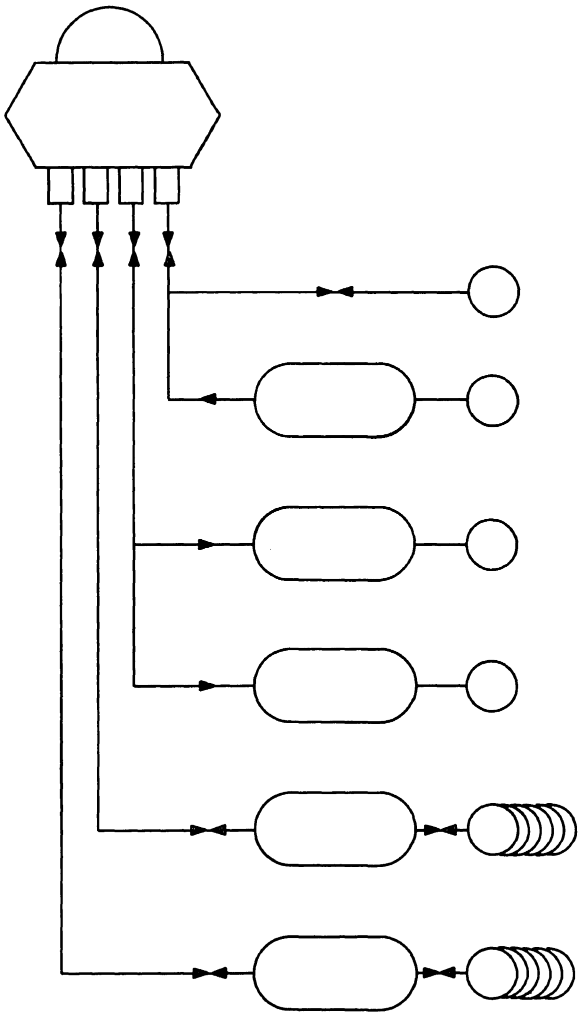


Equipment	Rental
Core Storage 16,384 words; 3404 Central Processor with 3410 floating point package	$14,550
3406 Data Channels (2)	2,200
3401 Console including I/O typewriter: 10 cps	720
3248 Card Read Controller and 405 Card Reader: 1,200 cpm	915
3245 Card Punch Controller and IBM 523 Card Punch: 100 cpm	440
3256 Line Printer Controller and 501 Line Printer: 1,000 lpm	1,880
3229 Magnetic Tape Controller	800
604 Magnetic Tape Units (6): 60,000 char/sec	4,050
TOTAL:	$25,555.

§ 031.

.2 INTEGRATED 10-TAPE GENERAL BUSINESS SYSTEM; CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . . Card Reader is 140% faster.
Line Printer is 100% faster.
Core storage is 33% larger.

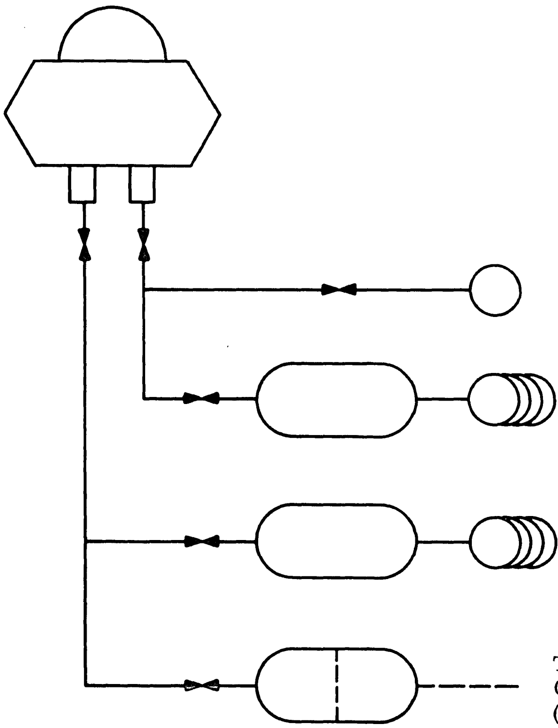


Equipment	Rental
Core Storage: 16,384 words; 3404 Central Processor with 3410 floating point package	$14,550
3406 Data Channels (4)	4,400
3401 Console including I/O Typewriter: 10 cps	720
3248 Card Reader Controller and 405 Card Reader: 1,200 cpm	915
3245 Card Punch Controller and IBM 523 Card Punch: 300 cpm	440
3659 Line Printer Controller	1,490
501 Line Printer: 1,000 lpm	1,165
3229 Controllers (2) and	1,600
604 Magnetic Tape Units (10) 60,000 char/sec	6,750
TOTAL:	$30,930

§ 031.

3. PAIRED 10-TAPE GENERAL BUSINESS SYSTEM; CONFIGURATION VIIB

Deviations From Standard Configuration: . . . . . Direct Connection to Auxiliary Computer. Core storage is 33% larger.



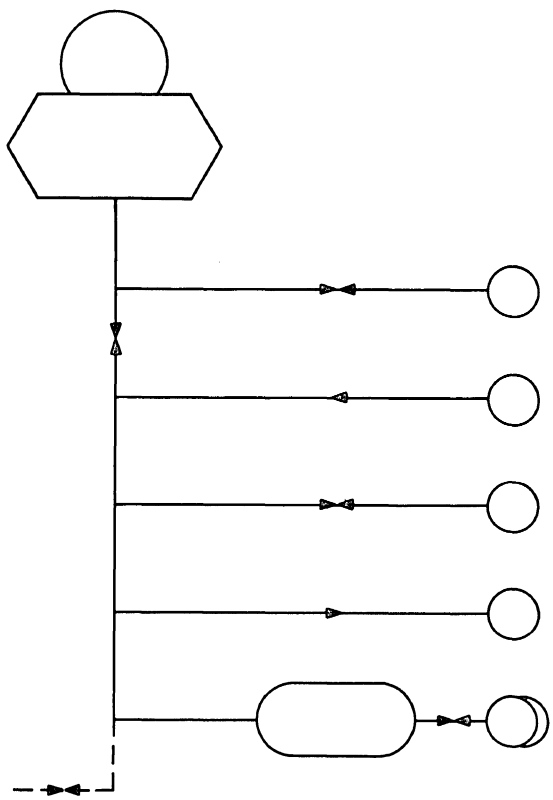
To Auxiliary Computer (at right)

Equipment	Rental
Core Storage: 16,384 words; 3404 Central Processor with 3410 Floating Point Hardware	$14,550
3406 Data Channels (2)	2,200
3401 Console including I/O Typewriter: 10 cps	720
3228 Magnetic Tape Controller (2)	1,440
and	
604 Magnetic Tape Units (8) 60,000 cps	5,600
3681 Data Channel Converter	275
3682 Satellite Coupler	415
TOTAL:	$25,200
Total, including both computers:	$31,859

§ 031.

Auxiliary Computer (CDC 160)

Deviations from Standard Configuration: . . . . . direct connection to main computer.
printer is 100% faster.
card reader is 50% slower.
multiply/divide included.
typewriter output.
paper tape input and output.



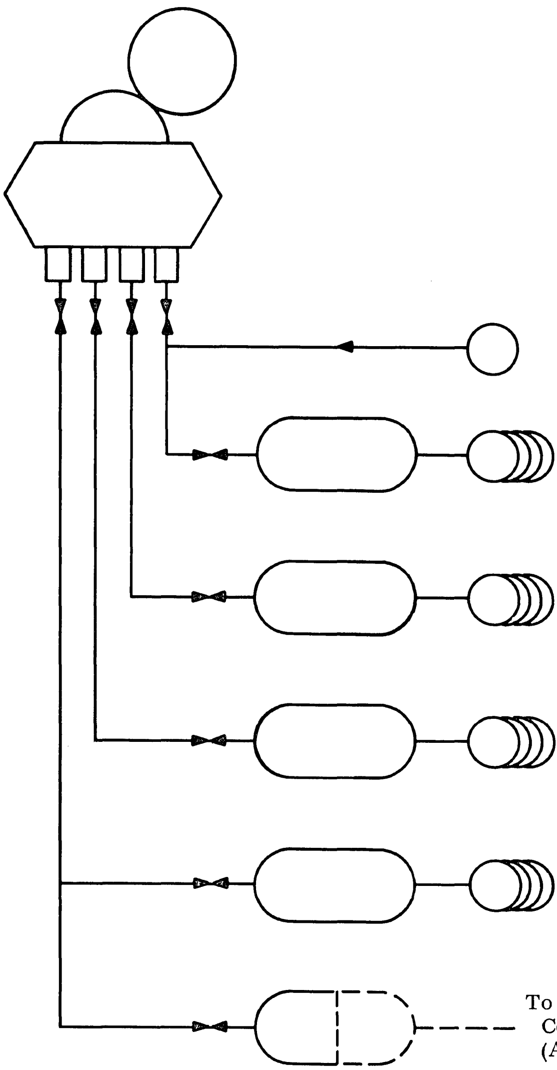
To Main Computer
(at left)

Equipment	Rental
Core Storage: 4,096 12-bit words	
CDC 160 Central Processor:	$1,762.
Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	
167 Card Reader: 250 cards/minute	400
1609 Card Read/Punch Unit: 100 cards/minute	1,175
1612 Line Printer: 1000 lines/minute	1,840
163-2 Magnetic Tape Unit with 2 tape units; peak speed 30,000 char/sec:	1,482
TOTAL:	$6,659

§ 031.

.4 PAIRED 20-TAPE GENERAL BUSINESS SYSTEM: CONFIGURATION VIIIB

Deviations from Standard Configuration: . . . . . 4 less index registers.
Direct connection to auxiliary computer.
Core storage is 800% larger.

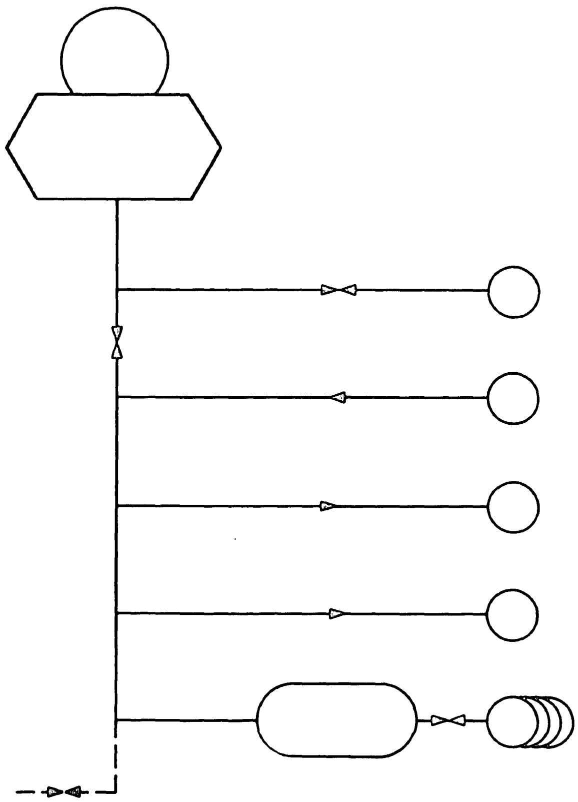


Equipment	Rental
3409 Core Storage: 16,384 words	$ 3,500
Core Storage: 16,384 words; 3404 Central Processor with 3410 Floating Point Package	13,550
3406 Bi-directional Data Channels (4)	4,400
3401 Console including I/O Typewriter: 10 cps	720
3228 Magnetic Tape controllers (4)	2,880
and	
607 Magnetic Tape Units (16): 120,000 cps	14,960
3681 Data Channel Converter	275
3682 Satellite Coupler	415
TOTAL:	$40,420
Total, including both computers:	$49,330

§ 031.

Auxiliary Computer (CDC 160-A)

Deviations from Standard Configuration: . . . . . direct connection to main computer.
card reader is 75% slower.
printer is 50% slower.
multiply/divide included.
typewriter output.
paper tape input and output.



To Main Computer (At left)

Equipment	Rental
Core Storage: 8,192 12-bit words CDC 160-A Central Processor: Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	$2,250
167 Card Reader: 250 cards/minute	400
170 Card Punch Controller	335
IBM 523 Punch: 100 card/minute	85
1612 Line Printer: 1000 lines/minute	1,840
162-2 Magnetic Tape	700
System with 4 tape units; peak speed 83,400 char/sec.	3,300
TOTAL	$8,910

INTERNAL STORAGE: CORE STORAGE

§ 041.

.1 GENERAL

.11 Identity: . . . . Core Storage, part of 3404 Central Processor (16K) 3409 Storage Module (16K).

.12 Basic Use: . . . . working storage.

.13 Description

The CDC 3404 Central Processor includes a core storage module with a capacity of 16,384 words, as part of the basic system. The optional 3409 Core Storage Module doubles the total storage capacity from 16,384 to 32,768 words. Each word location holds 48 data bits plus 3 parity bits. Core storage cycle time is 1.5 microseconds.

The expanded storage permits more throughput and faster operations by providing larger input and output areas. The addition of the extra module does not constitute a separate "bank" as in the CDC 3600, and its operations cannot be overlapped with those of the first storage module.

A maximum of four bi-directional input-output data channels are available for connecting peripheral units directly to the core storage.

.14 Availability: . . . . . . ?

.15 First Delivery: . . . . November, 1964.

.16 Reserved Storage: . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . magnetic cores.

.23 Storage Phenomenon: direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . . no.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . no.
.245 Storage changeable: . no.

.27 Interleaving Levels: . none.

.28 Access Techniques: . coincident current.

.29 Potential Transfer Rates

.292 Peak data rates
Cycling rates: . . . . 667,000 cps.
Unit of data: . . . . . one 48-bit word.
Gain factor: . . . . . 1; only 1 bank.
Data rate: . . . . . . 667,000 words/second.

.3 DATA CAPACITY

.31 Module and System Sizes

Minimum storage: . . 16,384 48-bit words.
Maximum storage: . . 32,768 48-bit words.

.32 Rules for Combining Modules: . . . . only one module per system.

.4 CONTROLLER: . . . no separate controller required.

.5 ACCESS TIMING

.52 Simultaneous Operations: . . . . none.

.53 Access Time Parameters and Variations

.531 For uniform access
Cycle time: . . . . . 1.5 μsec.
For data unit of: . . 48-bit word.

.6 CHANGEABLE STORAGE: . . . . . . none.

.7 STORAGE PERFORMANCE

.72 Transfer Load Size

With self, via accumulator: . . . . . . one 48-bit word.

.73 Effective Transfer Rate

With self: . . . . 1,051,525 characters/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Receipt of data:	generate parity bits.	
Recording of data:	record parity bits.	
Recovery of data:	check	optional interrupt.
Reference to programmed-control locked area:	check	optional interrupt.
Instruction parity:	interlock	halt, light.

INTERNAL STORAGE: DISK FILE

§ 042.

.1 GENERAL

.11 Identity: . . . . 828 Disk File.

.12 Basic Use: . . . . auxiliary storage.

.13 Description

The 828 Disk File, manufactured by Data Products Corp., provides 33,000,000 characters of random access storage in a single peripheral unit. Access time to a randomly-placed disc record is approximately a quarter of a second, giving a capacity of 240 random accesses per minute per data channel. Actual data transfer rate, after access, is dependent on block size and can reach magnetic tape speeds. The frequency of repositioning the access arms over the appropriate parts of the file cannot be reduced by any equivalent of the "cylinder"* mode, so that the random access time remains an important consideration.

The 828 Disk File consists of 16 discs (32 recording surfaces) capable of storing up to 33 million characters. Four different controllers are available — Models 3632, 3633, 3634, and 3645 — which control one, two, three, or four Disk Files, respectively. Each of the controllers is a dual-channel device that allows any two of the three functions of reading, writing, and positioning to proceed simultaneously. Single-channel controllers are not available. (Note: positioning, which averages 225 milliseconds for a random movement, occupies a data channel throughout the operation, just the same as reading or writing.)

Each disc surface is divided into two 128-track parts called the outer and inner zones. Each circumferential track is, in turn, divided into a number of addressable blocks; 20 blocks per outer-zone track and 12 per inner-zone track. This arrangement yields a total of 4,096 fixed, addressable block positions on each disc surface at which the reading or writing of data can begin. Each block has a fixed capacity of 256 six-bit characters.

Each disc is served by an individually positionable access arm containing eight read-write heads, four for the upper disc surface and four for the lower disc surface. Two of the four heads access tracks in the outer zone, and the other two access tracks in the inner zone. At any one position, eight tracks may be accessed to enable the sequential transfer of up to 32,768 characters. Considering all 16 discs, up to 525,000 characters (65,536 words) can be transferred with no movement of

* In the cylinder mode, all the arms are synchronized, so that if any one arm moves, they all move. Effectively, this means that where files can be arranged to occupy an equivalent track on each disc (i.e., in a single "cylinder"), repositioning access time is drastically reduced.

.13 Description (Contd.)

the access arms. However, because each positioning arm moves independently, there is no "cylinder" mode of operation.

The total access time for the 828 Disk File can be determined by combining four different timing considerations:

- Positioning motor power — 11 milliseconds are required to turn on power for an arm positioning motor; only two can be on concurrently.
- Arm positioning — this time can range from zero (for no movement) to 250 milliseconds (for maximum movement). Average positioning time for all 4,096 possible positioner movements is 145 milliseconds.
- Position confirmation — each block address recorded around the accessed track is checked against the current address sent from the computer; thus the full disc revolution time of 52 milliseconds is needed to perform this operation. This period also helps reliability by allowing any vibrations to die down before data transmission.
- Latency — average time to reach the addressed block is one-half a disc revolution or 26 milliseconds.

The peak data transfer rate is 59,000 (inner zone) or 98,000 (outer zone) characters per second. The effective transfer rates resulting from different block sizes on a purely random basis are shown in graph 246:042.900.

A parity check is made on each character transferred to or from the core storage. In addition, each 256-character block has an associated 12-bit cyclic code check word to help increase reading and writing accuracy. The detection of a parity error results in the termination of the disc operation. A unique 19-bit address for each block is permanently recorded at the beginning of each block for both block identification and track address confirmation. The block address is also checked for parity.

.14 Availability: . . . . not specified.

.15 First Delivery: . . . . . not specified.

.16 Reserved Storage

Purpose	Number of locations
Clocking:	4 tracks on top disc, using fixed heads.
Spares:	3 tracks.
Format:	none.
Address:	19 bits at beginning of each block.

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.2 PHYSICAL FORM

.21 Storage Medium: . . . . multiple magnetic discs.

.22 Physical Dimensions

.222 Disc
Diameter:. . . . . 31 inches.
Thickness or length:. thin.
Number on shaft: . . . 16.

.23 Storage Phenomenon: . magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changable: . . . no.

.25 Data Volume per Band of 1 Track

	Inner Zone	Outer Zone
Words:	384	640.
Characters:	3,072	5,120.
Digits:	3,072	5,120.
Instructions:	768	1,280.
Blocks	12	20.

.26 Tracks per Physical Unit: . . . . 512 (256 per disc surface).

.27 Interleaving Levels: . . 1; i.e., no interleaving.

.28 Access Techniques

.281 Recording method: . . . individual multiple-head positioning arms.

.283 Type of access

Description of Stage	Possible Starting Stage?
Turn on positioning arm motor:	if this disc is not currently in use (maximum of 2 discs in use at a time).
Move head to selected track:	if new track is selected.
Confirm track address:	no.
Wait for start of selected block: . .	if same track was previously selected.
Transfer data:	no.

.29 Potential Transfer Rates

.291 Peak bit rates
Cycling rates: . . . . . 1,200 rpm.
Bit rate per track: . . 350,000 or 590,000 bits/sec/track.

.292 Peak data rates
Unit of data: . . . . . . character.
Conversion factor: . . 6 bits/character.
Data rate: . . . . 59,000 (inner zone) or 98,000 (outer zone) char/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

	Minimum Storage	Maximum Storage (per Controller)
Identity:	828	828.
Discs:	16	64.
Words:	4,250,000	17,000,000.
Characters:	33,000,000	132,000,000.
Instructions:	8,500,000	34,000,000.
Blocks:	131,200	524,800.
Files:	1	4.

.4 CONTROLLER

.41 Identity: . . . . 3632 Disk File Controller (for 1 file).
3633 Disk File Controller (for 2 files).
3634 Disk File Controller (for 3 files).
3635 Disk File Controller (for 4 files).
Each of these controllers has 2 read-write controls.

.42 Connection to System

.421 On-line: . . . . up to 4 controllers.
.422 Off-line: . . . . none.

.43 Connection to Device

.431 Devices per controller: 1, 2, 3, or 4 files depending on controller model.

.44 Data Transfer Control

.441 Size of load: . . . . 1 to N blocks, limited by core storage capacity.
.442 Input-output area: . . . core storage.
.443 Input-output area access: . . . . each word or character.
.444 Input-output area lockout: . . . . none.
.445 Synchronization: . . . . automatic.
.447 Table control: . . . . . . none.
.448 Testable conditions: . . device-controller ready; device busy; error condition.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks
Stacks per system: . . 128 to 512 per controller.
Stacks per file: . . . . 128.
Stacks per yoke: . . . 8.
Yokes per file: . . . . 16 (one for each disc).
.512 Stack movement: . . . . horizontal only.

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.513 Stacks that can access any particular location: .... 1.

.514 Accessible locations
By single stack
With no movement:. 12 or 20 blocks.
With all movement:. 768 or 1,280 blocks.
By all stacks
With no movement:. 2,050 blocks per file.

.52 Simultaneous Operations:........... All Disk File Controllers provide dual, simultaneous access to 1 or 2 files, allowing any combination of 2 of the three functions of reading, writing or positioning.

.53 Access Time Parameters and Variations

.532 Variation in access time

Stage	Variation (msec)	Average (msec)
Turn on positioning arm motor:.....	0 or 11	10.
Move head to selected track:......	0 to 250	145.
Confirm track address:........	52	52.
Wait for selected block:	0 to 52	26.
Transfer 1 block:..	2.6 or 4.3	3.
Total:	54.6 to 369.3	236.

.6 CHANGEABLE STORAGE:....... none.

.7 AUXILIARY STORAGE PERFORMANCE

.72 Transfer Load Size

With core storage:... 1 to N blocks.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	not possible.	
Invalid code:	check	interrupt.
Receipt of data:	12-bit cyclic code check word per block	interrupt.
Recording of data:	generate 12-bit check word.	
Recovery of data:	none.	
Dispatch of data:	none.	
Timing conflicts:	none.	
Physical record missing:	check	interrupt.
Reference to locked area:	check	interrupt.
Wrong block selected:	address comparison	interrupt.

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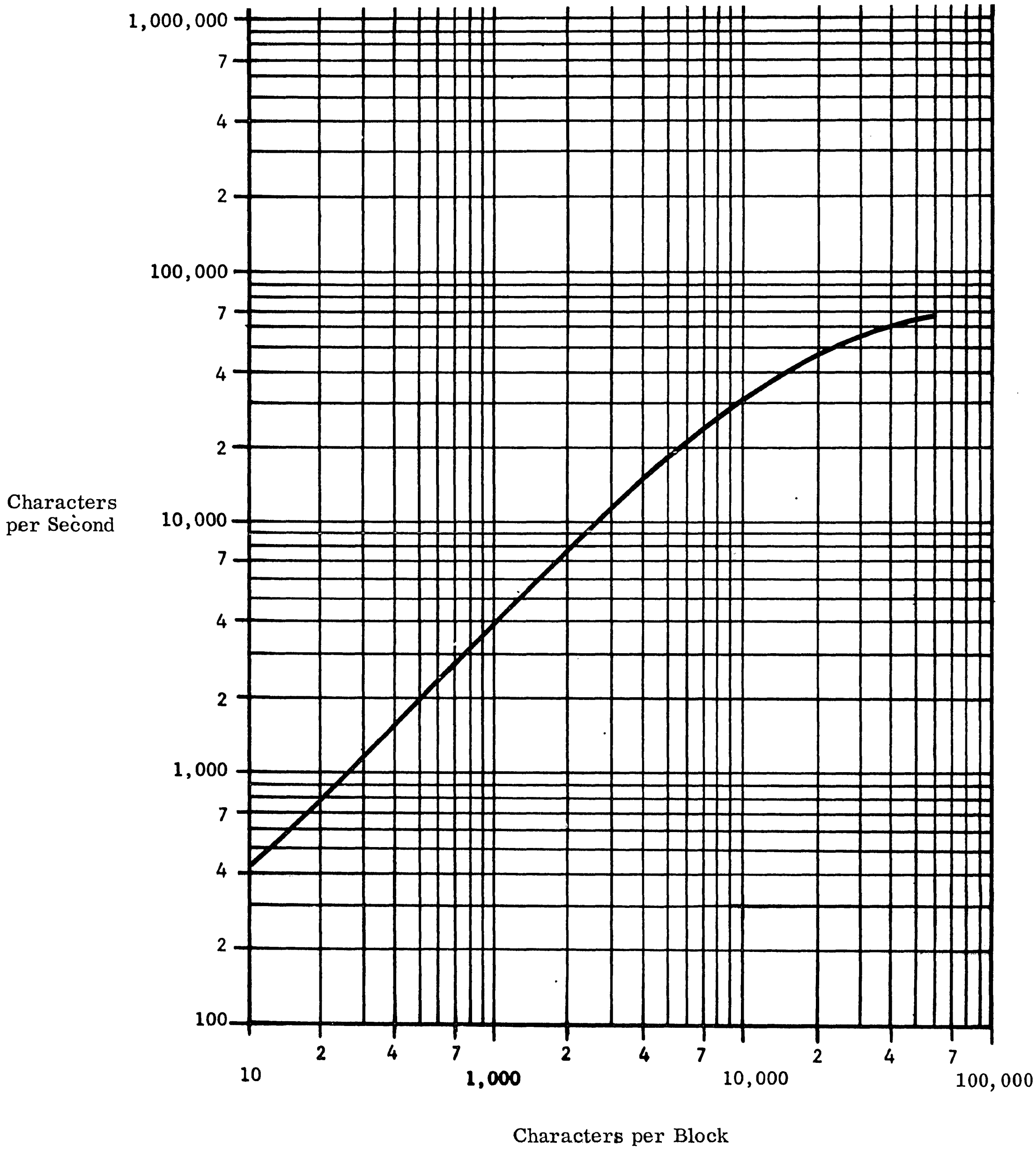
EFFECTIVE SPEED: 828 DISK FILE

Based on random accessing and varying record sizes



CENTRAL PROCESSOR

§ 051

.1 GENERAL

.11 Identity . . . . 3404 Basic Computer.

.12 Description

The 3404 Basic Computer is a single-address, fixed word-length, binary processing unit. Except for a few special-purpose instructions, this processor maintains upward program compatibility with the larger-scale Control Data 3600 processor. In addition to the arithmetic and control logic, the 3400 processor cabinet includes 16,384 words of core storage, described in Section 246:041.

Arithmetic operations are performed in parallel on 48-bit words. A word can contain a pair of 24-bit single-address instructions or one 48-bit input-output instruction. The operand addresses of most instructions can be indexed or indirectly addressed. Three bit positions are provided in the instruction for selecting one of six index registers; one of the values formed by these bits (111) is used to signify indirect addressing.

Fixed point arithmetic operations using 48-bit operands (or 96 bits in the case of multiplication and division) are standard. An optional floating point hardware package is available which adds Floating Point Add, Subtract, Multiply and Divide to the instruction repertoire. Floating point operands consist of an 11-bit exponent and sign, plus a 36-bit fixed point part.

The Augment instructions are a family of 24-bit instructions that modify the second 24-bit instruction of the same instruction word pair. This is a powerful facility that can be used, among other things, to:

- provide double indexing capabilities for most 24-bit instructions. The resultant operand address that is used in executing the modified instruction is computed by adding the contents of the index register of the Augment instruction to the address of the actual instruction, which can itself have a specified index register. Thus, the result of executing the instruction pair "Augment, index register 3; Add, index register 4, 00500" when index register 3 contains 00011, and index register 4 contains 01020, would be to add the contents of storage location 01531 to the contents of register A. (Indirect addressing is possible as an alternative to direct indexing in both the augmenting and augmented instruction.)

.12 Description (Contd.)

- direct which of a number of modifications to standard instructions should be used. The actual modifications available depend on the instruction, and provide for a choice of conditions such as normalized or non-normalized arithmetic, signed operand or absolute value, and others.

The Boolean AND, exclusive OR, and inclusive OR commands are provided, along with a useful set of Storage Search instructions which include both complete-word and masked operations. The latter set, however, lacks the flexibility of searching within words and of optional incrementation, as can be done with similar instructions in the Control Data 3600 system.

Two instructions are included that specify the range of core storage locations available to a particular program. These instructions are used to load an upper and a lower "bounds" register with specific limiting values selected by the program. References to data outside these limits can be made, but no instruction can be taken from the out-of-bounds area. These registers can be used together to provide both upper and lower limits for a program, or only one can be used to specify a single (upper or lower) boundary.

The 3400 has an interrupt system that can be placed under control of the program. Three classes of interrupt are recognized:

- internal and peripheral operations,
- floating point instructions without the required hardware, and
- illegal operations.

Individual interrupt conditions can be honored or ignored as the program warrants. An interrupt is executed by transferring control to a fixed location, recording a return address, and initiating an interrupt routine lock-out that remains in effect until a return jump is executed. The programmer must include his own routines to select and handle each type of internal and peripheral interrupt condition.

Because of the hardware lockout feature of the interrupt system, care must be exercised to prevent the program from entering endless loops.

.13 Availability: . . . . not specified by manufacturer.

.14 First Delivery: . . November, 1964.

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.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point			
	Add-subtract:	automatic	binary	1 word.
	Multiply			
	Short:	none.		
	Long:	automatic	binary	2 words.
	Divide			
	No remainder:	none.		
	Remainder:	automatic	binary	2 words.
.212	Floating point			
	Add-subtract:	automatic*	binary	36 & 11 bits.
	Multiply:	automatic*	binary	36 & 11 bits.
	Divide:	automatic*	binary	36 & 11 bits.
.213	Boolean			
	AND:	automatic	binary	1 word.
	Inclusive OR:	automatic	binary	1 word.
	Exclusive OR:	automatic	binary	1 word.
.214	Comparison			
	Numbers:	yes		1 word or parts. **
	Absolute:	yes		1 word or parts. **
	Letters:	yes		1 word or parts. **
	Mixed:	yes, if both alphabetic and numeric data are in equivalent binary form.		1 word or parts. **

Collating sequence: 0-9, A-Z; for intervening special characters see Data Code Table, page 246:141.100.

* Optional.
** Partial comparisons can be performed, using one mask for both operands.

.215 Code translation: . . none.
.216 Radix conversion: . . none.
.217 Edit format: . . . . . own coding.
.218 Table look-up: . . . . table items up to 48 bits in size can be searched in contiguous words. The search may be for equal or greater than. Table look-up may be performed on whole words or (by masking) any part of the word. The specification of an index register is necessary; after each interrogation the index is decremented by 1.

.22 Special Cases of Operands

.221 Negative numbers: . . one's complement.
.222 Zero: . . . . positive or negative zero are treated as equal in arithmetic or "equal compare." In "threshold compare," the sequence is -1, -0, +0, +1.
.223 Operand size determination: . . . variable; may be described in 24-bit bytes or full 48-bit word.

.23 Instruction Formats

.231 Instruction structure: 24 or 48 bits.
.232 Instruction layout

23 – 18	17 – 15	14 – Bit 0
f	b or j	m, y, or k

24-bit instructions designated by three-letter mnemonics:

23 – 15	14 – Bit 0
f	y

f = 007

48-bit instructions designated by four-letter mnemonics:

47 – 39	38 – 24	23 – 21	20 – 18	17 – 15	14 – Bit 0
f	n	0	x	0	m

f = 74.0

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.233 Instruction parts

Designator	Name	Purpose
b	Index Register	specifies 1 of 6 index registers.
f	Function Code	a 6- or 9-bit code that specifies the operation to be performed.
j	Condition	conditions in jump and stop operations.
k	Unmodified Shift Count	number of shifts to be executed.
m	Unmodified Execution Address (Address One)	address of operand.
n	Address Two	usually used as a reject jump address.
x	Channel Number	specifies I/O channel, or channel for interrogation purposes.
y	Unmodified Operand	used in execution address portion of instruction; specifies that this address will be used as the operand.

.234 Basic address structure: . . . . . 1 + 0.

.235 Literals
Arithmetic: . . . . 15-bit address part is added to register A.

Incrementing modifiers: . . . . . 15-bit address part.

.236 Directly addressed operands
Internal storage type: core storage.
Minimum size: . . . . 48-bit word.

.237 Address indexing
.2371 Number of methods: 1.
.2374 Index specification: bits 15, 16, and 17 of instruction word.

.2375 Number of potential indexers: . . . . . 6.
.2376 Addresses which can be indexed: . . . . operand addresses, in arithmetic, logical, load, and store instructions.

.2377 Cumulative indexing: . . . . yes; using the Augment instruction, double indexing is possible. See Instruction List (Section 246:121).
.2378 Combined index and step: . . . . none.

.238 Indirect addressing
.2381 Recursive: . . . . . . yes.
.2382 Designation: . . . . . "7" configuration of the index register designator bits of the instruction. The new address is that of the lower instruction in the designated word.
.2383 Control: . . . . the last address in the recursive sequence specifies a direct address; i.e., other than a "7" index designator in the lower instruction of the word.
.2384 Indexing with indirect addressing . . . . . only the last address in the indirect address chain may be modified by indexing.

.239 Stepping
.2391 Specification of increment: . . . . . stepping instructions.
.2392 Increment sign: . . . minus or plus.
.2393 Size of increment: . . minus unity, plus unity, or plus 15-bit literal in stepping instruction.
.2394 End value: . . . . . . zero or equality.
.2395 Combined step and test: . . . . yes.

.24 Special Processor Storage

(See table at top of next page.)

.242 Category of storage: all registers listed in table.
Total number of locations: . . . . . . 15.
Physical form: . . . . circuitry
Access time, μsec: . 0.1
Cycle time, μsec: . . not applicable.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . 1.
.315 Sequence control step size: . . . . 1 word; i.e., moves by instruction pairs.
.316 Accessibility to routines: . . . . yes, by "Return Jump" instruction.
.317 Permanent or optional modifier: . . . . none.

.32 Look-Ahead: . . . . . none.

.33 Interruption

The programmer has control of the interrupt system of the 3400, since he can allow or disallow any or all types of interrupt conditions. Interrupts are classified as internal (computation errors), external (input-output device conditions), or illegal operation.

The internal and external interrupt conditions can cause an interrupt only when there is a corresponding "1" bit in the appropriate position of the Interrupt Mask register. The program must set each control bit by means of individual instructions. When an interrupt occurs, control is transferred to a fixed location and the cause of the interrupt must be determined. In the case of external interrupts, up to 12 different "status" indicators may need to be tested in order to isolate the specific interrupt condition.

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.24 Special Processor Storage

.241

Category of storage	Number of locations	Size in bits	Program Usage
A Register:	1	48	main accumulator.
Q Register:	1	48	second accumulator.
P Register:	1	15	increments instruction address after each step, or is replaced if a jump instruction is executed.
U Register:	1	48	contains instruction during execution.
Index Register:	6	15	
Interrupt Register:	1	48	interrupt conditions for I/O channels and internal conditions.
Interrupt Mask Register:	1	48	set mask to test interrupt indicators.
Product Register:	1	48	result of logical operation of interrupt mask.
Upper Bounds Register:	1	8	used to set upper limit of storage.
Lower Bounds Register:	1	8	used to set lower limit of storage

.331 Possible causes
- In-out units: . . . . . external unit conditions such as "ready", "end of file", or "abnormal end of operation." The exact meaning of these items is specified for each individual unit.
- In-out controllers: . . power off, missing, or non-functional.
- Program errors: . . . over-capacity shifts. fixed and floating point operands out of range. division by zero. illegal instruction. illegal reference to locked-out area of storage.
- Processor errors: . . parity error in operand or instruction.
- Other: . . . . console operator request. floating point instructions without the required hardware. real-time clock.

.332 Control by routine
- Individual control: . . each interrupt condition can be individually set.

.333 Operator control: . . . if program permits.

.334 Interruption conditions: interrupt system activated. specific interrupt approved by program. interrupt routine not in progress.

.335 Interruption process
- Registers saved: . . . sequence control register.
- Destination: . . . . . fixed location.

.336 Control methods
- Determine cause . . . 2 jumps and a subroutine are required to identify cause of interrupt or data channel concerned.
- Enable interruption: by program.

.34 Multi-Running: . . . . the interrupt facilities are sufficiently extensive to permit multirunning techniques; no control routines to provide for this type of operation have as yet been written.

.344 Program protection
- Storage: . . . . upper and lower "bounds" registers (see Description).

.35 Multi-Sequencing: . . . only with multiple processors connected by a CDC 3682 Satellite Coupler.

.4 PROCESSOR SPEEDS

.41 Instruction Times in μsecs

.411 Fixed point
- Add-subtract: 3.0
- Multiply: 17.6
- Divide: 17.6

.412 Floating point
- Add-subtract: 6.0*
- Multiply: 14.5*
- Divide: 14.5*

.413 Additional allowance for
- Indexing: . . . . none.
- Indirect addressing: . 1.5 average per indirect address.
- Re-complementing: . ?

.418 Shift: 3.0

* With optional floating point hardware.

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.42 Processor Performance in μsecs

.421 For random addresses	Fixed point	Floating point*
c = a + b:	9.0	12.0
b = a + b:	8.2	12.0
Sum N items: . . .	3.0N	6.0N
c = ab:	23.6	20.5
c = a/b:	23.6	20.5
.422 For arrays of data		
$c_i = a_i + b_j$:	15.0	18.0
$b_j = a_i + b_j$:	14.2	18.0
Sum N items: . . .	6.0N	9.0N
$c = c + a_i b_j$:	31.8	26.5

*With optional floating point hardware.

.423 Branch based on comparison
Numeric data: . . . 24.0
Alphabetic data: . . 24.0

.424 Switching
Unchecked: 12.0
Checked: 24.0
List search: . . . . 12.9 + 3.7 N

.425 Format control per character
Unpack: 12.0
Compose: 90.0

.426 Table look per comparison
For a match: . . . . } 2.2 N + 3.0 per word
For greatest: . . . } 2.2 N + 3.0 per word

.428 Moving: . . . . 6.0 per word.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	check	specific bit is set, and (optionally) interrupt occurs; interrupt system is deactivated, instruction address is stored, and forced jump is made to a specific location for each case.
Underflow:	check	(same)
Zero divisor:	check	(same)
Shift fault:	check	(same)
Out-of-bounds instruction:	check	(same)
Operand:	check	(same)
Invalid instruction:	check	(same)
Storage reference:	parity check	(same)
Receipt of data:	parity check	(same)
Internal reject:	parity check	(same)
Abnormal end of operation on connected I/O device:	check	(same)

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . 3401 Console.

.12 Associated Units: . . IBM 731 Selectric Typewriter.

.13 Description

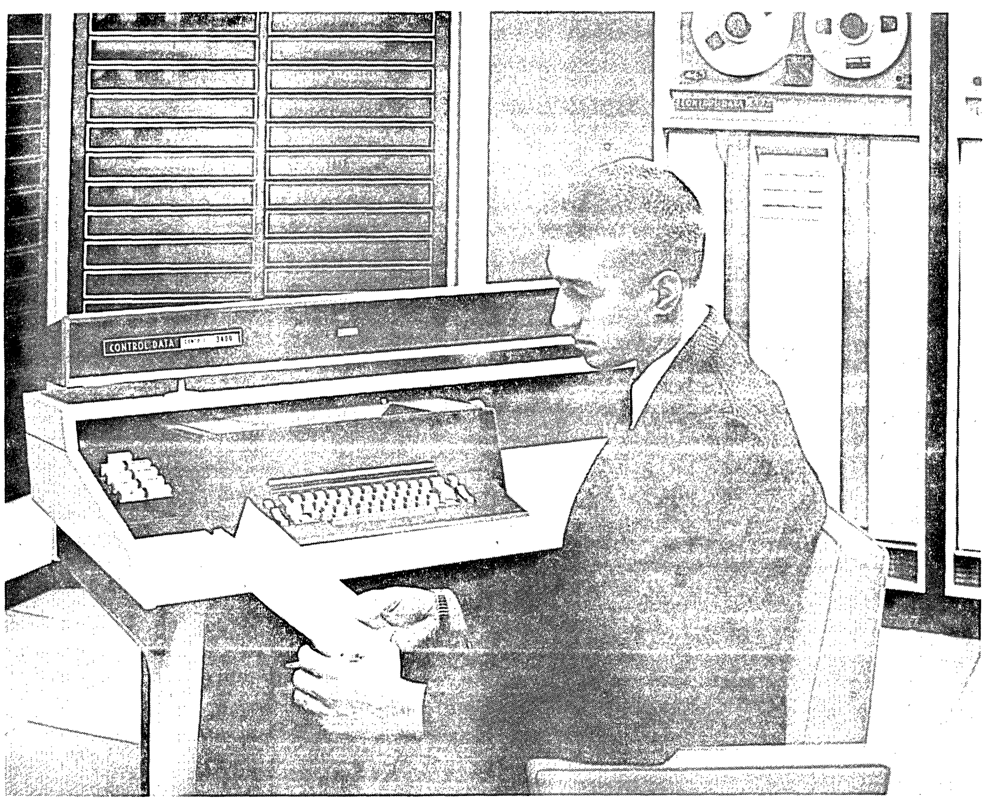
The console is a desk-type unit that includes an IBM 731 Selectric input-output typewriter as standard equipment. A group of 40 indicator lights and 8 switches enables the operator to determine normal and abnormal conditions during the running of a program. The lights indicate such conditions as channel activity, parity errors, and other faults. The following switches are available to the operator:

- Three program-testable select-jump switches — these can direct the action of the program to a particular program precedent.
- Auto-load button — loads bootstrap routines from standard peripheral device.

.13 Description (Contd.)

- Manual interrupt button — enables the programmer to make a manual alteration via the typewriter at any time, if the interrupt system is active.
- Restart button — stops operation and clears all peripheral interrupt activity; then causes a return jump to a specified location in order to restart operation.
- End of Record — sends end of record signal to I/O channel, which in turn terminates the input buffer.
- System Active On-Off switch — controls starting and stopping of system operation. On starting, a Master Clear operation is performed and a "running time" meter is activated. On stopping, any input-output operations will continue until normal termination.

The 3401 Console provides desk space and a good view, as shown in the photograph below.



INPUT–OUTPUT: 405 CARD READER

§ 071.

.1 GENERAL

.11 Identity: . . . . 405 Card Reader.
3248 Card Reader Controller.
3447 Card Reader Controller.
3649 Card Reader Controller.

.12 Description

The Control Data 405 Card Reader is a fast asynchronous unit that can read 80-column cards at a rated speed of 1,200 cards per minute. The cards are fed one at a time by a vacuum pickoff and transported by a series of pinch rollers. One of three different controllers (models 3248, 3447, and 3649) can be housed in the same cabinet with the 405 Reader. All controllers provide for automatic Hollerith code translation and checking operations, and the 3447 and 3649 have, in addition, an 80-character buffer storage unit. The 3649 unit has a second read control.

The card reader and controller are connected to the 3400 Processor through the 3406 standard 12-bit data channel. The extra read control on the 3649 allows two data channels to be physically connected to the controller, although only one channel can be used at a time. The buffer storage facility improves the system's overall simultaneity by providing a saving in the time that the reader data channel is occupied with card operations. Since up to four data channels can be connected to the processor, there can be a theoretical maximum of four card reader operations occurring in parallel with internal processing.

Reading is done by two sets of 12 photoelectric cells each, which read one column at a time. Each column can either be translated from Hollerith code or treated as a 12-bit binary image. The dual read station provides a comparison check, while a "light-dark" pre-read check helps to ensure correct card registration. Input and output bin capacities are each 4,000 cards. A secondary receiving (reject) bin has a capacity of 240 cards. Cards can be added to or removed from either the feeding or receiving bin while the reader is operating.

The card reader's demand on core storage is only about 0.1%.

INPUT–OUTPUT: CARD PUNCHES

§ 072.

.1 GENERAL

.11 Identity: . . . . CDC 415 Card Punch.
IBM 523 Card Punch.
3245 Card Punch Controller.
3446 Card Punch Controller.
3644 Card Punch Controller.

.12 Description

A Control Data 415 Card Punch or an IBM 523 Card Punch can be used in conjunction with any one of three controllers to provide a punched card output facility for the Control Data 3400 system. A summary of the general characteristics of this equipment is given below:

Card Punch:	415	523
Speed (80-column cards):	250 cpm	100 cpm
Card hopper capacity:	1,200 cards	800 cards
Punch method:	row-by-row	row-by-row

Card Punch Controller:	3245	3446	3644
Checking:	no	yes	yes.
Full card buffer:	no	yes	yes.
No. of write controls:	1	1	2.

.12 Description (Contd.)

The buffer storage facility of the 3446 and 3644 Controllers consists of a 12 by 80 matrix of magnetic cores which holds the data to punch one card. An output punch instruction can load the buffer storage on a 6-bit or 12-bit column-by-column basis, but the cards are always punched on a row-by-row basis. The 3644 also has two write controls, so that the card punch can be connected to either of two data channels.

Punching can be accomplished with or without automatic translation from binary coded decimal to Hollerith code. A binary mode is also available wherein the 12-bit binary image of one-half of a core storage location is punched in each card column. In either case, the relatively low data transfer rates of the punches result in negligible demands (less than 0.05%) on the core storage throughout the punch operation. Binary to decimal conversion operations require a programmed subroutine.

INPUT-OUTPUT: PAPER TAPE READER/PUNCH

§ 073.

.1 GENERAL

.11 Identity: . . . . 3691 Paper Tape Reader/ Punch.

.12 Description

The 3691 Paper Tape Reader/Punch is a free-standing unit housing a reader, punch and control circuitry for punched tape input and output. The reading unit is a Control Data 350 Paper Tape Reader, while the punch is the Teletype BRPE-11 Paper Tape Punch. The control circuitry is connected to one input-output channel of the 3400 system and is shared by both the reader and punch. Concurrent reading and punching operations are therefore not possible, but either a read or punch operation can proceed simultaneously with computing and other peripheral operations.

.12 Description (Contd.)

The reader operates at a peak speed of 350 characters per second using standard paper or plastic tape with fully punched holes. Reading is done by means of photoelectric cells and can take place either a character at a time or continuously, as determined by programmed instruction. Five-level, seven-level, and eight-level tape of standard width can be read. Conversion to the internal BCD character code, when necessary, must be accomplished by programming through the use of suitable translation tables. Conversion from BCD to binary requires the use of special subroutines.

The punch has a speed of 110 characters per second and, like the reader, can be programmed on a character-by-character or continuous basis. Only 7- or 8-level codes can be punched, but 5-level punching can be simulated by using special 7-level punching with blank columns. Regardless of program mode, the demand times on core storage are less than 0.06%, whether reading or punching.

INPUT-OUTPUT: 3253 LINE PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . 3253 Line Printer.

.12 Description

The 3253 Line Printer is an updated version of the older Model 166 Printer that is used with the Control Data 160 and 160-A Systems. It has been speeded up by doubling the revolution speed of the print drum, and it has also been re-engineered to eliminate certain troublesome aspects of 166 operation. The 3253 has a full-line buffer and uses a 64-character set. The print line is 120 characters wide, and a peak speed of 300 single-spaced lines per minute is attained when printing the entire character set. The printer and its buffer-controller are supplied as one unit, which is currently available for 40% of the cost of the faster 3655 High-Speed Printer described in the next report section (Section 246:082). The 3253 Printer is manufactured by the Holley Computer Products Company, and has the same general characteristics as those described in detail for the 160-A system (refer to Section 244:082).

The general method of handling input-output data transfers in the 3400 System results in a printer demand time on core storage of less than 0.01%.

INPUT–OUTPUT: 3655 PRINTER

§ 082

.1 GENERAL

.11 Identity: . . . . 3655 High Speed Printer.

.12 Description

The 3655 High Speed Printer is an adaptation of the older Model 1612 High Speed Printer that is used with the Control Data 1604 and 1604-A Systems. It has a full-line buffer and uses a 64-character set in a 120-column line. The maximum paper advance speed is 25 inches per second, and line advancing is controlled automatically by means of a pre-punched tape in the printer. The peak operating speed is 500 single-spaced lines per minute when using the entire character set. However, a speed of 1,000 lines per minute can be attained when using a restricted, 48-character "FORTRAN" character set. The 3655 Printer is manufactured

.12 Description (Contd.)

by the Anelex Corporation, and has the same general characteristics as those described in detail for the 1604-A System (refer to Section 243:081).

The general method of handling input-output data transfers in the 3400 system results in a printer demand time on core storage of 0.2% based upon the 1,000 line-per-minute rate.

The future of the 3655 Printer is doubtful in view of the introduction of the new CDC-built 501 Printer described in the following report section. The 501 unit prints a 136-character line and has a peak speed of 1,000 lines per minute. Current pricing information indicates that the 501 will normally be supplied with a dual-channel controller at about 33% higher cost than the 3655 Printer with its single-channel controller.

INPUT–OUTPUT: 501 HIGH–SPEED LINE PRINTER

§ 083.

.1 GENERAL

.11 Identity: . . . . 501 Printer.

.12 Description

The 501 Printer is a recently announced addition to Control Data's growing line of peripheral equipment. Its main characteristics are:

- A speed of 1,000 single-spaced lines per minute using a 45-character alphanumeric printing set (Synchronous operation).
- A speed of 800 single-spaced lines per minute using the full 64-character set (Asynchronous operation).
- A skipping speed of 25 inches per second for paper advancing.
- Single- or double-channel control. (Double-channel control, described below, allows a single unit to be used by two independent programs without interfering with each other's print-outs.)

.12 Description (Contd.)

- Format control by 8-channel plastic tape, with facilities for completing a page after the "paper low" signal.
- Separate interrupts based on printer availability, normal end of operation, and abnormal end of operation.
- A maximum central processor loading of about 0.2%.
- Paper advance before or after printing, under program control.

There are two available controllers — the 3256 and 3659 — which are, respectively, single- and double-channel controllers. In a double-channel controller, once one channel has reserved an input-output unit (in this case the printer), the unit will accept data only from that channel, and a special status code is returned in response to a request from the other channel.

Thus it is possible to have two programs sharing a single printer, perhaps printing in units of one page — not alternately or in some other fixed proportion, but as the situation requires, rather like a typist typing letters for two executives.

INPUT–OUTPUT: MAGNETIC TAPE UNITS

§ 091.

.1 GENERAL

.11 Identity: . . . . Magnetic Tape Units. CDC 604, 607.

.12 Description

The 604 and 607 Magnetic Tape Units are new additions to the Control Data line of tape units, and offer for the first time densities of 800 characters per inch (120 KC character rate) and the ability to read backward. These units use a standard reel and half-inch tape compatible with the earlier Control Data 603 and 606 Tape Units and with the IBM 727, 729 series, and 7330 Tape Units. The major difference between the 604 and 607 is in speed, as summarized in the following table:

Model	Tape speed, inches/sec.	Density, char/inch	Peak transfer rate, char/sec.
604:	75	200	15,000
		556	41,667
		800	60,000
607:	150	200	30,000
		556	83,400
		800	120,000

Information is recorded in variable-length blocks on 2,400-foot reels, and the data can be in either BCD or pure binary form. When used to store blocks of 1,000 characters, the capacity of each reel extends from 5 to 14.4 million characters depending on recording density. The interblock gap is 0.75 inch, and the overhead per block is 7 or 10 milliseconds, dependent on the model. Effective data transfer rates for each model are shown in the graphs at the end of this section.

A tape unit's demands on core storage can vary significantly depending upon the type of input-output instruction that is used and the data transfer rate. In terms of the percentage of core storage time required during the data transfer portion of a single tape operation, this demand extends from slightly less than 1% (at the 15 KC transfer rate of the 604 unit) to as high as 8.9% (at the 120 KC rate of the 607 unit). This demand is incurred for each unit operating.

Two single-channel tape controllers are available for use with either model of tape unit: the Model 3228 Controller handles up to four tape units, while Model 3229 can control up to eight tape units. Controller models 3421, 3422, and 3423 provide dual-channel access for four, six, and eight tape units, respectively. In addition, any of the 3600 series of tape controllers (3621 through 3626) can be used to provide two-, three-, or four-channel facilities with up to 8 or 16 tape units connected to each controller. A maximum of eight controllers can be connected to any one data channel in the 3200 system.

.12 Description (Contd.)

Operations on tape include: Read, Read Backward, Write, Write End of Record, Write File Mark, Search File Mark Forward or Backward, Backspace, Skip Bad Spot, Rewind, and Rewind-Unload. The tape control system allows for program interrupts to be generated upon occurrence of the following conditions:

- Ready and Not Busy
- End of Operation
- Abnormal End of Operation.

The data recorded on tape is checked in two ways:

- A lateral parity check is made upon each character and a longitudinal parity check is made upon each block.
- A read-after-write check using two-gap heads detects most recording errors at the time of occurrence. (This check is based on verifying correct parity in the recorded character, rather than on comparing it with the character code that should have been recorded.)

.13 Availability: . . . . ?

.14 First Delivery: . . . . . May, 1964.

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pneumatic capstan.
.212 Reservoirs
Number: . . . . 2.
Form: . . . . vacuum.
Capacity: . . . . each about 7 feet.
.213 Feed drive: . . . . motor.
.214 Take-up drive: . . . . . motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.
.222 Sensing system: . . . . . magnetic head.
.223 Common system: . . . . 2 heads.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . . erase.
Stacks: . . . . 1.

Use of station: . . . . . . recording.
Distance: . . . . 0.4375 inch after erase head.
Stacks: . . . . 1.
Heads/stack: . . . . . . 7.
Method of use: . . . . . 1 row at a time.

§ 091.

.24 Arrangement of Heads (contd.)

Use of station: . . . . . sensing.
Distance: . . . . 0.3 inch after recording head.
Stacks: . . . . 1.
Heads/stack: . . . . . . 7.
Method of use: . . . . . 1 row at a time.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . plastic tape with magnetizable surface.
.312 Phenomenon: . . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . 1 to N rows at 200, 556, or 800 rows/inch.
.322 Parallel by: . . . . 7 tracks.
.324 Track use
Data: . . . . 6.
Redundancy check: . . 1.
Timing: . . . . 0 (self clocking).
Control signals: . . . . 0.
Unused: . . . . 0.
Total: . . . . 7.
.325 Row use
Data: . . . . 1 to N.
Redundancy check: . . 1.
Timing: . . . . 0.
Control signals: . . . . 0 (record and segment marks are optional).
Unused: . . . . 0.
Cap: . . . . 0.75-inch interblock gap. 6.0-inch end-of-file mark.

.33 Coding: . . . . binary mode: 6 bits per row; even parity.
BCD mode: 1 tape row per character as in Data Code Table; even parity.

.34 Format Compatibility: with IBM BCD and binary codes at 200, 556, and 800 rows per inch.

.35 Physical Dimensions

.351 Overall width: . . . . . . 0.50 inch.
.352 Length: . . . . 2,400 feet per reel.

.4 CONTROLLER

A variety of controllers can be used, depending on whether 1, 2, 3, or 4 simultaneous data transmissions are required and whether up to 4, 8, or 16 tape units are to be connected to 1 controller. The maximum practical number of controllers is 32. The available controllers are listed in the Price Data section, 246:221.

.44 Data Transfer Control

.441 Size of load: . . . . 1 to N words, limited by available core storage.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . each word.
.444 Input-output area lockout: . . . . none.
.445 Table control: . . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . . 1 to N words, limited by available core storage; 1 row per character; 8 rows per word.
.512 Block demarcation
Input: . . . . gap on tape or cut-off specified in buffer control word.
Output: . . . . cut-off specified in buffer control word.

.52 Input-Output Operations

.521 Input: . . . . 1 block or file forward or backward, with cut-off available at N words.

.522 Output: . . . . 1 block forward of N words.

.523 Stepping: . . . . none.
.524 Skipping: . . . . 1 block or file forward or backward.
erase 6 inches forward (to skip defective tape areas).
.525 Marking: . . . . end-of-file mark, preceded by an automatic 6-inch gap, followed by a longitudinal parity character and the regular interblock gap.
.526 Searching: . . . . none.
.53 Code Translation: . . . automatic.
.54 Format Control: . . . . none.
.55 Control Operations
Disable: . . . . only by unload.
Request interrupt: . . . yes, either for error or when free.
Select format: . . . . . . no.
Select code: . . . . yes, binary mode or BCD mode.
Rewind: . . . . yes.
Unload: . . . . yes.
.56 Testable Conditions
Disabled: . . . . no.
Busy device: . . . . yes.
Output lock: . . . . yes.
Nearly exhausted: . . . yes, end-of-tape mark indicates a minimum of 8 feet remaining (approx. 20,000 char).
Busy controller: . . . . no.
End of medium marks: end-of-tape mark (reflective spot).
load point.
Ready to read: . . . . . . yes.
Ready to write: . . . . . yes.
Error condition: . . . . parity or length error separately.
Interrupt condition: . . whether selected to interrupt.

§ 091.

.6 PERFORMANCE (Model 604 Tape Unit; for 607 Tape Unit see below)

.61 Conditions: . . . . performance varies with recording density, as indicated below.

.62 Speeds (604 Unit only)

Density (char/inch):	800	556	200.
.621 Nominal or peak speed (char/sec):	60,000	41,667	15,000.
.622 Important parameters			
Name			
Tape speed (inches/sec):	75	75	75.
Density (char/inch):	800	556	200.
Start or stop time to/from full speed (msec):	2.75	2.75	2.75.
Start time until data transmission begins (msec):	8 avg.*	8 avg.*	8 avg.*
Gap crossing time without stopping (msec):	10	10	10.
Gap crossing time with stops (msec):	13	13	13.
Full rewind time (minutes):	1.3	1.3	1.3
Gap size (inch):	0.75	0.75	0.75

* varies according to conditions prevailing when instruction is issued.

.624 Effective speeds (char/sec):	60,000N/(N + 780)	41,667N/(N + 540)	15,000N/(N+195).

N is number of characters per block (also see Graph 246:091.900).

.63 Demands on System (604 Unit only)

Component	Density, char/inch	Msec per quarter-word	Percentage of data transfer time
Core Storage:	800	0.0015	4.5%
Core Storage:	556	0.0015	3.1%
Core Storage:	200	0.0015	1.1%

.6 PERFORMANCE (Model 607 Tape Unit; for 604 Tape Unit, see above)

.61 Conditions: . . . . performance varies with recording density, as indicated below.

.62 Speeds (607 Unit only)

Density (char/inch):	800	556	200.
.621 Nominal or peak speed (char/sec):	120,000	83,400	30,000.
.622 Important parameters			
Name			
Density (char/inch):	800	556	200.
Tape speed (inches/sec):	150	150	150.
Start or stop time to/from full speed (msec):	2.75	2.75	2.75.
Start time until data transmission begins (msec.):	3.7 avg.*	3.7 avg.*	3.7 avg.*
Gap crossing time without stopping (msec.):	5.0	5.0	5.0
Gap crossing time with stops (msec):	7.25	7.25	7.25
Full rewind time (minutes):	1.3	1.3	1.3
Gap size (inch):	0.75	0.75	0.75

* varies according to conditions prevailing when instruction is issued.

.623 Overhead (msec/block):	7.25	7.25	7.25
.624 Effective speeds (char/sec):	120,000N/(N+870)	83,400N/(N+605)	30,000N/(N+217).

N is number of characters per block (also see Graph 246:091.901).

.63 Demands on System (607 Unit only)

Component	Density, char/inch	msec per quarter-word	Percentage of data transfer time
Core storage:	800	0.0015	8.9%
Core storage:	556	0.0015	6.2%
Core storage:	200	0.0015	2.3%

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . recording density.
Method: . . . . switch.
Comment: . . . . selects density.

.72 Other Controls

Function	Form	Comment
Unit Number Selector:	dual	selects 1 of 8 addresses.
File protection ring:	plastic ring affixed to tape reel	absence of ring inhibits tape writing.
Load Point:	button	lowers tape into reservoirs and winds tape forward to load point.
Unload:	button	removes tape from reservoirs and raises upper portion of head assembly.

§ 091.

.73 Loading and Unloading

.731 Volumes handled

Storage: . . . . reel of 2,400 feet.

Capacity (for 1,000-character blocks): . 5,000,000 characters at 200 char/inch, 11,300,000 characters at 556 char/inch; 14,400,000 characters at 800 char/inch.

.732 Replenishment time: . . 1.0 to 1.5 minutes; tape unit needs to be stopped.

.734 Optimum reloading period

Model 604: . . . . 6 minutes.

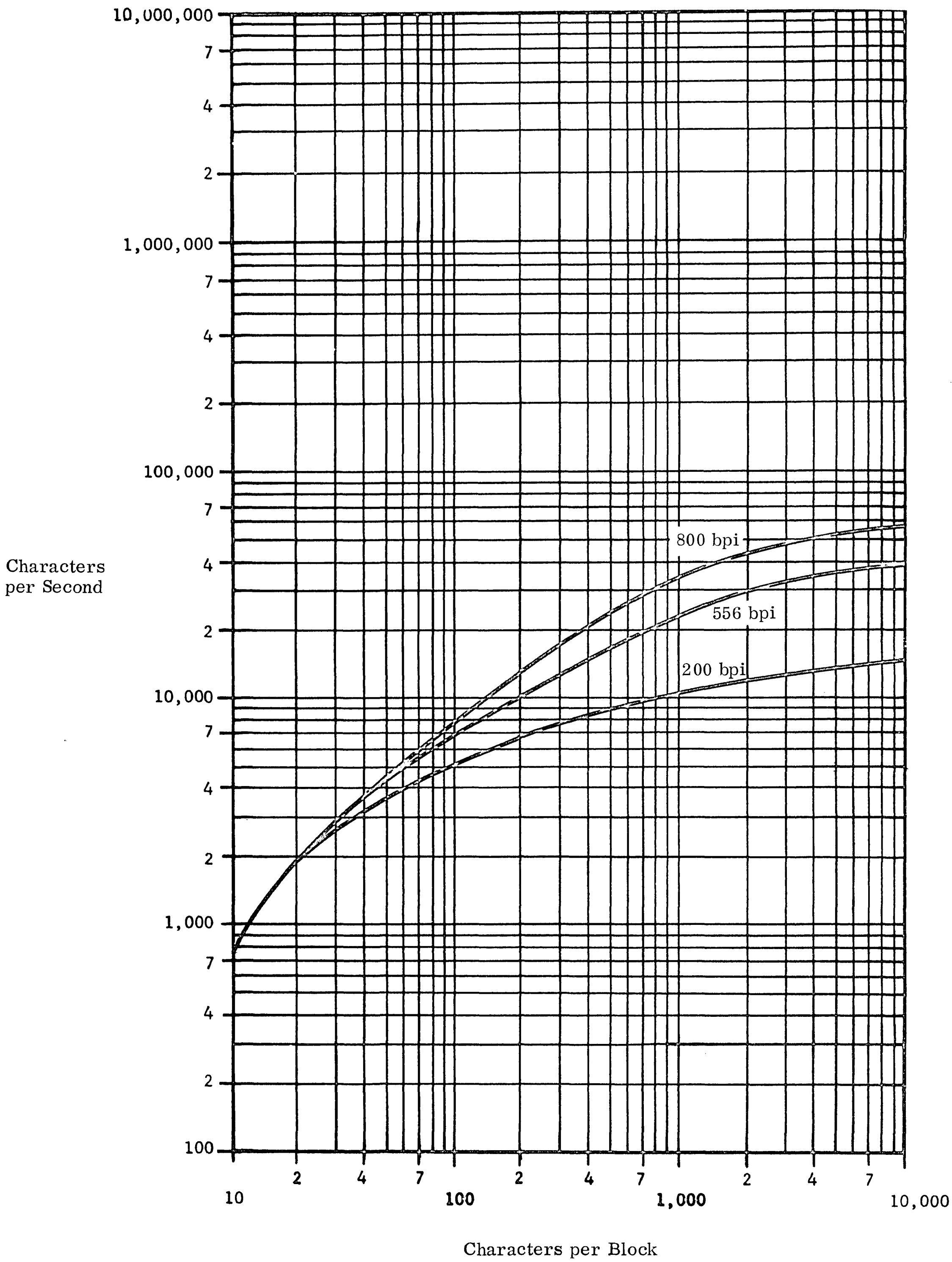
Model 607: . . . . 3 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read after write with lateral parity check	interrupt.
Reading:	lateral and longitudinal parity checks	interrupt.
Input area overflow:	buffer control word specifies cut-off.	stop transfer.
Invalid code:	check	interrupt.
Exhausted medium:	reflective spot on tape	interrupt.
Imperfect medium:	none.	
Timing conflicts:	none.	

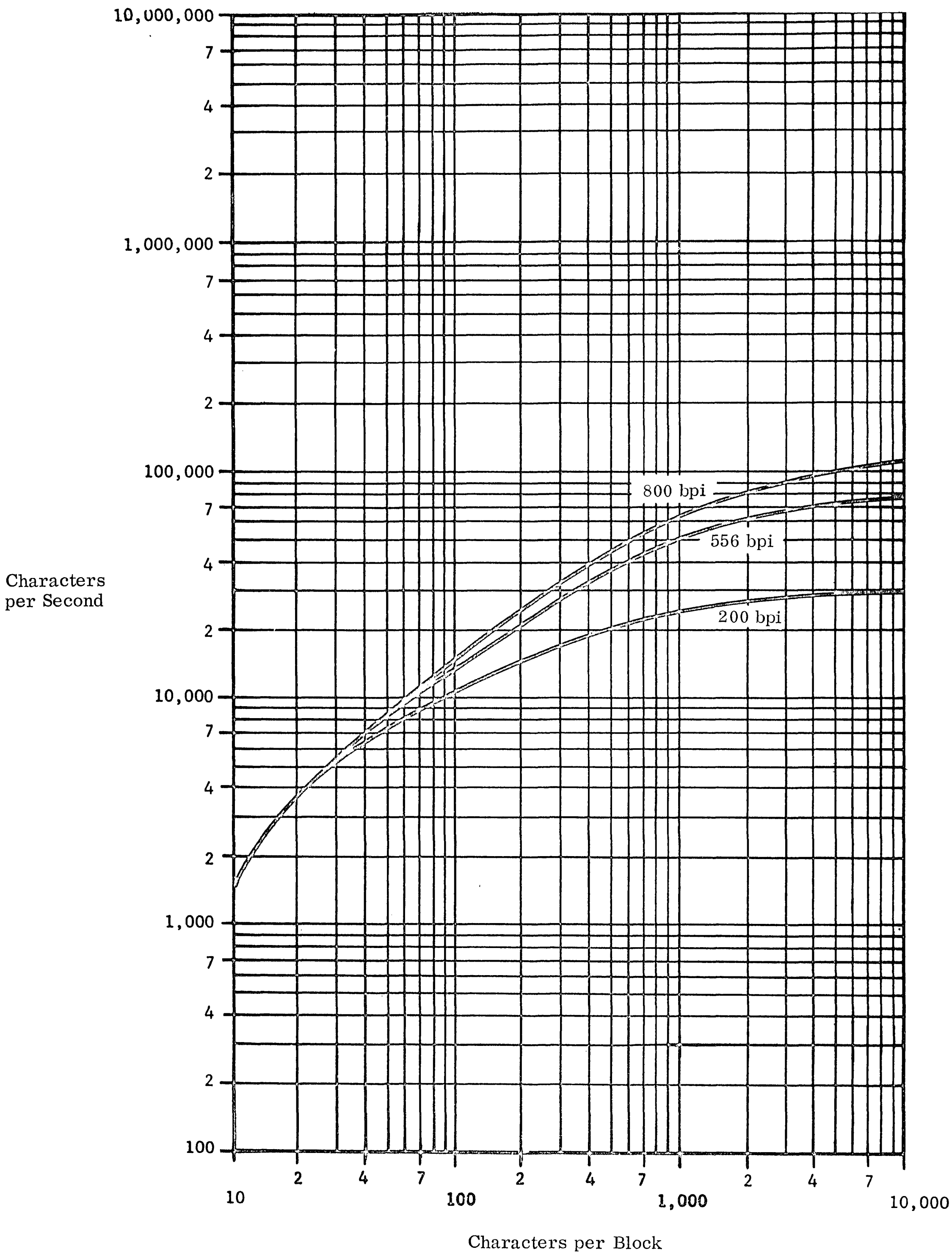
§ 091.

EFFECTIVE SPEED: 604 MAGNETIC TAPE UNIT
(with stops between blocks)



§ 091.

EFFECTIVE SPEED: 607 MAGNETIC TAPE UNIT
(with stops between blocks)



AUERBACH

INPUT–OUTPUT: SATELLITE COUPLER

§ 101.

.1 GENERAL

.11 Identity: . . . . 3682 Satellite Coupler.
3681 Data Channel Converter.

.12 Description

The 3682 Satellite Coupler is used to allow a computer system to communicate directly with another, physically adjacent system. The basic technique involved is that an input-output channel is used, and request and control signals from computer system A to computer system B are received in the same way as the equivalent status signals from any input-output unit. When the appropriate signals have passed, an input-output instruction will transfer data directly from one computer to the other computer memory at a speed limited only by the memory cycle timing of the slower computer.*

This arrangement will usually be used to connect a large computer to a smaller one. Three examples

* The transmission rate of data leaving the 3400 system is 1.3 million characters per second utilizing the standard 3406 Data Channel. With the special channels available, this rate could be doubled or quadrupled, but it may still be limited by the receiving system.

.12 Description (Contd.)

of such connections are illustrated below. The Control Data 3400 could utilize a Satellite Coupler to connect:

- A 3400 to a smaller system (Control Data 160 or 3200);
- Two 3400 systems together;
- A 3400 system to a larger system (Control Data 3600 or 6600);
- Several like or unlike systems, to form a "ring" of interconnected computer systems. (System "A" could be connected to system "B" and "Z"; system "B" to system "C" and "A", etc.).

The programming systems required for the control of all but the simplest cases of these multi-computer configurations may well be complex. In general, their design is the responsibility of the installation itself, since at the present time it is unusual to find two installations with the same needs.

If one of the interconnected computer systems is the Control Data 160-A, a 3681 Data Channel Converter is required in addition to the 3682. The differentiation between the 3681 and 3682 is that the 3681 simulates the appropriate 3000 series data channel, while the 3682 (which is made up of two identical elements acting as buffers between the two systems) buffers and controls the data transmissions themselves.

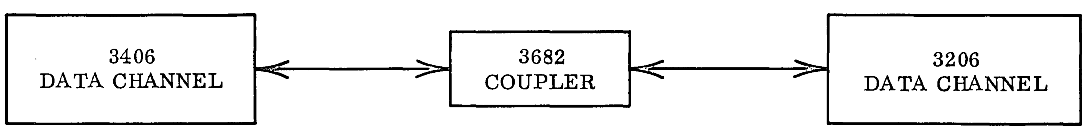


Fig. 1: Coupling of a Control Data 3400 system to a 3200 system.

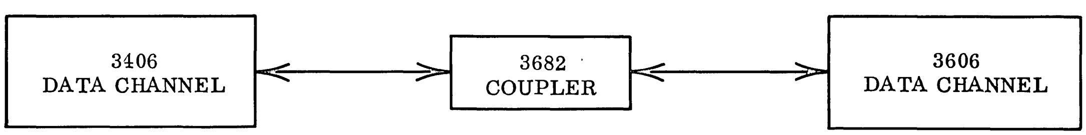


Fig. 2: Coupling of a Control Data 3400 system to a 3600 system.

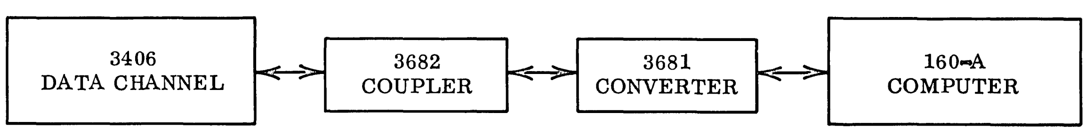


Fig. 3: Coupling of a Control Data 3400 system to a 160-A system.

SIMULTANEOUS OPERATIONS

§ 111.

.1 GENERAL

The Control Data 3400 system allows for the connection of up to four input-output data channels. Each data channel is serviced by a bi-directional, 12-bit parallel interface unit called the 3406 Standard Input/Output Channel.* Up to eight different peripheral equipment controllers can be connected to one 3406. These facilities make it possible for up to four input-output operations on any of 32 different controllers to proceed simultaneously with computation.

A choice of single- and dual-channel controllers is available for the card and printer equipment. Full line buffers are included with each of the printer controllers, but card buffers are optional depending upon the choice of card reader or card punch controller. The magnetic tape units, paper tape units, and typewriter simply have 12-bit interfaces.

Magnetic tape controllers can be selected from among 10 different units that provide from 1 to 4 channel accesses, and which are capable of controlling from 1 to 16 tape transports. Thus, if enough data channels are available, from one to four tapes on each controller can be operational in any combination, in addition to non-magnetic-tape peripherals and the processor.

All Disk File controllers are dual-channel devices that permit any two of the three disc operations of reading, writing, or positioning to be overlapped with other operations.

The input-output operations allow 12-, 24-, or 48-bit transfers.** Each input-output transfer is initiated after a series of instructions which connect the desired channel, test for "busy" or other status conditions in the input-output equipment, and select the desired function. The input-output transfer instruction (a full 48-bit word instruction) is then issued to start the transfer.

After the starting address and word count for the transfer are fetched from memory and stored in special registers in the input-output channel, the main program is released from further control of the input-output operation. For each transfer, the 3406 Communication Channel issues a data transfer request to the input-output equipment, and the data transfer is made between storage and the data channel. The starting address is incremented, the word count is decremented, and the entire transfer sequence is repeated until the transfer count becomes equal to zero. An automatic interrupt can be specified to notify the program immediately upon completion of the transfer.

The delay to the program caused by the core storage accesses required by any particular input-output unit is 1.5 microseconds per 12-bit byte. The percentage of core storage time required by individual peripheral operations is listed in the table below:

* For special applications, either a 24-bit (Model 3407) or 48-bit (Model 3408) data channel can be used, but at least one channel must be reserved for the standard 3406 12-bit unit.

** 24-bit transfers are only possible with a 3407 channel, and 48-bit transfers with a 3408 channel.

§ 111.

.1 GENERAL (Contd.)

Peripheral Operation	Transfer of 12-bit Bytes
607 Tape Unit	
120,000 char/sec:	8.9%
83,400 char/sec:	6.2%
30,000 char/sec:	2.3%
604 Tape Unit	
60,000 char/sec:	4.5%
41,667 char/sec:	3.1%
15,000 char/sec:	1.1%
Line Printer, 1000 lpm:	0.2%
Line Printer, 300 lpm:	0.04%
Card Reader, 1,200 cpm:	0.1%
Card Punch, 250 cpm:	0.03%
Paper Tape Reader or Punch:	0.06%

Core Storage Demands (%)

.2 RULES

The following processes can take place simultaneously:

- One computation; plus
- As many buffered input-output operations* as there are buffers (up to about 50); plus
- As many non-buffered input-output operations** as there are data channels (a maximum of 4 channels); plus
- As many "non-supervised" peripheral operations*** as there are appropriate units.

* The present printers are always buffered; card equipment is optionally buffered.

** Paper tape, magnetic tape, and random access disc operations are non-buffered; the number of such operations may also be restricted by the manner in which the controllers are connected to the data channels.

*** Magnetic tape rewinding and Search File Mark are the only presently defined "non-supervised" operations.

INSTRUCTION LIST

§ 121.

SYMBOLS

k = Address portion of instruction	b = Designator for index register
K = k + (B^b), Modified shift count	j = Designator for 22, 23, 75, 76
m = Address portion of instruction	# = Restrict instruction to upper
M = m + (B^b), Modified operand address	' = Complemented
y = Address portion of instruction	( ) = Contents of
Y = y + (B^b), Modified operand	NI = Next instruction
* = 48-bit instruction	+ = Floating point option

FULL WORD DATA TRANSMISSION

LDA	12	Load A	(M)→A
LAC	13	Load A complement	(M)→' A
STA	20	Store A	(A)→M
LDQ	16	Load Q	(M)→Q
LQC	17	Load Q complement	(M)→' Q
STQ	21	Store Q	(Q)→M

PARTIAL WORD DATA TRANSMISSION

*	LDC	63	Load character ($Byte_{0-7}$)→A_{05-00} (63 b v0006 50 0 m)
*	STC	63	Store character (A_{05-00})→$Byte_{0-7}$ (63 b v0006 50 5 m)
	SAU	60	Substitute address upper (A_{14-00})→M_{UA}
	SAL	61	Substitute address lower (A_{14-00})→M_{LA}

INTER-REGISTER TRANSMISSION

IAQ	00	Interchange A and Q (A)→Q, (Q)→A (00 7 00554)
ATI	00	Transmit A to index (A_{14-00})→B^b (00 7 4054b)

SHIFTING

ARS	01	Shift (A) right by K
QRS	02	Shift (Q) right by K
LRS	03	Shift (AQ) right by K
ALS	05	Shift (A) left by K
QLS	06	Shift (Q) left by K
LLS	07	Shift (AQ) left by K

INDEXING

ENI	50	Enter index	y→B^b
INI	51	Increase index	y + (B^b)→B^b
LIU	52	Load index upper	(m_{UA})→B^b
LIL	53	Load index lower	(m_{LA})→B^b
SIU	56	Store index upper	(B^b)→m_{UA}
SIL	57	Store index lower	(B^b)→m_{LA}
ISK #	54	Index skip: (B^b) ≠ y: (B^b) + 1→B^b, continue; (B^b) = y: 0→B^b, skip lower instruction	
IJP	55	Index jump: (B^b) ≠ 0: (B^b) − 1→B^b, jump to m; (B^b) = 0: continue	

ARITHMETIC

FIXED POINT

ADD	14	Add to A	(A) + (M)→A
SUB	15	Subtract from A	(A) − (M)→A
MUI	24	Multiply integer	(M) (A)→QA
DVI	25	Divide integer	(QA) / (M)→A, rem Q
RAD	70	Replace add	[(M) + (A)]→M & A
RSB	71	Replace subtract	[(M) − (A)]→M & A
RAO	72	Replace add one	[(M) + 1]→M & A
RSO	73	Replace sub. one	[(M) − 1]→M & A
SCA	34	Scale A	Shift (A) left until $A_{47} \neq A_{46}$ or k = 0; (k − no. of shifts)→B^b
SCQ	35	Scale AQ	Shift (AQ) left until $A_{47} \neq A_{46}$ or k = 0; (k − no. of shifts)→B^b

FLOATING POINT

+	FAD	30	Floating add.	[(A) + (M)]→A
+	FSB	31	Floating sub.	[(A) − (M)]→A
+	FMU	32	Floating mult.	(A) (M)→A
+	FDV	33	Floating div.	(A) / (M)→A

Reproduced from Control Data 3400 Preliminary Reference Manual, Appendix D.

§ 121.

LOGICAL

SST 40 Selective set
Set (A_n) to 1 for (M_n) = 1
SCL 41 Selective clear
Clear (A_n) to 0 for (M_n) = 1
SCM 42 Selective complement
Complement (A_n) for (M_n) = 1
SSU 43 Selective substitute
(M_n) ⟶ A_n for (Q_n) = 1
LDL 44 Load Logical L (Q) (M) ⟶ A
ADL 45 Add logical [(A) + L (A) (M)] ⟶ A
SBL 46 Sub. logical [(A) − L (Q) (M)] ⟶ A
STL 47 Store logical L (Q) (A) ⟶ M

INPUT/OUTPUT

* CONN 74.0 Connect
* EXTF 74.1 Function
* BEGR 74.2 Read
* BEGW 74.3 Write
* COPY 74.4 Copy status
* CLCH 74.5 Clear channel
* CCWD 74.6 Change control word

NO MEMORY REFERENCE

ENQ 04 Enter Q Extend sign Y, Y ⟶ Q
ENA 10 Enter A Extend sign Y, Y ⟶ A
INA 11 Increase A Extend sign Y,
Y + (A) ⟶ A
EUB 77.5 Enter upper bound
ELB 77.6 Enter lower bound

GENERAL

INF 77.0 Internal function
AUG 77.1 Augment
CIS 77.2 Copy interrupt status
SEN 77.3 Internal sense
CPR 77.4 Copy product register

MEMORY TEST

SSK# 36 Storage skip (M) neg: skip lower instruction; (M) pos: continue
SSH# 37 Storage shift (M) neg: skip lower instruction, left 1; (M) pos: continue, left 1
EQS# 64 Search (B^b) words, if (M − 1), or (M − 2), etc. = (A) skip lower instruction; ≠ A, continue
THS# 65 Search (B^b) words, if (M − 1), or (M − 2), etc. > (A) skip lower instruction; ≦ A, continue
MEQ# 66 Search (B^b) words, if L (Q) (M − 1), or (M − 2), etc. = (A) skip lower instruction; ≠ A, continue
MTH# 67 Search (B^b) words, if L (Q) (M − 1), or (M − 2), etc. > (A) skip lower instruction; ≦ A, continue

A AND Q TEST

AJP 22 Jump to m on condition j
QJP 23 Jump to m on condition j

SELECTIVE JUMP AND STOP

SLJ 75 Jump to m on condition j
SLS 76 Stop on j, and jump to m

j	22	23	75	76
0	(A) = 0: Jump	(Q) = 0: Jump	Jump	Stop: Jump
1	(A) ≠ 0: Jump	(Q) ≠ 0: Jump	Key 1: Jump	Key 1: Stop: Jump
2	(A) Pos: Jump	(Q) Pos: Jump	Key 2: Jump	Key 2: Stop: Jump
3	(A) Neg: Jump	(Q) Neg: Jump	Key 3: Jump	Key 3: Stop: Jump
4	(A) = 0: Ret. Jump	(Q) = 0: Ret. Jump	Ret. Jump	Stop: Ret. Jump
5	(A) ≠ 0: Ret. Jump	(Q) ≠ 0: Ret. Jump	Key 1: Ret. Jump	Key 1: Stop: Ret. Jump
6	(A) Pos: Ret. Jump	(Q) Pos: Ret. Jump	Key 2: Ret. Jump	Key 2: Stop: Ret. Jump
7	(A) Neg: Ret. Jump	(Q) Neg: Ret. Jump	Key 3: Ret. Jump	Key 3: Stop: Ret. Jump

DATA CODE TABLE

§ 141.

Internal BCD Code*	Character	Card	Internal BCD Code*	Character	Card
00	0	0	40	(minus)	11
01	1	1	41	J	11, 1
02	2	2	42	K	11, 2
03	3	3	43	L	11, 3
04	4	4	44	M	11, 4
05	5	5	45	N	11, 5
06	6	6	46	O	11, 6
07	7	7	47	P	11, 7
10	8	8	50	Q	11, 8
11	9	9	51	R	11, 9
12		8, 2	52	-0	11, 0
13	=	8, 3	53	$	11, 8, 3
14	(dash)	8, 4	54	*	11, 8, 4
15		8, 5	55		11, 8, 5
16		8, 6	56		11, 8, 6
17		8, 7	57		11, 8, 7
20	+	12	60	(Space)	Blank
21	A	12, 1	61	/	0, 1
22	B	12, 2	62	S	0, 2
23	C	12, 3	63	T	0, 3
24	D	12, 4	64	U	0, 4
25	E	12, 5	65	V	0, 5
26	F	12, 6	66	W	0, 6
27	G	12, 7	67	X	0, 7
30	H	12, 8	70	Y	0, 8
31	I	12, 9	71	Z	0, 9
32	+0	12, 0	72		0, 8, 2
33	.	12, 8, 3	73	,	0, 8, 3
34	)	12, 8, 4	74	(	0, 8, 4
35		12, 8, 5	75		0, 8, 5
36		12, 8, 6	76		0, 8, 6
37		12, 8, 7	77		0, 8, 7

*Octal representation of 6-bit BCD codes shown.

PROCESS ORIENTED LANGUAGE: 3400 FORTRAN

§ 162.

.1 GENERAL

.11 Identity: . . . . 3400 FORTRAN.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . 3400 FORTRAN General Information Manual, Pub. No. 555.

.14 Description

The 3400 FORTRAN language incorporates nearly all the features of FORTRAN IV and a number of improvements. Among the added features allowed in 3400 FORTRAN are:

- More than one entry point per subprogram, implemented by the ENTRY statement, which identifies alternate entry points in a function or subroutine subprogram.
- Use of mixed mode arithmetic.
- Multiple arithmetic replacement statements, e.g.:

  A = B = C = D = X + Y

  which causes the variables A through D to be replaced by the value of the expression X + Y.
- Use of the masking (Boolean) operators .NOT., .AND., and .OR. on 48-bit arrays.
- Buffering of all input-output operations by use of the BUFFER IN and BUFFER OUT statements.
- Use of subscripted subscripts. For example, the FORTRAN IV statements:

  L = J(K)
  M = I(L)
  C = D(M)

  can be expressed by the following single statement in 3400 FORTRAN:

  C = D(I(J(K))).
- Use of arithmetic expressions in subscripts; e.g., B(B*K*SINF(J)). The form of all subscripts must agree with the standard FORTRAN forms.
- ENCODE and DECODE statements, which permit transfer of data from one location in memory to another. The data is converted according to FORMAT statements and stored in an array or list of variables.

.14 Description (Contd.)

- Eight modes of arithmetic. The five modes offered in FORTRAN IV — INTEGER, REAL (single precision floating point), DOUBLE PRECISION floating point, COMPLEX, and LOGICAL — are standard; the remaining three types are arbitrary and must be defined by the programmer. The user must specify the variable involved in a TYPE declaration and insert library routines which execute the cues generated by the compiler.
- A multi-branch status statement

  IF (UNIT, u) n_1, n_2, n_3, n_4

  which causes the program to jump to statement n_i upon detection of the following conditions of input-output device u:

  n_1 - not ready;
  n_2 - ready and no previous error;
  n_3 - EOF sensed on last input operation;
  n_4 - parity error on last input operation.

The input-output statements of FORTRAN II have been retained in addition to those of FORTRAN IV. As in FORTRAN II, source statements are used instead of library calls to test for sense light, overflow, sense switch, and divide check or fault conditions.

The degree of compatibility of 3400 FORTRAN with Control Data FORTRAN-62, 3600 FORTRAN, and 3200 FORTRAN can be summarized as follows:

- All 3400 FORTRAN programs are acceptable to the 3600 FORTRAN compiler.
- 3200 FORTRAN programs can be compiled by the 3400 FORTRAN compiler if the type CHARACTER is not used and if the library routines are replaced by source statements in certain cases.
- FORTRAN-62 can be made compatible with 3400 FORTRAN by changing Boolean statements, FORMAT statements, arithmetic checks, Hollerith constants, and subroutines as required to meet the 3400 FORTRAN definitions.

The 3400 FORTRAN compiler consists of a translator and an assembler (COMPASS). The translator reads the source program from an input tape, and the translator and assembler communicate with each other via lists which may be recorded on a scratch tape. Each FORTRAN subprogram is compiled independently, and the object program output consists of binary card images on magnetic tape.

§ 162.

.14 Description (Contd.)

The compiler operates in conjunction with the 3400 SCOPE monitor system, and the object programs generated by the compiler are designed for execution under SCOPE control.

The following lists represent a tabulated comparison of 3400 FORTRAN with the IBM 7090/7094 FORTRAN IV language, as described in Section 408:162.

Restrictions upon 3400 FORTRAN

(1) The ALOG10 (real common logarithm) function is not currently available.

(2) Hollerith constants cannot exceed 120 characters in 3400 FORTRAN; in FORTRAN IV, the maximum length is 132 characters.

(3) The logical constants .TRUE. and .FALSE. of FORTRAN IV are represented by 1 and 0 in 3400 FORTRAN.

(4) The FORTRAN IV form DATA i_1/value list/, i_2/value list/... must be changed to DATA (i_1 = value list), (i_2 = value list) for 3400 FORTRAN.

(5) The subprograms EXIT (terminate job execution), DUMP (dump core storage and then terminate job execution), and PDUMP (dump core storage and then continue execution) are not provided.

(6) The statements calling subroutines BLOCK DATA, SLITE, SLITET, SSWTCH, OVERFL, and DVCHK of FORTRAN IV must be replaced by source statements in 3400 FORTRAN.

(7) The END statement is used to mark the physical end of a subprogram in 3400 FORTRAN. It also acts as a RETURN as the last statement in a subroutine (the RETURN statement can be omitted in this case). In FORTRAN IV, the END statement is used only to terminate a compilation.

Extensions of 3400 FORTRAN

(1) Names may be up to 8 characters in length.

(2) Integer constants can have a maximum value of $2^{47} - 1$ and can be up to 15 digits in size; floating point constants can range from 10^{-308} to 10^{+308} and can be up to 11 digits in size for real constants and 25 digits for double precision constants; Boolean constants can be up to 16 octal digits (48 bits) in size.

(3) BUFFER IN and BUFFER OUT initiate the buffered reading or writing of one block on magnetic tape from sequential core storage locations, beginning and ending with specified variables.

(4) ENCODE and DECODE control code or radix conversions and packing into or unpacking from sequential locations of a list of variables (usually those involved in a buffered input or output operation).

(5) Conditional statements may be of the type IF (e) n_1, n_2, where e is a logical expression. A branch to statement n_1 is executed if e is true, or to n_2 if e is false. (Both 3400 FORTRAN and FORTRAN IV have the statement IF (e)s, which causes a branch to statement s if logical expression e is true; if e is false, the next sequential statement is executed.)

(6) Multiple replacement statements (e.g., A = B = C = D = X + Y) store the value of the expression on the right in each of the variables appearing on the left, with type conversion if necessary.

(7) Up to eight type declarations can be used to specify the mode of the associated variables. Five types are standard, and an additional three can be defined by the programmer in the "TYPE namet (e) list" statement. Modes can be mixed in arithmetic expressions. The mode of an expression corresponds to the highest order of any operand type within the expression. The order of the standard types from highest to lowest is:

COMPLEX
DOUBLE
REAL
INTEGER
LOGICAL.

(8) The ENTRY statement designates an entry point other than the first executable statement in a subprogram.

(9) The PROGRAM statement is the first statement in the main program.

(10) Subscripts may be arithmetic expressions or subscripted subscripts.

(11) The operators .AND., .OR., and .NOT. can be used for masking operations upon two 48-bit operands, thus providing the Boolean capacity of FORTRAN II.

(12) If a type LOGICAL variable is dimensioned, up to 32 bits will be stored in a single word. If the variable is not dimensioned, each bit will be assigned a separate word location in storage.

(13) Statement numbers can range from 1 to 99999.

(14) Status checking statements — IF(EOF, u) n_1, n_2; IF (IO CHECK, u) n_1, n_2; and IF (UNIT, u) n_1, n_2, n_3, n_4 — check for end-of-file, parity errors, and ready conditions.

(15) A LENGTHF (i) function returns the number of words read during the last input operation on unit i.

(16) The statement IF EXPONENT FAULT n_1, n_2 checks for exponent overflow.

§ 162.

.14 Description (Contd.)

(17) No parenthesized list of statement numbers is required in an assigned GO TO statement.

(18) The character "$" can be used as a statement separator, permitting more than one source statement to be written on a line.

(19) The COMMON statement can designate two types of common block storage — labeled and numbered (or blank). Data can be prestored in labeled common areas by means of the DATA statement.

(20) In FORMAT statements, the following added types of conversions are permitted: logical conversion (Lw); alphanumeric conversion right justified in storage with zero fill (Rw); and complex conversion (C(Zw.d, Zw.d), where Z may be either E or F conversion).

MACHINE ORIENTED LANGUAGE: 3400 COMPASS

§ 171.

.1 GENERAL

.11 Identity: . . . . 3400 COMPASS.

.12 Reference: . . . . 3400 COMPASS General Reference Manual.

.13 Description

COMPASS is the basic assembly language of the CDC 3400 system and is used with the SCOPE operating system. This language includes all the machine code instructions. COMPASS allows for source language changes to already assembled programs, and for system, installation, or programmer-provided macro instructions. Programmer-provided macros may be included in the library. Communication between different subprograms and library subroutines is provided by use of COMMON blocks and the EXTernal pseudo-operation. Communication with the operating system is by way of the system macros.

There are COMPASS assembly languages for the Control Data 3200, 3400, and 3600 systems. While they are based on a common pattern, there is no overall compatibility between the three languages. Upward compatibility does exist, in normal circumstances, between 3400 COMPASS and 3600 COMPASS.

Use of COMPASS eliminates the need for the programmer to take care of complex format requirements of many of the CDC 3400 instructions. In particular, the many modifications which are available in the use of the AUGMENT instructions can now be contained within the augmented instruction instead of being written separately.

There are three types of macro codes. These are 3400 System macros (provided with the CDC system itself), Library macros (provided by the installation), and programmer-provided macros (provided within the program itself). These macros are normally written in COMPASS language and are inserted into the assembled coding each time they are called. However, some control is included by providing two pseudo-operations IFN, and IFZ. During assembly, these operations are used to test the value of one parameter or expression against another to determine whether or not to insert the next "n" instructions of the macro coding.

.13 Description (Contd.)

Closed subroutines may be called into a program by the use of the EXTERNAL function. These are only incorporated into the program once.

The assembly language performs two roles: first it allows a programmer to write machine instructions and constants in a conventional form: and second, it provides a systematic means of using any library, monitor, or subroutines as desired.

Labeling is unusually free. Address symbols are normally one letter with an option of being followed by up to seven further alphameric characters for all labels. Three other types (+, -, and all numeric symbols) serve other functions.

There are two types of data areas; both are called "COMMON" areas. These are differentiated in the language by having alphameric (called "Labeled COMMON") or numeric (called "Numbered COMMON") labels, and in usage by being able to preset the contents of the areas at load time only if "Labeled COMMON" is used.

Communication with other independently written routines is arranged by the ENTRY points and the EXTernal symbol linkage. These operations provide for a label to be common to more than one routine. The actual linkage is created at loading time.

The assembly program for the CDC 3400 is designed to accept, as input, cards or card images containing symbolic 3400 programming instructions. It translates the symbolic instructions into 3400 machine language programs in relocatable binary, for loading into any portion of memory at run time. The assembler will produce as output any combination of:

- Output listing of the assembled program.
- Relocatable binary card output for subsequent loading and execution of the assembled program.
- Relocatable binary card images on an "assemble and run" tape for immediate loading and execution of the assembled program.
- Compressed symbolic output deck to be used as input for subsequent modification and reassembly.

§ 171.

.2 LANGUAGE FORMAT

.21 Diagram: . . . . same as for 3600 COMPASS; see Page 247:171.100.

.22 Legend

Operation Code Field: . . . . This field holds any of the CDC 3400 mnemonic instruction codes with modifiers, an octal integer 00-77, the name of a macro instruction, or any of the pseudo instructions. If a modifier is used, it must be separated from the operation code by a comma: no blank columns may intervene.

Address Field: . . . . The address field begins anywhere after the blank which terminates the operation field (but before column 41) and ends at the first blank column. It may have one or more subfields, depending upon the instruction. Subfields, which are separated by commas on the coding form, specify the following:

- m word address
- y operand
- b index register
- x shift count
- mandatory location symbol
- v second index register

Comments Field: . . . Comments may be included with any instruction. They are separated from the last character in the address field by a blank and they may extend to column 72. Comments do not affect assembly, but will be included on the output listing.

Sequence Number Field: . . . . Columns 73-80 may be used for sequence numbers or for program identification. This field has no effect upon assembly, but is checked for proper sequencing during the assembly process.

.23 Corrections: . . . . . . three pseudo instructions, DELETE, REPLACE, and INSERT, are available which operate on a condensed (COSY) deck.

.24 Special Conventions

.241 Compound addresses: . . . . . e.g., SYMBOL + 5.
.242 Multi-addresses: . . none.
.243 Literals: . . . . 8 to 16 characters, depending on the code.
.244 Special coded addresses: . . . . . * means this address.
** means 77777_8.
± forces an instruction into the upper or lower half of a word.

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . 1,500.
.312 Common label formation rule: . . 1 to 8 alphamerics including certain special characters. Blanks are not required. First character must be alphabetic.
.313 Reserved labels: . . none.
.315 Designators: . . . . . none.
.316 Synonyms: . . . . . . yes, via EQUivalence pseudo-op.

.32 Universal Labels: none, but individual labels can be made universal to several independent subprograms, being called an External Table Entry to each subprogram.

.33 Local Labels

.331 Labels for procedures
Existence: . . . . . optional.
Formation rule
First character:. alphabetic character (A-Z).
Others: . . . . . . A-Z, 0-9, or period.
Number of characters: . . . 1 to 8.
.332 Labels for library routines: . . . . . . same as for procedures.
.333 Labels for constants: . . . . . same as for procedures.
.334 Labels for files: . . none.
.335 Labels for records: . . . . . . none.
.336 Labels for variables: . . . . . same as for procedures.
.337 Labels for other subprograms: . . . same as for procedures.
.338 Others
Labels for blocks containing preset data
Existence: . . . . optional.
Formation rule: . 1 to 8 alphabetics; "Labeled Common Blocks."
Labels for reserved blocks for working storage
Existence: . . . . . optional.
Formation rule: . 8 numeric or blank characters; an all blank label is acceptable; "Numbered Common Blocks."
Labels for arrays: same as for procedures.

§ 171.

.4 DATA

.41 Constants

.411 Maximum size constants

Machine Form	External Form
Decimal integer:	decimal integer, with optional scaling factor expressed in binary or decimal.
Fixed numeric:	not allowed.
Floating numeric:	decimal integer or fraction with scaling factor.

.412 Maximum size literals
Integer
Decimal: . . . . . . 14 digits.
Octal: . . . . 16 octal digits.
Fixed numeric: . . . not allowed.
Floating numeric: $10^{\pm 308}$.
Alphameric: . . . . . 8 characters.

.42 Working Areas

.421 Data layout
Implied by use: . . . no.
Specified in program: . . . . . . VFD (Variable Field Definition), BLOCK and COMMON statements.
.422 Data type: . . . . implied by use.
.423 Redefinition: . . . . . . use of BLOCK statements.

.43 Input-Output Areas: . specified in program.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
Existence: . . . . . . optional with absolutes.
Number: . . . . 96.
Example: . . . . FDV; Floating Divide.
Comment: . . . . where one op code has more than one type of operation, mnemonic modifiers are written after the operation code; thus, FDV, MG, UR would indicate that the magnitude of the addressed operand be used, and that the operation should be unrounded.
.512 Absolute
Existence: . . . . . . optional with mnemonic.
Number: . . . . 64.
Example: . . . . 45 for Add Logical.

.52 Macro-Codes: . . . . yes, as provided by system installation in the library, or by programmer at head of the program.

.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control
Allocation counter: . . . . . various pseudo-ops.
Label adjustment: . various pseudo-ops.
Annotation: . . . . . Remarks.
.542 Allocation counter
Set to absolute: . . no (ORGR relocatable pseudo-op entry in location).
Set to label: . . . . yes.
Set relative to label: . . . . yes.
Step forward: . . . implied by "set relative to label."
Step backward: . . . implied.
Reserve area: . . . yes.

.543 Label adjustment
Set labels equal: . yes.
Set label relative: . yes.
Set absolute value: yes.
Clear label table: . not within single subprogram; yes, by dividing into separate subprograms.
.544 Annotation
Comment phrase: yes.
Title phrase: . . . . no.
.545 Other
Allocation mode: . absolute or relocatable.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: none.

.62 Special Functions

.621 Facilities: . . . . . none; any could be added in installation library.
.622 Method of call: . . . LIBM names the library macro-operations at the start of the program.
The use of a declared macro name in the operation field of the coding sheet calls the actual macro.

.63 Overlay Control: . . . handled by operating system.

.64 Data Editing

.641 Radix conversion: . . decimal-to-binary for initial constants.
Code translation: . alphabetic-to-BCD, typewriter.
.642 Format control: . . . none.

.65 Input-Output Control: . . . . . . own program, with I/O pseudo-op check on I/O units involved.

.66 Sorting: . . . . none.

.67 Diagnostics: . . . . . none can be specified by the programmer for use at running time.

§ 171.

.7 LIBRARY FACILITIES

.71 Identity: . . . . installation library.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master:. . yes.

.73 Storage Form: . . . . magnetic tape.

.74 Varieties of Contents: . . . . as determined by installation.

.75 Mechanism

.751 Insertion of new item: . . . . via SCOPE Monitor.
.752 Language of new item: . . . . open.
.753 Method of call: . . . . operation code identifies routine.
ENTRY identifies entry point.
Operating Manual lists special calls.

.76 Insertion in Program

.761 Open routines exist: yes.
.762 Closed routines exist: . . . . yes.
.763 Open-closed is optional: . . . . yes.
.764 Closed routines appear once: . . . . yes.

.8 INSTRUCTION CODE REPERTOIRE

.81 Macros: . . . . as provided by installation library.

.82 Pseudos (Extracted from Control Data 3400 Computer System COMPASS General Information Manual)

BCD: . . . . insert BCD characters.
BES: . . . . reserve block of storage.
BLOCK: . . . . specify block of common.
BSS: . . . . reserve block of storage.
CALL: . . . . enter subprogram
COMMON: . . . . declare array in common.

.82 Pseudo (Contd.)

COSY: . . . . COSY identification. *
DELETE: . . . . delete portions of program.
INSERT: . . . . insert portions of program.
REPLACE: . . . . . . replace portions of program.
DEC: . . . . insert decimal integer constants.
EJECT: . . . . eject a page on output listing.
END: . . . . specify end of subprogram.
ENDIF: . . . . terminate an IF or IFT statement.
ENDM: . . . . terminate a macro definition.
ENTRY: . . . . define entry point.
EQU: . . . . equate undefined symbol to defined symbol.
EXIT: . . . . exit to monitor.
EXT: . . . . define external symbol.
IDENT: . . . . identify subprogram name.
IF: . . . . conditional assembly — numeric.
IFT: . . . . conditional assembly for macros — literal.
IOTR: . . . . insert input-output transmission control word.
LIBM: . . . . library macros.
LIST: . . . . resume output listing.
MACRO: . . . . definition of macro instruction.
NOLIST: . . . . supress output listing.
NOP: . . . . inserts a do-nothing operation code.
OCT: . . . . insert octal constant.
ORGR: . . . . set location counter.
REM: . . . . insert remarks.
SCOPE: . . . . return to SCOPE control.
SPACE: . . . . insert spaces in output listing.
TYPE: . . . . insert typewriter code.

*COSY is the name given to an optional compressed reproduction of the symbolic source program which, in turn, may be used as input for subsequent assemblies.

.84 Direct: . . . . All instructions in the instruction repertoire have been given mnemonic names and are allowable in the COMPASS language. These mnemonic names are listed in the Instruction List (Section 246:121).

OPERATING ENVIRONMENT: 3400 SCOPE

§ 191.

.1 GENERAL

.11 Identity: . . . . 3400 SCOPE.

.12 Description

3400 SCOPE is an operating system that allows a group of programs to be run sequentially — one program at a time — on a Control Data 3400 computer.

During the running of a program, the operating system occupies the lower portion of core storage; the actual amount of storage utilized depends upon the routines called in. Normally SCOPE's demand on central processor time will be negligible.

The three basic languages (3400 FORTRAN, 3400 COBOL, and 3400 COMPASS) all use SCOPE during both the testing and production stages. For efficient operation of SCOPE with these translations, a 4-tape system with 32,768 core storage locations is required.

.12 Description (Contd.)

Like all operating systems, 3400 SCOPE provides a number of services to the various people involved. Some of these services naturally restrict the freedom of these involved by predetermining methods of operation which may or may not be the best ones possible under the existing circumstances. Other services involve giving up areas of storage, the use of specific peripherals, etc., and to this extent it can be said that they may have a "cost" involved.

In the following tables the facilities provided by 3400 SCOPE are listed as looked at from various points of view — those of the FORTRAN or COBOL programmer, the assembly language programmer, the user (i.e., the person who uses a "canned" program he may not have written), the computer room operator, and the data processing manager. All these individuals have different points of view, but all have a vital interest in maximizing the overall effectiveness of the computer system.

For the COBOL & FORTRAN Programmer	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
During Writing:	Snapshot facilities in assembly language (191.5).	Debug facilities in source language (191.5). Trace facilities in assembly language (191.5).	Storage space is needed for these facilities.
During Testing:	Standard Recovery Dump option.		

§ 191.

For the Assembly Language Programmer	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
During Writing:	Input-output routines and radix conversions (191.2). Segmentation control system (191.3).		Standard routines must be used.
During Testing:	Snapshot facilities (191.5). Automatic dumps on abnormal operation (191.4).	Restart procedure (191.45). Trace facilities (191.5).	

For the "Canned Program" User	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
During Normal Running:	Allocation of peripherals (191.3).	Automatic servo swap facilities or printouts (191.32). Time-shared operation with other programs (191.4).	Standard I/O routines and radix conversion routines must be used. Restricted simultaneity for some peripherals.
	Overlay facilities (191.3).	Automatic segmentation (191.3).	Segments must be predefined.
During and After Abnormal Running:	Automatic dump procedure (4 types) (191.45).	Setting up of restart points. Automatic restart facilities. Standard interrupt processing routines (SCOPE simply directs the interrupt to a programmer-provided routine) (191.4).	

§ 191.

For the Computer Room Operator	SCOPE Provides	SCOPE Does Not Provide	Resultant Restrictions
During Normal Running:	Standard Procedures for input-output unit allocation. Type-outs for loading and unloading tape. Run-to-run supervision Amendment of running order (191.6).	Re-run ability (191.4).	
During and After Abnormal Running:	Automatic dump procedure (4 types).	Setting up of restart points. Automatic restart facilities.	
For the Data Processing Manager	**SCOPE Provides**	**SCOPE Does Not Provide**	**Resultant Restrictions**
All circumstances:	Accounting records (191.7).		

.14 Originator: . . . . . . Control Data Corporation

.15 Maintainer: . . . . . . Control Data Corporation.

.16 First Use: . . . . November, 1964

.2 PROGRAM LOADING

.21 Source of Programs

.211 Programs from on-line libraries: . . . . the SCOPE library tapes (which can be created as desired) can contain any collection of translators, subroutines and other data or programs. These may be incorporated at load time or during a run.

.212 Independent programs: loaded from card reader or tape unit with a control card.

.213 Data: . . . . any available type of input device, as specified in the program. (The data for a program is frequently loaded immediately behind the program itself.)

.214 Master routines: . . . the SCOPE routines are held on all library tapes, together with bootstrap routines to bring them into memory.

.22 Library Subroutines: can be called at load time or during a run from a library tape.

.23 Loading Sequence: . . control card; subroutines for this run in any order (these are stored on a magnetic tape unit if necessary); data for this run if desired; further runs; ending with an End of Job control card.

Normally jobs are loaded and executed sequentially as physically placed on the input unit; however, the operator has emergency facilities to override this sequence.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . object programs, written as subprograms, can be divided into overlays defined by the programmer, and moved as needed into memory.

§ 191.

.312 Occupation of working storage: . . . . all addresses are relocated during loading. Once loaded, no further change is made.

.32 Input-Output Units

.321 Initial assignment: . . . performed by SCOPE, using equipment availability table and logical unit definition.
.322 Alternation: . . . . automatic, by SCOPE.
.323 Reassignment: . . . . . manual alteration of equipment availability table, followed by SCOPE operation.

.4 RUNNING SUPERVSION

.41 Simultaneous Working: controlled by the programmer's own coding; each input-output request is accepted or rejected depending upon the immediate availability of an appropriate input-output channel

.42 Multi-Programming: no provision.

.43 Multi-Sequencing: . . . no provision.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Allocation impossible:	check by loader	flagged during loading.
In-out error-single:	check by input/output control	status information list for progrmmer.
In-out error-persistent:	check by input/output control	status information list for progrmmer.
Invalid instructions:	check	transfer to specific programmer coding.
Underflow:	check	transfer to specific programmer coding.
Invalid operation:	check	transfer to specific programmer coding.
Improper format:	check by loader	error routine called in.
Invalid address:	check	transfer to specific programmer coding.
Reference to forbidden area:	check	transfer to specific programmer coding.

.45 Restarts

.451 Establishing restart points: . . . . recovery dumps are written when a job is abandoned. No facility is available to automatically set up restart points ahead of time.
.452 Restart process: . . . own coding.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . no provision.
.512 Snapshots: . . . . SNAP is a SCOPE control statement which prints the contents of a single core location.
.52 Post Mortem: . . . . . . a recovery dump can be written.

.6 OPERATOR CONTROL

.61 Signals to Operator

.611 Decision required by operator: . . . . . . own coding.
.612 Action required by operator: . . . . print-out on output comment medium.
.613 Reporting progress of run: . . . . print-out on output comment medium (normally console typewriter).

.62 Operator's Decisions: console typewriter.

.63 Operator's Signals

.631 Inquiry: . . . . manual interrupt buttom on console.
.632 Change of normal progress: . . . . SCOPE statements via console typewriter.

.7 LOGGING

.71 Operator Signals: . . . console typewriter.

.72 Operator Decisions: . . console typewriter.

.73 Run Progress: . . . . . console typewriter.

.74 Errors: . . . . errors which will cause job termination are logged on the console.

.75 Running Times: . . . . . console typewriter and, optionally, the accounting medium.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . 1 3402 computer module.
1 3401 console with typewriter.
1 3409 storage module.
1 3447 Card Reader controller with 405 Card Reader.

§ 191.

.811 Minimum Configuration (Contd.): 1 3655 line printer.
1 3406 bidirectional data channel.
1 magnetic tape control (dual channel).
4 magnetic tape units.

.812 Usable extra facilities: additional tapes, I/O channels, and I/O equipment.

.813 Reserved equipment: . the System Units (see below) are not available to the programmer except for the specified purposes. However, it is not necessary to use or assign all system units, and more than one system unit function can be allocated to a single physical unit.

System Units include the following:
Standard Input,
Standard Output,
SCOPE Libraries,
System Scratch Record,
Standard Load and Go.

.82 System Overhead

.821 Loading time: . . . . . . under 1 minute.

.822 Reloading frequency:. . only if the SCOPE resident routines have been overwritten. Normally this is not done.

.83 Program Space Available: . . . . storage requirements for the resident 3400 SCOPE routines are not available to date.

.84 Program Loading Time: . . . . under 1 minute.

.85 Program Performance essentially unaffected during normal production runs, since SCOPE merely directs run-to-run changeovers.

SYSTEM PERFORMANCE

§ 201.

GENERALIZED FILE PROCESSING (246:201.100)

These problems involve updating a master file from transaction data in a detail file and producing a printed record of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

The graphs for Standard File Problems A, B, C, and D show the total time required for each Control Data 3400 standard configuration shown in Section 246:031 to process 10,000 master file records. For Configurations VIIB and VIIIB, where all four input-output files are on magnetic tape, total times are shown for both unblocked and blocked records in the detail and report files. Central processor time is essentially the same for all configurations.

In integrated Configurations VI and VIIA, in which the detail file is read by the card reader and the report file is produced by the on-line printer, the printer is the controlling factor on total time required over most of the detail activity range. The central processor is occupied for only a small fraction of the total processing time. In most of the cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, a processing run with all files on magnetic tape, and a tape-to-card transcription of the report file. The curves for paired Configuration VIIB show that the time required for the all-tape main processing run is tape limited. This is also true for Configuration VIIIB, even though faster magnetic tape units are used. The card-to-tape and tape-to-printer transactions will run at card reader and printer-limited speeds, and their demands on the processor will be small.

The master file record format is a mixture of alphameric and binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. (Even so, most of the central processor time is devoted to editing and radix conversion operations, using programmed non-standard subroutines.) A moderate degree of packing led to a record length of 18 Control Data 3400 words.

SORTING (246:201.200)

The standard estimates for sorting 80-character records by straightforward merging on magnetic tape (Graph 246:201.214) were developed from the processing times for Standard File Problem A according to the method explained in the Users' Guide, Paragraph 4:200.213.

MATRIX INVERSION (246:201.300)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplication ($c = c + a_i b_j$) in single-precision floating point (see Paragraph 246:051.422).

GENERALIZED MATHEMATICAL PROCESSING (246:201.400)

This problem measures over-all system performance on a simple mathematical application that involves widely varying ratios of input-to-computation-to-output volume, as described in Section 4:200.4 of the Users' Guide. As in the File Processing problem, the total elapsed time is shown for both unblocked and blocked input and output files.

All computations are performed in single-precision floating point. In Configurations VI and VIIA, input is via the on-line card reader and output is via the on-line printer. If card-to-tape and tape-to-printer transcriptions are carried out in separate runs, the time required for the all-tape main processing run can be read from the curves for paired Configuration VIIB. Configuration VIIIB utilizes high-speed tapes.

GENERALIZED STATISTICAL PROCESSING (246:201.500)

This problem measures overall system performance on a common statistical application: the development of cross-tabulation tables, as in the analysis of the results of a survey. The problem is defined in Section 4:200.5 of the Users' Guide, and the performance of the Control Data 3400 is shown in Graph 246:201.514.

§ 201.

WORKSHEET DATA TABLE 1							
WORKSHEET	ITEM		CONFIGURATION				REFERENCE
			VI, VIIA	VIIB (Blocked Files 3 & 4)	VIIIB	VIIIB (Blocked Files 3 & 4)	
1	Char/block	(File 1)	1,024	1,024	1,024	1,024	
	Records/block	K (File 1)	8	8	8	8	
	msec/block	File 1 = File 2	27	27	14	14	
		File 3	50	24*	6	12*	
Input-Output Times		File 4	98	24*	6	12*	
	msec/switch	File 1 = File 2	0.01	0.01	0.01	0.01	4:200.112
		File 3	0.01	0.01	0.01	0.01	
		File 4	0.01	0.01	0.01	0.01	
	msec penalty	File 1 = File 2	0.26	0.26	0.26	0.26	
		File 3	0.02	0.24*	0.02	0.24*	
		File 4	0.03	0.24*	0.03	0.24*	
2	msec/block	a_1	0.119	0.119	0.119	0.119	
	msec/record	a_2	0.167	0.167	0.167	0.167	
Central Processor Times	msec/detail	b6	1.410	1.410	1.410	1.410	4:200.1132
	msec/work	b5 + b9	0.230	0.230	0.230	0.230	
	msec/report	b7 + b8	1.092	1.092	1.092	1.092	
3	msec/block for C.P.	a_1	0.12	0.12	0.12	0.12	
		a_2 K	1.36	1.36	1.36	1.36	
Standard Problem A		a_3 K	21.88	21.88	21.88	21.88	4:200.114
		File 1 Master In	0.26	0.26	0.26	0.26	
F = 1.0		File 2 Master Out	0.26	0.26	0.26	0.26	
		File 3 Details	0.16	0.16	0.16	0.16	
		File 4 Reports	0.24	0.24	0.24	0.24	
		Total	24.28	24.28	24.28	24.28	
4	Unit of measure	(48-bit word)					
		Std. routines	2,048	2,048	2,048	2,048	
		Fixed					
Standard Problem A Space		3 (Blocks 1 to 23)	189	189	189	189	4:200.1151
		6 (Blocks 24 to 48)	2,424	2,424	2,424	2,424	
		Files	762	762	762	762	
		Working	200	200	200	200	
		Total	5,623	5,623	5,623	5,623	

* 12 records per block in File 3; 8 in File 4.

§ 201.

WORKSHEET DATA TABLE 2

WORKSHEET	ITEM			CONFIGURATION: VI, VIIA	CONFIGURATION: VIIB	CONFIGURATION: VIIIB	REFERENCE
5	Fixed/Floating point			Floating	Floating	Floating	
	Unit name	input		Card Reader	604 MTU	607 MTU	
		output		Line Printer	604 MTU	607 MTU	
	Size of record	input		80 digits	80 digits	80 digits	
Standard Mathematical		output		80 digits	80 digits	80 digits	
	msec/block	input	T_1	50	unblocked 12; blocked 4	unblocked 6; blocked 2	4:200.413
		output	T_2	65	unblocked 12; blocked 4	unblocked 6; blocked 2	
Problem A	msec penalty	input	T_3	2	2	2	
		output	T_4	3	2	2	
	msec/record		T_5	2.86	2.86	2.86	
	msec/5 loops		T_6	1.80	1.80	1.80	
	msec/report		T_7	2.90	2.90	2.90	
7	Unit name			604 MTU		607 MTU	
	Size of block			604 MTU		607 MTU	
Standard Statistical	Records/block		B	16		16	
	msec/block		T_1	26		13	
	msec penalty		T_3	.06/block		.06/block	
Problem A	C. P.	msec/block	T_5	.016		.016	4:200.512
		msec/record	T_6	.007		.007	
		msec/table	T_7	.049		.049	

SYSTEM PERFORMANCE

§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

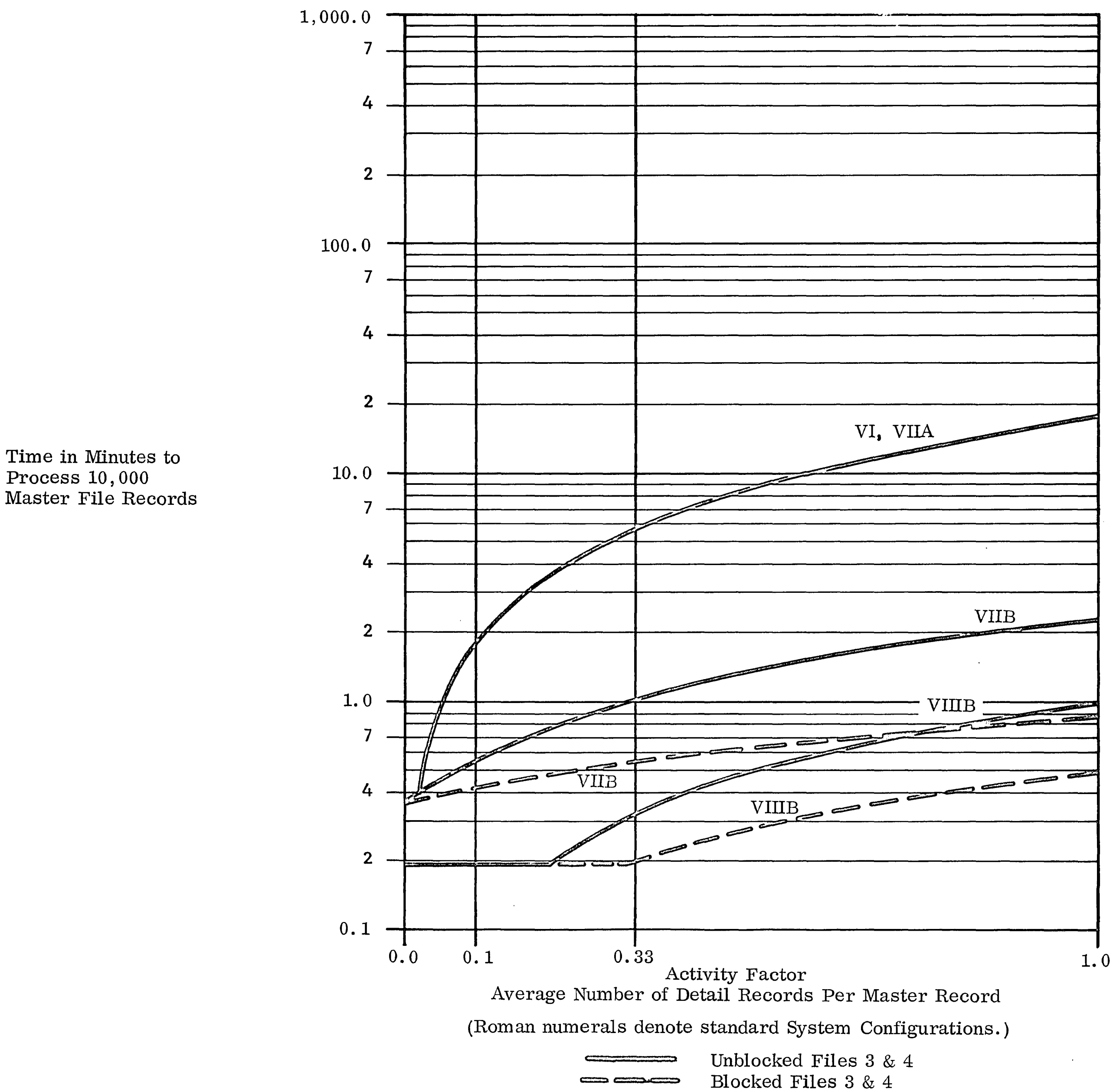
.111 Record Sizes
Master file: . . . . . . 108 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.112 Computation: . . . . standard.

.113 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . see graph below.

.115 Storage space required: . . . . 5,623 words.



(Roman numerals denote standard System Configurations.)

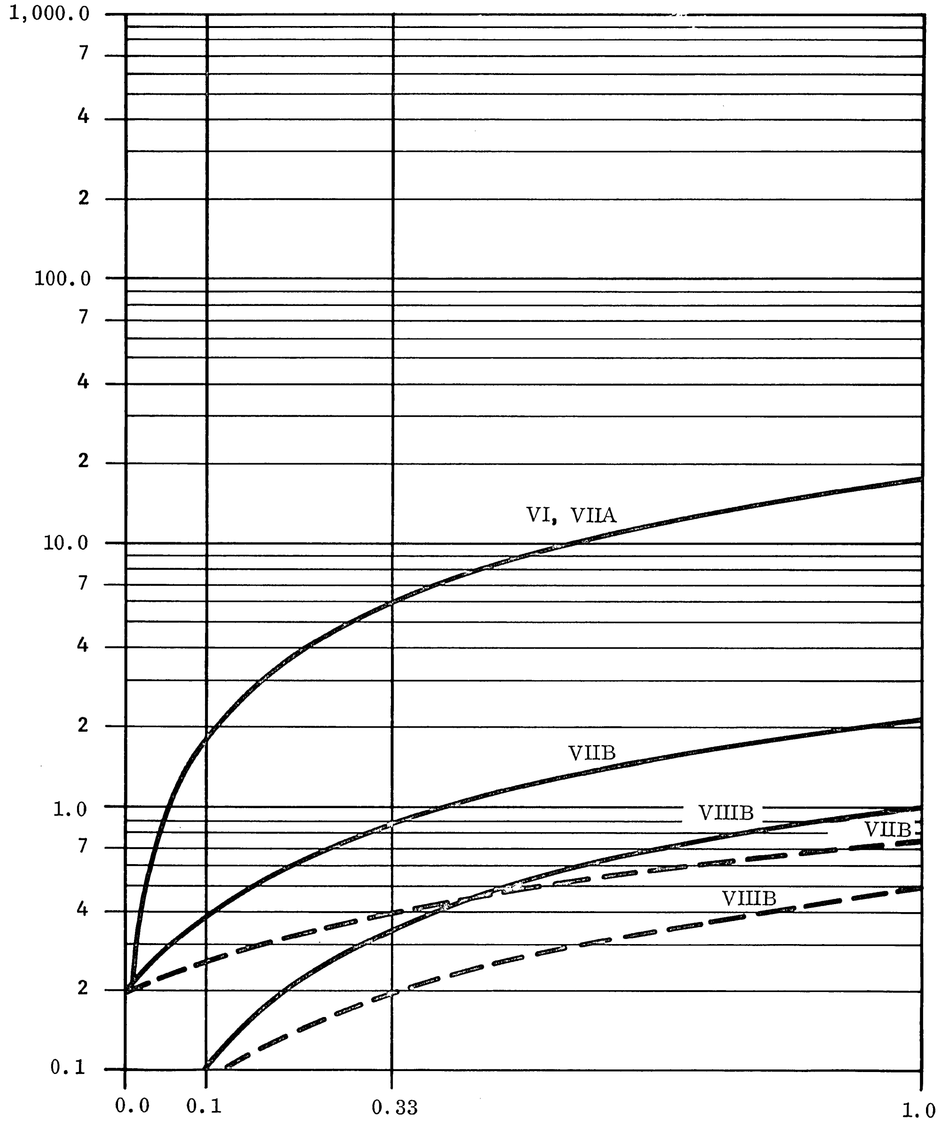
§ 201.

.12 Standard File Problem B

.121 Record sizes
Master file: . . . . . . 54 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.122 Computation: . . . . standard.
.123 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . see graph below.

Time in Minutes to Process 10,000 Master File Records



Activity Factor
Average Number of Detail Records Per Master Record

(Roman numerals denote Standard Configurations.)

Unblocked Files 3 & 4
Blocked Files 3 & 4

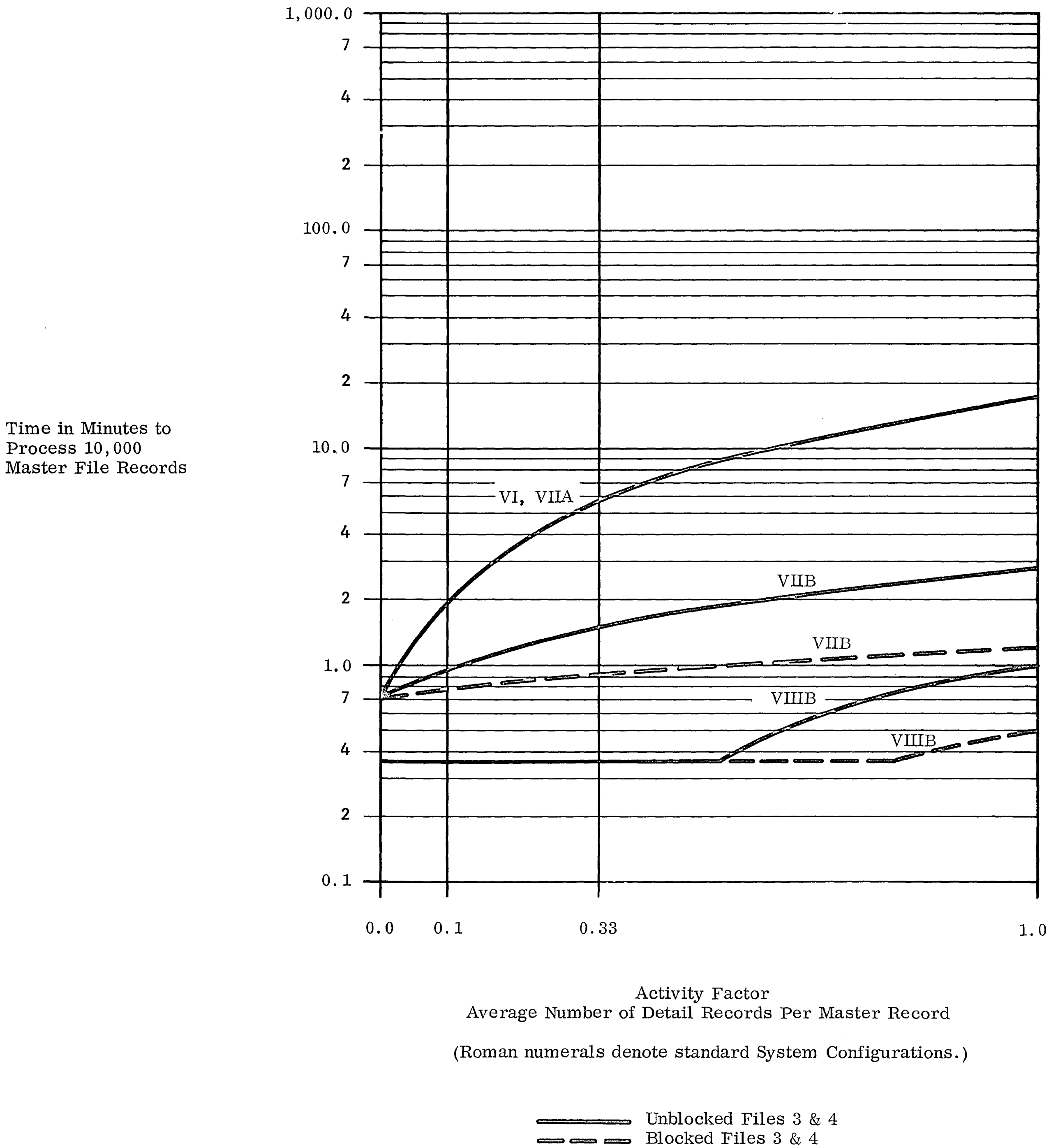
AUERBACH

§ 201.

.13 Standard File Problem C

.131 Record sizes
Master file: . . . . 216 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.132 Computation: . . . . standard.
.133 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

§ 201.

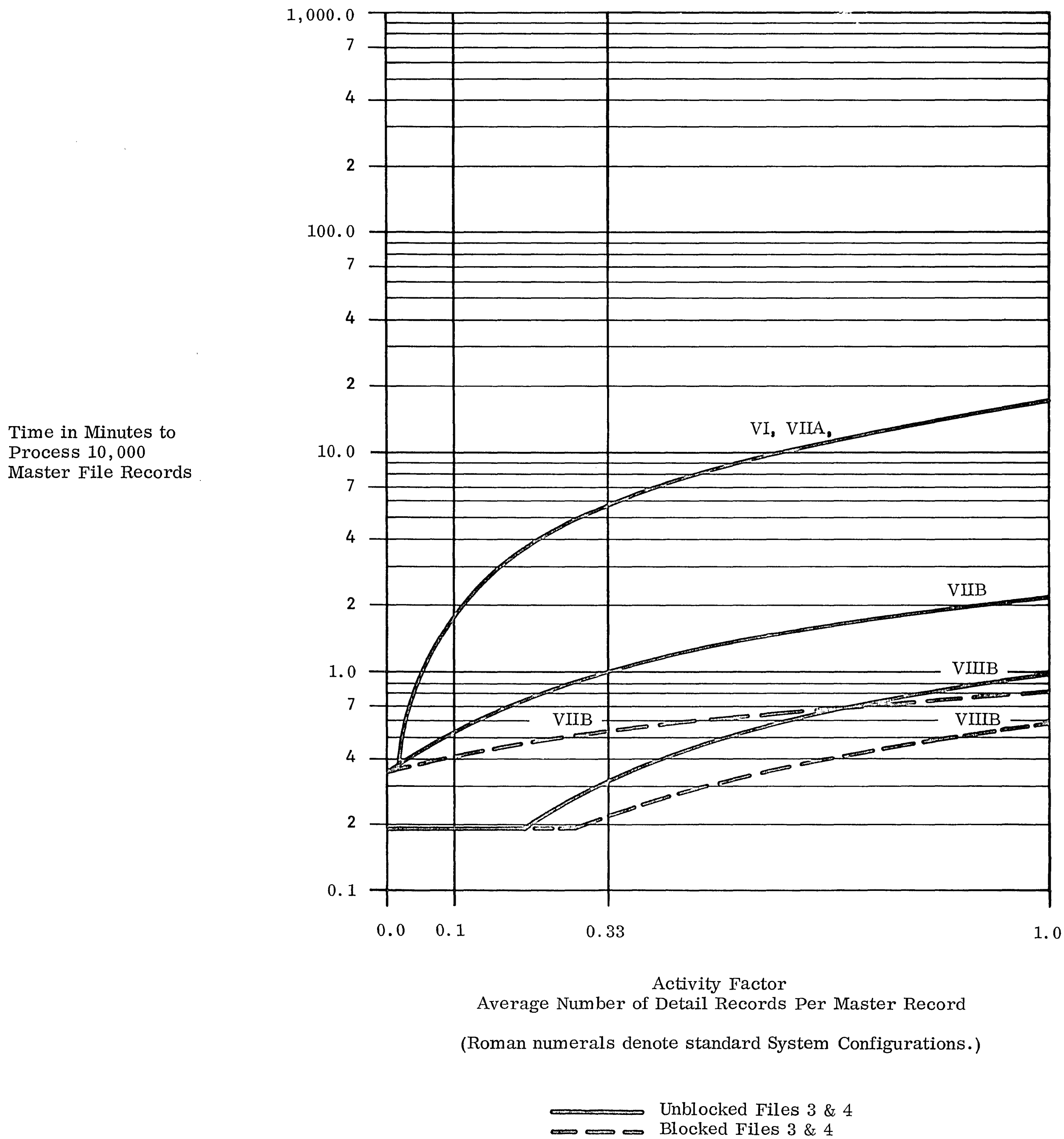
.14 Standard File Problem D

.141 Record sizes
- Master file: . . . . . . 108 characters.
- Detail file: . . . . 1 card.
- Report file: . . . . 1 line.

.142 Computation: . . . . trebled.

.143 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.

.144 Graph: . . . . see graph below.

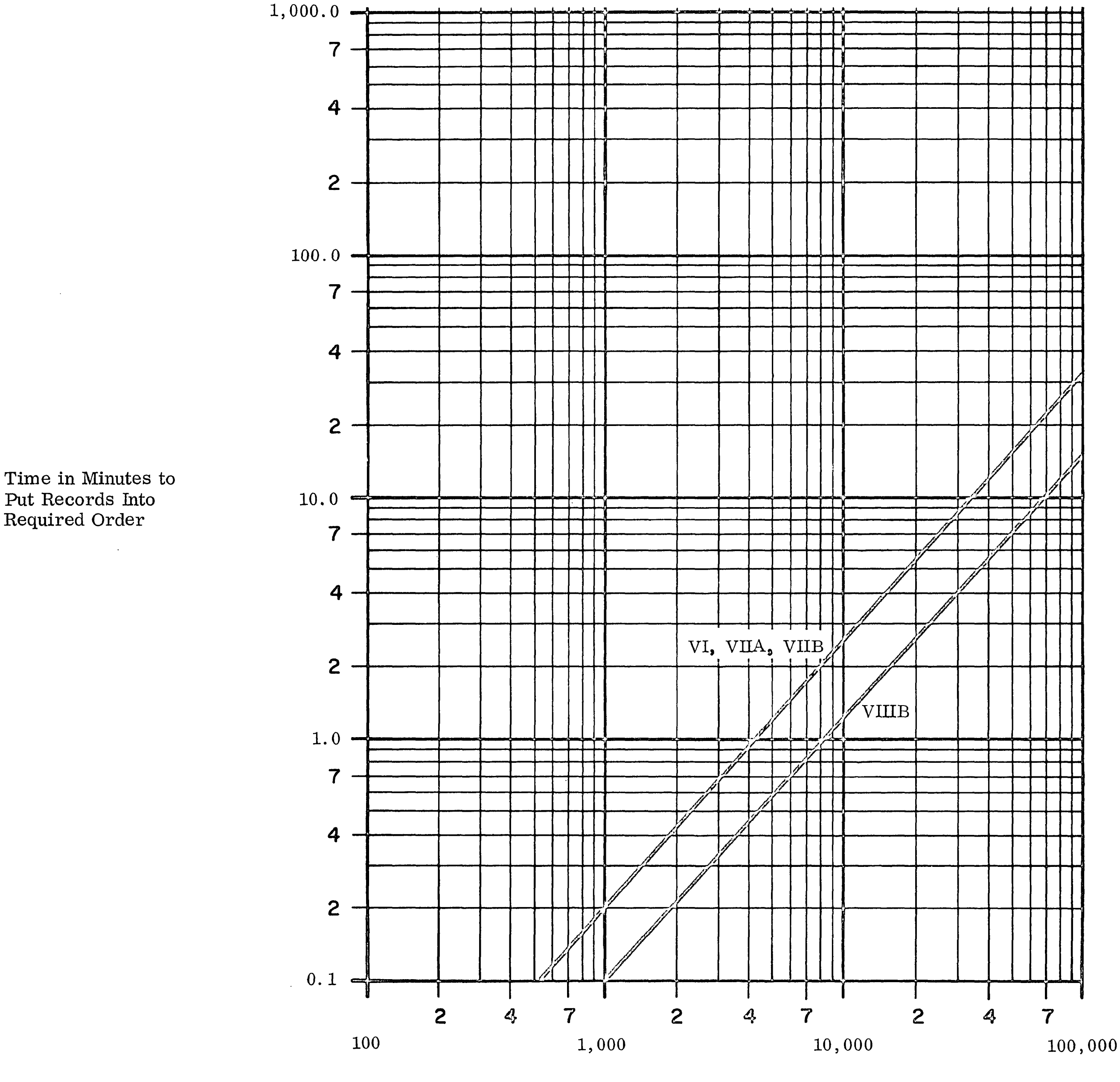


§ 201.

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . 80 characters.
.212 Key size: . . . . 8 characters.
.213 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.
.214 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

§ 201.

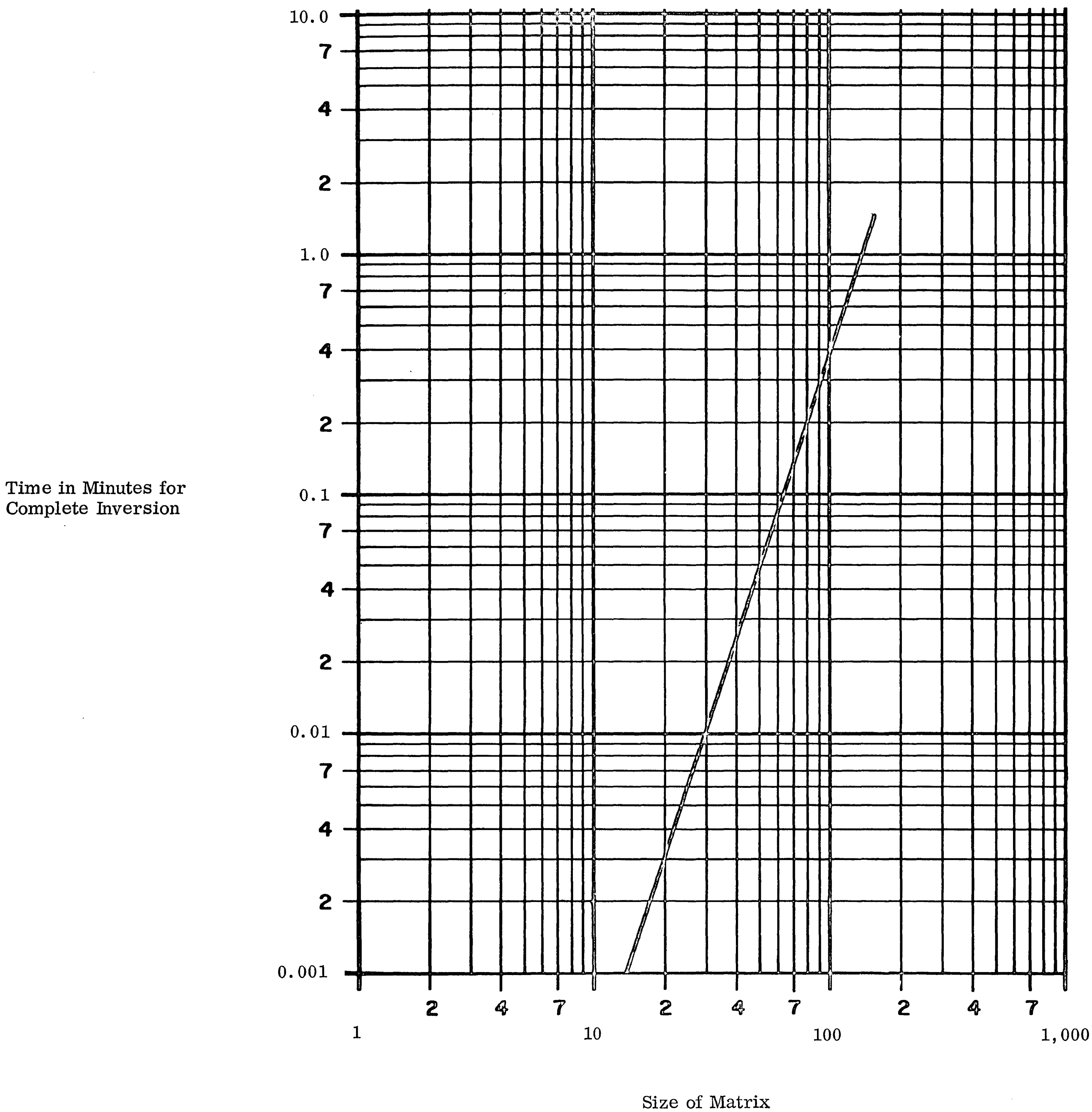
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.312; 11-digit precision floating point, using the optional floating point hardware.

.313 Graph: . . . . see graph below.



§ 201.

.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates (Unblocked Input and Output)

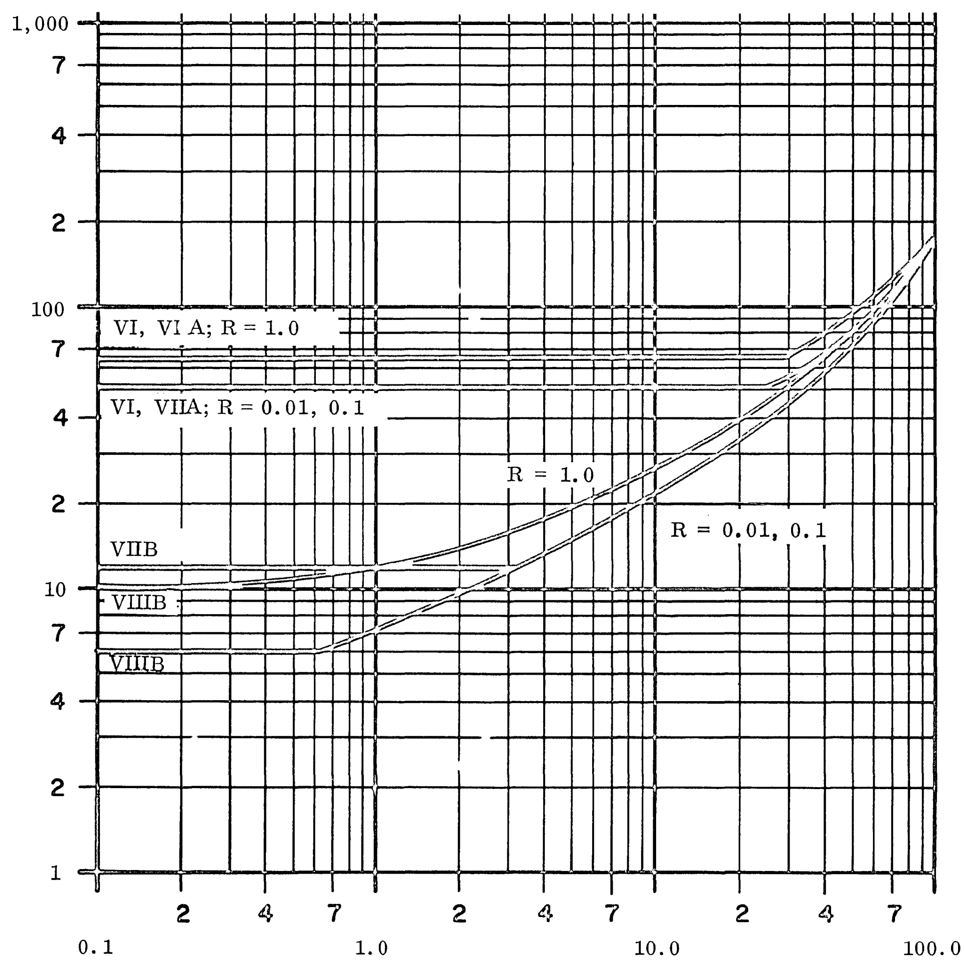
.411 Record sizes: . . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

.412 Computation: . . . . 5 fifth-order polynomials.
5 divisions.
1 square root.

.413 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.413; unblocked input and output records; all arithmetic in 11-digit precision floating point, using the optional floating point hardware.

.414 Graph: . . . . see graph below.

Time in Milliseconds per Input Record



C, Number of Computations per Input Record

(R = Number of output records per input record; Roman numerals denote standard System Configurations.)

§ 201.

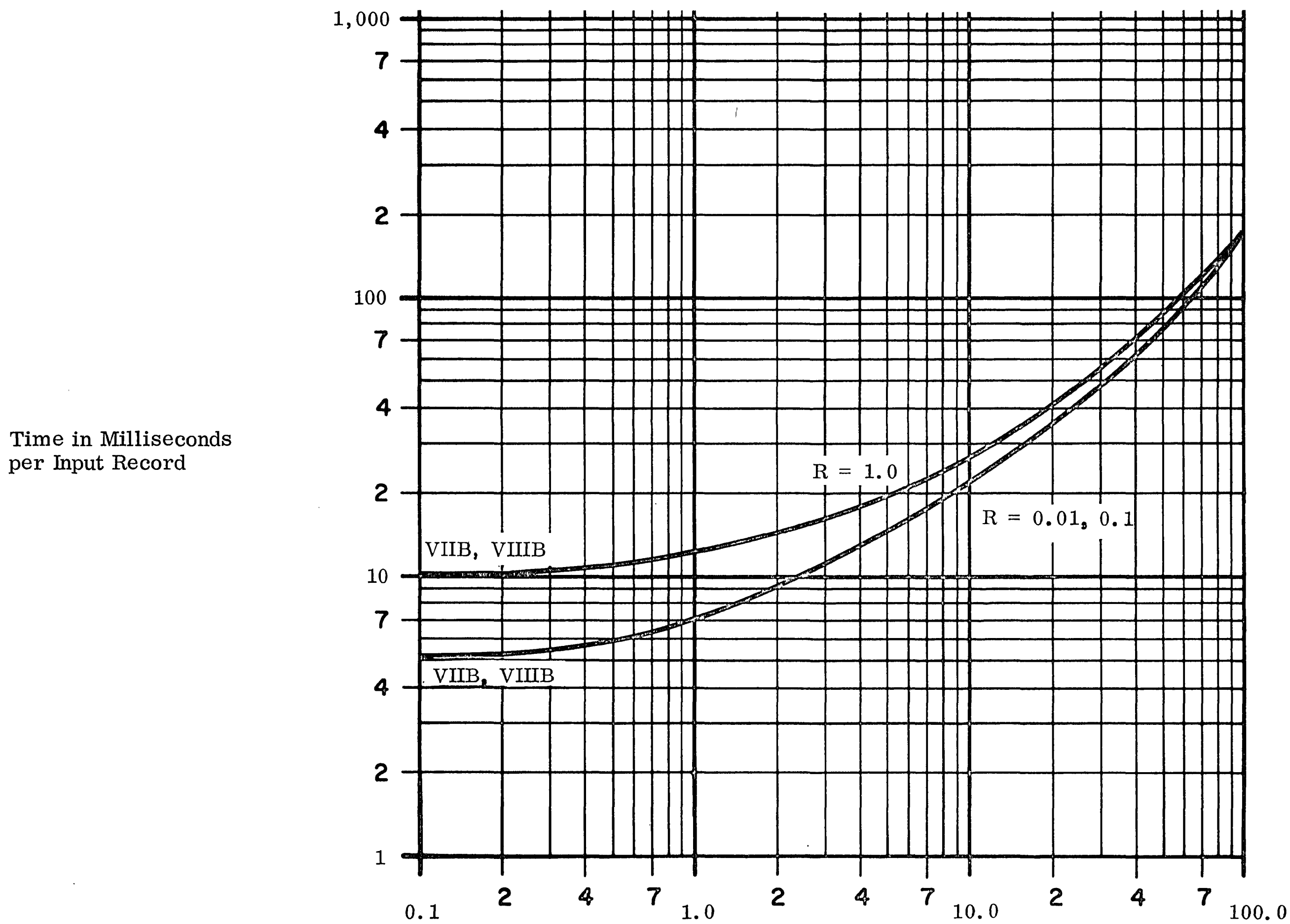
.42 Standard Mathematical Problem A Estimates (Blocked Input and Output)

.421 Record sizes: . . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

.422 Computation: . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.423 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.413; blocked input and output records; all arithmetic in 11-digit precision floating point, using the optional floating point hardware.

.424 Graph: . . . . see graph below.



C, Number of Computations per Input Record

(R = Number of output records per input record; Roman numerals denote standard System Configurations.)

§ 201.

.5 GENERALIZED STATISTICAL PROCESSING

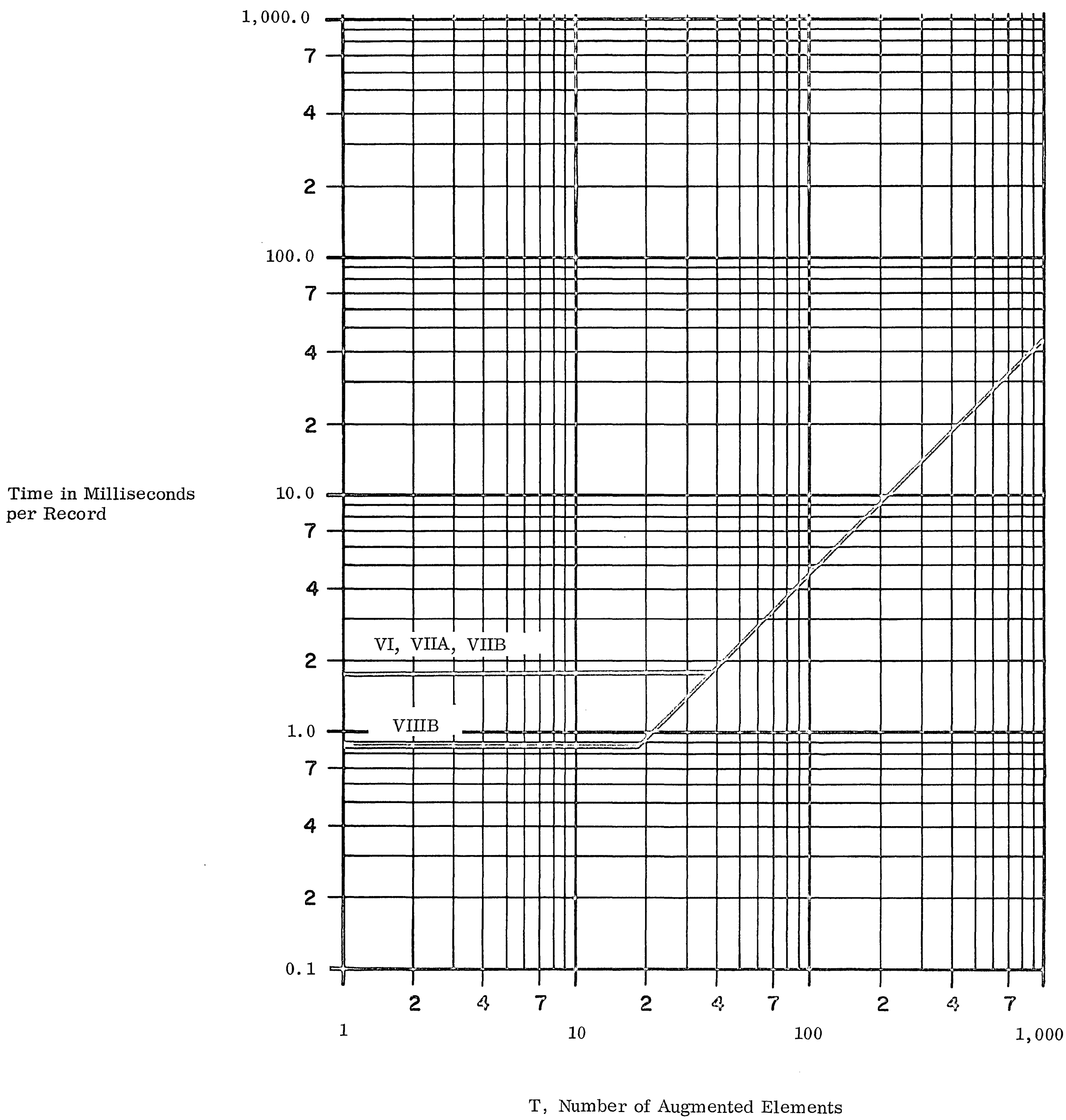
.51 Standard Statistical Problem A Estimates

.511 Record size: . . . . thirty 2-digit integral numbers.

.512 Computation: . . . . augment T elements in cross-tabulation tables.

.513 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.513.

.514 Graph: . . . . see below.



(Roman numerals denote standard Configurations.)

PHYSICAL CHARACTERISTICS

§ 211.

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
3404 Central Computer	83.8	20	75	1,800	1.8	3,300
3401 Console	46.0	28	40	500	0.5	3,300
3409 Core Storage Module	40.8	20	75	950	1.0	5,250
3406 Data Channel	40.8	20	75	950	1.0	5,250
Power Control	40.8	20	75	950	1.0	4,300
All Magnetic Tape Controllers	45.0	27	75	950	1.0	5,250
3446 Peripheral Controller	40.8	20	75	950	1.0	5,250
3691 Paper Tape Reader-Punch	40.0	24	39	400	0.6	2,000
405 Card Reader	57.0	33	46	1,020	?	8,730
604, 607 Magnetic Tape Units	28.0	33	72	1,200	?	8,500
828 Disk File	68.3	35	63	2,575	3.5	?

General Requirements

Temperature: . . . . 65 to 85°F.
Relative Humidity: . . . . 40 to 60%.
Power: . . . . 208/120 volt, 3-phase, 4-wire, 60-cycle source.

PRICE DATA

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
STORAGE AND COMPUTATION	3404	Central Computer; including maintenance control panel, power converter and control, and 16,384 words of magnetic core storage.	13,750	?	622,000
	3409	32K Storage Option; 16,384 additional words of core storage.	3,500		165,000
	3410	Floating Point Option; provides single precision floating point instructions.	800		34,000
	3401	Console; includes input/output typewriter.	720		33,500
COMMUNICATION	3404	Standard Data Channel	1,100	?	49,500
	3407	Special 24-bit Data Channel*	1,250		56,500
	3408	Special 48-bit Data Channel*	1,400		63,500
	3681	Data Channel Converter; permits 160/160-A to use 3400 peripheral equipment.	275		10,800
	3682	Satellite Coupler; permits direct connection between any two standard 12-bit bi-directional channels or Data Channel Converters.	415		16,200
INPUT-OUTPUT	3447	Card Reader Controller; controls CDC 405 Card Reader	525	?	24,500
	405	Card Reader; 1,200 cpm	550		30,250
	3446	Card Punch Controller; controls an IBM 523 or 544 card punch	645		31,500
	3256	Line Printer Controller; controls one 501 printer	715	?	22,000
	501	High-Speed Line Printer; prints 1,000 lines per minute.	1,167		57,400
	3253	Line Printer; 300 lines per minute	735		36,735
	3691	Paper Tape Reader-Punch; 350 cps reader and 110 cps punch	640	?	25,000
	3692	Program Controlled Input-Output Typewriter	280		11,000
	3293	Incremental Plotter	285		9,000
	3421	Magnetic Tape Controller; two read-write controls to control one to four 604/607 Magnetic Tape Transports	1,250	?	65,000
	3422	Magnetic Tape Controller; two read-write controls to control one to six 604/607 Magnetic Tape Transports	1,750		83,000

* Available for special applications only.

§ 221.

PRICE DATA (Contd.)

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
INPUT-OUTPUT (Contd.)	3423	Magnetic Tape Controller; two read-write controls to control one to eight 604/607 Magnetic Tape Transports	2,250	?	101,000
	604	Magnetic Tape Transport; up to 60KC	675		32,500
	607	Magnetic Tape Transport; up to 120KC	935		41,700
	3632	Disk File Controller; two read-write-positioning controls for one 828 Disk File	2,750	?	110,000
	3633	Disk File Controller; same as 3632 but controls up to two 828 Disk Files	3,050		122,000
	3634	Disk File Controller; same as 3632 but controls up to three 828 Disk Files	3,350		134,000
	3635	Disk File Controller; same as 3632 but controls up to four 828 Disk Files.	3,650		146,000
	828	Disk File; dual access.	2,800		122,000

CDC 3600

Control Data Corporation

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CONTENTS

RIP = Report in Process
INA = Information Not Available

CONTENTS (Contd.)

INA = Information not Available

INTRODUCTION

§ 011.

The CDC 3600 computer system can perform nearly half a million additions per second, thus making it one of the fastest commercially available internal processing systems. The core storage capacity ranges from 16,384 to 262,144 words (48 bits), and an elaborate data channel system featuring a separate communication module permits an almost indefinite number of peripheral units (or central processors) to be connected. For simultaneous operation standard systems can include up to 512 tape units. The cost of the 3600, which begins at $45,000, is lower than that of the IBM 7094 and Philco 212, and is higher than that of the UNIVAC 1107 and the H-1800.

Although the 3600 is basically an advanced version of the CDC 1604 large scale computer system, a number of changes have been made to the CDC 1604 central processor design. Primarily, these changes include instructions which handle parts of words, or "bytes". The performance characteristics of the system are thereby greatly changed and the processing times for many of the problems used as central processor performance criteria, even without considering the faster internal core storage (1.5 compared to 3.2 microseconds), have improved by 70 percent compared to those for the same functions on the 1604.

A number of additional instructions have been included in the 3600 that do not exist in the 1604. These instructions include double precision floating point arithmetic, the ability to perform double indexing of operands, etc., and are particularly valuable in matrix calculation programs. However, they do not have the same impact on the over-all system performance as the byte-handling capabilities.

CDC 1604 programs can be run on the 3600, but the reverse is possible only under restricted circumstances. FORTRAN 63, CXA (a version of Algol 60), and COBOL-61 translators are being made available for both computer systems; thus programs written in these languages can be compiled for either system.

Across the board programming compatibility is restricted to that which is obtained by use of common languages: FORTRAN, COBOL, and ALGOL. For details, see the sections describing these languages.

The magnetic tape codes and the internal BCD code for the CDC 3600 and 1604 are identical to those for the IBM 7090 and 7094 systems with IBM 729 tape units. Tapes can be exchanged between the systems; i.e., the CDC 606 tape unit can use magnetic tape reels written by IBM 729 units and vice versa.

The 3600 central processor is an improved version of its equivalent CDC 1604 unit. The improvements have been designed to retain compatibility with the 1604, yet give much-improved performance.

Several powerful instructions have been included in the 3600 repertoire, two of which act on other ordinary instructions to permit the programmer to perform many extensions of the basic instruction. For instance, complementation, clearing the operational source, and changing the sign, can all be performed simultaneously with addition or subtraction.

The main improvements incorporated into the 3600 are the double precision operations, byte operations, the new D (or Flag) Register, and the table and list instructions:

- Double Precision Floating Point operations with 84-bit mantissas are possible.
- Byte-handling instructions process parts of words and considerably reduce the housekeeping involved in such things as code conversions and almost all types of character handling operations.

INTRODUCTION (Contd.)

§ 011.

- Bit-directed facilities. Single bits can be tested, set, and branched upon when encountered. These facilities also can direct a 1-instruction, 49-way branch which scans a 48-bit word and jumps to a position based on the most significant 1-bit. Used in conjunction with the input-output and other control registers, this feature considerably reduces the time involved in getting through a network of subroutines. Again, the improved performance comes from the elimination of housekeeping efforts rather than the faster computation.

- Table-searching and list-construction instructions Single instructions can automatically search tables (within limits) for the following conditions within 2 microseconds: equal, not equal, greater than, less than. Search instructions can handle any character size from 1 to 48 bits. A list held in a specific prescribed form can be created and changed continuously.

Input and output are controlled by means of Communication Modules. Rates of up to 133,000 characters per second are always possible, even under worst-case conditions; however, at present no character rate greater than 83,000 characters per second is available. The Communication Modules have direct access to each 16,384-word bank of core storage, which means that the central processor is delayed during input-output operations only if both the input-output and the central processor are attempting to access the same core storage bank. The basic system has 2 banks, and expanded versions have up to 16 banks.

Each of the core storage banks initiates its word cycle independently of the others. This provides for asynchronous operation if different banks are used. Although the cycle time (1.5 microseconds) is fixed, the extent to which each bank is used is determined only by the program. For this and other reasons, the actual times quoted for an instruction are only approximate. Changes in speed of up to 20 percent are possible, depending upon the actual situation, and should be anticipated by each installation manager.

Peripherals for the 3600 system which have been announced include CDC 606 Tape Units, two card readers (one IBM, one CDC), paper tape equipment, a card punch, and a 1,000 line per minute printer. Full details are available only for the tape units and the IBM card readers. The other announced units are apparently similar to their predecessors as used in the 1604 system.

These peripherals provide for three types of interrupts within the central processor, and for automatic translation to and from internal binary coding.

The means for connecting magnetic tape units into 3600 systems are much more flexible than in the 1604. Two, three, or four tape units per controller can be used at one time, and no restriction now exists as to how many units can be reading and how many can be writing. All can be reading or all can be writing, or any mixture of the two modes of operation can be utilized.

Direct Data Communication links are available for the 3600 and two controllers are available which link the 3604 Central Processor to one or more 160 or 160-A computers. Development appears to have been concentrated on providing controllers for peripheral units.

A comprehensive body of software exists insofar as a number of routines, assemblers, supervisors, etc., have been developed for the CDC 1604, which can therefore be run with little or no modification on the 3600. Faster processing will be achieved, but no advantage will accrue to the user from the new specialized instructions. Details of these routines are given in the report on the CDC 1604-A (Report 243:).

New software for the 3600 includes:

- A run-to-run supervisory Master Control System, which supervises the input-output handling, interrupts, relocation, etc., but deals with only one program at a time. In view of the high processing speeds of the 3600, these often take little running time, so that routines like this which reduce operator delays become of greater importance.

INTRODUCTION (Contd.)

§ 011.

Search operands can be indirectly addressed, os that a search can be conducted even when the keys are scattered, provided their addresses are listed in a table.

- FORTRAN-63. An advanced FORTRAN language which is compatible with the FORTRAN 63 of the CDC 1604-A. The translator is specialized with subscripts to deal economically with expressions and provides buffer control for the FORTRAN programmer. The FORMAT statement is still handled interpretively at running time by being scanned each time it is encountered.

- An ALGOL dialect, CXA, to be released in 1963.

- A COBOL-61 Compiler, to be released late in 1963.

DATA STRUCTURE

§ 021.

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	48 bits	basic addressable unit; contains data item or two instructions.
Character:	6 bits	internal BCD code.
Block:	1 to N words	magnetic tapes.

.2 DATA FORMATS

Type of Information	Representation
Operands:	48-bit fixed point words. 48- or 96-bit floating point word.
Instructions:	24 or 48 bits. 24-bit instructions are packed two per 48-bit word.
Fixed Point:	47 data bits plus 1 sign bit.
Floating Point	
(Single Precision): . .	36 bits plus sign for fixed point part 11-bit exponent.
(Double Precision): . .	84 bits plus sign for fixed point part 11-bit exponent.

NOTES ON SYSTEM CONFIGURATION

§ 031.

The CDC 3600 system is organized along four basic lines:

1. The Core Store

The core store consists of from one to sixteen 16,384-word modules. Each module has independent access to all computing modules and communication modules.

2. The Computing Modules and the Communication Modules

At least one of each, and at most a combined total of five can be used in a system. Note that these modules act in parallel; thus, it is not necessary for input or output data to pass through the computing modules while passing between the core store and the peripheral units.

3. Data Channels

From one to eight data channels can be connected to each communication module. Each channel added allows one further data transmission to proceed in parallel.

4. Peripheral Units, Controllers and Adapters

A combination of up to eight peripheral units, controllers, and adapters can be connected to any one channel. Each controller can control up to 16 units, depending on the design of the actual equipment. Additional bits are available which would theoretically allow 512 units to be referenced by each controller.

Peripheral units, such as printers, card readers, etc., can be connected directly to the data channels.

Adapters to connect the data channel with satellite computers, data transmission devices, etc., can also be connected. It is not necessary for the adapter to connect the satellite computer directly to the store, although this can be done. If required, the connection can be to other input-output devices connected to the communication module.

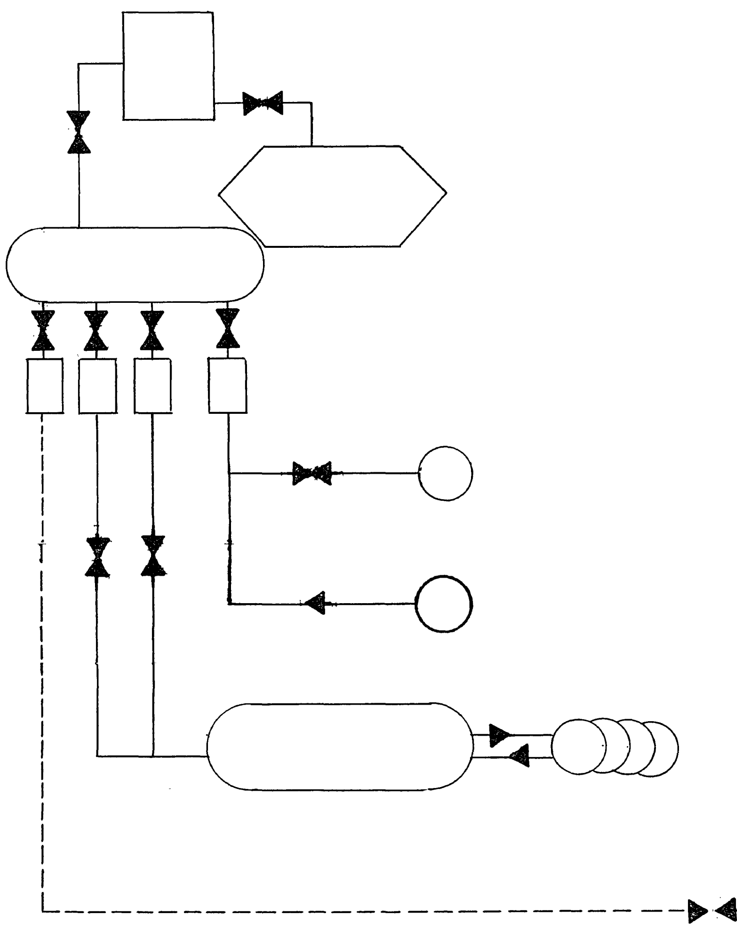
SYSTEM CONFIGURATION

§ 031.

.1 PAIRED 6-TAPE BUSINESS/SCIENTIFIC SYSTEM (CONFIGURATION VI B)

Main Computer

Deviations from Standard Configuration: . . . . direct connection to auxiliary computer.
1 additional magnetic tape transfer while computing.
1 additional input/output transfer while computing.
3 extra index registers.

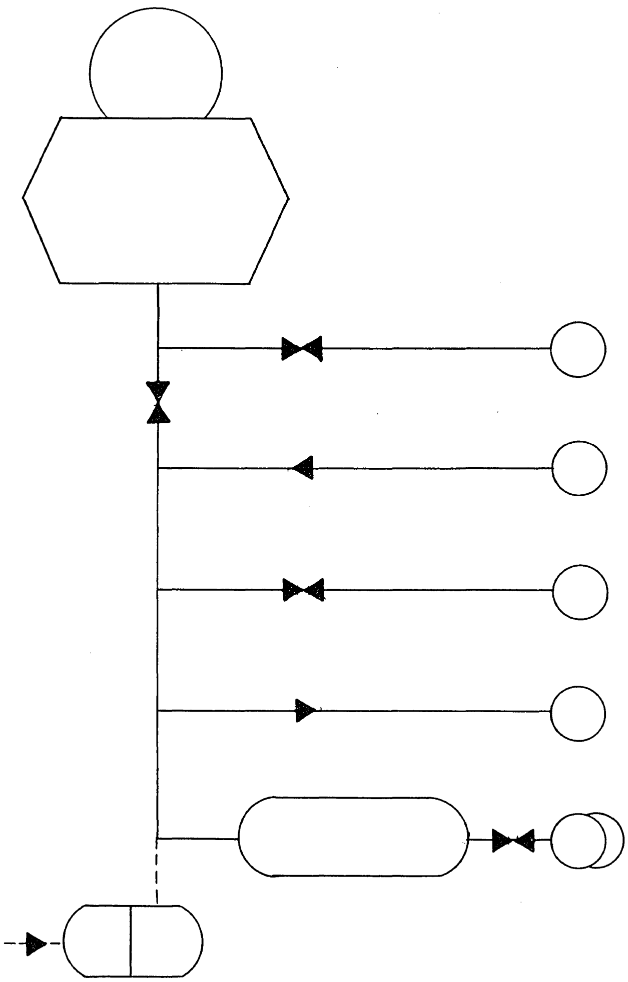


Equipment	Rental
Model 3603 Storage Module 32,768 words core store.	$14,360
Model 3604 Computation Module including Real Time Clock	20,755
Model 3602 Communication Module.	3,255
4 Model 3606 Standard Bi-directional Data Channels.	3,600
Console including: Typewriter, 10 char/sec;	1,790
Model 3641 Card Reader: 250 cards/min.	695
CDC 3621 Magnetic Tape System with 4 magnetic tape units;	2,700
peak speed 83,000 char/sec.	3,300
CDC 3667 Power Convertor and Power Control	795
TOTAL	$51,250
TOTAL, including both computers	$58,599

§ 031.

Auxiliary Computer

Deviations from Standard Configurations: . . . . direct connection to main computer 12-bit words extra storage.
faster printing (1,000 instead of 500 cards/min.)
slower card-reading (250 instead of 500 cards/min.)
multiply/divide included.
typewriter output.
paper tape input and output.



To Main Computer

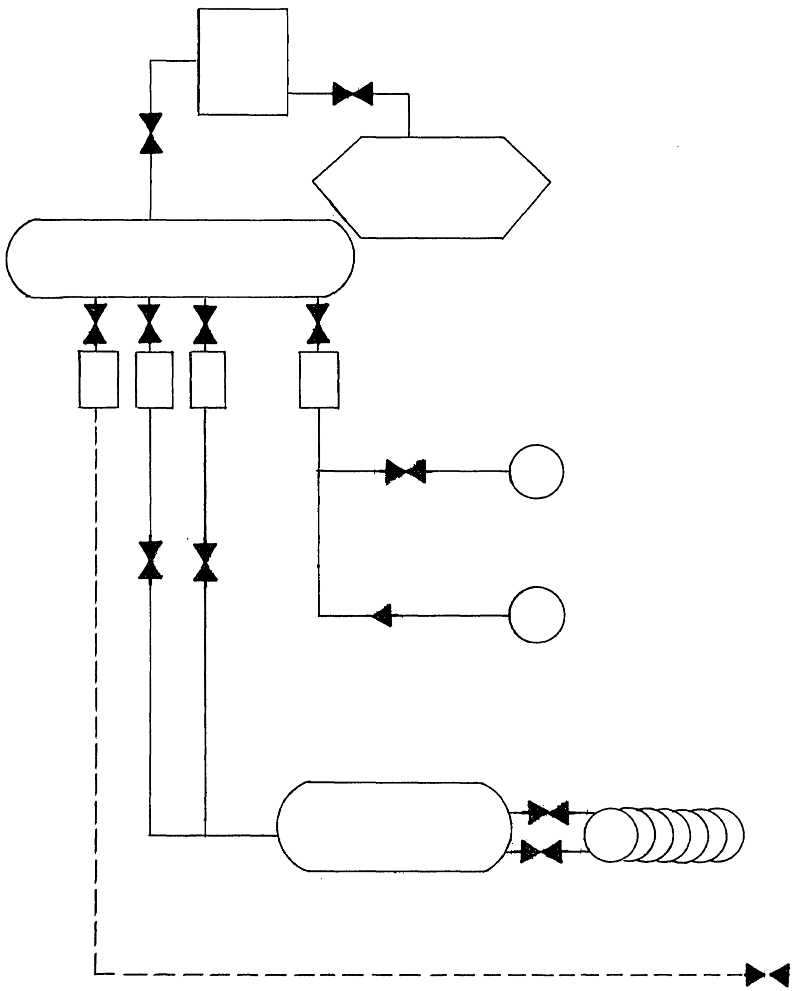
Equipment	Rental
Core Storage: 12-bit words.	
CDC 160 Computer Central Processor:	$1,762
Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	
CDC 167 Card Reader: 250 cards/minute	400
CDC 1609 Card Read/Punch Unit: 100 cards/minute	1,175
CDC 1612 Line Printer: 1000 lines/minute	1,840
CDC 163-2 Magnetic Tape Unit with 2 tape units; peak speed 30,000 char/sec;	1,482
CDC 3681 Data Channel Converter	275
CDC 3682 Satellite Compiler	415
TOTAL	$7,349

§ 031.

.2 PAIRED 10-TAPE GENERAL SYSTEM (CONFIGURATION VII B)

Main Computer

Deviations from Standard Configuration: . . . . Direct connection to auxiliary computer. tape units 40 percent faster.



Model 3603 Storage Module 32,768 words core store	$14,360
Model 3604 Computation Module including Real Time Clock	20,755
Model 3602 Communication Module	3,255
4 Model 3606 Standard Bi-directional Data Channels	3,600
Console including: Typewriter, 10 char/sec:	1,790
Model 3641 Card Reader: 250 cards/min.	695
CDC 3261 Magnetic Type System, with 8 CDC 606 tape units; peak speed 83,400 char/sec:	2,700 6,600
CDC 3667 Power Converter and Power Control	795
TOTAL	$54,550

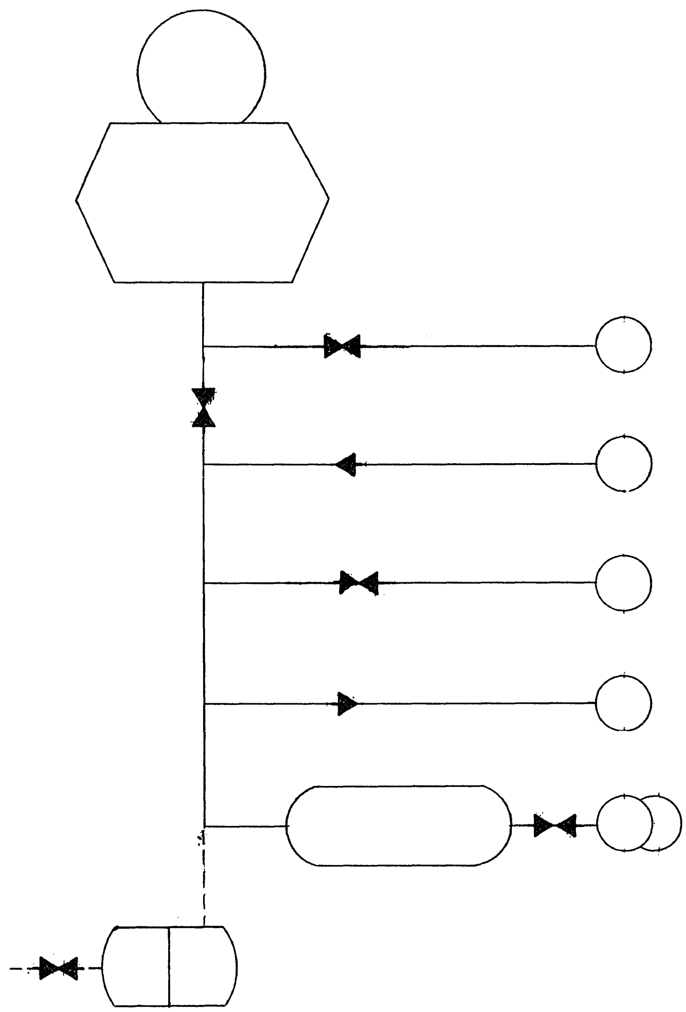
To Auxiliary Computer

TOTAL, including both computers: $61,899

§ 031.

Auxiliary Computer

Deviations from Standard Configurations: . . . .
direct connection to main computer
12-bit words extra storage.
faster printing (1,000 instead of 500 cards/min.)
slower card-reading (250 instead of 500 cards/min.)
multiply/divide included.
typewriter output.
paper tape input and output.



To Main Computer

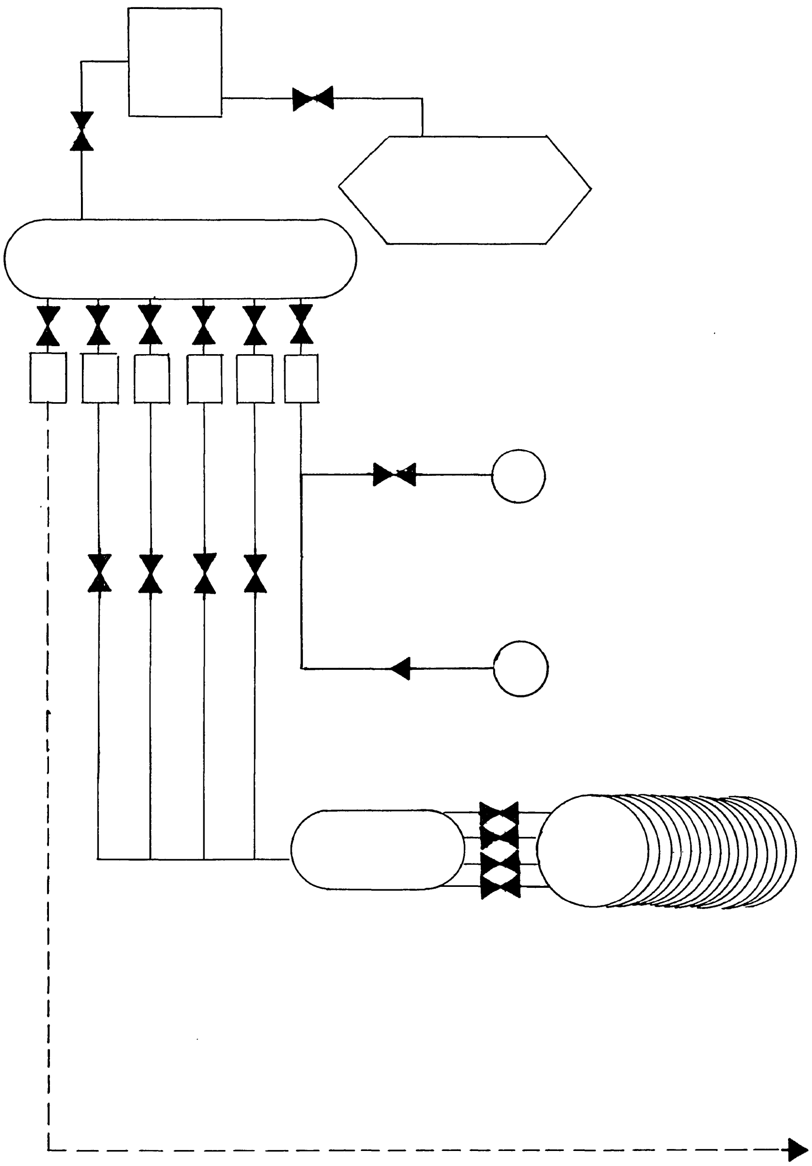
Equipment	Rental
Core Storage: 12-bit words	$1,762
CDC 160 Computer Central Processor:	
Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	
CDC 167 Card Reader: 250 cards/minute	400
CDC 1609 Card Read/Punch Unit: 100 cards/minute	1,175
CDC 1612 Line Printer: 1000 lines/minute	1,840
CDC 163-2 Magnetic Tape Unit with 2 tape units; peak speed 30,000 char/sec:	1,482
CDC 3681 Data Channel Converter	275
CDC 3682 Satellite Compiler	415
TOTAL	$7,349

§ 031.

.3 PAIRED 20-TAPE GENERAL SYSTEM (CONFIGURATION VIIIB)

Main Computer

Deviations from Standard Configuration: . . . . direct connection to auxiliary computer
4,000 48-bit words extra storage.
tape units 30 percent slower.

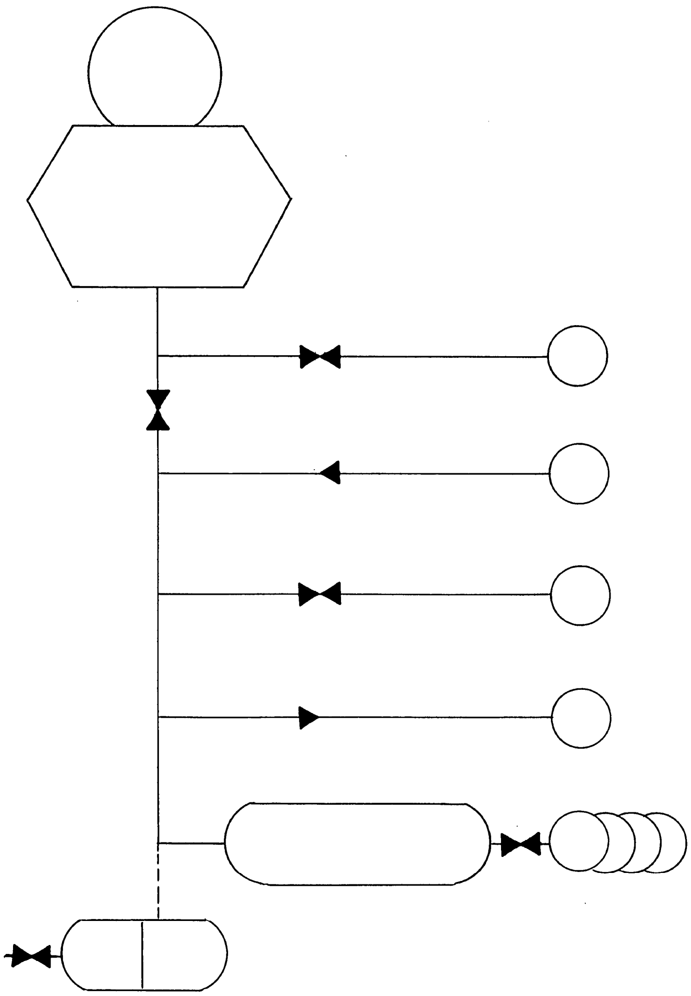


Model 3603 Storage Module 32,768 words core store.	$14,360
Model 3604 Computation Module including Real Time Clock.	20,755
Model 3602 Communication Module.	3,255
6 Model 3606 Standard Bi-directional Data Channels	5,400
Console including: Typewriter, 10 char/sec:	1,790
Model 3641 Card Reader: 250 cards/min.	695
CDC 3624 Magnetic Tape Systems, each	4,750
with 16 CDC 606 tape units; peak speed 83,600 char/sec.:	13,200
CDC 3667 Power Converter and Power Control.	795
TOTAL	$65,000
TOTAL, including both computers:	$73,910

§ 031.

Auxiliary Computer

Deviations from Standard Configurations: . . . . .direct connection to main computer
12-bit words extra storage.
faster printing (1,000 instead of 500 lines/min.)
slower card-reading (250 instead of 500 cards/min.)
multiply/divide included.
typewriter output.
paper tape input and output.



To Main Computer

Equipment	Rental
Core Storage: 8,192 12-bit words; CDC 160-A Central Processor; Console including: Typewriter, 10 char/sec; Paper Tape Reader, 350 char/sec; Paper Tape Punch, 110 char/sec.	$2,250
CDC 167 Card Reader: 250 cards/minute	400
CDC 170 Card Punch Controller	335
IBM 523 Card Punch	85
CDC 1612 Line Printer: 1000 lines/minute	1,840
CDC 162-2 Magnetic Tape	700
System with 4 tape units; peak speed 82,300 char/sec;	3,300
TOTAL	$8,910

INTERNAL STORAGE: CORE STORAGE

§ 041.

.1 GENERAL

.11 Identity: . . . . Core Storage, Model 3609.

.12 Basic Use: . . . . working storage.

.13 Description

The core store of the CDC 3600 system consists of from 1 to 16 storage modules. Each module contains 16, 384 48-bit words, and is connected to all the computing modules and the communication modules in the system.

These connections are direct and independent of the connections between the same units and other storage modules. Thus, it is effectively possible to:

(1) Avoid delay in computation by overlapping the access times of multiple banks.

(2) Add additional input-output capability to a system simply by adding more storage banks. The time spent in accessing these banks can, if needed, be totally overlapped with the time used to access the original banks of the system.

The cycle time of each bank of store is 1.5 microseconds. The effective cycle time of the store while being used for computation is approximately 1 microsecond, taking into account the overlapping of the bank containing the instructions and the bank containing the operands. (It is assumed that these are normally in different banks.)

Core storage banks are called "overlapped" whenever the cycle of one proceeds simultaneously with but independently of the cycle of another. This normally occurs when an operand is requested from one core bank very soon after one has been read from another independent bank. Since the operand which was read becomes available when the read/rewrite cycle is only about one-third complete, it is possible (and the 3600 is able) to be ready for the next operand before the cycle is completed. When this occurs, time can be saved by requesting the second operand from an independent store whose read/rewrite cycle can be initiated before completion of the cycle that obtained the first operand.

The CDC 3604 central processor normally requests data from two banks, the instruction bank (I) and the operand bank (O), in the order: (I), (O), (O); (I), (O), (O). Fetching of the instruction is always a read operation; therefore, access to the first operand is always overlapped with the instruction cycle. However, the second operand, since it is in the same bank, is not overlapped.

.13 Description (Contd.)

The input-output capacity of each 16, 384-word storage bank is approximately 5 six-bit characters per microsecond, which is approximately 60 times the data transmission rate of a CDC 606 tape unit. As noted above, if a system requires additional input-output storage capacity, this capacity can be obtained by adding another storage bank.

The bank address is manually set by means of a rotary switch on the cabinet. Physically, two 16, 384-word banks are contained in one cabinet, which is called a 3603 Storage Module. This use of bank addresses is a restriction only insofar as:

(1) an additional instruction is needed to change the bank from which either operand or instructions are being chosen, and

(2) both base operand addresses in an instruction pair must be taken from the same bank.

Parity bits are carried with each word. The three parity bits which are used are formed from parts of the word as used in instruction pairs. Thus, one bit is logically attached to each operand address, and one bit is attached to the two operation code portions. Words are divided thus whether or not they are actually to be used as instruction pairs.

.14 Availability: . . . . . . 7 months.

.15 First Delivery: . . . . 1963.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic cores.

.22 Physical Dimensions

.221 Magnetic core type storage
Core diameter: . . . . ?
Core bore: . . . . . . ?
Array size: . . . . . . ?

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . . yes.
.243 Data volatile: . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

§ 041.

.27 Interleaving Levels: . . none within 1 bank. The use of multiple core storage banks effectively provides interleaving, reducing access time to approx. 1 μsec.

.28 Access Techniques

.281 Recording method: . . . coincident current.
.282 Reading method: . . . . sense wire.
.283 Type of access: . . . . read out followed by rewrite.

.29 Potential Transfer Rates

.292 Peak data rates
Cycling rates: . . . . up to 667,000 cps per bank.
Unit of data: . . . . . one 48-bit word.
Gain factor: . . . . . use of 2 or more 3609 stores.
Data rate: . . . . . . 667,000 words/sec/bank.
Compound data rate: . 667,000 to 21,333,000 words/sec, depending on number of banks connected.

.3 DATA CAPACITY

.31 Module and System Sizes

48-bit words: . . . . . 32,768.
24-bit instructions: . . 65,536.

.4 CONTROLLER: . . . . no separate controller.

.5 ACCESS TIMING

.51 Arrangement of Heads: each 16,384-word store has independent access facilities.

.52 Simultaneous Operations: . . . . . . accesses to each store are asynchronous and independent of each other.

.53 Access Time Parameters and Variations

.531 Cycle time: . . . . . . 1.5 μsec.
For data unit of: . . . . 1 word.
2 instructions.
.532 Variation in cycle time: see introduction.

.6 CHANGEABLE STORAGE: . . . . . . none.

.7 STORAGE PERFORMANCE

.71 Data Transfer

Pair of storage unit possibilities
With self: . . . . yes.

.72 Transfer Load Size

With self: . . . . any number of words, using the transmit instruction.

.73 Effective Transfer Rate

With self: . . . . 385,000 words/sec.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Receipt of data:	address parity check	computer halted if parity is incorrect.
Recording of data:	3 parity bits recorded with data word	none at this stage.
Recovery of data for transmission to computing module:	parity check	console lamp lit, and optional interrupt.
Recovery of data for transmission to output:	parity check	parity check bit set, with optional interrupt.

CENTRAL PROCESSOR

§ 051.

.1 GENERAL

.11 Identity: . . . . Central Processor.
CDC 3604.

.12 Description

The 3600 is a single-address, fixed word length, binary processor. Many instructions take under 2 microseconds, and each module has the capability for executing approximately 600,000 instructions per second. Arithmetic operations are performed in binary on 48-bit words. The operations are performed in a parallel mode. Each word normally contains a pair of 24-bit single address instructions but other instruction lengths are also used. The address of an instruction can either be indexed or used as an indirect address. Three index-bit positions are provided in each instruction to select one of six index registers. However, one value of the index-bits specifies an indirect address, and indirect addressing may be recursive.

Operations are provided both in fixed point and in single and double precision floating point. Fixed length operands are 48 bits in size while floating point operands consist of an 11-bit characteristic and sign plus 84 or 36-bit fixed point parts. Both integral and fractional fixed point multiplication and division are provided.

Indexing by means of any one of the six index registers is available to almost all instructions. Increments from 1 to 32,768 words can be indexed, but provide access to the entire store only when a single 32,768 word module is attached.

The augment instructions are 24-bit instructions which modify the succeeding 24-bit instruction. This is a powerful device which has been used, among other things:

(1) To provide double precision floating point instructions by modifying the basic floating point instruction.

(2) To provide double indexing capabilities for most 24-bit instructions. The resultant operand address used in execution of the modified instruction is computed by adding the contents of the index register specified by the augment instruction to the address of the actual instruction which can itself have a specified index register. Thus the instruction pair "Augment, index register 3; ADD, index register 4, 00500" executed when index register 3 contains 30, and index register 4 contains 4, would add the contents of 00534 to the contents of register A. (Indirect addressing is available as an alternative to direct indexing in both the augmenting and augmented instruction.)

.12 Description (Contd.)

(3) To direct which of a number of modifications to standard instructions should be used. The actual modifications available are related to the actual instruction; typical examples are: to not round results, to not normalize results, to ignore the sign of the operand, to clear the operand location to zero after loading the operand into the register. Thus, if the instruction pair used in the example above were amended to read, "Augment, index register 3, t^4; ADD index register 4 00500" then the complement of the contents of 00534, not the contents themselves, would be added. A number of other, more complicated instruction modifications are available and their use will reduce the over-all number of instructions which must be executed.

The Execute Instruction, which itself can be augmented to provide a double-indexed instruction address, executes the instruction pair at specified locations, and then returns to normal sequencing. As the instruction pair itself can use one or two index registers, it is possible to design very short central loops involving a number of variaables. This approach has been used in estimating the time for the standard statistical problem. Here, in preparing a table, it is necessary to compute the address $(x - 1) + X(y - 1)$. Normally, multiplication is required but this has been avoided using the augment techniques. (See also Users' Guide.)

Further details of many of these instructions are given in the Instruction Code section of the report and reference should be made to that section.

Searching can be done by word or by byte †, with the housekeeping being performed within the logic of the instruction. Conditions which can be searched for include equality, inequality, more than, and less than.

The byte-handling facilities, in addition to being used in search operations, also can be used in Transmit and other bit-based or character-based operations, such as editing and code conversion. One of the major gaps in the instruction repertoire of the CDC 1604 is thereby filled.

Additional instructions which enhance the bit and character handling capabilities of the 3600 are the Inter-Register Transmit and the Register Jump instructions. The registers concerned include those used in computation, some temporary storage registers, and those reflecting external conditions. These registers can

† A "byte" is part of a computer word, consisting of from 1 to 48 bits. These bytes can be measured from either the most significant or the least significant end of the word.

§ 051.

.12 Description (Contd.)

be tested, interchanged, complemented, etc., as necessary within a single instruction and by the Jump-On Flag instruction, (which jumps to the one of 48 positions, if any of the 48 bits of the register are set at "1").

Increased processor speeds are normally achieved by the use of two storage banks. These banks can be overlapped only by taking instructions from one bank and data from another.

Because of the overlapped stores, execution time for individual instructions and sequences of instructions can vary up to 25 per cent above and below average. It is possible, however, to take some advantage of the timing variations by careful planning. The real-time clock system has two registers. One contains the clock itself, and is automatically incremented each millisecond; the other is a Time Limit register. The programmer can arrange for interruptions when the contents of these are equal; he does not have to wait until the actual clock location overflows.

Running more than one program at a time can be achieved by the usual method of adding additional computing modules. However, a number of registers in the processing module make it possible to achieve multi-running safely within the same computing module. These are the bounds registers, which prescribe upper and lower limits of an area that can be used for instructions and data. Reference to data outside these limits can be made, but no instruction can be taken from the out-of-bounds area. The actual programs can be sequenced by means of the interrupt system, using either the real-time clock or the input-output interrupts to initiate change overs.

.13 Availability: . . . . ?

.14 First Delivery: . . . . 1963.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point			
	Add-Subtract:	automatic	binary	1 word.
	Multiply			
	Short:	none.		
	Long, integral:	automatic	binary	2 words.
	Divide			
	No remainder:	none.		
	Remainder, integral:	automatic	binary	2 words.
	Remainder, fractional:	automatic	binary	2 words.
.212	Floating point			
	Add-Subtract:	automatic	binary	36 & 11 bits. or 84 & 11 bits.
	Multiply:	automatic	binary	36 & 11 bits. or 84 & 11 bits.
	Divide:	automatic	binary	36 & 11 bits. or 84 & 11 bits.
.213	Boolean			
	AND:	automatic		1 word.
	Inclusive OR:	automatic	binary	1 word.
	Other logical and mask-type operations:	automatic		1 word.

.214 Comparison

Numbers:	yes	by word or by byte.
Absolute:	yes	by word or by byte.
Letters:	yes	by word or by byte.
Mixed:	yes	by word or by byte.

.215 Code Translation

Code translation from external BCD to internal BCD normally is automatically provided when magnetic tapes recorded in BCD are being read. This is not done in 1604 mode so as to maintain compatibility with the CDC 1604.

Code translation between Hollerith coding and internal BCD is a function of the input-output controller concerned, and details on this are given in the input-output section.

.216 Radix Conversion

Radix conversion between BCD, fixed point binary, or floating point binary (single precision or double precision) is performed by standard program subroutines. Timing details are not available and will depend considerably on the amount of storage which can be allocated to the routines; however, 50 microseconds per number (of 1 through 8 digits) converted fixed point appears to be a conservative estimate for BCD binary conversion, and 30 microseconds for fixed point to floating point conversion.

.217 Edit Format: . . . . . . own coding.

.218 Table Look-Up

Tables in the 3600 may be stored in three ways, depending on the item size. If the item is less than 25 bits the bits are packed together into a series of contiguous words, with as many items in a single word as possible. The item size is defined as a "byte" and the search is made byte by byte; with the search instruction going from word to word as needed.

If the items of the table between 25 and 48 bits (one word), they are stored separately in consecutive words. If the item is longer than a word, an integral number of words is allocated to each item, and the search is handled by incrementing the starting address by a fixed increment (the item size) between each key word to be searched.

.219 List Search

Lists are treated in the CDC 3600 by using part of one item to store the address of the next element in the list. The arrangement of the actual items and addresses is not material, so that items can be included in or dropped from a list by altering one address only.

Lists cannot be searched by a single instruction, but items can be automatically counted and thus the address of the nth item can be determined.

.22 Special Cases of Operands

.221 Negative numbers: . . . 1's complement.

.222 Zero: . . . . positive zero and negative zero.

§ 051.

.223 Operand size determination: . . . . variable may be described in bytes or in 48 or 96-bit words.

.23 Instruction Formats

.231 Instruction structure
The normal instruction on the CDC 3600 is a 24-bit instruction. This is illustrated below and described in Paragraph 232. A number of instructions use different codes. These include:

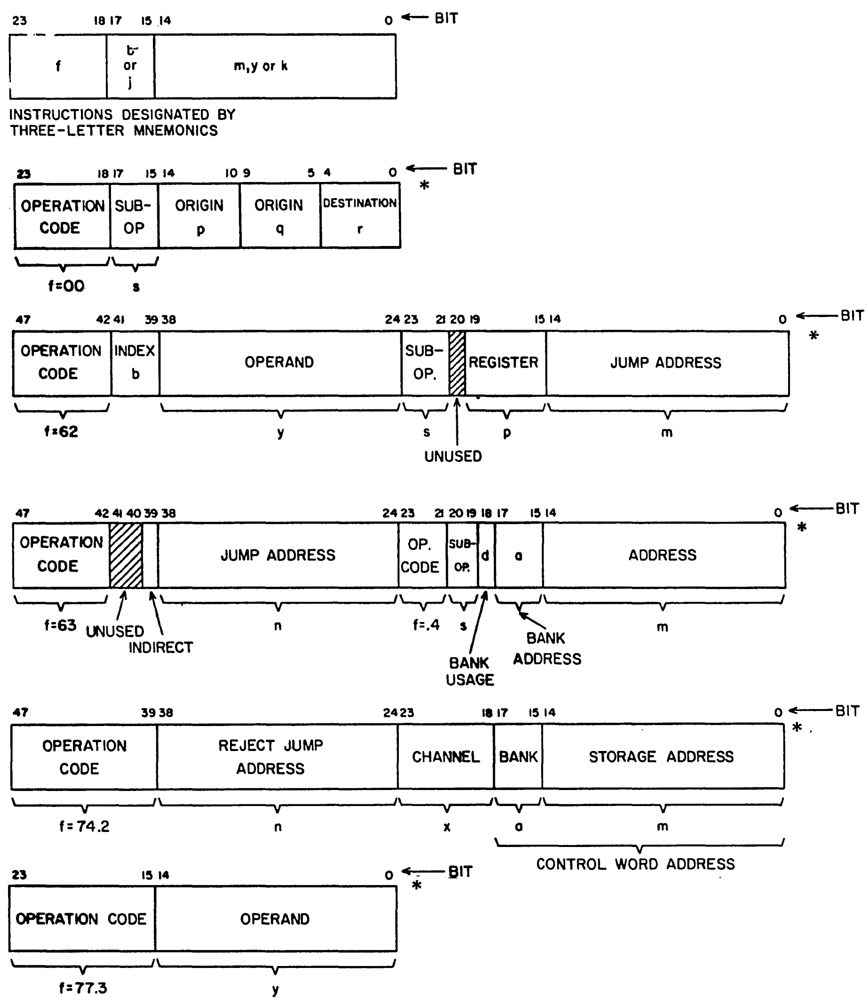
- The Inter Register Instructions (00; with its subsidiary instructions 000 through 006, which control arithmetic or logical operations; instruction 007 which can be a Transmit or Swap operation).

.231 Instruction structure (contd.)

- The Register Jump Instruction 62.
- The Table Search and List Element Locate instruction 63.
- The Bit Sensing and Byte handling instruction 63.
- The Bank Jump instructions 63.
- The Input-Output instructions 74.

These are illustrated below; but their structure is not further described here. Details on these are given in the Instruction List.

.232 Instruction Layout



* Described in Instruction List (Section :121).

§ 051.

.233 Instruction parts

Designator		Use
a	First Bank Address	With first storage address, 'm', specifies an 18-bit composite storage location.
b	First Index	Specifies index register (B) used, or whose contents are used in the operation.
d	Bank Address Usage	Indicates whether or not bank address designators ('a' or 'i') will be interpreted in the operation (if d = 0, not used; d = 1, used).
f	Function Code	A 6 or 9-bit code (depending on the operation) which specifies the operation to be performed.
j	Condition	Conditions operations in jumps and stops.
k	Unmodified Shift Count	Number of shifts to be executed.
m	Unmodified Execution Address (Adress One)	Address of operand.
n	Address Two	Usually used as a jump address.
p	Operand One	Register which holds first operand in Inter-Register and Register Jump instructions.
q	Operand Two	Register which holds second operand in Inter-Register instruction.
r	Destination	Register to which result is sent after specified operation is complete.
s	Sub-operation Code	Specifies one or more sub-operations to be performed. (See individual instructions for interpretations of 's'.)
x	Channel Number	Specifies data channel; also used to specify channel whose status will re read or sensed.
y	Unmodified Operand	Used in execution address portion of instruction; specifies this address will be used as the operand. Specifies a 15-bit comparison quantity in Register Jump instruction. Designates the quantity used as an addend in Add to Exponent instruction.

.234 Basic address structure: 1 + 0, with bank address taken from special register.

.235 Literals

Arithmetic: . . . . . . 15-bit address part.
Incrementing modifiers: . . . . . 15-bit address part.

.236 Directly addressed operands

.2361 Internal storage

Type: . . . . core.
Size: . . . . 48 bits or 96 bits.
Volume accessible: . 1 bank of 16,384 words.

.2362 Increased address capacity: . . . . . . up to 16 banks referenced by change of bank indicator.

.237 Address indexing

.2371 Number of methods: . 1.
.2373 Indexing rule: . . . . . addition modulo store size.
.2374 Index specification: . . 3-bit positions within the instruction to be modified, or in a previous instruction.
.2375 Number of potential indexers: . . . . . . 6.
.2376 Addresses which can be indexed: . . . . . operand addresses in arithmetic, logical, load, and store instructions.
shift counts.
jump locations.
.2377 Cumulative indexing: . yes, more than 1 index register can be involved.
.2378 Combined index and step: . . . . none.

.238 Indirect addressing

.2381 Recursive: . . . . . . yes.
.2382 Designation: . . . . . "7" configuration of the index designator character of the instruction. The new address and index register is that of the lower instruction in the designated word.
.2383 Control: . . . . the last address in the recursive sequence specifies a direct address; i.e., other than a "7" index designator in the lower instruction of the word.
.2384 Indexing with indirect addressing: . . . . . only the last address in the indirect address chain may be modified by indexing.

.239 Stepping

.2391 Specification of increment: . . . . . stepping instructions.
.2392 Increment sign: . . . . minus, plus.
.2393 Size of increment: . . minus unity, plus unity, or plus 15-bit literal in stepping instruction.
.2394 End value: . . . . . . zero, equality.
.2395 Combined step and test: . . . . yes.

§ 051.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size of bits	Program usage
A Register:	1	48	Main Accumulator.
Q Register:	1	48	Second Accumulator.
D Register:	1	48	Used as temporary storage.
6 Index Register:	6	15	
Time Register:	1	27	Real-Time Clock.
Time Limit Register:	1	27	Used to cause interrupts at specific time.
Interrupt Mask Register:	1	48	Inhibition of specific interrupts.
Interrupt Register:	1	48	Interrupts condition for 32 I/O channels and 16 internal conditions.
Instruction Bank Register:	1	3	Bank address added to obtain instruction address.
Operand Bank Register:	1	3	Bank address added to operand address.
Product Register:	1	15	Shows interrupt conditions which are not inhibited.
Shift Count Register:	1	7	Shift Count; destroyed when further instructions are executed.
Miscellaneous Mode Register:	1	15	Hold 6 Console Switch Flags.
All "0":	1	48	
All "1":	1	48	Constants.
"+1":	1	48	

.242

Category of storage	Total number locations	Physical form	Access time (sec)	Cycle time (μsec)
All above:	21	?	?	0.25.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing

.311 Number of sequence control facilities: . . . 1 per processor module.

.315 Sequence control step size: . . . . 1 word; i.e., moves by instruction pairs.

.316 Accessibility to routines: . . . . yes, by means of a "Return Jump" instruction.

.317 Permanent or optional modifier: . . . . yes, instruction bank address.

.32 Look-Ahead: . . . . . . none.

.33 Interruption

The programmer has completed control of the interrupt system of the 3600 and is able to allow or disallow any or all of the interrupt conditions.

The four main types of interrupts are:

Internal computing errors
External conditions in each I/O unit.
Special operating modes (e.g., 1604 mode which traps the 1604 instructions which are not available on the 3600, or the Trace mode).
Real-Time Clock interrupt.

.33 Interruption (Contd.)

The 13 internal interruptible conditions listed in Paragraph .331 cause an interrupt only when a bit is in the appropriate position of the Interrupt Mask Register. Otherwise, they merely set a bit in the Interrupt Register. If the program has allowed the particular type of interrupt, the interrupt system is turned off, and a series of forced jumps are made into the routine handling the specific condition. In all, it is possible for 16 different conditions to be serviced in this way, although, at present, only 13 are specified. Functionally, a typical interrupt has to unload and restore the operational registers it uses, and reactivate the interrupt system before returning to the main program. Typically, approximately 15 microseconds is required for each interrupt occurrence in addition to the time spent in the actual routine.

External interrupts are more complex. Each data channel can cause an interrupt, which cannot be stopped by programming action. After this interrupt has occurred, three forced jumps enter the routine associated with the specific data channel. It is necessary at this point to examine where the interrupt originated. This can be in the data channel itself (a parity error, or the end of a "chained" input-output operation) or in any of the eight units connected to the channel. Two additional forced jumps are used to enter the routine concerned with the specific condition. If the interrupt originated from a specified equipment, it is necessary to read the 12-bit status data into one of the six index registers (which probably has to be unloaded for the purpose) and perform an additional jump before entering the routines. Otherwise, the overhead processing is similar to that for the internal interrupts, but amount to approximately 25 microseconds per interruption in addition to the time required to handle the actual condition.

Subsequent to completion of the routine, the interrupt system is re-activated and any interrupt conditions which have accumulated are examined prior to return to the major routine.

.331 Possible causes

In-out units: . . . . . External Unit in "Ready", "End of File" or "Abnormal end of operation". The meaning of these items is as specified for each individual unit.

In-out controllers: . . power off, missing, or non-functioning.

Program errors: . . . over-capacity shifts.
fixed and floating point operands out of range.
division by zero.
illegal instruction.
illegal reference to locked out area of store.

Processor error: . . . parity error in operand or instruction.

Other conditions: . . . time reading from Real-Time Clock.
Console Operator request.
a jump instruction (when in Trace Mode).
a non 3600 instruction (when in 1604 Mode).

§ 051.

.332 Control by routine

Individual control: . . internal and controller interrupts which are specific in themselves, are set by masks.

Method: . . . . external interrupts are individually chosen by function. Three functions are available for each individual unit. The 3640 Card Reader, for instance, can interrupt when ready, when end-of-file occurs, or when error has occurred. Each of these can be individually set or cleared by the program. If, however, more than one is set, then some cycles are used in addition to the normal interrupt overhead, in housekeeping prior to entering the interrupt routine.

.333 Operator control: . . . none.

.334 Interruption conditions: interruption condition.
specific interrupt approved by program.
interrupt routine not in progress.
interrupt system activated.

.335 Interruption process

Registers saved: . . . sequence control register.

Destination: . . . . . fixed location.

.336 Control methods

Determine cause: . . 2 jumps, in standard sequence identify cause of interrupt OR data channel concerned.

Enable interruption: . program.

.34 <u>Multi-running</u>: . . . . . see description.

.35 <u>Multi-sequencing</u>

.351 Method of control: . . . in general, by providing more than one computing module.

.352 Maximum number of programs: . . . . . . 4 (this would allow only 8 data channels among all four computing modules).

.353 Precedence rules: . . . each independent and with equal access to all stores.

.354 Program protection

Storage: . . . . bounds registers within each module gives upper and lower addresses beyond which reference cannot be made. Can be altered by program.

In-out units: . . . . . none.

.4 PROCESSOR SPEEDS

.41 Instruction Times in μsec

.411 Fixed point

Add-Subtract: 2.1
Multiply: 6.44
Divide: 14.8

.412 Floating point

Add-Subtract: . . . . 4.5 average.
Multiply: . . . . 6.4 average.
Divide: . . . . 13.0 average.

.413 Additional allowance for

Indexing: . . . . none.
Indirect addressing: . 1.0 average, per indirect reference.
Complementing: . . . 0.1
Double Precision Addition/Subtraction: 2.23
Double Precision Multiplication: . . . 22.1
Double Precision Division: 14.1

.414 Control

Branch: 2.1

.415 Counter control

Step: 1.1
Step down and test zero: 2.07
Step up and test equal: 1.69

.418 Shift: 1.44

.42 Processor Performance in μsec

.421 For random addresses	Fixed point	Floating point
$c = a + b$:	6.0	8.4
$b = a + b$:	5.3	8.4
Sum N items:	2.1N	4.5N
$c = ab$:	10.3	10.3
$c = a/b$:	20.0	19.0

.422 For arrays of data	Fixed point	Floating point
$c_i = a_i + b_j$:	9	11.4
$b_j = a_i + b_j$:	8.4	11.4
Sum N items:	2.25 + 4.1N	2.25 + 6.5N
$c = c + a_ib_j$:	15.76	15.76

.423 Branch based on comparison

Numeric data: 7.4
Alphabetic data: . . . 7.4

.424 Switching

Unchecked: 4.0
Checked: 15.6
List search: . . . . . 6.12 + 2.38N

.425 Format control per character (including BCD-binary conversion)

Unpacking: 10
Packing: 15

.426 Table look-up per comparison

For a match: . . . . . 4.12 + 2.38N
For greatest: . . . . . 2.38N (or 4.0 whenever new "greatest" is found).
For least: . . . . . . 5.26N (or 5.1 whenever new "least" is found).
For interpolation point: . . . . 2.38N from most significant end-of-table.

§ 051.

.427 Bit indicators

Set bit in separate location:	1.88
Set bit in pattern:	1.88
Test bit in separate location:	1.88
Test bit in pattern:	1.88
Test AND for B bits:	6.4
Test OR for B bits:	6.4

.428 Moving: . . . . 290,000 48-bit words/second.

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow: Underflow: Zero division: Shift fault: Out-of-bounds instruction: Out-of-bounds operand: Invalid instruction:	check	specific bit set, optionally interrupt occurs; interrupt system deactivated, instruction address stored, and forced jump to specific differing location for each case.
Storage reference: Receipt of data: Internal reject:	parity check	specific bit set, optionally interrupt occurs; interrupt system deactivated, instruction address stored, and forced jump to specific differing location for each case.
Abnormal end of operation on connected I/O device:	check	specific bit set, optionally interrupt occurs; interrupt system deactivated, instruction address stored, and forced jump to specific differing location for each case.

CONSOLE

§ 061.

.1 GENERAL

.11 Identity: . . . . Model 3601 Console.

.12 Associated Units: . . . IBM 731 Selectric Typewriter is built into the console desk.

.13 Description

The operational and the maintenance consoles (see Figures 1 and 2) are mounted on the left and right extensions, respectively, of the V-shaped desk. It is assumed that either the operator or maintenance engineer will be occupying the console desk at one time.

Each console handles only one computing module. If more are connected, special consoles are needed.

The operator can tell at a glance:

- Whether a fault has occurred, and if so, which of 12 types it is.
- Whether the computing module is operating in Standard mode, simulating a 1604, being used in Trace mode (probably for debugging), or is in an interrupt routine.
- Which bits of the D Flag register are set. The display is arranged as an 8 by 6 rectangular array of 48 lamps. The surface of each lamp is labeled with the appropriate bit number and can be easily read.
- The physical conditions inside each of the units, and whether or not the computer will shut off automatically if the temperature exceeds the limits prescribed for the computer.

The operator has available to him:

- The Auto-load button, which loads and enters bootstrap routines from a standard peripheral device.
- Nine sense switches (which can be tested by programs while running) to reflect such information as a program requires about the requisites for the particular run.
- An Interrupt button, which enables him to make any alterations required at any time via the keyboard.
- An "Interlock Bypass" lamp which enables him to bypass the automatic shut-off when the temperature exceeds the prescribed limits.

The console has ample desk space, a good view, and adequate input-output facilities. Supplementary information can be obtained from the maintenance console.

INPUT-OUTPUT: GENERAL

§ 070.

Each input-output unit in the 3600 system has:

- Three different interrupt conditions which, with program permission can cause the program to be interrupted.
- Twelve status bits, which provide the program with precise details concerning the current operating condition of the unit.

Input-Output operations are initiated in the central processor, using the interrupt and status data of the individual unit as guides. The central processor defines the action to be taken (reading or writing), defines an input-output area, and transfers control to the communication module. At this point, the central processor is no longer affected until the operation is ended; however, it can obtain details of the status of the unit and of the portion of the instruction still to be performed at any time. It should be noted that a single instruction can cause many cards to be read to fill up the specified storage area.

The delay to the program caused by any particular input-output unit is literally zero if the input-output area is not in either the instruction core storage bank or the operand bank. The maximum delays are negligible except for the CDC 606 tape unit. When working at high density each tape will utilize one and a half storage cycles out of every hundred. If the same storage bank is used for input-output and for computation, computation can be delayed. The duration of the delay will be proportional to the use of the storage bank during computation. Under worst conditions, the delay will not exceed one and one half per cent of the elapsed time per CDC 606 tape unit. Other details of the maximum delay possible are given below.

Input-Output Area is in the:	Instruction Bank (%)	Operand Bank (%)	Instruction and Operand Bank † (%)
Input-Output Unit ‡ Each CDC 606 Tape Unit (83,400 char/sec)	0.5	1.0	1.5
IBM 088 Card Reader (650 cards/minute)	0.005	0.01	0.015
IBM 088 Card Reader (250 cards/minute)	0.002	0.004	0.006
Punched Paper, Character Mode (350 frames/second)	0.02	0.03	0.05
Line Printer (1,000 lines/minute)	0.012	0.025	0.037

† i.e., the instructions and operands are in the same bank.
‡ The Card Punch, Paper Tape Punch, Console Typewriter all take negligible times.

INPUT-OUTPUT: CDC 3641 CARD READER

§ 071.

.1 GENERAL

.11 Identity: . . . . CDC 3641 Card Reader.

.12 Description

The 3661 Card Reader is an adaptation of the basic CDC-manufactured card reader. (CDC 167 on the 160 systems; CDC 1617 on the 1604 systems). No details of its operational characteristics except its speed (250 cards per minute) have been released.

INPUT-OUTPUT: 3642 CARD PUNCH

§ 072.

.1 GENERAL

.11 Identity: . . . . CDC 3642 Card Punch.

.12 Description

The only detail of information on the 3642 Card Punch which has been issued is its operational speed (100 cards per minute). It can be assumed that the unit will have the ability to cause an interrupt on any of the three standard interruptible conditions for I/O units (Ready, End of File, Abnormal End of Operation) and that the data channel concerned will also be able to initiate interrupts on parity errors, or at the end of a chained input-output operation (i.e., Scatter-Read, Gather-Write).

Provided that there are sufficient data channels available, theoretically, there is no restriction on the number of card punches which can be included in the 256 possible units of input-output equipment which can be connected directly to the system.

INPUT-OUTPUT: CARD READER

§ 074.

.1 GENERAL

.11 Identity: . . . . CDC 3643 Card Reader.
IBM 088 Collator.

.12 Description

This card reader can read 650 cards per minute from either 1 or 2 card feeds with automatic translation of data to BCD form. If two feeds are used, the reading rate is doubled; however, the card read cannot be checked by the program in this case. Normally, both reading stations are used to read the same deck of cards in order to permit an internally programmed card comparison. This action takes approximately 40 microseconds and the ensuing conversion to binary takes 50 microseconds per number. This overhead processing can normally be absorbed within the card read time.

Each read station can be set to interrupt the main processing whenever it is ready, when an abnormal end-of-operation is sensed, or when an end-of-file signal is received. The end-of-file interrupt does not occur when a particular punching code is sensed, but only when an input hopper becomes emptied and a switch is depressed by the operator.

Status bits monitor only four conditions: three standard ones (Ready, Busy, Hopper Empty) and one in which binary-coded (as opposed to Hollerith) cards are being read. The status bit acts as a safeguard against confusing the two types of cards (binary- or Hollerith-coded) which can be read.

Error checking consists of programmed comparison in the actual computer store. No other checking is available. However, as the size of the input area is defined in the original card read instruction, input area overflow cannot occur.

As the operating systems require a card reader to be on-line, either this unit or some other card reader must be included in a system.

.13 Availability: . . . . . . 10 months.

.14 First Delivery: . . . . 1963.

INPUT-OUTPUT: CDC 3691 PAPER TAPE READER/PUNCH

§ 075.

.1 GENERAL

.11 Identity: . . . . CDC 3691 Paper Tape Reader/Punch.

No details have been released for this unit.

INPUT-OUTPUT: CDC 3655 PRINTER

§ 081.

.1 GENERAL

.11 Identity: . . . . CDC 3655 Printer.

.12 Description

The 3655 Printer is an adaptation of the Analex-manufactured CDC 1612 Line Printer, described under the 1604 systems (Section 241:081). No details except its operating speed have been released.

The general method of handling input-output shows that the printer will most probably operate with eight alphameric characters packed into a word. Storage loading is thus minimized during printing to a load of approximately 0.04 per cent of the capacity of a single bank.

INPUT-OUTPUT: CDC 606 MAGNETIC TAPE UNIT

§ 091.

.1 GENERAL

.11 Identity: . . . . Magnetic Tape Unit. CDC 606.

.12 Description

The CDC 606 Magnetic Tape Unit provides the following facilities under program control.

While writing:
(1) Packing density either 200 or 556 rows per inch.
(2) Binary or BCD coding.
(3) Interrupt on: next error, when ready, end of file, or any combination.
(4) Skip bad spot.
(5) Write end-of-file mark.
(6) Rewind with or without interlock.
(7) Automatic conversion between Internal and External BCD.

While reading:
(1) Binary or BCD coding.
(2) Read one file, or one record.
(3) Skip one file or one record, forward or backward.
(4) Interrupt on either next error or when ready.
(5) Rewind with or without interlock.
(6) Automatic conversion between Internal and External BCD.

At any time, individual sense instructions can be used to test for the following conditions:

(1) Parity Error.
(2) Length Error.
(3) End-of-tape mark sensed.
(4) Tape positioned at Load Point.
(5) Interrupt requested on unit.
(6) Unit available.
(7) Certain types of program error have occurred and have been suppressed (e.g., read selection while writing is in progress).

The CDC 606 Magnetic Tape Unit, controlled by the CDC 1615 Control Unit, forms a magnetic tape system.

The 606 has a peak data rate of 83,400 characters per second. At this peak speed, one 606 requires 0.5 per cent of the store module running time.

The tapes are completely compatible with tapes written by IBM 729 units having densities of either 200 or 556 characters per inch. Both CDC and IBM tape units are similar except that the CDC uses pneumatic capstans instead of pinch rollers. Reading and writing can occur only in a forward direction; searching for end of tape, and rewinding can be done

.12 Description (Contd.)

in either direction. The maximum rewind time of a 2,400 foot tape is 80 seconds.

Data is stored in the computer in multiples of eight characters; i.e., sets of full words. If a block being read from tape does not fill an exact number of words, the least significant end of the last word is filled with zeros before being put into the core storage. If this occurs, a length error is recorded and program examination of the Buffer Control Word can determine the cause. However, it is not possible to determine how many zeros have been incorporated in the record. The adding of zeros can never occur when tapes written by CDC 3600 are being used, but can occur when tapes written by other machines (including the CDC 160 and 160-A) are used.

.13 Availability: . . . . . . ?

.14 First Delivery: 1962

.2 PHYSICAL FORM

.21 Drive Mechanism

.211 Drive past the head: . . pneumatic capstan.
.212 Reservoirs
Number: . . . . 2.
Form: . . . . vacuum.
Capacity: . . . . each about 7 feet.
.213 Feed drive: . . . . . . motor.
.214 Take-up drive: . . . . . motor.

.22 Sensing and Recording Systems

.221 Recording system: . . . magnetic head.
.222 Sensing system: . . . . magnetic head.
.223 Common system: . . . 2 heads.

.23 Multiple Copies: . . . . none.

.24 Arrangement of Heads

Use of station: . . . . . erase.
Stacks: . . . . 1.

Use of station: . . . . . recording.
Distance: . . . . 0.4375 inch.
Stacks: . . . . 1.
Heads/stack: . . . . . . 7.
Method of use: . . . . . 1 row at a time.

Use of station: . . . . . sensing.
Distance: . . . . 0.3 inch.
Stacks: . . . . 1.
Heads/stack: . . . . . 7.
Method of use: . . . . . 1 row at a time.

§ 091.

.3 EXTERNAL STORAGE

.31 Form of Storage

.311 Medium: . . . . plastic tape with magnetizable surface.
.312 Phenomenon: . . . . . . magnetization.

.32 Positional Arrangement

.321 Serial by: . . . . 1 to N rows at 200 or 556 rows/inch.
.322 Parallel by: . . . . . . 7 tracks.
.324 Track use
- Data: . . . . 6.
- Redundancy check: . . 1.
- Timing: . . . . 0 (self clocking).
- Control signals: . . . 0.
- Unused: . . . . 0.
- Total: . . . . 7.

.325 Row use
- Data: . . . . 1 to N.
- Redundancy check: . . 1.
- Timing: . . . . 0.
- Control signals: . . . 0 (record and segment marks are optional).
- Unused: . . . . 0.
- Cap: . . . . 0.75-inch interblock gap. 6.0-inch end-of-file mark.

.33 Coding: . . . . BCD mode; 1 tape row per character as in Data Code Table No. 3, even parity.

.34 Format Compatibility: . IBM BCD and binary codes at 200 and 556 rows per inch.

.35 Physical Dimensions

.351 Overall width: . . . . . 0.50 inch.
.352 Length: . . . . 2,400 feet per reel.

.4 CONTROLLER

A variety of controllers can be used, depending on whether 2, 3, or 4 simultaneous data transmissions are required and whether 8 or 16 tape units are to be connected to 1 controller. The maximum practical number of controllers is 32.

.43 Connection to Device: . up to 8 per 1615.

.44 Data Transfer Control

.441 Size of load: . . . . . . 1 to N words, limited by available core storage.
.442 Input-output areas: . . core storage.
.443 Input-output area access: . . . . each word.
.444 Input-output area lockout: . . . . none.
.445 Table control: . . . . . none.
.446 Synchronization: . . . . automatic.

.5 PROGRAM FACILITIES AVAILABLE

.51 Blocks

.511 Size of block: . . . . . 1 to N words, limited by available core storage; 8 rows per word.
.512 Block demarcation
- Input: . . . . gap on tape or cut-off specified in buffer control word.
- Output: . . . . cut-off specified in buffer control word.

.52 Input-Output Operations

.521 Input: . . . . 1 block or file forward, with cut-off available at N words; zeros fill in the last word.
.522 Output: . . . . 1 block forward of N words.
.523 Stepping: . . . . none.
.524 Skipping: . . . . 1 block or file forward. 1 block or file backward. erase 3.5 inches forward (to skip defective tape areas).
.525 Marking: . . . . end-of-file mark, preceded by an automatic 6-inch gap, followed by a longitudinal parity character and the regular interblock gap.
.526 Searching: . . . . none.

.53 Code Translation: . . . matched codes.

.54 Format Control: . . . . none.

.55 Control Operations

- Disable: . . . . only by unload.
- Request interrupt: . . . yes, either for error or when free.
- Select format: . . . . . no.
- Select code: . . . . . . yes, binary mode or BCD mode.
- Rewind: . . . . yes.
- Unload: . . . . yes.

.56 Testable Conditions

- Disabled: . . . . no.
- Busy device: . . . . . . yes.
- Output lock: . . . . . . yes.
- Nearly exhausted: . . . yes, end-of-tape mark indicates a minimum of 8 feet remaining (approx. 20,000 char).
- Busy controller: . . . . no.
- End of medium marks: end-of-tape mark (reflective spot). load point.
- Ready to read: . . . . . yes.
- Ready to write: . . . . yes.
- Error condition: . . . . parity or length error separately.
- Interrupt condition: . . whether selected to interrupt.

§ 091.

.6 PERFORMANCE

.61 Conditions

I: . . . . high density (556 char/inch).
II: . . . . low density (200 char/inch).

.62 Speeds

	Condition	I	II
.621	Nominal or peak speeds:	83,400	30,000.
.622	Important parameters		
	Name		
	Density:	556 char/inch	200 char/inch.
	Start or stop time:	max 4 msec	max 4 msec.
	Full rewind time:	1.3 min.	1.3 min.
	Interblock gap:	0.75 inch	0.75 inch.
.623	Overhead:	max 8 msec/ block	max 8 msec/ block.
.624	Effective speed, characters/sec:	83,400N/(N + 698) (See Graph)	30,000N/ (N + 240).

.63 Demands on System

Component	Condition	msec per word or	Percentage
Core Store:	I	.0015	1.5.
Core Store:	II	.0015	0.6.

.7 EXTERNAL FACILITIES

.71 Adjustments

Adjustment: . . . . . . recording density.
Method: . . . . switch.
Comment: . . . . selects high or low density, but is overridden by program changes.

.72 Other Controls

Function	Form	Comment
Unit Number Selector:	dial	select 1 of 8 addresses.
File protection ring:	plastic ring affixed to tape reel	absence of ring inhibits tape writing.
Load Point:	button	lowers tape into reservoirs and winds tape forward to load point.
Unload:	button	removes tape from reservoirs and raises upper portion of head assembly.

.73 Loading and Unloading

.731 Volumes handled
Storage: . . . . reel.
Capacity: . . . . 2,400 feet; for 1,000 char blocks, 5,000,000 at 200 char/inch; 11,300,000 chars at 556 char/inch.

.732 Replenishment time: . . 1.0 minute.

.734 Optimum reloading period: . . . . 4 minutes.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Recording:	read after write with lateral parity check	interrupt.
Reading:	lateral and longitudinal parity checks	interrupt.
Input area overflow:	check	stop transfer, interrupt.
Output block size:	present.	
Invalid code:	check	interrupt.
Exhausted medium:	reflective spot on tape	interrupt.
Imperfect medium:	none.	
Timing conflicts:	none.	
Parity error:	check	interrupt.

DATA CHANNEL CONVERTERS

§ 101.

.1 IDENTITY: . . . . CDC 3681, 3682 Data Channel Converters.

.11 General

These Data Channel Converters can have the following functions:

(1) To permit a CDC 160 or 160-A to use 3600-type peripherals. One or two 3681 converters are connected to a 160 or 160-A computer and then operate as 3600 data channels. (See Figure 1).

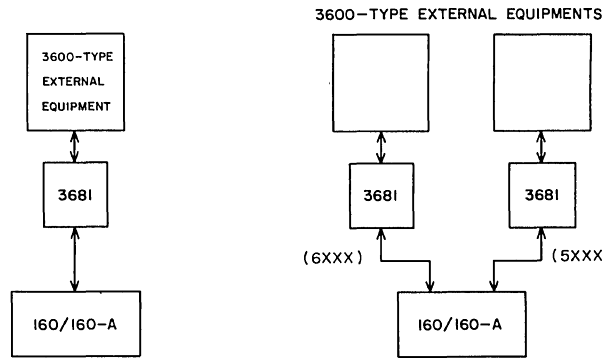


Figure 1. Non-Satellite System

(2) To permit a CDC 160 or 160-A to be connected as a satellite computer which is able to receive or transmit data from the storage of a 3600 system. This arrangement requires a 3681 data channel converter and an additional 3682 converter. The 3681 simulates a 3601 data channel, and the 3682 interconnects two 3606 data channels; the 3681 handles the necessary control and checking information. (See Figure 2).

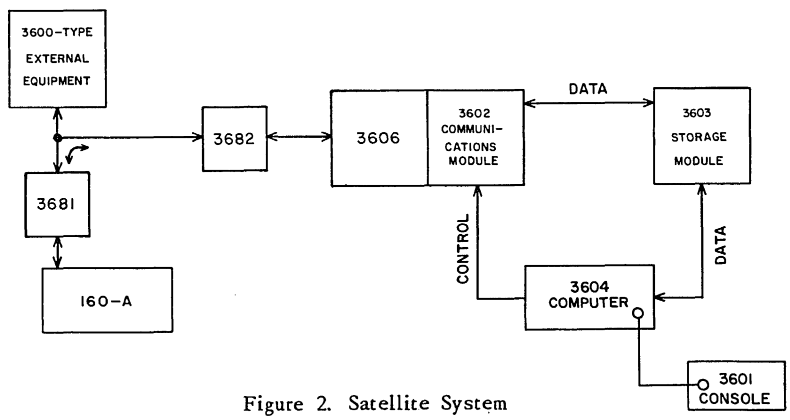


Figure 2. Satellite System

(3) To connect one 3600 system with another 3600 system, permitting transfer of data between the systems. This only requires a 3682 data channel converter. (See Figure 3).

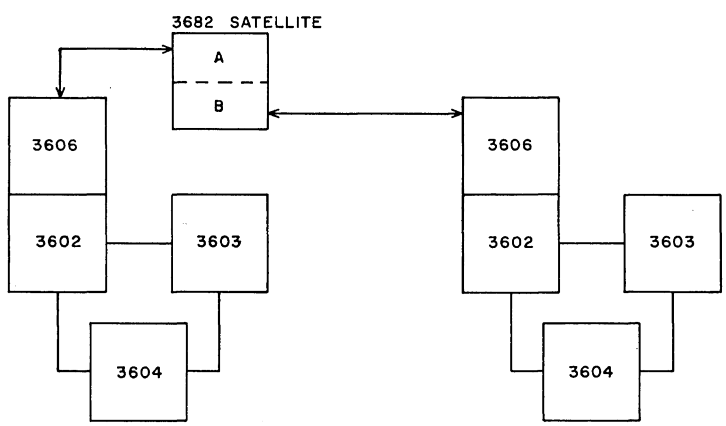


Figure 3. Typical 3682 Configuration

Configuration Possibilities

Either one or two 3681 converters can be connected to a 160/160-A computer. Up to eight 3682 converters can be connected to a data channel or to a 3681 converter

INPUT-OUTPUT: PROGRAM CONTROLLED INPUT-OUTPUT TYPEWRITER

§ 102.

.1 GENERAL

.11 Identity: . . . . CDC 3692 Program Controlled Input-Output Typewriter.

No details have been released for this unit.

SIMULTANEOUS OPERATIONS

§ 111.

.1 GENERAL

All CDC 3600 input-output operations can proceed simultaneously with computation, irrespective of the number of input-output channels or the number of computation modules used. However, the number of magnetic tapes running at a given time is restricted by the number of data channels. At present two-, three-, or four-channel controllers are available, so that from two to four tapes from each controller can be operational in any combination, in addition to all non-magnetic-tape peripherals and the central processor(s). A maximum of 32 data channels can be used.

As noted in INPUT-OUTPUT: GENERAL (Section 247:070), these operations need cause no computational or input-output delay whatsoever, even when all 32 possible input-output channels are in use. The maximum delay in the worst case approximates a percentage equal to 1.5 times the number of CDC 606 tape units in use, with a built-in maximum of 80 percent. (The maximum cannot be reached with the present tape decks.) This condition occurs when all tape units are using the same core storage bank as both the instruction and the data.

.2 RULES

The following processes can take place simultaneously:

As many computations as there are computing modules, plus

As many card, paper tape, or equivalent operations as there are data channels connected to these units (Maximum of 32), plus

As many tape reads or tape writes as there are data channels attached to the tape synchronizers (each synchronizer can have two, three, or four channels each).

INSTRUCTION LIST

§ 121.

These instructions are extracted from Preliminary Reference Manual. The effect of most instructions can be changed by using the Augment Instructions. This and the other instructions which are identified thus: ⟶ are further defined in the appendix to the instruction code.

	Octal Code	Mnemonic Code	Name	Indirect Addressing	Storage* References	Address Modification	Number of Instruction Bits
		Inter-Register Transmission					
⟶	00	ROP	Inter-Register	No	0		24
		Full-Word Transmission					
	12	LDA	Load A	Yes	1	Yes	24
	16	LDQ	Load Q	Yes	1	Yes	24
	20	STA	Store A	Yes	1	Yes	24
	21	STQ	Store Q	Yes	1	Yes	24
	13	LAC	Load A, Complement	Yes	1	Yes	24
	17	LQC	Load Q, Complement	Yes	1	Yes	24
⟶	63.2	XMIT	Transmit	No	2	No	48
⟶	63.2	———	Transmit Augment	No	2r	Yes	48
		Address Transmission					
	53	LIL	Load Index (lower)	Yes	1	No	24
	52	LIU	Load Index (upper)	Yes	1	No	24
	57	SIL	Store Index (lower)	Yes	1	No	24
	56	SIU	Store Index (upper)	Yes	1	No	24
	61	SAL	Substitute Address (lower)	Yes	1	Yes	24
	60	SAU	Substitute Address (upper)	Yes	1	Yes	24
	50	ENI	Enter Index	Yes	0	No	24
	04	ENQ	Enter Q	Yes	0	Yes	24
	10	ENA	Enter A	Yes	0	Yes	24
		Instruction Augment					
⟶	77.1	———	Single Precision Augment	Yes	0	Yes†	24
⟶	77.2	———	Double Precision Augment	Yes	0	Yes†	24

* If indirect addressing is designated, at least one additional storage reference is required.
† On lower address.
r Number of repetitions of the operation.
⟶ Defined in Appendix.

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Octal Code	Mnemonic Code	Name	Indirect Addressing	Storage References	Address Modification	Number of Instruction Bits
	Fixed Point Arithmetic					
14	ADD	Add	Yes	1	Yes	24
15	SUB	Subtract	Yes	1	Yes	24
24	MUI	Multiply Integer	Yes	1	Yes	24
26	MUF	Multiply Fractional	Yes	1	Yes	24
25	DVI	Divide Integer	Yes	1	Yes	24
27	DVF	Divide Fractional	Yes	1	Yes	24
--	--	Truncated Divide				
	Single Precision Floating Point Arithmetic					
30	FAD	Floating Add	Yes	1	Yes	24
31	FSB	Floating Subtract	Yes	1	Yes	24
32	FMU	Floating Multiply	Yes	1	Yes	24
33	FDV	Floating Divide	Yes	1	Yes	24
77.3	ADX	Add to Exponent	No	0	Yes	24
	Double Precision Floating Point Arithmetic					
77.2-30	DFAD	Floating Add	Yes	2	Yes	48
77.2-31	DFSB	Floating Subtract	Yes	2	Yes	48
77.2-32	DFMU	Floating Multiply	Yes	2	Yes	48
77.2-33	DFDV	Floating Divide	Yes	2	Yes	48
	Address Arithmetic					
11	INA	Increase A	Yes	0	Yes	24
51	INI	Increase Index	Yes	0	No	24
54	ISK	Index Skip	Yes	0	No	24
	Logical					
40	SST	Selective Set	Yes	1	Yes	24
41	SCL	Selective Clear	Yes	1	Yes	24
42	SCM	Selective Complement	Yes	1	Yes	24

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Octal Code	Mnemonic Code	Name	Indirect Addressing	Storage References	Address Modification	Number of Instruction Bits
43	SSU	Selective Substitute	Yes	1	Yes	24
44	LDL	Load Logical	Yes	1	Yes	24
45	ADL	Add Logical	Yes	1	Yes	24
46	SBL	Subtract Logical	Yes	1	Yes	24
47	STL	Store Logical	Yes	1	Yes	24
	Shifting					
01	ARS	A Right Shift	Yes	0	Yes	24
02	QRS	Q Right Shift	Yes	0	Yes	24
03	LRS	Long Right Shift (AQ)	Yes	0	Yes	24
05	ALS	A Left Shift	Yes	0	Yes	24
06	QLS	Q Left Shift	Yes	0	Yes	24
07	LLS	Long Left Shift (AQ)	Yes	0	Yes	24
34	SCA	Scale A	Yes	0	No	24
35	SCQ	Scale AQ	Yes	0	No	24
	Replace					
70	RAD	Replace Add	Yes	2	Yes	24
71	RSB	Replace Subtract	Yes	2	Yes	24
72	RAO	Replace Add One	Yes	2	Yes	24
73	RSO	Replace Subtract One	Yes	2	Yes	24
	Storage Test					
36	SSK	Storage Skip	Yes	1	Yes	24
37	SSH	Storage Shift	Yes	2	Yes	24
	Search					
64	EQS	Equality Search	Yes	n	Yes †	24
65	THS	Threshold Search	Yes	n	Yes †	24
66	MEQ	Masked Equality Search	Yes	n	Yes †	24

† If b = 0, only the word at 'm' is searched; if $(B^b) = 0$, no search is made.
n Number of words searched.

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	Octal Code	Mnemonic Code	Name	Indirect Addressing	Storage References	Address Modification	Number of Instruction Bits
	67	MTH	Masked Threshold Search	Yes	n	Yes †	24
→	63.4	SEQU	Equality Search	Yes	n	Yes	48
→	63.4	SMEQ	Masked Equality Search	Yes	n	Yes	48
→	63.4	SEWL	Search Within Limits	Yes	n	Yes	48
→	63.4	SMWL	Search Magnitude Within Limits	Yes	n	Yes	48
→	63.3	LSTU LSTL	Locate List Element	Yes	n	Yes	48
		Jumps and Stops					
	22	AJP	A Jump	Yes	1*	No	24
	23	QJP	Q Jump	Yes	1*	No	24
	55	IJP	Index Jump	Yes	0	No	24
	75	SLJ	Selective Jump	Yes	1*	No	24
	76	SLS	Selective Stop	Yes	1*	No	24
→	63.7	EXEC	Execute	Yes	0 + x	Yes	48
	62	RGJP	Register Jump	Yes	0	Yes	48
→	77.6	DRJ	D Register Jump	No	0	No	24
→	63.6	NBJP ZBJP	Bit Sensing	Yes	0	Yes	48
		Bank Jumps					
	63.0	UBJP	Unconditional Jump	Yes	0	Yes	48
	63.0	BRTJ	Unconditional Return Jump	Yes	1	Yes	48
	63.1	BJPL	Unconditional Jump Lower	Yes	0	Yes	48
	63.0	BJSX	Jump and Set Index	Yes	1	Yes	48

† If b = 0, only the word at 'm' is searched; if $(B^b) = 0$, no search is made.
n Number of words searched.
* Return jump only.
x Number of storage references required by the executed instruction(s).
→ Defined in Appendix.

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Octal Code	Mnemonic Code	Name	Indirect Addressing	Storage References	Address Modification	Number of Instruction Bits
	Variable Data Field					
→ 63.5	LBYT	Load Byte	Yes	1	Yes	48
→ 63.5	SBYT	Store Byte	Yes	2	Yes	48
→ 63.5	SCAN	Scan Byte	Yes	s	Yes	48
	Interrupt					
77.4	MPJ	Main Product Register Jump	No	0	No	24
77.5	CPJ	Channel Product Register Jump	No	0	No	24
	Input/Output					
74.0	CONN	Connect	No	0	No	48
74.1	EXTF	Function	No	0	No	48
74.2	BEGR	Read	No	0	No	48
74.3	BEGW	Write	No	0	No	48
74.4	COPY	Copy Status	No	0	No	48
74.5	CLCH	Channel Clear	No	0	No	48
74.6	IPA	Input to A	No	0	No	24
74.7	ALG	Perform Algorithm	No	0	No	24
77.0	INF	Internal Function	No	0	No	24
77.7	FAUL	Fault	No	0	No	24

s Number of words scanned.
→ Defined in Appendix.

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SYMBOLS

The following symbols are used in the List of Instructions.

A	The A register
A_n	The binary digit in position 'n' of the A register
B^b	Designated first index register
D	Auxiliary register; also referred to as the Flag register
Exit (full)	Proceed to upper instruction of next program step
Exit (half)	Proceed to lower instruction of same program step
Exit (skip)	Proceed to upper instruction of next program step plus one
Exit (jump)	Proceed to the address specified by the execution address
LA	Lower address; execution address portion of lower instruction of a program step
Q	Auxiliary Arithmetic register
UA	Upper address
V^v	Designated second index register
( )	Contents of a register or storage location
( )'	One's complement contents of a register or storage location
( )f	Final contents of a register or storage location
( )i	Initial contents of a register or storage location
#	A flag to denote the instruction must be located in the upper instruction position of an instruction word
$\vee$	The logical inclusive OR function
$\dot{\vee}$	The logical exclusive OR function
$\wedge$	The logical AND function
$\supset$	The logical implication function
$\equiv$	The logical equivalence function

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CDC 3643 CARD READER

CONNECT	Connect Reader 1, Equipment N	N001
	Connect Reader 2, Equipment N	N002
	Release Reader 1, Equipment N	N010
	Release Reader 2, Equipment N	N020
FUNCTION	Set Interrupt On Ready	0001 (bit 0)
	Clear Interrupt On Ready	000$\overline{1}$ ($\overline{\text{bit 0}}$)
	Set Interrupt On End of File	0002 (bit 1)
	Clear Interrupt On End of File	000$\overline{2}$ ($\overline{\text{bit 1}}$)
	Set Interrupt On Abnormal End of Operation	0004 (bit 2)
	Clear Interrupt On Abnormal End of Operation	000$\overline{4}$ ($\overline{\text{bit 2}}$)
	Negate Automatic Hollerith To Internal BCD Conversion	0010 (bit 3)
	Release Negation	00$\overline{1}$0 ($\overline{\text{bit 3}}$)
STATUS	Reader Ready	0001
	Reader Busy	0002
	Binary Card	0004
	End of File	0010

CONSOLE TYPEWRITER

CONNECT	
Connect Equipment N	NXXX
FUNCTION	
Set Interrupt On Abnormal Operation	XX01
Clear Interrupt On Abnormal Operation	XX02
Clear Interrupt	XX04
Set Interrupt On End of Write	XX10
Clear Interrupt On End of Write	XX20
STATUS	
Busy	XXX2
End of Line	XX4X
Selected For Input To A	XXX1
Upper/Lower Case	XXX4
Type Parity Error	2XXX

§ 121.

CDC 362X MAGNETIC TAPE CONTROLLERS

TAPE MOTION	
Rewind	0010
Rewind Unload	0011
Backspace	0012
Search File Mark Forward	0013
Search File Mark Reverse	0014
Write End of File Mark	0015
Skip Bad Spot	0016
FORMAT	
Release	0000
Binary	0001
Coded	0002
High Density	0003
Low Density	0004
Clear	0005
INTERRUPT	
Interrupt On Ready	0020
Release Interrupt On Ready	0021
Interrupt On End of Operation	0022
Release Interrupt On End of Operation	0023
Interrupt On Abnormal End of Operation	0024
Release Interrupt On Abnormal End of Operation	0025

STATUS REPLIES	
XXX1	Ready
XXX2	R/W Control and/or Busy
XXX4	Density ("1" in bit 2 indicates Hi, "0" in bit 2 indicates Lo)
XX1X	File Mark
XX2X	Load Point
XX4X	End of Tape
X1XX	Write Enable
X4XX	Lost Data
1XXX	Longitudinal Parity Error
2XXX	Vertical Parity Error
4XXX	Reserve Reject

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APPENDIX TO INSTRUCTION LIST

INTER-REGISTER TRANSMISSION (ROP)

Bit 23–18	17–15	14–10	9–5	4–0
OPERATION CODE	SUB-OP	ORIGIN p	ORIGIN q	DESTINATION r
f=00	s			

The 24-bit Inter-Register Transmission instruction performs an operation, 's', upon operands 'p' and 'q', and places the result in 'r'. Origin (operand) or destination registers are indicated below according to their octal values of 'p', 'q', and 'r'.

00 - Time Limit Register
01 - B^1
02 - B^2
03 - B^3
04 - B^4
05 - B^5
06 - B^6
07 - A Lower Address
10 - A Upper Address
11 - Q Lower Address
12 - Q Upper Address
13 - A Full
14 - Q Full
15 - D Full
16 - Bounds Register
17 - Interrupt Mask Register

The registers indicated below must be used for operands only.

20 - Interrupt Register
* 21 - All "0's"
* 22 - +1
* 23 - All "1's"
24 - Instruction Bank Register
25 - Operand Bank Register
26 - Shift Count Register
27 - Miscellaneous Mode Selections
30 - P Register
31 - Time Register

The operations which may be performed are listed below according to their octal values of 's'.

s = 0 Register Or $p \vee q \rightarrow r$
Forms the logical OR of operands 'p' and 'q' and places the result in 'r'.

s = 1 Register Exclusive Or $p \veebar q \rightarrow r$
Forms the logical exclusive OR of operands 'p' and 'q' and places the result in 'r'.

* All "0's", +1, and all "1's" are not registers, but are forced operands which may be referenced in an operation.

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s = 2 Register And $p \wedge q \rightarrow r$
Forms the logical AND of operands 'p' and 'q' and places the result in 'r'.

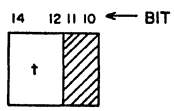
s = 3 Register Implication $p \supset q \rightarrow r$
Forms the logical implication of operands 'p' and 'q' and places the result in 'r'.

s = 4 Register Equivalence $p \equiv q \rightarrow r$
Forms the logical equivalence of operands 'p' and 'q' and places the result in 'r'.

s = 5 Register Sum $p + q \rightarrow r$
Adds the contents of 'p' to the contents of 'q' and places the result in 'r'.

s = 6 Register Difference $p - q \rightarrow r$
Subtracts the operand 'q' from 'p' and places the result in 'r'.

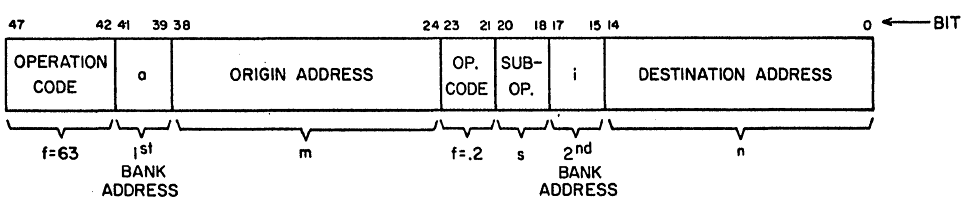
s = 7 Register Transmit/Swap (RXT/RSW)
Uses register designators 'q' and 'r' only. The unused 'p' portion of the Inter-Register instruction format becomes a function modifier with the following designator:



Values for the 't' designator are:

0 Swap (q) and (r); do not clear q; do not clear r
1 Swap (q) and (r); do not clear q; clear r
2 Swap (q) and (r); clear q; do not clear r
3 Swap (q) and (r); clear q; clear r
4 Transmit (q) to r; do not clear q; do not clear r
5 Transmit (q) to r; do not clear q; clear r
6 Transmit (q) to r; clear q; do not clear r
7 Transmit (q) to r; clear q; clear r

TRANSMIT COMMANDS AND TRANSMIT AUGMENT (XMIT)



The Transmit commands read an operand from the storage location designated by the first storage address 'a m', perform the specified operations, and place the results in storage address 'i n'. At the end of the operation, the Operand Bank register is set to 'i'. Interpretations of the 3-bit suboperation designator 's' are given below (the lower-order two bits of 's' specify the operation):

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s = X00 Transmit

The contents of storage location 'a m' are transmitted to storage location 'i n'. The contents of 'a m' remain unchanged.

s = X01 Transmit Complement

The complement of the contents of storage location 'a m' are placed in storage location 'i n'. The contents of 'a m' remain unchanged.

s = X10 Transmit Masked

The logical product of the contents of storage location 'a m' and Q is placed in storage location 'i n'. The contents of 'a m' remain unchanged.

s = X11 Transmit + Constant

The contents of storage location 'a m' are added to a constant (constant is in A) and transmitted to storage location 'i n'. The contents of 'a m' remain unchanged.

Values for the upper order bit of 's' are:

- s = 0XX Execute the specified Transmit command without augmentation.
- s = 1XX Augment the specified Transmit command.

The augment portion of this instruction may be used to increase the capability of the designated command. Commands may be executed without using the augment capability; in this case, just one word is transmitted.

With augmentation selected, the specified Transmit operation may be repeated a given number of times. Storage addresses may be increased by an increment quantity for each repetition of the operation. Five index registers are assigned to hold the necessary control quantities for an augmented Transmit operation. These registers must be loaded with the appropriate control quantities prior to executing this instruction. Index register assignment is as follows:

B^1 - Holds word count; i.e., the number of words to be transmitted. Its contents are reduced by one after each operation. When $(B^1) = 0$, the operation is complete.

B^2 - Holds new origin address modifier (increment in B^3 has been added to old origin address). Normally, this index register is clear at start.

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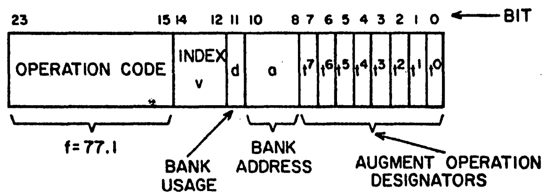
SINGLE PRECISION AUGMENT



The 24-bit Single Precision Augment command may be used to perform one or more of the following operations:

1) Increase the capabilities of certain instructions by specifying additional operations to be performed.
2) Change the value of the Operand Bank register.
3) Provide additional modification of the address portion of the lower instruction.

When this command is used in the lower instruction position of a program step (case 2 above), the following operations occur:

1) The value of the Operand Bank register is set to 'a' (if 'd' is a "1").
2) All other designators perform no meaningful operations and have no effect on subsequent instructions.

When this command is used in the upper instruction position of a program step (case 1 above), the following operations occur:

1) The value of the Operand Bank register is set to 'a' (if 'd' is a "1").
2) Operations using the index designator 'v' are performed (refer to table 3-3).
3) The augment operation designators 't' are stored to condition the operation of the lower instruction being augmented.

Instructions which may be augmented using 'v' and the augment designators 't' are listed in tables 3-4 and 3-5. Designators which may be used when augmenting a given instruction are checked opposite that instruction. Augment operation designators are tabulated below.

§ 121.

TABLE 3-2. AUGMENT OPERATION DESIGNATORS

Designator	Value If a "0"	If a "1"
d	Bank address not used	Bank address is used; the value of the bank address designator 'a' is always placed in the Operand Bank register.
t^0	Rounded arithmetic	Un-rounded arithmetic*
t^1	Normalized arithmetic	Un-normalized arithmetic
t^2	Use signed operand	Use magnitude of operand (positive value)
t^3	Leave source alone	Clear source (source is always a register)
t^4	Do not complement operand	Complement operand
t^5	Do normal operation	Do replace operation
t^6	Direction of shift determined by lower instruction operation code (normal).	Direction of shift determined by lower instruction operation code as modified by operand sign value (i. e., if $k + (B^b) + (V^v)$ is a negative value, reverse the direction of the shift being augmented).
t^7	Shift being augmented is end around (left shift) or end-off and sign extended (right shift).	Shift being augmented is end-off (left or right) or sign not extended (right shift).

* If augmenting Divide Fractional instruction, execute Truncated Divide.

When the Augment command is in the upper instruction position of a program step, the index designator 'v' may be used in the following manner to augment the lower instruction.

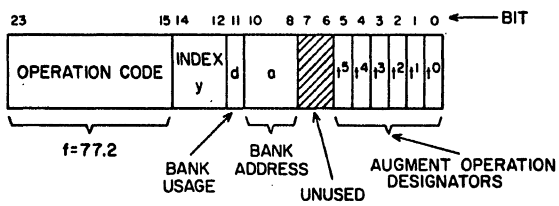
TABLE 3-3. AUGMENT OPERATION WITH 'v'

Value	Operation
v = 0	If v = 0, this designator has no significance in the operation.
v = 1-6	If v = 1-6, address modification rules apply. The contents of the index register specified by 'v' are added to the address portion (bits 00-14) of the lower instruction to form M, Y, or K, whichever the case.
v = 7	If v = 7, indirect addressing rules apply. The quantity held in the address portion (bits 00-14) of the lower instruction is treated as a storage address (whether 'm', 'y', or 'k'). The lower 18 bits at this storage address are read from storage and: a) The upper 3 bits (new 'v') are placed in the 'v' designator position of the augment instruction. b) The lower 15 bits are placed in the address portion of the lower instruction. If new v = 7, indirect addressing continues until completed; if new v = 1-6, address modification is performed.

Upon completing the operations specified by the upper (Augment) instruction, the address portion of the lower instruction now contains a modified value (if 'v' specified indirect addressing or address modification). When the instruction being augmented (the lower instruction) is executed, its index designator is interpreted in the normal manner. Indirect addressing or address modification is performed on the address modified by the Augment operation.

§ 121.

DOUBLE PRECISION AUGMENT



The 24-bit Double Precision Augment command is used in the same manner as the Single Precision Augment command. Instructions which may be augmented by this command are listed in table 3-6. Operations in this instruction category are performed on 96-bit operands. Designators which may be used when augmenting a given instruction are checked opposite that instruction. Augment operation designators are listed in table 3-7.

TABLE 3-6. AUGMENTABLE INSTRUCTIONS

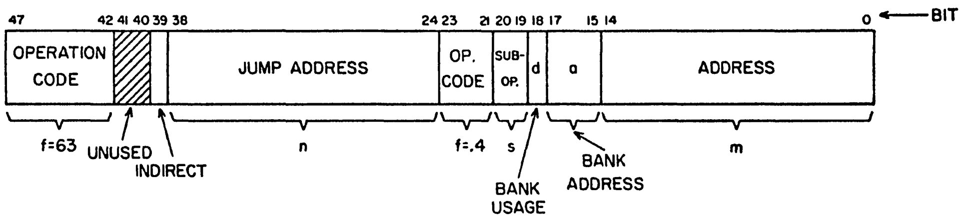
Instruction to be Augmented	t^5	t^4	t^3	t^2	t^1	t^0
LDA		X		X		
STA		X	X	X		
FAD	X	X		X	X	X
FSB	X	X		X	X	X
FMU		X		X	X	X
FDV		X		X		X

TABLE 3-7. AUGMENT OPERATION DESIGNATORS

Designator	Value: If a "0"	If a "1"
t^0	Rounded arithmetic	Un-rounded arithmetic
t^1	Normalized arithmetic	Un-normalized arithmetic
t^2	Use signed operand	Use magnitude of operand
t^3	Leave source alone	Clear source
t^4	Do not complement operand	Complement operand
t^5	Do normal operation	Do replace operation
d	Bank address not used	Bank address is used; the value of the bank address designator 'a' is always placed in the Operand Bank register.

§ 121.

SEARCH ORDER



Four search operations are conditioned by the designator 's'.

s = 0 Equality Search (SEQU) s = 2 Search Within Limits (SEWL)

s = 1 Masked Equality Search (SMEQ) s = 3 Search Magnitude Within Limits (SMWL)

Each of these operations searches a list of operands to find one that satisfies the specific criterion. These items may be in sequential or incremented (other than 1) addresses. The first item is in the location specified by starting address 'a m' + B^2.

If bit 39 is a "1", indirect addressing is used to determine the starting address. The contents of index register B^2 are added to 'm' to form 'a M'. The storage word at address 'a M' is the address of the storage word to be searched. If bit 39 is a "0", operation proceeds without indirect addressing. (B^1) is reduced one count for each word that is searched until an operand is found that satisfies the criterion or until B^1 equals zero. If the search is terminated by finding an operand which meets the criterion, an exit is performed to the next instruction. The address of the operand that meets the criterion is $m + (B^2) - (B^3)$. If no operand in the list is found that meets the criterion, a jump is executed to the location specified by the jump address 'n' (jump is effected within the same storage bank).

Three index registers used in the search operations are assigned as follows:

B^1 - Holds the word count; i. e., the number of words to be searched.

B^2 - Holds the new operand address modifier (the increment has been added to the old address modifier).

B^3 - Holds the increment quantity; i. e., the quantity which will be added to the operand address modifier to specify a new operand address.

Index register values are set by program, prior to executing the Search instruction.

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The search operations are:

s = 0 Equality Search (M) = (A)

Searches a list of operands to find one such that (M) is equal to (A).

s = 1 Masked Equality Search L(Q)(M) = (A)

Searches a list of operands to find one such that the logical product of (M) and (Q) is equal to (A).

s = 2 Search Within Limits $(A) \geq (M) > (Q)$

Searches a list of operands to find one whose value lies between (A) and (Q).

s = 3 Search Magnitude Within Limits $(A) \geq |(M)| > (Q)$

Searches a list of operands to find one whose absolute magnitude lies between (A) and (Q). (Magnitude refers to the magnitude of signed operands.)

The flow diagram below outlines the sequence of events during a typical search operation.

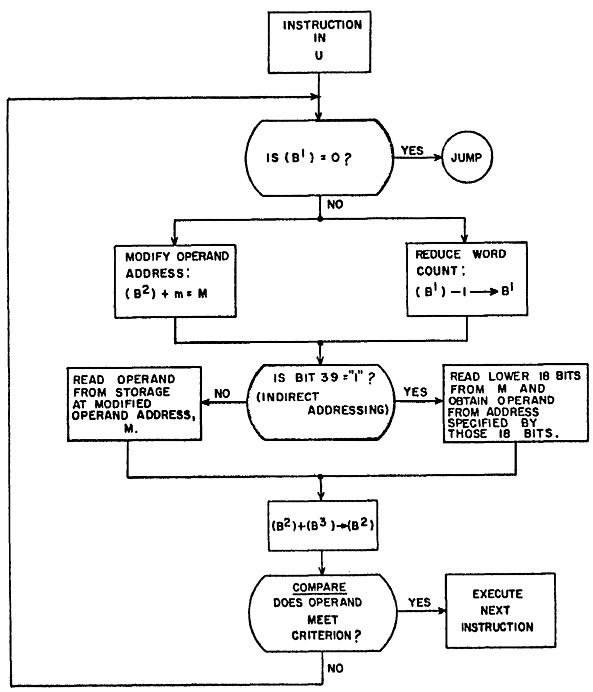
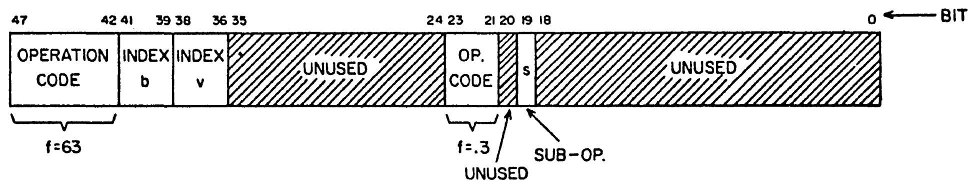


Figure 3-4. Sequencing for 63.4 Search Operations

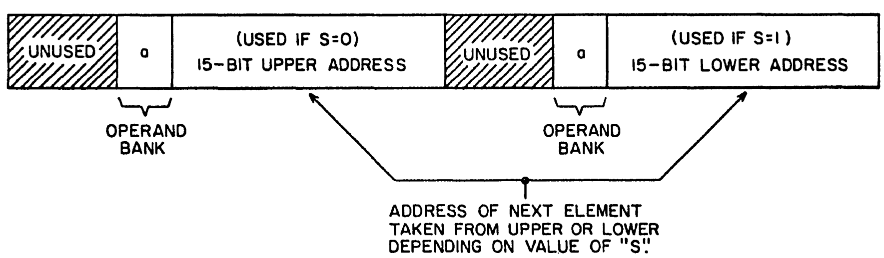
§ 121.

LOCATE TEST ELEMENT (LSTU, LSTL)



This instruction may be used to locate elements of a list when the elements are scattered throughout a storage bank or throughout several storage banks. An element of the list contains two parts: (1) data, and (2) the location (storage address) of the next element of the list. An element may occupy one storage word or several. If the element occupies several storage words, the words are usually in consecutive storage locations.

The format of the word holding an element (or the format of the first word if the element occupies several words) is as follows:



Note that the format permits several options for positioning data within the word:

1) If the lower 18 bits are used to specify the address of the next element (s = 1 in the instruction word), the entire upper 30 bits may be used to hold data.

2) If the upper address portion is used to specify the address of the next element (s = 0 in the instruction word), the lower 24 bits and the uppermost 6-bit portion may be used to hold data.

Interpreting data is determined by the list containing it, its location in a particular list, or by an identifying tag in the data portion of the element.

§ 121.

Executing the Locate List Element instruction locates the 'nth' element of the list.

Before executing the Locate List Element instruction, two operations must have been accomplished. These are:

1) The first element of the list is located at the storage address designated by the contents of V^v. (The first element must be in the storage bank currently in use as the operand bank.) Therefore, this index register must be loaded with the appropriate address before executing this instruction.

2) A second index register (designated by B^b) holds the count field; i.e., a count 'n' to enable locating the 'nth' element. Thus, the programmer must load B^b with 'n' before the operation.

Operation then proceeds as follows:

1) Read element from storage at address specified by (V^v).

2) Examine (B^b). If (B^b) = 0, the 'nth' element has been located and the operation is complete. If (B^b) $\neq$ 0, reduce (B^b) by one.

3) If s = 0 (refer to instruction format), replace the old (V^v) with the upper address portion of the new storage word (refer to the format of the word holding an element).

If s = 1, replace the old (V^v) with the lower address portion of the new storage word.

NOTE

> Once the value of 's' is set in the instruction word, it cannot be changed during the course of the instruction. For example, if 's' is set to "1", the lower address portion of the storage word will be used to locate the next element each time until the 'nth' element is located.

4) Examine (V^v). If the new (V^v) = 0, the operation is complete. (The programmer must previously have loaded all zeros in the designated address portion of the last storage word of the list.) Address 00000 may be used as the first list element location, but operation will halt (since the check on V^v occurs after the first storage reference) if address 00000 is used to locate a subsequent list element.

§ 121.

If $(V^v) \neq 0$, (V^v) now designates the address of the next element. Also, if the new $(V^v) \neq 0$, the Operand Bank register is switched to 'a' (where 'a' is the bank designator adjacent to the designated address portion of the storage word).

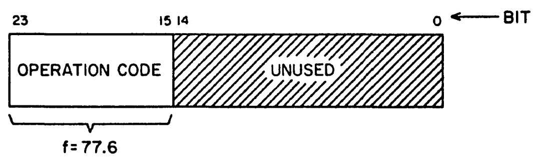
5) Return to step 1.

At the end of operations:

1) If the 'nth' element has been located, B^b holds a count of zero, V^v holds the address of the 'nth' element, and the Operand Bank register is set to the bank containing that element.

2) If the 'nth' element has not been located and the last element has been reached, B^b holds a non-zero count (indicating an erroneous count was initially placed in B^b), V^v holds 00000, and the Operand Bank register holds the bank address of the last element.

D Register Jump (DRJ)#

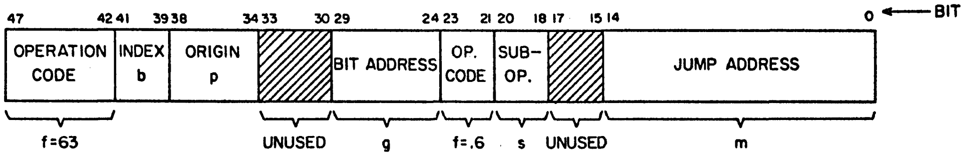


This instruction scans the D (Flag) register from left to right. If a non-zero bit is detected, a jump is executed to address P + i + 1 (where P is the current address and 'i' is the location of the first non-zero bit in the D register).* If the D register is zero, the next instruction is executed. This instruction is restricted to use as an upper instruction.

* 'i' = the location of the particular bit within the register. Though the register is numbered from right to left, scanning is from left to right. The first bit scanned is bit 47. If a "1" exists in bit 47, i = 47, and a jump is effected to [P + 47 + 1] (decimal notation).

§ 121.

NBJP, ZBJP bm Bit Sensing



This instruction examines a single bit of 48 (specified by 'g') in a designated register ('p' specifies the register - see Inter-Register instruction). A 3-bit sub-operation designator 's' specifies the operation to be performed on this bit.

The lower order two bits of 's' specify the operation to be performed after the sense operation:

s = 0 Leave bit alone
s = 1 Set bit to "1"
s = 2 Clear bit
s = 3 Complement (toggle) the bit

If, in the execution of this instruction, an attempt is made to alter the contents of registers designated by codes 20-31, the following occurs:

1) That operation which would alter the contents of registers 20-31 is not performed, and

2) The instruction continues to completion.

This operation does not constitute a fault or interruptible condition.

The upper order bit of 's' conditions a jump operation.

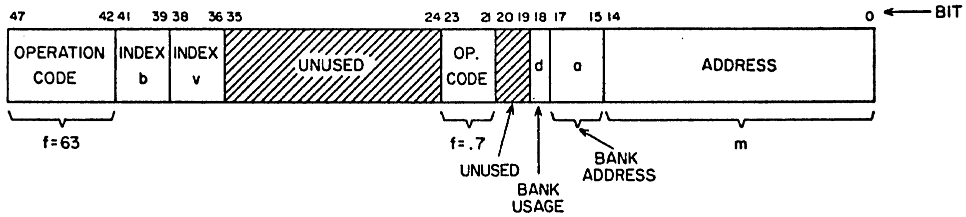
If upper order bit of s = 1 Jump if bit being examined in the specified register is a "0".

If upper order bit of s = 0 Jump if bit being examined in the specified register is a "1".

If the condition is met, the jump is to the address specified by M. If the jump condition is not met, the next instruction is executed.

§ 121.

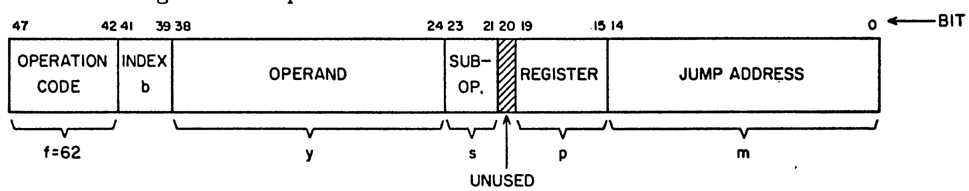
EXEC b v m Execute



Jumps to M $\left[M = m + (B^b) + (V^v)\right]$ and executes both instructions at M.

The Operand Bank switch is set to 'a' if 'd' is a "1". After executing M, the main sequence continues unless the instruction executed was a jump. In this case, a new sequence is initiated at the jump address in the same program bank as EXEC. This instruction is effectively an indirect instruction, or a subroutine of a single instruction. Note that the instruction bank address is not changed by the execute instruction. Note also that the contents of P remain at the address of the EXEC instruction.

RGJB b m Register Jump



Jumps to M $\left[M = m + (B^b)\right]$ if, in the operation specified by 's', the condition is met. If the condition is not met, it executes the next instruction.

If, in the execution of this instruction, an operation would attempt to alter the contents of registers designated by codes 20-31, the following occurs:

1) That operation (s = 6 or 7) which could alter registers 20-31 is not performed, and
2) The instruction continues to completion.

This operation does not constitute a fault or interruptible condition.

§ 121.

Octal values for 's' and the specific operations are:

s	Operation
0	(p) = y?
1	(p) > y?
2	(p) < y?
3	(p) ≠ y?
4	(p) ≤ y?
5	(p) ≥ y?
6	(p) < y? } if (p) < y, then (p) - y → (p)
7	(p) ≥ y? } if (p) < y, then (p) - y → (p)

In executing the above operations, the following arithmetic properties hold:

a) If 'p' designates a 48-bit register, the sign bit of 'y' is extended, and signed quantities are compared in the operation.

b) If 'p' designates a 15-bit register, the operands are compared as 48-bit quantities (15-bit quantities with "0's" extended in the upper bit positions).

Operand registers are indicated below according to their octal values of 'p'.

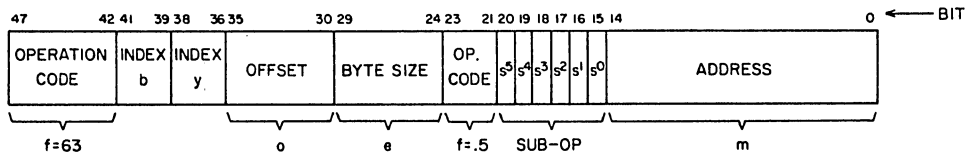
00 - Time Limit Register	15 - D Full
01 - B^1	16 - Bounds Register
02 - B^2	17 - Interrupt Mask Register
03 - B^3	20 - Interrupt Register
04 - B^4	* 21 - All "0's"
05 - B^5	* 22 - +1
06 - B^6	* 23 - All "1's"
07 - A Lower Address	24 - Instruction Bank Register
10 - A Upper Address	25 - Operand Bank Register
11 - Q Lower Address	26 - Shift Count Register
12 - Q Upper Address	27 - Miscellaneous Mode Selections
13 - A Full	30 - P Register
14 - Q Full	31 - Time Register

* These are not registers, but forced operands which may be referenced in the operation.

§ 121.

VARIABLE DATA FIELD

Byte (LBYT, SBYT, SCAN)



The byte instruction performs two general operations on specified portions (bytes) of A, Q, or a designated storage operand. These operations are:

Transmit

1) Load - Loads a byte of the specified register (A or Q) with the designated byte of M.
2) Store - Stores a byte of A or Q in the selected byte of M.

Scan

Searches storage operands in byte-size increments until the specified condition is met or until (A) = 0 (the A register holds the byte count). Operation designators are tabulated below.

CODING SPECIMEN: COMPASS

§ 132.

.1 CODING SPECIMEN

The following is an example of the COMPASS output listing.

ORIGINAL SOURCE DECK LISTING

```
              IDENT         SENSLESS
A             BLOCK         0
              COMMON        ARRAY1(100B), ARRAY1A(20B)
PROGRAMA      SLJ           **
              STA           TEMP,1
              STQ           TEMP,2
              LDA,MG        TEMP,1
              RTJ           PROGRAMB
              EXT           PROGRAMB
+             LDQ           =O7700000
              STL           TEMP
              ENTRY         PROGRAMA
                .
                .
                .
              LIU           PROGRAMB,3
              SIL           ARRAY1+20B,3
                .
                .
                .
              SLJ           PROGRAMA
B             BLOCK         0
              COMMON        ARRAY2(100)
              ORGR          ARRAY2
              OCT           0,1,2,3
              ORGR          *
EXCH          SLJ           **
              LBYT,A0,E6,RI,CL    0,3,4
              INI           1,3
              ENI           42,4
              SLJ           EXCH
              END
```

§ 132.

.1 CODING SPECIMEN (Contd.)

```
                              OUTPUT LISTING FROM ABOVE SOURCE DECK
                                             IDENT     SENSLESS                    00001
PROGRAM LENGTH               00307
BLOCK NAMES
                    A        00120
                    B        00144
ENTRY POINTS
                    PROGRAMA 00000

EXTERNAL SYMBOLS
                    PROGRAMB
                                  A          BLOCK     0                           00002
 00000                                       COMMON    ARRAY1(100B),ARRAY1A(20B)   00003
 00100                                                 ARRAY1A(20B)
 00000      75 0    77777         PROGRAMA   SLJ       **                          00004
            20 1   P00221                    STA       TEMP,1                      00005
 00001      21 2   P00221                    STQ       TEMP,2                      00006
            50 0    00000
 00002      77 1    00004                    LDA,MG    TEMP,1                      00007
            12 1   P00221
 00003      75 4   X77777                    RTJ       PROGRAMB                    00008
                                             EXT       PROGRAMB                    00009
            50 0    00000
 00004      16 0   P00306         +          LDQ       =07700000                   00010
            47 0   P00221                    STL       TEMP                        00011
                                             ENTRY     PROGRAMA                    00012
   .                                           .                                     .
   .                                           .                                     .
   .                                           .                                     .
   .                                           .                                     .
 00207      52 3   X00003                    LIU       PROGRAMB,3                  00131
            57 3   C00020                    SIL       ARRAY1+20B,3                00132
                                               .
                                               .
 00301      75 0   P00000                    SLJ       PROGRAMA                    00178
            50 0    00000
                                  B          BLOCK     0                           00179
 00000                                       COMMON    ARRAY2(100)                 00180
                   C00000                    ORGR      ARRAY2                      00181
 00000      00 0    00000                    OCT       0, 1, 2, 3                  00182
            00 0    00000
 00001      00 0    00000                              1
            00 0    00001
 00002      00 0    00000                              2 .
            00 0    00002
 00003      00 0    00000                              3
            00 0    00003
                   P00302                    ORGR      *                           00183
 00302      75 0    77777         EXCH       SLJ       **                          00184
            50 0    00000
 00303      63 3    40006                    LBYT,A0,E6,RI, CL    0, 3, 4          00185
            52 0    00000
 00304      51 3    00001                    INI       1,3                         00186
            50 4    00052                    ENI       42,4                        00187
 00305      75 0   P00302                    SLJ       EXCH                        00188
            50 0    00000
 00306      00 0    00000
            07 7    00000
                                             END                                   00189
```

§ 132.

.1 CODING SPECIMEN (Contd.)

CORRECTION DECK TO BE ASSEMBLED WITH COSY DECK ASSOCIATED WITH ABOVE LISTING

```
REPLACE   3
COMMON    ARRAY1(120B)
COMMON    ARRAY1A
REPLACE   5, 6
DSTA      TEMP+2
INSERT    10
ADD       =0400000
DELETE    131
```

OUTPUT LISTING FROM ASSEMBLY OF ABOVE CORRECTION DECK AND COSY DECK

```
                                            IDENT      SENSLESS                  00001
PROGRAM LENGTH              00310
BLOCK NAMES
                    A       00121
                    B       00143
ENTRY POINTS
                    PROGRAMA 00000

EXTERNAL SYMBOLS
                    PROGRAMB

                                   A        BLOCK      0                         00002
00000                                       COMMON     ARRAY1(120B)              00003
00120                                       COMMON     ARRAY1A                   00004
00000    75  0   77777    PROGRAMA SLJ        **                        00005
         50  0   00000
00001    77  2   00000             DSTA       TEMP+2                    00006
         20  0  P00220
00002    77  1   00004             LDA,MG     TEMP,1                    00007
         12  1  P00216
00003    75  4  X77777             RTJ        PROGRAMB                  00008
                                   EXT        PROGRAMB                  00009
         50  0   00000
00004    16  0  P00306             LDQ        =07700000                 00010
         14  0  P00307             ADD        =0400000                  00011
00005    47  0  P00216             STL        TEMP                      00012
                                   ENTRY      PROGRAMA                  00013
  .                                  .                                    .
  .                                  .                                    .
00207    57  3  C00020             SIL        ARRAY1+20B, 3             00131
  .                                  .                                    .
  .                                  .                                    .
  .                                  .                                    .
00301    75  0  P00000             SLJ        PROGRAMA                  00178
         50  0   00000

                          B        BLOCK      0                         00179
00000                              COMMON     ARRAY2(100)               00180
                C00000             ORGR       ARRAY2                    00181
00000    00  0   00000             OCT        0, 1, 2, 3                00182
         00  0   00000
00001    00  0   00000                        1
         00  0   00001
00002    00  0   00000                        2
         00  0   00002
00003    00  0   00000                        3
         00  0   00003
                P00302             ORGR       *                         00183
00302    75  0   77777    EXCH     SLJ        **                        00184
         50  0   00000
00303    63  3   40006             LBYT,A0,E6,RI,CL  0, 3, 4            00185
         52  0   00000
00304    51  3   00001             INI        1, 3                      00186
         50  4   00052             ENI        42, 4                     00187
00305    75  0  P00302             SLJ        EXCH                      00188
         50  0   00000
00306    00  0   00000
         07  7   00000
00307    00  0   00000
         00  4   00000             END                                  00189
```

DATA CODE TABLE No. 1

§ 141.

.1 USE OF CODE: . . . . internal collating sequence.

.2 STRUCTURE OF CODE

In ascending sequence

0	□	
1	undefined	Y
2	undefined	Z
3	undefined	≠
4	-	,
5	J	%
6	K	undefined
7	L	undefined
8	M	undefined
9	N	
?	O	
#	P	
@	Q	
undefined	R	
undefined	0	
undefined	$	
&	*	
A	undefined	
B	undefined	
C	undefined	
D	blank	
E	/	
F	S	
G	T	
H	U	
I	V	
+	W	
'	X	

DATA CODE TABLE NO. 2

§ 142.

.1 USE OF CODE: . . . . binary 6-bit code. internal.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . 2 zone bits; B, A = 32, 16.

.222 Less significant pattern: . . . . 4 numeric bits; 8, 4, 2, 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0	0	&	-	Blank
1	1	A	J	/
2	2	B	K	S
3	3	C	L	T
4	4	D	M	U
5	5	E	N	V
6	6	F	O	W
7	7	G	P	X
8	8	H	Q	Y
9	9	I	R	Z
10	?	+0	-0	ǂ
11	#	.	$	,
12	@	□	*	%
13				
14				
15				

DATA CODE TABLE NO. 3

§ 143.

.1 USE OF CODE: . . . . BCD 6-bit code. magnetic tape.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . 2 zone bits: B, A = 32, 16.

.222 Less significant pattern: . . . . 4 numeric bits, 8, 4, 2, 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN			
	0	16	32	48
0		Blank	-	&
1	1	/	J	A
2	2	S	K	B
3	3	T	L	C
4	4	U	M	D
5	5	V	N	E
6	6	W	O	F
7	7	X	P	G
8	8	Y	Q	H
9	9	Z	R	I
10	0	ǂ	-0	+0
11	#	,	$	.
12	@	%	*	□
13				
14				
15	TM		Δ	⧧

DATA CODE TABLE NO. 4

§ 144.

.1 USE OF CODE: . . . . CDC 1612 Printer, internal.

.2 STRUCTURE OF CODE

.21 Character Size: . . . . 6 bits.

.22 Character Structure

.221 More significant pattern: . . . . 3 bits: 4, 2 and 1.

.222 Less significant pattern: . . . . 3 bits: 4, 2 and 1.

.23 Character Codes

LESS SIGNIFICANT PATTERN	MORE SIGNIFICANT PATTERN							
	0	1	2	3	4	5	6	7
0	:	8	Blank	Y	-	Q	+	H
1	1	9	/	Z	J	R	A	I
2	2	∅	S	⊐	K	%	B	<
3	3	=	T	,	L	$	C	.
4	4	≠	U	(	M	*	D	)
5	5	≤	V	→	N	↑	E	≥
6	6	'	W	≡	O	↓	F	?
7	7	⊏	X	~	P	>	G	;

NOTE: Characters ~ , %, and $ appear for business application and are replaced respectively by ∧ , ∨ , and ¬ for scientific application.

PROBLEM ORIENTED FACILITIES

The following routines were developed for the CDC 1604 and are available for the CDC 3600.

§ 151.

.1 UTILITY ROUTINES

.11 Simulators of Other Computers

IBM 650
Reference: . . . . . . 02 NBSB.
Data available: . . . . 1961.
Description
The routine simulates an IBM 650 computer containing a 2,000 word drum, index registers and floating point. The simulator operates on a CDC 1604 with an IBM 407, 088 and 523 unit.

CDC 1604-A: . . . . . . by a switch on 1604-A console.

.12 Simulation by Other Computers

CDC 160-A: . . . . INTERFOR system simulates 20 of the 62 operations, and includes other facilities.

.13 Data Sorting and Merging

Reference: . . . . M 4 CODA KSM.
Record size: . . . . . . 80 or 120 characters.
Block size: . . . . 1 record per block.
Key size: . . . . any number of keys of any length.
File size: . . . . any number of tape reels.
Number of tapes: . . . 4 upwards.
Date available: . . . . . 1961.
Description
The routine provides data editing facilities and operates only on BCD data.

.14 Report Writing: . . . . none.

.15 Data Transcription

Convert Symbolic Magnetic-Tape-to-Paper-Tape
Reference: . . . . . . M 2 CODA MAGPT.
Data available: . . . . 1961.
Description
Converts 80 or 120 character BCD magnetic tape to Flexowriter tape.
Performance limited by Flexowriter output.

.16 File Maintenance: . . . only routines for specific installations are available

.17 Other

Arithmetic Functions

	TIME (μsec) +	TIME (μsec) -	TIME (μsec) x
Complex Numbers, Floating Point	50	50	100

Mathematical Functions (Representative cases, all floating point)

	TIME (μsec)	SPACE	ERROR (Max)
Sine	275	68	2.1×10^{-11}
Cos	275	68	2.1×10^{-11}
Tan	320	53	2.4×10^{-11}
Arc Sine	460	115	8.7×10^{-11}
Arc Cos	310	115	8.7×10^{-11}
Arc Tan	280	71	8.7×10^{-11}
Exponential	156	32	8.7×10^{-11}
Natural log	190	45	8.7×10^{-11}

Polynomial Evaluation

	TIME (μsec)	SPACE
Hermite	37 + 47 (N-1)	24
Laguerre	37 + 67 (N-1)	24
Legendre	35 + 70 (N-1)	25

Other
Hypergeometric Functions   Space: 2,491 locations, timing unknown.

.2 PROBLEM ORIENTED LANGUAGES

PERT
Linear Programming Package
Civil Engineering Computation System

MACHINE ORIENTED LANGUAGE: COMPASS

§ 171.

.1 GENERAL

.11 Identity: . . . . COMPASS.

.12 Reference: . . . . COMPASS Reference Manual.

.13 Description

COMPASS is the basic assembly language of the CDC 3600 system and is used with the SCOPE operating system. This language includes all the machine code instructions. COMPASS allows for source language changes to already assembled programs, and for system, installation, or programmer-provided macro instructions. Programmer-provided macros may be included in the library. Communication between different subprograms and library subroutines is provided by use of COMMON blocks and the EXTernal pseudo-operation. Communication with the operating system is by way of the system macros.

Use of COMPASS eliminates the need for the programmer to take care of complex format requirements of many of the CDC 3600 instructions. In particular, the many modifications which are available in the use of the single and double precision AUGMENT instructions can now be contained within the augmented instruction instead of being written separately.

There are three types of macro codes. These are System macros (provided with the CDC 3600 system itself), Library macros (provided by the installation), and programmer-provided macros (provided within the program itself). These macros are normally written in COMPASS language and are inserted into the assembled coding each time they are called. However, some control is included by providing two pseudo-operations IFN, and IFZ. During assembly, these operations are used to test the value of some parameters or expression against zero to determine whether or not to insert the next "n" instructions of the macro coding.

Closed subroutines may be called into a program by the use of the EXTERNAL function. These are only incorporated into the program once.

The assembly language performs two roles: first, it allows a programmer to write machine instructions and constants in a convenient form; and second, it provides a systematic means of using any library, monitor, or subroutines as desired.

Labeling is unusually free. Address symbols are normally one letter with an option of being followed by up to seven further alphameric characters for all labels. Three other types (+, -, and all numeric symbols) serve other functions.

There are two types of data areas; both are called "COMMON" areas. These are differentiated in the language by having alphameric (called "Labeled COMMON") or numeric (called "Numbered COMMON") labels, and in usage by being able to preset the contents of the areas at load time only if "Labeled COMMON" is used.

Communication with other independently written routines is arranged by the ENTRY points and the EXTernal Symbol linkage. These operations provide for a label to be common to more than one routine. The actual linkage is created at loading time.

The assembly program for the 3600 is designed to accept as input, cards or card images containing symbolic 3600 programming instructions. It translates the symbolic instructions into 3600 machine language programs in relocatable binary, for loading into any portion of memory at run time. The assembler will produce as output any combination of:

- Output listing of the assembled program.
- Relocatable binary card output for subsequent loading and execution of the assembled program.
- Relocatable binary card images on an assemble and run tape for immediate loading and execution of the assembled program.
- Compressed symbolic output deck to be used as input for subsequent modification and reassembly.

.2 LANGUAGE FORMAT

.21 Diagram

LOCN		OPERATION,MODIFIERS ADDRESS FIELD	COMMENTS		IDENT
1 2 3 4 5 6 7 8	9	10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40	41 42 43 44 45 46 47	68 69 70 71 72	73 74 75 76 77 78 79 80

§ 171.

.22 Legend

LOCATION FIELD (LOCN): The location field, called an L-term, label, symbol, or identifier, may consist of one of the following types:

TYPE 1: A symbol from 1 to 8 characters; the first is alphabetic, the rest are alphabetic or numeric. Leading, imbedded, and trailing blanks will be ignored and the symbol will be packed left justified by COMPASS.

TYPE 2: A plus (+) anywhere in the field and blanks in the remaining columns.

TYPE 3: A minus (-) anywhere in the field and blanks in the remaining columns.

TYPE 4: A label consisting of 8 characters all of which must be either numeric or blank.

OPERATION FIELD: The operation field may consist of:

1. One of the mnemonic operation codes listed in 247:171.84 followed by a blank column or one or more modifiers. Commas are used to separate the operation code from the modifiers and the modifiers from each other.
2. One of the pseudo operations listed in 247:171.82.
3. The name of a macro-instruction.
4. One of the octal numbers 0-77.

A blank in column 10 terminates the operation field and the operation code is given the value zero.

ADDRESS FIELD

Expressions: The address field may contain the bank, (a), memory address or operand, m, and index registers, b and v, required to identify an operand or a storage location. Each of the terms in the address field may be defined by an arithmetic expression involving symbols and constants. The bank term, if present, must be enclosed in parentheses. Constants must be decimal or octal integers less than 2^{15}. A constant will be interpreted as decimal. A symbol in an arithmetic expression must be a TYPE 1 symbol. The four operations permitted in the arithmetic expression are: addition (+), subtraction (-), multiplication (*), and division (/).

Special Symbols: * (this location).
**(77777_8).

Literals: restricted to single or double precision constants, in Decimal, Octal, Hollerith, or Typewriter code.

.23 Corrections: . . . . . . three pseudo instructions, DELETE, REPLACE, and INSERT, are available which operate on a condensed deck.

.24 Special Conventions

.241 Compound addresses: . e.g., SYMBOL + 5.
.242 Multi-addresses: . . . none.
.243 Literals: . . . . up to 40 char, any code.
.244 Special coded addresses: . . . . . . * means this address.
** means 77777_8.
± forces an instruction into the upper or lower half of a word.

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . no practical limit.
.312 Common label formation rule: . . . . 1 to 8 alphamerics including certain special characters. Blanks are not required. First character must be non-numeric.
.313 Reserved labels: . . . . none.
.315 Designators: . . . . . . none.
.316 Synonyms: . . . . yes, via EQUivalence pseudo-op.

.32 Universal Labels: . . . none, but individual labels can be made universal to several independent subprograms, being called an External Table Entry to each subprogram.

.33 Local Labels

.331 Labels for procedures
Existence: . . . . . . optional.
Formation rule
First character: . . non-numeric character.
Others: . . . . any non-blank character.
Number of characters: . . . . 1 to 8.
.332 Labels for library routines: . . . . same as for procedures.
.333 Labels for constants: . same as for procedures, or as an element of an array within a numbered COMMON statement.
.334 Labels for files: . . . . none.
.335 Labels for records: . . none.
.336 Labels for variables: . same as for procedures.
.337 Labels for other subprograms: . . . . same as for procedures.
.338 Others
Labels for blocks containing preset data
Existence: . . . . . optional.
Formation rule: . . 1 to 8 alphabetics, "Labeled Common Blocks."
Labels for reserved blocks for working storage
Existence: . . . . . optional.
Formation rule: . . 8 numeric or blank characters, an all blank label is acceptable, "Numbered Common Blocks."
Labels for arrays: . . same as for procedures.

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.4 DATA

.41 Constants

.411 Maximum size constants

Machine Form	External Language
Integer:	14 decimal digits plus sign. 16 octal digits plus sign.
Fixed numeric:	not allowed.
Floating numeric:	28 digits with a decimal or binary exponent of up to 3 digits, plus sign.

.412 Maximum size literals
- Integer
  - Decimal: . . . . . . 28 decimal.
  - Octal: . . . . 16 octal digits plus sign.
- Fixed numeric: . . . . only integer.
- Floating numeric: . . $10^{\pm 308}$
- Alphameric: . . . . . 16 characters.

.42 Working Areas

.421 Data layout
- Implied by use: . . . . no.
- Specified in program: VFD (Variable Field Definition), BLOCK and COMMON statements.

.422 Data type: . . . . implied by use.
.423 Redefinition: . . . . . . use of BLOCK statements.

.43 Input-Output Areas: . . specified in program.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic
- Existence: . . . . . . optional with absolutes.
- Number: . . . . 145.
- Example: . . . . FDV; Floating Divide.
- Comment: . . . . . . where one op code has more than one type of operation, mnemonic modifiers are written after the operation code, thus FDV, CM, MG, UR would indicate that the magnitude of the complement of the addressed operand be used, and that the operation should be unrounded.

.512 Absolute
- Existence: . . . . . . optional with mnemonic.
- Number: . . . . 145.
- Example: . . . . 45 for Add Logical.

.52 Macro-Codes: . . . . . yes, as provided by system installation in the library, or by programmer at head of the program.

.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control
- Allocation counter: . . various pseudo-ops.
- Label adjustment: . . various pseudo-ops.
- Annotation: . . . . . . Remarks.

.542 Allocation counter
- Set to absolute: . . . . no. (ORGR relocatable pseudo-op entry in location).
- Set to label: . . . . . yes.
- Set relative to label: . yes.
- Step forward: . . . . . implied by set relative to label.
- Step backward: . . . . implied.
- Reserve area: . . . . yes.

.543 Label adjustment
- Set labels equal: . . . yes.
- Set label relative: . . yes.
- Set absolute value: . . no.
- Clear label table: . . not within single subprogram; yes, by dividing into separate subprograms.

.544 Annotation
- Comment phrase: . . yes.
- Title phrase: . . . . . yes.

.545 Other
- Allocation mode: . . . absolute or relocatable.

.55 Facilities Omitted: . . none.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: . . none.

.62 Special Functions

.621 Facilities: . . . . none; any could be added in installation library.
.622 Method of call: . . . . . LIBM declares all used pseudo operations at the start of the program. The use of a declared macro name in the operation field of the coding sheet calls the actual macro.

.63 Overlay Control: . . . . handled by operating system.

.64 Data Editing

.641 Radix conversion: . . . decimal-to-binary for initial constants.
Code translation: . . . alphabetic-to-BCD, Flexowriter and Teletype.
.642 Format control: . . . . none.

.65 Input-Output Control: . own program, with I/O pseudo-op check on I/O units involved.

.66 Sorting: . . . . none.

.67 Diagnostics: . . . . . . none can be specified by the programmer for use at running time in COMPASS system.

.7 LIBRARY FACILITIES

.71 Identity: . . . . installation library.

.72 Kinds of Libraries

.721 Fixed master: . . . . . no.
.722 Expandable master: . . yes.

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.73 Storage Form: . . . . . magnetic tape.

.74 Varieties of Contents: . as determined by installation.

.75 Mechanism

.751 Insertion of new item: . via SCOPE Monitor.
.752 Language of new item: . open.
.753 Method of call: . . . . . operation code identifies routine. ENTRY identifies entry point. Operating Manual lists special calls.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: yes.
.764 Closed routines appear once: . . . . yes.

.8 INSTRUCTION CODE REPERTOIRE

.81 Macros: . . . . as provided by installation library.

.82 Pseudos

Code	Description
BCD	Insert BCD characters.
BES	Reserve block of storage.
BLOCK	Specify block of common.
BSS	Reserve block of storage.
CODAP	Change input to CODAP-1 format.
COMMON	Declare array in common

.82 Pseudos (Contd.)

Code	Description
COMPASS	Change input to COMPASS format.
DEC	Insert single precision decimal constants.
DECD	Insert double precision decimal constants.
DELETE	Delete portions of a program.
ECHO	Replicate a sequence.
EJECT	Eject a page on the output listing.
END	Specify the end of a subprogram.
ENDM	Terminate a macro-definition.
ENDT	Specify the end of a subprogram.
ENTRY	Define entry points in a subprogram.
EQU	Equate an undefined symbol to a defined symbol.
EXT	Define external symbols.
IDENT	Identify the subprogram by name.
IFN	Macro control pseudo instruction.
IFZ	Macro control pseudo instruction.
INSERT	Insert changes in a program.
LIBM	Declare library macros.
LIST	Resume output listing.
MACRO	Define a macro.
MACRO-INSTRUCTION	Calls a macro.
NOLIST	Suppress output listing.
OCT	Insert octal constants.
ORGR	Set location counter.
REM	Insert remarks on the output listing.
REPLACE	Replace portions of a program.
SCOPE	Terminates assembly process.
SPACE	Insert spaces in the output listing.
TYPE	Insert typewriter codes.
VFD	Assign data in variable byte sizes.

.84 Direct

Operation Field	Address Field	Instruction
ROP, s	p, q, r	Register OPeration (Inter Register Transmission) 1/
RSW,CQ,CR	q, r	Register SWap 1/
RXT,CQ,CR	q, r	Register TRANSmiT 1/
LDA,CM,MG	(a)m, b, v	LoaD A.
LAC,CM	(a)m, b, v	Load A Complement.
LDQ,CM,MG	(a)m, b, v	LoaD Q.
LQC,CM	(a)m, b, v	Load Q Complement.
STA,CM,CL,MG	(a)m, b, v	STore A.
STQ,CM,CL,MG	(a)m, b, v	STore Q.
LIU	(a)m, b, v	Load Index Upper.
LIL	(a)m, b, v	Load Index Lower.
SIU	(a)m, b, v	Store Index Upper.
SIL	(a)m, b, v	Store Index Lower.
ADD,CM,MG	(a)m, b, v	ADD.
SUB,CM,MG	(a)m, b, v	SUBtract.
MUI,CM,MG	(a)m, b, v	MUltiply Integer.
DVI,CM,MG	(a)m, b, v	DiVide Integer.
MUF,CM,MG	(a)m, b, v	MUltiply Fractional.
DVF,CM,MG,TR	(a)m, b, v	DiVide Fractional.
FAD,RP,CM,MG,UN,UR	(a)m, b, v	Floating ADd.
FSB,RP,CM,MG,UN,UR	(a)m, b, v	Floating SuBtract.
FMU,CM,MG,UN,UR	(a)m, b, v	Floating MUltiply.

1/ In ROP the modifier s is required. In ROP, RSW, and RXT a modifier does not cause insertion of the single precision augment.

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.84 Direct (Contd.)

Operation Field	Address Field	Instruction
FDV,CM,MG,UR	(a)m,b,v	Floating DiVide.
ADX	y	ADd to eXponent.
ENA,CM	(a)m,b,v	ENter A.
ENQ,CM	(a)m,b,v,	ENter Q.
ENI	(a)m,b,v	ENter Index.
NOP		No OPeration (ENI o).
INA,CM	(a)m,b,v	INcrease A.
INI	(a)m,b,v	INcrease Index.
SAU	(a)m,b,v	Substitute Address Upper.
SAL	(a)m,b,v	Substitute Address Lower.
ISK	(a)m,b,v	Index SKip.
SST	(a)m,b,v	Selective SeT.
SCM	(a)m,b,v	Selective CoMplement.
SCL	(a)m,b,v	Selective CLear.
SSU	(a)m,b,v	Selective SUbstitute.
LDL	(a)m,b,v	LoaD Logical.
ADL,RP,CM	(a)m,b,v	ADd Logical.
SBL,RP,CM	(a)m,b,v	SuBtract Logical.
STL	(a)m,b,v	STore Logical.
ARS,EO,SS	(a)m,b,v	A Right Shift.
QRS,EO,SS	(a)m,b,v	Q Right Shift.
LRS,EO,SS	(a)m,b,v	Long Right Shift.
ALS,EO,SS	(a)m,b,v	A Left Shift.
QLS,EO,SS	(a)m,b,v	Q Left Shift.
LLS,EO,SS	(a)m,b,v	Long Left Shift.
SCA	(a)m,b,v	SCale A.
SCQ	(a)m,b,v	SCale aQ.
RAD	(a)m,b,v	Replace ADd.
RSB	(a)m,b,v	Replace SuBtract.
RAO	(a)m,b,v	Replace Add One.
RSO	(a)m,b,v	Replace Subtract One.
SSK	(a)m,b,v	Storage SKip.
SSH	(a)m,b,v	Storage SHift.
EQS	(a)m,b,v	EQuality Search.
THS	(a)m,b,v	THreshold Search.
MEQ	(a)m,b,v	Masked EQuality Search.
MTH	(a)m,b,v	Mashed THreshold Search.
AJP,ZR 2/ NZ PL MI	(a)m,v	A JumP.
QJP,ZR 2/ NZ PL MI	(a)m,v	Q JumP.
ARJ,ZR 2/ NZ PL MI	(a)m,v	A Return Jump.
QRJ,ZR 2/ NZ PL MI	(a)m,v	Q Return Jump
IJP	(a)m,b,v	Index JumP.
SLJ	(a)m,b,v	SeLective Jump.
SJ1	(a)m,v	Selective Jump - key 1.
SJ2	(a)m,v	Selective Jump - key 2.
SJ3	(a)m,v	Selective Jump - key 3.
RTJ	(a)m,v	ReTurn Jump.
RJ1	(a)m,v	selective Return Jump key 1.
RJ2	(a)m,v	selective Return Jump key 2.
RJ3	(a)m,v	selective Return Jump key 3.

2/ In AJP,QJP,ARJ and QRJ a modifier is required and does not cause insertion of the single precision augment instruction.

§ 171.

.84 Direct (Contd.)

Operation Field	Address Field	Instruction
SLS	(a)m, b, v	SeLective Stop.
SS1	(a)m, v	Selective Stop jump key 1.
SS2	(a)m, v	Selective Stop jump key 2.
SS3	(a)m, v	Selective Stop jump key 3.
SRJ	(a)m, v	Stop Return Jump.
SR1	(a)m, v	Selective Stop Return jump key 1.
SR2	(a)m, v	Selective Stop Return jump key 2.
SR3	(a)m, v	Selective Stop Return jump key 3.
DLDA, CM, MG	(a)m, b, v	Double precision LoaD A.
DSTA, CM, CL, MG	(a)m, b, v	Double precision STore A.
DFAD, RP, CM, MG, UN, UR	(a)m, b, v	Double precision Floating ADd.
DFSB, RP, CM, MG, UN, UR	(a)m, b, v	Double precision Floating SuBtract.
DFMU, CM, MG, UN, UR	(a)m, b, v	Double precision Floating MUltiply.
DFDV, CM, MG, UR	(a)m, b, v	Double precision Floating DiVide.
XMIT, CM, AUG	(a)m, (i)n	TRANSMIT
MK		
PC		
SEQU, I	(a)m, n	Search for EQUality.
SMEQ, I	(a)m, n	Search for Masked EQuality.
SEWL, I	(a)m, n	SEarch Within Limits.
SMWL, I	(a)m, n	Search Magnitude Within Limits.
LSTU	b, v	Locate liST element Upper.
LSTL	b, v	Locate liST element Lower.
NBJP, ST	p, g, m, b	Non zero Bit JumP.
CL		
CM		
ZBJP, ST	p, g, m, b	Zero Bit JumP.
CL		
CM		
EXEC	(a)m, b, v	EXECute.
RGJP, s	p, y, m, b	ReGister JumP 3/
UBJP	(a)m, b, i	Unconditional Bank JumP.
BJPL	(a)m, b, i	unconditional Bank JumP Lower.
BRTJ	(a)m, b, i	unconditional Bank ReTurn Jump.
BJSX	(a)m, b, i	Bank Jump and Set indeX.
LBYT, Ao, Ei, LI, CL	m, b, v	Load BYTe 4/
Qo RI		
SBYT, Ao, Ee, LI, CL	m, b, v	Store BYTe 4/
Qo RI		
SCAN, Qo, Ee, EQ	m, b, v	SCAN byte 4/
GT		
LT		
NE		
LE		
GE		
INF	m	INternal Function.
CONN	x, e, c, n	CONNect.
EXTF	x, c, n	EXTernal Function.
BEGR	x, (a)m, n	BEGin Read.
BEGW	x(a)m, n	BEGin Write.
COPY, CW, CWA	x, b	COPY status.
CLCH	x	CLear CHannel.
IPA		InPut to A.
ALG	y	perform ALGorithm.
MPJ		Main Product register Jump.
CPJ	x	Channel Product register Jump.
DRJ		D Register Jump.
	INPUT/OUTPUT CONTROL WORDS	
IOSW, C	(a)m, w	Skip words (write zeros under Word count control).
IOTW, C	(a)m, w	Transmit data under Word count control.
IOSR, C	(a)m, w	Skip words (write zeros) under word count or to end of Record (and write end of record).
IOTR, C	(a)m, w	Transmit data under word count or to end of Record (and write end of record).
IOJP	(a)m	JumP to (a)m for next control word.

3/ In RGJP the modifier s is required.

4/ In LBYT, SBYT and SCAN the modifiers Ao or Qo and Ee are required. If neither LI nor RI appear, no indexing will be assumed.

NOTES ON SYSTEM PERFORMANCE

§ 201.

File Processing

The main file in the File Processing Problem has been condensed by designing the system to take maximum advantage of features of the CDC 3600 order code, in particular the "Jump on Flag" instruction.

Accordingly:

(1) Trailers were used to handle data which might not be physically present.

(2) Flags were added to denote the presence or absence of trailers.

(3) Most data was stored in binary form, reducing the space requirement.

(4) The 20-character field for the name was broken into words. Flags were used to denote the number of words.

These practices reduced the data volume of the main file to an average of 8.6 words of 48 bits, i.e., the equivalent of sixty-eight 6-bit BCD characters.

CDC 3600
SYSTEM PERFORMANCE

CDC 3600 SYSTEM PERFORMANCE

WORKSHEET DATA TABLE 1

Worksheet	Item		Configuration: VI B, VII B (Blocked) †		VI B, VII B (Unblocked)		VIII B (Blocked) †		VIII B (Unblocked)		Reference
1 INPUT-OUTPUT TIMES	Char/block	(File 1)	1,000		1,000		1,000		1,000		4:200.112
	Records/block	K (File 1)	15		15		15		15		
	msec/block	File 1 = File 2	17		17		17		17		
		File 3	17		6		17		6		
		File 4	17		6		17		6		
	msec/switch	File 1 = File 2	---		---		---		---		
		File 3	---		---		---		---		
		File 4	---		---		---		---		
	msec penalty	File 1 = File 2	0.1		0.1		0.1		0.1		
		File 3	0.1		0.004		0.1		0.004		
		File 4	0.1		0.008		0.1		0.008		
2 CENTRAL PROCESSOR TIMES	msec/block	a1	0.12		0.12		0.12		0.12		4:200.1132
	msec/record	a2	0.13		0.13		0.13		0.13		
	msec/detail	b6	0.32		0.32		0.32		0.32		
	msec/work	b5 + b9	0.225		0.225		0.225		0.225		
	msec/report	b7 + b8	0.63		0.63		0.63		0.63		
3 STANDARD PROBLEM A F = 1.0	msec for C. P. and dominant column.	a1	0.12		0.12		0.12		0.12		4:200.114
		a2 K	0.25		0.25		0.25		0.25		
		a3 K	24.00		24.00		24.00		24.00		
		File 1 Master In	0.1	17.0	0.1	17.0	0.1		0.1		
		File 2 Master Out	0.1		0.1		0.1		0.1		
		File 3 Details	0.15		0		0.15		0		
		File 4 Reports	0.2	33.0	0	93.0	0.2	33.0	0	93.0	
		Total	24.92	50.0	24.57	110.0	24.92	33.0	24.57	93.0	
4 STANDARD PROBLEM A SPACE	Unit of measure	(48-bit word)									4:200.1151
		Std. routines	2,048		2,048		2,048		2,048		
		Fixed	1,024		1,024		1,024		1,024		
		3 (Blocks 1 to 23)	400		400		400		400		
		6 (Blocks 24 to 48)	600		600		600		600		
		Files	1,000		622		1,000		622		
		Working	200		200		200		200		
		Total	5,272		4,894		5,272		4,894		

† Detail records are blocked 10 records per 1,000-character block.
Reports are blocked 8 records per 1,000-character block.

CDC 3600 SYSTEM PERFORMANCE (Contd.)

WORKSHEET DATA TABLE 2

Worksheet	Item			Configuration: All (Blocked)	Configuration: All (Unblocked)	Configuration	Reference
5 STANDARD MATHEMATICAL PROBLEM A	Fixed/Floating point						4:200.413
	Unit name	input		606 MTU	606 MTU		
		output		606 MTU	606 MTU		
	Size of record	input		80 char	1,000 char		
		output		108 char	1,000 char		
	msec/block	input	T1	6			
		output	T2	6			
	msec penalty	input	T3	0	0.1		
		output	T4	0	0.1		
	msec/record		T5	0.08	0.08		
	msec/5 loops		T6	0.665	0.665		
	msec/report		T7	0.67	0.67		
7 STANDARD STATISTICAL PROBLEM A	Unit name			606 MTU			4:200.512
	Size of block			960 char			
	Records/block		B	8 †			
	msec/block		T1	16			
	msec penalty		T3	0.1			
	C. P.	msec/block	T5	0.15			
		msec/record	T6	0.003			
		msec/table	T7	0.018			

† Detail records are blocked 10 records per 1,000-character block.
Reports are blocked 8 records per 1,000-character block.

SYSTEM PERFORMANCE

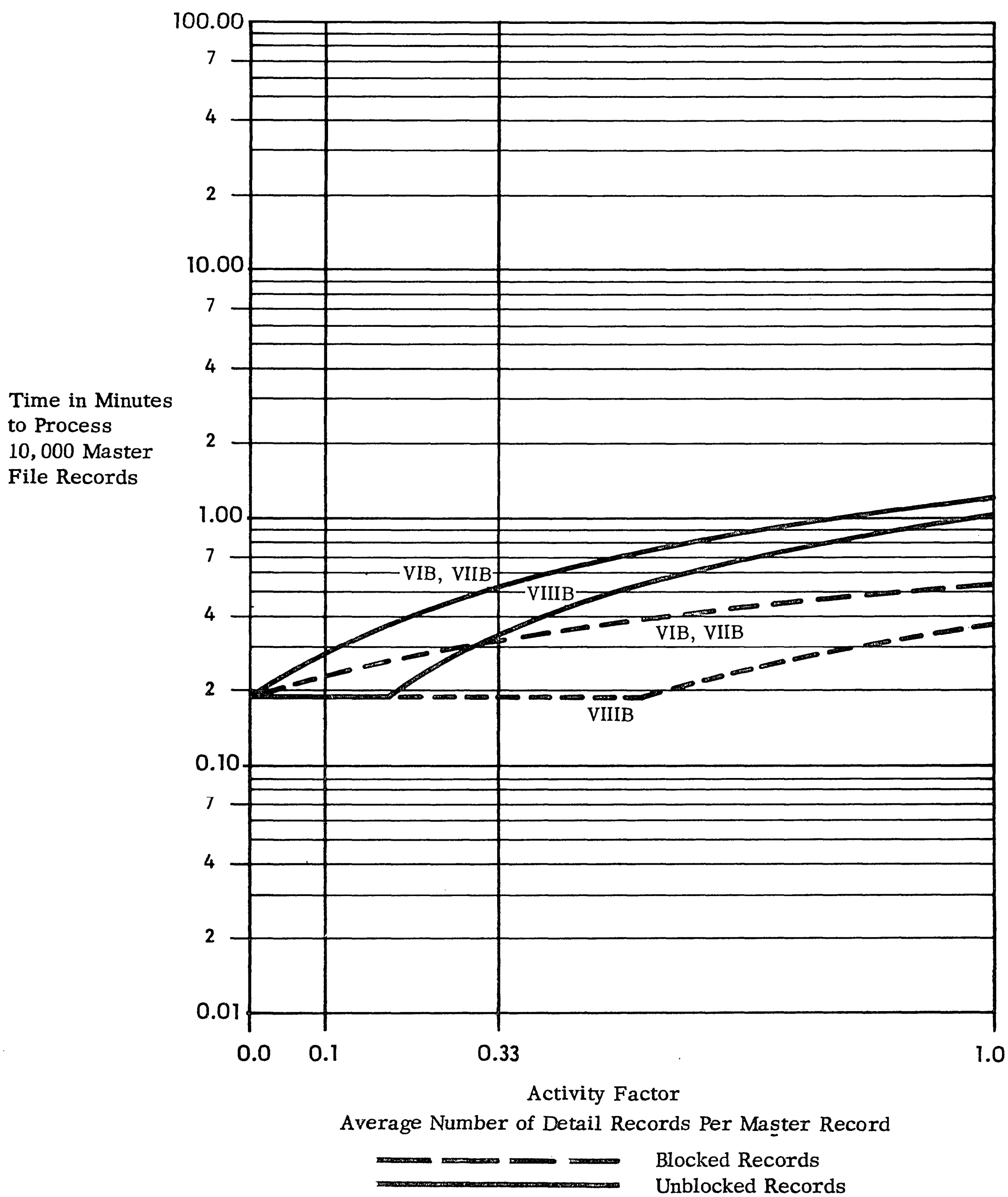
§ 201.

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A (Unblocked & Blocked)

.111 Record Sizes
Master File: . . . . . 108 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.112 Computation: . . . . . . standard.
.113 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.
.114 Graph: . . . . see graph below.
.115 Storage Space Required: 5,272 words.

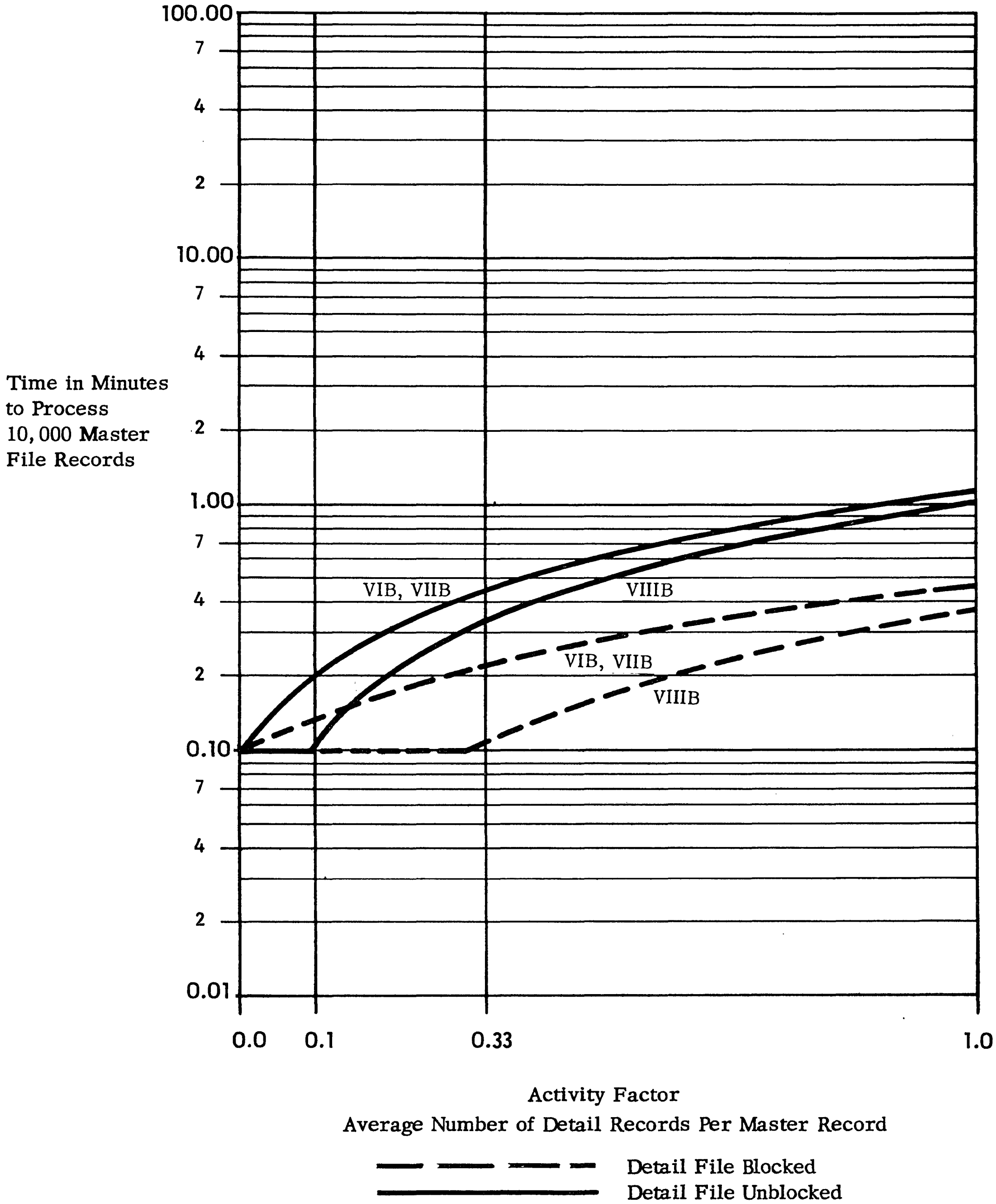


§ 201.

.12 Standard File Problem B (Unblocked & Blocked)

.121 Record Sizes
Master File: . . . . . 54 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.122 Computation: . . . . . standard.
.123 Timing Basis: . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . see graph below.

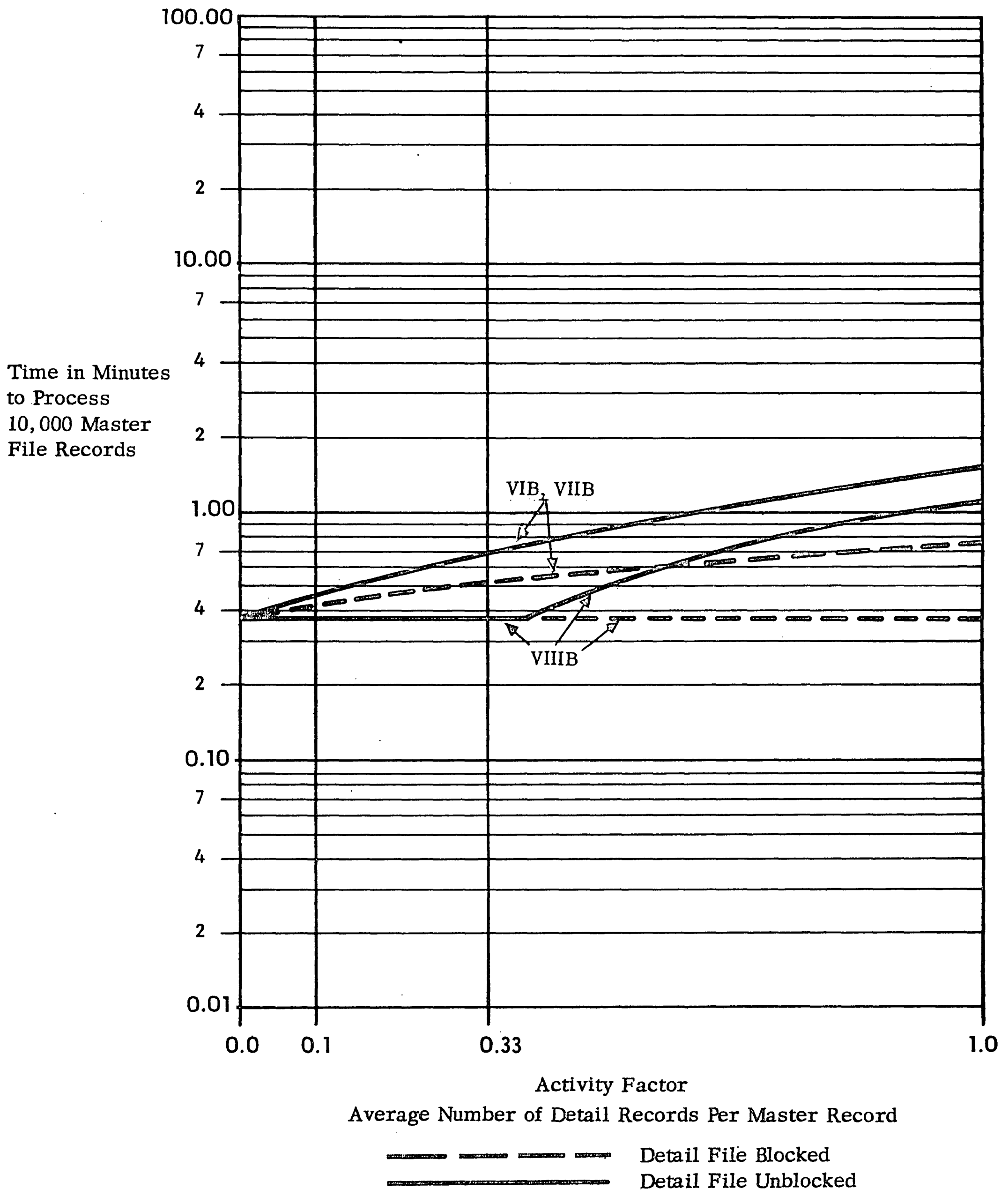


§ 201.

.13 Standard File Problem C (Unblocked & Blocked)

.131 Record Sizes
Master File: . . . . . 216 characters.
Detail File: . . . . . 1 card.
Report File: . . . . . 1 line.

.132 Computation: . . . . . . standard.
.133 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . see graph below.



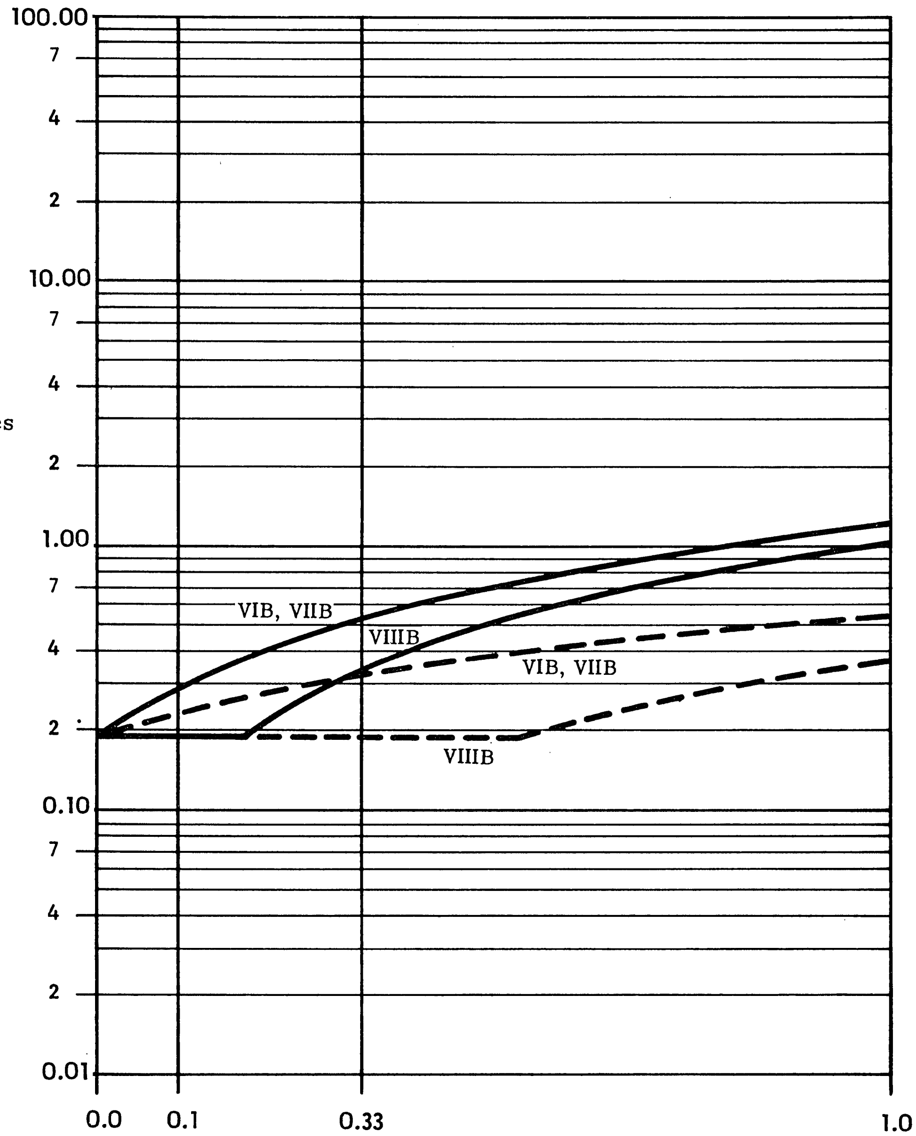
§ 201.

.14 Standard File Problem D (Unblocked & Blocked)

.141 Record Sizes
Master File: . . . . . . 108 characters.
Detail File: . . . . . . 1 card.
Report File: . . . . . . 1 line.

.142 Computation: . . . . . . trebled.
.143 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.144 Graph: . . . . see graph below.

Time in Minutes to Process 10,000 Master File Records



Activity Factor
Average Number of Detail Records Per Master Record

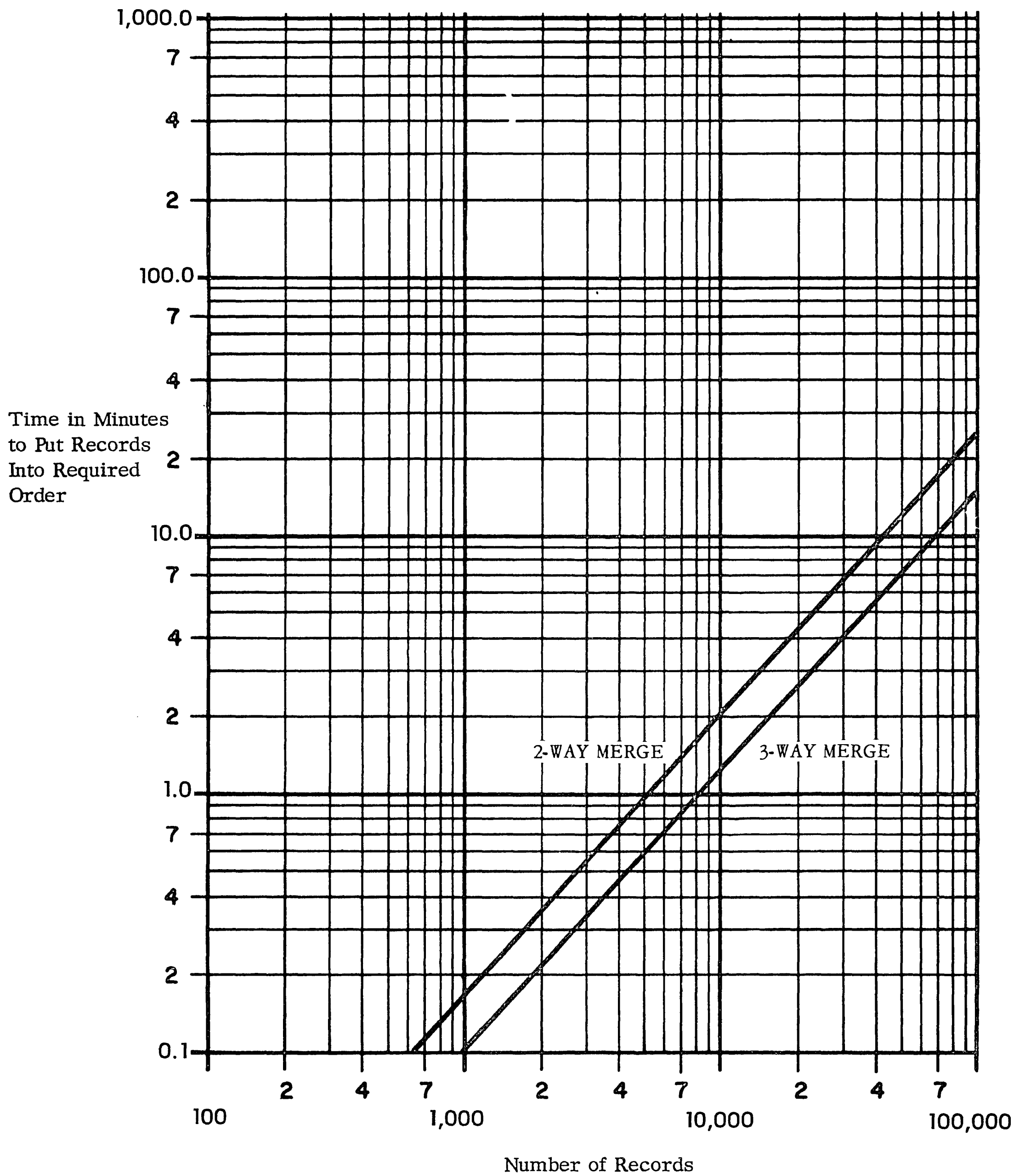
— — — — Detail File Blocked
———— Detail File Unblocked

§ 201.

.2 SORTING

.21 Standard Problem Estimates

.211 Record size: . . . . 80 characters.
.212 Key Size: . . . . 8 characters.
.213 Timing Basis: . . . using estimate procedure outlined in User's Guide, 4:200.213
.214 Graph: . . . . . . see graph below.



§ 201.

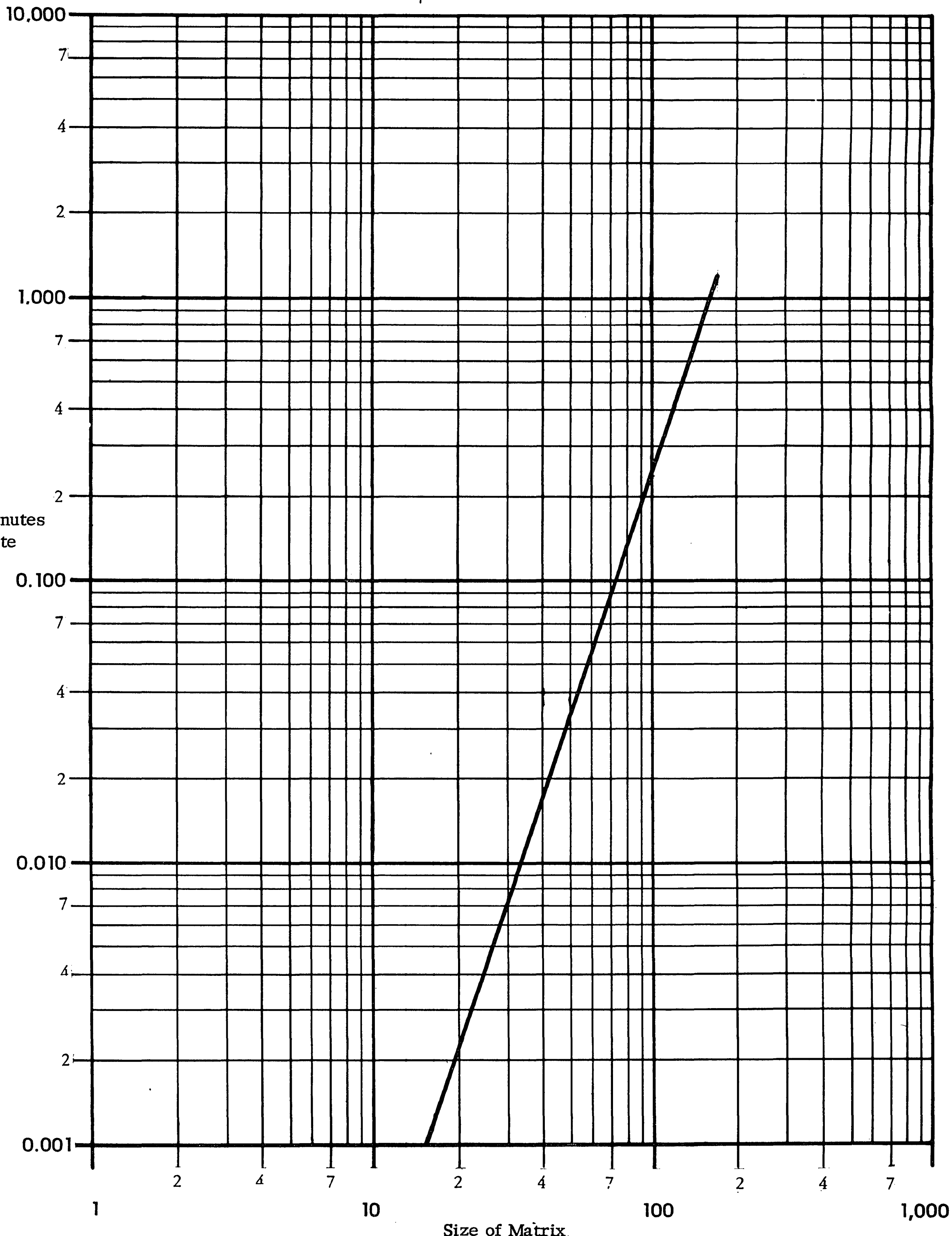
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . using estimating procedure outlined in User's Guide, 4:200.312.

.313 Graph: . . . . see graph below.



§ 201.

.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates (Unblocked & Blocked)

.411 Record sizes: . . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

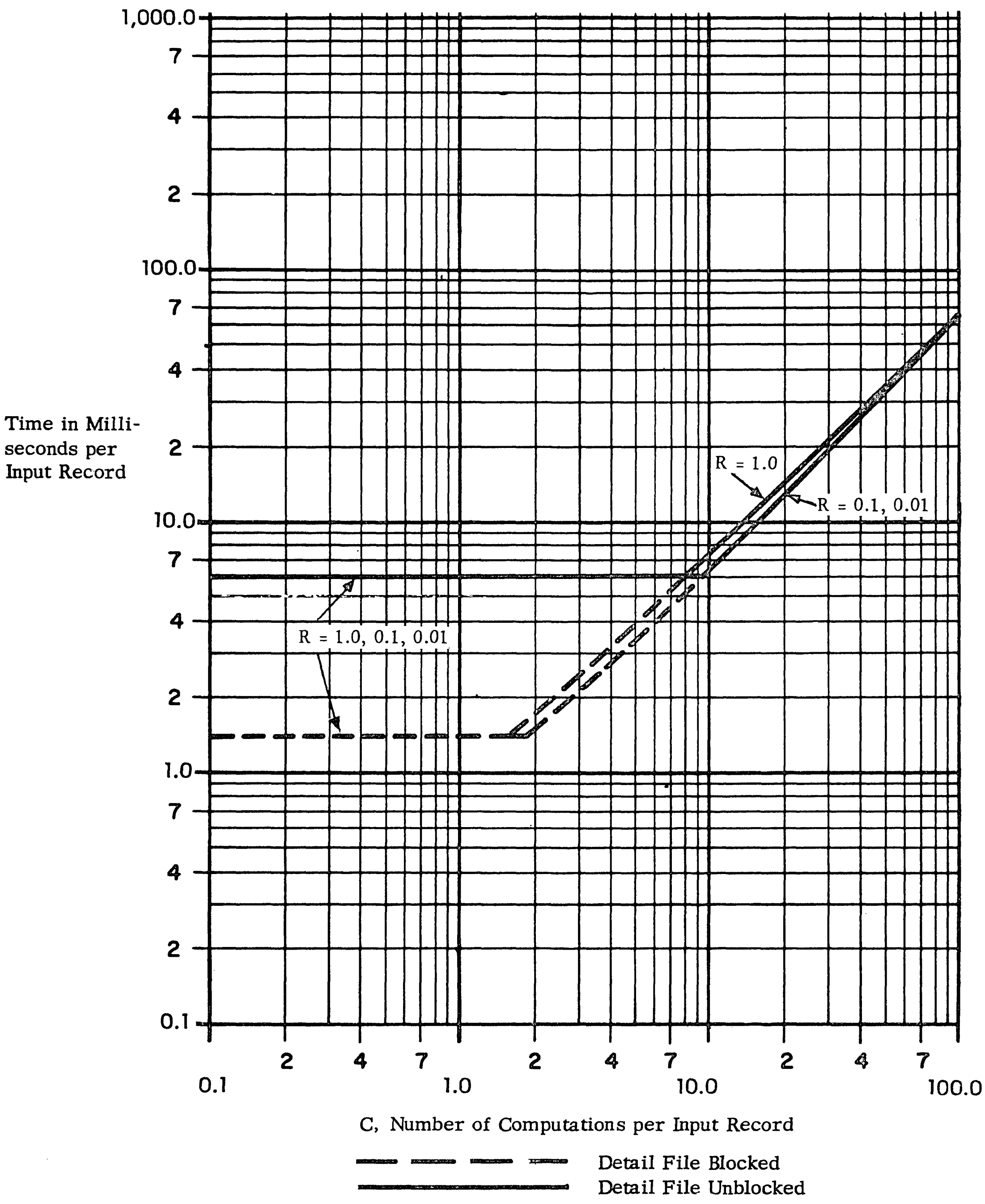
.412 Computation: . . . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.413 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.413.

.414 Graph: . . . . see graph below.

ALL CONFIGURATIONS ONE WORD LENGTH (36 BIT PRECISION); FLOATING POINT

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



§ 201.

.5 GENERALIZED STATISTICAL PROCESSING

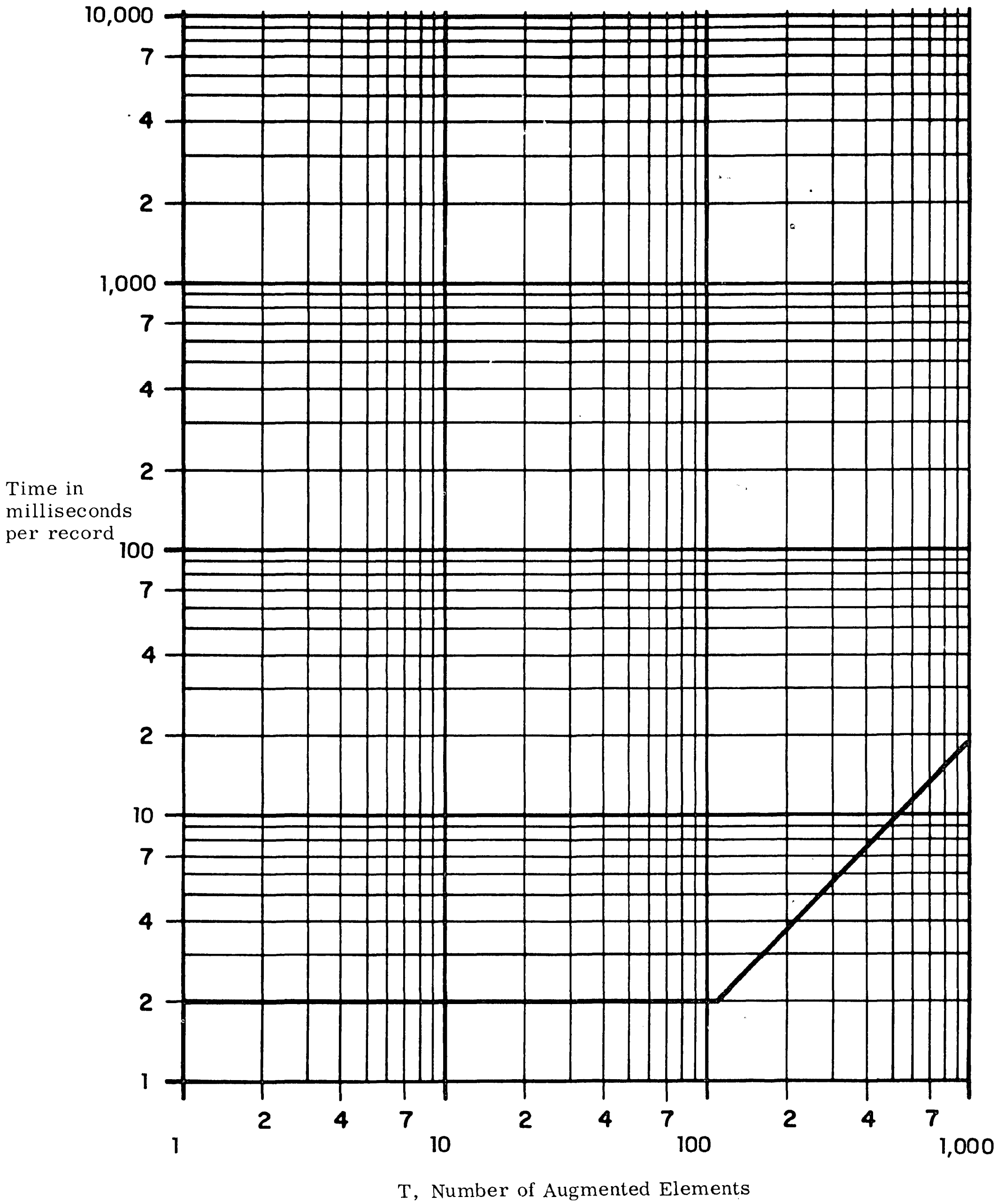
.51 Standard Statistical Problem A Estimates

.511 Record size: . . . . . . thirty 2-digit integral numbers.

.512 Computation: . . . . augment T elements in cross-tabulation tables.

.513 Timing basis: . . . . using estimating procedure outlined in Users' Guide, 4:200.513

.514 Graph: . . . . see graph below.



AUERBACH ®

CDC 3600
PHYSICAL CHARACTERISTICS

CDC 3600 PHYSICAL CHARACTERISTICS

IDENTITY	Unit Name		Console	Data Interchange 1 to 5 Channels	Data Interchange 6 to 8 Channels	Storage Module	Storage Module	Computation Module
	Model Number		3601	3602	3602	3603	3609	3604
PHYSICAL	Height × Width × Depth, in.		44 × 110 × 75[a]	75 × 81 × 20	75 × 121 × 78	75 × 79 × 81	75 × 79 × 81	75 × 161 × 20
	Weight, lbs.		900	2,000	3,100	2,000	1,100	4,000
	Maximum Cable Lengths							
ATMOSPHERE	Storage Ranges	Temperature, °F.						
		Humidity, %						
	Working Ranges	Temperature, °F.	← 50 to 70 (equipment), 60 to 85 (room) →					
		Humidity, %	← 40 to 60 →					
	Heat Dissipated, BTU/hr.		4,300	12,000	18,000	16,000	8,000	17,000
	Air Flow, cfm.		350	700	1,050	700	350	1,400
	Internal Filters		Mechanical filters with a 30% efficiency using N.B.S.[b] discoloration test with atmospheric dust. Electrostatic filters with 90% efficiency at 500 fpm.					

			3601		3602 (1 to 5)		3602 (6 to 8)		3603		3609		3604	
ELECTRICAL	Voltage	Nominal	208	115	208	115	208	115	208	115	208	115	208	115
		Tolerance	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%	10%
	Cycles	Nominal	400	60	400	60	400	60	400	60	400	60	400	60
		Tolerance	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%	5%
	Phases and Lines		3 phase	single phase	3 phase	single phase	3 phase	single phase	3 phase	single phase	3 phase	single phase	3 phase	single phase
	Load KVA		1.0	0.175	3.0	0.35	4.5	0.525	4.2	0.35	2.1	0.175	4.0	0.7

NOTES (Console): [a] Two arms at 120 degrees. [b] National Bureau of Standards.

CDC 3600 PHYSICAL CHARACTERISTICS (Contd.)

			Magnetic Tape Controllers		Peripheral Controller		Magnetic 606 Tape Unit	Card Reader	Card Punch	High Speed Printer	Paper Tape Reader Punch
IDENTITY	Unit Name		Magnetic Tape Controllers		Peripheral Controller		Magnetic 606 Tape Unit	Card Reader	Card Punch	High Speed Printer	Paper Tape Reader Punch
	Model Number		3621-3626		3681-3682		606	3641	3642	3655	3691
PHYSICAL	Height × Width × Depth, in.		78×96×27		75×40×20		72×28×33	41×30×18	52×40×26	61×47×34	40×53×29
	Weight, lbs.		2,000		1,100		800	210	700	1,600	600
	Maximum Cable Lengths										
ATMOSPHERE	Storage Ranges	Temperature, °F.									
		Humidity, %									
	Working Ranges	Temperature, °F.	← 50 to 70 (equipment), 60 to 85 (room) →								
		Humidity, %	← 40 to 60 →								
	Heat Dissipated, BTU/hr.		4,900 to 8,500		4,300		10,000	710	3,600	7,700	5,100
	Air Flow, cfm.		700		350		1,000	100		1,200	540
	Internal Filters		Mechanical filters with a 30% efficiency using N.B.S.[b] discoloration test with atmospheric dust. Electrostatic filters with 90% efficiency at 500 fpm.								
ELECTRICAL	Voltage	Nominal	208	115	208	115	208	115	115	115	115
		Tolerance	10%	10%	10%	10%	10%	10%	10%	10%	10%
	Cycles	Nominal	400	60	400	60	60	60	60	60	60
		Tolerance	5%	5%	5%	5%	5%	5%	5%	5%	5%
	Phases and Lines		3 phase	single phase	3 phase	single phase	3 phase	single phase	single phase	single phase	single phase
	Load KW		1.0 to 1.5	0.35	1.0	0.175	1.2	0.21	1.06	2.3	1.5
NOTES			Variations depend on model used.								

PRICE DATA

§ 221.

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
STORAGE & COMPUTATION	3609	Storage Module, 16,384 Words Magnetic Core Storage	7,455	800	290,000
	3603	Storage Module, 32,768 Words Magnetic Core Storage	14,360	1,285	560,000
	3604	Computation Module; Includes Real Time Clock	20,755	1,825	810,000
	3601	Console; Includes Typewriter	1,790	125	70,000
COMMUNICATION	3602	Communication Module	3,255	275	126,000
	3606	Standard Bi-directional Data Channel	900	125	35,000
	3607	Special 24-bit Data Channel--See Note 1	900	150	35,000
	3608	Special 48-bit Data Channel--See Note 1	900	160	35,000
	3681	Data Channel Converter for 160/160-A; Permits use of 3600 peripheral equipment	275	20	10,800
	3682	Satellite Coupler; Permits direct communication between 160/160-A and 3600	415	25	16,200
INPUT-OUTPUT	3641	Card Reader; 250 cpm	695	150	27,000
	3642	Card Punch; 100 cpm	630	90	24,500
	3643	Card Reader Controller, Controls 088 Card Reader (include the 088)	1,240	100	49,000
	3655	High-Speed Line Printer; 1000 lpm	1,840	400	73,500
	3691	Paper Tape Reader/Punch	640	125	25,000
	3692	Program Controlled Input/Output Typewriter	280	70	11,000
	606	Magnetic Tape Transport	825	140	36,000
	3621	Magnetic Tape Controller; Two Read-Write Controls to control one to eight 606 Magnetic Tape Transports	2,700	215	105,000
	3622	Magnetic Tape Controller; Two Read-Write Controls to control one to sixteen 606 Magnetic Tape Transports	4,000	305	155,000
	3623	Magnetic Tape Controller; Four Read-Write Controls to control one to eight 606 Magnetic Tape Transports	3,600	290	140,000
	3624	Magnetic Tape Controller; Four Read-Write Controls to control one to sixteen 606 Magnetic Tape Transports	4,750	380	185,000
	3625	Magnetic Tape Controller; Three Read-Write Controls to control one to eight 606 Magnetic Tape Transports	3,430	250	133,500
	3626	Magnetic Tape Controller; Three Read-Write Controls to control one to sixteen 606 Magnetic Tape Transports	4,350	340	169,500
POWER	3667	Power Converter and Power Control	795	80	31,000

Note 1: Available for special applications only.

Note 2: Increasing Core Storage from 16K to 32K . . . . $350, 000.

CDC 3100

Control Data Corporation

AUERBACH STANDARD EDP REPORTS

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CDC 3100

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CONTENTS

*Refer to indicated section of the CDC 3200 Computer System Report.

INTRODUCTION

The Control Data 3100 computer system incorporates a slower version of the 3204 Basic Processor used in the Control Data 3200 computer system. It has the same instruction code (which traps and uses subroutines to handle floating-point and decimal operations), the same maximum memory size (32,768 24-bit words), and the same number of available data channels (eight). The core storage cycle time is 1.75 microseconds (versus 1.25 microseconds in the 3204), and the maximum system capacity for input-output data is only 450,000 characters per second (versus the 2,670,000-characters-per-second capacity of the 3200 computer systems). This drastic change in input-output capacity results from the Register File being held in main core storage instead of in a separate, faster store as in the 3200. Only one word of input or output data can be transferred every five machine cycles (four are used by the Register File and one is allocated to the central processor), so that 8.75 microseconds are required for each word transferred.

The Control Data 3100 system, scheduled for first deliveries in January 1965, is priced at up to about $2,000 per month below comparable Control Data 3200 computer systems. Both systems can use all the same peripherals, all the same software packages, and, for practical purposes, all the same programs. In general, however, the subroutines used for decimal and floating-point simulation in the 3100 take about twenty times longer to execute than the machine instructions available in some models of the CDC 3200 processor, so it is expected that 3100 systems will be used either where their program-compatibility with the 3200 systems or their fixed-point binary operating speeds (or both) are found to be valuable.

The Control Data 3100 computer system is machine-code compatible only with the CDC 3200 and 3300 systems. It has, in addition, some compatibility through common programming languages with the Control Data 3400, 3600, and 3800 computer systems.

Hardware

The 3104 is a single-address, fixed word-length, binary processor. It can execute all the instructions in the Control Data 3200 computer system repertoire either by hardware or by software. It is not capable of directly processing instructions requiring floating-point or decimal arithmetic facilities, so the processor automatically "traps" these instructions and simulates their functions by the use of subroutines.

The fixed-point binary instruction times are quite fast: 24-bit addition takes 3.5 microseconds, 48-bit addition takes 5.25 microseconds, and 24-bit multiplication takes 20 microseconds. Simulated floating-point operations take considerably longer: an addition takes 220 microseconds and a multiplication takes 350 microseconds.

An "off-line" search facility allows consecutive locations in core storage to be searched while the main program continues unhindered. The usefulness of this facility is limited by the fact that, unless the program has been carefully designed, core storage may already be "saturated" by the other demands of the processor and peripheral devices. Future developments in this area could, however, be of great value in information storage and retrieval applications.

The Control Data 3100 system can be equipped with up to eight input-output data channels, enabling the system to compute while simultaneously performing up to eight read-write operations which use any eight peripheral devices in the system. Use of the available buffered peripheral units, which require little data channel time, can allow the number of concurrently operating peripherals to increase to well beyond the number of data channels in a system.

Many of the input-output controllers supplied with Control Data 3100 computer systems have two or more data channel connections. Such controllers can be used to switch peripheral units between two computer systems. The use of more than one central processor in an installation is comparatively frequent in Control Data 3000 Series installations, as both peripheral units and storage modules can be easily switched under program control.

Significant recent announcements by Control Data have included IBM System/360-compatible magnetic tape units and the provision of controllers for the IBM 1311 and 2311 Disk Storage Drives. The present peripheral units available with the 3100 computer system (and with all Control Data 3000 Series computer systems) include:

- Model 828 and 838 Disk Files –
  Capacity: 33 or 66 million characters
  Access time: 187 milliseconds average

- IBM 1311 and 2311 Disk Storage Drives —
  Capacity: 3 or 9.7 million characters
  Access time: 170 milliseconds average

- Model 3235 Drum Storage —
  Capacity: 0.5 million characters
  Access time: 17 milliseconds average
  Data transfer rate: 167,000 characters per second

- Model 861 and 862 Drum Storage —
  Capacity: 4.2 or 2.1 million characters
  Access time: 17 or 8.6 milliseconds average
  Data transfer rate: up to 2,000,000 characters per second

- Punched card equipment —
  Maximum reader speed: 1,200 cards per minute
  Maximum punch speed: 250 cards per minute

- Paper tape equipment —
  Maximum reader speed: 1,000 frames per second
  Maximum punch speed: 110 frames per second

- Line printing equipment —
  CDC 501: 1,000 lines per minute
  CDC 505: 500 lines per minute
  CDC 3152: 150 lines per minute
  IBM 1403 Model 2: 600 lines per minute
  IBM 1403 Model 3: 1,100 lines per minute

- 7-track and 9-track magnetic tape units —
  Maximum 7-track speed: 120,000 six-bit characters per second
  Maximum 9-track speed: 90,000 eight-bit characters per second

Software

The major assembly language for the Control Data 3100, 3200, and 3300 computer systems is called 3200 COMPASS. It bears only a general resemblance to the COMPASS language used for the Control Data 3600, and programs written in the two assembly languages are not interchangeable. The 3200 COMPASS assembler requires 8,192 words of core storage and 5 input-output devices, including at least 2 magnetic tape units, during the assembly process. The output of the assembler is machine-language coding suitable for use with the SCOPE Operating System. A reduced form of the 3200 COMPASS assembler, with no macro facilities, is available for Control Data 3100 computer systems which have only 4,096 words of storage.

The standard mathematical compiler is 3200 FORTRAN. This compiler uses a FORTRAN IV style language which is not simply an exact copy of some other language, but rather an independently designed scientific programming language that offers a number of performance-improving features. In this respect it appears that Control Data is continuing a policy established in its FORTRAN-63 compiler for the CDC 1604, that of constructively re-evaluating the "standard" language before implementation. This policy gives promise of continued improvements in FORTRAN.

Programs written in 3200 FORTRAN can be compiled on any Control Data 3100, 3200, or 3300 computer system that has at least 8,192 words of core storage, 3 magnetic tape units, and 2 other input-output devices. The 3200 FORTRAN compiler was released to customers in November 1964. A Basic FORTRAN II system is available for smaller configurations.

COBOL language processing is provided for the Control Data 3100, 3200, and 3300 computer systems by the 3200 COBOL compiler. The language includes almost all of Required COBOL-61, and the compiler requires a 4,096-word system with 3 tape units and 2 other input-output devices for compilation. Release of 3200 COBOL to customers is scheduled for March 1965.

The SCOPE Operating System helps to assemble programs and to provide input-output services as required. It uses between 700 and 1,500 core storage locations to hold the resident program during operation; the exact amount depends upon the number and type of input-output routines required by a particular program. At present 3200 SCOPE is oriented toward magnetic tape processing, but a random access enhancement, specifically designed to service the IBM 1311 and 3211 Disk Storage Drives, is expected to be released in Spring 1965.

Other program packages under development include a Report Generator (scheduled for June 1965), a Linear Programming Package (June 1965), and a PERT Package (March 1965).

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	24 bits	basic addressable unit (data or instruction).
Character:	6 bits	addressable data unit.
Block:	1 to N characters or 1 to N words	Search, Move, and Input-output instructions.

.2 INFORMATION FORMAT

Type of Information	Representation
Operand:	24- or 48-bit fixed point word. 48-bit floating point word. 6-bit character. 4-bit BCD character.
Instruction:	1 or 2 words.
Field:	1 to 13 BCD characters.

SYSTEM CONFIGURATION

GENERAL

Every Control Data 3100 computer system includes the following units:

- A 3104 Processor.
- A 1.75-microsecond Core Storage Unit ranging from 4,096 to 32,768 words (16,384 to 131,072 characters) in capacity.
- An integrated console with detachable keyboard.
- A Power Converter and Control Unit.

One 3106 Data Channel is included in the basic system. Up to seven more can be added, so that a fully-extended Control Data 3100 computer system will have eight data channels. Eight peripheral units or controllers can be connected to each data channel.

The data channels used in all of the Control Data 3000 Series computers present a common interface with peripheral units. As a result of this, any of the 3000 Series peripheral units can be connected through a 3106 Data Channel to a Control Data 3100 computer. The available peripheral units are described in the Control Data 3200 Computer System Report. Details of the loadings these units place on a Control Data 3100 computer system are described in the Simultaneous Operations section of this report, starting on page 254:111.100.

Some peripheral units or controllers can be connected to more than one data channel. This facility may be used either to allow two concurrent data transmissions to take place, or to allow the peripheral unit to be switched between two computer systems. A bank of magnetic tape units connected to a dual-channel controller is a case where multiple data transmissions would be the normal reason for having the two data channels; while a printer connected to two different computer systems by way of a dual-channel controller could be used by either system, as the situation in the computer room demands.

The core storage modules can similarly be connected to, and accessed by, two computers. Each 16,384-word module is independent and permits dual access by a second processor or special device.

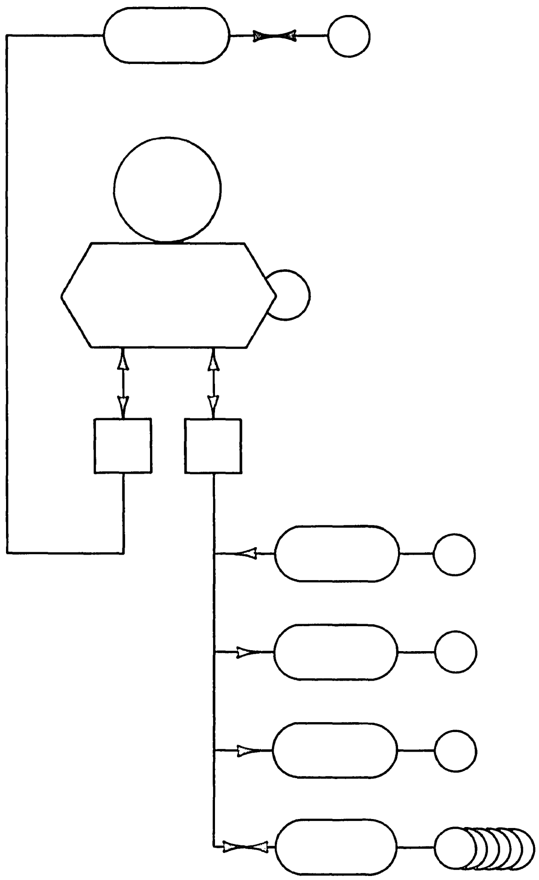
SELECTION OF REPRESENTATIVE CONFIGURATIONS

The Control Data 3200 computer system is shown in the following Standard System Configurations, as defined in the Users' Guide, page 4:030.100:

- Configuration V; 6-Tape Auxiliary Storage Configuration.
- Configuration VI; 6-Tape Business/Scientific Configuration.
- Configuration VIIA; 10-Tape General Integrated Configuration.
- Configuration VIIB; 10-Tape General Paired Configuration, using a Control Data 160 Computer System as the satellite system.

.1 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V

Deviations from Standard Configuration: . . . . auxiliary storage capacity is 65% larger.
card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 40% faster.

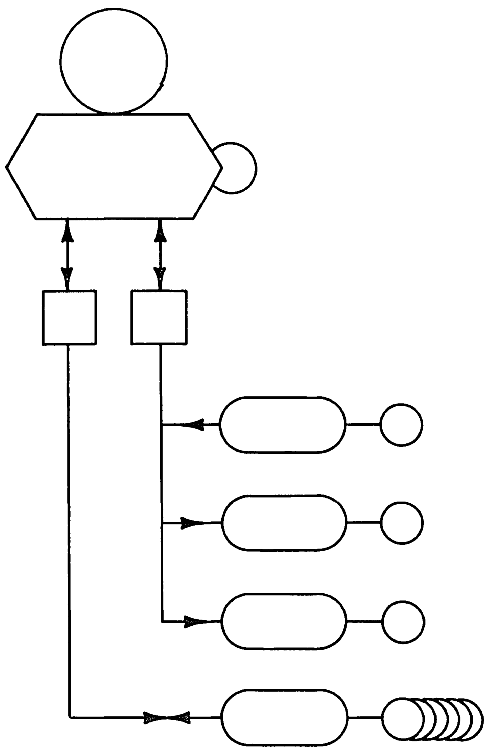


Equipment	Rental
828 Disk File (33 million char)	$ 2,400
3432 Controller	1,050
8,192 words of Core Storage	700*
3104 Computer	2,700*
Monitor Typewriter	240
3106 Data Channels (2)	120*
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3245 Controller	330
505 Line Printer (500 lpm)	635
3256 Line Printer Controller	515
603 41.7KC Magnetic Tape Units (6)	3,300
3229 Controller	600
TOTAL RENTAL:	$13,385

* The rental for the 3104 Computer includes the charges for the first 4,096 words of core storage and for the first 3106 Data Channel.

.2 6-TAPE BUSINESS/SCIENTIFIC SYSTEM; CONFIGURATION VI

Deviations from Standard Configuration: . . . . card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 40% faster.
no floating point hardware.

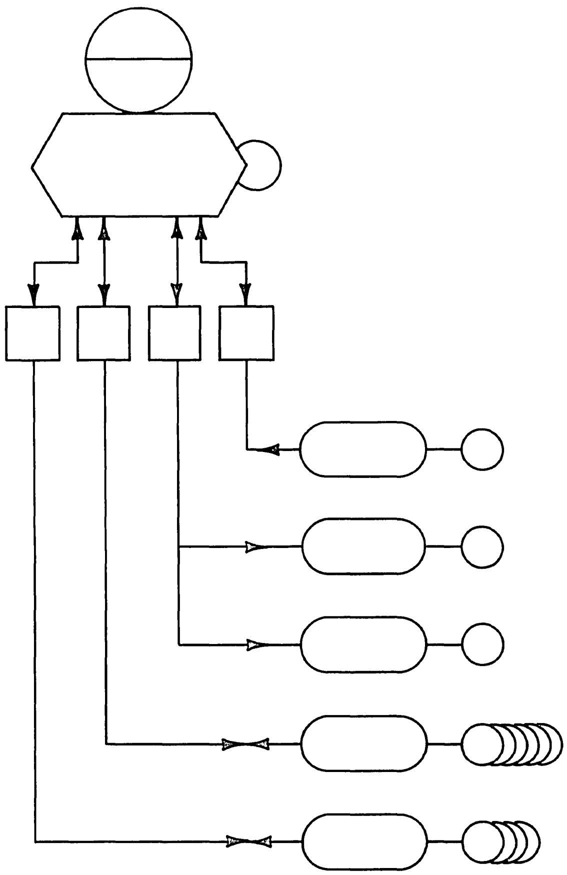


Equipment	Rental
16,384 words of Core Storage	$ 1,510*
3104 Computer	2,700*
Monitor Typewriter	240
3106 Data Channels (2)	120*
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3246 Line Printer	515
603 41.7KC Magnetic Tape Units (6)	3,300
3229 Controller	600
TOTAL RENTAL:	$10,865

* The rental for the 3104 Computer includes the charges for the first 4,096 words of core storage and for the first 3106 Data Channel.

.3 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . core storage is 33% larger.
3 less index registers provided.
card reader is 140% faster.
card punch is 150% faster.
no floating point.

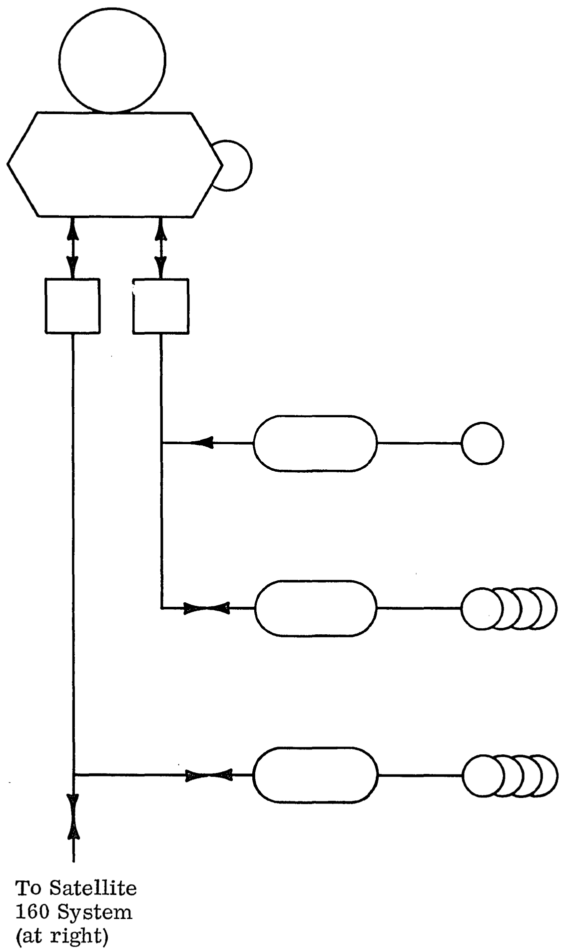


Equipment	Rental
32,768 words of Core Storage	$ 3,310*
3104 Computer	2,700*
Monitor Typewriter	240
3106 Data Channels (4)	360*
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
604 60KC Magnetic Tape Units (6)	3,600
3229 Controller	600
604 60KC Magnetic Tape Units (4)	2,400
3228 Controller	425
TOTAL RENTAL:	$16,030

* The rental for the 3104 Computer includes the charges for the first 4,096 words of core storage and for the first 3106 Data Channel.

.4 10-TAPE GENERAL SYSTEM (PAIRED); CONFIGURATION VIIB*

Deviations from Standard Configuration: . . . . 3 less index registers.
direct connection to satellite system.
card reader is 1100% faster.
no floating point hardware.

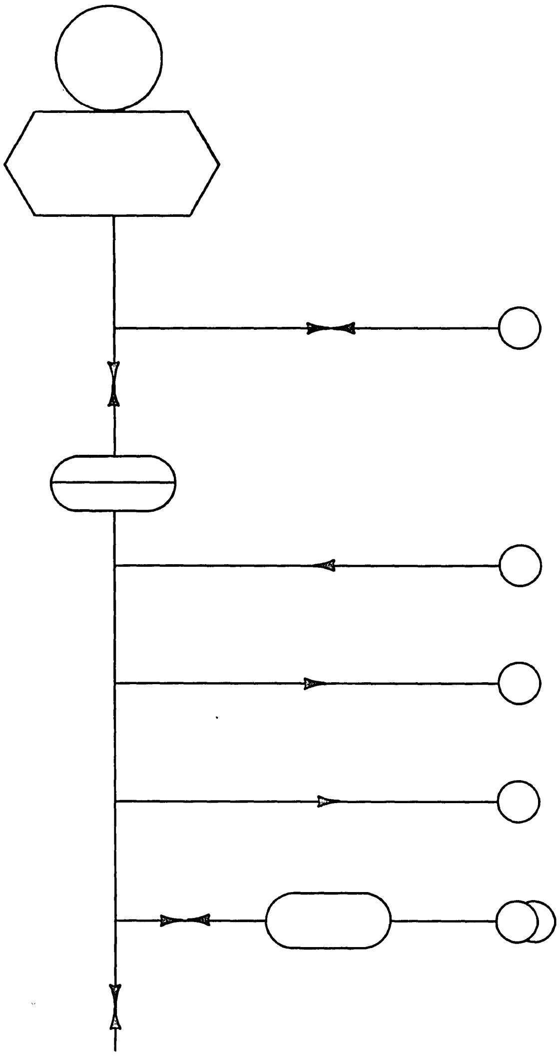


Equipment	Rental
16,384 characters of Core Storage	$ 1,510*
3104 Computer	2,700*
Monitor Typewriter	240
3106 Data Channels (2)	120*
405 Card Reader (1,200 cpm)	400
3248 Controller	100
604 60KC Magnetic Tape Units (4)	2,400
3228 Controller	425
604 60KC Magnetic Tape Units (4)	2,400
3228 Controller	425
TOTAL ON-LINE EQUIPMENT:	$10,720
TOTAL SATELLITE EQUIPMENT:	$ 5,165
TOTAL RENTAL:	$15,885

* This rental for the 3104 Computer includes the charges for the first 4,096 words of core storage and for the first 3106 Data Channel.

SATELLITE EQUIPMENT (CDC 160)

Deviations from Standard Configuration: . . . .
direct connection to main system.
core storage is 100% larger.
multiply/divide is included.
paper tape equipment is included.
card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 30% slower.



Equipment	Rental
4,096 words of Core Storage 160 Processor Console with Monitor Typewriter Paper Tape Reader (350 cps) Paper Tape Punch (110 cps)	$1,500
3681 Data Channel Converter	275
3682 Satellite Coupler	175
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
601 21KC Magnetic Tape Units (2)	500
3127 Controller	320
TOTAL SATELLITE EQUIPMENT:	$5,165

To 3100 System
(at left)

INTERNAL STORAGE: CORE STORAGE

.1 GENERAL

.11 Identity: . . . . 3103 Storage Module (16K).
3108 Storage Module (4K).
3109 Storage Module (8K).

.12 Basic Use: . . . . . working storage and operational control.

.13 Description

A Control Data 3100 computer system can have between 4,096 and 32,768 24-bit word locations of core storage, operating with a cycle time of 1.75 microseconds per word. Overlapping of storage cycles, in order to reduce the loading placed on the central processor by input-output operations, is only possible in those systems which have 32,768 words; in smaller systems all of the core storage cycles at the same time, making it impossible to overlap one cycle with another.

Sixty-four words of core storage are reserved for an Integrated Register File. This file contains the sequence control registers, input-output controls, and Autoload and Autodump entries. The functions of the Integrated Register File are described in the central processor section of this report, on page 254:051.100.

Each physical storage location consists of 28 bits, of which 24 are data bits and 4 are parity bits. The 24 data bits are functionally broken down into four 6-bit characters, and one of the parity bits is associated with each separate character. Addressing of core storage can be by word or character, using 15 bits or 17 bits per address, respectively.

The core storage can be connected directly to a single Control Data 3104 central processor, or it can be shared by two independent 3104 processors. When the core storage is shared, manual switches on the outside of each module allow the operator to allocate the store to either computer, or to enable them to share it on a no-priority basis.

.14 Availability: . . . . . ?

.15 First Delivery: . . . January, 1966.

.16 Reserved Storage: . . 64-word Integrated Register File.

.2 PHYSICAL FORM

.21 Storage Medium: . . magnetic cores.

.23 Storage Phenomenon: direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . yes.
.242 Data regenerated constantly: . . . . . no.
.243 Data volatile: . . . . no (safeguarded by power-off interrupt).
.244 Data permanent: . . . no.
.245 Storage interchangeable: . . . . no.

.27 Interleaving Levels: . no interleaving as such; however, two 3103 Storage Modules provide asynchronous operation with overlapped accesses.

.28 Access Techniques: . coincident current.

.29 Potential Transfer Rates

.292 Peak data rates -
Cycling rates: . . . 570,000 cps.
Unit of data: . . . . word or character.
Data rate: . . . . . 570,000 words (or characters)/sec.

.3 DATA CAPACITY

.31 Module and System Sizes
(See table below.)

.32 Rules for Combining Modules: . . . . . four possibilities are shown in preceding entry; there may be others.

.4 CONTROLLER

.41 Identity: . . . . no separate controller required.

.31 Module and System Sizes

	Minimum Storage			Maximum Storage
Identity:	3108 Storage Module	3109 Storage Module	3103 Storage Module	2 3103 Storage Modules
Modules:	1	1	1	2
Words:	4,096	8,192	16,384	32,768
Characters:	16,384	32,768	65,536	131,072
Instructions:	4,096	8,192	16,384	32,768

.42 Connection to System: one core memory can be connected to one or two 3104 Central Processors.

.5 ACCESS TIMING

.51 Arrangement of Heads: 1 read/write control per system, except for 32K systems, which have 2 read/write controls and permit overlapped operations.

.52 Simultaneous Operations: . . . . none, except in 32K systems, where access to each 16K module is asynchronous and independent.

.53 Access Time Parameters and Variations

.531 For uniform access -
Access time: . . . . ?
Cycle time: . . . . 1.75 μsec.
For data unit of: . . 1 word or 1 character.

.6 CHANGEABLE STORAGE: . . . . . none.

.7 STORAGE PERFORMANCE

.72 Transfer Load Size

With self: . . . . . . 1 to 128 characters, one character at a time.
1 to 32 words, four characters (i.e., one word) at a time.

.73 Effective Transfer Rate

With self: . . . . . . 91,000 words/second.

.8 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Invalid address:	none	high-order bits are truncated.
Invalid code:	not possible.	
Receipt of data:	generate parity bit.	
Recording of data:	record parity bit.	
Recovery of data:	parity check	halt operation; console light.
Dispatch of data:	send parity bit.	
Timing conflicts:	interlock until cleared.	

CENTRAL PROCESSOR

.1 GENERAL

.11 Identity: . . . . 3104 Computer.

.12 Description

The 3104 Computer is the only available central processor for the Control Data 3100 computer system. It is a fixed-point binary processor with built-in subroutines entries for floating-point and decimal operations, exactly the same as the 3204 Basic Processor. There are no optional facilities available for the 3104 Computer; the 3100 system is upward-compatible with both the Control Data 3200 and 3300 computer systems, and it is anticipated that users will move on to these systems rather than build up the capacity of the 3104.

Word length of core storage locations is 28 bits (24 data bits plus 4 parity bits). One location can contain an instruction, a 24-bit fixed-point binary data word, one half of a 48-bit fixed- or floating-point data word, or an alphanumeric word consisting of four 6-bit BCD characters. An instruction word normally consists of a 6-bit operation (or function) code, an addressing mode bit (indirect or direct), a 2-bit index register designator, and a 15-bit core storage address field. In some cases the indirect addressing flag, index register designation, and address bits are used for other purposes such as operand values, shift counts, and extensions of the function code or address field. Only three index registers are provided, and their use is pre-empted by various instructions. To some extent this limits the programmer in his use of automatic address modification techniques.

Operations which are performed by hardware are fast, although not as fast as in the 3200 processors. A fixed-point 24-bit addition requires only 3.5 microseconds. Multiplication operations take from 10.6 to 14.8 microseconds. Search operations take 5.4 microseconds for each operand inspected.

Floating-point operations, which must be handled by subroutines, naturally take longer, A 48-bit add operation takes about 200 microseconds, multiplication takes 330 microseconds, and division takes about 600 microseconds. The times required for simulation of decimal arithmetic operations have not yet been determined.

The Register File, which controls the input-output operations, searches, and moves and performs other control functions, is held in the upper areas of core storage rather than in a special fast-access file as in the Control Data 3200 and 3300 computer systems.

The "block" operations use special processor controls and are of three types: Search, Move, and Input-Output. After one of these operations has been activated, the processor can return to its main program and continue until an interrupt is generated or the program senses completion of the block operation. Each of these operations requires three instruction words, which contain the starting and ending addresses (or source and destination addresses for a Move command) for the operation and a "reject" instruction. The reject instruction is used if the block controls or the addressed input-output data channel happens to be busy. All three types of block operations are carried out on a character-by-character basis. The input-output instructions, which can also specify a word-by-word transfer, are described in more detail under Simultaneous Operations (Section 245:111).

The 3100 has a program interrupt system which permits interruption when any of the following conditions occur: arithmetic faults (overflow, divisor too small, exponent too large), completion of a block operation (search, move, or input-output), manual switch operation (console key), an interrupt request from any of the eight peripheral positions on each data channel, or a real-time interrupt controlled by the Real-Time Clock. When an interrupt condition is recognized, the current instruction address is stored along with a number that indicates the specific interrupt condition, and program control is transferred to a fixed location. The programmer, however, can choose to honor or ignore any particular interrupt condition by setting appropriate bits in an Interrupt Mask register. In addition, several instructions are available for sensing and clearing interrupts independently, and for either enabling or disabling the entire interrupt system.

A special power failure interrupt automatically (and unequivocally) transfers control to a fixed location (location 00010) in the event power fails within the 3100 system. A special routine then prepares the system for an orderly shutdown so that no data will be lost. The whole operation takes a maximum of 30 milliseconds; 16 milliseconds for detection, and 14 milliseconds for processing the interrupt.

.13 First Delivery: . . . . . January 1965.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add-subtract:	automatic	binary	24 bits.
		automatic	binary	48 bits.
		subroutine	decimal	1 to 12 BCD chars.
	Multiply —			
	Short:	none.		
	Long:	automatic	binary	24 bits.
		subroutine	binary	48 bits.
		subroutine	decimal	variable.
	Divide —			
	No remainder:	none.		
	Remainder:	automatic	binary	24 bits.
		subroutine	binary	48 bits.
		subroutine	decimal	variable.
.212	Floating point —			
	Add-subtract:	subroutine	binary	36 & 11 bits.
	Multiply:	subroutine	binary	36 & 11 bits.
	Divide:	subroutine	binary	36 & 11 bits.
.213	Boolean —			
	ADD	automatic	binary	24 bits.
	Inclusive OR:	none.		
	Exclusive OR:	automatic	binary	24 bits.
.214	Comparison —			
	Numbers:	automatic.		
	Absolute:	none.		
	Letters:	automatic.		
	Mixed:	6-bit characters.		
	Collating sequence:	0-9, A-Z, with special characters and unassigned symbols in various places; see page 245:141.100 in CDC 3200 Computer System Report.		

.215 Code translation:

Code translation from external BCD to internal BCD is automatic when magnetic tapes recorded in BCD format are being used.

Details of other code translations needed, and the timing of the subroutines used to accomplish the translations, are shown in Table I.

.216 Radix conversion:

Radix conversion between BCD and binary forms is performed by standard subroutines. The timings of these subroutines are listed in Table I.

.217 Edit format: . . . . own coding; the character-by-character search for equality or inequality appears to be the only instruction specifically oriented toward this task.

	Operation	Provision	Size	Comment
.218	Table look-up —			
	Equality:	automatic	by word	entries may be spaced every 1, 2, 3, 4, 5, 6, 7, or 8 words. Masked operands are allowed.
	Greater than:	automatic	by word	
	Greatest:	none.		
	Least:	none.		
.219	Others —			
	Character Search:	automatic	character-by-character	the search is made off-line, using the block transfer facilities; single character equality or inequality can be searched for.

TABLE I: CONVERSION TIMES FOR STANDARD SUBROUTINES

ORIGINAL OPERAND		MICROSECONDS REQUIRED FOR CONVERSION TO:				
Type	Magnitude	Internal BCD (1)	Fixed Point Binary (2)	Floating Point Binary (3)	Column BCD (4)	Row BCD (5)
Internal BCD	$< 10^7$	—	18/digit	18/digit + 25/operand	7,000/card	42,000/card
Internal BCD	$\geq 10^7$	—	32/digit	32/digit + 25/operand	7,000/card	42,000/card
Fixed Point Binary	$< 10^7$	31/digit	—	25/operand	31/digit + 7,000/card	31/digit + 42,000/card
Fixed Point Binary	$\geq 10^7$	62/digit	—	25/operand	62/digit + 7,000/card	62/digit + 42,000/card
Floating Point Binary	$< 10^7$	31/digit + 39/operand	39/operand	—	31/digit + 39/operand+ 7,000/card	31/digit + 39/operand + 42,000/card
Floating Point Binary	$\geq 10^7$	62/digit + 39/operand	39/operand	—	62/digit + 39/operand + 7,000/card	31/digit + 39/operand + 42.000/card

(1) Internal BCD is used in decimal arithmetic, for card reader input and for printer output.
(2) Fixed Point Binary is used for 24 or 48-bit binary arithmetic.
(3) Floating Point Binary is used for all floating point operations.
(4) Column BCD is used for output via buffered card punch equipment.
(5) Row BCD is used for output via unbuffered card punch equipment.

Note: "digit" refers to decimal digits in all of the above times.

.22 Special Cases of Operands

.221 Negative numbers: . . . one's complement.
.222 Zero: . . . . positive zero and negative zero.
.223 Operand size determination: . . . . normally 24 bits; 48 bits available in double precision and floating point instructions, and variable length of 1-12 decimal digits in BCD operations.

.23 Instruction Formats

.231 Instruction structure: . basically 1-address.
.232 Instruction layout

Part:	f	a	b	m
Size (bits):	6	1	2	15

.233 Instruction parts

Name	Purpose
f:	function code.
a:	indirect addressing flag.
b:	index register designation.
m:	operand address.

Note: In many cases the indirect addressing flag and the index register designation are used for other purposes. These cases include:

- when literals are used instead of operand addresses;
- when Search or Move operations are involved;
- when the operand address is a register;
- when selective jumps based on console keys are involved.

In most BCD character operations, indirect addressing is not available, and only one specific index register can be used with a particular instruction.

Register file addresses cannot be indexed or indirectly addressed.

.234 Basic address structure: . . . . 1 + 0.
.235 Literals —
Arithmetic: . . . . no facility.
Comparisons and tests: . . . . literals can be compared with index register counts and accumulator contents only; maximum size is 262,145.
Incrementing modifiers: . . . . only in the Block Search operation.
.236 Directly addressed operands —
Internal storage type: . . . . core storage.
Minimum size: . . . . . 1 character.
Maximum size: . . . . 1 or 2 words.
Volume accessible: . . all.
.237 Address indexing
.2371 Number of methods: . two.

.2372 Names: . . . . normal indexing.
specific indexing.

.2373 Indexing rule (normal indexing): . . . . addition of contents of one of the 3 index registers to the address in one's complement mode.

.2373 Indexing rule (specific indexing): . . . . same as normal indexing except that a specified index register is always used with the particular instruction.

.2374 Index specification: . . bits 15 and 16, or bit 17, of instruction word.

.2375 Number of potential indexers: . . . . 3.

.2376 Addresses which can be indexed: . . . . . . operand addresses in arithmetic, logical, load, and store instructions, and some jump instructions.

.2377 Comulative indexing: . no.

.2378 Combined index and step: . . . . no.

.238 Indirect addressing

.2381 Recursive: . . . . yes.

.2382 Designation: . . . . . . single bit in appropriate instructions and in each indirect operand address.

.2383 Control: . . . . the last address in the recursive sequence is the first address reached which has no indirect addressing flag.

.2384 Indexing with indirect addressing: . index modification always takes place first. All levels of a recursive indirect address sequence may be indexed.

.239 Stepping

.2391 Specification of increment: . . . . . . within instruction.

.2392 Increment sign: . . . . + or -.

.2394 End value: . . . . positive zero; tests are also available for comparison with literals.

.2395 Combined step and test: . . . . yes, for ± 1 increments only.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size in bits	Program usage
Registers:	3	24	arithmetic and instructions.
Registers:	4	14	address handling.
Registers:	57	24	I/O control, clock, temporary storage, etc.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: . . . . sequential.

.32 Look-Ahead: . . . . none.

.33 Interruption

.331 Possible causes —

In-out units: . . . . . . the state of any specific device connected to one of the eight I/O controllers can initiate an interrupt. Conditions which can cause interrupts vary for different types of I/O devices, but usually include normal end of an operation, abnormal end, and inability to respond to an instruction.

In-out controllers: . . the failure of an I/O controller to accept or reject a Connect or Function instruction.

Processor errors: . . arithmetic overflow.
divide fault (division by too small a number, not simply by zero).
exponent overflow ($>2^{10}-1$).
BCD fault (irregular characters).

Other: . . . . power failure.
real-time clock.
search-move interrupt.

.332 Control by routine: . . . interrupts may be masked by the program. In addition, they are automatically inhibited (except for the Power Failure Interrupt) by the entry into any interrupt routine, and a special instruction must be used to re-enable the preselected interrupts after each interrupt.

.333 Operator control: . . . . none, except that he always may originate a manual interrupt, or use the six Sense switches to set the mask.

.334 Interruption conditions: (1) an interrupt condition must arise.
(2) it must not be inhibited either permanently or during the processing of an interrupt routine.
(3) the priority scanner must have reached the priority level of the interrupt condition.

.335 Interruption process —

Disabling interruption: . . . . operating instruction proceeds to an orderly halt.

Registers saved: . . . program address register only.
A nine-bit interrupt identification code is placed in a fixed location.

Destination: . . . . . . 00003 or 00010.

.336 Control methods —

Determine cause: . . . own coding.

Enable interruption: . own coding.

.34 Multiprogramming: . . no special provisions.

.35 Multi-Sequencing: . . . the block operations (search for character equality/inequality, move characters, input-output instructions) can proceed in parallel with and independently of the main program, once initiated.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

	Binary (24 bits)
.411 Fixed point —	
Add-subtract:	3.5
Multiply:	10.6 to 14.8
Divide:	14.5
.412 Floating point —	
Add-subtract:	210.*
Multiply:	340.*
Divide:	600.*
.413 Additional allowance for —	
Indexing:	0.53
Indirect addressing:	1.8
Re-complementing:	zero.
.414 Control —	
Compare:	2.6
Branch:	1.8
Compare and branch:	2.6
.415 Counter control —	
Step:	1.8
Step and test:	2.6
Test:	2.6
.416 Edit:	not available.
.417 Convert:	see Table I.
.418 Shift:	1.8 to 5.3.

.42 Processor Performance in Microseconds

.421 For random addresses —

	Fixed point (24 bits)	Floating point* (48 bits)
c = a + b:	10.5	220.
b = a + b:	8.8	2220
Sum N items:	3.5N	220N.
c = ab:	19.7	350.
c = a/b:	23.3	600.

* Performed by subroutine initiated by "trapped" instruction code.

.422 For arrays of data —

	Fixed point (24 bits)	Floating point* (48 bits)
$c_i = a_i + b_j$	16.49	230.
$b_j = a_i + b_j$	14.26	230.
Sum N items:	6.63N	230N.
$c = c + a_i b_j$	28.66	360.

.423 Branch based on comparison —
Numeric data: 21.53
Alphabetic data: 21.53

.424 Switching —
Unchecked: 7.63
Checked: 12.83
List search: . . . . . . 20.03+5N

.425 Format control, per character —
Unpack: . . . . 170.
Compose: . . . . 170.

.426 Table look-up, per N comparisons —
For a match: . . . . . . 5.4 + 5.4N
For least or greatest: 5.4 + 5.4N
For interpolation point: . . . . 5.4 + 5.4N

.427 Bit indicators —
Set bit in pattern: . . . 10.5
Test bit in pattern: . . 7.9

.428 Moving, per N words: . 7.0 + 11.0N (91,000 24-bit words/sec).

.5 ERRORS, CHECKS AND ACTION

Error	Check or Interlock	Action
Overflow:	check	specific bit is set; optionally, interrupt occurs (interrupt system is deactivated, instruction address is stored, and a forced jump is made to a specific location for each case).
Underflow:	check	(same)
Divisor too small:	check	(same)
Shift faults:	check	(same)
Invalid instructions:	check	(same)
Abnormal end of an I/O operation:	check	(same)
Storage reference:	parity check	optional halt; console light.
Receipt of data:	parity check	optional halt; console light.
Internal reject:	parity check	optional halt; console light.
Dispatch of data:	parity bits are included, but not checked.	none.

CONSOLE

.1 GENERAL

.11 Identity: . . . . 3101 Desk Console.
Integrated Console.

.12 Associated Unit: . . Input-Output Typewriter.

.13 Description

Two consoles, functionally identical to each other, are available for the Control Data 3100 system — the optional 3101 Desk Console and the standard Integrated Console. Both consoles have indicators for displaying various register contents and conditions within the system. Binary displays are provided, but not octal or decimal displays. Seven groups of display lights are used to display the operational registers of the computer.

A movable input keyboard is incorporated in both console designs. This keyboard can either be operated at the console or removed and carried to a suitable nearby location. An input-output typewriter is included with the 3101 Desk Console, or it can be separately obtained as the Model 3192 On-line Monitor Typewriter. These units (the keyboard and the input-output typewriters) do not use the regular data channels during operation, but have their own buffer registers and direct access to the computational module.

The 3101 Desk Console provides ample desk space and a good view. The Integrated Console provides a standup operator control panel for space-limited or multiple-processor installations.

The "external" status indicators display the existing condition of the input-output channels, while six columns of "internal" condition indicators provide the following information:

- Storage Active — for addressing purposes, the four possible 8,192-word sections of storage are designated by digits 0-3. Whenever one of these storage sections becomes active, the corresponding indicator light is lit.
- Conditions — a Standby light indicates that the main power switch is on, but that individual supplies are still off; an Interrupt Disabled light is on whenever the interrupt system is disabled by the program.
- Cycle — four cycles are represented: Read Next Instruction, Read Address, Read Operand, and Store Operand. These indicators are lit whenever the cycles are in progress.
- Faults — these lights represent four arithmetic faults: Arithmetic Overflow, Divide, Exponent Overflow, and Decimal (BCD).
- Temperature Warning and Temperature High — up to four cabinet sections are represented.

The console switches are divided into two groups — those used for normal operations of the system and those used primarily for maintenance purposes. Operational switches are included on the main console and on an entry keyboard. The keyboard replaces the Set and Clear pushbuttons that are found on most Control Data computers for the manual entry of information.

The main console switches provide for such operating controls as breakpoint/run mode selection, automatic load/dump initiation for a designated device, selective jump instruction keys, manual interrupt, and master clear buttons. The keyboard switches provide for start and stop controls, register display control, and the manual entry of information into core storage or a designated register.

INPUT–OUTPUT AND RANDOM ACCESS PERIPHERAL UNITS

All of the Control Data 3000 Series computers, including the CDC 3100 system, use the same input-output units, the same random access storage units, and the same controllers. The program-compatible Control Data 3100, 3200, and 3300 computers also use the same supporting routines, although naturally both the timing of the routines and the loads placed on the core storage modules by the input-output operations will vary between the different computer systems. In order to place proper emphasis upon the family similarities and differences, our coverage of the Control Data 3000 Series peripheral units as used in the CDC 3100 system is organized as follows:

The Control Data 3200 Computer System Report includes:

- The DESCRIPTION of each unit and controller (see pages 245:042.100 through 245:102.100).
- The PRICE of each unit and controller (see page 245:221.101).
- The details of the SUPPORT PROGRAMS (if any) for each unit.

This Computer System Report includes:

- The LOADING that each peripheral unit imposes on the 3100 core storage modules (see the Simultaneous Operations section, page 254:111.101).
- The TIMING details for code and radix conversions used in connection with peripheral operations (see the Central Processor section, page 254:051.220).

SIMULTANEOUS OPERATIONS

1. GENERAL

The Control Data 3100 system allows for the connection of up to eight input-output data channels. Each data channel is serviced by a bi-directional, 12-bit parallel interface unit called the 3106 Standard Communication Channel †. Up to eight different peripheral equipment controllers can be connected to one 3106. These facilities make it possible for up to eight input-output operations on any of 64 different controllers to proceed simultaneously with computation.

A choice of single- and dual-channel controllers is available for the card and printer equipment. Full line buffers are included with each of the printer controllers, but card buffers are optional depending upon the choice of card reader or card punch controller. The magnetic tape units, paper tape units, and typewriter simply have 12-bit interfaces.

Magnetic tape controllers can be selected from among 8 different units that provide from 1 to 4 channel accesses, and which are capable of controlling from 1 to 16 tape transports. Thus, if enough data channels are available, from one to four tapes on each controller can be operational in any combination, in addition to non-magnetic-tape peripherals and the processor.

The so-called "block" operations (Search and Move) can also occur in parallel with the main computational process, once they have been initiated.

The input-output operations are of two types: character-block transfers and word-block transfers. Character operations permit either 6 or 12 bits to be transferred in parallel between core storage and the peripheral channel, while word operations allow 24-bit transfers. Each input-output transfer is initiated after a series of instructures which connect the desired channel, test for "busy" or other status conditions in the input-output equipment, and select the desired function. The input-output transfer instruction (a two-word instruction) is then issued to start the transfer.

After the starting and ending addresses for the transfer are stored in reserved locations of the processor's fast register file, the main program is released from further control of the input-output operation. For each transfer, the Communication Channel issues a data transfer request to both the input-output equipment and the priority controls of the register file. The character or word address is then delivered from the register file to the core storage address control, and the data transfer is made between storage and the data channel. The starting address is incremented and the entire transfer sequence repeated until the operation is complete, as evidenced by the starting address becoming equal to the ending address. An automatic interrupt can be specified to notify the program immediately upon completion of the transfer.

Each four-character word transferred uses one core memory cycle (1.75 microseconds) during its accession or storage, and a further three Register File cycles (also 1.75 microseconds per cycle, as the Register File is contained in core storage) are used to control the transfer operation. The central processor is allocated at least one memory cycle after each input-output word is handled, so that no more than one word can be transferred during each five core memory cycles.

During the input-output operations, the central processor is unable to gain access to the core storage module involved, or to the Register File, so computation is delayed. The probable delaying effect which input-output operations will have on processing can be calculated using the core storage utilization figures which are listed for all the standard peripheral units in Table I. Where two or more core storage modules are incorporated into a single computer system, it may be possible to reduce such processor delays by overlapping storage references.

.2 RULES

The following processes can take place simultaneously:

- One computation; plus
- One "block" operation (Search or Move); plus
- A Console key-in operation; plus
- As many buffered input-output operations* as there are buffers (up to about 50); plus
- As many non-buffered input-output operations** as there are data channels (a maximum of 8 channels); plus

---

† A 24-bit interface unit (the 3107 Special Communication Channel) can be used in place of two 3206 units.

* The present printers are always buffered; card equipment is optionally buffered.

** Paper tape, magnetic tape, and random access drum and disk operations are non-buffered; the number of such operations may also be restricted by the manner in which the controllers are connected to the data channels.

.2 RULES (Contd.)

- As many "non-supervised" peripheral operations*** as there are appropriate units.

The number of concurrent input-output operations may also be limited by the maximum throughput capacity of the computer system, which is 456,000 characters per second.

*** Magnetic tape rewinding, backspace operations, and searching for file marks, disk arm positioning and address search operations are typical "non-supervised" peripheral operations.

TABLE I: SIMULTANEOUS OPERATIONS

OPERATION	Cycle Time, msec.	Start Time			Data Transmission			Stop Time		
		Time, msec.	Core Use	Channel Use	Time, msec.	Core[b] Use	Channel Use	Time, msec.	Core Use	Channel Use
828, 838 Disk Files	---	250 av	0.0	1 msec	Var	7.8 or 12.5%	Yes	0.0	---	---
1311 Disk Storage Drive	---	170 or 270 av	0.0	1 msec	Var	9.0%	Yes	0.0	---	---
2311 Disk Storage Drive	---	97.5 av	0.0	1 msec	Var	23%	Yes	0.0	---	---
3235 Drum Storage	34.4	17.2 av	0.0	1 msec	Var	27%	Yes	0.0	---	---
861 Drum Storage	34.4	17.2 av	0.0	?	Var	(350/I)%	Yes	0.0	---	---
862 Drum Storage	17.2	8.6 av	0.0	?	Var	(350/I)%	Yes	0.0	---	---
405 Card Reader 1,200 cpm, unbuffered	50.0	18.0	0.0	Yes	32.0	17%	Yes	0.0	---	---
405 Card Reader 1,200 cpm, buffered	50.0	42.0	0.0	Yes	8.0	70%	Yes	0.0	---	---
415 Card Punch 250 cpm, unbuffered	240.0	48.0	0.0	Yes	190.0	6.2%	Yes	2.0	0.0	No
415 Card Punch 250 cpm, buffered	240.0	48.0	4.4%	2.2 msec	190.0	0.0%	No	2.0	0.0	No
523 Card Punch 100 cpm, unbuffered	600.0	84.0	0.0	Yes	514.0	2.3%	Yes	2.0	0.0	No
523 Card Punch 100 cpm, buffered	600.0	84.0	2.8%	2.2 msec	514.0	0.0%	No	2.0	0.0	No
544 Card Punch 250 cpm, unbuffered	240.0	48.0	0.0	Yes	190.0	6.1%	Yes	2.0	0.0	No
544 Card Punch 250 cpm, buffered	240.0	48.0	4.4%	2.2 msec	190.0	0.0%	No	2.0	0.0	No
3691 Paper Tape Reader 350 cps	2.9	?	0.0	Yes	2.9	<0.2%	Yes	2.0	0.0	No
3691 Paper Tape Punch 110 cps	9.0	?	0.0	Yes	9.0	<0.1%	Yes	3.0	0.0	No
3694 Paper Tape Reader 1,000 cps	1.0	?	0.0	Yes	1.0	<0.6%	Yes	0.8	0.0	No
3694 Paper Tape Punch 110 cps	9.0	?	0.0	Yes	9.0	<0.1%	Yes	3.0	0.0	No
3152 Line Printer 150 lpm	400 + 9.7LS	0	---	---	375	<0.1%	0.1 msec	25 + 9.7LS	0.0	No
1403 Model 2 Printer 600 lpm	100 + 5LS	0	---	---	80	<0.3%	0.1 msec	20 + 5LS	0.0	No
1403 Model 3 Printer 1,100 lpm	55 + 5LS	0	---	---	35	<1.0%	0.1 msec	20 + 5LS	0.0	No
501 Printer 1,000 lpm	60 + 6.7LS	0	---	---	45	<1.0%	0.1 msec	13 + 6.7LS	0.0	No
505 Printer 500 lpm	120 + 6.7LS	0	---	---	105	<0.5%	0.1 msec	13 + 6.7LS	0.0	No
601 Magnetic Tape Unit 20.8 KC	---	3.0	0.0	Yes	Var	3.4%	Yes	3.0	0.0	No
603 Magnetic Tape Unit 41.7 KC	---	2.75	0.0	Yes	Var	7.3%	Yes	2.25	0.0	No
604 Magnetic Tape Unit 60.0 KC	---	2.75	0.0	Yes	Var	10.5%	Yes	2.25	0.0	No
606 Magnetic Tape Unit 83.4 KC	---	2.75	0.0	Yes	Var	14.5%	Yes	1.75	0.0	No
607 Magnetic Tape Unit 120 KC	---	2.75	0.0	Yes	Var	21.0%	Yes	1.75	0.0	No
692 Magnetic Tape Unit 30 KC	---	?	0.0	Yes	Var	7.0%	Yes	?	0.0	No
694 Magnetic Tape Unit	---	?	0.0	Yes	Var	14.0%	Yes	?	0.0	No
696 Magnetic Tape Unit	---	?	0.0	Yes	Var	21.0%	Yes	?	0.0	No
3692 Program Controlled Input-Output Typewriter	67	0	---	---	Var	<0.01%	Yes	0	---	---
3293 Incremental Plotter	3.3 or 5.0	100	0.0	No	No	<0.05%	No	100	0.0	No

av Average time — see main report section on this device for details.
b For the word mode. If character mode is used, the core usage should be quadrupled.
I Interlace factor (can be 1, 2, 4, 8, 16, or 32).
LS Number of lines skipped between successive printed lines.
Var Data transmission time varies with record length.

SOFTWARE

The program-compatible Control Data 3100, 3200, and 3300 computer systems all utilize the same software. For a complete description, refer to the CDC 3200 Computer System Report, pages 245:151. 100 through 245:191. 600.

The Instruction List and Data Code Table for the Control Data 3100, 3200, and 3300 systems will also be found in the CDC 3200 report, on pages 245:121. 100 and 245:141. 100, respectively. (The 3100 uses subroutines to simulate the floating-point and decimal arithmetic instructions.)

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (254:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master file records is shown by solid lines. For Configuration VIIB, where all four input-output files are on magnetic tape, total times for cases using both unblocked and blocked records in the detail and report files are shown by means of solid and dashed lines, respectively. Central processor time becomes the controlling factor in Configuration VIIB when moderate activity ratios are reached.

Worksheet Data Table 1 (page 254:201.011) shows that the printer is the controlling factor on total time required over most of the detail activity range for the integrated Configuration VI. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a small fraction of the total processing time.

The master file record format is a mixture of alphameric BCD and pure binary numeric items, designed to minimize the number of time-consuming radix conversion operations required. (Even so, most of the central processor time is devoted to editing and radix conversion operations, using programmed, nonstandard subroutines.) An optimized degree of packing led to a record length of 20 words (the equivalent of 80 6-bit characters).

SORTING (254:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem according to the method explained in the Users' Guide, Paragraph 4:200.213, using a three-way merge.

MATRIX INVERSION (254:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplications ($c = c + a_i b_j$) in 36-bit precision floating point (see Paragraph 254:051.422).

GENERALIZED MATHEMATICAL PROCESSING

This problem is normally executed in floating point, which is available in the Control Data 3100 only through the use of time-consuming subroutines. The cost of such subroutines can be seen in the Matrix Inversion graph, so the Generalized Mathematical Processing Problem has not been programmed for the Control Data 3100 system.

GENERALIZED STATISTICAL PROCESSING (254:201.5)

The Generalized Statistical Processing program uses extensive fixed-point computation, which is probably the strongest feature of the Control Data 3100 system. The problem measures overall system performance on a common statistical application: the development of cross-tabulation tables, as in the analysis of the results of a survey. The problem is defined in Section 4:200.5 of the Users' Guide, and the performance of the Control Data 3100 is shown in Graph 254:201.500.

WORKSHEET DATA TABLE 1									
	Item		Configuration VI		VII B (Unblocked Files 3 & 4)		VII B (Blocked Files 3 & 4)		Reference
1 Standard File Problem A Input-Output Times	Char/block	(File 1)	960		960		960		4:200.112
	Records/block	K (File 1)	12		12		12		
	msec/block	File 1 = File 2	34		26		26		
		File 3	50		11.5		26*		
		File 4	160		12.0		38*		
	msec/switch	File 1 = File 2							
		File 3							
		File 4							
	msec/penalty	File 1 = File 2	1.45		1.45		1.45		
		File 3	0.12		0.12		0.12		
		File 4	0.18		0.18		0.18		
2 Central Processor Times	msec/block	a_1	1.60		1.60		1.60		4:200.1132
	msec/record	a_2	0.48		0.48		0.48		
	msec/detail	b_6	2.05		2.05		2.05		
	msec/work	$b_5 + b_9$	0.46		0.46		0.46		
	msec/report	$b_7 + b_8$	2.70		2.70		2.70		
3 Standard File Problem A	msec/block for C.P. and dominant column.		C.P.	I/O	C.P.	I/O	C.P.	I/O	4:200.114
		a_1	1.6		1.6		1.6		
		a_2K	5.7		5.7		5.7		
		a_3K	62.4		62.4		62.4		
F = 1.0		File 1 Master In	1.45		1.45	26	1.45	26	
		File 2 Master Out	1.45		1.45		1.45		
		File 3 Details	1.44		1.44		1.44		
		File 4 Reports	2.16	1,920	2.16	144	2.16	38	
		Total	76.20	1,920	76.20	170	76.20	64	
4 Standard File Problem A Space	Unit of measure	(24-bit word)							4:200.1151
		Std. routines	600		600		600		
		Fixed	2,000		2,000		2,000		
		3 (Blocks 1 to 23)	600		600		600		
		6 (Blocks 24 to 48)	1,000		1,000		1,000		
		Files	2,000		2,000		2,000		
		Working	600		600		600		
		Total	6,800		6,800		6,800		

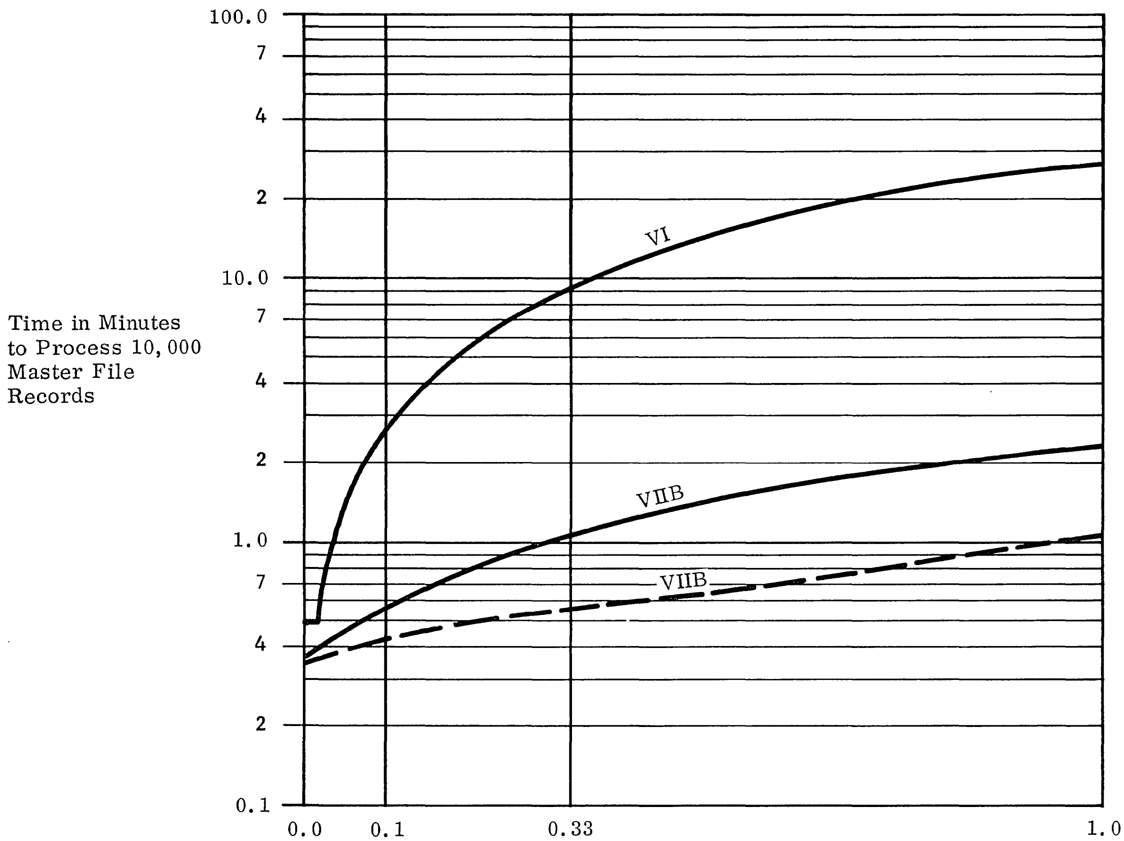
* 12 records per block.

WORKSHEET DATA TABLE 2					
	Item		Configuration VI	VIIB	Reference
7 Standard Statistical Problem A	Unit name		603 Tape	604 Tape	4:200.512
	Size of block		960 char	960 char	
	Records/block	B	15	15	
	msec/block	T_1	34.0	26.0	
	msec penalty	T_3	0.35	0.35	
	C.P. msec/block	T_5	0.01	0.01	
	C.P. msec/record	T_6	0.01	0.01	
	C.P. msec/table	T_7	0.055	0.055	

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes
Master file: . . . . 108 characters (packed into 20 CDC 3100 words).
Detail file: . . . . 1 card.
Report file: . . . . 1 line.
.112 Computation: . . . . standard.
.113 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.113
.114 Graph: . . . . see graph below.
.115 Storage space required
Configuration VI: . . . 6,800 words.
Configuration VII B (Unblocked Files 3 & 4): . . . . 6,800 words.
Configuration VII B (Blocked Files 3 & 4): . . . . 6,800 words.



Activity Factor
Average Number of Detail Records Per Master Record

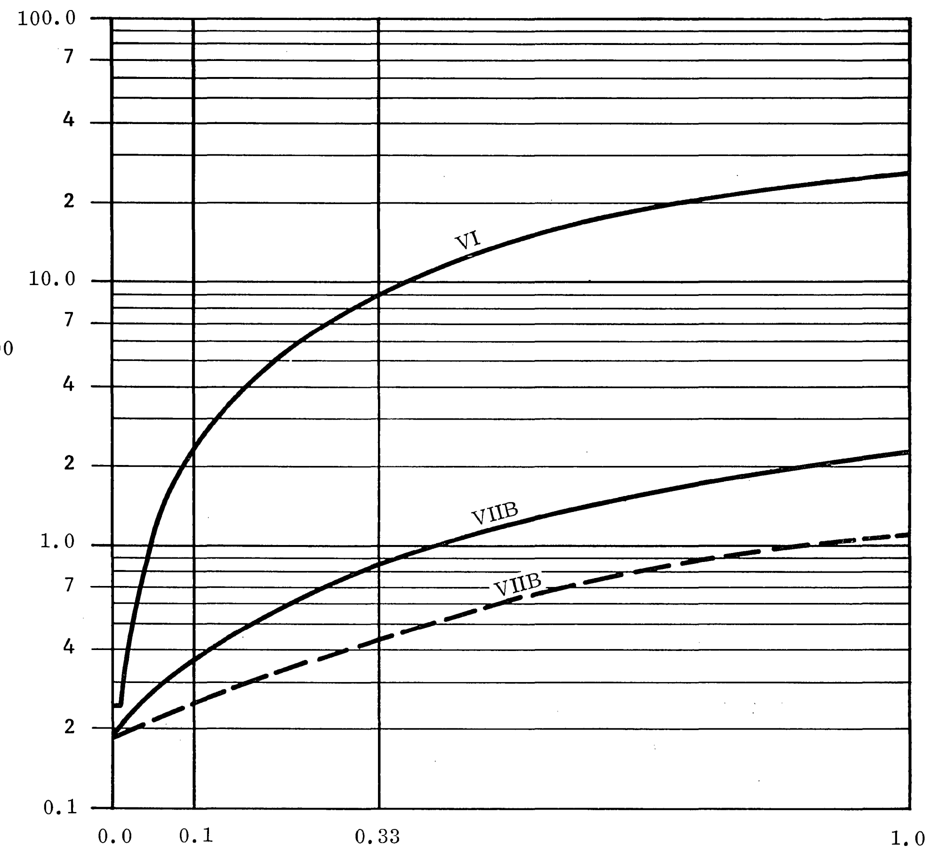
NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 254:031.

.12 Standard File Problem B

.121 Record sizes
Master file:. . . . . . . 54 characters.
Detail file: . . . . 1 card.
Report file: . . . . . . 1 line.

.122 Computation: . . . . standard.
.123 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . see graph below.

Time in Minutes to Process 10,000 Master File Records



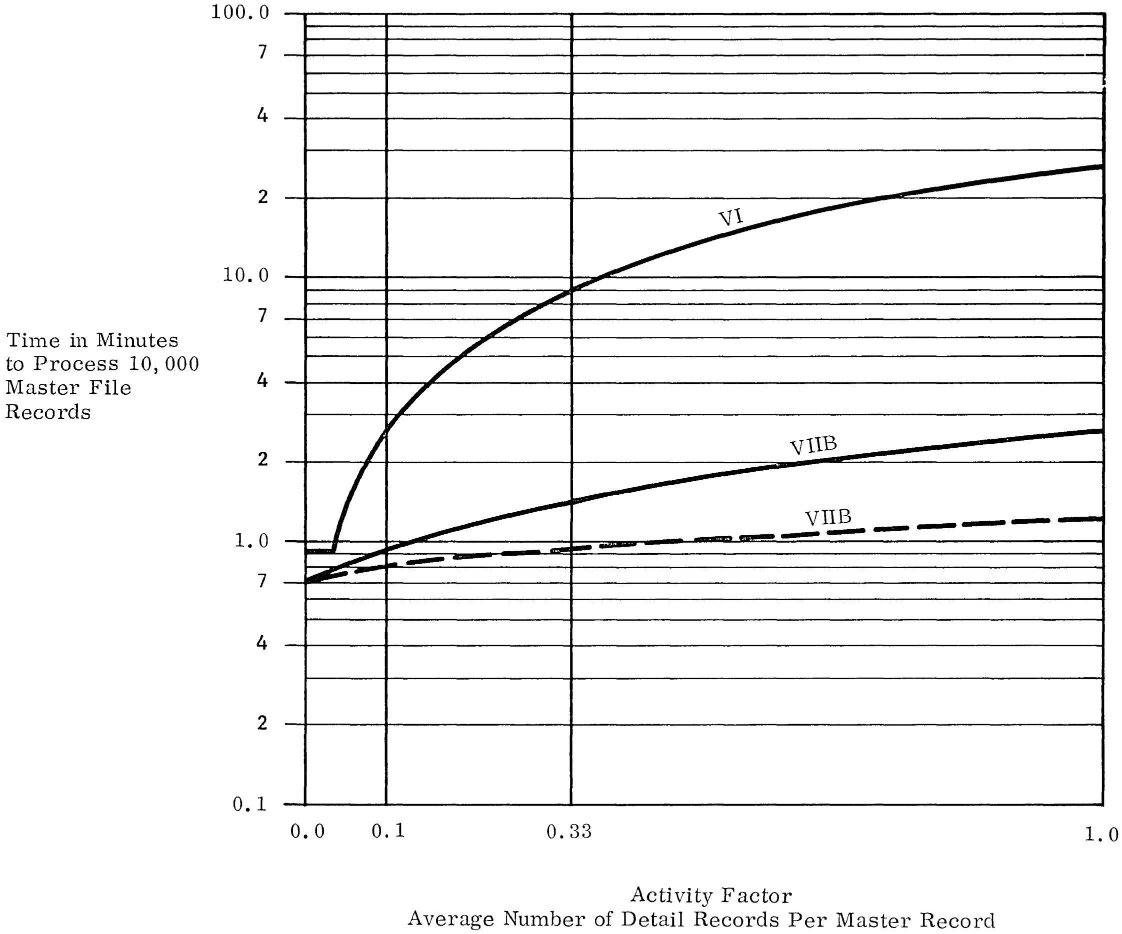
Activity Factor
Average Number of Detail Records Per Master Record

NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 254:031.

.13 Standard File Problem C

.131 Record sizes
Master file: . . . . 216 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.132 Computation: . . . . standard.
.133 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.
.134 Graph: . . . . see graph below.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numberals denote standard system configurations shown in Section 254:031.

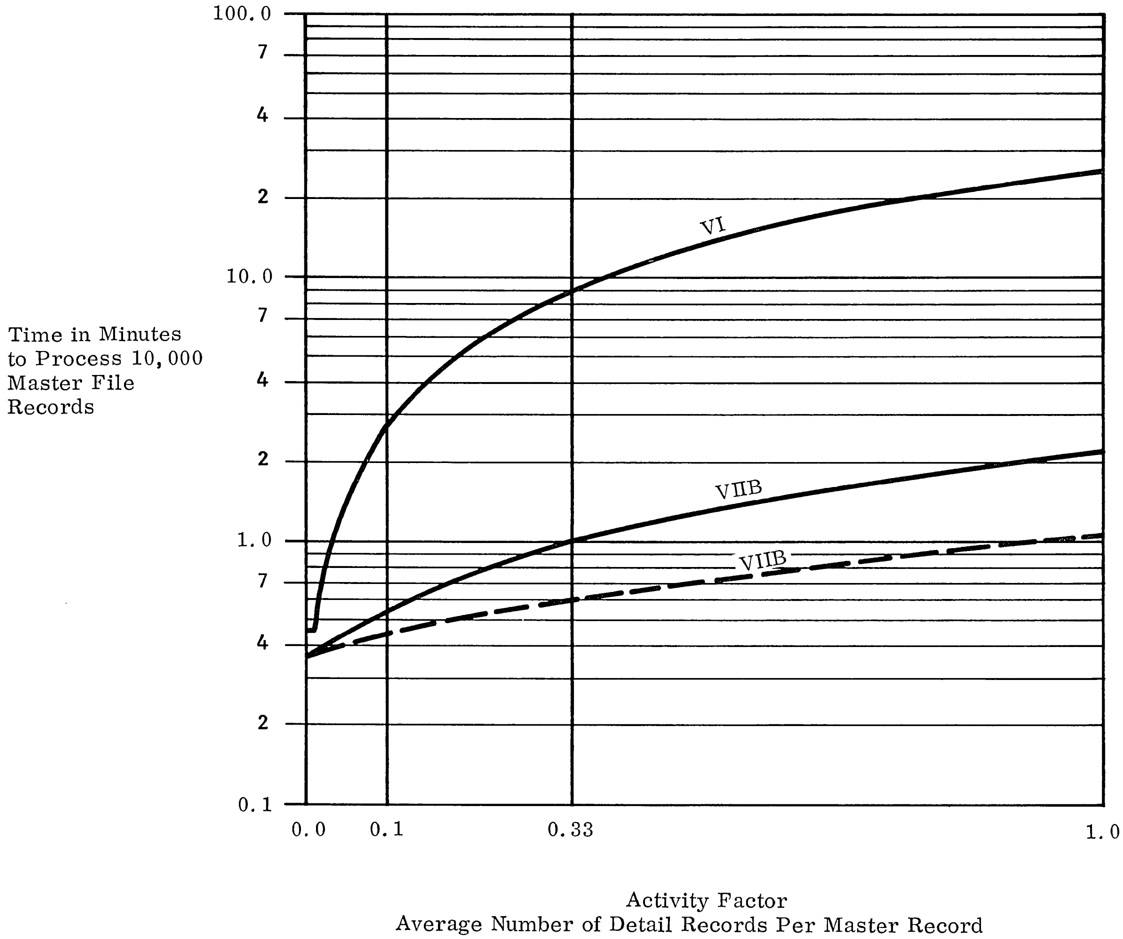
.14 Standard File Problem D

.141 Record sizes
- Master file: . . . . 108 characters.
- Detail file: . . . . 1 card.
- Report file: . . . . 1 line.

.142 Computation: . . . . trebled.

.143 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide. 4:200.14.

.144 Graph: . . . . see graph below.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 254:031.

AUERBACH

.2 SORTING

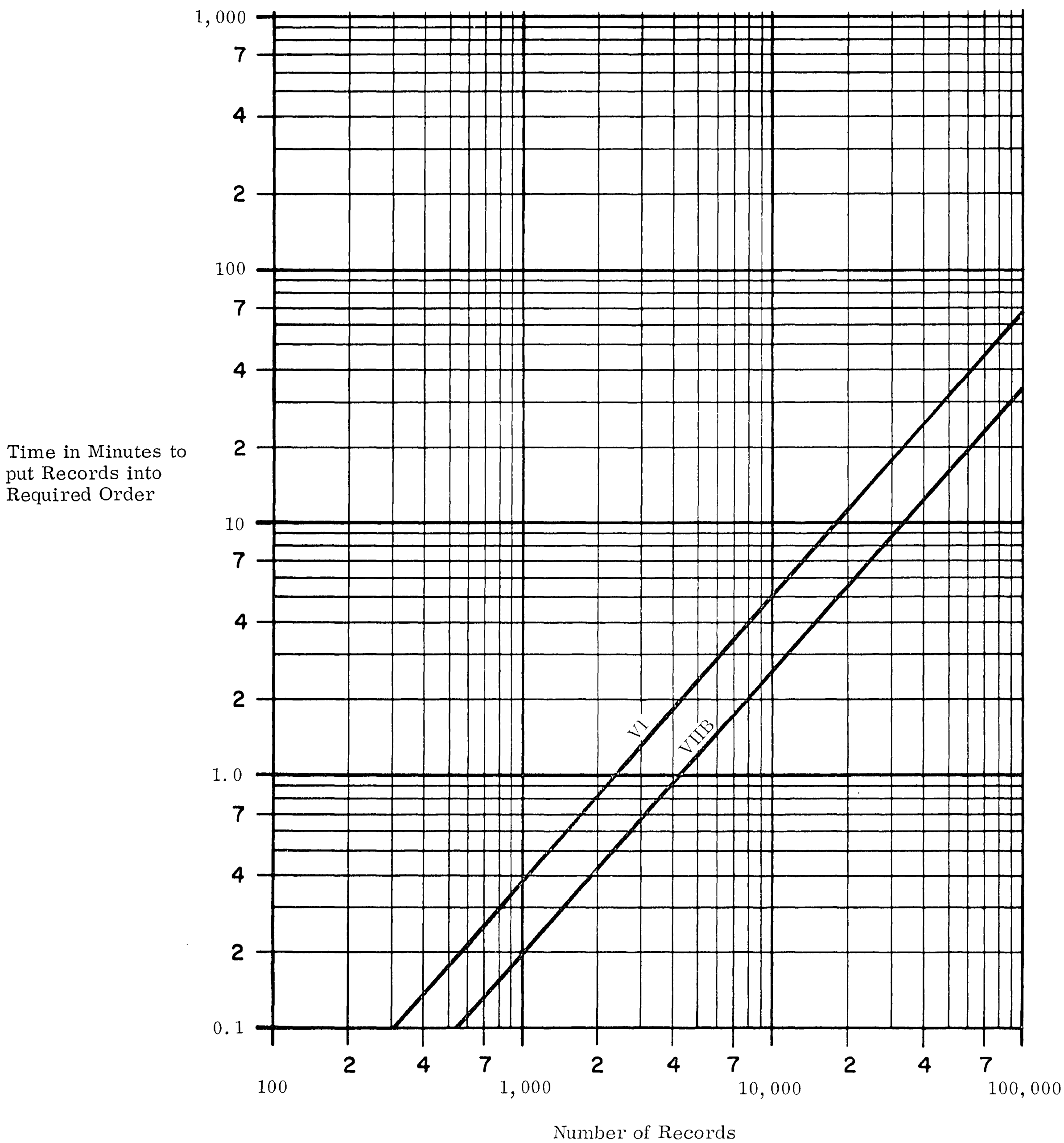
.21 Standard Problem Estimates

.211 Record size: . . . . 80 characters.

.212 Key size: . . . . 8 characters.

.213 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . see graph below.



NOTE: Roman numerals denote standard system configurations shown in Section 254:031.

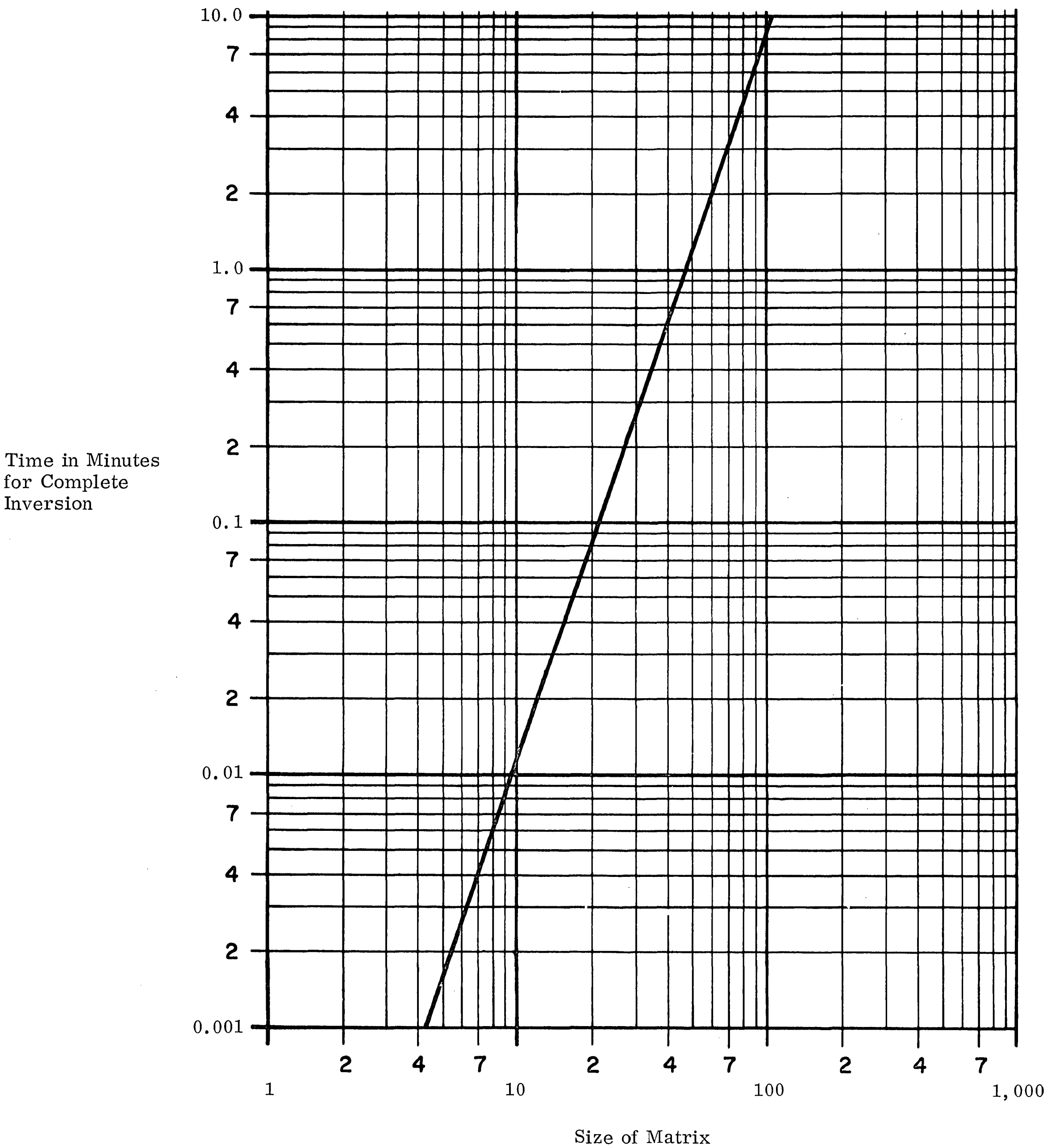
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.312; floating-point arithmetic performed by subroutines.

.313 Graph: . . . . see graph below.



.5 GENERALIZED STATISTICAL PROCESSING

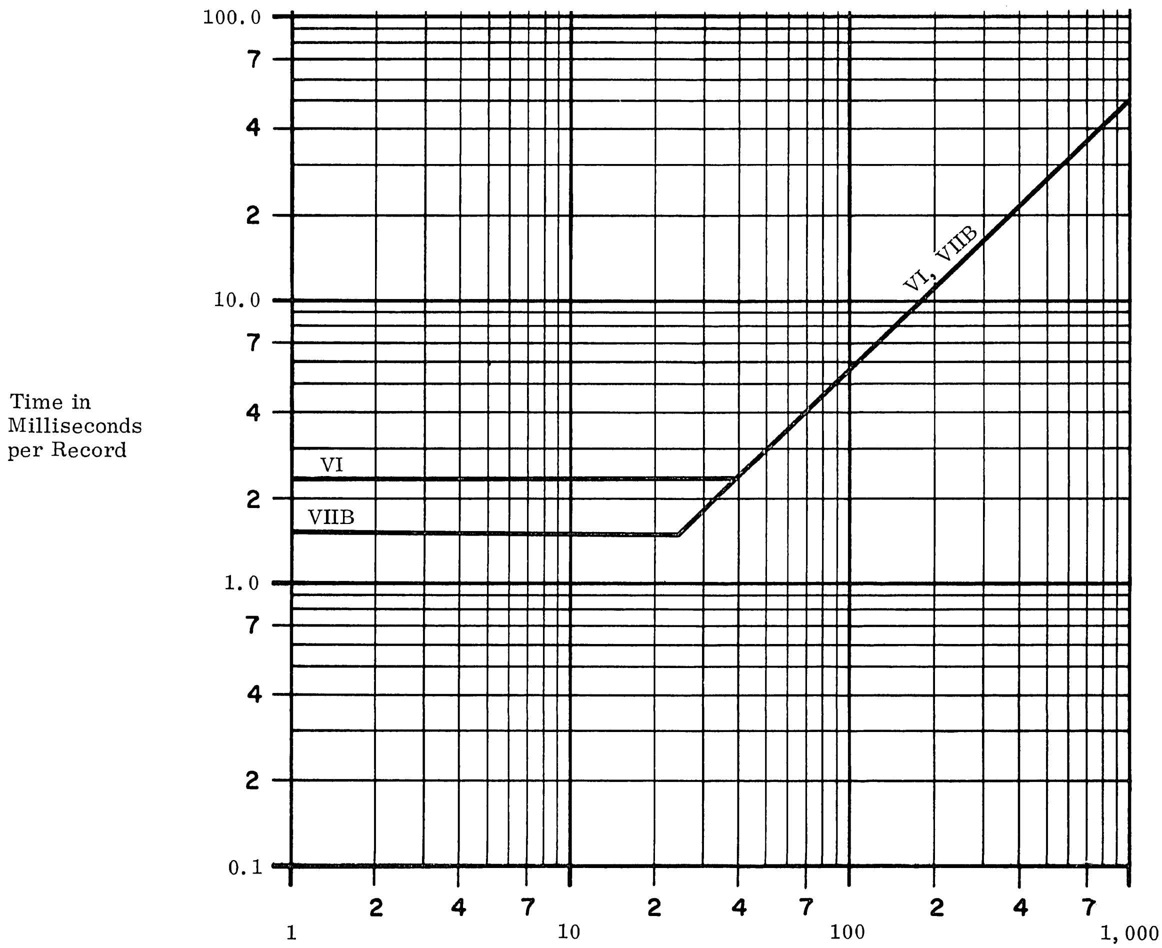
.51 Standard Statistical Problem A Estimates

.511 Record size: . . . . thirty 2-digit integral numbers.

.512 Computation: . . . . augment T elements in cross-tabulation tables.

.513 Timing basis: . . . . . . using estimating procedures outlined in Users' Guide, 4:200.513.

.514 Graph: . . . . see below.



T, Number of Augmented Elements

Roman numerals denote standard configurations.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSOR	3104	COMPUTER: 6, 24, and 48-bit modes, three index registers, indirect addressing. Includes console, communication channel, 4,096 words of storage, and control for referencing up to 32,768 words of storage and up to four 3106 communication channels.	2,700	173.00	95,000
DATA CHANNELS	3106	COMMUNICATION CHANNEL: bi-directional, buffered, 12-bit data exchange. Permits attachment of one to eight 3100, 3200, 3400, or 3600 peripheral controllers to a 3100 system.	120	35.00	5,000
	3107	COMMUNICATIONS CHANNEL: bi-directional, buffered, 24-bit data exchange. Includes 12 to 24-bit assembly/disassembly, permits attachment of one to eight peripheral controllers to a 3100 system.	200	50.00	8,500
INTERNAL STORAGE	3108	STORAGE MODULE: 4,096 words or 16,384 characters of magnetic core storage.	700	102.00	30,000
	3109	STORAGE MODULE: 8,192 words or 32,768 characters of magnetic core storage.	810	127.00	42,000
	3103	STORAGE MODULE: 16,384 words or 65,536 characters of magnetic core storage. Each word or character is parity checked. One read/write control, accessible from two processors or special devices.	1,800	148.00	80,000
INPUT-OUTPUT	3192	ON-LINE MONITOR TYPEWRITER: direct connection into 3104 computer.	240	85.00	9,000

NOTE: All Control Data 3000 Series computers use the same peripheral units. These peripheral units are described in the CDC 3200 Computer System Report, and their prices are listed in the Price Data section beginning on page 245:221.101.

CDC 3300

Control Data Corporation

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CONTENTS

* Refer to indicated section of the CDC 3200 Computer System Report.

INTRODUCTION

The Control Data 3300 computer system was announced in the summer of 1964 as a faster version of the CDC 3200 system. First deliveries of the new system probably will not be made before the Spring of 1966; the 3300 was announced primarily to assure users of the CDC 3100 and 3200 computer systems that they will be able to move up to a larger, faster computer without reprogramming and conversion problems. At present, this assurance is probably the most important single characteristic of the CDC 3300, although as delivery approaches, interest may well focus upon the matured software systems which users will be able to transfer from the CDC 3200 to the 3300 system. These software systems will include FORTRAN and COBOL compilers, a report generator, an operating system (SCOPE), a linear programming package, and a PERT program.

The CDC 3300 is a scientific computer system with large-scale performance capabilities (as judged against 1964 equipment). The cycle time of its core storage modules is 800 nanoseconds, and that of its Register File (used for various control purposes) is 300 nanoseconds. Its instruction times are correspondingly fast. Fixed-point, 24-bit addition takes 1.6 microseconds; floating-point, 36-bit precision addition takes 7 microseconds; and decimal addition takes 7.6 microseconds for 12-digit operands. The binary multiplication times are 6 microseconds and 11 microseconds for fixed-point and floating-point operations, respectively. There are no hardware facilities for decimal multiplication or division.

The off-line search facilities and the interrupt system used in the Control Data 3200 computer system are included in the 3300 system, without alteration.

The input-output throughput capacity has been increased by 60% over the CDC 3200's capacity, to a maximum of 4,333,333 characters per second. The number of data channels that can be connected remains at eight, so the number of concurrent operations that can be simultaneously supervised by the central processor (also eight) is unchanged.

The maximum amount of addressable core storage has been increased fourfold from its capacity of 32,768 24-bit words in the CDC 3200 system, to 131,072 words. It is not yet known whether the whole of this storage will be character-addressable, as well as word-addressable.

A multiprogramming facility will be included in the Control Data 3300 repertoire. Presently-announced features (dynamic storage protection and automatic program relocation), while useful in themselves, will not help to reduce the time involved in switching from one program to another. Where this switching is at all frequent, a considerable executive program overhead may be incurred in interchanging and protecting the contents of the index registers and parts of the Register File.

The CDC 3300, like the CDC 3200 system, is designed to enable multi-computer installations to be simply organized. All 16,384-word core storage modules are independent and permit access by either of two processors. Most of the peripheral units can be supplied with dual-channel controllers and switched from one processor to another under program control.

The peripheral units available with the Control Data 3300 system are exactly the same as those available for the Control Data 3100 and 3200 systems. They are described in detail in Computer System Report No. 245, on the Control Data 3200. Particularly interesting peripheral units include IBM System/360-compatible magnetic tape units, and the Model 861 and 862 Drum Storage units which can transfer data at up to 2,000,000 characters per second.

The software for the Control Data 3300 will be taken directly from the Control Data 3200 system, except for some changes to the SCOPE Operating System to adapt it for multiprogrammed operation. No alterations in any compilers, assemblers, or utility programs are expected to be necessary.

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word:	24 bits	basic addressable unit (data or instruction).
Character:	6 bits	addressable data unit.
Block:	1 to N characters or 1 to N words	Search, Move, and Input-output instructions.

.2 INFORMATION FORMAT

Type of Information	Representation
Operand:	24- or 48-bit fixed point word. 48-bit floating point word. 6-bit character. 4-bit BCD character.
Instruction:	1 or 2 words.
Field:	1 to 13 BCD characters.

SYSTEM CONFIGURATION

GENERAL

Every Control Data 3300 computer system includes the following units:

- A 3300 General Processor.
- A 0.8-microsecond Core Storage Unit ranging from 8,192 to 32,768 words (32,768 to 131,072 characters) in capacity.
- A desk console with detachable keyboard and an adjacent I/O typewriter station.
- A Power Converter and Control Unit.

Two 3306 Data Channels are included in the basic system. Up to six more can be added, so that a fully-extended Control Data 3300 computer system will have eight data channels. Eight peripheral units or controllers can be connected to each data channel.

The data channels used in all of the Control Data 3000 Series computers present a common interface with peripheral units. As a result of this, any of the 3000 Series peripheral units can be connected through a 3306 Data Channel to a Control Data 3300 computer. The available peripheral units are described in the Control Data 3200 Computer System Report. Details of the loadings these units place on a Control Data 3300 computer system are described in the Simultaneous Operations section of this report, starting on page 255:111.100.

Some peripheral units or controllers can be connected to more than one data channel. This facility may be used either to allow two concurrent data transmissions to take place, or to allow the peripheral unit to be switched between two computer systems. A bank of magnetic tape units connected to a dual-channel controller is a case where multiple data transmissions would be the normal reason for having the two data channels; while a printer connected to two different computer systems by way of a dual-channel controller could be used by either system, as the situation in the computer room demands.

The core storage modules can similarly be connected to, and accessed by, two computers. Each 8,192-word module is independent and permits dual access by a second processor or special device.

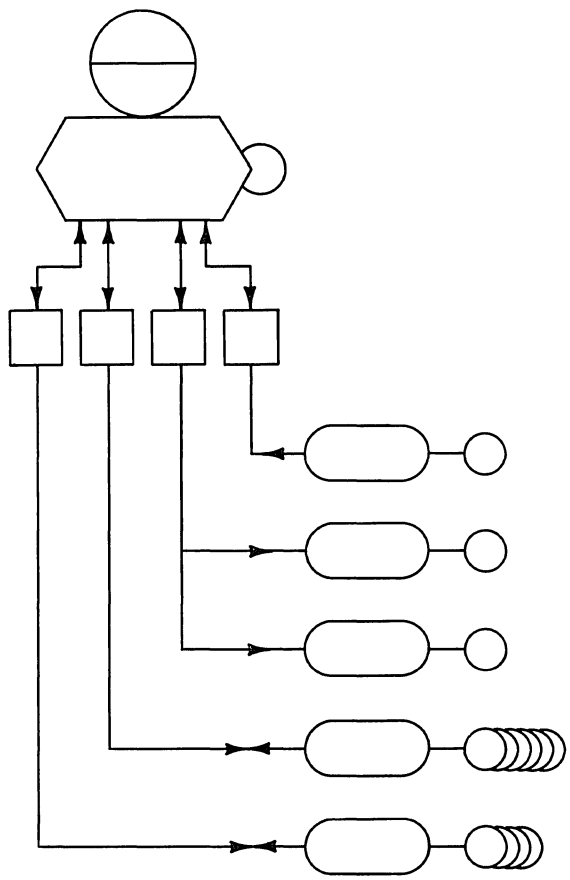
SELECTION OF REPRESENTATIVE CONFIGURATIONS

The Control Data 3300 computer system is shown in the following Standard System Configurations, as defined in the Users' Guide, page 4:030.100:

- Configuration VIIA; 10-Tape General Integrated Configuration.
- Configuration VIIB; 10-Tape General Paired Configuration, using a Control Data 160 Computer System as the satellite system.

.1 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . core storage is 33% larger.
3 less index registers provided.
card reader is 140% faster.
card punch is 150% faster.

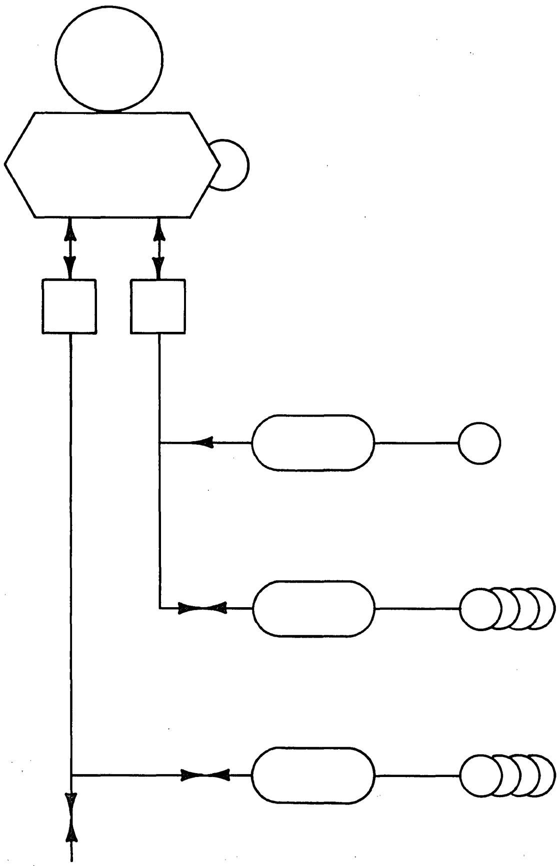


Equipment	Rental
32,768 words of Core Storage	INA
3300 General Processor Console with Monitor Typewriter	INA
3306 Data Channels (4)	INA
405 Card Reader (1,200 cpm)	$ 400
3248 Control	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
604 60KC Magnetic Tapes (6)	3,600
3229 Controller	600
604 60KC Magnetic Tapes (4)	2,400
3228 Controller	425
TOTAL RENTAL:	$ INA

INA: Prices not announced to date.

.2 10-TAPE GENERAL SYSTEM (PAIRED): CONFIGURATION VIIB*

Deviations from Standard Configuration: . . . . 3 less index registers.
direct connection to satellite system.
card reader is 1100% faster.



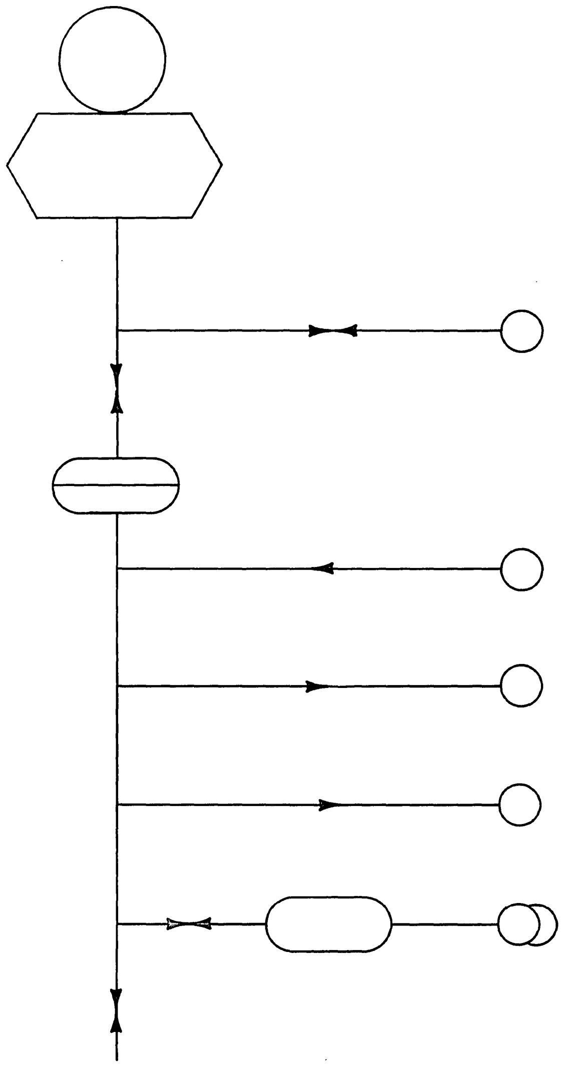
To Satellite
160 System
(at right)

Equipment	Rental
16,384 words of Core Storage	INA
3300 General Processor Console with Monitor Typewriter 3206 Data Channels (2)	INA
405 Card Reader (1,200 cpm) 3248 Controller	$ 400 100
604 60KC Magnetic Tape Units (4) 3228 Controller	2,400 425
604 60KC Magnetic Tape Units (4) 3228 Controller	2,400 425
TOTAL ON-LINE EQUIPMENT:	$ INA
TOTAL SATELLITE EQUIPMENT:	$5,165
TOTAL RENTAL:	$ INA

INA: Prices not announced to date.

SATELLITE EQUIPMENT (CDC 160)

Deviations from Standard Configuration: . . . .
direct connection to main system.
core storage is 100% larger.
multiply/divide is included.
paper tape equipment is included.
card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 30% slower.



Equipment	Rental
4,096 12-bit words of Core Storage 160 Processor Console with Monitor Typewriter Paper Tape Reader (350 cps) Paper Tape Punch (110 cps)	$1,500
3681 Data Channel Converter	275
3682 Satellite Coupler	175
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
601 21KC Magnetic Tapes (2)	500
3127 Controller	320
TOTAL SATELLITE EQUIPMENT:	$5,165

INTERNAL STORAGE: CORE STORAGE

.1 GENERAL

.11 Identity: . . . . 3300 General Processor, containing 8K words.
3309 Storage Module (8K).
3303 Storage Module (16K).

.12 Basic Use: . . . . working storage.
random access storage.
intercommunication with other computer systems.

.13 Description

A Control Data 3300 computer system must contain 8, 192 24-bit word locations of core storage, and can optionally be connected to a 3309 Storage Module, which is a second, independent 8, 192-word module, for a total of 16, 384 words. Additionally, the 3300 computer system can be connected to up to seven 3303 Storage Modules, each of 16, 384 words, for a total potential capacity of 131, 072 words, or 524, 288 characters, of core storage.

The 3309 and 3303 Storage Modules differ in their function as well as in their size. The 3309 is connected directly to a single 3300 computer system, while each of the 3303 Storage Modules can be connected to two different computer systems. Control Data expects the 3303 Modules to be used for random access storage and for inter-computer communication, rather than as regular working storage.

All the core storage units have cycle times of 0.8 microseconds and access times of 0.4 microseconds. Each module is independent, and significant speed increases can be achieved by placing the instructions in one bank and the operands in another, or by separating the input-output areas from the computational areas in a program.

.14 Availability: . . . . ?

.15 First Delivery: . . . . . Spring, 1966.

CENTRAL PROCESSOR

.1 GENERAL

.11 Identity: . . . . 3300 General Processor.

.12 Description

Preliminary details indicate that the CDC 3300 General Processor will be a faster version of the CDC 3215 General Processor, with a few additional instructions introduced to simplify multiprogramming, and the ability to address up to 131,072 words of storage. The reader is referred to the description of the 3215 General Processor on page 245:051.100 (in the CDC 3200 Computer System Report) for details of the facilities of the 3300 Processor.

The faster operation of the CDC 3300 results from its faster core storage cycle time (0.8 versus 1.25 microseconds), a reduction in the proportion of the core storage cycle which is needed simply to access data (50% of the complete cycle, versus 60% in the CDC 3200), and a reduction in the cycle time of the 64-word Register File (300 versus 500 nanoseconds). The Register File itself will cycle independently of the core storage; this will help by reducing the load placed on the core storage by input-output operations rather than by speeding up the computational operations.

The multiprogramming facilities announced to date consist of dynamic storage protection and automatic program relocation. Only one set of three index registers and one Register File are provided, so that switching from one program to another will usually entail unloading and restoring most, if not all, of these registers.

Only preliminary information about the performance of the Control Data 3300 computer system is available to date. This information has been used to derive instruction times and subroutine times, which differ from those reported for the Control Data 3200 computer system. These times are reported below and in Table I. For the rest of the details regarding the Control Data 3300 Processor and its facilities, reference should be made to the description of the CDC 3215 General Processor on page 245:051.100.

.13 First Delivery: . . . . . Spring, 1966.

.14 Availability: . . . . ?

.2 PROCESSING FACILITIES

See Paragraph 245:051.2 in the CDC 3200 report.

.3 SEQUENCE CONTROL FEATURES

See Paragraph 245:051.3 in the CDC 3200 report.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

		Binary (24 bits)	BCD (12 char)
.411	Fixed point —		
	Add-subtract:	1.8	7.4
	Multiply:	5.0 to 7.0	not available.
	Divide:	7.3	not available.
.412	Floating point —		
	Add-subtract:	6.4 to 7.7	
	Multiply:	9.0 to 11.5	
	Divide:	13.0	
.413	Additional allowance for —		
	Indexing:	0.24	
	Indirect addressing:	0.8	
	Re-complementing:	0.0	
.414	Control —		
	Compare:	1.2	
	Branch:	0.8	
	Compare and branch:	1.2	
.415	Counter control —		
	Step:	0.8	
	Step and test:	1.2	
	Test:	1.2	
.416	Edit:	not available.	
.417	Convert:	see Table I.	
.418	Shift:	0.8 to 2.4	

.42 Processor Performance in Microseconds

		Fixed point (24 bits)	BCD (12 char)	Floating point (48 bits)
.421	For random addresses —			
	c = a + b:	4.8	17.5	11.9
	b = a + b:	4.0	17.5	11.9
	Sum N items:	1.6N	7.4N	7.0N
	c = ab:	9.2	not available	15.0
	c = a/b:	11.2	not available	15.0
.422	For arrays of data —			
	$c_i = a_i + b_j$:	7.6	22.5	14.5
	$b_j = a_i + b_j$:	6.8	23.7	14.5
	Sum N items:	3.1N	8.8	8.5
	$c = c + a_i b_j$:	13.4	—	—

.423 Branch based on comparison —
Numeric data: 10.0
Alphabetic data: 10.0
.424 Switching —
Unchecked: 3.45
Checked: 5.8
List search: . . . . . . 9.4 + 2.7N
.425 Format control, per character —
Unpack: . . . . 76.
Compose: . . . . 76.
.426 Table look-up, per N comparisons —
For a match: . . . . . . 2.7 + 2.7N
For least or greatest: 2.7 + 2.7N
For interpolation point: . . . . 2.7 + 2.7N
.427 Bit indicators —
Set bit in pattern: . . . 4.8
Test bit in pattern: . . 3.6
.428 Moving, per N words: . 2.1 + 2.9N (345,000 24-bit words/sec).

.5 ERRORS, CHECKS, AND ACTION

See Paragraph 245:051.5 in the CDC 3200 report.

TABLE I: CONVERSION TIMES FOR STANDARD SUBROUTINES

ORIGINAL OPERAND		MICROSECONDS REQUIRED FOR CONVERSION TO:				
Type	Magnitude	Internal BCD (1)	Fixed Point Binary (2)	Floating Point Binary (3)	Column BCD (4)	Row BCD (5)
Internal BCD	$<10^7$	-	9/digit	9/digit + 12/operand	4,000/card	20,000/card
Internal BCD	$\geq 10^7$	-	15/digit	15/digit + 12/operand	4,000/card	20,000/card
Fixed Point Binary	$<10^7$	14/digit	-	12/operand	14/digit + 4,000/card	14/digit + 20,000/card
Fixed Point Binary	$\geq 10^7$	28/digit	-	12/operand	28/digit + 4,000/card	28/digit + 20,000/card
Floating Point Binary	$< 10^7$	14/digit + 18/operand	18/operand	-	14/digit + 18/operand + 4,000/card	14/digit + 18/operand + 20,000/card
Floating Point Binary	$\geq 10^7$	28/digit + 18/operand	18/operand	-	28/digit + 18/operand + 4,000/card	28/digit + 18/operand + 20,000/card

(1) Internal BCD is used in decimal arithmetic, for card reader input, and for printer output.
(2) Fixed Point Binary is used for 24 or 48-bit binary arithmetic.
(3) Floating Point Binary is used for all floating point operations.
(4) Column BCD is used for output via buffered card punch equipment.
(5) Row BCD is used for output via unbuffered card punch equipment.

Note: "digit" refers to decimal digits in all of the above times.

CONSOLE

.1 GENERAL

.11 Identity: . . . . 3301 Desk Console.

.12 Associated Unit: . . . Input-Output Typewriter is included with the 3301.

.13 Description

Details of the 3301 Desk Console have not been completely specified, but in general it will be similar to the 3201 Desk Console used with CDC 3200 computer systems, modified as necessary for the additional storage capabilities of the newer system and for its storage protection and automatic relocation features. The following description (taken from the Console section of the CDC 3200 Computer System Report) describes the 3201 Desk Console, and contains the best currently available information about the 3301.

The Desk Console includes a movable input keyboard, which can either be operated at the console or removed and carried to a suitable nearby location. An input-output typewriter is also incorporated in the console design. Both the keyboard and the typewriter have direct access to the computational module, and do not use the regular data channels.

Octal or decimal displays are used to display the contents of the seven operational registers. The operator sitting at the console has a good view of these displays, and of the equipment itself.

The "external" status indicators display the existing condition of the input-output channels, while six columns of "internal" condition indicators provide the following information:

- Storage Active — for addressing purposes, the four possible 8,192-word sections of storage are designated by digits 0-3. Whenever one of these storage sections becomes active, the corresponding indicator light is lit.
- Conditions — a Standby light indicates that the main power switch is on, but that individual supplies are still off; an Interrupt Disabled light is on whenever the interrupt system is disabled by the program.
- Cycle — four cycles are represented: Read Next Instruction, Read Address, Read Operand, and Store Operand. These indicators are lit whenever the cycles are in progress.
- Faults — these lights represent four arithmetic faults: Arithmetic Overflow, Divide, Exponent Overflow, and Decimal (BCD).
- Temperature Warning and Temperature High— up to four cabinet sections are represented.

The console switches are divided into two groups — those used for normal operations of the system and those used primarily for maintenance purposes. Operational switches are included on the main console and on an entry keyboard. The keyboard replaces the Set and Clear pushbuttons that are found on most Control Data computers for the manual entry of information.

The main console switches provide for such operating controls as breakpoint/run mode selection, automatic load/dump initiation for a designated device, selective jump instruction keys, manual interrupt, and master clear buttons. The keyboard switches provide for start and stop controls, register display control, and the manual entry of information into core storage or a designated register.

INPUT–OUTPUT AND RANDOM ACCESS PERIPHERAL UNITS

All of the Control Data 3000 Series computers, including the CDC 3300 system, use the same input-output units, the same random access storage units, and the same controllers. The program-compatible Control Data 3100, 3200, and 3300 computers also use the same supporting routines, although naturally both the timing of the routines and the load placed on the core storage modules by the input-output operations will vary between the different computer systems. In order to place proper emphasis upon the family similarities and differences, our coverage of the Control Data 3000 Series peripheral units as used in the CDC 3300 system is organized as follows:

The Control Data 3200 Computer System Report includes:

- The DESCRIPTION of each unit and controller (see pages 245:042. 100 through 245:102. 100).
- The PRICE of each unit and controller (see page 245:221. 101).
- The details of the SUPPORT PROGRAMS (if any) for each unit.

This Computer System Report includes:

- The LOADING that each peripheral unit imposes on the 3300 core storage modules (see the Simultaneous Operations section, page 255:111. 101).
- The TIMING details for code and radix conversions used in connection with peripheral operations (see the Central Processor section, page 255:051. 423).

SIMULTANEOUS OPERATIONS

1. GENERAL

The Control Data 3300 system allows for the connection of up to eight input-output data channels. Each data channel is serviced by a bi-directional, 12-bit parallel interface unit called the 3306 Standard Communications Channel†. Up to eight different peripheral equipment controllers can be connected to one 3306. These facilities make it possible for up to eight input-output operations on any of 64 different controllers to proceed simultaneously with computation.

A choice of single- and dual-channel controllers is available for the card and printer equipment. Full line buffers are included with each of the printer controllers, but card buffers are optional depending upon the choice of card reader or card punch controller. The magnetic tape units, paper tape units, and typewriter simply have 12-bit interfaces.

Magnetic tape controllers can be selected from among 8 different units that provide from 1 to 4 channel accesses, and which are capable of controlling from 1 to 16 tape transports. Thus, if enough data channels are available, from one to four tapes on each controller can be operational in any combination, in addition to non-magnetic-tape peripherals and the processor.

The so-called "block" operations (Search and Move) can also occur in parallel with the main computational process, once they have been initiated. The Search instruction initiates a search through a block of character storage addresses looking for equality or inequality with a character contained in the instruction word. The Move order is used to move a block of n characters from one area of storage to another. It should be noted, however, that no real advantage results from this feature if the program requires access to the same storage module as that involved in the block operation. As a result, careful program design is required to realize the potential benefits of these overlapped internal operations.

The input-output operations are of two types: character-block transfers and word-block transfers. Character operations permit either 6 or 12 bits to be transferred in parallel between core storage and the peripheral channel, while word operations allow 24-bit transfers. Each input-output transfer is initiated after a series of instructions which connect the desired channel, test for "busy" or other status conditions in the input-output equipment, and select the desired function. The input-output transfer instruction (a two-word instruction) is then issued to start the transfer.

† A 24-bit interface unit (the 3307 Special Communication Channel) can be used in place of two 3206 units.

After the starting and ending addresses for the transfer are stored in reserved locations of the processor's fast register file, the main program is released from further control of the input-output operation. For each transfer, the Communication Channel issues a data transfer request to both the input-output equipment and the priority controls of the register file. The character or word address is then delivered from the register file to the core storage address control, and the data transfer is made between storage and the data channel. The starting address is incremented and the entire transfer sequence repeated until the operation is complete, as evidenced by the starting address becoming equal to the ending address. An automatic interrupt can be specified to notify the program immediately upon completion of the transfer.

Each four-character word transferred uses one core memory cycle (0.8 microseconds) during its accession or storage, and a further three Register File cycles (0.3 microseconds) are used to control the transfer operation. During these operations the central processor is unable to gain access to the core storage module involved, or to the Register File, so computation is delayed. The probable delaying effect which input-output operations will have on processing can be calculated using the core storage utilization figures which are listed for all the standard peripheral units in Table I. Where two or more core storage modules are incorporated into a single computer system, it may be possible to reduce such processor delays by overlapping storage references.

.2 RULES

The following processes can take place simultaneously:

- One computation; plus
- One "block" operation (Search or Move); plus
- A Console key-in operation; plus
- As many buffered input-output operations* as there are buffers (up to about 50); plus
- As many non-buffered input-output operations** as there are data channels (a maximum of 8 channels); plus

* The present printers are always buffered; card equipment is optionally buffered.

** Paper tape, magnetic tape, and random access drum and disk operations are non-buffered; the number of such operations may also be restricted by the manner in which the controllers are connected to the data channels.

- As many "non-supervised" peripheral operations*** as there are appropriate units.

*** Magnetic tape rewinding, backspace operations, and searching for file marks, disk arm positioning and address search operations are typical "non-supervised" peripheral operations.

The number of concurrent input-output operations may also be limited by the maximum throughput capacity of the computer system, which is 4,444,444 characters per second.

TABLE I: SIMULTANEOUS OPERATIONS

DEVICE	Cycle Time,	Start Time			Data Transmission			Stop Time		
	msec.	Time, msec.	Core Use	Channel Use	Time, msec.	Core[b] Use	Channel Use	Time, msec.	Core Use	Channel Use
828, 838 Disk Files	---	250 av	0.0	1 msec	Var	1.4 or 2.2%	Yes	0.0	---	---
1311 Disk Storage Drive	---	170 or 270 av	0.0	1 msec	Var	1.6%	Yes	0.0	---	---
2311 Disk Storage Drive	---	97.5 av	0.0	1 msec	Var	4.1%	Yes	0.0	---	---
3235 Drum Storage	34.4	17.2 av	0.0	1 msec	Var	3.2%	Yes	0.0	---	---
861 Drum Storage	34.4	17.2 av	0.0	?	Var	(41/I)%	Yes	0.0	---	---
862 Drum Storage	17.2	8.6 av	0.0	?	Var	(41/I)%	Yes	0.0	---	---
405 Card Reader 1,200 cpm, unbuffered	50.0	18.0	0.0	Yes	32.0	1.9%	Yes	0.0	---	---
405 Card Reader 1,200 cpm, buffered	50.0	42.0	0.0	Yes	8.0	8.0%	Yes	0.0	---	---
415 Card Punch 250 cpm, unbuffered	240.0	48.0	0.0	Yes	190.0	0.7%	Yes	2.0	0.0	No
415 Card Punch 250 cpm, buffered	240.0	48.0	4.4%	2.2 msec	190.0	0.0%	No	2.0	0.0	No
523 Card Punch 100 cpm, unbuffered	600.0	84.0	0.0	Yes	514.0	0.3%	Yes	2.0	0.0	No
523 Card Punch 100 cpm, buffered	600.0	84.0	2.8%	2.2 msec	514.0	0.0%	No	2.0	0.0	No
544 Card Punch 250 cpm, unbuffered	240.0	48.0	0.0	Yes	190.0	0.7%	Yes	2.0	0.0	No
544 Card Punch 250 cpm, buffered	240.0	48.0	4.4%	2.2 msec	190.0	0.0%	No	2.0	0.0	No
3691 Paper Tape Reader 350 cps	2.9	?	0.0	Yes	2.9	<0.03%	Yes	2.0	0	No
3691 Paper Tape Punch 110 cps	9.0	?	0.0	Yes	9.0	<0.02	Yes	3.0	0.0	No
3694 Paper Tape Reader 1,000 cps	1.0	?	0.0	Yes	1.0	<0.2%	Yes	0.8	0.0	No
3694 Paper Tape Punch 110 cps	9.0	?	0.0	Yes	9.0	<0.02%	Yes	3.0	0.0	No
3152 Line Printer 150 lpm	400 + 9.7LS	0	---	---	375	<0.01%	0.1msec	25 + 9.7LS	0.0	No
1403 Model 2 Printer 600 lpm	100 + 5LS	0	---	---	80	<0.07%	0.1msec	20 + 5LS	0.0	No
1403 Model 3 Printer 1,100 lpm	55 + 5LS	0	---	---	35	<0.2%	0.1msec	20 + 5LS	0.0	No
501 Printer 1,000 lpm	60 + 6.7LS	0	---	---	45	<0.07%	0.1msec	13 + 6.7LS	0.0	No
505 Printer 500 lpm	120 + 6.7LS	0	---	---	105	<0.03%	0.1msec	13 + 6.7LS	0.0	No
601 Magnetic Tape Unit 20.8 KC	---	3.0	0.0	Yes	Var	0.4%	Yes	3.0	0.0	No
603 Magnetic Tape Unit 41.7 KC	---	2.75	0.0	Yes	Var	0.9%	Yes	2.25	0.0	No
604 Magnetic Tape Unit 60.0 KC	---	2.75	0.0	Yes	Var	1.2%	Yes	2.25	0.0	No
606 Magnetic Tape Unit 83.4 KC	---	2.75	0.0	Yes	Var	1.7%	Yes	1.75	0.0	No
607 Magnetic Tape Unit 120 KC	---	2.75	0.0	Yes	Var	2.4%	Yes	1.75	0.0	No
692 Magnetic Tape Unit 30 KC	---	?	0.0	Yes	Var	0.8%	Yes	?	0.0	No
694 Magnetic Tape Unit	---	?	0.0	Yes	Var	1.6%	Yes	?	0.0	No
696 Magnetic Tape Unit	---	?	0.0	Yes	Var	2.4%	Yes	?	0.0	No
3692 Program Controlled Input-Output Typewriter	67	0	---	---	Var	<0.001%	Yes	0	---	---
3293 Incremental Plotter	3.3 or 5.0	100	0.0	No	No	<0.03%	No	100	0.0	No

av Average time — see main report section on this device for details.
b For the word mode; if character mode is used, the core usage should be quadrupled.
I Interlace factor (can be 1, 2, 4, 8, 16, or 32).
LS Number of lines skipped between successive printed lines
Var Data transmission time varies with record length.

SOFTWARE

The program-compatible Control Data 3100, 3200, and 3300 computer systems all utilize the same software. For a complete description, refer to the CDC 3200 Computer System Report, pages 245:151. 100 through 245:191. 600.

The Instruction List and Data Code Table for the Control Data 3100, 3200, and 3300 systems will also be found in the CDC 3200 report, on pages 245:121. 100 and 245:141. 100, respectively.

SYSTEM PERFORMANCE

GENERALIZED FILE PROCESSING (255:201.1)

These problems involve updating a master file from information in a detail file and producing a printed record of the results of each transaction. This application is one of the most typical of commercial data processing jobs and is fully described in Section 4:200.1 of the Users' Guide.

In the graphs for Standard File Problems A, B, C, and D, the total time required for each standard configuration to process 10,000 master file records is shown by solid lines. For Configuration VIIB, where all four input-output files are on magnetic tape, total times for cases using both unblocked and blocked records in the detail and report files are shown by means of solid and dashed lines, respectively. Central processor time is essentially the same for all configurations, and never becomes the controlling factor.

Worksheet Data Table 1 (page 255:201.011) shows that the printer is the controlling factor on total time required over most of the detail activity range for the integrated Configuration VI. In these configurations the detail file is read by the on-line card reader and the report file is produced by the on-line printer. The central processor is occupied for only a small fraction of the total processing time. In most of the cases, it will be more efficient to divide the file processing problem into three separate runs: a card-to-tape transcription of the detail file, the processing run with all files on magnetic tape, and a tape-to-card transcription of the report file. The curves for paired Configuration VIIB show the time required for the all-tape main processing run in this case and point out that the computer is tape bound. The card-to-tape and tape-to-printer transactions will run at card reader and printer-limited speeds, and their demands on the processor will be small.

The master file record format is a mixture of alphameric BCD and pure binary numeric times, designed to minimize the number of time-consuming radix conversion operations required. (Even so, most of the central processor time is devoted to editing and radix conversion operations, using programmed, nonstandard subroutines.) An optimized degree of packing led to a record length of 20 words (the equivalent of 80 6-bit characters).

SORTING (255:201.2)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed from the time for Standard File Problem A according to the method explained in the User's Guide, Paragraph 4:200.213, using a three-way merge.

MATRIX INVERSION (255:201.3)

In matrix inversion, the object is to measure central processor speed on the straightforward inversion of a non-symmetric, non-singular matrix. No input-output operations are involved. The standard estimate is based on the time to perform cumulative multiplications ($c = c + a_i b_j$) in 36-bit precision floating point (see Paragraph 255:051.422).

GENERALIZED MATHEMATICAL PROCESSING (255:201.4)

This problem measures over-all system performance on a simple mathematical application that involves widely varying ratios of input-to-computation-to-output volume, as described in Section 4:200.4 of the Users' Guide. As in the File Processing problem, the total elapsed time is shown by the solid lines in Graph 255:201.400.

All computations are performed in single precision floating point. In Configuration VI, input is via the on-line card reader and output is via the on-line printer. If card-to-tape and tape-to-printer transcriptions are carried out in separate runs, the time required for the all-tape main processing run can be read from the curves for paired Configuration VIIB.

GENERALIZED STATISTICAL PROCESSING (255:051.5)

This problem measures overall system performance on a common statistical application: the development of cross-tabulation tables, as in the analysis of the results of a survey. The problem is defined in Section 4:200.5 of the Users' Guide, and the performance of the Control Data 3300 is shown in Graph 255:201.500.

WORKSHEET DATA TABLE 1

	Item		Configuration: VI		VII B (Unblocked Files 3 & 4)		VII B (Blocked Files 3 & 4)		Reference
1 Standard File Problem A Input-Output Times	Char/block	(File 1)	960		960		960		4:200.112
	Records/block	K (File 1)	12		12		12		
	msec/block	File 1 = File 2			26		26		
		File 3	50		11.5		26*		
		File 4			12.0		38*		
	msec/switch	File 1 = File 2							
		File 3							
		File 4							
	msec penalty	File 1 = File 2	0.15		0.15		0.15		
		File 3	0.01		0.01		0.01		
		File 4	0.02		0.02		0.02		
2 Central Processor Times	msec/block	a_1	0.64		0.64		0.64		4:200.1132
	msec/record	a_2	0.17		0.17		0.17		
	msec/detail	b_6	0.93		0.93		0.93		
	msec/work	b5 + b9	0.12		0.12		0.12		
	msec/report	b7 + b8	1.11		1.11		1.11		
3 Standard File Problem A F = 1.0	msec/block for C.P. and dominant column.		C.P.	I/O	C.P.	I/O	C.P.	I/O	4:200.114
		a_1	0.64		0.64		0.64		
		a_2K	2.04		2.04		2.04		
		a_3K	26.50		26.50		26.50		
		File 1 Master In	0.15		0.15	26	0.15	26	
		File 2 Master Out	0.15		0.15		0.15		
		File 3 Details	0.15		0.15		0.15		
		File 4 Reports	0.22	1,920	0.22	144	0.22	38	
		Total	29.85	1,920	29.85	170	29.85	64	
4 Standard File Problem A Space	Unit of measure	(24-bit word)							4:200.1151
		Std. routines	600		600		600		
		Fixed	2,000		2,000		2,000		
		3 (Blocks 1 to 23)	600		600		600		
		6 (Blocks 24 to 48)	1,000		1,000		1,000		
		Files	2,000		2,000		2,000		
		Working	600		600		600		
		Total	6,800		6,800		6,800		

* 12 records per block.

WORKSHEET DATA TABLE 2

	Item		Configuration: VI	VIIIB	Reference
5 Standard Mathematical Problem A	Fixed/Floating point		Floating	Floating	4:200.413
	Unit name	input	Card Reader	604 Tape	
		output	Line Printer	604 Tape	
	Size of record	input	1 card	80 char	
		output	1 line	120 char	
	msec/block	input T_1	50	11.3	
		output T_2	120	12.0	
	msec penalty	input T_3	0.01	0.01	
		output T_4	0.02	0.02	
	msec/record	T_5	3.2	3.2	
	msec/5 loops	T_6	1.6	1.6	
	msec/report	T_7	1.9	1.9	
7 Standard Statistical Problem A	Unit name		Tape	604 Tape	4:200.512
	Size of block		960 char	960 char	
	Records/block	B	15	15	
	msec/block	T_1	34.0	26.0	
	msec penalty	T_3	0.16	0.16	
	C.P. msec/block	T_5	0.005	0.005	
	C.P. msec/record	T_6	0.007	0.007	
	C.P. msec/table	T_7	0.025	0.025	

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes
Master file:. . . . . . . 108 characters (packed into 20 CDC 3300 words).
Detail file: . . . . 1 card.
Report file:. . . . . . . 1 line.

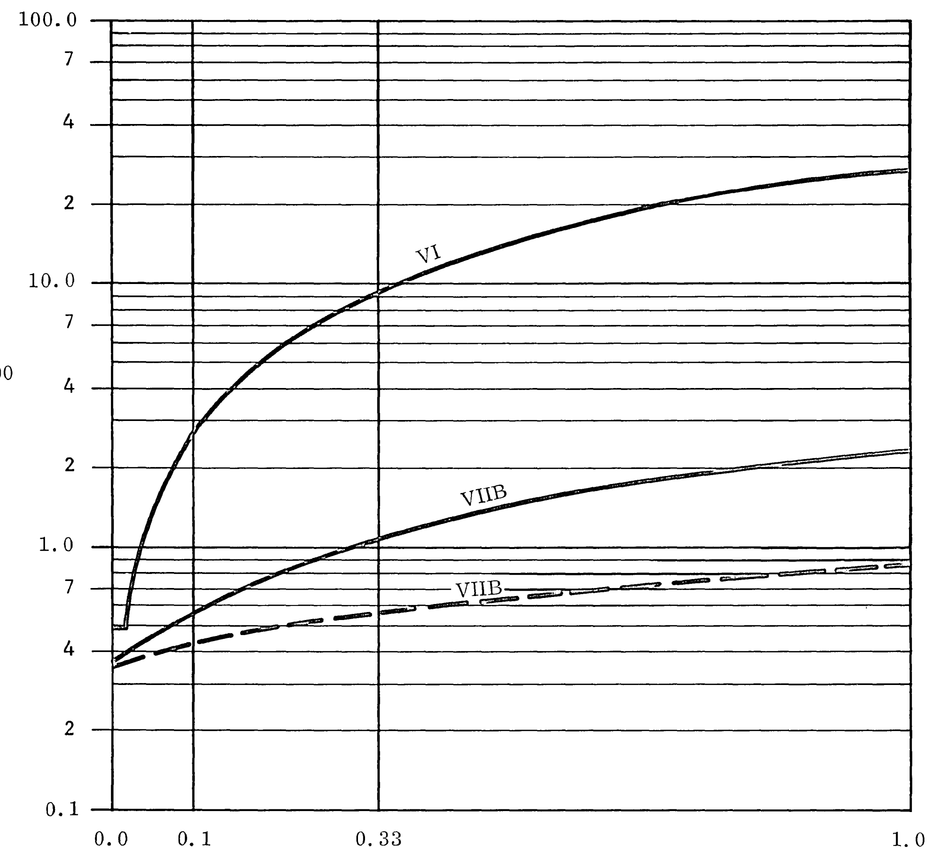
.112 Computation:. . . . . . . standard.

.113 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.113.

.114 Graph: . . . . see graph below.

.115 Storage space required
Configuration VI: . . . 6,800 words.
Configuration VII B (Unblocked Files 3 & 4): . . . . 6,800 words.
Configuration VII B (Blocked Files 3 & 4): . . . . 6,800 words.

Time in Minutes to Process 10,000 Master File Records



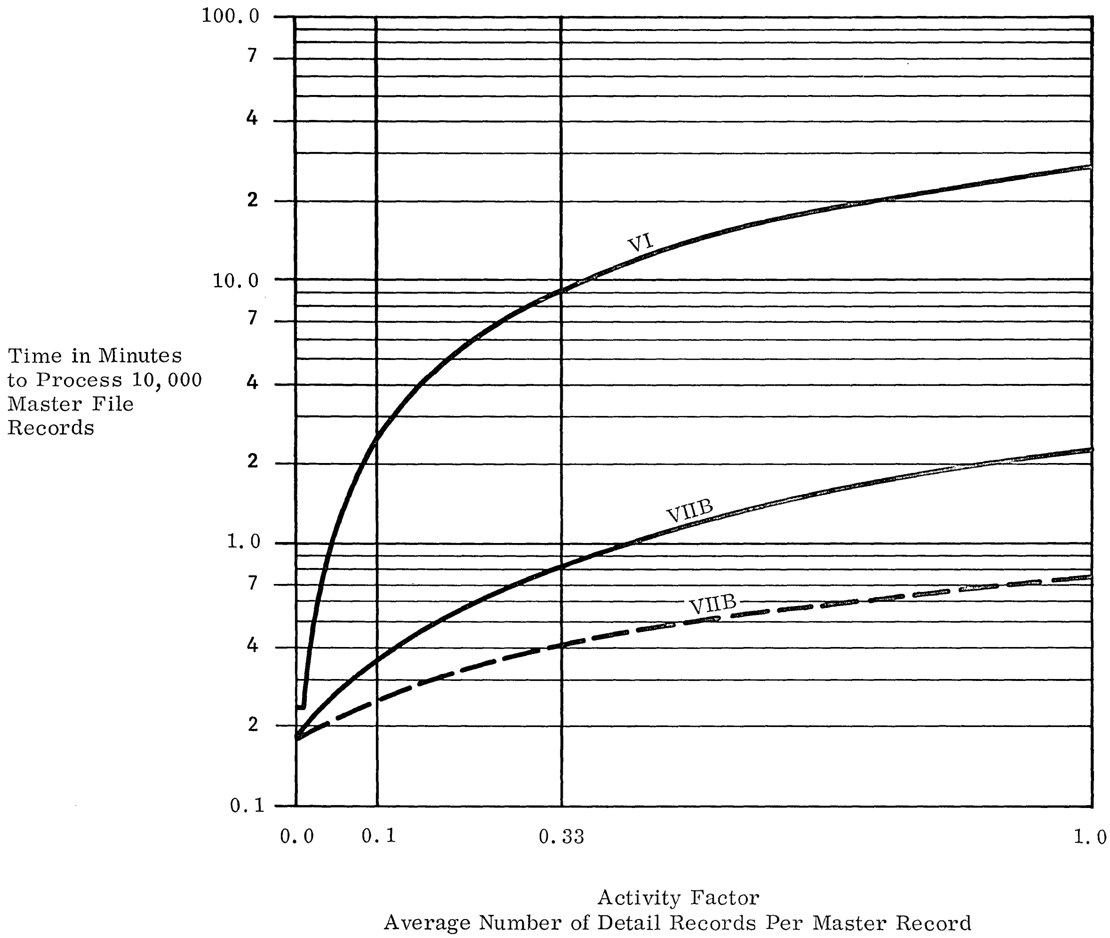
Activity Factor
Average Number of Detail Records Per Master Record

NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 255:031.

.12 Standard File Problem B

.121 Record sizes
Master file: . . . . 54 characters.
Detail file: . . . . 1 card.
Report file: . . . . 1 line.

.122 Computation: . . . . standard.
.123 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.12.
.124 Graph: . . . . see graph below.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 255:031.

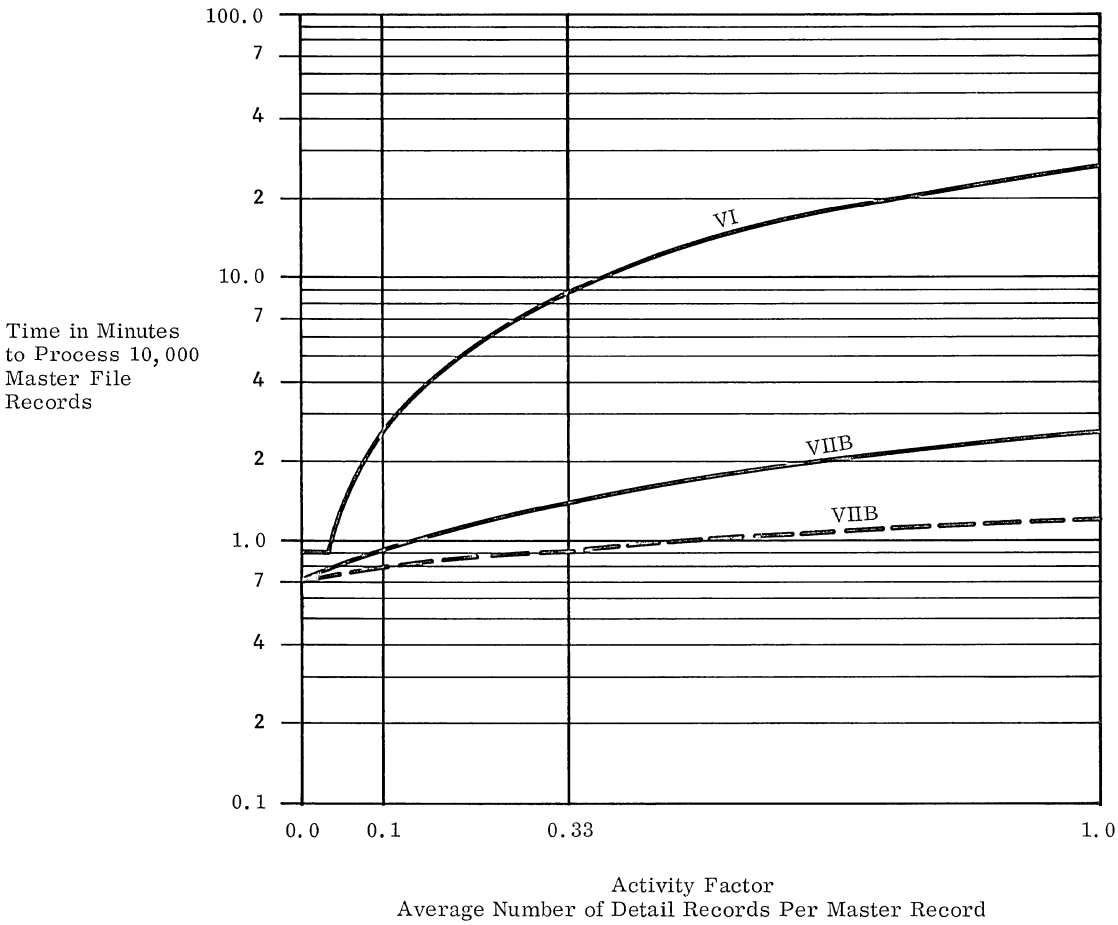
.13 Standard File Problem C

.131 Record sizes
- Master file: . . . . 216 characters.
- Detail file: . . . . 1 card.
- Report file: . . . . 1 line.

.132 Computation: . . . . standard.

.133 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13.

.134 Graph: . . . . see graph below.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 255:031.

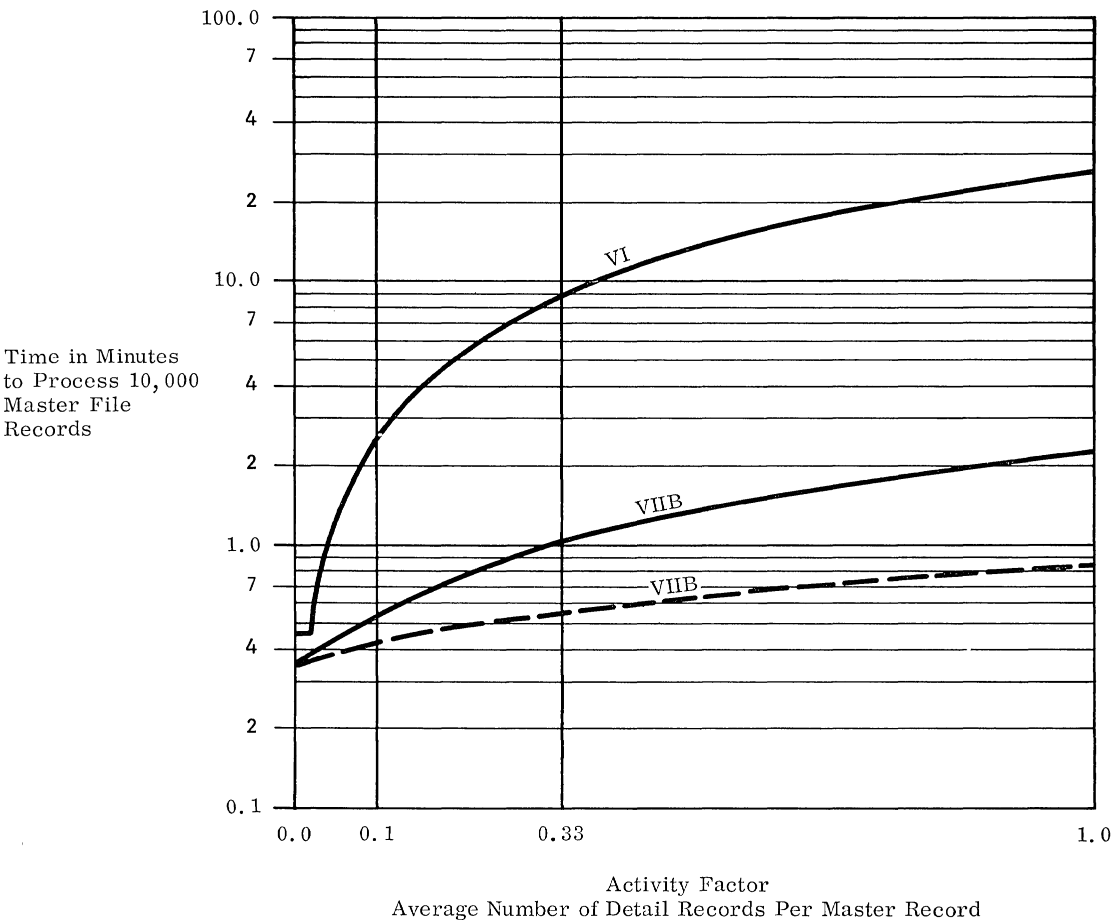
.14 Standard File Problem D

.141 Record sizes
- Master file: . . . . 108 characters.
- Detail file: . . . . 1 card.
- Report file: . . . . 1 line.

.142 Computation: . . . . trebled.

.143 Timing Basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.14.

.144 Graph: . . . . see graph below.



NOTE: Dashed line denotes blocked Files 3 and 4; Roman numerals denote standard system configurations shown in Section 255:031.

AUERBACH

.2 SORTING

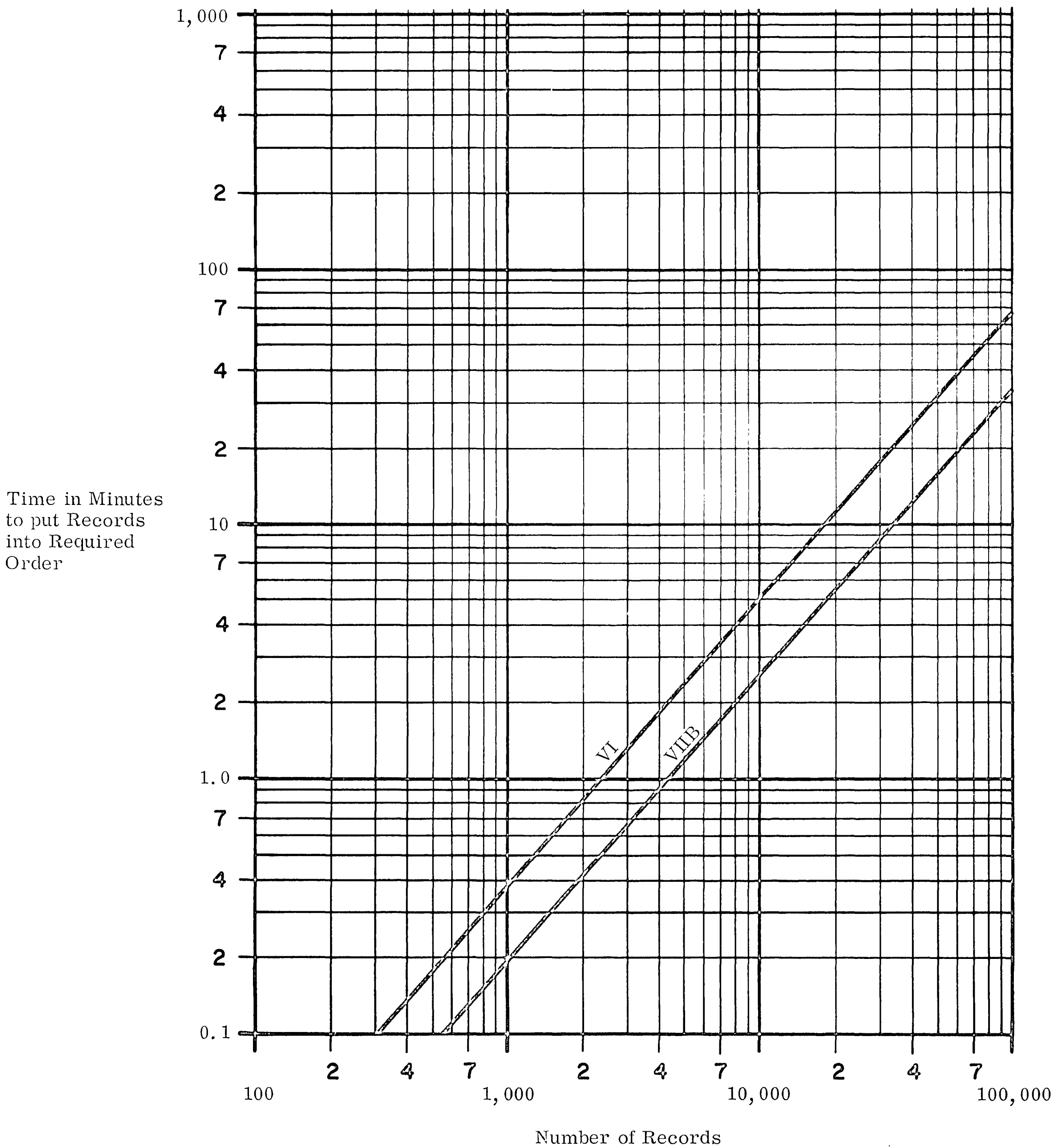
.21 Standard Problem Estimates

.211 Record size: . . . . 80 characters.

.212 Key size: . . . . 8 characters.

.213 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . see graph below.



NOTE: Roman numerals denote standard system configurations shown in Section 255:031.

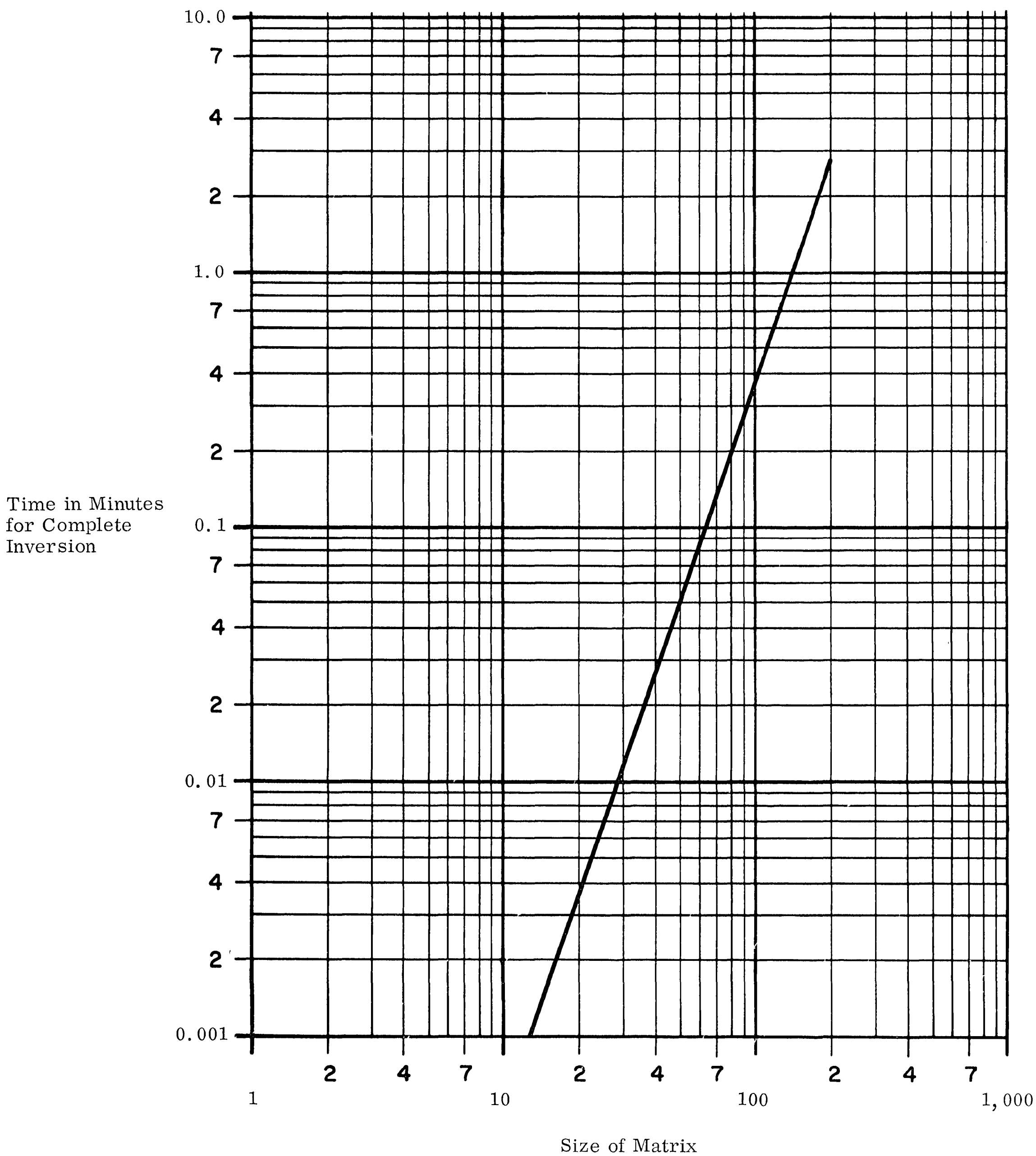
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits.

.312 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . see graph below.



.4 GENERALIZED MATHEMATICAL PROCESSING

.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . . 10 signed numbers, avg. size 5 digits, max. size 8 digits.

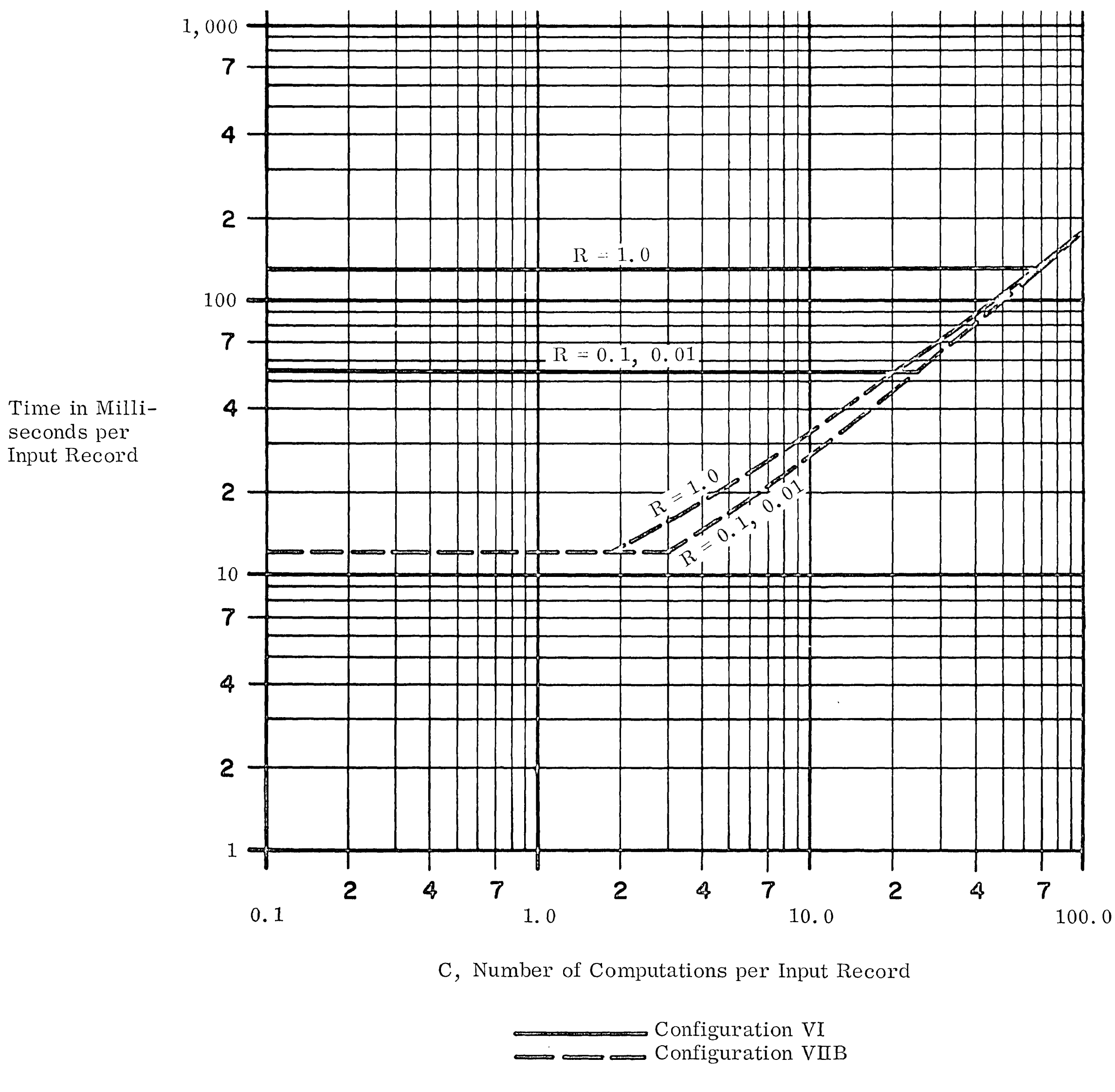
.412 Computation: . . . . 5 fifth-order polynomials. 5 divisions. 1 square root.

.413 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide 4:200.413.

.414 Graph: . . . . see graph below.

FLOATING POINT, 36-BIT PRECISION

R = NUMBER OF OUTPUT RECORDS PER INPUT RECORD



.5 GENERALIZED STATISTICAL PROCESSING

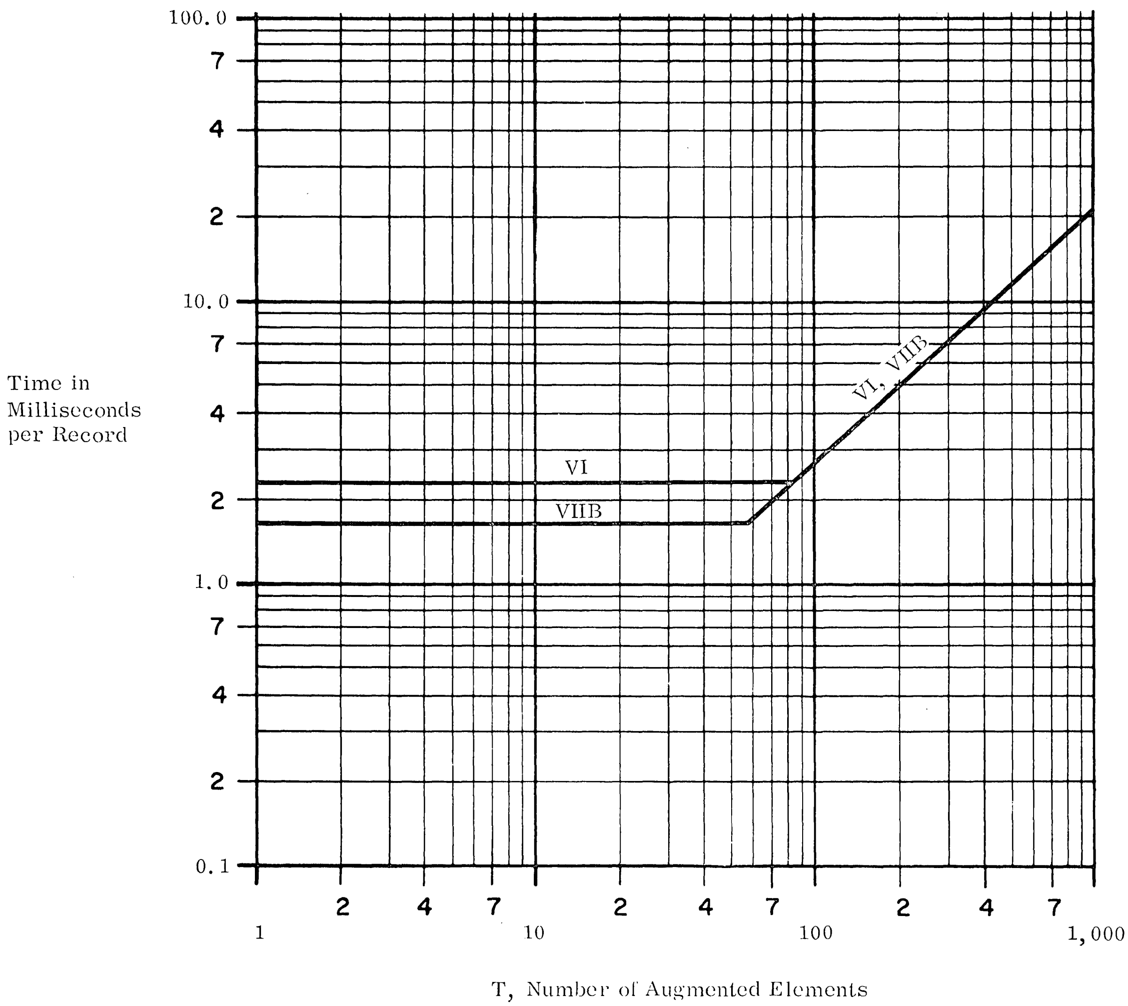
.51 Standard Statistical Problem A Estimates

.511 Record size: . . . . thirty 2-digit integral numbers.

.512 Computation: . . . . augment T elements in cross-tabulation tables.

.513 Timing basis: . . . . . . using estimating procedures outlined in Users' Guide, 4:200.513.

.514 Graph: . . . . see below.



Roman numerals denote standard configurations.

CDC 6000 SERIES

Control Data Corporation

STANDARD EDP REPORTS

AUERBACH INFO, INC.

PRINTED IN U. S. A.

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CONTENTS

INTRODUCTION

.1 SUMMARY

The Control Data 6000 Series is a group of three very fast, large-scale computer systems that have been designed to provide users with vast computational power in service of a large number of concurrently-operating programs. The marketing campaign for the 6000 Series, directed to both scientific and commercial computer users, emphasizes that the use of a large central computer system can be more economical for a company than the use of multiple smaller-scale systems scattered over a wide area.

Such operational goals have necessitated the design of specialized central computing equipment, flexible peripheral systems, extensive data communications facilities, and highly sophisticated software support. The minimum hardware configuration for the 6400 computer system — at the low end of the 6000 Series — includes one Central Processor with a 100-nanosecond clock-cycle time, a 1-microsecond Central Memory of 32,768 60-bit words, ten independently-operating Peripheral and Control Processors with private core storage units of 4,096 12-bit words each, and twelve floating input-output Data Channels that are each capable of transmitting I/O data at a rate of 2 million characters per second. Peripheral devices can include additional Peripheral and Control Processors, a new Extended Core Storage unit, several new display units, disc files, magnetic tape units, and all of the peripheral units designed for use with the Control Data 3000 Series systems. Control Data also makes available the controllers, multiplexors, and adapters necessary to control data communications networks that utilize a wide variety of remote terminal equipment.

Software for the 6000 Series represents a determined effort by Control Data to dispel a once-widespread impression that the corporation was unwilling or unable to develop and supply full-scale, integrated software support. Effective utilization of the powerful 6000 Series hardware demands a comprehensive, integrated software control system, and Control Data supplies such an operating system (SIPROS) with each 6000 Series system. The concurrent operation of multiple processors simultaneously executing a large number of programs is the normal mode of operation for the 6000 Series systems. Standard equipment configurations that include the Extended Core Storage unit are also well suited for time-sharing operations. The SIPROS operating system coordinates and controls the many levels of concurrent operations inherent in these multiprocessing, multiprogramming, and time-sharing modes of operation.

Monthly rentals for the 6000 Series systems range from about $30,000 for a basic 6400 system to about $170,000 for a large 6800 system. The 6800 computer system appears to be rivalled only by the recently-announced Burroughs B 8500 in competition for the title of "largest computer in the world," both in terms of magnitude of pure processing power and potential size of system hardware configuration.

The Control Data 6600 was first delivered early in 1965. The less powerful, cheaper Control Data 6400 system, announced in December 1964, will have its initial delivery early in 1966. The ultra-high-speed 6800 (more than four times faster than the 6600) was also announced in December 1964. First delivery of the 6800 system is expected sometime in 1967.

.2 PROCESSORS

.21 Central Processors

Every Control Data 6000 Series computer system includes a Central Processor, a central core memory, and ten Peripheral Processors, each with a private core memory bank. The 6600 and 6800 Central Processors contain ten specialized, independently-operating functional units that theoretically enable them to execute up to ten machine instructions simultaneously. The 6400 Central Processor contains a single general-purpose instruction execution unit. Additional central processing power can be obtained in 6400 computer systems by including a second 6400 Central Processor in the configuration.

A 6000 Series Central Processor, at any one time, can access only one continuous segment of the central core memory, as defined by a Lower Boundary and an Upper Boundary. Any reference to a location outside this area which is attempted by a Central Processor program automatically results in an interrupt and a call to the executive program. The processor

.21 Central Processors (Contd.)

does not access the central memory directly either for instructions or operands; instead, it uses an eight-word instruction stack (which holds the present instruction and the previous seven instruction words) and 24 operating registers: eight A (Address) registers, eight B (B-line or index) registers and eight X (60-bit operand) registers. Although the B-registers are used for purposes analogous to index registers, the form of the 6000 Series instruction, which never directly refers to central core memory operands, precludes the use of indexing or indirect addressing in the usual sense of these terms.

The relationships among the processors, memory units, and input-output channels are shown in Figure 1. On the left, the input-output channels are all shown connected to a ten-way switch, so that input-output data can be passed through the independent memory banks of any of the ten identical Peripheral Processors (numbered 1 through 10). Each of the Peripheral Processors also has access to the central core memory of the system, and data can be transferred between the Peripheral Processor memories and the central memory without any Central Processor operations.

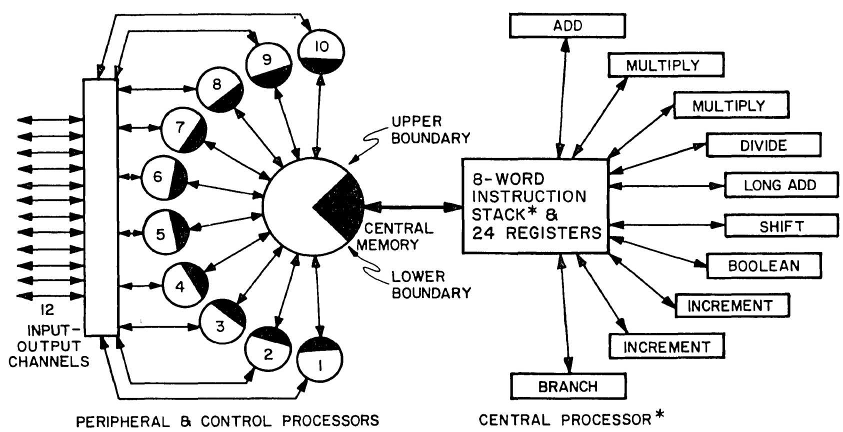


Figure 1. Structure of the Control Data 6000 Series Processors

* Note: The 6400 has no instruction stack nor multiple arithmetic processing units.

The instruction stack and the 24 operating registers act as a buffer between the comparatively slow core memory and the ten fast functional units, and allow the simultaneous operation of more than one of these units. Use of this relatively small number of registers permits great reductions in the instruction sizes, so that many three-address instructions require only 15 bits, or one-fourth of an instruction word.

Parallelism of operation is one of the keys to the rapid processing speeds of the 6000 Series Central Processors. In addition to the ten concurrently-operating functional units in the 6400 and 6600 Central Processors, all Central Processors in the Series have the ability to access simultaneously up to eight locations in Central Memory. As a result, instructions and operands can be accessed in anticipation of their actual need, and Central Processor delays caused by the need to await completion of Central Memory accesses can be greatly reduced.

The internal clock-cycle time of the 6400 and 6600 Central Processors is identical — 100 nanoseconds. Many instructions within the simplified 6000 Series instruction set consume only three or four internal Central Processor cycles. The 6600's 8-word instruction stack and 10 functional units make its performance considerably better than that of the 6400 (see comparative task timings in Table I). The 6800 Central Processor has a basic clock-cycle time of 25 nanoseconds and generally performs four times as fast as the 6600. However, Control Data intimates that the actual performance of the 6800 Central Processor will be significantly better than its specifications.

Table I lists some characteristics and representative execution times of the Control Data 6400, 6600, and 6800 Central Processors.

(Contd.)

TABLE I: CHARACTERISTICS OF THE 6000 SERIES CENTRAL PROCESSORS

System Identity			CONTROL DATA 6400	CONTROL DATA 6600	CONTROL DATA 6800
Computer System Report No.			263	264	265
DATA STRUCTURE	Word Length	Binary Bits	60	60	60
		Decimal Digits	18	18	18
		Characters	10	10	10
	Floating Point Representation	Radix	Binary	Binary	Binary
		Fraction Size	48 or 96 bits	48 or 96 bits	48 or 96 bits
		Exponent Size	11 bits plus sign	11 bits plus sign	11 bits plus sign
CENTRAL PROCESSOR	Model Number		6401, 6404, 6405	6601, 6604, 6605	6801, 6804, 6805
	Arithmetic Radix		Binary	Binary	Binary
	Operand Length, Words		1	1	1
	Instruction Length, Words		1/4 or 1/2	1/4 or 1/2	1/4 or 1/2
	Addresses per Instruction		3	3	3
	Likely Fixed Point Execution Times, μsec (5 Digits Min. Precision)	c = a + b	0.6*	0.3*	0.08*
		c = ab	—	—	—
		c = a/b	—	—	—
	Likely Floating Point Execution Times, μsec	c = a + b	1.1*	0.4*	0.1*
		c = ab	5.7*	1.0*	0.25*
		c = a/b	5.6*	2.9*	0.73*
	Checking	Data Transfers	None	None	None
		Arithmetic	Interrupt	Interrupt	Interrupt
	Number of Index Registers		Eight	Eight	Eight
	Indirect Addressing		Not applicable	Not applicable	Not applicable
	Special Editing Capabilities	Mathematical	None	None	None
		Commercial	None	None	None
	Boolean Operations		AND, INC OR, EXC OR	AND, INC OR, EXC OR	AND, INC OR, EXC OR
	Table Look-up		None	None	None
	Console Typewriter	Input	Yes	Yes	Yes
		Output	No; displays are used	No; displays are used	No; displays are used
	Features and Comments		Supported by 10 Peripheral Processors; sequential execution of one instruction at a time.	Supported by 10 Peripheral Processors; up to 10 instructions can be executed concurrently.	Four times as fast as the CDC 6600; otherwise almost identical.

* Execution times are elapsed times for Register-to-Register tasks, with no allowance for transferring data to and from main core storage; these data transfers can be overlapped and do not necessarily add to the time used.

.22 Peripheral and Control Processors

The ten Peripheral and Control Processors that form an integral part of every Control Data 6000 Series computer system are logically and functionally independent processors, each with a private core storage bank of 4,096 12-bit words. The Peripheral Processors have an instruction repertoire of 64 instructions, including fixed-point binary addition and subtraction, testing instructions, incrementing instructions, and an Exchange Jump instruction that facilitates switching between programs.

Due to the power and flexibility of the Peripheral Processors, many tasks that are performed by the central processors in more conventional systems are divided among the 6000 Series Peripheral Processors, permitting the 6000 Series Central Processor to concentrate upon performing the central computational loops of multiple programs. The principal roles of the Peripheral and Control Processors include controlling all input-output operations, performing executive and monitor services for the entire system, performing data transcription operations, and serving the Central Processor program by performing time-consuming operations such as data conversions, file searching, and array manipulations.

The Peripheral and Control Processors that are used with the Control Data 6400 and 6600 systems have a clock-cycle time of 1 microsecond and use core storage modules with the same cycle time. The 6800 Peripheral Processors have an internal clock-cycle time of

.22 Peripheral and Control Processors (Contd.)

250 nanoseconds and a matching cycle time in their core memory modules. Most Peripheral Processor instructions can be executed within one to four processor cycles. Transfer of data between each of the Peripheral Processors and any of the twelve standard input-output Data Channels can proceed at up to 2 million characters per second in the 6400 and 6600 computer systems and at up to 8 million characters per second in the 6800 computer system.

.3 INTERNAL STORAGE

The Control Data 6000 Series offers a wide variety of internal storage devices of diverse capacities and speeds, designed to serve specific functions within the total integrated computer system. Central Memory can be considered as the private, high-speed core storage for the Central Processor, with direct data paths to the Peripheral Processors and to the optional Extended Core Storage unit. Central Memory capacities range from 320,768 to 1,310,720 six-bit characters; transfer rates extend from 80 to 400 million characters per second, depending on the unit's size and model. Table II lists the principal characteristics of the Central Memory units.

TABLE II: CENTRAL MEMORY CHARACTERISTICS

Computer System	6400 or 6600			6800		
Core Storage Capacities, in 60-bit Words	32,768	65,536	131,072	32,768	65,536	131,072
Cycle Time per Word, μsec	1.0	1.0	1.0	0.25	0.25	0.25
Independent Banks of Storage	8	16	32	8	16	32
Interleaved Cycle Time per Word, μsec	0.13	0.10	0.10	0.03	0.025	0.025
Peak Transfer Rate, Millions of Words per Second	8	10	10	32	40	40

Each of the ten Peripheral Processors has a core memory unit consisting of 4,096 12-bit words to serve the general computational needs of the Peripheral Processor, to hold in residence the system's control programs, and to provide private input-output buffer areas for data transferred to and from Central Memory. Data can be transferred between a Peripheral Processor memory unit and Central Memory at the rate of 2 million and 8 million characters per second in the 6400/6600 and 6800 systems, respectively.

Control Data 6000 Series users can optionally include the newly-developed Extended Core Storage unit in their hardware configuration to provide very fast and comparatively inexpensive auxiliary core storage in capacities up to 167 million characters (see Table III). Blocks of data can be transferred between Extended Core Storage and Central Memory at the rate of 100 million characters per second in the 6400 and 6600 systems. Similar transfers in the 6800 can be effected at the rate of 400 million characters per second. The entire 1,310,720 characters of a 131K 6800 Central Memory can be exchanged with the same number of characters stored in Extended Core Storage in 6.5 milliseconds. These data transfer

TABLE III: EXTENDED CORE STORAGE CHARACTERISTICS

Computer System	6400 or 6600				6800	
Extended Core Storage Capacities, in 60-Bit Words*	131,072	262,144	1,048,576	2,097,152	524,288	1,048,576
Number of Memory Banks	1	2	8	16	4	8
Number of Characters Accessed per Cycle	80	80	80	80	160	160
Cycle Time, in Microseconds	3.2	3.2	3.2	3.2	1.6	1.6
Peak Transfer Rate, Millions of Characters per Second	25	50	100	100	400	400

* Larger Extended Core Storage capacities, ranging up to 16,777,216 60-bit words, are available upon request.

.3 INTERNAL STORAGE (Contd.)

rates are so impressive that Control Data plans to utilize the technique of swapping programs between Extended Core Storage and Central Memory as the heart of its time-sharing systems for the 6000 Series. This "roll-in/roll-out" method provides the Central Processor with almost immediate access to any program.

No internal parity checking is performed in any of the 6000 Series core storage units. Control Data emphasizes the high degree of reliability built into its third-generation core memories and suggests the use of software checking techniques when absolute assurance of reliability is required. The extra time required to perform some form of software checking is implied as being insignificant in view of the extremely high processing speeds of the 6000 Series systems.

Three types of random-access disc storage units are offered as part of the 6000 Series hierarchy of storage devices. The 6603 Disk File is a Bryant-made unit capable of storing up to 80.8 million characters. Either the 6603 Disk File or the new 6607 or 6608 Disk File (with a better price/performance ratio) must be included in every 6000 Series configuration as the "System Disk." The 6607 can store up to 84 million characters of data, and the 6608 can hold up to 168 million characters. These two devices feature rapid-access actuator arms in a reactively-balanced positioning mechanism developed by Control Data. The new 850 Series Disk Storage Drives can also be used with the 6000 Series. These units provide inexpensive "Disk Pack" storage with capacities up to 9.6 million characters per pack, and Model 852's Disk Packs are compatible with those used by the IBM 1311 Disk Storage Drive. Table IV lists the principal features of these random-access disc storage devices.

TABLE IV: DISC STORAGE CHARACTERISTICS

Device	Capacity (millions of characters per unit)	Average Access Time (milliseconds)	Data Transfer Rate (char/sec)	Report Reference
6603 Disk File	80.8	93	1,048,000 to 1,342,000	260:044
6607 Disk File System	84	59.3	1,680,000	260:045
6608 Disk File System	168	59.3	3,360,000	260:045
852 Disk Storage Drive	2.0 to 2.9	77.5	77,730	260:046
853 Disk Storage Drive	4.8	70	208,333	260:046
854 Disk Storage Drive	9.7	70	208,333	260:046

INPUT-OUTPUT EQUIPMENT

Control Data provides a wide range of local and remote peripheral devices for the 6000 Series, emphasizing that input-output equipment considerations should not be permitted to impede the performance of the powerful 6000 Series processing and core storage units. Any of the input-output units provided for the Control 3000 Series computer systems (and described in Report Sections 245:041 through 245:102) can be connected to a 6000 Series system through use of 6681 Data Channel Converters. Several other devices have been developed especially for use with the 6000 Series; these units are described below.

- 6411 Augmented Input-Output Buffer and Control — a large-scale multiple-device subsystem that can virtually double the input-output capabilities of a basic 6000 Series configuration. The 6411's components include 12 high-speed bidirectional Data Channels, 10 Peripheral and Control Processors, each with a private core storage unit that consists of 4,096 12-bit words, and one Main Memory unit consisting of 16,384 60-bit words. The 6411 is, in effect, an additional 6000 Series computer system, minus the Central Processor. Up to twelve Augmented Input-Output Buffer and Control Units can be connected to a 6400 or 6600 computer system.

- 6602 Display Console — a dual-display cathode-ray unit used as the basic local console device in every 6000 Series computer system. The 6602 uses two 10-inch cathode-ray tubes as the sole output media and uses a console typewriter for input purposes. There are no other displays, indicators, switches, or other special-purpose hardware devices on the console. The system can edit and display instructions to the operator, messages and/or graphs for the programmer, or any other relevant data, in any appropriate format. The display can be retained on the scope as long as desired (perhaps until some action such

.4 INPUT-OUTPUT EQUIPMENT (Contd.)

as mounting a tape has occurred) and then erased to make room for other displays. Each line in the display can be up to 64 characters wide, and a maximum of 32 lines can be displayed. Graphical data can be displayed, but at present there is no provision for light pen input.

During normal operation, one of the two scopes is reserved for communication with the computer operators and the other is used for messages and displays initiated by the program itself (see Figure 2). At least one Model 6602 Display Console is used with each Control Data 6000 Series system. Additional consoles can be used in conjunction with time-shared operations, with each scope servicing a different program or group of programs.

- 6090 Entry/Display Console — a 14-inch cathode-ray tube display device and associated typewriter-style keyboard, used as the basic component of a high-speed data entry and retrieval system. Slow-speed card reader and printer units can operate in conjunction with the 6090 Console to provide hard-copy records of the data requests and the retrieved information. Either 10 or 20 lines of 50 symbols can be displayed on the 6090's output screen. The 6090 is usually used as a remote unit, communicating with the central computer over voice-grade telephone lines.
- 6060 Remote Calculator — a desk-type electronic calculator that permits users in remote locations to utilize the mathematical processing capabilities of a large-scale central computer. Problems can be keyed in on the keyboard, using a simplified FORTRAN-like mathematical notation. Computer-generated solutions are transmitted to the site of the 6060 Calculator over voice-grade lines and displayed on an illuminated 12-digit display panel.
- 626 14-Track Magnetic Tape Unit — a specially-designed unit capable of recording at 800 rows per inch, with each row holding two 6-bit characters and two parity bits. The speed of the one-inch tape is 150 inches per second, developing a peak data transfer rate of 240, 000 6-bit characters per second. The 626 is not an industry-compatible unit; it was designed to provide high-performance data transfer capabilities within a 6000 Series system. (Standard 7-track and 9-track IBM-compatible magnetic tape units are also provided for use with the 6000 Series.)

.5 DATA COMMUNICATIONS

Due to the great power inherent in the 6000 Series processing equipment, many installations will include numerous remote devices communicating with the central computer via communications lines. Control Data offers facilities to connect any of its own remote terminal equipment and most of the industry-standard terminal devices to the 6000 Series systems.

The 3276 Communication Terminal Controller is a multiplexing control unit that enables a wide variety of standard and specialized data communications devices to be connected to the standard 6000 Series Data Channels via a 6681 Data Channel Converter. First used with the Control Data 3000 Series systems, the 3276 Controller can control up to 32 simplex telegraph-grade lines (16 sending and 16 receiving), or up to 16 half-duplex or full-duplex telegraph-grade lines, or up to 8 half-duplex or full-duplex voice-grade lines. The 3276 provides the speed and mode conversions required to communicate with the 6000 Series systems.

The 6600 Series Data Set Controllers are single-speed communications control units designed specifically for the 6000 Series computer systems. Five different models permit various types of communications devices and remote computer systems to be connected directly to the 6000 Series Data Channels. The 6600 Series Controllers communicate with the remote devices over the public or private communications facilities of the telephone or telegraph companies, using standard data set modems as interfacing units at the remote and central ends of the transmission lines. One model permits computer-to-computer communication at 40, 800 bits per second over Telpak A lines. Another model permits up to 200 Teletype Model 33 or 35 terminals to communicate with a single 6000 Series Data Channel.

.6 SOFTWARE

Five of the first six users of the Control Data 6600 were supplied with an interim software package centered around the "Chippewa" operating system. In addition to the standard operating system functions, such as system monitor, loader, peripheral and display device control, and library supervision, the Chippewa package also provides a FORTRAN IV compiler and a Central Processor assembly language. According to several reports, the performance of the Chippewa operating system and its components has been unimpressive and has failed to harness the potential power of the 6000 Series hardware. Control Data emphasizes that the Chippewa system is simply an interim software package, designed to permit early users to begin productive processing as soon as possible.

(Contd.)

.6 SOFTWARE (Contd.)

Beginning in December 1965 and continuing through 1967, the SIPROS operating system and its associated control routines and compilers will be delivered. SIPROS (Simultaneous Processing Operating System) is the official operating system for the 6000 Series. Control Data expects that overall efficiency of the SIPROS programs will be at least 50% better than that of the original Chippewa operating system.

SIPROS will be delivered in three phases, with each phase adding new or expanded language and control modules. SIPROS 1.0, to be delivered in December 1965, includes basic operating system functions, many of which are listed below. Phase 2 will be delivered in January 1966 and includes the routines necessary to handle all 3000 Series peripheral device controllers. SIPROS 3.0, scheduled for delivery in April 1966, will include all announced SIPROS functions in versions that will operate with any validly-configured 6000 Series system. A specialized version of SIPROS designed for remote time-sharing operations and centering around the Extended Core Storage unit is expected to be delivered during the third quarter of 1967.

SIPROS' Executive and Monitor routines assume full control of the system and multiprocess jobs from a job stack, using priorities to decide schedule details. One of the functions is to place the output data from a program in temporary storage when this is necessary to allow the program to run at peak operational speed. Later, when appropriate equipment becomes available, the operating system handles the output data transcriptions runs.

The operating system handles the compilation and the execution of programs written in FORTRAN-66, COBOL, ALGOL, ASCENT (the Central Processor assembly language), and ASPER (the Peripheral Processor assembly language). It is common practice for a programmer to write a program in more than one language, intermingling FORTRAN statements with ASCENT and ASPER coding, but using a common symbol table. During compilation, the FORTRAN compiler and the assemblers are loaded into Central Memory as one program in order to save load time when switching from one language to another. The resulting object program, now in binary machine-language form, can be tested and executed as one of the programs in the job stack.

SIPROS requires the use of a Model 6603 or 6607/6608 Disk File, two magnetic tape units, a card reader, card punch, and printer. Two of the ten Peripheral Processors are permanently dedicated to the operating system, and others are used by the operating system whenever they are needed. Functions which are normally handled by the Peripheral Processors include disc reading and writing (which takes two processors), loading jobs into the system, bringing jobs from the disc unit into the central memory for execution, job termination functions, data transcription functions associated with jobs being executed, off-line data transcriptions, and comparisons. These services use the Peripheral Processors on an as-available basis. A programmer can "take over" one or more Peripheral Processors for his own program, but of course this will reduce the number of Peripheral Processors available in the pool.

Control cards loaded with each job describe time limits, equipment requirements, termination instructions for normal and error cases, etc. The time limits are specified in terms of central processor time usage, maximum number of cards punched, maximum number of lines printed, and maximum length of time the program should spend in a specific input-output loop. No provision is made for placing a maximum limit upon total elapsed time for each program; this is because several programs will normally be processed concurrently, and any one program may be delayed as a result of overriding priorities of other programs.

When an error stop occurs (due to an out-of-range address, exponent overflow, or occurrence of an indefinite result), a map and/or a dump of the job's allocated memory area is produced if previously requested. In any case, upon job termination a Job Accounting Log will be created for each program and either displayed on the console or written on some output medium. Charge distribution is a responsibility of the installation. A display of a typical job accounting record is shown in Figure 2.

During the execution of a job, an input-output delay or some other occurrence may prevent that job from making further immediate use of the Central Processor. In such a case the Executive routine that resides in a reserved Peripheral Processor is notified by the monitor routine, whereupon it activates one of the other programs which is resident in the central core memory. That program will continue to make use of the central processing facilities until it too is interlocked, or until some other program which has a higher priority is able to make use of the central processing facilities. Each changeover from program to program can be accomplished within five to ten microseconds through use of a special Exchange Jump instruction.

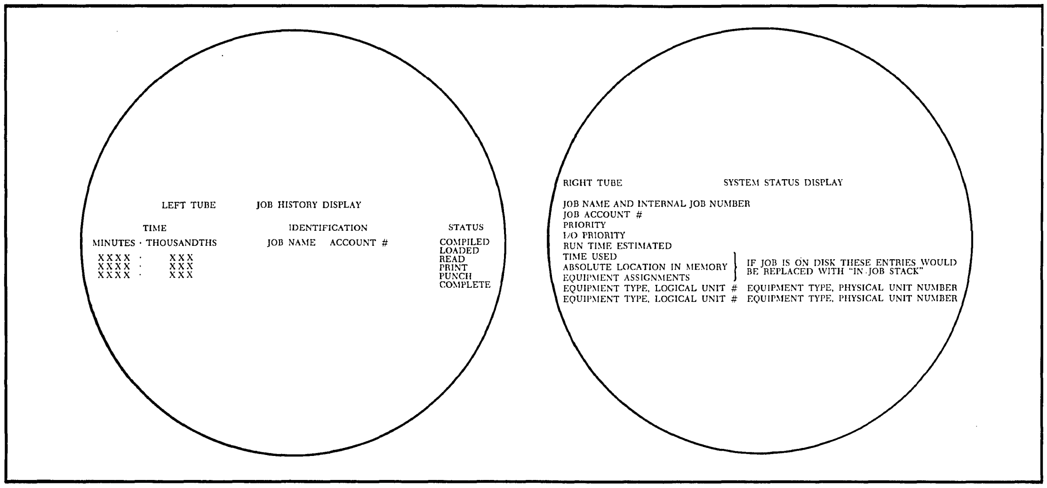


Figure 2. Cathode-Ray Display of a Set of Job Accounting Information as Produced for Each Job Handled by the SIPROS Operating System

.6 SOFTWARE (Contd.)

Control Data's FORTRAN-66 language is basically the same as FORTRAN-63 for the Control Data 1604-A computer system. The FORTRAN-66 dialect of FORTRAN IV permits the use of single and double precision floating-point, integer, complex, and logical operations in mixed mode. ENCODE/DECODE statements permit internal transfers of data within core memory, and other specific instructions are provided for input-output buffering purposes when the programmer elects to override the system's automatic buffering facilities. FORTRAN-66 also permits the use of 6000 Series central register names as operands and the use of ASPER and ASCENT assembly-language statements at any place in the FORTRAN program. The FORTRAN-66 compiler provides an optional code optimization algorithm which simulates the execution of the initially-generated object code in order to determine ways to utilize more effectively the Central Processor's 24 central registers and (in the 6600 and 6800 systems) 10 functional units.

Control Data also supplies an ASA standard FORTRAN IV compiler that can function under control of SIPROS and a special translation program that can convert existing FORTRAN IV programs to the more flexible (but non-compatible) FORTRAN-66 language.

The ASCENT and ASPER assemblers are parts of the basic integrated software package that also includes the FORTRAN-66 compiler and a library maintenance system (LIBRIOUS). ASCENT, the assembly language used for coding Central Processor routines, contains standard assembly-language features, including the use of literals, programmer-defined macros, pseudo-instructions, and system macros to control the use of Central Memory and disc storage areas. Macros are also provided to control program overlays, to initiate Peripheral Processor programs, and to communicate with SIPROS.

The ASPER assembly language permits direct control of the Peripheral Processors when specialized tasks are to be executed. (Normally, all Peripheral Processor task assignments and specifications are performed by SIPROS according to the needs of the currently-operating Central Processor program). ASPER includes all the facilities necessary to utilize the input-output functions of the Peripheral Processors, as well as the facilities to use these processors as standard computational/logical units. ASPER statements can be coded in-line with ASCENT statements.

SIPROS provides a control system called the File Manager for handling the storage, retrieval, usage, and modification of data files stored on mass storage devices. Routines are supplied for full control of drum, disc, and Extended Core Storage units, and for dumping and reloading magnetic tape files. The File Manager can normally perform its functions through the use of a single Peripheral Processor, using SIPROS control routines whenever possible.

A COBOL-65 compiler is promised for use with the 6000 Series, but no delivery date has yet been announced. The 6000 Series ALGOL compiler is scheduled for delivery in August, 1966. Other software packages planned for the 6000 Series include KWIC, SIMSCRIPT, PERT TIME, PERT COST, a Statistical Programming Package, an IBM 7090/7094 Simulator, a linear programming routine, and a sort/merge routine.

DATA STRUCTURE

.1 STORAGE LOCATIONS

Name of Location	Size	Purpose or Use
Word —		
Central Memory:	60 bits	basic addressable storage unit; holds 10 characters, up to four instructions, or one single-precision fixed-point or floating-point binary operand.
Peripheral Processor Memory:	12 bits	basic addressable storage unit; holds two characters, one single-precision fixed-point binary operand, one 12-bit instruction, or half of a 24-bit instruction.
Extended Core Storage —		
6400 and 6600 systems:	480 bits	basic unit of Extended Core Storage.
6800 systems:	960 bits	
Row (magnetic tape) —		
Models 601 through 607:	7 bits	holds 1 character and 1 parity bit.
Models 692, 694, and 696:	9 bits	holds 1 byte and 1 parity bit, or 2 decimal digits and 1 parity bit.
Model 626:	14 bits	holds 2 6-bit characters and 2 parity bits.
Sector (Disc Storage) —		
6603 Disk File:	346 12-bit words	basic addressable storage unit.
6607/6608 Disk File:	2,560 12-bit words	basic addressable storage unit.
852 Disk Storage Drive:	100 7-bit characters	basic addressable storage unit.
853/854 Disk Storage Drives:	4,833 6-bit characters	maximum-sized addressable storage unit.

.2 INFORMATION FORMATS

Type of Information	Representation
Alphanumeric character:	6-bit portion of a word.
Fixed-point binary operand:	one word of 12 or 60 bits.
Floating-point binary operand:	one 60-bit word; 48-bit fraction and 12-bit binary exponent.
Floating-point binary operand (double precision):	two 60-bit words; 96-bit fraction and 12-bit binary exponent.
Instruction —	
Central Processor:	15 or 30 bits.
Peripheral Processors:	12 or 24 bits.

SYSTEM CONFIGURATION

.1 BASIC SYSTEMS

The overall design of the Control Data 6000 Series provides the flexibility for a great variety of system configurations. Since the 6000 Series centers on the use of ultra-high-speed processors and many independent storage units, there are few, if any, constricting or conflicting configuration rules regarding the number, type, and mix of peripheral devices that can be connected to each system.

The nucleus of every 6000 Series computer system consists of a Central Processor, a large Central Memory, 10 Peripheral and Control Processors with individual small memories, and 12 bi-directional Data Channels for input-output operations. Figure 1 illustrates this basic configuration.

Figure 2 shows the Dual Central Processor capability of the 6400 computer system. The two Central Processors are functionally identical, and their use provides the Control Data 6400 user with the multiprocessing power of 12 independently-operating processors (10 Peripheral Processors and 2 Central Processors). Both Central Processors have full access to all of the storage and input-output facilities of the 6400 system.

Figure 3 represents the Extended Core Storage configuration of the Control Data 6000 Series. This configuration differs from the basic configuration in Figure 1 solely in its use of Control Data's recently-developed Extended Core Storage Unit, which provides up to 167 million characters of high-speed auxiliary core storage. This arrangement of processors and core storage provides for extremely rapid (up to 400 million characters per second) transfers of programs and segments of programs between the Central Processor and Extended Core Storage, a facility that makes possible a direct, efficient approach to time-sharing activities.

The 6600 and 6800 computer systems can also be configured in what is termed the Augmented Input-Output System, illustrated in Figure 4. The distinguishing feature of this configuration is the Augmented Input-Output Buffer and Control device, designed to nearly double the simultaneously-operating input-output device capability of the basic 6000 Series computer systems. This device is actually an input-output subsystem that includes the same number of Data Channels (12) and the same number of Peripheral and Control Processors (10, each with 4,096 12-bit words of core memory) as a full 6400 system, but has a smaller Main Memory (16,384 60-bit words) and no Central Processor. As many as 12 of these Augmented Input-Output Buffer and Control devices can be connected to a 6000 Series computer system, thereby providing virtually unlimited I/O flexibility.

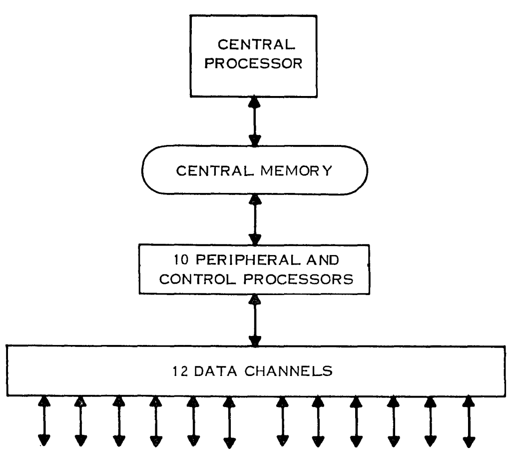


Figure 1. Basic 6000 Series System

(Contd.)

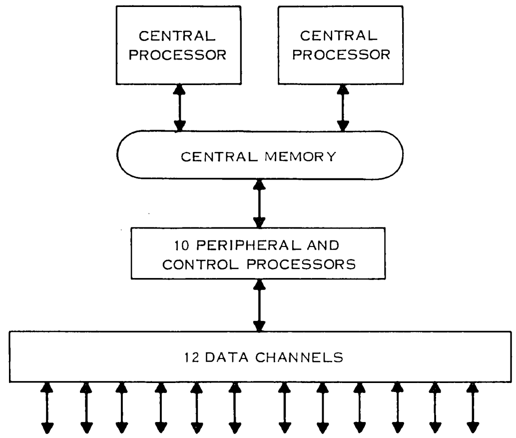


Figure 2. Dual Central Processor 6400 Computer System

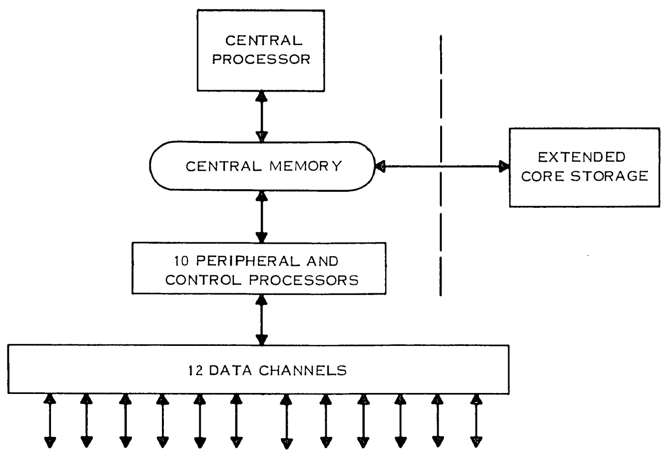


Figure 3. Extended Core Storage Configuration

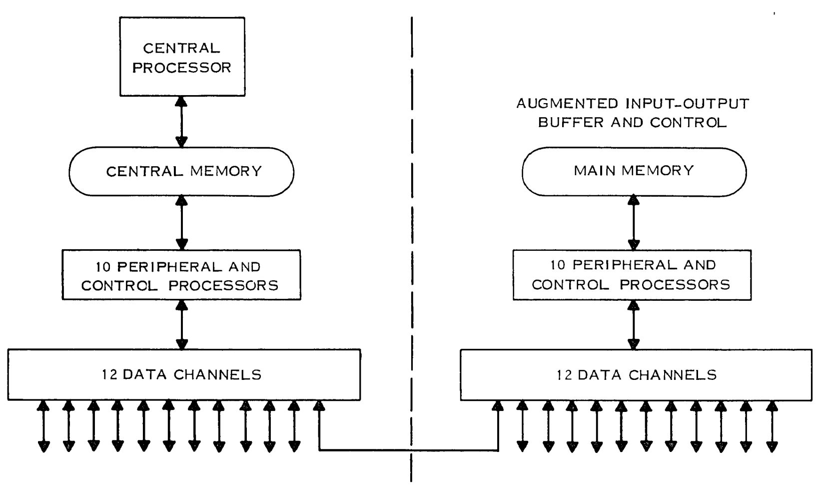


Figure 4. Augmented Input-Output System

.2 INPUT-OUTPUT EQUIPMENT

The peripheral devices can be classified in three general categories, as follows:

- System Peripherals, or those used by the computer system for operator communications and for residence and working storage for its control and problem programs. Included in this category are the following devices:

  6602 Display Console
  6603 Disk System
  6607 Disk System
  6608 Disk System
  Extended Core Storage Units

- Local Peripherals, or those directly connected to the Data Channels and normally located in the same room as the Central Processor. Devices that can be used as local peripherals include:

  800 Series Disk Files
  6603 Disk System
  IBM 2311 Disk Storage Drive
  IBM 2314 Disk Storage Drive
  861 Drum Unit
  862 Drum Unit
  3265 Drum Unit
  Extended Core Storage Units

  405 Card Reader
  415 Card Punch
  3691 Punched Paper Tape Reader/Punch
  3694 Punched Paper Tape Reader/Punch

  501 Line Printer
  505 Line Printer

  600 Series Magnetic Tape Transports

  3293 Incremental Plotter

- Remote Peripherals, or those normally connected to the Data Channels from a remote location by means of communications lines. Devices that can be used in this manner include:

  6060 Remote Calculator
  6602 Display Console

Any peripheral device designed for use with the Control Data 3000 Series (and described in Computer System Reports 245, 246, and 247) can be connected to any 6000 Series system through the use of a 6681 Data Channel Converter. Special-purpose peripheral units are available from Control Data Corporation for linking 6000 systems to many varieties of communications networks, including those using analog input and output.

Diagrams and prices of standard system configurations for each member of the Control Data 6000 Series are presented in the subreports for the individual 6000 Series models:

Control Data 6400 . . . . Section 263:031
Control Data 6600 . . . . Section 264:031
Control Data 6800 . . . . Section 265:031

INTERNAL STORAGE: CENTRAL MEMORY

.1 GENERAL

.11 Identity: . . . . Central Memory for Control Data 6400, 6600, and 6800 computer systems.

.12 Basic Use: . . . . working storage.

.13 Description

The Central Memory units for the Control Data 6000 Series are high-speed, high-capacity magnetic core storage units designed to provide memory-to-memory communication between the major components of the system at memory access speeds. The high-speed data transfers contribute significantly to the multiprogramming and multiprocessing capabilities of the Control Data 6000 Series. Table I lists the storage capacities and cycle times for the Central Memory units available with Control Data 6400, 6600, and 6800 computer systems.

The current programs and data blocks stored in the Central Memory can be simultaneously accessed by the Central Processor, by all of the Peripheral and Control Processors, and by the optional Extended Core Storage unit. As a result of this arrangement, all of the processors can operate independently of each other, and yet can communicate with each other at high speeds. The Central Memory can effectively (and simultaneously) serve as the Central Processor's private memory, as the buffer between the Peripheral and Control Processors and the Central Processor, and as storage for job stacking from the Extended Core Storage unit.

The basic memory module of the Central Memory consists of a coincident-current magnetic core memory of 4,096 12-bit words. Five of these basic modules are stacked together to form one bank of 4,096 60-bit words. Banks of memory are then grouped in 8, 16, or 32-bank units, forming the three sizes of Central Memory available with the Control Data 6000 Series: 32,768, 65,536, or 131,072 60-bit words. Each memory bank is logically independent, and consecutive memory addresses are assigned to different banks. The number of simultaneous accesses permitted to Central Memory is eight (one per bank) in 32K systems and ten (limited by the capacity of the Central Address Control) in 65K and 131K systems.

Maintenance of the Central Memory's core storage banks is facilitated by the design of the banks. Each of the five core storage modules that comprise a memory bank is constructed in small plug-in modules, individually accessible for ease of examination and/or replacement.

There are two basic core storage cycle times for the Central Memory units: the 6400 and 6600 computer systems use a Central Memory with a 1-microsecond cycle time, and the 6800 computer system uses a 250-nanosecond Central Memory. All words in storage are accessed in parallel by bank, and up to 10 banks can be accessed simultaneously. The resulting peak data transfer rates range from 8 to 40 million 60-bit words per second, as shown in Table I.

The address word for access to Central Memory locations consists of a 12-bit address quantity and a 5-bit bank quantity. The bank quantity defines one of the 8, 16, or 32 storage banks, and the address quantity defines the 4,096 separate word locations within each bank. All references to Central Memory are evaluated by its Address Control unit and then sent to the addressed word location in the appropriate bank. Address Control accepts addresses from all parts of the system according to a fixed priority scheme in order to avoid conflicts. For example, memory access requests from the Central Processor have priority over requests from the Peripheral and Control Processors.

The memory protection scheme used in the Central Memory of the Control Data 6000 Series is simple and yet apparently adequate to fulfill the needs of a system in which many programs and their data reside concurrently in the Central Memory. Each program is assigned a Field Length value at assembly, compilation, or load time. This value determines the upper boundary limit for all references to the program. Another individual program

TABLE I: 6000 SERIES CENTRAL MEMORY CHARACTERISTICS

Computer System	6400 or 6600			6800		
Core Storage Capacities, in 60-bit Words	32,768	65,536	131,072	32,768	65,536	131,072
Cycle Time per Word, μsec	1.0	1.0	1.0	0.25	0.25	0.25
Independent Banks of Storage	8	16	32	8	16	32
Interleaved Cycle Time per Word, μsec	0.13	0.10	0.10	0.03	0.025	0.025
Peak Transfer Rate, Millions of Words per second	8	10	10	32	40	40

.13 Description (Contd.)

value, the Reference Address value, is assigned to the program when it is initially called into Central Memory. This value determines the basic core storage address, or lower boundary, of the program. Any memory reference within the program that exceeds the value of the Field Length plus the Reference Address register causes an interrupt, halts the Central Processor, and alerts the system operator.

The Reference Address register scheme also facilitates dynamic program relocation, since all addresses within a program are relative to the base value of the Reference Address. This address can be altered as the program is relocated in Central Memory.

No parity checking is performed on data transferred to or from Central Memory. Control Data emphasizes the reliability of the Central Memory's core storage modules, and indicates that rapid software checks can be utilized whenever desired to ensure the accuracy of results. In addition, a memory diagnostic program can be periodically called into operation and run concurrently with the problem programs to verify that the memory modules are functioning properly.

.14 Availability: . . . . 6 months.

.15 First Delivery: . . . . . 6400: March 1966.
6600: 1965.
6800: 1967.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

.22 Physical Dimensions: . each basic memory module consists of 4,096 12-bit words.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Memory Bank

Words: . . . . 4,096.
Characters: . . . . 40,960.
Digits: . . . . 73,728.
Instructions: . . . . up to 16,384.

.26 Banks per Physical Unit: . . . . 8, 16, or 32.

.27 Interleaving Levels: . . 8 with 32K Central Memory; 10 with 65K and 131K Central Memories.

.28 Access Techniques

.281 Reading and recording method: . . . . coincident current.

.283 Type of access: . . . . uniform.

.29 Potential Transfer Rates

.292 Peak data rates; 6400 and 6600 Central Memory —
Cycling rate: . . . . . 1,000,000 cps.
Unit of data: . . . . . . 60-bit word.
Gain factor: . . . . . . 8 or 10 simultaneous accesses.
Data rate: . . . . 1,000,000 words per second.
Compound data rate: . 8,000,000 or 10,000,000 words per second.

Peak data rates; 6800 Central Memory —
Cycling rate: . . . . . 4,000,000 cps.
Unit of data: . . . . . . 60-bit word.
Gain factor: . . . . . . 8 or 10 simultaneous accesses
Data rate: . . . . 4,000,000 words per second.
Compound data rate: . 32,000,000 or 40,000,000 words per second.

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . see table below.

.32 Rules for Combining Modules: . . . . all permissible capacities are shown in Paragraph .31; modules cannot be interchanged between 6400/6600 and 6800 computer systems.

.4 CONTROLLER: . . . . no independent controller.

.5 ACCESS TIMING

.52 Simultaneous Operations: . . . . . . 8 or 10 memory accesses.

.53 Access Time Parameters and Variations

	6400/6600	6800
Access time:	0.8 μsec	0.2 μsec
Cycle time:	1.0 μsec	0.25 μsec
For data unit of:	60-bit word	60-bit word

.6 CHANGEABLE STORAGE: . . . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With Peripheral Processor Core Store: . . . . 4,096 12-bit words.

.31 Module and System Sizes (for all 6000 Series Central Memories)

Words:	32,768	65,536	131,072
Characters:	327,680	655,360	1,310,720
Instructions:	Up to 131,072	Up to 262,144	Up to 524,288
Banks:	8	16	32
Modules:	40	80	160

(Continued on Page 260:042.300, overleaf.)

INTERNAL STORAGE: PERIPHERAL PROCESSOR MEMORY

.1 GENERAL

.11 Identity: . . . . Peripheral and Control Processor Memory.

.12 Basic Use: . . . . working storage for Peripheral and Control Processor programs, and high-speed buffers between the Peripheral and Control Processors and Central Memory.

.13 Description

Each of the ten Peripheral and Control Processors included in every Control Data 6000 computer system contains its own independent core storage unit, consisting of 4,096 12-bit words. The memory cycle time for the memories associated with the 6400 and 6600 systems is 1 microsecond per word; the cycle time for the memories associated with the 6800 system is 250 nanoseconds. Effective data transfer rates of 2 million characters per second can be obtained when data is transferred between the Central Memory and a Peripheral and Control Processor memory of the 6400 and 6600 computer systems; the corresponding rate for 6800 systems is 8 million characters per second.

The Peripheral and Control Processors and their associated memory units can function independently of each other and also independently of the Central Processor and Central Memory. However, the several roles of the Peripheral Processors result in intersystem communication activities. The Peripheral Processor memories hold in residence the various control programs of SIPROS, the operating system that controls and integrates the operations of the total 6000 Series system. These memory units also hold the programs that direct input-output activities, and they act as high-speed buffers for data transmission to and from Central Memory. The Peripheral and Control Processor memory units also act as conventional memory units, supplying instructions, issuing operands, and storing results for their respective processors.

The 4,096 individual storage locations within each Peripheral and Control Processor memory unit can be addressed in several ways. A six-bit address is used to access directly the first 64 words of storage. If this six-bit address is zero, another twelve-bit address is appended to address directly any of the 4,096 locations. This 18-bit address scheme can also be used for indirect addressing of the 4,096 locations by using the first six bits as an index register to produce operand addresses.

Data from an external I/O device is read into the memory of a Peripheral and Control Processor, and then, if necessary, transferred to Central Memory for use by the Central Processor. There are four instructions that transfer one word or a block of words between the peripheral memory units and Central Memory. Separate input-output instructions control the transfer of data between the peripheral memory units and the I/O devices.

The Peripheral and Control Processor memory units do not utilize parity bits to check the integrity of data transfers. Control Data emphasizes the inherent reliability of the memory units, and suggests software checking of memory performance whenever checking is regarded as absolutely essential.

There are no memory protection features in the peripheral memory units. However, Peripheral Processor memory accesses are normally under strict control of reliable system programs assigned by SIPROS to perform specific tasks in support of Central Processor programs. User programming of the Peripheral Processors is possible through use of the ASPER assembly language, but such programming is not recommended unless absolutely essential.

.14 Availability: . . . . 9 months.

.15 First Delivery: . . . . . 1965.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

.22 Physical Dimensions: . array size is 4,096 bits by 12 bits.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent:. . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Memory Bank

Words: . . . . 4,096.
Characters: . . . . 8,192.
Instructions: . . . . 4,096.

.26 Banks per Physical Unit: . . . . .one per Peripheral Processor.

.27 Interleaving Levels: . . 1.

.28 Access Technique: . . . coincident current.

.29 Potential Transfer Rates

.292 Peak data rates: 6400 and 6600 peripheral memories —
Cycle rate: . . . . 1 μsec.
Unit of data: . . . . . . 12-bit word.
Data rate: . . . . 2 million char/sec.

Peak data rates: 6800 peripheral memory —
Cycle rate: . . . . 0.25 μsec.
Unit of data: . . . . . . 12-bit word.
Data rate: . . . . 8 million char/sec.

.3 DATA CAPACITY: . . . every Control Data 6000 Series system includes 10 independent Peripheral and Control Processor memory units, each of which contains 4,096 12-bit words.

.4 CONTROLLER: . . . . . no independent controller.

.5 ACCESS TIMING

.52 Simultaneous Operations: . . . . one operation in each of the 10 Peripheral and Control Processor memory units.

.53 Access Time Parameters and Variations

.531 For uniform access (6400, 6600) —
Access time: . . . . . . 0.5 μsec.
Cycle time: . . . . 1.0 μsec.
For data unit of: . . . 12-bit word.

For uniform access (6800) —
Access time: . . . . . . 0.125 μsec.
Cycle time: . . . . 0.250 μsec.
For data unit of: . . . 12-bit word.

.6 CHANGEABLE STORAGE: . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size: . . from 10 to 8,190 characters.

.73 Effective Transfer Rate: . . . . 2 million char/sec in 6400 and 6600.
8 million char/sec in 6800.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	impossible.	
Invalid code:	impossible.	
Receipt of data:	no check.	
Recording of data:	no check.	
Recovery of data:	no check.	
Dispatch of data:	no check.	
Timing conflicts:	check	Central Processor accesses are given priority.

INTERNAL STORAGE: CENTRAL MEMORY (CONTINUED FROM PAGE 260:041.130)

.72 Transfer Load Size (Contd.)

With Extended Core Store: . . . . 131,072 60-bit words.
With 6603 Disk File: . 4,096 12-bit words.

.73 Effective Transfer Rate (6400/6600)

With a Peripheral Processor Core Store: . . . . 2 million char/sec
With Extended Core Store: . . . . 48 million char/sec. (32K systems) or 60 million char/sec (65K and 131K systems).
With 6603 Disk File: . 1.2 million char/sec.
With self: . . . . 1 million char/sec (via Peripheral Processors);
With self (Contd.): . . . 2.5 million char/sec (via 6400 Central Processor); 13.3 million char/sec (via 6600 Central Processor).

.73 Effective Transfer Rate (6800)

With a Peripheral Processor Core Store: . . . . 8 million char/sec.
With Extended Core Store: . . . . 192 million char/sec (32K systems) or 240 million char/sec (65K and 131K Systems).
With 6603 Disk File: . 1.2 million char/sec.
With self: . . . . 4 million char/sec (via Peripheral Processors); 53.2 million char/sec (via Central Processor).

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	check	Control is transferred to Peripheral Processor monitor.
Invalid code:	not possible.	
Receipt of data:	none.	
Recording of data:	none.	
Recovery of data:	none.	
Dispatch of data:	none.	
Timing conflicts:	not possible.	
Reference to locked area:	check	Control is transferred to Peripheral Processor monitor.

INTERNAL STORAGE: EXTENDED CORE STORAGE

.1 GENERAL

.11 Identity: . . . . 6400 Extended Core Storage.
6600 Extended Core Storage.
6800 Extended Core Storage.

.12 Basic Use: . . . . fast auxiliary core storage.

.13 Description

The Extended Core Storage provided for use with the Control Data 6000 Series computer systems offers very fast and comparatively inexpensive auxiliary core storage in capacities of up to 167 million characters. The peak data transfer rate that can be achieved in moving blocks of data between the Extended Core Storage and the Central Memory unit is 400 million characters per second in Control Data 6800 systems.

The primary role of Extended Core Storage in the 6000 Series computer systems is to hold large numbers of scheduled programs and data in readiness for immediate transfer to Central Memory for use by the Central Processor. When Extended Core Storage is included in a 6000 Series system, the multiprogramming capabilities are made even more powerful and efficient than with a basic system. Not only can the large Central Memory hold several programs or segments of programs for alternate execution by the Central Processor, but the Extended Core Storage can exchange the entire contents of Central Memory within a few milliseconds to provide the Central Processor with rapid access to a vast store of programs. The entire 1,310,720 characters contained in a Control Data 6800 Central Memory can be exchanged with the same number of characters stored in Extended Core Storage in 6.5 milliseconds.

The transfer rates are so impressive that Control Data plans to utilize the concept of swapping programs between Extended Core Storage and Central Memory as the heart of its time-sharing system for the 6000 Series. Rather than having a relatively small number of program segments arranged in independent "pages" of Central Memory, Control Data advocates arranging a large number of program segments in Extended Core Storage. The roll-in/roll-out method is then utilized to provide the Central Processor with almost immediate access to any program and to switch programs with little delay when each "time-slice" is completed.

The high data transfer rates are made possible by synchronization of the access and cycle times of the Extended Core Storage with those of Central Memory, and by the use of a special, synchronously-designed data channel to connect these two storage units. Other vital factors in the speed potential of the Extended Core Storage are its parallel access method (capable of accessing either 480 or 960 bits simultaneously) and its division into up to four independent modules or banks, all of which can be accessed simultaneously. Successive data words are stored in different banks so that the maximum number of banks can be concurrently used in the transfer of large blocks of data.

The Extended Core Storage that is provided for use with the Control Data 6400 and 6600 computer systems is physically different from that supplied for use with the 6800 system, although their functions are identical. The 6400's Extended Core Storage is arranged in the form of 16,384 480-bit words per bank, which is equivalent to 131,072 60-bit computer words per bank. Four banks can be arranged in a bay that contains 524,288 60-bit words, and four bays can be joined to form a 2,097,152-word "star." A total of 8 stars of Extended Core Storage (167,772,160 characters) can be accessed by a single 6400 or 6600 computer system, and each 60-bit word is individually addressable.

The cycle time for the Extended Core Storage used with the 6400 and 6600 computer systems is 3.2 microseconds per 480-bit memory-bank word. Therefore, the data transfer rate per bank of 1,310,720 characters is 25 million characters per second. Although a maximum of 128 banks of storage can be connected, only four can be simultaneously accessed by the Central Processor. Thus, the maximum data transfer rate between the Extended Core Storage and Central Memory of a Control Data 6400 and 6600 is 100 million characters per second. Table I presents the capacities and speeds of the 6400/6600 Extended Core Storage and compares these characteristics with those of the faster 6800 Extended Core Storage.

The 6800 Extended Core Storage is organized in banks of 8,192 960-bit words, with a cycle time of 1.6 microseconds. Four memory banks can be grouped in a bay, and a maximum of 2 bays can be supported by a 6800 system, providing a total storage capacity of 20,971,520 characters. The data transfer rate per bank is 100 million characters per second. Since a maximum of four banks are accessed simultaneously, the maximum transfer rate per 6800 computer system is 400 million characters per second.

Data transfers between Extended Core Storage and Central Memory are effected by means of two Central Processor instructions and two central registers. The AO register specifies the initial 17-bit transfer address in Central Memory of a word or block of words, and the XO register specifies the initial 24-bit transfer address in Extended Core Storage. The Read and Write Extended Core instructions transfer data between Extended Core Storage and Central Memory, beginning at the locations specified in the XO and AO registers, respectively. During the transfer of data to or from Extended Core Storage, the Central Memory can be periodically accessed by the Central Processor and the Peripheral and Control Processors.

Extended Core Storage can also be utilized in those 6400 and 6600 computer systems that make use of

TABLE I: EXTENDED CORE STORAGE CHARACTERISTICS

Control Data Computer System	6400 and 6600				6800	
Extended Core Storage Capacities in 60-bit Words*	131,072	262,144	1,048,576	2,097,152	524,288	1,048,576
Number of Characters Accessed per Cycle	80	80	80	80	160	160
Cycle Time, in Microseconds	3.2	3.2	3.2	3.2	1.6	1.6
Number of Memory Banks	1	2	8	16	4	8
Peak Transfer Rate, Millions of Characters per Second	25	50	100	100	400	400

* Larger Extended Core Storage capacities, ranging up to 16,777,216 60-bit words, are available upon request.

.13 Description (Contd.)

the 6411 Augmented Input-Output Buffer and Control device (see Section 260:101). With this configuration, data can be transferred not only between Central Memory and Extended Core Storage, but also between the 6411's Main Memory and Extended Core Storage. The Main Memory of the 6411 can be used to gather programs from remote locations and transfer them to Extended Core Storage for eventual execution by the Central Processor. This configuration seems well-adapted for use in Control Data's approach to time-shared operations.

The transfer of data between Extended Core Storage and the 6411's Main Memory is effected by two instructions in the 6411's Peripheral and Control Processors: Read Program Address and Exchange Jump. These Peripheral Processor instructions normally communicate with the Central Processor, but when used with the Peripheral Processors of the 6411 unit, they are free to take on other meanings because there is no Central Processor in the 6411 subsystem. In configurations that employ a 6411 and Extended Core Storage, the Read Program Address instruction examines the "busy" status of the data channel that connects the Main Memory of the 6411 to the Extended Core Storage. The Exchange Jump instruction in this environment initiates a memory read or write operation and specifies the word count and starting addresses in Main Memory and Extended Core Storage.

The Extended Core Storage has four independent access trunks, enabling it to be shared by up to four Control Data 6000 Series computer systems (or 6411 Augmented Input-Output Buffer and Control devices) for multiprocessing purposes.

As in the other Control Data 6000 Series core storage units, there are no provisions for parity checking in the Extended Core Storage. Software checking schemes are recommended to verify the validity of results whenever such verification is thought to be absolutely essential. Memory protection is provided by the upper and lower boundaries associated with every problem program.

In summary, the Extended Core Storage is capable of transferring blocks of data at rates that are more than ten times faster than those of any commercially-available disc or drum storage device or any previously-announced competitive mass core storage device. The price of the Extended Core Storage is about one-tenth that of the 6000 Series Central Memory units, on a character-for-character basis. (See Section 260:221 for detailed pricing information.) The extremely high data transfer rates of the Extended Core Storage, combined with its comparatively low cost, make the use of this unit worthy of serious consideration by all prospective and current users of the Control Data 6000 Series.

.14 Availability: . . . . ?

.15 First Delivery: . . . . . 1966.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic core.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Bank (6400 and 6600)

480-bit words: . . . . . . 16,384.
Characters: . . . . 1,310,720.

.25 Data Volume per Bank (6800)

960-bit words: . . . . . . 8,192.
Characters: . . . . 1,310,720.

.26 Banks per Physical Unit: . . . . up to 16 per "star."

.27 Interleaving Levels: . . one per bank, to a maximum of four levels.

.28 Access Technique: . . . coincident current.

.29 Potential Transfer Rates

.292 Peak data rates (6400, 6600) —
Cycle time: . . . . . . 3.2 μsec per 480-bit memory-bank word.
Unit of data: . . . . . . 60-bit computer word.
Conversion factor: . . 8 computer words per memory-bank word.
Gain factor: . . . . . . up to 4 banks can be accessed simultaneously.
Data rate: . . . . 2.5 million computer words/sec/bank.
Compound data rate: . . . . up to 10 million words/sec.

Peak data rates (6800) —
Cycle time: . . . . 1.6 μsec per 960-bit memory-bank word.
Unit of data: . . . . . . 60-bit computer word.
Conversion factor: . . 16 computer words per memory-bank word.
Gain factor: . . . . . . up to 4 banks can be accessed simultaneously.
Data rate: . . . . 10 million computer words/sec/bank.
Compound data rate: . up to 40 million words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes: . . . . see table below.

.32 Rules for Combining Modules: . . . . modules of 6400/6600 and 6800 Extended Core Storage cannot be intermixed in the same system.

.4 CONTROLLER: . . . . . no separate controller.

.5 ACCESS TIMING

.52 Simultaneous Operations: . . . . up to 4 memory banks can transfer data simultaneously.

.53 Access Time Parameters and Variations

.531 For uniform access (6400, 6600) —
Access time: . . . . . . 1.6 μsec.
Cycle time: . . . . 3.2 μsec.
For data unit of: . . . 480 bits.

For uniform access (6800) —
Access time: . . . . . . 0.8 μsec.
Cycle time: . . . . 1.6 μsec.
For data unit of: . . . 960 bits.

.6 CHANGEABLE STORAGE: . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size

With Central Memory: . . . . 1 to 131K 60-bit words.

.73 Effective Transfer Rate (60-bit words/sec)

With 6400 and 6600 computer systems: . . 8 million (32K systems). 10 million (65K, 131K systems).

With 6800 computer systems: . . . . 32 million (32K systems). 40 million (65K, 131K systems).

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Receipt of data:	no check.	
Recording of data:	no check.	
Recovery of data:	no check.	
Dispatch of data:	no check.	
Timing conflicts:	not possible.	
Reference to protected area:	program boundary check	data transfer is aborted.

.31 Module and System Sizes

	Minimum Storage			Maximum Storage
Identity:	Bank	Bay	Star	8 Stars
Words (60-bit):	131,072	524,288	2,097,152	16,777,216
Characters:	1.3 million	5.2 million	21 million	168 million
Banks:	1	4	16	128

INTERNAL STORAGE: 6603 DISK FILE

.1 GENERAL

.11 Identity: . . . . Control Data 6603 Disk File.

.12 Basic Use: . . . . auxiliary storage and System Disk.

.13 Description

The Control Data 6603 Disk File is a single-module, high-performance disc storage unit that can be used with Control Data 6000 Series computer systems as the System Disk. The 6603 is a Bryant disc file that uses 14 non-removable discs and is capable of storing up to 80 million 6-bit characters. Parallel accessing of 12 disc surfaces contributes to transfer rates that range between 1.0 and 1.3 million characters per second. Up to eight 6603 Disk Files can be connected to a 6000 Series computer system.

The System Disk is an integral part of every Control Data 6000 Series computer system. Its use is normally directed and regulated exclusively by SIPROS, the 6000 Series operating system, although direct user access to the unit is also possible. The principal functions of the System Disk include the following:

- To accumulate portions of a program's output when the program is being processed periodically, as in a multiprogramming or time-sharing environment;
- To store the input job stack, providing Central Memory and/or Extended Core Storage with quick access to scheduled programs and their data;
- To gather input data from relatively slow input devices, and to transfer this information as complete data sets to core storage for non-interrupted processing;
- To store the results of program compilations when these programs are not scheduled for immediate execution;
- To hold in residence the 6000 Series system library; and
- To provide SIPROS with the generalized services of random-access, intermediate storage.

The Control Data 6607 and 6608 Disk Files (described in the following report section, 260:045) can also be used as the System Disk in a 6000 Series computer system. The 6607 and 6608, which are manufactured by Control Data Corporation, are expected to supersede the Bryant-made 6603 in 6000 Series systems within the near future.

The 6603 Disk File contains 14 discs, each coated on both sides with a magnetic-oxide material. Twenty-four of the twenty-eight disc surfaces are used for recording data, two are used for timing purposes, and two are used for spares. Each disc surface is divided into four concentric zones, and each zone is further divided into 128 concentric recording tracks.

In the outer two zones of each disc surface, the 256 recording tracks are divided into 128 sectors. The 256 recording tracks of the inner two zones are divided into 100 sectors. Physically, each sector on a particular track holds 351 bits of information. Logically, however, a sector spreads over the 12 corresponding tracks of 12 disc surfaces, since these 12 tracks are read and recorded simultaneously. Therefore, a logical sector consists of 351 12-bit words. The first four 12-bit words of each sector are used for synchronization purposes and the last word is used for parity checking, so the data capacity of each sector is 346 twelve-bit words.

Each of the 24 disc recording surfaces is provided with four read-write heads, one per zone, attached to a common arm. Each arm assembly is in turn attached to a common head-positioning axis that moves all of the arms in unison. In any one position of the comb-like multiple-arm access mechanism, approximately 88,500 characters can be read or recorded on the outer zones using the 12-head parallel accessing method. The 6603 Disk File has a total of 8 such 12-head groups, each of which can alternately access 88,500 (outer zones) or 69,200 (inner zones) characters without any arm movement. As each head-group completes its reading or recording operation, a "revolution mark" on the disc is sensed. At this point another head-group can be specified to continue the data transfer operation. As a result, approximately 631,104 characters can be accessed while the access mechanism is in any one position, with head-group switching being performed electronically.

Each of the 24 usable disc surfaces has a storage capacity of approximately 20 million bits of information, spread throughout 58,368 346-bit physical sectors. Since all reading and writing operations transfer 12 bits in parallel, the 6603 Disk File's data word is considered to be 12 bits in length. Each logical sector, consisting of 346 twelve-bit words, is individually addressable. The total data storage capacity of a 6603 Disk File consists of 116,736 addressable sectors that contain 40,390,656 twelve-bit words.

Data records can be of variable length and do not need to coincide with sector boundaries. The 6603's synchronization device inserts four words of zeros at the beginning of each record and a parity word at the end of each record. The 12-bit parity word is read during every read operation and is compared to a newly-generated parity word to ensure the validity of data transfers. However, the Disk File does not automatically regenerate and compare the parity word after a write operation.

The total time required to read or write data consists of the time required to position the access arm to the selected track, the time required to wait for the selected sector on the track, and the time required to transfer the data. Whenever a

.13 Description (Contd.)

different track is selected, a fixed track-positioning delay of 120 milliseconds occurs, allowing any mechanical vibrations to cease before data transmission starts. The discs revolve at a rate of 900 to 950 rpm, or one revolution every 63 to 66 milliseconds, so the average rotational delay is about 33 milliseconds. The total average access time for data accessing that requires arm movement is therefore 153 milliseconds. In situations that do not require head positioning, the significant timing considerations are the time to switch electronically between the eight read-write head-groups (0 to 66 milliseconds), and the rotational delay (0 to 66 milliseconds). Head-group switching time is overlapped with track positioning delay when access arm movement is required.

.14 Availability: . . . . 6 months.

.15 First Delivery: . . . . . 1965.

.16 Reserved Storage

Purpose	Number of locations
Synchronization:	4 words/sector.
Parity:	1 word/sector.
Head-group switching:	351 words/track.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . disc.

.22 Physical Dimensions

.222 Disc —
Diameter: . . . . ?
Thickness or length: . ?
Number on shaft: . . . 14.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 12 Tracks

	Outer Zones	Inner Zones
Words:	44,288	34,600
Characters:	88,576	69,200
Instructions:	44,288	34,600

.26 Bands per Physical Unit: 1,024 800

.27 Interleaving Levels: . . 1 (i.e., no interleaving when reading or recording is performed under control of standard software).

.28 Access Techniques

.281 Reading and recording method: . . . . moving heads.

.282 Type of access —

Description of stage	Possible starting stage
Track positioning: . .	yes.
Head-group selection:	yes.
Sector positioning: . .	yes.
Data transfer:	no.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . . 900 to 950 rpm.
Bit rate per track: . . 700,000 bits/sec/track.

.292 Peak data rates —
Unit of data: . . . . . . word.
Conversion factor: . . 12 bits/word.
Gain factor: . . . . . . 12 tracks/band.
Loss factor: . . . . . . none (no interleaving).
Data rate —
Outer zones: . . . . . 671,051 12-bit words/sec.
Inner zones: . . . . . 524,246 12-bit words/sec.

.3 DATA CAPACITY

.31 Module and System Sizes

Identity: . . . . 6603.
Discs: . . . . 14.
Words (12-bit): . . . . . 40.4 million.
Characters: . . . . 80.8 million.
Instructions: . . . . 40.4 million.
Modules: . . . . 1.

.32 Rules for Combining Modules: . . . . up to eight 6603 Disk Files per system.

.4 CONTROLLER: . . . . . no independent controller.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks —
Heads per stack: . . . 12.
Stacks per system: . . 8.
Stacks per yoke: . . . 8.
Yokes per system: . . 1.

.512 Stack movement: . . . . vertically across the face of 14 recording surfaces.

.513 Stacks that can access any particular location: . . . . 1.

.514 Accessible locations:
By single stack —
With no movement: . outer zones: 44,288 12-bit words.
inner zones: 34,600 12-bit words.
With all movement: . outer zones: 5,668,864 12-bit words.
inner zones: 4,428,800 12-bit words.

By all stacks —
With no movement: . 315,552 words per system.

.52 Simultaneous Operations: . . . . only one operation at a time per 6603 Disk File.

.53 Access Time Parameters and Variations

Stage	Variation	Example
Track positioning:	0 to 120	120 msec.
Head-group selection: (overlapped with track positioning time)	0 to 66 msec	33 msec.
Sector positioning:	0 to 66 msec	33 msec.
Data transfer:	0.5 to 65 msec	0.5 msec.
Total:	0.5 to 251 msec	153.5 msec.

.6 CHANGEABLE STORAGE: . . . . none.

.7 PERFORMANCE

.72 Transfer Load Size: . . 1 to 44,288 12-bit words.

.73 Effective Transfer Rate

With outer zone sectors: . . . . 671,051 12-bit words/sec.
With inner zone sectors: . . . . 524,246 12-bit words/sec (exclusive of access times).

.74 Update Cycle Rate

3.6 references/sec, based on random reference to a record, updating and read-verifying it.

4.0 references/sec, based on random reference to a record, updating it, but not read-verifying.

5.0 references/sec, based on updating and read-verifying a record without head repositioning.

.75 Read-Only Reference Cycle Rate

6.7 references/sec, based on random reference to a record.

15 references/sec, based on reference without head repositioning.

30 references/sec, based on reference without head repositioning or head-group selection.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	prevented by software.	
Receipt of data:	none.	
Recording of data:	generate and record 12-bit parity word.	
Recovery of data:	regenerate and compare parity word	set testable indicator.
Dispatch of data:	none.	

INTERNAL STORAGE: 6607/6608 DISK FILE SYSTEMS

.1 GENERAL

.11 Identity: . . . . 6607 Disk File System.
6608 Disk File System.
807 Disk File.
808 Disk File.

.12 Basic Use: . . . . auxiliary storage and System Disk.

.13 Description

The Control Data 6607 and 6608 Disk File Systems provide large-capacity, high-performance disc storage for the Control Data 6000 Series computer systems. Announced in September 1965, the 6607/6608 Disk Systems offer considerable performance improvements over the 6603 Disk File (described in Section 260:044), and, like the 6603, can be used as System Disk units for the 6000 Series computer systems. The 6607/6608 Disk Systems are manufactured by Control Data Corporation.

The 6607/6608 Disk Files can store up to 168 million characters of information and can transfer data at a rate of 1.67 million characters per second. More than 5 million characters can be accessed in any one position of the access mechanism via electronic head-switching, and the maximum length of time required to position the read/write access arms to any selected data track is 100 milliseconds. Up to eight independently-operating 6607 or 6608 Disk File Systems can be connected to a Control Data 6000 Series computer system.

The Control Data 807/808 Disk Files are the basic components of the 6607/6608 Disk File Systems. In addition to the 807/808 components, the Disk Systems also include built-in dual-channel controllers. The 6607 system consists of an 807 Disk File and a time-shared, dual-channel controller. The 6608 consists of an 808 Disk File, a time-shared, dual-channel controller, and (optionally) a second dual-channel controller to provide simultaneous read/write operations on each half of the 808 Disk File.

The basic structure of the 807 Disk File consists of two vertical shaft assemblies, each controlling 18 non-removable discs. The discs on both shafts are accessed by a single hydraulic actuator assembly that contains two groups (or "combs") of 16 access arms. The access arms move in unison across the surfaces of the discs on each shaft. The requested positioning of one group of access arms is automatically countered by diametrically-opposed movement of the other group of arms in order to minimimize mass imbalance and reduce vibrations.

The 808 Disk File, used exclusively in the 6608 Disk File System, also consists of two vertical shaft assemblies, but with twice the number of discs and two independently-operating actuator arms. Thus, the 808 Disk File can be considered to be two 807 Disk Files, physically and logically integrated into a single, dual-functioning unit.

The 807 Disk File contains 36 aluminum discs, 26 inches in diameter, coated on both sides with a magnetic-oxide material. The 808 Disk File contains 72 discs of the same type. Four 807 discs are not available for recording data, but are used for timing purposes and for spares. Eight 808 discs are similarly unavailable. Therefore, 64 and 128 disc surfaces are available for storing data in the 807 and 808 Disk Files, respectively.

Each disc surface is divided into 192 concentric storage tracks, and each track is segmented into 16 sectors. Up to 2,560 data bits of information can be stored in each sector, or 7.8 million bits per surface. Reading and recording of data are performed simultaneously on 12 corresponding tracks of 12 different disc surfaces, establishing the basic unit of data as a 12-bit word. Thus, each access to a selected disc sector makes available 2,560 twelve-bit words or 5,120 characters.

The newly-designed actuator assembly controls the accessing of data on 64 disc surfaces. Each of the actuator's two combs contains 16 access arms, and each arm contains two 6-head stacks of read-write heads mounted back-to-back in order to provide simultaneous access to corresponding tracks of an upper and lower disc surface. The six-head stack can access six adjacent tracks per surface without requiring arm movement. Since each disc surface contains 192 data tracks, the 6-head access arms, moving in unison, need to move to only 32 discrete positions per surface to provide access to all data stored on each surface of the entire file.

In any one of the 32 positions of the actuator assembly's duplex, reactively-functioning, comb-like access mechanisms, more than 2.625 million characters (5.25 million in the 808 Disk File) are accessible via electronic head-switching. The total storage capacity of the 807 Disk File is approximately 84 million characters. The capacity of the 808 Disk File, which uses twice the number of discs and a second actuator assembly, is approximately 168 million characters.

The 807/808 Disk Files provide fast random access to any part of the file. If the addressed sector is not among the 16.4 or 32.8 thousand sectors that are rotating directly under the read-write heads at any time, repositioning of the access arms is required. In this situation, any 5,120-character sector can be accessed in between 34 and 152.5 milliseconds. Access arm positioning requires from 34 to 100 milliseconds, and the disc rotational delay, at 1140 disc revolutions per minute, is a maximum of 52.5 milliseconds. The comparatively short access arm positioning time is made possible by reducing the number of discrete head positions per track and by minimizing the settling time after arm positioning by means of the self-balancing actuator assembly.

.13 Description (Contd.)

The maximum data recording density on the 807/808 discs is 850 bits per inch. Reading and recording 12 bits in parallel, the 807/808 Disk Files produce data transfer rates of 1.67 million characters per second.

The read-write heads are positioned to "fly" at approximately 0.0004 inch from the disc surface. If for any reason the disc rotational speed drops below a certain level, the read-write heads are automatically retracted.

The smallest record that can be written is the size of one logical sector, or 2,560 12-bit words. If a program calls for fewer words to be written, the remainder of the sector is filled with zeros. After each sector is written, an automatic 12-bit parity word is generated and written as the sector's 2,561st word. Subsequent Disk File read instructions automatically regenerate the parity word and compare it to the original. Parity errors are indicated by setting a specific bit in the status word that the Disk File controller constructs for testing by the 6000 Series Peripheral and Control Processors.

Each 807 Disk File that is used with a Control Data 6000 Series computer system is capable of performing only one read, write, or seek operation at any one time. However, the 808 Disk File can be supplied with an optional controller that permits read/write/seek overlap on each half of the Disk File.

.14 Availability: . . . . ?

.15 First Delivery: . . . . . third quarter, 1966.

.16 Reserved Storage

Purpose	Number of locations
Synchronization:	127 12-bit words.
Parity:	1 12-bit word.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . magnetic discs.

.22 Physical Dimensions

.222 Disc —
Diameter: . . . . 26 inches.
Number on shaft: . . . 36.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Permanence

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . no.

.25 Data Volume per Band of 12 Tracks

Words: . . . . 40,960 12-bit words.
Characters: . . . . 81,920 characters.
Instructions: . . . . 40,960 12-bit instructions.

.26 Bands per Physical Unit: . . . . 192.

.27 Interleaving Levels: . . 1 (i.e., no interleaving).

.28 Access Techniques

.281 Reading and recording method: . . . . moving heads.
.283 Type of access —

Description of stage	Possible starting stage
Access arm positioning:	yes.
Head-group selection:	yes.
Rotational delay:	yes.
Data transfer:	no.

.29 Potential Transfer Rates

.291 Peak bit rates —
Cycling rates: . . . . 1140 rpm.
Bits/inch/track: . . 850 bits/inch maximum.
Bit rate per track: . 833,333 bits/sec/track.
.292 Peak data rates —
Unit of data: . . . . . word.
Conversion factor: . 12 bits/word.
Gain factor: . . . . . 12 tracks/band.
Loss factor: . . . . . none (no interleaving).
Data rate: . . . . . . 833,333 12-bit words/sec.
Compound data rate: . . . . 1,666,667 12-bit words/sec (808 Disk File only).

.3 DATA CAPACITY

.31 Module and System Sizes

	807 File	808 File
Discs:	32	64.
Words (12-bit):	42 million	84 million.
Characters:	84 million	168 million.
Instructions:	42 million	84 million.
Modules:	1	1.

.32 Rules for Combining Modules: . . . . up to eight 807 or 808 Disk Files per system.

.4 CONTROLLER: . . . . controller is an integral part of 6607/6608 Disk File Systems.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks —	807	808
Heads per stack: . .	6	6.
Stacks per system: .	64	128.
Stacks per yoke: . .	64	128.
Yokes per system: .	1	2.

.512 Stack movement: . . . horizontally across the disc surfaces.
.513 Stacks that can access any particular location: . . . . 1.
.514 Accessible locations (by all stacks, with no arm movement): . 2.625 (807) or 5.25 (808) million characters per Disk File.

.52 Simultaneous Operations: . . . . only one operation at a time in the 807 Disk File; two simultaneous operations available with optional equipment in the 808 Disk File.

(Contd.)

.53 Access Time Parameters and Variations

Stage	Variation	Example
Access arm positioning:	0, or 34 to 100 msec	100 msec.
Head-group selection (time is overlapped with arm positioning time):	---	---
Rotational delay:	0 to 52.5 msec	26.3 msec.
Data transfer:	3.0 to 48 msec	3.0 msec.
Total:	3.0 to 200.5 msec	129.3 msec.

.6 CHANGEABLE STORAGE: . . . . none.

.7 PERFORMANCE:

.72 Transfer Load Size: . . 2,560 to 40,956 12-bit words.

.73 Effective Transfer Rate: . . . . 833,333 12-bit words/sec, exclusive of access times.

.74 Update Cycle Rate

5.0 references/second, based on random reference to a record of 2,560 12-bit words, updating it, and read-verifying it.

6.7 references/second, based on random reference to a record of 2,560 12-bit words, updating it, but not read-verifying it.

7.5 references/second, based on updating this record and read-verifying it, but without head repositioning.

.75 Read-Only Reference Cycle Rate

10.4 references/second, based on random reference to a record of 2,560 12-bit words.

34.1 references/second, based on reference to a record of 2,560 12-bit words without head positioning.

.8 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Invalid address:	prevented by software.	
Receipt of data:	none.	
Recording of data:	generate and record 12-bit parity word.	
Recovery of data:	regenerate and compare parity word	set testable indicator.
Dispatch of data:	none.	

INTERNAL STORAGE: 850 SERIES DISK DRIVES

.1 GENERAL

.11 Identity: . . . . 852 Disk Storage Drive.
853 Disk Storage Drive.
854 Disk Storage Drive.

.12 Basic Use: . . . . random-access auxiliary storage.

.13 Description

The Control Data 850 Series Disk Storage Drives, announced in September 1965, provide Control Data 3000 and 6000 Series users with random-access "Disk Pack" storage facilities. On-line data capacities per Disk Storage Drive range from 2 to 8.2 million characters, and access times vary from 30 to 145 milliseconds. The Model 852 Disk Storage Drive uses the same data recording mode as the IBM 1311 Disk Storage Drive, and their respective Disk Packs are functionally interchangeable.

The 852, 853, and 854 Disk Storage Drives each hold a single removable Disk Pack that consists of 6 discs. Ten of the 12 available disc surfaces are used for recording data. There are 100 data tracks on each disc surface in Models 852 and 853, and 200 data tracks on each Model 854 disc surface. The total storage capacity of Model 852 is 2 million or 2.98 million characters. Model 853 can store up to 4.1 million characters, and Model 854, with twice as many data recording tracks as Model 853, can store up to 8.2 million characters. Table I compares the characteristics of the three models of the 850 Series Disk Storage Drives.

Each 850 Series Disk Storage Drive is serviced by a single comb-like access mechanism that moves horizontally between the disc surfaces. Each of the ten access arms that make up the access mechanism contains a single dual-gap read-write head to service all 100 tracks (or 200 in Model 854) of one disc surface. The ten data tracks that can be accessed when the ten-armed access mechanism is in any given position are referred to as a "cylinder." The total number of characters that can be stored per cylinder and accessed by electronic switching, without access arm positioning, is 20,000 characters in Model 852 and 40,960 characters in Models 853 and 854.

When access arm positioning is required to read or record on a selected track, the access time ranges from 30 to 145 milliseconds, assuming that the Direct Seek feature is installed. Without Direct Seek, the access arm moves to the selected track only after first returning to a starting or "home" position, and access times will be significantly longer.

Random record access time is also affected by the rotational delay, or the time required for the addressed record to pass under the read-write head once the proper track has been selected. This rotational delay varies from 0 to 40 milliseconds in the 852 Disk Storage Drive, and from 0 to 25 milliseconds in the 853 and 854 Disk Storage Drives. The total update cycle time to read a randomly-addressed 100-character record, update it, and perform a write-check operation is 159 milliseconds in Model 852. This same random update and check operation can be performed in 120 milliseconds in Models 853 and 854.

The principal performance difference between the 852 and 853 Disk Storage Drives lies in the disc rotational speed. The discs of Model 852 rotate at 1500 rpm, and those of Model 853 rotate at 2400 rpm. The principal difference between the 853 and 854 Disk Storage Drives lies in the storage capacity of each unit's disc surfaces. Model 853's disc surfaces contain 100 data tracks each, whereas Model

TABLE I: CHARACTERISTICS OF CONTROL DATA 850 SERIES DISK STORAGE DRIVES

MODEL NUMBER	852	853	854
Storage Capacity per Pack (millions of characters)	2.0 (Sector Mode) 2.98 (Track Mode)	4.09	8.19
Discs per Pack	6	6	6
Recording Surfaces per Pack	10	10	10
Tracks per Disc Surface	100	100	100
Sectors per Track	20	16	16
Characters per Sector	100	256	256
Characters Stored per Track	2,000 (Sector Mode) 2,980 (Track Mode)	4,096	4,096
Disc Rotation Speed (rpm)	1,500	2,400	2,400
Rotational Delay (msec)	0 to 40	0 to 25	0 to 25
Access Time with Direct Seek (msec)	30 to 145	30 to 145	30 to 145
Data Rate (char/sec)	77,730	208,333	208,333

(Contd.)

.13 Description (Contd.)

854 has 200 data tracks per surface. A total of up to 4.096 million characters can be stored on-line in each 853 Disk Storage Drive, and up to 8.192 million characters in each 854 Disk Storage Drive.

The 852 Disk Storage Drive can store up to 2 million 7-bit characters when recording is performed in the Sector Mode. In this mode, each track is divided into 20 sectors, and each sector holds a 5-character address and up to 100 7-bit alphameric characters of data. When data is recorded in the Full-Track Mode (i.e., with each record occupying a full data track), each track can hold 2,980 seven-bit characters, for a total drive capacity of 2.98 million characters. The 852 Disk Storage Drive records data in the NRZI (Non-Return to Zero) data recording mode. A parity bit is generated and recorded with each character of data.

The 853 and 854 Disk Storage Drives use the "double-frequency" recording technique and record data only in the Sector Mode — never in the Full-Track Mode. Normally each read and write operation transfers a full sector of data (i.e., 256 six-bit characters). However, if reading and recording are selected to be performed in the End of Record Mode, these operations can be terminated prior to the end of the associated sector by means of an End of Record mark. A 16-bit check character is generated with every record that is recorded. This check character is regenerated and compared with the recorded version each time the record is read; unequal comparison results in a data transmission error signal.

.14 Availability: . . . . ?

.15 First Delivery: . . . . . 3rd quarter, 1966.

.16 Reserved Storage: . . . none.

.2 PHYSICAL FORM

.21 Storage Medium: . . . . multiple magnetic discs.

.22 Physical Dimensions

.222 Disc —
Diameter: . . . . 14 inches.
Number on shaft: . . . 6.

.23 Storage Phenomenon: . direction of magnetization.

.24 Recording Performance

.241 Data erasable by instructions: . . . . . . yes.
.242 Data regenerated constantly: . . . . no.
.243 Data volatile: . . . . . . no.
.244 Data permanent: . . . . no.
.245 Storage changeable: . . yes, see Paragraph .6.

.25 Data Volume per Band of 1 Track

	852	853/854
Words	variable	variable.
Characters:	2,000 or 2,980	4,096.
Digits:	2,000 or 2,980	4,096.
Instructions:	variable	variable.
Sectors:	20 or 1	16.

.26 Bands per Physical Unit: . . . . Models 852 and 853: 100 per disc surface. Model 854: 200 per disc surface.

.27 Interleaving Levels: . . 1 (i.e., no interleaving).

.28 Access Techniques

.281 Reading and recording method: . . . . magnetic heads which move horizontally in unison on a comb-like access arm mechanism.

.283 Type of access —

Description of stage	Possible starting stage
Move heads to selected track (cylinder):	if new cylinder is selected.
Wait for beginning of selected track: . .	if same cylinder was previously selected.

.29 Potential Transfer Rates

.291 Peak bit rates —

	Model 852	Models 853/854
Cycling rate: . . .	1500 rpm.	2400 rpm.
Bits/inch/track:	988 bpi max.	1105 bpi max.
Bit rate per track:	699,530 bits/sec/track	1,250,000 bits/sec/track.

.292 Peak data rates —

Unit of data: . . .	character	character.
Conversion factor:	7 bits per character (6 plus parity)	6 bits per character.
Data rate:	77,730 characters per second	208,333 characters per second.

.3 DATA CAPACITY

.31 Module and System Sizes

Model:	852	853	854
Discs:	6	6	6
Tracks:	1,000	1,000	2,000
Cylinders:	100	200	200
Words:	variable	variable	variable
Characters:	2,000,000 or 2,980,000	4,096,000	8,192,000
Modules:	1	1	1

.32 Rules for Combining Modules: . . . . up to 8 Model 852, 853, or 854 Disk Storage Drives can be connected to a basic 6000 Series computer system.

.4 CONTROLLER

.41 Identity: . . . . controller is an integral part of each 852 Disk Storage Drive.
3234 Disk Storage Controller services up to 8 Model 853 and/or 854 Disk Storage Drives.

.5 ACCESS TIMING

.51 Arrangement of Heads

.511 Number of stacks —
Heads per stack: . . . 1.
Stacks per drive: . . . 10.
Stacks per yoke: . . . 10.
Yokes per drive: . . . 1.

.512 Stack movement: . . . . horizontally across disc surface to one of 100 (Models 852 and 853) or 200 (Model 854) tracks.

.513 Stacks that can access any particular location: . . . . . . 1.

.514 Accessible locations:
By single stack —
With no movement: . 1 track.
With all movement: . 100 tracks (852 and 853); 200 tracks (854).
By all stacks —
With no movement: . 10 tracks per drive.

.52 <u>Simultaneous Operations</u>: . . . . a read, write, or seek operation in any Storage Drive can be overlapped with a seek operation in any other Drive. The Seek Overlap feature is standard on all models.

.53 <u>Access Time Parameters and Variations</u>: . . . . see Table II.

.6 <u>CHANGEABLE STORAGE</u>

.61 <u>Cartridges (Disk Packs)</u>

.611 Cartridge capacity —
Model 852: . . . . 2,980,000 characters.
Model 853: . . . . 4,096,000 characters.
Model 854: . . . . 8,192,000 characters.

.612 Cartridges per module: . . . . 1.

.613 Interchangeable: . . . . yes, between all Disk Storage Drives of the same model; Model 852 Disk Packs can also be interchanged with the IBM 1316 Disk Packs used with IBM 1311 Disk Storage Drives.

.62 <u>Loading Convenience</u>

.621 Possible loading —
While computing system is in use: . . . . yes.
While storage system is in use: . . . . yes, if the particular Disk Storage Drive is not being addressed.

.622 Method of loading: . . . operator.

.623 Approximate change time: . . . . 1 minute.

.624 Bulk loading: . . . . . . no; only one cartridge of 6 discs is loaded at any one time.

.7 <u>PERFORMANCE</u>

.72 <u>Transfer Load Size</u>

	852	853/854
Single track:	1 to 2,000 chars.	1 to 4,096 chars.
Cylinder:	up to 20,000 chars.	up to 40,960 chars.

.73 <u>Effective Transfer Rate</u>

Cylinder mode, 1-way transfer: . . . . 69,840 char/sec* 193,750 char/sec*

* Based on random accessing and transferring of one cylinder (see Paragraph .72 above) of data.

.74 <u>Update Cycle Rate</u>

With no overlapping of seek times: . . . . . 6.3 (Model 852) or 8.3 (Models 853/854) references/second.
With maximum overlapping of seek times: 9.8 (Model 852) or 15.8 (Models 853/854) references/second.

Note: Based on random accessing of one 100-character record, and reading, updating, and rereading for checking purposes.

.75 <u>Read-Only Reference Cycle Rate</u>

With no overlapping of seek times: . . . . 12.7 (Model 852) or 14.1 (Models 853/854) references/second.
With maximum overlapping of seek times: . . . . 47.1 (Model 852) or 76.9 (Models 853/854) references/second.

Note: Based on random accessing and reading of one 100-character record, with no updating or rewriting.

.8 <u>ERRORS, CHECKS, AND ACTION</u>

Error	Check or Interlock	Action
Invalid address:	prevented by software.	
Receipt of data:	none.	
Recording of data:	parity, cyclic code	set testable indicator.
Recovery of data:	parity, cyclic code	set testable indicator.
Dispatch of data:	none.	

TABLE II: VARIATIONS IN ACCESS TIME (USING DIRECT SEEK FEATURE)

Stage	Model 852		Models 853 and 854	
	Variation, msec	Average, msec	Variation, msec	Average, msec
Move head to selected track (cylinder):	30 to 145	57.5	30 to 145	57.5
Wait for beginning of selected track:	0 to 40	20.	0 to 25	12.5
Transfer data:	24 per track	24.	23.1 per track	23.1
Total:		101.5		93.1

CENTRAL PROCESSORS

.1 GENERAL

.11 Identity: . . . . 6400 Central Processor;
6600 Central Processor;
6800 Central Processor.

.12 Description

The central processor of a Control Data 6000 Series computer system is the largest and most powerful of the 11 processors included in every system. The central processor should not be confused with the 10 subsidiary Peripheral and Control Processors that are described in the following report section, 260:052. The central processor is a high-speed, parallel-functioning arithmetic, logical, and control device that can effectively share its operations between multiple programs concurrently residing in Central Memory or in the Extended Core Storage.

Among the outstanding features of the 6000 Series central processor are the following:

- Parallel execution of up to 10 arithmetic/logical operations.
- Simultaneous accessing of up to 8 Central Memory locations, providing anticipated instruction access and operand preparation, and resulting in virtually no central processor delays caused by the need to await completion of Central Memory accesses.
- An instruction stack of 8 words (up to 32 instructions), facilitating the look-back operations used in program looping.
- Exchange Jump and Internal Jump facilities to switch control between central processor programs in less than 5 microseconds.

Unlike typical central processors, the Control Data 6000 Series central processor can be almost exclusively engaged in performing high-speed, highly-productive computations. Time-consuming input-output and data manipulation operations can be performed by the 10 Peripheral and Control Processors. If the peripheral processors should become overloaded, the central processor can be utilized to assist in the brute data processing.

Three basic central processors are offered with the 6000 Series — a different processor for use with the 6400, 6600, and 6800 computer systems. The central processors have similar roles in their respective systems and are closely related in their hardware organization. The 6400 and 6600 central processors have the same clock-cycle time of 100 nanoseconds; the ultra-high-speed 6800 central processor has a clock-cycle time of 25 nanoseconds.

The 6400 central processor can optionally function in parallel with another 6400 central processor, providing true multiprocessing facilities that include 12 independently-operating processors (2 central and 10 peripheral). However, the 6400 Central Processor has no instruction stack, nor can it execute more than one instruction at a time.

The 6600 and 6800 central processors feature a high degree of processing simultaneity through the use of an eight-word instruction stack and 10 independent arithmetic-logical units. The result is effective overlapping of instruction access and execution. The principal difference between the 6600 and 6800 central processors lies in internal circuit performance: the 6800 can execute instructions approximately four times faster than the 6600 central processor.

This report section describes the general functional characteristics on the three central processors available with the Control Data 6000 Series. Performance timings are not included in this section, since they vary among the processors. Instead, the central processor performance measurements are included in the Central Processor sections of the the individual subreports on the 6400, 6600, and 6800 computer systems, Sections 263:051, 264:051, and 265:051, respectively.

.121 Central Registers and Instruction Stack

The central processor can be accessed by the Peripheral and Control Processors only through the Central Memory, and all accesses to Central Memory are performed through central registers. Instructions and operands are drawn from registers that are constantly being refilled from Central Memory in order to minimize central processor dependence on or delays from any other parts of the system.

An eight-word instruction stack provides the central processor with the present instruction and the seven previous instruction words. Instruction words from Central Memory enter the bottom of the stack and push up the preceding instructions. Programs that branch back to an instruction in the previous stack registers can be contained entirely within the stack loop, minimizing the time expenditures for repeated accesses to the same instructions. In straight-line programs, only the bottom two stack registers are used, providing effective overlapping of instruction access. (In the 6400 central processor, the two-register sequential buffer or stack is the only instruction stacking mechanism available.)

The 24 high-speed central registers also contribute to the high degree of overlap in instruction preparation and to the consequent speed of instruction execution. These registers act as buffers between the relatively slow Central Memory and the rapid processing units, supplying addresses and operands in anticipation of the central processor's needs. Eight of these registers (B or B-line) are 18-bit index registers, used to increment or decrement the contents of any of the 24 central registers. Eight registers (A) are used as 18-bit address registers, serving to address the five Read Central Memory and two Store Central Memory trunks. Eight 60-bit

.121 Central Registers and Instruction Stack (Contd.)

floating-point registers (X) are used as operand registers, with direct access to and from Central Memory.

Any change in the A registers (caused by the arrival of a new instruction) implicitly causes the corresponding operand registers to be filled with the addressed data from Central Memory, or the results of some computational instruction to be stored in Central Memory. Since there are only eight central registers of each variety, and since the instructions address these registers directly, very short instruction lengths can result. For example, a three-address Add instruction can require only 15 bits, or one-fourth of an instruction word.

Another central processor register, the P or Program Address Register, is an 18-bit counter that holds the address of the current instruction word. It is normally advanced by one when the entire instruction word has been executed. However, branch instructions set the P register to the address of the destination instruction, and the Exchange Jump instruction (see Paragraph .123 below) sets the Program Address register to the first instruction of the next program to be executed within the Central Processor.

.122 Arithmetic Units

The central registers of a Control Data 6000 Series central processor can collectively be considered as a control unit that effectively isolates the operations of the arithmetic unit. It is in this arithmetic unit that all central processor arithmetic and logical operations take place.

The central processor of the 6400 computer system contains a unified three-address arithmetic unit that accepts each instruction in sequence and executes it in the same sequence. Instruction preparation is still overlapped with instruction execution, but only one instruction can be executed at any given time.

By contrast, the central processors of the 6600 and 6800 computer systems utilize an arithmetic unit that consists of 10 fast functional units, each of which can perform computational and logical work concurrently with the others. Included among the independent functional units are two Increment units, two Multiply units, and one of each of the following: Add, Long Add, Divide, Shift, Boolean, and Branch. These functional units will accept and concurrently perform as many instructions as there are appropriate functional units available, provided that there is no logical interdependence between the sequential instructions. The three-address structure of the functional units and the specific design of the 6000 Series instruction repertoire tend to increase the probability of logical independence of consecutive instructions.

When the parallel operations of the multiple functional units are utilized, it is entirely possible that the instruction execution sequence will not follow the order in which the instructions were originally written on the coding sheet. If the execution of an instruction must be delayed because its operands are not immediately available, the next instruction(s) may be executed before or in parallel with the original instruction. A hardware device, called the "scoreboard," monitors each instruction as it enters the instruction stack and maintains a record of the current use of each of the central registers and functional units. The scoreboard determines logical dependencies between instructions and delays the execution of dependent instructions until required operands are made available from the execution of previous instructions. Thus, hardware protection is included to ensure that the automatic resequencing and parallel execution of instructions will not result in errors in logic.

.123 Instruction Format

The Control Data 6000 Series central processors use two instruction formats: a 15-bit and a 30-bit format, which can be intermixed within a 60-bit instruction word. In most 15-bit formats, a 6-bit operation code specifies the functional unit and code, and three 3-bit addresses specify the operand registers where the operands can be found and the result stored. The 30-bit format consists of a 6-bit operation code, two 3-bit register addresses (where one operand can be found and the result stored), and an 18-bit second operand that is used directly. The diagrams below illustrate the two basic instruction formats.

f	m	i	j	k	
3	3	3	3	3	15 bits

f	m	i	j	K	
3	3	3	3	18	30 bits

f: . . . instruction type.
m: . . . operation code.
i: . . . result operand register.
j: . . . operand register or shift count.
k: . . . operand register or shift count.
K: . . . literal operand.

.124 Instruction Repertoire

The central processor of the Control Data 6000 Series has an instruction set which is separate and distinct from that of the Peripheral and Control Processors. The central processor's instruction repertoire contains only 86 instructions, which fall into a mere nine logical classes. For example, the "SET" instruction class consists of 33 instructions that "set" one of the 24 operational registers to some particular value. The value is determined either from the contents of two of the operational registers or from a literal written into the instruction and the contents of one of the operational registers. In all cases, two values are used to determine the resultant final value to be inserted into the designated operational register. (One of the operational registers is permanently set to zero, however, so a programmer can easily use only a single value if he wishes.) The two values can be added together, or one can be subtracted from the other.

The 33 different Set instructions are all written by using the same single-letter mnemonic code S (for Set), followed by three register names (or two register names and a literal) separated by a plus or a minus sign. For example "SA3 B4 + 28" simply means "Set Register A3 to the contents of Register B4 plus 28." Similarly, "SA5 A5-B5" will decrement Register A5 by the contents of Register B5. Because all of the Set instructions use this format and the same one-letter mnemonic code, the programmer will soon view the 33 Set instructions as a single, highly versatile instruction.

(Contd.)

.124 Instruction Repertoire (Contd.)

Other classes of closely related instructions include the 8 Boolean operations, the 12 floating-point operations (add, subtract, multiply, and divide in either single-length unrounded, single-length rounded, or double-length unrounded form) and the 18 jump instructions. This leaves only 15 other instructions that the programmer will need to remember in addition to these four general categories. The surprising simplicity of the Central Processor instruction code has a major effect on the operational efficiency of the Control Data 6000 Series systems, because it makes hand coding relatively easy to learn, easy to check, and easy to revise when necessary.

With such a small instruction repertoire, attention is naturally focused on those instructions which are not present although they might be expected in such expensive systems. In considering these apparent omissions, it is important to consider the limited role of the Central Processor, and the type of work for which the Control Data 6000 Series systems were designed.

Monitoring and executive functions and control of input-output operations are not expected to be performed by the Central Processor; these are functions of the Peripheral Processors exclusively. The predominance of floating-point operations reflects the computational needs of the atomic energy industry, for which the system was originally designed. However, in view of Control Data's promotion of the system for commercial as well as scientific purposes, the absence of fixed-point multiplication and division instructions and of any radix conversion instructions is particularly conspicuous. Another noticeable lack in the instruction set is the absence of any mass data transfer instructions. Two words is the largest possible load that can be transferred during a single operation, and such an operation requires the execution of several Set instructions. Less obvious omissions are some of the more sophisticated instructions present in the slower Control Data 3600 computer — including a very useful off-line search instruction which can search through core memory for either equality or threshold conditions, and which has unusually flexible incrementing capabilities. The provision of such facilities would have increased the cost of the 6000 Series systems, and on balance it was thought more desirable to handle operations such as data moving, searching, and radix conversion through a "brute force" approach which takes advantage of the high speeds of the Central Processors.

In their handling of the 60-bit floating-point operands, the 6000 Series central processors use the concepts of out-of-range numbers and indefinite operands. Special codes permit identification of operands in each of these categories. A number which is out-of-range is simply a number whose binary exponent is greater than 1024 or less than -1024. An out-of-range number is treated as infinity or zero, as appropriate. Operations using out-of-range numbers as operands are specially handled. In some cases the results of such operations can continue to be used (e.g., $\infty + \infty$, which is defined as yielding ∞). In other cases the results must be designated as "indefinite" operands (e.g., $\infty - \infty$, the result of which cannot be guessed). The use of any indefinite operand in an operation makes all the results of that operation indefinite also.

A complete list of the 6000 Series central processor instruction set is presented in Section 260:121 of this report.

.125 Interrupt Facilities

Since the Control Data 6000 Series central processor performs no input-output or system control functions, its interrupt facilities are predictably simple. If an attempt is made to address a Central Memory location that is outside the range of the program being executed, the central processor is interrupted. This control is made possible by means of the memory protection scheme utilized by the central processor and Central Memory (see Section 260:041). Each program in Central Memory has an upper and lower boundary associated with it, and this range cannot be exceeded during the program's execution. During the floating-point arithmetic operations, interrupts also occur if the operands are out-of-range (i.e., exponent overflow) or if erroneous "indefinite" results are developed (see Paragraph .124 above). Interrupt control is normally handled by the executive/monitor routines of SIPROS, the integrated operating system that resides in one of the Peripheral and Control Processors.

The Exchange Jump facility, used by the Peripheral Processors to initiate and exchange programs in the central processor, causes external interruption of the central processor. The Peripheral and Control Processor, under the direction of SIPROS, interrupts the central processor and provides it with the initial address of a 16-word package in Central Memory. The Exchange Jump package contains such information as the initial contents of the 24 central registers, the program's upper and lower boundaries, and the current program address. The central processor enters this information in the appropriate registers and then stores the corresponding information from the interrupted central processor program in the same 16 words of Central Memory. Using the Exchange Jump facility, two programs can be exchanged in the central processor in less than five microseconds. This facility is a key factor in achieving efficient performance in multiprogramming and time-sharing operations.

The Internal Jump instruction, a modified version of the Exchange Jump instruction, enables the central processor to interrupt itself or another central processor and then perform the same program-switching operation as that effected by Exchange Jump. Thus, the central processor has the ability to operate in two states: normal and monitor. The central processor's ability to initiate program switching without resorting to the executive control programs in the Peripheral Processor will considerably increase the efficiency of multiprogramming and time-sharing operations. Both the Internal Jump and Exchange Jump instructions are available in the 6400, 6600, and 6800 central processors.

.126 Inter-Series Compatibility

Control Data states that any program written for and compiled on a specific member of the Control

.126 Inter-Series Compatibility (Contd.)

Data 6000 Series will run on any other member of the Series without prior modifications. The sequence of instruction execution and the instruction execution times may vary between the Control Data 6400, 6600, and 6800 central processors, but the results of the program's operation will be the same.

.13 Availability: . . . . 6400 — 6 months.
6600 — 6 months.
6800 — 1 year.

.14 First Delivery: . . . . . 6400 — 1966.
6600 — 1965.
6800 — 1967.

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add-subtract:	automatic	binary	60 bits
	Multiply:	none.*		
	Divide	none.*		
.212	Floating point —			
	Add-subtract:	automatic	binary	96 & 12 or 48 & 12 bits.
	Multiply:	automatic	binary	96 & 12 or 48 & 12 bits.
	Divide:	automatic	binary	96 & 12 or 48 & 12 bits.
.213	Boolean —			
	AND:	automatic	binary	60 bits.
	Inclusive OR:	automatic	binary	60 bits.
	Exclusive OR:	automatic	binary	60 bits.
.214	Comparison —			
	Numbers:	automatic		18 or 60 bits.
	Absolute:	none.		
	Letters:	automatic		18 or 60 bits.
	Mixed:	automatic		18 or 60 bits.
	Collating sequence:	A-Z, 0-9, blank, +, -, *, /, (,), =, ≠, ., ,.		

.215 Code translation: . . . . . none.
.216 Radix conversion: . . . . none.
.217 Edit format: . . . . only between fixed and floating point formats.
.218 Table look-up: . . . . none.
.219 Others —

	Provision	Size
Binary shift:	automatic	60 bits.
Normalization:	automatic	12 + 48 bits.

.22 Special Cases of Operands

.221 Negative numbers: . . . . one's complement.
.222 Zero: . . . . one form.

.23 Instruction Formats: . . see Paragraph .123, above.

.234 Basic address structure: . . . . 3-address.
.235 Literals —
Arithmetic: . . . . 18 bits.
Comparisons and tests: . . . . 18 bits.
Incrementing modifiers: . . . . 18 bits.
.236 Directly addressed operands —
.2361

Internal storage type	Minimum size	Maximum size	Volume accessible
Registers:	1 18-bit word	2 60 bit-words	24 registers
Core Storage:	1 60-bit word	2 words	131,072 words
Extended Core Storage:	1 60-bit word	131,072 words	16,777,216 words

.2362 Increased address capacity: none.
.237 Address indexing —
.2371 Number of methods: . . one.

* Fixed-point multiply and divide operations can be performed indirectly in the floating-point functional units with the assistance of the pack and shift instructions.

(Contd.)

.2373 Indexing rule: ...... base address field and index field are added to form core address. Indexing is not used to select register addresses. Overflows cause program interrupts.

.2374 Index specification: ... within the instruction.

.2375 Number of potential indexers: .... 8.

.2376 Addresses which can be indexed —

Type of address	Application
Core memory:	selection of operands for later instructions, and storage addresses for instruction results.

.2377 Cumulative indexing: .... not possible.

.2378 Combined index and step: .... yes.

.238 Indirect addressing: .... none.

.239 Stepping —

.2391 Specification of increment: .... in register.

.2392 Increment sign: .... positive or negative.

.2393 Size of increment: ..... 18 bits.

.2394 End value: .... specified in test instruction.

.2395 Combined step and test: .... not available.

.24 Special Processor Storage

.241

Category of storage	Number of locations	Size in bits	Program usage
A registers:	8	18	address storage.
B registers:	8	18	index storage.
X registers:	8	60	operand storage.

.242

Category of storage	Total number of locations	Access time, μsec	Cycle time, μsec
A, B, X Registers:	24	0.1 (6400, 6600) 0.025 (6800)	0.1 (6400, 6600) 0.025 (6800)

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: the instructions are placed in the instruction stack in ordinary sequence; their execution sequence is determined by the availability of the operands and the functional units, as explained in Paragraphs .121 and .122.

.32 Look-Ahead: .... see Paragraphs .121 and .122 for descriptions of the various facilities incorporated to ensure effective utilization of the central processor.

.33 Interruption

.331 Possible causes —

In-out units: ...... no.

In-out controllers: .. no.

Storage access: .... yes.

Processor errors: .. yes.

Other: .... Exchange Jump request from a Peripheral Processor, or Internal Jump request from Central Processor.

.332 Control by routine: ... handled in Peripheral Processor.

.334 Interruption conditions: Peripheral Processor or Central Processor monitor control is enabled.

.335 Interruption process —

Registers saved: ... all operational registers are saved, ready for Exchange Jump or Internal Jump program switching.

Destination: ...... processor waits until program switching is completed and new program is initiated.

.336 Control methods —

Determine cause: ... handled by executive program, with assistance of special hardware diagnostic program where necessary.

.34 Multiprogramming

.341 Method of control: ... Peripheral Processors constantly monitor current central processor program, and prepare further programs. Highest priority program which is ready is immediately instituted as the active program.

.342 Maximum number of programs: .... no limit.

.343 Precedence rules: . . . priority algorithm in Peripheral Processor program.

.344 Program protection —

Storage: . . . . each program can access only one contiguous area of central memory.

Maximum separate units: . . . . no hardware limit.

.35 Multi-sequencing: . . . the sequencing of the central processor is completely independent of the sequencing of the various Peripheral Processors.

.4 PROCESSOR SPEEDS

The performance of each Control Data 6000 Series system, in terms of both basic instruction times and speeds on our standard measures of performance, is shown in the Central Processor section of the appropriate subreport:

Control Data 6400 — Section 263:051
Control Data 6600 — Section 264:051
Control Data 6800 — Section 265:051.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock	Action
Overflow:	check	flag set, result set to maximum value.
Underflow (float-pt):	check	flag set, result set to zero.
Zero divisor:	check	flag set, result set to maximum value.
Invalid data:	not possible.	
Invalid operation:	not possible.	
Arithmetic error:	no check.	
Invalid address:	check	program halt.
Receipt of data:	no check.	
Dispatch of data:	no check.	

PERIPHERAL AND CONTROL PROCESSORS

.1 GENERAL

.11 Identity: . . . . 6400 Peripheral and Control Processor; 6600 Peripheral and Control Processor; 6800 Peripheral and Control Processor.

.12 Description

Every Control Data 6000 Series computer system includes 10 logically independent Peripheral and Control Processors in addition to the high-speed Central Processor described in the preceding report section. Each Peripheral and Control Processor has an associated core storage unit consisting of 4,096 twelve-bit words, and the necessary arithmetic and logical capabilities to enable it to execute independent programs. The Central Processor's program is not delayed in any way by the multiprocessing operations of the 10 Peripheral and Control Processors.

The principal roles of the Peripheral and Control Processors in the 6000 Series computer system can be summarized as follows:

- To control all input-output operations through direct communication with the 12 Data Channels.
- To perform executive and monitor control services for the entire system.
- To direct the buffered overlapping of high-speed disc-file operations.
- To perform "off-line" data transcription operations.
- To serve the program in the Central Processor by performing necessary but time-consuming operations such as file searching and array manipulations.
- To exchange operating programs in the Central Processor in order to ensure that the Central Processor remains productively occupied.
- To perform high-speed block transfers of data to and from the Central Memory.

The Peripheral and Control Processors that are used with the Control Data 6400 and 6600 computer systems have a clock cycle time of 1 microsecond; those used with the 6800 computer system have a clock cycle time of 250 nanoseconds. Data transmission between any of the input-output Data Channels and the memory unit of a Peripheral and Control Processor can proceed at 2 million characters per second in the 6400 and 6600 computer systems, and at 8 million characters per second in the 6800 computer system.

This report section describes the general functional characteristics of the Peripheral and Control Processors. The individual subreports for each computer system in the Control Data 6000 Series contain the processing performance measurements for the Peripheral and Control Processors, as follows:

6400 Peripheral and Control Processors: . . . . Section 263:052.
6600 Peripheral and Control Processors: . . . . Section 264:052.
6800 Peripheral and Control Processors: . . . . Section 265:052.

.121 Multiplexed Instruction Execution

The instructions within the programs of each Peripheral Processor are executed in the normal sequential order. Each of the 10 programs operates from a separate, individual memory unit, and each uses four separate registers within a Register Barrel. A single instruction execution unit, called the Instruction Control device, is shared by the 10 Peripheral and Control Processors, with each processor receiving a turn during every 1-microsecond or 0.25-microsecond cycle. The execution of most instructions requires from two to four cycles or passes through the Instruction Control device.

One instruction from each of the 10 peripheral programs enters the Register Barrel and begins its circular tour to the Instruction Control device. During 90 percent of the instruction cycle, the instruction is being interpreted and prepared for execution. Only 10 percent of the instruction cycle is spent in the Instruction Control device, which actually executes the instruction. This multiplexed arrangement provides each Peripheral Processor with an assurance of executing one instruction or portion of an instruction every 1 microsecond (in the 6400 and 6600 systems) or every 250 nanoseconds (in the 6800 system).

.122 Instruction Format

Peripheral and Control Processor instructions can have a 12-bit or a 24-bit format. The 12-bit format has a 6-bit operation code, F, and a 6-bit operand or operand address, d, as illustrated on the next page. The 24-bit format uses an additional 12-bit quantity, m, to form with d an 18-bit operand or operand address.

These formats provide for 6-bit or 18-bit operands and 6, 12, or 18-bit addresses. The quantities d or dm can be used directly in some instructions as literals. The 6-bit segment d can directly address one of the first 64 addresses in the processor's memory unit, or it can provide an indirect address, the content of which is the address of the desired operand. In order to address any of the 4,096 words of a Peripheral and Control Processor's core storage unit, the quantities m and d (possibly zero) are added together to produce the 12-bit operand address.

.122 Instruction Format (Contd.)

The diagram below illustrates the two basic instruction formats.

12-Bit Format:

F	d
6	6

24-Bit Format:

F	d	m
6	6	12

F: . . . . operation code.
d: . . . . literal, address, or index value.
m: . . . . portion of a literal or address.

.123 Instruction Repertoire

The instruction repertoire of the Peripheral and Control Processors is normally of no concern to the programmer of a Control Data 6000 Series computer system because these processors normally are not programmed by the user. They are usually assigned tasks by SIPROS, the integrated operating system for the 6000 Series. SIPROS controls a sufficiently large number of system routines to provide all input-output, data transcription, and standard system servicing operations.

The programmer generally writes his program for execution by the Central Processor and allows SIPROS to determine when and to what extent the Peripheral and Control Processor programs should be utilized. However, in those cases in which the FORTRAN, COBOL, or ASCENT (Central Processor assembly language) programmer explicitly chooses to perform specific routines in the Peripheral and Control Processors, he can code these routines in-line by means of the ASPER Peripheral Processor assembly language (see Section 260:172).

The Peripheral and Control Processors have an instruction repertoire of 64 instructions, including fixed-point binary addition and subtraction, testing, incrementing, jumps, shifts, and input-output device control. Two additional instructions are included to transmit blocks of data between the peripheral memory units and Central Memory. No instructions are supplied to provide automatic editing, code translation, or radix conversion facilities.

Two instructions can be used by the Peripheral and Control Processors to communicate with the Central Processor. The Exchange Jump instruction, described in Paragraph .124, enables a Peripheral and Control Processor to remove a Central Processor program from operation and to replace it with another program in Central Memory, all in less than 5 microseconds. Another instruction, called Read Program Address, permits the Peripheral and Control Processor to monitor the status of the current Central Processor program. Any delays or program exits within the Central Processor program can then be determined, and another program can be initiated by means of the Exchange Jump instruction.

A complete list of the instruction set for the Control Data 6000 Series Peripheral and Control Processors is presented in Section 260:121.

.124 Interrupt Facilities

Two basic Data Channel conditions can be tested by the Peripheral and Control Processors to assist in the control of input-output operations. Each of the 12 basic Data Channels has an active/inactive flag to signal the testing processor that the channel has been selected for use and is busy with an external device. Each channel also has a full-empty flag to indicate that a word (data or I/O control) is available in the 12-bit data register associated with each Data Channel. A thirteenth Data Channel is used in all 6000 Series systems for communication with a real-time clock that runs continuously and is incremented once every Peripheral Processor clock cycle. The clock's value can be tested at any time by the Peripheral and Control Processors, and can be used to determine program running time or the time of day, as required. None of the above I/O flags or conditions can actually interrupt the Peripheral and Control Processors' programs; these processors must test the flags and indicators, and initiate appropriate action depending on the results of the tests.

The Exchange Jump instruction gives the Peripheral and Control Processors the ability to interrupt the Central Processor and exchange its currently-operating program with another from Central Memory. When each program that is to be executed in the Central Processor is loaded into Central Memory, a 16-word "control package" is loaded with it. Exchange Jump signals the Central Processor to exchange the contents of its registers and other control information with the 16-word control package for the program that has been selected for initiation. The control package includes such information as the initial contents of the eight A and eight X Central Processor registers, the Central Memory reference address of the program, the program execution address (P register), and the Field Length of the program for purposes of memory protection. A complete exchange of Central Processor programs can be performed in less than five microseconds.

.125 Software Assignments

The Peripheral and Control Processors are normally assigned programs by SIPROS, the operating system for the Control Data 6000 Series, according to demands within users' programs and requirements of the system's supervision. Two of the Peripheral and Control Processors are permanently assigned to system control activities, and two additional Peripheral Processors are dedicated for use by the system whenever disc file input-output operations occur. The remaining Peripheral Processors, called Pool Processors, are available for performing any tasks assigned them by SIPROS in service of the Central Processor program, the programs in the other Peripheral and Control Processors, and the routines of SIPROS itself. Table I shows the typical assignments of Peripheral and Control Processors within a Control Data 6000 Series system. The Executive/Monitor routines and other services of SIPROS are described in Section 260:191 of this report.

(Contd.)

TABLE I: ALLOCATION OF PERIPHERAL PROCESSORS

PERIPHERAL PROCESSOR (PP)	DUTIES
1	Executive & Monitor PP; this processor is permanently dedicated.
2	Disk Executive PP; this processor is permanently dedicated.
3	Primary Disk Slave PP; this unit is dedicated whenever there are any disk requests.
4	Secondary Disk Slave PP; this unit is dedicated whenever there are any disk requests.
5-10	Pool PP's; these units are available for other system operations, off-line transcriptions, and internal operations, as stipulated in user's program.

.13 Availability: . . . . 6 months.

.14 First Delivery: . . . . . 1965 (with 6600 system).

.2 PROCESSING FACILITIES

.21 Operations and Operands

	Operation and Variation	Provision	Radix	Size
.211	Fixed point —			
	Add/subtract:	automatic	binary	12 bits.
	Multiply:	none.		
	Divide:	none.		
.212	Floating point:	none.		
.213	Boolean —			
	AND:	automatic	binary	12 bits.
	Inclusive OR:	automatic	binary	12 bits.
	Exclusive OR:	automatic	binary	12 bits.

.214 Comparison: . . . . no automatic facilities.
.215 Code translation: . . . . none.
.216 Radix conversion: . . . none.
.217 Edit format: . . . . none.
.218 Table lookup: . . . . . . none.

.22 Special Cases of Operands

.221 Negative numbers: . . . one's complement.
.222 Zero: . . . . two forms; negative zero is considered non-zero in tests for zero.
.223 Operand size determination: . . . . . determined by the instruction requirements.

.23 Instruction Formats: . see Paragraph .122.

.234 Basic address structure: . . . . one-address.
.235 Literals —
Arithmetic: . . . . 18 bits.
Comparisons and tests: . . . . 18 bits.
Incrementing modifiers: . . . . . . 6 bits.

.236 Directly addressed operands —
Internal storage type: . . . . Peripheral Core Storage.
Minimum size: . . . . 12-bit word.
Maximum size: . . . . 12-bit word.
Volume accessible: . 4,096 words.
Increased address capacity: . . . . use of A register to hold address makes all of Central Memory accessible.
.237 Address indexing: . . . none as such; address increment values can be included within an instruction.
.238 Indirect addressing: . . specified in operation code; not recursive.
.239 Stepping: . . . . any 12-bit word can be stepped by +1 or -1.

.24 Special Processor Storage

Category of storage	Size in bits	Program usage
A Register:	18	adder in each processor.
P and Q Registers:	12	program addressing and incrementing operations.
K Register:	9	operation control.

.3 SEQUENCE CONTROL FEATURES

.31 Instruction Sequencing: . . . . see Paragraph .121.

.32 Look-Ahead: . . . . none.

.33 Interruption: . . . . none; see Paragraph .124.

.34 Multiprogramming: . . none; i.e., only one program at a time per Peripheral Processor.

.35 Multi-sequencing: . . . achieved through assignment, by either SIPROS or the programmer, of appropriate portions of user programs to individual Peripheral and Control Processors.

.4 PROCESSOR SPEEDS

The performance of the Control Data 6000 Series Peripheral and Control Processors, in terms of both their basic instruction times and speeds on our standard measures of performance, is shown in the appropriate subreport section for each 6000 Series computer system:

6400 Peripheral and Control Processors: . Section 263:052.
6600 Peripheral and Control Processors: . Section 264:052.
6800 Peripheral and Control Processors: . Section 265:052.

.5 ERRORS, CHECKS, AND ACTION

Error	Check or Interlock
Overflow:	no check.
Invalid data:	not possible.
Invalid operation:	not possible.
Arithmetic error:	no check.
Invalid address:	no check.
Receipt of data:	no check.
Dispatch of data:	no check.

CONSOLES: 6602 DISPLAY CONSOLE

.1 GENERAL

.11 Identity: . . . . 6602 Display Console.

.12 Associated Units: . . . . none.

.13 Description

The 6602 Display Console is an essential unit in every Control Data 6000 Series computer system. It consists of two cathode-ray display units and a manual keyboard, providing communication capabilities between the system operator and the SIPROS operating system, which, in turn, can communicate with every device in the computer system complex.

The 6602 Display Console is connected to the computer system by means of a permanently-assigned Data Channel. It therefore functions in much the same way as any input-output subsystem. Additional Display Consoles can be added if desired, but a Data Channel must be reserved for the use of each Display Console that is added.

The operator enters information into the system through the 50 alphanumeric keys on the Display Console's keyboard. This keyboard is used to initiate a control program in one of the Peripheral and Control Processors. The control program examines the keyboard input, extracts requested data from various parts of the system, formats this data, and displays it on one of the cathode-ray display screens. The keyboard input itself and system directives to the operator are usually presented on one display screen, and status information concerning the current problem program and other concurrently-running programs is displayed on the other screen.

The 6602 Display Console does not have the capability to display automatically the contents of any of the registers or memory locations, but equivalent functions can be performed by means of the SIPROS control program in one of the Peripheral and Control Processors. According to the data entered manually via the Display Console's keyboard, the control program can also alter the contents of the Central Memory and the main registers, and can interrupt, step, and/or terminate a program in the Central Processor.

The use of multiple 6602 Display Consoles can be controlled by a single Peripheral and Control Processor. This usage could conceivably reduce system idle time by allowing the simultaneous debugging and monitoring of a number of unrelated problems that are currently being multiprogrammed in the system.

.14 Availability: . . . . 6 months.

.15 First Delivery: . . . . . 1965.

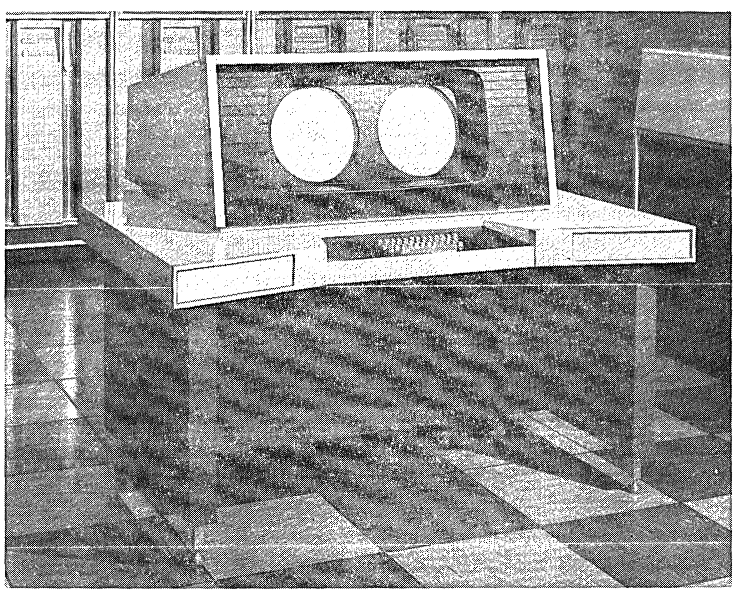


Figure 1: View of 6602 Display Console

CONSOLES: 6060 REMOTE CALCULATOR

.1 GENERAL

.11 Identity: . . . . 6060 Remote Calculator.

.12 Associated Units: . . . . 6677 Multiplexor.
310 Acoustic Coupler or Bell System 103A Data Set.

.13 Description

The Control Data 6060 Remote Calculator is a desk-type electronic calculator that permits users in remote locations to utilize the mathematical processing capabilities of a large-scale computer center. Using the Remote Calculator, the operator simply keys in his problems in standard FORTRAN-like mathematical notation and calls for a display of the solution. His statements are transmitted to the computer center over voice-grade telephone lines.

The 6060 Remote Calculator is a portable device, weighing approximately 40 pounds, that can be used wherever there is a normal telephone hand-set. After the computer center has been called, the telephone hand-piece is placed on a Control Data 310 Acoustic Coupler which connects to the Remote Calculator. Remote operations can begin at once. Communication between the Remote Calculator and the computer center can alternatively be established via a Bell System 103A Data Set.

The 6060 Remote Calculator's interface at the computation center is the Control Data 6677 Multiplexor. Up to 128 Remote Calculators can be connected to each 6677 Multiplexor, and up to four Multiplexors can be connected to one Peripheral and Control Processor through the standard input-output Data Channels.

When requests for specific mathematical functions and procedures are entered at the Remote Calculator and transmitted to an assigned Peripheral and Control Processor, a resident control program, REMCOP, translates and monitors these requests and enters the desired programs into the Central Processor's work queue. As soon as the problem has been solved, REMCOP transmits the solution to the Remote Calculator for display.

The 6060 Remote Calculator consists of an illuminated 12-digit decimal display panel and five basic groups of keys spread over the inclined surface of the keyboard. The display panel is used to view the problem statement as it is keyed in, assisting in the correction of keyboard errors. The display panel also presents the computer system's solution to the mathematical problem.

The data entry section of the keyboard permits direct entry of numeric values and mathematical operation symbols. The "variables" keys provide the facility for attaching alphabetic variable names to user-provided values for use in the problem statements. A third group of keys provides 32 standard mathematical functions that can be called for to assist in obtaining the desired solution. The variety of keyboard functions can be altered to meet the specific needs of each user. The status keys provide basic communication ability with the Control Data 6000 system and also serve as status illuminators. One of these keys also provides access to any named mathematical function in the central computer's memory. The fifth group of keys controls the execution and display of the computational statements and solutions.

First deliveries of the 6060 Remote Calculator are scheduled for 1966. No details are available to date concerning the demand on the Central Processor caused by Remote Calculator operations.

CONSOLES: 6090 ENTRY/DISPLAY CONSOLE

.1 GENERAL

.11 Identity: . . . . 6090 Entry/Display Console (formerly Model dd12 Remote Data Display).

.12 Associated Units: . . . . Model 6090 Central Control Unit.
Model 6678 Multiplexor.

.13 Description

The Control Data 6090 Entry/Display Console is the basic component of a high-speed data entry and retrieval system for the Control Data 6000 Series. The 6090 uses a 14-inch rectangular cathode-ray tube to display both the entered and retrieved information. A standard typewriter-styled keyboard is used to enter requests for data. The Entry/Display Console system can be augmented by a 75-card-per-minute card reader and/or a 100-line-per-minute line printer. The printer can provide hard-copy records of the data requests and the retrieved information. The 6090 Entry/Display Console is normally used as a remote device, communicating with the central computer over voice-grade telephone lines. Up to 64 Entry/Display Consoles can be multiplexed into a single 6000 Series Data Channel by means of a Model 6678 Multiplexor.

The 6090 Entry/Display Console displays up to 1,000 symbols on a 14-inch rectangular screen. The console is available in two models: Model 6090-1, which displays 10 lines of 50 symbols, and Model 6090-2, which displays 20 lines of 50 symbols. The symbol repertoire includes the upper case alphabet, the numerals 0 through 9, the period, comma, semicolon, and several other special characters.

Data is entered on the Entry/Display Console keyboard, where it is converted into 6-bit characters by the 6090 Central Control Unit. The Central Control Unit then generates the display of this information and transmits it to the computer center. The display of information retrieved from the computer and transmitted over standard telephone lines is also controlled by the Central Control Unit.

Data transfers use the 6-bit character as the basic unit of information. The transmission of these characters is protected by the automatic generation and validation of a parity bit for each character.

As announced, the 6090 Entry/Display system is general in its design and can be modified to suit specific requirements.

No details are available to date concerning the software support available for use with the 6090 Entry/Display Consoles. However, it is known that this software will be integrated with the SIPROS software package.

The 6090 is manufactured by Control Data Corporation.

.14 Availability: . . . . 1 year.

.15 First Delivery: . . . . . December 1966.

INPUT-OUTPUT: 405 CARD READER

.1 GENERAL

.11 Identity: . . . . 405 Card Reader.
3248 Card Reader Controller.
3447 Card Reader Controller.
3649 Card Reader Controller.

.12 Description

The Control Data 405 Card Reader is a fast, asynchronous photoelectric reader that operates at 1,200 cards per minute when reading full 80-column cards, and at up to 1,600 cards per minute with 51-column stub cards. The input hopper can hold 4,000 cards. Two output stackers are provided: one main stacker which can hold 4,000 cards, and a reject stacker which can hold 240 cards. The cards are turned individually as they are being read so that the card deck in the output stacker is in exactly the same order as it was before being read.

The card read operation proceeds serially, column-by-column. Two separate photoelectric read stations read each column, and the two readings are checked within the card reader before the column image is forwarded to the card reader controller. Conversion from Hollerith to BCD code is normally executed automatically on all cards which do not have positions 5 and 7 punched in column 1. The conversion can, however, be inhibited by program where desirable.

There are three different Card Reader Controllers. The controllers differ in their buffering provisions and in the number of data channels which can be connected to each controller. The available controller models and their characteristics are:

Model 3248: unbuffered, one data channel connection.
Model 3447: full-card buffer, one data channel connection.
Model 3649: full-card buffer, two data channel connections.

The Card Reader Controllers intervene between the 6681 Data Channel Converter and the card reader itself. The Data Channel Converter connects to one of the 12 6000 Series Data Channels, which, in turn, communicates with one of the 10 Peripheral Processors. The program facilities available with the Control Data 405 Card Reader do not differ significantly when different controllers are used, except that where the controller can be physically connected to two data channels, it is possible to switch one card reader between the two computer systems by connecting the two channels to different systems.

A single card read instruction defines an area in core storage which is to be filled with data read by the card reader. As many cards as are necessary to fill this area are read in under the supervision of a card reader controller, without further program intervention being necessary.

Data Channel control flags can be set when the card reader becomes available, when a card read operation is successfully completed, or when for some reason a card read operation ends without being successfully completed. The Peripheral Processor program can test all of these conditions.

In addition, status indicators show: whether the unit is currently able to respond to an instruction; which interrupt conditions are presently activated; whether the card presently being read is a binary card; whether a card jam, empty input hopper, or full output hopper condition is present; whether a card read error has been noted; and whether the operator has set a switch on the reader indicating that the last card of the card file being read is physically in the card reader.

Each card reader must have its own individual card reader controller, so the number of card readers which can be connected to a computer system is related to the number of data channels and the number of selectable positions on each data channel.

The card reading operation does not delay the Central Processor in any way. However, its operation does place a small load upon the Peripheral Processor that controls the card reading. Since the amount of this delay varies with each member of the Control Data 6000 Series, it is presented in the Simultaneous Operations section of the subreport on each system.

.13 Availability: . . . . 4 months.

.14 First Delivery: . . . . . 1963.

INPUT-OUTPUT: CARD PUNCHES

.1 GENERAL

.11 Identity: . . . . 415 Card Punch.
IBM 523 Card Punch.
IBM 544 Card Punch.
3245 Card Punch Controller.
3446 Card Punch Controller.
3644 Card Punch Controller.

.12 Description

A Control Data 415 Card Punch can be connected to any Control Data 6000 Series computer through a Card Punch Controller. The punch operates at 250 cards per minute and uses a row-by-row punching technique. The punched data is then read at a post-punch read station, which counts the number of holes in the card. Subsequent to the post-punch read station, a card can be offset in the output stacker so that the operator can take any necessary action to remove mispunched cards from the card files.

IBM 523 or 544 Card Punches can be used in place of the Control Data 415 Card Punch. These IBM card punches operate at 100 and 250 cards per minute, respectively, and are functionally equivalent to the Control Data 415 except that they have no provision for offsetting mispunched cards.

There are three different Card Punch Controllers, any one of which can control one card punch unit. The controllers differ in their buffering provisions and in the number of data channels which can be connected. The available controller models and their major characteristics are as follows:

Model 3245:	unbuffered	one data channel connection.
Model 3446:	full-card buffer	one data channel connection.
Model 3644:	full-card buffer	two data channel connections.

The Card Punch Controllers intervene between the 6681 Data Channel Converter and the card punch itself. The Data Channel Converter connects to one of the 12 6000 Series Data Channels, which, in turn, communicates with one of the 10 Peripheral Processors. The available program facilities differ depending on which controller is used. The differences in program facilities are:

- Error Checking: Where the controller does not have a full-card buffer, the hole count reported by the post-punch read station cannot be used because no equivalent hole-count of the card image exists; therefore, no comparison between the two counts can be made.
- Card Punch Coding: Where the controller does not contain a full-card buffer, the computer must provide the data in exactly the form in which it is to be punched.

  Where the controller does contain a full-card buffer, the data can be supplied in BCD column-by-column format and automatically "turned around" in the buffer and converted to the row-by-row format required by the card punch without any program supervision. At the same time, automatic conversion from internal BCD to Hollerith coding can occur if desired.
- Switching Between Computer Systems: Where the controller can be physically connected to two data channels, it is possible to switch the card punch unit from one computer system to the other by connecting the two data channels to different computer systems and using either channel as required. Special instructions are available to reserve the punch for one system at a time, to allow for controlled operation.

A single card punch instruction defines an area in core storage whose contents are to be punched out. As many cards as are needed to accommodate all of the data in the designated area will be punched in response to the instruction.

Data Channel control flags can be set when the card punch becomes available, when an operation is successfully completed, or when for some reason an operation ends without being successfully completed. In addition, status indicators show whether the unit is currently able to respond to an instruction, what interrupt conditions are presently activated, and whether there has been a failure to feed a card.

Each card punch must have its own individual controller, so the number of card punches that can be connected to a computer system is related to the number of data channels and the number of selectable positions on each data channel.

The card punching operation does not delay the Central Processor in any way. However, its operation does place a small load upon the Peripheral Processor that controls the card punching. Since the amount of this delay varies with each member of the Control Data 6000 Series, it is presented in the Simultaneous Operations section of the subreport on each system.

.13 Availability: . . . . 4 months.

.14 First Delivery: . . . . . December 1964.

INPUT-OUTPUT: PAPER TAPE READER/PUNCHES

.1 GENERAL

.11 Identity: . . . . 3691 Paper Tape Reader/Punch.
3694 Paper Tape Reader/Punch.

.12 Description

.121 3691 Paper Tape Reader/Punch

The 3691 Paper Tape Reader/Punch is a free-standing unit which in its normal version is 36 inches high, 28 inches deep, and nearly 48 inches wide. A "ruggedized" version, built to withstand adverse physical conditions, has different dimensions, which are summarized in the Physical Characteristics section of this Computer System Report, on page 260:211.100.

The 3691 contains logically-separate reading and punching sub-units and a single data channel connection for their joint use. The single data channel connection makes it impossible to run the reader and the punch concurrently. Spooling facilities are not provided.

The Paper Tape Reader operates at a peak speed of 350 characters per second, in the forward direction only. A Control Data Model 350 photoelectric reader is currently being used.

The Paper Tape Punch is supplied by the National Cash Register Company, and operated at a rated speed of 110 characters per second.

Five, seven, or eight-level paper tape can be used by either unit; a manual switch selection and tape width adjustment are required when a different type of paper tape is mounted. There are no provisions for automatically checking the parity of the characters on the paper tape itself, and any required checking or preparation of parity-checked characters must be handled by the program. Each tape character can be read into, or punched from, a separate computer word location; or, alternatively, a number of characters can be packed into a single word. In the packed format, a 12-bit peripheral computer word stores either two 5-bit characters or one 7-bit or 8-bit character. Conversion to or from the appropriate internal code must be accomplished by programming.

Data channel control flags are set when the unit becomes available, when an operation ends successfully, or when for some reason an operation ends without being successfully completed. In addition, status indicators show whether the unit is ready to respond to an instruction, whether the punch tape supply is low, and whether the punch or the reader unit was last connected to the data channel.

.122 3694 Paper Tape Reader/Punch

The 3694 Paper Tape Reader/Punch is a free-standing unit, about 60 inches high, 24 inches deep, and 42 inches wide. A large proportion of the total space is taken up by the spooling facilities which are a feature of this unit. Two separate data channels can be connected to the self-contained control mechanism within the 3694 Paper Tape Reader/Punch, so that concurrent paper tape reading and punching can take place.

The Paper Tape Reader operates at a peak speed of 1,000 characters per second, using standard paper or plastic tape with fully-punched holes. Reading operates photoelectrically, in either the forward or reverse direction. Control Data is currently using a Digitronics Corporation paper tape reader for this unit.

The Paper Tape Punch is supplied by the National Cash Register Corporation, and operates at a rated speed of 110 characters per second.

Five, seven, or eight-level paper tape can be used by either unit; a manual switch selection and tape width adjustment are necessary when a different type of paper tape is mounted. Character parity can be optionally used on both reading and punching, under program control. Each tape character can be read into, or punched from, a separate computer word location; or, alternatively, a packed format can be used. In the packed format, a 12-bit peripheral computer word stores either two 5-bit characters or one 7-bit or 8-bit character. Conversion to or from the appropriate internal code must be accomplished by programming.

Data channel control flags are set when the unit becomes available, when an operation ends successfully, or when for some reason an operation ends without being successfully completed.

.123 Processor Demands

The paper tape reading and punching operations do not place any load on the Central Processor. However, these operations do place a small load on the Peripheral Processor that controls the paper tape reading and/or punching. Since the size of this demand, or "interference," varies with each member of the Control Data 6000 Series, it is presented in the Simultaneous Operations section of the subreport on each system.

.13 Availability: . . . . 6 months.

.14 First Delivery

3691 Paper Tape Reader/Punch: . . . . 1963.
3694 Paper Tape Reader/Punch: . . . . 1964.

INPUT-OUTPUT: 3152 LINE PRINTER

.1 GENERAL

.11 Identity: . . . . 3152 Line Printer.

.12 Description

The Control Data 3152 Line Printer operates at up to 150 single-spaced alphanumeric lines per minute. It contains its own control unit, which is connected to one channel via the 6681 Data Channel Converter, and a 120-character line buffer. The 3152 is a drum printer; it normally uses a 63-character drum, although alternative drums are available. The drum revolution time is 400 milliseconds, and an infinite clutch is used so that asynchronous printing is possible. Paper control is handled either by the program directly, or by a combination of the program and a 6-level format tape. Skipping over non-printed areas takes place at approximately 100 line-spaces per second. The effective speed of the 3152 Printer, including allowances for paper advance, is summarized in Table I.

Program facilities include printing with single or double spacing, page ejection, and automatic advancing to the last line of a page. In conjunction with the 132-position, 6-level format loop which is mounted by the operator before printing starts, the program can instruct the paper to be positioned at the line position corresponding to the next punched hole in the specified channel of the format tape. All paper-positioning instructions can take place either before or after printing, as the program directs.

Data channel control flags can be set when the printer becomes available, when an operation is successfully completed, or when for some reason an operation ends without being successfully completed. In addition, status indicators show whether the printer is ready to respond to an instruction, whether the paper supply is exhausted, or whether the printed form is positioned at the last line of the page.

Printing and spacing operations do not delay the Central Processor in any way. However, these operations do place a small load on the Peripheral Processor that controls them. Since the amount of this delay varies with each member of the Control Data 6000 Series, it is presented in the Simultaneous Operations section of the subreport on each 6000 Series computer system.

The 3152 Printer is manufactured by Control Data Corporation.

.13 Availability: . . . . 4 months.

.14 First Delivery: . . . . . June 1963.

TABLE I: EFFECTIVE SPEED OF THE CONTROL DATA 3152 PRINTER

Lines Advanced per Line Printed	Printed Lines per Minute Using AUERBACH Standard Character Set*
1	150
2	150
3	150
4	150
5	150
6 (1 inch)	150
12 (2 inches)	118
18 (3 inches)	108
24 (4 inches)	100
30 (5 inches)	90

* 0-9, A-Z, minus, comma, period, dollar sign.

INPUT-OUTPUT: IBM 1403 PRINTER

.1 GENERAL

.11 Identity: . . . . IBM 1403 Printer, Models 2 and 3.
Control Data Line Printer Controller, Model 3258.

.12 Description

Either Model 2 or Model 3 of the IBM 1403 Printer can be connected to a Control Data 6000 Series computer system by means of a Model 3258 Line Printer Controller. A separate controller is required for each printer which is to be connected to the computer system. Up to 8 controllers can be connected to each 6681 Data Channel Converter.

The IBM 1403 Model 2 operates at a peak speed of 600 lines per minute and uses a horizontal-chain printing mechanism. The 1403 Model 2 is described in detail in the IBM 1401 Computer System Report, on page 401:081.100. The newer Model 3 can operate at 1,100 alphanumeric lines per minute, using a train of type slugs which move through a horizontal channel. The 1403 Model 3 is described in detail in the IBM 1410 Computer System Report, on page 402:082.100.

Data channel control flags can be set when the printer becomes available, when an operation is successfully completed, or when for some reason an operation is ended without being successfully completed. In addition, status indicators show whether the printer is available to respond to an instruction and whether the paper supply is exhausted.

Printing operations do not delay the Central Processor in any way. However, these operations do place a small load on the Peripheral Processor that controls them. Since the amount of this delay varies with each member of the Control Data 6000 Series, it is presented in the Simultaneous Operations section of the subreport on each 6000 Series computer system.

.13 Availability: . . . . ?

.14 First Delivery: . . . . . October 1964 (with Control Data computer system).

INPUT-OUTPUT: 501 AND 505 LINE PRINTERS

.1 GENERAL

.11 Identity: . . . . 501 Line Printer.
505 Line Printer.
3256 Line Printer Controller.
3659 Line Printer Controller.

.12 Description

The Control Data 501 and 505 Line Printers operate at up to 1,000 and 500 single-spaced alphanumeric lines per minute, respectively. Except for their operating speeds, the two units are functionally identical. Each printer contains its own 136-character line buffer and can be connected to a 6000 Series computer system through either the 3256 or 3259 Controller. Up to 8 of these controllers can be connected to each 6681 Data Channel Converter. The 3659 Controller has two channel connections, permitting two computer systems to share its use.

Physically, the printer is enclosed in a four-foot-high cabinet, similar to those used for peripheral control equipment. The cabinet has semi-translucent front panels, through which the operator can observe the printing operation. The use of the cabinet reduces the noise level during printing.

Both the 501 and 505 are drum printers, and both normally employ a 63-character drum, although alternative drums are available. The drum revolution time is 60 milliseconds on the 501 and 120 milliseconds on the 505; an asynchronous clutch is used so that printing of a line can be initiated at any time.

Paper control is handled by the program, either directly or in conjunction with the 6-level format tape. Skipping over non-printed areas takes place at 150 line-spaces per second. The effective speeds of both printers, including allowances for paper advance, are summarized in Table I.

Program facilities include printing with single or double spacing, page ejection, and an automatic advance to the last line of a page. In conjunction with the 132-position, 6-level format loop which is mounted by the operator before printing starts, the program can instruct the paper to be positioned at the line position corresponding to the next hole punched in the specified channel of the format tape. All paper-positioning instructions can take place either before or after printing, as the program directs.

Data Channel control flags can be set when the printer becomes available, when an operation is successfully completed, or when for some reason an operation ends without being successfully completed.

In addition, status indicators show whether the printer is available to respond to an instruction, whether the paper supply is exhausted or the paper torn, or whether the printed form is currently positioned at the last line of the page.

Printing operations do not delay the Central Processor in any way. However, these operations do place a small load on the Peripheral Processor that controls them. Since the amount of this delay varies with each member of the Control Data 6000 Series, it is presented in the Simultaneous Operations section of the subreport on each 6000 Series computer system.

.13 Availability: . . . . 4 months.

.14 First Delivery

501 Printer: . . . . June 1964.
505 Printer: . . . . Spring 1965.

TABLE I: EFFECTIVE SPEEDS OF THE CONTROL DATA 501 AND 505 PRINTERS

Lines Advanced per Line Printed	Printed Lines per Minute Using AUERBACH Standard Character Set*	
	501 Printer	505 Printer
1	1,000	500
2	750	500
3	714	500
4	667	400
5	600	375
6 (1 inch)	571	375
12 (2 inches)	416	300
18 (3 inches)	333	250
24 (4 inches)	267	215
30 (5 inches)	227	187

* 0-9, A-Z, minus, comma, period, dollar sign

INPUT-OUTPUT: 600 SERIES 7-TRACK MAGNETIC TAPE UNITS

.1 GENERAL

.11 Identity: . . . . Control Data 601 through 607 Magnetic Tape Units and associated Magnetic Tape Controllers.

.12 Description

The Control Data 600 Series of 7-track magnetic tape units offers packing densities of 200, 556, or 800 characters per inch and tape speeds of 37.5, 75, or 150 inches per second. The 7-track tape units record one parity bit and six data bits in each tape row. These units, which are compatible with the IBM 729 Magnetic Tape Units and other equivalent units, are described in this section and summarized in Table I. The 9-track units, which record eight data bits and one parity bit in each tape row and are compatible with the IBM 2400 Series Magnetic Tape Units used in the IBM System/360, are described in the next section of this Computer System Report, on page 260:092.100. Compatibility between the two groups of units is limited to their mutual use of one-half-inch magnetic tape reels as a recording medium, and to the possible modification of 9-track units so that they can read or write 7-track magnetic tape instead of (not as well as) 9-track magnetic tape.

The peak data transfer rates of the 7-track magnetic tape units vary from 20,850 to 120,000 characters per second, depending upon which specific unit is in use. The Central Processor is not delayed in any way during data transmissions to and from the magnetic tape units, but a small demand is placed on the memory of the Peripheral Processor that controls these operations. Since the amount of this delay varies with each member of the Control Data 6000 Series, it is presented in the Simultaneous Operations section of the subreport on each 6000 Series computer system.

The effective data transfer rates are controlled by the time taken to pass over the inter-block gap and by the length of each physical tape block. All Control Data 7-track magnetic tape units use the IBM-compatible three-quarter-inch inter-block gaps, so that their performance when the tape speed is low and short blocks are in use is not as high as that of other magnetic tape units which have otherwise identical specifications but which are able to use shorter inter-block gaps (e.g., the Honeywell 204B Series).

The Control Data Magnetic Tape Unit Controllers can control a maximum of from 4 to 16 tape units each, depending on which model is selected (see Table II). All the tape units connected to a particular controller must have the same physical tape speed.

Each controller can handle as many simultaneous data transmissions as it has data channels connected to it. Models are available with one, two, three, or four possible data channel connections, as shown in Table II. These data channels are connected to a 6681 Data Channel Converter, which provides the interface between the tape controllers

TABLE I: CHARACTERISTICS OF THE CONTROL DATA 7-TRACK MAGNETIC TAPE UNITS

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, char per sec	Interblock Gap Lengths			Efficiency, %(3)		Rewind Speed, inches per sec
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks	
601	37.5	556	20,850	0.75	20.0	417	19%	71%	200
		200		0.75	20.0	150	40%	87%	
603	75.0	556	41,700	0.75	10.0	417	19%	71%	350
		200		0.75	10.0	150	40%	87%	
604	75.0	800	60,000	0.75	10.0	600	14%	62%	
		556		0.75	10.0	417	19%	71%	350
		200		0.75	10.0	150	40%	87%	
606	150.0	556	83,400	0.75	5.0	417	19%	71%	350
		200		0.75	5.0	150	40%	87%	
607	150.0	800	120,000	0.75	5.0	600	14%	62%	350
		556		0.75	5.0	417	19%	71%	
		200		0.75	5.0	150	40%	87%	

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.
(2) Number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.

TABLE II: CONTROLLERS FOR CONTROL DATA 7-TRACK MAGNETIC TAPE UNITS

Controller Model	No. of Channels	Max. No. of Tapes	Acceptable Tape Unit Models*
3127	1	4	601
3228	1	4	604 or 607
3229	1	8	604 or 607
3421	2	4	604 or 607
3422	2	6	604 or 607
3423	2	8	604 or 607
3622	2	16	606 or 607
3625	3	8	606 or 607
3626	3	16	606 or 607
3623	4	8	606 or 607
3624	4	16	606 or 607

* Tape units with different tape transport speeds must not be connected to the same magnetic tape controller.

.12 Description (Contd.)

and a 6000 Series Data Channel. Where there are multiple data channels connected to a single magnetic tape controller, it is not necessary that each data channel be connected to the same Control Data computer system. Where there are two computers at a single site, it is common practice to connect a single tape controller to both computer systems. This allows both computers to use any of the magnetic tape units connected to the controller, and eliminates the necessity for special switching devices.

The 7-track magnetic tape units can use pure binary or BCD formats and can read backward as well as forward. Writing must always operate in the forward direction. Searching backward or forward to find a file mark, and rewinding with or without automatic unloading of the tape reel, can be handled by the magnetic tape subsystem independently of the Peripheral Processor once the operation has been initiated.

Data channel control flags can be set under three separate conditions: when a tape unit becomes available, when an operation ends normally (i.e., successfully), and when something has prevented an operation from being successfully completed. In addition, there are 11 status codes which can be tested by the Peripheral Processor program. These status codes are available for use whenever required. They indicate whether a tape unit is available or not; whether the tape is positioned at a file mark, at the load point, or at the physical end of the tape; what density is currently being used, whether writing is permitted, and whether data has been lost through timing conflicts or is of dubious value because of the known occurrence of a transverse or longitudinal parity error.

.13 Availability: . . . . . . 6 months.

.14 First Delivery

Model 601 . . . . January 1965.
Model 603 . . . . March 1963.
Model 604 . . . . May 1964.
Model 606 . . . . August 1962.
Model 607 . . . . May 1964.

.2 PHYSICAL FORM

Each tape drive is a single unit. The drive past the read, write, and erase heads uses pneumatic capstans. The magnetic tape passes through vacuum reservoirs immediately before and after passing under the heads themselves. The vacuum reservoirs are vertical and can hold about seven feet of tape except on the tape units which operate at 37.5 inches per second; on these units the reservoirs are placed horizontally and have a capacity of about three feet of tape.

There are three heads: the erase head followed by the write head and the read head. The gaps between the heads are 0.4375 inches between the erase and write heads, and 0.3 inches between the write and read heads.

.3 EXTERNAL STORAGE

The Control Data 600 Series Magnetic Tape Units use one-half-inch plastic tape. Normally 2,400-foot reels are used, but some installations are successfully using 3,600-foot reels with these tape units.

The coding used is exactly the same as that used with the IBM 729 Magnetic Tape Units.

.4 CONTROLLERS

All tape units must be connected to a controller. The wide range of available controllers is shown in Table II.

.5 PROGRAM FACILITIES AVAILABLE

The tape units can read a single block in the forward or reverse direction, or write a block in the forward direction only. The size of the block is determined by the amount of storage specified as the input or output area in the instruction, and is limited only by the amount of core storage available. An end-of-file mark can be written and is preceded by a 6-inch gap. Search operations to find the end-of-file mark can be conducted in either direction. A special instruction is available to erase 6 inches of tape, in order to skip over a bad spot on the tape.

(Contd.)

.5 PROGRAM FACILITIES AVAILABLE (Contd.)

The program can select either binary or BCD codes and can test the control flags to determine when a tape unit becomes available, when an operation is completed normally, or when an operation is completed in some abnormal manner.

The current status of a tape unit can be tested at any time. Special status indicators show: whether the unit is available or not; whether the tape is positioned at a file mark, at the load point, or whether it is approaching the physical end of the tape; what density is currently being used; and whether the tape reel presently mounted can be written on. Error status indicators show whether any data has been lost through timing conflicts or whether any parity errors have been found.

.6 PERFORMANCE

The major performance characteristics of the Control Data 600 Series of magnetic tape units (7-track) are summarized in Table I. The effective speed of any particular tape unit at any particular block size can be calculated by using the formula "Effective speed = Peak speed x Block length in chars/(Block length + Interblock gap length in chars)." The required values are included in Table I. Alternatively, the effective speeds can be read from the graphs at the end of this section.

.7 EXTERNAL FACILITIES

The unit number is displayed on a dial at the top of the unit. There are ten positions, eight of which are marked 1 through 8 and two marked "stand-by." Single button controls are used to bring the mounted tape to the load point and to prepare a tape reel for dismounting. Loading and unloading a reel of tape takes approximately one minute, and the tape unit must be stopped while this is done.

The peak frequency of reloading is directly related to the tape transport speed, and is once every 13, 6.5, or 3.25 minutes for units with tape speeds of 37.5, 75, and 150 inches per second, respectively.

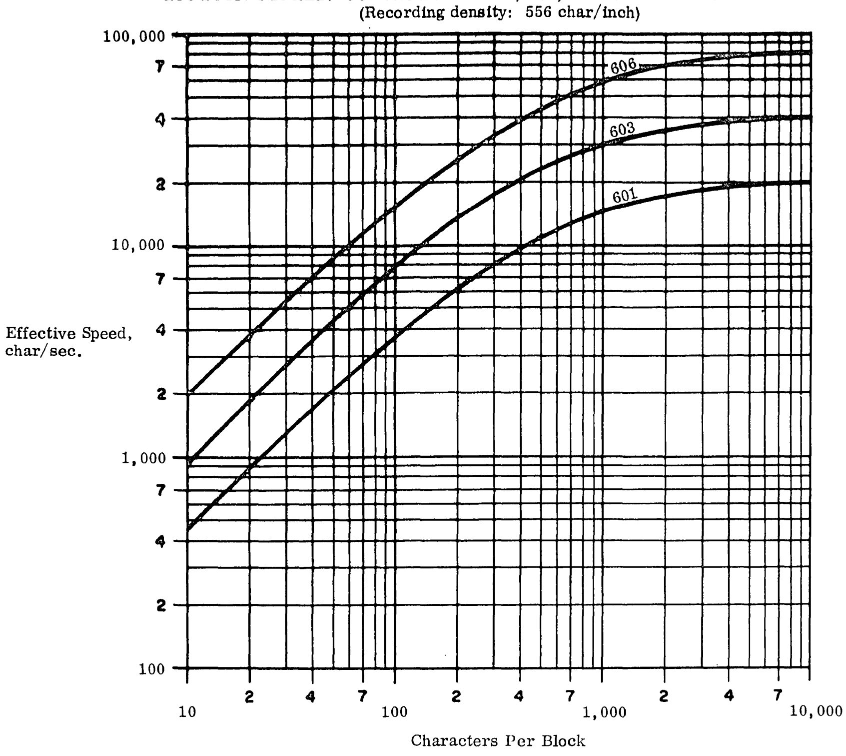
.8 ERRORS, CHECKS, AND ACTION

Parity errors cause the setting of an indicator that can be tested by the Peripheral Processor programs. Such errors may be noted either during the automatic read-back operation, which occurs while writing is in progress, or during normal reading. Two parity checks are made, one on each 6-bit data character transferred and one on the longitudinal parity character at the end of each physical tape block.

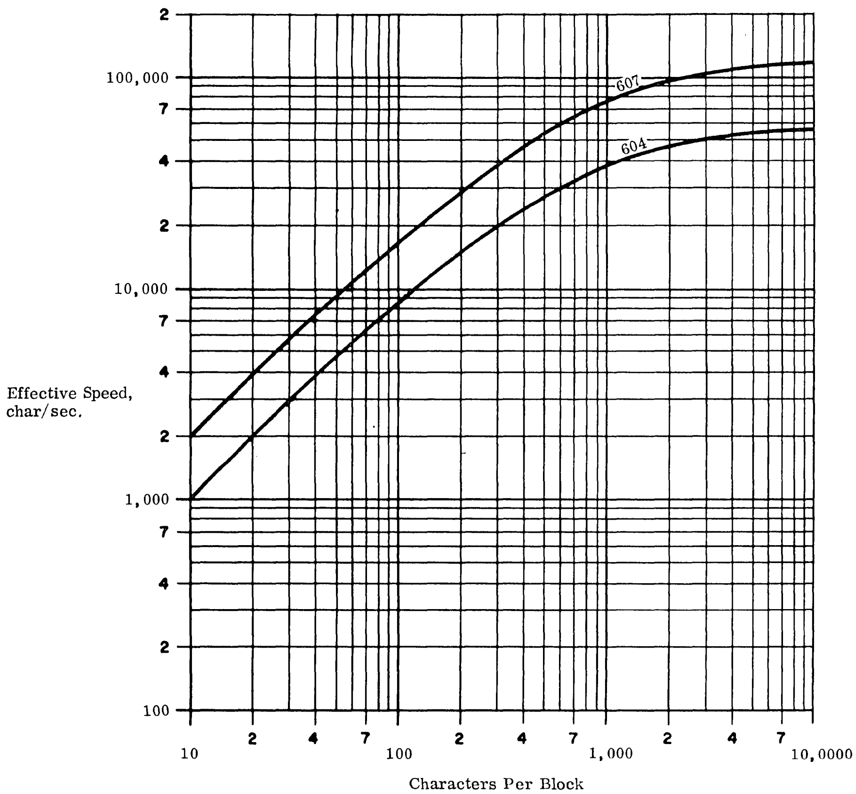
Errors which arise from timing conflicts and which lead to a loss of data are similarly handled—by setting a testable indicator.

Checks are made for the approaching end of the tape, and for a match between the actual length of an incoming tape block and the input area set aside to receive the block. Indicator settings are available to notify the program of the result of these checks. No explicit check is made upon the adequacy of the plastic tape itself; reliance is placed upon the parity checks on the data recorded on the tape.

EFFECTIVE SPEED: CONTROL DATA 601, 603, and 606 MAGNETIC TAPE UNITS
(Recording density: 556 char/inch)



EFFECTIVE SPEED: CONTROL DATA 604 AND 607 MAGNETIC TAPE UNITS
(Recording density: 800 char/inch)



AUERBACH

INPUT-OUTPUT: 600 SERIES 9-TRACK MAGNETIC TAPE UNITS

.1 GENERAL

.11 Identity: . . . . Control Data Magnetic Tape Units, Models 692, 694, 696, and associated Magnetic Tape controllers

.12 Description

The Control Data 692, 694, and 696 Magnetic Tape Units use 9-track coding, with a recording density of 800 bits per inch. Their peak data transfer rates are 30,000, 60,000 and 90,000 bytes per second, respectively, and the tape recording used is compatible with the IBM 2400 Series 800 bpi magnetic tape units, since they use the same coding, the same checking, and the same densities. They are not compatible under normal circumstances with the other tape units used with the Control Data 6000 Series; however, they can be modified to read and write seven-track tape instead of (not as well as) nine-track tape.

The effective data transfer rates are affected by the time taken to pass over the interblock gap and by the physical length of each magnetic tape block. The interblock gap length is 0.6 inch, and the effective data transfer rates for various block lengths are shown in both Table I and the graph on the next page.

The peak speeds of the Control Data 692, 694, and 696 tape units are 30,000, 60,000 and 90,000 eight-bit bytes per second, respectively. These speeds are functionally equivalent to 40,000, 80,000, and 120,000 six-bit characters per second, respectively, unless the data is recorded in the 8-bit Extended BCD or 4-bit packed decimal codes used in the IBM System/360.

The reading and recording operations are checked by the standard row and track parity checking schemes. In addition, a cyclic code check is used to test the validity of each tape block or physical record. This check is based on an 8-bit character that is generated from the data bytes during the write operation and then recorded at the end of the tape block. During subsequent read operations, the check character is regenerated and compared to the check character that was originally recorded.

Models 3825, 3826, and 3827 controllers have been announced for the 9-track Control Data tape units. The ratio of data channel connections to magnetic tape unit connections is unusually high, one data channel being provided for every two magnetic tape units which can be connected. Preliminary indications are that it will be possible to connect any of the three 9-track tape unit models to any of the three controller models. The number of magnetic tape units and data channels that can be connected to each controller model are as follows:

Controller Model:	3825	3826	3827
Magnetic Tape Units:	4	6	8
Data Channels:	2	3	4

The physical and functional details of the Models 692, 694, and 696 Magnetic Tape Units are, except for the coding and checking methods, identical with those of the Control Data 7-track magnetic tape units; these are described in detail in the preceding report section, 260:091. The major design features of these tape units are the use of vacuum capstans and vacuum reservoirs for tape control, combined read/write heads for read-after-write checking, and automatic searching for end-of-file marks in either the forward or backward direction.

The 9-track magnetic tape units are manufactured by Control Data Corporation.

.14 Availability: . . . . . . ?

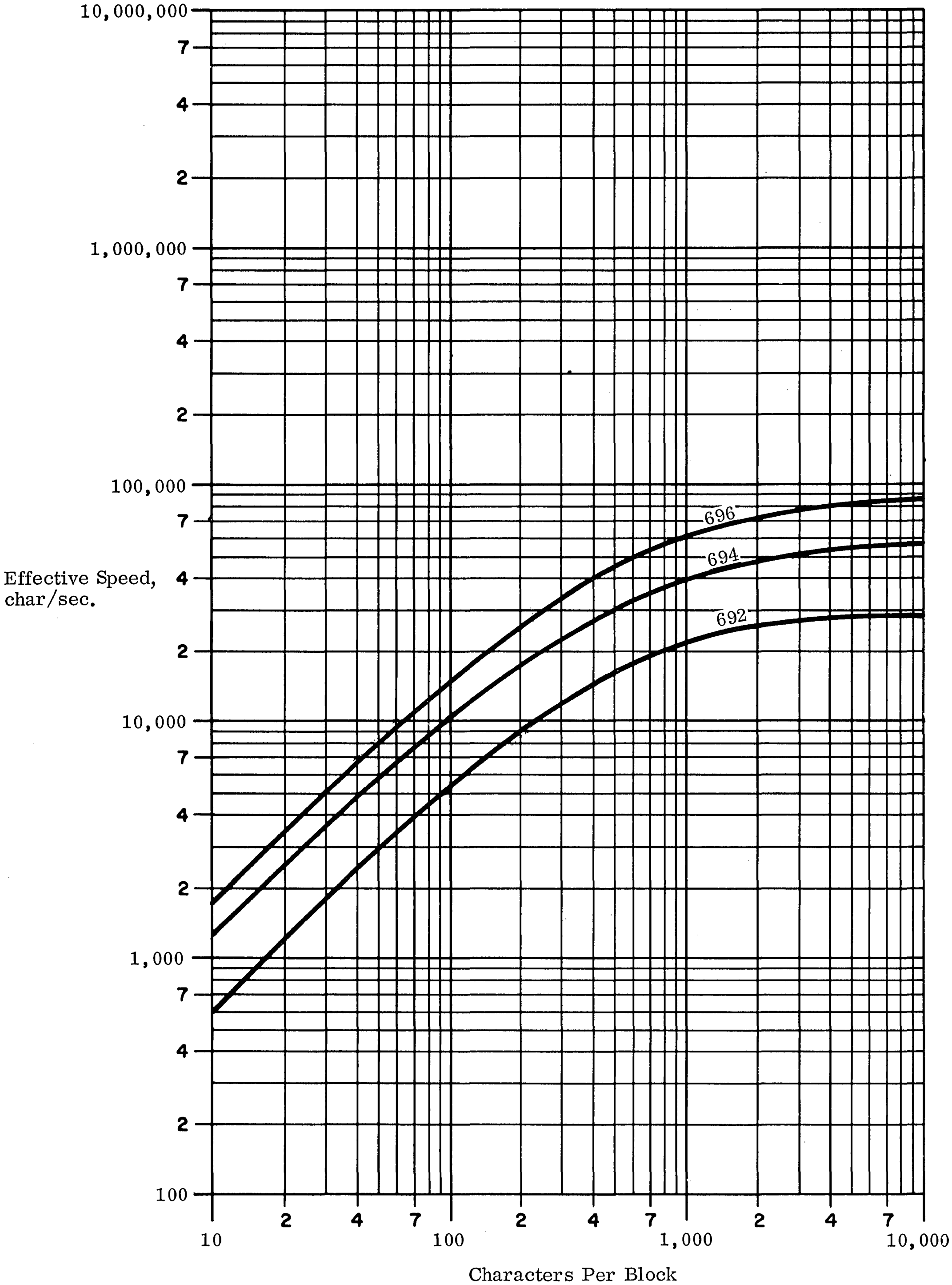
.15 First Delivery: . . . . ?

TABLE I: CHARACTERISTICS OF THE CONTROL DATA 9-TRACK MAGNETIC TAPE UNITS

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, bytes per sec	Interblock Gap Lengths			Efficiency, % (3)		Rewind Speed, inches per sec
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks	
692	37.5	800	30,000	0.6	16.0	480	17	68	200
694	75.0	800	60,000	0.6	8.0	480	17	68	350
696	112.5	800	90,000	0.6	5.4	480	17	68	?

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.
(2) Number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.

EFFECTIVE SPEED: CONTROL DATA 692, 694, AND 696 MAGNETIC TAPE UNITS
(Recording density: 800 bytes/inch)



INPUT-OUTPUT: 626 14-TRACK MAGNETIC TAPE UNIT

.1 GENERAL

.11 Identity: . . . . Control Data 626 Magnetic Tape Unit and 6622 Magnetic Tape Controller.

.12 Description

The Control Data 626 Magnetic Tape Unit is the only 14-track magnetic tape equipment available with the 6000 Series. The 626 uses one-inch tape, recorded at 800 rows per inch, with a tape speed of 150 inches per second. Each row contains two 6-bit characters and a parity bit for each character. The resulting peak data transfer rate is 240,000 six-bit characters per second.

Functionally, there is no compatibility between the Control Data 626 Magnetic Tape Unit and any other magnetic tape equipment in the industry. Unlike the 7-track and 9-track 600 Series models described in Sections 260:091 and 260:092, the Model 626 is designed simply to provide high data transfer rates within a Control Data 6000 Series computer system.

Operational characteristics and data transfer efficiencies of the 626 Magnetic Tape Unit are shown in Table I, in a format that facilitates comparisons with other tape units. The effective data transfer rates are affected by the time required to pass over the interblock gap and by the physical length of each magnetic tape block. The interblock gap length is 0.75 inch, and the effective data transfer rates for various block lengths are shown in the graph on the next page.

The physical and functional details of the Model 626 are essentially identical with those of the Model 607, as described in Section 260:091. Noteworthy features include the use of vacuum capstans and vacuum reservoirs for tape control, combined read/write heads for read-after-write checking, and automatic searching for end-of-file marks in either the forward or backward direction.

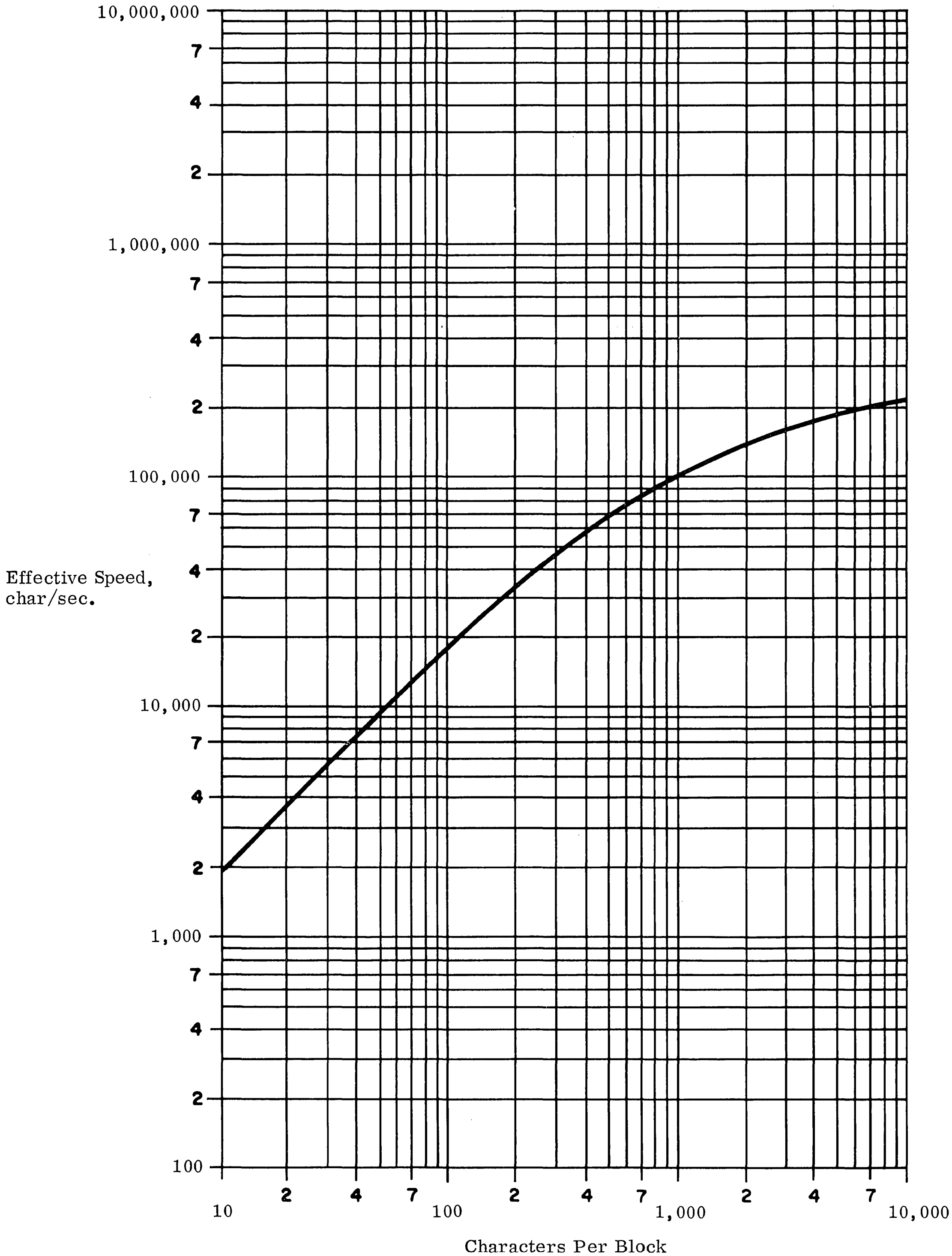
The Model 6622 Magnetic Tape Controller can handle up to four Model 626 Magnetic Tape Units. However, since the 6622 Controller provides only a single data channel, only one tape unit per Controller can be writing or reading at any one time.

TABLE I: CHARACTERISTICS OF THE CONTROL DATA 626 MAGNETIC TAPE UNIT

Model No.	Tape Speed, inches per sec	Recording Density, bits per inch	Peak Speed, bytes per sec	Interblock Gap Lengths			Efficiency, % (3)		Rewind Speed, inches per sec
				inches	msec (1)	chars (2)	100-char blocks	1,000-char blocks	
626	150	800	240,000	0.75	5.0	1,200	7.6	45	350

(1) Time in milliseconds to traverse each interblock gap when reading or writing consecutive blocks.
(2) Number of character positions occupied by each interblock gap.
(3) Effective speed at the indicated block size, expressed as a percentage of peak speed.

EFFECTIVE SPEED: CONTROL DATA 626 MAGNETIC TAPE UNIT



INPUT-OUTPUT: AUGMENTED INPUT-OUTPUT BUFFER AND CONTROL

.1 GENERAL

.11 Identity: . . . . 6411 Augmented Input-Output Buffer and Control.

.12 Description

The 6411 Augmented Input-Output Buffer and Control unit is a large-scale, multiple-device subsystem that is designed to virtually double the input-output and control facilities of a Control Data 6400 or 6600 computer system. The 6411 is, in effect, an additional basic 6000 Series computer system without a Central Processor and with a smaller Central Memory.

The components of a 6411 Input-Output Buffer and Control unit include:

- 12 high-speed, bi-directional Data Channels;
- 10 logically independent Peripheral and Control Processors, each with a private core storage unit that consists of 4, 096 12-bit words; and
- 1 Main Memory unit consisting of 16, 384 60-bit words of core storage, with a cycle time of 1 microsecond, accessible to all of the Peripheral and Control Processors.

Up to twelve 6411 Input-Output Buffer and Control units can be connected to a 6400 or 6600 computer system, providing extensive, flexible, and powerful input-output and multiprocessing facilities.

The 6411 can function as an on-line satellite computer system for a Control Data 6400 or 6600, connected via the Standard Data Channels. Data from a wide variety of sources, both remote and local, can be buffered in the 6411, selected, gathered, batched, and scheduled for transmission to Central Memory for eventual processing by the Central Processor, without placing any demands or delays on any other part of the 6000 Series computer system. Another use of the 6411 unit is to provide specific groups of I/O devices or classes of data with individual and absolutely private storage and processing units. This arrangement can also be used to advantage in remote time-sharing operations.

The 6411 Augmented Input-Output Buffer and Control unit is controlled and integrated with the rest of the 6000 Series system by means of a modified version of the SIPROS operating system. One of the Peripheral and Control Processors within the 6411 subsystem is designated as the Executive/Monitor control processor for the entire 6411. This control system works in conjunction with, although subordinate to, the SIPROS Executive/Monitor in the central computer system.

The instruction repertoire of the Peripheral Processors within the 6411 unit is identical with that of the basic 6000 Series Peripheral and Control Processors described in Section 260:052. However, the two instructions that normally provide communication with the Central Processor are modified as used in the 6411 subsystem because no Central Processor is included in the 6411. The Read Program Address instruction in the 6411 examines the status of the data trunk that can be used to link the 6411's Main Memory and the optional Extended Core Storage unit (see Section 260:043). The 6411 unit uses the Exchange Jump instruction to initiate block data transfers between its Main Memory unit and the Extended Core Storage unit.

It is significant to note that the 6000 Series programmer need not be concerned about the instruction set or processing capabilities of the 6411's Peripheral and Control Processors, since he normally programs exclusively for the Central Processor. All Peripheral Processor task assignments are normally designated by the 6411's Executive/Monitor operating system. The programmer, however, can explicitly assign tasks to the Peripheral and Control Processors by coding specialized routines in the ASPER assembly language (described in Section 260:172).

INPUT-OUTPUT: 3276 COMMUNICATION TERMINAL CONTROLLER

.1 GENERAL

.11 Identity . . . . Control Data 3276-A Communication Terminal Controller.

.12 Description

The Control Data 3276 Communication Terminal Controller is a multiplexing control unit, originally developed for Control Data's 3000 Series computers, that enables a wide variety of standard and specialized data communications devices to be connected to the standard 6000 Series data channels via a 6681 Data Channel Converter. Numerous data set adapters and terminal units are provided by Control Data to function under control of the 3276 Controller, providing the 6000 Series with the capability to communicate with specialized remote devices ("Class A" operations), generalized, conversational remote devices ("Class B" operations), and remote computer centers ("Class C" operations).

The 3276 Communication Terminal Controller is capable of controlling up to 32 simplex telegraph-grade lines (16 sending lines and 16 receiving), or up to 16 half-duplex or full-duplex telegraph-grade lines, or up to 8 half-duplex or full-duplex voice-grade lines. A maximum of eight 3276 Controllers can be connected to each 6000 Series data channel through a single 6681 Data Channel Converter interface. The 3276 provides the necessary speed conversion for all data being transmitted to and from the high-speed data channels, and performs the serial-to-parallel bit transmission conversions required to communicate with the 6000 Series computer system.

Data is transferred to the computer in groups of 12-bit words. Four bits of each word are character-transfer status bits, and the remaining eight bits are data bits. Many of Control Data's terminal units cannot perform automatic parity checking. Instead, this operation is performed under program control in the 6000 Series Peripheral and Control Processors.

Besides its multiplexing operations, the 3276 Communication Terminal Controller performs the following functions:

- Decodes the "connect codes" sent by the Peripheral and Control Processors to the individual remote input-output units. A Read Connect Code causes the 3276 to scan the status of the low-speed input units. (The 3276 cannot interrupt the Peripheral and Control Processors when data is available for processing; these processors must periodically connect to and interrogate the 3276 by program to determine whether input data is available.)
- Converts the input bit-serial characters (one bit at a time) to parallel characters of up to 8 data bits for transmission to the Peripheral Processors.
- Converts the output parallel characters sent from the Peripheral Processors and transmits these characters, one bit at a time, to the 3276's output channels for bit-serial transmission.
- Connects the Peripheral Processors to transmission lines of widely varying speeds.
- Sends to the Peripheral Processors status response codes such as Character Ready, Character Request, Character Lost, Channel Idle, and Broken Circuit.
- Distributes input-output data between the Peripheral Processors and the external communications lines.

Table I lists the principal terminal units that can be included within the modular 3276 Communication Terminal Controller. The table also indicates the type and speed of the transmission lines that are required for use with these terminal units. Standard data sets are also listed for those terminal units that require them.

Described below are these and other Control Data terminal units and data set adapters that can be controlled by the 3276 Communication Terminal Unit, plus some of the remote devices that can be connected to these terminals.

- 311 Data Set Adapter — provides the interface for IBM 1009 Data Transmission Units, IBM 1013 Card Transmission Terminals, and IBM 7702 Magnetic Tape Transmission Terminals.
- 312 Data Set Adapter — provides the same interfacing capabilities as the 311 Data Set Adapter, but transmits data over 2,000-bps lines rather than the 311's 2,400-bps lines.
- 313 Data Set Adapter — provides the terminal connection between half- or full-duplex low-speed (200-bps) communications lines and the 3276 Controller. Models 33 and 35 Teletype units and IBM 1050 Data Communication Systems can be controlled by the 313.
- 314 Data Set Adapter — enables the connection of standard TWX equipment, the IBM 1050, Models 33 and 35 Teletype units, Control Data's 8092 Teleprogrammer System, and Control Data 160-A and 8090 computer systems.

.12 Description (Contd.)

- 315 Data Set Adapter — communicates with Control Data's 1010 Card Input Station and 8011 Data Collector, as well as with AT&T's Dataspeed Type 5 equipment (750 words per minute).

- 316 Data Set Adapter — can control the same remote devices as the 315 Data Set Adapter; if both adapters are used in the same communication system, one for receiving and one for sending data, they can be operated with a Model 801 Data-Phone Automatic Calling Unit.

- 317 Data Set Adapter — provides the terminal connection between half- or full-duplex medium-speed communications lines (up to 1,200 bps) and the 3276 Controller. Dataspeed Type 2 terminals (1,050 words per minute) can be connected via the 317.

- 318 Data Set Adapter — provides the same terminal unit capabilities as the 317 Data Set Adapter. Unlike the 317, the 318 Data Set Adapter can be operated with a Model 801 Data-Phone Automatic Calling Unit.

- 321 Teletype Terminal Unit — communicates over private or leased telegraph-grade lines with the IBM 1050 system and with standard Teletype equipment.

- 323 Teletype Terminal Unit — provides the same interfacing capabilities as the 321 Teletype Terminal Unit, but can only send or receive data. (The 321 serves as both an input and output terminal unit.)

TABLE I: TERMINAL UNITS USED WITH THE 3276 COMMUNICATION TERMINAL CONTROLLER

Terminal Unit No.	Type of Line	Data Sets Required	Terminal Positions Required*	
			Send	Receive
311	2400-bps leased telephone line	201B	2	2
312	2000-bps telephone network	201A and 801 Dialer	2	2
313	200-bps leased telephone line	103A	1	1
314	200-bps TWX network	103A and 801 Dialer	2	2
315	750-wpm telephone line	402C	2	—
316	750-wpm telephone line	402D	—	2
317	1050-wpm telephone line	202C	2	2
318	1050-wpm telephone line	202D and 801 Dialer	2	2
321	Full- or half-duplex telegraph-grade	None	1	1
323	Simplex telegraph-grade	None	1	—
323	Simplex telegraph-grade	None	—	1

* Each 3276 Communication Terminal Controller contains 32 terminal positions — 16 send and 16 receive.

INPUT-OUTPUT: 6600 SERIES DATA SET CONTROLLERS

.1 GENERAL

.11 Identity: . . . . 6675 Data Set Controller.
6676 Data Set Controller.
6677-A Multiplexor.
6677-B Multiplexor.
6678 Data Set Controller.

.12 Description

The 6600 Series Data Set Controllers are single-circuit multiplexing terminal units that can connect a wide variety of remote data communications devices and remote computer systems directly to the input-output data channels of the 6000 Series computer systems. These controllers communicate with the remote devices over the public or private communications line facilities of the telephone or telegraph companies and use standard data set modems as interfaces at the remote and central ends of the transmission lines.

The 6600 Series Controllers assemble the serial data received from the data sets into 12-bit parallel data for use by the 6000 Series Peripheral and Control Processors, and they perform the converse data manipulation operations when data is transmitted to the remote stations. In addition, each Controller generates a 12-bit error-check code word in its cyclic encoding unit during the transmission and receipt of each data block. If Controllers are used at both ends of the transmission lines, the code word can be generated at both locations and compared to detect data transmission errors. Control Data states that the reliability factor for this technique of error detection is better than 99.9%, provided that the data block length does not exceed 4,096 bits.

The maximum number of 6600 Series Data Set Controllers that can be connected directly to each 6000 Series data channel is a function of the 6000 Series operating system and the maximum duty cycles of the system; therefore, it can only be determined by a throughput analysis of each proposed data communications system configuration.

.121 6675 Data Set Controller

The 6675 Data Set Controller can be used to connect a central 6000 Series computer system with a remote Control Data 1600 Series, 3000 Series, or another 6000 Series computer system. Data transmission between the systems is accomplished over Telpak A telephone lines at the rate of 40,800 bits per second. Bell System 301B Data Sets are the standard modems used at either end of the transmission line, but Models 201A, 201B, and 301C can also be used. Up to four 301B Data Sets can be multiplexed into each 6675 Data Set Controller. If slower-speed data sets are used, a maximum of 20 such devices can be used with a 6675 Controller. In addition to the 6675 Controller at the central 6000 Series computer site, another 6675 Controller is required at the remote site if the remotely-linked computer is also a 6000 Series system. If the remote computer is a Control Data 1600 Series system, a Model 8529 or 68529 Data Set Controller must provide the immediate interface; if the remote computer is a Control Data 3000 Series system, a Model 3275 or 63275 Data Set Controller is required as the immediate interfacing unit.

.122 6676 Data Set Controller

The 6676 Data Set Controller can control up to 64 Bell System 103A2 Data Sets located at the central 6000 Series computer site. Data is transmitted over private telegraph-grade lines (up to 20 miles) or over voice-grade telephone lines at 110 bits per second. At the remote end of the communications link, a Bell System 101C Data Set interfaces with a standard Model 33 or 35 Teletype terminal unit of either the ASR or KSR type. Up to 200 Teletype stations can communicate with a single 6000 Series data channel through use of this communications network.

.123 6677-A and 6677-B Multiplexors

The 6677-A Multiplexor can control up to 64 Bell System 103A or 103F Data Sets; the 6677-B can control up to 128 data sets of the same type. Data is transmitted over telephone lines at a speed of 240 bits per second. A typical remote device used with the 6677 Multiplexors is Control Data's 6060 Remote Calculator (see Report Section 260:062).

.124 6678 Data Set Controller

The 6678 Data Set Controller can control up to 64 Bell System 201A or 201B Data Sets, but the two data set models cannot be intermixed on the same 6678 Controller. A typical remote device used with the 6678 Data Set Controller is Control Data's 6090 Entry/Display system (see Report Section 260:063). Data is transmitted between the 6678 Data Set Controller and its remote devices over telephone lines at a rate of either 2,000 or 2,400 bits per second.

SIMULTANEOUS OPERATIONS

.1 GENERAL

A Control Data 6000 Series computer system can concurrently:

- Execute up to 10 independent instructions from a single Central Processor program; and
- Execute up to 10 independent peripheral programs, one in each of the Peripheral and Control Processors; and
- Transfer data between Central Memory and Extended Core Storage; and
- Control up to 12 input-output operations, one on each Data Channel; and
- Handle as many additional input-output operations as can be supported on the Data Channels by multiplexing or buffering the individual peripheral devices or their controllers.

Input-output operations place no demands (or "interference" delays) on the Central Processor because they are controlled by the independently-operating Peripheral and Control Processors. Even accesses to Central Memory by the Peripheral Processors normally impose no delays upon the Central Processor, since up to 10 Central Memory banks can be accessed simultaneously. Whenever a Peripheral Processor and the Central Processor attempt to access the same Central Memory bank at the same time, the Central Processor's access request is given priority.

Every input-output operation does cause a certain amount of delay to the Peripheral Processor that is controlling it. The amount of this delay is frequently multiplied because of the manner in which the SIPROS I/O routines handle the slower input-output operations. In fact, a given set of input-output data will, in many cases, pass into and out of the memory of a Peripheral Processor four times before the input or output operation is complete. Typically, data can pass from the input Data Channel, to the memory of a Peripheral and Control Processor, to the System Disk for batching, back to the memory of the Peripheral Processor, and finally to Central Memory for processing. This path is reversed for an output operation.

This four-way Peripheral Processor loading (or the corresponding two-way loading when the System Disk is not used for intermediate storage) has been calculated for each of the major peripheral devices. Because these times will vary for the three computer systems within the Control Data 6000 Series, the Simultaneous Operations section of the appropriate Computer System Subreport should be consulted to obtain these I/O timing delays:

Control Data 6400 . . . . Section 263:111.
Control Data 6600 . . . . Section 264:111.
Control Data 6800 . . . . Section 265:111.

INSTRUCTION LISTS: CONTROL DATA 6000 SERIES

This section of the Control Data 6000 Series report presents two separate and distinct instruction lists — one for the 6000 Series Central Processors and one for the Peripheral and Control Processors that are included as integral, independently-functioning parts of every 6000 Series system. Both instruction lists include brief descriptions of the instructions, as well as the time required to execute each instruction. Immediately following each instruction list is a table explaining the symbols used in the descriptions.

TABLE I: CENTRAL PROCESSOR INSTRUCTION LIST

Mnemonic	Functional Unit	Description	Execution Time in Minor Cycles		
			6800 (25 ns/cycle)	6600 (100 ns/cycle)	6400 (100 ns/cycle)
	BRANCH				
PS		Program Stop	---	---	---
RJ		Return jump to K	13	13	12
JP		Jump to Bi + K	14*	14*	12
ZR		Jump to K if Xi = 0	9	9	12
NX		Jump to K if Xj ≠ 0	9	9	12
PL		Jump to K if Xj is plus (positive)	9	9	12
NG		Jump to K if Xj is negative	9	9	12
IR		Jump to K if Xj is in range	9	9	12
OR		Jump to K if Xj is out of range	9	9	12
DF		Jump to K if Xj is definite	9	9	12
ID		Jump to K if Xj is indefinite	9	9	12
EQ		Jump to K if Bi = Bj	8*	8*	12
ZR		Jump to K if Bi = B_O	8*	8*	12
NE		Jump to K if Bi ≠ Bj	8*	8*	12
NZ		Jump to K if Bi ≠ B_O	8*	8*	12
GE		Jump to K if Bi > Bj	8*	8*	12
PL		Jump to K if Bi ≥ B_O	8*	8*	12
LT		Jump to K if Bi ≤ Bj	8*	8*	12
NG		Jump to K if Bi ≤ B_O	8*	8*	12
	BOOLEAN				
BXi		Transmit Xj to Xi	3	3	4
BXi		Logical product of Xj & Xk to Xi	3	3	4
BXi		Logical sum of Xj & Xk to Xi	3	3	4
BXi		Logical difference of Xj & Xk to Xi	3	3	4
BXi		Transmit the complement of Xk to Xi	3	3	4
BXi		Logical product of Xj & Xk; complement to Xi	3	3	4
BXi		Logical sum of Xj & Xk; complement to Xi	3	3	4
BXi		Logical difference of Xj & Xk; complement to Xi	3	3	4
	SHIFT				
LXi		Left shift Xi, jk places	3	3	5
AXi		Arithmetic right shift Xi, jk places	3	3	5
LXi		Left shift Xk nominally Bj places to Xi	3	3	5
AXi		Arithmetic right shift Xk nominally Bj places to Xi	3	3	5
NXi		Normalize Xk to Xi and Bj	4	4	6
ZXi		Round and normalize Xk in Xi & Bj	4	4	6
UXi		Unpack Xk to Xi and Bj	3	3	6
PXi		Pack Xi from Xk and Bj	3	3	6
MXi		Form mask in Xi, jk bits	3	3	5
	ADD				
FXi		Floating sum of Xj and Xk to Xi	4	4	11
FXi		Floating difference Xj and Xk to Xi	4	4	11
DXi		Floating double precision sum of Xj and Xk to Xi	4	4	11
DXi		Floating double precision difference of Xj & Xk to Xi	4	4	11
RXi		Round floating sum of Xj and Xk to Xi	4	4	11
RXi		Round floating difference of Xj and Xk to Xi	4	4	11
	LONG ADD				
IXi		Integer sum of Xj and Xk to Xi	3	3	6
IXi		Integer difference of Xj and Xk to Xi	3	3	6

TABLE I: CENTRAL PROCESSOR INSTRUCTION LIST (Contd.)

Mnemonic	Functional Unit	Description	Execution Time in Minor Cycles 6800 (25 ns/cycle)	6600 (100 ns/cycle)	6400 (100 ns/cycle)*
	MULTIPLY				
FXi		Floating product of Xj and Xk to Xi	10	10	56
RXi		Round floating product of Xj & Xk to Xi	10	10	56
DXi		Floating double precision product of Xj & Xk to Xi	10	10	56
	DIVIDE				
FXi		Floating divide Xj by Xk to Xi	29	29	56
RXi		Round floating divide Xj by Xk to Xi	29	29	56
NO		No operation	---	---	---
CXi		Count the number of 1's in Xk to Xi	8	8	68
	INCREMENT				
SAi		Set Ai to Aj + K	3	3	5
SAi		Set Ai to Aj + complement of K	3	3	5
SAi		Set Ai to Bj + K	3	3	5
SAi		Set Ai to Bj + complement of K	3	3	5
SAi		Set Ai to Xj + K	3	3	5
SAi		Set Ai to Xj + complement of K	3	3	5
SAi		Set Ai to Xj + Bk	3	3	5
SAi		Set Ai to Aj + Bj	3	3	5
SAi		Set Ai to Aj - Bk	3	3	5
SAi		Set Ai to Bj + Bk	3	3	5
SAi		Set Ai to Bj - Bk	3	3	5
SBi		Set Bi to Aj + K	3	3	5
SBi		Set Bi to Aj + complement of K	3	3	5
SBi		Set Bi to Bj + K	3	3	5
SBi		Set Bi to Bj + complement of K	3	3	5
SBi		Set Bi to Xj + K	3	3	5
SBi		Set Bi to Xj + complement of K	3	3	5
SBi		Set Bi to Xj + Bk	3	3	5
SBi		Set Bi to Aj + Bk	3	3	5
SBi		Set Bi to Aj - Bk	3	3	5
SBi		Set Bi to Bj + Bk	3	3	5
SBi		Set Bi to Bj - Bk	3	3	5
SXi		Set Xi to Aj + K	3	3	5
SXi		Set Xi to Aj + complement of K	3	3	5
SXi		Set Xi to Bj + K	3	3	5
SXi		Set Xi to Bj + complement of K	3	3	5
SXi		Set Xi to Xj + K	3	3	5
SXi		Set Xi to Xj + complement of K	3	3	5
SXi		Set Xi to Xj + Bk	3	3	5
SXi		Set Xi to Aj + Bk	3	3	5
SXi		Set Xi to Aj - Bk	3	3	5
SXi		Set Xi to Bj + Bk	3	3	5
SXi		Set Xi to Bj - Bk	3	3	5
?		Read Mass Core	?	?	?
?		Write Mass Core	?	?	?

*Add 6 minor cycles to branch time for a branch to an instruction which is out of the stack.

Interpretation of Descriptive Symbols

A	One of eight 18-bit address registers.
B	One of eight 18-bit index registers; B_0 is fixed and equal to zero.
i	Register specified by the 3-bit i portion of the instruction.
j	Register specified by the 3-bit j portion of the instruction.
jk	Constant, indicating number of shifts to be taken (6 bits).
k	Register specified by the 3-bit k portion of the instruction.
K	Constant, indicating branch destination or operand (18 bits).
X	One of eight 60-bit operand registers.

(Contd.)

TABLE II: PERIPHERAL AND CONTROL PROCESSOR INSTRUCTION LIST

Mnemonic	Description	Execution Time in Major Cycles *
PSN	Pass	1
LJM	Long jump to m + (d)	2-3
RJM	Return jump to m + (d)	3-4
UJN	Unconditional jump d	1
ZJN	Zero jump d	1
NJN	Nonzero jump d	1
PJN	Plus jump d	1
MJN	Minus jump d	1
SHN	Shift d	1
LMN	Logical difference d	1
LPN	Logical product d	1
SCN	Selective clear d	1
LDN	Load d	1
LCN	Load complement d	1
ADN	Add d	1
SBN	Subtract d	1
LDC	Load dm	2
ADC	Add dm	2
LPC	Logical product dm	2
LMC	Logical difference dm	2
PSN	Pass	1
PSN	Pass	1
EXN	Exchange jump	2 (minimum)
RPN	Read program address	1
LDD	Load (d)	2
ADD	Add (d)	2
SBD	Subtract (d)	2
LMD	Logical difference (d)	2
STD	Store (d)	2
RAD	Replace add (d)	3
AOD	Replace add one (d)	3
SOD	Replace subtract one (d)	3
LDI	Load ((d))	3
ADI	Add ((d))	3
SBI	Subtract ((d))	3
LMI	Logical difference ((d))	3
STI	Store ((d))	3
RAI	Replace add ((d))	4
AOI	Replace add one ((d))	4
SOI	Replace subtract one ((d))	4
LDM	Load (m + (d))	3-4
ADM	Add (m + (d))	3-4
SBM	Subtract (m + (d))	3-4
LMM	Logical difference (m + (d))	3-4
STM	Store (m + (d))	3-4
RAM	Replace add (m + (d))	4-5
AOM	Replace add one (m + (d))	4-5
SOM	Replace subtract one (m + (d))	4-5
CRD	Central read from (A) to d	6 (minimum)
CRM	Central read (d) words from (A) to m	5 plus 5/word
CWD	Central write to (A) from d	6 (minimum)
CWM	Central write (d) words to (A) from m	5 plus 5/word
AJM	Jump to m if channel d active	2
IJM	Jump to m if channel d inactive	2
FJM	Jump to m if channel d full	2
EJM	Jump to m if channel d empty	2
IAN	Input to A from channel d	2
IAM	Input to (A) words to m from channel d	4 plus 1/word
OAN	Output from A on channel d	2
OAM	Output (A) words from m on channel d	4 plus 1/word
ACN	Activate channel d	2
DCN	Disconnect channel d	2
FAN	Function (A) on channel d	2
FNC	Function m on channel d	2

*The 6400/6600 Peripheral Processor Major Cycle time is 1 microsecond; the 6800's Major Cycle time is 250 nanoseconds.

Interpretation of Descriptive Symbols

d	Implies d itself (6-bit literal).
(d)	Implies the contents of d.
((d))	Implies the contents of the location specified by d.
m	Implies m itself (12-bit quantity) used as an address.
m + (d)	The contents of d are added to m to form an operand (jump address).
(m + (d))	The contents of d are added to m to form the address of the operand.
dm	Implies an 18-bit quantity with d as the upper 6 bits and m as the lower 12 bits.

DATA CODE TABLE

Character	Internal BCD*	Tape and Printer BCD*	Card
0	00	12	0
1	01	01	1
2	02	02	2
3	03	03	3
4	04	04	4
5	05	05	5
6	06	06	6
7	07	07	7
8	10	10	8
9	11	11	9
A	21	61	12-1
B	22	62	12-2
C	23	63	12-3
D	24	64	12-4
E	25	65	12-5
F	26	66	12-6
G	27	67	12-7
H	30	70	12-8
I	31	71	12-9
J	41	41	11-1
K	42	42	11-2
L	43	43	11-3
M	44	44	11-4
N	45	45	11-5
O	46	46	11-6

Character	Internal BCD*	Tape and Printer BCD*	Card
P	47	47	11-7
Q	50	50	11-8
R	51	51	11-9
S	62	22	0-2
T	63	23	0-3
U	64	24	0-4
V	65	25	0-5
W	66	26	0-6
X	67	27	0-7
Y	70	30	0-8
Z	71	31	0-9
=	13	13	3-8
- (dash)	14	14	4-8
+	20	60	12
+0	32	72	12-0
.	33	73	12-3-8
)	34	74	12-4-8
- (minus)	40	40	11
-0	52	52	11-0
$	53	53	11-3-8
*	54	54	11-4-8
(space)	60	20	blank
/	61	21	0-1
,	73	33	0-3-8
(	74	34	0-4-8

* Octal representation of 6-bit BCD codes is shown.

PROBLEM ORIENTED FACILITIES

.1 UTILITY ROUTINES

.11 Simulators of Other Computers

IBM 7090/7094 Simulator

Reference: . . . . preliminary information.
Date available: . . . . . December 1965.
Description:

This simulator accepts 7090/7094 machine-language programs and converts them to instruction and data formats that are directly executable on any 6000 Series system. The maximum size object program that can be simulated is 32K 7090/7094 words. Standard input-output operations are simulated, and provisions will also be included to handle other I/O equipment, such as disc files, drums, and data cells. The simulator operates under the control of the SIPROS operating system and utilizes about 40,000 words of 6000 Series Central Memory. In most cases, according to Control Data, the simulated programs run at approximately the same speed as the original programs on an IBM 7090.

.12 Simulation by Other Computers: . . . . none.

.13 Data Sorting and Merging

6000 Series Sort/Merge

Reference: . . . . 6000 Series Computer Systems Manual (preliminary edition).
Record size: . . . . not specified to date.
Block size: . . . . not specified to date.
Key size: . . . . not specified to date.
File size: . . . . not specified to date.
Number of tapes/ discs: . . . . 3 to 16 tapes, or minimum of one disc unit.
Date available: . . . . . July 1966.
Description:

The 6000 Series Sort/Merge package is a generalized program that is designed to function as an integral part of the SIPROS operating system. Incoming files on tape or disc units can be sorted as an independent operation or as an integrated subtask of a total processing job. The Sort/Merge program is basically disc-oriented for efficiency of operation, but magnetic tape units can also be utilized, depending on disc availability at sort time.

Optimized input-output routines have not been included in the Sort/Merge package, since it is assumed that all I/O operations will be overlapped with the execution of several other programs by the Central Processor. Internal sorting operations will take advantage of as much core and disc storage as is specified by parameter cards as being currently available. Merging is accomplished through use of a polyphase technique. Only the several sorting keys within each record need to be sorted; the data portions of the records can be stripped off at input time and later retrieved after the keys have been sorted into the proper sequence.

Input files can be on either magnetic tape or disc file storage, and can be written in either binary or BCD form. Fixed or variable-length records can be sorted, in either ascending or descending sequence. Control cards can specify exits to user-supplied routines at various stages in the sort/merge process.

No timing information for the 6000 Series Sort/Merge has been released to date.

.14 Report Writing: . . . . . facilities will be provided both in the COBOL language and in the Linear Programming System (see Paragraph .17)

.15 Data Transcription

6000 Series Utility Programs

Reference: . . . . 6000 Series Computer Systems Manual (preliminary edition).
Date available: . . . . . December 1965.
Description:

Data transcription routines are contained in the 6000 Series library system (LIBRIOUS) and operate under control of the SIPROS operating system. These routines can be used as necessary by the SIPROS Executive, or they can be called for by operating programs, or they can be summoned by control cards to perform "off-line" data transcriptions.

SIPROS assigns a Peripheral and Control Processor to perform each data transcription task and calls the designated routine from the library. The standard routines supplied include:

Card to Card
Card to Print
Card to Tape
Tape Comparison
Card to Disk
Tape to Card
Tape to Print
Tape to Tape
Disk to Card
Disk to Print
Disk to Tape.

Code conversion can also be specified by control card, permitting data transcriptions and code conversions to be performed during a single operation. For example, the Card to Tape routine permits conversion from Hollerith to BCD, Hollerith to Display code, or no conversion (binary cards). Variously-coded magnetic tapes can be dumped in octal mode.

.16 File Maintenance

6000 Series File Manager

Reference: . . . . preliminary information.
Date available: . . . . . June, 1966.

.16 File Maintenance (Contd.)

Description:

The File Manager system for the 6000 Series provides a simplified method for controlling the storage, retrieval, usage, and modification of data files recorded on mass storage devices. The various facilities of the File Manager can be called for by means of system macro-instructions. Alternatively, these facilities can be utilized by means of control card statements entered in the input job stream. The control cards serve both to designate the files that are to be maintained and to specify the type of maintenance operation to be performed.

The 6000 Series File Manager operates under control of the SIPROS operating system. The File Manager also makes use of SIPROS' I/O control routines, device assignment and memory allocation routines, and Peripheral Processor scheduling routines. All File Manager functions can be carried out by a single Peripheral Processor, but the use of additional Processors will increase the File Manager's efficiency.

Files and portions of files (as small as individual records) can be created, stored, displayed, dumped, deleted, and modified temporarily or permanently. In addition, the status of stored files can be determined and logged, and file directories can be altered. The File Manager will be usable with any of the following classes of mass storage devices: magnetic tapes (dumping and reloading only), drums, discs, auxiliary core storage, and data cells.

.17 Other

Mathematical Subroutine Library

Reference: . . . . 6000 Series Computer Systems Manual (preliminary edition).
Date available: . . . . . April 1966.
Description:

The Mathematical Subroutine Library is a part of LIBRIOUS, the 6000 Series Library System of I/O and Utility Systems. The Mathematical library contains a complete set of standard FORTRAN mathematical subroutines that have been specially developed to take advantage of the 6000 Series' advanced hardware. Considerations in the development of these subroutines have included the 60-bit data word, the 8-word instruction stack, the 24 central operating registers, and the 10 Central Processor functional units (see Report Section 260:051). All mathematical subroutines are equally accessible to FORTRAN and ASCENT (Central Processor Assembly System) programmers.

Among the available mathematical subroutines are the following: Square Root, Cube Root, Sin, Tan, Arctan, Arcsin, Exponential, and Logarithm. Report Section 260:161 contains a complete list of the mathematical functions available through use of the FORTRAN-66 language. No details are currently available concerning the execution speeds of these routines.

.18 Application Packages

.181 Linear Programming System (LP-66)

The 6000 Series Linear Programming System includes "technologically current" LP algorithms, a complete control language, and a report writer. LP-66 operates under control of the SIPROS operating system and is implemented in a combination of FORTRAN-66 and ASCENT programming languages. An optimization routine and other selected subroutines are called from the FORTRAN-66 library. The availability date for LP-66 is currently undetermined.

.182 Matrix Algebra

A Matrix Algebra package will be available to 6000 Series users in April 1966. Individual matrix manipulation subroutines are provided to aid in the solution of specific matrix handling problems. The supplied matrix operations include: Move, Transpose, Add, Subtract, Multiply, Invert, Eigenvalues and Eigenvectors, and facilities to solve simultaneous equations.

.183 Statistical Programs

The 6000 Series Statistical Programs package consists of four basic programs;

- Basic Descriptive Statistics — computes mean, standard deviation, third and fourth moments, skewness, kurtosis, and associated standard errors for each of a series of variables.
- Normal Probability Function — computes the ordinate or several other functions of the fail-area probability of the normal distribution N for a given value of an argument.
- Correlation Matrix — generates a matrix whose element a_{ij} is the correlation coefficient between the ith and jth variables. Eigenvalues and eigenvectors of the correlation matrix are also obtained to enable principal-components or factor analysis to be performed.
- Random Number Generator — produces a stream of random, equi-probable decimal digits.

The Statistical Programs Package operates under control of the SIPROS operating system and will be available in March 1966.

.184 PERT

Several PERT programs are available for use with the 6000 Series. The NASA-FORTRAN PERT-TIME II program has been converted for use with the 6000 Series, and a companion PERT-COST program is currently under development. In addition, Control Data will supply its own combined PERT-TIME/COST package which produces the standard PERT-TIME reports plus four PERT-COST reports: management summary, project status, financial plan and status, and manpower loading. Control Data's PERT-TIME will be available in June 1966; PERT-COST will be available in October 1966.

.185 SIMSCRIPT

A compiler for the SIMSCRIPT simulation language will be provided for use with the 6000 Series and will be available in June 1966. No details concerning Control Data's SIMSCRIPT language and compiler are currently available.

PROCESS ORIENTED LANGUAGE: FORTRAN 66

.1 GENERAL

.11 Identity: . . . . Control Data 6000 Series FORTRAN 66.

.12 Origin: . . . . Control Data Corporation

.13 Reference: . . . . FORTRAN 66 Programming System/Reference Manual, No. 60101500A.

.14 Description

Several varieties of the FORTRAN language can be used with the Control Data 6000 Series. Early users of 6000 Series systems were supplied with a FORTRAN IV language and compiler that runs under control of the interim-designed Chippewa operating system. Standard FORTRAN IV language facilities were provided, and compilation speeds up to 12,000 statements per minute were achieved. However, the efficiency of the generated object code was not high, and the many unique features of the 6600 and 6800 Central Processors were not effectively utilized. The language facilities of Chippewa FORTRAN IV include mixed-mode arithmetic, double-precision and complex variables, and the ability to intermix FORTRAN II statements whenever they are not inherently incompatible with FORTRAN IV.

FORTRAN 66, however, is the official FORTRAN language for the Control Data 6000 Series. The FORTRAN 66 compiler has been specifically designed to take full advantage of the 6000 Series hardware. It operates under control of the SIPROS operating system and can utilize the extensive hardware and software facilities of the total system.

FORTRAN 66 LANGUAGE

The FORTRAN 66 language is a greatly expanded, though completely compatible, version of FORTRAN 63, a dialect of FORTRAN IV implemented by Control Data for its 1600 and 3000 Series systems. The widely-used IBM 7090/7094 FORTRAN IV language is basically a compatible subset of FORTRAN 66, yet some incompatibilities do exist. Paragraph .142 lists the few deficiencies of FORTRAN 66 relative to IBM's FORTRAN IV, and Paragraph .143 lists the major extensions of FORTRAN 66 relative to the same 7090/7094 FORTRAN IV language.

For those users who insist on coding in "pure" FORTRAN IV, Control Data has provided its FORTRAN 66 compiler with an optional running mode to handle programs written in ASA-standard FORTRAN IV. When the FORTRAN IV subset-compiler is called for, an expanded diagnostic package can be provided because the FORTRAN IV compiler consumes less space in Central Memory.

Control Data's implementation of FORTRAN 66 includes many of the newest and most powerful features of the FORTRAN language. Special emphasis is placed on both speed of compilation and object program efficiency. Listed below are some of the principal features of the FORTRAN 66 language/compiler.

- FORTRAN 66 includes all FORTRAN 63 facilities; hence, it is compatible with FORTRAN 63 and essentially with FORTRAN IV.
- Assembly-language and FORTRAN 66 statements can be intermixed on a line-for-line level. Total communication between the two source languages is provided. FORTRAN statement numbers can be referred to in ASCENT (Central Processor Assembly System) instructions, and symbolic ASCENT location tags can be referred to in the FORTRAN statements. In a similar fashion, data values computed by ASCENT instructions or generated by pseudo-operations can be referenced as FORTRAN operands, and values computed by FORTRAN procedures can be used as arguments in ASCENT instructions.
- Input-output buffering facilities can be selected to be performed automatically or under control of the FORTRAN programmer. Direct buffer control statements are provided, as well as several statements that check the status of input-output operations and buffer transfer activities.
- Special ENCODE/DECODE statements are included to permit code and radix conversions to be performed while moving data through core storage.
- Central Processor register names can be used directly as operands. This feature permits the programmer to perform computations from the central registers, eliminating the need for many redundant memory accesses. This feature also provides another communications link between the FORTRAN and ASCENT source languages.
- FORTRAN 66 built-in functions and mathematical subroutines utilize specialized coding techniques that maximize the use of the 6000 Series' 60-bit word length and the parallel instruction execution facilities in the 6600 and 6800 Central Processors. Table II lists the basic library functions provided with FORTRAN 66.
- An object code optimization algorithm is provided to permit debugged source programs to be recompiled in a manner that approaches the execution-time efficiency of machine-language-coded programs. When the FORTRAN compilation is performed in the optional optimization mode, the compiler performs simulations of various Central Processor instruction execution sequences in order to determine efficient scheduling of the 10 functional units

.14 Description (Contd.)

and to provide anticipatory loading of the 24 central registers.

Paragraph .143 lists several other important features included in the FORTRAN 66 language.

FORTRAN 66 Compiler

Control Data states that the FORTRAN 66 compiler, when operating in the optimization mode, generates object code that is at least 80% as efficient as good machine coding in the complex 6600/6800 Central Processors. Compilation speeds up to 10,000 statements per minute have been achieved when unoptimized object code is generated. No times are currently available for measuring the compilation speed of the FORTRAN 66 compiler when optimized object code is produced.

Control Data estimates that the size of the complete compiler plus the Central Processor and Peripheral Processor assemblers will be approximately 8 to 12 thousand 60-bit words. The assemblers are normally loaded with the FORTRAN compiler to facilitate the handling of source programs that use intermixed FORTRAN and assembly-language statements. Working storage and symbol table requirements can consume another 12 to 16 thousand words of storage if the compiler is to perform efficiently.

Time-Sharing FORTRAN 66

Included in Control Data's scheduled software for support of integrated Time-Sharing 6000 Series systems is an Interpretive Mode FORTRAN 66 compiler and a companion Machine Mode compiler. The Interpretive Mode FORTRAN compiler will be written in re-entrant coding to permit efficient utilization of core storage and to minimize program swap time. In addition to the full FORTRAN 66 capabilities, the Interpretive Mode FORTRAN system will provide remote terminal users with the following facilities:

- Syntax analysis of the most recently entered FORTRAN statement within an average of three seconds of the statement's entry.
- Interline diagnostics of previously-entered statements, categorizing the errors and indicating the degree of acceptability.
- Start and stop control of the executing program at specified statements.
- Console displays of symbolically-specified variables or arrays, or of the contents of symbolically-specified consecutive memory locations.
- Source statement insertion and deletion at any specified point in the program.
- Listings of program segments or of the entire compiled program.
- Complete system object-program diagnostics that can be displayed on console devices or printed as hard-copy documentation.

The Machine Mode FORTRAN compiler for 6000 Series Time-Sharing systems will provide all of the language facilities of FORTRAN 66 and will particularly emphasize the generation of efficient object code. The Machine Mode compiler will normally not be used until the user at the remote terminal is reasonably certain that the program has been completely debugged.

.141 Availability

Language specifications: . . . . April 1965.
Compiler —
Preliminary version: . . . . December 1965.
Complete version: . . . . April 1966.
Time-sharing version: . . . . 3rd quarter 1967.

.142 Restrictions of FORTRAN 66 Relative to IBM 7090/7094 FORTRAN IV*

(1) Logical constants TRUE and FALSE cannot be defined.

(2) Logical expressions cannot be used as parameters in function definitions or in CALL subroutine statements.

(3) The settings of sense switches and sense lights cannot be altered during a program's execution.

(4) The BLOCK DATA statement is not provided; however, any labelled COMMON data block can be initialized through use of the FORTRAN 66 DATA statement.

.143 Extensions of FORTRAN 66 Relative to IBM 7090/7094 FORTRAN IV*

(1) Numerous language capabilities are extended as indicated in Table I.

(2) Mixed-mode arithmetic is permitted in logical and arithmetic expressions and in the formation of subscripts.

(3) Assembly-language statements can be intermixed with FORTRAN 66 statements.

(4) Hollerith-coded constants are permitted in arithmetic expressions.

(5) Logical bit-by-bit masking of variables by constants or other variables can be performed through use of the AND, NOT, and OR operators.

(6) ENCODE and DECODE statements are implemented to facilitate code and radix conversions.

(7) BUFFER IN and BUFFER OUT statements are included to increase overlapping of input-output data transfers.

(8) Checks for the status of input-output operations by designated I/O units are provided. Variations of the IF statement permit specific checks for operation-complete, operation-incomplete, end-of-file, end-of-tape, and parity errors.

(9) Logical unit numbers can be specified for input-output operations.

* Detailed specifications of the IBM 7090/7094 FORTRAN IV language are provided in Report Section 408:162.

(Contd.)

TABLE I: COMPARATIVE FORTRAN LANGUAGE CAPABILITIES

	FORTRAN 66	FORTRAN IV (7090/7094)
Sense lights:	60 (simulated)	4
Sense switches:	60 (simulated)	6
Integer magnitude:	$2^{59}-1$	$2^{35}-1$
Integer accuracy:	18 digits	10 digits
Single-precision magnitude:	$10^{\pm 308}$	$10^{\pm 38}$
Single-precision accuracy:	15 digits	8 digits
Double-precision magnitude:	$10^{\pm 308}$	$10^{\pm 38}$
Double-precision accuracy:	29 digits	16 digits
Statement numbers:	1 to 99999	1 to 32767
Variable names:	1 to 8 alpha. chars.	1 to 6 alpha. chars.
Continuation cards:	no limit (a statement may have up to 660 operators, delimiters, and identifiers)	1 to 19
Character set:	A-Z; 0-9; 10 symbols; blank	A-Z; 0-9; 9 symbols (no $); blank
Multiple replacement statements:	yes	no
Multiple statements per line:	yes	no

.143 Extensions of FORTRAN 66 Relative to IBM 7090/7094 FORTRAN IV (Contd.)

(10) Subroutines can be entered at any specified entry points.

(11) In the logical IF statement, an explicit destination can be specified for the false condition as well as for the true condition.

(12) Complex expressions can be used in the three-way branching IF statement, although only the real part is tested for zero.

(13) The control variables within a DO loop can be dynamically altered during the execution of the loop. In addition, primary DO loop control is tested before the loop is initially entered, permitting all passes through the loop to be bypassed when appropriate.

TABLE II: STANDARD FORTRAN 66 LIBRARY FUNCTIONS

Form	Definition	Actual Parameter Type	Mode of Result
ABSF(X)	Absolute Value	Real	Real
XABSF(i)	Absolute Value	Integer	Integer
INTF(X)	Truncation, integer	Real	Real
XINTF(X)	Truncation, integer	Real	Integer
MODF(X_1, X_2)	X_1 modulo X_2	Real	Real
XMODF(i_1, i_2)	i_1 modulo i_2	Integer	Integer
MAX0F(i_1, i_2, ...)	Determine maximum argument	Integer	Real
MAX1F(X_1, X_2, ...)	Determine maximum argument	Real	Real
XMAX0F(i_1, i_2, ...)	Determine maximum argument	Integer	Integer
XMAC1F(X_1, X_2, ...)	Determine maximum argument	Real	Integer
MIN0F(i_1, i_2, ...)	Determine minimum argument	Integer	Real
MIN1F(X_1, X_2, ...)	Determine minimum argument	Real	Real
XMIN0F(i_1, i_2, ...)	Determine minimum argument	Integer	Integer
XMIN1F(X_1, X_2, ...)	Determine minimum argument	Real	Integer
SINF(X)	Sine X, radians	Real	Real
COSF(X)	Cosine X, radians	Real	Real
TANF(X)	Tangent X, radians	Real	Real
ASINF(X)	Arcsine X, radians	Real	Real
ACOSF(X)	Arccos, X, radians	Real	Real
ATANF(X)	Arctangent X, radians	Real	Real
TANHF(X)	Hyperbolic tangent X, radians	Real	Real
SQRTF(X)	Square root of X	Real	Real
LOGF(X)	Natural log of X	Real	Real
EXPF(X)	e to Xth power	Real	Real
SIGNF(X_1, X_2)	Sign of X_2 times $\|X_1\|$	Real	Real
XSIGNF(i_1, i_2)	Sign of i_2 times $\|i_1\|$	Integer	Integer
DIMF(X_1, X_2)	If $X_1 > X_2$: $X_1 - X_2$ If $X_1 \leq X_2$: 0	Real	Real
XDIMF(i_1, i_2)	If $i_1 > i_2$: $i_1 - i_2$ If $i_1 \leq i_2$: 0	Integer	Integer
CUBERTF(X)	Cube root of X	Real	Real
FLOATF(I)	Integer to Real conversion	Integer	Real
RANF(N)	Generate random number	–Real –Integer	Real
	(Repeated executions give uniformly distributed numbers)	+Real +Integer	Integer
XFIXF	Real to Integer conversion	Real	Integer
POWER(X_1, X_2)	$X_1^{X_2}$	Real, Real	Real
ITOJ(I, J)	I^J	Integer, Integer	Integer
XTOI(X, I)	X^I	Real, Integer	Real
ITOX(I, X)	I^X	Integer, Real	Real
LENGTHF(i)	Number of words read on unit i	Integer	Integer

PROCESS ORIENTED LANGUAGE: COBOL

.1 GENERAL

.11 Identity: . . . . 6000 Series COBOL.

.12 Origin: . . . . unspecified subcontractor.

.13 Reference: . . . . Control Data 6000 Series Preliminary Technical Information Manual.

.14 Description

Control Data plans to supply for its 6000 Series systems a COBOL language that will include all the features of COBOL-61 Extended, plus all the language facilities of COBOL-65 as recently approved by the Department of Defense. The COBOL compiler will be written by an independent software house and will probably be available in mid-1967. Like all other software systems provided for use with the 6000 Series, the COBOL compiler will utilize the facilities of and operate under control of the SIPROS operating system in a multiprogramming environment.

A complete listing of language specifications for 6000 Series COBOL has not been released to date. However, Control Data has offered the following language features as representative samplings from the extensive facilities to be provided in its new COBOL language:

- The SEGMENTATION feature allows the programmer to subdivide his program into various logical segments. When the executing object program requires additional program segments, they are loaded automatically by the SIPROS operating system.
- The library control statements COPY and INCLUDE permit access to an open-ended COBOL library. These statements enable stored portions of the Environment, Data, and Procedure Divisions to be retrieved from the library at compilation time and to be inserted in line with the source program.
- The source-language debugging verbs MONITOR, TRACE, and DUMP provide comprehensive diagnostics at programmer-specified points during the execution of the object program.
- The COBOL user can specify the collating sequence to be followed during the execution of each object program. This facility will ease the conversion problems normally encountered when attempting to compile and execute COBOL programs written for computers with internal characteristics that differ from the compiling computer.
- The SEARCH verb and its several options facilitate table lookup operations.
- The SET verb provides the user with direct control of the central processor's 24 operating registers.
- The Report Writer package permits the programmer to generate printed reports by simple data and report format specifications. The verbs GENERATE, INITIATE, and TERMINATE control the Report Writer's operations.
- The Mass Storage File Descriptor and several new input-output verbs provide the COBOL programmer with direct control over the storage and retrieval of data files written on mass storage devices.
- The ADD, SUBTRACT, and MOVE verbs include the CORRESPONDING option.
- The SAME AREA clause permits the programmer to specify that two or more files are to use the same input-output memory area.
- The special symbols ** and ↑ specify exponentiation in arithmetic expressions, and the symbols $\leq$ and $\geq$ can be used in relational expressions.

Control Data's 6000 Series COBOL will also implement a number of features originally listed as "electives" in the D.O.D. COBOL-61 language specifications. Table I presents a partial list of these features.

Compiler

The 6000 Series COBOL compiler will be a three-pass translator, including an optional object-code optimization pass. The compiler will emphasize efficiency, both in the compilation process and in the object code generated. Control Data expects that compilation speeds of up to 6,000 statements per minute will be achieved when compiling on the 6600 computer system.

.141 Availability

Language: . . . . ?
Compiler: . . . . mid-1967.

TABLE I: PARTIAL LIST OF COBOL-61 ELECTIVES TO BE IMPLEMENTED IN 6000 SERIES COBOL

Key No.*	Elective	Comments
	Characters and Words	
1	Formula characters	+, −, *, /, **, ↑.
2	Relationship characters	=, >, <, ≤, ≥.
3	Semicolon	Can be used for punctuation.
4	Long literals	Maximum size is 4,095 characters.
5	Figurative constants	HIGH or LOW BOUND(S) are available.
6	Figurative constants	HIGH or LOW VALUE(S) are available.
	Record Description	
14	Item length	Variable-length items can be specified.
20	Conditional ranges	VALUES can be ascribed to conditionals.
	Verbs	
22	COMPUTE	Algebraic formulas can be used.
24	ENTER	Non-COBOL languages can be entered.
25	INCLUDE	Library routines can be called.
26	USE	Non-standard I/O error and label handling routines can be used.
	Verb Options	
27	LOCK	Locks rewound tapes and files on disc storage.
28	MOVE CORRESPONDING	Commonly named items in a group can be moved.
30	ADVANCING	Paper advance can be specified.
32	Formulas	Algebraic formulas can be used.
37	Complex conditionals	ANDs and ORs can be intermixed.
38	Complex conditionals	Nested conditionals can be used.
39	Conditional statements	IF, SIZE ERROR, AT END, ELSE (OTHERWISE) can be followed by an imperative statement.
	Environment Division	
40	SOURCE-COMPUTER	Computer description can be given, with MEMORY SIZE specification.
41	OBJECT-COMPUTER	Computer description can be given, with MEMORY SIZE specification.
42	SPECIAL-NAMES	Hardware devices and their status conditions can be assigned special names.
43	FILE-CONTROL	Library descriptions can be copied.
45	I/O CONTROL	Library control sections can be copied.
	Special Features	
48	Library	Library routines can be called.
49	Segmentation	Program segmentation is permitted.

* See Users' Guide, page 4:161.300.

MACHINE ORIENTED LANGUAGE: ASCENT

.1 GENERAL

.11 Identity: . . . . ASCENT — Assembly System, CENTral Processor.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . ASCENT Programming System/Reference Manual, No. 60101600A.

.14 Description

.141 General Facilities

The ASCENT language is a symbolic, machine-oriented language that is used in writing assembly-language-level programs for the Central Processors of 6000 Series computer systems. Peripheral Processor programs are written in another assembly language, ASPER, which is described in Report Section 260:172. ASCENT provides the programmer with direct, simplified acess to the 6000 Series hardware features and to the many system control facilities of the SIPROS operating system (described in Report Section 260:191).

Among the most useful features of the ASCENT assembly system are the following:

- Use of a powerful and flexible macro-instruction system that will reduce the time required for program coding.
- Provisions to relegate all input-output control operations to the SIPROS operating system.
- Use of a pseudo-operation system for assembler control.
- Ability to intermix ASCENT and FORTRAN statements on a line-for-line basis. Both ASCENT and FORTRAN refer to the 24 Central Processor registers by the same register names.
- Ability to call ASPER Peripheral Processor routines from a library or from own-coding appended to the ASCENT program.
- Access to a complete subroutine library, the contents of which are called during program execution.

.142 Instruction Format

The ASCENT language uses one basic instruction format that consists of an 8-character instruction location symbol (optional), a variable-length Opcode (operation code) field, and up to two symbolic addresses or literals. Provision is also made for inclusion of the programmer's comments. Up to six symbolic instructions can be placed on each source card.

The mnemonic Opcode generally consists of a one- or two-letter symbolic code and a Central Processor register designation which indicates the register that is to receive the action or the result of the instruction. The address fields can contain the actual names of the central registers to be used in executing the instruction. Thus, the ASCENT instruction.

SA3 = X5 + B2

is interpreted as meaning Set Address Register 3 equal to the sum of the contents of Operand (X) Register 5 and Index (B) Register 2. This example also illustrates the way in which the arithmetic operators +, -, *, and / can be used in conjunction with an abbreviated mnemonic code to define a computational operation. These operators can also be used in address modification operations. Mnemonic operation codes are provided for every Processor instruction.

Many instructions include the facility for use of literals. Literal data can assume any of the following forms:

- Constant — decimal integers, octal digits, single-precision floating-point, complex, or double-precision floating-point.
- Symbol — any arrangement of numbers and letters that contains no more than 8 characters.
- Symbol ±I — where I is an integer, octal, or symbolic constant.
- Symbol-Symbol — another form of address modification.

Table I presents sample coding in the ASCENT assembly language, illustrating various types of symbolic Central Processor instructions.

.143 Macro Instructions

The ASCENT language provides a full complement of system macros and facilities to permit the use of user-supplied macro-instructions. The system macro-instructions provide the communication links between a Central Processor program and the ten Peripheral Processors. Most system macros give the programmer the capability to direct the system's input-output operations, but other macros are available to request equipment assignment, to check the status of external operations, to control the use of program overlays, and to coordinate the interrelationships that can exist between Central Processor and Peripheral Processor programs. Table II lists the standard system macros supplied with the ASCENT assembly system.

As an aid to efficient multiprogramming, each system macro can be executed in a buffered or non-buffered mode. In the non-buffered mode, with the letter "W" appended to the macro code, the associated Central Processor Program waits until the macro-operation is completed or aborted. (Control is transferred to SIPROS during this delay, permitting other Central Processor programs to be initiated.) In the buffered mode, the macro code is

TABLE I: SAMPLE ASCENT CODING

LOCATION	INSTRUCTION	REMARKS
	BX6 X1	.X1 TO X6
START	BX4 —X3	.—X3 TO X4
	FX7 X6*X4	.FLOATING X6*X4 to X7
	BX3 —X4 + X1	.X1 + COMP. X4 TO X3
	EQ B5 B2 AB	.IF B5 = B2, GO TO AB
	SA7 B2 + DATA	.STORE X7 TO DATA + B2
	SA7 DATA	.STORE X7 TO B0 + DATA
	NZ X1 ABC	.IF X1 NOT ZERO, GO TO ABC
	RJ SUB	.RETURN JUMP TO SUB
START1	RDC 1, ST, (BA), (BA + 8), 8, 2	.LIST
	SB1 1 $ SA2 DATA + 1	.PACKED CARD
START2	LX1 6 $ MX2 48 $ JP AB + 2	.MAXIMUM 6 PER CARD
	SB6 —8 $ SA5 B6 + DATA $ SB7 B5—B6	.BEGIN REMARKS WITH PERIOD
	JP B2 + BETA	.JUMP TO B2 + BETA

TABLE II: ASCENT SYSTEM MACRO INSTRUCTIONS

Code	Meaning
RQTW	Request tape assignment from system.
DRTW	Release tape back to system.
SFFW	Search file mark forward.
SFBW	Search file mark backward.
WFMW	Write file mark.
RWLW	Rewind tape to load point.
RWUW	Rewind tape for unload.
FSPW	Forespace.
BSPW	Backspace.
RFCW	Read tape forward coded mode.
RFBW	Read tape forward binary mode.
WRCW	Write tape coded mode.
WRBW	Write tape binary mode.
RDHW	Read record and hold data on disc.
RDRW	Read record and release data on disc.
WRDW	Write record on disc.
SSPW	Single space printer.
DSPW	Double space printer.
FC7W	Select Format Channel 7.
FC8W	Select Format Channel 8.
MC1W	Select Monitor Channel 1.
MC2W	Select Monitor Channel 2.
MC3W	Select Monitor Channel 3.
MC4W	Select Monitor Channel 4.
MC5W	Select Monitor Channel 5.
MC6W	Select Monitor Channel 6.
CMCW	Clear Monitor Channels 1 – 6.
SPAW	Suppress space after next print.
PRNW	Print single line or multiple lines.
PCHW	Punch cards.
RDCW	Read cards.
DSRW	Display on right scope for system time limit.
DSLW	Display on left scope for system time limit.
DHRW	Display on right scope and hold indefinitely.
DHLW	Display on left scope and hold indefinitely.
RDPW	Remove display.
RTYW	Read console typewriter.
WAIW	Check status word.
TPPW	Transfer program SYMBOL from CM to PP memory and begin execution with first ASPER instruction.
ROMW	Request memory.
DRMW	Release memory.
RQDW	Request disc space.
DRDW	Release disc space.
LOAD	Load segment SYMBOL.

.143 Macro Instructions (Contd.)

used without the letter "W". In this case the program that initiated the system macro can continue processing while the macro-operation is concurrently being processed in a Peripheral Processor. In the buffered mode of operation, the Central Processor program must do its own checking to determine when the asynchronously-processed macro-operation has been completed.

The programmer can define his own macro routines through the use of a few simple pseudo-operation statements. After the new routine is named and its list of parameters specified, the programmer codes the macro routine in exactly the same manner as he codes the other sections of the ASCENT program.

.144 Pseudo-Instructions

The ASCENT language includes conventional assembler-control statements to provide the programmer with some control over the operations of the assembler and over the form and contents of its output. Several pseudo-operations are also provided to direct the assembler to perform specified code and radix conversion operations on lists of data. Table III is a list of the standard pseudo-operations available with the ASCENT assembler.

.145 ASCENT Translator

The ASCENT translator (i.e., the program that performs the assembly) operates under the control of SIPROS in the standard 6000 Series multiprogramming and multiprocessing environments. Because a single translator program is used throughout the 6000 Series, identical (and therefore unoptimized) object code is produced for the 6400 Central Processor and the more advanced 6600/6800 Central Processors. The listing generated by the translator includes conventional assembly-language error indications. It also includes an assembly summary report that provides information such as the number of errors detected, the number

(Contd.)

TABLE III: ASCENT PSEUDO-INSTRUCTIONS

OPCODE	MEANING
ASCENT	Defines CP program
END	Defines end of CP program
ASPER	Defines PP routine
SUBROUTINE	Defines subroutine name
BSSD	Reserves disc space
BSS	Reserves Central Memory region
BSSZ	Reserves Central Memory region and presets it to zero
EQU	Equates a symbol to a value
DPC	Inserts display-coded characters into program
BCD	Inserts BCD characters into program
CON	Defines constants in program
LIST	Controls side-by-side listing
SPACE	Spaces side-by-side listing
EJECT	Ejects page on side-by-side listing

.145 ASCENT Translator (Contd.)

of symbols assigned, the length of the ASCENT program, the lengths of any ASPER programs that may have been included, and a list of symbols that are undefined, duplicated, or not referenced.

.15 Publication Date: . . . . April 1965.

.16 Delivery Date: . . . . . . ?

.2 LANGUAGE FORMAT

.21 Diagram: . . . . see Table I for an example of ASCENT coding.

.22 Legend

Location: . . . . assigns a symbolic name to a statement.

Instruction —
Opcode: . . . . defines a machine instruction code or a pseudo-code.
Address: . . . . supplies the instruction with appropriate operands that consist of either a register name, two register names connected by an arithmetic operator, or a register name and a constant connected by an operator.
Remarks: . . . . used only for programmer-supplied comments.

.23 Corrections: . . . . no special provisions.

.24 Special Conventions

.241 Compound addresses: . joined by the arithmetic operators +, -, *, and /.
.242 Multi-addresses: . . . . separated by the space character.
.243 Literals: . . . . enclosed within parentheses.
.244 Special coded addresses: . . . . * represents the current value of the location counter.
.245 Others: . . . . $ indicates the start of the next instruction on a multiple-instruction source card.

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . determined by individual installations.
.312 Common label formation rule: . . . . yes; 8 or fewer alphameric characters.
.313 Reserved labels —
For operand registers: . . . . X_0 through X_7.
For index registers: . B_0 through B_7.
For address registers: . . . . A_0 through A_7.
.314 Other restrictions: . . . none.
.315 Designators: . . . . none.
.316 Synonyms permitted: . . yes; EQU pseudo.

.32 Universal Labels

Existence: . . . . mandatory if referenced by another instruction.
Formation rule —
First character: . . . . alphabetic.
Last character: . . . alphameric.
Others: . . . . alphameric.
Number of characters: . . . . . 1 to 8.

.33 Local Labels

Region: . . . . all library routines and all routines that are local to a subprogram or overlay segment.
Existence: . . . . . . mandatory if referenced by another instruction.
Formation rule: . . . same as for universal labels.

.4 DATA

.41 Constants

.411 Maximum size constants:
Integer —
Decimal: . . . . 18 decimal digits.
Octal: . . . . 20 octal digits.
Fixed numeric: . . . . not available.
Floating numeric (single precision) —
Decimal: . . . . 15 and 3 decimal digits.
Floating numeric (double precision) —

.411 Maximum size constants: (Contd.)
Decimal: . . . . 29 and 3 decimal digits.
Complex numeric —
Decimal: . . . . 2 single-precision floating-point numbers.
Alphabetic: . . . . not available.
Alphameric: . . . . . . not available.
.412 Maximum size literals: same as constants; see Paragraph .411.

.42 Working Areas

.421 Data layout —
Implied by use: . . . . no.
Specified in program: yes, by use of macro instructions.
.422 Data type: . . . . tabulated in program.
.423 Redefinition: . . . . not possible.

.43 Input-Output Areas

.431 Data layout: . . . . defined in pseudo and macro instructions.
.432 Data type: . . . . defined in macro instructions.
.433 Copy layout: . . . . not available.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence: . . . . alternative.
Number: . . . . 84.
Example: . . . . RJ — Return Jump.
.512 Absolute —
Existence: . . . . alternative.
Number: . . . . 71.
Example: . . . . 10 — Move X_j to X_i.

.52 Macro-Codes

.521 Number available —
Input-output: . . . . . . 43.
Arithmetic: . . . . none.
Math functions: . . . . none.
Error control: . . . . . 1.
Restarts: . . . . none.
.522 Examples —
Simple: . . . . SFF — Search File Mark Forward.
Elaborate: . . . . TPP — Transfer control from Central Memory program to a Peripheral Processor program.
.523 New macros: . . . . inserted through use of MACRO pseudo-instruction.
.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control —
Allocation counter: . . EQU pseudo instruction.
Label adjustment: . . by arithmetic operators and literal or symbolic data.
Annotation: . . . . Remarks field on coding sheet.
.542 Allocation counter —
Set to absolute: . . . . not possible.
Set to label: . . . . . . EQU pseudo instruction.
Step forward: . . . . . not possible.
Step backward: . . . . not possible.
Reserve area: . . . . . BSS and BSSZ.
.543 Label adjustment —
Set labels equal: . . . . EQU.
Set absolute value: . . not possible.
Clear label table: . . . ?
.544 Annotation —
Comment phrase: . . . written alongside the symbolic instruction.
Title phrase: . . . . . . included in header card.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: . . . none.

.62 Special Functions

.621 Facilities: . . . . standard FORTRAN functions are available in the subroutine library.
.622 Method of call: . . . . . . CALL pseudo-instructions.

.63 Overlay Control

.631 Facilities: . . . . each Central Processor program can have a basic segment and one additional segment residing in Central Memory at any given time. Further segments must be overlaid as required.
.632 Method of call: . . . . . . LOAD pseudo-operation.

.64 Data Editing

.641 Radix conversion: . . . binary to decimal; decimal to binary.
.642 Code translation: . . . . BCD to or from Hollerith; BCD to or from Display Code.
.643 Format control: . . . . . own coding required.

.65 Input-Output Control: . handled by system macro-instructions.

.66 Sorting: . . . . not available in ASCENT language.

.67 Diagnostics: . . . . no object-program diagnostics can be embedded through ASCENT instructions.

.7 LIBRARY FACILITIES

.71 Identity: . . . . System Disk Library.

.73 Storage Form: . . . . . . disc file.

.74 Varieties of Contents: . SIPROS system control and I/O routines; system and user-supplied subroutines.

.75 Mechanism

.751 Insertion of new item: . . . . ?
.752 Language of new item: . . . . ASCENT, ASPER, and/or FORTRAN.
.753 Method of call: . . . . . . CALL pseudo-operation.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: . . . . yes.
.764 Closed routines appear once: . . . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . see Table II.

.82 Pseudos: . . . . see Table III.

MACHINE ORIENTED LANGUAGE: ASPER

.1 GENERAL

.11 Identity: . . . . ASPER — Assembly System, PERipheral Processors.

.12 Origin: . . . . Control Data Corporation.

.13 Reference: . . . . ASPER Programming System/Reference Manual, No. 60101700A.

.14 Description

.141 General Facilities

The ASPER language is a symbolic, machine-oriented language that is used in writing assembly-language-level programs for the ten Peripheral and Control Processors that are included in every 6000 Series computer system. Central Processor assembly-language programming is done in the ASCENT language (described in Report Section 260:171).

It is generally not necessary for users to write programs for the Peripheral Processors because their tasks are usually directly assigned by the SIPROS operating system. However, direct programming of these Processors in the ASPER language can be desirable if, for example, a specialized, independently-operating utility routine is planned, or if non-standard supporting tasks are to be assigned to the Peripheral Processors to operate asynchronously with the main Central Processor program.

Some of the principal features of the ASPER assembly system are the following:

- Access to all symbols within the ASCENT or FORTRAN source-language Central Processor program with which the ASPER program is associated. This facility also provides access to variables in COMMON Central Memory storage.
- Ability to reserve storage blocks in Central Memory for private use by the associated Peripheral Processor program.
- An overlay control system to assist in the efficient utilization of the relatively small Peripheral Processor memory units (4,096 12-bit words each).
- A macro instruction system to permit the use of other Peripheral Processors in performing system-supervised input-output operations.
- Other system macros to request loading of other Peripheral Processor programs, a facility that permits each Peripheral Processor to share in the system control functions of the SIPROS operating system.

.142 Instruction Format

The ASPER language uses one basic instruction format that includes an optional 8-character instruction location symbol, a mnemonic or machine language Opcode, an address field (whose content and length vary according to the type of instruction), and a remarks field for programmer's comments. The address portion of the instruction can consist of a symbol, a symbol modified by the arithmetic operators + and - used in conjunction with a constant, a symbol minus another symbol, or a simple constant. Up to six symbolic instructions can be placed on each source card.

The third letter of the three-letter mnemonic operation code designates the type of address that is to be used in interpreting the symbolic instruction, as shown below:

Mnemonic ends in —

N: . . . . no address; direct 6-bit operand.
D: . . . . direct address.
I: . . . . indirect address.
M: . . . . indexed direct address.
C: . . . . no address; direct 18-bit operand.

A complete list of the standard ASPER symbolic Peripheral Processor instructions is shown on page 260:121.102, in the Instruction List section. Of the 62 listed instructions, it should be noted that most fall into a few basic functional categories such as Add, Subtract, Load, etc. The repertoire is not exceptionally rich.

.143 Macro-Instructions

The ASPER language provides a comprehensive set of system macro-instructions that, in conjunction with the pseudo-instructions, serve to integrate the ASPER program into the overall 6000 Series system and to coordinate the functions of the ASPER program with the many control functions of the SIPROS operating system. Specifically, the system macros provide direct communication links between the ASPER routine and the system-control Peripheral Processors in which various parts of SIPROS reside. (See Report Section 260:191 for a description of the SIPROS system.)

The ASPER macro-instructions direct SIPROS to perform input-output operations, to assign I/O devices and reserve core storage areas, to check the status of external operations, to load program overlays, and to provide scheduling services for use of the I/O channels. Table I lists the standard ASPER system macros and identifies their usage.

Most of the system macros provide a choice of buffered or non-buffered modes of operation. In the non-buffered mode, with the letter "W" appended to the macro operation code, the processing is discontinued until the macro-initiated operation is completed or aborted. In the buffered mode, without the addition of "W" to the macro code, the ASPER routine continues processing while the

TABLE I: ASPER SYSTEM MACRO-INSTRUCTIONS

Code	Meaning
RQTW	Request tape assignment from system
DRTW	Release tape back to system
SFFW	Search file mark forward
SFBW	Search file mark backward
WFMW	Write file mark
RWLW	Rewind tape to load point
RWUW	Rewind tape for unload
FSPW	Forespace
BSPW	Backspace
RFCW	Read tape forward coded mode
RFBW	Read tape forward binary mode
WRCW	Write tape coded mode
WRBW	Write tape binary mode
RDHW	Read record and hold data on disc
RDRW	Read record and release data on disc
WRDW	Write record on disc
SSPW	Single space printer
DSPW	Double space printer
FC7W	Select Format Channel 7
FC8W	Select Format Channel 8
MC1W	Select Monitor Channel 1
MC2W	Select Monitor Channel 2
MC3W	Select Monitor Channel 3
MC4W	Select Monitor Channel 4
MC5W	Select Monitor Channel 5
MC6W	Select Monitor Channel 6

Code	Meaning
CMCW	Clear Monitor Channels 1 — 6
SPAW	Suppress space after next print
PRNW	Print single line or multiple lines
PCHW	Punch cards
RDCW	Read cards
DSRW	Display on right scope for system time limit
DSLW	Display on left scope for system time limit
DHRW	Display on right scope and hold indefinitely
DHLW	Display on left scope and hold indefinitely
RDPW	Remove display
RTYW	Read console typewriter
WAIW	Check status word
TPPW	Transfer program SYMBOL from CM to PP memory and begin execution with first ASPER instruction
RQMW	Request memory
DRMW	Release memory
RQDW	Request disk space
DRDW	Release disk space
RQCW	Request I/O channel
DRCW	Release I/O channel
DRPP	Release Peripheral Processor
LOAD	Load segment SYMBOL

.143 Macro-Instructions (Contd.)

macro-initiated routine is being processed asynchronously in another Peripheral Processor. In the buffered mode, the ASPER routine must perform its own checks to determine when the macro-operation is completed.

Facilities to provide programmer-defined macro routines are not implemented in the ASPER language.

.144 Pseudo-Instructions

The 17 standard ASPER pseudo-instructions provide the means for the programmer to direct the assembler to perform certain functions. Among the functions controlled by these pseudo-instructions are overlay and subroutine identification and definition, memory assignments according to type (absolute or relocatable), reservation of storage areas on the System Disk and in specified areas of Peripheral Processor and Central Memory, conversion of data codes and radices, and formatting of the output assembly listing. A listing of the ASPER pseudo-instructions is presented in Table II.

.145 ASPER Translator

Like all standard 6000 Series software packages, the ASPER translator (or assembler) operates under the supervision of SIPROS in a multiprogramming and multiprocessing environment. The listing generated by the translator includes conventional assembly-language error indications. It also includes an assembly summary report that provides information such as the number of errors detected, the number of symbols assigned, the length of the associated ASCENT Central Processor program, the length of the ASPER program, and a list of symbols that are undefined, duplicated, or not referenced.

.15 Publication Date: . . . . April 1965.

.16 Delivery Date: . . . . . . ?

.2 LANGUAGE FORMAT

.21 Diagram

Location	Opcode Address	Remarks

.22 Legend

Location: . . . . assigns a symbolic name to a statement.

Opcode: . . . . defines a machine instruction code, a macro code, or a pseudo code.

Address: . . . . specifies a direct or indirect operand address, or a direct operand.

Remarks: . . . . used for programmer-supplied comments.

.23 Corrections: . . . . no special provisions.

.24 Special Conventions

.241 Compound addresses: . joined by the arithmetic operators + and -.

.242 Multi-addresses: . . . . not permitted.

.243 Literals: . . . . enclosed within parentheses.

.244 Special coded addresses: . . . . * represents the current value of the location counter.

.245 Others: . . . . $ indicates the start of the next instruction on a multiple-instruction source card.

(Contd.)

TABLE II: ASPER PSEUDO-INSTRUCTIONS

OPCODE	MEANING
ASPER	Defines PP program
SUBP	Defines overlay
ORG	Assigns program words to direct locations, nonrelocatable
ORGR	Assigns program words to nondirect locations, relocatable
BSSD	Reserves disc space
BSS	Reserves Peripheral Memory region
BSSZ	Reserves Peripheral Memory region and presets it to zero
BSSCM	Reserves Central Memory region
EQU	Equates a symbol to a value
DPC	Inserts display-code characters into program
BCD	Inserts BCD characters into program
CON	Constructs 12-bit constants
COND	Constructs 18-bit constants
END	Defines end of PP program
LIST	Controls side-by-side listing
SPACE	Spaces side-by-side listing
EJECT	Ejects page on side-by-side listing

.3 LABELS

.31 General

.311 Maximum number of labels: . . . . determined by individual installations.
.312 Common label formation rule: . . . . yes; 8 or fewer alphameric characters.
.313 Reserved labels: . . . . none.
.314 Other restrictions: . . . none.
.315 Designators: . . . . none.
.316 Synonyms permitted: . yes; EQU pseudo.

.32 Universal Labels

.321 Labels for procedures —
Existence: . . . . mandatory if referenced by another instruction.
Formation rule —
First character: . . . . . alphabetic.
Last character: . . . . . . alphameric.
Others: . . . . alphameric.
Number of characters: . 1 to 8.
.322 Labels for library routines: . . . . same as procedures.
.323 Labels for constants: . same as procedures.
.324 Labels for files: . . . . same as procedures.
.325 Labels for records: . . same as procedures.
.326 Labels for variables: . same as procedures.

.33 Local Labels

.331 Region: . . . . local to a subprogram or overlay segment.
.332 Labels for procedures —
Existence: . . . . mandatory if referenced by another instruction.
Formation rule: . . . . same as for universal labels.
.333 Labels for library routines: . . . . library routines are always universal.
.334 Labels for constants: . same as procedures.
.335 Labels for files: . . . . same as procedures.
.336 Labels for records: . . same as procedures.
.337 Labels for variables: . same as procedures.

.4 DATA

.41 Constants

.411 Maximum size constants:
Integer —
Decimal: . . . . 0 through 4,095.
Octal: . . . . 4 octal digits.
Fixed numeric: . . . . not available.
Floating numeric: . . not available.
Alphabetic: . . . . not available.
Alphameric: . . . . . . not available.
.412 Maximum size literals: . . . . same as constants; see Paragraph .411.

.42 Working Areas

.421 Data layout —
Implied by use: . . . . no.
Specified in program: yes, by use of macro-instructions.
.422 Data type: . . . . tabulated in program.
.423 Redefinition: . . . . not possible.

.43 Input-Output Areas

.431 Data layout: . . . . defined in pseudo and macro instructions.
.432 Data type: . . . . defined in macro instructions.
.433 Copy layout: . . . . not available.

.5 PROCEDURES

.51 Direct Operation Codes

.511 Mnemonic —
Existence: . . . . alternative.
Number: . . . . 62.
Example: . . . . RAM — Replace Add to Memory.
.512 Absolute —
Existence: . . . . alternative.
Number: . . . . 64.
Example: . . . . 02 — Return Jump.

.52 Macro-Codes

.521 Number available —
Input-output: . . . . . . 41.
Arithmetic: . . . . none.
Math functions: . . . . none.
Error control: . . . . . 1.
Restarts: . . . . none.
Memory assignment control: . . . . 2.
Processor assignment control: . . . . 1.
Segment loading control: . . . . 2.

.522 Examples —
Simple: . . . . SFF — Search File Mark Forward.
Elaborate: . . . . TPP — Transfer control from Central Memory program to a Peripheral Processor program.

.523 New macros: . . . . not available.

.53 Interludes: . . . . none.

.54 Translator Control

.541 Method of control —
Allocation counter: . . EQU pseudo-instruction.
Label adjustment: . . by arithmetic operators (+ and - only) and symbolic data.
Annotation: . . . . Remarks field on coding sheet.

.542 Allocation counter —
Set to absolute: . . . . not possible.
Set to label: . . . . . . EQU pseudo-instruction.
Step forward: . . . . . not possible.
Step backward: . . . . not possible.
Reserve area: . . . . . use of ORG, ORGR, and several other pseudo-instructions.

.543 Label adjustment —
Set labels equal: . . . EQU pseudo-instruction.
Set absolute value: . . use of ORG pseudo-instruction.
Clear label table: . . . ?

.544 Annotation —
Comment phrase: . . . written alongside the symbolic instruction.
Title phrase: . . . . . . use of ASPER and SUBP header cards.

.6 SPECIAL ROUTINES AVAILABLE

.61 Special Arithmetic: . . none.

.62 Special Functions

.621 Facilities: . . . . Central Processor programs and ASPER macro routines can be processed asynchronously with the ASPER program.

.622 Method of call: . . . . . system macro codes.

.63 Overlay Control

.631 Facilities: . . . . any number of defined overlay segments can be called in during execution of ASPER program.

.632 Method of call: . . . . . LOAD macro-instruction.

.64 Data Editing

.641 Radix conversion: . . . binary to decimal; decimal to binary.

.642 Code translation: . . . . BCD to or from Hollerith; BCD to or from Display Code.

.643 Format control: . . . . . own coding required.

.644 Method of call: . . . . . handled by system macro instructions.

.66 Sorting: . . . . not available in ASPER language.

.67 Diagnostics: . . . . no object-program diagnostics can be embedded through ASPER instructions.

.7 LIBRARY FACILITIES

.71 Identity: . . . . System Disk Library.

.73 Storage Form: . . . . disc file.

.74 Varieties of Contents: . SIPROS system control and I/O routines; system subroutines.

.75 Mechanism

.751 Insertion of new item: . ?
.752 Language of new item: ASPER.
.753 Method of call: . . . . . SUBProgram pseudo-instruction.

.76 Insertion in Program

.761 Open routines exist: . . yes.
.762 Closed routines exist: . yes.
.763 Open-closed is optional: . . . . yes.
.764 Closed routines appear once: . . . . yes.

.8 MACRO AND PSEUDO TABLES

.81 Macros: . . . . see Table I.

.82 Pseudos: . . . . see Table II.

OPERATING ENVIRONMENT: SIPROS

.1 GENERAL

.11 Identity: . . . . SIPROS — SImultaneous PRocessing Operating System.

.12 Description

.121 General Facilities

Control Data's Simultaneous Processing Operating System (SIPROS) is a comprehensive control system designed to coordinate the parallel and independent operations of the multiple-processor, multiprogramming 6000 Series systems. SIPROS has been advertised as the official 6000 Series operating system, designed to supplant the "Chippewa" operating system that was supplied to early 6000 Series users as an interim system. However, the basic facilities originally provided by Chippewa have been improved and expanded by both Control Data and the early 6000 Series users. At the request of its users, Control Data is currently re-evaluating the entire software problem. The ultimate form and content of 6000 Series software are, therefore, undetermined at present.

SIPROS provides the control routines necessary to supervise the execution of many main programs or program segments residing in Central Memory and the concurrent execution of independently-functioning programs in each of the ten Peripheral and Control Processors that are basic to every 6000 Series system. The standard version of SIPROS controls stacked-job processing of a large number of programs scheduled on the System Disk. Specialized executive routines can be supplied for conversational-mode remote terminal processing; these special-purpose routines are integrated into the SIPROS system and can utilize the many general-purpose SIPROS facilities. The full version of the standard SIPROS operating system is scheduled for delivery in April 1966. An improved and expanded version of SIPROS, designed specifically for control of remote-console time-sharing operations, is scheduled for delivery during the third quarter of 1967. The general facilities of Time-Sharing SIPROS are described in Paragraph .125 of this report section.

The major objective of SIPROS is to handle dynamically-changing situations in which many jobs are being processed concurrently, with input-output operations, computations, compilations, and system and program testing operations being simultaneously active. SIPROS constantly evaluates the status of all parts of the system and attempts to maximize the use of all system components — especially the Central Processor. Thus, processing and input-output optimization procedures are performed automatically, without extensive pre-planning by the programmer and/or system operator.

SIPROS performs the following major functions in the 6000 Series systems:

- Controls the operation of all standard 6000 Series language processors and utility routines.
- Provides for automatic stacked-job processing, centered around the System Disk.
- Automatically controls the physical assignment of input-output devices and core storage according to equipment availability. (Operator-defined I/O unit assignment is also possible.)
- Performs switching control functions between the several active programs residing concurrently in Central Memory.
- Assigns tasks to the ten Peripheral and Control Processors and supervises their concurrent operation.
- Provides for "continuous mode" operation of relatively slow output devices (card punch, printer, plotter, etc.) by storing the output data of a particular job on disc storage until the job is complete and then performing the output operation. Input data from low-speed devices can similarly be buffered by storing a job's total input on intermediate disc storage.
- Performs integrated diagnostic routines to check the functioning of various system components (including Central Memory and the Central Processor's functional units) during the processing of the day's scheduled jobs.
- Provides full accounting information for each job processed at the conclusion of the job or upon operator request. Logged status data can be displayed on the system's console device and/or line printer. Usage of the Central Processor, Peripheral Processors, and I/O devices is measured and displayed.
- Enables the operator to override SIPROS and standard installation conventions and parameters through use of the console keyboard. The operator can modify job priorities, introduce new jobs, delete active jobs, remove specified I/O devices from "available" status, etc.
- Provides an automatic file-management system, File Manager, for simplified file control and updating by control cards. The File Manager is described in Paragraph 260:151.16.
- Provides access to a complete library of system and problem programs stored on the System Disk, and supervises the operations of LIBRIOUS, the system librarian routine.

.122 SIPROS Residence and System Overhead

SIPROS is a complex, multi-part operating system whose control routines and various functions are supervised by the SIPROS Executive routine that resides in one of the Peripheral Processors. The SIPROS Monitor routine (see Paragraph .124) shares the use of this reserved Peripheral Processor. Another reserved Peripheral Processor

.122 SIPROS Residence and System Overhead (Contd.)

houses SIPROS' Disk Executive and Display routines, which control all disc file and console display operations. The Disk Executive can load disc file input-output routines into two additional slave Peripheral Processors that actually perform the disc I/O operations.

All remaining Peripheral Processors (including the disc slave Processors when not engaged in specifically-assigned disc I/O operations) are termed "Pool" Peripheral Processors. Located in the upper 512 12-bit words of each Pool Processor's core memory is a control routine called the PP Resident, whose function is to interpret SIPROS-directed task assignments and to load the required system or user program into the remaining block of Peripheral Processor core storage. The PP Resident then initiates processing of the assigned task.

Another control routine that is a standard element within the SIPROS operating system is the Central Processor Resident. This is a small routine that resides in Central Memory with each operational program. The Central Processor Resident routine serves as the communication link between its associated program and the SIPROS Executive; it performs such tasks as interpreting the program's system macro requests, supplying the programmer's parameters to the macro routines, and loading I/O buffer areas with print, punch, and card reader data that is to be transferred to temporary storage on the System Disk.

The system overehead associated with any operating system is generally expressed not only in terms of the equipment that is reserved for use by the operating systems, but also in terms of the amount of Central Processor time that is required to perform the executive/monitor functions. However, in the Control Data 6000 Series computer systems, the SIPROS operating system imposes no demands upon the Central Processor, which can therefore devote all of its time to the processing of users' programs. The Peripheral Processors perform all of SIPROS' control functions, and the Central Memory accesses required for SIPROS operations can be completely overlapped with Central Memory accesses by the Central Processor, which is given priority whenever there are conflicting requests for access to a particular memory bank.

.123 Multiprogramming and Multiprocessing

The standard environment in which SIPROS functions consists of many programs concurrently residing in Central Memory, with each program periodically receiving processing control. Simultaneously, the ten Peripheral and Control processors can be performing other independent tasks, both system control functions and jobs assigned by the Executive, either in support of Central Processor programs or as independent "off-line" operations (such as data transcriptions).

A comprehensive priority system determines the order in which SIPROS assigns equipment to the jobs in Central Memory and initiates their execution. Priorities can be assigned by the programmer, by the operator, or by the system, and different priorities can be assigned to the program's main processing and its input-output operations. Priorities can also be designated as changing or fixed; changing priorities will be modified periodically by SIPROS to ensure that lower-priority programs will receive a proportionate amount of processing time and will not be ignored due to the insistent demands of higher-priority programs with which the less important jobs may co-exist. A Central Processor program that is currently being processed loses control whenever it encounters a program wait, such as a wait for an input-output operation to be completed. The SIPROS Monitor then switches control to the next eligible job in priority sequence.

Adequate memory protection for the multiprogrammed 6000 Series systems is provided by a combined hardware-software technique that recognizes the upper and lower bounds of each program and prohibits unauthorized Central Memory accesses beyond these boundaries. Any attempt to access memory beyond the legal limits results in an "Address Out of Range" error stop and a diagnostic map and/or dump of the job's allocated memory area.

.124 Principal Control Programs

Executive: The SIPROS Executive schedules the operations of the Central Processor, the Peripheral Processors, the 12 input-output channels, and the peripheral equipment (except for disc file units). The Executive also maintains a status list for each active job in the system, whether currently in Central Memory or stacked in the System Disk. The Executive continuously examines these status lists and initiates appropriate action upon detecting status changes.

Monitor: The SIPROS Monitor routine resides in a reserved Peripheral and Control Processor together with the Executive described above. The Monitor works in conjunction with the Executive, continuously checking the progress of the program in Central Memory that is being executed by the Central Processor. Any need for action, such as an I/O request, is relayed to the Executive for initiation of appropriate action. As the Monitor cycles through its list of jobs and finds "wait" conditions, it switches control to the next eligible job in priority sequence.

Disk Executive: The Disk Executive routine of SIPROS directs the activities of the System Disk. This routine also schedules all disc file read/write/search requests from processing programs and assigns two slave Peripheral and Control Processors to perform these disc operations. The scheduling function ensures that all disc requests that can be performed at the current position (and the next requested positions) of the disc read/write heads will be performed consecutively. The Disk Executive also coordinates all disc file operations by ordering the repositioning of heads on one file while the slave processors are reading or writing from another disc file unit.

Batch Loader: The SIPROS Batch Loader routine is called by the Executive whenever available space on the System Disk is detected. The Batch Loader then examines the system's input units (either card readers or magnetic tapes) and loads any jobs waiting in the input job stream into the System Disk until the latter device again becomes filled or until the input stream is exhausted. The operations of the Batch Loader are directed in large part by each job's control cards. From information contained

(Contd.)

.124 Principal Control (Contd.)

in these cards, the Batch Loader places identification and control information for each program in a Job Table in Central Memory for subsequent use by the Executive.

Job Loader: The Job Loader routine is called whenever the Executive determines that sufficient space in Central Memory and sufficient peripheral equipment are available for additional jobs that are stacked in the System Disk. The Job Loader then transfers the Executive-selected programs from the System Disk to Central Memory and sets the status of the successfully-loaded programs to "waiting." Control is then passed to the newly-loaded programs according to the priority scheme described above. Another function of the Job Loader is to load into Central Memory any library functions that are required for use by the programs that are transferred from the System Disk.

Display Program: The SIPROS Display Program resides in a reserved Peripheral and Control Processor together with the Disk Executive routine. The Display routine is used primarily to display on the operator's console display device the status of the presently-active Central Processor job. It is also used to provide the control routines required for standard operator/system communication. Requests from processing programs for data displays are also handled by the SIPROS Display package.

.125 SIPROS Time-Sharing System

Control Data plans to supply, during the third quarter of 1967, a version of SIPROS that is specifically designed to provide efficient operation of remote-console, time-sharing 6000 Series systems. The manufacturer's objective is to permit up to 200 remote users to simultaneously request processing by the central computer system, and to give these users what will appear to be instantaneous service. Access to all central facilities will be provided, in both conversational and stacked-job processing modes.

The time-sharing system is functionally centered around Control Data's Extended Core Storage (ECS) unit (see Report Section 260:043). The unit's data storage capacity (up to 2 million 60-bit words in the standard units) and data transfer rates (up to 400 million characters per second) are so high that Control Data plans to store a large number of active jobs in the Extended Core Storage unit and to "swap" whole programs between the ECS and Central Memory whenever an installation-determined "time-slice" is terminated for the program currently being processed in Central Memory. Thus, the Central Memory can be kept small in size, since only one program need reside in it at any given time. The relatively inexpensive ECS unit provides the mass storage required for all jobs which are currently active.

High-speed swapping of the Central Memory program and the highest-priority program in ECS is facilitated by the fact that the SIPROS-controlled time-sharing compilers will produce object programs in the form of "pure procedures" or "re-entrant coding" (i.e., programs in which instructions are never modified during the program's execution). As a result, the procedures (segments containing only instructions) of the program in Central Memory need not be rolled out to the Extended Core Storage unit, since an exact copy of these procedures already resides there; only the program's working data needs to be transferred to ECS at program swap time. Even when the entire program must be rolled out, assuming that an average program uses 16K 60-bit words, a complete swap between two programs can be performed in 3.2 milliseconds in a Control Data 6400 system or 800 microseconds in a 6800 system.

The 6000 Series time-sharing technique utilizes the speed and capacity of the ECS unit to eliminate the need for the complex addressing schemes (and associated expensive hardware) that are being used in competitive time-sharing systems (and in Control Data's own 3000 Series) to facilitate dynamic relocation of programs. It is too early to judge the overall effectiveness of Control Data's approach, although conceptually it is a straightforward and promising one.

The minimum configuration requirements for the SIPROS time-sharing system include all equipment used in the basic 6000 Series configurations, plus an Extended Core Storage unit and a 6411 Augmented Input-Output Buffer and Control (see Report Section 260:101) for expanded I/O capabilities.

.13 Availability

SIPROS 1.0 (basic system):	December 1965.
SIPROS 2.0 (with 3000 Series peripheral device control facilities):	January 1966.
SIPROS 3.0 (full system usable with smallest 32K configurations):	April 1966.
Time-Sharing SIPROS:	3rd quarter 1967.

.14 Originator: . . . . Control Data Corporation.

.15 Maintainer: . . . . Control Data Corporation.

.2 PROGRAM LOADING

.21 Source of Programs

.211	Programs from on-line libraries:	System Program Library on System Disk.
.212	Independent programs:	in System Library, or from any device designated as a System Input device.
.213	Data:	as required by users' programs.
.214	Master routines:	System Library.

.22 Library Subroutines: . . Executive provides automatic call facility.

.23 Loading Sequence: . . . sequential loading of programs onto System Disk; see Paragraph .124 for description of scheduling of Central Memory loading and program initiation.

.3 HARDWARE ALLOCATION

.31 Storage

.311 Sequencing of program for movement between levels: . . . . . . Executive calls in program segments as specified by the programmer.

.312 Occupation of working storage: . . . program segments are called from System Disk to Central Memory and overlaid as necessary.

.32 Input-Output Units

.321 Initial assignment: . . . physical unit assignment is normally a function of SIPROS, but the operator can also make these assignments.

.322 Alternation: . . . . provided automatically by SIPROS.

.323 Reassignment: . . . . . . provided by SIPROS or by operator.

.4 RUNNING SUPERVISION

.41 Simultaneous Working: . I/O Data Channel control is provided automatically by SIPROS and its I/O routines.

.42 Multiprogramming: . . controlled by Executive and Monitor function of SIPROS; see Paragraphs .123 and .124.

.43 Multi-sequencing: . . . system macro routines can operate independently of the initiating program.

.44 Errors, Checks, and Action

Error	Check or Interlock	Action
Loading input error:	?	?
In-out error:	?	?
Arithmetic overflow:	hardware check	optional ignore, or dump program and abort.
Indefinite result:	hardware check	optional ignore, or dump program and abort.
Reference to forbidden area:	hardware check	dump program and abort.

.45 Restarts: . . . . not provided to date.

.5 PROGRAM DIAGNOSTICS

.51 Dynamic

.511 Tracing: . . . . specified by MONITOR statement in COBOL source language.

.512 Snapshots: . . . . performed automatically by SIPROS at error stops.

.52 Post Mortem: . . . . . performed automatically by SIPROS.

.6 OPERATOR CONTROL

.61 Signals to Operator: . . typed message on console device.

.62 Operator's Decisions: . keyboard or control-card entries.

.63 Operator's Signals

.631 Inquiry: . . . . keyboard entries.

.632 Change of normal progress: . . . . all operator "system override" actions can be entered by keyboard entries or by control cards.

.7 LOGGING: . . . . typed record of keyboard entries, typed messages, and console displays.

.8 PERFORMANCE

.81 System Requirements

.811 Minimum configuration: . . . . basic 6000 Series system, including Central Processor, at least 32K 60-bit words of Central Memory, 10 Peripheral and Control Processors, and 12 I/O Data Channels; also, console display device, System Disk (6603 or 6607/6608), two 607 or 626 Magnetic Tape Units, card reader, card punch, and line printer.

.812 Usable extra facilities: all; control cards or keyboard entries are used to inform SIPROS of changes in equipment availability.

.813 Reserved equipment: . two Peripheral and Control Processors, plus an unspecified amount of System Disk storage.

.82 System Overhead

.821 Loading time: . . . . . . performed by SIPROS in a Peripheral Processor, causing no Central Processor delay.

.822 Reloading frequency: . . Executive, Monitor, Disk Executive, Display, and PP Resident routines reside permanently in Peripheral Processors; other control routines are called from System Disk as required.

.83 Program Space Available: . . . . the maximum size of program and I/O control tables in Central Memory is determined by the individual installation.

.84 Program Loading Time: . . . . loading time from input device to System Disk depends on speed of input unit.

.85 Program Performance: . . . . SIPROS control routines cause no Central Processor delay; see Paragraph .122.

SYSTEM PERFORMANCE

GENERAL

This section contains the system performance measurements for the Control Data 6400, 6600, and 6800 computer systems. It is possible to show on a single graph the performances of these three systems on a particular problem because all three systems use the same peripheral devices, and therefore, on I/O-limited jobs, all three will yield identical elapsed-time curves.

This method of presenting the performance figures of the Control Data 6000 Series has several distinct advantages. First, the comparative processing speeds of the three 6000 Series systems can be conveniently evaluated by observing the three Central Processor elapsed-time curves in the graph for each problem. Second, a single graph shows the raw processing power of each system in its relationships to the job-limiting input-output speeds. These relationships clearly point out the extent to which the developments in high-performance input-output devices (by current standards) have lagged behind the enormous improvements in central processor speeds. As can be seen in the logarithmic plots that follow, input-output time is frequently as much as three orders of magnitude greater than the extremely fast Central Processor times of the Control Data 6000 Series systems.

Multiprogramming and multiprocessing are the normal modes of operation with the Control Data 6000 Series. As a result, all standard problems in which input-output times are significant have been solved by using tape-to-tape operations exclusively, realizing that input card-to-tape and output tape-to-printer transcription runs can easily be performed (and their times completely masked) during the main tape-to-tape processing runs. The magnetic tape elapsed-time curves that result from this approach are equivalent to the curves that would result if these same problems were solved using our standard paired configurations VIIB and VIIIB, in which the card-to-tape and tape-to-printer operations are assumed to be performed off-line.

The performance graphs also illustrate the amount of Central Processor time that is available for multiprogramming operations while each of the I/O-limited standard problems is being processed. The amount of time available for additional jobs is equal to the difference between the Central Processor curves (broken lines) and the magnetic tape input-output times (solid lines). The processing times for the subsidiary Peripheral Processors are completely masked behind the elapsed time for the total job.

The most noteworthy and advantageous characteristic of the performance of the Control Data 6000 Series is the possible complete elimination of any Central Processor delays or interference caused by input-output operations, housekeeping routines, file-scanning and table-lookup operations, etc. These time-consuming operations can be performed by the Peripheral and Control Processors concurrently with the main processing performed by the Central Processor. However, it is entirely conceivable that the use of the Peripheral Processors will in some cases be so great that their capacity will be exceeded, causing a system delay and a resultant reduction in the throughput of the overall system. The Control Data 6400 and 6600 computer systems can provide for this situation by permitting connection of up to 120 additional Peripheral and Control Processors in the form of 6411 Augmented Input-Output Units (Section 260:101). The effectiveness of this approach has not been demonstrated to date.

In order to utilize the full power and simultaneity of the Control Data 6000 Series systems in the performance of our standard benchmark problems, some minor adjustments were made in the problem solution methods. The principal changes involved a resequencing of the program logic flow for each of the File Processing Problems (the standard flow-charts are presented in Section 4:200.1 of the Users' Guide), and a partitioning of work between the Central Processor and one or more of the Peripheral Processors. The amount of Peripheral Processor usage is noted for each problem. These adjustments allow meaningful comparisons to be made between the performance graphs for the 6000 Series and those of all other computer systems analyzed in AUERBACH Standard EDP Reports.

GENERALIZED FILE PROCESSING (260:201.100)

These problems involve updating a master file from information in a detail file and producing a printed record of each transaction. This application is one of the most common commercial data processing jobs and is fully described in Section4:200.1 of the Users' Guide. Standard File Problems A, B, and C show the effects of varying record sizes in the master file. Standard File Problem D increases the amount of computation performed upon each transaction. Each problem is estimated for activity factors (ratios of number of detail records to number of master records) of zero to unity. In all cases a uniform distribution of activity is assumed.

Table I presents in detail the techniques used to adapt our standard file processing job solution methods to the unique simultaneous operations facilities of the Control Data 6000 Series. Work distribution between the Central Processor and the several "Pool" Peripheral Processors is shown, and the simultaneous use of the multiple arithmetic units (in the 6600 and 6800 systems) is also explained.

In every case measured for the 6000 Series computer systems, the tape-to-tape elapsed time is far greater than the required Central Processor time. Even in the worst case (the 6400 system, Configuration VIII, processing blocked detail files with computations tripled and high master-file activity), the Central Processor uses only 20% of the total elapsed time.

SORTING (260:201.200)

The standard estimate for sorting 80-character records by straightforward merging on magnetic tape was developed fromthe time for Standard File Problem A by the method explained in Paragraph 4:200.213 of the Users' Guide. A three-way merge is used in all system configurations for the Control Data 6000 Series. The results are shown in Graph 260:201.200.

MATRIX INVERSION (260:201.300)

The standard estimate for inverting a non-symmetric, non-singular matrix was computed by the simple method described in Paragraph 4:200.312 of the Users' Guide. Computation is performed in single-precision floating-point format (14-digit precision). The results are shown in Graph 260:201.300.

GENERALIZED MATHEMATICAL PROCESSING (260:201.400)

Standard Mathematical Problem A is an application in which there is one stream of input data, a fixed computation to be performed, and one stream of output results. Two variables are introduced to demonstrate how the time for a job varies with different proportions of input, computation, and output. The factor C is used to vary the amount of computation per input record. The factor R is used to vary the ratio of input records to output records. The procedure used for the Standard Mathematical Problem is fully described in Section 4:200.4 of the Users' Guide.

Computations are performed in single-precision floating-point arithmetic, which provides 14-digit precision as compared with the minimum 8-digit precision prescribed in the Users' Guide. The multiprocessing capabilities of the standard Control Data 6000 Series configurations were utilized by simply dividing the total computational load between the Central Processor and the Peripheral Processors. The work required to execute the five polynomial loops and the square root operation is performed by the Central Processor. The standard SIPROS Peripheral Processors and one additional Peripheral Processor are used to prepare the input data and to generate the output report.

Again, since multiprogramming is standard with the 6000 Series, the graph shows both Central Processor time and total elapsed time. All input-output operations are performed using magnetic tape; any necessary data transcription runs are assumed to be overlapped with the main processing program. The Central Processor time for each system is represented by a single line, pointing out that variations in output frequency, factor R, do not affect Central Processor performance; increased output demands are absorbed by the Peripheral Processors.

(Contd.)

TABLE I: DIVISION OF COMPUTATIONAL WORK BETWEEN THE CENTRAL AND PERIPHERAL PROCESSORS

FLOW-CHART REFERENCES*	COMPUTATION UNIT	CENTRAL PROCESSOR WORK	PERIPHERAL PROCESSOR WORK
a1 (Blocks 1 through 9)	Per input block	Central Processor program initiation for each input block containing one or more active records.	All normal input-output computation involved in this activity, using the standard Magnetic Tape and Disk routines of the SIPROS Operating System.
a2 (Blocks 10 through 23)	Per input record	Record activity check, performed only when the record is in a block containing at least one active record.	All normal block activity checking and control total computations, using a Pool Peripheral Processor dedicated to this program.
b6 (Blocks 38 through 42)	Per detail record	No time used.	All normal computation involved in this detail record input operation, using the standard Magnetic Tape routines of the SIPROS Operating System.
b5 + b9 (Blocks 24 through 37, and 47 through 48)	Per active record	All computational work, consisting of Blocks 24 through 37. For the 6600 and 6800, the flowchart blocks were rearranged in order to initiate Blocks 32 and 33 immediately, thus bringing the two multiplications into parallel operations. The divide operation in Block 34 is then executed as soon as the multiplications are completed. All other operations (namely, Blocks 27 through 31, the checking in Block 33, and Blocks 35 through 37) are overlapped with the multiply and divide operations.	The unpacking and repacking operations in Blocks 24, 47, and 48, using a Pool Peripheral Processor.
b7 + b8 (Blocks 43 through 46)	Per report	No time used.	All output preparations, using a Pool Peripheral Processor dedicated to this program, in conjunction with SIPROS facilities.

* The detailed flow-chart of the AUERBACH Standard File Processing Problems is presented in Section 4:200.1 of the Users' Guide to AUERBACH Standard EDP Reports.

WORKSHEET DATA TABLE

	ITEM		CONFIGURATION* VIIA (Blocked)	VIIA (Unblocked)	VIIIA (Blocked)	VIIIA (Unblocked)	REFERENCE
1 Standard File Problem A Input-Output Times*	Char/block	(File 1)	1,080	1,080	1,080	1,080	4:200.112
	Records/block	K (File 1)	12	12	12	12	
	msec/block	File 1 = File 2	28	28	14	14	
		File 3	26 (1)	11	13 (1)	6	
		File 4	34 (1)	12	17 (1)	6	
	msec/switch	File 1 = File 2	0	0	0	0	
		File 3	0	0	0	0	
		File 4	0	0	0	0	
	msec penalty	File 1 = File 2	0	0	0	0	
		File 3	0	0	0	0	
		File 4	0	0	0	0	

	ITEM		6400**	6600**	6800**	REFERENCE
2 Central Processor Times**	μsec/block	a_1	2.0 or 0 (2)	1.0 or 0 (2)	0.25 or 0 (2)	4:200.1132
	μsec/record	a_2	3.4 or 0 (2)	2.0 or 0 (2)	2.50 or 0 (2)	
	μsec/detail	b_6	95.5	12.9	3.2	
	μsec/work	$b_5 + b_9$	95.5	12.9	3.2	
	μsec/report	$b_7 + b_8$	0	0	0	

	ITEM		6400 C.P.	6400 File 4	6600 C.P.	6600 File 4	6800 C.P.	6800 File 4	REFERENCE
3 Standard File Problem A at F = 1.0	msec/block for C.P. and dominant I/O column.	a_1	0.002		0.001		0.0003		4:200.114
		a_2K	0.041		0.024		0.006		
		a_3K	1.150		0.156		0.039		
		File 1: Master In	0		0		0		
		File 2: Master Out	0		0		0		
		File 3: Details	0		0		0		
		File 4: Reports	0	17-144 (3)	0	17-144 (3)	0	17-144 (3)	
		Total	1.193	17-144	0.181	17-144	0.0453	17-144	

	ITEM		6400	6600	6800	REFERENCE
4 Standard File Problem A Space	Unit of measure	(60-bit words)				4:200.1151
		Std. routines	0	0	0	
		Fixed	20	20	20	
		3(Blocks 1 to 23)	1 PPU (4)	1 PPU (4)	1 PPU (4)	
		6 (Blocks 24 to 48)	1,000	1,000	1,000	
		Files	2,000	2,000	2,000	
		Working	500	500	500	
		Total	3,520	3,520	3,520	

	ITEM		CONFIGURATION VIIB	VIIIB	REFERENCE
5 Standard Mathematical Problem A	Fixed/Floating point		Floating point	Floating point	4:200.413
	Unit name	input	604 Tape Unit	607 Tape Unit	
		output	604 Tape Unit	607 Tape Unit	
	Size of record	input	80 chars	80 chars	
		output	120 chars	120 chars	
	msec/block	input: T1	11	5	
		output: T2	12	6	
	msec penalty	input: T3	0	0	
		output: T4	0	0	

ITEM		VIIB 6400	VIIB 6600	VIIB 6800	VIIIB 6400	VIIIB 6600	VIIIB 6800
msec/record	T5	0	0	0	0	0	0
msec/5 loops	T6	0.24	0.006	0.0015	0.24	0.006	0.0015
msec/report	T7	0	0	0	0	0	0

* Select the input-output data for the desired configuration. This data will be identical for any Control Data 6000 Series computer system.

** Select the Central Processor data for the desired Control Data 6000 Series computer system. This data will be identical for any standard configuration.

(1) Files 3 and 4 are blocked 12 records/block.

(2) No Central Processor time is used if no records in the block are to be updated.

(3) The dominant column time at 1.0 activity is always File 4. Its value varies with the configuration used and the blocking factors, as follows: VIIB (blocked) — 34; VIIB (unblocked) — 144; VIIIB (blocked) — 17; and VIIIB (unblocked) — 72 msec.

(4) One Pool Peripheral Processor with 4,000 12-bit words can be used for storing this program segment.

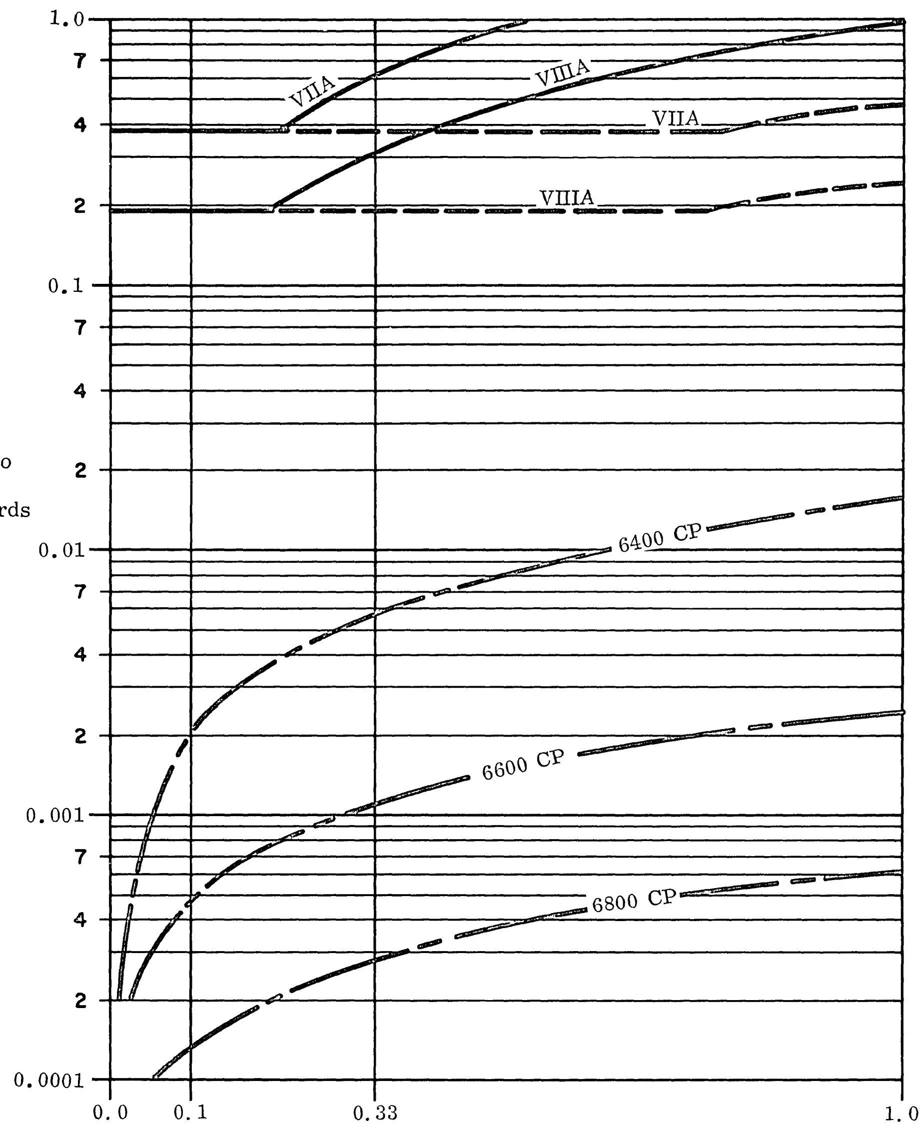
(Contd.)

.1 GENERALIZED FILE PROCESSING

.11 Standard File Problem A

.111 Record sizes —
Master file: . . . . . . 108 characters, coded and held in 45 12-bit words.
Detail file: . . . . 1 card.
Report file:. . . . . . . 1 line.

.112 Computation:. . . . . . . standard.
.113 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.113, adjusted for multiprocessing.
.114 Graph: . . . . see graph below.
.115 Storage space required: . . . . 3,520 60-bit words.



(Roman numerals denote standard System Configurations.)

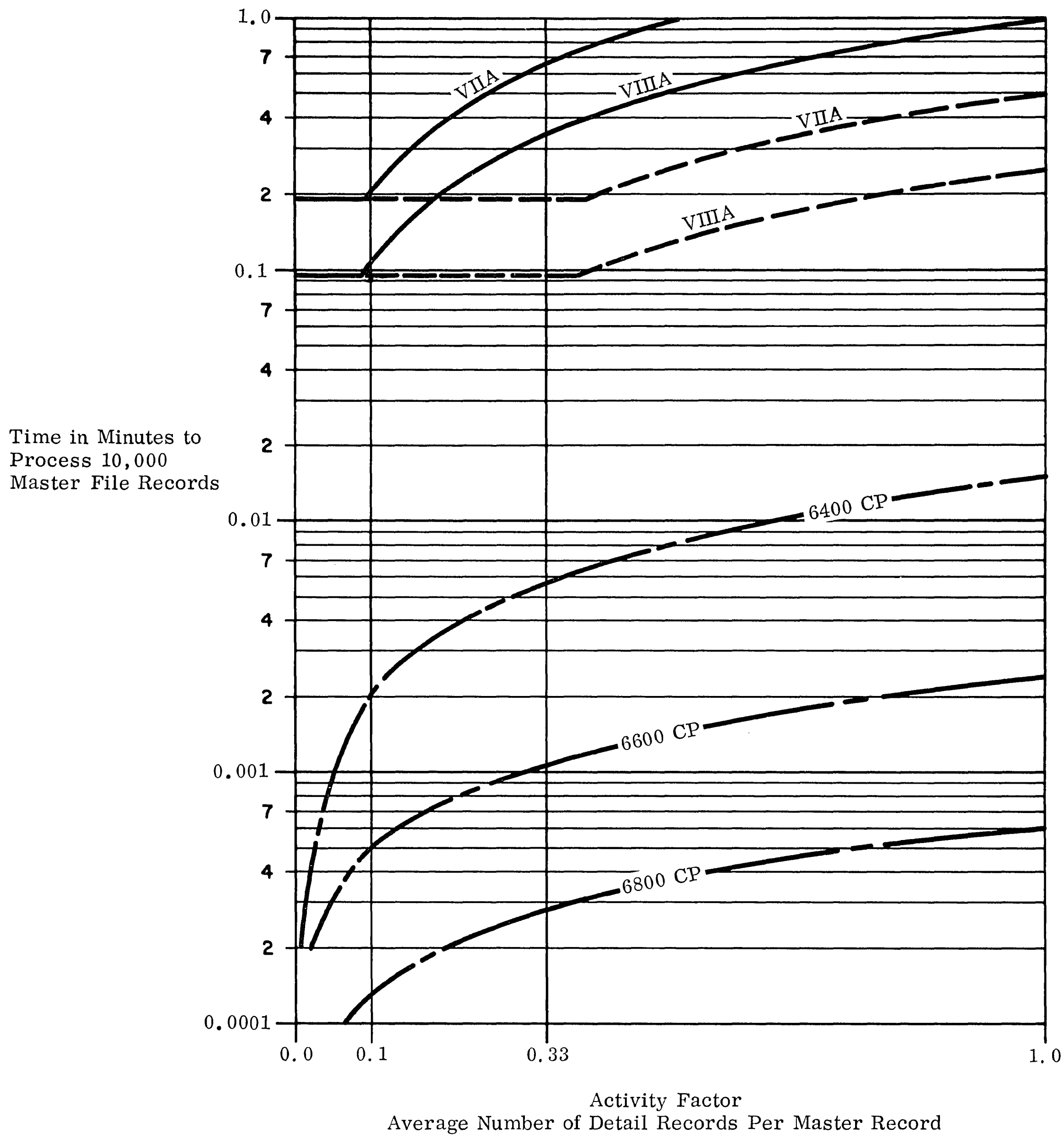
LEGEND

———————	Elapsed time for main processing run (Files 3 & 4 unblocked).
— — — — —	Elapsed time for main processing run (Files 3 & 4 blocked).
— - — 6400 CP —	6400 Central Processor time for main processing run.
— - — 6600 CP —	6600 Central Processor time for main processing run.
— - — 6800 CP —	6800 Central Processor time for main processing run.

.12 Standard File Problem B

.121 Record sizes —
Master file: . . . . . . 54 characters.
Detail file: . . . . 1 card.
Report file:. . . . . . . 1 line.

.122 Computation:. . . . . . . standard.
.123 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.12, adjusted for multiprocessing.
.124 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

LEGEND

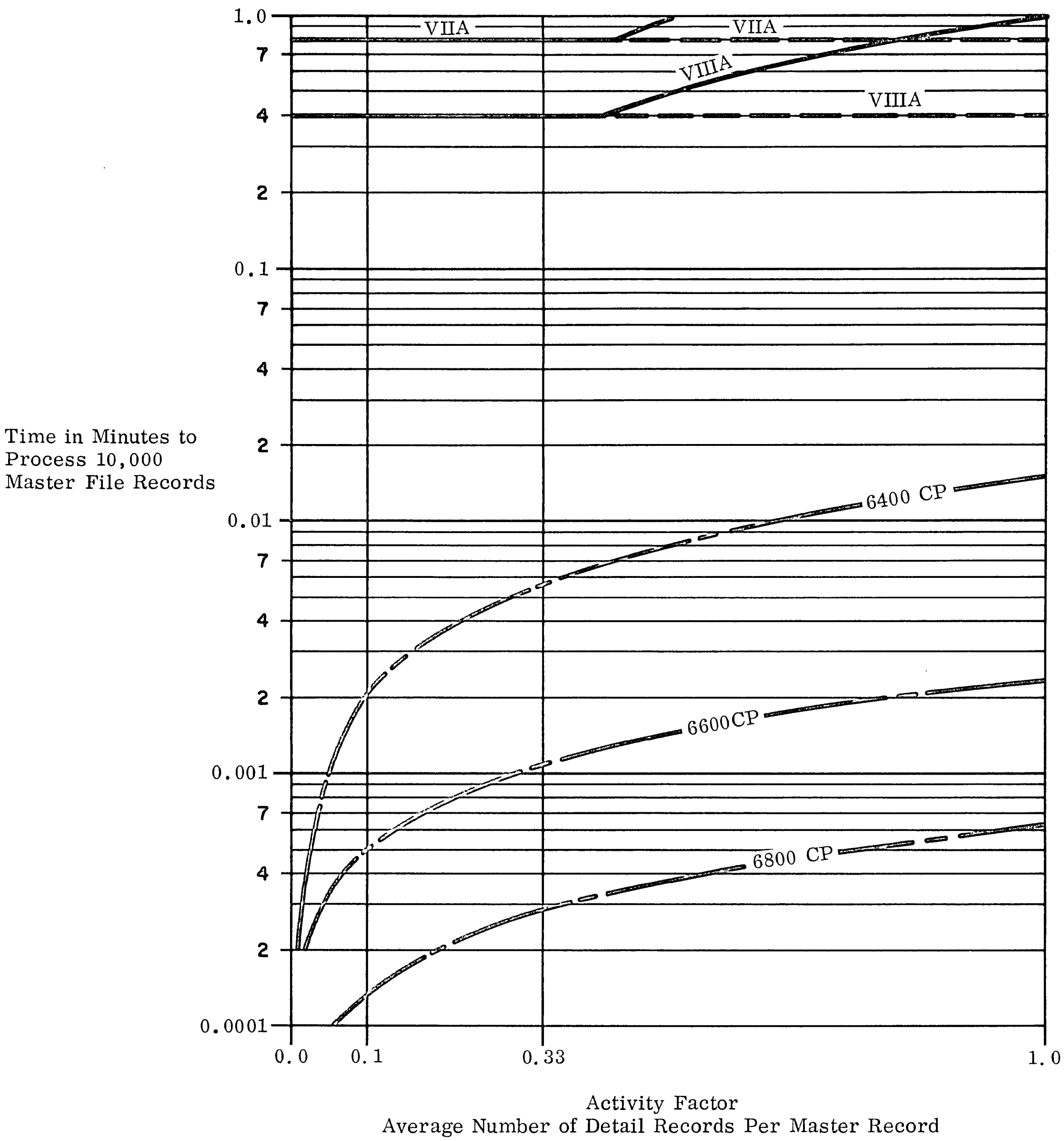
————	Elapsed time for main processing run (Files 3 & 4 unblocked).
— — — —	Elapsed time for main processing run (Files 3 & 4 blocked).
—— — —— 6400 CP ———	6400 Central Processor time for main processing run.
—— — —— 6600 CP ———	6600 Central Processor time for main processing run.
—— — —— 6800 CP ———	6800 Central Processor time for main processing run.

(Contd.)

.13 Standard File Problem C

.131 Record sizes —
Master file: . . . . . . 216 characters.
Detail file: . . . . 1 card.
Report file:. . . . . . . 1 line.

.132 Computation:. . . . . . . standard.
.133 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.13, adjusted for multiprocessing.
.134 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

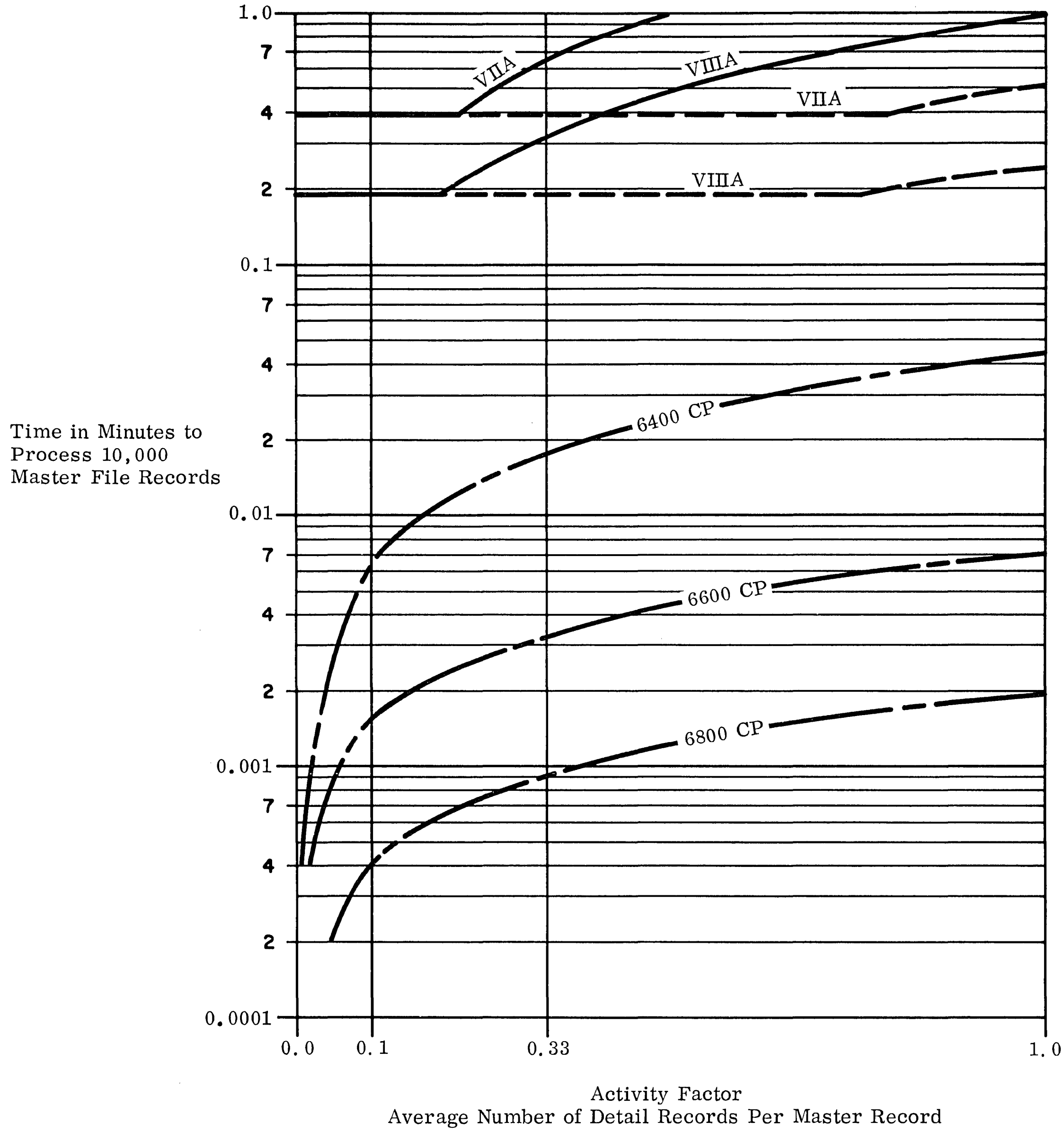
LEGEND

————	Elapsed time for main processing run (Files 3 & 4 unblocked).
— — — —	Elapsed time for main processing run (Files 3 & 4 blocked).
— — 6400 CP —	6400 Central Processor time for main processing run.
— — 6600 CP —	6600 Central Processor time for main processing run.
— — 6800 CP —	6800 Central Processor time for main processing run.

.14 Standard File Problem D

.141 Record sizes —
Master file: . . . . . . 108 characters.
Detail file: . . . . 1 card.
Report file:. . . . . . . 1 line.

.142 Computation:. . . . . . . trebled.
.143 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.14, adjusted for multiprocessors.
.144 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

LEGEND

- ——— Elapsed time for main processing run (Files 3 & 4 unblocked).
- — — — Elapsed time for main processing run (Files 3 & 4 blocked).
- —— - —— 6400 CP ——- 6400 Central Processor time for main processing run.
- —— - —— 6600 CP ——- 6600 Central Processor time for main processing run.
- —— - —— 6800 CP ——- 6800 Central Processor time for main processing run.

(Contd.)

.2 SORTING

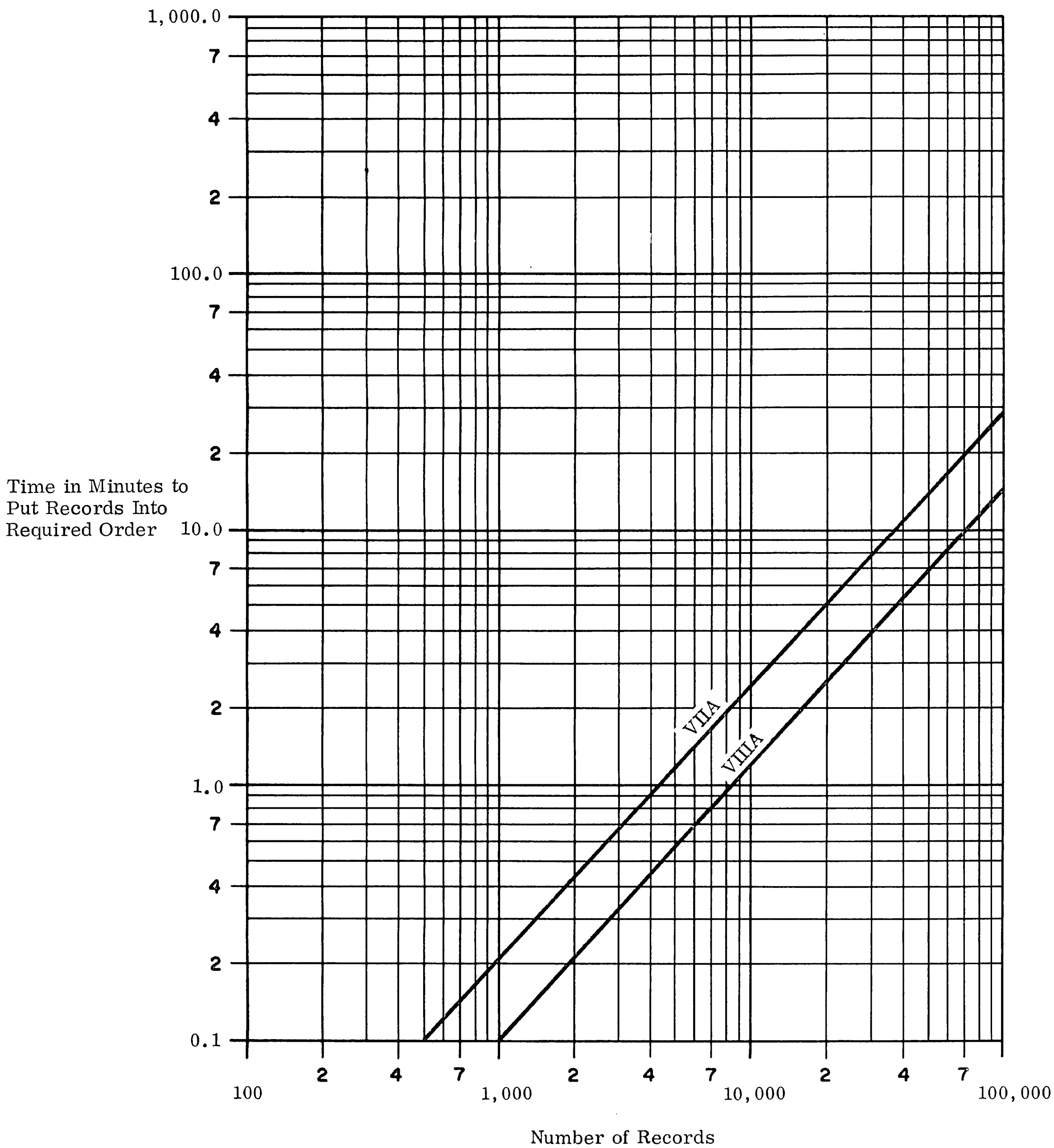
.21 Standard Problem Estimates

.211 Record size: . . . . 80 characters.

.212 Key size: . . . . 8 characters.

.213 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.213.

.214 Graph: . . . . see graph below.



(Roman numerals denote standard System Configurations.)

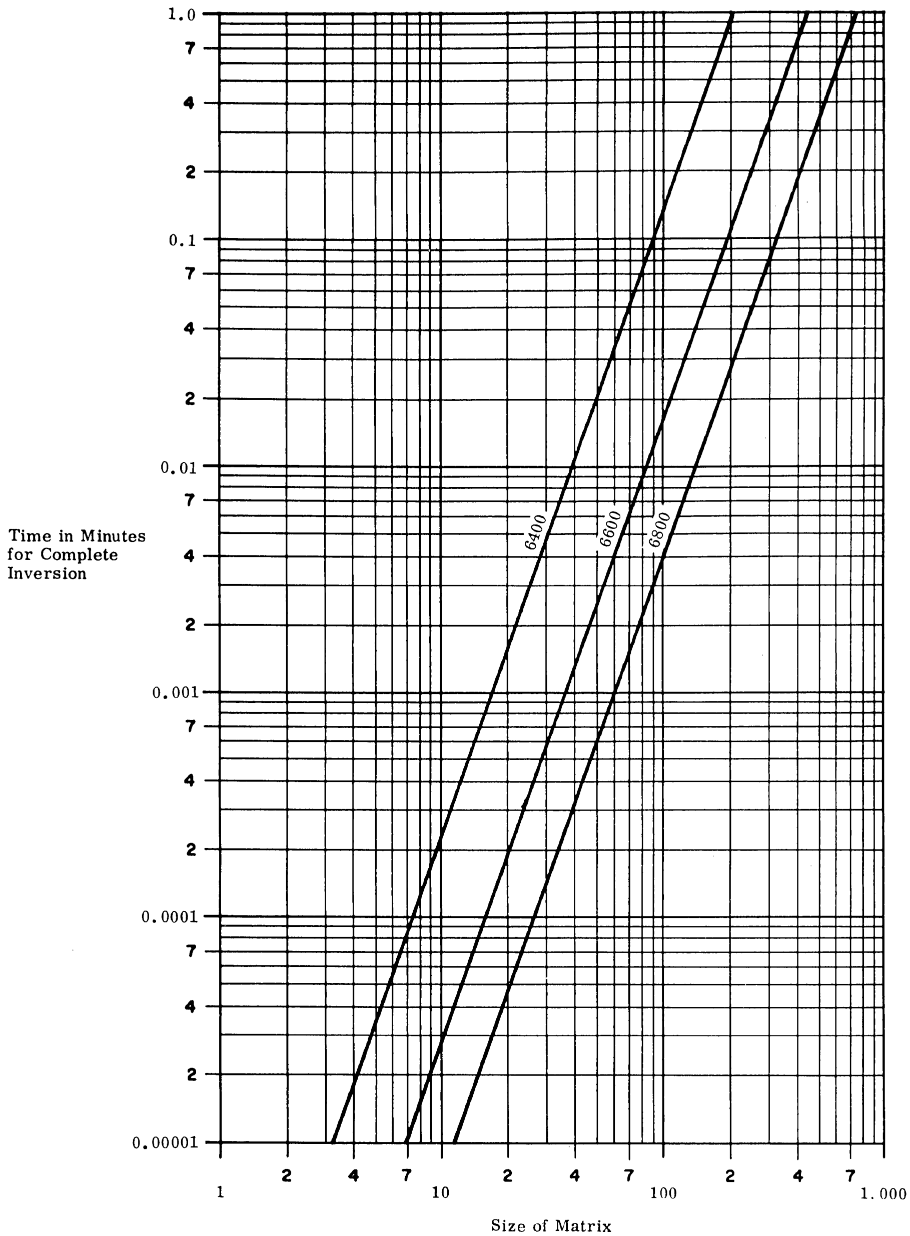
.3 MATRIX INVERSION

.31 Standard Problem Estimates

.311 Basic parameters: . . . general, non-symmetric matrices, using floating point to at least 8 decimal digits precision.

.312 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.312.

.313 Graph: . . . . see graph below.



.4 GENERALIZED MATHEMATICAL PROCESSING

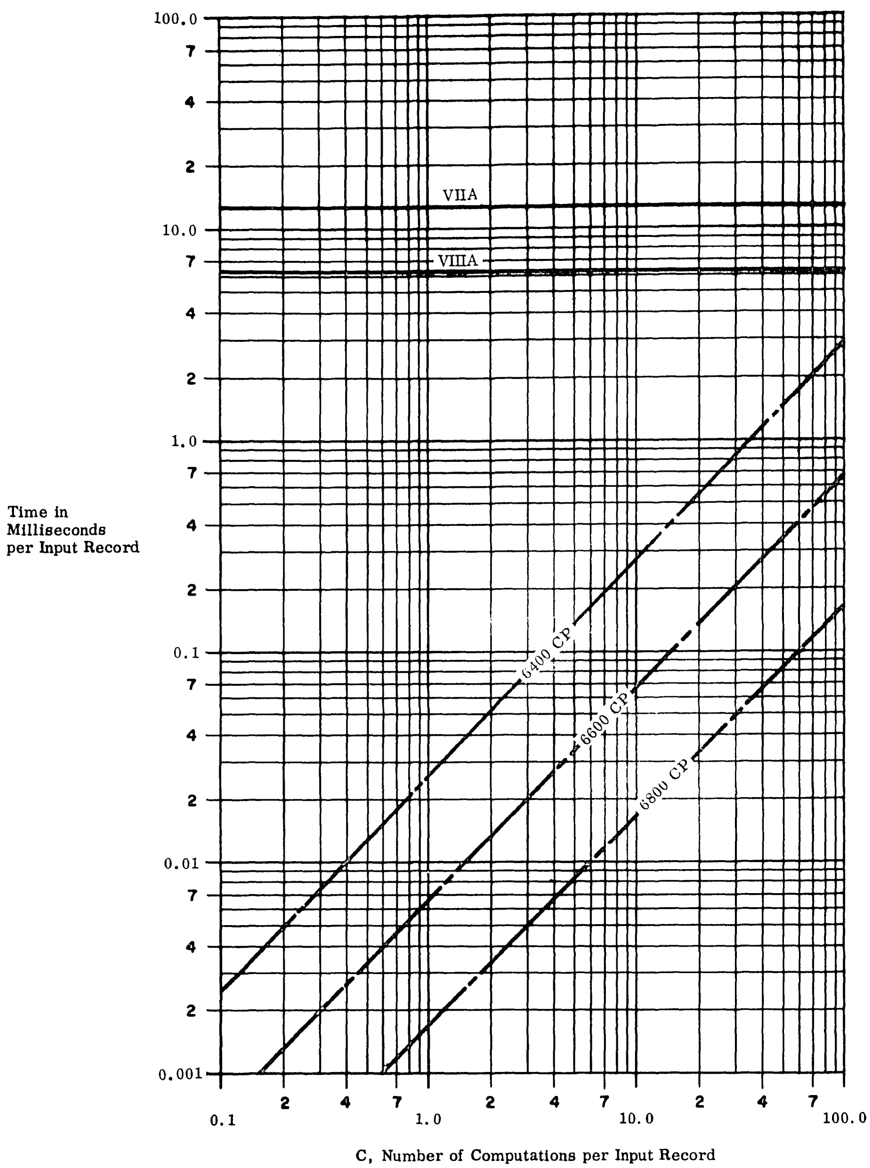
.41 Standard Mathematical Problem A Estimates

.411 Record sizes: . . . . . . 10 signed numbers; average size 5 digits, maximum size 8 digits.

.412 Computation:. . . . . . . 5 fifth-order polynomials; 5 divisions; 1 square root.

.413 Timing basis: . . . . . . using estimating procedure outlined in Users' Guide, 4:200.413; floating-point arithmetic with 14-digit precision.

.414 Graph: . . . . see graph below.



LEGEND

Elapsed time.
6400 CP — 6400 Central Processor time.
6600 CP — 6600 Central Processor time.
6800 CP — 6800 Central Processor time.

STANDARD EDP REPORTS
AUERBACH

PHYSICAL CHARACTERISTICS

Unit	Width, inches	Depth, inches	Height, inches	Weight, pounds	Power, KVA	BTU per hr.
6401 Central Computer	165	98.5	79.8	11,400	27.97	95,400
6404 Central Computer	165	32	79.8	7,800	18.65	69,250
6405 Central Computer	165	32	79.8	7,800	18.65	69,250
6411 Augmented I/O Buffer and Control	98.5	32	79.8	4,200	9.31	31,400
6601 Central Computer	165	165	79.8	15,000	37.3	102,000
6604 Central Computer	165	98.5	79.8	11,400	27.97	95,400
6605 Central Computer	165	98.5	79.8	11,400	27.97	95,400
6602 Console Display	60	52	48.5	900	5 amps.	2,100
6060 Remote Calculator	19.4	23.1	9.5	40	10 amps.	?
852 Disk Storage Drive	24	36	40.8	480	9 amps.	3,000
853 Disk Storage Drive	24	36	40.8	480	9 amps.	3,000
854 Disk Storage Drive	24	36	40.8	480	9 amps.	3,000
6603 Disk System:						
Main Cabinet	60	46	53	2,800	5 amps.	24,000
Auxiliary Cabinet	22	46	53	850	70 amps.	---
6607 Disk System:						
Disk File Cabinet	108	39	77	3,350	?	34,100
Auxiliary Cabinet	48	39	77	1,000	?	---
6608 Disk System:						
Disk File Cabinet	108	39	77	4,000	?	44,370
Auxiliary Cabinet	48	39	77	1,000	?	---
626 Magnetic Tape Transport	28	33	72	1,200	11 amps.	11,000
General Purpose Peripheral Controller Cabinet	48	32	48	800	5 amps.	3,900
3276 Communication Terminal Controller	32.8	29.8	68.8	700	12 amps.	5,900

General Requirements

Temperature: 72° ± 3°F.
Relative Humidity: 35% — 50%.
Power —

1. 50/60-cycle, single-phase, 115±10 vac. This provides power to each cabinet for blowers and utility outlets.
2. 400-cycle, 3-phase, 208 vac, 4-wire. This is produced by a motor-generator frequency converter and provides primary power for the dc supplies. The motor-generator frequency converter requires 3-phase, 3- or 4-wire, 50/60-cycle power, at a line-to-line voltage of either 208, 220, or 440 vac.
3. Peripheral equipment will require either 50/60 cycle, 3-phase, 4-wire, Y-connected, 208 ± 20 vac; or 50/60 cycle, single-phase, 115 ± 10 vac.

PRICE DATA

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
CENTRAL PROCESSORS	6401	Central Computer for 6400 system, with 131,072 words of core storage, 10 Peripheral Processors with storage, power and cooling apparatus	50,000	6,100	2,100,000
	6404	Central Computer — same as 6401, but with 65,536 words of core storage	30,950	3,525	1,300,000
	6405	Central Computer — same as 6401, but with 32,768 words of core storage	17,850	2,340	750,000
	6410	Additional Central Processor, with arithmetic and control functions of the basic 6400 Central Processor	9,700	1,000	410,000
	6411	Augmented Input-Output Buffer and Control, with 16,384 words of core storage and 10 Peripheral Processors with storage	7,100	530	340,000
	6601	Central Computer for 6600 system, with 131,072 words of core storage, 10 Peripheral Processors with storage, power and cooling apparatus	71,500	7,210	5,110,000
	6604	Central Computer — same as 6601 but with 65,536 words of core storage	53,500	6,400	3,450,000
	6605	Central Computer — same as 6601, but with 32,768 words of core storage	41,900	5,700	2,600,000
	6801	Central Computer for 6800 system, with 131,072 words of core storage, 10 Peripheral Processors with storage, power and cooling apparatus	77,500	7,210	3,600,000
	6804	Central Computer — same as 6801, but with 65,536 words of core storage	53,500	6,400	2,400,000
	6805	Central Computer — same as 6801, but with 32,768 words of core storage	41,900	5,700	1,800,000

CLASS	IDENTITY OF UNIT		PRICES		
	No.	Name	Monthly Rental $	Monthly Maintenance $	Purchase $
BULK CORE STORAGE	6830	Extended Core Storage; 524,288 words	29,000	1,800	800,000
	6831	Extended Core Storage; 1,048,576 words	58,000	2,800	1,600,000
INPUT-OUTPUT		Consoles and Displays			
	6602	Console Display (with controller)	900	160	45,750
	6060	Remote Calculator	125	18	4,500
		Disk File Storage			
	852	Disk Storage Drive	?	?	?
	853	Disk Storage Drive	320	?	14,200
	854	Disk Storage Drive	470	?	21,000
	6603	Disk System	5,600	610	225,000
	6607	Disk System	4,900	610	200,000
	6608	Disk System	7,250	755	295,000
		Magnetic Tape			
	626	Magnetic Tape Transport; 240,000 characters/sec, 14 tracks.	1,075	185	51,600
	6622	Magnetic Tape Controller	560	85	24,000
		Data Communications			
	3276	Communication Terminal Controller	250	55	12,500
	6675-D	Data Set Controller	1,450	180	60,000
	6676	Data Set Controller	1,900	120	75,000
	6677-A	Multiplexor	1,250	110	50,000
	6677-B	Multiplexor	1,500	130	60,000
	6678	Data Set Controller	1,900	150	75,000
DATA CHANNEL CONVERTER	6681	Data Channel Converter	310	40	13,500
	6682	Satellite Coupler, for direct connection of 6000 Series Data Channels	90	12.50	4,100

NOTE: FOR PRICES OF THE CONTROL DATA 3000 SERIES PERIPHERAL UNITS, SEE PAGE 245:221.101.

CDC 6400

Control Data Corporation

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INTRODUCTION

The Control Data 6400 Computer system is characterized by a Central Processor that executes one instruction at a time using an internal clock-cycle time of 100 nanoseconds. A two-register instruction access buffer or stack is used to minimize delays in instruction retrieval. The 6400 utilizes a Central Memory with a cycle time of one microsecond per 60-bit word. Up to 10 banks of Central Memory can be accessed concurrently. The ten Peripheral Processors that form an integral part of the 6400 system have fairly complete instruction sets and individual, independent core storage units of 4,096 12-bit words, with a cycle time of one microsecond.

This report concentrates upon the performance of the Control Data 6400 system in particular. All general characteristics of the 6000 Series hardware and software are described in Computer System Report 260: Control Data 6000 Series — General.

The System Configuration section which follows shows the Control Data 6400 in the following standard configurations:

V:	6-Tape Auxiliary Storage System
VI:	6-Tape Business/Scientific System
VIIA:	10-Tape General System (Integrated)
VIIIA:	20-Tape General System (Integrated).

These configurations were selected to show the 6400 both in its minimum configurations (V and VI) and in larger multi-tape configurations (VIIA and VIIIA). Multiprogramming and multiprocessing are the 6400's normal modes of operation. As a result, the main processing runs and the input-output data transcription runs in our standard benchmark problems are assumed to be performed in parallel.

The system configurations are arranged according to the rules in the Users' Guide, page 4:030.120, and any significant deviations from the standard specifications are listed. The principal deviations include the ten Peripheral Processors that are standard in every 6000 Series system, and the System Disk, required for use by the SIPROS operating system.

Section 260:051 provides detailed central processor timing data for the 6400. See Section 260:051 for the other characteristics of the program-compatible 6000 Series processors.

System Performance measurements for the 6400 computer system are presented in Section 260:201, together with the measurements for the 6600 and 6800 systems for ease of comparison.

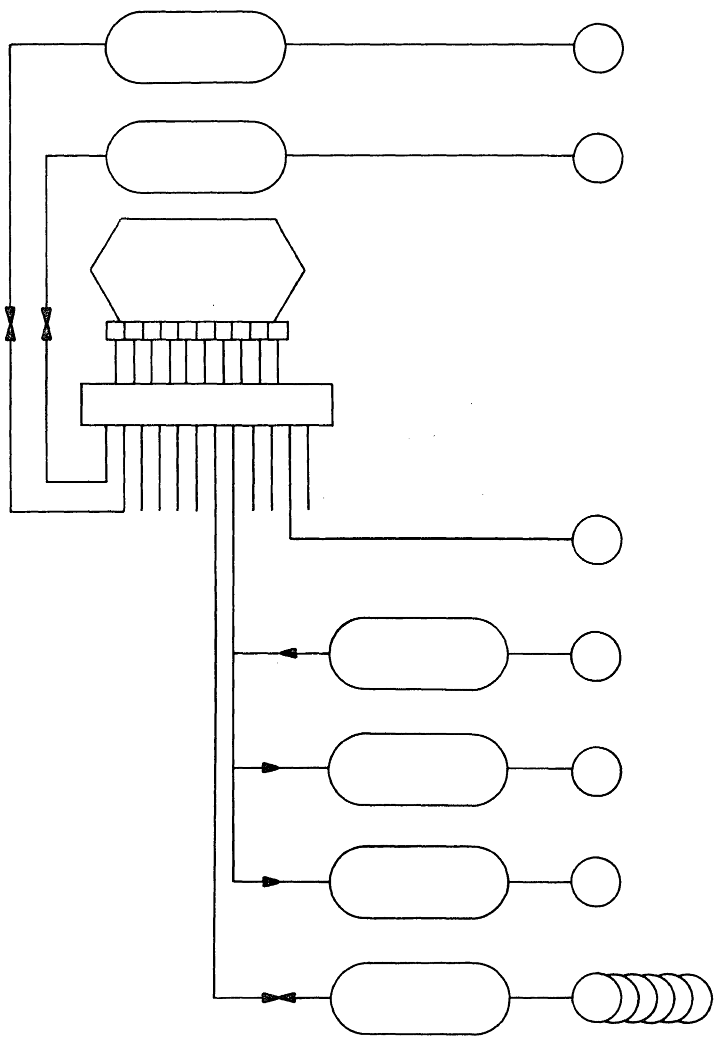
The software that is provided for all 6000 Series systems is described in Sections 260:151 through 260:191.

SYSTEM CONFIGURATION

The basic Control Data 6000 Series system configuration possibilities are summarized in report Section 260:031. This section shows the Control Data 6400 Computer System arranged in several configurations that conform to our Standard Configurations, as defined in the Users' Guide, page 4:030.120. Note that the 6681 Data Channel Converter is used in each configuration. This device permits the use of any peripheral units that are used with the Control Data 3000 Series computer systems.

.1 6-TAPE AUXILIARY STORAGE SYSTEM; CONFIGURATION V

Deviations from Standard Configuration: . . . . auxiliary storage capacity is 65% larger.
card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 40% faster.
320,000 additional characters of core storage.

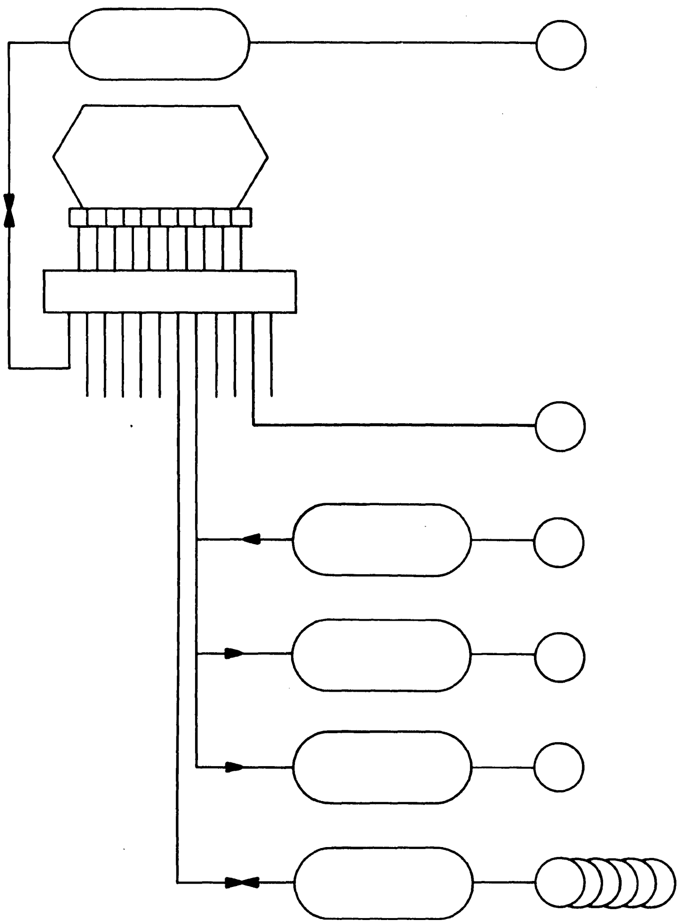


Equipment	Rental
828 Disk File (33 million char)	$ 2,400
3432 Controller	1,050
6607 Disk System* with controller (84 million characters)	4,900
6400 Central Processor with 32K 60-bit words of storage	
10 Peripheral Processors, each with 4K 12-bit words of storage	17, 850
10 x 12 Bus	
12 Input/Output Channels	
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3245 Controller	330
505 Line Printer (500 lpm)	635
3256 Line Printer Controller	515
6681 Data Channel Converter	310
603 41.7KC Magnetic Tape Units (6)	3,300
3229 Controller	600
6681 Data Channel Converter	310
TOTAL:	$33,895

* Provided for operating system purposes.

.2 6-TAPE BUSINESS/SCIENTIFIC SYSTEM; CONFIGURATION VI

Deviations from Standard Configuration. . . . . card reader is 140% faster.
card punch is 150% faster.
magnetic tapes are 40% faster.
240,000 additional characters of core storage.



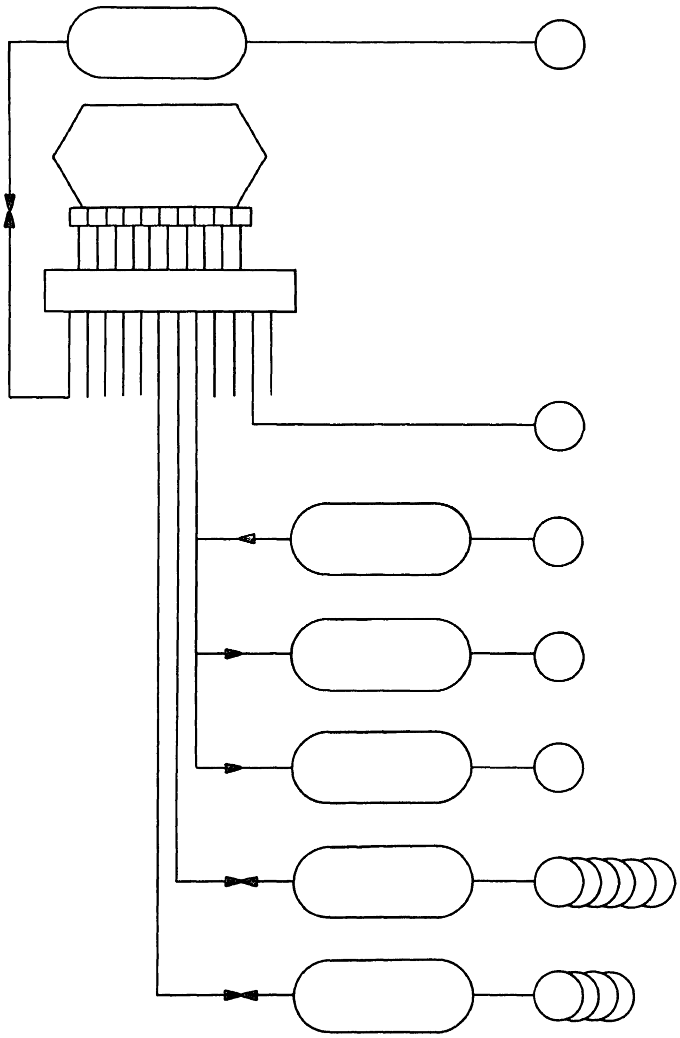
Equipment	Rental
6607 Disk System* with controller (84 million characters)	$ 4,900
6400 Central Processor with 32K 60-bit words of storage	
10 Peripheral Processors, each with 4K 12-bit words of storage	17,850
10 x 12 Bus	
12 Input/Output Channels	
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Line Printer	515
6681 Data Channel Converter	310
603 41.7KC Magnetic Tape Units (6)	3,300
3229 Controller	600
6681 Data Channel Converter	310
TOTAL:	$30,565

* Provided for operating system purposes.

(Contd.)

.3 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . card reader is 140% faster.
card punch is 150% faster.
200,000 additional characters of core storage.

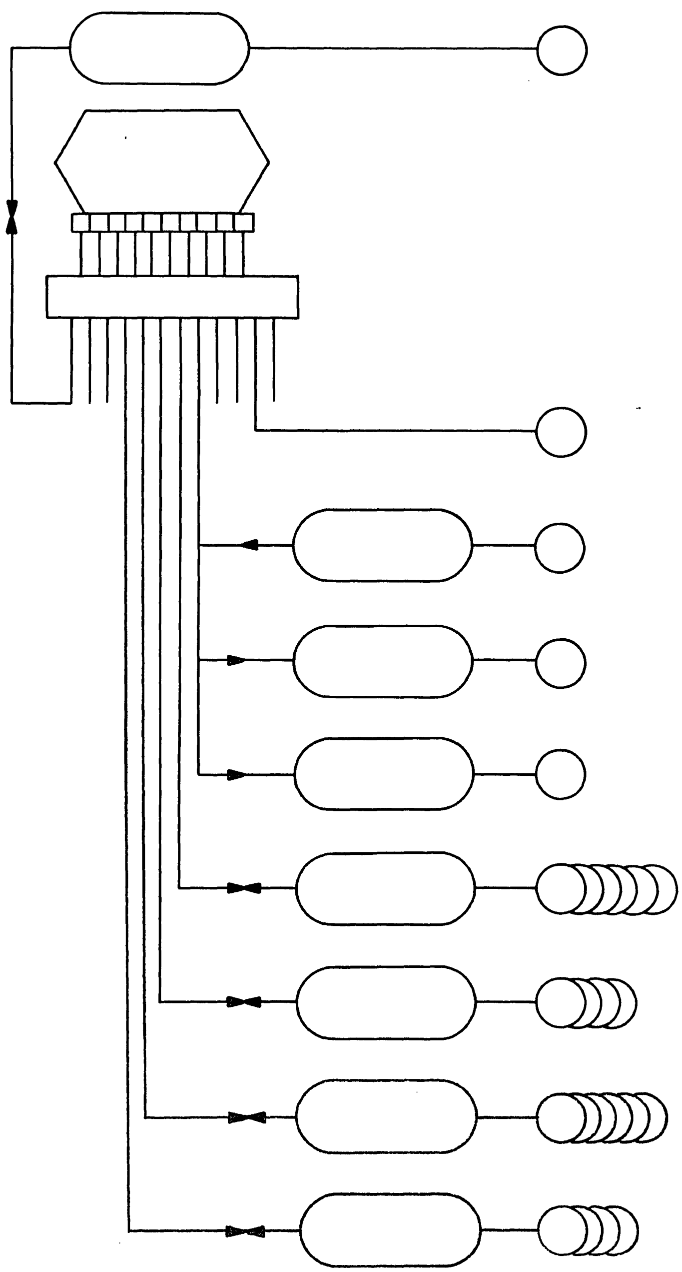


Equipment	Rental
6607 Disk System* with controller (84 million characters)	$ 4,900
6400 Central Processor with 32K 60-bit words of storage; 10 Peripheral Processors, each with 4K 12-bit words of storage; 10 x 12 Bus; 12 Input/Output Channels	17,850
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
6681 Data Channel Converter	310
604 60KC Magnetic Tape Units (6)	3,600
3229 Controller	600
6681 Data Channel Converter	310
604 60KC Magnetic Tape Units (4)	2,400
3228 Controller	425
6681 Data Channel Converter	310
TOTAL:	$34,000

* Provided for operating system purposes.

.4 20-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIIA

Deviations from Standard Configuration: . . . . card reader is 20% faster.
card punch is 25% faster.
80,000 additional characters of core storage.



Equipment	Rental
6607 Disk System* with controller	$ 4,900
6400 Central Processor with 32K 60-bit words of storage; 10 Peripheral Processors, each with 4K 12-bit words of storage; 10 x 12 Bus; 12 Input/Output Channels	17,850
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (6)	5,250
3229 Controller	600
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (4)	3,500
3228 Controller	425
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (6)	5,250
3229 Controller	600
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (4)	3,500
3228 Controller	425
6681 Data Channel Converter	310
TOTAL:	$47,145

* Provided for operating system purposes.

CENTRAL PROCESSOR

.1 GENERAL

.11 Identity: . . . . Control Data 6400 Central Processor.

.12 Description

See Section 260:051 for a comprehensive description of the characteristics of all the Control Data 6000 Series Central Processors.

See Section 263:011 for a summary of the distinguishing features of the Control Data 6400 Central Processor as used in Control Data 6400 computer systems.

The Instruction Times and Processor Performance Times for the Control Data 6400 Central Processor, in fixed-point and floating-point arithmetic modes, are listed below. See Paragraphs 4:050.41 and 4:050.42 of the Users' Guide for the definitions of these standard measures of central processor performance.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
- Add-subtract: 0.6
- Multiply: . . . . instruction not available.
- Divide: . . . . instruction not available.

.412 Floating point —
- Add-subtract: 1.1
- Multiply: 5.7
- Divide: 5.6

.413 Additional allowance for —
- Indexing: . . . . not used.
- Indirect addressing: . 1.0
- Recomplementing: . . 0

.414 Control –
- Compare: 1.2
- Branch: 1.2
- Compare and branch: 1.2

.415 Counter control —
- Step: 0.5
- Step and test: . . . . . instruction not available.
- Test: 1.2

.416 Edit: . . . . instruction not available.

.417 Convert: . . . . instruction not available.

.418 Shift: 0.6

.42 Processor Performance in Microseconds

	Fixed point	Floating point
.421 For random addresses —		
$c = a + b$:	2.1	2.0
$b = a + b$:	2.1	2.0
Sum N items:	1.1N	1.0N
$c = ab$:	—	7.1
$c = a/b$:	—	7.1
.422 For arrays of data —		
$c_i = a_i + b_j$:	4.3	4.2
$b_j = a_i + b_j$:	4.3	4.2
Sum N items:	3.9N	3.8N
$c = c + a_ib_j$:	—	6.8

.423 Branch based on comparison —
- Numeric data: . . . . . 1.0 + 6.1N
- Alphabetic data: . . . . 1.0 + 6.1N

.424 Switching –
- Unchecked: 3.4
- Checked: 6.3
- List search: . . . . . . 1.0 + 5.1N

.425 Format control: . . . . . normally performed by Peripheral Processors.

.426 Table lookup, per comparison —
- For a match: 5.1
- For least or greatest: 4.1
- For interpolation point: 5.1

.427 Bit indicators —
- Set bit in separate location: 1.0
- Set bit in pattern: . . . 2.4
- Test bit in separate location: 1.7
- Test bit in pattern: . . 2.6
- Test AND for B bits: 3.1
- Test OR for B bits: . 3.1

.428 Moving —
- With self: . . . . 0.5 million words/sec.
- With a Peripheral Processor Memory: 2 million words/sec.
- With an Extended Core Memory: . . . . 10 million words/sec.

STANDARD EDP REPORTS

PERIPHERAL AND CONTROL PROCESSORS

.1 GENERAL

.11 Identity: . . . . Control Data 6400 Peripheral and Control Processors.

.12 Description

See Section 260:052 for a comprehensive description of the functional characteristics of all the Control Data 6000 Series Peripheral and Control Processors.

The Instruction Times and Processor Performance times for the Control Data 6400 Peripheral and Control Processors, in the fixed-point binary arithmetic mode, are listed below. See Paragraphs 4:050.41 and 4:050.42 of the Users' Guide for the definitions of these standard measures of processor performance.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
- Add-subtract: 2.0
- Multiply: . . . . not available.
- Divide: . . . . not available.

.412 Floating point: . . . . . not available.

.413 Additional allowance for —
- Indexing: 1.0
- Indirect addressing: 1.0

.414 Control —
- Compare: . . . . not available.
- Branch: 1.0
- Compare and branch: . . . . not available.

.415 Counter control —
- Step: 4.0
- Step and test: . . . . . not available.
- Test: 2.0

.416 Edit: . . . . not available.

.417 Convert: . . . . not available.

.418 Shift: 1.0

.42 Processor Performance in Microseconds

.421 For random addresses —
- c = a + b: 6.0
- b = a + b: 3.0
- Sum N items: 2.0N

.422 For arrays of data —
- $c_i = a_i + b_j$: 17.0
- $b_j = a_i + b_j$: 14.0
- Sum N items: 5.0N

.423 Branch based on comparison —
- Numeric data: 60
- Alphabetic data: . . . 60

.424 Switching —
- Unchecked: 22
- Checked: 34
- List search: . . . . . 14 + 10CN, where C = number of characters in the item.

.425 Format control, per character —
- Unpack: . . . . ?
- Compose: . . . . ?

.426 Table lookup, per comparison —
- For a match: . . . . . . 10C.
- For least or greatest: . . . . 25.
- For interpolation point: . . . . 25.

.427 Bit indicators —
- Set bit in separate location: . . . . 3.
- Set bit in pattern: . . . 9.
- Test bit in separate location: . . . . 2.
- Test bit in pattern: . . 8.
- Test AND for B bits: . 8.
- Test OR for B bits: . 8.

.428 Moving: . . . . 5 + 2.5C, where C = number of 6-bit characters moved.

SIMULTANEOUS OPERATIONS

A Control Data 6400 computer system can concurrently:

- Execute one Central Processor machine instruction (or two using the Dual Processor configuration); and
- Perform 10 independent peripheral programs, one in each of the Peripheral and Control Processors; and
- Perform an additional 120 independent peripheral programs through use of the full complement of 12 Augmented Input-Output Buffer subsystems; and
- Access up to 10 banks of Central Memory; and
- Perform a mass data transfer between Central Memory and Extended Core Storage; and
- Control up to 12 input-output operations, one on each Data Channel; and
- Control as many further input-output operations as there are additional Data Channels and/or multiplexing and buffering capabilities of individual I/O devices and controllers.

The Central Processor is normally not delayed in any way by input-output operations. However, a Peripheral and Control Processor is delayed to some extent during each I/O operation. Table I lists the amount of Peripheral and Control Processor input-output delay for each of the peripheral units that can be connected to the Control Data 6400 computer system, including several devices originally used with the Control Data 3000 Series.

Also included in Table I is the amount of Data Channel time that is consumed during each input-output operation. Because the data transfer rate between Data Channels and Peripheral Processors is so high (2 million characters per second), the individual Data Channels can be effectively multiplexed between several input-output devices. The extent of Data Channel multiplexing varies from one peripheral device to another and is therefore discussed in the individual report sections that describe the various peripheral devices.

TABLE I: SIMULTANEOUS OPERATIONS

DEVICE	Cycle Time, msec.	Start Time				Data Transmission				Stop Time			
		Time, msec.	PP Use %	CP Use %	Channel Use	Time, msec.	PP Use %	CP Use %	Channel Use	Time, msec.	PP Use %	CP Use %	Channel Use
828, 838 Disk Files	52.0	250 av	0.0	0.0	1 msec	Var	6.4 or 11.0	0.0	Yes	0.0	---	---	---
852 Disk Transport	40.0	77.5 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
853 Disk Transport	25.0	70.0 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
854 Disk Transport	25.0	70.0 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
6603 Disk File	66.6	93.0 av	100.0	---	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
6607/6608 Disk File	52.5	59.3 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
3235 Drum Storage	34.4	17.2 av	0.0	0.0	1 msec	Var	16.8	0.0	Yes	0.0	---	---	---
861 Drum Storage	34.4	17.2 av	0.0	0.0	?	Var	200.0	0.0	Yes	0.0	---	---	---
862 Drum Storage	17.2	8.6 av	0.0	0.0	?	Var	200.0	0.0	Yes	0.0	---	---	---
6430 Extended Core Storage	---	0.0	0.0	0.0	---	Var	0.0	?	No	0.0	---	---	---
405 Card Reader, 1,200 cpm, unbuffered	50.0	18.0	0.0	0.0	Yes	32.0	<0.1	0.0	Yes	0.0	---	---	---
405 Card Reader, 1,200 cpm, buffered	50.0	42.0	0.0	0.0	Yes	8.0	<0.1	0.0	Yes	0.0	---	---	---
415 Card Punch, 250 cpm, unbuffered	240.0	48.0	0.0	0.0	Yes	190.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
415 Card Punch, 250 cpm, buffered	240.0	48.0	<0.1	0.0	2.2 msec	190.0	<0.1	0.0	No	2.0	0.0	0.0	No
523 Card Punch, 100 cpm, unbuffered	600.0	84.0	0.0	0.0	Yes	514.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
523 Card Punch, 100 cpm, buffered	600.0	84.0	<0.1	0.0	2.2 msec	514.0	<0.1	0.0	No	2.0	0.0	0.0	No
544 Card Punch, 250 cpm, unbuffered	240.0	48.0	0.0	0.0	Yes	190.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
544 Card Punch, 250 cpm, buffered	240.0	48.0	<0.1	0.0	2.2 msec	190.0	<0.1	0.0	No	2.0	0.0	0.0	No
3691 Paper Tape Reader, 350 cps	2.9	?	0.0	0.0	Yes	2.9	<0.1	0.0	Yes	2.0	0.0	0.0	No
3691 Paper Tape Punch, 110 cps	9.0	?	0.0	0.0	Yes	9.0	<0.1	0.0	Yes	3.0	0.0	0.0	No
3694 Paper Tape Reader, 1,000 cps	1.0	?	0.0	0.0	Yes	1.0	<0.1	0.0	Yes	0.8	0.0	0.0	No
3694 Paper Tape Punch, 110 cps	9.0	?	0.0	0.0	Yes	9.0	<0.1	0.0	Yes	3.0	0.0	0.0	No
3152 Line Printer, 150 lpm	400 + 9.7LS	0.0	---	---	---	375	?	0.0	0.1 msec	25 + 9.7LS	0.0	0.0	No
1403 Model 2 Printer, 600 lpm	100 + 5LS	0.0	---	---	---	80	?	0.0	0.1 msec	20 + 5LS	0.0	0.0	No
1403 Model 3 Printer, 1,100 lpm	55 + 5LS	0.0	---	---	---	35	?	0.0	0.1 msec	20 + 5LS	0.0	0.0	No
501 Printer, 1,000 lpm	60 + 6.7LS	0.0	---	---	---	45	?	0.0	0.1 msec	13 + 6.7LS	0.0	0.0	No
505 Printer, 500 lpm	120 + 6.7LS	0.0	---	---	---	105	?	0.0	0.1 msec	13 + 6.7LS	0.0	0.0	No
601 Magnetic Tape Unit, 20.8 KC	---	3.0	0.0	0.	Yes	Var	4.1	0.0	Yes	3.0	0.0	0.0	No
603 Magnetic Tape Unit, 41.7 KC	---	2.75	0.0	0.0	Yes	Var	8.3	0.0	Yes	2.25	0.0	0.0	No
604 Magnetic Tape Unit, 60.0 KC	---	2.75	0.0	0.0	Yes	Var	12.0	0.0	Yes	2.25	0.0	0.0	No
606 Magnetic Tape Unit, 83.4 KC	---	2.75	0.0	0.0	Yes	Var	16.7	0.0	Yes	1.75	0.0	0.0	No
607 Magnetic Tape Unit, 120 KC	---	2.75	0.0	0.0	Yes	Var	24.0	0.0	Yes	1.75	0.0	0.0	No
626 Magnetic Tape Unit, 240 KC	---	2.75	0.0	0.0	Yes	Var	48.0	0.0	Yes	1.75	0.0	0.0	No
692 Magnetic Tape Unit, 30 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
694 Magnetic Tape Unit, 60 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
696 Magnetic Tape Unit, 90 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
3692 Program Controlled Input-Output Typewriter	67	0.0	---	---	---	Var	0.0	0.0	Yes	0.0	---	---	---
3293 Incremental Plotter	3.3 or 5.0	100.0	0.0	0.0	No	No	0.0	0.0	No	100.0	0.0	0.0	No

Note: PP Use is the percentage of the total input-output time during which a single Peripheral and Control Processor is used. In the calculation of Peripheral and Control Processor usage, it is assumed that temporary I/O storage is provided by the 6607 System Disk, except in those cases in which the I/O operation is itself a disc file or drum operation.

CP Use is the percentage of the total input-output time during which the Central Processor is used.

---

av: Average time; see main report section on this device for details.
LS: Number of lines skipped between successive printed lines.
Var: Data transmission time varies with record length.

CDC 6600

Control Data Corporation

AUERBACH

STANDARD EDP REPORTS

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CDC 6600

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INTRODUCTION

The Control Data 6600 computer system is characterized by a Central Processor that can execute up to ten instructions simultaneously and can utilize an eight-word instruction stack for register-speed program looping operations. The Central Processor functions at an internal clock-cycle rate of 100 nanoseconds. The 6600 can concurrently access up to 10 core storage locations in the Central Memory, which features a basic cycle time of one microsecond per 60-bit word. The ten Peripheral Processors that form an integral part of the 6600 system have fairly complete instruction sets and individual, independent core storage units of 4,096 12-bit words, with a cycle time of one microsecond. When auxiliary mass storage is included in a 6600 system in the form of the Extended Core Storage unit, the system is well suited for time-sharing applications using the "roll-in/roll-out" mode of operation.

This report concentrates upon the performance of the Control Data 6600 system in particular. All general characteristics of the 6000 Series hardware and software are described in Computer System Report 260: Control Data 6000 Series — General.

The System Configuration section which follows shows the Control Data 6600 in the following standard configurations:

VIIA:	10-Tape General System (Integrated)
VIIIA:	20-Tape General System (Integrated).

These configurations were selected because multiprogramming and multiprocessing are the 6600's standard modes of operation. To reflect this type of operation, the main processing runs and the input and output data transcription runs in our standard benchmark problems are assumed to be performed in parallel.

The system configurations are arranged according to the rules in the Users' Guide, page 4:030.120, and any significant deviations from the standard specifications are listed. The principal deviations include the ten Peripheral Processors that are standard in every 6000 Series system, and the System Disk, required for use by the SIPROS operating system.

Section 260:051 provides detailed central processor timing data for the 6600. See Section 260:051 for the other characteristics of the program-compatible 6000 Series processors.

System Performance measurements for the 6600 computer system are presented in Section 260:201, together with the measurements for the 6400 and 6800 systems for ease of comparison.

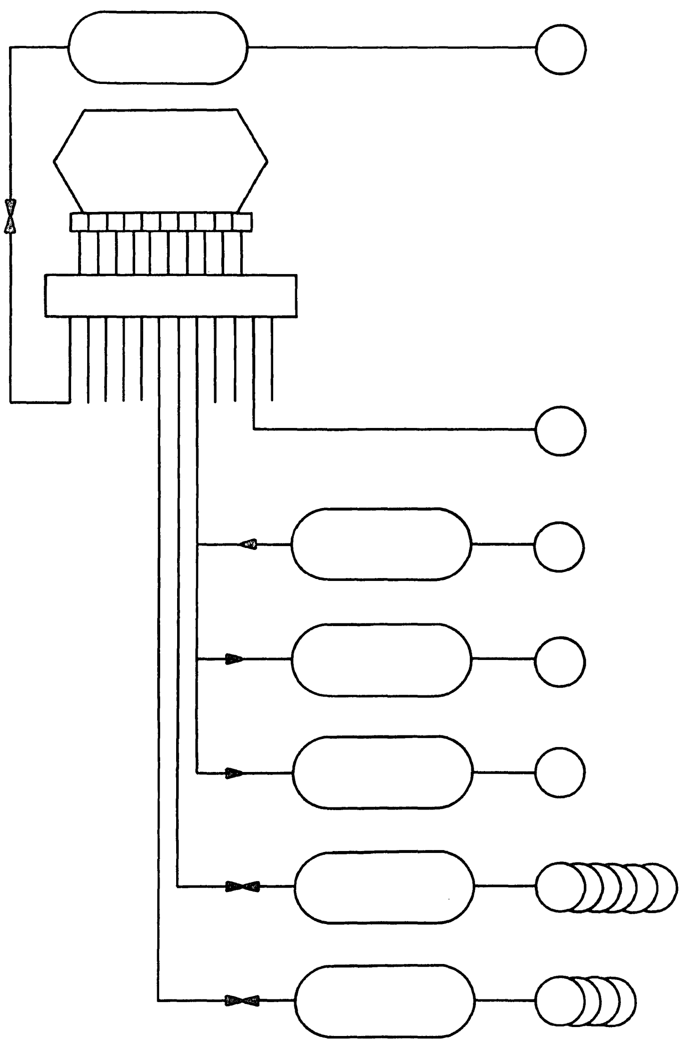
Software for all 6000 Series systems is described in Sections 260:151 through 260:191.

SYSTEM CONFIGURATION

The basic Control Data 6000 Series system configuration possibilities are summarized in report Section 260:031. This section shows the Control Data 6600 Computer System arranged in two configurations that conform to our Standard Configurations, as defined in the Users' Guide, page 4:030.120. Note that the 6681 Data Channel Converter is used in each configuration. This device permits the use of any of the peripheral units that are used with the Control Data 3000 Series computer systems.

.1 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: . . . . card reader is 140% faster.
card punch is 150% faster.
200,000 additional characters of core storage.

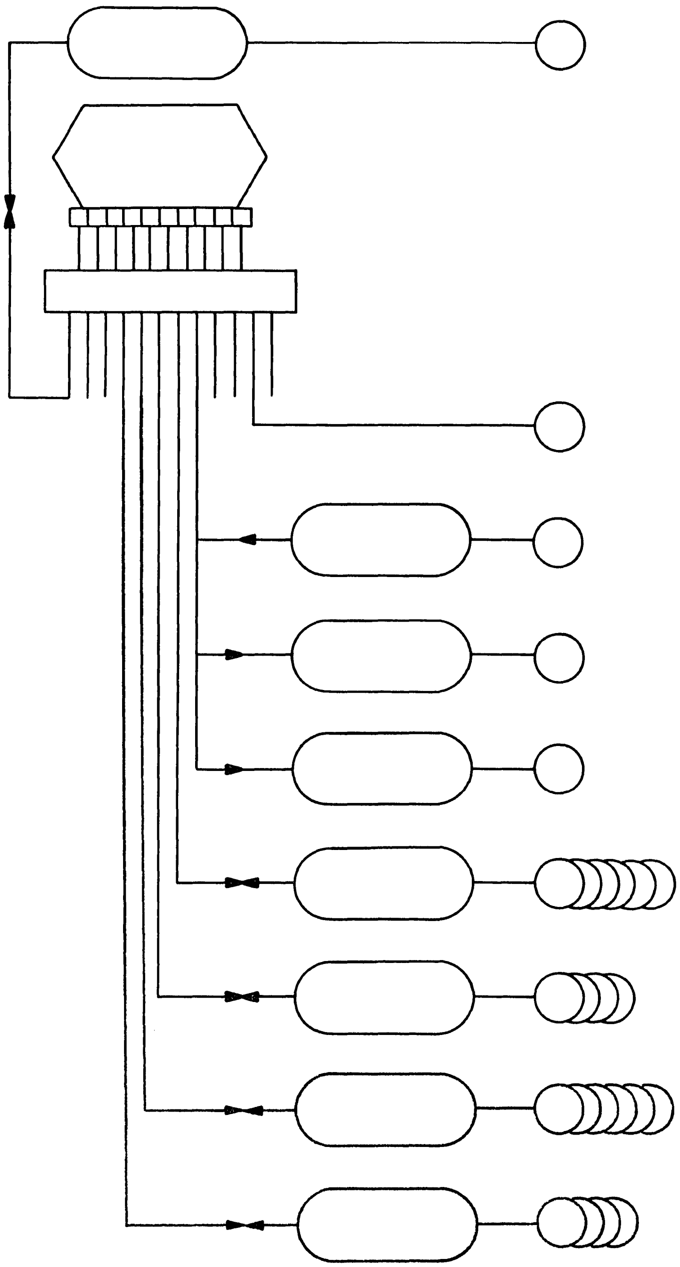


Equipment	Rental
6607 Disk System* with controller	$ 4,900
6600 Central Processor with 32K 60-bit words of storage	
10 Peripheral Processors, each with 4K 12-bit words of storage	41,900
10 x 12 Bus	
12 Input/Output Channels	
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
6681 Data Channel Converter	310
604 60KC Magnetic Tape Units (6)	3,600
3229 Controller	600
6681 Data Channel Converter	310
604 60KC Magnetic Tape Units (4)	2,400
3228 Controller	425
6681 Data Channel Converter	310
TOTAL:	$58,050

* Provided for operating system purposes.

.2 20-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIIA

Deviations from Standard Configuration: .... card reader is 20% faster.
card punch is 25% faster.
80,000 additional characters of core storage.



Equipment	Rental
6607 Disk System* with controller (84 million characters)	$ 4,900
6600 Central Processor with 32K 60-bit words of storage	
10 Peripheral Processors, each with 4K 12-bit words of storage.	41,900
10 x 12 Bus	
12 Input/Output Channels	
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (6)	5,250
3229 Controller	600
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (4)	3,500
3228 Controller	425
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (6)	5,250
3229 Controller	600
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (4)	3,500
3228 Controller	425
6681 Data Channel Converter	310
TOTAL:	$71,195

* Provided for operating system purposes.

CENTRAL PROCESSOR

.1 GENERAL

.11 Identity: . . . . Control Data 6600 Central Processor.

.12 Description

See Section 260:051 for a comprehensive description of the characteristics of all the Control Data 6000 Series Central Processors.

See Section 264:011 for a summary of the distinguishing features of the Control Data 6600 Central Processor as used in Control Data 6600 computer systems.

The Instruction Times and Processor Performance Times for the Control Data 6600 Central Processor, in fixed-point and floating-point arithmetic modes, are listed below. See Paragraphs 4:050.41 and 4:050.42 of the Users' Guide for the definitions of these standard measures of central processor performance. The Processor Performance Times shown in Paragraph .42 of this section assume that all counts, increment values, and sub-totals are maintained in the 24 central registers, and that all other operands are held in Central Memory.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
- Add-subtract: 0.3
- Multiply: . . . . instruction not available.
- Divide: . . . . instruction not available.

.412 Floating point —
- Add-subtract: 0.4
- Multiply: 1.0
- Divide: 2.9

.413 Additional allowance for —
- Indexing: . . . . not used.
- Indirect addressing: . 1.0
- Recomplementing: . . 0

.414 Control —
- Compare: 0.9
- Branch: 0.9
- Compare and branch: 0.9

.415 Counter control —
- Step: 0.3
- Step and test: . . . . . . instruction not available.
- Test: 0.8

.416 Edit: . . . . instruction not available.

.417 Convert: . . . . instruction not available.

.418 Shift: 0.3

.42 Processor Performance in Microseconds

	Fixed point	Floating point
.421 For random addresses —		
$c = a + b$:	1.0	1.0
$b = a + b$:	1.0	1.0
Sum N items:	0.6N	0.6N
$c = ab$:	-	1.2
$c = a/b$:	-	3.1

	Fixed point	Floating point
.422 For arrays of data —		
$c_i = a_i + b_j$:	2.0	2.0
$b_j = a_i + b_j$:	2.0	2.0
Sum N items:	1.2N	1.2N
$c = c + a_i b_j$:	-	1.2

.423 Branch based on comparison —
- Numeric data: . . . . . 2.0 + 2.1N
- Alphabetic data: . . . . 2.0 + 2.1N

.424 Switching —
- Unchecked: 4.4
- Checked: 5.2
- List search: . . . . . . 1.4 + 3.0N

.425 Format control: . . . . . normally performed by Peripheral Processors.

.426 Table lookup, per comparison —
- For a match: 1.1
- For least or greatest: 1.1
- For interpolation point: 1.8

.427 Bit indicators —
- Set bit in separate location: 0.3
- Set bit in pattern: . . . 0.3
- Test bit in separate location: 1.0
- Test bit in pattern: . . 1.3
- Test AND for B bits: . 2.0
- Test OR for B bits: . . 2.0

.428 Moving —
- With self: . . . . 1 million words/sec.
- With a Peripheral Processor Memory: 2 million words/sec.
- With an Extended Core Memory: . . . . 10 million words/sec.

PERIPHERAL AND CONTROL PROCESSORS

.1 GENERAL

.11 Identity: . . . . Control Data 6600 Peripheral and Control Processors.

.12 Description

See Section 260:052 for a comprehensive description of the functional characteristics of all the Control Data 6000 Series Peripheral and Control Processors.

The Instruction Times and Processor Performance times for the Control Data 6600 Peripheral and Control Processors, in the fixed-point binary arithmetic mode, are listed below. See Paragraphs 4:050.41 and 4:050.42 of the Users' Guide for the definitions of these standard measures of processor performance.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
- Add-subtract: 2.0
- Multiply: . . . . not available.
- Divide: . . . . not available.

.412 Floating point: not available.

.413 Additional allowance for —
- Indexing: 1.0
- Indirect addressing: . . 1.0

.414 Control —
- Compare: . . . . not available.
- Branch: 1.0
- Compare and branch: . not available.

.415 Counter control —
- Step: 4.0
- Step and test: . . . . . . not available.
- Test: 2.0

.416 Edit: . . . . not available.

.417 Convert: . . . . not available.

.418 Shift: 1.0

.42 Processor Performance in Microseconds

.421 For random addresses —
- c = a + b: 6.0
- b = a + b: 3.0
- Sum N items: 2.0N

.422 For arrays of data —
- $c_i = a_i + b_j$: 17.0
- $b_j = a_i + b_j$: 14.0
- Sum N items: 5.0N

.423 Branch based on comparison —
- Numeric data: 60
- Alphabetic data: 60

.424 Switching —
- Unchecked: 22
- Checked: 34
- List search: . . . . . . 14 + 10CN, where C = number of characters in the item.

.425 Format control, per character —
- Unpack: . . . . ?
- Compose: . . . . ?

.426 Table lookup, per comparison —
- For a match: 10C
- For least or greatest: 25
- For interpolation point: 25

.427 Bit indicators —
- Set bit in separate location: 3
- Set bit in pattern: . . 9
- Test bit in separate location: 2
- Test bit in pattern: . . 8
- Test AND for B bits: . 8
- Test OR for B bits: . . 8

.428 Moving: . . . . 5 + 2.5C, where C = number of 6-bit characters moved.

SIMULTANEOUS OPERATIONS

A Control Data 6600 computer system can concurrently:

- Execute up to 10 Central Processor machine instructions; and
- Perform 10 independent peripheral programs, one in each of the Peripheral and Control Processors; and
- Perform an additional 120 independent peripheral programs through use of the full complement of 12 Augmented Input-Output Buffer subsystems; and
- Access up to 10 banks of Central Memory; and
- Perform a mass data transfer between Central Memory and Extended Core Storage; and
- Control up to 12 input-output operations, one on each Data Channel; and
- Control as many further input-output operations as there are additional Data Channels and/or multiplexing and buffering capabilities of individual I/O devices and controllers.

The Central Processor is normally not delayed in any way by input-output operations. However, a Peripheral and Control Processor is delayed to some extent during each I/O operation. Table I lists the amount of Peripheral and Control Processor input-output delay for each of the peripheral units that can be connected to the Control Data 6600 computer system, including several devices originally used with the Control Data 3000 Series.

Also included in Table I is the amount of Data Channel time that is consumed during each input-output operation. Because the data transfer rate between Data Channels and Peripheral Processors is so high (2 million characters per second), the individual Data Channels can be effectively multiplexed between several input-output devices. The extent of Data Channel multiplexing varies from one peripheral device to another and is therefore discussed in the individual report sections that describe the various peripheral devices.

TABLE I: SIMULTANEOUS OPERATIONS

DEVICE	Cycle Time, msec.	Start Time				Data Transmission				Stop Time			
		Time, msec.	PP Use %	CP Use %	Channel Use	Time, msec.	PP Use %	CP Use %	Channel Use	Time, msec.	PP Use %	CP Use %	Channel Use
828, 838 Disk Files	52.0	250 av	0.0	0.0	1 msec	Var	6.4 or 11.0	0.0	Yes	0.0	---	---	---
852 Disk Transport	40.0	77.5 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	---	---	---
853 Disk Transport	25.0	70.0 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	---	---	---
854 Disk Transport	25.0	70.0 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	---	---	---
6603 Disk File	66.6	93.0 av	100.0	---	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
6607/6608 Disk File	52.5	59.3 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
3236 Drum Storage	34.4	17.2 av	0.0	0.0	1 msec	Var	16.8	0.0	Yes	0.0	---	---	---
861 Drum Storage	34.4	17.2 av	0.0	0.0	?	Var	200.0	0.0	Yes	0.0	---	---	---
862 Drum Storage	17.2	8.6 av	0.0	0.0	?	Var	200.0	0.0	Yes	0.0	---	---	---
6630 Extended Core Storage	---	0.0	0.0	0.0	---	Var	0.0	?	No	0.0	---	---	---
405 Card Reader, 1,200 cpm, unbuffered	50.0	18.0	0.0	0.0	Yes	32.0	<0.1	0.0	Yes	0.0	---	---	---
405 Card Reader, 1,200 cpm, buffered	50.0	42.0	0.0	0.0	Yes	8.0	<0.1	0.0	Yes	0.0	---	---	---
415 Card Punch, 250 cpm, unbuffered	240.0	48.0	0.0	0.0	Yes	190.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
415 Card Punch, 250 cpm, buffered	240.0	48.0	<0.1	0.0	2.2 msec	190.0	<0.1	0.0	No	2.0	0.0	0.0	No
523 Card Punch, 100 cpm, unbuffered	600.0	84.0	0.0	0.0	Yes	514.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
523 Card Punch, 100 cpm, buffered	600.0	84.0	<0.1	0.0	2.2 msec	514.0	<0.1	0.0	No	2.0	0.0	0.0	No
544 Card Punch, 250 cpm, unbuffered	240.0	48.0	0.0	0.0	Yes	190.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
544 Card Punch, 250 cpm, buffered	240.0	48.0	<0.1	0.0	2.2 msec	190.0	<0.1	0.0	No	2.0	0.0	0.0	No
3691 Paper Tape Reader, 350 cps	2.9	?	0.0	0.0	Yes	2.9	<0.1	0.0	Yes	2.0	0.0	0.0	No
3691 Paper Tape Punch, 110 cps	9.0	?	0.0	0.0	Yes	9.0	<0.1	0.0	Yes	3.0	0.0	0.0	No
3694 Paper Tape Reader, 1,000 cps	1.0	?	0.0	0.0	Yes	1.0	<0.1	0.0	Yes	0.8	0.0	0.0	No
3694 Paper Tape Punch, 110 cps	9.0	?	0.0	0.0	Yes	9.0	<0.1	0.0	Yes	3.0	0.0	0.0	No
3152 Line Printer, 150 lpm	400 + 9.7LS	0.0	---	---	---	375.0	?	0.0	0.1 msec	25 + 9.7LS	0.0	0.0	No
1403 Model 2 Printer, 600 lpm	100 + 5LS	0.0	---	---	---	80.0	?	0.0	0.1 msec	20 + 5LS	0.0	0.0	No
1403 Model 3 Printer, 1,100 lpm	55 + 5LS	0.0	---	---	---	35.0	?	0.0	0.1 msec	20 + 5LS	0.0	0.0	No
501 Printer, 1,000 lpm	60 + 6.7LS	0.0	---	---	---	45.0	?	0.0	0.1 msec	13 + 6.7LS	0.0	0.0	No
505 Printer, 500 lpm	120 + 6.7LS	0.0	---	---	---	105.0	?	0.0	0.1 msec	13 + 6.7LS	0.0	0.0	No
601 Magnetic Tape Unit, 20.8 KC	---	3.0	0.0	0.0	Yes	Var	4.1	0.0	Yes	3.0	0.0	0.0	No
603 Magnetic Tape Unit, 41.7 KC	---	2.75	0.0	0.0	Yes	Var	8.3	0.0	Yes	2.25	0.0	0.0	No
604 Magnetic Tape Unit, 60.0 KC	---	2.75	0.0	0.0	Yes	Var	12.0	0.0	Yes	2.25	0.0	0.0	No
606 Magnetic Tape Unit, 83.4 KC	---	2.75	0.0	0.0	Yes	Var	16.7	0.0	Yes	1.75	0.0	0.0	No
607 Magnetic Tape Unit, 120 KC	---	2.75	0.0	0.0	Yes	Var	24.0	0.0	Yes	1.75	0.0	0.0	No
626 Magnetic Tape Unit, 240 KC	---	2.75	0.0	0.0	Yes	Var	48.0	0.0	Yes	1.75	0.0	0.0	No
692 Magnetic Tape Unit, 30 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
694 Magnetic Tape Unit, 60 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
696 Magnetic Tape Unit, 90 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
3692 Program Controlled Input-Output Typewriter	67	0.0	---	---	---	Var	0.0	0.0	Yes	0.0	---	---	---
3293 Incremental Plotter	3.3 or 5.0	100.0	0.0	0.0	No	No	0.0	0.0	No	100.0	0.0	0.0	No

Note: PP Use is the percentage of the total input-output time during which a single Peripheral and Control Processor is used. In the calculation of Peripheral and Control Processor usage, it is assumed that temporary I/O storage is provided by the 6607 System Disk, except in those cases in which the I/O operation is itself a disc file or drum operation.

CP Use is the percentage of the total input-output time during which the Central Processor is used.

av: Average time; see main report section on this device for details.
LS: Number of lines skipped between successive printed lines.
Var: Data transmission time varies with record length.

CDC 6800

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INTRODUCTION

The Control Data 6800 computer system features a Central Processor that can execute up to ten instructions simultaneously at an internal clock-cycle rate of 25 nanoseconds. The Central Processor also utilizes an eight-word instruction stack for register-speed program looping operations. Up to 10 banks of Central Memory can be accessed concurrently, with a basic cycle time of 250 nanoseconds per 60-bit word. The ten Peripheral Processors that form an integral part of the 6800 system utilize fairly complete instruction sets and independent core storage units of 4,096 12-bit words, with a cycle time of 250 nanoseconds. When auxiliary mass storage is included in a 6800 system in the form of the Extended Core Storage unit, the system is well suited for time-sharing applications using the "roll-in/roll-out" mode of operation.

This report concentrates upon the performance of the Control Data 6800 system in particular. All general characteristics of the 6000 Series hardware and software are described in Computer System Report 260: Control Data 6000 Series — General.

The System Configuration section which follows shows the Control Data 6800 in the following standard configurations:

VIIA: 10-Tape General System (Integrated)
VIIIA: 20-Tape General System (Integrated).

These configurations were selected because multiprogramming and multiprocessing are the 6800's standard modes of operation. To reflect this type of operation, the main processing runs and the input and output data in our standard benchmark problems are assumed to be performed in parallel.

The system configurations are arranged according to the rules in the Users' Guide, page 4:030.120, and any significant deviations from the standard specifications are listed. The principal deviations include the ten Peripheral Processors that are standard in every 6000 Series system, and the System Disk, required for use by the SIPROS operating system.

Section 260:051 provides detailed central processor timing data for the 6800. See Section 260:051 for the other characteristics of the program-compatible 6000 Series processors.

System Performance measurements for the 6800 computer system are presented in Section 260:201, together with the measurements of the 6400 and 6600 systems for ease of comparison.

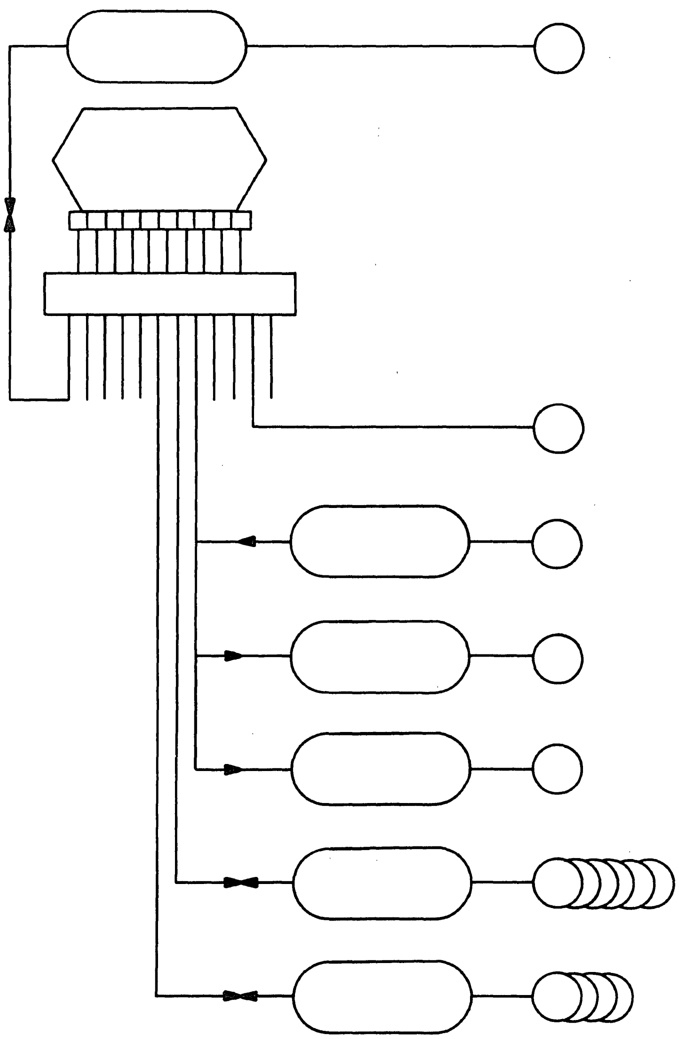
Software for all 6000 Series systems is described in Sections 260:151 through 260:191.

SYSTEM CONFIGURATION

The basic Control Data 6000 Series system configuration possibilities are summarized in report Section 260:031. This section shows the Control Data 6800 Computer System arranged in two configurations that conform to our Standard Configurations, as defined in the Users' Guide, page 4:030.120. Note that the 6681 Data Channel Converter is used in each configuration. This device permits the use of any of the peripheral units that are used with the Control Data 3000 Series computer systems.

.1 10-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIA

Deviations from Standard Configuration: .... card reader is 140% faster.
card punch is 150% faster.
200,000 additional characters of core storage.

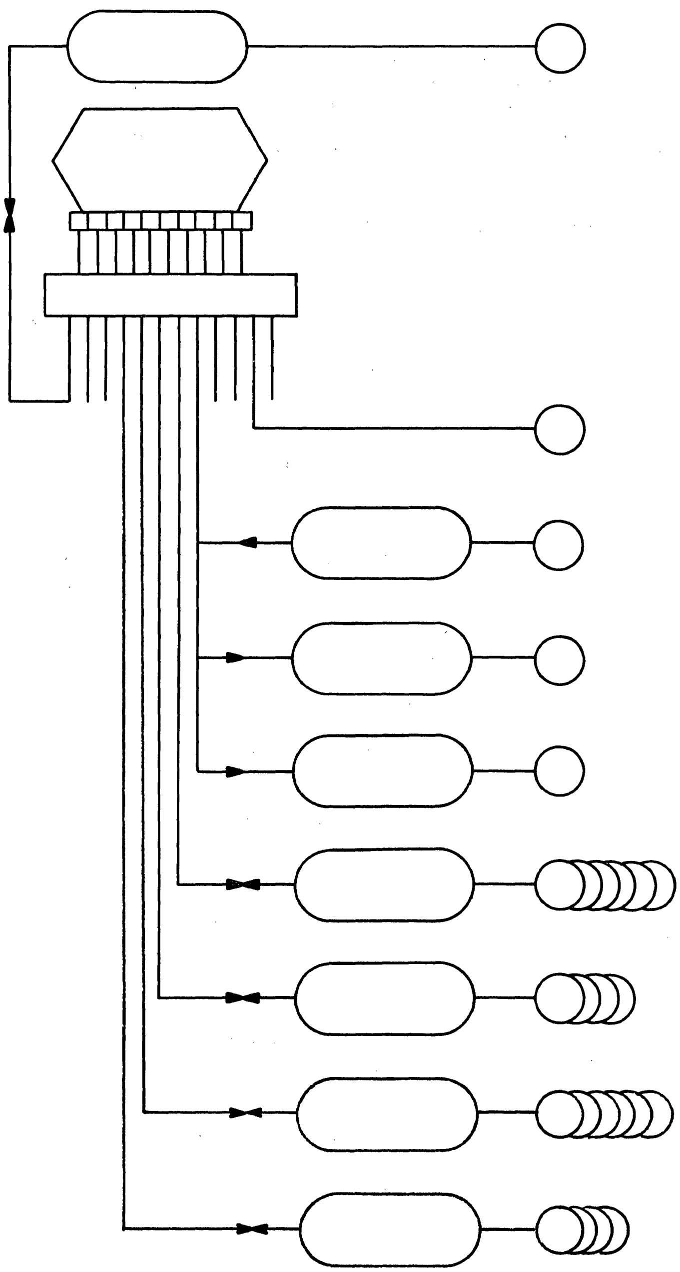


Equipment	Rental
6607 Disk System* with controller (84 million characters)	$ 4,900
6800 Central Processor with 32K 60-bit words of storage; 10 Peripheral Processors, each with 4K 12-bit words of storage; 10 x 12 Bus; 12 Input/Output Channels	41,900
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Control	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Control	515
6681 Data Channel Converter	310
604 60KC Magnetic Tape Units (6)	3,600
3229 Controller	600
6681 Data Channel Converter	310
604 60KC Magnetic Tape Units (4)	2,400
3228 Controller	425
6681 Data Channel Converter	310
TOTAL:	$57,740

* Provided for operating system purposes.

.2 20-TAPE GENERAL SYSTEM (INTEGRATED); CONFIGURATION VIIIA

Deviations from Standard Configuration: . . . . card reader is 20% faster.
card punch is 25% faster.
80,000 additional characters of core storage.



Equipment	Rental
6607 Disk System* with controller (84 million characters)	$ 4,900
6800 Central Processor with 32K 60-bit words of storage	
10 Peripheral Processors, each with 4K 12-bit words of storage	41,900
10 x 12 Bus	
12 Input/Output Channels	
6602 Console Display	900
405 Card Reader (1,200 cpm)	400
3248 Controller	100
415 Card Punch (250 cpm)	295
3446 Controller	450
505 Line Printer (500 lpm)	635
3256 Controller	515
6681 Data Channel Converter	
607 120KC Magnetic Tape Units (6)	5,250
3229 Controller	600
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (4)	3,500
3228 Controller	425
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (6)	5,250
3229 Controller	600
6681 Data Channel Converter	310
607 120KC Magnetic Tape Units (4)	3,500
3228 Controller	425
6681 Data Channel Converter	310
TOTAL:	$70,885

(The rental of 41,900 is bracketed to cover the 6800 Central Processor, 10 Peripheral Processors, 10 x 12 Bus and 12 Input/Output Channels.)

* Provided for operating system purposes.

CENTRAL PROCESSOR

.1 GENERAL

.11 Identity: .... Control Data 6800 Central Processor.

.12 Description

See Section 260:051 for a comprehensive description of the characteristics of all the Control Data 6000 Series Central Processors.

See Section 265:011 for a summary of the distinguishing features of the Control Data 6800 Central Processor as used in Control Data 6800 computer systems.

The Instruction Times and Processor Performance Times for the Control Data 6800 Central Processor, in fixed-point and floating-point arithmetic modes, are listed below. See Paragraphs 4:050.41 and 4:050.42 of the Users' Guide for the definitions of these standard measures of central processor performance. The Processor Performance Times shown in Paragraph .42 of this section assume that all counts, increment values, and sub-totals are maintained in the 24 central registers, and that all other operands are held in Central Memory.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
- Add-subtract: 0.08
- Multiply: .... instruction not available.
- Divide: .... instruction not available.

.412 Floating point —
- Add-subtract: 0.1
- Multiply: 0.25
- Divide: 0.73

.413 Additional allowance for —
- Indexing: .... not used.
- Indirect addressing: . 0.25
- Recomplementing: . . 0

.414 Control —
- Compare: 0.23
- Branch: 0.23
- Compare and branch: 0.23

.415 Counter control —
- Step: 0.08
- Step and test: ..... instruction not available.
- Test: 0.20

.416 Edit: .... instruction not available.
.417 Convert: .... instruction not available.
.418 Shift: 0.075

.42 Processor Performance in Microseconds

	Fixed point	Floating point
.421 For random addresses —		
$c = a + b$:	0.25	0.25
$b = a + b$:	0.25	0.25
Sum N items:	0.15N	0.15N
$c = ab$:	-	0.30
$c = a/b$:	-	0.78

	Fixed point	Floating point
.422 For arrays of data —		
$c_i = a_i + b_j$:	1.25	1.25
$b_j = a_i + b_j$:	1.25	1.25
Sum N items:	0.3N	0.3N
$c = c + a_i b_j$:	-	0.3

.423 Branch based on comparison —
- Numeric data: ..... 0.5 + 0.5N
- Alphabetic data: .... 0.5 + 0.5N

.424 Switching —
- Unchecked: 1.1
- Checked: 1.3
- List search: ...... 0.35 + 0.75N

.425 Format control: ..... normally performed by Peripheral Processors.

.426 Table lookup, per comparison —
- For a match: 0.45
- For least or greatest: 0.28
- For interpolation point: 0.45

.427 Bit indicators —
- Set bit in separate location: 0.05
- Set bit in pattern: . . 0.30
- Test bit in separate location: 0.20
- Test bit in pattern: . . ?
- Test AND for B bits: . 0.40
- Test OR for B bits: . 0.80

.428 Moving —
- With self: .... 4 million words/sec.
- With a Peripheral Processor Memory: 8 million words/sec.
- With an Extended Core Memory: ... 40 million words/sec.

PERIPHERAL AND CONTROL PROCESSORS

.1 GENERAL

.11 Identity: . . . . Control Data 6800 Peripheral and Control Processors

.12 Description

See Section 260:052 for a comprehensive description of the functional characteristics of all the Control Data 6000 Series Peripheral and Control Processors.

The Instruction Times and Processor Performance times for the Control Data 6800 Peripheral and Control Processors, in the fixed-point binary arithmetic mode, are listed below. See Paragraphs 4:050.41 and 4:050.42 of the Users' Guide for the definitions of these standard measures of processor performance.

.4 PROCESSOR SPEEDS

.41 Instruction Times in Microseconds

.411 Fixed point —
- Add-subtract: 0.5
- Multiply: . . . . not available.
- Divide: . . . . not available.

.412 Floating point: . . . . . . not available.

.413 Additional allowance for —
- Indexing: 0.25
- Indirect addressing: . 0.25

.414 Control —
- Compare: . . . . not available.
- Branch: 0.25
- Compare and branch: . not available.

.415 Counter control —
- Step: 1.0
- Step and test: . . . . . . not available.
- Test: 0.5

.416 Edit: . . . . not available.

.417 Convert: . . . . not available.

.418 Shift: 0.25

.42 Processor Performance in Microseconds

.421 For random addresses —
- c = a + b: 1.5
- b = a + b: 1.5
- Sum N items: 0.5N

.422 For arrays of data —
- $c_i = a_i + b_j$: 4.25
- $b_j = a_i + b_j$: 3.50
- Sum N items: 1.25N

.423 Branch based on comparison —
- Numeric data: 15
- Alphabetic data: 15

.424 Switching —
- Unchecked: 5.5
- Checked: 8.5
- List search: . . . . . . 3.5 + 2.5CN, where C = number of characters in the item.

.425 Format control, per character —
- Unpack: . . . . ?
- Compose: . . . . ?

.426 Table lookup, per comparison —
- For a match: 2.5C
- For least or greatest: 6.25
- For interpolation point: 6.25

.427 Bit indicators —
- Set bit in separate location: 0.75
- Set bit in pattern: . . . 2.25
- Test bit in separate location: 0.5
- Test bit in pattern: . . 2.0
- Test AND for B bits: 2.0
- Test OR for B bits: . . 2.0

.428 Moving: . . . . 1.25 + 0.6C, where C = number of 6-bit characters moved.

SIMULTANEOUS OPERATIONS

A Control Data 6800 computer system can concurrently:

- Execute up to 10 Central Processor machine instructions; and
- Perform 10 independent peripheral programs, one in each of the Peripheral and Control Processors; and
- Access up to 10 banks of Central Memory; and
- Perform a mass data transfer between Central Memory and Extended Core Storage; and
- Control up to 12 input-output operations, one on each Data Channel; and
- Control as many further input-output operations as there are additional Data Channels and/or multiplexing and buffering capabilities of individual I/O devices and controllers.

The Central Processor is normally not delayed in any way by input-output operations. However, a Peripheral and Control Processor is delayed to some extent during each I/O operation. Table I lists the amount of Peripheral and Control Processor input-output delay for each of the peripheral units that can be connected to the Control Data 6800 computer system, including several devices originally used with the Control Data 3000 Series.

Also included in Table I is the amount of Data Channel time that is consumed during each input-output operation. Because the data transfer rate between Data Channels and Peripheral Processors is so high (8 million characters per second), the individual Data Channels can be effectively multiplexed between several input-output devices. The extent of Data Channel multiplexing varies from one peripheral device to another, and is therefore discussed in the individual report sections that describe the various peripheral devices.

TABLE I: SIMULTANEOUS OPERATIONS

DEVICE	Cycle Time, msec.	Start Time				Data Transmission				Stop Time			
		Time, msec.	PP Use %	CP Use %	Channel Use	Time, msec.	PP Use %	CP Use %	Channel Use	Time, msec.	PP Use %	CP Use %	Channel Use
828, 838 Disk Files	52.0	250 av	0.0	0.0	1 msec	Var	1.6 or 2.2	0.0	Yes	0.0	---	---	---
852 Disk Transport	40.0	77.5 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
853 Disk Transport	25.0	70.0 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
854 Disk Transport	25.0	70.0 av	100.0	0.0	Yes	Var	200.0	0.0	Yes	0.0	0.0	---	---
6603 Disk File	66.6	93.0 av	100.0	---	Yes	Var	?	0.0	Yes	0.0	0.0	---	---
6607/6608 Disk File	52.5	59.3 av	100.0	0.0	Yes	Var	?	0.0	Yes	0.0	0.0	---	---
3236 Drum Storage	34.4	17.2 av	0.0	0.0	1 msec	Var	4.2	0.0	Yes	0.0	---	---	---
861 Drum Storage	34.4	17.2 av	0.0	0.0	?	Var	?	0.0	Yes	0.0	---	---	---
862 Drum Storage	17.2	8.6 av	0.0	0.0	?	Var	?	0.0	Yes	0.0	---	---	---
6830 Extended Core Storage	---	0.0	0.0	0.0	---	Var	0.0	?	No	0.0	---	---	---
405 Card Reader, 1,200 cpm, unbuffered	50.0	18.0	0.0	0.0	Yes	32.0	<0.1	0.0	Yes	0.0	---	---	---
405 Card Reader, 1,200 cpm, buffered	50.0	42.0	0.0	0.0	Yes	8.0	<0.1	0.0	Yes	0.0	---	---	---
415 Card Punch, 250 cpm, unbuffered	240.0	48.0	0.0	0.0	Yes	190.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
415 Card Punch, 250 cpm, buffered	240.0	48.0	<0.1	0.0	2.2 msec	190.0	<0.1	0.0	No	2.0	0.0	0.0	No
523 Card Punch, 100 cpm, unbuffered	600.0	84.0	0.0	0.0	Yes	514.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
523 Card Punch, 100 cpm, buffered	600.0	84.0	<0.1	0.0	2.2 msec	514.0	<0.1	0.0	No	2.0	0.0	0.0	No
544 Card Punch, 250 cpm, unbuffered	240.0	48.0	0.0	0.0	Yes	190.0	<0.1	0.0	Yes	2.0	0.0	0.0	No
544 Card Punch, 250 cpm, buffered	240.0	48.0	<0.1	0.0	2.2 msec	190.0	<0.1	0.0	No	2.0	0.0	0.0	No
3691 Paper Tape Reader, 350 cps	2.9	?	0.0	0.0	Yes	2.9	<0.1	0.0	Yes	2.0	0.0	0.0	No
3691 Paper Tape Punch, 110 cps	9.0	?	0.0	0.0	Yes	9.0	<0.1	0.0	Yes	3.0	0.0	0.0	No
3694 Paper Tape Reader, 1,000 cps	1.0	?	0.0	0.0	Yes	1.0	<0.1	0.0	Yes	0.8	0.0	0.0	No
3694 Paper Tape Punch, 110 cps	9.0	?	0.0	0.0	Yes	9.0	<0.1	0.0	Yes	3.0	0.0	0.0	No
3152 Line Printer, 150 lpm	400 + 9.7LS	0.0	---	---	---	375	<0.1	0.0	0.1 msec	25 + 9.7LS	0.0	0.0	No
1403 Model 2 Printer, 600 lpm	100 + 5LS	0.0	---	---	---	80	<0.1	0.0	0.1 msec	20 + 5LS	0.0	0.0	No
1403 Model 3 Printer, 1,100 lpm	55 + 5LS	0.0	---	---	---	35	<0.1	0.0	0.1 msec	20 + 5LS	0.0	0.0	No
501 Printer, 1,000 lpm	60 + 6.7LS	0.0	---	---	---	45	<0.1	0.0	0.1 msec	13 + 6.7LS	0.0	0.0	No
505 Printer, 500 lpm	120 + 6.7LS	0.0	---	---	---	105	<0.1	0.0	0.1 msec	13 + 6.7LS	0.0	0.0	No
601 Magnetic Tape Unit, 20.8 KC	---	3.0	0.0	0.0	Yes	Var	1.1	0.0	Yes	3.0	0.0	0.0	No
603 Magnetic Tape Unit, 41.7 KC	---	2.75	0.0	0.0	Yes	Var	2.1	0.0	Yes	2.25	0.0	0.0	No
604 Magnetic Tape Unit, 60.0 KC	---	2.75	0.0	0.0	Yes	Var	4.0	0.0	Yes	2.25	0.0	0.0	No
606 Magnetic Tape Unit, 83.4 KC	---	2.75	0.0	0.0	Yes	Var	4.3	0.0	Yes	1.75	0.0	0.0	No
607 Magnetic Tape Unit, 120 KC	---	2.75	0.0	0.0	Yes	Var	6.0	0.0	Yes	1.75	0.0	0.0	No
626 Magnetic Tape Unit, 240 KC	---	2.75	0.0	0.0	Yes	Var	12.0	0.0	Yes	1.75	0.0	0.0	No
692 Magnetic Tape Unit, 30 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
694 Magnetic Tape Unit, 60 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
696 Magnetic Tape Unit, 90 KB	---	?	0.0	0.0	Yes	Var	?	0.0	Yes	?	0.0	0.0	No
3692 Program Controlled Input-Output Typewriter	67	0.0	---	---	---	Var	0.0	0.0	Yes	0.0	---	---	---
3293 Incremental Plotter	3.3 or 5.0	100.0	0.0	0.0	No	No	0.0	0.0	No	100.0	0.0	0.0	No

Note: PP Use is the percentage of the total input-output time during which a single Peripheral and Control Processor is used. In the calculation of Peripheral and Control Processor usage, it is assumed that temporary I/O storage is provided by the 6607 System Disk, except in those cases in which the I/O operation is itself a disc file or drum operation.

CP Use is the percentage of the total input-output time during which the Central Processor is used.

av: Average time; see main report section on this device for details.
LS: Number of lines skipped between successive printed lines.
Var: Data transmission time varies with record length.