RasterOps
RGS14188
User's Guide
Preliminary

REVISION XA1
11/2/90
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1.0 Introduction

The RGS14188 Frame Buffer Controller (FBC) is a high-performance CMOS device that controls the video display and dynamic memory of a bit-mapped graphics system. Although the RGS14188 was designed to provide control of varying size, multi-port DRAMs (VRAMs) it works equally well with standard DRAMS and is easily interfaced to a variety of CPUs and buses.

The principal role of an FBC is to provide an external processor with virtually unlimited access to (video) memory. It eliminates the delays and overhead caused by display update address generation, reloading shift registers, and DRAM refresh. Furthermore, the FBC reduces the amount of hardware needed to interface a RAM array and provides the user with the utmost flexibility.

Highly programmable, the RGS14188 supports a broad range of raster-scan display systems with various resolutions and scan rates. Some of the major functions for RGS14188 FBC are:

Generates all control signals necessary to control 256K, 1, 2, and 4 Megabyte VRAM devices, as well as those necessary to control conventional DRAMs of the same sizes.

Generates the video synchronization and blanking signals necessary to control a CRT monitor.

Accommodates processor data paths of arbitrary widths, working equally well with 8-bit to n-bit processors or bus architectures.

Supports both interlaced and non-interlaced displays of essentially any display resolution.

Automatically generates the special display-update cycles required by VRAM memories to maintain the CRT display.

Automatically performs periodic RAM refresh cycles necessary to maintain the data stored.

The block Diagram of a typical system using the RGS14188 is shown in Figure 1-1.

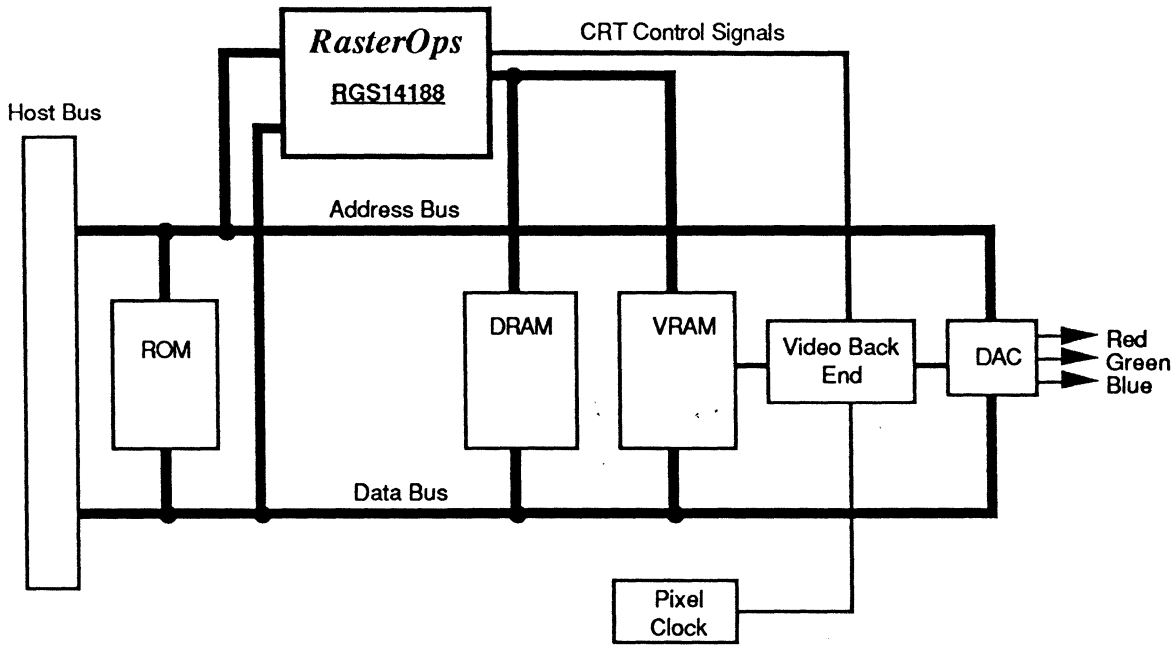


Figure 1-1 Typical System Using the RGS14188

2.0 Pinout and Signal Descriptions

A functional drawing of the RGS14188 is given in Figure 2-1 and the pin number assignments are given in Figure 2-2. A description of each signal is given in the following section. The RGS14188 comes in a 120-terminal plastic quad flat package (PQFP).

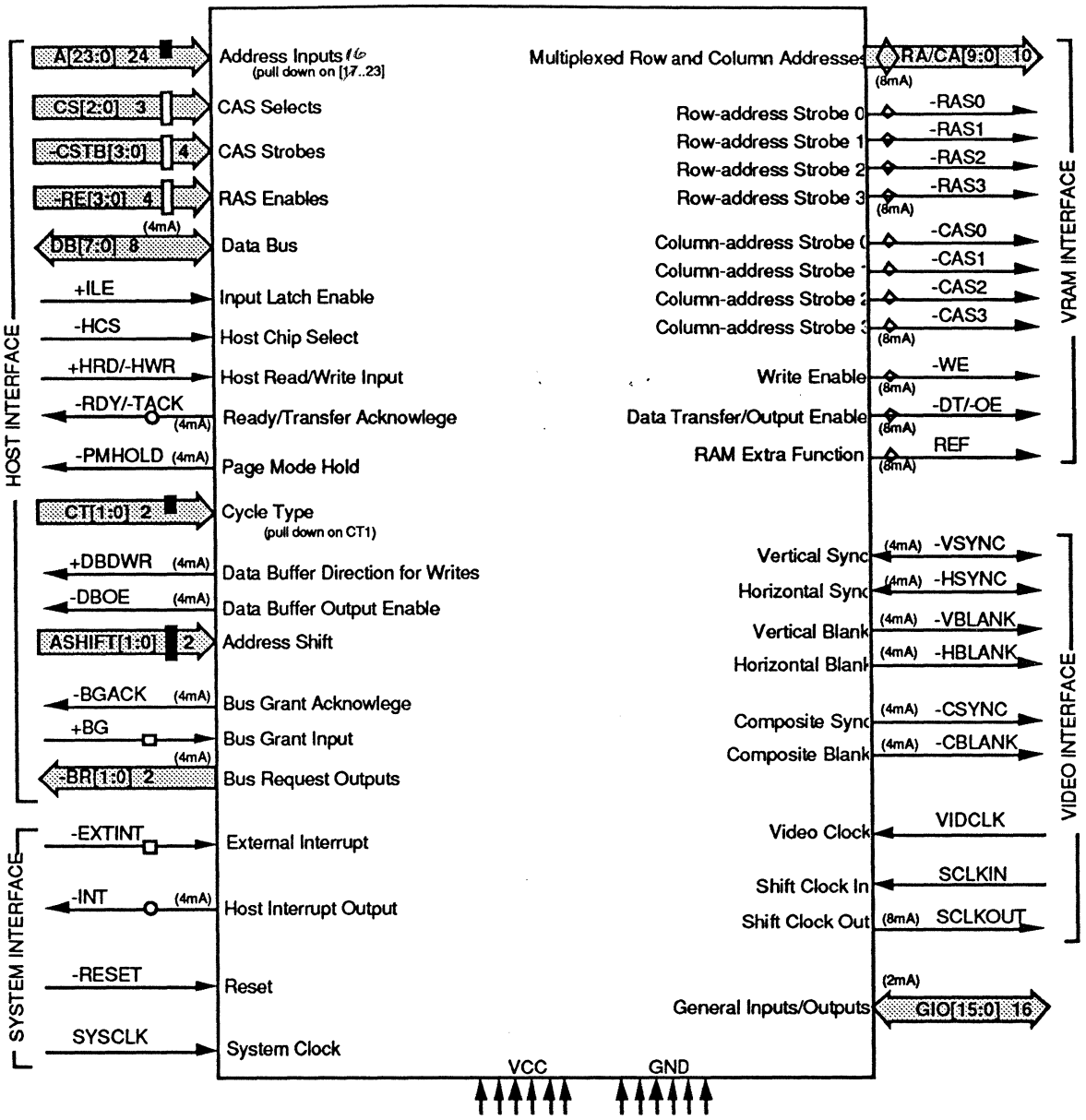


Figure 2-1 RGS14188 Functional Drawing

◇ Tri-state w/pullup
□ in w/ pullup
○ open drain
■ in w/ pulldown

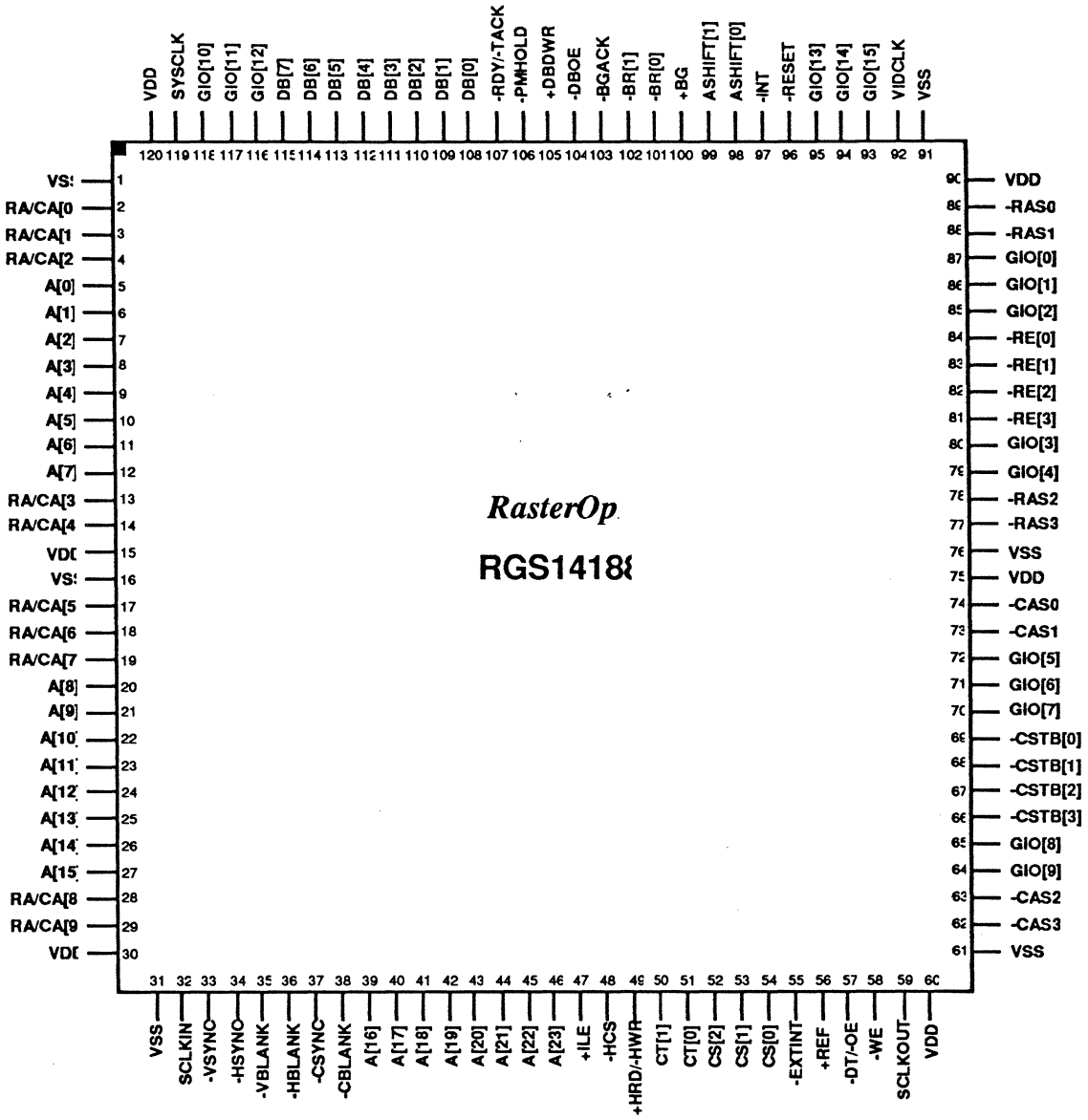


Figure 2-2 RGS14188 Pin Assignments and Signal Names

2.1 Signal Descriptions

A minus (-) in front of a signal name indicates it is asserted active low, a plus (+) indicates it is asserted active high.

Video Interface

VIDCLK - Video Clock (Input) up to 50MHz

The Video Clock is used to increment all the internal screen timing control counters. The period of the Video Clock signal dictates how closely a monitor's

timing can be matched. Typically, Video Clock is harmonically related to the pixel clock used to stream video data from the external shift registers in the memory system to the CRT monitor. The maximum Video Clock frequency is 50 MHz.

SCLKIN - Serial Data Shift Clock In (Input)

The Serial Data Shift Clock input is used to keep track of how many pixels have been displayed. This signal is identical to the VRAM shift clock used to shift the SAM port. The Maximum Frequency of Shift Clock is 50 MHz and it may be Asynchronous to Video Clock and System Clock. This signal must be provided if midline transfers are to be used.

SCLKOUT - Serial Data Shift Clock Out (Output)

This output can be used (possibly buffered) to drive the shift clock signal to the VRAM. It is not necessary to use this output but proper shift clock generation must be done if midline transfers are used.

-VSYNC - Vertical Sync (Input/Output)

Vertical Sync is one of the signals used to control a CRT monitor and operates as an output except when the external sync mode is enabled. Vertical Sync is driven active low during vertical sync intervals whose timing is determined by the values programmed in the RGS14188's vertical timing registers. In External Sync mode , Vertical Sync is an input, and a high to low transition on Vertical Sync resets the vertical counter to the value programmed in the the Vertical Count register. After reset Vertical Sync is configured as an output and forced to its inactive level.

-HSYNC - Horizontal Sync (Input/Output)

Horizontal Sync is one of the signals used to control a CRT monitor and operates as an output except when the external sync mode is enabled. Horizontal Sync is driven active low during horizontal sync intervals whose timing is determined by the values programmed in the RGS14188's horizontal timing registers. In External Sync mode , Horizontal Sync is an input, and a high to low transition on Horizontal Sync resets the horizontal counter to the value programmed in the Horizontal Count register. After reset Horizontal Sync is configured as an output and forced to its inactive level.

-HBLANK - Horizontal Blank (Output)

Horizontal Blank is asserted low for blanking the display during horizontal retrace periods. It is driven active low during horizontal blank intervals whose timing is determined by the values programmed in the RGS14188's horizontal timing registers. After reset Horizontal Blank is forced to its active level.

-VBLANK - Vertical Blank (Output)

Vertical Blank is asserted low for blanking the display during vertical retrace periods. It is driven active low during vertical blank intervals whose timing is determined by the values programmed in the RGS14188's vertical timing registers. After reset ~~Horizontal~~ VERTICAL Blank is forced to its active level.

-CSYNC - Composite Sync (Output)

Composite Sync is the logical OR of the Vertical Sync and Horizontal Sync signals (negative input NOR). It is driven active low during horizontal sync and vertical sync intervals whose timing is determined by the values programmed in the RGS14188's horizontal and vertical timing registers. After reset Composite Sync is forced to its inactive level.

-CBLANK - Composite Blank (Output)

The Composite Blank is the logical OR of the Vertical Blank and Horizontal Blank signals (negative input NOR). It is driven active low during horizontal blank and vertical blank intervals whose timing is determined by the values programmed in the RGS14188's horizontal and vertical timing registers. After reset Composite ~~Sync~~ Blank is forced to its inactive level.

VRAM Interface

RA/CA[9:0] - Row-address/Column-address[9:0] (Outputs)

These are the multiplexed Row and Column address lines for the VRAM or DRAM. The Row-address contains the most significant address bits for the memory. The address output on these lines depends on the memory configuration selected and the state of Address Shift (ASHIFT[1:0]) bits. RA/CA0 is the LSB and RA/CA9 is the MSB.

-RAS[3:0] - Row-address Strobe [3:0] (Outputs)

These active low signals strobe the Row-address into memory. They are controlled by RAS Enable[3:0] on host accesses. During RAM refresh all four Row-address Strobe lines are driven low. During transfer cycles the active Row-address Strobe can be a function of address or all can be driven low at the same time depending on the mode selected in Control Register 3.

-CAS[3:0] - Column-address Strobe[3:0] (Outputs)

These active low signals strobe the Column-address into memory. The four strobes provide byte wide access into memory. -CAS0 corresponds to byte address 0 and -CAS3 corresponds to byte address 3. These signals are

enabled based on the Cas Select[2:0] inputs for host accesses. On transfer cycles and refresh cycles all Column-address Strobe signals are active.

-WE - Write Enable (Output)

The active low Write Enable signal is used to control the write functions to RAM. During a normal write cycle Write Enable is asserted before -CAS[3:0] (early write). During a write-per-bit cycle Write Enable is asserted before -RAS[3:0].

-DT/-OE - Data Transfer / Output Enable (Output)

This active low signal is used to control output enable on the RAMs during a read cycle and the transfer function during a transfer cycle.

REF - Ram Extra Function (Output)

This pin is used to control split SAM transfer cycles on 1 MBit VRAMs (or any RAM that supports this function).

System Interface

SYSCLK - System Clock (Input)

This is the main RGS14188 clock. The period of SYSCLK dictates all the Host Interface and RAM cycle timing. The maximum frequency of System Clock is 50 MHz. It is not required to synchronize any signals to SYSCLK because resynchronization of necessary signals is performed internally.

-RESET - Reset (Input)

Reset is active low and is used to bring the RGS14188 to a known state. Reset can be asynchronous to SYSCLK because it is synchronized internally. Immediately following the inactive transition of reset the RGS14188 will perform CAS before RAS refresh cycles. When eight cycles are complete bit-7 in the Status register will be set and refresh cycles will continue to be performed until they are disabled or the refresh counter is reprogrammed. No RAM accesses should be performed until this bit is set.

-EXTINT - External Interrupt (Input)

This active low input is used to force an interrupt to the host processor. When an interrupt occurs the host processor must discover the source of the interrupt by reading the Status register, if more then one figure a priority, and service it (them). This input is falling edge triggered and can be enabled/disabled in Control Register 4.

-INT - Interrupt (Output, Open Drain)

Interrupt is used to signal a host processor that some event has occurred. This event can be internally generated or generated by an external source (External Interrupt). This output can be enabled/disabled in Control Register 4.

Host Interface

A[23:0] - Address[23:0] (Inputs)

These inputs are used to drive the RA/CA[9:0] outputs during VRAM access cycles. The least significant six bits are used to address internal registers during register access cycles. The falling edge of Input Latch Enable latches these inputs. If the input latches are not used the RA/CA[9..0] follow these inputs on host access cycles.

ASHIFT[1:0] - Address Shift[1:0] (Inputs)

During host accesses the combination of these inputs selects a 0, 1, 2, or 4-bit msb to lsb address shift of the address input on A[23:0]. The falling edge of Input Latch Enable latches these inputs. The decoding is shown in Table 2-1.

ASHIFT1	ASHIFT0	Function
0	0	No shift
0	1	Shift 1-bit to the left
1	0	Shift 2-bits to the left
1	1	Shift 4-bits to the left

Table 2-1 Address Shift Decoding

CS[2:0] - Cas Select[2:0] (Inputs)

These inputs select the active -CAS[3:0] output during a memory access cycle. The decoding is shown in Table 2-2. The falling edge of Input Latch Enable latches these inputs.

CS2	CS2	CS2	Function
0	0	0	All four -CAS signals are asserted
0	0	1	Two -CAS signals, -CAS1 and -CAS0, are asserted
0	1	0	All four -CAS signals are asserted
0	1	1	Two -CAS signals, -CAS3 and -CAS2, are asserted
1	0	0	One -CAS signal, -CAS0 is asserted
1	0	1	One -CAS signal, -CAS1 is asserted
1	1	0	One -CAS signal, -CAS2 is asserted
1	1	1	One -CAS signal, -CAS3 is asserted

Table 2-2 Cas Select Decoding

-CSTB[3:0] - Cas Strobe[3:0] (Inputs)

These inputs are used during page mode accesses to control -CAS[3:0]. When these inputs are enabled by the internal page mode controller, they connect directly with minimum delay to there respective CAS output. This allows the tightest possible page mode interface timing, and easy synchronization with external busses, leaving it up to an external controller. Some examples of decoding are shown in Table 2-3.

-CSTB3	-CSTB2	-CSTB1	-CSTB0	Function
0	0	0	0	-CAS0, -CAS1, -CAS2, -CAS3 active
1	1	1	0	-CAS0 active
1	1	0	1	-CAS1 active
1	0	1	1	-CAS2 active
0	1	1	1	-CAS3 active
0	0	1	1	-CAS2, -CAS3 active
1	1	0	0	-CAS0, -CAS1 active
1	1	1	1	No -CAS active

Table 2-3 Cas Strobe Function

-PMHOLD - Page Mode Hold (Output)

This signal, when asserted, requests an external controller to suspend its page mode accesses by removing -HCS and then reasserting -HCS. This output can be enabled/disabled in Control Register 2. It is not necessary to pay attention to this output in all system designs. This function becomes vital when the time to execute a page mode cycle approaches the duration of horizontal blank or interferes with midline transfer cycle execution.

DB[7:0] - Data Bus (Input/Output)

The 8-bit Data Bus is used to communicate data to and from the RGS14188's internal registers.

+DBDWR - Data Buffer Direction for Writes (Output)

This active high signal is used to control the direction of external data buffers intended to drive the RAM data bus. When this signal is asserted the data buffers should be driving the data inputs on the RAM (a host write cycle).

-DBOE - Data Buffer Output Enable (Output)

This signal is used as an output enable for the external data buffers used to drive the RAM data bus. This signal is inactive when the RGS14188 is not using the RAM Interface bus.

-BR[1:0] - Bus Request[1:0] (Outputs)

These outputs tell an external VRAM Interface Bus Master that the RGS14188 needs the VRAM Interface Bus. There are three types of requests with two different priorities. Table 2-4 shows the encoding.

-BR1	-BR0	Function
0	0	Internal and host cycle pending, Priority 1.
0	1	Internal cycle pending. Priority 1.
1	0	Host cycle pending. Priority 2.
1	1	No cycle pending

Table 2-4 Bus Request Encoding

Priority 1 - The RGS14188 must have the bus as soon as possible.
Priority 2 - It is up to the external controller to grant the bus in what it defines as the proper amount of time.

+BG - Bus Grant (Input)

This active high signal tells the RGS14188 that an external VRAM Interface bus master is relinquishing the bus. This signal can be asynchronous to SYSCLK.

-BGACK - Bus Grant Acknowledge (Output)

This active low signal tells all other VRAM Interface Bus Masters that the RGS14188 is using the Bus. When the RGS14188 has completed its transaction it will bring Bus Grant Acknowledge High indicating it is no longer using the bus (All drivers are tristated). The RGS14188 will perform one cycle per -BGACK and rearbitrate for other pending cycles (Fair Arbitration).

CT[1:0] - Cycle Type[1:0] (Inputs)

These two inputs are used to tell the RGS14188 what type of read or write cycle is to be performed. The falling edge of Input Latch Enable latches these inputs. The decode is shown in Table 2-5.

CT1	CT0	Function
0	0	Internal register access
0	1	Direct RAM access
1	0	Page mode RAM access
1	1	Direct Write-per-bit RAM access

Table 2-5 Cycle Type Decodes

+ILE - Input Latch Enable (Input)

The falling edge of Input Latch Enable latches all the necessary inputs to complete the requested cycle. The signals latched are Address, CAS Selects, RAS Enables, Host Read/Write, Cycle Type, and Address Shift. When +ILE is high the latches are transparent. +ILE can be tied directly to Host Chip Select if so desired.

-HCS - Host Chip Select (Input)

The falling edge of Host Chip initiates a host cycle based on the Cycle Type inputs. When Host Chip Select is deasserted the cycle is terminated.

+HRD/-HWR - Host Read / Host Write (Input)

This signal determines whether a read or a write cycle is being performed.

-RDY/-TACK - Ready / Transfer Acknowledge (Outputs)

During a memory read or write this signal goes low just after the falling edge of Row-address Strobe[3:0] indicating the cycle has been granted by the internal arbiter and is now ready to continue (Ready). If so desired, during memory cycles only, this signal can be delayed up to seven SYSCLK cycles for easy synchronization with the external system. The delay value is specified in Control register 4. During a register write this signal goes low when the data is written and on reads this signal goes low when the data is valid on the data bus (Transfer Acknowledge).

-RE[3:0] - RAS Enable[3:0] (Inputs)

When asserted -RE3 enables –RAS3, -RE2 enables -RAS2, -RE1 enables –RAS1 and -RE0 enables -RAS0 to go low if a host RAM cycle is being performed. This enables VRAM to be partitioned into banks. The falling edge of +ILE latches these inputs.

GIO[15:0] - General Input/Output[15:0] (Input/Output)

These sixteen pins are intended to be general purpose inputs or outputs as programmed in the General I/O Configuration register. As an output the bit can be written to and read from the host interface port and the state of the bit appears on the respective GIO pin. As an input the bit follows the state of the respective GIO pin and can be read from the host interface port. All the GIO pins have internal pullups. After reset they are configured as inputs.

3.0 Architecture

The RGS14188 consists of several basic functional Blocks. The Block diagram is shown in Figure 3-1.

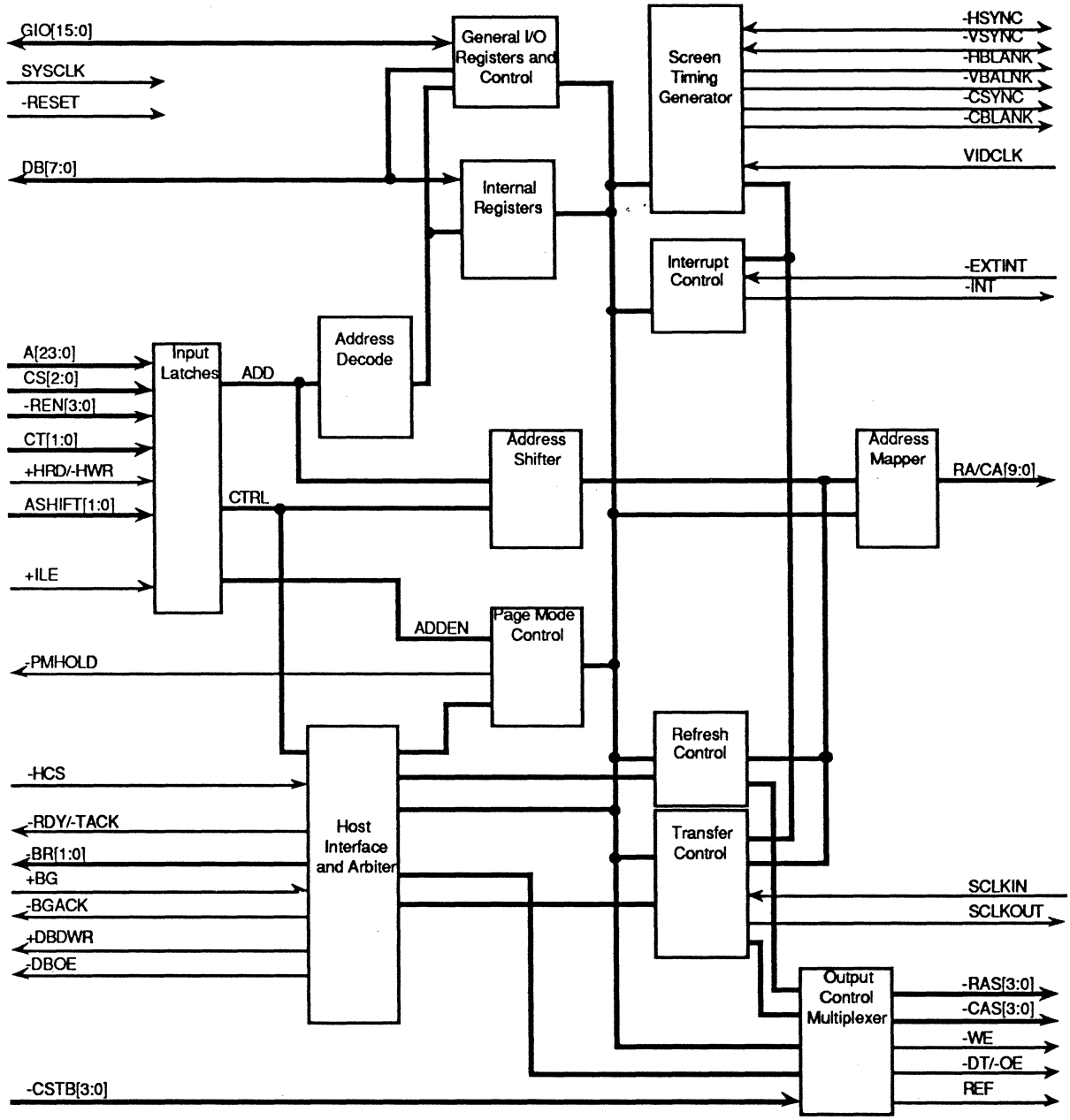


Figure 3-1 RGS14188 Block Diagram

3.1 Input Latches

The input latches are used as holding registers for host interface address input and control signals. These latches are transparent true and are controlled by

Input Latch Enable. This function is very useful with systems that have multiplexed address-data busses. Host Chip Select can be wired directly to Input Latch Enable if the designer so desires. If the address and control are stable throughout the all host cycles these latches do not have to be used.

3.2 Host Interface and Arbiter

The Host Interface is the heart of the RGS14188. It controls all arbitration, internal and external. It handles all cycle decoding and execution. The host interface also controls all register loading and reading. The registers are loaded and read independent of all arbitration. Therefore, care must be taken when loading and changing registers values. For example, the Screen Timing Generator should be disabled before the sync timing values are changed and the refresh function should be disabled before changing the refresh interval.

3.3 Address Decode

The RGS14188 needs a minimum of 48 bytes of address space so all internal registers can be accessed. The six least significant bits of the address input are used to select different internal registers. All other input address are don't cares when addressing the internal registers. Valid register address range is '00' hex to '2F' hex.

3.4 Address Shifter

Based on the Address Shift inputs the Address shifter performs a 0, 1, 2, or 4-bit address shift. This is helpful in systems which incorporate several banks of memory that can be switched in depending on pixel depth. The Address Shift only effects RAM access.

3.5 Page Mode Control

During page mode access this block is used to control how many of the least significant address bits are passed through the RGS14188. It is also responsible for enabling the Cas Strobe[3:0] inputs and asserting the Page Mode Hold signal when the RGS14188 wants to interject an internal cycle.

3.6 Internal Registers

The Internal Registers store all the necessary configuration information for the RGS14188 to function in a given system. These registers range from 8-bits to 24-bits and are all programmed in 8-bit increments. There are four control registers, one status registers, one refresh interval register, five transfer control registers, twelve screen timing registers, a few miscellaneous registers and several inaccessible internal registers. The registers that are accessible by the host are completely defined in section 4.

3.7 General I/O Registers and Control

These registers are hooked directly to 16 I/O pins and are configurable on a bit by bit basis as inputs or outputs. For example, every other bit could be an input and the remaining unused bits could be outputs. They are also mapped into the RGS14188 address space so the host can read or write these bits. These registers are designed to eliminate the need for external, readable registers which would contain system information such as bit depth, and switch settings.

3.8 Screen Timing Generator

The RGS14188 generates the Horizontal and Vertical signals used to drive a CRT monitor in a bit-mapped graphics system. These signals are synchronous to the Video Clock Input. The timing for these signals is controlled by the internal screen timing registers which are easily configured to accommodate a variety of display resolutions and CRT monitors in either interlaced on noninterlaced modes. The RGS14188 can also be configured to accept horizontal and vertical sync signals as inputs allowing synchronization to an external video source.

3.9 Interrupt Control

The RGS14188 is capable of providing two types of interrupts to the host processor. First it can generate an interrupt at any vertical line as programmed in the Vertical Interrupt Line register. Second it provides an input pin for an external interrupt source. Both interrupts can be disabled by writing the proper value to Control register 4.

3.10 Address Mapper

The address mapper is used to map a linear address into a multiplexed row column address based on the type of RAM being used. This mapping takes place after the address is shifted.

3.11 Refresh Control

The RGS14188 allows refresh interval to be programmed to a value that suits the system designers needs. When the refresh count is reached a refresh cycle is scheduled by the internal arbiter and when the cycle is granted a CAS before RAS refresh cycle is executed. After power up and reset CAS before RAS cycles are automatically generated to initialize the RAM array until the refresh count is reprogrammed or refresh cycles are disabled.

3.12 Transfer Control

The RGS14188 provides a robust mechanism for controlling screen update address generations and automatic transfer cycle execution. It allows standard

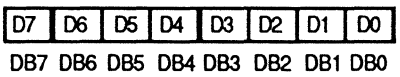
internally scheduled memory to shift register transfer cycles and is also capable of performing midline transfer cycles. One advantage of using midline transfer cycles is the screen size is independent of the VRAM shifter size.

3.12 Output Control Multiplexer

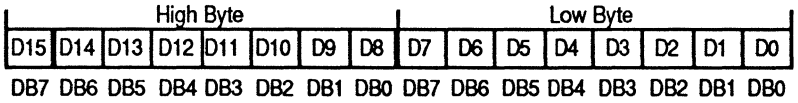
This block is responsible for mixing all the RAM control signals at the proper time to provide a variety of RAM controlling functions. It also passes the Cas Strobe[3:0] signals to the proper CAS lines during page mode cycles.

4.0 Programmable Registers

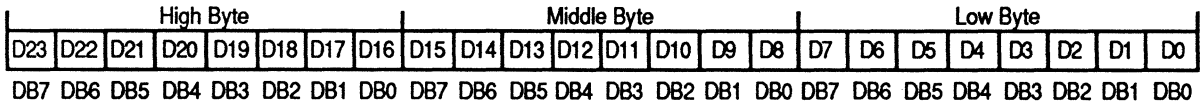
The RGS14188 contains 31 programmable register of either 8, 16, or 24-bits in width. Each register greater then 8-bits must be written or read a byte at a time. The bit numbering convention is shown in Figure 4-1.



8-bit Register



16-bit Register



24-bit Register

Figure 4-1 Bit Numbering Convention for Internal Registers

A host processor accesses the programmable registers within the RGS14188 by means of special read and write cycles. A register access cycle is selected by setting the Cycle Type bits (CT[1:0]) to a '00' binary. The least significant 6-bits of the Address input (A[5:0]) select the register to be read or written. All bits in all registers are both readable and writeable with the exception of the Status register. Bits in a register that have no definition simply don't do anything, however you can still read and write that specific bit. The system may use these unused bits for anything it wants. Table 4-1 gives the address decodes for all the registers.

Input Address							Register
Binary						Hex	
A5	A4	A3	A2	A1	A0	A[5:0]	
0	0	0	0	0	0	00	Control 1
0	0	0	0	0	1	01	Control 2
0	0	0	0	1	0	02	Control 3
0	0	0	0	1	1	03	Control 4
0	0	0	1	0	0	04	Status
0	0	0	1	0	1	05	Refresh Interval
0	0	0	1	1	0	06	General I/O Configuration - High Byte
0	0	0	1	1	1	07	General I/O Configuration - Low Byte
0	0	1	0	0	0	08	Unused
0	0	1	0	0	1	09	Display Start - High Byte
0	0	1	0	1	0	0A	Display Start - Middle Byte
0	0	1	0	1	1	0B	Display Start - Low Byte
0	0	1	1	0	0	0C	Unused
0	0	1	1	0	1	0D	Half Row Increment - High Byte
0	0	1	1	1	0	0E	Half Row Increment - Middle Byte
0	0	1	1	1	1	0F	Half Row Increment - Low Byte
0	1	0	0	0	0	10	Unused
0	1	0	0	0	1	11	Display Pitch - High Byte
0	1	0	0	1	0	12	Display Pitch - Middle Byte
0	1	0	0	1	1	13	Display Pitch - Low Byte
0	1	0	1	0	0	14	CAS Mask
0	1	0	1	0	1	15	Horizontal Latency
0	1	0	1	1	0	16	Horizontal End Sync - High Byte
0	1	0	1	1	1	17	Horizontal End Sync - Low Byte
0	1	1	0	0	0	18	Horizontal End Blank - High Byte
0	1	1	0	0	1	19	Horizontal End Blank - Low Byte
0	1	1	0	1	0	1A	Horizontal Start Blank - High Byte
0	1	1	0	1	1	1B	Horizontal Start Blank - Low Byte
0	1	1	1	0	0	1C	Horizontal Total - High Byte
0	1	1	1	0	1	1D	Horizontal Total - Low Byte
0	1	1	1	1	0	1E	Horizontal Half Line - High Byte
0	1	1	1	1	1	1F	Horizontal Half Line - Low Byte
1	0	0	0	0	0	20	Horizontal Count Load - High Byte
1	0	0	0	0	1	21	Horizontal Count Load - Low Byte
1	0	0	0	1	0	22	Vertical End Sync
1	0	0	0	1	1	23	Vertical End Blank
1	0	0	1	0	0	24	Vertical Start Blank - High Byte
1	0	0	1	0	1	25	Vertical Start Blank - Low Byte
1	0	0	1	1	0	26	Vertical Total - High Byte
1	0	0	1	1	1	27	Vertical Total - Low Byte
1	0	1	0	0	0	28	Vertical Count Load - High Byte
1	0	1	0	0	1	29	Vertical Count Load - Low Byte
1	0	1	0	1	0	2A	Vertical Interrupt Line - High Byte
1	0	1	0	1	1	2B	Vertical Interrupt Line - Low Byte
1	0	1	1	0	0	2C	General I/O - High Byte
1	0	1	1	0	1	2D	General I/O - Low Byte
1	0	1	1	1	0	2E	Y-Zoom
1	0	1	1	1	1	2F	Soft Register

Table 4-1 Register Addresses

0010 1100
1094 0000

4.1 Control 1 - Default Value = '10' hex

D7	D6	D5	D4	D3	D2	D1	D0
		+Transfer Enable	+Refresh Enable	+Invert Field	+Arb. On	RAM Size[1]	RAM Size[0]

Bits D1 - D0 RAM Size[1:0]
These bits specify the size of the RAM being connected to the RGS14188. They tell where the address is to be split for row-column addressing and other important things about the RAM architecture. Table 4-2 shows the encoding.

RAM Size[1]	RAM Size[0]	Function
0	0	64k x n
0	1	256k x n
1	0	1024k x n
1	1	128k x n

Table 4-2 RAM Size Encoding

Bit D2 +Arb. On
Set this bit to a '1' to enable external arbitration of the VRAM Interface. When arbitration is enabled system performance will drop slightly due to extra cycles needed to complete the arbitration handshaking. If there are no other masters of the VRAM interface port set this bit to a '0'. For more information on arbitration see Section 5.5.

Bit D3 +Invert Field
This bit is used to invert the sense of the field bit going to the address generation logic. In interlaced systems this bit is useful if the RGS14188's internal field bit disagrees with an external systems field bit with respect to the first line being displayed.

Bit D4 +Refresh Enable
Set this bit to a '1' to enable the RAM refresh function. The length of time between refresh cycles is set by the Refresh Interval register. Refresh should be disabled when changing the Refresh Interval register.

Bit D5 +Transfer Enable
Set this bit to a '1' to enable the VRAM transfer function (memory to shift register transfer). Transfers should be disabled when changing the Display Start register, Half Row Increment register, Display Pitch register, and the Horizontal Latency register.

4.2 Control 2 - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
+Parm. Test En.	PM Add Enable[2]	PM Add Enable[1]	PM Add Enable[0]	GIO Sel Out[1]	GIO Sel Out[0]	En. PM Hold[1]	En. PM Hold[0]

Bits D1 - D0 En. PM Hold[1:0]
These bits allow the user to enable or disable the Page Mode Hold output based on internal RGS14188 functions. The Page Mode Hold output tells an external page mode controller that the RGS14188 needs to perform an internally scheduled (Priority 1) cycle. For more information on page mode using the RGS14188 refer to section 5.4. Table 4-3 shows the encoding.

En. PM Hold[1]	En. PM Hold[0]	Function
0	0	PMHOLD disabled
0	1	PMHOLD on Transfer Cycles
1	0	PMHOLD on Refresh Cycles
1	1	PMHOLD on Transfer and Refresh Cycles

Table 4-3 Page Mode Hold Function Encoding

Bit D3-D2 GIO Sel[1..0]
These bits select what is output on the GIO[15:0] pins. In normal operation these bits will be set to '00'. If anything but '00' is used the GIO port must be configured properly. The extra selections were added for test purposes. Table 4-4 shows the GIO Sel[1:0] encoding.

GIO Sel Out[1]	GIO Sel Out[0]	GIO Pins
0	0	GIO Register
0	1	Horizontal Count*
1	0	Vertical Count*
1	1	Shift & Zoom Cntr.*

*** It is recommended that the GIO Port be configured as outputs for these modes**

Table 4-4 GIO Port Function Select Encoding

Bits D6-D4 PM Add Enable[2:0]
These bits are used to select the number of low order address bits that will pass through the RGS14188 during page mode cycles. Table 4-5 lists the options. For more information on page mode using the RGS14188 refer to section 5.4.

PM Add Enable[2]	PM Add Enable[1]	PM Add Enable[0]	Function
0	0	0	Enable Flow-through on A(0)
0	0	1	Enable Flow-through on A(1:0)
0	1	0	Enable Flow-through on A(2:0)
0	1	1	Enable Flow-through on A(3:0)
1	0	0	Enable Flow-through on A(4:0)
1	0	1	Enable Flow-through on A(5:0)
1	1	0	Enable Flow-through on A(6:0)
1	1	1	Enable Flow-through on A(7:0)

Figure 4-5 Page Mode Address Enable Encoding

Bits D7 +Parm. Test En.
This bit is used to enable the Input parametric test function. This bit should be set to a '0' for normal operation.

4.3 Control 3 - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
+Ext Sync Enable	+Sync Enable	-Force Blank	+STG Enable	+Interlaced	Xfer RAS Mode	+Mline Enable	+SC Gate Enable

Bit D0 +SC Gate Enable
This bit is used to enable the shift clock gating function which deletes the first shift clock going to the VRAM. This function is useful in systems that use midline transfers. For more information on midline transfers refer to Section 6.5.

Bit D1 +Mline Enable
This bit is used to enable the midline transfer function. If this bit is set to a '0' midline transfers are disabled. For more information on midline transfers refer to Section 6.5.

Bit D2 Xfer RAS Mode
If this bit is set to a '0' all RAS outputs (-RAS[3:0]) will go low during transfer cycles. If set to a one the upper bits of the transfer cycle address determine the active -RAS[3:0] during that transfer cycle. For more information on transfer cycles refer to Section 6.4.

Bit D3 +Interlaced
Setting this bit to a '1' causes the RGS14188 to generate and or accept interlaced screen timing. A '0' specifies non-interlaced mode.

Bit D4 +STG Enable
Setting this bit to a '1' enables the screen timing generator. After all the screen

timing registers are programmed this bit is set to start generating sync and blanking signals. The screen timing generator must be disabled to load new values.

Bit D5 -Force Blank
Setting this bit to a '0' forces the RGS14188 to drive its blanking signals to their active state. This bit must be set to a '1' for normal operation.

Bit D6 +Sync En
When this bit is a '0' the sync outputs of RGS14188 are driven to their inactive state. During normal operation this bit should be set to a '1'.

Bit D7 +Ext Sync En
This bit controls the direction of the -HSYNC and -VSYNC inputs. When set to a '1' (external sync mode) the RGS14188 is put into genlock mode monitoring and responding to external synchronization inputs. When set to a '0' (internal sync mode) the RGS14188 uses the internal screen timing generation logic to provide the monitor timing. After reset the RGS14188 is running in internal sync mode.

4.4 Control 4 - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
	Ready Delay[2]	Ready Delay[1]	Ready Delay[0]		+Enable Int. Output	+Enable Ext. Int.	+Enable Vert. Int.

Bit D0 +Enable Vert. Int.
This bit enables the internal vertical interrupt logic. At a certain line specified in the Vertical Interrupt Line register the RGS14188 will provide a interrupt to the host if the interrupt output is enabled (Bit D2).

Bit D1 +Enable Ext. Int.
This bit enables the external, edge triggered, interrupt logic. At the falling edge of the -EXTINT pin plus internal synchronization delay the RGS14188 will provide a interrupt to the host if the interrupt output is enabled (Bit D2).

Bit D2 +Enable Ext. Int.
This bit enables the interrupt output. If this bit is set to a '0' the interrupt sources still function and their status is available in the Status register but no interrupt will be generated on the -INT pin.

Bit D6-D4 Ready Delay[2:0]
On memory accesses the Ready/Transfer Acknowledge signal is asserted just after the falling edge of -RAS[3:0]. By setting these bits to values greater than 0 the Ready/Transfer Acknowledge signal can be delayed. Table 4-6 shows the encoding.

Ready Delay[2]	Ready Delay[1]	Ready Delay[0]	Amount of Delay
0	0	0	No Delay
0	0	1	One SYSCLK
0	1	0	Two SYSCLKs
0	1	1	Three SYSCLKs
1	0	0	Four SYSCLKs
1	0	1	Five SYSCLKs
1	1	0	Six SYSCLKs
1	1	1	Seven SYSCLKs

Table 4-6 Ready/Transfer Acknowledge Delay Encoding

4.5 Status - Default Value = 'XXXXXX00' binary

The status register has two primary functions. First, the report the status of the current events going on internal to the RGS14188. Second, it provides interrupt set and reset control.

D7	D6	D5	D4	D3	D2	D1	D0
Init. Done	+CBlank	+HBlank	+VBlank	+Set Ext. Interrupt	+Set Vert. Interrupt	+External Interrupt*	+Vertical Interrupt*

Bit D0 +Vertical Interrupt
When read this bit provides the status of the vertical interrupt. A '1' indicates the interrupt is active. If a '0' is written to this bit it will reset the interrupt if it was previously set. Writing a '1' to this bit has no effect.

Bit D1 +External Interrupt
When read this bit provides the status of the External interrupt. A '1' indicates the interrupt is active. If a '0' is written to this bit it will reset the interrupt if it was previously set. Writing a '1' to this bit has no effect.

Bit D2 +Set Vert. Int.
If a '1' is written to this bit it will cause a "Vertical Interrupt" to occur. This should only be done when Vertical Interrupts are disabled. Writing a '1' to this bit creates a pulse internally to set the interrupt register. A '0' must then be written to reset the pulse creation logic before the interrupt can be set again in this fashion.

Bit D3 +Set Ext. Int.
If a '1' is written to this bit it will cause a "External Interrupt" to occur. This should only be done when External Interrupts are disabled. Writing a '1' to this bit creates a pulse internally to set the interrupt register. A '0' must then be written to reset the pulse creation logic before the interrupt can be set again in this fashion.

Bit D4 +VBlank
This bit when '1' tells the host that the RGS14188 is asserting Vertical Blank. When '0' Vertical Blank is not asserted.

Bit D5 +HBlank
This bit when '1' tells the host that the RGS14188 is asserting Horizontal Blank. When '0' Horizontal Blank is not asserted.

Bit D6 +CBlank
This bit when '1' tells the host that the RGS14188 is asserting Composite Blank. When '0' Composite Blank is not asserted.

Bit D7 +Init Done
This bit when '1' tells the host that the RGS14188 has completed it RAM initialization refresh cycles and is ready to proceed. No access should be performed until this bit is set.

4.6 Refresh Interval - Default Value = '01' hex

D7	D6	D5	D4	D3	D2	D1	D0
Rfsh Count[7]	Rfsh Count[6]	Rfsh Count[5]	Rfsh Count[4]	Rfsh Count[3]	Rfsh Count[2]	Rfsh Count[1]	Rfsh Count[0]

Bit D7 - D0 Rfsh Count[7:0]
This register is used to set the amount of time from a refresh cycle completion to the next refresh request to the arbiter (T_{ref}). The actual amount of time between refresh cycles is a function of the value programmed in this register, internal, and external arbitration (if it is enabled) times. Refresh cycles have second priority in the internal arbitration scheme (Transfer Cycles are first priority). The value written to this register should be set slightly lower (to give the proper margin for the specific system) then the maximum interval for the RAMs being used.

$$T_{ref} = (\text{SYSCLK period})(4)(\text{Rfsh Count}) + (\text{SYSCLK period})$$

For example, if the system uses the maximum SYSCLK frequency (50 Mhz) and a refresh cycle of 15.625 µSec is desired (T_{ref}) the system designer would set this register to 'C3' hex. When using the maximum SYSCLK frequency the maximum refresh period is 20.42 µSec.

4.7 Display Start - Default Value = '000000' hex

D7	D6	D5	D4	D3	D2	D1	D0
DSR[23]	DSR[22]	DSR[21]	DSR[20]	DSR[19]	DSR[18]	DSR[17]	DSR[16]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
DSR[15]	DSR[14]	DSR[13]	DSR[12]	DSR[11]	DSR[10]	DSR[9]	DSR[8]

Middle Byte

D7	D6	D5	D4	D3	D2	D1	D0
DSR[7]	DSR[6]	DSR[5]	DSR[4]	DSR[3]	DSR[2]	DSR[1]	DSR[0]

Low Byte

Bit D23 - D0 Display Start[23:0] Horiz + Vert PAN

This 24-bit register contains the address of the pixel to be displayed at the upper most left corner of the screen. This register should only be written when Transfer Cycles are disabled.

4.8 Half Row Increment - Default Value = '000000' hex

D7	D6	D5	D4	D3	D2	D1	D0
HRI[23]	HRI[22]	HRI[21]	HRI[20]	HRI[19]	HRI[18]	HRI[17]	HRI[16]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
HRI[15]	HRI[14]	HRI[13]	HRI[12]	HRI[11]	HRI[10]	HRI[9]	HRI[8]

Middle Byte

D7	D6	D5	D4	D3	D2	D1	D0
HRI[7]	HRI[6]	HRI[5]	HRI[4]	HRI[3]	HRI[2]	HRI[1]	HRI[0]

Low Byte

Bit D23 - D0 Half Row Increment[23:0]
This register contains a '1' in the bit position that will increment the "half row address" for the type of VRAM chosen. The "half row address" is the MSB of the CAS address and is used only if midline transfer cycles are enabled. For example, when using 256K x n VRAMs and midline transfers, the Half Row Increment would be set to '000100' hex because the MSB of the CAS address is the ninth bit.

4.9 Display Pitch - Default Value = '000000' hex

D7	D6	D5	D4	D3	D2	D1	D0
DP[23]	DP[22]	DP[21]	DP[20]	DP[19]	DP[18]	DP[17]	DP[16]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
DP[15]	DP[14]	DP[13]	DP[12]	DP[11]	DP[10]	DP[9]	DP[8]

Middle Byte

D7	D6	D5	D4	D3	D2	D1	D0
DP[7]	DP[6]	DP[5]	DP[4]	DP[3]	DP[2]	DP[1]	DP[0]

Low Byte

Bit D23 - D0 Display Pitch[23:0]
This register contains the difference in addresses between two vertically adjacent pixels. In other words the first two pixels of two consecutive scan lines. For systems not using midline transfer cycles the display pitch is also the width of the display memory because each row of VRAM must contain all the information for a whole scan line. It is also possible to have a system where the screen is refreshed from the bottom. In this case load the 2's complement of the display pitch so that the screen refresh address is decremented between each

horizontal blanking interval.

4.10 CAS Mask - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
CM[7]	CM[6]	CM[5]	CM[4]	CM[3]	CM[2]	CM[1]	CM[0]

Bit D23 - D0 Display Pitch[23:0]
The value in this register specifies the LSBs of the CAS address to be masked during midline transfer cycles. A '1' indicates a masked condition. The value in this register also specifies which bit of the current CAS address will be used to schedule midline transfer cycles. Bit CM[0] corresponds to RA/CA[1], bit CM[1] corresponds to RA/CA[2] etc. For example, when using 256K x n VRAMs and midline transfer cycles this value would be programmed to '7F' hex. For more information on midline transfer cycles refer to section 6.4.

4.11 Horizontal Latency - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
HLat[7]	HLat[6]	HLat[5]	HLat[4]	HLat[3]	HLat[2]	HLat[1]	HLat[0]

Bit D7 - D0 Horizontal Latency[7:0]
Using this register the system designer can specify how long after horizontal blank that a transfer cycle is requested from the internal arbiter (T_{hlat}). This allows the transfer cycle that the VRAM sees to be moved throughout the horizontal blanking period.

$$T_{hlat} = (\text{SYSCLK period})(\text{Horizontal Latency}) + (\text{SYSCLK period})$$

4.12 Horizontal End Sync - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
HES[15]	HES[14]	HES[13]	HES[12]	HES[11]	HES[10]	HES[9]	HES[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
HES[7]	HES[6]	HES[5]	HES[4]	HES[3]	HES[2]	HES[1]	HES[0]

Low Byte

Bit D15 - D0 Horizontal End Sync[15:0]
The contents of this register is compared to the horizontal counter to identify the end of the horizontal sync interval. If the comparison shows they are equal the RGS14188 drives the -HSYNC pin inactive high (if not in external sync mode) and the -CSYNC pin inactive high (assuming we are not in vertical synchronization). The minimum Horizontal End Sync value is one, and the maximum is one less than the value in the Horizontal End Blank register. The value of the Horizontal End Sync register should be set to one less then the number of VIDCLK periods corresponding to the duration of the horizontal sync pulse.

4.13 Horizontal End Blank - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
HEB[15]	HEB[14]	HEB[13]	HEB[12]	HEB[11]	HEB[10]	HEB[9]	HEB[8]]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
HEB[7]	HEB[6]	HEB[5]	HEB[4]	HEB[3]	HEB[2]	HEB[1]	HEB[0]

Low Byte

Bit D15 - D0 Horizontal End Blank[15:0]
The contents of this register is compared to the horizontal counter to identify the end of the horizontal blank interval. If the comparison shows they are equal the RGS14188 drives the -HBLANK pin inactive high and the -CBLANK pin inactive high (assuming we are not in vertical blanking). The minimum Horizontal End Blank value is one greater then the value programmed in the Horizontal End Sync register, and the maximum is one less than the value in the Horizontal Start Blank register. The value of the Horizontal End Blank register should be set to one less then the number of VIDCLK periods corresponding to the duration of the horizontal sync pulse plus the duration of the horizontal back porch.

4.14 Horizontal Start Blank - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
HSB[15]	HSB[14]	HSB[13]	HSB[12]	HSB[11]	HSB[10]	HSB[9]	HSB[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
HSB[7]	HSB[6]	HSB[5]	HSB[4]	HSB[3]	HSB[2]	HSB[1]	HSB[0]

Low Byte

Bit D15 - D0 Horizontal Start Blank[15:0]
The contents of this register is compared to the horizontal counter to identify the start of the horizontal blank interval. If the comparison shows they are equal the RGS14188 drives the -HBLANK pin active low and the -CBLANK pin active low. The minimum Horizontal Start Blank value is one greater then the value programmed in the Horizontal End Blank register, and the maximum is one less than the value in the Horizontal Total register. The value of the Horizontal End Blank register should be set to one less then the number of VIDCLK periods corresponding to the duration of the horizontal sync pulse plus the duration of the horizontal back porch plus the horizontal visible time.

4.15 Horizontal Total - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
HT[15]	HT[14]	HT[13]	HT[12]	HT[11]	HT[10]	HT[9]	HT[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
HT[7]	HT[6]	HT[5]	HT[4]	HT[3]	HT[2]	HT[1]	HT[0]

Low Byte

Bit D15 - D0 Horizontal Total[15:0]
The contents of this register is compared to the horizontal counter to identify the start of the horizontal sync interval. If the comparison shows they are equal the RGS14188 drives the -HSYNC pin active low and the -CSYNC pin active low. The minimum Horizontal Total value is one greater then the value programmed in the Horizontal Start Blank register, and the maximum is 'FFFF' hex. The value of the Horizontal End Blank register should be set to one less then the number of VIDCLK periods corresponding to the duration of the horizontal scan line. For proper interlaced-mode operation, this register should be set to an even number (i.e., LSB = 0).

4.16 Horizontal Half Line - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
HHL[15]	HHL[14]	HHL[13]	HHL[12]	HHL[11]	HHL[10]	HHL[9]	HHL[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
HHL[7]	HHL[6]	HHL[5]	HHL[4]	HHL[3]	HHL[2]	HHL[1]	HHL[0]

Low Byte

Bit D15 - D0 Horizontal Half Line[15:0]
In interlaced mode the contents of this register is compared to the horizontal counter to identify the half line duration. If the comparison shows they are equal and the internal field bit is high (odd field) the RGS14188 drives the -HSYNC pin active low and the -CSYNC pin active low a half line (value programmed in this register) early. This is necessary to differentiate the fields and effect the interlace. The minimum Horizontal Half Line value is '2' hex., and the maximum is two less then the Horizontal Total Value. The value of the Horizontal Half Line register should be set to one less then the number of VIDCLK periods corresponding to one half the duration of a horizontal scan line.

4.17 Horizontal Count - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
HC[15]	HC[14]	HC[13]	HC[12]	HC[11]	HC[10]	HC[9]	HC[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
HC[7]	HC[6]	HC[5]	HC[4]	HC[3]	HC[2]	HC[1]	HC[0]

Low Byte

Bit D15 - D0 Horizontal Count[15:0]
This register is used to load the horizontal counter at the end of each horizontal scan line. It is NOT the horizontal count. This register is used primarily for chip test purposes. This register should be set to '0000' hex (default value) and left alone.

4.18 Vertical End Sync - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
VES[7]	VES[6]	VES[5]	VES[4]	VES[3]	VES[2]	VES[1]	VES[0]

Bit D7 - D0 Vertical End Sync[7:0]
The contents of this register is compared to the vertical counter to identify the end of the vertical sync interval. If the comparison shows they are equal the RGS14188 drives the -VSYNC pin inactive high (if not in external sync mode) and the -CSYNC pin inactive high (assuming we are not in horizontal synchronization). The minimum Vertical End Sync value is one, and the maximum is one less than the value in the Vertical End Blank register. The value of the Vertical End Sync register should be set to one less then the number of scan lines corresponding to the duration of the vertical sync pulse.

4.19 Vertical End Blank - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
VEB[7]	VEB[6]	VEB[5]	VEB[4]	VEB[3]	VEB[2]	VEB[1]	VEB[0]

Bit D7 - D0 Vertical End Blank[7:0]
The contents of this register is compared to the vertical counter to identify the end of the vertical blank interval. If the comparison shows they are equal the RGS14188 drives the -VBLANK pin inactive high and the -CBLANK pin inactive high (assuming we are not in horizontal blanking). The minimum Vertical End Blank value is one greater then the value programmed in the Vertical End Sync register, and the maximum is one less than the value in the Vertical Start Blank

register. The value of the Vertical End Blank register should be set to one less then the number of scan lines corresponding to the duration of the vertical sync pulse plus the duration of the vertical back porch.

4.20 Vertical Start Blank - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
VSB[15]	VSB[14]	VSB[13]	VSB[12]	VSB[11]	VSB[10]	VSB[9]	VSB[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
VSB[7]	VSB[6]	VSB[5]	VSB[4]	VSB[3]	VSB[2]	VSB[1]	VSB[0]

Low Byte

Bit D15 - D0 Vertical Start Blank[15:0]
The contents of this register is compared to the vertical counter to identify the start of the vertical blank interval. If the comparison shows they are equal the RGS14188 drives the -VBLANK pin active low and the -CBLANK pin active low. The minimum Vertical Start Blank value is one greater then the value programmed in the Vertical End Blank register, and the maximum is one less than the value in the Vertical Total register. The value of the Vertical Start Blank register should be set to one less then the number of scan lines corresponding to the duration of the vertical sync pulse plus the duration of the vertical back porch plus the vertical visible duration (all in scan lines).

4.21 Vertical Total - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
VT[15]	VT[14]	VT[13]	VT[12]	VT[11]	VT[10]	VT[9]	VT[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
VT[7]	VT[6]	VT[5]	VT[4]	VT[3]	VT[2]	VT[1]	VT[0]

Low Byte

Bit D15 - D0 Vertical Total[15:0]
The contents of this register is compared to the vertical counter to identify the start of the vertical sync interval. If the comparison shows they are equal the RGS14188 drives the -VSYNC pin active low and the -CSYNC pin active low. The minimum Vertical Total value is one greater then the value programmed in the Vertical Start Blank register, and the maximum is 'FFFF' hex. The value of the Vertical Total register should be set to one less then the number of scan lines corresponding to the duration of the vertical frames. For proper interlaced-mode operation, this register should be set to an even number (i.e., LSB = 0) that is the vertical total for two fields minus one, then divided by two. Each field has the number of lines in the Vertical Total register plus one half line. For example, if 481 lines are desired for interlaced mode the Vertical Total should be set to (481 - 1) ÷ 2 = 240 = '00F0' hex. This will result in a display of 240.5 horizontal lines per field.

4.22 Vertical Count - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
VC[15]	VC[14]	VC[13]	VC[12]	VC[11]	VC[10]	VC[9]	VC[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
VC[7]	VC[6]	VC[5]	VC[4]	VC[3]	VC[2]	VC[1]	VC[0]

Low Byte

Bit D15 - D0 Vertical Count[15:0]
This register is used to load the vertical counter at the end of each vertical frame. It is NOT the vertical count. This register is used primarily for chip test purposes. This register should be set to '0000' hex (default value) and left alone.

4.23 Vertical Interrupt Line - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
VIL[15]	VIL[14]	VIL[13]	VIL[12]	VIL[11]	VIL[10]	VIL[9]	VIL[8]]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
VIL[7]	VIL[6]	VIL[5]	VIL[4]	VIL[3]	VIL[2]	VIL[1]	VIL[0]

Low Byte

Bit D15 - D0 Vertical Interrupt Line[15:0]
The contents of this register is compared to the vertical counter. If the comparison shows they are equal and the vertical interrupt (and interrupt pin) is enabled the RGS14188 drives the -INT pin active low. The minimum Vertical Interrupt Line value is zero, and the maximum is the value in the Vertical Total register.

4.24 General IO Configuration - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
GIOC[15]	GIOC[14]	GIOC[13]	GIOC[12]	GIOC[11]	GIOC[10]	GIOC[9]	GIOC[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
GIOC[7]	GIOC[6]	GIOC[5]	GIOC[4]	GIOC[3]	GIOC[2]	GIOC[1]	GIOC[0]

Low Byte

Bit D15 - D0 General IO Configuration[15:0]
This register is used to configure the General IO port as inputs or outputs on a bit-by-bit basis. If a bit in this register is set to a '1' the corresponding General IO pin is a input. If a bit in this register is set to a '0' the corresponding General IO pin is a output. At power up all bits are configured as inputs and all the General IO pins have pullups.

4.25 General IO - Default Value = '0000' hex

D7	D6	D5	D4	D3	D2	D1	D0
GIO[15]	GIO[14]	GIO[13]	GIO[12]	GIO[11]	GIO[10]	GIO[9]	GIO[8]

High Byte

D7	D6	D5	D4	D3	D2	D1	D0
GIO[7]	GIO[6]	GIO[5]	GIO[4]	GIO[3]	GIO[2]	GIO[1]	GIO[0]

Low Byte

Bit D15 - D0 General IO[15:0]
This register is used to read or write the General IO bits depending on how they are configured in the General IO Configuration register. If a bit is configured as an output, writing the register will deposit the new value and that value will appear on the GIO[x] pin. If a bit is configured as an input, reading the GIO[x] bit in the register double reclocks and latches the value on the pin for the entire read cycle. This prevents the bit from changing mid-cycle.

4.26 Y-Zoom - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
YZ[7]	YZ[6]	YZ[5]	YZ[4]	YZ[3]	YZ[2]	YZ[1]	YZ[0]

Bit D7 - D0 Y-Zoom[7:0]
This register is used to select the y-zoom factor. The RGS14188 is capable of integer zoom from 1 to 256 times. A value of '01' hex corresponds to a y-zoom factor of 1X, a value of 'FF' hex corresponds to a value of 255X, and a value of '00' hex corresponds to a y-zoom of 256X. This register should only be changed during vertical blanking intervals.

4.27 Software Register - Default Value = '00' hex

D7	D6	D5	D4	D3	D2	D1	D0
SR[7]	SR[6]	SR[5]	SR[4]	SR[3]	SR[2]	SR[1]	SR[0]

Bit D7 - D0 Software Register[7:0]
This register can be used by anyone to store anything. Its contents has no effect on the RGS14188.

5.0 Host Interface Operation

The RGS14188 performs several types of access cycles because of its ability to control display update, CRT timing as well as RAM port data control. There are two types of cycles performed by the RGS14188, Host initiated and Internally Generated. Table 5-1 shows all the different types of cycles and who generates them.

Host Initiated Cycles	Internally Generated Cycles
Register Access	RAM Refresh
Direct Memory Access	Standard Read Transfer Cycle (Display Update)
Page Mode Memory Access	Split Read Transfer Cycle (Display Update)
Write-per-bit Memory Access	

Table 5-1 Access Cycles

A cycle is selected by the host via a 2-bit select code input on CT[1:0] (Cycle Type) as shown in Table 5-2. An active-high on the Host Chip Select input (-HCS) disables all host-initiated cycles. Table 5-3 shows the address mapping scheme from A[23:0] to the multiplexed address outputs RA/CA[9:0].

CT1	CT0	Function
0	0	Internal register access
0	1	Direct RAM access
1	0	Page mode RAM access
1	1	Direct Write-per-bit RAM access

Table 5-2 Cycle Type Incoding.

RAM Size[1]	RAM Size[0]	RAM Size	ADDRESS TIME	ASHIFT[1]	ASHIFT[0]	RA/CA[9]	RA/CA[8]	RA/CA[7]	RA/CA[6]	RA/CA[5]	RA/CA[4]	RA/CA[3]	RA/CA[2]	RA/CA[1]	RA/CA[0]
0	0	64K X N	CAS	0	0	A17	A16	A7	A6	A5	A4	A3	A2	A1	A0
0	0		RAS	0	0	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8
0	0		CAS	0	1	A18	A17	A8	A7	A6	A5	A4	A3	A2	A1
0	0		RAS	0	1	H18	A17	A16	A15	A14	A13	A12	A11	A10	A9
0	0		CAS	1	0	A19	A18	A9	A8	A7	A6	A5	A4	A3	A2
0	0		RAS	1	0	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
0	0		CAS	1	1	A21	A20	A11	A10	A9	A8	A7	A6	A5	A4
0	0		RAS	1	1	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
0	1	256K X N	CAS	0	0	A18	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1		RAS	0	0	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9
0	1		CAS	0	1	A19	A9	A8	A7	A6	A5	A4	A3	A2	A1
0	1		RAS	0	1	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
0	1		CAS	1	0	A20	A10	A9	A8	A7	A6	A5	A4	A3	A2
0	1		RAS	1	0	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
0	1		CAS	1	1	A22	A12	A11	A10	A9	A8	A7	A6	A5	A4
0	1		RAS	1	1	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13
1	0	1024K X N	CAS	0	0	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0		RAS	0	0	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
1	0		CAS	0	1	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
1	0		RAS	0	1	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
1	0		CAS	1	0	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2
1	0		RAS	1	0	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
1	0		CAS	1	1	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4
1	0		RAS	1	1	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14
1	1	128K X N	CAS	0	0	A17	0	A7	A6	A5	A4	A3	A2	A1	A0
1	1		RAS	0	0	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8
1	1		CAS	0	1	A18	0	A8	A7	A6	A5	A4	A3	A2	A1
1	1		RAS	0	1	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9
1	1		CAS	1	0	A19	0	A9	A8	A7	A6	A5	A4	A3	A2
1	1		RAS	1	0	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
1	1		CAS	1	1	A21	0	A11	A10	A9	A8	A7	A6	A5	A4
1	1		RAS	1	1	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12

Table 5-3 Address Mapping

5.1 Cycle Scheduling and Arbitration

All of the RGS14188's internally generated cycles are scheduled at periodic intervals determined by control parameters loaded into the internal registers by the host. The following control sequence within the RGS14188 governs the scheduling of these cycles. Section 6 goes into more detail on internally scheduled cycles.

1. At the beginning of the last horizontal blanking period during vertical blanking, and all other horizontal blanking periods (not during vertical blanking), after the horizontal latency is exhausted a transfer request is sent to the arbiter.

2. When the arbiter grants the request a transfer cycle is performed. If midline transfers are enabled another transfer cycle immediately follows without arbitration. This insures the other half of the serial port contains logically consecutive data.

3. When the count in the refresh counter equals the refresh interval a refresh request is sent to the arbiter.

4. When the arbiter grants the refresh request a CAS before RAS refresh cycle is performed.

5. When the Host Chip select input is driven low a host cycle request is sent to the arbiter.

6. When the arbiter grants the host cycle request the host cycle is performed.

When an arbitration conflict arises the following priority scheme is used.

1. First Priority - Any cycle already in progress.

2. Second Priority - A transfer cycle

3. Third Priority - A refresh cycle

4. Fourth Priority - A cycle requested by the host processor.

5.2 Direct RAM Access

A direct RAM access read or write cycle is an access performed by the host to or from a location in the memory system controlled by the RGS14188. The row and column addresses are supplied to the RGS14188 by the host on the A[23:0] inputs which are multiplexed to the RA/CA[9:0] outputs. An additional 4-bits, -REN[3:0], select one of four row address strobes to be activated during the cycle and 3-bits, -CS[2:0], select a combination of column address strobes to be activated during the cycle.

A direct RAM access read or write cycle is initiated under explicit control of the host. The Cycle Type inputs (CT[1:0]) identify the cycle as a Direct RAM Access, and the +HRD/-HWR input determines the direction of the transfer. The timing for a Direct RAM access is shown in Figure 5-1. The host signals the start of the cycle by driving the Host Chip Select input low. At the falling edge of Input Latch Enable, the address and control are stored. Using the input latch is optional however, if not used all host interface signals must remain stable throughout the whole cycle. The timing shown in Figure 5-1 assumes no delay due to external or internal arbitration. Just after the falling edge of -RAS[3:0] Ready/Transfer Acknowledge is driven low indicating the cycle is continuing (Ready). Ready/Transfer Acknowledged is delayed if the host cycle must be delayed due to arbitration.

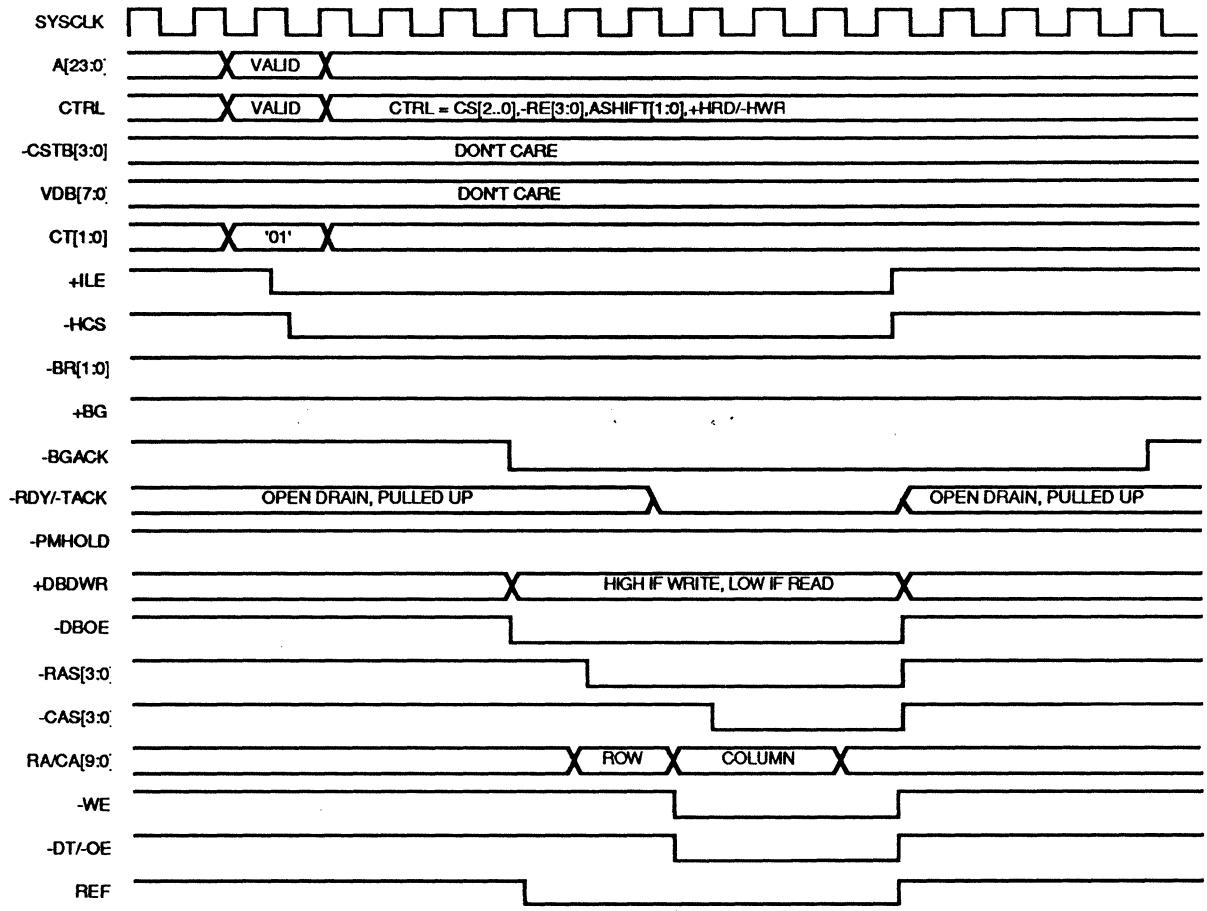


Figure 5-1 Direct RAM Access Cycle

5.2 Write-per-bit RAM Access

A write-per-bit RAM access write cycle is an access performed by the host to a location in the memory system controlled by the RGS14188. The row and column addresses are supplied to the RGS14188 by the host on the A[23:0] inputs which are multiplexed to the RA/CA[9:0] outputs. An additional 4-bits, -REN[3:0], select one of four row address strobes to be activated during the cycle and 3-bits, -CS[2:0], select a combination of column address strobes to be activated during the cycle.

A Write-per-bit RAM access write cycle is initiated under explicit control of the host. The Cycle Type inputs (CT[1:0]) identify the cycle as a Write-per-bit RAM Access, and the +HRD/-HWR input must be low. The timing for a Write-per-bit RAM access is shown in Figure 5-2. The host signals the start of the cycle by driving the Host Chip Select input low. At the falling edge of Input Latch Enable, the address and control are stored. Using the input latch is optional however, if not used all host interface signals must remain stable throughout the whole cycle. The timing shown in Figure 5-2 assumes no delay due to external or internal arbitration. Just after the falling edge of -RAS[3:0] Ready/Transfer Acknowledge is driven low indicating the cycle is continuing (Ready). Ready/Transfer Acknowledged is delayed if the host cycle must be delayed

due to arbitration.

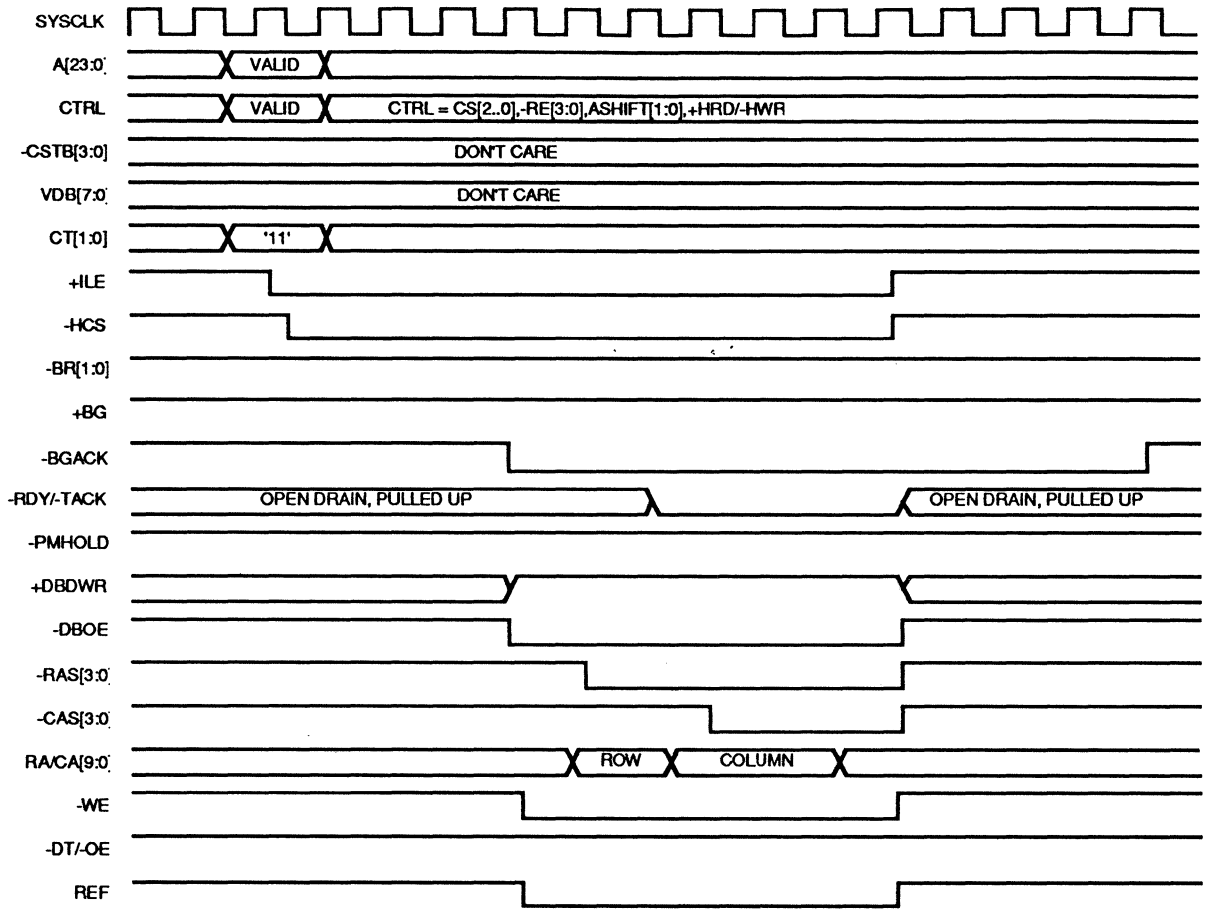


Figure 5-2 Write-per-bit RAM Access Cycle

5.3 Internal Register Access

31 register locations of various widths (8, 16, and 24-bit) are accessible to the host. The RGS14188's internal data bus (bidirectional pins DB[7:0]) is 8-bits wide, and each register must be accessed by the the host as one, two or three separate bytes. A register access read or write cycle is initiated by driving the Host Chip Select input low and asserting the proper Cycle Type inputs (CT[1:0]). The Host Read/Host Write input determines the direction of the transfer and the low six address bits (A[5:0]) determine the register to be accessed.

Because some of the registers are bigger then 8-bits, 2 or 3 separate accesses may be necessary to write or read the entire register. However, it is only necessary to access the byte(s) that need to be read or written. The timing for a register write is shown in Figure 5-3 and the timing for a register read is shown in Figure 5-4. The host signals the start of the cycle by driving the Host Chip Select input low. At the falling edge of Input Latch Enable, the address and +HRD/-HWR signal are stored. Using the input latch is optional however, if not used all host interface signals must remain stable

throughout the whole cycle. All register accesses are independent of all other RGS14188 functions so register cycles will never be delayed. Because of this feature care should be taken when changing register values. Functions such as refresh should be disabled before writing registers that control refresh. When the data is written on writes, or valid on reads Ready/Transfer Acknowledge is driven low indicating the transfer is complete (Transfer Acknowledge).

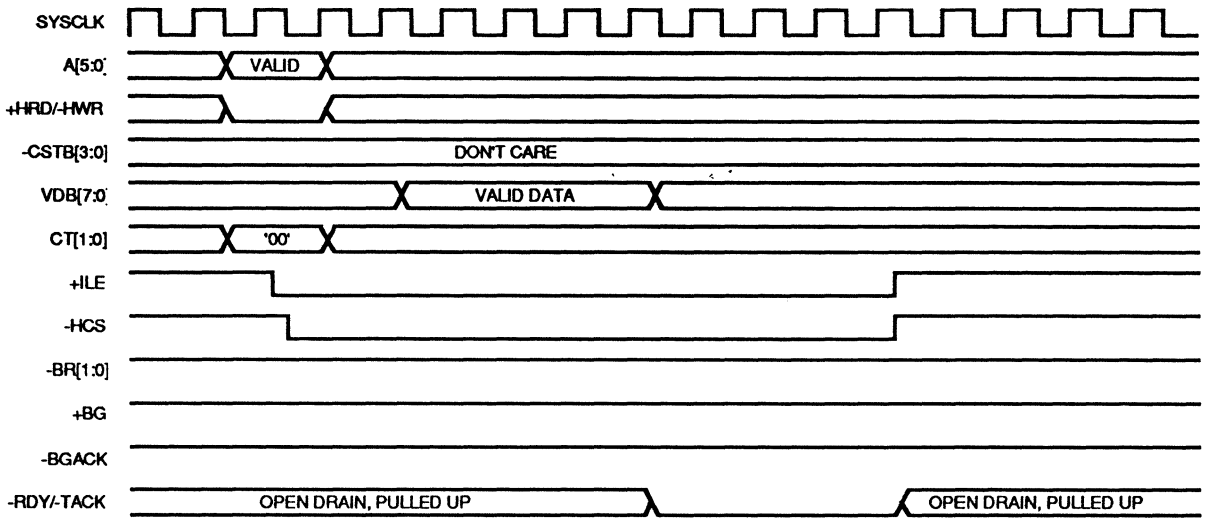


Figure 5-3 Register Write Access

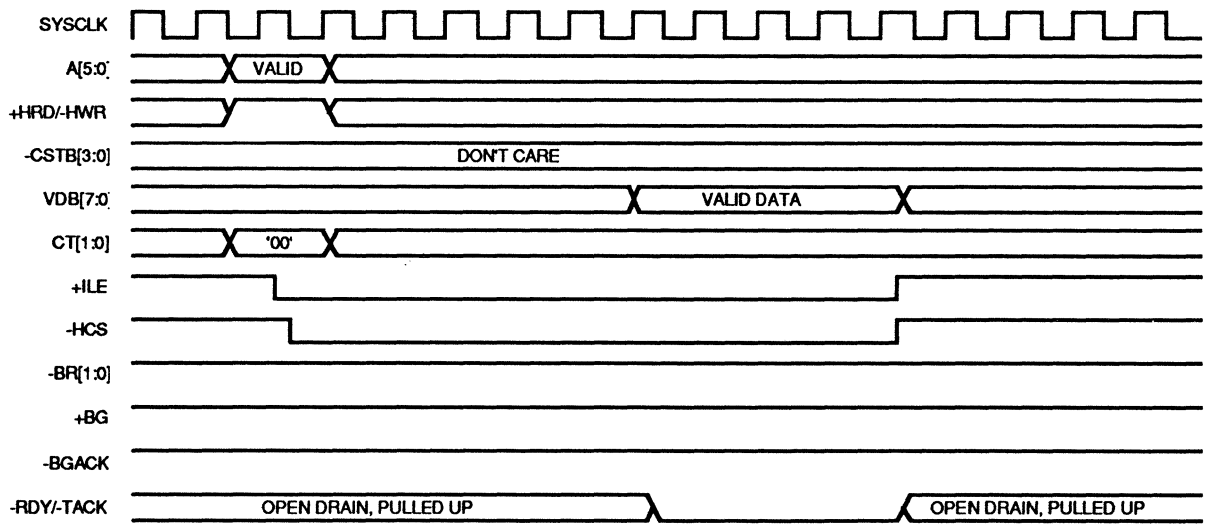


Figure 5-4 Register Read Access

5.4 Page Mode RAM Access

A Page Mode RAM access read or write cycle is an access performed by the host to or from several location in the memory system controlled by the RGS14188. The row and column addresses are supplied to the RGS14188 by the host on the A[23:0] inputs

which are multiplexed to the RA/CA[9:0] outputs for the beginning of the cycle. An additional 4-bits, -REN[3:0], select one of four row address strobes to be activated during the cycle.

A Page Mode RAM access read or write cycle is initiated under explicit control of the host. The Cycle Type inputs (CT[1:0]) identify the cycle as a Page Mode RAM Access, and the +HRD/-HWR input determines the direction of the transfer. The timing for a Page Mode RAM access is shown in Figure 5-5. The host signals the start of the cycle by driving the Host Chip Select input low. At the falling edge of Input Latch Enable, the address and control are stored. Using the input latch is optional however, if not used all host interface signals must remain stable throughout the whole cycle. The timing shown in Figure 5-5 assumes no delay due to external or internal arbitration. Just after the falling edge of RAS when CAS is ready to be asserted Ready/Transfer Acknowledge is driven low indicating the cycle is ready to continue (Ready). The external controller can now drive the Cas Strobe inputs and increment the address. It has full control until Host Chip Select is deasserted. In this way Page Mode Cycles are different from the other RAM cycles. The designer is responsible for providing CAS and the lower address bits he wishes to change during the cycle. Bits D6-D4 (PM Add. Enable[2:0]) of Control register 2 select the number of lower address bits which will be allowed to pass through the RGS14188. Also, at the falling edge of Ready/Transfer Acknowledge the Cas Strobe inputs are enabled. These inputs connect directly to their respective CAS outputs with minimum delay and are used to control the CAS generation. It is up to the designer to meet the exact RAM address/CAS timing specifications of the RAM used. The RGS14188 supports pass through on the lower 8-bits of A[23:0] which would allow page mode cycles of up to 256 transfers. Since the -CAS[3:0] outputs are individually controlled page mode accesses of bytes, words, and longs are also possible. The Page Mode Hold output which is enabled in Control Register 2 is used to suspend a page mode access so the RGS14188 can interject a necessary cycle. Figure 5-6 shows an example of a Page Mode cycle with Page Mode Hold active. When -PMHOLD is asserted the external controller suspends its access at a convenient time and releases Host Chip Select for at least one SYSCLK cycle. It then reasserts Host Chip Select and waits for the Ready/Transfer Acknowledge signal to go low. At this time it continues its page mode access from where it left off. Ready/Transfer Acknowledged is delayed if the host cycle must be delayed due to arbitration. It is not necessary to honor the Page Mode Hold request. However, if the length of the systems page mode cycles can interfere with the completion of transfer cycles during the horizontal blank time it will cause undesirable results on the display.

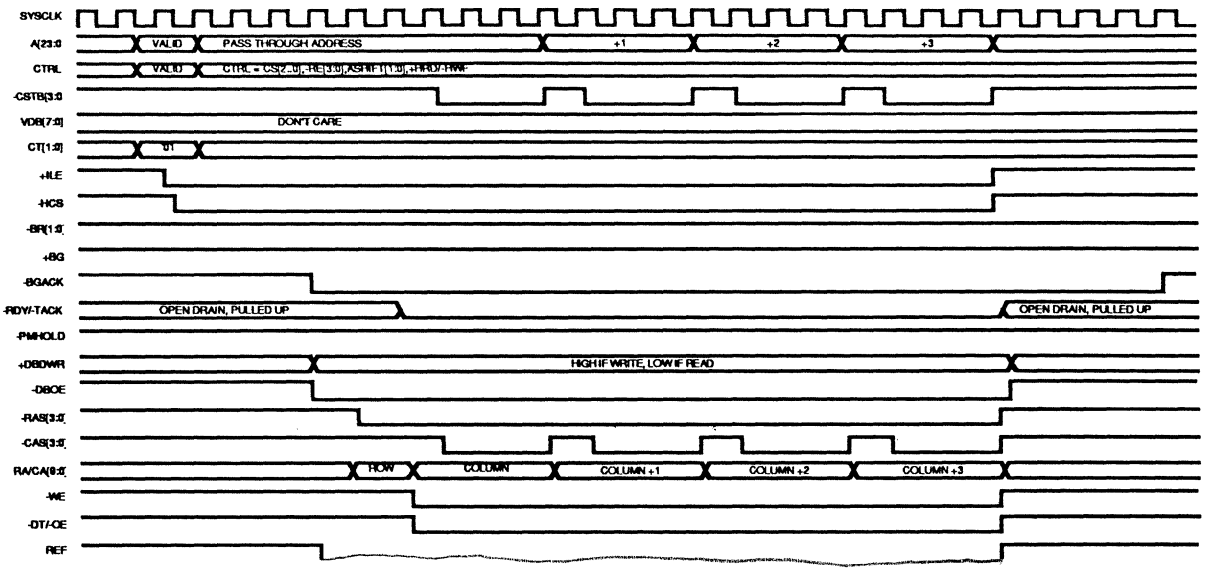


Figure 5-5 Page Mode Access

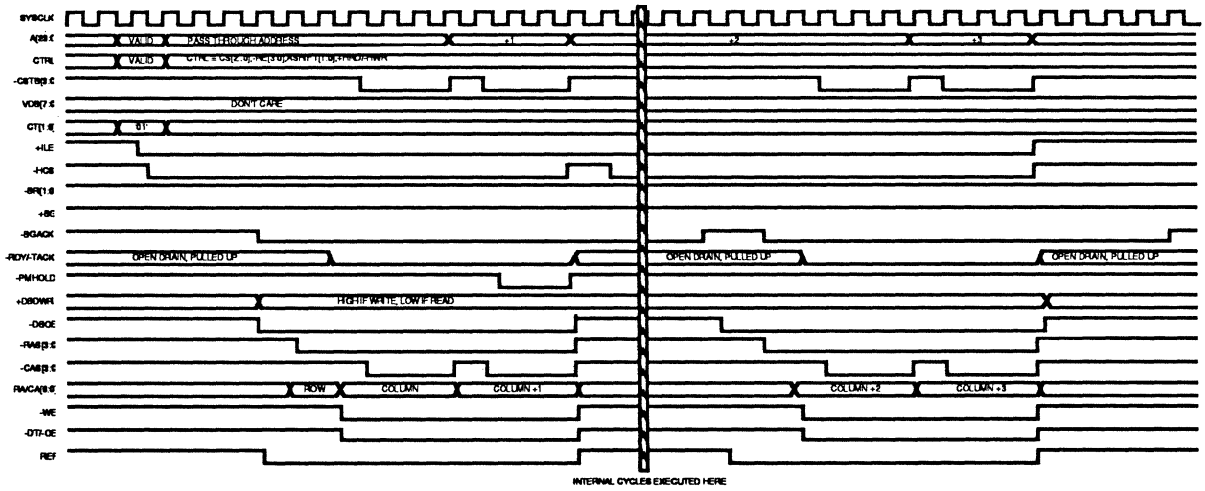


Figure 5-6 Page Mode Access with Page Mode Hold

5.5 VRAM Interface Bus Arbitration

The RGS14188 allows multiple masters of the VRAM Interface Bus. Arbitration is controlled with three external pins in the Host Interface Port, -BR[1:0], +BG, -BGACK. If arbitration is turned on in Control register 1 the RGS14188 will assert its Bus Request outputs to alert external masters that it needs the bus. There are two priority levels of bus requests. Priority 1 requests indicate the RGS14188 needs the bus as soon as possible. Priority 2 requests indicate that a host cycle is pending and it is up to the other bus masters to grant the cycle in the proper amount of time. The encoding is shown in Table 5-3.

-BR1	-BR0	Function
0	0	Internal and host cycle pending. Priority 1.
0	1	Internal cycle pending. Priority 1.
1	0	Host cycle pending. Priority 2.
1	1	No cycle pending

Table 5-3 Bus Request Encoding

After asserting the Bus Request outputs the RGS14188 waits for the Bus Grant input to go high. After resynchronization of the Bus Grant input it asserts Bus Grant Acknowledge indicating it is using the bus. When Bus Grant Acknowledge is released the RGS14188's VRAM Interface Bus drivers are tristated. The Bus Grant Acknowledge signal is always driven even if arbitration is turned off indicating the RGS14188 is using the bus. If more then one cycle is pending the RGS14188 will rearbitrate for each cycle (Fair Arbitration). For example, if a transfer cycle and Host Cycle are pending it will ask for the transfer cycle, when granted release the request, then ask for the host cycle. It is possible for the Bus Request outputs to change during a request. An external bus master must honor the changes and the RGS14188 will execute the pending cycles in order of priority, not on a first come basis. Figure 5-7 through 5-8 show the bus arbitration timing with a two different request scenarios.

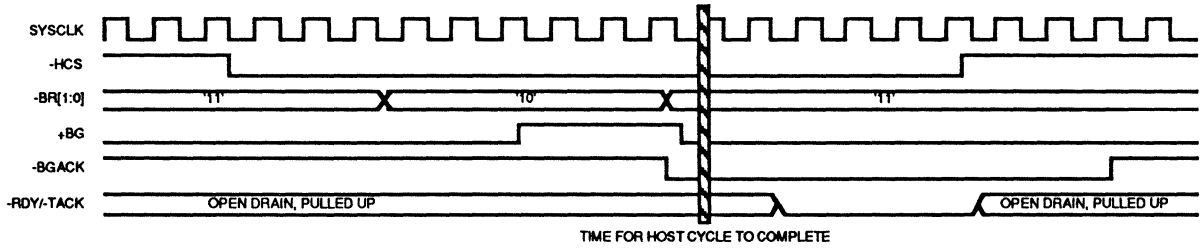


Figure 5-7 Bus Request Cycle

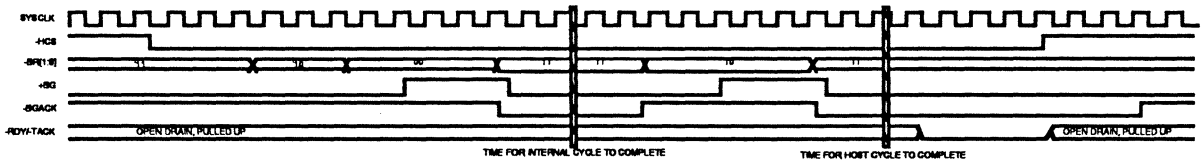


Figure 5-8 Bus Request Cycle

6.0 Video Timing and Screen Refresh

The RGS14188's interface provides the following features:

- Separate and Composite Sync and Blanking Signals
- Synchronization to Internal or External Sources
- Supports Interlaces or Noninterlaced displays

- Supports a Wide Variety of Screen Resolutions.
- Supports Automatic Screen Refresh Address Generation

The video timing interface is clocked by VIDCLK. The maximum frequency of Video Clock (VIDCLK) is 50 MHz. All internal counters related to video timing are clocked on the rising edge of Video Clock.

6.1 Noninterlaced Video

Noninterlaced operation is selected by setting the Interlaced bit in Control register 3 to a '0'. Each non interlaced frame consists of a integer number of horizontal scan lines. The Vertical Counter increments at the start of each horizontal sync interval, and the leading and trailing edges of the vertical sync pulse are coincident with the start of horizontal sync pulses. Both separate and composite blanking signals are available on the RGS14188. The leading and trailing edges of the vertical blanking signals are also coincident with the start of the horizontal sync pulses.

6.2 Interlaced Video

Interlaced operation is selected by setting the Interlaced bit in Control register 3 to a '1'. Horizontal timing register operation in interlaced mode is identical to the operation in noninterlaced mode. In interlaced mode, each display frame is composed of two fields of horizontal scan lines. The display consists of alternate lines from the two fields. This doubles the display resolution while only slightly increasing the frequency at which data is supplied to the screen.

In interlaced mode, two separate vertical scans are performed for each frame - one for the even line numbers (even field) and one for the odd line numbers (odd field). The even field is scanned first, starting at the top left of the screen. The end of the vertical sync pulse that precedes the even field coincides with the start of an horizontal sync pulse; however, the vertical sync pulse that precedes the odd field ends exactly halfway between two horizontal sync pulses.

In interlaced mode, video timing logic is altered so that the odd field begins when the horizontal count equals the value programmed in the Horizontal Half Line retester. The CRT beam is thus positioned so that the horizontal scan lines in the odd field fall between the horizontal scan lines in the even field. Horizontal Total must also be loaded with an odd number for this to happen.

6.3 External Sync Mode

External Sync Mode operation is selected by setting the Ext. Sync Enable bit in Control register 3 to a '1'. External Sync Mode allows the RGS14188 to use the horizontal and vertical sync signals from an external source. In this mode the Horizontal Sync and Vertical Sync pins are configured as inputs. When an active low sync pulse is input to one of these pins, the corresponding counter is forced to reload to the value programmed in its counter register. By forcing the counters to follow the

external sync signals, the blanking intervals and screen refresh cycles are also forced to follow the external video source.

The Horizontal Sync and Vertical Sync inputs are sampled on the rising edge of Video Clock. The horizontal and vertical counters will be reloaded two Video Clock periods following the high to low transition on a sync pin.

When configured for both external sync and interlaced operation, the RGS14188 discriminates between the odd and even fields of an interlaced framed based on the relationship of the falling edge of horizontal sync and the falling edge of vertical sync.

6.4 Screen Refresh Control

The RGS14188 automatically schedules VRAM-to-serial register transfer cycles, called transfer cycles (or screen refresh cycles, or screen update cycles, or display update cycles), needed to refresh a video screen. A transfer cycle typically affects all VRAMs in a system. During a transfer cycle, a selected row o the display memory is transferred to the internal serial register of each VRAM. The data is then shifted out to refresh the display. The RGS14188 supports transfer cycles that occur during horizontal blanking and that occur during the active display time (called midline transfer cycles). The address output during both types of transfer cycles is created by the transfer address generation logic.

The video timing logic schedules a transfer cycle at the beginning of each horizontal blanking interval. During blanking, the VRAM serial registers should not be shifting data. During the vertical blanking interval no transfer cycles take place until the horizontal blanking interval at the beginning of the first displayed line of the new frame.

The RGS14188 contains dedicated circuitry that operates synchronous to the VRAM's shift clock. This enables the RGS14188 to perform screen refresh cycles during the active display time in systems with VRAMs that have split serial registers. These occur without interrupting the flow of data to the screen. If enabled, midline transfer cycles occur as well as (not instead of) horizontal blanking transfer cycles. The Shift Count register (not accessible to the host) is loaded automatically during the horizontal blanking screen refresh with the column address portion of the logical address output to the VRAMs. When blanking ends, and shift clock starts again, Shift Count is incremented each time the VRAM serial registers shift out a bit of data. In this way, Shift Count always contains the column address of the bit of data currently being shifted out. When Shift Count increments to the next half row address (msb of the CAS address) a midline transfer cycle is scheduled. When midlines are enabled an extra screen refresh is scheduled during horizontal blanking. As during any horizontal blanking period, there is an ordinary memory to shift register transfer cycle the loads the specified row of the VRAM into the serial registers. This transfer loads both halves of the serial register. However, if the tap point is more then half way along the row, then the idle half of each serial register will not contain data from the next row of the VRAM to be displayed. To ensure that the idle half contains the next half row, and not the previous, a midline transfer cycle with the address of the next half row is generated

immediately following the ordinary horizontal blanking screen refresh. This is the same cycle used for midline transfer cycles during active video, and loads only half of each of the VRAM serial registers. Some VRAMs require a shift clock pulse to latch the tap point address into an internal counter. Since two tap point address are supplied during horizontal blanking a single shift clock pulse must be provided between the two transfer cycles. Correct shift clock generation is automatically done if the Shift Clock Out pin is used to drive shift clock to the VRAMs and bit-0 (+En. SC Gate) of Control register 3 is set. If the designer chooses not to use the RGS14188's shift clock out he must generate a shift clock pulse between the rising edge of -DT/-OE and the falling edge of -DT/-OE between the two transfer cycles to latch the CAS tap address. He must also provide one less shift clock during visible to account for the extra shift clock between the two transfer cycles (gate the first shift clock off).

6.5 Midline Reload Theory

If midline screen refreshes are enabled the column address part of the logical address must be identified. This is done through the CAS Mask register. It is necessary for two reasons. First, so that the midline scheduling logic knows what bits of the shift counter are significant. Second, so the correct row and column address can be isolated and output during the midline transfer cycle. For example, 1 Mbit (256K x 4) VRAMs have 9 row address and 9 column addresses, but because they also have split serial registers, each row of VRAM is conceptually split into two half rows. Each midline transfer cycle loads only one half of the row into the relevant half of the serial register. Therefore, the address must be incremented at the most significant column address bit, rather than the least significant row address bit to select between the two halves of the VRAM. The most significant column address bit is not considered to be part of the tap point, but as the least significant half row address. When a midline transfer cycle occurs, the address output to the VRAMs is the address of the first pixel in the next half row of the VRAM. Therefore, the column portion of the address is '0'.

6.6 Generating Screen Refresh Addresses

The transfer address generator outputs a 24 bit logical address to the internal address mapper. This address can be broken down into three fields shown in Figure 6-1.

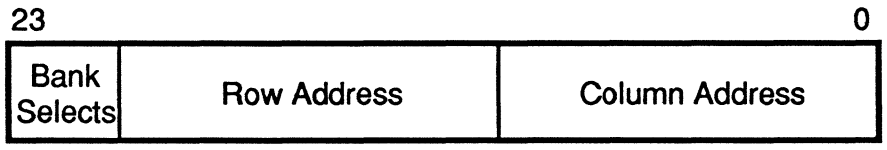


Figure 6-1 24-bit Logical Address for Transfer Address Generator

The precise positioning of all these fields is determined by the size of the VRAM selected. The address may not extend all the way to bit-23 as shown. In a typical system the full address range is not likely to be required. The row address output during the screen refresh cycle specifies the row in memory to be loaded into the serial register internal to the VRAM. the column address determines which bit of that row is

shifted out of the VRAM serial register first. If the display memory is arranged in multiple banks, up to 2-bits can be used for selecting between them.

6.6.1 Horizontal Blanking Screen Refresh Address

The portion of the screen memory actually output to the monitor is referred to as on screen memory. To generate the appropriate address for each horizontal blanking screen refresh one has to know the starting location of the on screen memory, the difference in addresses between two vertically adjacent pixels, the vertical magnification, and whether or not the display in interlaced. The starting location of the on screen memory is loaded into the Display Start register. The difference in addresses between two vertically adjacent pixels, called the display pitch, is loaded into the Display Pitch register and the vertical magnification is loaded into the Y-Zoom register.

6.6.2 Address Generation Hardware and Function

A block diagram of the address generation hardware is shown in Figure 6-2. The register transfer language (RTL) description for how the address generation hardware is controlled is given in the following sections.

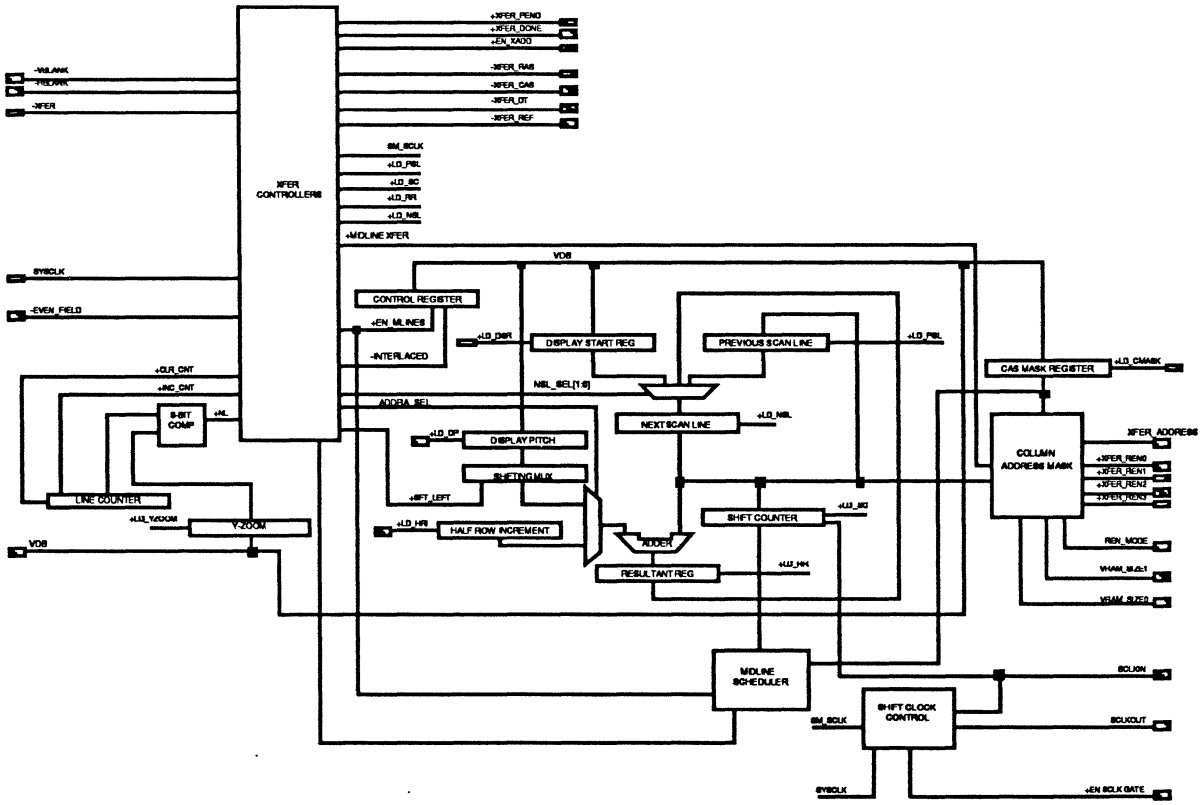


Figure 6-2 Block Diagram of Address Generator

The RTL register and signal descriptions are as follows:

[DSR] - Display Start Register, 24-bits, Host Accessible.
[NSL] - Next Scan Line Register, 24-bits, Not Host Accessible
[PSL] - Previous Scan Line Register, 24-bits, Not Host Accessible
[HRI] - Half Row Increment Register, 24-bits, Host Accessible
[DP] - Display Pitch, 24-bits, Host Accessible
[RR] - Resultant Register, 24-bits, Not Host Accessible
[SC] - Shift Counter, 12-bits, Not Host Accessible
[CM] - CAS Mask Register, 8-bits, Host Accessible
{HLAT} - Time specified in the Horizontal Latency Register
{NL} - Signal indicating the y-zoom count has been exhausted.
{SFT_LEFT} - Signal that selects the left shifted version of the DP register

6.6.2.1 Addressing Sequence for Noninterlaced Displays

```
At the beginning of Vertical Blank
        [DSR] -> [NSL];

At the last Horizontal Blank in Vertical Blank
        [NSL] -> [SC];  * Low 12-bits of the [NSL] *
        Wait for {HLAT} then request a transfer cycle;
        Wait for the transfer request to be granted  then
                [NSL] -> Xfer Cycle;
                [NSL] -> [PSL];
                if midlines are enabled then
                        [NSL] + [HRI] -> [RR];
                        [RR] -> [NSL];
                        [NSL] -> Midline Xfer Cycle, CAS & [CM];

if a midline transfer gets scheduled
        [NSL] + [HRI] -> [RR];
        [RR] -> [NSL];
        Request a transfer cycle;
        When the transfer cycle is granted;
                [NSL] -> Midline Xfer Cycle, CAS & [CM];
        Repeat this loop if more midlines get scheduled before next horizontal blank;

At following Horizontal Blanks

        [PSL] -> [NSL];
        [NSL] + [DP] -> [RR];
        if {NL} = 1 then  [RR] -> [NSL];
        [NSL] -> [SC]; * Low 12-bits of the [NSL] *
        Wait for {HLAT} then request a transfer cycle;
        Wait for the transfer request to be granted  then
                [NSL] -> Xfer Cycle;
                [NSL] -> [PSL];
                if midlines are enabled then
                        [NSL] + [HRI] -> [RR];
                        [RR] -> [NSL];
                        [NSL] -> Midline Xfer Cycle, CAS & [CM]);
```

```
If a midline transfer gets scheduled
        [NSL] + [HRI] -> [RR];
        [RR] -> [NSL];
        Request a transfer cycle;
        When the transfer cycle is granted;
                [NSL] -> Midline Xfer Cycle, CAS & [CM];
        Repeat this loop if more midlines get scheduled before next horizontal blank;
```

6.6.2.2 Addressing Sequence for Interlaced Displays

```
At the beginning of Vertical Blank for the EVEN field
        [DSR] -> [NSL];
        {SFT_LEFT} * Multiply the DP by 2 for the rest of this field *

At the last Horizontal Blank in Vertical Blank
        [NSL] -> [SC];  * Low 12-bits of the [NSL] *
        Wait for {HLAT} then request a transfer cycle;
        Wait for the transfer request to be granted  then
                [NSL] -> Xfer Cycle;
                [NSL] -> [PSL];
                if midlines are enabled then
                        [NSL] + [HRI] -> [RR];
                        [RR] -> [NSL];
                        [NSL] -> Midline Xfer Cycle, CAS & [CM];

if a midline transfer gets scheduled
        [NSL] + [HRI] -> [RR];
        [RR] -> [NSL];
        Request a transfer cycle;
        When the transfer cycle is granted;
                [NSL] -> Midline Xfer Cycle, CAS & [CM];
        Repeat this loop if more midlines get scheduled before next horizontal blank;

At following Horizontal Blanks

        [PSL] -> [NSL];
        [NSL] + [DP] -> [RR];
        if {NL} = 1 then  [RR] -> [NSL];
        [NSL] -> [SC]; * Low 12-bits of the [NSL] *
        Wait for {HLAT} then request a transfer cycle;
        Wait for the transfer request to be granted  then
                [NSL] -> Xfer Cycle;
                [NSL] -> [PSL];
                if midlines are enabled then
                        [NSL] + [HRI] -> [RR];
                        [RR] -> [NSL];
                        [NSL] -> Midline Xfer Cycle, CAS & [CM]);
```

```
If a midline transfer gets scheduled
        [NSL] + [HRI] -> [RR];
        [RR] -> [NSL];
        Request a transfer cycle;
        When the transfer cycle is granted;
                [NSL] -> Midline Xfer Cycle, CAS & [CM];
        Repeat this loop if more midlines get scheduled before next horizontal blank;

At the beginning of Vertical Blank for the Odd field
        [DSR] -> [NSL];
        [NSL] + [DP] -> [RR];
        [RR] -> [NSL];
        {SFT_LEFT} ; * Multiply the DP by 2 for the rest of this field *

At the last Horizontal Blank in Vertical Blank
        [NSL] -> [SC];  * Low 12-bits of the [NSL] *
        Wait for {HLAT} then request a transfer cycle;
        Wait for the transfer request to be granted  then
                [NSL] -> Xfer Cycle;
                [NSL] -> [PSL];
                if midlines are enabled then
                        [NSL] + [HRI] -> [RR];
                        [RR] -> [NSL];
                        [NSL] -> Midline Xfer Cycle, CAS & [CM];

if a midline transfer gets scheduled
        [NSL] + [HRI] -> [RR];
        [RR] -> [NSL];
        Request a transfer cycle;
        When the transfer cycle is granted;
                [NSL] -> Midline Xfer Cycle, CAS & [CM];
        Repeat this loop if more midlines get scheduled before next horizontal blank;

At following Horizontal Blanks

        [PSL] -> [NSL];
        [NSL] + [DP] -> [RR];
        if {NL} = 1 then  [RR] -> [NSL];
        [NSL] -> [SC]; * Low 12-bits of the [NSL] *
        Wait for {HLAT} then request a transfer cycle;
        Wait for the transfer request to be granted  then
                [NSL] -> Xfer Cycle;
                [NSL] -> [PSL];
                if midlines are enabled then
                        [NSL] + [HRI] -> [RR];
                        [RR] -> [NSL];
                        [NSL] -> Midline Xfer Cycle, CAS & [CM]);

If a midline transfer gets scheduled
        [NSL] + [HRI] -> [RR];
        [RR] -> [NSL];
        Request a transfer cycle;
        When the transfer cycle is granted;
                [NSL] -> Midline Xfer Cycle, CAS & [CM];
        Repeat this loop if more midlines get scheduled before next horizontal blank;
```