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APPLE CONFIDENTIAL

Programmers Model for the Big Mac

Introduction

This document describes the Big Mac hardware from the programmers view of the machine which includes a description of the address space maps and a description of each device.

CPU

Clock

The CPU clock is generated by the clock generator gate array which is controlled by three signals CSEL0, CSEL1 and M70. These signals are controlled by dip switches and described by the following table.

CSEL0	CSEL1	M70	OSCFREQ	CPUCLOCK
0	0	0	66.3552Mhz	11.0592Mhz
1	0	0	66.3552Mhz	14.7456Mhz
0	1	0	66.3552Mhz	16.5888Mhz
1	1	0	66.3552Mhz	22.1184Mhz
0	0	1	70.0416Mhz	11.6736Mhz
1	0	1	70.0416Mhz	15.5648Mhz
0	1	1	70.0416Mhz	17.5104Mhz
1	1	1	70.0416Mhz	23.3472Mhz

Interrupts

Level#	Interrupt source
1	Power switch
2	DMA IRQ and Sound interrupt
3	SCSI IRQ
4	VIA IRQ (timer, vsync and onesec)
5	Reserved for slot interrupts
6	SCC IRQ
7	NMI switch

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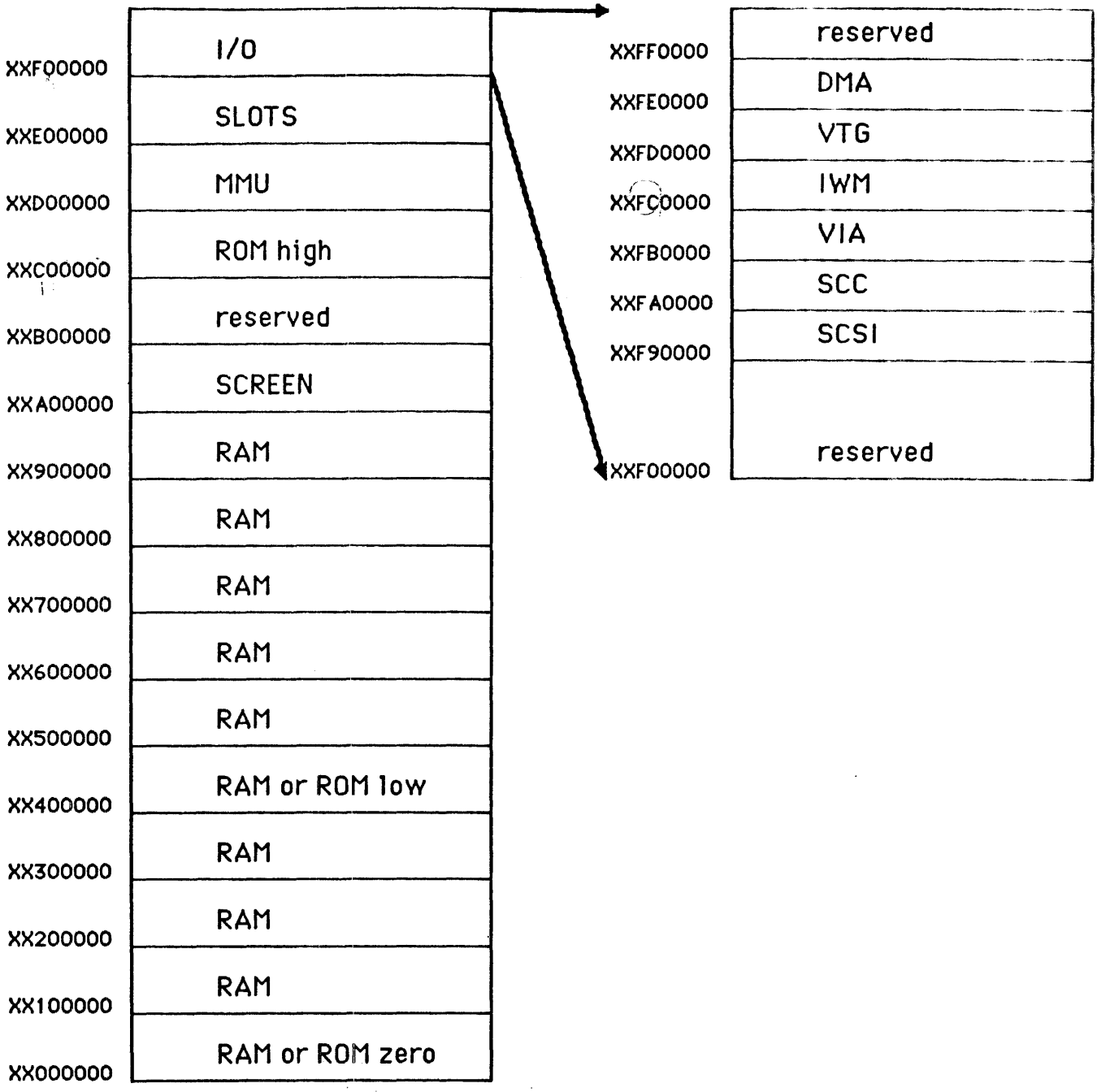
8/14/85

Big Mac Address Space Map (Supervisor State)



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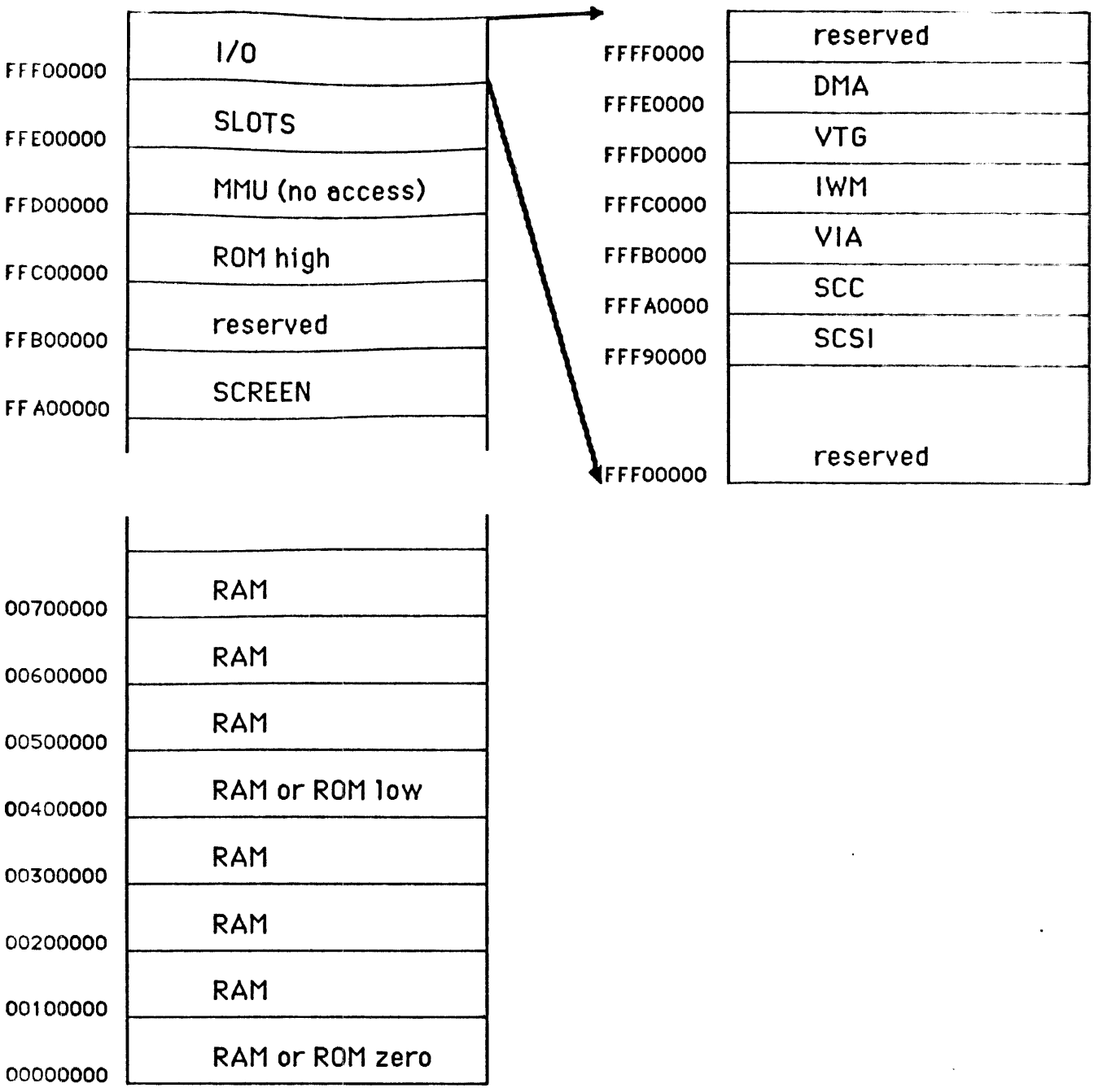
Big Mac Address Space Map (User State)



CPU (continued)

Bus Error

A bus error can be generated by either the AS watchdog or the MMU. The AS watchdog will generate a bus error for bus cycles longer than 2us.

High Decode Map Register

There exists a 4 bit register (located on the VIA) which controls the position of the ROM and provides a mechanism to limit the number of address bits used for decoding logical addresses. This register can programmed to cause the high address bits (those above A23) to be significant to the decoding hardware. This allows a range of address space sizes from 24 to 32 bits. In the smallest configuration, the address space is limited to 16Mb and the upper eight bits are insignificant to decoding which will allow software to use the upper eight bits as tags. In the largest configuration, the address space is 4Gb and none of upper bits are available.

Address Space Map

The address space map is determined by the High Decode Map register and the FC2 signal (ie. user/supervisor bit from the 68020). See the following pages for drawings of the supervisor and user state address space maps. There are five configurations which are defined as follows:

FC2	HDM3	HDM4	VMsize	RAMsize	RAM	I/O,ROM,MMU,SCREEN
1	X	X	16Mb	10Mb	/A23	A23
0	1	1	16Mb	8Mb	/A23	A23
0	1	0	32Mb	16Mb	/A24	A24*A23
0	0	1	512Mb	256Mb	/A28	A28*A24*A23
0	0	0	4Gb	2Gb	/A31	A31*A28*A24*A23

Note: The first configuration (ie. FC2 = 1) is supervisor state and the last four configurations (ie. FC2 = 0) are user state.

ROM

Size

The prototype is currently wired for a byte wide 32Kb EPROM with A0 brought into the most significant address line.

Decode

The position of the ROM is determined by the High Decode Map register and the FC2 signal (ie. user/supervisor bit from the 68020). The HDM1 bit overlays the ROM at location zero (ie. at power on) and the HDM2 bit is the ROM low/high select line. The configurations are defined as follows:

FC2	HDM1	HDM2	HDM3	HDM4	Location	ROM high bit decode
1	1	X	X	X	XX000000, XX400000, XXC00000	
1	0	1	X	X	XX400000	A23
1	0	0	X	X	XXC00000	A23
0	0	1	X	X	XX400000	A23
0	0	0	1	1	FFC00000	A23
0	0	0	1	0	FFC00000	A24*A23
0	0	0	0	1	FFC00000	A28*A24*A23
0	0	0	0	0	FFC00000	A31*A28*A24*A23

Note: The first three configurations (ie. FC2 = 1) are supervisor state with the high byte always ignored. The last five configurations are user state with the options to ignore some or all of the upper address bits.

I/O, SLOTS, MMU, ROM, SCREEN Addresses

The I/O, SLOTS, MMU, ROM and SCREEN are decoded using addresses A20 through A23 as follows:

Address	Device	Comments
FFF00000	I/O	Decoded using A16-A19 for I/O devices
FFE00000	SLOTS	256Kb per slot
FFD00000	MMU	Accessible only in supervisor state
FFC00000	ROM	Dependent on HDM1 and HDM2 bits
FFB00000	Reserved	
FFA20000	SCREEN	High video page 100Kb
FFA00000	SCREEN	Low video page 100Kb

Note: The high byte is determined by FC2, HDM3 and HDM4.

Input/Output Addresses

The I/O space is decoded using addresses A16 through A19 into eight spaces as follows:

	Address	Device	Register Decode Bits	Register Offset
9	FFF90000	SCSI	A4,A5,A6	$10
A	FFFA0000	SCC	A1,A2	$2
B	FFFB0000	VIA	A9,A10,A11,A12	$200
C	FFFC0000	IWM	A9,A10,A11,A12	$200
D	FFFD0000	VTG	A4,A5,A6	$10
E	FFFE0000	DMA	A1-A7	$2

SCC

Select lines

The A/B select line is connected to A1 and the C/D select line is connected to A2.

VIA

Select lines

The register select lines RS0 thru RS3 are connected to A9 thru A12.

Ports and Handshake lines

PA0	SV1	Sound volume LSB
PA1	SV2	
PA2	SV3	Sound volume MSB
PA3	APTKA1	Apple talk mode (low true?)
PA4	HDM1	Rom Overlay at zero (high true)
PA5	HDSEL	Floppy Head select & RTC chip enable
PA6	VIDPG	Video page select
PA7	WAREQ1	Scc wait request channel A
CA1	VSYNC	Vertical retrace 60Hz interrupt
CA2	CINT	RTC one second interrupt
PB0	HDM2	ROM position
PB1	HDM3	See address space map discussion
PB2	HDM4	See address space map discussion
PB3	FINT	FDB status line
PB4	ST0	FDB state 0 control line
PB5	ST1	FDB state 1 control line
PB6	PWROFF	Power off (low true)
PB7	SNDRES	Sound reset (low true)
CB1	FCLK	FDB & RTC clock
CB2	FDATA	FDB & RTC data

Note: When HDM1 (ie. PA4) is high ROM is overlayed at zero