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ADO
AMPEX DIGITAL OPTICS

SERVICE MANUAL

AMPEX CORPORATION
AUDIO-VIDEO SYSTEMS DIVISION

Prepared by

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ADO System Components

SECTION 1

GENERAL INFORMATION

1-1 SCOPE OF MANUAL

This manual provides the following information about the ADO (Ampex Digital Optics) System, NTSC, Ampex Part Number 1420200:

- Section 1, *General Information*, describes the general characteristics and functions of the ADO System.
- Section 2, *Installation*, provides instructions for mounting and interconnecting the System.
- Section 3, *Operation*, provides simplified operating instructions.
- Section 4, *Maintenance*, provides information about test equipment, disassembly, circuit breakers and fuses, and adjustments and troubleshooting.
- Section 5, *Theory of Operation*, provides system-level and PWA-level theory descriptions.

In the theory section of this manual the analog circuitry is described at the system level. Detailed theory for the image processing PWAs will be included in a future manual. Adjustment and troubleshooting procedures are presented for the analog section. The control system PWAs, primarily software-dependent computer PWAs, are also described at the system level. PWA theory descriptions of the analog PWAs and control unit PWAs will be provided in an addendum to this manual.

Although electrical maintenance and theory descriptions in this manual have been prepared from NTSC documentation, they are useful for PAL models as well. Circuit differences consist of PROM coding, PAL/NTSC jumper selections, and minor circuit changes. Documentation for PAL circuit differences will be given in an addendum to this manual, to be provided later.

1-2 RELATED PUBLICATIONS

ADO System related publications are listed below. See Appendix A for vendor publications.

- ADO Operator's Guide, Ampex Catalog No. 1809551
- ADO Parts Lists and Schematics, Ampex Catalog No. 1809564

1-3 INTENDED USE AND CAPABILITIES

The ADO system is used to transform the geometry of video pictures at real-time video rates. The transformations include translation, compression, expansion,

ADO

rotation, perspective projection, and combinations of these. To create a visual sequence, the operator uses a keyboard and a joystick control in conjunction with a menu displayed on a CRT monitor. An optional 5-1/4-inch floppy disk system provides storage of operating control sequences.

1-4 FUNCTIONAL DESCRIPTION

The ADO System consists of a control unit and a signal system chassis (Figure 1-1). The composite video input is converted to its luminance (Y) and chrominance (R-Y, B-Y) components which are then digitized. The digitized Y and chroma data is manipulated by the digital processor to provide the desired transformations. The processed digital information is then converted back to composite analog video. The digital processor also provides a key signal.

The keyboard CPU (Central Processing Unit) passes operator selection information to the CPP (Control Processor). The CPP controls the menu monitor display and optional disk drive and passes data to the HLC (High Level Controller) via the I/O PWA. The HLC drives the LLC (Low Level Controller), which directly controls the digital processor. The ADO System uses five microprocessors, two within the control unit, one within the HLC, and two within the LLC.

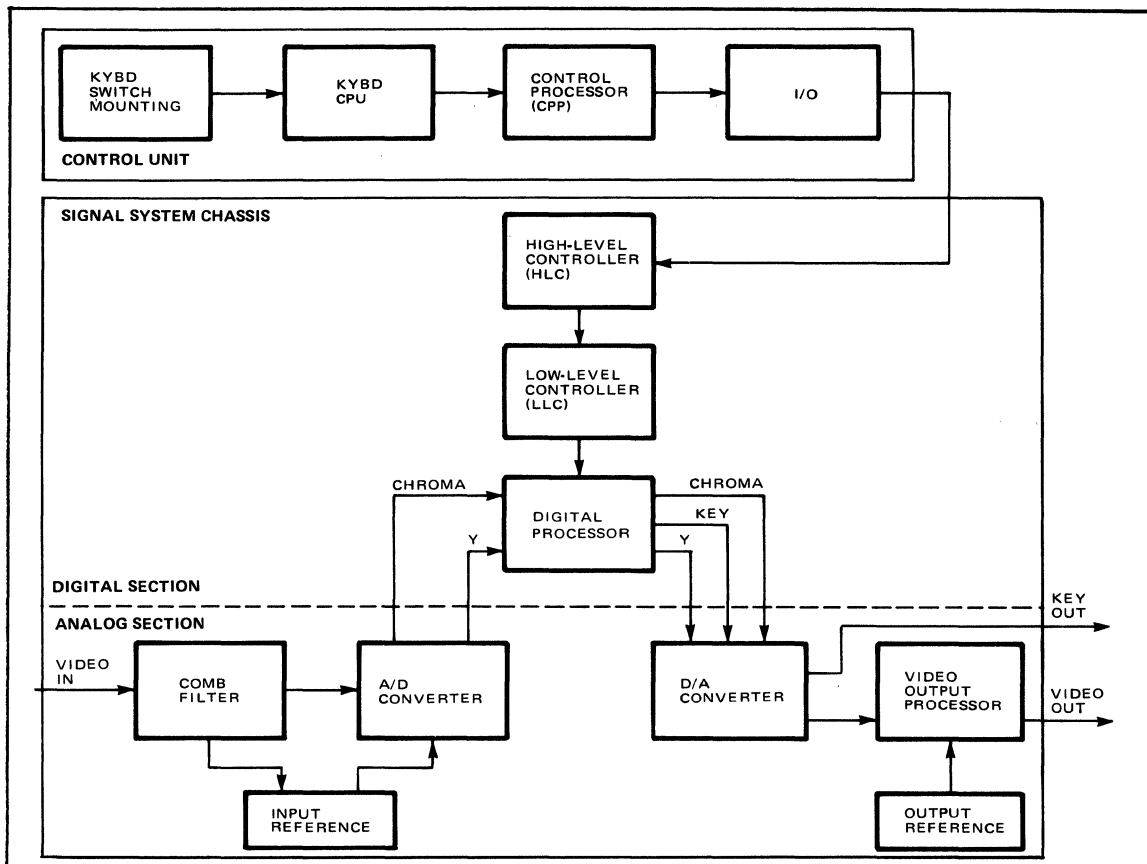


Figure 1-1. ADO Simplified Functional Diagram

1-5 PHYSICAL DESCRIPTION

The main components of the ADO System are shown in Figure 1-2. The control unit includes a keyboard and a CRT menu monitor which can be located on a desk or console for convenient use by the operator. The signal system chassis can be mounted in a 19-inch rack. Note that the ADO Parts Lists and Schematics manual refers to the signal system chassis as the "basic channel assembly."

1-6 Control Unit

The control unit components are:

- The keyboard, which contains a joystick and pushbutton keys used for entering ADO information; some of the keys are assigned by software.
- The menu monitor, which contains a CRT display, space for a floppy disk system, and a microprocessor.

The control unit is connected to the signal system chassis by serial data links. Additional ports are provided for connection to associated equipment.

1-7 Signal System Chassis

The signal system chassis contains analog and digital sections, power supplies, and cooling fans. The upper portion of the unit consists of the analog section, which

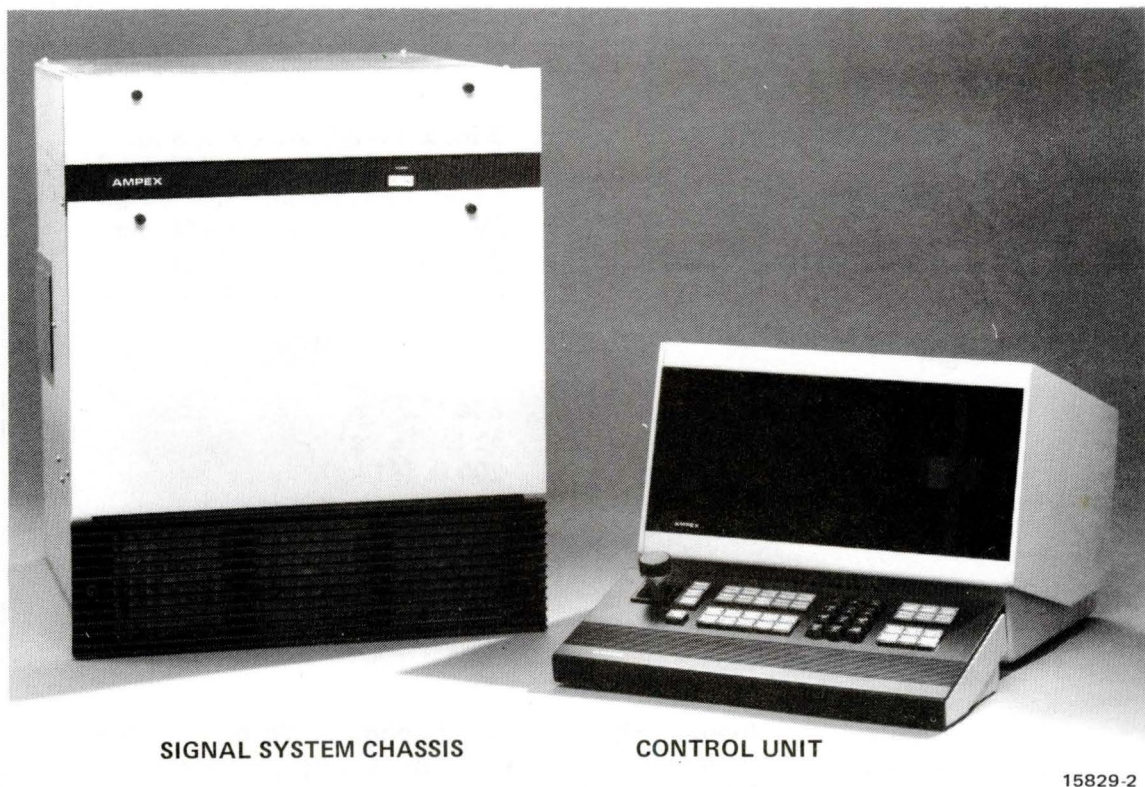


Figure 1-2. ADO System Components

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contains six PWAs (listed in Figure 4-4). The lower portion consists of the digital section. This section is accessed by a separate hinged panel and has provisions for 27 PWAs (listed in Figure 4-6). All connections to the signal system chassis are made by connectors located at the rear of the unit.

1-8 Software

All ADO software is contained in PROMs used within five microprocessors. Software in the menu monitor unit controls the ports used to connect the system to associated equipment. Required software changes can be provided by means of PROM exchanges.

1-9 OPTIONS, ACCESSORIES, AND SUPPLIES

Present and future options include the floppy disk drive, address generator, rotation, and concentrator. The Perspective I and II PWAs are also documented as options. However, these two PWAs are required for system operation at present, until other address generator PWAs are available. Analog and digital extender PWAs are provided with the basic PWAs, for servicing the unit. Supplies include the floppy disks for the optional disk drive.

1-10 SPECIFICATIONS

Physical dimensions and power requirements are given in Table 1-1.

Table 1-1. ADO Specifications

Size (HWD)	
Keyboard Unit:	5 in. x 15-1/4 in. x 7-5/8 in. (126 mm x 387 mm x 194 mm)
Menu Monitor:	12 in. x 15-3/8 in. x 15-3/4 in. (305 mm x 390 mm x 400 mm)
Signal System Chassis:	22-3/4 in. x 19 in. x 22 in. (578 mm x 483 mm x 560 mm)
Weight	
Keyboard Unit:	6 lb (2.7 kg)
Menu Monitor:	35 lb (16 kg)
Signal System Chassis:	200 lb (91 kg)
Power Requirements	
Control Unit:	115V @ 150W
Signal System Chassis:	115V @ 2500W
Video	
Input:	Input 1(A), input 2(B): 75 ohms, 1 Vp-p, composite
Output:	2 identical outputs: 75 ohms, 1 Vp-p, composite
Key Output:	Key Signal, 75 ohms, noncomposite

SECTION 2

INSTALLATION

This section provides information for unpacking, inspection, mounting, and inter-connection of the ADO System.

2-1 UNPACKING

The System is shipped from the factory in a specially constructed packing case. Caution should be exercised in unpacking to prevent damage to the cabinet finish or associated parts. Check contents of the packing case and check packing materials for accessory items. Check all items against the packing list to ensure shipment is complete. Carefully examine the contents for damage that may have occurred during shipment. Notify the carrier and the Ampex representative of any shortage or damages. If it is anticipated that equipment will be moved or reshipped, retain all shipping containers and packing materials.

2-2 LOCATION AND MOUNTING

The ADO keyboard unit and menu monitor can be mounted on any flat surface of suitable size. The signal system chassis can be mounted in a 19-inch rack. Refer to Table 1-1 for physical dimensions and power requirements. The area chosen for the System should be adequately ventilated and relatively dust free. Cooling air is drawn into the front of the System and is discharged at the rear. The System should not be close to any strong electromagnetic fields. Common sources of interference include fluctuating loads on nearby high-current lines, fluorescent lighting, heavy duty transformers, elevator motors, and radio, television, and amateur radio transmitting equipment.

For determining mounting-space requirements, physical dimensions for each major component are shown in Figures 2-1 through 2-3. When considering location, be certain to provide adequate access space at the rear of the CRT monitor and signal system chassis for cable connections and servicing. The keyboard unit and menu monitor can be located up to 2,000 ft (607 m) from the signal system chassis.

2-3 SIGNAL SYSTEM CHASSIS RACK MOUNTING

WARNING

BECAUSE OF THE WEIGHT OF THE SIGNAL SYSTEM CHASSIS TWO OR MORE PERSONS ARE NEEDED TO LIFT THE UNIT INTO PLACE IN THE RACK. FOR CONVENIENCE WHILE INSTALLING THE RACK-MOUNTING SCREWS, USE A BLANK PANEL OR OTHER SUPPORT FOR THE UNIT TO REST ON.

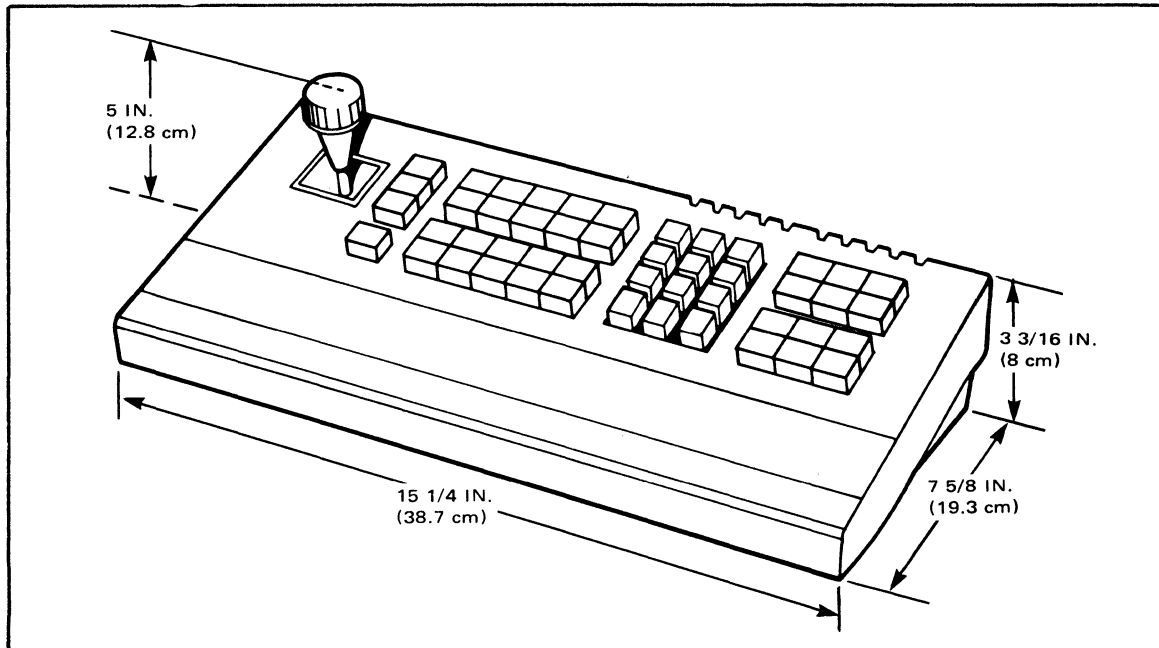


Figure 2-1. Keyboard Unit Dimensions

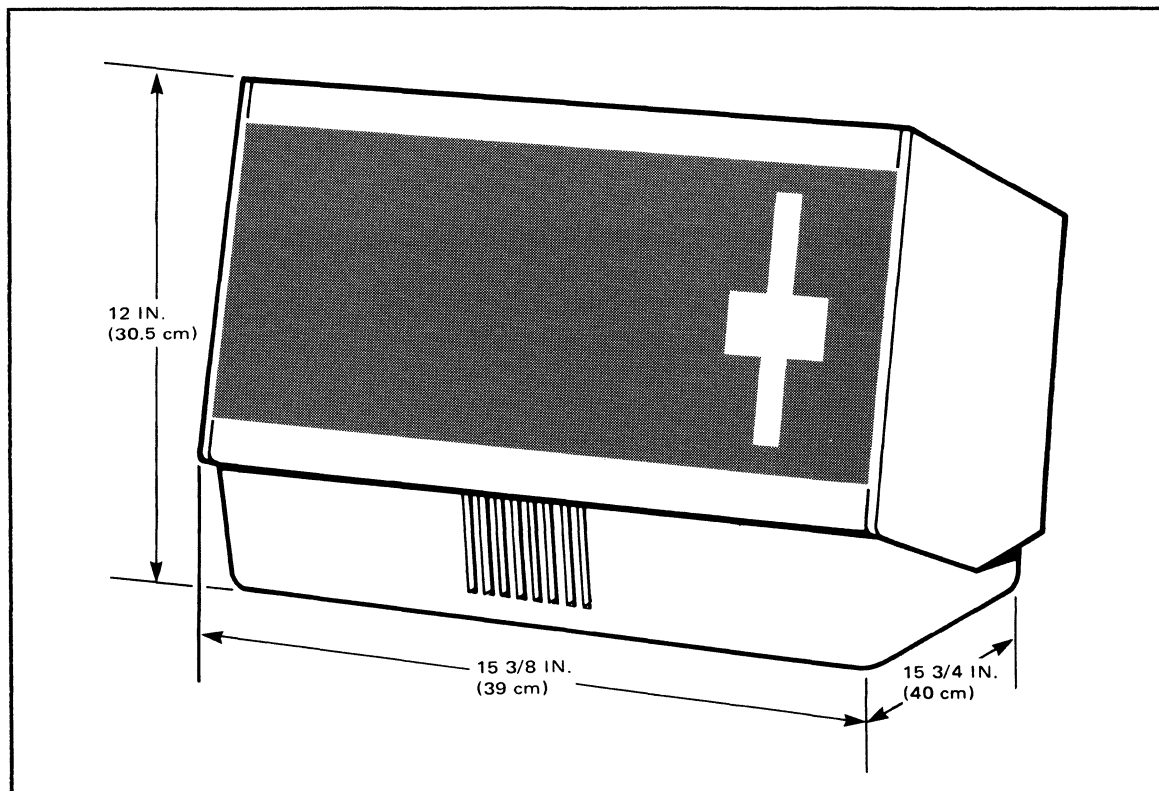


Figure 2-2. Menu Monitor Dimensions

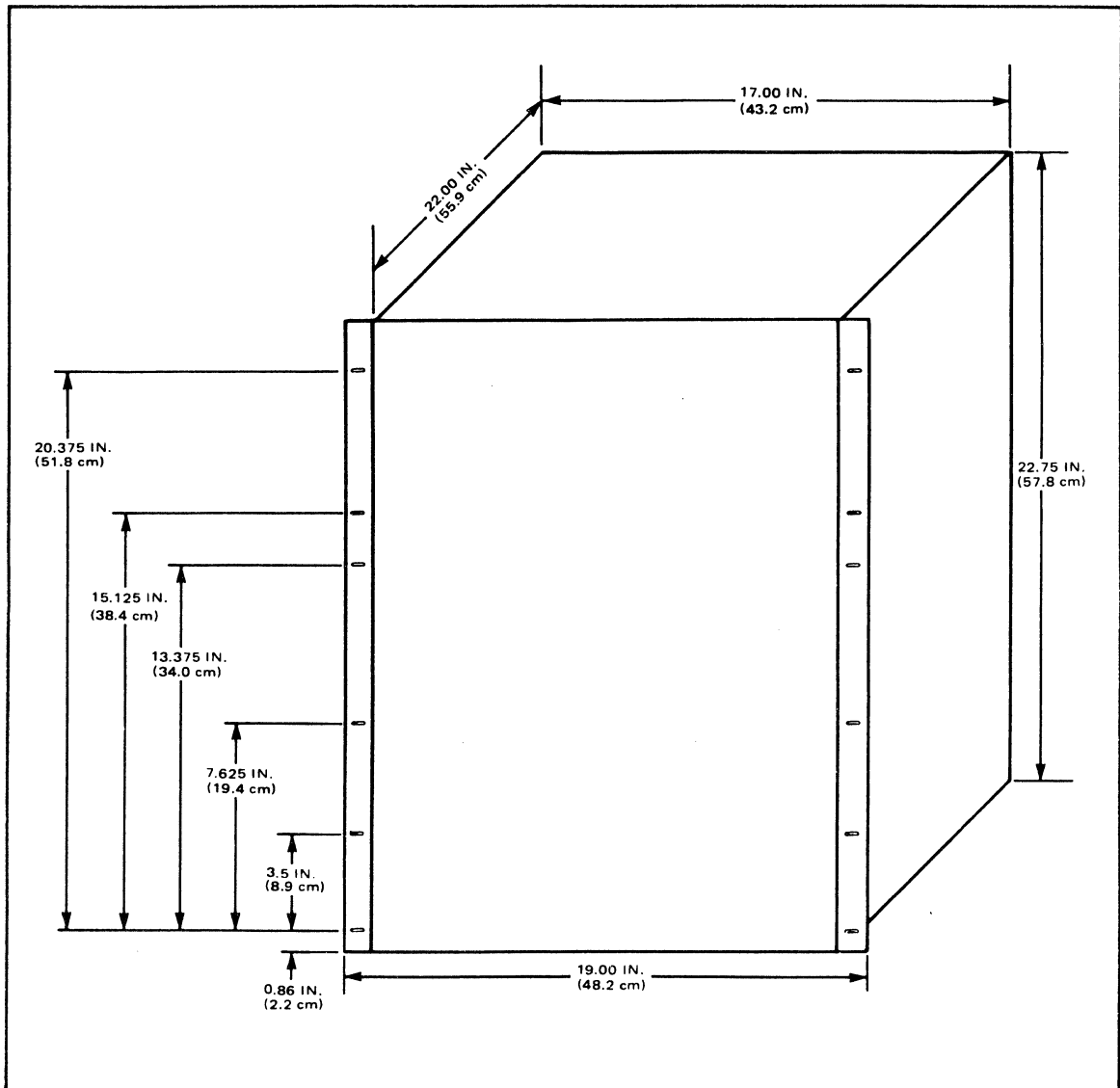


Figure 2-3. Signal System Chassis Dimensions

The signal system chassis is designed to mount in a standard 19-inch (483 mm) rack and occupy 22.75 inch (578 mm) of vertical rack space. For signal system chassis dimensions, refer to Figure 2-3. Allow adequate space behind the unit for cable connection, air flow, and servicing.

Mount the unit into a rack as follows:

- STEP 1** With the two doors closed, remove the two screws (A) that hold the grill to the bottom front of the cabinet. (See Figure 2-4.)
- STEP 2** Remove the two screws (B) that hold each of the two grill mounting clips.

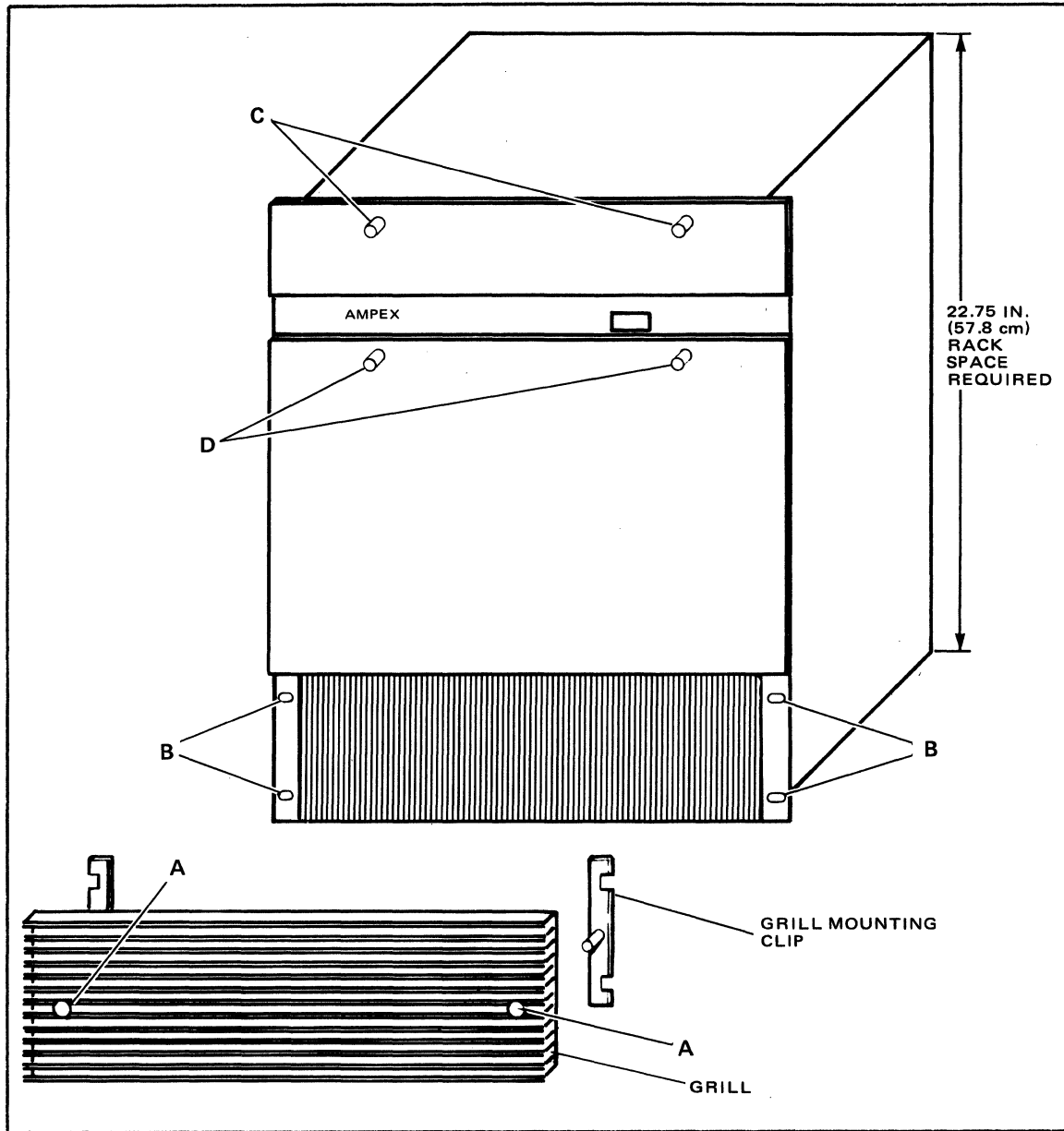


Figure 2-4. Signal System Chassis

Note

It is necessary to remove handles from sides of cabinet before mounting unit into rack (four screws each handle).

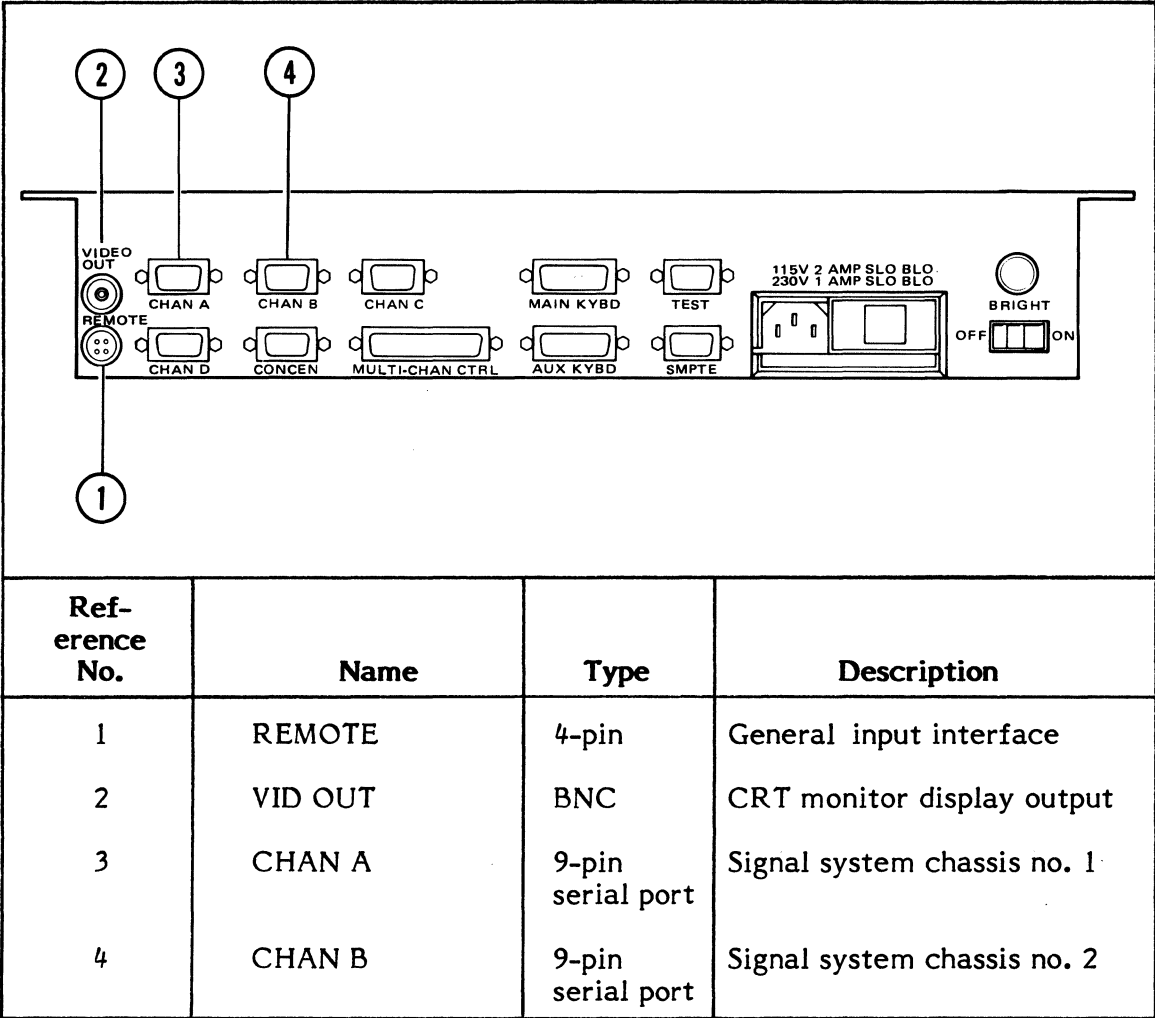
- STEP 3** Place unit into the 19-inch rack and secure with four screws (B).
- STEP 4** Turn latches (C) counterclockwise to release top door. Open door and install two mounting screws, one each side. Close and secure door.

- STEP 5 Turn latches (D) counterclockwise to release bottom door. Open door and install six mounting screws, three each side. Close and secure door.
- STEP 6 Loosen bottom four screws and install the slotted grill mounting clips. Tighten screws.
- STEP 7 Reinstall grill (two screws).

2-4 POWER AND SIGNAL CONNECTIONS

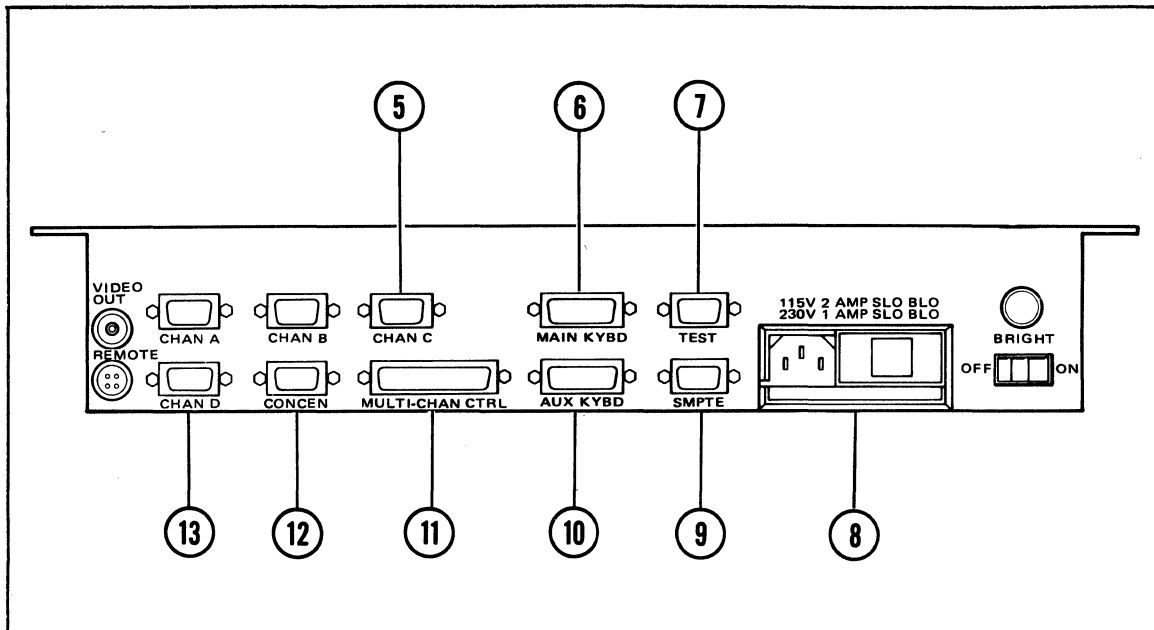
All connections to and from the ADO System are made to connectors at the rear of the menu monitor and the signal system chassis. These connections for a single-channel system are listed and described in Tables 2-1 and 2-2. Figure 2-5 is a basic system interconnection diagram.

Table 2-1. Menu Monitor Connector Panel



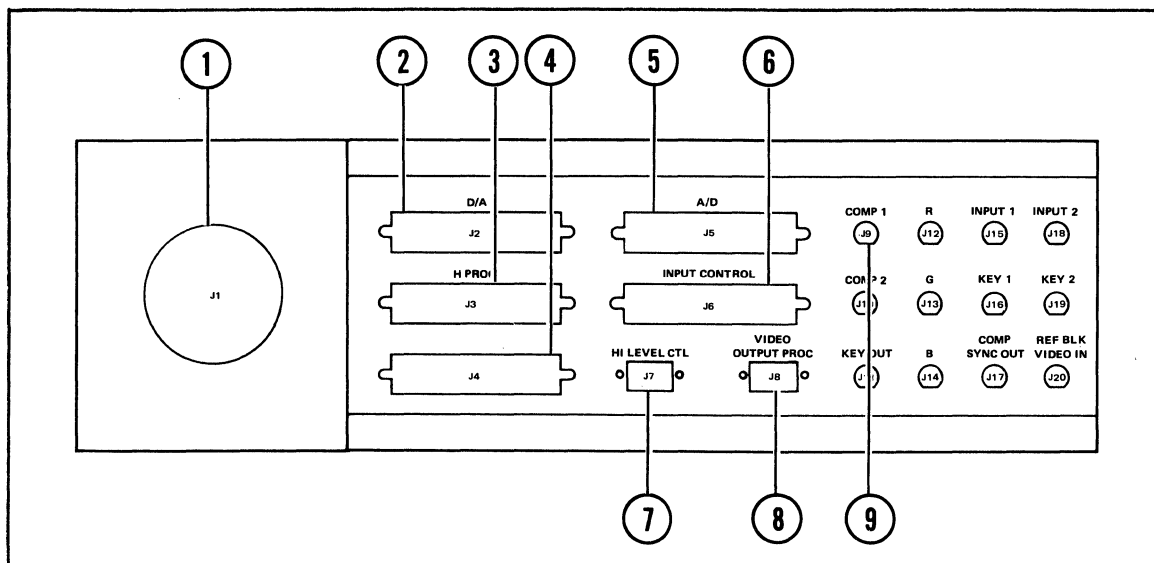
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Table 2-1. Menu Monitor Connector Panel (Continued)



Reference No.	Name	Type	Description
5	CHAN C	9-pin	Signal system chassis no. 3 serial port
6	MAIN KYBD	15-pin	Keyboard port
7	TEST		Not currently used
8	115V 2 AMP SLO BLO 230V 1 AMP SLO BLO	3-wire	115 Vac input connector fuse
9	SMPTE		Serial control port
10	AUX KYBD	15-pin	Auxiliary keyboard port
11	MULTI-CHAN CTRL	25-pin	Combined signal system ports
12	CONCEN	9-pin	Signal system chassis no. 5 serial port
13	CHAN D	9-pin	Signal system chassis no. 4 serial port

Table 2-2. Signal System Chassis Connector Panel



Reference No.	Number	Name	Type	Description
1	J1	115 VAC	Three-prong power	Power input
2	J2	D/A	Ribbon	Digital input to analog section
3	J3	H PROC	Ribbon	Digital processor output
4	J4	-	-	Not used
5	J5	A/D	Ribbon	Digital output from analog section
6	J6	INPUT CONTROL	Ribbon	Digital processor input
7	J7	HI LEVEL CTL	9-Pin, Type D	Serial port to CRT menu monitor
8	J8	VIDEO OUTPUT PROC	9-Pin, Type D	For concentrator option
9	J9	COMP 1	BNC	Composite video output 1

(Continued next page)

Table 2-2. Signal System Chassis Connector Panel (Continued)

Ref-erence No.	Number	Name	Type	Description
10	J10	COMP 2	BNC	Composite video output 2
11	J11	KEY OUT	BNC	Key output (noncomposite)
12	12	R	BNC	Red output (OPTIONAL)
13	J13	G	BNC	Green output (OPTIONAL)
14	J14	B	BNC	Blue output (OPTIONAL)
15	J15	INPUT 1	BNC	Composite video input 1 (Input A)
16	J16	KEY 1	BNC	Key video input 1 (Input A) (OPTIONAL)
17	J17	COMP SYNC OUT	BNC	Composite sync output (OPTIONAL)
18	J18	INPUT 2	BNC	Composite video input 2 (Input B)
19	J19	KEY 2	BNC	Key video input 2 (Input B) (OPTIONAL)
20	J20	REF BLK VIDEO IN	BNC	Station reference black burst video input

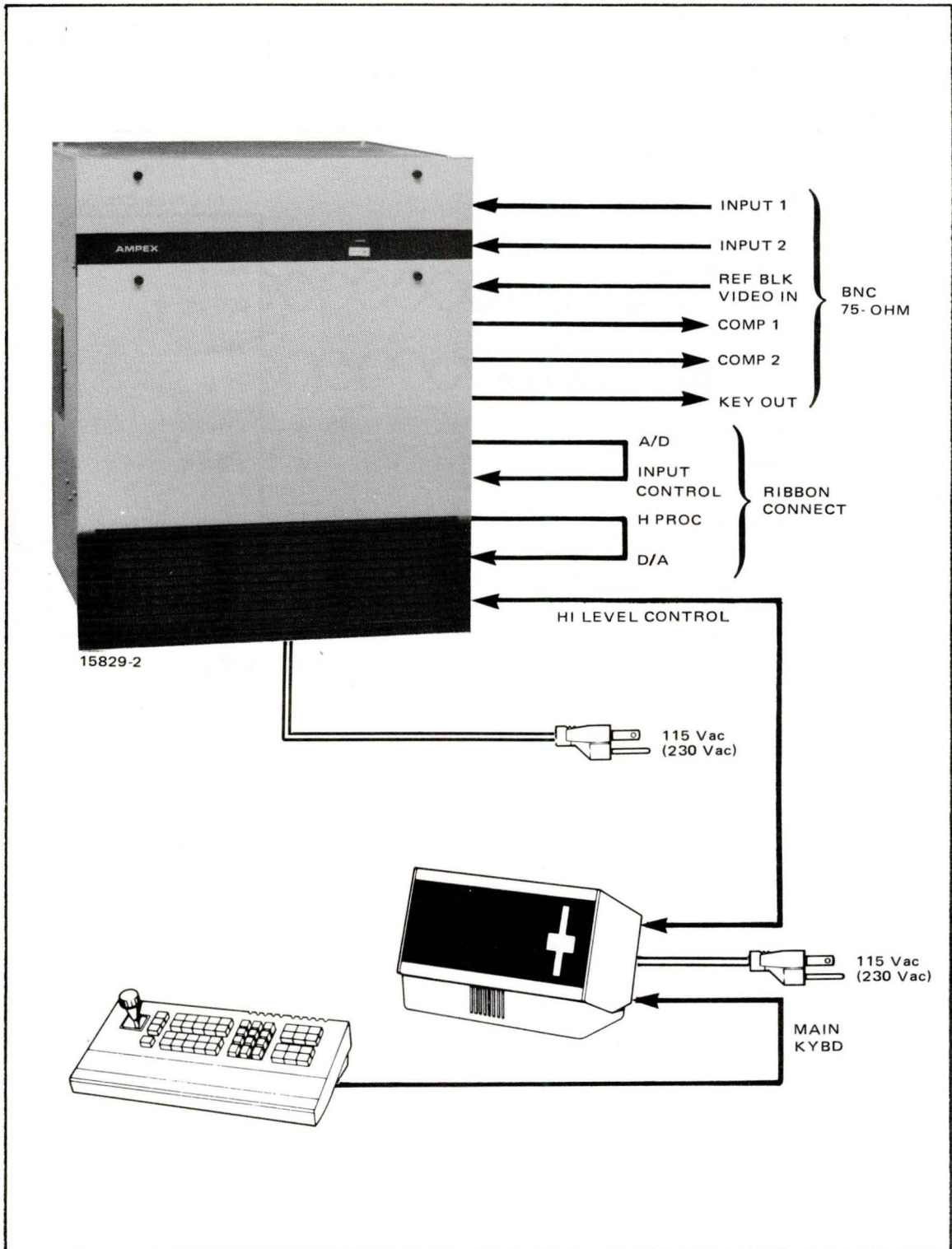


Figure 2-5. ADO System Basic Interconnection

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The connection between the connector HI LEVEL CTL on the rear of the signal system chassis and the CHAN 5 connector on the CRT display unit can be up to 2,000 ft (607 m) in length. Figure 2-6 is a wiring diagram of this cable.

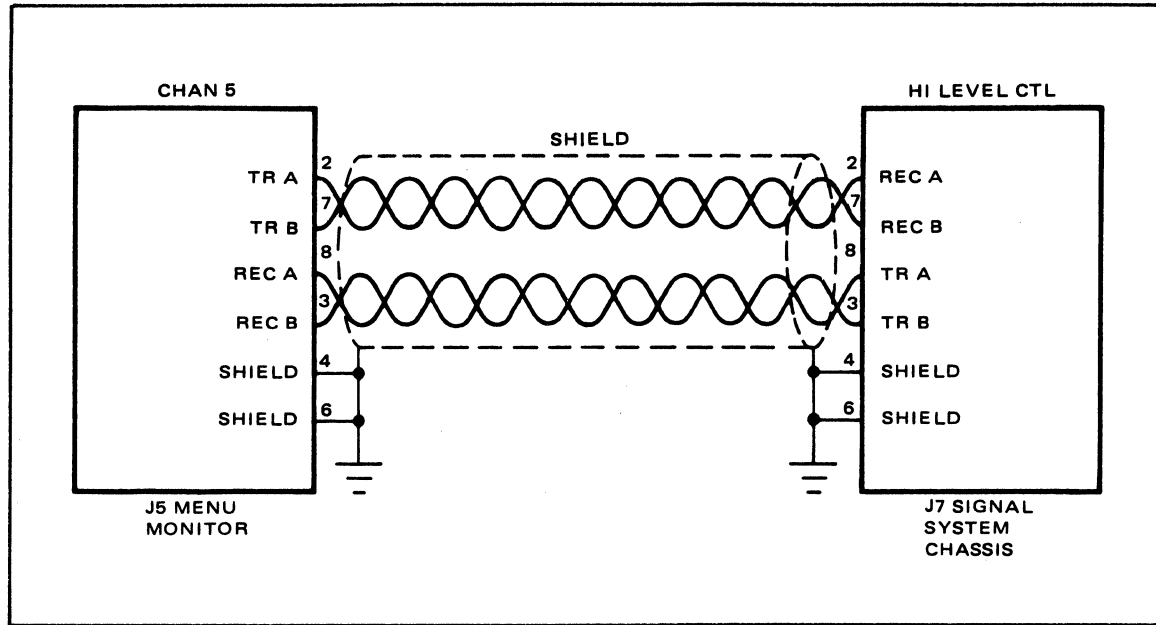


Figure 2-6. High Level Control to Channel 5 Cable

SECTION 3 OPERATION

3-1 INTRODUCTION

This section of the manual presents operating procedures and the locations and functions of operating controls and indicators. For detailed operating information, refer to the ADO Operator's Guide.

3-2 CONTROLS AND INDICATORS

Primary operating controls are located on the control unit. These controls are shown in Figure 3-1. Simplified descriptions of the controls are presented in Table 3-1. Refer to the ADO Operator's Guide for detailed descriptions.

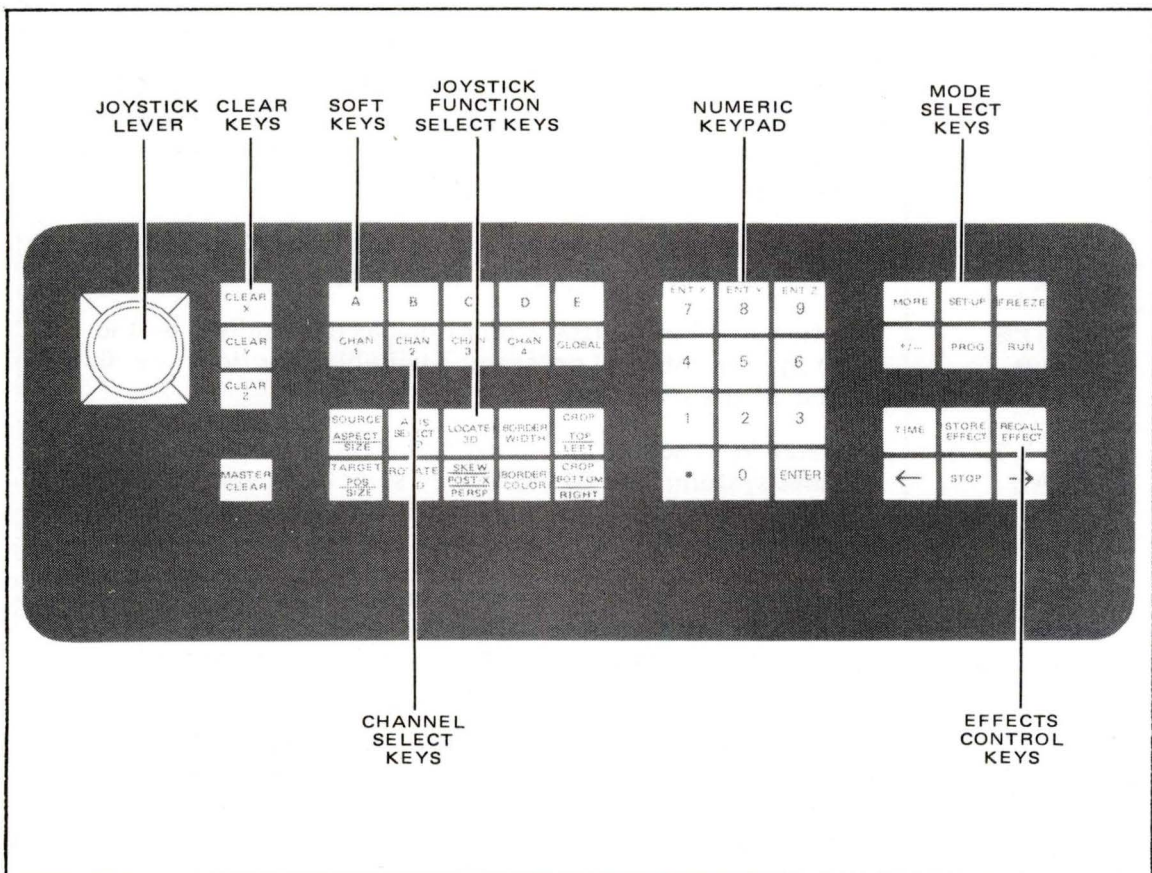


Figure 3-1. Keyboard Controls

Table 3-1. Keyboard Controls and Indicators

Description	Function
Joystick Lever and Knob	<p>Joystick lever is used to control the type of effect, its direction, and degree.</p> <p>The type of effect is selected by the Joystick Function Select Keys and the axis of deflection is controlled by the joystick lever.</p> <p>The X axis is controlled by deflecting the lever left or right.</p> <p>The Y axis is controlled by deflecting the lever forward or back.</p> <p>The Z axis is controlled by rotating the lever clockwise or counterclockwise.</p> <p>All parameters of the effect are controlled by the amount of deflection of the joystick.</p>
CLEAR X (or Y or Z)	<p>Removes any effect of the selected function present in the X (or Y or Z) axis. When in rotate mode, the CLEAR X (or Y or Z) key provides an additional function: when pushed once it clears to the nearest 90° of X (or Y or Z) rotation; when pushed again it clears to zero.</p>
MASTER CLEAR	<p>Removes all effects present in the X, Y, and Z axis of the video, and returns the picture to normal 1 to 1 ratio.</p>
A,B,C,D,E soft keys	<p>The five soft keys initiate functions as determined by the ADO System internal program. Available functions are displayed on the menu monitor.</p>
CHAN 1,2,3,4 GLOBAL	<p>Channel keys select individual channels in a multiple channel system; the GLOBAL key selects all channels. The GLOBAL key causes an overall configuration to be transformed rather than the individual key frames.</p>
Joystick Function Select Keys	<p>The ten joystick function select keys are mutually exclusive but can be performed serially. The joystick is used to manipulate the three axes of the video picture according to the function selected.</p>
SOURCE ASPECT/SIZE	<p>When this key is pressed, the joystick is used to change the aspect ratio of the video picture along the X (horizontal) or Y (vertical) axis; joystick rotation changes the overall size of the picture.</p>

(Continued next page)

Table 3-1. Keyboard Controls and Indicators (Continued)

Description	Function
AXIS SELECT 3D	Joystick selects key frame axis of rotation (X, Y, Z).
LOCATE 3D	Establishes joystick control of image movement with corresponding visual presentation of image area seen in new perspective (X, Y, Z axis—three dimensions). Changes the relative point of view of the ADO System image.
BORDER WIDTH	Selects border width. Border width entered through numeric keypad.
CROP TOP/LEFT	Sets the top and left edges of the crop; only X-axis and Y-axis controls are active.
TARGET POS/SIZE	Allows operator to move picture in a horizontal (X) or a vertical (Y) direction. Knob rotation controls the size of the picture.
ROTATE 3D	Permits operator to rotate image around any axis (X,Y,Z).
SKEW POST X/ PERSP	Joystick in X-axis skews (slants) the picture to right or left; or in the Y-axis executes the post-X function. This function is an advanced special effect X rotation not obtainable by use of the rotate 3D key; it operates in target space rather than in source space. (Refer to ADO Operator's Guide.) Rotating the joystick knob adds or subtracts degrees of perspective in the picture.
BORDER COLOR	Selects border color. Color entered through numeric keypad.
CROP BOTTOM/RIGHT	Sets the bottom and right edges of the crop; only X-axis and Y-axis controls are active.
0 through 9, ENT X, ENT Y, ENT Z	For entering numeric quantities such as duration times, freeze effect times, and effect code numbers.
.	Decimal point.
ENTER	Accepts a numeric entry.
Mode Select Keys	Select ADO mode of operation.

(Continued next page)

ADO

Table 3-1. Keyboard Controls and Indicators (Continued)

Description	Function
MORE	When there are more than five soft functions, pressing MORE enables paging through sets of five soft functions at a time.
SETUP	This key is for use by engineering personnel only. It sets up an adjustment mode for analog board parameters, making use of the soft keys and the menu monitor display. The setup mode also provides displayed values used in adjusting the joystick. In addition, it provides for initialization of blank disks.
FREEZE	Freezes the input video; with input video disconnected, this image can still be transformed in any manner.
+/-	The +/- pushbutton is pressed to change the sign of an entry entered through the numeric keyboard.
PROG	Program pushbutton switch. Allows operator to create an effect by placing the ADO in the program mode.
RUN	Executes a previously defined (created) effect.
Effects Control Keys	Used for controlling, storing, recalling, and changing duration of keyframes and effects.
TIME (duration)	Allows operator to program durations the ADO will use to transit from keyframe to keyframe. Durations are entered in seconds and frames.
STORE EFFECT	Stores programmed effect on disk. Up to 36 effects can be stored.
RECALL EFFECT	Summons selected effect from disk.
REVERSE	When pressed in program mode, system steps back one key frame in the effect. When pressed in run mode, effect runs backward from its present state.
STOP	When pressed in run mode, the effect stops at the point when pressed.
FORWARD	When pressed in program mode, system steps forward to next key frame in the effect or to next key frame available. When pressed in run mode, effect runs forward from its present state.

3-3 STARTING THE SYSTEM

Apply power to the ADO System and insert a diskette as follows:

CAUTION

REMOVE THE DISKETTE BEFORE TURNING POWER ON OR OFF.

- STEP 1** At the front of the signal system chassis, press the circuit-breaker switch to the ON position (Figure 3-2). The switch indicator will light.
- STEP 2** At the rear of the CRT menu monitor, press the power ON/OFF switch to the ON position. After the monitor CRT warms up, adjust the BRIGHT control for the desired level of CRT illumination.
- STEP 3** Open disk drive door by pulling the door latch forward (Figure 3-3).
- STEP 4** Insert a 5-1/4-inch diskette, with slot in jacket on the edge that enters the drive first and with notch on top edge, until the diskette jacket is solidly against the backstop.

CAUTION

IF THE DISKETTE IS NOT PROPERLY INSERTED, THE CENTER HOLE OF THE DISKETTE MAY BE DAMAGED WHEN THE DOOR IS CLOSED.

- STEP 5** Close disk drive door by pressing latch to the left.

3-4 DISKETTE HANDLING AND STORAGE

It is important that the diskette be handled and stored properly so that the integrity of the recorded data is maintained (Figure 3-4). A damaged or contaminated diskette can impair or prevent recovery of data and can result in damage to the read/write head.

3-5 MENU MONITOR DISPLAY

The monitor display consists of 16 lines x 64 characters of data. The first two lines are reserved for general header and status display. The last two lines are used to display the current meaning of all soft keys. In summary, the display consists of the following:

- 2 lines of general status
- 12 lines of data
- 1 blank line
- 1 line of soft key designations

The home menu is displayed on power-up and is used for channel acquisition, release, setup, and test. See the ADO Operator's Manual (Ampex 1809551) for further information.

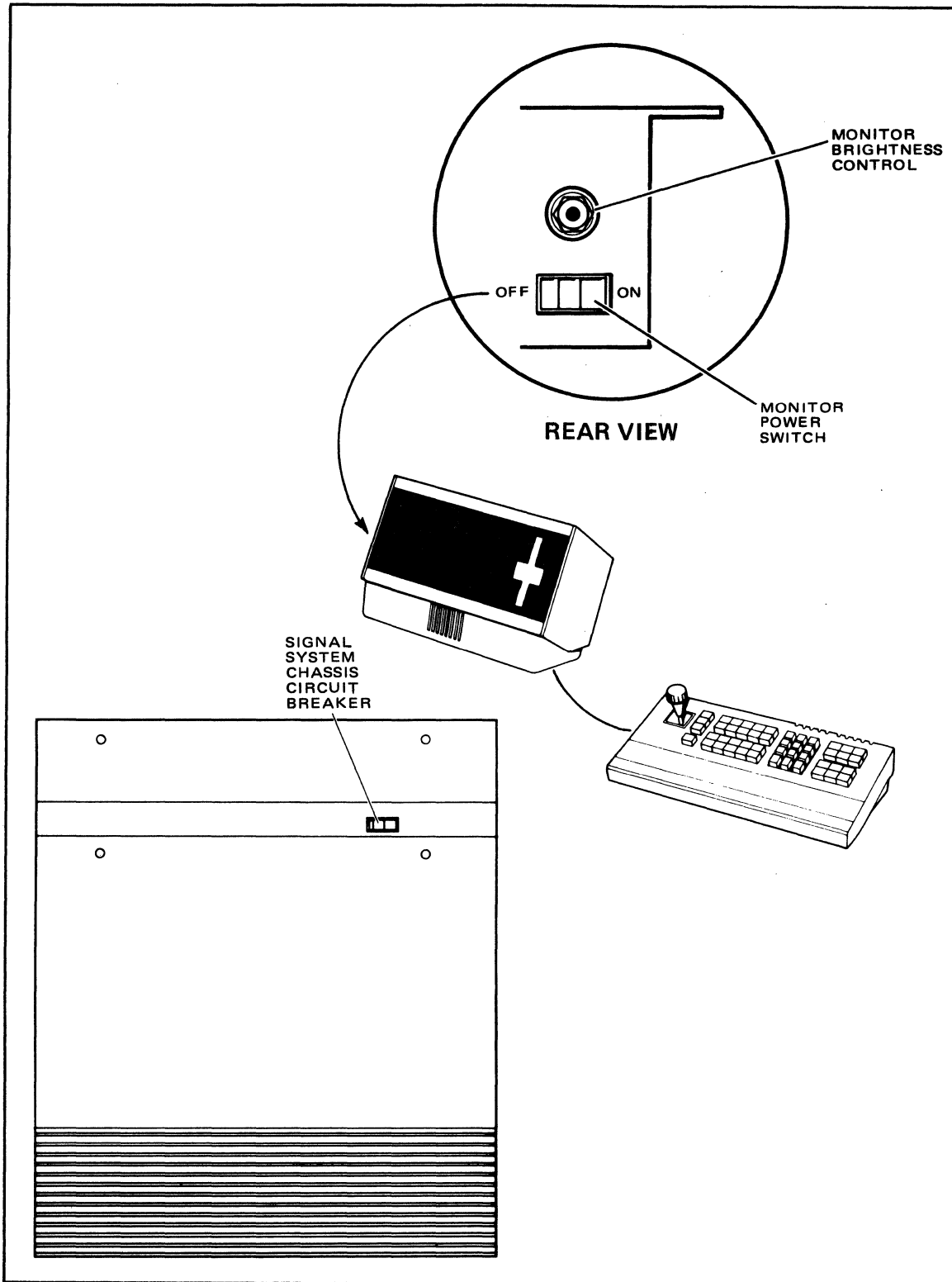


Figure 3-2. Power Switch Locations

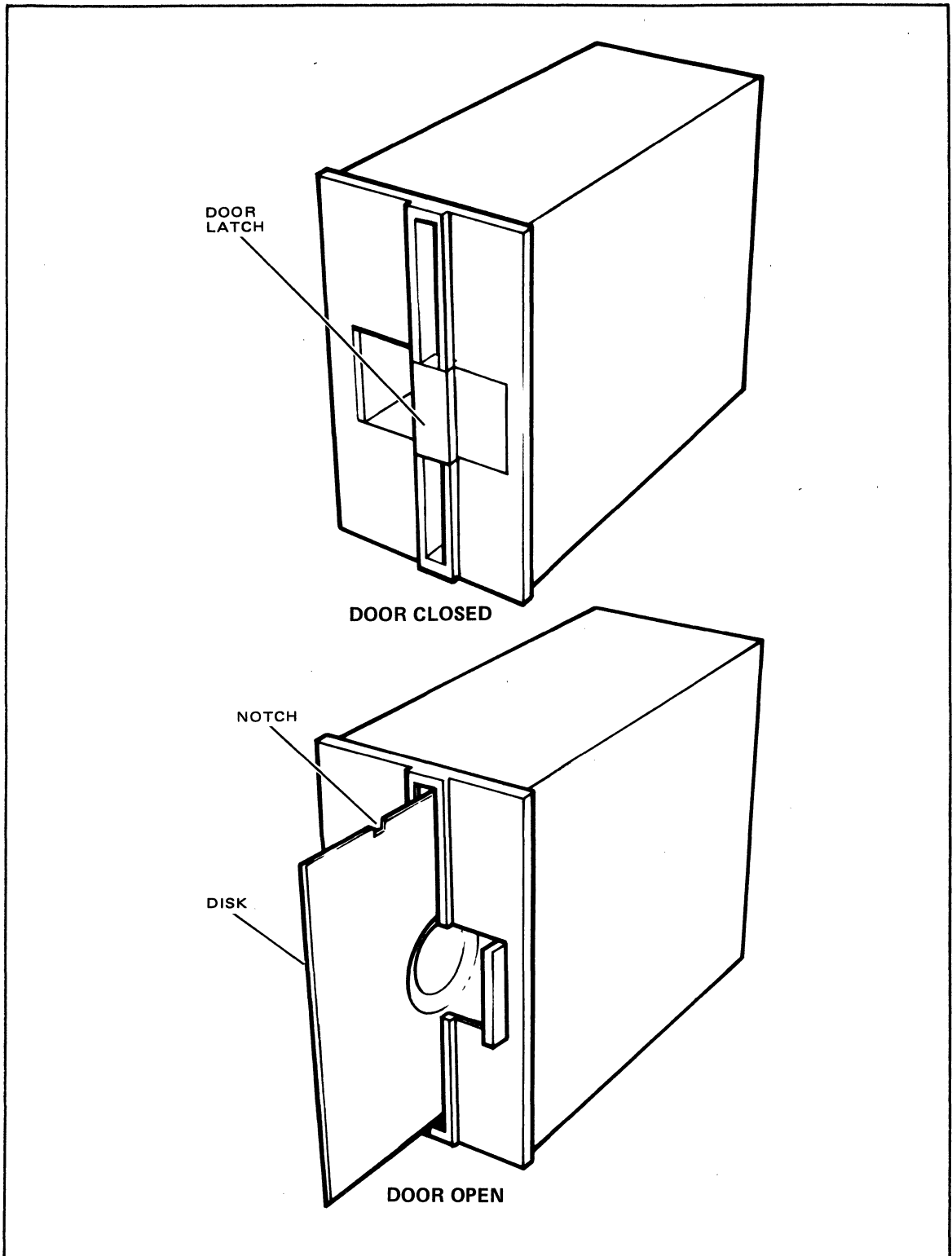


Figure 3-3. Loading Disk Drive

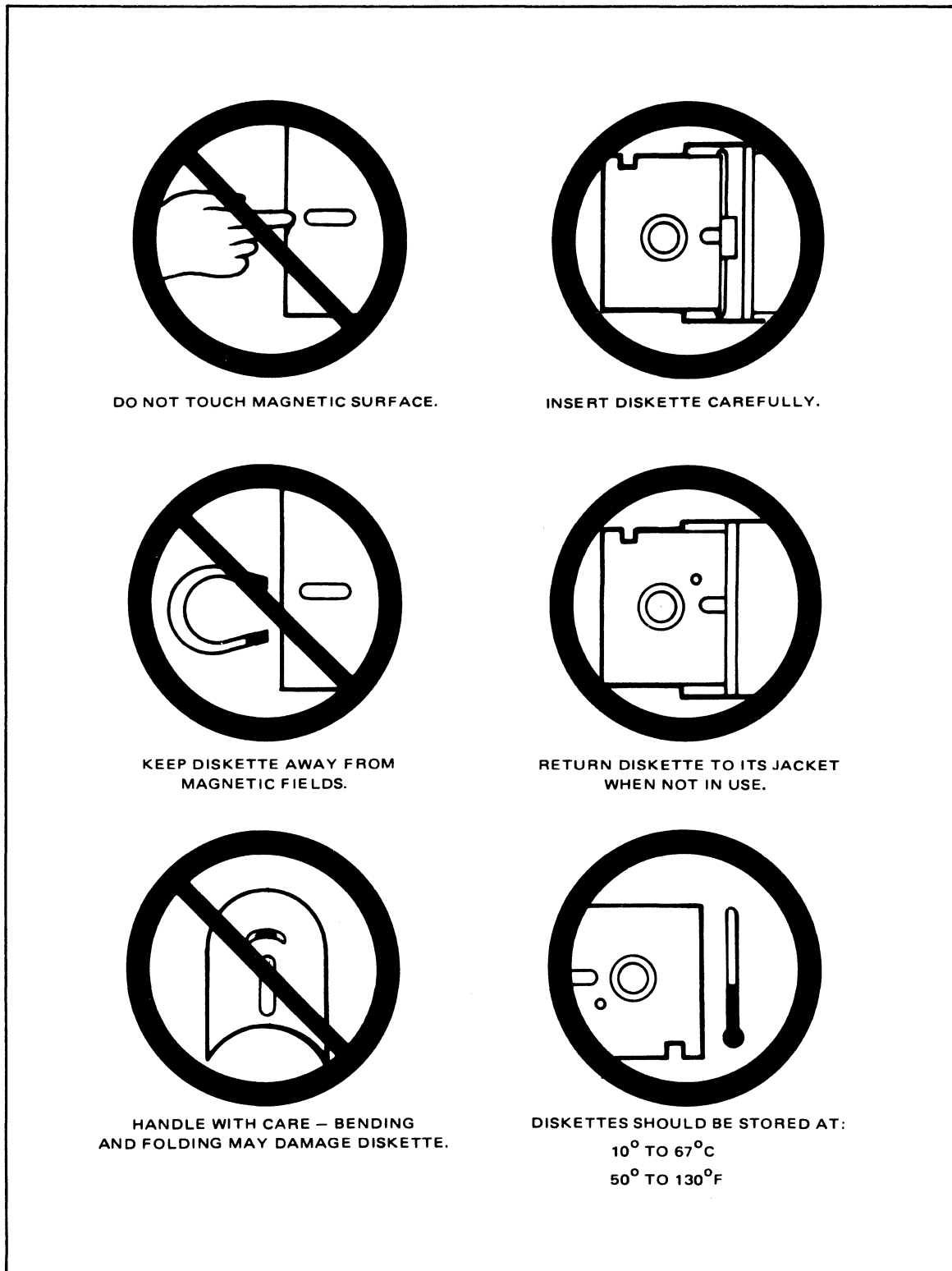


Figure 3-4. Diskette Handling and Care

SECTION 4

MAINTENANCE

4-1 INTRODUCTION

This section contains information on test equipment, circuit breakers, fuses, disassembly, adjustments, and troubleshooting.

4-2 TEST EQUIPMENT

Table 4-1 lists standard test equipment used for adjusting and troubleshooting the ADO System. Additional, optional, equipment is described in the adjustment and troubleshooting discussions.

Table 4-1. Typical Test Equipment

Item	Description	Type
1	Multimeter	Volt-ohmmeter
2	Oscilloscope	Dual Channel, 150 MHz
3	Signal Source	Color Bar Generator
4	Waveform Monitor	Tektronix 1485R or equivalent
5	Vectorscope	Tektronix 520A or equivalent
6	Analog Extender	Ampex Part No. 1409899
7	Digital Extender	Ampex Part No. 1409773

4-3 CIRCUIT BREAKERS AND FUSES

Locations of circuit breakers and fuses are shown in Figure 4-1. Table 4-2 describes and identifies the fuses and circuit breakers. The circuit breaker on the signal system chassis front panel has two trip mechanisms. One trips on excessive analog section current, and the other trips on excessive digital section current. The LED indicator in the circuit breaker is powered by the 5-Vdc digital section power supply. Circuit breakers and fuses differ in some respects for early NTSC models; Table 4-1 of the -02 version of this manual presents this information.

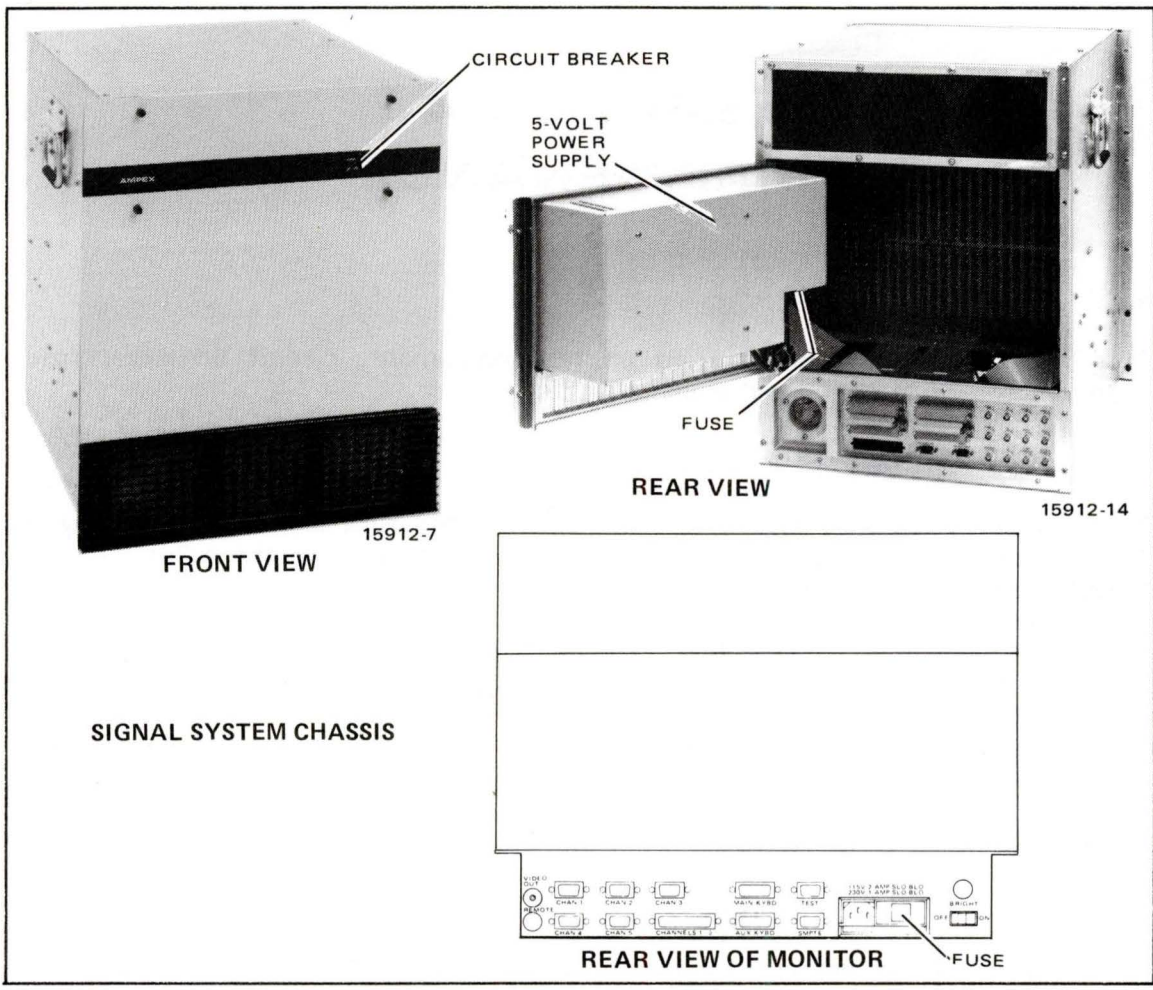


Figure 4-1. Circuit Breaker and Fuse Locations

Table 4-2. Circuit Breakers and Fuses

Item	Description	Function
1	Dual CB (115V), 20A/2.5A	20A for digital section; 2.5A for analog section
2	1.5A Slo Blo (115V)	Analog supply 0.8A Slo Blo (230V)
3	20A CB Type 3AB (115V)	+5 Vdc supply for 15A CB (230V) digital section
4	2A Slo Blo (115V) 1A Slo Blo (230A)	CRT monitor and keyboard

4-4 ACCESS AND DISASSEMBLY

Figure 4-2 shows the front and rear views of the ADO signal system chassis equipment doors and panels used for access. All PWAs are accessed from the front of the equipment without tools (Figure 4-2). All other equipment except the circuit breaker can be disassembled while the unit is installed in a rack cabinet.

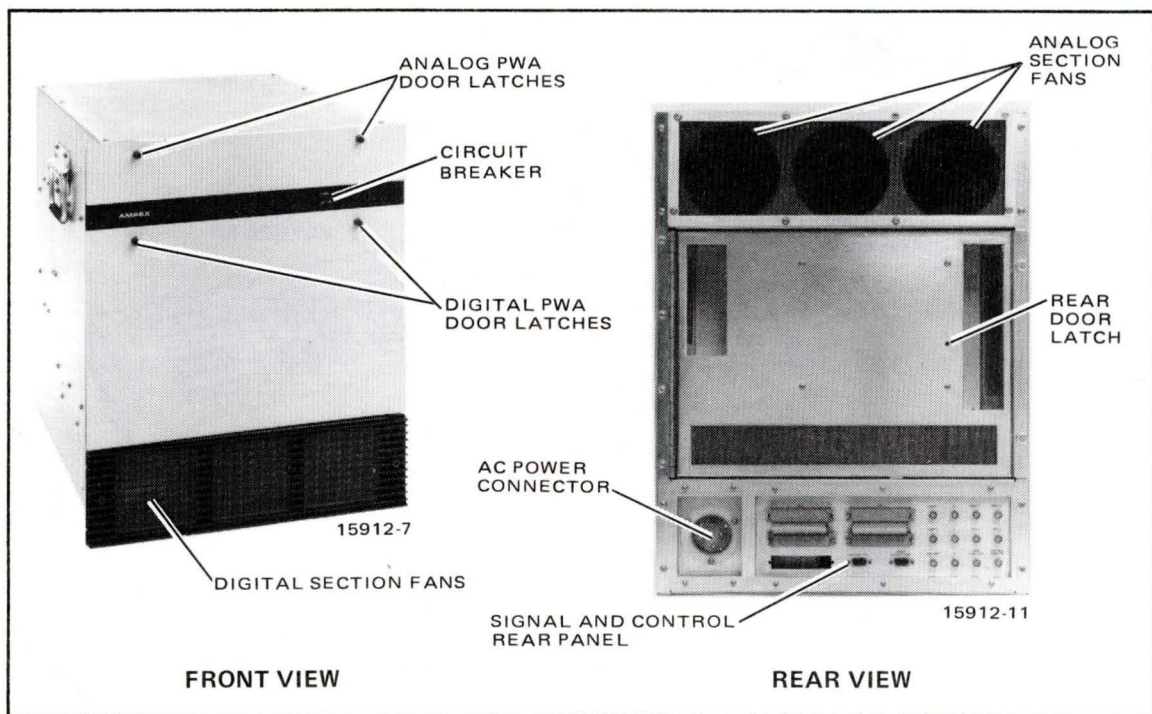


Figure 4-2. Signal System Chassis Identification

Figure 4-3 shows the ADO control unit, consisting of the CRT monitor and the keyboard. Access to interior PWAs and assemblies requires disassembly of their housings. It is possible to replace keyboard lamps without disassembling the keyboard.

Access and disassembly information for all units is given in the following paragraphs.

4-5 Analog Section Electronics

The analog section electronics is located in the top portion of the signal system chassis. Included are six PWAs, power supplies, and a fan assembly.

4-6 Analog Section PWAs

For access to analog PWAs proceed as follows:

STEP 1 Turn off ac power.

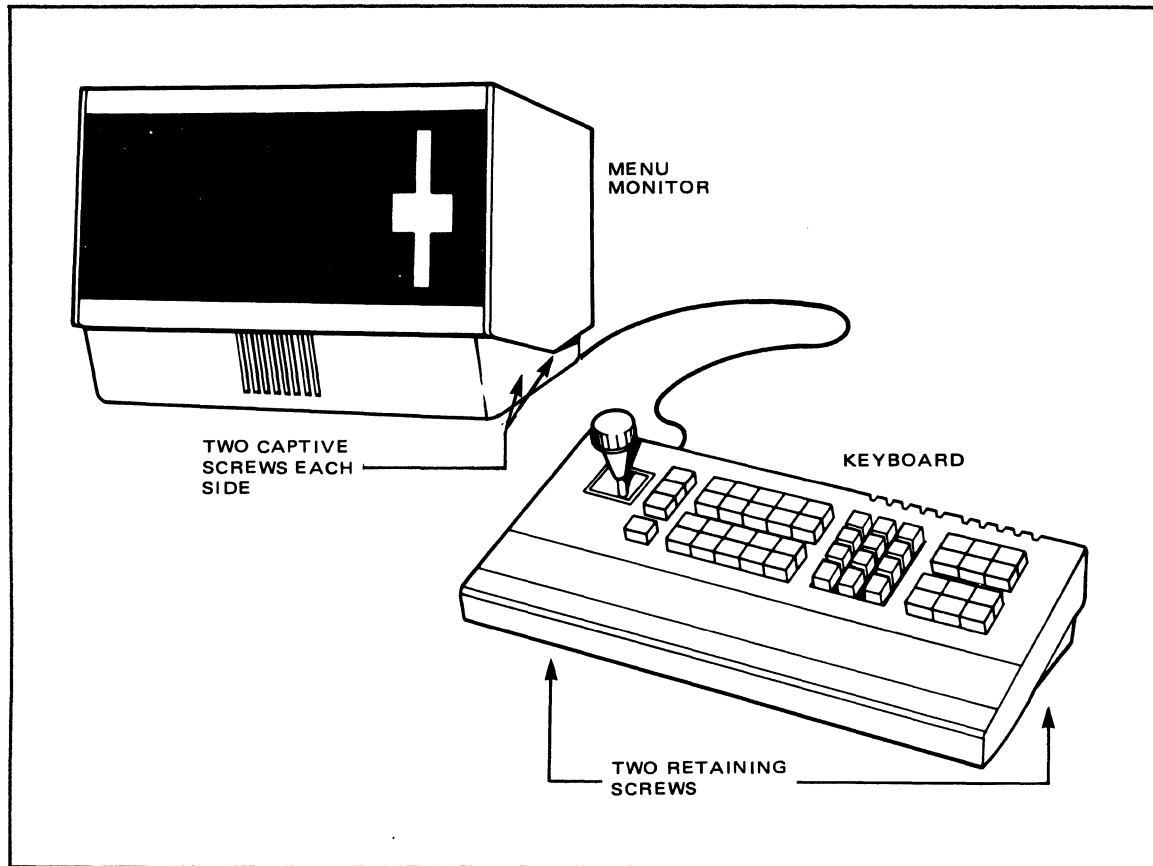


Figure 4-3. Control Unit Assemblies

STEP 2 Loosen two retaining screws (captive) and lower cover door. (See Figure 4-4.)

STEP 3 Use extractor handles to remove PWA.

STEP 4 For troubleshooting, use extender card no. 1409899.

4-7 Analog Section Fans

To remove or replace the analog section fans (Figure 4-5), proceed as follows:

STEP 1 Disconnect power plug.

STEP 2 Open rear door wide.

STEP 3 Remove 7 screws securing rear fan assembly to chassis.

STEP 4 If necessary, remove the screw holding cable clamp on the right and place unit on top of cabinet or other surface. The attached cord is long enough to permit setting unit on top of cabinet.

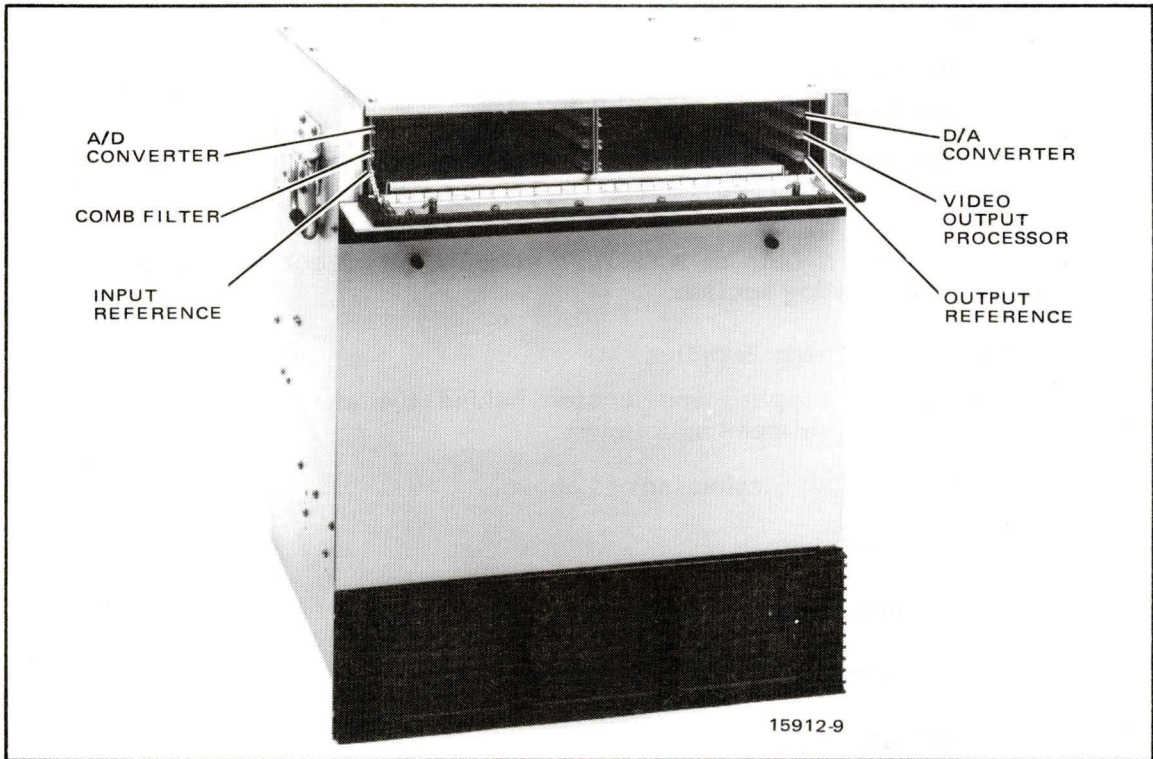


Figure 4-4. Analog Section PWAs

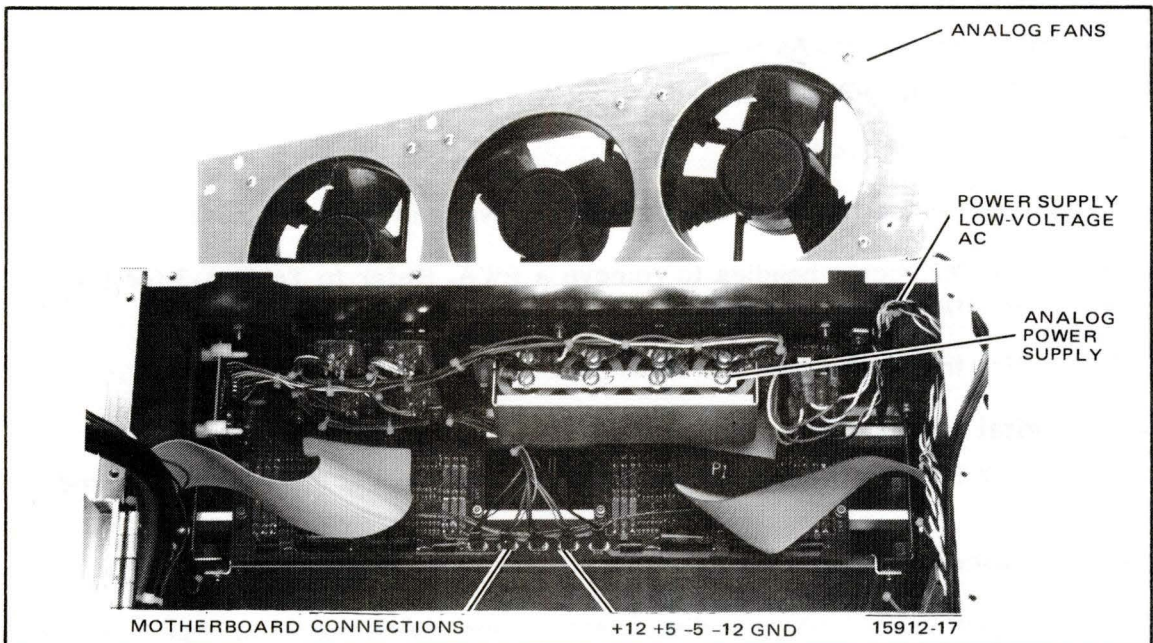


Figure 4-5. Analog Section Fans and Power Supply

ADO

STEP 5 To remove an individual fan:

- a. Unplug fan.
- b. Clip ties holding ac cable as required.
- c. Remove the four screws securing fan to rear panel.

Note

When replacing a fan, be sure it is oriented to direct the airflow outward from analog section.

4-8 Analog Section Power Supplies

Analog section power supplies are located behind the analog section fans (see Figure 4-5). To remove, proceed as follows:

- STEP 1 Remove analog section fans as above.
- STEP 2 Unplug lower power ac.
- STEP 3 Disconnect dc clips: +5, +12, -5, -12, and GND.
- STEP 4 Remove the six nuts holding the unit.

4-9 Digital Section Electronics

The digital section electronics occupies the lower section of the signal system chassis. The lower section accommodates space for 27 PWAs, an ac distribution and power supply assembly, a +5 volt power supply, and digital section fans.

4-10 Digital Section PWAs

For access to digital PWAs, proceed as follows:

- STEP 1 Turn off ac power.
- STEP 2 Loosen the two retaining screws (captive) and lower the cover door.
- STEP 3 Use extractor handles to remove a PWA. Refer to Table 4-3 for PWA locations.
- STEP 4 For troubleshooting use extender card no. 1409773.

4-11 Digital Section Fans

To remove or replace the digital section fans, refer to Figure 4-6 and proceed as follows:

- STEP 1 Disconnect power plug.
- STEP 2 Open rear door and disconnect power connections to fan assembly. Connections are 9 (hot) and 4 (neutral) on the terminal strip. See Figure 4-7. Disconnect both pair.

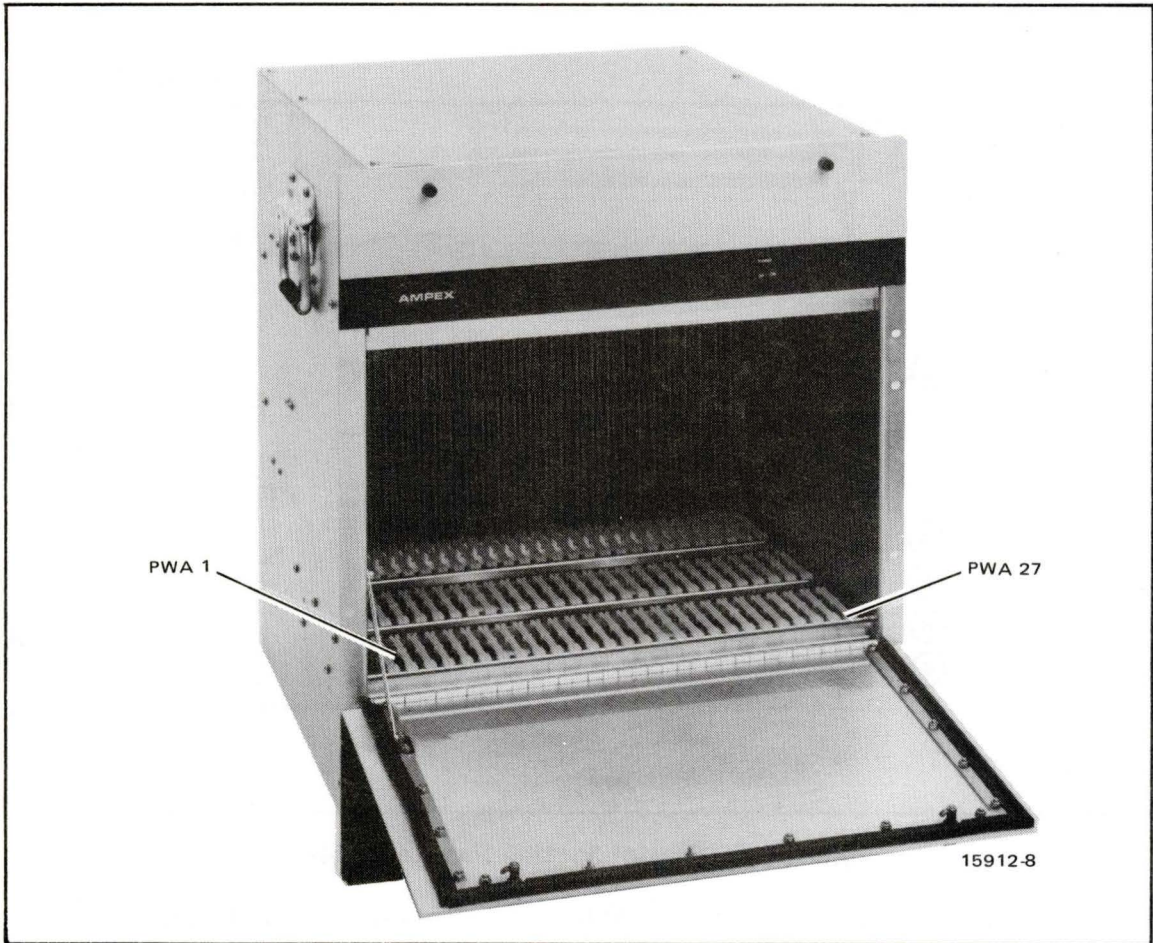


Table 4-3. Digital Electronics PWA Locations

PWA	Name	PWA	Name
1	Input Control PWA	15	Output Control PWA
2	Y Memory PWA	16	Y Memory PWA
3	Y Memory PWA	17	Y Memory PWA
4	Y Memory PWA	18	Color Processor PWA
5	Y Memory PWA	19	Chroma/Key Memory PWA
6	Y Memory PWA	20	Coefficient Store PWA
7	Color Processor PWA	21	Interpolator PWA
8	Chroma/Key Memory PWA	22	H Processor PWA
9	Coefficient Store PWA	23	Key Processor Horizontal PWA
10	Interpolator PWA	24	Add Generator PWA
11	V Processor PWA	25	Not Used
12	Key Processor Vertical PWA	26	Low-Level Controller PWA
13	Add Generator PWA	27	High-Level Controller PWA
14	Not Used		

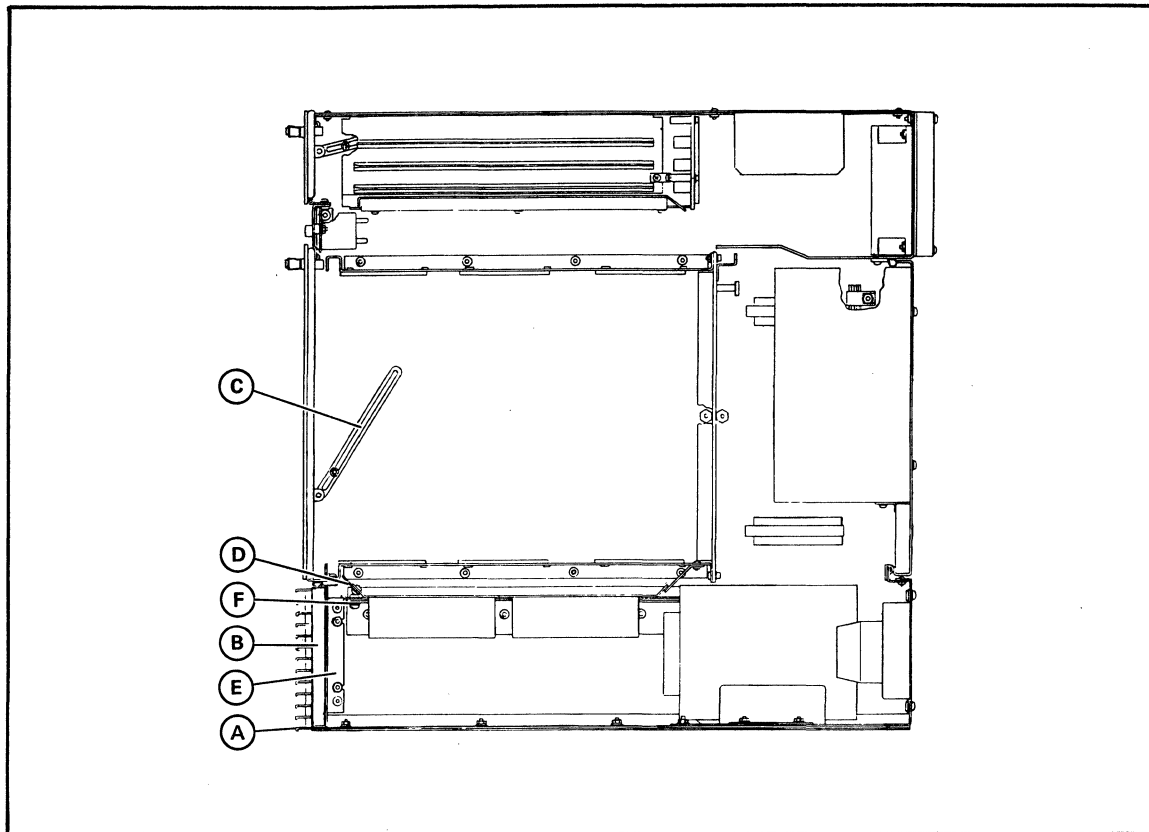


Figure 4-6. Digital Section Fan Assembly

- STEP 3 Remove grill (A) and filter (B) from the front of digital section.
- STEP 4 Remove front door by removing door support (C) and all screws securing door hinge to chassis.
- STEP 5 Remove the four screws holding the baffle strip.
- STEP 6 Loosen two nuts that secure slotted portions of each filter bracket (E) and remove brackets.
- STEP 7 Remove four screws that secure fan assembly (one at each corner of the assembly).
- STEP 8 Slide assembly forward and out of the front of the cabinet.
- STEP 9 Place assembly face down on a workbench.
- STEP 10 Unplug fan to be removed.
- STEP 11 Use a hex socket wrench through holes in the front of the fan to remove securing screws.

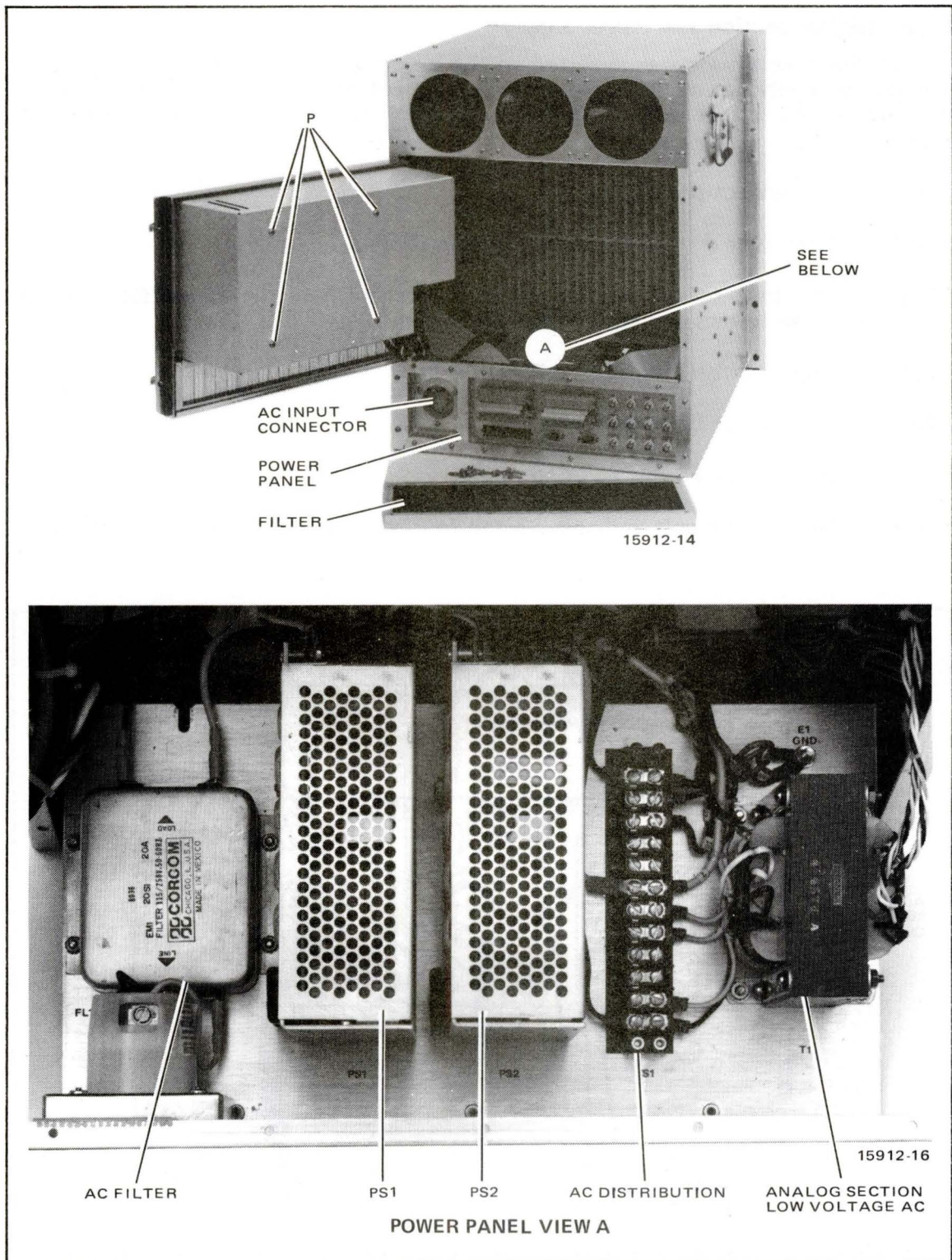


Figure 4-7. Power Panel

ADO

4-12 Digital Section +5V Power Supply

The +5 Vdc power supply is mounted on the inside of the rear door of the cabinet. The power supply has a self-contained fan. A sheet metal cover is used to control air flow in and out of slots in the door. To remove the power supply proceed as follows:

- STEP 1 Disconnect power plug.
- STEP 2 Open rear door of the signal system chassis.
- STEP 3 The four screws marked (P) in Figure 4-7 hold the air baffle. Remove these screws and remove the air baffle.
- STEP 4 Unplug sense plug J1 (see Figure 4-8).
- STEP 5 Disconnect three ac wires.
- STEP 6 Disconnect +5 volt and GND wires.
- STEP 7 Support the unit and remove the four screws in the rear door holding the unit.

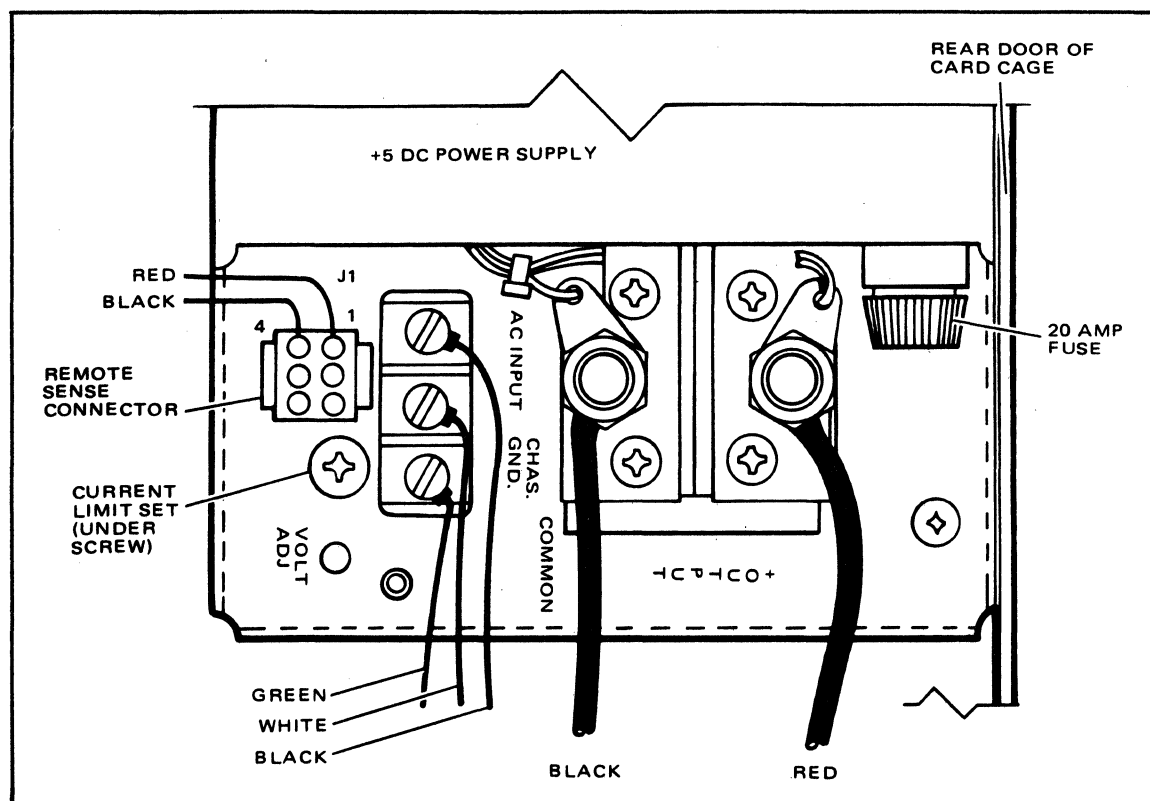


Figure 4-8. Digital +5V Power Supply

4-13 Rear Connector Panel Removal

The rear connector panel can be separated into two units: the ac power chassis and the signal and control connector panel. To remove the rear connector panel, proceed as follows (see Figure 4-4):

- STEP 1 Disconnect power plug.
- STEP 2 Open rear door.
- STEP 3 Remove screws marked (A) in Figure 4-9.
- STEP 4 Slide chassis about 1 inch to rear for access to interior connections.
- STEP 5 Disconnect connections to front panel circuit breaker.
 - a. Unplug black wire from ac filter.
 - b. Disconnect the two hot connections and the LED connections from the barrier strip.
- STEP 6 Disconnect the two red and two black wires connected to the digital motherboard.
- STEP 7 Unplug the low ac voltage to analog power supply.
- STEP 8 Remove screws marked (B) in Figure 4-9.
- STEP 9 Move connector panel to right and up out of the way while removing ac power chassis.

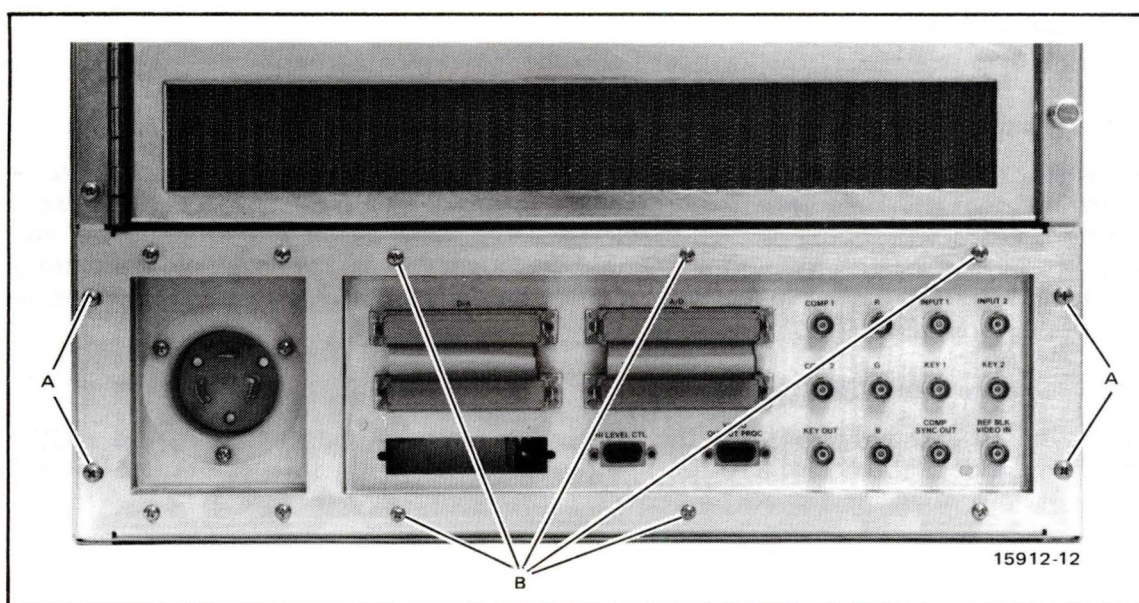


Figure 4-9. Rear Connector Panel Removal

ADO

4-14 Circuit Breaker Panel

If the ADO System card cage is mounted in an enclosed rack or cabinet, it is necessary to remove the signal system chassis from the enclosure to gain access to the circuit breaker panel mounting screws.

- STEP 1 Remove two screws holding circuit breaker panel from each side of card cage.
- STEP 2 Slide panel forward to gain access to wiring.
- STEP 3 See Figure 4-10 for wire identification.

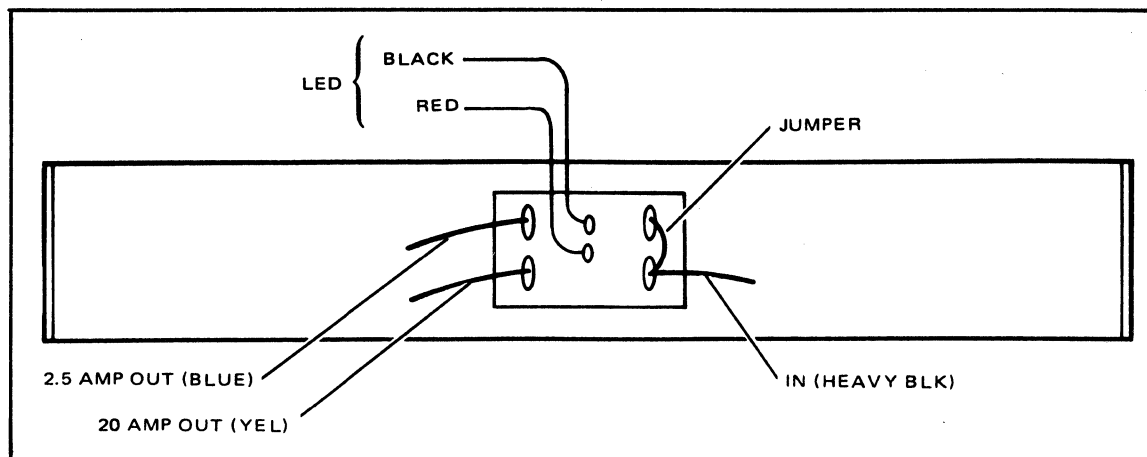


Figure 4-10. Rear View of Circuit Breaker Panel

4-15 Control Unit

The control unit includes the keyboard and the menu monitor unit.

4-16 Lamp Replacement

To replace a lamp in the keyboard, remove the key cap, insert (name), and key, by pulling straight up. Take care not to lose the insert, which is a separate part. Use a piece of 7/32-inch tubing or some self-adhesive tape as an aid in removing the lamp. Remove the lamp by pulling straight up (Figure 4-11). For replacement use a new lamp type 7378. The leads may have to be bent slightly to provide friction to hold the lamp in place.

4-17 Keyboard Disassembly

The keyboard assembly contains the joystick, a Switch Mounting PWA, and a CPU PWA. For access to the interior of the keyboard assembly, turn the unit over and remove two screws and the bottom cover. To remove PWAs (Figure 4-12):

- STEP 1 Unplug J1, J2, and J3.
- STEP 2 Remove the two screws marked (V). The bracket marked (W) can now be removed.

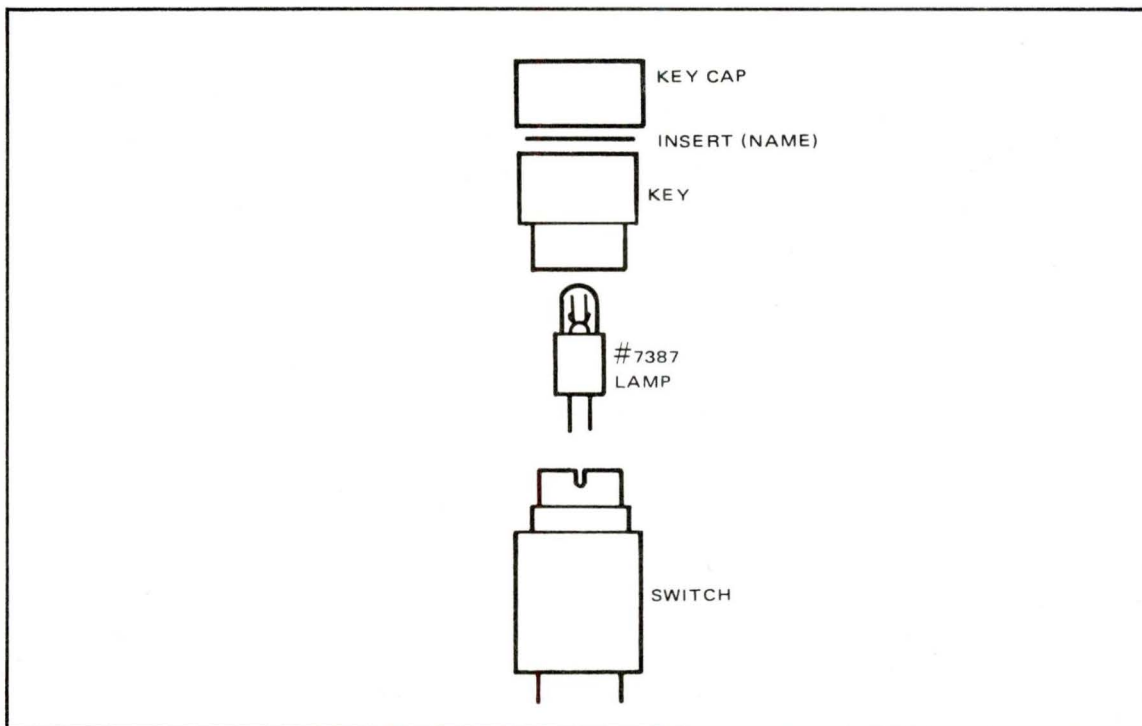


Figure 4-11. Keyboard Switch Assembly

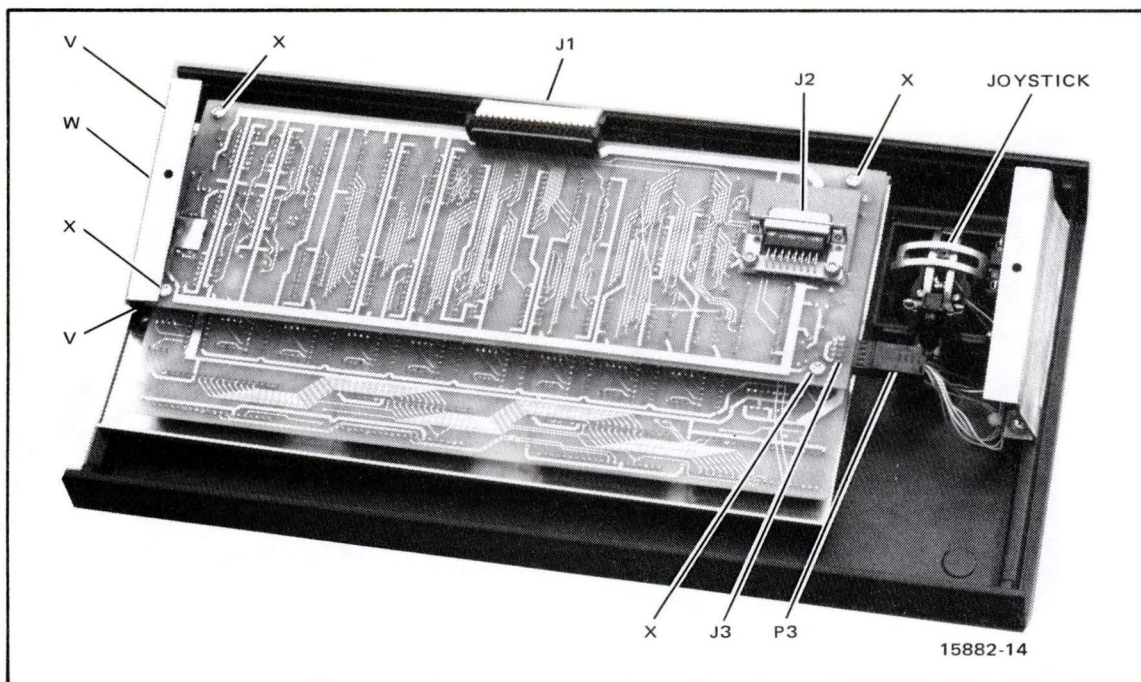


Figure 4-12. Keyboard Bottom View

ADO

- STEP 3 Remove the four screws marked (X). The CPU PWA can now be lifted free of the assembly.
- STEP 4 To gain access to the component side of the keyboard switch mounting PWA, remove the eight screws marked (Y) and unscrew the two spacers marked (Z) (Figure 4-13).

4-18 Joystick Disassembly

For individual replacement parts, refer to vendor information in Appendix B of this manual.

- STEP 1 For access to the underside of the joystick, see the keyboard disassembly for removal of the bottom cover (paragraph 4-17).
- STEP 2 Loosen the setscrew holding the knob and remove the knob (Figure 4-14).
- STEP 3 Remove the two butterfly plates, spring, and nylon washer assembly.
- STEP 4 Loosen the setscrew holding the collar. Carefully guide the slack in the Z-axis wires up through the stick while lifting the Z-axis potentiometer for access to the solder connections.
- STEP 5 Unsolder the connections and remove the Z-axis potentiometer.
- STEP 6 Loosen the hollow stick setscrew and remove the pot housing.

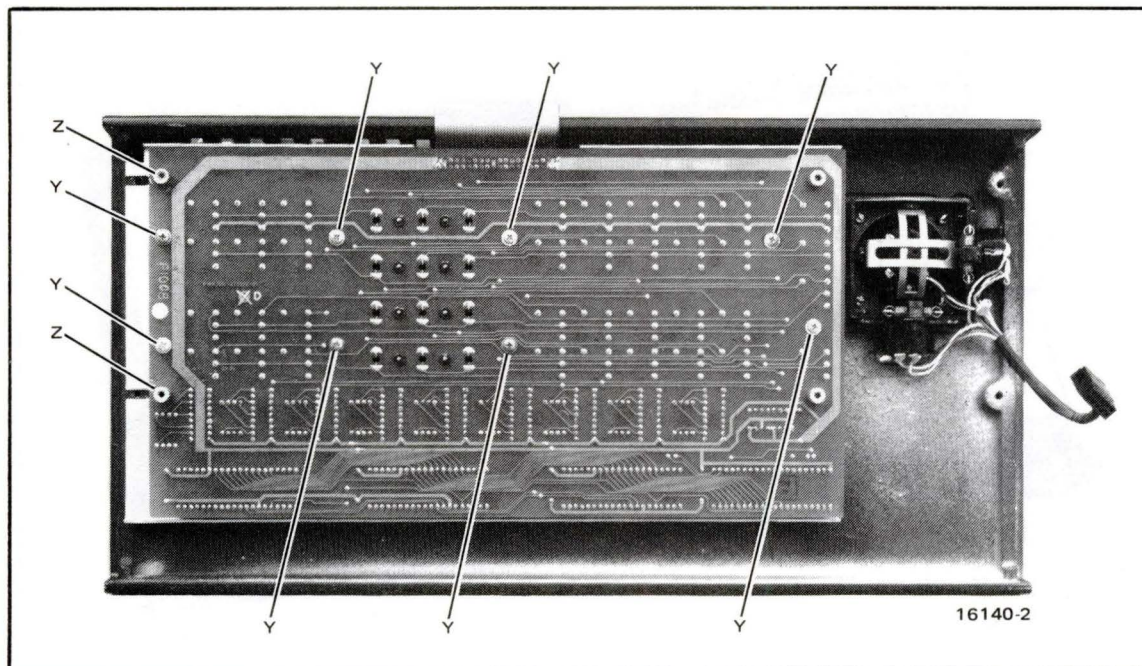


Figure 4-13. Keyboard Internal Assembly

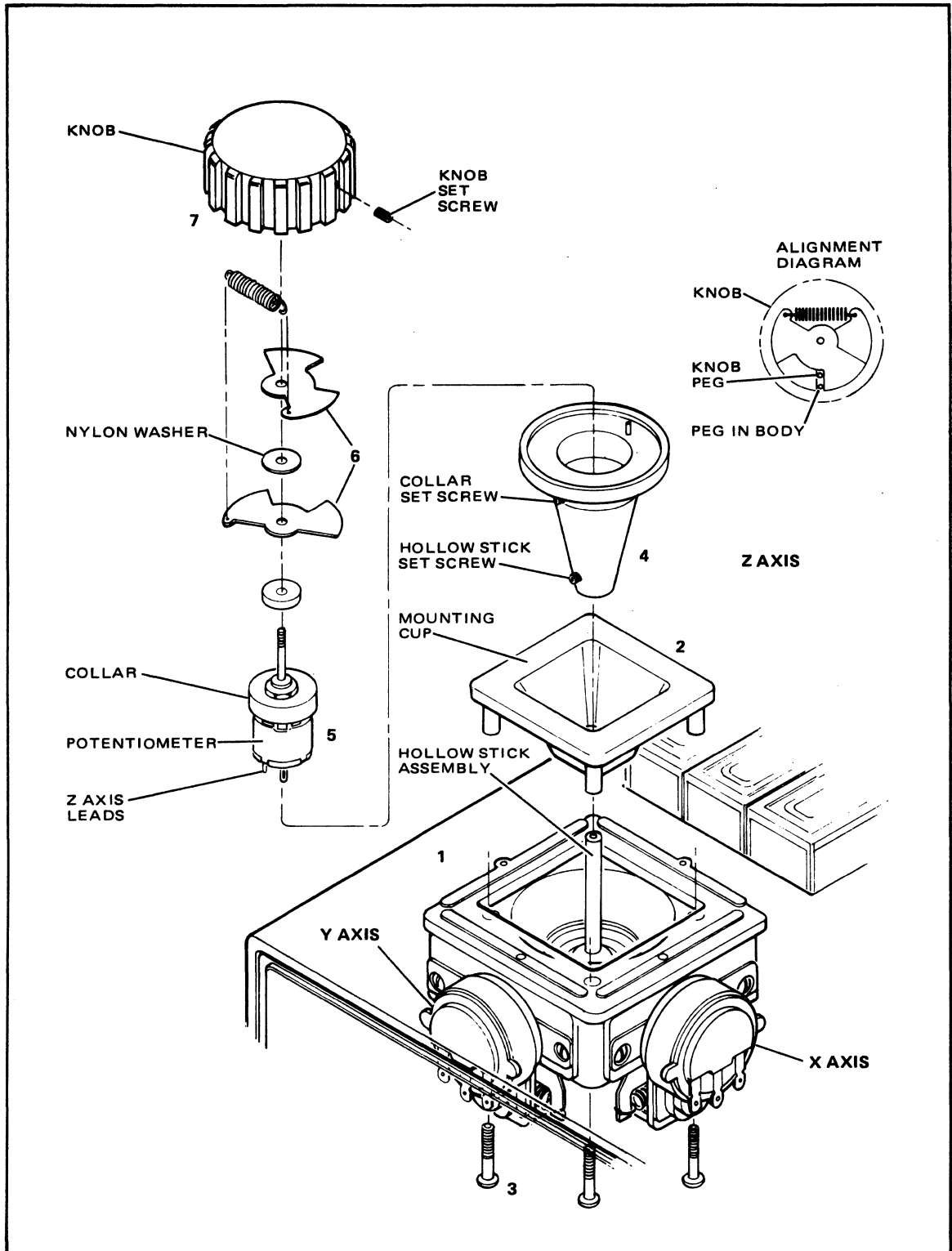


Figure 4-14. Joystick Assembly

ADO

STEP 7 Unsolder the X-axis and Y-axis potentiometers.

STEP 8 Remove the four mounting screws which release the mounting cup and gimbal mechanism.

4-19 Menu Monitor Disassembly

The menu monitor includes the following subassemblies: display CRT, disk drive, power supply, Control Processor PWA (CPP), I/O PWA, Control Interface PWA (rear panel connectors), and chassis assembly. To obtain access to the display CRT, disk drive, and power supply subassemblies, loosen two captive screws on each side of the housing (refer to Figure 4-3) and lift the cover off.

WARNING

UNPLUG MONITOR AC POWER BEFORE REMOVING COVER. CRT UNIT HAS HIGH VOLTAGE (ABOUT 13 kV).

4-20 Menu Monitor CRT Removal

To remove the CRT, the CRT and bezel must first be removed as a unit, and then separated. Then perform the following steps:

STEP 1 Unplug PWA connector (A) at rear of CRT (Figure 4-15).

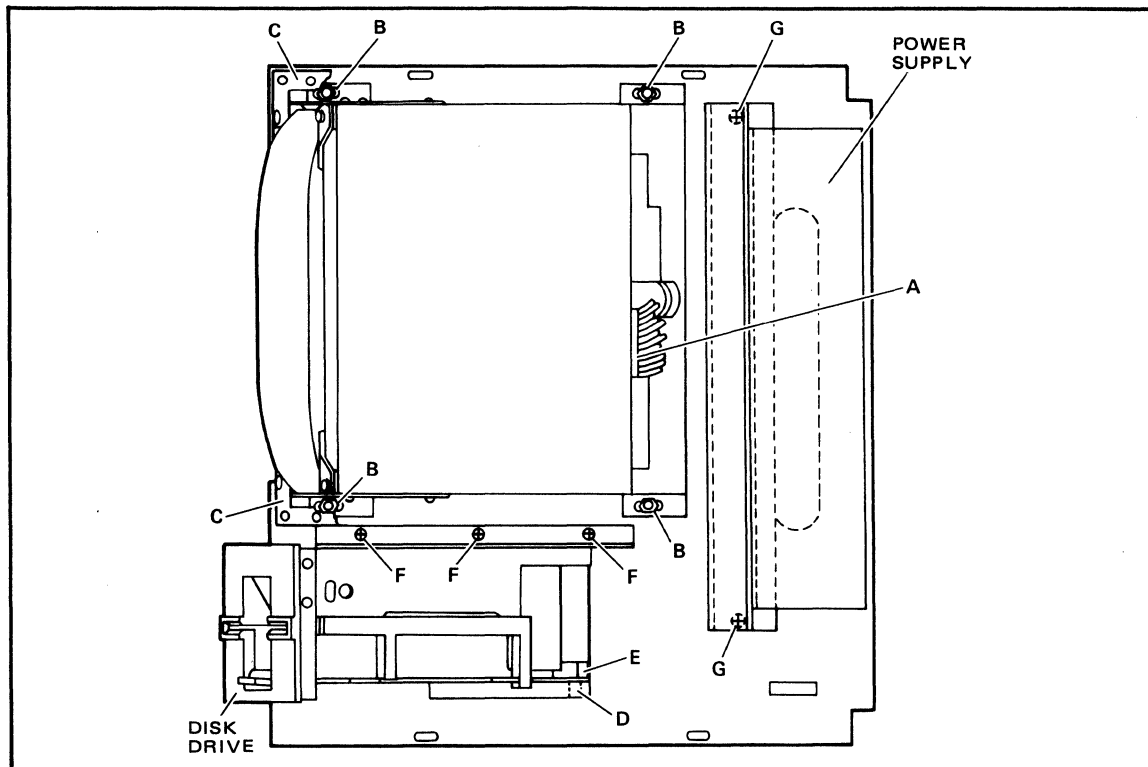


Figure 4-15. Menu Monitor Internal Assemblies (top view)

- STEP 2 Remove two nuts (B) each side.
- STEP 3 Remove entire CRT and bezel unit by lifting and pulling forward.
- STEP 4 Remove bezel from CRT by removing the four screws that secure it to the bezel brackets (C).
- STEP 5 If the CRT assembly is being replaced, transfer the two bezel brackets (C) to the new unit, then attach the bezel.

4-21 Disk Drive Removal

Observe high voltage warning, above. With cover off, remove bezel and CRT (paragraph 4-20 steps 1, 2, and 3). Then perform the following steps (Figure 4-15):

- STEP 1 Unplug PWA ribbon connector (D) and dc power connector (E) at rear of disk drive.
- STEP 2 Remove the three screws (F) securing bracket.
- STEP 3 When installing a new unit, transfer mounting bracket to new unit.
- STEP 4 The line termination in socket 2F and the programmable shunt in socket 1E (see vendor's manual) may have to be transferred to the new unit. The unit as shipped from the factory is configured to operate in a single drive system which is correct for the ADO System.

4-22 Menu Monitor Power Supply Removal

To remove the menu monitor power supply:

- STEP 1 Disconnect the power supply harness.
- STEP 2 Remove the two screws (G) securing the mounting bracket (Figure 4-15).
- STEP 3 If entire power supply is being replaced, transfer mounting bracket to new power supply unit.

4-23 Chassis Assembly Removal

To obtain access to the Control Processor PWA and the I/O PWA, perform the following steps:

- STEP 1 Remove bezel and CRT as a unit (paragraph 4-20, steps 1, 2, and 3).
- STEP 2 Lift chassis assembly from housing base.

4-24 POWER DISTRIBUTION

Figures 4-16 and 4-17 show the ac and dc power distribution for the control unit and for the signal system chassis, respectively. An indicator in the center of the front panel circuit breaker is lighted when the signal system chassis power is on.

ADO

4-25 ELECTRICAL ADJUSTMENTS

Adjustment procedures are given below for the analog and digital sections of the signal system chassis. No adjustments are required for the control unit.

The adjustment procedures for two of the analog PWAs include the use of optional test equipment, the Digital Test Signal Generator, Ampex Part Number 1420458. A description of this equipment is given in paragraphs 4-36 to 4-40.

All jumpers in the analog system PWAs are for factory use only, and are not to be changed in the field. Most of the jumpers are for factory test purposes. Some are for NTSC/PAL selection.

CAUTION

TURN POWER OFF BEFORE INSERTING OR REMOVING SIGNAL SYSTEM CHASSIS PWAS. WHEN USING EXTENDER BOARDS, BE SURE CARD EDGE PINS ARE PROPERLY ALIGNED.

4-26 Analog Section Adjustments

Some analog PWA adjustments are for factory use only and should not be adjusted in the field. The adjustments intended for field use are described below for each analog PWA. Before performing any of these adjustments, make sure that mid-range values are assigned (via the control unit set-up mode) for both Y and chroma.

4-27 Comb Filter PWA

The two field adjustments for this PWA should be done in the sequence given below.

STEP 1 The overall level of the narrowband luminance is adjusted to match the wideband luminance level. To perform this adjustment, proceed as follows:

- a. With power off, remove Comb Filter PWA. Place PWA on an extender and reinstall into card rack. Turn on power.
- b. Apply a split field signal from a color bar generator, 100% saturation, 100 IRE white, to ADO video input. Use connector J15, INPUT 1, located at rear connector panel of the signal system chassis.
- c. Connect a color monitor to video output, COMP 1, connector J10.
- d. Adjust R103 of the comb filter (Figure 4-18) to obtain proper color where Y-I-Q starts in the split field; adjust R103 so there is no black and very little white between color bars in Y-I-Q split field signal.

STEP 2 The comb mesh detector is adjusted to provide switching from wideband Y to narrowband Y as needed to eliminate 3.58 MHz moiré effects. To perform this adjustment, proceed as follows:

- a. With the same test setup as for adjustment 1 (luminance level matching), apply split field signal, 100% saturation, 100 IRE white, to video input, connector J15.

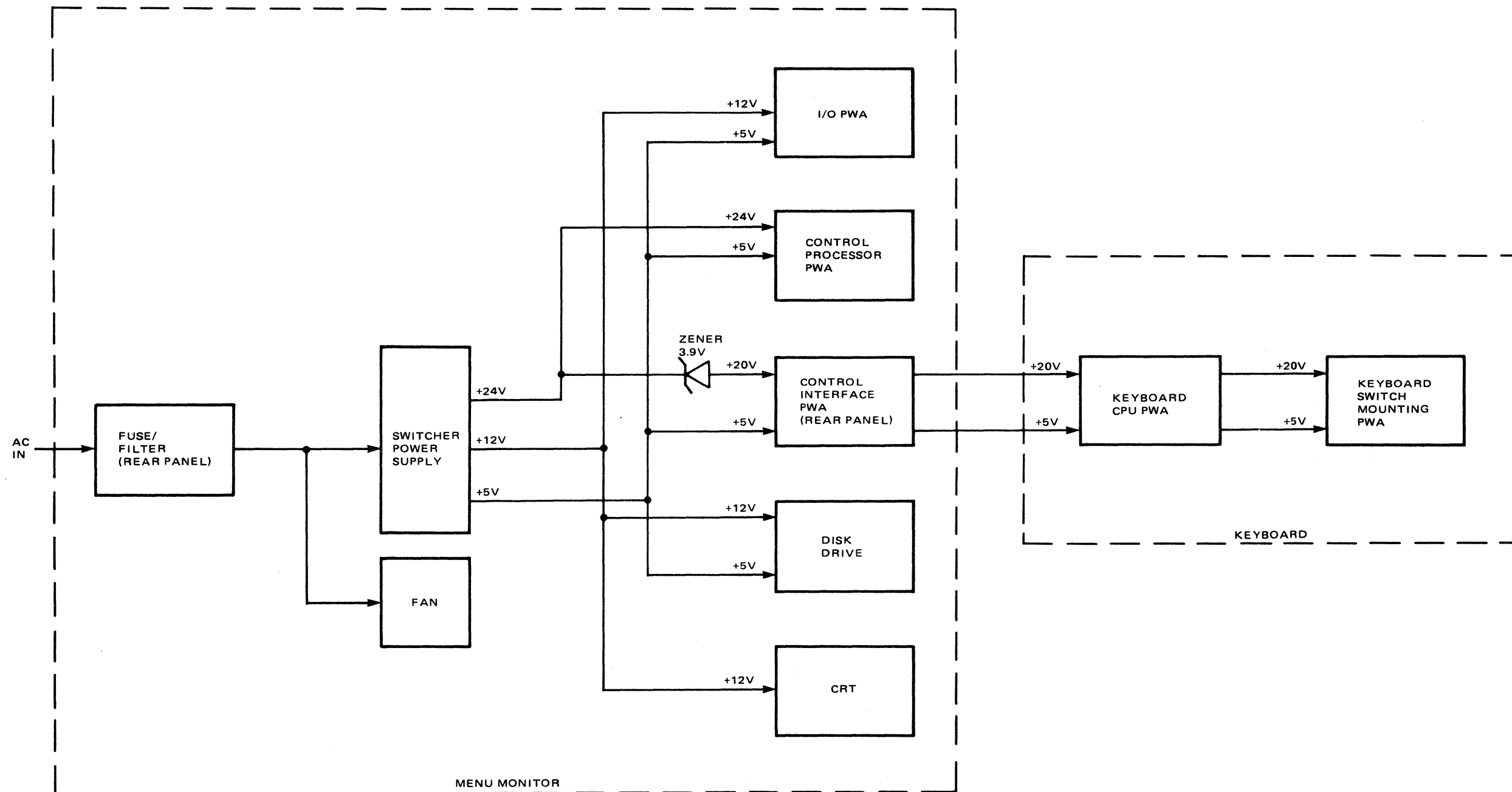


Figure 4-16.
Control Unit Power Distribution

ADO

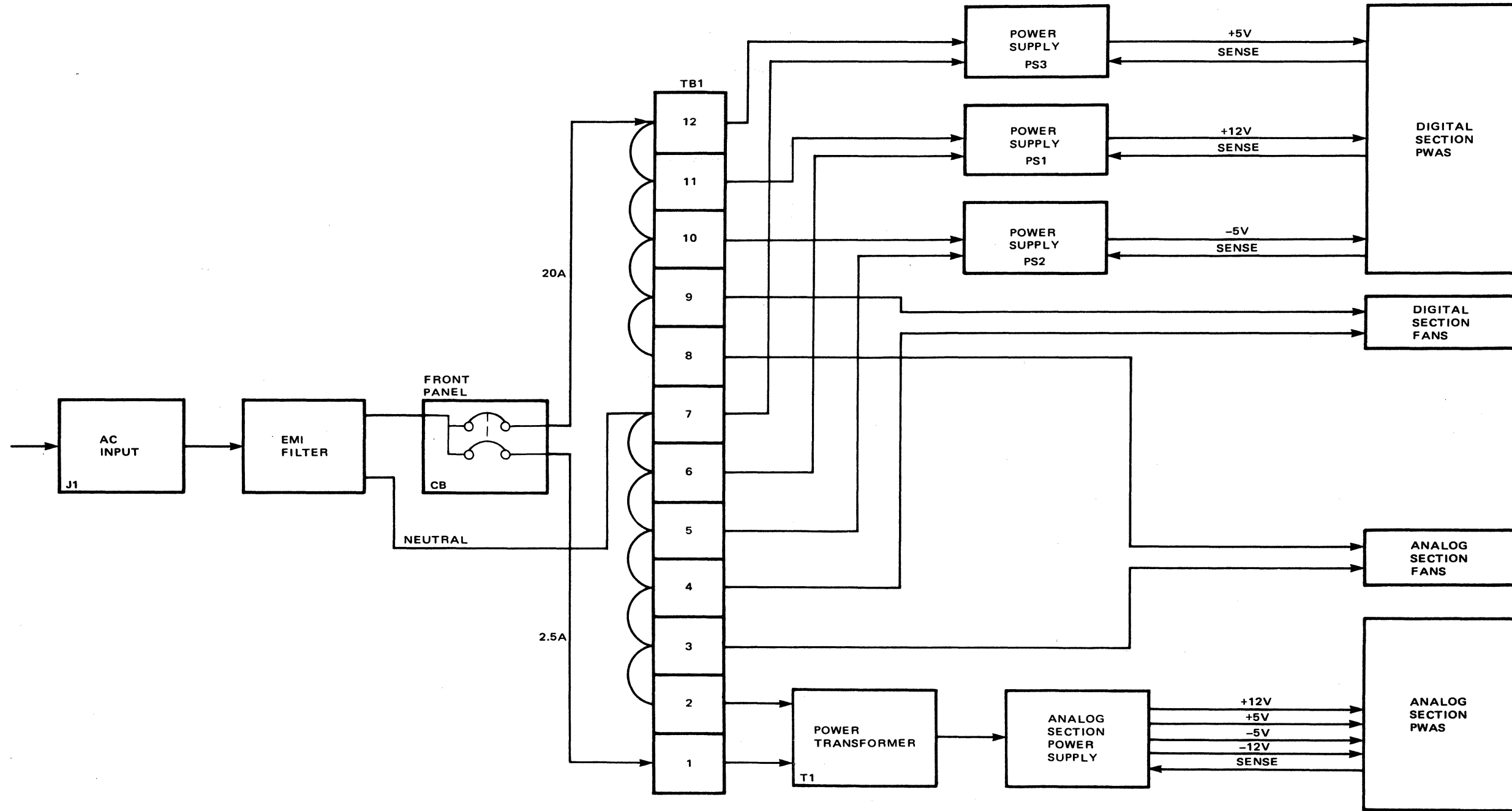


Figure 4-17.
Signal System Chassis Power Distribution

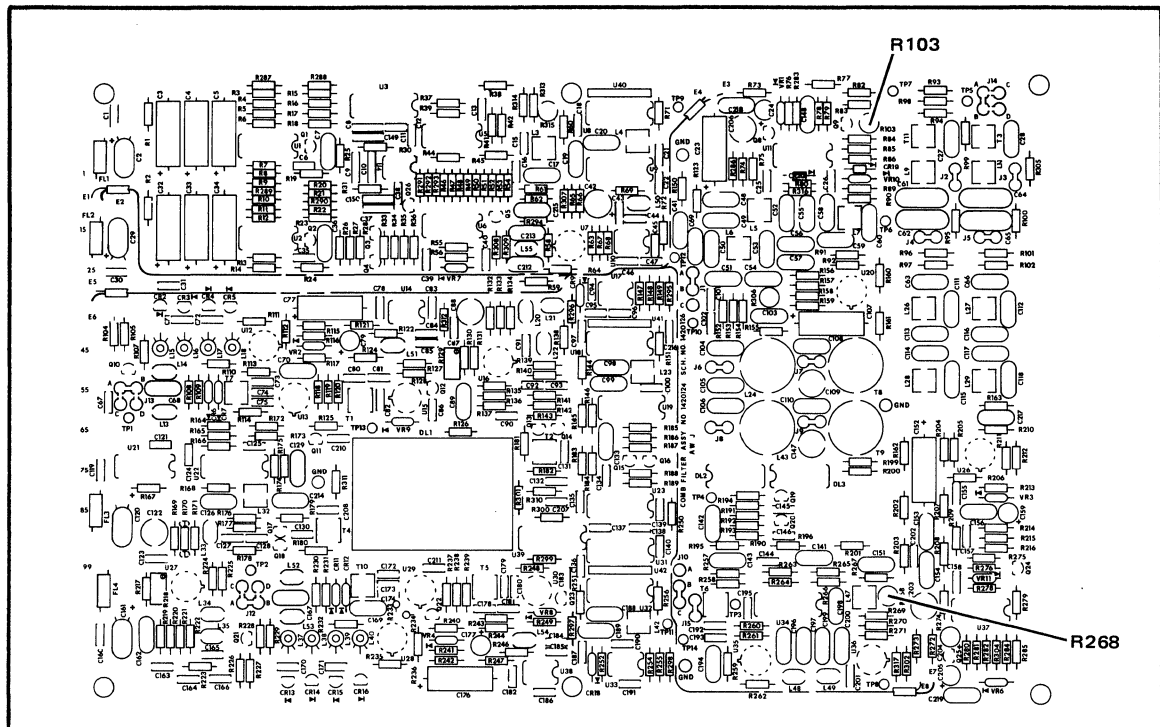


Figure 4-18. Comb Filter PWA

- b. Using ADO control unit, reduce the image slightly and rotate it 45° clockwise. Then enlarge image for best viewing on the color monitor.
- c. Observe jitter in the upper left-hand portion, between beginning of last line of color and Y-I-Q component. Adjust R268 to minimize this jitter. (Also see paragraph 4-31, adjustment number 2.)
- d. With power off, remove PWA and extender and reinstall PWA.

4-28 Input Reference PWA

The two field adjustments for this PWA should be done in the sequence given below.

STEP 1 The R-Y component is adjusted to match the B-Y component. To perform this adjustment, proceed as follows:

- a. With power off, remove Input Reference PWA. Place PWA on an extender and reinstall into card rack. Turn on power.
- b. Apply a full field color bar signal, 100% saturation, 100 IRE white, to the video input, connector J15.
- c. Connect a vectorscope to COMP 1 video output, connector J10.
- d. Regardless of video out level, calibrate vectorscope so the B-Y component is within the target area.

ADO

- e. Adjust R156 on Input Reference PWA (Figure 4-19) so the R-Y component is within the target area.

STEP 2 This adjustment establishes the correct color level (after B-Y and R-Y are matched). Proceed as follows:

- a. With the same test setup as for adjustment 1 (B-Y, R-Y matching), apply full field color bar signal, 100% saturation, 100 IRE white.
- b. Place vectorscope gain adjustment in calibrated position.
- c. Adjust R78 on Input Reference PWA so B and R vectors are again within their target areas.
- d. With power off, remove PWA and extender and reinstall PWA.

4-29 A/D Converter PWA

To adjust the luminance level, proceed as follows:

STEP 1 With power off, remove A/D Converter PWA. Place PWA on an extender and reinstall into card rack. Turn on power.

STEP 2 Apply standard color bar signal (full field or split field), 100% saturation, 100 IRE white, to video input, connector J15.

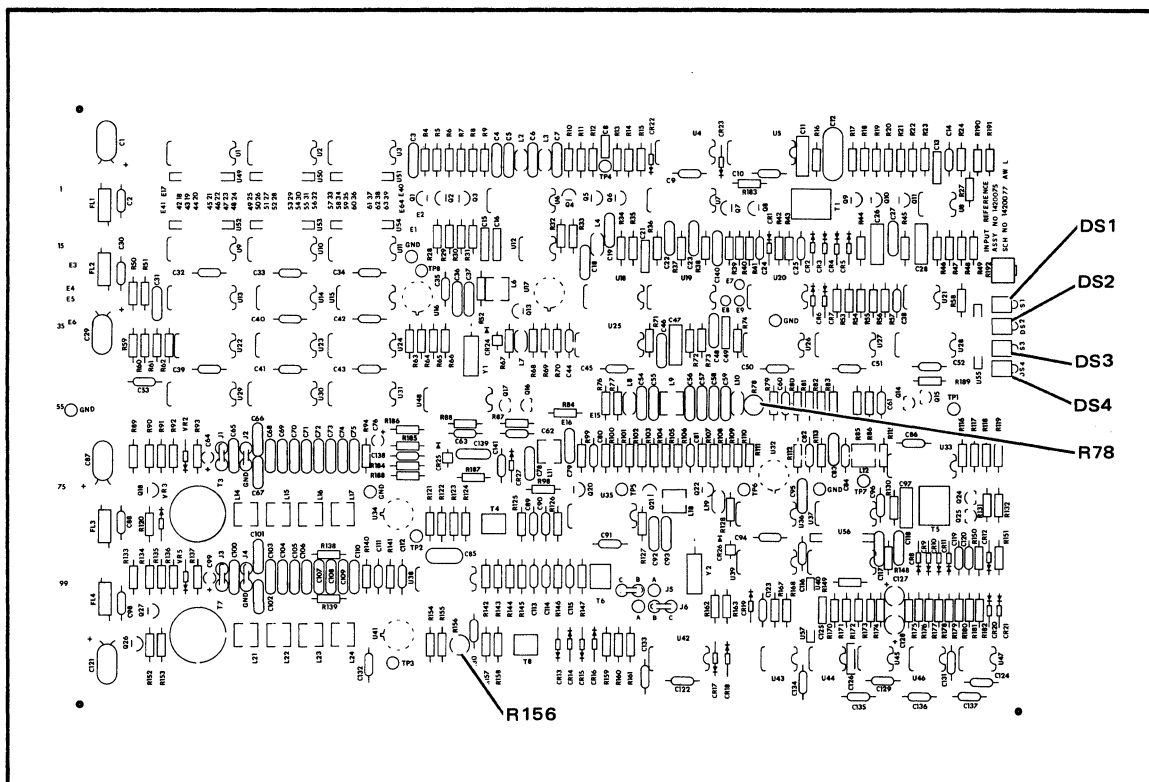


Figure 4-19. Input Reference PWA

- c. On digital test signal generator, set PATT SEL (pattern select) switch to position 2, CHROMA/KEY switch to PATT position, and LUMINANCE switch to PATT position. (This applies horizontally compressed full color bars, 100% saturation, 100 IRE white, with zero pedestal.)
- d. Connect oscilloscope probe to D/A converter R-Y output, pin 40.
- e. Adjust R35 (Figure 4-21) to obtain a 1 Vp-p output at pin 40.

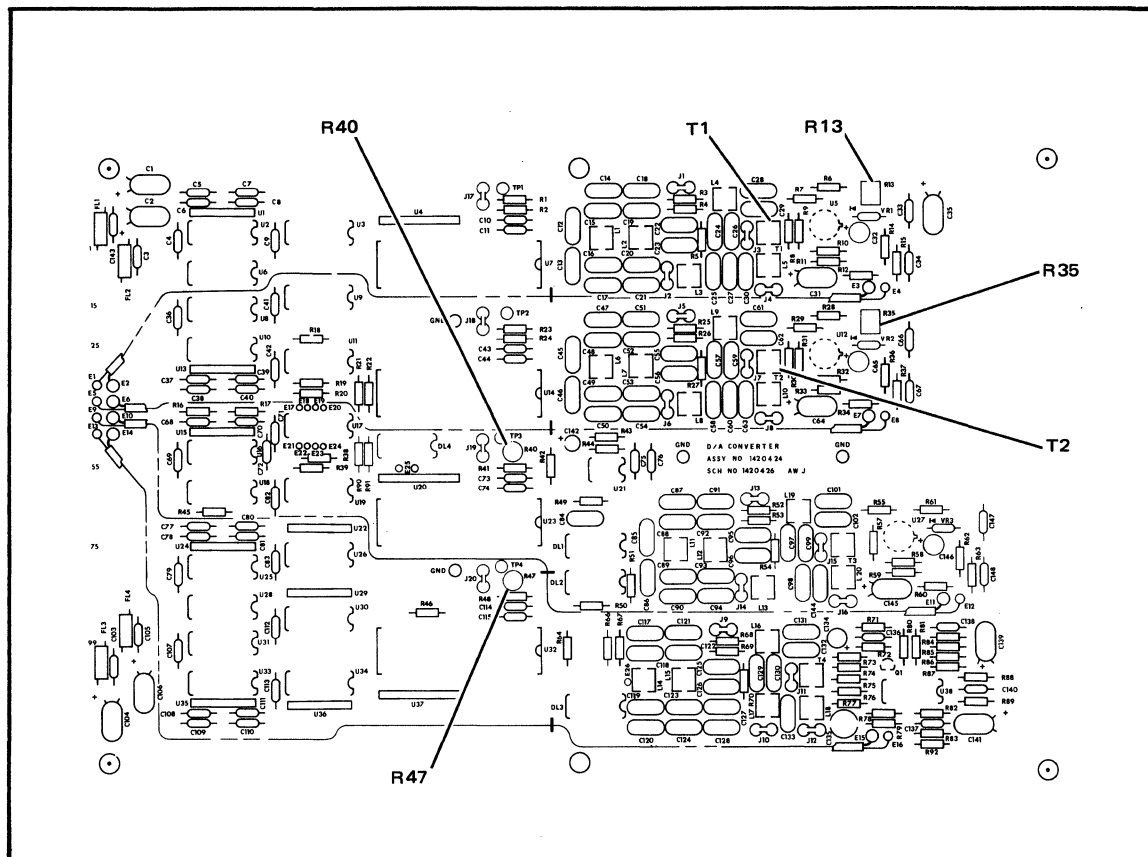


Figure 4-21. D/A Converter PWA

- f. Connect oscilloscope probe to the B-Y output, pin 36, and adjust R13 to obtain a 700 mVp-p output.
- g. On ADO control unit, press SET-UP mode key, to calibrate the SET-UP values.
- h. Connect a vectorscope to the video output, connector J10, and verify that color vectors are within target areas. If they are not, readjust R35 (R-Y) and R13 (B-Y) as needed.
- i. Connect oscilloscope probe to D/A converter key output, pin 44, and adjust R40 to obtain approximately a 900 mVp-p output.

- j. Connect oscilloscope probe to D/A converter luminance output, pin 48, and adjust R47 to obtain approximately a 720 mVp-p output.
- k. Connect waveform monitor to video output, connector J10. Verify that luminance level is 100 IRE after R47 is adjusted. (If it is not, it may be necessary to adjust Video Output Processor PWA first. See paragraph 4-31.)

STEP 2 To adjust the chroma-to-luminance phasing, proceed as follows:

- a. With the digital test signal generator still installed in the A/D converter slot, turn on power. Verify that the test signal switches are in the same position as for adjustment number 1: PATTERN SELECT in position 2, CHROMA/KEY at PATTERN position, and LUMINANCE at PATTERN position.
- b. Connect waveform monitor to video output, connector J10.
- c. Adjust T2 while monitoring the R-Y 20T pulse, to obtain best balance of chroma to Y. (Note that the R-Y and B-Y 20T pulses are not presented at the same amplitude.)
- d. Adjust T1 while monitoring the B-Y 20T pulse, to obtain best balance of chroma to Y.
- e. With power off, remove D/A converter, extender, and digital test signal generator. Reinstall A/D converter and D/A converter.

4-31 Video Output Processor PWA

The Digital Test Signal Generator PWA is used here for chroma/Y mixture and overall signal amplitude adjustments, for 3.58 MHz nulling, and for a chroma 90° phase difference adjustment.

STEP 1 To adjust the chroma-to-Y mixture and overall signal amplitude, proceed as follows:

- a. With power off, remove the Video Output Processor PWA. Place the PWA on an extender card and reinstall into card rack.
- b. With power still off, remove the A/D Converter PWA and install the Digital Test Signal Generator PWA in the A/D converter slot. Turn on power.
- c. On the digital test signal generator, set PATTERN SELECT switch to position 2, CHROMA/KEY switch to PATTERN position, and LUMINANCE switch to PATTERN position. (This applies horizontally compressed full color bars, 100% saturation, with zero pedestal.)
- d. Connect a waveform monitor and a vectorscope to the video output, connector J10.
- e. Adjust R238 on the video output processor (Figure 4-22) until the bottoms of the red and blue components are at the same IRE level.
- f. Adjust R239 until the overall signal p-p amplitude is 100 IRE.

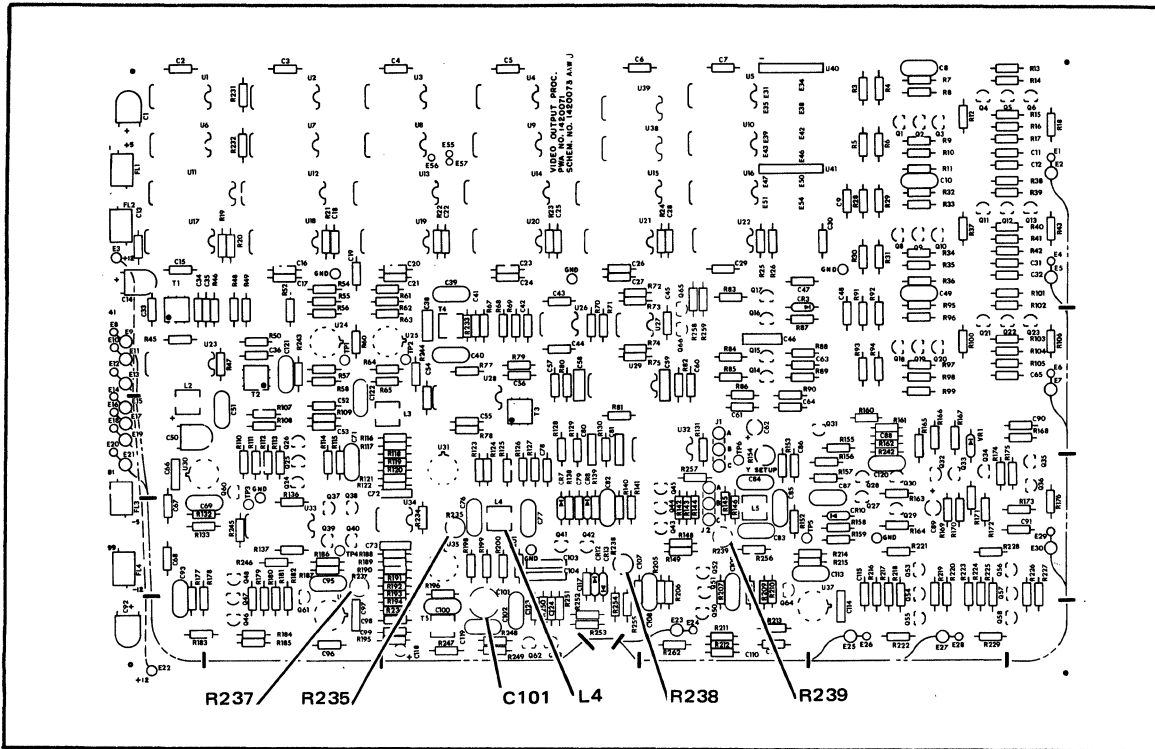


Figure 4-22. Video Output Processor PWA

- g. Continue to adjust R238 and R239 (interactive) until an overall amplitude of 100 IRE is obtained and the bottoms of the red and blue components are at the same IRE level.
- STEP 2** To minimize any 3.58-MHz component remaining after adjustment of the comb mesh detector (Comb Filter PWA), proceed as follows:
- a. With the digital test signal generator still installed in the A/D converter slot, verify that the test signal switches are in the same position as for adjustment number 1: PATT SEL in position 2, CHROMA/KEY at PATT position, and LUMINANCE at PATT position.
 - b. Connect a waveform monitor to the video output, connector J10. Look for 3.58 MHz appearing at the top of the white bar, as variations in the dc white level.
 - c. Adjust R235 and R237 on the video output processor to minimize any 3.58-MHz variations that appear. (R235 and R237 adjust the dc balance on the modulator output.)
- STEP 3** To adjust the 90° chroma vector phase difference, proceed as follows:
- a. With the digital test signal generator still installed in the A/D converter slot, verify that the test signal switches are in the same positions as for adjustment number 1: PATT SEL in position 2, CHROMA/KEY in PATT position, and LUMINANCE in PATT position.

- b. Connect a vectorscope to the video output, connector J10.
- c. Position 180° phase vector using vectorscope phase adjustment. Adjust L4 on the video output processor for the 270° vector and adjust C101 on the video output processor for the 90° vector, to position both chroma vectors within their target areas.
- d. With power off, remove Video Output Processor PWA and extender and Digital Test Signal Generator PWA. Reinstall A/D converter and vertical output processor.

4-32 Digital Section Adjustments

Clock adjustment procedures are given below for three digital section PWAs.

4-33 Output Control Clock

Refer to sheet 3 of schematic 1420055. First, determine that the frame pulse is present at 1H-2 (Figure 4-23). The phase lock loop error voltage is measured at 3G-6. Adjust L1 to obtain an error voltage level of 1.5V ±0.5V. (If the adjustment cannot be obtained, check the two frequencies applied to phase comparator 2G, pins 9 and 6.)

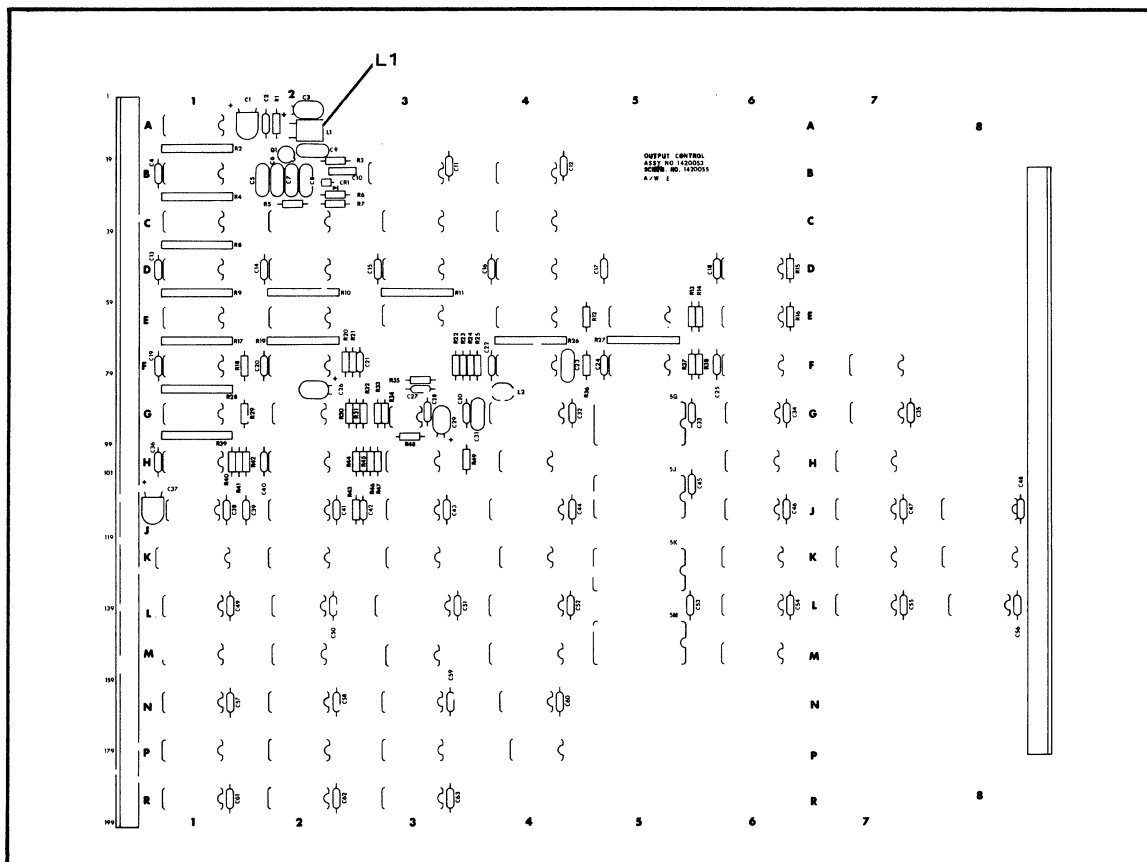


Figure 4-23. Output Control PWA

ADO

4-34 HLC Clock

Refer to sheet 8 of schematic 1464267. Adjust L1 (Figure 4-24) to obtain maximum signal amplitude at the Q4 collector.

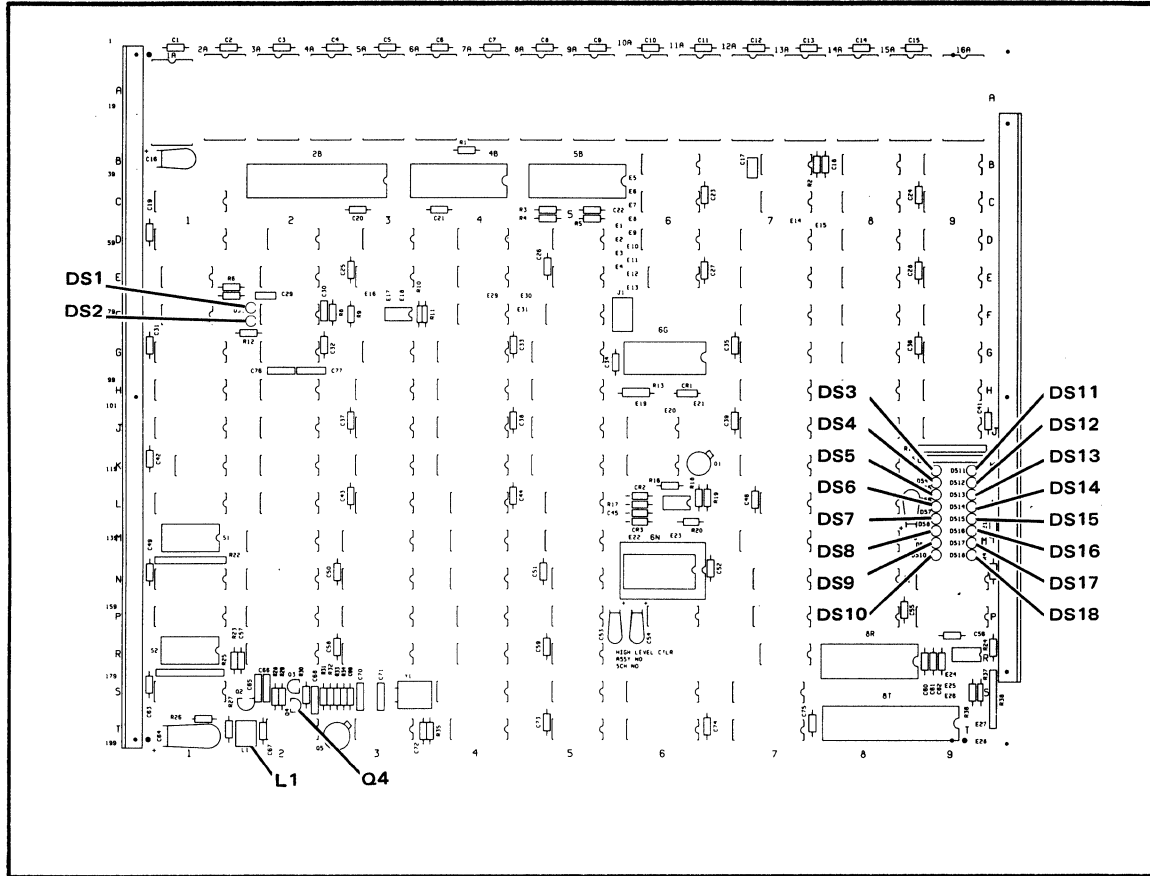


Figure 4-24. High Level Controller PWA

4-35 LLC Clock

Refer to sheet 2 of schematic 1464322. Adjust L1 (Figure 4-25) to obtain maximum signal amplitude at the Q3 collector.

4-36 Digital Test Signal Generator

The Digital Test Signal Generator, Ampex Part Number 1420458, is optional equipment. It is fabricated on a standard analog section PWA. In use, the PWA is inserted into the ADO analog card rack in place of the A/D Converter PWA. It provides an accurate, repeatable video test reference, free from noise and drift. The four types of signals generated are a digital ramp, color bars including 2T and 20T pulses, frequency sweeps, and flat fields. This equipment is described in the following paragraphs.

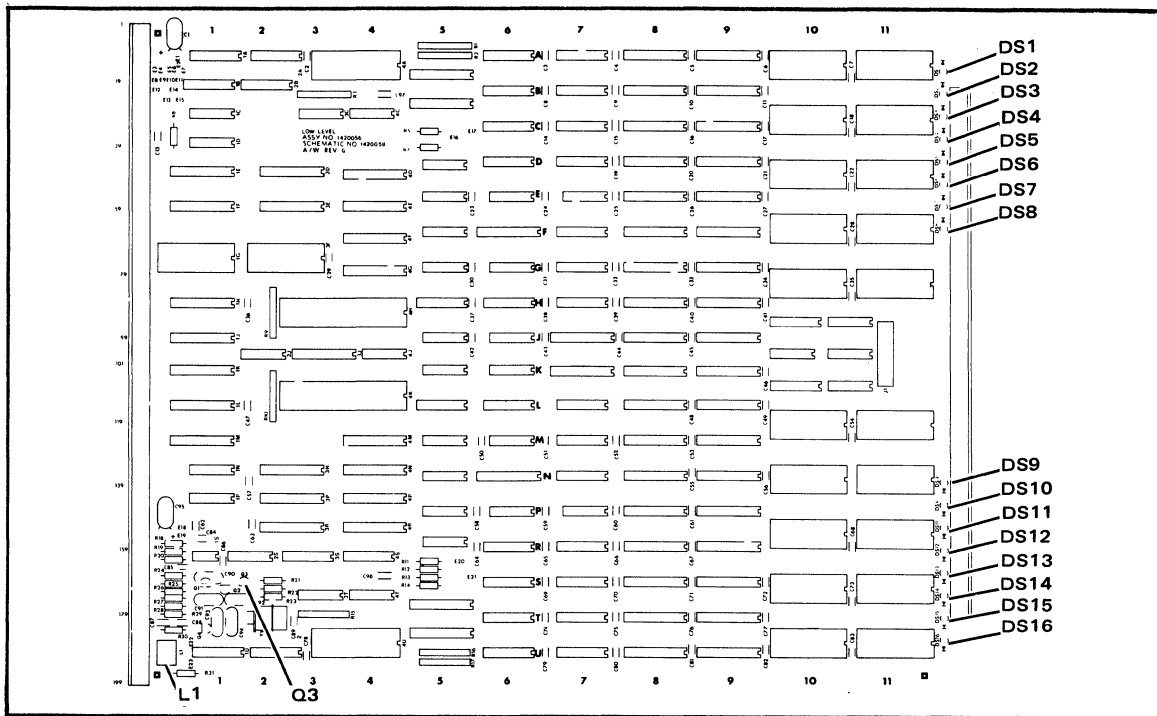


Figure 4-25. Low Level Controller PWA

4-37 Required Inputs

Apply composite video input and reference black video input to the ADO System when using the Signal Generator PWA. This PWA receives timing signals from two analog PWAs. The following three signals must be operational:

- Comb Filter PWA: VIDEO OUT (pin 26)
- Input Reference PWA: H (pin 53)
- Input Reference PWA: Fy (pins 47/48)

4-38 Controls and Outputs

The controls for the Signal Generator PWA consist of three toggle switches and a 16 position thumbwheel switch (Figure 4-26). The PATTERN SELECT and FLAT FIELD SELECT switches determine the signals generated. The CHROMA/KEY and LUMINANCE switches determine, independently of each other, which signals are applied to the chroma/key system and which are applied to the luminance system. The PATTERN SELECT and FLAT FIELD SELECT output signals are described below.

4-39 Pattern Select Signals

This switch selects one of three patterns:

1. A digital ramp consisting of a binary countup for Y and chroma/key channels (H patterns only).

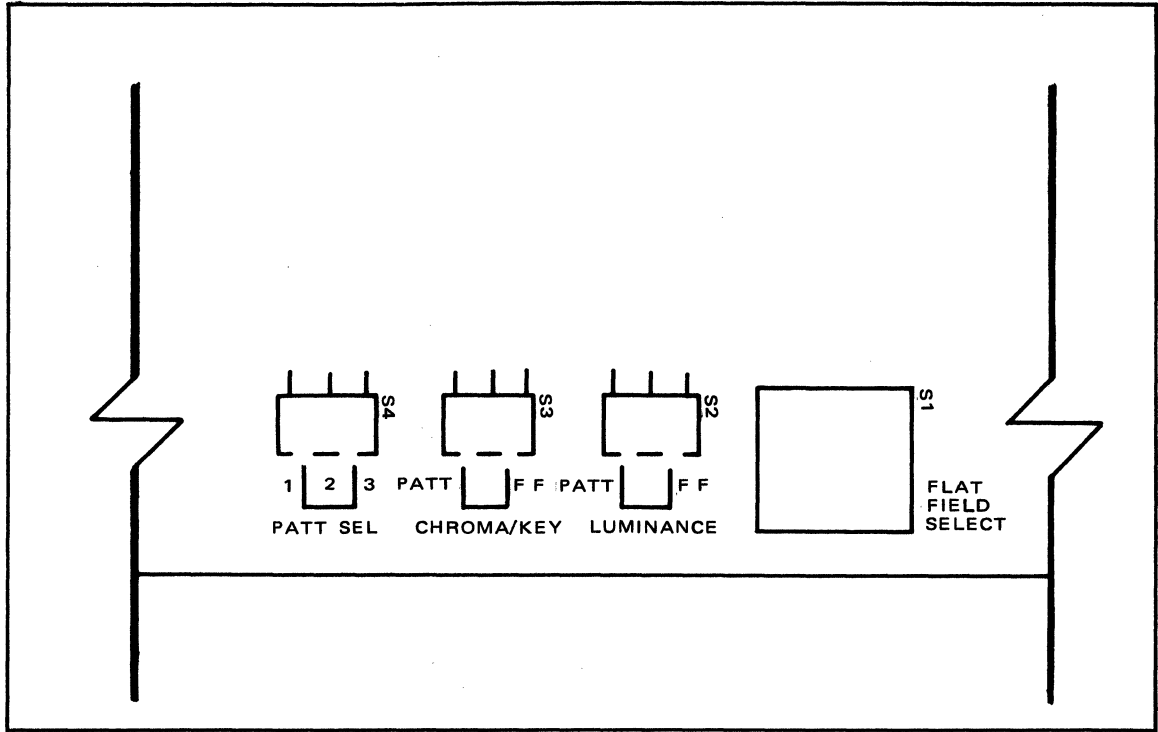


Figure 4-26. Digital Test Signal Generator Switches

2. Horizontally compressed EIA standard color bars, 100% saturated, 100 IRE white, zero pedestal. This pattern includes:
 - Standard 2T pulse (Y channel only).
 - Two modified 20T pulses, one with Y and R-Y components only and one with Y and B-Y components only. (The two pulses are not of equal amplitude.)
3. Frequency sweeps for Y and both chroma components, as follows:
 - Y sweep: reference 100 IRE, then +50 IRE, then 0 IRE, then a linear sweep from zero to 5 MHz.
 - Chroma sweeps: reference +100 IRE, then -100 IRE, then 0 IRE, then a linear sweep from zero to 1.5 MHz. (To observe a chroma channel, use output of D/A converter.)

4-40 Flat Field Select Signal

The flat field values are given in Table 4-4 for the 16 switch positions.

4-41 TROUBLESHOOTING

Troubleshooting information is given below for the analog and digital sections of the signal system chassis. Control unit troubleshooting usually cannot be done on the basis of the system output indications; perform standard PWA-to-PWA troubleshooting, from schematics.

Table 4-4. Flat Field Values

Switch Position	Y Amplitude	Burst Amplitude	Burst Phase
0	50	100	90
1	50	100	270
2	50	100	0
3	50	100	180
4	50	50	90
5	50	50	270
6	50	50	0
7	50	50	180
8	50	0	0
9	50	0	0
A	50	0	0
B	100	0	0
C	75	0	0
D	50	0	0
E	25	0	0
F	0	0	0

As an aid to standard troubleshooting methods, a few ADO guidelines are listed below:

- Observe signal system chassis PWA LEDs, described in Table 4-5.
- Observe system output on video monitor for visual indications listed in digital troubleshooting discussion, below.
- If indications do not point to the digital section or the analog section, begin with analog troubleshooting check; digital section troubleshooting requires a functional analog system.
- For luminance problems, the optional ADO Test Probe (luma probe), DT 1393420, can be used to isolate the fault.

4-42 Analog Section Troubleshooting

In the analog troubleshooting flowchart (Figure 4-27), the numbers assigned to the blocks correspond to the procedural steps described below. The analog input PWAs are the comb filter, A/D converter, and input reference. The analog output PWAs are the D/A converter, VOP (Video Output Processor), and output reference.

In general the procedures isolate a problem to the PWA level only. However, in some instances they include information on circuit level troubleshooting. Refer to Figure 4-27 and perform the following steps.

STEP 1 During system troubleshooting determine whether an analog problem is suspected.

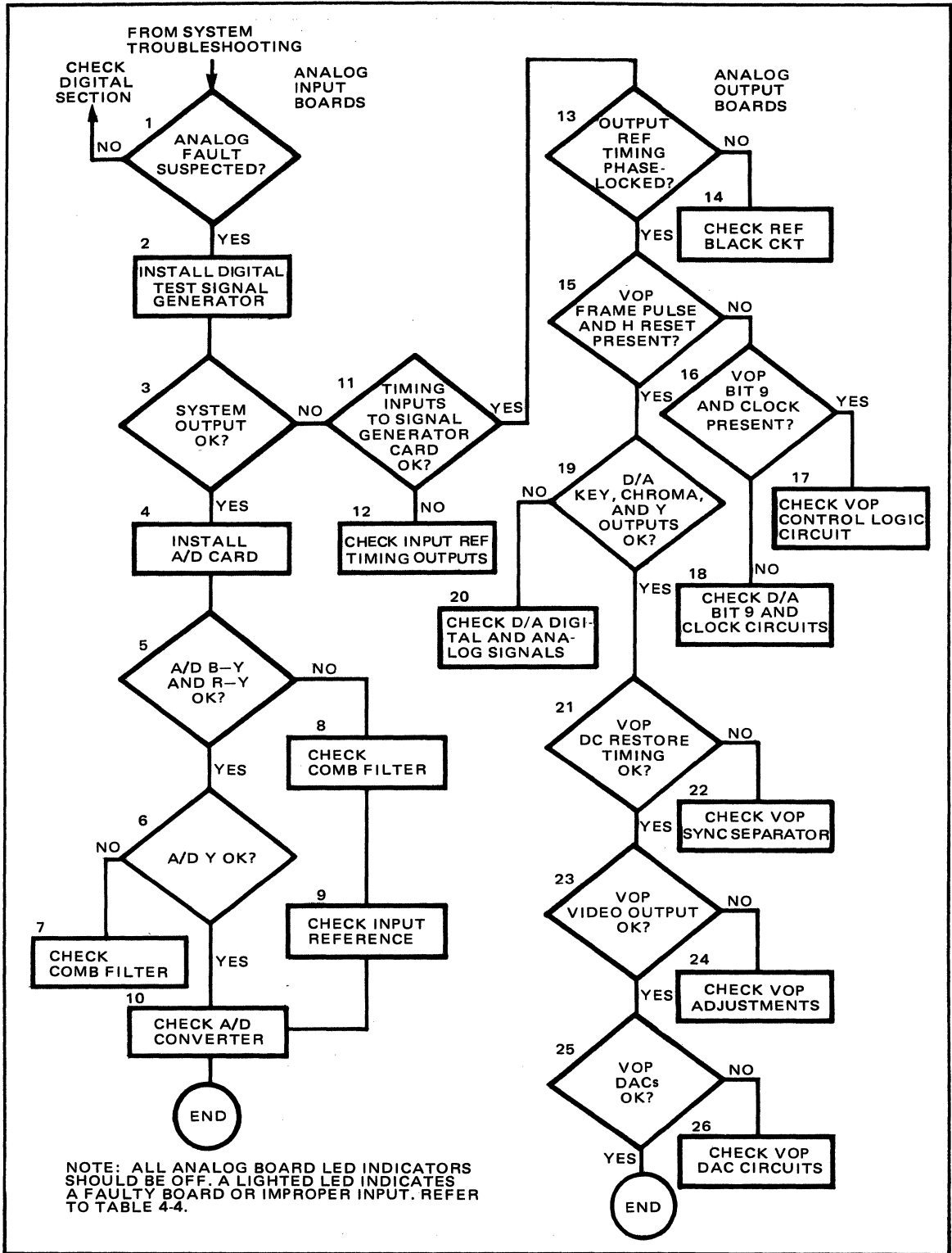


Figure 4-27. Analog Troubleshooting Flowchart

STEP 2 With power off, remove A/D Converter PWA and install Digital Test Signal Generator PWA (1420458) in A/D converter slot. Turn on power. On signal generator card, set PATT SEL (pattern select) switch to position 2. Set CHROMA/KEY switch to PATT, and LUMINANCE switch to PATT. (With neither switch at F.F., the FLAT FIELD SELECT switch is not enabled.) These settings provide horizontally compressed full color bars, 100% saturation, 100 IRE white, with zero pedestal.

STEP 3 Connect vectorscope and waveform monitor to system output, connector J9. With signal generator card installed, the waveform monitor should display the output shown in Figure 4-28. On vectorscope, B-Y and R-Y components should be in their target areas. If system output is correct with signal generator card installed, assume analog output PWAs are good. Proceed to steps 4 through 10, which check analog input PWAs. Note that only a few functions of the analog input PWAs are required for proper operation of the signal generator card:

- Comb Filter PWA—VIDEO OUT (pin 26)
- Input Reference PWA—H (pin 53) and Fy (pins 47/48)

If the system output is incorrect, check signal generator card inputs and output analog PWAs, according to steps 11 through 26.

STEP 4 With power off, remove signal generator card. Position A/D Converter PWA on extender, reinstall in A/D slot, and turn on power.

STEP 5 On A/D Converter PWA, use oscilloscope to verify that B-Y level (pin 60) and R-Y level (pin 64) are both at 800 mVp-p, with approximately 300 mV dc voltage offsets.

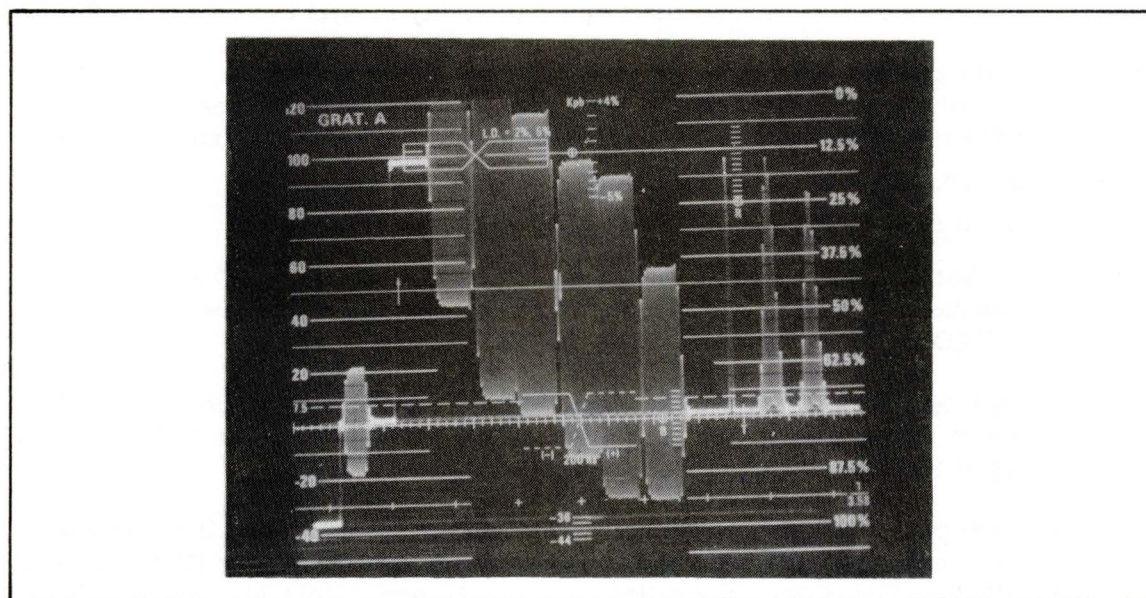


Figure 4-28. Digital Test Signal Generator Output

ADO

- STEP 6 On A/D Converter PWA, use oscilloscope to verify that Y level (pin 14) is 700 mVp-p.
- STEP 7 If A/D converter luminance input level is incorrect, perform comb filter adjustment procedure, paragraph 4-27. If there is no luminance output at pin 14 of Comb Filter PWA, or if it cannot be adjusted to proper level, replace Comb Filter PWA. (This assumes proper video input to Comb Filter PWA has been verified during system troubleshooting.) During comb filter Y check, if Y is readjusted to proper level but ADO system output is still incorrect, the fault is probably in A/D Converter PWA.
- STEP 8 With power off, remove Comb Filter PWA and place it on extender. Reinstall into card rack and turn on power. Connect oscilloscope probe to pin 30. Modulated chroma with no luminance on it should be observed. If not observed, the fault is probably in Comb Filter PWA. If proper chroma signal is observed, the Input Reference PWA should be checked.
- STEP 9 With power off, remove Input Reference PWA, place on extender, and reinstall. Turn on power. Connect oscilloscope probe to pin 30. Observe whether modulated chroma input is present. Then check for color difference outputs B-Y (pin 60) and R-Y (pin 64). With proper chroma and video inputs, if color difference signals are not both present the fault is in the Input Reference PWA. If both color difference signals are present, perform input reference adjustment procedure, paragraph 4-28. If this does not correct system output, A/D Converter PWA should be checked.
- STEP 10 If A/D Converter PWA is receiving proper Y and color difference signals, perform A/D converter adjustment procedure, paragraph 4-29. If system output is still incorrect, the fault is probably in A/D Converter PWA.
- STEP 11 With power off, remove Input Reference PWA and place it on extender. Reinstall into card rack and turn on power. Use oscilloscope to check for presence of the two timing signals required by the signal generator card:
- 13.5 MHz (input reference pins 47/48)
 - H (input reference pins 53/54)
- If both timing signals are present, analog output PWAs should be checked. If timing signals are not present, check for the presence of VIDEO OUT, Comb Filter PWA, pin 26.
- STEP 12 Use oscilloscope to verify video input at input reference pin 26. With video input present, if 13.5-MHz and H outputs are not both present, Input Reference PWA should be replaced.
- STEP 13 With power off, remove Output Reference PWA and place it on extender. Reinstall into card rack and turn on power. LED indicator DS3 should be off, indicating that the color phase lock loop is locked up. Use oscilloscope to verify presence of COMP SYNC (pins 29/30) and SC (pins 55/56/58). If all LEDs are off and all signals are present, sync separator circuit is functioning.

- STEP 14 If any output reference LED is lighted, or if all signals of step 13 are not present, use oscilloscope to verify presence of REF BLACK VIDEO IN (pin 26). If video input is present, replace Output Reference PWA or troubleshoot sync separator circuit.
- STEP 15 With power off, remove VOP PWA and place it on extender. Reinstall into card rack and turn on power. Use oscilloscope to check for presence of INHIBIT (pin 28) and H RESET (pins 61/62).
- STEP 16 On VOP PWA, use oscilloscope to check for presence of BIT 9 data (pin 56) and 13.5 MHz CLOCK signal (pin 76).
- STEP 17 Replace VOP PWA or troubleshoot decoder U1, U6, sequencer U2, U3, U7, U8, U9, or video timing counter U5, U10, U16, U22, U38.
- STEP 18 With power off, remove D/A Converter PWA and place it on extender. Reinstall into card rack and turn on power. Use oscilloscope to check BIT 9 output (pins 55/56) and 13.5 MHz output (pin 66). Check BIT 9 input during frame time (pins 69/70) and 13.5 MHz input (pins 59/60), to determine whether fault is in D/A Converter PWA.
- STEP 19 With power off, remove D/A Converter PWA and place it on an extender. Reinstall into card rack and turn on power. Use oscilloscope to check the following analog output levels:
- Y (pin 48) - 720 mV p-p
 - KEY OUT (pin 44) - 900 mV p-p
 - R-Y (pin 40) - 1.0 V p-p
 - B-Y (pin 36) - 700 mV p-p
- STEP 20 On D/A Converter PWA, use oscilloscope to verify that H RESET (pins 61/62) and Ms DISABLE (pin 31) are present. Then, if analog outputs are present but at incorrect levels, perform D/A converter adjustment procedure, paragraph 4-30.
- STEP 21 With power off, remove VOP PWA and place on extender. Reinstall into card rack and turn on power. Use oscilloscope to check the two dc-restore pulses. One is a 1.9 μ s positive-going pulse at the leading edge of H sync (U29 pin 13). This is used to restore dc level in both color difference signals. The second pulse is a 3.8 μ s positive-going pulse (U29 pin 5) at color burst time. This is used for clamping Y to zero IRE.
- STEP 22 On VOP PWA, use oscilloscope to verify Y input (pin 78). Then check sync separator circuit, Q14, Q15, Q16, Q17, and U29. Repair or replace VOP PWA.
- STEP 23 Connect waveform monitor and vectorscope to system video output, connector J10. Verify signal generator card switch settings: PATT SEL at position 2, CHROMA/KEY at PATT, and LUMINANCE at PATT.

ADO

Check whether waveform monitor displays output shown in Figure 4-28 and whether B-Y and R-Y components are in target areas on vector-scope.

- STEP 24 If output is present but at incorrect levels or phases, perform the VOP adjustment procedure, paragraph 4-31. If there is not adequate adjustment range for amplitude (adjustment 1 of VOP adjustment procedure), and if the video signal is correct, replace VOP PWA. If there is not adequate adjustment range for phase (adjustment 3 of VOP adjustment procedure), attempt to isolate the problem by checking phase at circuit node R247/R248. Use a Tektronix 465 (or equivalent) oscilloscope with a X10 probe, driving the vectorscope from the vertical output.
- STEP 25 To check the VOP DAC circuitry, connect vectorscope to system output, connector J10. On the control unit, enter start-up mode. With menu page 1 displayed, select burst phase by pressing soft key D, then use joystick to vary burst phase. Observe burst phase on vectorscope. Verify that it can be rotated 360° by joystick action. This verifies operation of DACs U18, U19, and associated circuitry. Similarly, select chroma gain in set-up mode and use oscilloscope to verify changes in pin 42 level while exercising joystick. Also check Y gain, verifying changes in pin 40 level. These two checks verify DACs U20 and U21, respectively.
- STEP 26 Troubleshoot DAC circuits as needed. Use an oscilloscope to check the analog outputs of DAC U18 (sine value), pins 2 and 4, and DAC U19 (cosine value), pins 2 and 4. With control unit in set-up mode and burst phase selected, exercise joystick and check for changes in outputs of these two DACs. If the outputs do not change, troubleshoot back through registers U12 - U15, sequencer U2, U3, U7, U8, U9, decoder U1, U6, and the clock circuit. Similarly, use set-up mode to check for chroma gain changes at U21 pin 2 and to check for Y gain changes at U20 pin 2, as needed. Perform further troubleshooting as needed.

4-43 Digital Section Troubleshooting

The troubleshooting description includes a simplified flowchart, fault isolation methods, and luminance troubleshooting. For a suspected digital section fault, first check the digital PWA LED indicators listed in Table 4-5 for fault indications. If none exist, refer to the flowchart, Figure 4-29, for general troubleshooting considerations.

4-44 Digital Troubleshooting Flowchart

The flowchart (Figure 4-29) presents only an initial method of approach. Troubleshooting of the digital section involves too many factors to be covered in a step by step flowchart.

It is useful to isolate the fault to one of three functions, Y, chroma, or key. If any of these functions has proper transformation geometry, the fault is probably in the Y, chroma, or key data paths rather than in the LLC, HLC, or address generator PWAs. If it is not obvious which of the three data paths is at fault, remove the

Table 4-5. Signal System Chassis Indicators

PWA	LED	Function	Remarks
Input Reference 1420077 (Figure 4-19)	DS1	SYNC PRESENCE	Normally OFF
	DS2	H LOOP LOCK	Normally OFF (but may flicker dimly in normal operation)
	DS3	COLOR PLL LOCKED	Normally OFF
Output Refer- ence 1420369 (Figure 4-30)	DS1	BURST PRESENT	Normally OFF
	DS2	SYNC PRESENT	Normally OFF
	DS3	COLOR PLL LOCKED	Normally OFF
Input Control (Figure 4-31)	DS1 DS2 DS3 DS4 DS5		All indicators sequentially blinking means normal cycling of Y memories.
HLC 1464265 (Figure 4-24)	DS1		ON for a downlink message (CPP to HLC)
	DS2		ON for an uplink message (HLC to CPP)
	DS3		Normally OFF; blinks if input video is not phase-locked to reference blank video input.
	DS4		OFF
	DS5		OFF
	DS6		OFF
	DS7		ON
	DS8		ON
	DS9		ON when either DS1 or DS2 is ON, OFF at other times. If not thus consistent, cable or XMT/RCV circuit has hardware fault.
	DS10-18		All ON
LLC 1464320 (Figure 4-25)	DS8, DS16 DS15		Both normally ON, indicating proper LLC operation.
			ON when input Y memories are in normal mode (reading out vertically). OFF when they are in transpose mode (reading out horizontally).

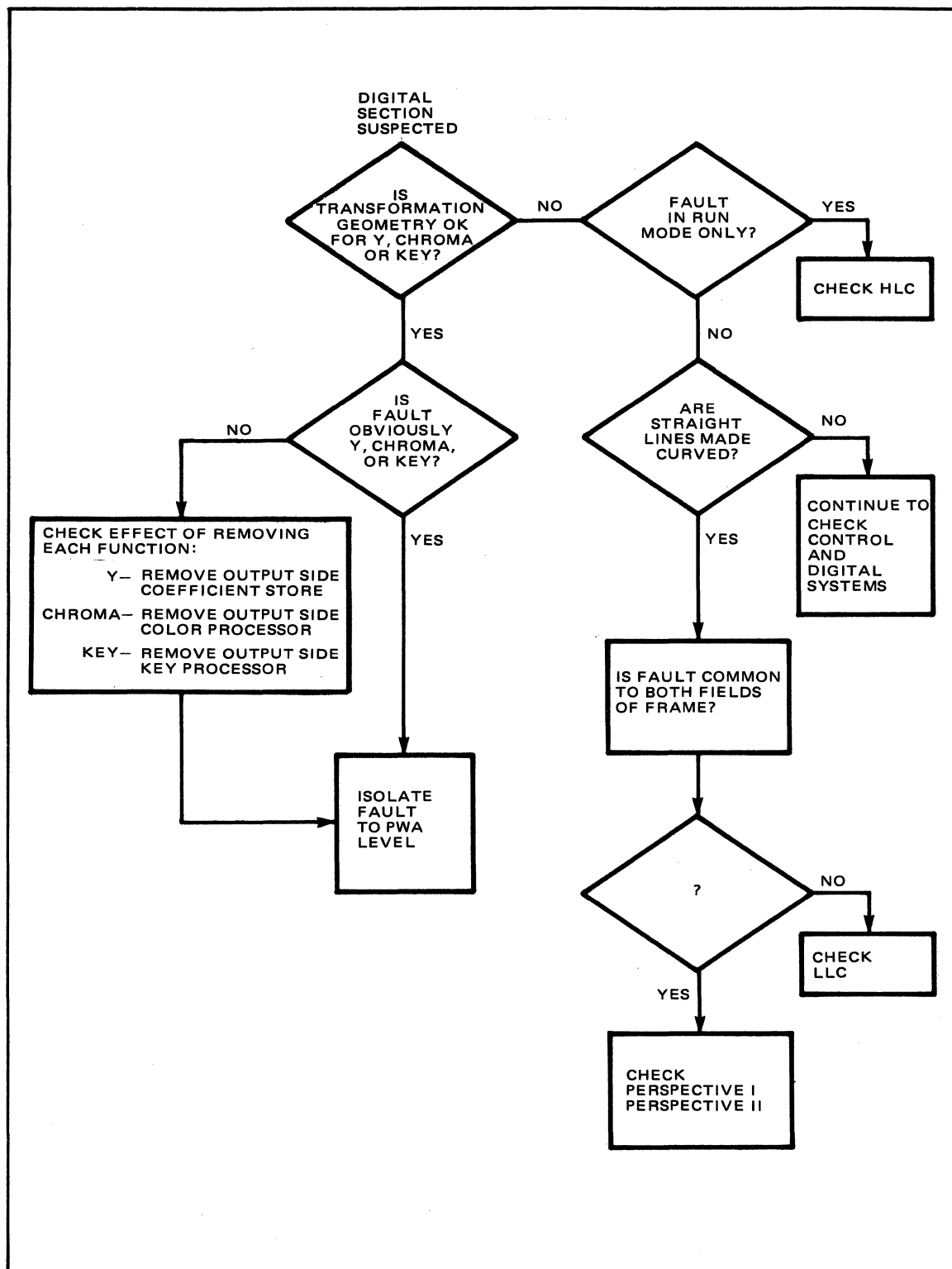


Figure 4-29. Digital Troubleshooting Flowchart

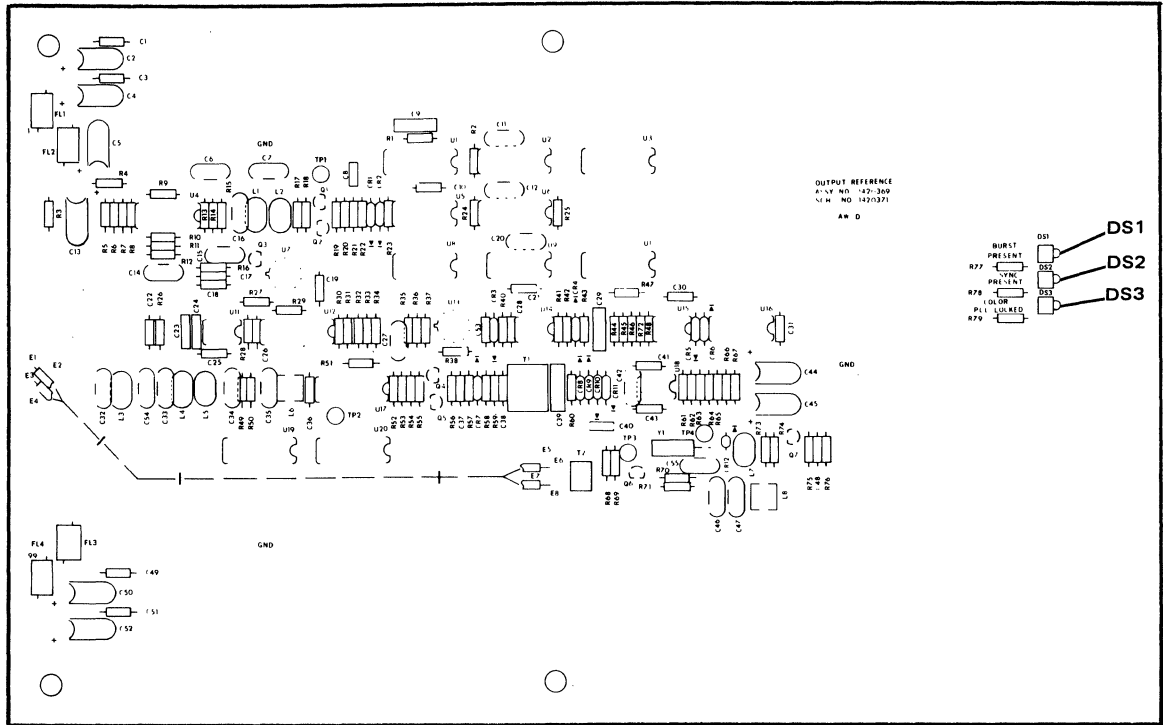


Figure 4-30. Output Reference PWA

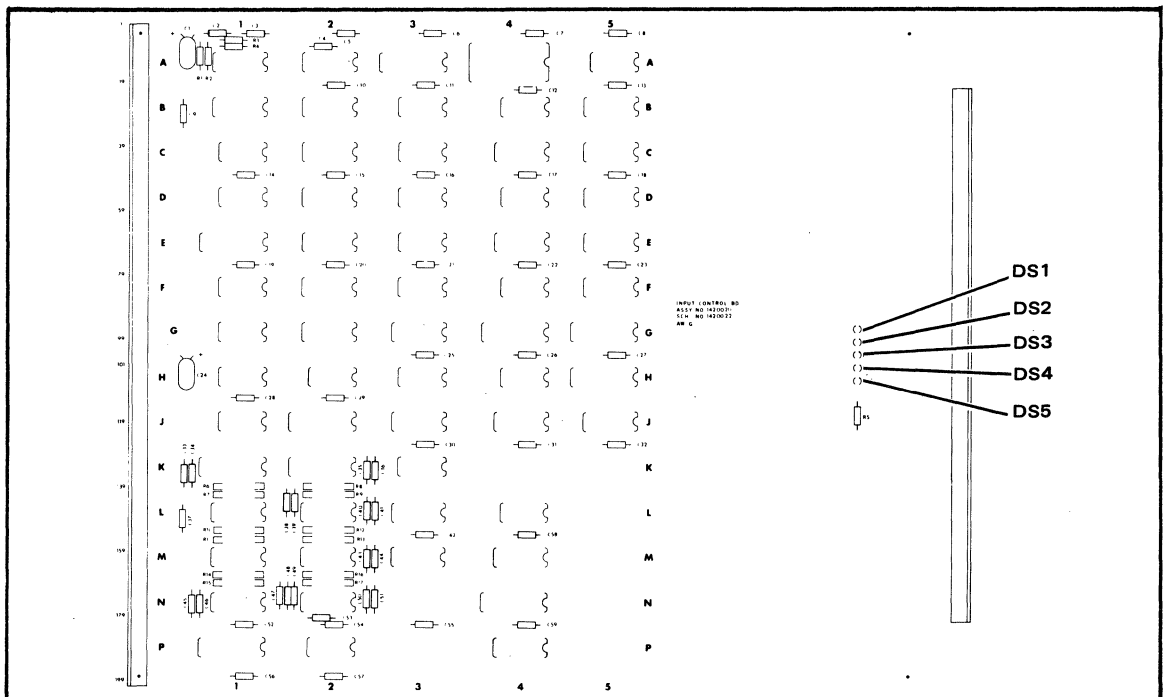


Figure 4-31. Input Control PWA

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PWAs as indicated in Figure 4-29, in turn, to determine the source of the fault. For example, if the output side color processor is removed, any Y problem would still be evident; removing the output side Coefficient Store PWA would remove the Y problem, leaving a stable chroma image. Removal of the output side key processor would not affect the Y problem.

CAUTION

**TURN POWER OFF WHEN REMOVING OR INSERTING PWAs.
WHEN USING EXTENDER BOARDS BE SURE CARD EDGE PINS
ARE PROPERLY ALIGNED.**

For image-geometry faults affecting Y, chroma, and key functions, the flowchart shows two examples of faults that point to the HLC or to the LLC and address generator PWAs. An overall image-geometry fault is likely to be in the address generator PWAs or in the control system (control unit plus HLC and LLC). For an address generator fault, the video monitor indication occurs in a vertical or horizontal direction. Typical geometry problems are accompanied by jumpy rotations around the Z-axis.

4-45 Fault Isolation Methods

Fault isolation to a given system, as discussed above, can be done by successively interrupting the Y, chroma, and key data paths just prior to the Horizontal Processor PWA, and noting the effect in each instance. Another useful technique is the swapping of identical PWAs between the input and output sides of the digital section. (See digital processor block diagram, Figure 5-3.) The input and output side PWAs for most ADO data functions are identical. The switching in/out of vertical or horizontal functions, where required, is accomplished by appropriate V and H side backplane wiring.

A typical image-geometry indication is the presence of horizontal or vertical line patterns. The lines are usually limited to one of the three functions, Y, chroma, or key, although this may not be obvious. For vertical lines, suspect output side (horizontal) PWAs; for horizontal lines suspect input side (vertical) PWAs. This is a good general rule, but there are exceptions.

The following troubleshooting example, based on definite V or H line indications, illustrates this method. Having identified a chroma problem causing horizontal lines, suspect the vertical section chroma PWAs: chroma/key memory and color processor (see Figure 5-3). Swap the V and H chroma/key memories (or the V and H color processors). If the lines become vertical a fault in the chroma/key memory (or the color processor) now in the H slot is indicated. However, if the lines still remain horizontal after swapping both types of PWAs, swap the H and V perspective I PWAs, and then the H and V perspective II PWAs. If the lines are still horizontal, suspect the Input Control PWA, which provides control signals to the input side chroma/key memory and color processor. Since the Control PWA cannot be swapped, troubleshooting within this PWA is needed to definitely isolate the fault to the PWA. Refer to the appropriate PWA theory discussion, Section 5 of this manual.

The fine blanking function also provides obvious fault indications. Improper top and bottom borders point to the vertical processor or the (V) color processor (Y or chroma). Improper left and right borders point to the horizontal processor or the (H) color processor (Y or chroma). It can be useful to compress a full size image and insert a border, to check this function. Similarly, coarse blanking faults point to the coefficient store PWAs (Y), to the color processor coefficient store circuits (chroma), or to the key processor (key).

4-46 Luminance Troubleshooting

Some characteristic Y fault indications are described below. Also, the use of the optional ADO Test Probe (luma probe) is described.

For a fault in one of the five input side Y memories, a one-in-five field flicker is seen on the video monitor. To determine which PWA is at fault, disable each PWA in turn. This is done by pressing the white button switch at the bottom front edge of each memory PWA; this disables the output latches. Disabling a good PWA increases the flicker rate; disabling the PWA at fault causes no change in the rate of flicker (though possibly in the degree). Similarly, loss of output from one of the two Y memories on the output side causes video monitor flickering on alternate fields, which is unaffected by the freeze function. Disable each output side PWA in turn to isolate the fault.

Loss of a group of drive signals to an input side memory is indicated by the sequencing DS1-5 LED indicators on the Input Control PWA (Table 4-5); one LED remains OFF. If DS1-5 are flashing in sequence, 1 cycle per frame (each indicator on for 1/5 frame or 6.67 ms), determine whether the fault is due to a single drive signal from the Input Control PWA. To do this, swap a suspected input side memory with a memory from the output side. Determine whether this changes the video monitor flicker rate from one-in-five to one-in-two. If it does, the suspected PWA is at fault. If the flicker rate does not change, suspect a single drive signal from the Input Control PWA to the indicated memory PWA location. If the indicators are flashing more slowly than 1 cycle per frame, the LLC is probably faulty.

Interpolation problems are typically characterized by definite amplitude variations in the image as viewed on the monitor. These are most easily seen in a flat field such as that provided by test signals. For Y problems of this type, swap the H and V interpolator PWAs and then the coefficient store PWAs to see which exchange causes a change in direction of the fault indication. Either PWA type can cause these amplitude variations.

4-47 Miscellaneous Fault Indications

Some additional fault indications, and the probable sources, are listed in Table 4-6. Also, the PWA block diagrams (Section 5) provide quick references of the functions associated with the various digital processor PWAs.

Table 4-6. Miscellaneous Fault Indications

Condition	Probable Cause
Image motion is jerky; effect is accentuated during rotation	Perspective I and II
Image completely erroneous	HLC
Alternate fields completely erroneous	LLC (one side)
Fault affects both Y and chroma (chroma effect may not be as noticeable)	Perspective I and II
Output sync fault	Horizontal Processor
Alternate field chroma flickering	Chroma/Key Memory
Chroma disappears for 1/2 size image	Color Processor

SECTION 5

THEORY OF OPERATION

5-1 INTRODUCTION

This section contains descriptions of system, subsystem, and PWA theory.

5-2 SYSTEM

As shown in the system functional diagram (Figure 5-1), composite video input is processed by three analog input PWAs and applied digitally to the digital processor. Here the source image data is transformed into target image data, at real time video rates. The transformed output, processed by three analog output PWAs, is reformatted to provide a composite video output.

Note that the control system includes the HLC (High Level Controller) and the LLC (Low Level Controller), along with the control unit. The HLC and LLC PWAs are located within the same card rack as the digital processor PWAs but are functionally part of the control system.

5-3 SUBSYSTEM FUNCTIONAL DESCRIPTION

The subsystem is divided into three main functional units (Figure 5-1): control system, analog system, and digital processor.

5-4 Control System

The control system consists of the control unit, the HLC, and the LLC. The keyboard CPU receives operator selections from the keyboard switch mounting PWA and receives analog coordinates from the joystick. It formats the information and sends it to the control processor (CPP). The CPP updates the menu monitor display, controls the optional floppy disk drive, and passes the operator selections on to the HLC, via the I/O PWA. The HLC provides smooth interpolations between the operator-selected key frame states. It sends commands to the LLC at a field rate.

The LLC implements HLC commands by calculating transformation parameters used by the digital processor PWAs. The LLC consists of two microcomputers that process transformation parameters for alternate fields. These transformation parameters are sent to the vertical and horizontal address generator PWAs. The LLC also sends commands and control data to most of the other digital processor PWAs. All this information is sent via a 23-bit computer bus consisting of 16 data lines, 6 address lines, and a strobe line.

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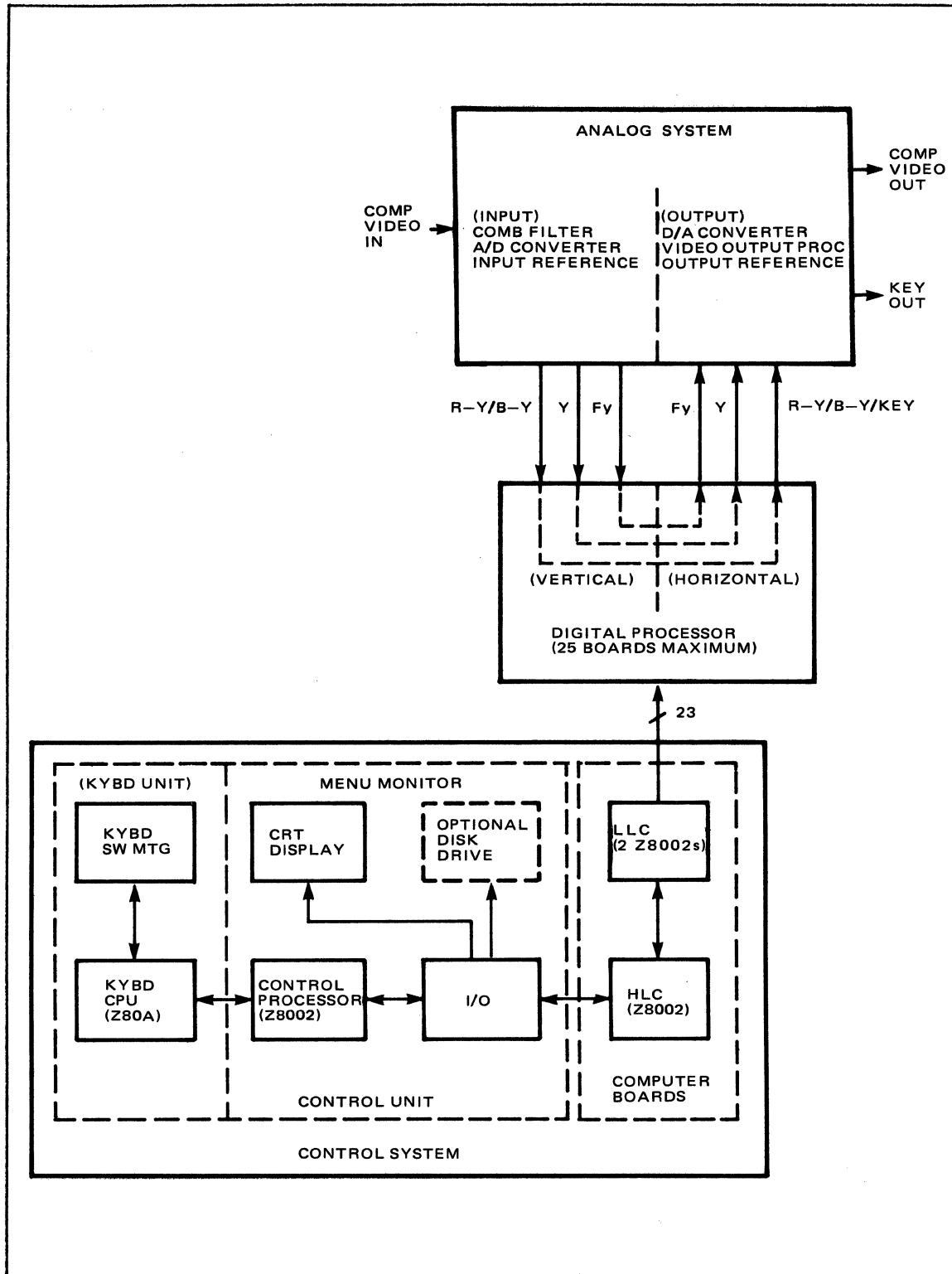


Figure 5-1. ADO System Functional Diagram

5-5 Analog System

The analog system is the analog portion of the signal system chassis. It includes three input PWAs and three output PWAs, indicated in Figure 5-1 and shown in more detail in Figure 5-2.

The Comb Filter PWA separates input video into Y and chroma components; any trace of chroma left in the Y signal adversely affects picture quality. The Y signal is routed to the A/D converter. The chroma signal is applied to the Input Reference PWA for demodulation. A 4SC sampling clock is used to provide an exact 90° phase separation for the R-Y and B-Y components. The Input Reference PWA uses the composite video signal for regenerating various video control signals. A 27-MHz crystal-controlled clock, periodically lined up with H-sync, provides 2Fy and Fy. Timing for the entire processing system is based on Fy (13.5 MHz) and a frame pulse derived from it.

The A/D converter samples Y at the Fy rate and samples multiplexed R-Y and B-Y signals at Fy/4. A digitized 8-bit pixel (picture element) value is produced separately for each Y, R-Y, and B-Y sample. The resulting fields are not tied to input video timing but only to Fy. Y bytes and multiplexed R-Y/B-Y bytes are sent over differential pairs to the digital processor. Also, R-Y, B-Y, and PLL feedback signals are sent to the Input Reference PWA, for phase correction.

The digital processor provides digitized key information, which is multiplexed with the chroma signals. The chroma/key sequence, applied to the D/A converter on differential pairs, is: B-Y, key, R-Y, key, and so forth. Also, the digital processor adds a ninth bit to the digitized Y signal, extending its range as needed for the H sync pulse. During frame vertical blanking the D/A converter uses the bit 9 channel to serially transmit computer information to the VOP (Video Output Processor). Y input to the BIT 9 channel is disabled during this time.

The D/A converter provides timing delays as needed to line up the digitized Y and chroma/key inputs before conversion to analog. Fy, Fy/2, Fy/4, and H RESET are used for timing the delays and for D/A conversions. The resulting Y, B-Y, and R-Y signals are applied to the VOP. The key signal is applied directly to the system KEY OUT connector, J11.

The VOP receives a color subcarrier, SC, modulates it with R-Y and B-Y, and combines it with the Y input. This PWA also receives a stream of bit 9 data, which includes chroma gain, Y gain, and SC phase values. These values are determined during setup mode by control unit inputs. The VOP also includes circuits that generate clamp pulses for Y and chroma. Transformed data is reformatted into composite video on this PWA, to provide the ADO System output.

The Output Reference PWA provides a means to synchronize the ADO output to the equipment load. It generates a 3.58-MHz subcarrier from a reference black video input. This SC signal, applied to the VOP for composite video modulation, is phase-locked to the station reference video.

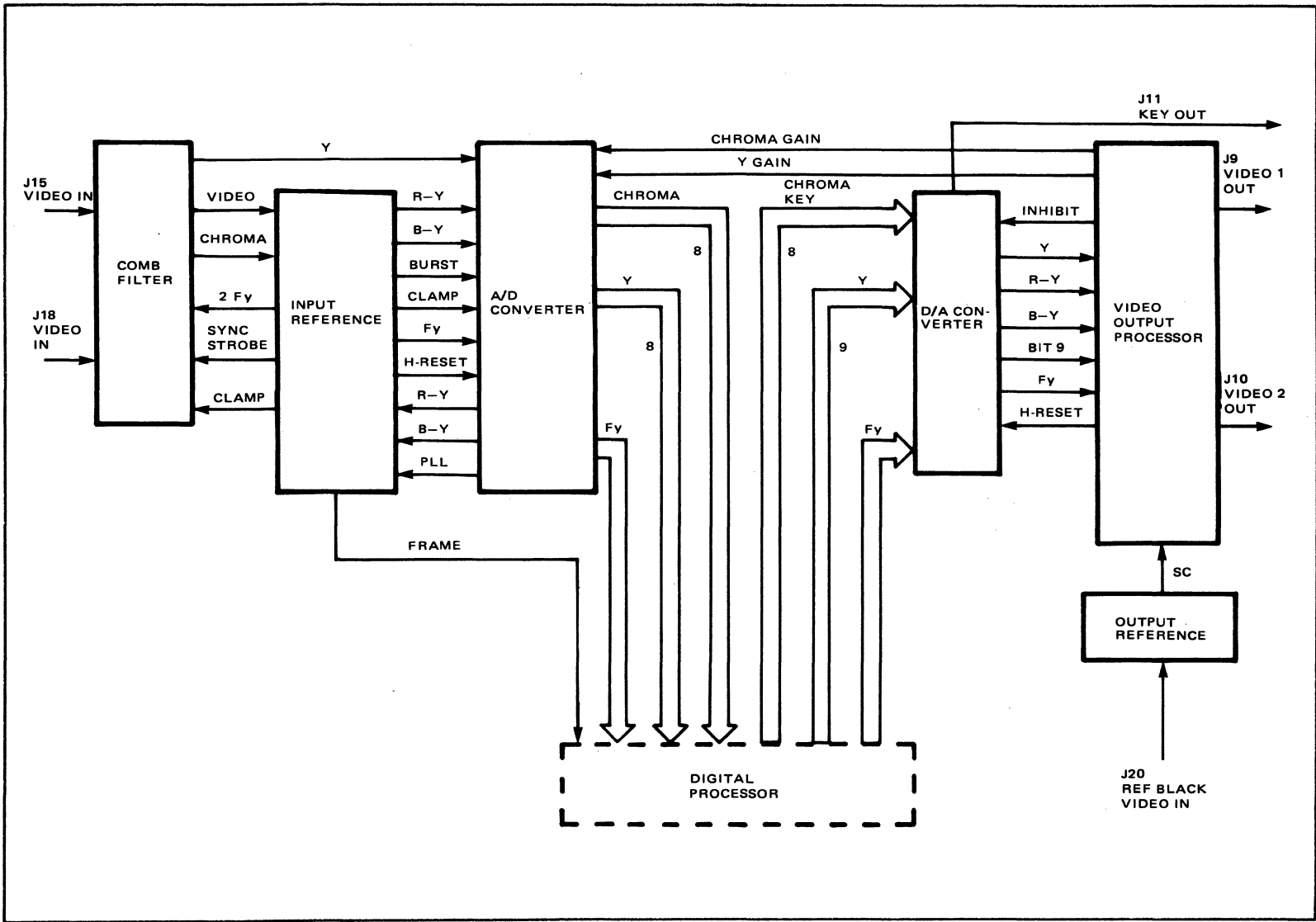


Figure 5-2. Analog System Block Diagram

5-6 Digital Processor

Under direct control of the LLC computers, the digital processor performs the following main functions:

1. Stores then modifies the source image pixel fields as required to provide suitable pixel frames.
2. Performs image transformations each frame on a pixel-by-pixel basis.
 - Interpolates; moves pixels by noninteger multiples of pixel spacing.
 - Moves pixels by distances that vary throughout a frame image.
3. Generates key data.
4. Adds blanking, sync, and color burst gate to the fully transformed data.

ADO special effects include translation, compression, expansion, rotation, perspective projection, and combinations of these. To accomplish these transformations at real time video rates, 13.5 MHz (Fy) clocking is used in conjunction with multiple parallel processing paths. As indicated in Figure 5-1, Y data and multiplexed chroma data follow separate, parallel processing paths throughout the digital processor. Further, each Y or chroma component is separately and sequentially transformed in the vertical and horizontal dimensions; while H circuits are processing a frame, V circuits are simultaneously processing the succeeding frame.

Details on the digital processor will be included in a future edition of this manual.

5-7 ANALOG SYSTEM PWAS

The analog system consists of the six PWAs located in the analog section of the signal system chassis. Refer to the analog system description, paragraph 5-5, and the analog block diagram, Figure 5-2. The analog PWAs are described below.

5-8 Comb Filter

The function of the Comb Filter PWA is to separate the input video into Y and chroma components. The PWA consists of two main circuit sections: IH delay paths (including input processing circuits) and Y and chroma matrices. Separate block diagrams are presented for the descriptions of these two functions. Also, a brief description of comb filter theory, as it applies to this PWA, is given.

5-9 Comb Filter Theory

Comb filtering is based on the spectral distributions of the Y and chroma components of a television signal. The principal Y frequency components occur at the horizontal scanning rate and its harmonics. The principal chroma components occur at the color subcarrier rate and within sidebands due to modulation of the subcarrier by the scanning rate and its harmonics. Therefore, in the chroma region, Y frequencies (dotted lines) and chroma frequencies (solid lines) are interleaved as

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shown in Figure 5-3a (for partial chroma region). Comb filtering uses 1H delays in conjunction with summing matrices to undo this interleaving, providing separate Y and chroma outputs. The highly simplified spectral distribution of Figure 5-3a includes the principal components only. However, the comb filter response is broad enough to handle sideband frequencies that occur at each of these spectral lines.

Figure 5-3b shows the 1H delay configuration for the Comb Filter PWA. The schematic notations Lt, Lm, and Lb (top, middle, and bottom lines of sheet 2 of schematic 1420126) are used. Figure 5-3c shows the basic Y and chroma matrix configurations for this PWA. The resistor values provide weighting factors of 1/4, 1/2, and 1/4 for Lt, Lm, and Lb values at the output summing point.

For the Y matrix, Y values are all additive, as the three lines are all in phase. That is, for 15.734 KHz and all multiples, the phase of the delayed signal is maintained for 1H and 2H delays. Note that this matrix affects the Y vertical resolution, since Ym values are modified by Yt and Yb values. Weighted chroma values applied to the Y matrix cancel out to zero since the Cm chroma signal is 180° out of phase with both lines adjacent to it. For the subcarrier frequency and all other odd multiples of half the line rate, the 180° phase difference between adjacent lines is maintained for 1H and 2H delays.

The chroma matrix uses a circuit inversion for the summed Lt and Lb inputs, making the chroma values additive for all three lines and causing the Y values to cancel to zero. In the Comb Filter PWA, additional circuits are added to the basic matrices to accommodate special conditions and to retain as much as possible of the original Y spectrum.

5-10 Input Processing and 1H Delay Paths

In Figure 5-4, the top row of blocks are input processing circuits and burst phase circuits. The two other rows are identical 1H delay paths. The circuits of this block diagram are described below.

5-11 Input Processing Circuits. Refer to sheet 1 of schematic 1420126. Identical amplifier and clamping circuits are provided for video inputs A and B. Video A input is applied to the U1 amplifier. Circuit output is dc-clamped to ground at back porch time. The CLAMP pulse, at pin 76, is inverted to close switch U3-3,4 for two microseconds. This charges C10 to the dc level of the circuit output (Q1 emitter). Op amp U4-1 compares this level with ground and applies any correction voltage to adjust the U1-4 base drive. This in turn corrects the Q1 base drive, clamping the circuit output dc level to ground. Dc clamping is continuous; output level is resampled each back porch time.

The VID SEL signal, pin 28, selects the video A or B amplified output. A high turns U6-10 on, to turn U6-4 off, selecting the video A output; a low VID SEL selects the B video. Selected output provides a VIDEO OUT signal at pin 26, via U5-10 and Q26. Selected video is also applied to the sync clipper.

The purpose of the sync clipper is to provide a reference level near the bottom of the range of subsequent digital coding. A normal sync pulse exceeds the negative digital range. A correct sync pulse is reestablished by an extended digital range,

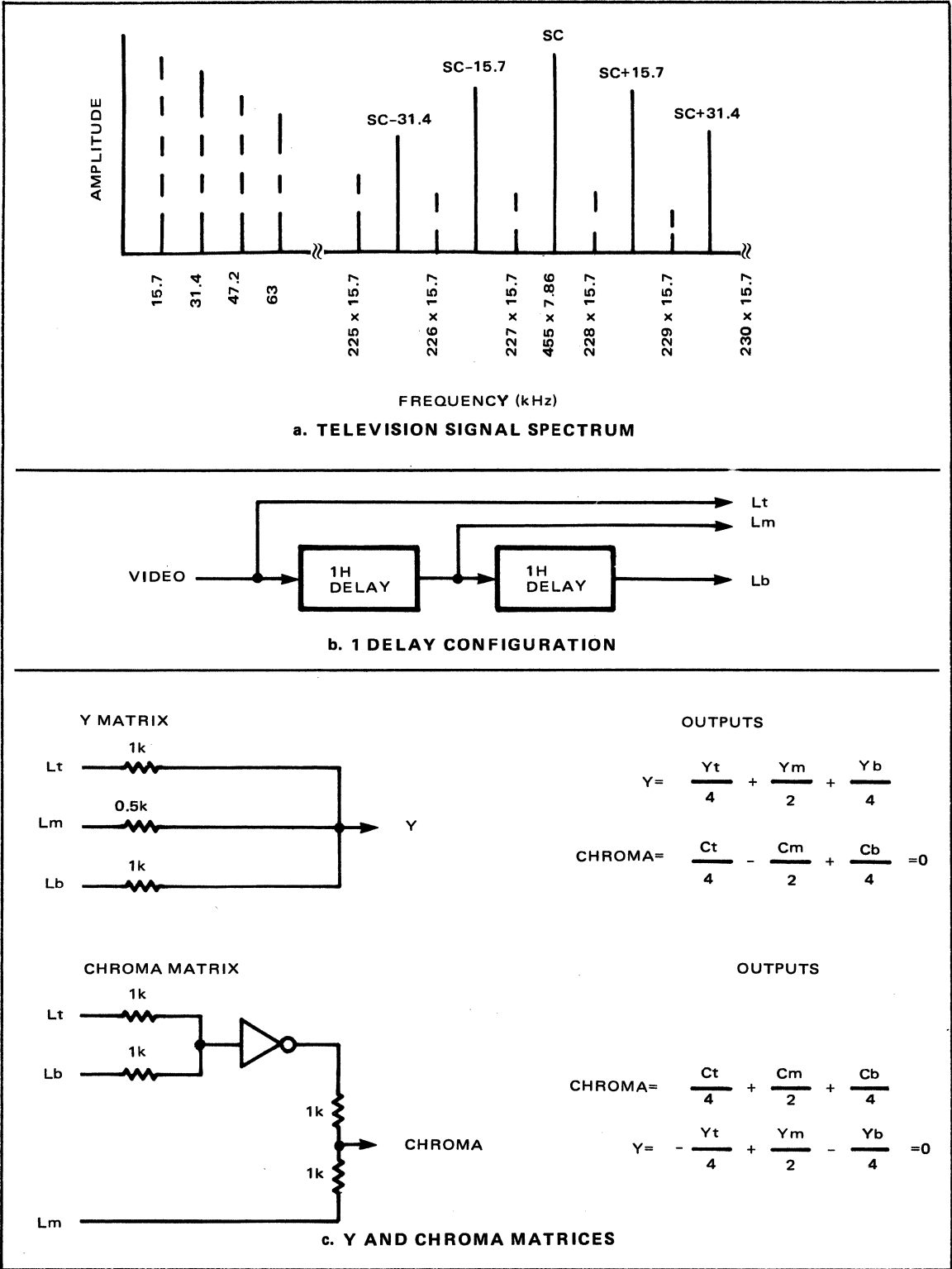


Figure 5-3. Comb Filtering

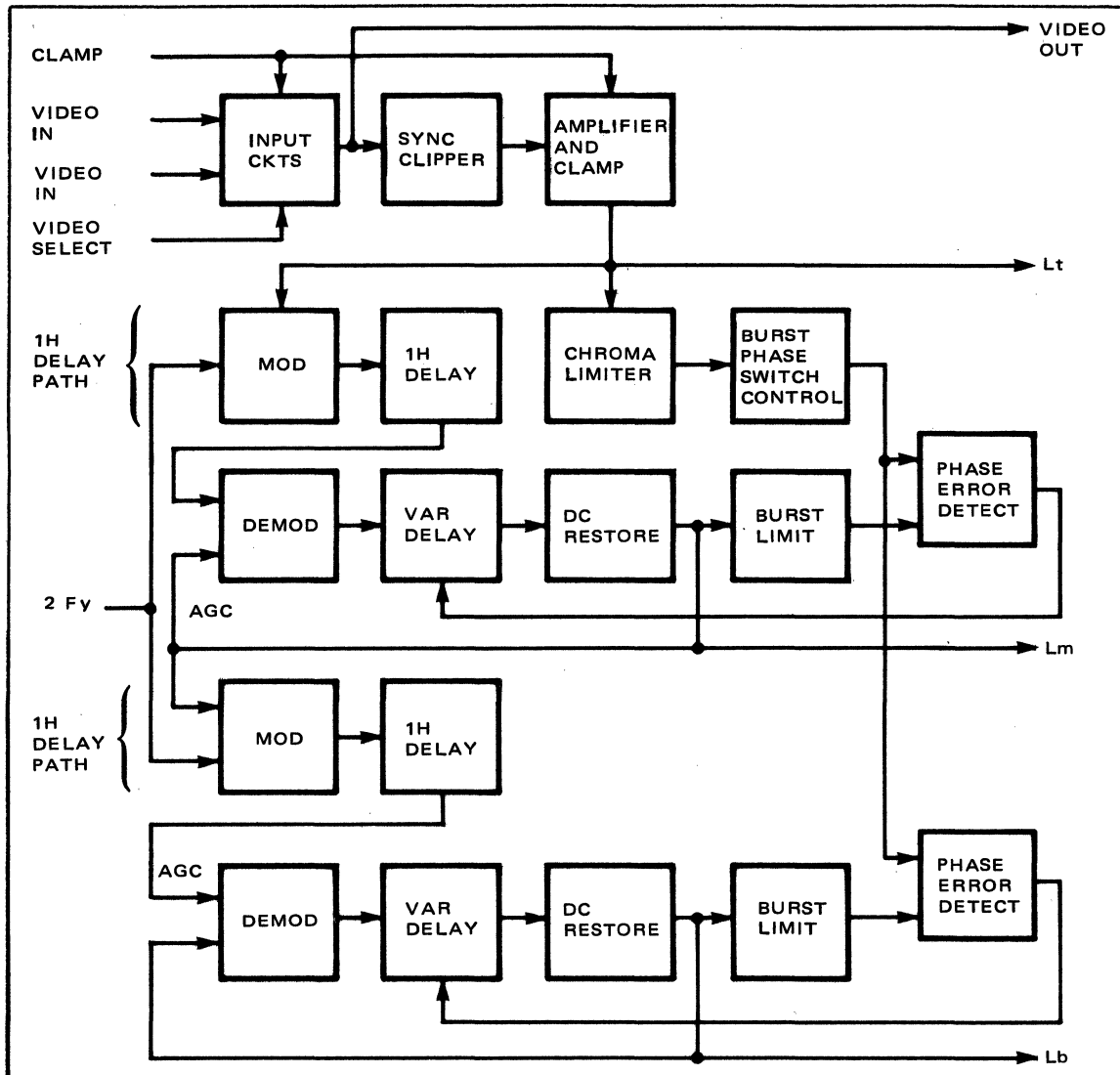


Figure 5-4. Input Processing and IH Delay Paths

following image transformation in the digital processor. The sync clipping circuit consists of U5-4, U5-2, Q5, and associated components. This circuit does not affect the video output applied to pin 26.

Video with clipped sync pulses is applied through a noise filter, L55/C212/C213, to the U7 amplifier and clamp circuit. The low-impedance U7 driver provides gain lost in the filter. Video output, at test point 12, is dc-clamped to ground at back porch time. The inverted CLAMP pulse closes switch U5-13,14, applying the circuit output dc level to C44. Op amp U10-1 applies any correction needed to U7-6 which in turn corrects the U7-9 drive. Circuit output dc level is continuously clamped, with resampling occurring each back porch time. The U7 circuit also provides a sync clamp output, used for automatic gain control. This function is discussed in the 1H delay path description.

The output signal, Lt, is applied to the Y and chroma matrices and to the modulator in the first 1H delay path. It also goes to a chroma limiter, which drives the burst phase switch control. The latter two circuits are used in the 1H delay paths, and are described in conjunction with the phase error detect circuit, below.

5-12 1H Delay Path. The two 1H delay paths are identical. Each delay path consists of a fixed delay of 100 ns less than 1H followed by a variable delay controlled by burst phase control circuits. This configuration compensates for initial tolerances of the glass delay line and for changes in it that occur with temperature. The path also includes automatic gain control, so that signals of opposing phases within the Y and chroma matrices will be completely cancelled out.

The 1H fixed delay is provided by an ultrasonic glass delay line that operates at 27 MHz. Therefore the Lt video is used to modulate a 27-MHz carrier, which is then applied to the delay line. Following the delay, the signal is demodulated.

The Lt video is applied to pin 1 of modulator U16. A buffered 2Fy (27 MHz) carrier is applied to pins 7 and 8. Modulated output at pins 6 and 9 is applied to Q13 and Q14, which drive the 1H delay, DL1, via transformer 2T. The delayed output drives the U13 demodulator circuit via transformer T1. Differential op amp U13-6,7 applies the delayed signal to a diode detector circuit consisting of CR6, CR7, and T7. The demodulated signal is filtered by L13 and L14.

This variable delay circuit includes transistor Q10 and an LC delay consisting of L15-L18 and the CR2-CR5 varicaps. Back biasing of the varicaps by burst phase comparison circuits controls the delay in a range of 20 to 60 ns. (Additional fixed delays occur in the modulation and demodulation circuits.) The orientation of the varicaps, with two in each direction, cancels distortion effects due to the non-linear varicap characteristics.

The 1H delayed signal is applied to the dc restore circuit. A high gain amplifier, U12, is clamped to ground at back-porch time, restoring video dc level. The inverted clamp pulse closes switch U39-13,14, applying the output level to U14-5. A ground level corrected for input offset is applied to U14-6. Any U14-5 error voltage, held at C84, drives the circuit in a direction to clamp the output to ground.

The U12 amplifier applies the Lm signal output to the Y and chroma matrices. This signal is also compared to the clipped sync reference level, to provide AGC feedback. An inverted sync pulse closes switch U9-3,4, sampling the clipped sync level that occurs at test point 12. This level is compared to the Lm level at U15-2,3. The U15 output is enabled at sync time via Q12. An error voltage held at C81 is applied to Q11, which in turn adjusts the gain of amplifier U13 in the demodulator. The Lm signal is therefore referenced to a level established by the sync clipper, as is the Lt signal.

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Precise control of the variable delay circuit is provided by the burst phase control circuits. These circuits phase the Lm and Lb signals to the burst of the Lt signal. These circuits are (refer to Figure 5-4):

- Chroma limiter
- Burst phase switch control
- Burst limit
- Phase error detect

The Lt signal, at TP12, is applied through the chroma limiter op amps, U8, to the burst phase switch control circuit. This circuit consists of two U19 ECL flip-flops and transistor switch Q15/Q16. Following the trailing edge of the CLAMP pulse, the U8-limited burst signal clocks U19-2, which then clocks U19-15. This flip-flop is wired as a one-shot. The grounded (ECL high) D input always provides a high, which charges C133, resetting the flip-flop to produce a 120 ns pulse. The pulse turns Q16 on and Q15 off. Switch U23 (phase error detect circuit) is closed for 120 ns.

The phase error detect circuits are identical for the Lm and Lb signals. The Lm burst signal, limited by three U18 op amps, clocks U31-3. The D input goes high when U19-2 clocks U13-3. At 120 ns the switch opens; the negative-going U31-3 output at this point in time is stored at C139. This voltage provides a precise measure of the phase of the Lm signal. The sampled level is applied through U39 to control the variable delay circuit. (The COLOR PRESENCE signal from the Input Reference PWA must be present to close U39.) The sampled negative level is applied to back bias varicaps CR3 and CR5. The sample is inverted by U17-7 to back bias CR2 and CR4. Exact 1H delays are obtained by adjusting L23 (Lm) and L42 (Lb), in the burst limit circuits.

5-13 Y and Chroma Matrices

This circuitry, shown in Figure 5-5, includes Y and chroma matrices for the normal mode, Y and chroma paths for the adaptive mode, a subcarrier detect circuit, and output select circuits. When a given level of subcarrier is detected, indicating Lt and Lb are out of phase, the Y and chroma adaptive mode paths are selected.

5-14 Y Matrix. The normal mode Y matrix includes wideband and narrowband circuits, the outputs of which are combined. As described in paragraph 5-9, the basic Y (wideband) matrix affects the vertical resolution of the image; the Y output includes weighted values of three successive lines (Figure 5-3c). In the chroma region, approximately 2 to 4 MHz, this is a necessary tradeoff for the combing out of all chroma components. However, the Y resolution below the chroma region is similarly affected in passing through the wideband matrix. Loss of resolution in this range is not necessary, so the narrowband matrix/filter circuit is used to prevent it. This circuit restores the original one-line resolution of the Y spectrum below the chroma region. The resistor/inverter configuration of the narrowband circuit (Figure 5-5) is chosen to cancel out the wideband Lt and Lb components in the low-pass region (2 MHz) and double the Lm component, to restore the single-line Y resolution.

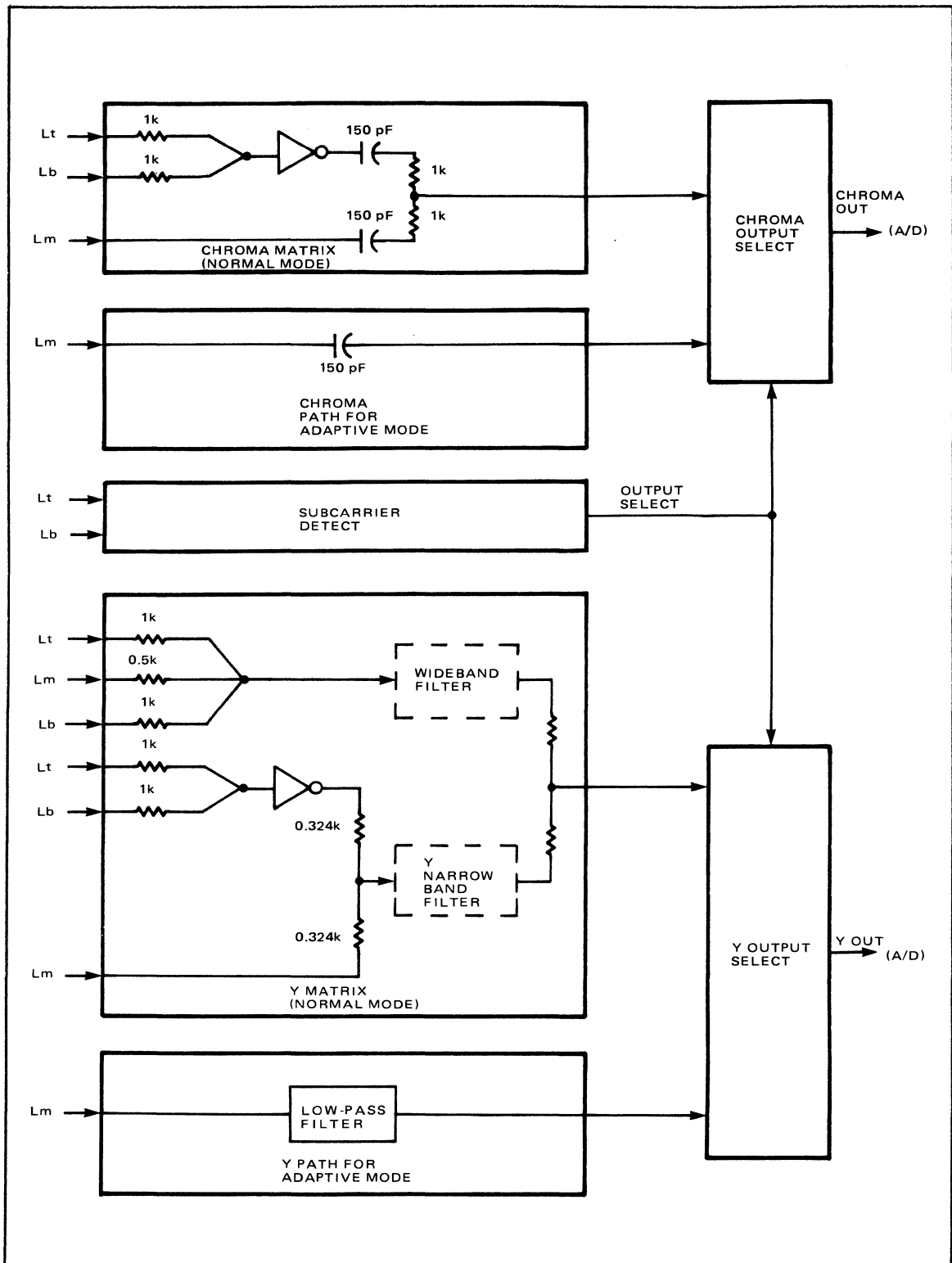


Figure 5-5. Y and Chroma Matrices

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Refer to schematic sheet 1. Lt, Lm, and Lb are passed through R195, R202, and R201 to the matrix summing point and applied to Q19 and Q20. As shown in Figure 5-3c, the luminance signal at this point consists of $Y_t/4 + Y_m/2 + Y_b/4$; the chroma components have cancelled out to zero. The Q19/Q20 outputs are first passed through DL2 and DL3 to provide a 250 ns delay. This compensates for delay time in the Y narrowband circuit, to line up the narrowband and wideband outputs.

The signal is then routed through the T9 and T8 phase equalizers. These circuits pre-equalize the signal for a low-pass filter at the output of the wideband circuit. Another phase equalizer, consisting of transistors U20-3, 6, and 9, and the associated RC network, provides equalization for DL2 and DL3. The wideband output is low-pass-filtered by L5-L7 and the associated capacitors. This circuit passes the luminance signal up to about 5.6 MHz.

The basic Y narrowband matrix/inverter configuration is shown in Figure 5-5. Lt and Lb are applied through R196 and R203 to U26-3. The transistor circuit inverts the signal, which is applied back to the R211/R213 junction. Lm is applied to the other end of the voltage divider. Therefore the signal out of the voltage divider, applied to R163, is $Y_m/2 - Y_t/4 - Y_b/4 +$ chroma terms. Although the chroma terms are all additive, they drop out because the signal is sent through a 2-MHz low-pass filter. R163 feeds the 2-MHz filter consisting of L29, L27, and associated capacitors. Phase equalization is provided by T3, L11, R99, and associated capacitors.

The narrowband output, applied through R98, combines with the wideband output to drive U11-2 in the normal mode. Output transistor Q8 provides the Y OUT signal at pin 14. Referring to Figure 5-3c, the wideband output in both the chroma region and below it is: $Y_m/2 + Y_t/4 + Y_b/4$. The 0 to 2 MHz narrowband output is: $Y_m/2 - Y_t/4 - Y_b/4$. Therefore, in the 0 to 2-MHz region the summed Y output is Y_m , restoring single-line resolution below the chroma region.

5-15 Chroma Matrix. Refer to the block diagram and schematic sheet 1. Lt and Lb are applied through R196 and R203 to the U26 transistor circuit, which inverts the summed signal. The inverted sum is applied through C156, which passes everything above 1 MHz, to R209. Lm components above 1 MHz are passed through C153 to R208. Referring to Figure 5-3c, the Y components cancel out, leaving $C_t/4 + C_m/2 + C_b/4$. This is applied to U37-9 to drive output transistor Q25, in the normal mode, providing CHROMA OUT at pin 30.

5-16 Subcarrier Detector. This circuit detects an out-of-phase condition between the Lt and Lb signals, causing switching from normal mode to adaptive mode. Lt and Lb are applied through high-pass RC inputs R263/C143 and R265/C151 to the inverting and noninverting inputs of ECL op amp U34-3. Any out-of-phase condition produces an output. The output is applied to a tuned circuit, R268/R267/C195/L47, which passes only the 3.58-MHz subcarrier. Op amp U34-6,7 drives transistors U35-9 and U35-3 via T6. The subcarrier is then filtered and a dc level is applied to comparator U36-3. When the reference level is exceeded, a low output is produced, switching the output select circuits to adaptive mode.

5-17 Adaptive Mode Circuits. Refer to Figure 5-5. The adaptive mode Y and chroma paths provide modified outputs that are preferable to those obtained from out-of-phase Lt and Lb signals. In the chroma adaptive path, Lm is applied through C154 and R275 to U37-2. Frequencies below 1 MHz are rejected by this RC input, reducing much of the luminance input. U37-11 is off in adaptive mode, and U37-2 is on. The inverted Lt + Lb sum is also applied to U37-2 through about 6K of resistance, R209, R208, R281, and R284. This further decreases the remaining luminance input of Lm. The resulting signal drives Q25, via U37-2, to produce the adaptive chroma output.

In the Y adaptive path, Lm is applied through R162 to a 2-MHz low-pass filter to remove all chroma (and high frequency Y). The filter and phase equalizer circuit, L26, L28, L9, T11, and associated components, is identical to that used for the narrowband portion of the Y matrix. In the adaptive mode, U11-3 is turned off, turning U11-2 off and turning U11-9 on. The Y path output is applied to U11-9 to drive output transistor Q8, providing a Y OUT signal of 2-MHz bandwidth.

5-18 Input Reference

The two main functions of this PWA are generation of video timing signals and demodulation of the chroma components. Separate block diagrams are presented for the descriptions of these two functions. The timing signal circuits are shown on sheet 2 of schematic 1420077. The demodulation circuitry is shown on sheet 3.

5-19 Video Timing Signals

The comb filter video output (Figure 5-6, and schematic sheet 2) is received at pin 26. VIDEO IN is applied through a buffer amplifier, Q1/Q2/Q3, to a low-pass filter consisting of L2, L3, and C4-C7. The video signal at test point 4 is applied to the video control circuit via the sync separator and is also applied to the sync sampling circuit. Block diagram circuits are described below.

5-20 Video Control. The sync separator circuit, Q5/Q6/U4, provides positive composite sync pulses (U4-12) to the video control circuit. This circuit consists of one-shots U5-13, U7-13, U7-5, U25-5, U25-4, and associated gates. These one-shots and associated gating provide the following control signals:

- The U25-12 output is gated (U37-11, U22-3) to provide a low-going 1.9- μ s CLAMP pulse that begins 0.5 μ s after the trailing edge of sync. This is used by the Comb Filter PWA for back porch clamping. A low-going 820 μ s pulse from U25-4 disables CLAMP during approximately the first thirteen lines of vertical blanking. U25-4 is triggered by the first narrow sync pulse (U17-5), during the 3.4 μ s output of U19-5.
- The U25-12 output is also inverted, to provide a positive 1.9 μ s BURST GATE pulse that begins 0.5 μ s after the trailing edge of composite sync.
- U5-4 controls the DS1 LED, holding it OFF if sync is present at least once every 470 μ s.
- The gated U7-13 output provides a low-going 1.3 μ s pulse, SYNC STROBE, coincident with the composite sync output. This signal is also disabled during the first thirteen lines of vertical blanking.

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- The U7-5 output is inverted to provide a low-going 0.5 μ s pulse, also called CLAMP, that begins at the trailing edge of composite sync. This pulse is used only in the A/D converter chroma feedback circuit, for clocking.

5-21 Sync Sampling. The VIDEO IN sync is used to phase the 27-MHz oscillator, which provides basic timing for the analog and digital systems. A very accurate determination of sync timing is required. The sync sampling circuit provides this by sensing the midpoints of the leading and trailing edges of sync.

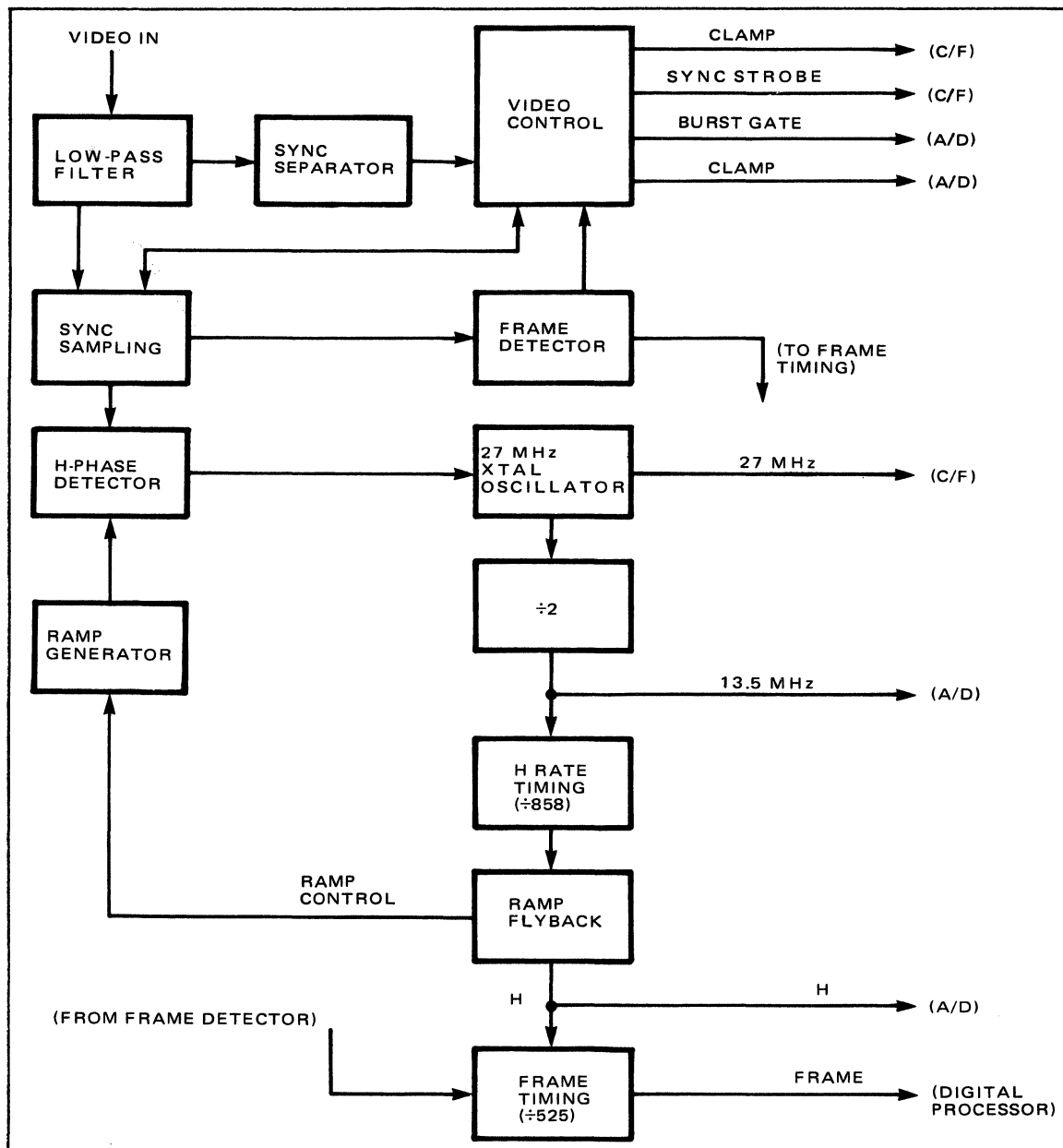


Figure 5-6. Video Timing Block Diagram

Sync tip voltage at TP4 (less dc drops) is sampled by C16 via switch U6, pins 1 and 15. A positive composite sync pulse at U7-13 actuates the switch. At back porch time pins 3 and 4 are switched by a 1.9 μ s burst gate pulse from U25-5; C15 samples the top of the sync pulse (less dc drops). The two samples are routed through op amps to the R32/R33 voltage divider, to apply a 50% reference value to U17-2. At the next sync pulse, U17-7 switches low as the sync pulse (less dc drops) passes its midpoint voltage. Similarly, U17-7 switches high as the sync trailing edge passes the midpoint value. The regenerated sync at U17-7 is applied to the frame detector circuit. The U17-5 inverted pulse is used to clock U25-1 in the video control circuit.

The U17-5 inverted output also triggers one-shot U18-6, which drives the H-phase detector. The one-shot provides a 42 μ s output, to eliminate 2H pulses; during vertical blanking alternate narrow or broad pulses are ignored. When U18-6 goes high, an RLC delay holds U28-9 low for about 40 ns, providing a positive H rate pulse to the H-phase detector.

5-22 Frame Detector. The purpose of this circuit is to count the six pre-equalizer pulses each vertical blanking time, to produce a reset load pulse for the frame timing circuit. Regenerated sync pulses from U17-7 are applied to serial shift register U20 and to one-shot U19-9. The trailing edge of the U19-12 pulse clocks U20 3.4 μ s later; only narrow sync pulses (2.3 μ s) cause ones to be shifted into U20. The six pre-equalizing pulses cause all ones to be applied to U26, and U26-8 goes low. At the next sync pulse this low is clocked into U27-2, and the trailing edge of U18-1 clocks the resulting high into U27-12. This applies a reset pulse to the frame timing circuit. Also, the first broad pulse drives U26-8 high, clocking U19-2. A 700 μ s low-going output at U19-4 holds U26-8 high for about eleven lines, so post-equalizing pulses won't produce a reset.

The U19-5 output is used by the video control circuit, at U25-2. The 3.4 μ s output is clocked into U25 only by the first pre-equalizing pulse; H sync pulses are too wide to clock it in. The 820 μ s output at U25-4 lasts almost thirteen lines. This one-shot isn't triggered again until the start of the next vertical blanking interval.

5-23 H Phase Detector. The H-phase detector compares the phase of the H-rate reference from the sync sampling circuit with the phase of a 27-MHz oscillator feedback value. The H-reference pulse drives the Q7/Q8/T1 circuit. The output diode bridge is returned to a feedback-controlled ramp voltage at the Q10/Q11/C12 junction. Any phase difference produces a correction voltage, locking the 27-MHz oscillator to the reference H-pulse.

5-24 27 MHz Oscillator. The crystal-controlled oscillator uses varicap CR24 for phase correction. An error voltage from U8-7 controls the Q13 circuit to momentarily vary the CR24 capacitance. The 27-MHz output is routed to the Comb Filter PWA via an ECL line driver (U13). Also, U15-6 divides the 27-MHz output, and applies 13.5-MHz clocking to the H-rate timing circuit. The 13.5 MHz-signal is also routed to the A/D converter, via an ECL line driver (U13).

If input sync is lost for more than 470 μ s the U5-4 output closes switch 48. This grounds the R49/R67 junction, stabilizing the oscillator at a nominal input level.

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5-25 H Rate Timing. The H-rate timing circuit consists of counters U9-U11 and flip-flops U24-10. Inputs are wired for dividing the 13.5-MHz clock by 857, to produce a carry output at U11-15. Count 858 is used to reload the counters. The U24-10 H-rate signal goes to the input reference demodulation circuit. The U24-11 output activates the ramp flyback counting circuit.

5-26 Ramp Flyback. This circuit controls the ramp generator, by digitally controlling transistor Q9 of that circuit, and also provides an H-reset output. The ramp flyback circuit consists of counters U31 and U32 and flip-flops U24-15, 2, 7 and U15-9.

The H-rate timing circuit presets U15-10 at count 858, and the ramp control output (U15-8) goes low. Counters U30 and U31 count to 131, which clocks U15-9 low, resetting the counters; the ramp control output (U15-8) goes high. During the counting a U30-12 H output occurs at count 64. This produces a 74 ns positive H reset output at pin 53.

Ramp flyback starts at count zero of U30/U31 and ends at count 131. The H reset output is set to occur at pin 53 when the midpoint of the ramp is reached. Flip-flops U24-15, 2, and 7 provide a timing delay.

5-27 Ramp Generator. The ramp generator provides an H-rate 4 Vp-p ramp, nominally centered at zero Volts. An H-phase adjustment circuit, consisting of potentiometer R192 and associated components, determines the level at which the ramp is centered. The ramp occurs at the Q10/Q11/C12 junction, applying a feedback level to the H-phase detector diode bridge. At count zero of the ramp flyback circuit a low is applied to the base of Q9, turning Q10 on, and the ramp starts down (flyback). At count 131 of the ramp flyback circuit a high is applied to the Q9 base, turning Q10 off. The ramp starts up from the -2V level, reaching a +2V level at count 858 of the H rate timer. When the oscillator is phase locked, the H reference pulse at Q7 occurs as the ramp flyback crosses the zero level. The H reset signal at pin 53 occurs at this time too.

5-28 Frame Timing. Frame timing counters U1-U3 are clocked by the H-rate signal from the ramp flyback circuit. Inputs are wired for divide by 525. A frame output is applied to U23-2 and is clocked 74 ns later. The 63.5 μ s positive FRAME pulse from ECL driver U29-14,15 is routed to the digital processor. The frame rate counter is initialized by clocking of a load pulse initiated by the frame detector. Subsequent load pulses are supplied by the frame outputs.

5-29 Demodulation

Chroma input from the comb filter (Figure 5-7, and schematic sheet 3) is received at pin 30. CHROMA is applied through a band-pass filter, L8-L10, C54-C60, and associated components, to reject noise. From test point 1, the chroma signal is applied to the burst limit and gate circuit, via R82. The chroma signal is also applied to the B-Y and R-Y demodulators, via Q16/Q17. The block diagram circuits are described below.

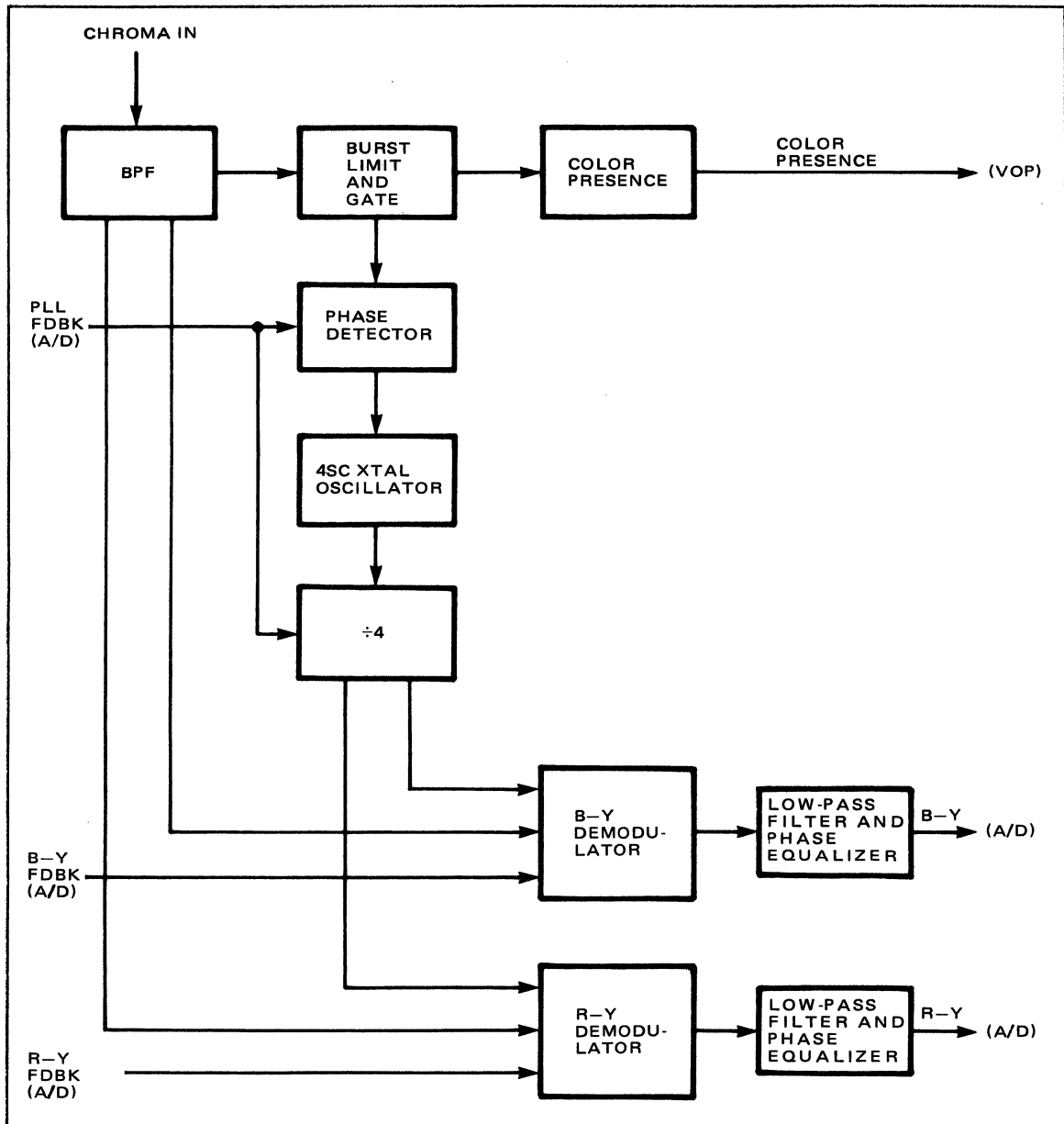


Figure 5-7. Demodulation Block Diagram

5-30 *Burst Limit and Gate.* This circuit passes two color burst cycles to the phase detector, for use in phasing the 4SC oscillator. The burst cycles are limited by U33-6,7 and are gated by the U37-8 output. The gating logic consists of shift register U39, U37-8, U32-5,7, and inverters. Shifting is clocked by burst cycles via U32-7. Input pin 1 of the shifter is normally high. Input pin 2 is high during burst gate time (except in the first thirteen lines of the vertical interval). Therefore U37-8 is low between the fifth and seventh burst cycles (positive transitions). This gates two cycles of the color burst (U33-7). The sampled cycles are applied through U33-2,3 and Q24/Q25 to T5 of the phase detector.

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5-31 Color Presence. The U32-5 output is strobed by the BURST GATE pulse. The resulting color burst output pulls C123 low. This point normally remains low, because of the 100 ms time constant, providing a continuous low at U36-6. The DS4 LED is held off, indicating that burst is present. A positive COLOR PRESENCE output occurs at pin 79.

5-32 Phase Detector. The limited burst cycles applied to the Q24/Q25 circuit provide narrow sampling pulses at T5. The U35-14 feedback signal is applied to the Q20 circuit, producing a sine wave. This sine wave is phase shifted by the Color PLL Feedback signal from the A/D converter and is applied to the diode bridge. It is sampled by the T5 narrow pulses, producing a phase error voltage. This is fed to the 4SC oscillator, phase-locking it to color burst.

5-33 4SC Crystal Oscillator. The 4SC oscillator circuit is configured in the same way as the 27-MHz oscillator (schematic sheet 2). Any error voltage at TP6 controls the CR26 capacitance, locking the oscillator to the sample color burst cycles. Since a 4SC frequency is provided, the U35-2 and U35-15 flip-flops apply subcarrier pulses to the two demodulators at exactly a 90° phase difference.

5-34 B-Y Demodulator/LPF/Phase Equalizer. The U35-3 subcarrier output is applied via transformer T4 to pins 7 and 8 of demodulator U34. The chroma signal is applied at pin 4. The demodulated B-Y output at pin 6 is fed through low-pass filter C68-C75/L15-L17 to remove harmonics. Phase equalization is then provided by the T3/L14 circuit. (Jumper J1 is normally removed; it is inserted only during factory test procedures.) Q18 provides output drive for the B-Y signal.

5-35 R-Y Demodulator/LPF/Phase Equalizer. The basic circuitry is identical to that for B-Y demodulation. (J3 is normally removed; it is inserted only during factory test procedures.) However, the subcarrier output from U35-15 is phased exactly 90° behind the B-Y subcarrier. Also, this signal is applied through an additional transformer, T6, and a diode bridge, controlled to provide alternating 180° phase shifting in PAL usage. The B-Y and R-Y outputs at pins 60 and 64 are routed to the A/D converter.

5-36 A/D Converter

This PWA (Figure 5-8) converts R-Y, B-Y, and luminance inputs into 8-bit digital outputs and applies them to the digital processor. Y is sampled at the F_y rate, 13.5 MHz. Each chroma component, R-Y and B-Y, is sampled at $F_y/4$. The R-Y and B-Y outputs are multiplexed. Also, feedback signals for R-Y, B-Y, and a phase lock loop are generated and sent to the Input Reference PWA.

The R-Y, B-Y, and Y samples for digitizing must be coincident in time. However, in order that R-Y and B-Y can be multiplexed through an A/D converter IC, the R-Y analog input is delayed by one $F_y/2$ period, then digitized. In other words, B-Y is digitized and 148 ns later the R-Y sample originally coincident with that B-Y sample is digitized.

Also, because of a difference in propagation time, the Y analog signal is ahead of the chroma analog signal. Therefore Y is digitized and then stored in RAM for the delay time needed to line it up with the chroma outputs. The circuit blocks are described below.

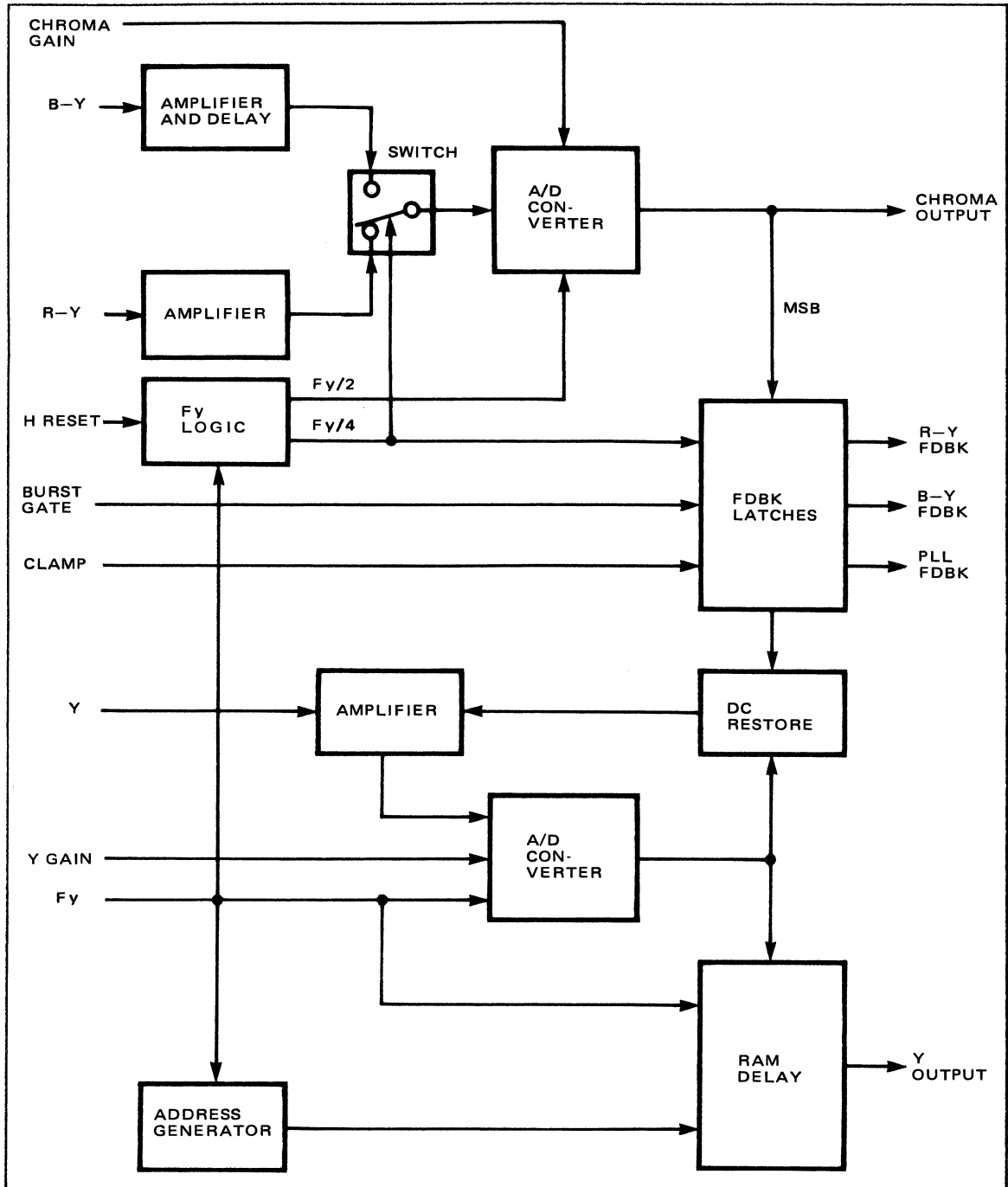


Figure 5-8. A/D Converter PWA

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5-37 Chroma Path

Refer to sheet 2 of schematic 1420070. The R-Y input, at pin 64, is applied to the Q16 buffer circuit then to a low-pass filter, L9/L10/C92/C76/C77. This filter also delays the signal by one $F_y/2$ period (148 ns). The U35/Q15 driver amplifier applies the delayed R-Y to the base of Q12, which drives A/D converter U28, via R94. Similarly, B-Y, at pin 60, is applied through a buffer and low-pass filter (no delay) to driver amplifier U19/Q9. This circuit drives Q11, to apply B-Y to the A/D converter.

Q11 and Q12 are alternately turned off, multiplexing R-Y and B-Y. The Q13/Q14 circuit, driven by an $F_y/4$ square wave from U24-2, turns Q11 and Q12 off for alternate 148 ns periods. A/D converter U28 receives an $F_y/2$ square wave from U29-13 at the CONVERT input, pin 30. CONVERT goes high, causing conversion, during the first 74 ns of each multiplexed R-Y and B-Y input time.

The U28 voltage reference input, pin 22, receives a CHROMA GAIN value from the video output processor. This gain value adjusts the digital output level as needed. The negative 6V supply input, at pins 47-50, is provided by the Q7/U18 regulator circuit. This circuit uses a +2V reference signal from the U13 voltage regulator IC. The Q7/U18 circuit also drives the Q6/U17 circuit, which provides a -2V reference level to the Video Output Processor PWA.

The 8-bit digitized outputs are applied through TTL to ECL differential drivers, U25 and U30, to the digital processor. One R-Y value and one B-Y value are provided during each 296 ns period.

5-38 Fy Logic and Feedback Latches

The F_y logic circuit consists of ECL flip-flops, U24, and ECL to TTL translators, U29. U24-15 is clocked at 13.5 MHz, from U8. The divide-by-two output drives the U28 CONVERT input, via U29, and clocks U24-2. The U24 $F_y/4$ output drives the Q13/Q14 multiplex switch and provides two square waves of opposite polarity to the feedback latches. The U24 flip-flops are reset each line by H RESET, pin 53.

The feedback latches use the most significant bit from U28 for R-Y and B-Y feedback. The bit is clocked each 148 ns, into U26-12 or U26-2, and applied to U27-12 or U31-12. These latter two flip-flops are clocked at back porch time, when the pin 39 CLAMP pulse goes low for 0.5 μ s. At this time the midrange chroma value should be just below the level at which the MSB goes high. The resulting feedback levels provide the correction needed at the demodulator outputs, on the Input Reference PWA.

BURST GATE provides clocking for the phase lock loop feedback level. The positive going BURST GATE pulse is clocked into shift register U20. At count eight, the chroma MSB is clocked into U27-5. The feedback signal is applied to the chroma phase detector, on the Input Reference PWA. The count eight pulse from U20 also clocks a clamp circuit in the luminance path, described below.

5-39 Y Path

The Y input at pin 14 is first applied to the U9 amplifier. (Note that the pin 14 Y input is designated F on some schematics.) The signal is amplified, low-pass-filtered, and applied to driver amplifier Q1/Q2/Q3, which drives the U5 A/D

converter. The U5 CONVERT input is enabled at the Fy rate. The digitized outputs are written into the delay RAM and are also used in a dc restore circuit.

The delay RAM consists of two 16 x 4-bit ECL register files, U7 and U16. The A/D converter outputs are applied to the RAM via TTL to ECL drivers U12 and U8. On the positive-going half of each Fy pulse at U1-9, the RAM read outputs are available. On the low-going half of each Fy pulse at U1-9, the read outputs are clocked into ECL flip-flops U6, U2, U14, and U10, and the next 8-bit byte is written into RAM.

The RAM addresses are generated by ECL counter U3. A hardwired value is applied to the D inputs to determine the delay period. The value of two, shown in the schematic, provides a delay of three Fy periods. After the hardwired two is loaded, the counter decrements at each count, and reloads on reaching the terminal count output. Therefore, during a read cycle, a byte is accessed three Fy periods after it is written into RAM.

5-40 DC Restore

This circuit consists of adders U4 and U16, flip-flop U15, and op amp U22-1. It clamps the Y dc level to a blanking value of binary 16 at back porch time. A signal from shift register U20-13, in the feedback latch circuit, provides the back porch timing pulse to clock U15-11. Adders U4 and U16 check the A/D converter Y level. A binary 16 produces a U16 carry, and flip-flop U15 provides a positive feedback to U9-2 in the Y amplifier. A value less than 16 produces a negative feedback, adjusting the gain as needed.

5-41 D/A Converter

The D/A Converter PWA (Figure 5-9) converts the transformed image data from the digital processor into analog signals and sends them to the video output processor. The D/A converter receives nine Y bits and eight multiplexed chroma/key bits. The ninth Y bit channel is time-shared by Y data and control unit information that includes Y gain, chroma gain, and SC phase values.

Because of differences in propagation times through the digital processor, the Y data is passed through a delay RAM to line it up with the chroma data. Also, the key analog output is passed through a 750 ns delay.

Refer to the D/A converter block diagram, Figure 5-9. The circuit blocks are described below.

5-42 Y Path

Refer to sheet 1 of schematic 1420426. The nine incoming Y bits are applied through ECL line receivers U28, U31, and U18 to the delay RAM. On the positive-going half of each 13.5-MHz pulse at U18-3, the read outputs are available at the U32 D/A converter inputs. On the low-going half of each clock pulse at U18-3, the RAM outputs are clocked into U32 and the next nine bits are written into RAM. The ninth bit is applied to U32 via U19-2, and requires a high MS DISABLE for gating.

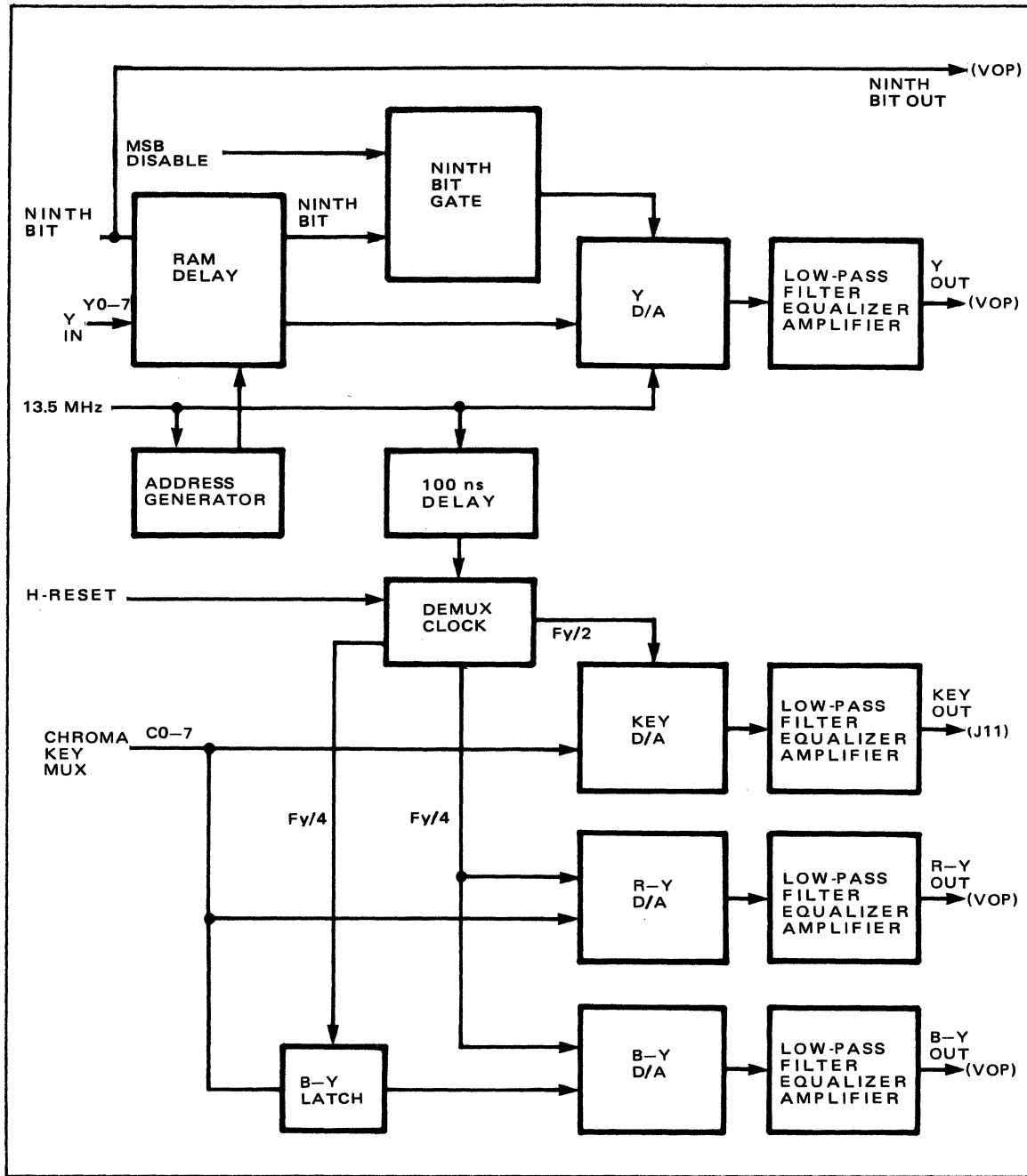


Figure 5-9. D/A Converter PWA

The RAM addresses are generated by ECL counter U17. A hardwired value is applied to the D inputs to determine the delay period. The value of eight, shown in the schematic, provides a delay of nine T_{74} ns periods. After the hardwired eight is loaded, the counter decrements at each count, and reloads on reaching the terminal count output. Therefore during a read cycle, a 9-bit RAM output is accessed nine clock periods after it is written into RAM.

The digital ninth bit, F1, is also routed to the vertical output processor, to provide computer information on Y gain, chroma gain, SC phase, and other system parameters. The information is sent during the last half of vertical blanking, between sync pulses. During this transmission, the U19-2 output is disabled, to block the data from the D/A converter. The rest of the time the ninth Y bit provides the extra digital range required to regenerate sync pulses.

The Y data is converted to analog at a 13.5-MHz rate. The U32 pin 7 output is passed through a 150 ns delay, DL3, and applied to a low-pass filter, C117-126/L14-16. It is applied through the L17/L18/T4 equalizer circuit to an output amplifier consisting of U38, Q1, and associated components. Y OUT, at pin 43, is routed to the video output processor.

5-43 Chroma Path

Refer to the D/A converter block diagram and to sheet 2 of the schematic. Eight chroma/key bits, C0-7, are received from the digital processor via ECL line receivers U6 and U8. The sequence of the multiplexed chroma/key data is key, B-Y, key, R-Y, key, and so forth, each data value occurring for 74 ns. The U11 demultiplex clock provides selection of the data at a 74 ns rate in the following sequence:

- Key is clocked into U23
- B-Y is clocked into delay latch U9/U3
- Key is clocked into U23
- R-Y is clocked into U14 and B-Y (delay latch output) is clocked into U7
- Key is clocked into U23

B-Y is delayed two intervals, 148 ns, so the B-Y and R-Y analog outputs will be coincident. The RESET signal, pin 62, provides a line reset to the clocking circuit.

The key analog signal, U23-7, is passed through DL1 and DL2, for a delay of 750 ns, to line it up with the chroma outputs. It is then applied through low-pass filter L11/L12 and associated capacitors and through the L13/L19/L20/T3 equalizer circuit. The U27 output amplifier provides the KEY OUT signal, pin 44, which is routed to the video output processor. Referring to sheet 2 of the schematic, it is seen that the R-Y and B-Y analog signals are passed through identical low-pass filter, equalizer, and amplifier circuits and routed to the VOP.

5-44 Output Reference

The Output Reference PWA (Figure 5-10) generates a 3.58-MHz subcarrier that is phase-locked to a reference black video input. The SC signal is applied to the video output processor for encoding the color difference signals. A composite sync signal is also generated from the reference black input. It is routed to the output control PWA, via the H processor, for possible use in comparing the ADO System phase and station reference phase.

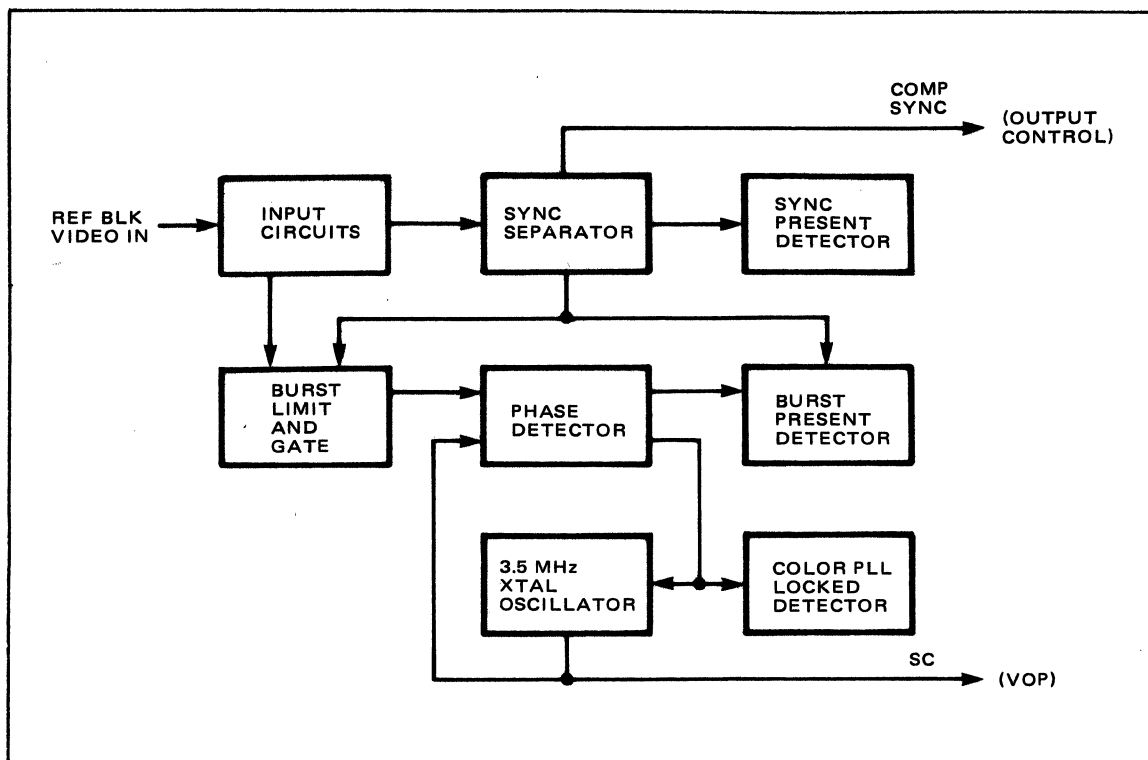


Figure 5-10. Output Reference PWA

5-45 Sync Separator

Refer to schematic 1420371. The reference black video input, pin 26, is applied through the U4 amplifier and a low-pass filter, L1/L2/C15/C16/C7, to the sync separator circuit. The low-going sync pulse at TP1 is applied through Q3 to a sync sampling circuit consisting of U12, U11-1, U11-7, and U7-7.

The sampling circuit provides an accurate determination of sync timing by sensing the midpoints of the leading and trailing edges of sync. The TP1 sync tip voltage is sampled by C23 via switch U12, pins 1 and 15. A positive composite sync pulse at U6-13 actuates the switch. At back porch time, pins 3 and 4 are switched by a 1.6 microsecond pulse from U2-5; C24 samples the blanking level. The two samples are routed through op amps to the R27/R28 voltage divider, to apply a 50% reference value to U7-2. At the next sync pulse, U7-7 switches low as the sync pulse passes the midpoint value. Similarly, U7-7 switches high as the sync trailing edge passes the midpoint value. The regenerated sync at U7-7 provides the COMP SYNC output, pins 30 and 29, via ECL line driver U17-2,3.

The TP1 composite sync pulse is passed through Q1 and Q2 and is inverted at U5-6. The trailing edge of this positive sync pulse triggers a 0.5 μs output at one-shot U6-5. The trailing edge of this one-shot output triggers the back porch output, U2-5, 12. The positive U5-6 sync pulse also triggers the sync present detector, U1-12. The 470 microsecond U1-12 output holds the DS2 LED off, indicating the presence of sync. DS2 remains off unless sync is missing for at least 470 microseconds.

5-46 Burst Limit and Gate

This circuit passes two color burst cycles to the phase detector, for use in phasing the SC oscillator. The reference black video input is applied to the circuit via the U4 amplifier and a bandpass filter consisting of L3-5 and the associated capacitors. Burst cycles are limited by U17-6,7 and are gated by the U9-8 output. Gating logic consists of shift register U8, U9-8, U13-7, and an inverter. Shifting is clocked by burst cycles via U13-7. A and B inputs are held low by the 1.6 μ s back porch pulse (U2-12) during the beginning of the color burst. Shifting begins when A and B go high, producing a U9-8 low-going output at counts 6 and 7. This gates two cycles of limited burst, which are applied through U17-15 to the Q4/Q5 circuit of the phase detector.

Also, the U13-5 output, strobed by U2-5 for 1.6 microseconds at back porch time, provides the burst cycles needed to indicate burst is present. The U13-5 output pulls C28 low. This point normally remains low, because of the 100 ms time constant. The DS1 LED is held off, indicating that burst is present.

5-47 Phase Detector

The limited burst cycles applied to the Q4/Q5 circuit provide narrow sampling pulses at T1. An SC feedback signal applied to the CR8-11 diode bridge is therefore sampled by the narrow pulses from T1, for detection of any phase error. A phase error voltage is applied to the SC oscillator circuit via U18-1.

5-48 3.58 MHz Oscillator

The crystal-controlled oscillator uses varicap CR12 for phase correction. An error voltage from U18-1 changes the CR12 capacitance, phase locking the oscillator to the reference input color burst. The Q6 output drives T2 to provide an SC signal to the video output processor, for composite video use. The Q6 output also provides the phase feedback signal to the phase detector.

If color burst is not present, U14-1 is low, and switch U12-12, 14 closes. This stabilizes the oscillator circuit at a nominal capacitance value.

5-49 Video Output Processor

The Video Output Processor (VOP) (Figure 5-11) receives the color subcarrier, encodes it with R-Y and B-Y, and combines chroma and Y to provide the ADO System composite video output. The PWA also receives computer data consisting of control unit values of Y gain, chroma gain, and burst phase. Refer to the VOP block diagram, Figure 5-11. The digital circuits are shown on sheet 1 of schematic 1420073. The analog circuits are shown on sheet 2. The VOP circuits are described below.

5-50 Digital Circuits

These circuits receive a data stream burst, via the bit 9 channel, during the last half of vertical blanking. Refer to schematic sheet 1. The data is applied through serial-to-parallel shifter U4, at a 13.5 MHz rate. Latching of successive bytes from U4 is initiated by 1010 coding of the four MSBs, A4-A7.

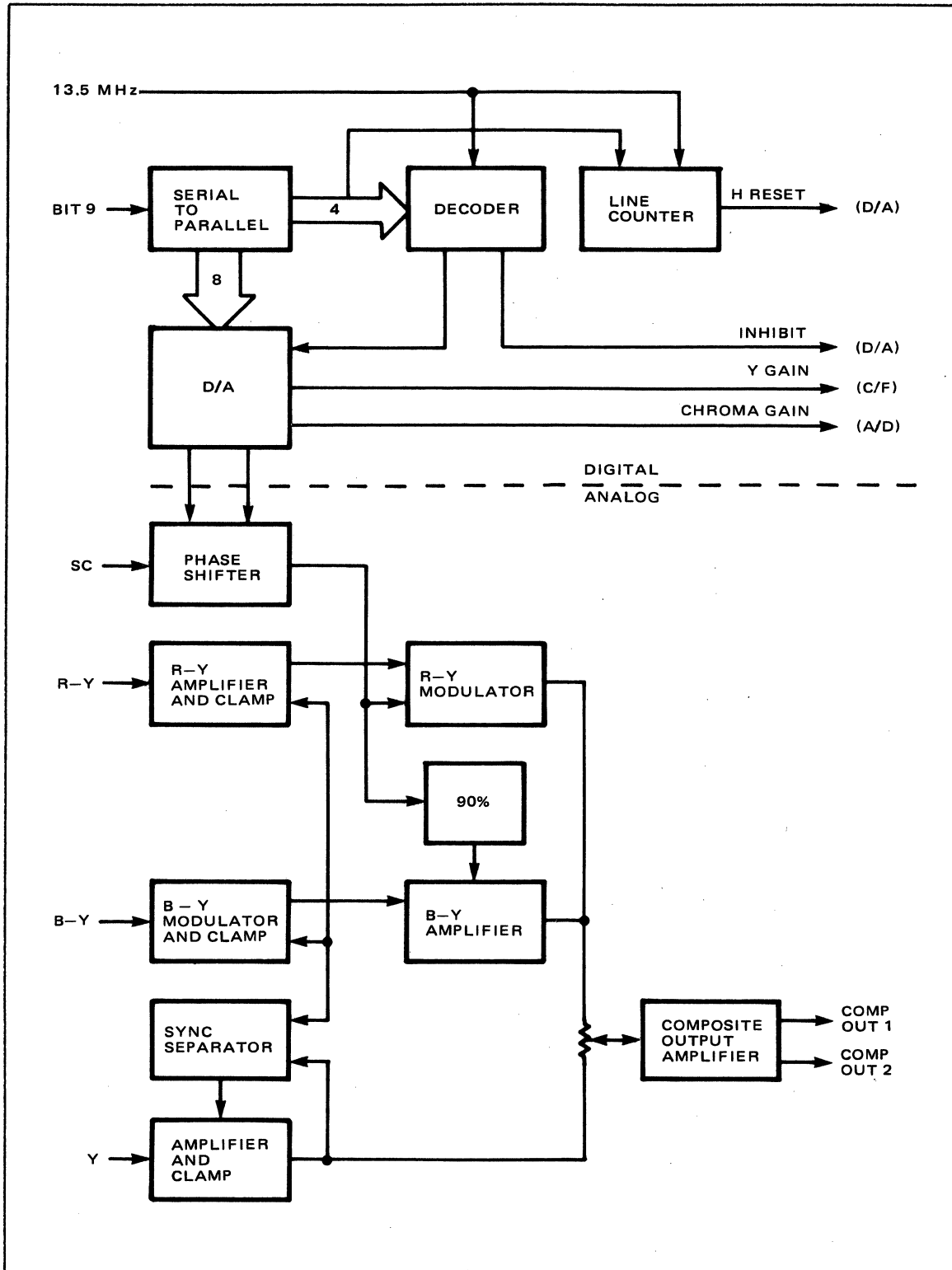


Figure 5-11. Video Output Processor Block Diagram

The decoding circuit consists of U1-8, counters U2 and U7, flip-flops U3, and decoder U9. A 1010 code produces a U1-8 output that loads counters U2 and U7 with preset values. The 13.5-MHz clocking sequences the U2/U7 outputs to drive the U3/U9 decoder circuit. Sequencing of latches U11-U15 stores the chroma gain byte in U15, the Y gain byte in U14, and the burst phase bytes in U13 and U12. These four latch outputs are applied to D/A converters U21-U18. Also, a video select bit, A7, is latched into U11 and applied to the comb filter via output pin 16.

The chroma gain analog value is sent to the A/D Converter PWA via U27-1. The Y gain analog value is sent to the comb filter via U27-7. A -2V reference level at pin 44 is provided by the A/D Converter PWA. The burst phase values are applied to the phase shifter circuit.

A carry-out signal from counter U7 provides a U3-5 pulse that is routed to the D/A Converter PWA via U23-7. This allows gating of the bit 9 Y data, on the D/A Converter PWA. During sequencing of U2 and U7 a low U3-5 output inhibits bit 9 Y data, on the D/A Converter PWA.

The U1-8 output also loads a divide by 858 line counter, U5/U10/U16, with preset values. An 857 output is applied from U38-8 to flip-flop U39-6, and produces an H RESET output at the 858th clock pulse. This resets the demultiplex clock on the D/A Converter PWA.

5-51 Analog Circuits

The color subcarrier from the Output Reference PWA is applied at pins 32 and 36 to T1. Line receivers U23 provide limiting of the SC signal. Transformer T2 applies SC to the carrier inputs of the sine synchronous detector, U24. The subcarrier is phase-shifted 90° by the L3/C121 circuit, and applied to the cosine synchronous detector, U25. Used in this way, U24 and U25 can phase shift the subcarrier by up to 360°, as controlled by the two burst phase values from the control unit. The merged U24/U25 SC output is applied through the T4 resonant circuit and through limiters U28 to T3.

The phased SC, at T4, is applied to the carrier inputs of the R-Y modulator, U31. Also, it is phase-shifted 90° by the L4/C76/C77 circuit and applied to the carrier inputs of the B-Y modulator, U35.

The R-Y input, pin 82, is amplified by the Q24-Q26 circuit and routed to the pin 1 signal input of modulator U31. The B-Y input, pin 84, is amplified by the Q46-Q48 circuit and routed to the pin 1 signal input of U35. Also, a 7.8-KHz input, pin 85, is applied to the Q41/Q42 switching circuit to provide PAL phase inversion when jumper J1 is in the PAL position. The B-Y and R-Y modulated signals are merged and applied through the Q62/Q63 amplifier to the chroma level control, R238, where it is combined with the luminance signal.

The R-Y and B-Y amplifier circuits include clamping of the color components during sync time. The U29-13 one-shot output from the sync separator circuit is a 1.9-μs positive pulse occurring at the leading edge of sync. It is used to strobe op amps U30-5 and U36-5, via Q60 and Q61. The op amps compare the circuit outputs

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to ground, when strobed. This generates correction signals to clamp the dc outputs to the chroma mid-level value. Switch U33 is also closed by the clamp pulse. This causes sampling of the clamped dc levels by C72 and C73. In conjunction with R235 and R237, these capacitors provide the modulator pin 4 signal inputs.

The Y signal, at pin 78, is amplified by the Q50-Q52 circuit and merged with the chroma signal, at R238. The amplified Y also drives the Q14-Q17 sync separator circuit that pulses U29-1 and U29-10. The U29-5 one-shot output is a 3.8- μ s positive pulse occurring at the trailing edge of sync. (Note that the pin 10 noninverting input is shown as inverting, on some schematics.) This pulse strobes U37-5 in the Y amplifier, each back porch time, causing clamping of the TP5 dc output to ground.

The VOP composite output amplifier, Q43-Q45, amplifies the merged Y and chroma signal. The signal is applied through the L5/C84 filter to output amplifiers that provide the ADO System COMP OUT 1 and COMP OUT 2 outputs.

5-52 CONTROL SYSTEM PWAS

These PWA descriptions are divided into the three functional groups of the control system: keyboard unit, menu monitor, and computer PWAs. Refer to Figure 5-1.

5-53 Keyboard Unit

This unit includes the Keyboard Switch Mounting PWA and the Keyboard CPU PWA. Functional and circuit descriptions are given below.

5-54 Keyboard Unit Function

The Keyboard Switch Mounting PWA (Figure 5-12) regularly scans the keyboard switches for closures. Each field time the Keyboard CPU PWA reads the switch closure data from the Keyboard Switch Mounting PWA. The CPP tells the keyboard CPU which keyboard lights to turn on; the keyboard CPU passes this data to the Keyboard Switch Mounting PWA. Meanwhile, the keyboard CPU continually receives X, Y, and Z axis analog signals from the control unit joystick, and converts them to digital form. The keyboard and joystick data is formatted by the keyboard CPU and sent in serial form to the Control Processor (CPP) PWA in the menu monitor, each field time.

5-55 Keyboard Switch Mounting

Refer to sheet 2 of schematic 1420183. The 48-switch keyboard is scanned by decoder U1 and keyboard interface chip U11 for switch closures. U11 is enabled (KEY) and clocked (AD CLK) by the keyboard CPU. It checks for switch closure ground levels on successive keyboard matrix rows. It sequences decoder U1, which applies a ground level to successive keyboard matrix columns. D0-D7 key closure data is read on the data bus by the keyboard CPU each field time.

Subsequently, the keyboard CPU sends switch lighting data (initiated by the CPP) to the keyboard light control circuit of the Keyboard Switch Mounting PWA. This circuit consists of three 8255A peripheral interface chips and nine Darlington

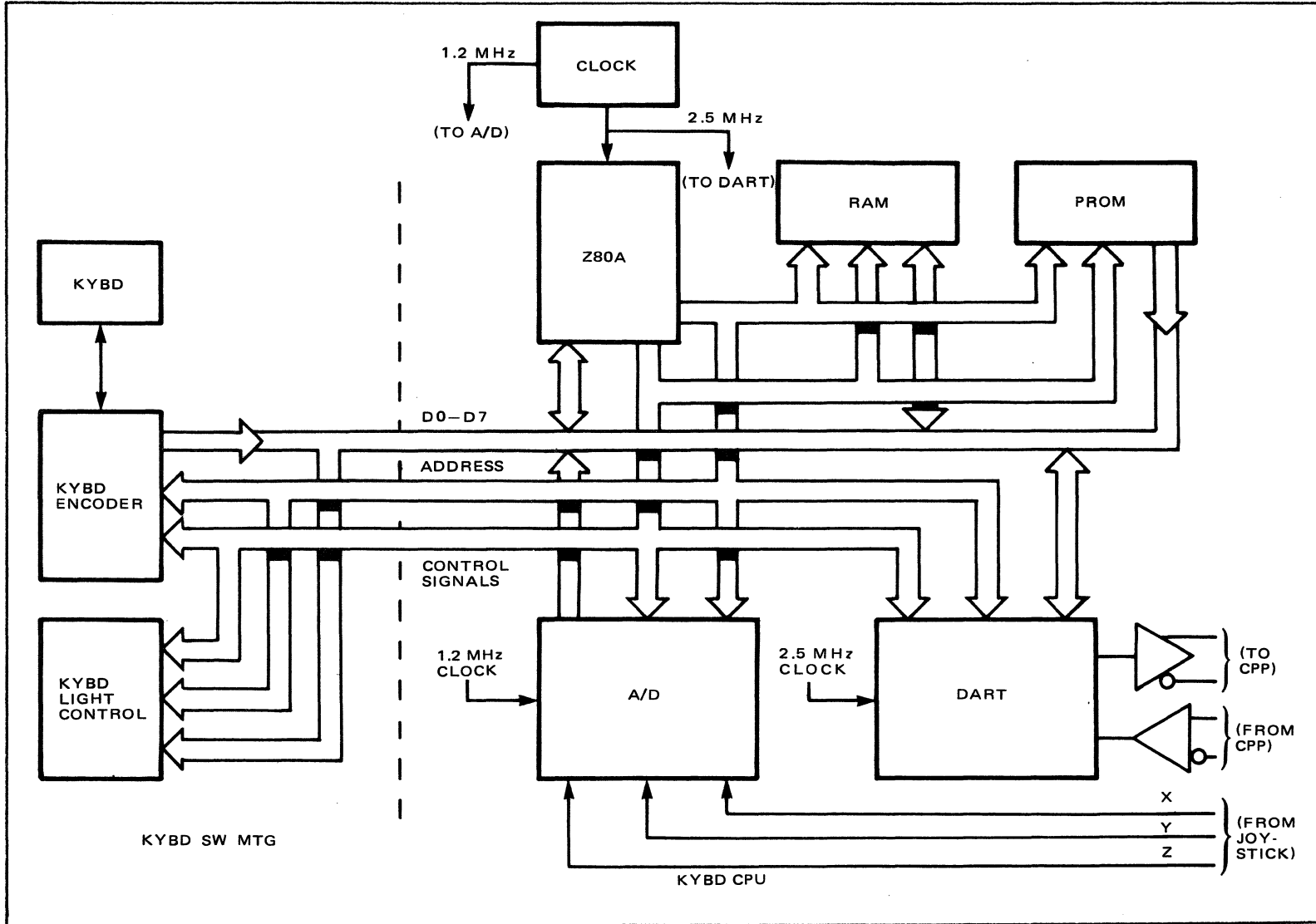


Figure 5-12. Keyboard Unit

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transistor arrays, U2-U10. The 8255As are enabled and controlled by signals from the keyboard CPU. U12-U14 drive the selected DS1-DS48 lights via the transistor arrays. A bright or dim illumination is selected by shunting or using the 300 ohm series resistor located at each light.

5-56 Keyboard CPU

Refer to sheet 2 of schematic 1420186. U8 is a Z80A 8-bit microprocessor. It receives keyboard data (keyboard switch mounting), digitized joystick data, CPP data from the DART (Dual Asynchronous Receiver/Transmitter), program instructions from the U5 EPROM, and data from the U3 RAM. Under control of the U5 program it formats keyboard and joystick data into data packets and applies them to the DART. The microprocessor and the DART are clocked at approximately 2.5 MHz. Pins 19-22, and 27, of the microprocessor provide control signals to cycle the DART, in transmit or receive mode. Two address bits from U8, A0 and A1, provide DART channel-select and control/data select inputs. The DART is wired for use of channel A only. Address bits A2-A4 and IORQ (Input/Output Request) are applied through decoder U20 to determine when the DART is enabled, by a low at pin 35. This decoder also provides the KEY and P1-P3 outputs used by the Keyboard Switch Mounting PWA.

The bidirectional data bus is passed by U21 under control of the microprocessor control outputs, gated by U18-11 and U17-8. Address drivers U6 and U7 and control signal driver U22 are wired for output mode only.

RAM U3 is a 2K-by-8-bit static memory. It is controlled via decoder U19 and the microprocessor write control output. U5 is a 4K-by-8-bit EPROM enabled via decoder U19. U4 is an optional 4K-by-8-bit PROM position for future use.

The A/D converter, U15, is addressed on three lines, A0-A2, for selection of up to eight analog inputs. Only three analog inputs, pins 26-28, are utilized. The X, Y, and Z axis inputs are multiplexed, to provide multiplexed 8-bit data outputs, D0-D7. Logic gating is provided for microprocessor address and control bits to start A/D conversion (U16-13) and to enable the output data (U17-6). The U15 A/D converter is clocked at one-fourth the microprocessor clock rate.

The keyboard CPU clock circuit consists of a crystal-controlled oscillator, U24, operating at 4.9152 MHz. A divide-by-two flip-flop output, U13-5, is inverted to clock the microprocessor at approximately 2.5 MHz. This signal is divided-by-two by counter U9 to provide the A/D clock rate of approximately 1.2 MHz. This signal is also routed to the Keyboard Switch Mounting PWA to clock the keyboard encoder.

5-57 Menu Monitor

The two menu monitor PWAs are the control processor (CPP) and input/output (I/O). These PWAs operate as a single functional unit, although two PWAs are required to hold all the circuitry. As shown in Figure 5-1, the CPP communicates with the keyboard unit. The CPP also communicates with the HLCs, via the I/O. Functional and circuit descriptions of the CPP and I/O are given below.

5-58 Menu Monitor Functions

In the Menu Monitor (Figure 5-13), the CPP and I/O functions are controlled by a processor system consisting basically of a Z8002 microprocessor, a program PROM and a 128K RAM. The primary function of the menu monitor PWAs is to send properly formatted keyboard unit data to the HLC, on a field basis.

A field update request from the HLC is received via the appropriate channel UART in the I/O, generating an interrupt to the Z8002. The processor responds by requesting keyboard unit status (keyboard and joystick selections), via the main keyboard UART of the CPP. The keyboard CPU then provides the data, in a format requested by the Z8002. The processor uses this data to update the key frame parameter list stored in the 128K RAM. This list determines the image transformations to be performed. The updated key frame data is downloaded to the HLC each field time.

The CPP and I/O also control the optional disk drive and update the menu monitor CRT.

5-59 Menu Monitor Control Processor (CPP)

As shown on sheet 2 of schematic 1464282, 6E is a 16-bit Z8002 microprocessor. Control inputs to the Z8002 include a WAIT signal (pin 23), a vectored interrupt, VI (pin 11), CLK (pin 30), and RESET (pin 14). The microprocessor outputs include a 16-bit bidirectional data bus, also used for addresses as well as status and control signals.

The wait logic, consisting of shift register 4E and associated gates, is used for functions that are too slow for the processor; a wait input indicates a memory or I/O device is not ready for data transfer. The WAITA and WAITB signals are applied from the I/O PWA. Wait inputs are also received from the program PROM and the EEPROM; these inputs are enabled by the processor memory request signal, MREQ. An interrupt, VI, is received from the I/O PWA; the processor responds with an interrupt acknowledge, VIACK, which is sent to the I/O. The 6-MHz processor clock is generated by a 12-MHz crystal-controlled multivibrator and a divide-by-two flip-flop, 7E. The 12-MHz signal is divided by three by counter 7F to provide the 4-MHz disk drive clock, FDCK. A one-shot provides the processor reset on power-up. The RESET signal also goes to the I/O PWA.

The Z8002 uses a bidirectional address/data bus in conjunction with an address strobe, AS (pin 29), and a data strobe, DS (pin 17). Flip-flops 7H and 6H are strobed to apply A0-A15 to the address bus. The direction of transceivers 6J and 7J is controlled to apply outgoing bits D0-D15 to the data bus or to apply incoming D0-D15 data to the processor.

Address bits A4-A15 and processor status outputs ST0-ST3 are applied to a programmable logic array, 5H, to provide a number of control signal outputs. Other processor control outputs are applied to inverters 5D and 5E and gates 5G, to provide additional control outputs as shown.

ADO

The program PROM, schematic sheet 3, consists of as many as sixteen 4K-by-8-bit 2532s. Decoder 5W selects pairs of 2532s, for reading 16-bit words, under control of two address bits and control signals from memory select circuits (schematic sheet 8). The 16-bit words are applied to the processor via the data bus.

The 64K RAM, schematic sheet 4, consists of sixteen 64K-by-1-bit 4164 memory chips, providing a 128K byte (64K 16-bit word) capacity. Addressing of 64K locations is done by sequentially strobing an 8-bit row address and an 8-bit column address. The address selection circuitry consists of memory drivers 3H and 3G, selectors 4G, 4H, and 3E, and their gates. This circuitry is controlled by address bits A0-A14 and control signals from the memory select circuits, schematic sheet 8. Data goes to and from the RAM via transceivers 3T and 4T.

The four CPP UARTs, schematic sheet 5, provide the data formatting and control needed to interface asynchronous serial data with the Z8002 processor operations. UARTs are provided for editor, main keyboard, auxiliary keyboard, and maintenance interfaces. The main keyboard UART, 5S, receives a data byte, D0-D7, from the Z8002 and transmits it serially via differential driver 5U. It receives serial data via differential receiver 4W and converts it to 8-bit bytes that are applied to the data bus. Chip selection is provided by decoder 3U, which is controlled by three address bits and the RAW URJP SEL control signal, from schematic sheet 2. A keyboard interrupt, SMP URJPINT, is generated when the UART receives serial data. This is applied to an interrupt control circuit in the I/O, which sends the VI signal to the Z8002 processor. Interrupts from two of the other three UARTs are gated with the interrupt from the keyboard to make the URJINT signal.

Refer to schematic sheet 6. Sixteen indicator LEDs are available for maintenance purposes. These indicators are only visible when the control unit cover is removed. Drivers 2U and 2P control these LEDs, directly from the data bus. Similarly, sixteen manual switches (1T and 1S) are available to provide logic inputs to the Z8002 via the data bus. The LEDs are primarily for development use. The manual switches are primarily for multichannel system use, providing system configuration data. The switches are also used for NTSC/PAL. The proper switch positions are identified in software release documentation.

Driver 2V is for use in receiving remote start control signals, REM1-REM3, and applying them to the data bus as D13-D15. Driver 2S applies an EE ROM BSY signal to the data bus as bit B0. All the drivers on sheet 6 are controlled from decoder 3U, sheet 5, and the processor data strobe, DS.

Refer to schematic sheet 7. The electrically erasable PROM, 2D, provides 2K X 8-bits of non-volatile storage for system setup parameters. Under control of the Z8002, updated parameter values can be written into the PROM when needed. Addresses are applied through flip-flops 1F and 2F. Data is written and read via transceivers 2B and 2C and flip-flop 1B. 21V programming pulses are provided by the 1A/Q1 circuit when enabled by one-shot 3A and the EE ROM EN signal.

The Z8002 controls the memory select circuitry, sheet 8, by means of the 16 data bus bits, one address bit, and control signals from schematic sheet 2. This circuit provides a means of extending the 16-bit address capability to handle 128K bytes of

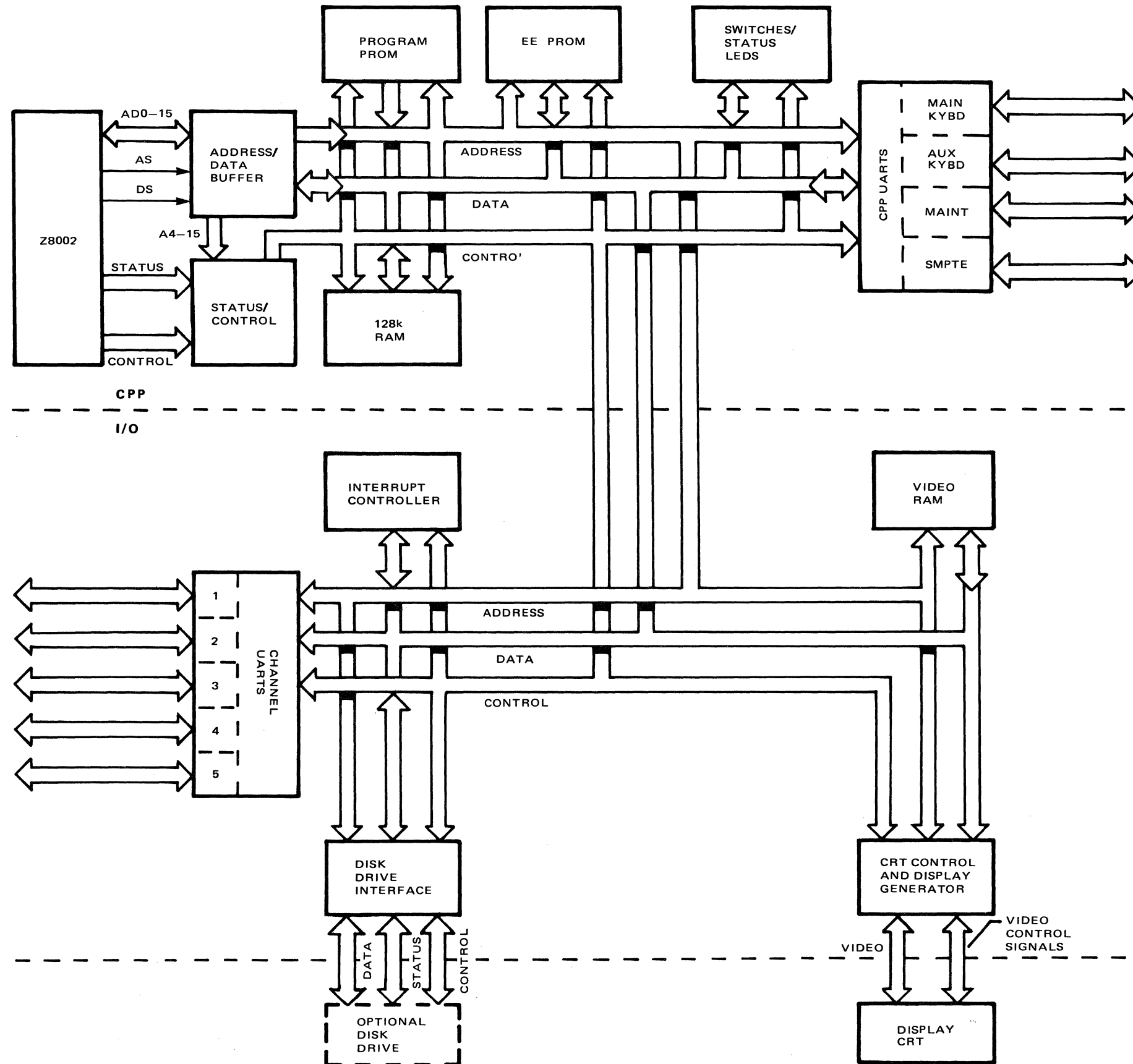


Figure 5-13. Menu Monitor

ADO

RAM and 66K bytes of PROM, including EE PROM 2D. The data bus bits are latched and applied to four 32-by-8-bit PROMs, 6A, 6B, 6C, and 7A. The output select signals are applied to the RAM, PROM, and EE PROM circuits.

5-60 Menu Monitor Input/Output (I/O)

As shown on sheet 2 of schematic 1420473, the I/O PWA connects to the Z8002 address and data buses, and receives Z8002 control signals. Drivers 1S and 1R buffer address bits A1-A11. Transceivers 1F and 1G buffer bidirectional data bits D0-D15. Directional control is provided by the 2U and 1T gate circuits.

Data bits D0-D7 are applied to a programmable interrupt controller, 5H, to set up the priority configuration for interrupts. This controller receives interrupts from the five channel UARTs (I/O PWA), from the SMPTE UART (CPP), and receives a gated interrupt, URJINT, from the three other CPP UARTs. The channel interrupts are from the various ADO systems used in a multichannel configuration. The interrupt controller produces wait and VI interrupts, which are routed to the Z8002. The Z8002 responds with a VIACK signal. On receiving VIACK the interrupt controller puts a code on the data bus that tells the processor which interrupt has occurred.

The processor writes display data into the video RAM, 5S and 5R. Each of these 2016P memories provides 2K-by-8-bit storage. The data bus is applied to video RAM via transceiver 4S, 3R, and 4R. The video RAM is addressed via selectors 2R, 2S, and 2T (schematic sheet 3); write mode uses address bus bits A1-A11, and read mode uses character counter and row counter outputs of a video timer and controller, 4P (sheet 3).

During read mode, VRAM SEL causes a WAIT2 signal at 4T-6 (sheet 2), preventing the processor from writing new data into the video RAM while reading is under way. Flip-flop 4T also provides an input to PROM 5T. The other 5T inputs are provided by a counter, 6S (sheet 3). The 5T outputs are latched in 6T to provide various control bits as shown (sheet 2).

Refer to schematic sheet 3. Drivers 1H, 1J, and 1K primarily buffer input control signals (from CPP). As shown, a few output signals (to CPP) are included: 6 MHZ CLK, WAIT0 (WAITA), and a gated WAIT1, WAIT2 signal (WAITB).

Sheet 3 also includes the video RAM address selectors 2R, 2S, and 2T, previously mentioned, and circuitry to drive the display CRT. This drive circuitry consists primarily of a video display generator, 5P, and a video timer and controller, 4P. The CRT8002 video display generator receives one video RAM byte (C0-C7) for addresses, and one byte (B8-B15) for video data. It also receives row addresses from the video timer and controller, 4P. The CRT8002 produces a VIDEO LEVEL output and a V SYNC output. The CRT5037 video timer and controller receives a control byte from the processor data bus via transceiver 3R (B0-B7). It also receives processor address bits A1-A4. The CRT5037 provides read addresses H0-H5 and DR0-DR3 for the video RAM and an H SYNC output. It also provides a composite sync output. This output and the CRT8002 video are applied through 1P to the Q1 circuit to produce a composite video signal at E1.

Refer to schematic sheet 4, which shows one of the five identical channel UART circuits. One UART is assigned to each channel in a multichannel system, for two-way communication with the control system. Four UARTs are designated for ADO channels and the fifth is designated for the combiner (concentrator). UART 4A is assigned to channel 1, as indicated at 4A pin 19. Sheet 3 also includes decoders 3G and 3H, which provide control signals from address bits A1-A4, and flip-flop 4F, which provides a divide-by-two clock signal. Flip-flop 2G provides enable signals for the five UART serial outputs. Flip-flop 5F applies a data byte, D0-D7, to all five UART circuits. Driver 3F applies UART status conditions to the data bus, as bits D4-D9. 2B also does this, using bits D8-D11.

In UART transmit mode, D0-D7 bytes are applied through flip-flop 5F (L0-L7) to a 128-by-9-bit FIFO, 5A. This frees the processor for other operations while the FIFO sequences the data bytes into the UART. Data is transferred to the UART by the 6A/7A sequencing circuit. The data is serialized by the UART and transmitted to the channel A system via differential driver 2A-14,15, if enabled by TO1.

In UART receive mode, serial data is received via differential receiver 1A-3. The DA (data available) UART output is activated, causing an interrupt via the interrupt controller, 5H (sheet 2). Under processor control, the UART then outputs the data in byte form, as D0-D7.

Schematic sheets 5 and 6 include the UART circuitry for channels 2-5. Circuitry is included for providing UART status to the data bus in the same manner as for the UART of sheet 4.

Refer to schematic sheet 7, which shows the disk drive interface circuit. The 1793 disk formatter/controller, 4L, receives data bytes D0-D7 and processor control signals. Transceiver 5L passes read and write data between 4L and the data bus. Controller 4L writes to the optional disk drive, and reads from it, serially.

The read clock is generated by an external-voltage-controlled oscillator, 2P. The 2P output is routed to the disk formatter/controller via the WD1691 support logic, 2L. The WD1691 compares the phase of the read data to that of the VCO and sends a phase correction voltage to the VCO. Also, a WD2143 four-phase clock generator, 2M, applies four clock phases to 2L. These inputs are used by 2L to generate precompensation signals, for writing to disk.

Miscellaneous circuits on sheet 7 include one-shot 4N, which receives timing inputs and applies a ready signal to 4L. Decoder 6P accepts control signals and three address bits to provide the FD1793 chip select signal. Flip-flops 4M provide 1-MHz and 2-MHz clock signals, for selection by jumper J12.

5-61 Computer PWAs

The computer PWAs consist of the High Level Controller (HLC) and the Low Level Controller (LLC). Functional and circuit descriptions are given below.

provided by gated WAITA and WAITB signals. The interrupt function uses a non-vectored interrupt, pin 12, NVI. The processor is clocked by a 4-MHz clock circuit (sheet 8), at pin 30. A power-on reset is provided by clock circuit 9R, wired as a one-shot.

Schematic sheet 3 shows the program PROM. At present, 16K bytes of program PROM are used. However, the PWA is wired for possible use of up to 64K bytes of PROM. Device selection is provided by decoder 6B, using two control signals and address bits A13-A15. On sheet 4, the 128K byte RAM uses the same memory chips and same general addressing scheme as described for the CPP RAM. Sequential strobing of 8-bit row and column addresses is performed in the same manner.

Refer to schematic sheet 5. Sixteen LEDs are available for indicating status conditions when the HLC is running. They are also available for maintenance purposes. The functions of these LEDs are described in Section 4 of this manual, in the troubleshooting paragraphs. Also, there are 16 manual switches (S1 and S2) available to provide logic inputs to the Z8002 via the data bus. The proper switch positions are identified in software release documentation.

Also on sheet 5, the FLD input at J1-160 is a field interrupt from the Output Control PWA in the digital processor. This produces an NVI REQUEST interrupt to the Z8002. The processor may examine the field signal via 1L, bit D9. The Z8002 responds with an interrupt acknowledge; RAW NVI ACK resets the interrupt logic, at 1F-13.

Driver 1L also receives a sequence of 14 bits via J1 pins 123-125, from the optional H phase counter, on the Output Control PWA. These bits are a measure of the phase difference between the ADO input and the output reference signal. They can be used to provide a precise phase correction, via data sent to the digital processor. An over-temperature indication from the address generator PWAs is received via J1 pin 126. Driver 1D receives various FIFO and UART signals (sheet 6) and passes them to the data bus. Drivers 1C and 1P each apply a byte of status data from the LLC to the data bus.

Schematic sheet 6 includes the UART (2B) and USART (5B) circuits. The 1854 UART is used for two-way communication with the CPP (via I/O PWA). It is clocked at 4 MHz, and operates at 153K baud. In transmit mode, data bits D0-D7 are applied to UART 2B, which transmits it serially via differential driver 2G-14, 15. In receive mode, serial data received via differential receiver 3F-3 is put into parallel form and applied from the UART receive bus, R0-R7, to FIFO 4B. The FIFO then sequences it onto the data bus in 9-bit form, D0-D8, including a parity bit. When serial data is being received, one-shot 2F-4 causes LED indicator DS1 to light. Similarly, DS2 lights during transmit mode.

The UART control logic consists of 3E/4E/4F/5F and associated gates. This circuitry is controlled by address bits A2 and A3, and control signals from the processor. Selection of the UART (or USART) causes shift register 5F to send WAITA, a wait signal, to the processor. For factory test, the UART output data can be circulated through 2G-14, 15 and 3F-2 (and a jumper) to feed it back into the UART.

ADO

The 5B USART, which is a synchronous/asynchronous device, provides an RS232C maintenance port. Data and controls are received via J1 pins 4, 6, and 8; data and controls are transmitted via J1 pins 1, 3, and 5. The USART interfaces with the data bus (D0-D7), receives processor control signals, and is clocked at approximately 2.5 MHz. Counters 6C and 6D accept a 2.5-MHz signal and provide 8 output frequencies as shown. Wire-wrap jumpering is used to select various UART and USART clock rates.

Schematic sheet 7 shows the multiplier and its control circuitry. Eight 8-bit 25LS14 multipliers are cascaded to provide 64-by-64 bit multiplication, generating a 64-bit product. The processor sequentially puts four 16-bit multiplicand words and four 16-bit multiplier words onto the data bus, loading two shift register strings in sequence. Shift registers 3M-2R then load the multipliers in parallel, a word at a time, via the data bus. The data in shift registers 5G-4K is entered via the serial inputs of each of the eight multiplier chips. The serial product output at 2L-6 is routed through adder/subtractor 4S, where it is combined with output bits from a control PROM, 4N, to provide rounding. The product is shifted serially into the 3M-2R shift register string, via 3M-11. The product is put on the data bus as four successive 16-bit words.

The shift register and multiplier controls are generated primarily by decoders 5L and 4L, from processor address bits and control signals. The clocking sequences required are generated by PROM 4N, which is sequenced by counters 5M and 4M.

Schematic sheet 8 includes the clock circuit and the output drivers. The Q2/Q3/Q4 crystal controlled clock circuit drives two counters, 3T and 4T, to provide the required HLC clocking signals. Driver 1J provides 8 address bits and 1H and 1G provide 16 data bit outputs. The resulting field rate outputs are applied alternately to the two LLC systems, one per field time, via the LLC shared RAM.

5-64 Low Level Controller

The Low Level Controller (Figure 5-15) consists of two identical sections, system 1 and system 2, and some common circuitry. The HLC sends key-frame/interpolated data to the LLC each field time, by applying it to the shared 4K RAM of Figure 5-15. The LLC can send status bytes from each of its two systems to the HLC. The two LLC systems communicate with each other via the shared 4K RAM. System 1 and the LLC common circuitry are described below.

The configuration of each LLC system is very similar to that of the HLC PWA. System 1 (refer to Figure 5-15) consists basically of a Z8002 16-bit microprocessor, a 4K RAM, a program PROM, and a 64-by-64 bit multiplier. Refer to sheet 2 of schematic 1464285. The AD0-AD15 data of system 1 is buffered by flip-flops 4E and 4G for address bits and by transceivers 4D and 4F for the bidirectional data bus. Z8002 control signals are buffered by driver 3J.

Schematic sheet 3 shows eight 2532 program PROMs per system. At present only 6 2532s are used, per system, providing 24K bytes of program PROM. The PWA is wired for possible use of up to 32K bytes of PROM per system. Decoder 10H provides chip selection, from three address bits and a processor control signal.

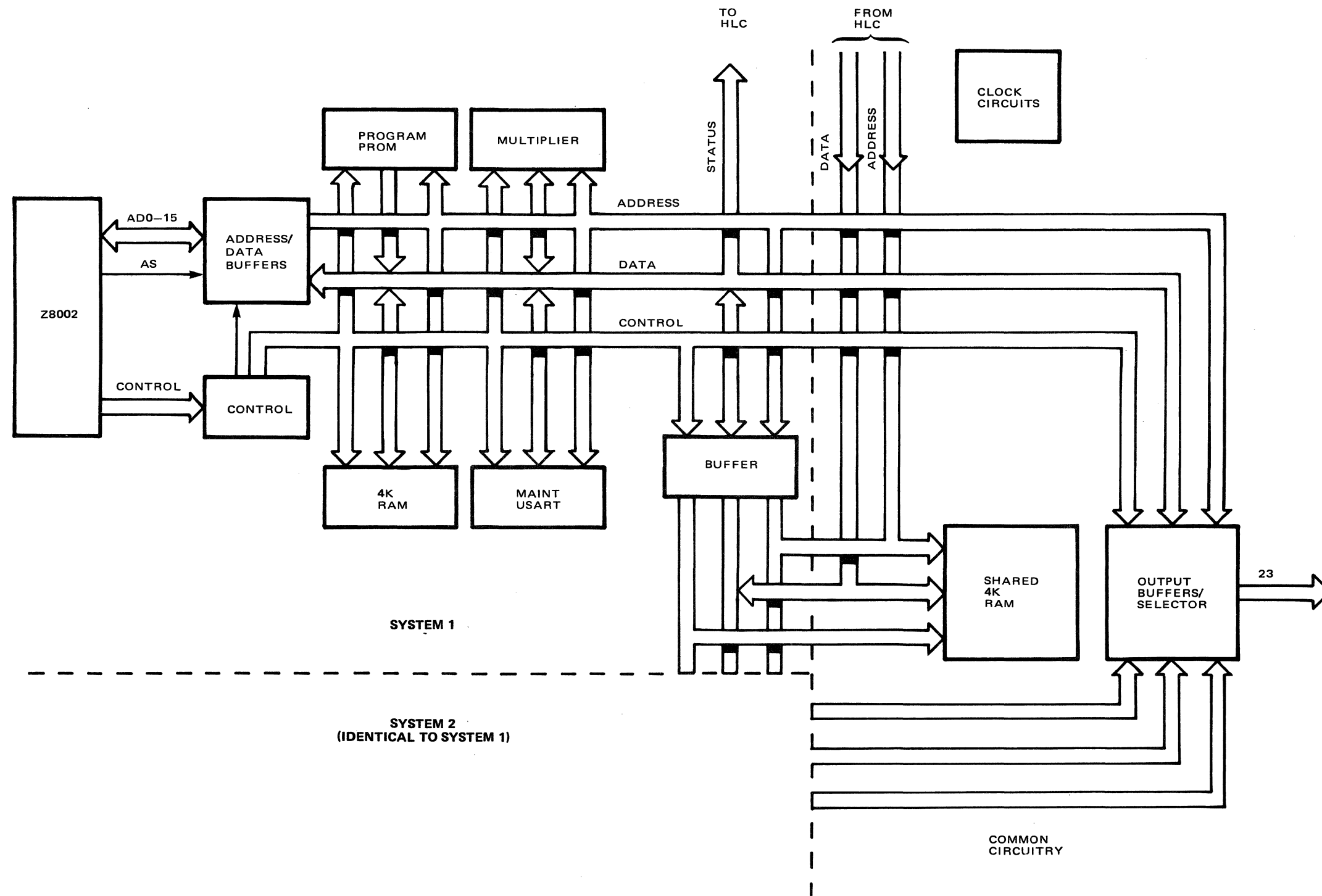


Figure 5-15. Low Level Controller

ADO

Schematic sheet 4 includes the 4K RAM, consisting of 10A and 11A. The control inputs include two processor control signals and the 1RAMS signal from decoder 10H (sheet 3). A maintenance USART, 4A, receives and transmits control inputs and serial data via J1 pins 1, 3, and 5. Its bidirectional 8-bit port connects to the processor data bus. The USART is controlled by the processor. Selectable USART clocking is provided by the sheet 9 common clock circuit.

Sheet 4 also includes data bus latch 5A, for driving status LEDs DS1-DS8. The functions of these LEDs are described in Section 4 of this manual, in the troubleshooting paragraphs. The status byte from 5A is also applied to the HLC, via J1 pins 9-16. Driver 5B applies four data bus bits, as control signals, to the shared RAM circuitry (sheet 8).

Four address bits and a processor memory request signal are applied to decoder 1A to generate control signals as shown. Shift register 2A applies a WAITA signal to the processor via gate 1C.

Refer to schematic sheet 6. Each LLC system uses a full 64-by-64 bit multiplier, during conversion of HLC data into control signals for the digital processor. The multiplier in each LLC system is identical to the multiplier used in the HLC PWA. Refer to the HLC PWA description.

Schematic sheet 8 includes the shared 4K RAM, consisting of 3F and 1G, and the associated input and output circuits. Data from the HLC, HLD0-HLD15, is buffered by drivers 1J and 1K and applied to the shared RAM. Addresses from the HLC (HLA1-HLA8) and control signals are buffered by 1H and 1L and applied to the RAM. Similarly, system 1 and 2 data and addresses are applied to the RAM as shown. System 1 and 2 communicate with each other by leaving messages in a designated portion of the shared RAM.

Systems 1 and 2 are clocked from the same clock circuit, shown on schematic sheet 2. This circuit is identical to that described for the HLC PWA. The LLC system timing allows only one or the other system to access the shared RAM at one time; priority logic is not required. However, the HLC PWA can access the shared RAM at any time, by sending a low HLCRTL signal, J1 pin 88. This disables the system 1 and 2 data and address inputs, and enables the HLC data and address inputs.

Sheet 9 shows the system 1 and 2 output buffers, and the selection logic. At each field time, alternately, one of the two LLC systems provides 16 data bits, 6 address bits, and a strobe signal. This 23 bit computer bus connects to most of the digital processor PWAs. The PWAs are addressed individually by the CA0-CA5 bits. Sheet 9 also includes counters 2B and 1B, which provide 8 USART clock frequencies, selectable by wire-wrapping.

APPENDIX A

VENDOR MANUALS AND ADDRESSES

The following assemblies are normally replaced as a unit. For service information on these units, contact the vendors directly.

Item	Unit	Vendor	Manual Number
1	CRT Monitor, 9 in.	C. ITOH ELECTRONICS, INC. 5301 Beethoven St., Los Angeles, Ca 90066 (213) 306-6700	Instruction Manual Spec. No. GK2-10-79
2	Disk Drive	TANDON MAGNETICS CORP 9333 Oso Avenue, Chatsworth, Ca 91311 (213) 993-6644	TM 100 Disk Drive Manual P/N 171024
3	Monitor Power Supply	BOSCHERT INCORPORATED 384 Santa Trinita Ave., Sunnyvale, Ca 94086 (408) 732-2440	
4	+12V Power Sup- ply, -5V Power Supply (Basic Channel)	POWER/MATE CORPORATION 1400 Coleman Ave. Suite E25 Santa Clara, Ca 95050 (408) 727-8118	

APPENDIX B

KRAFT JOYSTICK ASSEMBLY Kraft Part No. 900-034

The Kraft joystick is manufactured by:

Kraft Systems Inc.
450 W. California Ave.
P. O. Box 1268
Vista Ca 92083

Description:

This three-axis assembly has a square stick motion pattern for both the X and Y axis and a rotary Z axis knob. The Z axis potentiometer is built into the shaft of the joystick. All three axes use 5K ohms BOURNS conductive plastic potentiometers. All three axes are spring-loaded for centering. When the joystick is released, the gimbal and Z axis knob return to their center positions.

Assembly Details:

Figure B-1 is an exploded view of the joystick assembly. See Table B-1 for Kraft part numbers.

Table B-1. Three-Axis Gimbal Parts List

Item	Kraft Part No.	Quantity	Description
1	*	1	Knob
2	**	1	Socket setscrew
3	500-028	1	Spring, extension, 0.263 in. x 0.125 in.
4	850-042	2	Plate, butterfly
5	850-041	1	Washer, Teflon 5/16 in. OD x 1/8 in. x 0.005 in.
6	850-045	1	Spacer, 11/32 in. OD x 1/8 in. ID x 0.100 in.
7,9	106-013	1	Potentiometer/nut, 5K with 1/8 in. shaft
8	850-040	1	Collar
10	850-039	1	Pot housing
11	500-071	2	Socket setscrew 6-32 x 3/16 in.
12	850-015	1	Control stick housing
13	850-035	1	Stick & ball assy—hollow—short
14	850-017	1	Ball retainer
15	500-072	2	Roll pin 1/16 in. x 1/4 in.
16	850-044	1	Stick guide—bail end drilled for pin
17	500-007	4	Screw, No. 2 x 1/4 in. SMS
18	850-030	2	Bail pivot hinges
19	850-025	2	Bail to control pot coupling
20	850-026	1	Inside bail
21	850-027	1	Outside bail
22	850-024	1	Spacer - dog stop to bail
23	850-010	2	Washer, Teflon 1/2 in. OD x 1/4 in. ID x 0.005 in.
24	850-007	4	Dog stops
25	500-027	2	Spring—extension
26	500-016	2	Nut, 3/8-32 x 1/2 in. A.F. Hex
27	500-054	2	Washer, 5/8 in. OD x 3/8 in. ID x 0.025 in.
28	850-008	2	Brass bushing
29	500-011	4	Screw, No. 2 x 3/16 in. SMS
30	850-021	1	Control pot mounting plate No. 2
31	850-033	1	Adapter, pot to sideplate
32	850-019	2	Outer housing
33	850-018	2	Inner ring
34	500-073	2	Washer, 5/8 in. OD x 3/8 in. ID x 0.052 in.
35	106-027	2	Potentiometer, 5K conductive plastic

*Knob is Ampex Part Number 1420372
 **Setscrew is 2-56 x 0.050 in.

APPENDIX C

LUMINANCE CONVERSIONS

These are the 2s-complement luminance values for ADO in decimal, hexadecimal, and binary forms, and on the IRE scale.

Decimal	Hex	Binary	IRE	Decimal	Hex	Binary	IRE
-128	80	1000 0000	-6.6	-96	A0	1010 0000	+7.5
-127	81	1000 0001	-6.2	-95	A1	1010 0001	+8.0
-126	82	1000 0010	-5.8	-94	A2	1010 0010	+8.4
-125	83	1000 0011	-5.3	-93	A3	1010 0011	+8.8
-124	84	1000 0100	-4.9	-92	A4	1010 0100	+9.3
-123	85	1000 0101	-4.4	-91	A5	1010 0101	+9.7
-122	86	1000 0110	-4.0	-90	A6	1010 0110	+10.2
-121	87	1000 0111	-3.5	-89	A7	1010 0111	+10.6
-120	88	1000 1000	-3.1	-88	A8	1010 1000	+11.1
-119	89	1000 1001	-2.7	-87	A9	1010 1001	+11.5
-118	8A	1000 1010	-2.2	-86	AA	1010 1010	+11.9
-117	8B	1000 1011	-1.8	-85	AB	1010 1011	+12.4
-116	8C	1000 1100	-1.3	-84	AC	1010 1100	+12.8
-115	8D	1000 1101	-0.9	-83	AD	1010 1101	+13.3
-114	8E	1000 1110	-0.4	-82	AE	1010 1110	+13.7
-113	8F	1000 1111	0.0	-81	AF	1010 1111	+14.2
-112	90	1001 0000	+0.4	-80	B0	1011 0000	+14.6
-111	91	1001 0001	+0.9	-79	B1	1011 0001	+15.0
-110	92	1001 0010	+1.3	-78	B2	1011 0010	+15.5
-109	93	1001 0011	+1.8	-77	B3	1011 0011	+15.9
-108	94	1001 0100	+2.2	-76	B4	1011 0100	+16.4
-107	95	1001 0101	+2.7	-75	B5	1011 0101	+16.8
-106	96	1001 0110	+3.1	-74	B6	1011 0110	+17.3
-105	97	1001 0111	+3.5	-73	B7	1011 0111	+17.7
-104	98	1001 1000	+4.0	-72	B8	1011 1000	+18.1
-103	99	1001 1001	+4.4	-71	B9	1011 1001	+18.6
-102	9A	1001 1010	+4.9	-70	BA	1011 1010	+19.0
-101	9B	1001 1011	+5.3	-69	BB	1011 1011	+19.5
-100	9C	1001 1100	+5.8	-68	BC	1011 1100	+19.9
-99	9D	1001 1101	+6.2	-67	BD	1011 1101	+20.4
-98	9E	1001 1110	+6.6	-66	BE	1011 1110	+20.8
-97	9F	1001 1111	+7.1	-65	BF	1011 1111	+21.2

(Continued next page)

Luminance Conversions (Continued)

Decimal	Hex	Binary	IRE	Decimal	Hex	Binary	IRE
-64	C0	1100 0000	+21.7	-24	E8	1110 1000	+39.4
-63	C1	1100 0001	+22.1	-23	E9	1110 1001	+39.8
-62	C2	1100 0010	+22.6	-22	EA	1110 1010	+40.3
-61	C3	1100 0011	+23.0	-21	EB	1110 1011	+40.7
-60	C4	1100 0100	+23.5	-20	EC	1110 1100	+41.2
-59	C5	1100 0101	+23.9	-19	ED	1110 1101	+41.6
-58	C6	1100 0110	+24.3	-18	EE	1110 1110	+42.0
-57	C7	1100 0111	+24.8	-17	EF	1110 1111	+42.5
-56	C8	1100 1000	+25.2	-16	F0	1111 0000	+42.9
-55	C9	1100 1001	+25.7	-15	F1	1111 0001	+43.4
-54	CA	1100 1010	+26.1	-14	F2	1111 0010	+43.8
-53	CB	1100 1011	+26.5	-13	F3	1111 0011	+44.2
-52	CC	1100 1100	+27.0	-12	F4	1111 0100	+44.7
-51	CD	1100 1101	+27.4	-11	F5	1111 0101	+45.1
-50	CE	1100 1110	+27.9	-10	F6	1111 0110	+45.6
-49	CF	1100 1111	+28.3	-9	F7	1111 0111	+46.0
-48	D0	1101 0000	+28.8	-8	F8	1111 1000	+46.5
-47	D1	1101 0001	+29.2	-7	F9	1111 1001	+46.9
-46	D2	1101 0010	+29.6	-6	FA	1111 1010	+47.3
-45	D3	1101 0011	+30.1	-5	FB	1111 1011	+47.8
-44	D4	1101 0100	+30.5	-4	FC	1111 1100	+48.2
-43	D5	1101 0101	+31.0	-3	FD	1111 1101	+48.7
-42	D6	1101 0110	+31.4	-2	FE	1111 1110	+49.1
-41	D7	1101 0111	+31.9	-1	FF	1111 1111	+49.6
-40	D8	1101 1000	+32.3	0	00	0000 0000	+50.0
-39	D9	1101 1001	+32.7	+1	01	0000 0001	+50.4
-38	DA	1101 1010	+33.2	+2	02	0000 0010	+50.9
-37	DB	1101 1011	+33.6	+3	03	0000 0011	+51.3
-36	DC	1101 1100	+34.1	+4	04	0000 0100	+51.8
-35	DD	1101 1101	+34.5	+5	05	0000 0101	+52.2
-34	DE	1101 1110	+35.0	+6	06	0000 0110	+52.7
-33	DF	1101 1111	+35.4	+7	07	0000 0111	+53.1
-32	E0	1110 0000	+35.8	+8	08	0000 1000	+53.5
-31	E1	1110 0001	+36.3	+9	09	0000 1001	+54.0
-30	E2	1110 0010	+36.7	+10	0A	0000 1010	+54.4
-29	E3	1110 0011	+37.2	+11	0B	0000 1011	+54.9
-28	E4	1110 0100	+37.6	+12	0C	0000 1100	+55.3
-27	E5	1110 0101	+38.1	+13	0D	0000 1101	+55.8
-26	E6	1110 0110	+38.5	+14	0E	0000 1110	+56.2
-25	E7	1110 0111	+38.9	+15	0F	0000 1111	+56.6

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Luminance Conversions (Continued)

Decimal	Hex	Binary	IRE	Decimal	Hex	Binary	IRE
+16	10	0001 0000	+57.1	+56	38	0011 1000	+74.8
+17	11	0001 0001	+57.5	+57	39	0011 1001	+75.2
+18	12	0001 0010	+58.0	+58	3A	0011 1010	+75.7
+19	13	0001 0011	+58.4	+59	3B	0011 1011	+76.1
+20	14	0001 0100	+58.8	+60	3C	0011 1100	+76.5
+21	15	0001 0101	+59.3	+61	3D	0011 1101	+77.0
+22	16	0001 0110	+59.7	+62	3E	0011 1110	+77.4
+23	17	0001 0111	+60.2	+63	3F	0011 1111	+77.9
+24	18	0001 1000	+60.6	+64	40	0100 0000	+78.3
+25	19	0001 1001	+61.1	+65	41	0100 0001	+78.8
+26	1A	0001 1010	+61.5	+66	42	0100 0010	+79.2
+27	1B	0001 1011	+61.9	+67	43	0100 0011	+79.6
+28	1C	0001 1100	+62.4	+68	44	0100 0100	+80.1
+29	1D	0001 1101	+62.8	+69	45	0100 0101	+80.5
+30	1E	0001 1110	+63.3	+70	46	0100 0110	+81.0
+31	1F	0001 1111	+63.7	+71	47	0100 0111	+81.4
+32	20	0010 0000	+64.2	+72	48	0100 1000	+81.9
+33	21	0010 0001	+64.6	+73	49	0100 1001	+82.3
+34	22	0010 0010	+65.0	+74	4A	0100 1010	+82.7
+35	23	0010 0011	+65.5	+75	4B	0100 1011	+83.2
+36	24	0010 0100	+65.9	+76	4C	0100 1100	+83.6
+37	25	0010 0101	+66.4	+77	4D	0100 1101	+84.1
+38	26	0010 0110	+66.8	+78	4E	0100 1110	+84.5
+39	27	0010 0111	+67.3	+79	4F	0100 1111	+85.0
+40	28	0010 1000	+67.7	+80	50	0101 0000	+85.4
+41	29	0010 1001	+68.1	+81	51	0101 0001	+85.8
+42	2A	0010 1010	+68.6	+82	52	0101 0010	+86.3
+43	2B	0010 1011	+69.0	+83	53	0101 0011	+86.7
+44	2C	0010 1100	+69.5	+84	54	0101 0100	+87.2
+45	2D	0010 1101	+69.9	+85	55	0101 0101	+87.6
+46	2E	0010 1110	+70.4	+86	56	0101 0110	+88.1
+47	2F	0010 1111	+70.8	+87	57	0101 0111	+88.5
+48	30	0011 0000	+71.2	+88	58	0101 1000	+88.9
+49	31	0011 0001	+71.7	+89	59	0101 1001	+89.4
+50	32	0011 0010	+72.1	+90	5A	0101 1010	+89.8
+51	33	0011 0011	+72.6	+91	5B	0101 1011	+90.3
+52	34	0011 0100	+73.0	+92	5C	0101 1100	+90.7
+53	35	0011 0101	+73.5	+93	5D	0101 1101	+91.2
+54	36	0011 0110	+73.9	+94	5E	0101 1110	+91.6
+55	37	0011 0111	+74.3	+95	5F	0101 1111	+92.0

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ADO

Luminance Conversions (Continued)

Decimal	Hex	Binary	IRE	Decimal	Hex	Binary	IRE
+96	60	0110 0000	+92.5	+112	70	0111 0000	+99.6
+97	61	0110 0001	+92.9	+113	71	0111 0001	+100.0
+98	62	0110 0010	+93.4	+114	72	0111 0010	+100.4
+99	63	0110 0011	+93.8	+115	73	0111 0011	+100.9
+100	64	0110 0100	+94.2	+116	74	0111 0100	+101.3
+101	65	0110 0101	+94.7	+117	75	0111 0101	+101.8
+102	66	0110 0110	+95.1	+118	76	0111 0110	+102.2
+103	67	0110 0111	+95.6	+119	77	0111 0111	+102.7
+104	68	0110 1000	+96.0	+120	78	0111 1000	+103.1
+105	69	0110 1001	+96.5	+121	79	0111 1001	+103.5
+106	6A	0110 1010	+96.9	+122	7A	0111 1010	+104.0
+107	6B	0110 1011	+97.3	+123	7B	0111 1011	+104.4
+108	6C	0110 1100	+97.8	+124	7C	0111 1100	+104.9
+109	6D	0110 1101	+98.2	+125	7D	0111 1101	+105.3
+110	6E	0110 1110	+98.7	+126	7E	0111 1110	+105.8
+111	6F	0110 1111	+99.1	+127	7F	0111 1111	+106.2

AMPEX