5890 Functional Characteristics

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Revision Notice
This is the second edition.

Abstract
The *Amdahl 5890 Functional Characteristics* introduces the components and functions of these Amdahl 5890 uniprocessors and dual processors to management, programming, and operating personnel who are familiar with the following:

- *IBM System/370 Principles of Operation*
- *IBM System/370 Extended Architecture Principles of Operation*
- The concepts of virtual storage and virtual machines

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For Further Information
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Preface

Purpose
This manual defines the technical product specifications and functional characteristics of the Amdahl 580 Series 5890-190E Uniprocessor, and 5890-200E and 5890-300E Dual Processor systems.

Audience
This manual is intended for data processing technical management, operations management and senior computer operators, systems programmers, applications programmers, and hardware planners.

Related Publications
A list of related publications is contained in the bibliography.

Chapter Summaries

Introduction
Chapter 1 provides a brief system overview, lists characteristics of the Amdahl 5890-190E, 5890-200E and 5890-300E, and provides physical and functional descriptions.

Technology and Packaging
Chapter 2 provides information concerning logic, random access memory (RAM), and register chips, multiple chip carriers (MCC), and dual processor stacks.

System Director
Chapter 3 describes the system director.

Central Processing Units (CPU)
Chapter 4 discusses the major functions of the 5890 CPU. It also gives information concerning the CPU functional units.

Main Storage Unit
Chapter 5 discusses the logic portion of the main storage unit and includes the key facility and the switchbox.

External Director
Chapter 6 discusses the external director and its functions.

Channel Subsystem
Chapter 7 discusses the channel subsystem components and their relationship to the external director.

Console Subsystem
Chapter 8 describes the 5890 console subsystem.

Macrocode
Chapter 9 provides information concerning Macrocode.

Optional Features
Chapter 10 provides information on optional 5890 features.

Appendices
Appendix A describes the processor features and their applicability to System/370 and 370-XA modes. Appendix B categorizes feature availability by processor model.

FIGURE 1-1 5890 Uniprocessor or Dual Processor Computing System

1 Introduction

This section provides a brief system overview of Amdahl's 5890 uniprocessor and dual processor systems (figure 1-1). It lists characteristics of these processors and provides physical and functional descriptions. It also discusses physical planning requirements and system compatibility, giving standard and optional features and describing reliability, availability, and serviceability.

The Amdahl 5890 family consists of the 5890-190E Uniprocessor, the 5890-200E and 5890-300E Dual Processors, and the 5890-400E three-way and 5890-600E four-way Multiprocessors. These processors provide high-speed, general-purpose computing capabilities for business and scientific applications. They are a logical extension of the Amdahl 580 Series. Advanced design concepts and the application of Mācrocode and distributed microcode techniques allow Amdahl to meet the needs of the large-system user with unique but compatible solutions.

1.1 Characteristics

The following list highlights the characteristics of 5890 uniprocessor and dual processor systems:

- 5890-300E with approximately 1.85 to 2.2 times the throughput capacity of the 5870.
- 5890-200E with approximately 0.82 times the throughput capacity of the 5890-300E.
- 5890-190E with approximately 0.54 times the throughput capacity of the 5890-300E.
- 5890-200E field upgradeable to the 5890-300E, the 5890-400E, or the 5890-600E.
- 5890-300E field upgradeable to the 5890-400E or the 5890-600E.
- 5890-190E field upgradeable to the 5890-300E, the 5890-400E, or the 5890-600E.
- From 64 to 256 megabytes (MB) of main storage on a dual processor. From 32 to 256 MB of main storage on a uniprocessor.
- From 32 to 64 channels on a dual processor. Up to 16 channels may be byte-multiplexer channels.
- From 16 to 48 channels on a uniprocessor. Up to 12 channels may be byte-multiplexer channels.
- Compatible with *IBM System/370 Principles of Operation* and *IBM System/370 Extended Architecture Principles of Operation*.
- Functional flexibility through extensive use of Macrocode and distributed microcode.
- Machine cycle time of 15 nanoseconds (ns).
- 16-byte wide primary data paths between key system components.
- 400-gate and 1,000-gate, 0.35 ns, large-scale integration (LSI), emitter-coupled logic (ECL) chips.
- For dual processors, two CPUs housed in a single frame consisting of a .18 cubic meter (6.5 cubic feet) three-dimensional primary stack and a .16 cubic meter (5.6 cubic feet) secondary stack. These CPUs share main storage and channels and are capable of operating under a single system control program (SCP).
- For uniprocessors, one CPU housed in a frame consisting of a .18 cubic meter (6.5 cubic feet) stack.
- CPU, input/output (I/O), and support functions implemented on multiple chip carriers within the stacks.
- Channels implemented in I/O processors (IOPs), with up to 16 channels in each IOP.
- Data transfer rates of up to 3 MB/second for block-multiplexer channels and up to 200 KB/second for byte-multiplexer channels. Additionally, data transfer rates of up to 4.5 MB/second can be achieved with the 580/Electronic Direct Access Storage High Speed Channel Feature (580/EDAS HSCF) when used in conjunction with Amdahl's 6680 EDAS Product.
- Data streaming standard on all block-multiplexer channels.
- On dual processors, direct access from either CPU to any channel.
- Optional 580/Multiple Domain Feature (580/MDF) to provide near-native performance of up to four SCPs executing concurrently.
- Definition of channel protocols through independent interface handlers, allowing flexibility in implementing future channel protocols.

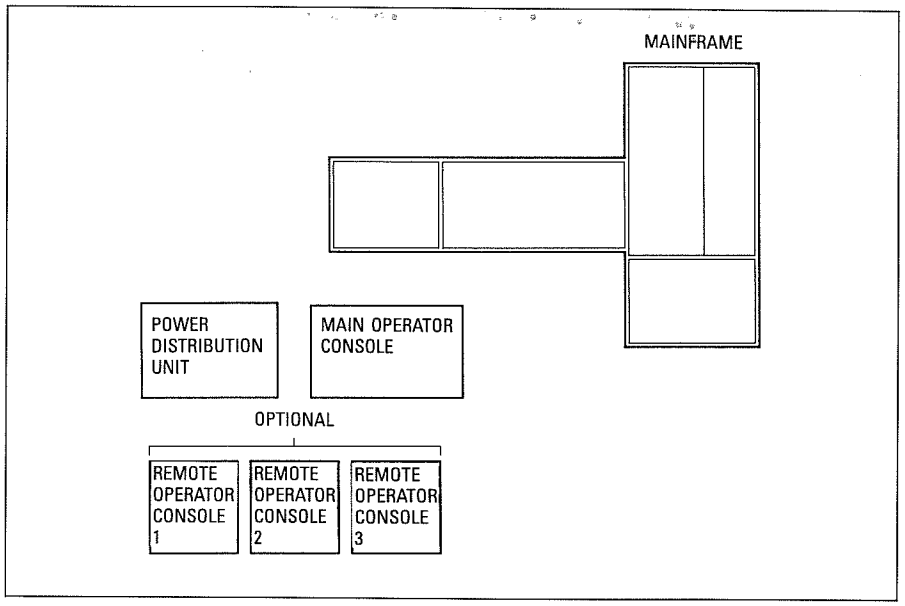

FIGURE 1-2 System Layout and Components

- Up to four optional channel-to-channel adapters (CCAs) for loosely coupled operation with another Amdahl processor or other compatible computing complexes. With 580/MDF, CCAs also allow communication between the multiple SCPs.
- 580/Expanded Storage feature, allowing a portion of main storage to be utilized as expanded storage.
- Support for the interpretive execution facility, allowing operation of guest SCPs under VM/XA Systems Facility.
- Advanced error-checking and correction circuitry.
- Functional packaging, minimizing the number of connections and permitting rapid fault isolation.
- Up to three optional remote operator consoles, which may be located up to 1,500 meters from the main operator console.
- Full air cooling.
- Compact size and low weight.

1.2 System Components

The 5890 uniprocessor and dual processor system components consist of a mainframe, power distribution unit, main operator console, and optional remote operator consoles. Figure 1-2 illustrates the system layout and components.

1.2.1 Mainframe

The major components of the mainframe are the processor unit, main storage unit, system support unit, and power supply unit. An optional channel extension unit may also be contained in the mainframe for configurations with more than 32 channels, or more than two CCAs. Figure 1-3 shows the mainframe components.

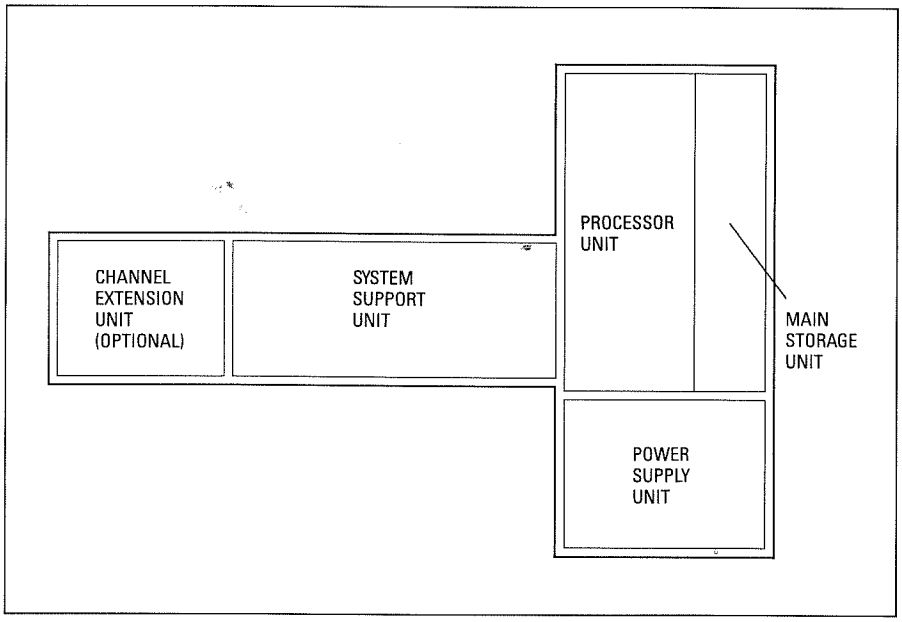

FIGURE 1-3 Mainframe Components

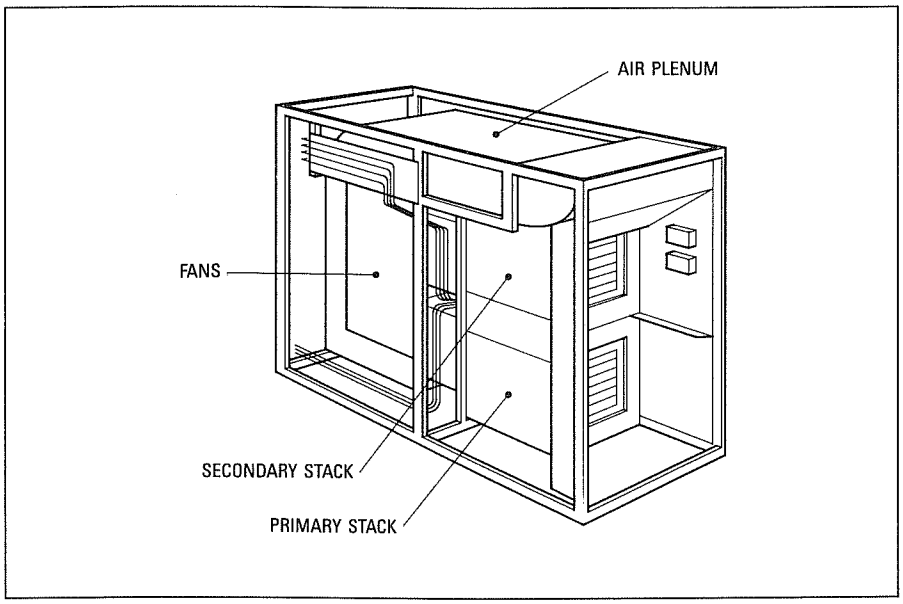

FIGURE 1-4 Processor Unit

The processor unit, which is located next to the main storage unit, houses one or two LSI stacks (figure 1-4). Each stack is a three-dimensional structure that holds multiple chip carriers (MCCs). The dual processor has two stacks in the processor unit, one above the other. The bottom stack has 15 MCC slots and the top stack has 13 MCC slots. The uniprocessor has only the bottom stack. The processor unit also contains suction fans and air ducts for cooling.

The main storage unit (figure 1-5) contains four groups of assemblies: main storage electronics, power supplies, power distribution box, and cooling fans. The main storage unit has a swing gate with a two-bay main storage card cage containing the main storage electronics. The power supplies are mounted on a hinged gate. Access to the processor unit fans is obtained by rotating this gate to the 90° open position.

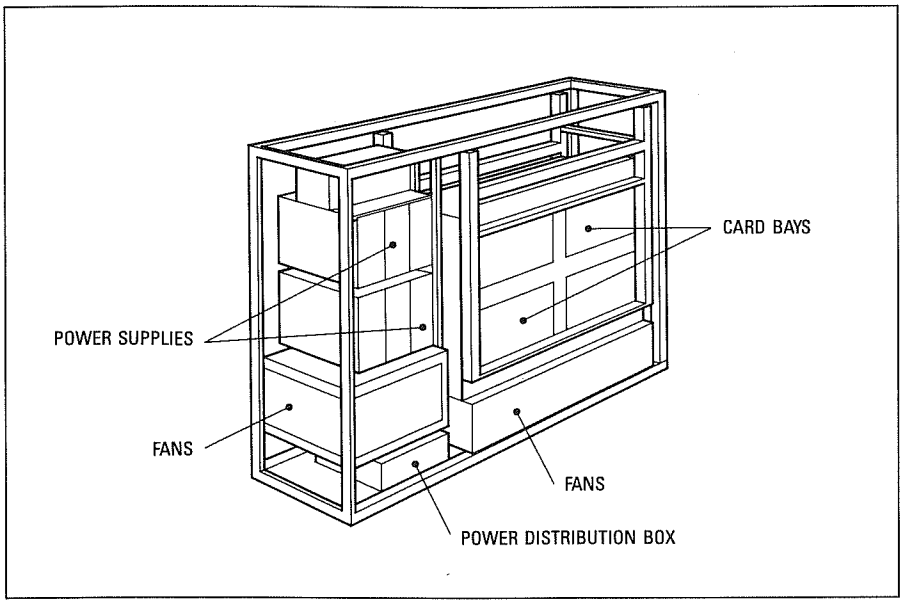

FIGURE 1-5 Main Storage Unit

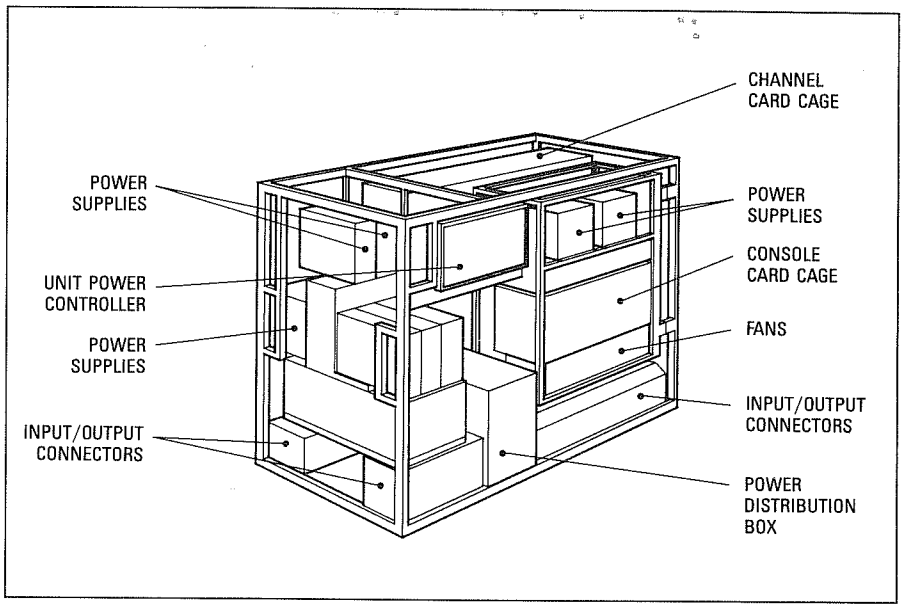

FIGURE 1-6 System Support Unit

The system support unit (figure 1-6) contains the following components: a two-bay channel card cage, console card cage, I/O connectors, power supplies, power distribution box, unit power controller, and cooling fans. The channel card cage accommodates channel interfaces, CCAs, and the optional Hardware Monitor Attachment Feature interface cards. The console card cage contains support logic for the system support processor MCC.

The power supply unit (figure 1-7) contains power supplies, two unit power controllers in a dual processor configuration, a power distribution box, and cooling fans for the power supplies.

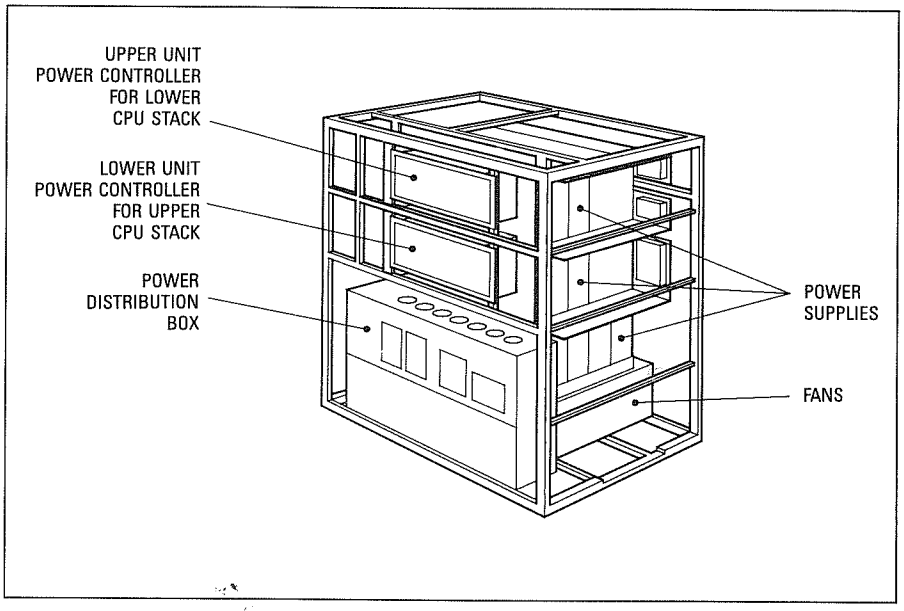

FIGURE 1-7 Power Supply Unit

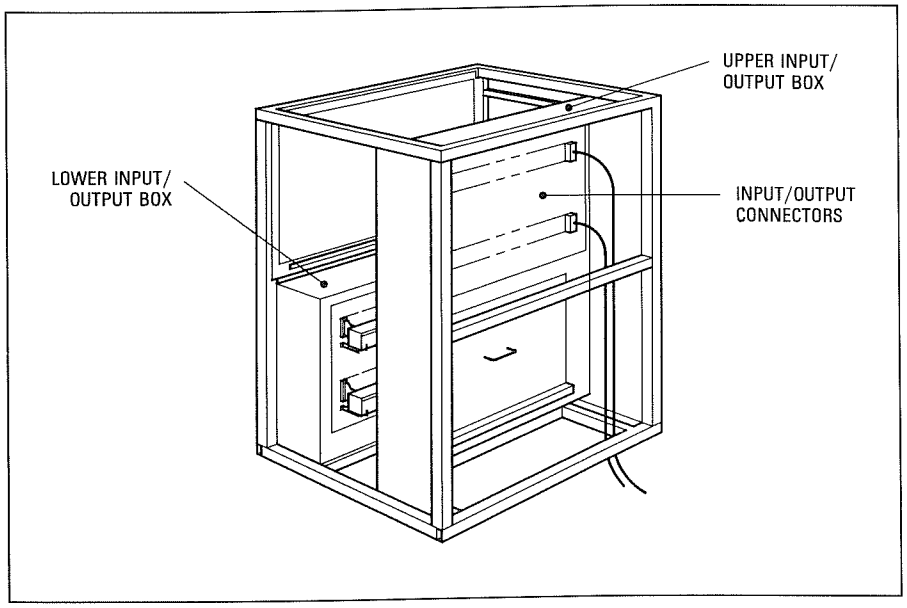

FIGURE 1-8 Channel Extension Unit (optional)

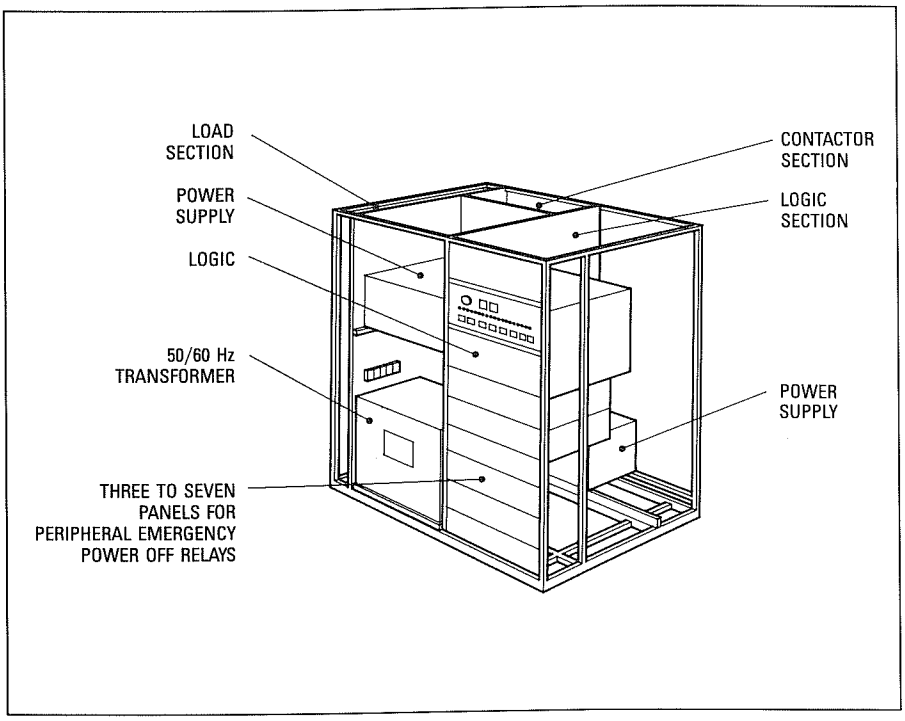

FIGURE 1-9 Power Distribution Unit

The optional channel extension unit (figure 1-8) provides I/O connectors for up to 32 channel interfaces and two CCAs.

1.2.2 Power Distribution Unit

The power distribution unit (figure 1-9) contains the AC input center, contactors, a power supply, and logic to manage and distribute 400 Hz or 50/60 Hz AC power. The power distribution unit can provide emergency power off connections for control units.

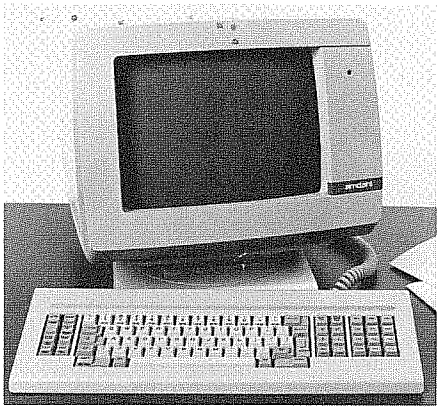

FIGURE 1-11 Remote Operator Console

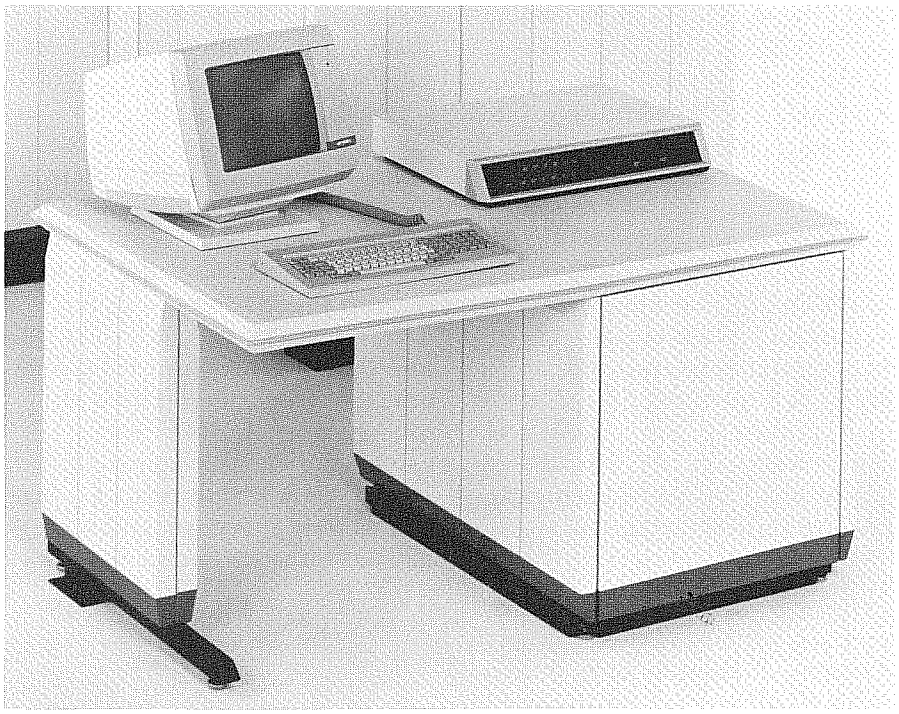

FIGURE 1-10 Main Operator Console

1.2.3 Operator Consoles

Up to four operator consoles (one main operator console and three remote operator consoles) can be connected to the processor. The main operator console consists of an operator complex and an electronics complex (figure 1-10). The operator complex comprises a display station and a keyboard. The electronics complex contains two floppy disk drives, an internal hard disk, a basic logic card, a maintenance panel, required power supplies, and a modem with an RS-232C interface for diagnostic operations.

Each optional remote operator console (figure 1-11) contains an operator complex (a keyboard and a display station) and uses the electronics complex facilities of the main operator console. A maximum of three remote operator consoles can be attached, and each can be located up to a maximum of 1,500 meters (4,921 feet) from the mainframe.

1.3 Functional Description

The major functional units of the system are the main storage unit, CPUs, system director, external director, channel subsystem, and console subsystem. Figure 1-12 illustrates the primary data paths and supporting control paths for the 5890 uniprocessor. Figure 1-13 illustrates the primary data paths and supporting control paths for the 5890 dual processor.

The main storage unit contains up to 256 MBs of main storage. Main storage is eight-way interleaved and is connected to the rest of the system via 16-byte wide data paths.

The CPU subsystem implements the IBM System/370 and 370-XA instruction sets and receives I/O interrupts and messages. Each dual processor contains two identical CPUs while a uniprocessor contains one CPU. Each CPU is made up of subunits. The instruction unit controls the fetching of instruction words and the execution of the designated operation. The CPU storage unit (CSU) provides a high-speed buffer between the CPU and main storage for instructions and instruction operands. The execution unit executes shift, logical, and arithmetic operations.

The system director controls data transfer between the main storage unit, the CPUs, and the external director. The system director also provides all address and control information required for moving data into the external director and the CPU buffers. The system director is the focus for inter-unit communication. All CPU and I/O data requests are sent to the system director, which in turn controls main storage accesses and ensures system-wide data integrity.

The external director connects the channel subsystem and the console subsystem to the rest of the processor complex. It receives all I/O instructions from the CPUs, processes them, and transfers them to the appropriate destination via a bus message. The external director also receives all I/O and system support processor requests for data, queues them, and makes appropriate requests to the system director. The external director implements portions of the extended dynamic channel subsystem, the I/O interrupt queuing and routing functions, and miscellaneous interrupt message routing.

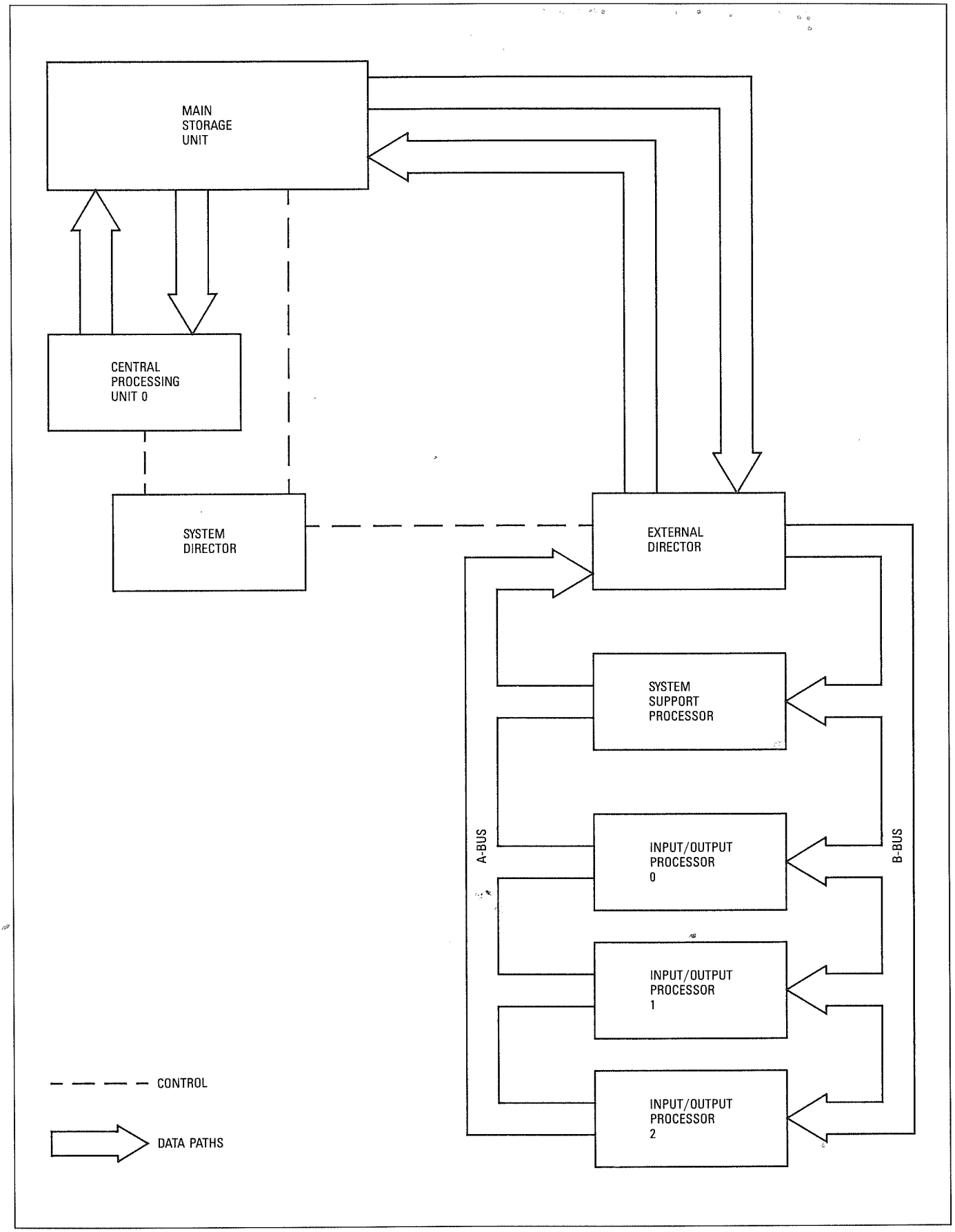

FIGURE 1-12 Uniprocessor Primary Data Paths

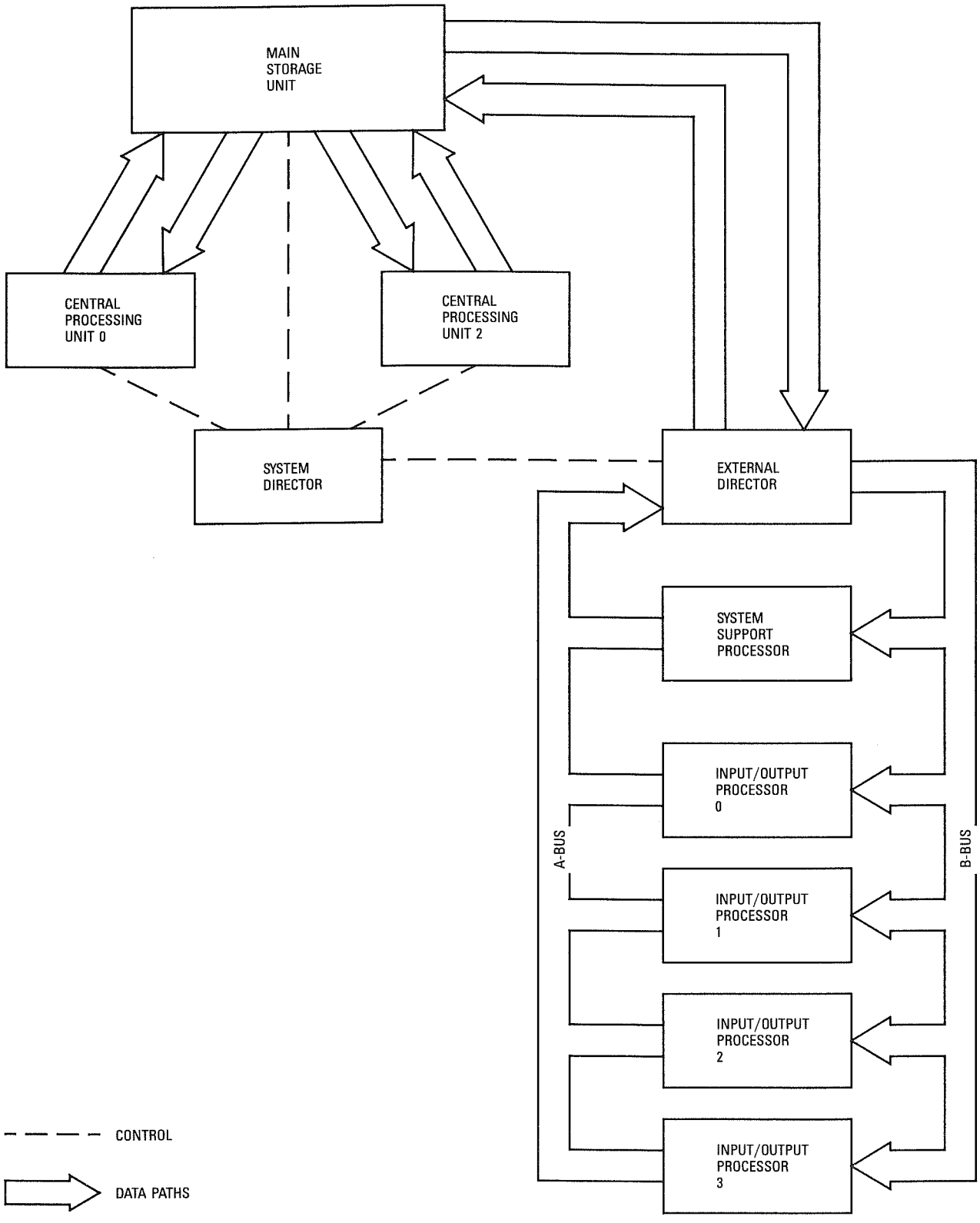

FIGURE 1-13 Dual Processor Primary Data Paths

The channel subsystem includes from one to four integrated IOPs, each containing 16 channels. The channels are configurable as byte- or block-multiplexers. A maximum of 4 byte-multiplexer channels is permitted in a 16-channel IOP group. A maximum of 16 byte-multiplexer channels are available in a fully configured 64-channel dual processor. A maximum of 12 byte-multiplexer channels are available in a fully configured 48-channel uniprocessor. All block-multiplexer channels are capable of data streaming, and can support all current single-byte interface I/O device data rates. When configured, all byte-multiplexer channels can operate at data rates of up to 200 KB/second in burst mode. Each channel can address up to 256 I/O devices.

The console subsystem, which includes the system support processor and operator consoles, provides a window to the system. It configures the mainframe, monitors the system operation, and may be used as a backup operator console for a customer's SCP. The console subsystem contains an independent service processor that provides tools for local and remote problem diagnosis.

More detailed information on each of the functional units is provided in chapters 3 through 8.

1.4 Compatibility

The 5890 processors support both System/370 and System/370 extended architecture (370-XA) modes. When operating in System/370 mode, 5890 processors conform to the System/370 architecture as described in the *IBM System/370 Principles of Operation*. When operating in 370-XA mode, 5890 processors conform to the System/370 extended architecture as described in the *IBM System/370 Extended Architecture Principles of Operation*. In either mode, 5890 processors conform to the *IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information*. When Interpretive Execution Facility (IEF) is supported, 5890 processors conform to the System/370 extended architecture as described in the *IBM System/370 Extended Architecture Interpretive Execution*.

1.4.1 Domains

Each 580 Series processor, including the 5890 models, provide a processing environment called a domain. A domain consists of main storage, channels, operator facilities, and logical processors that execute instructions. When activated, a domain has the facilities described in the *IBM System/370 Principles of Operation* or *IBM System/370 Extended Architecture Principles of Operation*. A standard configuration 5890 has one domain. With the optional 580/MDF, a 5890 uniprocessor or dual processor supports up to four domains.

The user defines the resources assigned to a domain and the domain's attributes. A domain can be redefined as requirements change, providing flexibility in allocation of system resources. Resources and attributes that can be defined for a domain include:

- An amount of main storage.
- An amount of expanded storage.
- Channels.
- On a dual processor, one or two logical processors, permitting a user workload in a domain to use one or both CPUs. On a uniprocessor, one logical processor.
- Up to 100 percent of the available CPU resources.
- Miscellaneous attributes, such as optional assists and architectural features.

Each domain has its own set of timing facilities.

1.4.2 Conformance to the Principles of Operation

Any program written to run in either System/370 mode or in 370-XA mode can run on a 5890 processor if the processor is operating in the appropriate mode and the program:

- Is not time-dependent.
- Is not dependent on the presence of system facilities (such as storage capacity, peripheral equipment, or optional features) when these facilities are not included in the system configuration.
- Is not dependent on the absence of system facilities when these facilities are included in the system configuration.
- Does not use or depend on fields associated with uninstalled facilities.
- Is not dependent on results or functions that are defined in the applicable principles of operation as being unpredictable or model-dependent, or as affecting compatibility.
- Is not dependent on results or functions that are defined to be deviations from the applicable principles of operation.
- Takes into account those changes to the System/370 architectural definition that affect compatibility between the System/370 mode and the 370-XA mode.
- When operating in System/370 mode, does not depend on the presence of the 2-kilobyte page size, nor the presence of storage protection keys associated with 2-kilobyte blocks of storage, nor the presence of the direct control and external signal facilities.

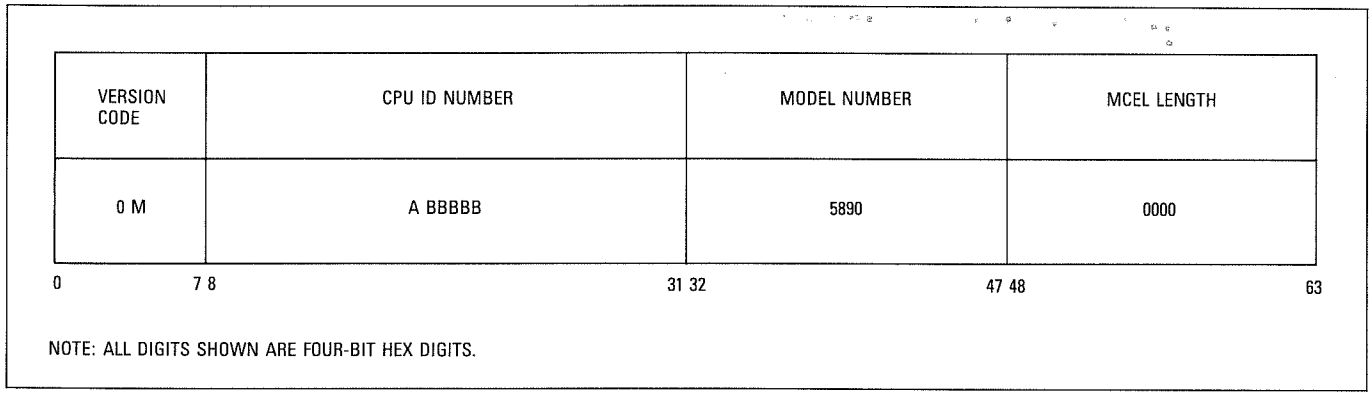

FIGURE 1-14 Results of STIDP Instruction

Any problem-state program written for System/370 operates in 370-XA mode, and any problem-state program written for System/360 operates in 370-XA mode or System/370 mode, provided that the program:

- Observes the limitations in the preceding statements.
- Does not depend on any programming support facilities that are not provided or that have been modified.
- Takes into account other changes made that affect compatibility between modes. These changes are described in the *IBM System/370 Extended Architecture Principles of Operation* and in the *IBM System/370 Principles of Operation*.

1.4.3 Model-Dependent Instructions

Three instructions produce model-dependent results on 5890 processors:

- STORE CPU ID (STIDP)
- STORE CHANNEL ID (STIDC)
- DIAGNOSE (DIAG)

STIDP stores model-dependent data at the double word addressed by the second operand. The CPU ID stored for a domain by the STIDP instruction is a double word with four fields of information (figure 1-14). This 64-bit field stores information that defines the processor model, processor serial number, and the maximum machine check extended logout (MCEL) length. Within the CPU ID, a 4-bit logical processor identifier (LPID) is appended to the processor serial number to allow each domain under 580/MDF to have unique CPU IDs. The user may override the default LPID if a specific LPID is desired. The purpose and value of bits 0-63 are detailed in table 1-1, as appropriate.

TABLE 1-1
Results of STIDP Instruction

Version Code	
Bits 0:3	Reserved—set to zeros.
Bits 4:7	Define model number code.
M	X'1'—Model 5890-190, 5890-190E X'2'—Model 5890-200, 5890-200E X'3'—Model 5890-300, 5890-300E
CPU ID Number	
Bits 8:11	Specify LPID.
A	Default LPID value. Bits 8:9 domain number. Bits 10:11 logical processor number.
Bits 12:31	Specify processor serial number.
BBBBB	
Model Number	
Bits 32:47	Set to X'5890'.
MCEL Length	
Bits 48:63	Maximum MCEL length set to X'0000'.

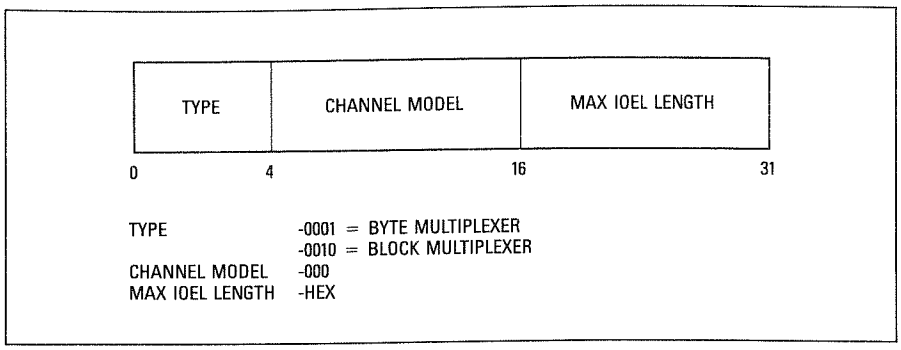

FIGURE 1-15 Results of STIDC Instruction

STIDC stores channel-dependent data at decimal location 168. Because the 580 channel model is implicit in the system model, zeros are stored in the channel model-number field. The remaining fields, channel type, and I/O extended logout (IOEL) length follow standard conventions (figure 1-15).

1.4.4 Programming Support

SCPs supported by the 5890 uniprocessor and dual processor systems are listed below.

1.4.4.1 System Control Programs

Depending on the mode of the domain into which the SCP is loaded, the following SCPs are supported:

- MVS/SP Version 1 (MVS/370)
- MVS/SP Version 2 (MVS/XA)
- VM/SP with High Performance Option (VM/SP HPO)
- VM/XA Systems Facility (VM/XA SF)
- UTS/580

Support for specific releases of SCPs is announced periodically by Amdahl.

1.4.4.2 Environmental, Recording, Editing, and Printing Program

The 5890 systems contain extensive system monitoring, logging, and recovery procedures to extend availability and collect data, making preventive maintenance and repair more efficient. This data is recorded on the console hard disk. It is printed with the Amdahl environmental, recording, editing, and printing (AMDEREP) program, an Amdahl-supplied application program. AMDEREP is Amdahl-specific, and is used primarily by Amdahl service representatives.

In the few cases where the 5890 needs SCP assistance to recover from an abnormal condition, the customer's SCP typically will also log the fact of the abnormal condition and the recovery action taken. This data is printed with the SCP's EREP program. CPU and channel information is generic and is used primarily for monitoring trends.

IBM EREP is not modified and Amdahl's AMDEREP is not subject to IBM maintenance. Unmodified EREP can process most of the error records; however, AMDEREP is required to process Amdahl-specific information in some of the records.

1.4.4.3 I/O Configuration Program

Amdahl provides an I/O configuration program (IOCP) which replaces the IBM-supplied IOCP on 5890 processors. Further details on the Amdahl IOCP are provided in chapter 7, Channel Subsystem.

1.4.4.4 MVS Model-Dependent Support

The model-dependent support options are discussed below.

Speed Table Constants. A modification to the MVS speed table constants in the system resource manager (SRM) is required. This modification ensures consistent computation of service units across the range of Amdahl and IBM processor models.

Common System Data Area. Modification to the IBM MVS/XA common system data area is available. This modification ensures proper

Amdahl and IBM processor identification for the IBM Resource Management Facility (RMF) program product. The common system data area modification does not apply to System/370 mode but is required in 370-XA mode if RMF Release 3.2.1 or higher is installed.

Processor Numbers. On 5890 dual processors, a modification to MVS/370 is required to allow the SCP to correctly address both CPUs.

RMF. A modification to the IBM RMF program product is available to ensure appropriate interpretation of 5890 system activity data. This modification does not apply in System/370 mode but is required in 370-XA mode.

1.4.4.5 VM Model-Dependent Support

Processor Capabilities. A modification to VM/SP HPO is available to correctly identify processor capabilities. This modification is required if the customer wishes to run MVS under VM or use the VM version of the IOCP. This modification is also recommended for other VM environments. A similar modification is available for VM/XA SF.

1.5 Upgradeability

Amdahl's 5890 processors can be upgraded as outlined in table 1-2.

TABLE 1-2

Upgrade Paths

	TO		
FROM	**5890-300E**	**5890-400E**	**5890-600E**
5890-190E	x	x	x
5890-200E	x	x	x
5890-300E		x	x

x = Available Upgrade Paths

1.6 Features

The 5890 processors provide support for a comprehensive set of standard features through the use of hardware, microcode, and Macrocode. These features and their applicability to System/370 and 370-XA modes are described in appendix A.

Detailed information on the available optional features is contained in chapter 10, Optional Features. Appendix B categorizes feature availability by processor model.

1.7 Reliability, Availability, and Serviceability

The 5890 processors include reliability, availability, and serviceability (RAS) features.

1.7.1 Reliability

Reliability is the prevention of errors that can cause system failure. Some highlights are listed below.

- Evolution of proven reliable ECL technology used in the 470 Series and other 580 Series processors.
- Design that minimizes the number of physical components and the number of connections between components.
- Air cooling.
- Extensive design validation and testing.
- System analysis during power on to ensure that any main storage page with an uncorrectable error is deallocated.

1.7.2 Availability

Availability is the continuation of system operation, despite component failure. The following list highlights some of the availability features provided by the system.

- Advanced error detection and correction capability.
- Independent system support processor to monitor system operation.
- Control store error detection and recovery capability.
- Monitoring of power and cooling systems to provide advance warning of error conditions.
- Redundancy in the power and cooling systems to allow continued system operation after a component failure.
- Ability to physically vary CPUs, channels, and portions of main storage offline to minimize impact of failures.
- Parity checking for registers and data buses.
- Main storage double-bit error detection and single-bit error correction.
- CPU instruction retry capability.
- I/O instruction retry capability.
- Isolation of one CPU from machine checks in the other CPU on a dual processor.

1.7.3 Serviceability

Serviceability is the swift diagnosis and repair of any system failure. Some highlights are listed below:

- Extensive error log to provide data for problem analysis.
- Automated event log to track site activity.
- Automated error isolation to a field-replaceable unit.
- Functional design to facilitate rapid fault isolation.
- Remote support assistance via Amdahl Diagnostic Assistance Center (AMDAC®).
- Field feedback system for transmission of key system activity data to an Amdahl central site.
- Independent system support processor to provide diagnostic aids.
- File transfer via a telephone link for microcode and Macrocode fixes and feedback data.
- Automated system configuration control.

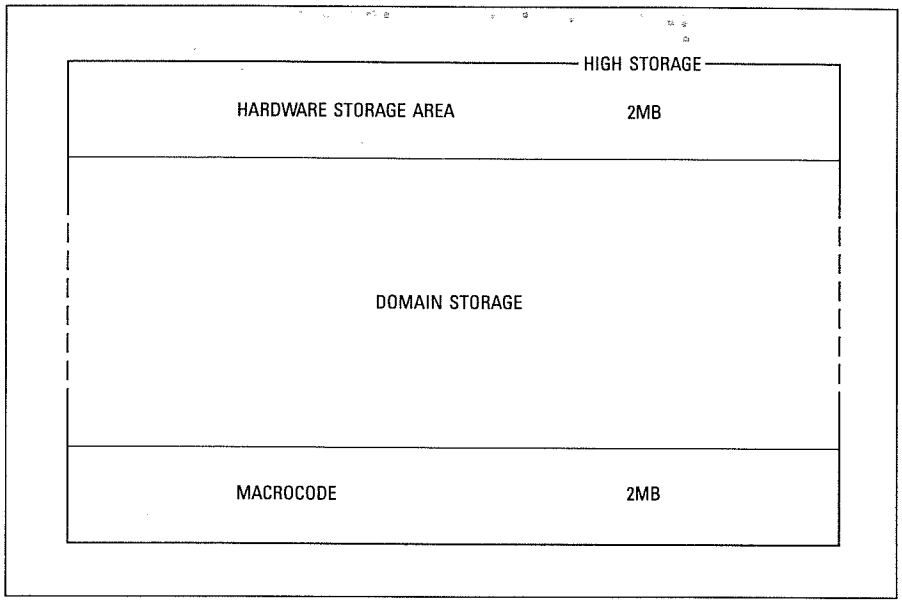

FIGURE 1-16 Allocation of Main Storage

1.7.3.1 **Amdahl Diagnostic Assistance Center**

AMDAC provides remote fault diagnosis, correction, and assistance. It is accessed through a dial-up telecommunications network and is designed to permit customer control over its activation and use. This control is enabled by use of a key that remains in the customer's possession. The customer may unilaterally terminate a session at any time.

1.8 Planning Requirements

Physical planning requirements for 5890 processors are specified in the *Amdahl Computing Systems Physical Planning Manual*. Appendix B presents a summary of some key planning requirements.

Main storage sizes on the 5890 uniprocessor and dual processors range from 32 to 256 MB. Some of this storage is reserved for use by the system, including 2 MB of main storage beginning at address zero. Hardware system area is allocated downwards from the high storage limit and also requires 2 MB of main storage. Domain storage appears to the user as if it starts at main storage location zero. Figure 1-16 shows the allocation of main storage.

2

Technology and Packaging

This section provides information concerning logic, random access memory and register chips, multiple chip carriers, and dual processor stacks. The 5890 processors incorporate advanced design and technology. Taking advantage of over ten years' experience in ECL technology, the 5890 processors provide leadership in addressing the marketplace requirements for: reliability, availability, and serviceability; compatibility; price/performance; and flexibility to accommodate future functions.

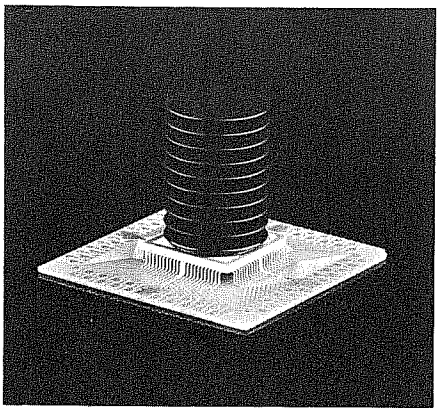

FIGURE 2-1 Logic Chip

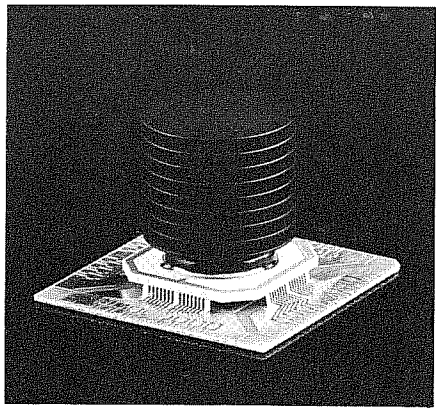

FIGURE 2-2 Random Access Memory Chip

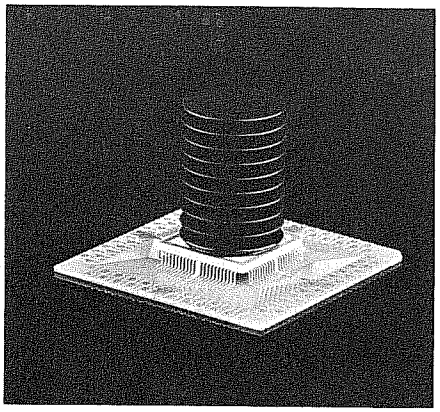

FIGURE 2-3 Register Chip

2.1 Logic Chips

Logic chips used in the 5890 processors (figure 2-1) contain up to 400 circuits and have an average switching speed of 350 picoseconds (.35 ns). These Amdahl-designed logic chips are used throughout the system and are the basis for the system's compact size and high performance.

2.2 Random Access Memory Chips

Two types of high-speed LSI random access memory (RAM) chips are used in the 5890 processors (figure 2-2). The 4-kilobyte RAM chip has an access time of 3.5 ns and provides speed and efficiency for CPU buffers and microcode control storage. The 16-kilobyte RAM chip has an access time of 15 ns. It is used in the system support processor and IOP, and as a history RAM. The history RAM accumulates recent activity that can be used by a field engineer to recreate failures or isolate failing components.

2.3 Register Chips

The register chip (figure 2-3) provides fast and efficient storage of register and other key system data. It has an access time of 3.5 ns.

2.4 Multiple Chip Carriers

MCCs are 14-layer printed circuit boards (figure 2-4). 5890 uniprocessors are implemented on 13, 14, or 15 MCCs, depending on configuration. 5890 dual processors are implemented on 23, 24, or 25 MCCs, depending on configuration. Each MCC measures 29 centimeters by 33 centimeters (11 inches by 13 inches) and can accommodate 121 LSI chips (over 45,000 circuits). Logic, RAM, and register chips are intermixed and mounted on MCCs for ease of interchip communication. The intermixing of chips permits distribution of microcode storage to individual MCCs, allowing functional customization and efficient operation.

2.5 Stacks

MCCs are mounted horizontally in three-dimensional stacks (figure 2-5) within each processor unit. The primary stack, present in both uniprocessors and dual processors, measures 59 centimeters by 52 centimeters by 61 centimeters (23 inches by 20 inches by 24 inches), and contains up to 15 MCCs. The secondary stack, present in dual processors only, measures 52 centimeters by 52 centimeters by 61 centimeters (20 inches by 20 inches by 24 inches), and contains up to 13 MCCs. MCCs are connected via the side panels, which are 12-layer printed circuit boards forming the sides of the stacks. The side panel connectors allow for short data paths and reliable interconnections. This design feature contributes to the 5890 processors performance and reliability.

The stacks contain the MCCs required to implement the system director, external director, CPU(s), IOP(s), and the system support processor.

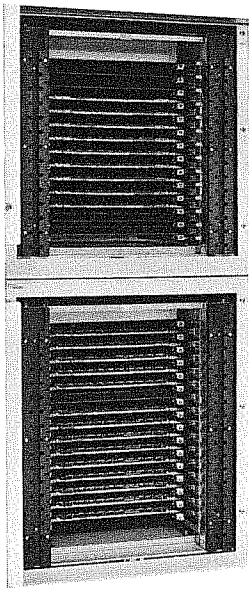

FIGURE 2-5 Stack

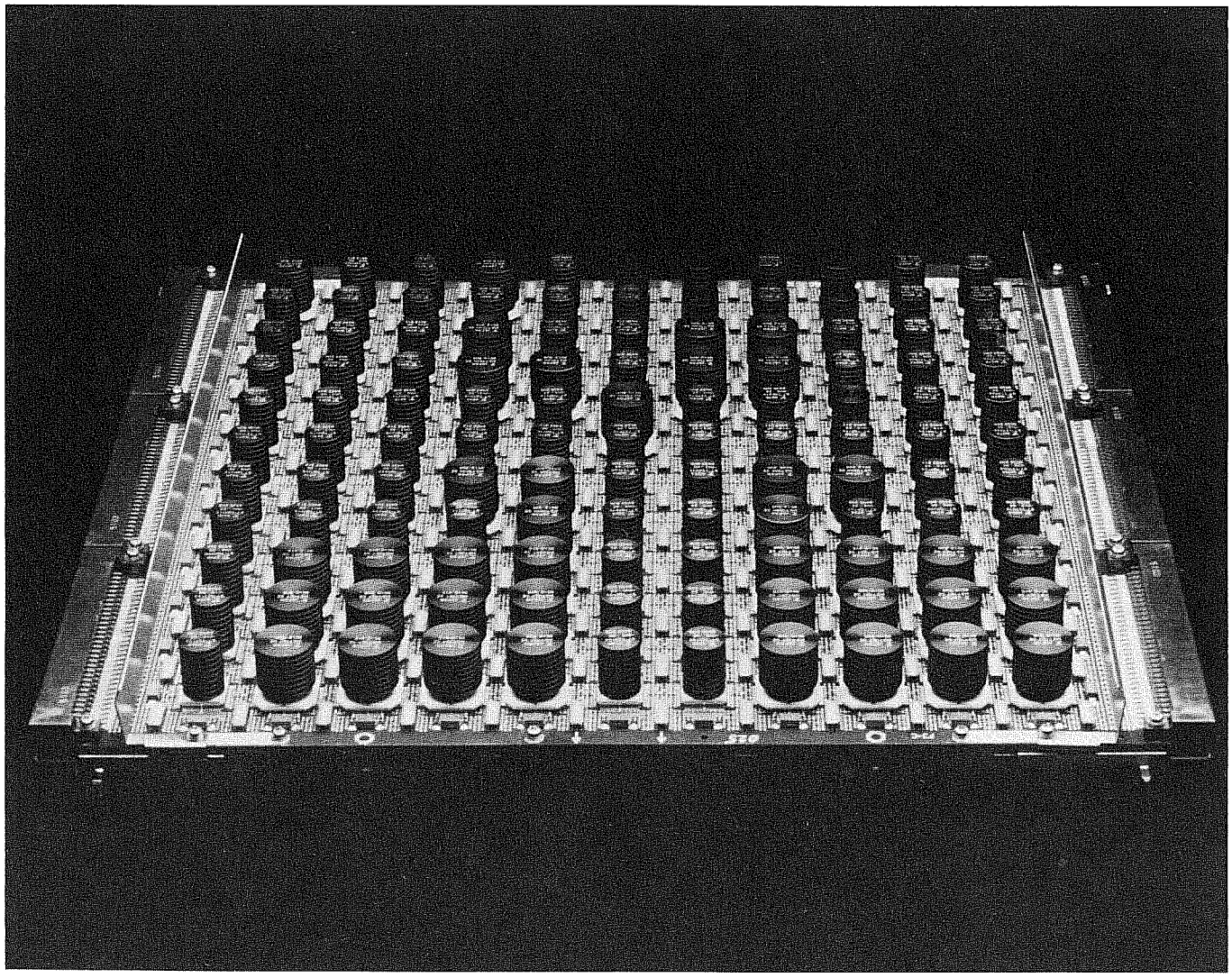

FIGURE 2-4 Multiple Chip Carrier

3 System Director

This section describes the system director. The data integrity of the entire Amdahl 5890 processor complex is the responsibility of the system director. This element provides system-wide data integrity by controlling and monitoring, but not performing, all requests for data and accesses to main storage throughout the system, and all storage protect key functions. Any unit in the complex needing a particular data item from main storage must request it via the system director. There, each request is satisfied (if possible) by searching main storage and the high-speed buffers to locate the required element. Then, the system director controls the data transfer to the requesting unit. Figure 3-1 illustrates the flow of data through the system director.

Requests for data from the CPU(s) and from the external director arrive on the signal buses. Requests are selected on a priority basis and are passed down the I-Bus into ports, where they await the availability of appropriate servers to handle them.

Each request can result in action from one of the following server functions:

- System-Integrity Server. This server searches to find the most up-to-date copy of the requested data.
- Move-Out Server. This server is responsible for controlling the transfer of data out of the processor buffers.
- Move-In Server. This server is responsible for controlling the transfer of data into the processor buffers.
- Main-Storage Server. This element provides controls to the main storage unit, causing data movement into, or out of, main storage. These controls include addresses, write enables, and timing signals.
- Key Server. This element signals the main storage unit that protect-key operations are to take place. It then supplies appropriate details to the main storage unit for action.

In this manner, the system director stays aware of the contents of the CPU(s), the external director data buffer, and the outstanding data movement activities taking place throughout the system.

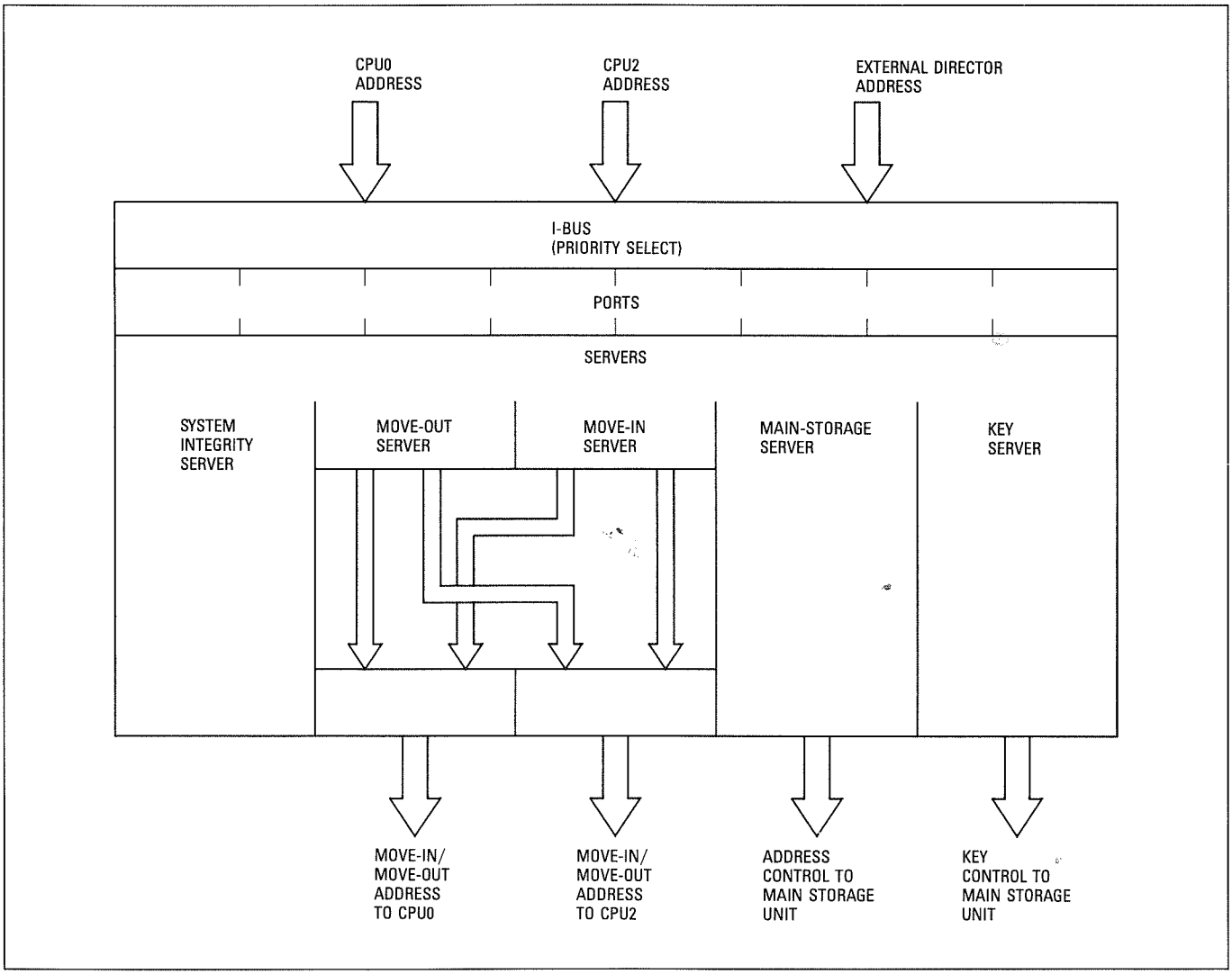

FIGURE 3-1 System Director Data Flow

4 Central Processing Units

This section discusses the major functions of the 5890 CPUs. It also gives information concerning the CPU functional units.

Each 5890 uniprocessor contains one CPU, and each 5890 dual processor contains two identical CPUs. The CPU subsystem is responsible for instruction processing and implements the System/370 and 370-XA instruction sets. Operation of each CPU is pipelined, allowing each CPU to have five instructions in some phase of execution simultaneously. Figure 4-1 illustrates the flow of data through each CPU.

The CPU functional units are:

- CPU Storage Unit
- Instruction Unit (I-Unit)
- Pipeline Flow
- Process Control
- Timing Facilities
- Execution Unit (E-Unit)

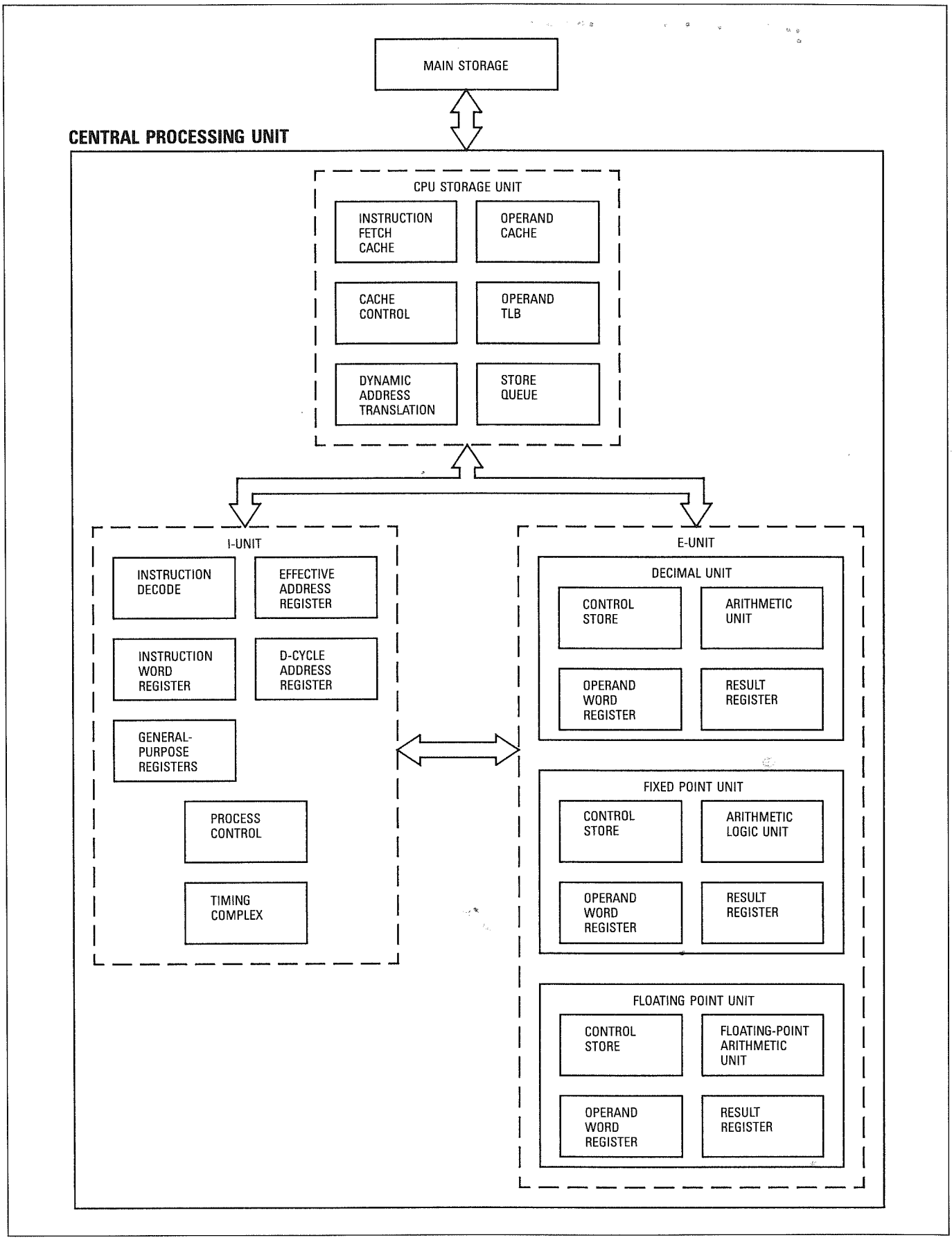

FIGURE 4-1 CPU Data Flow

4.1 CPU Storage Unit

The CPU storage unit receives and processes all requests for data by the I-Unit. It contains two independent, high-speed buffers or caches, a 32-kilobyte instruction cache which contains most-recently-accessed instructions, and a 64-kilobyte operand cache which contains most-recently-accessed operands. It also contains the Dynamic Address Translation (DAT) facility to provide translation of virtual addresses to real addresses and a store queue to improve execution times of CPU stores.

The high-speed caches permit each CPU to operate near maximum execution rate by reducing the frequency of references to main storage. When the I-Unit requests main storage data, the CPU storage unit first accesses the appropriate cache to see if the requested data is located there. If it is, the cache data is used. If it is not, the CPU storage unit initiates a request to the system director for main storage access.

The DAT facility of the CPU storage unit translates virtual addresses into real addresses and maintains the Translation Lookaside Buffer (TLB) to provide a fast address translation path.

In managing I-Unit data requests, the CPU storage unit attempts to keep the I-Unit pipeline executing at its maximum rate. To ensure that the pipeline will have the data it needs for instruction execution, the CPU storage unit prioritizes requests for access to the caches. Operand accesses for subsequent instructions are given higher priority than storage writes from completed instructions. To free up the pipeline after instruction execution, data for up to four storage writes from the I-Unit pipeline may be queued temporarily in the store queue before being written into the cache. When the cache is not being accessed by higher priority requests, any active write requests in the store queue are allowed to access the cache. This reduces contention for cache accesses and improves system throughput.

4.2 Instruction Unit

The I-Unit initiates and controls instruction execution and interrupt processing. The major tasks performed by the I-Unit are to:

- Fetch, buffer, and decode instructions.
- Calculate effective addresses for operand and instruction fetches.
- Provide access to registers for operands and addressing.
- Control machine state and process all interrupts and machine checks.
- Administer the CPU storage unit and the E-Unit to achieve overlapped pipeline execution.

The instruction fetch process is independent of the execution pipeline logic and consists of an instruction phase, a transfer phase, and a buffer fetch phase. In the transfer phase, the instruction fetch address is transferred to the instruction fetch cache address register. Finally, in the buffer fetch phase, the instruction fetch cache is accessed, and the cache data is loaded into the instruction word register to be passed to the execution pipeline.

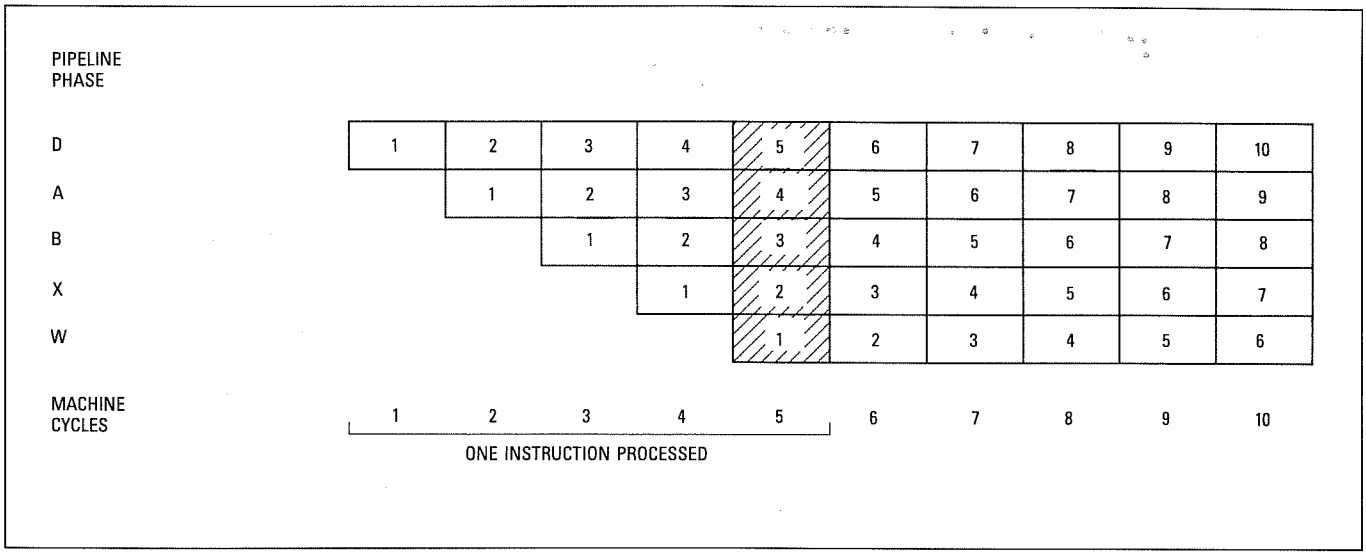

FIGURE 4-2 Pipeline Instruction Overlap

Eight bytes of instruction data can be fetched every cycle to keep the buffers full. Instruction execution condition codes are detected at the earliest possible stage, maintaining full use of the pipeline lookahead capability as branch instructions are encountered. The reliability of the I-Unit is enhanced by hardware instruction retry.

The I-Unit contains general-purpose registers, control registers, system registers, floating point registers, and timing complex registers.

4.2.1 Pipeline Flow

CPU operation is pipelined, allowing up to five instructions to be in separate phases of execution simultaneously within each CPU. Table 4-1 lists the functions of each pipeline phase.

Figure 4-2 illustrates the pipeline instruction overlap. The first instruction, upon completion of instruction fetch, enters the D-Phase and remains there for one machine cycle (15 ns). It then enters the A-Phase and a second instruction simultaneously enters the D-Phase. Up to five different instructions can be in the pipeline during a single machine cycle, each executing in a different phase. The sixth instruction enters the first phase as the first instruction exits the fifth phase.

4.2.2 Process Control

Process control manages the following CPU events that are not part of the normal instruction flow:

- Program interrupts from the pipeline
- Timer interrupts from the timing complex

TABLE 4-1

Pipeline Functions

PIPELINE PHASE	FUNCTION
D Instruction Decode	The instruction is analyzed and decoded, and the storage operand address is generated.
A Operand Address Generation	Storage operand address is transferred to the CPU storage unit, and the access for storage operands is initiated.
B Operand Cache Access	Storage operands are fetched from the operand cache, or register operands are read from the appropriate register complex.
X Execute	The operation specified by the instruction opcode is executed, and the result is placed in the result register.
W Write	Result register contents are stored in the operand cache (via the store queue) or written to a general-purpose register.

- I/O interrupts from the external director
- Machine checks from the machine-check handler
- Signals from the system support processor and the other CPU

4.2.3 Timing Facilities

The timing complex provides the timing facilities required by the CPU. Four registers in the timing complex implement the various clocks. The timing complex provides support for the SET and STORE instructions (including condition code setting) and for interrupt generation and reporting. There is one timing complex for each CPU. An update signal from the oscillator card triggers the increment or decrement of the timing complex registers every 125 ns. Table 4-2 lists the timing functions supported.

TABLE 4-2
Timing Functions

CLOCK TYPE	CLOCK FUNCTION
Time-of-Day Clock (TOD)	Provides an indication of the current date and time. A 55-bit TOD clock counter is updated every 125 ns by adding one to the low order bit. In a multiple-domain environment, each domain has its own time clock.
Clock Comparator	Provides the ability to generate an interruption at a particular date and time. The interruption is generated when the value of the TOD clock exceeds the value of the clock comparator.
CPU Timer	Measures elapsed CPU time. A 55-bit counter is decreased by one every 125 ns. An interruption is generated when the CPU timer value falls below zero, indicating that a specified amount of CPU time has elapsed.
Interval Timer	Measures elapsed time. A 16-bit binary counter is decreased by one every 125 ns. When its value becomes negative, an interruption is generated. The interval timer is available only in S/370 mode.

4.3 Execution Unit

Execution facilities have three subunits: a fixed point unit, a decimal unit, and a floating point unit.

The E-Unit receives operands for processing from the operand cache, the general-purpose registers in the I-Unit, or the floating point registers in the floating point unit.

The fixed point unit executes fixed point arithmetic operations, shifts, logical operations, and binary/decimal conversions. It also has byte- and word-moving capability, sets the condition codes, and makes branch decisions.

The decimal unit performs basic decimal arithmetic operations: add, subtract, compare, shift, multiply, and divide.

The floating point unit provides high-performance floating point capability. Most floating point operations have four phases: exponent comparison, fraction alignment, execution, and post-normalization. The floating point unit skips the alignment and/or normalization phases to reduce the overall execution time if those operations are not required.

Each execution subunit contains its own control store, arithmetic unit, operand word register, and result register. When computation by the appropriate execution subunit is complete, the E-Unit relinquishes control, permitting the write phase of the execution pipeline to store the results. When the data resulting from one instruction is to be used in a subsequent instruction that has already entered the I-Unit, a bypass exists, providing the I-Unit with the changed data instead of requiring a refetch from storage.

5 Main Storage Unit

This section discusses the logic portion of the main storage unit and includes the key facility and the switchbox. The key facility contains the key array, key data paths, and key control. The switchbox operates under the control of the system director. It controls the data buses and is responsible for moving data between main storage, the high-speed buffers, and the external director. Figure 5-1 illustrates the major components and interfaces of the main storage unit.

The main storage unit of a 5890 uniprocessor or dual processor contains data and key storage arrays for up to 256 MBs of main storage. The system director receives data requests from other functional units and generates control and timing signals to the main storage unit, which then satisfies the requests. Main storage is eight-way interleaved to allow overlapping of main storage accesses. Error-checking and correction codes are maintained for all main storage data, permitting single-bit error correction and double-bit error detection.

The 580/Expanded Storage feature allows a portion of main storage to be used as expanded storage, to reduce the paging and swapping load to channel-attached paging and swapping devices. Data movement between main storage and expanded storage is controlled by the SCP. No data can be transferred to expanded storage without passing through main storage. The amount of main storage to be used as expanded storage is determined at system initialization and is specified in 4-MB increments.

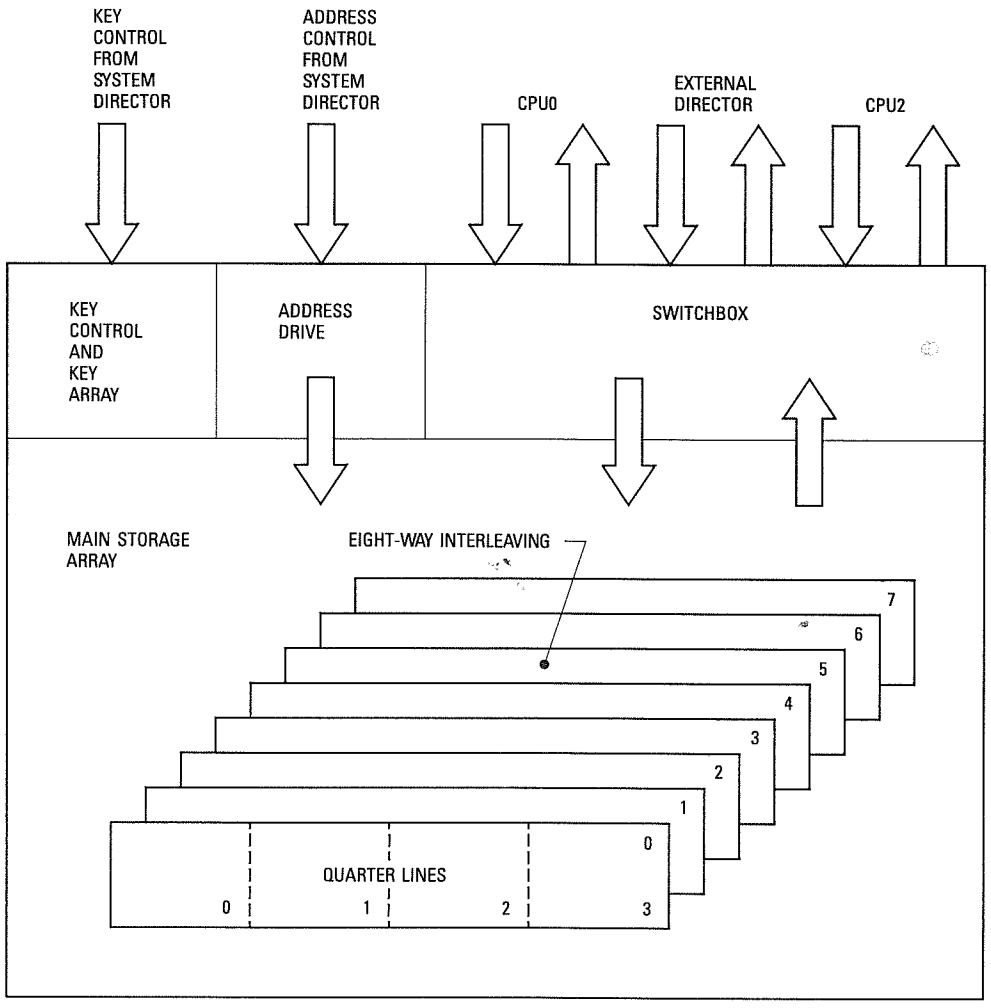

FIGURE 5-1 Main Storage Unit Major Components and Interfaces

6 External Director

This section discusses the external director and its functions. The external director is the logical and physical interface between the internal (CPU(s), system director, and main storage unit) and external (IOP(s) and system support processor) portions of the 5890 processors. Figure 6-1 shows a functional block diagram of the external director. The external director performs three functions: 370-XA I/O path selection, I/O interrupt routing, and message routing from the CPUs. Requests are received in two ways:

- Via signal paths from the CPU(s) and the system director, and
- Via data paths from the IOP(s) and system support processor.

Requests are satisfied by system elements on the external side of the 5890 processor. Besides providing the internal to external interfaces, the external director is also responsible for maintaining a record of the status of the I/O configuration and path status, for performing path selection for 370-XA mode I/O operations, and for controlling and monitoring the external dual eight-byte wide unidirectional buses. System bus management and clock synchronization are performed by the bus control and clock synchronization logic.

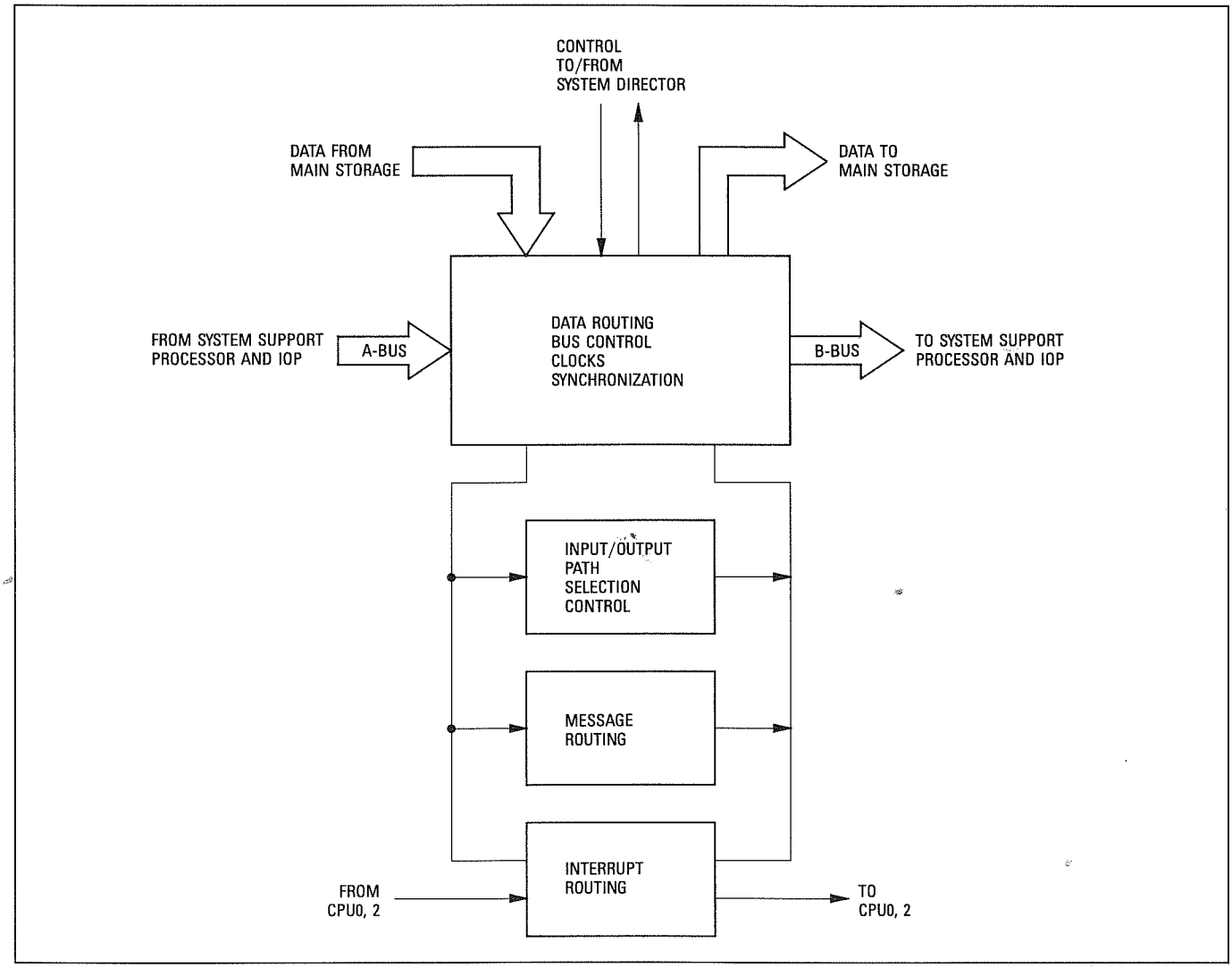

FIGURE 6-1 External Director Functional Block Diagram

7 Channel Subsystem

This section discusses the channel subsystem components and their relationship to the external director, which is vital to channel subsystem functions.

Channels, IOPs, and the interface handlers are the major channel subsystem units. They provide:

- I/O data paths between the peripheral devices and the external director
- System/370 I/O interrupt queuing and routing
- 370-XA channel path functions

The IOP hardware design provides up to 256 subchannels for each channel. A dual processor computing system has 2, 3, or 4 IOPs, each capable of supporting up to 16 channels, for a maximum of 64 channels. A 5890 uniprocessor has 1, 2, or 3 IOPs, each capable of supporting up to 16 channels, for a maximum of 48 channels.

7.1 Channels

Channels may be configured as either byte-multiplexer or block-multiplexer channels.

7.1.1 Block-Multiplexer Channels

Each block-multiplexer channel can operate in either interlock mode or data streaming mode. In interlock mode, the block-multiplexer channels support data rates up to 1.86 MB/sec. In data streaming mode, data rates up to 3.0 MB/sec are supported. With the optional 580/EDAS High Speed Channel Feature, data rates up to 4.5 MB/sec are supported.

7.1.2 Byte-Multiplexer Channels

Up to four channels per IOP can be configured as byte-multiplexer channels. These channels transfer data in either byte interleave mode or burst mode. Maximum data rates are 40 kilobytes per second in byte interleave mode and 200 kilobytes per second in burst mode.

7.1.3 Input/Output Configuration Program

Specific hardware I/O configuration data is required by the channel subsystem, which controls channel operations. The configuration data is stored in an I/O configuration data set (IOCDS) on the console hard disk.

When defining the I/O configuration, the following must be identified:

- Channel paths on the processor system
- Control units attached to the channel paths
- I/O devices assigned to the control units

The IOCDS must define all I/O paths in the 5890 configuration, whether the channel path is to be used in System/370 or 370-XA mode. Up to four IOCDSs can be stored, allowing several alternative configurations to be available. The user then selects the appropriate IOCDS at system initialization.

At system initialization, the configuration data from the selected IOCDS is used to build the appropriate I/O control blocks in the hardware system area of main storage. The IOCDS also determines the I/O resources to be initialized. The channel subsystem then uses the I/O control blocks during system operation as it satisfies I/O requests.

To create an IOCDS, the user runs the IOCP. Amdahl provides an IOCP that may be invoked as a standalone program from a 5890 console, and also offers a batch version of the IOCP that may be invoked from the user's SCP. The Amdahl IOCP provides function equivalent to that provided by the IBM IOCP and supports the maximum configurations of the 5890 processors. More information on IOCP operation is supplied in the *Amdahl 580 Series 5890 Control System Concepts,* the *Amdahl 580 Series 5890 Operation Manual,* the *Amdahl 580 Series 5890 Control System Reference Manual,* and the *IBM Input/Output Configuration Program User's Guide and Reference.*

7.2 Input/Output Processors

The IOPs are the primary interface between the interface handlers, which then communicate with peripheral devices, and the external director, which then communicates with the rest of the system. Channels access main storage through the IOPs.

An IOP consists of two functional units (figure 7-1).

- Input/Output Controller
- Bus Handler

7.2.1 Input/Output Controller

The input/output controller is the executive of the IOP and monitors and controls the actions of the interface handlers and the bus handler.

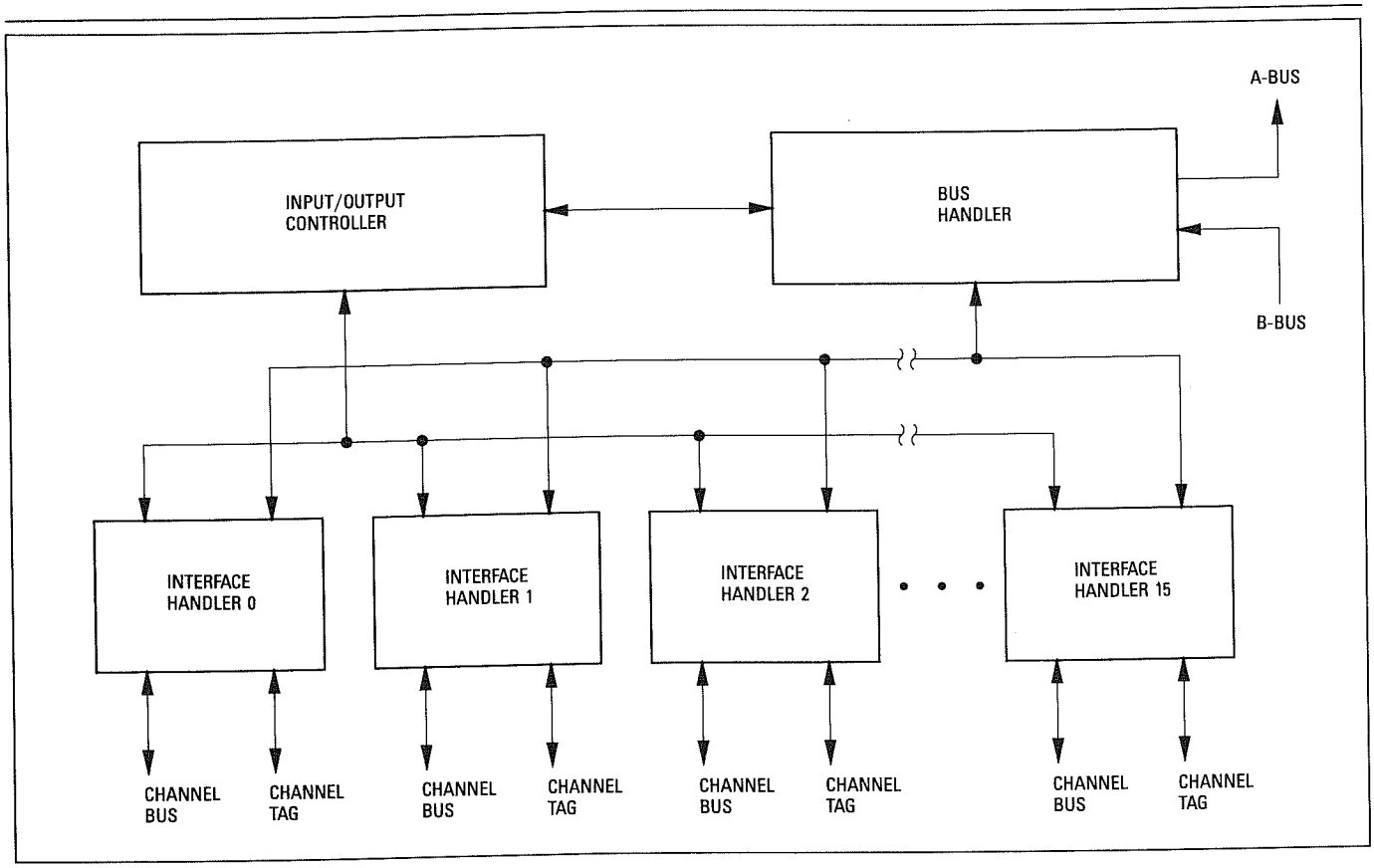

FIGURE 7-1 Input/Output Processor Bus and Channel Paths

7.2.2 Bus Handler

The bus handler is the IOP's interface to the bus system, external director, and main storage. It requests main storage accesses on behalf of the input/output controller and interface handlers and sends and receives messages for the input/output controller. After initiation by the input/output controller, all main storage-device data transfers are controlled by the bus handler and associated interface handler.

The A and B buses provide internal data communication and control for the components of the 5890 processors and internal message recycling.

The unidirectional A and B buses carry data and/or messages between the external director, IOPs, and system support processor. The buses are 72 bits wide to allow transmission of eight data bytes and associated parity information.

7.3 Interface Handlers

The interface handlers provide logical and electrical interfaces to the peripheral device control units, and support either block- or byte-multiplexer channels. Temporary data storage by the interface handlers ensures the timely data transfer to or from any attached external devices. Each interface handler supports one channel.

An interface handler performs normal data transfer operations necessary to provide the external interface to a peripheral device, including channel bus and tag manipulations as well as data buffering. The definition of channel protocols is handled solely by the interface handlers. The I/O protocol, interlock or data streaming, is determined by setup options defined for each block multiplexer interface handler.

Two interface handlers are physically implemented on a single 12-layer printed circuit board using the same ECL technology as the MCCs. These boards, referred to as double density interface handlers, are housed in the system support unit. There are two types of double density interface handlers, one with both interface handlers designed as block-multiplexer channels, and the other with one interface handler designed as a block-multiplexer channel and the other as a byte-multiplexer channel. Channels configured as a byte-multiplexer channel must have the latter type double density interface handler installed.

8 Console Subsystem

This section describes the 5890 console subsystem. The components of the console subsystem are the system support processor, the console support processor, operator consoles, and interfaces to the rest of the system. An overview of the console subsystem is shown in figure 8-1.

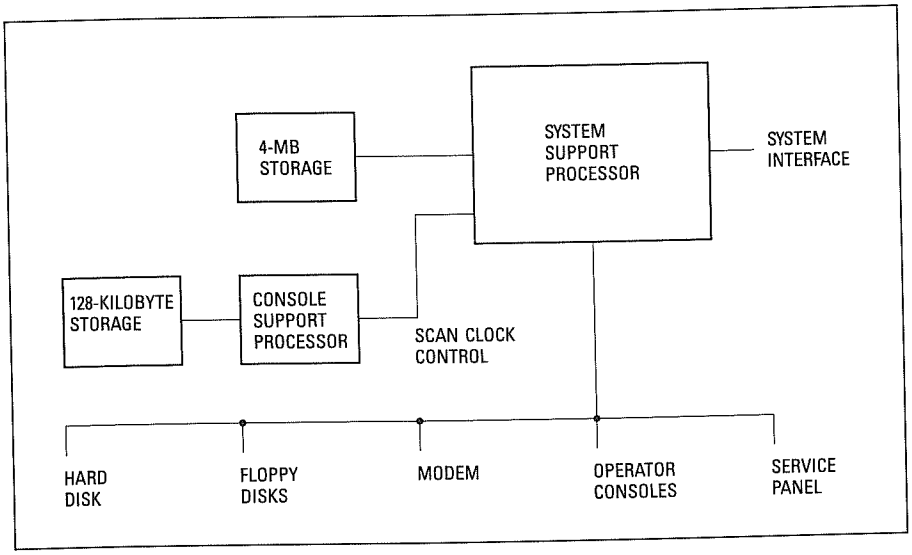

FIGURE 8-1 Console Subsystem Block Diagram

8.1 Console Functions

The console functions are performed by the system support processor. The primary functions are:

- System control functions such as reset, microcode load, and Macrocode load.
- System or domain console during normal operations.
- Monitoring and display of system activity.
- Monitoring and display of system status.
- Error logging, recovery, and problem determination when a failure is detected.
- Event logging for tracking of system activity.
- AMDAC interface for remote problem diagnosis.

8.2 System Support Processor

The system support processor is a complete computer system with its own processor, peripherals, and storage. Its processor implements a subset of the System/370 architecture. Its peripherals include a hard disk, two floppy disk drives, up to four operator terminals, and a modem used for connection to AMDAC.

8.3 Console Support Processor

The console support processor acts as the support processor for the system support processor. The console support processor accesses the operator terminals for its user interface. In normal machine operations, the console support processor is not visible to the customer. It can be used by Amdahl service personnel for system support processor initialization and diagnosis.

The system support processor and the console support processor are implemented on one MCC, referred to as the console MCC.

8.4 Operator Consoles

Each 5890 uniprocessor or dual processor has one main operator console and up to three optional remote operator consoles. An operator console may operate in one of four capacities:

- As a system console, performing system control functions and monitoring tasks, such as domain definition, logical processor reset, and IPL.
- As a maintenance console, monitoring system functions as well as performing problem diagnosis.
- As an AMDAC console, communicating between the dual processor system and the AMDAC network.
- As a backup operator console, conducting normal operational tasks associated with controlling and monitoring an SCP, in the event that the customer's 3278-type operator consoles are not available. An operator console used as a backup SCP console must be on a byte-multiplexer channel.

The main operator console contains the hard disk drive, the floppy disk drives, and the modem. In addition, it contains an operator terminal and a maintenance panel with associated lights and switches. Each remote operator console contains an operator terminal.

8.5 System Interface

There are three different types of system-to-console interfaces. The scan control interface provides the ability to scan-in and scan-out all latches in the system. This interface can also be used to read and write all the LSI RAMs in the system.

The bus interface provides the console with the ability to send and receive bus messages. Messages can be used to alter and display memory, to configure channels, and to receive commands from the system.

Console immediate control is a set of signals used by the console to control and monitor the system. Some of the uses are for resets, clock control, and system activity monitoring.

System interfaces are implemented on the console MCC.

8.6 System Activity Monitor

The System Activity Monitor (SAM) collects and displays system utilization data such as CPU busy or channel busy (figure 8-2). It accumulates samples, counts, computes percentages, and formats the results. SAM displays the results on as many as 18 horizontal graphs with appropriate titles and headings. Setup and change options control collection and display of system data. The SAM function can be started or stopped at any time without affecting system operation or performance. For additional information about SAM and its operation, see the *Amdahl 580 Series 5890 Operation Manual.*

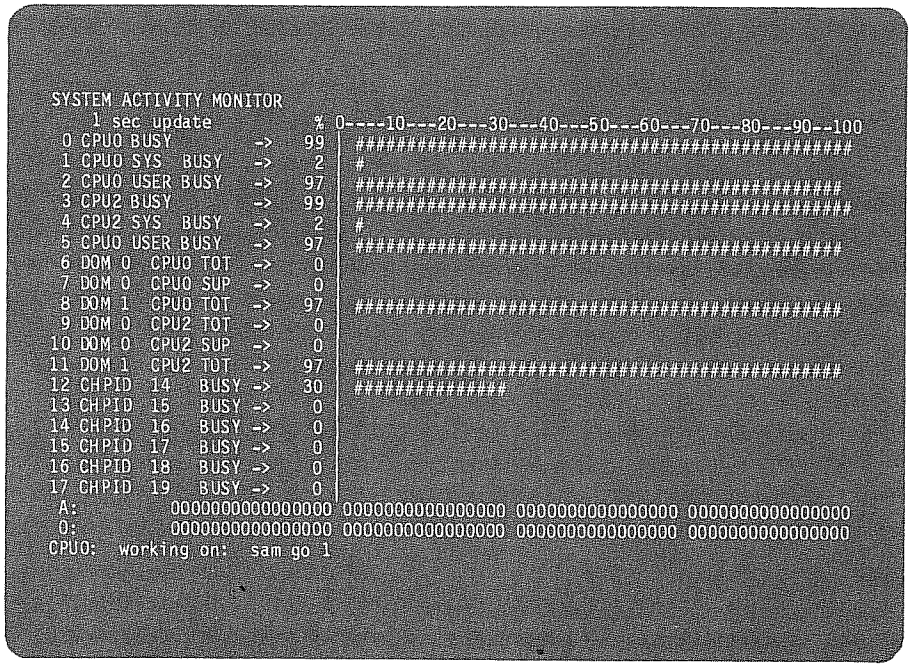

FIGURE 8-2 Sample System Activity Monitor Display

9 Macrocode

This chapter provides information concerning Macrocode, a class of firmware used to create and maintain a processing environment for an SCP. Macrocode provides:

- Facilities to manipulate resources associated with the dual processor complex.
- Model-dependent logout and recovery.
- Configuration definition facilities to define resources allocated to a domain. Configurations can be saved for later recall and activation.
- Facilities for creating, editing, saving, and invoking sets of operator commands called function lists (FLISTs). An FLIST can be saved and later recalled to simplify operator functions.

The *Amdahl 580 Series 5890 Control System Reference Manual* has complete information concerning the use of Macrocode and the facilities provided.

10 Optional Features

This section provides information on optional features available for the 5890 uniprocessors and dual processors.

10.1 Additional Main Storage

On the 5890 uniprocessors, main storage may be increased from 32 MBs to 256 MBs. On the 5890 dual processors, main storage may be increased from 64 MBs to 256 MBs.

10.2 Additional Channels

5890 uniprocessors may be extended from 16 to 48 channels.

5890 dual processors may be extended from 32 to 64 channels.

10.3 580/EDAS High Speed Channel Feature

The 580/EDAS High Speed Channel Feature offers improved I/O response time and higher system throughput by increasing data transfer rates to 4.5 MB/second when accessing Amdahl's 6680 EDAS product.

10.4 Channel-to-Channel Adapter

A CCA makes the channel of one system appear as a control unit to the channel of another system. Under 580/MDF, a CCA may also be used between two channels assigned to two different domains. A CCA synchronizes the operations performed on the two channels. Up to four CCAs can be installed on a 5890 uniprocessor or dual processor.

10.5 Hardware Monitor Attachment Feature

The Hardware Monitor Attachment Feature provides signal collection, signal processing, and standard interfacing necessary to attach customer-supplied, commercially available hardware monitors to the 5890 processor. The signals available include:

- CPU State: Supervisor, Stop, Wait
- Channel Operation (active)
- Protect Key
- Domain ID
- Instruction End Operation

10.6 Remote Operator Consoles

A 5890 uniprocessor or dual processor can attach up to three remote operator consoles at distances up to 1,500 meters from the main operator console.

10.7 580/Multiple Domain Feature

580/MDF extends the domain concept by supporting up to four domains on a 5890 uniprocessor or dual processor.

With 580/MDF, the user controls the allocation of system resources. The user decides what resource allocation best meets the individual requirements. Then, using simple operator commands, the user distributes system resources among domains.

In addition, 580/MDF provides the capability to address a variety of operational requirements such as:

- Testing: 580/MDF permits the user to establish testing environments that are available during prime shift without requiring standalone processors. It allows applications development personnel to conduct parallel testing with normal production operations. It permits data center operations to install and verify new peripheral hardware in a timely fashion.
- Non-homogeneous environments: 580/MDF allows the user to consolidate different environments, now running on separate systems, into one processor. These may include special SCP facilities, "departmental" processors, service bureaus, and limited use environments.
- Conversions: 580/MDF allows continuous adjustment of the resource allocation during conversions. At the start of a conversion process, a majority of the resources are normally allocated to the production environment. As the conversion progresses, resources can be gradually shifted to the new environment. 580/MDF is ideally suited to assist the 5890-200E and 5890-300E processor user in the conversion from MVS/370 to MVS/XA.
- Security: 580/MDF provides complete protection for each domain from interference by other domains. Thus, a domain can be used to establish an operating environment for those users who have special security requirements.

580/MDF supports both System/370 and 370-XA architectural modes and current releases of supported SCPs, operating concurrently in any combination. Supported SCPs are listed in chapter 1.4, Compatibility.

Appendix A

TABLE A-1

Standard Features

5890 UNIPROCESSOR AND DUAL PROCESSOR FEATURES	S/370 MODE NATIVE	S/370 (SIE) GUEST	370-XA MODE NATIVE	370-XA (SIE) GUEST
Basic-Control Mode	Y	Y	NA[1]	NA[1]
Bimodal Addressing	NA	NA	Y	Y
Branch and Save	Y	Y	Y	Y
Byte-Oriented Operand	Y	Y	Y	Y
Channel Indirect Data Addressing	Y	H	Y	Y
Channel Set Switching	Y	H	NA[2]	NA[2]
Channel Subsystem	NA	NA	Y	Y
Clear I/O	Y	H	NA[2]	NA[2]
Command Retry	Y	Y	Y	Y
Conditional Swapping	Y	Y	Y	Y
CPU Timer and Clock Comparator	Y	Y	Y	Y
Extended Precision Divide	NA	NA	Y	Y
Extended Precision Floating Point	Y	Y	Y	Y
Extended Real Addressing	Y	Y	NA[3]	NA[3]
Fast Release	Y	H	NA[2]	NA[2]
Floating Point Arithmetic	Y	Y	Y	Y
Halt Device	Y	H	NA[2]	NA[2]
Incorrect Length Indication Suppression	NA	NA	Y	Y
Interpretative Execution	NA	NA	Y	H
Interval Timer	Y	Y	NA	NA
I/O Extended Logout	Y	H	NA	NA
Key Controlled Storage Protection	Y	Y	Y[4]	Y[4]
Limited Channel Logout	Y	H	NA[2]	NA[2]
Monitoring	Y	Y	Y	Y

5890 UNIPROCESSOR AND DUAL PROCESSOR FEATURES	S/370 MODE NATIVE	S/370 (SIE) GUEST	370-XA MODE NATIVE	370-XA (SIE) GUEST
Multiprocessing				
CPU Address Identification	Y	H	Y	Y
CPU Signaling and Response	Y	H	Y	Y
Prefixing	Y	H	Y	Y
Shared Main Storage	Y	H	Y	Y
TOD Clock Synchronization	Y	H	Y	H
Page Protection	NA	NA	Y	Y
PSW Key Handling	Y	Y	Y	Y
Recovery Extensions	Y	H	NA	NA
Segment Protection	Y	Y	NA[5]	NA[5]
Service Signal	Y	H	Y	H
Status Verification	NA	NA	Y	Y
Storage-Key-Instruction Extension	Y	Y	Y	Y
Storage-Key Instructions (ISK, SSK)	Y	Y	NA[4]	NA[4]
Storage-Key 4-kilobyte Blocks				
Single-Key 4-kilobyte Blocks	Y	Y	Y	Y
Storage-Key Exception Control	Y	Y	NA[4]	NA[4]
System/370 Extended Facility	Y	Y	Y	Y
System/370 I/O Instructions	Y	H	NA[2]	NA[2]
Test Block	Y	Y	Y	Y
Time-of-Day Clock	Y	Y	Y	Y
Tracing (ASN, Branch and Explicit)	NA	NA	Y	Y

5890 UNIPROCESSOR AND DUAL PROCESSOR FEATURES	S/370 MODE NATIVE	S/370 (SIE) GUEST	370-XA MODE NATIVE	370-XA (SIE) GUEST
Translation				
Dynamic Address Translation				
4-kilobyte Page Size	Y	Y	Y	Y
64-kilobyte Segment Size	Y	Y	NA	NA
1M-kilobyte Segment Size	Y	Y	Y	Y
Extended Control Mode	Y	Y	NA[1]	NA[1]
Program Event Recording	Y	Y	Y	Y
Set System Mask Suppression	Y	Y	Y	Y
Store Status	Y	Y	Y	Y
3033 Extension				
Dual Address Space	Y	Y	Y[6]	Y[6]
SIOF Queuing	Y	H	NA[2]	NA[2]
Suspend and Resume	Y	H	NA[2]	NA[2]
31-Bit Indirect-Data-Address Words	Y	H	Y	Y
31-Bit Real Addressing	NA	NA	Y	Y

GLOSSARY

Y Implemented as defined in the appropriate principles of operation manual for this architectural mode.

NA Not applicable to this architectural mode.

H May be simulated for the guest by the host software; direct interpretive execution is not available.

NOTES

1 In 370-XA mode, operation is similar to EC-mode operation in S/370 mode.

2 In 370-XA mode, the channel subsystem provides equivalent function.

3 In 370-XA mode, 31-bit real addressing provides equivalent function.

4 The ISK, RRB, and SSK instructions are not defined in 370-XA; extended storage key instructions provide equivalent function.

5 In 370-XA mode, page protection provides equivalent function.

6 In 370-XA mode, dual address space (DAS) tracing is not available; address space number (ASN) tracing provides equivalent function.

TABLE A-2

Programming Assists

5890 UNIPROCESSOR AND DUAL PROCESSOR PROGRAMMING ASSISTS	S/370 MODE NATIVE	S/370 (SIE) GUEST	370-XA MODE NATIVE	370-XA (SIE) GUEST
Control Switch Assist	Y	NA	NA[1]	NA[1]
Preferred Machine Assist	Y	NA	NA[1]	NA[1]
System/370 Extended Facility				
MVS-Dependent Portion				
Four Lock-Handling Instructions	Y	Y	Y	Y
Six Tracing Instructions	Y	Y	NA[2]	NA[2]
Fix Page Instruction	Y	Y	NA	NA
SVC Assist Instruction	Y	Y	Y	Y
Add Functional Recovery Routine Instruction	Y	Y	Y	Y
VM Assist for MVS/370 Assists	Y	Y	NA[1]	NA[1]
Virtual Machine Assist	Y	NA	NA[1]	NA[1]

GLOSSARY

Y Provided as a standard feature for this architectural mode.

NA Not applicable to this architectural mode.

H May be simulated for the guest by the host software; direct interpretive execution is not available.

NOTES

1 580/MDF and SIE both provide concurrent execution of multiple guest SCPs.

2 370-XA tracing provides equivalent function.

Appendix B

TABLE B-1

5890-190E Uniprocessor Feature Availability

FEATURES	STANDARD CONFIGURATION	EXPAND TO	INCREMENTS OF
Main Storage (MB)	32	128	32
		256	64
Block-Multiplexer Channels	16	48	8
Byte-Multiplexer Channels	—	12	1
Total Channels	16	48	8
Channel-to-Channel Adapters	—	4	1
Main Operator Console	1	—	—
Remote Operator Console	—	3	1
Power Distribution Unit	1	—	—
580/Expanded Storage	Standard		
580/VM Performance Assist	Standard		
580/Multiple Domain Feature	Optional		
580/EDAS High Speed Channel Feature	Optional		
Hardware Monitor Attachment Feature	Optional		
Performance	0.54 times a 5890-300E		
Upgrade to	5890-300E, 5890-400E, 5890-600E		

NOTE:

The workloads used to estimate relative performance are approximations of true production workloads. Relative performance for a specific customer workload will vary, depending on the customer's application and operating environment.

TABLE B-2

5890-200E Dual Processor Feature Availability

FEATURES	STANDARD CONFIGURATION	EXPAND TO	INCREMENTS OF
Main Storage (MB)	64	128	32
		256	64
Block-Multiplexer Channels	32	48	8
		64	16
Byte-Multiplexer Channels	—	16	1
Total Channels	32	64	8,16
Channel-to-Channel Adapters	—	4	1
Main Operator Console	1	—	—
Remote Operator Console	—	3	1
Power Distribution Unit	1	—	—
580/Expanded Storage	Standard		
580/VM Performance Assist	Standard		
580/Multiple Domain Feature	Optional		
580/EDAS High Speed Channel Feature	Optional		
Hardware Monitor Attachment Feature	Optional		
Performance	0.82 times a 5890-300E		
Upgrade to	5890-300E, 5890-400E, 5890-600E		

NOTE:

The workloads used to estimate relative performance are approximations of true production workloads. Relative performance for a specific customer workload will vary, depending on the customer's application and operating environment.

TABLE B-3

5890-300E Dual Processor Feature Availability

FEATURES	STANDARD CONFIGURATION	EXPAND TO	INCREMENTS OF
Main Storage (MB)	64	128	32
		256	64
Block-Multiplexer Channels	32	48	8
		64	16
Byte-Multiplexer Channels	—	16	1
Total Channels	32	64	8,16
Channel-to-Channel Adapters	—	4	1
Main Operator Console	1	—	—
Remote Operator Console	—	3	1
Power Distribution Unit	1	—	—
580/Expanded Storage	Standard		
580/VM Performance Assist	Standard		
580/Multiple Domain Feature	Optional		
580/EDAS High Speed Channel Feature	Optional		
Hardware Monitor Attachment Feature	Optional		
Performance	1.85–2.2 times a 5870		
Upgrade from	5890-190E, 5890-200E		
Upgrade to	5890-400E, 5890-600E		

NOTE:

The workloads used to estimate relative performance are approximations of true production workloads. Relative performance for a specific customer workload will vary, depending on the customer's application and operating environment.

TABLE B-4

5890-190E Physical Characteristics*

Power Consumption	50 Hz: 7.4 kVA 60 Hz: 7.1 kVA 400 Hz: 21.6 kVA
Heat Dissipation	20.1 kW (68.5 kBTUs) per hour
Floor Space	
Without Service Clearance	7.5 sq m (81.1 sq ft)
With Service Clearance	21.6 sq m (232.4 sq ft)
Weight	2,931 kg (6,461 lbs)
Temperature Requirements	
Underfloor Air	10–19°C (50–66°F)
Room Air	16–32°C (60–90°F)
Humidity Requirements	
Underfloor Air	50–80%
Room Air	20–80%

*For a standard configuration 5890-190E Uniprocessor, including mainframe, main operator console, and power distribution unit.

TABLE B-5

5890-200E and 5890-300E Physical Characteristics*

Power Consumption	50 Hz: 8.4 kVA 60 Hz: 8.2 kVA 400 Hz: 33.6 kVA
Heat Dissipation	27.3 kW (93.0 kBTUs) per hour
Floor Space	
Without Service Clearance	7.5 sq m (81.1 sq ft)
With Service Clearance	21.6 sq m (232.4 sq ft)
Weight	3,162 kg (6,971 lbs)
Temperature Requirements	
Underfloor Air	10–19°C (50–66°F)
Room Air	16–32°C (60–90°F)
Humidity Requirements	
Underfloor Air	50–80%
Room Air	20–80%

*For a standard configuration 5890-200E or 5890-300E Dual Processor, including mainframe, main operator console, and power distribution unit.

Bibliography

The following related publications provide additional information about the 5890 uniprocessor and dual processor function and operation.

Amdahl Publications

MC-108334	*Amdahl Computing Systems Physical Planning Manual*
MC-119387	*Amdahl 580 Series 5890 Operation Manual*
MC-119400	*Amdahl 580 Series 5890 Control System Reference Manual*
MC-119425	*Amdahl 580 Series 5890 Control System Messages and Codes*
MC-119428	*Amdahl 580 Series 5890 Control System Concepts Manual*

IBM Publications

GA22-6974	*IBM System/360 and System/370 I/O Interface Channel to Control Unit Original Equipment Manufacturers' Information*
GA22-7000	*IBM System/370 Principles of Operation*
SA22-7085	*IBM System/370 Extended Architecture Principles of Operation*
SA22-7095	*IBM System/370 Extended Architecture Interpretive Execution*
GA22-7079	*IBM System/370 Assists for MVS*
SA22-7092	*IBM Assists for MVS/XA*
GC28-1027	*IBM Input/Output Configuration Program Users's Guide and Reference*

Glossary

ac Alternating Current

AMDAC Amdahl Diagnostic Assistance Center

AMDEREP Amdahl Environmental, Recording, Editing, and Printing

A-Phase Address generation phase of pipeline function

ASN Address Space Number

BLC Basic Logic Card

B-Phase Buffer (Operand Cache) access phase of pipeline function

CCA Channel-to-Channel Adapter

CEU Channel Extension Unit

chip An integrated circuit etched onto a piece of semiconductive material

CIC Console Immediate Control

CPU Central Processing Unit

CSP Console Support Processor

CSU CPU Storage Unit

DASD Direct Access Storage Device

DAT Dynamic Address Translation

dc Direct Current

D-Phase Decode instruction phase of pipeline function

DRAM Dynamic Random Access Memory

ECC Error Checking and Correction

ECL Emitter-Coupled Logic

EPO Emergency Power Off

EREP Environmental, Recording, Editing, and Printing

ES See 580/ES

E-Unit Execution Unit

EXT External Director

FCC Federal Communications Commission

580/EDAS HSCF 580/EDAS High Speed Channel Feature

580/ES 580/Expanded Storage

580/MDF 580/Multiple Domain Feature

580/VMPA 580/VM Performance Assist

FLIST Function List

FRU Field-Replaceable Unit

HMAF Hardware Monitor Attachment Feature

HSA Hardware System Area

Hz Hertz

IEF Interpretive Execution Facility

IH Interface Handler

I/O Input/Output

IOC Input/Output Controller

IOCP I/O Configuration Program

IOCDS I/O Configuration Data Set

IOEL Input/Output Extended Logout

IOP Input/Output Processor

I-Fetch Instruction Fetch

I-Unit Instruction Unit

KB kilobyte (1,024 bytes)

kBTUs Thousand British Thermal Units

kVA kilovoltampere

kW kilowatt

LSI Large Scale Integration

MB See megabyte

MCC Multiple Chip Carrier

MCEL Machine Check Extended Logout

MDF See 580/MDF

Megabyte 1,048,576 bytes

MOC Main Operator Console

MSA Main Storage Array

MSU Main Storage Unit

MVS/SP MVS/System Product

MVS/370 MVS/SP Version 1

MVS/XA MVS/SP Version 2

ns nanosecond

OWR Operand Word Register

PCB Printed Circuit Board

PDB Power Distribution Box

PDU Power Distribution Unit

PFX/DBA Prefix and Domain Base Adjust mechanism

PRU Processor Unit

PSU Power Supply Unit

RAM Random Access Memory

RMF Resource Management Facility

ROC Remote Operator Console

SAM System Activity Monitor

SCP System Control Program

SIE Start Interpretive Execution

SRM System Resource Manager

SSP System Support Processor

SSU System Support Unit

S/370 Architecture defined by the *IBM System/370 Principles of Operation*

STIDC STORE CHANNEL ID

STIDP STORE CPU ID

370-XA Architecture defined by the *IBM System/370 Extended Architecture Principles of Operation*

TLB Translation Lookaside Buffer

TOD Time-of-Day

UPC Unit Power Controller

VM Virtual Machine

VMPA See 580/VMPA

VM/SP VM/System Product

VM/SP HPO VM/SP with High Performance Option

VM/XA SF VM/XA Systems Facility

W-Phase Write phase of pipeline function

X-Phase Execution phase of pipeline operation