



TECHNICAL MANUAL
FOR

AM-410

DISK DRIVE CONTROLLER
CIRCUIT BOARD SET

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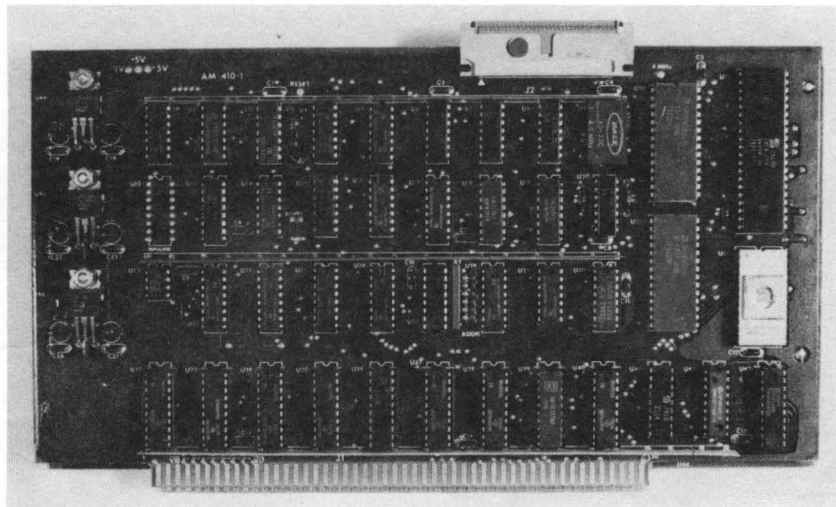
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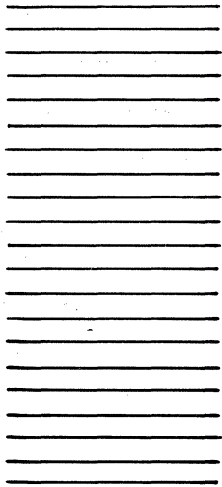
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TABLE OF CONTENTS

Paragraph		Page
SECTION 1 GENERAL DESCRIPTION		
1.0	Introduction	1-1
1.1	Circuit Board Description	1-1
1.2	Application	1-1
SECTION 2 OPERATING DATA		
2.0	Introduction	2-1
2.1	Capabilities and Specifications	2-1
2.2	Installation and Start-Up	2-4
2.2.1	Installation	2-4
2.2.2	System Start-Up.	2-8
2.3	Interface Description	2-9
2.3.1	S-100 Bus Interface	2-9
2.3.2	Disk Drive Interface	2-9
2.4	User Options	2-14
2.4.1	Address Code	2-14
2.4.2	Interrupt Lines.	2-14
2.4.3	Boot Option	2-14
2.4.4	AM-100 Preparation	2-14
SECTION 3 PROGRAMMING		
3.0	Introduction	3-1
3.1	Unique Software Considerations	3-1
3.2	Addressing	3-2
3.3	Initialization	3-2
3.4	Command Register	3-2
3.5	Status Register	3-3
3.6	Interrupt Mode	3-3
3.7	Handshake Sequence	3-3
3.8	DMA Buffer	3-7
3.8.1	DMA Buffer Operation for Disk Write.	3-10

Paragraph		Page
	SECTION 3 PROGRAMMING (Continued)	
3.8.2	DMA Buffer Operation for Disk Read	3-10
3.8.3	Physical Address	3-11
3.9	Restore Command	3-11
3.10	Status Check	3-12

SECTION 4 FUNCTIONAL THEORY OF OPERATION

4.0	Introduction	4-1
4.1	Circuit Board Operation	4-1
4.1.1	Power-Up Reset	4-24
4.1.2	Addressing	4-24
4.1.3	CPU Output	4-24
4.1.3.1	Command Data	4-25
4.1.3.2	Command Types	4-25
4.1.3.3	Output Data	4-30
4.1.4	CPU Input	4-30
4.1.4.1	Status Register	4-30
4.1.4.2	Status Word Formats.	4-31
4.1.4.3	Input Data Register.	4-31
4.1.5	Boot Load Procedure.	4-31
4.1.6	Interrupts	4-33
4.1.7	Byte Clock Counter	4-34
4.1.8	Disk Transfer Logic.	4-34
4.1.9	Sector Counter	4-34
4.1.10	Output to Disk Drive	4-35
4.1.10.1	Data Write Logic	4-35
4.1.10.2	Disk Drive Controls.	4-36
4.1.11	Input From Disk Drive.	4-36
4.1.12	AM-410 Board Set Operations and Timing	4-37
4.1.12.1	Data Transfer Operations	4-37
4.1.12.2	Disk Transfer Operations	4-38
4.1.12.3	Disk Read Clocks	4-39

Paragraph		Page
SECTION 4 FUNCTIONAL THEORY OF OPERATION		
(Continued)		
4.1.12.4	Disk Write Clocks	4-40
4.1.12.5	Sector Beginning Format Operations	4-40
4.1.12.6	Sector End Format Operations	4-42
4.1.12.7	DMA Transfer Operations	4-43
4.2	Circuit Module Description	4-44
4.2.1	CPU Microprocessor (AM-410-1, U10, U21).	4-44
4.2.1.1	Instruction Op-Code Fetch	4-49
4.2.1.2	Memory Read or Write Cycles.	4-50
4.2.1.3	Input or Output Cycles	4-51
4.2.1.4	Interrupt Request/Acknowledge Cycle	4-51
4.2.1.5	CPU Instruction Set	4-52
4.2.2	DMA Address Generator (AM-410-1, U10, U21)	4-57
4.2.2.1	Architecture	4-58
4.2.2.2	Control Modes.	4-62
4.2.2.3	Instructions	4-63
4.2.3	Cyclic Redundancy Check (CRC) Generator/ Checker (AM-410-1, U15)	4-65
4.2.4	Dual D Positive-Edge-Triggered Flip-Flops With Preset and Clear (AM-410-2, U37, U40, U44)	4-68
4.2.5	Dual J-K Negative-Edge-Triggered Flip-Flops With Preset and Clear (AM-410-1, U17).	4-68
4.2.6	Decoder (AM-410-1, U25, U26; AM-410-2, U7, U42)	4-69
4.2.7	Decoder/Demultiplexer (AM-410-1, U30)	4-70
4.2.8	Data Selector/Multiplexer (AM-410-1, U13).	4-71
4.2.9	Quad 2-Line to 1-Line Data Selector/Multiplex- er (AM-410-2, U23, U43)	4-72
4.2.10	Quad Inverting Two-Line to One-Line Data Selector/Multiplexer (AM-410-1, U18, U19)	4-73
4.2.11	Four-Bit Binary Counter with Asynchronous Clear (AM-410-2, U34)	4-74

Paragraph	Page
SECTION 4 FUNCTIONAL THEORY OF OPERATION	
(Continued)	
4.2.12	Four-Bit Binary Counter with Synchronous Clear (AM-410-2, U41) 4-77
4.2.13	Eight-Bit Serial In/Parallel Out Shift Regis- ter (AM-410-2, U31) 4-80
4.2.14	Eight-Bit Parallel In/Serial Out Shift Regis- ter (AM-410-2, U25) 4-81
4.2.15	Quad D Flip-Flops with Clear (AM-410-2, U13, U19) 4-83
4.2.16	Inverting Tri-State Buffer (AM-410-1, U34) . . 4-84
4.2.17	Octal D-Type Flip-Flop with Clear (AM-410-1, U35) 4-85
4.2.18	Tri-State Hex Buffers (AM-410-1, U28; AM-410-2, U33) 4-86
4.2.19	Octal D-Type Transparant Latch (AM-410-1, U39) 4-87
4.2.20	Tri-State D Flip-Flops (AM-410-1, U37, U38, U40; AM-410-2, U8, U12, U14, U18, U20, U24, U30) 4-88
4.2.21	Dual 4-Bit Binary Counter (AM-410-2, U32). . . 4-89
4.2.22	1024 x 4 Bit Static Random Access Memory (AM-410-1, U41, U42) 4-90
4.2.23	Bus Comparator (AM-410-1, U27; AM-410-2, U26). 4-91
4.2.24	Tri-State Octal Buffers (AM-410-1, U36; AM-410-2, U6). 4-92
4.2.25	Tri-State Inverting Octal Buffers (AM-410-2, U36) 4-93
4.2.26	Bidirectional Transceiver (AM-410-1, U43). . . 4-94

Paragraph		Page
	SECTION 5 MAINTENANCE AND TROUBLESHOOTING	
5.0	Introduction	5-1
5.1	Circuit Board Checkout	5-1
5.2	Warranty Procedures	5-2
5.3	Troubleshooting Procedures	5-2
5.3.1	Communications and Memory Test	5-4
5.3.2	Positioning Test	5-5
5.3.3	Data Transfer Test	5-6
5.3.4	Interrupt Circuitry Test	5-8
5.3.5	All Tests	5-8
5.3.6	Alignment Test	5-8
5.3.7	Test Modifications	5-9
5.4	Cartridge Module Drive (CMD) Alignment Pro- cedure	5-9
5.4.1	Equipment Required	5-11
5.4.2	General CMD Alignment Principles	5-12
5.4.3	Initial Head Alignment Procedures.	5-16
5.4.4	Cartridge Data Head Alignment Procedure.	5-29
5.4.5	Cartridge Servo Head Alignment Procedure	5-30
5.4.6	Fixed Disk Module Data Read/Write Head Alignment Procedure	5-30
5.4.7	Fixed Module Servo Head Alignment Procedure.	5-32
5.5	Preventive Maintenance	5-34
5.5.1	Prefilter and Absolute Filter Removal and Replacement	5-36
5.5.2	Actuator Assembly Inspection and Cleaning with Fixed Disk Module Still in the Drive	5-38
5.5.3	Power Supply Check	5-38

SECTION 6 SCHEMATIC AND PARTS LIST

LIST OF ILLUSTRATIONS

Figure	Page
1-1	AM-410 Simplified Block Diagram 1-3
2-1	Disk Drive Interface Cabling 2-5
2-2	Location of Jumpers for User Options. 2-15
3-1	AM-410 Commands 3-4
3-2	AM-410 Status Words 3-5
3-3	DMA Buffer Operation. 3-6
3-4	Handshake Sequence. 3-8
3-5	DMA Transfer Sequence 3-9
4-1	AM-410-1 Functional Block Diagram 4-3
4-2	AM-410-2 Functional Block Diagram 4-5
4-3	Status Word Formats 4-32
4-4	Data Transfer Timing. 4-37
4-5	Disk Transfer Timing. 4-38
4-6	BYTCLK-BYTENB Timing. 4-39
4-7	Disk Write Timing 4-40
4-8	Sector Beginning Timing 4-41
4-9	Sector End Format Timing. 4-42
4-10	DMA Transfer Timing 4-43
4-11	CPU Block Diagram 4-45
4-12	CPU Registers 4-45
4-13	CPU Pin Configuration 4-45
4-14	DMA Address Generator Connections 4-58
4-15	DMA Address Generator Block Diagram 4-59
4-16	Control Register Format Definition 4-60
4-17	CRC Checker Connections 4-66
4-18	CRC Equivalent Circuit for $X^{16} + X^{15} + X^2 + 1$. . 4-67
4-19	CRC Check Word Generation 4-67

Figure	Page
4-20	Dual D Flip-Flop Connections 4-68
4-21	J-K Flip-Flop Connections 4-68
4-22	Decoder Connections 4-69
4-23	Decoder/Demultiplexer Connections 4-70
4-24	Data Selector/Multiplexer Logic and Connections . 4-71
4-25	Quad 2-Line to 1-Line Data Selector/Multiplexer Connections 4-72
4-26	Quad Inverting 2-Line to 1-Line Data Selector/ Multiplexer Connections 4-73
4-27	Binary Counter with Asynchronous Clear Logic and Connections 4-75
4-28	Binary Counter with Synchronous Clear Logic and Connections 4-78
4-29	Eight-Bit Shift Register Logic and Connections. . 4-80
4-30	Eight-Bit Parallel-In/Serial-Out Shift Register Logic and Connections 4-81
4-31	Quad D Flip-Flops with Clear, Logic and Connec- tions 4-83
4-32	Inverting Tri-State Buffer Logic and Connections. 4-84
4-33	Octal D-Type Flip-Flop with Clear, Logic and Connections 4-85
4-34	Tri-State Hex Buffer Logic and Connections. . . . 4-86
4-35	Transparent Latch Logic and Connections 4-87
4-36	Tri-State D Flip-Flop Connections 4-88
4-37	Four-Bit Binary Counter Connections 4-89
4-38	RAM Connections 4-90
4-39	Bus Comparator Connections. 4-91
4-40	Tri-State Octal Buffer Logic and Connections. . . 4-92
4-41	Tri-State Inverting Octal Buffers Logic and Con- nections 4-93
4-42	Bidirectional Transceiver Logic and Connections . 4-94

Figure		Page
5-1	Head/Arm Removal and Replacement and Alignment .	5-13
5-2	Head Alignment Block Diagram	5-15
5-3	Guard-Band Waveform Pattern	5-22
5-4	Balanced Dibit Pattern	5-22
5-5	Carriage Locking Tool-Head Alignment Position . .	5-24
5-6	Filter Removal and Replacement	5-37

LIST OF TABLES

Table		Page
2-1	AM-410 Specifications	2-2
2-2	S-100 Bus Interface Signals List.	2-6
2-3	Disk Drive Interface Signals List	2-10
4-1	AM-410 Signals List	4-7
4-2	S-100 Bus Interface Signal Descriptions	4-10
4-3	Disk Drive Interface Signal Descriptions.	4-13
4-4	Tag Bus Decode	4-20
4-5	Non-Disk Command Bits	4-23
4-6	Non-Disk Command Formats	4-24
4-7	Disk Command Bits	4-25
4-8	Disk Command Codes	4-26
4-9	CPU Signal List	4-43
4-10	CPU Instruction Set	4-50
4-11	DMA Register Instructions	4-60
4-12	CRC Polynomial Select Codes	4-64
5-1	Maintenance Index and Schedule	5-34
5-2	Maintenance Materials	5-35
6-1	AM-410-1 Component Cross-Reference List	6-1
6-2	AM-410-2 Component Cross-Reference List	6-2

SECTION 1 GENERAL DESCRIPTION

1.0 INTRODUCTION.

This manual provides operating and maintenance instructions for the AM-410 Disk Drive Controller circuit board set manufactured by Alpha Microsystems Inc., located in Irvine, California. Circuit board description, operating and usage instructions, programming, theory of operation, and maintenance instructions are included to provide the user with the information necessary to utilize this circuit board to its full capability.

1.1 CIRCUIT BOARD DESCRIPTION.

The AM-410 Disk Drive Controller circuit board set provides data processing, control and interface capability between a standard S-100 Bus system and one to four CDC 9448 (Phoenix) hard disk drives. A CPU microprocessor, a DMA address generator, a Random Access Memory (RAM) with associated control logic provide the sophisticated data processing necessary for control of up to four 90-megabyte disk drives. A 2K Read Only Memory (ROM) is contained on the boards to provide a bootstrap load program and also to contain the microcode necessary for the CPU module operation.

A simplified block diagram of the circuit board is shown in Figure 1-1. For a complete detailed description of circuit board operation, see Section 4 of this manual. For programming requirements, see Section 3 of this manual.

1.2 APPLICATION.

This circuit board set provides the data processing and interface capability necessary for operation of up to four CDC 9448 (Phoenix) hard disk drives. This single spindle drive has a formatted capacity of 90 million bytes. Data is transferred

at an average rate of 9.67 MHz between the controller and drives. See Section 2 of this manual for wiring instructions and system interface information. For complete information on the disk drive, see the Control Data Corporation 9448 Hardware Maintenance Manual.

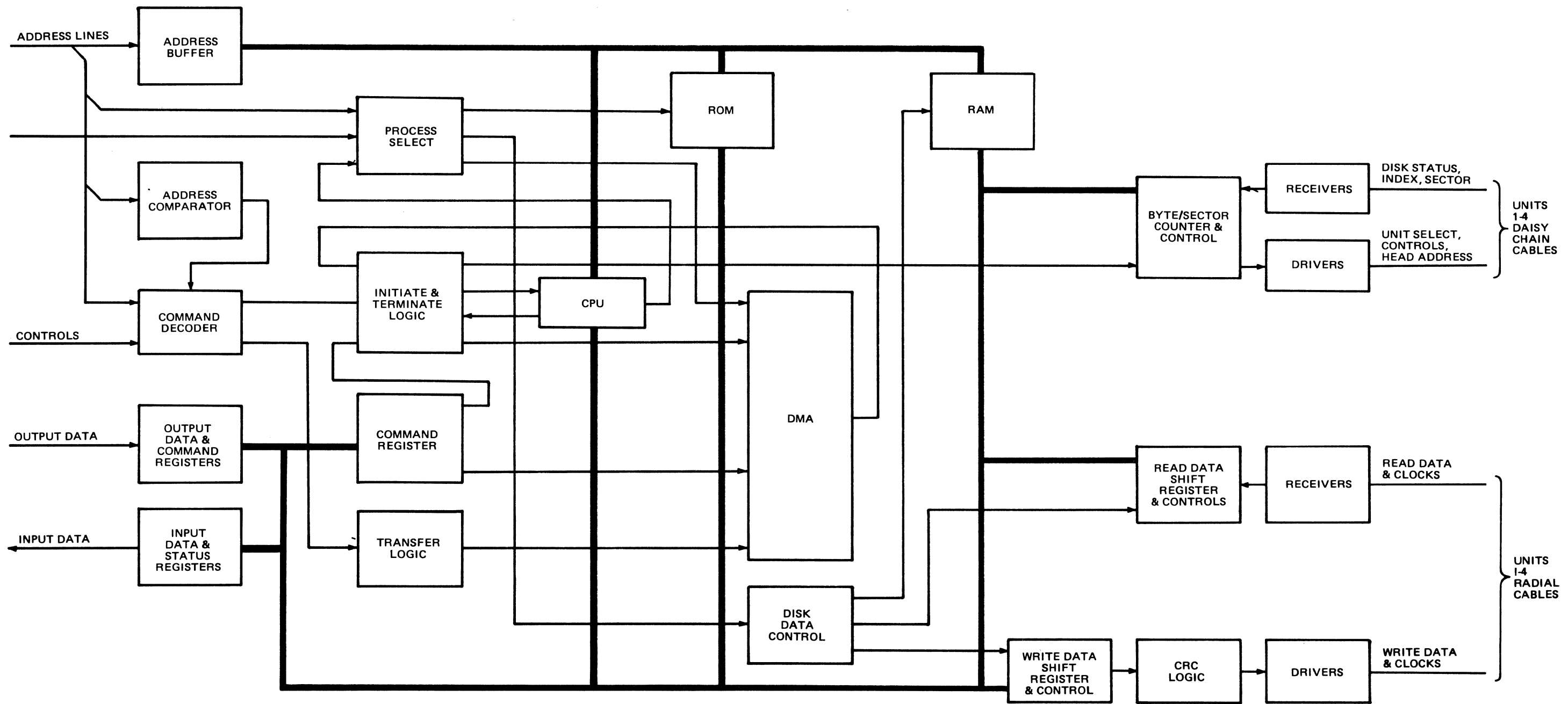


Figure 1-1. AM-410 Simplified Block Diagram

SECTION 2 OPERATING DATA

2.0 INTRODUCTION.

This section contains information on the use of the AM-410 Disk Controller circuit board set. Capabilities, specifications, interface wiring, and user option descriptions are provided for the successful integration of the AM-410 into the user's system.

2.1 CAPABILITIES AND SPECIFICATIONS.

This circuit board set operates from the standard S-100 Bus structure to interface with the CDC 9448 (Phoenix) hard disk drive with 90 megabyte formatted capacity (including 15 megabyte removable cartridge). The two-board set can interface with up to four disk drives. Detailed specifications are contained in Table 2-1.

Table 2-1. AM-410 Specifications

PARAMETER	SPECIFICATIONS
CPU Interface	Standard S-100 Bus
Drives per Controller	1-4
Printed Circuit Boards	2
Data Transfer Modes	Programmed Multi-Level Interrupts, Full Sector Block Transfers.
Data Transfer - Controller to Disk	Serial
Data Transfer - Controller to Computer	8-bit bytes Parallel
Data Transfer Format	512 bytes per sector, plus CRC and sentinel check bytes.
On-Board Buffer	1024 bytes
Error checking	CRC Error Code
Input Power	+8 volts dc @2.5 amps, -16 volts dc @0.45 amps
Interconnections	Two mounting slots of an S-100 bus chassis. One 60-pin cable to first drive (100 feet maximum cumulative length on four drives). Four 26-pin radial cables with one cable to each drive (50 feet maximum individual length).

Table 2-1 (Cont.). AM-410 SPECIFICATIONS

PARAMETER	SPECIFICATIONS
Dimensions	5¼" x 10" (13.3 cm x 25.4 cm)
Environment (operating) Temperature Humidity	60 ^o to 90 ^o F (16 ^o to 32 ^o C) 10% to 80% (non-condensing)

2.2 INSTALLATION AND START-UP.

When the AM-410 circuit board set is received, it is ready for use. No adjustment or calibration is required for operation. The hardware requirements for installation and use are described in this section and the software requirements are described in Section 3.

2.2.1 INSTALLATION.

First ensure that the proper power wiring is available and that the correct voltages are connected to the disk drive and to the various pins of the circuit board as shown in Table 2-2. Connect the cables to the disk drives and connect the cable between the two circuit boards as shown in Figure 2-1.

NOTE

When installing the radial cables (gray), be sure that it is inserted correctly as there are no guides for this connector. Card one in the disk drive may be removed for easier access. In the Phoenix, pin one is up; and on the AM-410, pin one is to the edge. The cable plugs into the face of the board.

Normally the standard grounding is adequate. If desired, a ground wire may be added between the lower right rear of the Phoenix to the back of the CPU chassis.

CAUTION

Use extreme care when closing the deck or the card cage to be sure that the cables near the card cage at the power supply are not pinched.

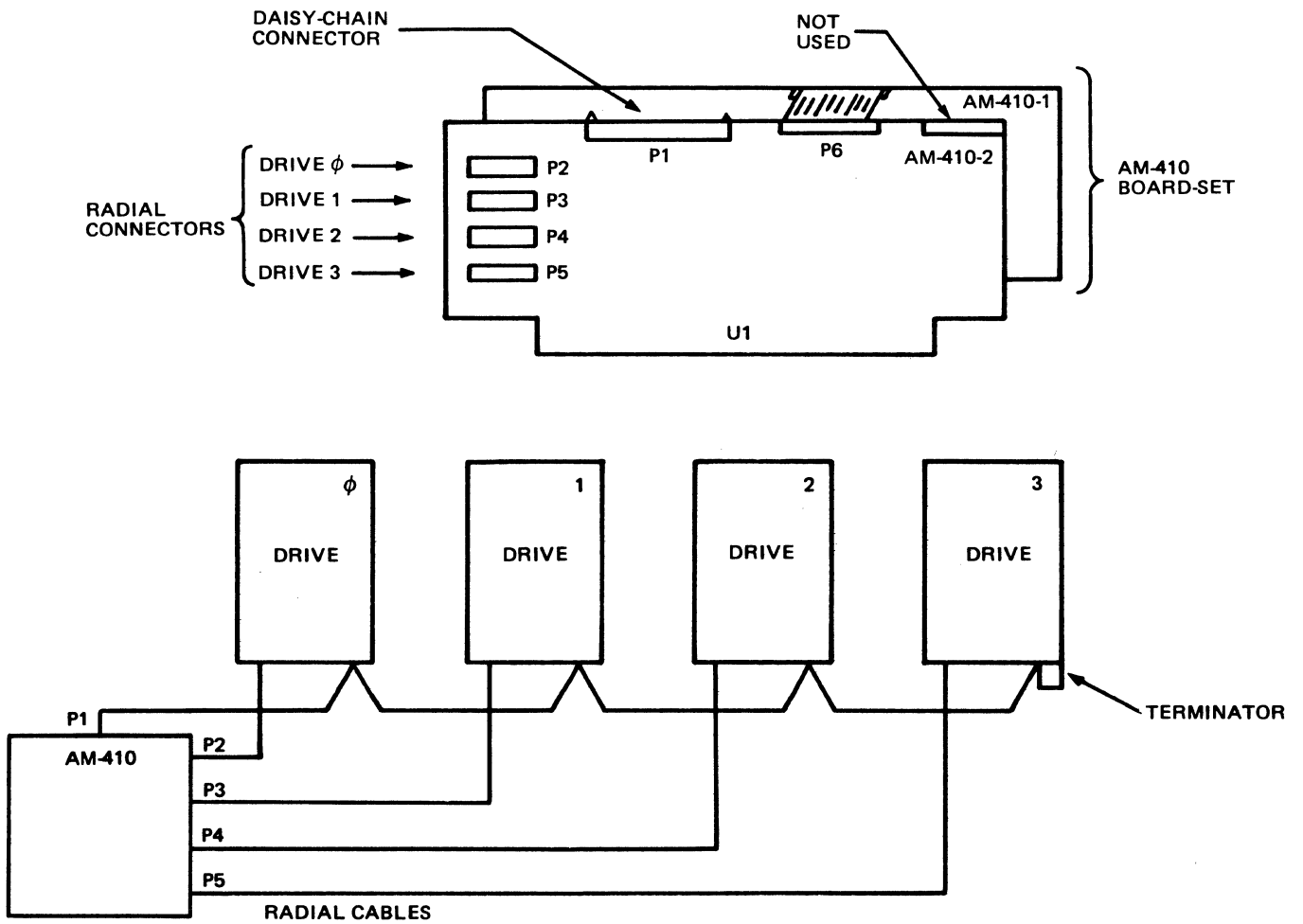


Figure 2-1. Disk Drive Interface Cabling

Table 2-2. S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN
A0	Address 0	79
A1	Address 1	80
A2	Address 2	81
A3	Address 3	31
A4	Address 4	30
A5	Address 5	29
A6	Address 6	82
A7	Address 7	83
A8	Address 8	84
A9	Address 9	34
A10	Address 10	37
A11	Address 11	87
A12	Address 12	33
A13	Address 13	85
A14	Address 14	86
A15	Address 15	32
DATAIN 0	Input Data Bit 0	95
DATAIN 1	Input Data Bit 1	94
DATAIN 2	Input Data Bit 2	41
DATAIN 3	Input Data Bit 3	42
DATAIN 4	Input Data Bit 4	91
DATAIN 5	Input Data Bit 5	92
DATAIN 6	Input Data Bit 6	93
DATAIN 7	Input Data Bit 7	43

Table 2-2 (Cont.). S-100 Bus Interface Signals List

MNEMONIC	NAME	PIN
DATAOUT 0	Output Data Bit 0	36
DATAOUT 1	Output Data Bit 1	35
DATAOUT 2	Output Data Bit 2	88
DATAOUT 3	Output Data Bit 3	89
DATAOUT 4	Output Data Bit 4	38
DATAOUT 5	Output Data Bit 5	39
DATAOUT 6	Output Data Bit 6	40
DATAOUT 7	Output Data Bit 7	90
PDBIN	Data Bus in	78
PHANTOM	Phantom	67
$\overline{\text{PWR}}$	Write Strobe	77
$\overline{\text{PRESET}}$	Reset	75
SINP	I/O Input Cycle	46
SOUT	I/O Output Cycle	45
$\overline{\text{VI0}}$	Interrupt 0	4
$\overline{\text{VI1}}$	Interrupt 1	5
$\overline{\text{VI2}}$	Interrupt 2	6
$\overline{\text{VI3}}$	Interrupt 3	7
$\overline{\text{VI4}}$	Interrupt 4	8
$\overline{\text{VI5}}$	Interrupt 5	9
$\overline{\text{VI6}}$	Interrupt 6	10
$\overline{\text{VI7}}$	Interrupt 7	11
+8VDC	+8VDC	1, 51
GND	Ground	50, 100

NOTE

When inserting the disk cartridge, make sure that all four of the steel carrier pins go into the white rails. If a cartridge cannot be removed, this may be the problem and the loading mechanism must be removed to remove the cartridge.

2.2.2 SYSTEM START-UP.

Cycle up the Phoenix drive using the START/STOP switch on the front panel as described in the Phoenix manual. Normally the AC switch on the back of the Phoenix drives should never be turned off. The CPU box may be turned off and on safely while the Phoenix is cycled down. The RESET button should be held down whenever the CPU box power is switched to avoid false FAULTS.

When the Phoenix disk drive is first received, it must be purged (AC blower on, front panel switch in the STOP position) with the cartridge in place for at least two hours. All new cartridges should be purged for at least one hour before using. In general, purging is required anytime the drive has been opened or the AC blower has been turned off.

On board one inside the Phoenix, the two switches are normally switched away from each other and the red LED is on. With the AM-410, it is possible to have both switches forward. In this position, power fail protection is better but the Phoenix may be more sensitive to power fluctuations.

The DIP switch on the Phoenix servo board selects the sectoring and should have 1, 3, and 6 off.

2.3 INTERFACE DESCRIPTION.

The AM-410 Disk Controller Circuit board set provides interface capability between the standard S-100 Bus and CDC 9448 (Phoenix) disk drives.

2.3.1 S-100 BUS INTERFACE.

The AM-410 circuit board set is fully S-100 bus compatible. The board and its associated disk drives are addressed through the address lines and data is transferred through the standard data in and data out ports. The S-100 bus connections are made via the bottom edge connector and are listed in Table 2-2. For a complete description of these signals and their operation in the AM-410, see Section 4 of this manual.

2.3.2 DISK DRIVE INTERFACE.

One AM-410 Circuit Board set accommodates a maximum of four Phoenix disk drives. Interface connections are made through two cables for each drive. One cable connects to all four drives in a daisy chain (30 twisted pair conductors) and the other cable connects from the AM-410 directly to each disk drive (26 conductor flat ribbon cable called radial cable). Pin one on the daisy chain cable is identified by a light brown and dark brown pair of wires along one edge. Connect pin one of the cable to pin one of the connector on both the drive and the AM-410. Terminate only the last drive in sequence on the daisy chain cable using the terminator card as described in the Phoenix manual.

For further information and drive preparation, see the Control Data Manual on the 9448 Cartridge Module Drive. Interface cabling is shown in Figure 2-1 and all interface signals are listed in Table 2-3. For further information on operation of the AM-410 interface, see Section 4 of this manual.

Table 2-3. Disk Drive Interface Signals List

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN
AMDETECT	Address Mark Found	Out	+P1-50 -P1-20
Bit 0	Tag Bus Bit 0	Out	+P1-34 -P1-4
Bit 1	Tag Bus Bit 1	Out	+P1-35 -P1-5
Bit 2	Tag Bus Bit 2	Out	+P1-36 -P1-6
Bit 3	Tag Bus Bit 3	Out	+P1-37 -P1-7
Bit 4	Tag Bus Bit 4	Out	+P1-38 -P1-8
Bit 5	Tag Bus Bit 5	Out	+P1-39 -P1-9
Bit 6	Tag Bus Bit 6	Out	+P1-40 -P1-10
Bit 7	Tag Bus Bit 7	Out	+P1-41 -P1-11

Table 2-3 (Cont.). Disk Drive Interface Signals List

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN
Bit 8	Tag Bus Bit 8	Out	+P1-42 -P1-12
Bit 9	Tag Bus Bit 9	Out	+P1-43 -P1-13
DATA CLK	Read Clock	In	P2-P5 + 17 - 5 GND 4
FAULT	Fault	In	+P1-45 -P1-15
INDEX	Disk Index	In	+P1-48 -P1-18
ONCYL	On Cylinder	In	+P1-47 -P1-17
OPEN CABLE DETECTOR	Open Cable Detector	Out	+P1-44 -P1-14
POWER SEQ HOLD	Power Sequence Hold	Out	P1-59
POWER SEQ PICK	Power Sequence Pick	Out	P1-29
READ DATA	Read Data	In	P2-P5 + 16 - 3 GND 15

Table 2-3 (Cont.). Disk Drive Interface Signals List

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN
SECTOR	Sector Pulse	In	+P1-55 -P1-25
SEEK END	Seek Operation End	In	P2-P5 + 23 - 10 GND 21
SEEKERR	Seek Error	In	+P1-46 -P1-16
SERVO CLK	Servo Clock	In	P2-P5 + 14 - 2 GND 1
TAG 1 (CYL)	Tag 1 (Cylinder Address)	Out	+P1-31 -P1-1
TAG 2 (HEAD)	Tag 2 (Head/Vol. Select)	Out	+P1-32 -P1-2
TAG 3 (CMD)	Tag 3 (Control Select)	Out	+P1-33 -P1-3
UNIT SELECT BUS 0	Unit Select Bit 2 ⁰	Out	+P1-53 -P1-23

Table 2-3 (Cont.). Disk Drive Interface Signals List

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN
UNIT SELECT BUS 1	Unit Select Bit 2 ¹	Out	+P1-54 -P1-24
UNIT SELECT BUS 2	Unit Select Bit 2 ²	Out	+P1-56 -P1-26
UNIT SELECT BUS 3	Unit Select Bit 2 ³	Out	+P1-57 -P1-27
UNIT SELECT TAG	Unit Select Tag	Out	+P1-52 -P1-22
UREADY	Unit Ready	In	+P1-49 -P1-19
WRITE CLK	Write Clock	Out	P2-P5 + 19 - 6 GND 7
WRITE DATA	Write Data	Out	P2-P5 + 20 - 8 GND 18
WRPROT	Write Protected	In	+P1-58 -P1-28

2.4 USER OPTIONS.

Some features of the AM-410 can be changed by selection of jumpers at the user's option. Location of the jumper pads is shown in Figure 2-2.

2.4.1 ADDRESS CODE.

Circuit board addressing can be selected at the user's option for any address block (in increments of four) on the address lines AD2-AD7. The standard address (D0 Hex) is contained in etch when the circuit board is manufactured. To change the address, cut the desired etch and leave open for pull up or jumper to ground to generate the desired board address.

2.4.2 INTERRUPT LINES.

Interrupt compatibility for any S-100 bus system is provided with jumpers to any of the vectored interrupt lines VI0-VI7. Attach the jumper wire from the pad located as shown in Figure 2-2 to the desired interrupt line. The standard interrupt line is VI2 which is contained in etch. Cut this jumper to change the interrupt.

2.4.3 BOOT OPTION.

The AM-410 contains a bootstrap loader program contained in an internal PROM that the user may utilize. If the user decides to boot from another source, the boot feature must be disabled with a jumper block as shown in Figure 2-2. When using the AM-410 subsystem with the AM-100/T CPU, always disable the boot feature.

2.4.4 AM-100 PREPARATION.

If the Alpha Micro AM-100 CPU is used in the system, the interrupt jumper must be added on the CPU board set at VI2 for compatibility with the AM-410.

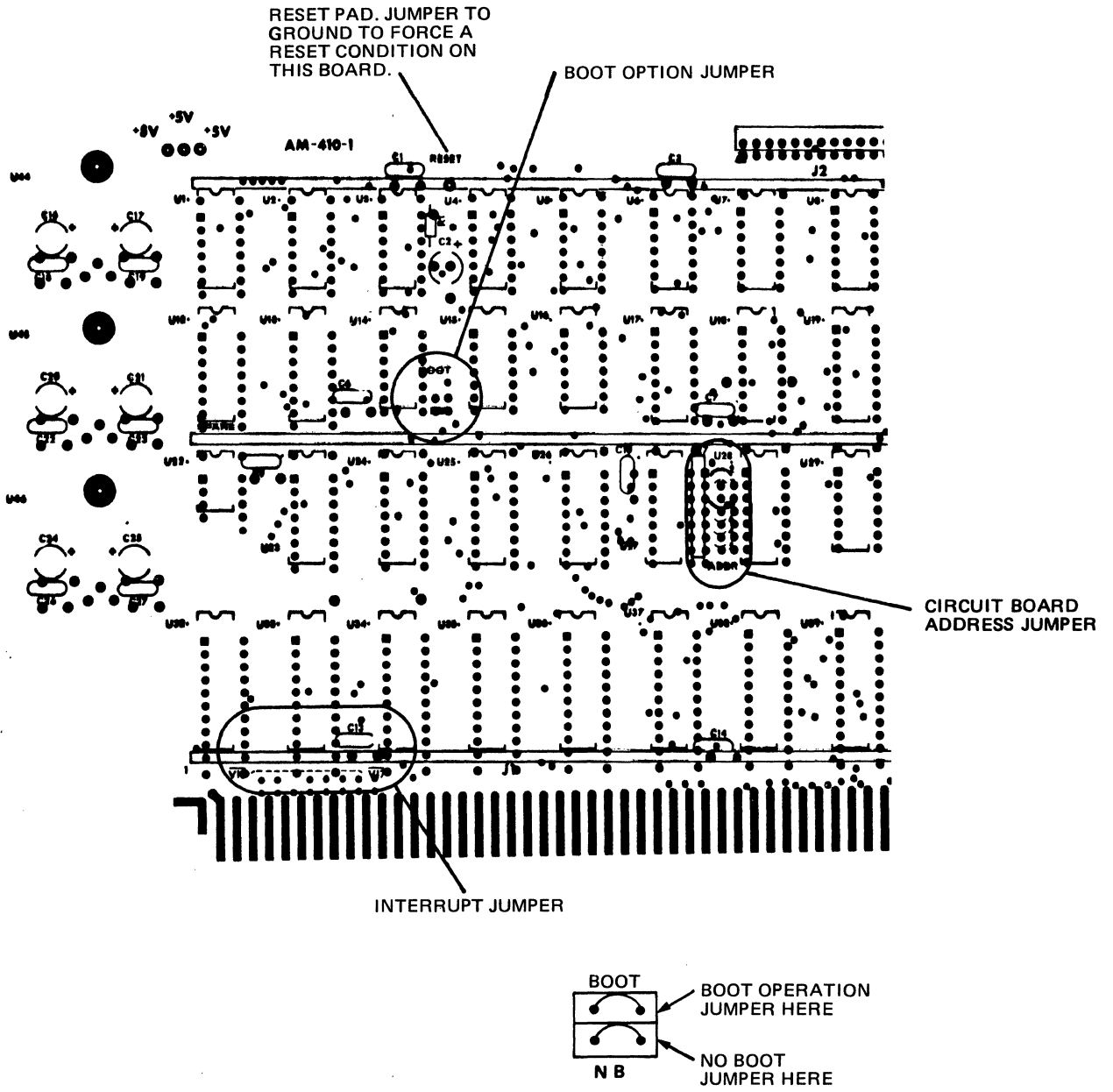


Figure 2-2. Location of Jumpers for User Options

SECTION 3 PROGRAMMING

3.0 INTRODUCTION.

This section describes the programming requirements for the AM-410 circuit board. Circuit board addressing, bootstrap loader, and AM-410 internal programming are described for complete system compatibility.

When the AM-410 circuit board is received, it is ready for use with the CDC 9448 (Phoenix) disk drive as described in Section 2 of this manual. The bootstrap loader and the micro-code contained in internal firmware is designed only for this disk drive.

3.1 UNIQUE SOFTWARE CONSIDERATIONS.

One of the most important differences between the Storage Module family of drives and conventional drives is that the software must accept media flaws. The track and bit densities are so great with these high capacity memory disks that it is impossible to manufacture platters with no media flaws. Therefore, software consideration is made for these faulty blocks.

The technique used to detect and flag these blocks writes to every block and reads from every block and flags the bit map of any blocks that are faulty. To accommodate this technique, a new program called "CRT410" is included and also new versions of old programs.

NOTE

Because of media flaws that are inherent to the Storage Module family, it is not possible to copy physical records to physical records.

3.2 ADDRESSING.

The AM-410 and associated disk drives are addressed through the S-100 bus address lines. The circuit board address is jumper selectable by the jumpers connected to U27. Pull-ups to either +5V or ground jumpers select the board address on S-100 bus address lines AD2-AD7. Address D0 (Hex) is etched in the board to occupy I/O ports D0 and D1 (Hex).

3.3 INITIALIZATION.

On initial power-up or reset, the AM-410 goes into a dormant state waiting for initialization. With the boot option enabled, the phantom signal is activated, disabling any phantom controlled memory. The S-100 bus is enabled to access the bootstrap loader contained in the AM-410 PROM.

The 2K x 8 PROM (U31) contains both the bootstrap routine and the controller microcode. The microcode resides in the first 1K bytes, and the bootstrap routine resides in the second 1K bytes of this PROM. The current bootstrap routine is written in AM-100 code. However, other user codes may be used.

NOTE

If the user code contained in the AM-410 PROM is changed from the current boot routine, the microcode in the first 1K of memory must be duplicated exactly.

Initialization of the AM-410 is accomplished by writing a zero byte into the AM-410 command register during system initialization. The on board CPU finishes initialization of the disk controller and releases the Phantom signal.

3.4 COMMAND REGISTER.

The command register receives AM-410 commands from the S-100 bus. It is accessed by writing to the selected address.

The legal base addresses are in multiples of four from the first address FF00 (Hex) to FFFC (Hex) in increments of four. A software handshake sequence must be used for the command transfer (see paragraph 3.7). FFDO (Hex) is the base address when it is shipped from the factory.

There are two basic types of commands used for operation of the AM-410 system; non-disk commands and disk commands. Both types are described in Figure 3-1.

3.5 STATUS REGISTER.

The status register is used to determine the current status of the AM-410 controller. It is accessed from the S-100 bus by reading from the user selected base address of the circuit board FFDO (Hex). The format of the status register is described in Figure 3-2.

3.6 INTERRUPT MODE.

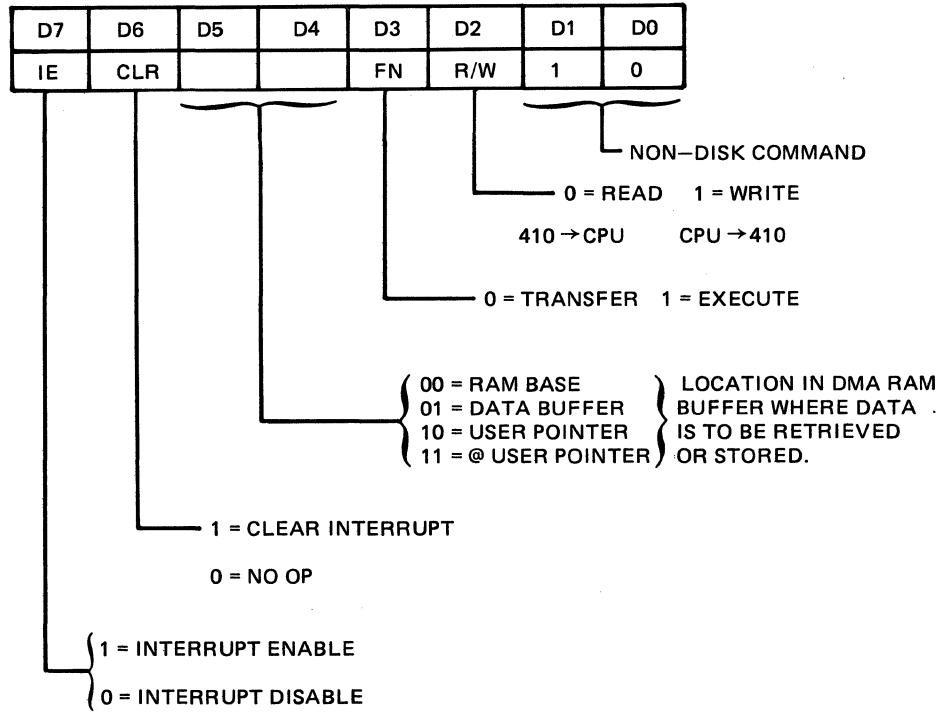
The interrupt mode in the AM-410 can be selected by both disk and non-disk commands. If the interrupt mode is selected, the interrupt occurs at the completion of the current AM-410 command. The interrupt must be cleared by the user by setting bit 6=1 of any non-disk command.

3.7 HANDSHAKE SEQUENCE.

A handshaking type interaction is required between the AM-410 circuit board and the CPU any time a command is sent to the AM-410. This handshaking is a software operation that uses bit 7 of the Status Register. Handshake operations proceed in the following sequence:

1. A command is sent from the S-100 bus to the Command Register.
2. The system software waits for bit 7 of the Status Register to become a 1 to guarantee that the AM-410 has received the command.

NON-DISK COMMANDS:



DISK COMMANDS:

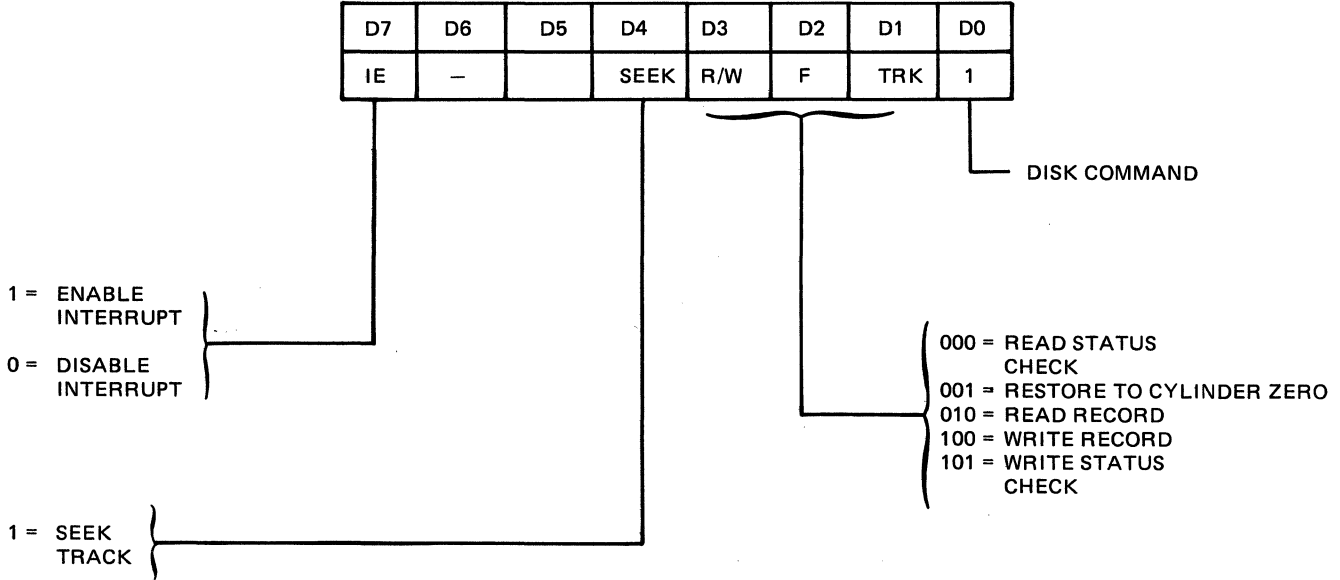
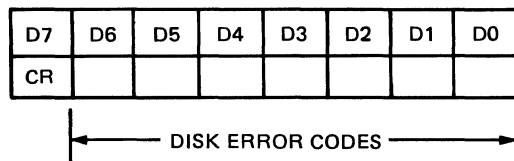


Figure 3-1. AM-410 Commands

STATUS REGISTER BITS



- 05 (HEX) = DISK NOT READY
- 0B (HEX) = DISK WRITE PROTECTED
- 0F (HEX) = DISK FAULT (THE CODE FOR THE FAULT IS LOCATED IN THE DATA REGISTER (BASE ADDRESS +1)).

DATA REGISTER BITS FOR DISK FAULTS ONLY

D7	D6	D5	D4	D3	D2	D1	D0
DN	CR	WP	AM	UR	OC	SE	FL

- DN = DONE. INDICATES THE STATUS OF THE DMA TRANSFER (ALWAYS CLEARED).
- CR = CRC ERROR. INDICATES A CRC ERROR HAS OCCURRED.
- WP = WRITE PROTECT. INDICATES THAT THE DISK IS PROTECTED (ALWAYS CLEARED).
- AM = ADDRESS MARK. NOT USED (ALWAYS CLEARED).
- UR = UNIT READY (ALWAYS CLEARED).
- OL = ON CYLINDER. INDICATES THAT THE DRIVE DID NOT ARRIVE ON CYLINDER IN TIME
- SE = SEEK ERROR. INDICATES THAT AN INVALID CYLINDER NUMBER WAS ISSUED TO THE DRIVE.
- FL = FAULT. A DRIVE FAULT HAS OCCURRED (SEE DRIVE MANUAL).

Figure 3-2. AM-410 Status Words

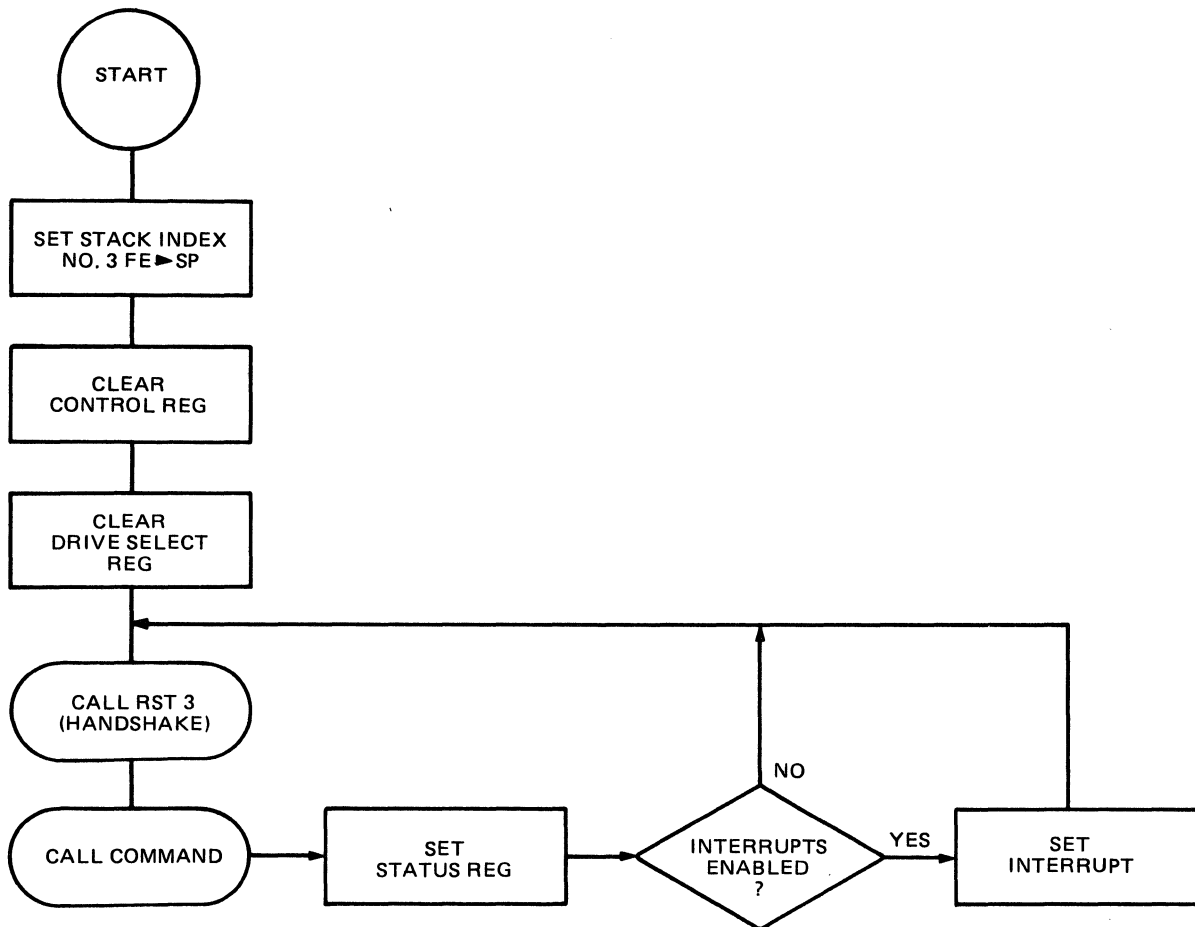


Figure 3-3. DMA Buffer Operation

3. The system software writes a zero into the Command Register to clear the previous command.
4. The system software waits until bit 7 of the Status Register becomes a 0 indicating that the Command Register has been cleared and the command has been executed.

This completes the handshake operation and the program continues.

3.8 DMA BUFFER.

The DMA buffer is the 1K RAM in the AM-410. All data transfers to or from the disk memory must pass through this buffer and are handled by the DMA logic.

The DMA buffer is accessed by addressing the AM-410 base address plus one and all data between the AM-410 and the S-100 bus must pass through this single port. No DMA type operations occur between the AM-410 and system memory because they are handled on a programmed basis only. The microcode initializes the buffer and sets the DMA channels for proper operation as shown in Figure 3-3. The Handshake sequence is shown in Figure 3-4, and the data transfer sequence is shown in Figure 3-5.

The starting location within the buffer is determined by bits 4 and 5 of non-disk commands. The RAM base address (D5=0, D4=0) points to the first location in the DMA buffer. The first eight locations of this buffer are used to store information regarding retry count, drive select, and track/sector/head select.

The data buffer address (D5=0, D4=1) points to the start of 512 data bytes within the buffer and begins at the ninth byte. The user pointer address (D5=1, D4=0) points to a location within the DMA buffer which may be loaded by the user to point to other buffer memory locations for data transfer or the start of user defined microcode. The actual location is the last two bytes of the 1K RAM used for the DMA buffer. The user

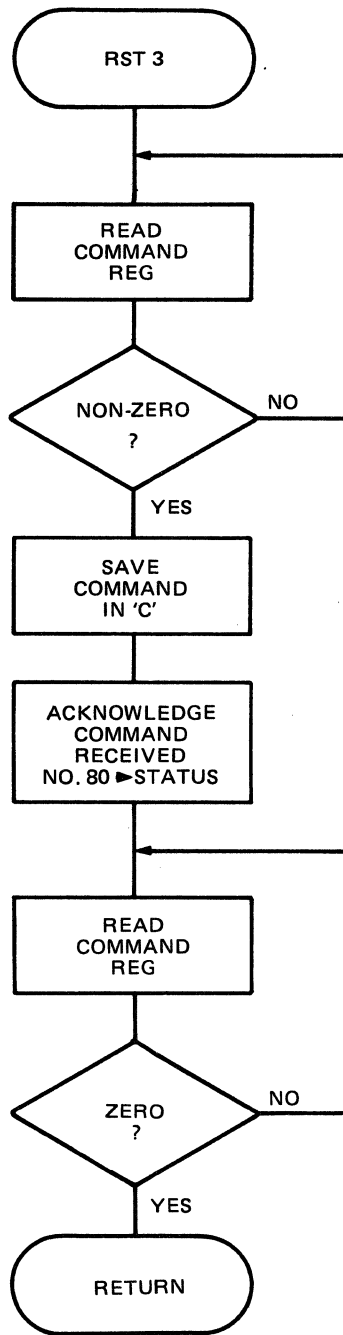


Figure 3-4. Handshake Sequence

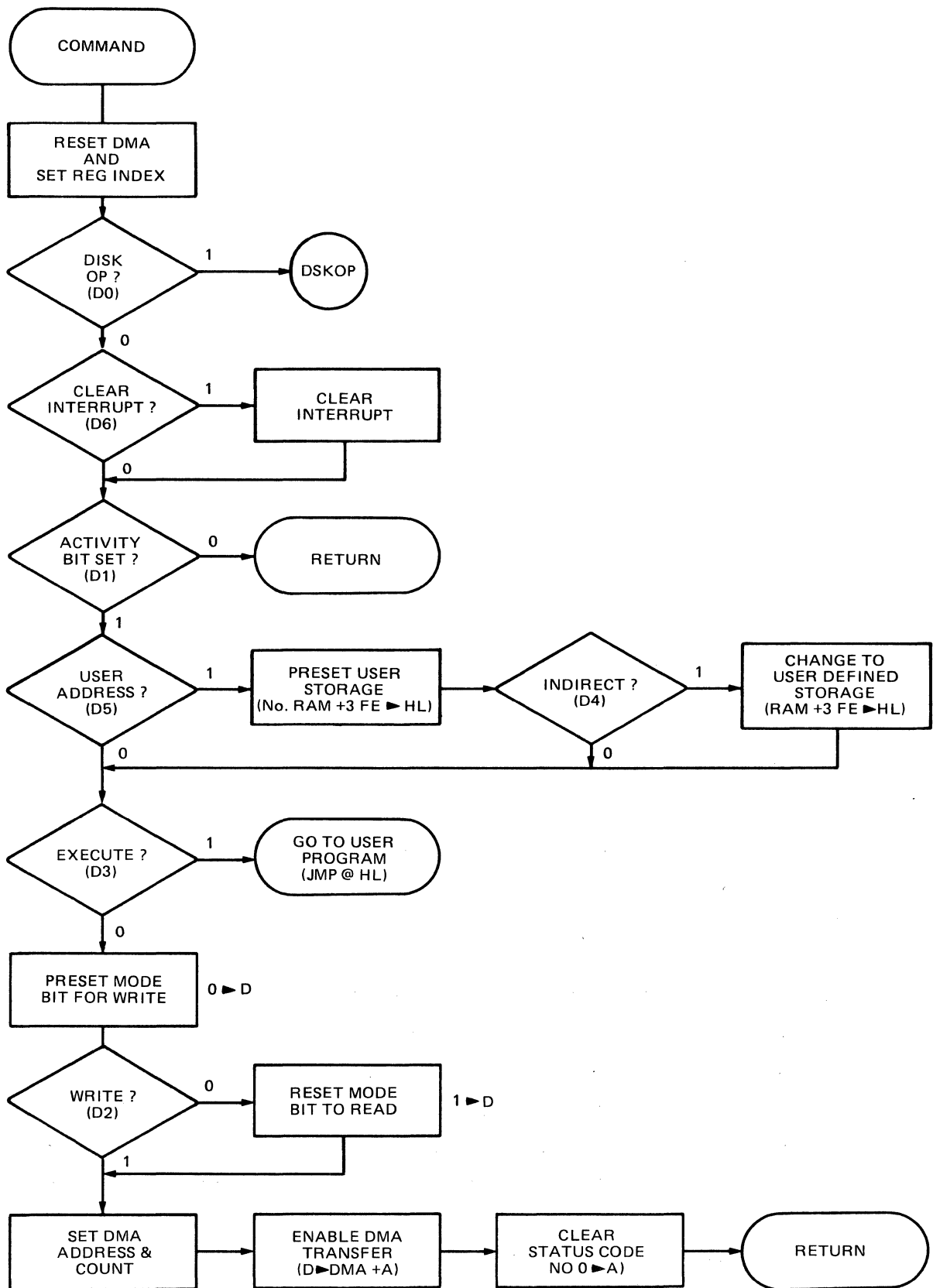


Figure 3-5. DMA Transfer Sequence

pointer (D5=1, D4=1) is used to make indirect data transfers or jumps to microcode using the user pointer.

3.8.1 DMA BUFFER OPERATION FOR DISK WRITE.

Transferring data to the DMA buffer and then performing disk write operations takes place as follows:

1. Send DMA write command 06 (Hex) to the AM-410 command register and perform a handshake.
2. Send retry count to AM-410 DMA buffer (normally 8).
3. Send disk unit Number (0-3) to DMA buffer.
4. Write physical address plus two bytes of zeros (6 bytes total), sector, head, cylinder (2 bytes).
5. Send data (0-512 bytes) to DMA buffer.
6. Send disk write command 19 (Hex), or 99 (Hex) for interrupt, to AM-410 command register and perform a handshake.
7. Read AM-410 status register and check for zero condition indicating no error.
8. Continue with next command if no errors are detected.

3.8.2 DMA BUFFER OPERATION FOR DISK READ.

Transferring data from the disk into the DMA buffer and then reading the DMA buffer is performed as follows:

1. Send a DMA write command 06 (Hex) to the AM-410 command register and perform a handshake.
2. Write retry count into the DMA buffer.
3. Write disk unit number (0-3) into the DMA buffer.
4. Write physical address plus two bytes of zeros (six bytes total), sector, head, cylinder (2 bytes).
5. Write disk read command 15 (Hex), or 95 (Hex) for interrupt, to the AM-410 command register and perform a handshake.
6. Read AM-410 status register and check for zero

- condition indicating that no errors have occurred.
7. Assuming that no errors occurred during the disk read, send the DMA read command 12 (Hex), or 92 (Hex) for interrupts to the AM-410 command register and perform the normal handshake.
 8. Read one byte of data from the DMA buffer and discard it (the first byte is always invalid data).
 9. Read the valid data (1 to 512 bytes) from the DMA buffer.

3.8.3 PHYSICAL ADDRESS.

The term physical address refers to a four byte block pointing to the cylinder/sector/head within the drive. The user enters these four bytes in the following order:

1. Sector (1 byte)
2. Head (1 byte)
3. Cylinder (2 bytes)

A valid sector number is between zero and the maximum number of sectors around a disk track. A valid head number is between zero and the maximum number of heads in the drive. A valid cylinder number is a two byte number between zero and the maximum number of cylinders within a drive. The valid numbers for the CDC Phoenix drive are:

1. Sectors 0-35
2. Heads 0-5
3. Cylinders 0-807

3.9 RESTORE COMMAND.

The restore command is used to reset the disk logic and force the disk head to return to track zero. The user may force a restore command with a disk command 3 (Hex), or the microcode will exercise the restore command on its own following certain errors.

If a disk fault occurs, the microcode attempts one restore and then checks the fault status again. If the fault still exists, the microcode aborts the command operation and reports an error to the CPU.

3.10 STATUS CHECK.

The Read and Write Status check commands are used to access specific status information from the disk drive.

The Write Status check command is used to determine if the currently addressed disk is write protected. It does not attempt to actually write any data. If the addressed disk is write protected, error code 0B (Hex) is placed in the status register.

The Read Status check command (if SEEK bit 4 is on) seeks for the currently addressed track and then returns. Data is not read from the disk. If an error occurred, an error code is placed in the status register.

SECTION 4

FUNCTIONAL THEORY OF OPERATION

4.0 INTRODUCTION.

The AM-410 Disk Controller circuit board set contains integrated circuit elements for the data processing necessary for the performance of the functions described in Sections 1, 2 and 3 of this manual. This section describes the functional theory of operation of the circuit board set and also provides information for each of the integrated circuit elements.

4.1 CIRCUIT BOARD OPERATION.

This circuit board set (two circuit board assemblies) provides control and interface capability between the S-100 bus and the CDC 9448 (Phoenix) hard disk drive. The functional block diagrams of the circuit boards are shown in Figures 4-1 and 4-2. The circuit board schematics, parts lists, and component cross-reference lists are contained in Section 6 of this manual. Table 4-1 contains a list of the signals used in these circuit boards with descriptions of their functions. For S-100 Bus interface signals, see Table 4-2. For disk drive interface signals, see Table 4-3.

The two-board set consists of the AM-410-1 and AM-410-2 circuit board assemblies connected together at the top edge with a ribbon cable as described in Section 2. The AM-410-1 board primarily contains the CPU microprocessor and the DMA Address Generator module with registers and control logic for the S-100 bus interface. The AM-410-2 board primarily contains control logic for disk operation with receivers and drivers for disk drive interface. Referencing between Figures 4-1 and 4-2 uses the notation for AM-410-1 and AM-410-2 inputs and outputs which refers to connections between Figures 4-1 and 4-2.

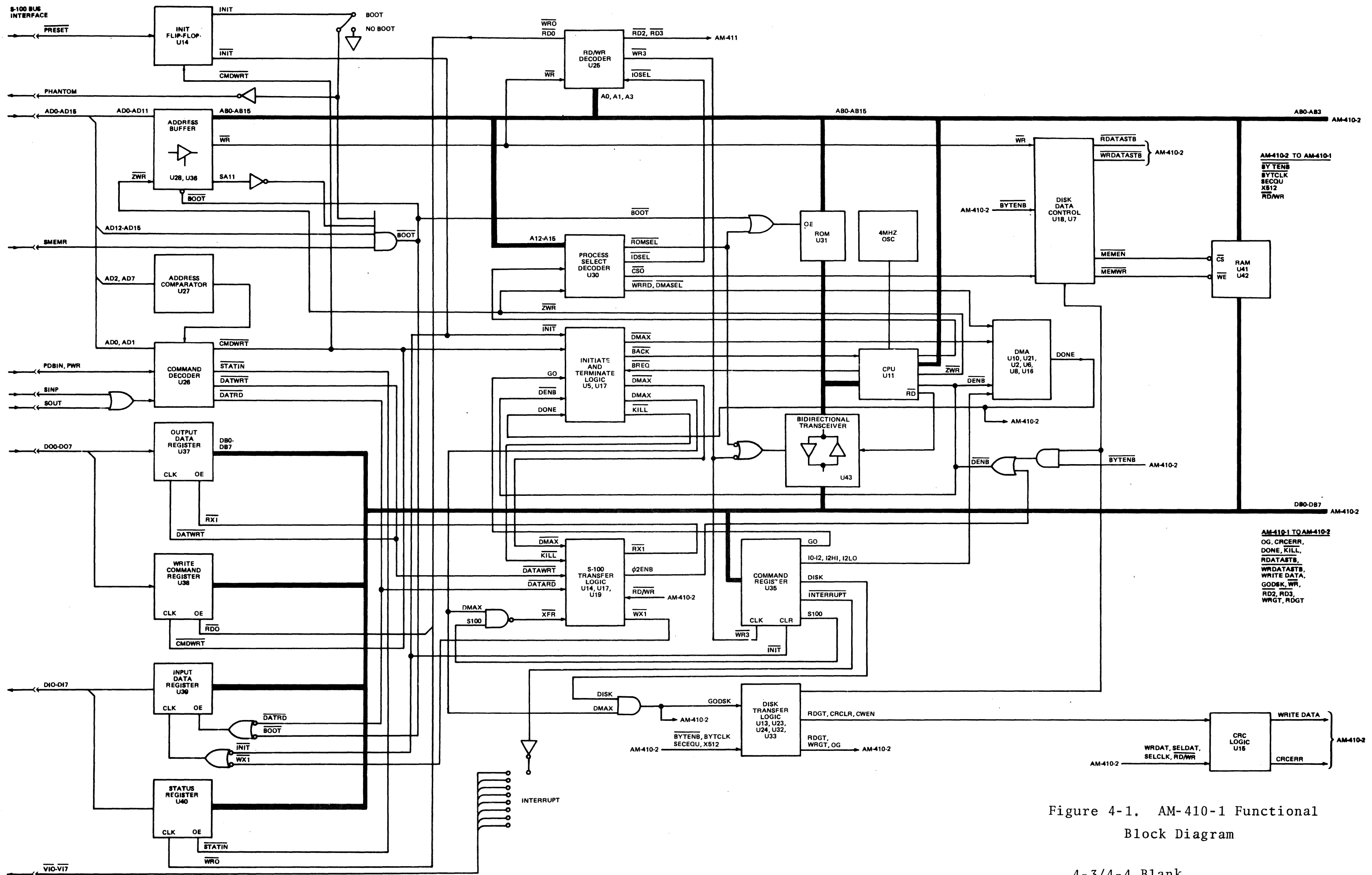


Figure 4-1. AM-410-1 Functional Block Diagram

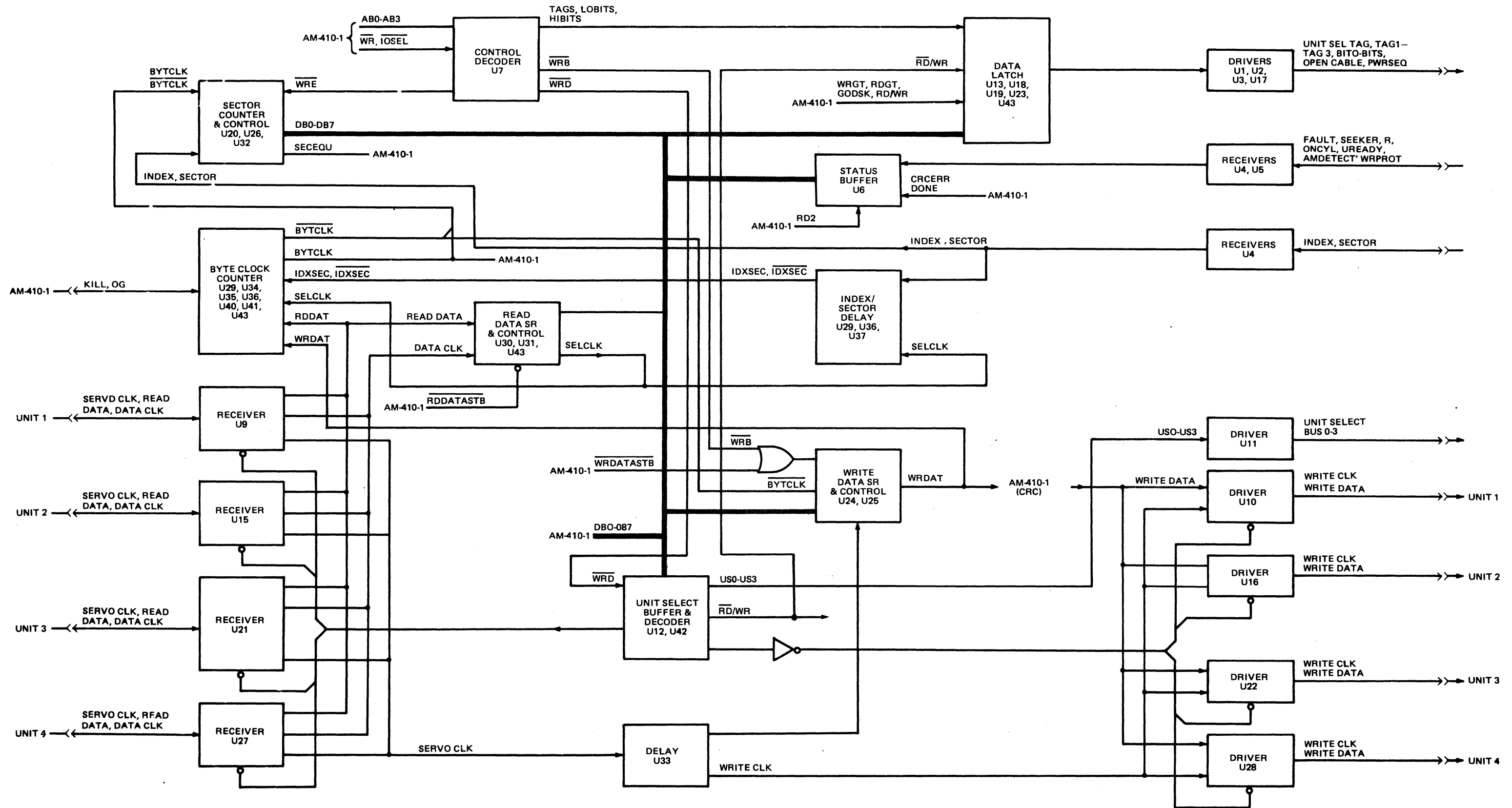


Figure 4-2. AM-410-2 Functional Block Diagram

Table 4-1. AM-410 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
AB0-AB15	Address Bus	AM-410-1 SH1	16 Bit Tri-state address bus. Provides addressing for memory, data exchanges and I/O device exchanges.
$\overline{\text{BACK}}$	Bus Acknowledge	AM-410-1 SH1	CPU module output indicating that the CPU module address bus, data bus, and tri-state control bus signals have been set to their high impedance state.
$\overline{\text{BOOT}}$	Bootstrap Load	AM-410-1 SH1	Generated when the bootstrap program has been selected. Enables the ROM, Address Buffer, and Input Data Register.
$\overline{\text{BREQ}}$	Bus Request	AM-410-1 SH1	CPU module input requesting that the CPU module set its address bus, data bus, and tri-state control bus to the high impedance state.
$\overline{\text{BYTCLK}}$ $\overline{\text{BYTCLK}}$	Byte Clock	AM-410-2 SH1	Generated by the Byte Clock Counter at the end of each byte of data written or read. Used to control the Shift/Load of the write data shift register and the disk transfer logic.
$\overline{\text{BYTENB}}$	Byte Enable	AM-410-2 SH1	Byte clock counter output at the same frequency as $\overline{\text{BYTCLK}}$ but twice the duration. Used by the disk transfer logic and disk data control logic.
$\overline{\text{CMDWRT}}$	Command Write	AM-410-1 SH1	Output of the Command Decoder to clock command data into the Write Command Register and set up the initiate logic.
CRCERR	CRC Error	AM-410-1 SH2	Output of the CRC checking module indicating an error in the data.
CRCLR	CRC Clear	AM-410-1 SH2	Master reset input to the CRC checking module.
$\overline{\text{CSO}}$	Chip Select	AM-410-1 SH1	Output of the process select decoder and is one of the signals that enables the RAM.
CWEN	Check Word Enable	AM-410-1 SH2	Generates the enable signal to the CRC checker allowing the check word to be generated and written onto the disk.
DATA CLK	Data Clock (Read Clock)	AM-410-2 SH1	This clock defines the beginning of the data cell. It is derived internally to the disk drive and is synchronous with the detected data.

Table 4-1 (Cont.). AM-410 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{DATRD}}$	Data Read	AM-410-1 SH1	Command Decoder output to enable the Input Data Register and to generate S-100 transfer signals.
$\overline{\text{DATWRT}}$	Data Write	AM-410-1 SH1	Command Decoder output to enable the Output Data Register and to generate S-100 transfer signals.
DENB	DMA Enable	AM-410-1 SH2	Provides clock input to the DMA Address Generator modules. DMA enable begins each cycle of the DMA.
$\overline{\text{DMASEL}}$	DMA Select	AM-410-1 SH1	Output of the process select decoder to enable the selected DMA address generator. Used to write data into or read data from the DMA address generator.
$\overline{\text{DMA}}\text{X}$ $\overline{\text{DMA}}\text{X}$	DMA Access Grant	AM-410-1 SH2	Indicates that the on-board CPU is off the busses and that control of those busses may now pass to the DMA logic.
DISK	Disk Command	AM-410-1 SH2	Output of the Command Register to set up a disk operation with DMA Access Grant signal.
DONE	Process Command	AM-410-1 SH2	Output of the DMA Address Generator indicating completion of the current operation.
D0-D7	Data Bus Bits 0-7	AM-410-1 SH1	Internal eight-bit tri-state data bus.
GO	GO	AM-410-1 SH2	Start command output from Command Register. Initiates the transfer of bus control from the on-board CPU to the DMA logic.
GODSK	Go Disk	AM-410-1 SH2	Initiates disk operations under DMA logic control.
$\overline{\text{IDXSEC}}$ $\overline{\text{IDXSEC}}$	Sector Reset	AM-410-2 SH2	Reset command to byte clock counter to reset count to beginning of each sector.

Table 4-1 (Cont.). AM-410 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
INDEX	Disk Index	AM-410-2 SH2	Index pulse from disk drive. Occurs once per revolution of the disk to define the beginning of sector zero.
$\overline{\text{INIT}}$	Initialize	AM-410-1 SH1	Internal reset signal generated from S-100 Bus $\overline{\text{PRESET}}$ signal.
$\overline{\text{IOSEL}}$	I/O Select	AM-410-1 SH1	Generated from either Read or Write output from the CPU microprocessor when address lines A14 and A15 from the internal address bus are both one.
I0, I1	Instruction Codes	AM-410-1 SH2	Instruction code inputs to the DMA Address Generator from the Command Register.
I2LO, I2HI	Instruction Codes	AM-410-1 SH2	Instruction code to either the upper eight bits or lower eight bits of the DMA Address generator from the command register.
$\overline{\text{JAM6}}$	Preset Six	AM-410-2 SH3	Presets byte clock counter to a count of six to synchronize the read timing.
$\overline{\text{KILL}}$	Terminate	AM-410-1 SH2	Terminates the operation in process.
$\overline{\text{MEMEN}}$	Memory Enable	AM-410-1 SH2	Enables the RAM for read or write operations.
$\overline{\text{MEMWR}}$	Memory Write	AM-410-1 SH2	Controls read or write operations of the RAM. Low = write, High = read.
OG	Output Gate	AM-410-1 SH2	Allows transfer of data into or out of the disk drive.
RDDAT	Read Data	AM-410-2 SH1	The data recovered from the disk in NRZ form.
$\overline{\text{RDDATA STB}}$	Read Data Strobe	AM-410-1 SH2	Generated by the Disk Data Control logic to transfer a byte of read data from the buffer register to the data bus DB0-DB7.
RDGATE	Read Transfer Gate	AM-410-2 SH2	Instructs the disk drive to gate the read data onto the interface. It occurs for any disk transfer cycle (read or write).

Table 4-1 (Cont.). AM-410 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
RDGT	Read Gate	AM-410-1 SH2	Same as RDGATE but only during a read disk transfer (gated by \overline{RD}/WR).
\overline{RD}/WR	Read/Write	AM-410-2 SH1	Generated from bit 4 of command word to set either disk Read or Write processing.
$\overline{RD0}-\overline{RD3}$	Read 0 - Read 3	AM-410-1 SH1	Read select outputs from the Read/Write decoder to enable read operations.
\overline{ROMSEL}	ROM Select	AM-410-1 SH1	Generates the output enable of the ROM.
$\overline{RX1}$	Output Data Transfer	AM-410-1 SH2	Output from the S-100 Bus Transfer logic to transfer data from the Output Data Register to the Internal data bus DB0-DB7 (logical OR of RD1 and the read pulse from the DMA logic).
SA11	S-100 Address Bit 11	AM-410-1 SH1	Buffered S-100 address bit 11.
\overline{SDREQ} \overline{SDREQ}	S-100 Data Request	AM-410-1 SH2	Generated from \overline{DATWRT} or \overline{DATRD} for S-100 Bus data transfers.
SECEQU	Sector Equal	AM-410-2 SH3	Pulse output of the Sector Counter and Control logic when the sector counter is equal to the sector latch indicating that the requested sector is under the read/write head.
SECTOR	Sector Pulse	AM-410-2 SH2	Sector pulse that occurs at the beginning of each disk sector except sector zero which is marked by the INDEX pulse.
SEEKEND	Seek Operation End	AM-410-2 SH1	Not used.
SELCLK	Selected Clock	AM-410-2 SH1	Either servo clock or data clock depending on state of read/write command.
SELDAT	Selected Data	AM-410-2 SH1	Either read data or write data depending on state of read/write command.

Table 4-1 (Cont.). AM-410 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
SERVO CLK	Servo Clock	AM-410-2 SH1	Input from disk drive. Phase-locked 9.677 MHz clock generated from the servo track dibits. Used for synchronization during write disk operations.
$\overline{\text{STATIN}}$	Status In	AM-410-1 SH1	Output of the command decoder to enable the Status Register.
S100	S-100 Select	AM-410-1 SH2	Command Register output to enable an S-100 bus data transfer.
US0-US3	Unit Select 0-3	AM-410-2 SH1	Binary coded select lines to select disk drives 0-3.
$\overline{\text{WR}}$	Write	AM-410-1 SH1	Generated from on-board CPU Write (ZWR) signal.
WRDAT	Write Data	AM-410-2 SH1	Serial write data from the shift register into the CRC generator.
$\overline{\text{WRDATA STB}}$	Write Data Strobe	AM-410-1 SH2	Generated by the Disk Data Control logic to clock the write data from the data bus DB0-DB7 into the write buffer register.
WRGATE	Write Trans- fer Gate	AM-410-2 SH2	Instructs the drive to write data onto the selected surface. It occurs for both read and write disk transfer cycles.
WRGT	Write Gate	AM-410-1 SH2	Same as WRGATE but only during a write disk transfer (gated by $\overline{\text{RD}}/\overline{\text{WR}}$).
WRITE DATA	Disk Write Data	AM-410-1 SH2	Disk write data from the CRC checker logic applied to the write data drivers.
$\overline{\text{WRRD}}$	Write-Read	AM-410-1 SH1	Read pulse or write pulse from the on board CPU.
WR0-WR3 WR8-WRF	Write0-Write3 Write8-WriteF	AM-410-1 SH1	Write select outputs from the Read/Write decoder that enable write operations to selected latches.
$\overline{\text{WX1}}$	Write 1	AM-410-1 SH2	The logical OR of WR1 and the write pulse from the DMA logic.

Table 4-1 (Cont.). AM-410 Signals List

SIGNAL	NAME	SCHEM PAGE OF SOURCE	DESCRIPTION
$\overline{\text{XFER}}$	Transfer	AM-410-1 SH2	Generated from DMAX AND S-100 to strobe the S-100 Transfer Logic to transfer data from the Input and Output Data Registers to the internal data bus.
X512	Times 512	AM-410-2 SH1	Used by the DMA logic to indicate when all data has been written or read and that CRC data is next.
$\overline{\text{ZWR}}$	CPU Write	AM-410-1 SH1	Indicates that the CPU Module holds valid data to be stored in the addressed memory.
4 MHZ	4 MHz Clock	AM-410-1 SH1	4 MHz clock from oscillator U9.
\emptyset 2ENB	S-100 Transfer	AM-410-1 SH2	Clock signal for every cycle of the S-100 data transfer.

Table 4-2. S-100 Bus Interface Signal Descriptions

MNEMONIC	NAME	PIN	DESCRIPTION
A0	Address 0	79	16 Bits of S-100 Addressing.
A1	Address 1	80	
A2	Address 2	81	
A3	Address 3	31	
A4	Address 4	30	
A5	Address 5	29	
A6	Address 6	82	
A7	Address 7	83	
A8	Address 8	84	
A9	Address 9	34	
A10	Address 10	37	
A11	Address 11	87	
A12	Address 12	33	
A13	Address 13	85	
A14	Address 14	86	
A15	Address 15	32	
DATAIN 0	Input Data Bit 0	95	Data Input Port. Bus Master Input from Slaves.
DATAIN 1	Input Data Bit 1	94	
DATAIN 2	Input Data Bit 2	41	
DATAIN 3	Input Data Bit 3	42	
DATAIN 4	Input Data Bit 4	91	
DATAIN 5	Input Data Bit 5	92	
DATAIN 6	Input Data Bit 6	93	
DATAIN 7	Input Data Bit 7	43	
DATAOUT 0	Output Data Bit 0	36	Data Output Port. Bus Master Output to Slaves.
DATAOUT 1	Output Data Bit 1	35	
DATAOUT 2	Output Data Bit 2	88	
DATAOUT 3	Output Data Bit 3	89	
DATAOUT 4	Output Data Bit 4	38	
DATAOUT 5	Output Data Bit 5	39	
DATAOUT 6	Output Data Bit 6	40	
DATAOUT 7	Output Data Bit 7	90	

Table 4-2 (Cont.). S-100 Bus Interface Signal Descriptions

MNEMONIC	NAME	PIN	DESCRIPTION
PDBIN	Data Bus In	78	Read enable. Used by bus master to request addressed slave to place data on input port.
$\overline{\text{PHANTOM}}$	Phantom	67	Disables phantom controlled memories when asserted.
PWR	Write Strobe	77	Write strobe generated by bus masters as write command to slaves.
$\overline{\text{PRESET}}$	Reset	75	AM-410 reset input from bus.
SINP	I/O Input Cycle	46	AM-410 I/O signal indicating I/O input operation.
SMEMR	Memory Cycle Input Status Line	47	Current bus cycle is a bus master input from a memory address.
SOUT	I/O Output Cycle	45	AM-410 I/O signal indicating I/O output operation.
$\overline{\text{VI0}}$	Interrupt 0	4	Jumper selected interrupts. Used for both interrupt requests and DMA requests. Normal configuration: VI6 used for DMA request.
$\overline{\text{VI1}}$	Interrupt 1	5	
$\overline{\text{VI2}}$	Interrupt 2	6	
$\overline{\text{VI3}}$	Interrupt 3	7	
$\overline{\text{VI4}}$	Interrupt 4	8	
$\overline{\text{VI5}}$	Interrupt 5	9	
$\overline{\text{VI6}}$	Interrupt 6	10	
$\overline{\text{VI7}}$	Interrupt 7	11	

Table 4-2 (Cont.). S-100 Bus Interface Signal Descriptions

MNEMONIC	NAME	PIN	DESCRIPTION
+8VDC	+8VDC	1, 51	+8V power.
GND	Ground	50, 100	System Ground.
-16VDC	-16VDC	52	-16V power.

Table 4-3. Disk Drive Interface Signal Descriptions

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN	DESCRIPTION
AMDETECT	Address Mark Found	Out	+P1-50 -P1-20	Pulse sent following recognition of at least 16 missing transitions and the first zero of the zeros pattern.
Bit 0	Tag Bus Bit 0	Out	+P1-34 -P1-4	Cylinder head address command and control lines. See Table 4-4 for tag bus decode information.
Bit 1	Tag Bus Bit 1	Out	+P1-35 -P1-5	
Bit 2	Tag Bus Bit 2	Out	+P1-36 -P1-6	
Bit 3	Tag Bus Bit 3	Out	+P1-37 -P1-7	
Bit 4	Tag Bus Bit 4	Out	+P1-38 -P1-8	
Bit 5	Tag Bus Bit 5	Out	+P1-39 -P1-9	

Table 4-3 (Cont.). Disk Drive Interface Signal Descriptions

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN	DESCRIPTION
Bit 6	Tag Bus Bit 6	Out	+P1-40 -P1-10	
Bit 7	Tag Bus Bit 7	Out	+P1-41 -P1-11	
Bit 8	Tag Bus Bit 8	Out	+P1-42 -P1-12	
Bit 9	Tag Bus Bit 9	Out	+P1-43 -P1-13	
DATA CLK	Read Clock	In	P2-P5 + 17 - 5 GND 4	This clock defines the beginning of the data cell. It is derived internally to the disk drive and is synchronous with the detected data.
FAULT	Fault	In	+P1-45 -P1-15	This line when active indicates that a fault condition exists within the disk drive. See Disk Drive manual for further information.

Table 4-3 (Cont.). Disk Drive Interface Signal Descriptions

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN	DESCRIPTION
INDEX	Disk Index	In	+P1-48 -P1-18	Pulse which occurs once per disk revolution; its leading edge being considered the leading edge of the Sector Zero. Pulse width is typically 2.5 μ s. Index to controller is gated off during volume change and RTZ.
ONCYL	On Cylinder	In	+P1-47 -P1-17	This status signal indicates that the servo system has positioned the heads of the selected volume over a track. The status is cleared with any seek instruction causing the carriage to move or a zero distance seek. A carriage offset will result in loss of On Cylinder for a period of 2.75 ms (nominal).
OPEN CABLE DETECTOR	Open Cable Detector	Out	+P1-44 -P1-14	This line allows information to be received over the interface. This signal must be true in order for selection and control to take place.

Table 4-3 (Cont.). Disk Drive Interface Signal Descriptions

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN	DESCRIPTION
POWER SEQ HOLD	Power Sequence Hold	Out	P1-59	Power sequencing levels. Ground on these two will cause the first drive in sequence to begin its spindle start sequence. Once the first is up to speed, the PICK signal is transferred to the next active drive which starts up and sends the PICK signal on, and so forth until all the drive units are up to speed. Individual units may be started and stopped manually once the start sequencing is completed. All units power down the spindles when ground on SEQUENCE HOLD is removed.
POWER SEQ PICK	Power Sequence Pick	Out	P1-29	
READ DATA	Read Data	In	P2-P5 + 16 - 3 GND 15	This line transmits the recovered data from the disk in NRZ form.
SECTOR	Sector Pulse	In	+P1-55 -P1-25	Pulse derived from the servo track which divides each track into sectors. Up to 127 sector pulses are available per cylinder depending on the setting of sector switches in the drive. Sector to controller is gated off during volume change and RTZ.

Table 4-3 (Cont.). Disk Drive Interface Signal Descriptions

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN	DESCRIPTION
SEEK END	Seek Opera- tion End	In	P2-P5 + 23 - 10 GND 21	This line combines the ON CYLINDER or SEEK ERROR signals indicating that a seek operation has terminated. This is redundant and not used by the AM-410.
SEEKERR	Seek Error	In	+P1-46 -P1-16	When this line is active, a Seek Error has occurred. The error may only be cleared by performing an RTZ. Seek Error means that the carriage was unable to complete a move within the specified time or that it moved to a position outside the recording field or received an illegal track address.
SERVO CLK	Servo Clk	In	P2-P5 + 14 - 2 GND 1	Phase-locked 9.677 MHz clock generated from the servo track dibits.
TAG 1 (CYL)	Tag 1 (Cylinder Address)	Out	+P1-31 -P1-1	This line when active indicates to the device that the information on the ten bus lines (Bits 0-9) represents a binary coded cylinder address number. See Table 4-4.

Table 4-3 (Cont.). Disk Drive Interface Signal Descriptions

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN	DESCRIPTION
TAG 2 (HEAD)	Tag 2 (Head/ Vol. Select)	Out	+P1-32 -P1-2	This line when active indicates that Head/ Volume select information is coded on bus lines BIT 0-2 (head) and Bit 4 (volume). TAG 2 must precede TAG 1 when a volume change is made. See Table 4-4.
TAG 3 (CMD)	Tag 3 (Con- trol Select)	Out	+P1-33 -P1-3	This line when active indicates to the device that the ten Bus lines contain control sig- nals. Table 4-4 lists these control signals.
Unit Select Bus 0	Unit Select Bit 2 ⁰	Out	+P1-53 -P1-23	These lines are binary coded to select the logical number of 1 of 16 devices. The lines are compared with the unit number (0-15) coded on three lines coming from a logic plug on the disk drive.
Unit Select Bus 1	Unit Select Bit 2 ¹	Out	+P1-54 -P1-24	
Unit Select Bus 2	Unit Select Bit 2 ²	Out	+P1-56 -P1-26	
Unit Select Bus 3	Unit Select Bit 2 ³	Out	+P1-57 -P1-27	

Table 4-3 (Cont.). Disk Drive Interface Signal Descriptions

SIGNAL	NAME	AM-410-2 INPUT/ OUTPUT	PIN	DESCRIPTION
UNIT SELECT TAG	Unit Select Tag	Out	+P1-52 -P1-22	This signal gates the desired logic number (coded on the UNIT SELECT 2 ^X lines) into the logic number compare circuit.
UREADY	Unit Ready	In	+P1-49 -P1-19	When active and the device is selected, this line indicates that the device is up to speed, the heads are positioned over the recording tracks and no fault condition exists within the device.
WRITE CLK	Write Clock	Out	P2-P5 + 19 - 6 GND 7	Clock signal that synchronizes the NRZ write data signal in the disk drive.
WRITE DATA	Write Data	Out	P2-P5 + 20 - 8 GND 18	Data that is to be recorded on the disk pack.
WRPROT	Write Protected	In	+P1-58 -P1-28	When active, this line indicates that the write protect function in the drive is active. The Write Protected Indicator on the operator panel will also be illuminated when write protect function is active.

Table 4-4. TAG Bus Decode

	TAG 1	TAG 2	TAG 3
BUS	CYLINDER ADDRESS	HEAD/VOLUME SELECT	CONTROL SELECT
BIT 0	2^0	2^0	WRITE GATE
1	2^1	2^1	READ GATE
2	2^2	2^2	SERVO OFFSET PLUS
3	2^3		SERVO OFFSET MINUS
4	2^4	2^4 *	FAULT CLEAR
5	2^5		AM ENABLE
6	2^6		RTZ
7	2^7		DATA STROBE EARLY
8	2^8		DATA STROBE LATE
9	2^9		

* This BIT is volume address which is stored within the drive. The stored volume address and "TAG 1" result in a volume select if the cylinder address is valid. Refer to disk drive manual for timing. A zero denotes the removable cartridge and a one denotes the fixed disks.

The major processing components of this board set are the CPU microprocessor (U11) and the DMA Address Generator (U10 and U21). The ROM (U31) contains the bootstrap load routine and also contain the microcode necessary for operation of the microprocessors.

4.1.1 POWER-UP RESET.

On initial power-up, the circuit board is in a dormant state waiting for initialization. The PRESET signal from the S-100 Bus sets the INIT flip-flop U14 to activate the PHANTOM signal to disable any memory under phantom control and to enable the bootstrap gate. INIT generally resets logic on the circuit board to initial conditions.

4.1.2 ADDRESSING.

Address data is received from the S-100 Bus on address lines AD0-AD15. This address data is transferred to the internal address bus during boot loading for use by the controllers and memories within the circuit board and is also used for direct addressing of the circuit board. Buffers on U28 and U36 gate the data to the internal bus when enabled by bootstrap signal BOOT.

Address lines AD2-AD7 are wired directly to comparator U27 for circuit board addressing. The other inputs come from circuit board etch or jumper wires to either +5V pull ups or ground to produce the desired address. The output of the comparator U27 is asserted when the data from the address lines compare with the address of the AM-410-1. This generates read and write signals from decoder U26. The address in etch is D0 (Hex) and other addresses can be selected as described in Section 2.

4.1.3 CPU OUTPUT.

CPU output data is transmitted to the AM-410-1 for circuit board control and data transfer by the S-100 Bus data and control lines. Data is received by the AM-410-1 by the Output Data

Register U37 and the Write Command Register U38. The input to these data registers comes from the S-100 Bus data lines D00-D07; and the output, when enabled, goes to internal data bus DB0-DB7.

4.1.3.1 COMMAND DATA.

Data from the S-100 Bus data lines is clocked into the Write Command Register by Command Write signal $\overline{\text{CMDWRT}}$ from the Command Decoder U26. This takes place when address lines AD0 and AD1 are zero and I/O output signal SOUT from the S-100 Bus is asserted. Signal $\overline{\text{CMDWRT}}$ also resets the INIT flip-flop U14 and resets the initiate logic.

When the CPU microprocessor issues a write command ($\overline{\text{ZWR}}$) and address lines AB14 and AB15 from the internal address bus are both one, $\overline{\text{IOSEL}}$ is asserted to enable the Read/Write decoder U25. Signal $\overline{\text{ZWR}}$ is also applied to buffer U28 to generate $\overline{\text{WR}}$ which is an input to the Read/Write decoder. When address bits AB0 and AB1 from the internal bus are zero, the $\overline{\text{RDO}}$ output from the Read/Write decoder transfers the contents of the write command register to the internal data bus.

4.1.3.2 COMMAND TYPES.

The non-disk commands issued to the AM-410-1 are used for control and operation of the logic internal to the circuit board. The bit functions are listed in Table 4-5 and the commands are listed in Table 4-6. Disk Commands are used to control the disk drive and access status information from the drive. Disk command bit functions are listed in Table 4-7, and disk command codes are listed in Table 4-8.

Table 4-5. Non-Disk Command Bits

BIT	NAME	FUNCTION																								
0	0	<div style="border: 1px solid black; display: inline-block; padding: 2px;">=0</div> Indicates non-disk command <div style="border: 1px solid black; display: inline-block; padding: 2px;">=1</div> Activity Bit.																								
1	1																									
2	R/W	Read/Write 0=read (AM-410 to CPU), 1=write (CPU to AM-410).																								
3	FN	Command Function 0=transfer 1=execute																								
4	BUF	Location in DMA buffer where data is to be retrieved or stored.*																								
5	DMA																									
6	CLR	Clear current interrupt 0=nop 1=clear																								
7	IE	Interrupt Enable 0=disable 1=enable																								
		<table border="1" style="border-collapse: collapse; width: 100%;"> <thead> <tr> <th colspan="2" style="text-align: left;">*</th> <th style="text-align: center;">Bit</th> <th style="text-align: center;">Location</th> </tr> <tr> <th style="width: 20px;"></th> <th style="width: 20px;"></th> <th style="width: 20px; text-align: center;">5</th> <th style="width: 20px; text-align: center;">4</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">0</td> <td style="text-align: center;">RAM Base (Direct)</td> </tr> <tr> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">Data Buffer</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">0</td> <td style="text-align: center;">1</td> <td style="text-align: center;">User Pointer</td> </tr> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">1</td> <td style="text-align: center;">@ User Pointer (Indirect)</td> </tr> </tbody> </table>	*		Bit	Location			5	4	0	0	0	RAM Base (Direct)	0	1	0	Data Buffer	1	0	1	User Pointer	1	1	1	@ User Pointer (Indirect)
*		Bit	Location																							
		5	4																							
0	0	0	RAM Base (Direct)																							
0	1	0	Data Buffer																							
1	0	1	User Pointer																							
1	1	1	@ User Pointer (Indirect)																							

Table 4-6. Non-Disk Command Formats

BITS 7 6 5 4 3 2 1 0	FUNCTION
0 0 0 0 0 0 0 0 X X 0 0 0 1 1 0 X X 0 1 0 1 1 0	Initialization/Boot Load Write data to DMA buffer (RAM Base) Write data to DMA buffer (Data Base)
X X 0 0 0 0 1 0 X X 0 1 0 0 1 0	Read data from DMA buffer (RAM Base) Read data from DMA buffer (Data Base)
0 1 0 0 0 0 0 0 X 1 X X X X 1 0	Clear Interrupt (Clear Only) Clear Interrupt (Plus some other non-disk command)
X X 1 0 0 1 1 0	Write user microcode pointer
X X 1 1 0 1 1 0	Indirect load via user pointer
X X 1 1 1 0 1 0	Execute from users microcode pointer
X X 1 1 0 0 1 0	Indirect read via user pointer
X X 1 0 0 0 1 0	Read user microcode pointer

Table 4-7. Disk Command Bits

BIT	NAME	FUNCTION
0	DSK	Always 1 for disk type commands
1 2		⌋ Command function comprised of bits 1, 2, and 3 taken as a whole (see Table 4-8).
3	R/W*	0=read 1=write
4	SK	Seek
5	-	Not used
6	-	Not used
7	IE	Interrupt enable 0=disable 1=enable

* See Table 4-8

Table 4-8. Disk Command Codes

BITS			FUNCTION
3 R/W	2	1	
0	0	0	Read Status Check
0	0	1	Restore to Cylinder Zero
0	1	0	Read Record
0	1	1	Read Record
1	0	0	Write Record
1	0	1	Write Status Check

4.1.3.3 OUTPUT DATA.

The output data from the CPU to the AM-410-1 transfers from the S-100 Bus data lines to the internal data bus through the Output Data Register U37. The input to the Output Data Register comes from the S-100 Bus data lines D00-D07; and the output, when enabled, goes to the internal AM-410 data bus DB0-DB7.

Data from the S-100 Bus data lines is clocked into the Output Data Register by data write signal $\overline{\text{DATWRT}}$. This is generated by the Command Decoder when the board is addressed and address lines AD0=1 and AD1=0 and I/O output signals SOUT and $\overline{\text{PWR}}$ from the S-100 Bus are asserted. Signal $\overline{\text{DATWRT}}$ also sets flip-flops in the S-100 transfer logic to generate $\overline{\text{RX1}}$ to transfer the data from the Output Data Register to the internal bus during internal S-100 type DMA cycles.

4.1.4 CPU INPUT.

CPU input data is transmitted from the AM-410-1 by the S-100 Bus data and control lines. It is transmitted from the AM-410-1 by the Status Register (U40) and the Input Data Register (U39).

4.1.4.1 STATUS REGISTER.

The Status Register is used to determine the current status of AM-410 board set operations and to indicate disk drive faults. The input to the Status Register comes from the internal data bus DB0-DB7; and the output, when enabled, goes to the S-100 Bus data lines DI0-DI7.

Data from the internal data bus is clocked into the Status Register by signal $\overline{\text{WRO}}$ from the Read/Write Decoder (U25). This occurs when the lines AD0, AD1, AD3 and $\overline{\text{WR}}$ are all low. The contents of the Status Register are transferred to the S-100 Bus data lines by the $\overline{\text{STATIN}}$ signal from the Command Decoder. This signal is issued when ABO=0, AB1=0, PDBIN is true (high) and $\overline{\text{PWR}}$ is false (high).

4.1.4.2 STATUS WORD FORMATS.

Status words contain information regarding the operation of the AM-410 board set and associated disk drives. Status word information and formats are contained in Figure 4-3. Bit 7 is the Command Received (CR) bit (1=Received, 0=Cleared).

When the status word is received by the CPU, the data is checked for any of the four codes shown at the top of Figure 4-3. If the disk error code is found, the disk error status is accessed from the data register. Bit definitions for disk faults are shown in Figure 4-3.

4.1.4.3 INPUT DATA REGISTER.

The Input Data Register (U39) controls the transfer of data from the internal data bus to the S-100 Bus data lines. The inputs to this register come from internal data bus DB0-DB7 and the output; when enabled, goes to the S-100 Bus data lines DI0-DI7.

Data from the internal bus is clocked into the register when either $\overline{\text{INIT}}$ or $\overline{\text{WX1}}$ are True. Signal $\overline{\text{INIT}}$ controls the register during a boot data transfer and Write transfer 1 ($\overline{\text{WX1}}$) signal comes from the S-100 Bus transfer logic. Signal $\overline{\text{WX1}}$ is generated in the same way as $\overline{\text{RX1}}$ described in paragraph 4.1.3.3 except $\overline{\text{RD}}/\text{WR}$ input to the S-100 transfer logic is in the Write state. Data is placed on the S-100 Bus data lines when in the bootstrap mode by $\overline{\text{BOOT}}$ or by the $\overline{\text{DATRD}}$ output of the Command decoder. Signal $\overline{\text{DATRD}}$ is issued when the board is addressed and $\text{AD0}=1$, $\text{AD1}=0$, Read Enable PDBIN is true (high) and Write Strobe $\overline{\text{PWR}}$ is false (high).

4.1.5 BOOT LOAD PROCEDURE.

The AM-410-1 contains a bootstrap load routine stored in the ROM on U31. The microcode for internal AM-410-1 microprocessor operation is also contained in the first 1K of ROM memory. The bootstrap program is contained in the second 1K of ROM memory.

BIT								FUNCTION
7*	6	5	4	3	2	1	0	
CR	0	0	0	0	0	0	0	Status OK - Function Complete
CR	0	0	0	0	1	0	1	Disk Not Ready
CR	0	0	0	1	0	1	1	Write Protected
CR	0	0	0	1	1	1	1	Disk Error - See Below

* CR = Command Received, 0 = Cleared, 1 = Received

DATA REGISTER BITS FOR DISK FAULTS

D7	D6	D5	D4	D3	D2	D1	D0
DN	CR	WP	AM	UR	OC	SE	FL

- DN = DONE. INDICATES THE STATUS OF THE DMA TRANSFER (ALWAYS CLEARED).
- CR = CRC ERROR. INDICATES A CRC ERROR HAS OCCURRED.
- WP = WRITE PROTECT. INDICATES THAT THE DISK IS PROTECTED (ALWAYS CLEARED).
- AM = ADDRESS MARK. NOT USED (ALWAYS CLEARED).
- UR = UNIT READY (ALWAYS CLEARED).
- OL = ON CYLINDER. INDICATES THAT THE DRIVE DID NOT ARRIVE ON CYLINDER IN TIME
- SE = SEEK ERROR. INDICATES THAT AN INVALID CYLINDER NUMBER WAS ISSUED TO THE DRIVE.
- FL = FAULT. A DRIVE FAULT HAS OCCURRED (SEE DRIVE MANUAL).

Figure 4-3. Status Word Formats

NOTE

If the user code is changed from the current boot routine, the microcode in the first 1K of memory must be duplicated exactly.

The CPU reads the bootstrap load program by addressing the AM-410 board set and reading from F400 (Hex) up. This address, combined with S_{MEMR} from the S-100 bus and a high $\overline{\text{INIT}}$ signal which takes place on initial start-up, generates the $\overline{\text{BOOT}}$ signal. If the optional jumper is in the NO $\overline{\text{BOOT}}$ position, one input to the BOOT AND gate is connected to ground, disabling the bootstrap feature.

The $\overline{\text{BOOT}}$ signal enables the ROM (U31), the Address Buffer (U28 and U36), and the Input Data Register (U39). The $\overline{\text{INIT}}$ signal enables the clock input to the Input Data Register and since it is a transparent latch type register, the bootstrap program transfers from the ROM to the system.

4.1.6 INTERRUPTS.

The interrupt mode can be selected for AM-410 board set operation when the software program sets bit 7 in either disk or non-disk commands. When the interrupt mode is selected, the interrupt occurs at the completion of the current AM-410 command. This is taken from the internal data bus by the command register (U35) and connected to the S-100 Bus vectored interrupt lines. Any one of the seven interrupt lines ($\overline{\text{VI0}}-\overline{\text{VI7}}$) may be selected by a jumper as shown in Section 2.

The interrupt mode may be cleared by the software program so that the interrupts do not occur. The program clears the interrupt mode by setting bit 6 in any non-disk command to a one (see Table 4-5).

4.1.7 BYTE CLOCK COUNTER.

The byte clock counter controls the shift registers for serial-to-parallel and parallel-to-serial conversion of read and write operations respectively. It consists of counters on U34 and U41 with associated select and gating logic.

Signal \overline{RD}/WR selects the necessary clocks and data for either read or write disk operations. During read operations, flip-flops on U40 detect the first bit (sentinel) and presets the byte counter (U41) to a count of 6 ($\overline{JAM6}$). This counter then counts the selected clock pulses until a full byte is loaded into shift register U31. The counter output is gated (count 7) to generate the clock to load the shift register data into buffer register U30 for transfer through the internal data bus to the RAM. Write operations are similar except the counter output \overline{BYTCLK} controls the shift/load control to write shift register U25.

4.1.8 DISK TRANSFER LOGIC.

The disk transfer logic consists of a ROM (U33), a counter to sequence the ROM (U23 and U24), an input MUX (U13) and a D flip-flop register to buffer the ROM output (U32): This logic is common to both disk read and disk write, DMA transfer operations.

Signal \overline{BYTENB} , that occurs once for each byte of data transferred, provides the clock input to the ROM sequence counter. Sequencing the ROM through its program controls the transfer of data from the disk to RAM and RAM to disk.

4.1.9 SECTOR COUNTER.

The sector counter logic enables the controller to read or write data in a specific sector on the selected disk. Signal \overline{WRE} clocks the data from the data bus DB0-DB7 into register U20. At the disk index, signal INDEX resets counter U32 to zero

and it then counts disk sector pulses (SECTOR) and provides its counter output to comparator U26. The other input to the comparator is the selected sector number stored in register U20. When the sector count equals the selected count, the compare output of the comparator generates sector equal signal (SECEQU) to the disk transfer logic on the AM-410 circuit board.

4.1.10 OUTPUT TO DISK DRIVE.

This circuit board set transfers disk drive controls and write data to the disk drives through shift registers and control logic located on the AM-410-2 circuit board. See Table 4-3 for a complete list of the signals between the AM-410-2 and the disk drive. All wiring is listed with a description of each signal.

4.1.10.1 DATA WRITE LOGIC.

The data write logic provides the clock and data outputs necessary for the disk drive write circuitry. Serial write data (WRDAT), from the write shift register on the AM-410-2 board, is sent to the CRC logic (U15) for error checking. For a description of the operation of the CRC module, see paragraph 4.2.3.

The selected clock and selected data (SELCLK and SELDAT) provide the data and clock inputs to the CRC module. Since this is a write operation, write data and servo clock are selected. The output of the CRC logic is WRITE DATA that is applied to drivers U10, U16, U22 and U28 to operate the selected write head. The SERVO CLK is inverted and applied to a delay to compensate for the propagation delays inherent in the write data path. The write clock is then applied to drivers in the same manner as the write data for operation of the selected disk drive.

4.1.10.2 DISK DRIVE CONTROLS.

Control and selection commands for the disk drives are listed with their descriptions in Table 4-3. This control data is taken through the data bus DB0-DB7 and stored in latches U13, U18 and U19. These latches are controlled by the control decoder from address bits AB0-AB3. The unit select data is also taken from the data bus and stored in the unit select buffer U12. The decoder U42 then selects read/ write pairs of drivers/receivers for disk operation via the unit select codes and also provides unit select outputs to the daisy-chain cable through driver U11. The other control outputs are also driven through drivers U1-U3 and U17 to the daisy-chain cable.

4.1.11 INPUT FROM DISK DRIVE.

This circuit board set reads disk data and receives clock and status data from the disk drive through shift registers and controls located on the AM-410-2 circuit board. See Table 4-3 for a complete list of the signals between the AM-410-2 and the disk drive. All wiring is listed with a description of each signal.

Write data and clocks are received from the selected drive through line receivers U9, U15, U21 and U27. Selection of the desired receiver occurs with the selection of the output drivers as described in the preceding paragraphs.

Serial READ DATA and DATA CLK are applied to shift register for serial-to-parallel conversion. The data is then clocked into the register (U30) at the end of each 8-bit byte by BYTCLK, the output of the byte clock counter. The read data strobe RDATASTB from the disk data control logic (U18) transfers that byte of data to the data bus DB0-DB7 and into the RAM (U41 and U42).

4.1.12 AM-410 BOARD SET OPERATIONS AND TIMING.

The following paragraphs describe the timing and sequence of operations of the AM-410 board set. The numbers in parenthesis refer to the numbers on the associated timing diagram.

4.1.12.1 DATA TRANSFER OPERATIONS.

The system CPU issues a command to the AM-410 to perform a data transfer type of operation (data to or from the disk, or data to or from the S-100 bus). The on-board CPU sets up the board for the kind of transfer requested (disk or S-100), sets the direction of transfer (read data into the board or write data out from the board) via the $\overline{RD}/\overline{WR}$ bit, and sets up the DMA chips with their required address and word counts. The CPU then issues a GO command as shown in Figure 4-4. When the GO line goes high, it sets flip-flop U5, which causes \overline{BREQ} to be asserted (1). When \overline{BREQ} (Bus Request) is asserted, the on-board CPU will, at its earliest convenience, take itself off the data and address busses and issue a \overline{BACK} (Bus Acknowledge) signal (2). Since \overline{BACK} indicates that the on-board CPU is tri-stated, the DMA circuitry can now use the data and address busses. The DMA circuit then does its job of transferring the data. When the last byte of data is transferred, a DONE signal is issued by the DMA logic. The issuance of DONE causes \overline{BREQ} to drop (3), thereby allowing the on-board CPU to reactivate itself (4), which then shuts off the GO signal (5).

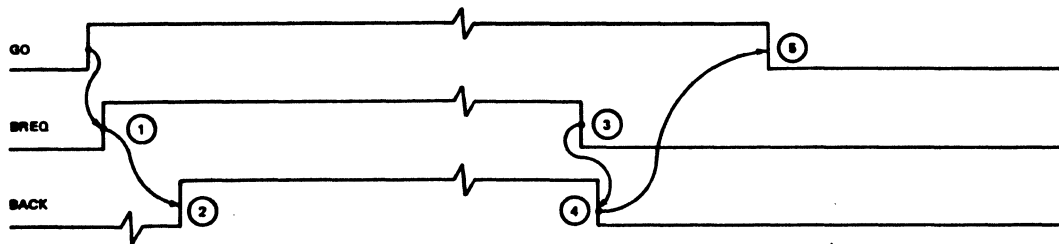


Figure 4-4. Data Transfer Timing

4.1.12.2 DISK TRANSFER OPERATIONS.

When the AM-410 has been issued a disk transfer command (read or write a sector), the on-board CPU checks the disk drive for error conditions and, if possible, corrects the condition.

If no error exists, or it is corrected, the on-board CPU issues a GODSK command, as shown in Figure 4-5. (GODSK is the logical AND of signals GO, DISK and the CPU being tri-stated--D_{MAX}).

GODSK causes the micro-engine (U13, U23, U24, U32, U33) to start up. The micro-engine then waits for the SECEQU (Sector Equals Requested Count) pulse. At this point, the micro-engine begins its sector format function, which causes the timing signals RDGATE, WRGATE, OG, CRCLR, CWEN (Read Gate, Write Gate, Output Gate, CRC Clear, Check Word Enable) to be issued at the appropriate time. The micro-engine is sequenced by the BYTCLK/BYTENB (Byte Clock, Byte Enable) signals, which are derived from the drive itself.

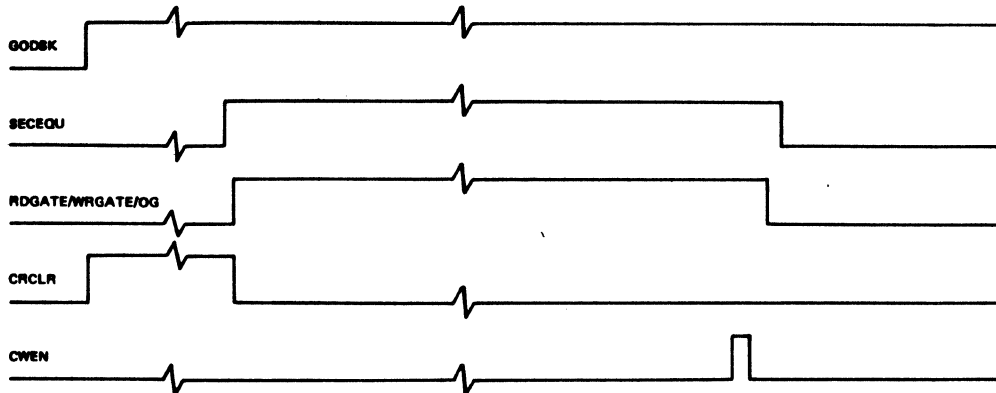


Figure 4-5. Disk Transfer Timing

4.1.12.3 DISK READ CLOCKS.

The BYTCLK, $\overline{\text{BYTENB}}$ timing, as shown in Figure 4-6, is based on the two signals SERVO CLOCK and READ CLOCK, both of which are received from the drive. The SERVO CLOCK signal is used for write timing while the READ CLOCK signal is used during a disk read function. Both BYTCLK and $\overline{\text{BYTENB}}$ are derived from a counter U41. The counter counts the rising edge of either SERVO CLOCK or READ CLOCK depending on the state of the $\overline{\text{RD}}/\text{WR}$ signal at U43. When this count equals 7, BYTCLK and $\overline{\text{BYTENB}}$ are issued. When the count equals 0 (the next state) BYTCLK is dropped but $\overline{\text{BYTENB}}$ remains high. This causes $\overline{\text{BYTENB}}$ to be twice as long as BYTCLK, but they both indicate when the last bit of a byte has been read or written.

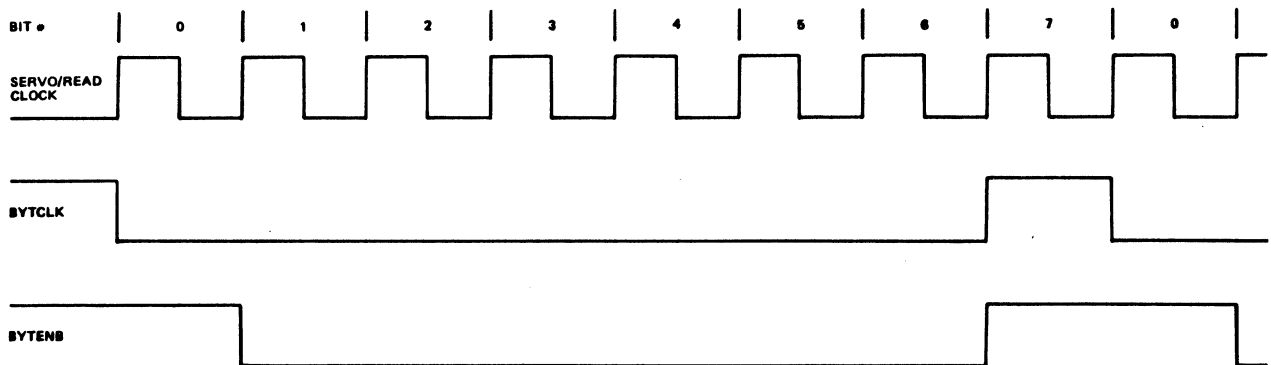


Figure 4-6. BYTCLK-BYTENB Timing

4.1.12.4 DISK WRITE CLOCKS.

The SERVO CLOCK from the drive is delayed and then transmitted as the WRITE CLOCK to the drive. The delay is set to equal the propagation delay of the CRC circuit. The WRITE CLOCK signal and the WRITE DATA signal must have the relationship shown in Figure 4-7. The rising edge of WRITE CLOCK must occur in the middle of the data cell of both the undelayed WRDATA and the CRC check word as it is issued from the CRC generator.

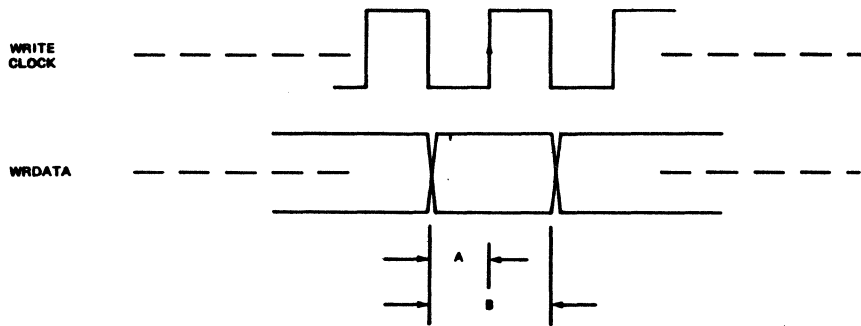


Figure 4-7. Disk Write Timing

4.1.12.5 SECTOR BEGINNING FORMAT OPERATIONS.

This timing shows in greater detail (see Figure 4-8) the relationship between the various sector format signals, as created by the microengine, at the beginning of the sector. Note that the microengine has no idea of the direction of transfer, and therefore issues timing signals for both the read and write transfers. When the sector counter equals the requested sector number, a SECEQU (Sector Equal) pulse is issued. At the next byte, the WRGATE (Write Gate) signal goes high and the CRCLR (CRC Clear) signal is dropped. One byte later the RDGATE (Read Gate) signal goes high. Twelve bytes after read gate, OG (Output Gate) is raised. This signal enables the transfer of data to/from the RAM. This twelfth byte is a special byte. During a

write, a "sentinel" bit is written, while during a read, the BYTCLK is disabled until the sentinel bit is detected. The BYTCLK is disabled until the sentinel bit is detected. The sentinel bit is the indicator of the physical beginning of the sector. It is written out on the twelfth byte so that during a read, when the absolute timing from the sector pulse to the first bit of data is not known, the data bit cells can be synchronized. This means that the sentinel bit is written so that during a read the byte is synchronized such that bit 0 is interpreted as bit 0 and not as any other bit.

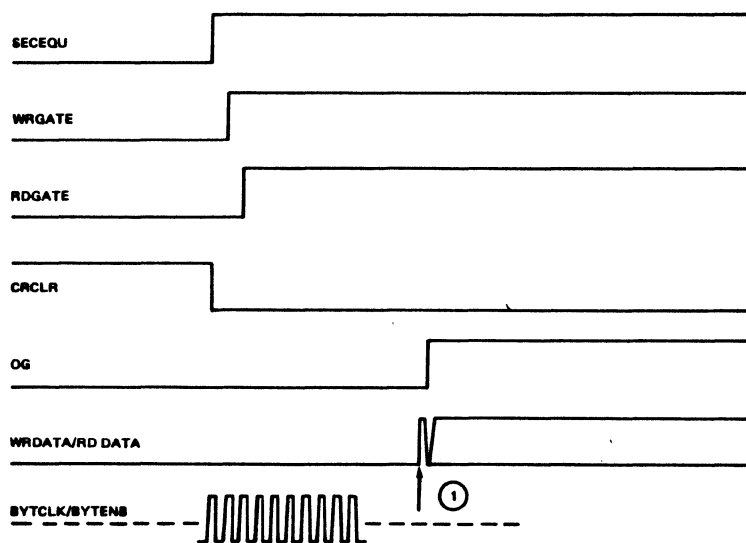


Figure 4-8. Sector Beginning Timing

4.1.12.6 SECTOR END FORMAT OPERATIONS.

This timing shows (see Figure 4-9) in greater detail the relationship between the sector format signals at the end of a sector. After 512 bytes of data have been transferred into RAM (one per $\text{BYTCLK}/\text{BYTENB}$) the CWEN (Check Word Enable) signal goes high causing the CRC generator to output the current check word if a write is occurring. During a read, the CWEN signal is ignored and the check word is entered into the serial data stream to be checked by the CRC chip. At the end of this time the CRC generator will issue a CRCERR (CRC Error) signal if an error in receiving occurred. A transmit CRC error is impossible. OG (Output Gate) drops at the end of the CRC field, shutting off further data transfers to RAM. RDGATE (Read Gate) is dropped after OG to insure that no glitches enter into the serial data stream, and WRGATE (Write Gate) drops several bytes later to insure that the data stream after the CRC check word is zero. A short while later, the next sector pulse, defining the next sector, occurs and SECEQU also drops. The DONE signal will have occurred coincident with the falling edge of OG causing the DMA cycle to end and return bus control back to the on-board CPU.

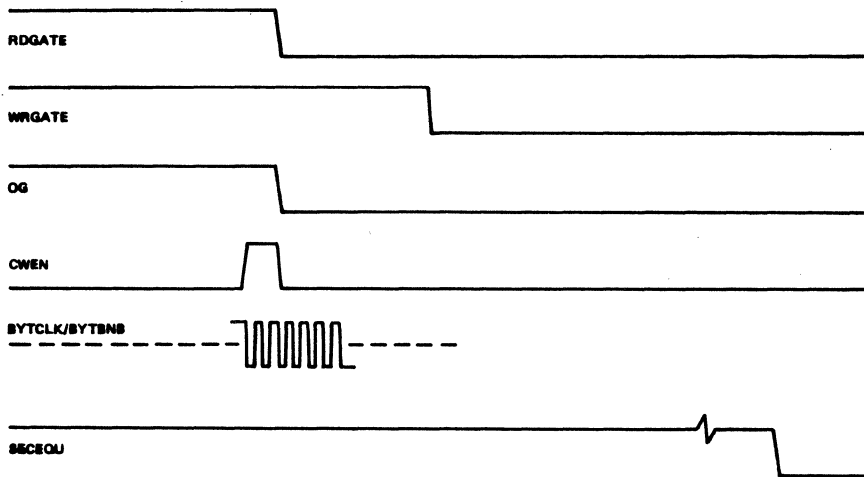


Figure 4-9. Sector End Format Timing

4.1.12.7 DMA TRANSFER OPERATIONS.

The whole process of transferring data to or from the RAM, to or from the board, is done as a DMA cycle. The CPU sets up the board for the transfer, sets the DMA address and word counts, sets the read/write bit for transfer into or out of the AM-410, and then sets the GO bit and either the DISK bit or the S-100 bit. These three bits, (DISK, S-100 and $\overline{RD/WR}$) cause the DMA cycle to follow the correct path. The IC's U18 and U19 steer the DMA logic to provide the requested transfer. U18 is used for a disk type transfer, while U19 is used for the S-100 type transfer. For any of the four types of transfers, RAM to S-100, S-100 to RAM, RAM to disk, or disk to RAM, the process is to set the three bits in the registers ($\overline{RD/WR}$, DISK, or S-100) and issue a GO command. The DMA hardware takes care of the rest of the process. Each byte is transferred into or out of RAM via one of two signals: BYTENB or \emptyset 2ENB (phase 2 Enable). BYTENB is used for a disk type transfer, and \emptyset 2ENB is used for the S-100 type transfers. Each signal was designed to be no less than 200ns, or the access time of the RAMs. To this end the signal \emptyset 2ENB is one whole cycle of the 4MHz master clock. When the system CPU reads from or writes to the AM-410 data ports, a DATRD (Data Read) or DATWRT (Data Write) pulse occurs. These signals are OR'ed to cause a SDREQ (S-100 DMA Request) which forces JK flip-flop U17 to toggle, creating \emptyset 2ENB.

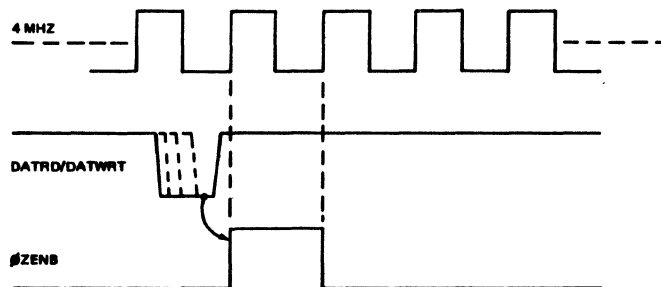


Figure 4-10. DMA Transfer Timing

4.2 CIRCUIT MODULE DESCRIPTION.

This section describes the operation of the individual circuit packages (DIPS) contained on the AM-410 circuit board. Most of the processing is handled by the CPU and DMA address generator modules, so these are described in detail. The control logic and interface modules are also described with logic and connection diagrams for each one.

4.2.1 CPU MICROPROCESSOR (AM-410-1, U11).

The CPU microprocessor is a single DIP module that handles the data processing of the AM-410 circuit board.

Figure 4-11 is a block diagram of the CPU, and Figure 4-12 details the internal register configuration which contains 208 bits of Read/ Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to an interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

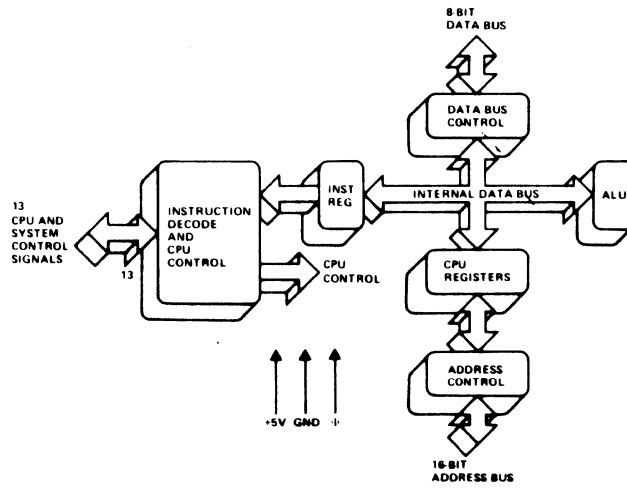


Figure 4-11. CPU Block Diagram

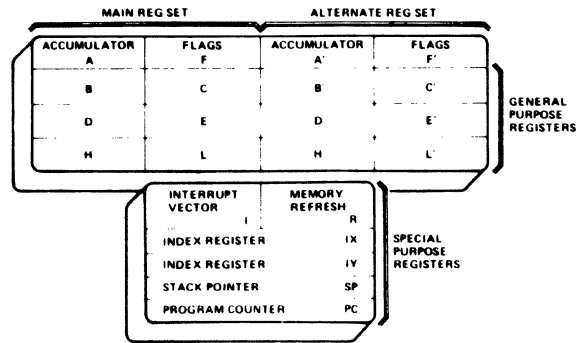


Figure 4-12. CPU Registers

Figure 4-13 shows the CPU pin configuration and Table 4-9 contains a list of the CPU signals.

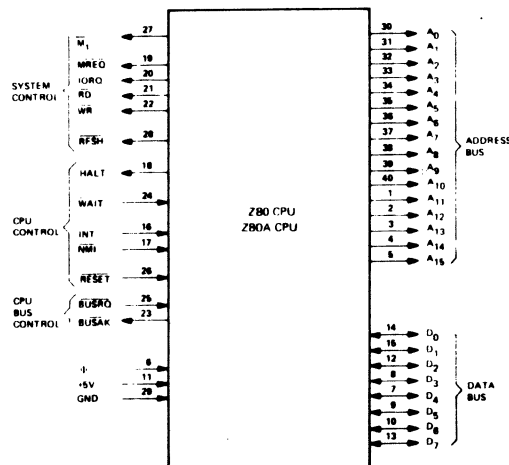


Figure 4-13. CPU Pin Configuration

Table 4-9. CPU Signal List

SIGNAL	PIN	FUNCTION
A0-A15 ADDRESS BUS		Tri-state output, active high. A0-A15 constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.
D0-D7 DATA BUS		Tri-state input/output, active high. D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.
$\overline{M1}$ MACHINE CYCLE ONE	27	Output, active low. $\overline{M1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.
\overline{MREQ} MEMORY REQUEST	19	Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.
\overline{IORQ} INPUT/OUTPUT REQUEST	20	Tri-state output, active low. The \overline{IORQ} signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An IORQ signal is also generated when an interrupt is being acknowledged to indicate that an

Table 4-9 (Cont.). CPU Signal List

SIGNAL	PIN	FUNCTION
		interrupt response vector can be placed on the data bus.
$\overline{\text{RD}}$ MEMORY READ	21	Tri-state output, active low. $\overline{\text{RD}}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
$\overline{\text{WR}}$ MEMORY WRITE	22	Tri-state output, active low. $\overline{\text{WR}}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
$\overline{\text{RFSH}}$ REFRESH	28	Output, active low. $\overline{\text{RFSH}}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{\text{MREQ}}$ signal should be used to do a refresh read to all dynamic memories.
$\overline{\text{HALT}}$ HALT STATE	18	Output, active low. $\overline{\text{HALT}}$ indicates that the CPU has executed a $\overline{\text{HALT}}$ software instruction and is awaiting either a nonmaskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

Table 4-9 (Cont.). CPU Signal List

SIGNAL	PIN	FUNCTION
$\overline{\text{WAIT}}$ WAIT	24	Input, active low. $\overline{\text{WAIT}}$ indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.
$\overline{\text{INT}}$ INTERRUPT REQUEST	16	Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.
$\overline{\text{NMI}}$ NON MASKABLE INTERRUPT	17	Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{\text{INT}}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{\text{NMI}}$ automatically forces the CPU to restart to location 0066H.
$\overline{\text{RESET}}$	26	Input, active low. $\overline{\text{RESET}}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state

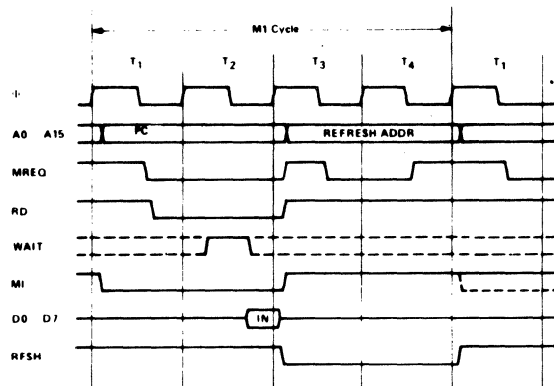
Table 4-9 (Cont.). CPU Signal List

SIGNAL	PIN	FUNCTION
		and all control output signals go to the inactive state.
$\overline{\text{BUSRQ}}$ BUS REQUEST	25	Input, active low. The bus request signal has a higher priority than $\overline{\text{NMI}}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.
$\overline{\text{BUSAK}}$ BUS ACKNOWLEDGE	23	Output, active low. Bus acknowledges is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

4.2.1.1 INSTRUCTION OP-CODE FETCH.

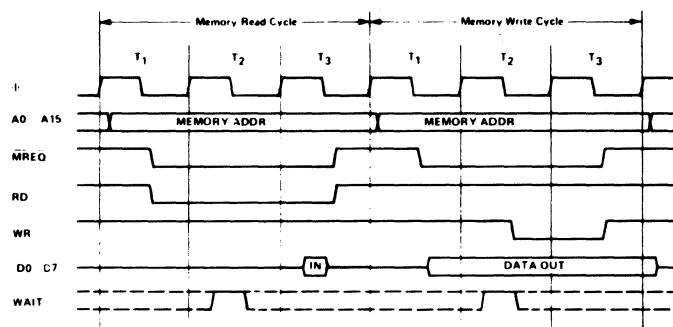
The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{\text{MREQ}}$ goes active. The falling edge of $\overline{\text{MREQ}}$ can be used directly as a chip enable to dynamic memories. $\overline{\text{RD}}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T3. Clock states T3 and T4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The

refresh control signal $\overline{\text{RFSH}}$ indicates that a refresh read of all dynamic memories should be accomplished.



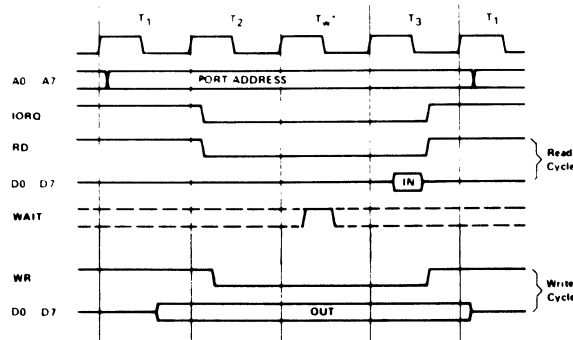
4.2.1.2 MEMORY READ OR WRITE CYCLES.

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M1 cycle). The $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{\text{MREQ}}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{\text{WR}}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



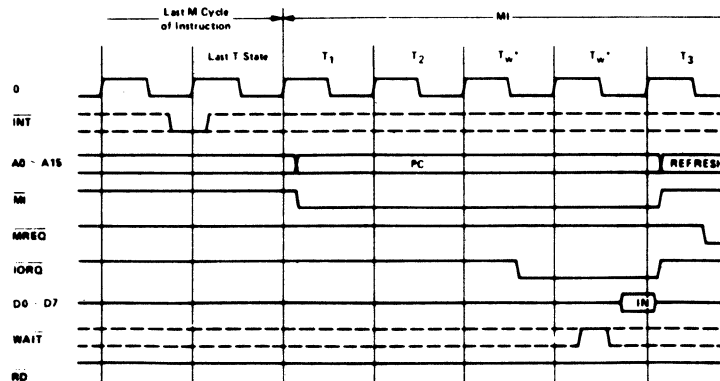
4.2.1.3 INPUT OR OUTPUT CYCLES.

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (T_w^*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{\text{WAIT}}$ line if a wait is required.



4.2.1.4 INTERRUPT REQUEST/ACKNOWLEDGE CYCLE.

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M1 cycle is generated. During this M1 cycle, the $\overline{\text{IORQ}}$ signal becomes active (instead of $\overline{\text{MREQ}}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (T_w^*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the peripheral controllers, can be easily implemented.



4.2.1.5 CPU INSTRUCTION SET.

The following is a summary of the CPU instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. The instructions are divided into the following categories:

8-bit loads	Miscellaneous Group
16-bit loads	Rotates and Shifts
Exchanges	Bit Set, Reset and Test
Memory Block Moves	Input and Output
Memory Block Searches	Jumps
8-bit arithmetic and logic	Calls
16-bit arithmetic	Restarts
General purpose Accumulator	Returns
& Flag Operations	

In Table 4-10, the following terminology is used:

b	≡ a bit number in any 8-bit register or memory location	d	≡ any 8-bit destination register or memory location
cc	≡ flag condition code	dd	≡ any 16-bit destination register or memory location
NZ	≡ non zero	e	≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing
Z	≡ zero	L	≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56
NC	≡ non carry	n	≡ any 8-bit binary number
C	≡ carry	nn	≡ any 16-bit binary number
PO	≡ Parity odd or no over flow	r	≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)
PE	≡ Parity even or over flow	s	≡ any 8-bit source register or memory location
P	≡ Positive	sb	≡ a bit in a specific 8-bit register or memory location
M	≡ Negative (minus)	ss	≡ any 16-bit source register or memory location
		subscript "L"	≡ the low order 8 bits of a 16-bit register
		subscript "H"	≡ the high order 8 bits of a 16-bit register
		()	≡ the contents within the () are to be used as a pointer to a memory location or I/O port number
			8-bit registers are A, B, C, D, E, H, L, I and R
			16-bit register pairs are AF, BC, DE and HL
			16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

Immediate	Indexed
Immediate extended	Register
Modified Page Zero	Implied
Relative	Register Indirect
Extended	Bit

Table 4-10. CPU Instruction Set

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	$r \leftarrow s$	$s \equiv r, n, (HL), (IX+e), (IY+e)$
	LD d, r	$d \leftarrow r$	$d \equiv (HL), r, (IX+e), (IY+e)$
	LD d, n	$d \leftarrow n$	$d \equiv (HL), (IX+e), (IY+e)$
	LD A, s	$A \leftarrow s$	$s \equiv (BC), (DE), (nn), I, R$
	LD d, A	$d \leftarrow A$	$d \equiv (BC), (DE), (nn), I, R$
16-BIT LOADS	LD dd, nn	$dd \leftarrow nn$	$dd \equiv BC, DE, HL, SP, IX, IY$
	LD dd, (nn)	$dd \leftarrow (nn)$	$dd \equiv BC, DE, HL, SP, IX, IY$
	LD (nn), ss	$(nn) \leftarrow ss$	$ss \equiv BC, DE, HL, SP, IX, IY$
	LD SP, ss PUSH ss	$SP \leftarrow ss$ $(SP-1) \leftarrow ss_H; (SP-2) \leftarrow ss_L$	$ss = HL, IX, IY$ $ss = BC, DE, HL, AF, IX, IY$
	POP dd	$dd_L \leftarrow (SP); dd_H \leftarrow (SP+1)$	$dd = BC, DE, HL, AF, IX, IY$
EXCHANGES	EX DE, HL EX AF, AF' EXX	$DE \leftrightarrow HL$ $AF \leftrightarrow AF'$ $\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L, (SP+1) \leftrightarrow ss_H$	$ss \equiv HL, IX, IY$
MEMORY BLOCK MOVES	LDI	$(DE) \leftarrow (HL), DE \leftarrow DE+1$ $HL \leftarrow HL+1, BC \leftarrow BC-1$	
	LDIR	$(DE) \leftarrow (HL), DE \leftarrow DE+1$ $HL \leftarrow HL+1, BC \leftarrow BC-1$ Repeat until $BC = 0$	
	LDD	$(DE) \leftarrow (HL), DE \leftarrow DE-1$ $HL \leftarrow HL-1, BC \leftarrow BC-1$	
	LDDR	$(DE) \leftarrow (HL), DE \leftarrow DE-1$ $HL \leftarrow HL-1, BC \leftarrow BC-1$ Repeat until $BC = 0$	

Table 4-10 (Cont.). CPU Instruction Set

	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK SEARCHES	CPI	A ← (HL), HL ← HL+1 BC ← BC-1	A ← (HL) sets the flags only. A is not affected
	CPIR	A ← (HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	
	CPD	A ← (HL), HL ← HL-1 BC ← BC-1	
	CPDR	A ← (HL), HL ← HL-1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	CY is the carry flag s ≡ r, n, (HL) (IX+e), (IY+e) s = r, n (HL) (IX+e), (IY+e) d = r, (HL) (IX+e), (IY+e)
	ADC s	A ← A + s + CY	
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	
	CP s	A - s	
	INC d	d ← d + 1	
DEC d	d ← d - 1		
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	} ss ≡ BC, DE HL, SP ss ≡ BC, DE, IX, SP ss ≡ BC, DE, IY, SP dd ≡ BC, DE, HL, SP, IX, IY dd ≡ BC, DE, HL, SP, IX, IY
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	
	ADD IY, ss	IY ← IY + ss	
	INC dd	dd ← dd + 1	
	DEC dd	dd ← dd - 1	
GP ACC. AND FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	A ← \overline{A}	
	NEG	A ← 00 - A	
	CCF	CY ← \overline{CY}	
	SCF	CY ← 1	

Table 4-10 (Cont.). CPU Instruction Set

	Mnemonic	Symbolic Operation	Comments
MISCELLANEOUS	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode
	IM 1	Set interrupt mode 1	Call to 0038H
	IM 2	Set interrupt mode 2	Indirect Call
ROTATES AND SHIFTS	RLC s		
	RL s		
	RRC s		
	RR s		
	SLA s		s ≡ r, (HL) (IX+e), (IY+e)
	SRA s		
	SRL s		
	RLD		
	RRD		
BITS S, R, AND T	BIT b, s	$Z \leftarrow \overline{s_b}$	Z is zero flag
	SET b, s	$s_b \leftarrow 1$	s ≡ r, (HL) (IX+e), (IY+e)
	RES b, s	$s_b \leftarrow 0$	
INPUT AND OUTPUT	IN A, (n)	A ← (n)	Set flags
	IN r, (C)	r ← (C)	
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C), HL ← HL - 1 B ← B - 1 Repeat until B = 0	

Table 4-10 (Cont.). CPU Instruction Set

	Mnemonic	Symbolic Operation	Comments
INPUT AND OUTPUT	OUT(n), A	$(n) \leftarrow A$	
	OUT(C), r	$(C) \leftarrow r$	
	OUTI	$(C) \leftarrow (HL), HL \leftarrow HL + 1$ $B \leftarrow B - 1$	
	OTIR	$(C) \leftarrow (HL), HL \leftarrow HL + 1$ $B \leftarrow B - 1$ Repeat until $B = 0$	
	OUTD	$(C) \leftarrow (HL), HL \leftarrow HL - 1$ $B \leftarrow B - 1$	
	OTDR	$(C) \leftarrow (HL), HL \leftarrow HL - 1$ $B \leftarrow B - 1$ Repeat until $B = 0$	
JUMPS	JP nn	$PC \leftarrow nn$	$\left. \begin{array}{l} \text{NZ} \text{ PO} \\ \text{Z} \text{ PE} \\ \text{NC} \text{ P} \\ \text{C} \text{ M} \end{array} \right\} \text{cc}$ $\left. \begin{array}{l} \text{NZ} \text{ NC} \\ \text{Z} \text{ C} \end{array} \right\} \text{kk}$ ss = HL, IX, IY
	JP cc, nn	If condition cc is true $PC \leftarrow nn$, else continue	
	JR e	$PC \leftarrow PC + e$	
	JR kk, e	If condition kk is true $PC \leftarrow PC + e$, else continue	
	JP (ss)	$PC \leftarrow ss$	
	DJNZ e	$B \leftarrow B - 1$, if $B = 0$ continue, else $PC \leftarrow PC + e$	
CALLS	CALL nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L, PC \leftarrow nn$	$\left. \begin{array}{l} \text{NZ} \text{ PO} \\ \text{Z} \text{ PE} \\ \text{NC} \text{ P} \\ \text{C} \text{ M} \end{array} \right\} \text{cc}$
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	
RESTARTS	RST L	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L, PC_H \leftarrow 0$ $PC_L \leftarrow L$	
RETURNS	RET	$PC_L \leftarrow (SP),$ $PC_H \leftarrow (SP+1)$	$\left. \begin{array}{l} \text{NZ} \text{ PO} \\ \text{Z} \text{ PE} \\ \text{NC} \text{ P} \\ \text{C} \text{ M} \end{array} \right\} \text{cc}$
	RET cc	If condition cc is false continue, else same as RET	
	RETI	Return from interrupt, same as RET	
	RETN	Return from non- maskable interrupt	

4.2.2 DMA ADDRESS GENERATOR (AM-410-1, U10, U21).

This device is a high-speed, eight-bit wide direct memory access address generator slice that can be cascaded to form larger addresses. Device connections are shown in Figure 4-14.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The device can be programmed to increment or decrement the memory address in any of four control modes and executes eight different instructions. The initial address and word count are saved internally so that they can be restored later in order to repeat the data transfer operation.

Logic Symbol

Connection Diagram Top View

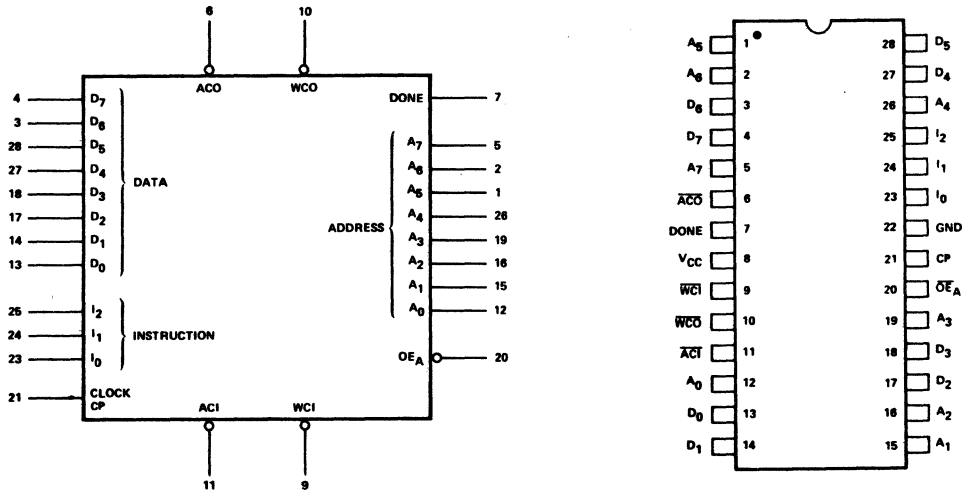


Figure 4-14. DMA Address Generator Connections

4.2.2.1 ARCHITECTURE.

As shown in Figure 4-15, the device consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

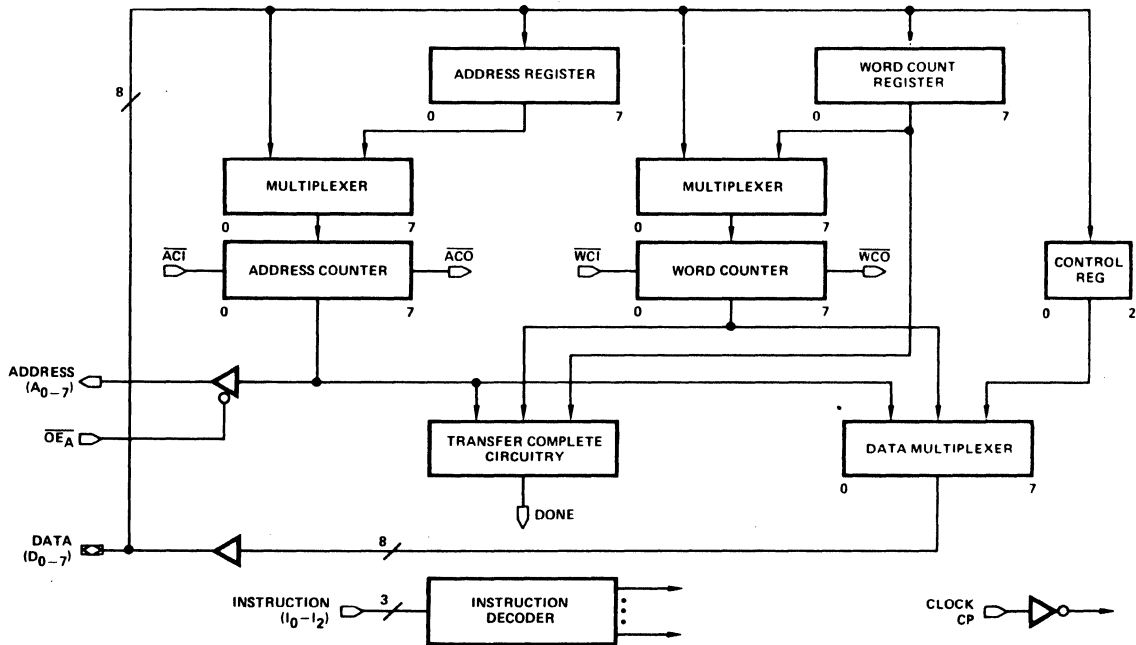


Figure 4-15. DMA Address Generator Block Diagram

Control Register. Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D0-D7. Control Register bits 0 and 1 determine the Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 4-16 defines the Control Register format.

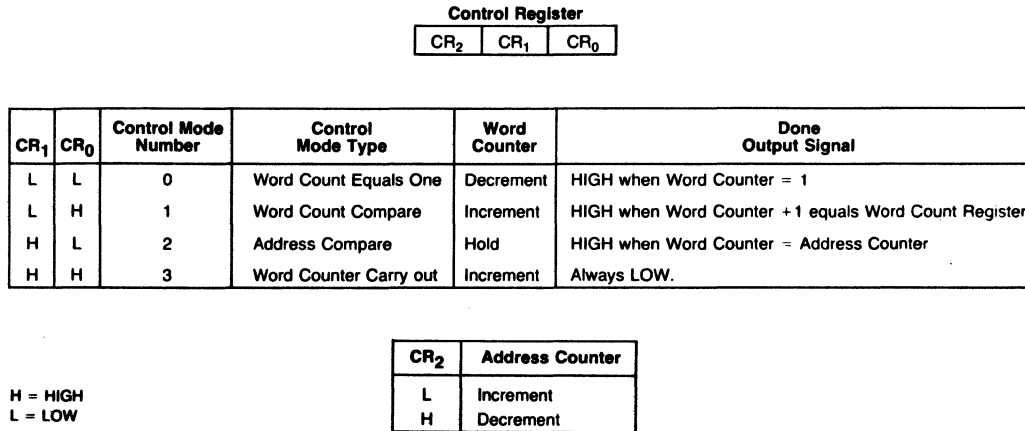


Figure 4-16. Control Register Format Definition

Address Counter. The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input (\overline{ACI}) and Address Carry Output (\overline{ACO}) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D0-D7, or the Address Register. When enabled and the \overline{ACI} input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A0-A7 under control of the Output Enable input, $\overline{OE\bar{A}}$.

Address Register. The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D0-D7.

Word Counter and Word Count Register. The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry. The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is an open-collector output, which can be dot-anded between chips.

Data Multiplexer. The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D0-D7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers. The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A0-A7, under external control. When the Output Enable input, OEA, is LOW, the Address output buffers are enabled; when OEA is HIGH, the ADDRESS lines are in the high-impedance state. The address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder. The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I0-I2 and Control Register bits 0 and 1.

Clock. The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

4.2.2.2 CONTROL MODES.

Control Mode 0 - Word Count Equals One Mode. In this mode, the number of data words to be transferred is initially loaded into the Word Counter and Word Count Register. When the Word Counter is enabled and the Word Counter Carry-in, WCI, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. The DONE signal is generated during the last word transfer; i.e., when the Word Counter equals one.

Control Mode 1 - Word Count Compare Mode. Initially, the number of data words to be transferred is loaded into the Word Count Register and the Word Counter is cleared. When the Word Counter is enabled and the WCI input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. In this mode, the Word Counter always indicates the number of data words that have been transferred. The Transfer Complete Circuitry compares the Word Counter with the Word Count Register and generates the DONE signal during the last word transfer; i.e., when the Word Counter plus one equals the Word Count Register.

Control Mode 2 - Address Compare Mode. In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the ACI input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer; i.e., when the Address Counter equals the Word Counter.

Control Mode 3 - Word Counter Carry Out Mode. For this mode of operation, the user can load the Word Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the WCI input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, WCO, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

4.2.2.3. INSTRUCTIONS.

The instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register; one instruction enables the Address and Word counters; and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 4-11 defines the instructions as a function of instruction inputs I0-I2 and the four Control Modes.

Table 4-11. DMA Register Instructions

I ₂	I ₁	I ₀	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D ₀ -D ₇
L	L	L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D ₀ -D ₂ →CR	INPUT
L	L	H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D ₀ -D ₂ (Note 1)
L	H	L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L	H	H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H	L	L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
						1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H	L	H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H	H	L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
						1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H	H	H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
						2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter

WCR = Word Count Reg.
WC = Word Counter
D = Data

L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D₃-D₇ are high during this instruction.

The WRITE CONTROL REGISTER instruction writes DATA input D0-D2 into the Control Register; DATA inputs D3-D7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D0-D2. DATA lines D3-D7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D0-D7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D0-D7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D0-D7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D0-D7, and the LOAD ADDRESS instruction writes DATA inputs D0-D7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

4.2.3 CYCLIC REDUNDANCY CHECK (CRC) GENERATOR/CHECKER (AM-410-1, U15).

Cyclic Redundancy Check (CRC) Generator/Checker is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. This device implements the polynomials listed in Table 4-12 by applying the appropriate logic levels to the select pins S0, S1 and S2. The CRC connections are shown in Figure 4-17.

The device consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the Block Diagram. The polynomial control code presented at inputs S0, S1 and S2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data Inputs (D), using the HIGH to LOW transition of the Clock Input (CP). This data is gated with the most significant Output (Q) of the register, and controls the Exclusive OR gates (Figure 4-18). The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating (Figure 4-19).

To check an incoming message for errors, both the data and check bits are entered through the D Input with the CWE Input held high. The device is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the device by a HIGH to LOW transition of \overline{CP} . If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH; ER remains valid until the next HIGH to LOW transition of \overline{CP} or until the device has been preset or reset.

A HIGH on the Master Reset Input (MR) asynchronously clears the register. A LOW on the Preset Input (\overline{P}) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials, only the most significant 12 or 8 register bits are set, and the remaining bits are cleared.

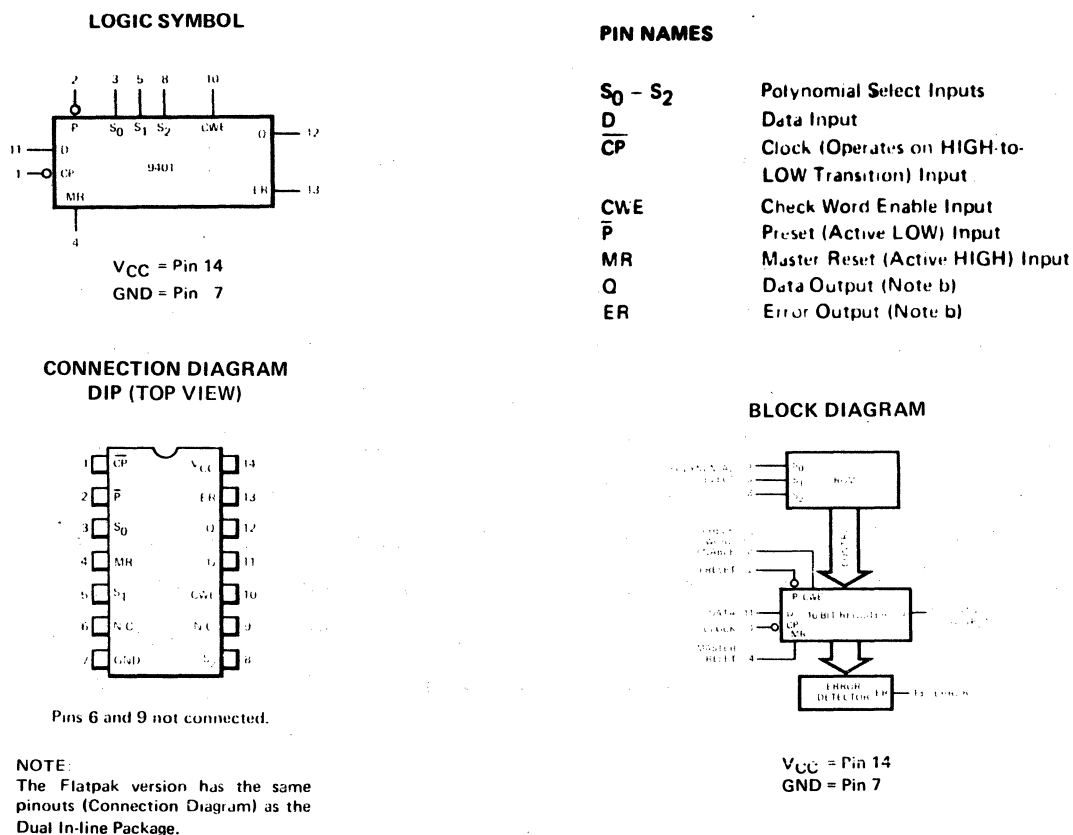


Figure 4-17. CRC Checker Connections

Table 4-12. CRC Polynomial Select Codes

SELECT CODE			POLYNOMIAL	REMARKS
S ₂	S ₁	S ₀		
L	L	L	$x^{16}+x^{15}+x^2+1$	CRC-16
L	L	H	$x^{16}+x^{14}+x+1$	CRC-16 REVERSE
L	H	L	$x^{16}+x^{15}+x^{13}+x^7+x^4+x^2+x^1+1$	
L	H	H	$x^{12}+x^{11}+x^3+x^2+x+1$	CRC-12
H	L	L	$x^8+x^7+x^5+x^4+x+1$	
H	L	H	x^8+1	LRC 8
H	H	L	$x^{16}+x^{12}+x^5+1$	CRC CCITT
H	H	H	$x^{16}+x^{11}+x^4+1$	CRC CCITT REVERSE

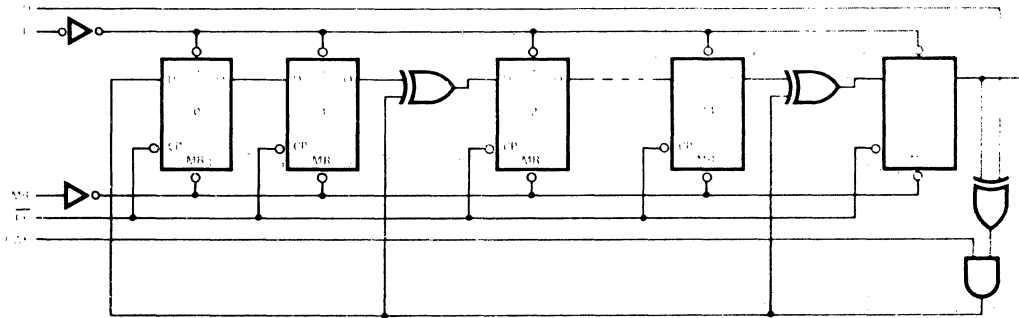
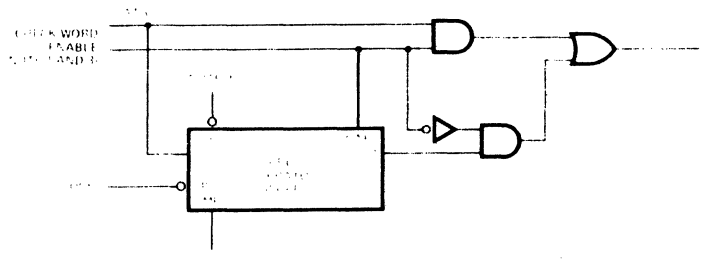


Figure 4-18. CRC Equivalent Circuit For $X^{16}+X^{15}+X^2+1$



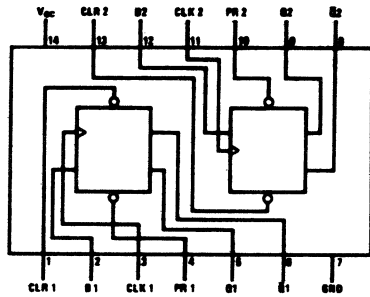
NOTES:

1. Check word Enable is HIGH while data is being clocked, LOW during transmission of status bits.
2. 9401 must be reset or preset before each computation.
3. CRC check bits are generated and appended to data bits.

Figure 4-19. CRC Check Word Generation

4.2.4 DUAL D POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR (AM-410-2, U37, U40, U44).

For logic and connections, see Figure 4-20.



TRUTH TABLE

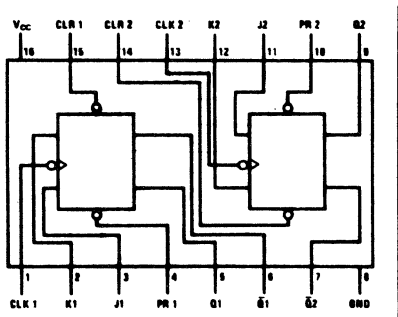
INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\bar{Q}0$

Notes. = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
 Q0 = the level of Q before the indicated input conditions were established.
 TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
 *This configuration is nonstable, that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Figure 4-20. Dual D Flip-Flop Connections

4.2.5 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR (AM-410-1, U17).

For device logic and connections, see Figure 4-21.



TRUTH TABLE

INPUTS					OUTPUTS	
PR	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\bar{Q}0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	Q0	$\bar{Q}0$

Notes. Q0 = the level of Q before the indicated input conditions were established.
 TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
 *This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

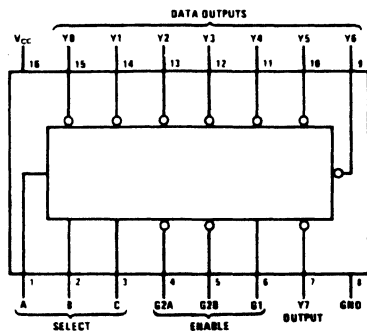
Figure 4-21. J-K Flip-Flop Connections

4.2.6 DECODER (AM-410-1, U25, U26; AM-410-2, U7, U42).

These are Schottky-clamped circuits designed for memory-decoding or data-routing applications requiring very short propagation delay times. This DIP decodes one of eight lines based on the conditions at the three binary select inputs and the three enable inputs. For logic and connections, see Figure 4-22.

Connection and Logic Diagram

Truth Table



ENABLE		SELECT			OUTPUTS							
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = High level, L = low level, X = don't care

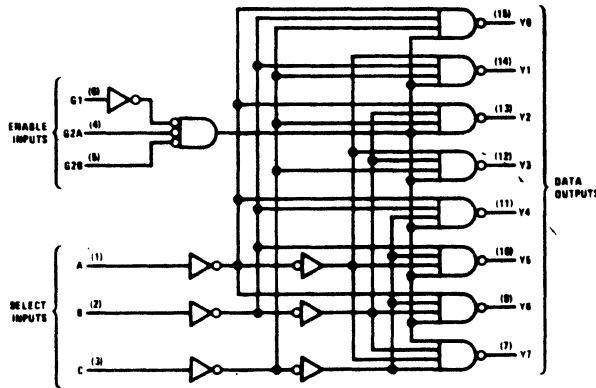


Figure 4-22. Decoder Connections

4.2.7 DECODER/DEMULTIPLEXER (AM-410-1, U30).

These Schottky-clamped circuits are designed to be used in high performance memory decoding or data routing applications requiring very short propagation delay times. This device contains two separate two-line to four-line decoders in one package. The active-low enable input can be used as a data line in demultiplexing applications. The device features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high performance Schottky diodes to suppress line-ringing. For logic and connections, see Figure 4-23.

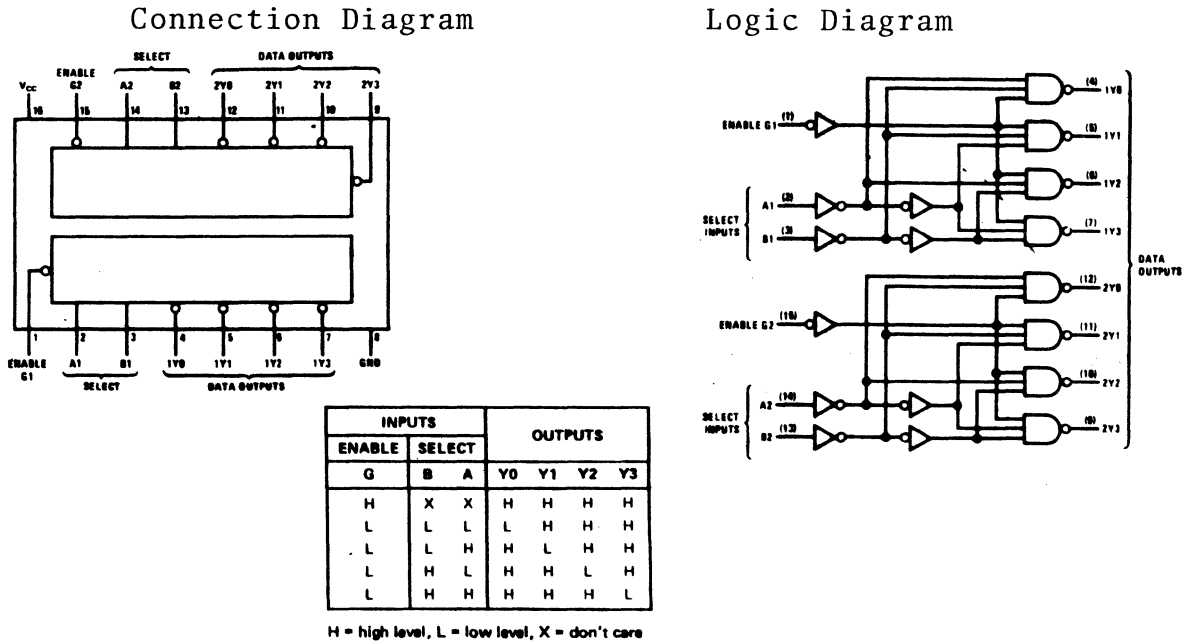
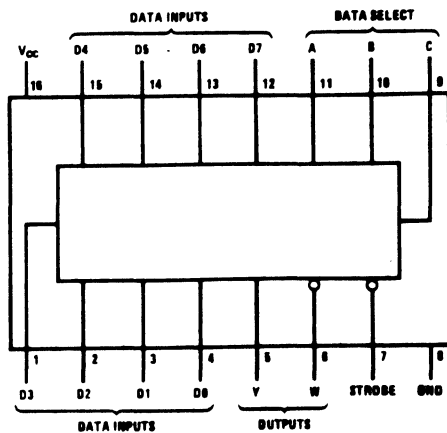


Figure 4-23. Decoder/Demultiplexer Connections

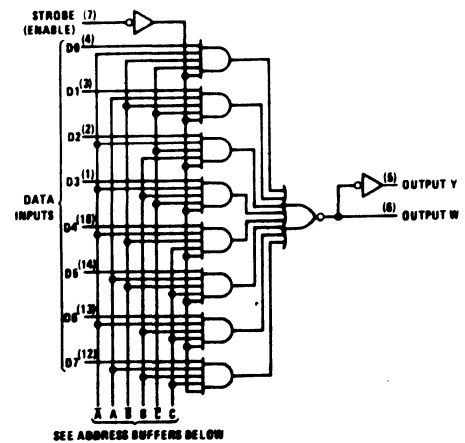
4.2.8 DATA SELECTOR/MULTIPLEXER (AM-410-1, U13).

This data selector/multiplexer contains full on-chip decoding to select one of eight data sources. A strobe input must be at a low logic level to enable the device. A high level at the strobe forces the W output high and the Y output low. See Figure 4-24 for logic and connections.

Connection Diagram



Logic Diagram



Truth Table

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D6	$\overline{D6}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
 $\overline{E0}, \overline{E1} \dots \overline{E7}$ = the complement of the level of the respective E input
 $\overline{D0}, \overline{D1} \dots \overline{D7}$ = the level of the respective D input

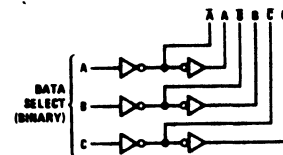
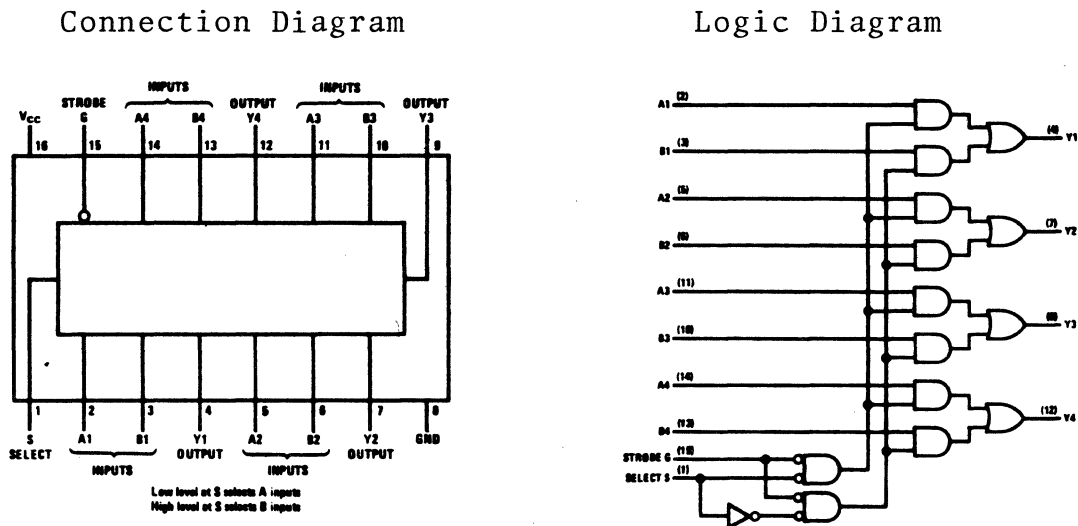


Figure 4-24. Data Selector/Multiplexer Logic and Connections

4.2.9 QUAD TWO-LINE TO ONE-LINE DATA SELECTOR/MULTIPLEXER (AM-410-2, U23, U43).

This data selector/multiplexer contains drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A four-bit word is selected from one of two sources and is routed to the four inputs. For logic and connections see Figure 4-25.



Truth Table

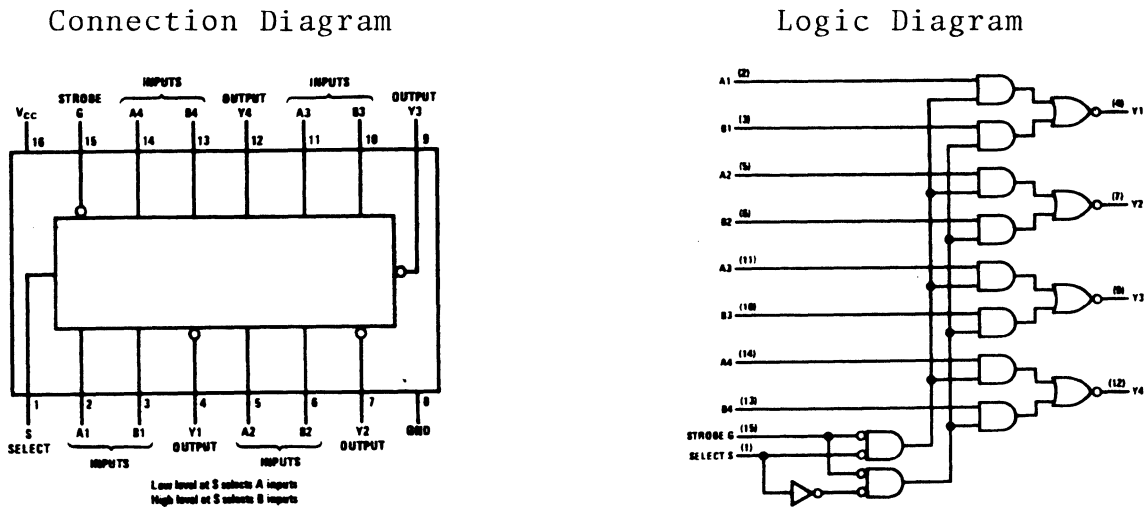
STROBE	INPUTS		OUTPUT Y
	SELECT	A B	
H	X	X ¹ X	L
L	L	L X	L
L	L	H X	H
L	H	X L	L
L	H	X H	H

H = High Level, L = Low Level, X = Don't Care

Figure 4-25. Quad 2-Line to 1-line Data Selector/Multiplexer Connections

4.2.10 QUAD INVERTING TWO-LINE TO ONE-LINE DATA SELECTOR/
MULTIPLEXER (AM-410-1, U18, U19).

This data selector/multiplexer contains inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A four-bit word is selected from one of two sources and is routed to the four inputs. For logic and connections see Figure 4-26.



Truth Table

STROBE	SELECT	INPUTS		OUTPUT Y
		A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High Level, L = Low Level, X = Don't Care

Figure 4-26. Quad Inverting 2-Line to 1-Line Data Selector/Multiplexer Connections

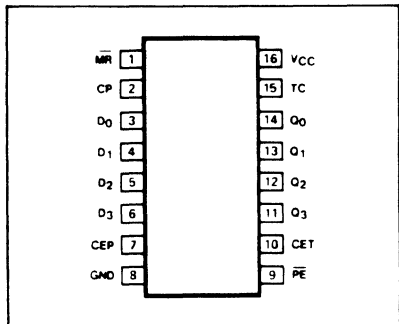
4.2.11 FOUR-BIT BINARY COUNTER WITH ASYNCHRONOUS CLEAR (AM-410-2, U34).

This device is a synchronous, presettable, 4-bit binary counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock.

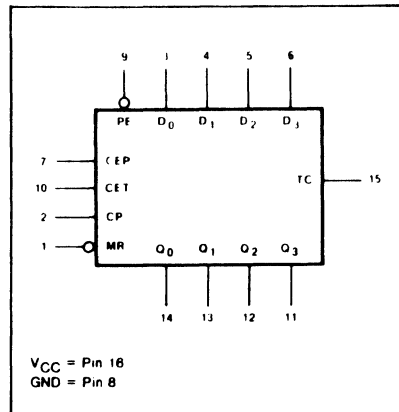
The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function is asynchronous. A LOW level on the Master Reset (\overline{MR}) input sets all four of the flip-flop outputs LOW, regardless of the levels of the CP, \overline{PE} , CET, and CEP inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET • CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled, will produce a HIGH output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This HIGH level TC pulse is used to enable successive cascading stages. For logic, connections, and timing, see Figure 4-27.

PIN CONFIGURATION



LOGIC SYMBOL



LOGIC DIAGRAM

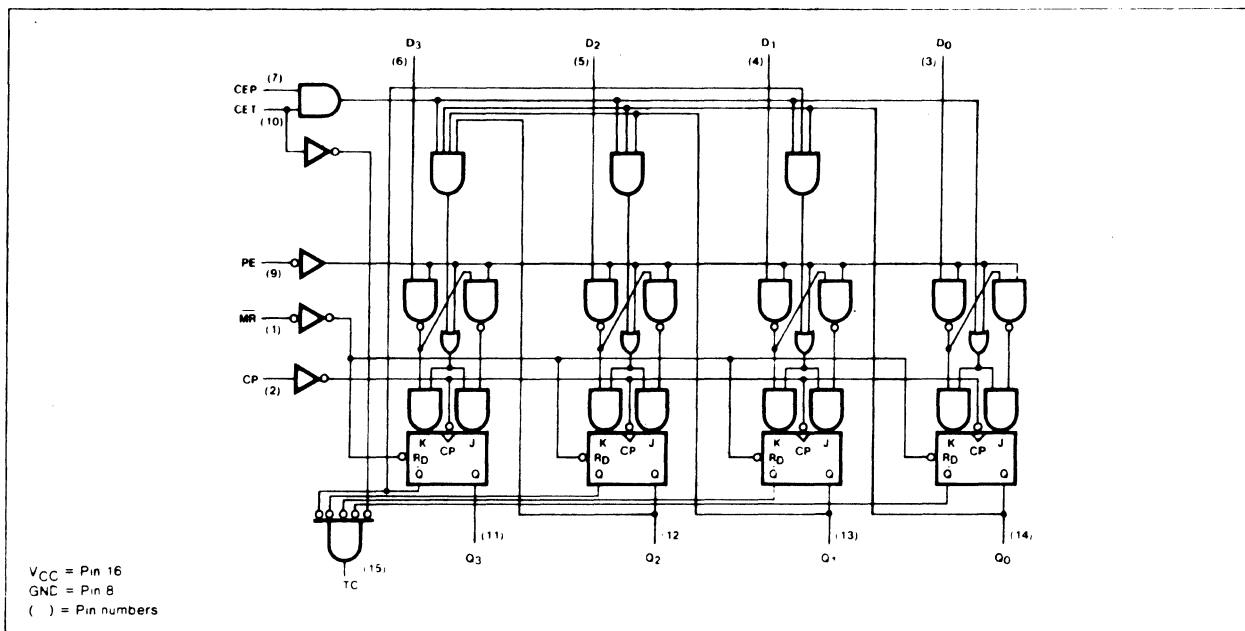


Figure 4-27 (SH1 of 2). Binary Counter with Asynchronous Clear Logic and Connections

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	MR	CP	CEP	CET	PE	D _n	Q _n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(b)
Count	H	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	H	X	l(c)	X	h(d)	X	q _n	(b)
	H	X	X	l(c)	h(d)	X	q _n	L

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
 l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
 ↑ = LOW-to-HIGH clock transition

NOTES

- (b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (#### for "161")
- (c) The HIGH-to-LOW transition of CEP or CET on the 54/74161 should only occur while CP is HIGH for conventional operation
- (d) The LOW-to-HIGH transition of PE on the 54/74161 should only occur while CP is HIGH for conventional operation

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

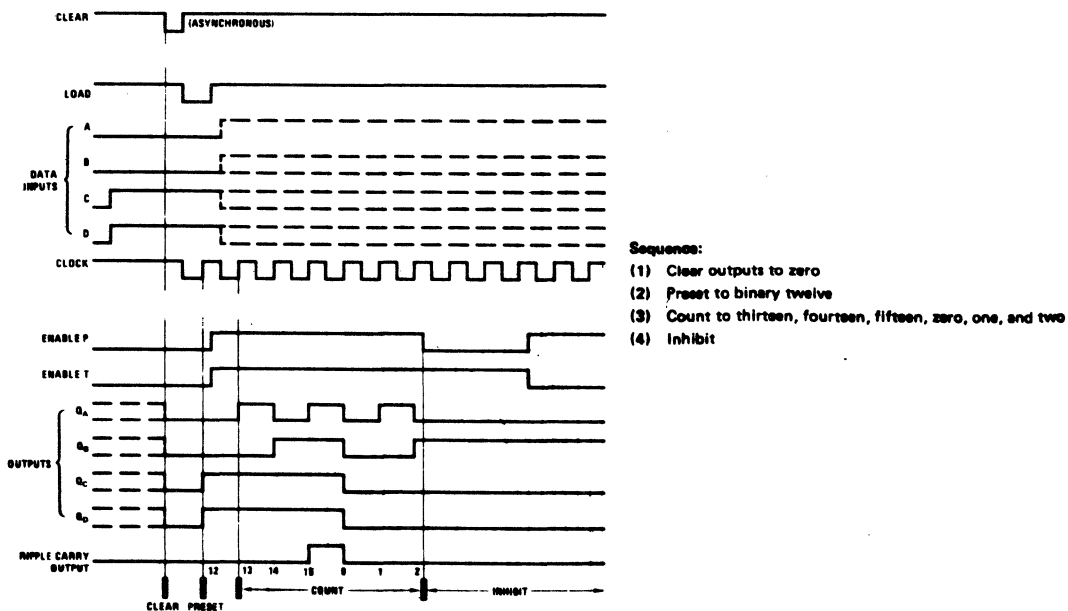


Figure 4-27 (SH2 of 2). Binary Counter with Asynchronous Clear Logic and Connections

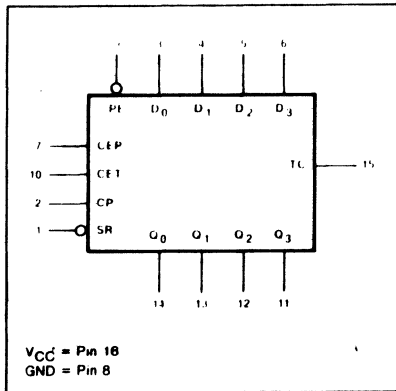
4.2.12 FOUR-BIT BINARY COUNTER WITH SYNCHRONOUS CLEAR (AM-410-2, U41).

This device is a synchronous presettable 4-bit binary counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the positive-going edge of the clock.

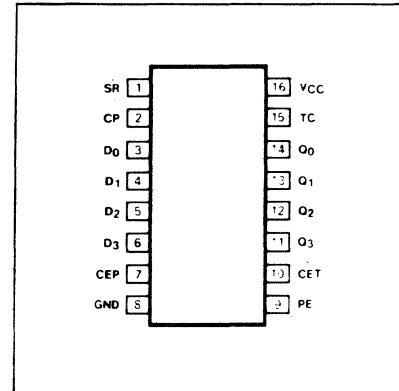
The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock, and takes place regardless of the levels of the count enable inputs. A LOW level on the Parallel Enable (\overline{PE}) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the clock. The reset (clear) function is synchronous with the clock. The Synchronous Reset (\overline{SR}), when LOW one setup time before the LOW-to-HIGH transition of the clock, overrides the CEP, CET, and \overline{PE} inputs, and causes the outputs to go LOW coincident with the positive clock transition.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs (CET - CEP) and a Terminal Count (TC) output. Both count enable inputs must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This HIGH level TC pulse is used to enable successive cascaded stages. For logic connections and timing, see Figure 4-28.

LOGIC SYMBOL



PIN CONFIGURATION



LOGIC DIAGRAM

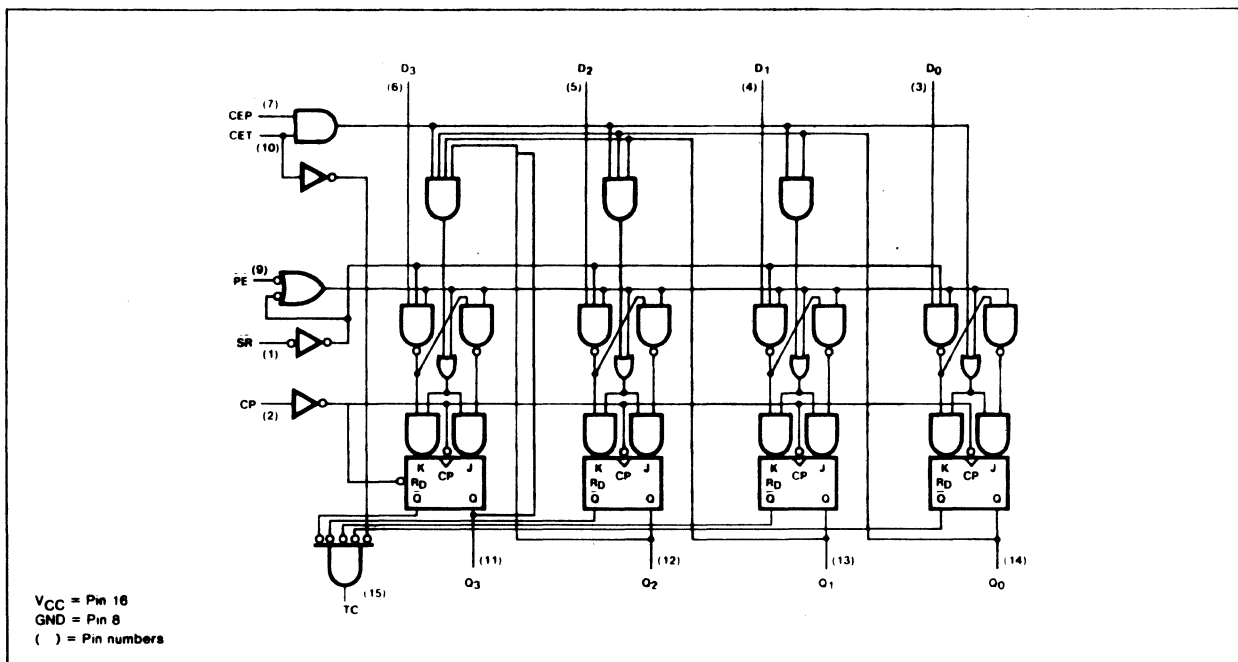


Figure 4-28 (SH1 of 2). Binary Counter with Synchronous Clear Logic and Connections

MODE SELECT - FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	\overline{SR}	CP	CEP	CET	\overline{PE}	D_n	Q_n	TC
Reset (Clear)	1	↑	X	X	X	X	L	L
Parallel Load	h(d)	↑	X	X	1	1	L	L
	h(d)	↑	X	X	1	h	H	(b)
Count	h(d)	↑	h	h	h(d)	X	count	(b)
Hold (do nothing)	h(d)	X	l(c)	X	h(d)	X	q_n	(b)
	h(d)	X	X	l(c)	h(d)	X	q_n	L

H = HIGH voltage level steady state.
 L = LOW voltage level steady state.
 h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
 1 = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
 X = Don't care.
 q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
 ↑ = LOW-to-HIGH clock transition

NOTES

- (b) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (#### for "163")
- (c) The HIGH-to-LOW transition of CEP or CET on the 54/74163 should only occur while CP is HIGH for conventional operation
- (d) The LOW to HIGH transition of PE or SR on the 54/74163 should only occur while CP is HIGH for conventional operation

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

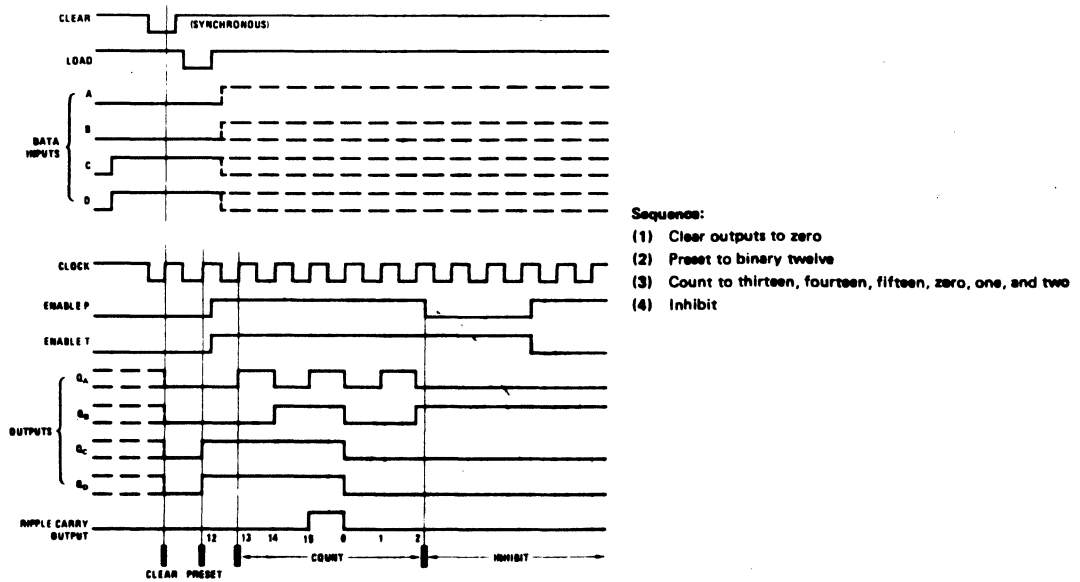
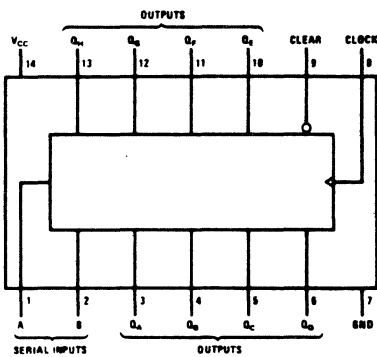


Figure 4-28 (SH2 of 2). Binary Counter with Synchronous Clear Logic and Connections

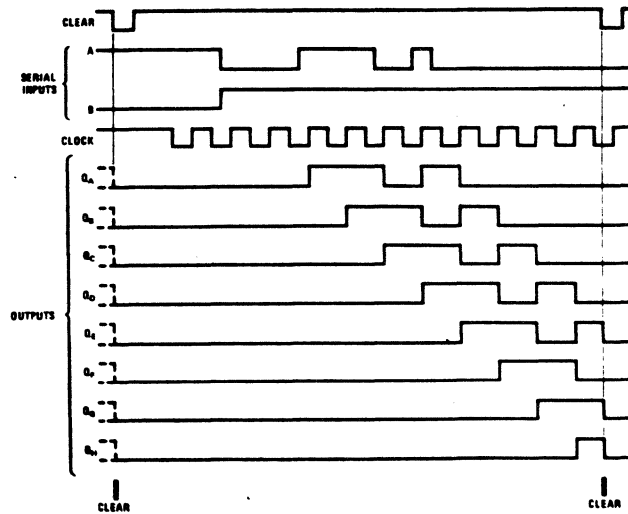
4.2.13 EIGHT-BIT SERIAL IN/PARALLEL OUT SHIFT REGISTER
(AM-410-2, U31).

This 8-bit shift register features gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects. For logic and connections see Figure 4-29.

Connection Diagram



Timing Diagram



Logic Diagram

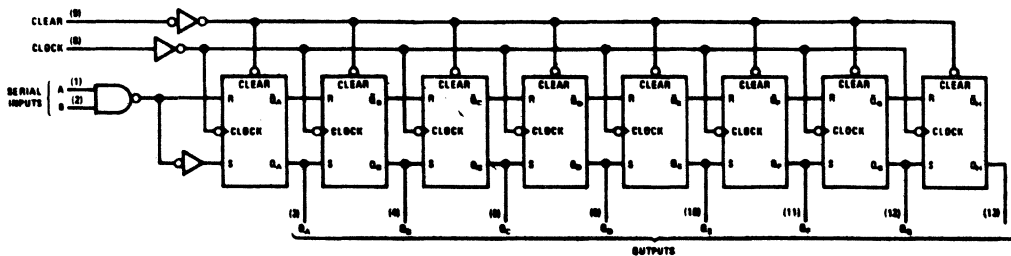
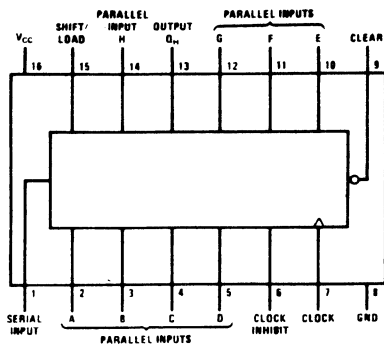


Figure 4-29. Eight-Bit Shift Register Logic and Connections

4.2.14 EIGHT BIT PARALLEL IN/SERIAL OUT SHIFT REGISTER
(AM-410-2, U25).

This parallel-in or serial-in, serial-out shift register features gated clock inputs and an overriding clear input. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. For logic and connections see Figure 4-30.

Connection Diagram



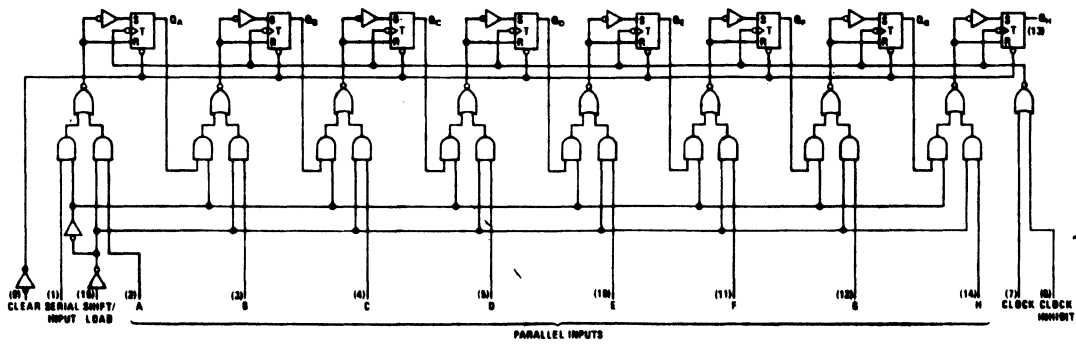
Truth Table

CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	INPUTS	INTERNAL OUTPUTS		OUTPUT
					PARALLEL A...H	Q _A	Q _B	Q _H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q _{A0}	Q _{B0}	Q _{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q _{A_n}	Q _{G_n}
H	H	L	↑	L	X	L	Q _{A_n}	Q _{G_n}
H	X	H	↑	X	X	Q _{A0}	Q _{B0}	Q _{H0}

H = High Level (steady state), L = Low Level (steady state)
 X = Don't Care (any input, including transitions)
 ↑ = Transition from low to high level
 a...h = The level of steady-state input at inputs A through H, respectively.
 Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B or Q_H, respectively, before the indicated steady-state input conditions were established.
 Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock

Figure 4-30. Eight-Bit Parallel In/Serial Out Shift Register
Logic and Connections (Sheet 1 of 2)

Logic Diagram



Timing Diagram

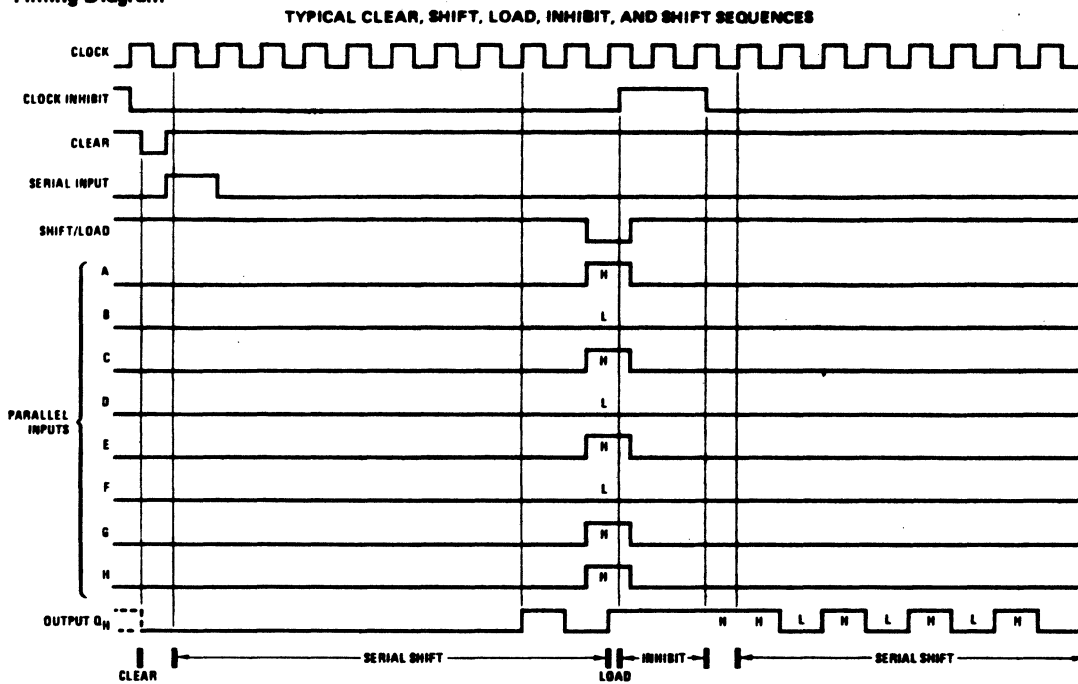
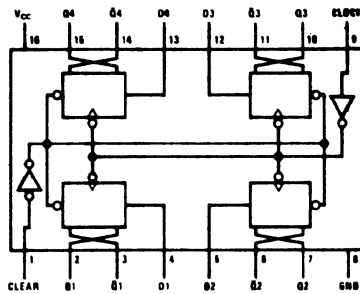


Figure 4-30. Eight-Bit Parallel In/Serial Out Shift Register
Logic and Connections (Sheet 2 of 2)

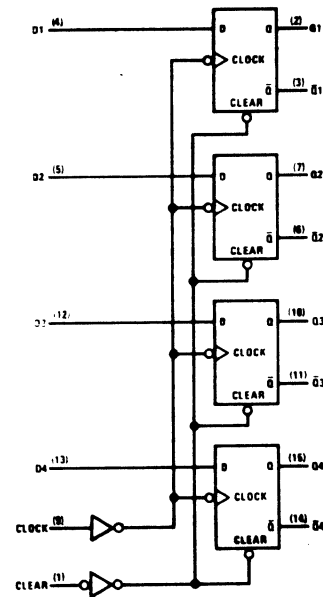
4.2.15 QUAD D FLIP-FLOPS WITH CLEAR (AM-410-2, U13, U19).

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. They feature a direct clear input and complementary outputs from each flip-flop. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For logic and connections see Figure 4-31.

Connection Diagram



Logic Diagram



Truth Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

H = High Level (steady state)
 L = Low Level (steady state)
 X = Don't Care
 ↑ = Transition from low to high level
 Q_0 = The level of Q before the indicated steady-state input conditions were established.
 † = 175, LS175, and S175 only

Figure 4-31. Quad D Flip-Flops With Clear, Logic and Connections

4.2.16 INVERTING TRI-STATE BUFFER (AM-410-1, U34).
 For logic and connections see Figure 4-32.

Connection Diagram

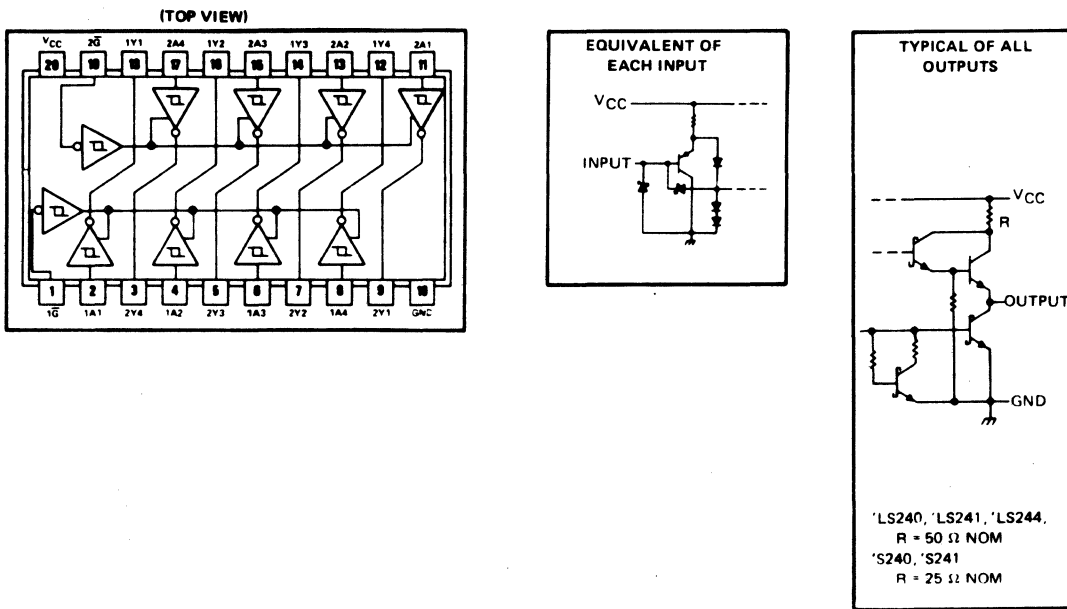
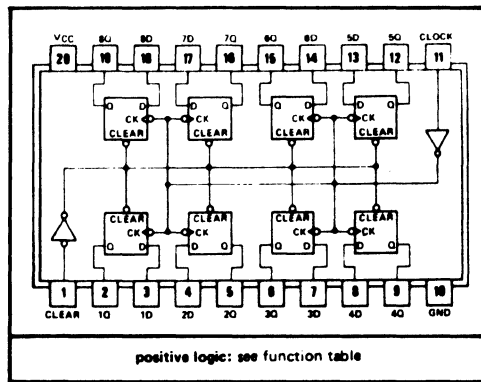


Figure 4-32. Inverting Tri-State Buffer
 Logic and Connections

4.2.17 OCTAL D-TYPE FLIP-FLOP WITH CLEAR (AM-410-1, U35).
 These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. For logic and connections see Figure 4-33.

Connection Diagram



Truth Table

(EACH FLIP-FLOP)			
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

Logic Diagram

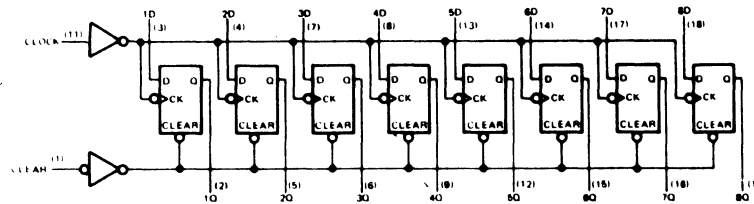
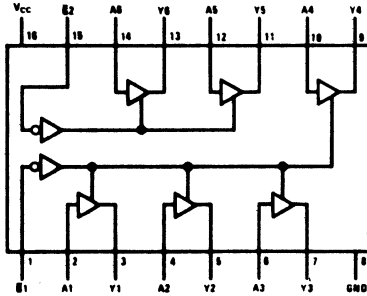


Figure 4-33. Octal D-Type Flip-Flop With Clear, Logic And Connections

4.2.18 TRI-STATE HEX BUFFERS (AM-410-1, U28; AM-410-2, U33).
 For logic and connections see Figure 4-34.

Logic and Connections

Truth Table



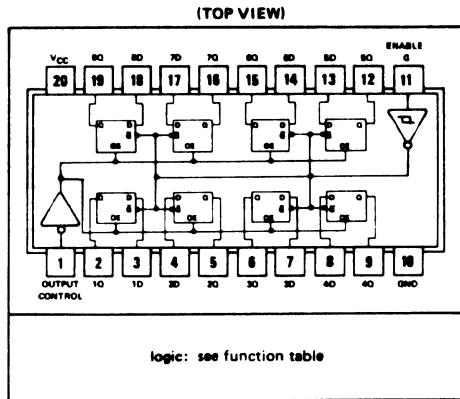
INPUTS		OUTPUT
\bar{G}	A	Y
H	X	Z
L	H	H
L	L	L

Figure 4-34. Tri-State Hex Buffer Logic And Connections

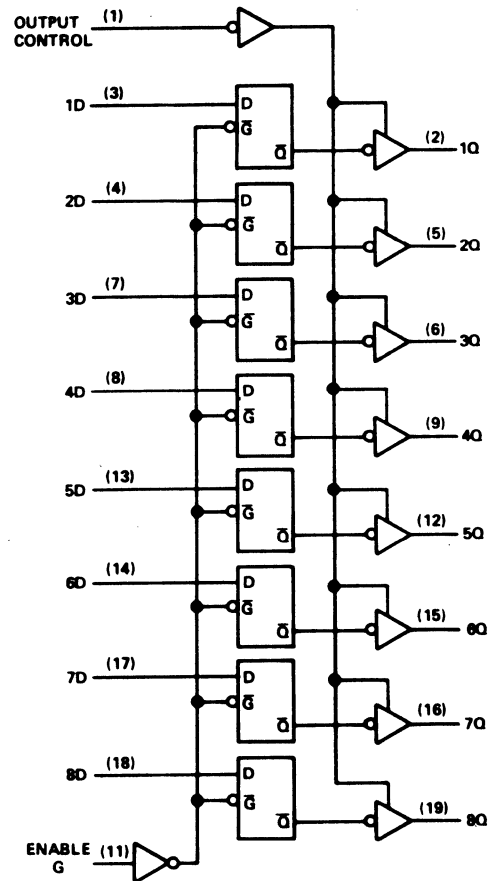
4.2.19 OCTAL D-TYPE TRANSPARENT LATCH (AM-410-1, U39).

This 8-bit register is a transparent D-type latch with three-state outputs. While the enable (G) is high, the Q outputs follow the data (D) inputs. When the enable is low, the output will be latched at the level of the data that was set up. For logic and connections, see Figure 4-35.

Connection Diagram



Logic Diagram



FUNCTION TABLE

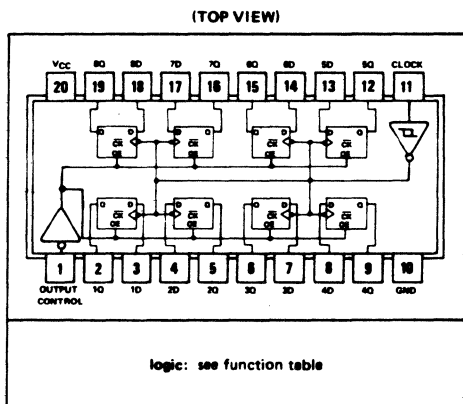
OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Figure 4-35. Transparent Latch Logic and Connections

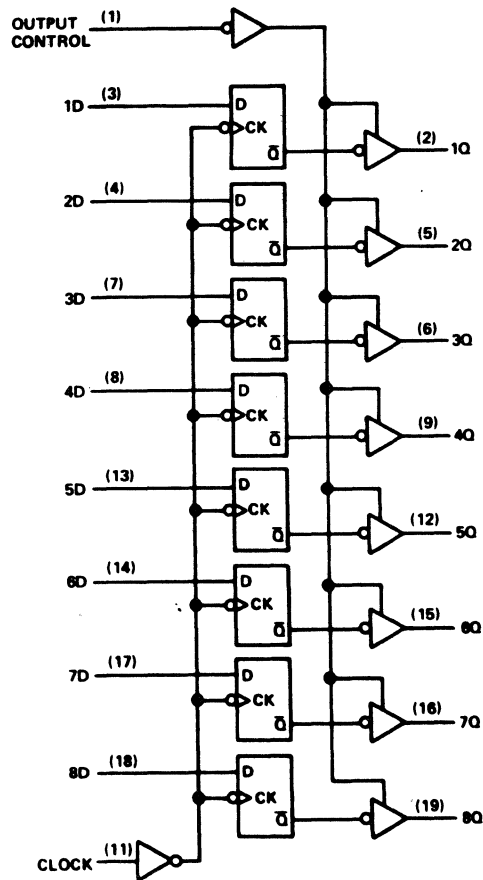
4.2.20 TRI-STATE D FLIP-FLOPS (AM-410-1, U37, U38, U40;
AM-410-2, U8, U12, U14, U18, U20, U24, U30).

These 3-bit registers contain D-Type flip-flops with totem-pole tri-state outputs capable of driving highly capacitive or low impedance loads. When the output control is taken to a high logic level, the outputs go into the high impedance state. When a low logic level is applied to the output control, data at the D inputs are loaded into their respective flip-flops on the next positive-going transition of the clock. For logic and connections see Figure 4-36.

Connection Diagram



Logic Diagram



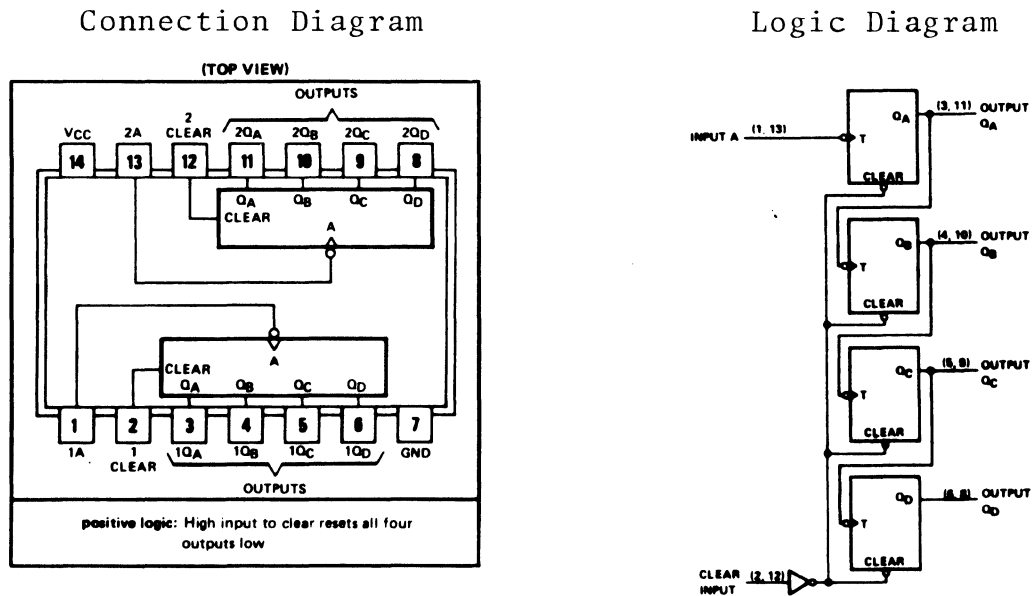
Truth Table

OUTPUT CONTROL	CLOCK	D	OUTPUT
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

Figure 4-36. Tri-State D Flip-Flop Connections

4.2.21 DUAL 4-BIT BINARY COUNTER (AM-410-2,U32).

These devices contain eight master-slave flip-flops and additional gating to implement two individual four bit counters in a single package, each with a clear and clock input. Parallel outputs are available from each counter so that any submultiple of the input count frequency is available. For logic and connections see Figure 4-37.



Truth Table

COUNT SEQUENCE
(EACH COUNTER)

COUNT	OUTPUT			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Figure 4-37. Four-Bit Binary Counter Connections

4.2.22 1024 X 4 BIT STATIC RANDOM ACCESS MEMORY (AM-410-1, U41, U42).

This device is a 4096-bit static Random Access Memory organized as 1024 words by 4 bits and requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided and a separate chip select (CS) lead allows easy selection of an individual package. For logic and connections, see Figure 4-38.

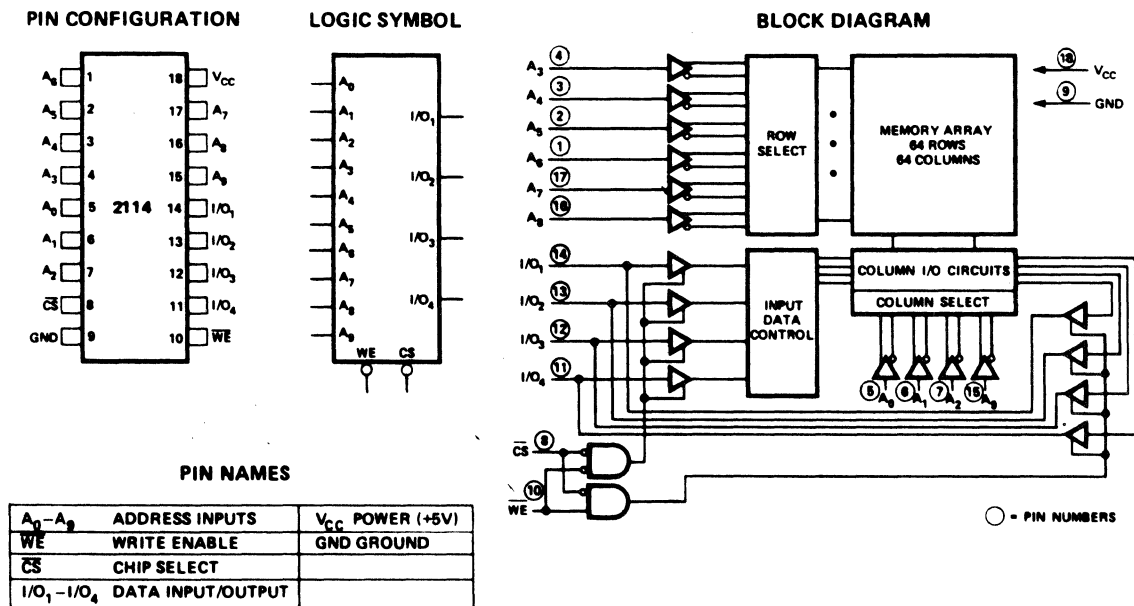
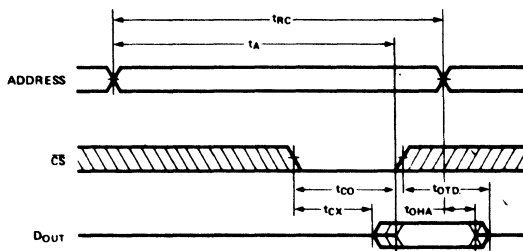


Figure 4-38. RAM Connections

WAVEFORMS

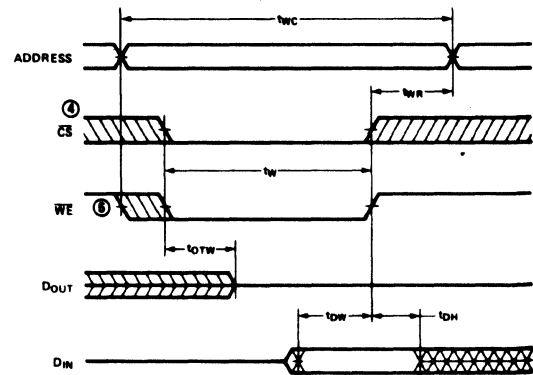
READ CYCLE ③



NOTES:

- ③ WE is high for a Read Cycle.
- ④ If the CS low transition occurs simultaneously with the WE low transition, the output buffers remain in a high impedance state.
- ⑤ WE must be high during all address transitions.

WRITE CYCLE



4.2.23 BUS COMPARATOR (AM-410-1, U27; AM-410-2, U26).

This device compares two binary words of two to six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are TTL inputs, whereas inputs of the second word are high impedance receivers driven by a terminated data bus. The output has a latch that is strobe controlled. The transfer of information to the output occurs when the STROBE input goes from a logical 1 to a logical 0 state. Inputs may be changed while the STROBE is at the logical 1 level, without affecting the state of the output. For logic and connections, see Figure 4-39.

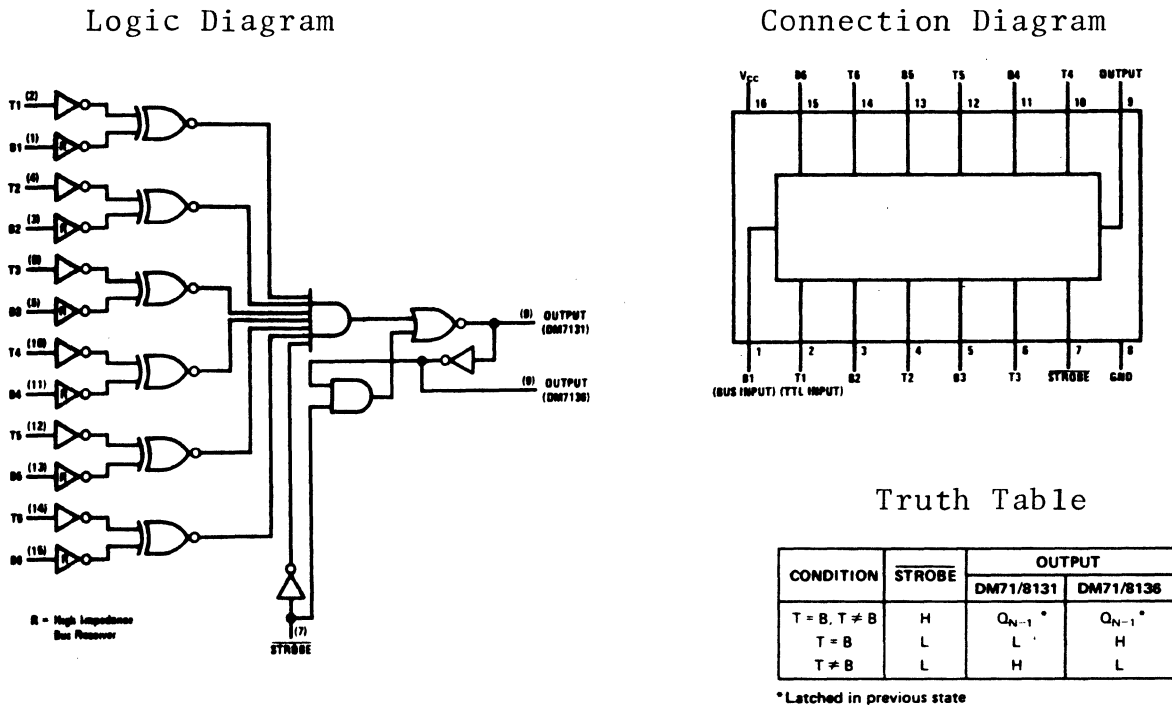
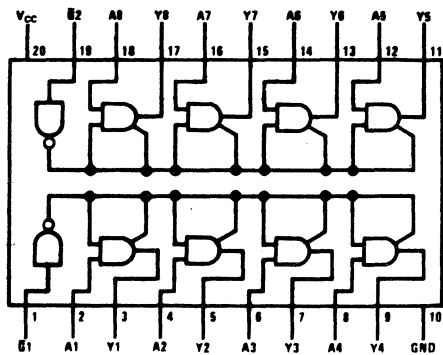


Figure 4-39. Bus Comparator Connections

4.2.24 TRI-STATE OCTAL BUFFERS (AM-410-1, U36; AM-410-2, U6). This device provides eight, two-input buffers and employs Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state, while the other input passes the data through the buffer with no inversion. Four buffers are enabled from one common line and the other four are enabled from another common line. The outputs are placed in the tri-state condition by applying a high logic level to the enable pins. For logic and connections, see Figure 4-40.

Logic and Connections



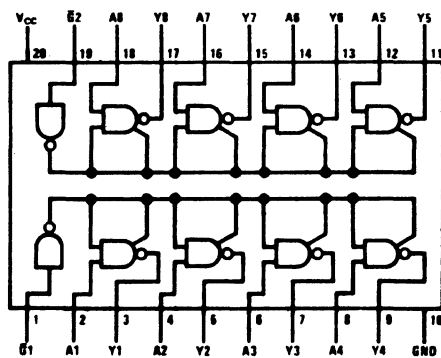
Truth Table

INPUTS		OUTPUT
\bar{G}	A	Y
H	X	Z
L	H	H
L	L	L

Figure 4-40. Tri-State Octal Buffer Logic and Connections

4.2.25 TRI-STATE INVERTING OCTAL BUFFERS (AM-410-2, U36). This device provides eight, two-input buffers and employs Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high impedance state, while the other input passes the data through the buffer with a logical inversion. Four buffers are enabled from one common line and the other four are enabled from another common line. The outputs are placed in the tri-state condition by applying a high logic level to the enable pins. For logic and connections, see Figure 4-41.

Logic and Connections



Truth Table

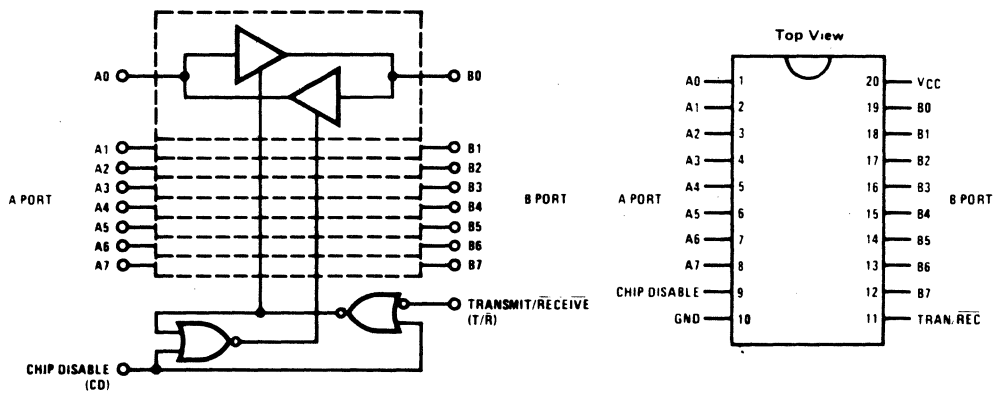
INPUTS		OUTPUT
\bar{G}	A	Y
H	X	Z
L	H	L
L	L	H

Figure 4-41. Tri-State Inverting Octal Buffers Logic and Connections

4.2:26 BIDIRECTIONAL TRANSCEIVER (AM-410-1, U43).

This device is a Schottky device that provides bidirectional drive for bus oriented microprocessor systems. Transmit/Receive inputs determine the direction of logic signals through the device. The Chip Disable input disables both A and B ports by placing them in a tri-state condition. For logic and connections, see Figure 4-42.

Logic and Connection Diagrams



Logic Table

Inputs		Resulting Conditions	
Chip Disable	Transmit/Receive	A Port	B Port
0	0	OUT	IN
0	1	IN	OUT
1	X	TRI-STATE	TRI-STATE

X - Don't Care

Figure 4-42. Bidirectional Transceiver Logic and Connections

SECTION 5 MAINTENANCE AND TROUBLESHOOTING

5.0 INTRODUCTION.

The AM-410 circuit board set performs to full capability with a minimum of maintenance. This section describes maintenance and troubleshooting procedures and procedures for handling warranty returns.

5.1 CIRCUIT BOARD CHECKOUT.

The AM-410 circuit board set was fully tested before it left Alpha Microsystems and will operate satisfactorily in the system if the hardware and software requirements of Sections Two and Three of this manual are met. Should a problem arise, use the following procedures to identify and locate the fault.

1. Check all cables for proper seating of connectors. The daisy chain cable terminator in the Phoenix (the second plug in the Phoenix card one) can be inserted one row off. Ensure that it is installed correctly.
2. Check each of the wires at the cable connectors to ensure that each wire is properly seated in its groove.
3. Check the gray radial cable to ensure that the edge wires (not the ground plane) are not frayed and making only intermittent contact.
4. Check the cables at the bottom of the card cage to ensure that they have not become loose during shipping.

5. Check the circuit boards for proper seating in the slot.
6. Check the Hash totals on the latest operating system.
7. Check all power connections for correct voltages.
8. Check jumper options to ensure correctness of application. These include boot jumper and interrupt jumper on AM-100.
9. Verify that the fault is in the AM-410 and not either in the system or in the peripherals. This can best be accomplished with substitution of a known good circuit board.
10. Perform the diagnostic tests included with the circuit board as described in paragraph 5.3.

5.2 WARRANTY PROCEDURES.

This circuit board is covered by warranty issued by Alpha Microsystems Inc., Irvine, California. Complete details of the warranty are included with the circuit board. Should a problem arise with this circuit board, call your dealer or the Alpha Micro International Support Services Group for information.

5.3 TROUBLESHOOTING PROCEDURES.

Diagnostic testing software is included with the AM-410 circuit board set and should be used for troubleshooting and to verify proper operation. The diagnostic consists of a main program with a series of overlays to perform the specific tests. The test routines are as follows:

1. Communications and Memory Test - MEM410.OVR
2. Positioning Test - POS410.OVR
3. Data Transfer Test - DAT410.OVR
4. Interrupt Circuitry Test - INT410.OVR
5. All Tests
6. Alignment Test - ALN410.OVR

Each of these tests may be run independently or all tests run consecutively. To select the desired test, query the main menu and enter the number of the desired test.

These tests exercise the abilities of the AM-410 to receive and execute non-disk commands and move data back and forth to the RAM buffer. With the completion of all four phases of testing, over 521,000 transfers have taken place between the S-100 Bus and the AM-410 circuit board set. The test results are as follows:

1. If test one fails, it displays an error message and aborts the test.
2. If test two fails, it displays an error message and continues.
3. If test three fails, it displays an error message and continues.
4. As test four runs, it displays a running tally of the number of passes and total error count. If the error count reaches 32,000, the test aborts and an error message is displayed.

This diagnostic is a stand alone test and does not require a resident disk driver. Because of this restriction, it must be the only thing accessing the AM-410 and disk drive.

5.3.1 COMMUNICATIONS AND MEMORY TEST.

The Communications and Memory Test consists of the five subtests listed below which are displayed in the menu.

1. Communications Test
2. Write 00 Byte Test
3. Write FF Byte Test
4. Write incrementing Byte Test
5. Run All Tests

To run the Communications and Memory Test, select choice one in the AM-410 main menu. The Communications and Memory Test menu is then displayed for selection of the desired testing. The five subtests are described in the following paragraphs.

Communications Test. This subtest attempts to communicate with the AM-410 and aborts if unsuccessful.

Write 00 Byte Test. This subtest writes a zero byte to the first location of AM-410 RAM.

Write FF Byte Test. This subtest writes an FF byte to the first location of AM-410 RAM.

Write Incrementing Byte Test. This subtest writes an incrementing byte pattern into the AM-410 RAM starting at zero and incrementing through for 255 passes. At completion of this test, every byte has been exercised with every bit pattern. The last two locations of RAM are not written to since the on-board CPU is in a call and writing here would destroy the stack.

This test checks the RAM addressing circuitry and DMA circuitry since a total of 521,220 reads and writes are

made to the AM-410.

Run All Tests. This runs all the above tests.

5.3.2 POSITIONING TEST.

This test exercises the disk positioning circuitry and the ability of the disk drive to respond in the proper manner to both legal and illegal commands. To run this test, select the positioning test from the main menu and the menu for this test will be displayed. The Positioning Test consists of the following subtests which are displayed in the menu:

1. Restore the Drive
2. Test Illegal Cylinder
3. Sequential Seek to All Cylinders
4. Random Seek (Timed)
5. Alternating Seeks
6. Overlapped Seeks
7. All Tests

Each test can be run independently or all tests run consecutively (choice 7). All of the tests provide an error message that gives the type of AM-410 error associated with the failure. For All Tests, the default time for test four is ten minutes.

Restore the Drive Test. This subtest performs RESTORE on the user selected drive.

Test Illegal Cylinder. This subtest forces an illegal cylinder condition and reports the failure of the drive.

Sequential Seek to All Cylinders Test. This subtest seeks forward to the maximum cylinder and back to cylinder zero and reports all normal disk errors.

Random Seek (Timed). This subtest performs random seeks for a user specified time period in minutes of not greater than 20 hours.

Alternating Seeks Test. This subtest seeks from cylinder zero to the maximum cylinder, decrementing by one each time until maximum cylinder reaches zero and then seeks back out incrementing by one.

Overlapping Seeks Test. This subtest seeks between two counts; one decrementing and the other incrementing.

All Tests. This mode runs all tests sequentially. The Random Seek Test runs for ten minutes.

This test inquires for the drive number in a range of 0-23. The low drive number is the cartridge in each group of drive numbers. 0-5 is unit zero, 6-11 is unit 1, 12-17 is unit 2, and 18-23 is unit 3.

5.3.3 DATA TRANSFER TEST.

This test exercises the AM-410 and disk drive read/write circuitry. Testing begins with simple read/write tests and progresses to more complex operations. The Data Transfer test consists of the following subtests which are displayed in the menu:

1. Read/Write Test
2. Head Select Test
3. Sequential Write Test
4. Random Write/Read Test
5. Worst Case Peak Shift Data
6. Worst Case One Bit Shift Data
7. High Amplitude, Low Frequency Data
8. Low Amplitude, High Frequency Data
9. All Tests

Each test can be run independently or all tests run consecutively (choice 9). All of the tests provide an error message which gives the type of error encountered. In All Tests, the default time to run tests four through eight is ten minutes.

Read/Write Test. This subtest writes and reads to cylinder zero, sector zero of a user selected disk.

Head Select Test. This subtest reads data from every head of a selected unit to verify that data can be read.

Sequential Write Test. This test writes cylinder number to sector zero of each cylinder, restores and reads to verify operation.

Random Write/Read Test. This subtest seeks to a random cylinder and sector on a user selected drive and writes random data. Another random write/read sequence is performed and then the test returns to the last one to verify the data, then returns to the second cylinder and sector to verify the data. The test runs for a user selected time period.

Worst Case Peak Shift Data Test. This subtest performs the same testing as the Random Write/Read test except it uses the data pattern 1463 octal.

Worst Case One Bit Shift Data Test. This subtest performs the same testing as the Random Write/Read Test except it uses the data pattern 34716 octal.

High Amplitude, Low Frequency Data Test. This subtest performs the same testing as the Random Write/Read test except it uses all zeros as data.

Low Amplitude, High Frequency Data Test. This subtest performs the same testing as the Random Write/Read test except it uses 17777 octal as data.

All Tests. This selection runs all tests in sequence. All timed tests default in ten minutes.

5.3.4 INTERRUPT CIRCUITRY TEST.

This is a test of the AM-410 interrupt circuitry. A non-disk command generates an interrupt and the test checks for proper handling of the interrupt. Test four in the main menu selects this test and a RETURN must be typed before the test will proceed. Test results are either a pass or fail response.

5.3.5 ALL TESTS.

This selection runs all tests in sequence. The drive number must be entered for the test to proceed and all timed tests are set to default in ten minutes.

5.3.6 ALIGNMENT TEST.

This test simulates the use of a field test unit for use as an alignment aid. The two functions performed are as follows:

1. Allows the user to seek between two cylinders on a user selected device.
2. Seeks to a user selected cylinder on a user selected drive and turns on read gate.

See paragraph 5.4 for complete alignment procedures.

5.3.7 TEST MODIFICATIONS.

Some of the parameters of this program may be changed at the user's option. These parameters with their offsets from the program base are described in the following paragraphs. All offsets are in octal.

PORT. Base + 4. Set to 177720 (octal) for standard interface.

TIMDEL. Base + 14. This is the number of real time clock pulses of wait time before abortion of a command sequence to the AM-410 when there is no acknowledgment. This is normally set to 60 decimal.

TIMER. Base + 16. This is the number of minutes to run timed tests in All Tests mode. The timer works properly for 50 or 60 Hz systems. It is normally set to ten decimal.

VEC. Base + 20. Interrupt vector of board under test. Normally set to two decimal.

5.4 CARTRIDGE MODULE DRIVE (CMD) ALIGNMENT PROCEDURE.

This section describes the procedure which should be used to align the heads of the Cartridge Module Drive (CMD) and describes the operation of some of the equipment used. For additional information on the CMD, refer to the Control Data Corp. hardware maintenance manual no. 75888415.

CAUTION

The maintenance manual specifically instructs field personnel to utilize correct tools and procedures when performing "Head Arm Alignment." The following steps should be taken to prevent any further head arm or alignment tool damage due to unfamiliarity.

- A. Read and understand the "Head Arm Alignment" procedure as explained in the maintenance manual.
- B. Use only the specified alignment tool and calibrated torque screwdriver/bit.
- C. Ensure the alignment tool is clean and free of damage.
- D. Ensure the head mounting screws are tightened to the specified torque requirement. (Damage to the tool or head arm can occur if adjustment is attempted on a head that has been tightened in excess.)
- E. When inserting the adjustment tool, locate the head arm slot with the tip of the tool prior to applying any turning force.
- F. When turning the adjustment tool, enough inward force should be applied on the tool to prevent the tip of tool from disengaging from the adjustment slot.

NOTE

"Rounding-out" of the head arm adjustment slot prevents further adjustment of that particular head and may ultimately require replacement. Steps D, E and F are especially intended to prevent "Rounding-out" of the head arm adjustment slot and/or damage to the adjustment tool.

Any change in initial position of the fixed disk module servo head affects the alignment of all the fixed disk module data heads. Since there are no alignment tracks on or available to the fixed disk module data heads, the heads are not normally adjusted. However, should it be necessary to align one or

more of the fixed disk module heads after the initial alignment, a procedure is given at the end of this section which describes the means of realignment of a fixed disk module servo or data head, though it is more involved than the normal procedure.

Head alignment on the CMD requires an alignment extender PWA to adapt the CMD Head Alignment PWA (AZPV) for use with the CMD electronics module. The AZPV Head Alignment PWA operates as described in the following paragraphs.

The specific procedures contained in the following paragraphs are as follows:

- A. Initial Head Alignment Procedure.
- B. Cartridge Read/Write Data Head Alignment Procedure.
- C. Cartridge Servo Head Alignment Procedure.
- D. Fixed Disk Module Data Read/Write Head Alignment Procedure.
- E. Fixed Disk Module Servo Head Alignment Procedure.

5.4.1 EQUIPMENT REQUIRED.

- A. CE Cartridge (P/N 76204400)
- B. AM-410 Alignment Software
- C. Extender Board (P/N 75886001)
- D. Alignment Board (P/N 54285300)
- E. Cable 8-Pin (P/N 77612337)

- F. Cable-Head Alignment (P/N 75882394)
- G. Oscilloscope-Techtronix 465 or Equivalent
- H. DVM (Used as a nullmeter)
- I. Head Alignment Tool (P/N 75893963)
- J. Torque Wrench with Hex Bit

5.4.2 GENERAL CMD ALIGNMENT PRINCIPLES.

NOTE

Each CMD is aligned at the factory and should not need any additional alignment at the customer site. Due to the differences in CE cartridges, thermal stability and mechanical tolerances, it is possible to exceed the standards of this procedure when checking alignment with a different CE cartridge--in other words, one other than the one with which the original alignment was made. The only time alignment would become necessary is if data recovery becomes a problem (data errors or seek errors). Alignment should then be accomplished as per this procedure to minimize these accumulative differences.

In general, the head alignment is accomplished on all heads by first mechanically aligning each of the fixed disk module heads when the module is first installed. Figure 5-1 shows how the oblong slot in the side of the head arm is "eyeball" aligned in the center of the round hole 5 in the carriage. An RTZ command then positions the fixed servo head on track zero, and with that carriage position as a reference, the

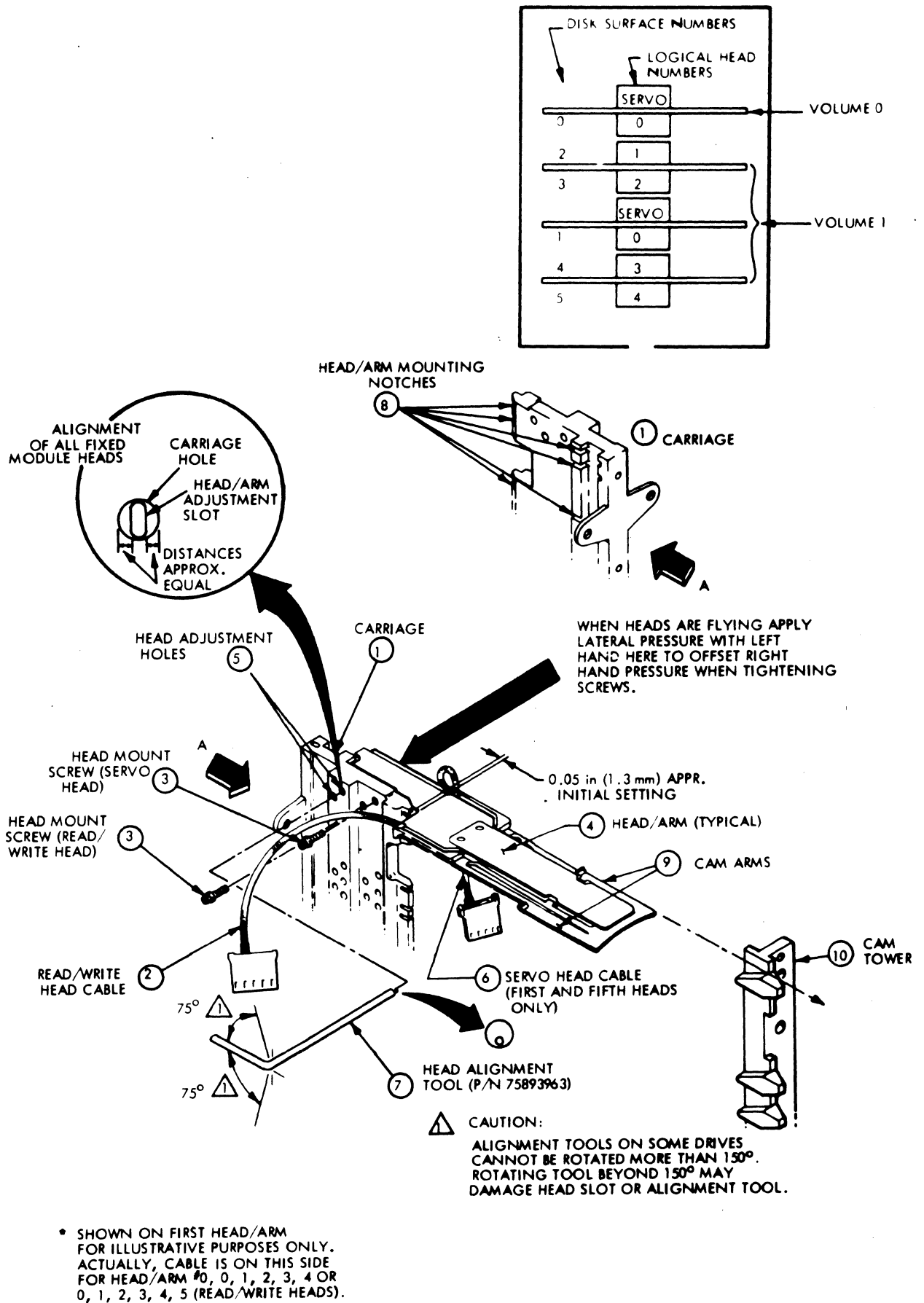


Figure 5-1. Head/Arm Removal and Replacement and Alignment

cartridge head is aligned. If only the two cartridge heads need to be aligned, the fixed servo head is positioned to track zero and the cartridge servo head aligned. Once the cartridge servo head is aligned, it is used as a reference for aligning the cartridge data head. Once this alignment is made, only the cartridge heads are normally aligned after that.

The Head Alignment Printed Wiring Assembly (PWA) (called AZPV hereafter) develops an alignment voltage derived from a voltage the Servo and Read/Write Preamplifiers produce from read head signals. When reading from a CE cartridge, the voltage from the AZPV PWA will be proportional to the distance that the cartridge servo (or data) head is offset from the track centerline. The drive actuator should have been positioned to the track zero centerline as defined by the fixed disk module servo head when aligning the cartridge servo head, or to the centerline as defined by the cartridge servo head when aligning the data head. Measure the voltage proportional to the offset produced by the AZPV PWA as shown in Figure 5-2.

There are three toggle switches on the AZPV PWA which control the AZPV PWA operation. These are shown in Figure 5-2, and their operation is described below:

- S1. This switch changes the polarity of the alignment voltage produced on the AZPV. This switch is used when null meter readings are taken for the purpose of calculating the offset of the head being aligned.

- S2. This switch selects the head output which will be used as an input to AZPV. Position S selects the tracking servo head as an input to the AZPV.

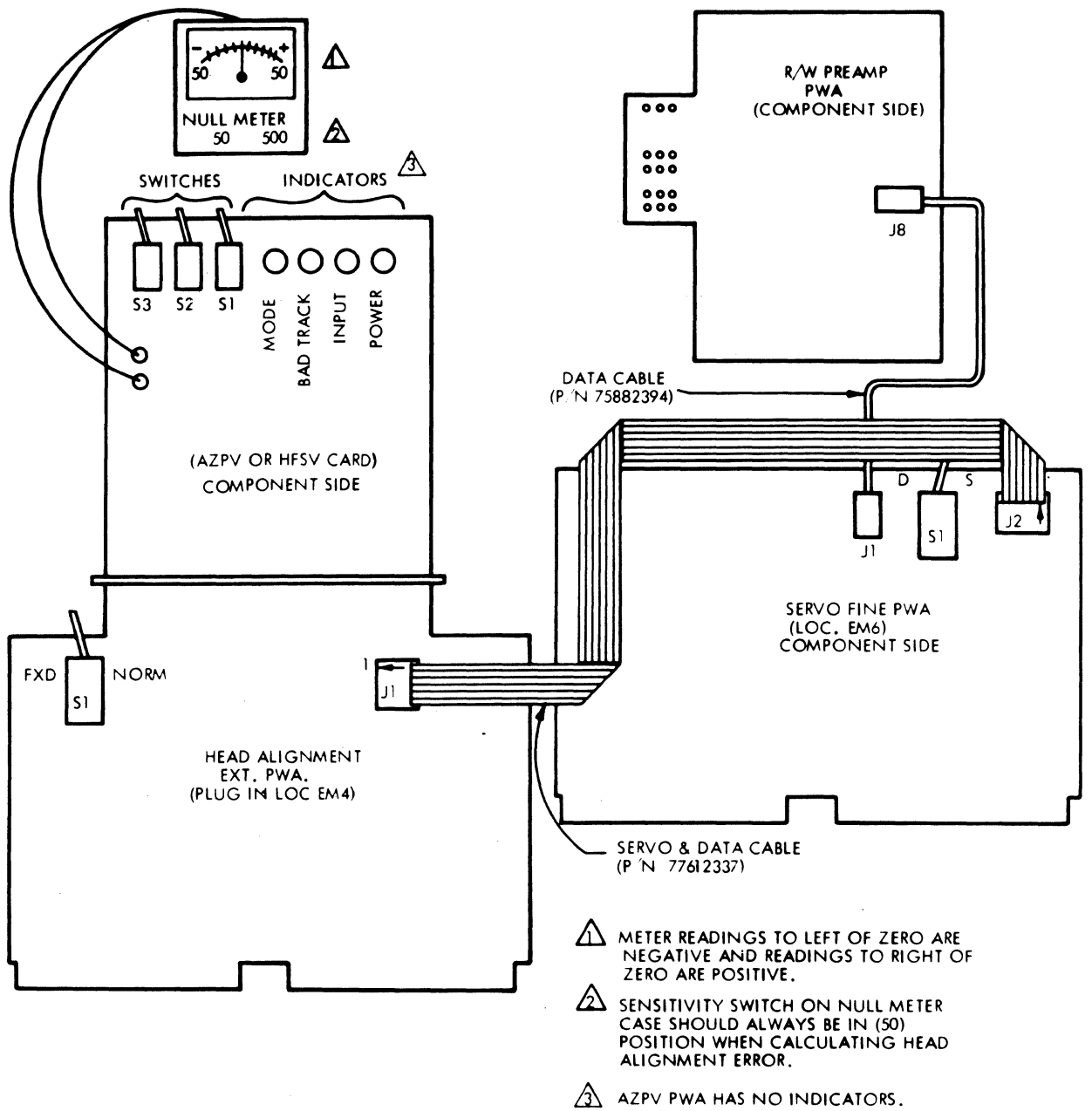


Figure 5-2. Head Alignment Block Diagram

(The tracking servo head is the one selected by S1 on the Head Alignment Extender PWA.) Position R/W selects whichever of the cartridge heads (servo or data) have been selected by the BUS OUT interface lines or by the S1 on the Servo Fine PWA located in EM6.

- S3. This switch selects the sensitivity range of the AZPV. In the X.1 position, the alignment voltage is attenuated by a factor of 10. Head alignment error cannot be accurately measured with S3 in this position. In the X1 position, the alignment voltage is not attenuated and the head alignment error can be accurately measured.

NOTE

Head alignment is required on a new drive before leaving the factory, when a used drive has a fixed disk module replaced, and when any of the drive servo or data heads are replaced. If a head replacement is required because of contact between the disk and the head, the disk module involved should also be replaced, as a new head would not fly over a damaged disk.

5.4.3 INITIAL HEAD ALIGNMENT PROCEDURES.

The following is a description of the initial head alignment procedure; that is, the procedure to be used when aligning the heads for the first time on a new unit or when the fixed disk module is replaced.

1. Operate the START switch to the STOP position to stop the drive motor. Wait until the drive motor has stopped (when the READY indicator has stopped blinking).

2. Set AC circuit breaker on the rear of the unit to OFF position.
3. Install the CE cartridge (P/N 76204400) and activate the write protect switches located on the operator control panel.
4. Remove the case cover assembly.
5. Install the AZPV Head Alignment PWA (P/N 54226509) into the Head Alignment Extender PWA (see Figure 5-2) and install the entire assembly in the electronics module location EM4.
6. Install the two head alignment cables between the Head Alignment Extender PWA, the Servo-Fine PWA (located in EM6), and the Read/Write Preamp PWA as illustrated in Figure 5-2.

NOTE

Make sure the arrow on the connector head lines up with pin 1 of both connectors, J1 and J2 on the Head Alignment Extender PWA, and J2 on the Head Alignment Extender PWA and the Servo-Fine PWA.

7. Set switch S1 on the Head Extender PWA to FXD position.
8. Connect the null meter leads to test points Z and X on the AZPV PWA (red wire to +).
9. Refer to the AM-410 Diagnostic Documentation (Alignment Section). Also, ensure that the diagnostic software is on the systems disk.

10. Connect oscilloscope to ground and dibit test points (marked READ SIGNAL) on the Head Alignment PWA AZPV.
11. Remove screws which secure the electronics module to the hinge bracket and carefully lift the module directly up and slowly swing it out to the side and leave it in the rest position.

CAUTION

Use only head alignment tool #75893963 (7 in Figure 5-1). Use of a different tool can cause permanent damage to head/arm and carriage.

12. Inspect head adjustment tool for damage (nicks, scratches, etc.) at adjustment end. End should have a polished surface where it enters the carriage. Polish end with crocus cloth if aluminum deposits are present and wipe clean. Do not use emery cloth, sandpaper, paper, or files which can permanently damage tool and subsequently damage heads and carriage holes. Do not use a defective tool. Repair or replace tool if damage exists.

NOTE

Use care when using the head alignment tool (refer to Figure 5-1). The tool should slip easily through the alignment hole (in the carriage) and into the slot in the head/arm. When adjusting the head, the tool should turn freely in the hole. If anything more than a small amount of force is required to adjust the head/arm,

the tool is probably binding in the hole
(in the carriage).

13. Center the alignment slot of all heads (read/write, data and servo) associated with the fixed disk module (see 5 in Figure 5-1).

NOTE

While torquing the head clamping screws (see 3 in Figure 5-1), use only a straight Allen wrench and keep it as perfectly aligned as possible with head mounting screw. If care is not taken during this operation, head/arm may be pushed out of alignment.

14. Torque all fixed pack head clamping screws to $12 \pm \frac{1}{2}$ lb-in (1.26 to 1.38 Nm) while observing the centering (see Figure 5-1).
15. Torque the head clamping screws of the removable cartridge heads to $4 \pm \frac{1}{2}$ lb-in (0.40 to 0.51 Nm).
16. Set AC power circuit breaker to ON.
17. Press START switch to start drive motor and load heads.
18. Perform thermal stabilization: Allow drive to run with heads loaded for a minimum of 60 minutes. If head/arm alignment check is being performed on more than one drive, the CE disk pack needs only a 15 minute purge per drive after head/arm alignment check has been performed on the preceding drive (provided drive under test has been running for 60 minutes immediately preceding check).

CAUTION

Make certain that no electrical conductors, such as the carriage locking tool, head alignment tool, screw driver, or other such tools, come in contact with the heat sinks mounted on top of the voice coil actuator.

19. Insure the following switches are set in the positions given:
 - a. S1 of Servo-Fine in SERVO position.
 - b. S1 of Head Alignment Extender PWA in FIXED position.
 - c. S1 of AZPV PWA in N position.
 - d. S2 of AZPV PWA in RW position.
 - e. S3 of AZPV PWA in X1 position.

NOTE

All AZPV PWA switches are positioned toward the rear of the drive.

20. On the system terminal, type "410" and a carriage return. Select the alignment section (#6). Issue a restore command (#1). This command is necessary to initialize the servo on track 0 of the fixed pack.

CAUTION

Whenever the heads are adjusted and the clamping screws are turned while the heads are flying, extreme care should be taken

so as not to move the carriage assembly in a lateral direction (right angles to the normal direction of head movement). The resultant force can rotate the carriage assembly and cause severe damage to the heads and disks. This motion can be prevented by applying sufficient counter force on the opposite side of the carriage as shown by the large arrow in Figure 5-1.

21. Assuming the head alignment tool is to be manipulated with the right hand, place the left hand with the side of the pointer finger against the carriage assembly on the opposite side from where the head alignment tool is inserted. Apply pressure with the left hand only when the right hand applies pressure and then try to apply equal pressure with both hands (see Step 22 below).
22. Using a head alignment tool (P/N 75893963), move the cartridge servo head toward the rear of the drive until the outer guard band is reached. The outer guard band can be located by observing the waveform shape on the oscilloscope (see Figure 5-3). The waveform shape and amplitude remains constant throughout the guard band.
23. Once the guard band has been located, use the tool to move the cartridge servo head toward the disk center until cylinder zero is reached. This can be determined by the meter reading of null (centered) and a scope waveform as shown in Figure 5-4. Remove the head alignment tool.

OSCILLOSCOPE SETTINGS

LOGIC GROUND TO SCOPE GROUND

VOLTS/DIV

CH 1 - 0.5 V
CH 2 - NOT USED

TIME/DIV

A - 0.5 μ s
B - NOT USED

TRIGGERING

A - INTERNAL POSITIVE
B - NOT USED

PROBE CONNECTIONS (USE X10 PROBE)

CH 1 TO FTU DIBITS JACK
CH 2 NOT USED

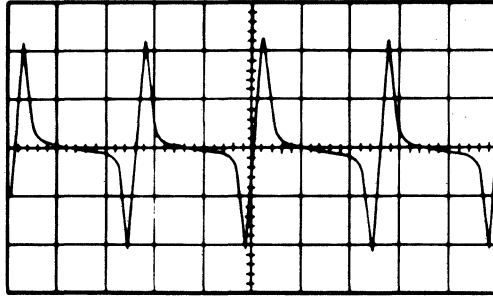


Figure 5-3. Guard-Band Waveform Pattern.

OSCILLOSCOPE SETTINGS

LOGIC GND TO SCOPE GND

VOLTS DIV

CH 1 - 0.2 V
CH 2 - NOT USED

TIME DIV

A - 0.5 μ s
B - NOT USED

TRIGGERING

A - INTERNAL POSITIVE
B - NOT USED

PROBE CONNECTIONS (USE X10 PROBE)

CH 1 TO FTU DIBITS JACK
CH 2 - NOT USED

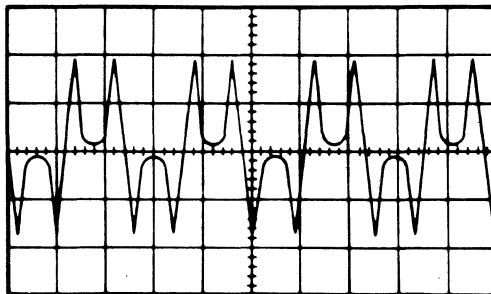


Figure 5-4. Balanced Dibit Pattern

NOTE

Steps 22 and 23 should be repeated to insure that cylinder zero is captured.

24. Perform a seek to cylinder 404. Null meter should be set to its least sensitive range.
25. Install Carriage Locking Tool (P/N 75891573). See Figure 5-5. Allow drive temperature to stabilize for 5 minutes at this cylinder.
26. Calculate the offset using the following procedure:

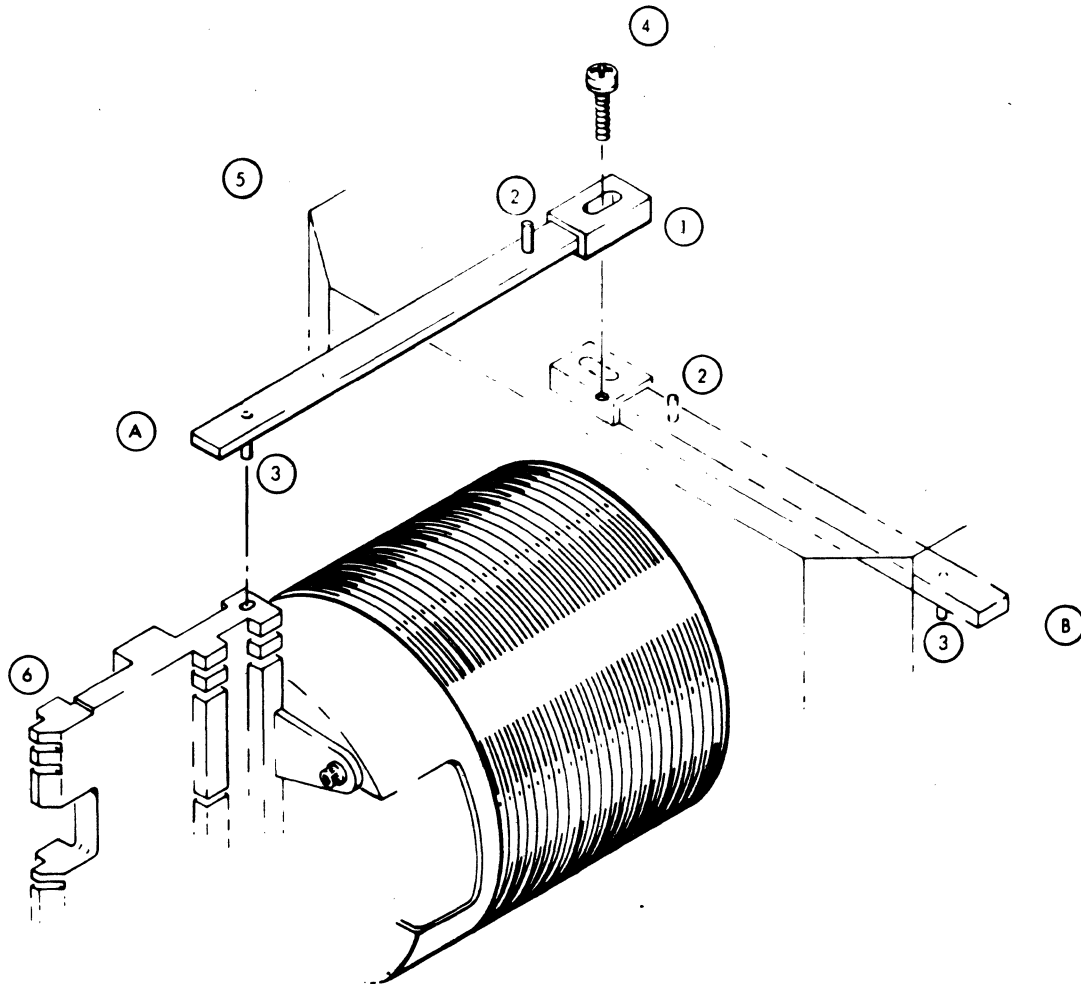
- a. Oscilloscope waveform should be similar to Figure 5-4.
- b. Set null meter to its least sensitive range (switch S3 of AZPV PWA must be on X1).
- c. Move S1 of AZPV PWA to "P" and record meter reading.
- d. Calculate the offset as described below:
 $(P) - (N) = \text{OFFSET}$

P is the meter reading with POS/NEG switch in the POS position.

N is the meter reading with the POS/NEG switch in the NEG position.

Meter readings to the right of zero are positive.

Meter readings to the left of zero are negative.



- (A) CARRIAGE LOCK PIN (1) IN HEAD ALIGNMENT POSITION
- (B) CARRIAGE LOCK PIN (1) IN OPERATING POSITION

Figure 5-5. Carriage Locking Tool-Head Alignment Position

EXAMPLE 1: $P = +20, N = +15; (P) - (N) =$
 $(20) - (15) = 5$

EXAMPLE 2: $P = +20, N = -15; (P) - (N) =$
 $(20) - (-15) = 35$

EXAMPLE 3: $P = -20, N = +15; (P) - (N) =$
 $(-20) - (+15) = -35$

27. Insert the head alignment tool again and, remembering to offset any force applied by the tool hand with the other hand, adjust the cartridge servo head position to obtain a calculated offset of less than ± 50 mV.
28. Torque the servo head clamping screw to $12 \pm \frac{1}{2}$ lb-in (1.26 to 1.38 Nm).
29. Re-calculate the offset and make any minor (only) adjustment required if the offset calculates to be greater than ± 50 mV. A minor (but only minor) adjustment can be made after the clamping screw has been tightened.
30. Remove the carriage locking tool, being careful to keep hands out of the way of the carriage in case it should retract.
31. Perform a seek to cylinder 8. Allow drive to stabilize five minutes at this cylinder.
32. Calculate the offset as above. Record the offset calculated for later reference.
33. Seek to cylinder 800. Allow drive to stabilize for five minutes at this cylinder.

34. Calculate the offset as in steps above and record the offset for later reference.

NOTE

Oscilloscope waveforms at cylinders 8 and 800 should be similar to Figure 5-4. Calculated offset should be less than ± 350 mV. If either cylinder offset is greater than ± 350 mV, repeat steps 23 through 33. Minor compensatory adjustments can be made at cylinder 404 in an attempt to effect the offset at cylinders 8 and 800. However, the final calculated offset cannot exceed ± 100 mV at cylinder 404.

35. Set the following switches to the positions given:
 - a. S1 of Servo Fine to DATA.
 - b. S1 of Head Alignment Extender PWA to NORMAL.
 - c. S1 of AZPV PWA to N.
 - d. S2 of AZPV PWA TO R/W.
 - e. S3 of AZPV PWA to X1.
36. Command RTZ. This ensures that the drive will servo on the cartridge servo and select data head 0.
37. Repeat steps 24 through 30 for the cartridge data head.
38. Command an alternate seek between cylinders 257 and 512 for a minimum of 30 seconds.

39. Check the cartridge servo head alignment. To do this, set the following switches to the positions given:
 - a. S1 of the Servo Fine PWA to SERVO.
 - b. S1 of the Head Alignment Extender PWA to FXD.
 - c. S1 of AZPV to N.
 - d. S2 of AZPV to R/W.
 - e. S3 of AZPV to X1.
40. Seek to cylinder 404 and allow drive to stabilize five minutes. Then calculate the offset as in step 26 for the cartridge servo head. If the calculated offset is greater than ± 100 mV, repeat steps 24 through 34 and then 38 and 39.
41. Check the cartridge data head alignment. To do this, set the following switches to the positions given and perform the other operations as specified:
 - a. S1 of the Servo Fine PWA to DATA.
 - b. S1 of the Head Alignment Extender PWA to NORM.
 - c. Select head 0 (i.e., issue RTZ command).
42. Seek to cylinder 404, allow drive to stabilize five minutes and calculate the offset for the cartridge data head as described in step 26. If the calculated offset exceeds ± 100 mV, repeat steps 35 through 40.

43. When head alignment is completed, press the STOP/START switch to stop the drive and wait until the spindle drive motor has stopped.
44. Remove the CE cartridge and install the cartridge into its protective cover.
45. Write Protect switches on the operator panel can be released if desired.
46. Set the AC circuit breaker (rear of drive) to the OFF position.
47. Remove the head alignment kit from:
 - a. Drive.
 - b. Meter.
 - c. AZPV PWA and Extender PWA.
 - d. Cable from R/W preamp PWA to Servo Fine PWA.
 - e. Cable from extender PWA to Servo Fine PWA.
48. Return the Electronics Module to its normal position and install locking screws.

CAUTION

Use extreme caution when setting the Electronics Module down into its normal position. Cables that are in the close proximity of the Electronics Module will be damaged if caution is not used.

49. Store the carriage locking tool in its normal operating position as shown in Figure 5-5.
50. Install the drive cover assembly.

5.4.4 CARTRIDGE DATA HEAD ALIGNMENT PROCEDURE.

The procedure for aligning a newly replaced cartridge data read/write head is given in the following paragraphs.

CAUTION

Use only head alignment tool P/N 75893963. (7 in Figure 5-1.) Use of a different tool can cause permanent damage to head/arm carriage. Inspect head adjustment tool for damage (nicked, scratched, etc.) at adjustment end. End should have a polished surface where it enters carriage. Polish end with crocus cloth if aluminum deposits are present and wipe clean. Do not use emery cloth, sandpaper, or files which can permanently damage tool, and subsequently damage heads and carriage holes. Do not use a defective tool. Repair or replace tool if damage exists. Use care when using the head alignment tool 7 (refer to Figure 5-1). The tool should slip easily through the alignment hole in the carriage and into the slot in the head/arm. When adjusting the head, the tool should turn freely in the hole. If anything more than a small amount of force is required to adjust the head/arm, the tool is probably binding in the hole in the carriage.

1. Refer to paragraph 5.4.3, INITIAL HEAD ALIGNMENT PROCEDURE, in performing the following steps for the CARTRIDGE DATA HEAD.
 - a. Perform steps 1 through 11.
 - b. Perform steps 14 through 17.
 - c. Perform steps 35 through 38.
 - d. Perform steps 40 through 48.

5.4.5 CARTRIDGE SERVO HEAD ALIGNMENT PROCEDURE.

The procedure for aligning a newly replaced cartridge servo head is given in the following paragraphs.

1. Refer to paragraph 5.4.3, INITIAL HEAD ALIGNMENT PROCEDURE, in performing the following steps for the CARTRIDGE SERVO HEAD.
 - a. Perform steps 1 through 11.
 - b. Perform steps 14 through 48.

5.4.6 FIXED DISK MODULE DATA READ/WRITE HEAD ALIGNMENT PROCEDURE.

The procedure for aligning a newly replaced fixed disk module data read/write head is given in the following paragraphs.

NOTE

In order to recover data when changing a fixed disk module data read/write head, the host system must be utilized in order to read the formatted surface involved.

1. Allow the drive to stabilize by running with the heads loaded for a minimum of 15 minutes.
2. Seek to and attempt to read from the replaced head at cylinder 404 (a continuous loop read and error print-out is desired).
3. Install the carriage locking tool in the head alignment position as shown in Figure 5-5.
4. Connect an oscilloscope so as to be able to look at the read analog differential voltage across TP1 and TP2 of the read/write preamp PWA. Move the newly replaced head slowly in the forward and reverse directions with the head alignment tool while watching the read voltage and listening to the error print out. Adjust initially for maximum read voltage. Continue adjusting until no error is printed.
5. Torque the head clamping screw to $12 \pm \frac{1}{2}$ lb-in (1.26 to 1.38 Nm) and readjust the head for zero error printout if necessary.
6. Repeat the fine tune adjustment step with the head alignment tool until the drive will read error free.
7. Remove the head alignment tool.
8. Remove carriage locking tool being careful to keep hands out of the way of the carriage in case it should retract. It should be noted that the above procedure is designed to recover as much of the customer data as possible. The error rate performance cannot be guaranteed

over the range of environmental extremes normally specified for the drive. Therefore, it is recommended that all of the data be recovered from and be rewritten on the surface covered by the newly replaced head.

9. Operate the STOP/START switch to the STOP position and wait for the drive to stop turning.
10. Set the AC circuit breaker to OFF.
11. Install case cover assembly.
12. Turn on AC circuit breaker and start the drive.

5.4.7 FIXED MODULE SERVO HEAD ALIGNMENT PROCEDURE.

The procedure for aligning a newly replaced fixed servo head is given in the following paragraphs.

1. The fixed disk module servo head clamping screw should have been torqued to $4 \pm \frac{1}{2}$ lb-in (0.4 Nm) when installed.
2. Plug the cartridge servo head connector into J3 (bottom header) of the Servo Preamp PWA.
3. Plug the fixed disk module servo head connector into J1 (the top header).
4. Refer to paragraph 5.4.3, INITIAL ALIGNMENT PROCEDURE, in performing the following steps.
5. Perform steps 5 through 11 for the fixed disk module servo head.

6. Perform steps 15 through 34 for the fixed disk module servo head.
7. Perform steps 38, 39 and 41 for the fixed disk module servo head.

NOTE

Make sure adjustment is on the fixed disk module servo head.

8. Set CB1 to the OFF position.
9. Plug the Cartridge servo head connector into header J1 of the Servo Preamp PWA.
10. Plug the fixed disk module servo head connector into header J3 of the Servo Preamp PWA.

NOTE

It is recommended that the data on the fixed disk module be recovered and reformatted subsequent to completion of the alignment procedure involving a fixed pack servo.

11. Set AC circuit breaker to the ON position.
12. Start the Drive.
13. Recover and reformat the fixed disk module data.
14. Stop the Drive.
15. Perform steps 44 through 48.

5.5 PREVENTIVE MAINTENANCE.

The CMD is designed to require minimal preventive maintenance. The preventive maintenance index provided in Table 5-1 is meant to be used only as a general guideline. The preventive maintenance index consists of seven levels based on a calendar period or on hours of operation (whichever comes first). For corrective maintenance of the CMD, refer to the Control Data Corp. hardware maintenance manual 75888415.

CAUTION

No electrical or electronic component/assembly should be removed and/or replaced when the AC power is applied to the unit. Anytime the AC power is ON, the DC voltages are present on the electronics.

I/O cables should absolutely NOT be removed or replaced when AC power is applied to the unit.

Table 5-1. Maintenance Index and Schedule

PREVENTIVE MAINTENANCE	PARA.	SCHEDULE
Pre-Filter Removal and Replacement	5.5.1	4*
Inspect Actuator Assembly (Disks in)	5.5.2	4
Check Power Supply Outputs	5.5.3	4
Absolute Filter Removal and Replacement	5.5.1	6*

Table 5-1 (Cont.). Maintenance Index and Schedule

DEFINITION OF SCHEDULE
Level 0 - Daily, depending on conditions stated
Level 1 - Weekly or 150 hours (no preventive maintenance scheduled)
Level 2 - Monthly or 500 hours (no preventive maintenance scheduled)
Level 3 - Quarterly or 1500 hours
Level 4 - Semi-annually or 3000 hours (no preventive maintenance scheduled)
Level 5 - Annually or 6000 hours
Level 6 - 9,000 hours

* Maximum times. Preventive maintenance may be required more frequently depending on dust contamination level of operation area.

The materials used in the procedures of this section are listed in Table 5-2.

Table 5-2. Maintenance Materials

MATERIAL	SOURCE
Gauze Lint-Free	Control Data 12209713
Media Cleaning Solution	Control Data 95033502
Tongue Depressors	Commercially available
Dust Remover, Super Dry	Control Data 95047800
Computer Card	No. 5084

5.5.1 PREFILTER AND ABSOLUTE FILTER REMOVAL AND REPLACEMENT.

Refer to Figure 5-6 for the following procedure.

1. Remove the front panel (1) mounting screws (2) which are accessed through the front panel air inlet slot at each side, and at the back of the inlet hole.
2. Remove the front panel.
3. The prefilter (3) is secured at the right and left edges by a bracket (5) at each edge. Remove the screw (4) holding each bracket and remove the brackets. Remove the prefilter (3).
4. The prefilter can be cleaned or replaced. To clean the prefilter agitate it in a mild detergent solution. Blow in the reverse direction with a low pressure nozzle until dry.
5. Reinstall the prefilter by reversing steps 1, 2 and 3.
6. Remove top cover and raise deck per procedure given in CMD hardware maintenance manual.
7. To remove the absolute filter (6) lift it at its rear end enough to allow it to be pulled toward the rear of the unit. This should free the front end from the hole in the manifold. Lift the filter out of the unit. Replace the filter with movements the reverse of those required for removal.
8. Lower the deck, install Front Panel and replace the top cover per the procedure in the hardware maintenance manual.

9. Restore power to the unit. Allow blower to purge the unit for 10 minutes.
10. Restore drive to normal operating condition.

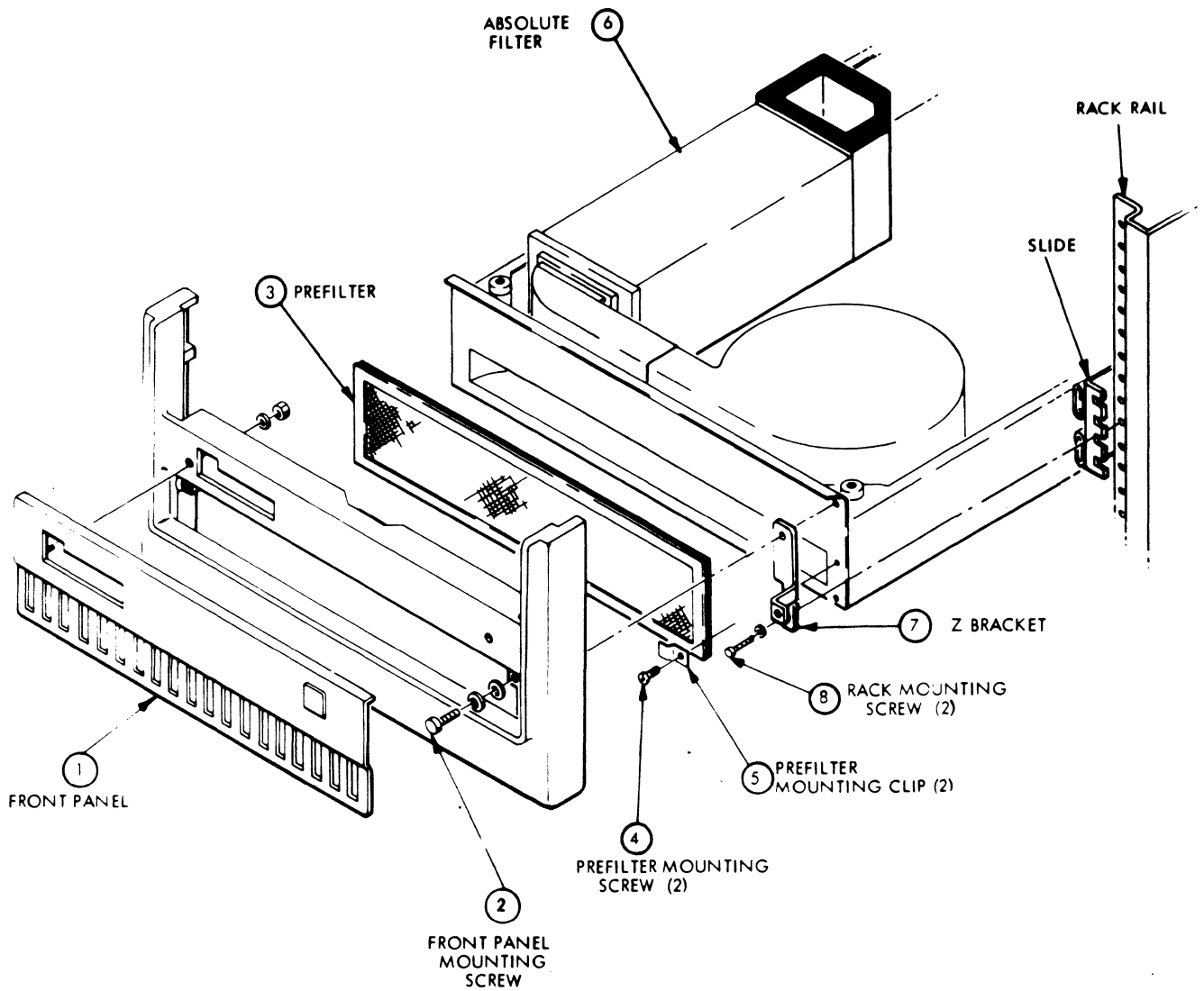


Figure 5-6. Filter Removal and Replacement

5.5.2 ACTUATOR ASSEMBLY INSPECTION AND CLEANING WITH FIXED DISK MODULE STILL IN THE DRIVE.

1. Set AC POWER circuit breaker to OFF.
2. Remove top cover per hardware maintenance manual.
3. Remove disk cartridge disk module.
4. WITHOUT LOADING THE HEADS, inspect entire actuator for presence of dust and other foreign materials. Pay particular attention to the rail surfaces of the carriage and bearing assembly, but do not load heads. The heads may be moved up to $\frac{1}{2}$ inch (12 mm) toward the spindle in order to inspect the rail and bearings.
5. Use lint-free gauze dampened with media cleaning solution (not soaked) to remove deposits or attracted particles.
6. Push the carriage back into the fully retracted position.
7. Restore drive to normal operating condition.

5.5.3 POWER SUPPLY CHECK.

Power supply outputs can be checked at EM pins called out by wire list in hardware maintenance manual.

SECTION 6
SCHEMATIC AND PARTS LIST

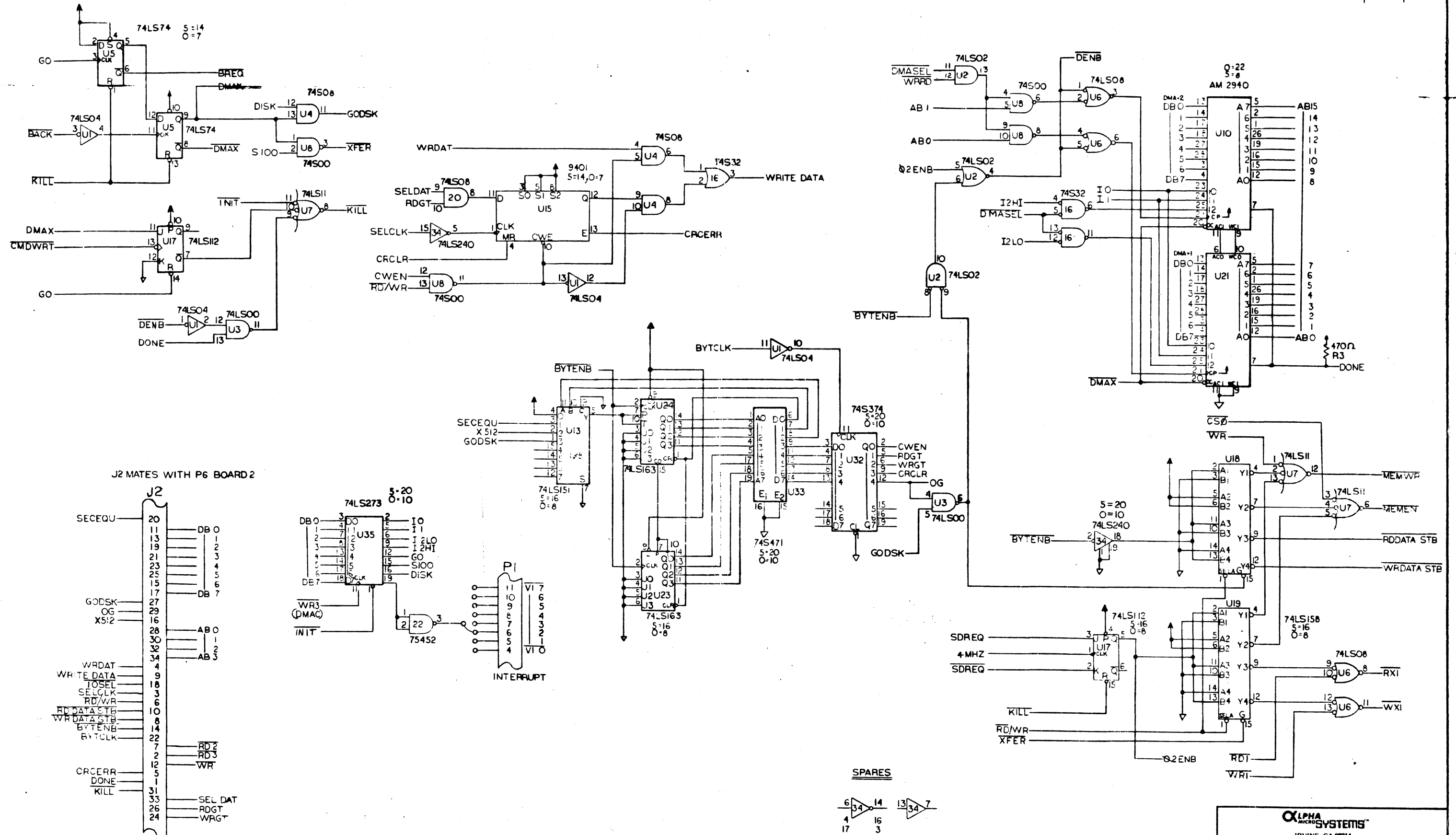
Table 6-1. AM-410-1 Component Cross-Reference List

REF DESIG	MFG. TYPE NO.	PAR. NO.	REF DESIG	MFG TYPE NO.	PAR NO.
U1	74LS04	-	U24	74LS163	4.2.12
U2	74LS02	-	U25	74LS138	4.2.6
U3	74S00	-	U26	74LS138	4.2.6
U4	74LS08	-	U27	8131	4.2.23
U5	74LS74	4.2.4	U28	74LS367	4.2.18
U6	74LS08	-	U29	74LS30	-
U7	74LS11	-	U30	74LS139	4.2.7
U8	74LS00	-	U31	DWB-00412-00	-
U9	4MHz Osc.	-	U32	74S374	4.2.20
U10	2940	4.2.2	U33	DWB-00413-00	-
U11	Z80	4.2.1	U34	74LS240	4.2.16
			U35	74LS273	4.2.17
U13	74LS151	4.2.8	U36	81LS97	-
U14	74LS74	4.2.4	U37	74LS374	4.2.20
U15	9401	4.2.3	U38	74LS374	4.2.20
U16	74LS32	-	U39	74LS373	4.2.19
U17	74LS112	4.2.5	U40	74LS374	4.2.20
U18	74LS158	4.2.10	U41	2114	4.2.22
U19	74LS158	4.2.10	U42	2114	4.2.22
U20	74LS08	-	U43	8304	-
U21	2940	4.2.2	U44	7805	-
U22	75452	-	U45	7805	-
U23	74LS163	4.2.12	U46	7805	-

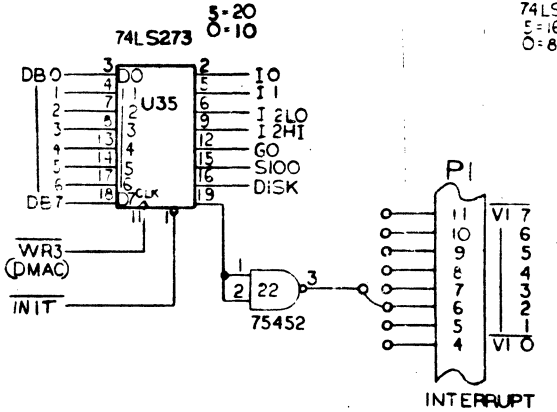
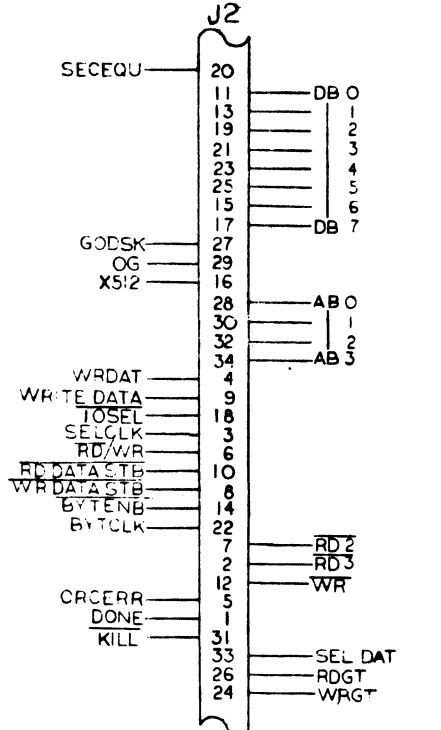
Table 6-2. AM-410-2 Component Cross-Reference List

REF DESIG	MFG TYPE NO.	PAR. NO.	REF DESIG	MFG TYPE NO.	PAR NO.
U1	3453	-	U24	74LS374	4.2.20
U2	3453	-	U25	745166	4.2.14
U3	3453	-	U26	8131	4.2.23
U4	3450	-	U27	3450	-
U5	3450	-	U28	3453	-
U6	81LS97	-	U29	74LS27	-
U7	74LS138	4.2.6	U30	74LS374	4.2.20
U8	74LS374	4.2.20	U31	74LS164	4.2.13
U9	3450	-	U32	74LS393	4.2.21
U10	3453	-	U33	745367	4.2.18
U11	3453	-	U34	74LS161	4.2.11
U12	74LS374	4.2.20	U35	74LS11	-
U13	74LS175	4.2.15	U36	81LS98	-
U14	74LS374	4.2.20	U37	74LS74	4.2.4
U15	3450	-	U38	74LS02	-
U16	3453	-			
U17	3453	-	U40	74LS74	4.2.4
U18	74LS374	4.2.20	U41	74LS163	4.2.12
U19	74LS175	4.2.15			
U20	74LS374	4.2.20	U43	74LS157	4.2.9
U21	3450	-	U44	74LS74	4.2.4
U22	3453	-	U45	7805	-
U23	74LS157	4.2.9	U46	7805	-
			U47	7905	-

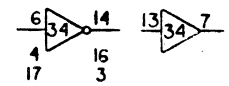
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
000			



J2 MATES WITH P6 BOARD 2



SPARES

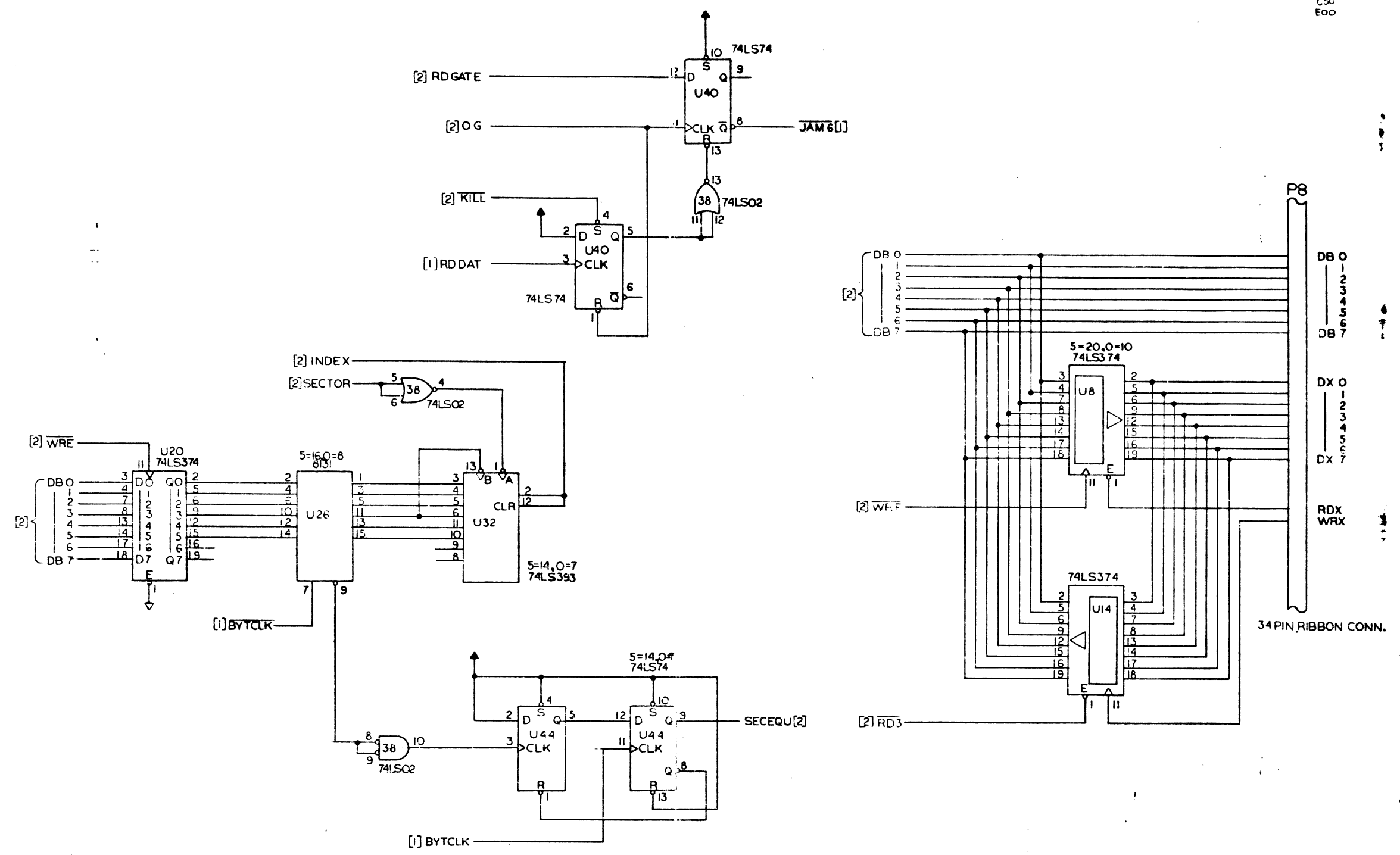


ALPHA MICRO SYSTEMS
IRVINE, CA 92714

TITLE: AM-410 STORAGE MODULE CONTROLLER

DESIGNED BY	CHECKED BY	REV	PAGE	DRAWING NO.
		000	2/2	DW-00410-XX

REVISIONS			
REV	DESCRIPTION	DATE	APPROVAL
ACC			
COO			
EOO			



ALPHA MICRO SYSTEMS IRVINE, CA 92714			
TITLE		AM-411 STORAGE MODULE CONTROLLER	
REV	PAGE	DRAWING NO	
EOO	3/3	DWL-00411-XX	

FBILL # DWB-00410-00

REV.000

14 Dec,1979

DESCRIPTION ASSY STORAGE MODULE CONT AM-410-1

PART NUMBER	DESCRIPTION	QTY
1	DWF-00410-01 PCB STORAGE MODULE CONT AM-410	1
2	HDM-00007-00 HEAT SINK .750WI .375HT .750LG	3
3	HDS-00632-01 SCREW 6-32 X .250	3
4	HDN-00632-01 NUT HEX 6-32 STL SM PATTERN	3
5	HDW-00632-01 WASHER LOCK 6-32	3
6	ICL-07805-00 IC REGULATOR + 5V	3
7	CNS-00008-00 SOCKET 8 PIN DIP	1
8	CNS-00014-00 SOCKET 14 PIN DIP	14
9	CNS-00016-00 SOCKET 16 PIN DIP	11
10	CNS-00018-00 SOCKET 18 PIN DIP	2
11	CNS-00020-00 SOCKET 20 PIN DIP	10
12	CNS-00024-00 SOCKET 24 PIN DIP	1
13	CNS-00028-00 SOCKET 28 PIN DIP	2
14	CNS-00040-00 SOCKET 40 PIN DIP	1
15	IC1-07400-01 IC QUAD 2 INPUT NAND GATE	1
16	IC1-07402-01 IC QUAD 2 INPUT NOR GATE	1
17	IC1-07408-01 IC QUAD 2 INPUT AND GATE	1
18	IC1-07430-01 IC 3 INPUT NAND GATE	1
19	IC1-07432-01 IC QUAD 2 INPUT OR GATE	1
20	IC1-07474-01 IC DUAL D FLIPFLOP	2
21	IC1-08131-00 IC COMPARATOR 6 BIT	1
22	IC1-08197-01 IC BUFFER OCTAL	1
23	IC1-74240-01 IC OCTAL BUS DRIVER INVERTING	1
24	IC1-74112-01 IC DUAL J-K NEGATIVE FLIPFLOP	1
25	IC1-74138-01 IC DECODER 3TO 8 LINE	2
26	IC1-74139-01 IC DECODER 2 TO 4 LINE DUAL	1
27	IC1-74151-01 IC 8 INPUT MULTIPLEXER	1
28	IC1-74273-01 IC OCTAL D REGISTER W/RESET	1
29	IC1-74367-00 IC HEX BUFFER	1
30	IC1-74374-01 IC OCTAL D FLIPFLOP	3
31	IC1-74374-02 IC OCTAL D FLIPFLOP	1
32	ICM-02114-04 RAM 1K X 4 BIT STATIC	2
33	DWR-00412-00 ASSY FROM SMDLOB	1
34	ICS-00080-00 IC MICROPROCESSOR Z-80	1
35	ICS-02940-00 IC DMA ADDRESS GENERATOR	2
36	ICS-09401-00 IC GENERATOR CRC	1
37	RS2-00102-00 RESISTOR 1 K 1/4W 5% CAR	4

PART NUMBER	DESCRIPTION	QTY
38	RS2-00331-00 RESISTOR 330 OHM 1/4W 5% CAR	1
39	RS2-00471-00 RESISTOR 470 OHM 1/4W 5% CAR	1
40	CPP-00156-01 CAPACITOR 15 UF 20V	7
41	CPN-00103-01 CAPACITOR .01 UF	20
42	IC1-74373-01 IC OCTAL D FLIPFLOP	1
43	IC1-75452-00 IC DUAL NAND POWER DRIVER	1
44	IC1-08304-00 IC TRANSCEIVER OCTAL	1
45	IC1-74163-01 IC SYNCHRONOUS COUNTER	2
46	DWB-00413-00 ASSY PROM ROM410	1
47	IC1-07411-01 IC TRIPLE 3 INPUT AND GATE	1
48	IC1-74158-01 IC QUAD 2 TO 1 DATA SELECTOR	2
49	ICS-00003-00 IC OSCILLATOR 4 MHZ	1
50	RSN-00008-00 RES PACK 8 PIN SIP 1 K	1
51	CNF-00003-01 HEADER 34 PIN W/O EJC RT ANGLE	1
52	IC1-07408-02 IC QUAD 2 INPUT AND GATE	2
53	IC1-07404-01 IC HEX INVERTER	1
54	IC1-07400-02 IC QUAD 2 INPUT NAND GATE	1
55	HDM-00003-09 BUS BAR PC MOUNT 9 POSITION	2
56	HDM-00003-11 BUS BAR PC MOUNT 11 POSITION	1
57	HDM-00012-00 THERMAL GREASE	1
58	CNF-00004-01 HEADER 8 PIN STRAIGHT	2
59	CNA-00006-00 CONN RECEPTACLE SHORTING 2CONT BLK	1
60	DWL-00410-XX LOGIC STORAGE MODULE CONT AM-410	1

REV.E00

14 Dec,1979

DESCRIPTION ASSY STORAGE MODULE CONT AM-411

PART NUMBER	DESCRIPTION	QTY
1	DWF-00411-XX * * * * RECORD NOT FOUND * * * *	1
2	CNF-00006-11 HEADER 26 PIN DBL ROW STRAIGHT	4
3	CNF-00003-01 HEADER 34 PIN W/O EJC RT ANGLE	1
4	CNF-00005-01 HEADER 60 PIN W/O EJC RT ANGLE	1
5	CNS-00014-00 SOCKET 14 PIN DIP	8
6	CNS-00016-00 SOCKET 16 PIN DIP	26
7	CNS-00020-00 SOCKET 20 PIN DIP	7
8	CPN-00103-01 CAPACITOR .01 UF	21
9	CFP-00156-01 CAPACITOR 15 UF 20V	4
10	IC1-07402-01 IC QUAD 2 INPUT NOR GATE	1
11	IC1-07411-01 IC TRIPLE 3 INPUT AND GATE	1
12	IC1-07427-01 IC TRIPLE 3 INPUT NOR GATE	1
13	IC1-07474-01 IC DUAL D FLIPFLOP	3
14	IC1-08131-00 IC COMPARATOR 6 BIT	1
15	IC1-08197-01 IC BUFFER OCTAL	1
16	IC1-08198-01 IC INVERTER OCTAL	1
17	IC1-74138-01 IC DECODER 3 TO 8 LINE	2
18	IC1-74157-01 IC QUAD 2 TO 1 DATA SELECTOR	2
19	*** DELETED PART ***	0
20	IC1-74161-01 IC SYNCHRONOUS 4 BIT COUNTER	1
21	IC1-74163-01 IC SYNCHRONOUS COUNTER	1
22	IC1-74164-01 IC 8 BIT SER IN PAR OUT SR	1
23	IC1-74166-00 IC 8 BIT PAR IN SER OUT SR	1
24	IC1-74175-01 IC QUAD D FLIPFLOP	2
25	IC1-74367-00 IC HEX BUFFER	1
26	IC1-74374-01 IC OCTAL D FLIPFLOP	5
27	IC1-74393-01 IC DUAL 4 BIT BINARY COUNTER	1
28	IC1-03450-00 IC QUAD LINE RECEIVER	6
29	IC1-03453-00 IC QUAD LINE DRIVER	9
30	ICL-07805-00 IC REGULATOR + 5V	1
31	ICL-07905-01 IC REGULATOR -5 V TO-3	1
32	HDM-00021-00 HEAT SINK 1.4 WI .5 HT 1.890L	2
33	HDM-00012-00 THERMAL GREASE	0
34	HDN-00632-01 NUT HEX 6-32 STL SM PATTERN	4
35	HDS-00632-01 SCREW 6-32 X .250	4
36	HDW-00632-01 WASHER LOCK 6-32	4
37	*** DELETED PART ***	0

BILL # DWB-00411-00

DESCRIPTION ASSY STORAGE MODULE CONT AM-411


PART NUMBER	DESCRIPTION	QTY
38 RSN-00006-00	RES PACK 10PIN SIP 56 OHM	2
39 DWL-00411-XX	LOGIC STORAGE MODULE CONT AM-411	1
40 RSN-00011-00	RES PACK 8 PIN SIP 56 OHM	5
41 RS2-00222-00	RESISTOR 2.2 K 1/4W 5% CAR	2
42 RS2-00472-00	RESISTOR 4.7 K 1/4W 5% CAR	2
43 TRN-03904-00	TRANSISTOR NPN	2

APPLICATION		REVISIONS					
NEXT ASSY	USED ON	REV.	DESCRIPTION	DATE	APPROVED		

X = Don't care

PIN # NAME	ROM ADDR.					ROM OUTPUTS							COMMENTS	
	A4	A3	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2		D1
	0	0	0	0	0	1	0	0	1	1	1	1	0	Initialization (Writing)
4	0	0	0	0	1	0	1	0	1	0	0	1	0	RAM Write
5.	0	0	0	1	0	1	1	0	1	1	1	1	0	
6	0	0	0	1	1	0	0	1	1	1	1	1	1	Wait for DRQ (bit A3)
stop 7.	0	0	1	0	0	0	0	0	0	1	1	1	1	
1.	0	0	1	1	0	X	Y	Y	X	X	X	X	Y	
3.	0	0	1	1	0	X	X	Y	X	X	X	X	Y	
4	0	1	1	1	1	0	0	0	1	1	1	1	1	Rest State
	0	1	0	0	0	1	0	0	1	1	1	1	0	1st State - Write Seq. * REASD
	0	1	0	0	1	0	1	0	1	0	0	1	0	RAM Write
	0	1	0	1	0	1	1	0	1	1	1	1	0	
	0	1	0	1	1	0	0	1	1	1	1	1	1	
	0	1	1	0	0	0	0	0	1	1	1	1	1	Jump to start
	0	1	1	0	1	Y	Y	X	Y	X	Y	X	X	
	0	1	1	1	0	Y	Y	X	Y	X	X	X	X	
2.	0	1	1	1	1	0	0	1	1	1	1	1	1	
	1	0	0	0	0	1	0	0	1	1	1	1	1	Initialization (...
	1	0	0	0	1	0	1	1	1	0	1	0	1	
	1	0	0	1	0	1	1	0	1	1	0	1	1	
6.	1	0	0	1	1	0	0	1	1	1	1	1	1	
stop 7.	1	0	1	0	0	0	0	0	0	1	1	1	1	Wait for DRQ
	1	0	1	0	1	X	Y	Y	Y	Y	Y	Y	Y	
	1	0	1	1	0	Y	Y	Y	Y	X	X	Y	Y	
1.	1	0	1	1	1	0	0	0	1	1	1	1	1	Rest State for pending Read
3.	1	1	0	0	0	1	0	0	1	1	0	1	1	Select RAM
4.	1	1	0	0	1	0	1	0	1	1	0	0	0	WE to 1791
5.	1	1	0	1	0	1	1	0	1	1	0	1	1	End RE
	1	1	0	1	1	0	0	1	1	1	1	1	1	
8.	1	1	1	0	0	0	0	0	1	1	1	1	1	Jump to start
	1	1	1	0	1	Y	Y	Y	Y	Y	Y	Y	Y	
	1	1	1	1	0	X	Y	Y	Y	X	Y	Y	Y	
2.	1	1	1	1	1	0	0	0	1	1	1	1	1	Rest State

A0 A1 A2 D0 D1 D2 D3 D4 D5 D6 D7 D8

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± XXX ±	CONTRACT NO.		 IRVINE CA 92714 POWELL, INC.	
	APPROVALS	DATE		
MATERIAL	DRAWN	8X32 ROM TRUTH TABLE		
FINISH	CHECKED	(74LS288 OR EQUIV)		
DO NOT SCALE DRAWING	ISSUED	SIZE	FSCM NO.	DWG. NO.
		A		-02 Version F.C.
		SCALE		SHEET



Alpha Microsystems
17881 Sky Park North
Irvine, California 92714