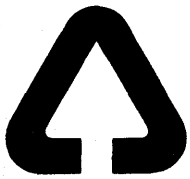

Advanced Computer Design

PDQ-3 Hardware User's Manual

PDQ-3 Hardware User's Manual

VERSION 1.0

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1. INTRODUCTION

This manual is designed to be used as an aid in the installation, configuration, and operation of the PDQ-3 Computer System. Knowledge of the Q-Bus or LSI-11 Bus, UCSD Pascal language, or UCSD operating system is not required for the use of this manual. For more information on these subjects, please refer to the reference materials listed in section 1.1.

Chapter 2 describes the various options available when ordering a PDQ-3 system, and specifies the technical attributes of the major components. Chapter 3 describes procedures and precautions to observe when installing, configuring, and operating the PDQ-3 computer. Chapter 4 gives a general description of the PDQ-3 system components. Chapter 5 describes the Q-Bus. Chapter 6 describes the PDQ-3 CPU Module.

1.0 General

The PDQ-3 is a 16-bit, stack-oriented computer system. Its CPU is a 16-bit MOS microprocessor, microcoded to execute the UCSD Pascal Version III.0 P-code. In addition, the CPU includes hardware floating point (IEEE draft standard), integer arithmetic, and multiply and divide instructions. The CPU Module board contains the microprocessor, a DMA floppy controller, an RS-232C terminal interface, a real time clock, an interval timer, and a low level debugger. Each CPU Module is assigned a unique serial number accessible to the software.

The PDQ-3 adopts the industrial de-facto standard Q-Bus as its system bus, enabling the system to be configured to a wide variety of applications. These range from word processing, data communications, and accounting, to scientific research and industrial process control. By selecting from a large list of readily available memory modules and peripheral controllers, the user of the system can easily adapt the PDQ-3 to almost any application.

The Q-Bus is an 18-bit wide Asynchronous Interlock Bus that allows the CPU to communicate with memory and I/O devices of vastly different speeds. Other features of the Q-Bus include daisy-chained, prioritized interrupt service and direct memory access to improve system performance. Power up/power down sequencing and battery back-up are also available.

Figure 1.0 illustrates how the Q-Bus connects the CPU with its memory modules and peripherals. Up to 14 memory modules and peripherals may be connected to the Q-Bus along with the PDQ-3 CPU Module, providing up to 64K words of directly addressable memory space. 4K words is reserved for memory mapped I/O and ROM (see Appendix B).

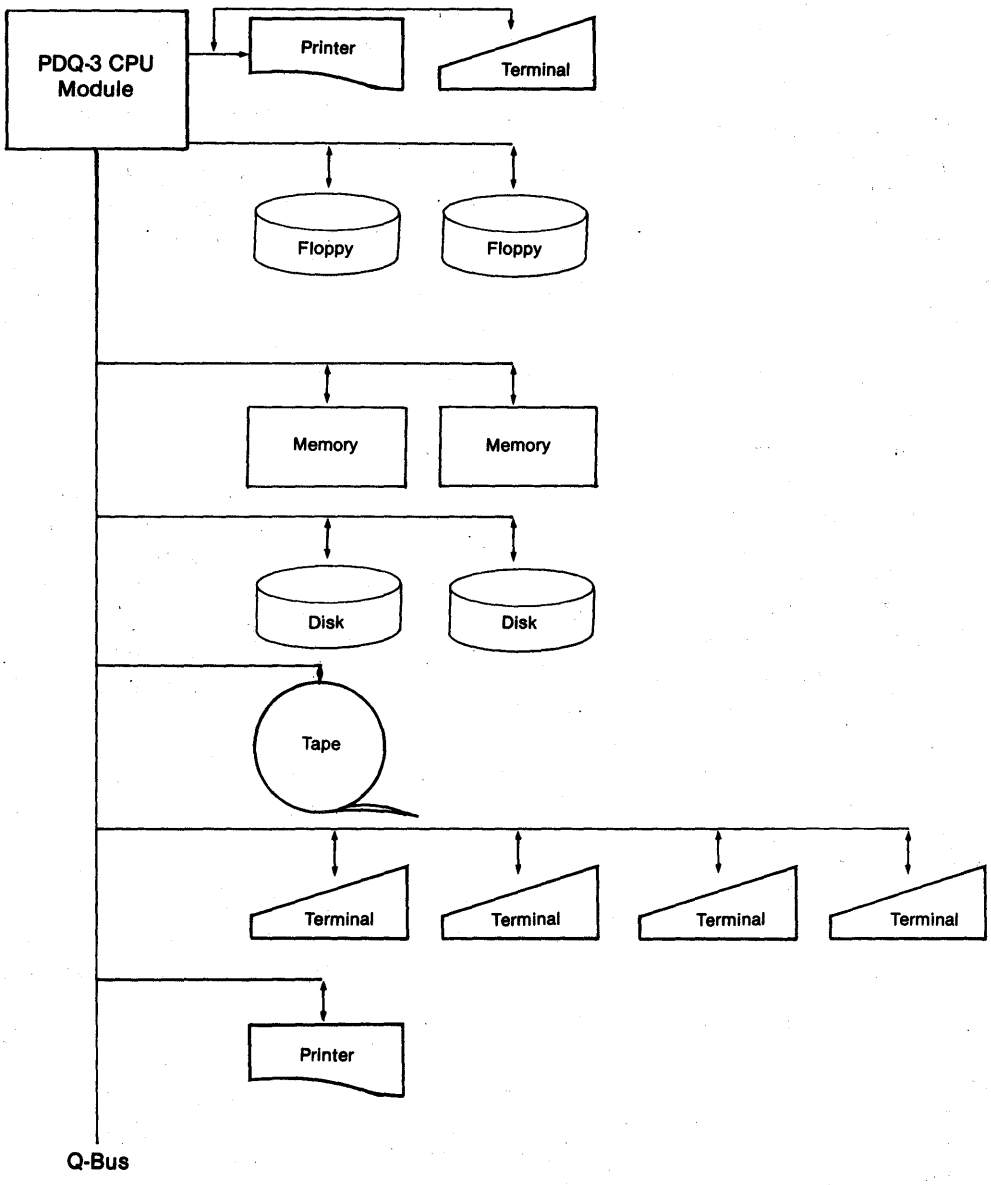


Figure 1.0 Block Diagram of the PDQ-3 Computer System

1.1 Reference Materials

*** PDQ-3 Software User's Manual	Advanced Computer Design
Programming in Pascal	Peter Grogono Addison-Wesley Publishing Co., Inc. Reading, Mass., 1978
Beginner's Guide For the UCSD Pascal System	Kenneth Bowles, UCSD Byte Publications, Inc.
Pascal User's Manual & Report	Jensen & Writh Springer-Verlag New York, 1974
Microcomputer Handbook	Digital Equipment Corp. Digital Publishing Corp. Maynard, Mass., 1979
*** ADDENDA	Advanced Computer Design

*** Provided by Advanced Computer Design as reference material with this manual.

2. SYSTEM OVERVIEW

2.0 Basic System and Available Versions

The PDQ-3 series computers are available in two basic versions: the PDQ-3 CPU Module only, and the PDQ-3 Computer System.

2.0.0 The PDQ-3 CPU Module Version

Under this version the buyer purchases only the CPU Module. This version is available in five models. Each includes the CPU, the Real Time Clock, the Interval Timer, the RS-232C controller, and the double density DMA floppy disk controller. The models differ only in their bootstrapping ROMs.

a) The PDQ-3/1. The bootstrapping ROM provided with this model boots from the on-board floppy disk controller.

b) The PDQ-3/2. The bootstrapping ROM provided with this model boots from an RXV-01 floppy disk subsystem.

c) The PDQ-3/3. The bootstrapping ROM provided with this model boots from an RXV-02 floppy disk subsystem.

d) The PDQ-3/4. The bootstrapping ROM provided with this model boots from an RP-01 mass storage disk subsystem.

e) The PDQ-3/5. The bootstrapping ROM provided with this model boots from an RP-02 mass storage subsystem.

The factory may be contacted for other bootstrapping requirements.

2.0.1 The PDQ-3 Computer System Version

A PDQ-3 Computer System includes one of the CPU Module versions described above and a combination of options selected from the five following categories:

1) 110 V (60 cycle) or 220 V (50 cycle)

2) Single-sided or double-sided floppy disk drives

3) One or two 8 dual-size slot backplanes

4) 64K or 128K bytes

5) Desk-top or Rackmount version

The system model number can be found on the Model Specifications label on the rear panel of the chassis. It appears as follows:

PDQ-3(A)-(B)-(C)-(D)

A: S = Single-sided floppy disk drives
   D = Double-sided floppy disk drives

B: 4 = One 8 dual-size slot backplane
   8 = Two 8 dual-size slot backplanes

C: 064 = 64K byte configuration
   128 = 128K byte configuration

D: 1 = Desk-top version
   2 = Rack-mount version

2.1 General Specifications

2.1.0 The CPU Module

(A) CPU

Word Size	: 16 bits Instruction
Instruction Length	: One to four bytes
Typical Instruction Cycle	: 12 microseconds (based on memory access time of 400 nsec)
Addressing Range	: 64K words (with 4K words memory mapped I/O)
Interrupt Level	: BR4 only

(B) Multiplexed Serial Port Controller

Interface	: EIA RS-232C
Baud Rate	: 50 to 19,200
Order	: Least significant bit first.
Distance	: Depends on the baud rate. (see Appendix D)
Character Format	: 7 or 8 bits, no parity, two stop bits.
Console Signals	: TD, RD, RTS, CTS, DTR, DSR
Printer Signals	: TD, DTR

(C) DMA Floppy Disk Controller

Interface	:	Shugart SA800/SA850, single/ double density, single/double sided, 8" soft sectored drives with automatic Track 43 current switching.
Format	:	Software controlled IBM formats : 1 (FM), 2 (MFM) 1D (FM), 2D (MFM)
Number of Drives	:	up to 4 single/double density, single/double sided drives

(D) DC Power Requirements

+5V +/- 5% @ 2.80 Amp. Max.

+12V +/- 5% @ 0.15 Amp. Max.

-12V +/- 5% @ 0.04 Amp. Max.

(E) Environmental Requirements

Operating Temperature range	:	Celcius	: 0C to 50C
		Farenheit	: 32F to 122F
Non-Operating Temperature Range	:	Celcius	: -40C to 80C
		Farenheit	: -40F to 176F
Humidity	:	10% to 90% without condensation	
Air Flow	:	30 cubic feet/minute minimum is recommended	

(F) Physical Size : One Quad-size card, 8.5" x 10.5"

2.1.1 The LSI-11 Backplane

(A) Number of Dual Size Slots : 8 per backplane

(B) Number of Backplanes : 2 per system chassis
3 maximum per system

(C) Power Requirements

	Voltage (+/- 5%)	Amperage
Primary Backplane (with 250 Ohm termination resistors)	+5 V	1.1 A
	+12 V	0.2 A
Secondary Backplane(s) (with 120 Ohm termination resistors)	+5 V	1.1 A
	+12 V	0 A

The power required for the Primary Backplane is used by the power up/down sequencing logic, 250 Ohm Bus termination resistors, and the front console.

The power required for the Secondary Backplane is used by 120 Ohm Bus termination resistors.

2.1.2 The Memory Modules

(A)	Memory Capacity	: 32K and 64K word configurations available.
(B)	Read Access Time	: 300 nsec max.
	Cycle Time	: 500 nsec max.
(C)	Physical Size	: One Dual-size card, 8.5" x 5.2"
(D)	Electrical Specifications	: Refer to the Memory Module technical manual

2.1.3 The Floppy Drives

(A)	Type of Drives	: 8" single/double sided, single/double density soft sectored floppy drives with Shugart interface
(B)	Number of Drives	: 2 per system chassis 4 maximum per system

(C) Performance

	Single Density	Double Density
(a) Formatted Capacity		
Single Side	0.5 Megabyte	1.0 Megabyte
Double Side	1.0 Megabyte	2.0 Megabyte
(b) Transfer Rate	250,000 bits/sec	500,000 bits/sec
	Single Sided	**Double Sided**
(c) Latency		
Average	83.3 ms	83.3 ms
Maximum	166.7 ms	166.7 ms
(d) Seek Times		
Track/Track	6 ms	3 ms
Average	275 ms	96 ms
Head Settling	15 ms	20 ms
(e) Head Load	60 ms	40 ms

(D) Power Requirements (per drive)

(a) AC	110V @ 60Hz	220V @ 50Hz
Voltage Range		
single-sided	100V to 130V	200V to 240V
double-sided	90V to 132V	196V to 264V
Frequency	+/- 2%	+/- 2%
Current (typ)		
single-sided	0.85A	0.53A
double-sided	0.4A	0.25A

(b) DC (+/- 5%)	Selected	Unselected
+5V	1.1A max.	1.1A max.
+24V	1.4A max.	0.3A max.

2.1.4 The Power Supplies

(A) Primary and Secondary Power Supplies

(a) Type : Switcher
(b) Minimum Load : 2.5A on +5V per supply
(c) Number of Power Supplies
Per 8 dual size slot backplane : 1
Per chassis : 2 max.
(d) Maximum Power : 150W (primary supply)
150W (secondaries)

# of dual slots	Power Supply	+5V	+12V	+24V
8	primary	20A max	5.0A max	2.0A max
16	primary + secondary	40A max	10.0A max	2.0A max

(B) DC/DC Converter
(Mounted on the Primary Backplane for CPU and backplane logic requirements only)

(a) Input : +5V +/- 5% @ 0.5A max.
(b) Output : -12V +/- 5% @ 80mA max.

(C) Available DC Power and Current for LSI-11 modules (Including CPU)

	Primary Supply	Secondary Supply
Total DC Power*	90W max	145W max
+5V	17A max	19A max
+12V	4.8A max	5A max

* Note that the total combined power used by +5V and +12V must not exceed this maximum.

2.1.5 System AC Power Requirements

No. of dual size slots	110V @ 60Hz*		220V @ 50Hz*	
	In rush (for 8 ms)	Steady	In rush (for 8 ms)	Steady
8	32.0A max	5.2A max	20.0A max	3.2A max
16	62.0A max	8.3A max	40.0A max	5.2A max

* 110V +/- 20% (90V min, 132V max)
  60HZ +/- 2%
  220V +/- 10% (196V min, 264V max)
  50Hz +/- 2%

2.1.6 System Environment Requirements

	Temperature		Humidity
	Celcius min/max	Farenheit min/max	Non-condensing
Storage	-40C/60C	-40F/140F	5% to 95%
Operation	5C/40C	41F/104F	20% to 80%

2.1.7 System Physical Specifications

PDQ-System with Two Drives	Dimensions (in)	Dimensions (cm)	Weight (lb)	Weight (kg)
Rackmounted				
Width	18 15/16"	48.10 cm.		
Height	10 9/16"	26.83 cm.	63 lbs.	138.6 kg.
Depth	22 5/8"	57.47 cm.		
Desk-Top				
Width	18 1/16"	45.88 cm.		
Height	11"	27.94 cm.	57 lbs.	125.4 kg.
Depth	22 3/4"	57.79 cm.		

3. SYSTEM CONFIGURATION AND INSTALLATION

This chapter discusses the basic considerations, requirements, and instructions for the configuration, installation, and operation of the PDQ-3 Computer Systems. The PDQ-3 Computer Systems are factory configured and may be used without reconfiguration in many applications. However, all PDQ-3 CPU modules and all Q-Bus memory and peripheral modules contain jumpers and/or switches which allow the user to reconfigure the system to specific needs.

3.0 Installation

This section describes the recommended procedures for setting up the PDQ-3 Computer System. The topics covered are packing and unpacking, opening and inspecting the chassis, system configuration, and power and environmental requirements.

3.0.0 Packing and Unpacking

When unpacking the PDQ-3 Computer for the first time, do so according to the following procedure:

1) Inspect the shipping carton for any signs of damage. Report any damage to the freight carrier immediately.

2) The carton will arrive with a packing slip listing the package contents. Make sure that all listed items are accounted for.

3) Open the packing carton. Before removing the inner carton, check for and remove any loose parts (cables, manuals, etc.) around the carton. The inner carton contains the PDQ-3 Computer. Lift out the inner carton and open it.

4) Before removing the PDQ-3 Computer from its carton, make sure it is intact and that there are no loose parts in the carton. Remove the foam corner braces. Then, with the help of another person, gently lift the PDQ-3 Computer out of the carton and place it on a sturdy surface off the floor.

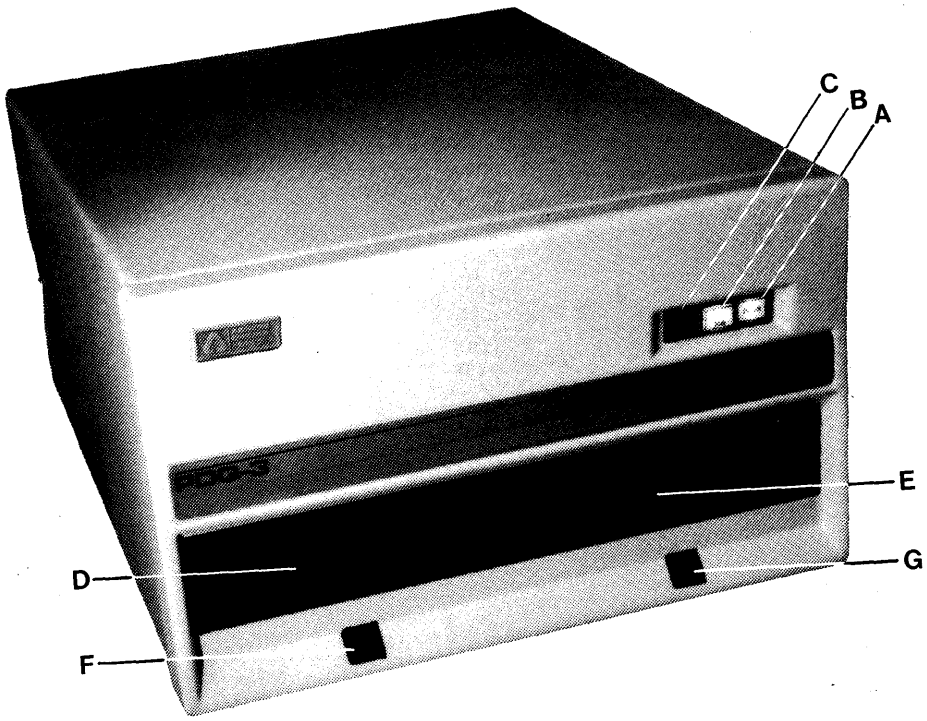
   WARNING: When lifting the PDQ-3, always get a firm grip on the bottom of it. Do not lift the PDQ-3 by the Front Panel (which pulls off).

5) Once the PDQ-3 is out of the box, carry out a visual inspection of the chassis to insure that it is not damaged in any way. Check the chassis for dents, cracks, or scratches. Check the condition of the switches on the front and rear panel. The procedure for inspecting the interior of the PDQ-3 Computer is described in section 3.0.1.

6) Report any damage to Advanced Computer Design immediately.

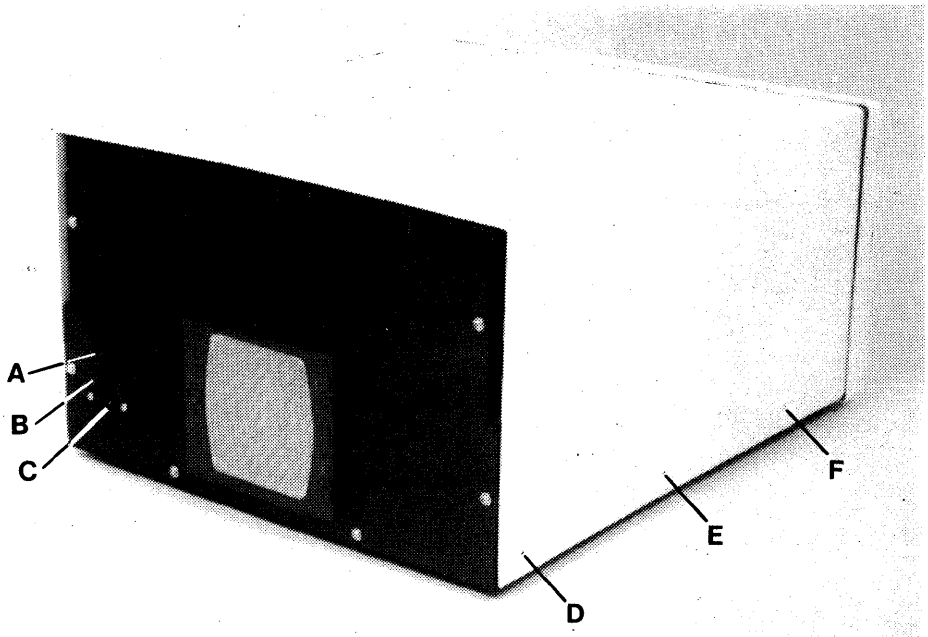
7) It is a good idea to save the packing material and box in case the PDQ-3 ever has to be packed for shipping.

8) To ship the PDQ-3, use the original packing materials and cartons to package the PDQ-3 in exactly the same way in which it was received. Seal the cartons securely.



A) DC Power On/Off switch and light indicator
B) Run/Halt mode switch and light indicator
C) System Reset switch and Bus activity LED
D) Floppy Drive Unit #0
E) Floppy Drive Unit #1
F) Door Release Lever Unit #0
G) Door Release Lever Unit #1

Figure 3.0.0.A The PDQ-3 Computer System: Front View (Desk-Top Model shown)



A) AC On/Off Switch
B) Fuse Holder
C) AC plug and EMI filter
D-F) Cover screws (desk-top model only)

Figure 3.0.0.B The PDQ-3 Computer System: Rear View (Desk-Top Model shown)

3.0.1 Opening and Inspecting The Chassis

IMPORTANT: Do not connect any power to the system until everything has been properly inspected and reassembled. Always disconnect the AC power cable (rear panel) before removing the top cover or the rear panel.

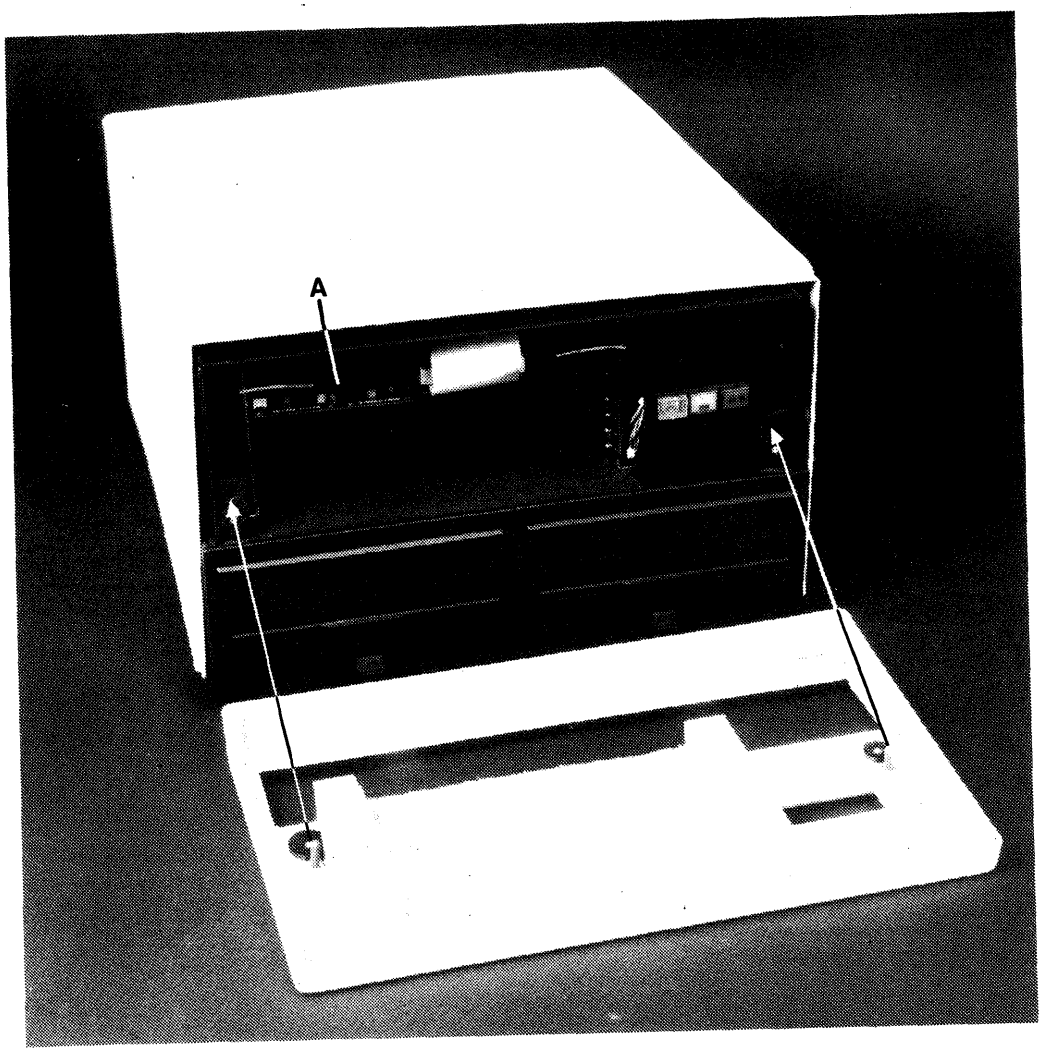
WARNING: Most LSI-11 Modules are static sensitive. They should be handled only in static controlled environments.

To open and inspect the chassis of the PDQ-3 Computer:

1) Pull the Front Panel forward to remove it (see Figure 3.0.1.A).

2) The CPU Module arrives from the factory configured for a terminal transmitting and receiving data at 9600 baud. If the console terminal does not operate at 9600 baud (see the terminal Operator's Guide for details), the CPU module must be configured for the appropriate baud rate (see section 3.1.0).

3) Verify that all modules are securely in place and are making positive contact with the backplane connectors.



A) Card Cage

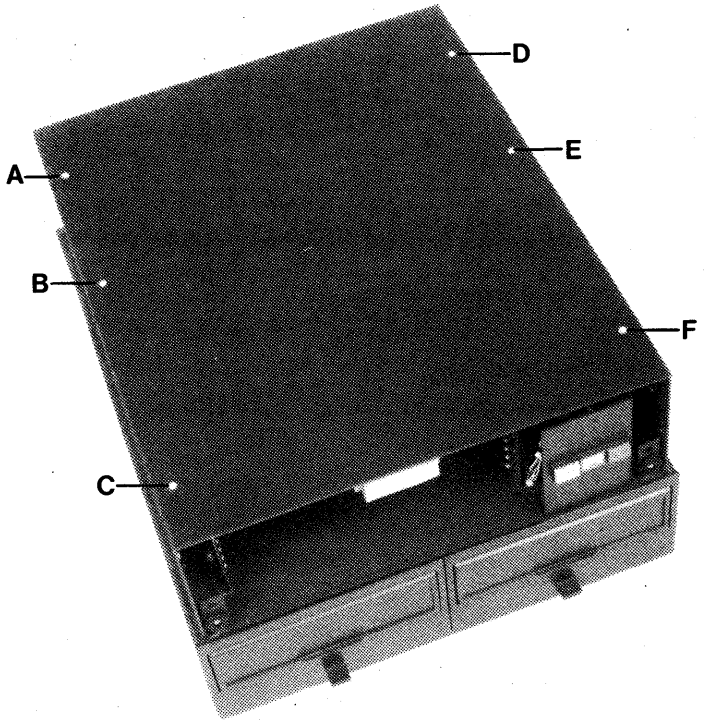
Figure 3.0.1.A. Removing the Front Panel

5) If the PDQ-3 system is a desk-top version, unscrew the three(3) screws (see Figure 3.0.0.B) on each side of the rectangular cover, and lift the cover to remove it.

6) Remove the cover of the chassis by unscrewing the six(6) top screws, and lifting the cover off (see Figure 3.0.1.B).

7) In the rear half of the chassis (see Figure 3.3.0) are one(1) or two(2) 8 dual-size-slot backplanes, depending on what was ordered, and their corresponding power supplies. If there are two(2) backplanes, the secondary power supply is mounted on a plate behind the backplanes. Beneath this is the primary power supply (see section 3.3.1).

8) Check to see that there are no disconnected cables or loose parts.



A-F) Chassis Cover screws

Figure 3.0.1.B Opening the Chassis

3.0.2 Inserting and Removing Circuit Boards

WARNING: To prevent static electricity from damaging circuit boards, all modules should be handled in a static controlled environment.

Once the front panel has been removed (see section 3.0.1), the circuit boards are exposed, and may be removed, or new ones inserted (see Figure 3.0.4).

To remove circuit boards from the PDQ-3:

1) Disconnect any cables from the board.

2) If the board has metal push-bar levers on either side, grasp these and pull them away from the circuit board until the teeth of the levers are free of the slots of the card cage; then carefully slide the board out of the chassis.

If there are no push-bar levers, grasp the plastic card handle at either side of the board and slide the circuit board out of the card cage.

To insert circuit boards into the PDQ-3:

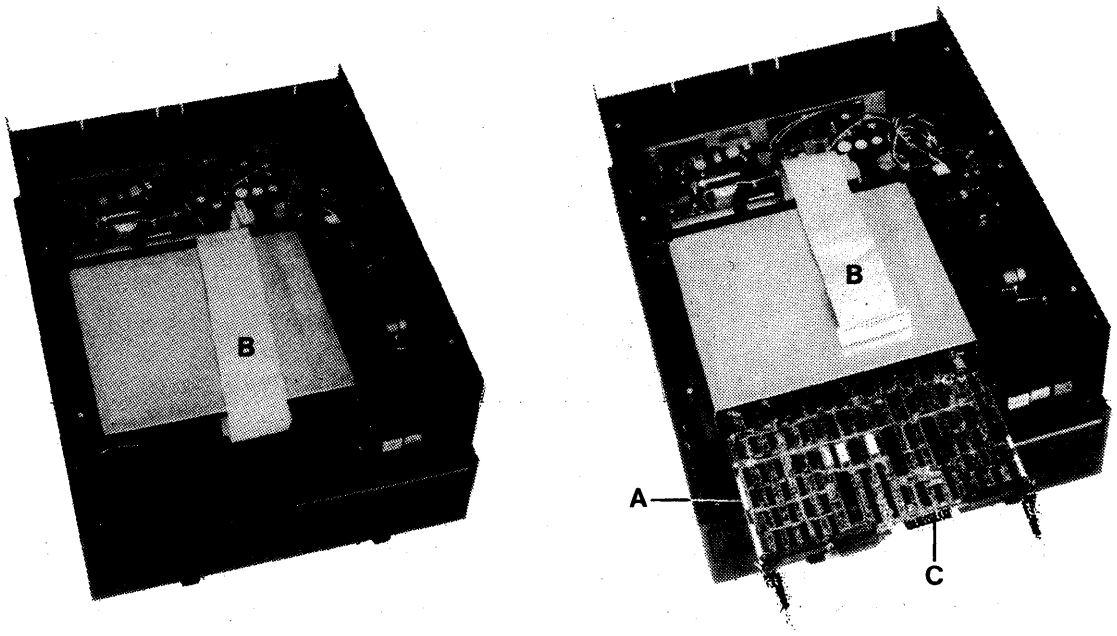
1) With the finger connectors of the board facing the back-plane(s), insert the board, component side up, into the tracks on either side of the card cage.

2) Carefully slide the board toward the backplane (into the card cage).

3) If the circuit board has metal push-bar levers on either side, slide the board in far enough (with the levers out) to fit the teeth of the levers into the slots in the card cage. Press the levers carefully toward the circuit board until they are flush with the board. Sometimes one lever will have to be pressed in slightly to center the board before the other will move.

   If there are no push-bar levers, grasp the plastic card handle at the front of the circuit board, and push the board into the backplane until the it is firmly connected to the backplane.

4) Connect all necessary cables to the circuit board.



A) CPU Module
B) Floppy Control cable
C) Floppy Control cable finger connectors

Figure 3.0.2 Inserting and Removing Circuit Boards

3.0.3 Configuring a PDQ-3 System

The PDQ-3 System is configured at the factory. If any modules

are added to or removed form the system, the PDQ-3 may need reconfiguring.

To Configure a PDQ-3 System:

1) Set the device and interrupt vector addresses (if any), and other required parameters of each module according to the module's instruction manual. All modules provided with the PDQ-3 system are preconfigured for use with the system. A list of reserved device and vector addresses may be found in Appendix B.

2) Determine the relative DMA and interrupt priority of each module in the system. The relative priority should be chosen in such a way that the system will operate to its maximum efficiency. This is generally accomplished as follows:

   a) Fast devices should have higher priority over slower ones to prevent data loss.

   b) Devices from which it is impossible or costly to recover lost data should have higher priority over devices from which lost data can be easily recovered.

   c) Devices which require less processor service should have higher priority to maximize system throughput.

3) In the PDQ-3 system, the CPU Module always resides in the top-most slot of the Primary Backplane. For modules that initiate DMA and/or interrupt requests, modules with higher priority should be installed 'electrically' closer to the CPU than modules with lower priority (see section 3.1.2 for device priority assignments). The position of modules which do not initiate DMA and/or interrupt requests is unimportant. However, each slot of the backplane between the CPU and a DMA/Interrupt module must be filled to avoid breaking the DMA/Interrupt request daisy chain.

4) Calculate the total combined DC power requirements of the modules in each backplane. Power requirements for each module may be found in the specific module's instruction manual, generally under "Power Requirements". This total should not exceed the maximum power available for each backplane (see section 2.1.4). It is recommended that modules with higher power requirements be installed in the Secondary backplane to take advantage of the extra power available on that backplane. However, DMA and Interrupt priority order must be observed.

WARNING: The Secondary power supply requires a minimum current consumption of 2.5A on the +5V in order to regulate its outputs to the correct voltage levels. The total combined +5V current consumption of all the modules in the Secondary Backplane should exceed or equal 2.5A. The Secondary power supply will not be damaged if it is not loaded.

5) The PDQ-3 systems are designed with adequate cooling to

operate under the environmental conditions specified in section 2.1.6. However, the following additional procedures are recommended when configuring a system:

a) Dual-size devices with higher power consumption, and therefore, higher heat dissipation, should be placed on the left side of the card cage (connectors A and B), providing the priority requirements are not violated.

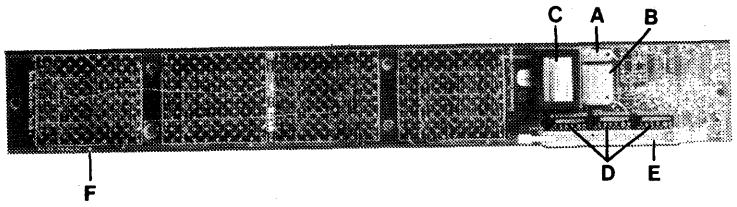
b) To avoid creating a hot spot inside the card cage, modules with high heat dissipation should not be installed adjacent to each other.

3.0.3.0 Backplane Configuration

The PDQ-3 System may contain one or two backplanes. The first backplane is called the Primary Backplane, and the second is called the Secondary Backplane. The two backplanes are interconnected by a 50 conductor ribbon cable for backplane expansion (see Figures 3.0.3.A - 3.0.3.D).

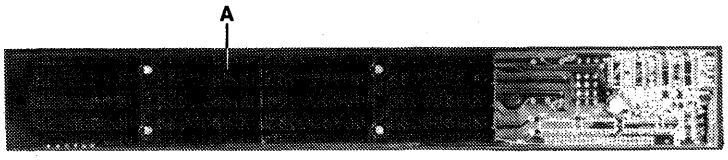
A) Q-Bus connector
B) Power up/down sequencing logic
C) Connector for front panel control switches

Figure 3.0.3.A Primary Backplane (Front View)



A) Battery back-up connector
B) Power supply input source
C) +5V to -12V DC/DC converter
D) Termination resistor packs and IC sockets
E) Primary to secondary backplane expansion ribbon cable connector
F) Jumpers E1 to E6

Figure 3.0.3.B Primary Backplane (Rear View)



A) Q-Bus connector

Figure 3.0.3.C Secondary Backplane (Front View)

(Provided as Addendum)

A) Battery back-up connector
B) Power supply input source
C) Termination resistor packs and IC sockets
D) Primary to secondary backplane expansion ribbon cable connector
E) Jumpers E1 to E6

Figure 3.0.3.D Secondary Backplane (Rear View)

3.0.3.0.0 The Primary Backplane

The Primary Backplane is the main backplane of the PDQ-3 system. The top-most slot is reserved for the CPU Module. The interrupt and DMA priority daisy chains are jumpered at the factory to be compatible with the DEC backplane configuration. For the Primary backplane, the E1 and E2 jumpers are connected for the BIAKI L and BIAKO L interrupt daisy chain, and the E4 and E5 jumpers are connected for the BDMGI L and BDMGO L interrupt daisy chain. The interrupt and DMA priority order for the Primary backplane is shown in Table 3.1. Three 250 Ohm termination resistor packs are used for bus signal terminations.

	Slot A	Slot B	Slot C	Slot D
Row 1	PDQ-3 CPU Module			
Row 2	Priority B		Priority A	
Row 3	Priority C		Priority D	
Row 4	Priority F		Priority E	

(Front View)

Note : The PDQ-3 Module on-board devices have highest priority. The priority order of other positions is from A (highest) to F (lowest).

Table 3.1 Primary Backplane Interrupt and DMA Priority Configuration

3.0.3.0.1 The Secondary Backplane

The Secondary backplane is used for backplane expansion. It is connected to the Primary backplane by a 50 pin ribbon cable. The interrupt and DMA priority daisy chains are jumpered at the factory to be compatible with the DEC backplane configuration. For the Secondary backplane, the E1 and E2 jumpers are connected for the BIAKI L and BIAKO L interrupt daisy chain, and the E4 and E5 jumpers are connected for the BDMGI L and BDMGO L interrupt daisy chain. The interrupt and DMA priority order for the Secondary backplane is shown in Table 3.2. Three 250 Ohm termination resistor packs are used for bus signal terminations.

	Slot A	Slot B	Slot C	Slot D
Row 1	Priority H		Priority J	
Row 2	Priority L		Priority K	
Row 3	Priority M		Priority N	
Row 4	Priority O		Priority P	

(Front View)

Note : The modules in the Primary backplane have priority over the modules in the Secondary backplane. The priority order of positions in the Secondary backplane goes from H (highest) to P (lowest).

Table 3.2 Secondary Backplane Interrupt and DMA Priority Configuration

3.0.3.1 Memory Configuration

For memory configuration information, please refer to the memory user's manual provided.

3.0.3.2 Other LSI-11 Modules

Recommended Device and vector address assignments are listed in Appendix B. For configuration of other LSI-11 modules, please refer to the specific module's user's manual.

3.0.4 Power Requirements

For the power requirements of the PDQ-3, please refer to section 2.1.5, System AC Power Requirements.

3.0.5 Environmental Requirements

For the environmental requirements of the PDQ-3, please refer to section 2.1.6, System Environment Requirements.

3.1 Configuring the PDQ-3 Modules

3.1.0 Factory Configuration

The PDQ-3 Computer System is configured at the factory as follows:

1) The CPU module is strapped with jumper E14 and the System Environment switches are configured for a 9600 baud rate (see section 3.1.1 for a description of the jumper and switch options).

2) The memory address space is configured for the size of the system memory ordered, with memory starting at location 0000. The last 4K words of memory in a 64K word memory space is disabled in favor of the Q-Bus memory mapped I/O device address (see Appendix B).

3) The Backplane(s) is(are) configured for interrupt and DMA priority and terminated as shown in Figure 5.8.0.

4) The left floppy disk drive is configured for unit #0 (or logical unit #4). The right drive is cofigured for unit #1 (or logical unit #5).

3.1.1 CPU Module Jumper and Switch Options

The CPU Module is pictured in Figure 3.1.0.

1) Jumpers:

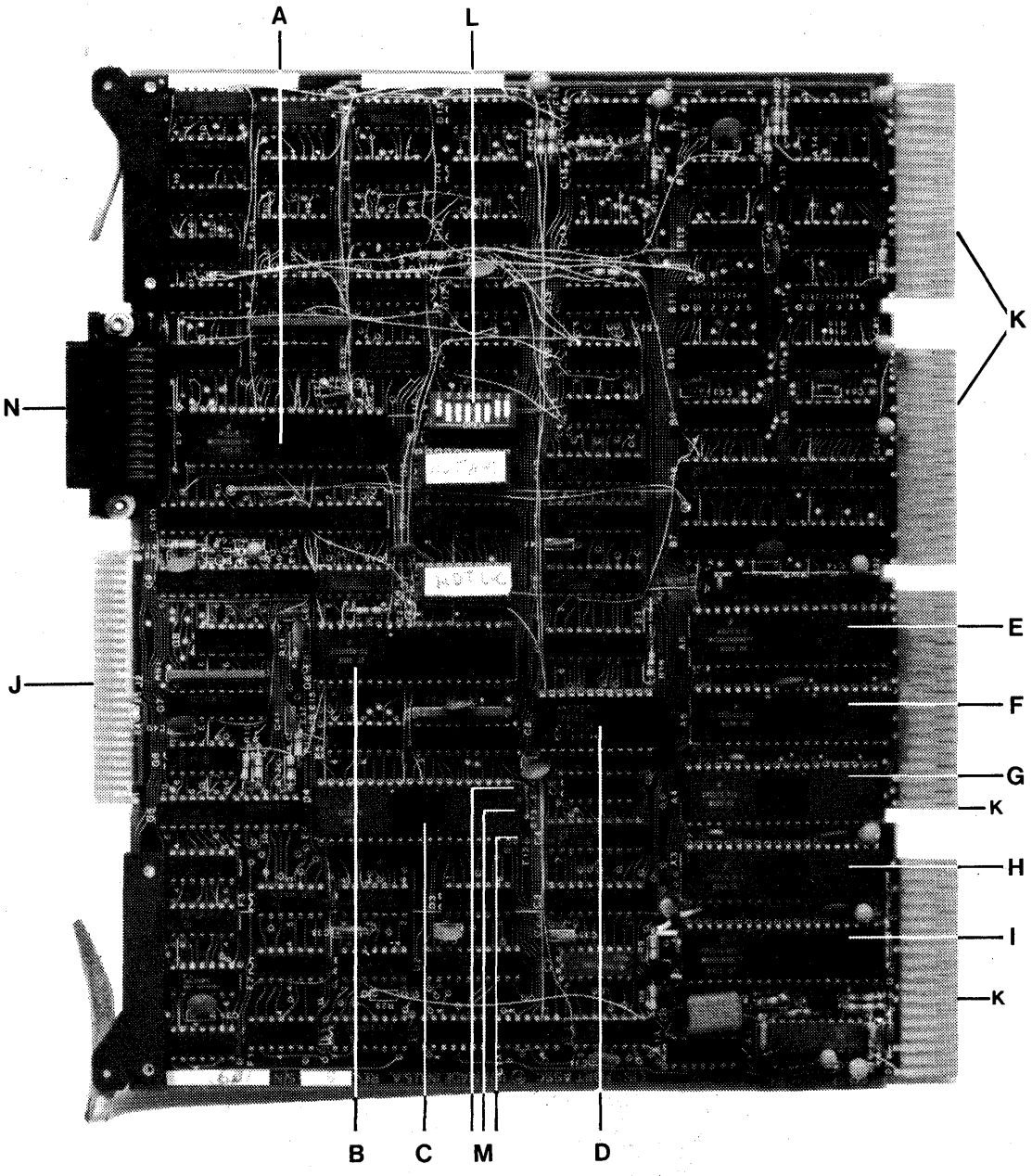
The state of the PDQ-3 after power-up or reset is determined by the connection of option jumpers E12 or E14 to jumper E13. If jumpers E14 and E13 are connected, the PDQ-3 comes up in the Hexadecimal Debugging Tool (HDT) state (see Appendix A). If jumpers E12 and E13 are connected, the PDQ-3 comes up in the automatic bootstrapping routine and bootstraps from the appropriate device, depending on the version of the CPU module. The CPU module is strapped with jumper E14 by the factory.

2) System Environment Switches:

Switches one(1) through three(3) select the baud rate for the console CRT, and should be set as shown in Figure 3.1.1. They are configured at the factory for 9600 baud.

Switches four(4) and five(5) select the printer baud

rate, and should be set as shown in Figure 3.1.2. Switches six(6) and seven(7) are unused and available for user applications. Switch eight(8) is used for maintenance, and should always be on (open).



A) USART
B) 1793 Floppy Controller
C) 1883 DMA Controller
D) 8253 Counter Timer
E-I) Micro-Engine Chip set
J) Floppy finger connectors
K) Q-Bus finger connectors
L) System Environment Switches
M) Jumpers E12, E13, E14
N) Console plug

Figure 3.1.0 The CPU Module

Console Baud Rate	Switches 1	2	3
110	open	open	open
300	closed	open	open
600	open	closed	open
1200	closed	closed	open
2400	open	open	closed
4800	closed	open	closed
9600	open	closed	closed
19200	closed	closed	closed

note: open = on, closed = off

Figure 3.1.1 Table of Switch Options: 1-3

Printer Baud Rate	Switches 4	5	6	7	8
9600	open	open	X	X	open
1200	closed	open	X	X	open
300	open	closed	X	X	open
110	closed	closed	X	X	open

note: open = on, closed = off, X = don't care

Figure 3.1.2 Table of Switch Options: 4-8

3.2 First Time Operation

This section describes the procedure for the first time operation of the PDQ-3 System, but procedures and information describing powering up and down, bootstrapping, and inserting and removing floppy diskettes can be applied to general system operation.

3.2.0 Turning Power On

IMPORTANT: Before powering up the PDQ-3, make sure it is completely reassembled. Operating the PDQ-3 with any cover removed hinders proper air circulation and may cause damage to the system.

Before plugging the AC power into the PDQ-3, the following items should be checked:

1) The AC Rating on the Model Specifications label on the rear panel should be checked for power specifications. They must be compatible with the AC power specifications for the AC power source that will be used.

2) The power requirements of all circuit boards in each backplane should be checked against the power ratings for the power supply connected to each backplane (see section 2.1.4). The maximum power requirements must not add up to more power than the power supply can produce.

3) The AC switch (rear panel) should be in the off (down) position.

4) The DC ON button (front panel) should be in the off (out) position.

5) Either the floppy drive doors should be open, or all floppy diskettes should be removed from the floppy drives. LEAVING DISKETTES IN THE FLOPPY DRIVES WITH THE DOORS CLOSED WHILE POWERING UP OR DOWN IS NOT RECOMMENDED.

To power on:

1) Check the console CRT baud rate for compatibility with the CPU Module baud rate (see section 3.1.1).

2) Plug the AC power cord into the rear panel of the PDQ-3 and into the wall socket. Plug the console CRT into the wall socket and turn its power ON (see the Terminal's Operation guide for details).

3) Connect the console transmission cable to the console input and to the console socket on the rear panel of the PDQ-3.

4) Flip the AC switch to the on (up) position. This should turn on the fans and start the motors for the floppy disk drives running. If the motors do not start running, check the rear panel (Figure 3.0.0.B) for a blown fuse.

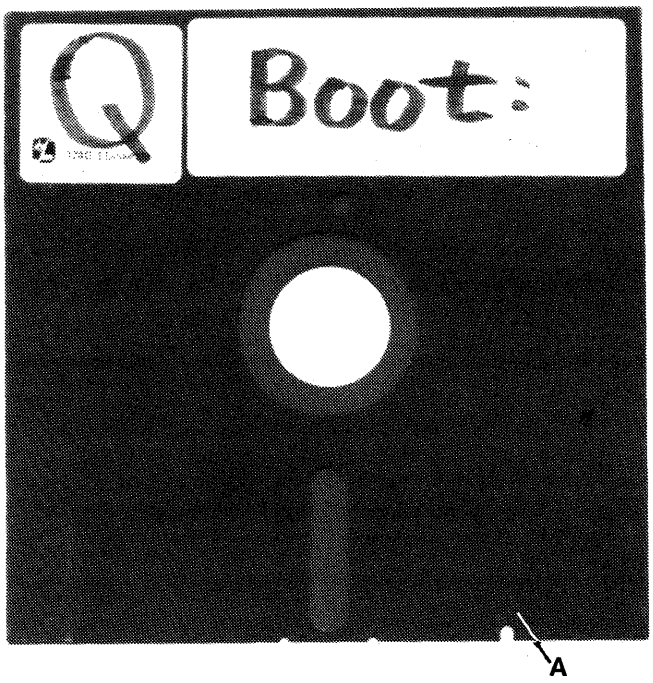
WARNING: Do not operate the PDQ-3 if any fan is not running or the system will overheat.

5) Push the DC ON button to the on (in) position. The DC ON button should be lit.

6) Check to see that the Run button (front panel) is in the Run (out) position. The Run button should be lit after the DC power is on.

3.2.1 Bootstrapping UCSD Pascal (CPU Version PDQ-3/1)

Once the PDQ-3 has been powered up, it is ready to boot. Bootstrapping the UCSD Pascal system on the PDQ-3 requires the diskette labelled "BOOT", provided with the PDQ-3, and a scratch disk. The scratch disk must not be write-protected. If the diskette has a write-protect notch in the lower right corner (see Figure 3.2.0), the notch must be covered with the silver tape provided with the diskette before proceding.



A) Write-protect notch

Figure 3.2.0 The Diskette Write-Protect Notch

To bootstrap the PDQ-3:

1) Press the Reset button on the front panel.

2) Insert the "BOOT" disk into the left floppy disk drive as follows:

   a) For single-sided drives, press down on the lever below the left floppy disk drive. For double-sided drives, push in the bar below the door. The door of the drive will pop open.

   b) Holding the diskette at the label end, with the label up, slide the diskette into the left disk drive (see Figure 3.2.1) until the diskette touches the back of the drive.

   c) Push the door of the floppy disk drive back down to close it. The door will click audibly when it latches.

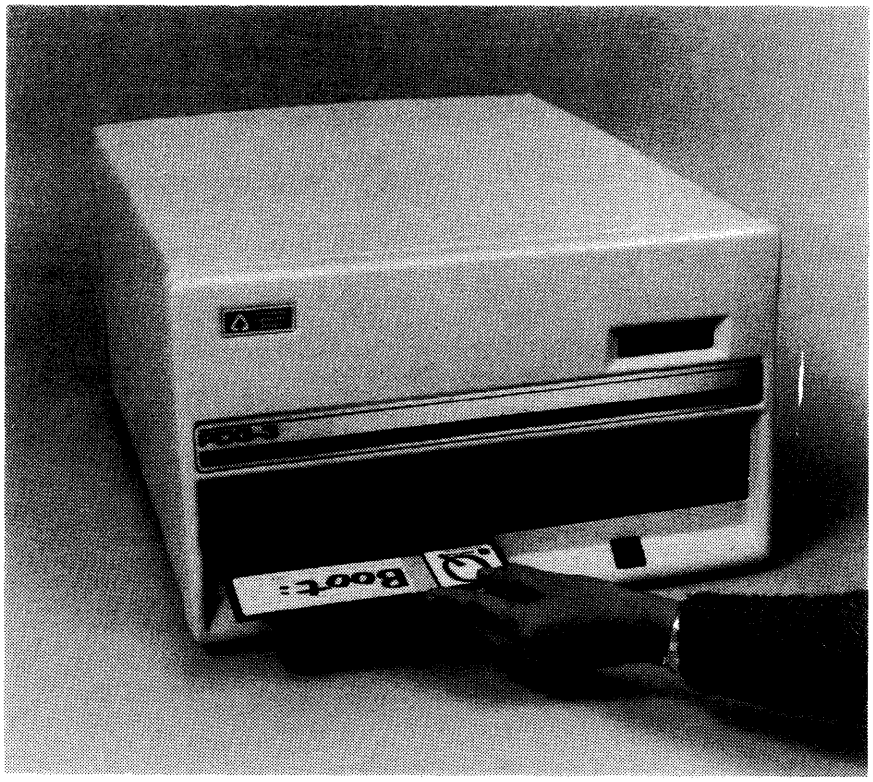


Figure 3.2.1 Inserting a Diskette

3) The PDQ-3 requires approximately fifteen(15) seconds to boot the UCSD Pascal System. The jumper options (see section 3.1.1) determine the state of the PDQ-3 after the Reset button is pressed:

   a) The PDQ-3 comes up in the HDT state, prompting the user with a '#' (see Appendix A for details on HDT). Once a bootable diskette has been inserted into the left floppy disk drive, the user can press R to boot the UCSD Pascal System.

   b) The machine comes up in an automatic bootstrap routine. Assuming a bootable diskette has been inserted in the left drive, the floppy disk drives should start running. If they do not, check to make sure the diskette has been inserted correctly, and that the Run/Halt button (front panel) is in the Run (out) position. Also check that the floppy control cable is securely connected to the CPU Module (refer to section 3.0 for details).

4) The "BOOT" disk will boot a configuration program. Undecipherable characters will appear on certain types of console CRTs. This problem will be cleared up once the screen is configured (later in the initial bootstrapping process). Read the text on the screen. The user is instructed to insert a scratch disk into the right-hand drive and press the carriage return key on the keyboard. The program will procede to make

a work disk from the scratch disk. Henceforth, this work disk should be used for booting, and the "BOOT" disk should be saved.

5) After the work disk is made, the program will prompt the user for the type of console CRT to be used with the PDQ-3.

6) The program has finished when "Done." appears on the screen. Remove the diskettes from the drives as follows:

   a) Press down on the lever below the drive. The door will pop open, and the edge of the diskette will be visible.

   b) Gently pull the diskette forward, out of the drive.

7) Insert the newly created work disk into the left-hand disk drive, and bootstrap it (starting at step 1 above). IT IS RECOMMENDED THAT THE BOOT DISK BE SAVED AND THAT THE WORK DISK BE USED HENCEFORTH.

3.2.2 Turning Power Off

To power down the PDQ-3:

1) REMEMBER TO REMOVE ALL DISKETTES FROM ALL FLOPPY DRIVES BEFORE POWERING UP OR DOWN.

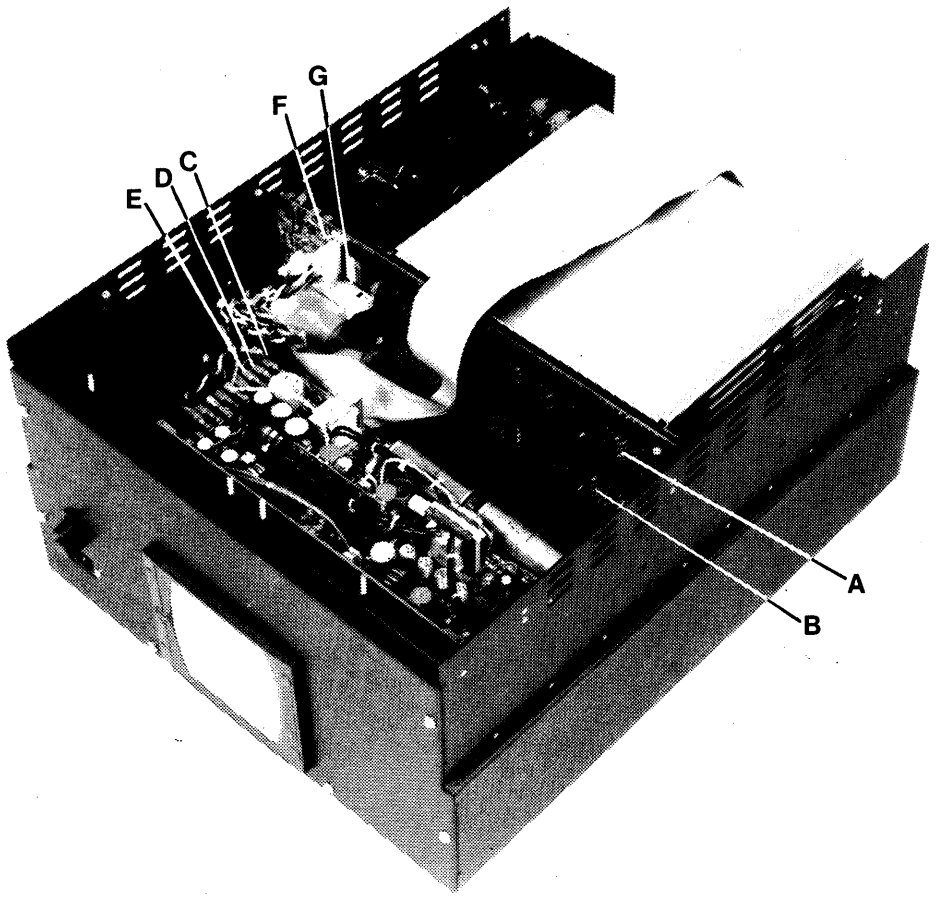
2) Turn off the DC power (front panel) by pressing the DC ON button. When the DC power is off, the DC ON button will be unlit.

3) Turn off the AC power (rear panel) by flipping the AC power switch down.

3.3 Disassembling the PDQ-3 System

IMPORTANT: To avoid possible electrical shock, always disconnect the AC power cable (rear panel) before disassembling the PDQ-3.

To disassemble the PDQ-3, begin by opening the chassis. This procedure is described in section 3.0.1. The backplane(s) and secondary power supply (if there are two backplanes) will then be exposed (see Figure 3.3.0).



A) Primary backplane
B) Secondary backplane
C-E) Primary power supply AC input cables
F) Primary backplane power supply cable
G) Backplane interconnect cable

Figure 3.3.0 Backplanes and Secondary Power Supply

3.3.0 Removal of Secondary Power Supply

The secondary power supply sits behind the backplane and above the primary power supply (see Figure 3.3.0).

1) Remove the six(6) rear panel screws, two(2) on each side, and two(2) on the bottom. The rear panel will now fold down (see Figure 3.3.1).

2) To remove the plate separating the primary and secondary power supplies:

   a) Unplug the secondary power supply from the backplane.

   b) There are three(3) wires that run from the secondary power supply, through a slot in the plate, down to the AC connector strips. These wires are: black for AC In

(hot), white for ACC In (neutral), and green for GND (ground). Disconnect these three wires from the power supply.

c) Remove the four(4) screws that secure the plate to the chassis and slide the plate out towards the rear of the chassis.

The primary power supply should now be exposed.

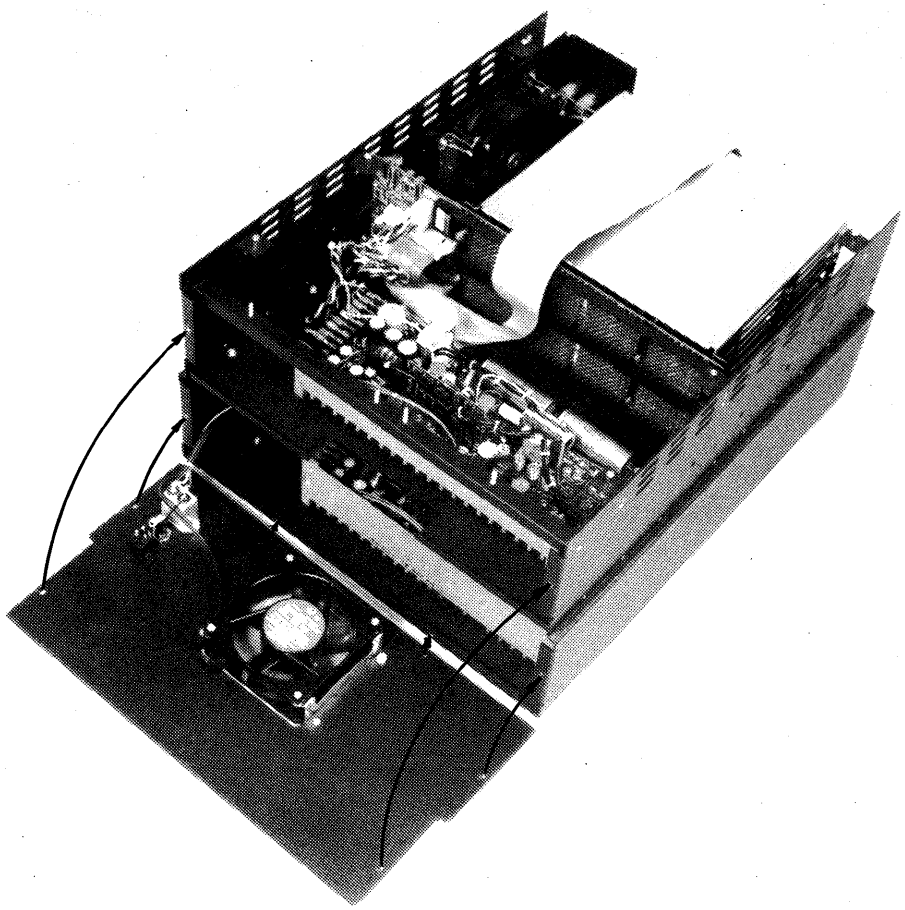


Figure 3.3.1 Removing the Rear Panel

3.3.1 Removal of Primary Power Supply

The primary power supply sits in the bottom of the chassis, back-to-back with the floppy disk drives. Once the secondary power supply has been removed (see section 3.3.0), the primary power supply may be removed for replacement as follows:

1) Disconnect the primary power supply from the primary backplane by unplugging the DC power cable.

2) Disconnect the primary power supply from the AC distributing

strip by disconnecting the black, white and green wires.

3) Disconnect the primary power supply from the floppy disk drive DC power cable.

4) There are four(4) screws on the bottom of the chassis for the power supply (see Figure 3.3.2). Remove these screws.

5) Slide the power supply out of the rear of the chassis.

3.3.2 Removal of Floppy Drives

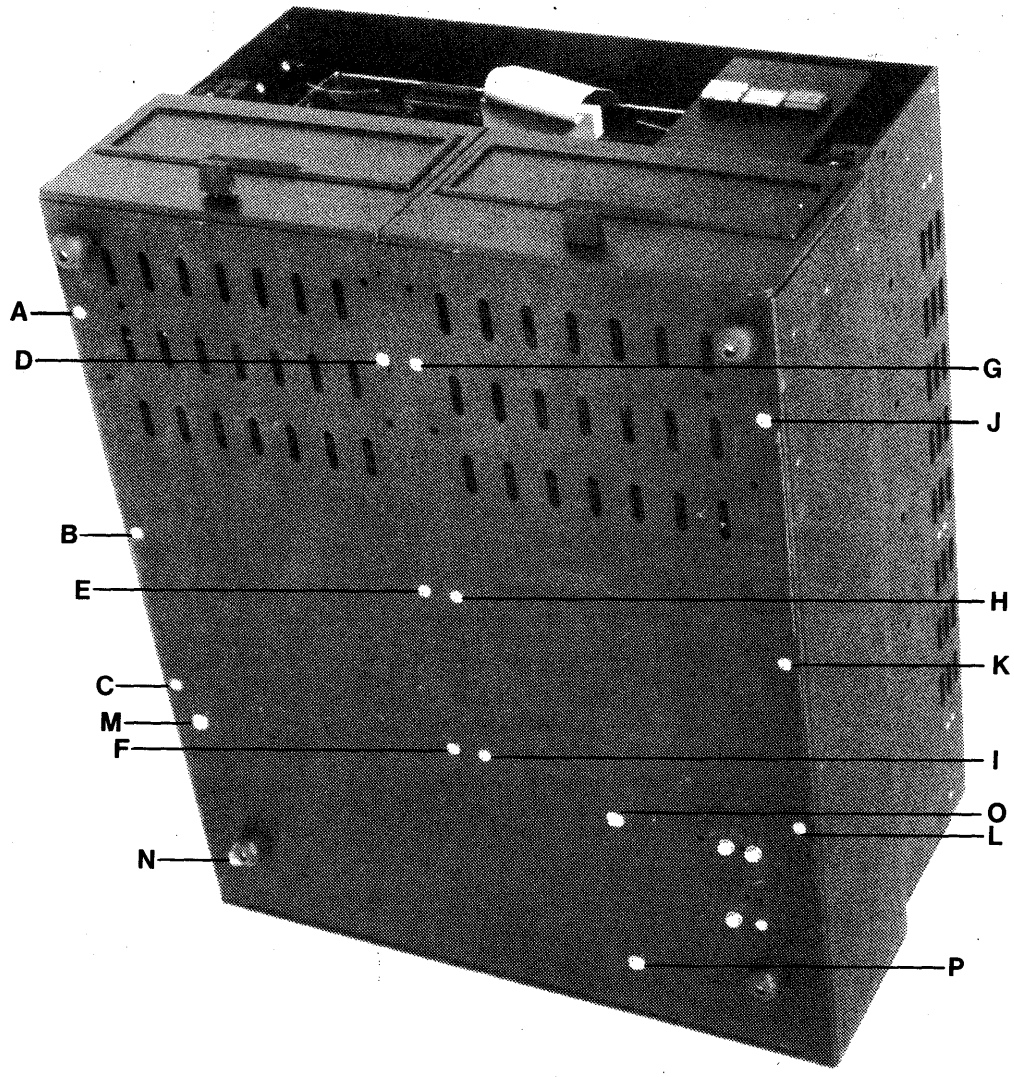
The floppy drives sit in the bottom of the chassis, back-to-back with the primary power supply. The floppy disk drives may be removed for replacement as follows:

1) There are six(6) screws on the bottom of the chassis for each drive (see Figure 3.3.2). Once these are removed, the drive(s) should be slid toward the front of the chassis far enough to disconnect any cables from the drive(s).

2) Disconnect the floppy control cable from the drives.

3) Disconnect the AC and DC power cables from the drives.

4) Slide the drive(s) out the front of the chassis.



A-F) Screws for Floppy Drive Unit #0
G-L) Screws for Floppy Drive Unit #1
M-P) Screws for Primary Power Supply

Figure 3.3.2 The Bottom of the Chassis

4. THE PDQ-3 SYSTEM COMPONENTS

The PDQ-3 System consists of the Rear Panel, the Front Panel, the Floppy Drives, the Backplane(s), the Power Supplies and the PDQ-3 CPU Module. This chapter discusses each component, except for the CPU Module, in detail. Discussion of the CPU Module is deferred to chapter six.

4.0 The Rear Panel

The Rear Panel consists of the AC input and EMI filter, AC fuse, AC ON/OFF switch, and the model specifications (see Figure 3.0.0.B).

4.0.0 The Model Specifications

The Model Specification Label is located on the lower right hand corner of the Rear Panel. It contains the following information:

1) The model number: the specific version of the PDQ-3 Computer System (see section 2.0.1).

2) System serial number: the serial number of the PDQ-3 Computer System.

3) AC rating: the AC voltage, maximum current and frequency required to operate the PDQ-3 Computer System.

WARNING: Do not connect the computer to any AC source with a different power rating than that of the computer or serious damage will result.

4.0.1 The AC Input and EMI Filter

The AC Input and EMI filter are located in the lower left hand corner of the Rear Panel. The AC Input supplies all the AC power to the system via the power cord supplied with the system. The AC Input contains an internal EMI filter which acts as a noise filter for all incoming AC power. Before connecting the AC Input to an AC source, there are several safety precautions that should be taken:

1) Make sure the AC power switch is OFF.

2) Verify that the AC ratings of the system, which may be found on the Model Specifications Label mounted on the Rear Panel of the PDQ-3, match the AC ratings of the intended wall socket.

3) Make sure that the PDQ-3 is completely assembled, with all electrical components securely connected.

4.0.2 The Fuse Holder

The fuse holder contains the main system AC power fuse. To replace the fuse, first make sure the AC power switch is in the off position, then remove the fuse holder cap by turning it counter-clockwise while pushing in. Replace the fuse with another of the same rating only. Then, replace the fuse holder cap by turning it clockwise while pushing in.

4.0.3 The AC ON/OFF Switch

The AC ON/OFF Switch is the main AC power control of the system. When it is switched on, AC power is applied to the floppy disk drive motors, the cooling fans, and the power supplies. At this point, the floppy drives and the fans should be active. The power supplies, however, remain in the standby mode until the DC ON/OFF Switch on the Front Panel is depressed.

WARNING: Before switching on AC power, make sure the DC ON/OFF Switch on the Front Panel is OFF. Do not use the system if any fan is not active after the AC ON/OFF Switch is switched on, or the system will overheat.

4.1 The Front Panel

The front panel consists of the Operator's Console and Floppy Disk Drives 0 and 1.

4.1.0 The Operator's Console

The Operator's Console is located in the upper right corner on the front panel of the computer (see Figure 3.0.0.A). It consists of three push-button switches and their light indicators. The functions of these switches, from right to left, are:

1) DC ON switch. This is a one break and one make switch. When it is in the OUT position, and the indicator light is off, all DC power supplies are in the standby mode. When the switch is IN, the red indicator light is ON, and all DC power supplies are enabled, supplying +5V, +12V, and +24V DC power to the system. If the indicator light fails to turn on, one of the following conditions is indicated:

   a) No AC is present. Check the AC ON/OFF switch, the power cord, and the fuse (see section 4.0.2).

   b) +12V DC is missing. This may be caused either by a primary power supply malfunction or a short circuit condition within the computer system.

   WARNING: Always remove diskettes from the floppy drives before switching DC ON or OFF. Do not turn DC power on if the fans are not running, or a system overheat may

occur.

2) RUN switch. This is a one break and one make switch. When the switch is in the OUT position, the CPU is in RUN mode, and the yellow indicator light is ON. When the switch is IN, the CPU is in HALT mode, and the light is OFF. In HALT mode, all CPU operations are suspended. However, interrupts are latched, and DMA operations from peripheral controllers may continue.

3) RESET switch. This is a momentary contact switch. It is normally in the OUT position. When it is depressed, the computer system is reset and will remain so until the switch is released. This switch contains a green LED, which is used to display the state of the system bus. If the LED is off, it indicates that the system is inactive. It will go off whenever the RESET switch is depressed, but it may be on when the Run/Halt switch is depressed, due to DMA operations. The LED will remain ON for the active period of the bus control synchronization signal BSYNC. However, it will be turned off if the active period of BSYNC is longer than 20 microseconds.

4.1.1 The Floppy Disk Drives

Either single-sided or double-sided disk drives may be installed in the PDQ-3 computer. Double-sided drives differ from single-sided drives as follows:

1) Double sided drives allow both sides of a diskette to be used for data storage.

2) Double sided drives are equipped with a Drive Access LED indicator light mounted on the Diskette Ejector. This LED is lit whenever the drive is selected by the Floppy Drive Controller.

In systems that include Floppy Disk Drives, Drive 0 is located in the lower left hand corner of the Front Panel; Drive 1 is located in the lower right hand corner. For insertion and removal of diskettes from the disk drives, refer to section 3.2.1. Drive 0 corresponds to UCSD system unit #4 and should contain the UCSD Pascal operating system diskette. Drive 1 corresponds to system unit #5.

4.2 The Backplane Module

The Backplane Module is fastened to the card rack by two screws, and is the link that transmits Q-Bus signals (see chapter 5) to all the parts of the system. It contains:

1) The eight dual-size slot LSI-11/23 Bus Connector blocks and 3 resistor packs and IC sockets for bus termination.

2) The LSI-11/23-compatible power-up/power-down sequencing logic

(primary backplane only).

3) The backplane module expansion connector.

4) The -12V DC to DC converter (primary backplane only).

5) The DC power input connector.

6) The battery backup power input connector.

7) The Operator's console input connector (primary backplane only).

4.3 The Power Supply Module

For information on the power supply module, please refer to the power supply manual provided with this manual.

5. THE Q-BUS

The DEC LSI 11/23 Q-bus is an electrical signal convention utilized by the DEC LSI family of computers to communicate with memory and peripherals also implementing the convention. The electrical signals presented to the backplane by the PDQ-3 CPU module conform to the Q-bus conventions, thus facilitating communication between the PDQ-3 CPU Module and memory or any other Q-bus compatible peripheral in the backplane.

The Q-bus comprises an 18-bit multiplexed address and data bus, Q-bus control signals, power, and ground. It enables memory and controller modules, which operate at different speeds, to communicate with each other by an interlocking handshaking protocol. This protocol includes data input and output in either word or byte modes, processor service interrupt requests, and direct memory access (DMA) bus requests.

The PDQ-3 CPU Module is the default Q-bus master, but a Q-bus compatible I/O device controller may request and be granted temporary control of the bus for a DMA operation. The PDQ-3 CPU module is compatible with all devices designed to operate on the LSI 11/23 Q-bus.

Both interrupt requests and the DMA requests are prioritized using a daisy-chain method. The controller that is electrically closer to the processor has the higher priority (see section 3.1.2). The bus is designed so that any bus-compatible module may be inserted into any bus location and still receive interface signals. However, the module's priority will change according to its location relative to the processor.

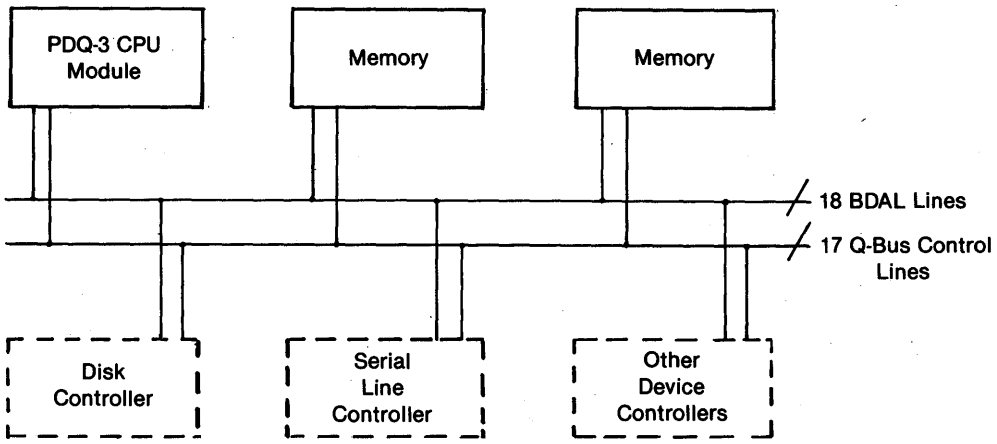
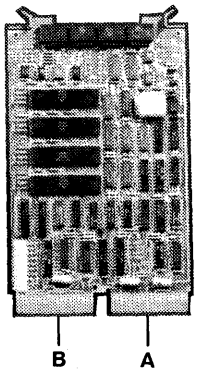


Figure 5.0.0 Q-Bus

5.0 Module Bus Connection Pin Identification

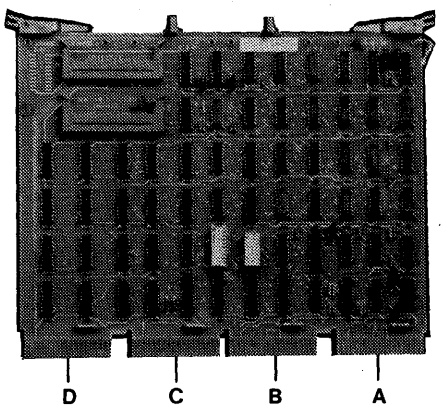
The Q-Bus accepts both dual size and quad size modules (see Figures 5.0.1.A and 5.0.1.B). A dual size module requires two slots on the backplane module (slots A & B or C & D); a quad size module requires four slots on the backplane module (slots A, B, C, and D). Each slot contains 36 connection pins: 18 on the component

side of a module (side 1), and 18 on the solder side (side 2). Each pin in a slot is identified by a letter of the alphabet from A to V (excluding G, I, O, and Q), starting from the right on the component side. Hence, the rightmost pin of slot A on the component side is AA1. The first A refers to Slot A; the second A refers to Pin A; the number 1 refers to the component side. Likewise, the third pin from the right, on slot D, on the solder side, is DC2.



A) Slot A B) Slot B

Figure 5.0.1.A Dual Size Module Configuration



A) Slot A C) Slot C
B) Slot B D) Slot D

Figure 5.0.1.B Quad Size Module Configuration

The bus is designed so that corresponding pins of slots A and C, and slots B and D, are assigned identical signal names. For example, the bus synchronization control signal (BSYNC L) is assigned both to pin AJ2 and CJ2. Note that modules are polarized by a notch between two adjacent slots. This notch acts as a key to mate with a protrusion on the connector block for correct module positioning. Table 5.0 lists the backplane pin assignments for slots A and B. The pin assignments for slots C and D are identical

to those for slots A and B.

NOTE: The trailing L (low) or H (high) of a signal mneumonic indicates the active state of the signal.

Table 5.0
Backplane Pin Assignments

Bus pin	Mnemonic	Description
AA1	BSPARE1	
AB1	BSPARE2	Unassigned bus spares.
AC1	BAD16	
AD1	BAD17	Extended address bits.
AE1	SSPARE1	
AF1	SSPARE2	Unassigned, unbussed special spares.
AH1	SSPARE3	Available for user interconnections.
AJ1	GND	System signal ground and DC return.
AK1	MSPAREA	Maintainence spares. Normally connected
AL1	MSPAREA	on the backplane at each option location.
AM1	GND	System signal ground and DC return.
AN1	BDMR L	Direct Memory Access (DMA) Request. A device asserts this signal to request control of the bus. The CPU arbitrates bus mastership between itself and all the DMA devices on the bus. If the processor is to relenquish bus mastership it grants bus mastership to the electrically closest requesting device by asserting BDMGO L. The device responds by negating BDMR L and asserting BSACK L.
AP1	BHALT L	Processor halt. When BHALT L is asserted, the processor responds by halting normal program execution. Interrupts are latched, and DMA request/grant sequences are enabled.
AR1	BREF L	Memory refresh. Not used by the PDQ-3.
AS1	PSPARE3	Unassigned spare. Usage not recommended.
AT1	GND	System signal ground and DC return.
AU1	PSPARE1	Unassigned spare. Usage not recommended.
AV1	+5B	+5V battery power. Secondary +5V power connection. Battery power may be used with certain devices.

BA1	BDCOK H	DC power ok. Asserted by the power up/down sequence logic of the primary backplane when there is sufficient DC voltage available to reliably sustain system operation.
BB1	BPOK H	Power ok. Asserted by the power up/down sequence logic of the primary backplane when power supply is normal. If negated during processor operation, a power fail interrupt sequence is initiated.
BC1	SSPARE4	
BD1	SSPARE5	
BE1	SSPARE6	
BF1	SSPARE7	Unassigned, unbussed special spare.
BH1	SSPARE8	Available for user interconnections.
BJ1	GND	System signal ground and DC return.
BK1	MSPAREB	Maintainence spare. Normally connected on the backplane at each option location.
BL1	MSPAREB	
BM1	GND	System signal ground and DC return.
BN1	BSACK L	Slave acknowledgement. Asserted by a DMA device in response to the processor's BDMGO L signal, indicating that the DMA device is the new bus master.
BP1	BSPARE6	Unassigned bus spare.
BR1	BEVNT L	External event interrupt request. Not used by the PDQ-3.
BS1	PSPARE4	Unassigned spare. Usage not recommended.
BT1	GND	System signal ground and DC return.
BU1	PSPARE2	Unassigned spare. Usage not recommended.
BV1	+5	+5V DC system power.
AA2	+5	+5V DC system power.
AB2	-12	-12V DC power.
AC2	GND	System signal ground and DC return.
AD2	+12	+12V DC system power.
AE2	BDOUT L	Data output. Asserted by the bus master to imply that valid data is available on BDAL0-15 L and that an output trans-

		fer is taking place. To complete the transfer, the addressed device must acknowledge the receiving of data by asserting BRPLY L in response to BDOUT L.
AF2	BRPLY L	Reply. Asserted in response to BDIN L or BDOUT L and during interrupt acknowledge. It is generated by an addressed device to indicate that the device has input data available on the BDAL bus or that it has accepted output data from the bus.
AH2	BDIN L	Data input. BDIN L is used for two types of bus operations: 1) When asserted by the bus master during BSYNC L time, implies an input transfer and requires a response. BDIN L is asserted when the master device is ready to accept data from a addressed device. 2) When asserted without BSYNC L, it indicates that an interrupt operation is in progress.
AJ2	BSYNC L	Synchronize. Asserted by the bus master to indicate that it has placed an address on BDAL0-15 L and intiate an input or output bus cycle. The cycle is in progress until after the master receives BRPLY L from the addressed device.
AK2	BWTBT L	Write/byte. BWTBT L is used in two ways to control a bus cycle: 1) It is asserted during the leading edge of BSYNC L to indicate that an output sequence is to follow, rather than an input sequence. 2) It is asserted during BDOUT L, in a DATO bus cycle, for byte addressing.
AL2	BIRQ L	Interrupt request. A device asserts this signal when its interrupt enable and interrupt request flip-flops are set. This signal informs the processor that a device needs processor service. The processor acknowledges the request by asserting BDIN L and BIAKO L.
AM2 AN2	BIAKI L BIAKO L	Interrupt Acknowledge Input and Interrupt Acknowledge Output. This signal is generated by the processor in response to an interrupt request (BIRQ L). The processor asserts BIAKO L, which is

		routed to the BIAKI L pin of the first device on the bus. If that device is not asserting BIRQ L, the device will pass BIAKI L to the next lower priority device via its BIAKO L pin and the lower priority device's BIAKI L pin. If it is requesting an interrupt, it will not assert BIAKO L.
AP2	BBS7 L	Bank 7 select. Asserted by the bus master when an address in the upper 4K words (addresses F000 hex to FFFF hex) is placed on the bus. This address space is normally reserved for memory mapped I/O. BSYNC L is then asserted and BBS7 L remains active during the addressing portion of the bus cycle.
AR2 AS2	BDMGI L BDMGO L	DMA Grant Input and DMA Grant Output. This processor generated signal grants bus mastership to the highest priority DMA device on the bus. The processor routes the BDMGO L signal to the BDMGI L pin of the first device on the bus. If this device is not requesting bus control, it passes the signal to BDMGI L pin of the next device on the bus. However, if the device is requesting bus control, it will inhibit the passage of the BDMGO L signal to the next device.
AT2	BINIT L	Initialization. Asserted by a) the processor or b) the RESET switch on the front panel or c) the primary backplane during the power up/down logic sequence to clear or initialize all devices in the system.
AU2 AV2	BDAL0 L BDAL1 L	Data/Address Lines. These two lines are part of the 18-line data/address bus over which data and address information is transmitted. Address information is first placed on the bus by the bus master device. Then the master device either receives data from, or outputs data to the addressed device or memory over the same bus lines.
BA2	+5	+5V DC system power.
BB2	-12	-12V DC power.

BC2	GND	System signal ground and DC return.
BD2	+12	+12V DC system power.
BE2	BDAL2 L	
BF2	BDAL3 L	
BH2	BDAL4 L	
BJ2	BDAL5 L	
BK2	BDAL6 L	
BL2	BDAL7 L	
BM2	BDAL8 L	
BN2	BDAL9 L	
BP2	BDAL10 L	
BR2	BDAL11 L	
BS2	BDAL12 L	
BT2	BDAL13 L	Data/Address Lines. These 14 lines are
BU2	BDAL14 L	part of the 18-line data/address bus
BV2	BDAL15 L	described for BDAL0 and BDAL1.

5.1 Bus Cycles

Each processor instruction requires at least one I/O operation. The first is a data input, which fetches an instruction from the location addressed by the program counter. This operation is called a DATI bus cycle. If no additional operands are referenced in memory or in an I/O device, no additional bus cycles are required for instruction execution. However, if additional memory or devices are referenced, additional data input/output or data transfer cycles are required. Between processor bus cycles, the bus is available for DMA access. In addition, interrupt requests may be serviced prior to instruction fetches. The following sections describe the types of bus cycles. It should be noted that the bus sequences for I/O operations between processor and memory or I/O devices are identical.

5.1.0 DATI Operations

The DATI cycle (see Figure 5.1.0) is asynchronous and requires a response from the addressed device or memory. An address is put onto the BDAL lines, and the BSYNC L signal is asserted. The addressed device or memory responds to an input request (BDIN L) by putting the data on the bus lines and then asserting BRPLY L. Upon receiving BRPLY L, the processor terminates the cycle by negating BDIN L and BSYNC L. If BRPLY L is not asserted within 15 microseconds after BSYNC L, the processor terminates the DATI operation, and executes a bus-error interrupt through location 2.

(Provided as addendum)

Figure 5.1.0 DATI Sequence

5.1.1 DATO Operations

The DATO cycle (see Figure 5.1.1) is asynchronous, and requires a response from the addressed device or memory. An address is put onto the BDAL lines and the BSYNC L signal is asserted. BWTBT L is asserted during the addressing portion of the cycle to indicate that an output data transfer is to follow. If a DATOB (DATO Byte) is to be executed, BWTBT L remains active for the rest of the bus cycle. However, if a DATO is to be executed, BWTBT L is negated and remains so for the rest of the bus cycle. The addressed device or memory responds to an output request (BDOUT L) by accepting the data and then asserting BRPLY L. Upon receiving BRPLY L, the processor terminates the cycle by negating BDOUT L and BSYNC L. If BRPLY L is not asserted within 15 microseconds after BSYNC L, the processor terminates the DATO operation, and executes a bus-error interrupt through location 2.

(Provided as addendum)

Figure 5.1.1 DATO Sequence

5.2 DMA Operations

DMA I/O operations involve both memory and peripheral devices. These devices may transfer data to or from any address in the address space, including the I/O addresses. The sequence of operations involved in executing a DMA data transfer is as described for input and output bus cycles (see section 3.1), except that the DMA device, not the processor, is the bus master. Memory addressing, timing, and control signal generation and response are provided by the logic contained on the DMA device's interface module. The processor is not involved with address or data transfers during such operations. Figure 5.2.0 illustrates in detail how a DMA bus request sequence occurs.

Note that because of the daisy chain involving the BDMGI L and the BDMGO L signals, all Q-Bus backplane slots between the processor and the DMA module must be filled. Otherwise, the daisy chain is broken and no DMA grant is received.

(Provided as Addendum)

Figure 5.2.0 DMA Bus Request Sequence

5.3 Interrupts

Interrupts are requests made by peripheral devices which cause the processor to temporarily suspend its program execution in order to service the interrupting device. Each device has its own service routine which it enters once its interrupt request has been acknowledged by the processor. After completion of this routine, program control is returned to the interrupted program. Such

interrupts are very useful when dealing with peripheral devices that operate much more slowly than the processor itself.

A device may generate an interrupt request at any time, however, it can interrupt the processor only when interrupts are enabled and the device is the electrically closest interrupting device to the processor on the bus. When the interrupt sysyem is disabled, interrupts are latched but not serviced. Interrupt nesting to any level is possible.

Associated with each device is an interrupt vector that is hard-wired into the device's interface/control logic. This vector is an address pointer that allows automatic entry into a service routine without device polling. A device interrupts the processor by asserting BIRQ L. The processor acknowledges the interrupt by asserting BIAKI L. A DATI bus cycle is then executed to cause the interrupting device to transfer the interrupt vector address into the BDAL lines.

Note that because of the daisy chain involving the BIAKI L and the BIAKO L signals, all Q-Bus backplane slots between the processor and the interrupting module must be filled. Otherwise, the daisy chain is broken and no interrupt acknowledge will be received.

(Provided as Addendum)

Figure 5.3.0 Interrupt Timing Sequence

5.4 Bus Initialization

The Q-Bus control signal BINIT L is asserted whenever the RESET button on the front panel is drpressed. It will hold the system in the initialized state until the button is released. The ability to reset the system without powering the system down is not available in DECs Q-Bus line of computers. This feature is incorporated by ACD to facilitate system reset without powering down, and hence preventing a loss of data. However, some devices, such as an intelligent DMA controller, may lock up the bus if a manual asynchronous reset is generated while DMA operations are being performed. In this case, a system power down is necessary to reinitialize the controller.

The system may also be reset under software control. In this case, every device on the bus, except the CPU chip set, is initialized. This is accomplished by setting the INIT bit of the System Status Register (see section 6.7).

5.5 Power-up/Power-down Sequence

The power status signals BPOK H and BDCOK H are used to control a power up or power down sequence as power is applied or removed, so that the system may carry out an orderly start up or

shut down.

During a power up sequence, BPOK H, BDCOK H, and BINIT L are low. Approximately 3 milliseconds after the DC power supply (supplies) outputs rise to their proper voltage levels and are stable, the power supply (supplies) asserts the signal PF. Upon receiving PF, the primary backplane power up/down logic sequence drives both BDCOK H and BINIT L high. After a delay of another 70 milliseconds, the logic drives BPOK H high. At this point, the PDQ-3 CPU processor begins to execute its power up routine.

A power down sequence occurs when the power supply (supplies) detects the AC power dropping below its operating limit. The power supply (supplies) begins the sequence by negating PF. This causes BPOK H to be negated and causes the processor to execute a power fail interrupt through word location 6. Approximately 3 milliseconds later, the primary backplane logic drives both the BDCOK H and BINIT L low.

5.6 Halt Mode

The processor is placed in Halt mode by asserting BHALT L low. While the processor waits for negation of BHALT L, DMA requests and refresh operations still occur, and interrupts are latched, but not executed.

5.7 Memory Refresh

The PDQ-3 CPU Module does not provide memory refresh control signals (BREF L is permanently negated). Thus, any dynamic semiconductor memory module used with the PDQ-3 must provide its own memory refresh logic.

5.8 Bus Configuration

The following sections describe methods of Q-Bus termination recommended for the PDQ-3 systems. Each Q-Bus signal (excluding the SPARE signals) is terminated by a 250 Ohm termination resistor on the CPU board (see Figure 5.8.0).

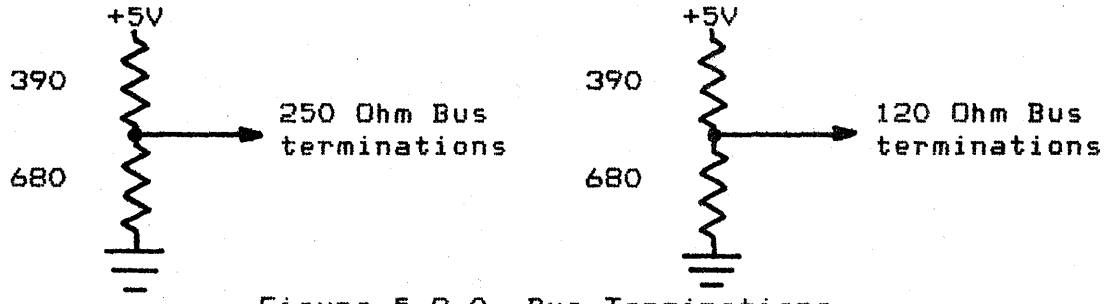


Figure 5.8.0 Bus Terminations

5.8.0 System with Primary Backplane Only

In this configuration, all necessary terminations are provided and configured at the factory as shown in Figure 5.8.1. Signal types MSPARE, SSPARE, and PSPARE are not terminated by the backplane. One unit load is defined to be one DEC bus receiver and two DEC bus drivers.

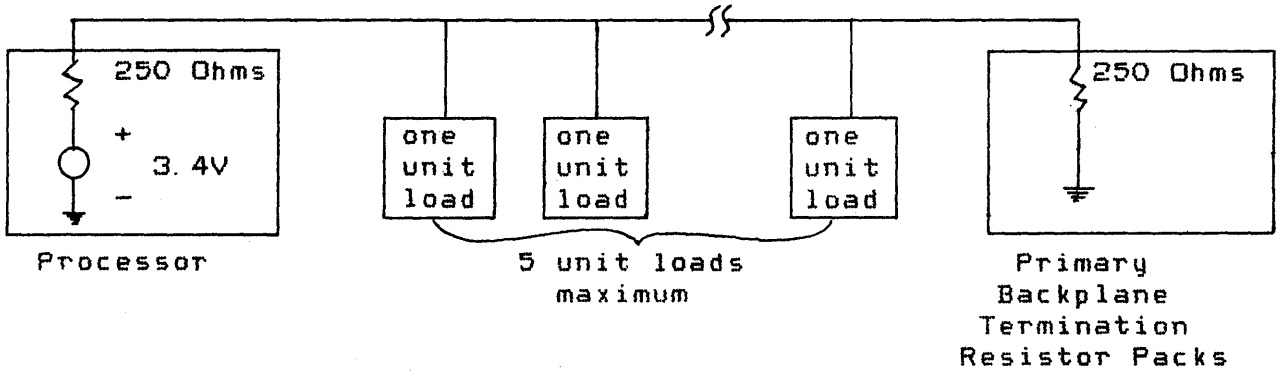


Figure 5.8.1 Bus Terminations for System with Primary Backplane Only

5.8.1 System with Both Primary and Secondary Backplanes

In this configuration, all necessary terminations are provided and configured at the factory as shown in Figure 5.8.2. The Primary and Secondary backplanes are interconnected by a 50 conductor ribbon cable. Signal types MSPARE, SSPARE, and PSPARE are not terminated by the backplane nor are they interconnected by the ribbon cable between the backplanes. One unit load is defined to be one DEC bus receiver and two DEC bus drivers.

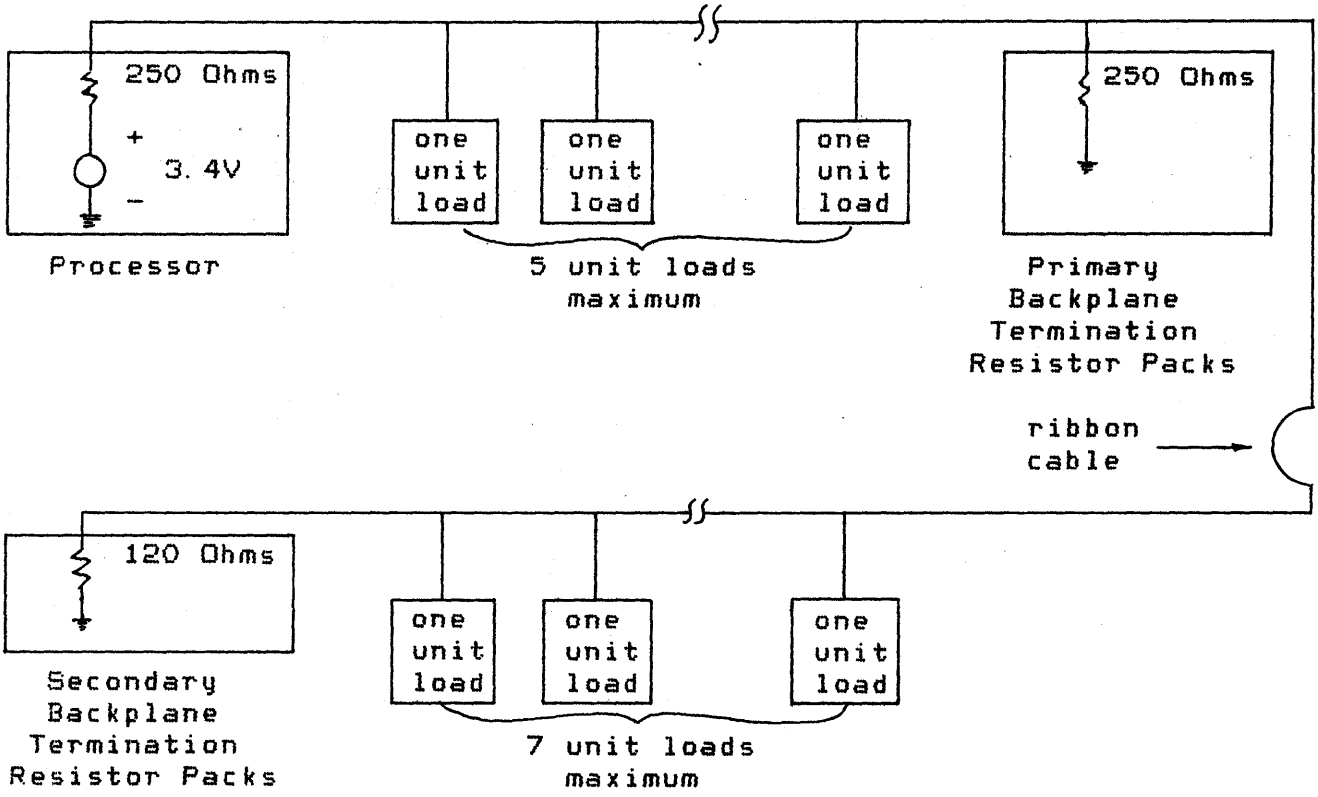


Figure 5.8.2 Bus Terminations for System with Primary and Secondary Backplanes

6 THE PDQ-3 CPU MODULE

This section describes the PDQ-3 CPU module. It contains descriptions of the CPU module internal WD-Bus, major CPU module components, and various internal architectural features.

The PDQ-3 computer module is electrically and mechanically compatible with the Digital Equipment Corporation LSI 11/23 Q-bus (described in chapter five; a superset of the LSI 11/03 Q-bus) and executes the UCSD version III.0 P-code. The module implements the following features:

A. Q-bus interface
B. Direct execution of UCSD version III.0 P-code
C. Real-time clock with programmable interval timer
D. Multiple unit floppy disk controller with DMA controller, data separator, and write pre-compensation
E. Non-existing device or memory detection
F. Power fail and recovery detection and interrupt
G. 1024 byte ROM with hardware debugger (HDT)
H. Vectored interrupts
I. DMA arbitration between multiple DMA devices
J. Programmable asynchronous serial I/O port
K. Programmed CLEAR function
L. Hardware NIL detection and interrupt

6.0 CPU Module Organization

The PDQ-3 CPU Module contains the WD 9000 MicroEngine processor chip set, a DMA Floppy controller, a USART, real time clocks, and a Q-bus interface. The processor uses the internal WD-Bus to communicate with each on-board device, and uses the Q-bus interface to communicate with any Q-Bus devices. Each on-board device is assigned an address location in a manner similar to devices on the Q-bus. Thus, communication between the processor and memory or I/O devices is routed first on the WD-Bus then, if necessary, through the Q-bus interface onto the Q-bus.

A 10 Megahertz crystal oscillator provides clocking for the processor and all on-board devices. A 2.5 Megahertz four phase clock is derived from it for the processor chip set.

6.1 Internal WD-Bus

The internal WD-Bus comprises 13 control signals and 16 multiplexed data/address signals (see Table 6.1). The processor is the default bus master and, using the WD-Bus, can control I/O between itself and any on-board or off-board device. The on-board DMA controller can also gain temporary control of the WD-Bus to transfer memory data to or from the Floppy disk controller.

Signal	Description
WDAL0:15	data/address lines
SYNC	bus syncronization
DIN	data in control
DOUT	data out control
REPLY	address acknowledge
W/R	write-not-read and byte control
BUSY	processor wait control
RESET	processor reset
COMP	processor active control
I0	interrupt request level 0
I1	interrupt request level 1 (not used)
I2	interrupt request level 2 (not used)
I3	interrupt request level 3 (not used)
IACK	interrupt acknowledge

Table 6.1 WD-Bus Signals

6.1.0 WD-Bus Data/Address Signals

The WDAL0 through WDAL15 lines carry either a 16 bit address, an 8 bit byte, or a 16 bit word of data depending on the state of the SYNC, W/R, DIN, DOUT, and REPLY control signals.

6.1.1 SYNC

The SYNC control signal is used to initiate a data access operation and to control its duration. SYNC is asserted high by the processor as soon as an address becomes valid on the WDAL lines. This occurs at clock phase 2 during execution of an input or output operation. It remains high until the termination of the operation.

If SYNC remains asserted longer than 15 microseconds, the bus error recovery logic is activated (see section 6.5).

6.1.2 DIN

The DIN (Data IN) signal is used by the processor to signal memory or an I/O device to put a byte or word on the bus. During a read operation, the processor asserts DIN high either at the time the address is secured from the WDAL lines or on the clock phase 2, following the assertion of SYNC (whichever is first). DIN is negated low at the end of the data input operation or when SYNC is negated low (whichever is first).

6.1.3 DOUT

The DOUT (Data OUT) signal is used by the processor to signal

the addressed device that data is stable on the bus. During a write operation, the processor asserts DOUT high during clock phase 1 when the write data is placed on the WDAL lines. It remains asserted for the duration of the write operation and is negated one clock phase prior to the removal of the data from the WDAL lines. The addressed device uses this signal to clock data appearing on the WDAL lines into its selected memory or register location.

6.1.4 REPLY

The REPLY signal synchronizes the processor to I/O operations, thus permitting devices to complete any required internal operations related to the I/O operation prior to the bus master's resumption of execution. Assertion of REPLY by a memory or I/O device signals the processor that the I/O device has gated data onto the bus in response to the assertion of DIN, or that the device has accepted the data in response to DOUT. The bus master interrogates the REPLY signal following execution of an input or output operation and enters the Wait state on each clock phase 3 until the REPLY signal is asserted by the addressed device. The WD 9000 processor also interrogates the REPLY signal prior to the execution of input or write operations at clock phase 3.

6.1.5 W/R

The W/R (Write-not-Read) signal is asserted high by the processor during the device selection sequence to signal the addressed device that a DOUT signal will follow immediately. The slave device may use the assertion or negation of W/R to initiate operations preparatory to an output or input operation, respectively.

The assertion of W/R during DOUT signals that a byte operation is being performed, and the WDAL8:15 lines are automatically forced to zero (required by the MicroEngine chip set).

6.1.6 BUSY

The BUSY signal is examined by the processor at clock phase 3 prior to an input or output operation. If BUSY is found asserted high, the processor enters the Wait state and does not attempt to use the WDAL bus lines or assert any control signals until BUSY is negated.

A DMA request from an I/O device causes BUSY to be asserted. It will remain asserted until the DMA operation completes and the DMA device relinquishes control of the bus.

6.1.7 RESET

Assertion of the RESET signal causes the processor to enter a reset state and tri-state both SYNC and DIN. Subsequent negation

of the RESET signal causes the processor to enter into the HDT bootstrap PROM.

6.1.8 COMPUTE

Assertion of the COMPUTE signal causes the processor to execute microinstructions. It is examined by the processor at each clock phase 1. If COMPUTE is found negated low, the processor enters the Wait state thereby ceasing execution of the microprogram. While in this state the processor continues to monitor the COMPUTE signal at each clock phase 1. When COMPUTE is found asserted high, the processor resumes execution of the microprogram. COMPUTE is low when the processor is put into the Halt mode by depressing the front panel "RUN" switch.

6.1.9 Interrupt Sense Lines

There are four interrupt sense lines, I0 through I3.

An I/O device makes an interrupt request by asserting I0. If the Interrupt Enable bit of the System Status Register (see section 6.7) is set (enabling interrupt requests), the processor microprogram enters an interrupt acknowledge sequence. This sequence first asserts IACK and SYNC, and then DIN, to which the interrupting device of the highest priority responds with its unique interrupt vector on the data lines.

The interrupt request lines I1, I2, and I3 are not used.

6.1.10 IACK

The IACK (Interrupt ACKnowledge) and SYNC signals are asserted high by the processor during clock phase 2 in response to an interrupt request appearing on I0. It remains asserted until the interrupting device responds with REPLY and the interrupt vector address on the data lines.

6.2 Processor Chip Set

The PDQ-3 CPU Module processor is a WESTERN DIGITAL CORPORATION WD9000 processor chip set. This set comprises the Control Chip, Data Chip and three Control Memory Chips. The Control chip and Data chip execute microcode found in the three Control Memory chips.

6.2.0 Control Chip

The control chip provides the thirteen control signals used to control the internal WD-bus (see section 6.1).

6.2.1 Data Chip

The Data Chip contains the arithmetic logic unit, the micro-instruction decode logic, and the internal processor register files. It controls the 16 WDAL signal lines described in section 6.1.

6.2.2 Control Memory Chips

The three Control Memory Chips contain the microinstructions necessary to emulate the UCSD Pascal version III.0 P-machine. The Software User's Manual provided with this document contains a description of the III.0 P-machine. Each memory chip provides 512 words of 22 bits apiece.

6.3 Interrupt System

An interrupt request on the IO control line, occurring with interrupts enabled, causes the processor to begin an interrupt sequence. Both the DIN and the IACK signals are asserted high at the beginning of this sequence. The assertion of DIN signals the highest priority device with an interrupt pending to gate its interrupt vector address onto the data lines and then assert REPLY. The processor then vectors an interrupt through this location.

The assertion of IACK causes the the Interrupt Enable bit of the System Status register (see section 6.7) to be reset. This permits whatever interrupt service routine is invoked by the interrupt condition to be executed without being interrupted. The service routine must re-enable interrupts at the appropriate time by setting the Interrupt Enable bit of the System Status register (see section 6.7).

The PDQ-3 CPU Module on-board devices are assigned an interrupt priority above that of the devices on the Q-Bus. The relative priorities of the on-board devices are shown in Table 6.3.

For details on how to write an interrupt routine in UCSD Pascal, refer to the SOFTWARE USER'S MANUAL.

DEVICE	VECTOR	PRIORITY
Bus Error	0002	0 (highest)
Power Fail	0006	1
DMA (and Floppy disk)	000A	2
Console Transmitter Ready	000E	3
Console Receive Data	0012	4
Printer Protocol	0016	5
System Clock	001A	6
Interval Timer	001E	7 (lowest)

Table 6.3 PDQ-3 Device Priority Assignment

The interrupt vector assignments of the standard Q-Bus devices, are listed in Appendix B.

6.4 Power Fail and Power Recovery

Power failure and power recovery are detected on the PDQ-3 by monitoring the Q-Bus signals BDCOK H and BPOK H. Assuming the system memory is non-volitile (either because of the type of memory used or because of battery backup), it is possible to recover from a power failure. When a power failure occurs, the Power Fail bit in the System Status register (see section 6.7) is set. If interrupts are enabled, an interrupt is vectored through location 6. Under these conditions, the system has approximately 3 ms to prepare for power failure.

When power is restored, the PDQ-3 enters a RESET state and the HDT prom is invoked (see Appendix A). If the memory can be determined to be intact, processing is resumed at the point of power failure. Note that the USART baud rate, the System clock rate, and the Interval Timer rate are reset to their initial values. If memory cannot be determined to be intact, the PDQ-3 is bootstrapped either into HDT or into the operating system according to the E12 jumper (see section 3.2.1).

6.5 Bus Error

A Bus Error on the PDQ-3 is triggered by an access to a non-existent memory or I/O device address. A device failing to respond to the assertion of SYNC causes the bus master to continue to assert SYNC. The duration of the SYNC signal is monitored by bus timeout logic. If SYNC persists beyond 15 microseconds, the Bus Error recovery logic is initiated. This logic sets the Bus Error bit in the System Status register (see section 6.7) and asserts REPLY to complete the cycle. If interrupts are enabled, an interrupt is vectored through location 2.

6.6 Interfacing the WD-Bus to the Q-Bus

The Data/Address lines and signals referred to in this section are described in detail in the sections on the Q-Bus (see chapter 5) and WD-Bus (see section 6.1).

The WD-Bus connects all modules internal to the CPU module. This bus interfaces to the Q-Bus through the Q-Bus interface. The on-board WD-Bus provides connections between:

1. the Processor Control chip (see section 6.2.0)
2. the Processor Data chip (see section 6.2.1)
3. the Real-Time Clock chip (see section 6.9)
4. the DMA Controller (see section 6.11.1)
5. the Floppy Disk Controller (see section 6.11.0)
6. the USART (see section 6.10)
7. the Bootstrap PROMs
8. the System Environment Switches (see section 6.8)
9. the System Status Register (see section 6.7)
10. the on-board Address Registers
11. the on-board Address Decoder
12. the WD-Bus Control Signal Buffer Drivers
13. the WDAL Buffer Drivers
14. the Processor Address Buffer Drivers

The WD-Bus Control Signal Buffer Drivers, the WDAL Buffer Drivers, and the Processor Address Buffer Drivers are necessary for electrical driving capacities. In addition, the Processor Address Buffer Drivers interface the CPU address with the Q-Bus BDAL address lines.

6.6.0 Address and Data Lines

When the CPU is the bus master, the WDAL lines carry word addresses. The Q-Bus BDAL lines always carry byte addresses. In order to interface a CPU word address to a Q-Bus byte address, the CPU address is shifted left one bit (doubled) by the Processor Address Buffer Driver. Hence, WDAL0 becomes BDAL1, and BDAL0 is always driven to 0.

When the DMA Controller is the bus master, the WDAL lines carry byte addresses. All addresses are buffered by the WDAL Buffer Drivers, and no shifting is necessary.

The WDAL lines are interfaced to the Q-Bus BDAL lines by standard DEC drivers, receivers and transceivers. Their Q-Bus timing sequence is derived from the 10 MHz master clock.

6.6.1 Control Lines

The WD-Bus control signals SYNC, DIN, DOUT, and W/R are mapped onto the Q-Bus as BSYNC, BDIN, BDOUT, and BWTBT by standard DEC drivers. The Q-Bus BRPLY signal is received by a standard DEC receiver, and controls the WD-Bus REPLY signal. COMPUTE is controlled by the Q-Bus BHALT L signal. It is negated when BHALT L is asserted. RESET is controlled by the Q-Bus signal BINIT L. It is asserted whenever BINIT L is asserted. The Q-Bus signal BBS7 is asserted during address time when address bits 13, 14, 15, and 16 are asserted. All Q-Bus timing is controlled by a timing sequence derived from the 10 MHz master clock.

6.6.2 Interrupt Lines

The Q-Bus interrupt signal BIRQ L is "OR"ed with other on-board device interrupt request lines to generate the WD-Bus IO signal. The Q-Bus signal BIAKO L is controlled by the WD-Bus IACK signal, which propagates through all on-board devices. If no on-board device is requesting interrupt service, BIAKO L will be asserted when IACK is asserted. Otherwise, the on-board device blocks the propagation of IACK and BIAKO L remains negated.

6.6.3 DMA Lines

The Q-Bus DMA request line BDMR L is "OR"ed with the request of the on-board DMA Controller to generate a DMA request to the processor. The DMA grant logic generates a bus grant signal, DMGO. This signal propagates through the on-board DMA Controller. If the DMA Controller is not requesting the bus, the Q-Bus signal BDMGO L is asserted when DMGO is asserted. Otherwise, the on-board controller blocks the propagation of DMGO and BDMGO L remains negated.

6.7 System Status Register

The System Status register is an 8-bit read/write register that provides information concerning the status of PDQ-3 CPU Module on-board devices, and the means effect certain controls over them. Its word address is FC24 (hex). It occupies the least significant byte of a 16-bit word; the most significant byte is undefined. The register is defined as follows:

BITS

7	6	5	4	3	2	1	0
INIT	INTEN	PRNT	PWRF	0	INTVL	TICK	BERR

WARNING: Storing a value into one particular bit of this register stores a value into ALL bits (probably zero). The implications of such a storage must be considered carefully.

1) BERR:

The BERR bit indicates a Bus Error condition. It is set to 1 after either memory or an I/O device fails to assert the bus signal REPLY within 15 microseconds of the assertion of the SYNC signal. A BERR condition also occurs as a result of setting the INIT bit of the System Status register to 1. If the interrupt system is enabled, a Bus Error condition causes a processor interrupt through the interrupt vector at location 2. The Bus Error condition must be cleared in order to satisfy the interrupt. The BERR bit is set to 0 by writing a 1 into BERR.

2) TICK:

The TICK bit indicates the System Clock counter (#1; see section 6.9) has counted down to 0. If the interrupt system

is enabled, a System clock 'tick' causes a processor interrupt through the interrupt vector at location 1A hex. The TICK condition must be cleared in order to satisfy the interrupt. The TICK bit is set to 0 by writing a 1 into TICK.

3) INTVL:

The INTVL bit indicates the Interval Timer counter (#2; see section 6.9) has counted down to 0. If the interrupt system is enabled, an Interval Timer 'tick' causes a processor interrupt through the interrupt vector at location 1E hex. The INTVL condition must be cleared in order to satisfy the interrupt. The INTVL bit is set to 0 by storing a 1 into INTVL.

4) bit 3:

This bit must be zero for the PDQ-3 to run correctly.

5) PWRF:

The PWRF bit is set to 1 when a Power Failure is imminent (the BPOK bus signal is negated). If the interrupt system is enabled, a Power Failure causes a processor interrupt through the interrupt vector at location 6. The PWRF condition must be cleared in order to satisfy the interrupt. The PWRF bit is set to 0 by writing a 1 into PWRF.

If, after clearing the PRWF condition, the PWRF bit is still set to 1, a complete power failure will occur within 3 milliseconds. In this case, the interrupt system should remain off, and the power failure interrupt handler should prepare for the power failure. Its last action should be to loop until the PWRF bit is set to 0. Assuming a recovery is possible (see section 6.4), the loop will be exited upon recovery.

6) PRNT:

The PRNT bit is a write-only bit which determines the ultimate destination of the USART transmit data. If a 0 is written into this bit, the USART transmit data is gated to the system console. If a 1 is written into this bit, the USART transmit data is gated to the printer (see section 6.10.1). The PRNT bit is always read as a 0.

7) INTEN:

The INTEN bit reflects the state of the PDQ-3 interrupt system. If the INTEN bit is set to 1, the interrupt system is enabled (see section 6.3). If the INTEN bit is set to 0, the interrupt system is disabled and all interrupts are latched. The state of the interrupt system can be changed by loading a different value into INTEN.

8) INIT:

When read, the INIT bit reflects the jumper status of the E12, E13, and the E14 jumpers. If E12 is is jumped to E13, the INIT bit is set to 0. If E14 is jumped to E13, the INIT bit is set to 1. The HDT prom program (see Appendix A) uses this value to determine the bootstrapping sequence.

When written to, the INIT bit is used as a bus reset control. Writing a 1 into this bit causes the assertion of the BINIT bus signal for 96 microseconds. During this period, the processor is placed in the BUSY state and all system devices are re-initialized. (The 8253 counter described in section 6.9 is the exception.)

6.8 Environment Switch

The Environment Switch is an 8 bit DIP switch (see Figure 3.1.0) used to communicate certain information about the hardware environment to the operating system. The value of the register may be read as the low order byte of the word at device address FC18 hex. The contents of the high order byte is undefined.

The DIP switches are defined as in Table 6.8.

NOTE: Bit 0 of the byte value corresponds to the dip switch marked '1'. A bit value of 0 corresponds to a dip switch in the closed (off) position.

Bits	Value	Meaning
7	1	Boot into HDT
6	-	Reserved for user applications
5	-	Reserved for user applications
4:3	00	Printer Speed is 110 baud
	01	Printer Speed is 300 baud
	10	Printer Speed is 1200 baud
	11	Printer Speed is 9600 baud
2:0	000	Console Speed is 19200 baud
	001	Console Speed is 9600 baud
	010	Console Speed is 4800 baud
	011	Console Speed is 2400 baud
	100	Console Speed is 1200 baud
	101	Console Speed is 600 baud
	110	Console Speed is 300 baud
	111	Console Speed is 110 baud

Table 6.8 DIP Switch Configuration

6.9 Real Time Clocks

Real time clock functions are provided by an Intel 8253 programmable counter/timer chip. This device provides three counter/timers: one for the USART Baud Rate clock, one for a 100 Hz System clock, and one for a programmable Interval Timer with a

range from 10ms to 10 minutes in 10ms increments.

The 8253 is driven by a 1.25MHz clock derived from the system 10MHz oscillator. This clock is used to strobe successive decrements of the System clock and Baud Rate clock counter registers. A clock "ticks" when its counter register reaches zero. The Interval Timer is decremented on successive "ticks" of the System clock.

The 8253 comprises four registers as shown in Table 6.9 and described below.

REGISTER	BITS	ADDRESS (word)	ACCESS
Baud Rate clock counter	8	FC20	Read/Write
System clock counter	8	FC21	Read/Write
Interval Timer counter	8	FC22	Read/Write
Mode Register	8	FC23	Write Only

Table 6.8 Real Time Clock Registers

6.9.0 Mode Register

The Mode Register controls the operation of each of the counters. The Mode Register format is shown below.

BITS

7	6	5	4	3	2	1	0
COUNT REG SEL	LOAD METHOD			MODE			0

1) COUNT REG SEL:
These two bits specify the counter to which the remaining mode control information is to apply:

00 = Baud Rate Clock counter
01 = System Clock counter
10 = Interval Timer counter
11 = Illegal

2) LOAD METHOD:
These two bits specify the method to be used in latching the initial contents of the specified counter register:

00 = Not used by the PDQ-3.
01 = Load the least significant byte of counter only.
10 = Load the most significant byte of counter only.
11 = Load the least significant byte first, followed by the most significant byte.

3) MODE:

These three bits specify the operating mode of the specified counter:

Counter	Recommended Mode
Baud Rate clock	010
System clock	010
Interval Timer	000 or 010

6.9.1 Using the Clocks

To program a clock counter, the mode for the counter is specified by loading the mode register, then the counter register is loaded. The mode characterizes the conditions under which the specified counter decrements and whether or not the counter restarts after reaching zero. On the PDQ-3, all counters start decrementing on the clock transition immediately following the last load necessary to initialize the counter. It is necessary to load the counter register either once or twice depending on whether one or two bytes of the counter are being initialized.

6.9.1.0 Baud Rate Clock

This counter creates the baud rate timing for the on-board USART. USART operation from 50 baud to 19,200 baud is possible. The base frequency of this counting register is 1.25MHz. The USART baud rate is set by loading the Baud Rate clock counter register with the baud factor (BF) where:

$$BF = 39066/B$$

'B' is in bits per second, and BF is rounded to the nearest integer. The Baud Rate clock is programmed (using mode 010) to restart itself when it counts down to zero, thus providing a steady pulse rate of the desired frequency.

The Baud Rate clock is normally initialized by the HDT ROM at system reset time according to the state of the Environment Switch Register (see section 3.1.1).

6.9.1.1 System Clock

This counter produces the 10ms pulses used by the PDQ-3 to provide a real time clock. The input clock rate to this counter is 1.25MHz. To generate the an arbitrary pulse rate, the System clock counter register is loaded with the Clock Factor (CF):

$$CF = 1250000 \times T$$

'T' is the pulse period in seconds. For example, to set the System clock to generate 10ms pulses, CF = 1250000 x .01 = 12500. Thus 12500 is loaded into the System clock counter register. The System clock is programmed (using mode 010) to restart itself when it counts down to zero, thus providing a steady pulse rate of the desired frequency.

When the System clock counter register counts down to zero, the System clock bit in the System Status register (see section 6.7) is set. If interrupts are enabled, an interrupt will be generated through location 1A hex.

6.9.1.2 Interval Timer

This counter is loaded by the system or application as required. The input clock to this counter is the System clock pulse. Assuming the System clock pulses at 10 ms intervals, the Interval Timer may be programmed to produce time-out intervals from 10ms to 10 minutes. To generate an arbitrary interval pulse, the Interval Timer counter register is loaded with the Interval Factor (IF), computed as follows:

$$IF = 100 \times I$$

'I' is the time-out interval in seconds. Thus, to generate a pulse of 1 second (IF = 100 x 1 = 100), the Interval Timer counter register is loaded with 100. The Interval Timer is programmed either to restart itself when it counts down to zero (using mode 010) or to terminate on the first pulse (using mode 000).

When the Interval Timer counter register counts down to zero, the Interval Timer bit in the System Status register (see section 6.7) is set. If interrupts are enabled, an interrupt will be generated through location 1E hex.

6.10 Console Controller

The PDQ-3 RS-232C Console Controller is a WD1931 USART located onboard the PDQ-3 CPU Module. It supports full duplex communication with the console at speeds ranging from 50 to 19,200 bits per second. Recommendations for cabling between the PDQ-3 CPU Module and the operator's console are found is Appendix D.

6.10.0 USART Registers

The USART provides five 8-bit interface registers. Communication with the USART registers may be carried on in either the word or byte mode. Significant data always occupies the low order byte, and the value of the high order byte is undefined.

Table 6.10 lists the USART registers accessable by the processor.

REGISTER	ADDRESS (Word)	ACCESS
Control Register #1	FC10	Read/write
Control Register #2	FC11	Read/Write
Status Register	FC12	Read only
Transmitter Holding Register	FC13	Write only
Receiver Holding Register	FC13	Read only

Table 6.10 USART Registers

6.10.0.0 Control Registers

The two 8-bit Control registers hold device programming information such as mode selection, interface signal control, and data format.

6.10.0.0.0 Control Register #1

The USART Control register #1 is used to define line protocol and data control functions. It is defined as follows:

BITS

7	6	5	4	3	2	1	0
LOOP	BRK	MISC	ECHO	PE	RE	RTS	DTR

1) LOOP:

The Loop/Normal bit allows all data sent to the transmitter to appear at the receiver, thus forming an internal diagnostic data loop. When this bit is set to 1, the loop is activated and ring interrupts are disabled. When this bit is set to 0, the ring interrupt is enabled and the USART is configured to operate in normal full duplex mode.

2) BRK:

The Break bit allows the transmitter output line to be held in a continuous space state starting at the next character. When this bit is set to 0 and the transmitter is enabled, the transmitter acts normally except that the transmitter output line is held in the spacing state.

3) MISC:

This bit determines the number of stop bits to be transmitted with each character. When this bit is set to 0, a single stop bit is transmitted. When this bit is set to 1, two stop bits are transmitted with each character 6, 7, or 8 bits long, and 1.5 stop bits for characters 5 bits long.

4) ECHO:

The Echo Mode bit allows data on the receiver input line to be duplicated on the transmitter ouput line. When this bit is set to 0 and the receiver is enabled, the clocked regenerated data is presented to the Transmitted Data output.

5) PE:

The Parity Enable bit enables checking of the parity on received characters and generation of parity on transmitted characters. When this bit is set to 0, parity checking/ generation is enabled. When this bit is set to 1, parity checking/generation is disabled.

6) RE:

The Receiver Enable bit controls the receiver logic. When this bit is set to 0, characters may be placed in the Receiver Holding register and Status register bits 1 through 4 may be updated. When this bit is set to 1, status bits 1-4 are cleared and the receiver is disabled.

7) RTS:

The Request To Send bit controls the data set CA circuit. This bit must be set to 0 and the Clear To Send input must be asserted for the transmitter to be enabled. When this bit is set to 1, the transmitter is disabled and the RTS output is turned off at the completion of any current character transmissions.

8) DTR:

The Data Terminal Ready bit controls the data set CD circuit. When set to 0, Carrier, Data Set Ready, and Ring interrupts are enabled. When set to 1, the Ring interrupt is enabled.

6.10.0.0.1 Control Register #2

The USART Control register #2 controls the data format and transmission/receive rates. It is defined as follows:

BITS

7	6	5	4	3	2	1	0
Char Length		Mode	Odd/Evn	RX Clk	Clock select		

1) CHAR LENGTH:

The Character Length bits select the number of bits per character as follows:

00 - five bits
01 - six bits
10 - seven bits
11 - eight bits

2) MODE:
The Character Mode bit configures the USART for asynchronous character mode. This bit is set to 1 on the PDQ-3. (Syncronous character mode is not used.)

3) ODD/EVN:
The Odd/Even bit determines the transmit/receive parity. When this bit is set to 0, odd parity is generated/expected. When this bit is set to 1, even parity is selected.

4) RX CLK:
The alternate RX clock bit determines the separate receive data clock rate. This feature is not used on the PDQ-3 and this bit must always be set to 0.

5) CLOCK SELECT:
These bits select the transmit and receive clocks, and must always be set to 110 on the PDQ-3. This allows the Baud Rate generator (see section 6.9.1.0) to determine both clock rates.

6.10.0.1 Status Register

The USART Status register contains information relating to the status of the USART. It is defined as follows:

BITS

7	6	5	4	3	2	1	0
DSC	DSR	CD	FE	PE	OE	DR	THRE

1) DSC:
The Data Set Change bit is set to 0 after a change in the state of either the DSR or CD control inputs (assuming the DTR bit in Control register #1 is programmed 0) or Ring control input (assuming the DTR bit in Control register #1 is programmed 1). This bit is set to 1 after the Status register is read.

2) DSR:
The Data Set Ready bit is the Data Set Ready control input from the Data Set.

3) CD:
The Carrier Detect bit is the Carrier Detect control input from the Data Set. On the PDQ-3, it is used to monitor the DTR signal of a printer when the serial port is multiplexed between a CRT and a serial printer.

4) FE:

The Framing Error bit is set to 0 if the receiver is enabled and the last character received is found not to have a stop bit. A framing error condition is cleared (this bit is set to 1) when the receiver is disabled then reenabled.

5) PE:

The Parity Error bit is set to 0 when the receiver and Receive Parity are enabled and the last received character has a parity error. A parity error condition is cleared (this bit is set to 1) when the receiver is disabled then reenabled.

6) OE:

The Overrun Error bit is set to 0 when a character has been received and is ready to be transferred to the Receiver Holding register, but DR is set to 0 (indicating that the processor has not responded to the last character). In this case, the newest character is lost. An overrun error condition is cleared (this bit is set to 1) when the receiver is disabled then reenabled.

7) DR:

The Data Received bit is set to 0 when the receiver is enabled and the Receiver Holding register is loaded from the Receiver. It is set to 1 when the Receiver Holding register is read by the processor or when the receiver is disabled.

8) THRE:

The Transmitter Holding Register Empty bit is set to 0 when the contents of the Transmitter Holding Register is transferred to the transmitter register and Transmitter is enabled. It is set to 1 when the Transmitter Holding Register is loaded by the processor or when transmitter is disabled.

6.10.0.2 Transmitter Holding Register

The Transmitter Holding register buffers data for transmission. When the transmitter is not busy and the transmitter is enabled, the contents of the Transmitter Holding register is transferred to the transmitter and a THRE condition is generated. Note that the Transmitter Holding register is loaded with the 1's complement of the character to be transmitted.

6.10.0.3 Receiver Holding Register

The Receiver Holding register buffers data received from the operator's console. A DR status condition is generated when the Receiver Holding register is full. Note that the data contained in the Receiver Holding register is the 1's complement of the data received.

6.10.1 Printer Multiplexing

The Printer Muliplexing feature permits a serial printer to share the USART with the operator's console. The printer is selected by the assertion of the PRNT bit of the System Status register (see section 6.7). When the printer is selected, character transmission proceeds over the Secondary Transmit line of the RS-232C connector. Handshaking between the processor and the printer is accomplished by connecting the printer Data Terminal Ready signal to the Carrier Detect line of the RS-232C connector. For cabling details, refer to Appendix D.

Note that the receiver lines of the USART are not connected to the printer. Therefore, no character transmission from the printer to the USART is possible. Note, also, that if the printer baud rate differs from the operator's console baud rate, the Baud Rate generator (see section 6.9) must be reprogrammed each time the USART is redirected. During this time, the USART receiver should be disabled since any data received from the operator's console is invalid. USART operation should not be switched between the console and the printer any sooner than one character time after the last character output. This allows time for the USART to finish transmitting that character.

6.10.2 USART Interrupts

Assuming interrupts are enabled (see section 6.3), the USART may generate processor interrupts under one of three conditions:

1) The Transmitter Holding register is empty. An interrupt is generated through location OE hex. Note that this interrupt is continuously generated until either the Transmitter Holding register is full, the transmitter is disabled (see the RTS bit of Control register #1), or interrupts are disabled.

2) The Receiver Holding register is full. An interrupt is generated through location 12 hex.

3) The Carrier Detect Signal (DTR from the printer) or the Data Set Ready signal has changed. An interrupt is generated through location 16 hex. This interrupt is continuously generated until either interrupts are disabled or the USART status register is read.

6.11 DMA Floppy Disk Controller

The DMA Floppy Disk Controller consists of the Western Digital WD1883 DMA controller, the WD1793-02 Floppy controller and their supporting logic. The DMA controller interfaces the floppy controller to the WD-bus for control/status operations, interrupt operations, and DMA data transfers.

6.11.0 Floppy Controller

The floppy controller provides all necessary floppy drive control functions including stepping pulse generation and timing, track 0 detection, CRC generation and checking, write precompensation, receive data recovery and diskette formatting. The floppy controller is capable of controlling up to four (4) single side or double side disk drives in either single density (IBM 1 and 1D FM) or double density (IBM 2 and 2D MFM) formats. Density selection is software controllable, enabling transfers between disks formatted in either single or double density format.

The floppy controller communicates with the DMA controller (see section 6.11.1) to perform floppy data transfers and status interrupts. The floppy controller signals the DMA controller to transfer a byte between memory and the floppy controller. It also signals the DMA controller upon completion of any floppy operation. The DMA controller processes the completion signal from then on.

The floppy controller provides five interface registers. There are two copies of each register in memory. One copy is a 16-bit register containing a copy of the Floppy Drive Select register (see section 6.11.0.0) in the most significant 8 bits, and a copy of the interface register in the least significant 8 bits. The second copy is an 8-bit register containing the interface register in the least significant 8 bits (the most significant 8 bits is undefined). Table 6.11.0 shows the device addresses of these registers.

REGISTER	WIDTH (bits)	ADDRESS (word)	WIDTH (bits)	ADDRESS (word)	ACCESS
	With Drive Select Register		Without Drive Select Register		
COMMAND	16	FC34	8	FC30	Write Only
STATUS	8	FC34	8	FC30	Read Only
TRACK	16	FC35	8	FC31	Read/Write
SECTOR	16	FC36	8	FC32	Read/Write
DATA	16	FC37	8	FC33	Read/Write

Table 6.11.0 Floppy Disk Interface Registers

6.11.0.0 Drive Select Register

The Drive Select register resides in the most siginificant byte of the 16-bit copies of the floppy interface registers. It is a write-only register, containing the floppy drive, side and recording density select bits.

BITS

15	14	13-12	11	10	9	8
SIDE SEL	SDEN	xxxxx	SEL-3	SEL-2	SEL-1	SEL-0

1) SIDE SEL:
This bit selects side 1 when set to 1, and side 0 of a double sided drive when set to 0. It should be set to 0 for single-sided drives.

2) SDEN:
This bit selects single density operation when set to 1, and selects double density when set to 0. Operations on Track 0 are in single density mode, regardless of the value of this bit.

3) SEL3:0:
These bits select floppy disk drives 3, 2, 1, and 0, respectively, when set to 1. Only one drive should be selected at any one time.

6.11.0.1 Command Register

The Command register is an 8-bit or 16-bit write-only register (depending on its address). The most significant byte of the 16-bit version is a copy of the drive select register. The most significant byte of the 8-bit version is undefined. The least significant byte of both versions contains the command issued to the floppy controller. The eleven commands are divided into four groups: read/write head move commands (Type 1), data read/write commands (Type 2), formatting commands (Type 3) and forced interrupt commands (Type 4).

Note that the floppy controller cannot execute more than one command at a time. Unpredictable results occur when the command register is loaded without either the Not-Ready bit of the Floppy Status register set, or the Busy bit reset (see section 6.11.0.2). The exception to this rule is the Type 4 interrupt command described in section 6.11.0.1.3.

Type	Command	Bit # 7 6 5 4 3 2 1 0
I	Restore	0 0 0 0 h V R r
I	Seek	0 0 0 1 h V R r
I	Step	0 0 1 u h V R r
I	Step In	0 1 0 u h V R r
I	Step Out	0 1 1 u h V R r
II	Read Sector	1 0 0 m S 0 C 0
II	Write Sector	1 0 1 m S 0 C a
II	Read Address	1 1 0 0 0 1 0 0
III	Read Track	1 1 1 0 0 1 0 0
III	Write Track	1 1 1 1 0 1 0 0
IV	Force Interrupt	1 1 0 1 p q s t

flags reviewed below

Table 6.11.1.A Command Summary

TYPE I

h = Head Load Flag (bit 3)
h = 1, Load head at beginning
h = 0, Unload head at beginning
V = Verify Flag (bit 2)
V = 1, Verify on last track
V = 0, No verify
R,r = Stepping Motor Rate (bits 1,0)
(see Table 6.11.1.E for rate summary)
u = Update Flag (bit 4)
u = 1, Update Track register
u = 0, No update

Table 6.11.1.D Flag Summary (Type I)

TYPE II

m = Multiple Record Flag (bit 4)
m = 0, Single Record
m = 1, Multiple Records
S = Side Select Flag (bit 3)
S = 0, Select Side 0
S = 1, Select Side 1
C = Side Compare Flag (bit 1)
C = 0, Disable Side Comparison
C = 1, Enable Side Comparison
a = Data Address Mark (bit 0)
a = 0, FB (Data Mark)
a = 1, F8 (Deleted Data Mark)

Table 6.11.1.D Flag Summary (Type II)

TYPE IV

p, q, s, t = Interrupt Condition Flags (bits 3-0)
all 0, Immediate Interrupt(1)
p = 1, Immediate Interrupt(2) (bit 3)
q = 1, Index Pulse (bit 2)
s = 1, Ready to Not-Ready Transition (bit 1)
t = 1, Not-Ready to Ready Transition (bit 0)

Table 6.11.1.D Flag Summary (Type IV)

R	r	Per Track
0	0	3 ms
0	1	6 ms
1	0	10 ms
1	1	15 ms

Table 6.11.1.E Stepping Rates

6.11.0.1.0 Type I Commands

Type I commands are used to control the positioning and loading of the read/write head of the drive selected in the Drive Select register. With the exception of the Seek command, the only action necessary to invoke a Type 1 command is the storage of the command in the Floppy Command register. Type 1 commands are executed regardless of the ready status of the floppy drive.

The Head Load bit of the Floppy Command register causes the floppy controller to load or unload the read/write head before the head is moved. The head is automatically unloaded either when the drive is re-selected or three seconds after the head is last used by the floppy controller.

After the Head Load command is complete, the head is stepped at a rate corresponding to the state of the R and r bits in the command register. If the Verify bit of the command register indicates that the head position is to be verified at the destination track, the head is loaded at the conclusion of the stepping operation (if it is not already loaded), and a 15 millisecond head settling delay commences. When the Head Load settling timer expires, the first encountered sector ID is read in the format specified in the Drive Select register. A verification is performed by comparing the track number in the sector ID with the contents of the Track Register. The verification can terminate in three ways:

1) The track numbers don't match and the CRC field of the sector ID is valid. The Seek-Error bit of the status register is set, and the command is terminated.

2) For four revolutions of the floppy, no sector ID can be found

with a valid CRC field. The CRC-Error bit of the status register is set, and the command is terminated.

3) The track numbers match and the CRC field of the sector ID is valid. The command is successful.

Type I commands terminate when either the status register Not Ready bit is set, or the Busy bit is reset. They may be prematurely terminated by a Force Interrupt command (Type IV).

6.11.0.1.0.0 Restore

This command steps the read/write head out (toward lower track numbers) until track 0 is encountered or until 255 steps have been performed. If track 0 is found, the Floppy Track register is set to zero. If track 0 has not been found after 255 steps, the command is terminated and the Seek-Error bit of the status register is set. This may be the result of a restore operation on a drive whose head is outside of track 0.

6.11.0.1.0.1 Seek

This command steps the read/write head to the track specified by the contents of Floppy Data register. The track register is updated on each step until it equals the data register. If no head movement is necessary, the floppy controller terminates the command within 200 microseconds.

6.11.0.1.0.2 Step

This command steps the read/write head one track in the direction the head was last moved. If the Update bit of the command register is set, the track register is updated.

6.11.0.1.0.3 Step In

This command steps the read/write head one track towards the center of the disk (higher track numbers). If the Update bit of the command register is set, the track register is incremented.

6.11.0.1.0.4 Step Out

This command steps the read/write head one track towards the edge of the disk (lower track numbers). If the Update bit of the command register is set, the track register is decremented.

6.11.0.1.1 Type II Commands

Type II commands are used to read or write sector data fields on the diskette. A Type II command requires that the DMA

controller be programmed to transfer the required number of bytes from/to the appropriate buffer address (see section 6.11.1). The floppy drive (selected in the Drive Select register) must be on-line and ready, and the floppy read/write head must be positioned over the desired track.

A Type II command is issued by loading the desired sector number into the Floppy Sector register and storing the command into the Floppy Command register.

Upon receipt of the Type II command, the floppy controller sets the Busy bit of the Floppy Status register, loads the read/write head, and waits 15 milliseconds for the head to settle. After expiration of the head load timer, the floppy controller searches the track for a sector ID whose CRC field is valid, and whose track and sector fields match the contents of the Track and Sector registers. In addition, if the command's Side Compare bit is set to 1, the floppy-side bit of the sector ID must match the Side Sel bit of the Drive Select register. The command can proceed in three ways:

1) For four revolutions of the floppy, no match is found. The Record-Not-Found bit of the status register is set, and the command is terminated.

2) A match is found, but a CRC error is detected in the sector ID. The CRC-Error bit and the Record-Not-Found bits of the status register are set, and the command is terminated.

3) A match is found, and the CRC field of the sector ID is valid. The data field of the sector is located and data transfer is initiated.

Each of the Type II commands contains a Multiple Sector bit which specifies multiple sector operations. If this bit is 0, a single sector is transferred. If this bit is 1, the requested sector is transferred, the Sector register is incremented, and another transfer is attempted. This sequence continues until a floppy error occurs. Since there are 26 sectors on a track, when a transfer is attempted on sector 27, a Record-Not-Found error will occur, and the command will terminate. Thus, the Multiple Sector bit is a directive to transfer until the end of the track is reached.

Type II commands terminate when either the status register Not-Ready bit is set, or the Busy bit is reset. They may be prematurely terminated by a Force Interrupt command (Type IV).

6.11.0.1.1.0 Read Sector Command

The Read Sector command causes the floppy controller to read the data field of the sector named in the Floppy Sector register. The floppy controller must find the Data Address Mark of the Data Field within 30 bytes of the last byte of a single density sector ID CRC field (within 43 bytes for double density); otherwise the

Record-Not-Found bit of the Status register is set, and the command is terminated.

Upon receipt of a data byte from the floppy drive, the floppy controller signals the DMA controller to transfer the byte from the Floppy Data register into memory. If the DMA controller has not read the Data register by the time a new byte is ready, an overrun condition occurs. The Lost-Data bit of the Status register is set, and the command is terminated.

At completion of the data transfer, the Record-Type bit of the status register is set according to the type of Data Address Mark found at the beginning of the sector. If the CRC field computed from the sector data does not match the data CRC field on the floppy, the CRC Error bit of the status register is set.

6.11.0.1.1.1 Write Sector Command

The Write Sector command causes the floppy controller to write to the data field of the sector named in the Floppy Sector register. The floppy controller signals the DMA controller to load the Floppy Data register with a data byte from memory. The floppy controller activates the floppy drive write logic 11 bytes (22 bytes in double density) after the last byte of the sector ID CRC field.

If the DMA controller has not loaded a data byte into the Data register by this time, the Lost-Data bit in the Floppy Status register is set, and the command is terminated. If the Data register has been loaded, six bytes of zeros (12 bytes in double density) are written onto the disk. The Data Address Mark is then written according to the Address Mark field of the write sector command. If this bit is 0, a Data Mark is written. If this bit is 1, a Deleted Data Mark is written.

A data request is made to the DMA controller for each byte written to the floppy. If the Data register has not been loaded by the appropriate time, the Lost-Data bit in the Status register is set, and a zero byte is written to the floppy. Transfer continues until the last data byte is written. The two-byte CRC field is computed and written, followed by a byte containing FF hex (4F hex in double density). The Write Gate is then deactivated.

6.11.0.1.2 Type III Commands

Type III commands are used to read or write track diskette formatting information. A Type III command requires that the DMA controller be programmed to transfer the required number of bytes from/to the appropriate buffer address (see dection 6.11.2), and that the floppy read/write head be positioned over the desired track. The floppy drive (selected in the Drive Select register) must be on-line and ready, and the floppy read/write head must be positioned over the desired track.

A Type III command is issued by storing the command into the Floppy Command register.

Upon receipt of the Type III command, the floppy controller sets the Busy bit of the Floppy Status register, loads the read/write head, and waits 15 milliseconds for the head to settle.

Type III commands terminate when either the Status register Not-Ready bit is set, or the Busy bit is reset. They may be prematurely terminated by a Force Interrupt command (Type IV).

6.11.0.1.2.0 Read Address

The Read Address command causes the floppy controller to transfer the sector ID field of the next sector to arrive under the floppy read/write head. The sector ID field contains six bytes and appears in memory as follows:

Byte	Contents
0	Track Number
1	Side Number
2	Sector Number
3	Sector Length
4	CRC1
5	CRC2

If the CRC field of the sector ID is not valid (CRC1 and CRC2) the CRC-Error bit of the Floppy Status register is set. In any case, the floppy controller stores the track number found in the sector ID into the Floppy Sector register.

6.11.0.1.2.1 Read Track

The Read Track command causes the floppy controller to wait for the floppy Index Mark. It then transfers all bytes on the floppy until the next Index mark is encountered. This includes sector ID's, sector data fields, and track formatting information. No CRC checking is performed.

Note that there is an in-determinable number of bytes of formatting information on each track. Thus, either a transfer byte count under-run should be expected from the DMA controller, or a Lost-Data status should be expected from the floppy controller.

6.11.0.1.2.2 Write Track

The Write Track command causes the the floppy controller to write one full track of formatting information to the disk. The information contains sector IDs, CRC fields, reserved clocking patterns, and other information as described in Table 6.11.2.

The floppy controller starts writing at the leading edge of the Index Pulse and continues until the next Index Pulse. Prior to the first write operation, the floppy controller requests one byte from the DMA controller. If the DMA controller has not loaded the Floppy Data register within 96 microseconds (48 microseconds for double density), the Lost-Data bit of the Floppy Status register is set, and the command is terminated. The DMA controller is signalled each time another byte is required. If an under-run occurs, a zero byte is transferred and the Lost-Data bit of the Status register is set.

Data Pattern (Hex)	Single Density Function	Double Density Function
00 thru F4	Write 00 thru F4 with Clk = FF	Write 00 thru F4 in MFM
F5	Not Allowed	Write 0A * in MFM, preset CRC
F6	Not Allowed	Write C2 ** in MFM
F7	Generate 2 CRC bytes	Generate 2 CRC bytes
F8 thru FB	Write F8 thru FB, Clk=C7, Preset CRC	Write F8 thru FB in MFM
FC	Write FC with Clk=D7	Write FC in MFM
FD	Write FD with Clk=FF	Write FD in MFM
FE	Write FF with Clk=FF	Write FE in MFM
FF	Write FF with Clk=FF	Write FF in MFM

* Missing clock transition between bits 4 and 5
** Missing clock transition between bits 3 and 4

Table 6.11.2 Formatting Control Byte Functions

6.11.0.1.3 Type IV Commands

Type IV commands are Force Interrupt commands, and are the only commands which may be issued to the floppy controller when the Busy bit of the Floppy Status register is set. A Type IV command is issued by loading it into the Floppy Command register. This command terminates upon the satisfaction of the condition specified by the Interrupt Condition bits (bits 0 - 3). Upon termination, the Busy bit of the status register is reset. If there was a floppy command in progress when the Type IV command was initiated, the command is terminated, and the Status register is updated according to the type of the interrupted command. If no floppy command was in progress, the Status register is set as if a Type I

command was executed.

The termination conditions for the Type IV commands are described in Table 6.11.3.

BITS p	q	s	t	TERMINATION CONDITIONS
0	0	0	0	Immediate Termination: The Busy bit of the status register is reset. Any command terminates, but no interrupt is generated.
0	0	0	1	Termination occurs when the selected unit's status changes from Not-Ready to Ready. The busy bit is immediately reset and an interrupt is generated.
0	0	1	0	Termination occurs when the selected unit's status changes from Ready to Not-Ready. The busy bit is immediately reset and an interrupt is generated.
0	1	0	0	Termination occurs when the floppy controller encounters the next Index Pulse. The busy bit is immediately reset and an interrupt is generated.
1	0	0	0	Immediate Interrupt: An interrupt is generated, but the Busy bit of the status register is not reset.

Table 6.11.3 Type IV Termination Conditions

6.11.0.2 Status Register

The Floppy Status Register is either an 8-bit or a 16-bit read-only register (depending on its address). It resides in the least significant byte of both versions. Since the Floppy Select register occupies the most significant byte of the 16-bit version, but is a write-only register, the most significant byte of both versions of the Status register is undefined.

The Status register reflects the status of the last command executed on the floppy drive that was last selected in the Drive Select register. Upon receipt of any command except a Type IV command (see section 6.11.0.1.3), the Busy status bit is set.

The Status register is interpreted according to the type of command last executed by the floppy controller.

6.11.0.2.0 Type I Command Status

The bits of the Status register are interpreted after the termination of a Type I command as follows:

BITS							
7	6	5	4	3	2	1	0
NOT READY	WRITE PROT	HEAD LOAD	SEEK ERROR	CRC ERROR	TRACK 00	INDEX PULSE	BUSY

1) NOT READY:
This bit is set to 1 when the selected drive is not ready. It is set to 0 if the drive is ready.

2) WRITE PROT:
This bit is set to 1 if the diskette installed in the selected drive is write protected. It is set to 0 if a write operation is possible.

3) HEAD LOAD:
This bit is set to 1 if the read/write head on the selected drive is loaded and engaged. This occurs about 35ms after a head load command is issued. The bit is set to 0 when the head is unloaded.

4) SEEK ERROR:
This bit is set to 1 following a Verify operation where no sector ID is found to have both a valid CRC field, and a track number matching the contents of the Track register within 4 revolutions of the disk.

5) CRC ERROR:
This bit is set to 1 if a CRC Error is detected during a Verify operation and a sector ID is encountered with an invalid CRC field.

6) TRACK 00:
This bit is set to 1 when the read/write head of the selected drive is positioned over track 00.

7) INDEX:
This bit is set to 1 when the floppy index mark is detected by the selected drive.

8) BUSY:
This bit is set to 1 for the duration of the execution of a command. It is set to 0 upon the termination of the command.

6.11.0.2.1 Type II and Type III Command Status

The bits of the Status register are interpreted after the termination of a Type II or a Type III command as follows:

BITS

7	6	5	4	3	2	1	0
NOT READY	WRITE PROT	RECORD TYPE / WRITE FAULT	RECORD NOT FOUND	CRC ERROR	LOST DATA	DATA REQUEST	BUSY

1) NOT READY:
This bit is set to 1 if the selected drive is not ready. It is set to 0 if the drive is ready.

2) WRITE PROT:
This bit is set to 1 if the diskette in the selected drive is write-protected. It is set to 0 if a write operation is possible.

3) RECORD TYPE/WRITE FAULT:
This bit is set to 1 following a Read Sector if the selected sector contains a Deleted Data Mark. It is set to 0 if the mark is not present. This bit is not used on a Read Track command. Following either a Write Sector or a Write Track command, this bit is set to 1 if the selected floppy drive signals a Write Fault. It is set to 0 if the write operation is successful.

4) RECORD NOT FOUND:
This bit is set to 1 if no sector ID can be found that both has a valid CRC field, and matches the sector contained in the sector register. It is also set to 1 if no Data Mark can be found within 30 bytes of the preamble CRC (43 bytes for double density). This bit is set to 0 if the command is successful.

5) CRC ERROR:
This bit is set to 1 if a CRC Error has been detected. If the error is found in a sector ID field, the Record-Not-Found bit is also set to 1. This bit is set to 0 if the command is successful.

6) LOST DATA:
This bit is set to 1 if either a read data over-run or a write data under-run is detected. If the error is detected during a read operation, the over-run byte is lost. If the error is detected during a write operation, a zero byte is written to the floppy. This bit is set to 0 if the command is successful.

7) DATA REQUEST:
This bit is set to 1 when the floppy controller signals the DMA controller to service the Floppy Data register. It is set to 0 when the DMA controller satisfies the request.

8) BUSY:
This bit is set to 1 to indicate that a command is in progress.

6.11.0.2.2 Type IV Command Status

If a Force Interrupt command is executed when there is a current command under execution, and the 'p' bit of the Command register is set to 0, the Busy status bit is set to 0, and the rest of the status bits are unchanged. If a Force Interrupt command is issued and the controller is not executing a command, the Busy status bit is set to 0, and the status for a Type 1 command is loaded into the Status register (see section 6.11.0.2.0).

6.11.0.3 Data Register

The Floppy Data register is either an 8-bit or a 16-bit read-write register (depending on the address) that buffers data for the DMA controller during data Type II operations (see section 6.11.0.1.1). It also contains the destination track number during a Seek operation (see section 6.11.0.1.0.1).

6.11.0.4 Track Register

The Floppy Track register is either an 8-bit or a 16-bit read-write register (depending on the address) that contains the track number under the read/write head of the most recently accessed floppy drive. This register is updated by the Type I commands, and used in verifying the head position during Type I and Type II commands.

When it is possible that the floppy controller may be used with more than one floppy drive, the current track for any unselected drives must be maintained by the software floppy driver. When the previously unselected drive is selected, the Track register must be loaded with the appropriate track number.

Note: This register should not be loaded when the floppy controller is busy.

6.11.0.5 Sector Register

The Floppy Sector register is either an 8-bit or a 16-bit read-write register (depending on the address) that contains the sector number to be accessed by a Type II command (see section 6.11.0.1.1). It also contains the current track number after the execution of a Read Address command (see section 6.11.0.1.2.0).

Note: This register should not be loaded when the floppy controller is busy.

6.11.1 DMA Controller

The DMA Controller interfaces the Floppy Disk Controller and the memory. It generates all bus request signals, all bus protocol signals, and status interrupts necessary to effect DMA transfers between the floppy controller and memory without processor intervention. Moreover, all floppy controller data transfers and interrrupt processing is performed by the DMA controller. Floppy controller register addresses select the DMA controller, which in turn selects the appropriate register of the floppy controller. Floppy controller interrupts are communicated to the DMA controller, which may be programmed to allow, or disallow the interrupt.

The DMA controller provides 4 groups of interface registers: the Control register, Status register, Byte Count register, and the Memory Address register. They are listed in Table 6.11.4 with their corresponding device address locations.

REGISTER	WIDTH (bits)	ADDRESS (word)	ACCESS
CONTROL	8	FC38	Write Only
STATUS	8	FC39	Read/Write
BYTE COUNT (low)	8	FC3A	Read/Write
BYTE COUNT (high)	8	FC3B	Read/Write
ADDRESS (low)	8	FC3C	Read/Write
ADDRESS (high)	8	FC3D	Read/Write
ADDRESS (extension)	2	FC3E	Read/Write

Table 6.11.4 DMA Interface Registers

Each DMA interface register is contained in the least significant byte of a 16-bit word. The most significant byte is undefined. The high Byte Count and low Byte Count registers combine to form the most and least significant bytes, respectively, of a 16-bit two's complemented byte count register. The extension Address, high Address, and low Address registers combine to form an 18-bit memory buffer address register. This register is the address of a memory byte. Since addresses on the PDQ-3 are word addresses, a byte address is obtained from a word address by adding the word address to itself.

The DMA Controller may be programmed to transfer information between the floppy and memory in four steps:

1) Store the byte address of the memory buffer into the Address register group.

2) Load the Byte Count registers with the two's complement of the buffer size.

3) Program the Control register for the direction, the interrupt characteristics, and the bus handling characteristics of the transfer.

4) Program the floppy controller to start the data transfer.

The transfer starts when the floppy controller signals the DMA controller that DMA service is necessary. The DMA controller issues a DMA bus request then waits until it is granted the bus mastership. As the bus master, the DMA controller controls the bus handshaking protocol necessary to transfer a byte of data between the memory and the floppy controller. After the byte is transferred, the memory buffer address is incremented to point at the next byte for transfer.

6.11.1.0 DMA Control Register

The DMA Control register is a write-only register used to initiate DMA operations. The DMA controller may be programmed to interrupt on a number of different conditions including floppy controller completion, bus timeout, and DMA termination.

BITS

7	6	5	4	3	2	1	0
X	AECE	HBUS	IOM	TCIE	TOIE	DIE	RUN

1) AECE:

When the Address Extension Carry Enable is set to 1, carry operations out of the high Address register are propagated into the extension address register. This bit should be set to 1 when accessing more than 64K bytes of memory.

2) HBUS:

When the Hold Bus bit is set to 1, the DMA controller acts as bus master for the entire duration of the DMA operation. If this bit is set to 0, the DMA controller relinquishes the bus mastership after each byte transfer. This bit should be set to 0.

3) IOM:

The I/O Mode bit is set to 1 in order to perform DMA transfers from the floppy controller to memory. This bit is set to 0 in order to perform DMA transfers from memory to the floppy controller.

4) TCIE:

The Transfer Count Interrupt Enable bit is set to 1 in order to allow the DMA controller to interrupt the processor when both the low and high Byte Count registers are zero. This bit is set to 0 in order to disallow the interrupt.

5) TOIE:

The Time Out Interrupt Enable bit is set to 1 in order to allow the DMA controller to interrupt the processor if the memory does not respond within 5 microseconds of a DMA Sync signal. This bit is set to 0 in order to disallow the interrupt.

6) DIE:
The Device Interrupt Enable bit is set to 1 in order to allow a Floppy Controller task completion interrupt to interrupt the processor. This bit is set to 0 in order to disallow the interrupt.

7) RUN:
The Run bit is set to 1 in order to start a DMA operation. Thereby causing the Busy bit in the Status register to be set. This bit is set to 0 to cancel any DMA operations.

6.11.1.1 DMA Status Register

The DMA Status register contains the status information for the DMA controller. It may be read at any time, but may be written only when the Busy status bit is set to 0.

BITS

7	6	5	4	3	2	1	0
BUSY	AECE	HBUS	IOM	TCZI	TOI	DINT	BOW

1) BUSY:
The Busy bit is set to 1 when a DMA operation is in progress.

2) AECE:
The Address Extension Carry Enable bit is a copy of the AECE bit of the command register.

3) HBUS:
The Hold Bus bit is a copy of the HBUS bit of the command register.

4) IOM:
The I/O Mode bit is a copy of the IOM bit of the command register.

5) TCZI:
The Transfer Count Zero Interrupt bit is set to 1 to indicate that both the high and the low Byte Count registers are zero. If the TCZI bit of the Command register is set to 1, an interrupt is generated. The interrupt is cleared by making either the high or the low Byte Count register non-zero, then by setting the TCZI bit to 0.

6) TOI:
The Time Out Interrupt bit is set to 1 to indicate that the memory did not respond with a Reply signal within 5 microseconds of the DMA Sync signal. If the TOIE bit of the command register is set to 1, an interrupt is generated. The interrupt is cleared by setting the TOI bit to 0.

7) DINT:

The Device Interrupt bit is set to 1 to indicate that the Floppy Controller has completed an operation. If the DIE bit of the command register is set to 1, a processor interrupt is generated. The interrupt is cleared by reading the Floppy Controller Status register, then by setting the DINT bit to 0.

8) BOW:

The Byte Or Word bit is set to 1 if the DMA controller transfers a byte in a DMA cycle. It is set to 0 if a word is transferred. The DMA controller on the PDQ-3 always transfers a byte.

6.11.1.2 Byte Count Registers

The high Byte Count and low Byte Count registers combine to form the most and least significant bytes, respectively, of a 16-bit byte count register. The 16-bit register is loaded with the two's complement of the number of bytes in the DMA transfer, and is incremented each time the DMA controller transfers a byte. When the 16-bit register reaches 0, the DMA operation terminates, and the TCZI bit of the Status register is set. If the TCIE bit of the Command register is set to 1, a processor interrupt will also be generated.

Each register is loaded independently, and can be loaded only when the Busy bit of the Status register is set to 0. Attempts to load these registers while this bit is set to 1 are ignored by the DMA controller.

6.11.1.3 Memory Address Registers

The extension Address, high Address, and low Address registers combine to form an 18-bit memory buffer address register. This register is the address of a memory byte. Since addresses on the PDQ-3 are word addresses, a byte address is obtained from a word address by adding the word address to itself. Note that the PDQ-3 uses only the low order 17 bits of the 18-bit address.

Each register is loaded independently, and can be loaded only when the Busy bit of the status register is set to 0. Attempts to load these registers while this bit is set to 1 are ignored by the DMA controller.

6.11.2 Initialized State

The DMA Floppy Disk Conroller is initialized by powering on, or by pressing the Reset button on the front console, or when I/O Reset bit of the System Status register is set to 1. In the initialized state, all drive select bits in the Drive Select register are set to 0, and the Floppy Status register Not-Ready bit is set to 1. The Floppy Track, Sector, and Data registers are undefined.

The DMA controller Address registers are set to 0, and the Byte Count registers are programmed for 65535 bytes. The DMA controller status is inactive, with all interrupts disabled and the Hold Bus and Write options enabled.

6.11.3 DMA/Floppy Controller Interrupts

Assuming the interrupt system is enabled, the DMA controller may be programmed to generate processor interrupts under any of three conditions:

1) Termination of a floppy controller command. This interrupt is enabled when the DIE bit of the DMA Command register is set to 1. Note that this bit must be set in order to generate floppy interrupts whether or not a DMA transfer is involved.

2) Termination of a DMA transfer command. This interrupt is enabled when the TCIE bit of the DMA Command register is set to 1. A processor interrupt occurs whenever both the high Byte Count and the low Byte Count registers are 0.

3) Time-out during a DMA transfer. This interrupt is enabled when the TOIE bit of the DMA Command register is set to 1. A processor interrupt occurs whenever the memory does not respond to the DMA controller within 5 microseconds.

The DMA Floppy Controller interrupts through the interrupt vector at location 0E hex. When an interrupt occurs, the PDQ-3 interrupt system is disabled, and the software interrupt handler is invoked. All DMA interrupts must be specificly disabled by the software interrupt handler before the PDQ-3 interrupt system is re-enabled. A DMA interrupt is disabled when a 0 is stored into the DMA status register bit corresponding to the active interrupt. Moreover, if the interrupt is caused because the Byte Count registers are 0, a non-zero quantity must be loaded into one or both registers in order to preclude the interrupt's re-occurance. Note that if the DMA interrupt is not disabled in this manner, a DMA interrupt will occur immediately upon re-enabling the interrupt system.

6.12 CPU Module Serial Number

Each CPU Module has been assigned a unique serial number which can be accessed via the HDT PROM. This serial number is located at word address F5FF and may be read and acted upon by applications software.

A. HEXADECIMAL DEBUGGING TOOL (HDT)

The Hexadecimal Debugging Tool (HDT) is a powerful, low level debugger capable of examining memory, examining I/O device registers, bootstrapping the UCSD Pascal system, and recovering from power failures. It is implemented as a UCSD Pascal program resident in PROMS located on the PDQ-3 CPU Module. The PROMS occupy memory locations F400 hex through F7FF hex. HDT uses memory between 100 hex and 200 hex for temporaries.

A.1 Invoking HDT

HDT is activated under one of four conditions:

1) Invokation of the RESET button. HDT is automatically executed when the RESET button is pushed. If the E14 jumper is installed on the PDQ-3 CPU Module (see section 3.2.1), HDT attempts to bootstrap the UCSD Pascal system from the bootstrap device. If the E12 jumper is installed, HDT prints a '#' on the console and waits for an HDT command. The 'R' command causes HDT to boot the UCSD Pascal system from the bootstrap device.

2) Initial power up. HDT checks for a power fail restart in progress. If a restart is in progress, HDT restarts the UCSD Pascal system at the point where a power failure interrupted it. If a restart is not in progress, HDT behaves as if the RESET button was invoked.

3) Invokation of the control-P key. HDT is invoked as a high priority process (priority 255) and the UCSD Pascal system is suspended. It prints a '#' on the console and waits for an HDT command. During the execution of HDT, all interrupts are latched and any outstanding DMA operations continue. Resumption of the UCSD Pascal system occurs on receipt of the 'P' command from the console.

4) Invokation of the HALT procedure from a Pascal program. This invokes HDT in the same manner as the console BREAK key.

Note that HDT is NOT invoked by depressing the HALT button on the front panel of the PDQ-3 System.

A.2 HDT Commands

HDT can be commanded to examine and modify a 'current location' in memory, boot the UCSD Pascal system from the bootstrap device, or proceed with a UCSD Pascal program currently executing. All numbers are input and output by HDT in hexadecimal format (eg. 1 hex = 1 decimal, A hex = 10 decimal, and 10 hex = 16 decimal). All addresses point to 16-bit word quantities. The commands are as follows:

'R' HDT reboots the UCSD Pascal system from the bootstrap device.

'P' The currently executing UCSD Pascal program is resumed.

'/' If a number has been entered, that number becomes the new current location. HDT then displays the contents of the new current location.

<cr> If a number has been entered, that number is stored into the current location. HDT then displays the HDT prompt '#'.

<lf> If a number has been entered, that number is stored into the current location. HDT then increments the current location, and displays the contents of the new current location.

'^' If a number has been entered, that number is stored into the current location. HDT then decrements the current location, and displays the contents of the new current location.

'@' If a number has been entered, that number is stored into the current location. The contents of the current location then becomes the new current location, and HDT displays the contents of the new current location.

B. RESERVED MEMORY LOCATIONS

B.0 Bus Address Assignments

Since I/O device registers are mapped into the memory space, locations F000 through FFFF are reserved for these registers. The PDQ-3 CPU Module onboard 'devices' are assigned addresses F400 through F7FF and FC00 through FC7F.

B.0.1 PDQ-3 Onboard Device Addresses

The following word addresses and interrupt vectors are assigned to devices located on the PDQ-3 CPU Module:

DEVICE	ADDRESS	INTERRUPT VECTOR
HDT ROM	F400 (lowest)	
	F5FF (CPU Module Serial #)	
	F7FF (highest)	
Console terminal control register 1	FC10	
Console terminal control register 2	FC11	
Console terminal status register	FC12	
Console terminal input register	FC13	0012
Console terminal output register	FC14	000E (data)
		0016 (protocol)
System environment switch	FC18	0002 (bus error)
		0006 (pwr fail)
Console baud rate generator	FC20	
System clock counter	FC21	001A
Interval timer	FC22	001E
Timer mode control byte	FC23	
System status register	FC24	
Floppy disk status/command register	FC34	000A
Floppy disk track register	FC35	
Floppy disk sector register	FC36	
Floppy disk data register	FC37	
DMA controller command register	FC38	000A
DMA controller status register	FC39	
DMA controller byte transfer count	FC3A (low)	
	FC3B (high)	
DMA controller memory start address	FC3C (low)	
	FC3D (high)	
DMA controller memory extension	FC3E	
Reserved ROM HDT	FC4x	
Reserved ROM HDT	FC5x	
Pointer to HDT ROM	FC68	
Reserved	FC6x	
Reserved	FC7x	

NOTE: x = don't care

B.0.2 Q-Bus Device Addresses

Addresses are reserved for certain devices on the Q-Bus. Their word addresses and interrupt vectors are as follows:

DEVICE		FIRST	LAST	VECTOR
Reserved		F000	F003	
IEEE std. 488 bus interface	IBV11-A	F033	F036	008A
Parallel line unit	DRV11 #3	F7F4	F7F7	0000-007F
Parallel line unit	DRV11 #2	F7F8	F7FB	0000-007F
Parallel line unit	DRV11 #1	F7FC	F7FF	0000-007F
Analog-to-digital converter	ADV11-A	F880	F882	0084
Programmable RTC	KWV11-A	F889	F897	0090
Digital-to Analog converter	AAV11-A	F890	F893	
Parallel line unit	DRV11-B #1	FA84	FA87	002A
Parallel line unit	DRV11-B #2	FA88	FA8B	0000-00FF
Parallel line unit	DRV11-B #3	FA8C	FA8F	0000-00FF
Magnetic Tape	TM-11	FAA8	FAAE	004A
256 word ROM	BDV11	FB00	FB5F	
RX01 Floppy disk	RXV11	FE3C	FE7E	005A
Hard Disk	RP-02	FEE0	FEEE	0056
RK05 Mass storage	RKV11	FF80	FF87	0048
Printer	LAV11, LPV11	FFA6	FFA7	0040
Terminals:				
partial modem control	DLV-11	FEB8	FFBB	0030
full modem control	DLV-11 E	FFB8	FFBB	0030
no modem control	DLV-11 F	FFB8	FFBB	0030
4 channel with partial modem control	DLV-11 J	FFB8	FFBB	0030
		FFA0	FFAE	006x

C. RECOMMENDED CRTs

MODEL	COMPANY
Elite 1521A *Elite 3052A DT80-1	DataMedia (manufacturer) 7300 North Crescent Blvd. Pennsauden, NJ 08110 (609) 665-2382
*Zephyr	Zentec Corporation (manufacturer) 2400 Walsh Ave. Santa Clara, CA 95050 (408) 246-7662
IQ120 *IQ140	Soroc Corporation (manufacturer) 165 Freedom Ave. Anaheim, CA 92801 (714) 992-2860
*Z-19	Advanced Digital Products (distributor) 7584 Trade St. San Diego, CA 92121 (714) 578-9595

* Highly recommended

D. CABLING RECOMMENDATIONS

D.0 Cable Length vs Baud Rate

The recommended maximum cable lengths for the baud rates supported by the PDQ-3 CPU Module are:

Baud Rate	Cable Length (ft)	(m)
110	400	32
300	400	32
600	400	32
1200	400	32
2400	400	32
4800	200	16
9600	100	8
19200	50	4

Belden 2464 cable or the equivalent is recommended.

D.1 PDQ-3 Cable Pin-out Requirements

The use of the RS-232C console connector on the PDQ-3 CPU module is multiplexed between terminal data and printer data. All terminal data is transmitted on the primary transmission lines, and all printer data is transmitted on the secondary lines. Thus, an RS-232C cable that services both a terminal and a printer must start with a common connector to the PDQ-3 CPU Module console connector, then split into a terminal cable and a printer cable. Such a cable is available with the PDQ-3 System and is wired as follows:

PDQ-3 CPU Module	CONNECTED PINS Terminal Connector	Printer Connector
1 (Frame Ground)	1 (Frame Ground)	1 (Frame Ground)
2 (Recv Data)	2 (Xmit Data)	
3 (Xmit Data)	3 (Recv Data)	3 (Recv Data)
6 (Data Term Rdy)	6 (Data Set Rdy)	
7 (Signal Ground)	7 (Signal Ground)	7 (Signal Ground)
14 (Sec Xmit)		
16 (Car Det)		20 (DTR)

Note: On the PDQ-3 CPU Module cable end, pins 4 (CTS) and 5 (RTS) must be shorted. On the Terminal Connector, pins 4 (RTS), 5 (CTS), and 8 (CARD) must be shorted. On the Printer Connector, pins 4 (RTS), 5 (CTS), 6 (DSR), and 8 (CARD) must be shorted.

Using this cable it is possible to communicate with any RS-232C terminal in full duplex. If handshaking is necessary, it must be carried out using a data sequence such as X-ON, X-OFF. Printer communication is possible in the output mode only. If handshaking is necessary, it must be carried out using the Data

Terminal Ready pin out of the printer and will appear as a Carrier Detect on the PDQ-3 console controller.

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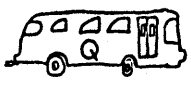

I. Errata

The following corrections should be made to the PDQ-3 Hardware User's Manual, Version 1.0 :

1) section 2.1.1, page 7 :

The power required for the Primary Backplane is used by the power up/down sequencing logic, 250 Ohm Bus termination resistors, and the front console.

should be :

The power required for the Primary Backplane is used by the power up/down sequencing logic, 250 Ohm Bus termination resistors, the front console, and the PDQ-3 CPU Module.

2) section 2.1.3, page 7 :

(d) Seek Times		
Track/Track	6 ms	3 ms

should be :

(d) Seek Times		
Track/Track	10 ms	6 ms

3) section 3.0.3.0.1, table 3.2, page 20 :

Row 4	Priority O	Priority P

should be :

Row 4	Priority P	Priority O

4) section 5.0, table 5.0, page 39 :

AA1	BSPARE1	
AB1	BSPARE2	Unassigned bus spares.

should be :

AA1	BIRQ5L	
AB1	BIRQ6L	Interrupt Request Priority 5 and 6. Not used by the PDQ-3.

AC1	BAD16	
AD1	BAD17	Extended address bits.

should be :

AC1	BDAL16L	
AD1	BDAL17L	Extended address bits.

AS1	PSPARE3	Unassigned spare. Usage not recommended.

should be :

AS1	+5B or +12B	Battery Backup Power.

5) section 5.0, table 5.0, page 40 :

BP1	BSPARE6	Unassigned bus spare.

should be :

BP1	BIRQ7L	Bus interrupt request, priority 7. Not used by the PDQ-3.

6) section 6.7, page 57 :

The PRNT bit is always read as a 0.

should be :

The PRNT bit is always read as a 1.

7) section 6.3, table 6.3, page 53 :

Console Transmitter Ready	000E	3
Console Receive Data	0012	4

should be :

Console Receive Data	0012	3
Console Transmitter Ready	000E	4

8) section 6.10.0.0.1, page 64 :

4) RX CLK:
The alternate RX clock bit determines the separate receive data clock rate. This feature is not used on the PDQ-3 and this bit must always be set to 0.

should be :

4) RX CLK:
The alternate RX clock bit determines the separate receive data clock rate. This feature is not used on the PDQ-3 and this bit must always be set to 1.

9) appendix B, section B.0.1, page 87 :

Console terminal input register	FC13	0012
Console terminal output register	FC14	000E

should be :

Console terminal input register	FC13	000E
Console terminal output register	FC14	0012

10) appendix D, section D.1, page 90 :

	CONNECTED PINS	
PDQ-3 CPU Module	Terminal Connector	Printer Connector
1 (Frame Ground)	1 (Frame Ground)	1 (Frame Ground)
2 (Recv Data)	2 (Xmit Data)	
3 (Xmit Data)	3 (Recv Data)	3 (Recv Data)
6 (Data Term Rdy)	6 (Data Set Rdy)	
7 (Signal Ground)	7 (Signal Ground)	7 (Signal Ground)
14 (Sec Xmit)		
16 (Car Det)		20 (DTR)

should be :

	CONNECTED PINS	
PDQ-3 CPU Module	Terminal Connector	Printer Connector
1 (Frame Ground)	1 (Frame Ground)	1 (Frame Ground)
2 (Recv Data)	2 (Xmit Data)	
3 (Xmit Data)	3 (Recv Data)	
7 (Signal Ground)	7 (Signal Ground)	7 (Signal Ground)
14 (Sec Xmit)		3 (Recv Data)
16 (Car Det)		
20 (Data Set Rdy)	20 (Data Term Rdy)	20 (DTR)

II. Addenda

The following additions should be made to the PDQ-3 Hardware User's Manual, Version 1.0 :

1) WARNING : This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart J of Part 15 of the FCC rules which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

2) Several additions and changes should be made for systems with Shuggart single-sided disk drives :

a) section 2.1.3, page 7 :

(C) Performance

	Single Density	Double Density
(a) Formatted Capacity		
Single Side	0.5 Megabyte	1.0 Megabyte
Double Side	1.0 Megabyte	2.0 Megabyte
(b) Transfer Rate	250,000 bits/sec	500,000 bits/sec
	Single Sided	**Double Sided**
(c) Latency		
Average	83.3 ms	83.3 ms
Maximum	166.7 ms	166.7 ms
(d) Seek Times		
Track/Track	6 ms	3 ms
Average	275 ms	96 ms
Head Settling	15 ms	20 ms
(e) Head Load	60 ms	40 ms

(D) Power Requirements (per drive)

	110V @ 60Hz	220V @ 50Hz
(a) AC		
Voltage Range		
single-sided	100V to 130V	200V to 240V
double-sided	90V to 132V	196V to 264V
Frequency	+/- 2%	+/- 2%
Current (typ)		
single-sided	0.85A	0.53A
double-sided	0.4A	0.25A

(b) DC (+/- 5%)	Selected	Unselected
+5V	1.1A max.	1.1A max.
+24V	1.4A max.	0.3A max.

should be changed to :

(C) Performance

	Single Density	Double Density
(a) Formatted Capacity		
Single Side	0.5 Megabyte	1.0 Megabyte
Double Side	1.0 Megabyte	2.0 Megabyte
(b) Transfer Rate	250,000 bits/sec	500,000 bits/sec

	Single Sided
(c) Latency	
Average	83 ms
(d) Seek Times	
Track/Track	8 ms
Average	260 ms
Head Settling	8 ms
(e) Head Load	35 ms

(D) Power Requirements (per drive)

(a) AC	110V @ 60Hz	220V @ 50Hz
Voltage Range single-sided	85V to 127V	170V to 253V
Frequency	+/- .5Hz	+/- .5Hz
Current (typ) single-sided	0.3A	0.18A
(b) DC (+/- 5%)	Selected	Unselected
+5V	.8A typ.	.8A typ.
+24V	1.3A typ.	1.3A typ.

b) section 3.2.1, page 26 :

a) For single-sided drives, press down on the lever below the left floppy disk drive. For double-sided drives, push in the bar below the door. The door of the drive will pop open.

should be changed to :

a) Push in the bar below the door. The door of the drive will pop open.

c) section 3.2.1, page 28 :

a) Press down on the lever below the drive. The door will pop open, and the edge of the diskette will be visible.

should be changed to :

a) Push in the bar below the drive. The door will pop open, and the edge of the diskette will be visible.

d) section 4.1.1, page 35 :

Either single-sided or double-sided disk drives may be installed in the PDQ-3 computer. Double-sided drives differ from single-sided drives as follows:

1) Double sided drives allow both sides of a diskette to be used for data storage.

2) Double sided drives are equipped with a Drive Access LED indicator light mounted on the Diskette Ejector. This LED is lit whenever the drive is selected by the Floppy Drive Controller.

should be changed to :

Either single-sided or double-sided disk drives may be installed in the PDQ-3 computer. Double sided drives allow both sides of a diskette to be used for data storage. All double-sided drives, and Shuggart single-sided drives are equipped with a Drive Access LED indicator light mounted on the Diskette Ejector. This LED is lit whenever the drive is selected by the Floppy Drive Controller and the head is loaded.

III. Applications Notes

1) A problem exists in the interaction between the PDQ-3 CPU and an interrupting device. When the PDQ-3 is running with the interrupt system enabled, an interrupt request from a device requiring processor intervention is latched at the beginning of a PDQ-3 instruction cycle. The interrupt vector is requested of the device at the end of the PDQ-3 instruction cycle. If the result of that PDQ-3 intruction cycle is to disable the interrupting device, the device does not know to supply an interrupt vector to the PDQ-3 when one is requested. Hence, the PDQ-3 waits for the vector forever. The solution to this problem is to make sure that the interrupt system is disabled before any device is disabled.

   Another facet of this problem applies to disabling the interrupt system. If an interrupt occurs at the beginning of an instruction that disables the interrupt system (by storing a 0 into the INTEN bit of the System Status Register), the interrupt is latched. The interrupt system becomes disabled as planned, but the PDQ-3 processor vectors to the interrupt routine anyway. Typically, the interrupt routine will re-enable the interrupt system and wait on another interrupt. When control is returned to the process that disabled the interrupt system, the interrupt is found to be enabled (even though that process thought it had been disabled). One reliable way to make sure that the interrupt system is disabled is to loop, turning off the interrupt system, until the INTEN bit of the System Status Register is seen to be 0.

2) There is a bug in the PDQ-3 DMA Controller that shows up when a device interrupt from the Floppy Controller arrives at the DMA Controller while the DMA Controller is requesting control of the Q-Bus. The DMA Controller freezes, as does the entire PDQ-3. This occurs only during track format operations (track read and track write) when the Floppy Controller encounters an index mark and interrupts the DMA Controller at the critical time. The solution is to program the DMA Count Registers so that the DMA transfer has terminated before the index pulse is sensed.