# 6

# Electrical Information

## Absolute Maximum Ratings

**Table 6-1. Absolute Maximum Ratings**

| Parameter | Range |
|---|---|
| Storage temperature | -65° to 150° C |
| Power supply voltage | 0 to 7 Volts |
| Voltage on any pin | -0.5 to Vcc+0.5 Volts |

## Operating Conditions

**Table 6-2. Operating Conditions**

| Parameter | Range |
|---|---|
| Ambient temperature | 0° to 70° C |
| Supply voltage | 4.5 to 5.5 Volts |
| Rise Time $t_r$ | ns |
| Fall Time $t_f$ | ns |
| Load Capacitance $C_L$ | 50 pf, unless otherwise noted |

# DC Electrical Characteristics

**Table 6-3. DC Electrical Characteristics**

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{il}$ | Input Low Voltage, All Pins | | | | 0.8 | V |
| $V_{ih}$ | Input High Voltage, All Pins | | 2.0 | | | V |
| $V_h$ | Input Hysteresis, SCSI Signals Only | | 200 | | | mV |
| $V_{ol1}$ | Output Low Voltage, PORTEN* | $I_{ol}$ = 2 mA | | | 0.5 | V |
| $V_{ol2}$ | Output Low Voltage, SD0-15, DRQ, IRQ, IOCS 16* | $I_{ol}$ = 24 mA | | | 0.5 | V |
| $V_{ol3}$ | Output Low Voltage, All SCSI Signals | $I_{ol}$ = 48 mA | | | 0.5 | V |
| $V_{oh1}$ | Output High Voltage, PORTEN* | $I_{ol}$ = –2 mA | 2.4 | | | V |
| $V_{oh2}$ | Output High Voltage, SD0-15 DRQ, IRQ | $I_{ol}$ = –8 mA | 2.4 | | | V |
| $I_{o2}$ | Output Leakage for Tristate and Open Collector Drivers | $V_{dd} \geq Vin \geq GND$ | | ±40 | | A |
| $I_{dd1}$ | Operating Current Consumption | 20 MHz External Clock | | 19.8 | 25 | mA |
| | | 20 MHz Internal Crystal Oscillator | | 29.0 | 35 | mA |
| $I_{dd2}$ | Powerdown Current Consumption | 20 MHz External Clock | | 5.8 | 10 | mA |
| | | 20 MHz Internal Crystal Oscillator | | 14.2 | 20 | mA |
| $I_{dd3}$ | Static Current Consumption | $V_{IN} = V_{dd}$, Pin F1 = $V_{dd}$ | | 1.5 | 5 | mA |
| $C_{IN}$ | Input Capacitance | $F_c$ = 1 MHz | | | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | | | 15 | pF |

# Crystal Oscillator Specification

**Table 6-4. Crystal Oscillator Specification**

| Parameter | Value |
|---|---|
| Design type | Pierce |
| Min. resistor shunting XIN and XOUT | 21,000 |
| Max. capacitance between XIN and XOUT | 12 pF[1] |
| Max. motional resistance of crystal | 50 ohm |
| Oscillation mode | Fundamental |
| Min. crystal Q | 20,000 |
| Oscillation frequency | 20 MHz |
| [1] including Co of crystal and board layout | |

**Notes:**

- Crystal cut is not critical, if fundamental is the strongest oscillation mode.
- The required capacitors are contained on the chip.
- Do not ground any crystal terminals.
- Since the oscillator is an analog device, it should experience as little power supply noise as possible. This means that the user must not inject PC board noise into XNE (VDD of the oscillator), and there should be a well-filtered internal VSS pin as close to the cell as possible. Switching noise on the outer VSS bus is isolated from the circuit and therefore is not a problem. Furthermore, the X1 input pin is sensitive to latch-up at voltages above approximately 80 mA.

# System Timing

This section contains AC timing information for the AIC-6360. All timing presumes operation with a 20 MHz clock.

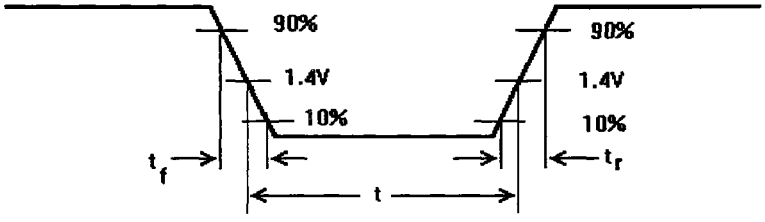
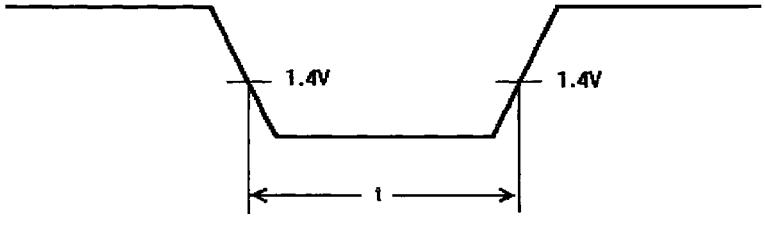



**Figure 6-1. AC Input Conditions**




C = 50 pf unless otherwise noted

**Figure 6-2. AC Output Conditions**

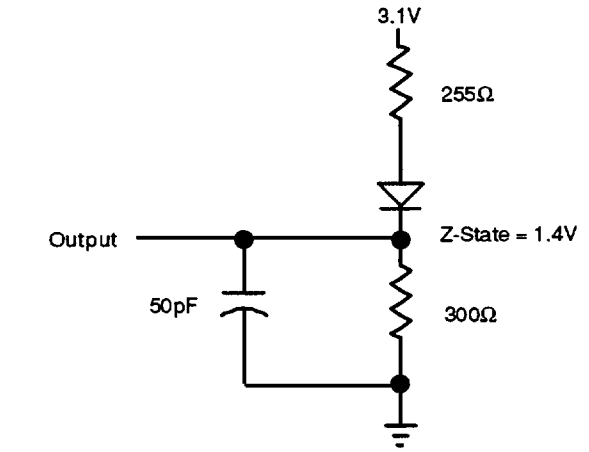



**Figure 6-3. AC Test Load for All Outputs Except SCSI and PORTEN**

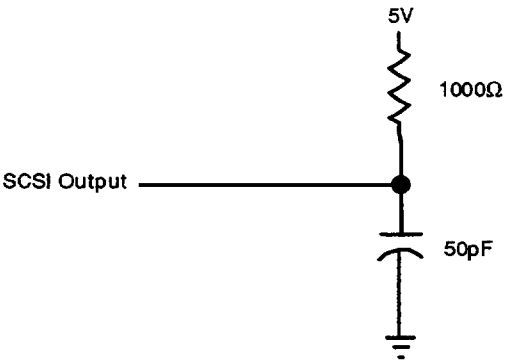



**Figure 6-4. AC Test Load for SCSI Outputs**

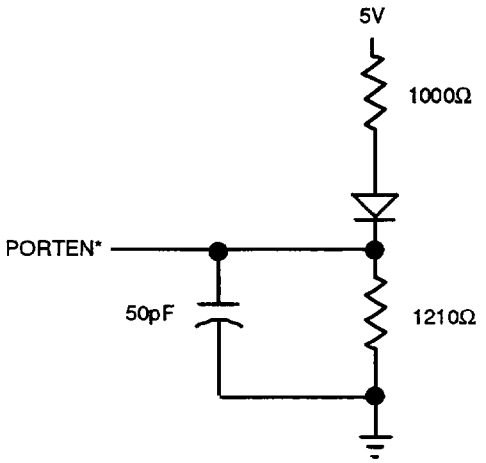
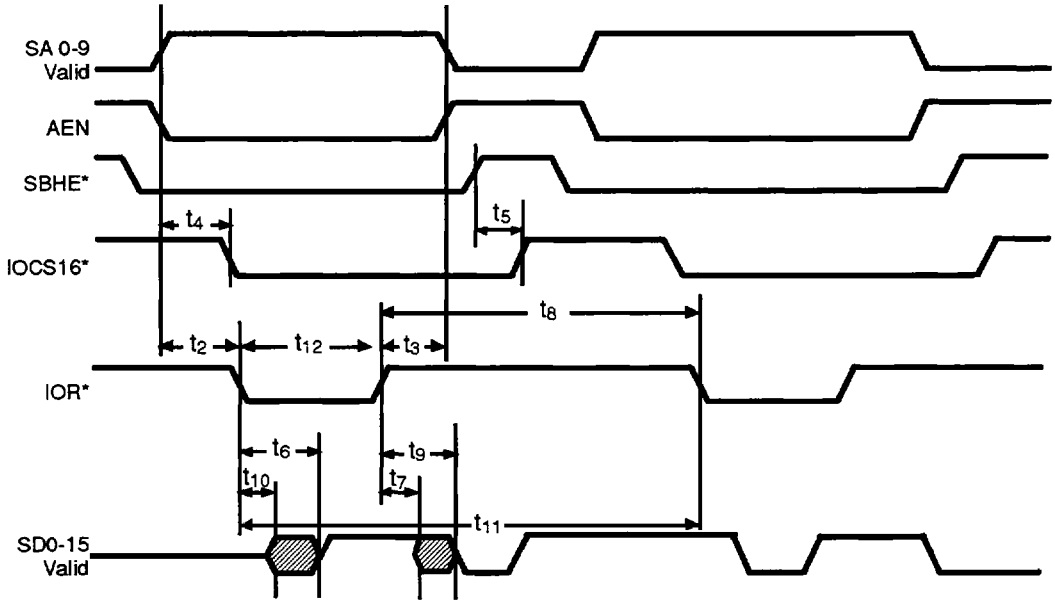



**Figure 6-5. AC Test Load for PORTEN Output**

## Host Processor PIO Data Read Operation



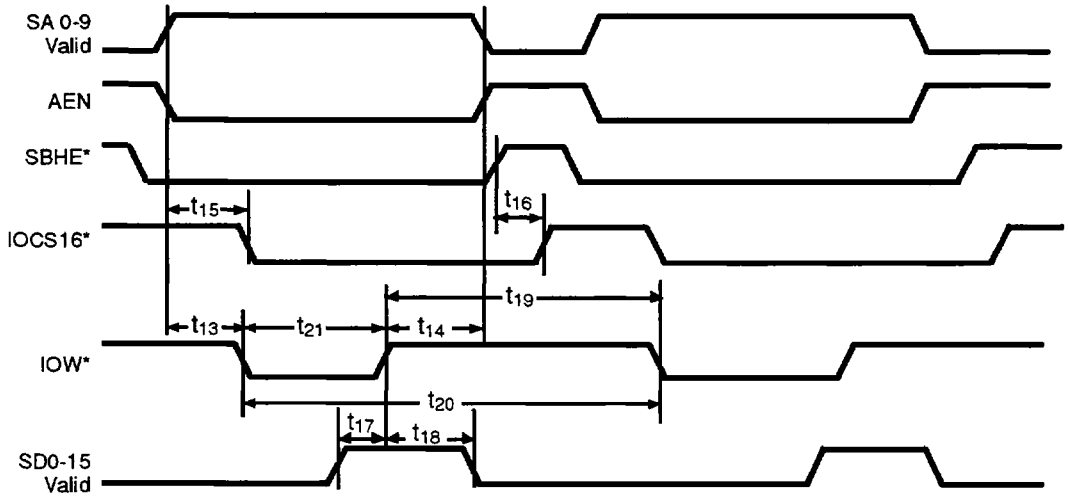

| Parameter | Description | Min[1] | Max[1] |
|---|---|---|---|
| $t_1$ | Chip clock period | 50 | |
| $t_2$ | Address setup time to IOR* falling | 25 | |
| $t_3$ | Address hold time after IOR* rising | 25 | |
| $t_4$ | IOCS16* valid after address and SBHE* valid | | 60 |
| $t_5$ | IOCS16* disabled after address and SBHE* invalid | | 30 |
| $t_6$ | Valid data delay from IOR* falling | 6 | 60 |
| $t_7$ | Data hold time after IOR* rising | 4 | |
| $t_8$ | Time between consecutive IOR* pulse | 100 | |
| $t_9$ | Driver OFF time from IOR* rising | | 25 |
| $t_{10}$ | Driver ON time from IOR* falling | 6 | 25 |
| $t_{11}$ | Read cycle time | 120 | |
| $t_{12}$ | IOR* pulse width | 20 | |

[1] Min and Max data in all the timing diagrams is given in nanoseconds.

**Notes:**

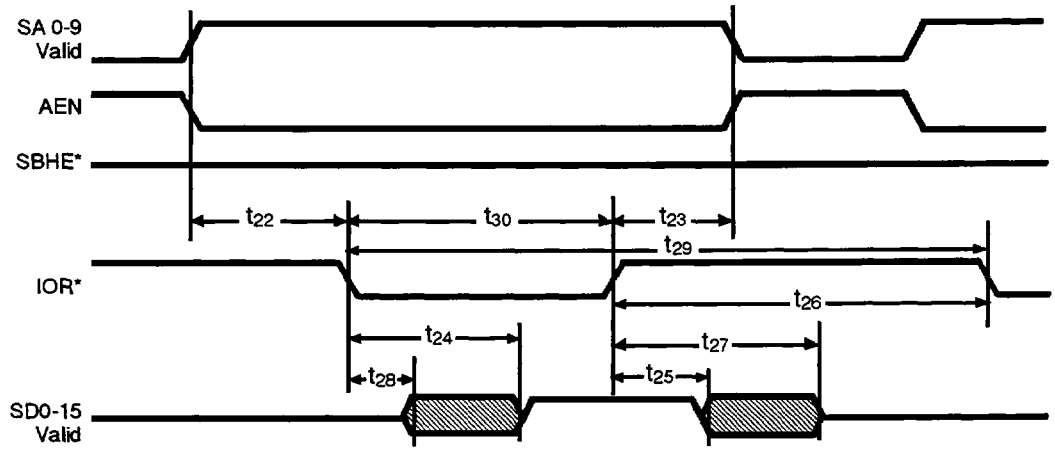
- $t_6$ is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.
- $t_7$ is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.
- $t_9$ is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.
- $t_{10}$ is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tristate bias voltage level of 1.4V.

## Host Processor PIO Data Write Operation




| Parameter | Description | Min | Max |
|---|---|---|---|
| $t_{13}$ | Address setup time to IOW* falling | 25 | |
| $t_{14}$ | Address hold time after IOW* rising | 25 | |
| $t_{15}$ | IOCS16* valid after address and SBHE* valid | | 60 |
| $t_{16}$ | IOCS16* hi-z after address and SBHE* invalid | | 30 |
| $t_{17}$ | Data setup time to IOW* rising | 5 | |
| $t_{18}$ | Data hold time after IOW* rising | 15 | |
| $t_{19}$ | Time between consecutive IOW* pulses | 100 | |
| $t_{20}$ | Write cycle time | 110 | |
| $t_{21}$ | IOW* pulse width | 10 | |

## Host Processor I/O Read Operation

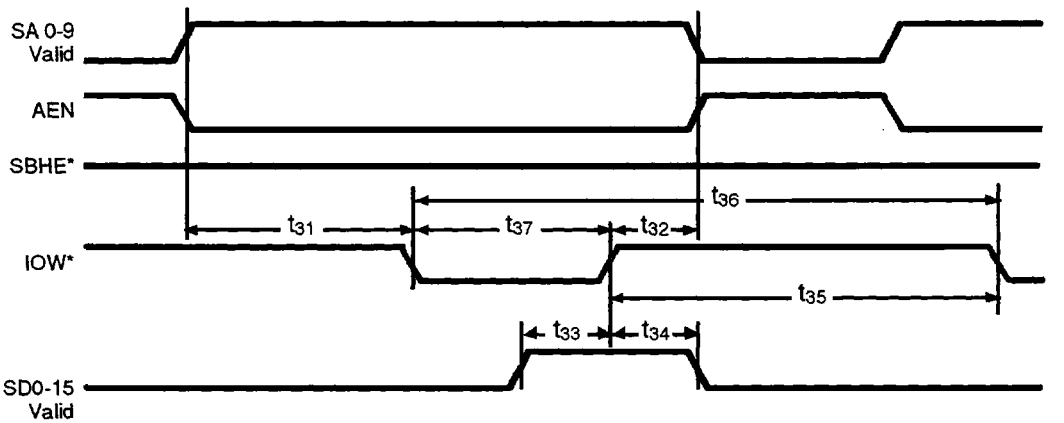



| Parameter | Description | Min | Max |
|---|---|---|---|
| t22 | Address setup time to IOR* falling | 25 | |
| t23 | Address hold time after IOR* rising | 25 | |
| t24 | Valid data delay from IOR* falling | | 60 |
| t25 | Data hold time after IOR* rising | 4 | |
| t26 | Time between consecutive IOR* pulses (DWORD) | 100 | |
| t27 | Driver OFF time from IOR* rising | | 25 |
| t28 | Driver ON time from IOR* falling | 6 | 25 |
| t29 | Read cycle time | 120 | |
| t30 | IOR* pulse width | 20 | |

**Notes:**

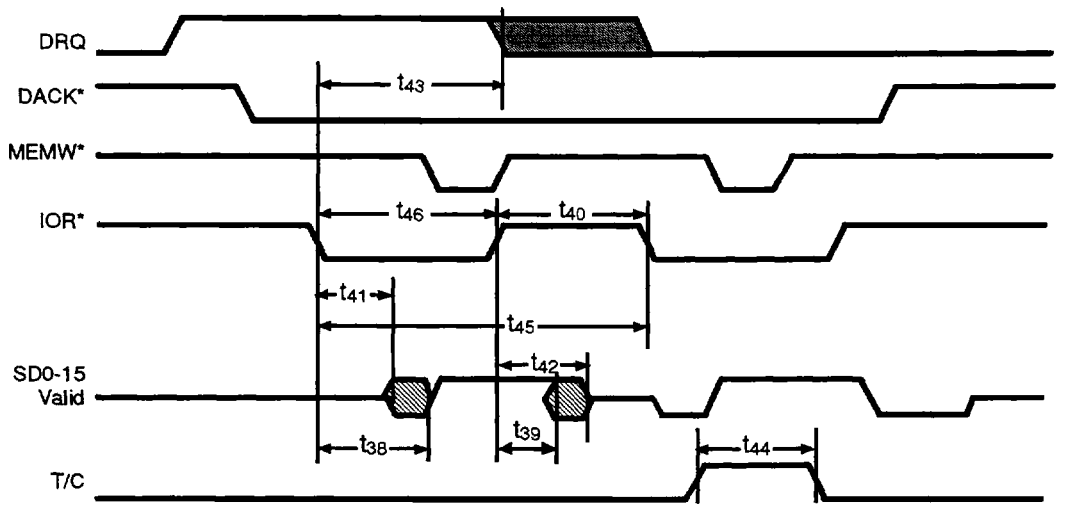
- $t_{24}$ is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.
- $t_{25}$ is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.
- $t_{27}$ is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.
- $t_{28}$ is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tristate bias voltage level of 1.4V.

## Host Processor I/O Write Operation




| Parameter | Description | Min | Max |
|---|---|---|---|
| t31 | Address setup time to IOW* falling | 25 | |
| t32 | Address hold time after IOW* rising | 25 | |
| t33 | Data setup time to IOW* rising | 5 | |
| t34 | Data hold time after IOW* rising | 15 | |
| t35 | Time between consecutive IOW* pulses (DWORD) | 100 | |
| t36 | Write cycle time | 110 | |
| t37 | IOW* pulse width | 10 | |

## Host Processor DMA Read Operation

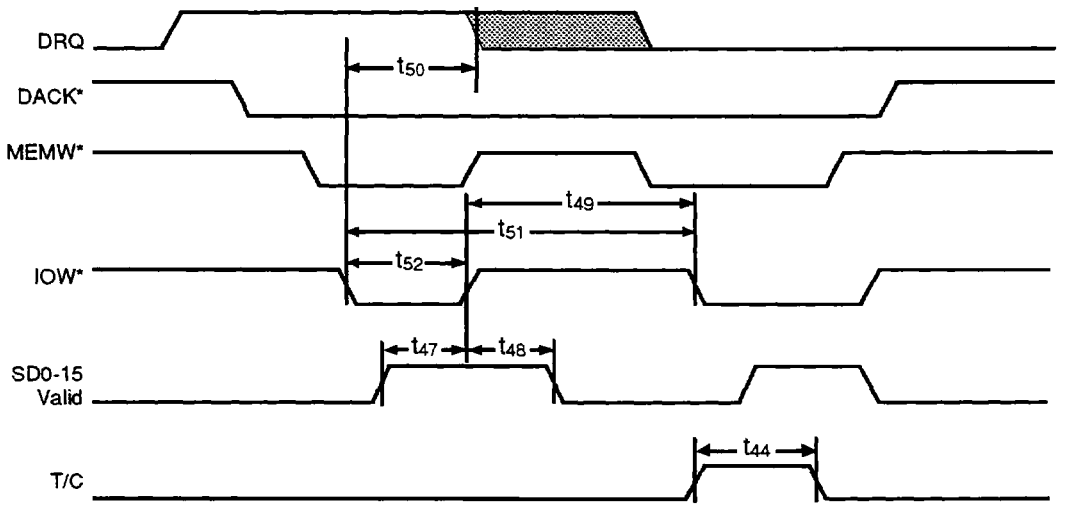



| Parameter | Description | Min | Max |
|---|---|---|---|
| $t_{38}$ | Data valid from IOR* falling | | 60 |
| $t_{39}$ | Data hold time after IOR* rising | 4 | |
| $t_{40}$ | Time between consecutive IOR* | 100 | |
| $t_{41}$ | Driver ON time from IOR* falling | | 25 |
| $t_{42}$ | Driver OFF time from IOR* rising | | 25 |
| $t_{43}$ | DRQ OFF time from IOR* falling | 10 | 60 |
| $t_{44}$ | Terminal count pulse width | 50 | |
| $t_{45}$ | Read cycle time | 120 | |
| $t_{46}$ | IOR* pulse width | 20 | |

**Notes:**

- $t_{38}$ is measured from the assertion of IOR* to the point at which the outputs on SD0-15 achieve a valid Voi or Voh output voltage level.
- $t_{39}$ is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 no longer maintain a valid Voi or Voh output voltage level.
- $t_{40}$ is measured from the deassertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from their asserted high or low logic level.
- $t_{41}$ is measured from the assertion of IOR* to the point at which the outputs on SD0-15 deviate by 0.1V from the tristate bias voltage level of 1.4V.

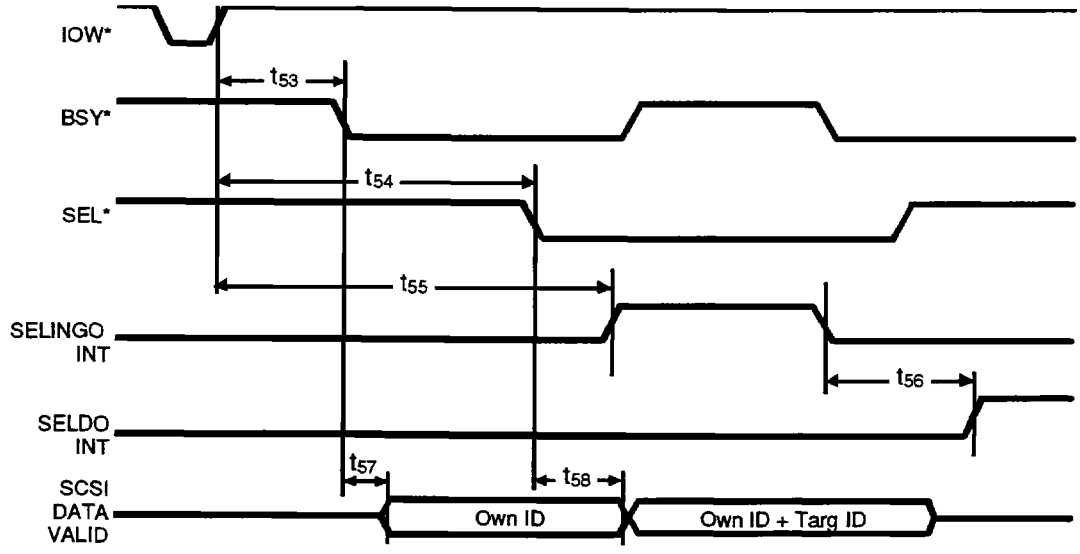
## Host Processor DMA Write Operation




| Parameter | Description | Min | Max |
|---|---|---|---|
| $t_{47}$ | Data setup time to IOW* rising | 5 | |
| $t_{48}$ | Data hold time to IOW* rising | 15 | |
| $t_{49}$ | Time between consecutive IOW* pulses | 100 | |
| $t_{50}$ | DRQ off time from IOW* falling | 10 | 60 |
| $t_{51}$ | Write cycle time | 110 | |
| $t_{52}$ | IOW* pulse width | 10 | |

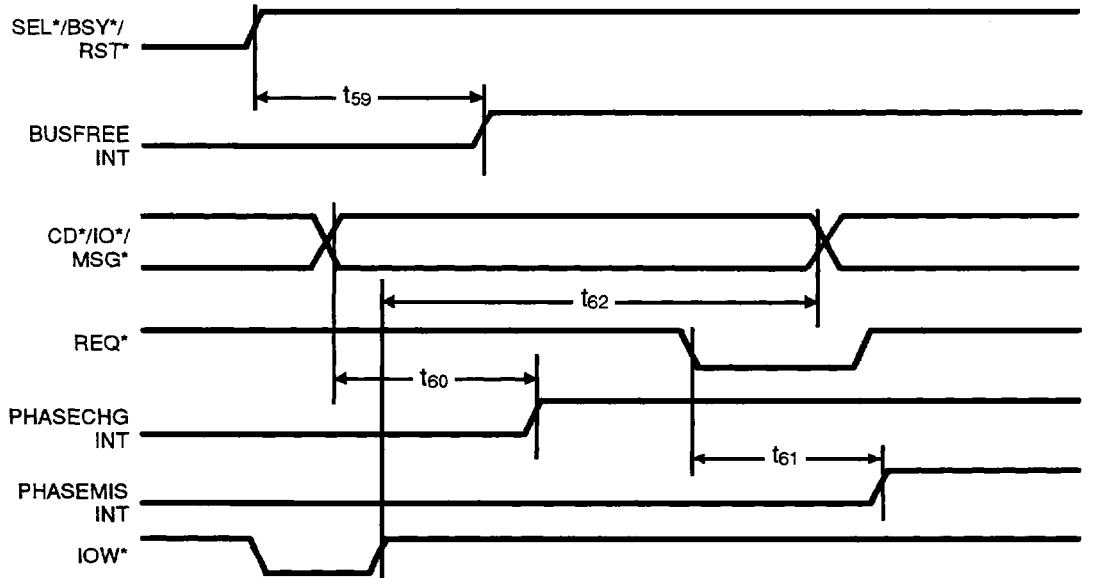
# SCSI Bus Timing

## Arbitration/Selection



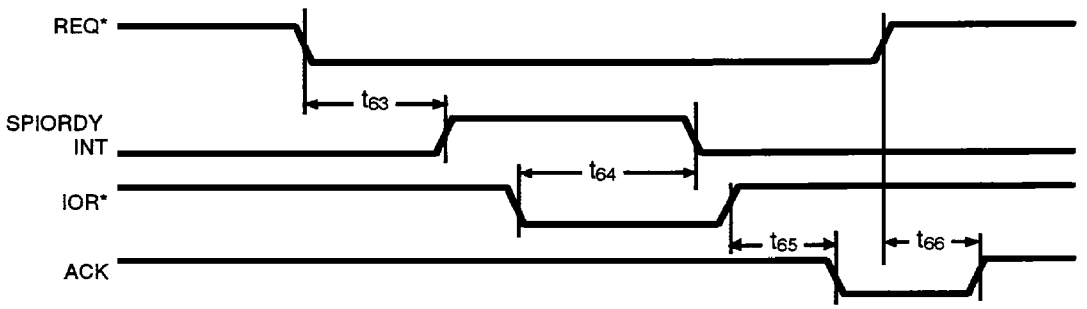

| Parameter | Description | Min | Max |
|---|---|---|---|
| $t_{53}$ | BSY* active from IOW* rising | | $16t_{1} + 60$ |
| $t_{54}$ | SEL* active from IOW* rising | | $64t_{1} + 60$ |
| $t_{55}$ | SELINGO interrupt from ENSELO | | $92t_{1} + 60$ |
| $t_{56}$ | SELDO interrupt from Target BSY* | | $4t_{1} + 60$ |
| $t_{57}$ | Own ID valid from BSY* falling | | 20 |
| $t_{58}$ | Target ID valid from SEL* falling | $24t_{1} + 60$ | |

## SCSI Bus Free Detection and Phase Change Interrupts



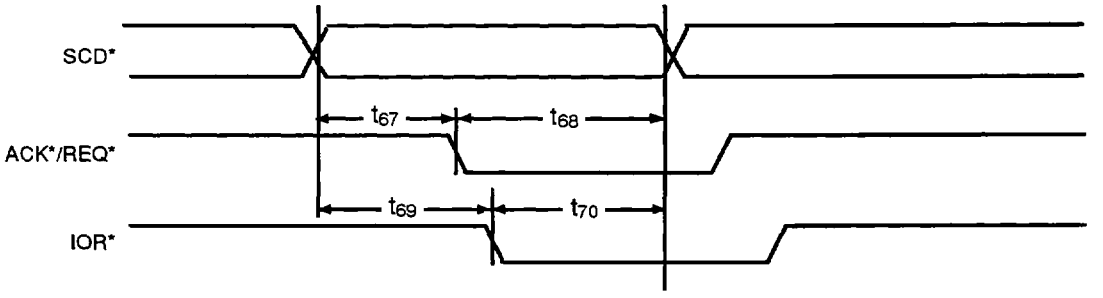

| Parameter | Description | Min | Max |
|---|---|---|---|
| $t_{59}$ | BUS FREE from SEL*/BSY*/RST* rising | | $9t_{1}+40$ |
| $t_{60}$ | Interrupt from phase change | | 37 |
| $t_{61}$ | Interrupt from phase change/REQ | | 40 |
| $t_{62}$ | Phase change[1] from IOW* rising | | 46 |
| [1] Target mode | | | |

## SCSI PIO




| Parameter | Description | Min | Max |
|---|---|---|---|
| $t_{63}$ | SPIORDY interrupt from REQ* falling | | $3t_1 + 35$ |
| $t_{64}$ | SPIORDY cleared from IOR* falling | | 60 |
| $t_{65}$ | ACK asserted from IOR* rising | | $3t_1 + 35$ |
| $t_{66}$ | ACK de-asserted from REQ* rising | | $2t_1 + 62$ |

## SCSI Data Setup and Hold, Latched Data and PIO




| Parameter | Description | Min | Max |
|---|---|---|---|
| t67 | SCSI Data setup to REQ* or ACK*[1] | 5 | |
| t68 | SCSI Data hold after REQ* or ACK*[1] | 15 | |
| t69 | SCSI Data setup to IOR* falling[2] | 15 | |
| t70 | SCSI Data hold after IOR* falling[2] | 5 | |

[1] Initiator mode uses leading edge of REQ* to latch data, and Target mode uses leading edge of ACK*. These times apply to synchronous, asynchronous, and auto PIO modes.

[2] These times apply to programmed I/O when reading port 347h.