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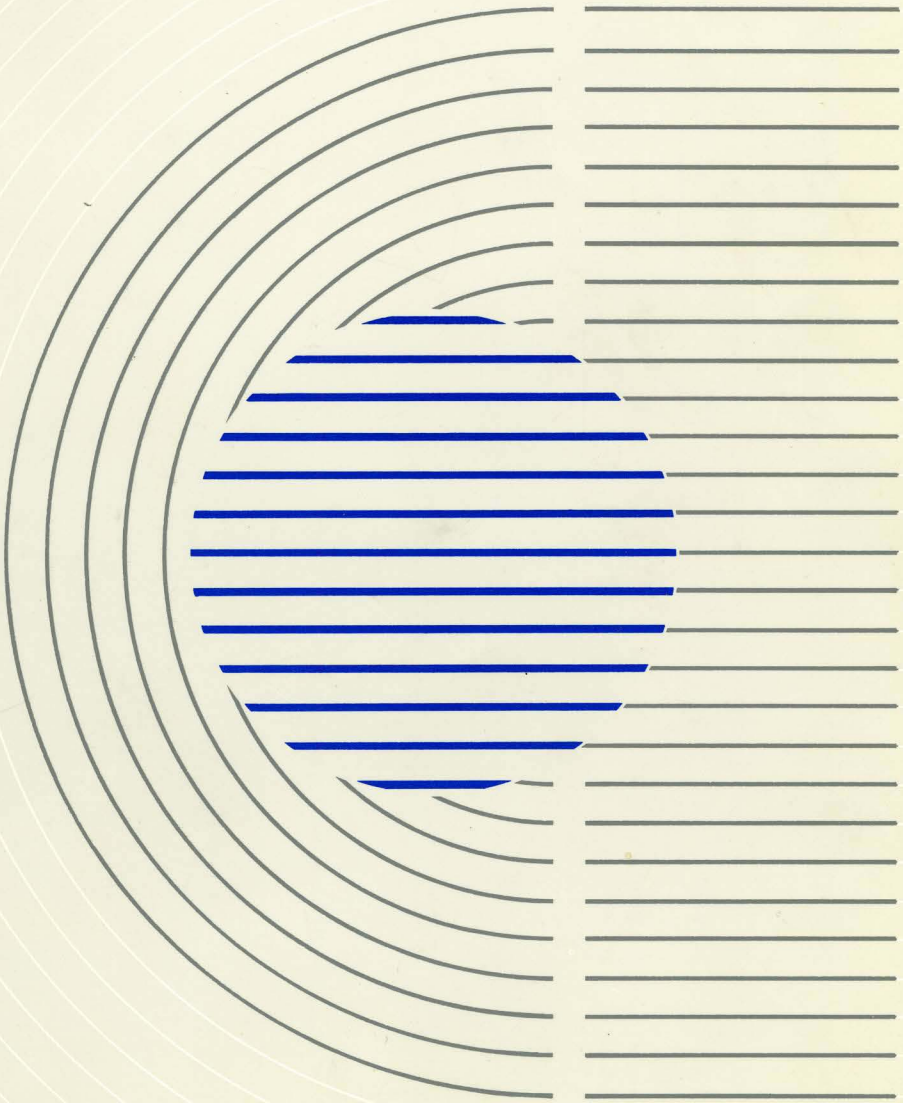
ACB-4000
OEM Manual



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ACB-4000
5¼" Winchester Disk Controller
OEM Manual

March, 1984

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Literature Department
580 Cottonwood Drive
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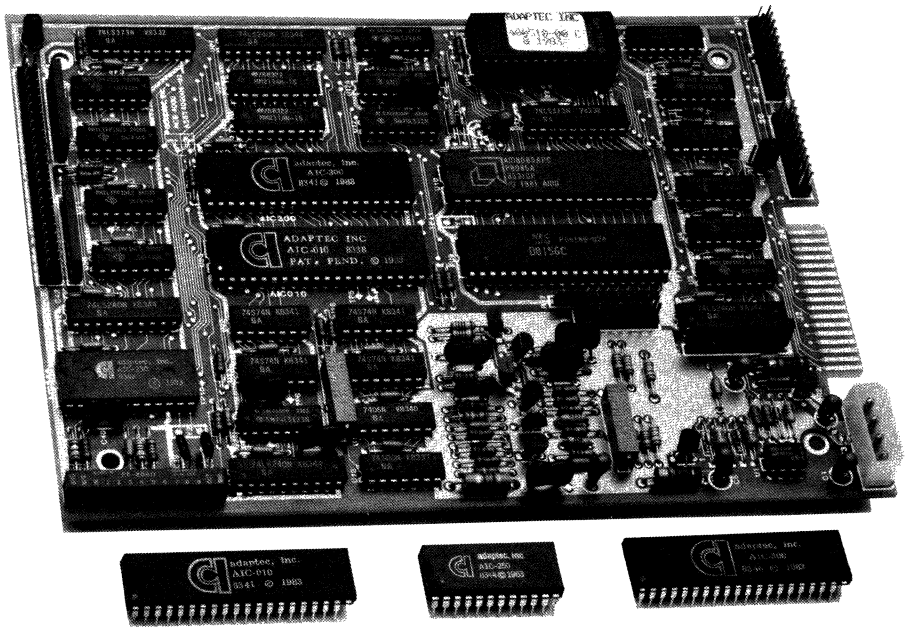


ACB-4000
5¼" Hard Disk
Controller

Introduction 1.0

The Adaptec ACB-4000 5¼" Hard Disk Controller board interfaces ST506-type Winchester disk drives to any ANSI X3T9.2 SCSI (Small Computer System Interface) standard host adapter interface.

BASIC DESCRIPTION 1.1

The ACB-4000 controller supports standard SCSI features plus extensions and controls two Seagate ST-506/412 or equivalent Winchester drives.

FEATURE SET 1.2

1) The ACB-4000 utilizing a 1K, dual-ported buffer, eliminates the need for sector interleaving. This allows the host to read a track of data in a single revolution of the disk.
2) The ACB-4000 auto-configures to any size, previously formatted, 5¼" drive, eliminating the need for host initialization of the controller for various drive types.
3) The ACB-4000 handles defects on a sector level transparent to the host. Since no alternate tracks are used, lengthy seeks to alternate tracks are eliminated and disk capacity is maximized.
4) The ACB-4000 guarantees maximum data integrity by utilizing a 32-bit ECC on both the data and ID fields. The computer-generated code provides correction of single-burst 8-bit errors.
5) The ACB-4000 offers variable sector lengths from 256 bytes to 1K bytes. The sector length is programmed at format time.
6) The ACB-4000 supports a high-speed data search where a programmed full sector bit pattern can be compared for an equal or unequal bit pattern within a range of sectors.

Physical Specifications 2.0

SIZE 2.1

The ACB-4000 is designed to fit in the form factor of a standard 5¼" drive. The physical dimensions of the controller are as follows:

Length: 7.75 inches (19.7 cm)
Width: 5.75 inches (14.6 cm)
Height: 0.75 inches (1.9 cm)
Weight: 1 pound, with packaging

POWER REQUIREMENTS 2.2

+5 VDC ± 5% at 1.5 amps (max.)
+12 VDC ± 10% at 300 mA (max.)

Power is applied through J3, 4-pin AMP connector. The recommended mating connector is AMP P/N 1-480424-0. J3 pins are numbered as shown in Figure 2-1.

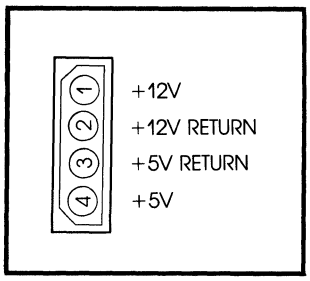


Figure 2-1. Connector J3 Pin Assignments

ENVIRONMENTAL LIMITS 2.3

	Operating	Storage
Temperature F/C	32/0 to 131/55	−40/−40 to 167/75
Humidity (non-cond.)	10% to 95%	10% to 95%
Altitude, ft.	Sea Level to 10,000	Sea Level to 20,000

HOST ADAPTER INTERFACE 3.1

The Adaptec ACB-4000 controller interfaces to a host adapter according to the proposed ANSI X3T9.2 Standard (SCSI). The data bus is a bidirectional 8-bit parallel interface.

3.1.1 HOST ADAPTER INTERFACE—PHYSICAL

A 50-pin flat ribbon connector is provided at J4. The 3M P/N 3425-3000 cable connector is recommended.

Single ended drivers and receivers allow a maximum cable length of 20 feet (6 meters) between the host adapter and the controller. All signals are low true. All odd pins are grounded. Figure 3-1 shows the SCSI bus pin assignments.

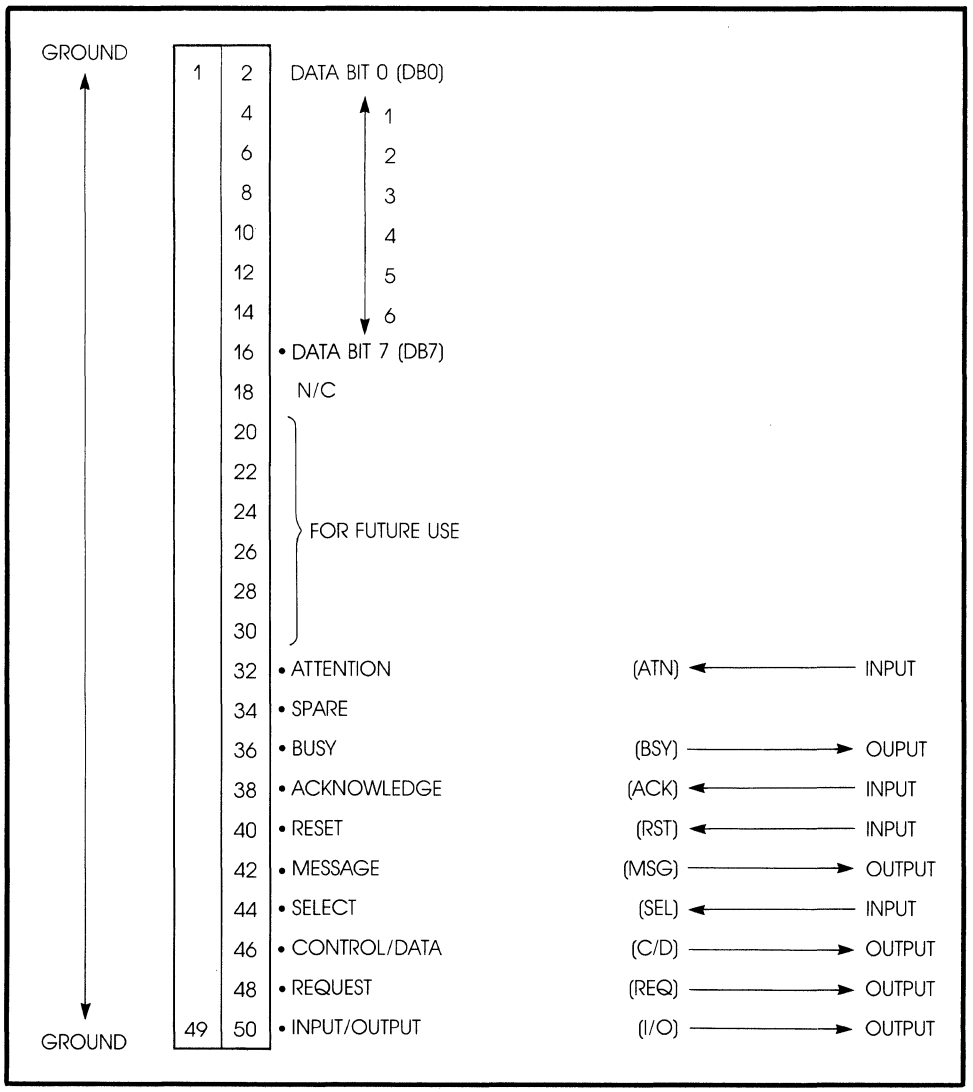


Figure 3-1. SCSI Bus Pin Assignments

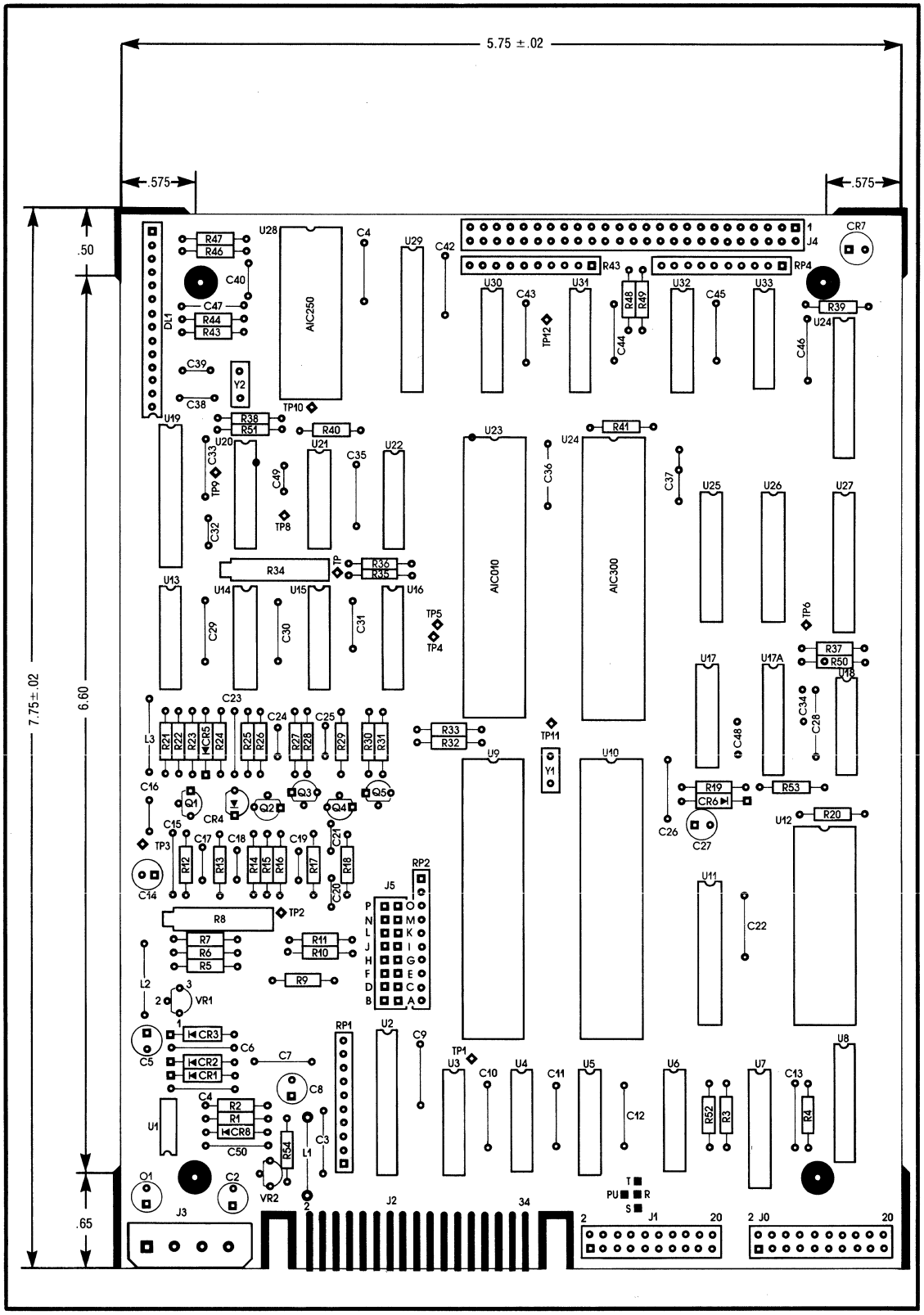


Figure 3-2.
ACB-4000 Board
Layout and
Connectors

3.1.2 HOST ADAPTER INTERFACE—ELECTRICAL

All signals are low true and use open collector drivers terminated with 220 ohms to +5 volts (nominal) and 330 ohms to ground at each end of the cable.

Each signal driven by the controller has the following output characteristics:

True (Signal Assertion) = 0.0 to 0.4 VDC @ 48 mA (max.)
False (Signal Non-Assertion) = 2.5 to 5.25 VDC

Adaptec controllers use a 7438 open collector driver to meet this specification.

Each signal from the host to the controller must have the following characteristics:

True (Signal Assertion) = 0.0 to 0.8 VDC @ .4 mA (max.)
False (Signal Non-Assertion) = 2.0 to 5.25 VDC

A 74LS14 receiver with hysteresis meets this specification.

Figure 3-3 shows an example of proper bus termination.

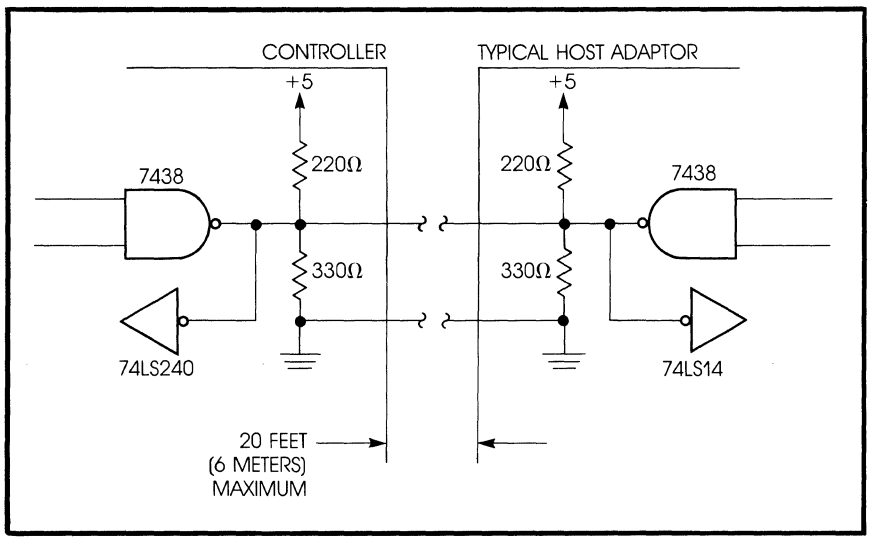


Figure 3-3. Host Adapter Bus Termination

3.2 DISK DRIVE INTERFACE

The ACB-4000 controller complies with the standard ST-506/412 interface.

A system interconnect diagram is shown in Figure 3-4. Board layout for connector positioning is shown in Figure 3-2.

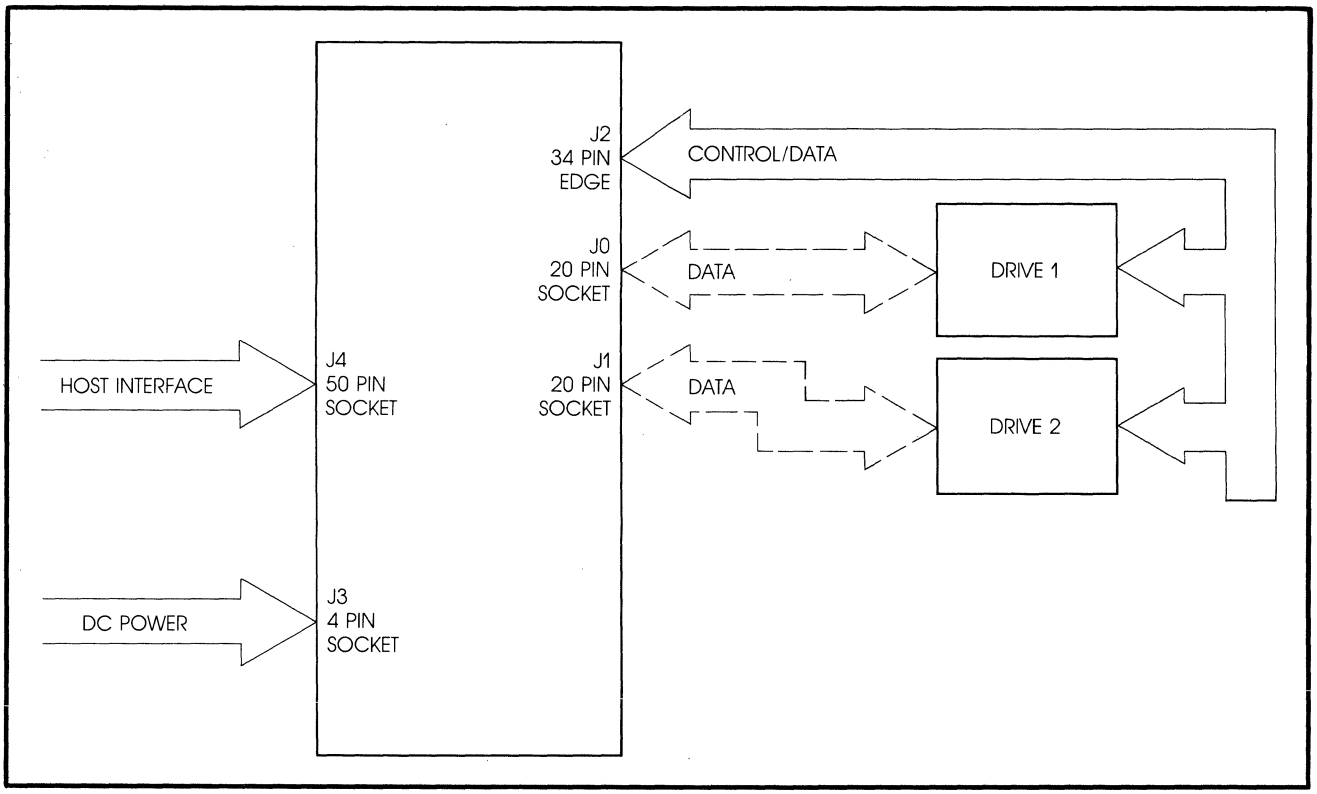


Figure 3-4. System Interconnect Diagram

3.2.1 DISK DRIVE INTERFACE—PHYSICAL

J2 is a 34-pin edge connector to which all drive control lines are daisy chained. Maximum cable length is 20 feet (6 meters). The suggested mating connector for this ribbon cable is 3M P/N 3402-0000.

The pins are numbered 1 through 34 with the even pins located on the component side of the controller board. Pin 2 is the pin closest to the power connector (J6). Table 3-1 shows pin assignments for connector J2.

J0 and J1 are the radial data connectors to each disk drive. Maximum cable length should not exceed 20 feet (6 meters). Suggested mating sockets for these connectors is 3M P/N 3421 Series. Table 3-2 shows pin assignments for connectors J0 and J1.

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
1	2	Reduced Write Current/Head Select 2^3
3	4	Head Select 2^2
5	6	Write Gate
7	8	Seek Complete
9	10	Track 0
11	12	Write Fault
13	14	Head Select 2^0
15	16	Reserved
17	18	Head Select 21
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Drive Select 4
33	34	Direction In

Table 3-1.
J2 Connector Pin Assignment

GND RTN PIN	SIGNAL PIN	SIGNAL NAME
2	1	Drive Selected
4	3	Reserved
6	5	Reserved
8	7 9,10	Reserved Reserved
12	11 13 14	GND MFM Write Data MFM Write Data
16	15 17 18	GND MFM Read Data MFM Read Data
20	19	GND

Table 3-2.
J0 and J1 Connector Pin Assignment

3.2.2 DISK DRIVE INTERFACE—ELECTRICAL

The last physical drive on the control bus daisy chain must be terminated with a resistor pack provided by the drive manufacturer. The control signal driver/receiver electrical specifications are shown in Figure 3-5.

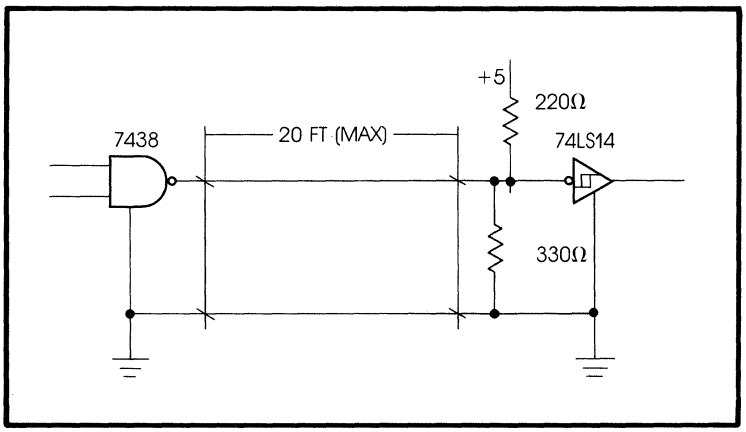


Figure 3-5. Control Driver/ Receiver Lines

The control signals are specified at:

True = 0.0 VDC to 0.4 VDC @ I = −48 mA (max.)
False = 2.5 VDC to 5.25 VDC @ I = +250 µA (open collector)

The read and write MFM data lines are differential signals, present on connectors J0 and J1. The Adaptec receiver/driver pairs meet the required RS-422 specifications. Figure 3-6 shows these lines for the ACB-4000.

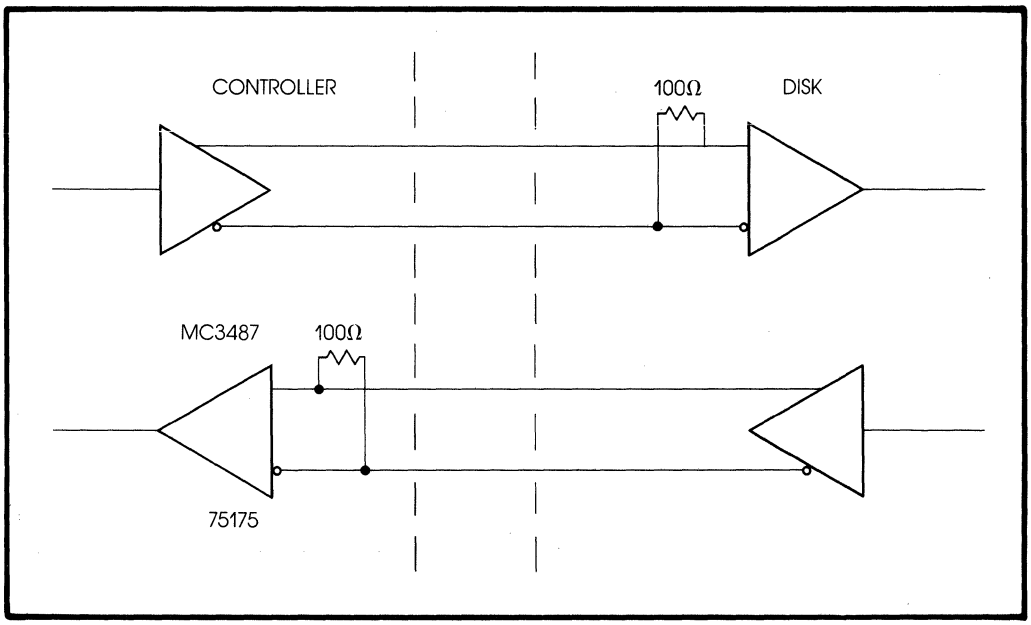


Figure 3-6. ACB-4000 Data Receiver/Driver Pairs

ACB-4000 SCSI FEATURES 4.1

This section describes in detail the SCSI protocol with the extensions which are implemented in the Adaptec ACB-4000 controller. The extended functions of the SCSI standard not supported by the ACB-4000 are command chaining and disconnection and reconnection. When designing systems for the ACB-4000 series, you may go directly from the "bus free" phase to the "selection" phase in the protocol description.

GENERAL DESCRIPTION OF SCSI 4.2

This system interface provides an efficient method of communication between computers and peripheral I/O devices. The eight-port, daisy-chained bus defined by this specification supports the following features:

- Single or multiple host system.
- Multiple peripheral devices and device types.
- Bus contention resolution through arbitration on a prioritized basis.
- Asynchronous data transfer at up to 1.5 MBytes/sec.
- Host-to-host communication.

Communication on the bus is allowed between two bus ports at a time. A maximum of eight bus ports are allowed. Each port is attached to a device (e.g. controller or host adapter).

When two devices communicate with each other on the bus, one acts as an INITIATOR and the other acts as a TARGET. The TARGET (typically a controller) executes the operation. A device will usually have a fixed role as an INITIATOR or TARGET, but some devices may be able to assume either role.

An INITIATOR may address up to two peripheral I/O devices that are connected to an ACB-4000 TARGET. The TARGET will provide a "virtual controller" for each of these devices, appearing to the system as two separate controller/device pairs.

Certain bus functions are assigned to the INITIATOR and certain bus functions are assigned to the TARGET. The INITIATOR may arbitrate for the bus and select a particular TARGET. The TARGET may request the transfer of COMMAND, DATA, STATUS or other information on the bus.

Data transfers on the bus are asynchronous and follow a defined REQUEST/ ACKNOWLEDGE handshake protocol. One eight-bit byte of information may be transferred with each handshake.

4.3 BUS SIGNALS

The nine control signals and eight data signals are described below:

4.3.1 BUSY (BSY)

BSY is an "or-tied" signal which indicates that the bus is in use.

4.3.2 SELECT (SEL)

SEL is an "or-tied" signal used by an INITIATOR to select a TARGET or by a TARGET to reselect an INITIATOR.

4.3.3 CONTROL/DATA (C/D)

C/D is a TARGET-driven signal to indicate whether CONTROL or DATA information is on the data bus. Assertion indicates CONTROL.

4.3.4 INPUT/OUTPUT (I/O)

I/O is a TARGET-driven signal which controls the direction of data movement on the data bus relative to an INITIATOR. Assertion indicates INPUT to the INITIATOR.

4.3.5 MESSAGE (MSG)

MSG is a TARGET-driven signal indicating the MESSAGE phase.

4.3.6 REQUEST (REQ)

REQ is a TARGET-driven signal indicating a request for a REQ/ACK data transfer handshake.

4.3.7 ACKNOWLEDGE (ACK)

ACK is an INITIATOR-driven signal indicating acknowledgment of a REQ/ACK data transfer handshake.

4.3.8 ATTENTION (ATN)

ATN is an INITIATOR-driven signal indicating the ATTENTION condition.

4.3.9 RESET (RST)

RST is an "or-tied" signal indicating the RESET condition.

4.3.10 DATA BUS (DB: 7-0)

Eight data bit signals comprise the DATA BUS. DB(7) is the most significant bit and has the highest priority during arbitration. Significance and priority decrease with decreasing bit number.

Each of the eight data signals DB(7) through DB(0) is uniquely assigned as a TARGET or INITIATOR bus address (i.e., DEVICE ID) which is normally assigned and "strapped" in the device during system configuration. In order to obtain the bus during arbitration, a device asserts its assigned data bit (DEVICE ID) and leaves the other data bits in the passive (non-driven) state.

BUS PHASES 4.4

The SCSI bus implemented by the ACB-4000 has six distinct operational phases and cannot be in more than one phase simultaneously.

- BUS FREE Phase
- SELECTION Phase
- COMMAND Phase
- DATA Phase
- STATUS Phase
- MESSAGE Phase

} Information Transfer Phases

4.4.1 BUS FREE PHASE

The BUS FREE phase, indicating that the bus is available for use, is invoked by the deassertion and passive release of all bus signals. All active devices must deassert and passively release all bus signals (within a BUS CLEAR DELAY) after deassertion of BSY and SEL.

Devices sense BUS FREE when both SEL and BSY are not asserted (simultaneously within a DESKEW DELAY) and the RESET condition is not active.

4.4.2 SELECTION PHASE

The SELECTION phase allows an INITIATOR to select a TARGET. The INITIATOR waits a minimum of BUS SETTLE DELAY (after detecting BUS FREE) before driving the DATA bus with the TARGET ID and (optionally) its own ID. After two DESKEW DELAYS, the INITIATOR can assert SEL.

On detecting the simultaneous condition (within one DESKEW DELAY) of SEL, its own ID asserted, and BSY and I/O not asserted, the selected TARGET examines the DATA bus for the INITIATOR ID and responds by asserting BSY.

After a minimum of two DESKEW DELAYS (following the detection of BSY from the TARGET), the INITIATOR deasserts SEL and may change the DATA signals.

The INITIATOR may "time out" the SELECTION phase by deasserting the ID bits on the bus. If (after a SELECTION RESPONSE TIME plus two DESKEW DELAYS) BSY has not been asserted, SEL may be deasserted. The TARGET must drive BSY within a SELECTION RESPONSE TIME of detecting SEL and its own ID.

4.4.3 INFORMATION TRANSFER PHASES

The COMMAND, DATA, STATUS and MESSAGE phases are all used to transfer data or control information through the DATA bus. The actual contents of the information is beyond the scope of this section.

The C/D, I/O and MSG signals are used to differentiate the various INFORMATION TRANSFER phases. Note that these signals are not valid without REQ asserted. See Table 4-1.

SIGNAL			PHASE NAME	DIRECTION OF INFORMATION TRANSFER
MSG	C/D	I/O		
0	0	0	DATA OUT Phase	(INIT to TARG)
0	0	1	DATA IN Phase	(INIT from TARG)
0	1	0	COMMAND Phase	(INIT to TARG)
0	1	1	STATUS Phase	(INIT from TARG)
1	0	0	Not Used	
1	0	1	Not Used	
1	1	0	MSG OUT Phase	(INIT to TARG)
1	1	1	MSG IN Phase	(INIT from TARG)

Notes:
0 = Signal Deassertion
1 = Signal Assertion
INIT = Initiator
TARG = Target

Table 4-1. Information Transfer Phase

The INFORMATION TRANSFER phases use the REQ/ACK handshake to control data transfer. Each REQ/ACK allows the transfer of one byte of data. The handshake starts with the TARGET asserting the REQ signal. The INITIATOR responds by asserting the ACK signal. The TARGET then deasserts the REQ signal and the INITIATOR responds by deasserting the ACK signal.

With I/O signal asserted, data will be input to the INITIATOR from the TARGET. The TARGET must ensure that valid data is available on the bus (at the INITIATOR port) before the assertion of REQ at the INITIATOR port. The data remains valid until the assertion of ACK by the INITIATOR. The TARGET should compensate for cable skew and the skew of its own drivers.

With the I/O signal not asserted, data will be output from the INITIATOR to the TARGET. The INITIATOR must ensure valid data on the bus (at the TARGET port) before the assertion of ACK on the bus. The INITIATOR should compensate for cable skew and the skew of its own drivers. Valid data remains on the bus until the TARGET deasserts REQ.

During each INFORMATION TRANSFER phase, the BSY line remains asserted, the SEL line remains deasserted, and the TARGET will continuously envelop the REQ/ACK handshake(s) with the C/D, I/O and MSG signals in such a manner that these control signals are valid for a BUS SETTLE DELAY before the REQ of the first handshake and remain valid until the deassertion of ACK at the end of the last handshake.

4.4.3.1 COMMAND PHASE

The COMMAND phase allows the TARGET to obtain command information from the INITIATOR.

The TARGET asserts the C/D signal and deasserts the I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

4.4.3.2 DATA PHASE

The DATA phase includes both the DATA IN phase and the DATA OUT phase.

The DATA IN phase allows the TARGET to INPUT data to the INITIATOR. The TARGET asserts the I/O signal and deasserts the C/D and MSG signals during the REQ/ACK handshake(s) of this phase.

The DATA OUT phase allows the TARGET to obtain OUTPUT data from the INITIATOR. The TARGET deasserts the C/D, I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

4.4.3.3 STATUS PHASE

The STATUS phase allows the TARGET to send status information to the INITIATOR.

The TARGET asserts C/D and I/O and it deasserts the MSG signal during the REQ/ACK handshake(s) of this phase.

4.4.3.4 MESSAGE PHASE

The MESSAGE phase includes the MESSAGE IN and MESSAGE OUT phases.

The MESSAGE IN phase allows the TARGET to INPUT a message to the INITIATOR. The TARGET asserts C/D, I/O and MSG during the REQ/ACK handshake(s) of this phase.

The MESSAGE OUT phase allows the TARGET to obtain a message from the INITIATOR. The TARGET may invoke this phase only in response to the ATTENTION condition created by the INITIATOR. In response to the ATTENTION condition, the TARGET asserts C/D and MSG and deasserts the I/O signal during the REQ/ACK handshake(s) of this phase.

4.4.4 SIGNAL RESTRICTIONS BETWEEN PHASES

When the BUS is between phases, the following restrictions apply to the bus signals:

- The BSY, SEL, REQ and ACK signals may not change.
- The C/D, I/O, MSG and DATA signals may change.
- The ATN and RST signals may change as defined under the descriptions for the ATTENTION and RESET conditions.

4.5 BUS CONDITIONS

The bus has two asynchronous conditions: the ATTENTION condition and the RESET condition. These conditions cause certain BUS DEVICE actions and can alter the bus phase sequence.

4.5.1 ATTENTION CONDITION

ATTENTION allows the INITIATOR to signal the TARGET of a waiting IDENTIFY message. The TARGET may access the message by invoking a MESSAGE OUT phase.

The INITIATOR creates the ATTENTION condition by asserting ATN at any time except during the BUS FREE phase. The TARGET responds when ready with the MESSAGE OUT phase. The INITIATOR keeps ATN asserted if more than one byte is to be transferred.

The INITIATOR can deassert the ATN signal during the RESET condition, during a BUS FREE phase, or while the REQ signal is asserted and before the ACK signal is asserted during the last REQ/ACK handshake of a MESSAGE OUT phase.

4.5.2 RESET CONDITION

The RESET condition, created by the assertion of RST, is used to immediately clear all devices from the bus and to reset these devices and their associated equipment as defined in the controller specification.

RESET can occur at any time and takes precedence over all other phases and conditions. Any device (whether active or not) can invoke the RESET condition. On RESET, all devices will immediately (within a BUS CLEAR DELAY) deassert and passively release all bus signals except RST itself. A TARGET capable of continuing an I/O operation after being interrupted by RESET will clear any I/O operation that has not been established.

The RESET condition stays on for at least one RESET HOLD TIME. During the RESET condition, no bus signal except RST can be assumed valid.

Regardless of the prior bus phase, the bus resets to a BUS FREE phase (and then starts a normal phase sequence) following a RESET condition.

PHASE SEQUENCING 4.6

Phases are used on the bus in a prescribed sequence. In all systems, the RESET condition can interrupt any phase and is always followed by the BUS FREE phase. (Any other phase can also be followed by the BUS FREE phase.)

The normal progression is from BUS FREE to SELECTION, and from SELECTION to one or more of the INFORMATION TRANSFER phases (COMMAND, DATA, STATUS or MESSAGE).

There are no restrictions on the sequencing between INFORMATION TRANSFER phases. A phase may even follow itself (e.g., a DATA phase may be followed by another DATA phase).

TIMING 4.7

A timing chart is provided in Figure 4-1. Unless otherwise indicated, the delay time measurements for each device are calculated from signal conditions existing at the device BUS PORT. Delays in the bus cable need not be considered for these measurements.

4.7.1 ABORTED SELECTION TIME: 200 microseconds (max.)

The maximum delay allowed from SELECT detection until a BSY response is generated by a TARGET (or INITIATOR) during SELECTION. This is not SELECT TIMEOUT.

4.7.2 BUS CLEAR DELAY: 650 nanoseconds (max.)

The maximum time allowed for a device to stop driving all bus signals after the release of BSY when going to BUS FREE.

4.7.3 BUS SET DELAY: 1.1 microseconds (max.)

The maximum time from detection of BUS FREE until BSY is driven.

4.7.4 BUS SETTLE DELAY: 450 nanoseconds (min.)

4.7.5 CABLE SKEW: 10 nanoseconds (max.)

The maximum difference in propogation time allowed between any two bus signals when measured between any two bus ports.

4.7.6 DESKEW DELAY: 45 nanoseconds (min.)

4.7.7 REQ RESPONSE TIMEOUT: 250 milliseconds (min.)

The delay allowed between assertion of REQ by the TARGET and time out (due to lack of ACK from the INITIATOR).

4.7.8 RESET HOLD TIME: 25 microseconds (min.)

The minimum time during which RST is asserted. No maximum.

4.7.9 SELECT TIMEOUT: 250 milliseconds (min.)

The delay allowed for a BSY response from a TARGET before time out during SELECTION.

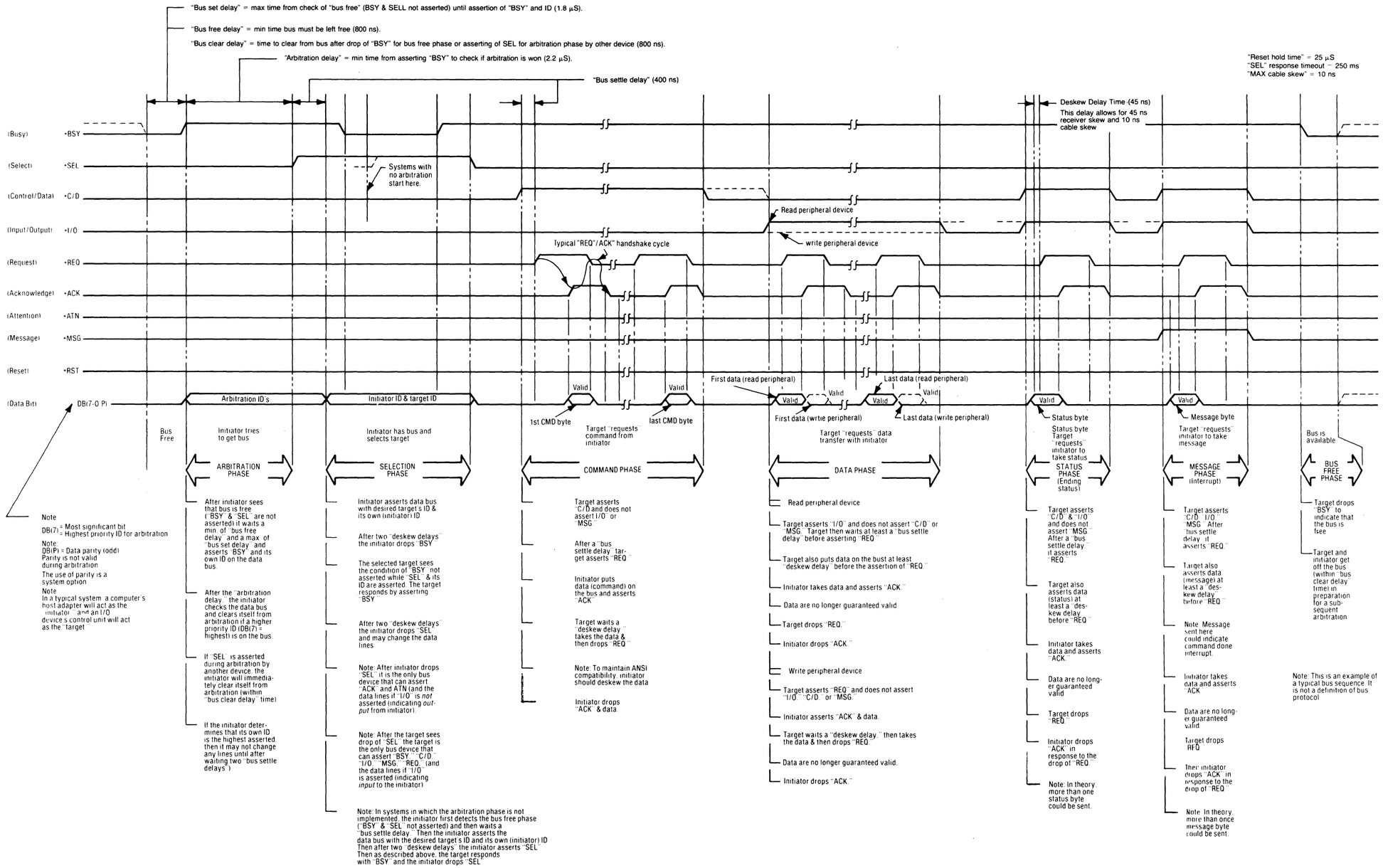


Figure 4-1.
Bus Timing Chart

MESSAGE SYSTEM 5.1

The message system allows communication between an INITIATOR and TARGET for purposes of physical path management. This section defines the messages and lists their assigned codes (in HEX).

Normally, the first message sent by the INITIATOR after the SELECTION phase is IDENTIFY (to establish the physical path). After reselection, the TARGET's first message is also IDENTIFY. Under certain conditions, an INITIATOR may send SELECTIVE RESET or BUS DEVICE RESET as the first message.

The ACB-4000 controller only supports the COMMAND COMPLETE message and does not respond to the ATN signal except during selection. Only COMMAND COMPLETE need be implemented in an ACB-4000 environment.

5.1.1 SINGLE BYTE MESSAGE

5.1.1.1 COMMAND COMPLETE (00H)

This code is sent from the TARGET at the completion of command execution (or at the end of a series of linked commands) to direct the INITIATOR to indicate COMMAND COMPLETE to the host.

This message does not imply good ending status; STATUS must be checked to determine end conditions.

GENERAL DESCRIPTION 6.1

This section of the Adaptec Controller Manual details the SCSI command set and related information.

By defining a fixed block structure using a simple, logical address scheme, the I/O interface can support device independence. In addition, by including the logical block address as a component of the command structure, physical requirements (such as SEEK) can be imbedded within the basic READ and WRITE requests.

This interface, despite its simplicity, is capable of providing the high level of performance required in multi-host/multi-task environments. Powerful functions, such as search, are included to enhance random access applications, and single-command, multi-block transfers are included to simplify sequential operations.

COMMAND AND STATUS STRUCTURE 6.2

6.2.1 COMMAND DESCRIPTOR BLOCK (CDB)

An I/O request to a device is made by passing a Command Descriptor Block (CDB) to the controller. The first byte of the CDB is the command class and operation code. The remaining bytes specify the Logical Unit Number (LUN), block starting address, control byte and the number of blocks to transfer. Commands are categorized into two classes supported by Adaptec controllers.

The SCSI Command Descriptor Block contains reserved bytes (for future SCSI definition). The ACB-4000 requires that those bytes be set to zero or the command will be rejected.

Class 0: 6-Byte commands.
Class 1: 10-Byte commands.

Figures 6-1 and 6-2 show typical command descriptor block formats.

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	Class Code			Op Code				
01	Logical Unit Number			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Number of Blocks							
05*	Reserved (0)							

*Control Byte

Figure 6-1. Class 00 Commands (6-Byte Commands)

BYTE	BIT 7	6	5	4	3	2	1	0
00	Class Code			Op Code				
01	Logical Unit Number			Command Specific Bits				
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Number of Blocks							
08	Number of Blocks							
09*	Reserved (0)							

*Control Byte

Figure 6-2. Class 01 Commands (10 Byte Extended Block Address)

6.2.2 CLASS CODE

The class code can be 0 to 7, but only 0 and 1 are used at this time.

6.2.3 OPERATION CODE

The operation code for each class allows 32 commands (00 to $1F_H$).

6.2.4 LOGICAL UNIT NUMBER

Logical unit numbers allow eight devices per controller. The ACB-4000 accomodates two devices per controller which must be devices 0 and 1.

6.2.5 COMMAND SPECIFIC BITS

Byte 01, bits 01–04 specify options which depend upon the particular command.

6.2.6 LOGICAL BLOCK ADDRESS

Class 0 commands contain 21-bit starting block addresses while class 1 supports 32-bit block addressing.

The "block" concept implies that the host and controller have "preset" the number of bytes of data to be transferred. You will note that the concept of sector is replaced by block.

6.2.7 NUMBER OF BLOCKS

A variable number of blocks may be transferred under a single command. Class 00 commands may transfer up to 256 blocks, while class 01 commands may transfer up to 64K blocks. A zero block number count defaults to the maximum value.

6.2.8 CONTROL BYTE

All bits in the control byte are reserved and must be zero.

COMMAND DESCRIPTIONS 6.3

The following section describes and details the complete command set for the ACB-4000 controller.

6.3.1 CLASS 00 COMMAND DESCRIPTIONS

The following is a series of command descriptions.

OP CODE	COMMAND	OP CODE	COMMAND
00	TEST UNIT READY	0F	TRANSLATE
01	REZERO UNIT	13	WRITE BUFFER
03	REQUEST SENSE	14	READ BUFFER
04	FORMAT UNIT	15	MODE SELECT
08	READ	1A	MODE SENSE
0A	WRITE	1B	START/STOP UNIT
0B	SEEK	1C	RECEIVE DIAGNOSTIC
		1D	SEND DIAGNOSTIC

Table 6-1. Class 00 Command Code Summary

6.3.1.1 TEST UNIT READY (00_H)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0	0
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Reserved (0)							
05*	Reserved (0)							

Figure 6-3. TEST UNIT READY Command

*Control Byte

This command returns zero status if the requested unit is powered on and ready. If not ready, a check condition will be set in the status byte. Possible errors are Drive Not Ready (04_H) and Write Fault (03_H).

6.3.1.2 REZERO UNIT (01_H)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	0	1
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Reserved (0)							
05*	Reserved (0)							

Figure 6-4. REZERO UNIT Command

*Control Byte

This command sets the selected drive to track zero and then sends completion status. Possible error returns are No Seek Complete (02_H), Drive Not Ready (04_H) and No Track Zero (06_H).

6.3.1.3 REQUEST SENSE (03_H)

See Paragraph 6.4 for details of the complete command as well as a complete discussion of returned sense data.

6.3.1.4 FORMAT UNIT (04_H)

The control unit will write from index to index all ID and data fields with a block size as specified by an immediately previous MODE SELECT (15_H) command. If no MODE SELECT (15_H) command has been executed, the previous data block size will be used. On unformatted disks or those whose format is determined bad (sense byte error code $1C_H$ returned following a READ), a MODE SELECT (15_H) command is required prior to the format command. Data fields are completely written with $6C_H$ unless otherwise specified in the format command.

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	0	0	0	0	0	1	0	0
01	Logical Unit Number			Data	Cmplt	List Format Bits		
02	Data Pattern							
03	(MSB) Interleave							
04	Interleave (LSB)							
05*	Reserved (0)							

*Control Byte

Figure 6-5. FORMAT UNIT Command

Byte 01 is used to indicate if a list of defect locations is appended and whether a unique fill character is required. Bit 04 indicates that defect data is appended to the command block and must be set if a defect list is present. The defect list must be less than 1024 bytes long. Bit 03 is defined by the SCSI specification as an indication that the defect list appended is a complete list. This bit must also be set if a defect list is present. Bit 02 indicates that bits 01 and 00 are used to further define the format and must be set if either a defect list or unique fill character is present. Bit 01 indicates that a unique fill character is contained in the next byte (byte 02). If this bit is not set, the ACB-4000 will fill all data fields with a "6C" data pattern. Bit 00 indicates the format of the appended defect list. This bit set to zero refers to a cylinder, head and byte format and must be used if defect data is present.

The ID fields will be interleaved as specified in bytes 3 and 4 of the CDB (byte 4, bit 0 LSB). The ACB-4000 controller does not require interleaving because of a high speed buffer control. An interleave number of 1 results in sequential ID fields being written on the disk. Any interleave number greater than 1 and one less than the total sectors per track result in interleaved formatting. A 0 in this field will cause the default interleave factor of 2 to be used. By using an interleave of 2 or greater, the ACB-4000 can format 33 256-byte sectors per track rather than the normal 32 sectors. (See Appendix A for details.) Note that byte 3 must always be zero and also that the value in byte 4 must not exceed the number of sectors per track minus one. An error code of 24_H (Bad Argument) will be returned if either of these rules is violated.

The interleave number is equivalent to the number of disk revolutions required to sequentially read one track. An example of an interleave number of 3 with 256-byte sectors follows:

P - 00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16
F - 00 23 12 01 24 13 02 25 14 03 26 15 04 27 16 05 28

P - 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33
F - 17 06 29 18 07 30 19 08 31 20 09 32 21 10 33 22 11

P = Physical sector count
F = Formatted sector locations (with interleave of 3)

Table 6-2 defines the use of the data and list format bits:

Table 6-2. FORMAT UNIT Defect Options

FMT DATA	CMPLT	BIT 02	BIT 00	DEFINITION
0	0	0	0	Format with no appended defect information.
1	1	1	0	Format with appended defect information. Defect locations are in cyl., head and byte displacement format.

The following is the format for the appended defect list. The list includes the physical coordinates of known media flaws in cylinder, head and bytes from index. All defects must be listed in ascending order.

BYTE	BIT 7	6	5	4	3	2	1	0
00	Reserved (0)							
01	Reserved (0)							
02	Length of							
03	Defect List in Bytes (8N)							
04	(MSB)	Cylinder Number of Defect #1						
05	Cylinder Number of Defect #1							
06	Cylinder Number of Defect #1							(LSB)
07	Head Number of Defect #1							
08	(MSB)	Bytes from Index						
09	Bytes from Index							
10	Bytes from Index							
11	Bytes from Index							(LSB)
• • •								
8N – 4 to 8N + 3	Nth Defect							

Note:
See example in Appendix A.

Figure 6-6. Defect Data Block

If data errors are noted by the controller while reading the defect list, all formatting is stopped and a Bad Argument error (24_H) is returned to the host.

If, in time, other defects appear on a drive, the contents of the entire drive should be backed up and a new format operation performed. To identify the physical locations of the troublesome blocks use the TRANSLATE command. The new defect locations must then be added and sorted into the complete list.

The defect skipping technique implemented by the ACB-4000 is at the sector level and does not require time-consuming seeks to spare track locations.

Therefore, the tracks specified by a drive manufacturer as "spare" may be utilized for data, increasing the effective capacity of the device.

6.3.1.5 READ (08_H)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	0	0
01	Logical Unit Number			(MSB)	Logical Block Address			
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Number of Blocks							
05*	Reserved (0)							

Figure 6-7. READ Command

*Control Byte

This command transfers (to the host) the specified number of blocks starting at the specified logical starting block address.

The control unit will verify a valid seek address and proceed to seek to the specified starting logical block address. When the seek is complete the controller then reads the starting address data field into the buffer, checks ECC and begins DMA data transfer.

Subsequent blocks of data are transferred into the buffer in a similar manner until the block count is decremented to zero. Cylinder switching is transparent to the user. On a data ECC error, the block is reread up to five times to establish a solid error syndrome. Only then is correction attempted. Correction is done directly into the data buffer transparent to the host.

Blocks containing uncorrectable data errors will be transferred to the host prior to an ending check status. A REQUEST sense will return an uncorrectable data error (11_H).

6.3.1.6 WRITE ($0A_H$)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	1	0
01	Logical Unit Number			(MSB)	Logical Block Address			
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Number of Blocks							
05*	Reserved (0)							

Figure 6-8. WRITE Command

*Control Byte

This command transfers (to the target device) the specified number of blocks starting at the specified logical starting block address. The controller seeks to the specified logical starting block. When the seek is complete, the controller transfers the first block into its buffer and writes its buffered data and its associated ECC into the first logical sector.

Subsequent blocks of data are transferred as available from the FIFO buffer until the block count is decremented to zero. Cylinder switching and defect skipping are transparent to the user.

The ACB-4000 also supports corresponding extended READ and WRITE commands using the class 01 CDB format.

6.3.1.7 SEEK ($0B_H$)

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	0	0	0	0	1	0	1	1
01	Logical Unit Number			(MSB)	Logical Block Address			
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Reserved (0)							
05*	Reserved (0)							

*Control Byte

Figure 6-9. SEEK Command

This command causes the selected drive to seek to the specified starting address. The ACB-4000 returns completion status immediately after the seek pulses are issued and head motion starts , allowing it to free the bus and accept further commands prior to actual seek completion. Note: Any command received for a unit with a seek in progress will immediately complete with a command completion status of busy (bit 3 set). This is done to allow the host to use the SCSI bus to do other processing while waiting for seek complete.

The drive is stepped to the addressed track position but no ID field verification is attempted.

All ACB-4000 uses an implied seek on READ, WRITE and SEARCH commands obviating the need for issuance of SEEK commands with each operation.

6.3.1.8 TRANSLATE ($0F_H$)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	0	1	1	1	1
01	Logical Unit Number			(MSB) Logical Block Address				
02	Logical Block Address							
03	Logical Block Address							(LSB)
04	Reserved (0)							
05*	Reserved (0)							

*Control Byte

Figure 6-10. TRANSLATE Command

This command performs a logical address to physical address translation and returns the physical location of the requested block address in a cylinder, head, bytes from index format. This data can be used to build a defect list for the FORMAT command.

Eight bytes are returned in the format of defect descriptors required by FORMAT.

If there is a data error in the ID field, an error status will be returned. It is then necessary to TRANSLATE the blocks before and after the targeted block to determine the location of the target block. The use of interleaved sectors and formatted (skipped) defects may complicate the determination of the error location.

BYTE	BIT 7	6	5	4	3	2	1	0
00	(MSB) Cylinder Number							
01	Cylinder Number							
02	Cylinder Number							(LSB)
03	Head Number							
04	(MSB) Bytes from Index							
05	Bytes from Index							
06	Bytes from Index							
07	Bytes from Index							(LSB)

Figure 6-11. TRANSLATE Data

6.3.1.9 WRITE DATA BUFFER (13_H)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	1	0	0	1	1
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Reserved (0)							
05*	Reserved (0)							

*Control Byte

Figure 6-12. WRITE DATA BUFFER Command

This command serves buffer RAM diagnostic purposes. The controller will fill the buffer with 1K bytes of data from the host. There is no guarantee that this data will not be overwritten by other operations initiated by other INITIATORs.

6.3.1.10 READ DATA BUFFER (14_H)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	1	0	1	0	0
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Reserved (0)							
05*	Reserved (0)							

*Control Byte

Figure 6-13. READ DATA BUFFER Command

READ DATA BUFFER will pass the host 1K of data from the buffer. It is intended for RAM diagnostic purposes. The same caveat applies to this as to write buffer. In addition, although data remains in the buffer after normal data operations, the ordering of the data found there may vary.

6.3.1.11 MODE SELECT (15_H)

This command is used in ACB controllers to specify format parameters and should always preceed the FORMAT command. When a blown format error (code 1C) is detected due to the controller being unable to read the drive information from a drive already formatted, the user should use this command to inform the controller about the drive information. Then the drive should be backed up and reformatted.

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	0	0	0	1	0	1	0	1
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Number of Bytes							
05*	Reserved (0)							

*Control Byte

Figure 6-14. MODE SELECT Command

Byte 4 of the command specifies the number of information bytes to be passed with the command. A minimum of twelve bytes ($0C_H$) must be specified. If drive parameters are being specified the count should be 22 bytes (16_H).

The parameter list is four bytes long with the first three bytes reserved (zero filled). The fourth byte contains the length in bytes of the extent descriptor list; this is always eight. (Only a single extent is supported.)

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	Reserved (0)							
01	Reserved (0)							
02	Reserved (0)							
03	Length of Extent Descriptor List = 08_H							

Figure 6-15. MODE SELECT Parameter List

BYTE	BIT 7	6	5	4	3	2	1	0
00	Density Code							
01	Reserved (0)							
02	Reserved (0)							
03	Reserved (0)							
04	Reserved (0)							
05	(MSB) Block Size							
06	Block Size							
07	Block Size							(LSB)

Figure 6-16. Extent Descriptor List

Byte 0 of the extent descriptor list specifies the data density of the drive. Current ACB products support only MFM and a value of 00 in this byte is required. Bytes 1, 2 and 3 are reserved and must be zero, specifying that the entire drive is to be formatted. Bytes 5 through 7 are used to specify the data block size. The block size must not be less than 256 or exceed the RAM buffer capacity which is 1024 characters.

The extent descriptor list and following drive parameter list are a single large data block which follows the command. The ACB-4000 must be set up with a value 256, 512 or 1024 bytes.

Any violation of the above constraints will result in Check status with an error code of 24_H, indicating an invalid argument in parameter data.

BYTE	BIT 7	6	5	4	3	2	1	0
00	List Format Code = 01							
01	MSB Cylinder Count							
02	Cylinder Count							LSB
03	Data Head Count							
04	MSB Reduced Write Current Cylinder							
05	Reduced Write Current Cylinder							LSB
06	MSB Write Precompensation Cylinder							
07	Write Precompensation Cylinder							LSB
08	Landing Zone Position							
09	Step Pulse Output Rate Code							

Figure 6-17. Drive Parameter List

The drive parameter list includes all the data necessary to specify a drive. It is optional, but if present must be complete and the items must be within the limits stated. If these parameters are not supplied the format operation will use previously supplied values if available or the default values given below.

The list format code must be 01.

The cylinder count is the number of data cylinders on the drive. Due to the in-line defect skipping formatting cylinders normally set aside as spares may be included in this total. The minimum is one. The maximum supported is 2048. The default value is 306.

The data head count is the number of usable data surfaces. The heads will be selected from 0 to head count minus 1. The minimum is 1; maximum is 16. A drive with nine or more heads will use the reduced write current line as the high order head select. The default value is 2.

The reduced write current cylinder is the cylinder number beyond which the controller will assert the reduced write current line. Minimum value is 0; maximum is 2047. The default value is cylinder 150. Note that reduced write current assumes a different meaning on drives with more than 8 heads.

The write precompensation cylinder is the cylinder beyond which the controller will compensate for inner track bit shift. The specs for this function agree with those of most disk manufacturers. Minimum value is 0; maximum is 2047.

> **NOTE:** On the ACB-4000 this field is ignored. The precomp threshold is the same as the reduced write current value. As most drives now ignore the reduced write current signal this is not a serious restriction. However, for those drives with more than eight heads, jumpers are provided on the board which allow the precompensation to be selected as always on, always off or tied to reduced write current. The normal position is tied to reduced write current. This jumper applies to both drives.
>
> For drives which do not require reduced write current or write precompensation, the user must specify the maximum cylinder address +1 in these two parameters to prevent the controller from asserting the reduced write current signal.

The landing zone position is used with the START/STOP command to indicate the direction and number of cylinders from the last (or first) data cylinder to the shipping position. The most significant bit indicates the direction with a zero meaning that the landing zone is beyond the highest track, and a one indicates the landing zone is outside track zero. The low seven bits gives the number of cylinders. The default is zero (land on inner most track).

The step pulse output rate code specifies the timing of seek steps. Three options are currently available:

00 = Non-Buffered Seek—3.0 mS rate—ST-506
01 = Buffered Seek—28 μS rate—ST-412
02 = Buffered Seek—12 μS rate

6.3.1.12 MODE SENSE ($1A_H$)

This command is used to interrogate the ACB-4000 device parameter table to determine the specific characteristics of any disk drive currently attached. The attached drive must have been formatted by an ACB-4000 for this to be a legal command.

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	0	0	0	1	1	0	1	0
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Number of Bytes Returned							
05*	Reserved (0)							

*Control Byte

Figure 6-18. MODE SENSE Command

Byte 4 of the command specifies the number of data bytes to be returned from the command. A minimum of 12 bytes ($0C_H$) must be specified. If the drive parameter list is required, the count should be 22 bytes (16_H).

The returned information will be the four byte parameter list, the extent descriptor list and the drive parameter list (if requested). These lists take the exact format of those in the MODE SELECT command. Please reference that command for exact detail.

6.3.1.13 START/STOP UNIT ($1B_H$)

Byte 04, bit 00 of this command should be set if this is a START command, otherwise it is a STOP command.

This command is designed for use on drives with a designated shipping or landing zone.

A STOP command will position the head to the landing zone position.

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	1	1	0	1	1
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Reserved (0)							St/Stp
05*	Reserved (0)							

Figure 6-19. START/STOP UNIT Command

*Control Byte

6.3.1.14 RECEIVE DIAGNOSTIC ($1C_H$)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	1	1	1	0	0
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	(MSB)	Data Length						
04	Data Length							(LSB)
05*	Reserved (0)							

Figure 6-20. RECEIVE DIAGNOSTIC Command

*Control Byte

This command sends analysis data to host after completion of a SEND DIAGNOSTIC command. Bytes 3 and 4 designate the size of the available buffer (in bytes).

RECEIVE DIAGNOSTIC is used to transfer data to the host and must immediately follow a SEND DIAGNOSTIC command which initiates the dump action. Otherwise, the command will be rejected.

The data length specified should be 104_H or more, although, if a smaller buffer is provided, only that much data will be transferred and the command will terminate normally.

The data buffer received as a result of a dump will be formatted as shown in Figure 6-21.

BYTE	BIT 7	6	5	4	3	2	1	0
00	(MSB) Data Block Length (=0104$_H$)							
01	Data Block Length							(LSB)
02	(MSB) Starting Address of Dump							
03	Starting Address of Dump							(LSB)
04	Dumped Data (xx00)							
103	Dumped Data (xxFF)							

Figure 6-21. RECEIVE DIAGNOSTIC Data

6.3.1.15 SEND DIAGNOSTIC (ID_H)

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	1	1	1	0	1
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	(MSB) Data Length							
04	Data Length							(LSB)
05*	Reserved (0)							

*Control Byte

Figure 6-22. SEND DIAGNOSTIC Command

This command sends data to the controller to specify diagnostic tests for controller and peripheral units.

Bytes 3 and 4 specify the length of the data to be sent.

The data length specified in the command must be at least 4 bytes long and should be equal to the length of the data block to be passed over to the controller. If the length specified is longer than needed, the excess is ignored and not read.

Byte 00 of the parameter list specifies the particular function being requested. The options available at this time, along with their associated codes are:

60_H — Re-initialize Drive
61_H — Dump Hardware Area (4000-40FF)
62_H — Dump RAM (8000-80FF)
63_H — Patch Hardware Area
64_H — Patch RAM
65_H — Set Read Error Handling Options

Of these options, only the patch options require a data block longer than 4 bytes.

Byte 01 specifies a subtest or qualifier needed only if 63_H or 64_H is selected in byte 00. (Because of the potential danger in patching controller programs, this byte provides a safety mechanism to prevent obsolete patches.)

BYTE	BIT 7	6	5	4	3	2	1	0
00	Diagnostic Specifier							
01	Diagnostic Option or Coded Release Level							
02	Low Byte of Patch Starting Address or Qualifier							
03	Patch Data Length (00 = 100_H) (N) or Reserved							
04	Optional Patch Data							
N+3	Optional Patch Data							

Figure 6-23. SEND DIAGNOSTIC Parameter List

Byte 02 of the data block specifies the actions to take place if option 65_H is selected. The default state is established by a controller reset. These options, once set, stay in effect until the next reset. They apply only to the LUN addressed by the command.

The set read error handling options are:

00 Selects default operation where a correctable error will be corrected without comment and all data transferred without check status. If the error is not correctable, the controller will transfer the uncorrected data and set check status with an error code of 91_H. The valid address will be that of the bad block.

01 Disable retry and error correction. All ECC errors on first read will stop data transfer with a check status and an error code of 98_H.

02 Report all corrections after unsuccessful rereads and stop. A correctable error will be corrected and the data transferred, but the operation will stop with a check status and an error of 98_H. An uncorrectable error will be handled as in 00.

Otherwise, Byte 02 specifies the starting address in RAM or the memory-mapped registers to be patched. The high byte of the address is implicit in the diagnostic specified. Therefore, a Patch RAM operation with a third byte of $A1_H$ will overwrite an area of RAM starting with $80A1_H$.

The Byte 03 gives the number of bytes to be overwritten. This can range from 1 to 256, with a zero yielding 256.

6.3.2 CLASS 01 COMMAND DESCRIPTIONS

OP CODE	COMMAND
25	READ CAPACITY
28	READ
2A	WRITE
2E	WRITE AND VERIFY
2F	VERIFY
31	SEARCH DATA EQUAL

Table 6-3. Class 01 Command Code Summary

6.3.2.1 READ CAPACITY (25_H)

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	0	0	1	0	0	1	0	1
01	Logical Unit Number			Reserved (0)				Rel Ad
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Reserved (0)							
08	Full or Partial Media Indicator							
09*	Reserved (0)							

*Control Byte

Figure 6-24. READ CAPACITY Command

If byte 8 of the CDB is 00_H, this command will return the address of the last block on the unit. It is not necessary to specify a starting block address in this command mode. If byte 8 is 01_H, this command will return the address of the block (after the specified starting address) at which a substantial delay in data transfer will be encountered (e.g., a cylinder boundary). Any value other than 00_H or 01_H in byte 08 will cause Check status with an error code of 24_H for an invalid argument.

In both cases, the format block size is defined by the last four bytes of the 8-byte data field returned 4 bytes of block address and 4 bytes of block size.

6.3.2.2 READ (28_H)

This command is an extended address command which is identical to the class 00 READ (08_H) command.

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	1	0	1	0	0	0
01	Logical Unit Number			Reserved (0)				
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Number of Blocks							
08	Number of Blocks							
09	Reserved (0)							

Figure 6-25. READ Command

6.3.2.3 WRITE

This command is an extended address command identical to the class 00 WRITE (OA_H) command.

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	1	0	1	0	1	0
01	Logical Unit Number			Reserved (0)				
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Number of Blocks							
08	Number of Blocks							
09	Reserved (0)							

Figure 6-26. WRITE Command

6.3.2.4 WRITE AND VERIFY ($2E_H$)

This command is similar to the traditional read after write function. It is an extended address command which operates like a WRITE command over the specified number of blocks and then verifies the data written on a block by block basis. The verify function transfers no data to the host and only checks the ECC to be correct.

Since no data is transferred to the host during verify, correctable data checks will be treated in the same manner as uncorrectable data checks.

BYTE	BIT							
	7	6	5	4	3	2	1	0
00	0	0	1	0	1	1	1	0
01	Logical Unit Number			Reserved (0)				
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Number of Blocks							
08	Number of Blocks							
09	Reserved (0)							

Figure 6-27.
WRITE AND VERIFY
Command

6.3.2.5 VERIFY ($2F_H$)

This command is similar to the previous WRITE AND VERIFY except that it verifies the ECC of an alreading existing set of data blocks. It is up to the host to provide data for rewriting and correcting if an ECC error is detected.

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	1	0	1	1	1	1
01	Logical Unit Number			Reserved (0)				
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Number of Blocks							
08	Number of Blocks							
09	Reserved (0)							

Figure 6-28. VERIFY Command

6.3.2.6 SEARCH DATA EQUAL (31_H)

This powerful extended address command provides for a search and compare on equal of any data on the disk. A starting block address and number of blocks to search are specified and a search argument is passed from the host which includes a byte displacement and the data to compare.

The invert bit (Byte 01, Bit 04) inverts the sense of the search comparison operation. With invert on, a SEARCH DATA EQUAL command would succeed on data not equal. The invert bit on the ACB-4000 allows SEARCH EQUAL inverted which succeeds on the first block not equal to the pattern.

This command allows the host to perform a high-speed data verify. Unlike the VERIFY command which only checks for ECC errors, the search data equal will compare a chosen data pattern against data contained in selected blocks "on the fly." This feature provides an excellent method of verifying disk integrity after format by searching not equal for a "6C" or other unique fill character.

When a search is satisfied, it will terminate with an Equal status. A REQUEST SENSE command can then be issued to determine the block address of the matching record. A REQUEST SENSE command following a successful SEARCH DATA command will:

1) Report a Sense Key of Equal if the search was satisfied by an exact match. If the search was satisfied by an inequality, a Sense Key of No Sense is reported.

2) Set the valid bit to one.

3) Report the address of the block containing the first matching record in the Information Bytes.

A REQUEST SENSE command following an unsuccessful SEARCH DATA command will:

1) Report a Sense Key of No Sense, provided no errors occurred.

2) Set the valid bit to zero.

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	0	0	1	1	0	0	0	1
01	Logical Unit Number			Invert	Reserved (0)			
02	(MSB) Logical Block Address							
03	Logical Block Address							
04	Logical Block Address							
05	Logical Block Address							(LSB)
06	Reserved (0)							
07	Number of Blocks							
08	Number of Blocks							
09	Reserved (0)							

Figure 6-29. SEARCH DATA EQUAL Command

BYTE	BIT 7	6	5	4	3	2	1	0
00	(MSB)			Record Size				
01				Record Size				
02				Record Size				
03				Record Size				(LSB)
04	(MSB)			First Record Offset				
05				First Record Offset				
06				First Record Offset				
07				First Record Offset				(LSB)
08	(MSB)			Number of Records				
09				Number of Records				
10				Number of Records				
11				Number of Records				(LSB)
12	(MSB)			Search Argument Length				
13				Search Argument Length				(LSB)
14	(MSB)			Search Field Displacement				
15				Search Field Displacement				
16				Search Field Displacement				
17				Search Field Displacement				(LSB)
18	(MSB)			Pattern Length				
19				Pattern Length				(LSB)
20				Data Pattern				
•								
•								
•								
M+19				Data Pattern				

Figure 6-30.
SEARCH DATA
EQUAL Argument

A definition of the required data in the SEARCH argument is shown in Table 6-4.

BYTES	PARAMETER
00 to 03	**Record Size (Bytes)** For the ACB-4000 this must equal the block size or zero. Zero will be taken to mean the format block size.
04 to 07	**First Record Offset (Bytes)** For the ACB-4000 this must be zero.
08 to 11	**Number of Records** For the ACB-4000 this must be less than or equal to the number of blocks specified in the command and greater than zero. The search will terminate upon a match or when the smaller of these values is encountered.
12 to 13	**Search Argument Length (Bytes)** The number of bytes in the following search argument. Must equal the pattern length + 6.
14 to 17	**Search Field Displacement** The displacement from the beginning of the record to the first byte to be compared. Must be zero for the ACB-4000 series controllers.
18 to 19	**Pattern Length (M Bytes)** The number of bytes in the following data pattern to be compared with a like size field in each record. Pattern length must equal block size on the 4000 series controllers.
20 to M+19	**Data Pattern** A variable length field of M bytes up to block size—displacement bytes. The ACB-4000 pattern must be one block long.

Table 6-4. SEARCH DATA EQUAL Argument

6.4 COMPLETION STATUS BYTE

Status is always sent at the end of a command or set of linked commands. Intermediate status is sent at the completion of a linked command. Any abnormal condition encountered during command execution causes command termination and ending status.

Figure 6-31. Completion Status Byte

	BIT							
BYTE	7	6	5	4	3	2	1	0
00	Reserved (0)				Busy	Equal	Check	Reserv

Bits 0, 5, 6 and 7: Must be zero.

Bit 1: Check condition. Sense is available. See REQUEST SENSE below.

Bit 2: Equal. Set when any SEARCH is satisfied.

Bit 3: Busy. Device is busy or reserved. Busy status will be sent whenever a target is unable to accept a command from a host. This condition occurs when a host that does not allow reconnection requests an operation from a reserved or busy device.

6.4.1 REQUEST SENSE (03_H)

This command returns unit sense information.

The sense data will be valid for the Check status condition sent to the host and will be saved by the controller until requested. Sense data will be cleared on receiving a subsequent command from the host that received the check condition. Therefore, Check status should always be followed by a SENSE command.

The number-of-blocks field (byte 04) specifies the number of bytes allocated by the host for returned sense. Values of 0 to 3 bytes will default to 4 bytes. Check status will not be sent in response to this command.

BYTE	BIT 7	6	5	4	3	2	1	0
00	0	0	0	0	0	0	1	1
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Number of Bytes							
05*	Reserved (0)							

*Control Byte

Figure 6-32. REQUEST SENSE Command

SENSE BYTES 6.5

BYTE	BIT 7	6	5	4	3	2	1	0
00	AdrVal*	Error Class			Error Code (See Tbls 10-12)			
01	Reserved (0)			(MSB)	Logical Block Address			
02	Logical Block Address							
03	Logical Block Address							(LSB)

*The address valid bit (byte 00, bit 07) indicates that the Logical Block Address bytes contain valid information.

Figure 6-33. REQUEST SENSE Data

CODE	ERROR
00	No Sense
01	No Index Signal
02	No Seek Complete
03	Write Fault
04	Drive Not Ready
06	No Track 00

Table 6-5. Class 00 Error Codes in Sense Byte (Drive Errors)

CODE	ERROR
10	ID CRC Error
11	Uncorrectable Data Error
12	ID Address Mark Not Found
13	Data Address Mark Not Found
14	Record Not Found
15	Seek Error
16	Not Assigned
17	Not Assigned
18	Data Check in No Retry Mode
19	ECC Error During Verify
1A	Interleave Error
1B	Not Assigned
1C	Unformatted or Bad Format On Drive
1D	Self Test Failed
1E	Not Assigned
1F	Not Assigned

Table 6-6. Class 01 Error Codes in Sense Byte (Target Errors)

CODE	ERROR
20	Invalid Command
21	Illegal Block Address
22	Not Assigned
23	Volume Overflow
24	Bad Argument
25	Invalid Logical Unit Number
26–2F	Not Assigned

Table 6-7. Class 02 Error Codes (System-Related Errors)

Appendix

Installation of the ACB-4000 and Introduction to SASI/SCSI A

INTRODUCTION 1.0

The SASI/ANSI SCSI bus provides a simple means for interfacing one or more controllers to a host system. However, the SCSI spec as defined by ANSI is plagued by the problem of being so precise that it is difficult to read and understand quickly. This appendix is designed for two groups of people. The first are the people who just wish to see the controller work without getting bogged down with the fine points of the spec. The second group is the user who is attempting to replace a 'SASI-like' controller (hereafter called brand-X) with a true SASI/SCSI controller (hereafter called ACB-4000). Once the initial hurdle of getting the controller/drive combination to operate properly is overcome, it is recommended that the user go back to the SASI/SCSI document and learn the subtle points.

THE BUS AND INTERFACE 2.0

The SASI/SCSI bus is a 50-pin flat cable with 18 active lines and 25 interleaved ground lines (all odd-numbered pins are ground). This is the so-called unbalanced SASI/SCSI bus. Eight of the lines are the bidirectional data lines (byte-wide), one is the data parity (not used on the ACB-4000), and nine are control/status lines. The bus is open-collector driven and terminated on both ends by a 220-330 ohm pull-up/pull-down network (220 ohm pull-up to +5, 330 ohm pull-down to ground). The bus is active-low, thus a grounded line is considered active or asserted.

The host adapter must be able to drive or receive the data on the eight data lines, drive the ACK, SEL and RST lines and receive the C/D, I/O, MSG, BSY and REQ lines.

The ATN line is not used by brand-X controllers and must not be used with an Adaptec ACB-4000 unless you have an intelligent host adapter. The attention signal is used by an intelligent host to indicate an IDENTIFY message is available. If the ATN line is asserted by a host adapter unable to use the message protocol, a different command send routine is required which will cause most driver software to 'hang.' If the ATN line is not being used, it should be terminated by the host adapter.

The REQ and ACK lines form the handshake to sync the data rates of the controller and the host. These lines can be used in the program I/O mode (PIO) where the host system polls the REQ, gets or puts the data and drives the ACK line or can be used with a DMA controller (LSI or discrete).

It is important to note that the host adapter must not drive ACK until after data has been written to the bus (for a host to controller transfer) or read from the bus (for a controller to host transfer). Driving ACK before data has been written or read will cause erroneous data transfers with the ACB-4000.

The SEL and BSY lines are used mainly for initial selection (waking up) of the controller. The SEL line says 'Get onto the bus' and the BSY is the 'I am on the bus' reply. The SEL line should remain asserted until BSY is detected.

The C/D, I/O and MSG lines are status lines from the controller that indicate data direction (I/O), command or data phase (C/D) and command complete (MSG).

The final control line is the RST or reset line. This line causes the controller to abort its current operation (if any) and get off of the bus. In addition, the ACB-4000 will reinitialize causing a reread of the disk parameters from the drive(s).

The SASI/SCSI spec calls for a minimum RST pulse width of 25 µS. However, some brand-X controllers will accept a very short reset pulse and users have relied upon this ability in designing host adapters with very short reset pulses. The Adaptec ACB-4000 can accept a 50 nS wide pulse. For new host adapter design, it is suggested that the SASI/ SCSI 25 µS spec be followed to assure upward compatibility with newer controllers.

The data parity line is not used on the Adaptec ACB-4000 controller and is not terminated at the controller end.

3.0 SETTING UP THE HARDWARE

If you are replacing a brand-X unit, the Adaptec ACB-4000 is form and footprint compatible with one exception. The SASI/SCSI connector on the Adaptec unit is designed for consistant cable layout (pin 1 always to the left as viewed from the board edge) and so is reversed compared to the brand-X units. Pin 1 can be identified by the square pad on the solder side of the board (closest to the LED). All other connectors are identical.

If this is a new system, you will need one 34 pin (PC finger to PC finger) control cable and a 20 pin (PC finger to header socket) data cable for each drive. The 20-pin connector marked J0 must go to drive 0 and J1 to drive 1.

The drives should be set up as drive 0 and 1 according to the manufacturer's instructions. If there is only one drive, leave the terminating resistor pack in place. If there are two drives, remove the terminator from the drive closest to the controller. Watch the pin-1 orientation on all cables! Do not use the 'radial' or always selected option if the drive has one.

Also, if you are using a Seagate ST506-type drive, do not enable the half step option since the controller supports only the 3 ms step rate for unbuffered drives.

The controller requires +5 and +12 volts using the same connector and pinout as the drive. The DC should be as 'clean' as possible as noise spikes can cause soft data errors on the drive system. If your system develops a large number of soft errors, you may want to try a different or isolated supply. The Adaptec ACB-4000 requires 1.3 amps on the +5 supply and 70 mA on the +12 supply.

Two trim pots located on the board are used to set the Phase-Locked Loop (PLL) of the data separator and are factory adjusted. Do not adjust them in the field!

Jumper position J5 is used to set the SASI/SCSI bus address of the controller. Jumpers A-B, C-D and E-F set the controller address on the SASI/SCSI bus from 0 to 7. An installed

jumper is a 1 and a removed jumper is a 0. Jumper E-F is most significant and jumper A-B is least significant. For a controller address of 0, all three jumpers should be removed.

The K-L, M-N and O-P jumpers are not used by the controller and should be left open.

Two DMA transfer speeds are supported on the ACB-4000. Some host adapters or DMA channels cannot support the maximum transfer rate of the controller. By setting the jumper between position G-H, the transfer rate is cut in half and runs at a rate of SYSCLOCK/4 on single sector transfers. Multisector transfers are always made at a rate of DATA CLOCK/2 and will not be affected by this jumper.

The final jumper position (near J1) sets the precomp to be used for the drive. If jumpers R-S are shorted, the precomp starts at the reduce write current point. If jumpers R-T are shorted, precomp is applied to all tracks. If jumper R-PLL is installed, no tracks are precomped. See the drive's manual to determine the precomp requirements of your drive. Please note that the precomp applies to both drives.

TALKING TO THE CONTROLLER 4.0

When power is supplied to the system, the controller will enter a power-up mode and wait for a maximum of 18 seconds for the drive to become ready. During the 18 sec power-on sequence, the controller is checking for drive 0 and drive 1 to become ready (9 sec/drive). If the host senses a command requiring access to a drive before it has become ready (and before 18 sec has elapsed) the controller will accept the command and continue to check for a ready status. Once the drive comes ready, the controller will then execute the command; if 18 secs elapse and the drive does not come ready a DRIVE NOT READY (04_H) error will result. The controller will then check for a ready status on the next command requiring access to that drive.

Once a drive comes ready, the controller will recalibrate the head to track 0 if needed. If the drive started at track 0, the controller will step the head off of track 0 to confirm that the drive can seek and that the track 0 signal was valid. With the drive's ability to seek confirmed, the controller then seeks back to track 0. The drive actuator (if it can be seen) appears to make a short 'blip.'

The controller then attempts to read from track 0, parameter information, which is written during formatting. If the drive is unformatted or had been formatted by a brand-X controller, the parameter information is not present so the controller then sets a bit in its memory called 'blown format' to warn the user that the drive is unusable. If the drive format is blown, the reset sequence is stopped and the controller is ready for a command. The drive must be formatted to allow a READ or WRITE access to disk data.

If the drive is correctly formatted, the controller will seek the drive to the last cylinder and read the largest block address present. The parameter information and largest block address are saved on the ACB-4000.

Once the last block address has been read, the controller will seek the drive back to track 0, stopping several times in 'zones' on the way back to read the defect count at that point. This defect count is also saved in the controller to allow the controller to better predict the location of a block on the disk. Since the ACB-4000 does not waste an entire track (8K) for a defect like the brand-X controllers, the position of a given block on the drive can't be predicted without knowing how many 'hidden' defective blocks there are before the desired block.

In addition to the drive seeks and reads, the Adaptec ACB-4000 does a series of self-diagnostics after power-up. The immediate selection of the disk and movement of the heads during this period, although different from the brand-X controllers, is a sign of the proper functioning of Adaptec ACB-4000.

Let's assume that the drive is new (unformatted). The first step is to format with the Adaptec ACB-4000. The MODE SELECT command should be issued to send the drive parameters to the controller (these parameters usually come from the user through a FORMAT utility program). Then a FORMAT command will complete the sequence. A MODE SELECT must preceed a FORMAT command or the command will be rejected. At this time, the drive will be formatted in an Adaptec format and the drive parameters sent in the MODE SELECT command have been saved on the disk. Since the drive parameters (including step pulse information) are stored on the disk and read into the controller at power-on time, there is no need to send this information to the controller with every reset or power-up as required by the brand-X controllers. The Adaptec ACB-4000 allows you to power down a system, install or change a formatted drive, power up and have the controller self-configure for the new drive. The host can determine the drive size (READ CAPACITY command) self-configure without any driver software modification. This device independence provides a major advantage for host systems using a true SASI/SCSI controller over the SASI-like units that send parameters at reset and with all commands.

5.0 SASI/SCSI HANDSHAKING

The SASI/SCSI bus is a simple bus to interface. However, a quick reading of the SASI/SCSI spec may leave you lost due to its extreme attention to detail. Also, some SASI-like controllers exist on the market which allow some deviation from the ANSI/SCSI protocol. We have noted that some driver routines designed for brand-X controllers simply will not work due to some short-cuts and oversights that the SASI-like devices will tolerate. The driver routines, located in this appendix, will work with a full-SASI/SCSI controller like the ACB-4000 and are downward-compatible in protocol (perhaps not actual command format) with the SASI-like units. The driver code example is written in 8080 code but can be translated to many other CPUs.

An important point to remember in designing a driver routine is that once the controller is started by the host, THE CONTROLLER CONTROLS THE SASI/SCSI BUS. The controller drives the data direction line (I/O), the phase lines (C/D and MSG) and initiates data transfers (REQ). The host driver should make no assumptions about the bus phases or

byte counts. In fact, the controller can (and will) change phases between operations. The SASI/SCSI spec allows the controller to go through intermediate phases. Thus, the phase lines (C/D and MSG) are only valid when the controller asserts REQ. Do not write your driver or allow your hardware to follow phases when REQ is not active or it may be 'fooled' by phase changes between REQs. Also, other controllers only support some 6 byte commands, thus some users have set up counters in their software to only send a 6 byte command. Since the ACB-4000 controller supports 6 and 10 byte commands, the hardware/software should not count out the command bytes but rather should send command bytes as long as the controller requests them. Trust the controller; it 'knows' how many bytes it needs.

The sequence of operations for a single command would be:

1) Select the controller onto the bus (wake it up).
2) Send it command bytes until it changes phases (do not count bytes).
3) If requested, send/receive data until phase changes (do not count bytes; controller will determine data direction).
4) Receive (REQ/ACK cycle) 1 status byte and save for evaluation.
5) Receive (REQ/ACK cycle) 1 message byte (always 00 for ACB-4000, may be ignored).
6) Check status byte. If busy bit set, resend command; if check bit set, send sense command to get error code.

Note that some brand-X controllers do not support the SASI/SCSI defined busy bit. However, these controllers do set this bit to zero so this procedure will work with the ACB-4000 controllers and is down-level compatible with the others.

THE COMMANDS 6.0

The final components needed to operate the controller are the commands. The SCSI spec defines most of the commands that are available in the ACB-4000. However, some brand-X controllers use variations of the SCSI commands that will cause command rejects by the Adaptec ACB-4000.

The major conflict with brand-X is the 'reserved' bits in the SCSI spec, which states that these reserved bits must be set to zero and the controller should test them. However, some other manufacturers have placed their own unique codes in these bits. If a system sends something other than 0 in these bits, the ACB-4000 will reject the command.

If you find that your new or existing drivers get command rejects, check for 1s in these reserved bit positions.

7.0 A SAMPLE FORMAT SEQUENCE

For your reference here is a suggested command sequence to format a blank or differently formatted drive. Note that all commands are in HEX.

Command 1. MODE SELECT
The MODE SELECT command sends drive parameters to the controller to be written onto the drive at format time. The MODE SELECT command must be sent before a FORMAT command or the FORMAT command will be rejected.

15 MODE SELECT
00 For Drive 0, 20 for Drive 1
00 Reserved
00 Reserved
16 Length of Data Block
00 Reserved

The data block to send after the command will be:

00 Reserved
00 Reserved
00 Reserved
08 Length of Descriptor List
00 Data Density Code
00 Reserved
00 Reserved
00 Reserved
00 Reserved
00 high byte of block size (256 in this example)
01 high byte of block size (256 in this example)
00 low byte of block size (256 in this example)
01 interface code (must be 01)
01 high byte of cylinder count (306 in this example)
32 low byte of cylinder count (306 in this example)
04 total number of heads (4 in this example)
01 high byte of reduced current cyl (256 in this example)
00 low byte of reduced current cyl (256 in this example)
01 high byte of precomp cyl (not used by controller)
00 low byte of precomp cyl (not used by controller)
00 landing zone position (00 = none)
01 stepping code (01 = 28 µs/step, buffered)

The available step codes are:

00 3 mS per step, unbuffered (ST-506)
01 28 µS per step, buffered (ST-412)
02 12 µS per step, buffered (most others)

Command 2. FORMAT

The FORMAT command will rewrite all ID and data fields on the drive. The listed format command will assume no defects. The user should then verify the disk with a VERIFY command to find the bad areas and reformat, this time sending the bad block list to the controller. If you have a bad block list from the disk manufacturer, it can be used in the first format pass instead of a two-pass format.

A valuable feature in the ACB-4000 controller is the ability to format the drive with a default data byte (6C hex), or a user selected byte. This example will assume that the format is for a CP/M system that requires an E5 (HEX) data field.

04 FORMAT
02 for drive 0, 22 for drive 1
E5 the desired data field
00 high byte of interleave (must be 0)
02 low byte of interleave factor
00 RESERVED

The ACB-4000 allows you to select the desired interleave factor with the FORMAT command. The interleave can range from zero to the number of blocks per track-1. The number represents the number of blocks between consecutive block numbers, thus an interleave of 1 means that the sectors are consecutive. If you send an interleave of 0, the controller will default to 2.

The use of an interleave factor of 1 allows a maximum transfer rate but will only be effective with a host adapter and system capable of very high transfer rates. On the other hand, the use of some interleave maximizes the storage capacity of your drive.

The ACB-4000 also has the ability to pack 33 sectors of 256 bytes on a track. This is automatically done if the interleave is not equal to 1. Below is a table of blocks/track with different interleaves.

SECTOR SIZE	INTERLEAVE	SECTORS/TRACK
256	1	32
256	>1	33
512	1	17
512	>1	18
1024	1	9
1024	>1	9

Table A-1. Interleaved Sectors/Track

SAMPLE DRIVER ROUTINE 8.0

Following is a sample of driver routine. The hardware of this sample driver is assumed to be a simple PIO driver of the data bus and control lines. The only driver function handled in hardware is the ACK signal. We assume that reading/writing the data bus port when REQ is active will cause an automatic ACK response to be sent to the controller.

```
        TITLE   ******                  SAMPLE SASI DRIVER ROUTINES
        CSEG
        NAME    ('DRIVER')
        .PHASE 100H                 ;assemble in CP/M TPA

;*********************************************************
;*                                                       *
;*                   HARDWARE EQUATES.                   *
;*                                                       *
;*********************************************************

BASE    EQU     0D0H                ;base port address of host adaptor
HADATA  EQU     BASE                ;SASI data bits
HACTRL  EQU     BASE+1              ;enable and SEL output bits
HASTAT  EQU     BASE+2              ;SASI status bits


;*********************************************************
;*                                                       *
;*           CONTROL REGISTER BIT EQUATES                *
;*                                                       *
;*********************************************************

SELECT  EQU     40H                 ;asserts SEL to get
                                    ;controller onto bus


;*********************************************************
;*                                                       *
;*           RETURNED STATUS BYTE BIT EQUATES            *
;*                                                       *
;*********************************************************

BSYBIT  EQU     08H                 ;LUN is busy
ERROR   EQU     02H                 ;error in last operation


;*********************************************************
;*                                                       *
;*           STATUS REGISTER BIT EQUATES                 *
;*                                                       *
;*********************************************************

REQ     EQU     80H                 ;SASI REQ line      sserted)
IO      EQU     40H                 ;SASI I/O line (  nput)
MSG     EQU     20H                 ;SASI MSG line (1=asserted)
CD      EQU     10H                 ;SASI C/D line (1=command)
BUSY    EQU     08H                 ;SASI BUSY line (1=asserted)


;*********************************************************
;*                                                       *
;*      THE DRIVER ROUTINE ASSUMES THAT THE COMMAND      *
;*      IS STORED IN LOCATION 'CMD' AND A RAM BUFFER     *
```

Sample Driver Routine

```
;*      BIG ENOUGH FOR THE DATA HAS BEEN ALLOCATED AT   *
;*      LOCATION 'BUFFER'. IF THE COMMAND COMPLETES     *
;*      WITHOUT ERROR, LOCATION 'ENDSTA' WILL BE ZERO.  *
;*                                                      *
;*      IF AN ERROR WAS DETECTED, LOCATION 'ENDSTA'     *
;*      WILL CONTAIN 02 AND THE 4 RAM LOCATIONS         *
;*      STARTING AT 'ERCODE' WILL HOLD THE ERROR CODE   *
;*      AND ADDRESS.                                    *
;*                                                      *
;********************************************************

DRIVER: PUSH    PSW             ;temp save A/PSW
        PUSH    B               ;temp save B/C
        PUSH    D               ;temp save D/E
        PUSH    H               ;temp save H/L
RETRY:  CALL    WAKEUP          ;get controller onto bus
        LXI     H,CMD           ;point H/L at command to send
        CALL    SEND            ;send command
        CALL    WAITRQ          ;wait for REQ to come active
        IN      HASTAT          ;get bus phase status
        ANI     CD              ;test for command or data
        JNZ     GETSTA          ;if command, no data so get out
        IN      HASTAT          ;get a new copy of status
        LXI     H,BUFFER
        ANI     IO              ;test the I/O direction
        JZ      DOWRT           ;if zero, do a write
        CALL    READ            ;otherwise, do a read
        JMP     GETSTA          ;and get status

DOWRT:  CALL    WRITE           ;call the data write routine
GETSTA: CALL    STATUS          ;get drive status
        JC      RETRY           ;if busy, retry the command
        JZ      RETURN          ;if no error, return


;********************************************************
;*                                                      *
;*      THERE WAS AN ERROR IN THE LAST COMMAND, GET     *
;*      THE SENSE INFORMATION.                          *
;*                                                      *
;********************************************************


        CALL    WAKEUP          ;get controller onto bus
        LXI     H,SENSE         ;point H/L at command to send
        CALL    SEND            ;send command
        CALL    WAITRQ          ;wait for REQ to come active
        LXI     H,ERCODE        ;point H/L at error code
        CALL    READ            ;get the error code
        CALL    STATUS          ;get status (will be 00)
        MVI     A,02H           ;load error code into A
        STA     ENDSTA          ;save as status

RETURN: POP     H               ;recover H/L
        POP     D               ;recover D/E
        POP     B               ;recover B/C
        POP     PSW             ;recover A/PSW
        RET                     ;and return
```

Sample Driver Routine

```
;#############################################################
;#                                                           #
;#              SUPPORT SUBROUTINES                          #
;#                                                           #
;#############################################################



;***********************************************************
;*                                                         *
;*      THE WAKEUP ROUTINE GETS THE CONTROLLER             *
;*                      ONTO THE BUS                       *
;*                                                         *
;***********************************************************

WAKEUP: PUSH    PSW             ;temp save A/PSW
TSTBSY: IN      HASTAT          ;get current SASI status
        ANI     BUSY            ;test busy line
        JNZ     TSTBSY          ;is bus is busy, wait in loop
        MVI     A,Ø1            ;controller ID=Ø1
        OUT     HADATA          ;put it onto the data bus
        MVI     A,SELECT        ;activate select bit
        OUT     HACTRL          ;assert SEL line

CKBUSY: IN      HASTAT          ;get current SASI status
        ANI     BUSY            ;test only the BUSY line
        JZ      CKBUSY          ;wait for busy from controller
        MVI     A,ØØH           ;release the SEL line....
        OUT     HACTRL          ;once BUSY is active
        POP     PSW             ;then recover A/PSW
        RET                     ;and return


;***********************************************************
;*                                                         *
;*      THE SEND ROUTINE SENDS THE COMMAND POINTED         *
;*      BY THE H/L REGISTER TO THE CONTROLLER.             *
;*                                                         *
;***********************************************************


SEND:   PUSH    PSW             ;temp save A/PSW
        PUSH    H               ;temp save H/L
SEND1:  CALL    WAITRQ          ;wait for REQ from controller
        IN      HASTAT          ;get SASI status
        ANI     CD              ;test command/data bit
        JZ      RET1            ;if data phase, get out
        IN      HASTAT          ;get status again
        ANI     IO              ;test the direction line
        JNZ     RET1            ;if command in phase, get out
        MOV     A,M             ;if command out, get next byte
        OUT     HADATA          ;put on data bus
        INX     H               ;bump pointer
        JMP     SEND1           ;and loop back
```

Sample Driver Routine

```
RET1:   POP     H               ;recover H/L
        POP     PSW             ;recover A/PSW
        RET                     ;and return

;*********************************************************
;*                                                       *
;*      THE READ ROUTINE RECEIVES THE DATA AND SAVES     *
;*      IN THE BUFFER POINTED BY THE H/L REGISTER        *
;*                                                       *
;*********************************************************


READ:   PUSH    PSW             ;temp save A/PSW
        PUSH    H               ;temp save H/L
READ1:  CALL    WAITRQ          ;wait for REQ from controller
        IN      HASTAT          ;get SASI status
        ANI     CD              ;test command/data bit
        JNZ     RET2            ;if command, we are done
        IN      HADATA          ;if still data, get a byte
        MOV     M,A             ;save it in ram
        INX     H               ;bump pointer
        JMP     READ1           ;and loop till command phase

RET2:   POP     H               ;recover H/L
        POP     PSW             ;recover A/PSW
        RET                     ;and return


;*********************************************************
;*                                                       *
;*      THE WRITE ROUTINE SENDS THE DATA IN THE BUFFER   *
;*      POINTED BY THE H/L REGISTER                      *
;*                                                       *
;*********************************************************


WRITE:  PUSH    PSW             ;temp save A/PSW
        PUSH    H               ;temp save H/L
WRITE1: CALL    WAITRQ          ;wait for REQ from controller
        IN      HASTAT          ;get SASI status
        ANI     CD              ;test command/data bit
        JNZ     RET3            ;if command, we are done
        MOV     A,M             ;if still data, get buffer byte
        OUT     HADATA          ;send to controller
        INX     H               ;bump pointer
        JMP     WRITE1          ;and loop till command phase

RET3:   POP     H               ;recover H/L
        POP     PSW             ;recover A/PSW
        RET                     ;and return


;*********************************************************
;*                                                       *
```

Sample Driver Routine

```
;*      THE STATUS ROUTINE GETS THE STATUS AND MESSAGE  *
;*      BYTES FROM THE CONTROLLER. THE ROUTINE RETURN   *
;*      WITH THE ZERO BIT SET IF THERE WAS NO ERROR AND *
;*      THE CARRY BIT SET IF THE CONTROLLER WAS BUSY    *
;*                                                      *
;********************************************************

STATUS: CALL    WAITRQ          ;wait for request
        IN      HADATA          ;get the status byte
        STA     ENDSTA          ;save in ram
        CALL    WAITRQ          ;wait for request
        IN      HADATA          ;get (and ignore message)
        LDA     ENDSTA          ;get end status
        ANI     BSYBIT          ;test the busy bit
        JZ      NOTBSY          ;if not busy, jump around
        STC                     ;if busy, set carry
        JMP     RET4            ;and return
NOTBSY: LDA     ENDSTA          ;if not busy, get status again
        ANA     A               ;test value
RET4:   RET                     ;and return

;********************************************************
;*                                                      *
;*      THE WAITRQ ROUTINE WAITS FOR THE CONTROLLER     *
;*      TO ASSERT THE REQ LINE OF THE SASI BUS.         *
;*                                                      *
;********************************************************

WAITRQ: PUSH    PSW             ;temp save A/PSW
WAITLP: IN      HASTAT          ;get current SASI status
        ANI     REQ             ;look at the REQ line
        JZ      WAITLP          ;loop till request active
        POP     PSW             ;recover A/PSW
        RET                     ;and return

        PAGE
;********************************************************
;*                                                      *
;*              BUFFERS AND CONSTANTS                   *
;*                                                      *
;********************************************************

SENSE:  DB      03,00,00        ;sense command for errors
        00,00,00

CMD:    DB      00,00,00,00,00  ;10 byte command area
        00,00,00,00,00

ENDSTA: DB      00              ;ending status

ERCODE: DB      00,00,00,00     ;error code

BUFFER: DS      256             ;256 byte data buffer

        END
```

Sample Driver Routine

Optional Command Recognition in the ACB-4000 B

USING THE EXPANDED COMMAND SET 1.0

1.1 DEFINITION

All commands noted in Section 6 of this manual are fully supported by the ACB-4000 controller. These are a direct implementation of the ANSI SCSI command set and will cause a command reject if any of the reserved areas are violated.

In order to use the ACB-4000 in existing systems which are non-compliant with the SCSI specification, a series of optional commands are supported. In most cases, these commands are simply ignored since their functions are already available in the standard command set.

This optional command set does not imply that a different disk formatting scheme is possible. In all cases, a standard SCSI Mode Select and Format program must be written and defect skipping is always done on the block (sector) level.

1.2 USE OF OPTIONAL COMMAND SET

In order to implement the expanded alternate command set on the ACB-4000, a jumper plug must be installed at position I-J on the jumper pad of the ACB-4000 board. This jumper is continually sampled during operation, so temporary insertion is possible for periodic use of optional commands. Under normal Adaptec SCSI use, this jumper should not be installed.

COMMAND	ACB-4000	EXPANDED OPTION	NOTES
00 TEST UNIT READY	Yes	Yes	
01 REZERO UNIT	Yes	Yes	
03 REQUEST SENSE	Yes	Yes	
04 FORMAT UNIT	Yes	Yes	(1)
05 CHECK TRACK FORMAT	No	Yes	(2)
08 READ	Yes	Yes	(3)
0A WRITE	Yes	Yes	(3)
0B SEEK	Yes	Yes	
0C INITIALIZE DRIVE	No	Yes	(4)
0D READ ECC BURST LEN.	No	Yes	(5)
0E TRANSLATE	Yes	No	
0F WRITE BUFFER	No	Yes	(6)
10 READ BUFFER	No	Yes	(6)
13 WRITE BUFFER	Yes	Yes	
14 READ BUFFER	Yes	Yes	
15 MODE SELECT	Yes	Yes	
1A MODE SENSE	Yes	Yes	
1B START/STOP UNIT	Yes	Yes	
1C RECEIVE DIAGNOSTIC	Yes	Yes	
1D SEND DIAGNOSTIC	Yes	Yes	
25 READ CAPACITY	Yes	Yes	
28 READ	Yes	Yes	
2A WRITE	Yes	Yes	
2E WRITE & VERIFY	Yes	Yes	
2F VERIFY	Yes	Yes	
31 SEARCH DATA EQUAL	Yes	Yes	
E0 RAM DIAGNOSTIC	No	Yes	(7)
E3 DRIVE DIAGNOSTIC	No	Yes	(7)
E4 CONTROLLER DIAG.	No	Yes	(7)

Table B-1. Command Sets Available

Notes:

1) FORMAT UNIT works according to Adaptec specifications only.

2) CHECK TRACK FORMAT always returns good status.

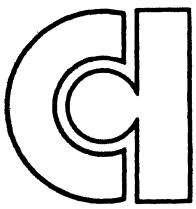
3) The reserved and vendor unique bits in the control byte are ignored when the option jumper is in place. Normal ACB-4000 use causes command rejection if these bits are set. Variable step rates and ECC control are always set by MODE SELECT and SEND DIAGNOSTIC commands, respectively.

4) INITIALIZE is accepted, but ignored. MODE SELECT overrules. Good status is returned.

5) READ ECC BURST LENGTH always returns a value of 8.

6) These vendor unique buffer commands transfer one "block size" of data.

7) Adaptec diagnostics are executed at power-on. Requests for these diagnostics are ignored and good status is always returned.



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ACB-4010 SCSI HARD DISK CONTROLLER

WITH HARD SECTOR AND REMOVABLE MEDIA SUPPORT

USER APPLICATION DOCUMENT

The ACB-4010 is a new addition to Adaptec's ACB-4000 family. The ACB-4010 controller supports all the standard features of the ACB-4000 controller, and in addition supports Hard Sector drives and Removable Media drives. The following is provided for your information.

580 cottonwood drive • milpitas, ca 95035 • telephone (408) 946-8600

ACB-4010 SCSI HARD DISK CONTROLLER

WITH HARD SECTOR AND REMOVABLE MEDIA SUPPORT

USER APPLICATION DOCUMENT

1.0 INTRODUCTION

The ACB-4010 hard disk controller board is intended for use in controlling 5 1/4" winchester disk drives. The controller board interfaces to the drive using a ST-506/412 interface, and to the host through the SCSI (Small Computer System Interface) bus.

The ACB-4010 is part of the Adaptec ACB-4000 series winchester disk controller product line, and can control two ST-506/412 drives. The ACB-4010 controller supports all the standard features of the ACB-4000 controller, and in addition supports Hard Sector drives and Removable Media Drives.

The ACB-4010 controller interfaces to the host through the industry standard SCSI (Small Computer System Interface) bus, and is fully software compatible with the ACB-4000 controller. A full description of the command set and the hardware interface is given in the ACB-4000 OEM manual.

2.0 SOFTWARE INTERFACE

The only command in the standard ACB-4000 SCSI command set that is affected by these enhancements is the Mode Select (15H) Command. This command has to be sent to the controller before attempting to format the drive. The data field for this command contains the information about the physical characteristics of the drive. This information is recorded on the drive at format time.

The Command data block consists of six (6) bytes and is shown below.

Byte	7	6	5	4	3	2	1	0
00	0	0	0	1	0	1	0	1
01	Logical Unit Number			Reserved (0)				
02	Reserved (0)							
03	Reserved (0)							
04	Number of Bytes (18)							
05	Reserved (0)							

The data block associated with this command is 24 (18H) bytes long, and the breakdown is shown below.

Byte	7	6	5	4	3	2	1	0
00	Reserved (0)							
01	Reserved (0)							
02	Reserved (0)							
03	Length of Extent List (08)							
04	Density Code (00)							
05	Reserved (0)							
06	Reserved (0)							
07	Reserved (0)							
08	Reserved (0)							
09	MSB Block Size							
0A	Block Size							
0B	Block Size							LSB
0C	List Format Code (02)							
0D	MSB Cylinder Count							
0E	Cylinder Count							
0F	Head Count							
10	MSB Reduced Write Current Cylinder							
11	Reduced Write Current Cylinder							LSB
12	MSB Write Precompensation Cylinder							
13	Write Precompensation Cylinder							LSB
14	Landing Zone							
15	Step Pulse Rate							
16	0	0	0	0	F/R	H/S	0	0
17	Sectors per Track							

Notes:

1) The Block size specified in bytes 09, 0A and 0B must be the same as the hard sector size.
2) In byte 16, bit 2 = 0, soft sector drive
1, hard sector drive
bit 3 = 0, fixed media
1, removable media
3) The number of sectors per track specified in byte 17, must be the same as specified by the hard sector drive manufacturer.

Once the disk is formatted, the hard sector disk operation will be transparent to the user. The hard sector drive may be used as either drive 0 or drive 1. Once the drive has been formatted, the controller will read the device characteristics from the disk, to differentiate between hard and soft sector drives.

3.0 HARDWARE INTERFACE

The differences between hard sector drives and soft sector drives are transparent to the host system. There are three signals associated with removable media drives. These are the 'Cartridge Changed', 'Change Cartridge' and 'Write Protect' signals.

The first signal informs the disk controller that the removable cartridge was changed. The second signal allows the disk controller to stop the disk drive, hence allowing the user to change the cartridge. The third signal informs the controller that the cartridge is write-protected.

The ACB-4010 hardware supports these three signals in the following manner:

3.1 Cartridge Changed

The ACB-4010 monitors the drive READY line constantly. When the line changes state from READY to NOT-READY, the controller will report an error '28', which means that the cartridge was changed.

The monitoring of the drive READY status is done every five seconds. Therefore, the user may notice the disk select LED light flashing once every five seconds.

3.2 Write Protect

When the write protect tab of the cartridge is set, the disk drive will prohibit any write operations. When the controller attempts to write, the disk drive will set the FAULT signal.

The ACB-4010 will monitor the 'FAULT' signal during a write operation. When the 'FAULT' signal is set, the write operation is aborted and a '03' error is reported.

3.3 Change Cartridge

The change cartridge signal only shuts off the drive. All removable media drives have a manual stop switch. The user can press this switch to remove the cartridge. Therefore, the change cartridge signal does not really eliminate operator intervention. Hence the ACB-4010 does not support this function.

4.0 SUMMARY

In addition to being compatible with the ACB-4000 controller, the hard sector support on the ACB-4010 is compatible to that on the ACB-5500, which is Adaptec's full function SCSI to four (4) ST-506/412 hard drive controller. In other words, media formatted on these two controllers is fully interchangeable.

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