MICROVERTER
SERIES

USER GUIDE
10353X07

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MICROVERTER SERIES

USER GUIDE NUMBER: 10353X07

April 1985

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CHAPTER 1

How To Use This Manual

Congratulations on your purchase of a MICROVERTER SERIES product from ABLE Computer. We are sure that it will provide you with years of satisfactory service. We have prepared this manual to help you maximize the effectiveness of this product in your system.

This manual is provided to assist you with the installation, use and care of your MICROVERTER product. Repair information is not provided; if repair is ever needed, the work should be performed at the ABLE factory.

This manual is organized into the following chapters:

* Chapter 2 provides a general description, a functional description and a list of the primary features of MICROVERTER products. It also includes electrical, physical, and environmental specifications and a description of the use of the device.

* Chapter 3 contains the installation procedure for MICROVERTER 73.

* Chapter 4 contains the installation procedure for MICROVERTER PLUS.

* Chapter 5 contains the installation procedure for MICROVERTER BD.

* Chapter 6 contains programming information, which includes information on the I/O map registers, the clock status register, and the software Map Enable.

* Chapter 7 contains information on servicing and support.

* Appendix A contains directions for modifying a backplane for 22-bit Q-Bus addressing.

* Appendix B contains patching information to allow RSTS/E V7.0 and V7.1 to operate with 22-bit parity memory.

* Appendix C contains directions for addressing UNIBUS memory for use with MICROVERTER.

* Appendix D contains installation troubleshooting information.

The following publications are delivered with MICROVERTER 73:

* DEC LSI-11/73 User Guide

* User guide for 1-Megabyte Q-Bus Memory

To understand the contents of this manual, you should be familiar with the PDP-11 UNIBUS

and LSI-11 Q-Bus architectures. For information on these architectures, refer to the following DEC documents:

* Microcomputers and Memories Handbook
* PDP-11 Bus Handbook
* PDP-11 Terminals and Communications Handbook

These manuals are available from DEC either by placing an order by telephone, or by mail. The following information has been supplied by DEC for your convenience:

BY TELEPHONE:

FROM	CALL
New Hampshire, Alaska or Hawaii	(603) 884-6660
Continental U.S.A. or Puerto Rico	(800) 258-1710
Canada (Ottawa-Hull)	(613) 234-7726
Canada (British Columbia)	(800) 267-6146
Canada (All other)	(800) 267-6146

BY DIRECT MAIL:

FROM U.S.A OR PUERTO RICO:

DIGITAL EQUIPMENT CORPORATION

Attn: Accessories and Supplies Center
P.O. Box CS2008
Nashua, NH 03061

FROM CANADA:

DIGITAL EQUIPMENT OF CANADA, LTD.

940 Belfast Road
Ottawa, Ontario K1G 4C2
Attn: ASG Business Manager

FROM ANY OTHER AREA:

DIGITAL EQUIPMENT CORPORATION

Accessories and Supplies Center
ASG Business Manager
c/o Digital's local subsidiary or
approved distributor

CHAPTER 2

THE MICROVERTER SERIES

2.1 GENERAL DESCRIPTION

There are three products in the ABLE MICROVERTER SERIES:

* MICROVERTER 73, a complete product for upgrading a PDP-11/34 (or similar system) to LSI-11/73 performance. MICROVERTER 73 includes an LSI-11/73 processor and Q-Bus memory, has its own backplane, and is installable in a PDP-11/34 system chassis.

* MICROVERTER PLUS, similar in function to MICROVERTER 73 but supplied without an LSI-11 processor and Q-Bus memory. These are supplied by the user. MICROVERTER PLUS is compatible with LSI-11/23, -11/23+, and -11/73 processors.

* MICROVERTER BD, a single-board product which allows UNIBUS peripheral device controllers to be coupled to the Q-Bus of an LSI-11 system. MICROVERTER BD is installable in an

LSI-11 system backplane, and is compatible with the LSI-11/23, -11/23+, and -11/73 processors.

2.1.1 MICROVERTER 73

MICROVERTER 73 is a Q-Bus to UNIBUS converter which upgrades a PDP-11/34 computer system to LSI-11/73 performance. The PDP-11 processor and UNIBUS memory are replaced with an LSI-11/73 processor and 1 megabyte of Q-Bus memory. MICROVERTER 73 is shown in Figure 2-1.

MICROVERTER 73 consists of the following:

* ABLE MICROVERTER board
* ABLE power regulator/console interface board
* DEC 1-megabyte Q-Bus memory board
* DEC LSI-11/73 processor board (modified)
* ABLE hybrid (Q-Bus and UNIBUS) backplane
* UNIBUS cable
* Optional front panel interface cable (for use with KY11-LA front panel).

The MICROVERTER board is a quad-width board (shown in the photograph of Figure 2-3) which performs the following principal functions:

* Serves as a Q-Bus to UNIBUS converter.
* Increases the addressing capability of

UNIBUS DMA controllers from 256K bytes up to 4 megabytes on the Q-Bus.

* Provides a KW11-L compatible line time clock.

The MICROVERTER backplane is a 9-slot backplane with four slots (1 through 4) configured as Q-Bus slots and five slots (5 through 9) configured as UNIBUS slots. The MICROVERTER board must be installed in slot 4, sockets A through D, of this backplane.

The power regulator/console interface is a dual-width board which provides PDP-11/34 front panel bootstrap and control functions, receives the line time clock signal, and receives +15 volts from the UNIBUS and regulates it to +12 volts for the Q-Bus. The power regulator/console interface board must be installed in slot 4, sockets E and F, of the special backplane. This board is shown in Figure 2-4.

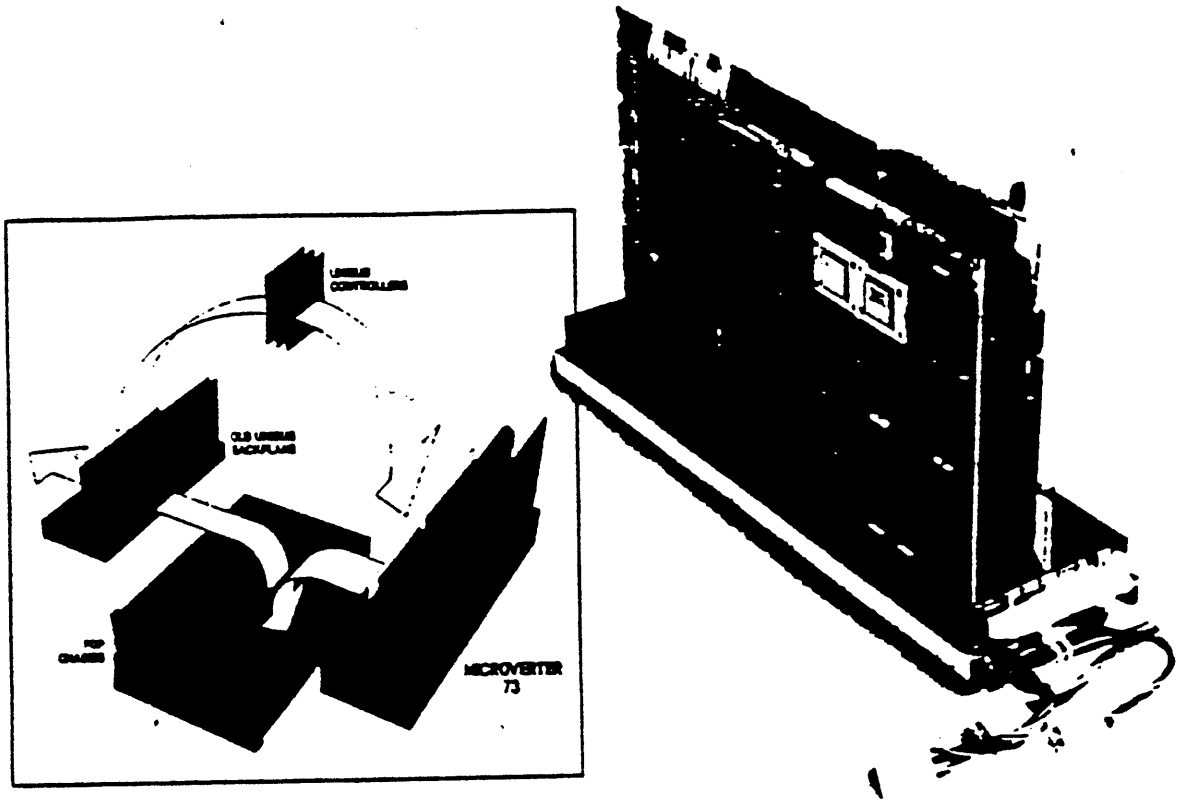

Figure 2-1: MICROVERTER 73

2.1.2 MICROVERTER PLUS

MICROVERTER PLUS consists of MICROVERTER 73 without the LSI-11/73 processor and the Q-Bus memory. Like MICROVERTER 73, MICROVERTER PLUS is installable in a PDP-11/34 computer system. However, with MICROVERTER PLUS, the user supplies the LSI-11 processor and Q-Bus memory. MICROVERTER PLUS is compatible with the LSI-11/23, LSI-11/23+, and LSI-11/73 processors. The LSI-11/23+ processor board requires a simple modification for use with MICROVERTER PLUS. The LSI-11/73 processor requires modification using a cable supplied with the product by ABLE Computer.

MICROVERTER PLUS is shown in Figure 2-2. The MICROVERTER board is shown in Figure 2-3.

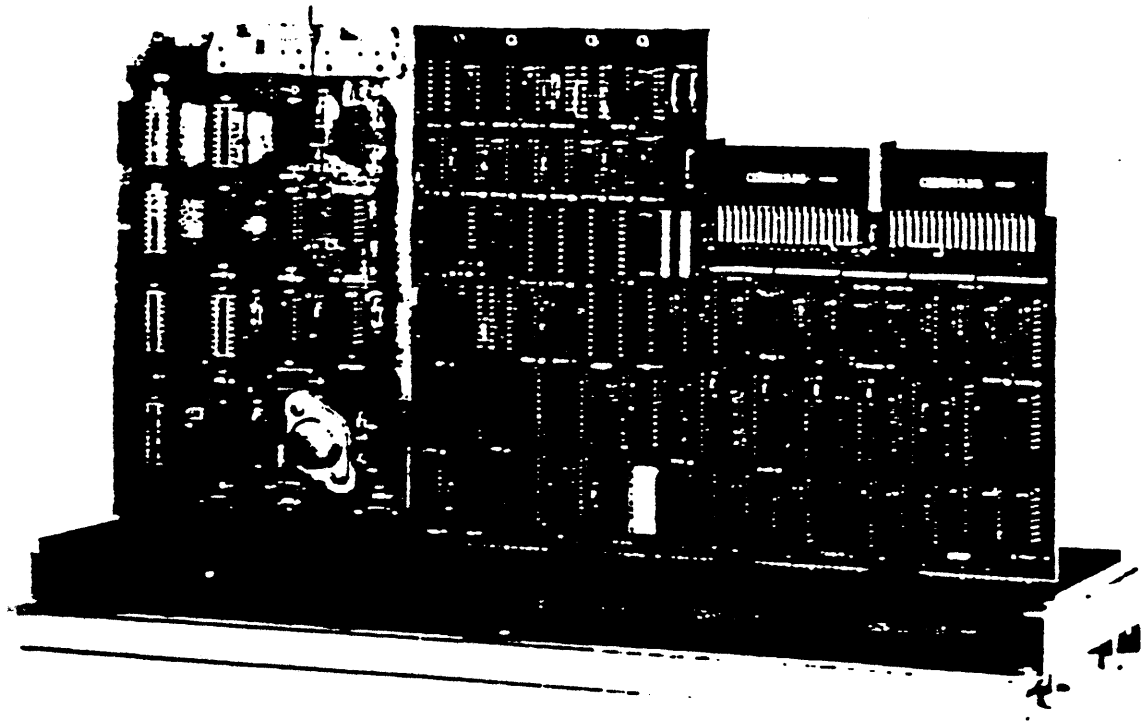

Figure 2-2: MICROVERTER PLUS

2.1.3 MICROVERTER BD

MICROVERTER BD consists of the MICROVERTER board only, and is installable in a Q-Bus backplane. This allows UNIBUS peripheral devices to be coupled to the Q-Bus and use Q-Bus memory.

MICROVERTER BD is compatible with the LSI-11/23, LSI-11/23+, and LSI-11/73 processors. The LSI-11/23+ processor requires a simple modification for use with MICROVERTER BD, and the LSI-11/73 processor requires modification using a cable supplied with the product by ABLE Computer.

With MICROVERTER, the LSI-11 processor, Q-Bus memories, and Q-Bus interrupt devices reside on the Q-Bus. 18-bit UNIBUS DMA device controllers and UNIBUS interrupt devices reside on the UNIBUS. The 18-bit addresses of NPR devices are mapped through the MICROVERTER onto the 22-bit Q-Bus.

MICROVERTER is installable in a quad slot of an LSI-11 backplane and interfaces to the Q-Bus via the A and B connectors on the board. Two UNIBUS connectors on the MICROVERTER provide connection to a UNIBUS cable (supplied with MICROVERTER 73 and MICROVERTER PLUS). MICROVERTER provides one end of UNIBUS termination.

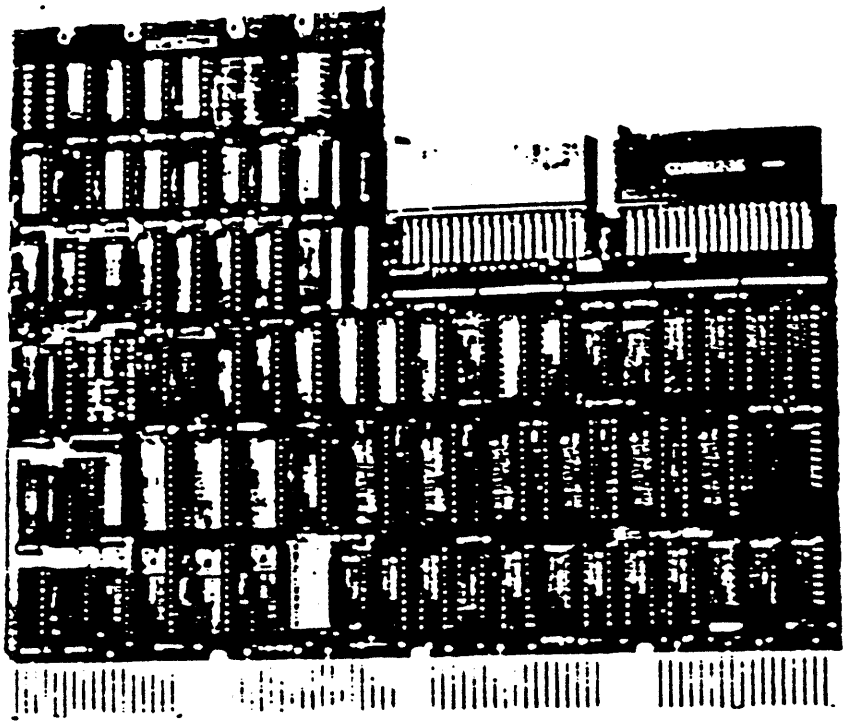

Figure 2-3: MICROVERTER Board

2.2 FEATURES

MICROVERTER SERIES products provide the following significant features:

* LSI-11/23, LSI-11/23+, and LSI-11/73 systems are supplied with the I/O mapping capability of PDP-11/44 or PAX-enhanced PDP-11/24 computers with up to 4 megabytes of main memory fully available for optimization of CPU, Q-Bus and/or UNIBUS operations.

* A line time clock (LTC) function to maintain software compatibility with existing operating systems.

* I/O map (IOM) functions providing software-compatible 4-megabyte addressing for 18-bit UNIBUS DMA devices.

* Supports the addition of up to 19 UNIBUS loads to any existing LSI-11/23 system.

* Front-end UNIBUS termination.

* Special memory implementations, such as UNIBUS bus window and UNIBUS dual port memory, are allowed.

* Software compatible with current versions of RSTS/E and RSX-11M (with no Q-Bus DMA devices present).

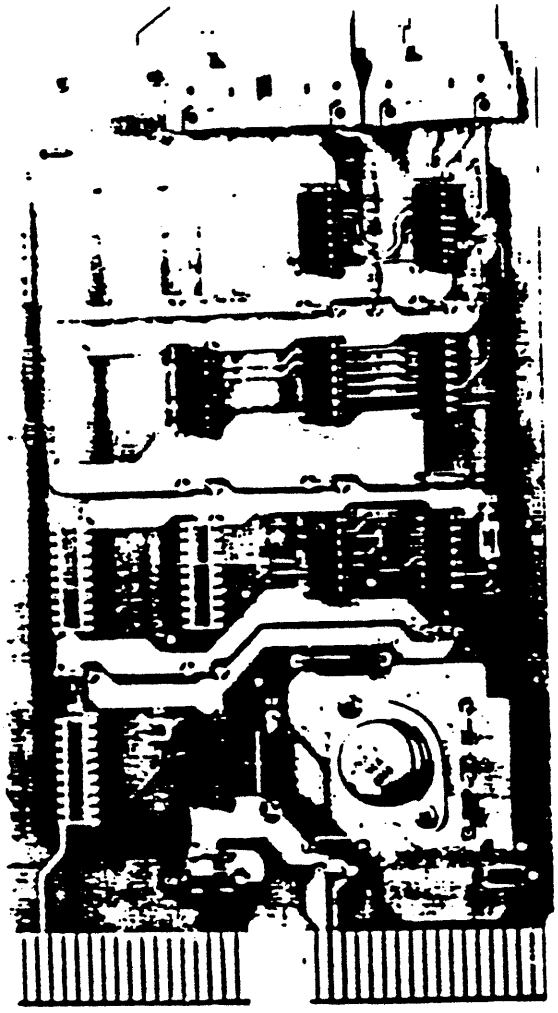

Figure 2-4: Power Regulator/Console Interface Board

2.3 SPECIFICATIONS

2.3.1 Electrical Specifications

MICROVERTER 73

Q-Bus Loading

MICROVERTER	1 DC Load
LSI-11/73	1 DC Load
1 MB memory	1 DC Load
Drive Capability	19 UNIBUS loads

Power Requirement

MICROVERTER	5.1 amps @ +5V
1 MB memory	2 amps @ +5V
LSI-11/73	4.5 amps @ +5V
Power regulator/ console interface	4 amps @ +12V (power supplied to Q-Bus)

2.3.2 General Specifications

Priority Level	LTC has fixed interrupt level of 6.
Vector Setting	LTC has fixed vector setting of 100 (octal).

2.3.3 Physical Specifications

MICROVERTER board	Std. quad-width board, measuring 10.45" x 8.40" (26.54 x 21.33 cm)
Power regulator/ console interface	Std. dual-width board, measuring 5.2" x 8.4" (13.2 x 21.3 cm)
Backplane	9-slot hex-width back-plane: 4 Q-Bus slots 5 UNIBUS slots
LSI-11/73	Std. dual-width board, measuring 5.2" x 8.4" (13.2 x 21.3 cm)
1 MB memory	Std. dual-width board, measuring 5.2" x 8.4" (13.2 x 21.3 cm)

2.3.4 Environmental Specifications

Operating Temperature	5 C to 40 C (41 F to 104 F).

Derate max. temperature by one degree Celsius for each 1,000 feet above 8,000.

Storage Temperature	-40 C to 65 C (-40 F to 149 F)
Rel. Humidity	10 to 90% noncondensing
Altitude	To 15,000 feet

2.4 FUNCTIONAL DESCRIPTION

MICROVERTER converts accesses on the Q-Bus into UNIBUS accesses. Q-Bus lines BDAL18 through BDAL21 and BBS7 are monitored for addresses in the range 3840K to 4096K bytes. Master sync (MSYNC) is asserted onto the UNIBUS only for accesses in that range.

Interrupt cycles on the UNIBUS are converted into interrupt cycles on the Q-Bus at the same level. For example, BR4 is converted to BIRQ4. MICROVERTER adheres to the position-independent priority rules of the Q bus. There are four interrupt request levels implemented on the Q-Bus. For position independent operation, each device must monitor bus interrupt requests so that when an interrupt acknowledge is received the device checks for interrupt levels higher than itself. If a higher level interrupt request is received, the device does not accept the interrupt acknowledge, but passes it on to the next device.

DMA cycles on the UNIBUS are converted to DMA cycles on the Q-Bus. This includes mapping from 18-bit UNIBUS addresses to 22-bit Q-Bus addresses. BSYNC is asserted on the Q-Bus only for UNIBUS addresses in the range 0 to 256K bytes. When memory must be placed on the UNIBUS, a window within this range can be excluded in 8K-byte increments between 0 and 256K bytes via upper and lower limit jumpers on the MICROVERTER board. When a DMA cycle addresses I/O address space 124K to 128K words, the I/O map function is disabled and the UNIBUS address is asserted onto the Q-Bus, with BBS7 also asserted.

Mapping of UNIBUS DMA devices is enabled by

setting bit 5 of Status Register 3 in the Memory Management Unit of the LSI-11/23, LSI-11/23+, or LSI-11/73 processor.

A programmable line time clock (LTC) is provided on the MICROVERTER board. When interrupts are enabled in its CSR, an interrupt to 100 (octal) is generated at BR6 for every clock tick. The clock signal is received from the BEVNT line of the Q-Bus. This line is generally sourced by the power supply, but may also be generated by a bootstrap board. The frequency is generally 50 or 60 Hz. The LTC can be disabled by opening a switch on the MICROVERTER board. If the LTC is used, the BEVNT interrupt of the LSI-11/23 processor must be disabled. If an LSI-11/23+ or an LSI-11/73 processor is used, the LTC must be disabled.

The power regulator/console interface has a jumper which determines whether the 60 Hz timing signal for LTC operation is to be supplied by the UNIBUS or by the bootstrap board.

2.5 HOW TO USE MICROVERTER

MICROVERTER SERIES products allow the wide range of PDP-11 UNIBUS peripherals to address up to four megabytes of Q-Bus memory. In the MICROVERTER 73 and MICROVERTER PLUS configurations, the MICROVERTER board must be installed in slot 4 (connectors A, B, C, and D) of the hybrid MICROVERTER backplane. In the MICROVERTER BD configuration (MICROVERTER board only), the MICROVERTER board can be installed in any quad slot of an LSI-11/23, LSI-11/23+, or LSI-11/73 system backplane. LSI-11

interfaces can be located either ahead of or behind the MICROVERTER. Devices located behind MICROVERTER have a lower priority than UNIBUS devices of the same level attached to the MICROVERTER. A typical MICROVERTER system block diagram is shown in Figure 2-5.

UNIBUS peripheral controller boards are installed in a UNIBUS backplane, which must be supplied with the appropriate power. With MICROVERTER 73 and MICROVERTER PLUS, five UNIBUS slots are provided in the hybrid backplane, and the MICROVERTER board is connected via a UNIBUS cable to the first UNIBUS slot of the backplane. With MICROVERTER BD, the UNIBUS backplane is connected to the MICROVERTER board with a standard UNIBUS extender cable connected between the first UNIBUS connectors in the UNIBUS backplane and the connectors at the top of the MICROVERTER board. In all MICROVERTER configurations, a UNIBUS terminator must be installed in connectors A and B of the last slot of the last UNIBUS backplane.

MICROVERTER provides the LSI-11 system with a second bus structure, UNIBUS. The LSI-11 processor controls the arbitration of both buses.

All 18-bit DMA devices must be installed on the UNIBUS. This permits 18-bit DMA addresses to be mapped through the MICROVERTER to form 22-bit addresses. MICROVERTER's "window" feature allows memory to be placed on the UNIBUS. This feature is used when an area of UNIBUS is used for special memory, such as multi-port memory or a bus window.

NOTE

Due to software limitations, ABLE does not recommend installation of Q-Bus 22-bit DMA devices with MICROVERTER, which would require the application of customer-supplied patches to the operating system.

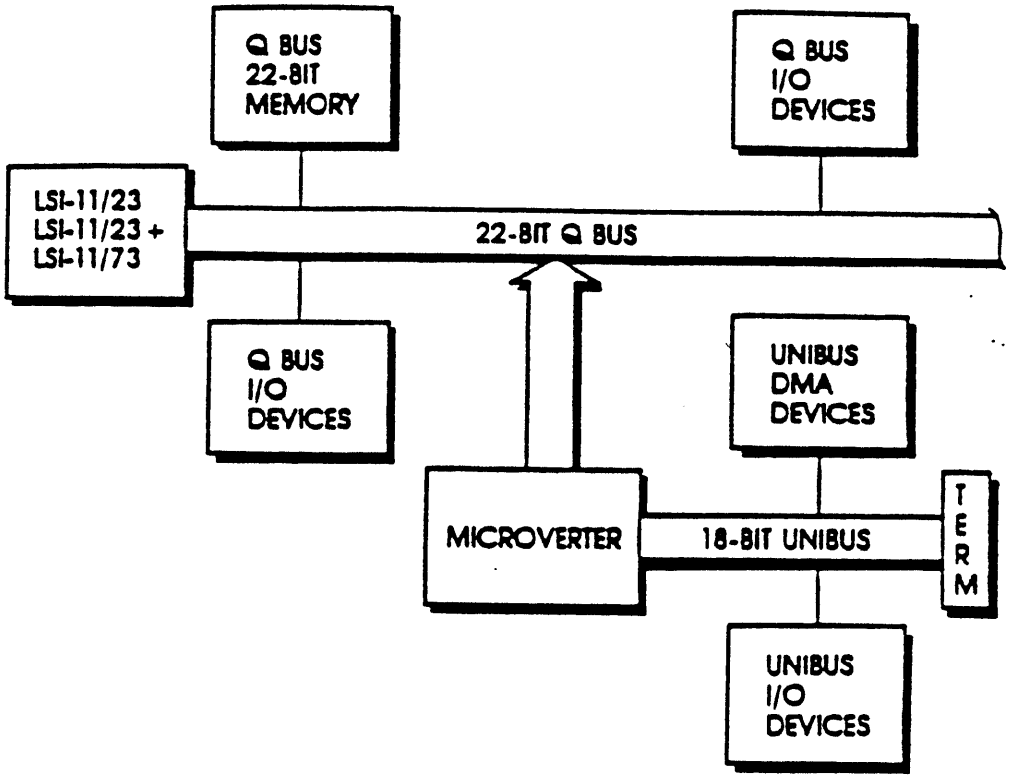

Figure 2-5: System Block Diagram

CHAPTER 3

MICROVERTER 73 INSTALLATION

3.1 GENERAL

This chapter contains procedures for installing the ABLE MICROVERTER 73 in a PDP-11/34 computer system. MICROVERTER 73 is compatible with a number of other PDP-11 systems; however, the detailed procedures given here apply to the PDP-11/34 (and /34A). If you are installing MICROVERTER 73 in any other PDP-11 system, some details may be different. In such cases, change the procedure as required to suit the particular system.

MICROVERTER 73 consists of the following components (the letter following each component indicates its label in Figure 3-1):

* ABLE MICROVERTER board (A)

* ABLE power regulator/console interface board (B)

* 1-Megabyte Q-Bus memory board (C)
* DEC LSI-11/73 processor board, modified for use with MICROVERTER (D)
* ABLE special MICROVERTER backplane (E)
* UNIBUS cable (F)
* Optional front panel interface cable.

MICROVERTER 73 is delivered with the following documentation:

* MICROVERTER Series User Guide, ABLE Number 10353X07
* LSI-11/73 Processor user guide
* Q-Bus Memory user guide.

3.2 EQUIPMENT NEEDED

Other than the PDP-11/34 system, no additional equipment is required to install and operate MICROVERTER 73. (However, additional Q-Bus memory modules can be added optionally, to a maximum of four megabytes.)

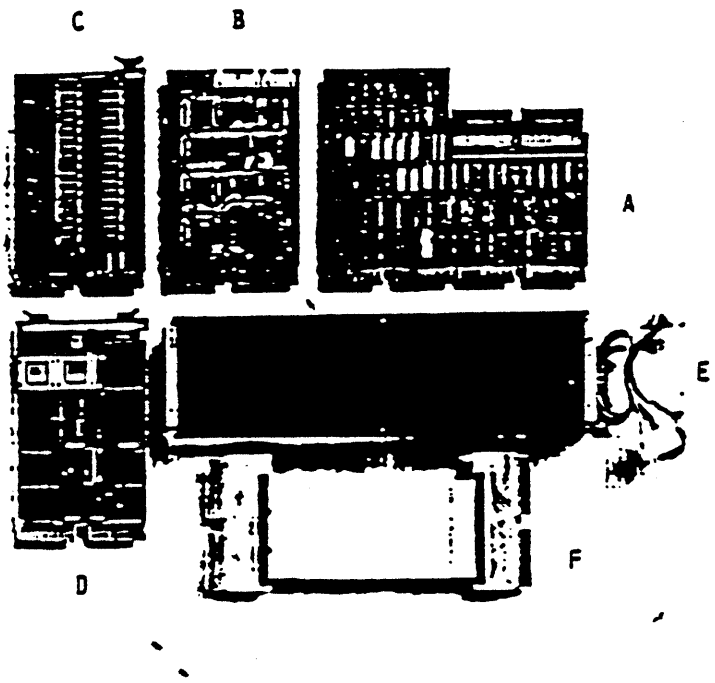

Figure 3-1: MICROVERTER 73 Components

3.3 SOFTWARE REQUIREMENTS

MICROVERTER 73 adds UNIBUS Mapping Registers (UMRs) to the Q-Bus system to give 18-bit UNIBUS devices access to 22-bit Q-Bus address space. The operating system must include software to handle UMRs. For example, RSX can be conditioned by being configured for operation on a PDP-11/44 computer. Other operating systems may need to be conditioned appropriately.

DEC operating systems RSTS/E V7.0 and V7.1 require patching to make them operate correctly with 22-bit parity memory. INIT 7.0 does not initialize the entire memory when run on a 22-bit system, and this can cause problems for RSTS/E after a power-up, due to random data and parity left in memory. See Appendix B for patches which allow INIT to correct all parity bits.

3.4 LSI-11/73 PROCESSOR

Configuration procedures for the LSI-11/73 processor board are given in the DEC LSI-11/73 user guide. When using either the DEC M9301 or M9312 bootstrap/terminator, set the processor to the micro-ODT power-up mode. Then enter the desired starting address and the micro-ODT command "G" for execution. Starting addresses (octal) are:

M9301	17773000
M9312 with diagnostics	17765020
M9312 without diagnostics	17765144

3.5 1-MEGABYTE Q-BUS MEMORY

Configuration procedures for the 1-megabyte memory board are given in the memory user guide delivered with MICROVERTER 73.

3.6 PREINSTALLATION PROCEDURE

Before beginning installation, all components should be unpacked and inspected, as follows:

STEP 1. Unpack Components

Verify that the correct equipment has been received by checking product numbers. Product numbers are:

MICROVERTER board	10340000
MICROVERTER backplane	10341000
Power regulator/console interface	10342000
UNIBUS cable	538-000-001
LSI-11/73 processor assembly	10377000
1-MB Q-Bus memory	920-010-000
Optional front panel interface cable	90000666
MICROVERTER Series User Guide	10353X07
LSI-11/73 User Guide	xxxxxxxx

1-Megabyte memory
user guide xxxxxxxx

If your shipment is not complete and correct, notify the ABLE factory immediately.

STEP 2. Inspect Components.

a. Inspect components for damage: if damage is detected, notify the carrier.

b. Save the protective containers used to ship MICROVERTER 73 for possible future use.

3.7 INSTALLATION PROCEDURE

The detailed procedures given in this chapter are correct for the PDP-11/34 and PDP-11/34A computer systems. MICROVERTER 73 is compatible with and can be installed in many other PDP-11 systems. However, variations in the construction of some systems may require differences in the detailed procedures for installing MICROVERTER 73. In such cases, the intent of the procedure should be followed rather than the exact procedure itself. For special problems, call the ABLE Support Services department (see Chapter 7).

STEP 1. Set MICROVERTER Switches

Set switches S1-1 through S1-10 on the MICROVERTER board as shown here.

Switch S1 is shown in Figure 3-2.

```
   1  2  3  4  5  6  7  8  9 10
 +-------------------------------+
 | -  -  C  -  -  -  -  C  C  - |
 +-------------------------------+
```

"C" = CLOSED (ON), "-" = OPEN (OFF)

STEP 2. Configure MICROVERTER for memory resident on UNIBUS (optional).

If the application requires the use of memory resident on the UNIBUS, configure the MICROVERTER board appropriately, using the procedure given in Appendix C.

STEP 3a. Remove NPG jumpers from backplane for DMA operation.

a. Determine the slots in the backplane which are to be used for DMA controllers.

b. Remove the NPG jumper from each of these slots. In the MICROVERTER backplane, these jumpers are located at E points adjacent to connector C, as shown in Figure 3-3.

Slot number	Jumper
5	E15 to E16
6	E13 to E14
7	E11 to E12
8	E9 to E10
9	E7 to E8

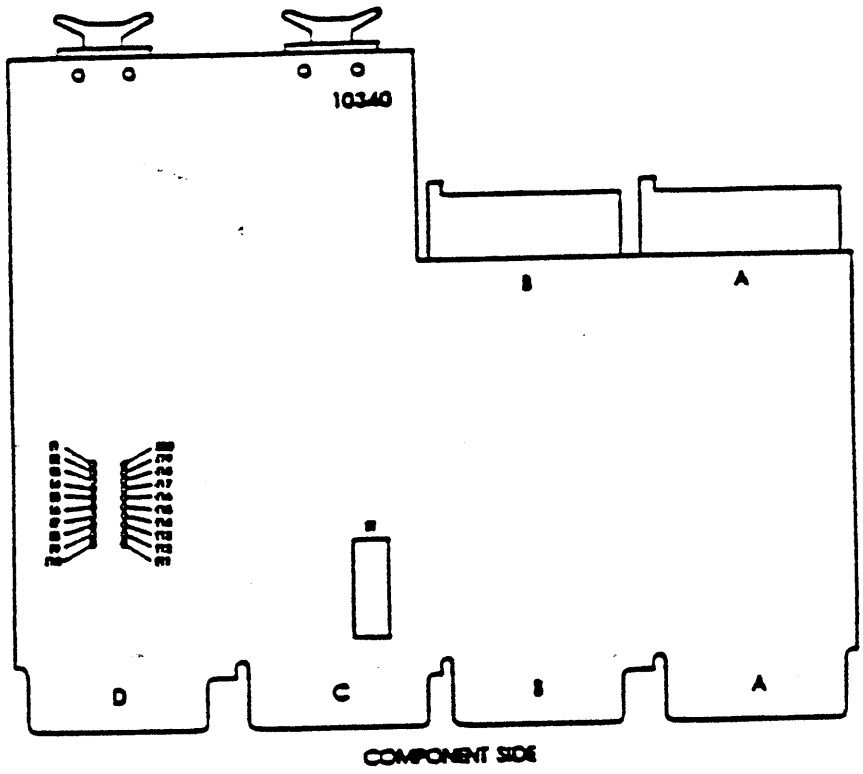

Figure 3-2: MICROVERTER Board Layout

If a DMA controller is to reside in a UNIBUS backplane other than the MICROVERTER backplane, NPG jumpers CA1 to CB1 must be removed from the appropriate slot. Consult the backplane manufacturer's documentation for the procedure.

STEP 3b. Remove IAK and DMG jumpers from backplane for Q-Bus I/O operation.

This step is required only if a Q-Bus I/O controller is to be installed in the MICROVERTER backplane.

IAK (Interrupt Acknowledge) and DMG (DMA Grant) jumpers are installed in the MICROVERTER backplane as follows:

Slot Number	Connectors
1	C, E
2	A, C, E
3	A, C, E

In each of these connectors, the IAK jumper is across pins M2 and N2, and the DMG jumper is across pins R2 and S2.

If a Q-Bus I/O controller is to reside in any of these slots, remove these jumpers from the associated connectors. (The jumpers are soldered to the pins.)

STEP 4. Select source of 60 Hz timing signal for LTC operation.

If the 60 Hz signal for the LTC is to be supplied by the UNIBUS via the power

regulator/console interface board, install a jumper across E1 and E2 on the power regulator/console interface board. See Figure 2-4 for location of E1-E2.

If the 60 Hz signal for the LTC is to be supplied by a Q-Bus board, verify that E1-E2 on the power regulator/console interface board is left open (i.e., no jumper).

STEP 5. Remove boards from PDP-11 backplane.

a. Turn off power to the PDP-11 system.

b. Pull out the drawer containing the system.

c. Locate the backplane containing the PDP-11/34 processor.

d. Locate the cable connecting the front panel with the interface board. Determine whether the cable is connected to the top of the interface board (PDP-11/34A, with keypad on front panel), or to the backplane (PDP-11/34, with no keypad on front panel). If the cable is connected to the top of the interface board, disconnect the cable from the interface board but leave it connected to the front panel. If the cable is connected to the backplane, remove the cable from the interface board and from the front panel.

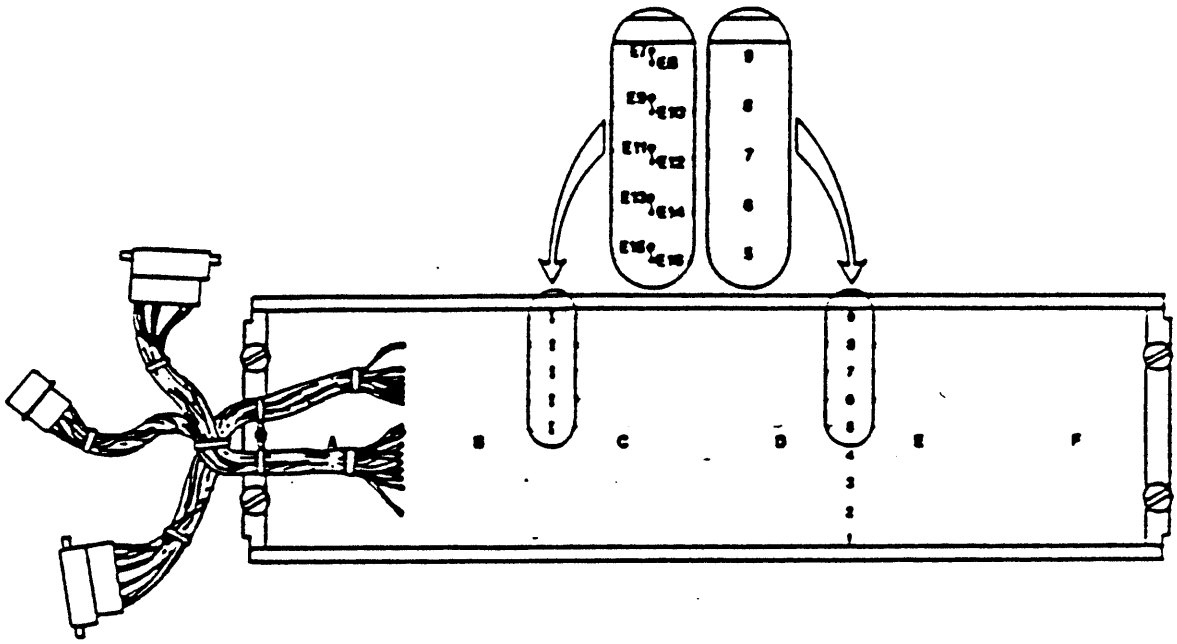

Figure 3-3: NPG Jumpers

e. Remove all boards from the processor backplane.

f. If the processor backplane is connected to the next backplane, disconnect the UNIBUS connecting cable from the processor backplane. Leave the cable connected to the next backplane.

STEP 6. Remove PDP-11 backplane from system.

a. Actuate the drawer release and swing the drawer up to expose the wirewrap side of the backplane.

b. Figure 3-4 is a view of the wirewrap side of the backplane showing the mounting screws and cable connectors. The cables are not shown.

c. Disconnect the backplane from the power distribution strip.

d. Unscrew the four mounting screws holding the backplane to the enclosure.

e. Remove the PDP-11 backplane from the system.

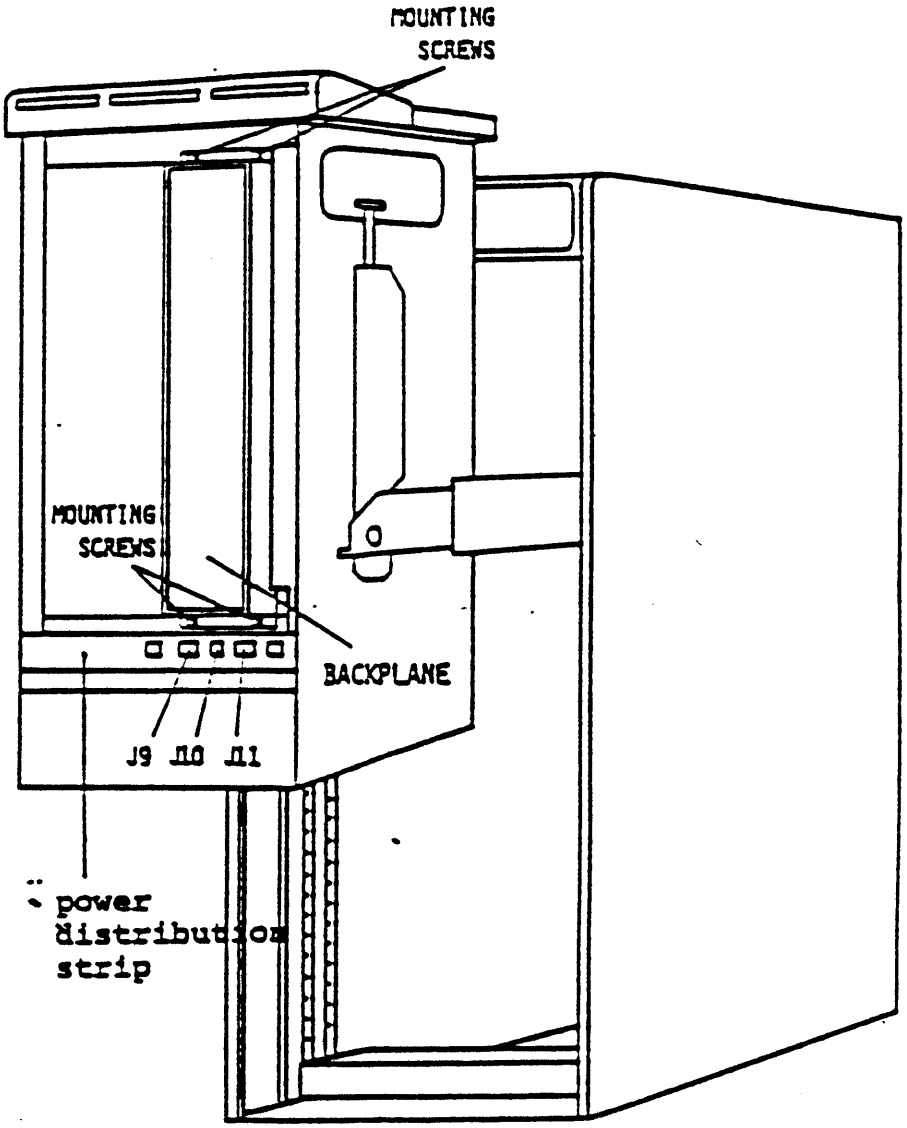

Figure 3-4: Installation of MICROVERTER Backplane

STEP 7. Install the MICROVERTER Backplane.

a. Place the MICROVERTER backplane in the space left by the PDP-11 backplane.

b. Secure the backplane in place with the four captive mounting screws.

c. Connect the backplane to the power distribution strip.

d. Swing the drawer back to its horizontal position.

STEP 8. Insert MICROVERTER Board

Insert the MICROVERTER board into slot 4 of the backplane, using sockets A through D. Insert the board so that the component side faces slot 1 of the backplane (to the right).

STEP 9. Connect UNIBUS Cable.

a. Attach one end of the UNIBUS cable (the one supplied with MICROVERTER 73) to connectors A and B at the top of the MICROVERTER board. (See Figure 3-5).

b. Insert the other end of the UNIBUS cable into slot 5 of the backplane, using sockets A and B.

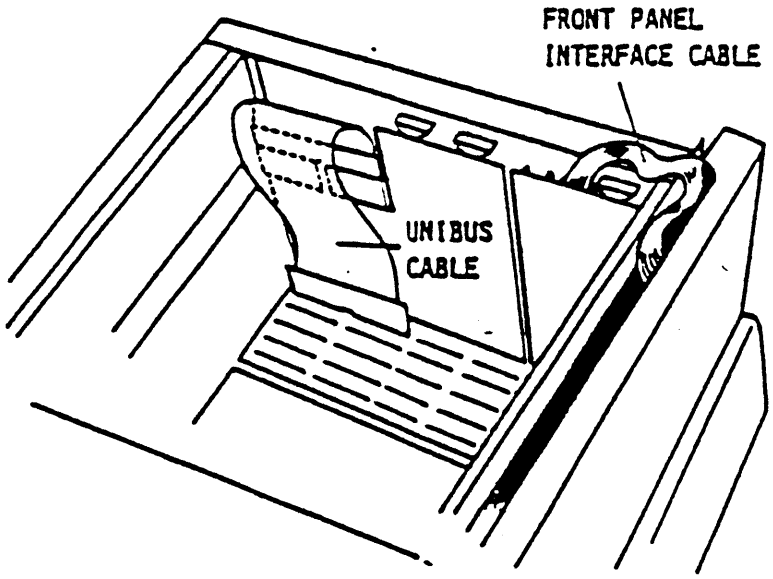

Figure 3-5: UNIBUS and Front Panel Interface Cables

STEP 10. Insert Power Regulator/Console Interface Board

Insert the power regulator/console interface board into slot 4 of the backplane, using sockets E and F. Insert the board so that the component side faces slot 1 of the backplane.

(The power regulator/console interface board and the MICROVERTER board should now be side by side in slot 4 of the backplane.)

STEP 11. Insert LSI-11/73 Processor Board

Insert the LSI-11/73 processor board into slot 1 of the backplane, using sockets A and B. Insert the board so that the component side faces the near edge of the backplane. There is a cable attached to the processor board; it passes through a strain-relief tie at the top of the board and terminates in a 4-pin connector. Plug this connector into the 4-pin socket at the top of the MICROVERTER board.

STEP 12. Insert Memory Board

Insert the 1-megabyte memory board into slot 1 of the backplane. For a dual-width board, use sockets C and D; for a quad-width board, use sockets C, D, E, and F. Insert the board so that the component side faces the near edge of the backplane. (Processor and memory are now side by side in slot 1 of the backplane.)

STEP 13. Insert Additional Memory Boards (If Any)

If additional Q-Bus memory boards are to be installed in the system, insert them into slot 2 of the backplane. Insert the boards so that the component side of each board faces slot 1 of the backplane.

STEP 14. Connect Front Panel to Power Regulator/Console Interface Board (See Figure 3-5.)

a. Determine the front panel type. If the front panel has two toggle switches, it is a (KY11/LA). If it has a group of pushbuttons, it is a KY11/LB.

b. If you have the KY11/LA front panel: locate the optional front panel interface cable supplied with MICROVERTER 73 (part number 90000666) and use this cable to connect J1 of the front panel to J2 of the power regulator/console interface board. Make this connection pin 1 to pin 1.

c. If you have the KY11/LB front panel: using the existing front panel interface cable, connect one end of the cable to the front panel, and plug the other end into connector J1 of the power regulator/console interface board. Make this connection pin 1 to pin 20.

(In Figure 3-5, the cable is shown

connected to J1 of the power regulator/console interface board, as it would be for a KY11-LB front panel.)

STEP 15. Install PDP-11 Boards in MICROVERTER Backplane.

a. If the PDP-11 backplane (removed earlier) was connected to the next backplane, insert the connecting UNIBUS cable into slot 9 of the MICROVERTER backplane, using sockets A and B.

b. Retrieve the circuit boards removed from the PDP-11 backplane.

c. Set aside the PDP-11 processor boards, the front panel interface board, and memory boards; they will not be used. (They are replaced by the LSI-11/73 processor board, the MICROVERTER power regulator/ console interface board, and the Q-Bus memory board.)

d. Insert the remaining boards into the MICROVERTER backplane, using slots 5 through 9. (Note: you should have removed the NPG jumpers from slots to be used for DMA devices.)

e. Insert the existing DEC M9301 or M9312 bootstrap/terminator in slot 6, connectors A and B, for the front-end termination of the UNIBUS. NOTE: Do not connect the bootstrap cable to the M9301 or M9312, because booting is provided through the

LSI-11/73 processor.

Check your configuration against Figure 3-6, which shows the MICROVERTER backplane with boards installed (UNIBUS controllers and bus grant cards not shown).

Check your configuration against Figure 3-7, which shows the layout of the MICROVERTER backplane.

f. Close the drawer containing the system.

g. Turn on power to the system.

h. Press the BOOT button (if necessary) to boot the system.

3.8 VERIFICATION

The system is now ready to be exercised under DEC X/11, using the "E" monitor. The KWA module can be used to exercise the Line Time Clock.

Use appropriate diagnostics to verify correct installation.

If the system does not operate correctly, go back to Step 1 of the installation procedure and verify that the entire procedure was completed correctly.

If the system still does not operate correctly, consult Appendix D, which contains installation troubleshooting

procedures.

If these measures fail to result in correct system operation, call the ABLE Support Service department (see Chapter 7 for details).

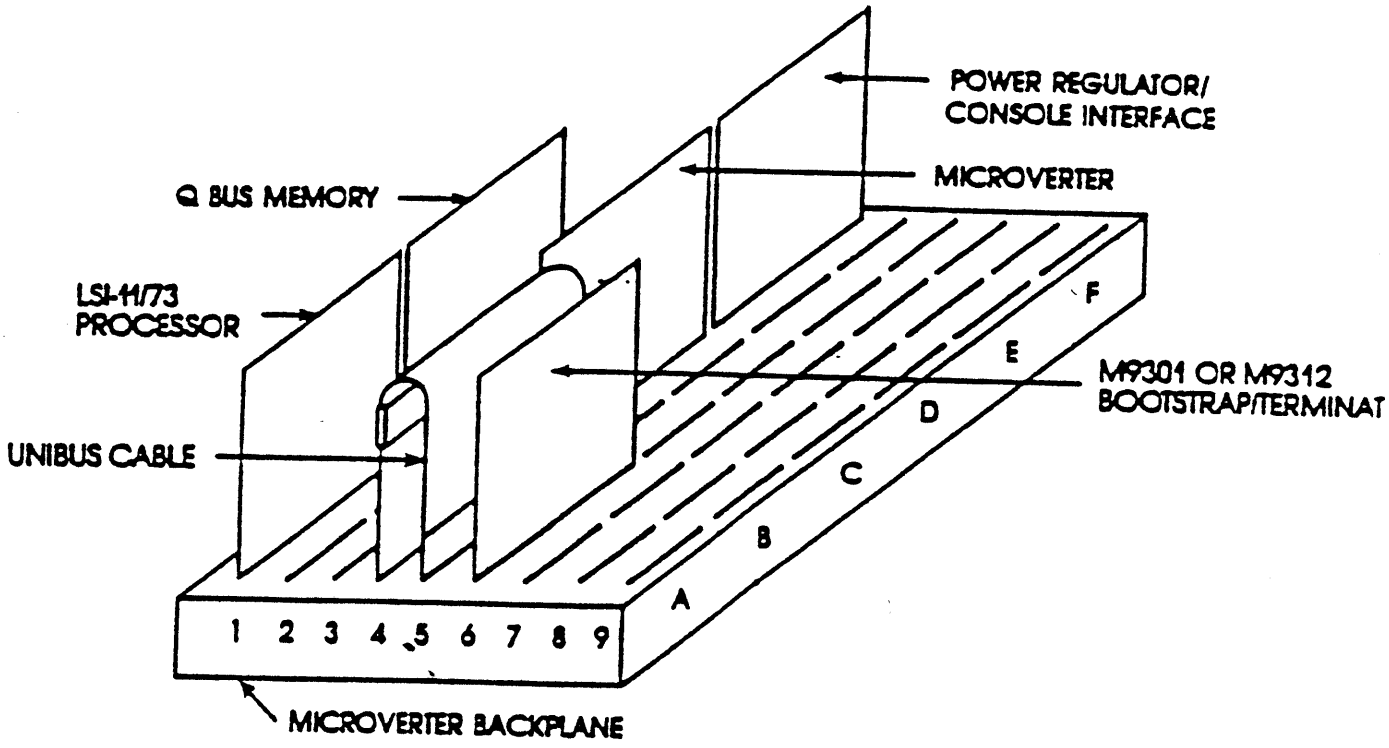

Figure 3-6: MICROVERTER 73 Configuration

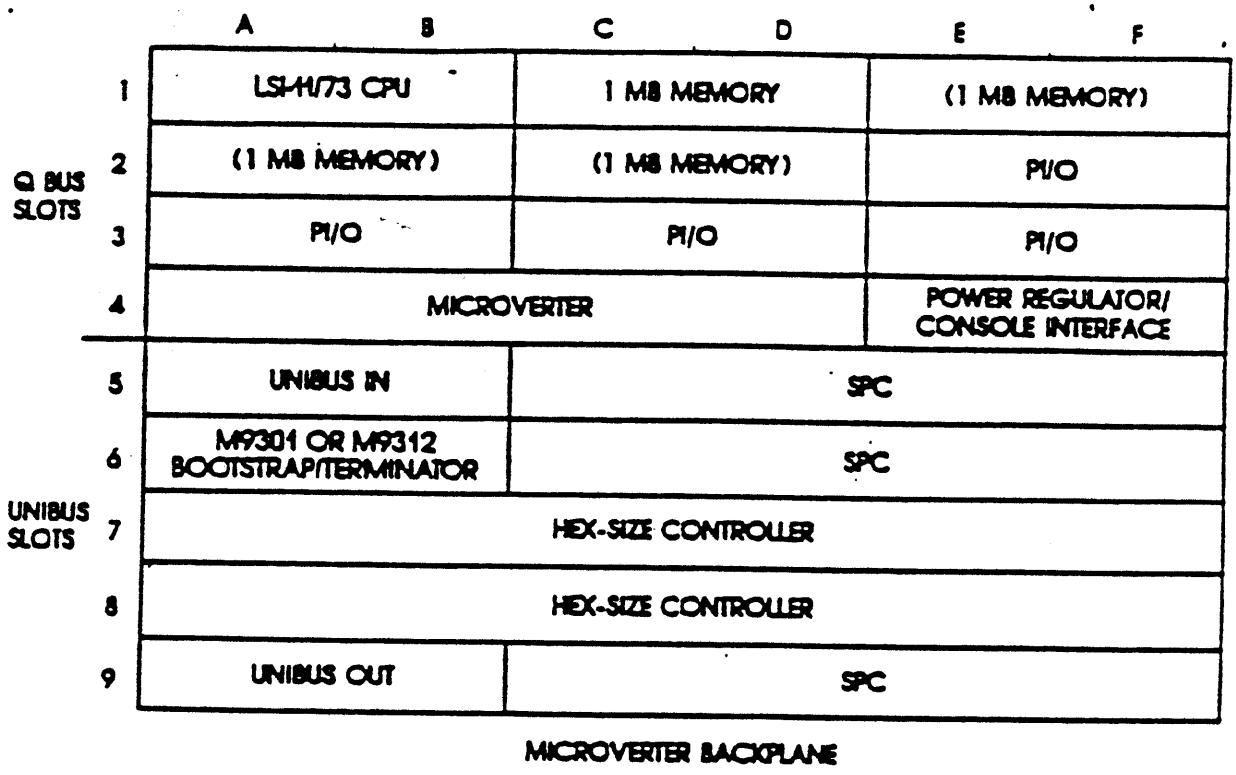

Figure 3-7: MICROVERTER Backplane Layout

CHAPTER 4

MICROVERTER PLUS INSTALLATION

4.1 GENERAL

This chapter contains procedures for installing the ABLE MICROVERTER PLUS in a PDP-11/34 computer system. MICROVERTER PLUS is compatible with a number of PDP-11 systems. However, the procedures given here apply in detail to the PDP-11/34. If you are installing MICROVERTER PLUS in another PDP-11 system, some details may be different. In such cases, change the procedure as required for the particular system.

MICROVERTER PLUS consists of the following components:

* ABLE MICROVERTER board
* ABLE Power regulator/console interface board
* ABLE hybrid MICROVERTER backplane

* UNIBUS cable
* Processor cable (required for LSI-11/73 only)
* Optional front panel interface cable
* MICROVERTER Series User Guide.

4.2 EQUIPMENT NEEDED

The following equipment, supplied by the user, is required to install and operate MICROVERTER PLUS:

* An LSI-11/23, LSI-11/23+, or LSI-11/73 processor
* Q-Bus memory modules (maximum of four megabytes)
* A DEC M9301 or M9312 bootstrap/terminator board
* A BA11-Kx expansion box
* UNIBUS controllers.

4.3 SOFTWARE REQUIREMENTS

MICROVERTER PLUS adds UNIBUS mapping registers (UMRs) to the Q-Bus system to give 18-bit UNIBUS devices access to 22-bit Q-Bus address space. The operating system must

include software to handle UMRs. For example, RSX can be conditioned by being configured for operation on a PDP-11/44 computer. Other operating systems may need to be conditioned differently.

DEC operating systems RSTS/E V7.0 and V7.1 require patching to make them operate correctly with 22-bit parity memory. INIT 7.0 does not initialize the entire memory when run on a 22-bit system, and this can cause problems for RSTS/E after a power-up, due to random data and parity left in memory. See Appendix B for patches which allow INIT to correct all parity bits.

4.4 PREINSTALLATION PROCEDURE

Before beginning installation, all components should be unpacked and inspected.

STEP 1. Verify Contents of Shipment

Verify that the correct equipment has been received by checking product numbers of the components. Product numbers are as follows:

MICROVERTER board	10340000
MICROVERTER backplane	10341000
Power regulator/console interface	10342000
UNIBUS cable	538-000-001
Processor cable	90000655

Optional front panel interface cable 90000666

If your shipment is not complete and correct, notify the ABLE factory immediately.

STEP 2. Inspect Components

a. Inspect components for damage. If damage is detected, notify the carrier immediately.

b Save the protective shipping containers for possible future use.

4.5 INSTALLATION PROCEDURE

The detailed procedures given in this chapter are correct for the installation of MICROVERTER PLUS in a PDP-11/34 and PDP-11/34A computer system. MICROVERTER PLUS is compatible with other PDP-11 systems. However, systems with differences in construction may require different detailed procedures for installing MICROVERTER PLUS. In such cases, follow the intent of the procedure rather than the exact procedure itself. For special problems, call the ABLE Support Services Department (see Chapter 7).

4.6 LSI-11/23 Processor

STEP 1. Set MICROVERTER Switches

This procedure applies to the installation of MICROVERTER PLUS in a system containing an

LSI-11/23 processor.

Set switches S1-1 through S1-10 on the MICROVERTER board as shown here. Switch S1 is shown in Figure 4-1. If the MICROVERTER LTC is not to be used, disable it by setting S1-10 open.

	SWITCH S1									
MAP ENABLE	1	2	3	4	5	6	7	8	9	10
AH1	C	-	-	-	-	-	C	C	C	C
Software	-	-	C	-	-	C	C	C	-	C

"C" = CLOSED (ON), "-" = OPEN (OFF)

STEP 2. Configure MICROVERTER for memory resident on the UNIBUS (optional).

If the application requires the use of memory resident on the UNIBUS, consult Appendix C for the procedure.

STEP 3a. Remove NPG jumpers from backplane for DMA operation.

a. Determine the slots in the backplane which are to be used for DMA controllers.

b. Remove the NPG jumper from each of these slots. The jumpers are located on the MICROVERTER backplane at E points adjacent to connector C:

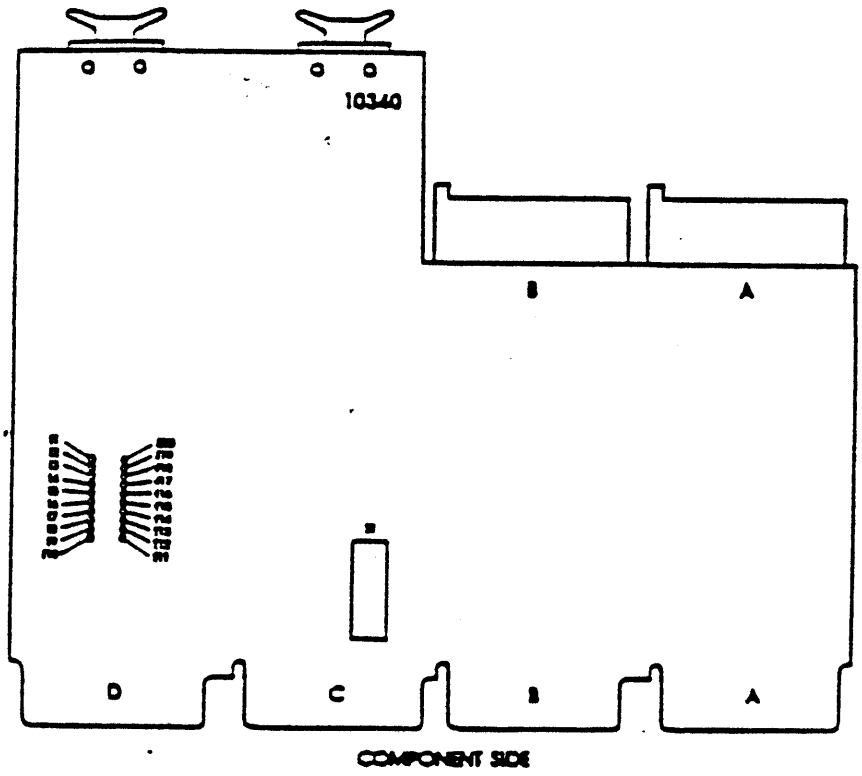

Figure 4-1: MICROVERTER Board Layout

Slot Number	Jumper
5	E15 to E16
6	E13 to E14
7	E11 to E12
8	E9 to E10
9	E7 to E8

See Figure 4-2 for the locations of these jumpers. If DMA controllers are to reside in other UNIBUS backplanes, NGP jumpers must be removed from the slots involved. Consult the backplane manufacturer's documentation for the procedure.

STEP 3b. Remove IAK and DMG jumpers from backplane for Q-Bus I/O operation.

This step is required only if a Q-Bus I/O controller is to be installed in the MICROVERTER backplane.

IAK (Interrupt Acknowledge) and DMG (DMA Grant) jumpers are installed in the MICROVERTER backplane as follows:

Slot Number	Connectors
1	C, E
2	A, C, E
3	A, C, E

In each of these connectors, the IAK jumper is across pins M2 and N2, and the DMG jumper is across pins R2 and S2.

If a Q-Bus I/O controller is to reside in any of these slots, remove these jumpers from the

associated connectors.

STEP 4. Disable BEVNT if required.

If the LTC on the MICROVERTER is to be used, disable BEVNT on the LSI-11/23 processor by installing jumper W4 on the processor board. Refer to the DEC Microcomputers and Memories Handbook for the location of jumper W4. If the MICROVERTER LTC is not to be used, disable it by opening switch S1-10 on the MICROVERTER.

STEP 5. Remove boards from PDP-11 backplane.

a. Turn off power to the PDP-11 system.

b. Pull out the drawer containing the system.

c. Locate the backplane containing the PDP-11/34 processor.

d. Remove the front panel interface cable.

e. Remove all boards from the processor backplane.

f. If the processor backplane is connected to the next backplane, disconnect the UNIBUS connecting cable from the processor backplane. Leave the cable connected to the next backplane.

STEP 6. Remove PDP-11 backplane from system.

a. Actuate the drawer release and swing the drawer up to expose the wirewrap side of the backplane.

b. Figure 4-3 is a view of the wirewrap side of the backplane showing the mounting screws and cable connectors. The cables are not shown.

c. Disconnect the backplane from the power distribution strip.

d. Unscrew the four mounting screws holding the backplane to the enclosure.

e. Remove the PDP-11 backplane from the system.

STEP 7. Install the MICROVERTER Backplane.

a. Place the special MICROVERTER backplane in the space left by the PDP-11 backplane.

b. Secure the backplane in place with the four captive mounting screws.

c. Connect the backplane to the power distribution strip.

d. Swing the drawer back to its horizontal position.

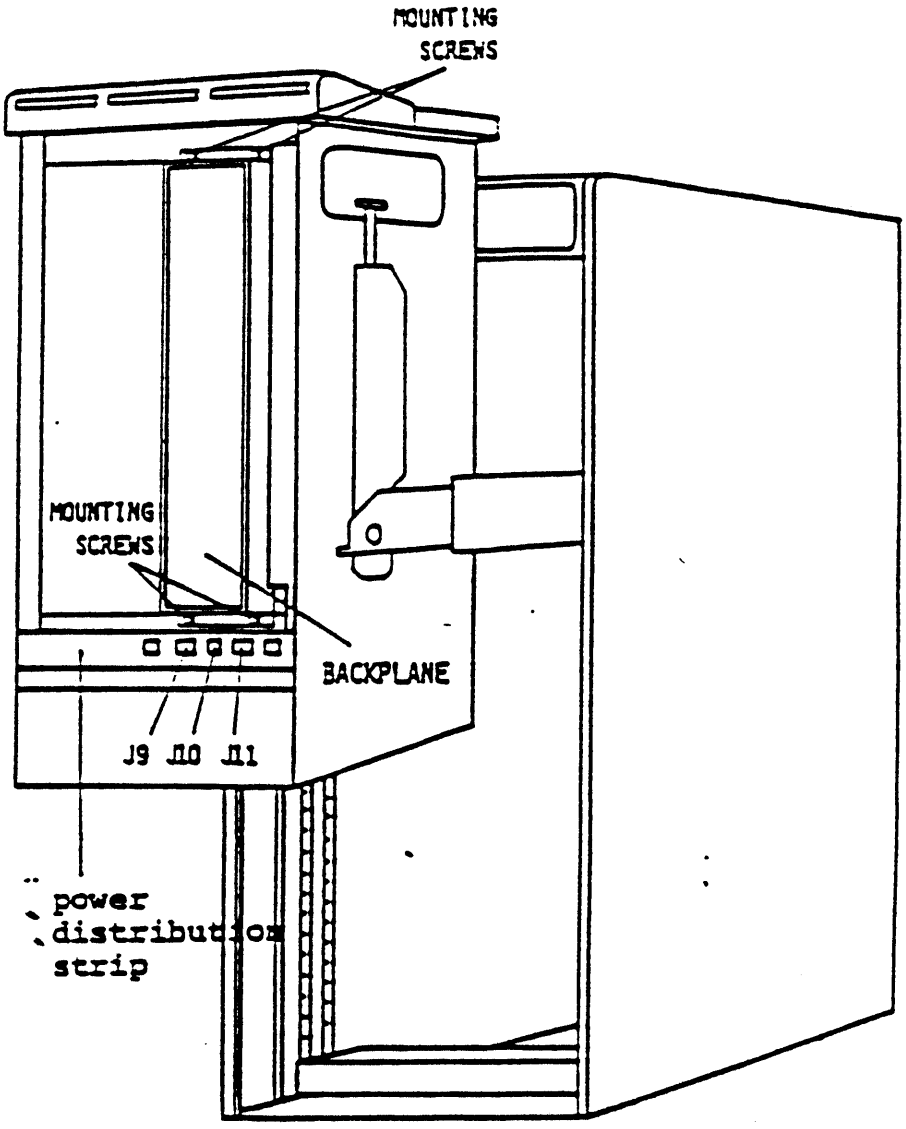

Figure 4-3: Installation of MICROVERTER Backplane

STEP 8. Insert MICROVERTER Board

Insert the MICROVERTER board into slot 4 of the backplane, using sockets A through D. Insert the board so that the component side faces slot 1 of the backplane.

STEP 9. Connect UNIBUS Cable.

a. Attach one end of the UNIBUS cable (supplied with MICROVERTER PLUS) to connectors A and B at the top of the MICROVERTER board. (See Figure 4-4).

b. Insert the other end of the UNIBUS cable into slot 5 of the backplane, using sockets A and B.

STEP 10. Insert Power Regulator/Console Interface Board.

Insert the power regulator/console interface board into slot 4 of the backplane, using sockets E and F. Insert the board so that the component side faces slot 1 of the backplane.

(The power regulator/console interface board and the MICROVERTER board should now be side by side in slot 4 of the backplane.)

STEP 11. Insert LSI-11/23 Processor Board

Insert the LSI-11/23 processor board into slot 1 of the backplane, using sockets A and B. Insert the board so that the component side faces the near edge of the backplane.

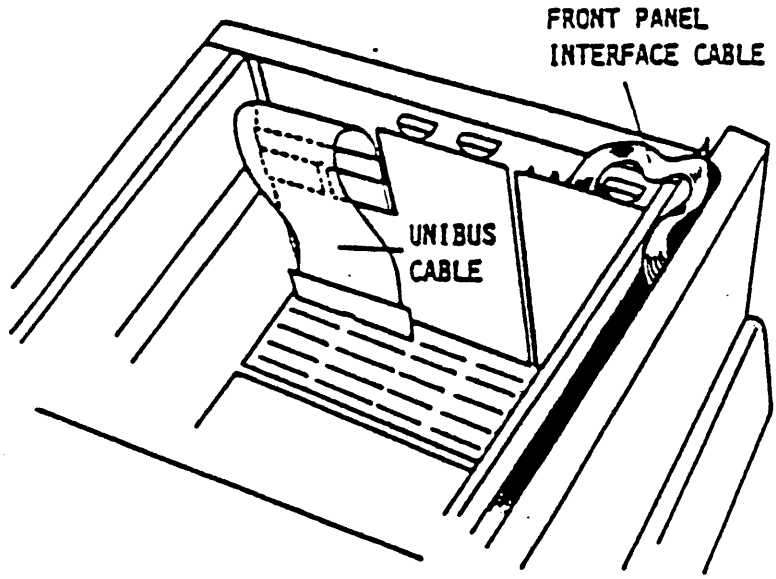

Figure 4-4: UNIBUS and Front Panel Interface Cables

STEP 12. Insert Memory Boards

Insert Q-Bus memory boards into slots 1 and 2 of the backplane. Insert each board so that the component side faces the near edge of the backplane.

STEP 13. Install PDP-11 Boards in MICROVERTER Backplane.

a. If the PDP-11 backplane (removed in Step 6) was connected to the next backplane, insert the connecting UNIBUS cable into slot 9 of the MICROVERTER backplane, using sockets A and B.

b. Retrieve the circuit boards removed from the PDP-11 backplane in step 5.

c. Set aside the two PDP-11 processor boards, the front panel interface board, and the UNIBUS memory boards: they will not be used in this system. (They are replaced by the LSI-11/23 processor board, the MICROVERTER power regulator/console interface board, and Q-Bus memory boards.)

d. Insert the remaining boards into the MICROVERTER backplane, using slots 5 through 9.

e. Insert the existing DEC M9301 or M9312 bootstrap/terminator in slot 6, connectors A and B, for the front-end termination of the UNIBUS.

f. Check your configuration against Figure 4-5, which shows the MICROVERTER backplane

with boards installed (UNIBUS controllers and bus grant cards not shown).

g. Check your configuration against Figure 4-6, which shows the MICROVERTER backplane layout.

h. Close the drawer containing the system.

i. Turn on power to the system.

j. Press the BOOT button (if necessary) to boot the system.

4.7 VERIFICATION

The system is now ready to be exercised under DEC X/11, using the "E" monitor. The KWA module can be used to exercise the Line Time Clock.

Use appropriate diagnostics to verify correct installation.

If the system does not operate correctly, go back to Step 1 of the installation procedure and verify that the entire procedure was completed correctly.

If the system still does not operate correctly, consult Appendix D, which contains installation troubleshooting procedures.

If these measures fail to result in correct system operation, call the ABLE Support Service department (see Chapter 7 for details).

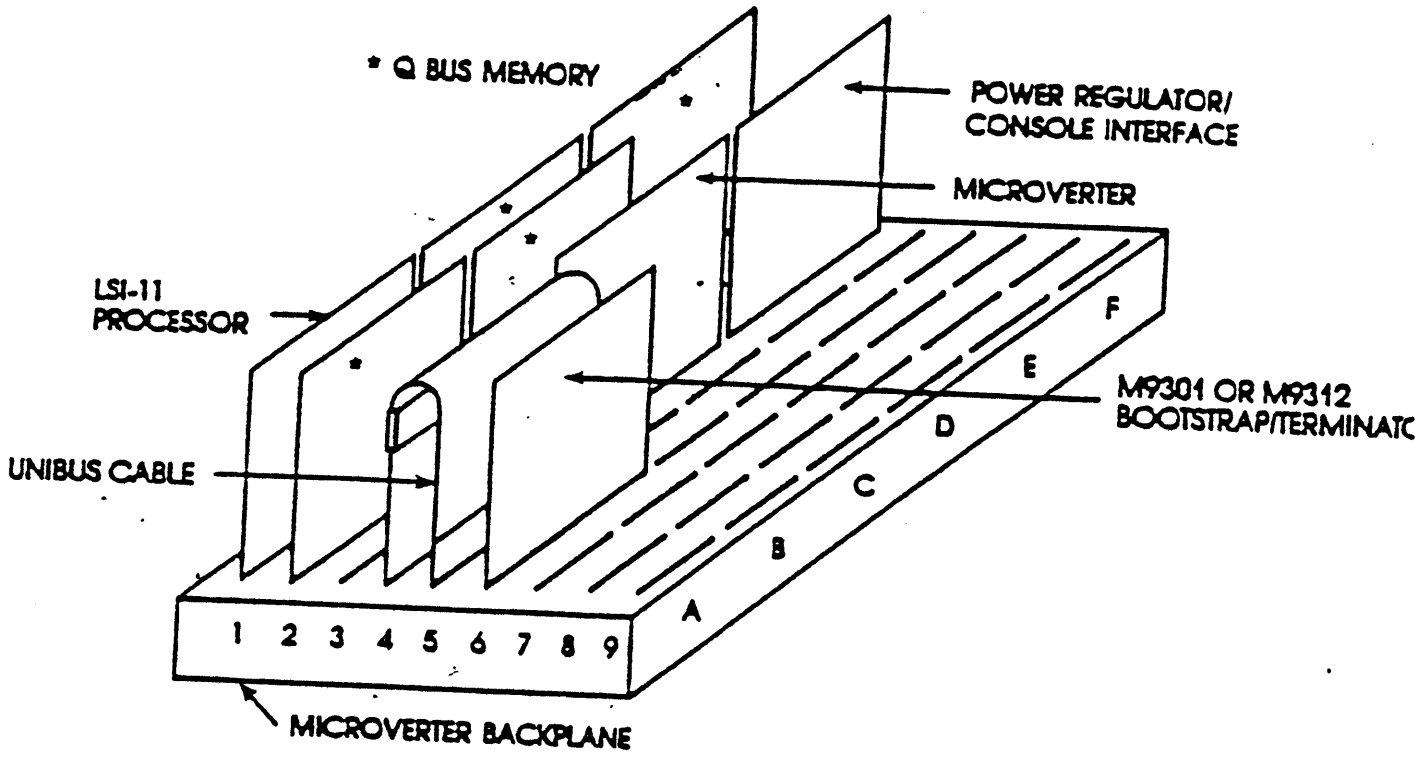

Figure 4-5: MICROVERTER PLUS Configuration

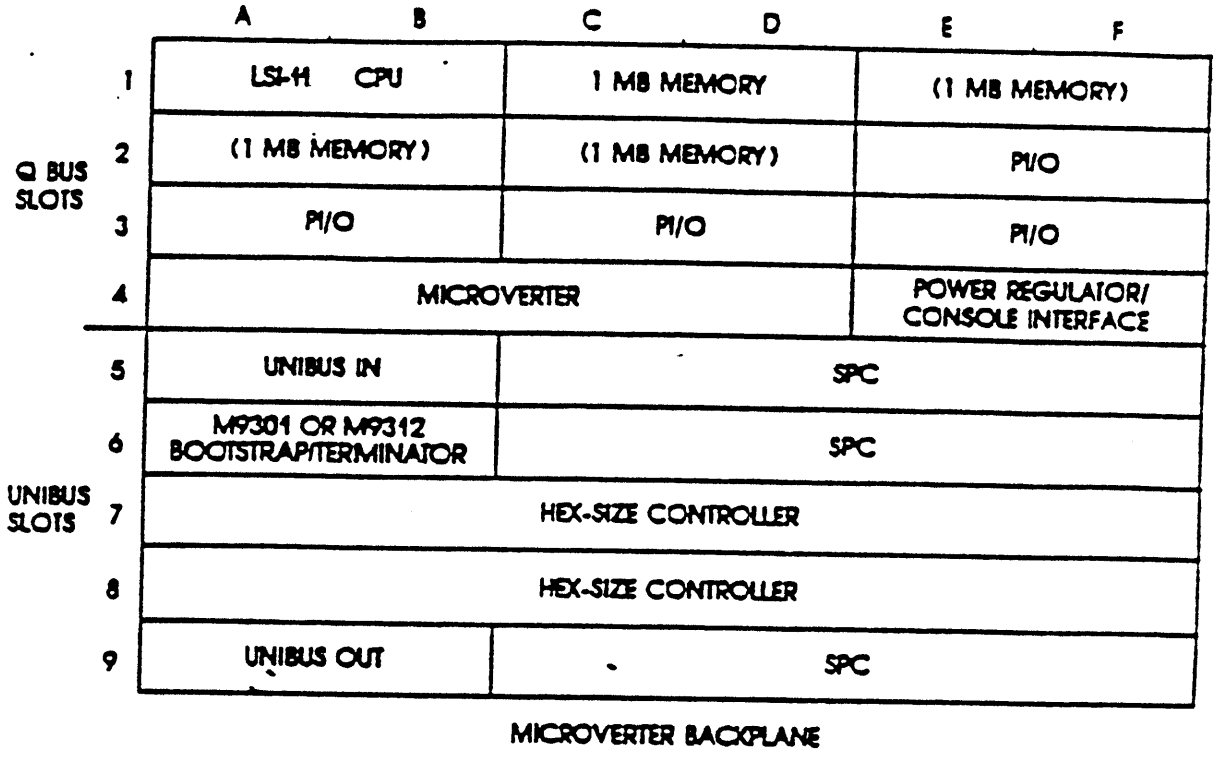

Figure 4-6: MICROVERTER Backplane Layout

4.8 LSI-11/23+ Processor

This procedure applies to the installation of MICROVERTER PLUS in a system containing an LSI-11/23+ processor.

STEP 1. Set switch S1 as shown below. To receive the Map Enable signal on pin AH1, set switch S1-1 closed. Switch S1-6 can optionally be set closed to enable the software-settable Map Enable function. If the software-settable Map Enable function is desired, hardware Map Enable switch positions S1-1 and S1-2 must be set open, as shown in the table below. Switch S1-10 must be set open, to disable the LTC.

	SWITCH S1									
MAP ENABLE	1	2	3	4	5	6	7	8	9	10
AH1**	C	-	-	-	-	-	C	C	-	-
Software	-	-	C	-	-	C	C	C	-	-

"C" = CLOSED (ON), "-" = OPEN (OFF)
"**" Requires change to processor board

STEP 2. Configure MICROVERTER for memory resident on the UNIBUS (optional).

If the application requires the use of memory resident on the UNIBUS, consult Appendix C for the procedure.

STEP 3. Modify processor board.

The LSI-11/23+ processor does not provide the UBMAPL signal required by the MICROVERTER board. However, the signal is present on the processor board, and it can be brought out to the MICROVERTER board by making the following modifications (see Figure 4-7):

1. Add a 1.5K-Ohm resistor from E74 pin 34 to E80 pin 14.

2. Add a 30-gauge wire from E74 pin 34 to backplane connector A, finger R2.

NOTE

Please contact Digital Equipment Corporation to determine whether this modification affects the warranty.

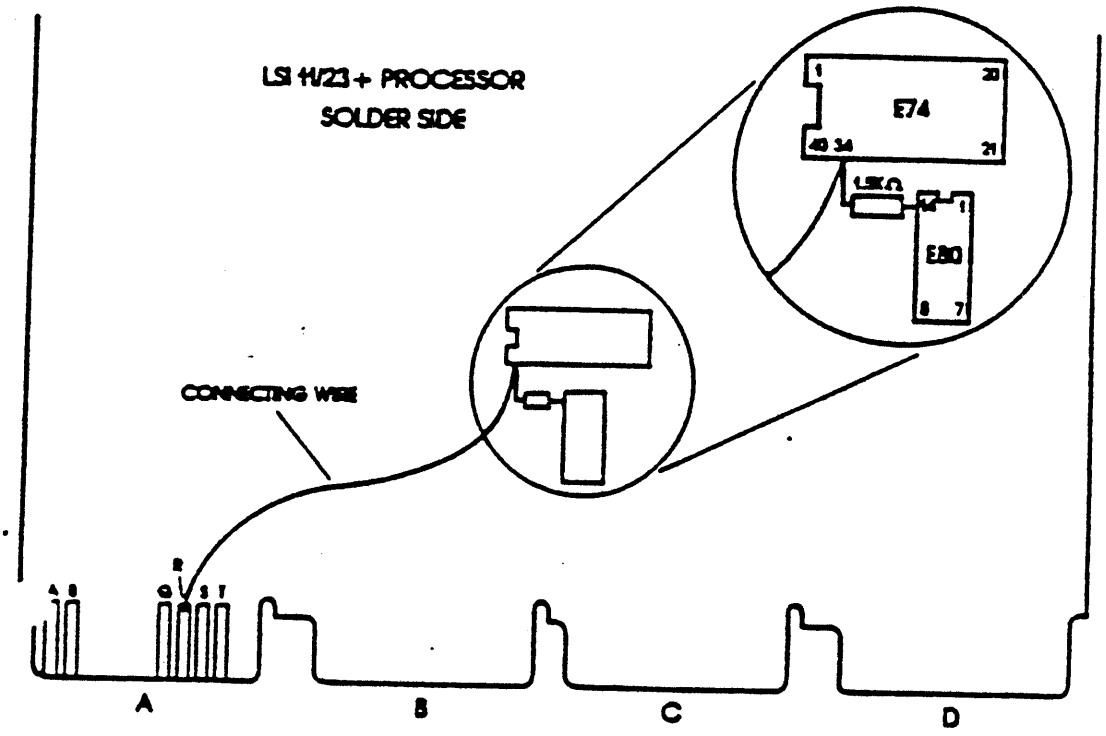

Figure 4-7: Modification to LSI-11/23+ Processor Board

STEP 4a. Remove NPG jumpers from backplane for DMA operation.

a. Determine the slots in the backplane which are to be used for DMA controllers.

b. Remove the NPG jumper from each of these slots. The jumpers are located on the MICROVERTER backplane at E points adjacent to connector C:

For slot 5, remove jumper from	E15 to E16
6	E13 to E14
7	E11 to E12
8	E9 to E10
9	E7 to E8

See Figure 4-2 for the locations of these jumpers. If DMA controllers are to reside in other UNIBUS backplanes, NPG jumpers must be removed from the slots involved. Consult the backplane manufacturer's documentation for the procedure.

STEP 4b. Remove IAK and DMG jumpers from backplane for Q-Bus I/O operation.

This step is required only if a Q-Bus I/O controller is to be installed in the MICROVERTER backplane.

IAK (Interrupt Acknowledge) and DMG (DMA Grant) jumpers are installed in the MICROVERTER backplane as follows:

Slot Number	Connectors
1	C, E
2	A, C, E
3	A, C, E

In each of these connectors, the IAK jumper is across pins M2 and N2, and the DMG jumper is across pins R2 and S2.

If a Q-Bus I/O controller is to reside in any of these slots, remove these jumpers from the associated connectors.

STEP 5. Remove boards from PDP-11 backplane.

a. Turn off power to the PDP-11 system.

b. Pull out the drawer containing the system.

c. Locate the backplane containing the PDP-11/34 processor.

d. Remove the cable connecting the front panel with the interface board.

e. Remove all circuit boards from the PDP-11 backplane.

f. If the processor backplane is connected to the next backplane, disconnect the UNIBUS connecting cable from the processor backplane, but leave the cable connected to the next backplane.

STEP 6. Remove PDP-11 backplane from system.

a. Actuate the drawer release and swing the drawer up to expose the wirewrap side of the backplane. (See Figure 4-3.)

b. Disconnect the backplane from the power distribution strip.

c. Remove the PDP-11 backplane from the system.

STEP 7. Install the MICROVERTER backplane.

a. Place the MICROVERTER backplane in the space left by the PDP-11 backplane.

b. Secure the backplane in place with the four captive mounting screws.

c. Connect the backplane to the power distribution strip.

d. Swing the drawer back to its horizontal position.

STEP 8. Insert the MICROVERTER board.

Insert the MICROVERTER board into slot 4 (A, B, C, and D) of the MICROVERTER backplane. Insert the board so that the component side faces slot 1 of the backplane.

NOTE

Slots 1 through 4 of the MICROVERTER backplane are wired for the Q-Bus. If UNIBUS boards are placed in these slots, damage can occur, resulting in repair costs not covered by warranty!

STEP 9. Connect UNIBUS cable.

a. Connect the UNIBUS cable (supplied with MICROVERTER PLUS) to connectors A and B at the top of the MICROVERTER board. (See Figure 4-4.)

b. Insert the other end of the UNIBUS cable

c. Set aside the PDP-11 processor boards, the front panel interface board, and the UNIBUS memory: they will not be used in this system. (They are replaced by the LSI-11/23+ processor board, the power regulator/console interface board, and the Q-Bus memory.)

d. Insert the remaining boards into the MICROVERTER backplane, using slots 5 through 9.

   NOTE: If a slot is used for a DMA controller, the associated NPG jumper must be removed from the backplane (see Step 6).

e. Insert the existing DEC M9301 or M9312 bootstrap/terminator in slot 6, connectors A and B, for the front-end termination of the UNIBUS.

f. Check your configuration against Figure 4-5, which shows the MICROVERTER backplane with boards installed (UNIBUS controllers and bus grant cards not shown).

g. Check your configuration against Figure 4-6, which shows the MICROVERTER backplane layout.

h. Close the drawer containing the system.

i. Turn on power to the system.

j. Press the BOOT button (if necessary) to boot the system.

4.9 VERIFICATION

The system is now ready to be exercised under DEC X/11, using the "E" monitor. The KWA module can be used to exercise the Line Time Clock.

Use appropriate diagnostics to verify correct installation.

If the system does not operate correctly, go back to Step 1 of the installation procedure and verify that the entire procedure was completed correctly.

If the system still does not operate correctly, consult Appendix D, which contains installation troubleshooting procedures.

If these measures fail to result in correct system operation, call the ABLE Support Service department (see Chapter 7 for details).

4.9.1 LSI-11/73 Processor

This procedure applies to the installation of MICROVERTER PLUS in a system containing an LSI-11/73 processor.

STEP 1. Set MICROVERTER switches.

Set switch S1 on the MICROVERTER board as shown below. (Set switches S1-3, S1-8, and S1-9 closed). Switch S1-6 can optionally be set closed to enable the Map Enable signal to be set by software. Switch S1-10 must be set open, to disable the LTC.

	SWITCH S1									
MAP ENABLE	1	2	3	4	5	6	7	8	9	10
Hardware*	-	-	C	-	-	-	-	C	C	-
Software	-	-	C	-	-	C	C	C	-	-

"C" = CLOSED (ON), "-" = OPEN (OFF)

STEP 2. Configure MICROVERTER for memory resident on the UNIBUS (optional).

If the application requires the use of memory resident on the UNIBUS, consult Appendix C for the procedure.

STEP 3. Select source of 60 Hz timing signal for LTC operation.

If the 60 Hz signal for the LTC is to be supplied by the UNIBUS via the power regulator/console interface board, install a jumper across E1 and E2 on the power

regulator/console interface board. (See Figure 2-4 for location of E1-E2.)

If the 60 Hz signal for the LTC is to be supplied by a Q-Bus board, verify that E1-E2 on the power regulator/console interface board is left open (i.e., no jumper).

STEP 4. Modify processor board

The Map Enable signal and the Address Latch Enable (ALE) Timing Strobe signal have their sources on the LSI-11/73 processor board, but are not available to the MICROVERTER board.

The processor cable is supplied with MICROVERTER PLUS for the purpose of bringing these signals to the MICROVERTER board. Two procedures are given here. The first procedure, using the cable as supplied, with two leads attached, is suitable for initial installation and product verification. The second procedure, in which the leads are cut off and the wires are soldered to the board, is recommended for permanent installation.

Interim Procedure

The processor cable has two color-coded leads, one red and one black.

a. Connect the black clip to pin 12 of IC 39, as shown in Figure 4-8.

b. Connect the red clip to pin 19 of IC 36, as shown in Figure 4-8.

Make the connections very carefully, to avoid short-circuiting to adjacent pins and also to avoid damaging the delicate clips.

NOTE

ABLE does not recommend the use of these leads on a long-term basis because of the possibility of intermittent errors.

Permanent Installation

a. Label or mark the wire carrying the red lead.

b. Cut the "red lead" wire to make it an inch or two shorter than the "black lead" wire.

c. Solder the shorter wire to pin 19 of IC 36, as shown in Figure 4-9.

d. Solder the other wire to pin 12 of IC 39, as shown in Figure 4-9.

e. Provide strain-relief for the cable: run the plastic tie wrap (supplied with the cable) through the left edge handle eyelet on the processor board and then around the cable. Make the wrap snug around the cable, but do not overtighten and damage the cable.

STEP 5a. Remove NPG jumpers from backplane for DMA operation.

a. Determine the slots in the backplane which are to be used for DMA controllers.

b. Remove the NPG jumper from each of these slots. The jumpers are located on the MICROVERTER backplane at E points adjacent to connector C:

Slot Number	Jumper
5	E15 to E16
6	E13 to E14
7	E11 to E12
8	E9 to E10
9	E7 to E8

See Figure 4-2 for the locations of these jumpers. If DMA controllers are to reside in other UNIBUS backplanes, NPG jumpers must be removed from the slots involved. Consult the backplane manufacturer's documentation for the procedure.

STEP 5b. Remove IAK and DMG jumpers from backplane for Q-Bus I/O operation.

If a Q-Bus I/O controller is to be installed in a backplane slot containing IAK (Interrupt Acknowledge) and DMG (DMA Grant) jumpers, remove the jumpers.

IAK and DMG jumpers are factory-installed in the MICROVERTER backplane as follows:

Slot Number	Connectors
1	C, E
2	A, C, E
3	A, C, E

In each of these connectors, the IAK jumper is across pins M2 and N2, and the DMG jumper is across pins R2 and S2. The jumpers are soldered to the pins.

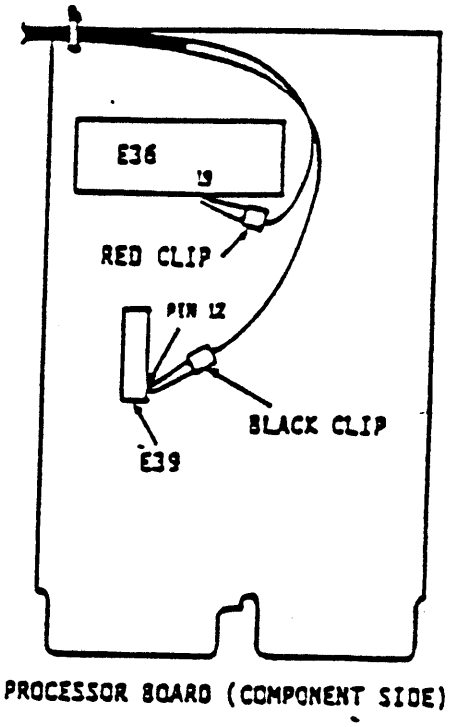

Figure 4-8: LSI-11/73 Processor Board
Temporary Modification

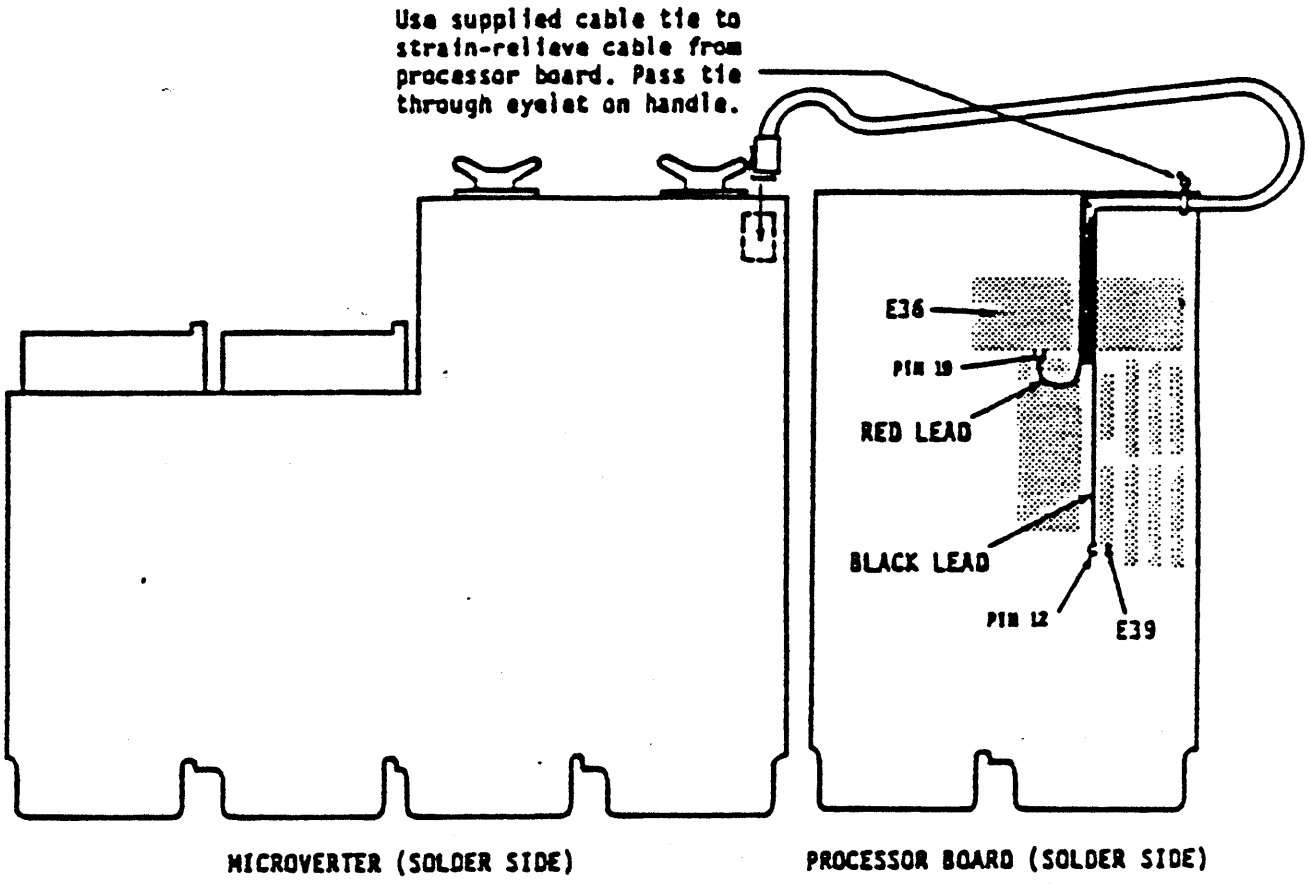

Figure 4-9: LSI-11/73 Processor Board Permanent Modification

STEP 6. Remove boards from PDP-11 backplane.

a. Turn off power to the PDP-11 system.

b. Pull out the drawer containing the system.

c. Locate the backplane containing the PDP-11/34 processor.

d. Locate the cable connecting the front panel with the interface board. Determine whether the cable is connected to the top of the interface board (PDP-11/34A, with keypad on front panel), or to the backplane (PDP-11/34, with no keypad on front panel). If the cable is connected to the top of the interface board, disconnect the cable from the interface board but leave it connected to the front panel. If the cable is connected to the backplane, disconnect the cable from the front panel.

e. Remove all boards. from the processor backplane.

f. If the processor backplane is connected to the next backplane, disconnect the UNIBUS connecting cable from the processor backplane. Leave the cable connected to the next backplane.

STEP 7. Remove PDP-11 backplane from system.

a. Actuate the drawer release and swing the drawer up to expose the wirewrap side of the backplane.

b. Figure 4-3 is a view of the wirewrap side of the backplane showing the mounting

screws and cable connectors. The cables are not shown.

c. If the front panel interface cable is connected to the backplane, disconnect the cable from the backplane. d. Disconnect the backplane from the power distribution strip.

e. Unscrew the four mounting screws holding the backplane to the enclosure.

f. Remove the PDP-11 backplane from the system.

STEP 8. Install the MICROVERTER Backplane.

a. Place the special MICROVERTER backplane in the space left by the PDP-11 backplane.

b. Secure the backplane in place with the four captive mounting screws.

c. Connect the backplane to the power distribution strip.

d. Swing the drawer back to its horizontal position.

STEP 9. Insert MICROVERTER Board

Insert the MICROVERTER board into slot 4 of the backplane, using sockets A through D. Insert the board so that the component side faces slot 1 of the backplane.

STEP 10. Connect UNIBUS Cable.

a. Attach one end of the UNIBUS cable (the one supplied with MICROVERTER 73) to

connectors A and B at the top of the MICROVERTER board. (See Figure 4-4).

b. Insert the other end of the UNIBUS cable into slot 5 of the backplane, using sockets A and B.

STEP 11. Insert Power Regulator/Console Interface Board

Insert the power regulator/console interface board into slot 4 of the backplane, using sockets E and F. Insert the board so that the component side faces slot 1 of the backplane.

(The power regulator/console interface board and the MICROVERTER board should now be side by side in slot 4 of the backplane.)

STEP 12. Insert LSI-11/73 Processor Board

Insert the LSI-11/73 processor board into slot 1 of the backplane, using sockets A and B. Insert the board so that the component side faces the near edge of the backplane. The processor cable (attached to the processor board and passing through a strain-relief tie at the top of the board) terminates in a 4-pin connector. Plug this connector into the 4-pin socket at the top of the MICROVERTER board.

STEP 13. Insert Memory Boards

Insert Q-Bus memory boards into slots 1 and 2 of the backplane. Insert the boards so that the component sides face the near edge of the backplane.

STEP 14. (PDP-11/34(A) only) Connect Front Panel Interface Cable. (See Figure 4-4.)

The PDP-11/34 and PDP-11/34A computer systems have different front panels. The PDP-11/34 front panel (KY11/LA) has two toggle switches labeled BOOT/HALT and CONTINUE/RUN respectively. The PDP-11/34B front panel (KY11-LB) has a keypad in addition to the two toggle switches. The KY11/LB front panel interface cable connects to the top of the interface board, but the KY11/LA front panel interface cable connects underneath the backplane. The PDP-11 front panel interface board is replaced by the MICROVERTER 73's power regulator/console interface board, which has connectors at the top of the board for the interface cable.

If you have the KY11/LB front panel, one end of the front panel interface cable is still connected to the front panel. Plug the free end of the cable into connector J1 on top of the power regulator/console interface board. Make this connection pin 1 to pin 20.

If you have the KY11/LA front panel, you have already removed the front panel interface cable completely. Locate the optional front panel interface cable supplied with MICROVERTER 73 (part number 90000666) and use this cable to connect J1 of the front panel to J2 of the power regulator/console interface board. Make this connection pin 1 to pin 1.

(In Figure 4-4, the cable is shown connected to J2 of the power regulator/console interface board, as it would be for a PDP-11/34, with KY11-LA front panel.)

STEP 15. Install PDP-11 Boards in MICROVERTER Backplane.

a. If the PDP-11 backplane (removed in Step 6) was connected to the next backplane, insert the connecting UNIBUS cable into slot 9 of the MICROVERTER backplane, using sockets A and B.

b. Retrieve the circuit boards removed from the PDP-11 backplane in step 5.

c. Set aside the two PDP-11 processor boards and the front panel interface board: they will not be used in this system. (They are replaced by the LSI-11/73 processor board and the MICROVERTER power regulator/ console interface board.)

d. Insert the remaining boards into the MICROVERTER backplane, using slots 5 through 9.

   NOTE: Each slot used for a DMA controller must have its NPG jumper removed (see Step 7).

e. Insert the existing DEC M9301 or M9312 bootstrap/terminator in slot 6, connectors A and B, for the front-end termination of the UNIBUS.

f. Check your configuration against Figure 4-5, which shows the MICROVERTER backplane with boards installed (UNIBUS controllers and bus grant cards not shown.)

g. Check your configuration against Figure 4-6, which shows the MICROVERTER backplane layout.

h. Close the drawer containing the system.

i. Turn on power to the system.

j. Press the BOOT button (if necessary) to boot the system.

4.10 VERIFICATION

The system is now ready to be exercised under DEC X/11, using the "E" monitor. The KWA module can be used to exercise the Line Time Clock.

Use appropriate diagnostics to verify correct installation.

If the system does not operate correctly, go back to Step 1 of the installation procedure and verify that the entire procedure was completed correctly.

If the system still does not operate correctly, consult Appendix D, which contains installation troubleshooting procedures.

If these measures fail to result in correct system operation, call the ABLE Support Service department (see Chapter 7 for details).

CHAPTER 5

MICROVERTER BD INSTALLATION

5.1 GENERAL

This chapter contains procedures for installing the ABLE MICROVERTER BD in a system containing an LSI-11/23, LSI-11/23+, or LSI-11/73 processor.

MICROVERTER BD consists of the following components:

* ABLE MICROVERTER board
* Processor cable (required for use with LSI-11/73 processor only)

5.2 EQUIPMENT NEEDED

The following equipment, supplied by the user, is required to install and operate MICROVERTER BD:

* An LSI-11/23, LSI-11/23+, or LSI-11/73 processor
* Q-Bus memory modules (maximum of four megabytes)
* A DEC M9301 or M9312 bootstrap/terminator board
* A BA11-Kx expansion box
* UNIBUS controllers.
* UNIBUS cable (BC11A-XX)

5.3 SOFTWARE REQUIREMENT

MICROVERTER BD adds UNIBUS mapping registers (UMRs) to the Q-Bus system to give 18-bit UNIBUS devices access to 22-bit Q-Bus address space. The operating system must include software to handle UMRs. For example, RSX can be conditioned by being configured for operation on a PDP-11/44 computer. Other operating systems may need to be conditioned differently.

DEC operating systems RSTS/E V7.0 and V7.1 require patching to make them operate correctly with 22-bit parity memory. INIT 7.0 does not initialize the entire memory when run on a 22-bit system, and this can cause problems for RSTS/E after a power-up, due to random data and parity left in memory. See Appendix B for patches which allow INIT to correct all parity bits.

5.4 PREINSTALLATION PROCEDURE

Before beginning installation of MICROVERTER BD, the components should be unpacked and inspected.

STEP 1. Unpack Components

Verify that the correct equipment has been received by checking product numbers:

MICROVERTER board	10340000
Processor cable (Required for LSI-11/73 only)	90000655

If your shipment is not complete and correct, notify ABLE COMPUTER immediately.

STEP 2. Inspect Components

a. Inspect components for damage. If damage is detected, notify the carrier.

b. Save the protective shipping container for possible future use.

5.5 INSTALLATION PROCEDURE

This chapter contains step-by-step procedures for installing MICROVERTER BD in a system containing an LSI-11/23, LSI-11/23+, or LSI-11/73 processor.

5.6 LSI-11/23 Processor

This procedures applies to the installation of MICROVERTER BD in a system containing an LSI-11/23 processor.

STEP 1. Set MICROVERTER switches

Set switches S1-1 through S1-10 as shown below. Switch S1 is is shown in Figure 5-1. To receive the Map Enable signal on pin AH1, set switch S1-1 closed. To receive the Map Enable signal on pin BH1, set switch S1-2 closed. Switch S1-6 can optionally be set closed to enable the software-settable Map Enable function. If the software-settable Map Enable function is desired, the hardware Map Enable switch position S1-1 and S1-2 must be set open. Switch S1-10 must be set closed, to enable the LTC.

MAP ENABLE	SWITCH S1 1	2	3	4	5	6	7	8	9	10
AH1	C	-	-	-	-	-	C	C	C	C
BH1	-	C	-	-	-	-	C	C	C	C
Software	-	-	C	-	-	C	C	C	-	C

"C" = CLOSED (ON), "-" = OPEN (OFF)

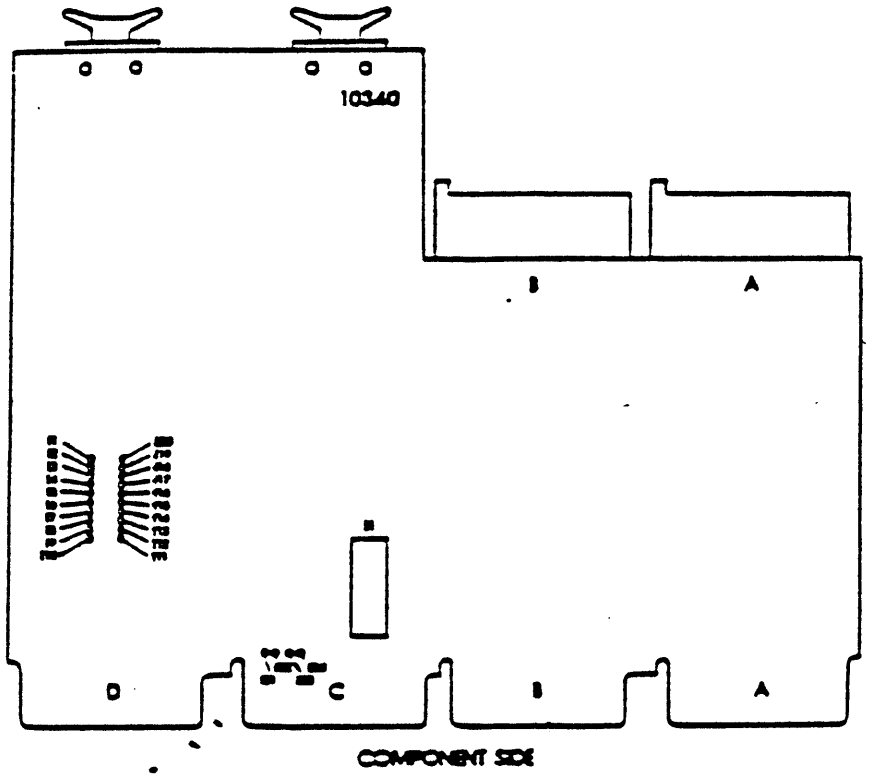

Figure 5-1: MICROVERTER Board Layout

STEP 2. Configure MICROVERTER for memory resident on the UNIBUS (optional).

If the application requires the use of memory resident on the UNIBUS, consult Appendix C for the procedure.

STEP 3. MICROVERTER Jumpers

If connectors C and D (in the backplane slot in which the MICROVERTER board is installed) are used for anything other than the Q-Bus, the following two jumpers, located on the MICROVERTER board, may have to be removed:

E21-E22 Passes DMG signal to devices located behind MICROVERTER.

E23-E24 Passes IAK signal to devices located behind MICROVERTER.

STEP 4. Configure processor for LTC.

If the LTC on the MICROVERTER is to be used, disable BEVNT on the LSI-11/23 by installing jumper W4 on the processor board. Refer to the DEC Microcomputers and Memories Handbook for the location of jumper W4.

STEP 5. Modify backplane.

a. MICROVERTER can receive the Map Enable signal on pin AH1 or pin BH1. Add a wire on the backplane from pin AR2 of the processor slot to pin AH1 or pin BH1 of the MICROVERTER board slot. (Note: your setting of

switches S1-1 and S1-2 in Step 3 must correspond with your selection here.)

b. If the backplane does not support 22-bit addressing, it must be modified. See Appendix A for a backplane modification procedure.

STEP 6. Insert MICROVERTER into backplane

Insert the MICROVERTER board into any quad-slot of the LSI-11/23 system backplane.

STEP 7. Verify bus grant continuity.

Verify that each slot between the MICROVERTER and the processor contains either a module or a Q-Bus grant card. If grant cards are not available, position the boards so that there are no empty slots between boards.

STEP 8. Verify that boards are in correct priority order.

MICROVERTER follows the position-independent priority rules of the Q-Bus. LSI-11 I/O interfaces can be located either ahead of or behind the MICROVERTER. Devices located behind MICROVERTER have a lower priority than UNIBUS devices of the same level attached to the MICROVERTER. Refer to the DEC Microcomputers and Memories Handbook for further information on the Q-Bus.

STEP 9. Install UNIBUS peripheral controllers.

Insert UNIBUS controller boards in a UNIBUS backplane which is supplied with the appropriate power. Insert a UNIBUS terminator in connectors A and B of the last slot of the UNIBUS backplane. (If there is more than one UNIBUS backplane, insert the terminator in the last slot of the last UNIBUS backplane.) Connect the UNIBUS backplane to MICROVERTER with a standard UNIBUS cable, utilizing the first UNIBUS connectors in the UNIBUS backplane and the connectors at the top of the MICROVERTER board. The resulting configuration is shown in Figure 5-2 (UNIBUS controllers, etc., not shown).

STEP 10. Verify that all 18-bit DMA devices are installed on the UNIBUS.

5.7 VERIFICATION

The system is now ready to be exercised under DEC X/11, using the "E" monitor. The KWA module can be used to exercise the Line Time Clock.

Use appropriate diagnostics to verify correct installation.

If the system does not operate correctly, go back to Step 1 of the installation procedure and verify that the entire procedure was completed correctly.

If the system still does not operate correctly, consult Appendix D, which contains installation troubleshooting procedures.

If these measures fail to result in correct system operation, call the ABLE Support Service department (see Chapter 7 for details).

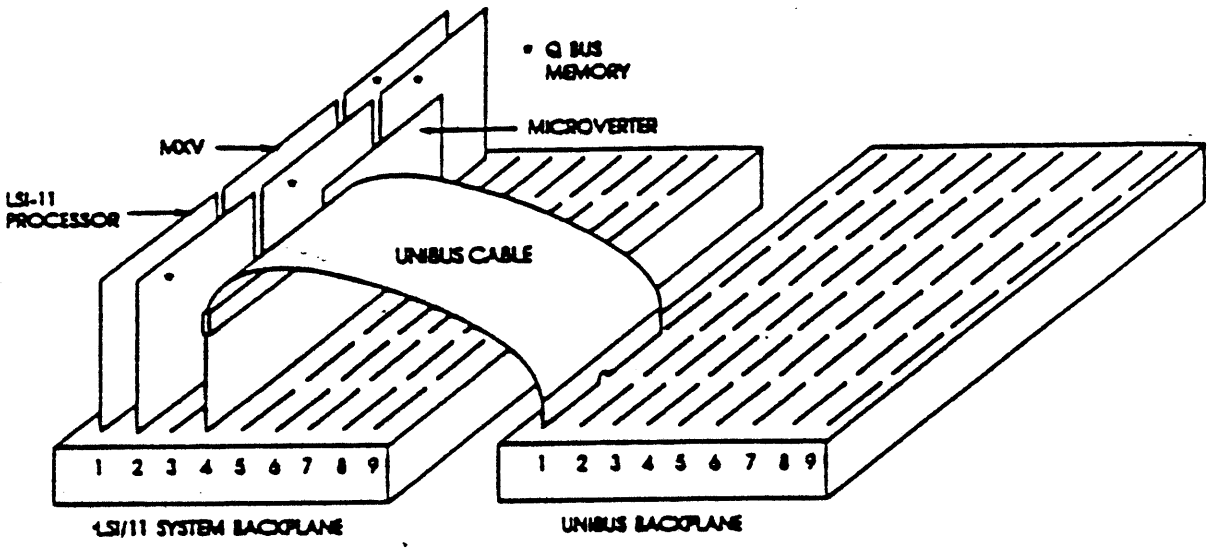

Figure 5-2: System Configuration

5.8 LSI-11/23+ Processor

This procedure applies to the installation of MICROVERTER BD in a system containing an LSI-11/23+ processor.

STEP 1. Set MICROVERTER switches.

Set switches S1 as shown below. To receive the Map Enable signal on pin AH1, set switch S1-1 closed. To receive the Map Enable signal on pin BH1, set switch S1-2 closed. Switch S1-6 can optionally be set closed to enable the software-settable Map Enable function. If the software-settable Map Enable function is desired, the hardware Map Enable switch positions S1-1 and S1-2 must be set open. Set switch S1-10 open, to disable the LTC.

MAP ENABLE	SWITCH S1 1	2	3	4	5	6	7	8	9	10
AH1**	C	-	-	-	-	-	C	C	-	-
BH1**	-	C	-	-	-	-	C	C	-	-
Software	-	-	C	-	-	C	C	C	-	-

"C" = CLOSED (ON), "-" = OPEN (OFF)

STEP 2. Configure MICROVERTER for memory resident on the UNIBUS (optional).

If the application requires the use of memory resident on the UNIBUS, consult Appendix C for the procedure.

STEP 3. Modify processor board

The LSI-11/23+ processor does not provide the UBMAPL-L signal required by the MICROVERTER. However, the signal is present on the processor board, and it can be brought out to the MICROVERTER by making the following modifications (see Figure 5-3):

1. Add a 1.5K-Ohm resistor from E74 pin 34 to E80 pin 14.

2. Add a 30-gauge wire from E74 pin 34 to backplane connector A, finger R2.

NOTE

Please contact Digital Equipment Corporation to determine whether this modification affects the warranty.

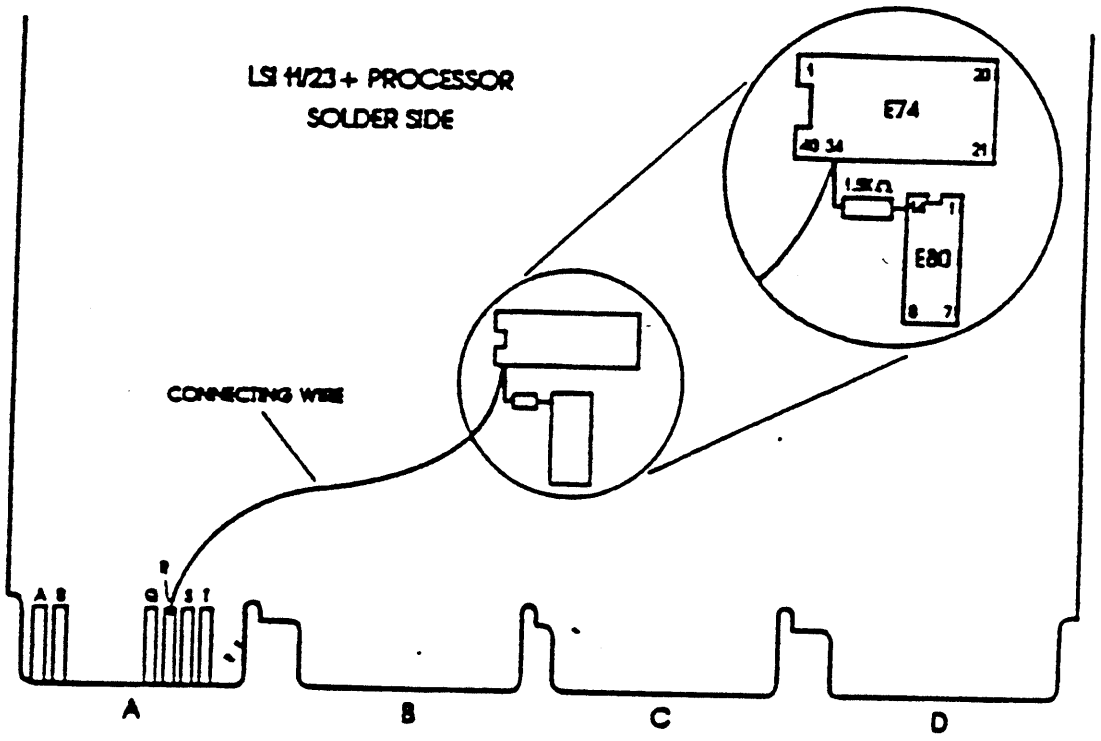

Figure 5-3: Modification to LSI-11/23+ Processor Board

STEP 7. Modify backplane

a. MICROVERTER can receive the Map Enable signal on pin AH1 or pin BH1. Add a wire on the backplane from pin AR2 of the processor slot to pin AH1 or pin BH1 of the MICROVERTER board slot. (Switches S1-1 and S1-2 must be set appropriately: see above.)

b. Determine whether the backplane supports 22-bit addressing. If it does not, it must be modified. See Appendix A for a backplane modification procedure.

STEP 8. Insert MICROVERTER in backplane

Insert the MICROVERTER board into any quad-slot of the LSI-11/23+ system backplane.

STEP 9. Verify bus grant continuity.

Verify that each slot between the MICROVERTER and the processor contains either a module or a Q-Bus grant card. If grant cards are not available, position the boards so that there are no empty slots between boards.

STEP 10. Verify that boards are in correct priority order.

MICROVERTER follows the position-independent priority rules of the Q-Bus. LSI-11 I/O interfaces can be located either ahead of or behind the MICROVERTER. Devices located behind MICROVERTER have a lower

priority than UNIBUS devices of the same level attached to the MICROVERTER. Refer to the DEC Microcomputers and Memories Handbook for further information on the Q-Bus.

STEP 11. Install UNIBUS peripheral controllers.

Insert UNIBUS controller boards in a UNIBUS backplane which is supplied with the appropriate power. Insert a UNIBUS terminator (or equivalent) in connectors A and B of the last slot of the UNIBUS backplane. (If there is more than one UNIBUS backplane, insert the terminator in the last slot of the last UNIBUS backplane.) Connect the UNIBUS backplane to MICROVERTER with a standard UNIBUS cable, utilizing the first UNIBUS connectors in the UNIBUS backplane and the connectors at the top of the MICROVERTER board. The resulting configuration is shown in Figure 5-2 (UNIBUS controllers, etc., are not shown).

STEP 12. Verify that all 18-bit DMA devices are installed on the UNIBUS.

5.9 VERIFICATION

The system is now ready to be exercised under DEC X/11, using the "E" monitor. The KWA module can be used to exercise the Line Time Clock.

Use appropriate diagnostics to verify correct installation.

If the system does not operate correctly, go back to Step 1 of the installation procedure and verify that the entire procedure was completed correctly.

If the system still does not operate correctly, consult Appendix D, which contains installation troubleshooting procedures.

If these measures fail to result in correct system operation, call the ABLE Support Service department (see Chapter 7 for details).

5.10 LSI-11/73 Processor

This procedure applies to the installation of MICROVERTER BD in a system containing an LSI-11/73 processor.

STEP 1. Set MICROVERTER switches

Set switch S1 as shown below (set switches S1-3, S1-8, and S1-9 closed). Switch S1-6 can optionally be set closed to enable the Map Enable signal to be set by software. Set switch S1-10 open, to disable the LTC.

MAP ENABLE	SWITCH S1 1	2	3	4	5	6	7	8	9	10
Hardware	-	-	C	-	-	-	-	C	C	-
Software	-	-	C	-	-	C	C	C	-	-

"C" = CLOSED (ON), "-" = OPEN (OFF)

STEP 2. Configure MICROVERTER for memory resident on the UNIBUS (optional).

If the application requires the use of memory resident on the UNIBUS, consult Appendix C for the procedure.

STEP 3. Modify processor board.

The Map Enable signal and the ALE Timing Strobe signal have their sources on this processor board but are not available to the MICROVERTER board.

The processor cable is supplied with MICROVERTER BD for the purpose of bringing these signals to the MICROVERTER board. Two procedures are given here. The first procedure, using the cable as supplied, with two leads attached, is suitable for initial installation and product verification. The second procedure, in which the leads are cut off and the wires are soldered to the board, is recommended for permanent installation.

Interim Procedure

The processor cable has two color-coded leads, one red and one black.

a. Connect the black clip to pin 12 of IC 39, as shown in Figure 5-4.

b. Connect the red clip to pin 19 of IC 36, as shown in Figure 5-4.

Make the connections very carefully, to avoid short-circuiting to adjacent pins and also to avoid damaging the delicate clips.

> ABLE does not recommend the use of these leads on a long-term basis because of the possibility of intermittent errors.

Permanent Installation

a. Label or mark the wire carrying the red lead.

b. Cut the "red lead" wire to make it an inch or two shorter than the "black lead" wire.

c. Solder the shorter wire to pin 19 of IC 36, as shown in Figure 5-5.

d. Solder the other wire to pin 12 of IC 39, as shown in Figure 5-5.

e. Provide strain-relief for the cable: run the plastic tie wrap (supplied with the cable) through the left edge handle eyelet on the processor board and then around the cable. Make the wrap snug around the cable, but do not overtighten and damage the cable.

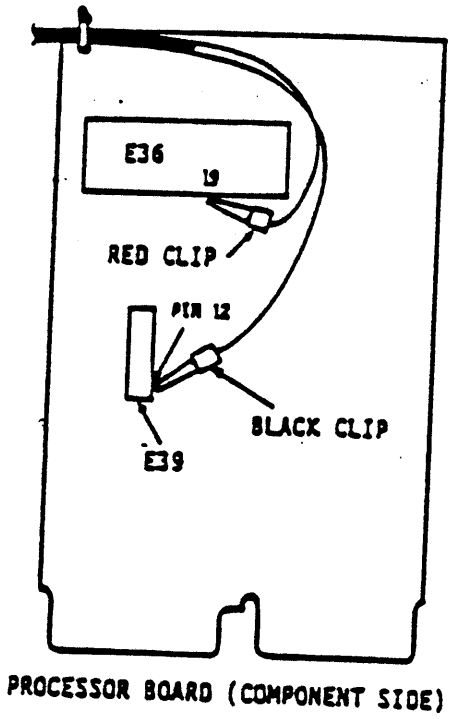

Figure 5-4: LSI-11/73 Processor Board
Temporary Modification

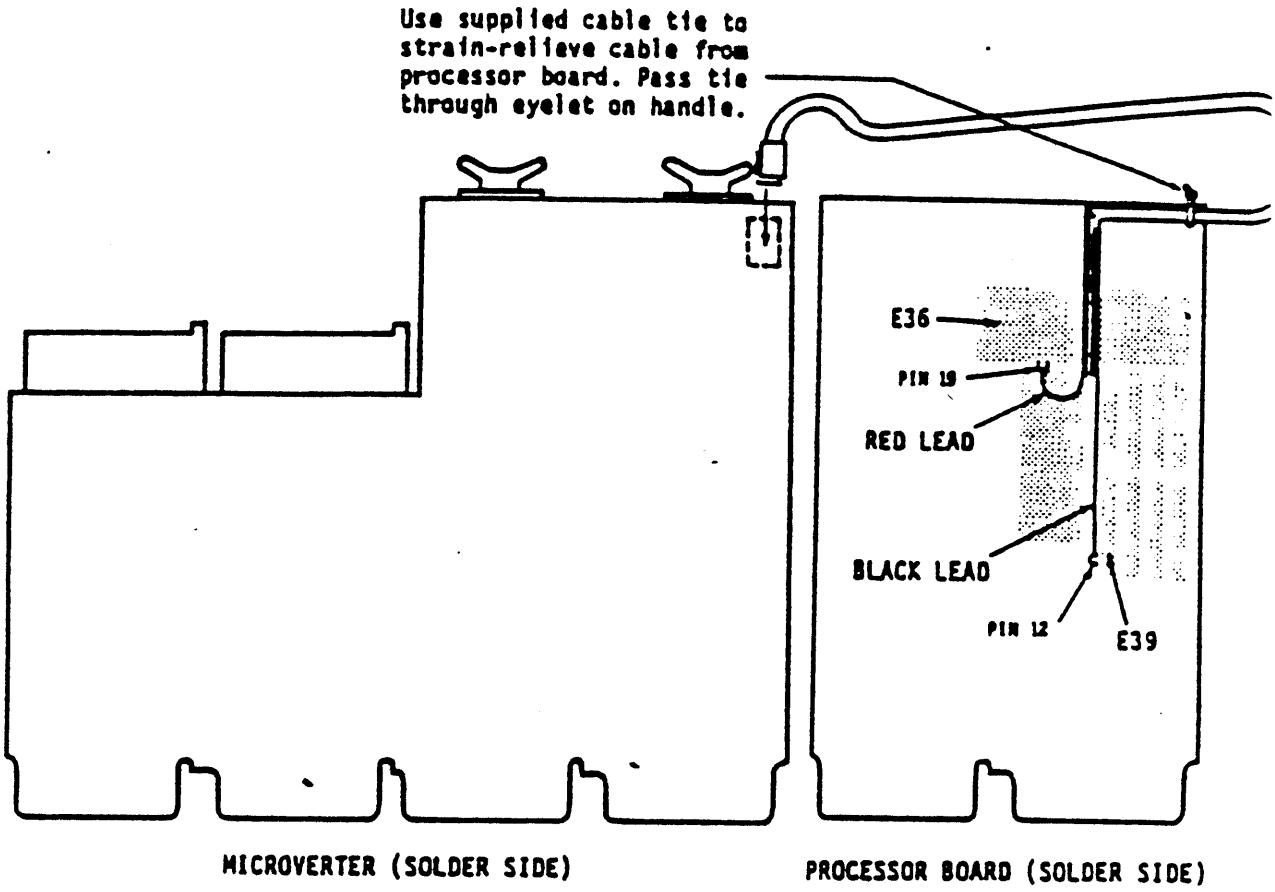

Figure 5-5: LSI-11/73 Processor Board
Permanent Modification

STEP 4. Modify backplane

a. MICROVERTER can receive the Map Enable signal on pin AH1 or pin BH1. Add a wire on the backplane from pin AR2 of the processor slot to pin AH1 or pin BH1 of the MICROVERTER board slot. (Switches S1-1 and S1-2 must be set appropriately: see above.)

b. Determine whether the backplane supports 22-bit addressing. If it does not, it must be modified. See Appendix A for a backplane modification procedure.

STEP 5. Insert MICROVERTER in Backplane

Insert the MICROVERTER board into any quad-slot of the backplane. If the hardware Map Enable option has been selected (via switch S1), plug the LSI-11/73 processor cable into the 4-pin socket on the MICROVERTER board. If the software-settable Map Enable function is selected, do not plug the processor cable into the MICROVERTER board.

STEP 6. Verify bus grant continuity.

Verify that each slot between the MICROVERTER and the processor contains either a module or a Q-Bus grant card. If grant cards are not available, position the boards so that there are no empty slots between boards.

STEP 7. Verify that boards are in correct priority order.

MICROVERTER follows the position-independent priority rules of the Q-Bus. LSI-11 I/O interfaces can be located either ahead of or behind the MICROVERTER. Devices located behind MICROVERTER have a lower priority than UNIBUS devices of the same level attached to the MICROVERTER. Refer to the DEC Microcomputers and Memories Handbook for further information on the Q-Bus.

STEP 8. Install UNIBUS peripheral controllers.

Insert UNIBUS controller boards in a UNIBUS backplane which is supplied with the appropriate power. Insert a UNIBUS terminator (or equivalent) in connectors A and B of the last slot of the UNIBUS backplane. (If there is more than one UNIBUS backplane, insert the terminator in the last slot of the last UNIBUS backplane.) Connect the UNIBUS backplane to MICROVERTER with a standard UNIBUS cable, utilizing the first UNIBUS connectors in the UNIBUS backplane and the connectors at the top of the MICROVERTER board. The resulting configuration is shown in Figure 5-2. (UNIBUS controllers, etc., are not shown).

STEP 9. Verify that all 18-bit DMA devices are installed on the UNIBUS.

5.11 VERIFICATION

The system is now ready to be exercised under DEC X/11, using the "E" monitor. The KWA module can be used to exercise the Line Time Clock.

Use appropriate diagnostics to verify correct installation.

If the system does not operate correctly, go back to Step 1 of the installation procedure and verify that the entire procedure was completed correctly.

If the system still does not operate correctly, consult Appendix D, which contains installation troubleshooting procedures.

If these measures fail to result in correct system operation, call the ABLE Support Service department (see Chapter 7 for details).

CHAPTER 6

PROGRAMMING

6.1 GENERAL

ABLE MICROVERTER Series products are compatible with DEC operating systems without additional programming. If it is desired to write special interface software, the information in this chapter is required. In this chapter, the term MICROVERTER refers to any of the MICROVERTER Series.

MICROVERTER is software transparent to the host computer. MICROVERTER is designed to operate with a single computer performing bus arbitration, and is not intended to be used as an interprocessor coupler.

Because MICROVERTER is software transparent to the host computer, diagnostics appropriate for devices being connected through MICROVERTER to the system can be used to verify system operation. Certain device or memory diagnostics may not be completely computer independent. Consult the diagnostic listing for applicable devices and processors.

NOTE

A KEY CONSIDERATION IS TO ENSURE THAT ADDRESS ASSIGNMENTS OF DEVICES ON THE UNIBUS AND Q-BUS DO NOT CONFLICT.

6.2 I/O MAP REGISTERS

The 32 I/O map registers provide direct memory access (DMA) address offset. Each I/O map register is a 22-bit, 2-word register. The low order word contains the 16 least significant bits (15-0) and the high order word contains the 6 most significant bits (21-16). The contents of these registers are user-programmable under software control.

DMA address offset is accomplished as follows:

* The upper five bits (17-13) of the DMA virtual address select one of 32 I/O map registers. If this address is inside the limit switches, the cycle is passed to the Q-Bus.

* Bits 12-1 of the DMA virtual address are added to bits 21-1 of the I/O map register and the sum is placed in bits 21-1 of the physical address.

* Bit 0 of the DMA virtual address is placed directly into bit 0 of the physical address.

Figure 6-1 illustrates the DMA memory offset. Table 6-1 provides addressing information for the map registers.

Map Number	Physical Address Low Word	Physical Address High Word	DMA Virtual Address
0	17770200	17770202	00XXXX
1	17770204	17770206	02XXXX
2	17770210	17770212	04XXXX
3	17770214	17770216	06XXXX
4	17770220	17770222	10XXXX
5	17770224	17770226	12XXXX
6	17770230	17770232	14XXXX
7	17770234	17770236	16XXXX
10	17770240	17770242	20XXXX
11	17770244	17770246	22XXXX
12	17770250	17770252	24XXXX
13	17770254	17770256	26XXXX
14	17770260	17770262	30XXXX
15	17770262	17770264	32XXXX
16	17770270	17770272	34XXXX
17	17770274	17770276	36XXXX
20	17770300	17770302	40XXXX
21	17770304	17770306	42XXXX
22	17770310	17770312	44XXXX
23	17770314	17770316	46XXXX
24	17770320	17770322	50XXXX
25	17770324	17770326	52XXXX
26	17770330	17770332	54XXXX
27	17770334	17770336	56XXXX
30	17770340	17770342	60XXXX
31	17770344	17770346	62XXXX
32	17770350	17770352	64XXXX
33	17770354	17770356	66XXXX
34	17770360	17770362	70XXXX
35	17770364	17770366	72XXXX
36	17770370	17770372	74XXXX
37*	17770374	17770376	76XXXX

*When DMA virtual address is within I/O range 76XXXX, relocation is disabled and I/O address is placed directly onto Q bus with signal BBS7 (Bank Select 7) also asserted.

Figure 6-1: DMA Memory Offset

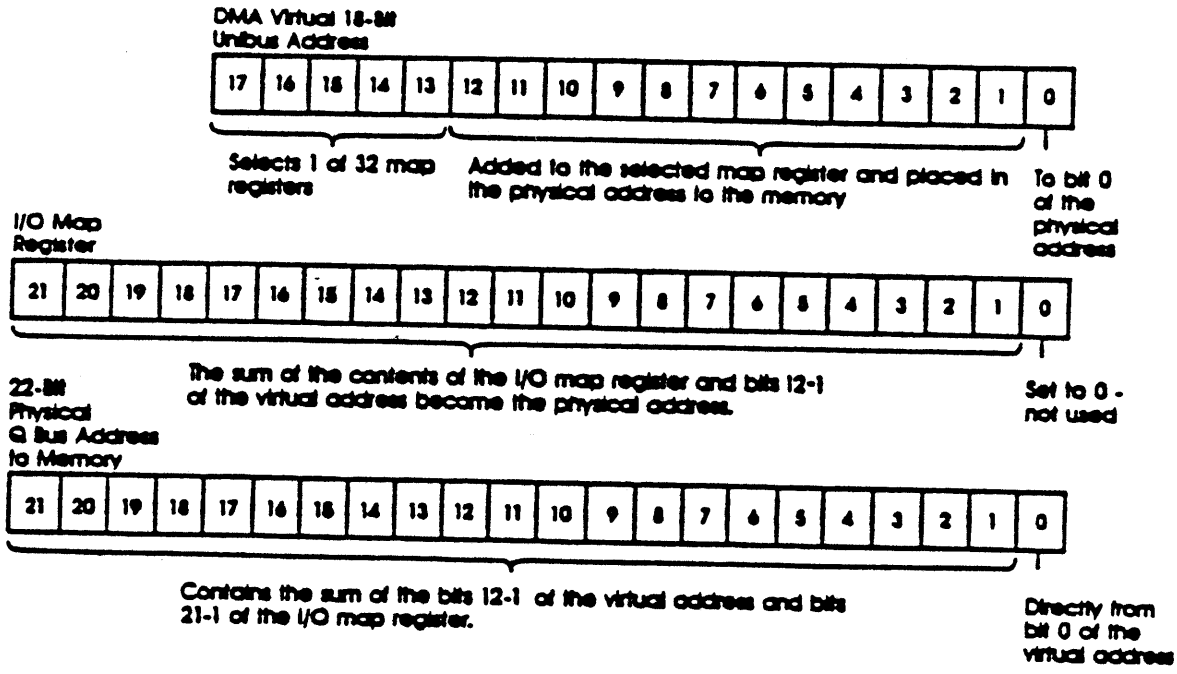

Table 6-1: I/O Map Register Addressing

6.3 MAPPING

Status Register 3 (SR3) is used to enable 22-bit mapping and I/O mapping. Bit 4, when set, enables 22-bit addressing. Bit 5, when set, causes the MICROVERTER to map I/O transfers. Status Register 3 is shown in Figure 6-2.

Status Register 3 is physically located on the LSI-11/23, LSI-11/23+, and LSI-11/73 processors at address 772516.

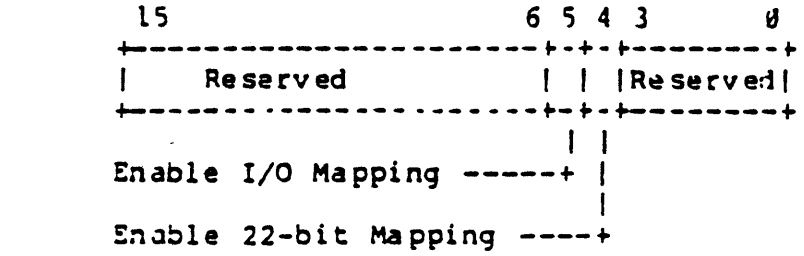

Figure 6-2: Status Register 3

6.4 SOFTWARE MAP ENABLE

Software Map Enable functions as follows:

1. Execution of the first write instruction to any MICROVERTER mapping register sets the Map Enable.

2. The Map remains enabled until either a Bus Init instruction is executed or system power is cycled.

.5 LINE CLOCK STATUS REGISTER

The MICROVERTER line clock status register, at location 17777546, controls the line time clock for the LSI-11/23 only. (The LSI-11/23+ and LSI-11/73 processors have their own clock status registers.) Format of the MICROVERTER line clock status register is as follows (see also Figure 6-3):

Bit	Description
15-08	Not used.
07	Monitor. This read/write 0 only bit is set by the clock and cleared by the program.
06	Interrupt Enable. When this read/write bit is set, the clock generates an interrupt at PR6 through location 100 (octal).
05	This read/write bit is reserved for ABLE use. It must be set to 0 for normal operation.
04-00	Not used.

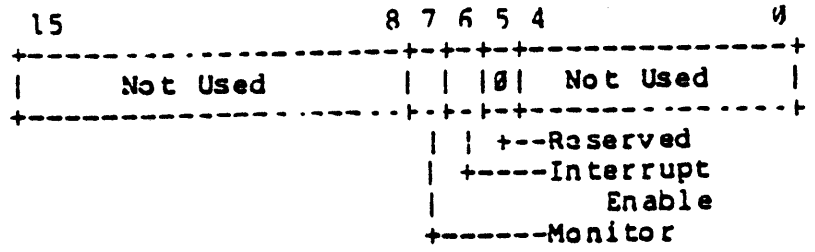

Figure 6-3: MICROVERTER Line Clock Status Register

CHAPTER 7

SERVICE AND SUPPORT

7.1 SERVICE

ABLE products are designed to provide years of service with a minimum of care. ABLE recommends the following procedures for trouble-free operation:

* If a printed circuit board is frequently inserted and removed, it tends to build up a gum-like residue on the contacts. Clean this off using a cotton swab and alcohol or freon.

* Every six months, remove each printed circuit board and clean off accumulated dust. Dust can impede air flow. While the board is out, inspect it for evidence of a potential problem such as damaged components, loose connections, etc.

ABLE's goal is to provide each customer with a product that works well in the customer's system. We design and build our products to provide high reliability and to minimize problems. When a problem does arise, it is our intent to do everything in our power to solve it quickly and efficiently. If a problem arises with the operation of your MICROVERTER Series product, proceed as described below.

7.2 FOR SERVICE WITHIN THE UNITED STATES

If your MICROVERTER Series product does not function properly and you are within the United States, contact our Product Support Center before sending it for repair. Have serial numbers available when calling.

ABLE Computer
3080 Airway Avenue
Costa Mesa, California 92626
(714) 979-7030
TWX 910-595-1729

If your product requires repair, it should be returned to the factory. Use the original containers or a corrugated cardboard carton with at least one inch of cushioning material on all sides. Include a description of the problem and a hard copy of the failure mode or diagnostic printout when available. Be sure to include your name, address, and telephone number. Ship it to the above address.

7.3 FOR SERVICE OUTSIDE THE UNITED STATES

If your MICROVERTER Series product does not function correctly, contact your local distributor or telex ABLE Computer for the name and address of your local distributor:

TWX 910-595-1729

In Europe, telex our London office at:

Telex 848715 ABLE G

APPENDIX A

BACKPLANE MODIFICATION

This appendix contains directions for modifying a backplane for 22-bit addressing on the Q-Bus.

ADDRESSING

22-bit addressing on the Q-Bus is provided only by the DEC H9275-A backplane. Other backplanes do not provide for 22-bit addressing.

To use backplanes other than the H9275-A, the user must bus the upper address lines onto all Q-Bus slots. They are found on the following pins:

BUS-DAL18-L	BC1, DC1
BUS-DAL19-L	BD1, DD1
BUS-DAL20-L	BE1, DE1
BUS-DAL21-L	BF1, DF2

NOTE

Add address wires to connector D only if Q-Bus signals are present on connectors C and D.

APPENDIX B

PATCHES FOR RSTS/E V7.0 or V7.1

This appendix contains directions for patching RSTS/E V7.0 or V7.1 to run with 22-bit parity memories.

.NIT V7.0 does not initialize all memory when run on a 22-bit system. This may cause problems with RSTS after a power-up due to random data and parity left in memory. The following patches allow INIT to correct all parity bits.

V7.0 PATCHES

```
OPTION:  PATCH INIT.SYS
BASE ADDRESS?  DEFAULT
OFFSET ADDRESS?  4602
  BASE OFFSET  OLD     NEW?
XXXXXX 004602  012701?  401
XXXXXX 004604  000002?  ^C

OPTION:
```

V7.1 PATCHES

```
OPTION:  PATCH INIT.SYS
BASE ADDRESS?  DEFAULT
OFFSET ADDRESS?  4760
  BASE OFFSET  OLD     NEW?
XXXXXX 004760  012701?  401
XXXXXX 004762  000002?  ^Z

OPTION:
```

NOTE: ^C represents CTRL C
^Z represents CTRL Z

APPENDIX C

UNIBUS MEMORY

This appendix contains directions for use of the "window" feature of MICROVERTER, which allows the use of 8K of memory resident on the UNIBUS.

If the application requires memory resident on the UNIBUS, set the UNIBUS memory lower and upper address limits via "E" points E1 through E20 on the MICROVERTER board. The MICROVERTER board is shown in Figure 3-2. (The "window" feature of MICROVERTER allows the use of 8K of UNIBUS memory. This area of memory is excluded from address translation by MICROVERTER.) Two groups of jumpers which specify the UNIBUS lower and upper address limits are used to exclude these addresses from mapping. Each group consists of five jumpers which allow limits to be set in 8K-byte increments.

Lower I/O Map Limits

Set the lower UNIBUS address using points E1 through E5 and E16 through E20. Table C-1 lists jumper configurations corresponding to UNIBUS addresses 0 through 248K bytes. Note that the factory setting is 248K bytes.

Upper I/O Map Limits

Set the upper UNIBUS address using points E6 through E15. Table C-2 lists jumper configurations corresponding to UNIBUS addresses 8K bytes through 248K bytes. Note that the factory setting is 248K bytes.

UNIBUS Memory Start Address, KB	E20 to E1	E19 to E2	E18 to E3	E17 to E4	E16 to E5
0	I	I	I	I	I
8	I	I	I	I	-
16	I	I	I	-	I
24	I	I	I	-	-
32	I	I	-	I	I
40	I	I	-	I	-
48	I	I	-	-	I
56	I	I	-	-	-
64	I	-	I	I	I
72	I	-	I	I	-
80	I	-	I	-	I
88	I	-	I	-	-
96	I	-	-	I	I
104	I	-	-	I	-
112	I	-	-	-	I
120	I	-	-	-	-
128	-	I	I	I	I
136	-	I	I	I	-
144	-	I	I	-	I
152	-	I	I	-	-
160	-	I	-	I	I
168	-	I	-	I	-
176	-	I	-	-	I
184	-	I	-	-	-
192	-	-	I	I	I
200	-	-	I	I	-
208	-	-	I	-	I
216	-	-	I	-	-
224	-	-	-	I	I
232	-	-	-	I	-
240	-	-	-	-	I
248 *	-	-	-	-	-

"I" = Jumper Installed; "-" = Jumper Removed
* = Factory Setting

Table C-1: I/O Map Lower Limit Jumper Settings

UNIBUS Memory End Address, KB	E15 to E6	E14 to E7	E13 to E8	E12 to E9	E11 to E10
8	I	I	I	I	I
16	I	I	I	I	-
24	I	I	I	-	I
32	I	I	I	-	-
40	I	I	-	I	I
48	I	I	-	I	-
56	I	I	-	-	I
64	I	I	-	-	-
72	I	-	I	I	I
80	I	-	I	I	-
88	I	-	I	-	I
96	I	-	I	-	-
104	I	-	-	I	I
112	I	-	-	I	-
120	I	-	-	-	I
128	I	-	-	-	-
136	-	I	I	I	I
144	-	I	I	I	-
152	-	I	I	-	I
160	-	I	I	-	-
168	-	I	-	I	I
176	-	I	-	I	-
184	-	I	-	-	I
192	-	I	-	-	-
200	-	-	I	I	I
208	-	-	I	I	-
216	-	-	I	-	I
224	-	-	I	-	-
232	-	-	-	I	I
240	-	-	-	I	-
248 *	-	-	-	-	I

"I" = Jumper Installed; "-" = Jumper Removed
* = Factory Setting

Table C-2: I/O Map Upper Limit Jumper Settings

APPENDIX D

INSTALLATION TROUBLESHOOTING

This appendix contains directions for troubleshooting a MICROVERTER installation.

TROUBLESHOOTING

If the system does not operate correctly when a MICROVERTER Series product 73 is installed, first perform a check of the installation procedure. If, after performing this check and correcting any errors found, the system still does not operate correctly, the problem may be due to a steal grant circuit in a controller. This circuit appears in many DEC controller designs and requires a simple modification for successful MICROVERTER operation.

The steal grant circuit causes an interrupt cycle to be aborted in favor of a pending non-processor request (NPR) cycle to improve DMA latency. This is normally transparent in UNIBUS processors, but is not in Q-Bus processors. Once an interrupt cycle is started on a Q-Bus processor, it must be completed or it will cause the processor to go through a request timeout (approximately 15 microseconds). These request timeouts accumulate and result in Data Late errors.

The DEC M7821 uses a typical steal grant circuit, partially shown in Figure D-1. Jumper N1 can be removed, causing the second input of the 8640 to be pulled up and thus disabled. In some controllers, this second input is hardwired to ground; in this case, it is necessary to lift the IC pin and jumper it to a pullup resistor. If a pullup resistor is not readily available, one may have to be added. A 4.7K ohm, 0.25 watt pullup resistor is recommended.

DEC normally provides a jumper option for enabling or disabling this circuit. Some