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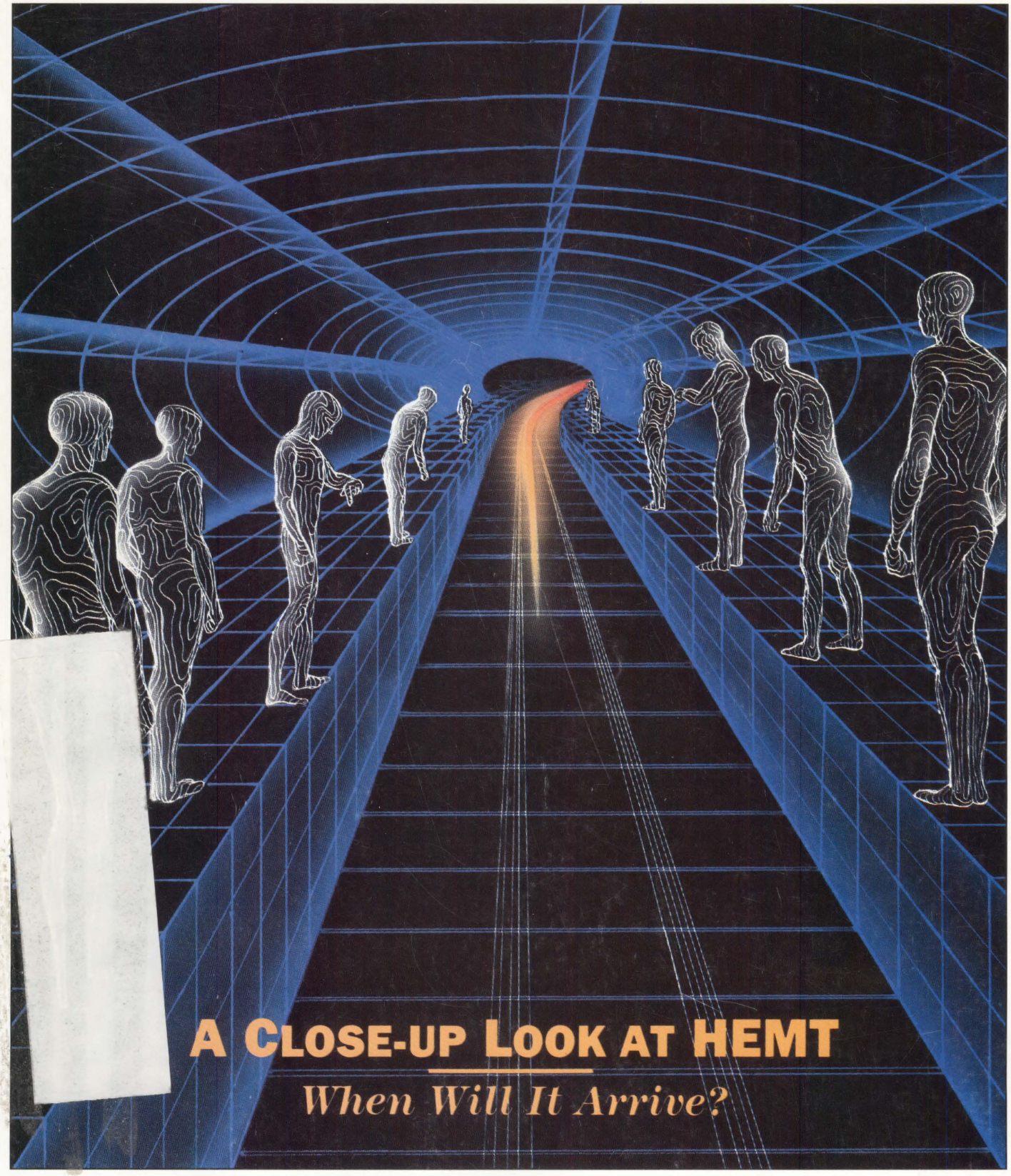
VLSI Systems Design

FOR DESIGNERS OF HIGH-PERFORMANCE SYSTEMS



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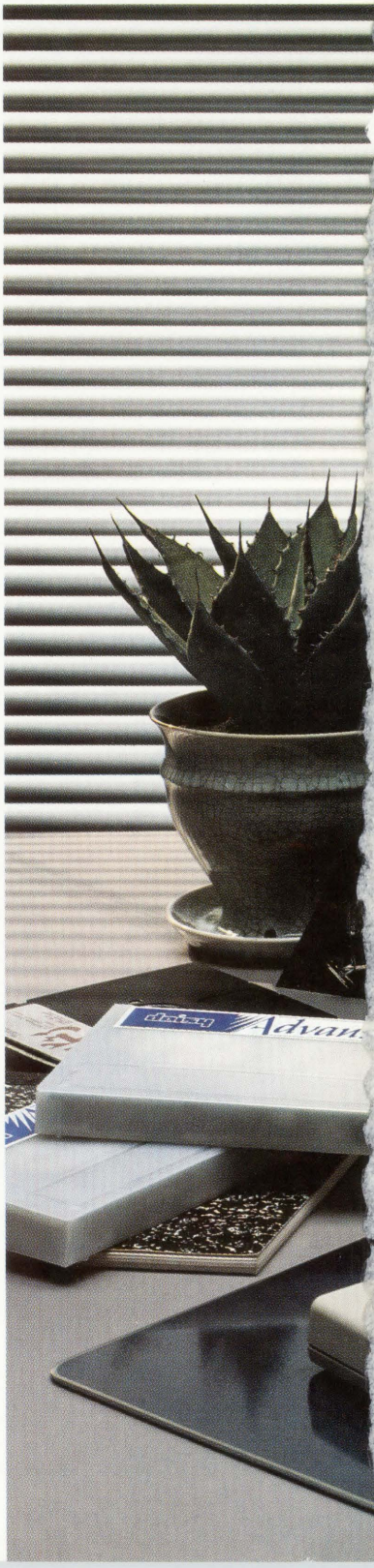

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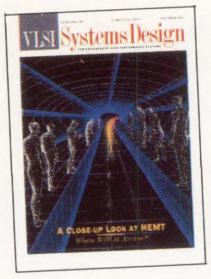

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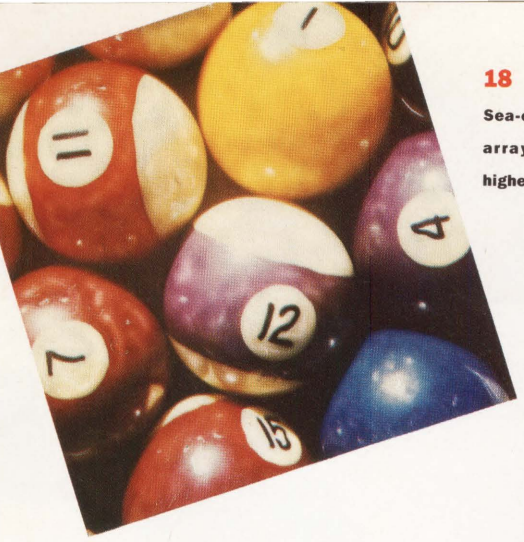

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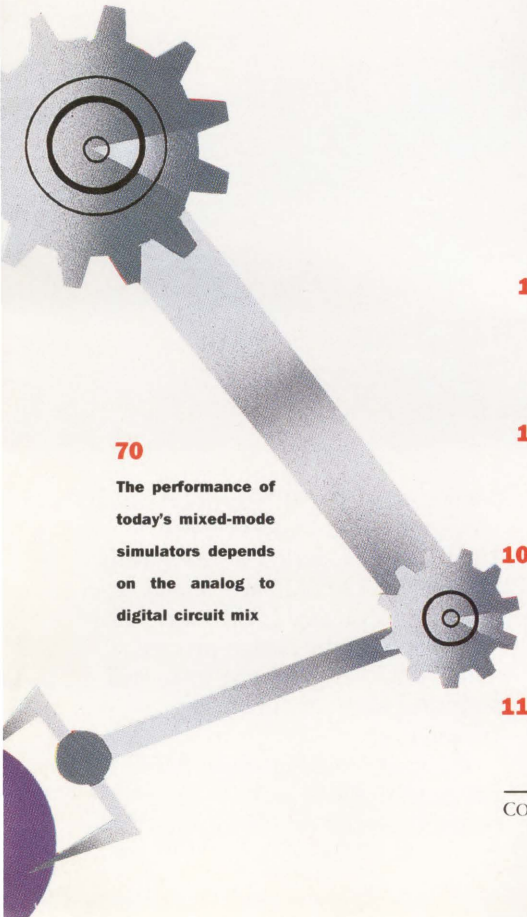

COVER ILLUSTRATION BY CAROL GILLOT

VLSI Systems Design

FOR DESIGNERS OF HIGH PERFORMANCE SYSTEMS

A CMP Publication

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CIRCLE NUMBER 2

VLSI: The Challenge to Innovate

With VLSI technology and foresight, the impractical can soon become the practical

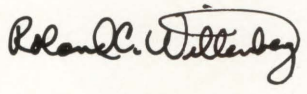
An article that appeared in our October 1988 issue, *A VLSI Join Module,* made me realize how many ideas that were formerly impossible (or more appropriately, impractical) had suddenly become practical as a result of the rapidly growing ability of VLSI technology to provide massive and complex functions on reasonably sized chips at *relatively* low cost.

This particular article described an architecture—implemented in VLSI—for speeding up searches in large databases. With traditional von Neumann architectures, words in a database are addressed and brought into a single central ALU, one at a time. The serial search is time consuming. Of course, performing the comparisons in parallel, would really accelerate the operation. But this "highly impractical" idea would require a separate ALU at every bit position in the memory.

Professor Ali Hurson and graduate student Charles Petrie at Pennsylvania State University took on this challenge. They combined VLSI technology and massive parallelism to provide a new solution to the problem. They've already designed the first chips (which IBM fabricated) and proved the validity of their circuits and algorithms. An improved version (to be fabricated by NCR) is also in the works.

Another example happened a few years ago. Howard Sachs of Fairchild Semiconductor foresaw that VLSI technology would allow him to build chips incorporating a number of performance boosting supercomputer techniques. The result was a breakthrough in microprocessor performance—the 5-Mips Clipper, now produced by Intergraph Corp.

There are many other examples of technologists, in all fields of endeavor, who have had the foresight to leverage a new technology to overcome the roadblocks that rendered a great idea impossible or impractical. VLSI is one of today's most challenging technologies. It challenges the foresighted technologist to dust off and re-examine all those great ideas that were abandoned for reasons such as "it's not practical; it would be too big, too slow, or too costly to implement." So let's ignore the roadblocks and accept the challenge of VLSI—and begin innovating new architectures, new systems, and new products.



ROLAND WITTENBERG
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Calendar

2ND INTERNATIONAL WORKSHOP ON VLSI DESIGN

December 15–18
Bangalore, India

This year's workshop will be held in Bangalore, which is also known as the "Silicon Valley" of India. It will feature tutorials and panel discussions, as well as technical presentations. Topics will include design rule checking, layout and routing, testing and test program generation, design database, CAE/CAD systems, workstations, test vector generation, implementation algorithms, logic and circuit simulation, timing analysis and verification, silicon compilation, expert system applications, fault modeling, and fault simulation. Additional information may be obtained by contacting Dr. Ravi M. Apte, Valid Logic Systems Inc., M/S 01, 2820 Orchard Pkwy., San Jose, Calif. 95134. (408) 432-9400. ■

IEEE INTERNATIONAL CONFERENCE ON WAFER-SCALE INTEGRATION

January 3-5, 1989
Fairmont Hotel
San Francisco, Calif.

This conference will present a balanced program of all the aspects of monolithic wafer-scale integration, including theory, technology, applications, and products. The program will feature contributed papers, poster presentations, and panel discussions and will cover topics such as WSI reliability, yield modeling, wafer-scale CAD systems, packaging, power/ground distribution, signal and image processors, and wafer-scale memory. For further information, contact Patty Patterson, TRW Defense Systems Group, 1 Space Park (R2/2076), Redondo Beach, Calif. 90278. (213) 812-0788. ■

1989 IEEE VLSI TEST WORKSHOP

April 11–13, 1989
Bally's Park Place
Casino Hotel
Atlantic City, N.J.

The purpose of this workshop is to discuss and explore current test concepts and future trends in VLSI devices designed as microsystems. Papers are solicited on topics including LSSD, BIT, testability trade-offs, test equipment, simulation, knowledge-based systems, redundancy, logistics, fault tolerance, packaging, analog/digital, and tester architecture. Authors interested in making a presentation should submit, by November 25, 1988, a 100–200-word abstract to Mukund Modi, Program Chairman, Naval Air Engineering Center, ATE Software Center, Code: 52514, Lakehurst, N.J. 08733, (201) 323-2560. Additional information about the workshop may be obtained by contacting Wesley E. Radcliffe, Chairperson, IBM East Fishkill, Dept. 277, Bldg. 321-5E1, Hopewell Junction, N.Y. 12533. (914) 894-4346. ■

INTERNATIONAL TEST CONFERENCE 1989

August 29–31, 1989
The Sheraton Washington Hotel
Washington, D.C.

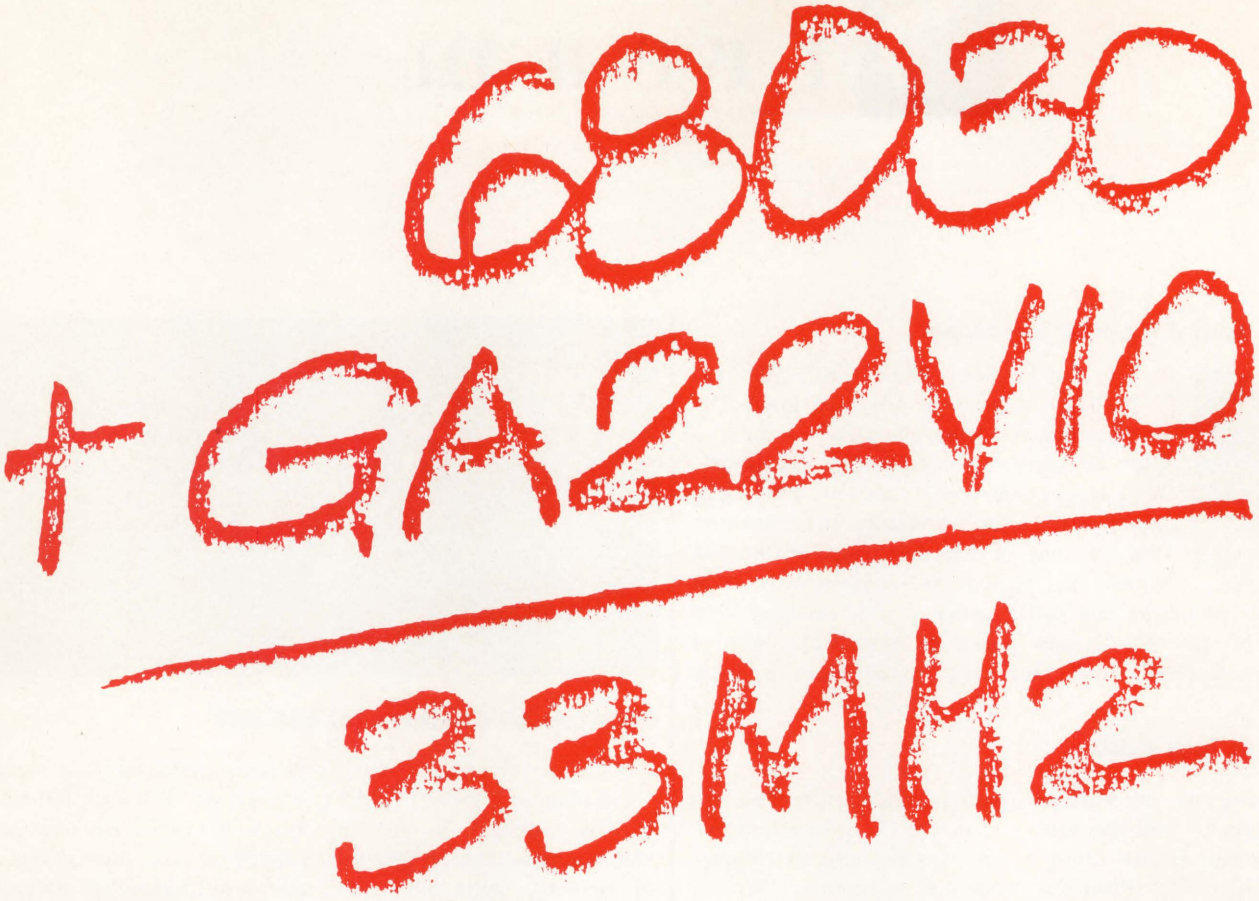
Sponsored by the IEEE's Computer Society and Philidelphia Section, the ITC provides a major forum for the exchange of information about the testing of electronic devices, assemblies, and systems. This year's conference focuses on innovative test techniques and equipment needed to meet the challenges of the future. Technical presentation topics will include built-in-self-test, computer-aided engineering, design for testability, design verification, fault modeling and simulation, memory devices, microcontrollers and microprocessors, printed circuit boards, surface mount assemblies, system test, wafer-scale assemblies, quality and reliability, standards, and test economics. Authors are invited to submit, by January 16, 1989, a 35-word abstract, and either a 500-word summary or a full manuscript to Ray Mercer, Program Chair, International Test Conference, Millbrook Plaza, Suite 104D, P.O. Box 264, Mount Freedom, N.J. 07970. For more details, call Doris Thomas, at (201) 895-5260. ■

INTERNATIONAL CONFERENCE ON SEMICONDUCTOR AND INTEGRATED CIRCUIT TECHNOLOGY

October 22–28, 1989
Beijing, China

Designed to provide an international forum on semiconductor and integrated circuit technology, this conference will cover such topics as amorphous silicon, bipolar technology, CAD, CMOS technology, dielectrics, electrical characterization, IC design, interconnect technology, multilevel interconnect, packaging, process characterization, rapid thermal processing, and reliability/yeild. By January 9, 1989, interested authors should submit a 300-word abstract detailing the work to be presented. To submit abstracts or to obtain additional information contact Linda Reid, Continuing Education in Engineering, University Extension, University of California, 2223 Fulton St., Berkeley, Calif. 94720. ■

ILLUSTRATION BY LORRAINE RAYWOOD



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AMD				
PAL22V10	15.0 ns	10.0 ns	10.0 ns	50 MHz
PAL16R8	7.5 ns	7.0 ns	6.5 ns	74 MHz
TEXAS INSTRUMENTS				
TIBPAL22VP10	20.0 ns	20.0 ns	12.0 ns	37 MHz
CYPRESS SEMICONDUCTOR				
PALC22V10	25.0 ns	15.0 ns	15.0 ns	33 MHz

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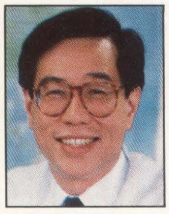
CIRCLE NUMBER 4

BIT Stream

Lattice Bags AMD PLD Executive



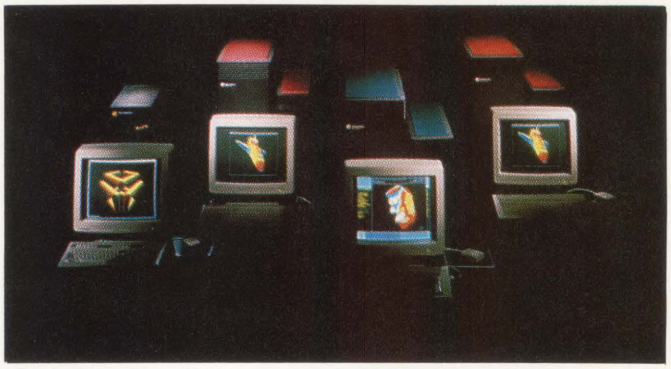
CYRUS TSUI

Cyrus Tsui has jumped from the Programmable Logic division of Advanced Micro Devices Inc. to assume the president and CEO posts at Lattice Semiconductor (Hillsboro, Ore.). "Ray bagged me," says Tsui, refering to Ray Capice, Lattice's executive vice president. Tsui was one of the developers of the PAL process, and moved up to executive posts at Monolithic Memories and AMD. Lattice, which emerged from Chapter 11 this year, is now poised to move from "tens of millions to hundreds of millions in sales," according to Capice. ■

DEC Buys into RISC

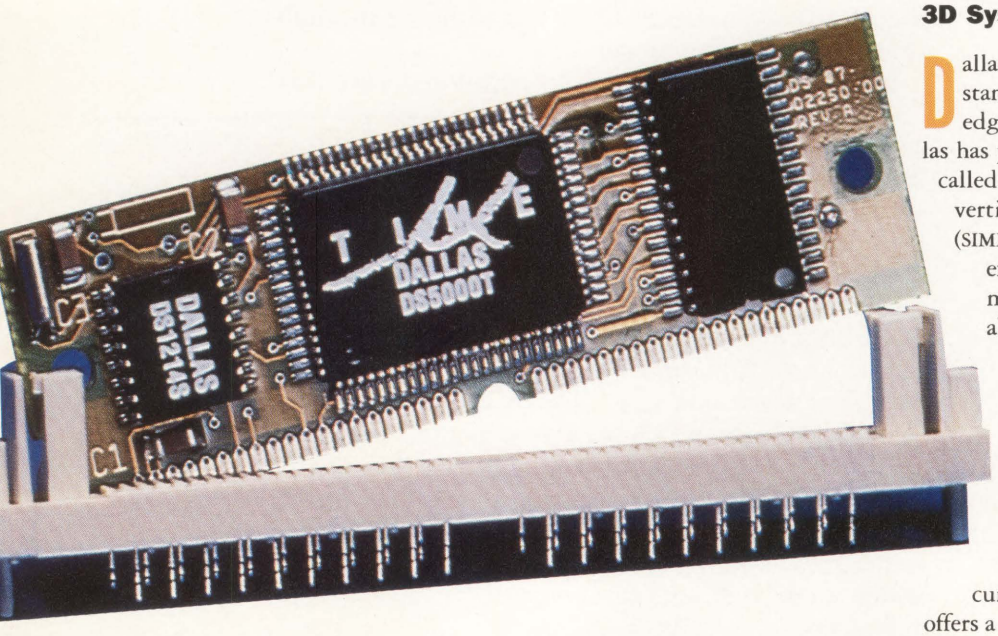
Eschewing its homegrown attempts to join the RISC movement, Digital Equipment Corporation (Maynard, Mass.) has signed a technology exchange agreement with MIPS Computer Systems Inc. (Sunnyvale, Calif.) to gain access to the MIPS' RISC technology and designs.

Digital's MicroVAX workstations have been hard pressed to match the integer-processing specifications of competing RISC platforms. "We intend to develop high-performance systems, for the desktop and upwards, which utilize RISC," explains Robert Palmer, Digital's vice president and group manager of Semiconductor Operations. ■



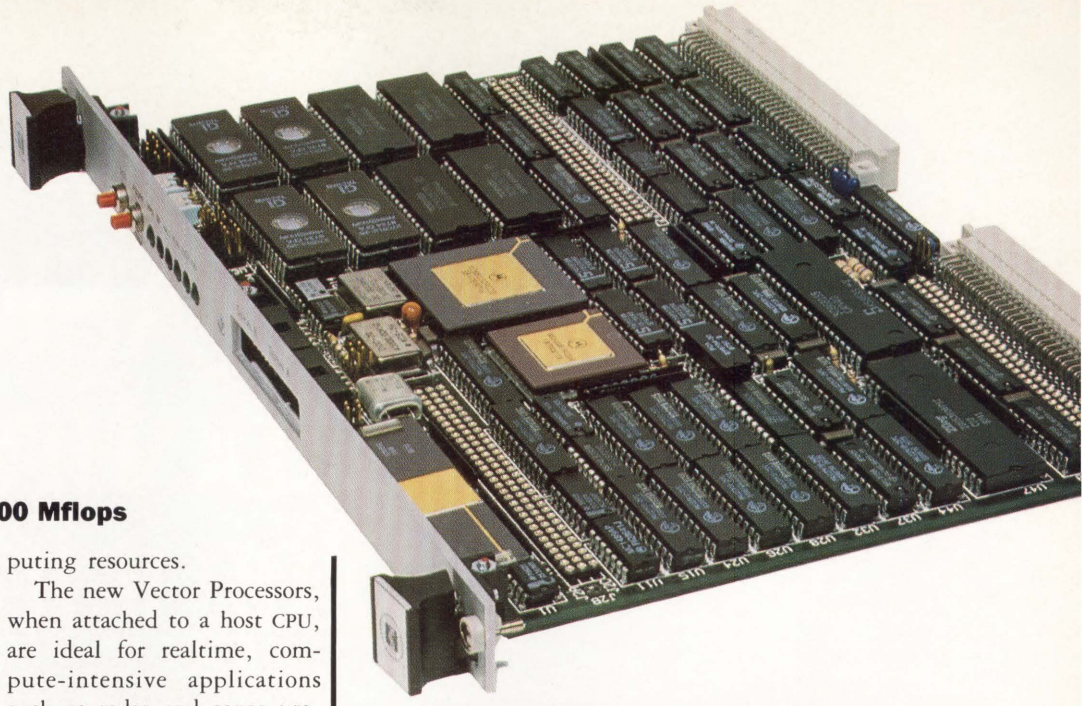
Desktop 3D Graphics for $16,000

Silicon Graphics Inc. (Mountain View, Calif.) has wrapped a 10-MIPS RISC microprocessor, 8-Mbytes of memory, eight color bitplanes, a 19-inch color monitor and its Geometry Engines into a workstation priced at $15,990. The Personal IRIS comes with a new user interface called IRIS WorkSpace, supports the Network Filing Systems, and runs all software written for IRIS workstations. Silicon Graphics has also expanded upward, introducing a line of multiprocessor systems that also run IRIS software. Called the POWER Series, they use as many as four 32-bit R3000 processors from MIPS Computer Systems, offering up to 80 Mips and 16 Mflops of computing resources. ■



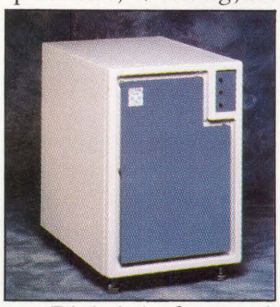
3D Systems Spring Up

Dallas Semiconductor (Dallas, Tex.) plans to stand board designs on their ends. Using new edge connectors developed by Amp Inc., Dallas has produced a series of plug-in subassemblies called SipStiks that extend board-level systems vertically. Like single in-line memory modules (SIMMs), SipStiks improve packing density by extending boards vertically from the system motherboard. Five SipStiks are now available: a nonvolatile 1-Mbit SRAM; a 16K X 9 FIFO; two microcontrollers with nonvolatile memory; and an ADPCM speech compression SipStik. Future releases include a modem, instrumentation, and a T1 line interface. SipSticks range from 2.5 to 3.5 inches long and are limited to a maximum height of 0.85 inches. They use CMOS integrated circuits to limit power dissipation. Dallas also offers a prototype mother board conforming to the Eurocard single-height standard. ■



A New Star Performs at 100 Mflops

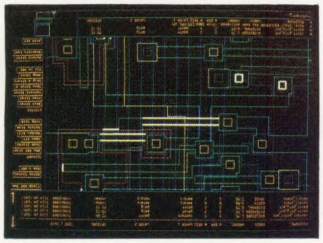
Star Technologies Inc. (Sterling, Va.) unveiled its new family of vector processors, the VP-1 and VP-2, that deliver 50 and 100 Mflop performance respectively. The new 32-bit CMOS processors, which were first shown at last month's Electronic Imaging-'88 conference, were designed to connect with a wide selection of host computers including those manufactured by IBM, Digital Equipment Corp., Concurrent, Gould, Sun Microsystems, and Alliant Computer Systems. Both the VP-1 and VP-2 can be simultaneously attached to up to three dissimilar host computers as shared computing resources.



The new Vector Processors, when attached to a host CPU, are ideal for realtime, compute-intensive applications such as radar and sonar processing, satellite imaging, and seismic data processing.

The VP-1 processor incorporates a single compute head, and is field-upgradeable to the dual-headed VP-2 with the addition of a second compute head. For those applications requiring even more power, up to three VP-2 systems can be stacked and directly interconnected to deliver up to 300 Mflops of computing power in a single 19 x 72 inch EIA rack. ■

Interactive Chip Debugging



Debugging the results from design-rule-check (DRC) software typically means wading through lists of design errors with cryptic location identifiers. Mentor Graphics Corp. (Beaverton, Ore.) has updated its IC layout tools to make this process graphical and interactive. Mentor's REMEDI software works within its ChipGraph system to perform dimensional checks on one or two mask layers interactively. The software can be directed to check only certain cells or a specific geometric section of the layout. It can check all geometric angles of the layout objects and can verify CMOS, BiMOS, Bipolar and GaAs fabrication technologies.

Violations are highlighted and can be corrected without leaving the layout environment. Also, multiple design rules can be applied in any single pass on the design. This debugging capability is enhanced by a two times improvement in the graphics performance of the ChipGraph layout editor. The REMEDI software package is priced at $14,900 through December. ■

No Waiting for VME Board's 1-Megabyte Memory

General Micro Systems Inc.'s (Montclair, Calif.) latest entry in the 32-bit VMEbus CPU board arena is its 68030-based GMSV17 that provides up to 1-Mbyte of on-board zero-wait-state, dual-ported SRAM. The new board uses Motorola's 33 MHz microprocessor together with the MMU and a 68882 floating point coprocessor. Also available are "mezzanine" modules that can provide an additional 1-Mbyte of dual-ported SRAM or four to 16 Mbytes of dual-ported DRAM on a local bus. This expanded-memory module still requires only a single VME slot. The GMSV17 is priced from $2,096 in 100 piece quantities. ■

Spectrum Speeds Analog Analysis

A third generation personal computer based software package for the analysis of analog circuits was recently rolled out by Spectrum Software (Sunnyvale, Calif.). Micro-Cap III is a window-based, interactive design and analysis system that features an integrated schematic editor and Spice-like analysis routines. Micro-Cap III can perform AC, DC, Fourier, and transient analysis on analog circuits directly from the schematic.

The new package performs both linear and non-linear analysis of components such as resistors, capacitors, inductors, bipolar and MOS transistors, and op amps. Mixed-mode simulation is also possible with the integrated switch models and macros. ■


Odds are 50-50
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By this simple, yet decisive measure, Mentor Graphics brings you unequaled design capability. While other EDA vendors scurry to produce their own ASIC libraries (with little guarantee of accuracy), more ASIC vendors put their libraries on Mentor Graphics workstations than any other. And in most cases, we're the first workstation supported, which means you have the first shot at exploiting new chip technologies.

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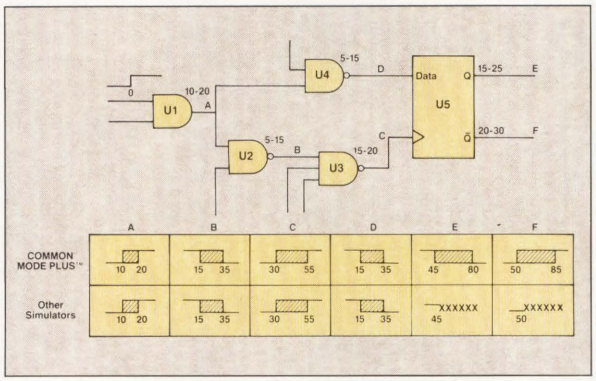
HHB's Henckels Likes To Be On The Cutting Edge

Lutz Henckels, president, CEO, and co-founder of HHB Systems Inc. (Mahwah, NJ), was born in Germany during World War II, and grew up in Solingen, a city on the Wupper River, east of Dusseldorf. Solingen gained fame when the craft of sword making was introduced there during the Middle Ages. But it also is well known for its worldwide reputation as a fine cutlery center, and as anyone knowledgable of fine cutlery might have guessed, the Henckels' family was heavily involved in cutlery. For over 250 years, they operated an internationally respected cutlery manufacturing business, J.A. Henckels Twin Works.

Lutz decided at an early age that he wanted to make his own mark in the world; he wanted to be at the cutting edge of technology. He did just that. He was one of the architects of the first commercially available digital simulator, CAPS, which was developed at GenRad Inc. (Concord, Mass.). CAPS was a cutting edge product targeted at the tester market. It brought a lot of attention to GenRad. "The product was enormously successful; we sold thousands of them," Henckels remarked.

He also remembers his first year in a university/industry cooperative engineering program in Berlin, when he had an opportunity to work for a few months at EG&G in Massachusetts. It was there that he heard about the great reputation that Massachusetts Institute of Technology enjoyed, particularly in the United States.

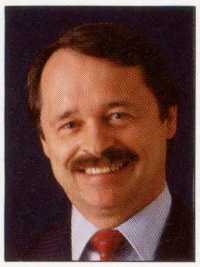


This prompted him to visit the school, where he applied for and was accepted in the electrical engineering program. "When I came here I only planned to stay for six months, but I ended up staying permanently," he added.

His years at MIT were very fruitful. He worked part time at GenRad while earning a BS and MS in Electrical Engineering and a Ph.D. in Computer Science. He also met his future partners, Rene Haas and Kenneth Brown, who were also attending MIT and working at GenRad on the CAPS simulator.

Since they first got together in 1971, Henckels, Haas and Brown, aka HHB, have been like the three musketeers. The great success of CAPS "gave us the confidence to leave GenRad and start our own business," said Henckels. However, as a result of the coverage that they received in the trade press when they left GenRad, they were swamped with job offers, some with equity benefits. "We were very young at that time and accepted an offer from Instrumentation Engineering in New Jersey that included two percent equity in the company. But, we soon realized that we wouldn't be able to accomplish our goals there.

'THE GREAT SUCCESS OF CAPS GAVE US THE



CONFIDENCE TO START OUR OWN BUSINESS'

However, we did stay two years until we finished a new simulator, called MicroSim. We left in 1977 to found HHB, and we've been here ever since," he added.

For the first five years, HHB was an profitable engineering services company developing simulators and automatic test program generation tools. But, after Haas and Henckels took the OMP course at Harvard University's Business School, they decided to become a product oriented company. The transition from a service oriented company to a product oriented one took two years, and of course, the first product out of the "new" organization was CADAT, an extremely successful simulator. Even today, the CADAT simulator together with the company's CATS hardware modeler accounts for more than half of HHB's business. Accelerators and automatic test generators also play a prominent part in the company's future. Recently, HHB's plans to broaden its base in the design automation arena have linked the company with several other design automation players.

When asked about the successful 17 year relationship that he has enjoyed with his two partners, Henckels comments, "We work together very hard, but when we're not working, we each go our own way." When he's not hard at work at HHB, where he devotes most of his time, Lutz Henckels likes to play hard. "I have the capacity to really switch off work and get involved with my family. Twice a year I take a vacation with my wife and three sons, and go to places like Chile, Ecuador, or the Galapagos Islands.

—Roland Wittenberg.

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CIRCLE NUMBER 5

A Prescription for Linear ASIC's

The predictions of five years ago have not been fulfilled

JIM WILLIAMS, STAFF SCIENTIST, LINEAR TECHNOLOGY CORP., MILPITAS, CALIF.

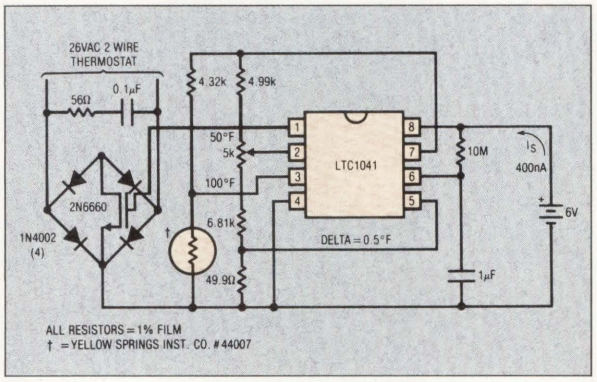
MY wife Celia is a physician. When considering a problem she frames it in terms of what *is not* said, as well as what *is* said. She's often more interested in how things are perceived and presented than in what is stated.

This approach produces some well chosen questions. She has confidence in her own abilities but doesn't confuse this with the crucial issue of getting the problem straight before operating on it.

There is a lesson here that might help us understand why linear ASICs have been such a disappointment. Disappointment? Yes. The technical and economic predictions of five years ago have not been fulfilled. Linear ASICs are a tiny portion of the linear marketplace. At least two companies that started to bring linear ASICs to market are currently building standard linear products. No linear ASIC effort has achieved anything near the growth rate, profitability or size of comparable age standard product linear companies.

What's wrong? The computer tools and models necessary to build successful linear ASICs are still crude and incomplete. Methods for selection, characterization and control of construction technologies for linear ASICs are still elusive. These and related problems are real issues and need fixing before linear ASICs can provide the desired performance and profit advantages.

Even if these problems go away, linear ASICs have a more serious issue. Most silicon scribes don't know beans about systems, and systems is what linear ASICs are all about. Few IC people have instrumented a pharmaceutical plant, or shepherded a box level product through to production. Not many have worked with an interdisciplinary team to produce a medical instrument that really does what is required. IC hackers have not considered the practical realities of transducer fed measurement in an industrial environment, in an airplane, the human body, or on an oil rig.



This ignorance of systems makes listening difficult. It's hard to know when to question or what to ask when you're ignorant. Worse, our human nature often steers us to cling to what is familiar, producing false confidence, even arrogance.

This ignorance can cause critical flaws in problem definition and communication between customer and vendor. No matter how highly developed linear ASIC technology is, it's useless if these issues are not dealt with. This point is well illustrated by the experience of standard product linear houses. Customers keep vendors on the phone with questions about "simple" linear products that they've been using for ten years. Regardless of how well written the data sheet is, no matter how much characterization or information is available, issues come up—real issues, that can sink the customer. Sometimes it takes 45 minutes just to understand what the customer is talking about, let alone arrive at a satisfactory solution. Sometimes the customer doesn't really understand what the problem is, even when they think they do. Other times you don't understand, even though you're sure you do.

'THE IGNORANCE OF MOST SILICON SCRIBES ABOUT

SYSTEMS MAKES LISTENING DIFFICULT'

I can't imagine the calamity of supporting somebody who wants 50,000 pieces of some linear ASIC. He (and I) may not know it, but he's the one providing the characterization and writing the data sheet. He expects to ship product, and I expect to make money.

The customer-vendor relationship is as crucial as the technology in attempts to build linear ASICs. For people making the ICs, this means learning a lot more about what their customers are doing than they may be used to. It also means learning how to observe and listen before saying, or even thinking, anything.

If linear ASIC is to make a significant contribution the fast talking must be replaced with some slow listening. ■

JIM WILLIAMS *is a staff scientist at Linear Technology Corporation, Milpitas, Calif., responsible for product definition, customer support and circuit design. Prior to LTC he worked at National Semiconductor and taught at M.I.T. for ten years. He has consulted for U.S. and foreign companies and governments and published over 100 articles covering analog circuit design.*

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CIRCLE NUMBER 6

SEA-OF-CELLS

ECL Arrays Come of Age

GEORGE OSTASZEWSKI,
TONY KING,
AND PHILIP WELSH, PLESSEY SEMICONDUCTORS, SWINDON, U.K.,
AND SCOTTS VALLEY, CALIF.

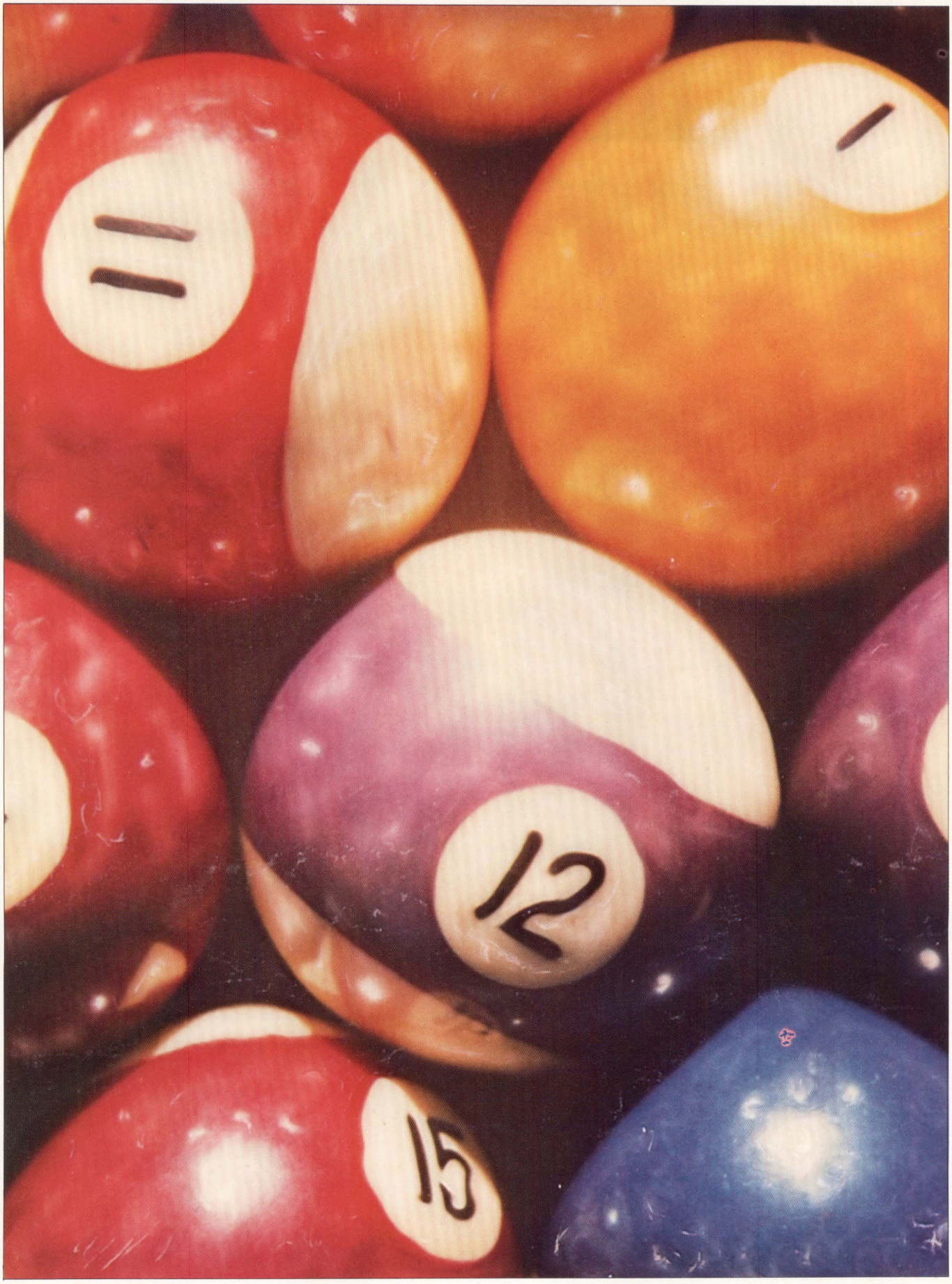
BRUCE COY AND
MIKE HOLLABAUGH,
APPLIED MICRO CIRCUITS CORP.,
SAN DIEGO, CALIF.

The sea-of-gates architectures has yielded density and performance improvements in CMOS technology. In the past, however, the high power dissipation of emitter-coupled logic (ECL) has rendered it impossible to make bipolar sea-of-gates arrays. Now, circuit design and fabrication process advances permit the hitherto impossible: 16,000-gate sea-of-gates arrays, with 95 percent utilization, a 1.2 GHz clock frequency, and power dissipation of less than 16 W.

This article presents the first bipolar sea-of-gates array capable of such performance. Available both as the ELA80K series from Plessey Semiconductors and as the Q20K series from Applied Micro Circuits Corp. (AMCC), the family offers up to some 15,000 usable gates and 256 I/Os on one chip. The arrays were jointly developed by Plessey and AMCC in a technology partnership, with both companies providing process and architecture expertise.

Novel Circuit and Processing Methods Boost Density

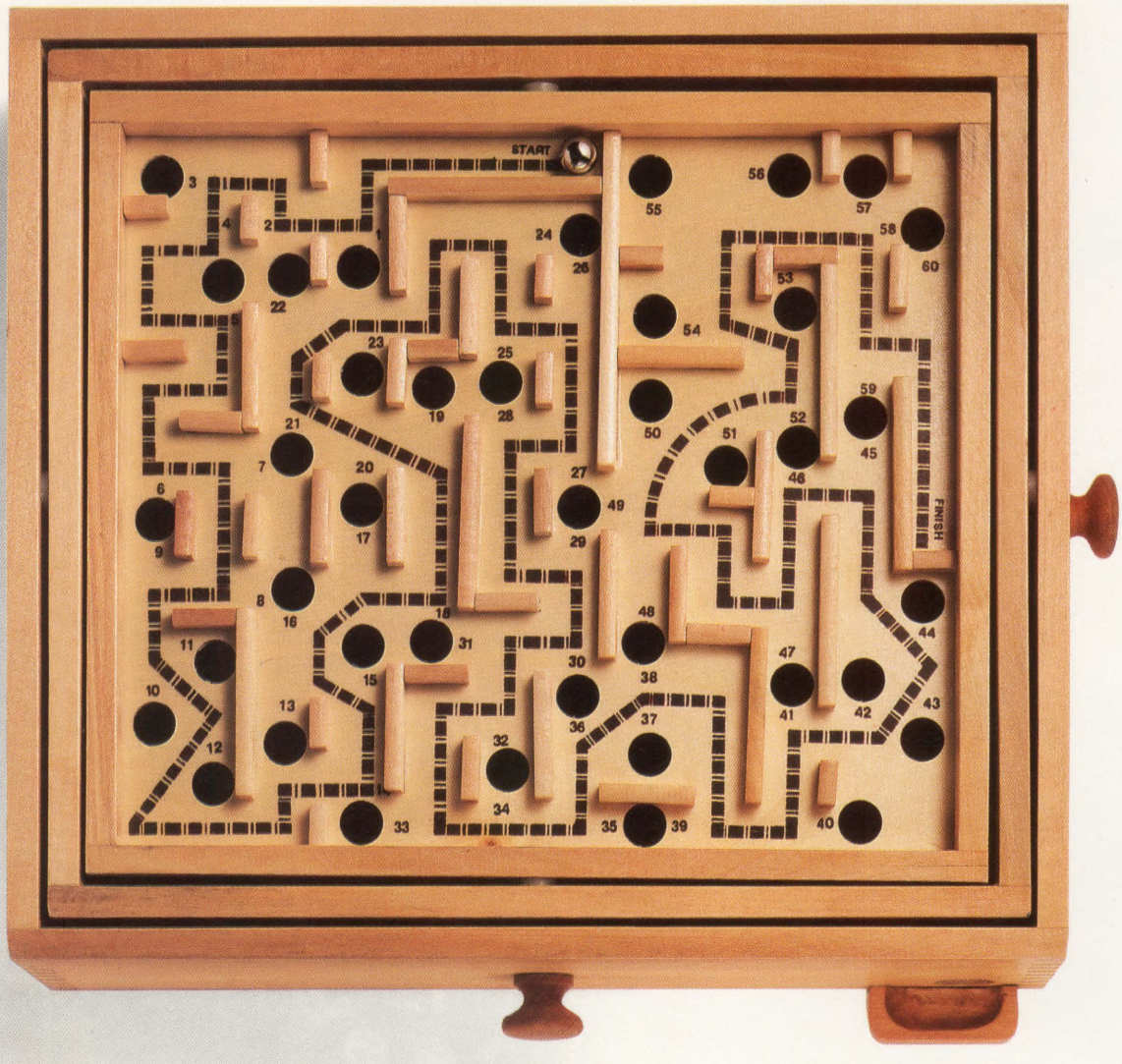
In the resulting bipolar sea-of-gates array family, innovative circuit design techniques have achieved symmetrical 130-ps gate delays with reduced static



THE SEA-OF-GATES ARCHITECTURE HAS BOOSTED ECL PACKING DENSITIES

POLOROID PRINT BY JIM FINLAYSON

The traditional approach to IC design.



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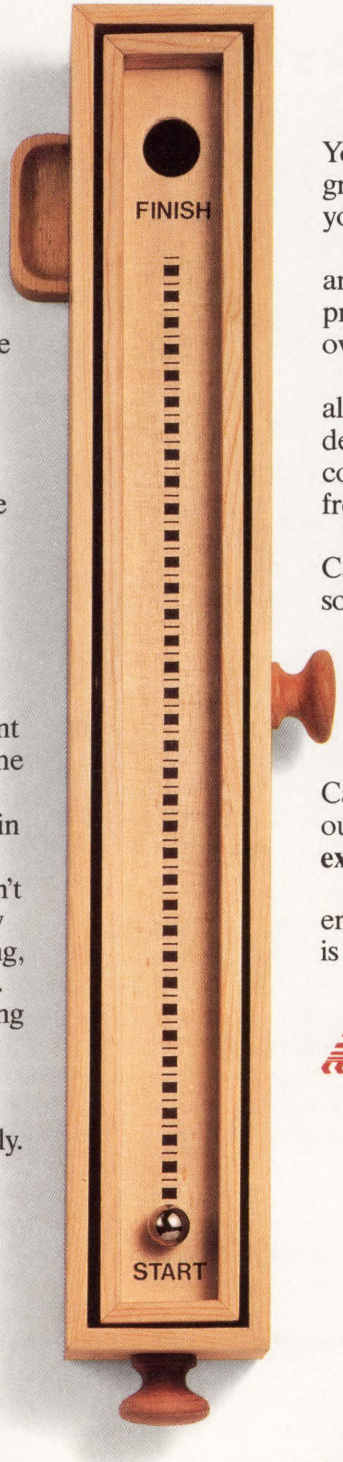

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Because in today's competitive environment playing by the old rules is a losing game.

CĀDENCE

Leadership by Design

CIRCLE NUMBER 7

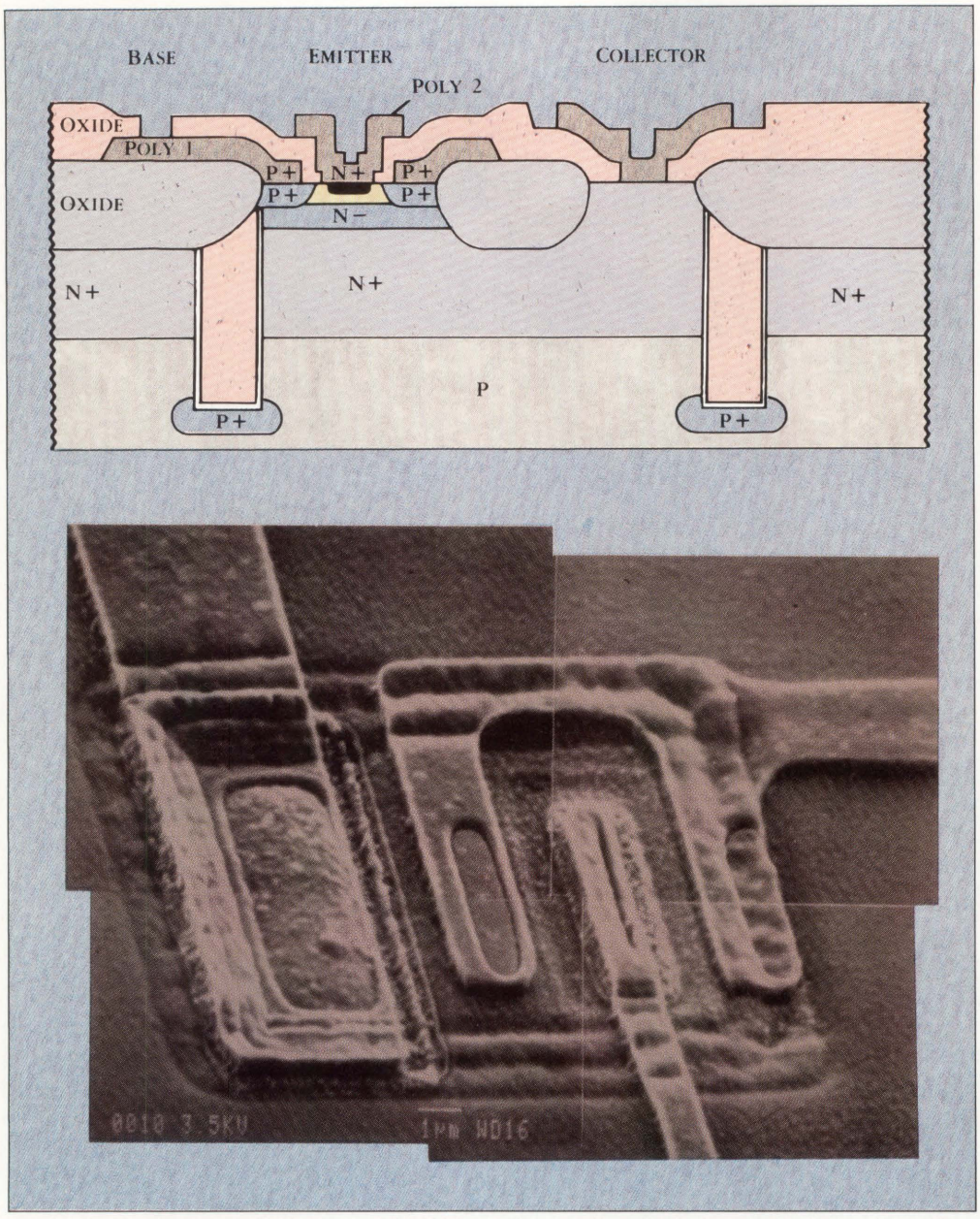

FIGURE 1. Cross-section (a) and photomicrograph (b) of the transistor structure, showing the trench isolation and polysilicon contacts.

power requirements. Since the array uses bipolar rather than CMOS process technology, gate delays are not adversely affected by capacitive loading. Sea-of-gates architectures and triple-level metal also make the arrays more compact, reducing wiring delays.

■ TECHNOLOGY

The array is manufactured on a silicon bipolar process incorporating two polysilicon contact layers (base and emitter) and trench isolation. Figure 1A shows a cross-section of the transistor structure.

The 1-μm wide trench decouples the active device from the rest of the die, reducing the collector substrate capacitance by more than half. Trench isolation is also more compact than conventional oxide isolation, doubling the possible packing density.

The minimum emitter feature size as drawn is 1 μm × 2 μm (0.6 μm × 1.6 μm effective). Combined with the low capacitance of the double-polysilicon trench-isolated process, the small feature size permits a cutoff frequency of 13.5 GHz. Figure 1B shows a photograph of a fabricated transistor with a 1 μm × 5 μm emitter.

There are two levels of polysilicon and three levels of metal interconnect in the process, resulting in extremely high routing density. The minimum wiring pitches are 4 μm, 5 μm, and 7 μm on the three metal levels.

Vias can be placed on any metal level without "yoking" (widening the metal tracks around the edge of the via). In processes that require yoking, vias cannot be placed adjacent to each other, as the widened metal tracks around each via would cause a metal short. As a result, yoking introduces restrictions on CAD tools and reduces the available routing area. The absence of restrictions on via placement in this array's process therefore facilitates automatic layout and increases the routing density.

■ TWO OBSTACLES TO HIGH-DENSITY ECL

It is the unique circuit design which, coupled with the advanced process, permits densities approaching those of CMOS in a bipolar array without sacrificing ECL's speed performance.

The new circuit structure is best understood by comparison with existing ECL. A conventional ECL output stage uses an emitter follower buffer stage to drive the load. However, in orthodox ECL technology, the emitter follower is biased by a static current source—a resistor. When the driving signal swings from low to high, the emitter follower pulls the output high at a speed commensurate with the high current available through the transistor. However, when there is a logic transition in the opposite direction, from high to low, the output is not actively pulled low; instead, the static current source sinks the required current.

The passive pull-down in conventional ECL has two disadvantages. First, the gates consume a great deal of power even when the outputs are static. In fact, the static current drain results in a power consumption on the order of 30 W for a 10,000-gate ECL chip. Power dissipation in excess of 15 W necessitates very expensive packaging with large heat sinks and at least forced-air cooling. And high current demands complicate system design and require expensive power supplies. Large power supplies increase the overall system size, further increasing system cost.

Secondly, the passive pull-down complicates logic design. Static current sources inherently introduce a difference in the transition times of the rising and falling edges, a skew that increases with interconnect loading. The presence of skew increases the likelihood of hazards and glitches.

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CIRCLE NUMBER 8

TABLE 1. I/O DRIVER COMPARISON

	TURBO FAMILY (TYP/MAX)	VITESSE VSC4500 (TYP/MAX)	RAYTHEON CGA70E18 (TYP/MAX)
ECL 10KH INPUT			
Tpd + + (ps)	200/250	514/935	430/624
Tpd − − (ps)	200/250	127/231	400/580
POWER (mW)	2.5/3.0	3.5/4.1	2.3/3.7
TTL INPUT			
Tpd + + (ps)	270/338	820/1,492	1,380/2,001
Tpd − − (ps)	100/125	1,046/1,904	530/769
POWER (mW)	1.0/1.3	6.6/7.3	3.3/5.3
ECL 10KH OUTPUT			
Tpd + + (ps)	270/338	820/1,492	830/1,204
Tpd − − (ps)	202/253	725/1,320	1,280/1,856
POWER (mW)	40.0/52.0	4.8/7.2	23.3/37.3

NOTE 1. ALL VALUES ARE FOR THE FULL MILITARY TEMPERATURE AND VOLTAGE RANGE.
NOTE 2. TURBO VALUES FOR TTL INPUT ARE BASED ON SIMULATION RESULTS. OTHER TURBO VALUES ARE ESTIMATES.
NOTE 3. VITESSE AND RAYTHEON INFORMATION FROM COMPANY DATA BOOK FIGURES.

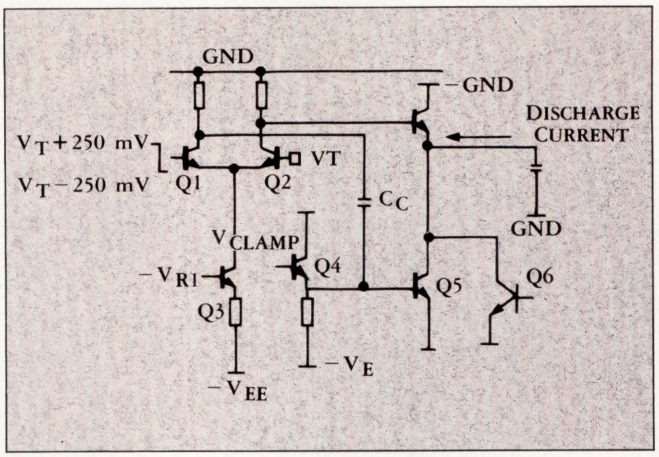

FIGURE 2. An inverter circuit in the ECL Turbo technology.

In the worst case, a circuit will not work; at best, it must run more slowly.

■ THE DYNAMIC DISCHARGE CIRCUIT

The Turbo dynamic discharge circuit overcomes the parallel problems of power dissipation and signal skew. Figure 2 shows an example Turbo circuit for an inverter. As in conventional ECL, an emitter follower provides an active pull-up of the load. However, this circuit supplements the conventional ECL structure with a capacitively coupled active pull-down arrangement. The circuit area is increased slightly by the additional capacitor and transistor. However, circuit area is not the limitation on ECL chip density; power consumption limits density much more than circuit size does. The dynamic discharge circuit yields such savings in power that chip density improves markedly despite the additional circuitry.

With the dynamic discharge circuit, an output is pulled from low to high in the same way as with conventional ECL, that is, with transistor Q_1 conducting the differential-pair current and the emitter follower strongly turned on. When the differential pair switches, the base of is charged up through C_C, turning on the active pull-down transistor. The output is then pulled from high to low through the collector of Q_5.

Since the output signal is actively pulled both up and down, rise and fall times are symmetrical. As with conventional ECL, the delays through the circuit are the same on high-going and low-going transitions; thus, the output response is completely balanced. Figure 3 shows the propagation delay for the active pull-down circuit, compared to a conventional ECL circuit in the same process technology. As can be seen, the passive pull-down delay increases by 90 ps per pF of loading, compared to about 20 ps/pF for the active pull-down.

■ I/O CELL DESIGN

Active pull-downs can be employed in gate array I/O cells for similar advantages. Differential I/O drivers typically differ in delay behavior with low-to-high and high-to-low transitions. With active pull-downs, the transitions are much more evenly balanced. Off-chip skews of signals at both 10KH and 100K logic levels have been demonstrated to show similar characteristics to those in Figure 3 over a range of typical loads. Table 1 compares I/O driver performance expected from the Turbo array technology with data sheet specifications of available ECL gate arrays from Raytheon and gallium arsenide arrays from Vitesse.

If a +5 V supply is available, the I/O cell can include a Darlington output as well as a Turbo dynamic discharge circuit. The current requirements for this +5 V supply are less than 50 mA for the entire chip.

With the Darlington output option, a single I/O cell can drive a 25-Ω parallel terminated line with significantly less current than required in using two parallel 50-Ω driver outputs, thereby reducing IC power dissipation even further.

■ ARRAY ARCHITECTURE

The reduced power dissipation makes it possible, for the first time, to use a sea-of-gates, or more appropriately, a "sea-of-cells" architecture in a bipolar array. Sea-of-cells architectures obviate the need for dedicated routing channels between core cells, yielding a 40 percent reduction in die size for a given number of cells. It is this large reduction in die size that makes the additional Turbo circuit components insignificant.

To achieve high cell utilization along with reduced die size, the array's core cells must be carefully designed for the maximum possible functional packing density. Since a bipolar gate tends to contain more components than a CMOS gate, it makes sense to use core cells that contain more components than typically found in CMOS sea-of-gates arrays.

In the Turbo array series, the core cells contain 18 active components, 10 resistors, and one capacitor (see Figure 4). The cell is thus large enough for a complete latch or a 6-input OR/NOR gate. Additional components may be shared with neighboring cells if only a small number of devices are needed for a function in any particular macro.

The array family contains three members offering up to 16,000 usable gates. The largest array contains 4290 core cells, arranged in 39 rows of 110 cells. These cell counts do not include three additional cell columns that are dedicated to provide the threshold and clamp generators required in ECL circuits (see Figure 2 again).

The sea-of-cells architecture uses all three levels of metal for signal distribution. The lowest metal level is used almost exclusively to wire the transistors into SSI, MSI and LSI macros such as NOR gates, multiplexers, latches, and counters.

The power grid for the array core is fixed and resides on the two upper metal layers, with horizontal power buses on the second level and vertical power buses on the third level. The matrix of second- and third-level metal power buses dis-

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fast, crisp graphics; intuitive and flexible data entry; GDSII and/or Gerber compatibility.

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inexpensive desktop workstations without the performance degradation of multi-user systems.

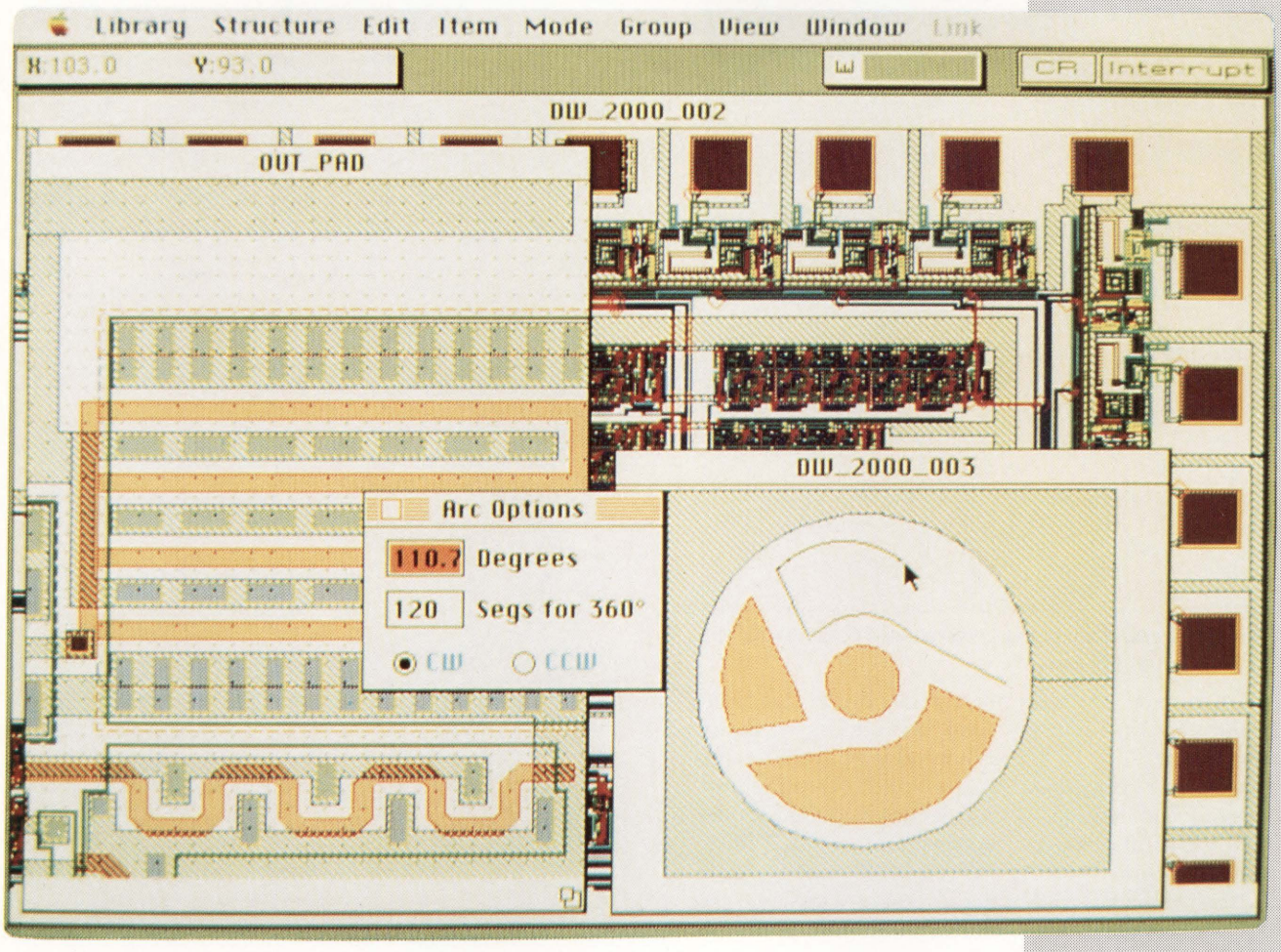
▲ Economy:

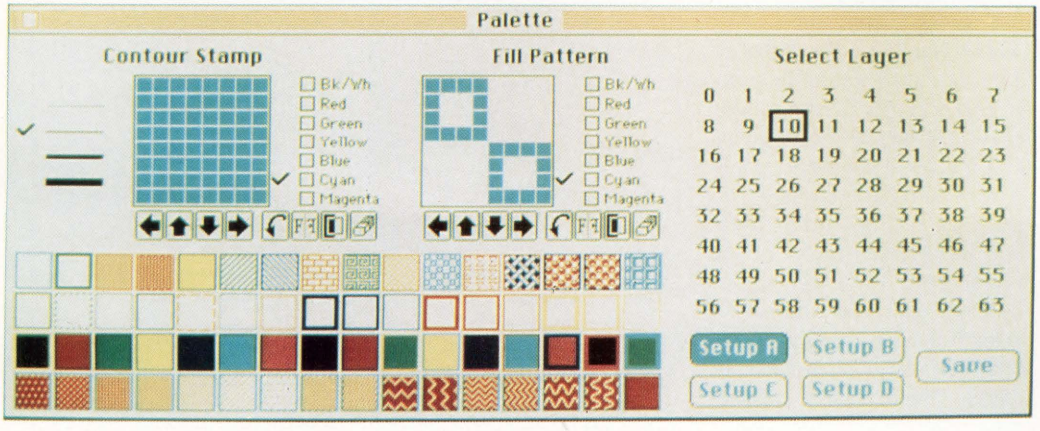
inexpensive to purchase without the overheads (installation, maintenance, training) of either mainframes or equivalent workstations.

▲ Ease of use:

user-friendly Macintosh II™ implementation of industry standard commands minimizes your 'learning curve'.

A: dw-2000™





Easily handles the largest layouts; multiple window capability.

Powerful Palette dialog replaces cumbersome multiple command interfaces and allows complete flexibility to create, mix and match contour and fill colors/ patterns.

DESIGN Workshop

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CIRCLE NUMBER 10

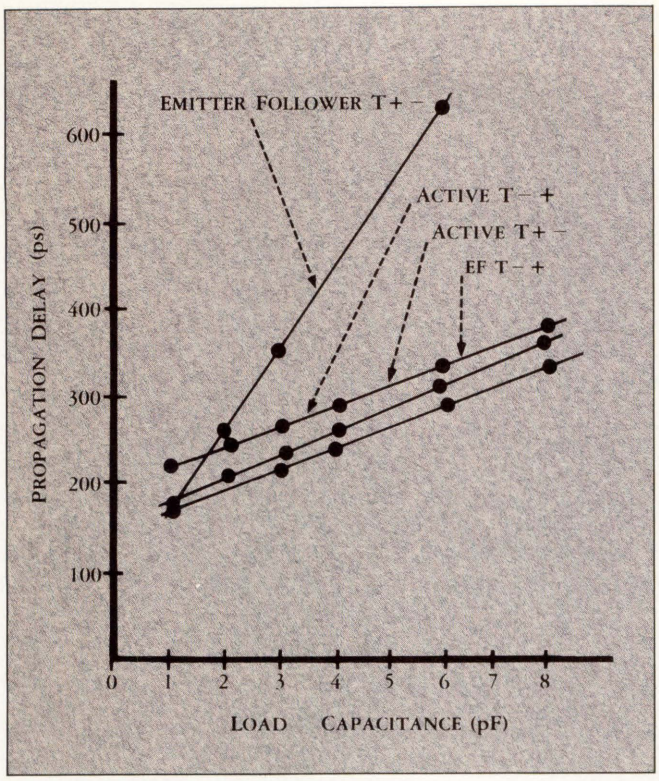


FIGURE 3. Propagation delay versus loading for conventional ECL (emitter follower) and for ECL Turbo (active) NOR gates.

tributes current evenly through the chip and minimizes bus drops.

The lower power dissipation with the active pull-down circuit design means that power buses can be narrower compared to conventional ECL and less of the metal levels are taken up by wide power lines. As a result, there is ample room for all the inter-macro signal routing on the second and third levels of metal, in the spaces between the power tracks. For example, in the 16,000-gate array, there are 702 horizontal and 660 vertical wiring channels for global interconnect. These channels are arranged with 18 running horizontally between each power bus on metal two, and 6 running vertically between each power bus on metal three.

The macros are wired up on the first metal level using a 4-μm pitch. The horizontal routing, however, has a 5-μm pitch, and vertical wiring has a 7-μm pitch. Because a substantial portion of the wiring is accomplished on metal level one, the larger pitches on higher metal levels do not impede routability. However, there is no direct correspondence between the grids on each metal level. Therefore, to facilitate global routing, the macros are handcrafted to offer multiple "hit points," where vias can be dropped from the global routing tracks onto the individual macros.

Obviously, hit points cannot occur in the same place as the power grid, else they would merely tie the signal to a power rail. Because the power grid occupies fixed locations every 19 horizontal channels and 7 vertical channels, macro wiring can "slide around" on the sea-of-cells array only within one such sector of the power grid.

With ECL, the number of transistors in a standard gate is relatively large compared to CMOS. There is also a larger variety of components needed for each gate. The cells in ECL sea-of-cells arrays are therefore larger. The power rail is fixed to fall on the cell boundary. The cells are 7 terminals wide and 16 terminals high. The horizontal power buses then fall over the resistors at the top and bottom of the cell, which tie to the power rails anyway, so no hit points are obstructed. The vertical rail falls over the leftmost column of components, all of which are internal gate components (biasing transistors and the coupling capacitor). There are therefore no problems with hit-point obstruction, even though a fixed power grid is employed.

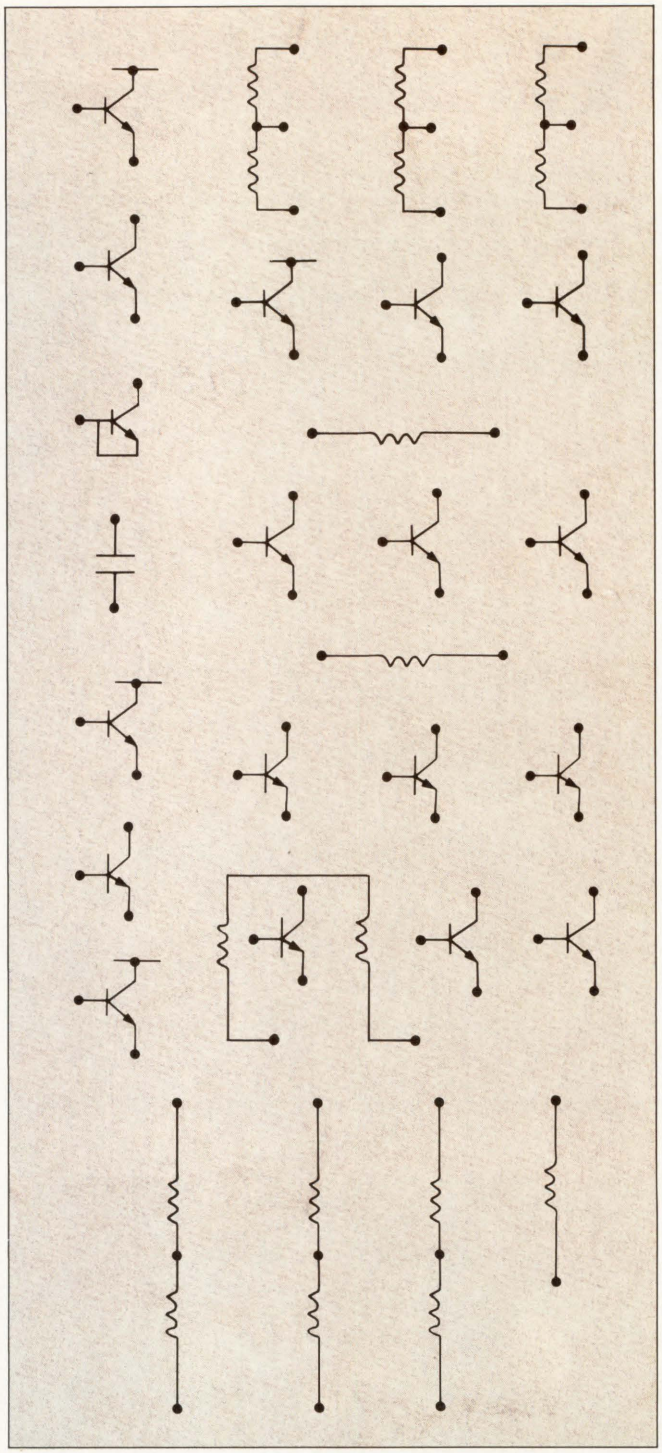


FIGURE 4. Component layout in the Turbo array constituent cells.

■ FRONT-END DESIGN SUPPORT

Both Plessey and AMCC support front-end design on the Macro-Matrix design environment, which is integrated with Daisy, Mentor, and Valid engineering workstations. These systems assist the designer in all phases of the design cycle. During initial specification, the designer can capture schematics and run product-dependent engineering rules checks. During design analysis, he can perform logic simulation and check

Z I L O G

Z180

Great code compatibility. Terrific performance. Superintegration.™

Zilog's Z80180™ is the CMOS general purpose controller with the high performance and the on-board peripherals that make it clearly the cost-effective, space-saving choice. Whether you're upgrading a Z80 application or designing a totally new system.

Zilog is Superintegration.

ASICs are the obvious answer to many of today's demands for customized products for specific uses. But it's also clear that, as the demand for higher levels of integration grows, the need for a new approach to ASIC arises. That new approach is Superintegration from Zilog.

Through Superintegration, Zilog has developed a rapidly growing family of Application Specific Standard Products (ASSPs). Simply put, ASSPs are working cores and cells combined and enhanced for specific applications. They are not custom parts. In fact, the ASSPs we develop use the same architecture and the same codes you're already working with. Compared to ASICs, ASSPs mean a lot less risk. And non-recurring engineering (NRE) charges are eliminated. Plus, tight on-silicon coupling enhances performance. And board real estate is significantly reduced. Think what all this can mean to your time-to-market.

And think about this. Nobody has a more complete library of proven, working generic cores, system cells, or I/O bolt-ons than Zilog. Nobody is better qualified to develop—and deliver—Superintegration parts.

Full software compatibility.

You'll be up and running with the Z180 immediately. Because it's 100% object code compatible with Z80/8080.™ You probably already know the code, so you can port right onto the Z180. Not only that, since Zilog originally developed the part jointly with Hitachi, the Z180 is directly compatible with Hitachi's version, the HD64180Z.™

Enhanced performance.

Of course, the Z180's CPU core gives you more power and speed than discrete CPUs. Besides that, there are several new instructions. You also get operating frequencies to 10 MHz. And you have the overall performance advantages of CMOS and Superintegration.™

The important peripherals are on board.

The Z180's high integration results in impressive savings in costs and real estate. The MMU gives you one Mbyte of addressing space. You have 2 DMA channels, 2 UART channels, and 2 16-bit programmable counter-timers. Plus wait-state generators, an interrupt controller, a clock oscillator/generator, and a clocked serial I/O port. All integrated on the Z180 chip.

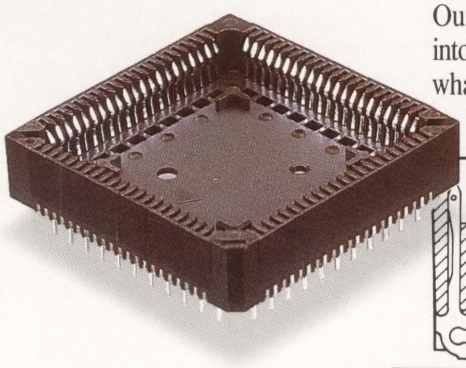
If this isn't enough to convince you to take a look at what the Z180 can do for your design project, here's a little more to consider. The full complement of development support tools are readily available from industry leaders. And the Z180 comes to you off-the-shelf, backed by Zilog's proven quality and reliability. Find out more about the Z180 or any of Zilog's growing family of Superintegration products. Contact your local Zilog sales office or your authorized distributor today. Zilog, Inc., 210 Hacienda Ave., Campbell, CA 95008, (408) 370-8000.

Right product. Right price. Right away. **Zilog**

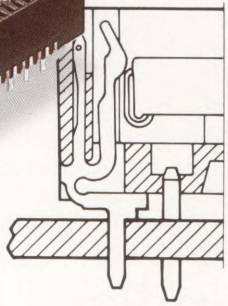
ZILOG SALES OFFICES: CA (408) 370-8120, (714) 838-7800, (818) 707-2160, **CO** (303) 494-2905, **FL** (813) 585-2533, **GA** (404)923-8500, **IL** (312) 517-8080, **MA** (617) 273-4222, **MN** (612) 831-7611, **NJ** (201) 288-3737, **OH** (216) 447-1480, **PA** (215) 653-0230, **TX** (214) 987-9987, **CANADA** Toronto (416) 673-0634, **ENGLAND** Maidenhead (44) (628) 39200, **W. GERMANY** Munich (49) (89) 612-6046, **JAPAN** Tokyo (81) (3) 587-0528, **HONG KONG** Kowloon (852) (3) 723-8979, **TAIWAN** (886) (2) 741-3125, **SINGAPORE** 65-235 7155, **DISTRIBUTORS: U.S.** Anthem Electric, Bell Indus., Hall-Mark Elec., JAN Devices, Inc., Lionex Corp., Schweber Elec., Western Microtech. **CANADA** Future Elec., SEMAD, **LATIN AMERICA** Argentina—Yel.-(1) 46-2211, Brazil—Digibyte (011) 241-3611, Mexico—Semiconductores Profesionales (5) 536-1312.

CIRCLE NUMBER 11

A chip carrier socket that won't play "pop goes the circuit."



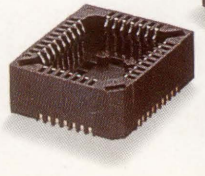
Our sockets are designed to get solidly into contact and stay in contact. No matter what the outside influences. Pop-out is simply not a problem.



Controlled contact interface angle in AMP HPT sockets ensures positive chip carrier retention. Our exclusive removable housing allows direct inspection of solder joints, and fast repair/replacement of contacts.

The contacts are High Pressure Tin, an AMP proprietary design which creates very high normal forces—a minimum of 200 grams per contact—for maximum retention and reliable interconnection. Short-signal-path contacts float in the housing to accommodate thermal expansion.

Two basic styles of sockets are available: square or 32-position rectangular EPROM and SO-J. Both come in solder

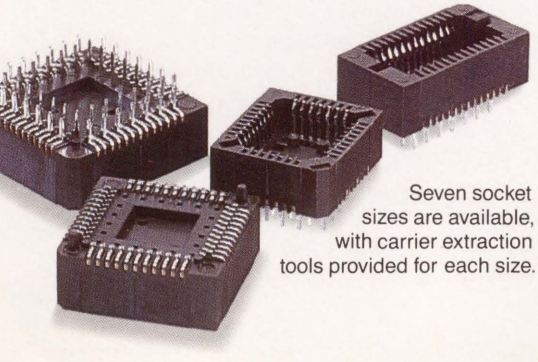


tail or surface mount versions and feature all the important details. Tin-over-nickel plating is applied after the contacts are formed, to assure full plating. We've built in visual indicators for locating pin 1, and polarizing to aid correct insertion.

Orientation holes in the 94V-0 housing floor make registration to the pc board both fast and simple, ideal for hand or tube-loaded robotic insertion. And the high pin counts make very effective use of real estate.

Call the AMP Information Center at 1-800-522-6752 for literature on HPT PLCC Sockets. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP Interconnecting ideas



Seven socket sizes are available, with carrier extraction tools provided for each size.

CIRCLE NUMBER 30

TABLE 2. D FLIP-FLOP COMPARISON

	TURBO FAMILY (TYP/MAX)	VITESSE VSC4500 (TYP/MAX)	RAYTHEON CGA70E18 (TYP/MAX)
C−>Q			
Tpd + +(ps)	362/427	1,035/1,884	680/986
Tpd + −(ps)	292/344	762/1,387	650/943
C−>QN			
Tpd + +(ps)	362/427	860/1,565	680/986
Tpd + −(ps)	292/344	977/1,778	650/943
POWER (mW)	3.2/3.8	2.0/2.8	5.0/8.0

NOTE 1. ALL VALUES ARE FOR THE FULL MILITARY TEMPERATURE AND VOLTAGE RANGE.
NOTE 2. TURBO VALUES ARE BASED ON CIRCUIT AND PROCESS SIMULATION RESULTS.
VITESSE AND RAYTHEON INFORMATION FROM COMPANY DATA BOOK FIGURES.

critical paths via static timing analysis under a range of operating conditions. In test generation, the engineer can verify test vector formatting and determine the vector set's fault coverage.

AMCC also offers a version of the MacroMatrix system that allows array users to perform their own placement and routing. The CAD tools, discussed below, incorporate a rule-based expert system that accepts user parameters and then generates a layout automatically.

MacroMatrix support also includes software that automates design submission to Plessey and AMCC, facilitating the otherwise onerous task of interfacing with the vendor.

Plessey also supports the mainframe-based CAE system PDSII. PDSII runs on all VAX VMS systems and offers all the same features as the engineering workstations. PDSII also supports all of Plessey's CMOS gate array and cell-based ASIC products and is furnished with a multiple-window interactive design and layout environment.

■ PLACEMENT AND ROUTING

Sea-of-gates arrays present unique challenges to layout tools because of the restricted routing space. Typical sea-of-gates offerings do not support utilizations much higher than about 45 percent (Meyer, 1988). However, due to the use of triple-level metal, an optimized power grid, and larger cells than found in CMOS arrays, the utilization of the bipolar sea-of-cells architecture in the Turbo arrays is more than twice as high. Moreover, because each cell is larger and contains more equivalent gates than CMOS sea-of-gates array cells, there is less global routing over a larger area, which makes layout a simpler task.

Currently available for automatic placement, AMCC's AMCCAD layout system uses an enhanced version of the least-squares algorithm found in In least-squares placement, the flattened netlist is projected onto an *N*-dimensional space with internodal distance dependent on user-defined weights. The *N*-dimensional representation is then flattened into a planar mesh.

Plessey is readying an automatic floorplanning and layout system that will be offered as part of PDSII. The floorplanner will use the hierarchy defined by the designer for an initial constructive placement. The placement within each block will then be optimized with a rule-based system. The optimization works from the logic structure, minimizing clock distribution and busing problems.

Because global routing occurs on only two of the three metal layers (with one layer dedicated to macro routing), a conventional two-level router can be employed for global signal routing.

Plessey's PDSII and AMCC's AMCCAD both offer *N*-level routers. These layout tools allow interactive routing of critical paths as well as completely automatic routing in accordance with user-specified net priorities.

As a result of the technology agreement between the two companies, designers can now not only design in the highest-performance arrays currently available, but also are furnished with a complete alternate-source capability on all aspects of the CAE and CAD process. The design engineers can use either Plessey's or AMCC's CAE system; either Plessey or AMCC will perform automatic placement and routing; and whichever CAE and CAD path is chosen, either prototypes or production quantities may be obtained from the other vendor if desired.

■ PERFORMANCE CONCLUSIONS

An advanced 1-μm bipolar process enabled the design of a 16,000-gate ECL array that can operate in the region of 1.5 GHz. By using the Turbo dynamic discharge circuitry in the core macros, static current consumption is dramatically reduced compared to conventional ECL. In addition, the dynamic discharge circuit yields symmetrical rise and fall delays over the full range of loading conditions.

The dynamic discharge circuit has for the first time made it possible to use a sea-of-cells architecture for a bipolar logic array. Removing routing channels increases circuit density and therefore reduces both chip size and wire delays. CAD support and careful array design make it possible to obtain 95 percent utilization of a 16,000-gate array.

Table 2 compares the performance parameters of the sea-of-cells array devices with those for existing channeled ECL (Raytheon) and gallium arsenide (Vitesse) arrays. The sea-of-cells Turbo architecture clearly will yield higher performance. The Turbo array also offers an order of magnitude higher gate density than GaAs arrays.

The speed and density of the array family makes it suitable for applictaions such as supercomputers, mainframes, military systems, optical data network support, and instrumentation. ■

REFERENCES

MEYER, E.L. 1988. *"Garnering the Gates in High-Density Arrays," VLSI Systems Design's Semicustom Design Guide.*

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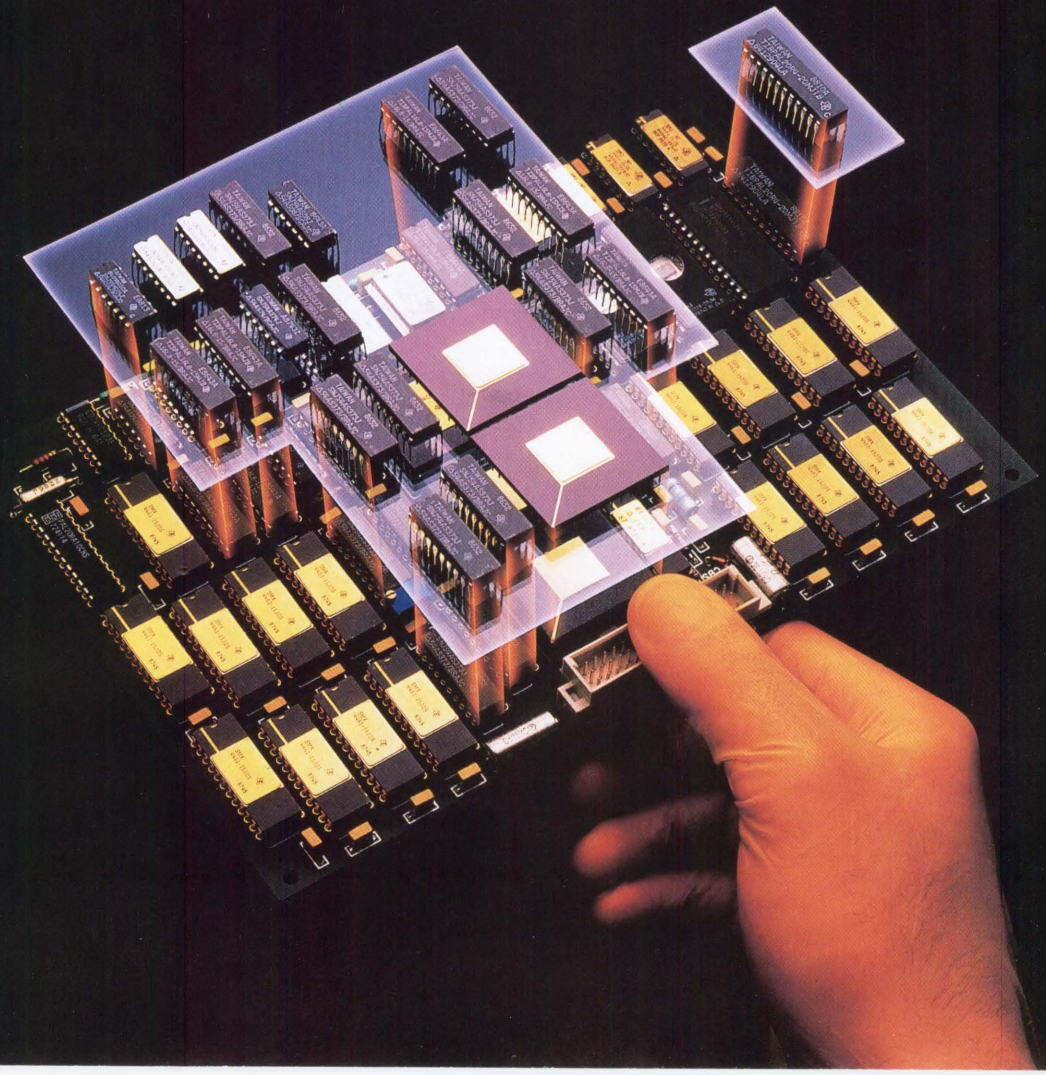
TEXAS INSTRUMENTS REPORTS ON

SYSTEMS LOGIC

IN THE ERA OF

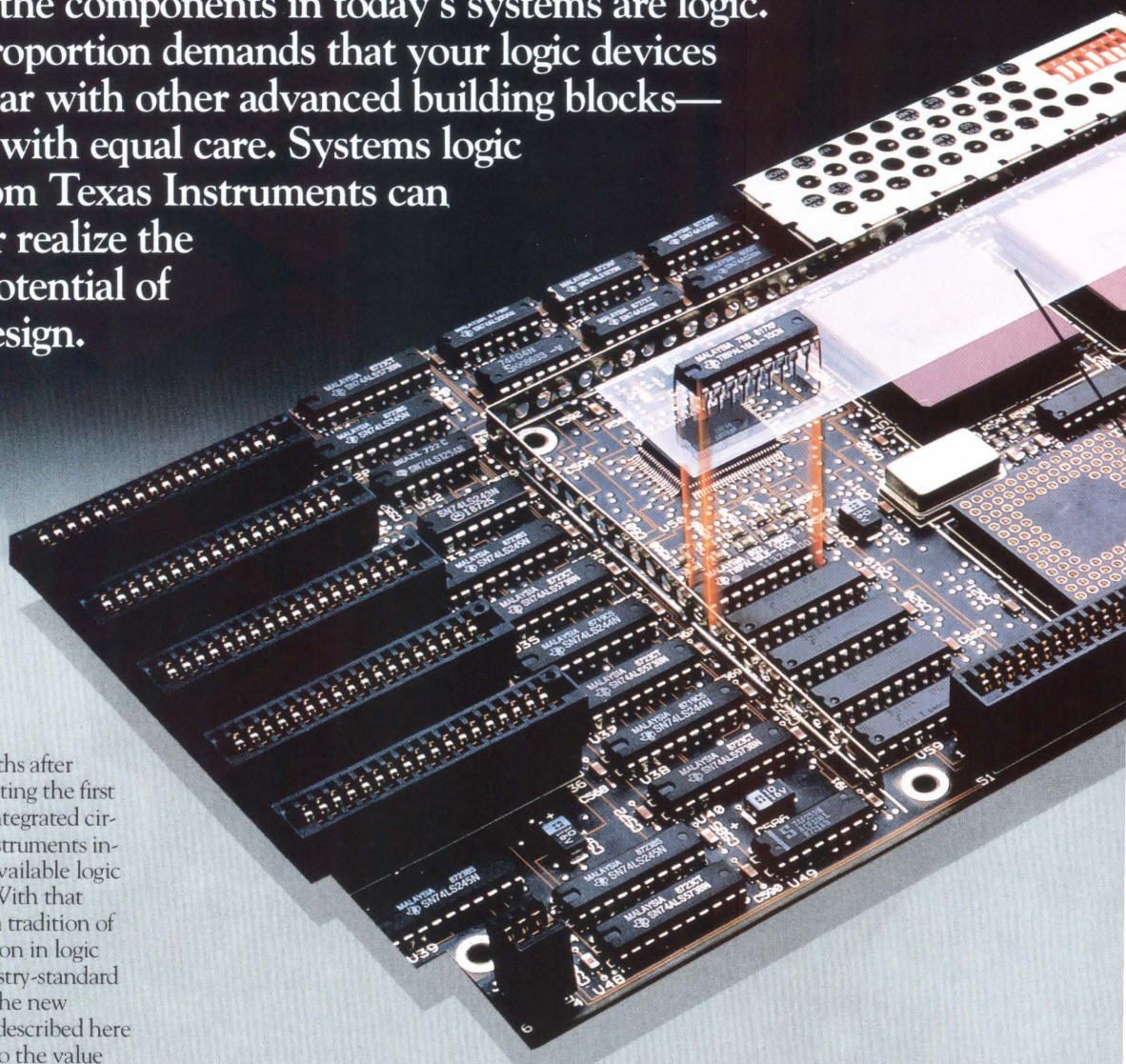
MegaChip TECHNOLOGIES



Systems logic in the Era of MegaChip Technologies:

No system should ever be limited by its to help your design perform at its best.

Up to 65% of the components in today's systems are logic. Such a large proportion demands that your logic devices perform on a par with other advanced building blocks—and be chosen with equal care. Systems logic alternatives from Texas Instruments can help you better realize the performance potential of your system design.



Within months after demonstrating the first working integrated circuit 30 years ago, Texas Instruments introduced a commercially available logic function, an RS flip-flop. With that beginning, TI established a tradition of development and innovation in logic that encompasses the industry-standard SN54/74 Series TTL and the new families of advanced logic described here that can add significantly to the value and performance of your overall system.

For example, for systems that require off-the-shelf flexibility with a degree of customization, TI's Programmable Logic Devices (PLDs) include popular 10-ns PAL® ICs available in high volume. And, to keep pace with today's high-speed microprocessors, TI plans to continue to drive PLD performance to sub-10-ns speeds.

TI's Advanced CMOS Logic (ACL) supports the design goal of high performance combined with low-power operation, while TI's new BiCMOS bus-interface family delivers very high drive current at very low power compared to bipolar circuits.

ON THE COVER: Suspended above the board, provided by Rockwell International, Missile Systems Division, are military versions of TI advanced logic devices.

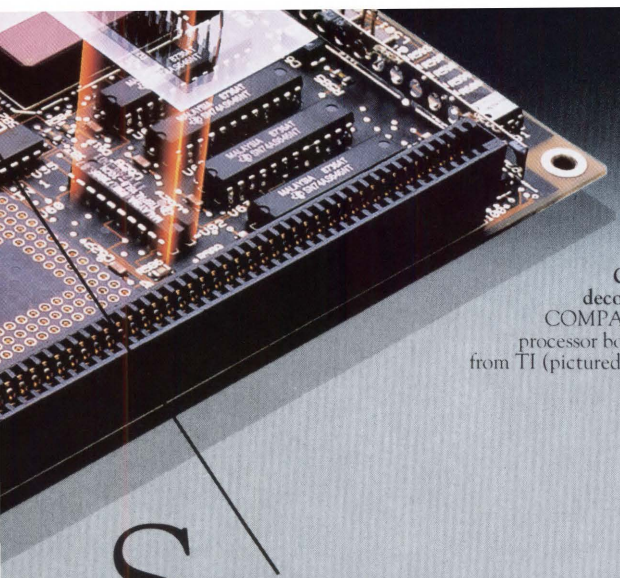
TI's MegaChip Technologies

Our emphasis on high-density memories is the catalyst for ongoing advances in how we design, process, and manufacture semiconductors and in how we serve our customers. These are our MegaChip™ Technologies, and they are the means by which we can help you and your company get to market faster with better products.

For systems requiring moderate densities and fast prototype cycle times, TI offers a new series of one-micron CMOS gate arrays. When you need higher levels of integration plus increased design flexibility, TI's one-micron CMOS standard cells provide the means for system consolidation.

And for military applications, TI offers a wide choice of high-reliability logic functions.

On the following pages are details of what you can expect from TI's range of logic options:



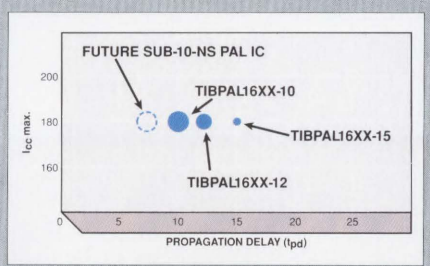
Contributing significantly to fast address decoding in speed-critical paths of the COMPAQ DESKPRO 386/20™ personal computer processor board are two TIBPAL16L8-10 PAL circuits from TI (pictured above a segment of the board).

Speed your system to market with TI's superfast PLDs.

PLDs are a functional alternative to standard logic ICs and gate arrays or standard cells.

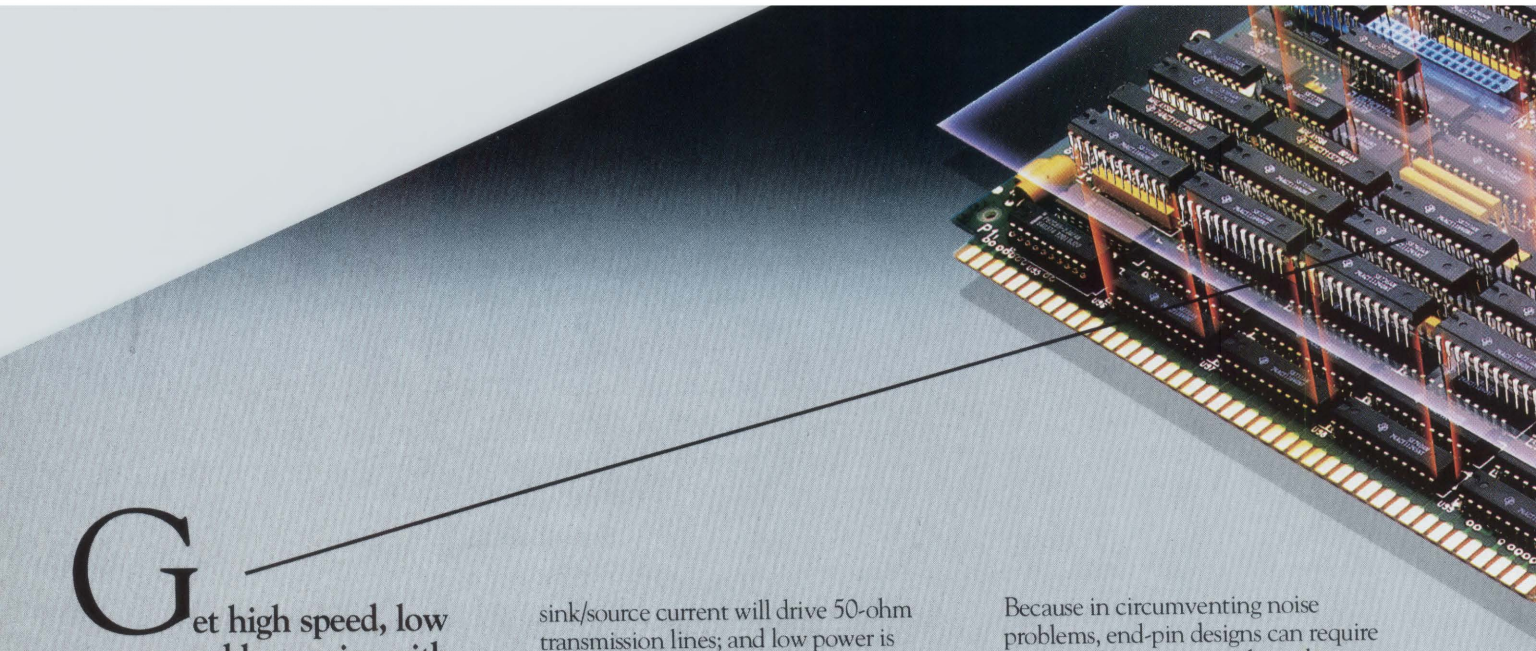
Because TI's PLDs are off-the-shelf items you program yourself, you avoid the longer design cycle times of custom ICs and move on to market faster. These PLDs offer very attractive performance advantages. Consider these:

- **TIBPAL16XX-10 PAL ICs** from TI deliver a 10-ns propagation delay and are available in quantity. Clock-to-Q time is 8 ns, and output-registered toggle frequency is 62.5 MHz. IMPACT-X™ technology gives these PAL ICs their superior speed; they are well suited for use with high-speed processors such as the Motorola 68030, the Intel 80386, and RISC-based architectures. The 10-ns performance brings a higher level of integration to speed-critical paths.
- **TI's TIEPAL10H16P8-6 IMPACT™ ECL PAL circuit** delivers even faster operation: 6-ns propagation delay max. You can now streamline conventional ECL designs by consolidating several discrete components into a single custom function.
- **TI's new 7-ns Programmable Address Decoder** is intended to help you squeeze more performance out of memory interface systems. By performing address decoding much faster than conventional PAL architectures—in 7 ns—the TIBPAD16N8-7 allows you to take advantage of the new processors to increase overall system performance.
- **TI's 50-MHz Programmable State Machines (PSMs),** TIB825S105B (16 x 48 x 8) and '167B (14 x 48 x 6), are ideal for use in high-performance computing, memory interface, telecommunications, and graphics. These PSMs may be used to implement custom sequential logic designs such as peripheral I/O controllers and video-blanking controllers.
- **The TIBPAL22VP10-20,** with a 20-ns delay, is 20% faster than the competition's "A" version and much more flexible. A programmable output macrocell allows two extra, exclusive output configurations, for a total of six.
- **TI's TICPAL16XX Series 20-pin CMOS PAL ICs** are the cure for power problems. They operate at virtually zero standby power and are reliable, high-performance replacements for conventional TTL and HCMOS logic. The devices can be erased and reprogrammed repeatedly.



TI's PAL IC road map shows consistent power and consistently higher speeds, with even faster versions on the way.

Turn page for more information

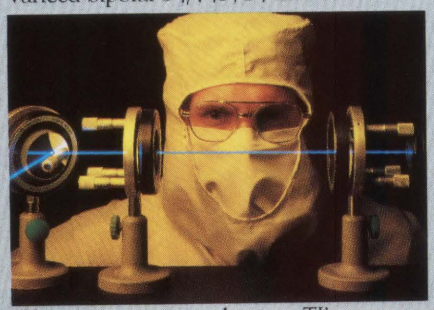


Get high speed, low power, and low noise with TI's broad ACL family.

It's an extensive family that includes gates, flip-flops, latches, registers, drivers, and transceivers. It's a readily available family in DIP and SOIC packages. It's TI's high-performance EPIC™ ACL family, bringing with it an important bonus—major reductions in noise.

Family speed is comparable to advanced bipolar 54/74F; 24 mA of sink/source current will drive 50-ohm transmission lines; and low power is characteristic of TI's EPIC technology. All this with "ground bounce" substantially reduced compared with end-pin ACL. The reasons are innovative packaging and a circuit-design technique called OEC™ (Output Edge Control) which softens the transition states that cause simultaneous switching noise. In fact, EPIC ACL noise levels are typically 10% less than those of bipolar devices.

The rapidly increasing customer acceptance of TI's ACL family confirms its noise-reduction advantages and its ease of use.



When every nanosecond counts, TI's new high-performance ACL family can help you significantly improve system speed.

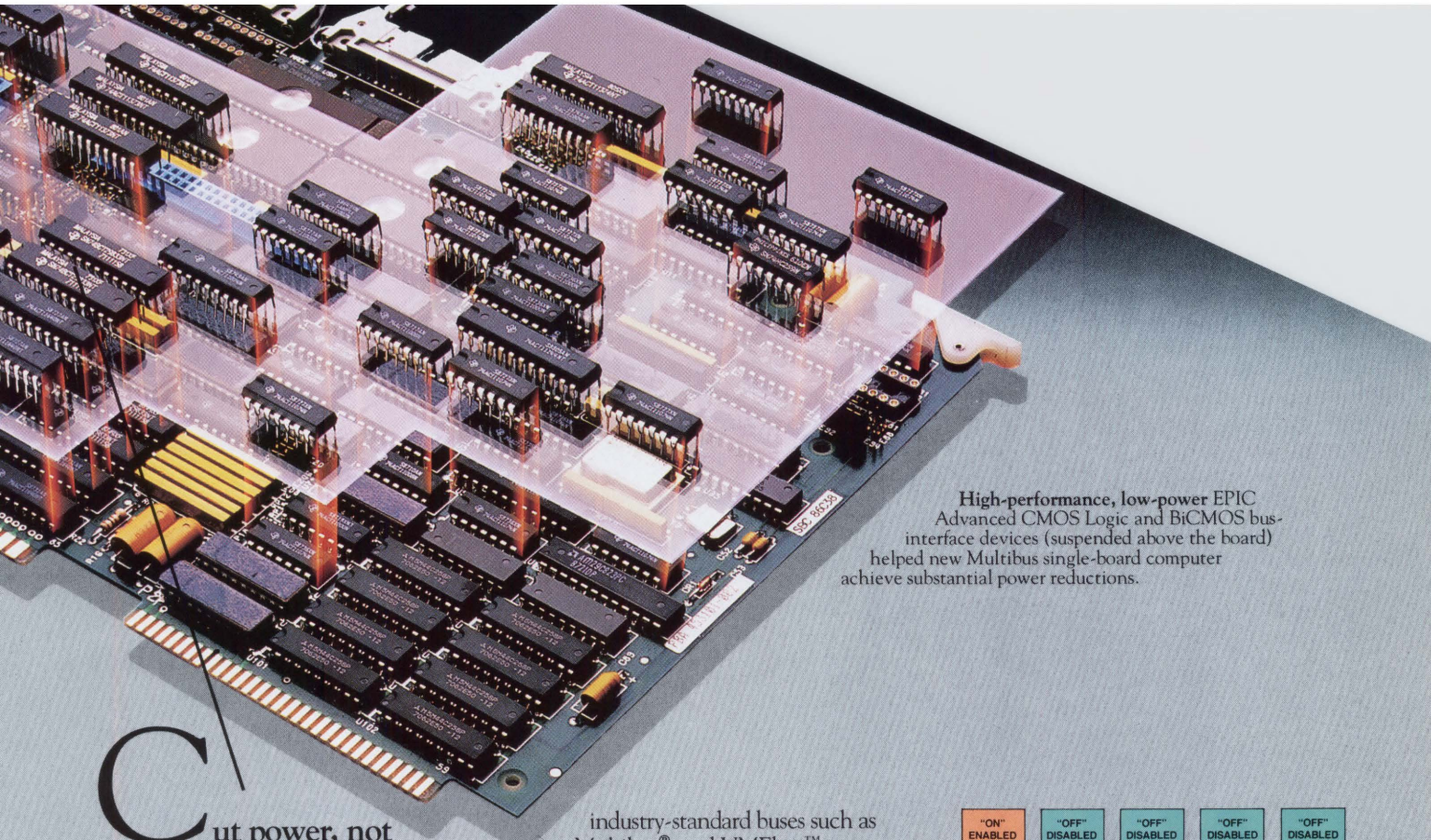
System design advantages

A unique "flow-through architecture" simplifies board design, layout, and troubleshooting. Inputs surround power pins on one side, outputs on the other, and control pins are strategically located at the package ends.

From a systems perspective, TI's arrangement offers the lowest-cost design when compared to end-pin ACL. Because in circumventing noise problems, end-pin designs can require additional components that take up to 32% more board area and slow system performance.

There are 146 functions, in both AC and ACT versions, currently announced in TI's ACL family, including such innovative, highly complex functions as advanced transceivers, line drivers, latches, feedback registers, multiplexers, and counters.

This ACL family, developed in cooperation with and supported by Philips/Signetics, fully meets JEDEC industry-standard No. 20 specifications for Advanced CMOS Logic.



High-performance, low-power EPIC Advanced CMOS Logic and BiCMOS bus-interface devices (suspended above the board) helped new Multibus single-board computer achieve substantial power reductions.

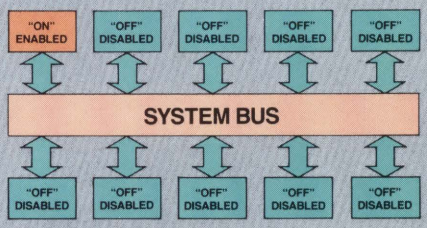
Cut power, not speed or drive, with TI's BiCMOS bus-interface ICs.

This new family is a simple, effective means to reduce system power consumption without compromising advanced performance.

As the BiCMOS name implies, TI combines bipolar IMPACT and CMOS processing to achieve switching speeds comparable to advanced bipolar products and provide the 48/64-mA drive current needed for high-capacitive loads and backplanes. In particular, family members meet the drive requirements of industry-standard buses such as Multibus® and VMEbus™

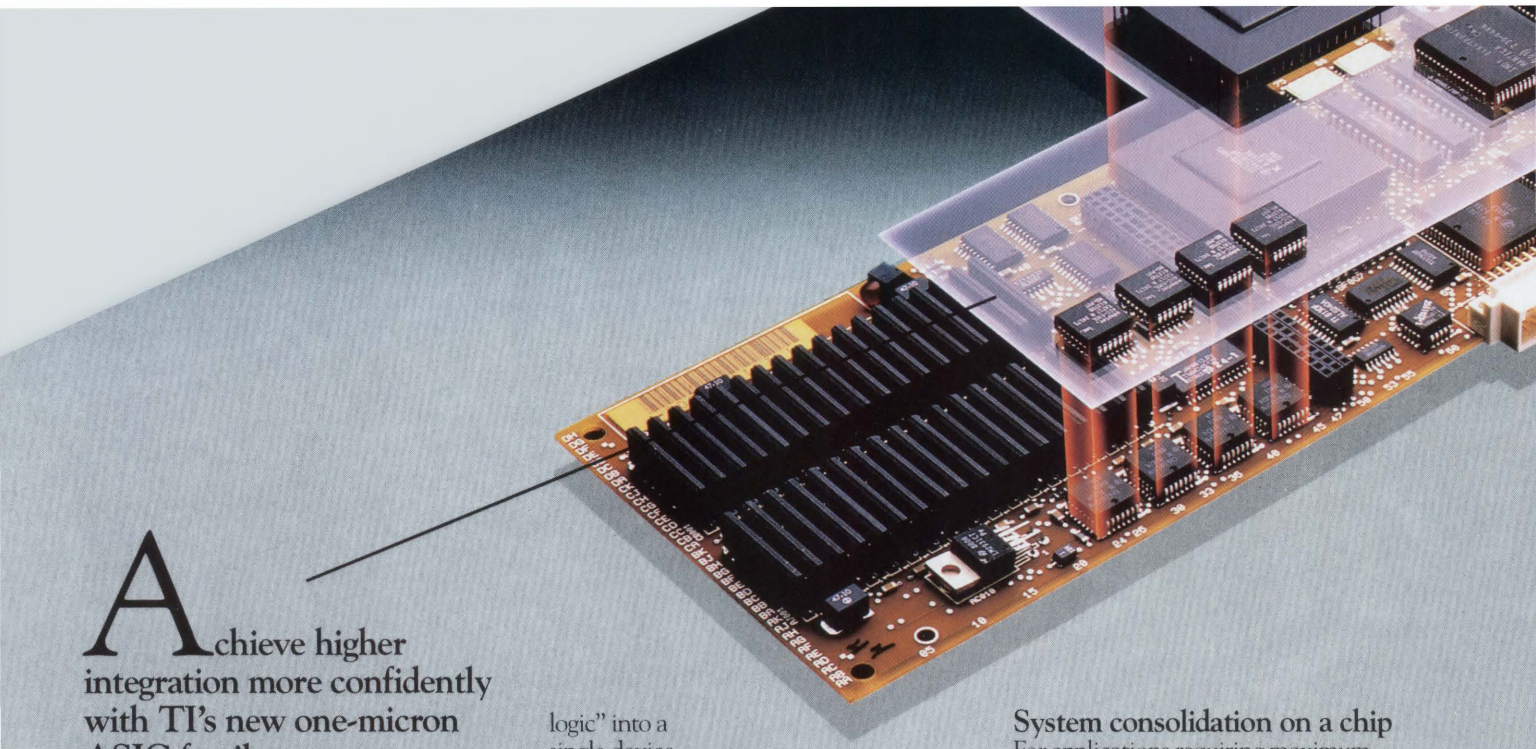
In addition, TI's BiCMOS devices can reduce disabled currents by 95% and active currents by 50%-80% compared to bipolar equivalents. Result: System IC power savings can be more than 25%.

There are more than 60 functions comprising TI's BiCMOS bus-interface family. Included are 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers—a wide choice that means you can easily find what you need to implement high-performance bus-interface designs.



An innovative circuit design in TI's BiCMOS bus-interface logic helps lower disabled currents. This is key to overall power savings because in a typical bus network only one device is enabled at a time.

Turn page for more information



Achieve higher integration more confidently with TI's new one-micron ASIC family.

Now, you can integrate more of your systems logic using TI's new one-micron CMOS ASIC (application-specific integrated circuit) family—the TGC100 Series gate arrays and the TSC500 Series standard cells. Each offers different degrees of design flexibility and system integration. The result is significantly reduced component count which cuts board size and system cost while improving reliability and performance.

And TI is supporting the family with comprehensive kits that help minimize design cost, risk, and time by providing a comfortable, easy-to-use design environment.

Efficient logic consolidation

Using TI's new TGC100 Series gate arrays, you can sweep major chunks of "glue logic" into a single device while realizing fast design and prototype cycle times. Array densities currently range to more than 8K usable gates and 142 bond pads; the Series will be extended to more than 16K usable gates and 216 bond pads in a major production release planned for late 1988. Prototype delivery is typically two to three weeks from approval of postlayout simulation results.

The TGC100 Series Design Kit gives you complete autonomy and control over the design process. It is a comprehensive set of the tools required for successful gate-array design and validation *(see last page for details)*.

Standard packages for the TGC100 Series range from 28-pin DIPs to 84-pin PLCCs, with optional packages up to 144 pins.

System consolidation on a chip

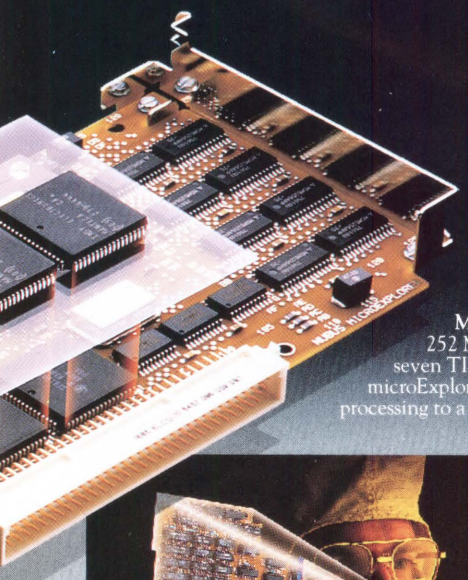
For applications requiring maximum design flexibility and higher levels of integration, TI has disclosed its third-generation standard-cell family, the TSC500 Series.

Complex system designs can be implemented using a growing core of basic SSI/MSI functions, as well as scan cells for testability and MegaModule™ building blocks such as register files. FIFOs, bit-slice family functions, RAM, and ROM are other aids to implementation. Output cells with drive capability up to 64 mA are available.

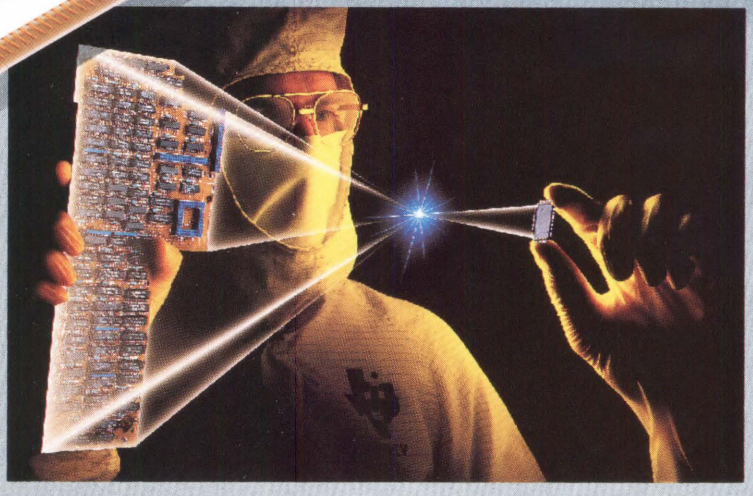
Package options include conventional through-hole DIPs, surface-mount PLCCs, and plastic quad flatpacks (QFPs) in both JEDEC and EIAJ standards, as well as high-pin-count plastic pin-grid arrays.

Both the TGC100 and TSC500 Series have a typical propagation gate delay of

logic. TI offers advanced logic families



Major logic consolidation, the equivalent of 252 MSI and LSI devices, was possible using the seven TI ASIC functions shown above the microExplorer™ board which brings symbolic processing to a MacIntosh II® desktop computer.



480 ps for a two-input NAND gate with a fanout of three; flip-flop toggle rates range up to 208 MHz. Both series offer output and bidirectional buffers with variable slew-rate control. And both series are fabricated in TI's high-performance EPIC process.

Apply TI's advanced logic to improve the performance of military systems.

Among TI's broad selection of logic devices produced to military requirements is a large PAL family. Propagation delays as fast as 15 ns are available over the military temperature range. The introduction of a 12-ns, 20-pin PAL circuit is planned, as well as military versions of the TIB825S105B and '167B Programmable State Machines.

TI is offering military counterparts selected from its ACL family, as well as 54F functions. Soon to come will be the BiCMOS family of bus-interface functions.

Included among TI's lineup of military ASICs are versions of the one-micron TGC100 Series gate arrays discussed at left, as well as two-micron standard cells.

TI's logic devices are among the more than 800 military functions offered compliant to MIL-STD-883C, Class B. Of this total, TI provides more than 200 to DESC-standard military drawings and is qualified to supply 285 JM38510 Class B devices (QPL 75).

THIRTIETH ANNIVERSARY
1958 1988
INVENTION OF INTEGRATED CIRCUIT

Milestones in Innovation

TI's tradition for milestone innovations extends from the infancy of semiconductor technology into the MegaChip Era. Among the major highlights:

- First commercial silicon transistor (1954)
- First commercially produced transistor radio (1954)
- First integrated circuit (1958)
- First integrated-circuit computer (1961)
- First hand-held calculator (1967)
- First single-chip microprocessor (1970)
- First single-chip microcomputer (1970)
- First single-chip speech synthesizer (1978)
- First advanced single-chip digital signal processor (1982)
- First video RAM (1984)
- First fully integrated trench memory cell (1985)
- First gallium arsenide (GaAs) LSI on silicon substrate (1986)
- First single-chip Artificial Intelligence microprocessor (1987)

Turn page for more information.

Comprehensive support from TI helps you improve your design performance as you improve system performance.

To enable you to excel in designing the logic portion of your system for maximum performance, TI has compiled or is making available a wide range of design tools and aids:

PLDs: The TI PLD data book (472 pages) contains design and specification data for 78 device types. Four application notes are incorporated as a reference tool. A qualification book is available, and a state-machine design kit is forthcoming.

ACL and BiCMOS Bus Interface: TI's ACL data book (348 pages) contains detailed specifications and applications information on the members of the one-micron ACL family. The ACL designer's handbook (299 pages) spells out the technical issues confronting advanced-logic design engineers and describes methods for handling the issues. A qualification book (358 pages) features extensive reliability and characterization data, die photos, and application derating factors. Customer evaluation capability is enhanced by TI's system evaluation board (available for demonstration through TI field sales offices) and third-party characterization boards.

Data sheets are available on each member of TI's BiCMOS bus-interface family.

ASICs: The TGC100 Series Design Kit gives you the tools needed to successfully complete a gate-array design: A macro library for Daisy or Mentor engineering workstations containing the graphic symbol and functional and simulation models for each macro; a software library of TI-specific software tools that streamline and simplify the design process; a design manual that answers "how to" questions about designing with the TGC100 Series; a two-volume data manual providing detailed specifications for each macro in the TGC100 Series software library; and a software user's manual.

An equally comprehensive design kit for the TSC500 Series is currently in development.

Extensive design support available for TI's systems logic families includes that for the new TGC100 Series gate arrays *(at top)*, Programmable Logic Devices *(at left)*, and Advanced CMOS Logic.

For more information on TI's advanced systems logic ICs and their support tools, complete and return the coupon today. Or write:
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P.O. Box 809066
Dallas, Texas 75380-9066

SDVØ83VD8ØØC

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Yes, please send me the following:
RYØ1 ____ ASIC Information Packet
DZØ1 ____ Programmable Logic Device Data Book
CAØ1 ____ ACL/BiCMOS Information Packet
CBØ1 ____ BiCMOS Data Sheet Packet

NAME

TITLE

COMPANY

ADDRESS

CITY STATE ZIP

AREA CODE TELEPHONE EXT.

TEXAS INSTRUMENTS

CUSTOM/SEMICUSTOM IC VENDORS

This short form directory lists vendors offering custom and semicustom gate array and cell-based ICs in a variety of fabrication technologies. If a vendor offers a particular technology, there will be a two number entry under this category. For example, if 240/14k is listed under "CMOS(SI-GATE, ME-GATE)" in the Gate Array Fabrication Technologies directory, the vendor's fabrication facility can deliver silicon- or metal-gate CMOS arrays with flip-flop toggle rates up to 240 MHz, and gate densities to 14,000. If 25/110 is listed under the "BIMOS" category for Cell Library Fabrication Technologies, the vendor can supply BiMOS chips with toggle rates to 25 MHz, and has 110 standard cells in this library. For more details see *VLSI Systems Design's 1988 Semicustom Design Guide.*

DIRECTORY OF GATE ARRAY FABRICATION TECHNOLOGIES

COMPANY	BICMOS	BIPOLAR (CDI, DI, I^2L, JI, OI)	BIPOLAR, ECL (OI)	BIPOLAR, ANALOG DIGITAL/JFETS (JI)	BIPOLAR, ECL/ CML (JI)	BIPOLAR, STTL/ TTL (OI)	CMOS (SI-GATE, ME-GATE)	CMOS, SOS (RAD-HARD)	GAAS, D-MESFET	GAAS, E/D-MESFET	NMOS
ACTEL							70/2k				
AMD			650/ 4988			560/ 5228					
APP. MICRO CIRC.		*	800/5k			800/5k	240/14k				
AT&T		250/670	600/6k			600/6k					
BARVON		100/2k					100/2k				
CALIFORNIA MICRO							30/10k				
CHERRY SEMI.		3/288									
COMMODORE							80/6k				
CONTROL DATA							75/20k				
CUSTOM ARRAYS		n/s/1.4k									
CUSTOM SILICON		350[1]/369					175/ 104,832				
DATA LINEAR		0.5–1 GHz[1]/ 347									
DESIGN DEVICES							150/ 129k				
ELECTRONIC TECH.		n/s/n/s				1/298	65/5k				
EXAR				1 GHz[1]/ 800							
FORD										1 GHz/ 3k	
FUJITSU	250/ 11,968	180/ 3240	1k/9856			150/ 3162	180/ 3240				
GAIN										1k/7k	
GE MICRO.							40/13.5k				
GENESIS							100/15k				
GENNUM				200/280							
GE SOLID STATE							250/54k	10/1.2k			
GOULD							100/14k				
HITACHI	100/ 2550						100/ 2550				
HOLT							20/255				
HONEYWELL		600/12k					50/40k				
HUGHES AIRCRAFT							200/41k				
ICI ARRAY							40/2650				
INTEGRATED CIRC.							85/66k				
INTEGRATED CMOS							50/ 30,380				
INTEGRATED LOGIC							150/ 100,512				
INT. MICROCIRCUITS							100/8k				
IMP							40/15k				
LSI LOGIC	n/s/43.5k						n/s/100k				
MARCONI							100/ 10,044	60/4048			
MATRA DESIGN							45/7.5k				
MCE				50/592			5/984				
MICREL		40/200					40/200				
MICRO LINEAR				100/ 1816							
MICRO LSI							90/3.5k				
MIETEC		40/n/s					60/n/s				
MITSUBISHI							175/20k				
MOTOROLA			>1k/ 10,332			>150/ 2860	>150/ 104,832				

* Bipolar, Trench Isolation; 1 f_T

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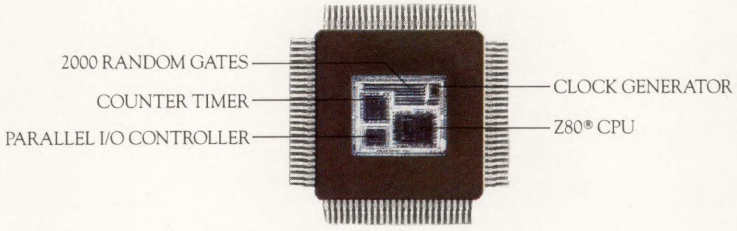
BOOTH NO. 1388-1397.

Leader Of



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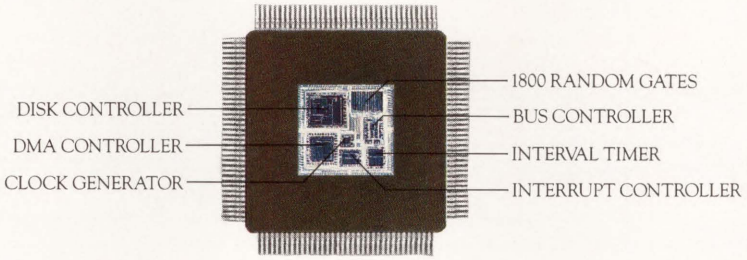

PACKAGE: 144 PFP, 25 MIL CENTERS*

*Die shown larger than actual size.

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MAS-88-001

DIRECTORY OF GATE ARRAY FABRICATION TECHNOLOGIES (continued)*

COMPANY	BICMOS	BIPOLAR (CDI, DI, I^2L, JI, OI)	BIPOLAR, ECL (OI)	BIPOLAR, ANALOG/ DIGITAL/JFETS (JI)	BIPOLAR, ECL/ CML (JI)	BIPOLAR, STTL/ TTL (OI)	CMOS (SI-GATE, ME-GATE)	CMOS, SOS (RAD-HARD)	GAAS, D-MESFET	GAAS, E/D-MESFET	NMOS
NATIONAL SEMI.			1.8k/15k				200/10k				
NCM		40/296					18/780				
NCR							85/8.5k				
NEC		300/20k	1.7k/ 4.4k				300/20k				
OKI							80/ 30,384				
PANASONIC							200/ 20,064				
PLESSEY		250/10k	2k/4.5k	n/s/213			100/ 10,044				
POLYCORE				n/s/280							
RAYTHEON		150/5k	1k/12.8k			25/300	40/ 10,013				250/ 5670
SILICONIX							10/2.4k				
SILICON SYSTEMS		25/712			>100/168	>100/n/s	25/712				
SILICON WEST							100/10k				
S-MOS SYSTEMS							120/ 38,550				
TEKTRONIX					500/300						
TEXAS INSTRUMENTS							150/ 18,620				
TLSI							40/4012				
TOSHIBA							200/ 129,042				
TRIQUINT										1k/4.2k	
UNICORN							30/3060				
UTMC							250/11k				
VITESSE									2k/1.5k	2k/1.5k	
VLSI TECHNOLOGY							250/54k				
VTC		250/572					200/6k				
XEROX			1.8k/15k				200/10k				
XILINX							70/9k				

DIRECTORY OF CELL LIBRARY FABRICATION TECHNOLOGIES

COMPANY	BICMOS	BIMOS	BIPOLAR (DI, JI, OI)	BIPOLAR (DI-ANALOG)	CMOS	CMOS, ME-GATE	CMOS, SI-GATE	CMOS, SOS (SI-GATE)	GAAS, D-MESFET	GAAS, E/D-MESFET, FET	NMOS
ABB HAFO						10/100	110/85	150/75			
ADAMS RUSSELL									n/s/>50		
AT&T							170/304			n/s/30	
BARVON	100/195						200/444				
CALIFORNIA MICRO							150/140				
COMMODORE							80/80				
CONTROL DATA							166/86				
CUSTOM ARRAYS			n/s/30								
CUSTOM SILICON							110/216				
DATA LINEAR				1 GHz[1]/ Many							
DESIGN DEVICES							150/180				
ELECTRONIC TECH.							75/86				
EXAR							100/182				
FUJITSU							120/168				
GE MICRO.							40/220				

* Bipolar, Trench Isolation; 1 f_T

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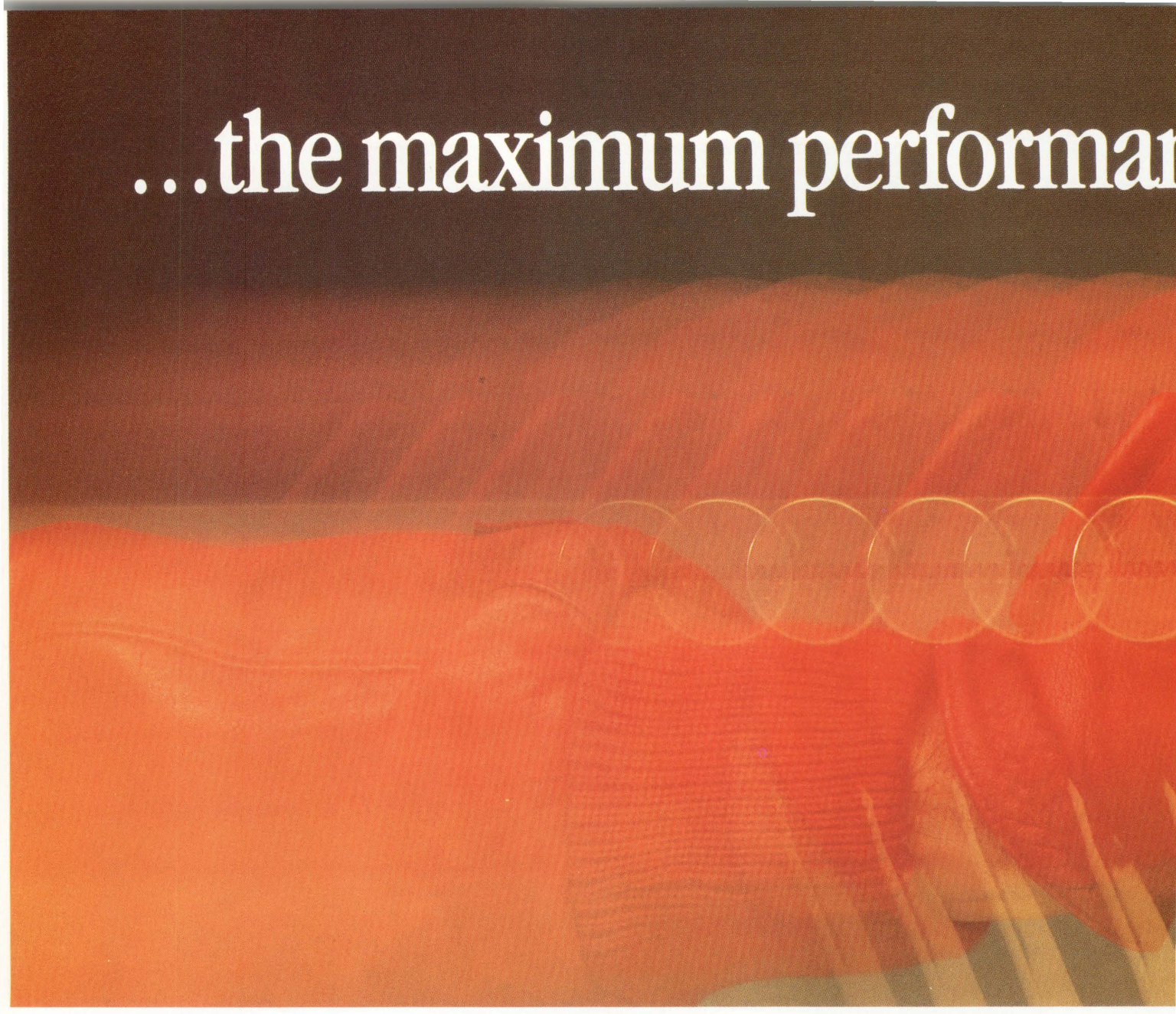

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Our broad range of ASIC products has grown to the point where we are now able to meet all the needs of ASIC users. We offer a full ASIC product range with a variety of options for digital, analog and mixed analog/digital applications, in gate arrays, standard cells, and full-custom. Advanced, state-of-the-art processes in fine geometry, high-density CMOS, bipolar and ECL technologies give you the highest levels of performance and system integration available today.

Plessey - Unparalleled CAD Support

The Plessey Design System (PDS) is a comprehensive suite of software embracing the design, simulation and implementation of gate arrays, standard cell and compiled ASICs in CMOS and bipolar technologies.

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nce that gives you the edge.

PLESSEY KEY PROCESS TECHNOLOGY

BIPOLAR

DESCRIPTION	f_t	EMITTER WIDTH	METAL LAYERS
Industry standard	400MHz	14μm	1
High voltage	400MHz	20μm	1
High speed linear	4.5GHz	4μm	2
High speed digital	6GHz	3μm	2
Ultra-high speed	14GHz	0.6μm	3

MOS

PROCESS FAMILY	fCLOCK	MINIMUM FEATURE	VSUPPLY
KC Industry standard CMOS	20MHz	4μm	3-10V
JG Double SiGate NMOS	10MHz	6μm	9-18V
VB High speed CMOS	40MHz	2μm	3-5V
VJ Very fast CMOS	50MHz	1.5μm	3-5V
VQ Ultra fast CMOS	75MHz	1.2μm	3-5V
MH/MA SiGate CMOS	30MHz	4μm	3-15V

BIPOLAR (CDI)

PROCESS	EMITTER WIDTH/ FEATURE SIZE	GRID PITCH	MAX. SPEED	MAX. POWER	MIN. POWER
ORIGINAL CDI	5μm				
CDI FAB I	3.75μm	11.5μm	10ns	2.4pJ	1.5pJ
CDI FAB IIa	2.5μm	8μm	4ns	1.2pJ	0.8pJ
Geometry change (utilizing multi-level differential logic-DML)					
CDI FAB IIb	2.5μm	8μm	800ps	0.8pJ	0.54pJ
CDI FAB III	1.5μm	6μm	400ps	0.4pJ	0.27pJ
CDI FAB IV	1.2μm	4.5μm	200ps	0.2pJ	0.14pJ

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Complementing the standard IC family, Plessey manufactures a complete line of discrete components including FETs, transistors and diodes available in SOT-23 and TO-92 packages.

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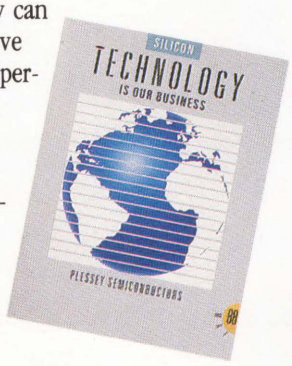

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PLESSEY

Number 1 for **ASICs**

CIRCLE NUMBER 13

DIRECTORY OF CELL LIBRARY FABRICATION TECHNOLOGIES (continued)

COMPANY	BICMOS	BIMOS	BIPOLAR (DI, JI, OI)	BIPOLAR (DI-ANALOG)	CMOS	CMOS, ME-GATE	CMOS, SI-GATE	CMOS, SOS (SI-GATE)	GAAS, D-MESFET	GAAS, E/D-MESFET, FET	NMOS
GENESIS							85/294				
GE SOLID STATE							100/266	15/56			
GIGABIT LOGIC									2300/35	3000/31	
GOULD							100/740				
HARRIS							150/188				
HOLT							15/100				
HUGHES AIRCRAFT							50/170				
INTEGRATED CIRC.							80/138				
INTEGRATED CMOS							50/127				
INTEL							65/112				
INT. MICROCIRCUITS						2/n/s	100/ 8000				
IMP							80/76				
LSI LOGIC							n/s/>900				
MARCONI							60/133	70/81			
MATRA DESIGN							45/126				
MCE			50/10			5/113	10/60				
MICREL			40/64				40/64				
MICRO LSI							90/111				
MICRO-REL		25/110	n/s/30				25/n/s				
MIETEC			40/52				60/156				
MITSUBISHI							100/269				
NATIONAL SEMI.							110/368				
NCM						5/52	18/59				
NCR							120/187				
NEC ELECTRONICS							250/385				
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CUSTOMIZING IMAGE PROCESSOR CHIPS WITH PLDs

BOBBY SAFFARI AND PAUL T. SASAKI, SIGNETICS CO.,
DIVISION OF NORTH AMERICAN PHILIPS CORP., SUNNYVALE, CALIF.

■ PROGRAMMABLE LOGIC DENSITIES AND PERFORMANCE CHALLENGE GRAPHICS APPLICATIONS ■

IN THE AREAS of image processing and graphics, intensive software and hardware design efforts have become necessary to satisfy increasing demands for performance. These demands have forced designers to use either specialized parts or user-designed (i.e., semicustom) ICs. Each method has its advantages and disadvantages.

Specialized graphics ICs provide hardware specifically geared to the designer's class of application. This solution generally involves the use of a programmable processor coupled with surrounding chips. The designer tailors the device to his system requirements by writing algorithms or graphics primitives (or both) in software for the processor. A programmable processor gives the designer the freedom to change his design during the later stages of his design cycle. With this approach, however, the designer must be extremely careful in the selection of devices to maintain a high level of throughput. Also, the code must be carefully written to guarantee the required performance.

These disadvantages could be circumvented by using a semicustom solution. This approach, however, entails an NRE charge and the possibility of a relatively long design cycle. These problems could be compounded if a designer is forced to start his design without having fully determined his design requirements just to avoid a late entry into the marketplace. Fortunately, another user-designed alternative—programmable logic—has achieved levels of density and performance sufficient for graphics and imaging functions.

Until recently, most PLD architecture had usable gate counts of under 600. They were excellent at consolidating random logic but could not implement whole functions, as gate arrays could. Smaller PLDs have been fast enough to meet the necessary requirements of graphics and image processing systems, but too many PLDswere called into play, consuming both board space and power. Those PLDs that had sufficient density to integrate complete functions were generally too slow.

The introduction of dense, high-speed PLDs finally makes programmable logic appropriate for graphics and image-processing functions. To demonstrate the use of such large PLDs in graphics and imaging systems, a member of the Signetics Programmable Macro Logic family—the PLHS502 (see sidebar)—is used to implement two specific functions: sort processing and morphology processing. The second function, in fact, has been implemented and placed on a frame-buffer board. Using Optivision image-processing software from Automated Visual Inspection, a specimen—an image called a Chinese hamster—was used to demonstrate its operation (Figure 1).

■ SORT PROCESSOR

The first function, the sort processor, is used primarily to search large databases. Sort processors are useful in graphics and imaging

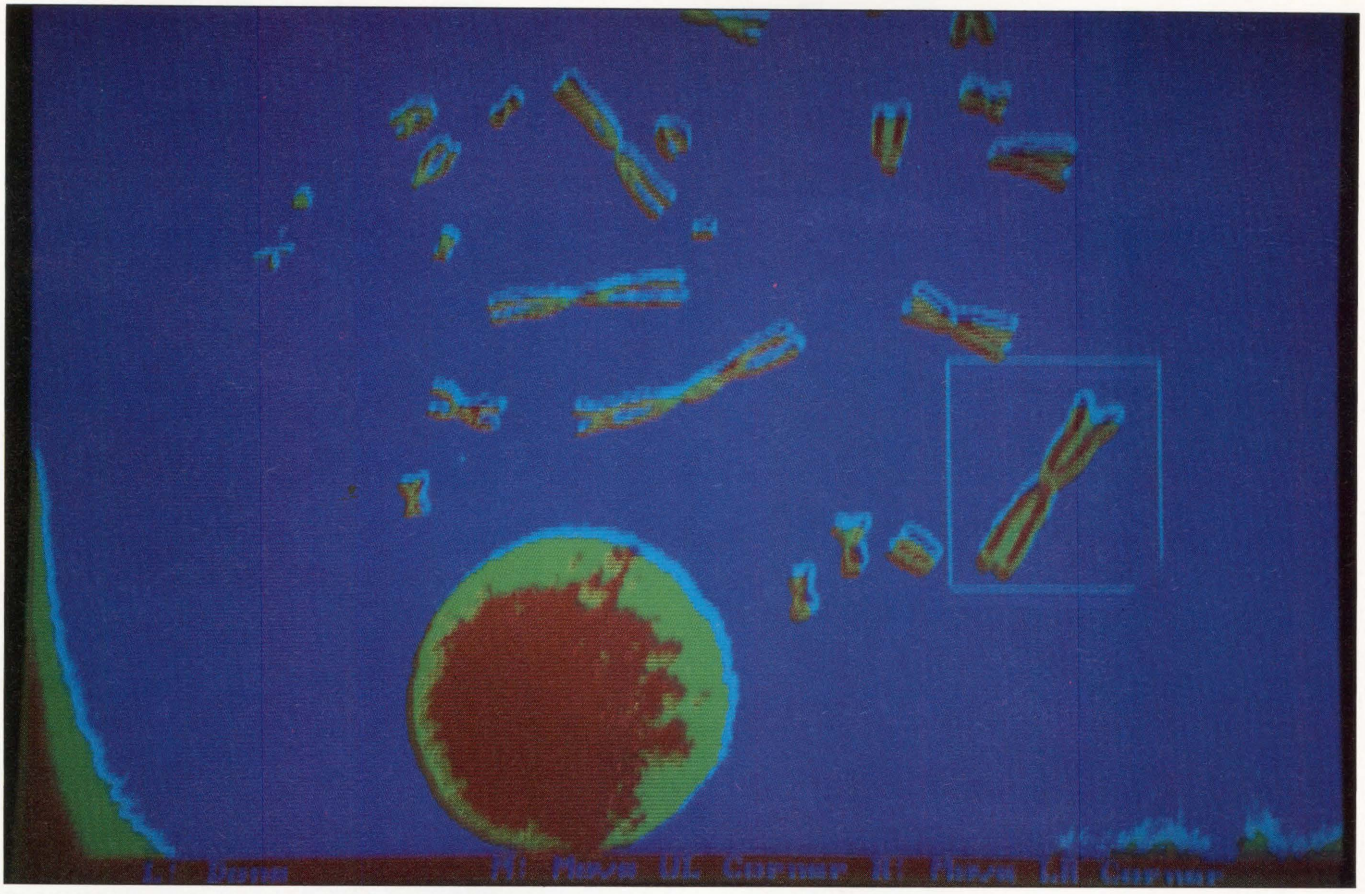
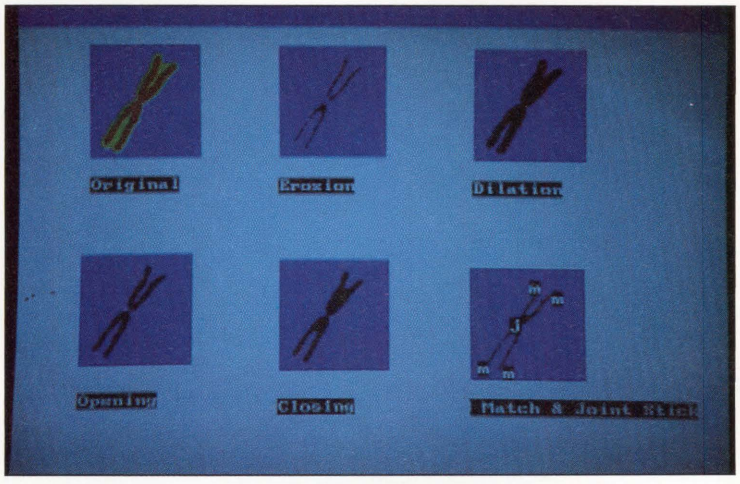


Figure 1. Morphology operations, a subset of image processing, submit a video image (a above) to a structuring element that processes it according to its shape, resulting in new forms for the image (b below).

when items in a database represent such data as color, intensity, or the shape of an object. Graphics systems display the data as images for the purpose of human interaction. Image processing, on the other hand, extracts facts about an object and analyzes them based on some type of criteria. Even though image processing and graphics sound distinct, they share many similarities. Both operate on picture elements (pixels) and both use the same basic hardware architecture. A dedicated graphics chip, such as a sort processor, can therefore be applied to some areas of image processing.

This sort processor example provides the minimum and maximum of a set of data inputs. This type of function is very useful for enhancement and analysis routines in image-processing systems and for special effects in graphics systems. As an example of image enhancement, median filtering is a process in which scattered random noise throughout the image is removed or reduced by statistically comparing each pixel with its closest neighbor. This operation



USING PROGRAMMABLE DEVICES REDUCES THE PENALTY OF CHANGES LATE IN THE DESIGN CYCLE

"cleans up" an image without blurring the sharp edges. The sort routine would be used to rank the pixels, then another routine could examine each value to see which ones were in the neighborhood. Since the values would be ordered, only the extremes of the set would have to be examined.

Image analysis, such as edge detection, constitutes another group of image processing routines that could benefit from dedicated sort-hardware. Edges are normally associated with the high frequency components of signals present in an image. In edge detection, the original image is typically convoluted with a template whose coefficients suppress the low frequency component of the signal. The maximum edge magnitude generated by these operations would be selected to indicate the presence of the best edge. Sort operations could examine the edge magnitudes generated by different convolutions and select the maximum magnitude for that pixel location.

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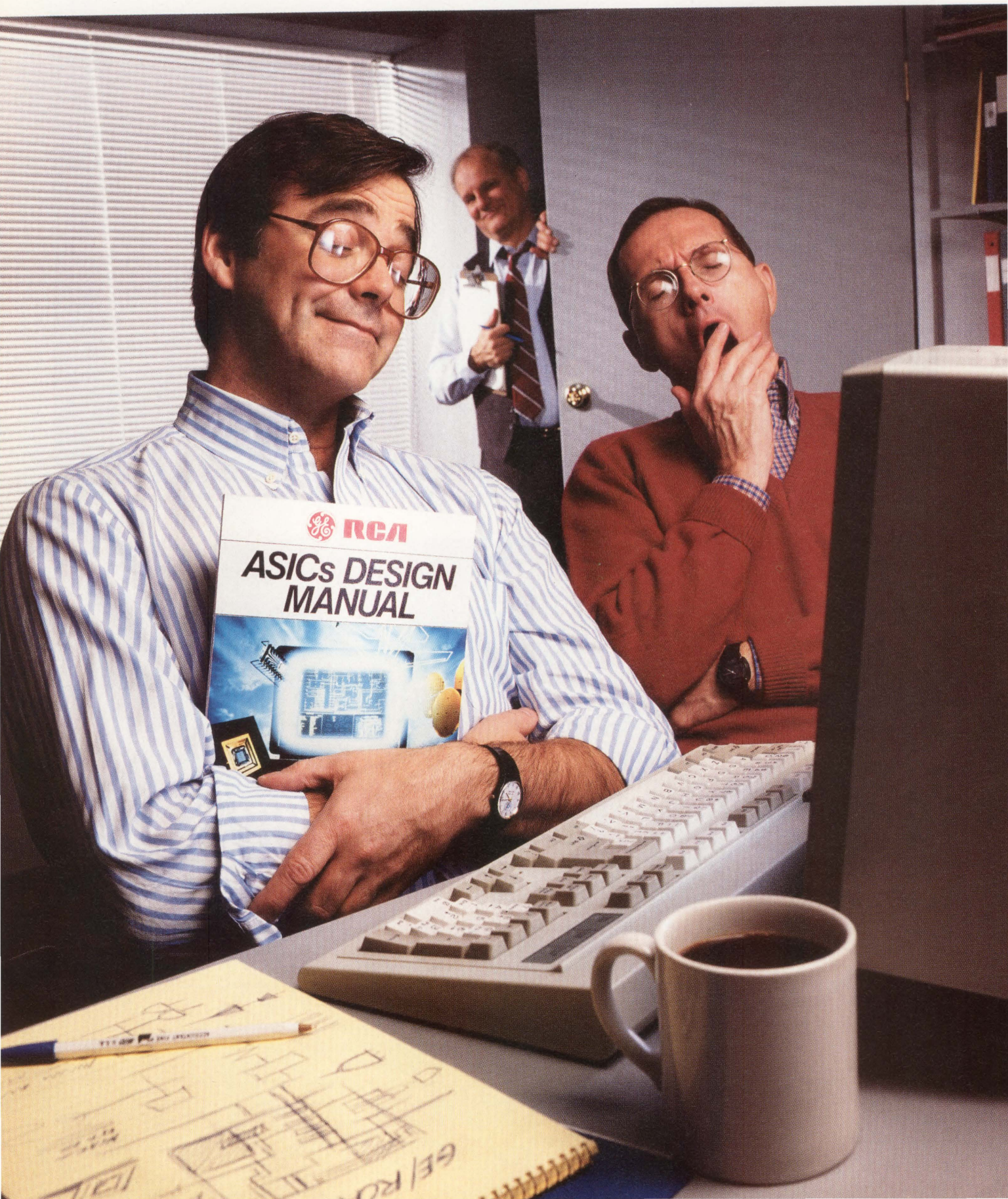

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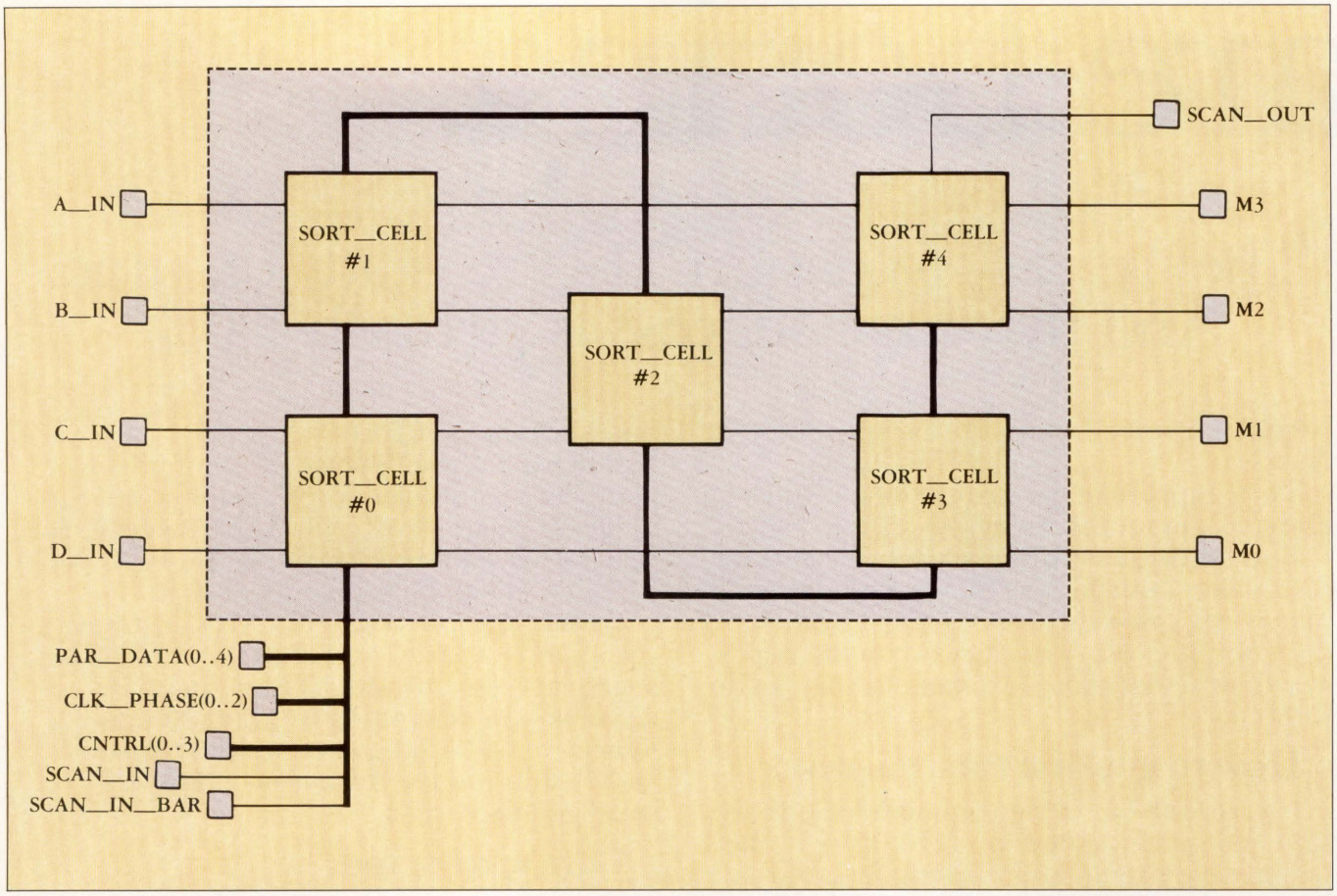

Figure 2. The PLHS502-based sort processor uses multi-level pipelining and parallelism to implement a binary "compare and exchange" concept know as a bubble sort.

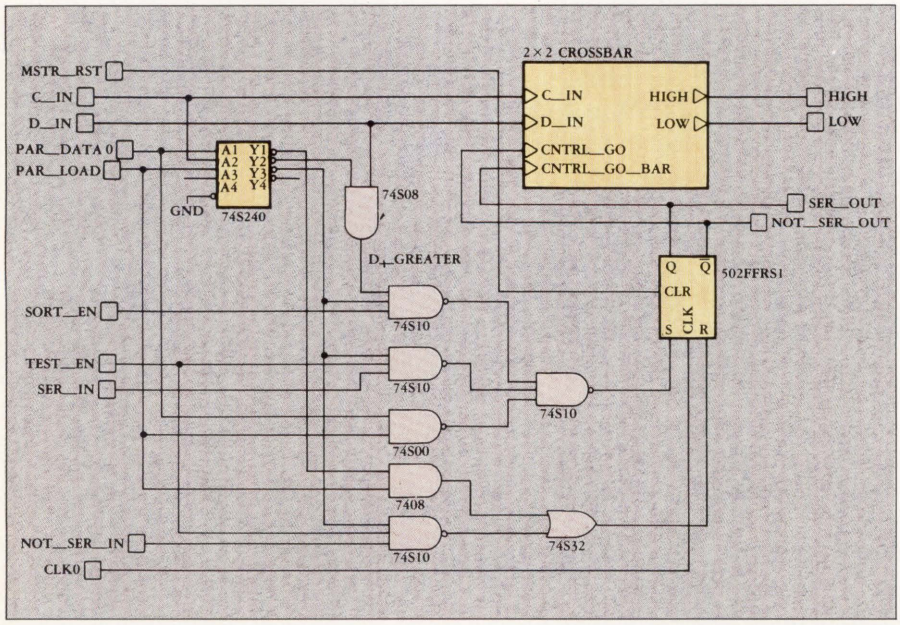

Figure 3. The sort cell uses a gated magnitude comparator to compare two pieces of data and a crossbar switch to direct the data to the appropriate outputs, based on their magnitudes.

Sort operations also have many uses in graphics applications. Pixel manipulations, for example, can use the sort routine to find the minimum or maximum values for a group of pixels. Consider a yellow circle that could be placed on a red triangle with a blue background. These objects can be ordered so that some appear in the front while the others appear behind. If two bright objects overlap each other and they are color coded, they could create a "hot spot," or saturation point, as the color values are added. As a result, the objects become indistinguishable. A sort processor can select objects for the background or foreground, thus allowing objects to be smoothly combined.

■ Parallel Pipelines

The PLHS502-based sort processor uses multilevel pipelining and parallelism to achieve a high computational throughput (Figure 2). It can be considered to have a SIMD (Single Instruction Multiple Data) architecture. The processor sorts any four serial random numbers that are shifted into the device from their most significant bits (MSB) to their least significant bits (LSB). By feeding results back into inputs, cascading this design creates a processor with no restrictions on the word size.

The algorithm used for the logic implementation of this device is based on a binary "compare and exchange" concept know as a bubble sort. The total function can be divided into smaller identical modules called cells to form a systolic array. Four serial bits of data enter through the input ports A—IN, B—IN, C—IN and D—IN. The clock CLK—PHASE[0:2] and control lines CNTRL[0:3] dictate the operation of each cell. Sorting takes place "bit serially" and is pipelined at the bit level.

Each sort cell consists of a gated magnitude comparator and a cross-bar switch (Figure 3). Once two serial pieces of data enter the sort cell (through C—IN and D—IN), it compares them and directs the

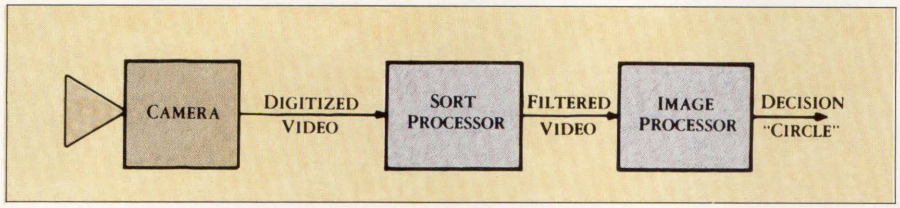

Figure 4. In a typical graphics application -- image recognition and scene analysis for robotics -- the sort processor can be used as a high pass filter to perform edge extraction, simplifying the task of the image processor.

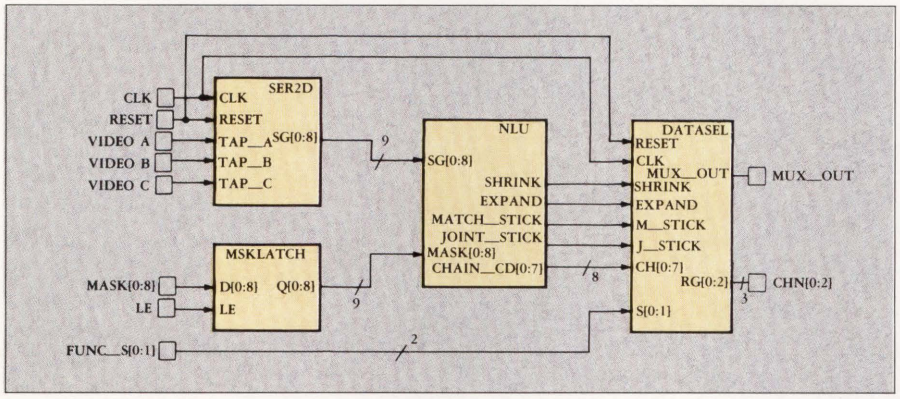

Figure 5. The morphology processor generates 9-bit neighborhood information (in block SER2D) and performs morphology functions in the NLU based on the structuring element help in the mask latch (MSKLATCH). A data selector module (DATASEL) routes the completed data to the image processor.

larger number to the upper output channel (high) and the smaller number to the lower channel (low). The CLK0 input controls the timing of the sort modules. The supporting PLD design software called SNAP (see sidebar) allows a designer to implement these functions by either schematic entry or Boolean equations.

The logic necessary for the main sort module and cross-bar switch is ideally implemented in the foldback gates. Since everything is buried, a high level of speed—clock speeds of up to 50 MHz—can be obtained. To reduce the number of delay flip-flops required for synchronous operation, a multiphase clock scheme is used to generate the proper timing for sampling the data at the appropriate time intervals.

■ Adding Testability Features

The other inputs, such as SCAN—IN (Figure 2), are used for testing purposes. Testability features were also added that would bypass the normal system clock and provide a scan path to test the logic. The testing circuitry enables the sort cells, and can load data either in parallel or serial. A test clock is then used to clock the data out. This circuitry is shown in the figures but for the sake of brevity is not discussed in detail.

Timing and control logic compromises a companion module necessary for the sort processor. The 502 PLD's combination of D and RS flip-flops make it very easy to implement not only the counters but the synchronization and arbitration logic. Since a pipelining feature is used, the timing generator separates the master clock (MSTR—CLK) into four clock signals, and controls whether the master clock or test clock (TEST—CLK) is used.

Figure 4 shows how the sort processor could fit into a typical graphics application—image recognition and scene analysis for robotics. This application can be used by a robot to either sort parts by type or remove defective parts in an inspection system. The camera of the robotics system looks at the image of the parts. The digitized data would then normally be processed by the image processor to determine the type of object. The sort processor can be used as a high pass filter to perform edge extraction, simplifying the task of the image processor. The sort processor off-loads the image processor and speeds up the overall response of the system.

■ Morphology Processor

The binary morphology processor is another custom processor useful for high-speed image-processing systems. This example of such a processor, based on the PLHS502, performs morphology operations such as dilation, expansion, and chain coding. To understand the design, a brief discussion of morphology is appropriate.

Mathematical morphology, or shape analysis, provides a method of processing digital images based on their sizes and shapes. It's particularly suited for tackling problems in machine vision applications

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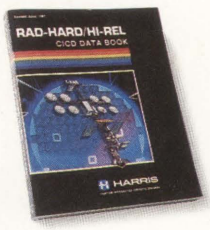

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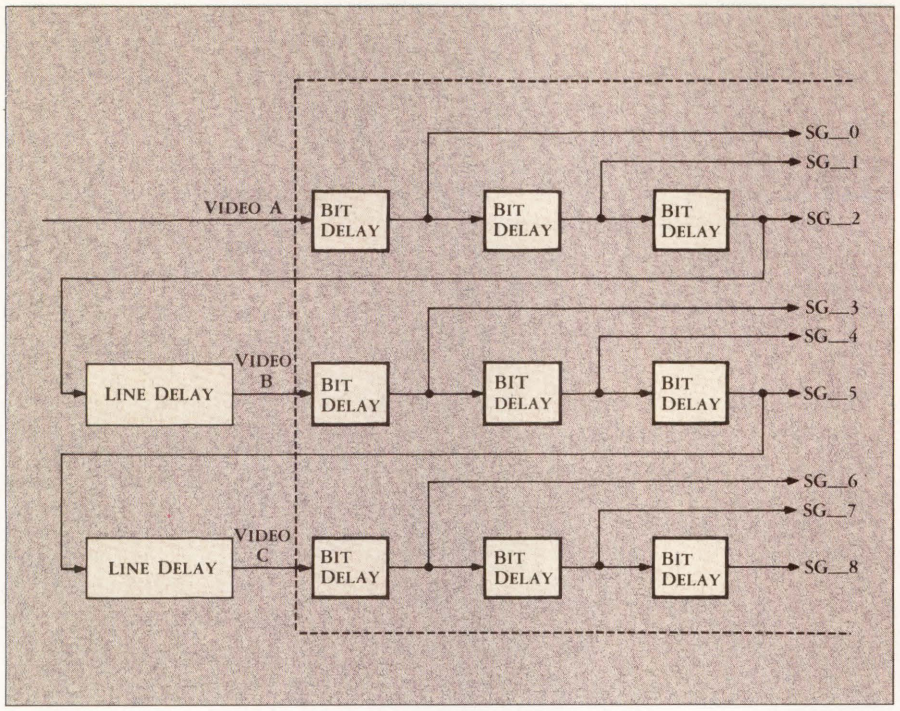

Figure 6. Module SER2D accepts three video signals, two of them delayed versions of the original, that form a 3 X 3 array of pixels called the neighborhood. The neighborhood is passed in a parallel fashion to another module as input for the morphology operations.

such as parts inspection and medical image enhancement. In morphology, the basic tool is to use elementary patterns called structuring elements. The structuring element is usually stored within the system as the set of coordinates of its points.

For the purposes of explanation, we will focus on dyadic operations which combine two images into one. For two images, possible logical combinations include the union, the intersection, and the difference of their areas. In simpler terms, these are equivalent to the logical operations of OR, AND, and XOR. Results of dyadic morphology functions presented here are shown in Figure 1.

■ Dilation and Erosion

The first two dyadic operations are dilation and erosion. Dilation is defined as the union (OR operation) of all the comparisons of the area of interest by the structuring element. Erosion can be defined as the set of points in which the structuring element fits into the area of interest. In simpler terms, dilation can be considered as expansion and erosion as shrinking.

The combination of erosion and dilation leads to two other functions in morphology called opening and closing. Opening is an erosion followed by dilation, while closing is a dilation followed by erosion. Opening is often referred to as a sizing operation. In essence it's a filtering operation that removes from the image those regions in which we cannot fit the given structuring element and leaves those that do fit. In contrast, closing is a filtering operation where an enlarged image is obtained. These operations are used for filtering the undesirable portion of an image without impacting the overall shape of the object, making them highly useful in the field of image processing.

Chain coding is another useful function in image-processing applications. An image that is represented as an array of picture elements (pixels) takes enormous amounts of storage. In robotic applications involving image recognition, the system can spend large amounts of time moving data between main memory and secondary storage devices. Chain coding mitigates this problem by representing the image only by its outline. It partitions the image into regions and uses a single entry to store the location of a first entry—the origin. Subsequent entries are numbers giving the direction between each point in the outline and its neighbor.

The binary morphology processor could fit into the same system as the sort processor. In Figure 4, the video camera sends a digitized video signal to the image processor, where a decision is made based on the results. The morphology processor can be used to take the filtered video image from the sort processor, further refine the filtering with a 3 × 3 pixel array structuring element, and then produce a chain code of the image. The image processor could compare this representation, which is much smaller than the original pixel representation, to reach a decision about the

video object. The morphology processor that is implemented also has the ability to use other 3 × 3 pixel structuring elements to perform comparisons on the video image.

The hardware implementation of these functions can substantially improve the speed and performance of any system. Unlike standard signal processing routines, these functions do not require a multiplier or an accumulator, Instead, they are logic intensive and use many logic gates such as AND, NAND, OR, and NOT. Because of its many "foldback" gates, the 502 easily implements these functions.

■ NEIGHBORHOOD WATCH

The morphology processor was designed using a modular hierarchical approach. The first of the four modules in the system (Figure 5) generates the 9-bit neighborhood information (SER2D). Another holds the mask information that represents the structuring element in a 9-bit latch (MSKLATCH). The third is a logic unit (NLU) used to generate the morphology operations and chain codes, and the last, a data selector module (DATASEL), routes the completed data to the image processor.

SER2D accepts three video signals, two of them delayed versions of the original (Figure 6). Shifted in serially, they form a 3 × 3 array of pixels (the "neighborhood"). The middle bit (SG—4) is the one of interest. The 3 × 3 pixel array then passes in a parallel fashion into the neighborhood logic unit (NLU). Both SER2D and MSKLATCH were designed with schematic capture, using flip-flop macro functions provided in the SNAP software.

The NLU performs transformations on the center pixel based on the values of the center and its eight neighbors. The morphological operations will filter the original video image. A chain code is then

Using PML is a SNAP

The PLHS502 (Figure A), like its predecessor, the PLHS501, combines buried logic with an interconnect array that allows complete freedom in connectivity. High-speed shifter circuits can be implemented in the chip's eight D-type and eight RS-type flip-flops that can toggle at rates up to 50 MHz. The PLHS502's 64 foldback NAND gates and the interconnect NAND array can readily be used to implement logic-intensive designs. These same gates can also be used to create latches or flip-flops at the inputs, or they can be "buried" inside the inner core. The clock NAND array, which accepts the outputs from each flip-flop as inputs, offers a choice of clocking strategies. Because the circuits are all buried and signal paths can remain on chip, the resulting performance is enhanced.

To fully utilize the complexity of PML, the SNAP (Synthesis Netlist, Analysis and Programming) software uses a design flow similar to that of gate arrays. Capable of running on a standard PC, the software can take a designer from basic schematic entry to programming the finished devices. The software provides a choice of entry formats: standard schematic entry, Boolean equations, state equations, or any combination of the three. Counters for timing control are best implemented by schematic entry. Multiplexers or decoders are easier to implement with equations than with schematic entry. The software will combine these methods to create a complete system. Also, SNAP includes a logic simulator with timing analysis, fault simulation, and an automatic test pattern generator.

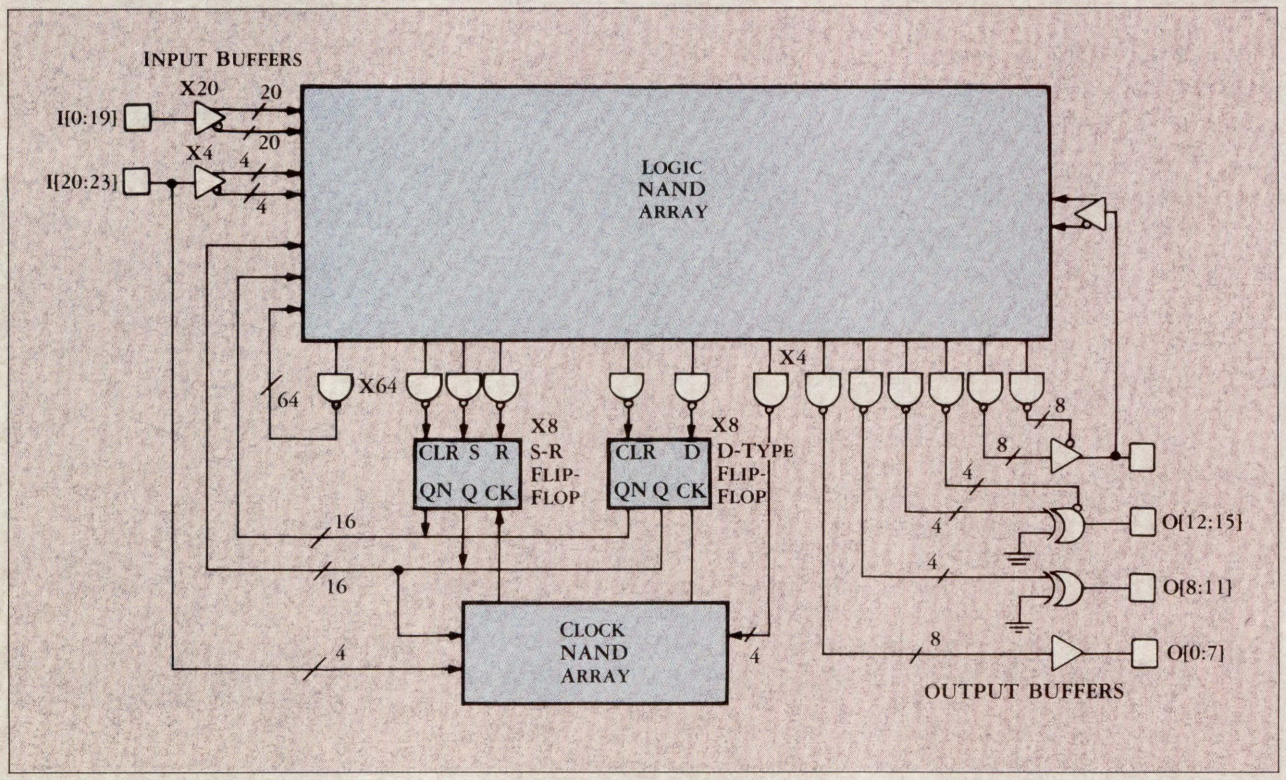

Figure A. The PLHS502 combines 50-MHz D- and RS-type flip flops with an interconnect NAND array that provides 64 feedback lines for multi-level logic.

```
SHRINK = (MASK_0 + SG_0) * (MASK_1 + SG_1) * (MASK_2 + SG_2) *
         (MASK_3 + SG_3) * (MASK_4 + SG_4) * (MASK_5 + SG_5) *
         (MASK_6 + SG_6) * (MASK_7 + SG_7) * (MASK_8 + SG_8);

EXPAND = (MASK_0 * SG_0) + (MASK_1 * SG_1) + (MASK_2 * SG_2) +
         (MASK_3 * SG_3) + (MASK_4 * SG_4) + (MASK_5 * SG_5) +
         (MASK_6 * SG_6) + (MASK_7 * SG_7) + (MASK_8 * SG_8);

JOINT_STICK = (SG_0 * SG_2 * SG_4 *SG_6 * SG_8) +
              (SG_1 * SG_3 * SG_5 *SG_7);
```

Figure 7. The morphology operations are easily implemented in Boolean equations. For example, EXPAND is nothing more than "ANDing" each individual pixel in the neighborhood with its corresponding MASK bit and combining the results with an OR operation.

created for the purpose of comparison to stored images. The results are then fed to the central processor for decision making.

The inputs to the NLU are the nine pixel bits from the video (SG[0:8]) and the nine bits from the masking image (MASK[0:8]). The data from each row of pixels from the digitized image are also used as inputs. The SHRINK and EXPAND outputs are the results of erosion and dilation operations, respectively. MATCH—STICK indicates the end-points of the skeleton (outline) of the image, and JOINT—STICK indicates where the images lineand the structuring elements cross.

■ BOOLEAN EQUATION IMPLEMENTATION

Because the module is logic intensive, it is very natural to implement this section from the Boolean equations (Figure 7). To understand why Boolean equations are used, one should consider the transformation referred to as expansion (dilation). Since this is in essence an OR function between the image of interest and the structuring element (mask), entering Boolean equations can be much easier than drawing an array of gates. EXPAND is nothing more than taking each individual pixel in the neighborhood and "ANDing" it with its corresponding MASK bit. The results are combined together (ORed) to form the final transformation. The NLU also generates the chain code which the last module, DATASEL, will convert into the directional values between 0 and 7.

The last module, DATASEL, is implemented using a mixture of schematic capture and Boolean equations. Figure 8 shows the block diagram of the module. The inputs, as discussed earlier, are the results of the chain coding and morphology operations. Control signals S0 and S1 are used to route the appropriate result of the morphology section to the image processor. This module also uses an 8-bit encoder to convert the chain code into the necessary directional coordinates and send them to the image processor.

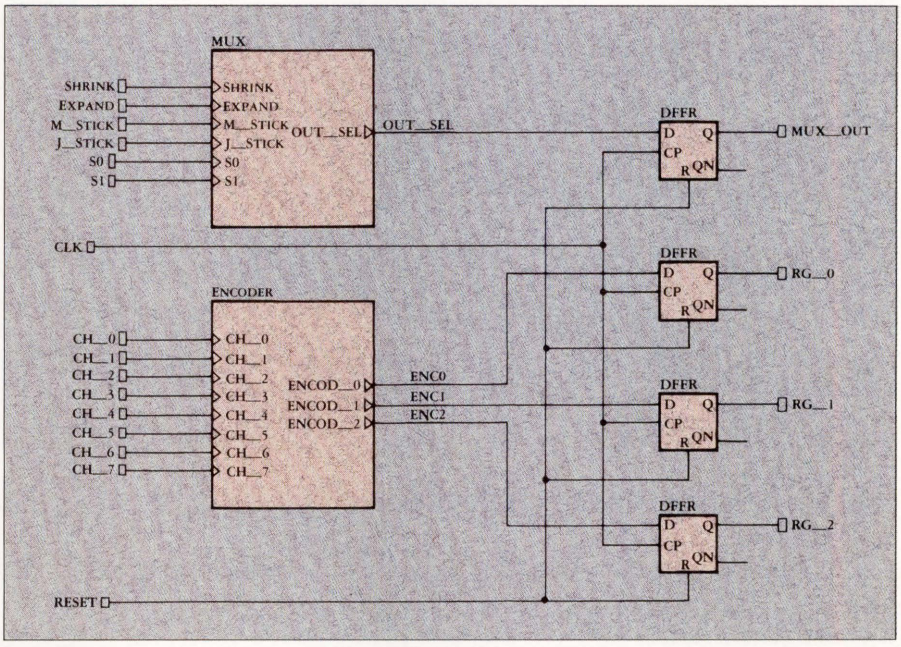

Figure 8. The DATASEL module routes the results of the chain coding and morphology operations under the direction of control signals S0 and S1. An 8-bit encoder converts the chain code into the necessary directional coordinates.

The SNAP software allows each section to be designed and individually tested for timing and logic functionality. When all modules are completed, the final operation is to merge all the sections together to complete the final design. Now a final logic simulation can be performed and the final results can be implemented in the PLHS502—which is now ready for insertion into a system. ■

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AN ENGINEERING INFORMATION SYSTEM

A DOD Standard for Integrating Design Automation Systems

DAVID SMITH, SENIOR EDITOR, VLSI SYSTEMS DESIGN

IMPLEMENTING EIS BOGGLES THE MIND

In this decade, the United States Department of Defense (DOD) has exercised its economic clout to develop some standard engineering practices. For example, it set a standard for IC processing technology through its very-high-speed integrated circuit program (VHSIC). While in the process of establishing VHDL as the defacto language standard for describing electronic hardware, the DOD is also applying its muscle to the problem of incompatible design-automation software. The results of these efforts, which will create a candidate standard for design-automation integration and management, is called the engineering information system, or EIS.

The EIS is a set of proposed standards for integrating engineering tools and managing design data; it is not a single implementation of a specific CAD system. The EIS framework consists of a set of fundamental services and a series of specifications, forming a baseline for communication and implementation. It addresses incompatibilities between engineering design tools and systems as well as the dearth of database management functions for engineering information. EIS aims to provide a framework for tool integration based on information sharing without compromising proprietary tools or corporate internal business practices.

The EIS is not used to design an electronic system. Rather, it is a complimentary information management environment in which CAD systems can function. It is a database program that addresses the incompatibilities of engineering design tools by allowing them to exchange data. However, it does not supply specific database manipulation functions; it relies on a local database management system (DBMS) to access the database.

The EIS may eventually be implemented in several different ways by many of the vendors of design automation programs. Any environment that contains all the pieces should be able to use any EIS-compatible tool or data source. Some commercial vendors are involved in special interest groups to influence the standard according to their experience. However, EIS describes the particular system that has its concepts and requirements defined in DOD documentation (Linn and Winner, 1986). It should not be used generically to describe any system with DOD-specified goals.

■ EIS HISTORY

In 1985 and 1986, the Defense Department developed the EIS requirements in response to the growing problem of engineering information management within its programs. However, since the EIS concepts had considerable potential for benefiting industry and academia as well, these groups were invited to help in its creation.

In July 1987, the DOD commissioned a three-year program to develop EIS specifications and to build and demonstrate a prototype. The EIS program is managed by the U.S. Air Force VHSIC program office at Wright-Patterson Air Force Base. Honeywell Inc., the prime contractor, is leading the development of the specifications, design and production of a prototype system, insertion of EIS technology and coordination with industry and the academic community. The present schedule calls for a definition of a specification this year,

ILLUSTRATION BY FRED OTNES

reviews of the prototype design in 1989, and an EIS prototype demonstration at the beginning of 1990.

■ THE EIS TEAM

Responsibilities are divided among EIS team members (Table 1). The Computer Corp. of America is responsible for object management and access. TRW Inc. will lead prototype acceptance testing, engineering information modeling tasks and demonstration efforts. CAD Language Systems Inc. will provide data exchange adapters. McDonnell Douglas Astronautics Co. will aid demonstration efforts and assist in EIS insertion. Finally, Arizona State University will provide workshop and training facilities and will be available to house the active prototype demonstration system.

To encourage cooperation with industry and academia, the EIS program hosted the first workshops at Arizona State University for more than 90 representatives of industry, government and academia. Five special interest groups were formed to provide input and review for following topics: the engineering information model, the object management system, the user interface system, adapters, and real-

TABLE 1. EIS PARTICIPANTS

CONTRACTORS

Honeywell Inc.
Prime contractor, leads the development of specifications, design and development of a prototype system, insertion of EIS technology and coordination with industry and academia.

Computer Corp. of America
Has responsibility for object management and access.

TRW Electronic Components Group
Leads prototype acceptance testing, engineering information modeling tasks, and demonstration efforts.

CAD Language Systems Inc.
Provides data exchange adapters.

McDonnell Douglas Astronautics Corp.
Will aid demonstration efforts and assist in EIS insertion.

Arizona State University
Will provide workshop and training facilities and will be available to house the prototype demonstration system.

SPECIAL INTEREST GROUPS (SIGs)

EIM SIG
Reviews syntax, semantics and draft model of EIM.

OMS SIG
Reviews the OMS and proposes candidate standard object models.

UIMS SIG
Focuses on how users view a system.

Scenario SIG
Devise EIS usage scenarios for EIS test and evaluation.

Adapter SIG
Evaluates EIM in regards to tools and workstations.

In addition, there are four working groups for four perspectives: the Department of Defense, design and engineering users, management and administrative users, and tool and workstation developers.

life scenarios. The representatives were also organized into working groups representing different viewpoints: DOD personnel; management and administrative users; tool and workstation developers; and design and engineering users.

By 1990, the EIS program will develop a prototype software system to demonstrate the merit of the recommended guidelines for the way engineering data is created, displayed, maintained, stored, and communicated. The prototype EIS will consist of a network of different host systems, operating systems, DBMSs, and CAD tools. All will be made compatible and interoperable through the EIS software.

■ EIS OBJECTIVES

According to Katie Rotzell, a Hewlett Packard Co. software development engineer who serves as the chairperson for the Object Management System Special Interest Group (OMS SIG), EIS differs from some commercial efforts at tool integration because it provides an "illusion of tool interoperability." Other tool-integration efforts, such as the CAD framework initiative, provide a specific framework and database that tools plug into. The EIS also contains longer-term requirements that extend beyond inter-operability, such as allowing execution of a tool to be suspended and restarted.

EIS will create a system that promotes compatibility and inter-operability between CAD tools, the data they generate, and the systems or methods used to store and group data. In addition to improving integration and portability, EIS seeks to encourage design-environment uniformity, simplify the exchange of information, and improve design management.

■ EIS TO ENCOURAGE INTEGRATION AND PORTABILITY

While it will not be a self-contained design automation system, EIS serves as a foundation for the integration of cost-effective, efficient design tools, both new and existing. In addition, it will encourage the portability of tools by providing cost-saving services and specifications. Portable tools should also enhance the portability of design databases because design data will exist independently of the tools. Independence of data from tools allows users to plug tools into a CAE system, which can immediately work with the data at hand. Tool developers will find that they won't have to support as many versions of a tool. And, more tools will be available for selection when they can be easily moved without changing them.

EIS should facilitate design information exchange. Its model for engineering data, data functions, and operations for accessing and storing data lets a variety of tools work from the same database. Any tool designed to work with the EIS specifications can access an EIS environment.

In defining an EIS environment, the issues to be considered include inter-tool interfaces, network and operating system interfaces, consistent user interfaces, standardization efforts and policies, and the migration of existing tools into an integrated EIS environment. Interfaces between the tools, database, and the underlying hardware and operating system are provided, so the same software can run anywhere. Standards for developing interfaces also allow the same "look and feel" with different software and hardware combinations.

The implementation of these policies and a database methodology support design management and the reuse of previous designs. The EIS allows controlled sharing of preliminary design data, protection of released design information, reuse of past designs, and monitoring of in-progress design methods. Implementation and enforcement of local policies allow companies to control designs however they choose.

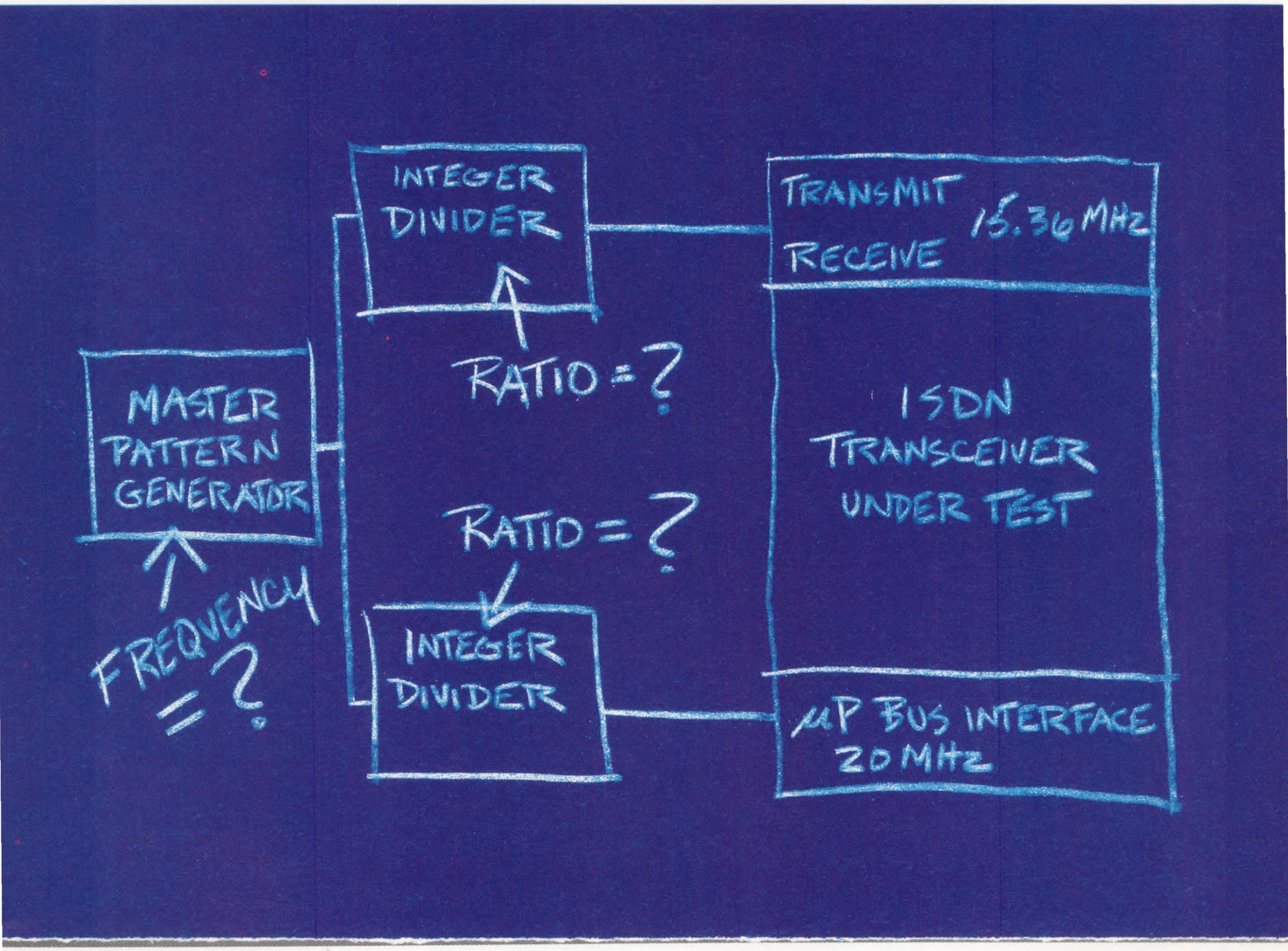
EIS will provide information management for control of data and versions of designs, for example. The system's administration functions provide the tools and specifications for managing the data dictionary, tools, workstations, user profiles, and control rules.

■ PROPOSED FEATURES FOR EIS

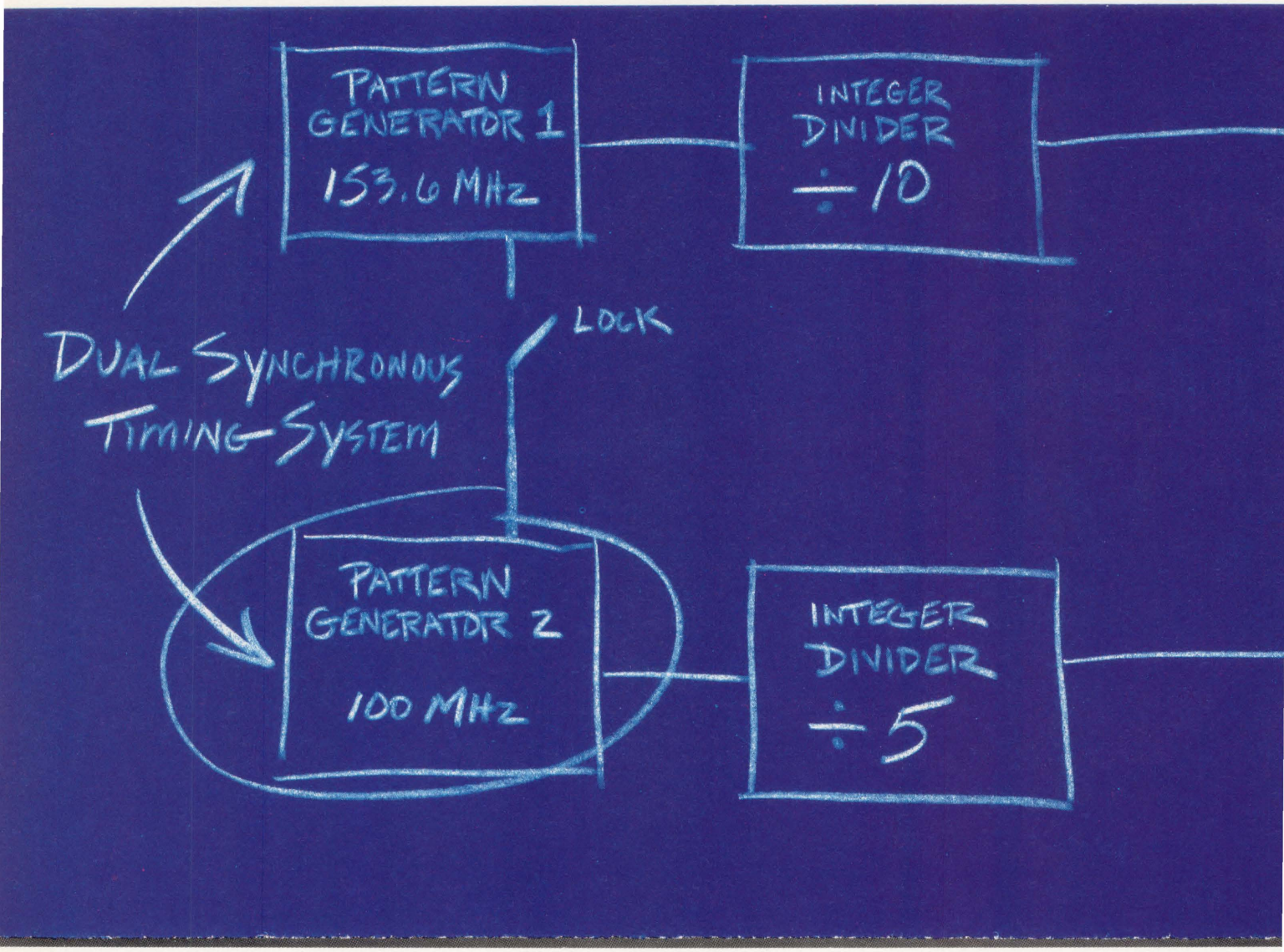
To meet all these goals, the proposed EIS will have to have the following features:

- Inter-operability—the means for the interchange and reuse of product-related information;
- External interface support—communication through standard facilities with the various interfaces required in the design process;
- A tools interface—generic facilities for input and output, translations, routing, and dialog manager services;
- Multiple host support—the ability to run on one or more diverse computers and operating systems;
- An engineering information model—a

Can you solve this problem with a one-clock telecom tester?



This ISDN transceiver requires synchronized transmit/receive data at 15.36 MHz *and* a bus interface pattern at 20 MHz. Given the tester's single master clock, what frequency do you program? What integer ratios do the dividers need?



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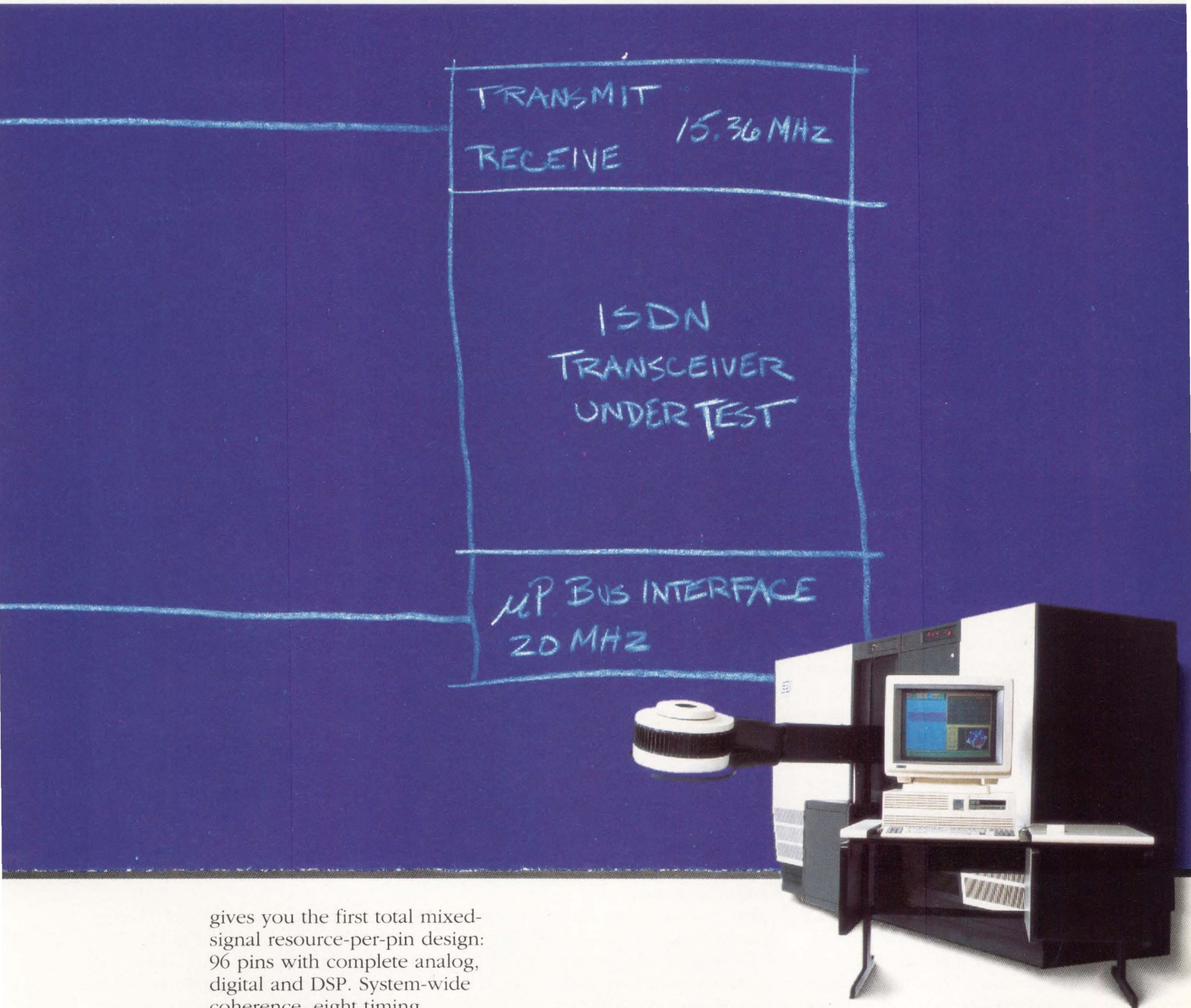

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LTX ***Responds.***

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standard for translation of engineering objects to and from different representation formats;

- An object-oriented design methodology—an approach for maximum system flexibility and extensibility;
- An Ada basis—a software standard for increased reliability and portability throughout the system; and
- Multiple languages—the ability to work with other popular languages, such as C.

■ COMPONENTS OF EIS

To provide these features, EIS has been broken up into eight interrelated components (Figure 1 and Table 2). These components, which include both static (data) and dynamic (routines) parts of the specifications of EIS, are as follows:

- The *engineering information model* (EIM). This is the formal statement of the information the EIS will track. The EIM is the cornerstone for data exchange and tool inter-operability because it gives EIS-managed information a structure and semantics. For the prototype EIS, the EIM describes electronic-engineering data, but it is extensible and can be updated to include other types of data such as mechanical and software-engineering data. According to the EIS project, the only sound way to achieve tool inter-operability is to develop a common information model.

For an engineering environment supported by EIS, the EIM provides a model of the classes of engineering information that are needed to describe the semantics of that information. The EIM won't represent engineering data itself; that is the purpose of a common exchange format like EDIF. Instead, it defines the information classes and modeling rules that form the basis for formulating a conceptual framework for information exchange.

According to Bill Johnson, the director of development at EDA Systems Inc. and a member of the EIM SIG, the EIM has an enormous number of objects and relationships to model. To reduce the total number of elements and relationships between them, some EIM objects may become attributes of others. This reduction will probably be necessary before EIM becomes a practical schema (a definition of the classes of object types and the functions relegated to a particular class).

The EIM uses three views to accommodate specific uses of the EIS-controlled data: an EDIF view for data exchange, a VHDL view for hardware modeling, and an EIS administrative view, which deals with configurations and versions. These views will be defined in terms of OMS objects and functions.

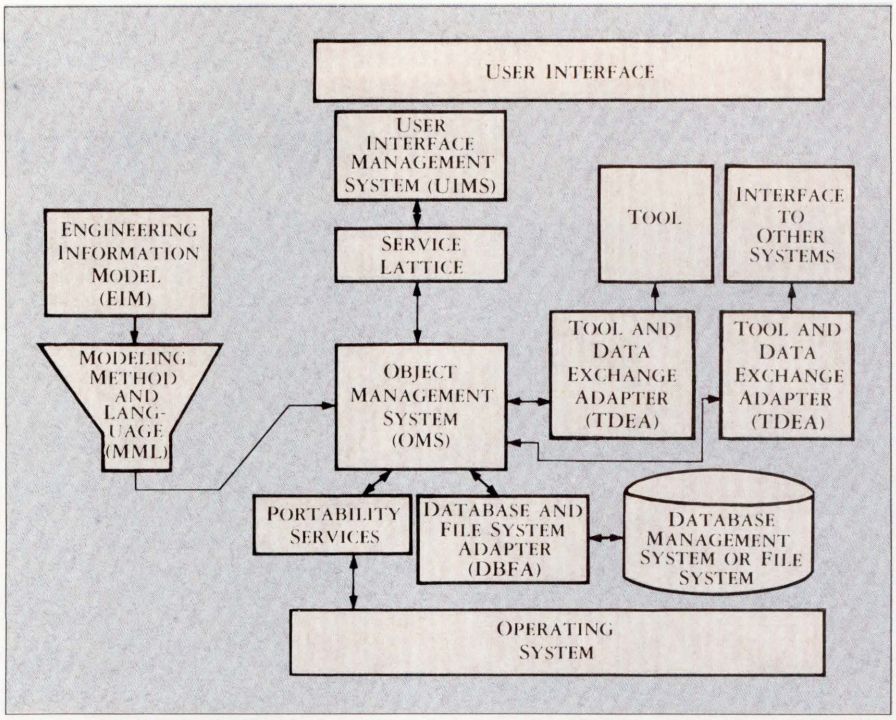

Figure 1. The eight components of the EIS integrate disparate tools, interfaces and databases, providing a common information model, object management system, and interfaces for engineering design data.

The EIM will be described in English, pictorially represented with IDEF1X-standard figures, supplemented with template descriptions and coded in a machine-executable language called OODL. It will be both stored and able to be queried in the prototype.

- The *modeling method and language* (MML). It defines a syntax for expressing the information within the EIM. It explains how to express the information in the EIM as objects, functions or types.

The MML supports abstract data types for object-oriented database management. It provides the ability to describe queries, including parameterized queries to the information described by the EIM. It must support the concept of imprecise values for properties, such as ranges, and means with standard deviation.

MML serves as a base for object-oriented data language (OODL), a modeling language being developed for EIS. OODL is an interface to underlying data servers. It can access existing database management systems and helps the incorporation of new ones.

- The *object management system* (OMS). It plans request execution and decomposes requests into steps to be distributed across DBMSs and computer systems. It consists of a functional model specification, the objects and their functions and facilities to map the model to underlying databases.

The OMS is not an object-oriented DBMS. It is the specification for the functions that the underlying DBMS must perform. This system is necessary to support EIS' object-oriented paradigm across the underlying file servers and DBMSs that may or may not be object-oriented.

It also provides a method for handling vast amounts of data in a "natural" way. Object-oriented data modeling and programming manipulate data in the same way that people mentally manipulate objects. Object-oriented programming, by making both tools and data into objects, therefore, can allow the computer to assume more information management effort.

- The *database and file system adapters* (DFSA). They translate the object-oriented expressions of the OMS into the specific query and update the data-definition languages accepted by various DBMSs or file systems. They give the user a choice of DBMSs and file systems for the OMS.
- The *tool and data exchange adapters* (TDEA). They attach tools to an EIS. They translate the requests and information from the tool into the appropriate actions by the OMS and return information from the database to the tools for processing.
- The *user interface management system* (UIMS). It allows an EIS implementer to build user interfaces, tools, terminal types, and dialog styles separately. The UIMS won't be another windowing standard, but a set of design guidelines and computer programs that guide and support development, execution, and maintenance of user interfaces. It manages the front-end capture and display of data on terminals and workstations.
- The *service lattice*. It allows the user to

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Output Drive	16 mA

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CIRCLE NUMBER 18

TABLE 2. EIGHT EIS COMPONENTS

Engineering Information Model (EIM)
Content, structure and semantics of information in an EIS.

Modeling Method and Language (MML)
Defines basic concepts of objects, functions and types to use in describing information in the EIM.

Object Management System (OMS)
Manages objects and their registration, including data, instructions, requests and operations.

Plans
Requests execution and decomposes requests into steps to be distributed across other DataBase Management Systems (DBMS) and systems.

Database and File Server Adapters (DFSAs)
Translates object-oriented expressions of the OMS into the specific query, update and data-definition languages accepted by various DBMSs or file systems.

Tool and Data Exchange Adapters (TDEAs)
Components to attach tools to an EIS.

User Interface Management System (UIMS)
Establishes guidelines and basic functions for creating consistent user interfaces.

Service Lattice
Allows user to tailor EIS services for local policies such as version control and audit trails.

Portability Services
Virtual interface between EIS and its underlying operating system

tailor EIS services for local design- and database-management policies. It provides basic services for tool builders and EIS administrators for configuration management, version control, and audit trails. The existence of the service lattice suggests that some EIS functions are not standardized, but open to various implementations. As a result, engineering efforts at each facility will be necessary to implement policies.

HP's Rotzell emphasizes the importance of the service lattice, because EIS developers use it to tailor and customize the capabilities and constraints of the EIS. It acts like a filter between the UIMS and the OMS, with restrictive policies to control the enormous number of operations possible within an EIS. It not only controls, it also simplifies by providing utilities for users to do meaningful design management.

- The *portability services*. They provide a virtual interface between an EIS and its underlying operating system. They also provide the capability to implement EIS on different operating systems and across multiple operating systems.

■ A MONSTER TASK

The EIS project will cover different hardware platforms, operating systems, tools written in a variety of programming languages, database management systems, networks, and user interfaces. Imagine trying to produce a set of standards that can guarantee data veracity and portability over such a wide range.

Some closely related to EIS are overwhelmed by its scope. "A lot of good will come of the project, but implementing it boggles my mind," said EDA's Johnson. He explains that his company's EDA framework, which already has 30 man-years of effort behind it, performs perhaps 10 percent of the functionality proposed for EIS. As EDA's framework represents a subset of the overall system proposed by EIS, the company intends to make it compatible with the standards, perhaps becoming a portion of the standard itself.

Just the OMS itself presents a major leap in CAD database technology. Most existing CAD databases have used a relational model, which stores only static information with no procedural information. The EIS, like other new database development projects, is attempting to use functional models within an object-oriented schema. Now, data is stored as objects that have clearly defined procedural behaviors (relationships or functions) between them. This approach provides clear benefits, for example, in a board design, where components have many attributes identified with them that are important for different tools.

Rotzell agrees that the EIS group "has taken on a monster task." In addition to developing significant new technology, the EIS must use some tools more appropriate for existing technology. Rotzell cites as an example of the types of drawings used—IDEF1X—which incorporate boxes to represent classes and lines to represent relationships. These drawings were developed to describe relational systems and don't have the capability to describe some of the characteristics of object-oriented systems.

■ A HEADSTART

Fortunately, some of the pieces of the EIS may already be available in the industry, such as the framework technology from EDA Systems, Cadence Design Systems Inc. and the efforts of the CAD Framework Initiative (CFI). The CFI, which includes members of EDA, Cadence and the EIS group, is also attempting to establish vendor-independent methods for allowing engineering tools to interact. Although not as complete as the EIS, particularly in the areas of object and interface management, CFI enjoys more direct input and support from the community of design automation vendors. The CFI also aims to integrate only tools for electronic design automation, eschewing mechanical and software engineering to simplify its task.

Although the first meeting of the CFI only occurred in May of this year, it's smaller scale, and more direct vendor support may result in practical implementations before the EIS prototype is up and running. In addition, because CFI members also work in EIS SIGs, EIS should be influenced by the CFI efforts, and vice versa. In the end, the efforts of EIS and CFI may be less competitive than complementary, if not redundant.

Other pieces of EIS, such as object-oriented programming and user-interface standards, are slowly emerging in CAE and CAD programming. Given awareness of the EIS program and the feedback channels of the SIGs, developers of CAE and CAD will probably mirror the technology being developed within EIS. This synergy may be the biggest contribution that the EIS project makes to most users of design automation. When EIS proposals come into consideration as standards, hopefully they will tie together existing capabilities, making integrated design environments available quickly and inexpensively. ■

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CIRCLE NUMBER 19

An Ideal Mixed-Mode SIMULATOR

GEOFFREY SAMPSON, MICROELECTRONICS DIVISION, NCR CORP., FORT COLLINS, COLO.

Truly integrated simulation tools for validating mixed analog/digital circuits are alive and thriving. In 1985, 22 percent of all semicustom IC designs combined digital and analog functions (according to The Technology Research Group Inc., Boston, Mass.), and this will jump to 39 percent by 1990. As chip density increases, the analog cells will also increase in size and complexity. But, can present-day mixed-mode simulators cope with so many large, complex, analog blocks combined with dense digital functions? In this article, we will examine the current state of mixed-mode simulation and see how close present-day simulators come to the capabilities of an "ideal" simulator. Then we will look beyond today's ideal simulator to tomorrow's "dream" simulator.

AN INDUSTRY STANDARD DIGITAL SIMULATOR CAN PROVIDE THE FOUNDATION

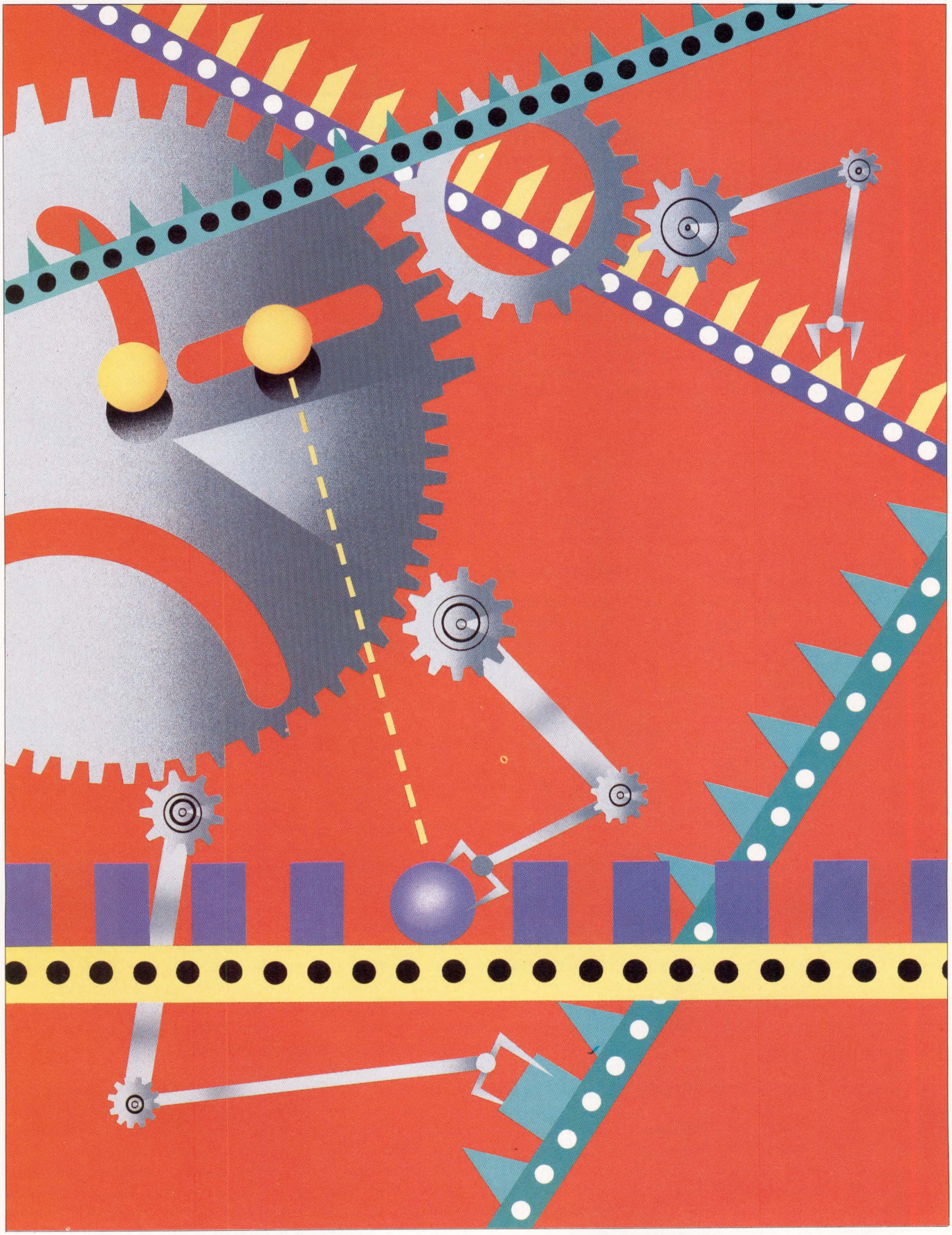
Today, mixed-mode simulation is viewed as an integration of existing analog and digital simulation techniques. The real challenge to designers of mixed-mode simulators is the interface that provides communication and synchronization between the digital and the analog sides.

In advancing towards an "ideal" simulator, a number of solutions have emerged that provide satisfactory results, albeit for a limited range of applications and needs, depending upon circuit topology and the mix of analog and digital circuits. Before discussing the ideal mixed-mode simulator we will examine some of the applications that lend themselves to these partial solutions.

■ APPLICATIONS VS. SOLUTIONS

● *Analog circuits with a few digital Parts.* Some circuits, while being essentially analog, contain some digital glue logic, such as a phase-locked loop. In this case an analog simulator that can model the digital devices at the appropriate level (gate, functional, or behavioral) will suffice. A simulator with fully integrated digital and analog simulation capabilities is not needed. These simulators combine SPICE, or a SPICE-derivative, with analog models of digital gates. The evaluation is generally two orders of magnitude slower than a digital simulator, but for an analog design with just a few digital gates it is a workable solution.

● *Digital circuits with a few analog parts.* In a mostly digital environment, analog simulator precision is sometimes required for systems that utilize charge sharing. The small number of analog parts can be modeled as digital parts, using piece-wise linear approximations, so long as the analog and digital elements are loosely coupled. Digital simulators with analog models (found primarily in foundry-specific mixed-mode simulators) handle loosely coupled analog simulation reasonably well. This kind of simulator does not deal with analog models separately from digital models. Instead, it simulates the entire mixed circuit at one time. In the process, each analog model is indepenently



INCREASINGLY COMPLEX MIXED-MODE ICS CHALLENGE TODAY'S SIMULATORS

ILLUSTRATION BY TERRY ALLEN

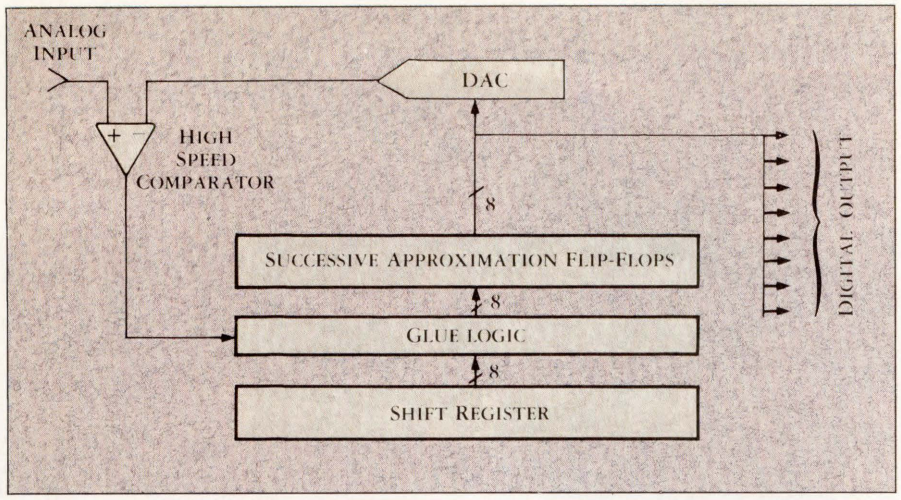


Figure 1. An eight-bit successive approximation analog-to-digital converter. Our ideal simulator should allow architectural experimentation by entering at a functional description level. Note that the feedback loop contains digital elements (glue logic and successive approximation flip-flops), an analog element (high speed comparator) and an interface element (DAC). Validating this circuit requires a mixed-mode simulator that uses hierarchy, allows mixed analog/digital/interface elements within a feedback loop, and has sufficient accuracy to demonstrate monotonicity (if true) at eight bits or better accuracy.

informed of changes at its terminals. It then responds to the changes and independently updates its terminals. Thus, an analog or mixed-analog-and-digital signal propagates through the simulated circuit by a sequence of model interactions. The processing of the models can be synchronized to handle feedback between analog and digital elements. The interaction sequence is controlled in an event-driven manner. Intelligence may be built into the analog models so that errors are flagged.

In a digital simulator with analog parts, the analog models must be custom crafted for each cell, so, unfortunately, this foundry-specific solution is not generic. Adding new analog cells is very difficult since a 10-bit A/D converter model, for example, may require thousands of lines of code. A more generic approach allows the user to write his own analog behavioral models in a high-level language like C, but this is a heavy burden for the designer. It is necessary then to have standard-part model libraries and ASIC model libraries readily available for the designer. In any case, with the digital simulator that has analog parts, the models do not contain the transistor-level detail of a SPICE simulation. Therefore the models are not as accurate . Also, behavioral models have limited ability to handle transient signals such as spikes and oscillations.

- *Circuits containing many analog **and** digital parts.* Designs incorporating extensive analog and digital elements, whose elements interact and control each other, require a tightly integrated solution. That solution must allow for both analog and digital hierarchies. Such tightly coupled electronic circuits include data converters, modems, and digitally controlled adaptive filters. Further, the ideal simulator must extend the hierarchy to include electromechanical devices so that servo control systems, for example, can be simulated.

■ Partial Solutions

Loosely coupled simulators. If both an analog and a digital simulator are available, it is always possible to run the simulations separately, and to work out the analog-to-digital or digital-to-analog interface. Traditionally this interfacing has been performed as a separate task after the simulations have been run, although there are now CAE tools that automate the translations. This approach only works for loosely coupled circuits without feedback. Still, this is a solution sometimes taken by CAE workstation vendors who have not yet achieved a tightly coupled integration.

Core solutions use just one simulator, either an analog simulator with a few digital models, or a digital simulator with a few analog models. As already discussed, it is possible to incorporate isolated models of analog components in a logic simulator, with some serious trade-offs. The inherent gate isolation of MOS devices provides decoupling between interface elements, so simulation is practical; but not so for bipolar interface elements.

Similarly, it is possible to include a few isolated digital parts in an analog simulation; but SPICE, with its matrix-solving algorithms, slows the simulation exponentially as components are added. The SPICE simulation typically analyzes every node at each time-step and, for digital circuits, it cannot take advantage of the inherent latency of digital circuits where, for a given clock cycle, only a relatively small portion of the gates change state.

- *A "general purpose" simulator.* One compromise solution that handles both analog and digital circuit elements is to provide a simulator that is more accurate than a switch-level logic simulator, but not as accurate as SPICE. For instance, if you've designed an op amp at the transistor level, this solution can be helpful within a larger circuit. Using piece-wise linear models, this solution assumes the device is operating in a linear fashion avoiding the need to solve differential equations with a matrix inversion. The digital models are all represented at the gate level, and they are event-driven so they do not have to be analyzed at every time-step.

Tightly coupled simulators. The ideal approach, combining both speed and accuracy, closely couples the matrix solution techniques of an analog simulator with an event-driven digital simulator. To assure proper synchronization and minimize execution time, the simulators pass information back and forth while controlling one another's progress. Both simulators should ease the use of hierarchy all the way from primitive modeling (analog transistors and digital gates) through functional modeling (op amps and shift registers) to behavioral modeling. Such use of hierarchy permits the designer to make architectural trade-offs early in the design process and to use simulation time efficiently.

■ Simulator Interfacing

The challenge in providing tight coupling between the simulators is dealing with the A/D and D/A interfaces, and in synchronizing the simulators. At the analog/digital simulator interface, considerations include: the impedances of the digital parts that drive analog signal levels; the drive strength; threshold levels; exception handling; and accounting for unknown states.

Careful attention must be paid to modeling the impedances at the interface. The model must account for non-linearities and second-order effects. There is considerable variation in the robustness of interface models currently offered.

Output levels of logic devices are not always ones and zeros, sometimes they are in the unknown, or X-state. This is not an error condition, but rather a natural outcome of a set of possible nodal conditions. For instance, a given node may be simultaneously driven by a one and zero so that the actual status of the node is unknown. If the logic simulator does not initialize every node, then many nodes may be set to X at the start of a simulation. Two signals on the input of a device may transition simultaneously, yielding a temporary un-

known state at the output. The unknown state may also result from a condition in which the node oscillates.

Digital simulators are designed to handle the X-state and to minimize the time spent propagating X's. In the analog domain, propagating X's causes a number of problems. First, modeling would be complicated by building X-handling into each model. In theory, X would be propagated throughout the signal paths, and, with feedback to the digital system, X would be propagated everywhere. The final result would be of little use and take a great deal of processing time.

Instead, the X-state should be treated as some specific analog condition, while alerting the designer that an unknown condition exists. There are five ways of driving an unknown node: selecting zero or one at random; forcing the node to oscillate at each time-step; always treating X as zero; always treating it as one; or leaving it at the last known state.

The best solution is the approach that makes the best approximation to the actual state of affairs at the affected node. This "best guess" is to place the node at its last known state, if it was determinate, or to randomly select a value of one or zero if the previous state was unknown.

■ Analog Modeling Language

The word "model" can have many meanings. Sometimes it represents a complex component by means of a set of parameters, like the beta of a bipolar transistor or the open-loop gain of an op amp. At other times it means the equations that use such parameters. In an ideal simulator, the "model" is the complete mathematical description—equations and parameters—of a component.

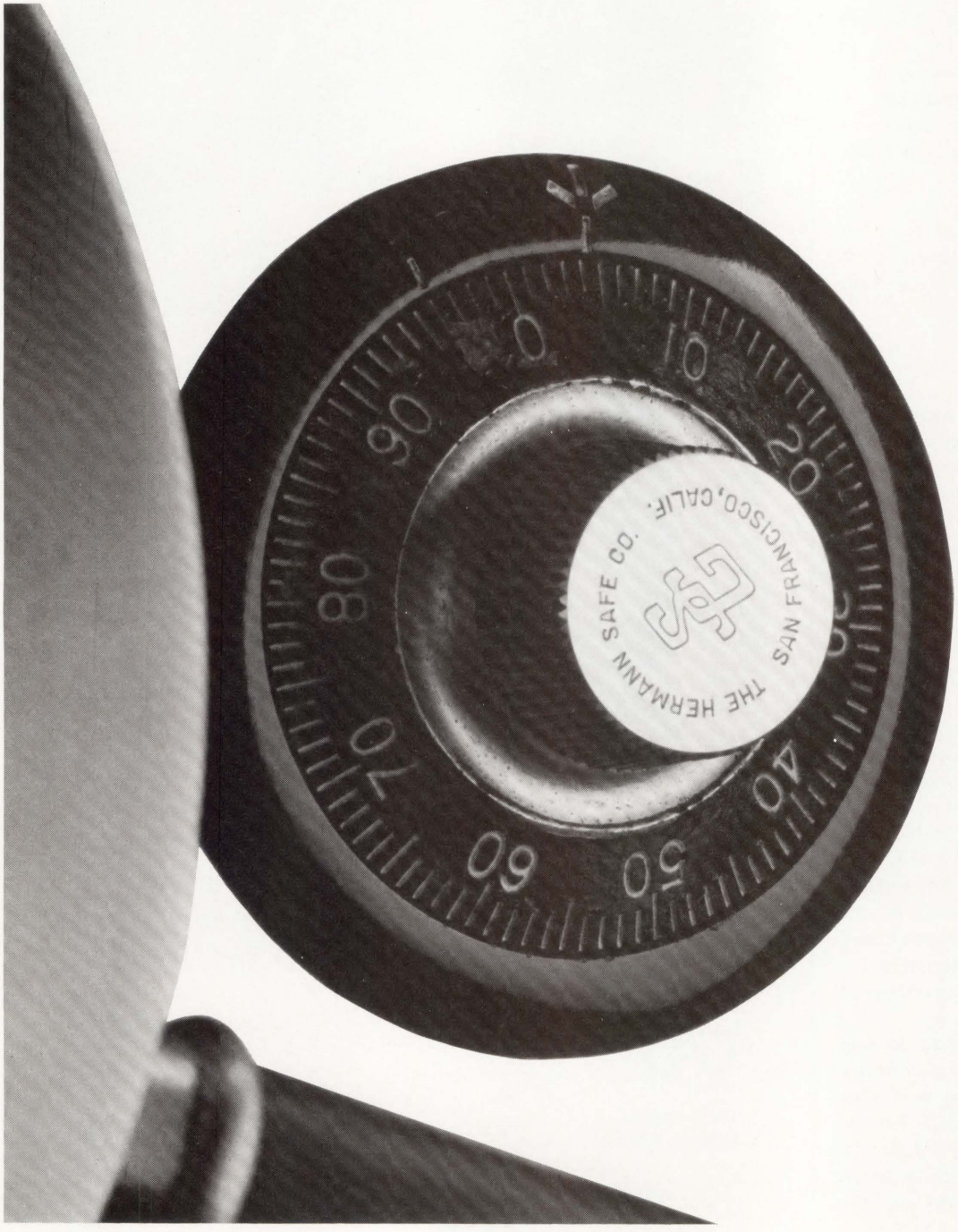
Such an ideal model would consist of two parts: a template that describes a component class in general terms and the set of parameter values that describes the particular component. For example, a model representing a resistor includes a primitive-level template that includes the voltage/current equation and a single parameter: the resistance value. The particular parameter value could then be the single number 1,000.0, which describes a 1-kohm resistance. A more complex primitive, like a transistor, would need a set of parameter values to describe it.

A circuit-level template of an op amp describes the interconnections of primitive transistors, capacitors, sources, and other parts to emulate its performance. At the next stage of complexity there might be a behavioral-level template, such as an op amp with open-loop gain, slew rate, and gain bandwidth, or a set of differential equations that describes the behavior of an electromechanical element, like a motor.

If a simulator accepts only a predefined set of templates, then modeling is reduced to a process of determining the parameter values of the item being modeled. However, if the simulator accepts the addition of user-defined templates, then it becomes possible to build the templates themselves, creating models for a wide range of components and systems. The template should be completely separate from the simulator, allowing the addition of components without having to delve into simulator details.

In the past, analog simulators have mainly addressed the lowest levels of the circuit hierarchy for a restricted set of analog systems. For example, they have supplied predefined primitive-circuit elements, such as transistors and capacitors, as well as blocks of subcircuits. For systems in which the predefined elements did the job, these simulators have given good solutions.

E²/DIGITAL/ANALOG. COMBINATION Y



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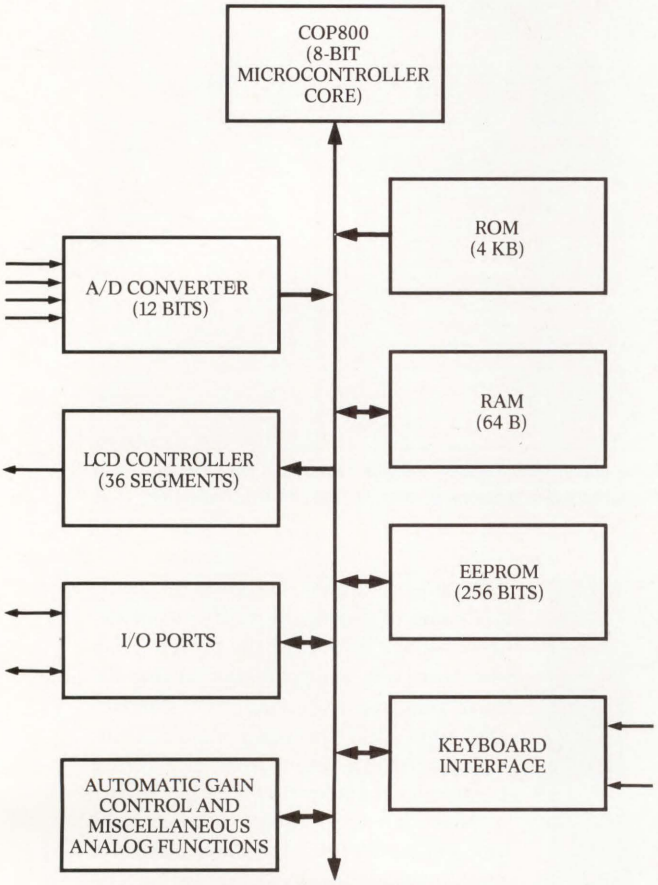

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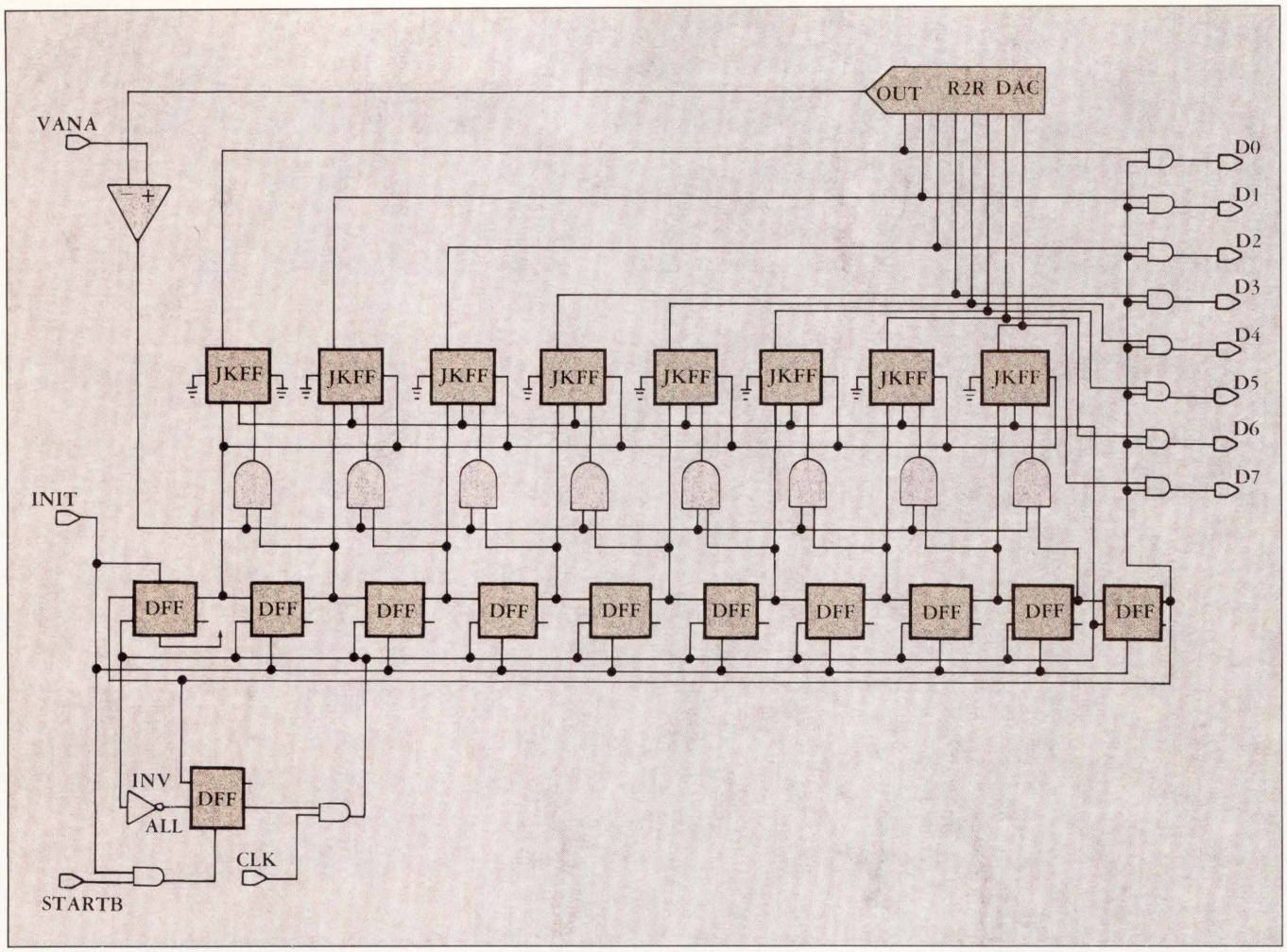


Figure 2. Once architectural trade-offs have been made at the functional level, the eight-bit successive approximation analog-to-digital converter is simulated at a lower hierarchical level. Mixed-mode simulators that don't use matrix solving techniques do not provide sufficient accuracy to determine offset voltages for the comparators, or DC levels, linearity, or settling time for the DAC.

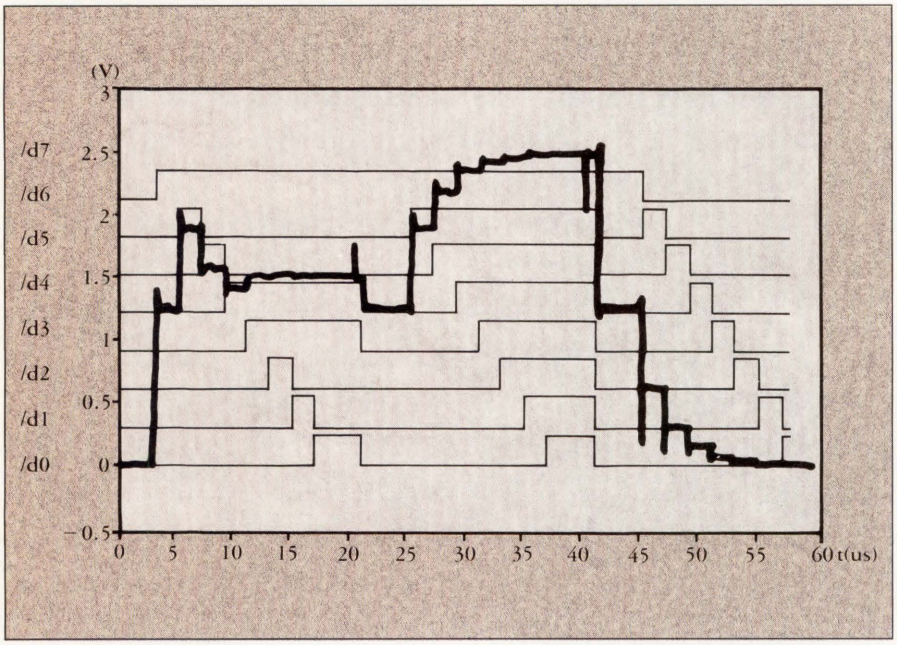


Figure 3. The analog output of the internal DAC is shown superimposed on the eight bits of digital output (for the converter in Figures 1 and 2). Glued-together simulators, at best, deliver glued-together output displays; the digital waveforms and analog waveforms may be seen simultaneously using windowing, but they appear in separate windows. This makes it difficult to properly scale the results, and almost impossible to superimpose the results. A tightly integrated solution allows the analog and digital to be displayed on the same axis with identical time scales.

Designers (digital designers at least) have come to expect the ability to model hierarchically. Consider the design of an 8-bit successive approximation analog-to-digital converter ASIC using CMOS standard cells. Our ideal simulator should allow architectural experimentation by entering at a functional description level (see Figure 1). Note that the feedback loop contains digital elements (glue logic and successive approximation flip-flops), an analog element (high-speed comparator), and an interface element (DAC).

Validating this circuit requires a mixed-mode simulator that handles hierarchies, allows mixed analog/digital-interface elements within a feedback loop, and has sufficient accuracy to demonstrate monotonicity (if true) at an accuracy of 8 bits or better. In addition, if the circuit is implemented in various mixed technologies, such as bipolar, ECL and/or TTL along with the CMOS standard cells, the simulator would allow for tight coupling between all circuit elements. The designer must then be able to descend the hierarchy to simulate at the level indicated in Figure

2 complete with gates, flip-flops, comparators, and a DAC macrocell. Mixed-mode simulators that don't use matrix-solving techniques do not provide sufficient accuracy to determine offset voltages for the comparator's, or DC level's, linearity, or settling time for the DAC. Matrix solutions provide the additional benefit of permitting ac analysis, Fourier, Monte Carlo, and noise analysis separately on the analog circuitry.

But, by their very nature, the analysis routines found in conventional analog simulators usually require all components to have continuous first derivatives. Moreover, unless predefined components are acceptable as an electrical analog (or the user is willing to alter the simulator), they cannot handle multi-discipline systems comprising electrical, electromechanical, and electro-optical subsystems.

In contrast, by not requiring components to have continuous first derivatives (although the function itself must be continuous) and by internally supporting a hierarchy, our ideal simulator can handle a wide variety of behavioral, functional, and primitive components and levels for any analog system. Additionally, the separation of the modeling aspects of the program from the analysis would allow new models to be added without recompiling or relinking.

■ THE USER INTERFACE

"Glued-together" simulators, at best, deliver glued-together output displays; that is, the digital waveforms and analog waveforms may be seen simultaneously using windowing, but they appear in separate windows. This makes it difficult to properly scale the results and almost impossible to superimpose the results. A tightly integrated solution lets you display analog and digital waveforms on the same axis with identical time scales. For instance, the display in Figure 3 shows the analog output of the internal DAC superimposed on the 8 bits of digital output for the 8-bit analog-to-digital converter illustrated in Figures 1 and 2. Note that three different input voltages were applied (1.5 V at t=O, 2.5 V at t=20 us, and OV at t=40us) and that with each time-step the output of the internal DAC closes in on the input voltage.

Users of digital simulators have come to expect some degree of interactivity. Similarly, with a mixed-mode simulator they want to be able to stop the simulation during the run, examine simulation results in either or both domains, and then resume the simulation from that point in time. While digital simulators typically save internal states (at least for predefined nodes), analog simulators do not; they tend to run as batch processes. Saving analog nodal information is an I/O-intensive process and lengthens simulation time, but it is required for simulation to resume from its temporary stop point.

No system can be considered truly interactive unless the simulation is executed in the shortest possible time. To assure reasonable run times a hierarchical approach is mandatory for both analog and digital circuit elements. This has generally been the case for digital simulators, but not for analog simulators. Since SPICE must always run at the level of transistor primitives, using SPICE in a mixed-mode simulator would be a serious drawback. High-level analog behavioral modeling is a must for efficiently executing board-level designs.

■ TOWARD THE IDEAL SIMULATOR

To gain widespread acceptance, today's ideal simulator will need to combine an industry-standard digital logic simulator

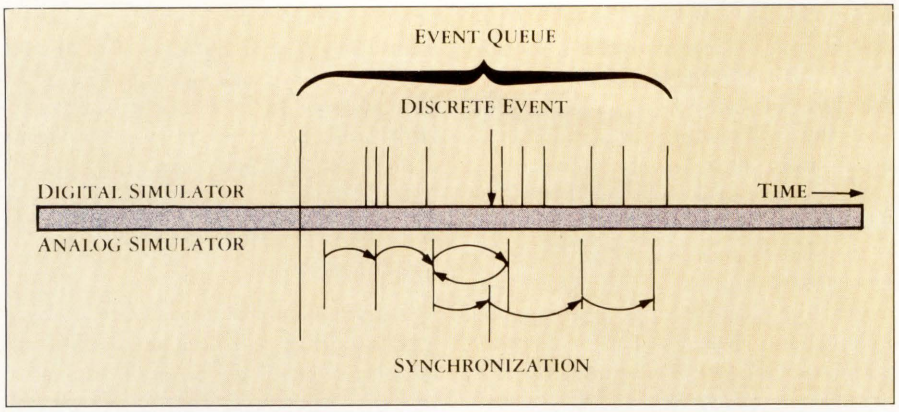


Figure 4. Synchronization between analog and digital simulators can be accomplished using a "leapfrogging" technique. Instead of providing a traditional lock-step algorithm, where the simulators have to reach a certain point in time before continuing, the analog simulator is permitted to run as far ahead in time as is required. When a digital event occurs that requires analog processing, the simulator reevaluates its solution and either continues forward in time or adjusts backwards in order to maintain accuracy.

with an analog simulator that provides true matrix solutions. The analog side will need to use SPICE-equivalent models to take advantage of the existing model databases developed at great effort and expense, and will require extension to behavioral modeling to achieve reasonable execution time. Furthermore, it will have to provide a clever scheme to synchronize the time-steps of the analog simulator with the event queue that drives the digital simulator. Only with such synchronization can the mixed-mode simulator handle feedback between analog and digital.

One such scheme splits the simulator into three parts: the analog simulator, the digital simulator, and the simulation control process. Using multitasking operating systems, the digital and analog simulators run as separate subprocesses under the simulation control process. The control process is responsible for initialization and synchronization of the analog and digital simulation subprocesses. Synchronization of the simulators is then performed by an algorithm that has access to information about the analog simulator's internal time-step and the digital simulator's event wheel. Logic events are scheduled in regular fashion, and the analog simulator's time-steps are adjusted only when a signal that affects both digital and analog circuitry changes. If the amount of activity across the boundaries between analog and digital circuits is small in comparison to the activity in the rest of the circuit, reasonable performance is possible.

A better technique breaks up the lock-step synchronization between the simulators by allowing "leapfrogging" (Figure 4). Instead of providing a traditional lock-step algorithm, where the simulators have to reach certain points in time before they continue, the analog simulator is permitted to run as far ahead in time as it needs to. When a digital event occurs that requires analog processing, the simulator reevaluates its solution and either continues forward in time or adjusts backwards in order to maintain accuracy. With this leapfrogging approach, both simulators analyze the system efficiently, sharing intermediate results of the solution. This allows feedback to propagate through the analog and digital simulators as required, and greatly decreases simulation run time.

In addition to synchronization of the two simulators, special attention must be given to cells that bridge the analog/digital domain. In one scheme, special analog devices model the interface between the logic simulator and the circuit simulator: a digital-to-analog (D/A) interface and an analog-to-digital (A/D) interface. Analog model statements control the characteristics of the interface devices. By varying these models, the user can create interfaces for different logic families.

Another approach to the A/D interface uses "hypermodels." These models can be looked upon as behavioral models that have interprocess communications capabilities built into them. In this scheme, where an A/D interface occurs in a circuit, nodes are split into two interface models; one digital and one analog.

All of the component tools and processes needed to synthesize the ideal mixed-mode simulator are present. The separate simulators are available and the problems of integrating them are understood. The marketplace is now seeing at least a few simulators that come very close to reaching this ideal.

■ Beyond the Ideal Simulator: The Dream Simulator

It is interesting to speculate on the capabilities that the next generation of mixed-mode simulators may provide, and to think about a wish-list for a "dream simulator." At present, even the close-to-ideal simulators suffer from the need for interprocess communications. Only a unified simulator with new algorithms that operate on all circuit elements will suffice. Such a simulator would likely come from a single company, not from a melding of two simulators, since neither company is likely to divulge the full source-code to the other.

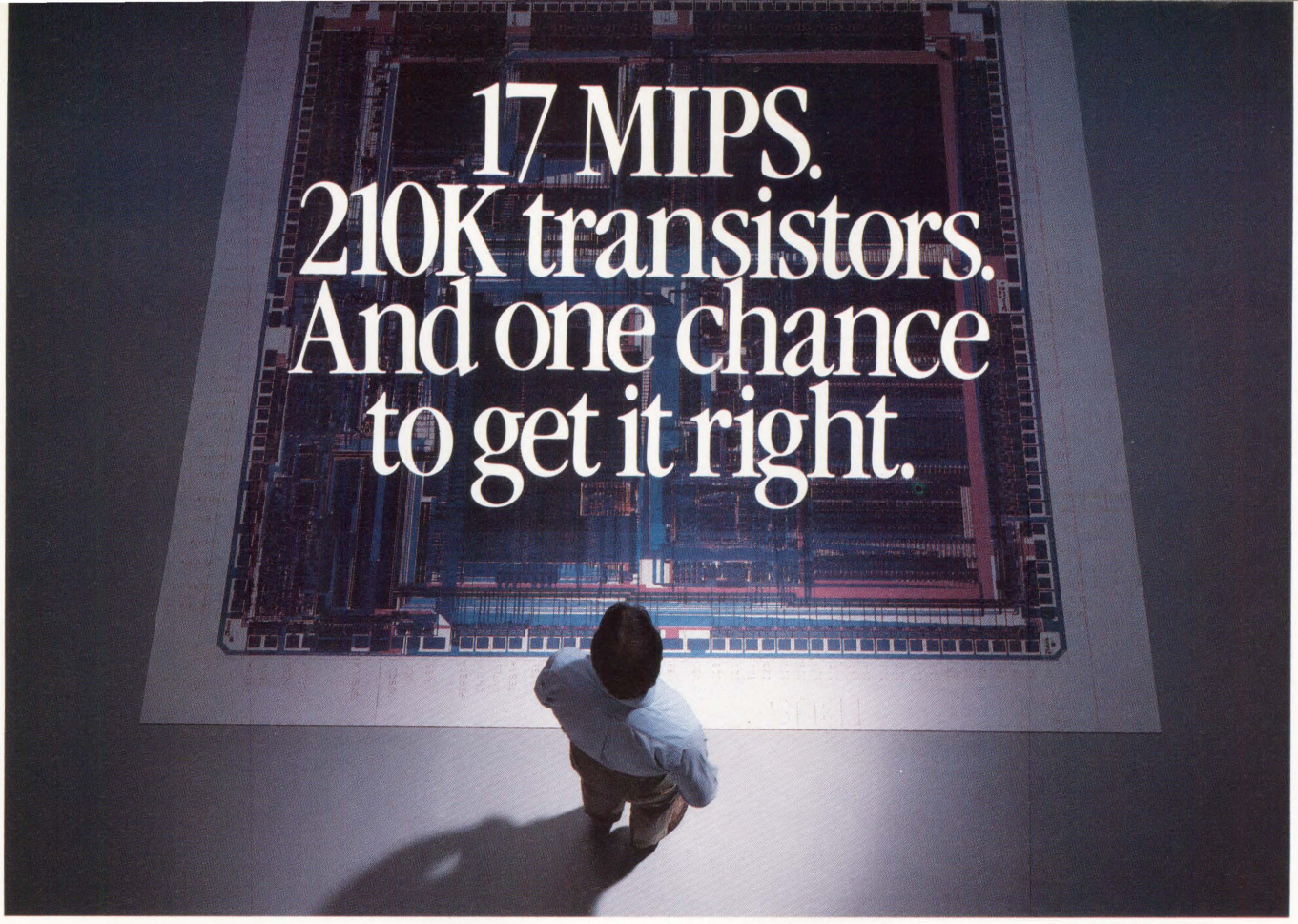
Next-generation simulators might have the capability to automatically extract simulation models by making measurements on existing parts similar to the way that parameter extraction programs work to extract SPICE data from transistors under test.

The "dream" simulator would extend hardware modeling, now available in the digital domain, to the analog domain, so that analog components such as A/D converters, op amps, comparators, and phase-locked loops could be plugged into the modeler and made a part of the simulation. To provide accurate timing information, at actual operating frequencies, careful attention would have to be paid to packaging and controlled-impedance interconnects.

This new simulator would extend software and hardware acceleration to the analog portions of the simulation. At present a number of dedicated logic simulation accelerators achieve 1,000X+ performance improvement by embedding the simulation algorithms in custom silicon or by microcoding. SPICE acceleration, on the other hand, has concentrated on parallel processing, taking advantage of the coarse grain parallelism inherent in operating on a number of SPICE circuits simultaneously. SPICE execution time increases exponentially with circuit size. Relaxation-based techniques require only a linear time increase with circuit size, but do not provide accurate results for tightly coupled circuits. The recent emergence of algorithms with the accuracy of SPICE but with better inherent performance has successfully addressed this problem. ■

About the Author

GEOFFREY SAMPSON *is a principal engineer in the Microelectronics Division of NCR Corp. He joined the company in 1986. Prior to that, he worked as an analog designer in the Communications Division of Tektronix Inc. Presently he is actively involved in analog circuit simulation, modeling, and mixed analog/digital simulation. He received a BSEE degree from the University of Colorado, Boulder, in 1984.*



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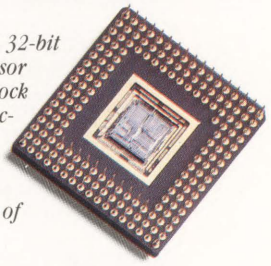

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Automatic FLOORPLANNING

RONALD AYERS, MOSIS PROJECT,
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The innovative part of VLSI chip design is often a set of custom layout blocks, blocks which by themselves have been cleverly planned and tuned. The remainder of the VLSI design is less innovative. This part of the design is completed as these blocks are placed in relation to one another, and then finally wired and given exact geometric placement.

This article will address the first of these two steps, automatic floor-planning. (The second step, fusion, implements the wiring and precisely positions the blocks.)

INNOVATIVE BLOCKS REQUIRE INNOVATIVE PLACEMENT ALGORITHMS

There are two levels of floor-planning. On a small scale, within an individual layout block, the process is a manual task. This kind of floor plan is part of the innovation of that block—the custom tiny cells, such as one bit of RAM, having been designed so as to fit most snugly within the floor plan.

Large-scale floor-planning (Figure 1) deals with layout blocks, that were not designed to fit snugly with one another. These large blocks of layout generally have unrelated sizes and pinouts.

Large-scale automatic floor-planning becomes indispensable as the number of blocks increases. For example, random logic might be implemented by several blocks, which usually perform better for the entire random logic and consume less area than a single array.

Automatic floor-planning becomes even more indispensable when accessing blocks from a library, which may offer multiple layouts for functions that differ, perhaps, in aspect ratio. If there are multiple layouts for several blocks, the total possible arrangements quickly increases.

Automatic floor-planning is most needed when the cells are computer generated. Often the size and number of cells are not known in advance. In addition, manual floor-planning could destroy an otherwise completely automatic generation of VLSI designs.

Figure 2A shows the minimum-bounding-boxes (MBBs) for a set of possible layouts of a given function. They are all centered at the origin. Since they all have nearly the same minimal area, the upper-right corners of the MBBs lie approximately on a "1/X" curve.

The following scenario should remind designers that they can't rely on a packing algorithm that opts for a minimal area solution at each and every step. Figure 2B shows that combining the minimal area solution with another block (on the right) may result in an overall area that is far from minimal. Figure 2C shows that another solution for the left block (although not of minimal area) yields minimal area overall.

Another consideration is that blocks that communicate heavily with one another (via many wires) should be close together in the final floor plan. This communications optimization can conflict with optimal packing. A good packing solution that includes large distances between heavily communicating blocks may backfire when all of the wires are implemented. The wires take up space, and may render the once good packing as sub-optimal.

The automatic floor-planner described here has two major phases. The first pulls together blocks that communicate most heavily with one another. The second does the packing, although greatly influenced by the closeness that was developed in the first phase.

For the remainder of the article the term "cell" will be used inter-

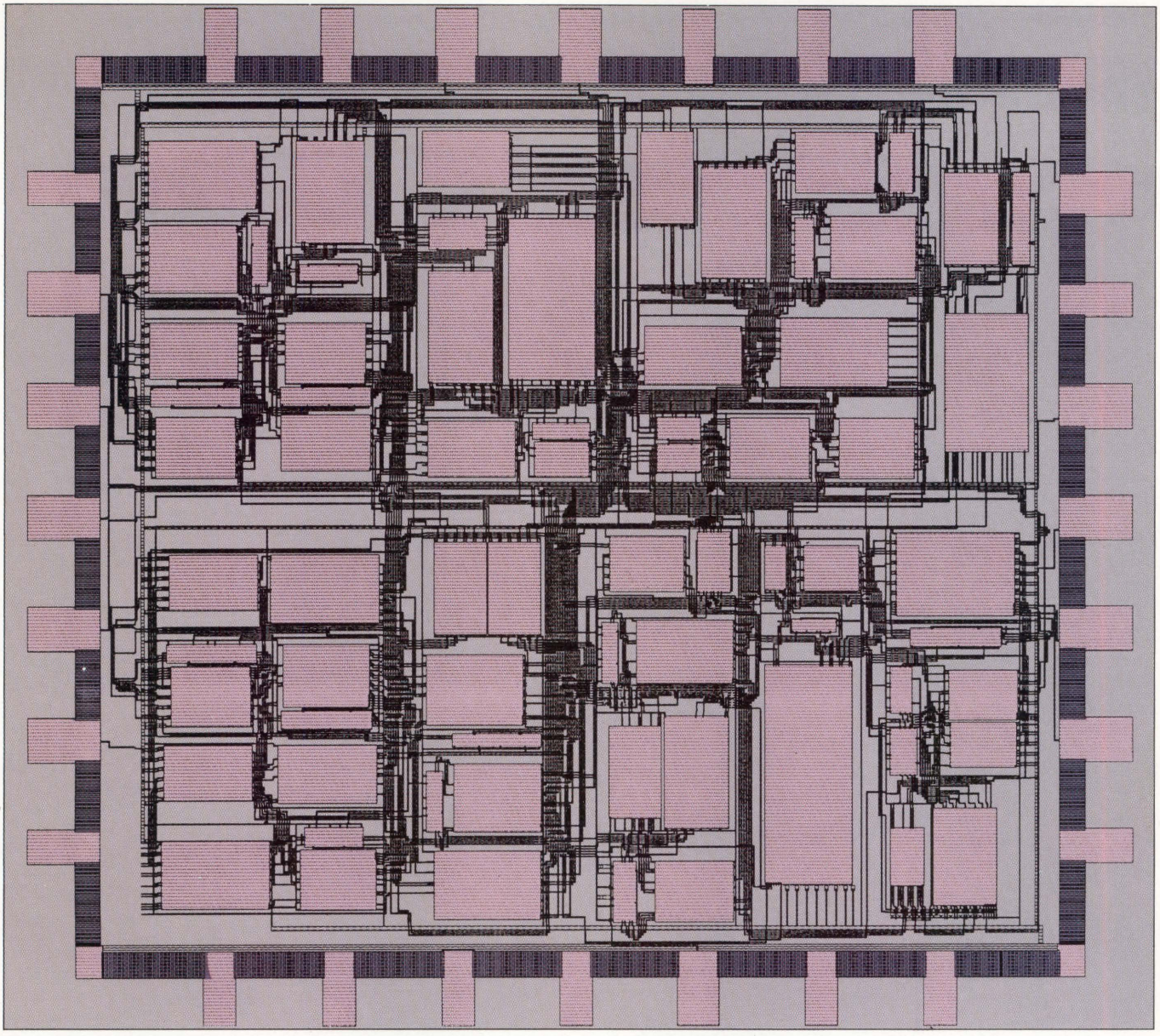


Figure 1. The above layout of an eight-channel, 64-level light controller chip is a result of the automatic floorplanner described in this article.

changeably with "block."

■ Representation of Floor Plan

A floor plan for a set of cells can be represented by a hierarchy, or tree, whose leaves are the individual cells (Ayres, 1983). The branches are nested lists. At the lowest levels in the hierarchy are lists whose elements are cells.

Figure 3 shows three distinct hierarchies, and the floor plan that each implies. A hierarchy is mapped into a floor plan using the following rule: Lists at the lowest levels in the hierarchy place their constituent cells left to right (Figure 3A). Lists just above those place their implied layouts from bottom to top (Figure 3B). The next higher lists place their implied layouts from left to right.

In general, each level in the hierarchy, places its cells alternately from left to right or bottom to top. This alternation gives rise to two-dimensional layouts.

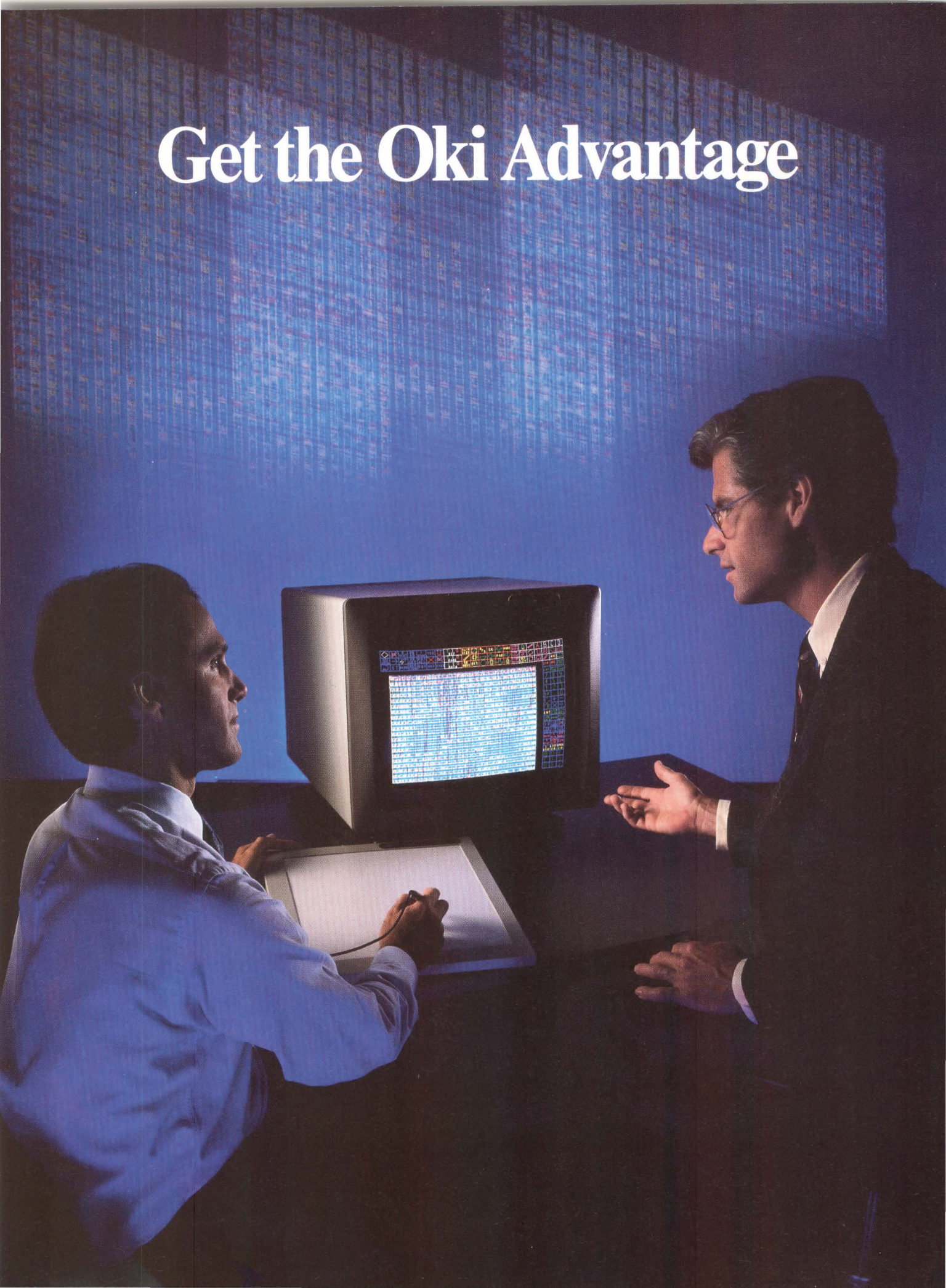
In fact, each list always places its elements left to right. But there is a final rotation applied to the left-to-right row, turning it into a bottom-to-top column. Nested applications of this "left to right then rotate" is what generates the the alternating left-to-right/bottom-to-top placement.

Enclosing a cell with an extra pair of brackets effectively rotates that cell. Enclosing a list with an extra pair of brackets rotates its placement, converting an originally left-to-right placement to a bottom-to-top placement, and vice versa. Thus, it is easy for a computer program to manifest a hierarchy in order to come up with another one that implies whatever floor plan the computer program dictates.

The hierarchy not only represents a two-dimensional floor plan, but also represents "closeness" among the cells. Cells belonging to the same list are located closest together. Thus the hierarchy represents both the closeness of the communicating cells and the packing of all cells.

Our automatic floor-planner produces two different hierarchies. The first, "grouping by communications," might represent poor

EFFICIENT FLOORPLANNING MUST INCLUDE CLOSENESS OF COMMUNICATING BLOCKS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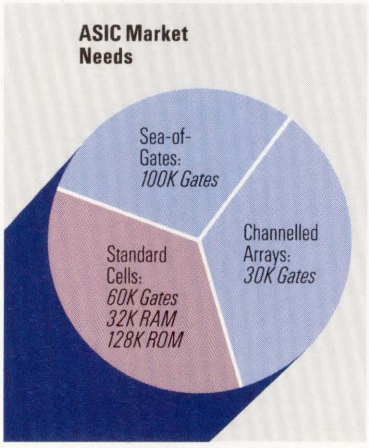

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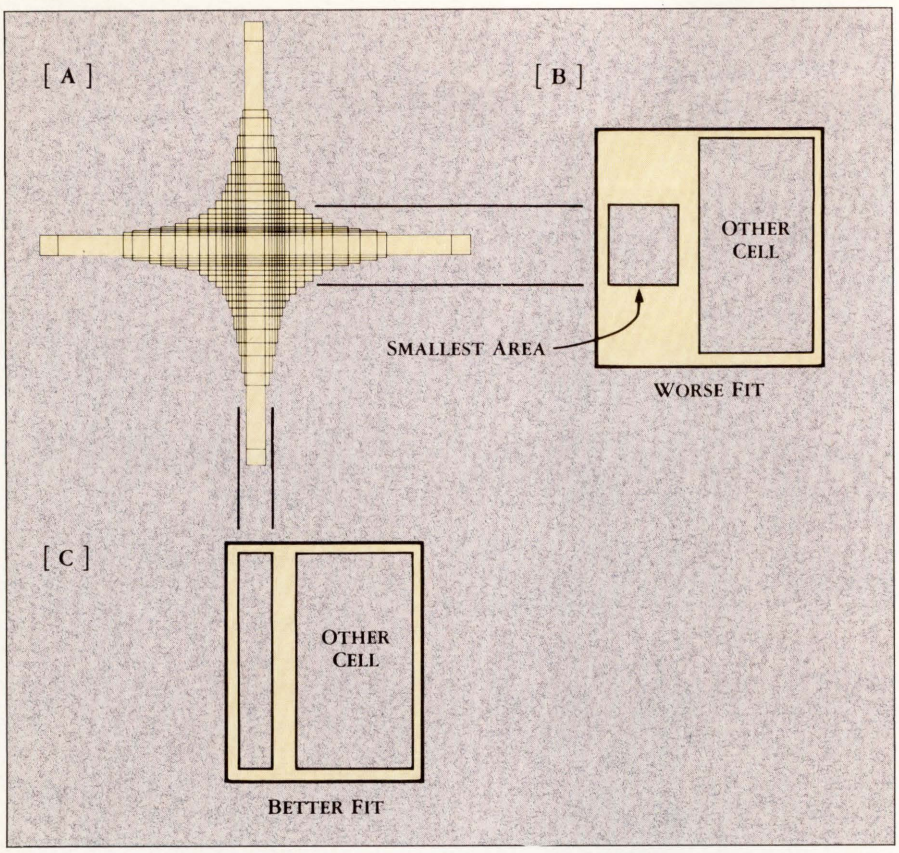

Figure 2. An algorithm that opts for a minimal area solution at each step may not provide the best solution.

packing. The second modifies this hierarchy slightly to produce good packing. By modifying the hierarchy, instead of creating one from scratch, some degree of closeness of cells is preserved in the final, well-packed hierarchy.

■ Grouping By Communications

In gathering the highly communicating cells together, we might be given a single list of cells to start out with. In this case, the entire hierarchy would have to be synthesized. Alternatively, we might start out with a hierarchy, in which case the task is to refine that hierarchy.

Each list in the hierarchy has an associated "interface." The interface represents the pinout of the layout that will be derived from that list. This pinout consists only of signals, not layers or positions. Since each point in the hierarchy has such an interface, we can measure the "closeness" of two sub-hierarchies by counting the number of signals they have in common in their interfaces. The more signals they have in common, the greater the need for increased closeness.

The operation of grouping by communications takes place one list at a time. The operation must be applied recursively to each element in the list. Then the number of signals that each pair of elements has in common must be evaluated.

This pair-by-pair communication bandwidth determines whether any two particular elements are communicating more with each other than any other elements. Then the identified pairs are combined: If one element is a list, the other is placed into it. If neither is a list, both cells are enclosed within a new pair of brackets.

After dispersing cells with such obvious communication preferences, the element pairs must be considered again to determine the greatest common interface within any pair. Then chains of elements are constructed in which each chain represents a set of elements, all of which communicate with one another at that maximum bandwidth. There may be several such chains. Figure 4 shows two groups with the maximum of three wires. We know that the cells within these groups communicates more with each other than with any cell outside the group.

If all the cells communicate with one another at the same maximum bandwidth, there is only one chain, and hence nothing has been gained by this attempted grouping. In this case, we leave this point in the hierarchy unchanged.

If the grouping is non-trivial, brackets are placed around each group, thereby refining the hierarchy. Then the grouping is performed recursively on each of these newly formed groups by the communications operator. (We flag the recursion so as to avoid duplicating the process on any of the original elements). The grouping algorithm has an n-squared behavior given a list length of n. If n is above 50, the given list is arbitrarily cut into shorter lists of less than 50. Within each list a non-recursive group-by-communications is performed to acquire bundles of the most actively communicating cells. Each list of 50 is thus shortened, and bundles are now referenced instead of individual cells. The shortened lists are recombined into a smaller set of lists of length 50. This operation is repeated until there is only one list of length 50 or less. At this point, the grouping algorithm takes over.

■ Weighting Signals Within a List in the Hierarchy

Not all wires are given the same weight in the preceding discussion. Wires that are shared more heavily are given lesser weights. That is, a wire that connects only two elements is given a weight of one. A wire that connects three elements is given a weight of one half. In general, we assign the weight $1/(N-1)$ to each signal that connects N elements together. N is derived by counting the number of elements within whose interfaces the signal resides, including the interface for the list at this level in the hierarchy.

Figure 5 illustrates the rationale for reducing the weights of highly shared signals. Part A shows what four distinct signals cost in terms of routing requirements. The channel above that row is four deep. In contrast, one signal shared among the four cells (part B) incurs a cost only one-quarter as high. Part C shows what our pair-by-pair formalism requires us to see. (Each pair is connected by what looks like a distinct wire). To continue to use the pair-by-pair model, we must apply a weight of only one-quarter to each "distinct" wire in order to accurately represent the real situation as illustrated in part B.

Figure 6 shows the effect of such weighting with regard to a multiplexer (MUX). Part A shows that K wires are shared among 2^K cells. Part B shows that the total weight between any pair of MUX elements is less than one. The "unshared" wires, between each MUX element and the block that it drives, all have a weight of one. This forces the grouping shown in part C, as opposed to the grouping in part D. Part D shows 2^K distinct signals as yet to be wired, whereas part C shows only K distinct signals yet to be wired.

■ Preparation For Packing

The packer will turn each list in the hierarchy into overall rectangular packing. After grouping by communications,

some lists in the hierarchy may come up short. Packing many elements together is often more efficient than packing fewer, larger elements. Therefore, the hierarchy is then modified by removing some pairs of brackets, which makes longer lists. The goal is list lengths of up to 7 or 8.

■ Ordering Within Each List

The order of elements within a list can be optimized. For example, if cell A talks to B, and B talks to C, then the order ABC is more optimal than, say, CAB. In this case, the new order will assure that cells that communicate most heavily with one another will appear closest together. So at this point, highly communicating cells have not only been brought into the same list within the hierarchy, but that list has been organized to further reduce wiring.

This organization is produced by first picking the element which has the largest interface. The new element is iteratively inserted into the placement built up so far. We chose the element that communicates most heavily with elements already in the order. Each possible insertion is considered, measuring both the cost of the element's communications with others from that position, and the cost of forcing apart the elements which lie to the left and right of the position. The lowest cost insertion is selected.

■ Packing

The basic packer turns a list of elements into a rectangular packing. This is achieved by adding more bracket pairs. The full recursive packer proceeds from the bottom up, tackling packing lists lowest in the hierarchy first.

The packer does not result in a single rectangular solution, but rather in a set of possible solutions, like those shown in figure 2A. This set is called an "ambiguous" solution, a term borrowed from language processing, where the (temporary) tolerance of ambiguity makes rich languages translatable.

■ Basic Packing

The task of basic packing is reduced to one of language processing. Any packing can be specified textually with the use of three operators: two binary operators that specify "abut horizontally (H)" and "abut vertically (V)," and one unary operator, "rotate."

For example, the floor plan in figure 3B can be represented as:

(1 H 2 H 3) V (4 H 5) V (6 H 7)

We consider all possible such phrases. In this example, H or V can be chosen for each of the six in-between positions. Rotation can also be spontaneously applied to any cell, or around any pair of corresponding parentheses.

Notice that for a list of length N, there are at least 2^N possible such phrases. Even in the presence of only one binary operator, there are many ways to place the parentheses. This placement is very important, as shown in Figure 7. The ability to spontaneously rotate an element, or a combined phrase of elements, is another way to exponentially place many phrases.

The language processing technique that

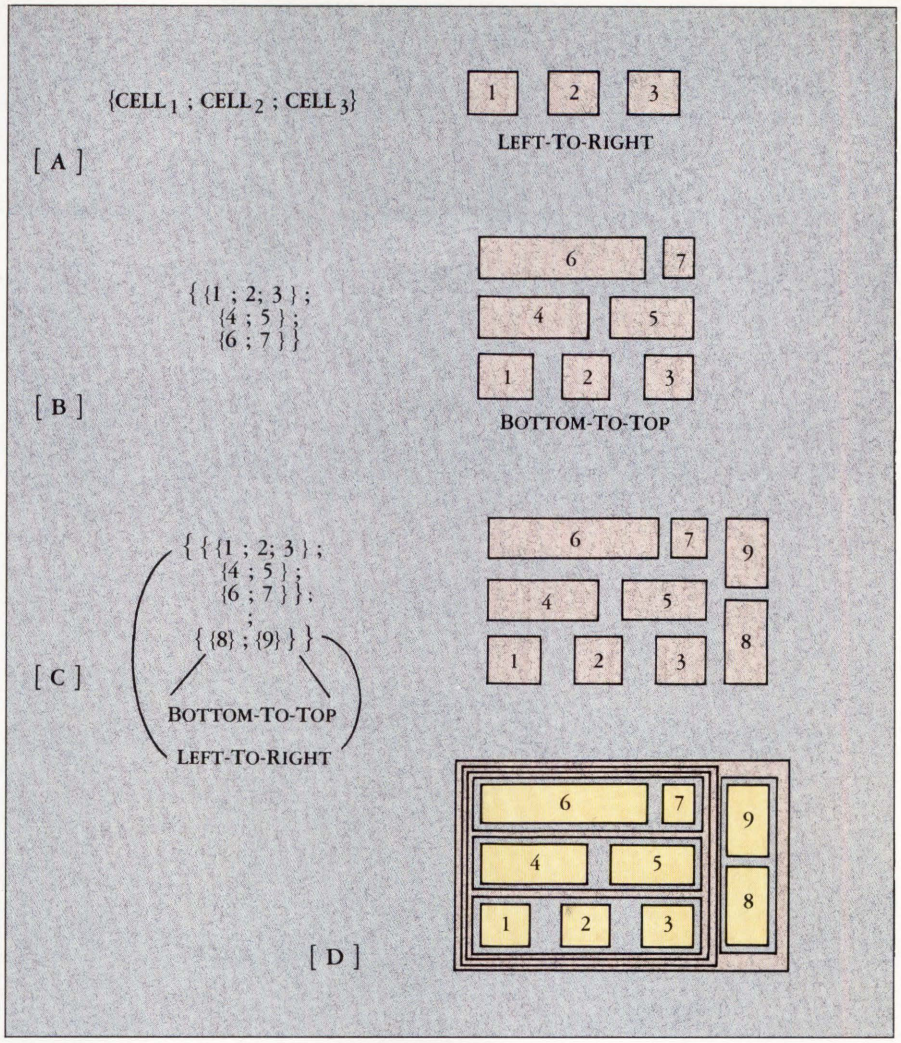

Figure 3. Three distinct hierarchies are shown above together with the floor plan that each implies.

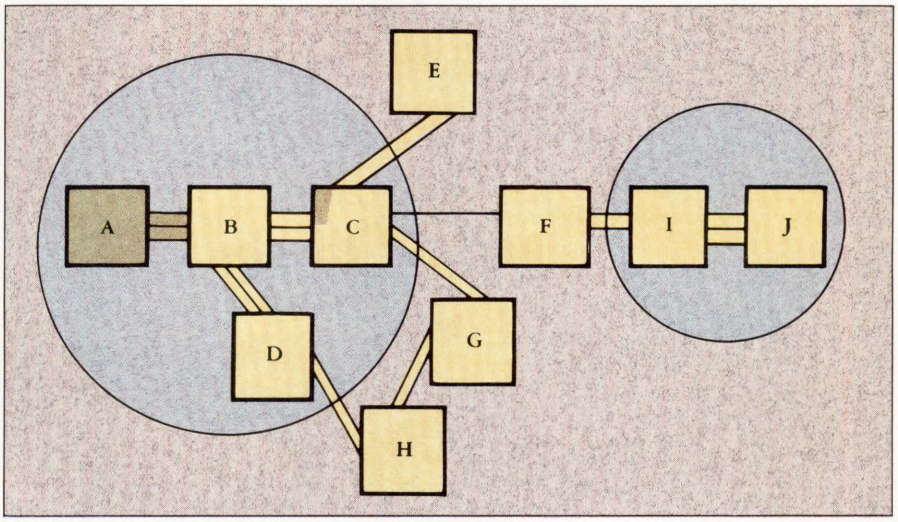

Figure 4. After dispersing cells with obvious communication preferences, the element pairs must be considered once again to determine the greatest common interface within any pair.

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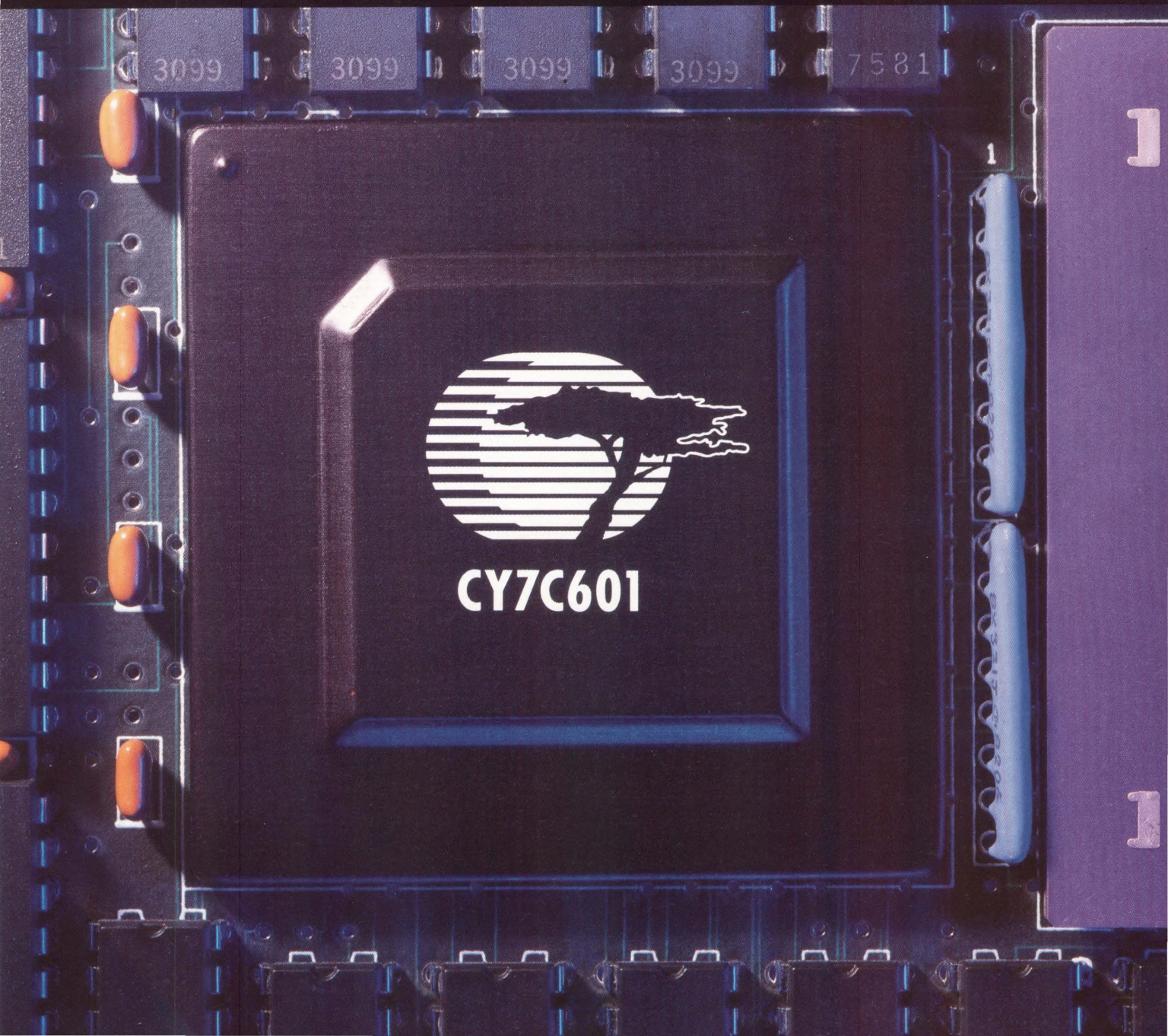

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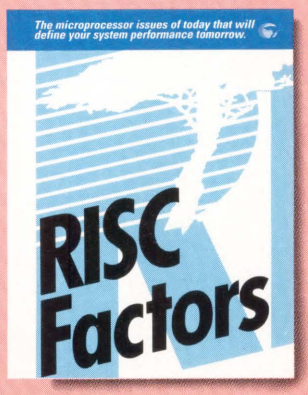

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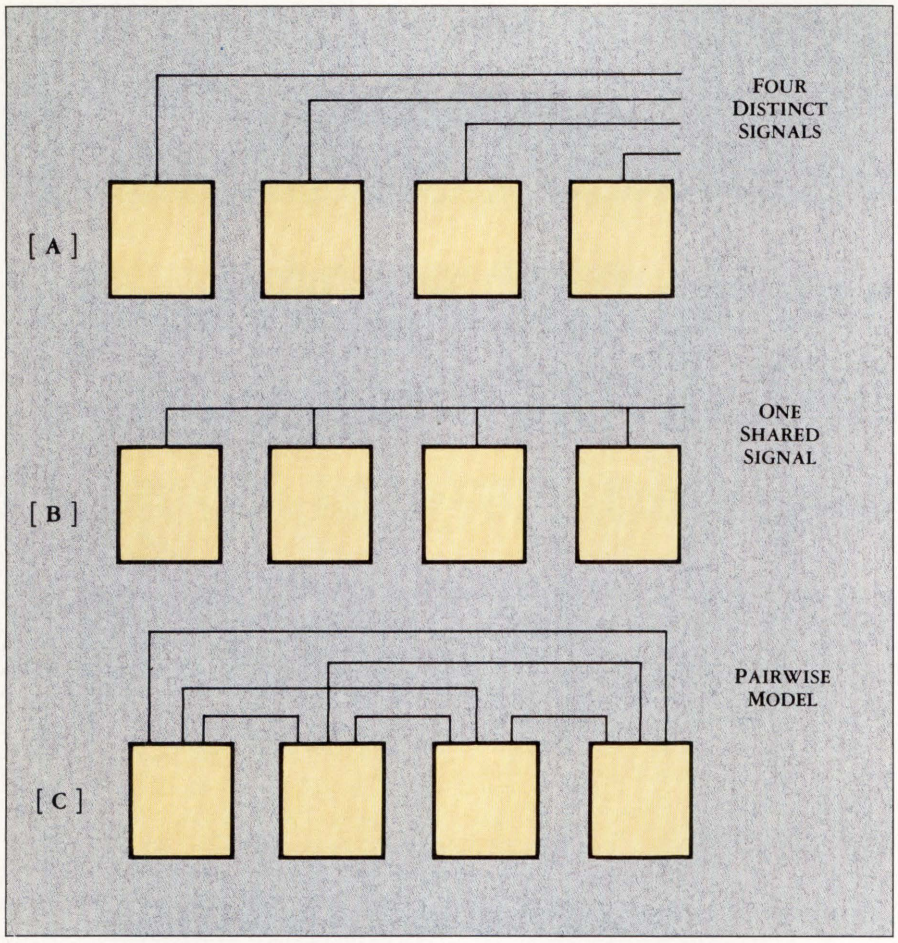

Figure 5. The rationale for reducing the weights of highly shared signals is illustrated above.

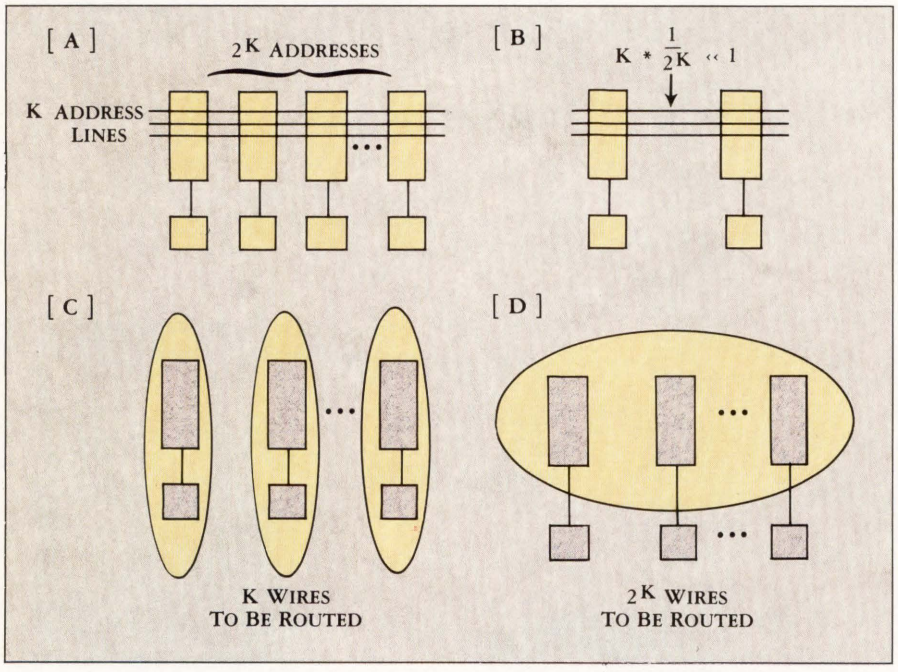

Figure 6. The effect of reducing the weights of shared signals with regard to a multiplexer (MUX) is shown above.

handles such enormous possibilities is called parsing. All possible interpretations of the phrase "1 H-or-V 2 H-or-V 3 H-or-V 4 H-or-V 5 H-or-V 6 H-or-V 7" will be considered by parsing this phrase with the following grammar:

solution -> solution (by rotation).

solution H solution -> solution (by horizontal abutment)

solution V solution -> solution (by vertical abutment)

This grammar is very ambiguous, meaning that the grammar will understand the overall phrase as a solution in many different ways. The grammar doesn't insist on a left-to-right grouping, and thus considers all possible placements of parentheses.

Parsing can consider all possible solutions in only polynomial time. The trick is to suppress "identical" solutions during the unrestricted application of these grammar rules at all possible sub-phrases.

For example, Figure 8A shows all possible phrase spans for the phrase "1 H 2 H 3 V 4."

Each such span, or parse, contains all possible solutions that involve the cells and operators over which it spans. Figure 8B shows such occupancy. Each time a new solution for a parse is proposed, we compare it against the existing solution in that parse, and select the best solution. A solution is better if it fits inside of the other solution. The occupancy in each parse is limited to approximately 20 distinct, best solutions. By definition, two solutions that have dimensions that are within five percent of one another are declared to be identical, and only the minimum area one is preserved. Solutions whose sizes are non-comparable (where neither one lies entirely within the other) are preserved. The surviving solutions all have nearly minimal area, and differ primarily in aspect ratio.

■ Recursive Packing and the Preservation of Ambiguity

Given a list in the hierarchy, the overall packer first provides an ambiguous solution for each element in the list, using recursion. The ambiguous solutions for the elements are then combined by the basic packer into a single ambiguous solution for the overall list.

Cells represented by the numbers in the previous discussion may actually be ambiguous solutions. For example, even the short phrase "1" (Figure 8B) can have an occupancy of more than one solution. (The "1" thus represents the ambiguous solution obtained from the sub-hierarchy represented by the first element in our list.) The tolerance of ambiguity within individual elements costs nothing more because the parsing algorithm already tolerates ambiguity in all non-trivial phrases, such as (1 H-or-V 2). Thus the currency of this packer, at all levels in the hierarchy, is an ambiguous solution.

The "leaves" at the bottom of the hierarchy can be presented as ambiguous solutions. This enables a desired function to present not one unique solution, but a whole suite of solutions. The "disambi-

guation" that occurs naturally throughout the packer serves also to decide among multiple solutions at the leaves. The leaf solutions are naturally chosen so as to minimize the overall area.

At the top of the hierarchy, we are also presented with an ambiguous solution. The choice of the overall solution should account for aspect ratios that may be required for subsequent manufacturing and testing.

■ Preservation of Order

All the solutions considered by the packer preserve the order initially imposed upon the lists, preserving the communications considerations. If the packer produces a list as a single row, the original order is clearly preserved. Other solutions are equivalent to the linear solution, with folds inserted. Those folds serve only to bring cells even closer together.

■ Estimate of Wiring

Within a given list in the hierarchy, the packer, with its grammar, produces all possible solutions, but ignores the space taken by the wiring. Within the parsing, which consumes N^3 of CPU time, wiring is ignored simply for speed.

Therefore, we repack each solution in an ambiguous solution. The topology of each solution is preserved, but extra space is imposed between cells in an attempt to predict wiring space. Wiring thicknesses are derived from the number of interface signals appearing within the hierarchy. These estimates have been tuned so as to provide the most realistic estimates, by looking at the results of the subsequent fusion (see, for example, Figure 1).

■ Large N

If a given list in the hierarchy has more than 10 elements, the same packing algorithm applies, but certain between-parse nodes are deleted. That is, after parsing the first 10 elements, the left-most node, between the first and second elements, is deleted. Also deleted are all parses either starting or ending there. One more element can thus be appended on the right, preserving the maximum of 10 between-parse nodes. In the worst case, this rule may remove from consideration a particular fold, although nearby folds will be preserved. However, the lost fold may still exist within solutions of the remaining parses that span the defunct node.

■ Two-Dimensional Ordering

Once the packing is done, the hierarchy is modified. We can reorder any list in the hierarchy without changing the packing. Thus, we reorder lists to bring heavily communicating elements closer together, but this time, we do it knowing what surrounds that list, in two dimensions. The ordering within two dimensions occurs from the top down. For each recursive call, context—which represents the outside world—is passed downwards. This context is a set of signals, where each signal has an interval of residence along each of the four sides. Each list is ordered within this context.

Two top-down sweeps are made. The first sweep propagates order constraints from left to right (or bottom to top for vertical lists). Each list is ordered seeing only the context to the left and below. Context on the other two edges hasn't yet been faithfully propagated.

The second sweep propagates order constraints from right to left (or top to bottom), and all four edges of context are seen. Each list is ordered now in the full context.

We order each list with a slight modification to the ordering algorithm used prior to packing. At each possible insertion location, the cost is augmented to include the communications cost between the inserted cell and the external context.

Mirroring of leaf cells and rotation of "nearly square" cells operations are also used to obtain better solutions.

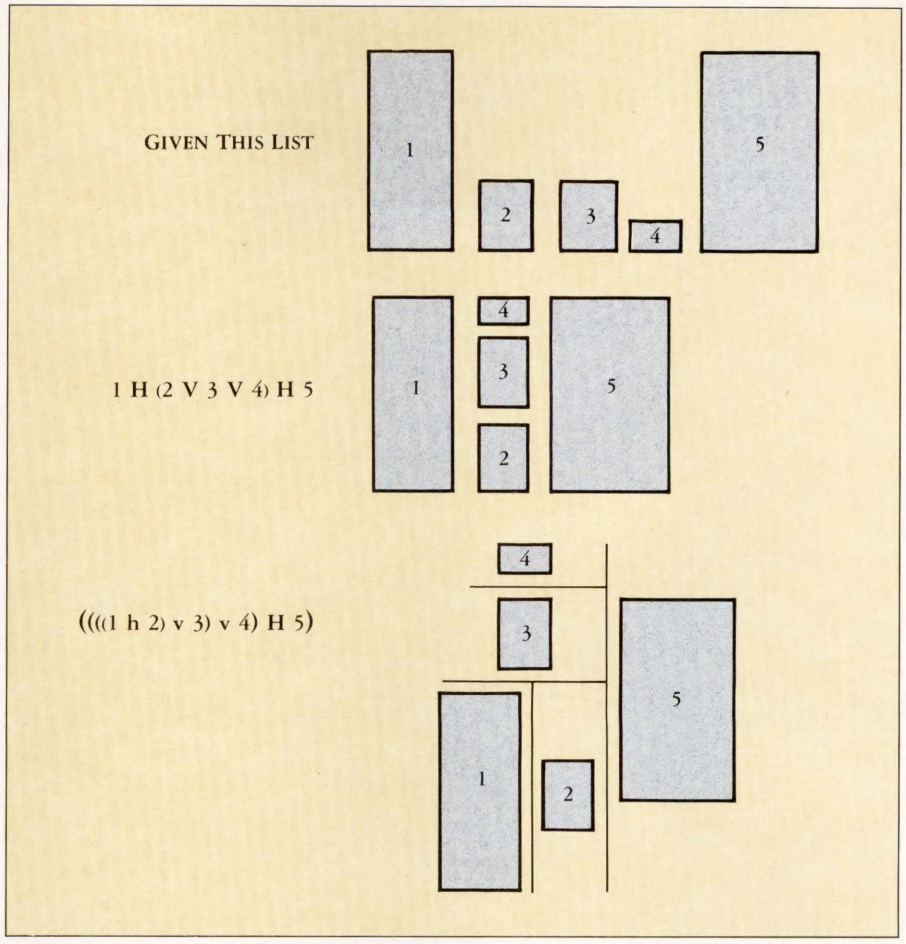

Figure 7. The importance of the placement of the parentheses is shown above.

■ The Participation of Block Generators in Automatic Floor-Planning

We allow a block generator to produce a "place-holder" cell together with an ambiguous solution. This solution is the generator's way of providing different possible solutions, one of which will be chosen during packing. The place-holder cell exists merely to get through the grouping-by-communications phase.

We then assume that the cell chosen by the packer is the cell meant to be produced by the block generator, although that it might again be a place holder, in which case, a "cell regeneration" program is also delivered. That regeneration program will be invoked during two-dimensional ordering, when the top-down algorithm arrives at the leaf cell, knowing the external placement of signals. The regeneration program is given this context, and produces a new cell customized to that environment. For example, logic arrays will respond by ordering inputs and outputs optimized for the given context.

For the regeneration program, care is taken to first orient the external context to match most optimally the place-holder

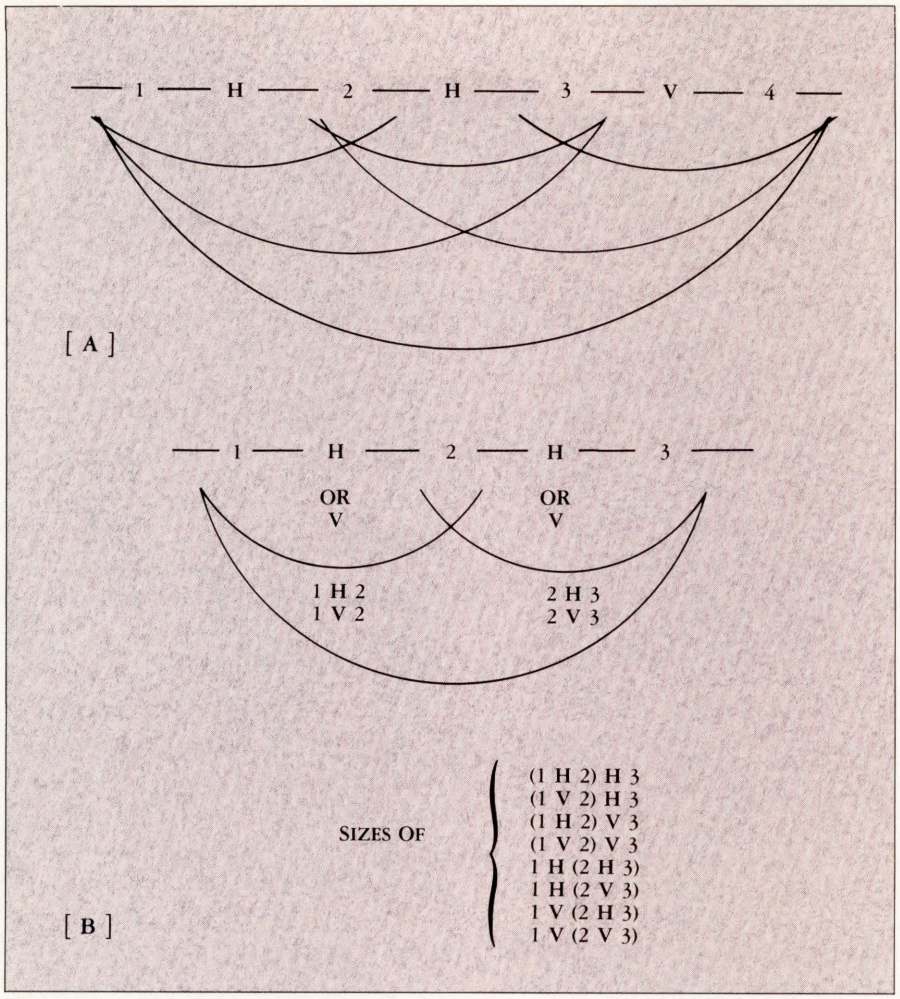

Figure 8. The occupancy of all possible phrase spans for the phrase "1 H 2 H 3 V 4" (A) is shown in (B).

cell. The regeneration is invoked within the oriented context, relieving the author of the regeneration program from considerations of alternative orientations. The resulting new cell is then oriented optimally within the actual context, as we do for any leaf cell in the hierarchy.

■ Equations and Many-To-One Mappings

Random logic specified as a set of Boolean equations may be implemented by a set of logic arrays. A given logic array may implement more than one equation, as is often the case for the most efficient implementation.

Grouping together highly communicating equations can be handled by the group-by-communications operation. We hide each equation under a dummy cell (size is unimportant) and apply the operation over the set of equations. We further optimize the resulting hierarchy by applying the prepacking ordering algorithm, and thus come up with a hierarchy of equations that has heavily communicating equations close to one another.

Traversing the hierarchy once again, we will see lists of equations at the lowest level. By combining sequences of adjacent equations into individual logic arrays, the overall hierarchy is transformed into another hierarchy, which has fewer (but real) cells as leaves. The automatic floor-planning can continue at the packing step.

■ Conclusions

This new automatic floor-planner has been successfully used for more than 100 projects. When the users' cells are blocks, (significantly larger than individual standard cells), the floor plans look almost as though the cells had been designed especially to fit within those floor plans. Figure 1 is a typical finished layout derived from the floor plan. The thicknesses of the wiring shows how well the floor plan brings highly communicating cells together, realizing that floor-planning is not just a packing job.

There are some special cases, such as standard floor plans with standard cells, for which the results are better than our methods. In extreme cases, standard-cell floor plans, with placement solved by simulated annealing, have achieved results 60 percent of the size achieved by our methods. But when cells are small, custom block generators (for datapaths, logic arrays, or standard cells with specific floor plans) produce the best results, and these blocks are the ideal candidates for floor-planning using our methods.

All features described here have been implemented , including the involvement of block generators and the application to sets of equations, with consistently successful results. All logic arrays produced for sets of complex equations were significantly smaller than an equivalent implementation in terms of standard cells. ■

Acknowledgments

We are grateful to Brent Nelson at the Brigham Young University and to Steve Burns at the California Institute of Technology for submitting the majority of fusion jobs having unspecified floor plans. Steve Burns also provided the simulated annealing alternative for standard cells.

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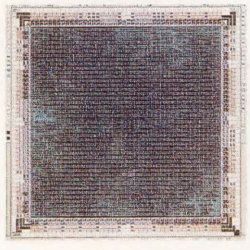

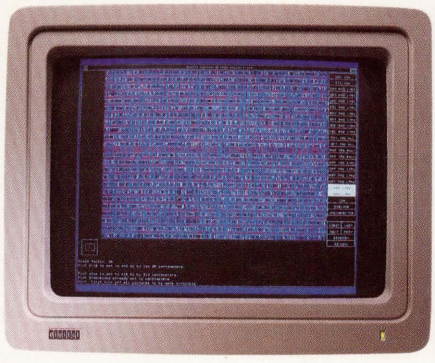

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Heterostructure FETs

Building a Better Transistor, Atom By Atom

RODERIC BERESFORD, SOLID STATE EDITOR

BEHIND THE CLOSED doors of the electronics industry's solid-state technology laboratories, scientists and engineers are scouting the prospects for a next-generation compound semiconductor technology that will produce a faster, higher transconductance, lower noise, more manufacturable transistor than today's best gallium arsenide MESFET process can muster. With the rapid developments and promising results to date, the question is not so much if but when heterostructure FET technology will make a contribution to digital LSI circuits.

No one knows the exact answer to that question, although some people say three years and some say much sooner. Industry insiders think that the first applications will be inside a Fujitsu Ltd. supercomputer. Fujitsu chooses not to say so explicitly; its published technical accounts call heterostructure FET ICs "ready for the next-generation mainframes and supercomputers."

In the U. S., AT&T Bell Laboratories is the acknowledged front-runner, thanks to the Defense Advanced Research Projects Agency, which is funding a pilot fabrication line for HFETs—also called high electron mobility transistors (HEMTs). Research programs are also underway at other laboratories, including those of Hughes, Honeywell, IBM, and Hewlett-Packard.

That research and development has been driven primarily by the extremely high electron mobility that can be achieved in aluminum gallium arsenide/gallium arsenide heterostructures grown by molecular beam epitaxy. While these intrinsic FET performance measures, obtained near absolute zero, far surpass anything available in conventional GaAs or silicon technologies, they may not be important or even relevant to digital applications of HFETs. To help in understanding what will be important, this article paints a portrait of HFET technology today, including device principles, circuit design, demonstration ICs, and recent research results, such as the highest transconductance and cutoff frequency yet for any FET. A comparison with heterostructure bipolar technology—preferred by companies such as Rockwell International and Texas Instruments—rounds out the picture.

■ ENGINEERED MATERIALS

Molecular beam epitaxy is the key to fabricating heterostructures, which require atomically perfect interfaces between different semiconductors. Heterostructures in turn are the key to a higher performance FET, whose high transconductance is mostly a matter of engineering a high electron density in a thin layer of extremely pure GaAs or a related semiconductor. (For an introduction to the basic concepts of heterostructure devices, see "Inside High-Mobility Devices" on page 100.)

As shown in Figure 1, an advanced MBE system priced at well over $1 million consists of several ultrahigh vacuum chambers and occupies a large room. The system pictured is built by Varian Associates (Palo Alto, Calif.), at the moment the only U.S. source of MBE equipment (Japanese and French companies also produce the gear). MBE growth tends to be slow, not batch-oriented, and therefore expensive: Commercially available MBE material on GaAs substrates may cost up to $4,000 per wafer.

There are currently three MBE systems on line at AT&T Bell Laboratories' HFET pilot fab in Reading. In its second year of a four-year DARPA contract, AT&T appears bullish on HFETs. In fact, according to Stuart H. Wemple, department head for GaAs IC Products, the AT&T program results suggest that there will be a yield advantage to HFETs compared with conventional GaAs MESFETs, thanks to better parameter control.

"This is going to end up being the low-cost way to go for GaAs ICs," he predicts. The advantage comes from the use of MBE, in which layer thickness and composition can be controlled precisely, and the fact that HFET parameters like threshold voltage are determined by the epitaxial growth conditions. In contrast, conventional GaAs MESFET parameters depend on channel implants, which are poorly controlled in comparison. Thus, the relatively

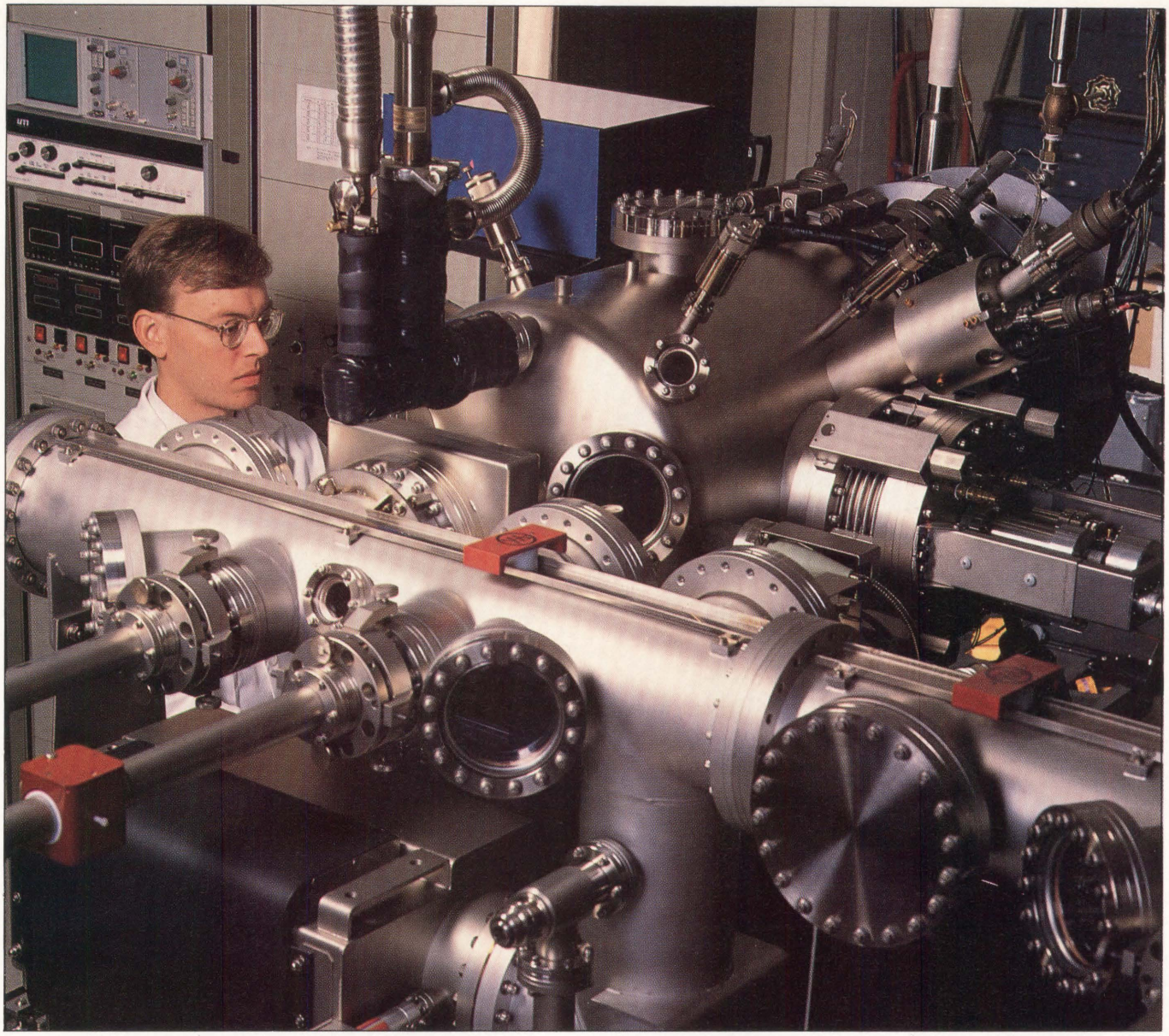

Figure 1. One growth chamber of the three-chamber molecular beam epitaxy system in operation at Columbia University in New York City. Under the direction of Professor Wen I. Wang, the facility is used to develop new materials and devices for electronics and optoelectronics.

high cost of MBE material may be more than offset by the effects of its process-control advantages.

While "scaling up" efforts such as AT&T's swing into high gear, researchers continue to exploit MBE in pursuit of ultimate performance. If the first chapter in this story was the precise control of layer composition and thickness, leading to the HEMT, the second chapter, now being written, is the technology of pseudomorphic heterostructures, in which material structure itself comes under the engineer's control.

All epitaxy needs a starting substrate, which normally dictates the lattice constant (atomic spacing) of the subsequent layers. The only suitable substrates at this point are GaAs and InP, limiting technologists to two "families" of materials. In pseudomorphic growth, however, a thin epitaxial layer is coaxed into adopting the lattice constant of the substrate instead of its own preferred spacing. In this way materials can be optimized for their transport properties with less regard for the constraints of crystal growth.

■ Record-Breaking Device Performance

Pseudomorphic HFETs hold the records at the moment for FET performance. In a development that will be presented at the upcoming International Electron Devices Meeting in San Francisco (December 11-14), the husband-and-wife team of U. Mishra and A. Brown along with S.E. Rosenbaum of Hughes Research Laboratories, Malibu, Calif., have investigated the dc and rf performance of 0.1-μm gate length pseudomorphic HFETs in the AlInAs/GaInAs system. These are the first 0.1-μm pseudomorphic HFETs on InP substrates and they show a transconductance of 1160 mS/mm, the highest value ever reported for a HEMT. Furthermore, the extrapolated cutoff frequency is 205 GHz, making this the first transistor to crack the 200-GHz barrier. Mishra and Brown were also invited to speak on the subject at the recent Gallium Arsenide IC Symposium, held November 6-9 in Nashville, Tenn. (The pair recently left Hughes for North Carolina, she to the Army Research Office and he to North Carolina State University.)

Although widely considered outstanding work, the Hughes efforts are by no means singular. In fact, since pseudomorphic HFETs are a natural follow-on to HFETs, they are evolving in parallel at the major laboratories. AT&T's Wemple notes that Bell Labs in Murray Hill, N.J. is also

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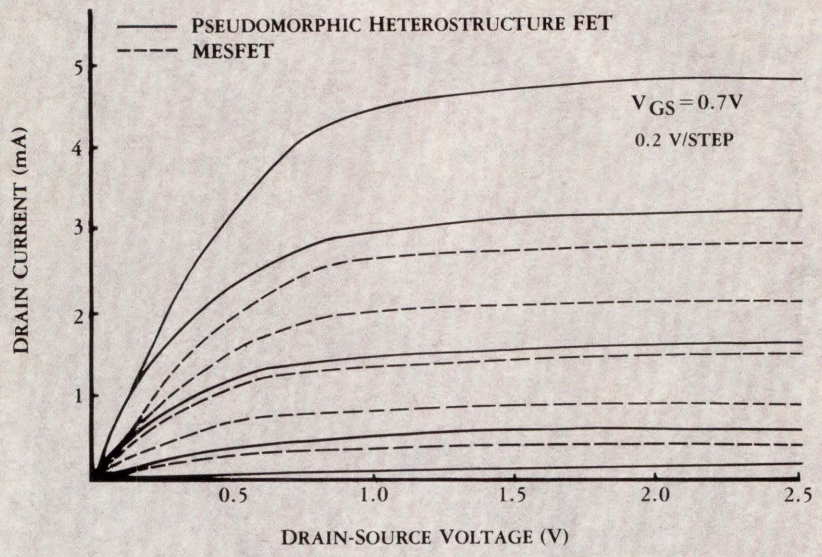

DEVICE TYPE	THRESHOLD VOLTAGE (V)	TRANSCONDUCTANCE (mS/mm)	MAX CURRENT (mA/mm)
MESFET	−0.5	175	150
HETEROSTRUCTURE FET	−0.3	250	180
PSEUDOMORPHIC HFET	−0.15	450	240

Figure 2. Comparison of 1-μm gate length (20-μm width) FETs: drain current characteristics show the high current and transconductance attained by a pseudomorphic HFET. The table also includes data for a lattice-matched HFET.

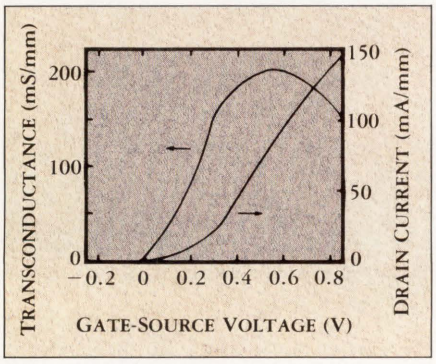

Figure 3. Typical dc characteristics of a 1.2-μm gate length HEMT (after Watanabe et al., 1987). Because the transconductance falls off at higher gate voltages, HEMT logic families need to limit voltage swings to about 0.7 V.

pursuing pseudomorphic HFETs (although not under the DARPA program) and has "seen results comparable to any of the 'hero' papers," a light-hearted reference to recent communications in *Electron Device Letters*, which typically report about a 50 percent higher carrier velocity in pseudomorphic GaInAs compared to GaAs. PHFET results have been reported by many groups, including General Electric, Texas Instruments, Matsushita, Cornell University, Massachusetts Institute of Technology, and the Universities of Illinois, Michigan, and Minnesota.

The question of performance comparison among PHFET, HFET, and conventional MESFET technologies is a sticky one, thanks to the usual practice of omitting from published accounts some of the details necessary to completely characterize a given technology. However, until last month when its doors were shut due to financial problems, Gain Electronics Corp. of Somerville, N.J., was selling MBE material for HFETs, and according to Rudi Hendel, vice president of Process Development, the company had done comparison studies at the device level on all three technologies.

The GaInAs material involved here has a 15 percent lattice mismatch with GaAs, which can be tolerated for channel thicknesses up to 10-20 nm. Gain's standard HFET AlGaAs/GaAs technology gives 250 mS/mm transconductance for a 1-μm device, while a comparable pseudomorphic device has 450 mS/mm. In Figure 2, the comparison data for PHFET, HFET, and MESFET devices clearly show the significant advantage in current drive obtained with PHFETs, thanks to the higher transconductance. This comparison is not entirely fair, in that the experimental devices do not have the same threshold voltage as the production MESFET; however, the discrepancy handicaps the HFET devices so that the advantages are presumably even greater than what's shown.

Gain also put target PHFET device parameters into a SPICE simulation to compare the performance of gate array macros like flip-flops and found the improvement to be at a factor of two. Hendel summed up the advantages this way: "You can either keep the device area the same and use the increased current to drive the interconnect capacitance faster or you can shrink the transistor and get the same speed [as MESFETs] with a smaller die size and smaller capacitances."

Although increased drive current may be an HFETs most important advantage when it comes to contemplating LSI circuit applications, it is not the only improvement over MESFETs. For a given gate length, you get a cutoff frequency that's about two times higher with HFETs than it is with MESFETs (Abe et al., 1987), as well as what appears to be an inherently lower noise figure. Both of these pluses are important for analog applications.

In fact, at Triquint Semiconductor (Beaverton, Ore.), a prominent supplier of GaAs MESFET technology, HFETs are viewed as a much less certain step in the digital realm than in microwave applications. Rich Koyama, director of Triquint's manufacturing, says that "ion-implanted MESFETs, properly designed, are almost the equal of HFETs in transconductance." On the other hand, he notes that even today, 0.25-μm HFETs are practically the norm in microwave applications. While it may be true that MESFETs can almost keep up with HFETs in transconductance, data from Fujitsu clearly show that MESFETs suffer major short-channel effects (threshold voltage shifts) at gate lengths below 1 μm, while HEMTs are pleasantly well-behaved (Notomi et al., 1987).

■ HFETs IN CIRCUIT DESIGN

From the circuit designer's perspective, HFETs have so much in common with MESFETs that digital circuit designs developed for GaAs MESFETs can be ported virtually unchanged. HFET ICs have used, for example, direct-coupled FET logic (Fujitsu) and capacitively enhanced logic (Hughes). What circuit designers would really like, however, is not a power-inefficient depletion-load circuit family, but a complementary device technology like CMOS. Researchers at IBM are in fact developing complementary HFETs, which would create the circuits of choice for data processing applications, provided the p-channel device parameters can be improved.

As is the case with MESFETs, HFET logic swings are limited because the gate contact is a Schottky barrier that will conduct excessively if the forward bias is too large.

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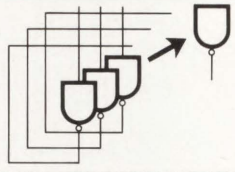

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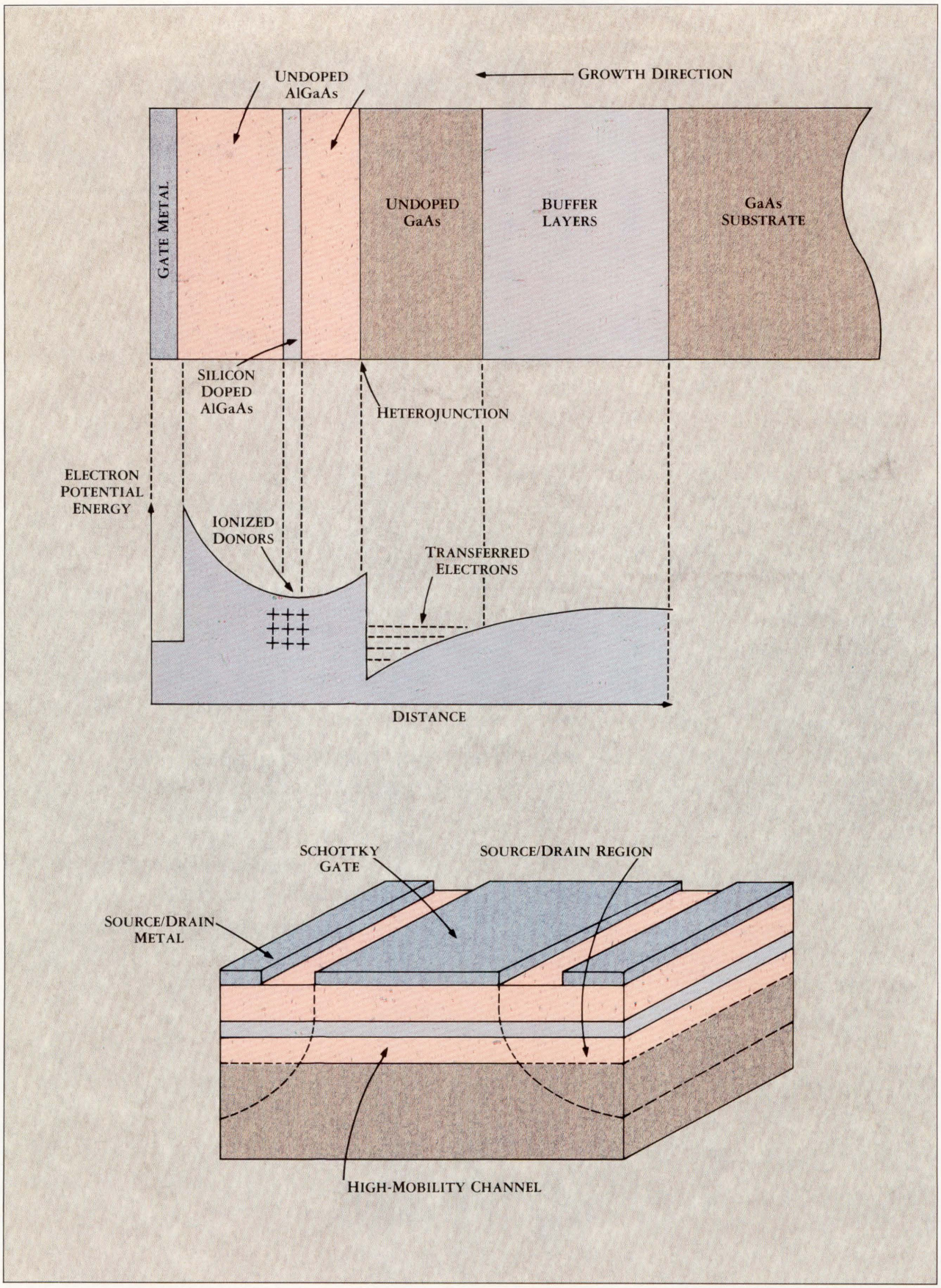

Figure A. Cross-section of an MBE wafer shows the layer growth sequence (top); the resulting electron potential energy profile suggests how charge contributed by the dopant atoms transfers to the "notch" just right of the heterojunction. Below, sectional view of an HFET shows how the gate metal may be used to self-align the source/drain implant; the alternative is to alloy the source/drain contacts.

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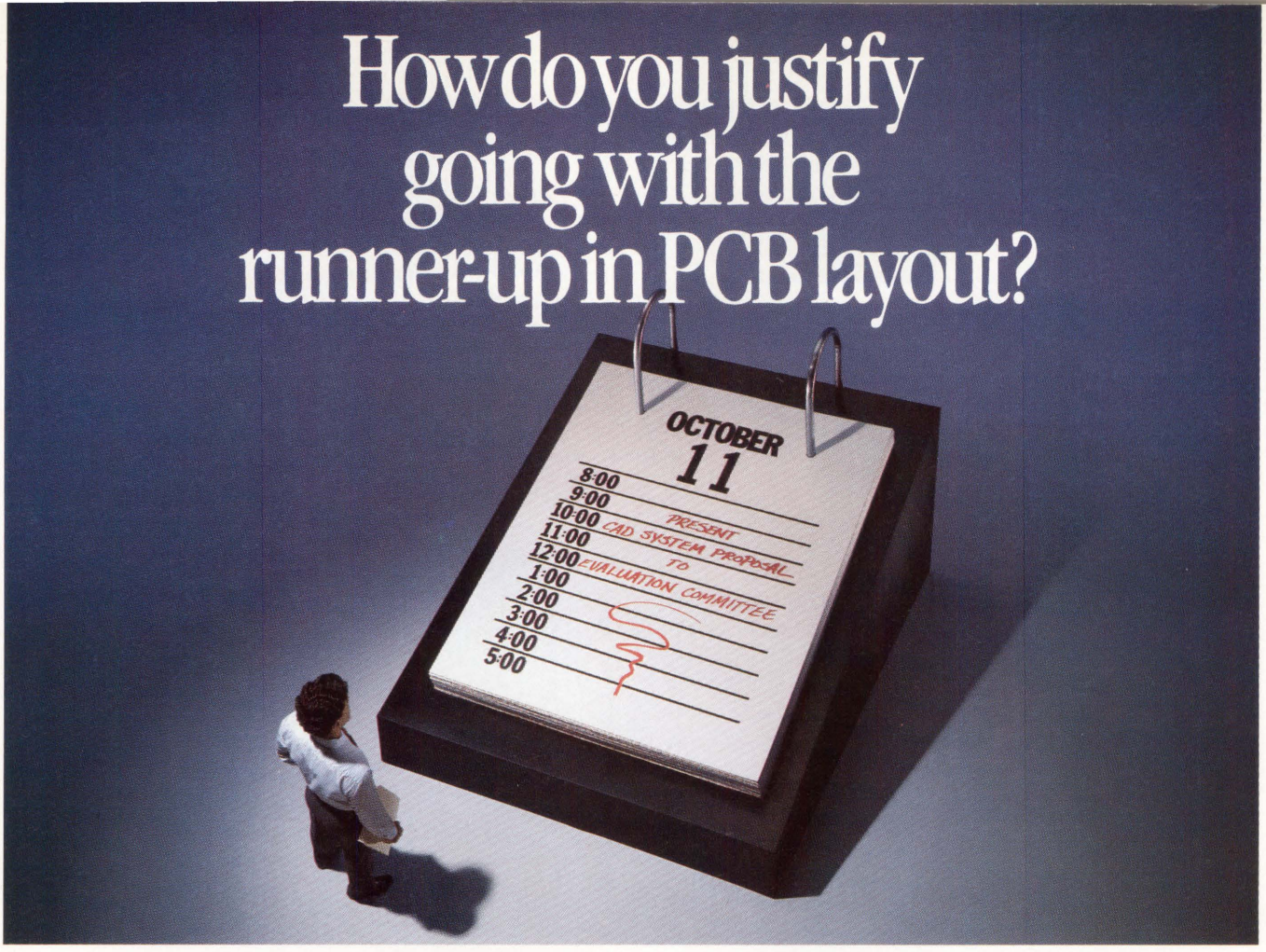

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HFETs have another related limitation, which is illustrated in Figure 3.

Above about 0.5 V, the HFETs high transconductance starts to roll off. Therefore, to maintain high performance, logic swings need to remain around 0.7 V or lower. That, according to Fujitsu, is the reason to prefer direct-coupled FET logic, whose logic swing nicely matches that requirement. Figure 4 shows the DCFL circuit technique, along with the buffered FET logic (BFL) and capacitively enhanced logic (CEL) circuit techniques—the other two most common circuit families.

DCFL has the drawback that the device parameters must be tightly controlled. Fujitsu also builds two different versions of DCFL, with different depletion thresholds for operation at room temperature and at 77 K. For low temperature operation, the depletion threshold is more

Inside High-Mobility Devices

Heterostructure FET evolution began with the high electron mobility transistor (HEMT, SDHT, MODFET), a field-effect device in which the carrier density in a semiconducting channel is changed by the voltage on a metal gate. The more electrons, the more conductive is the channel. So far, that's precisely the same principle as a MOSFET or conventional MESFET. Since the voltage cannot be increased substantially, the number of electrons in a conducting channel has a practical maximum. However, the conductance can also be increased if the electrons move faster, hence the HEMT. How fast they go, roughly speaking, depends on how often they scatter and lose energy.

In a perfect infinite crystal at absolute zero, an electron will never scatter—it is infinitely mobile. In a real finite crystal at non-zero temperature, an electron can scatter from crystal structure defects, from the lattice vibrations excited thermally, and from impurities in the crystal. Even at room temperature, impurity scattering is important, and as the temperature is reduced, it is a major limitation unless exceptionally pure material is used. As it happens, we can make material that pure, but without intentional doping, there won't be enough electrons around even to measure their mobility, much less make a useful device.

The HEMT is made possible by two maneuvers: The dopant atoms are removed to a nearby layer, leaving the gallium arsenide channel region pure (see Figure A on page 98). Just as important as this "modulation doping," however, the nearby doped layer must have less affinity for electrons. The alloy aluminum gallium arsenide typically is used for the low-affinity layer.

AlGaAs is a useful material because its lattice constant matches that of GaAs and its bandgap changes with the fraction of Al in the alloy. The conduction bands of GaAs and AlGaAs line up such that electrons see about a 0.3-eV barrier between the two materials in a typical device (the heterojunction effect). Under these conditions, the electrons contributed by dopants in the AlGaAs transfer to the GaAs channel region. Since they are then separated from the dopant ions, the electrons' scattering is much reduced. A typical HEMT channel exhibits electron mobility at room temperature 5-10 times higher than that of doped GaAs.

■ Saturation Velocity is the Key

Unfortunately, that high mobility is found at low electric fields only. At higher fields, the mobility quickly heads toward zero: Once "velocity saturation" is reached, pumping more energy to the electrons just increases their scattering, transferring the energy to the crystal lattice instead of into electron motion. This phenomenon is illustrated in Figure B,

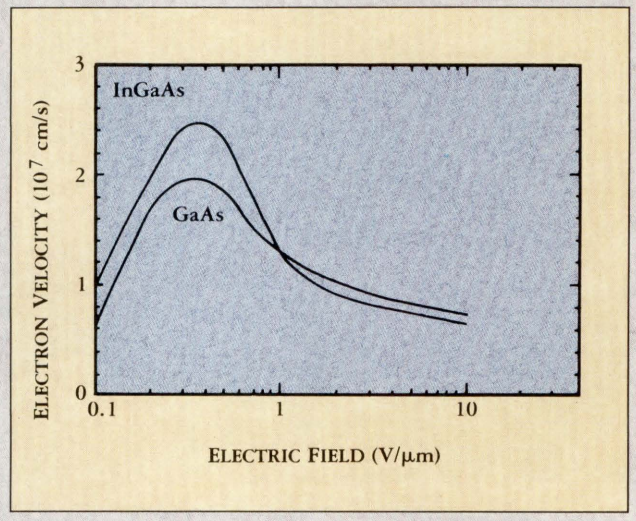

Figure B. Electron velocity as a function of electric field. Indium gallium arsenide alloys have significantly higher carrier velocities than gallium arsenide for moderate fields, leading to improved device transconductance.

which plots electron velocity versus applied electric field for two materials. In transistor applications, several volts may be applied across a channel of a micron or less, putting us well into the high-field regime. Thus, the more important parameter for devices is the saturation velocity, not the low-field mobility.

Realizing this distinction, researchers have considered indium arsenide, which exhibits a saturation velocity 4-5 times greater than that of GaAs. Prospects for an InAs transistor technology are unclear, because the material is not well developed and semi-insulating substrates are not available. However, indium phosphide is available as a semi-insulating substrate and, with just the right compositions, the alloys GaInAs and AlInAs lattice-match InP. So a heterostructure FET can be migrated from the AlGaAs/GaAs system to the AlInAs/GaInAs system. The saturation velocity of GaInAs improves over that of GaAs, but not surprisingly, it's not as good as for pure InAs.

In order to get around the composition constraint imposed by the need to match lattice constants (and thereby try to improve performance), an approach gaining favor is to grow "pseudomorphic" alloy layers. The name arises from the fact that the epitaxial layer starts growing by adopting the crystal structure of the host (the fake morphology), rather than its own. Only after a certain thickness of material is built up will the internal stress generate defects in the material as it tries to adopt its preferred structure. Pseudomorphic GaInAs and AlInAs layers can be grown on InP or GaAs substrates.

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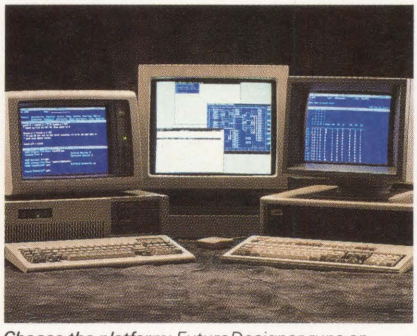

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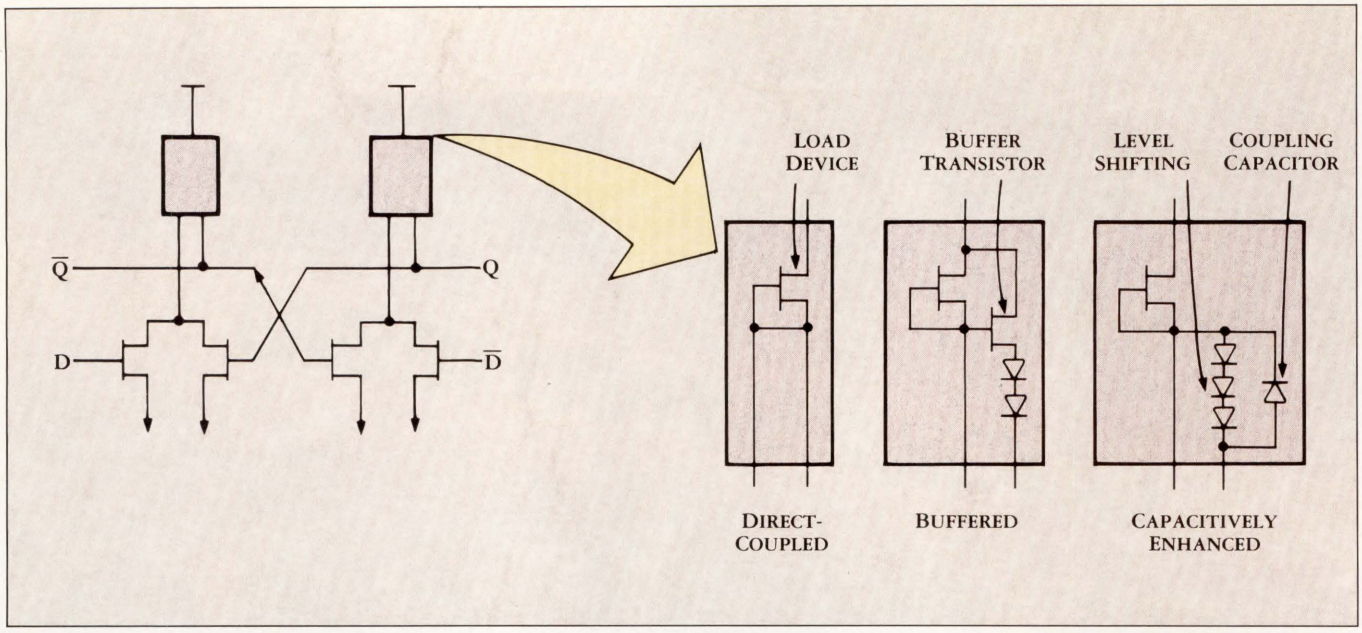

Figure 4. Comparison of FET logic families. The asynchronous latch pictured at left would require the load connections shown in the trio of insets, right. (Pull down connections for BFL and CEL are omitted in this drawing.)

negative to take advantage of the increased "drivability" of the gate. In the room-temperature version, the thresholds are at 0.22 V (enhancement) and −0.55 V (depletion) with a 0.2-V noise margin and 1.6-V supply voltage. Standard deviations in the thresholds across a wafer are reportedly 17 and 59 mV or 7.7 and 10.7 percent for enhancement and depletion devices, respectively (Kajii et al., 1988). A basic DCFL inverter dissipates 1 mW and drives a "standard" load (fan-out of 3 plus wiring) in 110 ps.

BFL can drive high fan-outs faster, but it also consumes more power, as is clear from the circuit drawings in Figure 4. According to the work done at Hughes, where CEL is preferred, the back-biased diode used as a coupling capacitor passes the fast switching currents. Since the current in the level-shifting diodes then does not set the gate speed, that current can be reduced for a power consumption advantage. In 25-GHz divide-by-two circuits built at Hughes, CEL dissipates 64 mW versus 450 mW for BFL (Jensen et al., 1988).

Ultimately, a very-low-power complementary HFET technology may be feasible, based on work underway at IBM's Watson Research Center. Richard A. Kiehl and his colleagues are combining n- and p-channel HFETs by stacking up the necessary epitaxial layers for both devices and etching away one set where the other type is needed (Kiehl et al., 1987). P-channel FETs in gallium arsenide are usually poor performers, because holes are some 20 times less mobile than electrons (5 times less mobile at 77 K). However, based on measurements of 1.5-μm devices, this group projects that they will be able to achieve room-temperature transconductances of 55 mS/mm in 0.7-μm p-channel HFETs, which compares well with 280 mS/mm for the n-channel partner. Kiehl is aiming for a CHFET technology that would offer 160-ps gate delays, and thanks to low-power complementary circuits, a power-delay product about 10 times better than all n-channel HFET technology.

■ Test Driving the Technology

A useful overall figure of merit for LSI technologies, the power-delay product for HFETs looks good indeed. Fujitsu's 0.5-μm HEMT technology sits right around 0.1 pJ (room temperature), based on measured gate delays of 35 ps at power dissipations of 3 mW in 5.5-GHz frequency dividers. Micron for micron, GaAs MESFET technologies are three to ten times worse (slower and higher power).

Most of the significant HFET demonstration vehicles that have been discussed publicly come from Fujitsu, including a 4,096-gate array and 4K static RAM. At AT&T Bell Laboratories, the DARPA pilot line program involves a sequence of demonstration chips of increasing complexity, which so far has resulted in a 6×6 multiplier, 16:1 multiplexer, shift registers, and in all, some eight low-integration-level test vehicles. According to Wemple, the next round is underway, with 3-5K gate chips in design. Depending on your level of optimism, AT&T could be viewed as two to three years behind Fujitsu, which submitted results on its 4K gate array (a 16×16-bit multiply in 5 ns) more than a year ago.

At the 1988 International Solid State Circuits Conference, Watanabe et al. from Fujitsu described a 4×9-bit data register geared for high data rates and low clock skew among the outputs. At about 1,100 gates, this chip is not pushing the limits of integration, but instead it's pushing the problems of high fan-out and delay variation that must be confronted in making practical circuits. The logic path from clock input to data output operated at 490 ps (an estimated 43 ps per gate), allowing the chip to run at clock rates over 1 GHz. No measurements of clock skew were published.

■ The Persistent Doubts

Are HFETs ready for real applications? The demonstration vehicles described show a capable and valuable technology, but every technology has its bugaboos and critical steps. The two critical ingredients of HFETs are high-quality MBE material and the selective dry etching of GaAs (stopping on AlGaAs). Both those elements have been demonstrated by many groups and in fact have become commercially viable via discrete devices for microwave applications. Still, there are subtle material problems that some think make HFETs a poor choice for LSI.

The AlGaAs alloy usually shows characteristic charge-trapping sites—cryptically called DX centers—that have been implicated in bad behavior of HFETs—collapse of the current-voltage characteristic and a persistent photoconductivity. Those kinds of problems lead George Heilmeier, senior vice president and chief technical officer of Texas Instruments, to say outright, "I don't see HEMTs being a big factor in the

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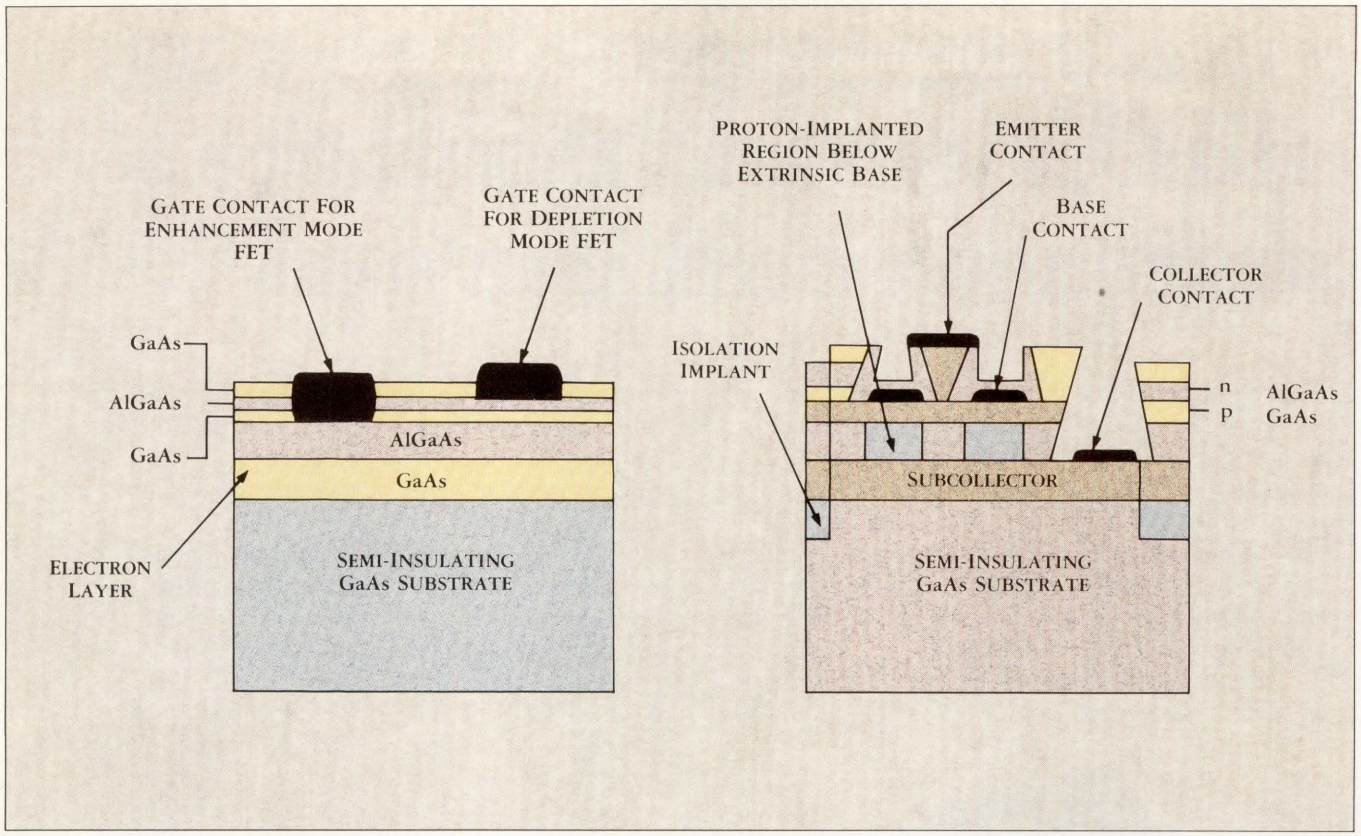

Figure 5. Process cross-sections comparing Fujitsu HFET (left) and Rockwell HBT (right). The HFET process requires selective etching to put the enhancement and depletion gates at the right depth (the alloyed ohmic contacts to source and drain are not shown). HBTs need a heavily p-type base and more layers than HFETs.

digital III-V regime." TI instead is emphasizing heterojunction bipolar transistors, which, as Heilmeier is quick to point out, offer higher power levels, lots of gain, and the ability to do analog/digital conversion as well.

HBT technology, like HFET technology, requires mastery of MBE growth (Figure 5). While it does not depend so critically on a selective etch, it has its own unique problem: Making a good HBT requires very high base doping, which may lead to segregation of the dopant and defect-ridden interfaces.

Rockwell International has perhaps pushed the hardest on HBT development, with notable success (Chang et al., 1987). In the words of Peter M. Asbeck, a researcher at the company's Science Center (Thousand Oaks, Calif.), "we have made HBT frequency dividers that operate up to 26.6 GHz, the limit of our test equipment. We believe these are the fastest frequency dividers in any semiconductor technology. For small-scale integration of ultra-high-speed circuitry, HBTs are unequaled. Rockwell is aggressively pursuing HBTs for larger digital circuits and A/D converters."

There is hardly a major electronics company without a stake in heterostructures, whether HFETs or HBTs. If Fujitsu and AT&T are proven correct on the manufacturability issue, HFETs may end up being a more practical technology than GaAs MESFETs, regardless of performance. With the performance edge already demonstrated, the ongoing research on pseudomorphic structures, and the hard logic of high-end system design, HFETs appear destined for an elite role in the highest clock-rate processors. ■

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The Rapid Prototype Machine implements ASIC designs in PGAs

ASIC Emulation Debugs ASICs And Their Systems

AS we all know, 95 percent of ASIC designs satisfy prototype test but 50 percent of them bomb when placed in their target system. Some suggest system-level simulation to shake out the ASIC design. This approach, unfortunately requires an enormous number of component models and CPU cycles to succeed.

Another solution is programmable gate arrays, but you could be stuck with one of a handful of potential suppliers. In addition, programmable products trail mask-programmed devices in speed and density.

Quickturn Systems, now led by Phil Kaufman, the ex-chief of Silicon Compiler Systems, has unleashed the potential of programmable gate arrays as a development vehicle for mask-programmed gate arrays. This startup's Rapid Prototype Machine (RPM) implements an ASIC design's gates in programmable gate arrays. A stimulus generator and logic analyzer can then exercise the design. Finally, an "in-circuit" interface allows the RPM to emulate the ASIC's function in its target system, acting as an ICE system for ASICs.

The ASIC design must first be processed on a Sun Microsystems' workstation, which can be embedded in the RPM. A fully-configured RPM can accommodate a 100,000-gate design containing one or more ASICs. The design's schematic netlist can be expressed in EDIF 2.0 or in the proprietary format of the following ASIC vendors: LSI Logic Corp., Fujistu Ltd., Daisy Systems Corp. and Mentor Graphics Corp. (an interface to Valid Logic Systems Inc. is due early in 1989). At present the design can use gate-array library components from LSI Logic's LCA10000 family and Fujistu's UH family.

In processing the design, workstation-based RPM software parses and expands the netlist, translates the library elements into elements in the Xilinx PGAs, partitions the design between PGAs, places and routes the designs in the PGAs and programs the devices. This overnight process, takes about 12 to 14 hours for a large design (20,000 gates, for example). Once the design is loaded, however, incremental design changes can be incorporated through incremental compiling.

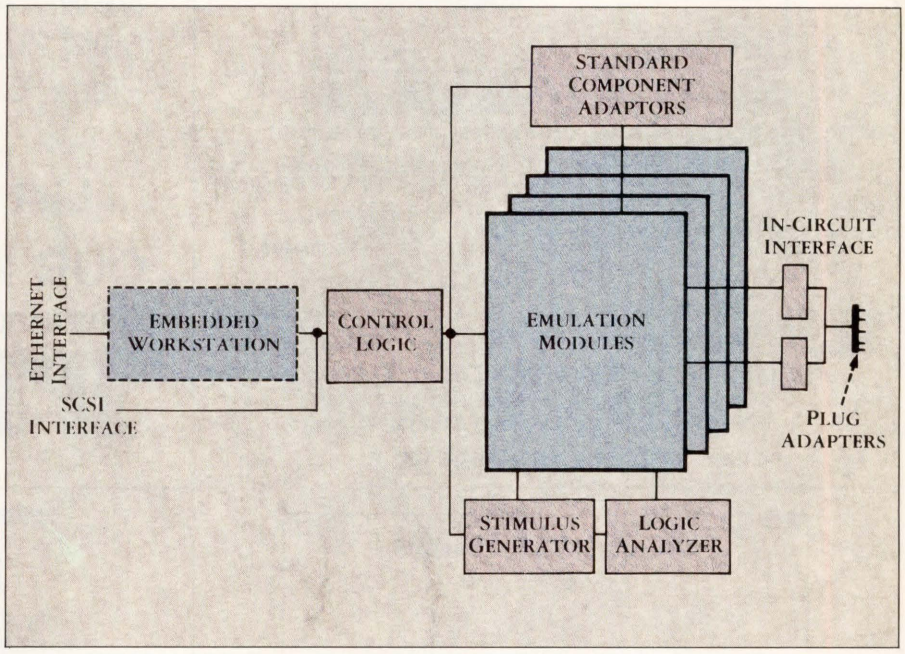

Figure 1. Quickturn System's RPM programs ASIC designs into its emulation boards. Users can then simulate the design, through the use of the RPM's stimulus generator and logic analyzer, and emulate the ASIC's function in its target system through an in-circuit interface.

After the design is loaded in, patterns can be run into it from the pattern generator. It is operated similar to a hardware-accelerated simulator, with gate functions implemented in hardware rather than software. Unlike a hardware accelerator, the entire design, rather than a few gate functions, exists in hardware. In this way, the ASIC design can execute millions of clock cycles each second.

To support the enormous number of vectors required for such simulation, the stimulus generator can accept simulation patterns in Daisy, Mentor and Valid formats, as well as a generic ASCII format.

The RPM is most effective when it emulates an ASIC in a target system. It provides that capability, in a manner similar to an in-circuit emulation (ICE) system. The the system plugs into the target system, operates similarly to the ASIC device and provides debugging capabilities. Running in emulation mode, all stimulus comes from the board so the logic analyzer can use all 128 channels.

The RPM chassis holds from one to four emulation modules. Each module contains enough Xilinx LCA programmable gate arrays to implement 25,000 gates of ASIC design. RPM connects to a workstation through a SCSI port.

The base system, with one module, is priced at $125,000. Shipments will start in the first quarter of 1989.

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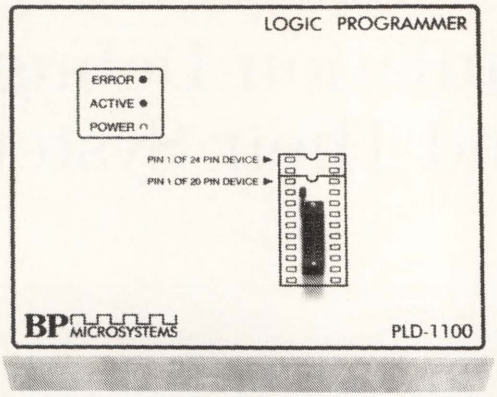

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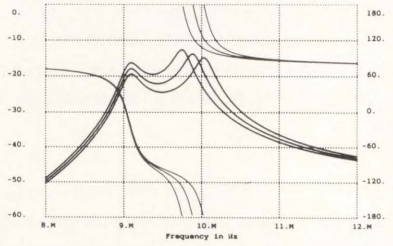

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Introducing Samsung CMOS Programmable Logic

We would never claim that CMOS programmable logic isn't already on the market. Because it is.

But it's never succeeded in becoming a *real* alternative to bipolar PALS®—despite the considerable advantages of low power.

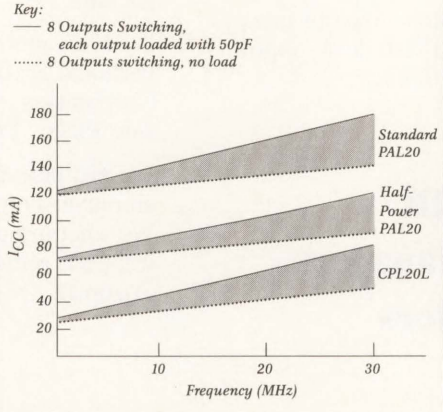
High costs and the lack of a strong volume manufacturer have simply kept CMOS programmable logic from being used, in all but a very few designs.

Samsung CPL™ changes that.

We're producing CPL (CMOS programmable logic) in volume. And we're offering it at a price that actually makes it competitive with bipolar PALs.

And as a result, CPL is the first *viable* low-power replacement for bipolar PALs.

CPL reduces power dissipation 70% compared to bipolar PALs.



Samsung CPL Parts

CPL20		*CPL24*	
CPL16L8	*CPL16R6*	*CPL20L10*	*CPL20R6*
CPL16R4	*CPL16R8*	*CPL20L8*	*CPL20R8*
		CPL20R4	

Speed options: 25 ns, 35 ns
Power options (Icc max.): 45 mA; 70 mA

Cut your power consumption 70%.

CPL will let you cut your power consumption a full *70%*. By directly replacing the bipolar PALs in your existing design.

With no new development tools. And with no redesign.

And that isn't all that CPL will do for you.

It will also give you parts that are more reliable. Because unlike bipolar PALs, our UV-erasable CPL devices are repro-

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Reality.

grammable. And we use that feature to offer parts that are 100% tested. Every single CPL device we ship has been subjected to programming, AC, and functional testing, and you can design them in with complete confidence.

Start prototyping immediately with our CPL starter kit.

Developing new, low-power designs with CPL is easy, and you can do it with existing tools. But we're also offering a low-priced Starter Kit so *everybody* can get started quickly.

The Starter Kit includes a software package designed by Personal CAD Systems and based on CUPL. It also includes samples of CPL20 and CPL24 devices, which are supported by the Starter Kit.

Since CPL devices are reprogrammable, this means the Kit provides everything you'll need to prototype and debug new designs.

The Starter Kit also includes CPL20 and CPL24 samples, a CPL data book, a CUPL manual, a Programmable Logic User Guide (PLUG) interactive diskette, and a booklet that leads you step-by-step through programmable logic design. It's priced at just $220.

Get started cutting power today. Use the coupon below to request free CPL samples, a data book, or CPL Starter Kit information. Or call Samsung CPL Marketing now at (408) 434-5400.

Send to Samsung CPL Marketing,
3725 North First Street, San Jose, CA 95134-1708

Please rush me:
☐ *Free CPL samples*
☐ *A CPL data book*
☐ *Information on the CPL Starter Kit*

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SAMSUNG
Semiconductor

CIRCLE NUMBER 28

Trust S-MOS. Our ASICs won't leave you out in the woods.

Instead, we'll help you along the path to higher productivity.

Through high-volume, high-yield technology, our manufacturing affiliate Seiko Epson Corp. produces millions of ASIC devices each month.

S-MOS backs up that production with a dependable design program that provides back annotation simulation and fault grades every chip to help your designs succeed.

To keep costs low, there are no CPU simulation charges.

Our full line of ASICs are migratable from gate arrays into standard cells and beyond to our Compiled Cell Custom cell-based designs.

Our ASIC solutions span from 513 to 38,550 gates with technologies down to 1.2 micron (drawn).

To save you time, we can use your existing arrays as future building blocks.

Most ASIC products are available in plastic quad flat packs, pin grid arrays, plastic leaded chip carriers, small outline packages and plastic dual-in-line packages.

So if you're looking for an ASIC program that will get you out of the woods, call us.

(408) 922-0200.

S-MOS SYSTEMS

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