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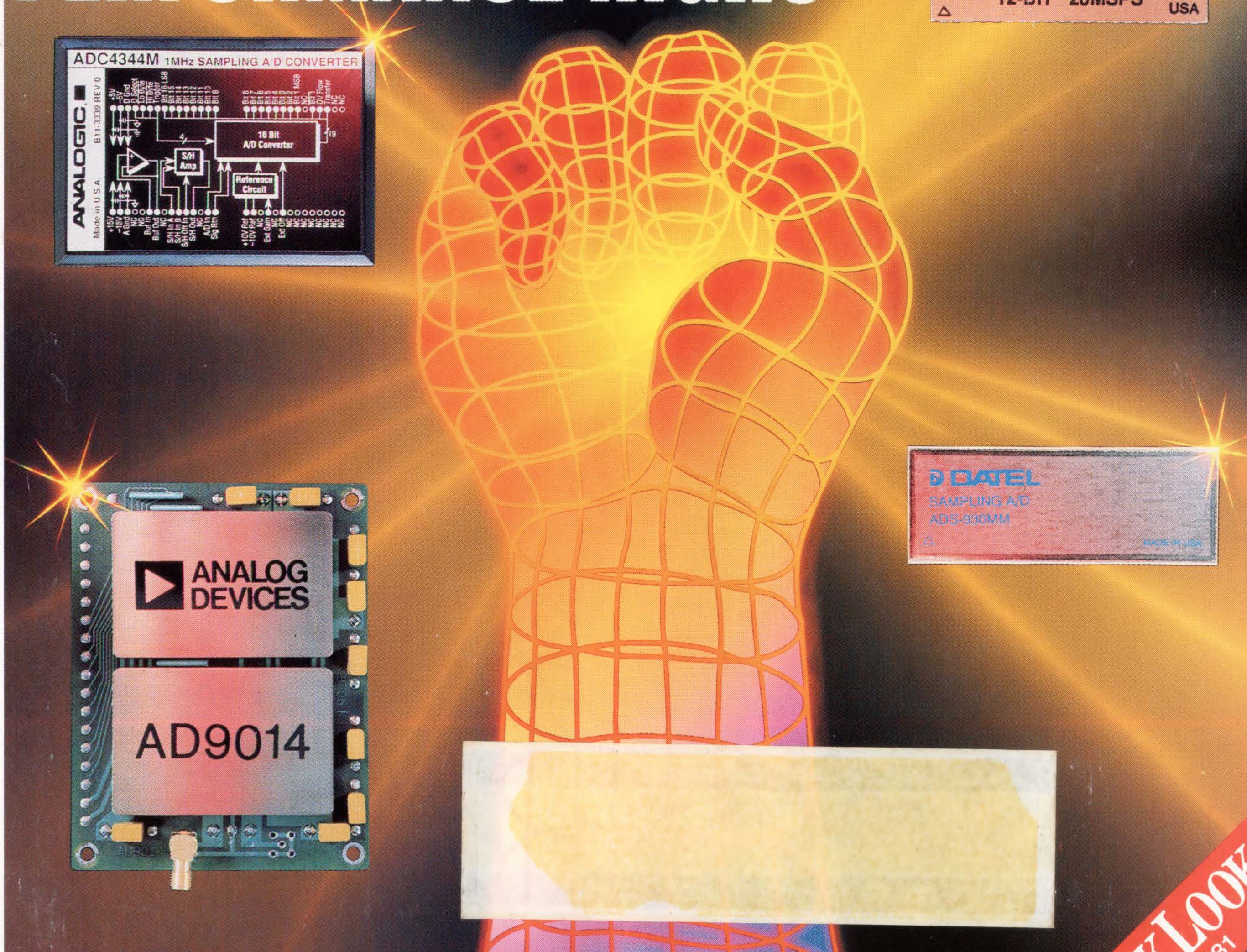
SEPTEMBER 13, 1990

HYBRID 12-TO-16-BIT ADCs SET NEW PERFORMANCE HIGHS

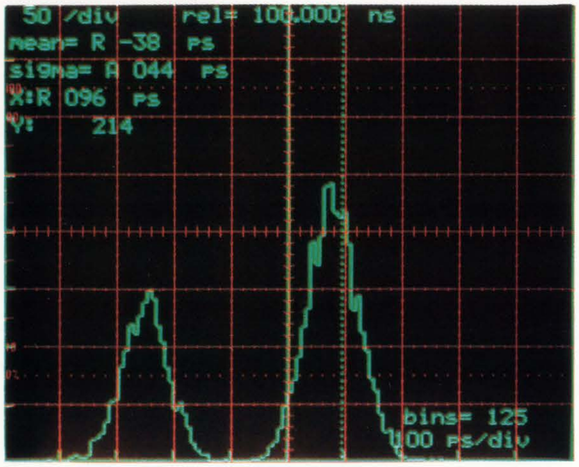


• ENCODING TECHNIQUE OPTIMIZES FPGA DESIGNS

QUICKLOOK PAGE 81

A picture is worth a thousand points in a time interval measurement.

SR620 Output



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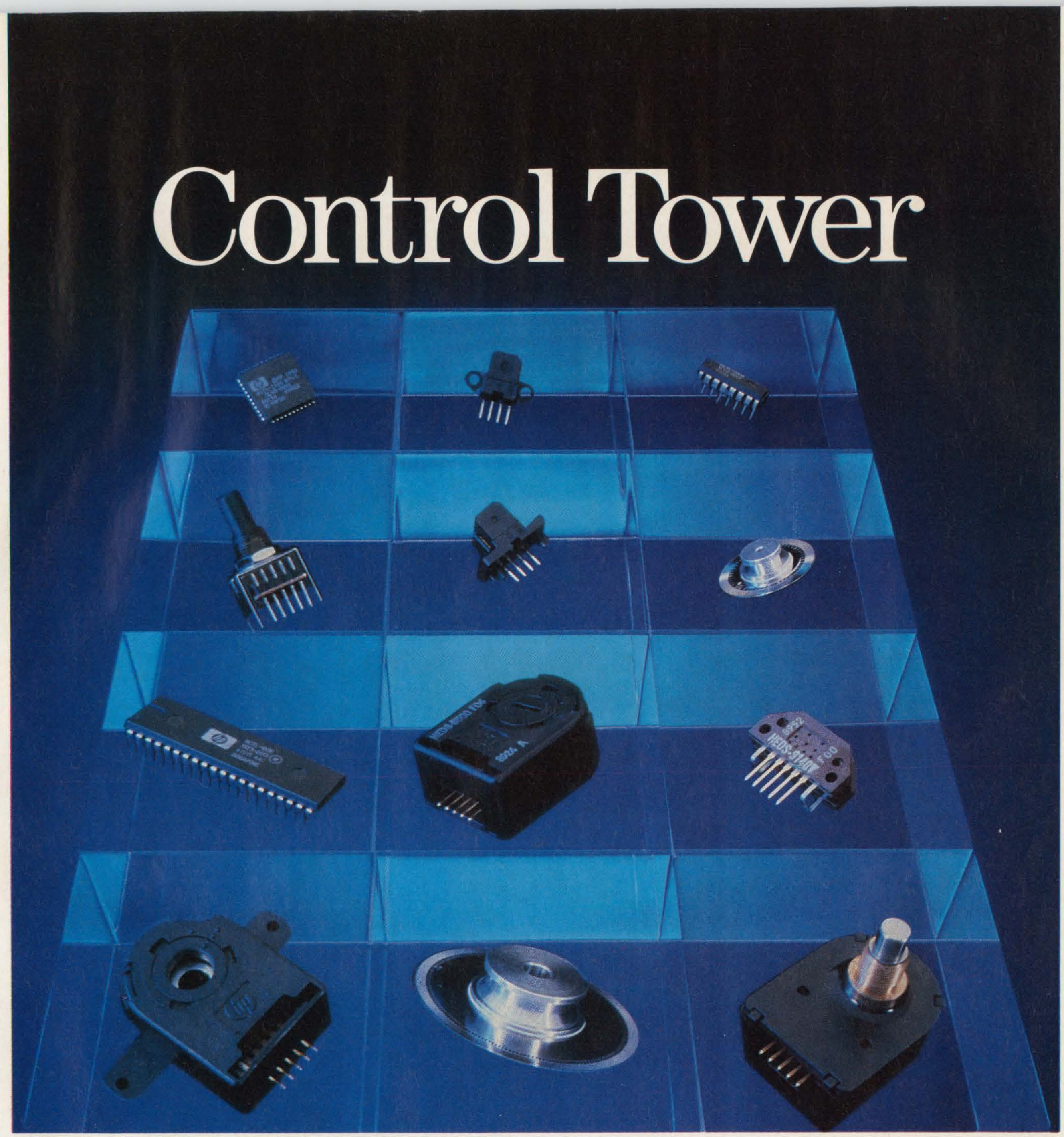

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SEPTEMBER 13, 1990 VOL. 38, NO. 17

ELECTRONIC DESIGN

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Cover photo: Jook Leung

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- How important are analog design skills for engineers in the future?
- How do the design skills of today's EE graduates stack up against those of young engineers of the past?

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COMING NEXT ISSUE
- Special Report: Graphics ICs take on more functions
- Memory-system-design feature: Designing a secondary cache for the 80486 microprocessor
- Evaluate microprocessor system architectures with a hardware modeller
- First details on a new, minimum-count PC chip set
- Pease Porridge: What's All this Noise Stuff, Anyhow? (Part 1)
- A new image-processing chip set offers expanded options
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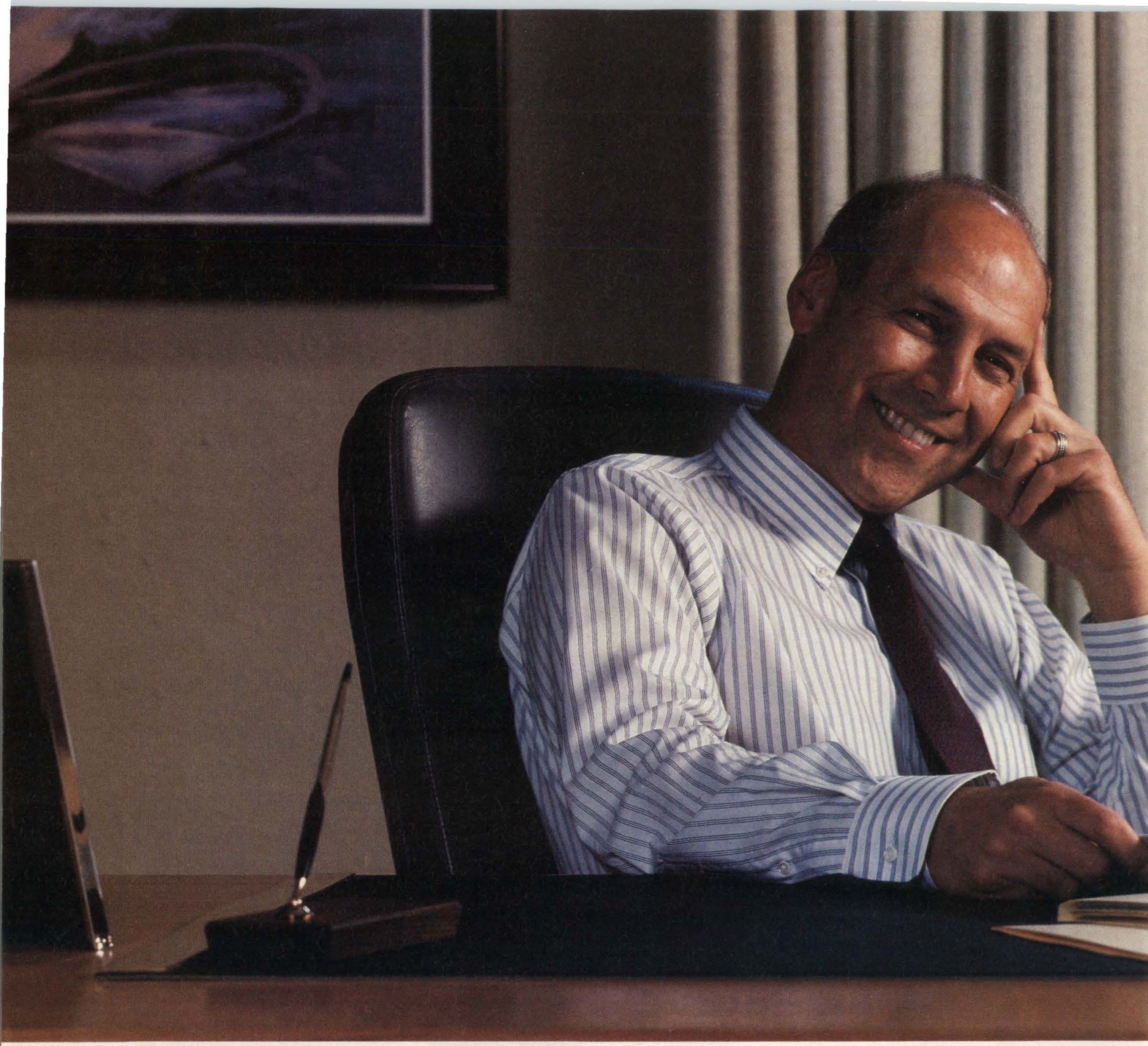

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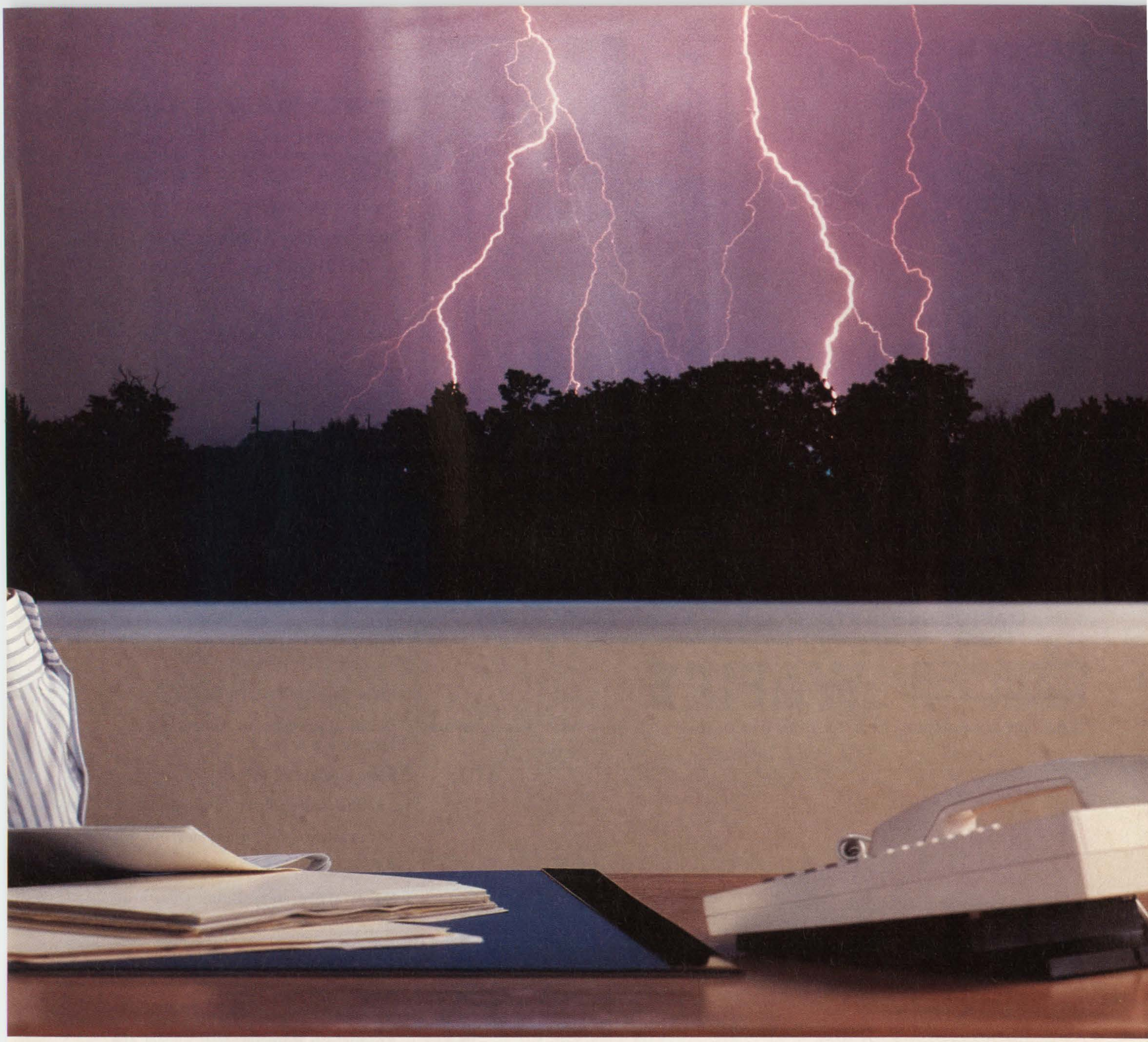

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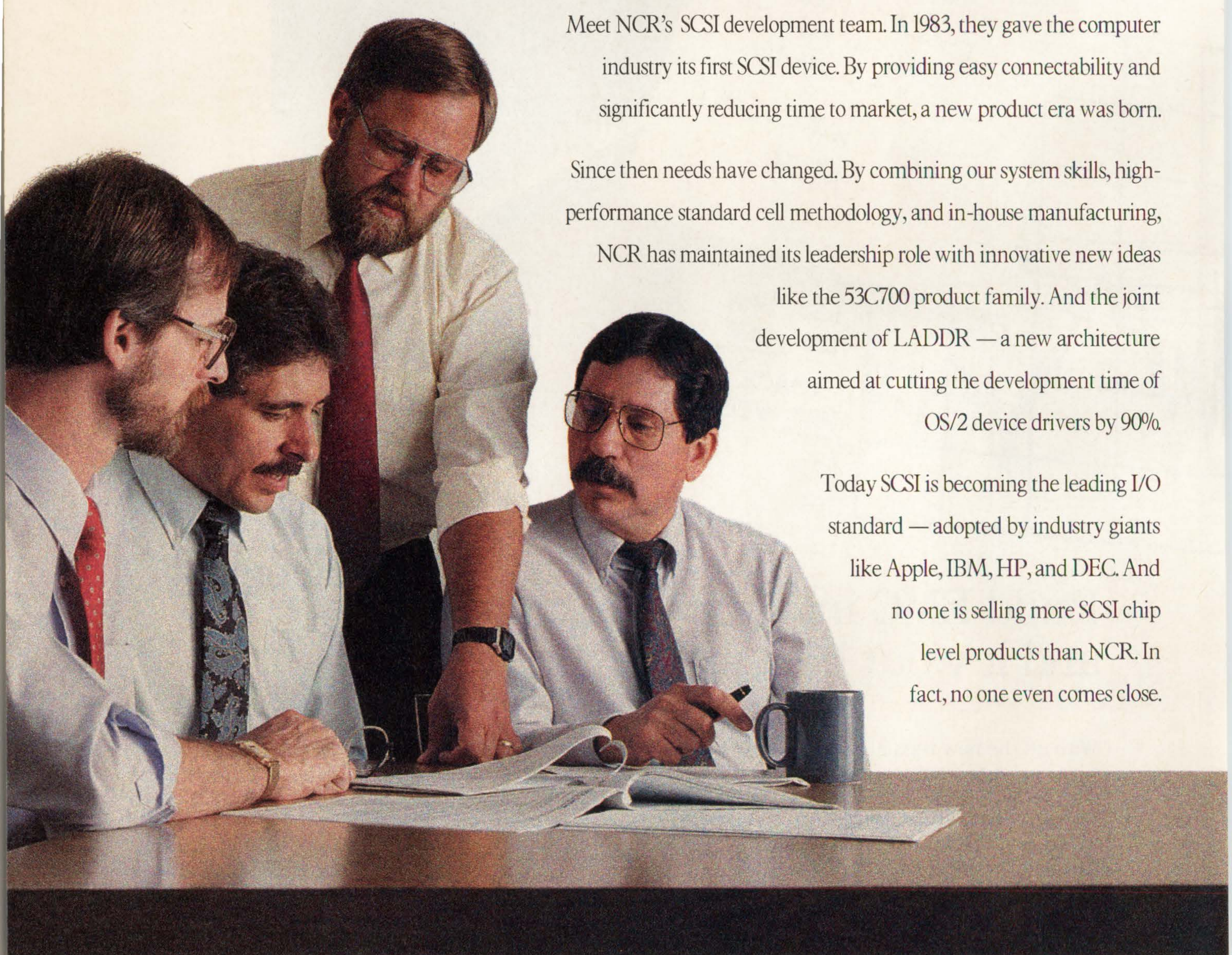

Part of the NCR SCSI Development Team: (left to right)
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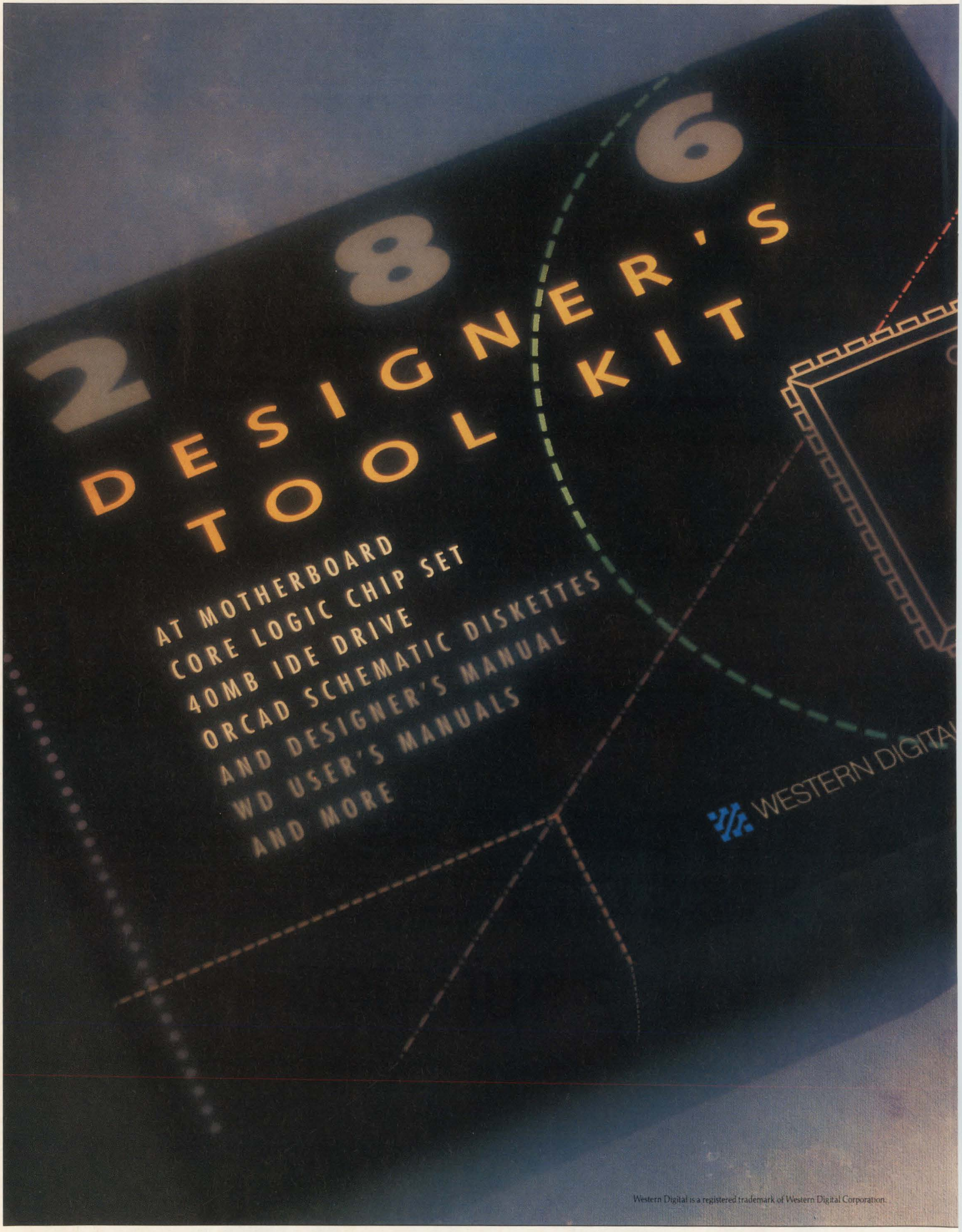

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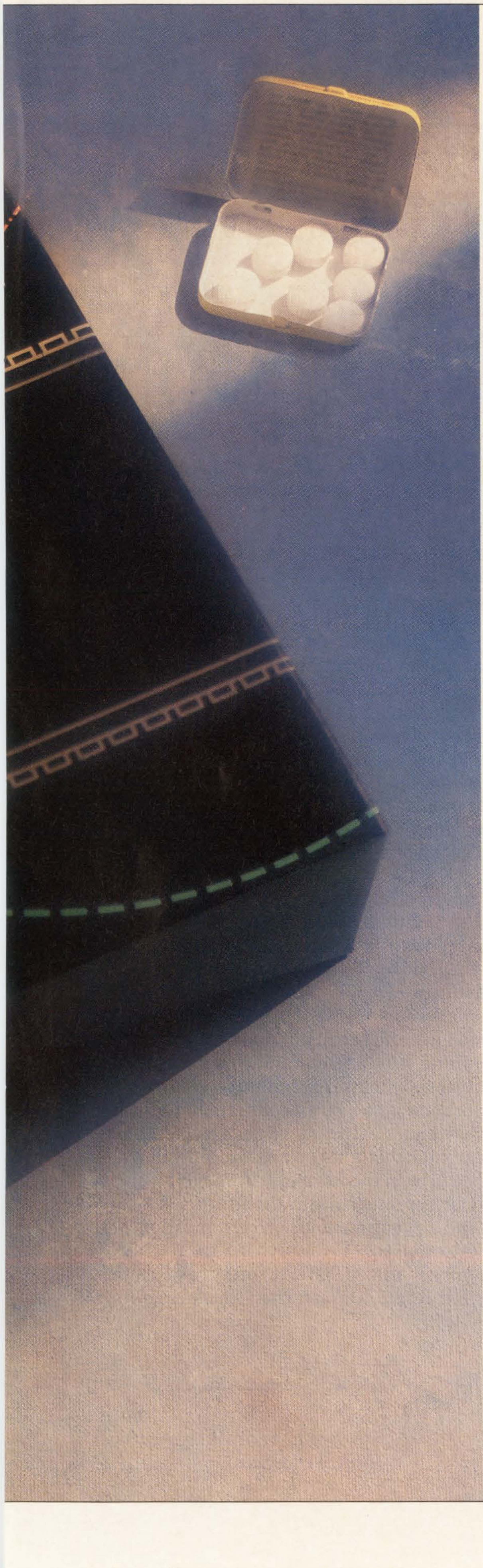

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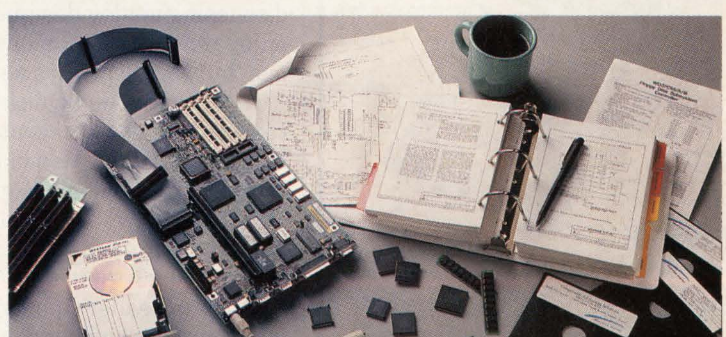

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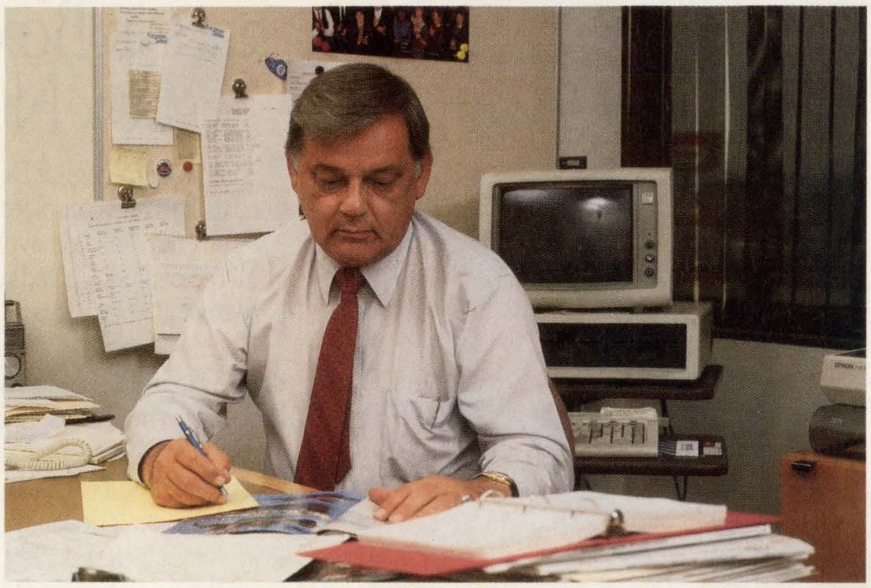
CIRCLE 152

EDITORIAL



ANALOG TAKES THE SPOTLIGHT

Designing in the analog technology world comes with its share of problems, but it also has many opportunities for innovation. In this issue, these topics are brought to the forefront. To start, there's the Special Report (page 47) by Analog Technology Editor Frank Goodenough, which covers the latest developments in fast, 12-bit sampling analog-to-digital converters. This field has blossomed in the past few years, with many new devices brought on by market demand, new semiconductor processes, and by the creativity of analog designers. Frank also penned the cover article (page 37), which introduces four new high-precision a-d converters from four different companies, all of which exploit the performance advantages of hybrid technology.

Next, we have the kickoff of a new column on analog: "Pease Porridge." This column, on page 94, is written by Bob Pease, Staff Scientist at National Semiconductor and an acknowledged expert in analog circuitry. By reading this first installment, you'll see that Bob addresses the challenges of designing analog systems in his own distinctive way. We're giving Bob a lot of freedom in this column because we believe he knows whereof he speaks when discussing analog designers' problems, and because, frankly, we think you'll enjoy reading his opinions. Sometimes they'll be outlandish and even humorous, but they'll always be insightful and thought-provoking.

In our expanded QuickLook section (page 81), we continue to publish our readers' opinions on contemporary topics affecting engineers and the electronics industry. We'd like to hear your thoughts on analog: How important do you think analog design skills will be in the future? (Our question doesn't suggest that we feel analog will be less important in the future—we simply want to hear what you think.) Send us your opinions on this question, and if possible, back them up with some examples.

Use our Reader Opinion fax number, 201-393-0637, or send your opinions to us at our editorial headquarters, 611 Route 46 West, Hasbrouck Heights, NJ 07604.

Stephen E. Scrupski

Stephen E. Scrupski
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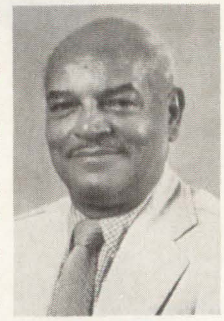
THE PROMISE OF ELECTRONIC IMAGING


MILT LEONARD
SENIOR EDITOR

When streamlining paper-intensive business transactions, electronic-imaging technology becomes appealing because it eliminates much of the manual document-handling. A recent study commissioned by the American Bankers Association concluded that image processing is highly beneficial for both transactional applications, such as check processing, and for storing business records, including correspondence and loan-processing documents. The study, conducted by Chicago-based Andersen Consulting Co., also found that reducing manual paper-based tasks and a simplified workflow translates to a three- to five-year payback period for an image-based transaction-processing system.

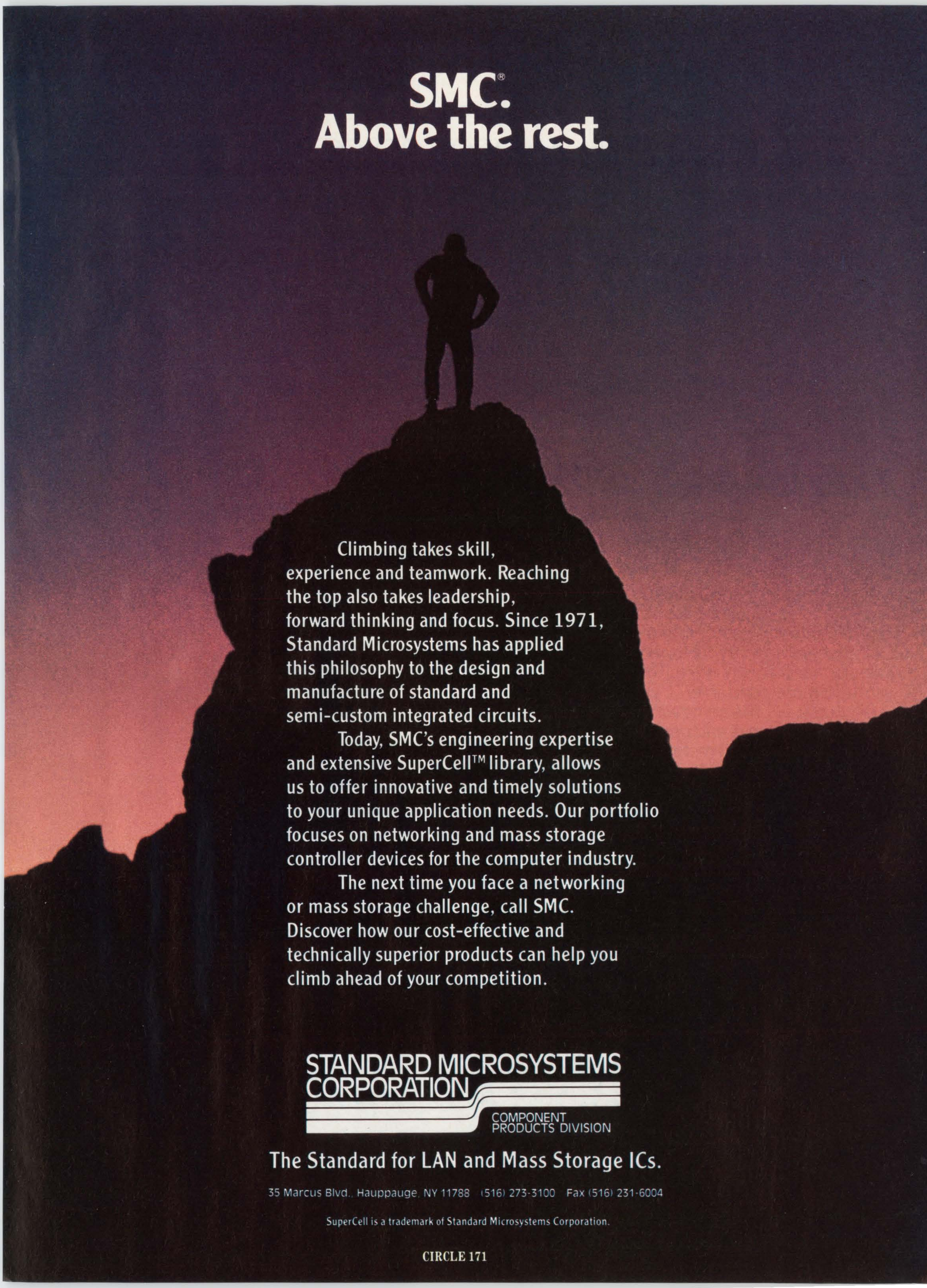
Image processing replaces paper by electronically scanning a document's text and graphics onto a magnetic or optical storage medium for subsequent access and display. According to the Association for Information and Image Management (AIIM), the biggest users are the health-care industry, government, manufacturing companies, and financial services. In each of these industries, documents must often be shared by multiple users across the organization. Ongoing advances in image-compression technology promise to benefit the engineering community as well.

Emerging image-compression chips can apply data-reduction algorithms that strip out redundant information in digitized text, engineering drawings, photos, and even moving video pictures—in black-and-white or color. This operation reduces the digital equivalent of a document by several orders of magnitude, slashing the amount of memory needed for data storage. Equally important, image compression minimizes the bandwidth required to transmit the data over ordinary telephone lines to remote sites where the document or drawing is reconstructed to its original form.

Employing this technology, new communication tools being developed will link widely dispersed design offices and manufacturing facilities for paperless sharing of information in real time. At a fraction of the cost, new silicon solutions for image processing offer the same functionality that once required multiple printed-circuit boards populated with expensive custom ICs and DSP chips. These developments will lower the cost of sophisticated communication tools, such as color facsimile machines, video telephones, and teleconferencing systems, to the point where they'll become commonplace.

Image-processing technology, however, isn't for everyone. "At this time, electronic imaging is usually not the best candidate for replacing microfilm- or microfiche-based systems with low retrieval rates when you're only trying to store information," says Sam Altiero, a partner in Andersen Consulting's office in metropolitan New York. Even when the technology appears viable for solving an organization's workflow problems, potential users may be frightened off by a number of barriers that stand in the way of a successful application.

First and foremost is high start-up cost for hardware and software. Andersen Consulting uses a three-step approach that evaluates a client's existing data-processing and document-handling infrastructure, and then examines image-processing options for meeting the client's business requirements within economic and technical constraints. Finally, the firm demonstrates the technology's viability by integrating a prototype image-processing system into the client's infrastructure. The prototype consists of imaging and data-processing software running on workstations that emulate the various hardware elements of the system. "Depending upon the business requirement, the cost of converting a document into an electronic image typically ranges between $0.05 and $0.35 per page," notes Altiero.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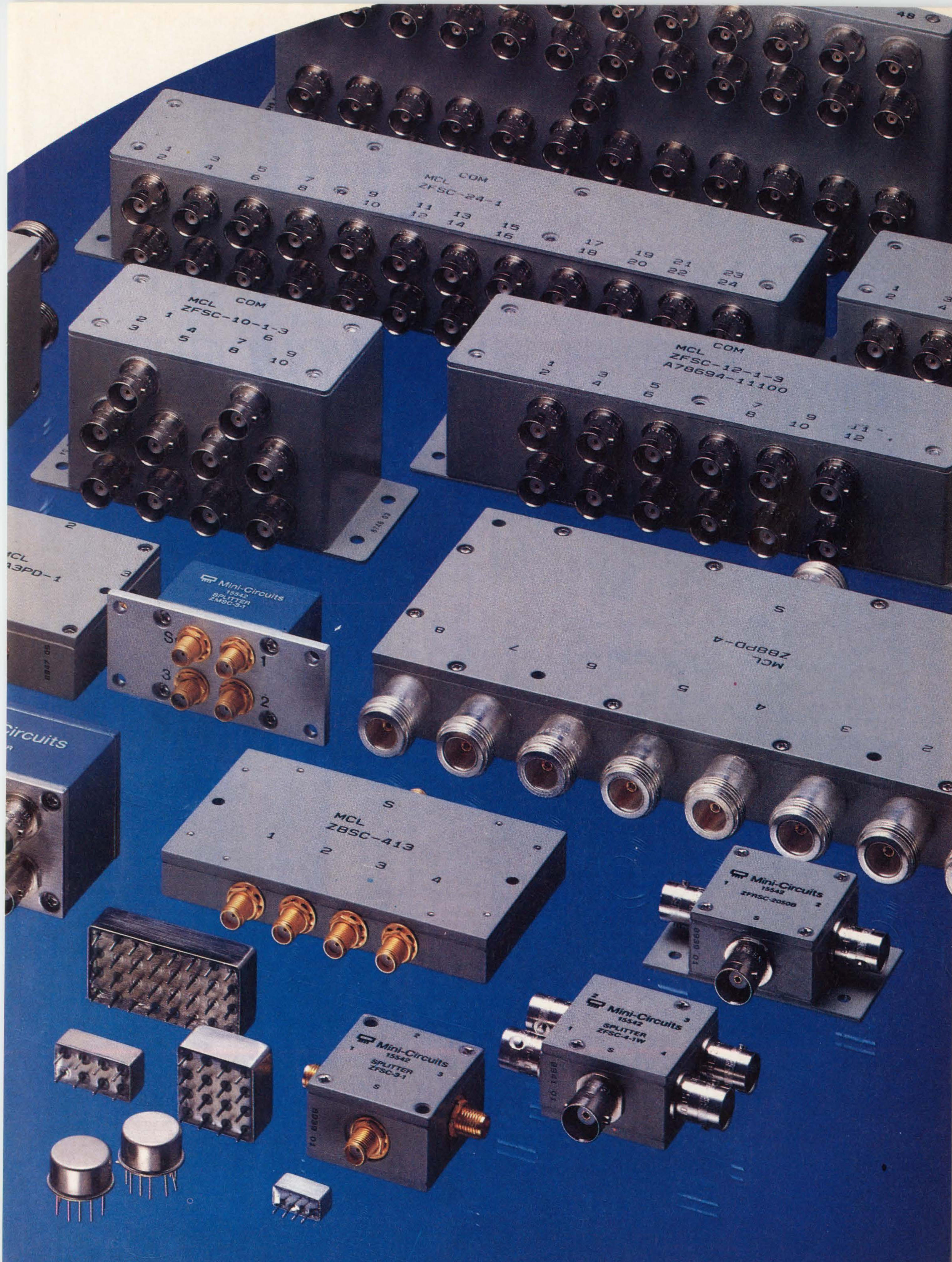
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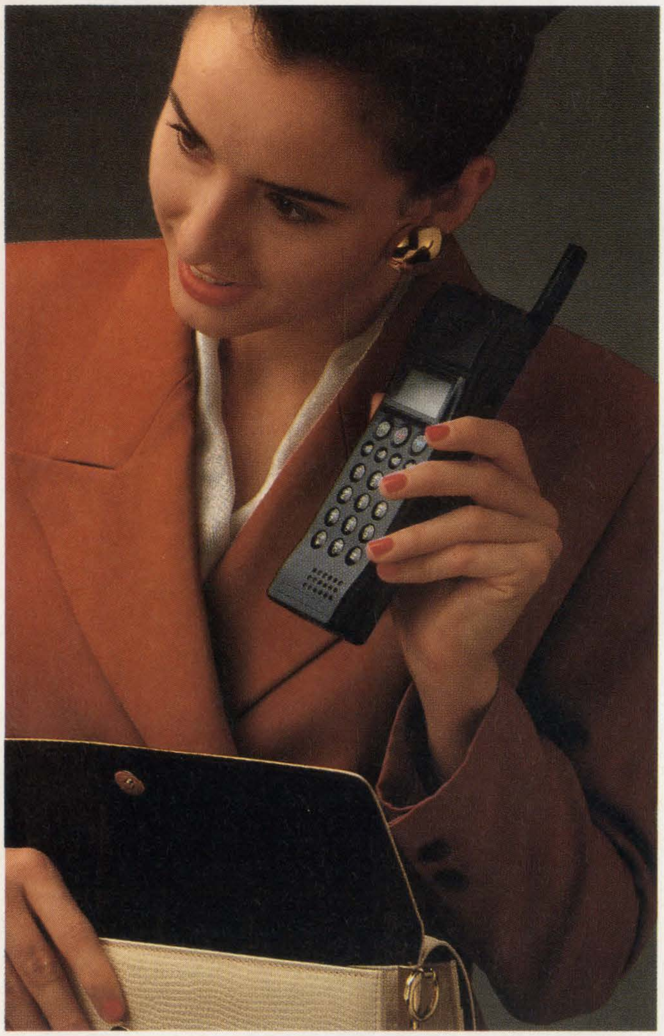

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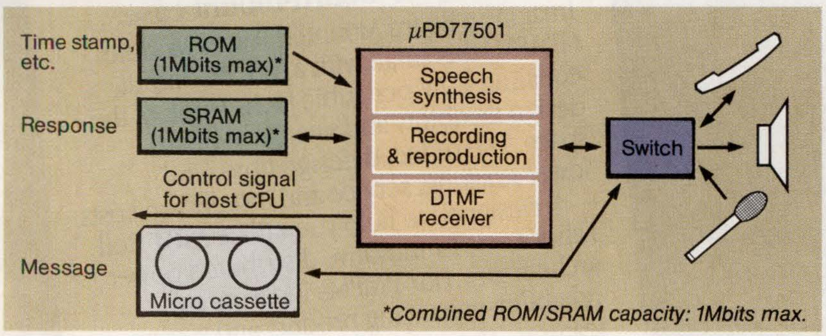

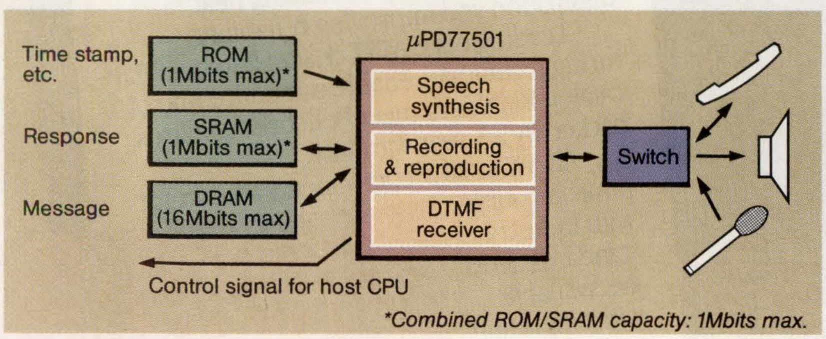

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The 77501 is the high-performance answer for solid-state systems. A competing chip lets you record 7 variable-length messages. The 77501 lets you record 64 messages of any length. That's a ninefold improvement in message capacity.

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CIRCLE 94

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CIRCLE 118

Optical System Bridges 153 km Sans Repeaters

Engineers at W. Germany's Philips Kommunikations Industrie AG (PKI) successfully sent 2.5 Gbits/s on a monomode optical fiber over a distance of 153 km, or about 95 miles, without repeaters along the line. The transmission system was tested under real operating conditions. The Nuremberg-based company, an affiliate of Philips N.V. of the Netherlands, thus established a new record. Until now, the greatest repeater-less distance for an optical transmission system was around 100 km, or roughly 62 miles. Most responsible for the feat is a new laser developed at the Philips Research Laboratories in Eindhoven, the Netherlands. Putting out 2 mW of power, the laser operates in the third optical window at 1550 nm. The 2.5-Gbit/s rate corresponds to 30,720 digital speech channels of 64 kbits/s each. The optical components that PKI is testing, including transmitters and receivers, are part of a synchronous multiplexing and line-transmission system slated for trials by Australia's communications authorities. JG

AMP, Siemens Agree On DIN Standards

In accordance with the International Electrotechnical Commission's (IEC) decision, metric designs will soon supplant the traditional inch-based technology for connectors. Modular Order 917 and the applicable DIN standards are the groundwork for this changeover. As a result, Siemens AG, Munich, Germany, is working with AMP Inc., Harrisburg, Pa., to develop a new generation of connectors that mix both 2- and 2.5-mm standard sizes. The first prototypes will be shown at November's Electronica show in Munich. In the future, connector users will be able to choose between the two system-compatible sizes, or mix the grid sizes in uniformly standardized metric equipment. DM

Vendors Join To Fight Software Bottleneck

A CAE company and silicon manufacturer are collaborating to battle software development, which is often a critical bottleneck in embedded-processor designs. Mentor Graphics Corp., Beaverton, Ore., and Intel Corp., Chandler, Ariz., will work together toward a full-system-simulation environment that includes simulating software running on the target hardware. The relationship will link Mentor's hardware-design and CASE tools with Intel's 80C186 embedded-processor core to develop standard or custom parts. Intel will contribute its library of fully functional VHDL models for the 80C186 core and its peripherals. To create code for their chip, engineers use Mentor's CodeLink Station software debug and test tool suite. Mentor's Express I/O tool will then model the target hardware and build test fixtures for quick software verification. With this environment, the actual software acts as the stimulus for the hardware simulation. Call Mentor at (503) 645-1551. LG

GaAs Diodes Cutoff At 2.5 THz

A family of GaAs Schottky diodes with a cutoff frequency of 2.5 terahertz (THz), or 2.5 million MHz, was developed by Telefunken Electronic GmbH, Germany. This high frequency suits the diodes for use in mixers operating at up to 100 GHz. Low input capacitances (typically between 6 and 34 fF) and small series resistances (from 3 to 13 Ω) create the high cutoff frequency. To produce the submicron structures needed on the GaAs wafer, Heilbronn-based Telefunken uses direct-write electron-beam lithography. So far, the firm has developed six different single and five double diodes in an antiparallel circuit configuration. The diodes will come as chips that can be soldered into the circuit, or contacted with a conductive paste for low series inductance. The development follows the company's work on GaAs mixers in superhigh-frequency (SHF) and extremely-high-frequency (EHF) receiver circuits operating at 35 GHz. JG

Mosaic And Cypress Share Mil Packaging

Designers of rugged industrial and military digital systems now have more options for squeezing very dense memories into tight spots. A licensing agreement between Mosaic Semiconductor, San Diego, Calif., and Cypress Semiconductor, San Jose, Calif., enables both companies to use Mosaic's proprietary vertical-in-line (VIL) packages. Under the agreement, Cypress' Multichip Technology subsidiary will produce high-density memory products using Mosaic's rugged, space-saving package. Multichip currently offers static-RAM (SRAM) modules in capacities up to 4 Mbits in various DIP, SIP, and ZIP packages. Mosaic now offers VIL-packaged 256-kbit and 1-Mbit SRAMs, 1- and 4-Mbit dynamic RAMs, and 256-kbit-by-4 video RAMs. DM

HIGH-PERFORMANCE CPUS APPEAR AT HOT CHIPS

At the second "Hot Chips" Symposium recently held at Santa Clara University, designers saw the future architectural direction of some popular CPUs, as well as math and image processor chips. Intel Corp., Santa Clara, Calif., for instance, divulged details of three processors—its next high-performance member of the 960 family, a long-instruction-word processor that's part of its iWarp project, and a two-chip set for digital-video interactive systems.

The forthcoming 960xx family member will include dual 2-kbyte caches (one for data, one for instructions) as well as a 64-entry translation-lookaside buffer and an on-chip MMU. High-speed math operations are possible thanks to 3-clock floating-point multiplication, addition, or subtraction, and 14-clock division. The CPU will have two buses—a 64-bit-wide memory bus that runs at 50 MHz, and a 32-bit I/O bus that runs at 25 MHz, giving the chip an aggregate I/O capability of 264 Mbytes/s. Intel's iWarp processor employs a 96-bit instruction word. It can simultaneously perform single-precision floating-point calculations at 20 MFLOPS, while running 20 MIPS in its integer processor and performing as many as three 20-Mword/s transfers. The processor was designed for a systolic environment and has four bidirectional communication ports for nearest-neighbor interconnections.

For digital-video subsystems, Intel reviewed its i750 chip set for digital video interface (DVI), the 82750DA display processor, and the 82750PA pixel processor. The chip set can create full-screen 30-frame/s motion video, perform real-time image capture and compression, display high-resolution still images, and perform graphics and animation. Furthermore, the company released details of its "B" level upgrade, which runs at twice the clock speed of the DA and PA and offers double the on-chip memory and I/O bandwidth. Moreover, the DB upgrade packs the triple color-palette memory and video digital-to-analog converters.

Working in GaAs technology to implement a Sun Sparc-compatible multichip module, designers at Systems and Processes Engineering Corp., Austin, Texas, described their attempt to build a Sparc CPU module with cache that runs at 200 MHz and delivers a peak throughput of 200 MIPS. The chip set will consist of an integer unit, a floating-point coprocessor, twin cache-and-memory-management units, and dual 16-kbyte caches. Expecting CMOS to deliver about the same throughput as GaAs, Metaflow Technologies Inc., San Diego, Calif., is working with LSI Logic Inc., Milpitas, Calif., and Hyundai Electronics, Seoul, Korea, to create a superscalar version of the Sparc. The performance target is 100 MIPS (average) for a chip set running at 50 MHz, with a peak speed of 200 MIPS. The superscalar approach issues four instructions per clock (up to three integer or floating-point instructions and one branch). Therefore, four of the six functional units can be kept busy. The chips will also permit dataflow-based out-of-order instruction execution with in-order completion, as well as speculative execution beyond unresolved branch instructions.

The forthcoming C4 chip set from Intergraph Inc.'s Advanced Products Div., Palo Alto, Calif., combines superscalar and superpipelined architectural approaches. Although code-compatible with its previous Clipper family chip sets, the C4 chip set splits the floating-point unit off as one of the two chips; previous families included that functionality on the CPU. Most instructions execute in one clock cycle. Because multiple instructions (floating-point and integer, for example) can be issued simultaneously, the processor will have an efficient clocks-per-instruction ratio of less than 1. When running at 50 MHz, the C4 can achieve a throughput of 21 to 33 MFLOPS (scalar or vector, respectively) with an integer throughput of about 50 MIPS.

For high-speed floating-point computations, Weitek Corp., Sunnyvale, Calif., unveiled a 120-MFLOPS (double-precision) CMOS floating-point processor. It's expected to be released in 1991. To achieve that performance level in CMOS, the company's designers will incorporate a large (32-word-by-64 bit, or 64-by-32) 8-port register file on the chip and a unique dual adder section in the ALU that reduces computation time by close to 50%. The multiplier section has a 2-cycle latency, but can deliver a 32- or 64-bit floating-point or integer result every cycle.

LSI Logic Corp. has focused on image processors for such applications as video compression, image compression, video telephones, and others. As a result of this effort, the company described a multichip set that puts the toughest parts of the algorithms onto four chips. The chips perform motion estimation, discrete cosine transform processing, quantization, and BCH encoding and decoding. To interconnect processors in an array, researchers from The California Institute of Technology, Pasadena, described a mesh-routing chip that has five input and five output channels, with each channel providing 11 signal lines. The chip was originally designed as part of the Defense Advanced Research Projects Agency (Darpa)-sponsored Touchstone project, for which Intel applied its iWarp processor. DB

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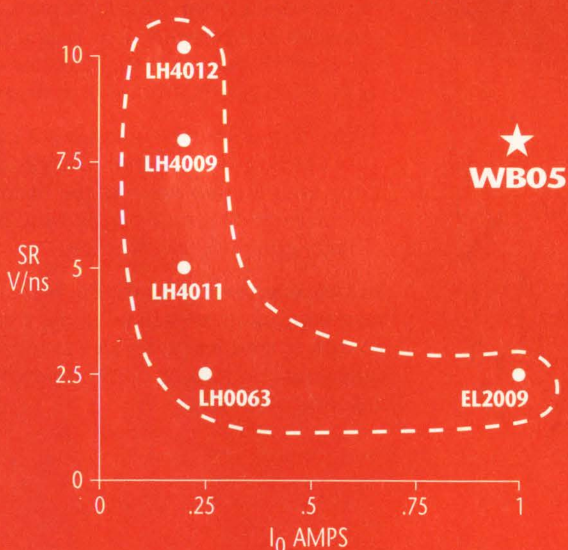

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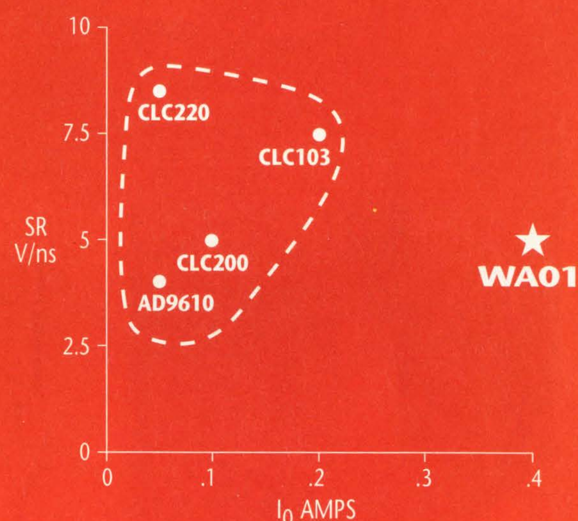

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CIRCLE 166

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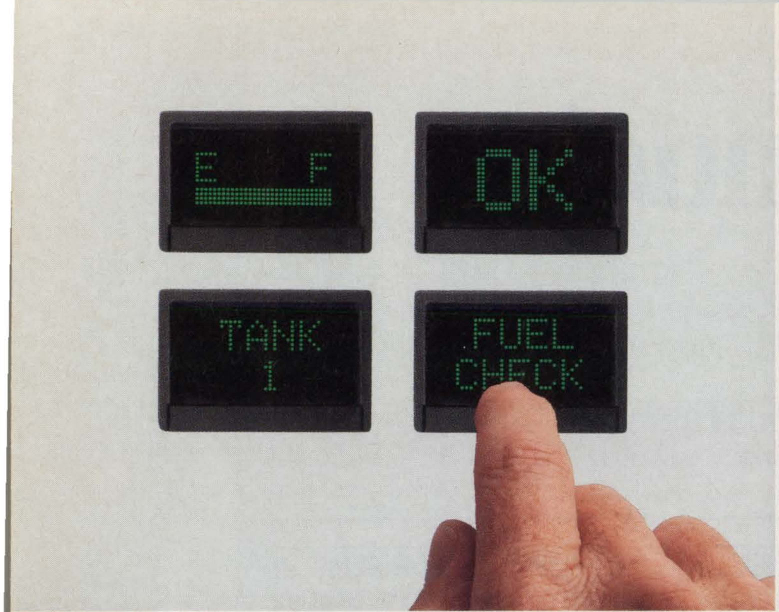

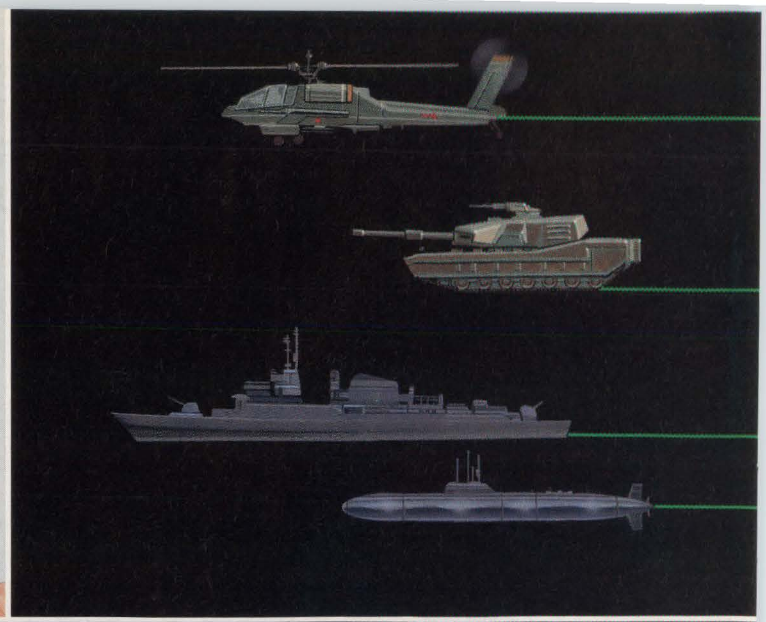

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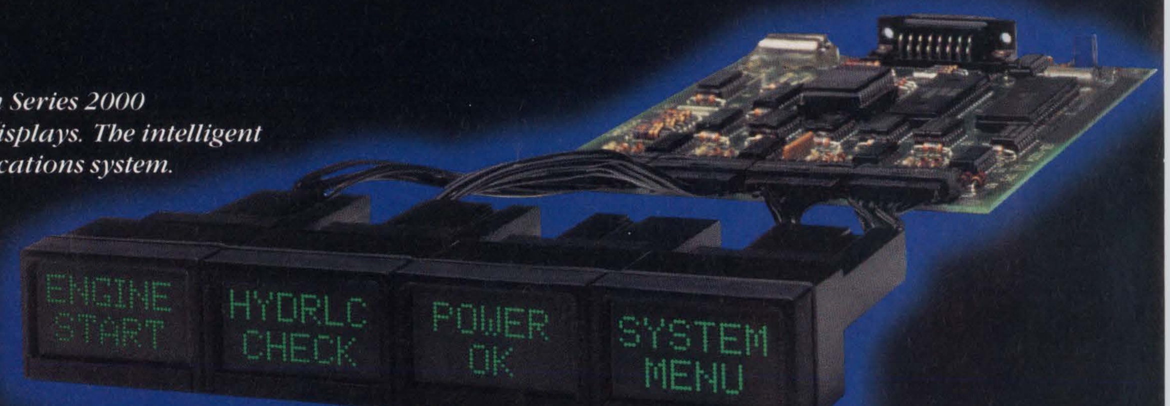


SERIES
VIVISUN 2000™

ROTATING DISK PRODUCES REAL 3D IMAGES

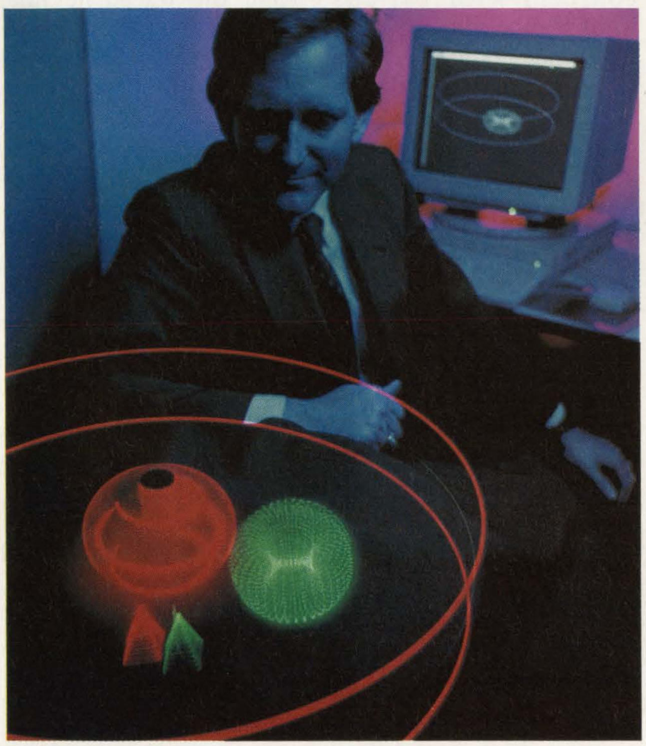
A unique prototype laser-display system can create true spatial 3D images viewable from any angle. According to Texas Instruments, Dallas, the new display technology overcomes many limitations inherent in other 3D display approaches, such as holographic, stereo-pair, and mirror-based multiplanar displays.

Unlike other techniques, the TI OmniView system presents a real, rather than a virtual, image within a dome-shaped display volume. As a result, the visual perspective of the displayed image changes with the viewing angle, just as it would with an actual object. Any number of individuals can watch the display simultaneously without special glasses, masks, or other viewing aids. The display can be viewed from any angle—even if walking around it in a 360-degree circle. The projected object remains stationary during movement of the viewer.

The 3D images are produced with a clear rotating plastic disk. The disk is set at an angle atop a motor shaft and rotated to create a display volume inside the dome-shaped bubble. In operation, the image appears as a double helix, occupying height, width, and depth. The size and shape of the disk can be varied to provide the best display volume for a specific application, ranging from tall and narrow to short and wide.

In TI's prototype system, which displays images created and stored on a Sun workstation, an extremely low-power laser modulated 10,000 times per second shines points of light on the display disk rotating at 600 rpm. The beam scans the disk in two dimensions; synchronization of the laser and the spinning disk create the image in the third dimension. The viewer's eyes fuse the discrete points of light painted on the disk into a 3D volume.

The current laser-scanning system design has a resolution of approximately 750-by-750 picture elements or pixels; multiple scanning systems can be used to increase resolution or support extremely large displays. Red, green, and blue lasers can be mixed to produce a full-color display



According to the company, the OmniView display technology particularly suits applications in which real 3D objects must be viewed in a volume. One application in this category is air traffic control. Such a system could show several controllers the positions of aircraft relative to one another, and ground-based reference points, such as airports, mountains, and tall buildings. Color coding could identify protected airspace and provide an index relating to different altitude levels.

Other potential applications cited by the company involve the modeling of real-world objects. Such examples include medical imaging, molecular modeling, weather-pattern analysis, and remote positioning and control of objects.

Texas Instruments is seeking partners to develop applications for the system. It will also grant licenses to those companies interested in producing the display for selected markets.

JON CAMPBELL

RISC TECHNIQUES PRODUCE SINGLE-CHIP TELEPHONE IC

Incorporating a bit-oriented reduced instruction set (Boris) and an on-chip read-only memory, a microcontroller chip contains all of the active circuitry needed to make a mid-range, single-chip telephone configurable to most countries' standards. Developed at Mietec Alcatel, Brussels, Belgium, the controller uses what communications product manager Ron Spooner calls a "data-movement engine," under the control of a ROM-based sequencer, to control all keypad operations, produce dialing tones or pulses, and perform hookflash and repertory dialing. "Its architecture has a specially developed counter structure for addressing ROM," says Spooner. "This allows program jumps and loops to be implemented without using wide-ROM or multiple-word instructions as normally used in controllers of this type."

It has just 22 instructions in its vocabulary—all of which can be conditionally executed—as defined by internal and external flag bits. Similar to most telecommunications applications, timing is critical, even to operate a "simple" telephone. "The application requires the generation of accurately timed events, such as hookflash, pulse dialing, and so on," Spooner notes. "The exact timing can vary depending on specifications set by the local telephone authority."

In Europe, for example, there are nearly 20 national PTTs (government-operated postal, telephone, and telegraph networks) each with its own slight variations on the specifications that a telephone must meet in order to be approved for connection to the public switched telephone network. These variations are handled with a selectable clock as well as a hardware loop-counter structure, while the mask-programmable ROM gives flexibility in setting and controlling options and operation sequences.

The chip—the MTC-20294 micro-MIP (maximum-integration phone)—was originally designed to meet the requirements of the French Centre National des Etudes pour Telecommunications (CNET), but Spooner says that it can be adapted easily to meet the specifications required by most PTTs and telephone administrations. It will sell for $2.50 in high quantities. Initially, standard parts will be made for use in France, but Spooner says that versions for the United Kingdom, Italian, and Spanish markets will be launched before the year's end. Meanwhile, Mietec is preparing to customize the device for potential North American and other international telephone makers.

The device has three 24-digit repertory memories, each of which can be activated by one keystroke. Dialing from memory and manual dialing can be connected in any order, provided that the maximum capacity of 24 digits isn't exceeded. Operating a last-number redial function follows a "sliding cursor" algorithm, which is intended to speed automatic dialing when intermediate pauses for PBX access or international dialing are required. Other features include on-hook dialing, and speech and tone processing.

The chip can be set up to conform with various hookflash, dialing, and pulse-period parameters through a matrix of diodes associated with a 20-key dial pad. Available options include dual-tone multifrequency (DTMF) or pulse dialing, regulated or unregulated speech gain, regulated or unregulated DTMF gain, 0 ms or 270 ms hookflash time, and a pulse mark-space ratio of either 3:2 or 2:1.

The chip requires between 3 V and 7 V, derived from the telephone line, and consumes about 60 mA in the active mode. However, when the phone is on-hook, all circuits except the repertory and last number redial memories are disconnected. In that condition, the chip draws about 2 μA from the line. A crystal or ceramic resonator oscillator provides a frequency reference for generating DTMF tones and loop-disconnect dialing pulses. More information is available from Mietec Alcatel, Raketstraat 62, B-1130 Brussels, Belgium. Telephone +32 (0)2 242 75 52.

PETER FLETCHER

IMPROVED ROUTING BOOSTS FPGA GATE COUNT

With increases in on-chip routing resources and antifuse programming elements, along with an improved logic cell, a field-programmable gate array can acheive the equivalent logic capability of an 8000-gate mask-programmable array. The array is part of Actel Corp.'s, Sunnyvale, Calif., second-generation of FPGAs that employ a 1.2-μm CMOS process, which leaves plenty of room for future scaling.

To get better routability with the higher gate counts, the Act-2 family employs many more programmable antifuses than in the Act-1 family—750,000 are on the 8000-gate chip. As many as 36 horizontal routing tracks are positioned between the rows of logic cells, and up to 15 vertical tracks are provided for every column on the chip. As part of the routing resources, unbroken long-line segments can be used for global (cross-chip) routing. Short segments are available for localized routing.

The logic cell module was also redesigned: Rather than one module type, Actel incorporated two module types on the chip. One module type was optimized for sequential operations, while the other was optimized for combinatorial functions. The combinatorial modules permit 13% more 4-input macros, or 12% more 5-input macros, than the cells in the Act-1 family. A combinatorial block has four data inputs, two control inputs, and one output. A sequential block includes a configurable flip-flop optimized to form high-speed flip-flops and latches.

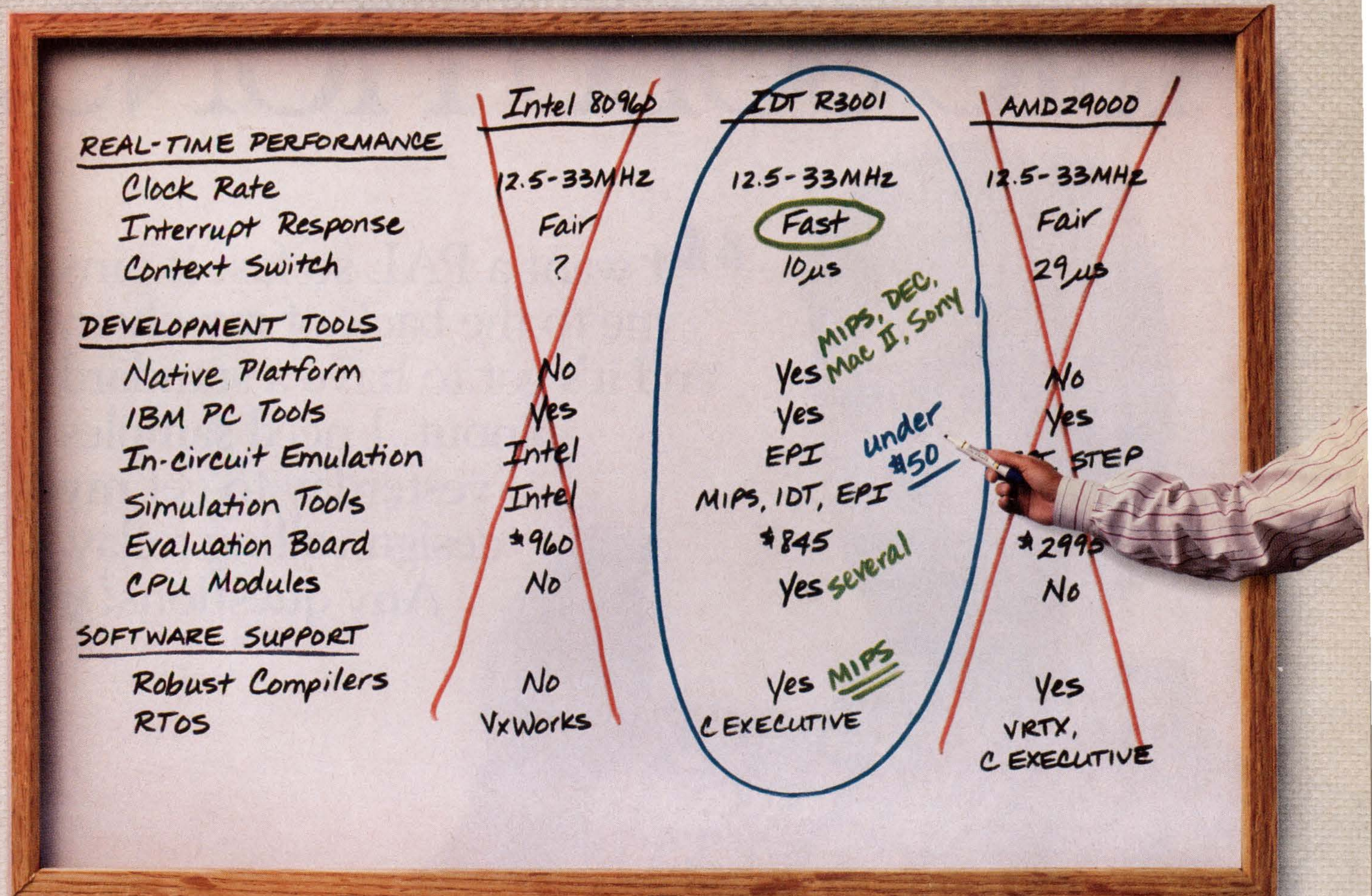
Software makes it possible for users to specify critical speed paths in the circuitry. Those paths are then routed with a maximum of only two low-resistance antifuses (less than 200 Ω each vs. about 500 Ω apiece in the previous family) in the signal path. The result is predictable performance even with fully automatic placement and routing. Moreover, gate utilization can reach close to 80% with a logic-cell utilization of about 95%. Furthermore, although the largest of the Act-2 family chips will offer about four times the gate count and twice the number of I/O lines (140) of the largest Act-1 family chip, it will operate at twice the speed.

Operating at system clock speeds of between 50 and 60 MHz, the Act-2 arrays can tackle many newer system applications that run with clock speeds of over 50 MHz. The A1280 is currently the largest Act-2 family member, packing about 8000 gates (equivalent to about 20,000 gates if PLD gate-counting rules are used). Two smaller family members, the A1240 and A1225, with 4000 and 2500 gates, and 104 and 82 I/O lines, respectively, are to be released the first half of 1991.

Improved software tools also play a significant role in achieving the high utilization, higher performance, and ease of circuit development. The enhanced software developed by Actel added about 50% to the circuit library, increasing the number of macrocells to about 250. For details, call Andy Haines, (408) 739-1010.

DAVE BURSKY

Embedded RISC

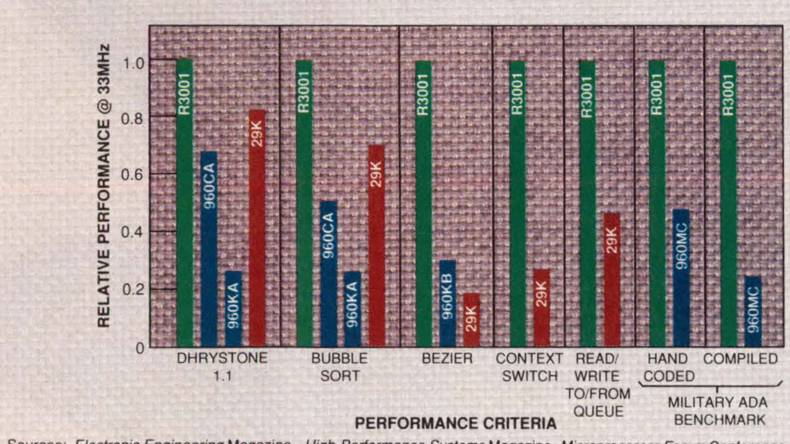


Get the Facts

When evaluating RISC processors for embedded applications, you need real benchmark data from independent sources. The *R3001 Performance Comparison Report* is a collection of the original third-party data used in the graph below.

Benchmark Your Code

Of course, we know that published data can't give you all the information. You'd prefer to perform benchmarks for your specific application, and our six technology centers are equipped to do just that — bring us your code and we'll run your benchmarks!



Sources: *Electronic Engineering* Magazine, *High-Performance Systems* Magazine, *Microprocessor Forum* Conference Fall 1989, *Independent Assessment Benchmark Report* Atlantic Research Corporation

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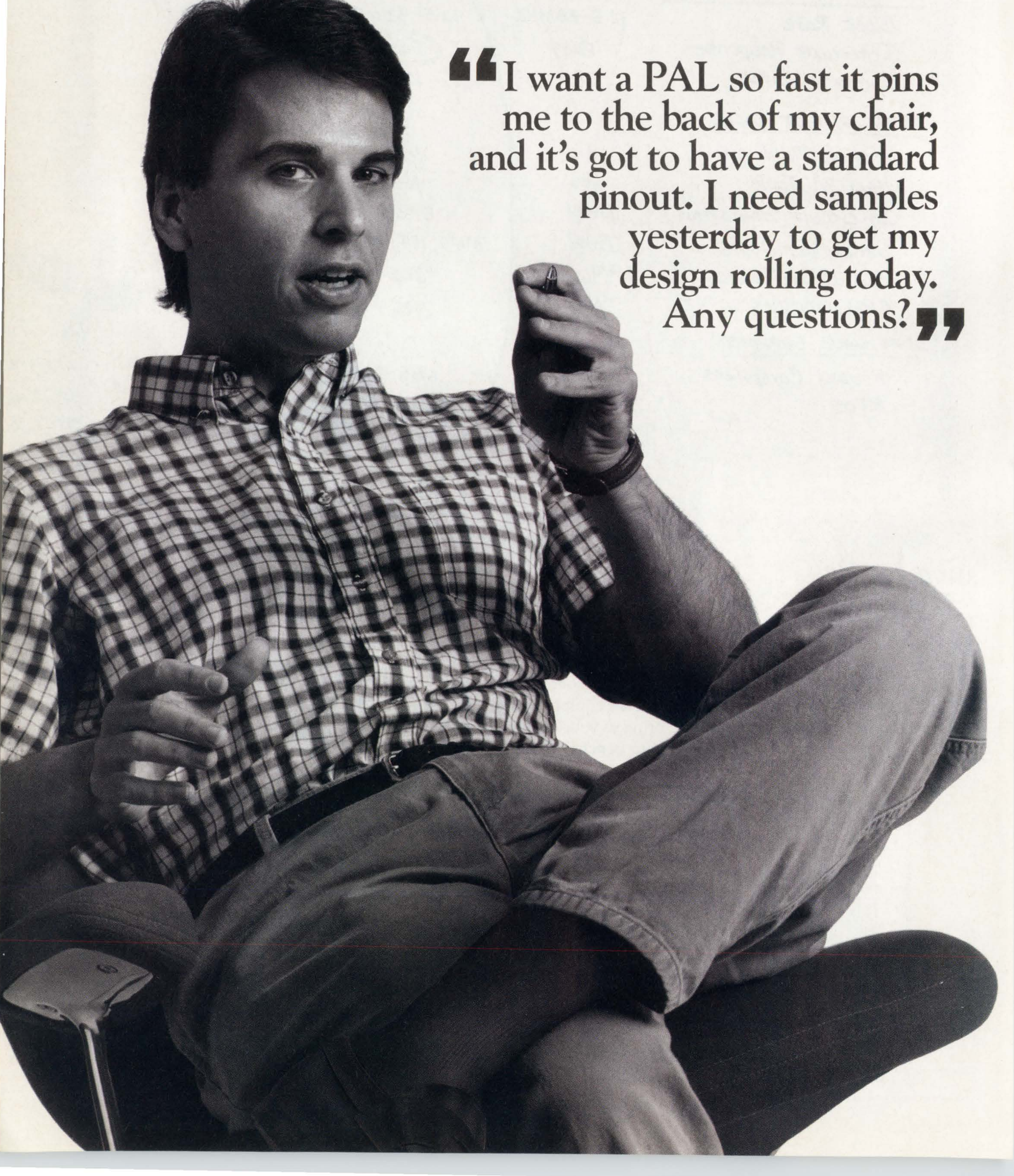

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TIBPAL16R4-XX	TIBPAL20R4-XX

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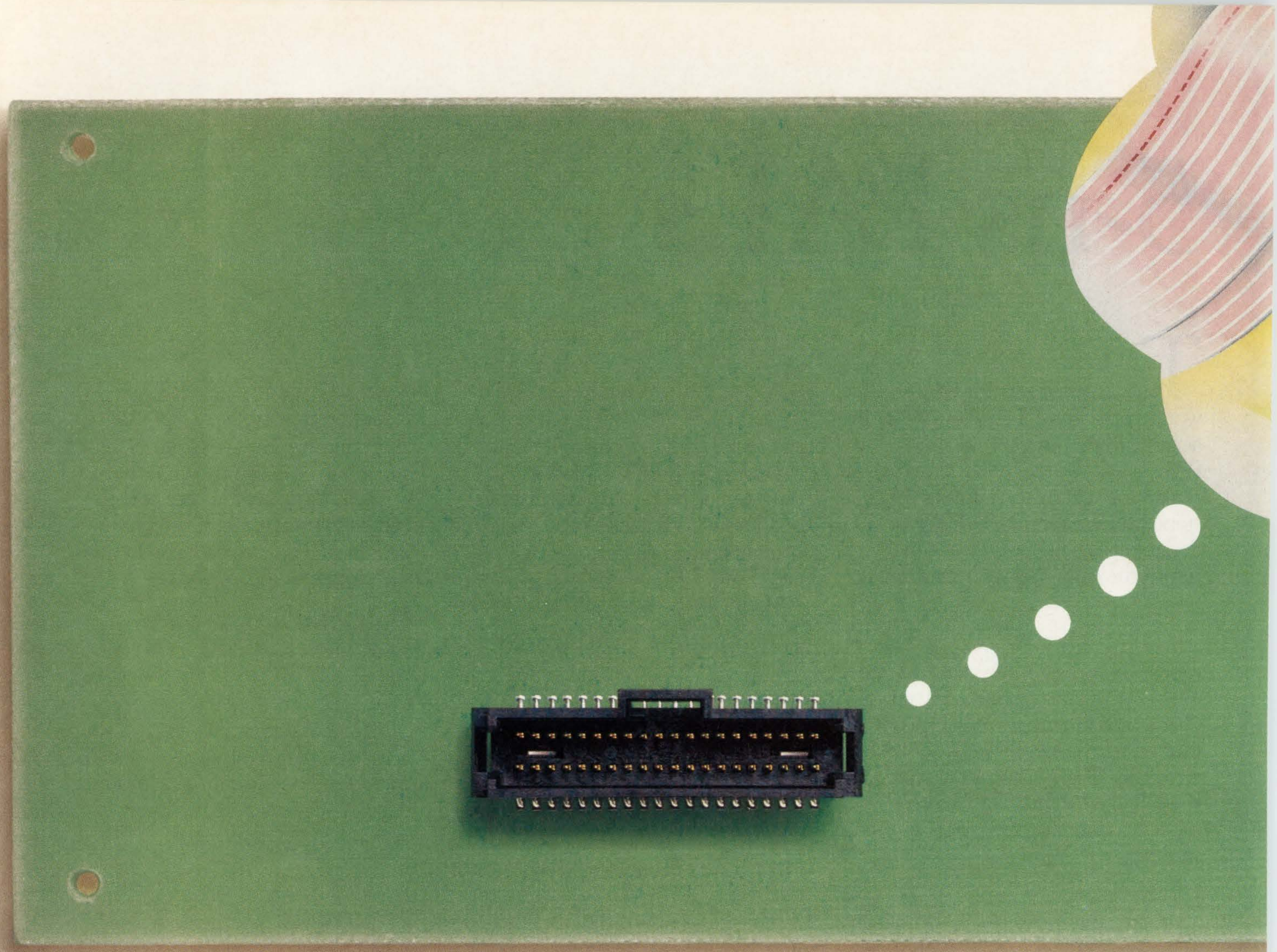
TEXAS INSTRUMENTS



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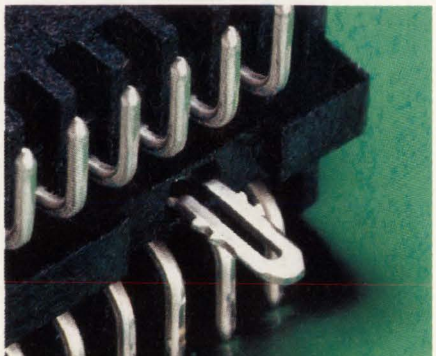

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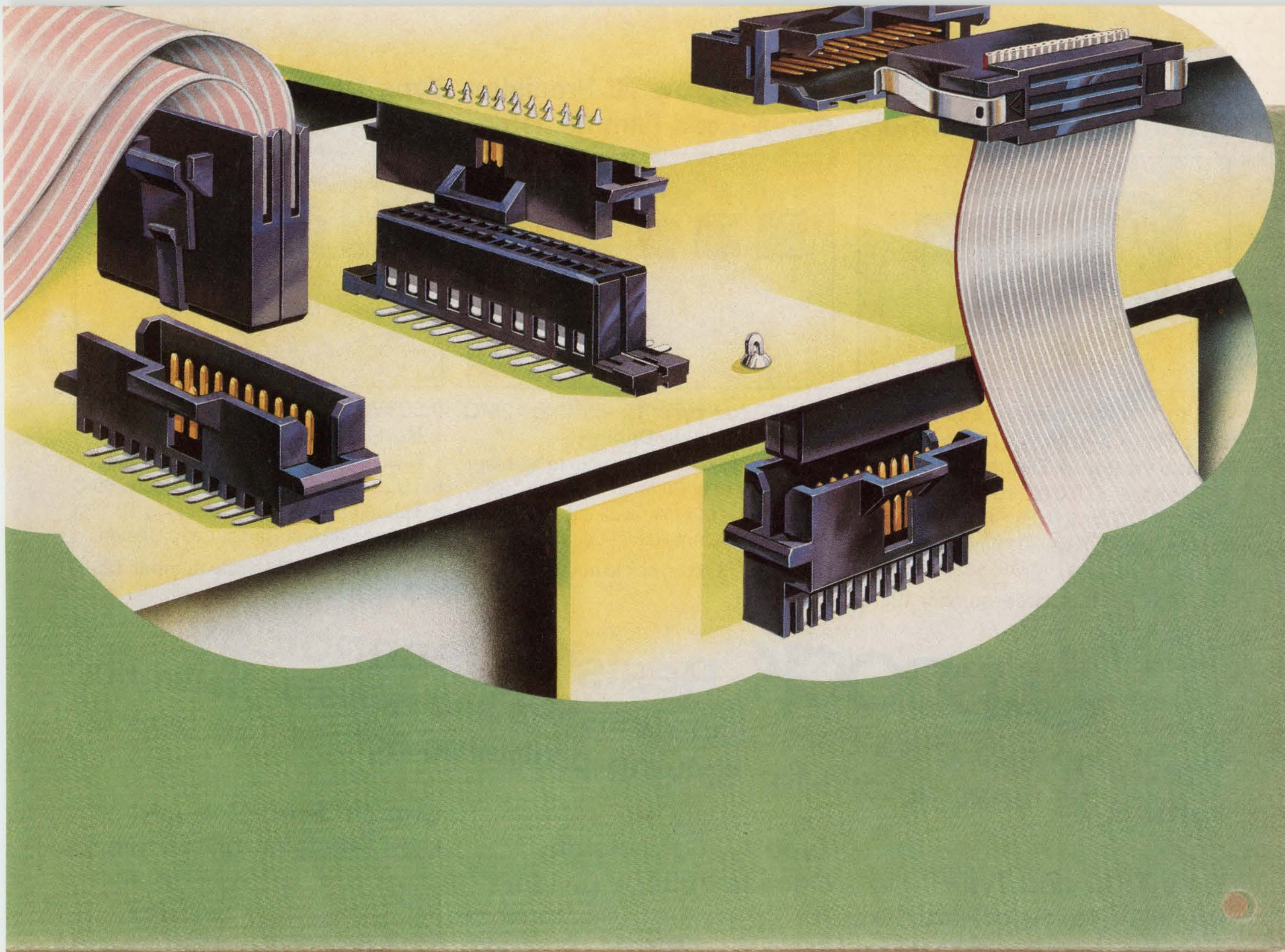

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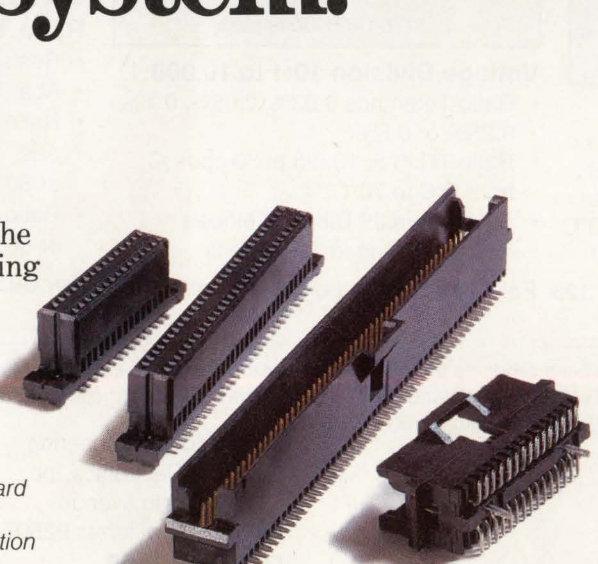

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CIRCLE 149

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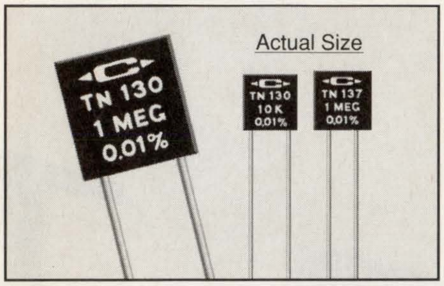

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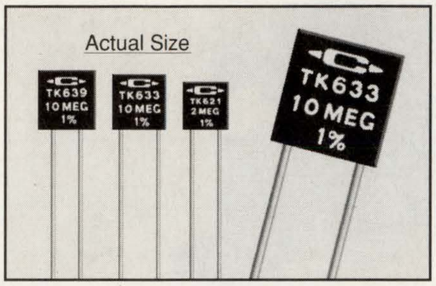
- Space Efficient Radial-Lead Design

For Type TN data, circle number 123

Type TK Low TC Precision Radial-Lead Film Resistors



Low TC to 5 ppm/°C, -55°C to 125°C

- **Non-Inductive Design**
- Resistance Range 1 Kohm to 10 Meg
- TC of 5, 10 or 20 ppm/°C, -55 to 125°C
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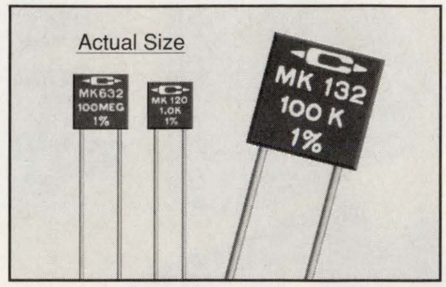
- Space Efficient Radial-Lead Design

For Type TK data, circle number 124

Type MK Precision Power Radial-Lead Film Resistors



0.50 Watt (CK05), 0.75 Watt (CK06)

- **Non-Inductive Design**
- Resistance Range 1 Ω to 100 Meg
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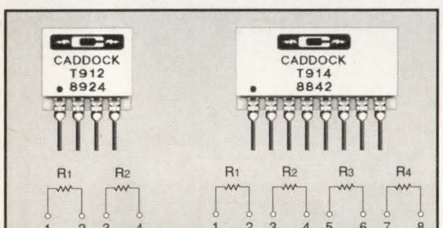

T912 Schematic 1:1, 9:1 or 10:1

T914 Schematic 4 equal value resistors

Ultra Precise Ratios to 0.01%

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For Type T912/T914 data, circle number 126

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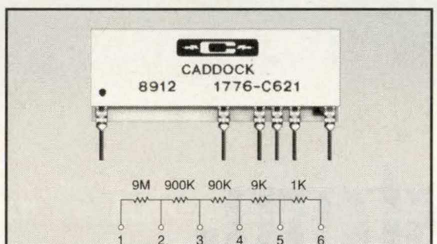

1776-C621 Schematic

Voltage Division 10:1 to 10,000:1

- Ratio Tolerance 0.02%, 0.05%, 0.1%, 0.25% or 0.5%
- Ratio TC of 5, 10, 25 or 50 ppm/°C, from 0°C to 70°C
- Select from 39 Different Models
- Voltage Rating to 1,200 Volts

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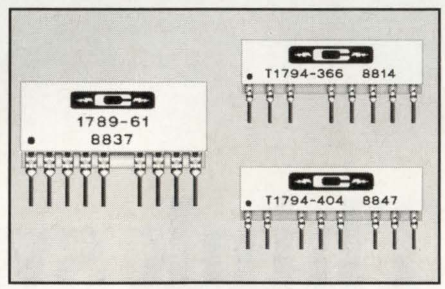

Ratio Tolerance to 0.01%

- Resistance Range 0.5 ohm to 50 Meg
- Abs. Tolerance from ±0.025% to ±1%
- Ratio Tolerance from 0.01% to 1%
- Abs. TC of 15 ppm, 25 ppm, 50 ppm or 80 ppm/°C, from 0°C to 70°C
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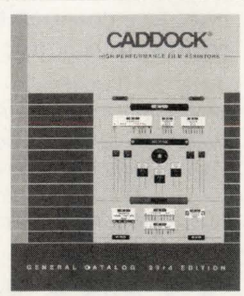
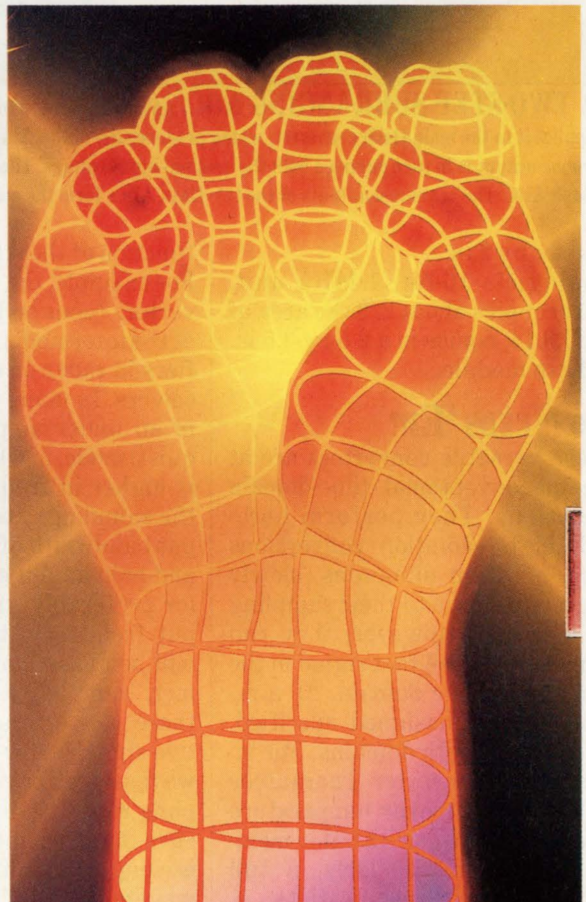


12-TO-16-BIT ADCS SAMPLE AND QUANTIZE 16 BITS AT 0.5 OR 1 MHZ, 14 BITS AT 10 MHZ, AND 12 BITS AT 20 MHZ.

FOUR HYBRID ADCS HIT NEW PERFORMANCE HIGHS

FRANK GOODENOUGH



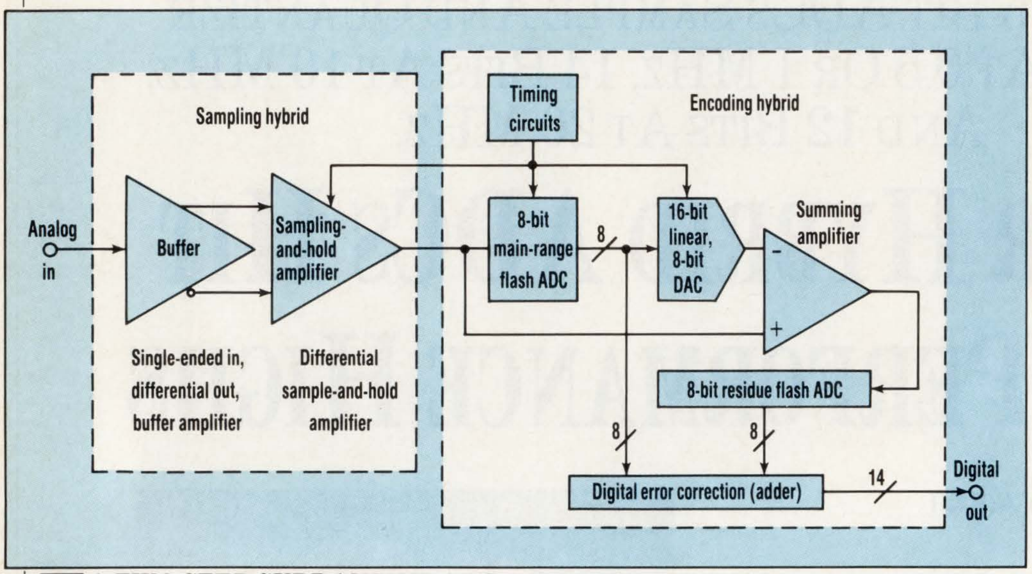
It wasn't that long ago that 12-bit, 10-MHz ADCs, as well as true 16-bit sampling ADCs, would fully occupy 5-by-7-in. pc boards. However, four new analog-to-digital converters demonstrate the rapid advances made in today's hybrid and semiconductor technologies. Two of the converters, the ADS-930 from Datel and the ADC4344 from Analogic, bring 500-kHz and 1-MHz sampling rates, respectively, to the 16-bit arena. A third, the AD9014 from Analog Devices, provides 14-bit samples at 10 MHz, while a fourth, the CLC936 from Comlinear, delivers 12-bit samples at 20 MHz.

All of these ADCs have several important characteristics in common: They are sampling-type converters incorporating proprietary circuit techniques and/or custom ICs; they employ some form of hybrid packaging technology; and their performance is based on two-step subranging architectures that use digital error correction. Perhaps most important, the mix of multistep design with hybrid packaging is the only practical way to meet the combined demands of size, speed, and resolution.

Each of the new converters presently holds sampling-rate speed records for its respective resolution (for more information on the industry's latest high-resolution, high-speed, sampling ADCs, see the special report on page 47 of this issue).

The largest of the group is Analog Devices' AD9014, which can be considered a complete subsystem. Consisting of two custom chip-and-wire hybrids mounted on a multilayer pc board of 3.25 by 4.225 in., it contains power-supply bypass capacitors and a right-angle SMC connector carrying the analog input signal. The total "thickness" of the board plus components is still just 0.5 in.

Although positioned at opposite ends of the speed-resolution spectrum, the 16-bit Datel converter and the 12-bit Comlinear unit each can squeeze into a 40-pin triple-width DIP. These chip-and-wire hybrids



A TWO-STEP SUBRANGING ADC, **Analog Devices' AD9014, samples the input signal and applies it to the main flash converter, which produces the MSBs. The flash output is applied to a DAC, whose output is in turn summed with the original input voltage. The difference is then applied to a second flash ADC. The combined outputs of the two flash ADCs form the output of the two-step ADC.**

are just 1 by 2 in.

Analogic's 16-bit, 1-MHz unit, which occupies about 2/3 the area of the AD9014, comes in a 2.5-by-3.5-in. metal-can module.

Who Needs 'Em?

These versatile converters are at home in conventional time-domain applications. They perform high-speed, high-resolution conversions of one, or often numerous, slowly changing (relative to their sampling rate) signal(s). However, they can also operate on one fast signal in the frequency or time domain. As a result, all are well-designed, specified, and tested for both domains. For instance, each converter guarantees no missing codes over temperature for time-domain use—at the maximum resolution. Similarly, a full suite of dynamic specifications, at low frequency and close to Nyquist, were provided for frequency-domain applications. These include one or more signal-to-noise and one or more harmonic distortion characteristics *(see the table).*

In a basic frequency-domain application, ADCs simultaneously downconvert and digitize a band-limited "high-frequency" signal. Here, the definition of "high frequency" is a function of the ADC's sampling rate. For example, the 10- and 20-MHz converters focus on handling the output of the intermediate-frequency amplifiers in radar or communications receivers. In many cases, they operate in an undersampling (or super-Nyquist) mode, in which the input signal is higher in frequency than half of the sampling rate. As long as the input bandwidth of the ADC's sample-and-hold amplifier (SHA) is equal to (or preferably greater than) the input frequency, the digitized signal will be aliased into base band. Similarly, sampling oscilloscopes can use these converters to digitize repetitive signals—for example, pure sine waves—well beyond the ADC's sampling rate. It's only necessary to ensure that each incoming signal cycle is sampled at a different point on the waveform.

The slower 16-bit devices employ lower carrier frequencies. However, they too can undersample: For example, the full-power bandwidth of the ADS-930 is a minimum of 1.5 MHz, and is typically at 2 MHz. Alternatively, they can be used at base band after the classic heterodyne techniques downconvert high-frequency carriers.

With the exception of pure oscilloscope-type applications, the output of virtually all of these converters feeds a digital-signal-processor chip or system. The processor in turn pulls signals out of noise, filters them, and often determines their source and intimate characteristics, such as "Is this radar signal friend or foe?" Usually the processor performs one or repeated fast Fourier transforms (FFTs) on the signal to produce its spectrum. In fact, a major application area for these types of ADCs is spectrum analysis.

Time-domain applications break down into the two major areas typically served by ADCs: digitizing a single fast-changing waveform, such as from CCD optical/infrared detectors and imagers; and digitizing many slowly varying signals at the output of a multiplexer at high speed. These include various medical and analytical instruments ranging from CAT scanners and nuclear-magnetic-resonance (NMR) systems to blood analyzers and gas and liquid chromotography systems. Input signals for most of these instrument applications carry information with a dynamic range from 100 to 120 dB and thus use a programmable gain amplifier (PGA) ahead of the ADC. However, the greater the ADC's dynamic range, the simpler the software for the digital signal processor and the faster it can run.

How They Work

Those are the similarities shared by these four machines; the next step is to look at how they work and the features that set them apart. While lower sampling-rate 16-bit converters have existed a while, the concept of a converter spitting out 14-bit parallel words at 10 MHz may still seem like something out of a designer's dream.

The AD9014 is a good example of what can be achieved with a two-step

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digital error-correcting architecture when the technology is pushed (not all multistep ADCs incorporate error correction, but at resolutions beyond 10-bits, it's virtually mandatory to ensure accuracy). Sampling a 10-MHz sine wave at 10 MHz (twice Nyquist), the device achieves a typical spurious-free dynamic range (SFDR) of 72 dB (11.7 bits). At close to Nyquist (a 4.3-MHz signal) SFDR is a minimum of 86 dB (14 bits). The AD9014's design typifies one of the two basic architectures used to build two-step ADCs *(see the figure)*. It consists of eight basic blocks. An input amplifier and a SHA form one of the hybrids. The other hybrid holds the 8-bit main-range flash ADC, an 8-bit digital-to-analog converter that's 16-bit accurate, a summing amplifier, a second 8-bit (residue) flash ADC, digital error-correction circuits, and timing circuits.

The input amplifier, a single-ended-in, differential-out buffer, drives the unique differential-in, differential-out SHA. The SHA samples the signal on a pair of capacitors, one between each input and output. Its output is then applied to the 8-bit main-flash converter and is quantized.

The resulting digital word (the MSBs) is fed to the 8-bit DAC and to the digital correction circuit—an adder. The output of the DAC and the voltage held in the SHA drive opposite-polarity inputs of the summing amplifier. At this point, they're subtracted from each other by the high-speed precision summing amplifier, and the difference is gained up and applied to the second flash converter. Its 8-bit output combines the 8 MSBs that provide the typical two bits of overlap required by the correction circuits to create the converter's 14-bit-accurate output.

The differential SHA reduces even-order spurious harmonics in the digital output. The harmonics are caused both by the amplifier's finite gain-bandwidth and by noise that affects the switching points between the sample-and-hold states. The circuit is switched between states by two diode bridges, one for each input-output.

The AD9014's 16-bit DAC is a custom chip that also uses differential circuits, including the diode switches that replace transistor current switches, to minimize settling time. The ECL encode input is also differential. The device's input impedance at the SMC connector can act as the termination of a 75-Ω coax line. A 1-kΩ resistor isolates each ECL output from the analog circuits. This isolation requires placing ECL latches, or receivers, as close as possible to the output pins.

At 20 MHz, the Comlinear CLC936 sets a sampling-speed record for hybrid 12-bit ADCs, which was 10 MHz. Sampling a near-Nyquist 9.992-MHz sine wave at 20 MHz, it achieves a spurious-free signal range of 69 dB (11.2 bits). Like the other ADCs, it comes complete with a reference and clock. The input buffer amplifier has a bandwidth of 70 MHz and an input impedance of 50 kΩ in parallel with 5.5 pF. As a result, it hangs easily on a 50- to 100-Ω terminated input line and will not degrade signals well above Nyquist. In fact, the converter's large signal bandwidth is a minimum of 45 MHz. Furthermore, internal ECL latches and buffers on the output eliminate the need to add them to the pc board.

CIRCUIT MAGIC

If it takes two bits of overlap for error correction, how is a 16-bit two-step ADC built with 8-bit flash ADCs? Though several 10-bit flash ADCs are available with 1024 comparators each, they're uneconomical in today's 16-bit ADCs.

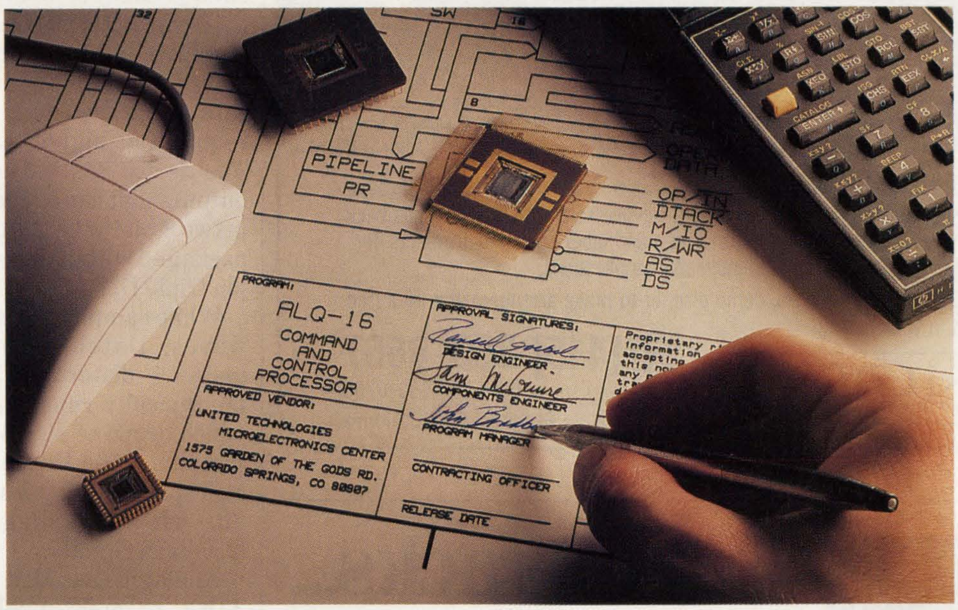
Therefore, to achieve 16 bits, Da-

HIGH-SPEED SAMPLING ADC SPECIFICATIONS

Specifications	CLC936AC Value	CLC936AC Conditions (f_{in}, MHz)	AD9014K Value	AD9014K Conditions (f_{in}, MHz)	ADC4344 Value	ADC4344 Conditions (f_{in}, kHz)	ADS-930 Value	ADS-930 Conditions (f_{in}, kHz)
Resolution (bits)	12		14		16		16	
Maximum sampling rate (MHz)	20		10		1		0.5	
Signal-to-(noise + distortion) (dB)	−72 −68	1.98 9.992	−75 (t)	0.54			−87 (t) −80 (t)	100 250
Total harmonic distortion (dB)	−71 −68	1.98 9.992	−90 −86	0.54 4.3	−90 −75	20 500	−95 (t) −89 (t)	100 250
Spurious-free dynamic range (dB)	72 72	1.98 9.992	90 86	0.54 4.3	92 82	100 500	not specified not specified	
Intermodulation distortion (dB)	−73	6.3 and 6.4	−90	2.3 and 2.4	Not available			
Full-power bandwidth (MHz)	45		60 (t)		1		1.5	
No-missing-code operation (bits)	12	Over temperature	14	Over temperature	16	Over temperature	16	Over temperature
Input-signal ranges (V)	±1		±1		±2.5, ±5 0 to +5, 0 to +10 0 to −5, 0 to −10		±5, ±10 0 to +10 0 to −10	
Power supplies (V)	±5, ±15		±5, ±15		±5, ±15		±5, ±15	
Power dissipation (W)	4.5		11.5		4		2.2	
Price (100s) ($)	750		2800		750		337	

Note: All specifications are minimums or maximums unless specified as typical (t).

At last, radiation survivability is standard procedure.



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CIRCLE 97

tel's ADS-930 employs several clever circuit tricks with 8-bit flash chips. It uses the second basic two-step architecture, in which the signal is passed through the same flash ADC twice, first to get the MSBs and then to develop the remaining LSBs.

In addition to the proprietary circuits needed for 16 bits, Datel added a 16-word FIFO (first-in, first-out) memory, whose contents can be stored at the 500-kHz throughput rate and passed on to the host when required at higher, or lower, rates. The device has latched, three-state outputs that can be read in parallel or in two 8-bit bytes. All of this has been packaged within the confines of a 40-pin triple DIP.

While sampling dc-to-100-kHz sine waves, Datel's device signal-to-(noise + distortion) ratio—S/(N + D), typically runs 87 dB (14.2 bits), which drops to 80 dB (13-bits) when sampling 250-kHz sine waves. Datel also specifies no missing codes to 15 bits when sampling Nyquist-rate (250-kHz) signals.

Analogic cascaded two 8-bit flash ADCs to build a 9-bit ADC. Two passes through it supply two bits of overlap. The overrange bit from one flash ADC becomes the MSB. A 16-bit-accurate, 9-bit DAC assures 16-bit accuracy. Total harmonic distortion plus noise is a minimum of 88, 84, and 77 dB as it samples, at 1 MHz, signals of 20, 100, and 500 kHz, respectively (14.3, 13.7, and 12.5 effective bits, respectively).□

PRICE AND AVAILABILITY

Sample quantities of all devices are available. See the table for prices.

Analogic Corp., 360 Audubon Rd., Wakefield, MA 01880; Don Travers, (508) 977-3000. CIRCLE 511

Analog Devices Inc., P.O. Box 9106, Norwood, MA 02062-9106; Allen Hill, (919) 668-9511. CIRCLE 512

Comlinear Corp., 4800 Wheaton Dr., Fort Collins, CO 80525; Allan Hansford, (303) 226-0500. CIRCLE 513

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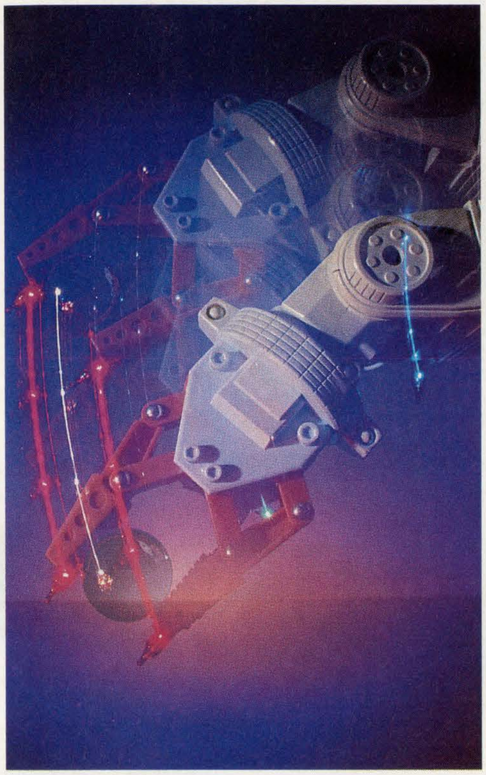

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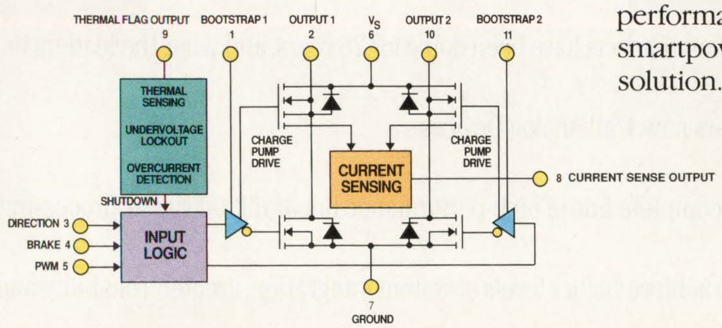

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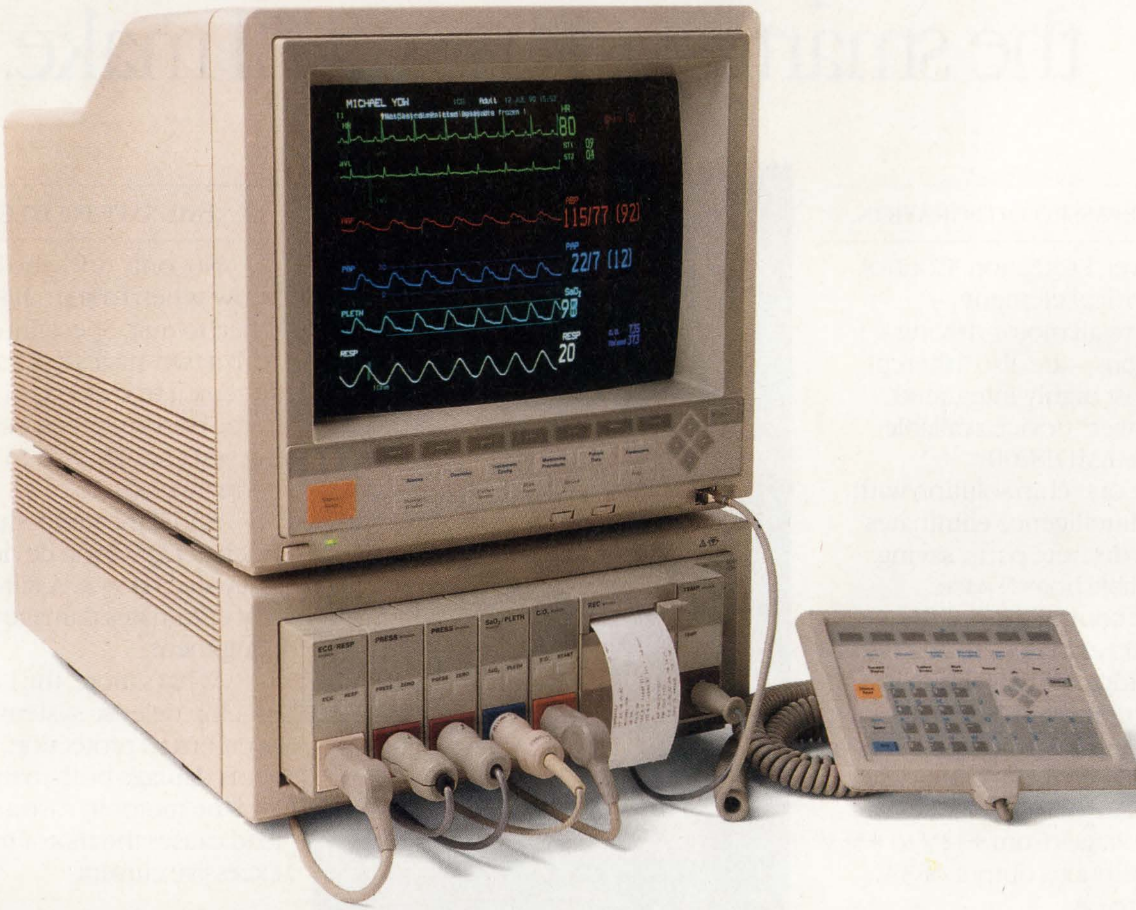

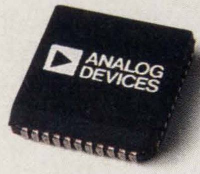

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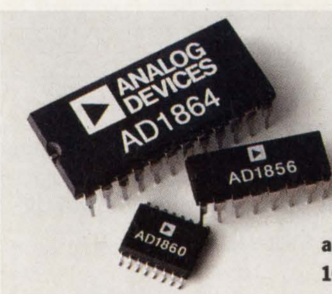

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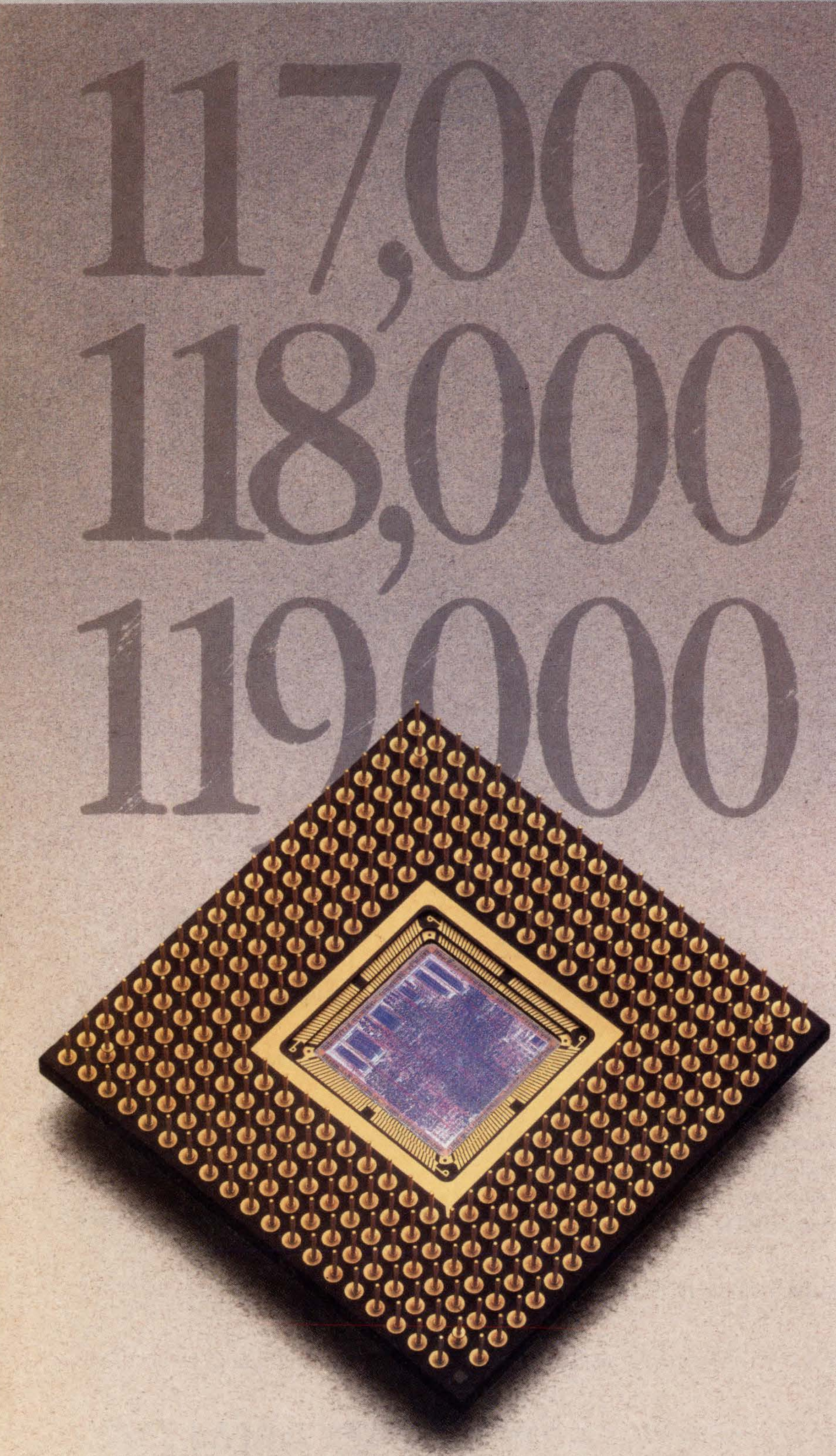

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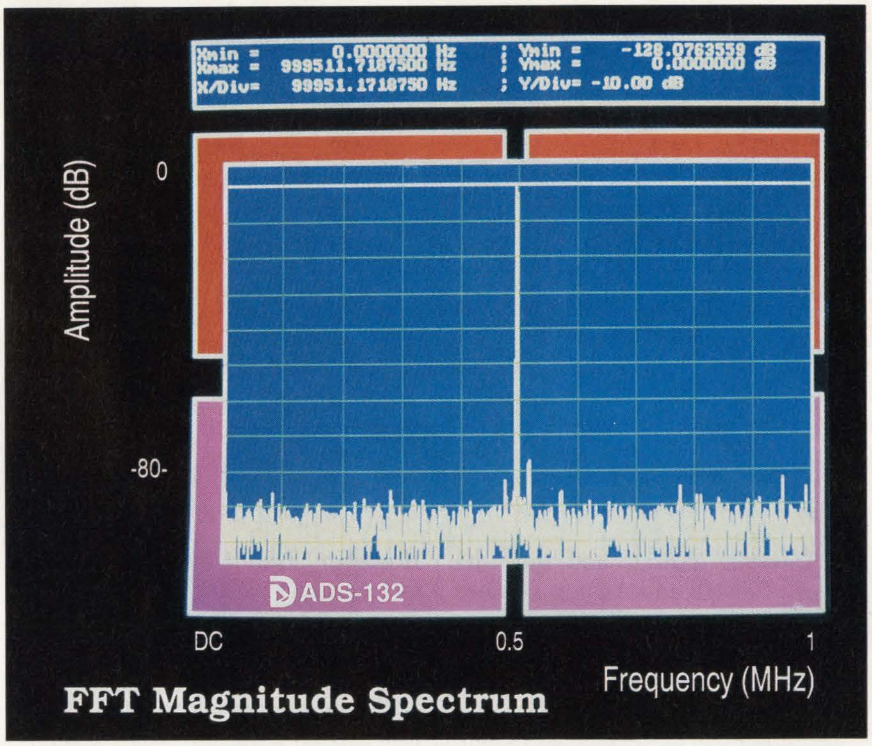
CIRCLE 137



FRANK GOODENOUGH

IC SAMPLING 12-BIT ADCS REACH 1-MHZ NYQUIST AND HYBRIDS REACH 20 MHZ—ALL SPORT DYNAMIC SPECIFICATIONS.

12-BIT SAMPLING ADCS COME OF AGE

Fast 12-bit and greater analog-to-digital converters (ADCs) have grown exponentially over the past four years, flooding the field with continually improving devices. The tables in this report defining just the 12-bit converters show that more than 90% of those converters didn't exist in the fall of 1986, when ELECTRONIC DESIGN published a similar roundup of ADCs *(*ELECTRONIC DESIGN, *Sept. 4, 1986, p. 90)*. And the performance reported in this report was just a goal back then.

Even if you're "up" on ADCs, you may find a few surprises while perusing these tables:

• Hybrid, and even discrete-device, converters are still going strong. In fact, in the gray area of throughput rates between 200 kHz and 2 MHz (conversion times between 5 and 0.5 μs), they still vie for sockets.

• If you haven't used sampling converters—converters with built-in sample-and-hold amplifiers (SHAs)—you may be surprised by the dominance of that architecture in both new ICs and hybrid 12-bit ADCs. In the 200-kHz to 2-MHz gray area and at higher speeds, virtually all new designs employ a multistep (multipass or subranging) architecture, regardless of other design aspects.

• Autocalibrated converters, new just four years ago, are now coming to center stage. Today they challenge classic laser-trimmed devices and newer, open-loop switched-capacitor designs in performance, power, and price.

• Though monolithic 12-bit ADCs seem to have hit a wall at 1 to 2 MHz, hybrids apparently don't have any speed limits. But you still may see a one-chip 12-bit converter running at 10 MHz within 18 months.

• With price erosion, you can now buy a 12-bit, 15-μs, ADC for "a buck a bit." (Note: Throughout this report, and in the tables, all values are minimums/maximums and over the device's operating-temperature range, unless noted.)

• The biggest surprise may be that the granddaddy of all 12-bit IC ADCs, the 12-year-old Analog Devices' 574, is still spawning clones (how many 12-year old digital ICs can make that boast?). Moreover, it didn't become a one-chip IC until about four years ago.

WHO'S DRIVING?

Many questions arise when trying to analyze the high-resolution ADC boom. Was it driven by the market, the technology, or the people? And what made it possible—new process, new architectures, or both? As with most major advances, it took a mix of all of these factors. Both the military and industrial markets have demanded faster, more-complete, smaller, lower-power, and lower-

TABLE 1. A FEW 12-BIT, NON-SAMPLING MONOLITHIC ADCs

Model	Company	Conversion time (ms)	Integral linearity error (±LSB)	Offset error (LSB)	Gain error (±LSB)	Input voltage range(s) (V)	Nominal supply voltage(s) /power (V/mW)	Package, features and output format (see footnotes)	Cost (100s)
ADC601	Burr-Brown	0.9, 0.7 (t)	1/2	2	±4	±5, ±10, 0 to – 10	±15, +5/1.7	1, 2, 4, 6, 21	$86
AD671K-750	Analog Devices	0.75	1	10	±4	±5, 0 to 5, 0 to 10	±5/620	2, 4, 26, 27	$75
AD7586K	Analog Devices	1	1.5	2	±2	0 to – 4	±5/300	2, 3, 4, 28	$80
AD7572L	Analog Devices	3	1/2	4	±8 (25°C)	0 to 5	+5, – 15/215	1, 2, 3, 4, 5, 27, 29, 30	$27
MAX7572	Maxim	3	1/2	4	±10 (25°C)	0 to 5	+5, – 15/215	1, 2, 3, 4, 5, 27, 30	$25
MAX170	Maxim	5.6	1/2	3	±10 (25°C)	0 to 5	+5, – 15/205	1, 6, 31, 32	$15
ADC-912	PMI	12	1/2	NA	NA	0 to 10	+5, – 15/95	2, 3, 4, 5, 27, 32	$12

Notes: All specifications are maximums or minimums and overtemperature unless noted.

Footnotes:
1 Reference
2 Clock or timing
3 Three-state output
4 Parellel output
5 Two bytes
6 Serial
21 32-pin DIP
26 Overrange flag
27 24-pin DIP
28 28-pin DIP
29 28-pin PLCC
30 5- 10-, 12-ms devices available
31 8-pin DIP
32 SOIC

cost converters. However, technology was also a driving force: hybrid for the fastest and most-complete devices, and monolithic for minimum size, power, price, and complexity without loss of versatility or accuracy. Moreover, it took new architectures and new semiconductor processes in both hybrids and ICs.

Hybrids (and other forms of multidevice technology) are still here today because they and the IC converter represent a symbiosis, which at times is planned. Multidevice converters act as the leaders in applying the latest semiconductor devices and in developing new architectures. Although first used to build 10-to-40-MHz pc-board converters, the two-step, or half-flash, architecture employing digital error correction was refined to build the first 12-bit, 1-μs (conversion time) IC ADCs in hybrid form *(for a working description of a subranging ADC and a taste of greater-than-12-bit devices, see the cover feature in this issue, p. 37)*.

Today, the two-step converter (or a subranging design using a greater number of passes) replaces the successive-approximation architecture for virtually all high-speed IC and hybrid ADCs, even challenging the monolithic flash itself. Yet, indicative of the hybrid-monolithic symbiosis, one or more monolithic flash converters lie at the heart of every hybrid and monolithic subranging ADC. For example, the four fastest monolithic 12-bit ADCs—the 0.5-μs Catalyst CAT5412, the 0.75-μs Analog Devices AD671, and the 1-μs Crystal CS5412 and Analog Devices AD7586—all use multistep designs *(see Tables 1 and 2)*.

Design Decisions

Complementing these ICs are non-sampling, two-step hybrids. Hybrids with conversion times ranging form 0.3 to 1 μs are available from Analog Devices, Burr Brown, Datel, ILC Data Devices Corp.(DDC), Micro Networks, Sipex (formerly Hybrid Systems) and Teledyne Components (formerly Teledyne Philbrick). Moreover, some of these hybrids are challenging the monolithics. For example, Datel's ADC-530 converts in 300 ns and offers no-missing codes to 12 bits over temperature along with ±3/4-LSB integral linearity. It comes in a 32-pin triple-width ceramic DIP and costs just $237 each in 100s. Another Datel device, the ADC-511, converts in 1 μs, is also 12-bit accurate over temperature, goes for $154 each in 100s, and comes in a tiny 24-pin double-width ceramic DIP (for the performance). Both chips run off 5- and ±15-V rails. The ADC-530 and -531 dissipate 2.1 W and 1.25 W, respectively. Full-scale input voltage ranges of the ADC-530 are 0 to 10, 0 to 20 and ±10 V. The ADC-511 handles 0 to 2.5, 0 to 5, and 0 to 10 V, as well as ±2.5, ±5 and ±10 V.

Looking at the monolithic ADCs, the AD671K-750 converts in 750 ns and guarantees 12-bit no-missing-codes over temperature, coupled with ±1-LSB integral linearity. However, it comes in 24-pin plastic and ceramic skinny DIPs with the former costing $75 each in 100s. The brand new Analog Devices AD7586 converts in 1 μs and also guarantees 12-bit no-missing-codes over temperature, delivering an integral linearity of ±1.5 LSB. Moreover, it also boasts a bus-access time of 57 ns while that of the AD671 is typically 200 ns. Few hybrids specify the access time. In fact, this specification, which is vital if you're interfacing with a microprocessor bus, is either missing from most data sheets or buried somewhere in a data sheet's interior (the same is often true of conversion times). The AD7586K also goes for $80 each in 100s.

Input signal ranges and power-supply requirements may be the key factors in choosing between these converters. The 530 and 511 need 2.5 and 1.2 W of power, respectively, from their 5-V and classic ±15-V rails, while the 671 and 7586 run off ±5 V. The 530 and 511 need just 621 mW, and the 671 and 7586 need a mere 300 mW. On the other hand, the hybrids handle a wide range of "standard" input voltages without signal conditioning; the 530 takes 0 to 10, 0 to 20, and ±10 V; the 511 takes those ranges plus 0 to 2.5, ±2.5, and ±5 V. The 671 handles 0 to 5, 0 to 10 and ±5 V. However, the 7576, like many of the newer IC converters, is limited to a rather unconventional signal-voltage range—in this case 0 to –4 V.

None of the converters were de-

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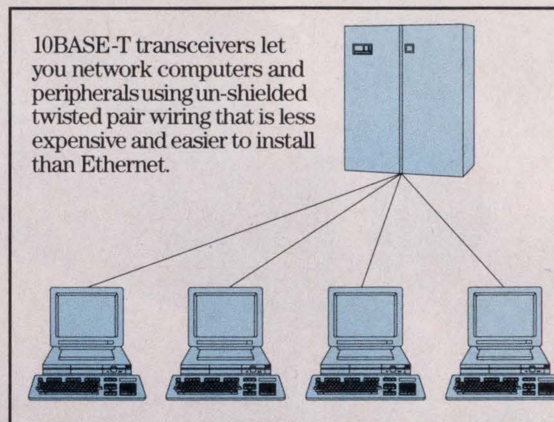

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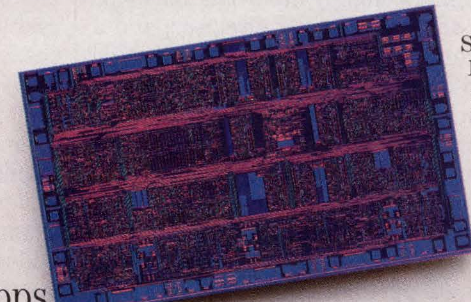

Semi-standard options of the standard 10BASE-T circuits are possible simply by modifying the metal mask on the FB3651 tile array.

And, unlike much of the technology you've been hearing about, these are products of experience. We've been shipping twisted pair transceivers since 1987, as part of Synoptics' LattisNet network.

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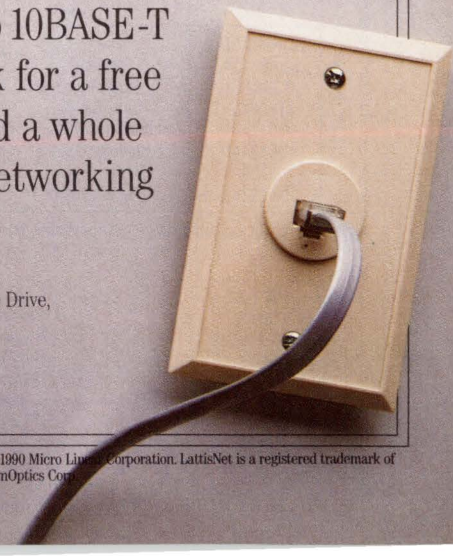

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CIRCLE 133

veloped without potential customers. Driven by the microprocessor's ubiquitous computing power, military, industrial, scientific, and medical-instrumentation markets need high-speed, multichannel, data-acquisition systems. By adding a fast sampling amplifier externally, you can grab 500-kHz waveforms.

In truth, five years ago, who would have expected to be able to buy a 10-MHz, 12-bit ADC smaller than a business card? On top of that, who would have presumed that the price for a commercial device would drop to under $500 and the size to 1 by 2 in.—with multiple suppliers? Nonetheless, today seven suppliers of these converters exist with prices running from less than $500 to over $1000 *(see Table 3)*. To cap it off, these sampling converters can continuously grab pieces of Nyquist-rate (5-MHz) sine waves.

Only hybrid technology could do the job of meeting all the specifications, requiring the two-step architecture. The first four hybrids came from a military-funded development involving Analog Devices, Burr-Brown, DDC, and TRW. The four companies agreed on the package size and pinout (2.4 by 1.6 in. and 46 pins). A fifth player, Comlinear, helped reduce the package to a 40-pin, 1-by-2-in. DIP. Since then, Datel and Sipex have entered the fray.

Although one or more off-the-shelf 6- to 8-bit flash converters can do the basic quantizing job, most suppliers employ many custom chips for the pure-analog circuitry, and a gate array for the high-speed logic and digital output circuits. The custom analog chips perform precision switching, sampling, gain, and buffering. Most are built on ultra-fast complementary-bipolar processes. In addition, custom, 12-bit-accurate IC DACs with 6-, 7-, or 8-bit resolution (depending on the resolution of the flash converters used) determine basic ADC accuracy. These high-speed DACs employ bipolar current switches and laser-trimmed thin-film resistors in segmented and/or binary-weighted architectures. All of these hybrids are complete converters incorporating a reference, SHA, clock, and timing circuits.

The military uses these converters in radar and electronic-countermeasure receivers to simultaneously down-convert the output of the intermediate-frequency amplifiers to base band and digitize the base band. The converters' outputs are fed to a digital signal processor, which pulls signals out of noise and performs a spectrum analysis to identify the signal source—is it friend or foe? As a result of their price-performance, these tools are now finding their way into various non-military applications. These span from broadband rf communication systems, where they duplicate their radar function, to general- and special-purpose spectrum-analysis equipment for test and measurement, to medical equipment, such as CAT scanners, where they digitize many channels of data at high speed.

What's next in this land of blinding speed and accuracy? To start, as the cover story on page 37 indicates, speed and resolution have already moved up, with Comlinear offering 15- and 20-MHz 12-bit converters and Analog Devices a 10-MHz, 14-bit unit. Datel is ex-

TABLE 2. A SAMPLING OF 12-BIT, SAMPLING IC ADCs

	Model	Company	Conditions: Sampling rate (kHz)	Conditions: Input frequency (kHz)	AC specifications: Signal-to-(noise + distortion) ratio (db)	AC specifications: Total harmonic distortion (dB)	AC specifications: Suprious-free dynamic range (dB)	Total conversion time (μs)
Non-autocalibrated	ADS7800K	Burr-Brown	330	47, 150	69, 67 (t)	– 77	77, 75 (t)	3
	AD678K	Analog Devices	200	10, 100	71, 70 (t)	– 80	80	5
	AD7870L	Analog Devices	100	10, 100	72, 71, 5 (t)	– 80, – 86	80, 86	7.6
	AD7875L	Analog Devices						9
	MAX164	Maxim	100	10, 50	70, 70 (t)	– 76	76	8.7
	MAX177	Maxim	100	10	64	– 72	72	7
	AD7880C	Analog Devices	66	1, 30	70, 66 (t)	– 80 (t)	80 (t)	15
	LTC1292	Linear Technology	50	25 (Nyquist)	73 (t)	na	na	20
Autocalibrated	CAT5412	Catalyst	2,000	100/490	70 (t)/NA	0.02% (t)/NA	75 (t)/72 (t)	0.7
	CS5412	Crystal/Gould	1,000	100/490	68/70 (t)	0.013% (t)/NA	75/70 (t)	1.4
	C55012A	Crystal/Gould	100	12	72 (1 kHz in)	0.008% (t)	84	7.2
Autocalibrated, 12-bit + sign	SDA11812D	Siemens	100	1/50	69/66	na/– 75 (t)	na	6
	SDA0812A	Siemens	100	na	na	na	na	6
	TLC1225B	Texas Instruments	100	na	na	na	na	10
	ADC7802	Burr-Brown	83	na	na	na	na	8
	ADC12451	National/TRW	83	20	73.5	– 78	80 (t)	8
	ADC12441	National/TRW	55	20	76.5	– 75	na	14
	ML2230	Micro Linear	32	10	73 (t)	– 75 (t)	na	31
	ML2221	Micro Linear	32	10	73 (t)	– 75 (t)	na	31

Notes: NA = not available, na = not applicable, (t) = typical

Footnotes:

1 Reference
2 Clock or timing
3 Three-state output
4 Parallel output
5 Two bytes
6 Serial
8 Power-down
9 Two-, six- eight-channel versions available
12 Four-channel
13 12-bit + sign
14 Eight-channel versions with reference available
27 24-pin DIP
28 28-pin DIP
29 29-pin PLCC
31 8-pin DIP
32 SOIC
34 40-pin DIP
35 40-pin CLCC

pected to have similar devices sometime next year, while other players to plug away. However, the dream of a 12-bit monolithic ADC running at 10 MHz may come true before the end of 1991; it, too, will be a sampling converter.

To answer questions that may have arisen concerning sampling, it's probably best to discuss a few IC and hybrid devices available from the feast of sampling ADCs *(see Tables 2 and 3, again)*. In the classic SHA-ADC application, the SHA is located between an analog multiplexer and a successive-approximation-register (SAR) ADC in a data-acquisition system. It ensures that even the slowly changing data from a thermocouple, or noise on the ac line, won't degrade the conversion's accuracy. It also enables the multiplexer to move on to another channel (Remember, the aperture time of a SAR-type converter is its conversion time. For example, the maximum sine wave that can be converted by a 12-bit, 100-μs SAR ADC is about 10 Hz. Higher frequencies—signals slewing faster than 0.2 V/μs—will be aliased).

Data-acquisition systems incorporate a multiplexer, SHA, and ADC in one package, thus simplifying the job of system designers. However, with the advent of digital signal processors operating on just one, or several, ac signals, the SHA's job has changed. Now, it must accurately and repeatedly supply samples of a fast-changing waveform to a high-speed ADC. With the ideal SHA, the ADC can quantize, or digitize, Nyquist-rate signals that are just a few hertz below one-half the sampling frequency. New rules apply when handling these dynamic signals. Now the important specifications are signal-to-noise ratio (SNR), signal-to-(noise + distortion) S/(N + D) ratio, effective number of bits (ENOB), total harmonic distortion, peak harmonic or spurious noise (also called spurious-free dynamic range), and intermodulation distortion *(to define and measure these specifications, see* ELECTRONIC DESIGN, *May 10, p. 95)*.

All of these specifications are measured at the converter's output by running a fast Fourier transform (FFT) on a PC or other computer. The result is a spectrum analysis *(see opening figure, which shows the spectrum of Datel's ADS-132 ADC sampling a 1-MHz sine wave at Nyquist frequency)*. For example, S/(N + D) is the ratio, expressed in dB, of the rms value of the measured input signal (which must be a "pure" sine wave) to the rms sum of all other spectral components below the Nyquist frequency—including harmonics but excluding dc. For the "ideal" ADC, S/(N + D) = (6.02n + 1.76) where n is the number of bits. Thus, for an "ideal" 12-bit ADC, the effective number of bits equals 74 dB. Solving the equation for n we get

$$n = \frac{S/(N + D) - 1.76}{6.02}$$

which is the ENOB, the dynamic performance of the converter, in bits, for a given sampling rate. Note that in the tables, the best specified converters give the dynamic specifications at some low frequency and at a frequency that's close to Nyquist. Ideally, data sheets should supply a

Integral linearity error (LSB)	Errors (±LSB) Offset Unipolar	Offset Bipolar	Gain	Input voltage range(s) (V)	Nominal supply voltage(s) and power (V/mW)	Package features and output format (see footnotes)	Cost (100s)
±1/2	NA	2	4 (25°C)	±10, ±5	5, – 15/215	1, 2, 3, 4, 5, 27, 32	$34
±1 (t)	2	10	4	0 to 10, ±5	±12, +5/745	1, 2, 3, 4, 5, 27	$35
±1	NA	5	5	±3	±5/95	1, 2, 3, 4, 5, 6, 28, 29	$30
±1	5	NA	8 (25°C)	0 to 5	±5/95	1, 2, 3, 4, 5, 27, 29	$30
±1	NA	6	10 (25°C)	±5	±5, – 12/150	1, 2, 3, 4, 5, 27, 32	$21.25
±1	NA	±8 mV	4 (25°C)	±2.5	±5, – 15/150	1, 2, 3, 4, 5, 29, 32	$10
±1	5	5	5	0 to 5, 0 to 10, ±5	+5/25	3, 4, 8, 27, 32	$16
±1/2	1.5	1.5	1/2	0 to 5, ±5	5 or ±5/500	3, 6, 8, 9, 31	$16
±1.5	1/2	1/2	1/2	0 to 3, ±1.5	±5/1000	3, 4, 34	$98
±1	NA	8	8	3 (pk-pk)	±5/1000	3, 4, 34, 35	$162
±1/2	Total unadjusted error = ±1/2 LSB			0 to 5, ±5	±5/250	3, 4, 5, 6, 34, 35	$24.60
±1/4	Total unadjusted error = ±3/4 LSB			0 to 5	5/25	2, 3, 5, 8, 12, 28, 29	$22.95
	Total unadjusted error = ±1/2 LSB			0 to 5	5/25	2, 3, 5, 8, 12, 28, 29	$20.15
±1/2 (unipolar input)	1/2	1/2	1	0 to 5, ±5	±5/25	3, 5, 13, 28	$17.25
	Total unadjusted error = ±1/2 LSB			0 to 5	5/25	2, 3, 5, 8, 12, 28, 29	$19.95
±1 (t)	3	3	3	0 to 5, ±5	±5/113	3, 5, 13, 29	$14.90
±1 (t)	1	1	2	0 to 5, ±5	±5/113	3, 5, 13, 29	$13.90
±1/2	NA	1	1	±2.5	±5/400	3, 5, 13, 14, 28	$15.95
±1/2	NA	1	1	±2.5	±5/400	3, 6, 13, 28, 29	$14.95

TABLE 3. 12-BIT, HYBRID SAMPLING ADCs

Model number	Company	Sampling rate (MHz)	Input frequency (MHz)	Signal-to-(noise + distortion) ratio (dB)	Total harmonic distortion (dB)	Peak harmonic or spurious noise (dB)	Full-power bandwidth (MHz)	Ingegral linearity error (LSB)	Input-voltage range (s)/ power (V/W)	Package, features and output format (see footnotes)	Cost (100s)
AD9005	Analog Devices	10	0.54/4.3	65/60	NA	−70/−65	38 (t)	±2.5	±1/4.2	1, 2, 4, 15, 18	495
ADC603	Burr-Brown	10	0.1/4.99	64/61	−67/−62	NA/−65	30	±1.25	±1.25/6.1	1, 2, 4, 15, 18	590
CLC926	Comlinear	10	0.4/4.99	62/59	−64/−60	−65/−63	45	±3	2pk-pk ±2/5 (t)	1, 2, 4, 16, 18, 34	835
ADC-00110	DDC*	10	0.1/4.99	66/64	−66/−64	NA	30	±0.05%	±2.5/9	1, 2, 4, 15, 18	1150
ADS-130	Datel	10	0.5/4.99	65/63	−68/−65	−69/−66	30	±1	±1.25/4	1, 2, 4, 16, 34	549
SP9560	Sipex	10	0.1/4.99	68/64 (t)	−72/−68 (t)	NA	NA	±1/2 (t)	±1/3.6 (t)	1, 2, 4, 15, 18	700
THC1202	TRW	10	0.4/4.99	62/59	−64/−60	−65/−63	45	±3	2pk-pk ±2/6	1, 2, 4, 16, 34	595
ADC604	Burr-Brown	5	0.08/2	65/62	−77/−73	−77/−73	30	±1.25	±1.25/7	1, 2, 4, 15, 18	1121
ADS-131	Datel	5	0.5/2.5	65/63	−68/−65	−68/−65	30	±1	±1.25/4	1, 2, 4, 16, 34	439
ADS-132	Datel	2	0.1/1	NA	−72/−67	NA	(19)	±1/2	(20)/3.2	1, 2, 3, 4, 16, 21	277
ADC-00305	DDC*	2	0.1/NA	65	NA	−68	10	±0.025%	(22)/3.7	1, 2, 3, 4, 18, 23	340
MN6249K	MicroNetworks	2	0.1/0.94	66/66	NA	−70/−70	12 (small signal)	±1	−2.5, −5/3,5 (t)	1, 2, 3, 4, 18, 23	305
ADS602	Burr-Brown	1	0.01/0.48	70/64	−75/−70	−76/−70	4	±1.25	0-to-10, ±5/3	1, 2, 4, 16, 21	165
ADS-112	Datel	1	0.1/0.5	66/66	−75/−68	−75/−70	2.5	±3/4	0-to-10, ±5/1.7	1, 2, 3, 4, 16, 27	207

Notes: * ILC Data Devices, NA = Not available, (t) = typical

Footnotes:
1 Reference
2 Clock or timing
3 Three-state output
4 Parallel output
15 Case: 2.3″ × 1.6″, 46 pins
16 5-V and ±15-V supplies
18 ±5-V and ±15-V supplies
19 sample-and-hold slew rate = 300V/μs, aperture jitter 40 ps max.
20 0 to −5, −10, −20, ±10, and ±5, ±10
22 0 to −5, −10, +5, +10, and ±2.5, ±5
23 Case: 1.3″ × 2.2″, 40-pin TDIP
27 24-pin DIP
34 40-pin DIP

family of curves made at various sampling rates, plotting input frequency on the horizontal axis, and ENOB and S/(N + D) on the vertical axis. In the sampling tables, dynamic specifications are given for two signal frequencies when available. A simple X-Y plot of ENOB vs. S/(N + D) makes a handy tool for relating the two specifications.

All of those dynamic specifications are for the SHA and ADC operating together, with the SHA first acquiring the signal and then switching into the hold state in minimum time. Then the converter can do its job. When sampling even Nyquist signals at rates below 10 kHz, circuit timing (and layout) with such ICs as the Harris HA-5320 and a 574 ADC isn't difficult. However, as frequencies climb, the need for a high-speed SHA and a converter in one package becomes obvious.

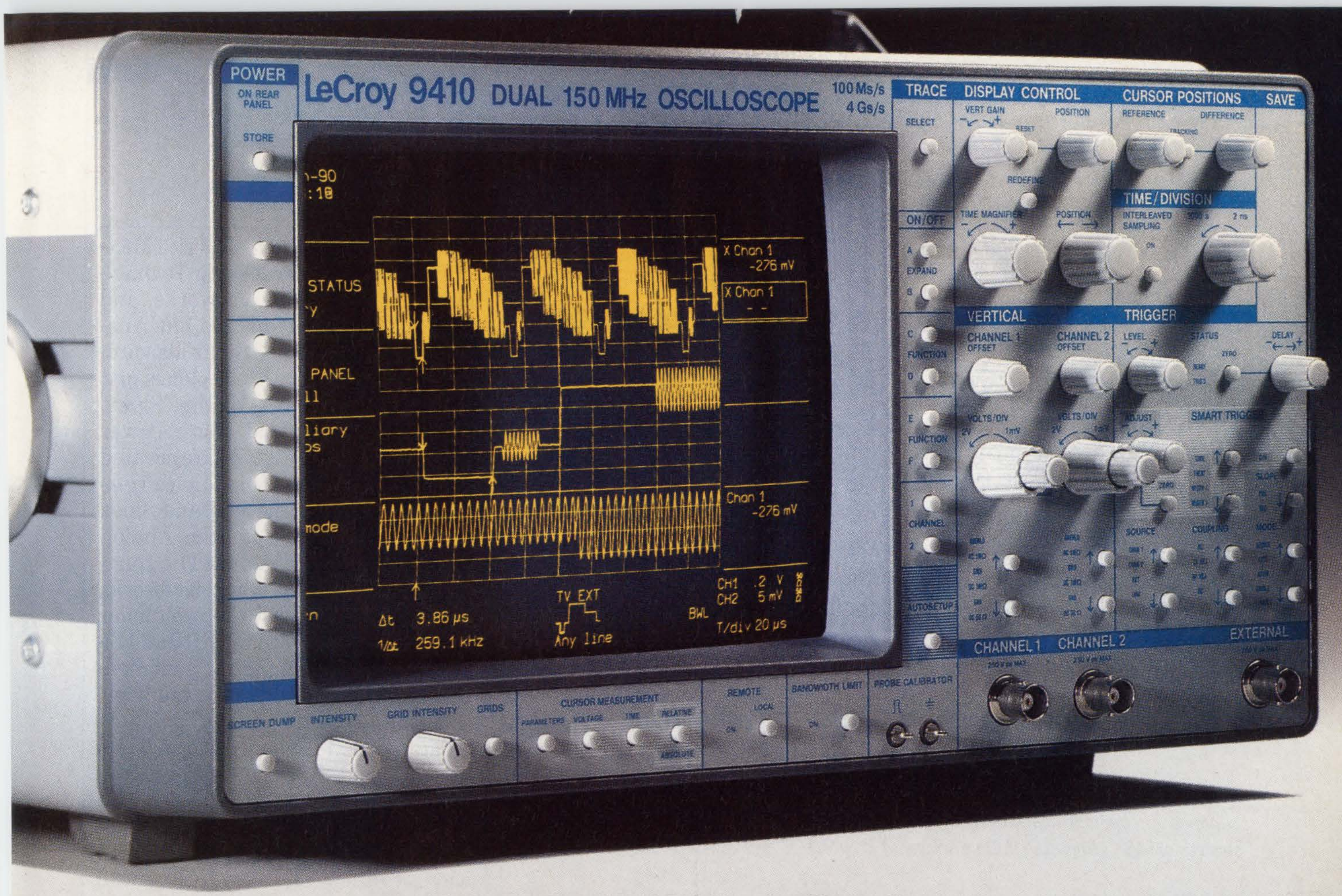
When 12-bit sampling ADCs started hitting the street, the auto- or self-calibrated devices for that venue began arriving—all being samplers as well as ICs. These can be found on the lower portion of the sampling IC table. These sophisticated devices either continuously, on command, or in the background, correct themselves for differential/integral linearity, zero, and gain errors. This eliminates the effects of time, temperature, and supply voltage. In fact, some offer a total unadjusted error of specification—at 12 bits—which includes linearity, zero, and gain. Autocalibrated ADCs should be considered when the ultimate in accuracy is required, even if sampling isn't an issue.

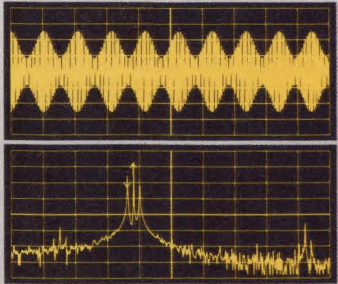
You can divide sampling ADCs into three basic classes offering overlapping cost-performance tradeoffs: hybrids, non-autocalibrated or basic ICs, and autocalibrated ICs.

In contrast with most hybrids, which employ two-step architectures with thin-film resistors setting their basic accuracy, the slower, basic sampling IC ADCs stick with the faithful SAR. Moreover, with the exception of the LTC1292 and the Burr-Brown ADS7800, which use a switched-capacitor (charge-redistribution) DAC, laser-trimmed thin-film resistors set the limits of both differential and integral linearity. Both the LTC1292 and ADS7800 are pure CMOS, but the remaining chips employ some form of bipolar-CMOS (biMOS, biCMOS) process. While some of the latter employ bipolar transistors for the current switches, most use CMOS switches. The ADS7800 samples at 330 kHz. However, unlike other monolithic sampling ADCs, it runs off standard supply rails (+5 and ±15 V) and handles standard ±5- and ±10-V input signals. Yet it dissipates only 215 mW. All of the non-sampling ICs also employ a SAR architecture implemented in biMOS.

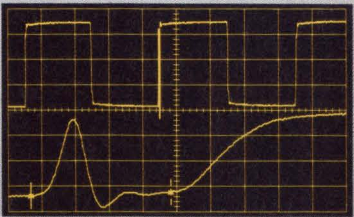
On the other hand, the autocalibrated converters (except for the Catalyst CAT5412, which is the fastest member of the species) employ some form of switched-capacitor technology, which in most cases offers inherent sampling. Both the Crystal CS5412 and the Catalyst chip employ two-step architectures. Catalyst's, however, is more conventional and uses a resistor-ladder DAC, while the former employs a capacitor DAC and a variable-reference generator for the chip's 6-bit flash converter. In addition, the Micro Linear ML2230 family, and the National/TRW ADC12451, ADC12441, ADC1251, and ADC1241 offer 12-bit + sign outputs. Though the last four are all sampling devices, the 1241 and 1251 offer superior dc performance (ac specifications aren't provided). Test procedures, and the number of good die per wafer, differ for the ac and dc specifications, resulting in different prices.

In addition to Analog Devices, there are at present count at least seven additonal sources for the 574





Spectrum Analysis Option



Glitch Trigger

and 674: Burr-Brown, Harris, Maxim, SPT (Signal Processing Technologies), Sipex, Micro Networks, and Micro Power Systems. All but Analog Devices, SPT, and Sipex also provide a 774. And four of the clones just appeared this year—Maxim, Sipex, Micro Networks, and Micro Power Systems. But not all 574s are created equal. Power dissipation ranges from 150 mW for the SPT and Sipex devices to 720 mW for the Analog Devices and Harris units. The Burr-Brown, Harris and Micro Networks ADCs use two chips, the remainder one. In addition, both the SPT and Sipex converters employ a switched-capacitor DAC, while the remainder, like the original 574, use laser-trimmed thin-film resistors. Thus the SPT and Sipex units are in the sampling camp. As a result, although not yet given ac specifications, they can digitize 10-kHz sine waves to 12-bit accuracy. And, these chips do not need a -15-V supply.

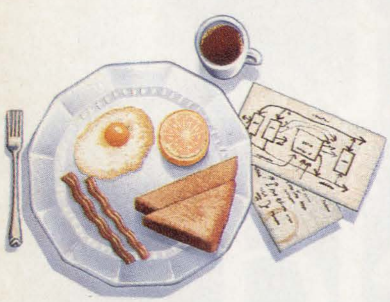
While the basic conversion specifications for all of these converters are similar, the ADCs can't necessarily drop into each other's sockets, due to subtle differences in timing characteristics. For example, bus-access times can vary. However, Micro Power Systems guarantees its new chips will work in any socket that has held a working Analog Devices 574 or 674. Less subtle is that fact that if you've designed in an SPT or Sipex device, you can't easily switch to the higher wattage units that need -15 V.

Finally, before the year is over, we'll see a one-chip 574 and 774 from Burr-Brown, using just 100 and 150 mW, respectively. These chips are based on the core of the ADS7800. They'll not only be sampling ADCs with switched-capacitor DACs, but will also be able to run off just a single 5-V rail. In addition, they'll be in skinnyDIP and SOIC packages. Why use a 574 if you're going to a new design and a new package? You can keep the same software.☐

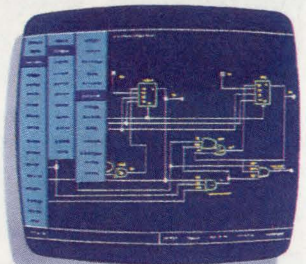
HOW VALUABLE?	**CIRCLE**
HIGHLY	550
MODERATELY	551
SLIGHTLY	552

Food For Thought About Field Programmable Gate Arrays.

Be Brilliant At In Productio

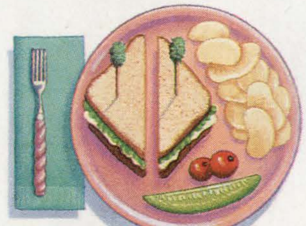


7:05 am : Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am : Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.

11:00 am : Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

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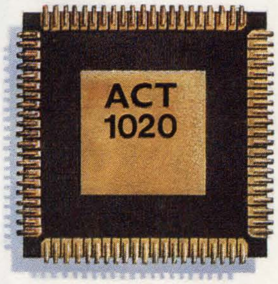
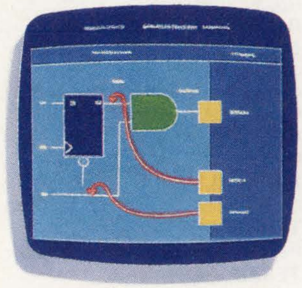
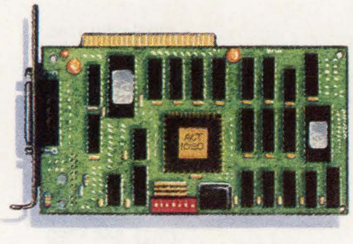
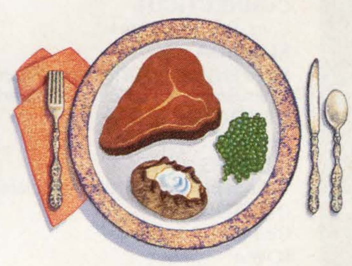
System Clock (MHz)		20-40	20-40
Availability		NOW	NOW
Technology (micron)		1.2	1.2

Breakfast And n By Dinner.









1:15 pm : Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a *very* quick coffee break while your design becomes a reality.

1:25 pm : Test
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4:00 pm : Production
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CIRCLE 99

PLD-BASED COPROCESSOR STABILIZES SERVO SYSTEM

DESIGNERS CAN OFFLOAD A SERVO SYSTEM'S MICROPROCESSOR BY ADDING A COPROCESSOR BASED ON PROGRAMMABLE LOGIC DEVICES.

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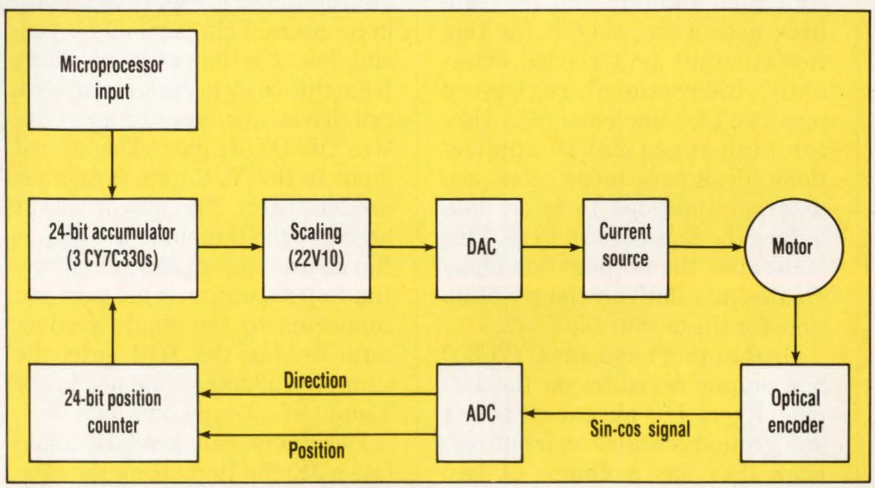
Keeping up with a servo control system can overload even a powerful processor. The problem is that a sampling rate of 8 to 10 times the highest frequency sampled may be needed to avoid aliasing or to increase stability, and at that rate the processor's bandwidth can be quickly exceeded. But designers can free up the processor and ensure a stable design by creating a servo "coprocessor" using programmable logic devices (PLDs).

The PLDs form a servo loop that functions as a coprocessor for the main CPU. Consequently, the CPU need not perform the control algorithm at a pace equal to the target sampling rate. Instead, all it has to do is merely input the desired reference point. Essentially, the processor can "set and forget" the servo coprocessor.

A good example is a laser-positioning system, in which an embedded 32-bit microprocessor orients a mirror to form images with a laser beam. As the microprocessor's tasks increase, its ability to maintain a stable servo system becomes marginal. Other servo applications that might have similar problems include: robotic assemblies, such as arms, camera mounts, etc.; aircraft control systems; printers, copiers, optical scanners, and plotters; and disk drives, VCRs, CD players, and turntables. The application described here was generalized from the real-world case of the laser-positioning system.

Designers can implement the coprocessor with several PLDs configured in a hybrid control loop. Using such third-generation devices as the CY7C330 simplifies design execution. Although engineers who have designed with 22V10s will be familiar with the general functionality of the CY7C330, the device has many other features that make it an ideal solution for this applica-



1. ADDING A HIGH-PRECISION accumulator to handle the feedback portion of a servo control system enables designers to take the host microprocessor out of the loop. Therefore, it doesn't have to run the control algorithm as fast as the target sampling rate.

tion *(see "A flexible PLD," below).*

In the example circuit, three PLDs are used to perform the loop's summing and proportional-feedback functions *(see "Closed-loop servo systems," p. 64).* The PLDs form an accumulator, with each device generating an 8-bit accumulate for 24 bits of precision *(Fig. 1).* The microprocessor simply provides the PLDs with a 24-bit position reference target, which is latched into the devices' on-board registers.

The desired position is compared to the present position, which is maintained in an external 24-bit present-position counter. The result of the comparison is the error signal, which is multiplied by a fixed unity gain. This proportional control signal is first converted to an analog signal and then to a current level so that it can control the positioning motor. The motor's shaft has an optical encoder that creates a sin-cos analog signal. When it's digitized, the signal indicates the direction of rotation and supplies a pulse that increments or decrements the present-position counter.

With this arrangement, the loop can operate as fast as the slowest of the following elements: the PLDs configured as a multistage accumulator/subtractor, the digital-to-analog converter (DAC), or the analog-to-digital converter. The host microprocessor is completely decoupled from the servo loop. Should the microprocessor halt, the servo circuitry will maintain the desired reference position without intervention.

Two Operating Modes

Essentially, the 7C330 macrocell output registers are programmed to act as an accumulator. Depending on the operation, the value generated by this accumulator represents one of two things: either a new servo-motor target position or the proportional-error feedback value to the servo. When the system starts, the macrocell input registers, which are dedicated to holding the motor's current target position, wake up with an initial value of zero.

At the same time, the external position counter is also set to zero. Then the microprocessor steps the target position until the laser targets an alignment sensor.

The first mode is the target-position update mode, which includes the following steps. First, the outputs of the external 24-bit position counter are placed into a three-state condition.

These outputs are shared with the microprocessor's outputs as inputs to the dedicated input registers. The processor then drives a step value onto the inputs, which is clocked into the 7C330's dedicated input registers with the CLK_1 pin *(Fig. 2).* On the rising edge of the CLK pin, the step value is added (from a set of PLD equations) to the current value in the ma-

A FLEXIBLE PLD

Although it's more flexible than simpler PLDs, the 22V10 does have limitations. The architecture of the CY7C330 addresses these shortcomings, increasing flexibility even further.

The 22V10 offers only D flip-flops, which are cumbersome for such applications as counters. And each flip-flop and its feedback uses a pin, even if the flip-flop's output isn't needed externally. Bidirectional, registered pins can't be implemented. Also, for high-speed 22V10 applications, designers must often use external flip-flops to latch data before the input of the PLD. This is because the propagation delay creates a relatively long set-up time for the output flip-flops.

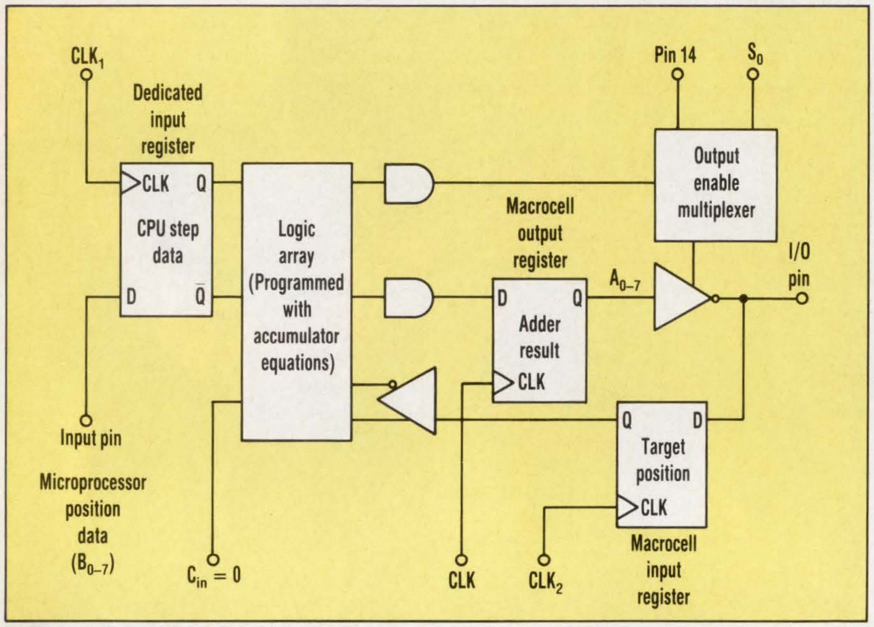
On the other hand, the CY7C330 has output registers on the I/O pins. Every I/O pin except power and ground contains an input register that has a choice of two clocks. In some applications, including up and down counters, three-stating the macrocell output drivers and loading data into the macrocell input register allows designers to use these macrocell input registers to hold reference values, such as the counter's upper or lower limit.

The CY7C330 also expands on the 22V10's functions by permitting designers to emulate T and JK flip-flops, a useful capability in counters. This capability is possible because the sum-of-products from the array in each I/O macrocell drives one input of an exclusive OR (XOR) gate. The second input to the XOR gate is another product term. The gate's output becomes the D input of the output flip-flop in the macrocell. If the flip-flop's Q output is fed back and connected to the single product term driving the XOR gate, the sum-of-products would act as the T input of a T-type flip-flop.

Designers can similarly emulate a JK flip-flop, using the relation T = J ! Q + KQ. The "!" symbol is an invert or NOT operator used in most PLD software packages. Of course, if a D flip-flop is all that's required, the XOR gate can be used to control polarity.

There are two paths into the CY7C330 array. The first is through a multiplexer that selects feedback from the register or the Q output of the input register. This is called the feedback multiplexer. The second path is through the shared-input multiplexer, whose inputs are the Q outputs of input registers belonging to adjacent I/O macrocells. This enables users to feed back the Q output of a macrocell's output register and still use the pin associated with that macrocell as an input. Of course, this can only be done with 6 of the device's 12 I/O macrocells.

If more registers are needed for an application, the CY7C330 has four additional buried (or hidden) registers. These are identical to the output register portion of the I/O macrocell, except they're not connected to any pin.



2. IN THE TARGET-POSITION update mode, the position data in the microprocessor is clocked into the dedicated input register with CLK$_1$ while the position counter's output is three-stated. On CLK$_2$, the new target position is loaded into the macrocell input register.

crocell input registers. The result of this addition, which is now in the macrocell output registers, is clocked with CLK$_2$ into the same macrocell input registers that were a source value for the add.

As a result, the 7C330s in this mode use the current value on the dedicated input pins to adjust the target position in the macrocell input registers with an accumulate cycle. Data from the microprocessor is always supplied as a delta or step from the current position. The accumulate can be either an add or subtract. The subtracts are done by supplying the step data from the microprocessor in two's-complement form. After alignment the system is then ready for operation.

When the coprocessor operates in the servo-control mode, the microprocessor outputs are three-stated and the value from the 24-bit position counter is loaded into the dedicated input registers *(Fig. 3)*. This value is always given in a two's-complement form by inverting the outputs of the position counter (one's complement) and setting carry-in, C_{in}, to one. Thus, the position counter data is subtracted from the present target-position value stored in the macrocell input registers. The resulting difference becomes the proportional-error feedback value that is used to control the servo motor.

In practice, the DAC doesn't need a 24-bit value for control. The actual design, therefore, uses an 8-bit value, with the 8th bit determining direction (clockwise versus counterclockwise).

The upper 16 bits from the two most significant PLDs are tested for

CLOSED-LOOP SERVO SYSTEMS

Closed-loop systems use information from the environment under control to influence the output. Designs can be purely analog or completely digital, but many popular versions use a hybrid of digital and analog techniques. The hybrid approach described in this article uses a digital element to perform the summing, control, and part of the feedback function.

The hybrid approach offers designers several ways to implement the controller—the part of the system that receives the error signal and generates an output signal aimed at reducing the error. Using a microprocessor, it's fairly easy to implement the controller and the summing function—the section that determines the size of the error—on-chip. A number of algorithms can be used to generate the control signal.

The simplest technique is proportional control, in which the correction is proportional to the error signal. The value that the error is scaled by is the proportionality constant or gain. Proportional control offers an intuitively reasonable solution: The larger the error, the larger the corrective signal.

Another method, integral control, bases the corrective signal on the time integral of the error multiplied by a weighting factor. This value is typically calculated with a numeric approximation. Systems usually combine integral control with proportional control to increase accuracy or reduce steady-state error.

Finally, derivative control involves multiplying the derivative of the error signal over time by a weighting factor. Again, a numeric approximation is used for the calculations. Adding this technique to proportional control stabilizes the system. However, it's often omitted in noisy systems because it tends to amplify high-frequency disturbances.

The three processes can be combined to create proportional-integral-derivative, or PID, control. The influences of the integral and derivative methods on PID are typically verified with analyses based on Laplace transforms. Using PID does reduce the processor bandwidth available to perform other tasks. Also, a finite amount of time is required to calculate the output value.

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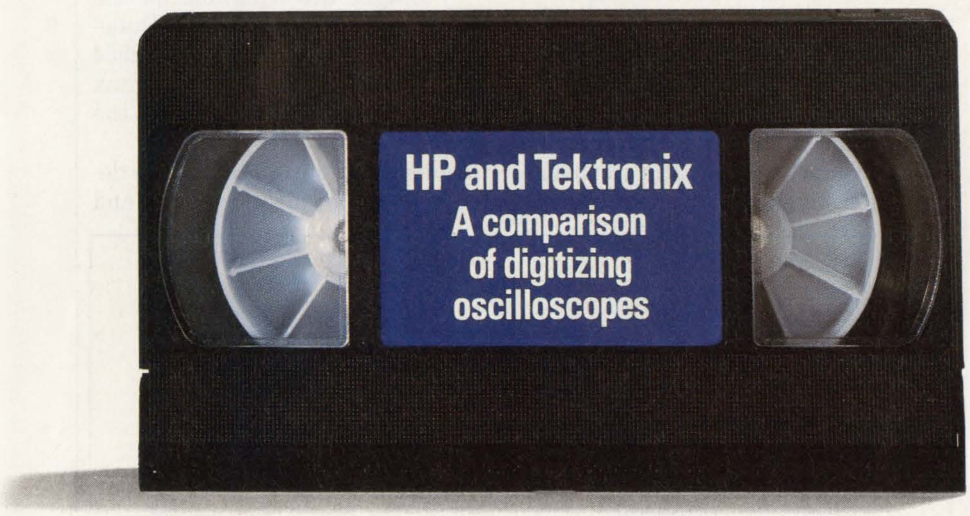

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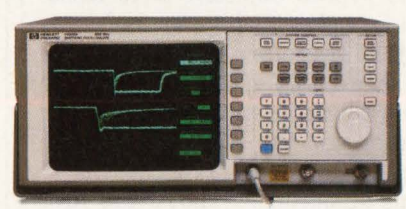

There is a better way.

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rail high and low conditions, and two off-scale bits are generated for each of these conditions. These four off-scale bits and the seven low-order bits are passed to another PLD (a 22V10) that drives the DAC *(Fig. 1, again)*.

If the four off-scale bits indicate that the upper bits are all close to zero, the seven low-order bits sent to the DAC are masked to zero. Likewise, if the upper bits are mostly ones, the DAC bits are set to one. This determination of how to use the off-scale bits for compensation in the scaling PLD is specific to a given application.

Logic Equations

The backbone of this design is the accumulator implemented in the PLDs. The logic required for a synchronous full adder is described by the equations for the sum and the carry of a given bit. In the general case,

$$S_n = (A_n \text{ XOR } B_n \text{ XOR } C_{n-1})$$

where S_n is the sum at bit position n with inputs A_n and B_n, and C_{n-1} is the carry in from the previous stage.

The equation for the carry out is:

$$C_{outn} = (A_n * B_n) + (A_n * C_{n-1}) + (B_n * C_{n-1}).$$

Several equations are involved when a 4-bit synchronous adder requires four clocks to complete *(see the table)*.

The Speed Objective

The overall objective is to calculate a complete 24-bit sum as fast as possible. Therefore, the equation for the carry out from the first bit of the adder (C_0) can be substituted into the equation for the second bit of the adder.

This substitution allows the first two bits to be added in one clock cycle. Likewise, the equation for the carry out from the second bit can be substituted into the equation for the third sum, and so on. The result is equations for three bits of substitution *(see the table, again)*.

ADDER EQUATIONS

General 4-bit adder

$S_0 = A_0 \text{ XOR } B_0 \text{ XOR } C_{in}$
$C_0 = (A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})$

$S_1 = A_1 \text{ XOR } B_1 \text{ XOR } C_0$
$C_1 = (A_1 * B_1) + (A_1 * C_0) + (B_1 * C_0)$

$S_2 = A_2 \text{ XOR } B_2 \text{ XOR } C_1$
$C_2 = (A_2 * B_2) + (A_2 * C_1) + (B_2 * C_1)$

$S_3 = A_3 \text{ XOR } B_3 \text{ XOR } C_2$
$C_3 = (A_3 * B_3) + (A_3 * C_2) + (B_3 * C_2)$

C_3 is the carry-out of the 4-bit adder.

Synchronous 3-bit adder

$S_0 = A_0 \text{ XOR } B_0 \text{ XOR } C_{in}$
$C_0 = (A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})$

$S_1 = A_1 \text{ XOR } B_1 \text{ XOR } [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})]$
$C_1 = (A_1 * B_1) + (A_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})]) + (B_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})])$

$S_2 = A_2 \text{ XOR } B_2 \text{ XOR } \{(A_1 * B_1) + (A_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})]) + (B_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})])\}$
$C_2 = (A_2 * B_2) + (A_2 * \{(A_1 * B_1) + (A_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})]) + (B_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})])\}) + (B_2 * \{(A_1 * B_1) + (A_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})]) + (B_1 * [(A_0 * B_0) + (A_0 * C_{in}) + (B_0 * C_{in})])\}$

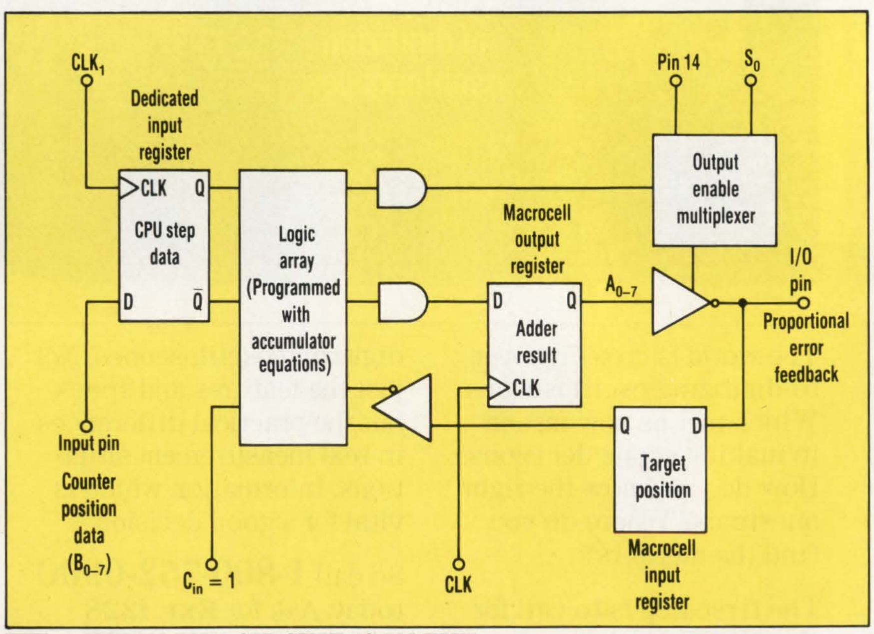
Note: The equations use substitution of the carry-out in the first 3 bits to generate a 3-bit result in one clock cycle.
A_n and B_n are inputs to be added at bit n; C_{in} is the carry-in to the adder.
S_n is the sum out for bit n and C_n is the carry-out from adder stage n.

Although the 7C330's XOR product term helps reduce the number of product terms required for a given sum bit, the equations for the fourth bit are complex. Even after Boolean reduction, the adder's fourth bit requires 30 product terms for the sum bit and 31 product terms for the carry-out bit to generate a 4-bit result in one clock cycle.

Because the maximum number of product terms for a given macrocell in the 7C330 is 19, the accumulate process must be accomplished over multiple 3-bit stages. Adding the first three bits will be complete after one clock cycle, the second three bits after two cycles, and so on. Therefore, the complete 24-bit accumulate requires nine clock cycles implemented on three 7C330s. With 66-MHz devices, this translates to a complete 24-bit calculation cycle in 120 ns.

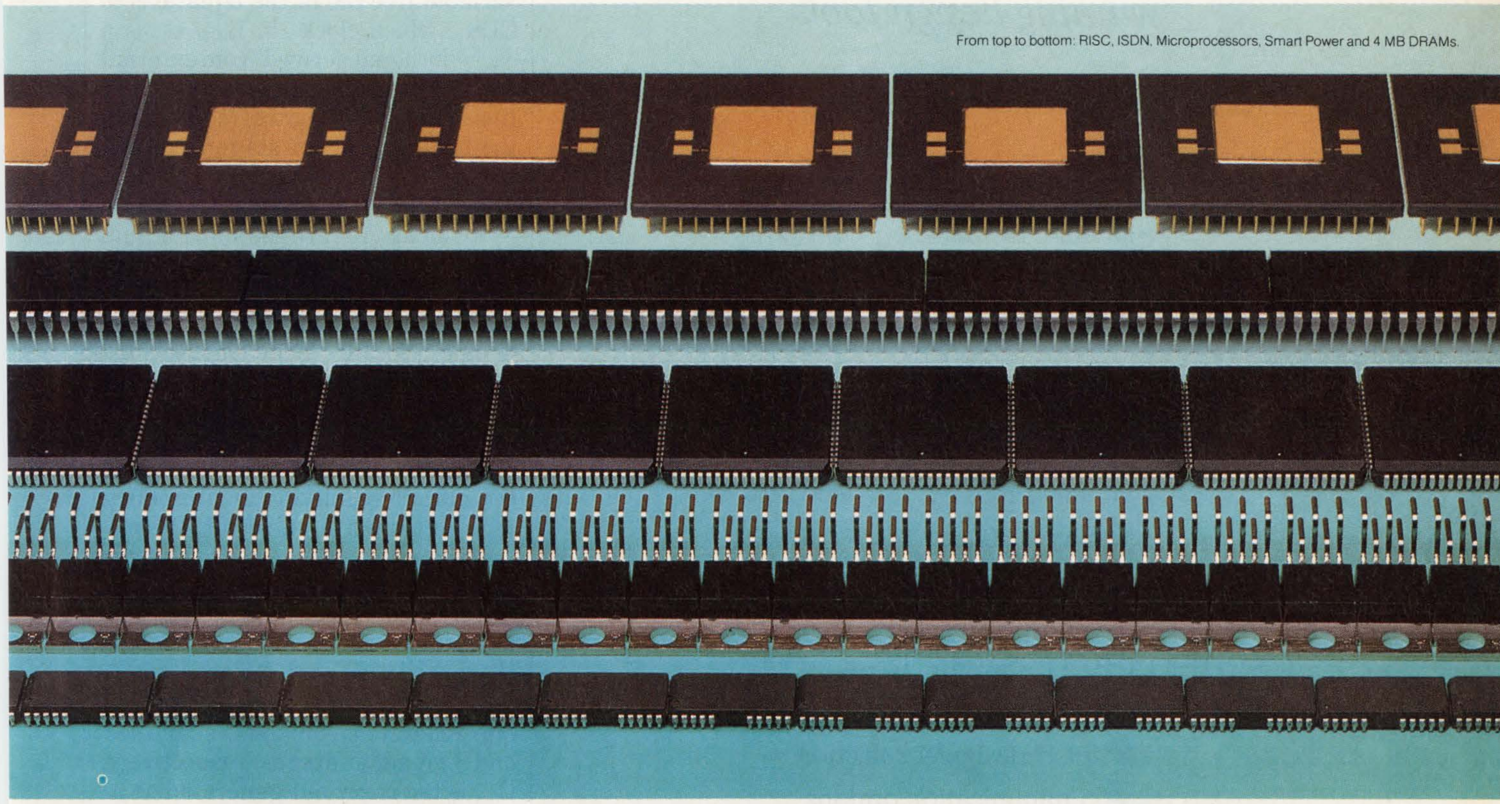
The minimized equations for the three 8-bit adder stages are available on the Cypress Applications Bulletin Board System, (408) 943-2954 (1200/2400 bps, 8-N-1). The syntax used for the equations is from the Cypress PLD Toolkit.

The terms in the equations are derived from the target-update and



3. WHEN THE CIRCUIT IS IN THE control mode, the dedicated input register receives position data from the external position counter. With the carry-in (C_1) now set to one, the logic equations subtract the current position from the target position, creating an error value.

SIEMENS



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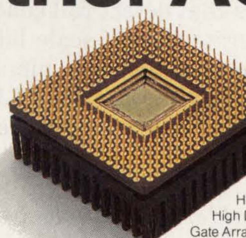

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DESIGN APPLICATIONS

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control-mode schematics. For example, variables B_{0-7} are the inputs to the CY7C330 from either the microprocessor or the current position counter *(Figs. 2 and 3, again)*. The variable INCLK in the equations is CLK_1, which clocks in B_{0-7}. C_{in} is a carry-in signal derived from external logic or from the previous stage of the adder (in the control mode, when the first 8-bit adder stage is set for subtraction, the external logic must assert C_{in}).

Variables A_{0-7} are the sum outputs for either the target update or control mode. If the processor is updating the target position by a step increment, A_{0-7} are loaded into the macrocell input registers with CLK_2 (ACLK in the equations). During the update process, the macrocells' output drivers aren't three-stated with the output-enable pin or a product-term equation. As a result, the macrocell output registers, which have the newly calculated target position, can be loaded into the macrocell input registers that are used to hold the target position.

C_2 and C_5 are internal carry-out bits generated from the first and second 3-bit adder stages, respectively. C_{out} is the carry-out generated as either the final carry-out or as the input to the carry-in of the next 8-bit adder stage.

The equations for the two upper stages are the same as those for the first stage, except for the addition of equations that detect rail conditions and generate the off-scale bits. Using these bits, which minimize the number of inputs for the PLD that feeds the DAC, depends on the application.□

Mark Aaldering, a field applications engineer responsible for supporting Cypress Semiconductor customers in the Northwest US and Canada, received a BS in engineering from California State University at Northridge.

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WHEN DESIGNING STATE MACHINES, A TECHNIQUE CALLED ONE-HOT ENCODING CREATES EFFICIENT CIRCUITS FOR TOP-PERFORMING FPGA MACROS.

ACCELERATE FPGA MACROS WITH ONE-HOT APPROACH

State machines—one of the most commonly implemented functions with programmable logic—are employed in various digital applications, particularly controllers. However, the limited number of flip-flops and the wide combinatorial logic of a PAL device favors state machines that are based on a highly encoded state sequence. For example, each state within a 16-state machine would be encoded using four flip-flops as the binary values between 0000 and 1111.

A more flexible scheme—called one-hot encoding (OHE)—employs one flip-flop per state for building state machines. Although it can be used with PAL-type programmable-logic devices (PLDs), OHE is better suited for use with the fan-in limited and flip-flop-rich architectures of the higher-gate-count field-programmable gate arrays (FPGAs), such as offered by Xilinx, Actel, and others. This is because OHE requires a larger number of flip-flops. It offers a simple and easy-to-use method of generating performance-optimized state-machine designs because there are few levels of logic between flip-flops.

A state machine implemented with a highly encoded state sequence will

STEVEN K. KNAPP
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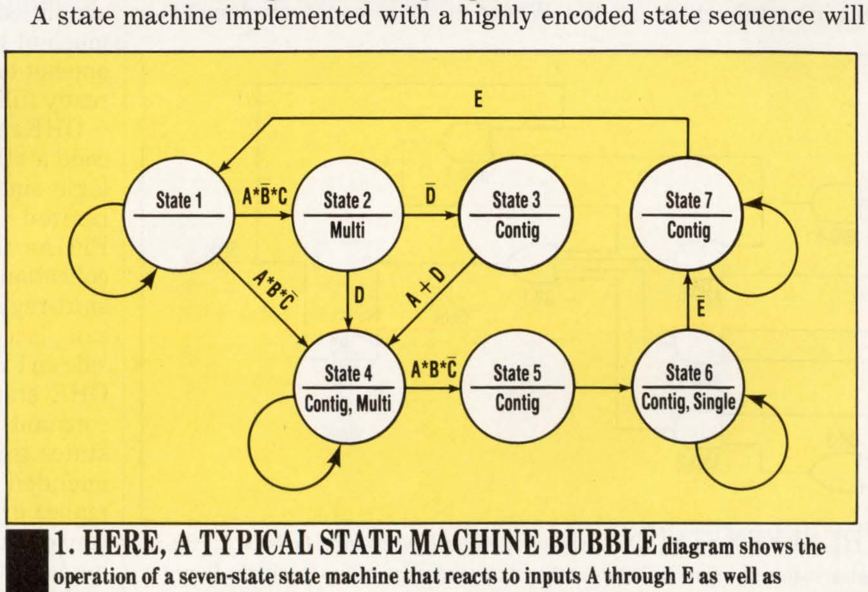
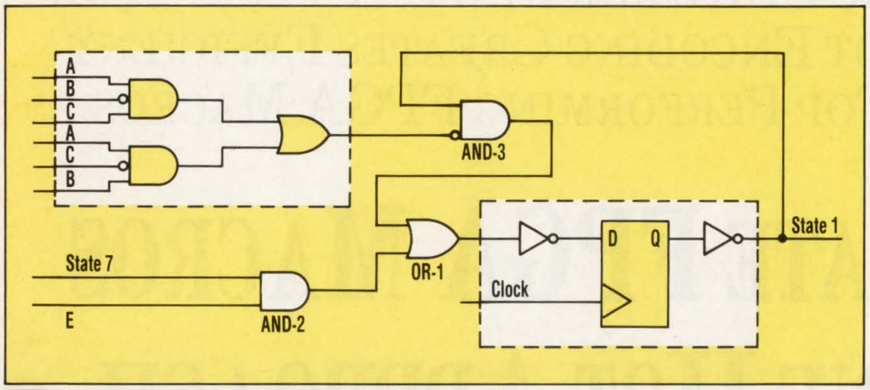


1. HERE, A TYPICAL STATE MACHINE BUBBLE diagram shows the operation of a seven-state state machine that reacts to inputs A through E as well as previous-state conditions.



2. INVERTERS ARE REQUIRED at the D input and the Q output of the state flip-flop to ensure that it powers on in the proper state. Combinatorial logic decodes the operations based on the input conditions and the state feedback signals. The flip-flop will remain in State 1 as long as the conditional paths out of the state are not valid.

generally have many, wide-input logic functions to interpret the inputs and decode the states. Furthermore, incorporating a highly encoded state machine in an FPGA requires several levels of logic between clock edges because multiple logic blocks will be needed for decoding the states. A better way to implement state machines in FPGAs is to match the state-machine architecture to the device architecture.

Limiting Fan-In

A good state-machine approach for FPGAs limits the amount of fan-in into one logic block. While the one-hot method is best for most FPGA applications, binary encoding is still more efficient in certain cases, such as for small state machines. It's up to the designer to evaluate all approaches before settling on one for a particular application.

FPGAs are high-density programmable chips that contain a large array of user-configurable logic blocks surrounded by user-programmable interconnects. Generally, the logic blocks in an FPGA have a limited number of inputs. The logic block in the Xilinx XC-3000 series, for instance, can implement any function of five or less inputs. In contrast, a PAL macrocell is fed by each input to the chip and all of the flip-flops. This difference in logic structure between PALs and FPGAs is important for functions with many inputs: Where a PAL could implement a many-input logic function in one level of logic, an FPGA might require multiple logic layers due to the limited number of inputs.

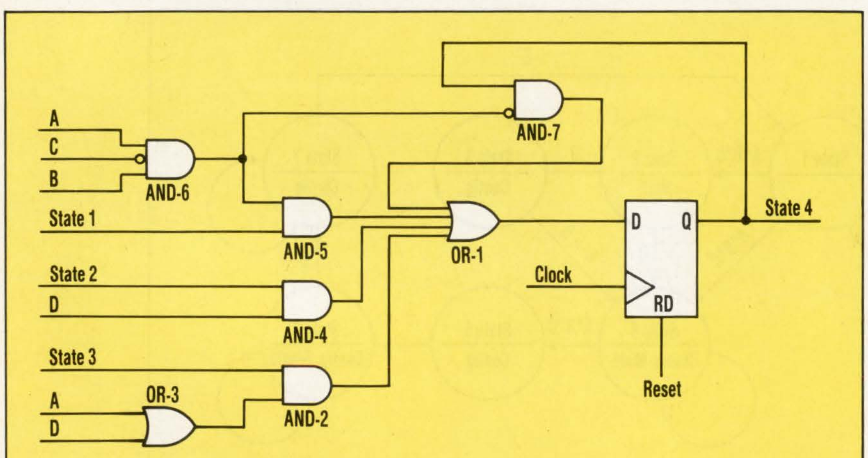
The OHE scheme is named so because only one state flip-flop is asserted, or "hot," at a time. Using the one-hot-encoding method for FPGAs was originally conceived by HighGate Design—a Saratoga, Calif.-based consulting firm specializing in FPGA designs.

The OHE state machine's basic structure is simple—first assign an individual flip-flop to each state, and then permit only one state to be active at any time. A state machine with 16 states would require 16 flip-flops using the OHE approach; a highly encoded state machine would need just 4 flip-flops. At first glance, OHE may seem counter-intuitive. For designers accustomed to using PLDs, more flip-flops typically indicates either using a larger PLD or even multiple devices.

In an FPGA, however, OHE yields a state machine that generally requires fewer resources and has higher performance than a binary-encoded implementation. OHE has definite advantages for FPGA designs because it exploits the strengths of the FPGA architecture. It usually requires two or less levels of logic between clock edges than binary encoding. That translates into faster operation. Logic circuits are also simplified because OHE removes much of the state-decoding logic—a one-hot-encoded state machine is already fully decoded.

OHE requires only one input to decode a state, making the next-state logic simple and well-suited to the limited fan-in architecture of FPGAs. In addition, the resulting collection of flip-flops is similar to a shift-register-like structure, which can placed and routed efficiently inside an FPGA device. The speed of an OHE state machine remains fairly constant even as the number of states grows. In contrast, a highly encoded state machine's performance drops as the states grow because of the wider and deeper decoding logic that's required.

To build the next-state logic for



3. OF THE SEVEN STATES, the state-transition logic required for State 4 is the most complex, requiring inputs from three other state outputs as well as four of the five condition signals (A - D).

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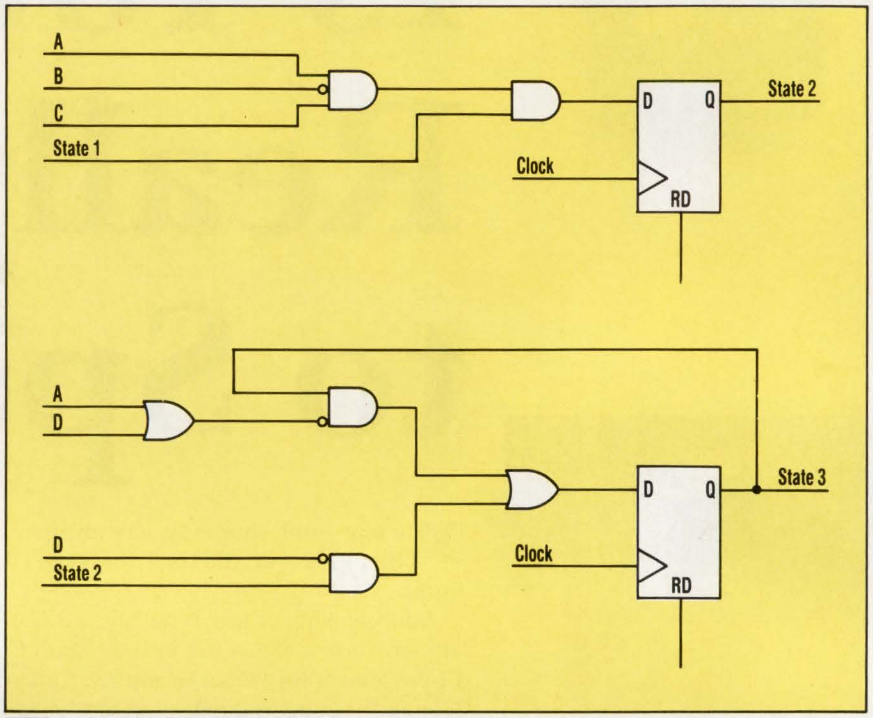
OHE state machines is simple, lending itself to a "cookbook" approach. At first glance, designers familiar with PAL-type devices may be concerned by the number of potential illegal states due to the sparse state encoding. This issue, to be discussed later, can be solved easily.

A typical, simple state machine might contain seven distinct states that can be described with the commonly used circle-and-arc bubble diagrams *(Fig. 1)*. The label above the line in each "bubble" is the state's name, the labels below the line are the outputs asserted while the state is active. In the example, there are seven states labeled State 1-7. The "arcs" that feed back into the same state are the default paths. These will be true only if no other conditional paths are true.

Each conditional path is labeled with the appropriate logical condition that must exist before moving to the next state. All of the logic inputs are labeled as variables A through E. The outputs from the state machine are called Single, Multi, and Contig. For this example, State 1, which must be asserted at power-on, has a doubly-inverted flip-flop structure *(shaded region of Fig. 2)*.

The state machine in the example was built twice, once using OHE and again with the highly encoded approach employed in most PAL designs. A Xilinx XC3020-100 2000-gate FPGA was the target for both implementations. Though the OHE circuit required slightly more logic than the highly-encoded state machine, the one-hot state machine operated 17% faster *(see the table)*. Intuitively, the one-hot method might seem to employ many more logic blocks than the highly encoded approach. But the highly encoded state machine needs more combinatorial logic to decode the encoded state values.



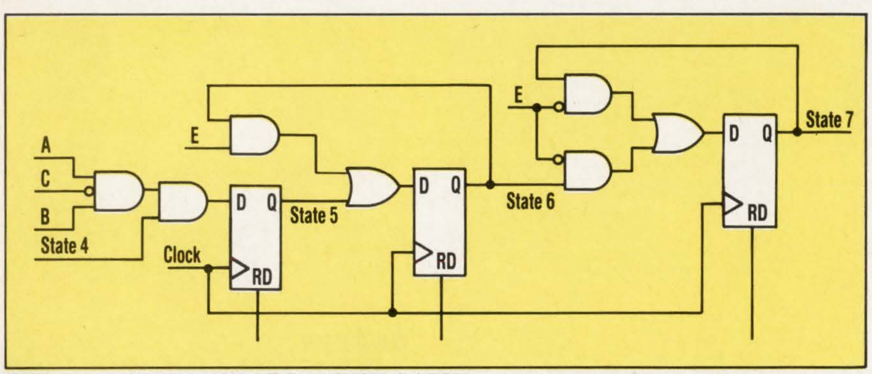
4. ONLY A FEW GATES are required by States 2 and 3 to form simple state-transition logic decoding. Just two gates are needed by State 2 (top), while four simple gates are used by State 3 (bottom).

The OHE approach produces a state machine with a shift-register structure that almost always outperforms a highly encoded state machine in FPGAs. The one-state design had only two layers of logic between flip-flops, while the highly encoded design had three. For other applications, the results can be far more dramatic. In many cases, the one-hot method yields a state machine with one layer of logic between clock edges. With one layer of logic, a one-hot state machine can operate at 50 to 60 MHz.

The initial or power-on condition in a state machine must be examined carefully. At power-on, a state machine should always enter an initial, known state. For the Xilinx FPGA family, all flip-flops are reset at power-on automatically. To assert an initial state at power-on, the output from the initial-state flip-flop is inverted. To maintain logical consistency, the input to flip-flop also is inverted.

All other states use a standard, D-type flip-flop with an asynchronous reset input. The purpose of the asynchronous reset input will be discussed later when illegal states are covered.

Once the start-up conditions are set up, the next-state transition logic can be configured. To do that, first examine an individual state. Then



5. LOOKING NEARLY THE SAME as a simple shift register, the logic for States 5, 6, and 7 is very simple. This is because the OHE scheme eliminates almost all decoding logic that precedes each flip-flop.

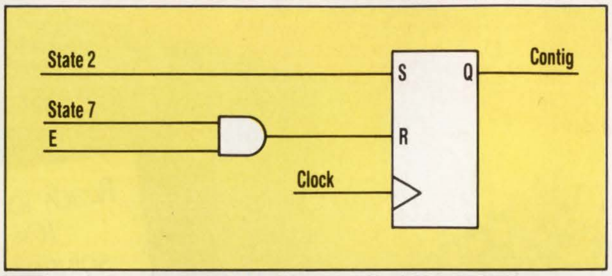
count the number of conditional paths leading into the state and add an extra path if the default condition is to remain in the same state. Second, build an OR-gate with the number of inputs equal to the number of conditional paths that were determined in the first step.

Third, for each input of the OR-gate, build an AND-gate of the previous state and its conditional logic. Finally, if the default should remain in the same state, build an AND-gate of the present state and the inverse of *all* possible conditional paths leaving the present state.

To determine the number of conditional paths feeding State 1, examine the state diagram—State 1 has one path from State 7 whenever the variable E is true. Another path is the default condition, which stays in State 1. As a result, there are two conditional paths feeding State 1. Next, build a 2-input OR-gate—one input for the conditional path from State 7, the other for the default path to stay in State 1 *(shown as OR-1 in Fig. 2)*.

The next step is to build the conditional logic feeding the OR-gate. Each input into the OR-gate is the logical AND of the previous state and its conditional logic feeding into State 1. State 7, for example, feeds State 1 whenever E is true and is implemented using the gate called AND-2 *(Fig. 2, again)*. The second input into the OR-gate is the default transition that's to remain in State 1. In other words, if the current state is State 1, and no conditional paths leaving State 1 are valid, then the state machine should remain in State 1. Note in the state diagram that two conditional paths are leaving State 1 *(Fig. 1, again)*.

The first path is valid whenever ($A*\overline{B}*C$) is true, which leads into State 2. The second path is valid whenever ($A*B*\overline{C}$) is true, leading into State 4. To build the default logic, State 1 is ANDed with the inverse of all of the conditional paths leaving State 1. The logic to perform this function is implemented in the gate labeled AND-3 and the logic elements that feed into the inverting input of AND-3 *(Fig. 2, again)*.



6. S-R FLIP-FLOPS OFFER ANOTHER approach to decoding the Contig output. They can also save logic blocks, especially when an output is asserted for a long sequence of contiguous states.

State 4 is the most complex state in the state-machine example. However, creating the logic for its next-state control follows the same basic method as described earlier. To begin with, State 4 isn't the initial state, so it uses a normal D-type flip-flop without the inverters. It does, however, have an asynchronous reset input, three paths into the state, and a default condition that stays in State 4. Therefore, a four-input OR-gate feeds the flip-flop *(OR-1 in Fig. 3)*.

The first conditional path comes from State 3. Following the methods established earlier, an AND of State 3 and the conditional logic, which is A ORed with D, must be implemented *(AND-2 and OR-3 in Fig. 3)*. The next conditional path is from State 2, which requires an AND of State 2 and variable D *(AND-4 in Fig. 3)*. Lastly, the final conditional path leading into State 4 is from State 1. Again, the State-1 output must be ANDed with its conditional path logic—the logical product, $A*B*\overline{C}$ *(AND-5 and AND-6 in Fig. 3)*.

Now, all that must be done is to build the logic that remains in State 4 when none of the conditional paths away from State 4 are true. The path leading away from State 4 is valid whenever the product, $A*B*\overline{C}$, is true. Consequently, State 4 must be ANDed with the inverse of the product, $A*B*\overline{C}$. In other words, "keep loading the flip-flop with a high until a valid transfer to the next state occurs." The default path logic uses AND-7 and shares the output of AND-6.

Configuring the logic to handle the remaining states is very simple. State 2, for example, has only one conditional path, which comes from State 1 whenever the product $A*\overline{B}*C$ is true. However, the state machine will immediately branch in one of two ways from State 2, depending on the value of D. There's no default logic to remain in State 2 *(Fig. 4, top)*. State 3, like States 1 and 4, has a default state, and combines the A, D, State 2, and State-3 feedback to control the flip-flop's D input *(Fig. 4, bottom)*.

State 5 feeds State 6 unconditionally. Note that the state machine waits until variable E is low in State 6 before proceeding to State 7. Again, while in State 7, the state machine waits for variable E to return to true before moving to State 1 *(Fig. 5)*.

Output Definitions

After defining all of the state transition logic, the next step is to define the output logic. The three output signals—Single, Multi, and Contig—each fall into one of three primary output types:

1. Outputs asserted during one state, which is the simplest case. The output signal Single, asserted only during State 6, is an example.

2. Outputs asserted during multiple, contiguous states. This appears simple at first glance, but a few techniques exist that reduce logic complexity. One example is Contig. It's asserted from State 3 to State 7, even though there's a branch at State 2.

3. Outputs asserted during multiple, non-contiguous states. The best solution is usually brute-force decoding of the active states. One

ONE-STATE VS. BINARY ENCODING METHODS

Method	Number of logic blocks	Worst-case performance
One-hot	7.5	40 MHz
Binary encoding	7.0	34 MHz

such example is Multi, which is asserted during State 2 and State 4.

OHE makes defining outputs easy. In many cases, the state flip-flop is the output. For example, the Single output also is the flip-flop output for State 6; no additional logic is required. The Contig output is asserted throughout States 3 through 7. Though the paths between these states may vary, the state machine will always traverse from State 2 to a point where Contig is active in either State 3 or State 4.

There are many ways to implement the output logic for the Contig output. The easiest method is to decode States 3, 4, 5, 6, and 7 with a 5-input OR gate. Any time the state machine is in one of these states, Contig will be active. Simple decoding works best for this state machine example. Decoding five states won't exceed the input capability of the FPGA logic block.

Additional Logic

However, when an output must be asserted over a longer sequence of states (six or more), additional layers of decoding logic would be required. Those additional logic layers reduce the state machine's performance.

Employing S-R flip-flops gives designers another option when decoding outputs over multiple, contiguous states. Though the basic FPGA architecture may not have physical S-R flip-flops, most macrocell libraries contain one built from logic and D-type flip-flops. Using S-R flip-flops is especially valuable when an output is active for six or more contiguous states.

The S-R flip-flop is set when entering the contiguous states, and reset when leaving. It usually requires extra logic to look at the state just prior to the beginning and ending state. This approach is handy when an output covers multiple, non-contiguous states, assuming there are enough logic savings to justify its use.

In the example, States 3 through 7 can be considered contiguous. Contig is set after leaving State 2 for either States 3 or 4, and is reset after leaving State 7 for State 1. There are no conditional jumps to states where Contig isn't asserted as it traverses from State 3 or 4 to State 7. Otherwise, these states would not be contiguous for the Contig output.

The Contig output logic, built from an S-R flip-flop, will be set with State 2 and reset when leaving State 7 *(Fig. 6)*. As an added benefit, the Contig output is synchronized to the master clock. Obvious logic reduction techniques shouldn't be overlooked either. For example, the Contig output is active in all states except for States 1 and 2. Decoding the states where Contig isn't true, and then asserting the inverse, is another way to specify Contig.

The Multi output is asserted during multiple, non-contiguous states—exclusively during States 2 and 4. Though States 2 and 4 are contiguous in some cases, the state machine may traverse from State 2 to State 4 via State 3, where the Multi output is unasserted. Simple decoding of the active states is generally best for non-contiguous states. If the output is active during multiple, non-contiguous states over long sequences, the S-R flip-flop approach described earlier may be useful.

One common issue in state-machine construction deals with preventing illegal states from corrupting system operation. Illegal states exist in areas where the state machine's functionality is undefined or invalid. For state machines implemented in PAL devices, the state-machine compiler software usually generates logic to prevent or to recover from illegal conditions.

In the OHE approach, an illegal condition will occur whenever two or more states are active simultaneously. By definition, the one-hot method makes it possible for the state machine to be in only one state at a time. The logic must either prevent multiple, simultaneous states or avoid the situation entirely.

Synchronizing all of the state-machine inputs to the master clock signal is one way to prevent illegal states. "Strange" transitions won't occur when an asynchronous input changes too closely to a clock edge. Though extra synchronization would be costly in PAL devices, the flip-flop-rich architecture of an FPGA is ideal.

Even off-chip inputs can be synchronized in the available input flip-flops. And internal signals can be synchronized using the logic block's flip-flops (in the case of the Xilinx LCAs). The extra synchronization logic is free, especially in the Xilinx FPGA family where every block has an optional flip-flop in the logic path.

Resetting State Bits

Resetting the state machine to a legal state, either periodically or when an illegal state is detected, gives designers yet another choice. The Reset Direct (RD) inputs to the flip-flops are useful in this case. Because only one state bit should be set at any time, the output of a state can reset other state bits. For example, State 4 can reset State 3.

If the state machine did fall into an illegal condition, eventually State 4 would be asserted, clearing State 3. However, State 4 can't be used to reset State 5, otherwise the state machine won't operate correctly. To be specific, it will never transfer to State 5; it will always be held reset by State 4. Likewise, State 3 can reset State 2, State 5 can reset State 4, etc.—as long as one state doesn't reset a state that it feeds.

This technique guarantees a periodic, valid condition for the state machine with little additional overhead. Notice, however, that State 1 is never reset. If State 1 were "reset," it would force the output of State 1 high, causing two states to be active simultaneously (which, by definition, is illegal).□

Steve Knapp, new product development manager at Xilinx, spent the last four years as a field applications engineer aiding customers in FPGA designs. He received a BS in materials science and engineering from Massachusetts Institute of Technology, Cambridge, Mass.

How Valuable?	Circle
Highly	544
Moderately	545
Slightly	546

SEPTEMBER 1990

NEWS

ABOUT
1553 DATA BUS
SYNCHRO CONVERSION
A/D & D/A CONVERSION
POWER & MEMORY HYBRIDS

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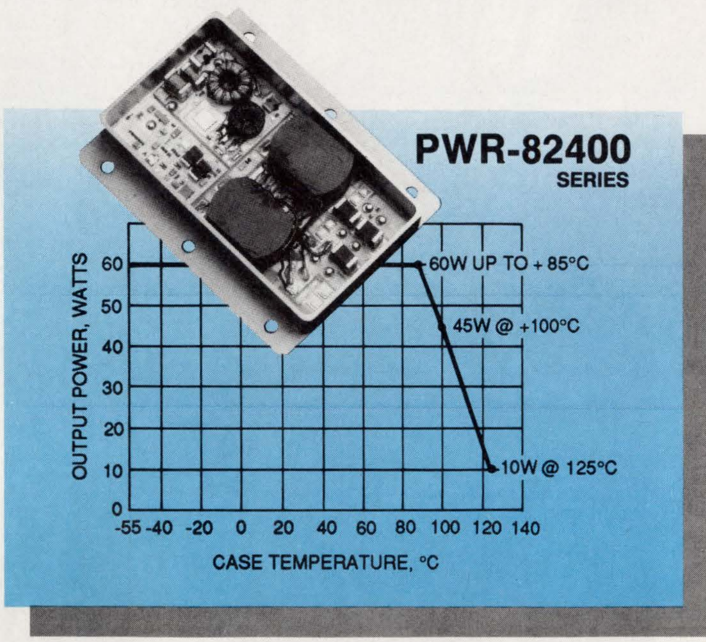
DC - DC CONVERTERS OPERATE OVER MIL TEMP RANGE



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For additional information contact Bob Fryer at 516/563-5390, or call toll-free 1-800-DDC-1772 (outside New York). □

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CIRCLE 130 FOR CONTACT

CIRCLE 131 FOR LITERATURE

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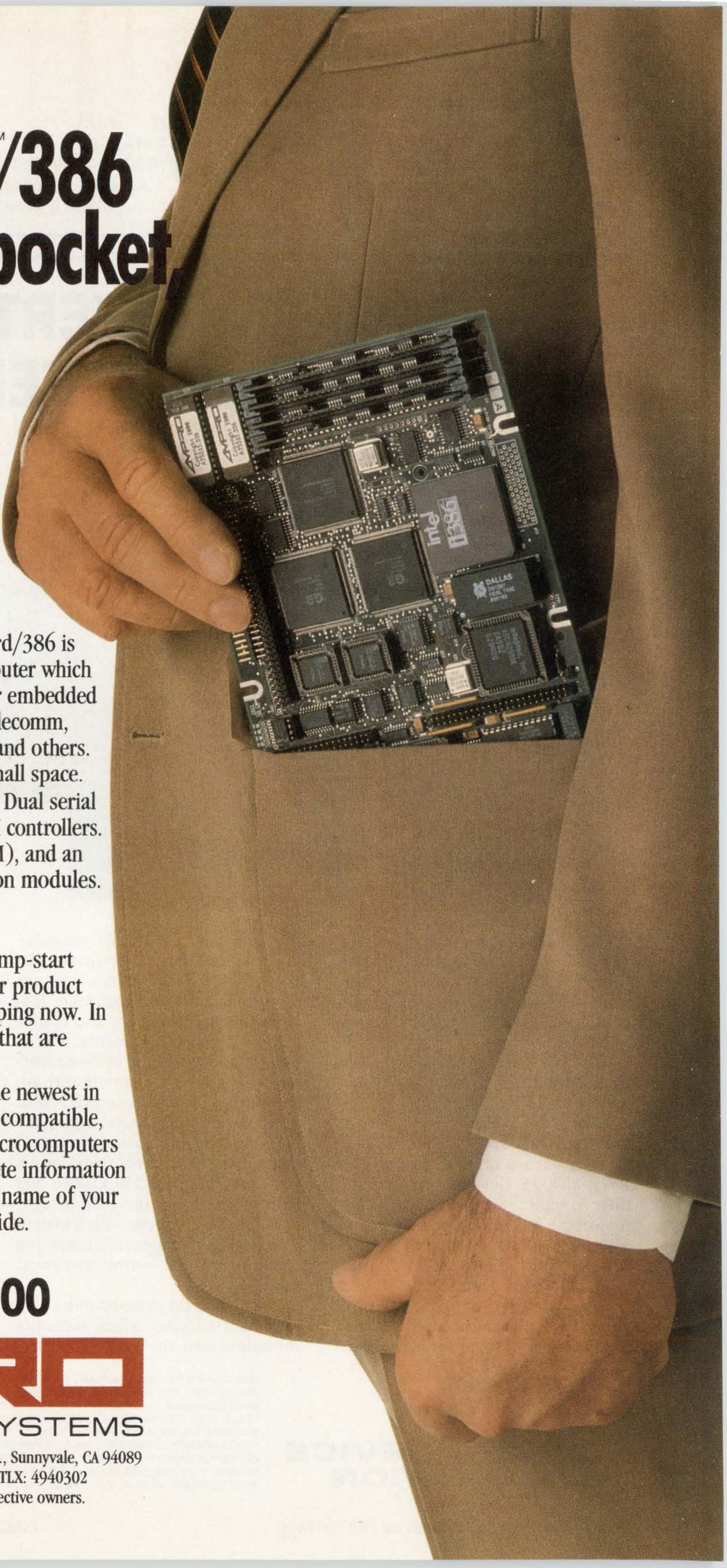

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CIRCLE 155

BEST SELLERS

Which technical books are the most popular in Silicon Valley?

ELECTRONICS:

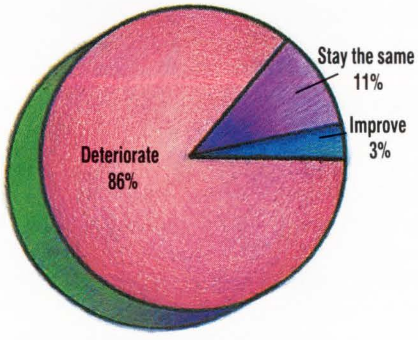
1. *SPICE: A Guide to Circuit Simulation and Analysis Using PSPICE.* Paul Tuinenga. Prentice-Hall, 1988. ***$21.***
2. *Noise Reduction Techniques in Electronic Systems*, 2nd ed. Henry W. Oh. Wiley, 1988. ***$42.95.***
3. *Microelectronics Packaging Handbook.* Rao R. Tummala and Eugene Rymaszewski. Van Nostrand-Reinhold, 1989. ***$94.95***
4. *Logic Design Principles.* Edward McClusky. Prentice-Hall, 1986. ***$58.60.***
5. *Art of Electronics.* Paul Horowitz and Winifred Hill. Cambridge University Press, 1989. ***$49.50.***

COMPUTER SCIENCE:

1. *Object-oriented Analysis.* Peter Coad and Edward Yourdan. Prentice-Hall, 1990. ***$29.80.***
2. *Object-oriented Design with Applications.* Grady Booch. Addison-Wesley, 1990. ***$37.25.***
3. *Envisioning Information.* Edward R. Tufte. Graphics Press, 1990. ***$48.***
4. *Computer Architecture: A Quantitative Approach.* John L. Hennessy and David A. Paterson. Morgan Kaufman, 1990. ***$54.95.***
5. *A Practical Guide to Structured Systems Design*, 2nd ed. Meilir Page-Jones, Prentice-Hall, 1988. ***$39.***

This list is compiled for *Electronic Design* by Stacey's Bookstore, 219 University Ave., Palo Alto, CA 94301; (415) 326-0681; fax (415) 326-0693.

HOW WOULD A COMPANY TAKEOVER OR BUYOUT AFFECT YOUR JOB STABILITY, PENSION, AND BENEFITS?



Source: 1990 IEEE Member Opinion Survey

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
Cupertino, Calif.; (408) 446-4458

Defining a project or program can be confusing and difficult. For one thing, many questions need to be answered before the definition can be produced. Generating acceptable responses is time-consuming and requires collecting input from many sources. For another, information from one source often conflicts with that produced by another. Privately held assumptions made by one group regularly cloud and stall the overall effort.

The product definition team must answer the same questions associated with making a decision to do just about anything. Why are we doing this? How will we do it? Who will do it? Just what, exactly, are we going to do? When do we need to complete the job? How much money do we have to spend? The list goes on . . .

Two extreme approaches can be followed to produce answers to the long, but finite, list. The first approach is to dive straight in with little or no information and figure things out as you go. Excessive analysis and analytic justification lie at the opposite end of the spectrum. With the first approach, the project starts quickly, but, because the definition changes with each new discovery, it is likely to finish outside the market window. The second approach is equally undesirable and produces nearly the same results; that is, the project never finishes because it never starts. For most projects, the right answer lies somewhere between the two poles. How do you go about determining the right balance for a given project or program? Clearly, a means is needed to guide the generation of a product's definition while being able to evaluate its quality and applicability to the work environment.

Before looking at generation methods, I'll give some insights on how you can go about evaluating the quality of a product's definition. When a product definition is weak, one of the responses emanating from R&D may be: "We're building this thing to be a top performer using only the latest in new technology. Its appearance is unlike anything you've ever seen before. Performance is a much higher priority than cost. Of course, we'll have it done within the next six months. But we can't get a sales forecast out of marketing, and manufacturing seems too busy dealing with today's shipments to even care about this effort." Marketing folks say, "Those wizards in the lab are brilliant, but we can't seem to get out of them what they are really doing. Try to talk to a customer about something you don't understand and see how far you get!" From manufacturing you might hear; "The last time we got involved good things happened, but then the war effort terminated and no one has been around since." Comments of this type lead to asking some probing questions of the cross-functional team and their managers:

- Does the product's definition fit your company's long-term vision of itself?
- Do you have some information to suggest that a market exists for the product?
- Does what you are about to do fit within your company's business plan?
- What is the product's classification (first-of-a-kind, me-too-with-a-twist, and so on)?
- What is the product's internal purpose?
- What is the product's external purpose?
- Do you have sample promotion material available to help others better understand the product?
- What are the necessary performance, feature, cost, prices, and time-to-market parameters?
- What does the user interface look like and how does it work?
- How do the financial numbers look?
- What do the people in other management positions and other functions think?

A quality business definition must be in place before a quality product definition can be produced. Understanding the meaning of the questions is the first test of definition quality from both perspectives. When definitions change, expenditures rise, time to market extends, frustrations ignite, and apathy spreads. In the next column, I'll begin exploring how to generate a definition from business and product perspectives.

QUICKLOOK

OFFERS YOU CAN'T REFUSE

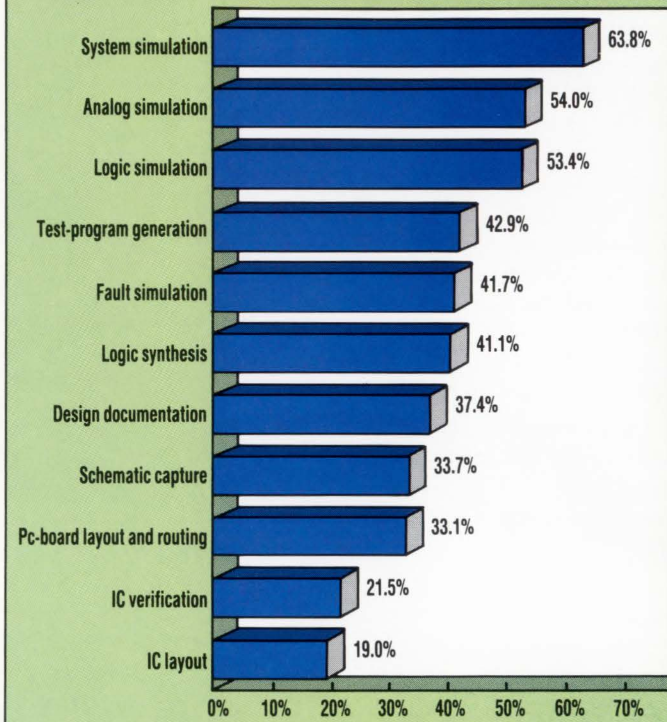
Like many areas in electronics, networking is rife with buzzwords and acronyms. To translate such abbreviations as QLLC (qualified logical link control), Racal-Milgo offers a free, 82-page *Networking Dictionary*. The dictionary defines 1200 networking terms, from ABAM (a Western Electric twisted-pair cable) to zero code suppression. For a copy of the dictionary, contact Racal-Milgo, 1601 N. Harrison Pkwy., Sunrise, FL 33323-2899; (305) 846-1601.

Calculating optical loss in fiber-optic testing can be confusing—measuring optical loss requires subtracting power transmitted from power launched. To simplify matters, Fotec has an optical loss calculator, a circular slide rule calibrated in dBm. An engineer sets the launched power in a window on the front of the calculator and reads the optical loss on the outer scale opposite the receiver power. The P600 converts from dBm to milliwatts, microwatts, and nanowatts, for those working in linear units. The calculator, which sells for $5, is available from Fotec Inc., 529 Main St., Box 246, Boston, MA 02129; (800) 537-8254.

Engineers working with power distribution may find a pocket handbook useful. Rochester Instrument Systems' *Power Distribution Handbook* is a quick reference tool that contains tables, conversion factors, device function numbers, and definitions. The free handbook also has information on the company's new fault monitor, which warns of deteriorating electrical insulation to ground without equipment shutdown. For a copy, contact Kathy Nacy at Rochester Instrument Systems, 255 North Union St., Rochester, NY 14605; (716) 238-4950.

CAE SURVEY

IF YOU HAD BETTER CAE/CAD TOOLS, WHICH FUNCTIONS WOULD YOU DO MORE OFTEN?



Source: A survey of Electronic Design readers conducted by the Adams Co., Palo Alto, Calif.

WHAT'S HAPPENING IN . . . ORLANDO

While tourism employs the most workers in Orlando, high-tech runs a close second. And Orlando's roster of electronics companies is growing. In the past 10 years, employment in Central Florida's high-tech sector soared 114%. In comparison, the national growth rate hovers at 40%.

Electronics and related companies head the list of 850 area manufacturers that employ 43,000 people. These industries got their start in the '50s, when aviation pioneer Glenn Martin built a missile manufacturing plant. Martin Co. became Martin Marietta; now the company puts 13,000 to work at two sites making defense and aerospace products. Stromberg-Carlson assembles electronic switching equipment for telephones. NCR manufactures electronic components for cash registers. Other electronics employers include Westinghouse Electric, AT&T Microelectronics, Asea Brown Boveri, Emerson Electric, Litton Laser Systems, Piezo Technology, and Control Laser.

One lure for manufacturers is a total labor force of 656,470 out of a population in the greater metropolitan area that tops 1.2 million. The city of Orlando's population, which numbers 166,283, has more than doubled since 1970. And 400,000 more people are expected to live in the area by the year 2000. However, wages in Florida lag national averages. The average worker nationwide made $20,540 last year while Floridians earned an average of $20,117 annually. Engineers stand to do much better—salaries are competitive and range up to $2000 per week, according to the U. S. Department of Labor.

Belying a popular misconception about Florida, the average area resident is 32.1 years old. One attraction for people of all ages is Orlando's climate. This central Florida city, flourishing between the Atlantic and Gulf coasts, has an average year-round temperature of 72°. Another bonus is that Florida has the second lowest tax bite of the 10 most populous states. Transportation, food, and health care also cost less in Florida than the national average.

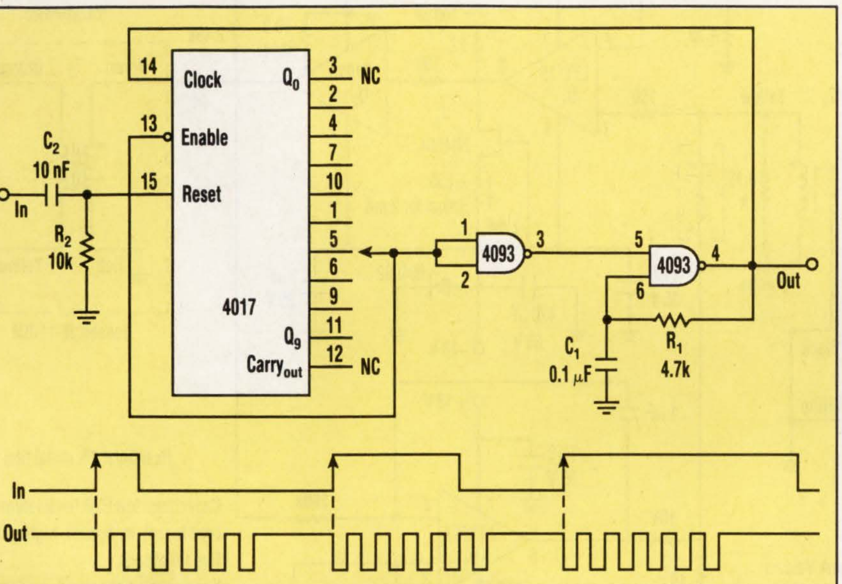
Florida's climate fosters many outdoor sports. With more than 40 public golf courses and 17 private ones, the Orlando area plays host to two PGA and two LPGA tournaments a year. Greater Orlando also has 800 tennis courts and 2,000 lakes, which offer various water sports: boating, sailing, water-skiing, canoeing, and fishing. The Orlando area also has 2,500 acres of park area. A large one is the 1,280-acre Orlando Wilderness park. The Ocala National Forest is nearby. Beaches on the Gulf and Atlantic coasts are about an hour's drive.

There are indoor attractions for the culturally inclined. Among Orlando's 11 museums is the Morse Museum of American Art, which houses a collection of Louis C. Tiffany's work. The Orlando Museum of Art offers a collection of pre-Columbian art. The Florida Symphony Orchestra gives concerts from November through May. There is also the Orlando Opera Company, Southern Ballet Theatre, and the Ballet Royal of Orlando and Winter Park. Plays are staged at the Bob Carr auditorium.

Because of tourist traffic, Orlando is geared to handling visitors. Orlando International Airport is the 20th busiest airport in the world and 17th busiest in the nation. About 24 carriers supply about 800 scheduled flights a day. Amtrak offers four daily trains that originate in New York, Miami, and Tampa.

CIRCLE 521 GET PULSE TRAIN FROM ONE PULSE

ELIAS ELIOPOULOS
117 Konstantinoupoleos, GR-132 31 Petroupoli, Greece.



THIS RATE-MULTIPLIER CIRCUIT contains a 4093 Schmitt trigger that acts as an oscillator, toggling the circuit's output (pin 4). The oscillator's pulses are then counted by the 4017 decade counter.

A rate-multiplier circuit can be used where one pulse must produce a pulse train, as in frequency multiplication, data sampling, etc. The cirucit was originally designed to convert the digital readout of an optical tachometer from revolutions/s to revolutions/min. It produces six pulses, but can be configured to generate a predetermined number of pulses for every input pulse. The circuit's advantage over frequency multipliers using a phase-locked loop and dividers is that phase loss doesn't occur at the stabilization of the pulse train. This trait is especially useful when sampling asynchronous data signals.

One NAND Schmitt trigger (1/4 4093) acts as an oscillator *(see the figure)*. When pin 5 goes low, the output stays high. When pin 5 goes high, the gate starts to oscillate with a free-running frequency:

$$f_{OSC} = R_1 \times C_1 \times \ln\{[V_{T+} \times (V_{DD} - V_{T-})]/[V_{T-} \times (V_{DD} - V_{T+})]\}$$

where V_{T+} and V_{T-} are the positive- and negative-going threshold voltages for the 4093. Their values can be found in the manufacturer's databook for the corresponding V_{DD} value.

When a positive-going pulse arrives at the In input, the 4017 decade counter is reset, output 0 goes high, and the decoded outputs 1 through 9 go low. The oscillator starts running and its pulses are counted by the 4017. The 4017's outputs go high sequentially until the sixth pulse. Then, the oscillator is inhibited and its output remains high, waiting for the next triggering pulse. To configure the circuit to produce between 1 and 9 pulses, tie pins 1 and 2 of the 4093 to the appropriate 4017 output.□

IFD WINNERS

IFD Winner for May 24, 1990

Noor Singh Khalsa, EG&G Inc., EM Div., P.O. Box 809, MS E-1, Los Alamos, NM 87544. His idea: *"Circuit Detects Switch Closure."*

VOTE!

Read the Ideas for Design in this issue, select your favorite, and circle the appropriate number on the Reader Service Card. The winner receives a $150 Best-of-Issue award and becomes eligible for a $1,500 Idea-of-the-Year award.

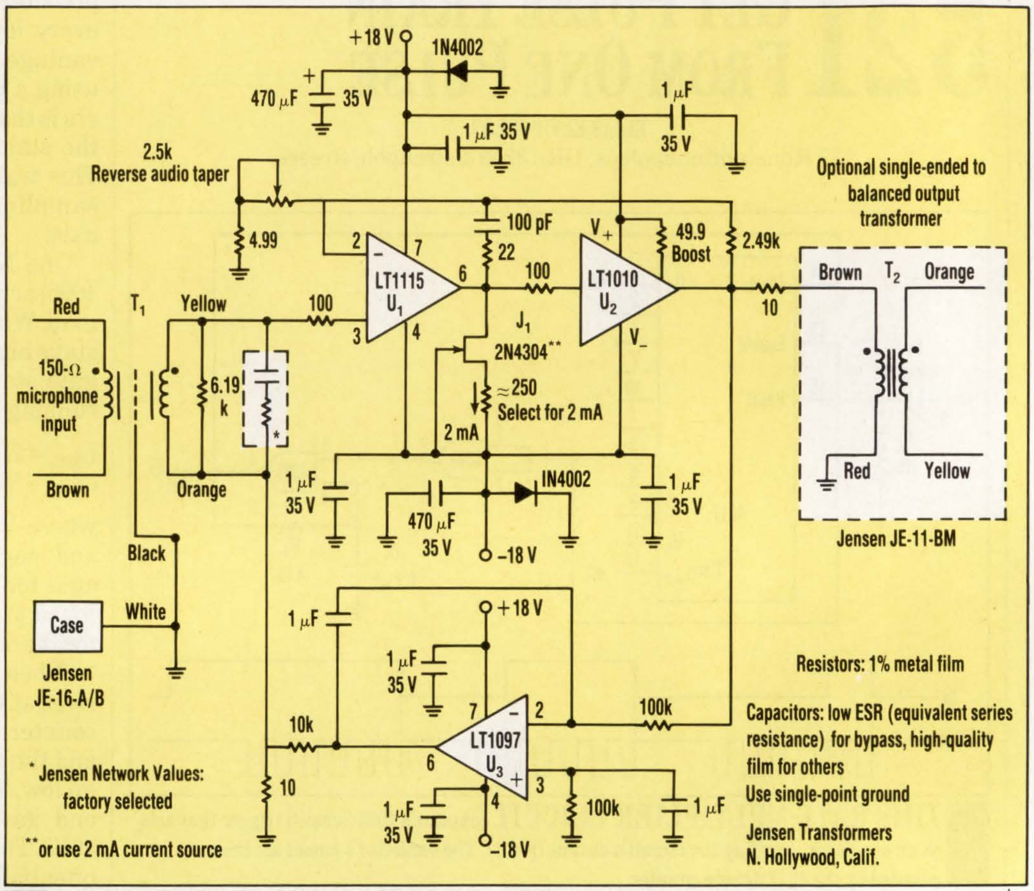
CIRCLE 522 QUALITY PREAMP CUTS COST, SIZE

WALT JUNG and RICHARD MARKELL
Linear Technology Corp., 1630 McCarthy Blvd., Milpitas, CA 95035; (408) 432-1900.

To achieve low noise and 600-Ω (or less) load capability, traditional recording-studio mixing panels use high-cost modular or hybrid amplifiers with matched input-stage transistors and push-pull A-B outputs. Though the expected high performance is achieved, the solution is large and expensive. An alternative approach uses a low-input-noise audio op amp added to a high-quality class-A buffer amp. The resulting circuit forms a variable-gain, transformer-coupled microphone preamp. The preamp is equal to the discrete design in performance, and superior in cost, size, and overall complexity.

IC U_1 is a low-noise LT1115 audio op amp that's operated in a class-A mode by J_1, a 2-mA current source *(Fig. 1)*. U_1's output is buffered by U_2, an LT1010 buffer amp. U_2 can be adjusted to supply a class-A standing current by the 49.9-Ω resistor at the Boost pin, and is capable of very low open-loop distortion.[1] U_3, an LT1097 precision op amp, is configured as a dc servo to null output offsets that can cause distortion in the output transformer, T_2. T_1 is carefully selected to match R_n, the LT1115's characteristic noise resistance.[2] Both transformers should be properly shielded and grounded for optimum performance in this low-level application.

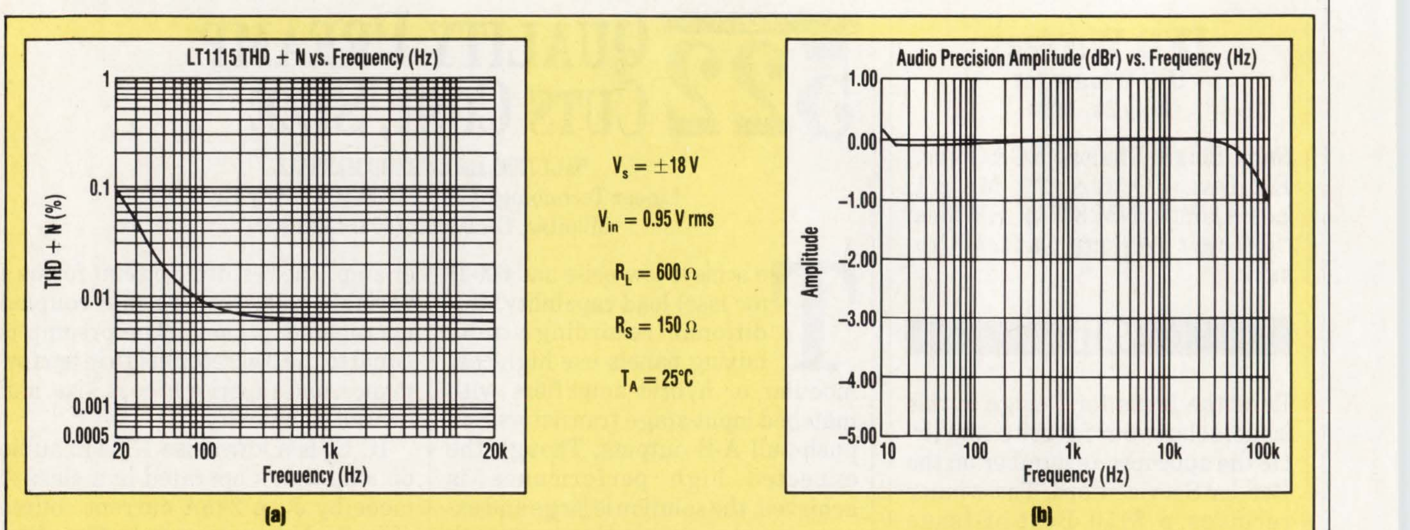
Using the gain control, the circuit's overall gain can be adjusted from 12 to 50 dB. The distortion and frequency-response, plotted at an operating gain of 20 dB, illustrate the circuit's performance *(Fig. 2)*. The risetime of the preamp approximates the Bessel response characteristic, now favored by specialists in the audio field. For top performance, the circuit should be operated with well-bypassed, low source-impedance power supplies.□



1. A LOW-INPUT NOISE AUDIO OP AMP (LT1115) is coupled with a class-A buffer amp (LT1010) to form a variable-gain, transformer-coupled microphone preamp. By altering the gain control, the circuit's overall gain can be adjusted from 12 to 50 dB.

[1]Jung, W.G., R.N. Markell, "Low Distortion Video Buffer," ELECTRONIC DESIGN, March 9, 1989.

[2]Jung, W.G., *Audio IC Op-Amp Applications*, Third Edition, Howard W. Sams and Co., Indianapolis, Ind., 1987.

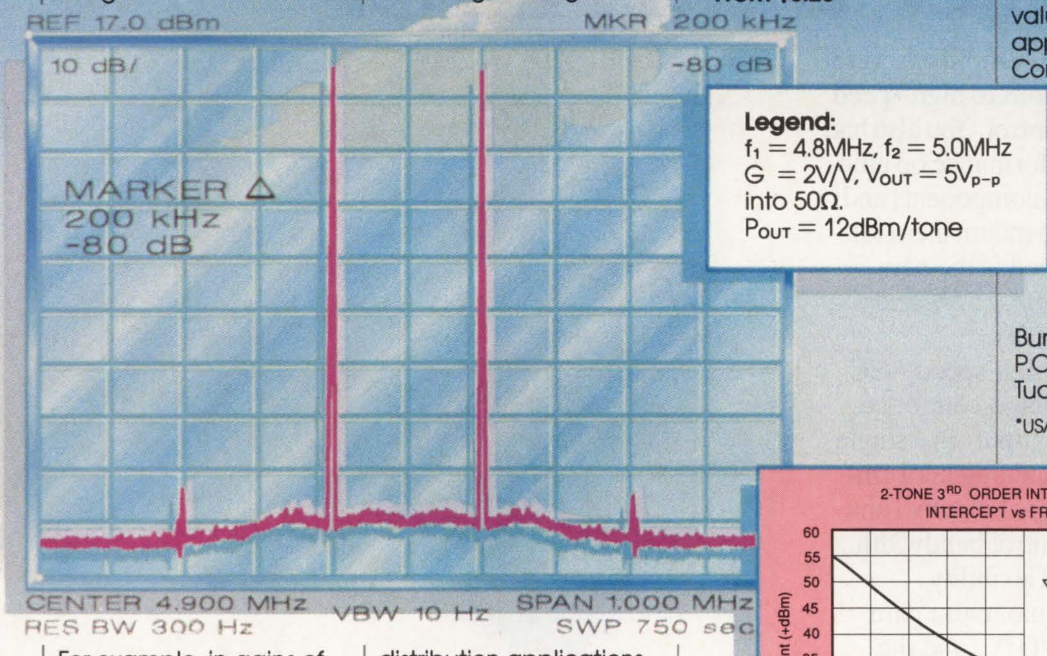


2. THE CIRCUIT'S TOTAL HARMONIC DISTORTION (THD) plus noise is plotted against frequency (a). A second plot shows the circuit's frequency response (b). Both plots illustrate an operating gain of 20 dB with a balanced input-output.

New Low Distortion, Wideband Op Amp Keeps RF Signals Clean and Clear.

-80dBc IMD (5MHz)

OPA621 is a versatile new op amp for RF, video, and other high speed signal processing applications. It gives designers exceptional speed, precision, and output drive in an economical monolithic design.



For example, in gains of 2V/V and above, the uncompensated OPA621 can drive 5Vp-p into 50Ω at 5MHz with a very low 3rd-order intermodulation ratio of −80dBc. This excellent low-distortion performance simplifies filtering tasks and improves signal purity.

OPA621's classic op amp design also avoids the problems of asymmetrical inputs and noisy, long settling tails associated with many current-feedback op amps. It has all the speed needed for RF/video buffering, PLL amplification, peak detecting, and signal distribution applications. Plus, its high current output lets you drive multiple cables and other heavy loads easily and economically.

Key OPA621 Features

- **Bandwidth, 500MHz (G = 2V/V)**
- **2-tone IMD at 5MHz, −80dBc**
- **Noise at 1MHz, 2.3nV/√Hz**
- **Settling to 0.01%, 25ns max**
- **Output drive, 6Vp-p into 50Ω**
- **Differential gain/phase error, 0.05%/0.05° (at 3.58MHz)**
- **0/+70°C, −55/+125°C temp ranges**
- **±5V supply**
- **Plastic, ceramic, SOIC packages and die**
- **From $8.25***

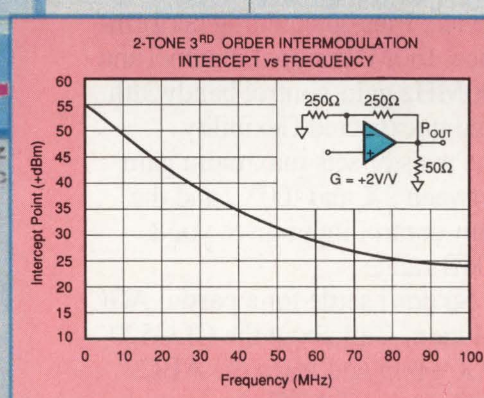
An internally compensated model, OPA620, is also available for unity-gain applications. Besides low distortion and high output drive, it settles to 0.01% in 25ns. Gain-bandwidth is 200MHz.

Design Tools

Burr-Brown makes it easy to put these parts to work in your system. The product data sheets include valuable charts and RF applications information. Contact your sales rep or call **1-800-548-6132** for immediate assistance.

Burr-Brown Corp.
P.O. Box 11400
Tucson, AZ 85734

*USA OEM prices, in 1000s.



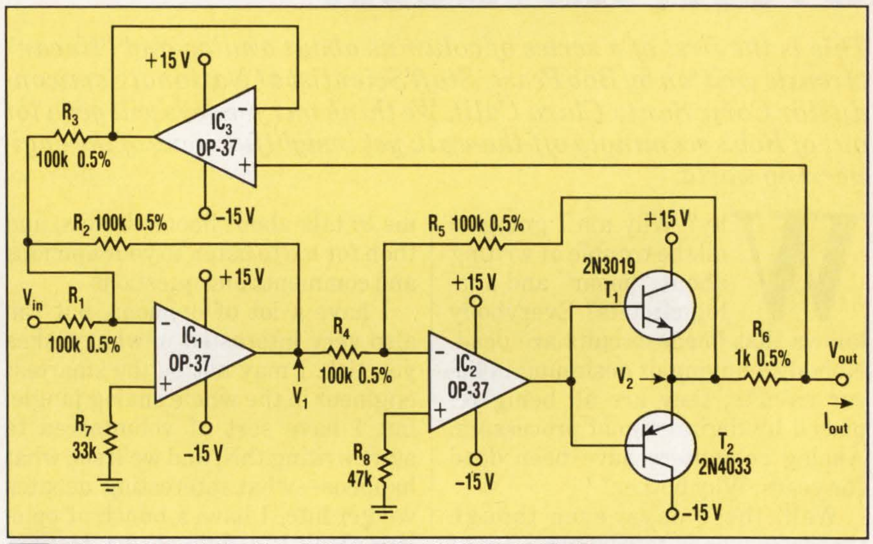
BURR-BROWN®

CIRCLE 116

CIRCLE 523

GROUND LOAD WITH V/I CONVERTER

FRANTISEK MICHELE
Barvicova 17A, CS 60200 Brno, Czechoslovakia.



THIS VOLTAGE-TO-CURRENT CONVERTER **has many advantages, such as working into a grounded load, high precision, and simple control of the I_{out}/V_{in} ratio.**

This voltage-to-current converter circuit is beneficial in many analog applications. The circuit, which consists of three op amps, two medium-power transistors, and a few passive components, has many advantages over alternative circuits *(see the figure)*. These include load-grounding possibilities, simple control of the I_{out}/V_{in} ratio, high precision, linearity, stability, bandwidth, and low noise. It also has an I_{out} range from about 1 μA to the maximum I_C of T_1 and T_2 and an output resistance of about 50 MΩ.

Op-amp IC_1 inverts the sum of V_{in} and V_{out}:

$$V_1 = -(V_{in} + V_{out}).$$

IC_2 and T_1 and T_2 invert V_1:

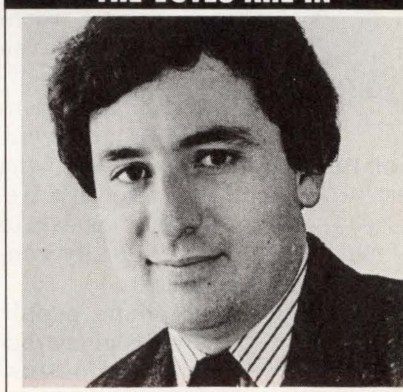
$$V_2 = -V_1 = -(-(V_{in} + V_{out})) = V_{in} + V_{out}.$$

Then, to calculate the output current I_{out}:

$$I_{out} = (V_2 - V_{out})/R_6 = (V_{in} + V_{out} - V_{out})/R_6 = V_{in}/R_6.$$

This formula shows that the value of I_{out} depends only on V_{in} and R_6. Voltage follower IC_3 reduces the current from the circuit's output to the input of IC_1 by a sufficient amount so that this current's influence can be neglected. □

THE VOTES ARE IN



We've tabulated all our readers' votes for the Annual Ideas For Design contest and have come up with a winner: Ricardo Jimenez's "Dc Voltmeter Speaks English." Mr. Jimenez, a test engineer with Shugart/Kennedy Corp., holds a BS in electrical engineering. Mr. Jimenez receives a $1500 honorarium as the annual award winner.

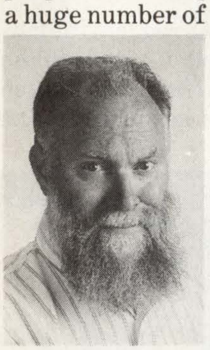
PEASE
PORRIDGE

WHAT'S ALL THIS ANALOG STUFF, ANYHOW?

This is the first of a series of columns about analog and "linear" circuits written by Bob Pease, Staff Scientist at National Semiconductor Corp, Santa Clara Calif. We think our readers will get a lot out of Bob's seemingly off-the-wall, yet insightful views of the engineering world.

Why? Why am I going to all the trouble of writing about "linear" and analog circuits? Everybody knows that linear circuits are dead. Nobody's buying or designing in linear circuits; they are all being replaced by digital signal processors. Analog computers have been dead for years. Why bother?

Well, these days, even though there are trends to perform a lot of functions with digital computations, people are finding that there are still a huge number of things that cannot be done properly without analog circuits. It's true that some of the trendy new radios claim to use a lot of digital techniques, but even there, the receivers and amplifiers are analog circuits—even if the the receiver's frequency appears to be digitally controlled.



BOB PEASE OBTAINED A BSEE FROM MIT IN 1961 AND IS STAFF SCIENTIST AT NATIONAL SEMICONDUCTOR CORP., SANTA CLARA, CALIF.

When people are designing digital computers, they need analog techniques to make good layouts for fast buses. They need power supplies— either linear ICs or switch-mode circuits (which use analog circuits internally). And, as for us analog designers, the old-timers and the rookie engineers—well— this column is intended as a soapbox for me to talk about linear circuits, and then for me to listen to your opinions and comments and questions.

I have a lot of opinions, but I'm also very interested in what makes you tick. I may not be the smartest engineer in the whole analog jungle, but I have sort of volunteered to start writing this, and we'll see what happens—what interesting debates we get into. I have a bunch of opinions about ICs, data sheets, testing, computer simulation, education, troubleshooting, along with a whole slew of little topics.

In every darned issue of Electronic Design, I'll try to have some provocative or insightful topic. Some will be pretty technical, others will be more philosophical in nature. But one thing's for sure, I'll try not to bore you. For example: What's all this heuristic stuff, anyhow?

HEURISTICS?

The other day I was talking with a young college graduate from a prestigious Eastern engineering school. He explained that his specialty was analog synthesis. I perked up my ears—I hadn't heard much about that. Where could I read more about this? "Oh," he said, "in some of the IEEE journals." Hmm. He started to explain the approach. It's a heuristic approach, he said. Hmm. What's a heuristic? He said, "You don't know what a heuristic is? Really?" I explained no, that we didn't have any heuristics when I was in school.

(Note: Mr. Webster says that heuristic means "serving to guide, discover, or reveal; specif.: valuable for stimulating or conducting empirical research but unproved or incapable of proof—often used of arguments, methods, or constructs that assume or postulate what remains to be proven or that leads a person to find out for himself.—from the Greek, heuriskein, to discover, find.")—Gee, that sounds like analysis or optimization to me—not synthesis.

The young man explained that when you make a lot of optimization experiments, heuristic refers to the starting place, the initial guess. H'mm. He said, "You feed in some requirements and some specifications, and it optimizes the performance." Hmm. Now, what circuit does it use? "Oh, it uses the circuit that you give it." Hmm.

THE KEY QUESTION

If you give it a circuit that doesn't work well enough, how does it generate a circuit that works better? "Oh, it doesn't." I explained to this young fellow, that in our whole product line, about 99% of the circuits are not optimized at all—at least not "optimized" in the sense he understands. If you really OPTIMIZED them, they would all be a little different than they are now. But each one has a different circuit that is a revolutionary—not just an evolutionary—change from any previous circuit. So there may be places in our company where optimization is useful and a good idea.

But I wish he wouldn't call it "analog synthesis," that seems to be a misnomer. The circuits around our area—the ones in the NSC Linear data books (and, I bet, in the PMI and Analog Devices data books, too), were not "synthesized" except by bright engineers who knew that the old circuits wouldn't cut it, and a new circuit was needed. Good luck, young fellow!

All for now. / Comments invited! / RAP / Robert A. Pease / Engineer

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Santa Clara, CA 95052-8090

SPEEDY FIFO MEMORIES COME IN BY-9 WIDTHS

Expanding its offering of 9-bit-wide FIFO registers, Mosel Corp., Sunnyvale, Calif., released a trio of units that access in as little as 25 ns. Now available are the MS7200, a 256-word by 9-bit register; the 7201A, a 512-by-9 device; and the 7202A, a 1024-by-9 memory. All three come in both a standard-power and a low-standby-power version. The low-power version has a power-down standby mode that drops the current drain to just 500 μA. The standard-power version has a 5-mA standby-current rating. Active current for the highest-speed version is 125 mA, with slower versions (such as units with 50-ns access times) typically consuming about 50 mA. Each FIFO memory includes three status flag lines—Empty, Full, and Half-full. The memories come in 28-pin 300- or 600-mil DIPs, 330-mil gullwing small-outline packages, or 32-lead plastic leaded chip carriers. All are available from stock. Prices for the standard-power 25-ns versions of the MS7200, 7201A, and 7202A are $12.80, $14.30, and $18.80, respectively. Contact Jeff Hall, (408) 733-4556. DB **CIRCLE 370**

SYNTHESIZED GENERATOR INCLUDES TRIGGER SOURCE

A 20-MHz function generator, which features a built-in trigger generator, eliminates the need for an external trigger source in trigger, gate, or burst modes. The model 90, from Wavetek San Diego Inc., can also be phase-locked to an external source. In this case, the instrument acquires, calculates, and displays the locking frequency automatically. The synthesized generator supplies programmable sine, triangle, square, and dc waveforms. A GPIB interface is standard. Frequency range is 1 to 20 MHz with 0.001% accuracy. Output is up to 40 Vpk-pk, and burst count is up to 1 million cycles. The unit includes modulation and sweep modes, and a nonvolatile memory for front-panel set-ups. Model 90 pricing starts at $3395, with delivery four weeks after receipt of an order. For more information, call (800) 874-4835. JN **CIRCLE 371**

ENERGY IC COLD-STARTS COMPUTER FROM KEYBOARD

Featuring special circuitry, a new CMOS chip can turn a computer on or off using the keyboard instead of a circuit-breaker switch. By using the DS1239 from Dallas Semiconductor, Dallas, Texas, equipment can be cold-started with a kick from a 3-V lithium source. This eliminates the need to reach around the computer and fumble for the on-off switch. The chip also isolates 110/220-V ac power from the person activating the switch. A power-supply monitor sends a warning signal to the processor if power falls out of tolerance. The DS1239 is available from stock for $3.50 each in 1000-piece quantities. JC **CIRCLE 372**

SOFTWARE MEASURES ANTENNA PATTERNS

A new software package can automate far-field antenna-pattern measurements, including gain, beamwidth, side-lobe levels, polarization, axial ratio, and beam symmetry. Running on an HP model 9000 series 300 workstation, the HP 85361A software integrates an HP 8753B/C network analyzer and a positioner/controller for measurements in the 300-kHz to 3-GHz range. The package works with positioners from Flam & Russell and Orbit. Single- or dual-axis control are possible, and patterns may use either continuous-wave or multiple frequencies. Data can be presented in Cartesian, polar, or three-dimensional formats. The software identifies peak gain, half-power beamwidth, and a user-specified beamwidth automatically. The HP 85361A package costs $12,000 and is available 6 weeks after ordering. Call (800) 752-0900. JN **CIRCLE 373**

TOOLSET IMPLIFIES MOTIF INTERFACE DESIGN

By employing graphics rather than command descriptions, the Builder Xcessory allows designers to create Motif user interfaces graphically, thus reducing application development design. The toolset, from Integrated Computer Solutions Inc., Cambridge, Mass., is an interactive, paint-like software utility that eases the task of prototyping and testing Motif user interfaces for the X-window environment. With the Xcessory, designers can click on icons and move them within the interface, similar to a paint program. Overall development time is reduced considerably because the interface can be tested and modified without compiling. The tools include a Palette, which contains a large collection of Motif interface objects; a Resource Editor, which enables interface objects to be customized; and the Browser, which illustrates widget instance hierarchy. The Builder Xcessory program runs on all Sun workstations, DECstations running Ultrix, Aviion platforms from Data General, workstations from Silicon Graphics and Sony, and the Apple Macintosh running A/UX. The company also plans to offer the software for VAX/VMS systems from DEC and the R6000-based systems from IBM. A single-platform version of the software sells for $2500 and is available immediately. Call Peter Winston, (617) 547-0510. DB **CIRCLE 374**

BIG CHANGE.

FOR THOSE WHO KNOW THE WORLD IS HEADED FOR HIGH PERFORMANCE, MORE POWER TO YOU.

If you're among the leading-edge designers on a power trip to the future, consider this. Motorola's Microcontroller Division just cut your travel costs with an offer too good to miss:

*Act between September 4 and October 12, and you can get a computer-based learning program and a development kit for our 32-bit microcontrollers for just $332. Plus, you could win a supercharged Macintosh® IIfx.**

This offer is the perfect way to learn about Motorola's 68332. The one microcontroller that delivers the 32-bit performance and integration you will need to be competitive in tomorrow's world. And it's available from Motorola today.

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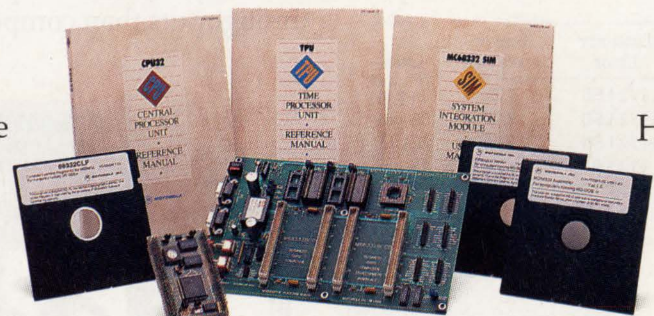
START OUT SMALL. END UP WITH BIG RESULTS.

This $332 introductory offer, *available only through your Motorola distributor,* includes our $32 68332CLP computer-based learning

SMALL CHANGE.

FOR THOSE WHO WANT TO KNOW MORE, OUR 32-BIT LEARNING TOOLS ARE NOW JUST $332.



program. As well as the $300 68332KIT.

The 68332CLP learning program alone is the equivalent of a full-day instructional seminar. It features a MS-DOS® programmed learning disk and a complete set of manuals that teach you how to design the 68332 into your next system.

The 68332KIT development package has everything you need to learn hands-on operation of the 68332, including a Business Card Computer (BCC). With a surface mount 68332, 128K bytes of EPROM, 64K bytes of RAM, and a RS232 port, the BCC provides stand-alone evaluation of the 68332 on a board the size of a business card.

The 68332KIT also features a Platform Board for mounting the BCC in expanded development operations. As well as assembler software. And a variety of support literature.

Perform the exercise included in your 68332KIT or 68332CLP and send us your completed entry form by December 31, 1990. If you performed the exercise correctly, you become eligible for a drawing to win one of five Mac IIfxs. (The Mac IIfx can be awarded to you, your company, or your favorite charity.)

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THE PATHWAY TO PERFORMANCE.

MOTOROLA

SAMPLING A/D CONVERTERS

Model	Resolution (Bits)	Throughput (MHz)	Linearity Error	Power (Watts)	Case
ADS-111	12	0.500	±3/4 LSB	1.3	24-pin
ADS-112	12	1.0	±3/4 LSB	1.3	24-pin
ADS-193	12	1.0	±3/4 LSB	1.3	40-pin
ADS-132	12	2.0	±3/4 LSB	2.9	32-pin
ADS-131	12	5.0	±1 LSB	3.6	40-pin
ADS-130	12	10.0	±1 LSB	3.7	40-pin
ADS-924	14	0.300	±1 LSB	1.4	24-pin
ADS-928	14	0.500	±1/2 LSB	2.9	32-pin
ADS-941	14	1	±3/4 LSB	3.1	32-pin
ADS-942	14	2	±3/4 LSB	3.2	32-pin
ADS-930	16	0.500	±1 LSB	1.8	40-pin

SAMPLE-HOLDS

Model	Linearity	Acquisition Time (ns)	Gain	Bandwidth	Case
SHM-42	0.01%	50	+1	40 MHz	14-pin
SHM-43	0.01%	25	+1	40 MHz	14-pin
SHM-945	0.001%	500	-1/2, -1, -2	12 MHz	24-pin

A/D CONVERTERS

Model	Resolution (Bits)	Conversion Time (µs)	Linearity Error	Power (Watts)	Case
ADC-228	8	0.040	±1/2 LSB	1.25	24-pin
ADC-530	12	0.350	±1/2 LSB	2.10	32-pin
ADC-908	14	1.0	±1/2 LSB	2.70	32 pin
ADC-914	14	2.4	±1 LSB	1.20	24-pin

Superior Performance From one Complete Source. DATEL's precision, high-speed data converters are the design advantage.

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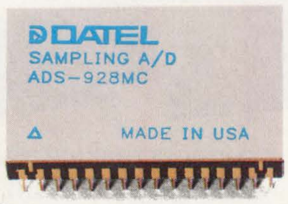

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DATA ACQUISITION SYSTEMS

Model	Resolution (Bits)	Throughput (KHz)	Power (Watts)	Channels	Case
HDAS-75	12	75	0.5	8 SE	40-pin
HDAS-76	12	75	0.5	4 DE	40-pin
HDAS-534	12	250	2.4	4 DE	40-pin
HDAS-538	12	250	2.4	8 SE	40-pin
HDAS-524	12	400	2.4	4 DE	40-pin
HDAS-528	12	400	2.4	8 SE	40-pin
HDAS-950	16	75	1.3	8 SE	40-pin
HDAS-951	16	75	1.3	4 DE	40-pin

MULTIPLEXERS

Model	Channels	Settling Time 20V to 0.01%	Input Range	Power (Watts)	Case
MX-826	8 SE	225 ns	±10.5V	0.370	24-pin
MX-850	4 SE	50 ns	±10.5V	0.210	14-pin

DATEL

INNOVATION AND EXCELLENCE IN PRECISION DATA ACQUISITION

CIRCLE 156

ENHANCED SCSI PROCESSOR PUSHES SYSTEM PERFORMANCE

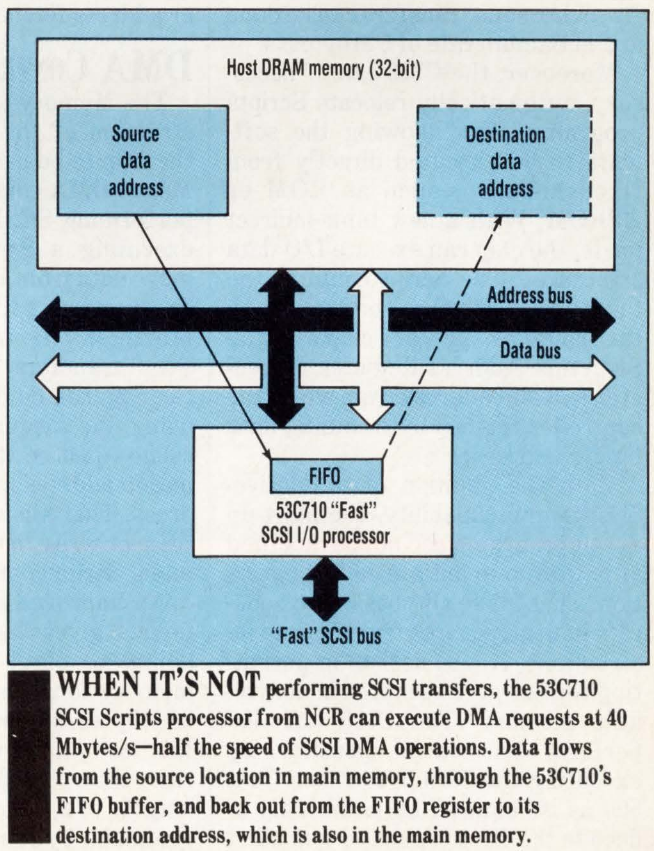
SCRIPTS CHIP ADDS MULTITHREADED I/O, 80-MBYTE/S DMA TRANSFERS, AND MORE FOR TOP SYSTEM DATA THROUGHPUT.

DAVE BURSKY

Moving an environment from single-tasking to multitasking requires more than just a flexible CPU that can quickly switch between jobs. Once in a multitasking environment, the mass-storage subsystem usually becomes one of the main performance bottlenecks. Most mass-storage systems that include disk drives and other storage devices have access times in the tens of milliseconds. And their data-transfer rates are a fraction of the host-system's bus bandwidth.

To eliminate this bottleneck, designers at NCR Microelectronics have added new features to their previously released 53C700 Scripts processor (ELECTRONIC DESIGN, *August 10, 1989, p. 37)*. The new features create a superset CMOS device dubbed the 53C710. The C710 was designed specifically to execute, without processor intervention (except at the end of an I/O operation), multithreaded I/O algorithms—such as the ones found in workstation and file-server environments.

Another feature is a 32-bit bus-master DMA channel capable of 80-Mbyte/s data transfers (about 50% faster than the previous chip). In addition, the processor has a byte-ordering control pin that swaps the byte order to match the word structure of the processor that the chip



WHEN IT'S NOT performing SCSI transfers, the 53C710 SCSI Scripts processor from NCR can execute DMA requests at 40 Mbytes/s—half the speed of SCSI DMA operations. Data flows from the source location in main memory, through the 53C710's FIFO buffer, and back out from the FIFO register to its destination address, which is also in the main memory.

connects to. Consequently, the controller can tie into either 80x86 or 680x0 buses with minimal circuitry.

An optional multiplexed address-and-data mode gives flexibility. This mode allows the chip to tie into low-cost host buses, such as Sun's SBus, with minimal support circuitry, or into more complex buses, with a few latches. Separate SCSI-bus and host-bus clock lines enable each bus to operate at its peak speed. System design requirements are thus simplified and each section of the system can be optimized for speed, cost, power, and other factors.

Furthermore, the glitches on the SCSI bus, which are typically generated when a SCSI device powers up or down, are also eliminated. Like the previous controller, the C710 can transfer data at 10 Mbytes/s in its synchronous mode. It can also implement a true "fast SCSI" subsystem with maximum cable lengths as specified by the SCSI-2 standard. Synchronous offsets from 1 to 8 bytes can be used. Most other chips that include a fast-SCSI option require significantly reduced cable lengths. Asynchronous transfers can be done at a maximum rate of 5 Mbytes/s.

Moreover, the C710 can, if necessary, automatically relocate Scripts programs, thus allowing the software to be executed directly from fixed memory, such as ROM or EPROM. With a new table-indirect mode, the chip can execute I/O data structures. The Script contains the table offset, which is combined with the contents of the chip's Data-Structure Address Register, to generate a 32-bit address from which the controller fetches byte counts, data buffer addresses, etc.

With the addition of a relative-Script-jump capability, the start-up Script program need not be modified at power-up to initiate an I/O operation. That makes it possible to separate data structures from Scripts instructions. It also assists in permitting the Script to be stored in nonvolatile memory. The C710 and 700 perform their control operations by executing the Scripts routines. Just 500 ns is required by either chip to decode the first command and start implementing a Script.

Scripts is the programming concept NCR introduced with the 53C700. A Script program consists of modular SCSI control routines that are compiled—using an NCR development tool—and reside in the main system memory. To develop the Script program more easily, the company created a Script compiler that runs on any computer with a C compiler. The company also has a library of sample Script programs to simplify the creation of a custom Script.

The wide variance in bus latency from system to system requires that the C710 permit designers to locate SCSI Scripts and indirect data structures in either the main system memory or in a local memory on the host adapter card. A Fetch pin on the chip is brought high to indicate that the C710 is fetching Script instructions. With the availability of such a signal, external logic can steer a Script fetch locally, instead of causing a fetch from the main memory. Alternately, the chip can be set up to raise the Fetch pin during indirect data-structure fetches (for byte-count or buffer-address fetches).

DMA Controller

The Memory-to-Memory Move instruction of the controller enables the chip to be used as a high-performance DMA controller when it isn't performing SCSI operations. When executing a Script, the C710 can move data from a source address to a destination address at up to 40 Mbytes/s *(see the figure)*. And, if SCSI transfers aren't being done, the chip can do data moves without using the system processor or its cache—just set the source or destination address to a chip register address. That allows the C710 to read from or write to the system memory under Script control.

An improved host-system bus interface gives the new controller the ability to burst data from a local memory to the host system at up to 66 Mbytes/s. Very fast cache-line refills or data-streaming operations can thus be performed. Burst lengths of 2, 4, or 8 bytes can be programmed by the user. To aid in the transfer, a 64-byte FIFO register (16 words by 32 bits) is part of the chip.

Thanks to a Back-off control pin on the controller, the host system can force the C710 to relinquish the host bus, allowing a system to preempt a data burst for another high-priority task. To resolve bus deadlocks and eliminate system hardware lockups, the chip also includes a bus-retry capability that rearbitrates for the bus and retries data transfers.

To take control of the bus quickly, designers at NCR added a fast arbitration mode that removes one clock cycle from the host-bus arbitration time. That makes it easier to use host buses requiring extra address setup time and to more efficiently use the bus bandwidth of processor buses. Four programmable Status Output pins are active when the chip is a bus master. The pins can supply the host system with information about the current operation, or serve as user-programmable signal pins.

The C710's activity timer can be used to time all SCSI-bus activity, and interrupt the system after 250 ms if it detects a hang-up. Previously, the host adapter or host system provided this function. Another error-prevention aspect included on the chip consists of an Exclusive-OR register, which gives a vertical parity (checksum) value at the end of a data transfer.

The controller comes in a 160-lead quad-sided flat package. As with all NCR SCSI chips, it includes single-ended drivers/receivers that are engineered to withstand the harsh electrical realities of the SCSI cabling environment.☐

Price And Availabilty

The 53C710 SCSI Scripts processor, sells for $63 in quantities of 1000. The previously released 53C700 sells for $51.95 in similar quantities. Delivery of C710 samples is from stock.

NCR Microelectronics Inc., 1635 Aeroplaza Dr., Colorado Springs, CO 80916; Brian Brown, (719) 596-5795. CIRCLE 537

How Valuable?	Circle
Highly	538
Moderately	539
Slightly	540

TEXAS INSTRUMENTS

A PERSPECTIVE ON DESIGN ISSUES:

Creating systems with an analog edge

IN THE ERA OF

MegaChip

TECHNOLOGIES

Advanced Linear can help you raise system performance levels.

A leadership family of analog circuits from Texas Instruments is helping designers meet difficult design challenges.

The evidence is strong. Throughout the design community, systems using the new breed of Advanced Linear functions from Texas Instruments are achieving the keener performance edges that can spell marketplace success.

TI's new analog devices are enabling design engineers to link digital brains to analog worlds more effectively and efficiently than ever before. Some offer new standards of accuracy or speed while others are highly integrated devices combining analog and digital functions on a single chip. The result is superior system performance and design flexibility.

These Advanced Linear functions are the result of leadership process technologies that we at TI firmly believe are the key to the advanced analog devices your future applications will demand.

Intelligent power for automobiles

Designers in the automotive industry face a tough challenge: Handle high reverse voltages and achieve rapid load turnoff while providing fault protection, detection, and reporting and efficient load management. To provide the needed intelligent power devices, we developed one of our newest process technologies, Multi-EPI Bipolar. It is unique because it can combine rugged power transistors with intelligent control functions.

The resulting circuits are now providing reliable, cost-efficient control of solenoids and valves in such automotive applications as antiskid braking systems, electronic transmission controls, and active suspension systems.

Other industry segments are also benefiting from TI's Advanced Linear process technologies. Here are a few of the winning designs to which we have helped add an analog edge:

Toledo Scale

Challenge: Improve the accuracy of point-of-purchase scales by eliminating drift over time and temperature.
Solution: The TI TLC2654 Chopper op amp. Our Advanced LinCMOS™ process makes possible chopping frequencies as high as 10 kHz, reducing noise to the lowest in the industry.

Pulsecom

Challenge: Develop a linecard capable of driving low-impedance loads with greater precision.
Solution: Our TLE206X family of JFET-input, low-power, precision operational amplifiers. These devices offer outstanding output drive capability, low power consumption, excellent dc precision, and wide bandwidth. Fabricated in our Excalibur process, they remain stable over time and temperature.

Leitch Video

Challenge: Design a compact, cost-efficient direct broadcast satellite TV descrambler for consumer use.
Solution: TI's TLC5602 8-bit Video DAC. Our LinEPIC™ process combines one-micron CMOS with precision analog to satisfy the demands of the application for video speeds and low-power operation.

U.S. Robotics

Challenge: Build a modem for high-speed data transmission between computers; allow flexible operation and minimize data errors.
Solution: Our TLC32040 Analog Interface Circuit (AIC). A product of our Advanced LinCMOS process, the AIC combines programmable filtering, equalization, and 14-bit A/D and D/A converters with such digital functions as control circuitry, program registers, and a DSP interface.

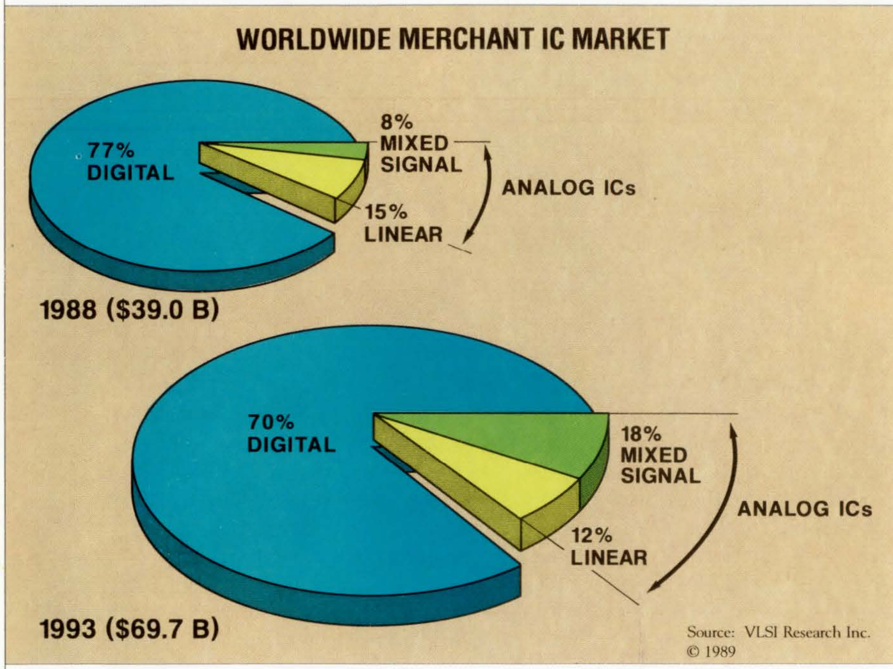
Xerox

Challenge: Cut component count and cost of copier systems while boosting reliability.
Solution: Our TPIC2406, a top-performance peripheral driver in a standard DIP package that is capable of driving heavy loads. It is fabricated using our Power BIDFET™ process which permits greater circuit density and incorporates CMOS technology for low total power dissipation.

Mr. Coffee

Challenge: Design an intelligent coffee maker that brews faster, maintains optimum temperature, shuts off automatically, and has a built-in cleaning cycle.
Solution: Our LinASIC™/LinBiCMOS™ capability permits us to combine both analog and digital library cells with custom analog cells. This results in cost-efficient integration of temperature monitoring, timing, and high-current outputs on a single control chip.

All of these examples point to one conclusion: TI's Advanced Linear functions are adding an analog edge to many system designs. They are contributing significantly to the enhanced system performance that marks a market winner.



Helping you implement your designs in a changing world.

An increasing share of the total analog market is being captured by mixed-signal devices. As they gain more widespread acceptance, they are driving the expansion of the overall analog market (*see above*).

Changes such as this are the order of the day in the IC marketplace. Texas Instruments continues to provide not only the high-performance circuits you need but also the depth of experience, support, and service fundamental to successful completion of your designs.

Experience: Building on three decades in ICs

We at TI can successfully meet your requirements for mixed-signal devices because we have acquired the necessary knowledge from 30 years of experience in developing both analog and digital functions. We have also drawn upon our digital ASIC strengths in developing our LinASIC capabilities.

Support: Speeding our chips to you

The faster we move new products through our design cycles, the faster you can get through yours.

We employ a wide variety of design-automation tools and sophisticated software to speed our development process.

Service: Providing a surety of supply

However advanced our circuits may be, they are of little value if they are inaccessible to you. TI operates on the principle of global coverage, local service. We manufacture semiconductors in 13 countries and operate support centers in 22. We have product and applications specialists, designers, and technicians around the world. They are linked by one of the world's largest privately owned communications networks so that we can bring you our best — circuits and support — from wherever they may be to wherever you are.

Keeping our communications open

The relationship between you as customer and us as vendor is vital: You are our chief source for firsthand information that can help guide us in developing the circuits you will need for your future designs. We at TI welcome your comments and your suggestions.

TI's Leadership Analog Processing Technologies

LinBiCMOS — Combines Advanced LinCMOS, digital ASIC CMOS, and up to 30-V bipolar technologies to allow the integration of digital and analog standard cells and handcrafted analog components on a monolithic chip.

LinEPIC — One-micron CMOS double-level metal, double-level polysilicon technology, which adds highly integrated, high-speed analog devices to the high-performance digital EPIC process.

Advanced LinCMOS — An N-well, silicon-gate, double-level polysilicon process featuring improved resistor and capacitor structures and having three-micron minimum feature sizes.

Power BIDFET — Merges standard linear bipolar, CMOS, and DMOS processes and allows integration of digital control circuitry and high-power outputs on one chip. Primarily used for circuits handling more than 100 V at currents up to 10 A.

Multi-EPI Bipolar — A very cost-effective technology that utilizes multiple epitaxial layers instead of multiple diffusion steps to reduce mask steps by more than 40%. Used to produce intelligent power devices that can handle loads as high as 20 A and voltages in excess of 100 V.

Excalibur — A true, single-level poly, single-level metal, junction-isolated, complementary bipolar process developed for high-speed, high-precision analog circuits providing the most stable op amp performance available today.

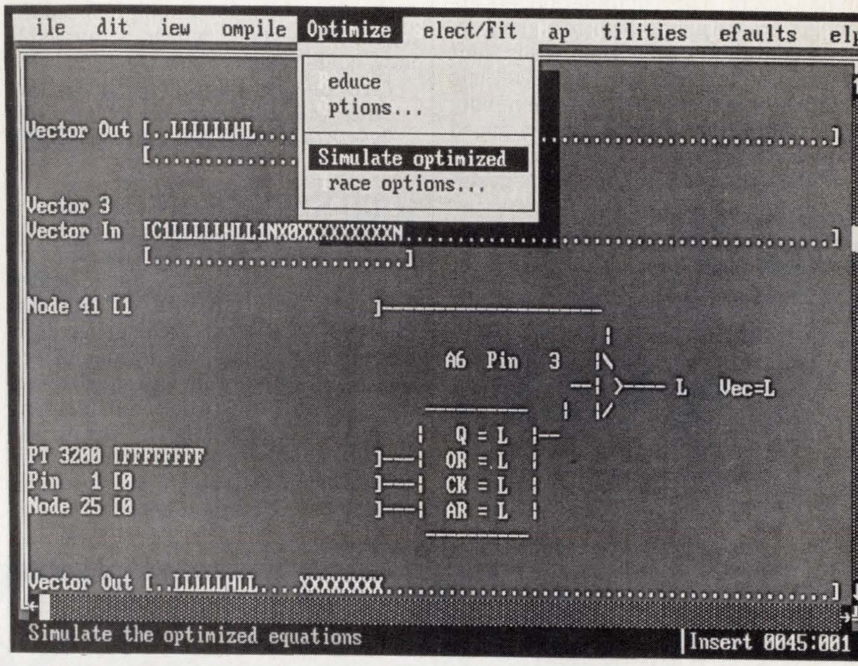
If you would like a more detailed explanation of our Advanced Linear process technologies, please call **1-800-336-5236, ext. 3423**. Ask for a copy of our *Advanced Linear Circuits* brochure.

TEXAS INSTRUMENTS

AN HDL RAISES THE LEVEL OF ABSTRACTION FOR PROGRAMMABLE-LOGIC DESIGN

LISA GUNN

An enhanced hardware description language (HDL) helps to raise the level of design abstraction for engineers using Data I/O's newest version of the Abel software, Abel-4. The new software also features a window-based interactive user interface, increased device support, SmartPart intelligent device selection, automatic logic optimization, and a testing option.



The Abel HDL is optimized for field-programmable-gate-array (FPGA) and programmable-logic-device (PLD) designs. Because it is device- and architecture-independent, engineers can enter and verify designs without part specifications. Language features give engineers control over device characteristics such as buried flip-flops and configurable macrocells. As a result, engineers choose the level of detail required for their design. Input to the HDL can be in the form of high-level equations, state diagrams, truth tables, and schematics.

Other HDL enhancements include clearly-defined Pin and Node declarations, simplified signal attributes, and signal dot extensions for more complex language situations. The Abel synthesis software creates circuits for PLDs and FPGAs, or transfers the design information to other environments through standard-format transfer files.

Expanded FPGA support includes the Xilinx LCAs, Actel ACT 1 family, Altera Max, and Plus Logic devices. In total, the Abel-4 design software supports over 6000 devices and over 300 architectures.

SmartPart intelligent device selection automatically generates a list of candidate devices for every design by comparing the design's requirements with device resources. A design can then be tried in multiple architectures to determine the best fit. Users can define device technology, speed, manufacturer, and price.

Abel-4 simulates a design at the device and system level for thorough verification. A design can be simulated at the functional level prior to device selection. Simulation results are given in both tabular and waveform formats. Device-level simulation allows for full verification before programming, including verifying that a design fits properly in the targeted device. Every fuse, node, and pin is fully debugged.

Multiple optimization techniques ensure an optimum device fit. Abel-4 algorithms contain device-independent synthesis features and device specifics. These specifics help to efficiently utilize complex device attributes such as multiple flip-flop types, exclusive OR gates, unique interconnect schemes, and folded arrays. Register synthesis, which lets users design independent of flip-flop type, automatically makes an intelligent decision based on the design. A reduction algorithm eliminates redundant circuitry.

Data I/O's recently announced Open-Abel is part of Abel-4. It lets users take advantage of a universal design language without sacrificing device support or optimization. This is because with Open-Abel, semiconductor companies can write specialized device algorithms to fully optimize the silicon resources. The algorithms are termed fitters. Data I/O is licensing semiconductor vendors to write fitters for Open-Abel by means of the Abel-PLA format.

The PLDgrade testing option to Abel-4 performs automatic fault grading and testability analysis. It allows user-generated test vectors to be fault-graded by the design engineer, prior to the design entering production.

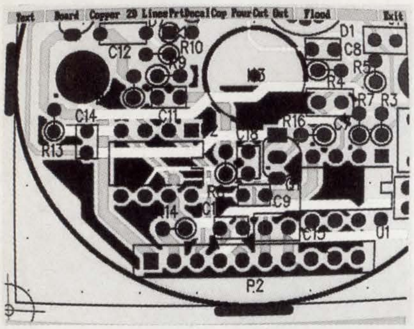
Abel-4 costs \$1995 for IBM XT, AT, and PS/2 computers and compatibles; \$2695 for Sun-3 and Sparcstation workstations; and \$4115 for VAX VMS workstations. The software is also available for site licensing. The PLDgrade option costs \$495. Abel-4 is shipping now with 2-4 week delivery after receipt of order.

Data I/O Corp., 10525 Willows Rd. N.E., P.O. Box 97046, Redmond, WA 98073-9746; (206) 881-6444.

CIRCLE 301

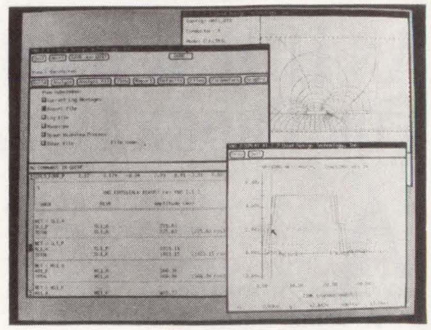
PCB DESIGN SOFTWARE USES VIRTUAL MEMORY

CAD Software Inc.'s top-of-the-line pc-board design system, called Pads-2000, runs on 80386- or 80486-based personal computers and uses virtual-memory management. This combination lets engineers create printed-circuit-board designs containing over 2000 equivalent 14-pin ICs. In addition, Pads-2000 has several features that have previously been found only in workstation-based pc-board tools. These features include a copper-pour routine that fills a designated area with copper while leaving the included tracks and pads isolated, 1-μm resolution, T routing, rotation of components and pads in 1/10th-degree increments, and five different autorouters. Engineers can design double-sided surface-mounted boards, mixed-technology boards, and high-speed designs. Pads-2000, which is available now, costs $6995.



CAD Software Inc., 119 Russell St., Suite #6, Littleton, MA 01460; (800) 255-7814 or (508) 486-9521. **CIRCLE 302**

HIGH-SPEED SIMULATOR PREDICTS SKIN EFFECT

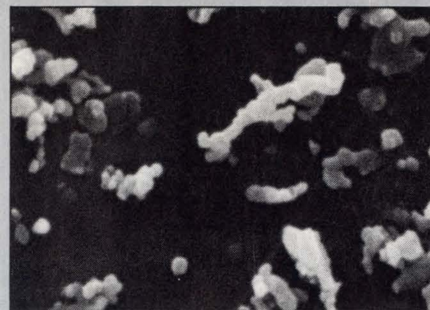


The newest release of Quad Design Technology's Crosstalk Tool Kit (XTK), XTK 2.0, can predict such high-frequency problems as the skin effect. This occurs when thin wires pick up extra resistance due to electron bunching at the wire surface. Thin wires are used in multichip designs. Version 2.0 simulates ultra-high-frequency, ultra-high-density printed-circuit boards. It calculates signal distortions and simulates their effects on system timing for boards with up to a 2-GHz operating frequency. Furthermore, it performs these tasks at both the board and net levels. XTK 2.0 is shipping now. It runs on Sun and HP/Apollo workstations, and memory-extended PCs. The Crosstalk Tool Kit software costs between $27,000 and $41,000, depending on the hardware platform.

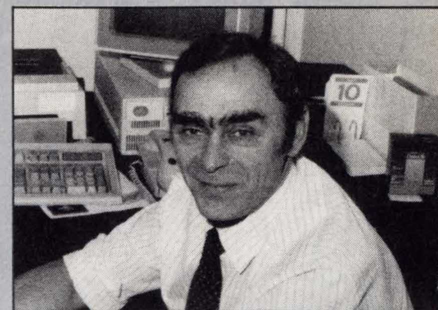
Quad Design Technology Inc., 1385 Del Norte Rd., Camarillo, CA 93010; (805) 988-8250. **CIRCLE 303**

INCO SPECIALTY POWDER PRODUCTS RESEARCH AND DEVELOPMENT... NEW PRODUCTS FOR NEW TECHNOLOGIES

Victor Ettel, Director of Battery Powder Research, Sheridan Park, Mississauga, Ontario, Canada. His job is to find new uses for carbonyl technology.

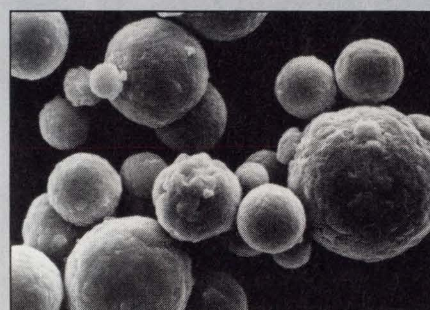


UFP, Ultra Fine Powder

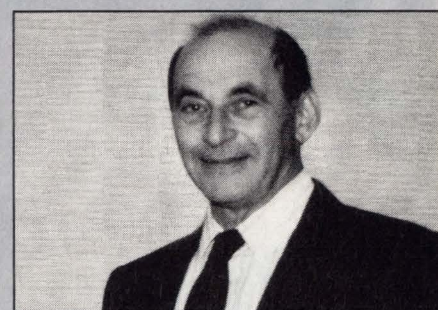


Eurof Rees, Pilot Plant Superintendent, Clydach Nickel Refinery, Wales, U.K. Eurof has been involved in carbonyl coating of substrates for more than twenty years.

Frank Heck, Technical Director, Novamet Specialty Products Corp. Wyckoff, New Jersey. Frank is always looking for new ways to produce a better powder.



4SP Spherical Powder



George Tyroler, Technical Superintendent, Copper Cliff Refinery, Sudbury, Canada. George likes working on the edge of developing nickel powder products.

INCO Specialty Powder Products is continuing to develop advanced powders and applications. Our mission is to develop new products for new technologies. INCO SPP personnel from marketing, manufacturing and research work together as a team, bringing to bear their disciplines to serve you and your needs.

NEW NICKEL POWDER PRODUCTS IN DEVELOPMENT

UFP, Ultra Fine Powder. A unique mixture of high nickel surface area, very fine particle size (0.8 microns) low density (0.07gm/cc) morphology and high purity. Surface area is 3 to 5 times that of other conventional carbonyl nickel powder. Surface resistivity in acrylics is at 10 ohms per square. It also presents possibilities for pasting in conductivity applications. This points to a greater range of resistivity with other agents, especially in thin film technology.

4SP Spherical Powder. Completely spherical and smooth in shape. Particle sizes of 8-9 microns. It has the potential to increase strength of P/M steel parts compared to other nickel powders. The particle shape presents opportunities for metal injection molding.

INTERNATIONAL RESEARCH GROUP

INCO Specialty Powder Products is conducting research and development at the Novamet Specialty Products Corp. in the US, at the Clydach Refinery in Wales, UK, and Sheridan Park Corporate Laboratory and Copper Cliff Refinery in Ontario, Canada. We are fortunate to have some of the leading powder technology researchers on our staff.

For more information write INCO Specialty Powder Products, Dept. 3-90, Park 80 West-Plaza Two, Saddle Brook, NJ 07662

INCO SPP

Park 80 West-Plaza Two, Saddle Brook, NJ 07662
Shin-Muromachi Building, 4-3 Nihonbashi-Muromachi 2-Chome, Chuo-ku, Tokyo 103 Japan
1-3 Grosvenor Place, London SW1X7EA England
15/Fl Wilson House, 19-27 Wyndham Street Central, Hong Kong

CIRCLE 85

GENERATE VHDL FROM GRAPHICAL MODELS

Designers can produce VHDL code from graphical models with the Express VHDL software from i-Logix Inc. The resultant code can be used to drive any VHDL-compliant simulator. The behavioral models are created in the company's Statecharts language, which extends state-transition diagrams with hierarchy, concurrency, and broadcasting. States and transitions are described with boxes and arrows. Labels on the transitions indicate when and under what conditions each transition will take place. Once a system's behavioral model is expressed graphically, the equivalent VHDL code is automatically generated with the push of a button. Express VHDL will start shipping in the fall. Pricing for the software starts at $32,500.

i-Logix Inc., 22 Third Ave., Burlington, MA 01803; (617) 272-8090. **CIRCLE 304**

DATABASE MEETS ENGINEERING NEEDS

ObjectStore is an object-oriented database management system (ODBMS) targeted at the electrical design-automation market. It supports object-oriented development in C++, and also supplies a migration path for applications developed in C to C++. In addition, ObjectStore applications are compatible with other subroutine libraries such as Fortran and Pascal. Development tools included with the DBMS are SchemaDesigner, an interactive graphical tool for creating database schemas; a browser; and a debugger. The database runs in any heterogeneous client-server environment of networked workstations and high-end PCs. Pricing for ObjectStore, which is on a per-seat basis, ranges from $2000 to $9000. Runtime license pricing is also available for independent software vendors. Shipment begins this month.

Object Design Inc., One New England Executive Park, Burlington, MA 01803; (617) 270-9797. **CIRCLE 305**

SIMULATE LARGE DESIGNS WITHOUT EXTRA MEMORY

Innovative simulation techniques and algorithms let a new simulator from Silicon Automated Systems run very large designs—those with over 100,000 gates—without additional memory. The company claims that the simulator runs ten times faster than other leading industry simulators. The X-Sim system simulation environment includes the X-Sim simulator executive and the X-Sim backplane bus. Various components, such as an HDL engine, VHDL engine, X-Sim control language, and test simulation server, communicate with each other through the backplane. The X-Sim control language has features for setting the simulation environment that eliminate the need for recompilation and linking. The system runs on Sun, IBM, and HP/Apollo workstations. Depending on the configuration, X-Sim costs between $20,000 and $70,000.

Silicon Automation Systems Inc., 1630 Oakland Rd., Suite #A104, San Jose, CA 95131; (408) 437-9161. **CIRCLE 306**

POWER SOLUTIONS THAT MAKE CENTS

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EconoMods

If you thought component-level power was too expensive for your high volume, cost sensitive, applications . . . we've got good news. Vicor's new EconoMod™ family of component-level power converters offers the size and performance advantages of Vicor's megahertz power technology at prices that won't hog your budget . . . as low as $0.33 per watt in OEM quantities.

Available in over 100 popular combinations of input voltage, output voltage and output power, and sharing Vicor's "industry standard" encapsulated package, EconoMods are the economical answer to contemporary power system requirements . . . from 50 watts to kilowatts. And EconoMods feature the high power density, high efficiency, "instant expandability" and component-level flexibility that make traditional power supplies obsolete.

By standardizing on EconoMod *you can bank on saving money, space and time.*

VICOR

Traded on NASDAQ under "VICR"

CIRCLE 91

Real-Time OS Upgrade Extends Connectivity, Adds X-window Support

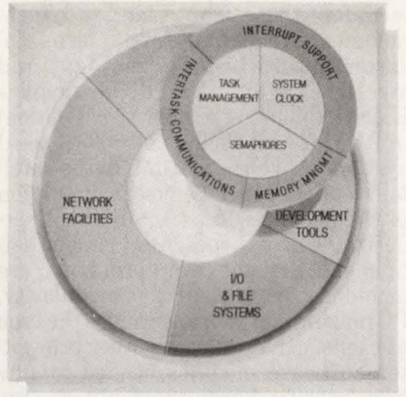
VxWorks version 5.0 is the latest release of Wind River Systems Inc.'s real-time operating system. Upwardly compatible with version 4.0.2, the software increases its kernel performance, I/O functions, connectivity support, debugging, and graphics.

The rewritten wind-kernel improvements include higher speed. Benchmarks on 25-MHz Motorola 68020-based target boards have clocked wind-context switches at 16 μs and interrupt latency at 8 μs. The software includes SLIP (serial-line interface protocol) and high-security login and remote login capabilities.

VxWorks 5.0 target configurations can range from a 60-kbyte, stand-alone, real-time kernel to a 465-kbyte full-scale development system including kernel, networking, file-system support, and development tools.

Device-independent SCSI support is combined with an MS-DOS media-compatible file system. Developers can use the ANSI C programming language in addition to a new set of internal system information utilities.

Options for VxWorks that weren't previously available include a remote



source debugger, and windX, client support for X-windows. The debugger, VxGDB, offers rehostable, retargetable source-code debugging that can simultaneously debug multiple tasks running on multiple targets.

Available now, a single-user development license costs $15,000. VxGDB costs $5000 and windX sells for $2500.

***Wind River Systems Inc.**, 1351 Ocean Ave., Emeryville, CA 94608; (415) 428-2623.* **CIRCLE 307**

■ *RICHARD NASS*

Open-System Model Lets DSP Systems Share Platforms

By creating an open-system model that DSP hardware manufacturers can incorporate in their systems, Spectron Microsystems hopes to proliferate its SPOX real-time operating system for DSP chips such as the Texas Instruments TMS320C30, the Motorola 96002, and others. The open signal-processing architecture (OSPA) defined by Spectron is an extension of the company's SPOX operating system and permits a common software platform to be shared by multiple hardware and software vendors. Thus software developed for any of a dozen C30- or 96002-based DSP cards can run on any of the cards.

With OSPA DSP software, developers can isolate the end-user application from the hardware and the real-time DSP tasks. The underlying SPOX operating system handles the DSP tasks and program developed with the OSPA guidelines call tasks from SPOX. Able to run under Microsoft's Windows 3.0 environment (X-windows by the end of this year), the OSPA model eases the development of application programs in multimedia, voice-response, process-control, and other systems. Spectron encourages three levels of third-party activity: first, DSP platform vendors must adopt the SPOX operating system; second, the independent software suppliers must "package" their DSP algorithms as SPOX applications; and third, system integrators must develop turnkey end-application programs.

To develop software for OSPA, designers must start with a DSP platform that runs the SPOX operating system and then add to it Spectron's Windows developers kit, as well Microsoft's Window's developers kit. Depending on the DSP platform, price can range from about $2500 to about $5000. A porting package for SPOX is about $18,000.

***Spectron Microsystems Inc.** 600 Ward Dr., Santa Barbara, CA 93111; Dave Wong, (805) 967-0503* **CIRCLE 308**

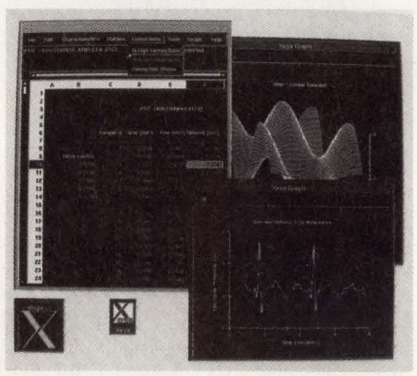
■ *DAVE BURSKY*

MODULAR BIOS FITS 80386-, 80486-BASED SYSTEMS

Release 3.1 of Award Software Inc.'s modular basic I/O system (BIOS) allows quick response to new chip sets, including those from Chips and Technologies, Headland, Intel, Texas Instruments, VLSI Technology, and Western Digital. The BIOS supplies EMS (Expanded-memory specification) in ROM for all 80486- and 80386-based systems as well as an LIM (Lotus-Intel-Microsoft) EMS 4.0 memory emulation in the same ROM as the BIOS. User-definable drive types, an expanded set-up menu, and password protection are included. Because of the modularity, PC makers can pick and choose the type of cache, drive, video, or other prewritten software modules needed to support specific hardware features. Release 3.1 is available now and costs from $70 to $80 in quantity one to upgrade from earlier versions, with significant discounts for large quantities.

Award Software Inc., 130 Knowles Dr., Los Gatos, CA 95030; (408) 370-7979. CIRCLE 309

SPREADSHEET ACCEPTS HIGH-LEVEL LANGUAGES



Engineers and scientists who require a level of computation beyond traditional spreadsheets can now turn to XESS (X-windows Engineering & Scientific Spreadsheet) from Applied Information Systems Inc. Running under Motif on Unix and VAX/VMS workstations, the software takes advantage of the speed, flexibility, and real-time data exchange that's possible in the X-windows environment.

In addition to standard spreadsheet functions, the program lets engineers quickly develop computational programs and interact with XESS by linking the XESS Connection Library to their C or Fortran programs. As calculation programs create new data, XESS can automatically incorporate the data, recalculate the spreadsheet, and display a continuously updated report. While connecting to multiple remote programs, XESS can calculate matrix, vector, and Fourier transforms, plus mathematical and statistical operations. Surface, line, histogram, and bar graphs enhance data visualization. XESS can import and export spreadsheets in WKS and WK1 formats, so that current spreadsheets can be moved to XESS and expanded.

XESS runs on X-windows workstations running X11.3 or X11.4 with Motif. It sells for $595 and will start shipping on Oct. 17.

Applied Information Systems Inc., 500 Eastowne Dr., Chapel Hill, NC 27514; (800) 654-2596 or (919) 942-7801. CIRCLE 311

RUN WINDOWS 3.0 ON 34020 AND X-WINDOWS ON A PC

Version 3.0 of DGIS (Direct Graphics Interface Standard) offers support for Microsoft Windows 3.0 and Texas Instruments' TMS34020 graphics processor. This means that, using DGIS 3.0, from Graphic Software Systems (GSS), 34010 and 34020 system developers can support Windows 3.0. Other enhancements to Version 3.0 include support for DOS extenders and virtual color maps. Because DGIS 3.0 executes on a graphics coprocessor in parallel with the system CPU, its performance is up to ten times faster than VGA controllers.

More than 600 applications can run on DGIS 3.0, including AutoCAD, Microstation, WordPerfect, Harvard Graphics, and Ventura Publisher. In addition to Windows 3.0, other graphical user interfaces are accelerated, including X-windows. Many major system makers already incorporate the DGIS system into their hardware, including Compaq, Dell, HP, and NEC. Available now, DGIS 3.0 comes with the source code and is priced on a license and royalty basis.

XVision, also from GSS, is a Microsoft Windows application that enables PC users to display multiple X-window applications alongside multiple Windows 3.0 applications. Users gain the ability to cut and paste between the two environments. XVision can be networked to various X-window hosts simultaneously over a TCP/IP network. XVision is compatible with all versions of Microsoft Windows. It's available now for $445.

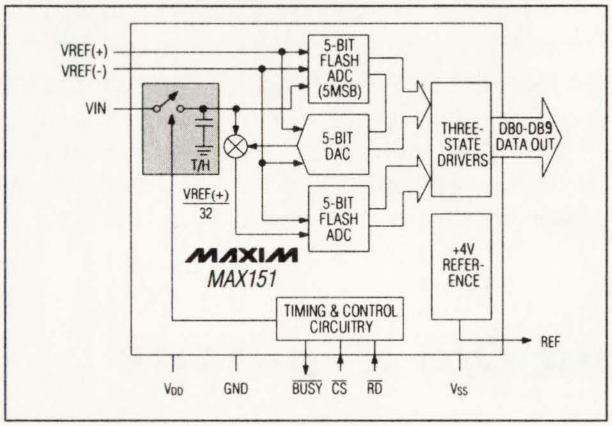
Graphic Software Systems Inc., 9590 SW Gemini Dr., Beaverton, OR 97005; (503) 641-2200. CIRCLE 312

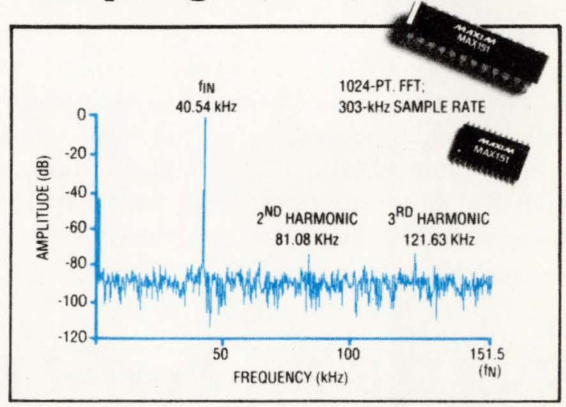
MAXIM
DESIGN NEWS
Analog Design Insights from Maxim Integrated Products

Fast 10-Bit Sampling A/D Converters Include Reference, DC and Dynamic Specs

Maxim's new 10-bit analog-to-digital converters come complete with internal voltage reference, track/hold, and clock - *saving valuable board space.* The MAX151 and MAX177 are ideal for applications such as digital-signal processing, audio and telecom processing, high-accuracy process control, electro-mechanical systems and high-speed data acquisition.

MAX151 - 300kHz/2.5µs 10-Bit Sampling A/D - $11.50*





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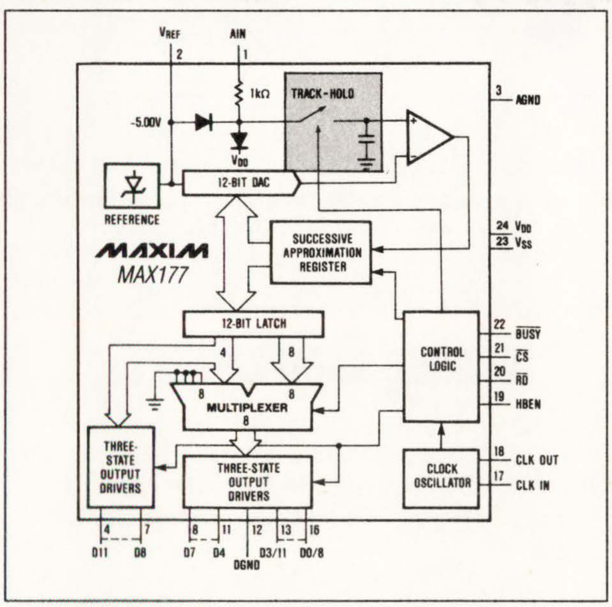
- ♦ **Internal ±60ppm/°C Voltage Reference**
- ♦ **No Missing Codes**
- ♦ **0 to +5V Input Range with ±5V Supplies**
- ♦ **5MHz Full Power Bandwidth**
- ♦ **±1ppm/°C Gain and Offset Drift**
- ♦ **Complete with Internal Track/Hold, Clock, Ref**
- ♦ **275mW Power Consumption, Including Ref**
- ♦ **Small Footprint SO and DIP Packages**

MAX177 - 100kHz/8.33µs 10-Bit Sampling A/D - $7.90*



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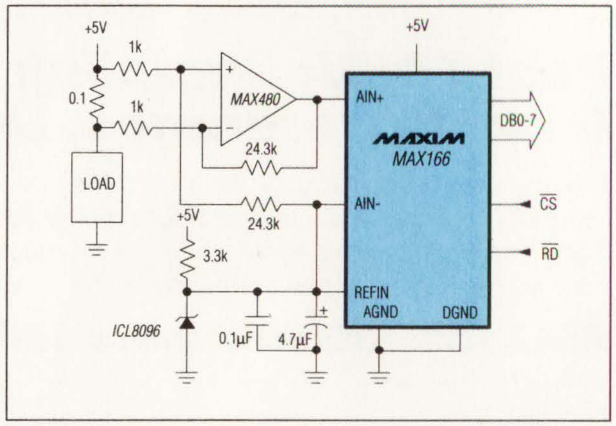
- ♦ **Internal ±40ppm/°C Voltage Reference**
- ♦ **No Missing Codes**
- ♦ **-2.5V to +2.5V Input Range**
- ♦ **6MHz Full Power Bandwidth**
- ♦ **High Input Impedance (500MΩ)**
- ♦ **Complete with Internal Track/Hold, Clock, Ref**
- ♦ **8- or 16-Wide µP Interface**
- ♦ **180mW Max Power Consumption, Including Ref**
- ♦ **Small Footprint SO and DIP Packages**

For applications that don't need the track/hold function, Maxim offers the MAX173, essentially a MAX177 but with 5µs speed, +5V input range at $7.00*.

* Price 1000-up FOB USA

8-Bit, 5µS A/D Converter with Track/Hold Accepts Differential Inputs - Only $4.90*

- ±1 LSB Total Unadjusted Error
- 50KHz Input Signal Bandwidth
- Single +5V Supply Operation
- Low 15mW Power Consumption
- 8-Bit µP Interface
- 100ns Data Access Time
- Small Footprint DIP and SO Packages

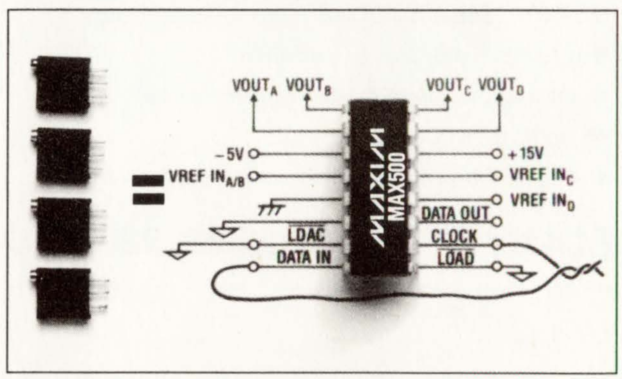


The MAX166 converts differential inputs from 0V to 2VREF using a single +5V supply. This reduces the output swing requirements on the input amplifier, and allows the converter to reject low-frequency common-mode signals. The high analog input impedence (>10MΩ) allows use of lower cost amplifiers to drive this A/D. The MAX166 is ideal for high-speed, low-power applications such as digital-signal processing, data acquistion, servo loops, data logging, telecommunications, and audio systems.

* 1000-up FOB USA

QUAD 8-Bit Serial-Input D/A Replaces Trimpots for $1.45*

- 16-Pin package reduces board space
- On-chip voltage output amplifiers ease drive requirements
- 5ppm/°C drift improves stability
- Cascadable serial interface simplifies µP connection
- Operates from single or dual supplies
- Small Footprint DIP and SO Packages



The MAX500 provides 256 digitally-programmable linear steps to digitally trim offsets, gain errors, and set trip-points. The low drift on-chip resistors and rugged latch-proof IC construction lets you free your system of trimpots. And, save both board area and cost. Applications include process control systems, automatic test equipment, and automatic calibration of system parameters such as gain and offset voltages.

* 1000-up FOB USA

★ FREE DATA SHEETS ★

MAX151 CIRCLE 71
MAX173 CIRCLE 72
MAX177 CIRCLE 73
MAX166 CIRCLE 74
MAX500 CIRCLE 75

★ FREE SAMPLES ★

For applications assistance, call (408) 737-7600, FAX (408) 737-7194 or write Maxim Integrated Products 120 San Gabriel Drive, Sunnyvale, CA 94086

14-BIT ADCS GRAB DYNAMIC SIGNALS AT 500 KHZ

A pair of high-speed 14-bit sampling and non-sampling a-d converters in 32-pin hybrid packages complement each other. The ADS-928 can continuously sample and digitize 500-kHz signals at 1 MHz with no missed codes, while the temperature varies over the commercial range. Total harmonic distortion (THD) while sampling dc to 100-kHz signals reaches -83 dB (perfection is -86 dB), which drops to -78 dB at Nyquist. (All specifications are minimums or maximums.) Signal-to-noise ratio (SNR) with and without distortion runs 72 dB and 78 dB respectively at Nyquist; it is 5 dB better from dc to 100 kHz. This represents 12 effective bit performance at Nyquist. Two-tone intermodulation distortion while digitizing a mixture of 100-kHz and 240-kHz sinewaves is -92 dB.

Acquisition time, to 0.01% accuracy, is 750 ns. Aperture uncertainty, or jitter, is just 100 ps, which reflects the device's small-signal and full-power input bandwidths--6 and 1.75 MHz, respectively. Thus signals with frequency components over 10 times Nyquist can be under-sampled. Applications for this digitally corrected sub-ranging (two-step or half-flash) machine range from spectrum, transient, vibration, and waveform analysis to imaging in radar and sonar and medical applications. The ADS-928's non-sampling cohort, the ADC-908 converter, performs a 14-bit accurate, no-missing-code conversion in 1 μs maximum over the commercial temperature range. For the military temperature range, that drops to 13 bits. Its dc specifications are similar to those of the 928. It is ideal in applications where a number of slowly varying signals must be digitized to 14-bit accuracy in a short period of time--for example, at the output of a high-speed multiplexer. Alternatively, it can be used with an external sampling amplifier and multiplexer for multiple higher frequency signals.

In quantities of 100, the commercial-grade sampling ADS-928 goes for $399 each, the non-sampling ADC-908 for $324 each.

Datel Inc., 11 Cabot Blvd., Mansfield, MA 02048; Call Bob Leonard (508) 339-3000. **CIRCLE 313**

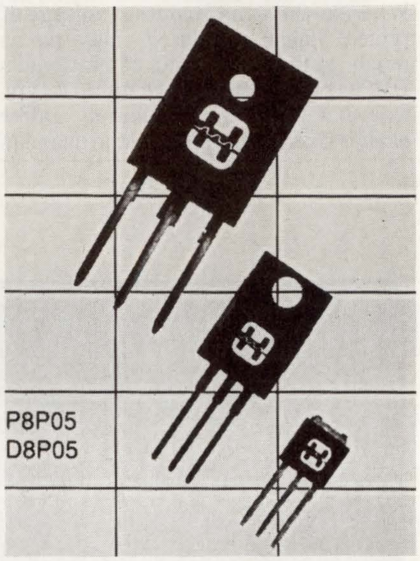
■ *FRANK GOODENOUGH*

REGULATOR LIMITS DROPOUT TO 0.5 V

Whereas the input-to-output voltage of typical linear regulators may be as much as 2 or 3 V, that of National's LM2941 low-dropout (LDO) chip is typically 0.5 V at 1 A. In addition, unlike earlier fixed-output LDOs, the user can set the LM2941's output between 5 and 20 V. The chip comes in a 5-pin TO-220 package; the fifth pin is used to turn it on or off with a logic voltage. In quantities of 100, the device is $1.15.

National Semiconductor Corp. 2900 Semiconductor DR., Santa Clara, CA 95052-8090; Hugh Wright (408) 721-5856. **CIRCLE 333**

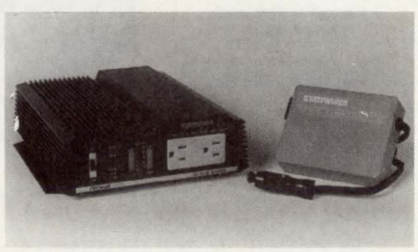
P-CHANNEL MOSFETS OFFER LOW RESISTANCE



Until now, no p-channel power MOSFETs could match the low on-resistance of n-channel devices. However, this new family of MegaFETs brings low on-resistance in 50- and 60-V devices, using over two million cells/square-inch. Moreover, the devices are ruggedized: they are the first p-channel devices with unclamped inductive-switching avalanche ratings. The process puts 15-A, 0.3-Ω, 50-V devices in a D-Pak (and surface mount D-pak); 15-A, 0.15-μ devices in a TO-220; and 30-A, 0.075-Ω devices in a TO-247. Thousand-piece pricing ranges from $0.69 each for D-Paks to $7.10 for TO-247s.

Harris Semiconductor, P.O. Box 883, Melbourne, FL 32901; 1 (800) 4 HARRIS. CIRCLE 314

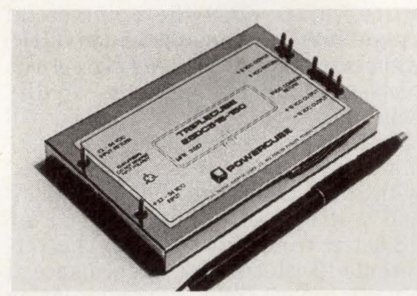
DC-TO-AC INVERTERS LIBERATE EQUIPMENT



Two dc-to-ac inverters permit ac-powered equipment to be operated from any 12-V dc source, such as an automobile battery. The Model III Pocket-Power inverter produces 200 W peak and 100 W of constant power. It measures 4.5 by 3.5 by 1.2 in. and weighs 14 ozs. The PROwatt 600 develops 500 W of continuous power and 600 W for 30 minutes. It can deliver a surge of 1500 W to operate equipment with high starting currents. The larger-output device measures 10 by 9 by 3 in. and weighs 5.25 lbs. The smaller and larger units cost $165 and $499, respectively. Call for availability.

Statpower Technologies Corp., 7012 Lougheed Hwy., Burnaby, B.C., Canada V5A 1W2; (604) 420-1585. CIRCLE 315

150-W DC-DC CONVERTER OFFERS HIGH EFFICIENCY



The first of a new family of high-density, multiple-output dc-dc switching regulator modules is available from Powercube. The 28DC515-150 features advanced integrated magnetics and control-circuit technology. It accepts a 28-V dc input per MIL-STD-704D and produces 150 W of output power at efficiencies of 80%. Other features include tight line and load regulation. In lots of 100, the converter costs $12.83. Delivery is in 10 to 14 weeks.

Powercube Corp., 8 Suburban Park Dr., Billerica, MA 01821; (508) 667-9500. CIRCLE 316

MILITARY SUPPLY IS 0.6-IN. HIGH

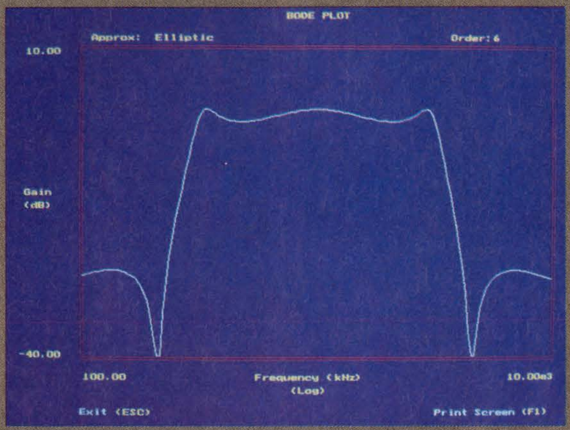
A power density of 30 W/in.^{2} and a 0.6-in profile mark the Powerboard military power supply. Two modules, which maintain component ratings within the NAVMAT-P4855 design guidelines, comprise the supply. The driver module converts an ac-input voltage to a high-voltage dc output. The device's 300-V dc output powers a triple-output dc-to-dc module. The output module delivers 5 V dc at 30 A and has two outputs rated at 15 V dc at 2 A. Typical overall efficiency is 75% under full load and nominal input voltage. The ac-to-dc module costs $450 and the dc-to-dc section goes for $1995, both in lots of 50. Delivery is in 12 to 14 weeks.

ATC Power Systems Inc., 472 Amherst St., Nashua, NH 03063; (603) 882-1366. CIRCLE 317

PSpice

MicroSim Corporation

The Standard for Circuit Simulation Has Expanded



Advanced Filter Designer Bode Plot

Advanced Filter Designer: *New* Front End Design Tool

The PSpice family of products includes both the Circuit Analysis and Circuit Synthesis packages. The Circuit Analysis package contains our PSpice circuit simulator and its options, and the Circuit Synthesis package contains our filter synthesis products, Advanced Filter Designer and Standard Filter Designer.

Advanced Filter Designer is an interactive design aid giving you the ability to design and analyze active filters. Features include a menu-driven interface, hard copy report summaries and plots, cascading multiple designs, and interfaces to PSpice and SWITCAP.

Advanced Filter Designer uses a well established methodology in applying classical approximations to your filter specification. Available filter types include low pass, high pass, band pass, and band reject, all of which may be synthesized by Butterworth, Chebyshev, Inverse Chebyshev, and Elliptic (Cauer) functions. There is also the capability to synthesize arbitrary fransfer functions and delay equalization filters.

A full editing capability allows you to insert, delete, and reorder stages, and modify coefficient values. These editing features allow a filter expert to fine tune a design, or quickly make a small modification to an existing design.

Advanced Filter Designer supports both active RC and switched-capacitor biquad filter structures. The components may be scaled or resized to center the values in preferred ranges.

Both Bode and pole-zero plots are available. Normally, you can determine the acceptability of your design by the inspection of its Bode plot. The Advanced Filter Designer plots gain, phase, and delay vs. frequency. For sampled data designs, you can plot your choice of the *s*- or *z*-domain transfer function. Pole-zero plots allow you to inspect the roots of the transfer function in either the *s*-domain or *z*-domain.

Filter Designer works with our PSpice circuit simulation package. PSpice and its options form an integrated package for the analysis of electronic and electrical circuits.

Each copy of our Circuit Analysis and Circuit Synthesis programs comes with our extensive product support. Our technical staff has over 150 years of experience in CAD/CAE, and our software is supported by the engineers who wrote it.

For further information about our Circuit Analysis or Circuit Synthesis packages, please call us at (714) 770-3022 or toll free (800) 245-3022.

20 Fairbanks • Irvine, CA 92718 USA • FAX (714) 455-0554

CIRCLE 134

Coilcraft Designer's Kits

First they save you time. Then they save you money.

These kits make it easier than ever to pick the right coils, chokes and other magnetics for your project.

Why waste hours calling around for samples or trying to wind them yourself. Coilcraft's low-cost kits put dozens of values right at your fingertips!

You not only save time on engineering. You also save money when you go into production because we stock just about all the parts in our kits at low off-the-shelf prices.

Call in today, and you can have your kit tomorrow!

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"Unicoil" 7/10 mm Tuneable Inductors
.0435 μH - 1.5 μH
49 shielded, 49 unshielded (2 of each)
Kit M102 $60

"Slot Ten" 10 mm Tuneable Inductors
0.7 μH - 1143 μH
18 shielded, 18 unshielded (3 of each)
Kit M100 $60

Surface Mount Inductors
4 nH - 33 μH
48 values (10 of each)
Kit C100 $125

Axial Lead Chokes
0.1 μH - 1000 μH
25 values (5 of each)
Kit F101 $50

Horizontal Mount Inductors
Tuneable and fixed
Inductance: 31.5 - 720nH
33 Values (6 of each)
Kit M104 $60

Common Mode Data Line Filters
Attenuation bandwidth: 15 dBm,1.5-30 mHz
DC current capacity: 100 mA
2, 3, 4 and 8 line styles (4 of each)
Kit D101 $65

Common Mode Line Chokes
Current: .25 - 9 amps RMS
Inductance: 508 μH - 10.5 mH
8 styles (2 of each)
Kit P202 $100

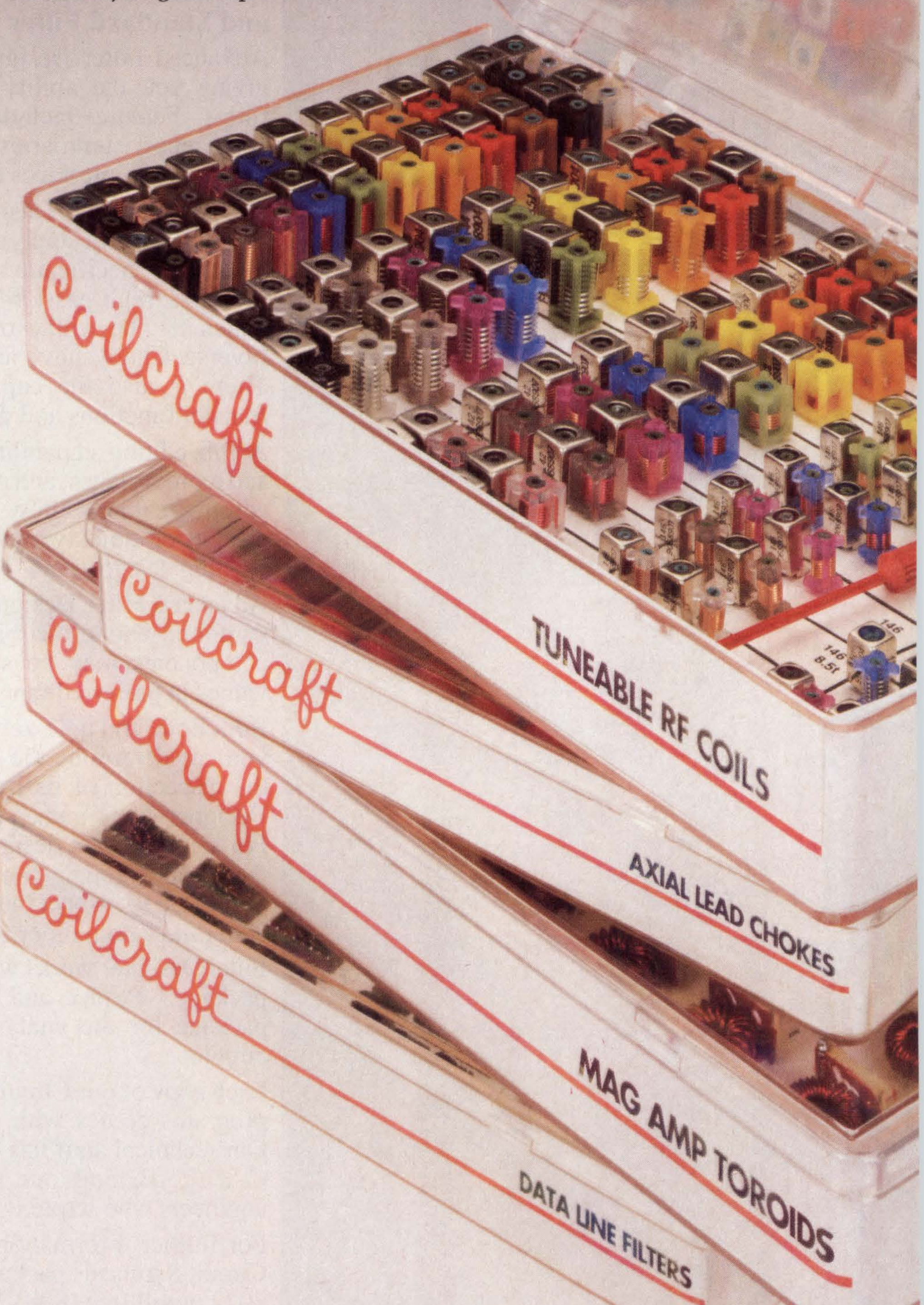
Current Sensors
Sensing range: 0.5-35 amps
Freq. resp.: 1 - 100 kHz, 50 - 400 Hz
Transformer and sensor-only versions
8 styles (15 total pieces)
Kit P203 $50

Base/Gate Driver Transformers
Inductance: 1.5 mH Min.
Frequency: 10 - 250 kHz
2 single, 2 double section (2 of each)
Kit P204 $50

Mag Amp Toroids
Current: 1, 5 amps
Volt-time product: 42 - 372 V-μsec
6 styles (2 of each)
Kit P206 $100

Power Filter Chokes
Current: 3, 5, 10 amps
Inductance: 5 - 300 μH
18 styles (48 total pieces)
Kit P205 $75

Axial Lead Power Chokes
Current: .03-4.3 amps
Inductance: 3.9 μH - 100 mH
60 styles (2 of each)
Kit P209 $150



Coilcraft

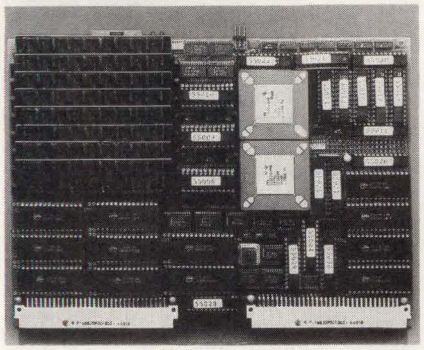
eem/electronic engineers master See our catalog in Vol. A, Section 1800

1102 Silver Lake Rd., Cary IL 60013 800/322-COIL Fax 708/639-1469

CIRCLE 90

FLOATING-POINT ARRAY PROCESSOR SUPPLIES 66 MFLOPS

Optimized for digital-signal-processing and imaging applications, the MSP-6C30 floating-point VME array processor from Analogic/CDA supplies up to 66 MFLOPS of peak processing power. The board, from Analogic/CDA, supports the company's extensive library of signal-



and image-processing functions. The board can operate as a standalone signal processor interfaced to external data-acquisition devices or as an array processor receiving control instructions from the host.

Designed in single- and dual-processor configurations, its Texas Instruments TMS320C30 32-bit digital-signal processors can function separately or together on computationally-intensive tasks, each performing simultaneous accesses on zero-wait-state memory. An optional SCSI port enables the board to connect to peripheral devices such as data-acquisition products and disk or tape drives.

Other external ports serve the VMEbus for system-wide data transfers, a general-purpose I/O that allows connection of multiple MSP-6C30 boards, and an RS-232C serial interface that's connected directly to the master processor.

Software support for the MSP-6C30 includes C and Fortran callable scientific signal-analysis and imaging subroutine libraries, an ANSI C compiler with an assembler, linker, and loader, a software simulator, and a hardware emulator with a C source-level debugger.

The standard 6U form-factor board can contain up to 1 Mbyte of static RAM and 32 Mbytes of dynamic RAM. The DRAM is configured in two banks, each with a dedicated crossbar switch. It's suited for applications requiring high throughput including communications, instrumentation, voice/speech analysis, medicine, and graphics and imaging.

Single-unit prices start at $4950 for the single-processor board. Prices for the board with dual processors start at $8450. Production quantities are available now.

***Analogic/CDA**, 8 Centennial Dr., Centennial Industrial Pk., Peabody, MA 01960; (508) 977-3030.*

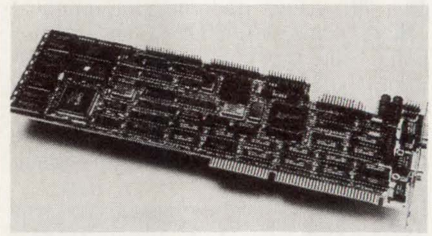
CIRCLE 318

■ *RICHARD NASS*

SUPER VGA CONTROLLER ADDS DISK CONTROLLER, SERIAL, PARALLEL PORTS

Helping users reclaim their vanishing expansion slots, the MicroPAQ 452 is a highly-integrated VGA-multifunction board that combines a Super VGA controller, a floppy/hard disk controller, and serial and parallel ports. The board, from Monolithic Systems Corp., supplies high-performance VGA graphics with EGA, CGA, Hercules, and MDA compatibility using Chips & Technologies' 82C452 video-controller chip. The card's 1 Mbyte video memory supports 256 simultaneous colors at 640 by 480 resolution, and 16 simultaneous colors at flicker-free, noninterleaved resolutions of 640 by 480, 800 by 600, 960 by 720, and 1024 by 768.

The board's IDE hard-disk interface supports up to two hard disks equipped with an embedded AT-bus interface. Its dual floppy-disk drive controller comes with a standard 34-pin ribbon cable connector and can be disabled with a jumper switch.



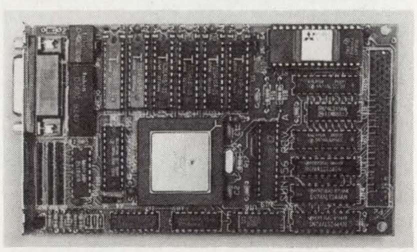
Two IBM-compatible serial ports and one bidirectional IBM PS/2-compatible parallel port are included. All three ports support printers and scanners. Three ribbon cable connectors on the 452 handle two DB9 nine-pin serial plugs and one DB25 25-pin parallel plug.

The 452 has a standard XT expansion-board form factor and can be used in any PC enclosure in 8-, 16-, and 32-bit slots with bus speeds up to 12.5 MHz.

***Monolithic Systems Corp.**, 7050 South Tucson Way, Englewood, CO 80112; (303) 790-7400.* **CIRCLE 319**

■ *RICHARD NASS*

SBUS CARD ADDS DSP POWER TO WORKSTATION



Occupying one SBus option slot, the S-56 and S-56X DSP plug-in coprocessor cards add 13.5 MIPS of processing power to Sun SparcStation workstations. The cards are based on the Motorola DSP56001 digital signal processor and include up to 192 kbytes of zero-wait-state memory and a NeXT-compatible port for serial I/O transfers. A DSP port handles synchronous transfer rates up to 6.75 Mbits/s and can be directly connected to the Ariel's previously released DM-N digital microphone for CD-quality recording and signal analysis. The S-56X enhances I/O capabilities by adding a Xilinx 3042 RAM-based programmable gate array between the DSP chip and an option connector. The PGA can be reprogrammed for multiple specialized I/O tasks. The S-56 sells for $1495; the S-56X for $1995. Software development tools include Bug-56, a symbolic debugger, the ASM-56 assembler-linker-librarian. Bundled, the software package sells for $1295.

Ariel Corp., 433 River Rd., Highland Park, NJ 08904; Les Listwa, (201) 249-2900. **CIRCLE 320**

HALF-SIZE CARD LINKS 1553B, 1750A BUSES

Occupying a short expansion slot in an IBM PC AT, a MIL-STD-1553B interface board creates a hard-wired connection between MIL-STD-1750A avionics computers and the local area networks to which they are connected. The board, designated the Shuttle, works as an on-line bus tap and can be dynamically reassigned as a bus protocol controller, remote terminal, or passive bus monitor. It is a doubly redundant LAN with 45 dB of common-mode noise rejection and a maximum bit-error rate of greater than 10^{-7}. Program development tools supplied with the board include two sets of utilities for generating communication routines for the 1553 bus. The complete development system costs $3495. Delivery is from stock to four weeks.

Sabtech Industries Inc., 3910-B Prospect Ave., Yorba Linda, CA 92686; (714) 524-3299. **CIRCLE 321**

The Emerging Standard in 574 Family 12-Bit A/D's

- **Monolithic construction**
- **Lowest power in the industry — 110mW**
- **No -15V power required**
- **25μs maximum conversion; 15μs maximum for 674**
- **Complete ADC — on-board SAMPLE/HOLD, reference, clock and tri-state output**
- **Available in surface-mount J-lead LCC and LCC**
- **Delivery from stock**

For a data sheet, pricing or samples, call **Sipex** direct at **1-800-272-1772**.

Sipex

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Billerica, MA 01821
800-272-1772
508-663-9691
FAX: 508-670-9001

CIRCLE 151

INPUT FLEXIBILITY AIDS DATA-ACQUISITION UNITS

A pair of data-acquisition instruments offer users the choice between a stand-alone unit and an instrument for use with PC-based systems. Both the 2620A data-acquisition unit and 2625A data logger accept a wide variety of signals on 21 analog input and 12 digital I/O channels. They can be configured by front-panel controls or through a standard RS-232C or optional IEEE-488 interface. The stand-alone 2625A has a nonvolatile data memory for over 200 scans.

The instruments work with most sensors and transducers, including thermocouple, dc-voltage, ac-voltage (true-rms), frequency, and resistance types, with a maximum input of 300 V. No signal conditioning is needed as measurements are filtered and linearized at up to 18 reading per second. Both units feature alarm limits; linear scaling; minimum, maximum, and last memory; automatic print output; battery-backed clock and program; conditional scan triggers; and universal ac or 9-16-V dc operation.

Included software supplies setup instructions and monitors and stores readings on a PC in real-time, where it can be input into popular spreadsheet programs. The software also retrieves readings stored in the 2625A's memory. Also standard is Laboratory Technologies' Acquire data-collection software. Optional software includes Labtech Notebook for advanced data manipulation and analysis, a driver for National Instrument's LabWindows, Fluke's TesTeam for systems applications, and Fluke's QuickLog package.

Model 2620A costs $1990 and model 2625A goes for $2690. Both are available starting November 1 on a 4-week delivery schedule.

John Fluke MFG. Co. Inc., P.O. Box 9090, Everett, WA 98206-9090; (206) 347-6100. CIRCLE 322

■ *JOHN NOVELLINO*

ICE COMMUNICATES WITH HOST COMPUTER

An in-circuit emulator for ROM code development is built around an intelligent microcontroller that can communicate with the host processor, perform self-testing, and upload as well as download data. Called the PROMICE, the unit emulates any 24-, 28-, or 32-pin Jedec ROM of up to 8 Mbits using only standard cables. An optional Analysis Interface module allows bidirectional communication between the host computer and the software (debugger) running in the target system without the need to modify the target. Data signals downloaded to the PROMICE can be loaded over a serial RS-232-C link at baud rates of up to 57.6 kbaud or over an optional parallel link for even faster loading. Prices start at $495 for a simplex unit that emulates one 256-kbit ROM. Duplex units start at $790.

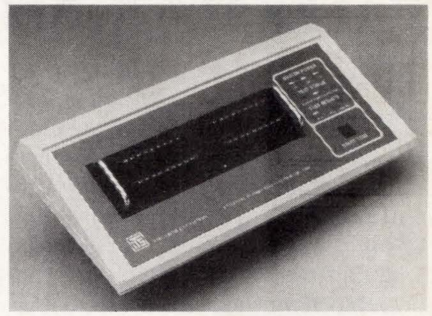
Grammar Engine Inc., 3314 Morse Rd., Columbus, OH 43231; (614) 471-1113. CIRCLE 332

ARBITRARY GENERATOR HAS INTERNAL TRIGGER

A synthesized 20-MHz arbitrary-waveform generator features a built-in trigger generator and up to 128 ksamples of waveform memory. The model 95 operates in noncontinuous modes (trigger, gate, and burst) and features burst counts to 1 million cycles. Range is 1 MHz to 20 MHz with 0.001% accuracy and automatic calibration. The model 95 prices start at $4495, with 4-weeks delivery.

Wavetek San Diego Inc., 9045 Balboa Ave., San Diego, CA 92123; (800) 874-4835. CIRCLE 324

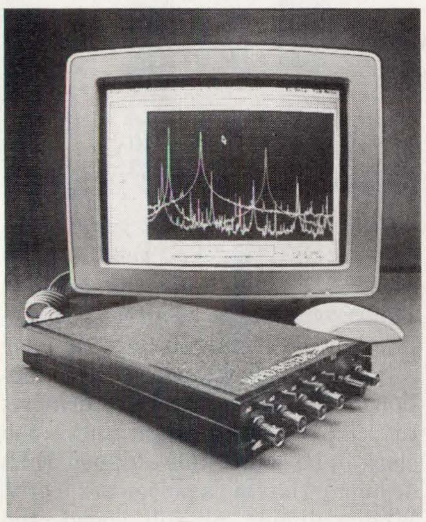
MEMORY TESTER CHECKS ACCESSES TO 300 NS



Even though it is simple to operate and easy to install, a PC-based memory tester is powerful enough to perform all the engineering tests needed to inspect dynamic and static RAMs, ROMs, EPROMs, and EEPROMs in any configuration from 16 kbits to 16 Mbytes. The Model 1000 checks access times ranging from 25 to 300 ns and uses industry-standard data and address test patterns. Even if the testing parameters for the memory device under test are unknown, the instrument's software can determine them automatically. The unit's test adapter handles up to eight devices at a time with programmable voltage cycling performed individually on each device. Adapters are available to accommodate virtually any memory device. The price of the Model 1000 is less than $4000, including system software.

Integrated Test Systems, 21621 Kerry Ct., El Toro, CA 92630; (714) 586-0332. CIRCLE 326

PC-BASED ANALYZER DOES FFTS TO 250 KHZ



An IBM PC-based spectrum analyzer add-on offers real-time fast Fourier transform analysis up to 250 kHz on two channels simultaneously. The unit, an external box, supplies a split-screen display of both frequency and time representations. Users can average from two to 1024 waveforms on both channels simultaneously.

Sample rates from 1 Hz to 500 kHz are available, and the instrument has 32-kword/channel data buffers, full digital and analog triggering, and can be set with programmable gains. Gain ranges are from 10 mV to 50 V per division, and frequency and amplitude scaling can be either linear or logarithmic. Included is mouse-driven EGA/VGA color software. The R310 is priced at $1995.

Rapid Systems Inc., 433 N. 34th St., Seattle, WA 98103; (206) 547-8311. CIRCLE 323

COMMUNICATIONS TESTER HANDLES FDDI, SONET

Operating at up to 700 MHz, the CSA 907 bit-error-rate tester is designed to facilitate testing to both the fiber distributed data interface (FDDI) and synchronous optical network (SONET) standards. The unit supplies 32-kbit RAM words for FDDI/SONET pattern simulations, which meets pattern-length requirements of both standards. The CSA 907 consists of two portable units, the CSA 907T pattern generator and the CSA 907R error detector. The CSA 907 costs $38,995 and is available 6 to 8 weeks after receipt of an order. Separately, the 907T pattern generator and 907R error detector go for $21,995 and $20,555, respectively.

Tektronix Marketing Communications Dept., P.O. Box 1700, Beaverton, OR 97077; (800) 426-2200. CIRCLE 325

EMBEDDED CONTROL VERSION OF 68000 PACKS DMA, SERIAL I/O, AND MORE

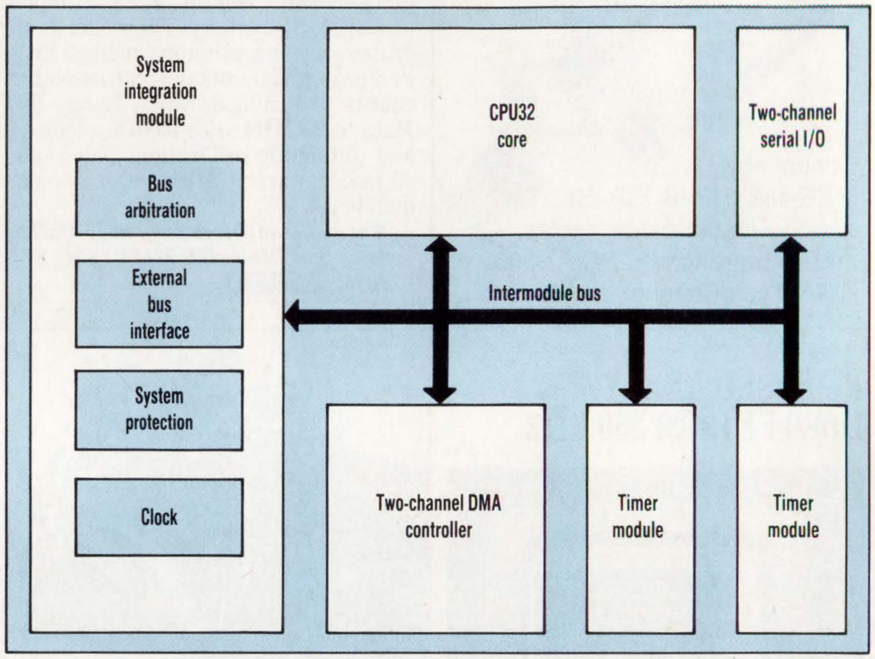
DAVE BURSKY

Designed to tackle many of the most demanding embedded-control applications, the 68340 microprocessor combines a 68000-family central processor core along with dual 32-bit DMA channels, dual serial channels, and a pair of counter-timers. Based on the same static CMOS logic processor core Motorola developed for the previously-released members of the 68300 family, the 68340 is upward object-code compatible with the 68000 and 68010 microprocessors.

Thus, although the core can execute existing 68000 and 68010 object code, several new instructions were added to simplify embedded-control applications. And, to simplify testing, a JTAG-compatible (IEEE 1149.1) test port is also included on the chip. Some of the main application areas envisioned for the 68340 include I/O processing such as in disk drives, networks, imaging systems (laser printers, fax cards, etc.), intelligent terminals (X-window, 3270), portable and handheld computers, and the control of multimedia systems such as compact-disk interactive systems.

In addition to the DMA, serial ports and timers, the processor contains another major block that handles many of the general system functions—clock generation, bus arbitration, system protection (watchdog timers and various signal monitors), and bus interface (control) logic. A programmable bus sizing capability permits both 8- and 16-bit peripherals to be attached to the host interface bus.

When operating at its maximum frequency of 16.78 MHz, the 68340 can deliver approximately three times the throughput of the original 68000 microprocessor running at the same clock frequency. Furthermore, the on-chip 32-bit DMA controllers can transfer data at rates of up to 33 Mbytes/s, thanks to the elimination of the overhead required by the CPU core to switch between the data-processing and data-transfer modes.



The twin serial channels on the chip are compatible with the popular 2681 full-duplex asynchronous/synchronous serial data communications chip. Each channel has a quadruple-buffered receiver and a double-buffered transmitter. Baud rates are independently programmable for each receiver and transmitter. There are 19 fixed rates from 50 to 76.8 kbits/s. By selecting a X1 clock instead of the standard X16 clock, data rates of up to 2 Mbits/s are also possible.

The dual programmable timers are 16-bits long, each with an 8-bit prescaler. Each timer can also be set to perform event counting, period and pulse-width measurement, input capture, output comparison, waveform generation, and pulse generation. Additionally, there are seven maskable interrupt conditions available for each of the programmable timers.

By using an on-chip phase-locked loop and a voltage-controlled oscillator, the 68340 can employ a low-frequency (32-kHz) crystal to generate the 16.78-MHz on-chip clock frequency. The PLL permits the internal clock frequency to be altered on-the-fly, thus permitting the programmer to tailor the chip's power consumption to the application. Furthermore, the chip's static design allows the clock to be completely stopped, thus dropping the chip's power to 2.5 mW. When running at full speed, the 68340 microprocessor draws about 800 mW.

Also coming from Motorola's Austin-based operation is a stripped-down version of the chip that contains only the processor core. That chip, the 68331, will be sampled next quarter.

Samples of the 68340 processor, which can be obtained in either a 144-lead ceramic quad flat package or a 145-pin plastic pin-grid array, are immediately available. In 1000-unit lots, the chip will sell for less than $50.

Motorola Inc., Microprocessor Products Group, 6501 William Cannon Dr. West, Austin, TX 78735-8598; (512) 891-2140.

CIRCLE 328

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Designed specifically for address decoding, a very-wide-input decoder packs 36 input lines, 10 dedicated output lines and 12 additional programmable I/O lines. Fabricated in an advanced bipolar process the PHD48N22-7 can decode up to a 48-bit bus pattern (by using the 12 I/O lines as additional inputs) in just 7.5 ns from input to output (through the AND logic), making the chip the fastest wide decoder available from any company. Four of the 12 bidirectional I/O lines also serve as OR logic outputs, and three of those four provide 7 product terms; the fourth line has 12 product terms. The wide decoder is available in production quantities, and the plastic-housed leaded-chip-carrier version sells for $22 in 1000-unit lots.

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SIX-CHIP BICMOS GATE-ARRAY FAMILY OPERATES AT 210 MHZ

A second-generation family of arrays, the Q24000 series from Applied Micro Circuits, includes six base chips that contain 800 to about 28,000 equivalent gates. Their maximum operating frequency of 210 MHz is the highest for a commercial biCMOS array family.

The arrays' internal logic cells contain 8 p- and 8 n-channel devices plus two pairs of bipolar totem-pole structures for use as line drivers. As a result, large macros such as multiplexers, flip-flops, and demultiplexers can fit in just one cell. Basic gates have a loaded propagation delay (fanout of 2 and 2 mm of wiring) of about 400 ps, with the delay increasing by 25 ps for each additional fanout.

I/O cells that surround the core can be configured for CMOS, ECL or TTL levels and can drive loads of up to 48 mA. The arrays contain 44 to 256 I/O pads. An additional 8 to 112 pads are available for power and ground connections. Power consumption ranges from 500 mW to about 9 W, depending on gate utilization, operating frequency, and package type.

Commercial- and military-temperature-range versions of the arrays are available. Design support for the arrays includes the company's MicroMatrix cell library and software tools. NRE charges range from \$5 to \$15/gate when the customer supplies a netlist. Production prices for commercial versions range from \$0.0075 to \$0.04/gate, depending on array size, package type, and screening level.

***Applied Micro Circuits Corp.**, 6195 Lusk Ave., San Diego, CA 92121; Marc Friedman, (619) 450-9333.*

CIRCLE 330

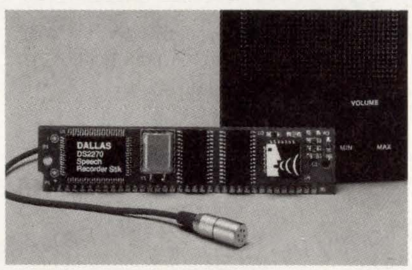
■ *DAVE BURSKY*

RECORD AND PLAYBACK HIGH-QUALITY SOUND FROM A SOLID-STATE RECORDER

A solid-state tape recorder from Dallas Semiconductor can reproduce high-fidelity sound at bit rates as low as 8 kbits/s. The DS2270 Speech Recorder Stik decreases size and improves durability over mechanical tape-based techniques.

Telephone-grade speech normally consumes 64 kbits/s, a rate that's too costly to store in semiconductor RAM. Using digital compression techniques, the standard for quality sound reproduction has been 32 kbits/s. But Dallas Semiconductor has reduced that number by 75% with an advanced speech-compression algorithm. This lower bit rate makes it feasible to store speech in silicon rather than rotating magnetic media.

The DS2270 converts analog sound to digital data at a rate of 64 kbits/s. A second computer mounted on the same chip stores the data in nonvolatile SRAM and keeps track of the messages. Forty of the chip's 64 kbytes of nonvolatile SRAM can store about 40 seconds of speech at 8 kbits/s. Extra memory can be attached to increase the amount of recordable speech. At 8 kbits/s, an hour-long conversation could be recorded and stored in less than 4 Mbytes of memory.



The key components of the recorder are available as a chip set specifically designed for incorporation into a PC. The chip set consists of a voice message processor for compressing speech, a dual digital potentiometer for adjusting volume settings, and a chip that interfaces directly to the computer's data bus. To complete the configuration, a small amount of EPROM or SRAM and a CODEC (for voice digitization) are needed. Available from stock, the DS2270 Speech Recorder Stick sells for \$96.25 in 500-piece quantities. The chip set containing the Stik's key components is priced at \$18 in quantities of 10,000.

***Dallas Semiconductor**, 4350 Beltwood Pkwy., Dallas, TX 75244.* **CIRCLE 331**

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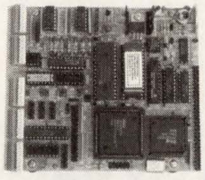

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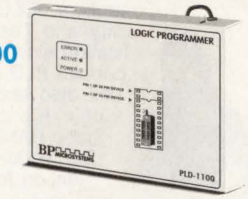

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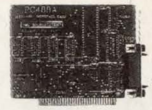

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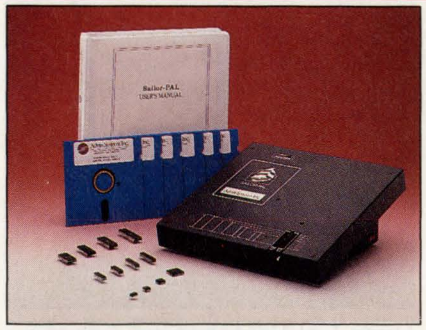

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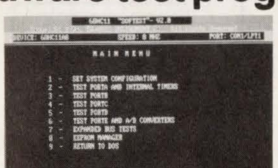

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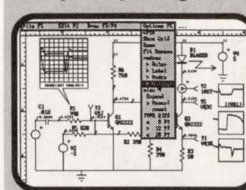

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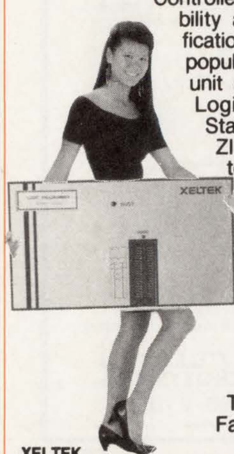

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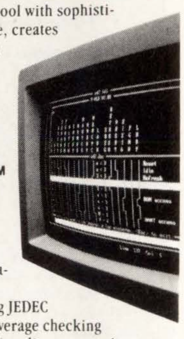

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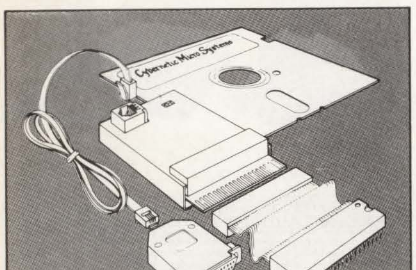

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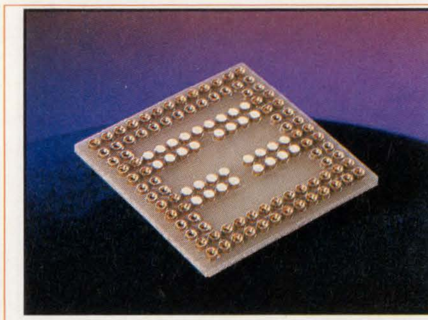

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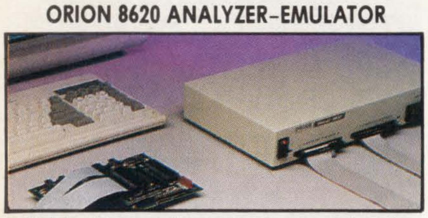

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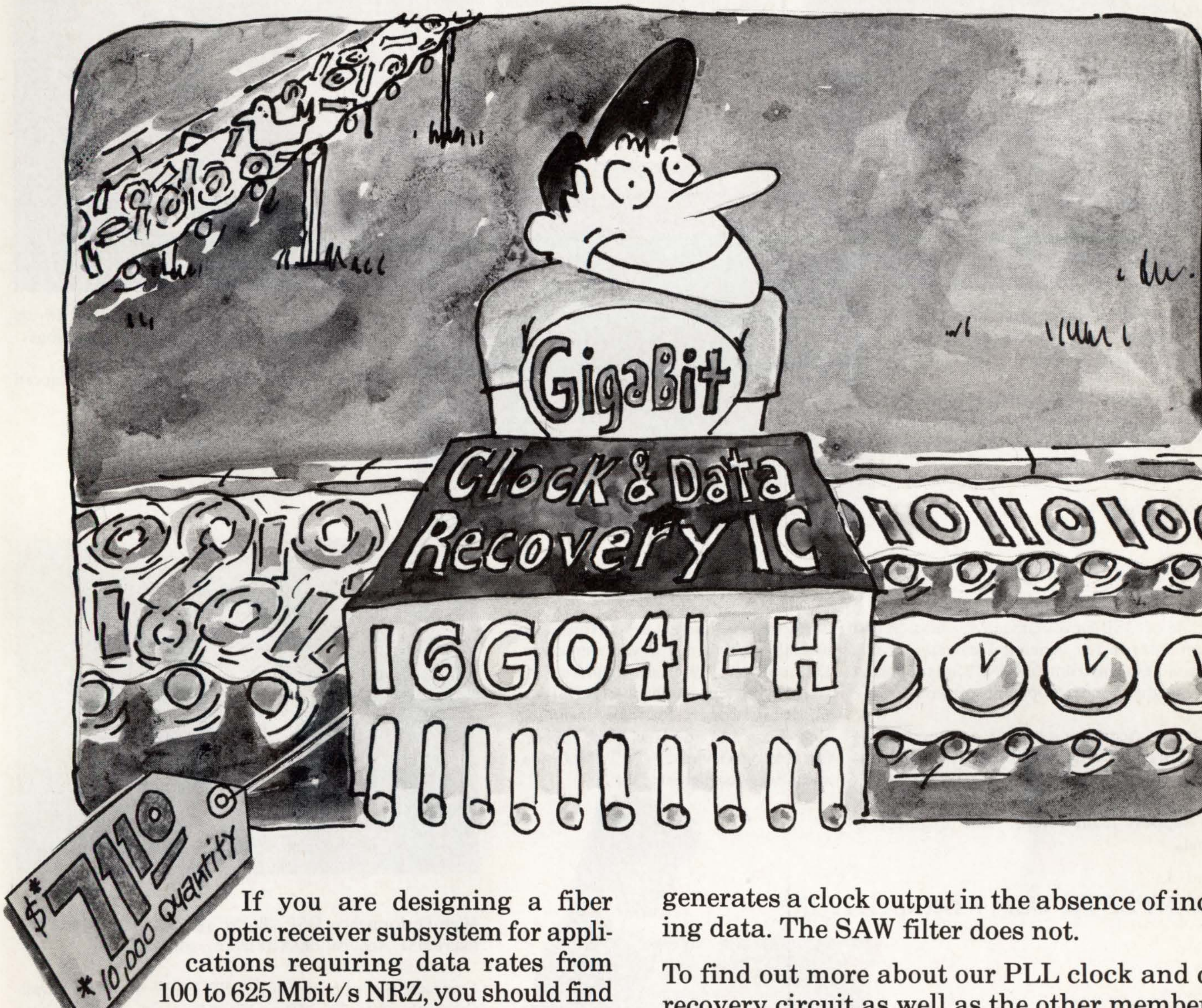

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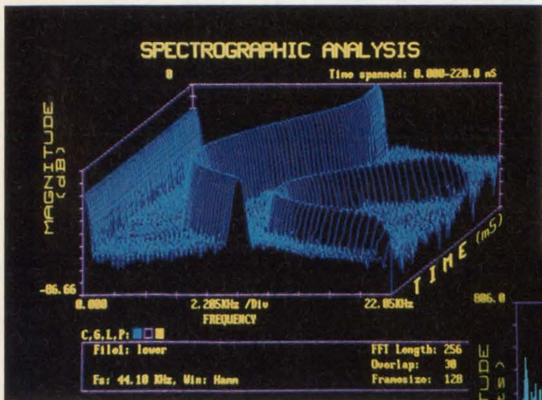

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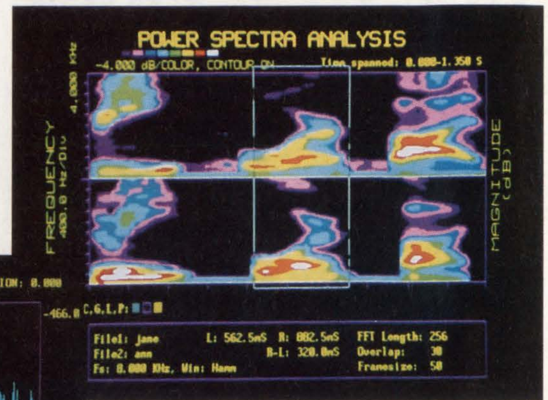

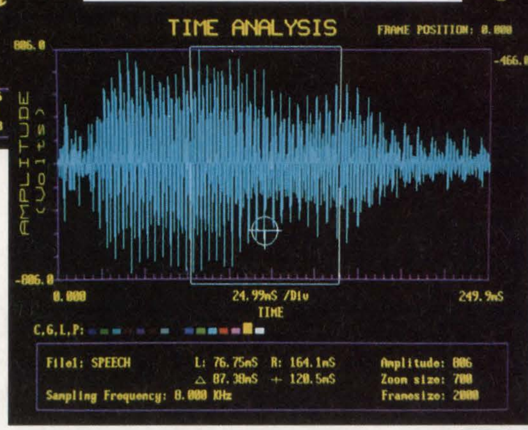

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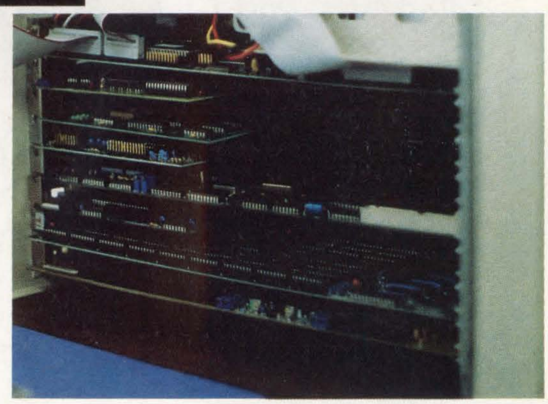

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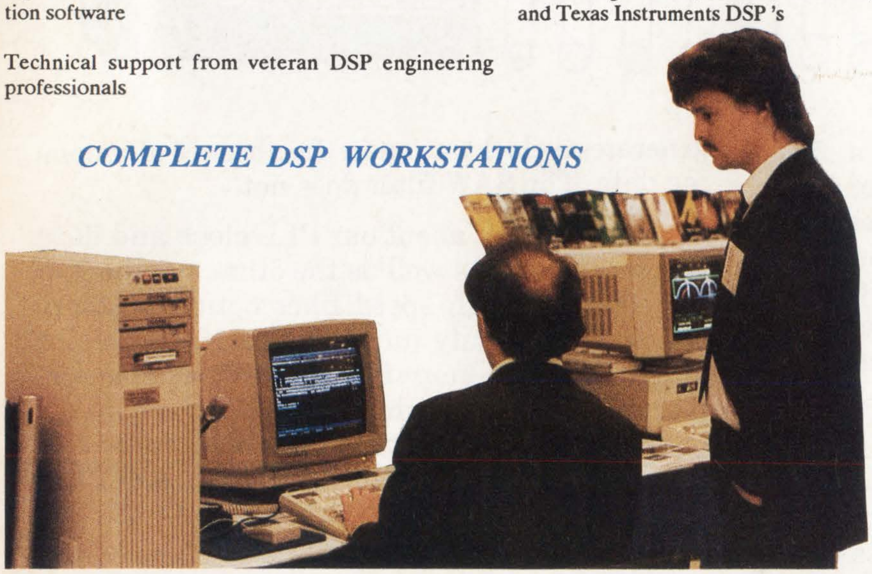

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